National Semiconductor

400023

Advanced Peripherals

Graphics Handbook

A Corporate Dedication to Quality and Reliability

National Semiconductor is an industry leader in the manufacture of high quality, high reliability integrated circuits. We have been the leading proponent of driving down IC defects and extending product lifetimes. From raw material through product design, manufacturing and shipping, our quality and reliability is second to none.

We are proud of our success . . . it sets a standard for others to achieve. Yet, our quest for perfection is ongoing so that you, our customer, can continue to rely on National Semiconductor Corporation to produce high quality products for your design systems.

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

Wir fühlen uns zu Qualität und Zuverlässigkeit verpflichtet

National Semiconductor Corporation ist führend bei der Herstellung von integrierten Schaltungen hoher Qualität und hoher Zuverlässigkeit. National Semiconductor war schon immer Vorreiter, wenn es galt, die Zahl von IC Ausfällen zu verringern und die Lebensdauern von Produkten zu verbessern. Vom Rohmaterial über Entwurf und Herstellung bis zur Auslieferung, die Qualität und die Zuverlässigkeit der Produkte von National Semiconductor sind unübertroffen.

Wir sind stolz auf unseren Erfolg, der Standards setzt, die für andere erstrebenswert sind. Auch ihre Ansprüche steigen ständig. Sie als unser Kunde können sich auch weiterhin auf National Semiconductor verlassen.

La Qualité et La Fiabilité:

Une Vocation Commune Chez National Semiconductor Corporation

National Semiconductor Corporation est un des leaders industriels qui fabrique des circuits intégrés d'une très grande qualité et d'une fiabilité exceptionelle. National a été le premier à vouloir faire chuter le nombre de circuits intégrés défectueux et a augmenter la durée de vie des produits. Depuis les matières premières, en passant par la conception du produit sa fabrication et son expédition, partout la qualité et la fiabilité chez National sont sans équivalents.

Nous sommes fiers de notre succès et le standard ainsi défini devrait devenir l'objectif à atteindre par les autres sociétés. Et nous continuons à vouloir faire progresser notre recherche de la perfection; il en résulte que vous, qui êtes notre client, pouvez toujours faire confiance à National Semiconductor Corporation, en produisant des systèmes d'une très grande qualité standard.

Un Impegno Societario di Qualità e Affidabilità

National Semiconductor Corporation è un'industria al vertice nella costruzione di circuiti integrati di altà qualità ed affidabilità. National è stata il principale promotore per l'abbattimento della difettosità dei circuiti integrati e per l'allungamento della vita dei prodotti. Dal materiale grezzo attraverso tutte le fasi di progettazione, costruzione e spedizione, la qualità e affidabilità National non è seconda a nessuno.

Noi siamo orgogliosi del nostro successo che fissa per gli altri un traguardo da raggiungere. Il nostro desiderio di perfezione è d'altra parte illimitato e pertanto tu, nostro cliente, puoi continuare ad affidarti a National Semiconductor Corporation per la produzione dei tuoi sistemi con elevati livelli di qualità.

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

GRAPHICS
DATABOOK

1988 Edition

Advanced Graphics Chipset

Application Notes

Physical Dimensions/Appendices

1
2
3

TRADEMARKS

Following is the most current list of National Semiconductor Corporation's trademarks and registered trademarks.

AbuseableTM
AnadigTM
ANS-R-TRANTM
APPSTM
Auto-Chem DeflasherTM
BCPTM
BI-FETTM
BI-FET IITM
BI-LINETM
BIPLANTM
BLCTM
BLXTM
Brite-LiteTM
BTLTM
CheckTrackTM
CIMTM
CIMBUSTM
Clock✓ChekTM
COMBOTM
COMBO ITM
COMBO IITM
COPSTM microcontrollers
Datachecker®
DENSPAKTM
DIBTM
Digitalker®
DISCERNTM
DISTILLTM
DNR®
DPVMTM
ELSTARTM
E-Z-LINKTM
FACTTM
FASTTM
5-Star ServiceTM
GAL®
GENIXTM
GNXTM
HEX 3000TM
HPCTM
ICMTM
INFOCHEXTM
Integral ISETM
IntelisplayTM
ISETM
ISE/06TM
ISE/08TM
ISE/16TM
ISE32TM
KeyScanTM
LMCMOSTM
M²CMOSTM
MacrobusTM
MacrocomponentTM
Meat✓ChekTM
Microbus™ data bus
MICRO-DACTM
μtalkerTM
MicrotalkerTM
MICROWIRETM
MICROWIRE/PLUSTM
MOLETM
MSTTM
Naked-8TM
National®
NAX 800TM
Nitride PlusTM
Nitride Plus OxideTM
NMLTM
NOBUSTM
NSC800TM
NSX-16TM
NS-XC-16TM
NURAMTM
OXISSTM
P²CMOSTM
Perfect WatchTM
Pharma✓ChekTM
PLANTM
PMPTM
PolycraftTM
POSitalkerTM
Power & ControlTM
QUAD3000TM
QUIKLOOKTM
RATTM
RTX16TM
SABRTM
Script✓ChekTM
SCXTM
SERIES/800TM
Series 3000TM
Series 32000®
Shelf✓ChekTM
SPIRETM
STARTM
Starlink™
STARPLEXTM
STARPLEX IITM
SuperChipTM
SuperScriptTM
SYS32TM
TapePak®
TDSTM
TeleGateTM
The National Anthem®
Time✓ChekTM
TINATM
TLCTM
TrapezoidalTM
TRI-CODETM
TRI-POLYTM
TRI-SAFETM
TRI-STATE®
TURBOTRANSCEIVERTM
VIPTM
VR32TM
WATCHDOGTM
XMOSTM
XPUTM
Z STARTM
883B/RETSTM
883S/RETSTM

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation 2900 Semiconductor Drive, P.O. Box 58090, Santa Clara, California 95052-8090 (408) 721-5000
TWX (910) 339-9240

National Semiconductor

Introduction

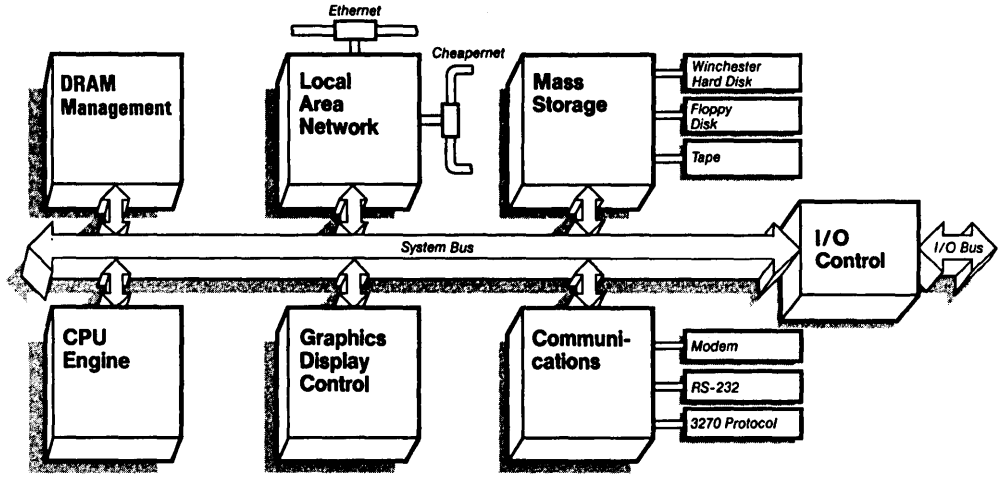
National Semiconductor's graphics and imaging products include complex VLSI peripheral circuits designed to serve a variety of applications. These products are especially well suited for microcomputer and microprocessor systems such as workstations, terminals, personal computers, and many others.

GRAPHICS

Sophisticated human interface is the mark of the newest computer systems. Today's personal computer may have better graphics display capability than engineering workstations of a few years ago. National Semiconductor has developed a new family of Advanced Graphics products to provide extremely high performance, high resolution monochrome or color graphics displays. The graphics chip set is designed to provide the highest level of performance without placing constraints on the overall system design or performance. Flexibility is as important as is overall performance. That flexibility is provided by the partitioned functionality, modular building block approach, open architecture, programmability of all components and the ability to address the frame buffer in a planar (parallel) mode or in a pixel-wise mode. The graphics system may be expanded to any number of color planes with virtually unlimited resolution. The Graphics Databook provides all of the details to make display system design easy.

National Semiconductor

Introduction Advanced Peripherals



TL/XX/0058-1

National Semiconductor Advanced Peripherals products include complex VLSI peripheral circuits designed to serve a variety of applications. The Advanced Peripherals products are especially well suited for microcomputer and microprocessor systems such as graphics workstations, personal computers, and many others. National Semiconductor Advanced Peripherals devices are fully described in a series of databooks and handbooks.

Among the Advanced Peripherals books are the following titles:

MASS STORAGE

The National Semiconductor family of mass storage interface products offers the industry's highest performance and broadest range of products for Winchester hard disks and floppy disks. The Mass Storage Handbook includes complete product information and datasheets as well as a comprehensive design guide for disk controller systems.

MEMORY SUPPORT

Today's large Dynamic Random Access Memory (DRAM) arrays require sophisticated high performance devices to provide timing access arbitration on board drive and control. National Semiconductor offers the broadest range of DRAM controllers with the highest "No-waitstate" performance available on the market. Controllers are available in Junction Isolated LS, Oxide Isolated ALS, and double metal CMOS for DRAMs from 64k bit through 4M bit devices, supporting memory arrays up to 64 Mbyte in size with only one LSI/VLSI device. For critical applications, National Semiconductor has developed several 16- and 32-bit Error Checking and Correction (ECC) devices to provide maximum data integrity. The Memory Support Handbook contains complete product information and several application notes detailing complete memory system design.

LOCAL AREA NETWORKS AND DATA COMMUNICATIONS

Today's computer systems have created a hugh demand for data communications and Local Area Networks (LANs). National Semiconductor supplies a broad range of products to fill these needs. The IEEE 802.3 Standard for Ethernet/Cheapernet LANs is one of the most popular solutions. National Semiconductor provides a complete three-chip solution for an entire 802.3 design. For IBM 370 class mainframe and system 34/36/38 peripheral connectivity, National offers a completely integrated solution. For the physical layer front end transceiving and processing of the IBM 3270/3299 "coaxial" and IBM 5250 "twinaxiar" protocols. To drive the communications lines, National Semiconductor has drivers and receivers designed to meet all the major standards such as RS-232, RS-422, and RS-485. Datasheets and applications information for all these products are in the LAN/DATA COMM Handbook.

GRAPHICS

Sophisticated human interface is a mark of the newest computer systems designs. Today's personal computer may have better graphics display capability than engineering workstations of a few years ago. National Semiconductor has developed a new family of Advanced Graphics products to provide extremely high performance, high resolution color graphics displays. The graphics chip set is designed to provide the highest level of performance with minimum demands and loading on the system CPU. The graphics system may be expanded to any number of color planes with virtually unlimited resolution. The Graphics Databook lays it all out and makes the display system design easy.

National Semiconductor

Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

National Semiconductor Corporation reserves the right to make changes without further notice to any products herein to improve reliability, function or design. National does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

Table of Contents

Alpha-Numeric Index

Section 1

Advanced Graphics Chipset

Section 1 Contents

National Semiconductor

PRELIMINARY

DP8500 Raster Graphics Processor

General Description

National's DP8500 Raster Graphics Processor (RGP) is a microprocessor specifically tuned for graphics applications. A member of the Advanced Graphics Chip Set, it provides the set of functions required for display buffer update and video refresh in mid-to-high-performance color or monochrome raster graphics systems employing both graphics primitives and text. The RGP combines the following elements: a general-purpose microcoded microprocessor, a programmable video refresh generator, a vector generator, a BITBLT controller and a rectangular clipper. As such, it may be used in standalone applications or as a dedicated graphics engine in conjunction with any general-purpose microprocessor.

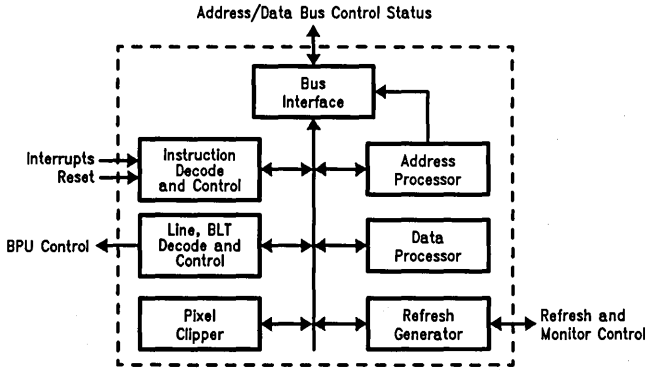
The RGP supports a system architecture that features constant drawing speed, measured in pixels/second, independent of the depth (number of bits) of the pixel. This key feature arises from the RGP's use of an external data path device, the BITBLT Processing Unit (BPU), for all drawing functions. By employing a BPU on each plane of memory, the traditional "bottleneck" is removed from the data manipulation path. In effect, the data bus width (for drawing purposes) is made proportional to the pixel depth, thus preserving the drawing speed as pixel depth is increased from one bit to any number of bits.

During video refresh, the RGP produces all synchronization and blanking signals for CRT displays and generates memory cycles, appropriate for the type of memory used, on behalf of the video shift registers. Any type of memory may be used: SRAM, DRAM or video RAM. In addition, the RGP supports the use of fast access modes in dynamic RAMS, such as page mode or static column mode.

Features

- 20 MHz operation
- Large, uniform address space
  - 28-bit bit (pixel) address
  - 24-bit word address
  - 16-bit data bus
  - Program, data, and display memories can reside anywhere
- Flexible bus interface
  - Processor independent
  - Conventional HOLD/HLDA mechanism
- Large drawing space
  - Up to 16384 by 16384 pixels per bitmap
  - Pixels of any depth
- Dedicated graphics hardware
  - Vector generator
  - Line pattern generator
  - BITBLT controller
  - Rectangular clipper
- Efficient text support
  - Character size to 256 by 256 pixels
  - Multiple fonts/sizes
  - Proportional spacing
- Programmable video refresh
  - Can be disabled for laser printer applications
  - Pixel rates to 250 MHz and beyond
  - Display formats to 65536 pixels by 4096 scan lines
  - Interlaced or non-interlaced
  - Genlock support
- microCMOS technology
- 68-lead PLCC package

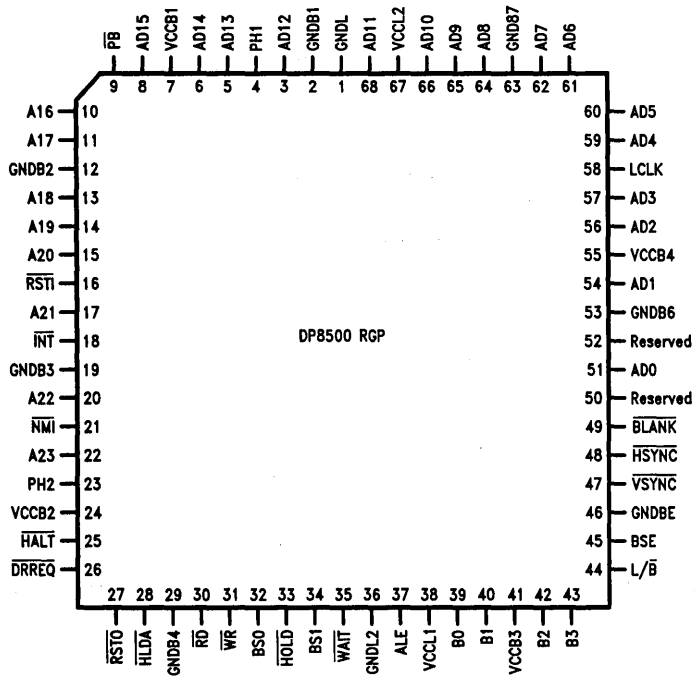
Block Diagram



TL/F/9427–1

Connection Diagram

Plastic Chip Carrier



TL/F/9427–2

Order Number DP8500V
See NS Package Number V68A

Pin Descriptions

Pin	Description
SUPPLIES	
VCCL1–VCCL2	Positive supply for internal logic: 5 Vdc ±10%.
GNDL1–GNDL2	Ground for internal logic.
VCCB1–VCCB4	Positive supply for on-chip buffers: 5Vdc ±10%.
GNDB1–GNDB7	Ground for on-chip buffers.
INPUTS	
PH1	Phase 1. PH1 is an MOS-level clock normally provided by the VCG. It must have no overlap with the PH2 clock.
PH2	Phase 2. PH2 is an MOS-level clock normally provided by the VCG. It must have no overlap with the PH1 clock.

Pin	Description
INPUTS (Continued)	
LCLK	Load Clock. LCLK is a TTL-compatible clock normally supplied by the VCG's LCLK0. It provides the basic time unit used in the registers that specify digitally the video refresh functions: sync, blanking and display-refresh bus cycles.
$\overline{\text{RSTI}}$	Reset In (active low) $\overline{\text{RSTI}}$ is used to place the RGP into the reset state; this is typically done at power-up. $\overline{\text{RSTI}}$ must be active for a minimum of 16 clock cycles.
$\overline{\text{WAIT}}$	Wait (active low). $\overline{\text{WAIT}}$ is used to cause the RGP to insert one or more wait states into the current bus cycle. This mechanism can be used to accommodate the RGP to relatively slow memory devices; it can also serve as a bus-not-ready indication from a bus arbiter. $\overline{\text{WAIT}}$ is sampled at the end of the second-last T-state or of any wait state to determine whether the next state should be the last T-state or a wait state.

Pin Descriptions (Continued)

Pin	Description
INPUTS (Continued)	
$\overline{HOLD}$	Hold Request (active low). $\overline{HOLD}$ serves as a request from another master for the RGP's bus. In response, the RGP will complete the current bus cycle (if any), TRI-STATE® only the address and data buses and assert Hold Acknowledge.
$\overline{INT}$	Interrupt Request (active low). $\overline{INT}$ causes the RGP to suspend normal processing after completion of the current instruction (if any), to save the Program Counter and Processor Status Register on the stack and to enter the user's interrupt service routine. This function can be disabled via the Processor Status Register.
$\overline{NMI}$	Non-Maskable Interrupt Request (active low). $\overline{NMI}$ causes the RGP to suspend normal processing after the completion of the current instruction (if any), to save the Program Counter and Processor Status Register on the stack and to enter the user's non-maskable interrupt service routine. This function cannot be disabled, but is not enabled until the first time after $\overline{RSTI}$ that data is stored into the Processor Status Register.
RESERVED	Reserved for NSC testing. Must be tied to ground.
OUTPUTS	
A16–A23	Address Lines. A16–A23 provide the most significant eight bits of memory addresses during bus cycles. A23 is the most significant. A16–A23 are at TRI-STATE whenever $\overline{HLDA}$ is asserted by the RGP. Addresses are guaranteed to be valid at the falling edge of ALE.
BS0–BS1	Bus Status Lines. BS0–BS1 are used to indicate the type of bus cycle to be performed by the RGP. (See Table I.) BS0–BS1 become valid during the first T-STATE of a bus cycle (before the rising edge of ALE) and remain valid through the end of the last T-state of that cycle.
$\overline{RD}$	Read (active low status). $\overline{RD}$ indicates that the current cycle will cause memory to be read. $\overline{RD}$ becomes valid during the first T-state of a bus cycle (before the rising edge of ALE) and remains valid through the end of the last T-state of that cycle. Both $\overline{RD}$ and $\overline{WR}$ may be asserted in the same cycle. This indicates that the RGP is requesting a read-modify-write operation in the current cycle.

Pin	Description
OUTPUTS (Continued)	
$\overline{WR}$	Write (active low status). $\overline{WR}$ indicates that the current cycle will cause memory to be written. $\overline{WR}$ becomes valid during the first T-state of a bus cycle (before the rising edge of ALE) and remains valid through the end of the last T-state of that cycle. Both $\overline{WR}$ and $\overline{RD}$ may be asserted in the same cycle. This indicates that the RGP is requesting a read-modify-write operation in the current cycle.
ALE	Address Latch Enable. ALE indicates the beginning of a bus cycle. Its rising edge indicates that bus status, consisting of BS0–1, $\overline{RD}$ and $\overline{WR}$ is valid. Its falling edge indicates that the $\overline{PB}$ and the address, consisting of AD0–15, A16–23 and (if used in this cycle) B0–3, is valid.
$\overline{PB}$	Page Break (active low status). $\overline{PB}$ indicates that the 16 most significant address bits (AD8–15 and A16–23) of the RGP's current bus cycle are not equal to the 16 most significant address bits generated by the RGP in the previous bus cycle. $\overline{PB}$ can be used by the system's memory controller to allow it to generate page-mode accesses to memory, resulting in shorter access times. Since the eight least significant bits of addresses are ignored in the above comparison, the page size is always 256 words.
$\overline{HLDA}$	Hold Acknowledge (active low). $\overline{HLDA}$ indicates that the RGP has put the address and data buses at TRI-STATE and has entered an internal *hold* condition. The RGP will not exit the hold condition until the $\overline{HOLD}$ input has been removed.
$\overline{HSYNC}$	Horizontal Synchronization (active low). $\overline{HSYNC}$ indicates to the CRT monitor that the horizontal sweep should begin its retrace. The RGP can be programmed to use this output as *composite sync*, that is, the exclusive-NOR of $\overline{HSYNC}$ and $\overline{VSYNC}$. This option is selected via the RGP's Video Control Register.
$\overline{BLANK}$	Composite Blanking (active low). $\overline{BLANK}$ is the result of ORing the internal vertical and horizontal blanking signals. $\overline{BLANK}$ indicates to the CRT monitor that the screen should be blanked.
$\overline{DRREQ}$	Display Refresh Request (active low). $\overline{DRREQ}$ indicates that a bus cycle is requested by the RGP to read data from memory for the screen refresh function. $\overline{DRREQ}$ can be used by an external bus arbiter as a high-priority bus request. It can also be used for precise control of video DRAM transfer cycles, e.g., when performing mid-scanline transfers.

Pin Descriptions (Continued)

Pin	Description
OUTPUTS (Continued)	
$\overline{L/B}$	Linedraw/BITBLT mode. $\overline{L/B}$ sets the operating mode of the BPU during drawing operations. $\overline{L/B}$ is high to place the BPU into line-drawing mode, low to place the BPU into BITBLT mode. $\overline{L/B}$ is asserted throughout execution of any drawing instruction that uses the BPU, starting prior to the generation of any bus cycles within that instruction.
BSE	BITBLT Source Enable. BSE directs the flow of data within the BPU. When high, BSE indicates to the BPU that the current bus cycle is associated with BITBLT data in the source rectangle. BSE is low during BITBLT destination data bus cycles and during non-BITBLT cycles. It is valid on the rising edge of ALE and remains valid throughout the bus cycle.
B0/LME	Bit Select 0 or Left Mask Enable. This output to the BPU serves two purposes. When $\overline{L/B}$ is high it functions as B0 (see below). When $\overline{L/B}$ is low it functions as LME, which serves to enable the left mask. LME is valid at the falling edge of ALE and remains valid throughout the bus cycle.
B1/RME	Bit Select 1 or Right Mask Enable. This output to the BPU serves two purposes. When $\overline{L/B}$ is high it functions as B1 (see below). When $\overline{L/B}$ is low it functions as RME, which serves to enable the right mask. RME is valid at the falling edge of ALE and remains valid throughout the bus cycle.
B2/FWR	Bit Select 2 or FIFO Write. This output to the BPU serves two purposes. When $\overline{L/B}$ is high it functions as B2 (see below). When $\overline{L/B}$ is low it functions as FWR, which causes the BPU's barrel-shifter output to be written to the BPU's FIFO. FWR is valid on the rising edge of PH1, two clock periods after $\overline{WAIT}$ is sampled high during the T2 state.
B3/FRD	Bit Select 3 or FIFO Read. This output to the BPU serves two purposes. When $\overline{L/B}$ is high it functions as B3 (see below). When $\overline{L/B}$ is low it functions as FRD, which causes the BPU's FIFO output to be read into the BPU's logic unit. FRD is valid at the rising edge of a PH1 during the fetch of the corresponding destination data word.
B0–B3	Bit Select. When $\overline{L/B}$ is low, these four outputs have other functions (see above). When $\overline{L/B}$ is high, B0–3 select a specific bit within the word addressed by AD0–15 and A16–23. B0–3 become valid prior to the falling edge of ALE and remain valid throughout the bus cycle.

Pin	Description
OUTPUTS (Continued)	
$\overline{HALT}$	Halt (active low). $\overline{HALT}$ indicates that the RGP has executed a HALT instruction and entered the *halt* state, a state in which no instructions are processed, but video refresh functions continue. The halt state can be exited via an interrupt or reset. $\overline{HALT}$ can be used as part of a handshaking mechanism between the RGP and another processor: the other processor passes the RGP a list of instructions (a *display list*) terminating in a HALT instruction. The $\overline{HALT}$ output from the RGP signals completion of processing the display list.
$\overline{RSTO}$	Reset Out (active low). $\overline{RSTO}$ is driven low whenever $\overline{RSTI}$ is driven low. It is also driven low (for two clock cycles) at the beginning of execution of FILLA or FILLT instructions. The INITB instruction drives $\overline{RSTO}$ low for two clocks. $\overline{RSTO}$ is normally connected to the BPU's $\overline{RESET}$ input.
INPUT/OUTPUTS	
AD0–AD15	Multiplexed Address and Data lines. AD0–15 serve as outputs early in a bus cycle, providing the 16 least significant memory address bits. Later in the bus cycle they serve as the data bus. AD0 is the least significant bit of data or address. As a data bus, these lines can be inputs (during reads), outputs (during writes) or can be ignored by the RGP (e.g., during BITBLTs). These lines are at TRI-STATE whenever Hold Acknowledge is asserted by the RGP. Addresses are guaranteed to be valid at the falling edge of ALE.
$\overline{VSYNC}$	Vertical Synchronization (active low). $\overline{VSYNC}$ can serve as an input or an output. As an output, it indicates to the CRT monitor that the vertical sweep should begin its retrace. As an input, it clears the internal counters associated with vertical sync generation within the RGP. As such, it allows the RGP to synchronize itself with an external video source (this assumes the use of horizontal synchronization features of the VCG). This option is selected via the RGP's Video Control Register.

Table I

Bus Status (BS1, BS0)	Cycle Type (Function)
0, 0	Operand Read or Write
0, 1	Instruction Fetch
1, 0	BITBLT/Draw (Address Only)
1, 1	Video Refresh (Address Only)

Architectural Description

AGCS OVERVIEW

The RGP, serving as the core of a bitmapped graphics system, is designed to work in concert with the other members of the Advanced Graphics Chip Set (AGCS). The other components of the chip set are the DP8512 Video Clock Generator (VCG), the DP8515/16 Video Shift Register (VSR) and the DP8511 BITBLT Processing Unit (BPU). Additional functions required for system implementation are provided by National through such components as the DP8520/22 Video DRAM Controller.

The components that comprise the Advanced Graphics Chip Set are fabricated in a variety of technologies, each appropriate to the function performed by that component. Both CMOS and bipolar technologies are used in the family. As a result, the family exhibits both VLSI functionality and 250 MHz operation.

The Advanced Graphics Chip Set supports a high-performance architecture without imposing a particular bus protocol, timing or memory type upon the system designer. As a result, AGCS-based systems can be realized with a range of solutions to the cost/performance tradeoff. Advances in memory technology can be capitalized upon in future systems while retaining software compatibility.

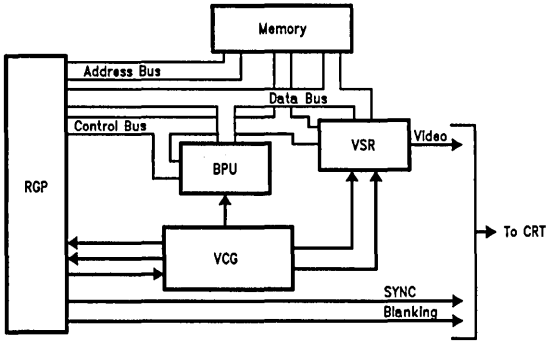
A major feature of the system architecture is the support of simultaneous data manipulation (during drawing) at each of the bitplanes. This allows the system to retain its drawing speed (in pixels per second) as pixel depth increases from one to any number of bits.

The functional interconnection of these components is illustrated in *Figure 1*, which represents a minimal bitmapped graphics system. In this system, the intensity of each pixel is described by a single bit, i.e., each pixel is either on or off. The roles of the various components are described below, as are design considerations for color systems.

DP8500 Raster Graphics Processor (RGP)

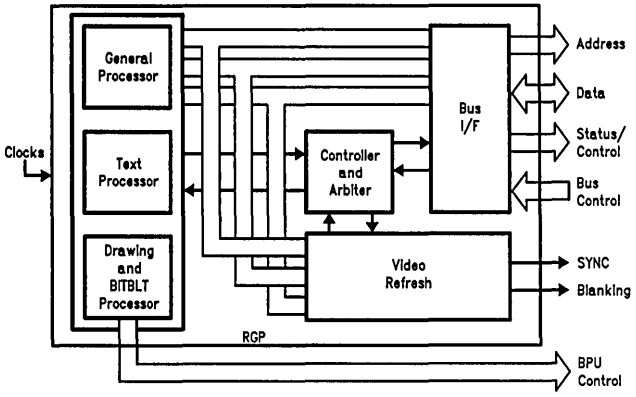
The RGP is designed to be the overall control mechanism in graphics systems. It draws graphics objects in the display buffer, refreshes the video display, and performs general purpose computing tasks.

The implementation of the RGP reflects these functions (see *Figure 2*). A general purpose microcoded microprocessor core is augmented by dedicated hardware for the setup and execution of graphics primitives. In addition, a programmable state machine handles all video synchronization functions and produces addresses for video refresh. Internal bus arbitration logic controls access to the external bus.



TL/F/9427–3

FIGURE 1. Minimal Bit-Mapped Graphics System



TL/F/9427–4

FIGURE 2. RGP Organization Diagram

Architectural Description (Continued)

DP8511 BITBLT Processing Unit (BPU)

The DP8511 BPU provides a data path for changing the contents of the frame buffer. The drawing functions of the RGP, e.g., line drawing and polygon filling, rely on the BPU to accept data from memory, modify it, and return it to memory. The general scheme underlying these operations is BITBLT (BIT boundary BLock Transfer). During BITBLT, the RGP serves as an address generator to initiate the appropriate memory cycles and as a strobe generator to control the BPU's operation.

The BPU is a microCMOS device intended to provide hardware support for BITBLT. It includes a barrel shifter, used to shift source data into bit alignment with the destination and a FIFO to contain a series of shifted source words. A 16-function logic unit allows all possible bitwise combinations between the source and destination data. The BPU has hardware to support pixel operations and line drawing. In particular, it can address a single bit within the current word and read and write the selected bit. Details of BPU operation can be obtained from the BPU data sheet.

The use of BITBLT as the underlying mechanism for all drawing operations promotes a common method for handling both simple systems, as shown in *Figure 1*, and more complex, high performance systems, as shown in *Figure 3*. This latter figure illustrates a multi-plane system, i.e., one in which several bits (one from each plane) describe the value of a pixel. This might be used to describe the intensity (in monochrome) or the hue (in color) of the pixel. The use of a BPU per plane, permitting simultaneous update of all planes, leads to the highest performance. Alternatively, a cost-performance trade-off might be made by sharing one or more BPUs across two or more planes. At one extreme (single BPU) updates are done serially to each plane. At the other extreme (a BPU per plane) updates are performed in a purely parallel manner. A middle ground could be implemented, updating the planes in a serial-parallel manner. The mechanism of implementing the data path function in the BPU, rather than the RGP, produces this design flexibility.

DP8515/16 Video Shift Register (VSR)

The DP8515/16 VSR shifts pixel information at the data rate required by the CRT. It is implemented in National's Bipolar-CMOS process. It combines CMOS control logic and a CMOS input FIFO with an ECL shifter. As a result, it provides the system designer additional timing flexibility in the load path coupled with 250 MHz shift capability without excessive current consumption. The DP8515 provides ECL 10k compatible outputs, while the DP8516 is ECL 100k compatible. Parallel loading of the VSR is initiated by the RGP and assisted by the VCG.

DP8512 Video Clock Generator (VCG)

The DP8512 VCG, implemented in National's oxide-isolated bipolar process, provides all clocks in the system. It generates all clocks from a relatively low frequency (less than 20 MHz) crystal or external clock, simplifying system design and reducing system cost.

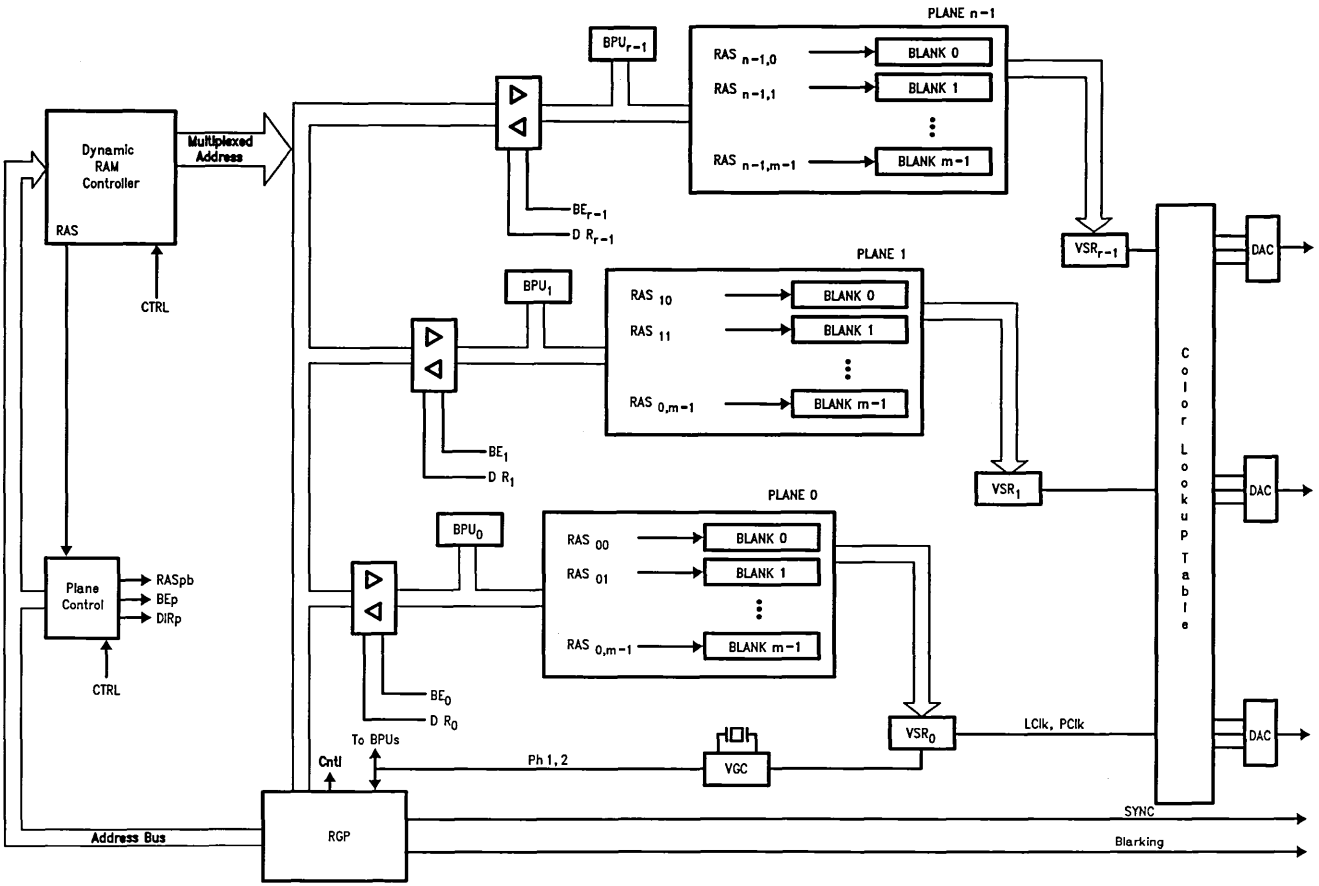
A two-phase MOS processor clock is supplied to the RGP and BPU; TTL clocks are generated for the RGP video refresh logic and for the VSR's FIFO control functions. The VSR's load and shift functions are controlled by ECL clocks generated by the VCG. An on-chip phase-locked loop (PLL) multiplies the reference crystal/clock in order to generate a pixel clock as high as 250 MHz. The VCG also includes another PLL for synchronizing the horizontal sync (generated by the RGP) to an external source.

PROGRAMMING MODEL

The RGP is a microprocessor combined with a concurrent video-refresh machine. This section will discuss the programmer-visible aspects of both the microprocessor and the video-refresh machine. For additional information, refer to the DP8500 RGP Programmer's Reference Manual (PRM).

The processor section of the RGP is a general purpose microprocessor with an instruction set expanded to include graphics operations. While the processor is microcode driven, certain graphics operations, notably BITBLT, line drawing and clipping, are implemented via dedicated hardware for increased throughput.

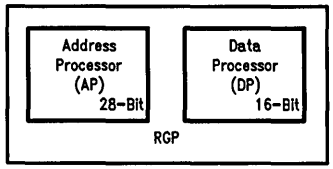
The organization of the processor, shown in *Figure 4*, reflects the duality, present in raster-graphics systems, of



TL/F/9427–5

FIGURE 3. High-End AGCS-Based Color Bit-Mapped Graphics System

Architectural Description (Continued)



TL/F/9427–6

FIGURE 4. RGP Dual-Processor Configuration

a virtual (Cartesian, x-y) drawing space and a physical (memory address) space. That is, the RGP's processor section actually consists of two processors, the Address Processor (AP) and the Data Processor (DP), operating concurrently, driven by common microcode. The RGP's register complement, described below, is shown in *Figure 5*.

The AP consists of a 28-bit Arithmetic and Logic Unit (ALU), having a relatively simple instruction set, and a private bank of sixteen 28-bit registers. The DP is composed of a 16-bit ALU, having a relatively rich instruction set, and a bank of sixteen 16-bit registers. These instruction sets operate register-to-register only and then only within their respective register banks.

The remaining registers of the RGP have dedicated functions in support of the graphics environment or the video refresh mechanism. Examples include the registers of the Clipper and the Display Buffer Base Address register (DBB).

A single stream of instructions, fetched from external memory, serves both processors via microcode control. This includes the register-to-register instructions of both the AP and DP and the instructions for data transfers between RGP registers and memory. Additional RGP instructions, not belonging exclusively to the AP or DP, use both processors and, often, additional on-chip resources; this is typical of all of the drawing instructions. An example of this is the DRLN (draw line) instruction, which uses both processors, the clipper, the line drawing controller, the line-pattern generator and the BITBLT controller.

While simple instructions like ADD and MOV leave unmodified any registers not specified in their encodings as being operands, the more complex drawing instructions like DRLN use certain registers of the AP and DP as implicit arguments or as temporary storage. These *side effects* of RGP drawing instructions are detailed in the PRM.

Memory Organization and Data Types

The RGP supports uniform 24-bit addressing; the unit of storage in memory is the word. That is, the memory space of the RGP consists of 2^{24} 16-bit words. Parts of the memory space can be designated by the user as Program, Data, Stack, Display Buffer, etc., at the user's discretion; the RGP imposes no restrictions upon these allocations.

For purposes of drawing, the RGP views the memory as being bit addressable (see Memory Addressing Section). In this case, the address is a 28-bit quantity, called a Bit Address, which consists of a 24-bit Word Address, left-shifted four bits and added to a 4-bit bit-selection field.

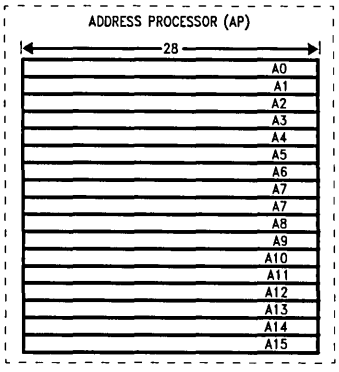
Data elements treated by the RGP vary in length (number of bits) from 3 to 28 bits according to their function. However, they are always stored right justified (that is, justified toward bit 0) in registers or in memory (see *Figure 6*). Further, when stored in memory, multiple-word quantities are always stored with the least significant word at the lowest storage address. The address of a memory-resident quantity is the address of its least significant word.

The following data element lengths are used by the RGP:

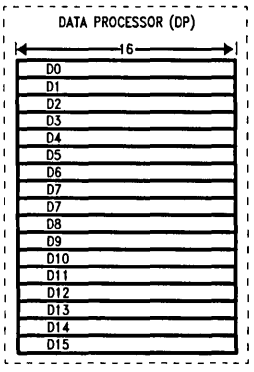
word	16 bits or less
word address	24 bits
bit address	28 bits

If an element is written from memory to a register that is shorter than the element, the more significant portion of the element is truncated to allow the less significant portion to fit into the register. If an element is written from a register to memory, the element is right justified in the memory location and unused bits are set to zero.

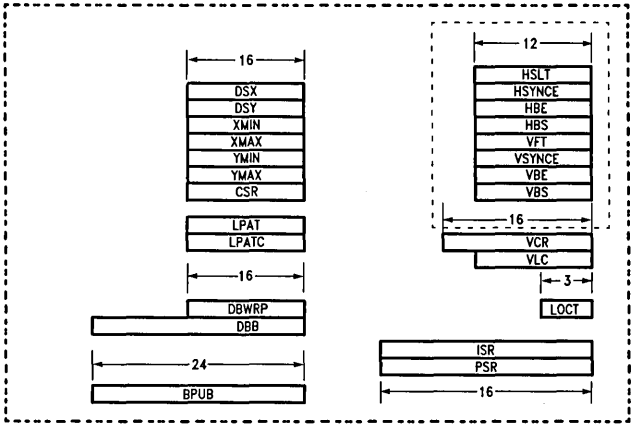
Architectural Description (Continued)



TL/F/9427–7

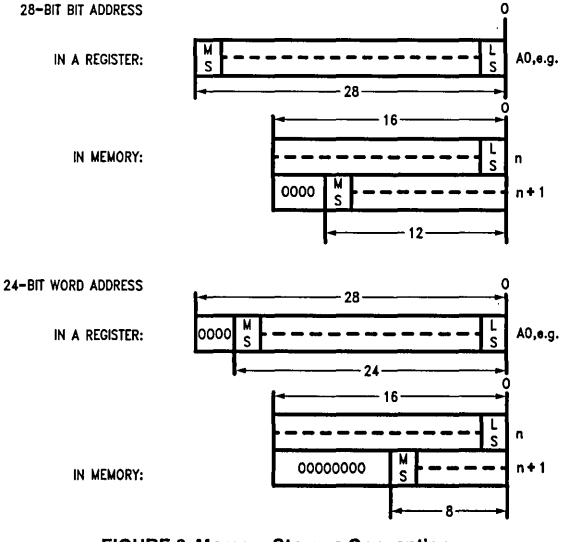


TL/F/9427–8



TL/F/9427–9

FIGURE 5. RGP Register Summary



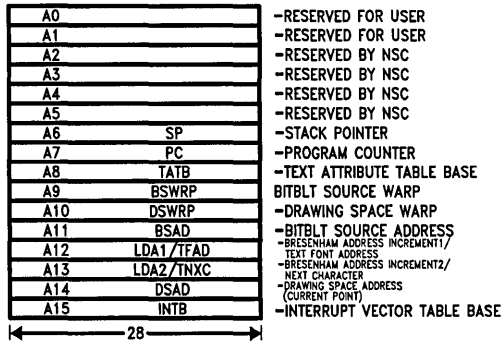
TL/F/9427–10

FIGURE 6. Memory Storage Conventions

Architectural Description (Continued)

Address Processor Registers

The registers of the Address Processor *(Figure 7)* are 28 bits in length. They are used to hold operands for the Address Processor or to hold Word Addresses or Bit Addresses. Registers A0, A1 and A2 are not subject to side effects of RGP drawing instructions.

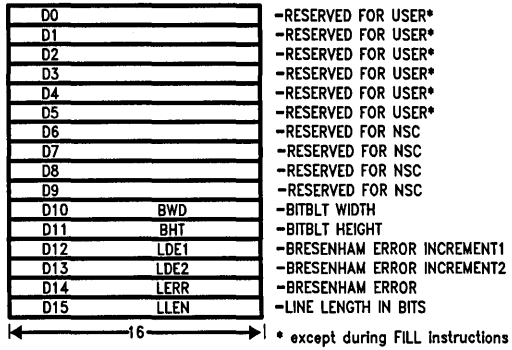


TL/F/9427–11

FIGURE 7. Address Processor Registers

Data Processor Registers

The registers of the Data Processor *(Figure 8)* are 16 bits in length. All of these registers are subject to side effects of RGP drawing instructions, but D0–5 are preserved through execution of all RGP instructions except those used for polygon filling.



TL/F/9427–12

FIGURE 8. Data Processor Registers

Architectural Description (Continued)

Status/Control Registers

The following registers indicate or control instruction or interrupt status of the RGP. They are each 16 bits in length.

The Processor Status Register (PSR, see *Figure 9*) indicates the status returned as a result of instruction execution. It also controls the enabling of maskable interrupts and the enabling of the clipper. The individual bits are defined as follows (all fields are asserted when set to one, negated when set to zero):

Z: Data Processor Zero bit

C: Data Processor Carry bit

N: Data Processor Negative bit

V: Data Processor Overflow bit

AZ: Address Processor Zero bit

AC: Address Processor Carry bit

K: An undrawn character code is present in register TNXC.

W: The current x,y is within the bounds of the clipper.

EIP: External Maskable Interrupt Pending

VIP: Video Interrupt Pending

CLE: Enable Clipper (1 to enable)

PTE: Enable Pick Trap

EIE: Enable External Maskable Interrupt

VIE: Enable Video Interrupt

See the PRM for more information

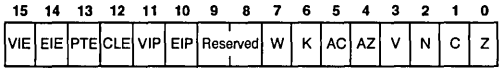


FIGURE 9. Processor Status Register

Clipper Registers

All drawing operations executed by the RGP are subject to the action of a rectangular clipper, when the clipper is enabled. The action of the clipper is to suppress the drawing of pixels outside its boundary. Clipping always takes place to bit resolution independently of the nature of the graphics primitive/operation.

That is, all lines, polygons, BITBLTs and text primitives are clipped exactly to the coordinate values defined in the clipper.

The clipper consists of six 14-bit coordinate registers and a 16-bit clipper status register, as follows:

XMIN The x-coordinate of the left boundary of the clipper

XMAX The x-coordinate of the right boundary of the clipper

YMIN The y-coordinate of the top boundary of the clipper

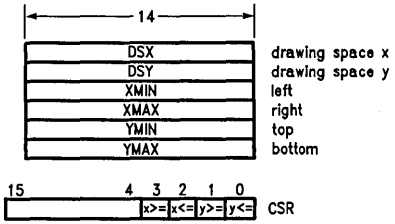
YMAX The y-coordinate of the bottom boundary of the clipper

DSX The x-coordinate of the current drawing point

DSY The y-coordinate of the current drawing point

CSR The 16-bit Clipper Status Register

When enabled, the clipper is invoked by the RGP for all drawing instructions. The clipper may also be utilized by drawing routines written by the user. The organization of the CSR *(Figure 10)* facilitates this use of the clipper. The CSR contains the results of the four meaningful comparisons between the clipper boundary registers and the current point registers. These results are expressed in "outcode" format in the four least significant bits of the CSR.



TL/F/9427–13

FIGURE 10. Clipper Registers

Architectural Description (Continued)

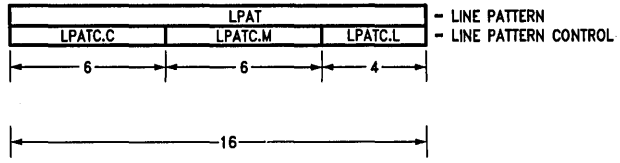


FIGURE 11. Line Style Generator

Line Style Registers

Those graphics primitives which are drawn by the RGP one pixel at a time, i.e., points, lines and polylines, are drawn subject to the action of a line pattern generator within the RGP. This mechanism produces a pattern along the length of a (presumed) line by suppressing the memory cycles associated with drawing certain points along the line, according to values contained in the registers of the line pattern generator. The line pattern generator includes a mechanism for pattern magnification. The registers of the line pattern generator *(Figure 11)* are defined as follows:

LPAT 16-bit Pattern Register

LPATC 16-bit Pattern Control Register, contains three fields:

LEN Pattern Length (4 bits)

MAG Pattern Magnification (6 bits)

CTR Pattern Counter (6 bits)

During pointwise drawing operations, the RGP examines the least significant bit of the LPAT register to determine whether or not to produce a memory cycle to draw the current point. A one in this position will enable drawing; a zero will inhibit drawing. At this point the memory cycle associated with drawing the current point will be executed if appropriate.

The least significant bit of LPAT remains in place for the number of points specified in the MAG field of LPATC; then a circular right shift is performed on the n least significant bits of LPAT, where n is the value specified by the LEN field of LPATC. The CTR field of LPATC serves as a counter used by the RGP to implement magnification. See the PRM for more information.

Since the length of the LPAT register is 16 bits, the maximum pattern length (assuming a magnification of one, i.e., no magnification) is 16 bits. However, shorter patterns can be implemented by setting the LEN field to an appropriate value. The length of the pattern is the number of least significant bits of LPAT that participate in the circular shift. LEN, MAG and CTR all have biases of +1. That is, values of 0 in these fields will program the line pattern generator for a pattern of length 1 and a magnification of 1.

The registers LPAT and LPATC are never reinitialized implicitly by RGP instructions. Once set, a pattern persists through all subsequent points, lines or polylines drawn.

Video Refresh Registers

The video refresh registers (*Figures 12* and *13*) contain the parameters for the programmable video refresh machine. They are of two types, distinguished by the mode of accessing them.

The first type is composed of eight registers that share a common register address (VIDEO); these can be accessed serially by successive MOV instructions. A 3-bit circular pointer (the VRX field of the VCR register) advances after each MOV and can be set to point to any of the eight registers.

The second type consists of 3 registers with separate addresses. The video refresh registers and their interpretations are detailed below. The eight serially addressable registers are shown first, in order. HSLT corresponds to a VRX value of 0, VBS to a value of 7.

HSLT Horizontal Scan Line Time (12 bits)

HSE Horizontal Sync End (12 bits)

HBE Horizontal Blanking End (12 bits)

HBS Horizontal Blanking Start (12 bits)

VFT Vertical Frame Time (12 bits)

VSE Vertical Sync End (12 bits)

VBE Vertical Blanking End (12 bits)

VBS Vertical Blanking Start (12 bits)

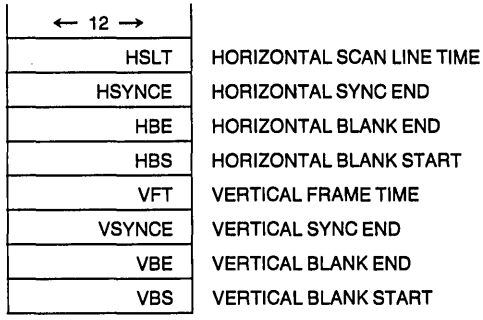


FIGURE 12. Video Refresh Parameter Block

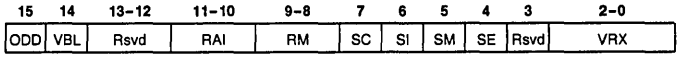


FIGURE 13. Video Control Register

Architectural Description (Continued)

VCR Video Control Register (16 bits), composed of the following fields:

- VRX Video Register Index (3 bits)
- SE Scan Enable (1 bit)
- SM Master Sync (1 bit)
- SI Interlaced Mode (1 bit)
- SC Composite Sync Mode (1 bit)
- RM Video Refresh Mode (2 bits)
- RAI Video Refresh Address Increment (2 bits)
- VBL The Vertical Blanking Flag
- ODD The Odd Video Field Flag

DBB Display Buffer Starting Address (24 bits)

DBWRP Display Buffer Warp (16 bits)

THE GRAPHICS ENVIRONMENT

This section discusses the conventions adopted by the RGP and the resultant environment within which all graphics operations take place.

Memory Addressing

For operations, such as instruction and operand fetching, stack operations and interrupt service, the RGP accesses memory as a uniform space of 2^{24} 16-bit words, starting at address 0 and extending to address FFFFFF hex. Bytes are not directly addressable by the RGP.

During drawing operations, the RGP can access individual bits in memory by means of a 28-bit quantity called a bit address. The correspondence between a bit address and the physical bit in memory is as follows: the 24 most significant bits of the bit address provide the address of the word in memory containing the addressed bit, while the four least-significant bits of the bit address select a bit within that word. If the four LSBs are zero, bit zero (i.e., the memory bit corresponding to the AD0 pin of the RGP) is addressed. Thus, the bit-addressed memory starts at Bit 0 of Word 0 and extends linearly to Bit 15 of Word $2^{24} - 1$.

In practice, the RGP does not read and write individual memory bits directly. When it generates a 28-bit bit address, the most-significant 24 bits are used to access a 16-bit word in the linear address space, while the 4 least significant bits go to the BPU as B0–3. The BPU contains hardware to read and write exactly one bit in the current word. In color systems with one BPU per plane, all BPUs operate in parallel, reading and/or writing the corresponding bit in each plane (that is, all the bits of a pixel). As a result, the 28-bit quantity can be viewed as a pixel address as well as a bit address, though this interpretation is system hardware dependent and may in fact be operation-dependent. This is discussed more fully in the Multiple-Bit Pixels Section.

Cartesian Drawing Space

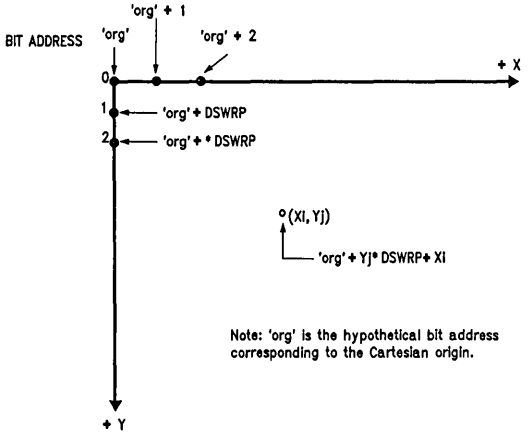
Drawing operations performed by the RGP execute in a logical drawing space which is Cartesian. This x-y space is defined as having the origin in the upper left. Movement to the right increases the x-coordinate; movement downward increases the y-coordinate. Each axis may be a maximum of 2^{14} bits in length. Therefore, each coordinate may take on any integer value in the range of 0 to $2^{14} - 1$.

A flexible mechanism controls the correspondence between the logical (x-y) location and the physical (bit) address in memory. Once the correspondence has been initialized by the user, the RGP maintains it throughout all drawing operations. The correspondence can be changed explicitly at any time.

The correspondence is shown in *Figure 14*. The Cartesian origin (x = y = 0) corresponds to the hypothetical bit address **org**. Incrementing the logical x-coordinate increments the bit address. Incrementing the y-coordinate adds the contents of the DSWRP register (the *warp* of the drawing space) to the bit address. The current bit address is maintained in the DSAD register. Thus,

DASD = **org** + DSY × DSWRP + DSX

The correspondence between Cartesian coordinates and bit addresses is established by explicitly loading the registers DSX, DSY and DSAD. This correspondence is maintained by the RGP during the execution of all instructions if DSWRP contains a value appropriate for the current drawing space. Note that the drawing space can coincide with or overlap the display buffer or can be entirely distinct from it, and the two spaces can have separate warps.



TL/F/9427–15

FIGURE 14. Logical and Physical Addresses

Architectural Description (Continued)

Dot/Line/Polyline/Polygon Drawing Operations

During the execution of the RGP's drawing instructions, the flow of data is between the memory and its associated BPU. The RGP's drawing operations can be divided into two classes, based upon the operating mode of the BPU: BITBLT or LINE, according to the state of the $\overline{L/B}$ line of the RGP and BPU(s). LINE mode is used for all pointwise drawing operations; BITBLT mode is used for all wordwise drawing operations.

Pointwise drawing operations include reading and writing individual bits (RDPT, DRPT), drawing lines (DRLN), drawing polylines (DRPLN) and drawing polygons (DRPGN). During all pointwise operations, the line pattern generator is active. The clipper (if enabled), is also active.

The clipper performs its function by suppressing the memory cycle associated with drawing the current point if that point is outside the clipper.

The line pattern generator operates in a continuous fashion within and between these instructions; it is not forced to a given state at the beginning of a pointwise drawing instruction. Therefore, a line pattern will continue around the vertices of a polyline. Also, a curve drawn with a series of DRPT instructions will be subject to the line pattern generator. Since the line pattern generator cannot be disabled, it must be loaded with a solid (all ones) pattern if a solid line (no pattern) is desired. Similarly, a pattern of all zeros will suppress all pointwise drawing.

The RDPT instruction is not affected by the clipper or line pattern generator, nor does it affect them.

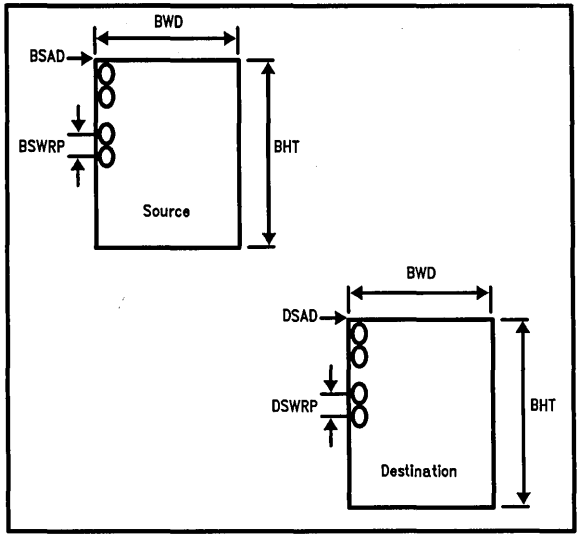
BITBLT Operations

Bit Boundary Block Transfer (BITBLT) operations are carried out by the RGP with the BPU(s) in BITBLT mode. BITBLT is the performance of sixteen specific bitwise logical operations between two rectangular arrays of bits, each having the same height and width and an arbitrary bit alignment (see *Figure 15*). In RGP-based color graphics systems, each DP8511 BPU participating in the BITBLT operation can be programmed to perform its logical operation independently of the others. This permits such effects as transparency and foreground-background color rendering.

During BITBLT, the RGP produces all memory (word) addresses and the set of BPU control signals necessary to control the FIFO and masking functions. The BPU is responsible for assembling and shifting source words, storing them in the FIFO, receiving destination words, logically combining them with the corresponding shifted source words, (masking any destination bits necessary) and returning the result to the destination.

As during pointwise operations, the clipper is active and clips the destination to pixel resolution. In the process, the BITBLT left and right masks may change from those predicted by the destination alignment alone. Thus, the minimum number of memory cycles required, considering the clipper, is always performed.

The two directions of execution of BITBLTs can be specified independently: right to left (versus left to right) and bottom to top (versus top to bottom).



BSAD — 28 bits, bit address
— BITBLT Source Address

DSAD — 28 bits, bit address
— Drawing Space Address

BSWRP — 24 bits, word count
— BITBLT Source Warp

DSWRP — 24 bits, word count
— Drawing Space Warp

BWD —14 bits, bit count
— BITBLT Width

BHT — 14 bits, line count
— BITBLT Height

BWD(source) = BWD(dest)
BHT(source) = BHt(dest)

TL/F/9427–16

FIGURE 15. BITBLT Parameter Definitions

Architectural Description (Continued)

The reading of the source rectangle and the reading of the destination rectangle can be suppressed by the user independently of one another. This should be done after taking into account the requirements of the complete set of logic operations being performed by the BPUs in the system. For example, if no function other than Function 0 (fill with zeros) or Function 15 (fill with ones) is being performed, both source and destination reads may be suppressed. If a two-operand function, such as XOR, is being performed by any of the BPUs, both the source and destination must be read. Various intermediate cases may arise. the leftmost and rightmost words of the destination are always read, since this is necessary in order to use the BITBLT left/right masks.

Each BITBLT rectangle (source and destination) has a starting address (BSAD and DSAB) and a warp (BSWRP and DSWRP); they have a common width and height (BWD and BHT). These must be initialized prior to executing the BITBLT instructions. Additionally, DSX and DSY must be in correspondence with DSAD. The use of independent warps in the source and destination spaces permits packing and unpacking of bitmaps (e.g., for fonts), providing a better environment for memory pool management and generally leading to more efficient use of memory.

Polygon-Fill Operations

The RGP supports the drawing of pattern-filled vertically-convex polygons via the FILLA and FILLT instructions. (See the PRM for more information.) The argument of the FILLA instruction is a list of vertices in counter-clockwise drawing order. The first (and last) vertex of the polygon is the current point, DSX, DSY, which must be an uppermost vertex of the polyon. The RGP's filling algorithm traverses the data structure, determining the polygon's intercept points with each horizontal line in the vertical extent of the polygon. Each line is filled, using a pattern contained in the BPU's FIFO.

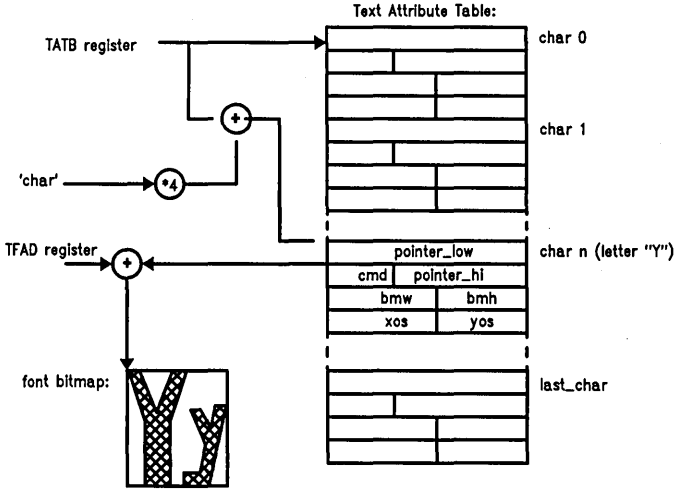
The FILLT instruction provides a similar mechanism for filling trapezoids with horizontal top and bottom edges. The key feature of this instruction is that the lines that form the right and left edges of the trapezoid need not start and end at the intersections with the top and bottom edges of the trapezoid.

Each horizontal line used in filling a polygon is treated as a BITBLT of one-bit height. The first horizontal line is filled by logically combining the first word from the BPU's FIFO with the successive words of the horizontal line. the second line is filled, in the same manner, utilizing the next word from the BPU's FIFO, etc. The FIFO read is non-destructive; as a result, the pattern repeats vertically every 16 words. Since the FIFO is 16 bits wide, the pattern is 16 by 16 bits.

Text Operations

Text primitives are handled by the RGP within an environment designed to support flexibly and efficiently such features as multiple fonts, multiple type sizes and styles, sub- and superscripts and proportional spacing. This environment maps cleanly into the logical x-y drawing space and does not require dedicated text planes.

Text is rendered from monochrome or full color storage into the drawing space by BITBLT. Therefore, a bitwise logical operation takes place between the text and the current information in the drawing space. The text instructions determine from the current state of the text environment (a set of pointers and data structures) the necessary BITBLT parameters, perform the BITBLT (subject to bitwise clipping, if the clipper is enabled) and update the state of the text environment in preparation for the next text instruction.



TL/F/9427–17

FIGURE 16. Text Address Calculations

Architectural Description (Continued)

The text environment is maintained in the AP as follows:

TFAD Text Font Base Address (A11)

TNXC Next Text Character (A3)

TCDB Text Character Descriptor Table Base (A10)

The major data structure used in support of text is the Text Character Descriptor Table *(Figure 16)*. This table contains a four-word entry for each character in the current font. Character codes are interpreted by the text instructions as offsets into the table. This gives the RGP access to the source bitmap of the character and additional information used in rendering the character and updating the text environment.

The entry consists of:

POINTER A relative pointer (28 bits) to the source bitmap

key A field specifying the interpretation of the table entry:

—Render as portrait mode

—Render as landscape mode

—Trap through INTB + 8

WD Source bitmap width (8 bits)

HT Source bitmap height (8 bits)

DX X-offset (signed, 8 bits)

DY Y-offset (signed, 8 bits).

If the character is to be rendered, the source bitmap is taken from TFAD + POINTER, the logical destination is (DSX + DX, DSY + DY), and the BITBLT height and width are HT and WD.

The environment will be updated as follows in the portrait mode:

DSX = DSX + DX + WD

DSY = DSY

DSAD = DSAD + DX + WD

The environment will be updated as follows in the landscape mode:

DSX = DSX

DSY = DSY + HT + DY

DSAD = DSAD + (HT + DY) * DSWRP

The subroutine call (trap) option is a general-purpose escape mechanism for handling EOT characters, line feeds, characters larger than 256 by 256 pixels, etc. When the key field indicates *trap*, the RGP does not interpret the other fields of the entry, leaving them free for other purposes.

Characters can have eight-bit codes or sixteen-bit codes. Eight-bit characters can be packed into sixteen-bit words and unpacked by means of the DCL or DCH instruction.

See the PRM for more information.

Multiple-Bit Pixels

The RGP hardware supports high-speed rendering of graphics primitives into a drawing space. In the process, it maintains the correspondence between logical and physical memory. This correspondence is independent of pixel size (depth, number of bits per pixel). In fact, the RGP architecture has no parameters for pixel size. This system-level parameter is effectively a hardware/software layer applied above the RGP architecture. This allows designers of AGCS-based systems some flexibility in trading off cost and performance.

The lowest cost approach is to use a single BPU per system, time-multiplexing it across the bit planes. Each graphics primitive must be rendered once in each bit plane. This can be done by assigning a block of memory addresses to each bit plane, and considering each bit plane as an independent drawing space. By changing the physical address corresponding to the drawing origin (modifying DSAD, typically by means of the SETPT instruction) the same display list can be executed in each plane.

The highest performance solution is obtained by using one BPU for each plane. The display list is executed once, with all planes being updated simultaneously. Each plane will have a unique block of addresses. In this case, however, the corresponding words in each plane must have addresses whose m least-signficant bits match, where 2^m is greater than or equal to the size of the plane. Then the higher-order address bits (above m − 1) can be decoded as to select the plane, and external logic can address the planes individually or in parallel (selecting some or all of the planes simultaneously). This requires a mechanism to isolate or connect, as required, the local data buses of the individual planes, typically a Tri-State buffer per plane, plus the logic to control the buffers and to distribute memory control signals, typically RAS, among the planes. This logic is referred to as the video plane control logic.

An intermediate solution might use a BPU for every other plane, multiplexing each BPU two ways. In this case, the display list would be executed twice. Other intermediate solutions are possible as well.

VIDEO REFRESH

The RGP's video refresh logic is designed to support a variety of raster graphics applications, including non-video applications such as laser printers. This is accomplished by means of flexible programming of the video parameters and through a section of video refresh modes.

The user must determine the appropriate video parameters for the chosen display device, additionally taking into account the chosen values for PCLK and LCLK (the pixel

Architectural Description (Continued)

and load clocks, respectively). These values are then written to the video parameter block.

Additional parameters associated with the video refresh logic are contained in the RGP's Video Control Register (VCR).

Signal Definitions

The RGP's video refresh logic is driven by a single signal, LCLK. From this clock, according to its operating modes, the RGP generates the signals required to directly control a video monitor: Horizontal Sync, Vertical Sync and composite Blanking. Bus cycles required for video refresh purposes are also initiated by this logic.

Horizontal Sync causes the monitor to initiate the horizontal retrace period. Vertical Sync causes the monitor to initiate the vertical retrace period. Blanking causes the monitor to shut off the video output, in order to prevent writing to the screen during retrace periods. This prevents spurious retrace lines from appearing in the display.

Video Parameter Definitions

The correspondence between the register-resident parameters and the video waveforms is depicted in *Figure 17*. Horizontal parameters are expressed in units of LCLKs; vertical parameters are expressed in units of scan lines.

The video refresh logic is a pair of counter-driven machines. The first, responsible for horizontal sync and blanking, increments on each LCLK. Its counting sequence is 0,1, ... HSLT,0,1 .... As a result, a scan line (including sync) is HSLT + 1 LCLKs in duration.

The second counter-driven machine is responsible for generation of the vertical sync and blanking. It increments once per scan line, on the LCLK during which the horizontal counter is cleared. Its counting sequence is 0,1, ... VFT − 1,0,1 .... As a result, a frame (including sync) is VFT scan lines in length.

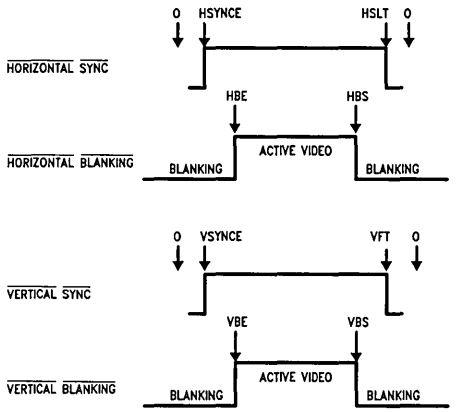
Refer to the PRM for more information.

Interlaced Refresh

The video refresh logic may be set up for interlaced scan mode by setting the SI-bit of the Video Control Register (VCR). In this mode, the screen is refreshed in two fields, the even and odd fields.

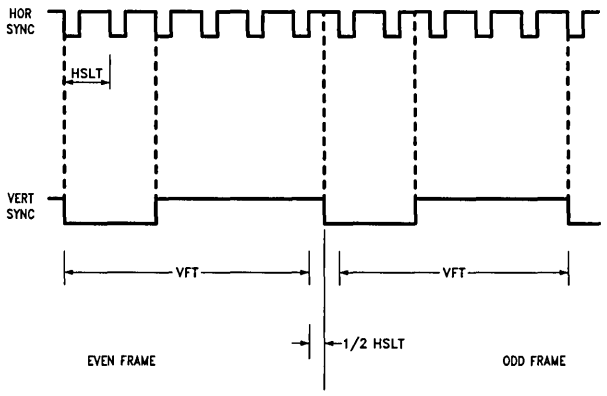
The even field consists of all even-numbered lines; the odd field consists of all odd-numbered lines.

Interlaced sync is generated by a slight modification to the vertical sync as shown in *Figure 18*.



TL/F/9427–18

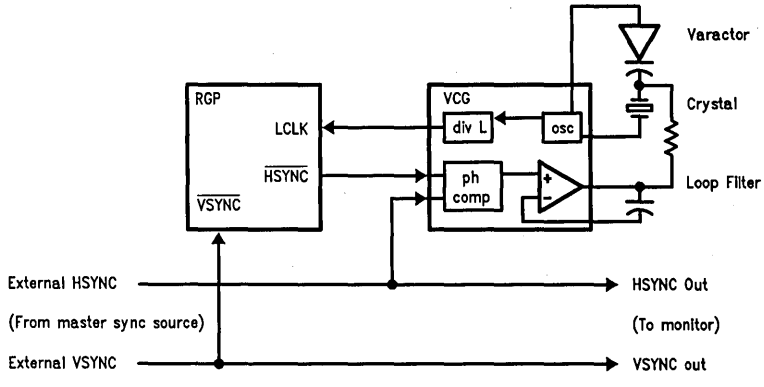
FIGURE 17. Video Parameter Definitions



TL/F/9427–19

FIGURE 18. Interlaced Video Timing

Architectural Description (Continued)



TL/F/9427–20

FIGURE 19. External Synchronization (Genlock)

Video Refresh Modes

The RGP provides four operating modes for the video refresh logic. The fundamental difference among the various modes is the way in which they allocate the available memory bandwidth between update (drawing) operations and video refresh operations. In this context, "drawing operations" refers to ALL operations other than video refresh. The mode is selected by means of the RM field of the Video Control Register (VCR).

Mode 0 No memory cycles are generated for refresh purposes. All memory bandwidth is available for drawing.

Mode 1 During active (non-blanked) video time, each LCLK causes the RGP to request one bus cycle for refresh purposes. The request is indicated by the RGP's assertion of DRREQ (Display Refresh Request) output. Drawing operations may take place at all other times.

Mode 2 During active video time a bus cycle is requested on each LCLK, alternating between video refresh cycles and drawing cycles. During blanking, only drawing cycles are generated.

Mode 3 A refresh cycle is requested by the RGP at the beginning of horizontal sync, in preparation for the next scan line. A refresh cycle will also be requested when the refresh address falls on a 256 word boundary. Drawing cycles can be generated at all other times. This mode is intended to support Video DRAMs.

External Sync Sources

The video refresh can be programmed for synchronization to an external source via the SM-bit of the Video Control Register (VCR). When in the Master Sync mode, the RGP generates all syncs and blanking signals with no external reference (except LCLK).

When in Slave Sync mode (see *Figure 19*), the RGP's Vertical Sync line becomes an input and is driven by the vertical sync from an external source. The negative transition of this input will clear the vertical counter in the RGP's video refresh logic. Thus, the RGP is forced into vertical sync with the outside source.

A phase-locked loop in the VCG forces the RGP's Horizontal Sync output into synchronization with the externally-supplied horizontal sync by adjusting the frequency of LCLK (indirectly; the RGP's processor clock is actually adjusted directly. LCLK is divided down from the processor clock).

INSTRUCTION SET

Addressing Modes

The Address and Data processors of the RGP are register-to-register machines. MOV instructions are included in the instruction set to provide a mechanism for transfers between registers and memory. MOV instructions can use the following addressing modes, which are also supported, to varying degrees, by the remainder of the instruction set:

Immediate The operand is contained in the word(s) of memory immediately following the instruction.

Direct The operand is contained in the memory location(s) pointed to by the 24-bit address quantity contained in the two memory words immediately following the current instruction. The least significant word of the address is stored at the lowest address.

Register Relative The operand is contained in the memory location(s) pointed to by the sum of the contents of the indicated AP register and the twos complement displacement quantity contained in the word immediately following the current instruction.

Register Indirect with Post-Increment The operand is contained at the memory location(s) pointed to by the contents of the indicated AP register, subject to the following convention: The AP register is incremented, by the number of words in the operand, after performing the operation.

Architectural Description (Continued)

Register Indirect with Pre-Decrement	The operand is contained at the memory location(s) pointed to by the contents of the indicated AP register subject to the following convention: The AP register is decremented, by the number of words in the operand, prior to performing the operation.

Instruction Set Summary

The instruction set of the RGP can be divided into the following categories:

Load and Store Instructions	Instructions that provide transfers between registers and memory.
General Processing Instructions	Register-to-register operations that take place in either the AP or DP.
Program Control Instructions	Instructions that control the flow of programs and the general software environment.
Graphics Instructions	Instructions that draw or that control drawing parameters only.

Load and Store Instructions

MOV Load register from memory or store from register-into memory.

General Processing Instructions

The General Processing instructions are those that execute within either the AP or the DP, or from DP to the U Bank or vice versa. They utilize register-to-register addressing only. All of these instructions will execute in the DP; some will execute in the AP as well. Both operands must belong to the same processor, except for those that act on registers from the DP and U Bank.

ADD	Add (AP or DP)
ADDC	Add with carry
AMD	Bitwise And
CMP	Compare
DEC	Decrement (AP or DP)
INC	Increment (AP or DP)
MOV	Move within DP Move within AP Move between DP and U Bank
EX	Exchange registers within AP Exchange registers within DP Exchange registers between DP and U-bank
EXLN	Exchange six registers used in line drawing with alternate register block
MULS	Multiply signed
MULU	Multiply unsigned
NOT	Bitwise Complement
OR	Bitwise Or
ROLC	Rotate Left with Carry
RORC	Rotate Right with Carry
SHL	Shift Left
SHRA	Shift Right, Arithmetic
SHRL	Shift Right, Logical (AP or DP)
SUB	Subtract (AP or DP)
SUBC	Subtract with Carry
TEST	Test with Mask
XOR	Bitwise Exclusive-Or

Program Control Instructions

The Program Control instructions affect the program flow by causing non-sequential instruction execution or by suspending processing. A number of these instructions execute conditionally; these are indicated by the **cc** field in their mnemonics, which is understood to mean one of the following interpretations of the condition code bits of the PSR:

Z	Zero	NZ	Not_Zero	(DP)
C	Carry	NC	No_Carry	(DP)
V	oVerflow	NV	No_oVerflow	(DP)
H	Higher	NH	Not_Higher	(DP)
N	Negative	NN	Not_Negative	(DP)
GT	Greater Than	LE	Less or Equal	(DP)
LT	Less Than	GE	Greater or Equal	(DP)
AZ	ApZero	NAZ	Not_ApZero	(AP)
AC	ApCarry	NAC	No_ApCarry	(AP)
W	Within	NW	NotWithin	(Clipper)
K		NK		
(K = 1 implies "character available in TNXC")				

Architectural Description (Continued)

ACKVI	Acknowledge VIDEO Interrupt (clear VIP)
BRKn	Break (trap) n
Bcc	Branch conditionally
BR	Branch unconditionally
CALLcc	Call subroutine conditionally
CALL	Call subroutine unconditionally
HALT	Halt instruction execution
INITB	Initalize BPU(s), i.e., force RSTO low for two clock periods
NOP	No operation
RET	Return from subroutine unconditionally
RETcc	Return from subroutine conditionally
RETI	Return from interrupt

Graphics Instructions

The Graphics instructions include two classes: those that actually draw, that is, those by means of which the RGP modifies memory in the drawing space by means of the BPU(s), and those that do setup in preparation for drawing. The setup instructions are considered first in the following listing.

The RGP maintains the concept of *current point*, analogous to the current location of the pen on a conventional plotter. Certain graphics instructions can be performed in one of two modes: relative to the current point *(relative)* and relative to the origin *(absolute)*. Instructions that can be performed in either mode are shown below in both mnemonic forms. The *A* suffix indicates absolute mode.

SETPT SETPTA	Set drawing point, given DSAD, DSWRP, x and y
SETPTS	Set source point, given BSAD, BSWRP, x and y
SETLN SETLNA	Calculate and retain parameters for Bresenham line-drawing algorithm, but do not draw line
BT *ulsd* *u* = {UD} *l* = {LR} *s* = {MB} *d* = {CW}	Perform BITBLT of size BWD and BHT, from source at BSAD with warp BSWRP, to destination at DSAD with warp DSWRP. *u* and *l* control BITBLT direction. *s* and *d* control reading source and destination.
DRPT	Draw point at DSAD
DRLN DRLNA	Draw line
DRLNS	Draw line using previously-calculated parameters (see SETLN/SETLNA)
DRPLN DRPLNA	Draw polyline
DRPGN DRPGNA	Draw polygon
FILLA*d*	Fill polygon. *d* controls reading the destination during the fill.
FILLT*d*	Fill trapezoid, using previously established register values. *d* controls reading the destination during the fill.
DCH*uld*	Draw character high. *u, l* and *d* control BITBLT direction and reading the destination
DCL*uld*	Draw character low. *u, l* and *d* control BITBLT direction and reading the destination
DCN*uld*	Draw character, next. *u, l* and *d* control BITBLT direction and reading the destination
DCW*uld* [An++]	Draw character, word. *u, l* and *d* control BITBLT direction and reading the destination

INITIAL OPERATION

When the RGP is placed into the reset state (see $\overline{\text{RSTI}}$), several registers revert to known states, and instruction execution begins. The following registers are initialized:

PC	Points to location 0
PSR	Bits VIE, EIE, PTE and CLE are zero
VCR	Fields VRX, SE, SM, SI, SC, RM and RAI are zero

Since interrupts cannot be processed properly before certain initialization has been performed, all interrupts are disabled when the RGP is placed into the reset state. Maskable interrupts must be enabled explicitly, while the nonmaskable interrupt becomes enabled as soon as a new value is stored into PSR.

The RGP begins execution by alternately fetching and executing instructions starting at address 0. Typically, this initial code is responsible for establishing base pointers for data and stack areas and generally establishing the software environment, as with any microprocessor. Next, necessary data structures and pointers are initialized to support the graphics environment. Any peripherals that reside in the RGP's memory space can be initialized at this point. Finally, the internal video refresh controller is programmed in a manner consistent with the CRT monitor being used (if any) and is enabled.

Architectural Description (Continued)

Operation beyond this point is highly implementation-dependent. In a workstation application, the RGP might execute a communications protocol with another processor upstream in the graphics pipeline, awaiting the arrival of a display list to be executed. Upon receipt, the RGP would directly execute or interpret the display list, rasterizing graphics primitives into the display buffer. Upon executing the final display list instruction, the RGP would typically signal completion, thus completing the protocol with the upstream processor and allowing the process to continue.

Alternatively, in a standalone application like a graphics terminal, the RGP might enter a control program, servicing peripherals and executing a command interpreter. Here, the RGP would be responsible for keyboard, mouse and UART service; at the same time, the RGP might execute a graphics language interpreter, responding to remote host commands by maintaining a graphics environment and drawing into the display buffer.

RGP BUS CYCLES

The RGP generates seven basic bus cycles, which it controls using the BS0, BS1, $\overline{RD}$, $\overline{WR}$ and $\overline{PB}$ status lines. (Note that both $\overline{RD}$, $\overline{WR}$ are status lines only and should not be used as strobes.)

The ALE output serves two main functions. First to de-multiplex the lower 16 address-data lines and second to indicate that the RGP is beginning a bus cycle. The surrounding hardware must interpret the RGP status signals and produce the necessary system level control strobes.

RGP bus cycles are of two basic types: non-drawing and drawing.

Non-Drawing Cycles

All non-drawing operations use AD0–23 for addressing and use AD0–15 for reading and writing data. BS0–1 distinguish among cycle types (see Table I).

An operand read or write cycle is signaled by values of BS0 = 0, BS1 = 0. $\overline{RD}$ = 0 and $\overline{WR}$ = 1 for an operand read. For operand write, $\overline{RD}$ = 1 and $\overline{WR}$ = 0.

An instruction fetch cycle is signaled by values of BS0 = 1, BS1 = 0, $\overline{RD}$ = 0 and $\overline{WR}$ = 1.

A video refresh cycle is signaled by values of BS0 = 1, BS1 = 1, $\overline{RD}$ = 0 and $\overline{WR}$ = 1. A video refresh cycle is executed as a result of a $\overline{DRREQ}$ output by the RGP.

All non-drawing cycles use the following protocol, which requires a minimum of three clock cycles. Each clock cycle (PH1 to PH1) corresponds to a T state.

a. ALE is generated during the T1 state.

b. RGP enters a wait loop during the T2 state. T2 is regenerated until $\overline{WAIT}$ is sampled high during PH2 falling. All RGP generated status is static during the T2 period. The RGP can remain waiting in T2 indefinitely.

c. T3 follows T2. For operand and instruction read, data is sampled in state T3 during the falling edge of PH2.

Drawing Cycles

During drawing operations, the RGP generates addresses and status and controls the BPUs via the BPU control lines. All data is passed through the BPUs. The RGP can be viewed as always residing in the drawing destination space; only for BITBLT source read operations does the RGP switch to drawing source space.

A BITBLT source read cycle is signaled by values of $\overline{L/B}$ = 0, BS0 = 0, BS1 = 1, $\overline{RD}$ = 0 and $\overline{WR}$ = 1.

A BITBLT destination write cycle is signaled by values of $\overline{L/B}$ = 0, BS0 = 0, BS1 = 1, $\overline{RD}$ = 1 and $\overline{WR}$ = 0.

A BITBLT destination read modify write cycle is signaled by values of $\overline{L/B}$ = 0, BS0 = 0, BS1 = 1, $\overline{RD}$ = 0 and $\overline{WR}$ = 0.

All shifting, masking, and boolean operations are based on the values previously programmed into the BPU's CRE and FSE registers and the current status of the BPU control lines.

A line drawing read modify write cycle is signaled by values of $\overline{L/B}$ = 1, BS0 = 0, BS1 = 1, $\overline{RD}$ = 0 and $\overline{WR}$ = 0. The RGP outputs B0–3 select a single bit of the addressed word. The value in the BPU pixel latch and the contents of FSE determine the Boolean result on the selected data bit.

All drawing cycles use the following protocol which require a minimum of two clock cycles. Each clock cycle (PH1 to PH1) corresponds to a T state.

a. ALE is generated during the T1 state.

b. RGP enters a wait loop during the T2 state. T2 is regenerated until $\overline{WAIT}$ is sampled high during PH2 falling. The RGP can remain waiting in T2 indefinitely.

c. The RGP begins execution of the next T1 on the next clock cycle.

BUS ARBITRATION

The RGP can share its bus with another bus master. When the RGP's $\overline{HOLD}$ input is asserted, the RGP completes its current bus cycle, then its address and data lines are at TRI-STATE and asserts $\overline{HLDA}$. Only the address and data lines are TRI-STATE. It remains in this state until $\overline{HOLD}$ is no longer asserted. During this time, all the video refresh signals, including $\overline{DRREQ}$, continue to function.

Absolute Maximum Ratings*

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to + 150°C
Supply Voltage (V_{CC})	−0.5V to 7V
Voltage at Any Pin with Respect to GND	−0.5V to V_{CC} + 0.5V
Package Power Dissipation @ 20 MHz	2.5W @ 25°C

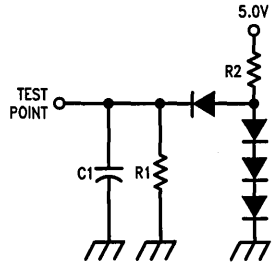
Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.*

***Note:** These are preliminary specifications.

DC Electrical Characteristics* $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, GND = 0V

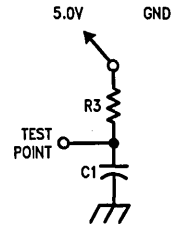
Symbol	Characteristics	Conditions	Min	Typ	Max	Units
V_{IH}			2.0			V
V_{IL}					0.8	V
V_{CH}	MOS Clock High	PH1, PH2 Pins Only, MOS	$V_{CC} - 0.5$			V
V_{CL}	MOS Clock Low	PH1, PH2 Pins Only, MOS			0.3	V
V_{CLT}	MOS Clock Ringing	PH1, PH2 Pins Only, MOS	−0.5		0.5	V
V_{OH}		$I_{OL} = -3$ mA	2.4			V
V_{OL}		$I_{OL} = 3$ mA			0.5	V
I_{IN}	Input Leakage Current	$V_{IN} = V_{IH}$ or V_{IL}			±10	μA
I_{OZ}	TRI-STATE Leakage for A16–A23	$V_O = V_{CC}$ or GND			+60	μA
	TRI-STATE Leakage for All Other Outputs	$V_O = V_{CC}$ or GND			±10	μA
I_{CC1}	Quiescent Current	PH1, PH2 at 20 MHz			50	mA
I_{CC2}	Supply Current	PH1, PH2 at 100 kHz			10	mA
I_{CC3}	Supply Current	PH1, PH2 at 20 MHz			70	mA
C_{IN}	Input Capacitance	f_{in} at 1 MHz			10	pF

*These are preliminary specifications.



TL/F/9427–46

RGP Output Test Load Circuitry



TL/F/9427–47

RGP Output TRI-STATE Test Load Circuitry

Note 1: C1 = 50 pF
R1 = 6 kΩ
R2 = 1.3 kΩ
R3 = 1.8 kΩ

Note 2: Connect SW to +5V for t_{PLZ} and t_{PZL} measurements.

Note 3: Connect SW to GND for t_{PHZ} and t_{PZH} measurements.

AC Electrical Characteristics

All AC timing parameters contained herein are considered *preliminary,* and subject to change without notice. Included, as part of the specifications, is 70°C, worst-case loading vs. propagation delay for the critical signals: ALE and $\overline{PB}$. The graphical information provided is intended to give the designer greater flexibility and understanding when designing with the aforementioned signals.

Symbol	*Figure*	Parameter	Conditions	30 pF Load		50 pF Load	
				Min	Max	Min	Max
tCp	*23*	PH1 or PH2 Clock Period	RE to Next RE				5
tCh	*23*	PH1 or PH2 High Time	RE 50% to Next FE 50%			19	
tnOVL	*23*	PH1, PH2 Non-Overlap Time	PH1 (PH2) FE 50% to Next PH2 (PH1) RE 50%			3	
tnOVLas	*23*	PH1 PH2 Asymmetry Non-Overlap Time	PH1 (PH2) FE 90% to Next PH2 (PH1) RE10%			0	
tLCp	*23*	LCK Period	LCK RE to Next LCK RE Mode 1 & 2 Mode 0 & 3				 3* 2*
tLCh	*23*	LCK High Time	LCK RE 50% to FE 50%			38	
tLCl	*23*	LCK Low Time	LCK FE 50% to RE 50%			38	
tLCKs	*23*	LCK High Setup Time	Before PH1 RE 50%			20	
tLCKh	*23*	LCK High Hold Time	After PH1 RE 50%			0	
tDIs	*24*	Data in Setup Time	Before PH2 FE 50%			15	
tDIh	*24*	Data in Hold Time	After PH2 FE 50%			12	
tDv	*26*	Data Valid Time	After PH2 RE 50%				44
tDiv	*26*	Data Invalid Time	After PH2 RE 50%			6	
tADf	*20*	AD 15–0 Bus Floating	After PH2 RE 50%			5	35
tALv	*20*	Address 15–0 Valid	After PH2 RE 50%				44
tALf	*24*	Address 15–0 Float	After PH2 RE 50%			6	
tALav	*24*	Address 15–0 Setup	Before ALE FE 50%			5	
tALiv	*26*	Address 15–0 Invalid	After PH2 RE 50%			6	
tALaiv	*27*	Address 15–0 Invalid	After ALE FE 50%			15	
tAHv	*20*	Address 23–16 Valid	After PH2 RE 50%				44
tAHiv	*24*	Address 23–16 Invalid	After PH2 RE 50%			6	
tAHf	*20*	Address 23–16 Floating	After PH2 RE 50%			5	35
tAHav	*24*	Address 23–16 Setup	Before ALE FE 50%			5	
tLMEv	*28*	LME Valid	After PH1 RE 50%				36
tRMEv	*28*	RME Valid	After PH1 RE 50%				36
tFWRv	*27*	FWR Valid	After PH1 RE 50%				36
tFRDv	*28*	FRD Valid	After PH1 RE 50%				36
tLMEiv	*28*	LME Invalid	After PH1 RE 50%			6	
tRMEiv	*28*	RME Invalid	After PH1 RE 50%			6	
tFWRiv	*27*	FWR Invalid	After PH1 RE 50%			6	
tFRDiv	*28*	FRD Invalid	After PH1 RE 50%			6	
tLBv		$\overline{L/B}$ Valid	After PH1 RE 50%				44
tBSEv	*27*	BSE Valid	After PH1 RE 50%				44
tLBiv		$\overline{L/B}$ Invalid	After PH1 RE 50%			6	
tBSEiv	*27*	BSE Invalid	After PH1 RE 50%			6	
tHALTv	*34*	$\overline{Halt}$ Valid	After PH1 RE 50%				42

*MHz

AC Electrical Characteristics

All AC timing parameters contained herein are considered *preliminary,* and subject to change without notice. Included, as part of the specifications, is 70°C, worst-case loading vs. propagation delay for the critical signals: ALE and $\overline{PB}$. The graphical information provided is intended to give the designer greater flexibility and understanding when designing with the aforementioned signals. (Continued)

Symbol	*Figure*	Parameter	Conditions	30 pF Load		50 pF Load	
				Min	Max	Min	Max
tHALTiv	*34*	$\overline{HALT}$ Invalid	After PH1 RE 50%			7	
tHOLDs	*20*	$\overline{HOLD}$ Setup	Before PH2 FE 50%			10	
tHOLDiv	*20*	$\overline{HOLD}$ Invalid	After PH2 FE 50%			10	
tHLDAv	*20*	$\overline{HLDA}$ Valid	After PH2 RE 50%				38
tHLDAiv	*20*	$\overline{HLDA}$ Invalid	After PH2 RE 50%			6	
tRSTIs	*37*	$\overline{RSTI}$ Setup	Before PH2 FE 50%			15	
tRSTIh	*37*	$\overline{RSTI}$ Hold	After PH2 FE 50%			10	
tPWR	*37*	Min RESET Low Time	After Power On				12*
tRSTOv	*38*	$\overline{RSTO}$ Valid	After PH1 RE 50%				44
tRSTOiv	*38*	$\overline{RSTO}$ Invalid	After PH1 RE 50%			6	
tALEv	*20*	ALE Valid	After PH2 RE 50%				32
tALEiv	*20*	ALE Invalid	After PH2 FE 50%			6	
tALEw	*20*	ALE Width	ALE RE 0.8V ALE FE 0.8V			17	
tWAITs	*21*	$\overline{WAIT}$ Setup	Before PH2 FE 50%			19	
tWAITh	*21*	$\overline{WAIT}$ Hold	After PH2 FE 50%			10	
tBSv	*20*	BS 1-0 Valid	After PH1 RE 50%				40
tRDv	*20*	$\overline{RD}$ Valid	After PH1 RE 50%				40
tWRv	*20*	$\overline{WR}$ Valid	After PH1 RE 50%				40
tBSiv	*24*	BS 1-0 Invalid	After PH1 RE 50%			6	
tRDiv	*24*	$\overline{RD}$ Invalid	After PH1 RE 50%			6	
tWRiv	*24*	$\overline{WR}$ Invalid	After PH1 RE 50%			6	
tBSAv	*20*	BS0-1 Valid	Before ALE RE 50%			5	
tRDAv	*20*	$\overline{RD}$ Valid	Before ALE RE 50%			5	
tWRAv	*20*	$\overline{WR}$ Valid	Before ALE RE 50%			5	
tBv	*30*	B 3-0 Valid	After PH1 RE 50%				36
tBiv	*30*	B 3-0 Hold	After PH1 RE 50%			6	
tPBv	*20*	$\overline{PB}$ Valid	After PH2 RE 50%				36
tPBiv	*24*	$\overline{PB}$ Invalid	After PH2 RE 50%			6	
tPBav	*24*	$\overline{PB}$ Setup	Before ALE FE 50%			5	
tHSYv	*39*	$\overline{HSYNC}$ Valid	After PH1 RE 50%				69
tHSYiv	*39*	$\overline{HSYNC}$ Invalid	After PH1 RE 50%			9	
tDRQv	*31*	$\overline{DRREQ}$ Valid	After PH1 RE 50%				54
tDRQiv	*31*	$\overline{DRREQ}$ Invalid	After PH1 RE 50%			6	

*MHz

AC Electrical Characteristics

All AC timing parameters contained herein are considered *preliminary,* and subject to change without notice. Included, as part of the specifications, is 70°C, worst-case loading vs. propagation delay for the critical signals: ALE and $\overline{PB}$. The graphical information provided is intended to give the designer greater flexibility and understanding when designing with the aforementioned signals. (Continued)

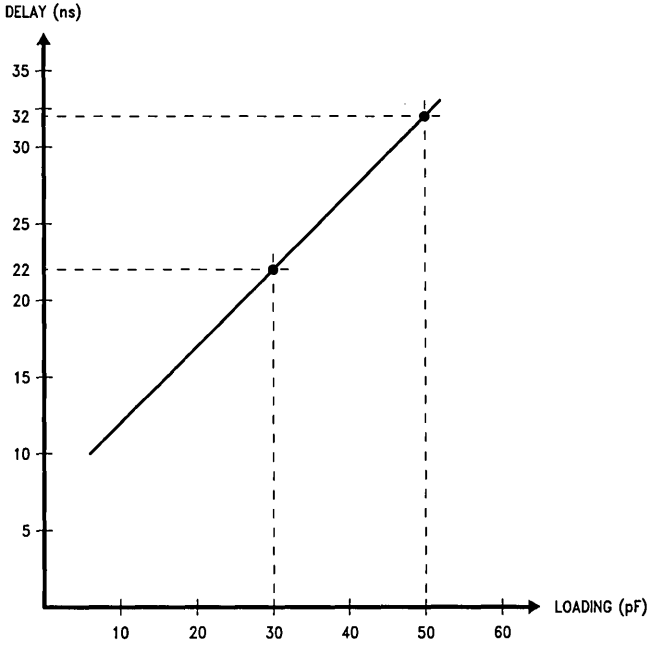
Symbol	*Figure*	Parameter	Conditions	30 pF Load		50 pF Load	
				Min	Max	Min	Max
tINTs	*35*	INT Setup	After PH2 FE 50%				15
tINTh	*35*	INT Hold	After PH2 FE 50%				10
tNMIw	*36*	NMI Min Width	FE to RE 50%			20	
tBLKv	*40*	$\overline{BLANK}$ Valid	After PH1 RE 50%				44
tBLKiv	*40*	$\overline{BLANK}$ Invalid	After PH1 RE 50%			6	
tVSYOv	*41*	$\overline{VSYNC}$ Output Valid	After PH1 RE 50%				69
tVSYOiv	*41*	$\overline{VSYNC}$ Output Invalid	After PH1 RE 50%			9	
tVSYIs	*42*	$\overline{VSYNC}$ Input Setup	After PH2 FE 50%			50	
tVSYIh	*42*	$\overline{VSYNC}$ Input Hold	After PH2 FE 50%			50	

Note 1: All parameters (except tLCp) are times in ns. Usually a number appears either in the column titled Max or in the column titled Min, since in most cases, only one of these is of significance. In cases where both are important, both appear.

Note 2: The column titled Reference gives the names of a reference signal from which the given parameter is measured. The designation RE or FE following a signal name indicates the rising edge or falling edge of that signal. A percentage following RE or FE indicates the percent of the total rise or fall of the signal at the point from which the parameter being described is measured.

Typical Performance Characteristics

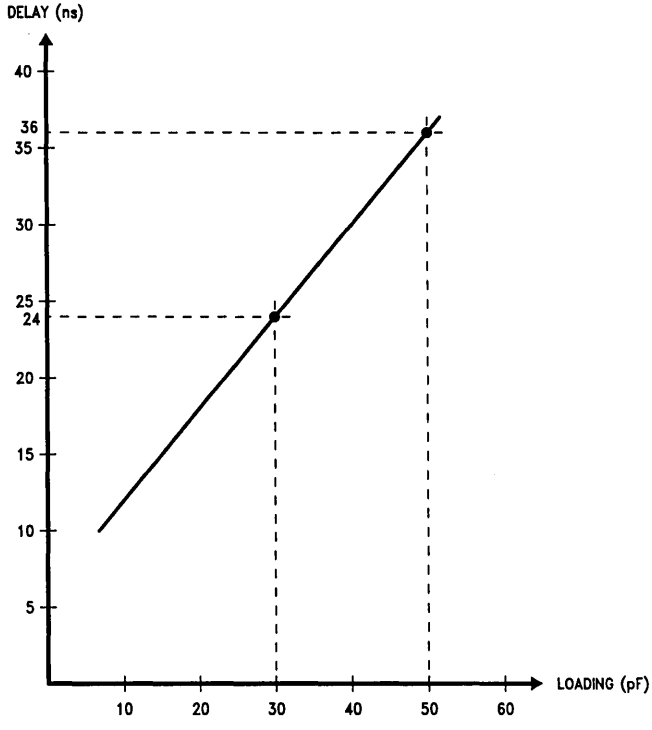
Worst Case ALE Propagation Delay at 70°C



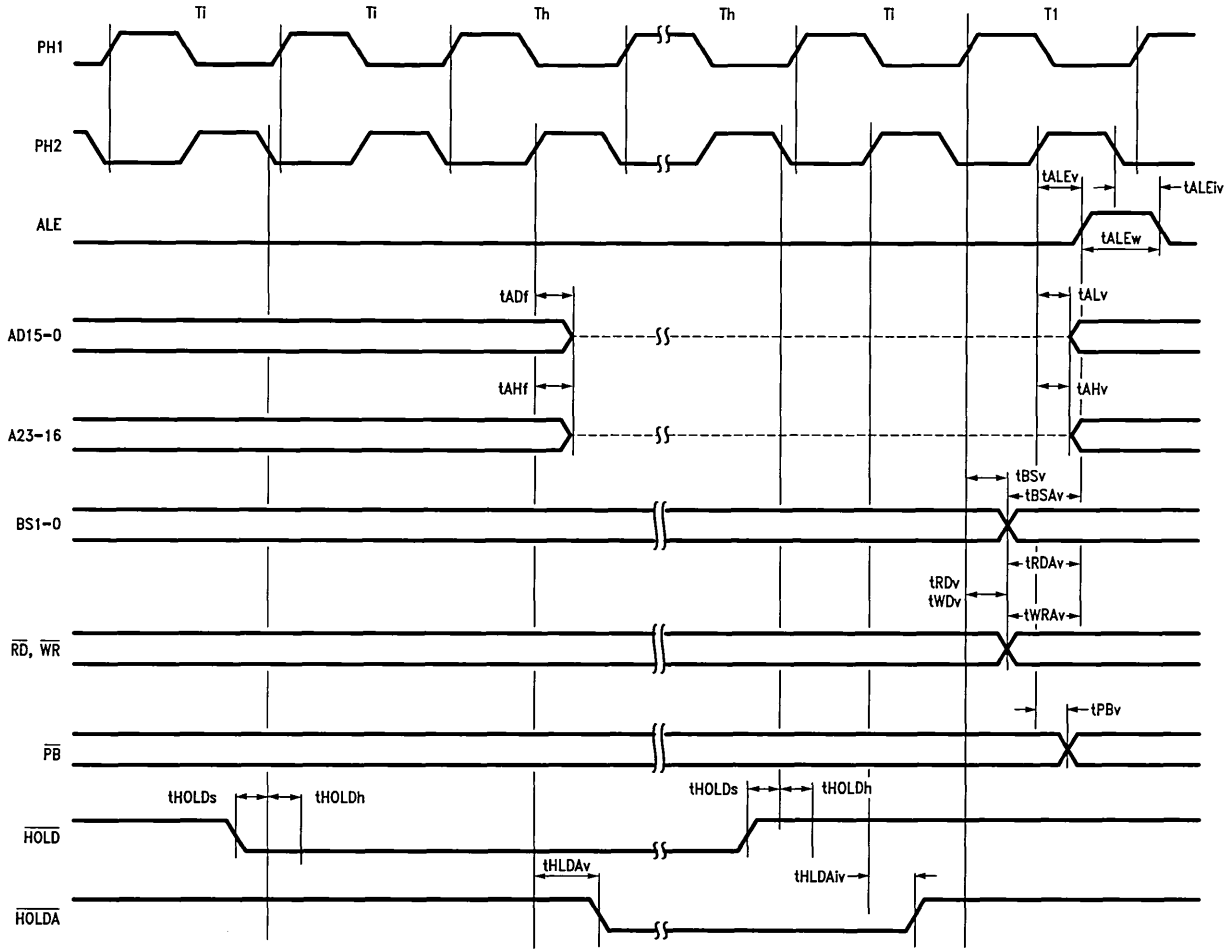
TL/F/9427–33

Typical Performance Characteristics (Continued)

Worst Case $\overline{PB}$ Propagation Delay at 70°C

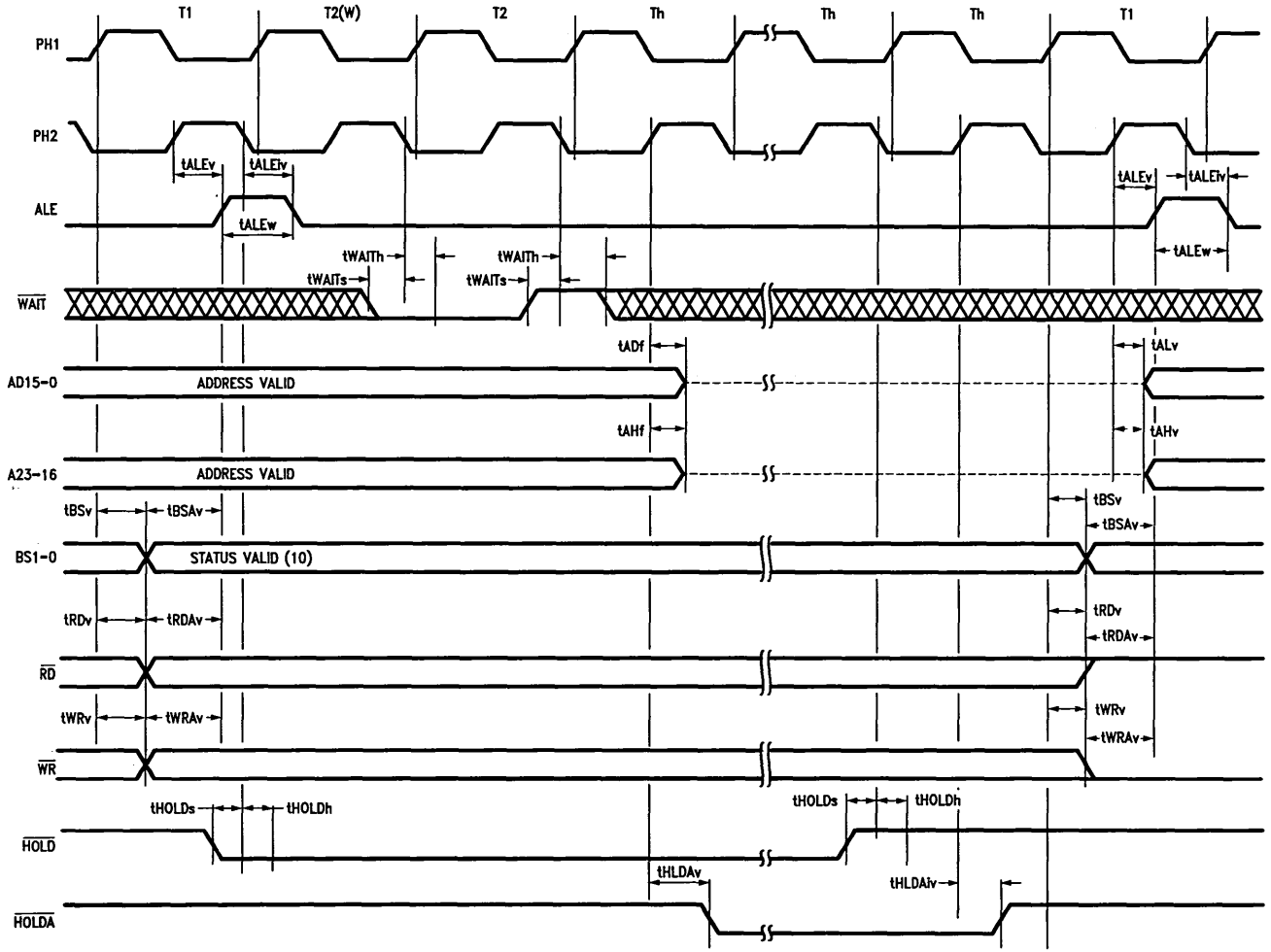


TL/F/9427–34



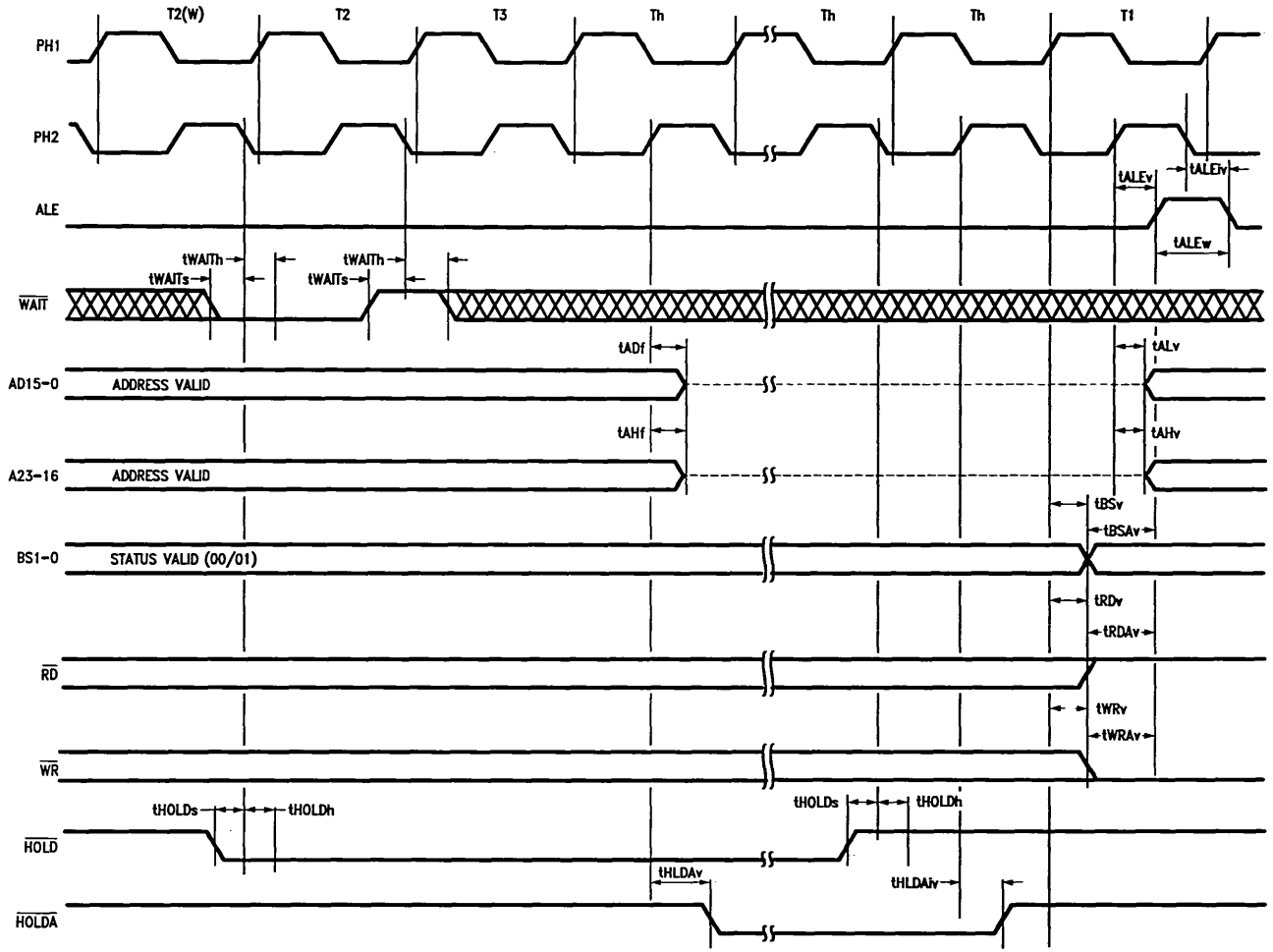
TL/F/9427–21

FIGURE 20. HOLD Timing (Bus Initially Idle)



TL/F/9427–22

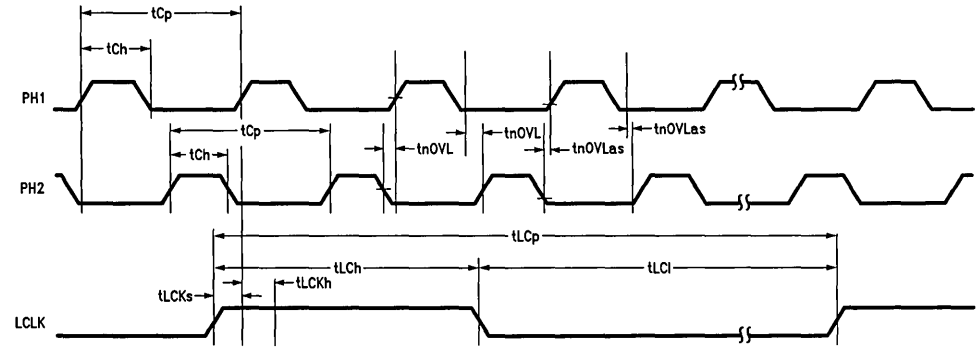
FIGURE 21. HOLD Timing (Bus Busy with Drawing Cycle)



TL/F/9427–23

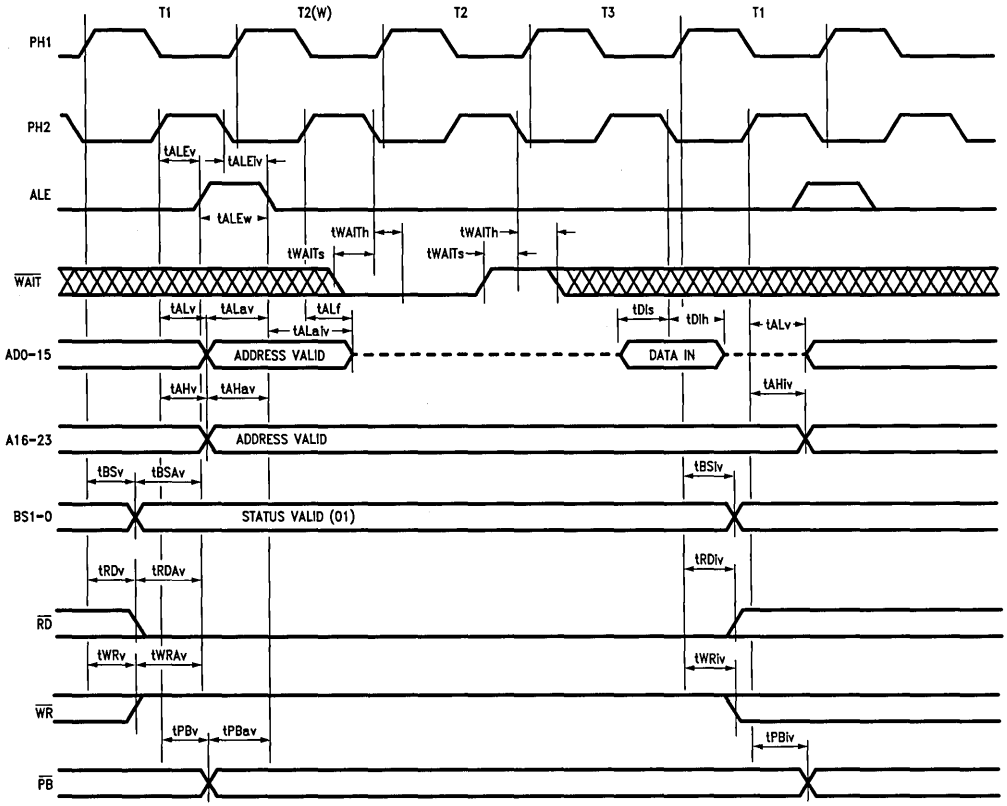
FIGURE 22. Hold Timing (Bus Busy with Non-Drawing Cycle)

Timing Waveforms (Continued)



TL/F/9427–24

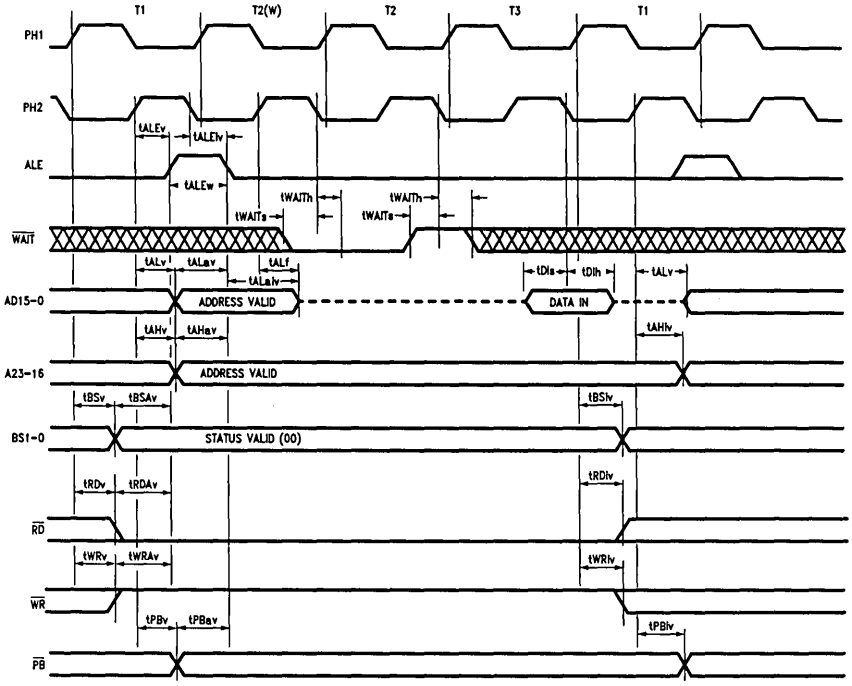
FIGURE 23. RGP LCLK Timing



TL/F/9427–25

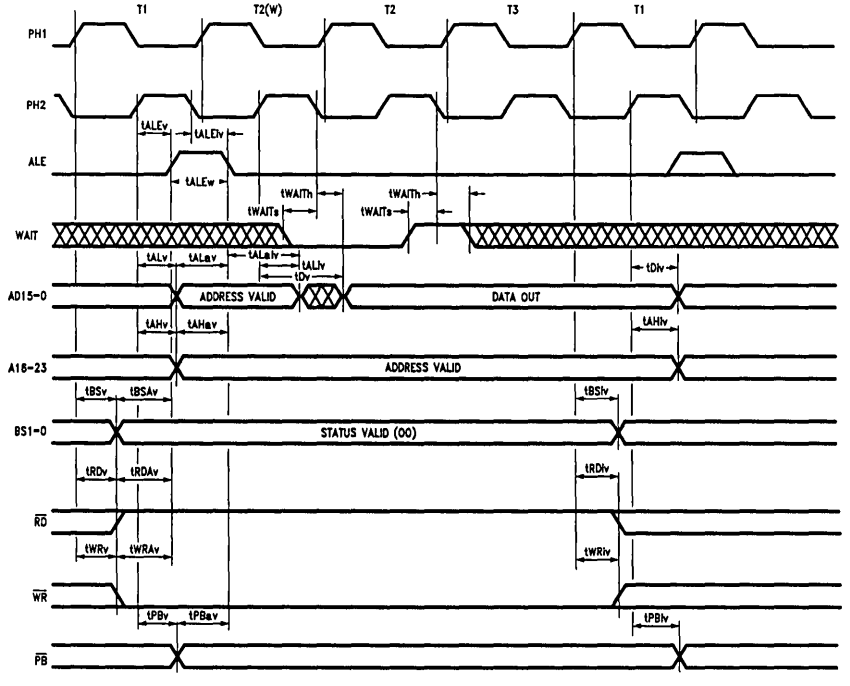
FIGURE 24. Instruction Read Cycle Timing

Timing Waveforms (Continued)



TL/F/9427-26

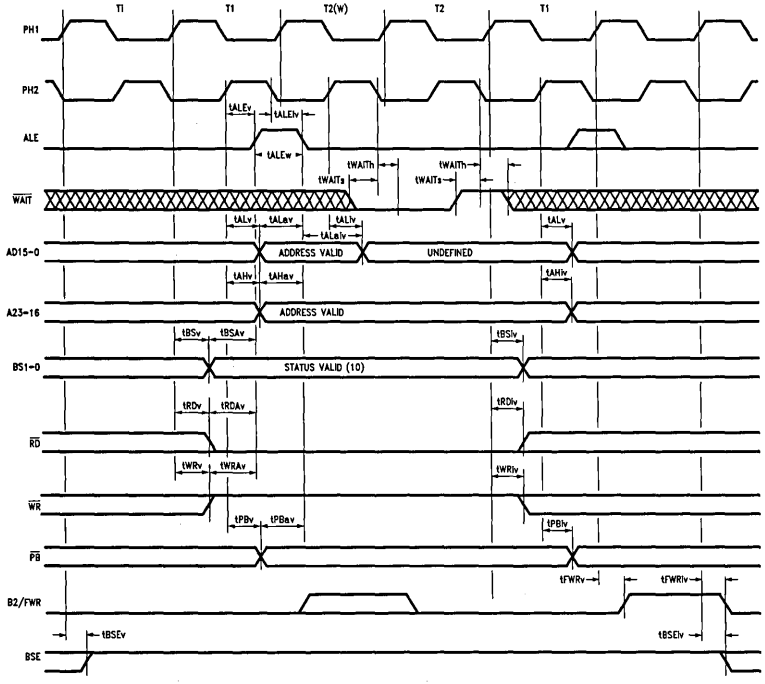
FIGURE 25. Operand Read Cycle Timing



TL/F/9427-27

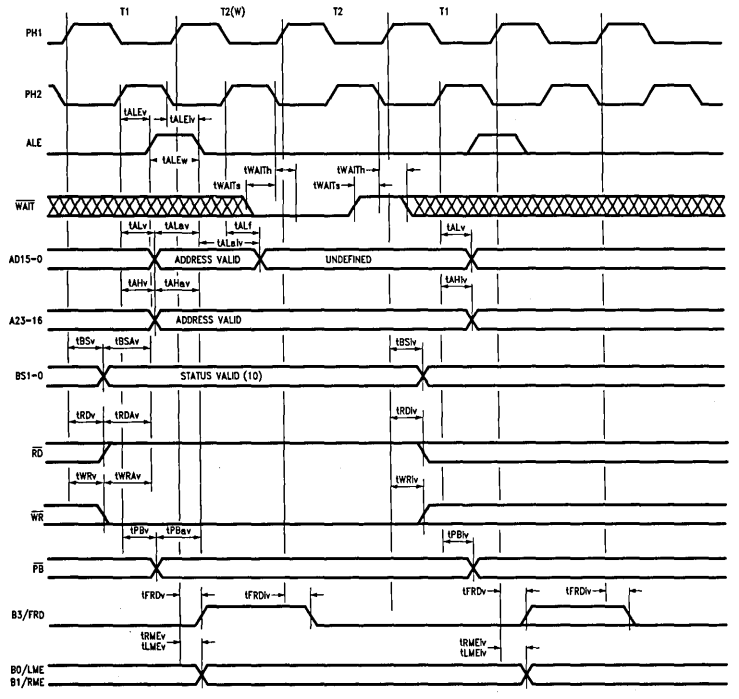
FIGURE 26. Operand Write Cycle Timing

Timing Waveforms (Continued)



TL/F/9427–28

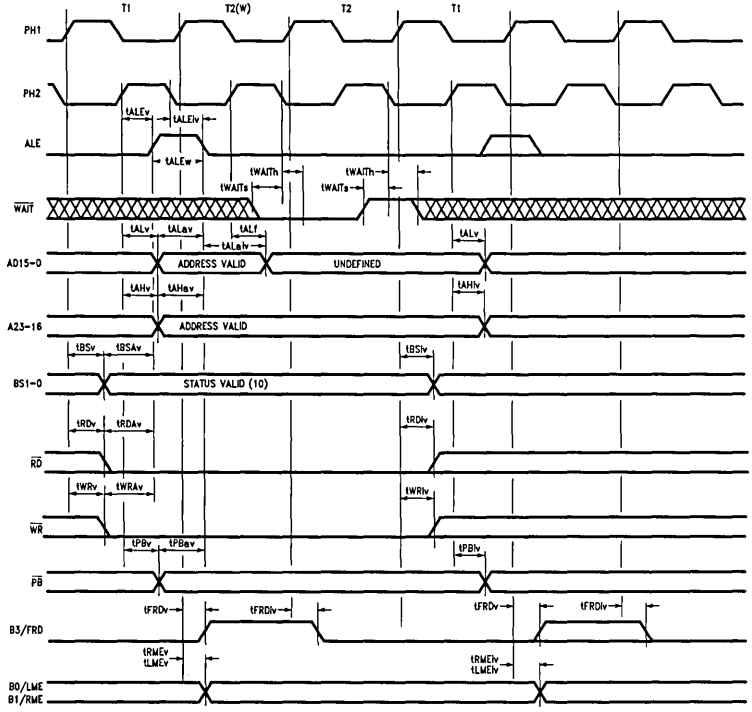
FIGURE 27. BITBLT Source Read Cycle Timing



TL/F/9427–29

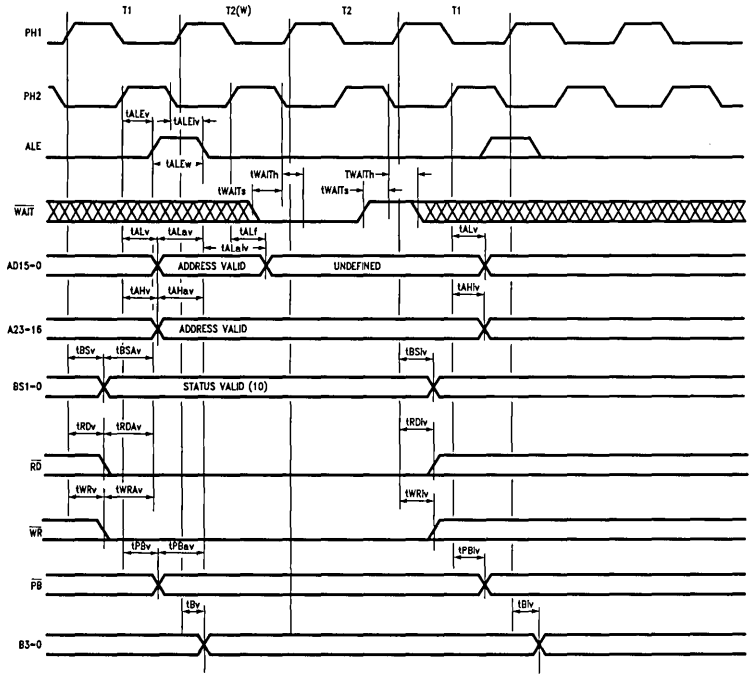
FIGURE 28. BITBLT Destination Write Cycle Timing

Timing Waveforms (Continued)



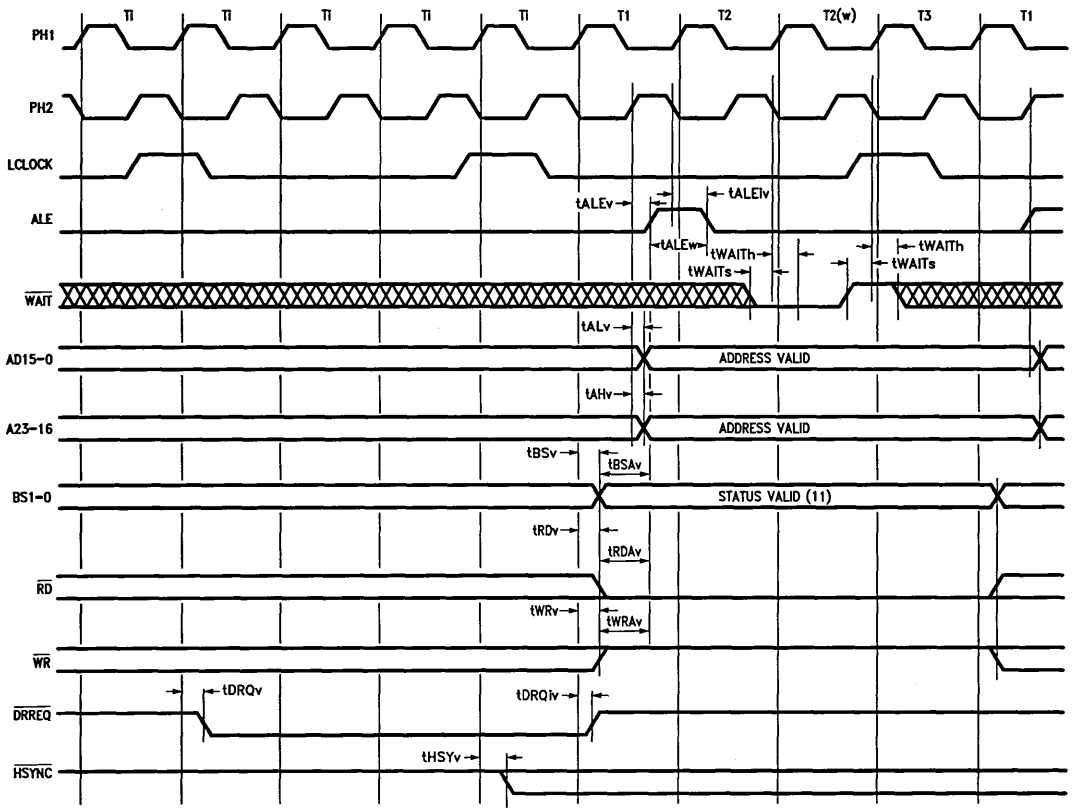
TL/F/9427–30

FIGURE 29. BITBLT Destination Read-Modify-Write Cycle Timing



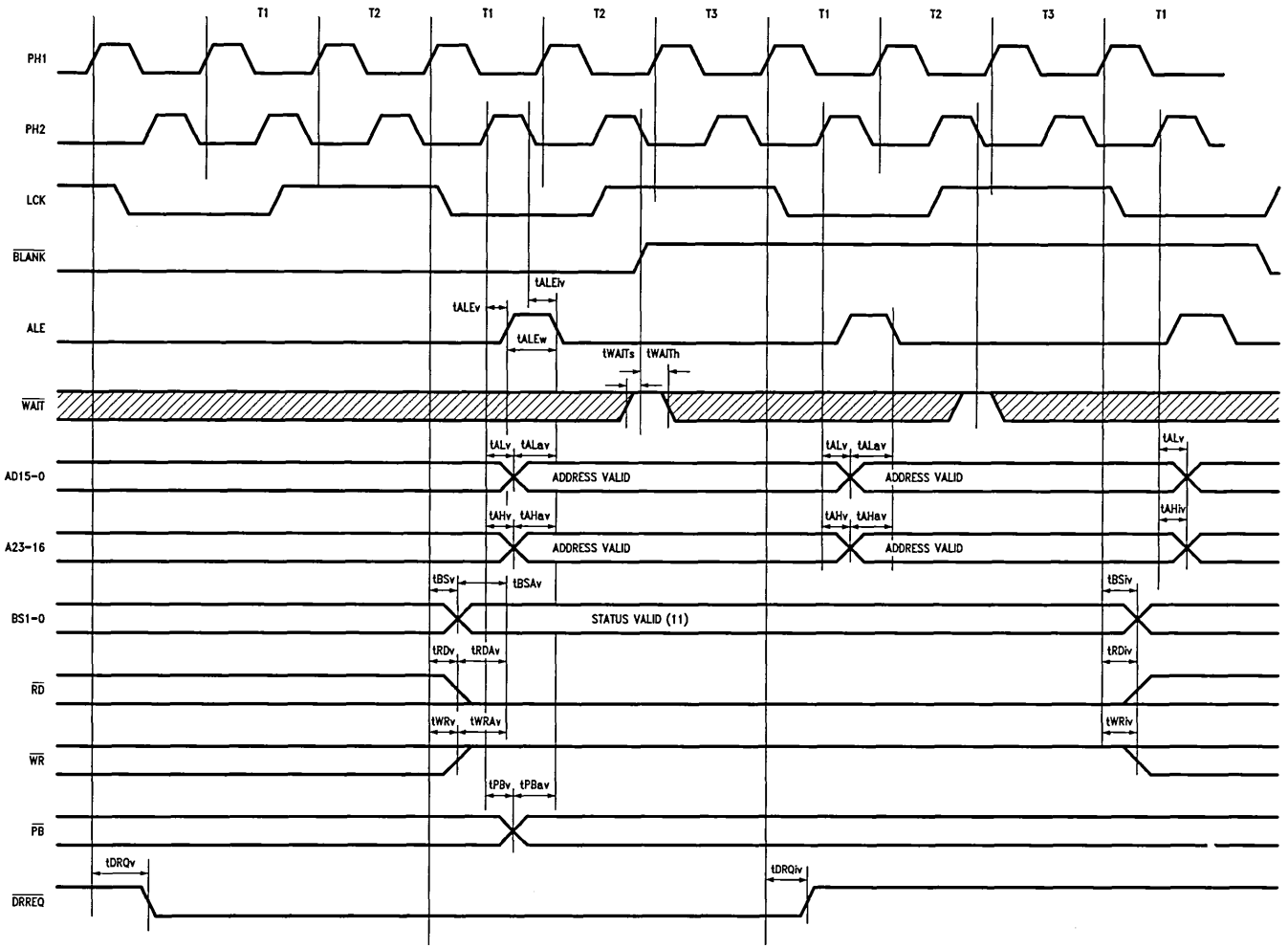
TL/F/9427–31

FIGURE 30. Line Drawing Read-Modify-Write Cycle



TL/F/9427-32

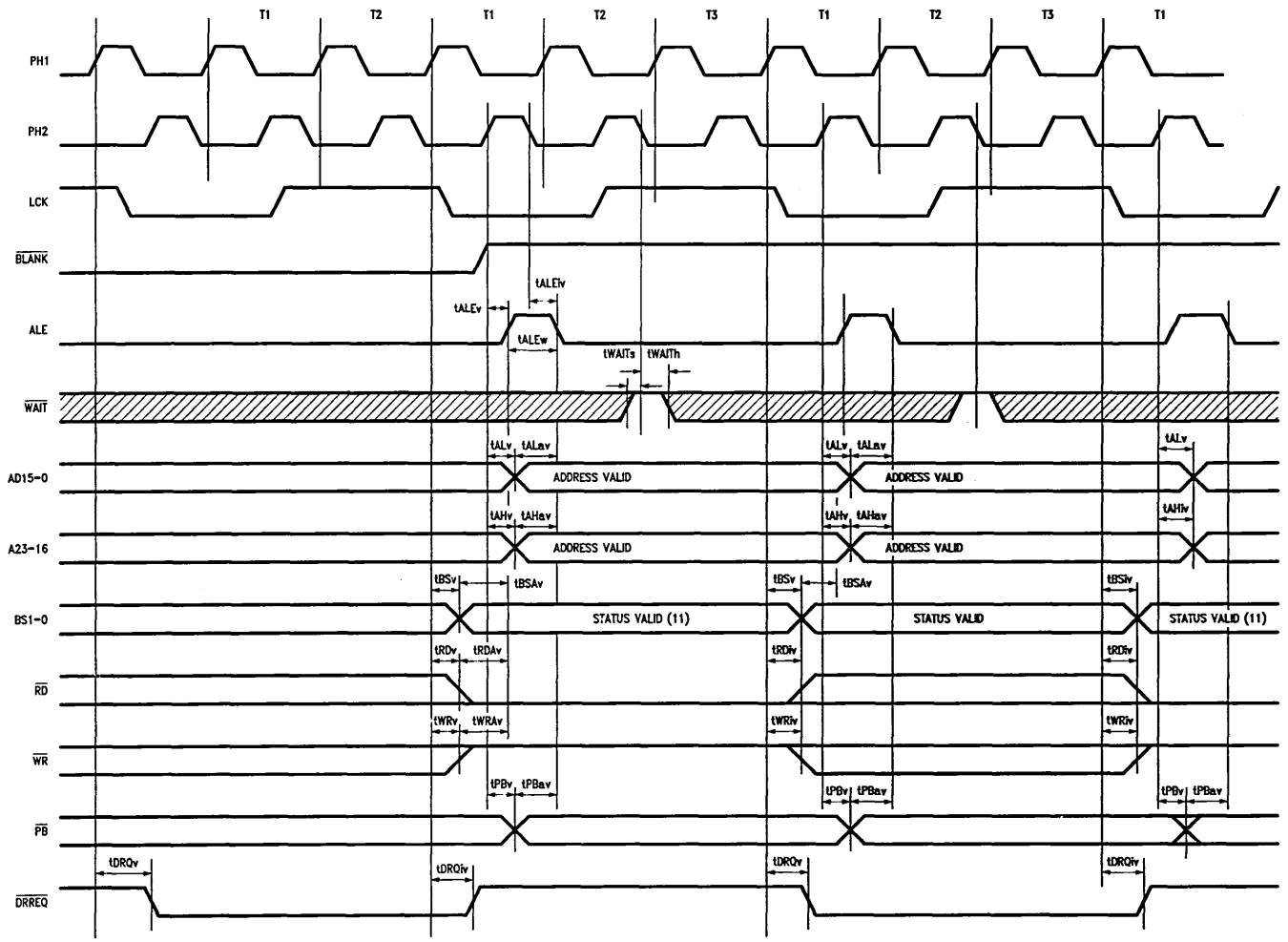
FIGURE 31. Mode 3 Video Refresh Cycle Timing



TL/F/9427–35

FIGURE 32. Mode 1 Display Refresh

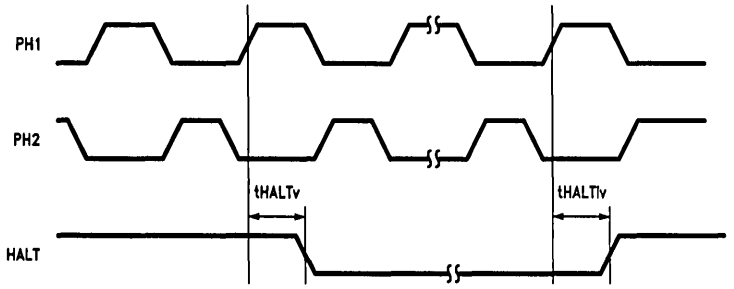
Timing Waveforms (Continued)



TL/F/9427–36

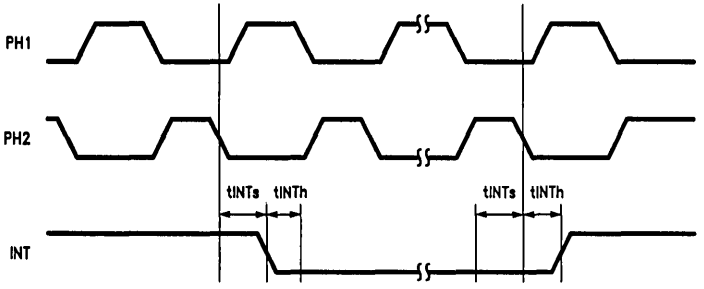
FIGURE 33. Mode 2 Display Refresh

Timing Waveforms (Continued)



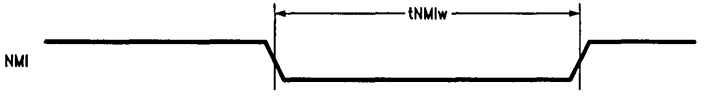
TL/F/9427–37

FIGURE 34. Halt Timing



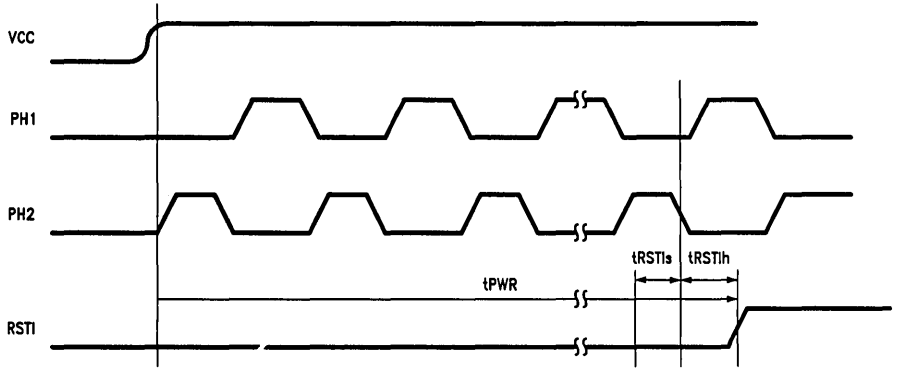
TL/F/9427–38

FIGURE 35. Interrupt Timing



TL/F/9427–39

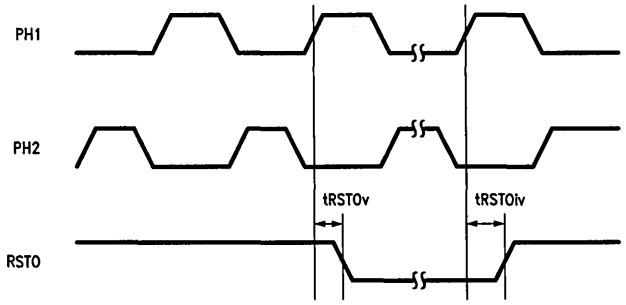
FIGURE 36. Non-Maskable Input Timing



TL/F/9427–40

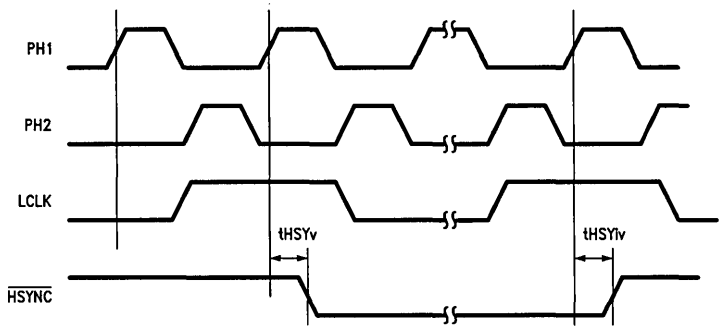
FIGURE 37. RESET Input Timing

Timing Waveforms (Continued)



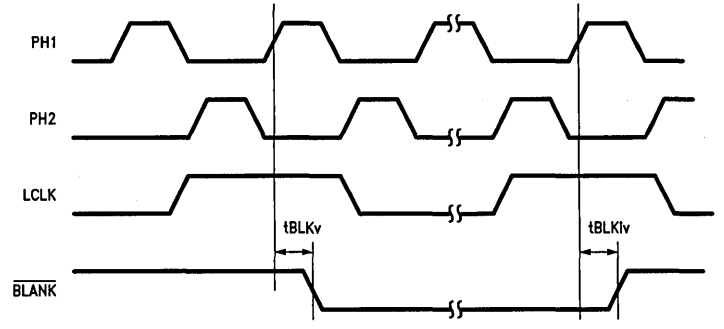
TL/F/9427–41

FIGURE 38. RESET Output Timing



TL/F/9427–42

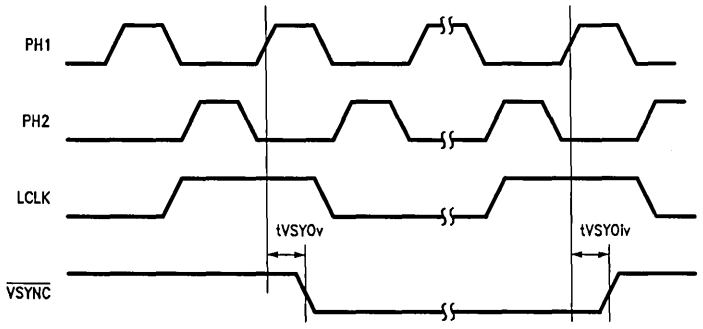
FIGURE 39. $\overline{\text{HSYNC}}$ Timing



TL/F/9427–43

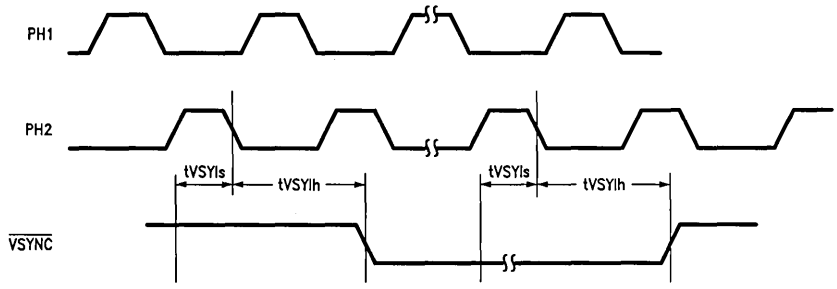
FIGURE 40. $\overline{\text{BLANK}}$ Timing

Timing Waveforms (Continued)



TL/F/9427–44

FIGURE 41. $\overline{\text{VSYNC}}$ Output Timing



TL/F/9427–45

FIGURE 42. $\overline{\text{VSYNC}}$ Input Timing

National Semiconductor

PRELIMINARY

DP8510 BITBLT Processing Unit

General Description

The DP8510 BITBLT Processing Unit (BPU) is a high-performance microCMOS device designed for use in raster graphics applications. It implements, in high-speed pipelined logic, the data operations which are fundamental to BITBLT (BIT boundary Block Transfer) graphics: shifting, masking and bitwise logic operations. Under control of external hardware such as a state machine or a general-purpose microprocessor, it provides all necessary data path operations, easing the implementation of a wide variety of BITBLT systems. A number of input pins control the proper data flow in the BPU. A simple handshake scheme is used to interface the CPU, the BPU and the memory system.

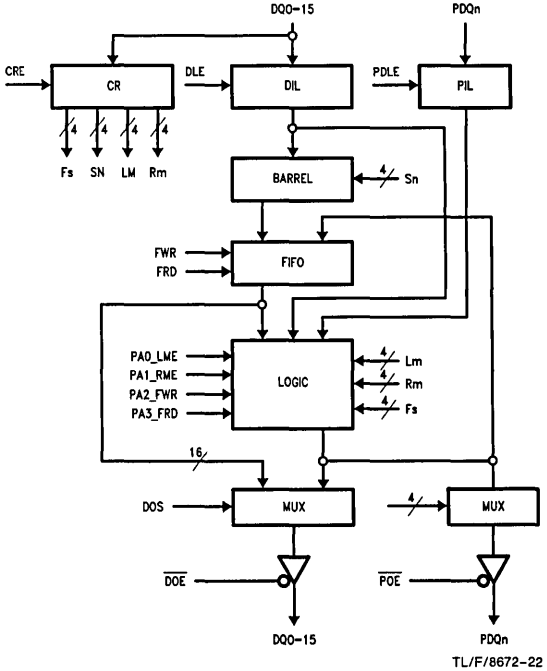
The BPU has two modes, BITBLT and line drawing. The mode is set by the $\overline{B}$/L pin. The line-drawing mode can be treated as a special case BITBLT with height and width equal to one.

In order to perform a BITBLT operation, the BPU's control register must first be loaded with four parameters: the shift number, left and right masks and the function select code, a total of 16 bits. BITBLT can then proceed, as directed by an external processor or state machine. It is the responsibility of the controller to generate appropriate addresses for the BITBLT, to interface with the frame buffer's memory control circuitry, and to control the BPU itself.

Features

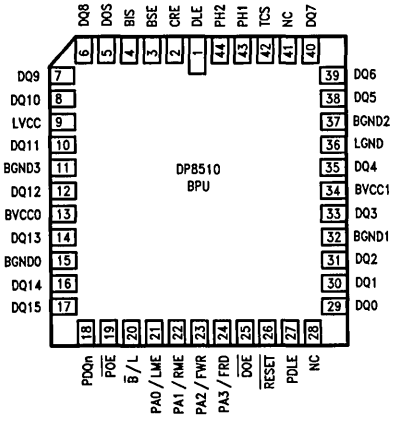
- Supports all 16 classical BITBLT functions
- Pipelined data input for high system throughput
- Flexible architecture allows BPU to be used with a state machine or processor
- Multiple BPUs can be used for multiple bitplane/color applications
- Line drawing support
- Compatible with static or dynamic RAMs, including Video DRAMs
- Compatible with page mode, nibble mode and static column RAMs
- 32-bit to 16-bit barrel shifter
- 16-bit data port
- 16-word FIFO
- 16-bit logic operations
- 20 MHz operation
- Single +5 volt supply
- All inputs and outputs TTL-compatible
- Packaged in a 44-pin PLCC
- Single-bit pixel I/O port
- A member of National's Advanced Graphics Chip Set
- microCMOS technology

Block and Connection Diagrams



TL/F/8672-22

Plastic Chip Carrier



TL/F/8672-2

Top View

Order Number DP8510V
See NS Package Number V44A

Pin Definitions

DQ0–DQ15: Data I/O Port, 16 bits wide. This is the main data port which is connected to the frame buffer. It serves as the 16-bit input to the Data Input Latch for both source and destination data. When $\overline{DOE}$ is active (low), this port serves as data output.

$\overline{DOE}$: Data Output Buffer Enable. A low signal on this pin enables the data output buffers of DQ0–DQ15.

PDQn: Pixel Data I/O Port, 1 bit wide. This I/O port is used in the line drawing mode only. It serves as the single bit input to the Pixel Input Latch to provide a source bit for line drawing. When $\overline{POE}$ is active (low), this port serves as an output for the pixel selected by PA0–PA3.

$\overline{POE}$: Pixel Output Buffer Enable. A low signal on this pin enables the pixel output buffer. This allows the CPU to read back the pixel data/value from the frame buffer in a multiple bit-plane system.

$\overline{B}$/L: BITBLT or Line Drawing. A low on this pin enables the BPU for BITBLT operation. A high on this pin sets the BPU to the line drawing mode.

PA0/LME: Pixel Address 0 or Left Mask Enable. When the BPU is in the line drawing mode, this pin inputs the least significant pixel address. When the BPU is in the BITBLT mode, this pin receives the Left Mask Enable signal. This input must be synchronized with respect to the falling edge of PH2.

PA1/RME: Pixel Address 1 or Right Mask Enable. When the BPU is in the line drawing mode, this pin inputs the second least significant pixel address. When the BPU is in the BITBLT mode, this pin receives the Right Mask Enable signal. This input must be synchronized with respect to the falling edge of PH2.

PA2/FWR: Pixel Address 2 or FIFO Write control. When the BPU is in the line drawing mode, this pin inputs the third least significant pixel address. When the BPU is in the BITBLT mode, this pin is the FIFO write control input. This input must be synchronized with respect to the falling edge of PH2.

PA3/FRD: Pixel Address 3 or FIFO Read control. When the BPU is in the line drawing mode, this pin inputs the most significant pixel address. When the BPU is in the BITBLT mode, this pin is the FIFO read control input. This input must be synchronized with respect to the falling edge of PH2.

BIS: Barrel Input Select. This signal controls the multiplexer prior to the BPU's barrel shifter. If this signal is high, a wordwise swap is performed between the two 16-bit inputs to the barrel shifter. If this signal is low, no swap is performed. Therefore, if this signal is low, the BIL register serves as the most-significant word to the barrel shifter, with the DIL-Source register serving as the least significant word. Conversely, when this signal is high, DIL Source serves as the most significant input word to the barrel shifter, with BIL being the least significant word.

BSE: BITBLT Source Enable, enables the BITBLT source input data path and controls the latching function of the BITBLT source pipeline register. BSE should be held low (disabled) during the BITBLT destination data read/write cycles. This input must be synchronized with respect to the falling edge of PH2.

TCS: TTL Clock Select. This pin should tie to either V_{CC} or Ground. A high level on this pin selects the TTL level clock input. The use of a conventional TTL clock, permitted at clock frequencies up to 10 MHz, simplifies system design. When using TTL clock all references to the falling edge of PH2 must be changed to the rising edge of PH1. A low level selects PH1 and PH2 (MOS level clocks) as the BPU clock inputs.

PH1: Phase 1 clock input or the TTL clock input. When TCS is set low, this is the PH1 clock input, MOS level, maximum clock rate 20 MHz. When the TCS pin is set high, this is the TTL clock input with a 10 MHz maximum rate.

PH2: Phase 2 clock input. MOS level, maximum clock rate 20 MHz. When using PH1 as TTL clock input (TCS high), PH2 must be tied to ground.

CRE: BPU Control Register Enable. A high signal on this pin enables the BPU's Control Register. The data on DQ0–DQ15 is latched into the BPU Control Register on the falling edge of the next PH2 clock. CRE must be synchronized with respect to the valid data and must be removed before the rising edge of the subsequent PH2 clock.

DLE: Data Latch Enable. A high signal on this pin enables the BPU's data input latch. The data on DQ0–DQ15 is latched into the BPU data input latch on the falling edge of the next PH2 clock. DLE must be synchronized with respect to the valid data and must be removed before the rising edge of the subsequent PH2 clock.

Pin Definitions (Continued)

PDLE: Pixel port Data Latch Enable. A high signal on this pin enables the BPU's pixel port data input latch. The data bit on PDQn pin is latched into the one-bit pixel input data latch on the falling edge of the next PH2 clock. PDLE must be synchronized with respect to the valid pixel data and must be removed before the rising edge of the subsequent PH2 clock.

DOS: Data Output Select. DOS selects the data output from either the FIFO (DOS = 1) or the BITBLT logic block (DOS = 0).

$\overline{\text{RESET}}$: FIFO control Reset. A low signal on this pin resets the BPU's FIFO read/write control circuitry. Data previously stored in the FIFO or on-chip latches are unchanged. This pin is controlled by the RGP's RESET line, an open-drain I/O pin. This input must be synchronized with respect to the falling edge of PH2. PA2/FWR and PA3/FRD inputs must be low 1 clock cycle prior to asserting $\overline{\text{RESET}}$ low in order to correctly reset the FIFO counters.

LVCC: Positive supply for on-chip logic circuits. 5V ±10%

LGND: Ground for on-chip logic.

BVCC0–BVCC1: Positive supply for output buffers, two pins. 5V ±10%.

BGND0–BGND3: Ground for output buffers, four pins.

BITBLT Fundamentals

BITBLT, BIT-aligned Block Transfer, is a general operator that provides a mechanism to move an arbitrary size rectangle of an image from one part of the frame buffer to another. During the data transfer process a bitwise logical operation can be performed between the source and the destination data. BITBLT is also called RasterOp: operations on rasters. It defines two rectangular areas, source and destination, and performs a logical operation (e.g., AND, OR XOR) between these two areas and stores the result back to the destination. It can be expressed in simple notation as:

Destination ← Source op Destination.

op: AND, OR, XOR, etc.

FRAME BUFFER ARCHITECTURE

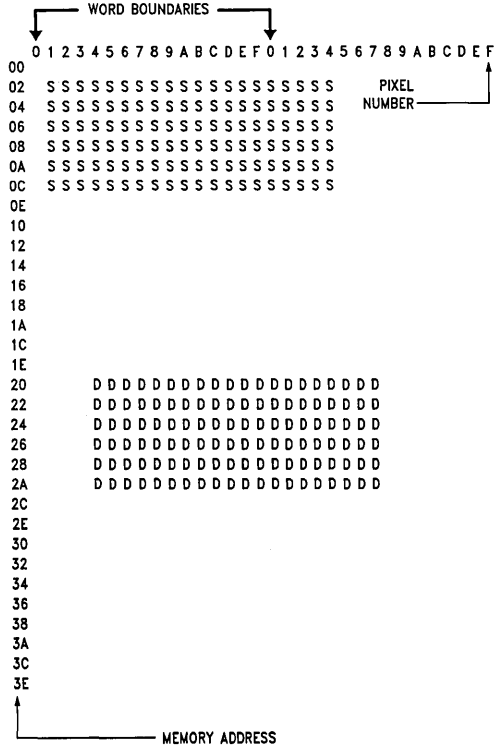
Generally, there are two kinds of frame buffer architectures: PLANE-oriented or PIXEL-oriented. BITBLT takes advantage of the plane-oriented frame buffer architecture's attribute of multiple, adjacent pixels-per-word, facilitating the movement of large blocks of data quickly in a frame buffer. However, the plane-oriented architecture has one inherent problem: the limit of resolution for memory addressing and access is the word, rather than the pixel. The BITBLT source starting address, the BITBLT destination starting address, the BITBLT width and the BITBLT height are all defined in pixels. The BITBLT source data block may start and end at any bit position of any word, and the destination data block also may start and end at any bit position of any word.

BIT ALIGNMENT

Before a logical operation can be performed between the source and the destination data, the source data must first be bit aligned to the destination data. In *Figure 1*, the source data need to be shifted three bits to the right in order to align the first pixel (that is, the pixel at the top left corner) in the source data block to the first pixel in the destination data block. For maximum performance, this alignment function must be implemented with a barrel shifter.

WORD BOUNDARIES AND DESTINATION MASKS

Each BITBLT destination scan line may start and end at any position in any data word. The neighboring bits (the bits sharing the same word address with any words in the destination data block, but not a part of the actual BITBLT rectangle) of the BITBLT destination scan line must remain unchanged after the BITBLT. Due to the plane-oriented frame buffer architecture, all memory operations must be word-aligned. In order to preserve the neighboring bits surrounding the BITBLT destination block, a left mask is needed for all the leftmost data words of the destination block, and a right mask is needed for all the rightmost data words of the destination data block. Both the left mask and the right mask remain the same throughout a given BITBLT operation.



TL/F/8672-3

FIGURE 1. A 32 by 32 Frame Buffer

BITBLT Fundamentals (Continued)

The following example illustrates the bit alignment requirement. In this example, the graphics controller has a 16-bit wide data bus. *Figure 1* shows a 32 pixel by 32 scan line frame buffer which is organized as a long bit stream which wraps around every two words (32 bits). Further, the top left corner of the frame buffer starts from the lowest word in the memory, address 000hex. Each word in the memory contains 16 bits, DQ0–DQ15. The most significant bit of a memory word, DQ15, is defined as the first *displayed* pixel in a word. In other words, memory's DQ15 to DQ0 correspond to pixels 0 to 15 respectively. In this example, BITBLT addresses are expressed in terms of pixel number, starting (with 0) from the upper-leftmost pixel. The BITBLT source starting address is set to 021hex (the second pixel in the third word). The BITBLT destination starting address is set to 204hex (the fifth pixel in the 33rd word). The BITBLT width is set to 013hex (=19 decimal, corresponding to a width of 20 pixels). The BITBLT height is set to 005hex (=5 decimal, corresponding to 6 scan lines).

The left BITBLT mask for the above example is:

0000,1111,1111,1111

The right BITBLT mask for the above example is:

1111,1111,0000,0000

Note: Zeroes in either the left mask or the right mask indicate the destination bits which will not be modified.

BITBLT DIRECTIONS

The BITBLT moves a rectangular block of data in a frame buffer. For a plane-oriented frame buffer, the BITBLT process can be considered a subroutine which has two nested loops. The loops are preceeded by the BITBLT setup computations. The outer loop is the BITBLT source and destination scan line pixel starting address calculation and line count test for completion. The innermost loop is the actual BITBLT data movement for a single BITBLT scan line and word count test for completion. The length of the innermost loop is the word count of the BITBLT width. The length of the second loop is equal to the BITBLT's height (number of scan lines involved in a BITBLT):

```
BITBLT: calculate BITBLT setup parameters ;once per BITBLT
                such as
                width, height
                bit misalignment (shift number)
                left, right masks
                horizontal, vertical directions
                etc
                .
                .

OUTERLOOP: calculate source, dest addresses ;once per scanline
  INNERLOOP: move data and increment addresses ;once per word
  UNTIL       done horizontally
UNTIL         done vertically
RETURN        (from BITBLT).
```

Each loop can be executed in one of two directions: the inner loop from left to right or right to left, the outer loop from top to bottom (down) or bottom to top (up).

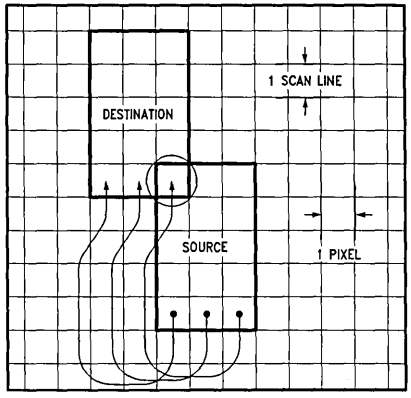
The ability to move data starting from any corner of the BITBLT rectangle is necessary to avoid destroying the BITBLT source data as a result of destination writes when the source and destination are overlapped (i.e., when they share pixels). This situation is routinely encountered while panning or scrolling.

A determination of the correct execution directions of the BITBLT must be performed whenever the source and destination rectangles overlap. *Any* overlap will result in the destruction of source data (from a destination write) if the correct vertical direction is not used. Horizontal BITBLT direction is of concern only in certain cases of overlap, as will be explained below.

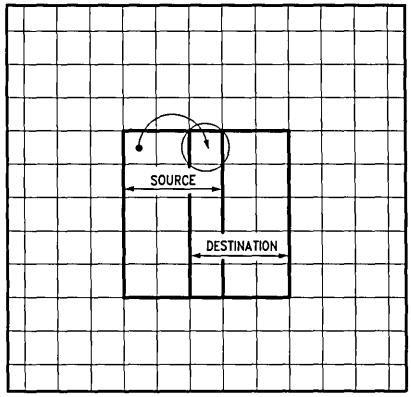
Figure 2 (a) and *(b)* illustrate two cases of overlap. Here, the BITBLT rectangles are three pixels wide by five scan lines high; they overlap by a single pixel in *(a)* and a single column of pixels in *(b)*. For purposes of illustration, the BITBLT is assumed to be carried out pixel-by-pixel. This convention does not affect the conclusions.

In *Figure 2(a)*, if the BITBLT is performed in the UP direction (bottom-to-top) one of the transfers of the bottom scan line of the source will write to the circled pixel of the destination. Due to the overlap, this pixel is also part of the uppermost scan line of the source rectangle. Thus, data needed later is destroyed. Therefore, this BITBLT must be performed in the DOWN direction. Another example of this occurs any time the screen is moved in a purely vertical direction, as in scrolling text. It should be noted that, in both of these cases, the choice of horizontal BITBLT direction may be made arbitrarily.

Figure 2(b) demonstrates a case in which the horizontal BITBLT direction may not be chosen arbitrarily. This is an



(a) TL/F/8672–4



(b) TL/F/8672–5

FIGURE 2. Overlapping BITBLT Operations

BITBLT Fundamentals (Continued)

instance of purely horizontal movement of data (panning). Because the movement from source to destination involves data within the same scan line, the incorrect direction of movement will overwrite data which will be needed later. In this example, the correct direction is from right to left.

BITBLT VARIATIONS

Some implementations of BITBLT are defined in terms of three operands: source, destination and mask/texture. This third operand is commonly used in monochrome systems to incorporate a stipple pattern into an area. These stipple patterns provide the appearance of multiple shades of gray in single-bit-per-pixel systems, in a manner similar to the 'halftone' process used in printing.

Destination ← Texture op1 Source op2 Destination

While the BPU is essentially a two-operand device, three-operand BITBLT can be implemented quite flexibly and efficiently by performing the two operations serially. The BPU permits the use of any of its sixteen operations for each of the two operators shown above as 'op1' and 'op2'. Additionally, the on-chip FIFO can be used to store the intermediate result (the result of op1 later used as an operand of op2) thus minimizing the number of memory accesses required.

ENHANCING BITBLT PERFORMANCE

There are various ways to enhance BITBLT performance (speed). The simplest way is to try to get data in and out of the memory system quickly. Most of the bitmapped graphics systems utilize DRAMs for both cost and storage density reasons. Since the BITBLT data shows strong locality, the graphics system can take advantage of certain fast memory access modes available to the DRAMs, such as page mode access, static column access, etc. The BPU, by means of an internal FIFO, can pipe the BITBLT source data to reduce the frequency of switching out of the current page address space, thus maximizing the ability of the system to capitalize on the data's locality. This operation is described in the following section.

PIPING THE BITBLT SOURCE DATA

When the BITBLT width is more than a word, up to 16 source data words can be piped into the BPU's on-chip FIFO. At the end of each BITBLT scan line or at the end of 16 source data words, the controller switches from the BITBLT source address space to the BITBLT destination address space. When the BITBLT destination data word is fetched, two possible memory control sequences can be used. One is the modify-write sequence: write the BITBLT result back to the destination memory immediately after the logical function is executed. The second sequence involves storing the BITBLT result back to the BPU's on-chip FIFO, to a maximum of 16 words. Either at the end of each BITBLT destination scan line or at the 16th destination data word, the BITBLT resultant data is then read out from the FIFO and written to the BITBLT destination memory sequentially.

Summary of the BITBLT Memory Control Sequences

BITBLT MEMORY SEQUENCE I

0) Load the BPU Control Register with [FS, SN, LM, RM], via the data bus.
1) Read in the BITBLT source data up to 16 words (17 words in certain cases), barrel-shift, then write them into the on-chip FIFO. (Only 16 barrel-shifted data words can be stored.)
2) Read in the BITBLT destination data while the barrel-shifted source data is read out from the on-chip FIFO and the selected logical operation is executed, then write back to destination.
3) Go to step 1 until the end of the BITBLT scan line.
4) Go to step 1 for the remaining BITBLT scan lines.

BITBLT MEMORY SEQUENCE II

0) Load the BPU Control Register with [FS, SN, LM, RM] via the data bus.
1) Read in the BITBLT source data up to 16 words (17 words in certain cases), barrel-shift, then write them into the on-chip FIFO. (Only 16 barrel-shifted data words can be stored.)
2) Read in the BITBLT destination data in sequence, execute the selected logical operation and then write the result back to the on-chip FIFO, maximum 16 BITBLT data words.
3) Read BITBLT result from the FIFO and write them back to the BITBLT destination memory.
4) Go to step 1 until the end of the BITBLT scan line.
5) Go to step 1 for the remaining BITBLT scan lines.

Block Diagram Description

GENERAL

Figure 3 illustrates the block diagram of the BPU. It consists of several 16-bit latches and multiplexers connected via 16-bit data paths to the three major functional blocks: the Barrel Shifter, the FIFO and the BITBLT Logic Unit. Latches are provided for input data from the BITBLT source and destination as well as for control parameters.

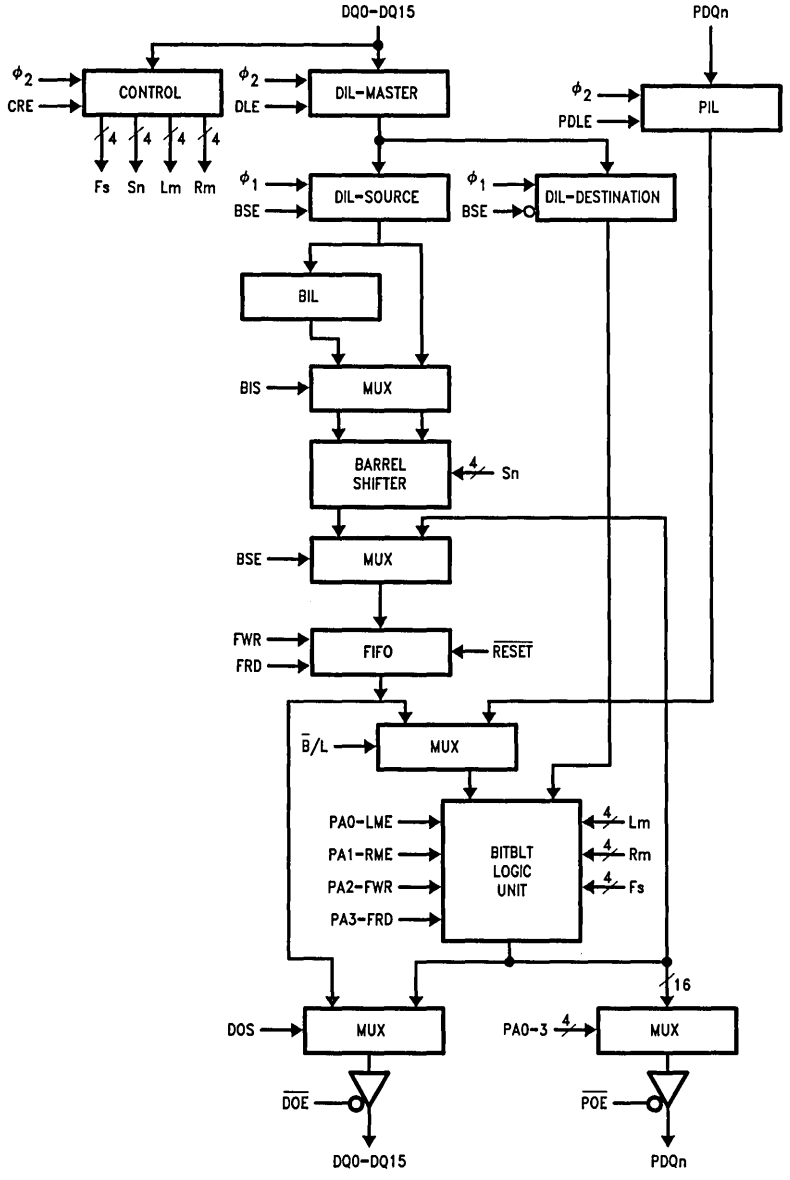
Control parameters consist of 16-bit data which are written to the Control Register. This data is used, in conjunction with the BPU's external control pins, to route and modify the BITBLT data.

The primary flow of data during a BITBLT is from the DQ0–DQ15 pins, through the Master Data Input Latch (DIL-Master) to either the source path or destination path to the BITBLT Logic Unit. The output of the logic unit is then routed through tri-state buffers back to the DQ0–DQ15 pins.

The source path consists of the Source Data Input Latch (DIL-Source), the Barrel Input Latch (BIL), the Barrel Shifter and the FIFO. The destination path consists of only the Destination Data Input Latch (DIL-Destination). The destination path terminates directly at one input port to the logic unit. The logic unit's other input port receives either the output of the FIFO or the output of the Pixel port data Input Latch (PIL), as determined by the state of the $\overline{B}$/L pin, for BITBLTs and line drawing, respectively.

The output of the logic unit is routed through multiplexers to the output drivers for both DQ0–DQ15 and PDQn. In the case of DQ0–DQ15, the multiplexer permits the FIFO output, rather than the logic unit output, to be routed to the output drivers. The PDQn port, being a single bit port, is driven by one of the sixteen output bits of the logic unit, as selected by the multiplexer, according to the state of the pixel address lines, PA0–PA3.

Block Diagram Description (Continued)



TL/F/8672-6

FIGURE 3. DP8510 BPU Detailed Block Diagram

Functional Block Description

BPU CONTROL REGISTER

The BPU Control Register consists of 4 fields, each field being four bits wide. The BITBLT Function Select field, FS, selects one of the 16 BITBLT operations. The barrel Shift Number field, SN, controls the number of bit positions shifted by the barrel shifter. The Left Mask field, LM, sets the BITBLT left mask pattern. The Right Mask field, RM, sets the BITBLT right mask pattern.

The SN will be explained in the barrel shifter section. The LM and the RM will be detailed in the BITBLT logic block section.

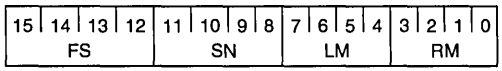


FIGURE 4. Control Register Fields

The content of this register must be loaded prior to the first BITBLT operation by asserting CRE (Control Register Enable). Only the Function Select, FS, is valid when the BPU is in the line-drawing mode. The SN, RM and LM have no effect in the line-drawing mode.

FUNCTION SELECT

The 16 classical BITBLT functions supported by the BPU are described in Table I.

SHIFT NUMBER

There are 16 different barrel shift positions controlled by the SN of the Control Register.

Let A=a15 . . .a0, B=b15 . . .b0 and C=c15 . . .c0, A and B are the input words, C is the output. An i-bit barrel-shift operation on A and B denoted by C=S(i;A,B) is the operation of concatenating the most significant (i) bits of word B to the least significant (16-i) bits of word A.

When A = B, the C=S(i;A, B) is equivalent to having i-bit circular left shift. The i-bit circular right shift is equivalent to the (16-i) bit circular left shift.

The truth table of the barrel-shift operation S(i;A, B) is shown in Table II. (i = shift number)

LEFT AND RIGHT MASKS

The Truth Table for the left and right mask is shown in Table III. Zeroes in the mask patterns indicate bits in the destination data which will be preserved during the BITBLT operation.

Both the LM and the RM can be invoked simultaneously. This may be necessary where the BITBLT width is less than 16 pixels.

TABLE I. BITBLT Function Definitions

#	f3	f2	f1	f0	
0	0	0	0	0	0
1	0	0	0	1	-s AND -d
2	0	0	1	0	-s AND d
3	0	0	1	1	-s
4	0	1	0	0	s AND -d
5	0	1	0	1	-d
6	0	1	1	0	s XOR d
7	0	1	1	1	-s OR -d
8	1	0	0	0	s AND d
9	1	0	0	1	s XNOR d
10	1	0	1	0	d
11	1	0	1	1	-s OR d
12	1	1	0	0	s
13	1	1	0	1	s OR -d
14	1	1	1	0	s OR d
15	1	1	1	1	1

Note: d: destination
s: source
f3–0: function select code, which selects one of the 16 BITBLT functions.

TABLE II. Truth Table for Barrel-Shift Operation S(i;A, B)

i	c15	c14	c13	c12	c11	c10	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
0	a15	a14	a13	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0
1	a14	a13	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0	b15
2	a13	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0	b15	b14
3	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0	b15	b14	b13
4	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a1	b15	b14	b13	b12
5	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0	b15	b14	b13	b12	b11
6	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0	b15	b14	b13	b12	b11	b10
7	a8	a7	a6	a5	a4	a3	a2	a1	a0	b15	b14	b13	b12	b11	b10	b9
8	a7	a6	a5	a4	a3	a2	a1	a0	b15	b14	b13	b12	b11	b10	b9	b8
9	a6	a5	a4	a3	a2	a1	a0	b15	b14	b13	b12	b11	b10	b9	b8	b7
10	a5	a4	a3	a2	a1	a0	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6
11	a4	a3	a2	a1	a0	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5
12	a3	a2	a1	a0	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4
13	a2	a1	a0	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3
14	a1	a0	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2
15	a0	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1

Functional Block Description (Continued)

TABLE III. Truth Table for Left and Right Mask

LM = 0,	L—mask =	1111	1111	1111	1111
LM = 1,	L—mask =	0111	1111	1111	1111
LM = 2,	L—mask =	0011	1111	1111	1111
LM = 3,	L—mask =	0001	1111	1111	1111
LM = 4,	L—mask =	0000	1111	1111	1111
LM = 5,	L—mask =	0000	0111	1111	1111
LM = 6,	L—mask =	0000	0011	1111	1111
LM = 7,	L—mask =	0000	0001	1111	1111
LM = 8,	L—mask =	0000	0000	1111	1111
LM = 9,	L—mask =	0000	0000	0111	1111
LM = 10,	L—mask =	0000	0000	0011	1111
LM = 11,	L—mask =	0000	0000	0001	1111
LM = 12,	L—mask =	0000	0000	0000	1111
LM = 13,	L—mask =	0000	0000	0000	0111
LM = 14,	L—mask =	0000	0000	0000	0011
LM = 15,	L—mask =	0000	0000	0000	0001
RM = 0,	R—mask =	1000	0000	0000	0000
RM = 1,	R—mask =	1100	0000	0000	0000
RM = 2,	R—mask =	1110	0000	0000	0000
RM = 3,	R—mask =	1111	0000	0000	0000
RM = 4,	R—mask =	1111	1000	0000	0000
RM = 5,	R—mask =	1111	1100	0000	0000
RM = 6,	R—mask =	1111	1110	0000	0000
RM = 7,	R—mask =	1111	1111	0000	0000
RM = 8,	R—mask =	1111	1111	1000	0000
RM = 9,	R—mask =	1111	1111	1100	0000
RM = 10,	R—mask =	1111	1111	1110	0000
RM = 11,	R—mask =	1111	1111	1111	0000
RM = 12,	R—mask =	1111	1111	1111	1000
RM = 13,	R—mask =	1111	1111	1111	1100
RM = 14,	R—mask =	1111	1111	1111	1110
RM = 15,	R—mask =	1111	1111	1111	1111

BARREL-SHIFTER

The function of the barrel shifter is to align the BITBLT source data to the destination data. Bit alignment may cross word boundaries.

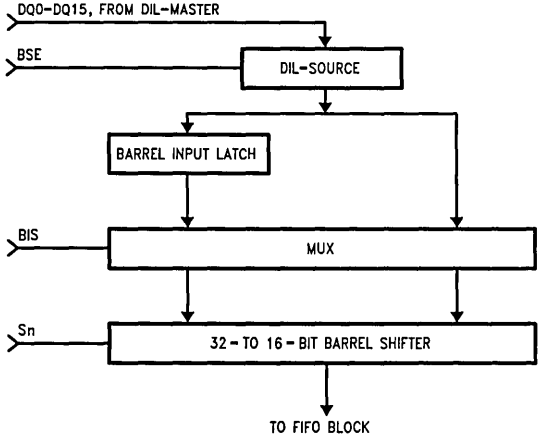
The barrel shifter in the BPU is implemented as a 32- to 16-bit multiplexer. Depending upon the type of the BITBLT and the BITBLT length, the necessary source data word(s) are fetched into the BPU forming a 32-bit input to the barrel shifter. Barrel Input Latch (BIL) stores the first source data word fetched and the Source Data Input Latch (DIL-source) stores the subsequent source data word.

A multiplexer precedes the barrel shifter to swap the input words if necessary. That is, Barrel Input Select (BIS) causes BIL (and DIL-Source) to be routed to the left or right (and right or left) half of the barrel shifter. Note that this is a word-level swap; it does not affect the ordering of the bits within the words. This swap mechanism facilitates the fetching of BITBLT data from left-to-right or right-to-left.

When the BITBLT direction is set from the left to the right (the source data words are fetched starting from the left-hand side of the BITBLT rectangle), the BIS pin should be set low. If the BITBLT direction is set from the right to the left, BIS must be set high to exchange the source data sequence.

Figure 5 depicts the data path in the BPU's barrel-shifter block.

The Barrel Input Latch (BIL) is the BITBLT source data pipeline register. It is loaded (from DIL-Source) one clock cycle after DIL-Source is loaded. Therefore, when the system fetches a BITBILT source word from memory (BSE asserted), this word will be first loaded into DIL-Source on the rising edge of a PH1; it will then be transferred to BIL on the rising edge of the following PH1. As a result, if the two words have been fetched in temporal sequence, the first word fetched will be in BIL; the second word will be in DIL-Source. It should be noted that this condition (different words in BIL and DIL-Source) will be true for only one clock period, since the next rising edge of PH1 will again cause BIL to be loaded from DIL-Source. Therefore, the shifted result (the output of the barrel shifter) must be written to the FIFO on the rising edge of PH1 immediately following the PH1 used to load DIL-Source.



TL/F/8672–7

FIGURE 5. BPU Barrel-Shifter Block

Functional Block Description (Continued)

Source Data Multiplexing, an Example:

Figure 6 shows an example of the BPU Barrel Shifter operation. Let Word A = aF..a0, Word B = bF..b0, SN = S3..S0 and BSE = 1. In both cases below, Word B is fetched **after** Word A.

FIFO

The FIFO, 16 bits by 16 words, constitutes the BPU's on-chip storage and is implemented with dual-port RAM. The FIFO has separate READ/WRITE controls, the FIFO Write (FWR) and the FIFO Read (FRD). The use of faster, localized memory access modes (e.g., page, static column) is supported by the BPU via the FIFO, since the FIFO provides storage for multiple, barrel-shifted source words.

Figure 7 depicts the BPU FIFO structure.

Case I. If BIS = 0,

```
Word A                              B
     F E D C B A 9 8 7 6 5 4 3 2 1 0 F E D C B A 9 8 7 6 5 4 3 2 1 0
SN
0   aFaEaDaCaBaAa9a8a7a6a5a4a3a2ala0
1     aEaDaCaBaAa9a8a7a6a5a4a3a2ala0bF
2       aDaCaBaAa9a8a7a6a5a4a3a2ala0bFbE
3         aCaBaAa9a8a7a6a5a4a3a2ala0bFbEbD
4           aBaAa9a8a7a6a5a4a3a2ala0bFbEbDbC
5             aAa9a8a7a6a5a4a3a2ala0bFbEbDbCbB
6               a9a8a7a6a5a4a3a2ala0bFbEbDbCbBbA
7                 a8a7a6a5a4a3a2ala0bFbEbDbCbBbAb9
8                   a7a6a5a4a3a2ala0bFbEbDbCbBbAb9b8
9                     a6a5a4a3a2ala0bFbEbDbCbBbAb9b8b7
A                       a5a4a3a2ala0bFbEbDbCbBbAb9b8b7b6
B                         a4a3a2ala0bFbEbDbCbBbAb9b8b7b6b5
C                           a3a2ala0bFbEbDbCbBbAb9b8b7b6b5b4
D                             a2ala0bFbEbDbCbBbAb9b8b7b6b5b4b3
E                               ala0bFbEbDbCbBbAb9b8b7b6b5b4b3b2
F                                 a0bFbEbDbCbBbAb9b8b7b6b5b4b3b2b1
```

Case II. If BIS = 1 (The BIS controls the multiplexing before the barrel shifter),

```
Word B                              A
     F E D C B A 9 8 7 6 5 4 3 2 1 0 F E D C B A 9 8 7 6 5 4 3 2 1 0
SN
0   bFbEbDbCbBbAb9b8b7b6b5b4b3b2blb0
1     bEbDbCbBbAb9b8b7b6b5b4b3b2blb0aF
2       bDbCbBbAb9b8b7b6b5b4b3b2blb0aFaE
3         bCbBbAb9b8b7b6b5b4b3b2blb0aFaEaD
4           bBbAb9b8b7b6b5b4b3b2blb0aFaEaDaC
5             bAb9b8b7b6b5b4b3b2blb0aFaEaDaCaB
6               b9b8b7b6b5b4b3b2blb0aFaEaDaCaBaA
7                 b8b7b6b5b4b3b2blb0aFaEaDaCaBaAa9
8                   b7b6b5b4b3b2blb0aFaEaDaCaBaAa9a8
9                     b6b5b4b3b2blb0aFaEaDaCaBaAa9a8a7
A                       b5b4b3b2blb0aFaEaDaCaBaAa9a8a7a6
B                         b4b3b2blb0aFaEaDaCaBaAa9a8a7a6a5
C                           b3b2blb0aFaEaDaCaBaAa9a8a7a6a5a4
D                             b2blb0aFaEaDaCaBaAa9a8a7a6a5a4a3
E                               blb0aFaEaDaCaBaAa9a8a7a6a5a4a3a2
F                                 b0aFaEaDaCaBaAa9a8a7a6a5a4a3a2al
```

FIGURE 6

Functional Block Description (Continued)

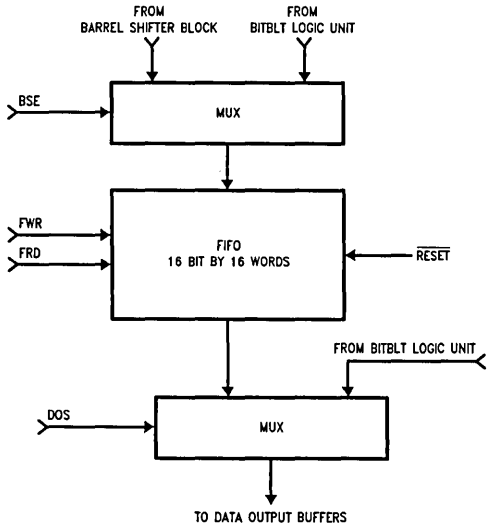


FIGURE 7. BPU FIFO Block

BITBLT LOGIC CONTROL UNIT

This block performs the selected BITBLT logical operation and the BITBLT destination data masking.

The 16 BITBLT functions can be expressed as:

```
f3 * (  s *  d ) +
f2 * (  s * -d ) +
f1 * ( -s *  d ) +
f0 * ( -s * -d )
```

where f0–f3 are the bits of the Function Select field, FS.

LINE DRAWING MODE ($\overline{B}$/L = 1)

Line drawing mode differs from BITBLT mode in the following respects:

1) the FIFO is not used in line drawing mode.
2) the Shift Number parameter is ignored in the line drawing mode
3) the Left Mask and Right Mask parameters are ignored in the line drawing mode. Instead, masks are generated in matched pairs, as needed, according to the current state of the Pixel Address lines PA0–PA3.

   For example, if the pixel address (the binary value on PA0–3) is 12 decimal (PA3 = PA2 = 1, PA1 = PA0 = 0), then the following masks will be generated:

```
          MS bit                LS bit
            ↓                     ↓
          LM = 0000 0000 0000 1111
and       RM = 1111 1111 1111 1000
```

   Since these masks are used simultaneously when the destination word is generated (during line drawing mode), and since zeroes in the mask indicate destination bits that are unaffected (are preserved) by the BITBLT operation, the AND of the two masks indicates the bit that will be affected by the BITBLT. In this example, bit 3 of the memory word is selected.

   It is important to note this mapping convention of the BPU: the logical pixel (indicated by PA0–3) associated with the current line drawing BITBLT operation corresponds to a physical bit (indicated by the ones-complement of PA0–3) in the current memory word. That is, logical pixel 0 corresponds to DQ15 in any word. Logical pixel 1 corresponds to DQ14 in any word, etc.
4) Conceptually, during line drawing, there is no "source", in the conventional BITBLT sense of replicating an item from one set of storage locations to another set of storage locations. Rather, the line is "created" bit-by-bit by an address-generating algorithm. However, a mechanism is provided in the BPU to establish a single bit which can be logically combined (in the BITBLT Logic Unit) with each bit of the destination. This mechanism is embodied in the pixel data port and its associated input latch (PIL).
5) the PIL bit is replicated into all 16 bits of the logic unit's source input port in line drawing mode.
6) a single bit of the logic unit's output port is selected to drive the PDQn output buffer, according to PA0–PA3, in line drawing mode. In BITBLT mode, this multiplexer is at TRI-STATE.

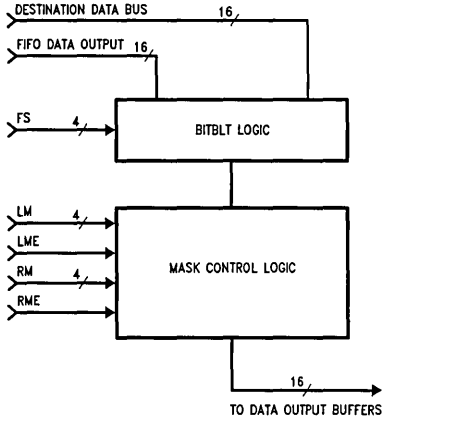


FIGURE 8. BPU Logical Control Unit

Applications of the DP8510 BPU

SYSTEM CONTROL SEQUENCE

Figure 9 illustrates a typical control and memory access sequence that might be used to accomplish BITBLT with the BPU. In this example, memory access time is sufficiently fast to avoid wait states (the BPU is capable of accepting a new operand at each clock). All control strobes are assumed to be generated by the CPU/state machine which is serving as the BPU's controller.

In this example, a single operation is performed per clock cycle for the sake of clarity. Overlap of memory access with internal BPU operations would reduce the number of clock cycles.

Clock	Action
1	address for source operand 1 is generated, first RAM access is started, data becomes valid at end of cycle
2	source operand 1 is latched in data input latch, address for source operand 2 is generated, second RAM access is started, data becomes valid at end of cycle
3	source operand 2 is latched in data input latch (forming the 32-bit input to the barrel shifter), data propagates through the barrel shift logic and becomes valid at the input to the FIFO
4	the barrel-shifted source word is written to the FIFO, the BPU's source path is disabled, the BPU's destination path is enabled
5	the address for the destination word is generated, the destination RAM access is started, data becomes valid at end of cycle
6	destination data is latched into data input latch, source word is read from internal FIFO, BITBLT logic unit produces resultant word
7	output buffers are enabled destination write to RAM occurs.

FIFO STRUCTURE, OPERATION AND RESTRICTIONS

The DP8510 BPU's FIFO is implemented as a file of sixteen 16-bit registers. The file has separate ports for read and write operations. Register selection is accomplished via a pair of shift-register ring counters. One of these is used during FIFO write cycles and is incremented by FIFO Write (FWR); the other is used during FIFO read cycles and is incremented by FIFO Read (FRD). At RESET, both ring counters are set to enable FIFO register 0. Both ring counters will wrap around; that is, they will select the FIFO registers in the sequence:

$$0, 1, 2, \ldots, 13, 14, 15, 0, 1, \ldots$$

During a FIFO write cycle, the FIFO register currently selected by the WRITE ring counter will be written with the appropriate internally-sourced data (barrel shifter output or logic unit output, according to the state of BSE); the WRITE ring counter will then be incremented to select the next FIFO register.

The FIFO read operation is implemented in a read-ahead manner as follows: the contents of the FIFO register selected by the FIFO READ ring counter is copied to a master latch (of a master-slave pair) during each PH2 regardless of the state of FRD; however, the contents of this latch are not passed on to the slave (output) latch until the next PH1 when FRD is active. This FRD also causes the FIFO READ ring counter to be incremented to the next FIFO register, initiating the read-ahead of that register in anticipation of the next FIFO read cycle.

In general, a given clock cycle can accomplish a simultaneous FIFO read and FIFO write. However, two restrictions apply to FIFO operations. First, a simultaneous FIFO read and FIFO write should apply to *different* FIFO registers; that is; the SAME register should NOT be read and written in the same cycle. Failure to meet this requirement is not destructive, but the result may be contrary to what the user indends: the output value will be the "old" contents of the currently-selected FIFO register, not the "new" value being written to that register. This behavior is a result of the read-ahead operation in conjunction with the two-phase master-slave output latch.

The second restriction is a speed-dependent one; it does not apply at clock frequencies of 10 MHz and below. At higher clock speeds, a two clock-cycle minimum is imposed between the FIFO write to a given location and the corresponding FIFO read of that location. Failure to meet this restriction may result in incorrect data being read from the FIFO. Consider the case of the FIFO at RESET: if the first FIFO write is performed during clock cycle (m), the first FIFO read (which is the read of that location) may not take place until clock cycle (m+2). An equivalent "FIFO-initially-empty" case occurs whenever the (n)th FIFO location is written and the (n−1)th FIFO location is read during the same clock cycle. This restriction does not impair the ability of the BPU to perform consecutive FIFO reads and/or FIFO writes at one-clock intervals.

BPU USED WITH A CPU OR STATE MACHINE

The BPU places no restrictions on the practical number of planes in a system; rather, systems can be expanded from one to any number of planes without compromising BITBLT performance. Data movement within each plane is carried out in parallel by a dedicated BPU for each plane; as a result, a BITBLT can be performed for any number of planes in the same period of time as in a single-plane monochrome system.

Systems currently implementing BITBLT completely in software can realize a major performance increase through the use of the BPU. In this case, the BPU can be thought of as a hardware accelerator for BITBLT. Two examples of the BPU in this application are shown in *Figures 10* and *11*. In both examples, the CPU is responsible for BITBLT preprocessing, such as the determination of direction, initial BITBLT addresses, etc. These examples illustrate the variety of cost/complexity versus performance tradeoffs that may be made. While *Figures 10* and *11* illustrate a single plane application, extension to multiple planes can be achieved by implementing a BPU on each bitplane which will result in virtually the same performance while delivering a greater number of shades or colors.

Applications of the DP8510 BPU (Continued)

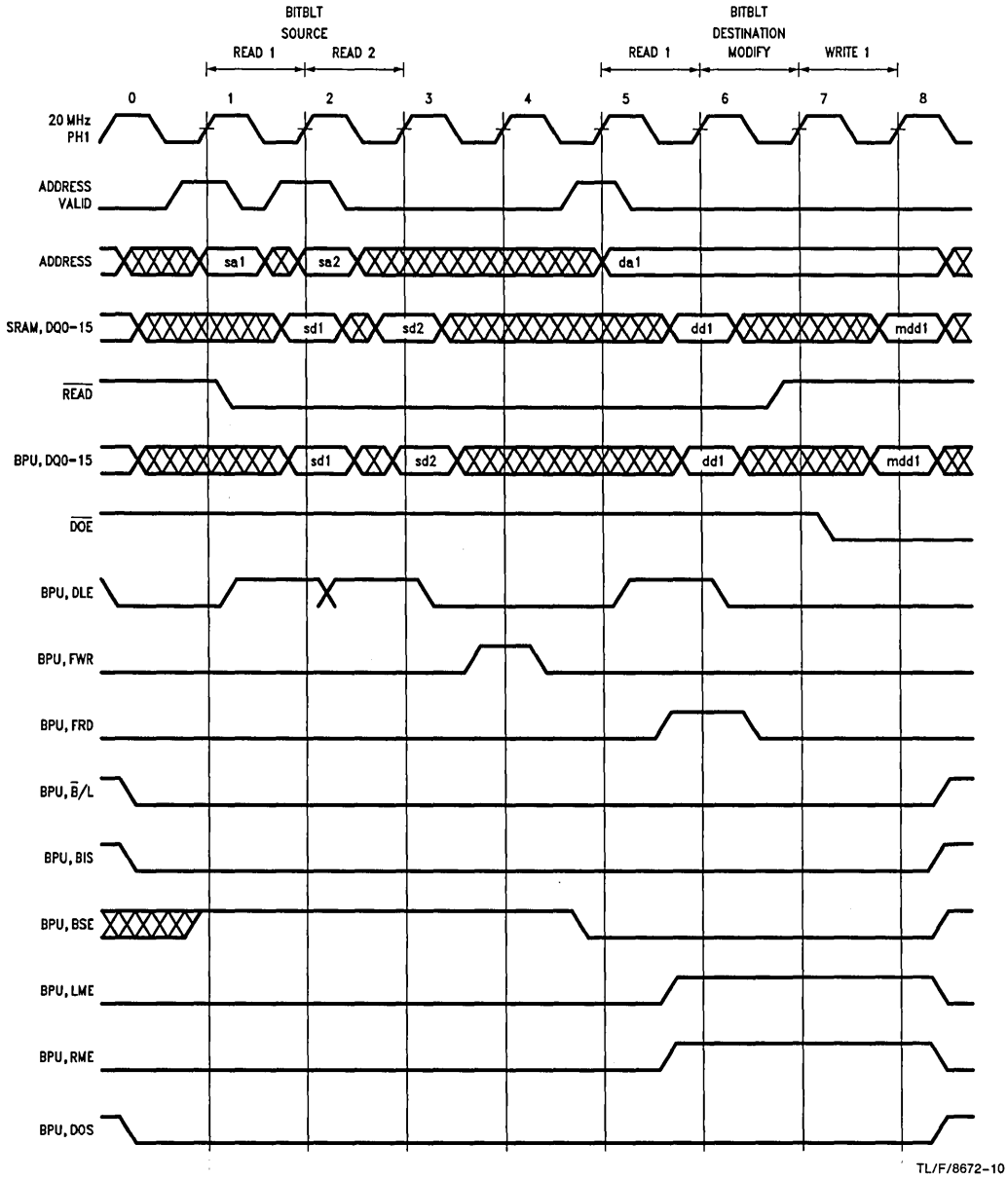
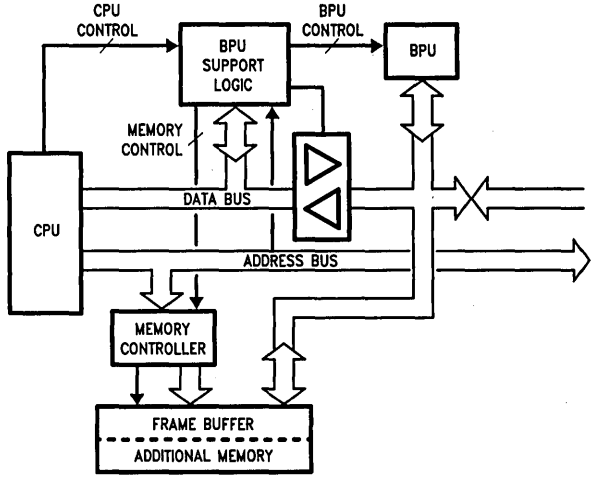


FIGURE 9. Typical BITBLT Timing (Using Fast Static RAM)

Applications of the DP8510 BPU (Continued)

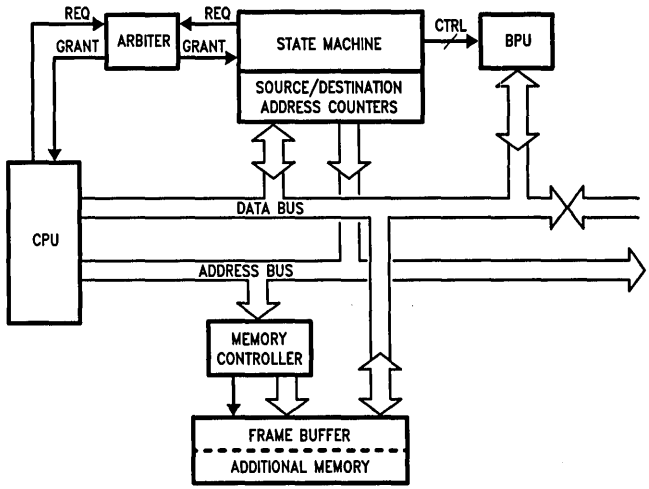


TL/F/8672–12

FIGURE 10. BPU with CPU using String/Block Move Instructions

Figure 10 presents a solution requiring minimal hardware but whose performance may be limited by the CPU's bus cycle time. In this example, the CPU's block move or string move instruction is used to produce the source and destination addresses for the BITBLT. The BPU, in conjunction with its support logic, intercepts the source data during the read cycle. The support logic is also responsible for turning the string/block instruction's write cycles into read-modify-writes to allow the BPU to receive the destination data, logically combine it with the source data, and return it to the destination address. The result is a relatively simple hardware/software implementation of a single scan line of the BITBLT.

Performance can be further enhanced, at the cost of greater hardware complexity, through an implementation as described in *Figure 11*. As in the previous example, this solution performs a single scan line of the BITBLT; however, in this case, the BITBLT proceeds without any involvement on the CPU's part. All intermediate addresses within the scan line are generated by up-down counters; all bus cycles are effected by the state machine's hardware. Within this scheme, further tradeoffs may be made. For example, the designer has the option of using the BPU's source pipeline to take advantage of faster memory access modes, such as page mode.



TL/F/8672–13

FIGURE 11. BPU with CPU and state machine

Absolute Maximum Ratings*

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature under bias	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
All input or output voltage with respect to GND	−0.5V to +7V
Power Dissipation @ 20 MHz	0.5W

ESD rating is to be determined.

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.*

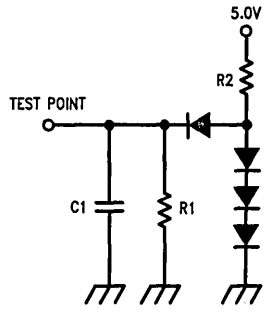
*Note: These are preliminary specifications

DC Electrical Characteristics* $T_A = 0°$ to $70°$, $V_{CC} = 5V \pm 10\%$, GND = 0V

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
V_{IH}			2.0		V_{CC} + 0.5	V
V_{IL}			−0.5		0.8	V
V_{CH}	MOS Clock High	PH1, PH2 Pins Only, MOS	V_{CC} − 0.5		V_{CC} + 0.5	V
V_{CL}	MOS Clock Low	PH1, PH2 Pins Only, MOS	−0.5		0.3	V
V_{CLT}	MOS Clock Ringing	PH1, PH2 Pins Only, MOS	−0.5		0.5	V
V_{TCH}	TTL Clock High	TTL Clock/PH1 Pin Only	2.5			V
V_{TCL}	TTL Clock Low	TTL Clock/PH1 Pin Only			0.8	V
V_{OH}		I_{OH} = −3 mA	2.4			V
V_{OL}		I_{OL} = 3 mA			0.5	V
I_{IN}	Leakage Current	$V_{IN} = V_{IH}$ or V_{IL}			±10	μA
I_{OZ}	TRI-STATE® Leakage	$V_O = V_{CC}$ or GND			±10	μA
I_{CC1}	Quiescent Current	PH1, PH2 at 20 MHz		3		mA
I_{CC2}	Supply Current	PH1, PH2 at 100 kHz		10		mA
I_{CC3}	Supply Current	PH1, PH2 at 20 MHz		20		mA
C_{IN}	Input Capacitance	f_{in} at 1 MHz			10	pF

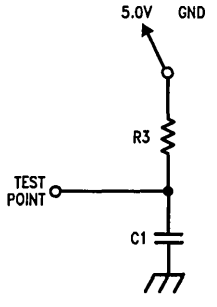
Note: All output test conditions are 50 pF plus one TTL load.

*These are preliminary specifications



TL/F/8672–14

FIGURE 12. BPU Output Test Load Circuitry



TL/F/8672–15

FIGURE 13. BPU Output TRI-STATE Test Load Circuitry

Note 1: C1 = 50 pF
R1 = 6 kΩ
R2 = 1.3 kΩ
R3 = 1.8 kΩ

Note 2: Connect SW to +5V for tpLZ and tpZL measurements.

Note 3: Connect SW to GND for tpHZ and tpZH measurements.

AC Electrical Characteristics

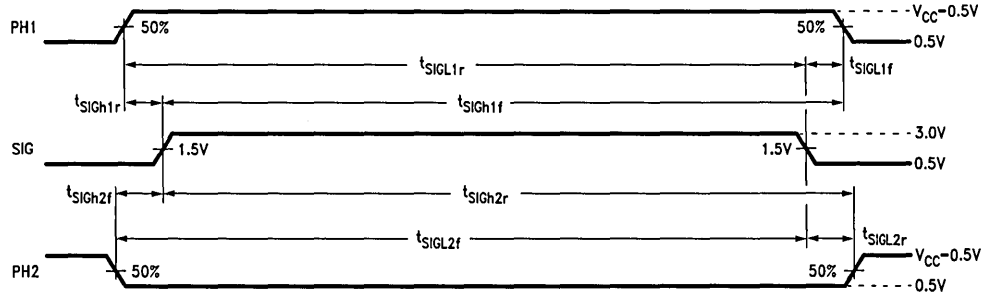
Symbol	Min	Typ	Max	Unit	Description
f			20	MHz	PH1, PH2 Frequency
tpn1a	16			ns	PH1 High Time (90% to 90%)
tpn2a	16			ns	PH2 High Time (90% to 90%)
tpn1b	19			ns	PH1 High Time (50% to 50%)
tpn2b	19			ns	PH2 High Time (50% to 50%)
tck1	25			ns	50% PH1 Rising to 50% PH2 Rising
tck2	22			ns	50% PH2 Rising to 50% PH1 Rising
tnov1	3			ns	PH2-to-PH1 50% Non-Overlap Time
tnov2	3			ns	PH1-to-PH2 50% Non-Overlap Time
tles1	15			ns	DLE, PDLE, CRE to PH2 Setup Time (TCS = 0)
tles2	25			ns	DLE, PDLE, CRE to PH1 Setup Time (TCS = 1)
tleh1	10			ns	DLE, PDLE, CRE to PH2 Hold Time (TCS = 0)
tleh2	20			ns	DLE, PDLE, CRE to PH1 Hold Time (TCS = 1)
tleis	15			ns	DLE, PDLE, CRE to PH2 Invalid Switching Time
tds2f1	15			ns	Data to PH2 Setup Time (TCS = 0)
tds1r	25			ns	Data to PH1 Setup Time (TCS = 1)
tdh2f1	10			ns	Data to PH2 Hold Time (TCS = 0)
tdh1r	20			ns	Data to PH1 Hold Time (TCS = 1)
tdpZH		20		ns	Data TRI-STATE to High Delay Time
tdpZL		20		ns	Data TRI-STATE to Low Delay Time
tdpHZ		20		ns	Data High to TRI-STATE Delay Time
tdpLZ		20		ns	Data Low to TRI-STATE Delay Time
tctls2f	25			ns	Control Signals to PH2 Setup Time (TCS = 0)
tctls1r	25			ns	Control Signals to PH1 Setup Time (TCS = 1)
tctlh2f	10			ns	Control Signals to PH2 Hold Time (TCS = 0)
tctlh1r	20			ns	Control Signals to PH1 Hold Time (TCS = 1)
tcl		30		ns	$\overline{B}$/L, DOS to Data Switching Time
tbiss1r	25			ns	BIS Setup to PH1 (TCS = X)
tbish2f	10			ns	BIS Hold to PH2 (TCS = 0)
tbish1r	20			ns	BIS Hold to PH1 (TCS = 1)
tbses1r	25			ns	BSE Setup to PH1 (TCS = X)
tbseh2f	10			ns	BSE Hold to PH2 (TCS = 0)
tbseh1r	20			ns	BSE Hold to PH1 (TCS = 1)
tpdn1r		50		ns	PH1 to Valid Pixel Data
tdq1r		25		ns	PH1 to Valid Output Data (DOS=0)
tdq1r		15		ns	PH1 to Valid Output Data (DOS=1)

*These are preliminary specifications.

Timing Diagrams

DEFINITIONS

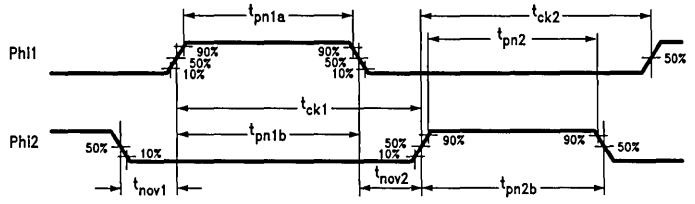
All the timing specifications given in this section refer to 50% of the leading or trailing edges of the appropriate clock phase and 0.5V or 3.0V on the appropriate signal as illustrated in the following figures, unless specifically stated otherwise.



TL/F/8672-16

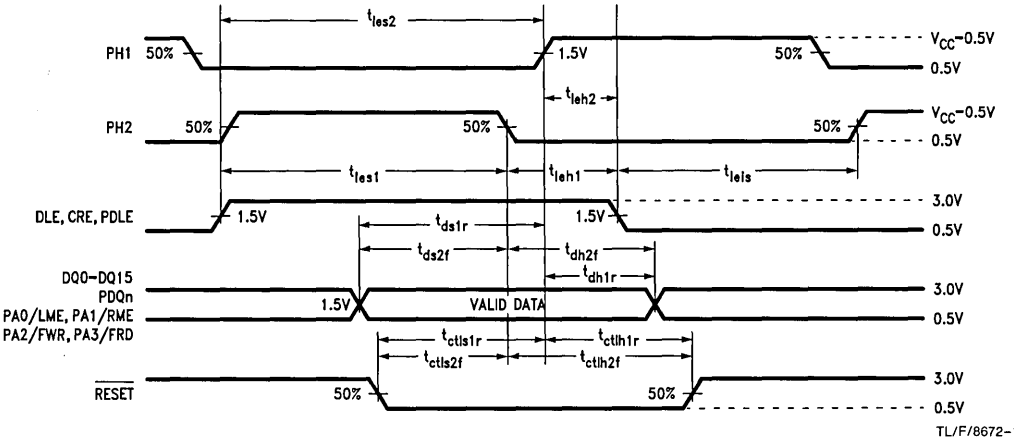
Note: Data is measured at 1.5V to 50% points of PH1 and PH2.

FIGURE 14. Timing Specification Standard



TL/F/8672-17

FIGURE 15. Two-Phase MOS Clock Timing Specification



TL/F/8672-18

FIGURE 16. Input Data Timing Specification

Timing Diagrams (Continued)

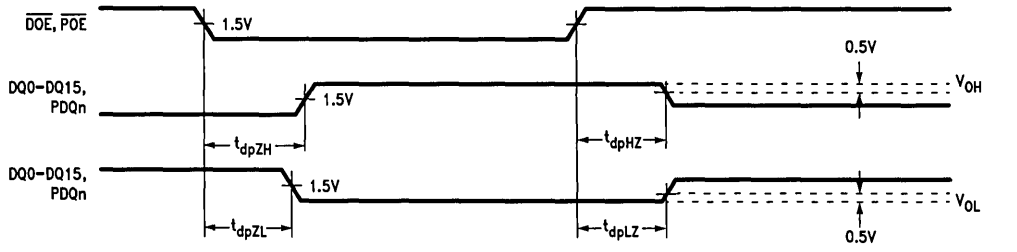


FIGURE 17. Output Enable Timing Specification

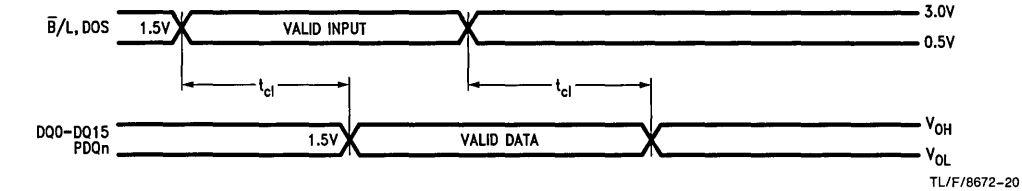


FIGURE 18. Mode Control Timing Specification

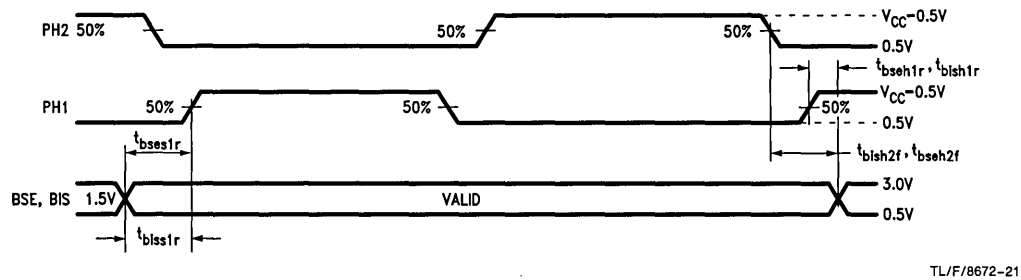
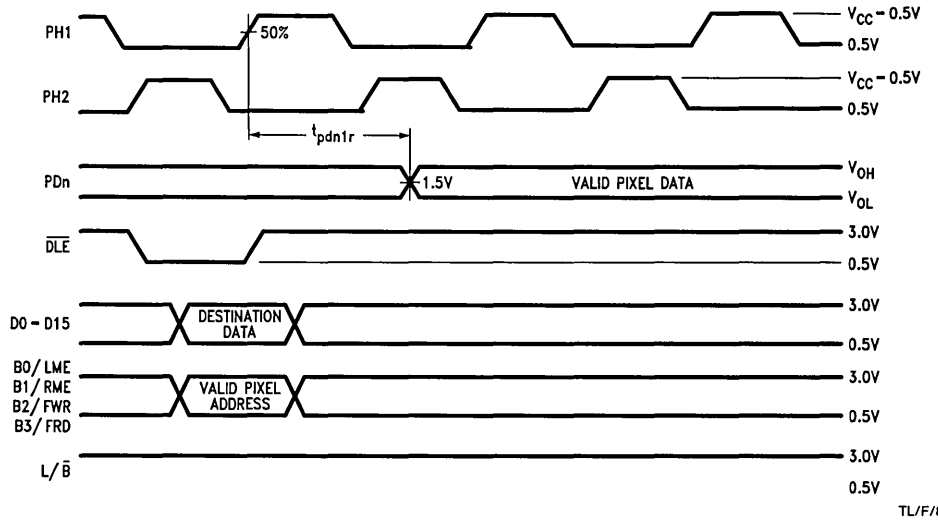


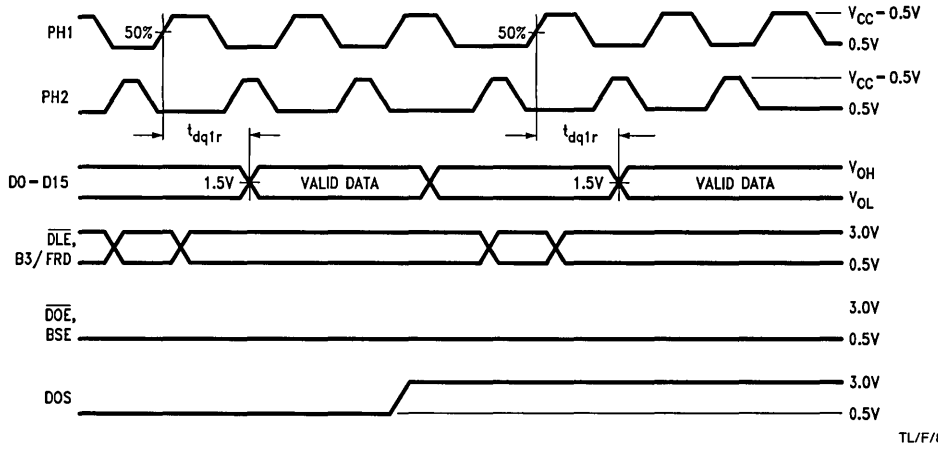
FIGURE 19. Control Signal Timing Specification

Timing Diagrams (Continued)



TL/F/8672-23

FIGURE 20. Pixel Read Timing Specification



TL/F/8672-24

FIGURE 21. FIFO/DIL-Dest Data Read Timing Specification

National Semiconductor

PRELIMINARY

DP8511 BITBLT Processing Unit (BPU)

General Description

The DP8511 BITBLT Processing Unit (BPU), a member of National Semiconductor's Advanced Graphics Chip Set (AGCS), is a high performance microCMOS device intended for use in raster graphics applications. Specifically designed to complement the DP8500 Raster Graphics Processor (RGP), the BPU performs data operations that are elementary to BITBLT (BIT boundary Block Transfer) graphics: Shift, mask, and bitwise logical manipulation of memory. Under the control of the RGP, the BPU performs the necessary BITBLT data path operations at pipelined hardware speeds. A simple set of control lines interfaces the BPU to the RGP and to the system memory.

The BPU has two modes of operation: BITBLT and Line Drawing. BITBLT performs shift and logical operations on blocks of 16-bit data words. Line drawing performs similar operations on single-bit pixel data by utilizing a single bit pixel port (PDn). This port allows data read and read-modify-write operations on single pixels across a number of bitplanes, giving access to pixel depth. The BPU provides both pixel level processing commonly used in image processing applications and extremely fast planar operations used most frequently in color graphics.

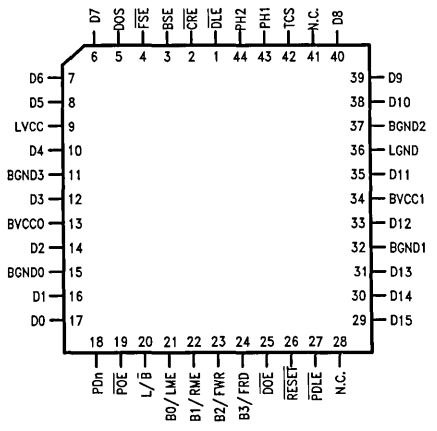
The BPU's operation is controlled by the values loaded to the Control Register (CR) and the Function Select Register (FSR). This dual register configuration of the DP8511 allows for high throughput in multi-plane systems that incorporate a BPU per plane. This performance advantage is achieved by allowing the flexibility of changing the FSR's contents independent of the CR, so that multiple bitplanes can be updated simultaneously while each BPU performs different logical operations on its own destination data.

Features

- Interfaces directly to the DP8500 Raster Graphics Processor
- 20 MHz operation
- Supports all 16 classical BITBLT functions
- Pipelined data input for high system throughput
- Provides performance independent of the number of bitplanes
- Line Drawing support
- Compatible with static, dynamic RAMs, and Video RAMs
- Compatible with page mode, nibble mode and static column RAMs
- 32-bit to 16-bit barrel shifter
- 16-bit data port, single bit pixel port
- 16-word FIFO
- 16-bit logic operations
- Single +5V supply
- All inputs and outputs TTL compatible
- 2 micron microCMOS technology

Connection Diagram

Plastic Chip Carrier



TL/F/9337–1

N.C. = No Connection

Top View

Order Number DP8511V
See NS Package Number V44A

Pin Descriptions

INPUTS

$\overline{DOE}$: Data Output Buffer Enable. When asserted low, this pin enables the output buffers on D0–D15. This input is generally driven by memory control logic.

$\overline{POE}$: Pixel Output Buffer Enable. Enables the Pixel Output Buffer when active (low). This pins allows for reading pixel data from the frame buffer in a multiple bitplane system. This signal is generally provided by the memory control logic.

L/$\overline{B}$: Line Drawing or BITBLT. A high on this input enables the BPU for line drawing mode. A low enables the BITBLT mode. This input is normally driven by the RGP.

B0/LME: Bit Select 0/Left Mask Enable. In the line drawing mode, this pin serves as the least significant pixel address bit. When in the BITBLT mode, this pin is used as the Left Mask Enable input. This input must be synchronized with respect to the falling edge of PH2. This pin is normally driven by the RGP.

B1/RME: Bit Select 1/Right Mask Enable. In the line drawing mode, this pin serves as the second least significant pixel address bit. When in the BITBLT mode, this pin is used as the Right Mask Enable input. This input must be synchronized with respect to the falling edge of PH2. This pin is normally driven by the RGP.

B2/FWR: Bit Select 2/FIFO Write Control. In the line drawing mode, this pin serves as the second most significant pixel address bit. When in the BITBLT mode, this pin is used as the FIFO Write control input. This input must be synchronized with respect to the falling edge of PH2. This pin is normally driven by the RGP.

B3/FRD: Bit Select 3/FIFO Read Control. In the line drawing mode, this pin serves as the most significant pixel address bit. When in the BITBLT mode, this pin is used as the FIFO Read control input. This input must be synchronized with respect to the falling edge of PH2. This pin is normally driven by the RGP.

BSE: BITBLT Source Enable. This pin enables the BITBLT source input data path and controls the latching function of the BITBLT source pipeline register. BSE is sampled and latched on the falling edge of PH2 clock. The level on BSE must be asserted one clock cycle prior to loading data to the Data Input Latch (DIL), and must remain constant during the subsequent data load cycle to ensure data integrity. This input is driven by the RGP.

TCS: TTL Clock Select. This pin is tied to either V_{CC} or GND. A high level on this pin selects the TTL level clock input mode which uses a conventional TTL level clock of up to 10 MHz, simplifying the system design. A low level selects a 2 phase MOS clock mode which uses PH1 and PH2 as clock inputs.

PH1: Phase 1 clock input/TTL clock input. When TCS is low, this input serves as the Phase 1 MOS clock input with a maximum clock rate of 20 MHz. When TCS is high, this input is the TTL clock input with a maximum rate of 10 MHz.

PH2: Phase 2 clock input. This pin is the Phase 2 MOS clock input with a maximum rate of 20 MHz. When using a TTL clock, this input must be tied to ground.

$\overline{CRE}$: BPU Control Register Enable. The data on D0–D15 is latched into the Control Register on the rising edge of $\overline{CRE}$. This input is driven by an address decoder residing in the RGP's address space.

$\overline{DLE}$: Data Latch Enable. A low on this pin enables the BPU's Data Input Latch (DIL). The data on D0–D15 is latched into the DIL on the falling edge of the next PH2 clock. $\overline{DLE}$ must be synchronized with respect to the valid data and must be removed before the rising edge of the subsequent PH2 clock. This input is generally driven by memory control logic.

$\overline{FSE}$: BPU Function Select Register Enable. The data on D0–D15 is latched into the Function Select Register on the rising edge of $\overline{FSE}$. This input generally is driven by an address decoder residing in the RGP's memory space.

$\overline{PDLE}$: Pixel port Data Latch Enable. A low level on this pin enables the BPU's pixel port data input latch. The data on the PDn pin is latched into the one-bit Pixel Input Latch on the falling edge of the next PH2 clock. $\overline{PDLE}$ must be synchronized with respect to the valid pixel data and must be removed before the rising edge of the subsequent PH2 clock.

DOS: Data Output Select: DOS selects the data output from either the FIFO (DOS = 1) or the BITBLT logic unit (DOS = 0). This input should be grounded when the BPU is controlled by an RGP.

$\overline{RESET}$: FIFO control Reset. A low on this pin resets the BPU's FIFO read/write control circuitry. Data previously stored in the FIFO or on-chip latches is unchanged. This input must be synchronized with respect to the falling edge of PH2. PA2/FWR and PA3/FRD inputs must be low 1 clock cycle prior to asserting $\overline{RESET}$. This pin is controlled by the RGP's RSTO line.

INPUTS/OUTPUTS

D0–D15: 16-bit Bidirectional Data Port. This port serves as the input to the Data Input Latch, Control Register, and to the Function Select Register. When $\overline{DOE}$ is active (low), this port serves as a 16-bit output buffer.

PDn: Pixel Data Port, a single bit bidirectional port. This I/O port is used in the line drawing mode (L/$\overline{B}$ = 1). It serves as the input to the Pixel Input Latch, providing a source bit for line drawing. When $\overline{POE}$ is active (low), this port serves as an output for the pixel previously latched in the Pixel Output Latch (POL).

SUPPLIES

LVCC: Positive supply for on-chip logic. 5 V_{DC} ±10%.

LGND: Ground for on-chip logic.

BVCC0–
BVCC1: Positive supply for output buffers, two pins total. 5 V_{DC} ±10%.

BGND0–
BGND3: Ground for output buffers, four pins total.

BITBLT Fundamentals

BITBLT, BIT-aligned Block Transfer, is a general operator that provides a mechanism to move an arbitrary size rectangle of an image from one part of the frame buffer to another. During the data transfer process a bitwise logical operation can be performed between the source and the destination data. BITBLT is also called RasterOp: operations on rasters. It defines two rectangular areas, source and destination, and performs a logical operation (e.g., AND, OR XOR) between these two areas and stores the result back to the destination. It can be expressed in simple notation as:

Destination ← Source op Destination.

op: AND, OR, XOR, etc.

FRAME BUFFER ARCHITECTURE

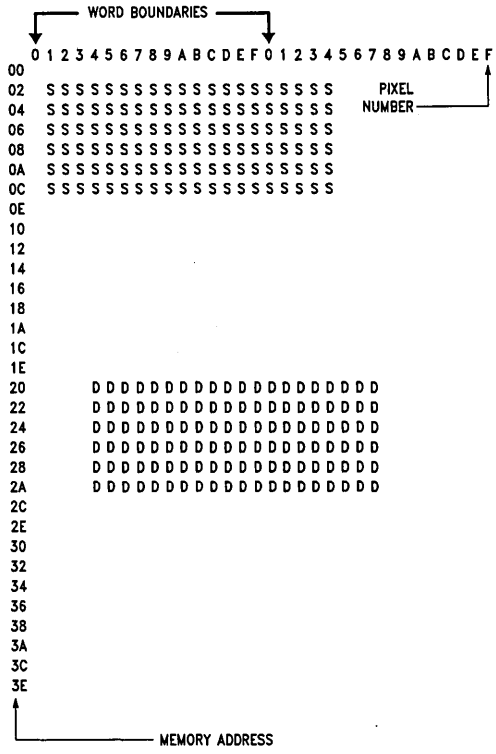
Generally, there are two kinds of frame buffer architectures: PLANE-oriented or PIXEL-oriented. BITBLT takes advantage of the plane-oriented frame buffer architecture's attribute of multiple, adjacent pixels-per-word, facilitating the movement of large blocks of data quickly in a frame buffer. However, the plane-oriented architecture has one inherent problem: the limit of resolution for memory addressing and access is the word, rather than the pixel. The BITBLT source starting address, the BITBLT destination starting address, the BITBLT width and the BITBLT height are all defined in pixels. The BITBLT source data block may start and end at any bit position of any word, and the destination data block also may start and end at any bit position of any word.

BIT ALIGNMENT

Before a logical operation can be performed between the source and the destination data, the source data must first be bit aligned to the destination data. In *Figure 1*, the source data need to be shifted three bits to the right in order to align the first pixel (that is, the pixel at the top left corner) in the source data block to the first pixel in the destination data block. For maximum performance, this alignment function must be implemented with a barrel shifter.

WORD BOUNDARIES AND DESTINATION MASKS

Each BITBLT destination scan line may start and end at any position in any data word. The neighboring bits (the bits sharing the same word address with any words in the destination data block, but not a part of the actual BITBLT rectangle) of the BITBLT destination scan line must remain unchanged after the BITBLT. Due to the plane-oriented frame buffer architecture, all memory operations must be word-aligned. In order to preserve the neighboring bits surrounding the BITBLT destination block, a left mask is needed for all the leftmost data words of the destination block, and a right mask is needed for all the rightmost data words of the destination data block. Both the left mask and the right mask remain the same throughout a given BITBLT operation.



TL/F/9337–17

FIGURE 1. A 32 by 32 Frame Buffer

BITBLT Fundamentals (Continued)

The following example illustrates the bit alignment requirement. In this example, the graphics controller has a 16-bit wide data bus. *Figure 1* shows a 32 pixel by 32 scan line frame buffer which is organized as a long bit stream which wraps around every two words (32 bits). Further, the top left corner of the frame buffer starts from the lowest word in the memory, address 000hex. Each word in the memory contains 16 bits, DQ0–DQ15. The most significant bit of a memory word, DQ0, is defined as the first *displayed* pixel in a word. In other words, memory's DQ0 to DQ15 correspond to pixels 0 to 15 respectively. In this example, BITBLT addresses are expressed in terms of pixel number, starting (with 0) from the upper-leftmost pixel. The BITBLT source starting address is set to 021hex (the second pixel in the third word). The BITBLT destination starting address is set to 204hex (the fifth pixel in the 33rd word). The BITBLT width is set to 013hex (=19 decimal, corresponding to a width of 20 pixels). The BITBLT height is set to 005hex (=5 decimal, corresponding to 6 scan lines).

The left BITBLT mask for the above example is:

0000,1111,1111,1111

The right BITBLT mask for the above example is:

1111,1111,0000,0000

Note: Zeroes in either the left mask or the right mask indicate the destination bits which will not be modified.

BITBLT DIRECTIONS

The BITBLT moves a rectangular block of data in a frame buffer. For a plane-oriented frame buffer, the BITBLT process can be considered a subroutine which has two nested loops. The loops are preceded by the BITBLT setup computations. The outer loop is the BITBLT source and destination scan line pixel starting address calculation and line count test for completion. The innermost loop is the actual BITBLT data movement for a single BITBLT scan line and word count test for completion. The length of the innermost loop is the word count of the BITBLT width. The length of the second loop is equal to the BITBLT's height (number of scan lines involved in a BITBLT):

```
BITBLT: calculate BITBLT setup parameters ;once per BITBLT
                such as
                width, height
                bit misalignment (shift number)
                left, right masks
                horizontal, vertical directions
                etc
                .
                .
OUTERLOOP: calculate source, dest addresses ;once per scanline
    INNERLOOP: move data and increment addresses ;once per word
    UNTIL       done horizontally
UNTIL           done vertically
RETURN          (from BITBLT).
```

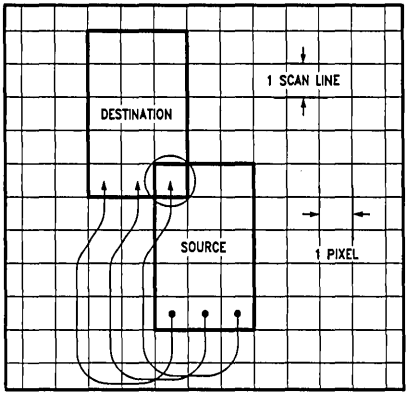
Each loop can be executed in one of two directions: the inner loop from left to right or right to left, the outer loop from top to bottom (down) or bottom to top (up).

The ability to move data starting from any corner of the BITBLT rectangle is necessary to avoid destroying the BITBLT source data as a result of destination writes when the source and destination are overlapped (i.e., when they share pixels). This situation is routinely encountered while panning or scrolling.

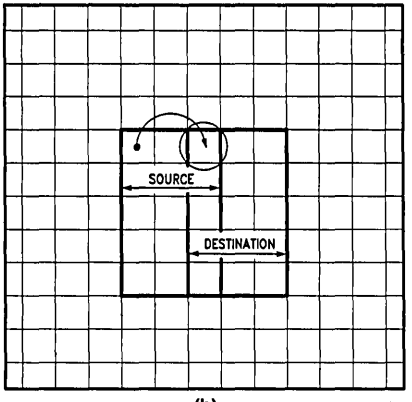
A determination of the correct execution directions of the BITBLT must be performed whenever the source and destination rectangles overlap. *Any* overlap will result in the destruction of source data (from a destination write) if the correct vertical direction is not used. Horizontal BITBLT direction is of concern only in certain cases of overlap, as will be explained below.

Figure 2 (a) and *(b)* illustrate two cases of overlap. Here, the BITBLT rectangles are three pixels wide by five scan lines high; they overlap by a single pixel in *(a)* and a single column of pixels in *(b)*. For purposes of illustration, the BITBLT is assumed to be carried out pixel-by-pixel. This convention does not affect the conclusions.

In *Figure 2(a)*, if the BITBLT is performed in the UP direction (bottom-to-top) one of the transfers of the bottom scan line of the source will write to the circled pixel of the destination. Due to the overlap, this pixel is also part of the uppermost scan line of the source rectangle. Thus, data needed later is destroyed. Therefore, this BITBLT must be performed in the DOWN direction. Another example of this occurs any time the screen is moved in a purely vertical direction, as in



(a) TL/F/9337–18



(b) TL/F/9337–19

FIGURE 2. Overlapping BITBLT Operations

BITBLT Fundamentals (Continued)

scrolling text. It should be noted that, in both of these cases, the choice of horizontal BITBLT direction may be made arbitrarily.

Figure 2(b) demonstrates a case in which the horizontal BITBLT direction may not be chosen arbitrarily. This is an instance of purely horizontal movement of data (panning). Because the movement from source to destination involves data within the same scan line, the incorrect direction of movement will overwrite data which will be needed later. In this example, the correct direction is from right to left.

BITBLT VARIATIONS

Some implementations of BITBLT are defined in terms of three operands: source, destination and mask/texture. This third operand is commonly used in monochrome systems to incorporate a stipple pattern into an area. These stipple patterns provide the appearance of multiple shades of gray in single-bit-per-pixel systems, in a manner similar to the 'halftone' process used in printing.

Destination ← Texture op1 Source op2 Destination

While the BPU is essentially a two-operand device, three-operand BITBLT can be implemented quite flexibly and efficiently by performing the two operations serially. The BPU permits the use of any of its sixteen operations for each of the two operators shown above as 'op1' and 'op2'. Additionally, the on-chip FIFO can be used to store the intermediate result (the result of op1 later used as an operand of op2) thus minimizing the number of memory accesses required.

ENHANCING BITBLT PERFORMANCE

There are various ways to enhance BITBLT performance (speed). The simplest way is to try to get data in and out of the memory system quickly. Most of the bitmapped graphics systems utilize DRAMs for both cost and storage density reasons. Since the BITBLT data shows strong locality, the graphics system can take advantage of certain fast memory access modes available to the DRAMs, such as page mode access, static column access, etc. The BPU, by means of an internal FIFO, can pipe the BITBLT source data to reduce the frequency of switching out of the current page address space, thus maximizing the ability of the system to capitalize on the data's locality. This operation is described in the following section.

PIPING THE BITBLT SOURCE DATA

When the BITBLT width is more than a word, up to 16 source data words can be piped into the BPU's on-chip FIFO. At the end of each BITBLT scan line or at the end of 16 source data words, the controller switches from the BITBLT source address space to the BITBLT destination address space. When the BITBLT destination data word is fetched, two possible memory control sequences can be used. One is the modify-write sequence: write the BITBLT result back to the destination memory immediately after the logical function is executed. The second sequence involves storing the BITBLT result back to the BPU's on-chip FIFO, to a maximum of 16 words. Either at the end of each BITBLT destination scan line or at the 16th destination data word, the BITBLT resultant data is then read out from the FIFO and written to the BITBLT destination memory sequentially.

Summary of the BITBLT Memory Control Sequences

BITBLT MEMORY SEQUENCE I

1) Load the BPU Control Register with [BIS, SN, LM, RM], via the data bus.
2) Load the BFU FS register with function select code.
3) Read in the BITBLT source data up to 16 words (17 words in certain cases), barrel-shift, then write them into the on-chip FIFO. (Only 16 barrel-shifted data words can be stored.)
4) Read in the BITBLT destination data while the barrel-shifted source data is read out from the on-chip FIFO and the selected logical operation is executed, then write back to destination.
5) Go to step 3 until the end of the BITBLT scan line.
6) Go to step 3 for the remaining BITBLT scan lines.

BITBLT MEMORY SEQUENCE II

1) Load the BPU Control Register with [BIS, SN, LM, RM] via the data bus.
2) Load BPU FS register with function select code.
3) Read in the BITBLT source data up to 16 words (17 words in certain cases), barrel-shift, then write them into the on-chip FIFO. (Only 16 barrel-shifted data words can be stored.)
4) Read in the BITBLT destination data in sequence, execute the selected logical operation and then write the result back to the on-chip FIFO, maximum 16 BITBLT data words.
5) Read BITBLT result from the FIFO and write them back to the BITBLT destination memory.
6) Go to step 3 until the end of the BITBLT scan line.
7) Go to step 3 for the remaining BITBLT scan lines.

Functional Block Description

BPU CONTROL REGISTER

The BPU Control Register (CR) is a 13-bit register consisting of three 4-bit fields and one single-bit field. The Right Mask field, RM, controls the BITBLT right mask pattern. The Left Mask, LM, controls the BITBLT left mask pattern. The barrel Shift Number, SN, determines the number of bit positions shifted by the Barrel Shifter. The BIS bit controls the organization of two 16-bit words at the input to the barrel shifter.

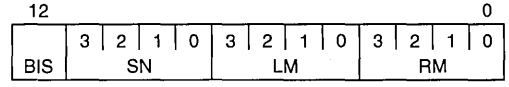


FIGURE 3. Control Register Fields

The CR is loaded by presenting the appropriate data at the Data Port (D0–D15) and then asserting a low level on the $\overline{CRE}$ (Control Register Enable) input. Data is latched into the register on the rising edge of $\overline{CRE}$.

Functional Block Description (Continued)

When the DP8511 is controlled by the RGP, the CR is treated as a memory mapped write only register and resides in the RGP's memory space. The address of this register is determined by the RGP's BPUB register (more information can be found in the RGP Programmer's Reference Manual). The CR Register contents are not affected when the BPU is in the line drawing mode (L/$\overline{B}$ = 1).

Left and Right Masks

The Left and Right mask fields are used to determine which portion of the destination data word to preserve during a BITBLT operation. Masks are used when a destination starting or ending address falls at a pixel address that is not on a word boundary. Since data is accessed and modified in 16-bit word quantities, neighboring bits on both sides of the destination data block must be protected or they risk being corrupted when the destination data is logically combined with the source data. The masks isolate the logic operation to only those bits that are enabled with a one in the mask fields (of course, RME and/or LME must be asserted concurrently). The truth table for the left and right mask patterns is shown in Table I.

The RM and LM values are automatically determined by the RGP during BITBLT and are based on the starting address of the destination data block specified in the DSAD register.

Shift Number

There are 16 different barrel shift operations controlled by the SN of the Control Register. Let A = a15 . . . a0, B = b15 . . . b0 and C = c15 . . . c0, A and B are the input words, C is the output. An i-bit barrel-shift operation on A and B denoted by C = S(i; A, B) is the operation of concatenating the least significant (i) bits of word B to the most significant (16-i) bits of word A.

When A = B, the C = S(i; A, B) is equivalent to having an i-bit circular left shift. The i-bit circular right shift is equivalent to the (16-i) bit circular left shift.

The truth table of the barrel-shift operation S(i, A, B) is shown in Table III. The shift number is represented by "i", A0–A15 corresponds to the most significant input word of the barrel shifter, and B0–B15 corresponds to the least significant input word of the barrel shifter. C0–C15 is the barrel shifter output.

Barrel Input Select (BIS)

The Barrel Input Select bit is used to route two 16-bit words, one in the Barrel Input Latch (BIL) and the other in the Data Input Latch (DIL), to either the most significant or the least significant word position of the Barrel Shifter. When the BIS bit is set high, the DIL source serves as the most significant input word to the barrel shifter with BIL data going to the least significant word position. When the BIS bit is set low, the DIL source input is routed to the least significant position of the barrel shifter and BIL data goes to the most significant position.

This bit is automatically set by the RGP during BITBLT operations.

FUNCTION SELECT REGISTER

The Function Select Register (FSR) is a 4-bit register used to set one of 16 BITBLT logic operations to be performed between the source and a destination data blocks. The function select truth table can be found in Table II.

TABLE I. Left and Right Mask Truth Table

LM = 0	L_mask =	1111	11111111 1111
LM = 1	L_mask =	0111	11111111 1111
LM = 2	L_mask =	0011	11111111 1111
LM = 3	L_mask =	0001	11111111 1111
LM = 4	L_mask =	0000	11111111 1111
LM = 5	L_mask =	0000	01111111 1111
LM = 6	L_mask =	0000	00111111 1111
LM = 7	L_mask =	0000	00011111 1111
LM = 8	L_mask =	0000	00001111 1111
LM = 9	L_mask =	0000	00000111 1111
LM = 10	L_mask =	0000	00000011 1111
LM = 11	L_mask =	0000	00000001 1111
LM = 12	L_mask =	0000	00000000 1111
LM = 13	L_mask =	0000	00000000 0111
LM = 14	L_mask =	0000	00000000 0011
LM = 15	L_mask =	0000	00000000 0001
RM = 0	R_mask =	1000	00000000 0000
RM = 0	R_mask =	1100	00000000 0000
RM = 2	R_mask =	1110	00000000 0000
RM = 3	R_mask =	1111	00000000 0000
RM = 4	R_mask =	1111	10000000 0000
RM = 5	R_mask =	1111	11000000 0000
RM = 6	R_mask =	1111	11100000 0000
RM = 7	R_mask =	1111	11110000 0000
RM = 8	R_mask =	1111	11111000 0000
RM = 9	R_mask =	1111	11111100 0000
RM = 10	R_mask =	1111	11111110 0000
RM = 11	R_mask =	1111	11111111 0000
RM = 12	R_mask =	1111	11111111 1000
RM = 13	R_mask =	1111	11111111 1100
RM = 14	R_mask =	1111	11111111 1110
RM = 15	R_mask =	1111	11111111 1111

"1" = Enable Logic Op
"0" = Disable Logic Op

The 16 BITBLT functions can be expressed as:

$$f3 * (-s * -d) +$$
$$f2 * (-s * d) +$$
$$f1 * (s * -d) +$$
$$f0 * (s * d) +$$

where f3–f0 are the bits of the Function Select Registers, 's' is the source data and 'd' is the destination data.

The FSR is loaded by asserting the Function Select Enable ($\overline{FSE}$) pin low while valid data is made available at the data port (D0–D15). Data is latched into the register on the rising edge of $\overline{FSE}$.

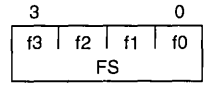
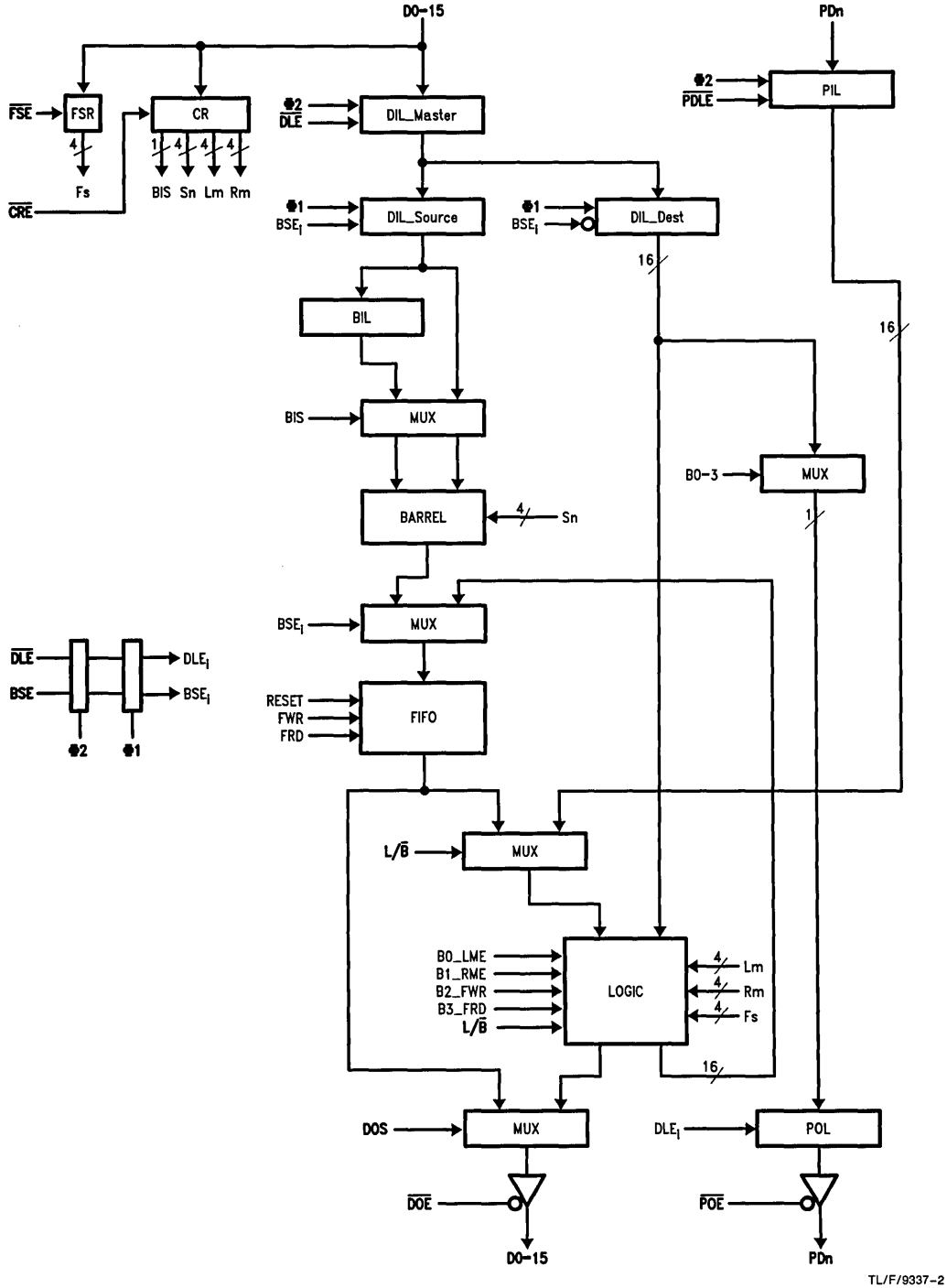


FIGURE 4. Function Select Register (FSR)

The contents of the FSR are defined by the user prior to BPU operations. In multi-plane systems that use a BPU per plane, each BPU can have its logic function programmed independently. This feature allows the RGP to BITBLT data to all bitplanes concurrently while maintaining the flexibility of having unique logical operations being performed on each plane.

Block Diagram



Functional Block Description (Continued)

TABLE II. BITBIT Function Definitions

Function Select Bits				Operation
f3	f2	f1	f0	Performed
0	0	0	0	0
0	0	0	1	s and d
0	0	1	0	s and −d
0	0	1	1	s
0	1	0	0	−s and d
0	1	0	1	d
0	1	1	0	s xor d
0	1	1	1	s or d
1	0	0	0	−s and −d
1	0	0	1	s xnor d
1	0	1	0	−d
1	0	1	1	s or −d
1	1	0	0	−s
1	1	0	1	−s or d
1	1	1	0	−s or −d
1	1	1	1	1

Note:
d: destination data
s: source data
f3–f0: function select code, which selects one of the 16 BITBLT functions.

BARREL SHIFTER

The function of the Barrel Shifter is to align the BITBLT source data to the destination data. Bit alignment may cross word boundaries.

The Barrel Shifter is implemented as a 32-to-16-bit multiplexer. Depending on the type and length of a BITBLT operation the necessary source data words are fetched from memory into the BPU to form a 32-bit input to the Barrel Shifter. The Barrel Input Latch (BIL) stores the first source data word fetched and the Source Data Input Latch (DIL-Source) stores the subsequent source data word.

A multiplexer precedes the Barrel Shifter to facilitate swapping the input words if necessary. This word swapping is controlled by the state of the BIS bit in the Control Register and does not affect the ordering of the data bits of the input words. This swap mechanism facilitates the fetching of BITBLT data from left-to-right or from right-to-left.

FIFO

The FIFO, 16 bits by 16 words, constitutes the BPU's on chip storage. Implemented as a dual port register file, the FIFO has separate READ/WRITE control inputs, FIFO Read (FRD) and FIFO Write (FWR). The registers are selected via two shift register ring counters which are incremented via the FRD and FWR inputs. These counters are set to zero with the $\overline{\text{RESET}}$ pin.

The FIFO facilitates the use of fast localized memory access modes such as page and static column modes by providing storage for multiple words of barrel shifted words.

BITBLT LOGIC CONTROL UNIT

The BITBLT Logic Control Unit (LCU) is responsible for the mask and bitwise logical operations performed on BITBLT and line drawing data.

In the BITBLT mode ($L/\overline{B} = 0$), the LCU performs a bitwise logical operation between a source data word read from the FIFO and the Destination Data Input Latch contents. The logic operation performed is specified in the FS Register. The LCU is also responsible for masking the appropriate destination data bits from change during the logic operation. The masking function is determined by the values set in the LM and RM fields of the Control Register and the state of both LME and RME control inputs.

During Linedrawing ($L/\overline{B} = 1$), the LCU performs a bitwise logical operation between the contents of the Pixel Input Latch and a single bit of the Destination Data Input Latch contents. This bit is selected by the state of Pixel Address bits B0–B3. The logical operation function is determined by the FS Register contents.

TABLE III. Barrel Shifter Truth Table*

i	c0	c1	c2	c3	c4	c5	c6	c7	c8	c9	c10	c11	c12	c13	c14	c15
0	a0	a1	a2	a3	a4	a5	a6	a7	a8	a9	a10	a11	a12	a13	a14	a15
1	a1	a2	a3	a4	a5	a6	a7	a8	a9	a10	a11	a12	a13	a14	a15	b0
2	a2	a3	a4	a5	a6	a7	a8	a9	a10	a11	a12	a13	a14	a15	b0	b1
3	a3	a4	a5	a6	a7	a8	a9	a10	a11	a12	a13	a14	a15	b0	b1	b2
4	a4	a5	a6	a7	a8	a9	a10	a11	a12	a13	a14	a15	b0	b1	b2	b3
5	a5	a6	a7	a8	a9	a10	a11	a12	a13	a14	a15	b0	b1	b2	b3	b4
6	a6	a7	a8	a9	a10	a11	a12	a13	a14	a15	b0	b1	b2	b3	b4	b5
7	a7	a8	a9	a10	a11	a12	a13	a14	a15	b0	b1	b2	b3	b4	b5	b6
8	a8	a9	a10	a11	a12	a13	a14	a15	b0	b1	b2	b3	b4	b5	b6	b7
9	a9	a10	a11	a12	a13	a14	a15	b0	b1	b2	b3	b4	b5	b6	b7	b8
10	a10	a11	a12	a13	a14	a15	b0	b1	b2	b3	b4	b5	b6	b7	b8	b9
11	a11	a12	a13	a14	a15	b0	b1	b2	b3	b4	b5	b6	b7	b8	b9	b10
12	a12	a13	a14	a15	b0	b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	b11
13	a13	a14	a15	b0	b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	b11	b12
14	a14	a15	b0	b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	b11	b12	b13
15	a15	b0	b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	b11	b12	b13	b14

*i = shift number

A0–A15 = barrel shifter most significant word

B0–B15 = barrel shifter least significant word

C0–C15 = barrel shifter output

Functional Block Description (Continued)

PIXEL PORT

The Pixel Port consists of a single-bit I/O port dedicated to pixel level operations. It consists of a Pixel Input Latch and Pixel Output Latch.

The Pixel Input Latch is used to store a single pixel value that will be logically combined with a destination data word during linedrawing. This value is then written back to the destination memory. The user is responsible for loading the PIL prior to line and point drawing operations.

In multiple bitplane/BPU systems, this port can be used to write single-bit pixel data to all planes concurrently.

The Pixel Output Latch is used for reading a single bit value of a destination data word. In multiple bitplane/BPU systems, this port allows for reading pixel data on the z-axis.

Operational Description

The BPU's primary function is to perform two types of data manipulation tasks: 1) execute shift, mask, and logic operations between source and destination data blocks (BITBLT operation); 2) logically combine line drawing data with destination data (Line Drawing operations).

These operations are carried out in the BPU via 3 major functional blocks: The Barrel Shifter, the FIFO, and the BITBLT logic Unit. These blocks in combination with a variety of latches and multiplexers synchronize, modify and route the data through and around the device.

Dataflow through the BPU is dictated by control parameters previously set up in the Control and Function Select Registers and by the state of various control inputs on the device.

BITBLT OPERATION

The mechanics of a BITBLT operation are relatively straightforward. Following *Figure 5*, a source data word is fetched from memory and latched into the Data Input Latch (DIL-Source) via the DIL-Master latch. A second source data word is subsequently fetched and latched into the DIL-Source latch while the first source data word is simultaneously transferred to the Barrel Input Latch. This makes both the first and second source data words available to the Barrel Shifter as a 32-bit data word. This 32-bit quantity is routed through a crossbar mux and into the Barrel Shifter which produces an aligned 16-bit source word. This data is latched into the FIFO on the next clock cycle.

The data is then read from the FIFO on a subsequent clock cycle and routed to the BITBLT Logic Unit where it is masked and logically combined with a destination data word previously fetched and latched into the DIL-Destination latch. The data is then routed back to the Data Port (D0–D15) so it can be written back to the destination data memory.

LINE DRAWING OPERATION

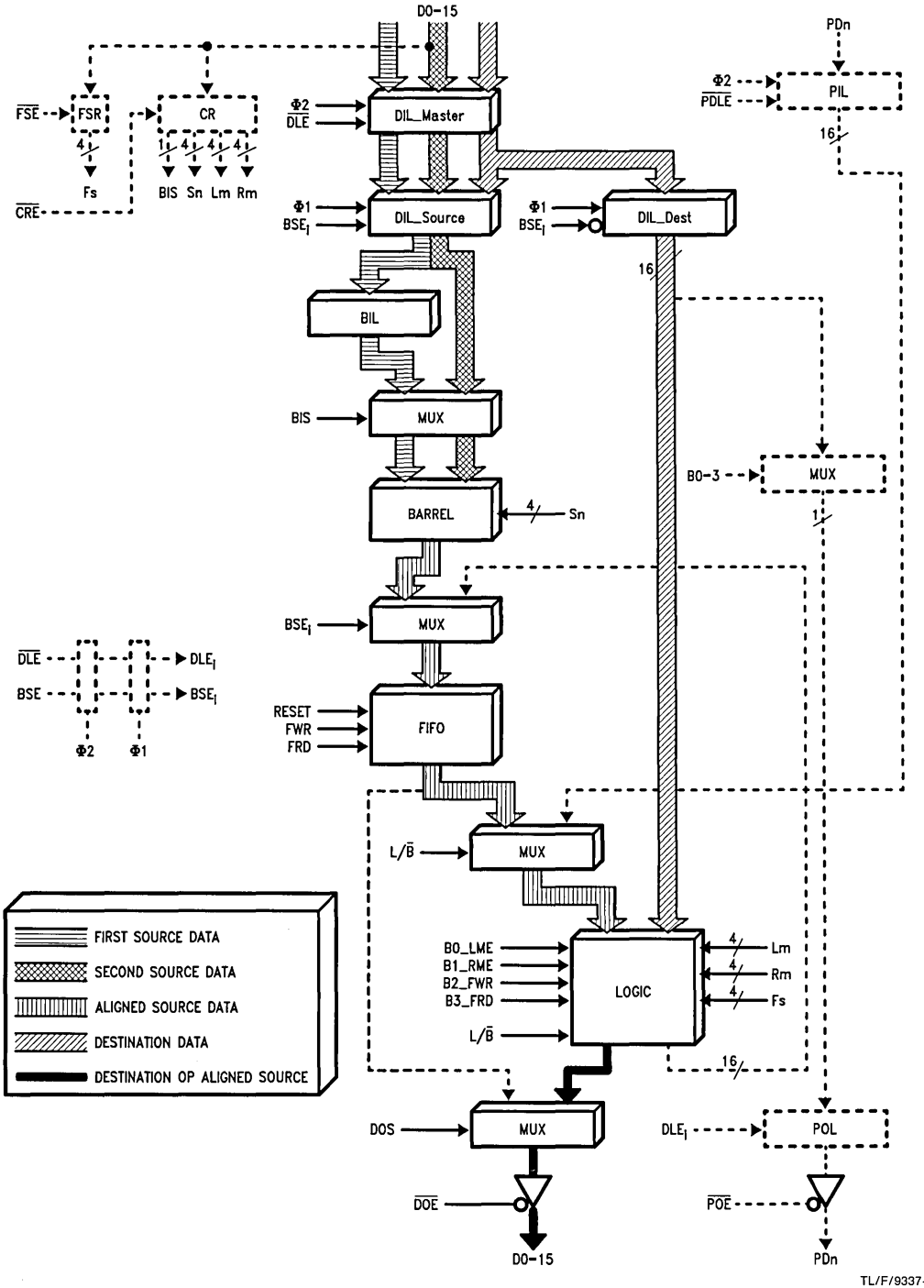
During a line drawing operation (see *Figure 6*), the 'source' data, referred to as the 'Pixel Input Data', actually comes from the Pixel Input Latch (PIL). The PIL input data is presented to the BPU via an external memory mapped buffer which is accessed via an RGP MOV instruction. This value is latched into the PIL and destination data is fetched from memory and written to the DIL-Destination latch. The pixel input data bit is internally replicated into all 16-bit positions of a data word and routed to the BITBLT Logic Unit where it is logically combined with the value in the DIL-Destination. Since only one bit of the destination word is to be modified with pixel data, a mask is generated based on the state of the pixel address lines (B0–B3) so that all other bits of the destination word are protected from change. The resulting data word is then routed back to the Data Port (D0–D15).

The Pixel Output Latch reflects a single pixel data value derived from a 16-bit word previously loaded to the DIL-Destination latch. The Output Pixel Data value is one-of-16 bits of the destination data word selected by the pixel address lines B0–B3 and is purely unmodified destination data.

TABLE IV. DP8500 RGP Drawing Instructions that utilize the DP8511 BPU

INITB	Asserts RST0 (resets FIFO pointers)
BTulsd	Block Transfer
DCbuld	Draw Character
DRLN[A]	Draw Line
DRLNS	Draw Line Steps
DRPGN[A]	Draw Polygon
DRPLN[A]	Draw Polygonal Line
DRPT	Draw Point
FILLAd	Fill Polygon
FILLTd	Fill Trapezoid
MOV s,FSE	Load Function Select Register (FSE = Address of FSE Register)
MOV s,PIL	Load Pixel Input Latch (PIL = Address of Pixel I/O Port)
MOV POL,d	Read Pixel Output Latch (POL = Address of Pixel I/O Port)
RDPT	Read Point

Operational Description (Continued)



TL/F/9337-3

FIGURE 5. Dataflow during a Typical BITBLT Operation. (RGP Instructions: BT, FILLA, DC.)

Operational Description (Continued)

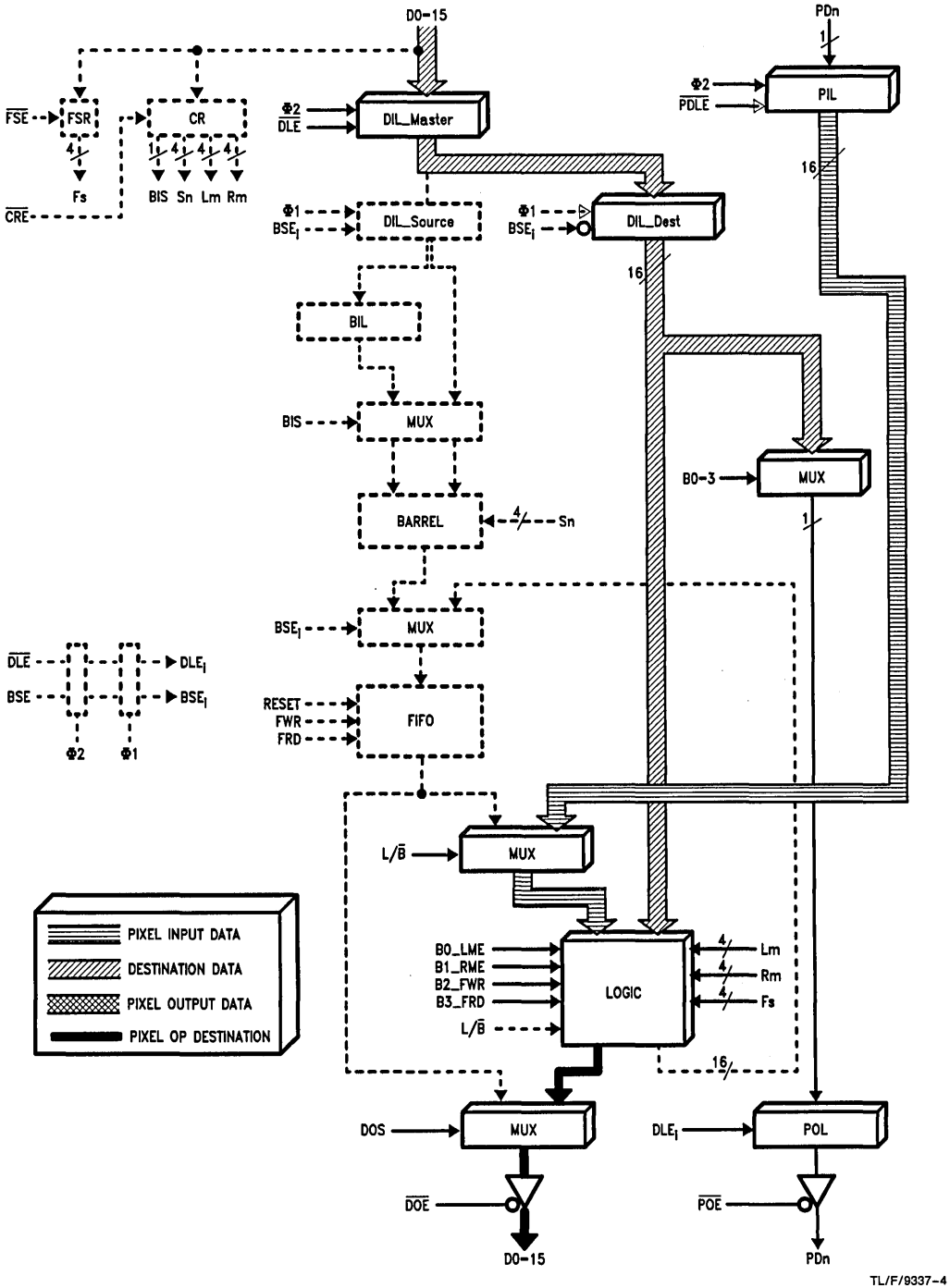


FIGURE 6. Dataflow during a Typical Line Drawing Operation. (RGP Instructions, RDPT, DRPT, DRLN, DRLNS, DRPGN, DRPLN.)

Systems Applications

A typical system example illustrating the BPU's interface to the RGP and system elements is shown in *Figure 7*. Included in the example is National's DP8500 Raster Graphics Processor, the DP8520 Video Ram Controller/Driver and the DP8511 BPU. A user defined state machine is used to control the dataflow between the RGP, BPU and Frame Buffer.

Since the BPU and RGP are members of an integrated family of devices, they have been designed to minimize the need for external glue logic between them. The user is left the task of defining the interface from the RGP/BPU to the frame buffer, tailoring it to the system needs.

STATE MACHINE TASKS

Referring to *Figure 7*, the state machine performs the following tasks:

1. Determines the start of an RGP memory cycle.
2. Determines the type of access to be performed.
3. Generates the necessary timing required to carry out the access including wait state generation.
4. Generates refresh timing signals.
5. Generates BPU Control Register strobe ($\overline{CRE}$).
6. Generates BPU Function Select Register strobe ($\overline{FSE}$).
7. Generates the $\overline{DOE}$, $\overline{DLE}$, $\overline{POE}$, and $\overline{PDLE}$ strobes to the BPU.

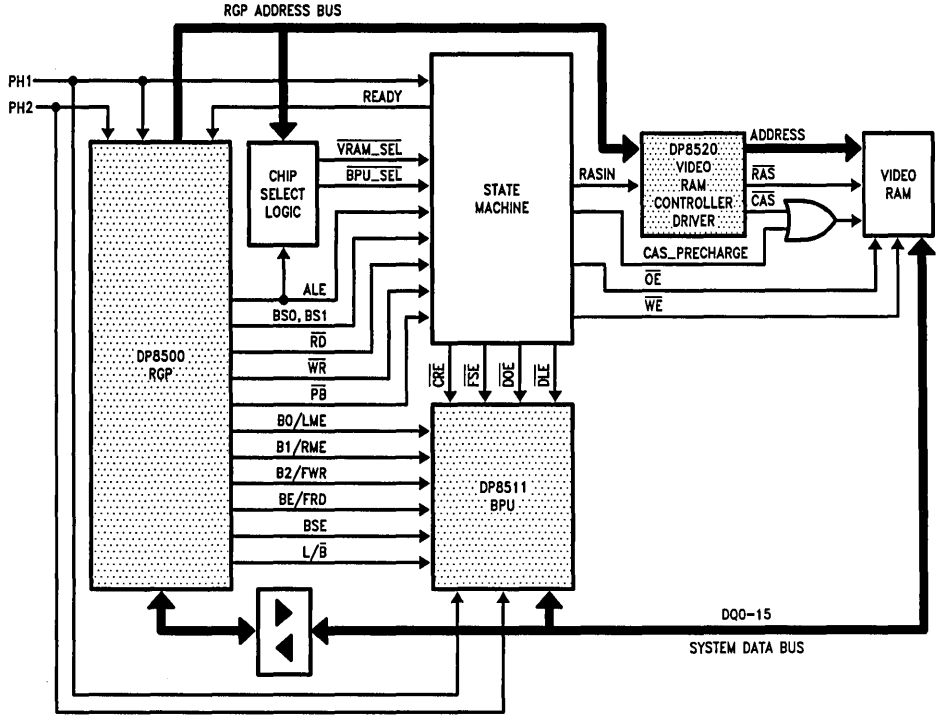
The memory address of the Control Register and Function Select Register are user defined locations in the RGP memory space. It is therefore necessary to generate the $\overline{CRE}$ and $\overline{FSE}$ strobes in order to select these registers. The $\overline{DOE}$ and $\overline{DLE}$ strobes must also be generated by the user since the timing characteristics of these signals are determined by the memory access timing requirements.

MULTIPLE BITPLANE ARCHITECTURE

The Advanced Graphics Chip Set (AGCS) architectural relationship, in particular that of the RGP/BPU devices, is such that multiple plane memory systems can be developed with relative ease and flexibility. The purpose of segregating the BITBLT and Line Drawing functions into a separate device (the BPU) becomes evident when studing the implementation of a multi-plane display system. *Figure 8* illustrates an approach to designing a multi-plane system.

In any BITBLT based display system, it is necessary to be able to move data rapidly between two areas of memory without restrictions imposed by memory organization. In multiplane systems it is necessary to allow for data operations to occur between planes of memory as well as locally within the bit-plane. The ability is governed by the logic in the video plane control block.

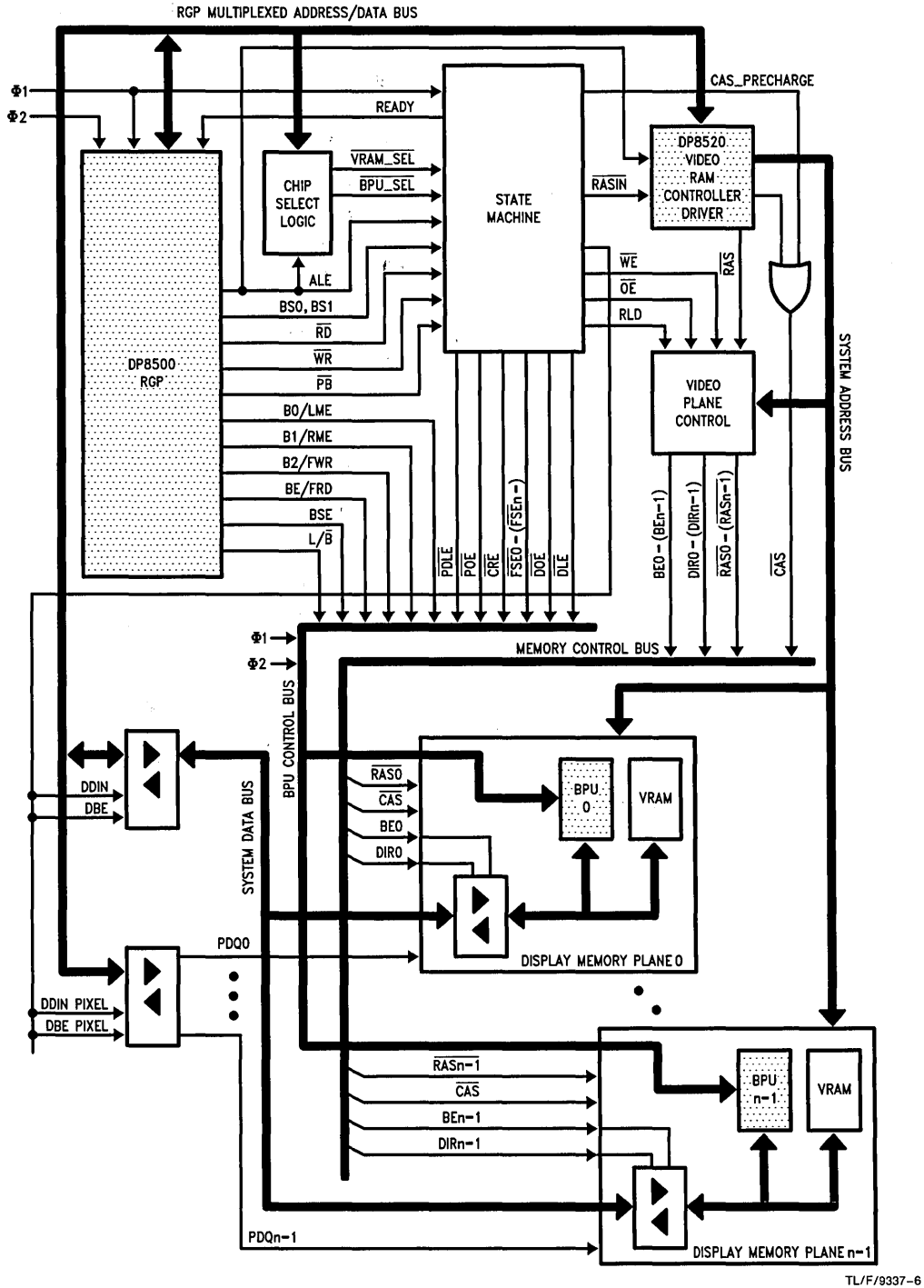
If a BPU is incorporated in each bit-plane of memory and the plane controller is designed correctly, data transfers can be performed in parallel across n-planes of memory, between specific bitplanes, as well as locally on each bitplane. As an added bonus, this design approach allows the system to be expanded to any practical number of bitplanes while maintaining the performance and throughput characteristics of a single plane system.



TL/F/9337–5

FIGURE 7. Typical System Interface

System Applications (Continued)



TL/F/9337–6

FIGURE 8. Typical Multiple Bitplane System

Absolute Maximum Ratings*

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature under Bias	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
All Input or Output Voltage with Respect to GND	−0.5V to +7V
Power Dissipation @ 20 MHz	0.5W

ESD rating to be determined.

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.*

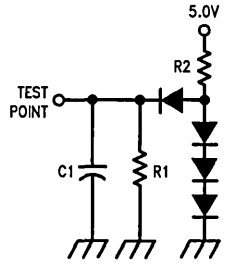
***Note:** These are preliminary specifications.

DC Electrical Characteristics* $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, GND = 0V

Symbol	Characteristics	Conditions	Min	Typ	Max	Units
V_{IH}			2.0		V_{CC} + 0.5	V
V_{IL}			−0.5		0.8	V
V_{CH}	MOS Clock High	PH1, PH2 Pins Only, MOS	V_{CC} − 0.5		V_{CC} + 0.5	V
V_{CL}	MOS Clock Low	PH1, PH2 Pins Only, MOS	−0.5		0.3	V
V_{CLT}	MOS Clock Ringing	PH1, PH2 Pins Only, MOS	−0.5		0.5	V
V_{TCH}	TTL Clock High	TTL Clock/PH1 Only	2.5			V
V_{TCL}	TTL Clock Low	TTL Clock/PH1 Only			0.8	V
V_{OH}		I_{OL} = −3 mA	2.4			V
V_{OL}		I_{OL} = 3 mA			0.5	V
I_{IN}	Leakage Current	$V_{IN} = V_{IH}$ or V_{IL}			±10	μA
I_{OZ}	TRI-STATE® Leakage	$V_O = V_{CC}$ or GND			±10	μA
I_{CC1}	Quiescent Current	PH1, PH2 at 20 MHz		3		mA
I_{CC2}	Supply Current	PH1, PH2 at 100 kHz		10		mA
I_{CC3}	Supply Current	PH1, PH2 at 20 MHz		20		mA
C_{IN}	Input Capacitance	f_{in} at 1 MHz			10	pF

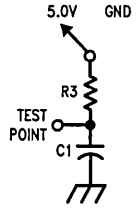
Note: All output test conditions are 50 pF plus one TTL load.

*These are preliminary specifications.



TL/F/9337–7

FIGURE 9. BPU Output Test Load Circuitry



TL/F/9337–8

FIGURE 10. BPU Output TRI-STATE Test Load Circuitry

Note 1: C1 = 50 pF
R1 = 6 kΩ
R2 = 1.3 kΩ
R3 = 1.8 kΩ

Note 2: Connect SW to +5V for tpLZ and tpZL measurements.

Note 3: Connect SW to GND for tpHZ and tpZH measurements.

AC Electrical Characteristics

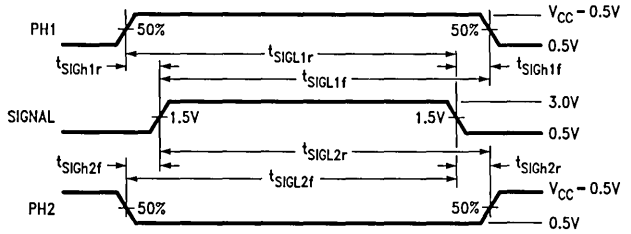
Symbol	Description	Min	Typ	Max	Units
f	PH1, PH2 Frequency			20	MHz
t_{pn1b}	PH1 High Time (10% to 10%)	16			ns
t_{pn2b}	PH2 High Time (10% to 10%)	16			ns
t_{pn1b}	PH1 High Time (50% to 50%)	19			ns
t_{pn2b}	PH2 High Time (50% to 50%)	19			ns
t_{ck1}	50% PH1 Rising to 50% PH2 Rising	25			ns
t_{ck2}	50% PH2 Rising to 50% PH1 Rising	22			ns
t_{nov1}	PH2-to-PH1 50% Non-Overlap Time	3			ns
t_{nov2}	PH1-to-PH2 50% Non-Overlap Time	3			ns
t_{nov3}	PH2-to-PH1 10% Non-Overlap Time	0			ns
t_{nov4}	PH1-to-PH2 10% Non-Overlap Time	0			ns
t_{les1}	$\overline{DLE}$, $\overline{PDLE}$ to PH2 Setup Time (TCS = 0)	15			ns
t_{les2}	$\overline{DLE}$, $\overline{PDLE}$ to PH1 Setup Time (TCS = 1)	25			ns
t_{leh1}	$\overline{DLE}$, $\overline{PDLE}$ to PH2 Hold Time (TCS = 0)	10			ns
t_{leh2}	$\overline{DLE}$, $\overline{PDLE}$ to PH1 Hold Time (TCS = 1)	20			ns
t_{leis}	$\overline{DLE}$, $\overline{PDLE}$ to PH2 Invalid Switching Time	15			ns
t_{ds2f}	Data to PH2 Setup Time (TCS = 0)	15			ns
t_{ds1r}	Data to PH1 Setup Time (TCS = 1)	25			ns
t_{dh2f}	Data to PH2 Hold Time (TCS = 0)	10			ns
t_{dh1r}	Data to PH1 Hold Time (TCS = 1)	20			ns
t_{dpZH}	Data TRI-STATE to High Delay Time		20		ns
t_{dpZL}	Data TRI-STATE to Low Delay Time		20		ns
t_{dpHZ}	Data High to TRI-STATE Delay Time		20		ns
t_{dpLZ}	Data Low to TRI-STATE Delay Time		20		ns
t_{ctls2f}	Control Signals to PH2 Setup Time (TCS = 0)	25			ns
t_{ctls1r}	Control Signals to PH1 Setup Time (TCS = 1)	25			ns
t_{ctlh2f}	Control Signals to PH2 Hold Time (TCS = 0)	10			ns
t_{ctlh1r}	Control Signals to PH1 Hold Time (TCS = 1)	20			ns
t_{cl}	L/$\overline{B}$, DOS to DATA Switching Time		30		ns
t_{pw}	$\overline{CRE}$, $\overline{FSE}$ Pulse Width	20			ns
t_s	Data to $\overline{CRE}$, $\overline{FSE}$ Setup Time	20			ns
t_h	Data to $\overline{CRE}$, $\overline{FSE}$ Hold Time	5			ns
t_{dq1r}	PH1 to Valid Output Data (DOS = 0)		25		ns
t_{dq1r}	PH1 to Valid Output Data (DOS = 1)		15		ns
t_{PDn1r}	PH1 to Valid Pixel Data		50		ns

*These are preliminary specifications.

Timing Diagrams

DEFINITIONS

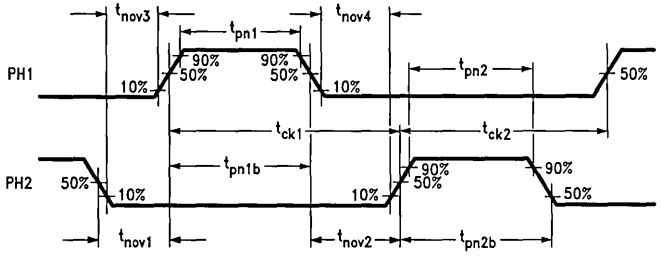
All the timing specifications given in this section refer to 50% of the leading or trailing edges of the appropriate clock phase and 0.5V or 3.0V on the appropriate signal as illustrated in the following figures, unless stated otherwise.



TL/F/9337–9

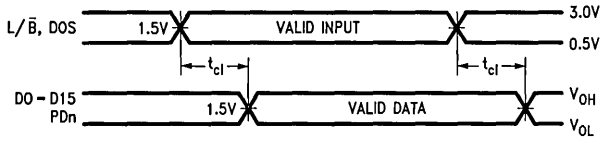
Note: Data is measured at 1.5V to 50% points of PH1 and PH2.

FIGURE 11. Timing Specification Standard



TL/F/9337–10

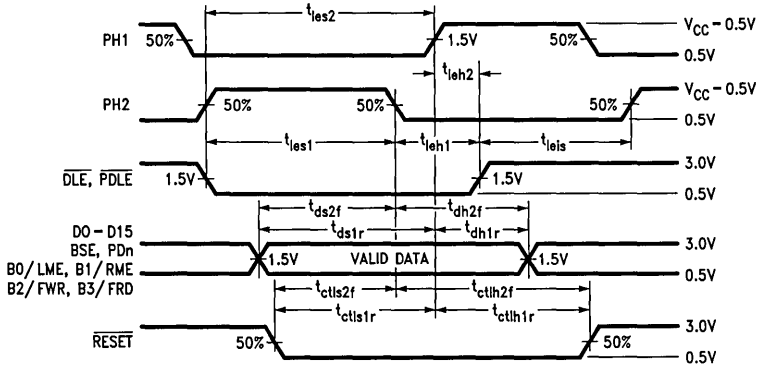
FIGURE 12. Two-Phase MOS Clock Timing Specification



TL/F/9337–11

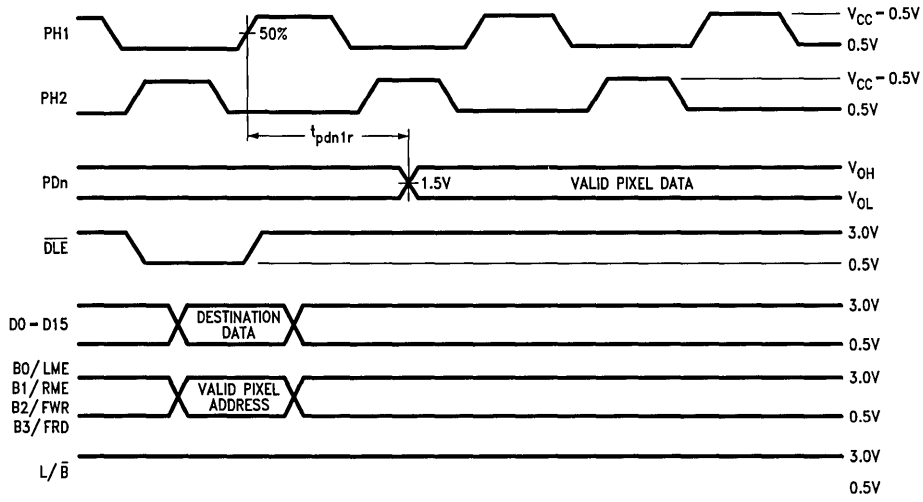
FIGURE 13. Mode Control Timing Specification

Timing Diagrams (Continued)



TL/F/9337–12

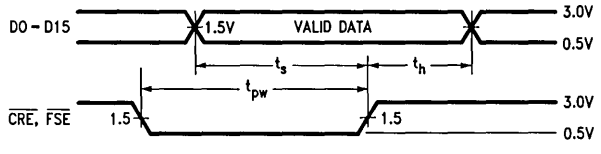
FIGURE 14. Input Data Timing Specification



TL/F/9337–13

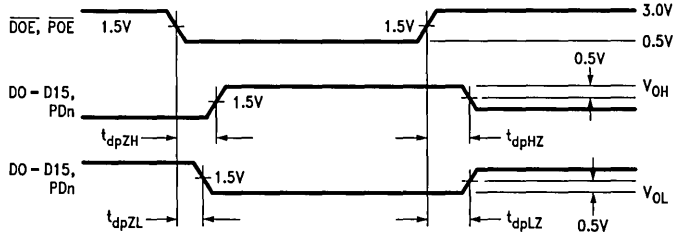
FIGURE 15. Pixel Read Timing Specification

Timing Diagrams (Continued)



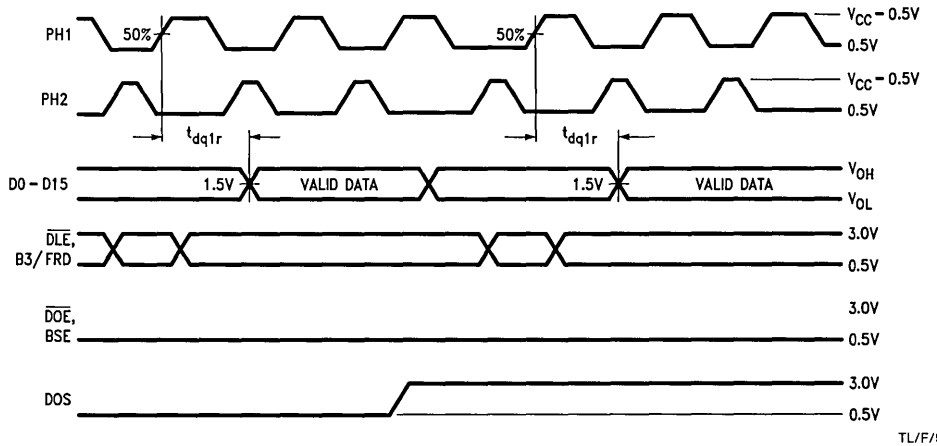
TL/F/9337-14

FIGURE 16. $\overline{CRE}$ and $\overline{FSE}$ Timing Specification



TL/F/9337-15

FIGURE 17. Output Enable Timing Specification



TL/F/9337-16

FIGURE 18. FIFO/DIL—Dest to Valid Data Timing Specification

National Semiconductor

DP8512 Video Clock Generator

General Description

The DP8512 is a clock generator intended for use in medium- to high-performance CRT graphics systems. The device simplifies timing and minimizes phase skew between the various signals involved in the transfer of DRAM (or VDRAM) data into a DAC for display on a CRT. The device generates several synchronous clocks from a single crystal resonator input using digital phase locked loop (PLL) techniques. These clock signals include a graphics processor clock, a raster-scan pixel clock, and various gated TTL and ECL clocks required to transfer data from VRAM to video shift registers. Circuitry is also provided which enables the user to phase lock his graphics system to an external video source. The DP8512 is optimized for single-board graphics systems. The DP8513 is a similar device intended for multi-board synchronous clock generation.

The graphics processor clocks (PHI1 and PHI2) are non-overlapping two-phase clocks with MOS-compatible outputs capable of driving 100 pF loads at up to a 20 MHz rate.

The raster-scan pixel clock (PCLK) and the parallel load clock (LCLK3) required for video shift register operation are generated from the crystal resonator source using two programmable counters in a phase locked loop configuration. Video word widths from 4 to 64 in increments of 4 are accommodated by these counters. The ECL-compatible PCLK outputs are capable of operating at up to 225 MHz from either a positive or a negative supply voltage.

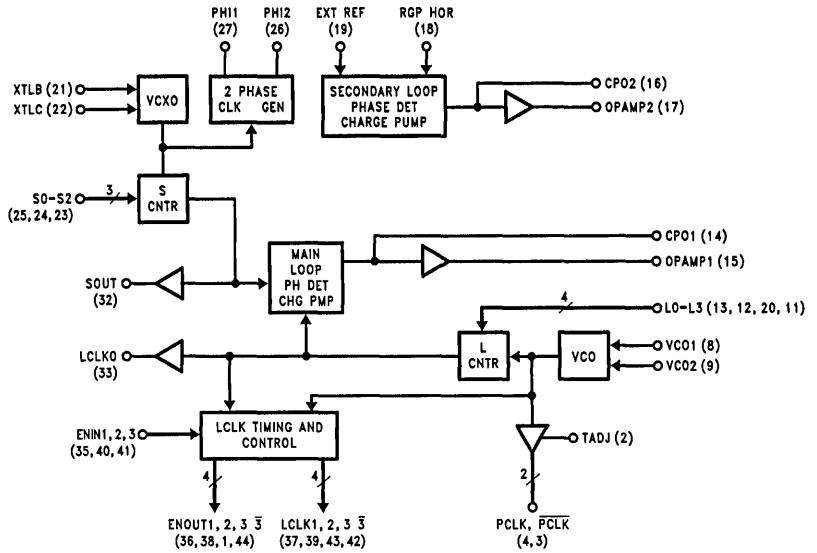
Two gated TTL clock outputs (LCLK1 and LCLK2) are also provided to enable easy transfer of data from a VRAM serial shift register directly into a video shift register or indirectly through a FIFO.

The graphics system can be linked to an external video source by means of a second phase locked loop on the chip. The crystal resonator can be operated as a voltage controlled oscillator allowing adjustment of its frequency until the system's horizontal frequency agrees with that of the external source.

Features

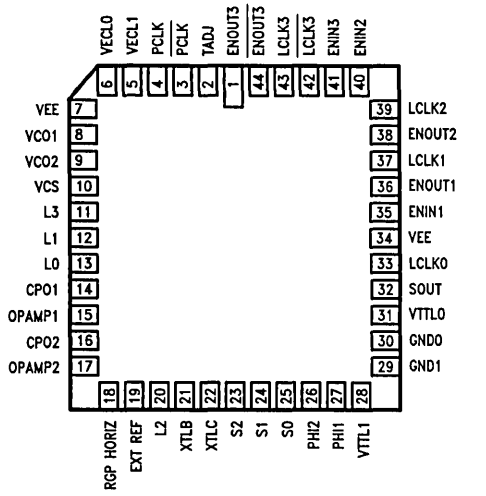
- On-chip crystal oscillator and phase-locked-loop generate synchronized system clock, PCLK, and LCLK
- MOS-compatible single-phase or non-overlapping two-phase system clock output
- 225 MHz ECL differential output pixel clock (PCLK)
- Gated and non-gated load clock (LCLK) outputs ease VRAM-to-VSR synchronization
- Accommodates video word widths from 4 to 64 in increments of 4
- Timing Adjust pin (Tadj) provides a fixed offset adjustment of PCLK to LCLK to ease system design
- ECL circuitry can be referenced to positive or negative power supply
- Enables horizontal synchronization to an external source

Block Diagram (numbers in parentheses indicate pin numbers)



TL/F/8758-1

Connection Diagram



TL/F/8758–2

Order Number DP8512V
See NS Package Number V44A

Pin Descriptions

1, 44—ENOUT3, $\overline{\text{ENOUT3}}$: Differential ECL video enable output synchronous to LCLK0 and gated by ENIN3 (10k and 100k ECL compatible). Outputs require conventional ECL 50Ω terminations.

2—TADJ: Timing Adjust pin allows the PCLK output transition to be offset by 2.5 ns relative to the ECL LCLK3 and ENOUT3 transitions to accommodate the setup and hold requirements of various shift registers more easily. A Logic HI = VECL0 and a Logic LOW = VEE.

3, 4—$\overline{\text{PCLK}}$, PCLK: Differential ECL pixel clock outputs driven by the VCO in the main loop (10k and 100k ECL compatible). Outputs require conventional ECL 50Ω terminations.

5—VECL1: ECL output buffer positive power supply which can be operated from 0V to +5.7V relative to GND. Note 1.

6—VECL0: ECL internal logic positive power supply which can be operated from 0V to +5.7V relative to GND. Note 1.

7, 34—VEE: ECL negative power supply. Note 1.

8, 9—VCO1, VCO2: External tank circuit connections for the Pierce VCO. See typical applications for typical wiring.

10—VCS: No connection required.

11, 12, 13, 20—L3, L1, L0, L2: Four bit word input used to select the L Counter modulus. Any modulus from 4 to 64 may be selected in increments of 4. L0 is the least significant bit. A Logic HI = VECL0 and a Logic LOW = VEE. It is recommended that these inputs be bypassed to VECL0 with .01 μF and the jumper lengths be minimized and not cross over any TTL traces as the logic thresholds are VECL0 − 200 mV.

14—CPO1: Main loop charge pump output. Used in conjunction with OPAMP1 to form the external loop filter.

15—OPAMP1: Op amp output of the main loop. This output is used to control the pixel clock frequency via the varactor diodes in the LC tank circuit.

16—CPO2: Charge pump output of the secondary loop. Used in conjunction with OPAMP2 to form the external loop filter.

17—OPAMP2: Op amp output of the secondary loop. This output is used to vary the crystal fequency (VCXO) in systems where it is desired to lock to an external video source.

18—RGP HORIZ: TTL compatible secondary loop phase comparator input. This signal completes the feedback path from the VCXO by way of the DP8500 Raster Graphics Processor's Horizontal Output. The phase detector #2 is negative edge triggered from this pin.

19—EXT REF: TTL compatible detector #2 reference input. This is the optional horizontal input for systems where it is desired to lock to an external video source. The phase detector #2 is negative edge triggered from this pin.

21, 22—XTLB, XTLC: External connections for the Pierce crystal oscillator. See typical applications for typical wiring.

23, 24, 25—S2, S1, S0: TTL compatible three bit word that determines the S Counter modulus. S0 is the least significant bit.

26, 27—PHI2, PHI1: MOS compatible two-phase non-overlapping clocks. The frequency of these clocks is that of the crystal frequency. If these outputs drive large capacitor loads, a 10 μF or larger capacitor is required directly across the VTTL1 and GND1 pins.

28—VTTL1: TTL output buffer supply. Specified for 5V ±10% operation. Note 1.

29—GND1: TTL output buffer supply return. Note 1.

30—GND0: TTL internal logic power supply return. Note 1.

31—VTTL0: TTL internal logic positive power supply. Specified for 5V ±10% operation. Note 1.

32—SOUT: TTL compatible ungated output of the S counter. It is also connected to one of the two inputs of the main loop phase comparator.

33—LCLK0: TTL compatible free-running Load clock. This signal is also connected to an input of the main loop phase comparator.

35—ENIN1: TTL compatible video enable input. A high on this input starts LCLK1 on the next positive transition of LCLK0.

36—ENOUT1: TTL compatible video enable output synchronous to LCLK0 and gated by ENIN1.

37—LCLK1: TTL compatible load clock equivalent to LCLK0, but gated by ENIN1.

38—ENOUT2: TTL compatible video enable output synchronous to LCLK0 and gated on the third positive transition of LCLK0 following a valid ENIN2 input.

39—LCLK2: TTL compatible load clock equivalent to LCLK0 but gated by ENIN2.

40—ENIN2: TTL compatible video enable input. A high on this input starts LCLK2 on the next positive transition of LCLK0.

41—ENIN3: TTL compatible video enable input. A high on this input starts LCLK3 on the next positive transition of LCLK0.

42, 43—$\overline{\text{LCLK3}}$, LCLK3: Differential ECL compatible load clock synchronous to LCLK0 and gated by ENIN3 (10k and 100k ECL compatible). Outputs require conventional ECL 50Ω terminations.

Note 1: Refer to the Typical Supply wiring diagrams for acceptable wiring of single and dual supply applications.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
TTL Signals	
Inputs	7V
Outputs	7V
ECL Signals	
Output Current	−50 mA
Supplies	
VEE to GND	−7V to +0.5V
VECL to GND	−0.5V to +7V
VTTL to GND	−0.5V to +7V
ESD susceptibility (see note 5)	1000V

Recommended Operating Conditions (Notes 1, 2, 3, 4)

Symbol	Parameter	Min	Typ	Max	Units
VTTL0, 1 to GND	TTL Power Supply	4.5		5.5	V
VECL0, 1 to VEE	ECL Power Supply	4.2		5.7	V
VEE to GND		−5.7		0	V
V_{IH}	High Level Input Voltage TTL Inputs	2			V
V_{IL}	Low Level Input Voltage TTL Inputs			0.8	V
I_{OH}	High Level Output Current TTL Outputs			−0.4	mA
	High Level Output Current MOS Compatible Outputs			−0.4	mA
I_{OL}	Low Level Output Current TTL Outputs			8	mA
	Low Level Output Current MOS Compatible Outputs			20	mA
F_{PCLK} (Note 6)	Pixel Clock Max Frequency			225	MHz
F_{XTL}	Crystal Oscillator Max Frequency			25	MHz
T_{SU1}	Setup Time ENIN1 to LCLK0	20	11		ns
T_{SU2}	Setup Time ENIN2 to LCLK0	20	11		ns
T_{SU3}	Setup Time ENIN3 to LCLK0	20	11		ns
T_{H1}	Hold Time LCLK0 to ENIN1	0	−9		ns
T_{H2}	Hold Time LCLK0 to ENIN2	0	−9		ns
T_{H3}	Hold Time LCLK0 to ENIN3	0	−9		ns
$T_{ambient}$	Operating Temp Range	0		70	°C

Note 1: See Timing Waveforms for relevant signal edges (positive or negative) from which all setup and hold times measurements are made.

Note 2: TTL inputs—ENIN1, 2, 3, RGP HORIZ, EXT REF, S0, S1, S2.

Note 3: TTL outputs—SOUT, LCLK0, 1, 2, ENOUT 1, 2; MOS Outputs—PHI1, 2.

Note 4: Inputs L0, L1, L2, L3, T_{ADJ} designed to be tied to VECL for high level or shorted to VEE (or left open) for low level. See input schematics.

Note 5: Human body model; 120 pF thru 1.5 kΩ.

Note 6: F_{PCLK} is the maximum frequency that the pixel clock output can be reliably "locked". The VCO range should be controlled to avoid exceeding 235 MHz when the maximum control voltage correction is applied.

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	VTTL0, 1 = 4.5V, I_{IN} = −18 mA					−1.5	V
V_{OH}	Output High Voltage	VTTL0, 1 = 4.5V to 5.5V	TTL Outputs, I_{OH} = −400 μA		VTTL−2			V
			MOS Outputs	I_{OH} = −100 μA	VTTL−0.4			
				I_{OH} = −400 μA	VTTL−2.3			
		VECL0, 1 = 0V VEE = −4.2V	ECL Outputs, 50Ω Load to −2V		−1045		−880	mV
			OPAMP Output, I_{OH} = − 1.25 × I_{CPO} Sink		VECL0−1.2			V
V_{OL}	Output Low Voltage	VTTL0, 1 = 4.5V	TTL Outputs, I_{OL} = 8 mA				0.5	V
			MOS Outputs	I_{OL} = +100 μA			0.4	
				I_{OL} = 20 mA			0.5	
		VECL0, 1 = 0V VEE = −4.2V	ECL Outputs, 50Ω Load to −2V		−1880		−1490	mV
			OPAMP Output, I_{OL} = −1.25 × I_{CPO} Source				VEE+0.5	V
I_I	Max High Level Input Current	VTTL0, 1 = 5.5V, TTL Inputs, V_{IN} = 7V					100	μA
I_{IH}	High Level Input Current	VTTL0, 1 = 5.5V, TTL Inputs, V_{IN} = 2.7V					20	μA
I_{IL}	Low Level Input Current	VTTL0, 1 = 5.5V, TTL Inputs, V_{IN} = 0.4V					−200	μA
I_O	Output Drive Current	VTTL0, 1 = 5.5V	TTL Outputs, V_O = 2.25V		−30		−110	mA
			MOS Outputs, V_O = 2.25V			−135		mA
I_{CPO}	Charge Pump Current	VEE = −4.2V to −5.7V VECL0, 1 = 0V		Source	−0.2	−0.5	−1.0	mA
				Sink	0.2	0.5	1.0	mA
				TRI-STATE®	−10	0	10	μA
I_{CC}	Supply Current	VTTL0, 1 = 5.5V		TTL Supply		30	40	mA
		VECL0, 1 = 0V	VEE = −5.7V, 10k ECL Supply Range			150	210	
			VEE = −4.8V, 100k ECL Supply Range			135	185	

Note 1: TTL inputs—ENIN1, 2, 3, RGP HORIZ, EXT REF, S0, S1, S2
TTL outputs—ENOUT1, 2, SOUT, LCLK0, 1, 2
MOS outputs—PHI1, PHI2
ECL outputs—ENOUT3, $\overline{\text{ENOUT3}}$, PCLK, $\overline{\text{PCLK}}$, LCLK3, $\overline{\text{LCLK3}}$

AC Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
F_{MAX}	Max VCO Freq (Note 2)	Self Osc		235			MHz
		Ext. Drive		235			
	Max XTL Freq			25	35		MHz
DC	Duty Cycle PHI1, 2	FXTL = 20 MHz		45	55		%
T_{EO1}	LCLK0 to ENOUT1			−7	−2	5	ns
T_{EO2}	LCLK0 to ENOUT2			−7	−2	5	ns
T_{EO3}	LCLK0 to ENOUT3			−15	−7	0	ns
T_{PCLK}	LCLK3, ENOUT3 to PCLK		Tadj = HI (VECL0)	0	2.5	5.0	ns
			Tadj = LOW (VEE)	−2.5	0	2.5	ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{LCLK1}	LCLK0 to LCLK1		−5	0	5	ns
T_{LCLK2}	LCLK0 to LCLK2		−5	0	5	ns
T_{LCLK3}	LCLK0 to LCLK3		−15	−7	0	ns
T_{PHI1}	LCLK0 to PHI1 ⌐			−5		ns
T_{SOUT}	LCLK0 to SOUT ⌐	f_{XTL} = 20 MHz, S = 8		0		ns
$T_{SO-PHI1}$	SOUT to PHI1 ⌐	Smod = 1 thru 8	−15	−5	5	ns
TNO	Nonoverlap Time PHI1 to PHI2	C_L = 50 pF		0		ns
T_R, T_F	Rise, Fall Time PHI1, 2	(Note 1)		4		ns

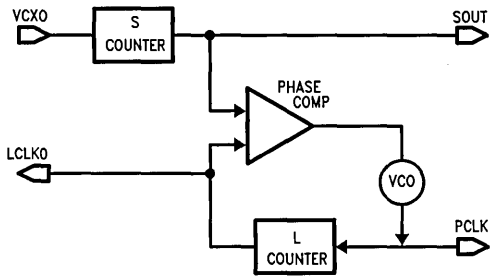
Note 1: Rise, Fall times measured from 0.5V to VTTL − 2V with C_L = 50 pF.

Note 2: F_{MAX} is not production tested but is assured by characterization to include sufficient margin beyond processing extremes.

Circuit Operation

The heart of the DP8512 Video Clock Generator is a crystal oscillator which is used as a frequency reference to generate several clock signals required in a video display system. Among the clocks generated are the two-phase clock for driving the RGP and BPU processors, ECL pixel and load clocks (PCLK and LCLK3) for high speed video shift register parallel load and shift operations, and TTL load clocks (LCLK0, LCLK1, and LCLK2) for moving DRAM and FIFO data to the video shift registers. The LCLK and PCLK outputs are all internally synchronized in order to simplify system timing.

The two-phase graphics processor clock (PHI1 and PHI2) operates at the frequency of the crystal oscillator. It is capable of directly driving the raster graphics and BIT-BLT processors. The two-phase clock is closely aligned with the other clocks generated by the device to maximize system operation. The PCLK and LCLK outputs are generated using a digital phase locked loop as shown in *Figure 1*.



TL/F/8758–10

FIGURE 1. PLL Block Diagram

The loop consists of the S and L counters, a phase comparator, and a voltage controlled oscillator (VCO) with the relationship between these elements in the loop defined as:

$$PCLK = \frac{VCXO \times L}{S}$$

where PCLK is the pixel clock frequency, L is the L Counter modulus, and S is the S Counter modulus. When the frequency of the VCO (PCLK) in the phase locked loop is stable the inputs to the phase detector are in phase, thus the S Counter and L Counter outputs are identical in both phase and frequency. The crystal oscillator ensures that the phase and frequency of the S Counter output remains constant. Any drift, or change in frequency, of the VCO will be divided down and appear as a shift in phase at the L Counter output. The phase detector will sense this phase error and generate a correction voltage for the VCO input which is proportional to the magnitude of the frequency error. This correction voltage will change the VCO frequency to eliminate the error thus keeping the loop locked. The correction voltage adjusts the VCO's frequency by changing the capacitance of the varactor in the LC oscillator tank circuit. The varactor's capacitance is proportional to the amount of reverse bias applied across it. The VCO correction voltage is provided from the OP AMP output which is a 3V typical operating range (VEE + 0.5V to VELC0 −1.2V). This operating range provides typically a ±10% VCO frequency tuning range. This operating range limits the device from being used at multiple pixel rates unless an external op amp is added to extend the tuning voltage range or tank circuit components are bandswitched in.

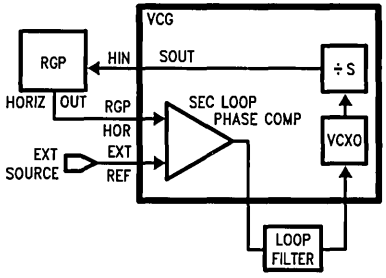
The presence of the S Counter in the loop enables the graphics processor to operate at full speed independent of PCLK frequency. The video shift register's parallel data width determines the L Counter modulus. An 8-bit parallel shift register would use an L Counter modulus of 8 so that a parallel load pulse occurs once every 8 pixel clocks. The L Counter output is used to derive the four LCLK outputs. These 4 LCLKs differ slightly in format to allow for the various system configurations highlighted in the following section.

Circuit Operation (Continued)

The ECL LCLK3 output is used in conjunction with the PCLK output to load data into a high-speed video shift register. The PCLK provides the clock and LCLK3 provides the load signal for the shift register. With a typical video shift register operating at frequencies around 200 MHz timing can become extremely critical. For this reason a Timing Adjust pin (Tadj) is provided that will allow the user to obtain the optimum LCLK3-to-PCLK setup and hold timing relationship.

The other three LCLK outputs (LCLK0, LCLK1, LCLK2) are TTL outputs. They can be used to control a selection of different DRAMs/video shift register configurations as shown in the system architecture section which follows.

Also included on the chip is a secondary phase locked loop which can be used to synchronize the graphics system to an external signal such as the horizontal sync pulse from a television broadcast. A block level diagram of this mode of operation is shown in *Figure 2*. The crystal oscillator is configured to operate as a voltage controlled crystal oscillator (VCXO). Any change in frequency of the VCXO forces the outputs of the S Counter and the RGP's horizontal counter to shift in phase relative to the external horizontal reference signal. The auxiliary phase comparator senses any phase differences between its two inputs and produces a correction voltage back to the VCXO which is proportional to the amount of the frequency error. This correction voltage will change the VCXO frequency to eliminate the error thus keeping the loop locked.



TL/F/8758–11

FIGURE 2

For most applications the crystal oscillator will be in the range of 20 MHz. With a typical 8-bit system this means that the PCLK output will be running at 20 MHz × 8 bits = 160 MHz. However, if the system is 16 bits wide instead of 8 bits the PCLK frequency would become 20 MHz × 16 bits = 320 MHz which is beyond the range of the VCO. Therefore the S Counter block must be added to divide the crystal oscillator frequency down to a more manageable frequency. Using the equation and the above example of a 20 MHz crystal oscillator with 16 bits of data, the S Counter is used as a divide-by-two counter to get a PCLK frequency of 160 MHz.

The S Counter can be programmed to divide by any integer up to 8 and the L Counter can be programmed for any word width from 4 bits to 64 bits in increments of 4. Table I shows some of the frequencies possible using various values for the S- and L-modulus.

VARIOUS SYSTEM ARCHITECTURES

Figure 3 demonstrates the DP8512 in a system using a video shift register and a DRAM. Another possible application uses a video DRAM, or VDRAM, in place of the DRAM, as shown in *Figure 4*. This system differs from *Figure 3* in that the VDRAM contains an internal shift register which allows memory to be randomly accessed while data is being output to the video shift registers through the serial port. The output of the VDRAM differs from the standard DRAM in that data is not valid at the output of the internal shift register until an SCLK pulse is provided. The offset in the LCLK3 waveform from LCLK1 is obtained by connecting ENOUT1 to ENIN3.

The third type of system employs a video shift register (such as the DP8515) that contains an onboard FIFO as shown in *Figure 5*. This architecture simplifies timing requirements in a high-speed multiboard system. The propagation delay time from the DRAM to the video shift register through the back plane is no longer restricted to be less than the clock frequency of the system. The VDRAM can be writing into the FIFO asynchronous to the data being loaded into the shift register. As in the previous systems, one LCLK1 pulse transfers the data to the VDRAM output. LCLK2 then writes several words into the FIFO prior to LCLK3 reading out the first word. The connections required to obtain this timing are shown in the diagram.

TABLE I. Partial Table of PCLK Frequencies

S MOD	8-Bit Word (L = 8)		16-Bit Word (L = 16)		32-Bit Word (L = 32)	
	PCLK Frequency		PCLK Frequency		PCLK Frequency	
	XTL = 10 MHz	XTL = 20 MHz	XTL = 10 MHz	XTL = 20 MHz	XTL = 10 MHz	XTL = 20 MHz
1	80.0 MHz	160.0 MHz	160.0 MHz	na	na	na
2	40.0	80.0	80.0	160.0 MHz	160.0 MHz	na
3	26.7	53.3	53.3	106.7	106.7	na
4	20.0	40.0	40.0	80.0	80.0	160.0 MHz
5	16.0	32.0	32.0	64.0	64.0	128.0
6	13.3	26.7	26.7	53.3	53.3	106.7
7	11.4	22.9	22.9	45.7	45.7	91.4
8	10.0	20.0	20.0	40.0	40.0	80.0

Circuit Operation (Continued)

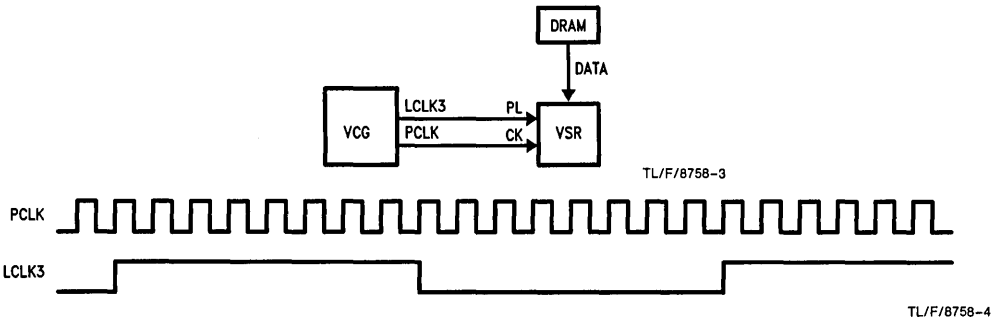


FIGURE 3. System Configuration and LCLK Waveforms using DRAM

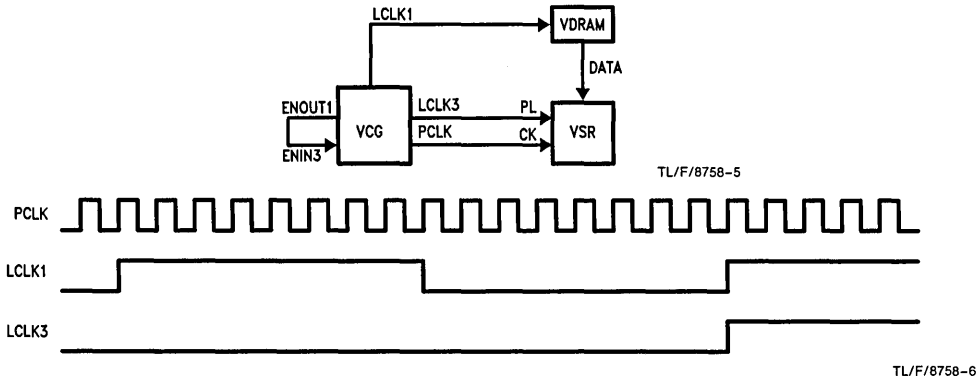


FIGURE 4. System Configuration and LCLK Waveforms using VDRAM

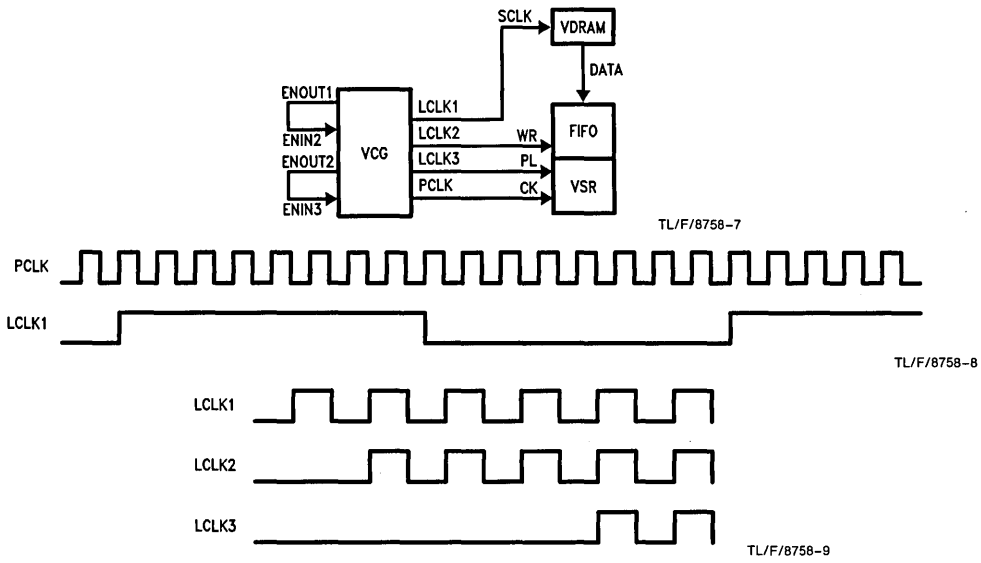
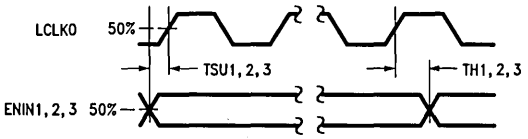


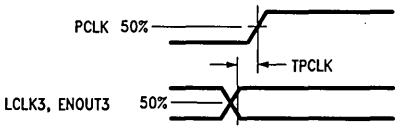
FIGURE 5. System Configuration and LCLK Waveforms using a VSR Containing FIFO

AC Timing Waveforms

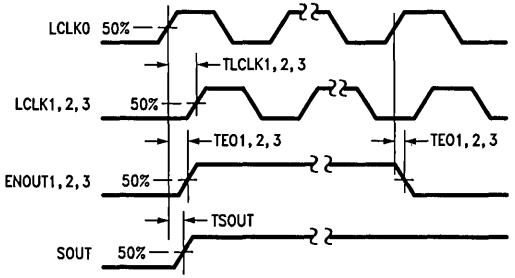
TSETUP, THOLD



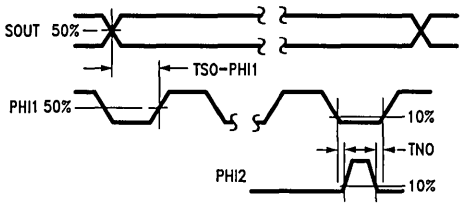
TL/F/8758–12



TL/F/8758–13

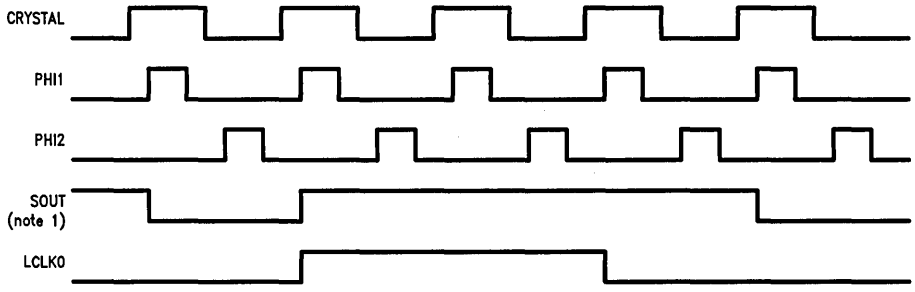


TL/F/8758–14



TL/F/8758–15

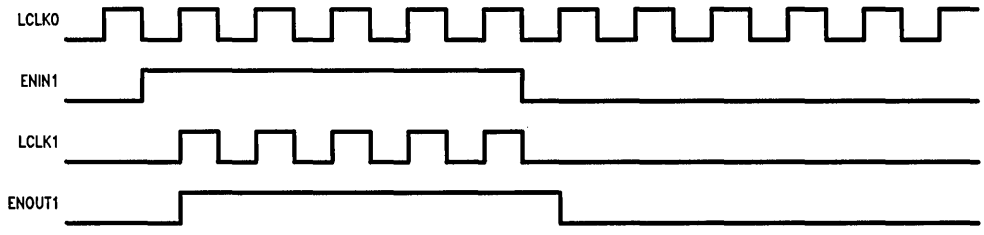
DP8512 Functional Waveforms



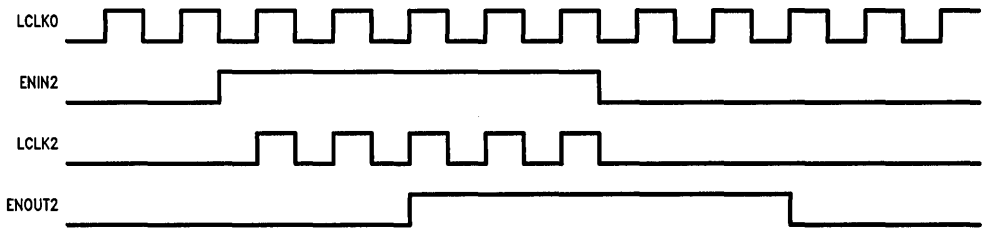
TL/F/8758–16

Note 1: SOUT waveform displayed with S Counter in divide-by-4 mode.

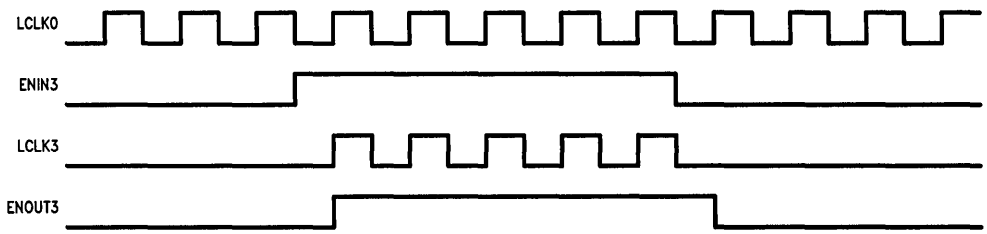
Load Clock Timing Diagram



TL/F/8758–17



TL/F/8758–18



TL/F/8758–19

Counter Modulus Tables

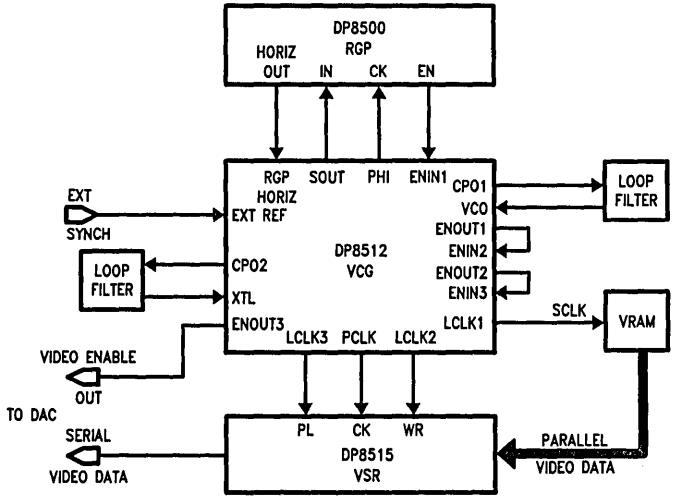
S MOD	S Counter Inputs		
	S2	S1	S0
1	L	L	L
2	L	L	H
3	L	H	L
4	L	H	H
5	H	L	L
6	H	L	H
7	H	H	L
8	H	H	H

L = TTL Logic Low Level
H = TTL Logic High Level

L MOD	L Counter Inputs			
	L3	L2	L1	L0
4	0	0	0	0
8	0	0	0	1
12	0	0	1	0
16	0	0	1	1
20	0	1	0	0
24	0	1	0	1
28	0	1	1	0
32	0	1	1	1
36	1	0	0	0
40	1	0	0	1
44	1	0	1	0
48	1	0	1	1
52	1	1	0	0
56	1	1	0	1
60	1	1	1	0
64	1	1	1	1

0 = VEE or open
1 = VECL0, 1

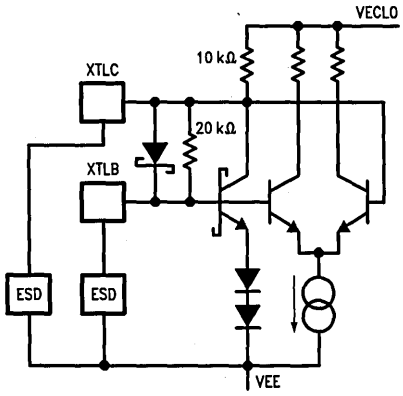
Typical System Diagram



TL/F/8758–20

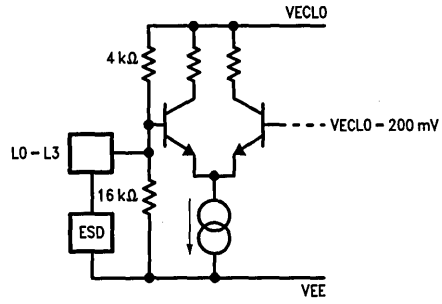
Input Schematics (Note 1)

VCXO Inputs



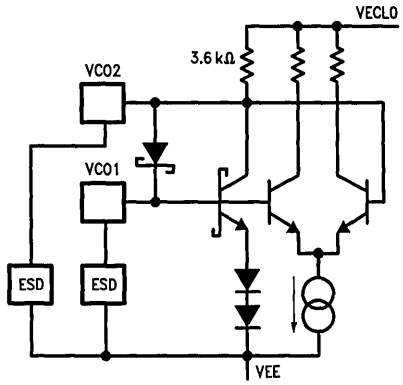
TL/F/8758–21

L0–L3 Inputs



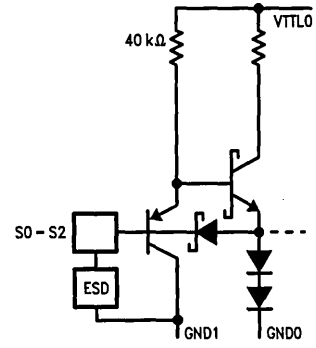
TL/F/8758–22

VCO Inputs



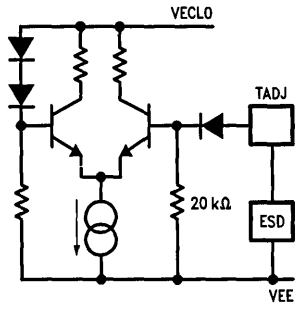
TL/F/8758–23

S Counter Inputs (TTL)



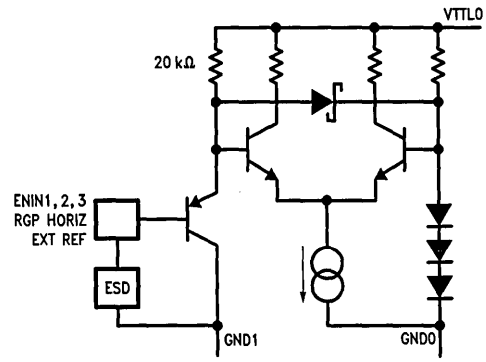
TL/F/8758–24

Timing Adjust Input



TL/F/8758–25

TTL Inputs

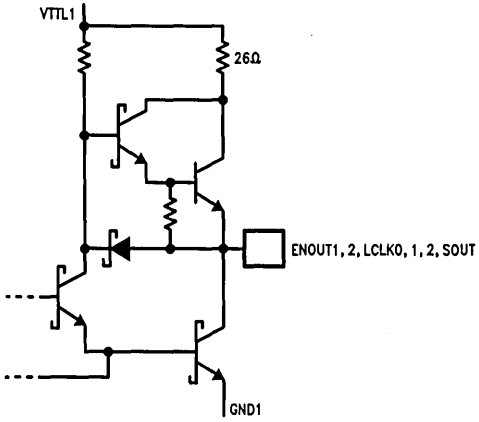


TL/F/8758–26

Note 1: Refer to the typical ESD circuit for all schematics.

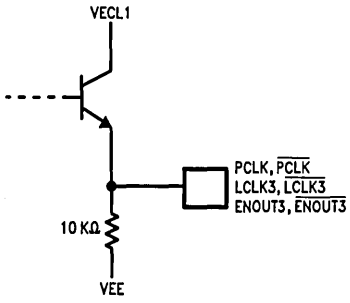
Output Schematics

TTL Outputs



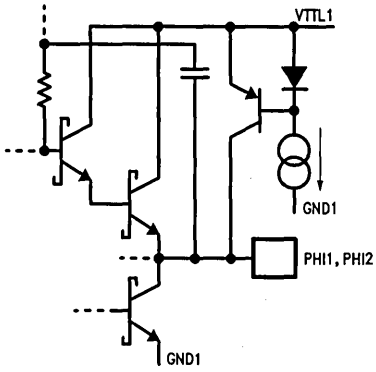
TL/F/8758-27

ECL Outputs



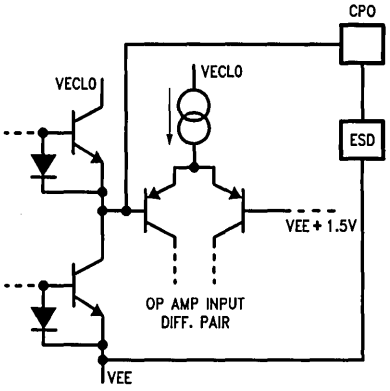
TL/F/8758-28

PHI1, PHI2 Outputs



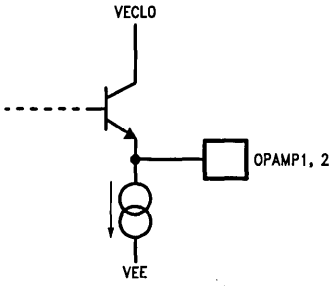
TL/F/8758-29

Charge Pump Output/Op Amp Input



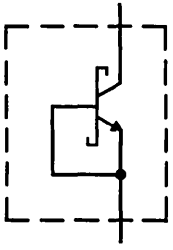
TL/F/8758-30

Op Amp Output



TL/F/8758-31

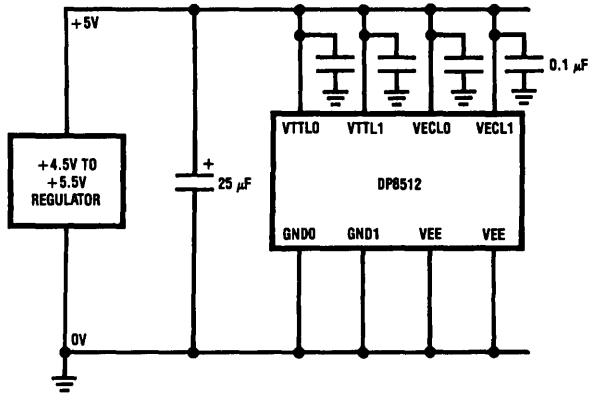
Typical ESD Circuit



TL/F/8758-33

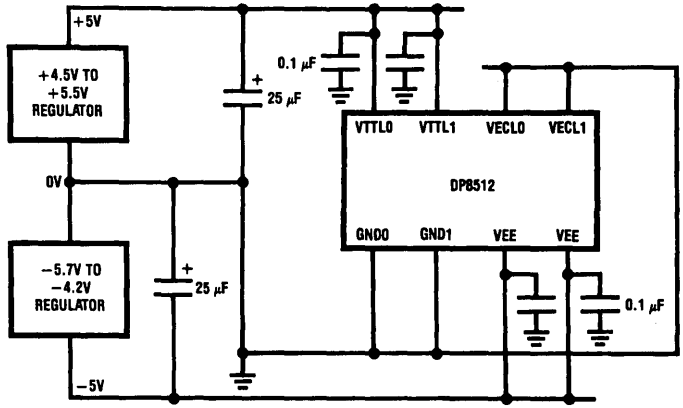
Typical Supply Wiring

Single Power Supply Operation



TL/F/8758–34

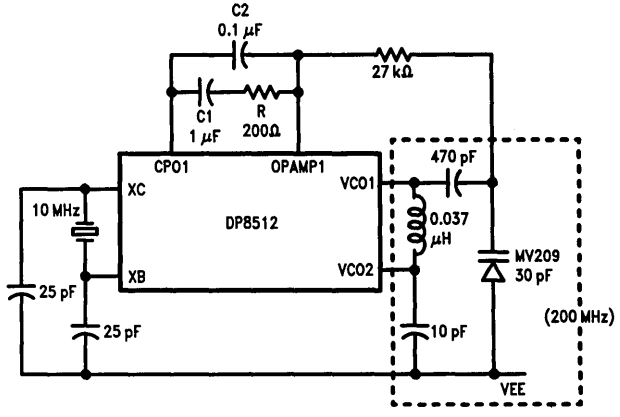
Dual Power Supply Operation



TL/F/8758–35

Typical Applications

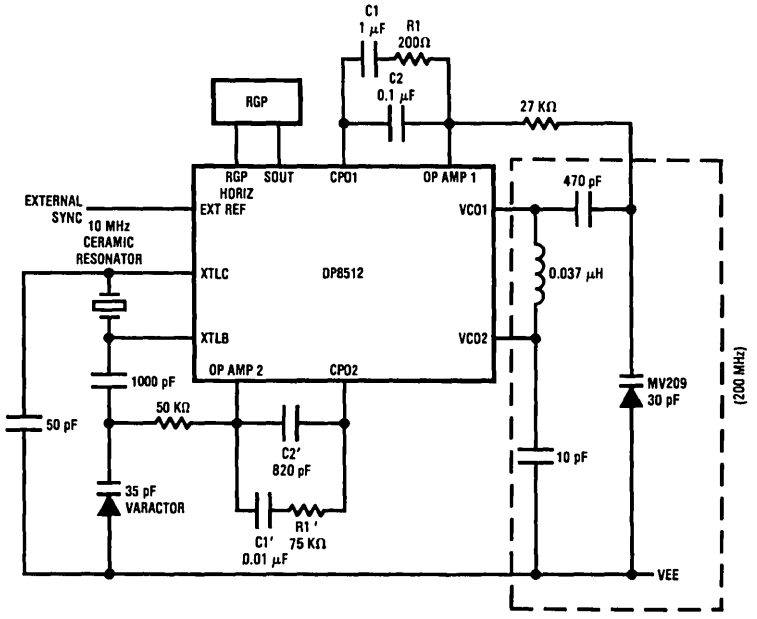
Crystal Reference System



TL/F/8758–32

Typical Applications (Continued)

External Reference System



TL/F/8758–36

Loop Filter Calculations

Several constants need to be known in order to determine the loop filter components. They are the loop divide ratio N, the phase detector gain K_p, the VCO gain K_o, the loop bandwidth ω_o and phase margin ϕ.

The constant K_p is fixed at 80 μA/rad for the DP8513. N is simply the L counter modulus for the main loop. For the secondary loop, N is the S counter modulus times any external division between the SOUT pin and the RGP HORIZ pin. (i.e., if S = 1 and there is a ÷100 counter between SOUT and RGP HORIZ, N = 1 × 100 = 100.) A 60° phase margin is recommended, however, the equations allow other values to be used if desired.

The oscillator gain constant of K_o can be obtained from Table III or determined experimentally. This is done by driving the 27k resistor which normally connects the varactor to the op amp output with an external power supply. Set the supply to V_{EE} + 3V and note the PCLK frequency. Next set the supply to V_{EE} + 2V and note the frequency again. The difference in these two frequencies (times 2π to convert to radians) is K_o. For optimum performance, the desired PCLK frequency should be somewhere between the two frequencies measured above. This may require adjustment of the coil.

Before choosing a value of ω_o, one fact should be pointed out. The 27k resistor and the 500 pF coupling capacitor between the coil and the varactor form a low pass filter with a cutoff of about 12 kHz. Thus, the loop bandwidth must be chosen to be less than this value. We recommend $2\pi \times$ 100 Hz to $2\pi \times 3$ kHz for ω_o.

Having found all these constants, the following equations are used to find the component values:

$$R1 = \frac{1.08\, N\, \omega_o}{K_p\, K_o} \qquad C1 = \frac{3.46\, K_p\, K_o}{N\, \omega_o^2} \qquad C2 = \frac{0.27\, K_p\, K_o}{N\, \omega_o^2}$$

To use a phase margin of other than 60°, use the following:

$$R1 = \frac{N\, \omega_o}{2\, K_p\, K_o}(\text{cosec}\, \phi + 1)$$

$$C1 = \frac{2\, K_p\, K_o}{N\, \omega_o^2} \tan \phi$$

$$C2 = \frac{K_p\, K_o}{N\, \omega_o^2}(\sec \phi - \tan \phi)$$

Example: Design a system with the following characteristics:

External horizontal sync of 100 kHz
1560 pixels per line (2000 pixels including retrace)
20 bit wide video data
10 MHz processor rate

Note that this system will sync to an external source so that both loops must be used.

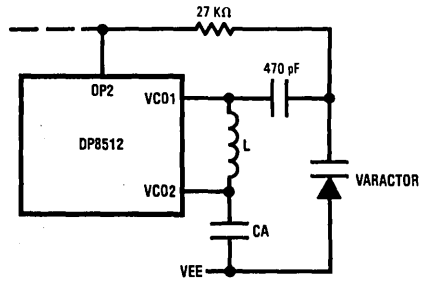
The PCLK frequency will be 100 kHz × 2000 pixels per line = 200 MHz. The components in Table III will be used. Note that K_o = 24 Mrad. Because it is a 20 bit wide system the L counter modulus must be 20.

By choosing $\omega_o = 2\pi * 2800$ Hz, the equations give R1 = 200Ω, C1 = 1.0 μF and C2 = 0.08 μF (use C2 = 0.1 μF).

In the secondary loop, a ceramic resonator is used in place of a crystal to allow more pullability. Its K_o is found experimentally to be 84 krads/V. The SOUT frequency will be the same as LCLK0 or 200 MHz ÷ 20 = 10 Mhz. Thus, there must be a ÷100 counter between SOUT and RGP HORIZ so N = 100 for the secondary loop.

In choosing ω_o, it should be noted that ω_o for the secondary loop should be smaller than ω_o for the primary loop so that the main loop will be able to track the secondary without losing lock. Picking $\omega_o = 2\pi \times 750$ Hz gives R1′ = 75k, C1′ = 0.01 μF and C2′ = 820 pF.

Recommended VCO Components



TL/F/8758–37

$$F_{VCO} = \frac{1}{2\pi\sqrt{LC_{TOT}}} \qquad C_{TOT} = \frac{1}{\frac{1}{CA} + \frac{1}{C_{VARACTOR}}}$$

TABLE III. Recommended VCO Components

Frequency (MHz)	L μH	TOKO Part #	CA pF	Cvaractor		Ko Mrad/V
				pF	Motorola #	
60	0.258	E 502HNS-6000026	56	30	MV209	16
80	0.17	E 502HNS-4000024	39	30	MV209	19
100	0.12	E 502HNS-3000023	30	30	MV209	21
120	0.07	E 502HNS-2000022	39	30	MV209	31
140	0.07	E 502HNS-2000022	22	30	MV209	27
160	0.07	E 502HNS-2000022	15	15	MV2205	27
180	0.07	E 502HNS-2000022	10	15	MV2205	26
200	0.037	E 502HNS-1000029	10	30	MV209	24
220	0.037	E 502HNS-1000029	10	15	MV2205	34

National Semiconductor

DP8513 Multi-Board Video Clock Generator

General Description

The DP8513 is a clock generator intended for use in medium- to high-performance CRT graphics systems. The device simplifies timing and minimizes phase skew between the various signals involved in the transfer of DRAM (or VDRAM) data into a DAC for display on a CRT. The DP8513 is used in conjunction with the DP8514 Crystal Clock Generator to simplify synchronization problems in multiboard systems. The device generates several synchronous clocks from a reference input using digital phase locked loop (PLL) techniques. These synchronous clocks include a graphics processor clock, a raster-scan pixel clock, and various gated TTL and ECL clocks required to transfer data from VRAM to video shift registers. Circuitry is also provided which enables the user to phase lock his graphics system to an external video source.

In a multiboard system the REFIN and REFCLK inputs enable the motherboard and the slave boards to be synchronously driven from a single master clock source such as the DP8514.

The graphics processor clocks (PHI1 and PHI2) are non-overlapping two-phase clocks with MOS-compatible outputs capable of driving 100 pF loads at up to a 20 MHz rate.

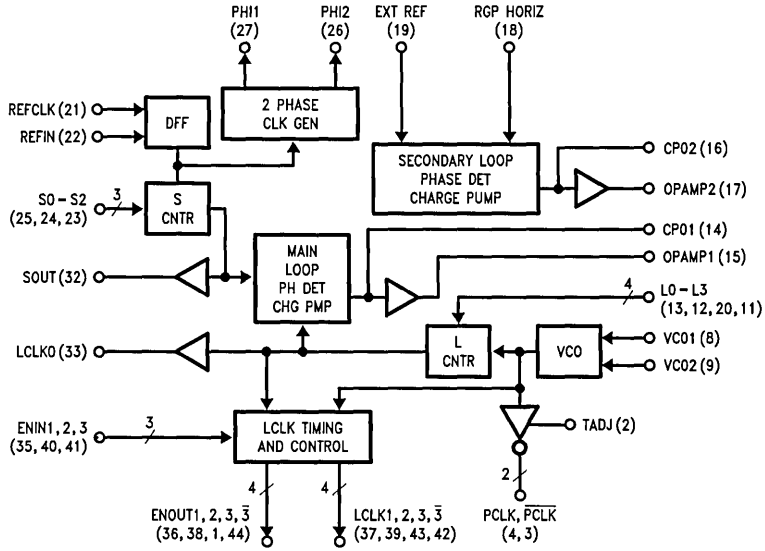
The raster-scan pixel clock (PCLK) and the parallel load clock (LCLK3) required for video shift register operation are generated from the REFIN and REFCLK inputs using two programmable counters in a phase locked loop configuration. Video word widths from 4 to 64 bits in increments of 4 are accommodated by these counters. The ECL-compatible PCLK outputs are capable of operating at up to 225 MHz from either a positive or a negative supply voltage.

Two gated TTL clock outputs (LCLK1 and LCLK2) are also provided to enable easy transfer of data from a VRAM serial shift register directly into a video shift register or indirectly through a FIFO.

Features

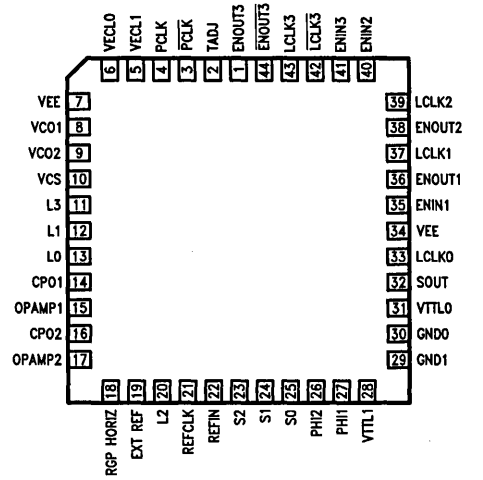
- Phase-locked-loop generates synchronized system clock, PCLK, and LCLK
- MOS-compatible single-phase or non-overlapping two-phase system clock output
- 225 MHz ECL differential output pixel clock (PCLK)
- Gated and non-gated load clock (LCLK) outputs ease VRAM-to-VSR synchronization
- Accommodates video word widths from 4 to 64 bits in increments of 4
- Timing Adjust pin (TADJ) provides a fixed offset adjustment of PCLK to LCLK to ease system design
- ECL circuitry can be referenced to positive or negative power supply
- Enables horizontal synchronization from an external source

Block Diagram (numbers in parentheses indicate pin numbers)



TL/F/9283–1

Connection Diagram



TL/F/9283–2

Order Number DP8513V
See NS Package Number V44A

Pin Descriptions

1, 44 **ENOUT3, $\overline{\text{ENOUT3}}$:** Differential ECL video enable outputs synchronous to LCLK0 and gated by ENIN3 (10k and 100k ECL compatible). Require conventional ECL 50Ω termination.

2 **TADJ:** Timing Adjust pin allows the PCLK output transition to occur 2.5 ns earlier than LCLK3 and ENOUT3 when taken to a high logic level. This allows the set-up and hold times of various Video Shift Registers to be accommodated. A logic high is VECL0, and a logic low is VEE.

3, 4 **$\overline{\text{PCLK}}$, PCLK:** Differential ECL pixel clock outputs driven by the VCO in the main loop (10k and 100k ECL compatible). Require conventional ECL 50Ω termination.

5 **VECL1:** ECL output buffer positive power supply.

6 **VECL0:** ECL internal logic positive power supply.

Note: VECL0 and VECL1 can be operated from 0V to +5.7V relative to GND.

7, 34 **VEE:** ECL negative power supply.

8, 9 **VCO1, VC02:** External tank circuit connections for the Pierce VCO. See typical applications for typical wiring.

10 **VCS:** No connection required.

11, 12, 13, 20 **L3, L1, L0, L2:** A four bit word input used to select the L Counter modulus. Any modulus from 4 to 64 may be selected in increments of 4. L0 is the least significant bit. High = VECL0, Low = VEE. These pins should be bypassed to VECL0 with 0.01 μF caps. These traces should not be allowed to cross any signal traces.

14 **CPO1:** Main loop charge pump output. Used in conjunction with OPAMP1 to form the external loop filter.

15 **OPAMP1:** Op amp output of the main loop. This output is used to control the pixel clock frequency via the varactor diodes in the LC tank circuit.

16 **CPO2:** Charge pump output of the secondary loop. Used in conjunction with OPAMP2 to form the external loop filter when synchronization to an external video source is desired.

17 **OPAMP2:** Op amp output of the secondary loop. This output is used to vary the crystal frequency (VCXO) in systems where it is desired to lock to an external video source.

18 **RGP HORIZ:** TTL compatible secondary loop phase comparator input. This signal completes the feedback path from the VCXO by way of the DP8500 Raster Graphics Processor's Horizontal Output. The falling edge triggers the secondary phase detector.

19 **EXT REF:** TTL compatible external horizontal reference input. This is the optional horizontal input for systems where it is desired to lock to an external video source. The falling edge triggers the secondary phase detector.

21, 22 **REFCLK, REFIN:** Reference source inputs from which all output clocks are generated. See the typical applications for typical wiring.

23, 24, 25 **S2, S1, S0:** TTL compatible three bit word that determines the S Counter modulus. S0 is the least significant bit.

Pin Descriptions (Continued)

26, 27 **PHI2, PHI1:** MOS compatible two-phase non-overlapping clocks. The frequency of these clocks is that of the REFIN input. Use of these outputs to drive large capacitive loads requires the use of high frequency bypass caps across VTTL1 and GND1 as close to the part as possible.

28 **VTTL1:** TTL output buffer supply. Specified for 5V ±10% operation.

29 **GND1:** TTL output buffer supply return.

30 **GND0:** TTL internal logic power supply return.

31 **VTTL0:** TTL internal logic positive power supply. Specified for 5V ±10% operation.

32 **SOUT:** TTL compatible ungated output of the S Counter. It is also connected to one of the inputs of the main loop phase comparator.

33 **LCLK0:** TTL compatible free-running Load Clock. This signal is also connected to an input of the main loop phase comparator.

35 **ENIN1:** TTL compatible video enable input. A high on this input starts LCLK1 on the next positive transition of LCLK0.

36 **ENOUT1:** TTL compatible video enable output synchronous to LCLK0 and gated by ENIN1.

37 **LCLK1:** TTL compatible load clock equivalent to LCLK0 but gated by ENIN1.

38 **ENOUT2:** TTL compatible video enable output synchronous to LCLK0 and gated on the third positive transition of LCLK0 following a valid ENIN2 input.

39 **LCLK2:** TTL compatible load clock equivalent to LCLK0 but gated by ENIN2.

40 **ENIN2:** TTL compatible video enable input. A high on this input starts LCLK2 on the next positive transition of LCLK0.

41 **ENIN3:** TTL compatible video enable input. A high on this input starts LCLK3 on the next positive transition of LCLK0.

42, 43 **$\overline{\text{LCLK3}}$ LCLK3:** Differential ECL compatible load clock synchronous to LCLK0 and gated by ENIN3 (10k and 100k ECL compatible). Require conventional ECL 50Ω termination.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
TTL Signals	
Inputs	7.0V
Outputs	7.0V
ECL Signals	
Output Current	−50.0 mA
Supply	
VEE to GND	−7V to 0.5V
VECL to GND	−0.5V to 7V
VTTL to GND	−0.5V to 7V
ESD susceptibility (see Note 5)	1000V

Recommended Operating Conditions (Notes 1, 2, 3, 4)

Symbol	Parameter	Min	Typ	Max	Units
VTTL0, 1 to GND	TTL Power Supply	4.5		5.5	V
VECL0, 1 to VEE	ECL Power Supply	4.2		5.7	V
VEE to GND		−5.7		0	V
V_{IH}	High Level Input Voltage TTL Inputs	2			V
V_{IL}	Low Level Input Voltage TTL Inputs			0.8	V
I_{OH}	High Level Output Current TTL Outputs			−0.4	mA
	High Level Output Current MOS Compatible Outputs			−0.4	mA
I_{OL}	Low Level Output Current TTL Outputs			8	mA
	Low Level Output Current MOS Compatible Outputs			20	mA
FPCLK (Note 6)	Pixel Clock Max Frequency			225	MHz
Fin MAX	REFCLK Frequency, REFIN = fREFCLK/2			50	MHz
T_{su1}	Setup Time ENIN1 to LCLK0	20	11		ns
T_{su2}	Setup Time ENIN2 to LCLK0	20	11		ns
T_{su3}	Setup Time ENIN3 to LCLK0	20	11		ns
T_{su4}	Setup Time REFIN to REFCLK$_\!\!\nearrow$	5			ns
T_{h1}	Hold Time LCLK0 to ENIN1	0	−9		ns
T_{h2}	Hold Time LCLK0 to ENIN2	0	−9		ns
T_{h3}	Hold Time LCLK0 to ENIN3	0	−9		ns
T_{h4}	Hold Time REFCLK $\_\!\!\nearrow$ to REFIN	2			ns
Tambient	Operating Temp. Range	0		70	°C

Note 1: See Timing Waveforms for relevant signal edges (positive or negative) from which all setup and hold times measurements are made.

Note 2: TTL inputs; ENIN1, 2, 3, RGP HORIZ, EXT REF, S0, S1, S2, REFIN, REFCLK

Note 3: TTL outputs; SOUT, LCLK0, 1, 2, ENOUT1, 2.
MOS outputs; PHI1, 2

Note 4: Inputs L0, L1, L2, L3, and TADJ designed to be tied to VECL for high level or shorted to VEE (or left open) for low level. See input schematics.

Note 5: Human body model; 120 pF thru 1.5 kΩ.

Note 6: Maximum frequency that PCLK can reliably be "locked". The VCO range should be controlled to avoid exceeding 235 MHz with the maximum control voltage applied to the VCO.

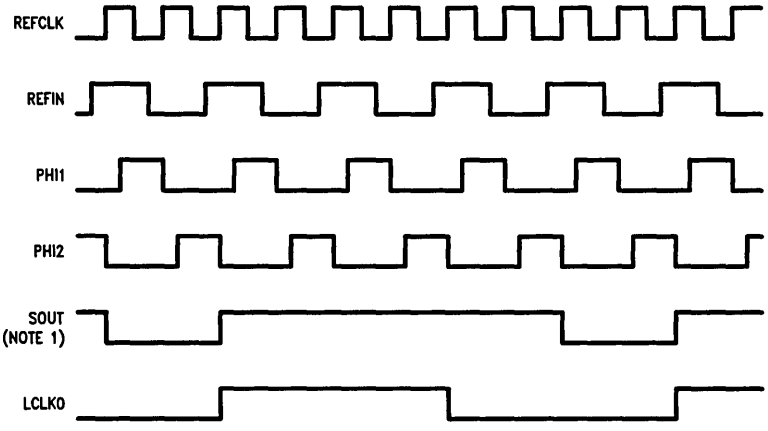
DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	VTTLO, I = 4.5V, Iin = −18 mA					−1.5	V
V_{OH}	Output High Voltage	VTTLO, I = 4.5V to 5.5V	TTL Outputs, I_{OH} = −400 μA		VTTL−2			V
			MOS Outputs	I_{OH} = −100 μA	VTTL−0.4			
				I_{OH} = −400 mA	VTTL−2.3			
		VECL0, I = 0V VEE = −4.2V	ECL Outputs, 50Ω load to −2V		−1045		−880	mV
			OPAMP Output, I_{OH} = −1.25 ICPO Sink		VECL0−1.2			V
V_{OL}	Output Low Voltage	VTTL0, I = 4.5V	TTL Outputs, I_{OL} = 8 mA				0.5	V
			MOS Outputs	I_{OL} = 100 μA			0.4	
				I_{OL} = 20 mA			0.5	
		VECL0, I = 0V VEE = −4.2V	ECL Outputs, 50Ω Load to −2		−1880		−1490	mV
			OPAMP Output, I_{OL} = −1.25 ICPO Source				VEE+0.5	V
I_I	Max High Level Input Current	VTTL0, I = 5.5V, TTL Inputs, V_{in} = 7V					100	μA
I_{IH}	High Level Input Current	VTTL0, I = 5.5V, TTL Inputs, V_{in} = 2.7V					20	μA
I_{IL}	Low Level Input Current	VTTLO, I = 5.5V, TTL Inputs, V_{in} = 0.4V					−200	μA
I_O	Output Drive Current	VTTL0, I = 5.5V	TTL Outputs, V_o = 2.25V		−30		−110	mA
			MOS Outputs, V_o = 2.25V			−135		mA
I_{CPO}	Charge Pump Current	VEE = −4.2V to −5.7V VECL0, I = 0V		Source	−0.2	−0.5	−1.0	mA
				Sink	0.2	0.5	1.0	mA
				TRI-STATE®	−10	0	10	μA
I_{CC}	Supply Current	VTTL0, I = 5.5V		TTL SUPPLY		30	40	mA
		VECL0, I = 0V	VEE = −5.7V, 10k ECL Supply			150	210	
			VEE = −4.8V, 100k ECL Supply			135	185	

Note 1: TTL Inputs; ENIN1, 2, 3 RGP HORIZ, EXT REF, S0, S1, S2, REFIN, REFCLK
TTL Outputs; ENOUT1, 2, 3, SOUT
MOS Outputs; PHI1, PHI2
ECL Outputs; ENOUT3, $\overline{\text{ENOUT3}}$, PCLK, $\overline{\text{PCLK}}$, LCLK3, $\overline{\text{LCLK3}}$

Functional Waveforms

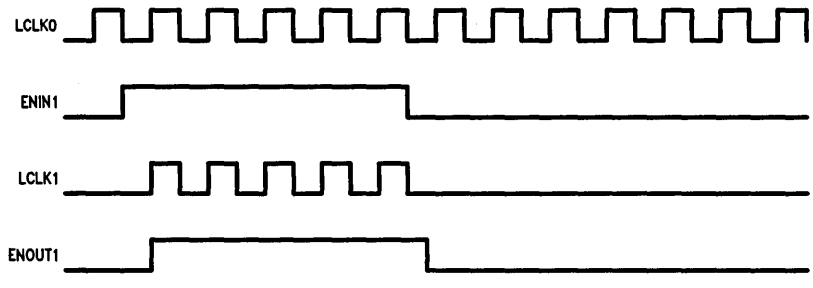
DP8513 Functional Waveforms



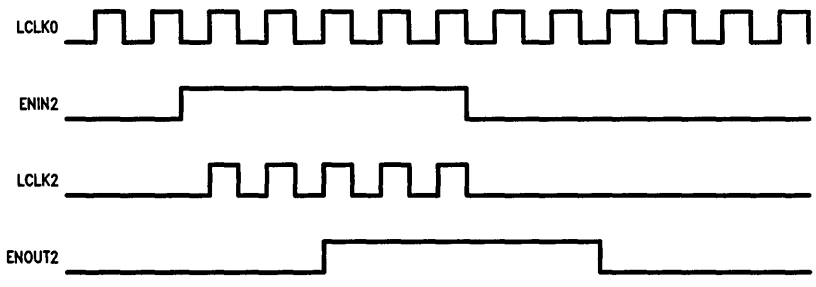
TL/F/9283–17

Note 1: SOUT waveform displayed with S Counter in divide-by-4 mode.

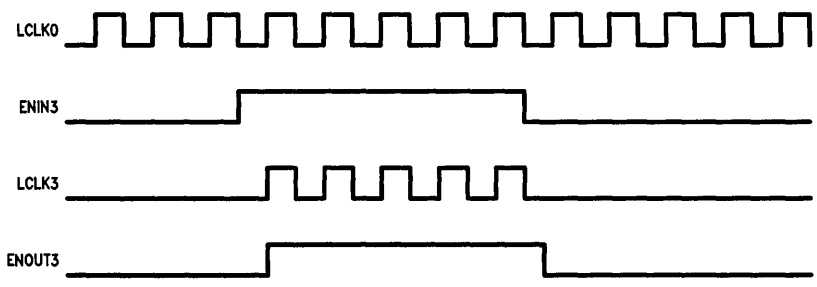
Load Clock Timing Diagram



TL/F/9283–18



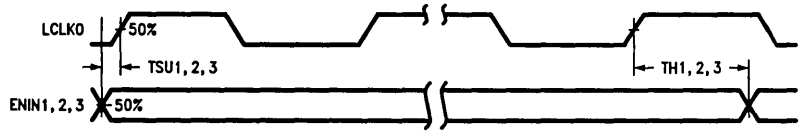
TL/F/9283–19



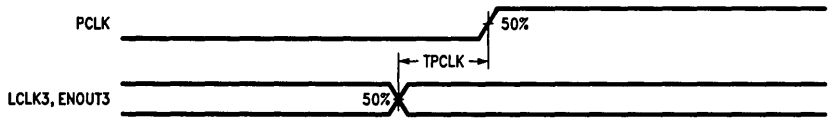
TL/F/9283–20

AC Timing Waveforms

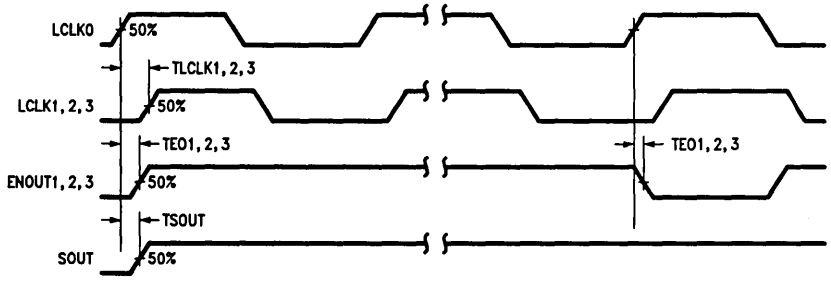
TSETUP, THOLD
LCLK0 to ENIN1, 2, 3



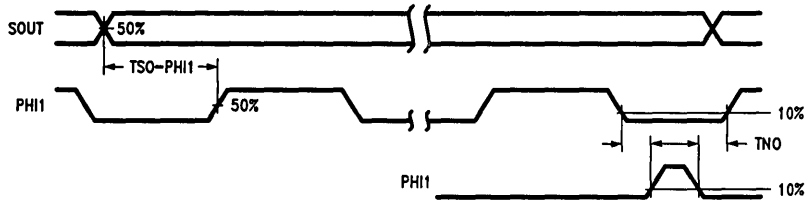
TL/F/9283–13



TL/F/9283–14



TL/F/9283–15



TL/F/9283–16

AC Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
FMAX	Max VCO Freq (Note 2)			235			MHz
FMAX	Max REFCLK Freq			50			MHz
PW	Pulse Width High PHI1, 2	REFCLK = 40 MHz, REFIN = 20 MHz		20	23	30	ns
T_{EO1}	LCLK0 to ENOUT1			−7	−2	5	ns
T_{EO2}	LCLK0 to ENOUT2			−7	−2	5	ns
T_{EO3}	LCLK0 to ENOUT3			−15	−7	0	ns
T_{PCLK}	LCLK3, ENOUT3 to PCLK		TADJ = HI (VECL0)	0	2.5	5.0	ns
			TADJ = LOW (VEE)	−2.5	0	+2.5	ns
T_{LCLK1}	LCLK0 to LCLK1			−5	0	5	ns
T_{LCLK2}	LCLK0 to LCLK2			−5	0	5	ns
T_{LCLK3}	LCLK0 to LCLK3			−15	−7	0	ns
T_{PHI1}	LCLK0 to PHI1↗	Loop Locked REFIN = 20 MHz S = 8			−5		ns
T_{SOUT}	LCLK0↗ to SOUT↗	Loop Locked REFIN = 20 MHz S = 8			0		ns
$T_{SO-PHI1}$	SOUT to PHI1↗			−15	−5	5	ns
TNO	Nonoverlap Time PHI1 to PHI2	C_L = 50 pF			0		ns
TR, TF	Rise, Fall Time PHI1, PHI2	(Note 1)			4		ns

Note 1: Rise and Fall times measured from 0.5V to VTTL1 − 2V with C_L = 50 pF

Note 2: This is not production tested but is assured by characterization to include sufficient margin beyond processing extremes.

Circuit Operation

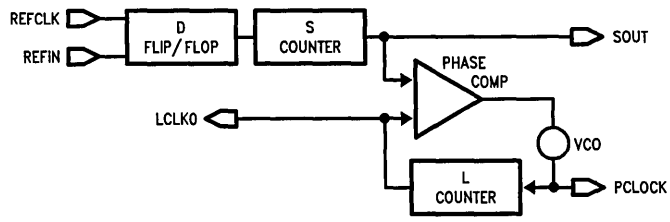
The DP8513 Video Clock Generator Slave generates several clock signals required in a video display system from two reference frequency inputs: REFCLK and REFIN. These signals are provided by the DP8514 Crystal Clock Generator. The 2X REFCLK input is used as a resynchronizing clock for the 1X REFIN input thus eliminating duty cycle distortion introduced by the backplane. Among the clocks generated are a two-phase clock for driving the RGP and BPU processors, ECL pixel and load clocks (PCLK and LCLK3) for high speed video shift register parallel load and shift operations, and TTL load clocks (LCLK0, LCLK1, and LCLK2) for moving DRAM and FIFO data to the video shift registers. The LCLK and PCLK outputs are all internally synchronized in order to simplify system timing.

The two-phase graphics processor clock (PHI1 and PHI2) operates at the frequency of the REFIN input. It is capable of directly driving the raster graphics and BIT-BLT processors. The two-phase clock is closely aligned with the other clocks generated by the device to maximize system operation. The PCLK and LCLK outputs are generated using a digital phase locked loop as shown in *Figure 1.*

The loop consists of the S and L counters, a phase comparator, and a voltage controlled oscillator (VCO) with the relationship between these elements in the loop defined as:

$$PCLK = \frac{REFIN \times L}{S}$$

where PCLK is the pixel clock frequency, REFIN is the REFIN frequency, L is the L Counter modulus, and S is the S Counter modulus. When the frequency of the VCO (PCLK) in the phase locked loop is stable the inputs to the phase detector are in phase, thus the S Counter and L Counter outputs are identical in both phase and frequency. As long as the REFCLK input is constant, the phase and frequency of the S Counter output remains constant. Any drift, or change in frequency, of the VCO will be divided down and appear as a shift in phase at the L Counter output. The



TL/F/9283–3

FIGURE 1. PLL Block Diagram

Circuit Operation (Continued)

phase detector will sense this phase error and generate a correction voltage for the VCO input which is proportional to the magnitude of the frequency error. This correction voltage will change the VCO frequency to eliminate the error and keep the loop locked by changing the capacitance of the varactor in the LC oscillator tank circuit. The varactor's capacitance is proportional to the amount of reverse bias applied across it. The correction voltage is provided by the OPAMP output which has a 3V typical operating range (VEE +0.5V to VECL0 −1.2V). This operating range provides a ±10% (typical) VCO frequency range. This restricts the use of multiple pixel rates. However, an external OPAMP can be added to extend the tuning voltage range or tank circuit components can be bandswitched in.

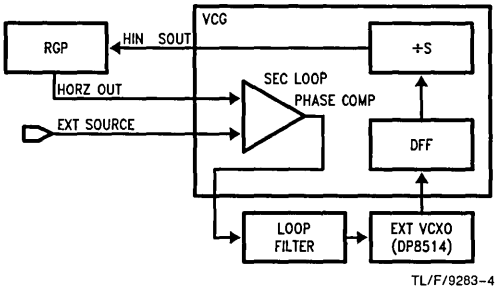
The presence of the S Counter in the loop enables the graphics processor to operate at full speed independent of PCLK frequency. The video shift register's parallel data width determines the L Counter modulus. An 8-bit parallel shift register would use an L Counter modulus of 8 so that a parallel load pulse occurs once every 8 pixel clocks. The L Counter output is used to derive the four LCLK outputs. These 4 LCLKs differ slightly in format to allow for the various system configurations highlighted in the following section.

The ECL LCLK3 output is used in conjunction with the PCLK output to load data into a high-speed video shift register. The PCLK provides the clock and LCLK3 provides the load signal for the shift register. With a typical video shift register operating at frequencies around 200 MHz timing can become extremely critical. For this reason a Timing Adjust pin (TADJ) is provided that will allow the user to obtain the optimum LCLK3-to-PCLK setup and hold timing relationship. See Pin Definitions for further info.

The other three LCLK outputs (LCLK0, LCLK1, LCLK2) are TTL outputs. They can be used to control a selection of different DRAMs/video shift register configurations as shown in the system architecture section which follows.

Also included on the chip is a secondary phase locked loop which can be used to synchronize the graphics system to an external signal such as the horizontal sync pulse from a television broadcast. A block level diagram of this mode of operation is shown in *Figure 2.* An external oscillator (such as the DP8514) is configured to operate as a voltage controlled crystal oscillator (VCXO). Any change in frequency of the VCXO forces the outputs of the S Counter and the RGP's horizontal counter to shift in phase relative to the external horizontal reference signal. The auxiliary phase comparator senses any phase difference between its two inputs and produces a correction voltage for the VCXO which is proportional to the amount of the frequency error.

This correction voltage will change the VCXO frequency to eliminate the error thus keeping the loop locked.



TL/F/9283–4

FIGURE 2

For most applications the REFIN input (and thus PHI1 and PHI2) will be in the range of 20 MHz. With a typical 8-bit system this means that the PCLK output will be running at 20 MHz × 8 bits = 160 MHz. However if the system is 16 bits wide instead of 8 bits the PCLK frequency would become 20 MHz × 16 bits = 320 MHz which is beyond the range of the VCO. Therefore the S Counter block must be added to divide the REFIN input frequency down to a more manageable frequency. Using the equation and the above example of a 20 MHz REFIN input with 16 bits of data, the S Counter is used as a divide-by-two counter to get a PCLK frequency of 160 MHz.

The S Counter can be programmed to divide by any integer up to 8 and the L Counter can be programmed for any word width from 4 bits to 64 bits in increments of 4. Table I shows some of the frequencies possible using various values for the S- and L-modulus.

VARIOUS SYSTEM ARCHITECTURES

Figure 4 demonstrates the DP8513 in a system using a video shift register and a DRAM. Another possible application uses a video DRAM or VDRAM, in place of the DRAM, as shown in *Figure 5.* This system differs from *Figure 4* in that the VDRAM contains an internal shift register which allows

TABLE I. Partial Table of PCLK Frequencies

S MOD	8-Bit Word (L = 8)		16-Bit Word (L = 16)		32-Bit Word (L = 32)	
	PCLK Frequency		PCLK Frequency		PCLK Frequency	
	REFIN = 10 MHz	REFIN = 20 MHz	REFIN = 10 MHz	REFIN = 20 MHz	REFIN = 10 MHz	REFIN = 20 MHz
1	80.0 MHz	160.0 MHz	160.0 MHz	na	na	na
2	40.0	80.0	80.0	160.0 MHz	160.0 MHz	na
3	26.7	53.3	53.3	106.7	106.7	na
4	20.0	40.0	40.0	80.0	80.0	160.0 MHz
5	16.0	32.0	32.0	64.0	64.0	128.0
6	13.3	26.7	26.7	53.3	53.3	106.7
7	11.4	22.9	22.9	45.7	45.7	91.4
8	10.0	20.0	20.0	40.0	40.0	80.0

Circuit Operation (Continued)

memory to be randomly accessed while data is being output to the video shift registers through the serial port. The output of the VDRAM differs from the standard DRAM in that data is not valid at the output of the internal shift register until an SCLK pulse is provided. The offset in the LCLK3 waveform from LCLK1 is obtained by connecting ENOUT1 to ENIN3.

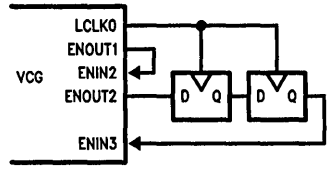
The third type of system employs a video shift register (such as the DP8515) that contains an onboard FIFO as shown in *Figure 6*. This architecture simplifies timing requirements in a high-speed multiboard system. The propagation delay time from the DRAM to the video shift register through the back plane is no longer restricted to be less than one LCLK period. The VDRAM can be writing into the FIFO asynchronous to the data being loaded into the shift register. As in the previous systems, one LCLK1 pulse transfers the data to the VDRAM output. LCLK2 then writes several words into the FIFO prior to the LCLK3 reading out the first word. The connections required to obtain this timing are shown in the diagram.

To implement a multiboard system the DP8513 is used in conjunction with the DP8514 and a Video Shift Register with a FIFO (such as the DP8515/16). The various LCLK signals from the DP8513 control the VRAM shifting and FIFO read and write operations to minimize the problems associated with backplane delays.

Typically the main board will contain a DP8513 Video Clock Generator Slave as well as a DP8514 Crystal Clock Generator, the DP8515/16 Video Shift Registers (one per plane), and a main graphics processor (such as the DP8500). See the multiboard diagram which follows. The other boards will contain one or more planes of memory and the associated BIT-BLT processors (such as the DP8510), and one DP8514 to generate the two-phase clock for the processors.

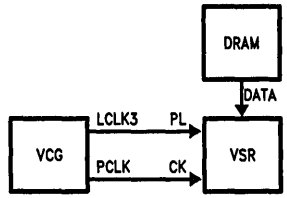
The 2X and 1X clocks (XOUT and DATA OUT) provided by the DP8514 on the main board are used by the DP8513 to generate non-overlapping clocks for the graphics processor. These 2x and 1x signals are also sent across the backplane to the memory boards where other DP8514's generate non-overlapping clocks for the BIT-BLT processors. The display of information is started by an ENABLE signal from the RGP to the ENIN1 of the DP8513. The remaining ENIN and ENOUT pins are connected as shown in *Figure 6* along with the resulting LCLK waveforms. LCLK3 and PCLK are used to read data from the FIFO and shift it to the DAC's. All of the VSR's must be on the main board to keep the 225 MHz PCLK signal off the backplane. LCLK1 is sent through the backplane to the SCLK inputs of all the VRAMS and causes data to be shifted out to the VSR's FIFO's. LCLK2 is sent through the backplane to a buffer and then through the backplane again to the WR inputs of the FIFO's. These two backplane delays are used to cancel the back plane delays from the DP8513's LCLK1 pin to the VRAM's SCLK pin and from the VRAM's output to the FIFO's input.

Following the path from the LCLK2 pin of the DP8513 to the WR pin of the VSR, we find two backplane delays and a buffer prop delay which is assumed to be negligible in the following discussion. Note from *Figure 6* that the LCLK3 occurs three LCLK periods after LCLK2. This means that two backplane delays can be as much as three LCLK periods, or $T_{BP} < 3/2\ T_{LCLK}$ for no loss of data. To increase this time further one or more D Flip Flops may be inserted between ENOUT2 and ENIN3 as shown in *Figure 3*. Each flip flop will increase the allowable backplane delay by approximately 1/2 LCLK period.

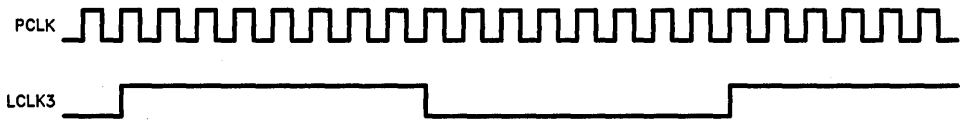


TL/F/9283–5

FIGURE 3



TL/F/9283–6



TL/F/9283–7

FIGURE 4. System Configuration and LCLK Waveforms Using DRAM

Circuit Operation (Continued)

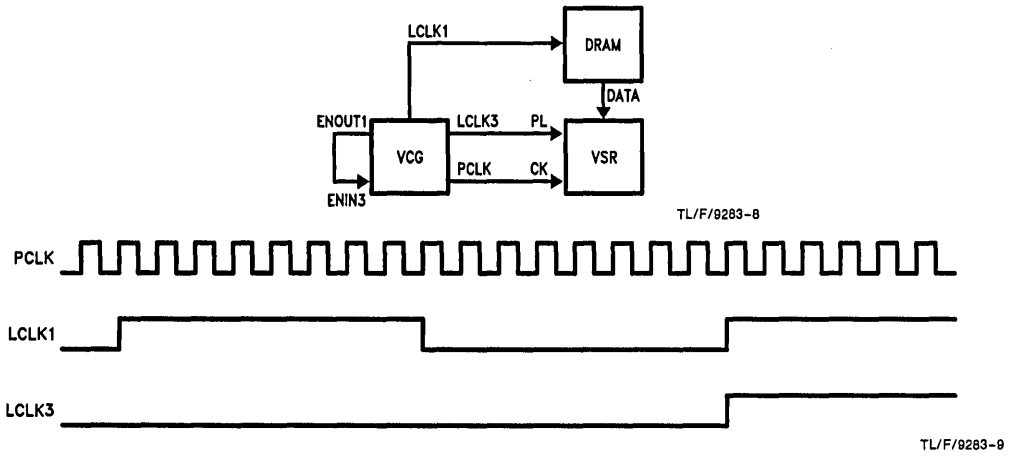


FIGURE 5. System Configuration and LCLK Waveforms Using VDRAM

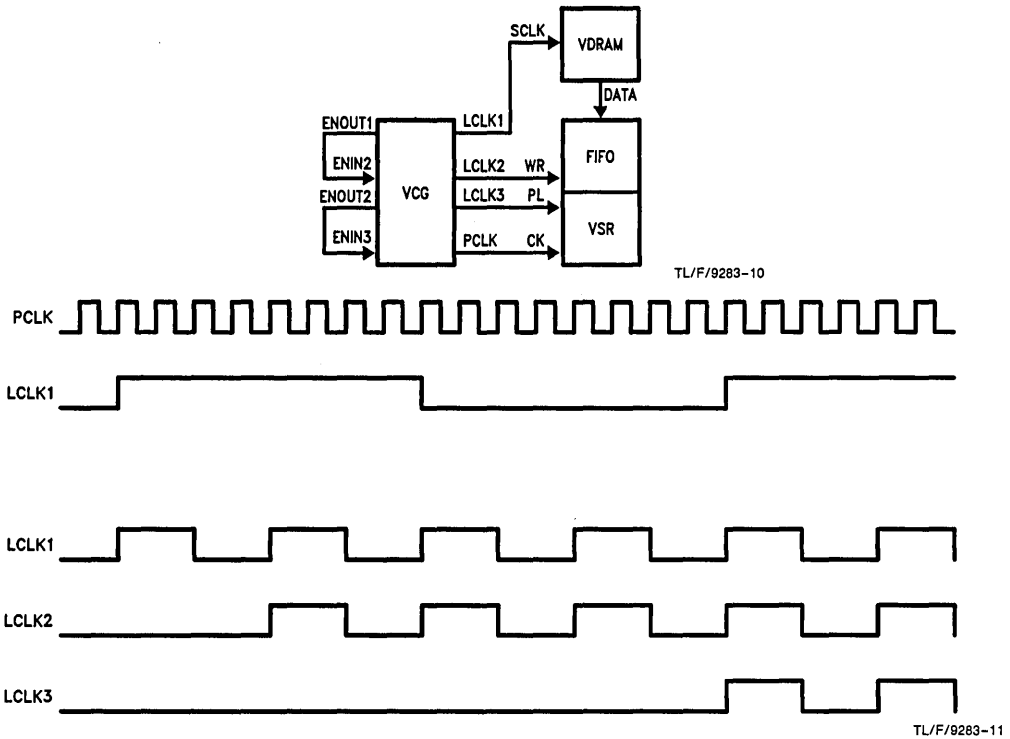
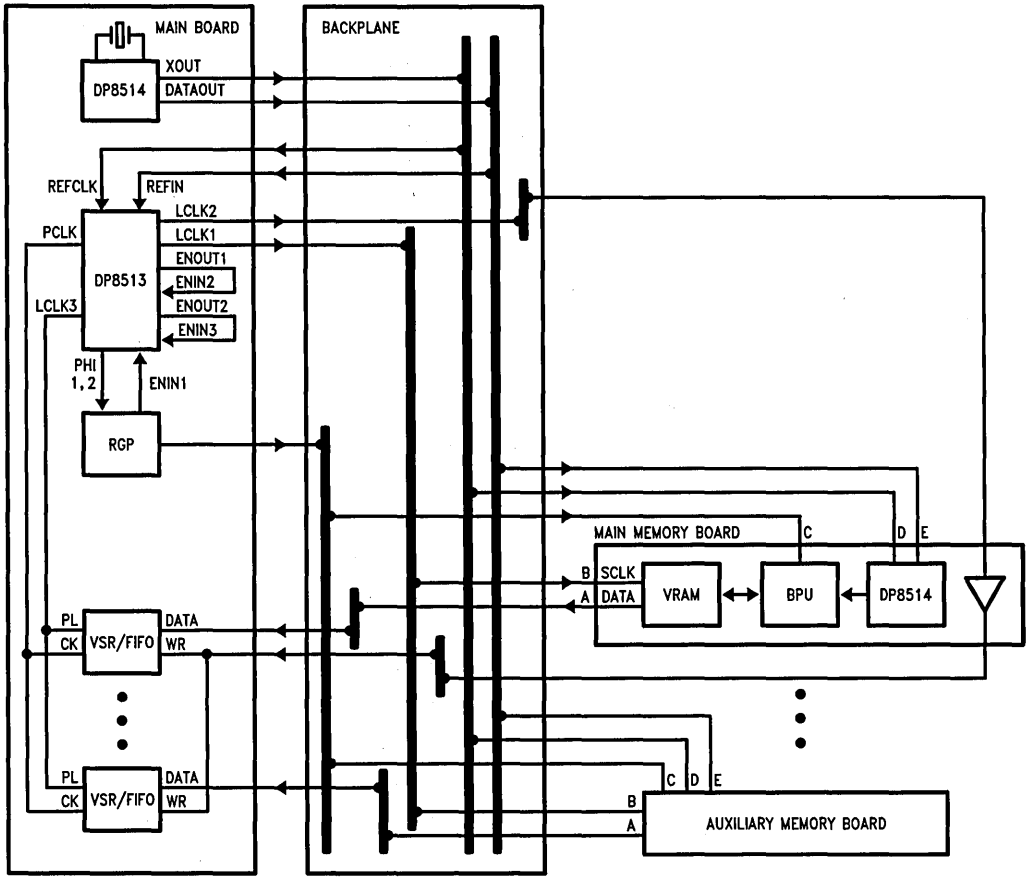


FIGURE 6. System Configuration and LCLK Waveforms Using a VSR Containing FIFO

Multi-Board Diagram



TL/F/9283–12

TABLE II. Counter Modulus Tables

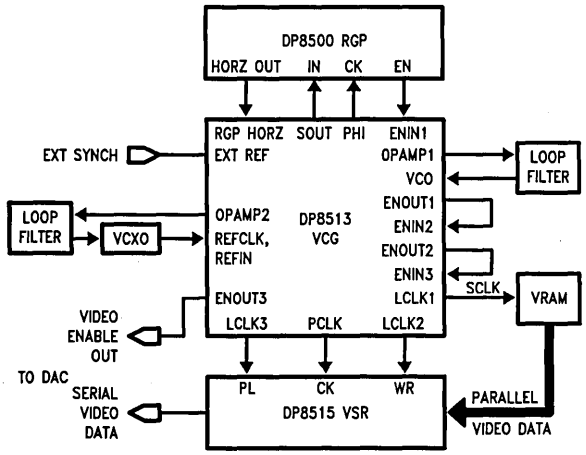
S MOD	S Counter Inputs		
	S2	S1	S0
1	L	L	L
2	L	L	H
3	L	H	L
4	L	H	H
5	H	L	L
6	H	L	H
7	H	H	L
8	H	H	H

L = TTL Logic Zero (GND0, 1)
H = TTL Logic One (VTTL0, 1)

L MOD	L Counter Inputs			
	L3	L2	L1	L0
4	0	0	0	0
8	0	0	0	1
12	0	0	1	0
16	0	0	1	1
20	0	1	0	0
24	0	1	0	1
28	0	1	1	0
32	0	1	1	1
36	1	0	0	0
40	1	0	0	1
44	1	0	1	0
48	1	0	1	1
52	1	1	0	0
56	1	1	0	1
60	1	1	1	0
64	1	1	1	1

0 = VEE
1 = VECL0, 1

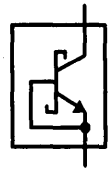
Typical System Diagram



TL/F/9283–21

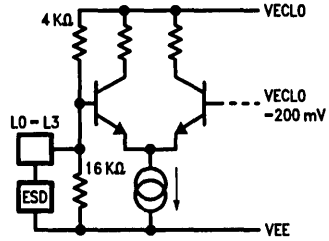
Input Schematics

Typical ESD Circuit



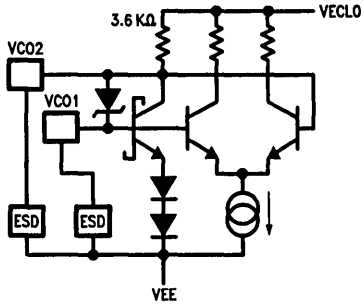
TL/F/9283-22

L0–L3 Inputs



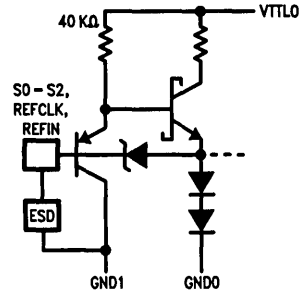
TL/F/9283-23

VCO Inputs



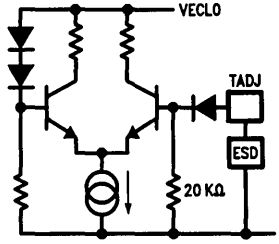
TL/F/9283-24

TTL Inputs
S0–S2, REFCLK, REFIN



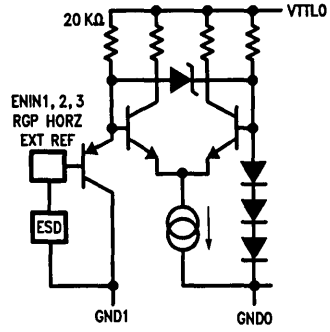
TL/F/9283-25

Timing Adjust Input



TL/F/9283-26

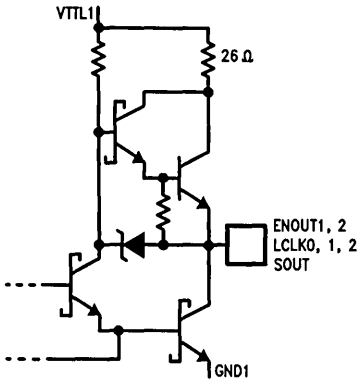
TTL Inputs
(ENIN1, 2, 3, RGP HORIZ, EXT REF)



TL/F/9283-27

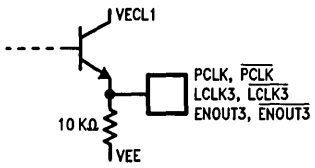
Output Schematics

TTL Outputs
(ENOUT1, 2, LCKL0, 1, 2, SOUT)



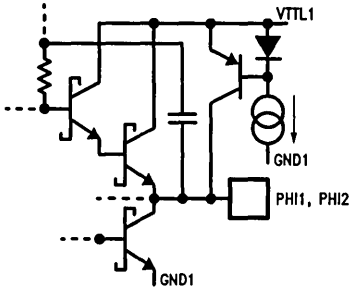
TL/F/9283–28

ECL Outputs



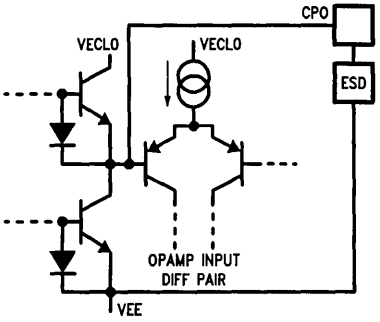
TL/F/9283–29

PHI1, PHI2



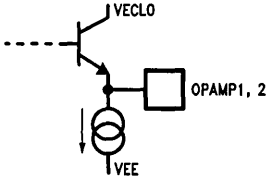
TL/F/9283–30

Charge Pump Output/OP Amp Input



TL/F/9283–31

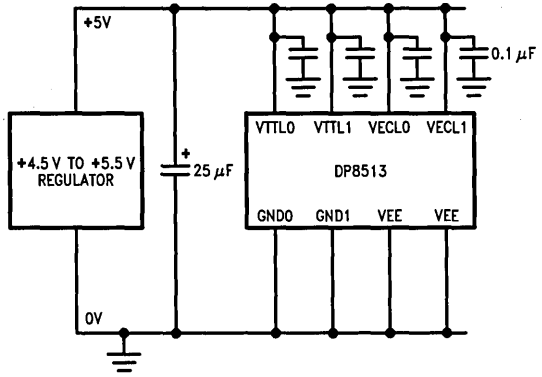
Op Amp Output



TL/F/9283–32

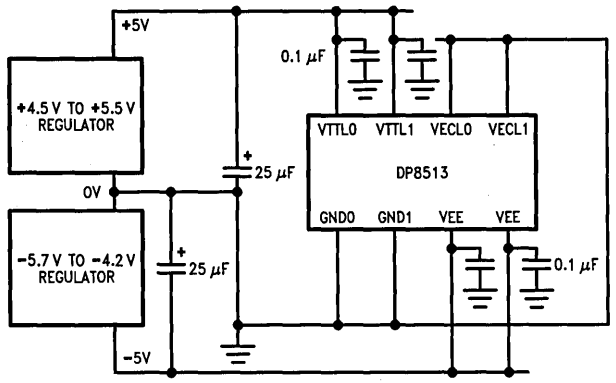
Typical Power Connections

Single Power Supply Operation



TL/F/9283–33

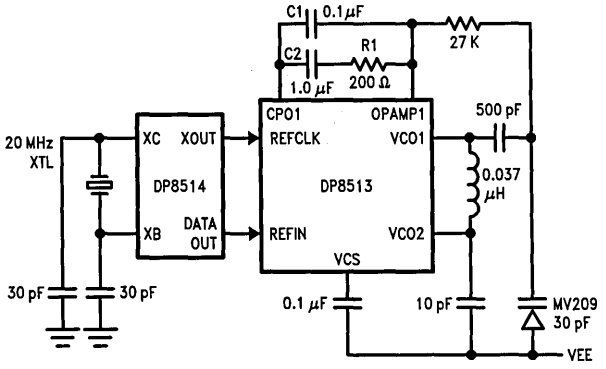
Dual Power Supply Operation



TL/F/9283–34

Typical Applications

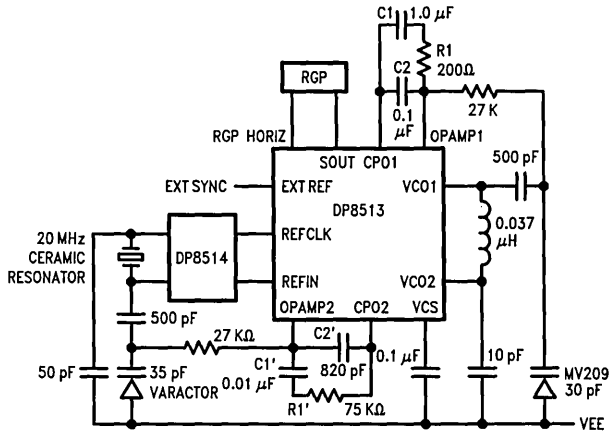
Crystal Referenced System
PCLK = 200 MHz, L = 20, S = 1



TL/F/9283–35

Typical Applications (Continued)

External Referenced System
PCLK = 200 MHz, L = 20, S = 1



TL/F/9283–36

Loop Filter Calculations

Several constants need to be known in order to determine the loop filter components. They are the loop divide ratio N, the phase detector gain K_p, the VCO gain K_o, the loop bandwidth ω_o, and phase margin ϕ.

The constant K_p is fixed at 80 μA/rad for the DP8513. N is simply the L counter modulus for the main loop. For the secondary loop, N is the S counter modulus times any external division between the SOUT pin and the RGP HORIZ pin. (i.e., if S = 1 and there is a ÷100 counter between SOUT and RGP HORIZ, N = 1 × 100 = 100.) A 60° phase margin is recommended, however, the equations allow other values to be used if desired.

The oscillator gain constant of K_o can be obtained from Table III or determined experimentally. This is done by driving the 27k resistor which normally connects the varactor to the op amp output with an external power supply. Set the supply to V_{EE} + 3V and note the PCLK frequency. Next set the supply to V_{EE} + 2V and note the frequency again. The difference in these two frequencies (times 2π to convert to radians) is K_o. For optimum performance, the desired PCLK frequency should be somewhere between the two frequencies measured above. This may require adjustment of the coil.

Before choosing a value of ω_o, one fact should be pointed out. The 27k resistor and the 500 pF coupling capacitor between the coil and the varactor form a low pass filter with a cutoff of about 12 kHz. Thus, the loop bandwidth must be chosen to be less than this value. We recommend $2\pi \times$ 100 Hz to $2\pi \times$ 3 kHz for ω_o.

Having found all these constants, the following equations are used to find the component values:

$$R1 = \frac{1.08\, N\, \omega_o}{K_p\, K_o} \quad C1 = \frac{3.46\, K_p\, K_o}{N\, \omega_o^2} \quad C2 = \frac{0.27\, K_p\, K_o}{N\, \omega_o^2}$$

To use a phase margin of other than 60°, use the following:

$$R1 = \frac{N\, \omega_o}{2\, K_p\, K_o}(\text{cosec}\, \phi + 1)$$

$$C1 = \frac{2\, K_p\, K_o}{N\, \omega_o^2} \tan \phi$$

$$C2 = \frac{K_p\, K_o}{N\, \omega_o^2}(\sec \phi - \tan \phi)$$

Example: Design a system with the following characteristics:

External horizontal sync of 100 kHz
1560 pixels per line (2000 pixels including retrace)
20 bit wide video data
10 MHz processor rate

Note that this system will sync to an external source so that both loops must be used.

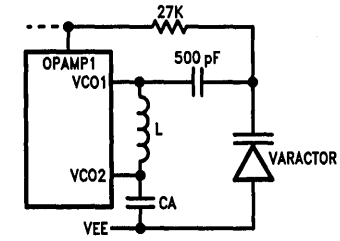
The PCLK frequency wil be 100 kHz x 2000 pixels per line = 200 MHz. The components in Table III will be used. Note that K_o = 24 Mrad. Because it is a 20 bit wide system the L counter modulus must be 20.

By choosing $\omega_o = 2\pi \bullet 2800$ Hz, the equations give R1 = 200Ω, C1 = 1.0 μF and C2 = 0.08 μF (use C2 = 0.1 μF).

In the secondary loop, a ceramic resonator is used in place of a crystal to allow more pullability. Its K_o is found experimentally to be 84 krads/V. The SOUT frequency will be the same as LCLK0 or 200 MHz ÷ 20 = 10 MHz. Thus, there must be a ÷100 counter between SOUT and RGP HORIZ so N = 100 for the secondary loop.

In choosing ω_o, it should be noted that ω_o for the secondary loop should be smaller than ω_o for the primary loop so that the main loop will be able to track the secondary without loosing lock. Picking $\omega_o = 2\pi \times 750$ Hz gives R1′ = 75k, C1′ = 0.01 μF and C2′ = 820 pF.

Recommended VCO Components



TL/F/9283–37

$$F_{VCO} = \frac{1}{2\pi\sqrt{LC_{TOT}}} \qquad C_{TOT} = \frac{1}{\frac{1}{CA} + \frac{1}{C_{VARACTOR}}}$$

TABLE III. Recommended VCO Components

Frequency (MHz)	L μH	TOKO Coil Type S18 Part #	CA pF	Cvaractor pF	Motorola #	K_O Mrad/volt
60	0.258	E502HNS-6000026	56	30	MV209	16
80	0.17	E502HNS-4000024	39	30	MV209	19
100	0.12	E502HNS-3000023	30	30	MV209	21
120	0.07	E502HNS-2000022	39	30	MV209	31
140	0.07	E502HNS-2000022	22	30	MV209	27
160	0.07	E502HNS-2000022	15	15	MV2205	27
180	0.07	E502HNS-2000022	10	15	MV2205	26
200	0.037	E502HNS-1000029	10	30	MV209	24
220	0.037	E502HNS-1000029	10	15	MV2205	34

National Semiconductor

PRELIMINARY

DP8514 Crystal Clock Generator

General Description

The DP8514 Crystal Clock Generator consists of a crystal or LC tank oscillator and a synchronizer/2-phase nonoverlapping MOS clock driver. It is designed to interface directly with the DP8513 Video Clock Generator in multiboard graphics applications. However its features and flexible design allow it to be used in numerous other applications as well.

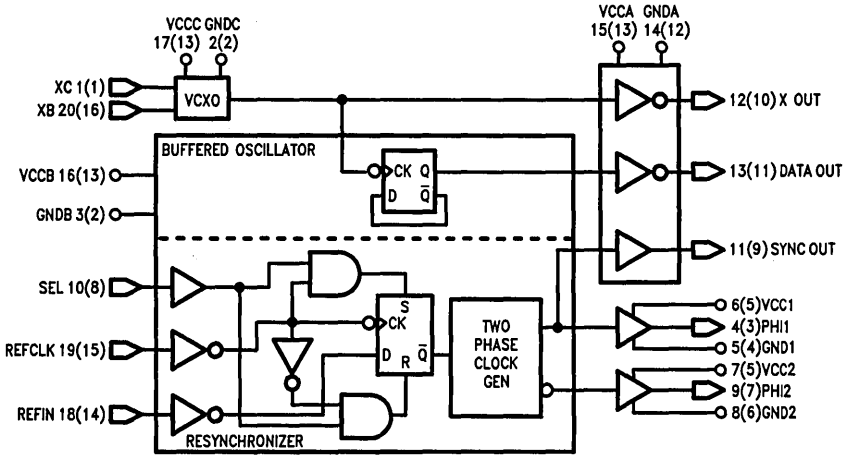
There are two outputs from the Pierce crystal oscillator. One is the same frequency as the crystal and has an approximate 50% duty cycle while the other is half the crystal frequency with a 50% duty cycle. Both of these outputs are TTL-compatible. The oscillator may also be used as an LC oscillator, if desired.

The other section of the die contains a resynchronizer with additional clock follow logic, and a 2-phase nonoverlapping MOS-compatible clock driver. Both sections of the die may be used independently of each other. The synchronizer is a D register which has a clock input, REFCLK, a data input, REFIN, and a mode control input, SEL, which allows the REFCLK input to control the synchronizer's output. This feature allows either the clock or the resynchronized clock ÷ 2 to be fed to the MOS clock driver. A TTL output (SYNC OUT) in phase with the PHI1 output is also provided.

Features

- Pierce oscillator may be used with crystal, ceramic resonator, or LC tank circuit. External varactor allows VCO or VCXO mode.
- TTL-compatible oscillator and oscillator ÷2 outputs.
- Two-phase nonoverlapping MOS-compatible clock outputs drive 100 pF loads at 20 MHz.
- Synchronizer/driver eases synchronization of PHI1 and PHI2 clocks on multiple boards.
- TTL-compatible SYNC OUT in phase with PHI1.
- Available in standard 16 pin DIP, 16 pin SO, and 20 pin PCC packages.

Block Diagram pin numbers are for 20 pin PCC (16 pin DIP) package

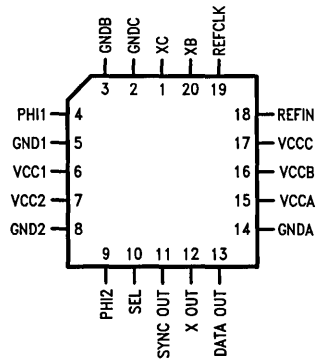


TL/F/9284–1

1

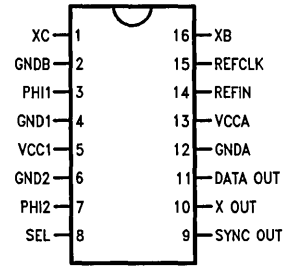
Connection Diagrams

PCC Package



TL/F/9284–2

Dual-In-Line Package



TL/F/9284–3

Order Number DP8514
See NS Package Number M16A, N16A or V20A

Pin Descriptions (parenthesis indicate 16 pin DIP)

1, 20 (1, 16)	**XC, XB:** External connections for the Pierce oscillator.
2, 3 (2)	**GNDC, GNDB (GNDB):** Power supply return for the crystal oscillator, and power supply return for all circuitry except the VCXO and output buffers. The 16 pin version has a single power supply return for all circuitry except the output buffers.
4, 9 (3, 7)	**PHI1, PHI2:** MOS-compatible two-phase non-overlapping clocks. The frequency of these signals is that of the REFCLK input when SEL is high and that of the REFIN input when SEL is low.
5, 8 (4, 6)	**GND1, GND2:** PHI1 and PHI2 output buffer power supply return.
6, 7 (5)	**VCC1, VCC2 (VCC1):** PHI1 and PHI2 positive power supplies specified for operation at 5V ±10%.
10 (8)	**SEL:** TTL-compatible MUX control input selects either the REFCLK input or the REFIN input (resynchronized to REFCLK by a Flip Flop) to be passed to the PHI generator circuitry. A low selects the REFIN input frequency and a high selects the REFCLK input frequency.
11 (9)	**SYNC OUT:** TTL-compatible output equivalent to PHI1.
12 (10)	**X OUT:** TTL-compatible output of the crystal oscillator.
13 (11)	**DATA OUT:** TTL-compatible output whose frequency is that of the crystal divided by two.
14 (12)	**GNDA:** TTL output buffer power supply return.
15, 16, 17 (13)	**VCCA, VCCB, VCCC (VCCA):** TTL output buffer, internal circuitry, and crystal oscillator positive power supply, respectively. The 16 pin version has a single positive power supply for all circuitry except the PHI1 and PHI2 buffers.
18 (14)	**REFIN:** TTL-compatible input typically used to generate PHI1 and PHI2. Equivalent to the REFIN input on the DP8513.
19 (15)	**REFCLK:** TTL-compatible input typically used to synchronize multiple DP8514's. This is the CK input of a positive edge triggered D Flip Flop. Equivalent to the REFCLK input on the DP8513.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
V_{CC}	7.0V
Inputs	7.0V
Outputs	7.0V

ESD rating is to be determined.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
F_{OSC}	Oscillator Frequency			40	MHz
F_{RESYNC}	Resynchronizer Frequency			40	MHz
T_{SU}	Setup Time REFIN to REFCLK	10			ns
T_H	Hold Time REFCLK to REFIN	0			ns

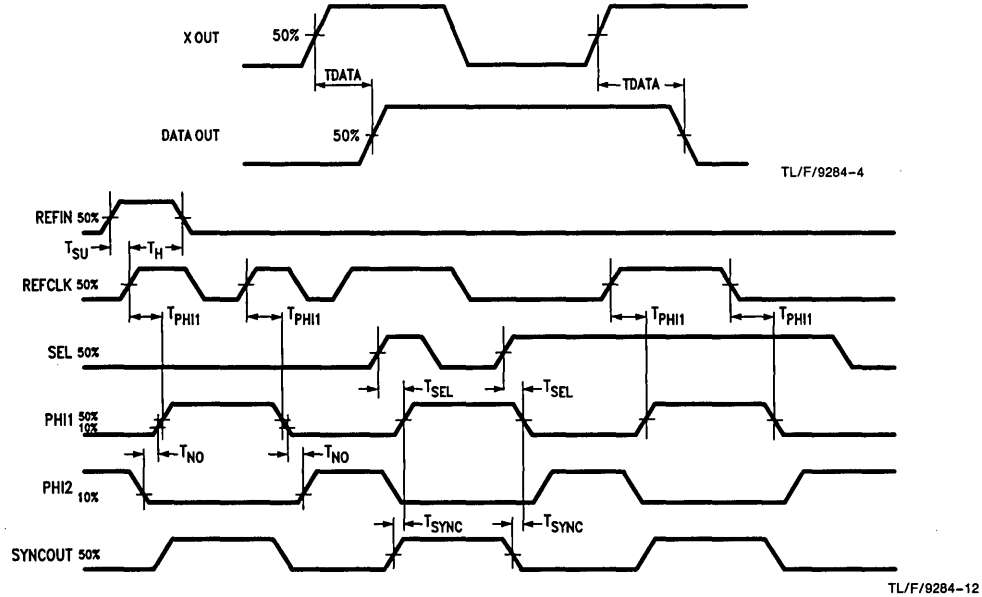
DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Nom	Max	Units
V_{OH}	High Level Output Voltage All Outputs	I_{OH} = −2 mA	V_{CC} − 2			V
	High Level Output Voltage MOS Outputs	I_{OH} = −100 μA	V_{CC} − 0.3			
V_{OL}	Low Level Output Voltage All Outputs	I_{OL} = 20 mA		0.35	0.5	V
	Low Level Output Voltage MOS Outputs	I_{OL} = 100 μA			0.3	
I_O	Output Drive Current TTL Outputs	V_O = 2.25V	−30		−110	mA
	Output Drive Current MOS Outputs	V_O = 2.25V		−135		
I_{CC}	Supply Current	V_{CC} = 5.5V		20	35	mA

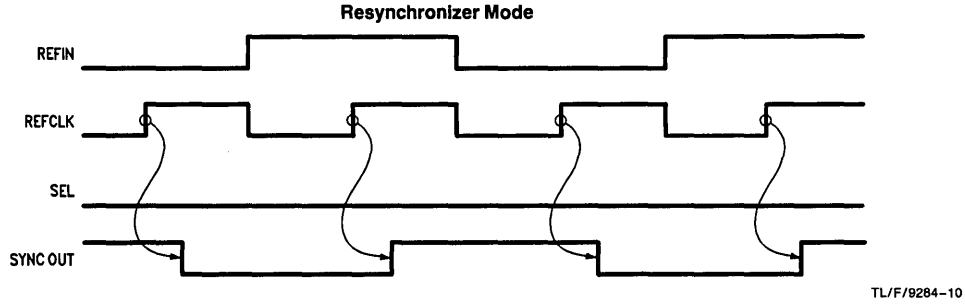
AC Electrical Characteristics

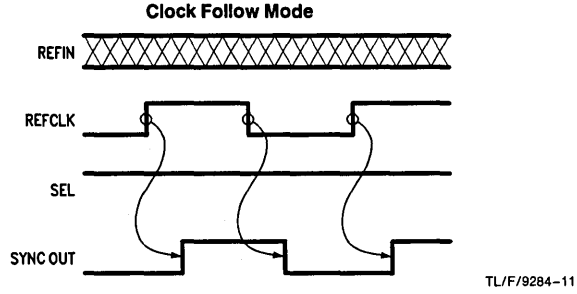
Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{MAX}	Max Oscillator Frequency		40			MHz
	Max Resynchronizer Clock Frequency	40% ≤ F_{IN} Duty Cycle ≤ 60%	40			
D_C	X OUT Duty Cycle		40		60	%
T_{DATA}	X OUT to DATA OUT		5	10	15	ns
T_{NO}	Non-overlap Time PHI1 to PHI2	C_L = 100 pF	0	4		ns
T_R, T_F	Rise, Fall Time PHI1 and PHI2	C_L = 100 pF, 10% to 90%		4	6	ns
T_{SYNC}	SYNC OUT to PHI1		−5	0	5	ns
T_{PHI1}	REFCLK to PHI1 ↗			40		ns
	REFCLK to PHI1 ↘			28		
T_{SEL}	SEL ↗ to PHI1 ↗	REFCLK = HIGH		40		ns
	SEL ↗ to PHI1 ↘	REFCLK = LOW		28		

AC Timing Waveforms

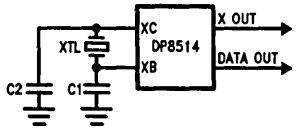


Functional Waveforms





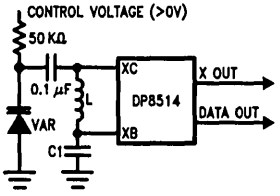
Typical Applications



TL/F/9284-7

C1, C2 dependent on crystal ≈ 30 pF

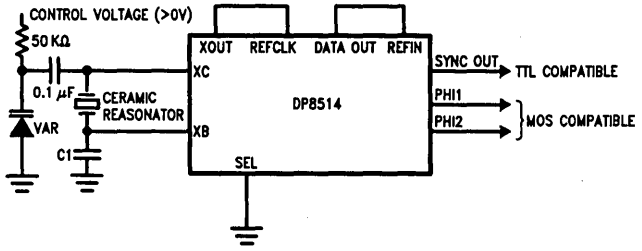
FIGURE 1. Crystal Oscillator



TL/F/9284-8

$$F_{X\,OUT} = \frac{1}{2\pi\sqrt{LC_T}} \quad \text{where } C_T = \frac{C1 \times VAR}{C1 + VAR} \text{ given } 0.1\ \mu F \gg C_T$$

FIGURE 2. VCO



TL/F/9284-9

$F_{SYNC\,OUT} = F_{CERAMIC\,RESONATOR} \div 2$

FIGURE 3. VCXO with MOS compatible outputs

National Semiconductor

DP8515/DP8515-350/DP8516/DP8516-350 Video Shift Register (VSR)

General Description

The DP8515/DP8515-350/DP8516/DP8516-350 Video Shift Register (VSR) provides the functions of a high speed sixteen bit shift register and parallel data input latches/flip-flops required in high performance raster scan video systems. Also on the VSR are four words of FIFO which by means of the mode control input pins M0 and M1 may be placed in front of the shift register if the user so desires.

The VSR has three operating modes; inputs configured as transparent latches, inputs configured as flip-flops (one word FIFO mode), and four word FIFO mode. As mentioned above, the mode control input pins, M0 and M1 select in which mode the part is operating. In all three modes, the WR input allows data into the part, the PARALLEL LOAD input loads data into the shift register, and the PIXEL CLOCK input shifts data out of the shift register.

In the four word FIFO mode, four write operations may occur before a shift register load operation is required in order to avoid writing over previously written data. The four words of FIFO significantly ease the timing constraints which are present when working with high speed multiple board systems.

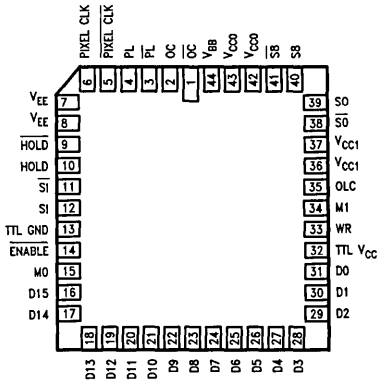
The VSR has a HOLD input which, when activated, inhibits the shift function of the shift register. Two other inputs, OUTPUT CONTROL and OUTPUT LEVEL CONTROL, hold the last bit of the shift register at a level chosen by the user while allowing the internal bits of the shift register to continue shifting. Another control input, $\overline{\text{ENABLE}}$, causes the parallel loading of the shift register to be inhibited when deactivated.

The inputs to the VSR, except those associated with the shift register, are TTL compatible. The shift register inputs and control signals are ECL compatible as are the outputs. Furthermore, two versions of the chip are available; the DP8515/DP8515-350 has ECL outputs which are 10K compatible and the DP8516/DP8516-350 has ECL outputs which are 100K compatible. All the ECL inputs and outputs are differential, however, a V_{BB} reference output is provided for the user who wishes to use only single ended signals. The VSR implements all the TTL to ECL conversions and gives the customer the choice of using positive or negative supplies for the ECL circuitry. When using positive supplies, the ECL and TTL may be operated off of the same, single, +5V supply.

Features

- TTL compatible parallel data inputs
- Data inputs may be used as transparent latches or flip-flops
- Four words of FIFO available—essential for high speed multiple board systems
- Accepts input data at rates up to 20 MHz (30 MHz for −350)
- Tap at eighth bit, allows use as 2 8-bit shift registers
- ECL inputs and outputs may be differential or single ended
- TTL to ECL conversion performed on chip
- Shift register clock rate of 225 MHz (350 MHz for −350)
- Can use positive or negative ECL supplies
- Entire chip can operate off of single +5V supply
- Total chip I_{CC} less than 200 mA
- Packaged in a 44-pin PLCC
- A member of National's Advanced Graphics Chip Set

Connection Diagram

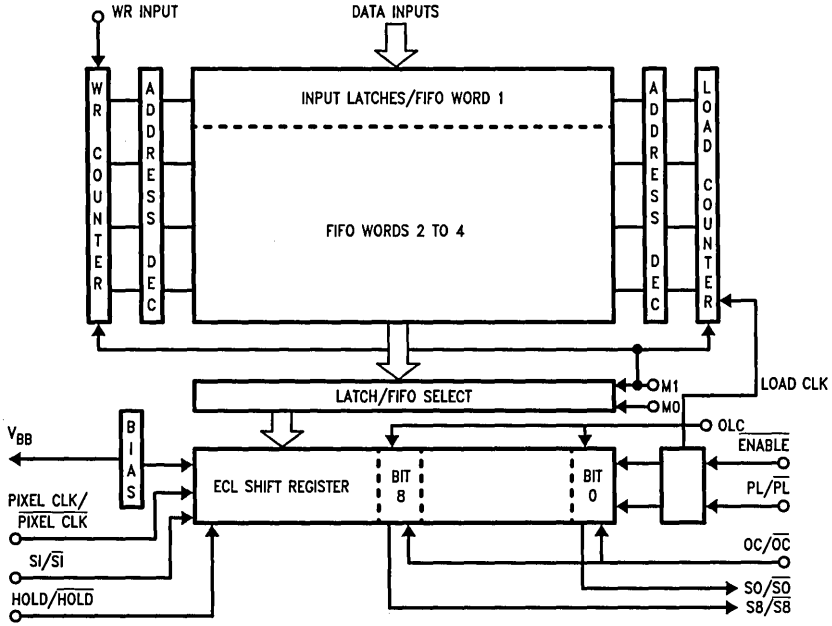


TL/F/8684-1

Top View

Order Number DP8515V, DP8515-350V, DP8516V, or DP8516-350V
See NS Package Number V44A

Block Diagram



TL/F/8684–2

Pin Descriptions

36,37 V_{CC1}—This is the supply for the collectors of the ECL emitter follower outputs. Both the 10K and 100K options are specified for a supply from 4.2V to 5.5V, assuming a positive supply is used. This allows use of the standard 5V ±10% supply, 5.2V ±5% 10K supply, or 4.5V ±0.3V 100K supply. For a negative supply, these pins are at ground potential.

42 V_{CC0}—This is one supply for the most positive rail of the ECL circuitry. It is a separate supply for the output buffers used to reduce noise coupling. The ranges are the same as those specified for V_{CC1}.

43 V_{CC0}—This is the supply for the most positive rail of the ECL internal circuitry. The ranges are the same as those specified for V_{CC1}.

32 TTL V_{CC}—This is the positive supply for the TTL circuitry. The supply is specified at +5.0V ±10%.

13 TTL GROUND

7,8 V_{EE}—This is the most negative rail for the ECL circuitry. Using a positive supply, this pin is at ground potential. For a negative supply, both the 10K and 100K options are specified from −4.2V to −5.5V. This allows use of the −5.2V ±5% 10K supply or the −4.5V ±0.3V 100K supply.

44 V_{BB}—This is the bias reference for the ECL inputs. All of the ECL inputs are differential; however, if single ended use is desired, the unused input may be tied to this V_{BB} pin. This pin is nominally set at V_{CC0} − 1.3V at room temperature for 10K ECL and V_{CC0} − 1.3V over temperature for 100K ECL. See the electrical characteristics table for the exact specifications for V_{BB}.

16–31 DATA INPUTS—These are TTL compatible inputs designed to meet the ALS specifications (as are all TTL inputs on this circuit). The data present at these inputs will be converted to serial data by the ECL shift register. Data on pin 31 (D0) will be the first bit shifted out of the shift register. The data on pin 16 (D15) will be the last bit shifted out of the shift register. Data at these inputs must meet the setup time requirements for the WR input.

15,34 MODE CONTROL INPUTS—M0, M1—These two TTL-compatible inputs control whether the data inputs are transparent latches or edge triggered flip flops. They also control whether or not the four word FIFO is placed in front of the shift register. With M0 set high the FIFO is not present and the data inputs are transparent latches. When M0 is high the level of the M1 input does not matter. With M0 low and M1 low the FIFO is again not present and the inputs are edge triggered flip flops. Actually this is equivalent to there being one word of FIFO present. A low level on M0 and a high level on M1 results in the four word FIFO being placed in front of the shift register. Although a power up reset is present for the FIFO address counters, if the user wishes to reset the FIFO address to word zero, a low pulse on M1 while the PARALLEL LOAD input is in a high state will accomplish this.

33 WR INPUT—This is a TTL compatible input. When data inputs are configured as flip flops, data on the bus is latched into the input flip flops on the positive edge of the WR input. If the inputs are configured as transparent latches, data is passed on to the shift register inputs so long as the WR input is low. If the four word FIFO is being used (M0 = 0 and M1 = 1), data on the bus will be latched into the first word on the positive edge of the WR input.

Pin Descriptions (Continued)

6,5 PIXEL CLOCK, $\overline{\text{PIXEL CLOCK}}$—These are the differential clock inputs for the ECL shift register. If single ended use is desired, one input should be connected to the V_{BB} pin. The first positive PIXEL CLOCK transition after a positive transition on the PARALLEL LOAD input loads into the ECL shift register the sixteen bit word present at or already latched into the inputs by the WR input. Subsequent positive PIXEL CLOCK transitions will shift the remaining 15 bits out of the shift register.

4,3 PARALLEL LOAD, $\overline{\text{PARALLEL LOAD}}$—These are the differential load inputs for the ECL shift register. If single ended use is desired, one input should be connected to the V_{BB} pin. When using the PARALLEL LOAD function, the setup time between PARALLEL LOAD and the positive going edge of PIXEL CLOCK must be met. To load a sixteen bit word from the input (latched or just present at the input depending on mode of operation) to the ECL shift register, a positive edge on the PARALLEL LOAD input is required and the first positive going edge of the PIXEL CLOCK following this positive edge will load the data into the shift register.

12,11 SERIAL INPUT, $\overline{\text{SERIAL INPUT}}$—These are the differential serial data inputs to the ECL shift register. If single ended use is desired, one input should be connected to the V_{BB} pin. These inputs may be used for expansion to a wider bus system where they are connected to the SERIAL OUTPUT, $\overline{\text{SERIAL OUTPUT}}$ of the previous shift register. The information on these input pins is shifted into the shift register on the positive edge of the PIXEL CLOCK.

39,38 SERIAL OUTPUT, $\overline{\text{SERIAL OUTPUT}}$—These are the differential data outputs of the ECL shift register. They are ECL compatible and are capable of driving 50Ω loads. Termination resistors are required when they drive the SERIAL INPUT pins of the next shift register in an expanded bus system. The first bit shifted out is D0.

40,41 S8, $\overline{\text{S8}}$ OUTPUTS—These are the differential data outputs of the ECL shift register for D8. If an eight bit wide word is used instead of a sixteen bit wide word, this output is the first bit of the second word. By providing this output, the number of Video Shift Registers required for eight bit wide systems is cut in half.

10,9 HOLD, $\overline{\text{HOLD}}$—These are the differential ECL inputs used to inhibit the shifting of the ECL shift register. A high level on the HOLD input will disable the shifting of the ECL shift register. If single ended use is desired, one input should be connected to the V_{BB} pin. When using the HOLD function, the setup time between HOLD and the positive going edge of the PIXEL CLOCK must be met. When HOLD is released, the output data will not change until the following positive edge of the PIXEL CLOCK. The HOLD function can be used as a simple way of doing a "zoom" operation in graphics systems.

2,1 OUTPUT CONTROL, $\overline{\text{OUTPUT CONTROL}}$—These are the differential ECL inputs which allow the user to manipulate the shift register data if he so chooses. If single ended use is desired, one input should be connected to the V_{BB} pin. With the OUTPUT CONTROL input high, the last bits of the shift register, that is the SERIAL OUTPUT S0 and the S8 bit are held at a level determined by the OUTPUT LEVEL CONTROL input while all the other bits are shifted by the PIXEL CLOCK. As with the HOLD input, the setup time between OUTPUT CONTROL and the positive going edge of the PIXEL CLOCK must be met. This feature provides for a simple way of implementing a scrolling function. Since all the internal bits of the shift register are shifting, the user can effectively control the shift of the data on the screen.

35 OUTPUT LEVEL CONTROL—This TTL compatible input selects the level to which the output bit of the shift register will be set when the OUTPUT CONTROL inputs are activated. A high level on this input sets the output to a one while a low level sets the output to a zero.

14 $\overline{\text{ENABLE}}$—This TTL compatible input, when taken to a high level, inhibits the PARALLEL LOAD operation of the ECL shift register. So long as the $\overline{\text{ENABLE}}$ input remains low, every positive edge of the PARALLEL LOAD input followed by a positive edge of the PIXEL CLOCK results in a load operation on the shift register. When the $\overline{\text{ENABLE}}$ input is taken high the next PARALLEL LOAD command is ignored and all subsequent PARALLEL LOAD commands are ignored until the $\overline{\text{ENABLE}}$ input is taken low. Once taken low, the first PARALLEL LOAD positive edge and PIXEL CLOCK positive edge pair will result in a load operation.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature −65°C to +150°C

TTL Signals
- Inputs 7V
- Supply 7V

ECL Signals
- Inputs (Using Negative Supply) V_{EE} to +0.5V
- Inputs (Using Positive Supply) GND to V_{CC} +0.5V
- Output Current (DC Output High) −50 mA
- Supply (V_{EE} to GND Using Negative Supply) −7V to +0.5V
- Supply (V_{CC} to GND Using Positive Supply) −0.5V to +7V

ESD Susceptibility (Note 4) 1500V

Operating Conditions (Notes 1, 3 and 5) T_A = 0°C to +70°C

Symbol	Parameter	Conditions	Min		Typ	Max		Units
			DP8515/16	−350		DP8515/16	−350	
V_{CC}	TTL Supply		4.5	4.5	5.0	5.5	5.5	V
V_{EE}	10K/100K ECL Using Negative Supply		−5.5	−5.5		−4.2	−4.2	V
V_{CC1}/V_{CC0}	10K/100K ECL Using Positive Supply		4.2	4.2		5.5	5.5	V
T_a	Ambient Temp		0	0	25	70	70	°C
$f_{(pixel\ clk.)}$	Shift Rate (See Note 1 A.C. Elec. Char.)					225	350	MHz
$f_{(write)}$	WR Rate					20	30	MHz
$f_{(read)}$	PARALLEL LOAD Rate FIFO Mode					14	25 (30)	MHz
$f_{(read)}$	PARALLEL LOAD Rate Transparent Mode					20	30	MHz
t_{W1}	Width of PIXEL CLOCK HI or LO		2.0	1.5				ns
t_{W2}	Width of WR Input LO		25	15				ns
t_{W3}	Width of WR Input HI		30 (25)	20 (18)				ns
t_{W4}	Width of PARALLEL LOAD Input HI FIFO MODE		22 (20)	14 (12)				ns
t_{W5}	Width of PARALLEL LOAD Input LO FIFO MODE		42 (32)	26 (21)				ns
t_{W6}	Width of PARALLEL LOAD Input HI Transparent Mode		15	8				ns
t_{W7}	Width of PARALLEL LOAD Input LO Transparent Mode		30 (25)	20 (17)				ns
t_{SU1}	Setup Time HOLD to PIXEL CLK		1.5	1.5				ns
t_{SU2}	Setup Time OUTPUT CONTROL to PIXEL CLK		3.0	2.5				ns
t_{SU3}	Setup Time PARALLEL LOAD to PIXEL CLK		1.5	1.5				ns
t_{SU4}	Setup Time SERIAL IN to PIXEL CLK		1.5	1.0				ns
t_{SU5}	Setup Time DATA to PARALLEL LOAD		20	10				ns
t_{SU6}	Setup Time $\overline{\text{ENABLE}}$ Inactive to PARALLEL LOAD		34	26				ns
t_{SU7}	Setup Time DATA to WR		5	4				ns
t_{SU8}	Setup Time $\overline{\text{ENABLE}}$ Active to PARALLEL LOAD		12	10				ns
t_{SU9}	Setup Time WR to PARALLEL LOAD (Note 2)		25	20				ns
T_{SU10}	Setup Time WR to PARALLEL LOAD Transparent Mode		35	26				ns
t_{H1}	Hold Time HOLD to PIXEL CLK		2.5	2.5				ns
t_{H2}	Hold Time OUTPUT CONTROL to PIXEL CLK		1.0	0.5				ns
t_{H3}	Hold Time PARALLEL LOAD to PIXEL CLK		1.0	1.0				ns
t_{H4}	Hold Time SERIAL IN to PIXEL CLK		1.3	1.1				ns
t_{H5}	Hold Time DATA to PARALLEL LOAD		0	0				ns
t_{H6}	Hold Time $\overline{\text{ENABLE}}$ Inactive to PARALLEL LOAD		0	0				ns
t_{H7}	Hold Time DATA to WR		12	10				ns
t_{H8}	Hold Time $\overline{\text{ENABLE}}$ Active to PARALLEL LOAD		0	0				ns

Note 1: See timing waveforms for relevant signal edges (positive or negative) from which all setup measurements are made.

Note 2: This is the time that a write operation on the WR input must precede a read operation on the PARALLEL LOAD input when in the one word FIFO mode (edge triggered flip flop inputs) and when in the FIFO mode and the FIFO is empty.

Note 3: Numbers in parenthesis are guaranteed when using a negative ECL supply with a V_{EE} max of −4.75V or when using a positive ECL supply with a V_{CC1}/V_{CC0} min of 4.75V.

Note 4: Human body model; 120 picofarads thru 1.5 kΩ.

Note 5: All measurements are made WRT 1.3V level on TTL signals and V_{CC0} — 1.3V on ECL signals.

DC Electrical Characteristics

TTL INPUTS AND SUPPLY (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_I = −18 mA			−1.5	V
V_{IH}	High Level Input Voltage	V_{CC} = Max	2			V
V_{IL}	Low Level Input Voltage	V_{CC} = Max			0.8	V
I_{IH}	High Level Input Current	V_{CC} = Max., V_I = 2.7V			20	μA
I_I	Max High Input Current	V_{CC} = Max., V_{IH} = 7V			100	μA
I_{IL}	Low Level Input Current	V_{CC} = Max., V_I = 0.4V			−200	μA
I_{CC}	TTL Supply Current	V_{CC} = Max.		20	35	mA

ECL INPUTS/OUTPUTS DP8516/DP8516-350 (100K) V_{EE} = −4.2V Output Load = 50Ω to −2V (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	(Notes 1, 2)	−1025	−950	−880	mV
V_{OL}	Output Low Voltage	(Notes 1, 2)	−1810	−1700	−1620	mV
V_{IH}	Input High Voltage	(Notes 1, 2)	−1165		−880	mV
V_{IL}	Input Low Voltage	(Notes 1, 2)			−1475	mV
V_{BB}	Bias Output	(Notes 1, 2) I_{SINK}/I_{SOURCE} < 1 mA	−1465	−1300	−1175	mV
I_{IH}	High Level Input Current	V_{IN} = V_{IH}(max)			100	μA
I_{IL}	Low Level Input Current	V_{IN} = V_{IL}(min)	−100		100	μA

ECL INPUTS/OUTPUTS DP8515/DP8515-350 (10K) V_{EE} = −5.2V Output Load = 50Ω to −2V (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	0°C	−1000		−840	mV
		25°C (Note 2)	−960		−810	mV
		70°C	−900		−720	mV
V_{OL}	Output Low Voltage	0°C	−1870		−1665	mV
		25°C (Note 2)	−1850		−1650	mV
		70°C	−1830		−1625	mV
V_{IH}	Input High Voltage	0°C	−1145		−840	mV
		25°C (Note 2)	−1105		−810	mV
		70°C	−1045		−720	mV
V_{IL}	Input Low Voltage	0°C			−1490	mV
		25°C (Note 2)			−1475	mV
		70°C			−1450	mV
V_{BB}	Bias Output	0°C	−1480		−1155	mV
		25°C (Note 2)	−1465		−1115	mV
		70°C	−1440		−1055	mV
		I_{SINK}/I_{SOURCE} < 1 mA				
I_{IH}	High Level Input Current	V_{IN} = V_{IH}(max)			100	μA
I_{IL}	Low Level Input Current	V_{IN} = V_{IL}(min)	−100		100	μA

ECL 10K/100K SUPPLIES

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	ECL Current	V_{CC} = Max., Outputs Open		100	163	mA

Note 1: These ECL 100K specifications are guaranteed over the temperature range 0°C to 70°C.

Note 2: ECL voltage levels are referenced to V_{CCO}.

Note 3: TTL voltage levels are referenced to TTL Ground. TTL specifications are guaranteed over the temperature range 0°C to 70°C.

AC Electrical Characteristics

Symbol	Parameter	Conditions	Min		Typ		Max		Units
			DP8515/16	-350	DP8515/16	-350	DP8515/16	-350	
f_{MAX}	PIXEL CLK		225	350	350 (Note 1)	450 (Note 2)			MHz
f_{MAX}	WR Input		20	30					MHz
f_{MAX}	PARALLEL LOAD (read)	FIFO Mode	14	25 (30)					MHz
f_{MAX}	PARALLEL LOAD (read)	Transparent Mode	20	30					MHz
t_{PD1}	PIXEL CLK to S0 or S8	wrt PIXEL CLK POS EDGE			2.0	1.8	3.0	2.7	ns
t_{PD0}	PIXEL CLK to S0 or S8	wrt PIXEL CLK POS EDGE			2.0	1.8	3.0	2.7	ns

Note 1: f_{MAX} is not tested but is assured by correlation with characterization data. f_{MAX} of 350 MHz typical is at room temp. and 5.0V. Typical parts run at 310 MHz over temp. and V_{CC}.

Note 2: f_{MAX} is not tested but is assured by correlation with characterization data. f_{MAX} of 450 MHz typical is at room temp. and 5.0V. Typical parts run at 400 MHz over temp. and V_{CC}.

Circuit Operation

When the VSR is powered up, on chip power up reset circuitry resets the FIFO write and read pointers. This is only necessary if the FIFO mode (M0 = 0, M1 = 1) is selected, although it is performed on every power up. Although no random information in the FIFO is cleared, this is not necessary since it will be written over. With the FIFO reset, and if the FIFO mode is selected, the circuit is now ready for a write operation into word number one. If, during the operation of the circuit, a reset of the FIFO is desired, this may be accomplished by applying a low pulse to the M1 input. To ensure proper internal circuit operation, starting this FIFO "reset" operation while the PARALLEL LOAD input is in a HIGH state is NECESSARY. Again, the circuit must be in the FIFO mode to do this.

Writing into the FIFO is accomplished on the positive edge of the WR input. When this occurs, data at the input which has met the specified setup time will be latched into the first word of the FIFO. Up to four write operations may be performed without a read operation; that is, without a positive edge of the PARALLEL LOAD input. If more than four consecutive write operations occur, previously written data will be overwritten. The WR input and the PARALLEL LOAD input may be asynchronous and writing and reading may occur simultaneously. However, when the FIFO is empty, if the user wants to read the new data about to be entered, then the read operation must occur no sooner than one WR to Parallel Load Setup Time after the write operation. If this condition is not met, the old data will be read from the FIFO.

So long as the $\overline{\text{ENABLE}}$ input is low, reading data from the FIFO will not be inhibited. Reading data out of the FIFO is accomplished on the positive edge of the first PIXEL CLOCK following a positive edge of the PARALLEL LOAD input which has met the specified setup time. The first word read will be the first word written into the FIFO. The sixteen bit word will be parallel loaded into the ECL shift register and Bit 0 will appear at the S0 SERIAL OUTPUT. Subsequent PIXEL CLOCK positive edges will shift the data out of the shift register so long as the HOLD input is low; if this input is high the shifting of data by the PIXEL CLOCK will be inhibited. With a positive edge of the PARALLEL LOAD input occurring every sixteen PIXEL CLOCKS, sixteen bit words will be shifted out of the shift register. If more than sixteen PIXEL CLOCKS occur before a PARALLEL LOAD positive edge, then the information at the SERIAL INPUT pin will be shifted out of the register. This input can be used to cascade shift registers for longer word lengths.

When the M0 input is low and the M1 input is low, the FIFO depth is reduced to one word; that is, the DATA inputs become edge triggered flip flops. With the inputs configured as edge triggered flip flops, data which meets the specified setup time is accepted on the positive edge of the WR input. As is the case in the four word FIFO mode, data will be loaded into the ECL shift register on the first positive edge of the PIXEL CLOCK following a positive edge of the PARALLEL LOAD input. Since the FIFO depth is one word, it is essential that each write operation precedes a read operation by the WR to Parallel Load Setup Time. Also, in this mode, every write operation must be followed by a read operation if the user does not want to write over any data. All of the operations pertaining to the shift register remain the same in this mode as in the four word FIFO mode.

When the M0 input is high, and the M1 input is at any value, the FIFO is disconnected and the data inputs become transparent latches. In the transparent latch mode information at the data inputs is passed through to the shift register parallel load inputs so long as the WR input is low. When the WR input is taken high, the information at the data inputs is latched into the input buffers.

As in the other operating modes, data is loaded into the shift register on the positive edge of the first PIXEL CLOCK following a positive edge of the PARALLEL LOAD input. If the WR input remains low, new data is loaded into the shift register following every PARALLEL LOAD/PIXEL CLOCK positive edge pair providing the data meets the setup time with respect to the PARALLEL LOAD input. If the WR input returns high after latching in the information at the data inputs, PARALLEL LOAD/PIXEL CLOCK positive edge pairs will load the shift register with the latched data. All of the operations pertaining to the shift register remain the same in this mode as in the other modes.

The OUTPUT CONTROL and OUTPUT LEVEL CONTROL inputs allow the user to manipulate the shift register data if he so chooses. With the OUTPUT CONTROL input high, the last bits of the shift register, that is the SERIAL OUTPUT, S0, and the S8 bit, are prohibited from shifting while all the other bits are being shifted by the PIXEL CLOCK. This has the effect of performing a basic scrolling function on the screen. The OUTPUT LEVEL CONTROL input determines to what level the last bit is set. When using the OUTPUT CONTROL, even though the eighth bit is held at the output, internally, information will be shifted through this bit.

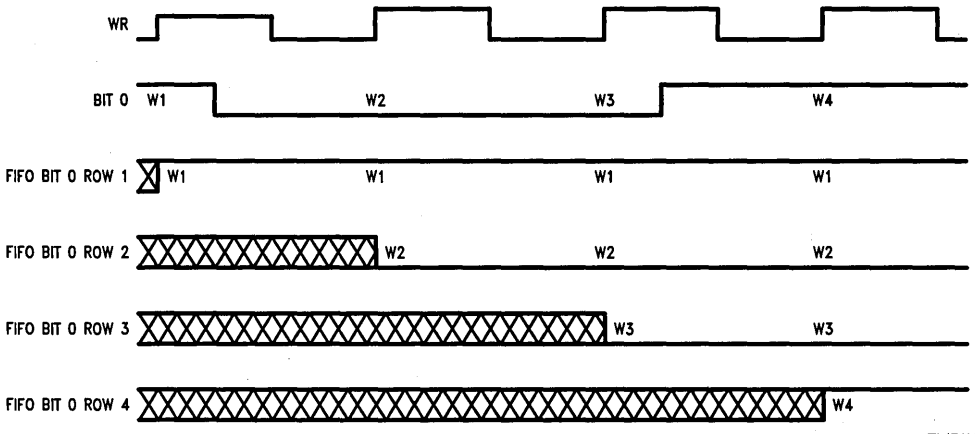
Circuit Operation (Continued)

As mentioned above, the HOLD input must be low for the PIXEL CLOCK to be able to shift data out of the shift register. A basic zoom feature may be performed by holding the HOLD input at a high level. When the HOLD input is held high for a certain number of PIXEL CLOCK periods, the same information will be present at the shift register output for the duration of the hold time. This has the effect of "stretching" the information from one pixel to multiple pixels.

The VSR may be used in systems employing word lengths other than 16 bits. For example, in a 32-bit system two VSR chips may be cascaded to form a 32-bit word. The S0 output of the first VSR is fed into the SI input of the second to accomplish this. In systems using 8 bit words, the S8 output may be used in addition to the S0 output resulting in one VSR being used for two words and cutting in half the number of packages required to do the parallel to serial conversion.

Any word length can be used so long as the PIXEL CLOCK rate is equal to the PARALLEL LOAD rate times the word length.

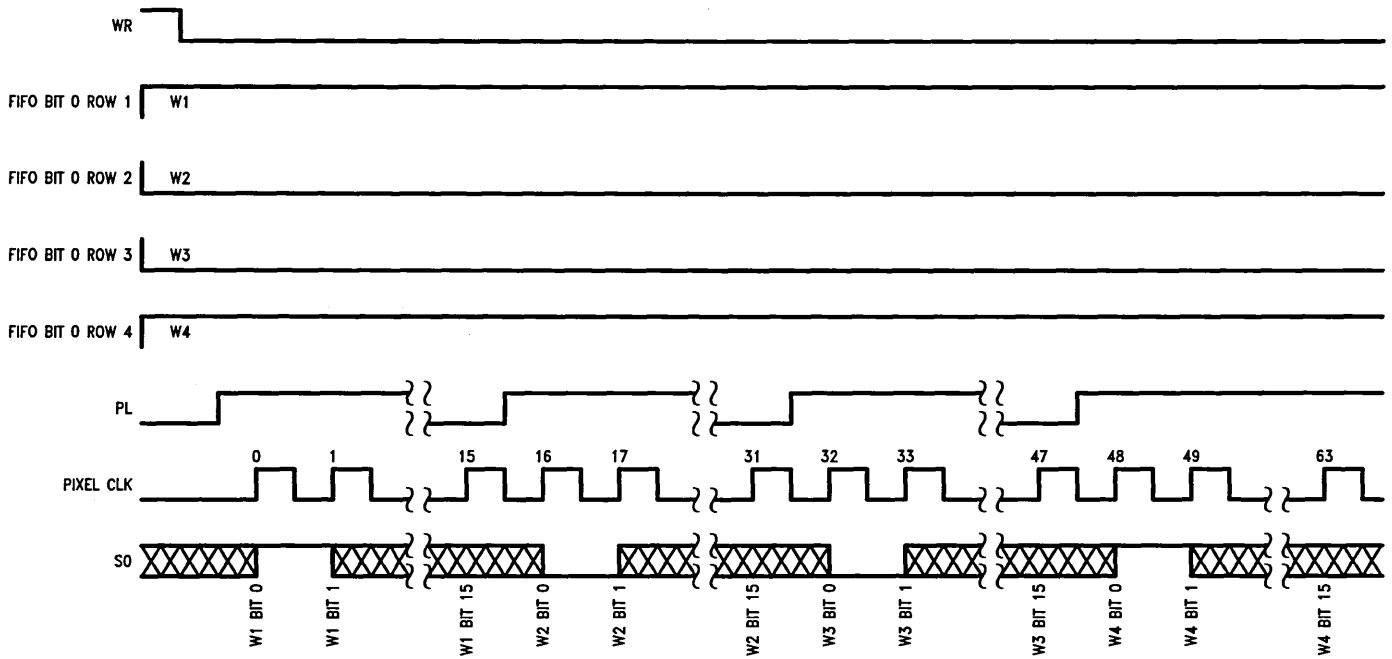
Four Word FIFO Mode (M0 = 0, M1 = 1)
Inputting four words without reading



TL/F/8684–3

FIGURE 1

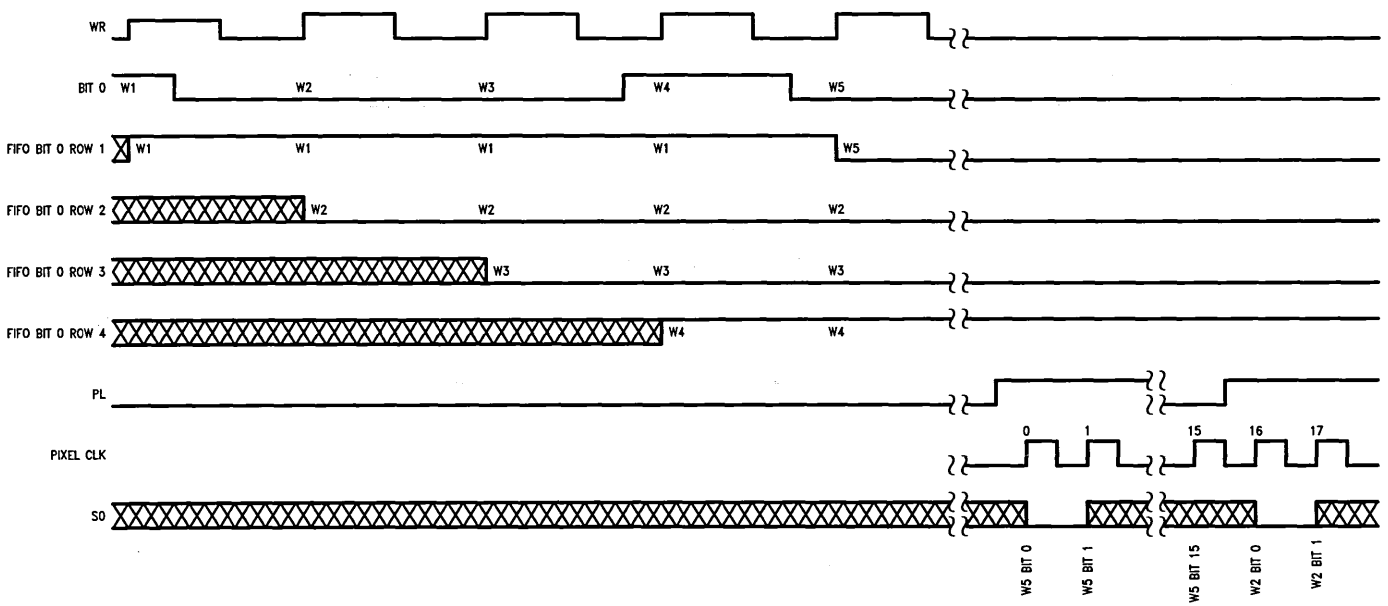
Four Word FIFO Mode (M0 = 0, M1 = 1)
Reading four words after writing four words



TL/F/8684–4

FIGURE 2

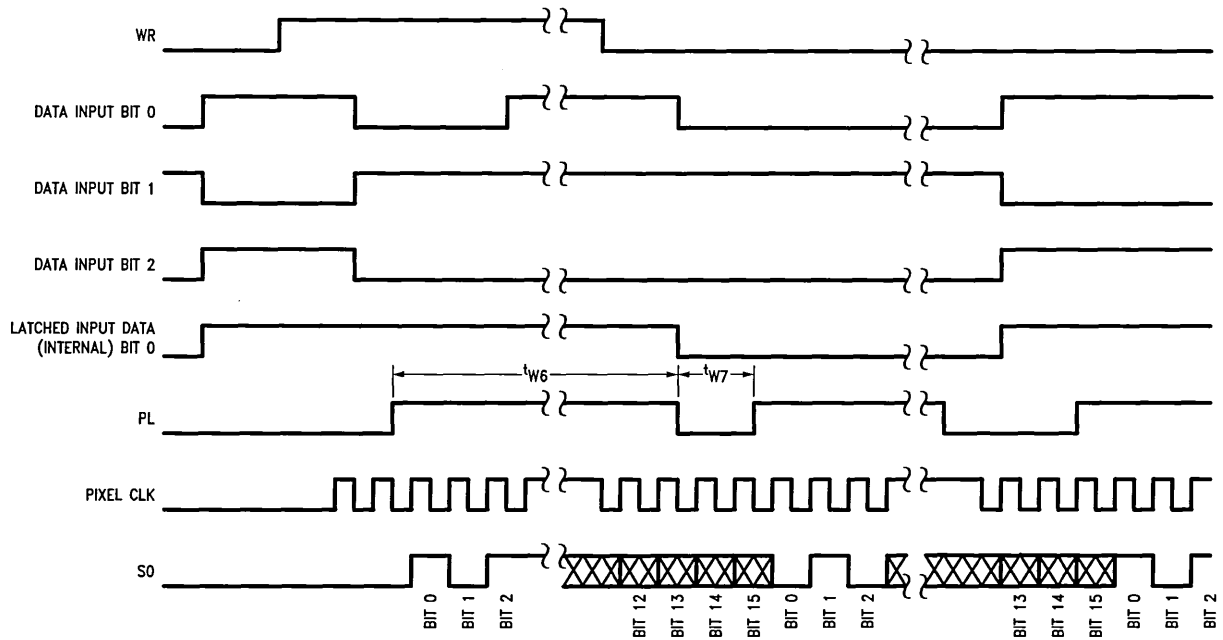
Four Word FIFO Mode (M0 = 0, M1 = 1)
Word 1 written over



TL/F/8684–5

FIGURE 3

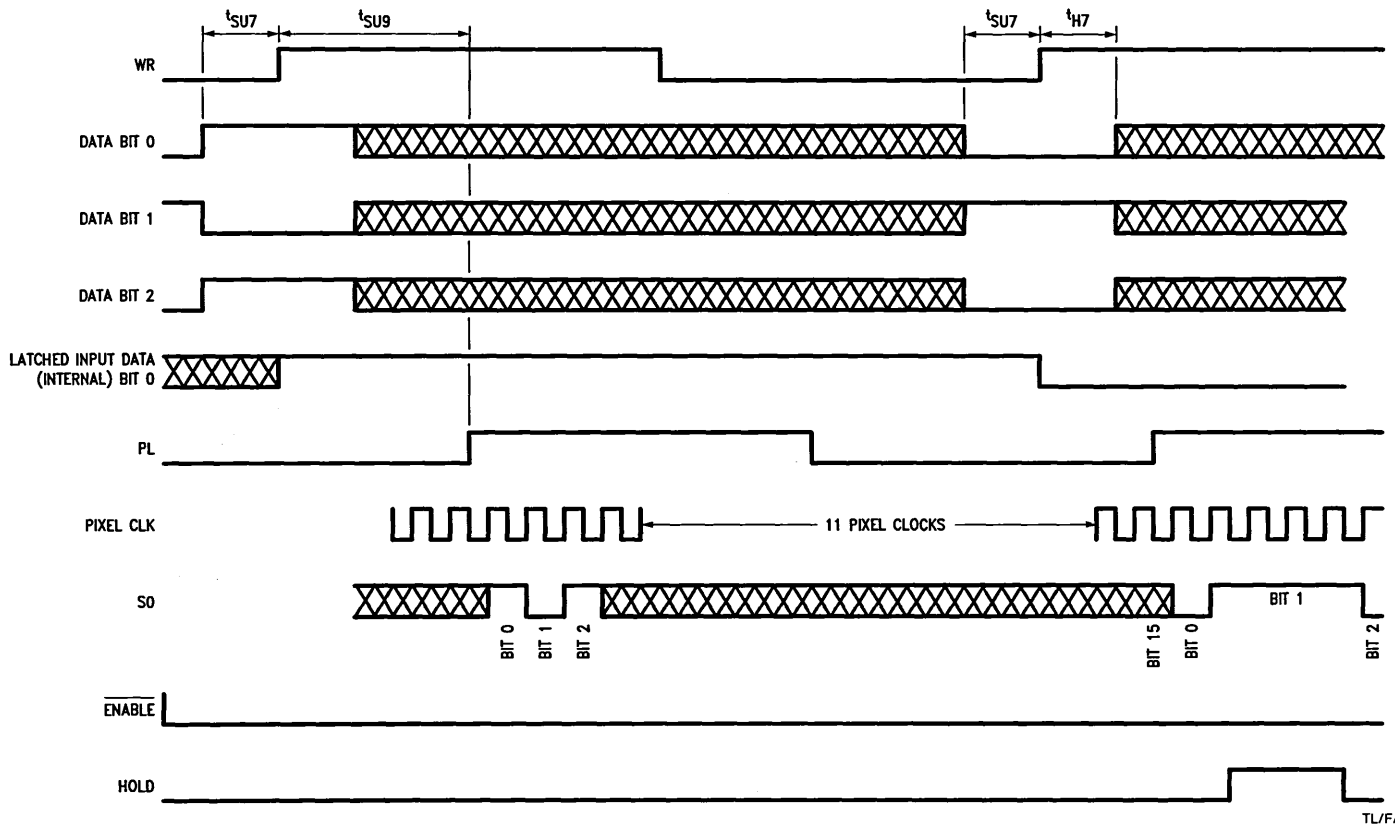
Transparent Latch Mode (M0 = 1, M1 = X)



TL/F/8684–6

FIGURE 4

One Word FIFO (D Flip Flop) Mode (M0 = 0, M1 = 0)

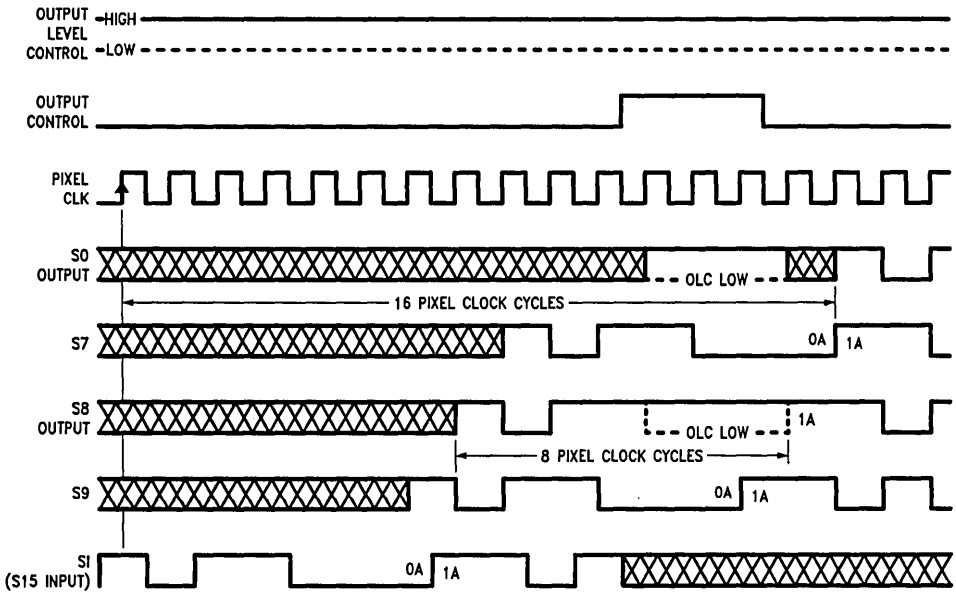


TL/F/8684–8

FIGURE 5

Circuit Operation (Continued)

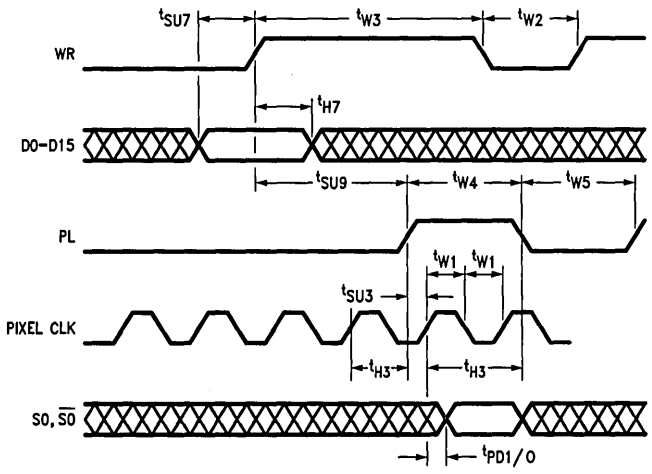
Shift Register Operation with Output Control



TL/F/8684–17

FIGURE 6

FIFO Timing Requirements

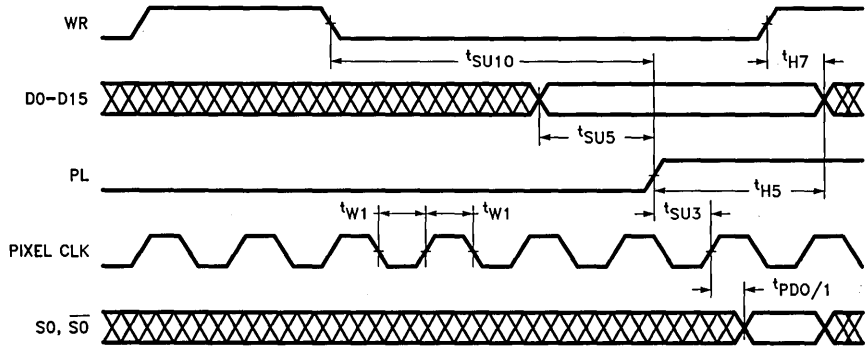


TL/F/8684–7

FIGURE 7

Circuit Operation (Continued)

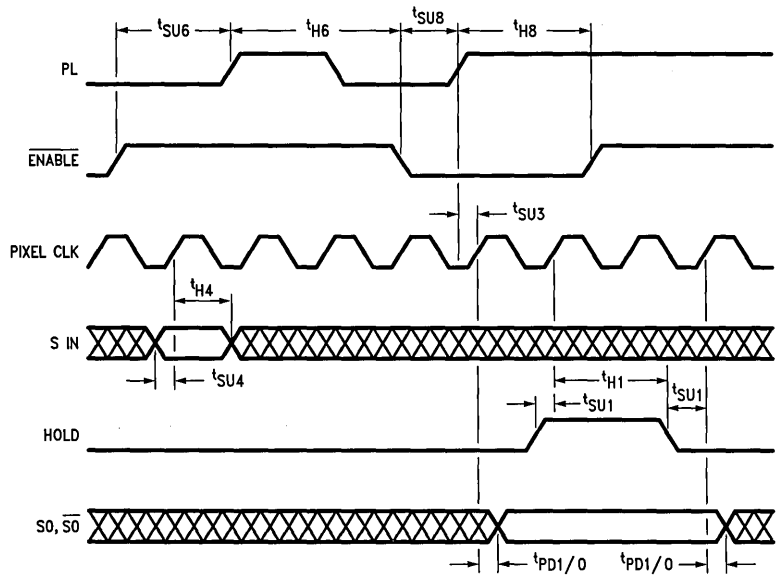
Transparent Latch Timing Requirements



TL/F/8684–16

FIGURE 8

Shift Register Timing Requirements

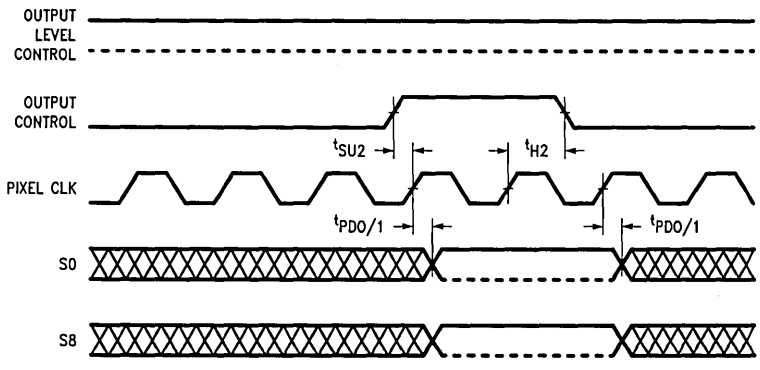


TL/F/8684–9

FIGURE 9

Circuit Operation (Continued)

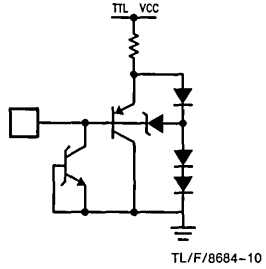
Shift Register Timing Requirements



TL/F/8684-18

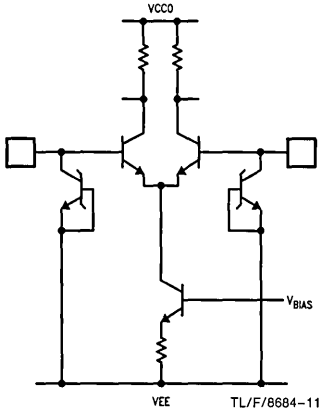
FIGURE 10

Equivalent Input/Output Schematics



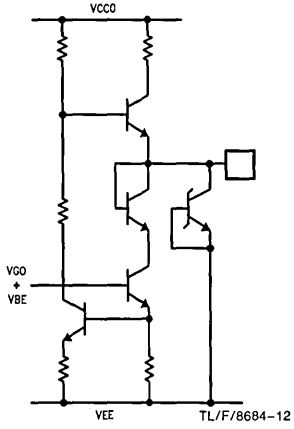
TL/F/8684-10

FIGURE 11. TTL Inputs



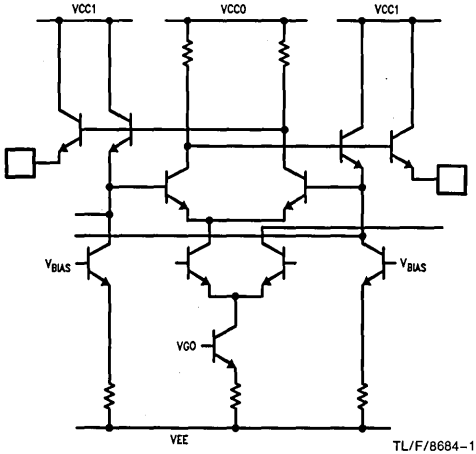
TL/F/8684-11

FIGURE 12. ECL Inputs



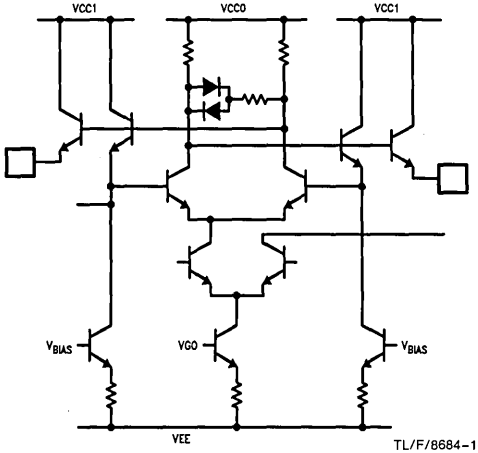
TL/F/8684-12

FIGURE 13. V_{BB} Output



TL/F/8684-13

FIGURE 14. DP8515/DP8515-350 10K ECL Output



TL/F/8684-14

FIGURE 15. DP8516/DP8516-350 100K ECL Output

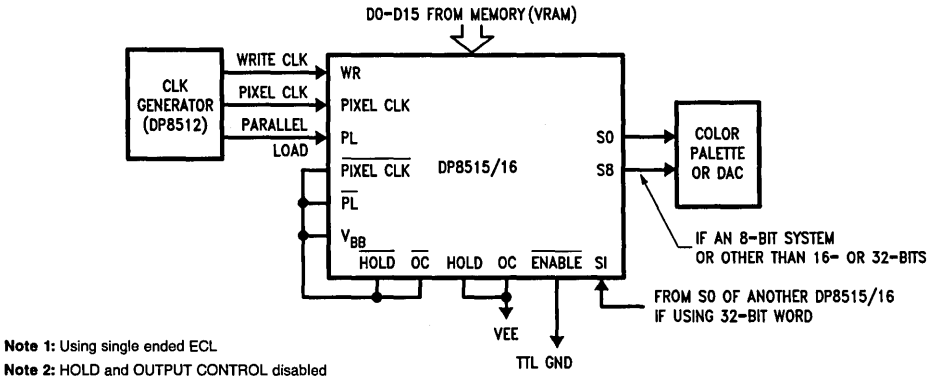
Connections to the DP8515/16

Figure 16 is a typical connection diagram for the VSR. Not shown in this diagram are the power connections. The data inputs, D0–D15, come from memory which may be Video Rams as an example. The clock signals are derived from clock generator circuitry such as National Semiconductor's DP8512. The VSR is capable of receiving differential ECL inputs. If differential use is not desired, the unused inputs may be tied to the V_{BB} reference which is provided as an output on the VSR. Although *Figure 16* shows the PIXEL CLOCK and PARALLEL LOAD inputs as single ended signals, the DP8512 provides these as differential outputs.

The ECL outputs, S0 and S8, are differential. Again, the user has the option of using these single ended if he so chooses. In systems where words other than 8 or 16 bits in length are used, the SI inputs may be fed from the S0 outputs of another VSR in order to modify the word length, such as increasing the length to 32 bits.

Figure 16 shows the part being continuously enabled by having the $\overline{EN}$ input tied to TTL ground. When this is done the clock generator circuitry should be able to inhibit the PARALLEL LOAD signal while a screen retrace is in progress. Another configuration might be to use the $\overline{ENABLE}$ input to gate the PARALLEL LOAD input. In this mode the clock generator circuitry must still ensure that the PARALLEL LOAD signal has the proper phase relationship with respect to the video sync signal. By using the $\overline{ENABLE}$ signal to gate the PARALLEL LOAD signal, the PARALLEL LOAD signal may be selectively gated to various video shift registers.

Figure 17 shows how when word lengths other than 32, 16, or 8 bits are used, several VSR circuits can be interfaced to reduce the total number of shift registers required for a system. In the example shown, three VSR circuits are used to shift two 24-bit words. Similar configurations can be used for other word lengths.



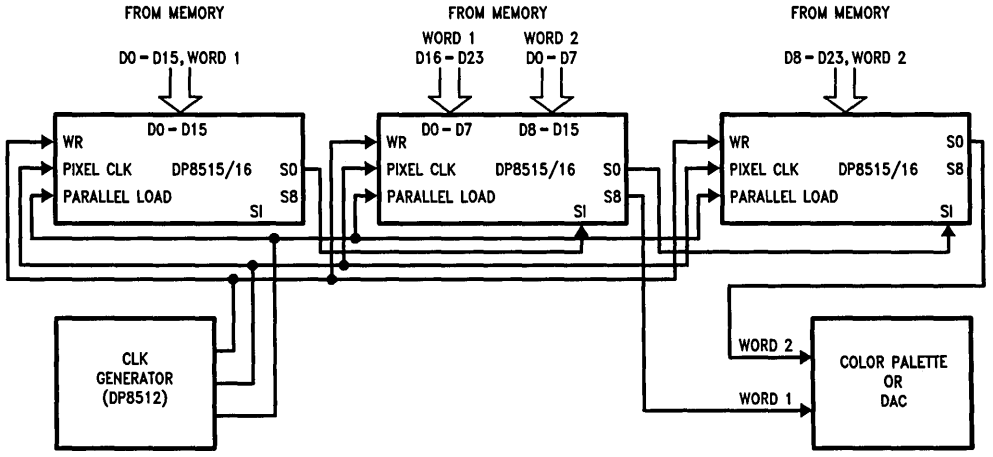
Note 1: Using single ended ECL

Note 2: HOLD and OUTPUT CONTROL disabled

Note 3: Device continuously enabled

TL/F/8684–15

FIGURE 16. Typical Connection to the DP8515/DP8515-350/DP8516/DP8516-350



TL/F/8684–19

FIGURE 17. DP8515/DP8515-350/DP8516/DP8516-350 Interconnection for 24-bit Word

National Semiconductor

PRELIMINARY

DP8520/DP8521/DP8522 microCMOS Programmable 256k/1M/4M Video RAM Controller/Drivers

General Description

The DP8520/21/22 provide single chip interfaces between dual port video RAM (and/or conventional DRAM) and any 8-, 16-, and 32-bit microprocessor as well as any specialized graphics processor chip or system. The DP8520/21/22 perform all control and timing functions required by both video RAM (VRAM) and conventional DRAM.

The DP8520/21/22 are easily programmed so that their control logic configuration may be optimized to interface virtually any graphics controller, microprocessor, bus, or system to any VRAMs up to the 4 Mbit x 4 variety, eliminating the need for external support circuits.

The DP8520/21/22 generate all required access control signal timing and automatically refresh all VRAMs as required. Furthermore, they perform all access/refresh arbitration and insert wait states into microprocessor access cycles when necessary during arbitration conflicts. All types of VRAM access cycles are supported, including VRAM transfer cycles from VRAM to the shift register and vice-versa (i.e., read, write, pseudo write transfer cycles). Control signal pulse widths are adjustable so that system timing may be optimized for clock rates to 20 MHz and beyond.

The DP8520 and DP8521 differ only in the number of address outputs, 9 and 10 respectively.

The DP8522 has 11 address outputs and has additional control circuitry to support two access ports to VRAM. This simplifies dual accessing (sometimes referred to as dual-porting) where two entities both access a common memory. Arbitration between these ports is done on-chip.

Controller	# of Pins (PLCC)	# of Address Outputs	Largest VRAM Possible
DP8520	68	9	256 kbit
DP8521	68	10	1 Mbit
DP8522	84	11	4 Mbit

Features

- Controls all Video RAMs up to 4 Mbit VRAMs (DP8522), 1 Mbit (DP8521), 256 kbit (DP8520)
- Allows no-wait state operation at frequencies of 10 MHz and above
- Can directly address and drive up to 64 Mbytes of VRAM using 4 Mbit VRAMs (DP8522), 16 Mbytes using 1 Mbit VRAMs (DP8521), 4 Mbytes using 256 kbit VRAMs (DP8520)

Dual Accessing Using the DP8522

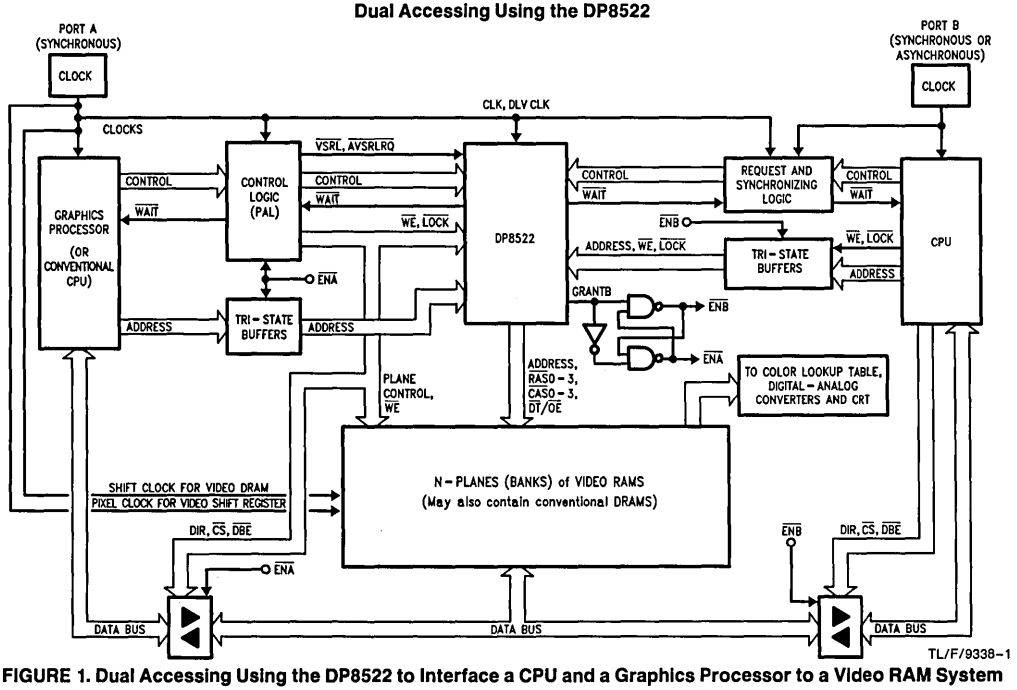


FIGURE 1. Dual Accessing Using the DP8522 to Interface a CPU and a Graphics Processor to a Video RAM System

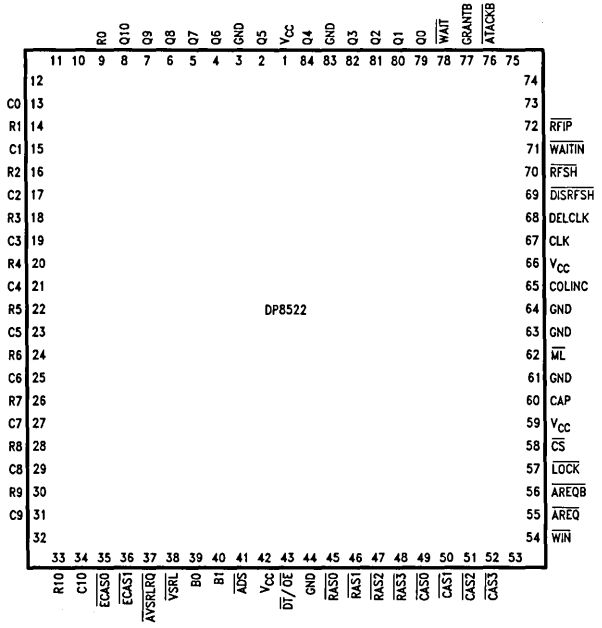
Features (Continued)

- On board port A access/port B access/refresh arbitration logic
- Direct interface to all major microprocessors as well as any specialized graphics processor chip (or system)
- Built in high precision delay line
- CMOS process for low power consumption
- All inputs are TTL compatible
- Programmable $\overline{\text{WAIT}}/\overline{\text{READY}}/\overline{\text{DTACK}}$ output to insert WAIT states into microprocessor access cycles, including burst mode accesses
- Dynamically variable wait state insertion (allows different number of wait states for READS and WRITES, etc.)
- Byte write capability up to 16 bits on chip
- Programmable VRAM row address hold time and column address setup time allows use with fast or slow VRAMs
- Programmable $\overline{\text{RAS}}$ low time during refresh
- Programmable $\overline{\text{RAS}}$ precharge time
- Programmable refresh period
- Staggered Refresh available
- Burst refresh available
- Scrubbing during refresh available with on-chip row, column and bank counters for VRAM systems employing error detection & correction
- 4 $\overline{\text{RAS}}$ and 4 $\overline{\text{CAS}}$ drivers
- Programmable $\overline{\text{RAS}}/\overline{\text{CAS}}$ configuration for maximum drive capability
- Supports all nibble, page and static column modes of operation
- Automatic column address increment on-chip allows fast multiple word accesses within a page after initial address is specified
- Allows memory accesses to different banks to be interleaved
- 84 pin PLCC package (DP8522)
- 68 pin PLCC package (DP8521)
- 68 pin PLCC package (DP8520)
- For non-video DRAM applications see the DP8420/21/22 datasheet

DP8522 Pins			DP8521 Pins*	
Input/ Output	**# of Pins**	**Pin Name**	**# of Pins**	**Pin Name**
I	11	R0–10	10	R0–9
I	11	C0–10	10	C0–9
O	11	Q0–10	10	Q0–9
O	4	$\overline{\text{RAS}}$0–3	4	
O	4	$\overline{\text{CAS}}$0–3	4	
I	2	B0, B1	2	
I	4	$\overline{\text{ECAS}}$0–1	2	
I	1	$\overline{\text{AVSRLRQ}}$	1	
I	1	$\overline{\text{VSRL}}$	1	
I	1	$\overline{\text{WIN}}$	1	
O	1	$\overline{\text{DT}}/\overline{\text{OE}}$	1	
I	1	$\overline{\text{AREQ}}$	1	
I	1	$\overline{\text{AREQB}}$	—	
I	1	COLINC (EXTENDRF)	1	
I	1	$\overline{\text{ADS}}$	1	
I	1	CLK	1	
I	1	DELCLK	1	
I	1	$\overline{\text{CS}}$	1	
O	1	$\overline{\text{WAIT}}$ ($\overline{\text{DTACK}}$)	1	
O	1	$\overline{\text{ATACKB}}$	—	
O	1	GRANTB	—	
I	1	$\overline{\text{LOCK}}$	—	
I	1	$\overline{\text{ML}}$	1	
I	1	$\overline{\text{RFSH}}$	1	
O	1	$\overline{\text{RFIP}}$	1	
I	1	$\overline{\text{WAITIN}}$	1	
I	1	$\overline{\text{DISRFSH}}$	1	
I	1	CAP	1	
I	10	VCC, GND	9	
	76 pins total		68 pins total	

*Note that the DP8520 is the same as the DP8521 except that there is no Q9 address output (only Q0–8).

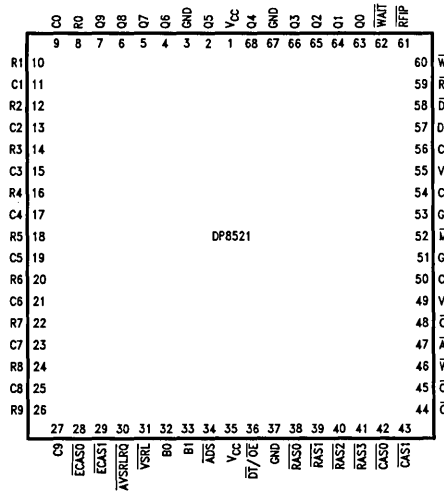
Connection Diagrams



TL/F/9338-2

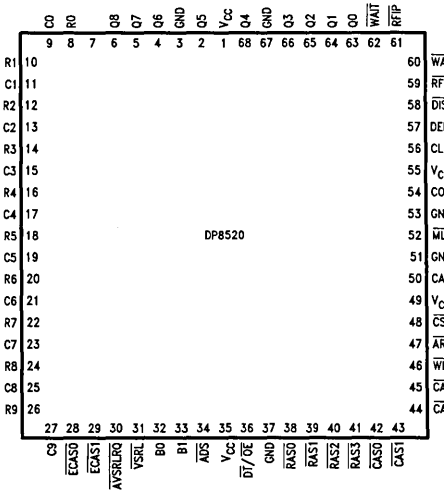
(Top View)
FIGURE 2

Order Number DP8522V
See NS Package Number V84A



TL/F/9338-3

(Top View)
FIGURE 3



TL/F/9338-4

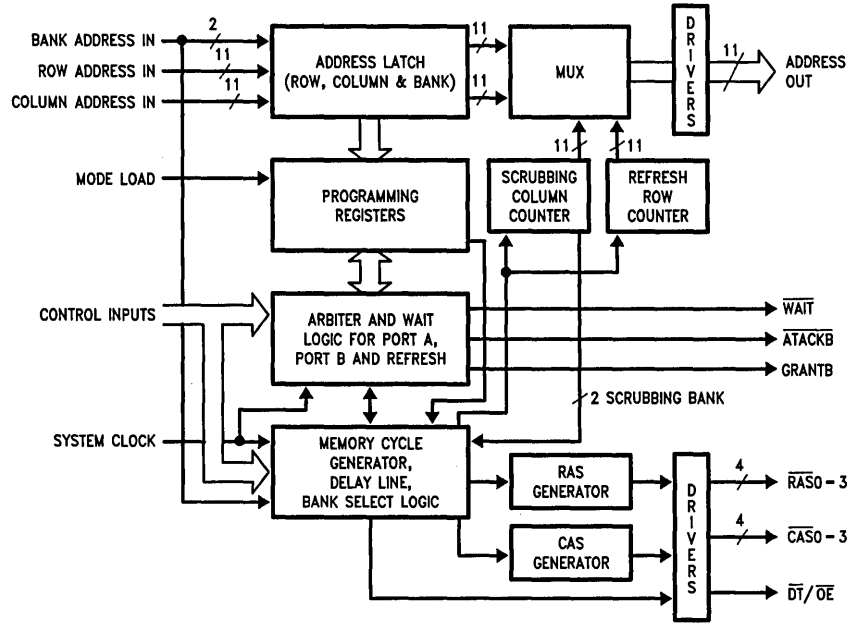
(Top View)
FIGURE 4

Order Number DP8520V or DP8521V
See NS Package Number V68A

1

Block Diagrams

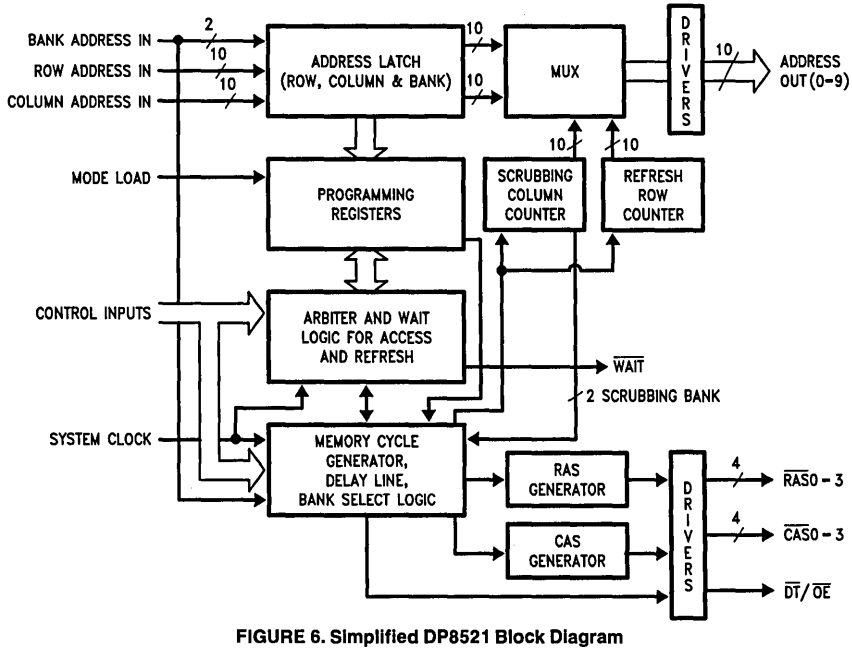
DP8522
VRAM Controller



TL/F/9338-5

FIGURE 5. Simplified DP8522 Block Diagram

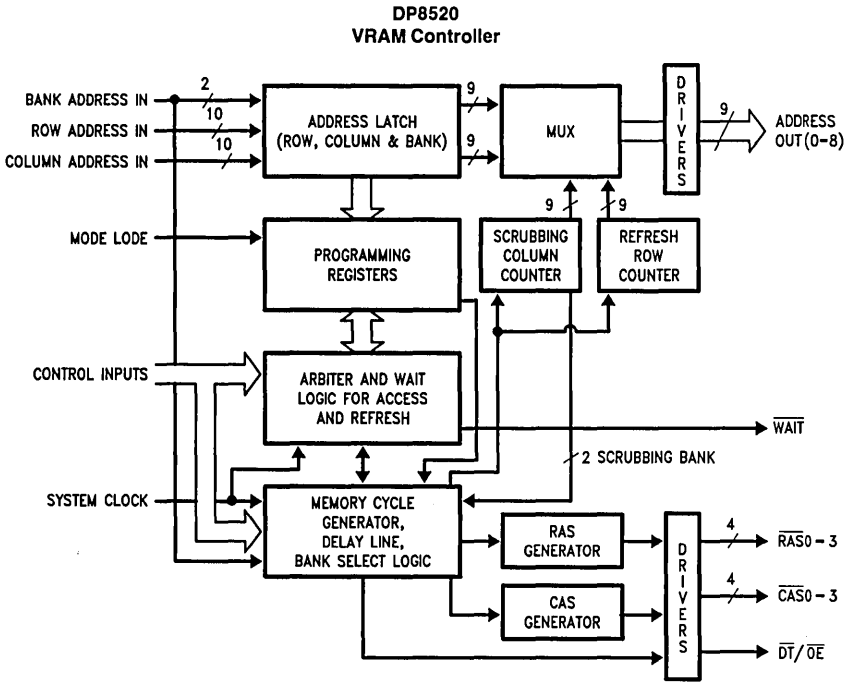
DP8521
VRAM Controller



TL/F/9338-6

FIGURE 6. Simplified DP8521 Block Diagram

Block Diagrams (Continued)



TL/F/9338-7

FIGURE 7. Simplified DP8520 Block Diagram

Table of Contents

Table of Contents (Continued)

1.0 DP8522, DP8521, DP8520 Pin Definitions

# of Pins	Name	Input/ Output	Description
11, 10, 10 11, 10, 10	R0–10, 9, 9 C0–10, 9, 9	I I	Address inputs—multiplexed to address outputs during an access. Also used to program the chip when $\overline{ML}$ is low
11, 10, 9	Q0–10, 9, 8	O	Address outputs—provide the access or refresh row and column inputs to the VRAMs
4	$\overline{RAS}$0–3	O	Row Address Strobes
4	$\overline{CAS}$0–3	O	Column Address Strobes
2	B0, B1	I	Bank Selects—select the bank of VRAM to be accessed depending on the $\overline{RAS}$, $\overline{CAS}$ configuration mode
2	$\overline{ECAS}$0–1	I	$\overline{CAS}$ enables—enables for individual $\overline{CAS}$ outputs; these inputs are useful in byte write operations (for enabling the individual $\overline{CAS}$s) and for nibble, page mode applications (for toggling $\overline{CAS}$) or for delaying $\overline{CAS}$ going low. $\overline{ECAS}$0 must be low for either $\overline{CAS}$0 or $\overline{CAS}$1 to go low during an access. $\overline{ECAS}$1 must be low for either $\overline{CAS}$2 or $\overline{CAS}$3 to go low during an access.
1	$\overline{AVSRLRQ}$	I	Advanced Video Shift Register Load Request—This must precede the $\overline{VSRL}$ input going low by the amount of time necessary to guarantee that any currently executing access and pending refresh can finish. This input disables Port B and refresh requests until four CLK periods after $\overline{VSRL}$ has transitioned low. This input may be held low until the video RAM transfer cycle is completed or may be momentarily pulsed low (tPAVL).
1	$\overline{VSRL}$	I	Video Shift Register Load—This input causes the $\overline{DT}$ output to transition low immediately. Therefore, when executing a video RAM shift register load, $\overline{VSRL}$ transitions low before $\overline{RAS}$ goes low. The $\overline{DT}$ output will transition high from $\overline{VSRL}$ going high or four CLK periods (rising clock edges) from $\overline{VSRL}$ going low, whichever occurs first. $\overline{VSRL}$ low also disables the $\overline{WIN}$ input from affecting the $\overline{DT}/\overline{OE}$ logic, until the video shift register load access is over.
1	$\overline{WIN}$	I	Write enable input—determines if $\overline{CAS}$ is delayed during an access (if delay $\overline{CAS}$ during write accesses is programmed)
1	$\overline{DT}/\overline{OE}$	O	Data Transfer/Output Enable—This output transitions low before $\overline{RAS}$ goes low and transitions high before $\overline{RAS}$ goes high during a video RAM shift register load operation (see $\overline{VSRL}$ pin description). During normal read and write accesses this output is held high. Also see section 22 number 3 for more information.
1	$\overline{AREQ}$	I	Access Request—ends access $\overline{RAS}$ for port A; in conjunction with $\overline{ADS}$ allows interleaving
1, –, –	$\overline{AREQB}$	I	Access Request B—latches row, column and bank address if so programmed. This input also requests and terminates access for port B

1.0 DP8522, DP8521, DP8520 Pin Definitions (Continued)

# of Pins	Name	Input/ Output	Description
1	COLINC (EXTENDRF)	I	Increment Column Address, (Extend Refresh)—during an access, toggling this pin increments the latched column address; during refresh this pin allows $\overline{RAS}$ and $\overline{CAS}$ low time to be extended beyond the normal refresh low time so that an error found while scrubbing can be corrected with a read-modify-write cycle
1	$\overline{ADS}$	I	Address Strobe—latches row, column and bank address programmed; this input also initiates an access for port A
1	CLK	I	CPU clock—system clock input; access requests must be synchronous with this clock; this clock is used internally for arbitration and timing purposes
1	DELCLK	I	Delay Line Clock—this clock may be asynchronous to the CPU clock, but should be a multiple of 2 mega-hertz (see section 8)
1	$\overline{CS}$	I	Chip Select— this input must be low to enable an access
1	$\overline{WAIT}$ ($\overline{DTACK}$)	O	WAIT (DATA TRANSFER ACKNOWLEDGE) output—this output can be programmed to insert wait states into a CPU access cycle when necessary
1, –, –	$\overline{ATACKB}$	O	Advanced Transfer Acknowledge B—can be used to insert wait states into port B accesses during arbitration conflicts
1, –, –	GRANTB	O	GRANT—indicates which port is currently granted ("0"-port A, "1"-port B)
1, –, –	$\overline{LOCK}$	I	LOCK—locks the currently granted port when low
1	$\overline{ML}$	I	Mode Load—this input enables the internal register that stores the chip's programming information; see section 3.0.
1	$\overline{RFSH}$	I	External Refresh Request—requests a single refresh (low one clock or less) or burst refresh (refreshing continues until $\overline{RFSH}$ returns high) provided that $\overline{DISRFSH}$ is low
1	$\overline{RFIP}$	O	Refresh in Progress—this output goes low just prior to a refresh cycle and goes high when the refresh is completed; during a burst refresh this output stays low as long as the burst refresh is in progress; this output may be useful in an error correcting memory system to indicate that a refresh with scrubbing is in progress
1	$\overline{WAITIN}$	I	Wait input—this input adds wait states in the current access cycle, when low, as programmed by the "WADD" (WAIT ADD) mode programming bit; it is useful in systems in which particular accesses require more time (clock periods or "T" states) than a typical access (e.g. byte writes in systems employing ECC)
1	$\overline{DISRFSH}$	I	Disable automatic internal refresh—this input must be low to use the $\overline{RFSH}$ input as an external refresh request; if it is high and $\overline{RFSH}$ goes low, no refresh will be done but the refresh counter will be cleared; normally when doing a burst refresh, $\overline{RFSH}$ should go low one clock period before $\overline{DISFRSH}$ so that the refresh counter is cleared before the burst starts
1	CAP	I	Capacitor—used for PLL based delay line stabilization (Typical value = 0.1 micro farad)
10	VCC, GND	I	Supplies
76 Pins			

2.0 Power Up Reset (Auto and External)

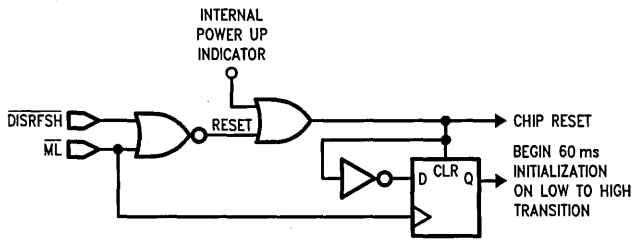


FIGURE 8. Simplified On-Chip Reset Logic and Begin Initialization Logic

All internal latches and flip-flops are cleared on power-up or when $\overline{ML}$ (mode load, used for programming the DP8520/21/22) and $\overline{DISRFSH}$ are both low for at least 16 clocks (see *Figure 8*).

After resetting the DP8520/21/22 with $\overline{ML}$ and $\overline{DISRFSH}$ both low, if the user brings $\overline{DISRFSH}$ high before $\overline{ML}$, then the low to high transition of $\overline{ML}$ will program the chip and trigger the initialization sequence as described in section 3.8. If $\overline{ML}$ is brought high before $\overline{DISRFSH}$, then the chip will not be programmed. In this case the first low to high transition of $\overline{ML}$ while $\overline{DISRFSH}$ is high will program the chip and start the initialization sequence. In both cases, the DP8520/21/22 must be programmed before using the chip.

3.0 Programming the DP8520/21/22

The DP8520/21/22 has a 22 bit programmable register. This register is loaded through the address bus: R0–9, C0–9 and B0–1. The programming bits are latched into this register by pulling $\overline{ML}$ low, putting the desired programming information on the address bus and then either initiating a "fake" access to VRAM or bringing $\overline{ML}$ high. The mode bits are latched when $\overline{AREQ}$ goes low with $\overline{CS}$ low (during a "fake" access to the VRAM), or when $\overline{ML}$ goes high, whichever happens first. All internal programming mode bits will be set to a high state while $\overline{ML}$ is low (except WAITDSEL and WAITM (0, 1)) so that the programmed mode takes effect when $\overline{ML}$ goes high; WAITDSEL and WAITM (0,1) take effect according to the address input while $\overline{ML}$ is low so that the DP8520/21/22 $\overline{WAIT}$ output allows the "fake" access to be terminated.

The inputs $\overline{ECAS0}$ and $\overline{ECAS1}$ may be used as programming bits in a future version of this chip. To be assured of complete compatibility with future versions of the DP8520/21/22, it is suggested that these inputs are both low when the chip is programmed.

3.1 DEFAULT MODE OF THE DP8520/21/22 UPON POWER UP

The DP8520/21/22 mode latch powers up in an undefined state. The system must program the DP8520/21/22 before attempting to use it.

3.2 EXTERNAL POWER UP CIRCUITRY CAN PROGRAM THE DP8520/21/22

The DP8520/21/22 could be automatically programmed during system power up by (see *Figure 9*, block diagram):

a) causing the system power up signal to TRI-STATE® the address buffers from the CPU and pull the $\overline{ML}$ input signal low on DP8520/21/22

b) tying pull-up or pull-down resistors to each input address line (R0–9, C0–9, B0–1) as appropriate to correctly program the DP8520/21/22

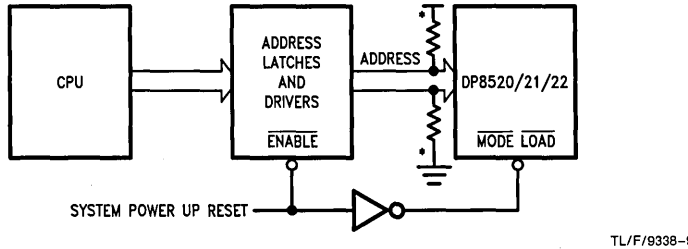
c) the power up signal going high, causing $\overline{ML}$ to go high to complete the programming sequence

3.3 PROGRAMMING THROUGH THE ADDRESS BUS

The DP8520/21/22 can be programmed using only the address bus by (see *Figure 10*, block diagram):

a) dedicating a block of the address space by tying one of the high order address bits or $\overline{CS}$ of a decoded address space to the $\overline{ML}$ input

b) doing an access within this address space ($\overline{ML}$ low); this method may be very costly to the system because it dedicates a large block of the address space to programming. Therefore, this method is recommended only if the methods mentioned in section 3.2, 3.4, and 3.5 are considered inadequate.



*Pull-Up or Pull-Down Resistors on Each Address Input

FIGURE 9. Programming the DP8520/21/22 During Power Up

3.0 Programming the DP8520/21/22 (Continued)

3.4 PROGRAMMING THROUGH THE ADDRESS BUS AND ONE BIT OF AN I/O PORT

Another way for a processor to program the DP8520/21/22 would be to (see *Figures 11* and *12*, timing and block diagrams):

a) bring $\overline{ML}$ low through an unused processor I/O port bit

b) perform a chip selected access of VRAM with the desired programming bits on the address bus (thus programming the DP8520/21/22)

c) bring $\overline{ML}$ high through the same I/O port bit used to generate it to complete the programming sequence

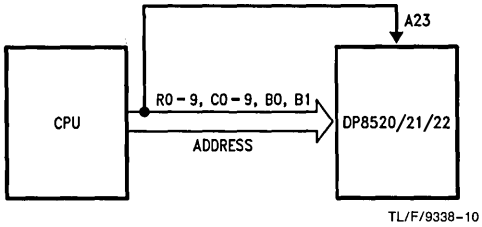


FIGURE 10. Programming the DP8520/21/22 through the Address Bus only

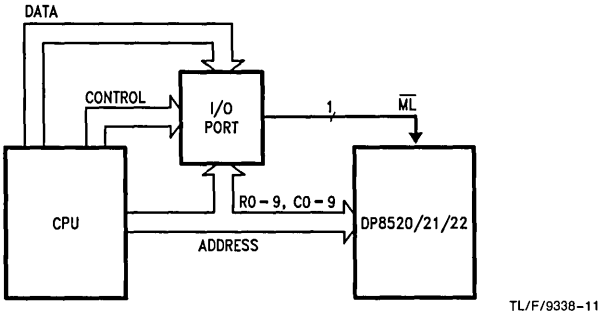


FIGURE 11. Programming the DP8520/21/22 through the Address Bus and an I/O Port

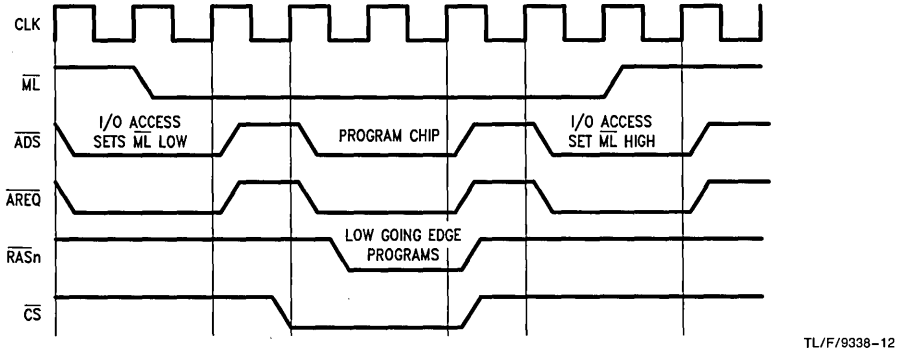


FIGURE 12. Timing of Programming the DP8520/21/22 through an I/O Port (Access Mode 1)

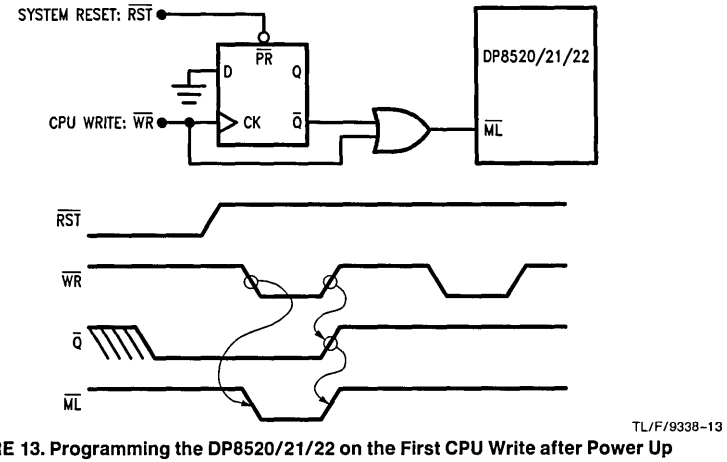


FIGURE 13. Programming the DP8520/21/22 on the First CPU Write after Power Up

3.0 Programming the DP8520/21/22 (Continued)

3.5 PROGRAMMING DURING THE FIRST SYSTEM WRITE AFTER POWER UP

A simple way for a processor to program the DP8520/21/22 would be to (see *Figure 13*, block diagram and timing):

a) have the power up reset signal preset a flip-flop which enables an "OR" gate

b) the first CPU write access will cause $\overline{ML}$ to go low

c) the write strobe going high will bring $\overline{ML}$ high programming the DP8520/21/22, and clock the flip-flop which will disable the "OR" gate so successive CPU write accesses do not re-program the DP8520/21/22.

3.6 INTERNAL PROGRAMMING MODE BITS

The 22 programming bits on the DP8520/21/22 are described below.

ADDRESS Bit(s)	Description
R0, R1	**RFPRCHGRL(0,1)** $\overline{RAS}$ low time during refresh and minimum $\overline{RAS}$ precharge time
R2, R3	**WAITM(0,1)** determines when $\overline{WAIT}$ ends ($\overline{DTACK}$ starts) such that the desired number of wait states are inserted into the initial access
R4, R5	**WBRST(0,1)** determines when $\overline{WAIT}$ ends ($\overline{DTACK}$ starts) such that the desired number of wait states are inserted during burst type accesses (using nibble or page mode VRAMs)
R6	**WADD** determines how many wait states are added to the current access (1 or 2 more wait states) via $\overline{WAITIN}$ input
R7	**WAITDSEL** $\overline{DTACK}$ or $\overline{WAIT}$ select
R8	**INTERLEAVE** allows the row addresses to be multiplexed to the VRAM controller address outputs after the column address has been held sufficiently with respect to $\overline{CAS}$ going low so that another access to a different bank can start
R9	**STAGGERED** Selects simultaneous $\overline{RAS}$ or staggered $\overline{RAS}$ during refresh
C0, C1, C2	**DIV(0,1,2)** DELCLK divisor select (divide DELCLK by 3, 4, 5, 6, 7, 8, 9, or 10 to create 2 MHz internal clock)
C3	**RFCKDIV** fine tunes refresh interval
C4, C5, C6	**CONFIG(0, 1, 2)** Error scrubbing during refresh or normal refresh select and $\overline{RAS}$, $\overline{CAS}$ configuration mode select
C7	**tASC**—select (0, 10 ns)
C8	**tRAH**—select (15, 25 ns)
C9	**DELAYCAS** Delay $\overline{CAS}$ from going low until the next rising CLK after $\overline{RAS}$ is low during a write access (when this bit is low)
B0	**ADSMODE** determines whether address latches are permanently fall-through or latch on $\overline{ADS}$ (port A granted) or $\overline{AREQB}$ (port B granted) falling edge
B1	**ACCMD** Selects access mode

3.0 Programming the DP8520/21/22 (Continued)

3.7 INTERNAL PROGRAMMING MODES

R0, R1	$\overline{RAS}$ High and Low Times	
	$\overline{RAS}$ Low Time During Refresh	Guaranteed $\overline{RAS}$ Precharge Time
0, 0	2 CLK periods (2T)	1 CLK period (1T)
0, 1	2T	2T
1, 0	3T	2T
1, 1	4T	3T

R2, R3	$\overline{WAIT}$ or $\overline{DTACK}$ Generation Modes for Non-Burst Accesses		
	If $\overline{WAIT}$ Output Chosen		If $\overline{DTACK}$ Output Chosen
	$\overline{WAIT}$ High from Access $\overline{RAS}$ Low (Non-Delayed Access)	$\overline{WAIT}$ High from Access $\overline{RAS}$ Low after Delayed Access	$\overline{DTACK}$ Low from $\overline{RAS}$ Low
0, 0	No WAIT states	0 T	0 T
0, 1	No WAIT states	½ T	½ T
1, 0	½ T	½ T	1 T
1, 1	1 T	1 T	1½ T

R4, R5	$\overline{WAIT}$ or $\overline{DTACK}$ Generation Modes During BURST Mode Accesses
	$\overline{WAIT}$ high ($\overline{DTACK}$ low) from $\overline{CAS}$ Low during Nibble or Page Mode Type Access
0, 0	No WAIT states; $\overline{WAIT}$ ($\overline{DTACK}$) stays high (low) from previous access
0, 1	½ T
1, 0	1 T
1, 1	0 T ; $\overline{WAIT}$ ($\overline{DTACK}$) goes low (high) from $\overline{CAS}$ going high and goes high (low) from $\overline{CAS}$ going low.

R6	Add Wait States to the Current Access if $\overline{WAITIN}$ is Low
0	Hold $\overline{WAIT}$ low ($\overline{DTACK}$ high) one extra clock period
1	Hold $\overline{WAIT}$ low ($\overline{DTACK}$ high) two extra clock periods
R7	**$\overline{WAIT}$ $\overline{DTACK}$ Select Mode Bit**
0	$\overline{WAIT}$ type output is selected
1	$\overline{DTACK}$ (data transfer acknowledge) type output is selected
R8	**Interleaving Mode Select**
0	Interleaved Mode: Multiplex the row address to the VRAM controller address outputs after the column address has been held sufficiently (50 ns minimum) with respect to $\overline{CAS}$ going low
1	Non Interleaved Mode: Hold the column address on the VRAM controller address outputs until $\overline{RAS}$ goes high

3.0 Programming the DP8520/21/22 (Continued)

R9	Staggered Refresh Mode Select
0	All $\overline{RAS}$ Refresh Mode: During refresh all $\overline{RAS}$s will transition low and high at the same time
1	Staggered Refresh Mode: During refresh the $\overline{RAS}$s will transition low sequentially (one clock period between each $\overline{RAS}$) one or two $\overline{RAS}$s at a time depending upon the $\overline{RAS}/\overline{CAS}$ configuration mode selected. Scrubbing is not allowed if staggered refresh is selected.

C0, C1, C2	Delay Line/Refresh Clock Divisor Select	
0, 0, 0	divide by 10	The user should choose the divisor such that the clock input DELCLK (usually the system clock, CLK) divided by the divisor will give a frequency as close as possible to 2 MHz.
0, 0, 1	divide by 6	
0, 1, 0	divide by 8	
0, 1, 1	divide by 4	
1, 0, 0	divide by 9	
1, 0, 1	divide by 5	
1, 1, 0	divide by 7	
1, 1, 1	divide by 3	

C3	Refresh Clock (Fine Tune) Divider
0	Divide above clock frequency (usually 2 MHz) by 30 to get the refresh clock period (15 μs if 2 MHz)
1	Divide above clock frequency by 26 (gives a refresh clock period of 13 μs if 2 MHz)

Note: The Refresh clock period is equal to DELCLK period X (C0, C1, C2 divisor) X (C3 divisor)

C4, C5 C6	$\overline{RAS}$ and $\overline{CAS}$ Configuration Modes
0, 0, 0	Error scrubbing during refresh; $\overline{RAS}$0–3 are brought low during an access. $\overline{CAS}$0–3 are all selected during an access but only those enabled by the corresponding $\overline{ECAS}$ can go low. B0 and B1 are not used.
0, 0, 1	No error scrubbing; $\overline{RAS}$ groups are selected by B1. B0 is not used. All $\overline{CAS}$ outputs are selected, making this mode useful for byte writing via $\overline{ECAS}$0–1 inputs and the $\overline{CAS}$0–3 outputs.
0, 1, 0	Error scrubbing during refresh; $\overline{RAS}$, $\overline{CAS}$ pairs selected by B0, B1. A particular $\overline{CAS}$ cannot go low unless its $\overline{ECAS}$ is also low. This mode can support memory interleaving.

B1	
0	$\overline{RAS}$0, 1
1	$\overline{RAS}$2, 3

B1	B0	
0	0	$\overline{RAS}$0 and $\overline{CAS}$0
0	1	$\overline{RAS}$1 and $\overline{CAS}$1
1	0	$\overline{RAS}$2 and $\overline{CAS}$2
1	1	$\overline{RAS}$3 and $\overline{CAS}$3

3.0 Programming the DP8520/21/22 (Continued)

C4, C5 C6	$\overline{RAS}$ and $\overline{CAS}$ Configuration Modes Description
0, 1, 1	No error scrubbing; $\overline{RAS}$n is selected by B0 and B1. All $\overline{CAS}$ outputs are selected, making this mode useful for byte writing via $\overline{ECAS}$0–1 inputs and the $\overline{CAS}$0–3 outputs.

B1	B0	
0	0	$\overline{RAS}$0
0	1	$\overline{RAS}$1
1	0	$\overline{RAS}$2
1	1	$\overline{RAS}$3

1, 0, 0	Error scrubbing during refresh; $\overline{RAS}$, $\overline{CAS}$ groups selected by B1. A particular $\overline{CAS}$ cannot go low unless its $\overline{ECAS}$ is also low. B0 is not used. This mode can support memory interleaving.

B1	
0	$\overline{RAS}$0, 1 and $\overline{CAS}$0, 1
1	$\overline{RAS}$2, 3 and $\overline{CAS}$2, 3

1, 0, 1	No error scrubbing; $\overline{RAS}$, $\overline{CAS}$ groups are selected B1. A particular $\overline{CAS}$ cannot go low unless its $\overline{ECAS}$ is also low. B0 is not used. This mode can support memory interleaving.

B1	
0	$\overline{RAS}$0, 1 and $\overline{CAS}$0, 1
1	$\overline{RAS}$2, 3 and $\overline{CAS}$2, 3

1, 1, 0	No error scrubbing; $\overline{RAS}$0–3 and $\overline{CAS}$0–3 are all selected during an access. Since all $\overline{CAS}$ outputs are selected, this mode is useful for byte writing via $\overline{ECAS}$0–1 inputs and the $\overline{CAS}$0–3 outputs. B0 and B1 are not used.
1, 1, 1	No error scrubbing; $\overline{RAS}$n and $\overline{CAS}$n are selected by B0 and B1. A particular $\overline{CAS}$ cannot go low unless its $\overline{ECAS}$ is also low. This mode can support memory interleaving.

B1	B0	
0	0	$\overline{RAS}$0 and $\overline{CAS}$0
0	1	$\overline{RAS}$1 and $\overline{CAS}$1
1	0	$\overline{RAS}$2 and $\overline{CAS}$2
1	1	$\overline{RAS}$3 and $\overline{CAS}$3

Note 1: The configuration modes allow $\overline{RAS}$s and $\overline{CAS}$s to be grouped such that each $\overline{RAS}$ and $\overline{CAS}$ will drive one-fourth of the total VRAM array whether the array is organized as 1, 2, or 4 banks.

Note 2: In modes 0, 2 and 4 error scrubbing is enabled during refresh. This allows a single memory access during every refresh cycle. If a single bit error is found it may be corrected and written back to memory, using the COLINC (EXTENDRF) input to extend the current error scribbing access.

Note 3: In order for a $\overline{CAS}$ output to go low during an access, it must be both selected and enabled. $\overline{ECAS}$0–1 are used to enable the $\overline{CAS}$ outputs ($\overline{ECAS}$0 enables $\overline{CAS}$0,1; $\overline{ECAS}$1 enables $\overline{CAS}$2,3). Selection is determined by the configuraton mode and B1, B0.

3.0 Programming the DP8520/21/22 (Continued)

C7	Column Address Setup Time (tASC) Mode Select
0	Select 10 ns column address setup time (minimum guaranteed)
1	Select 0 ns column address setup time (minimum guaranteed)
C8	**Row Address Hold Time (tRAH) Mode Select**
0	Select 25 ns row address hold time (minimum guaranteed)
1	Select 15 ns row address hold time (minimum guaranteed)
C9	**Delay $\overline{CAS}$ During WRITE Accesses Mode Select**
0	$\overline{CAS}$ is treated the same during WRITE or READ accesses
1	$\overline{CAS}$ will be initiated during WRITE accesses by whatever occurs last, the on-chip delay line initiating $\overline{CAS}$ or the next rising system clock (CLK) edge after $\overline{RAS}$ goes low. In other words, $\overline{CAS}$ will be delayed from occurring by at least one rising clock edge after $\overline{RAS}$ goes low.
B0	**Address Latch Mode**
0	$\overline{ADS}$ (Port A) or $\overline{AREQB}$ (Port B) along with the appropriate GRANT latch the input row, column, and bank address.
1	The row, column and bank latches are permanently in fall-through mode
B1	**Access Modes (for Port A)**
0	Access Mode 0: In this mode $\overline{ADS}$ initiates the access $\overline{RAS}$ from the next rising clock (CLK) edge. $\overline{AREQ}$ is used to hold $\overline{RAS}$ low during the access. Convenient for Series 32000, iAPX 86/88/186/188, iAPX286... etc.
1	Access Mode 1: $\overline{ADS}$ initiates the access immediately and $\overline{AREQ}$ ends $\overline{RAS}$ when it goes high. Convenient for 68000/08/10/20

3.8 PLL STABILIZATION AND VRAM INITIALIZATION AFTER PROGRAMMING

After power up, the first time $\overline{ML}$ goes low to high with $\overline{DISRFSH}$ high the DP8520/21/22 enters a stabilization period in which the on-chip phase-locked-loop, used to generate precise on-chip delays, locks on to the 2 MHz reference clock (created by dividing down the DELCLK input). During this time, any attempted access to VRAM will result in the DP8520/21/22 asserting $\overline{WAIT}$ ($\overline{DTACK}$ high). Also, $\overline{RFIP}$ is forced low during the entire stabilization time and indicates that the DP8520/21/22 is ready for use when it returns high.

During the stabilization time, refreshes are performed approximately every 15 μsec, eliminating the need for further VRAM warm-up cycles. The initialization process takes about 60 ms (see formula below).

The 60 ms initialization process is performed only following the first programming of the DP8520/21/22 after power up or reset. If the DP8520/21/22 is programmed again, without powering down, the 60 ms initialization is not performed.

The PLL initialization period = 4096 X [Delay line Divisor (C0, C1, C2) $\times$ Refresh clock Divisor (C3) $\div$ DELCLK frequency]

3.0 Programming the DP8520/21/22 (Continued)

3.9 INITIALIZATION OF ECC VRAM SYSTEM

Initialization of an error checking and correcting (ECC) dynamic memory system involves writing known data and check bits to every memory location. The user may or may not elect to initialize the memory. If the user elects to initialize the memory, it can be very time consuming if the processor is required to write every location in the memory system. The DP8520/21/22 allows the user to efficiently initialize the entire VRAM system through a unique method of doing a burst refresh (with scrubbing) and writing (known data and check bits) to all four banks of the VRAM. This is accomplished as follows:

a) program the DP8520/21/22 in configuration mode 0 (C4, C5, C6 = 0, 0, 0), which allows error scrubbing during refresh; this allows the user to write data to all four banks of VRAM at once

b) wait for the 60 ms initialization period

c) latch the data and check bits in the ECC chip that will be used to initialize the VRAM

d) clear the refresh counter by pulling $\overline{RFSH}$ low with $\overline{DISRFSH}$ high

e) through an I/O port (or some other means) do a burst refresh (pull $\overline{DISRFSH}$, $\overline{RFSH}$, and $\overline{WIN}$ low) for the size of the VRAMs being driven. For example, if the DP8520/21/22 is driving one mega-bit VRAMs the outputs $\overline{RFIP}$, $\overline{RASn}$, and Q10 could be gated together to produce an end-of-count signal that ends the burst (pulls $\overline{DISRFSH}$, $\overline{RFSH}$, and $\overline{WIN}$ high). This burst does not require the processors attention. The processor can simply periodically sample the $\overline{RFIP}$ output to detect when the burst initialization of memory is completed

f) re-program the DP8520/21/22 with the correct configuration mode

4.0 Guaranteeing $\overline{RAS}$ Low and $\overline{RAS}$ Precharge Time

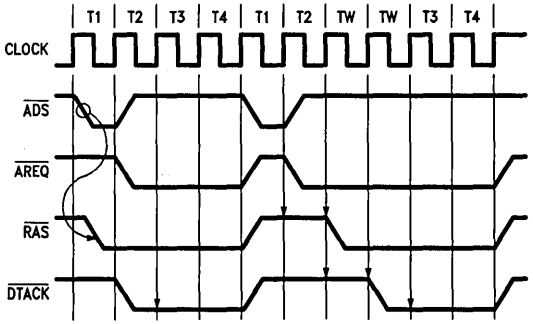
The user chooses between four combinations of $\overline{RAS}$ low, $\overline{RAS}$ precharge times through the programming bits R0, R1. The $\overline{RAS}$ low and $\overline{RAS}$ precharge time are based upon the input system clock (CLK). During refresh, $\overline{RAS}$ is initiated from the rising edge of CLK, and the $\overline{RAS}$ low time is met by counting rising clock edges.

The $\overline{RAS}$ precharge time is also guaranteed by counting rising clock (CLK input) edges.

As an example, suppose that the user had programmed two periods of $\overline{RAS}$ low time during refresh and two periods of $\overline{RAS}$ precharge time. During refresh, $\overline{RAS}$ would transition low from a rising clock edge and transition high two rising clock edges later. $\overline{RAS}$ precharge would than count two rising clock edges after an access or a refresh ends before allowing another access or refresh to take place (see *Figure 14*). Please note that the $\overline{RAS}$ precharge time could be quite a bit less than two clock periods. For example, if $\overline{RAS}$ went high one half clock after a rising clock edge the DP8520/21/22 would allow the next access to that bank ($\overline{RAS}$) to begin after two rising clock edges; only one and one half clock periods after $\overline{RAS}$ ended for the previous access.

Each bank has its own separate $\overline{RAS}$ precharge counter, thereby guaranteeing that the $\overline{RAS}$ precharge time will be met between any two accesses to the same bank, even during interleaved accesses.

Note that $\overline{RAS}$ low time is guaranteed as programmed only during refresh.



TL/F/9338–14

*$\overline{DTACK}$ set to one clock period after $\overline{RAS}$ goes low.

FIGURE 14. Guaranteeing $\overline{RAS}$ Precharge ($\overline{RAS}$ Precharge Set as Two Clock Periods) (Access Mode 1)

5.0 Wait State Support

There are six bits of programming (R2–R7), an input pin ($\overline{\text{WAITIN}}$) and an output pin ($\overline{\text{WAIT}}$) associated with the wait state logic for Port A. The Port B wait state logic has no programming bits or input pins associated with it, but uses one output pin ($\overline{\text{ATACKB}}$).

Wait states provide a means whereby a system peripheral can arbitrarily increase the length of a CPU access cycle by any number of CPU clock periods. The CPU determines whether to insert wait states (extra clock periods) into an access cycle based upon a wait input line. The wait input to the CPU is periodically sampled during an access to determine whether the access should be completed or if it should be prolonged by an extra clock period (see *Figures 14*, *15*, and *16*).

The decision as to whether or not to terminate the CPU access cycle is intimately tied to the CPU data. During a write access, has the data been written to the peripheral? If yes, then no more wait states should be inserted into the access cycle and the CPU can remove its data from the data bus. If no, then keep inserting wait states into the CPU access cycle until the data has been written. During a read access, wait states should be inserted into the CPU access cycle until the data is available for the CPU to read from its data bus.

The wait input line can be called by many different names depending upon the manufacturer and the particular CPU, i.e., $\overline{\text{WAIT}}$, $\overline{\text{DTACK}}$, $\overline{\text{READY}}$, $\overline{\text{DSACK}}$, $\overline{\text{XACK}}$, etc. Any of these signals can be grouped into being compatible with one of the two outputs of the DP8520/21/22, either $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$ (see *Figures 14*, *15*, *16*, *17* and *18*).

The wait state logic will automatically insert wait states into an access cycle due to:

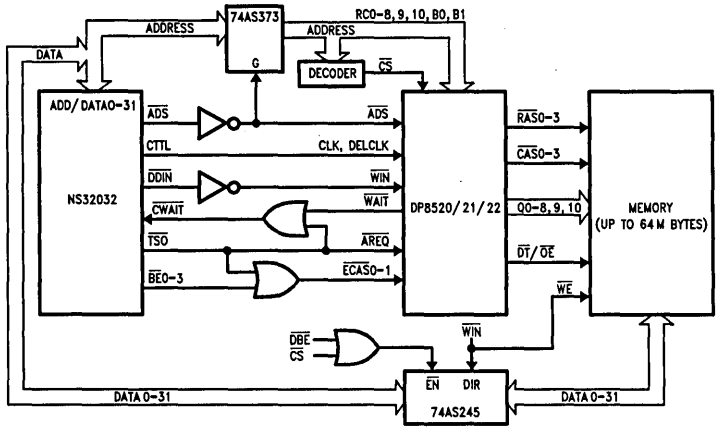
a) $\overline{\text{RASn}}$ precharge not completed,

b) Grant not being valid for that particular port, (DP8522 only)

c) Refresh currently in progress,

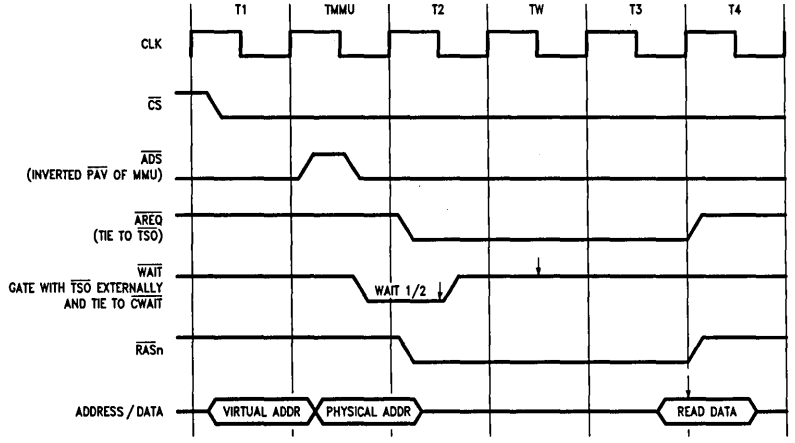
d) The user programmed wait states to occur during the access,

e) The $\overline{\text{WAITIN}}$ input is low causing extra wait states to be inserted into the access cycle.



TL/F/9338–15

FIGURE 15. NS32032/DP8520/21/22 Block Diagram

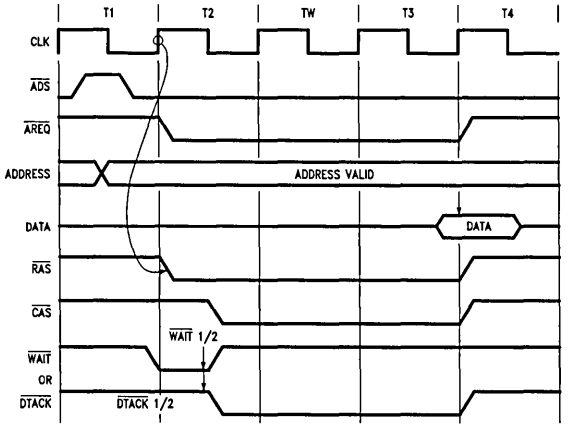


TL/F/9338–16

FIGURE 16. Series 32000® WAIT Example with Memory Management Unit (MMU) (Access Mode 0)

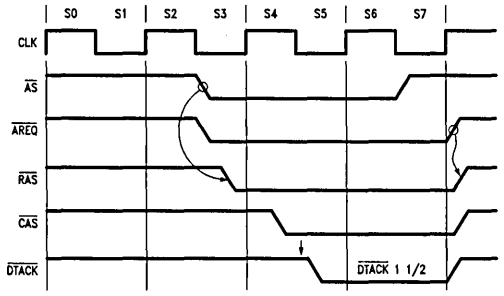
5.0 Wait State Support (Continued)

(EX: Access Mode 0 (Series 32000 Like), Read Access with one Wait State)



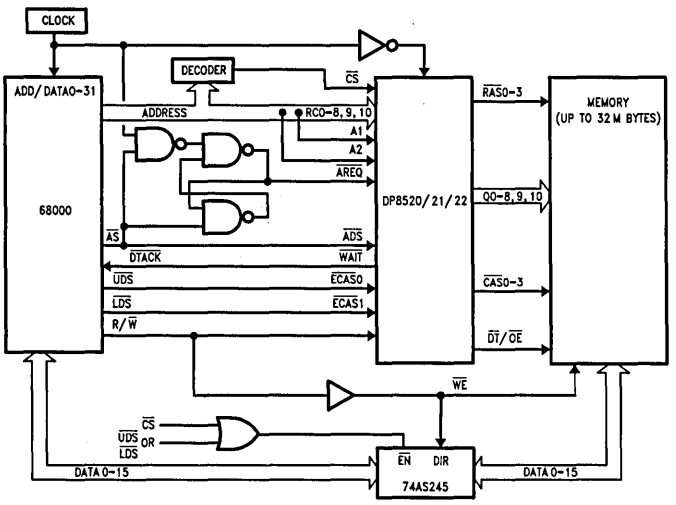
TL/F/9338–17

(EX: Access Mode 1 (68000 Like))



TL/F/9338–18

FIGURE 17. Access Modes and WAIT/DTACK (Data Transfer Acknowledge)



TL/F/9338–19

FIGURE 18. 68000/DP8520/21/22 Block Diagram

(68000 in Interleaved Mode to Guarantee Adequate RAS Precharge Time and Start the Access As Early as Possible)

5.0 Wait State Support (Continued)

5.1 WAIT/DTACK PROGRAMMING BIT FOR PORT A

One bit, programmed through the R7 address input, allows the user to choose between a Wait (WAIT) or Data Transfer Acknowledge (DTACK) type of output from the DP8520/21/22 (see *Figure 17*). In general, any CPU's wait state logic can directly input either WAIT or DTACK from the DP8520/21/22. As can be seen, as long as the WAIT output is sampled low by the CPU, wait states (extra clock periods) are inserted into the current access cycle. Once WAIT is sampled high, the access cycle is completed by the CPU. If DTACK is chosen when programming, as long as DTACK is sampled high by the CPU, wait states are inserted into the current access cycle. Once DTACK is sampled low, the access cycle is completed by the CPU.

5.2 PROGRAMMING THE NUMBER OF WAIT STATES FOR PORT A

Two bits, programmed through the R2, R3 address inputs, allow the user to select when WAIT goes high (DTACK goes low) in relation to RASn and the system clock (CLK) during an access (see *Figures 14, 15, 16, 17* and *18*).

If the WAIT output is selected and zero wait states are programmed into the DP8520/21/22, then the WAIT output will not go low during an access unless that access is delayed from occurring (i.e., a refresh being in progress, Port B currently accessing the VRAM . . . etc.). In this case, the WAIT output of the DP8520/21/22 will be low until either RASn goes low, or one half period after RASn goes low for that access (depending upon what was programmed into bits "R2, R3" of the DP8520/21/22, see "INTERNAL PROGRAMMING MODE BITS" section 3.6 of the data sheet).

All the logic on the DP8520/21/22 references the rising edge of the system clock (CLK) input. Therefore, if the user programmed that WAIT should transition high one half period after RASn goes low, the WAIT output will transition high as soon as the condition of RASn low and CLK low occurs (see *Figures 16* and *17*).

The WAIT output will transition low, given that wait states are to be inserted in the access cycle, whenever a chip selected access starts as determined by the ADS and CS inputs. The DTACK output will transition high at the end of the current access as determined by the AREQ input (see *Figure 17*).

5.3 PROGRAMMING THE NUMBER OF WAIT STATES DURING BURST MODE FOR PORT A

Two bits, programmed through the R4 and R5 address inputs, allow the user to select when WAIT goes high (DTACK goes low) in relation to CASn and the system clock (CLK) during a nibble or page mode access to a VRAM (see *Figures 19* and *20*).

Once an access is in progress (RASn is low) the selected CASn outputs are controlled by the ECASn inputs.

If the WAIT output is selected and zero wait states during burst mode accesses is programmed into the DP8520/21/22 (R4 = R5 = R7 = logic "0") then the WAIT output will not go low throughout the entire burst mode access. If the DTACK output is selected and zero wait states during burst mode accesses is programmed into the DP8520/21/22 (R4 = R5 = logic "0", R7 = logic "1") then the DTACK output will stay low during the entire burst mode access.

If "0T" is programmed into the DP8520/21/22 (R4 = R5 = logic "1") then the WAIT (DTACK) output would go low (high) from ECAS transitioning high and would transition high (low) from ECAS transitioning low thus being slightly different from the above mentioned case where (R4 = R5 = logic "0"). Depending upon where the processor samples WAIT or DTACK during the burst access, this mode may prove very useful in allowing the user to program any number of wait states he may desire.

Any burst mode type of access is preceeded by a non-burst type of access. During a nibble or page mode type of access the burst portion of the access is not started until after an ordinary (non-burst) access at which point the CAS input to the VRAM can be toggled (while holding RAS low) entering into the burst access (see *Figures 19, 20* and *21*).

5.4 PROGRAMMING EXTRA WAIT STATES THROUGH THE USE OF THE WAITIN INPUT FOR PORT A

One bit, programmed through the R6 address input, allows the user to select whether one or two clock periods are added to what was programmed through address bits R2, R3 (during a non-burst mode access), or through address bits R4, R5 (during a burst mode access) if WAITIN is low during an access (see *Figures 21, 22, 23, 24, 25 and 26).*

For example, suppose the user has programmed the DP8520/21/22 to function with DTACK going low one half system clock periods (referencing CLK) after RASn goes low during an access and one half period after CASn transitions low during a burst access. Suppose that the user has also programmed the DP8520/21/22 to add one clock period to the above programmed values if the WAITIN input is low during the access (burst or non-burst). Therefore, if WAITIN is low during a non-burst access, DTACK will go low one and one half clock periods after RASn transitions low. If WAITIN is low during a burst access, DTACK will go low one and one half clock periods after CASn transitions low (see *Figure 21*).

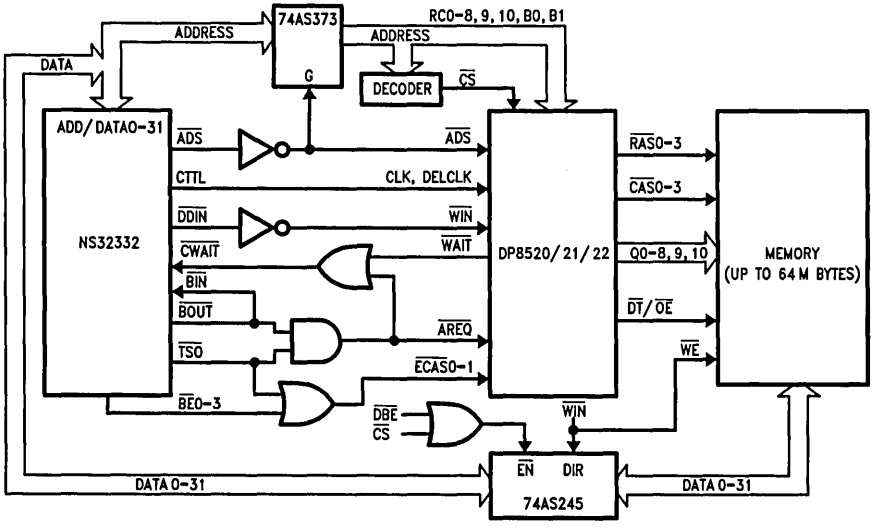
When using the WAITIN input the user should be aware that this input must be valid some setup time, tSWCK, before the clock edge that ends WAIT (starts DTACK). If zero wait states were programmed, the user must have the WAITIN input low some setup time, tSWCK (access mode 0) or tSWADS (access mode 1), before initiating the access. The WAITIN input can go high at the rising clock edge preceding the period during which WAIT ends (DTACK starts).

The WAITIN input may be useful in systems where, for example, the user wants zero wait states during write cycles and one wait state during read cycles.

An alternate example would be if the user is designing an error checking and correcting memory system. In this case he may desire one wait state during read or write operations and three wait states during byte write operations. Using the WAITIN input the user can cause the WAIT output to stay low two clock periods beyond what was programmed via the R2, 3 address inputs and therefore, add two wait states to that particular access.

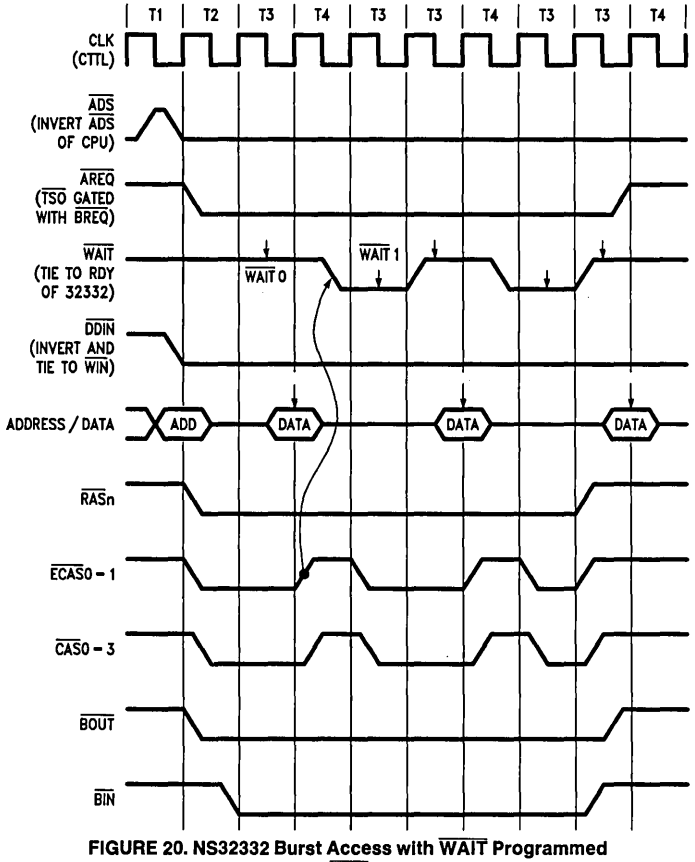
As a further example, the processor may be sharing the access port with a DMA controller. All processor accesses can proceed with zero wait states whereas all DMA accesses may require one wait state. The WAITIN input allows the user to configure his system in this way.

5.0 Wait State Support (Continued)



TL/F/9338-20

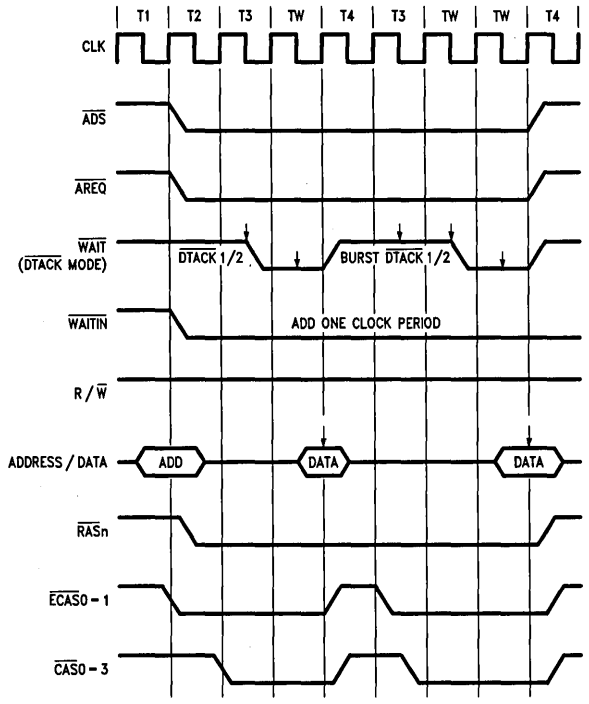
FIGURE 19. NS32332/DP8520/21/22 Block Diagram



TL/F/9338-21

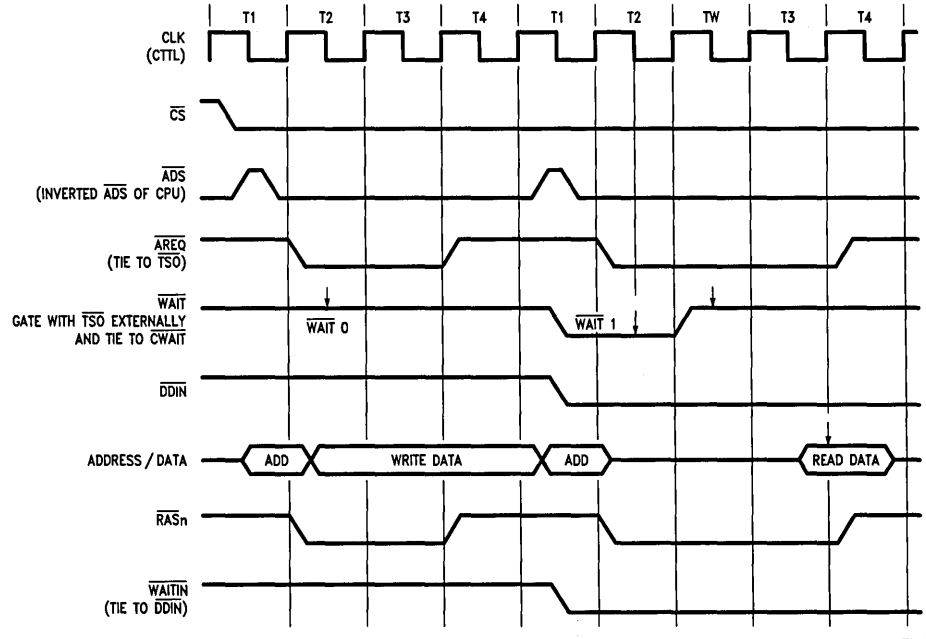
FIGURE 20. NS32332 Burst Access with WAIT Programmed to Go High One Period after CAS Goes Low (Access Mode 0)

5.0 Wait State Support (Continued)



TL/F/9338-22

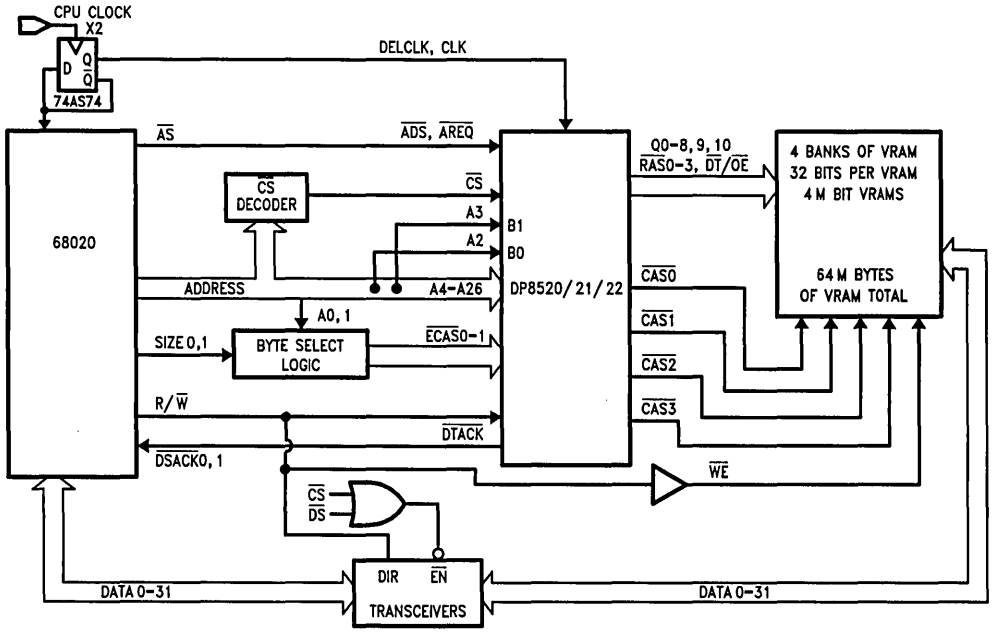
FIGURE 21. Example of the Effect of WAITIN (Access Mode 1) on Example CPU



TL/F/9338-23

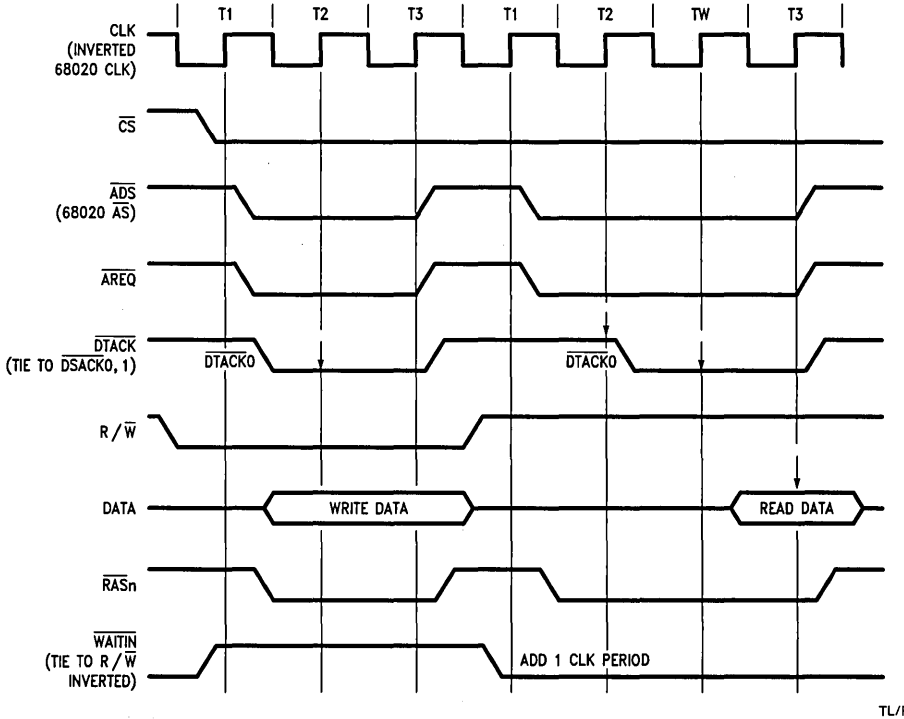
FIGURE 22. Series 32000 Example, Zero Wait States During Write Accesses and One Wait State During Read Accesses (Access Mode 0)

5.0 Wait State Support (Continued)



TL/F/9338-24

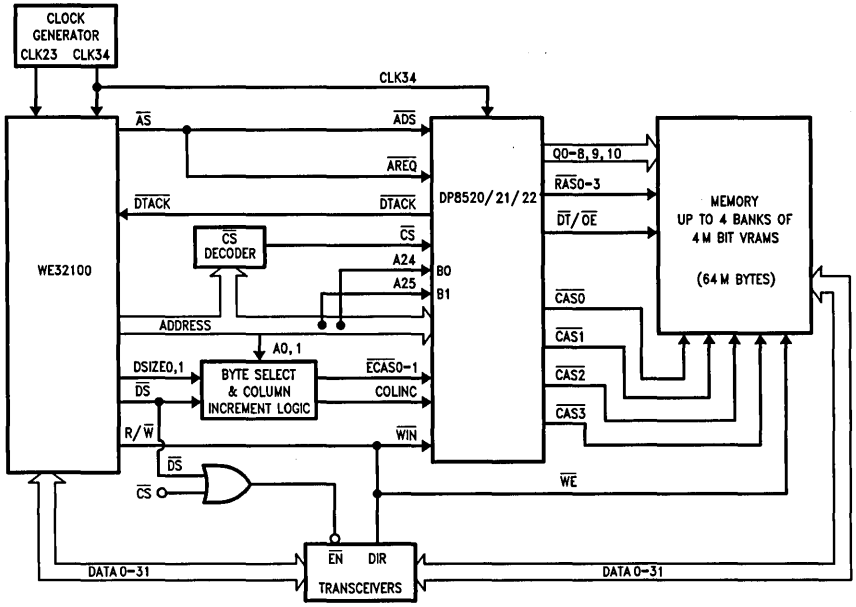
FIGURE 23. 68020 System Block Diagram (Access Mode 1)



TL/F/9338-25

FIGURE 24. 68020 DTACK Example, Zero Wait States During Write Accesses and One Wait State During Read Accesses

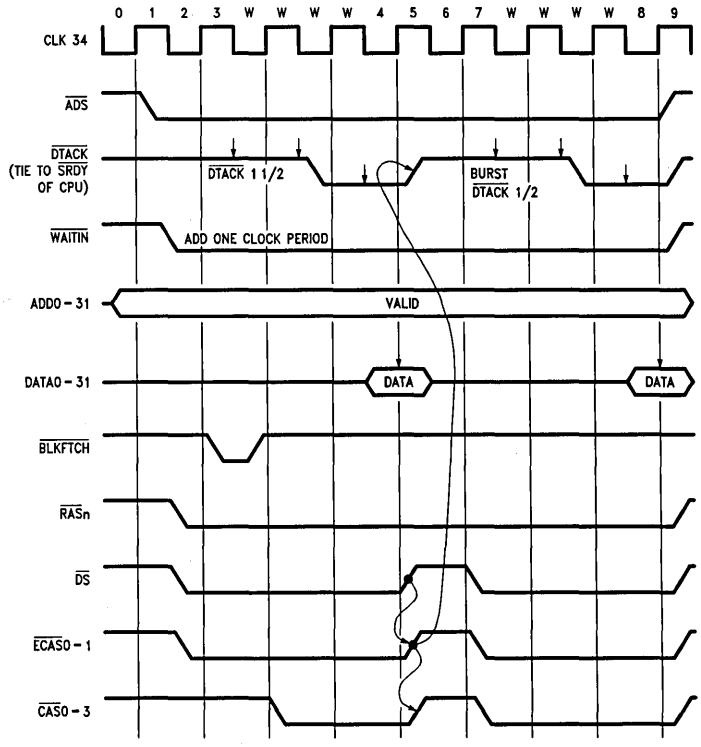
5.0 Wait State Support (Continued)



TL/F/9338-26

FIGURE 25. 32100 System Block Diagram (Access Mode 0)

Allows support of burst (up to 4 words) (Address 2, 3 go to C0, 1 inputs)



TL/F/9338-27

FIGURE 26. 32100 Burst Access with WAITIN Low (Access Mode 1)

5.0 Wait State Support (Continued)

5.5 PORT B WAIT STATE LOGIC (DP8522 ONLY)

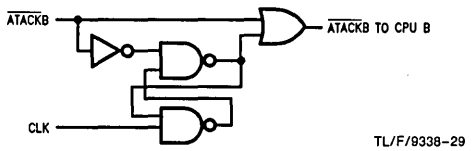
The advanced transfer acknowledge ($\overline{ATACKB}$) output for Port B functions essentially the same as the $\overline{DTACK}$ output for Port A programmed for zero wait states. In other words, as soon as $\overline{RASn}$ goes low for the Port B access the output $\overline{ATACKB}$ will go low and it will stay low until $\overline{AREQB}$ ends (see *Figure 27*).

It should be noted that the $\overline{ATACKB}$ output stays low (until the access ends) once it has gone low during an access. Therefore, if the user is doing a burst type access using Port B, only the condition of zero wait states is directly supported.

If the user desires to have a wait state in every Port B access, this can be performed in external logic fairly easily (see *Figure 28*) using the $\overline{ATACKB}$ output as a reference point.

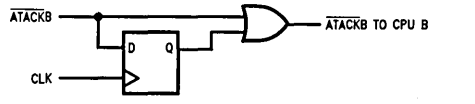
5.6 WAIT STATE LOGIC DURING VIDEO RAM SHIFT REGISTER LOAD FOR PORT A

If using the DP8520/21/22 in a system using video DRAMs, the CPU that controls loading the video RAM shift register must be connected to Port A. Given that this is the case, the $\overline{WAIT}$ output will remain low ($\overline{DTACK}$ will remain high) during a video RAM shift register load access until the output $\overline{DT}$ is brought high (loading the shift register of the video



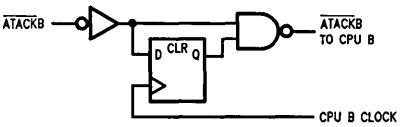
TL/F/9338-29

A) Extend $\overline{ATACK}$ to ½T (½ Clock) after $\overline{RAS}$ Goes Low



TL/F/9338-30

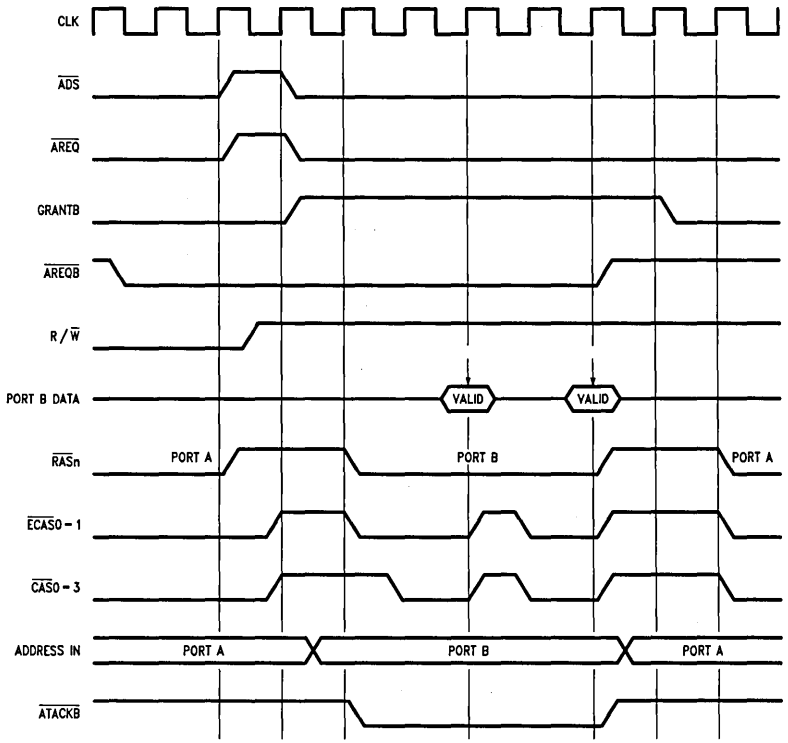
B) Extend $\overline{ATACK}$ to 1T after $\overline{RAS}$ Goes Low



TL/F/9338-31

C) Synchronize $\overline{ATACKB}$ to CPU B Clock. This is useful if CPU B runs asynchronous to the DP8522.

FIGURE 28. Modifying Wait Logic for Port B



TL/F/9338-28

FIGURE 27. Wait States During a Port B Access

5.0 Wait State Support (Continued)

RAM). At this point, $\overline{WAIT}$ will go high ($\overline{DTACK}$ will go low) immediately or one half system clock period later, depending upon how the user had programmed $\overline{WAIT}$ to end ($\overline{DTACK}$ to start) during a non-burst type of access. In other words, whether $\overline{WAIT}$ ended ($\overline{DTACK}$ started) upon a rising or falling system clock edge. The output $\overline{DT}$ will remain low during this access until either the input $\overline{VSRL}$ goes high or four clocks after $\overline{DT}$ went low, whichever occurs first (see *Figures 45* and *50*).

6.0 Support for Memory Interleaving (Address Pipelining)

"Memory Interleaving" refers to the concept of overlapping accesses to different memory banks. By guaranteeing each successive access is to a different memory bank the user can guarantee that the $\overline{RAS}$ precharge time of each bank is hidden in the access to the next sequential bank. Because of this, the effective cycle time of each VRAM access is greatly reduced.

Memory interleaving takes advantage of the fact that in general the majority of memory references generated by a processor are sequential in nature. This feature can be used to an advantage with a VRAM controller by tying the two least significant address bits of the processor to the bank select inputs (B0, B1) of the VRAM controller (i.e., DP8520/21/22). By doing this the system designer guarantees that sequential accesses will access different memory banks (bank 0- bank 1- bank 2- bank 3- bank 0 . . . etc.).

In the broader sense of "memory interleaving", performance can be increased beyond the ability to disregard $\overline{RAS}$ precharge time in sequential memory accesses. For example, several memory accesses could potentially be occurring at the same time.

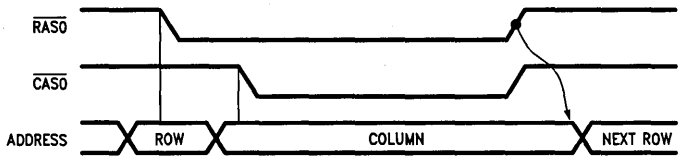
The DP8520/21/22 allows this ability through the use of a programming bit (R8). This programming bit allows the user to choose how long the column address is held valid after $\overline{CAS}$ goes low before switching back to the row address.

In most VRAM controllers, once the row address has been switched to the column address the column address is held until the access is finished (i.e., $\overline{RAS}$ goes high). The DP8520/21/22 allows the user to choose between this and holding the column address 50 ns then switching back to the row address. Given that the latter is chosen, another access can be started once the new row address is multiplexed to the VRAM controller's address outputs (Q0–Q10). This feature allows two memory accesses to overlap by starting a second memory access before the first access is finished (see *Figures 29, 30* and *31*).

The DP8522 supports memory interleaving in Port A but not in Port B. The two access request inputs for Port A, $\overline{AREQ}$ and $\overline{ADS}$, provide support for memory interleaving. $\overline{ADS}$ starts an access and $\overline{AREQ}$ is used to sustain and end the access. While $\overline{AREQ}$ is low another access can be started via $\overline{ADS}$.

As a note of caution, it should be apparent that it is not possible to choose the interleaving mode and allow burst mode types of accesses (ie. VRAM nibble, page, or static column mode). This is because when allowing burst type accesses the least significant bits (LSBs) of the address bus must be tied to the least significant bits of the DP8520/21/22 column address inputs. Whereas in memory interleaving the least significant bits of the address bus must be tied to the DP8520/21/22 bank address inputs.

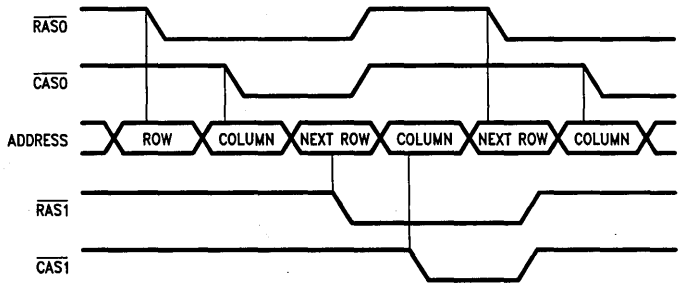
An 80386 system is shown in *Figures 32, 33* and *34.*



TL/F/9338–32

FIGURE 29. Non Interleaved Mode

*Column Address Held Until $\overline{RAS}$ Goes High

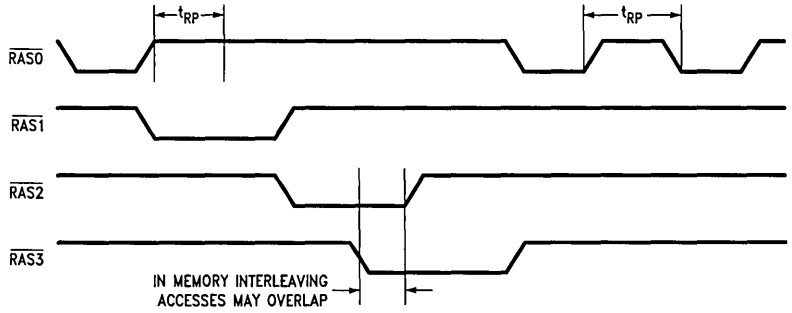


TL/F/9338–33

FIGURE 30. Memory Interleaved Mode

*Column address is held for a minimum of 50 ns before changing back to row address

6.0 Support for Memory Interleaving (Address Pipelining) (Continued)

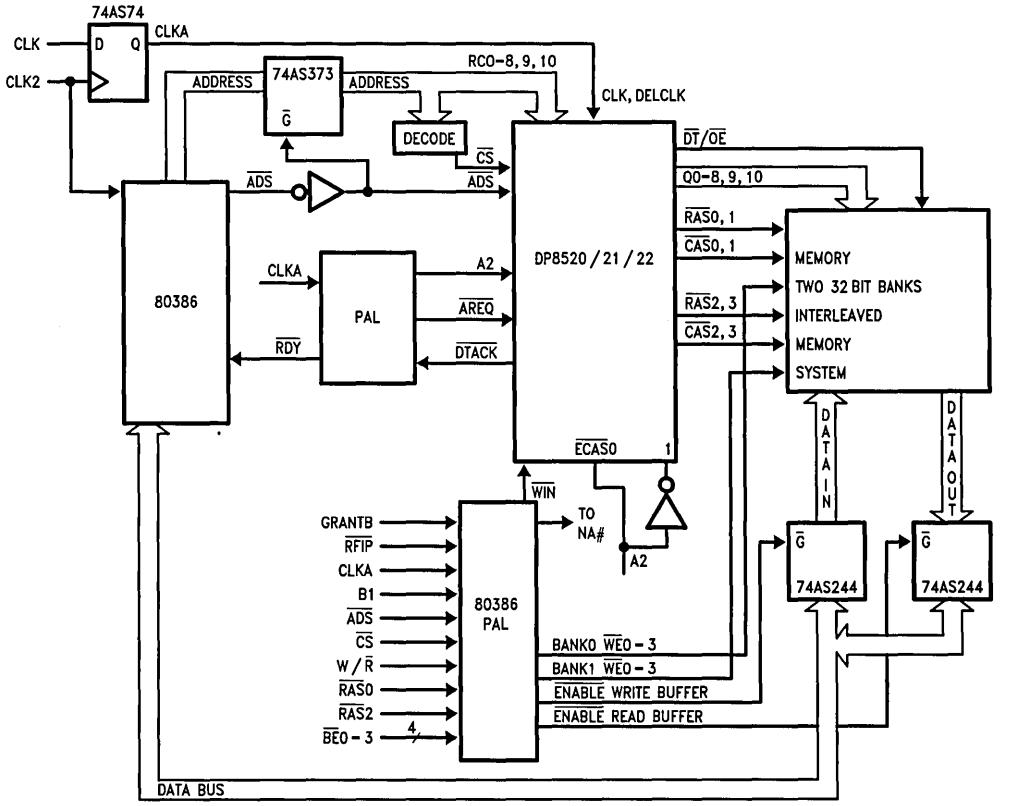


TL/F/9338–34

FIGURE 31. Memory Interleaving

A) Least significant address bits control the RAS bank accessed.

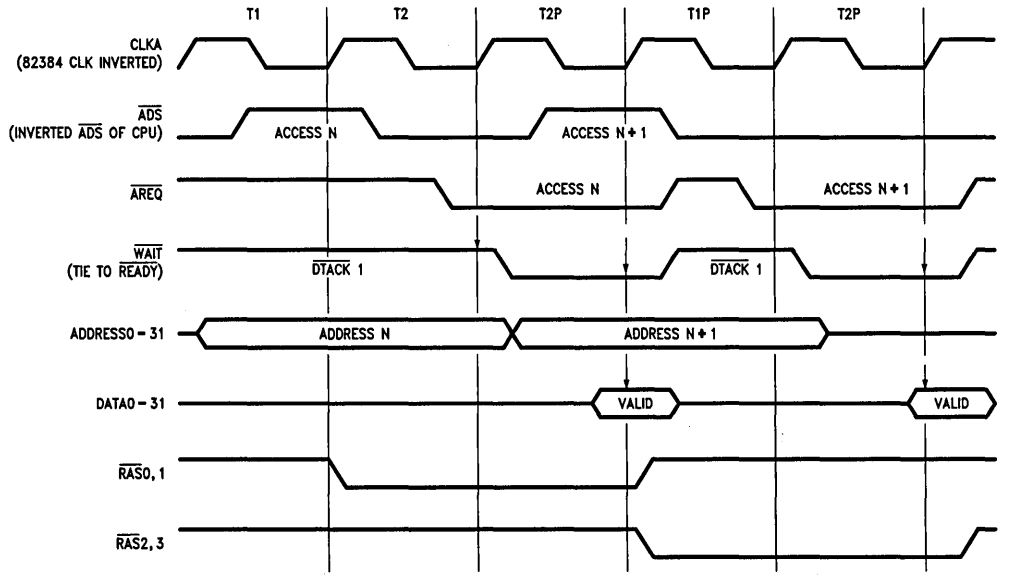
B) As long as VRAM accesses are sequential the VRAM RAS precharge time (tRP), which is normally part of the VRAM cycle time, may be hidden by consecutive accesses as shown below. Two consecutive accesses to the same memory bank must be delayed.



TL/F/9338–35

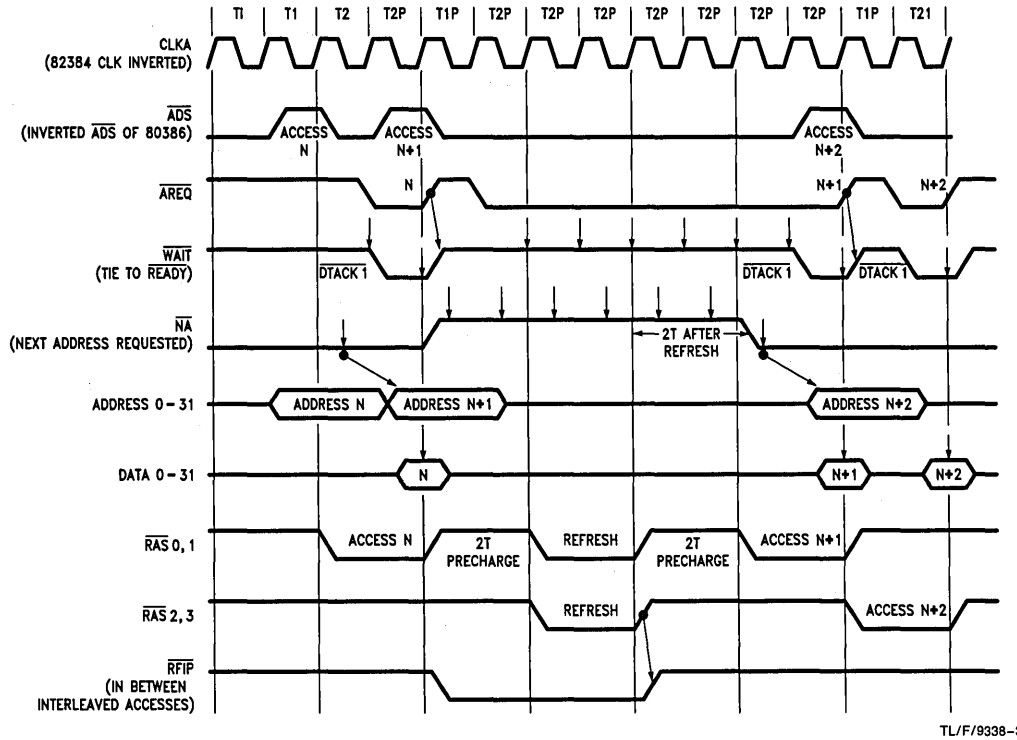
FIGURE 32. 80386/DP8520/21/22 Block Diagram

6.0 Support for Memory Interleaving (Address Pipelining) (Continued)



TL/F/9338-36

FIGURE 33. Interleaved Accesses on the 80386 (Access Mode 0) One Wait State in Non-Pipelined Access, Zero Wait States in Pipelined Access



TL/F/9338-37

FIGURE 34. Refresh/Access Arbitration and Address Pipelining on the 80386

7.0 VRAM Refresh Options

The DP8520/21/22 supports a wide variety of refresh options including automatic internally controlled refresh (all $\overline{RAS}$ refresh, staggered refresh, and ECC scrubbing during refresh), externally controlled single or burst refresh (all $\overline{RAS}$ refresh, staggered refresh, or ECC scrubbing during refresh), and various combinations of automatic internally controlled and externally controlled refresh (see *Figures 35, 36, 37* and *38*).

There are three pins on the DP8520/21/22 associated with refreshing the VRAMs; $\overline{DISRFSH}$, $\overline{RFSH}$, and $\overline{RFIP}$ (See section 1, pin definitions) and seven programming bits; R0–1, R9, C3, C4–6 (see section 3.6).

The two pins $\overline{DISRFSH}$ and $\overline{RFSH}$ are used in the externally controlled refresh mode (see section 7.2). The output $\overline{RFIP}$ applies to all refreshing modes. The output $\overline{RFIP}$ go low one period before the refresh $\overline{RAS}$s go low. If an access is currently in progress, $\overline{RFIP}$ will go low once the access is over ($\overline{AREQ}$ or $\overline{AREQB}$ and $\overline{CAS}$ high) up to one clock period (CLK) before $\overline{RAS}$ transitions low for the VRAM refresh.

Whether the DP8520/21/22 is executing an internally or externally requested refresh, the DP8520/21/22 refresh counter will automatically be incremented by $\overline{RAS}$ going high during the refresh.

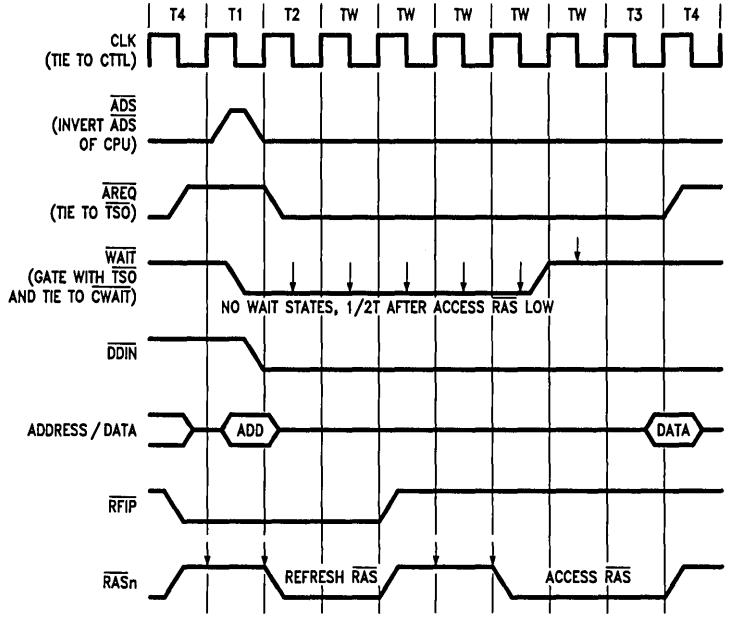
Also, any refresh may be extended through the use of the EXTENDRF input.

7.1 AUTOMATIC INTERNAL REFRESH OPTIONS

The automatic refresh is generated via an internal refresh request. The refresh request is generated from the internal refresh clock. The period of the refresh clock is user programmed into the DP8520/21/22 through the C0–3 address bits. As long as the automatic internal refresh is enabled ($\overline{DISRFSH}$ input is high), a VRAM refresh will be performed once each period of the refresh clock.

The automatic internal refresh will happen whenever a refresh request is generated (once each period of refresh clock) as long as a VRAM access is not currently in progress. If a VRAM access is in progress, the DP8520/21/22 arbitration circuitry will wait until the access is finished before initiating the refresh.

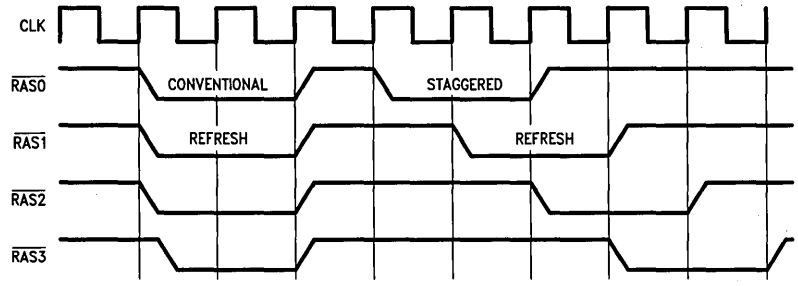
The refresh arbitration circuitry is intelligent enough to be able to insert a refresh cycle (internally or externally generated) between two interleaved accesses. This is accomplished by allowing the current access to finish while holding off the next access until the refresh cycle has been completed. The wait logic will automatically insert wait states into the next access cycle until the refresh, $\overline{RAS}$ precharge time, and preprogrammed wait states (with respect to the access $\overline{RAS}$) have been completed (see section 5 and *Figure 35*).



TL/F/9338–38

FIGURE 35. Refresh Access Arbitration with Series 32000 (Access Mode 0)

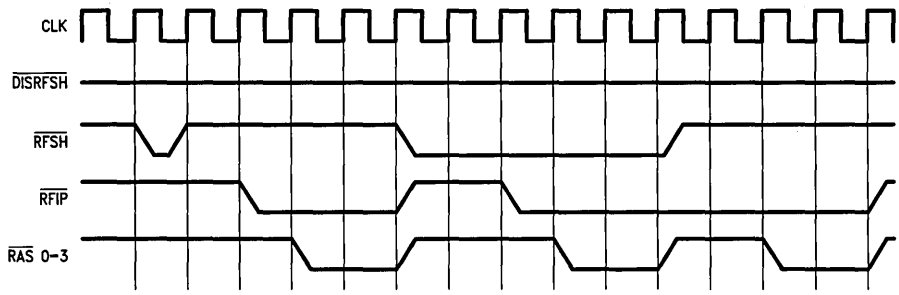
7.0 VRAM Refresh Options (Continued)



TL/F/9338–39

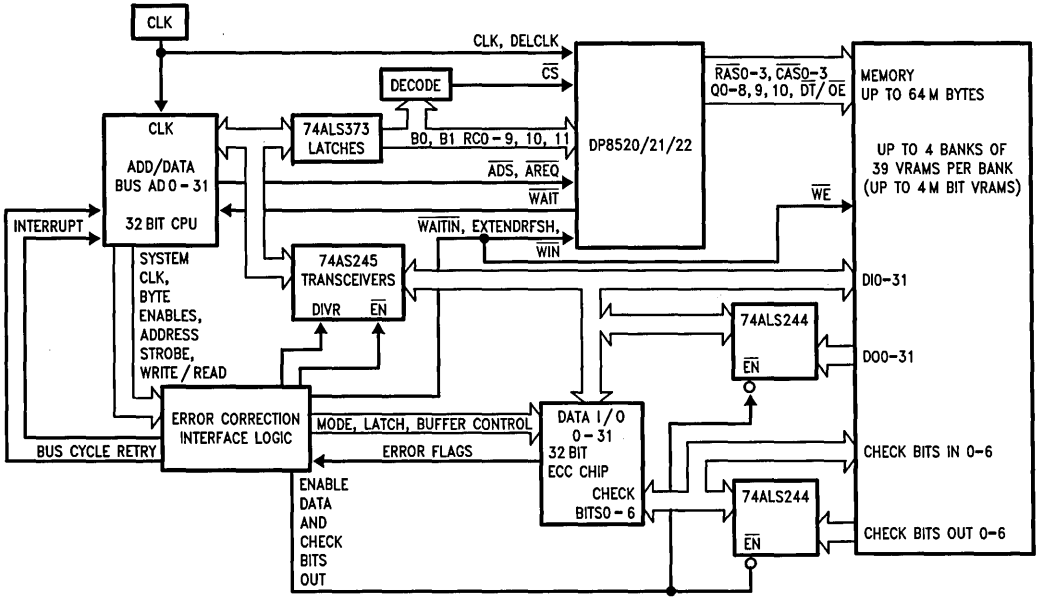
FIGURE 36. Regular and Staggered Refresh

(Ex: 2 Clock Periods $\overline{RAS}$ Low During Refresh, 1 Period $\overline{RAS}$ High for Precharge)



TL/F/9338–40

FIGURE 37. Externally Requested Single and Burst (of Two Refreshes) Refresh. DP8520/21/22 Programmed for Two Periods of $\overline{RAS}$ Low During Refresh and Two Periods of $\overline{RAS}$ Precharge Between Accesses to the Same $\overline{RAS}$ Bank.



TL/F/9338–41

FIGURE 38. DP8520/21/22 ECC Block Diagram

7.0 VRAM Refresh Options (Continued)

When using the DP8522 in a dual access VRAM system, the refresh arbitration circuitry has the ability to insert a refresh (externally or internally generated) between two accesses even when the $\overline{LOCK}$ input is low (generally used during a read modify write semaphore type of operation).

However, the refresh arbitration logic cannot interrupt a burst mode type of access (VRAM nibble, page, or static column mode access) in order to do a refresh. Therefore, it is the system designers responsibility to guarantee that the VRAM is refreshed often enough when allowing burst mode types of accesses. This could be guaranteed in one of the following ways;

a) only allow burst mode accesses that are less than a refresh clock period in length

b) by doing externally controlled single or burst type refreshes to guarantee adequate refreshing of the VRAM

7.1.1 INTERNALLY CONTROLLED ALL $\overline{RAS}$ REFRESH

In an internally controlled all $\overline{RAS}$ refresh, $\overline{RAS0-3}$ all go low and high during the refresh simultaneously and stay low the programmed amount of time (set by address bits R0, 1).

The $\overline{RAS}$ precharge time is guaranteed between the previous access ending to refresh starting and the refresh ending to the next access starting (see section 4 and *Figures 35* and *36*).

7.1.2 INTERNALLY CONTROLLED STAGGERED REFRESH

In an internally controlled staggered refresh, $\overline{RAS0-3}$ are each staggered by one system clock period (CLK) as they go low and high. In other words, during the refresh $\overline{RAS0}$ will go low, followed one period later by $\overline{RAS1}$, one period later by $\overline{RAS2}$, and finally one period later by $\overline{RAS3}$ (differs if $\overline{RAS}/\overline{CAS}$ configuration mode in which more than one $\overline{RAS}$ goes low during an access is selected). The $\overline{RAS}$s will end in a similar manner; $\overline{RAS0}$, followed one period later by $\overline{RAS1}$, one period later by $\overline{RAS2}$, and one period later by $\overline{RAS3}$ (see *Figure 36*).

The $\overline{RAS}$ precharge time is guaranteed between the previous access $\overline{RAS}$ ending to the refresh $\overline{RAS0}$ starting and the refresh $\overline{RAS3}$ ending to the next access $\overline{RAS}$ starting.

It should be noted that staggered refresh is not allowed when scrubbing is programmed, this combination is used as a test mode of the chip.

7.2 EXTERNALLY CONTROLLED REFRESH OPTIONS

The externally controlled refresh is generated externally through the use of two pins, $\overline{DISRFSH}$ and $\overline{RFSH}$.

If the user desires to control refreshes externally he should disable internal refreshes by tying $\overline{DISRFSH}$ low.

It is important to note that externally controlled refreshes can be all $\overline{RAS}$ refreshes or staggered refreshes depending upon how the DP8520/21/22 was programmed (program bit R9).

Similar to what was mentioned in section 7.1 regarding automatic internal refreshes, an externally controlled refresh request can insert a refresh (single or burst) between two interleaved accesses or between two locked ($\overline{LOCK}$ low) accesses when using the dual accessing capability. But even an externally controlled refresh request cannot stop a burst mode access. Therefore, during a burst mode access the system designer is responsible for guaranteeing that the VRAM is refreshed often enough.

7.2.1 EXTERNALLY CONTROLLED SINGLE REFRESHES

In order to do an externally controlled single refresh, the user should tie $\overline{DISRFSH}$ low and pulse $\overline{RFSH}$ low for a minimum of tPXX. If the user wants only one refresh cycle he must pull $\overline{RFSH}$ high a setup time, tSXX, before the clock edge that ends the refresh $\overline{RAS}$s. If the user holds $\overline{RFSH}$ low until after that clock edge another refresh cycle will be executed (see *Figure 37*).

7.2.2 EXTERNALLY CONTROLLED BURST REFRESHES

A burst refresh consists of multiple back to back refreshes that meet the refresh $\overline{RAS}$ low time and the $\overline{RAS}$ precharge time (programming bits R0–1). In order to do a burst refresh, $\overline{RFSH}$ must remain low until the required number of refreshes have been executed. ($\overline{DISRFSH}$ should be tied low).

If the user desires to burst refresh the entire VRAM (all row addresses) he could generate an end of count signal (burst refresh finished) by looking at one of the DP8520/21/22 high address outputs (Q7, Q8, Q9 or Q10), the $\overline{RFIP}$ output, and one of the $\overline{RAS}$n outputs. The Qn outputs function as a decode of how many row addresses have been refreshed (Q7 = 128 refreshes, Q8 = 256 refreshes, Q9 = 512 refreshes, Q10 = 1024 refreshes).

It should be mentioned that the user does not have to refresh the entire VRAM every time he does a burst refresh. The DP8520/21/22 allows the user to do burst refreshes of any length. As an example, the user could always do bursts of 16 refreshes using the above mentioned method by gating Q4 into the end of count logic.

7.3 COMBINATION OF INTERNAL AND EXTERNAL REFRESHING

It is also very simple to use a combination of internally and externally controlled refreshing with the DP8520/21/22. This feature may be very useful in a system where the VRAM can be refreshed by the automatic internal refreshes most of the time but sometimes requires bursts because a process runs that cannot be interrupted during the time it is accessing the VRAM. This process may be accessing the VRAM for several milliseconds at a time. Since it is not possible to do VRAM refreshes during this time, the system designer may decide to do a burst refresh before and after this particular access mode.

When the user wants to do a burst refresh in the above mentioned situation he may first want to clear the refresh counter (see section 7.5). He can then hold both $\overline{DISRFSH}$ and $\overline{RFSH}$ low for a predetermined amount of time (see section 7.2) until the burst refresh is finished.

During an externally controlled refresh ($\overline{DISRFSH}$ and $\overline{RFSH}$ both low) the system designer must guarantee that $\overline{DISRFSH}$ remains low for a minimum of 500 ns in order to clear the DP8520/21/22 internal refresh clock counter. By clearing the internal refresh clock counter the user is guaranteeing that an internally requested refresh will not be generated for one refresh clock period, approximately 15 μs (see section 7.1), from the time $\overline{DISRFSH}$ goes high.

7.4 TRANSPARENT SINGLE BIT ERROR SCRUBBING DURING MEMORY REFRESH

The DP8520/21/22 supports error scrubbing during VRAM refreshes (up to 4M-bit VRAMs) by containing a 24 bit internal refresh counter (11 row, 11 column, and 2 bank addresses). This is a useful function in a VRAM system employing Error Checking and Correcting (ECC) circuitry as is

7.0 VRAM Refresh Options (Continued)

explained below. The system designer chooses whether he wants error scrubbing during VRAM refreshes by how he programs the DP8520/21/22 (program bits C4–6, see section 3.6).

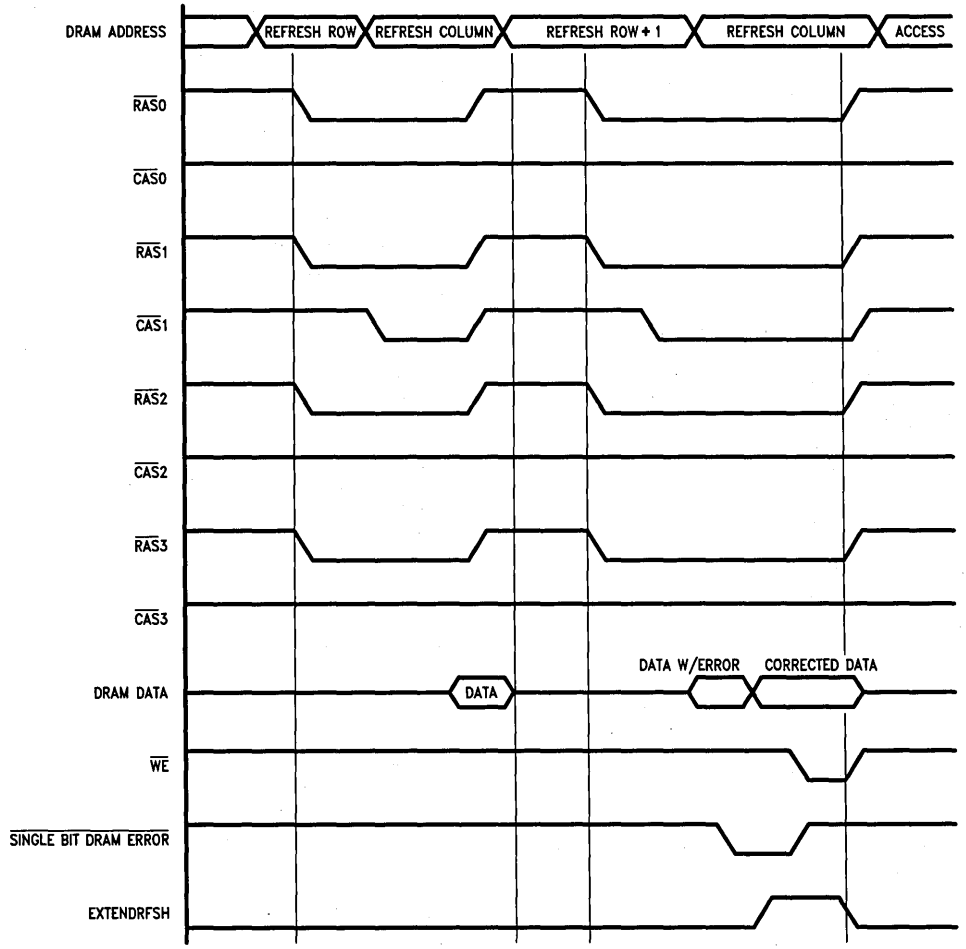
In a VRAM system employing ECC, the memory is always accessed as whole words because ECC circuitry must always read or write whole words. Therefore, byte writing to memory using byte $\overline{CAS}$s or $\overline{WE}$s is never done. Byte reads or writes are always done external to the VRAM system via the ECC chip and/or system transceivers.

In the general case the user can think of the VRAM as being organized as a $\overline{RAS}$ and $\overline{CAS}$ per bank. When an error scrubbing during refresh cycle is in progress the DP8520/21/22 not only outputs a refresh row address and brings all four $\overline{RAS}$s low, but it then automatically multiplexes the row to the column address and brings one $\overline{CAS}$ low (depending upon the bank select bits in the 24 bit refresh counter).

When the DP8520/21/22 is programmed to allow error scrubbing during VRAM refresh cycles, a complete memory access is done during the VRAM refresh cycle. In other words, VRAM refreshes are serving the dual function of refreshing the VRAM along with accessing the VRAM. If the ECC circuitry detects a single bit error during the refresh cycle, the error can be corrected and rewritten back to the VRAM (see *Figures 38* and *39*).

It is important to note that while an error scrubbing during refresh access is being performed it is the system designer's responsibility to properly control the $\overline{WE}$ input of the VRAM. For example, $\overline{WE}$ should be high during the initial access of the VRAM. This could be accomplished by gating $\overline{RFIP}$ with the processor access circuitry that creates $\overline{WE}$. If a single bit error is found in a particular word, the corrected data can then be written back to VRAM by bringing $\overline{WE}$ low.

In order to accommodate the extra time needed during the refresh cycle, if a single bit error is to be corrected and



TL/F/9338–42

FIGURE 39. An Error Checking and Correcting Memory System May Include the Useful Feature of Memory Scrubbing During VRAM Refresh as Shown Below (Scrubbing During VRAM Refresh may Take Longer than Ordinary VRAM Refresh)

7.0 VRAM Refresh Options (Continued)

rewritten back to memory, the DP8520/21/22 extend refresh (EXTENDRF) input can be pulled high. By pulling EXTENDRF high while the $\overline{RAS}$s are low during the refresh cycle, the current refresh cycle is extended ($\overline{RAS}$s and $\overline{CAS}$s remain low) until the next rising clock edge after $\overline{EXTENDRF}$ is brought low again (see *Figures 38* and *39*).

7.5 CLEARING THE REFRESH COUNTER

If the VRAM system is always doing burst refreshes to guarantee refreshing the VRAM often enough, the system designer is probably not worried about having the ability to clear the refresh counter. But if the VRAM system is doing burst refreshes part of the time and single refreshes some of the time, it is probably important to have the ability to clear the refresh counter. The refresh counter is cleared anytime that $\overline{DISRFSH}$ is high and $\overline{RFSH}$ is low (this condition does not cause a VRAM refresh). Typically, a burst is performed by bringing $\overline{RFSH}$ low and then $\overline{DISRFSH}$ low one clock later and holding them both low until the burst is completed.

7.6 CLEARING THE REFRESH REQUEST CLOCK

The internal refresh request clock counter can be cleared by making sure that $\overline{DISRFSH}$ remains low for a minimum of 500 ns (one period of the 2 MHz internal clock). By clearing the internal refresh clock counter the user is guaranteeing that an internally requested refresh will not be generated for one refresh clock period, approximately 15 μs (see section 7.1), from the time $\overline{DISRFSH}$ goes high.

8.0 CPU Clock Frequency Options

There are two clock inputs to the DP8520/21/22, CLK and DELCLK. These two clocks may both be tied to the same clock input, or they may be two separate clocks, running at different frequencies, asynchronous to each other.

The system clock input, CLK, may be in the range of 0 hertz up to approximately 25 MHz. This clock is used for all on chip functions that require a clock (except the refresh clock and the delay line) such as;

a) All on chip arbitration (Port A, Port B, and refresh)

b) guaranteeing $\overline{RAS}$ low time during refresh (see section 4)

c) guaranteeing $\overline{RAS}$ precharge time between refreshes and/or accesses

d) determining how the wait logic (see section 5) functions with respect to the DP8520/21/22 $\overline{RAS}$ and $\overline{CAS}$ outputs

All Port A and Port B accesses are assumed to be synchronous to the system clock CLK (see section 13).

The clock input, DELCLK, may be in the range of 6 MHz to 20 MHz and should be a multiple of 2 (ie. 6, 8, 10, 12, 14, 16, 18, 20 MHz) to have the DP8520/21/22 switching characteristics hold. If DELCLK is not one of the above frequencies the accuracy of the internal delay line will suffer. This is because the phase locked loop that generates the delay line assumes an input clock frequency of 2 MHz.

For example, if the DELCLK input is at 7 MHz and we choose a divide by 3 (program bits C0–2) this will produce 2.333 MHz which is 16.667% off of 2 MHz. Therefore, the DP8520/21/22 delay line would produce delays that are 16.667% shorter (faster delays) than what is intended. If divide by 4 was chosen the delay line would be 12.5% longer (slower delays) than intended (1.75 MHz instead of 2 MHz).

The effect of these discrepancies is determined as follows:

actual minimum tRAH (programmed 15 ns tRAH) =
[20 x { (DELCLK divisor x 2 MHz ÷ DELCLK freq.) − 1}]
+ 15

actual minimum tRAH (programmed 25 ns t RAH) =
[30 x { (DELCLK divisor x 2 MHz ÷ DELCLK freq.) − 1 }]
+ 25

actual minimum tASC (programmed 0 ns tASC) =
{15 x DELCLK divisor x 2 MHz ÷ DELCLK freq.} − 15

actual minimum tASC (programmed 10 ns tASC) =
{25 x DELCLK divisor x 2 MHz ÷ DELCLK freq.} − 15

actual delay to $\overline{CAS}$ = spec + actual t RAH
− spec tRAH + actual tASC − spec tASC

The refresh clock divider, that periodically produces the internal refresh request signal, also references this 2 MHz internal clock. The exact input clock frequency is not as critical, with respect to the refresh clock period, as it is with the delay line. This is because the exact refresh clock period is not terribly critical. As long as the VRAM is guaranteed to be refreshed often enough it is not terribly important whether it is refreshed every 15.6 μs or 15.0 μs just as long as it is refreshed a minimum of every 15.6 μs.

9.0 $\overline{RAS}$ and $\overline{CAS}$ Configuration Modes

The DP8520/21/22 supports eight $\overline{RAS}$ and $\overline{CAS}$ configuration modes (see section 3.6). The basic differences among these modes are:

a) support of error scrubbing during refresh

b) support of byte writing via the inputs $\overline{ECAS}$0–1 and the $\overline{CAS}$0–3 outputs

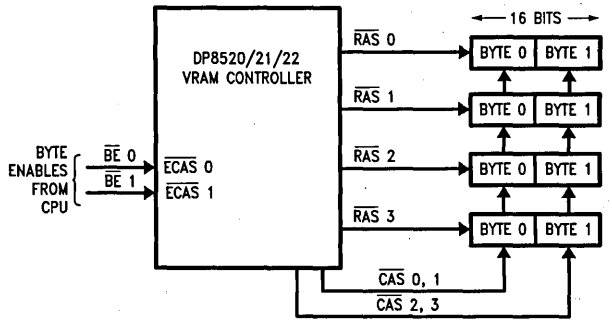
c) the number of $\overline{RAS}$ and $\overline{CAS}$ outputs that are selected during an access by the bank select inputs B1 and B0. One, two, or four $\overline{RAS}$s (and possibly $\overline{CAS}$s) may be selected during an access to go low. This allows all $\overline{RAS}$ and $\overline{CAS}$ drivers to be used regardless of how the memory is organized.

The DP8520/21/22 is specified driving 72 VRAMs, representing four banks of VRAM with 18 VRAMs per bank (one 16 bit word plus 2 parity bits) or 2 banks of 36 VRAMs each.

The DP8520/21/22 can directly drive four banks of 32 bits per bank, but the timing specs must be adjusted as described in the AC specification portion of this data sheet. For an example of three different $\overline{RAS}$ $\overline{CAS}$ configuration modes see *Figures 40a, 40b* and *40c*.

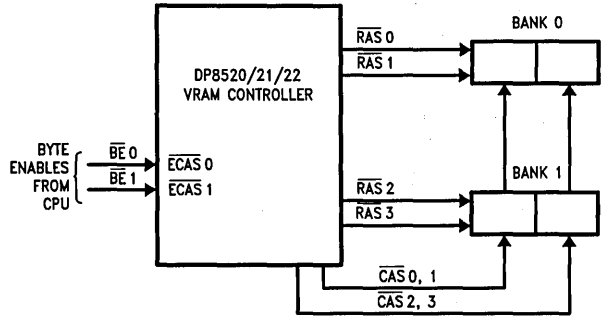
1

9.0 $\overline{RAS}$ and $\overline{CAS}$ Configuration Modes (Continued)



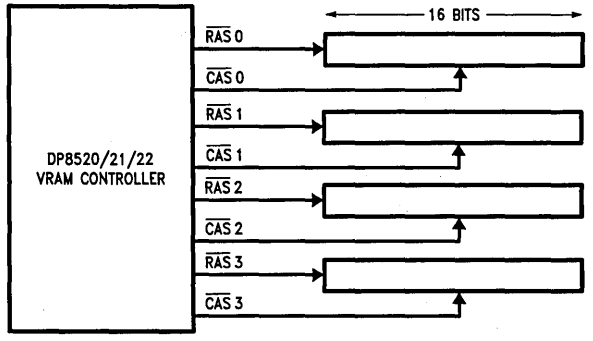
TL/F/9338-43

FIGURE 40a. $\overline{RAS}$, $\overline{CAS}$ Configuration Modes Support of Byte Writing



TL/F/9338-44

FIGURE 40b. Support of Wide Banks of Memory



TL/F/9338-45

FIGURE 40c. Support of Memory Interleaving or Error Correction (with Scrubbing During Refresh) Requires a $\overline{RAS}$/$\overline{CAS}$ Pair per VRAM Bank

10.0 VRAM Critical Timing Programming Options (tASC and tRAH)

There are two main timing parameters that must be met when controlling the access timing to a VRAM. These are the row address hold time (tRAH) and the column address setup time (tASC). Because the DP8520/21/22 contains a very precise internal delay line, there exists the ability to fine tune these two critical parameters when programming this chip (see *Figure 41*).

It is important to note that the DP8520/21/22 input DELCLK will affect the parameters tRAH and tASC. See section 8 for a detailed discussion of the effect of DELCLK on these two parameters.

The row address hold time (tRAH) is the time from $\overline{RAS}$ going low until the row address starts to change to the column address. In the DP8520/21/22, the user has a choice of 15 ns or 25 ns for tRAH.

The column address setup time (tASC) is the time from the column address being valid until $\overline{CAS}$ transitions low. In the DP8520/21/22, the user has a choice of 0 ns or 10 ns for tASC.

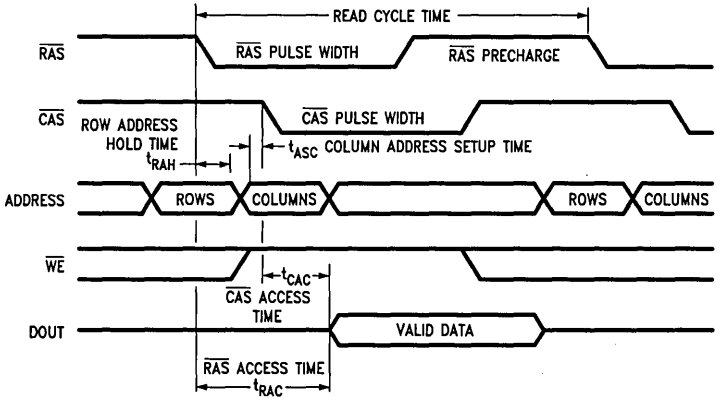
The user's choice of the two parameters will be primarily based on the particular VRAM chosen. For example, if the user was using one DP8520/21/22 to control eight banks of VRAM (each bank being 32 VRAMs in length) he would be forced to use external drivers for driving the VRAMs. In this case, he might choose to program the DP8520/21/22 with the larger tRAH and tASC to allow for skew between the outputs on the external driver chips.

11.0 Support for Late Write Accesses

In general, to gain the highest performance from a VRAM system it is necessary to start all VRAM accesses as early as possible. During a read access to the VRAM one wants as much time as possible to accomplish the access. This allows the designer to use slower VRAMs or to avoid the necessity of inserting wait states into the processor access cycles (thus achieving higher performance).

In a VRAM, if $\overline{WE}$ is low (write access to the VRAM), $\overline{CAS}$ going low latches the data into the VRAM. If write accesses are started as early as possible, the chance exists that $\overline{CAS}$ may go low before valid data is available to the VRAM. The DP8520/21/22 gets around this potential problem by providing a means to delay $\overline{CAS}$ from going low during write accesses until the rising system clock edge after $\overline{RAS}$ goes low (programming bit C9 and *Figure 42*).

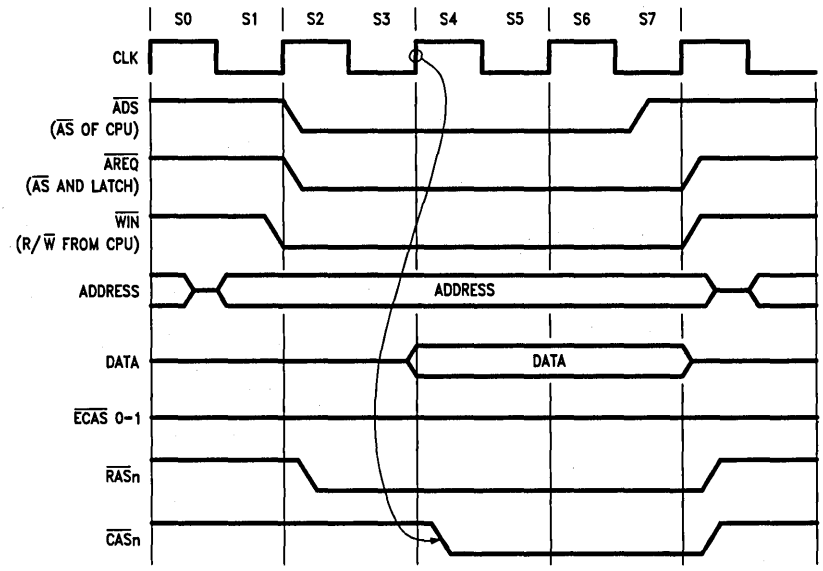
If there exists the possibility that valid data may still not be available (one period after $\overline{RAS}$ goes low) the user can further delay $\overline{CAS}$ from going low by externally controlling the $\overline{ECAS}0-1$ inputs.



TL/F/9338–46

FIGURE 41. VRAM Timing Read Access Cycle

11.0 Support for Late Write Accesses (Continued)



TL/F/9338–47

FIGURE 42. CAS Programmed Not to Go Low Until One Clock Period after RAS (next Rising CLK Edge) Goes Low During Write Access with 68000 CPU

12.0 The DP8520/21/22 Address Input Latches

The user can program (programming bit B0) whether the DP8520/21/22 address latches latch the input address while ADS or AREQB is low (with the appropriate GRANT), or remain permanently in fall-through mode.

If the address latches are used, the external address must satisfy the setup and hold requirements shown in the switching characteristics.

If the user intends to do burst mode accesses and make use of the COLINC input (auto increment of column address internal to the DP8520/21/22), the DP8520/21/22 must latch the addresses (see section 14.1.1).

The user should be cautioned that when the DP8522 is used in dual accessing applications the addresses for Port A will not be latched on-chip until both ADS is low and one system clock period has passed since GRANTB has transitioned low. Similarly, the Port B address is latched when AREQB is low and GRANTB has been high for at least one clock period. Therefore, the user will probably need to latch the addresses externally in dual accessing situations.

13.0 Access Modes Available on the DP8520/21/22

The DP8520/21/22 contains two access modes for Port A (mode 0 and mode 1, see section 3.6), and one access mode for Port B. Both of the Port A access modes are general purpose and allow an easy interface to any processor.

The Port B access mode is similar to the Port A mode 1 access mode.

A Port A access to the VRAM is initiated by three input pins, ADS, AREQ, and CS. A Port A access must be chip selected to cause the DP8520/21/22 to access the VRAM.

A Port B access to the VRAM is initiated by the input AREQB.

It is important that the inputs that initiate accesses to the VRAM (ADS, AREQ and AREQB) be synchronous to the system clock (CLK) (see AC specifications).

Once an access has been started through Port A or Port B, the DP8520/21/22 will automatically:

a) have the row address valid to the VRAMs, given that the address setup time to the DP8520/21/22 was met

b) bring appropriate RAS (or RASs) low to the VRAM

c) guarantee the programmed row address hold time (tRAH) at the VRAMs before allowing the DP8520/21/22 address outputs (Q0–Q10) to change to the column address

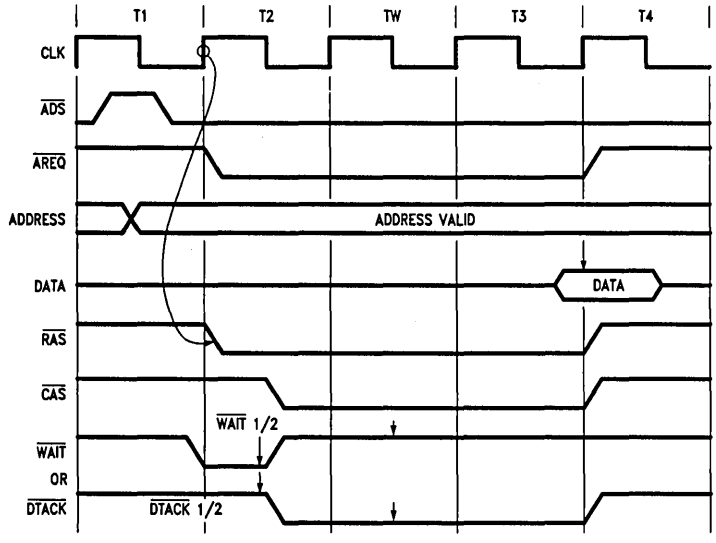
d) guarantee the programmed column address setup time (tASC) at the VRAMs before allowing the appropriate CAS (or CASs) to go low

e) hold the column address valid a minimum of 50 ns or until the access ends, depending on whether the DP8520/21/22 was programmed in interleaving or non-interleaving mode

Figure 43 shows the two access modes.

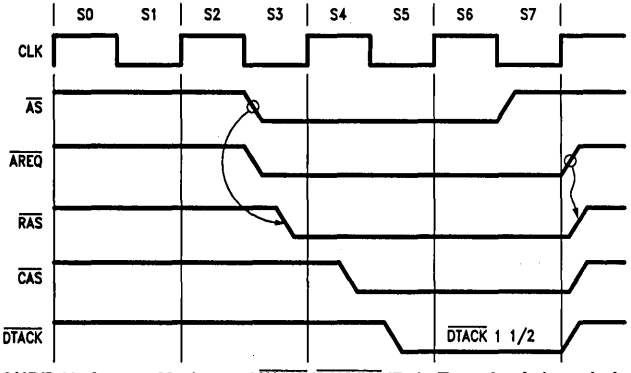
13.0 Access Modes Available on the DP8520/21/22 (Continued)

EX: Access Mode 0 (Series 32000 Like), Read Access with One Wait State



TL/F/9338–48

EX: Access Mode 1 (68000 Like)



TL/F/9338–49

FIGURE 43. Access Modes and WAIT/DTACK (Data Transfer Acknowledge)

13.1 REQUIREMENTS FOR PORT A ACCESSES USING MODE 0

Access mode 0 allows an access to be initiated from the rising edge of the system clock, CLK. When ADS pulses high an access will be initiated from the next rising edge of CLK, if the VRAM is free for an access at that time and CS is valid (*see Figure 43*). In dual-access applications (using DP8522), CS must remain valid the entire time that ADS is low. Otherwise, it need remain valid only until AREQ goes low.

When performing memory interleaving the ADS input cannot go high, to start another access, until AREQ (from the present access) has been low at least one clock period.

ADS may stay high several CLK periods but must return low before or during the clock period (period of time between two consecutive rising clock edges) when AREQ goes high.

Mode 0 is useful for processors such as the National Semiconductor Series 32000, including the NS32332, for the 8088/86/188/186/286/386, and possibly for other processors (such as 68000 family) depending upon the processor clock frequency and application. In these processors the address strobe pulses high (inverted 32000 ADS, 80286 "SO * ST" inverted) and can be tied to the ADS input of the DP8520/21/22. A read strobe gated with a write strobe could easily provide the AREQ input.

It is interesting to note that since the user programs the DP8520/21/22 as to how the wait logic should function (see section 5), he need not be concerned about when to end an access (AREQ high) if he uses a read and write strobe gated together since these outputs from the processor will not end until the access is completed.

13.0 Access Modes Available on the DP8520/21/22 (Continued)

13.2 REQUIREMENTS FOR PORT A ACCESSES USING MODE 1

Access mode 1 is very similar to access mode 0. The difference being that mode 1 allows an access to be intitiated from the low going edge of $\overline{ADS}$, if the VRAM is free to do an access at that time. Chip select ($\overline{CS}$) must be valid a setup time, tSCSADS before $\overline{ADS}$ becomes valid and be held until $\overline{ADS}$ goes invalid (high). $\overline{AREQ}$ going low at the same time as $\overline{ADS}$ or sometime later continues the access and ends the access upon going high (see *Figure 43*).

If the user is not interleaving accesses, the inputs $\overline{ADS}$ and $\overline{AREQ}$ will generally be tied to the same input signal, such as the $\overline{AS}$ output of the 68000.

If these two inputs are not tied together, $\overline{ADS}$ (for access "n") cannot transition high until some hold time (tHASAQ) after $\overline{AREQ}$ (for access "n") goes valid. If the $\overline{ADS}$ input is held low until after $\overline{AREQ}$ goes high, $\overline{AREQ}$ going high will still end the access $\overline{RAS}$. A new access will not be initiated until $\overline{ADS}$ goes high and then back low again.

During interleaving it is possible to have $\overline{ADS}$ go high (for access "n") after $\overline{AREQ}$ goes low and then have $\overline{ADS}$ return low again (for access "n" + 1) to initiate a new access (see section 6 for more information on interleaving).

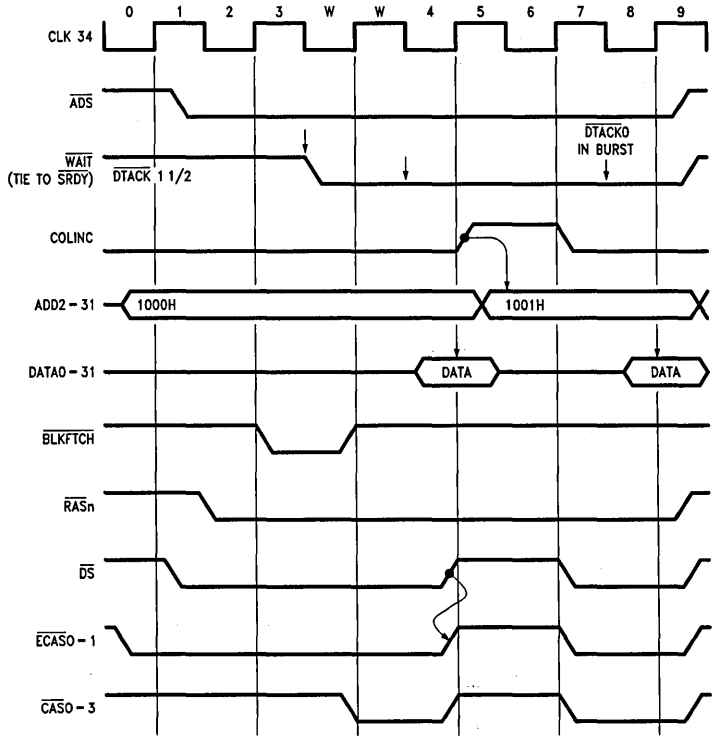
Mode 1 is useful for processors such as the 68000 family (68000/08/10/20), the 80286/386, and possibly for other processors (such as the National Semiconductor Series 32000) depending on the speed and application. In these processors the address strobe going low means that the address has been valid for some setup time and can be tied to the $\overline{ADS}$ input of the DP8520/21/22. The address strobe $\overline{AS}$ or a read strobe gated with a write strobe could easily provide the $\overline{AREQ}$ input.

Since the user programs the DP8520/21/22 as to how the wait logic should function (see section 5) that he need not be concerned about when to end an access ($\overline{AREQ}$ high) if he uses $\overline{AS}$ or a read and write strobe gated together since these outputs from the processor will not end until the access is completed.

13.3 REQUIREMENTS FOR ACCESSES THROUGH PORT B (DP8522 ONLY)

Port B allows an access to be initiated from the falling edge of the $\overline{AREQB}$ input, similar to access mode 1 of Port A. $\overline{AREQB}$ must be held low until the access is completed (see *Figure 27*).

The user should gate the Port B access request with its chip select externally to produce a $\overline{AREQB}$ input. If Port B is asynchronous to the CLK input of the DP8522, the user should externally synchronize the Port B request ($\overline{AREQB}$) to CLK. See AC specifications for $\overline{AREQB}$ to CLK requirements.



TL/F/9338-50

FIGURE 44. 32100 Burst Access Using Static Column VRAMs and DP8522

14.0 Support for Burst Mode Accesses

The DP8520/21/22 provides broad support for burst mode accesses (VRAM nibble, page, and static column modes) for Port A and Port B (DP8522 only). However, the Port B burst mode support does not include as much wait state generation support as Port A (see section 5.5).

14.1 SUPPORT FOR PORT A BURST MODE ACCESSES

Port A has the following input pins which help support burst mode type accesses: $\overline{\text{ECAS0}}$, $\overline{\text{ECAS1}}$ and COLINC. These inputs primarily affect the DP8520/21/22 logic blocks concerned with wait state generation, column address strobe ($\overline{\text{CAS0}}$–3) generation, and the address latches.

The $\overline{\text{ECAS0}}$–1 inputs allow the user to control when the $\overline{\text{CAS0}}$–3 outputs go low and high during an access. $\overline{\text{ECASn}}$ must be low for $\overline{\text{CASn}}$ to be low during an access. The DP8520/21/22 supports burst type accesses by allowing the user to connect the appropriate processor control signals to the $\overline{\text{ECASn}}$ inputs. The processor can then toggle the $\overline{\text{ECASn}}$ input during a memory access to cause $\overline{\text{CASn}}$ to toggle at the output of the DP8520/21/22 (see *Figures 20* and *26*).

The DP8520/21/22 also provides wait logic support for burst mode accesses through Port A (see section 5.3).

14.1.1 Support for Port A Burst Mode Automatic Column Address Increment

The DP8520/21/22 has the added feature of being able to support sequential burst accesses through the COLINC input. The COLINC input allows the column address to be incremented by one whenever COLINC transitions high during an access, provided that the column address is latched. This feature allows the support of a sequential page mode (or static column mode) access in which the CPU (or controller) puts out a single address and does a read or write of multiple sequential words of data (see *Figure 44*).

The user must be aware that to use the COLINC input (in Port A) he must program the DP8520/21/22 to latch the address when $\overline{\text{ADS}}$ is low (see section 12) and have chosen the non-interleaved mode (see section 6). The COLINC input has the dual function of incrementing the column address during burst mode accesses and extending refreshes when doing a refresh. Therefore, in designing external logic to support the column increment function the user should allow COLINC to go high during a burst access only when he wants the column address to be incremented.

It should be noted that if a refresh is currently in progress and an access is pending the COLINC input going high will function as the extend refresh input (EXTENDRF) and will not increment the column address of the memory access.

14.1.2 Requirements for the DP8520/21/22 $\overline{\text{ADS}}$ and $\overline{\text{AREQ}}$ Inputs when Doing Burst Mode Accesses

The input $\overline{\text{ADS}}$ must be held low the entire access in order to use the COLINC input. If the COLINC input will not be used during the burst access the $\overline{\text{ADS}}$ input need only stay low until $\overline{\text{AREQ}}$ goes low in the mode 1 access mode (see section 13). The input $\overline{\text{AREQ}}$ should be held low until it is desired to end the burst access (see *Figures 20, 26* and *44*).

14.2 SUPPORT FOR PORT B BURST MODE ACCESSES (DP8522 ONLY)

Port B allows the same support for burst mode accesses as Port A but does not include as much support in terms of the wait logic (see section 5.5). The access request input, $\overline{\text{AREQB}}$, should be held low until it is desired to end the burst access.

15.0 Support for Error Checking and Correcting (ECC) Memory Systems

The DP8520/21/22 supports ECC memory systems in a variety of ways. In section 3.5.1 an efficient method of initializing an ECC memory system with user generated data and check bits is discussed. In section 5.4 the wait state logic and the $\overline{\text{WAITIN}}$ input and its relationship to ECC is discussed. In section 7.4 error scrubbing during memory refresh is discussed. In section 9 it is shown that the programmed $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ configuration modes effect whether error scrubbing during refresh is allowed (see *Figure 38*, ECC block diagram).

The types of errors possible in a memory system can be grouped into two categories, soft errors and hard errors.

A soft error is a random non-repeatable type of error. A soft error occurs when a bit stored in memory incorrectly changes state because of such things as noise in the system, intermittent failure of memory or support chips, improper system timing, pattern sensitivity, temperature sensitivity, alpha particle radiation, ... etc. A soft error can be corrected by overwriting the erroneous data with correct data.

A hard error can be classified as an error that is always there anytime one reads a specific memory location. Hard errors can be caused by such things as stuck memory bits, memory chip failure, memory interface circuit failures, ... etc. The only way to correct a hard error in a system is to replace or repair the faulty component.

All error checking and correcting chips for memory systems on the market employ a modified hamming code. These chips (such as the National Semiconductor DP8400-2 or DP8402) allow detection and correction of all single bit errors (hard and soft) to the system host and detection of all double and some triple bit errors. It is possible to correct some multiple bit errors in a data word by applying such techniques as the double complement method. Also, only soft errors can be corrected by writing the corrected data back to memory.

The probability of a multiple bit error occurring in the memory is very slim because it means that several soft errors must occur within the same memory word. The chance of this occurring is reduced much further if the memory is being scrubbed during refresh cycles (see section 7.4).

In the rest of this section several application examples involving ECC will be discussed.

15.1 APPLICATION # 1; USING ECC WITH BUS CYCLE RETRY IN THE ERROR MONITORING MODE

If a correctable error occurs during a bus cycle some processors support a bus cycle retry feature (i.e. National Semiconductor Series 32000, 68020). This feature allows a processor to repeat the erroneous bus cycle.

15.0 Support for Error Checking and Correcting (ECC) Memory Systems (Continued)

If the system processor supports the bus cycle retry feature, an ECC memory system can be operated in an error monitoring mode. In this mode there is no performance penalty paid for including ECC in the memory system. The data that is read from the VRAM is always assumed to be correct. If a single bit error is found the appropriate control signals can be used to signal the processor to rerun the bus cycle. While the CPU is rerunning the bus cycle the ECC unit can correct the single bit error, and write the corrected data back to the VRAM. The rerun bus cycle will then access the corrected data. The system designer may want to consider adding some type of time out feature so that if a single hard error is in memory the system does not get stuck rerunning the erroneous bus cycle indefinitely (i.e. three consecutive errors in a bus cycle causes a system interrupt or bus error). If a double bit error should occur, the processor can be interrupted and the appropriate action taken.

15.2 APPLICATION #2; USING ECC WITHOUT BUS CYCLE RETRY IN THE ERROR MONITORING MODE

The "error monitoring method" could be used in a system which does not support the "bus cycle retry" feature. As in application #1 (above) there is no performance penalty paid for including ECC in the memory system when using the error monitoring method. The data that is read from the VRAM is always assumed to be correct.

In this application all single bit error correction takes place within the scrubbing during refresh cycles. Since a single memory location gets scrubbed approximately every 15 μs and the DP8520/21/22 allows up to four banks of 4 Mbit VRAMs (24 bit scrubbing refresh counter) the entire memory will be scrubbed every 4.2 minutes. By continuous scrubbing of the entire memory the probability of the processor seeing a single bit error is greatly reduced (compared to a non-scrubbing during refresh system).

If a single or multiple bit error should occur the processor can be interrupted and the appropriate action taken.

15.3 APPLICATION #3, USING ECC IN THE ALWAYS CORRECT MODE

If a memory system uses ECC in the "always correct mode" the memory system will pay a performance penalty. The "always correct method" involves always running the memory data through the ECC circuitry before giving it to the processor. By doing this the processor is always guaranteed to get correct data even if the data has a single bit error (hard or soft error). Because the data is always run through the ECC unit, wait states must usually be inserted into the processor access cycle to allow for the extra time this takes. Therefore, this method is not as performance efficient as the previously mentioned methods. If the data has multiple bit errors the processor can be interrupted and appropriate action can be taken.

If a single bit error is found, the corrected data can be written back to the VRAM during the present access cycle or left alone, allowing the appropriate scrubbing during refresh cycle to correct it.

16.0 Dual Access of the VRAM with the DP8522

The DP8522 has the built in arbitration circuitry necessary to support two separate ports (A and B) and refresh (internally or externally controlled). VRAM refresh has the highest priority followed by the currently granted port. The ungranted port has the lowest priority. The "most recently used" arbitration algorithm is used to determine access priority on the DP8522. This means that the currently granted port (A or B) will stay granted until the condition of a rising system clock edge with no access request from the currently granted port (A or B) and an access request from the other port occurs. At this point GRANT will switch to grant VRAM access rights to the other port.

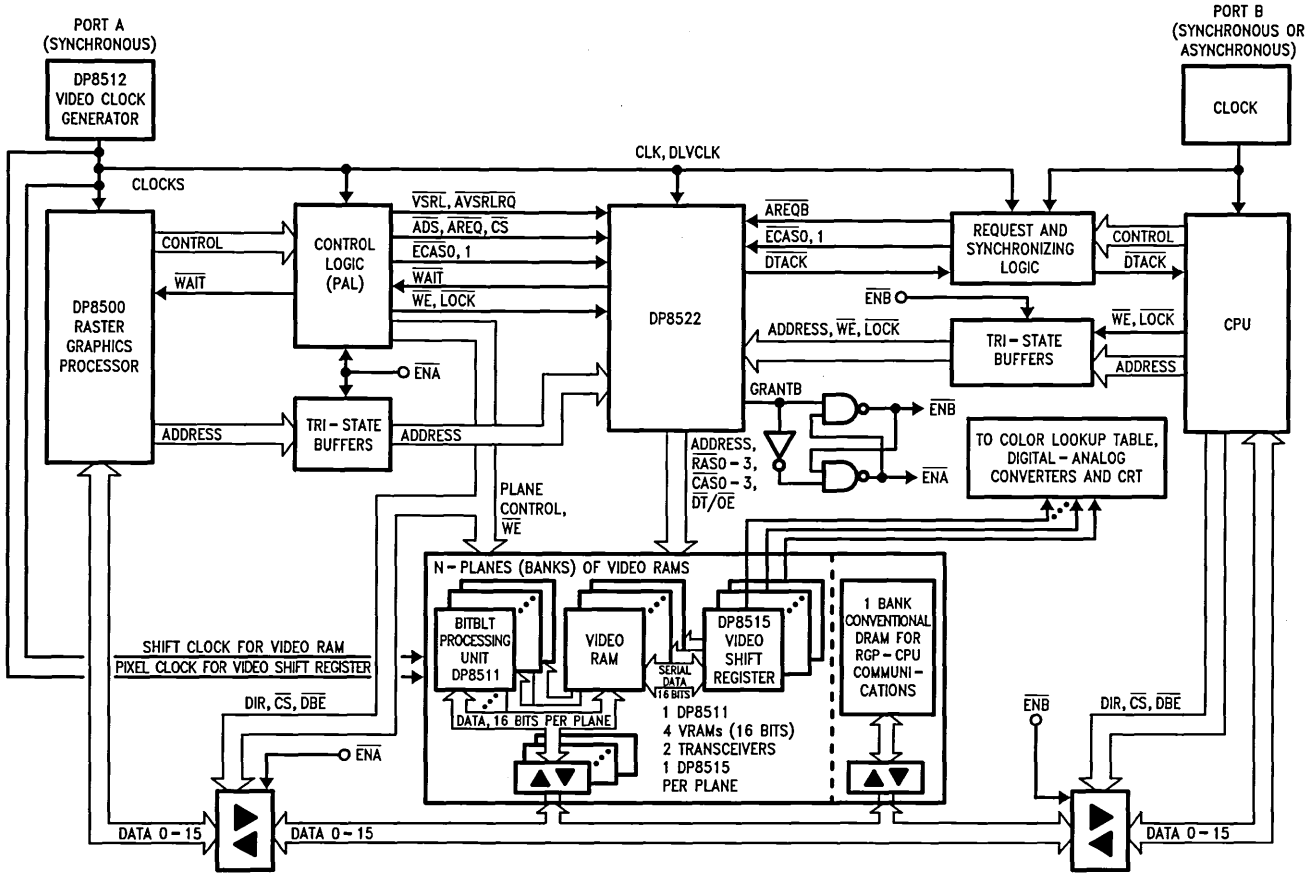
It should be noted that $\overline{CS}$ should be kept low, from Port A, during the entire Port A access ($\overline{ADS}$, $\overline{AREQ}$ low). This guarantees that GRANTB does not change to Port A unless a $\overline{CS}$ access from Port A is pending.

The access functions supported by Ports A and B have been discussed in section 13 (access modes available on the DP8522). The address latches in relation to dual accessing have been discussed in section 12.

The processors connected to Ports A and B could be completely different (different processors, clock speeds, bus cycles, . . . etc.).

A GRANTB output of the DP8522 can be used externally to multiplex the addresses, $\overline{LOCK}$ input, $\overline{CAS}$ enables, and $\overline{WIN}$ input of the particular port granted to the DP8522. When GRANTB is high, Port B is granted; while low, Port A is granted. The DP8522 holds a pending access from a particular port from starting until one clock period (CLK) after GRANTB becomes valid for the particular port. This allows time for the granted port's address and control signals to become valid at the VRAM inputs before a VRAM access is allowed to start. Once a port has become granted its accesses are allowed to start immediately when requested, unless a refresh is in progress or $\overline{RAS}$ precharge is not completed (see *Figures 45* and *27*).

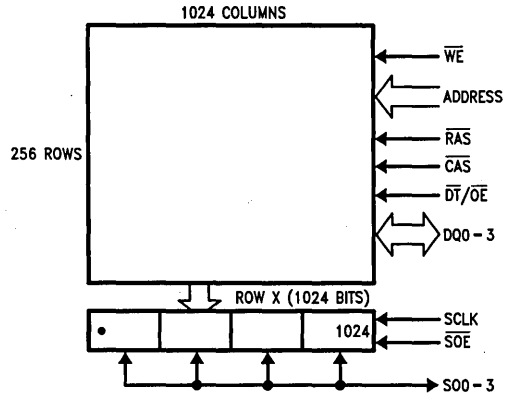
Dual Accessing Using the DP8522



TL/F/9338–51

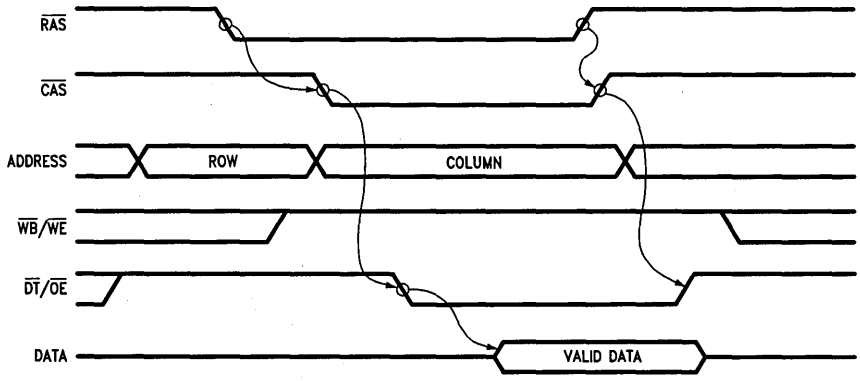
FIGURE 45. Dual Accessing using the DP8522. A CPU and the National Semiconductor DP8500 Advanced Graphics Chip Set both have access to the memory (video and conventional DRAM).

16.0 Dual Access of the VRAM with the DP8522 (Continued)



TL/F/9338–52

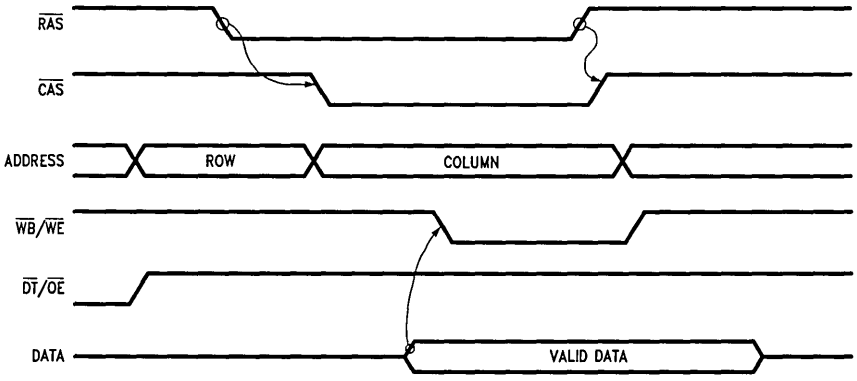
FIGURE 46. The Video RAM (A Dual Ported Memory)
Ideal solution for graphics frame buffer. Screen refresh can occur at the same time as random access to the frame buffer for screen update and manipulation.



TL/F/9338–53

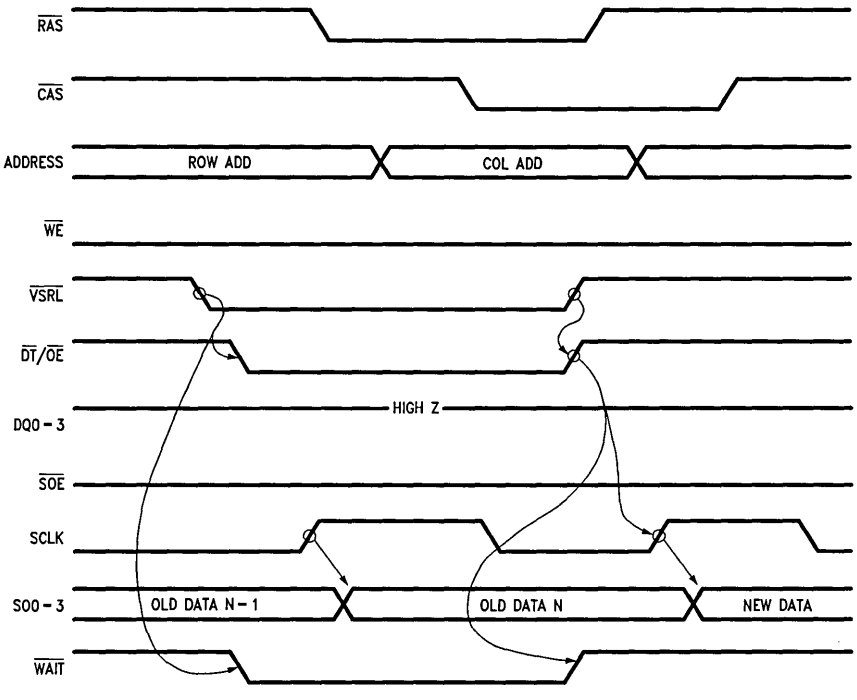
FIGURE 47. Video RAM Random Access Read Cycle
(See Section 22.0 number 3 for further information)

16.0 Dual Access of the VRAM with the DP8522 (Continued)



TL/F/9338–54

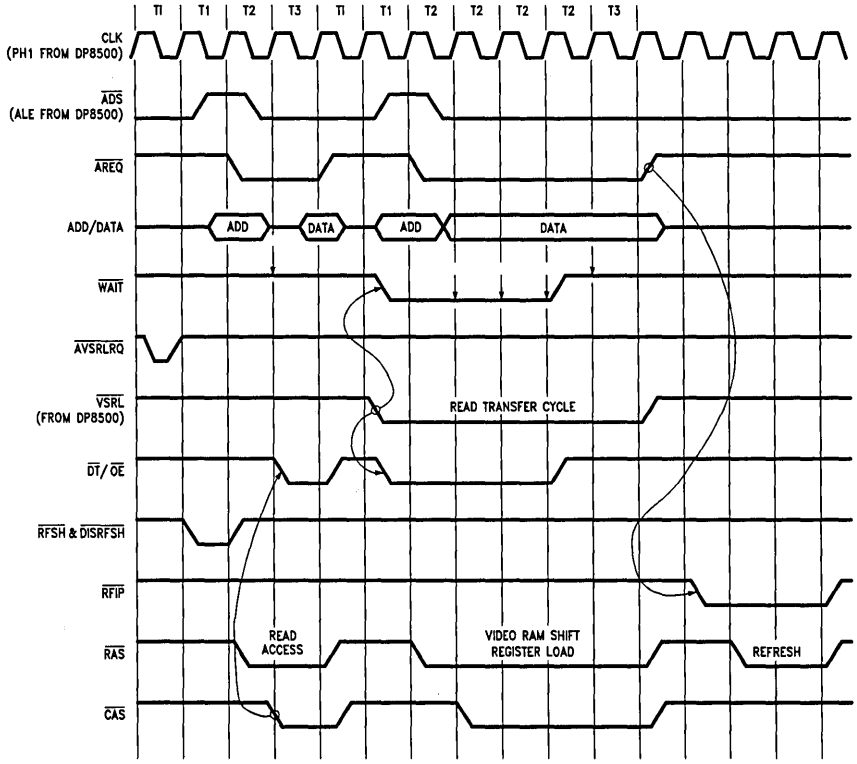
FIGURE 48. Video RAM Random Access Write Cycle



TL/F/9338–55

FIGURE 49. Video RAM Timing READ Transfer Cycle, B Port Active (Transfer VRAM Row Data into Shift Register)

16.0 Dual Access of the VRAM with the DP8522 (Continued)



TL/F/9338–56

FIGURE 50. The DP8500 Raster Graphics Processor Interfaced to the DP8520/22 Video RAM Controller

16.1 THE PORT LOCK FUNCTION

When the DP8522 is being used as a dual port VRAM controller the $\overline{LOCK}$ input allows the currently granted port to lock out the other port. In other words, if Port B is granted access to the VRAMs (GRANTB is high) it can bring $\overline{LOCK}$ low thereby disallowing Port A from accessing the VRAM, until $\overline{LOCK}$ is brought high.

Note that $\overline{LOCK}$ being low does not disable refreshes from happening, but only holds GRANTB valid to the particular port.

17.0 DP8520/21/22 Video RAM Support

The DP8520/21/22 provides full support for all access modes of video RAMs through the addition of three pins ($\overline{AVSRLRQ}$, $\overline{VSRL}$, and $\overline{DT/OE}$) to the standard DP8420/21/22. The access modes of video RAMs can be split up into two groups; video RAM transfer cycles (read with the serial port in active or in standby mode, write, and pseudo write transfer cycles), and non-transfer cycles. The DP8520/21/22 support of video RAMs allows the full capabilities of the National Semiconductor Advanced Graphics chip set (DP8500 Series) to be realized. See *Figures 45, 46, 47, 48, 49* and *50.*

17.1 SUPPORT FOR VRAM TRANSFER CYCLES (TO THE SERIAL PORT OF THE VRAM)

The DP8520/21/22 supports VRAM transfer cycles with the serial port in the active or standby mode. Active or standby refers to whether data is or is not currently being shifted in or out of the VRAM serial port (i.e., whether the shift clock is currently active). The DP8520/21/22 support for data transfer cycles with the serial port in the active mode includes the ability to support transfer cycles with the serial port in the standby mode. Hereafter, the term VRAM transfer cycle means VRAM transfer cycle with the serial port in the active mode.

In order to support VRAM transfer cycles, the DP8520/21/22 must be able to guarantee timing with respect to its input CLK (which must be synchronous to VRAM shift clock), $\overline{RAS}$, $\overline{CAS}$, and $\overline{DT/OE}$. *Figure 50* shows the timing of a graphics memory system where the DP8520/21/22 is being used with the National Semiconductor DP8500 Raster Graphics Processor (RGP). If the DP8520/21/22 is being used in a graphics frame buffer application, it has the ability to support a VRAM transfer cycle during active video time (ex. mid scan line). This is one of the very attractive features supported by the National Semiconductor Advanced Graphics chip set. Most of the commercial graphics controller chip sets available will only support VRAM transfer cycles during blanking periods (while the VRAM is in standby mode).

17.0 DP8520/21/22 Video RAM Support (Continued)

The DP8520/21/22 supports VRAM transfer cycles during active video time by being able to guarantee an exact instant during which the transfer of VRAM data to the VRAM shift register will occur. This exact instant can be guaranteed through the $\overline{AVSRLRQ}$ and $\overline{VSRL}$ inputs.

The input $\overline{AVSRLRQ}$ disables any further internally or externally requested refreshes or Port B access requests from being executed. The $\overline{AVSRLRQ}$ input does this by making the VRAM controller arbitration logic think that a Port A access is in progress from the point where the $\overline{AVSRLRQ}$ input goes low until the VRAM shift register load operation is completed. *Figure 50* shows the case of an externally requested refresh being disabled, because of a previous $\overline{AVSRLRQ}$, until the VRAM shift register load has been completed.

The $\overline{VSRL}$ input causes the $\overline{DT}/\overline{OE}$ output to transition low immediately, regardless of what else may be happening in the DP8520/21/22 (see *Figures 49* and *50*). Therefore, it is the system designer's responsibility to guarantee that all pending accesses have been completed by the time the $\overline{VSRL}$ input transitions low. The system designer can guarantee this by issuing $\overline{AVSRLRQ}$ far enough in advance to guarantee that all pending accesses have been completed by the time $\overline{VSRL}$ transitions low.

Generally, the $\overline{VSRL}$ is the status of the upcoming access cycle (of the graphics processor). Therefore, this input precedes the inputs $\overline{ADS}$ and $\overline{AREQ}$ that execute the VRAM shift register load transfer cycle. This sequence of events guarantees the correct relationship of $\overline{DT}/\overline{OE}$, $\overline{RAS}$ and $\overline{CAS}$ ($\overline{DT}$ preceding $\overline{RAS}$ and $\overline{CAS}$ when transitioning low and high). The wait logic is intimately connected to the graphics functions on the DP8520/21/22. Wait states are inserted into the VRAM transfer cycle until $\overline{VSRL}$ transitions high or until four rising clock (CLK) edges from $\overline{VSRL}$ going low, whichever occurs first. The $\overline{DT}$ output functions the same way. In other words, $\overline{DT}$ goes low when $\overline{VSRL}$ goes low, and stays low until $\overline{VSRL}$ goes high, or until four rising clock edges from $\overline{VSRL}$ going low, whichever happens first. This allows $\overline{DT}$ to transition high before $\overline{RAS}$ and $\overline{CAS}$ transition high, thus guaranteeing the correct timing relationship during the transfer cycle (see *Figure 50*). The $\overline{WE}$ input of the VRAM determines whether the access is a read or write transfer cycle.

17.2 SUPPORT FOR VRAM ACCESS CYCLES THROUGH PORT A USING THE DP8520/21/22

During read and write accesses the $\overline{DT}/\overline{OE}$ output will be held high. See Appendix (section 22) number 3 for more information.

During a transfer cycle ($\overline{VSRL}$ low during the access) $\overline{WIN}$ is disabled from affecting the $\overline{DT}/\overline{OE}$ logic until the transfer cycle is completed as shown by $\overline{CAS}$ transitioning high.

18.0 Test Mode

The error scrubbing during refresh mode cannot be used with the staggered refresh mode. This particular combination of modes is used as a test mode of the DP8520/21/22. It divides the 24 bit refresh counter into a 13-bit and an 11-bit counter. During refreshes both counters are incremented. This is done to reduce test time.

19.0 Absolute Maximum Ratings*

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
All Input or Output Voltage with Respect to GND	−0.5V to +7V
Power Dissipation @ 20 MHz	0.5W
ESD rating to be determined.	

Note: *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.*

20.0 DC Electrical Characteristics* $T_A = 0°$ to $+70°$, $V_{CC} = 5V \pm 10\%$, GND = 0V

Symbol	Characteristics	Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage	Tested with a Limited Functional Pattern	2.0		$V_{CC} + 0.5$	V
V_{IL}	Logical 0 Input Voltage	Tested with a Limited Functional Pattern	−0.5		0.8	V
V_{OH1}	Q and $\overline{DT}/\overline{OE}$ Outputs	$I_{OH} = -10$ mA			$V_{CC} - 1.0$	V
V_{OL1}	Q and $\overline{DT}/\overline{OE}$ Outputs	$I_{OL} = 10$ mA			0.5	V
V_{OH2}	All Outputs Except Q_S, $\overline{DT}/\overline{OE}$	$I_{OH} = -3$ mA			$V_{CC} - 1.0$	V
V_{OL2}	All Outputs Except Q_S, $\overline{DT}/\overline{OE}$	$I_{OL} = 3$ mA			0.5	V
I_{IN}	Input Leakage Current	$V_{IN} = V_{CC}$ or GND			±10	μA
I_{ILML}	$\overline{ML}$ Input Current (Low)	V_{IN} = GND			200	μA
I_{CC1}	Quiescent Current	CLK at 20 MHz (Inputs Inactive)		10		mA
I_{CC2}	Supply Current	CLK at 20 MHz (Inputs Active, $I_{OL} = 0$ mA)		20		mA
C_{IN}	Input Capacitance	f_{IN} at 1 MHz			10	pF

*These are preliminary specifications

21.0 Preliminary Switching Characteristics: DP8520/21/22

Unless otherwise stated V_{CC} = 5.0V ±10%, 0 < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 VRAMs per bank, including trace capacitance.

Load Capacitance = $\overline{DT}/\overline{OE}$, Q0–Q10, CL = 380 pF; $\overline{RAS}$0–3, $\overline{CAS}$0–3, C_L = 125 pF; all other outputs, C_L = 50 pF. See *Figures 51, 52* and *54*. Maximum propagation delays are specified with all outputs switching simultaneously.

Number	Symbol	Access Parameter	Min	Max	Units
ACCESS MODE 0 SWITCHING CHARACTERISTICS					
A1	tSCSCK	$\overline{CS}$ Setup to CLK (Rising Edge)	15		ns
A2	tSADSCKNL	$\overline{ADS}$ High Setup to CLK (Rising Edge), Not Using the On-Chip Address Latches	20		ns
A3	tSADSCKL	$\overline{ADS}$ High Setup to CLK (Rising Edge), if Using the On-Chip Address Latches	45		ns
A4	tWADS	$\overline{ADS}$ Pulse Width, to Start an Access, or to Latch the Input Address	15		ns
A5	tSBADDCK	Bank Address (B0,1) Setup to CLK (Rising Edge) that Initiates $\overline{RAS}$n	25		ns
A6	tSADDCK	Access Mode 0 Row/Column Address Setup to CLK (Rising Edge) that Initiates $\overline{RAS}$n	15		ns
A7	tPCKRL	CLK (Rising Edge) to $\overline{RAS}$ Low		35	ns
A8	tPCKCL	CLK (Rising Edge) to $\overline{CAS}$ Low (with tASC = 0, tRAH = 15 ns)		95	ns
A9	tHCKADS0	CLK Rising Edge to $\overline{ADS}$ High to Guarantee Correct Refresh/ Access Arbitration	3		ns
ACCESS MODE 1 SWITCHING CHARACTERISTICS					
B1	tSADSCK	$\overline{ADS}$ Low to CLK (Rising Edge) Setup Time	15		ns
B2	tSCSADS	$\overline{CS}$ to $\overline{ADS}$ Low Setup Time	5		ns
B3	tPADSRL	$\overline{ADS}$ Low to $\overline{RAS}$ Low During an Access		40	ns
B4	tPADSCL	$\overline{ADS}$ Low to $\overline{CAS}$ Low During an Access		100	ns
B5	tSADDADS	Address Setup to $\overline{ADS}$ Low During an Access	10		ns
B6	tHADDADS	Address Hold from $\overline{ADS}$ Low During an Access, if Using the On-Chip Latches	20		ns
B7	tHCKADS1	CLK Rising Edge to $\overline{ADS}$ Low to Guarantee Correct Refresh/ Access Arbitration	5		ns
B8	tSWADS	$\overline{WAITIN}$ Low Setup to $\overline{ADS}$ Low			
B9	tSADSCKW	$\overline{ADS}$ Low Setup to CLK Rising Edge to Guarantee Correct Functioning of the $\overline{WAIT}/\overline{DTACK}$ Logic	36		ns
COMMON SWITCHING CHARACTERISTICS					
C1	tPENCH,L	$\overline{ECAS}$0–1 High or Low to $\overline{CAS}$ High or Low		40	ns
C3	tPCINCQ	COLINC High to Q's Output Column Address Incremented		55	ns
C4	tSCINEN	COLINC High Setup to $\overline{ECAS}$0–1 Low to Guarantee Q's Output Column Address is Valid 0 ns before $\overline{CAS}$0–3 Transitions Low	25		ns
C5	tPAQ	Address Input to Q's Outputs Valid		45	ns
C6	tPADSWL	$\overline{ADS}$ to $\overline{WAIT}$ Low (Programmed as $\overline{WAIT}$)		57	ns
C7	tPCLKWH	CLK to $\overline{WAIT}$ High (Programmed as $\overline{WAIT}$)		46	ns
C8	tPCLKDL	CLK to $\overline{WAIT}$ Low (Programmed as $\overline{DTACK}$)		43	ns
C9	tPAREQDH	$\overline{AREQ}$ to $\overline{WAIT}$ High (Programmed as $\overline{DTACK}$)		40	ns

21.0 Preliminary Switching Characteristics: DP8520/21/22

Unless otherwise stated V_{CC} = 5.0V ±10%, 0 < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 VRAMs per bank, including trace capacitance.

Load Capacitance = $\overline{DT}/\overline{OE}$, Q0–Q10, CL = 380 pF; $\overline{RAS}$0–3, $\overline{CAS}$0–3, C_L = 125 pF; all other outputs, C_L = 50 pF. See *Figures 51, 52* and *54*. Maximum propagation delays are specified with all outputs switching simultaneously. (Continued)

Number	Symbol	Access Parameter	Min	Max	Units
COMMON SWITCHING CHARACTERISTICS (Continued)					
C10	tPADSD	$\overline{ADS}$ Low to $\overline{WAIT}$ Low (Programmed as $\overline{DTACK}$ 0T from $\overline{RAS}$), $\overline{ADS}$ May Be Tied to $\overline{AREQ}$		44	ns
C11	tPCKG	CLK (Rising Edge) to GRANTB Valid		35	ns
C12	tSADDCK	Address Setup to CLK (Rising Edge) that Initiates $\overline{RAS}$n when Using the DP8522 in a Dual Access Application	0		ns
C13	tSARQCK1	$\overline{AREQ}$ High Setup to CLK Rising Edge (One Period of $\overline{RAS}$ Precharge Programmed, this Guarantees that the First CLK Rising Edge is Seen as One Period of Precharge)	50		ns
C13	tSARQCK2	$\overline{AREQ}$ High Setup to CLK Rising Edge (Two or Three Periods of $\overline{RAS}$ Precharge Programmed, this Guarantees that the First CLK Rising Edge is Seen as One Period of Precharge)	35		ns
C14	tHMLADD	$\overline{ML}$ High to Mode Addresses Allowed to Change	10		ns
C15	tHRASWE	$\overline{RAS}$ Low to $\overline{WIN}$ Low to Guarantee $\overline{CAS}$n is Held High for a Write Access (Where the Chip is Programmed to Hold $\overline{CAS}$n High Until the Next Rising CLK Edge)	10		ns
C16	tSWCK	$\overline{WAITIN}$ Low Setup to CLK Rising Edge (to Guarantee Adding Extra Wait States)	6		ns
C17	tSLOCKCK	$\overline{LOCK}$ Low Setup to CLK Rising Edge (to Guarantee Locking the Current Port)	0		ns
C18	tPCKRAS	CLK Rising Edge (after Completion of Precharge Time) to $\overline{RAS}$n Low		35	ns
C19	tPARQCAS1	$\overline{AREQ}$ High to $\overline{CAS}$n High (During INTERLEAVED Mode)		48	ns
C20	tPARQCAS2	$\overline{AREQ}$ High to $\overline{CAS}$n High (During NONINTERLEAVED Mode)		54	ns
C21	tPRASCAS1	$\overline{RAS}$n to $\overline{CAS}$n (tRAH = 15 ns, tASC = 0 ns)		60	ns
C22	tPRASCAS2	$\overline{RAS}$n to $\overline{CAS}$n (tRAH = 15 ns, tASC = 10 ns)		70	ns
C23	tPRASCAS3	$\overline{RAS}$n to $\overline{CAS}$n (tRAH = 25 ns, tASC = 0 ns)		70	ns
C24	tPRASCAS4	$\overline{RAS}$n to $\overline{CAS}$n (tRAH = 25 ns, tASC = 10 ns)		80	ns
C25	tPARQRAS	$\overline{AREQ}$ High to $\overline{RAS}$n High		50	ns
C26	tD1	Difference Between Access $\overline{RAS}$n High (from $\overline{AREQ}$ High) to Refresh $\overline{RAS}$n Low (from CLK Rising Edge) During the Access/Refresh Precharge Time (tPARQRAS–tPCKRAS)			
C27	tD2	Difference Between Refresh $\overline{RAS}$n High (from CLK Rising Edge) to Access $\overline{RAS}$n Low (from CLK Rising Edge for both Access Mode 0 and 1) During the Refresh/Access Precharge Time (tPCKRFASH–tPCKRAS)			
C28	tD3	Difference Between Access $\overline{RAS}$n High (from $\overline{AREQ}$ High) to Access Port B RASn Low (from CLK Rising Edge) During Port A to Port B Precharge Time (tPARQRAS–tPCKRASB)			
C29	tD4	Difference Between Port B Access $\overline{RAS}$n High (from $\overline{AREQB}$ High) to Access Port A $\overline{RAS}$n Low (from CLK Rising Edge) During Port B to Port A Precharge Time (tPARQRASH–tPCKRAS)			

21.0 Preliminary Switching Characteristics: DP8520/21/22

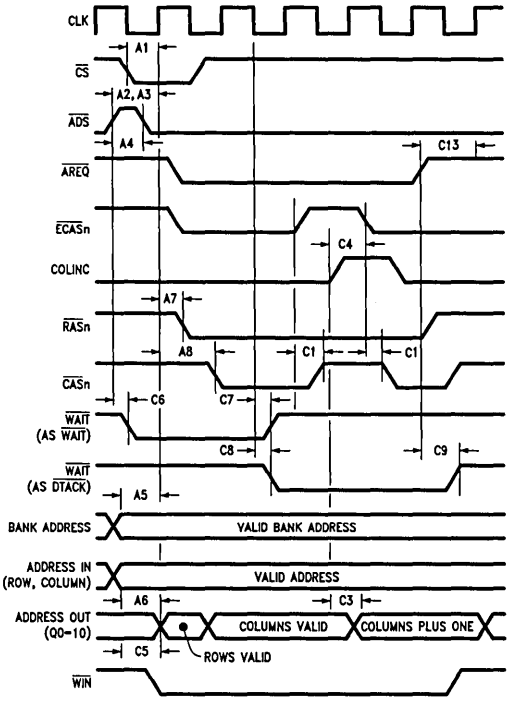
Unless otherwise stated V_{CC} = 5.0V ±10%, 0 < T_A < 70°C, the output load capacitance is typical for 4 banks of 18 VRAMs per bank, including trace capacitance.

Load Capacitance = $\overline{DT}/\overline{OE}$, Q0–Q10, CL = 380 pF; $\overline{RAS}$0–3, $\overline{CAS}$0–3, C_L = 125 pF; all other outputs, C_L = 50 pF. See *Figures 51, 52* and *54*. Maximum propagation delays are specified with all outputs switching simultaneously. (Continued)

Number	Symbol	Access Parameter	Min	Max	Units
COMMON SWITCHING CHARACTERISTICS (Continued)					
C30	tD5	Difference Between Refresh $\overline{RAS}$n Low (from CLK Rising Edge) to Refresh $\overline{RAS}$n High (from CLK Rising Edge) During Refresh Precharge Time (tPCKRFRASL–tPCKRFRASH)			
C31	tD6	Difference Between Access $\overline{RAS}$n High (from (AREQ high) to Access $\overline{RAS}$n Low (from $\overline{ADS}$ Low) for Access Mode 1 (tPARQRAS–tPADSRL)		10	ns
C32	tD7	Difference Between Access $\overline{RAS}$n High (from $\overline{AREQ}$ High) to Access $\overline{RAS}$n Low (from Rising Clock Edge) for Access Mode 0 (tPARQRAS–tPCKRL)		10	ns
PORT B SWITCHING CHARACTERISTICS					
D1	tHCKARQB	CLK Rising Edge to $\overline{AREQB}$ Low to Guarantee Correct Refresh/ Port B Access Arbitration	2		ns
D2	tSARQBCK	$\overline{AREQB}$ Low Setup to CLK Rising Edge to Guarantee Correct Port A/Port B Arbitration	6		ns
D3	tPCKRASB	CLK Rising Edge to $\overline{RAS}$ Valid for Pending Port B Access after GRANTB		50	ns
D4	tPARQBRASL	$\overline{AREQB}$ Low to $\overline{RAS}$ Low for Port B		50	ns
D5	tPARQBRASH	$\overline{AREQB}$ High to $\overline{RAS}$ High for Port B		50	ns
D6	tPARQBATKB	$\overline{AREQB}$ Low to $\overline{ATACKB}$ Low for Port B		50	ns
D7	tPCKATKB	CLK Rising Edge to $\overline{ATACKB}$ Low for Port B Access that has been Pending		50	ns
REFRESH SWITCHING CHARACTERISTICS					
E1	tSRFCK	$\overline{RFSH}$ Low Setup to CLK Rising Edge	20		ns
E2	tSDRFCK	$\overline{DISRFSH}$ Low Setup to CLK Rising Edge	20		ns
E3	tSCINCCK1	EXTENDRFSH High Setup to CLK Rising Edge (to Extend $\overline{RAS}$n During Refresh)	15		ns
E4	tSCINCCK2	EXTENDRFSH Low Setup to CLK Rising Edge (to End $\overline{RAS}$n During Refresh)	15		ns
E5	tPCKRFL	CLK Rising Edge to $\overline{RFIP}$ Low (Refresh Starting)		45	ns
E6	tPARQRF	$\overline{AREQ}$ High to $\overline{RFIP}$ Low (for Pending Refresh During Access)		65	ns
E7	tPCKRFH	CLK Rising Edge to $\overline{RFIP}$ High (Refresh Ending)		55	ns
E8	tPCKRFRASH	CLK Rising Edge to Refresh $\overline{RAS}$ Ending		40	ns
E9	tPCKRFRASL	CLK Rising Edge to Refresh $\overline{RAS}$ Starting		35	ns
E10	tPARQAD	$\overline{AREQ}$ High to $\overline{RFSH}$ Address Valid for a Pending Refresh		58	ns
GRAPHICS SWITCHING CHARACTERISTICS					
F1	tSCKVSRL	$\overline{VSRL}$ Low Setup to CLK Rising Edge to Guarantee Counting $\overline{VSRL}$ as Being Low (Used to Determine When to End Graphics Shift Load Access)	15		ns
F2	tHVSRLCK	$\overline{VSRL}$ Low from CLK Rising Edge (to Guarantee $\overline{VSRL}$ Is Not Counted as Being Low until the Next Rising Clock Edge)	6		ns
F3	tSCKAVSRL	$\overline{AVSRLRQ}$ Low before CLK Rising Edge to Guarantee Locking the VRAM to Only Port A Accesses	15		ns
F4	tPVSRLDT	$\overline{VSRL}$ Low to $\overline{DT}$ Low During Graphics Shift Register Load Access		35	ns

21.0 Preliminary Switching Characteristics: DP8520/21/22 (Continued)

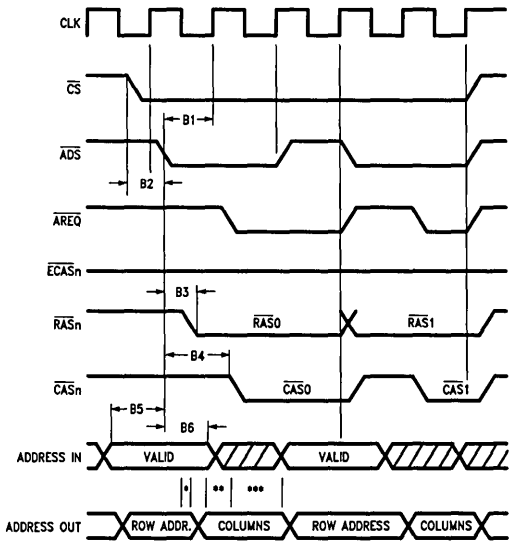
Access Mode 0



TL/F/9338-58

FIGURE 51. Access Mode 0, Noninterleaved, Timing Diagram

Access Mode 1, Interleaved, Using Latches

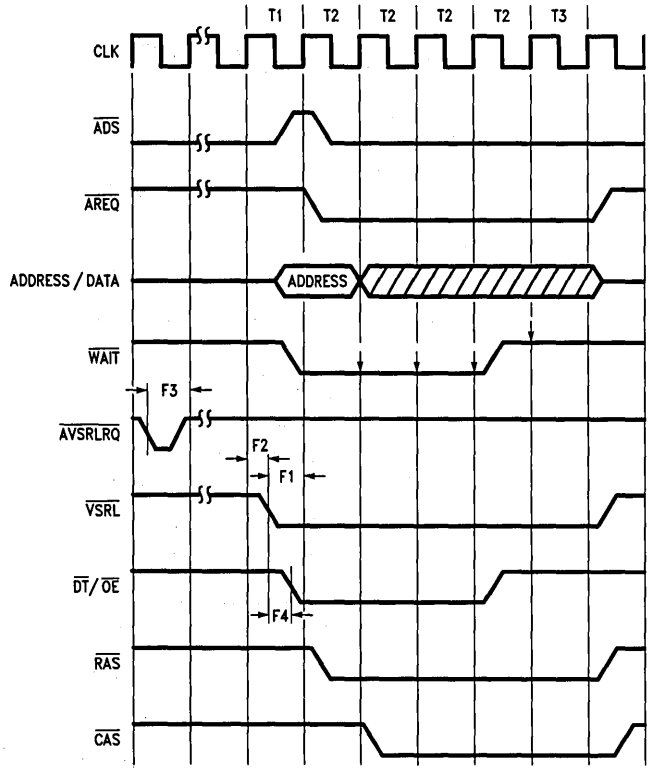


*tRAH
**tASC
***tCAH

TL/F/9338-59

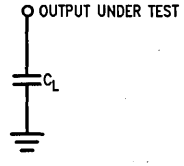
FIGURE 52. Access Mode 1, Interleaved Timing Diagram

21.0 Preliminary Switching Characteristics: DP8520/21/22 (Continued)



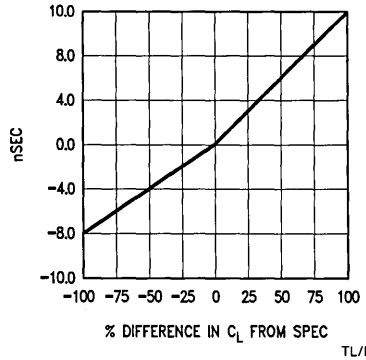
TL/F/9338–57

FIGURE 53. Graphics Timing Diagram



TL/F/9338–60

FIGURE 54. Test Load



TL/F/9338–61

FIGURE 55. Change in Propagation Delay vs. Percentage Change in Load Capacitance Relative to AC Switching Characteristics Specified Load

22.0 Appendix: Differences between the DP8520/21/22 and the DP8520A/21A/22A and How the User Can Guarantee Compatibility between These Parts in His Design

1) The DP8520A/21A/22A will allow the user to extend $\overline{CAS}$n beyond $\overline{RAS}$n. $\overline{CAS}$n can be extended up to the next rising system clock after $\overline{RAS}$n transitions high, in the NONINTERLEAVED MODE, by holding $\overline{ECAS}$n low after $\overline{RAS}$n transitioned high. This is useful in systems where it would normally be difficult to guarantee $\overline{RAS}$ precharge time, such as in consecutive accesses to the same bank, without inserting extra wait states in each access. By ending $\overline{RAS}$n earlier in the access, and allowing $\overline{CAS}$n to hold the data valid (in a read access cycle), up to an extra system clock period of $\overline{RAS}$ precharge time can be gained in consecutive accesses to the same memory bank (same $\overline{RAS}$).

   In the DP8520/21/22 the $\overline{RAS}$n output transitioning high ended $\overline{CAS}$n.

   Since $\overline{CAS}$n can be extended up to one system clock period (next rising system clock) after $\overline{RAS}$n transitions high (DP8520A/21A/22A), the user should make sure that $\overline{CAS}$n will not be low when $\overline{RAS}$n transitions low for the next access. This would cause a $\overline{CAS}$ before $\overline{RAS}$ refresh in most VRAMs. Besides this potential problem, holding the $\overline{ECAS}$n inputs low after $\overline{RAS}$n transitions high will not cause compatibility problems in most systems.

   Another way to guarantee compatibility between the two versions of the DP8520/21/22 is to gate access request with the $\overline{ECAS}$n input logic. In this way the $\overline{ECAS}$n inputs will only be low during an access, allowing the $\overline{CAS}$n outputs to be low only while $\overline{RAS}$n is low for the access.

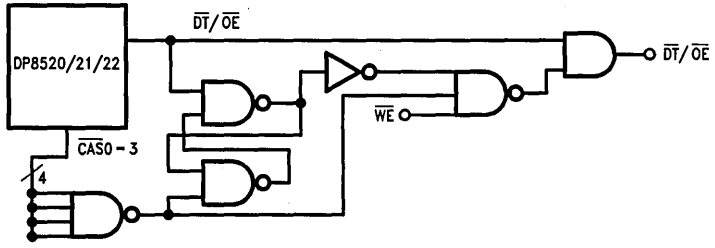
2) Another mode may be added to the DP8520A/21A/22A. This mode will be programmed if the $\overline{ECAS}$0 input is high during mode load.

   To remain compatible with the DP8520/21/22 the user should hold $\overline{ECAS}$0 low during mode load.

3) The DP8520A/21A/22A will provide full support for VRAMs. The DP8520/21/22 did provide support for VRAMs in terms of bringing $\overline{DT}/\overline{OE}$ low during the VRAM shift register load, but it did not bring $\overline{DT}/\overline{OE}$ low during VRAM read accesses, therefore it was necessary to externally bring $\overline{DT}/\overline{OE}$ low during read accesses (see *Figure* below).

   In the DP8520A/21A/22A, the $\overline{DT}/\overline{OE}$ output will stay high during write accesses. During read accesses, this output will transition low after $\overline{CAS}$n goes low and will transition high when $\overline{CAS}$n goes high, causing the VRAM outputs to be enabled. If $\overline{CAS}$n toggles during a page mode read access, then the $\overline{DT}/\overline{OE}$ output will also toggle following $\overline{CAS}$n. *Figures 47* and *50* show the timing of $\overline{DT}/\overline{OE}$ in a VRAM read access when using the DP8520A/21A/22A.

   If the circuitry below is used, the DP8520A/21A/22A is completely compatible with the DP8520/21/22 in terms of how $\overline{DT}/\overline{OE}$ functions.



TL/F/9338–62

National Semiconductor

PRELIMINARY

DP8530 Clock Generator

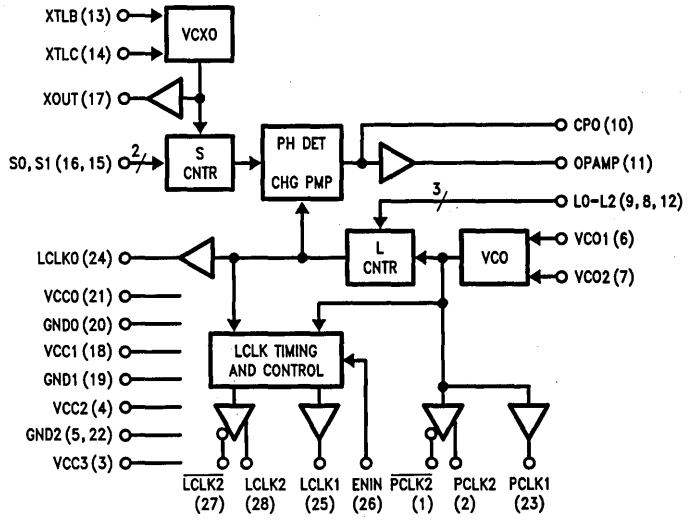
General Description

The DP8530 is a clock generator intended for use in medium-performance CRT graphics systems. The device generates both ECL and TTL pixel and load clocks from a single crystal resonator using digital phase locked loop (PLL) techniques. The L counter inputs allow the pixel clock to be divided by 4 to 32 in increments of 4 to drive the LCLK. The S counter inputs allow the system clock (XOUT) to run up to four times the LCLK. Both free-running and gated (by ENIN) LCLK outputs are available.

Features

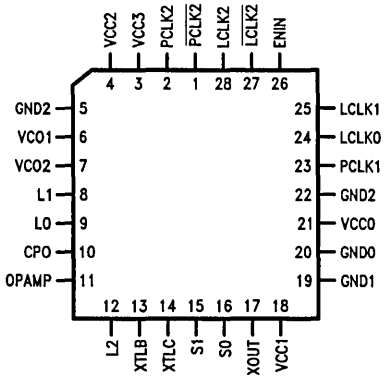
- On-chip crystal oscillator and phase-locked-loop generate TTL and ECL PCLK and LCLK outputs
- 125 MHz ECL differential output pixel clock (PCLK)
- Gated TTL and ECL load clock (LCLK) outputs
- Pixel clock to load clock divide ratios from 4 to 32 in increments of 4

Block Diagram Numbers in parentheses indicate pin numbers



TL/F/9328–1

Connection Diagram



TL/F/9328-2

Order Number DP8530
See NS Package Number V28A

Pin Descriptions

1, 2, 23—$\overline{\text{PCLK2}}$, PCLK2, PCLK1: Differential ECL and TTL compatible pixel clock outputs driven by the VCO (ECL outputs are 10k and 100k ECL compatible).

3—VCC3: ECL output buffer positive power supply.

4—VCC2: ECL internal logic positive power supply.

5, 22—GND2: ECL negative power supply.

6, 7—VCO1, VCO2: External tank circuit connections for the Pierce VCO.

8, 9, 12—L1, L0, L2: A three-bit word input used to select the L Counter modulus. Any modulus from 4 to 32 may be selected in increments of 4. L0 is the least significant bit.

10—CPO: Charge pump output. Used in conjunction with OPAMP to form the external loop filter.

11—OPAMP: Op amp output of the loop. This output is used to control the pixel clock frequency via the varactor diode in the LC tank circuit.

13, 14—XTLB, XTLC: External connections for the Pierce crystal oscillator.

15, 16—S1, S0: Two-bit word that determines the S Counter modulus. S0 is the least significant bit.

17—XOUT: MOS output generated from XTLB, XTLC.

18—VCC1: TTL output buffer supply. Specified for 5V ±10% operation.

19—GND1: TTL output buffer supply return.

20—GND0: TTL logic power supply return.

21—VCC0: TTL logic positive power supply. Specified for 5V ±10% operation.

24—LCLK0: TTL load clock output. Also is connected to an input of the phase comparator.

25—LCLK1: Gated load clock output.

26—ENIN: TTL compatible video enable input. A high on this input starts LCLK1 and LCLK2 on the next positive transition of LCLK0.

27, 28—$\overline{\text{LCLK2}}$, LCLK2: ECL compatible load clock.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature −65°C to +150°C

TTL Signals
- Inputs 7.0V
- Outputs 7.0V

ECL Signals
- Output Current −50 mA

ESD rating is to be determined.

Recommended Operating Conditions (Notes 1, 2, 3, 4, 5)

Symbol	Parameter		Min	Typ	Max	Units
VCC0, 1 to GND0, 1	TTL Power Supply		4.5		5.5	V
VCC2, 3 to GND2	ECL Power Supply	Mode 1	4.5		5.5	V
		Mode 2	4.2		5.7	
V_{IH}	High Level Input Voltage, TTL Inputs		2			V
V_{IL}	Low Level Input Voltage, TTL Inputs				0.8	V
I_{OH}	High Level Output Current, TTL Outputs				−0.4	mA
	High Level Output Current, MOS Outputs				−2	
I_{OL}	Low Level Output Current, TTL Outputs				8	mA
	Low Level Output Current, MOS Outputs				20	
F_{PCLK}	Pixel Clock Frequency	TTL			80	MHz
		ECL			125	
F_{XTL}	Crystal Frequency				20	MHz
T_{SU1}	Setup Time ENIN to LCLK0			20		ns
T_{H1}	Hold Time LCLK0 to ENIN		0			ns
$T_{AMBIENT}$	Operating Temp Range		0		70	°C

Note 1: See timing waveforms for relevant signal edges (positive or negative) from which all setup and hold time measurements are made.

Note 2: TTL inputs—ENIN, S0, S1.

Note 3: TTL outputs—XOUT, LCLK0, ENOUT1, 2.

Note 4: Inputs L0, L1, L2 designed to be tied to VCC2, 3 for high level or tied to GND2 (or left open) for low level. See input schematics.

Note 5: Mode 1: GND2 = 0V;
Mode 2: VCC2 = 0V.

DC Electrical Characteristics

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	VCC0, 1 = 4.5V, I_{IN} = −18 mA					−1.5	V
V_{OH}	Output High Voltage	VCC0, 1 = 4.5V	TTL Outputs	I_{OH} = −400 μA	VCC0, 1 − 2			V
			MOS Outputs	I_{OH} = −100 μA	VCC0, 1 − 0.3			
				I_{OH} = −2 mA	VCC0, 1 − 2			
		VCC2, 3 = 0V	ECL Outputs	I_{OH} = −24 mA	VCC2, 3 − 1045		VCC2, 3 − 880	mV
		GND2 = −4.2V	OPAMP Output	I_{OH} = −1 mA	VCC2, 3 − 1.2			V
V_{OL}	Output Low Voltage	VCC0, 1 = 4.5V	TTL Outputs	I_{OL} = 8 mA			0.5	V
			MOS Outputs	I_{OL} = 100 μA			0.3	
				I_{OL} = 20 mA			0.5	
		VCC2, 3 = 0V	ECL Outputs	I_{OL} = −5 mA	VCC2, 3 − 1810		VCC2, 3 − 1490	mV
		GND2 = − 4.2V	OPAMP Output	I_{OL} = 1 mA			GND2 + 0.4	V
I_I	Max High Level Input Current	VCC0, 1 = 5.5V	TTL Inputs	V_{IN} = 7V			100	μA

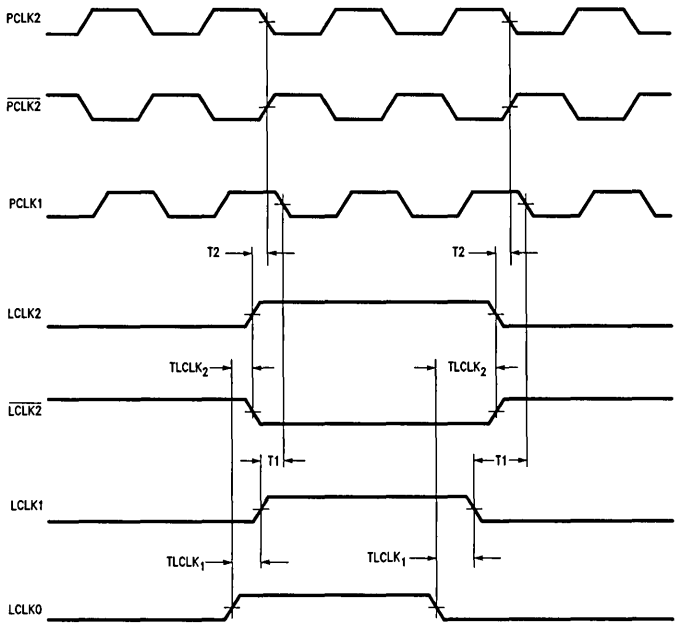
DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
I_{IH}	High Level Input Current	VCC0, 1 = 5.5V TTL Inputs		V_{IN} = 2.7V			20	μA
I_{IL}	Low Level Input Current	VCC0, 1 = 5.5V TTL Inputs		V_{IN} = 0.4V			−200	μA
I_O	Output Drive Current	VCC0, 1 = 5.5V TTL Outputs		V_{OUT} = 2.25V	−30		−110	mA
I_{CPO}	Charge Pump Current	VCC2 = 0V		Source	−0.2	−0.5	−1.0	mA
				Sink	0.2	0.5	1.0	mA
				TRI-STATE®	−10	0	10	μA
I_{CC}	Supply Current	VCC0, 1 = 5.5V, GND0, 1 = 0V				22	28	mA
		VCC2, 3 = 5.5V, GND2 = 0V				95	140	
		VCC2, 3 = 0V	GND2 = −5.7V	10k ECL range		95	140	
			GND2 = −4.8V	100k ECL Range		85	120	

AC Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
F_{MAX}	Max PCLK Freq		ECL	125			MHz
			TTL	80			
F_{MAX}	Max XTL Freq			20			MHz
T1	LCLK1 to PCLK1			4			ns
T2	LCLK2 to PCLK2			2			ns
T_{LCLK1}	LCLK0 to LCLK1			−5	0	5	
T_{LCLK2}	LCLK0 to LCLK2			−10	−5	0	

Timing Diagram

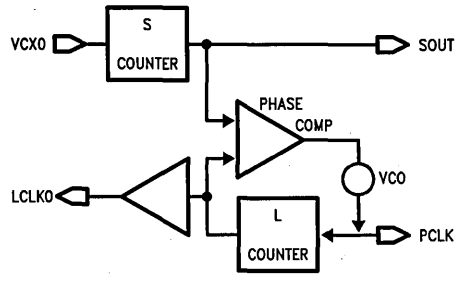


TL/F/9328–3

Circuit Operation

The heart of the DP8530 Video Clock Generator is a crystal oscillator which is used as a frequency reference to generate several clock signals required in a video display system. Among the clocks generated are the ECL load and pixel clocks (LCLK2 and PCLK2) for high speed video shift register parallel load and shift operations, and TTL load clocks (LCLK0 and LCLK1) for moving DRAM data to the video shift registers. The LCLK and PCLK outputs are all internally synchronized in order to simplify system timing.

The LCLK and PCLK outputs are generated using a digital phase locked loop as shown in *Figure 1*.



TL/F/9328–4

FIGURE 1. PLL Block Diagram

The loop consists of the S and L counters, a phase comparator, and a voltage controlled oscillator (VCO) with the relationship between these elements in the loop defined as:

$$PCLK = \frac{VCXO \times L}{S}$$

where PCLK is the pixel clock frequency, L is the L Counter modulus, and S is the S Counter modulus. When the frequency of the VCO (PCLK) in the phase locked loop is stable the inputs to the phase detector are in phase; thus the S Counter and L Counter outputs are identical in both phase and frequency. The crystal oscillator ensures that the phase and frequency of the S Counter output remain constant. Any drift, or change in frequency, of the VCO will be divided down and appear as a shift in phase at the L Counter output. The phase detector will sense this error and generate a correction voltage for the VCO input which is proportional to the magnitude of the frequency error. This correction voltage will change the VCO frequency to eliminate the error thus keeping the loop locked.

The presence of the S Counter in the loop enables the graphics processor to operate at full speed independent of PCLK frequency. The video shift register's parallel data width determines the L Counter modulus. An 8-bit parallel shift register would use an L Counter modulus of 8 so that a parallel load pulse occurs once every 8 pixel clocks. The L Counter output is used to derive the three LCLK outputs.

The ECL LCLK2 output is used in conjunction with the PCLK2 output to load data into a high-speed video shift register. The PCLK2 provides the clock and LCLK2 provides the load signal for the shift register.

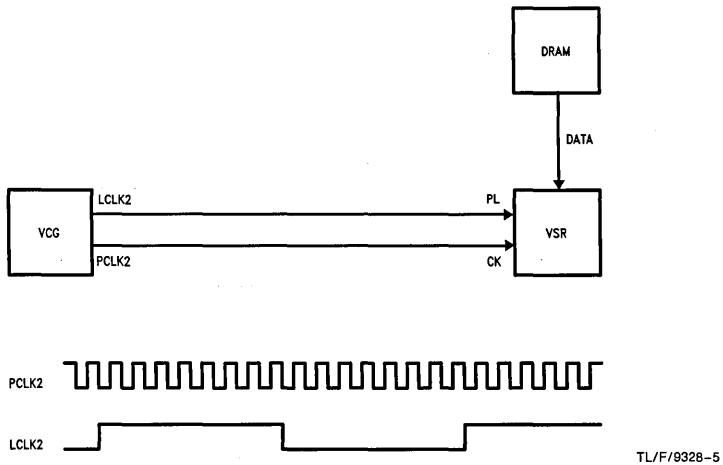
The other two LCLK outputs (LCLK0, LCLK1) are TTL outputs. They can be used to control a selection of different DRAMs/video shift register configurations as shown in the typical system architecture section which follows.

The S Counter can be programmed to divide by any integer up to 4 and the L Counter can be programmed for any word width from 4 bits to 32 bits in increments of 4. Table I shows some of the frequencies possible using various values for the S-modulus with an L-modulus of 8.

TABLE I. Partial Table of PCLK Frequencies

S MOD	8-Bit Word (L = 8) PCLK Frequency XTL = 10 MHz
1	80.0 MHz
2	40.0 MHz
3	26.7 MHz
4	20.0 MHz

Figure 2 demonstrates the configuration and the resultant waveforms with a DP8530 driving a video shift register and a DRAM.



TL/F/9328–5

FIGURE 2. System Configuration and LCLK Waveforms Using DRAM

Loop Filter Calculations

Several constraints need to be known in order to determine the loop filter components. They are the loop divide ratio (N), the phase detector gain (K_p), the VCO gain (K_O), the loop bandwidth (W_0), and the phase margin (ϕ).

The constant K_p is fixed at 80 μA/rad for the DP8530. N is the L counter modulus for the loop. A 60° phase margin is recommended, however the equations allow other values to be used if desired.

The oscillator gain constant K_O can be obtained from Table II or obtained experimentally. This is done by driving R2, the resistor which normally connects the varactor to the OPAMP OUTPUT, with an external power supply. Set the supply to GND2 + 3V and note the PCLK frequency. Next, set the supply to GND2 + 2V and note the frequency again. The difference in these two frequencies (times 2π to convert to radians) is K_O. For optimum performance the desired PCLK frequency should be somewhere between the two frequencies measured above. This may require adjustment of the coil.

Before choosing a value for W_0 one fact should be pointed out: R2 and C3 (the coupling capacitor between the coil and the varactor) form a low pass filter. Thus the loop bandwidth must be chosen to be less than the cutoff frequency of this filter. We recommend a value of 100 Hz to 3 KHz (times 2π) for W_0.

Having determined all these constants the following equations are used to find the component values:

- R1 = $(1.08\ N\ W_0)/(K_p\ K_O)$
- C1 = $(3.46\ K_p\ K_O)/(N\ W_0^2)$
- C2 = $(0.27\ K_p\ K_O)/(N\ W_0^2)$

To use a phase margin of other than 60° use the following:

- R1 = $(N\ W_0/2\ K_p\ K_O)$ (cosec 0 + 1)
- C1 = $(2\ K_p\ K_O/N\ W_0^2)$ (tan 0)
- C2 = $(K_p\ K_O/N\ W_0^2)$ (sec 0–tan 0)

For example: design a system with the following characteristics:

- 1560 pixels per line (2000 pixels including retrace)
- 8 bit wide video data
- 10 MHz processor rate

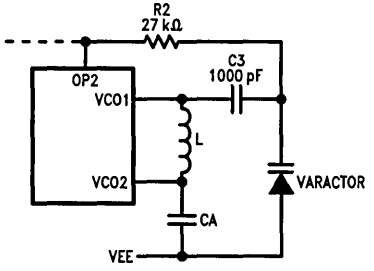
The PCLK frequency will be 10 MHz × 8 bits = 80 MHz. The components in Table II will be used. Note that K_O is 19 Mrad/Volt. Because it is an 8-bit wide system the L counter modulus must be 8. By choosing W_0 to be 2800 Hz (times 2π) the equations give:

- R1 = 100Ω
- C1 = 2.0 μF
- C2 = 0.17 μF (0.2 μF may be used)

TABLE II

Recommended VCO Components

$$F_{VCO} = \frac{1}{2\pi\sqrt{LC_{TOT}}}$$

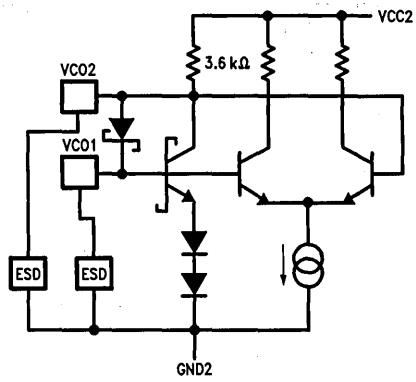


$$C_{TOT} = \frac{1}{\frac{1}{C_A} + \frac{1}{C_{VARACTOR}}}$$

TL/F/9328–8

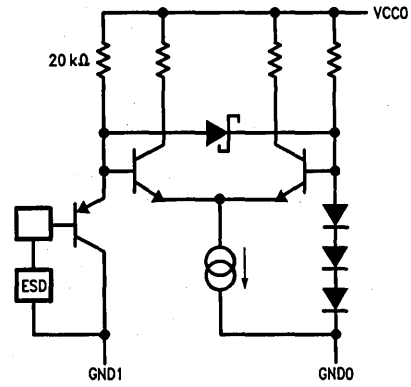
Frequency (MHz)	L μH	Toko Part #	CA pF	$C_{VARACTOR}$ pF	$C_{VARACTOR}$ Motorola #	K_O Mrad/volt
60	0.258	E502HNS-6000026	56	30	MV209	16
80	0.17	E502HNS-4000024	39	30	MV209	19
100	0.12	E502HNS-3000023	30	30	MV209	21
120	0.07	E502HNS-2000022	39	30	MV209	31

Input Schematics



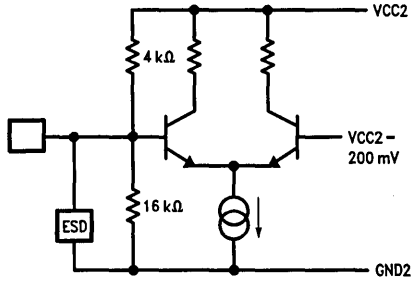
TL/F/9328–9

FIGURE 3. VCO Inputs



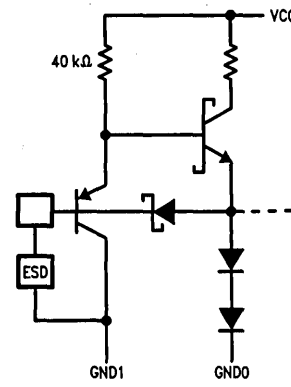
TL/F/9328–10

FIGURE 4. TTL Inputs



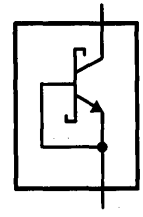
TL/F/9328–11

FIGURE 5. L Inputs



TL/F/9328–12

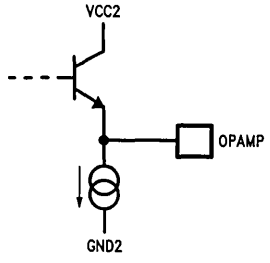
FIGURE 6. S Inputs



TL/F/9328–13

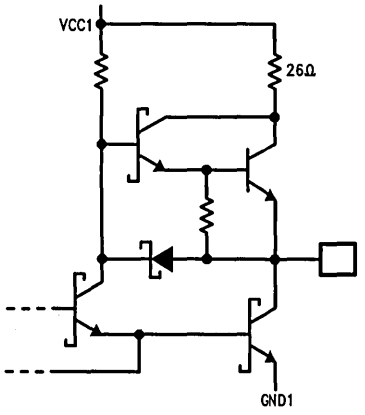
FIGURE 7. Typical ESD Circuit

Output Schematics



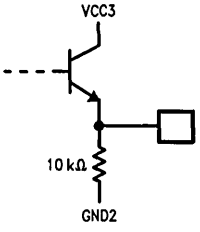
TL/F/9328–14

FIGURE 8. Op Amp Output



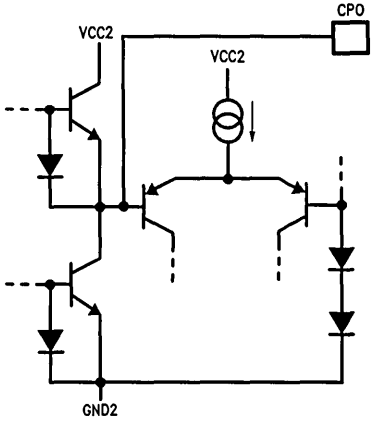
TL/F/9328–15

FIGURE 9. TTL Outputs



TL/F/9328–16

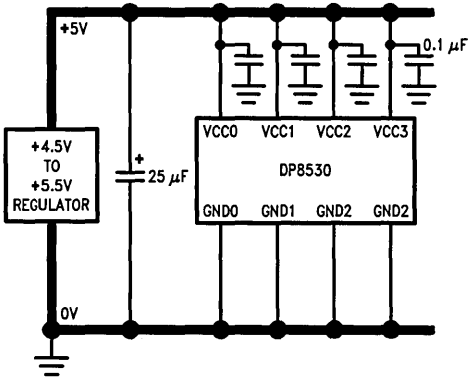
FIGURE 10. ECL Outputs



TL/F/9328–17

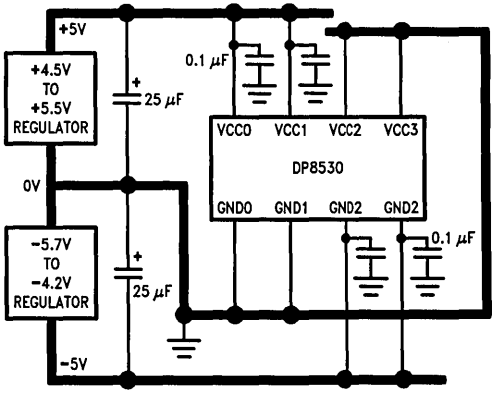
FIGURE 11. Charge Pump Output/Op Amp Input

Single Power Supply Operation



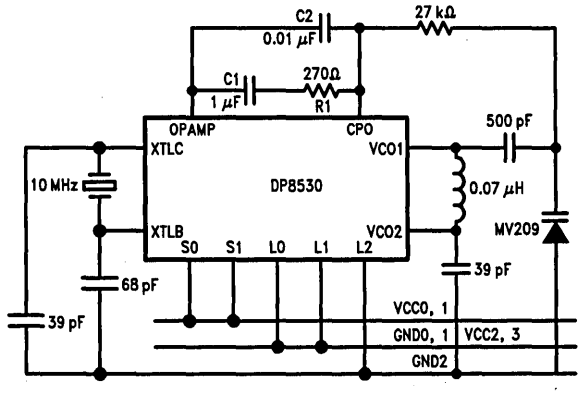
TL/F/9328–6

Dual Power Supply Operation



TL/F/9328–7

Typical Application



TL/F/9328–18

PCLK = 80 MHz
L = ÷16
Split Supply Mode

Section 2

Application Notes

Section 2 Contents

An Architectural Solution For High Performance Graphics

National Semiconductor
Application Note 451
Charles Carinalli

INTRODUCTION

Computer graphics is one of today's fastest growing market segments. The fundamental reason for this dramatic growth relates directly to the productivity improvement that a graphic representation can give to nearly all problems in the engineering, scientific, business, and consumer market segments. Nothing does more to ease the "man to computer" interface data interpretation and presentation problems than a graphics display and efficient application software.

Penetration of computer graphics into all market segments has grown especially fast in the past few years since it has become more affordable. This is due to the decreasing costs of high quality CRT displays and significant reductions in the cost of Dynamic RAM. In the near future, high performance graphics support hardware will be more available in the form of a number of VLSI integrated circuits, further decreasing the costs of graphics hardware.

Now that more people have a good understanding of the importance of computer graphics to the productivity of their job, the demand for higher resolution, faster graphics will increase significantly. This will be especially true in the engineering, scientific, and business communities. The current challenge for this generation of graphics hardware is clearly in the area of affordable, high resolution, fast computer graphics. Attaining these goals will not only do much to expand the useage of computer graphics but also expand application areas.

GRAPHICS ARCHITECTURE

It is not the purpose of this paper to discuss the varied aspects of software and hardware computer graphics architectures. What will be addressed are the problems of hardware architectures in the area of list driven display generation, manipulation, and screen refresh. Current monochrome graphics hardware architectures generally do not satisfy the current demands of high performance computer graphics which include display resolutions of 1000 pixels by 1000 pixels and above, very high speed screen manipulations, and color.

To reinforce the growth of computer graphics, hardware architectures must be developed which will support the rapid growth in display resolution which will occur in the next few years. The architectures must allow a high degree of application independence yet not require significant changes in the overhead software interface. The hardware architecture must be expandable, again avoiding significant software changes. Finally, the architecture must be implemented in VLSI for reasons of cost and speed.

This paper will describe a graphics hardware architecture that meets these criteria.

KEY PERFORMANCE ISSUES

Figure 1 is a block representation of the logical hardware and software partitioning associated with a typical graphics system. The left block represents the application interface and image creation segments. Data must be translated from the database found on disk (or received via communications networks) to a format which will be meaningful in the CRT display. At the application level this may involve database interpretation and translation to and from graphics standards such as GKS and CORE. But it also involves the final translation from what is described as the "world space" representation to the "normalized" coordinate space associated with the hardware of the particular graphics system in use. This is done with the Main CPU in software or through hardware acceleration via usage of a number of VLSI integrated circuits on the market.

Once this translation is completed the transfer to the actual "display" coordinates is usually accomplished through an instruction list given to a graphics processor linked directly to the CRT frame buffer. It is the function of this graphics processor to offload the main CPU in the creation and manipulation of the massive amounts of data in the actual bit map in the frame buffer. Without this block, any large bit map manipulation would cripple the main CPU in its main application chores.

The final blocks represent the portion of the graphics system which handles the lower level image movements and manipulations as well as the screen refresh function. High speed hardware implementations of these blocks with an architecture that links closely with the graphics processor is the only way performance can be maintained as display resolution increases along with the increasing number of memory planes for color.

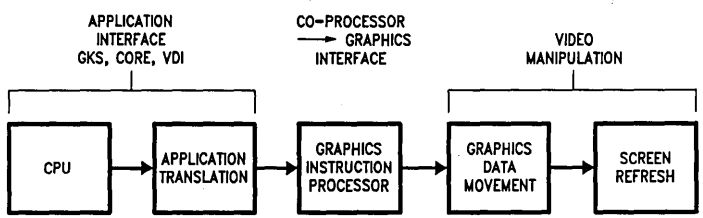


FIGURE 1

We will focus on the performance issues of the last two major blocks of *Figure 1* and factors that will influence.

- List Driven Display Generation
- Graphic Data Manipulation and Movement
- Screen Refresh

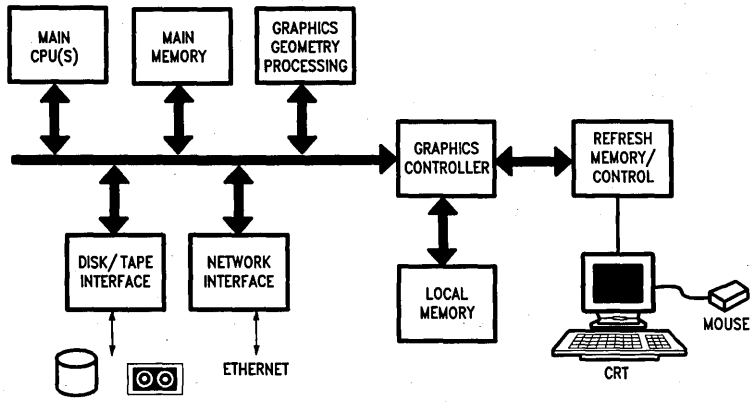
The technical problems of providing cost effective architectural solutions with present hardware (given the current and future performance requirements) make these functions ideal candidates for VLSI integrated circuits.

THE GRAPHICS FRAME BUFFER— SCREEN REFRESH ARCHITECTURE

To focus on these performance issues requires a good understanding of the tradeoffs associated with the graphics frame buffer. *Figure 2* is a simplified diagram of a typical graphics workstation. The graphics controller is shown closely linked to the memory associated with the CRT screen display (called the CRT refresh memory or the frame buffer) and the main CPU with its associated graphics geometry processing hardware and software. This figure shows the popular configuration in which a special processor is allocated to handle graphics functionality thus off loading the main CPU with respect to fundamental graphics operations. Those operations are list driven based on a lower level graphics software language. We will talk later about advantages of this and some specific implementations.

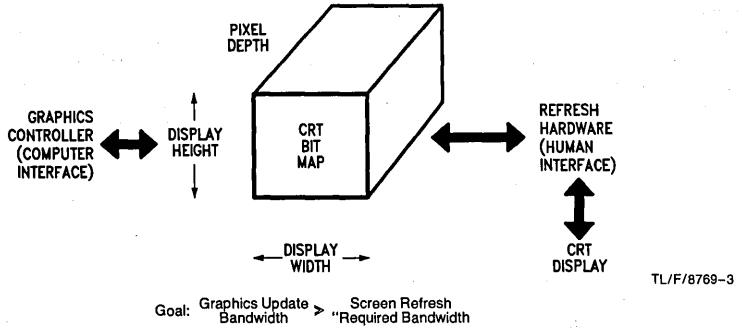
The image that is stored in the frame buffer is actually stored conceptually in three dimensions as shown by the cube represented in *Figure 3*. Each pixel on the screen can be mapped to multiple pixels (in the case of color) contained within this cube. Access to the data stored in this cube is necessary for both screen refresh, update, and data manipulation. Ideally, the amount of time available for manipulation should greatly exceed the time required for screen refresh, thus enabling very quick display update and image movement.

The fundamental graphics tradeoffs involve the need to maximize CPU or graphics controller access to the frame buffer while maintaining regular (required) CRT refresh. As display resolution increases and color becomes more important these issues become significant factors in the design and cost of the graphics sub-system.



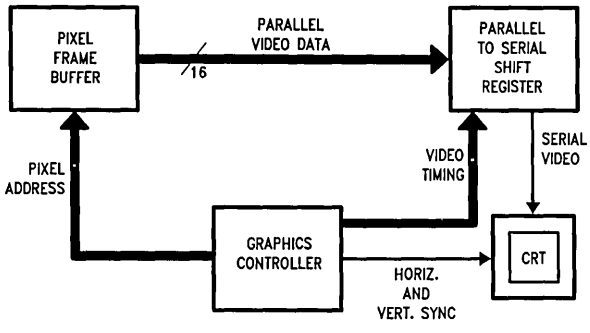
TL/F/8769–2

FIGURE 2. Typical Graphics Workstation



TL/F/8769–3

FIGURE 3. Graphics Frame Buffer



TL/F/8769–4

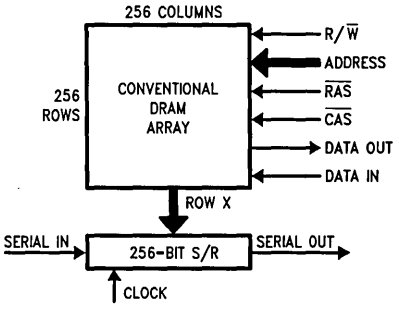
FIGURE 4. The Graphics Video Loop

Current video rates for medium resolution graphics systems easily exceed 50 MHz. High resolution systems attain video rates on the order of 100 to 125 MHz with clear trends to rates in excess of 125 MHz in the near future. Given these clock rates, screen refresh has become a significant problem in the design of the graphics sub-system.

The high video rates have forced a graphics memory organization for refresh as shown in *Figure 4*. Since the size of the frame buffer is large, the desired memory component because of cost and space is the DRAM. However, the DRAM does not have access speeds suitable for current high resolution displays. As a result, the screen refresh process is implemented through a parallel to serial conversion in the "video loop". To refresh the screen, the graphics controller presents a word address to the frame buffer, the resulting data word (usually 16 pixels) is then converted into a serial video stream via an external (usually TTL to ECL) shift register under the timing and control of the graphics refresh hardware. *Figure 4* shows the implementation for a single plane system, multiple plane systems would require the same number of 16 Bit refresh pixel words and parallel to serial video shift registers as the number of planes.

If the video rate is 100 MHz, this parallel to serial buffering reduces the need for a parallel word from the frame buffer to a clock rate of 6.25 MHz if the word is 16 bits wide. This is still an access time of 160 ns. Given this, it is clear that with conventional time multiplexed DRAM design, the only time left for data manipulation and screen update will be during horizontal and vertical blanking when screen refresh is disabled. With the demands of current graphics end applications, this is clearly not enough!

A number of frame buffer architectures have been developed to get around this problem. These include double frame buffering, dual porting, and making maximum use of page mode access. The most popular solution to this problem is the one provided via a new type of DRAM called the Video DRAM shown in *Figure 5*. The video DRAM is a conventional DRAM with a 256 bit shift register on board. This shift register is connected such that a complete row of memory cells can be loaded into the shift register at one time. The shift register has its own output which can be controlled with separate input lines to the video DRAM. If you configure the Video DRAM as shown in *Figure 6*, you can see we have implemented a dual ported memory. The left side is configured as a typical DRAM interface. The right side is configured for screen refresh with the parallel word being generated from the shift registers of the Video DRAM (this parallel configuration is still needed since the Video DRAM shift registers are not able to clock at the full video rate in high performance systems).

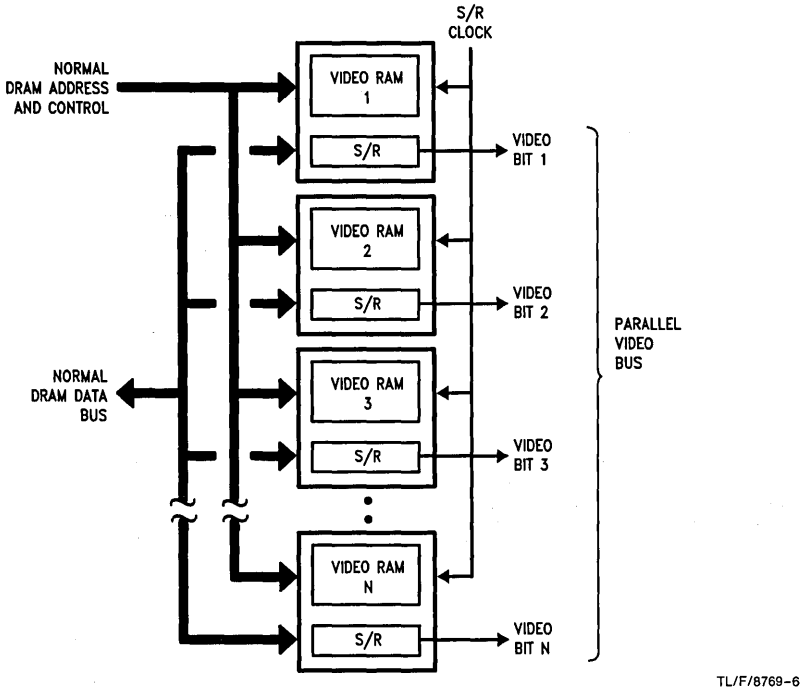


TL/F/8769–5

FIGURE 5. The Video DRAM

The advantage that this configuration provides is nearly full time access for screen update and manipulation since only one load to the shift register is generally needed per scan line. While the pre-loaded video data is clocked out of the shift register, random access can occur in the frame buffer by either the graphics controller or the main CPU.

Many configurations of the Video DRAM are becoming available with multiple vendors committing to the architecture already in place. It will clearly become the standard component for building graphics frame buffers. Any new graphics hardware architecture must be designed to optimize the use of this type of memory component.



TL/F/8769-6

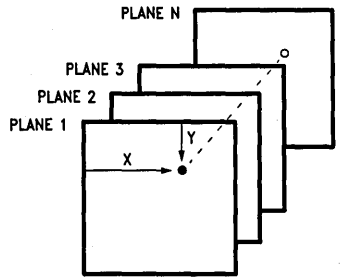
FIGURE 6. Multiple Video DRAMs

THE GRAPHICS FRAME BUFFER— UPDATE/MANIPULATION ARCHITECTURE

We have discussed the preferred frame buffer architecture with respect to screen refresh. Now we will evaluate the tradeoffs associated with the update and manipulation side. The performance issues associated with the graphics processor or main CPU update or manipulation of the image in the frame buffer have a major influence on the data and address configuration of the frame buffer. There are generally three such configurations—pixel, plane, and mixed.

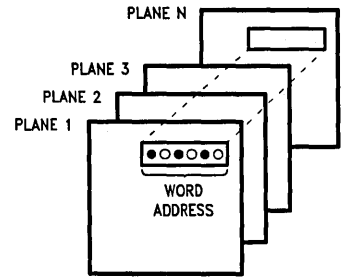
The pixel architecture is shown in *Figure 7*. This architecture is best described as one in which the frame buffer data is manipulated one pixel at a time. For multiple planes, the address to the frame buffer generates a data word which is composed of pixels at the same location across multiple planes—thus the term "pixel depth". This is the architecture often found in image processing and solids modeling applications where the value of each pixel is very computation intensive due to color value or shading variations. These applications typically require 16 to 32 memory planes.

In the plane architecture, *Figure 8*, the frame buffer data is manipulated one word (usually 16 bits) at a time within each plane. To change one bit, 15 other bits must be carried along. Also, since the word boundary of the 16 bits exists, a barrel shifter is needed if image placement and movement accuracy is needed down to the actual pixel level. Despite these disadvantages, in the engineering and business application area, the plane architecture is the most popular since these applications are less pixel computational intensive but more data creation and image movement intensive. This architecture is lower cost and brings with it higher performance when large bit maps must be manipulated.



TL/F/8769-7

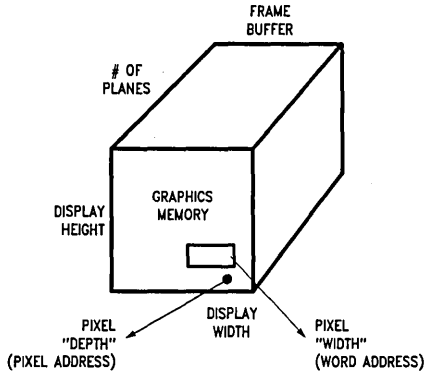
FIGURE 7. Pixel Architecture



TL/F/8769-8

FIGURE 8. Plane Architecture

Where the application has need for both types of architectures, the mixed architecture shown in *Figure 9* is implemented. Here, access to the frame buffer can be either at word width or pixel depth, thus providing the best of both worlds. In the past, this architecture has been implemented only in the more expensive of workstations due to the overhead hardware costs. But, the applications of workstations that need high speed update along with computation intensive displays is increasing. The time has come for a graphics hardware architecture that can efficiently merge these two architectures.



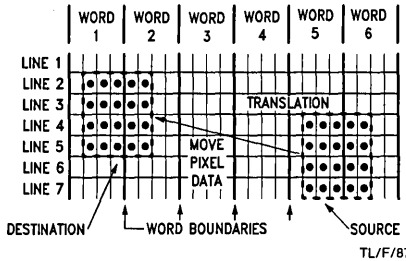
TL/F/8769–9

FIGURE 9. Plane and Pixel Architecture

WORD BOUNDARIES AND THE BARREL SHIFTER

In the engineering and business community, the most popular frame buffer architecture is the plane architecture. But as the quality of these displays increase, restrictions associated with the plane architecture word boundary constraints have limited the flexibility and performance of these systems. To solve these problems, some of the designs have switched to the pixel architecture. With the "correct" architectural solution this switch would have not been necessary.

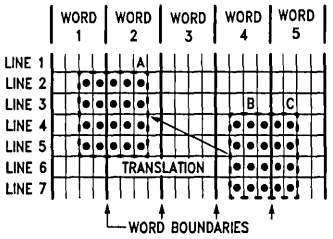
Figure 10 demonstrates the word boundary problem via a 4 bit word example. This figure demonstrates a "word boundary aligned" translation. The relative pixel locations of the 4 bit word are the same at the destination image as they are in the source image. Thus the pixels maintain the same alignment to the word boundary. This is a simple transfer where manipulation of the pixel positions in the source word need not be modified to transfer it to the destination.



TL/F/8769–10

FIGURE 10. Plane Oriented Translation (Word Boundary Aligned)

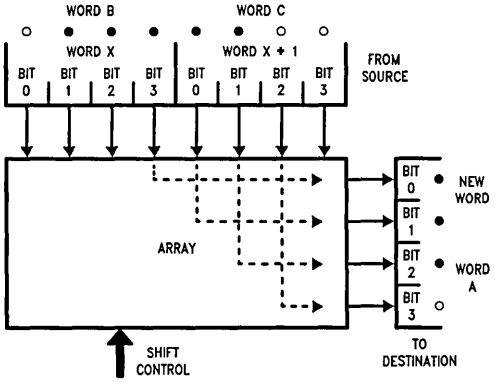
In *Figure 11*, the source word pixel alignment does not agree with the desired pixel destination alignment. In this transfer, the source pixel map is shifted one pixel to the right in the transfer. This type of control is not available if the frame buffer is addressed by words. If the frame buffer is addressed by pixel, then the price paid for overhead access to do this simple manipulation is significant. A better solution to this problem is to employ an additional hardware function called a barrel shifter and maintain word boundary addressing.



TL/F/8769–11

FIGURE 11. Plane Oriented Translation (Non-Word Boundary Aligned)

A simplified diagram of a barrel shifter is shown in *Figure 12*. In order to maintain consistency across word boundaries on a shift like the example in *Figure 11*, two source words must be read to create a new shifted destination word. The barrel shifter solves the fundamental restrictions of the plane architecture with respect to exact pixel manipulations. But, if these manipulations occur within the main CPU or for that matter in the main graphics processor a new performance bottle neck may result in multiple plane color systems. The ultimate performance of such a system is associated with the speed of the barrel shifter and its location. Ideally, for maximum performance, you would want a barrel shifter for each plane.



TL/F/8769–12

FIGURE 12. The Barrel Shifter

BITBLT

Due to the growth of display resolution and the resulting demand for movement of massive amounts of data, the need for a lower level graphics operator that well describes these data movements and manipulations has increased. The most popular operator or function is BITBLT (for **BIT** Boundary **BL**ock **T**ransfer) originally developed at Xerox PARC (Palo Alto Research Center). This function is also called Raster Op (short for Raster Operator).

Fundamentally, BITBLT is a logical operator which simply describes the manipulation of rectangular bit maps of any size. For this reason it should be viewed as a lower level language for graphics bit maps. *Figure 13* is a conceptual drawing of how BITBLT works.

The block on the right is a source bit map area which can be outside or within the view area of the frame buffer. On the left is the destination area generally, though not necessarily, within the view area of the frame buffer. If the graphics hardware is implemented with BITBLT in mind, a single simple setup from the main CPU (via an instruction list) can cause the graphics controller to move massive amounts of data. The only information needed is the absolute pixel address of the source and its width and height in pixels, the destination pixel address, and the clipping rectangle pixel address with its associated pixel width and height.

Resulting from this single setup, any size bit map can be moved without intervention from the main CPU. Additionally, if a barrel shifter is integrated within this operation, the BITBLT is not bounded by word boundary constraints. Finally, if multiple BITBLT processors and barrel shifters are used, for example one set per plane, transfers within all planes can be done in parallel.

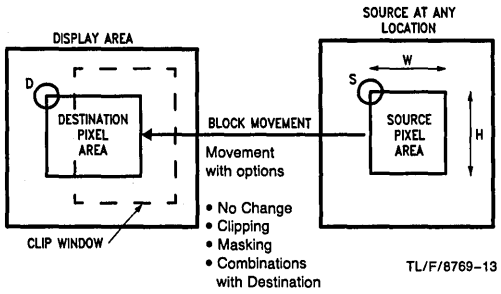


FIGURE 13

If interaction is desired from the source image with the destination area, logical operations may be implemented within the BITBLT operation, such as AND, OR, and XOR. To do this, the source data is first read and barrel shifted to align with the destination word. The destination word is then read and the desired operation performed, creating a new destination word. This word is then transferred to the destination. This is described by the following equation—

SOURCE OP DESTINATION → DESTINATION

Where OP can be a logical operator such as AND, OR, XOR, etc.

BITBLT is particularly well suited for applications where there is a high mixture of graphics, text, and windowing. Pop-up menu's, icons, accelerated filling, fat line drawing, and high speed text transfer are all functions where BITBLT provides accelerated solutions.

Clearly, for any architecture to be a good match to high resolution displays and fast screen update, the main CPU should not be involved in the simplest of image movement chores. The main advantage of BITBLT functionality comes in off loading the main CPU with the detail of the bit map operations and at the same time adding a powerful functional operator.

PREVIOUS SOLUTIONS

Historically, graphics VLSI controllers have not well addressed the high resolution color applications of modern bit mapped graphics terminals. As a consequence, much of the graphics hardware was implemented with bipolar bit slice processors and random logic, much of which was Schottky TTL or ECL. The result was a costly high power solution, difficult to map into future high resolution multiple plane applications.

A new generation of graphics VLSI integrated circuits will be introduced during the next year, from a variety of semiconductor vendors. Many of these I.C.'s have been developed to address the performance problems associated with high performance bit mapped displays. In nearly all cases, to make these controllers effective, a graphics hardware architecture had to be selected. In most cases this has restricted the performance and applicability of these devices across the spectrum of graphics applications.

Typically, most of these architectures suffer from inflexibility in the processor to memory plane interface. *Figure 14* is an example of this problem. Some of these architectures are designed to directly support 1, 4, or 8 planes of memory. Transition to more planes requires additional processors. The result is an associated cost increase in hardware usually coupled with a degradation of performance due to synchronization problems between processors.

Although performance may be good within the fundamental bounds of a single processor, the rules significantly change when the transition is made to multiple processors. Nearly without exception, this new generation of VLSI components has the main controller or processor intimately involved with both frame buffer addressing and data manipulation. This is where the main limitation exists; when memory plane expansion occurs, the graphics processor again becomes the bottle neck to graphics system performance. It matters little whether this is a BITBLT based architecture with internal

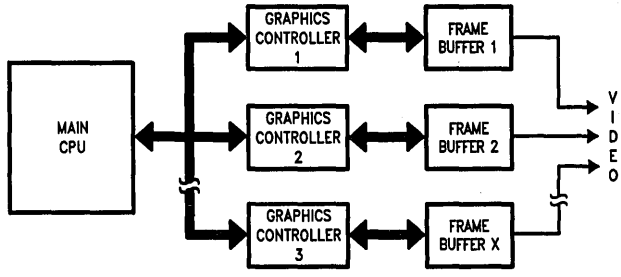


FIGURE 14. Current Graphics Chips Color Application

barrel shifters, the common data and address graphics function is the limitation to expansion and performance.

Many of these new chips begin to address the notion of parallelism. Operations can occur in different memory planes at the same time. However, due to pin and architecture limitations, expansion to more planes than supported by a single processor significantly degrades performance.

OPTIMUM ARCHITECTURE

The only practical way to solve these problems and still adequately address all the performance issues we have discussed here is to implement an architecture as shown in *Figure 15*.

In this diagram a single graphics processor assumes the responsibility of address and timing associated with the graphics frame buffer while maintaining the classical address and data interface with the main CPU and processing functionality with its local program storage memory.

With such a processor, based on a BITBLT architecture, frame buffer address operations are its responsibility while actual data manipulation is the responsibility of the slave BITBLT data manipulation functions.

The Slave Controller (data manipulator) is a data handling chip which receives all control from the single main graphics processor. It is responsible for masking, barrel shifting, and BITBLT operations associated with its own memory plane.

A separate control bus from the graphics processor passes all control and setup information to the slave manipulators in parallel with other control information via the data bus. Once this initial information is set-up, the main graphics processor is no longer involved in graphics data manipulation while the graphics function is implemented. The slave manipulators can be configured via the control and data bus for the exact destination left and right masking, BITBLT operation, and amount of barrel shift.

Additionally, operations can occur in parallel with all slave manipulators working within their own plane. When plane to plane transfers are required, one slave manipulator acts as the source and any number or combination of slave manipulators act as the destination. Here again, any BITBLT operation, either within a plane or plane to plane is fully set-up via a single graphics processor independent of the number of planes used.

Most importantly, performance is independent of the number of planes. Operations for 32 planes of BITBLT take the same short time as if only one plane were used since the architecture is the same. Plane to plane transfers have the same speed whether you are transferring the image to one plane or 16 planes!

In summary, in this architecture, the main graphics processor is concerned with graphics setup and addressing to the frame buffer during the graphics operation. With a BITBLT architecture, large data movements, character/text transfer, and line drawing and filling all exhibit high performance. Since the processor function occurs only once in the system, the higher cost associated with such processors is a constant and independent of the number of planes.

The more cost effective Slave manipulators are concerned with the actual data manipulation via control from the main graphics processor. They are local to each memory plane frame buffer and fully synchronized by the main processor for operations within the plane or for plane to plane transfers.

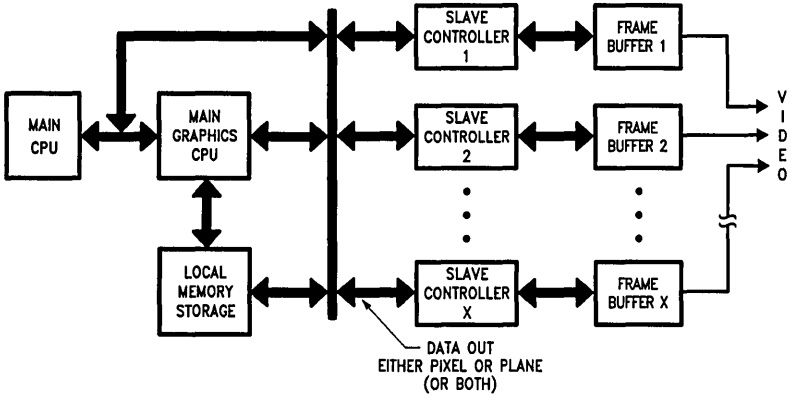
This architecture provides one consistent hardware interface independent of the number of memory planes utilized. The hardware interface is the same for one plane or 32. This lends itself to a level of software consistency not found in any other graphics architecture.

Finally, the level of parallelism in this architecture creates a consistent growth path for performance. As the number of frame buffer memory planes is increased, the performance does not degrade but remains equal to a single plane architecture. In fact, with proper implementation in VLSI components, the true speed limitation of such an architecture is limited only by the speed of the DRAM used for the frame buffer.

VLSI IMPLEMENTATION

National Semiconductor Corporation is developing a graphics chip set to match this graphics architecture. The first four chips in this chip set will be introduced during 1986 and are shown in *Figure 16* for an example of 3 memory planes. The chip set is fully expandable to any number of memory planes.

The RGP (Raster Graphics Processor) is the main graphics processor, the BPU (BITBLT Processing Unit) the slave data manipulator. The VCG (Video Clock Generator) is a timing and control generator for the graphics system with

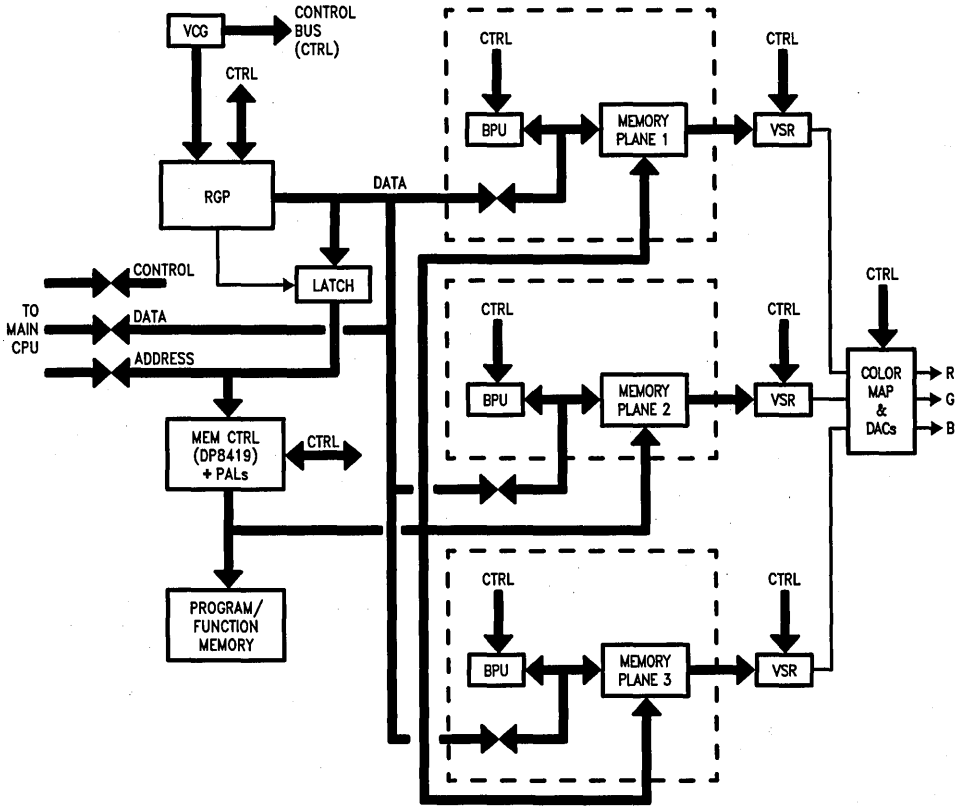


TL/F/8769–15

FIGURE 15. Optimum Solution BITBLT Based

capability of generating clocks in excess of 150 MHz. The VSR (Video Shift Register) acts as a parallel to serial converter capable of clock rates in excess of 150 MHz. The chip set has been designed to support all types of RAM components that may be used in the frame buffer, including Video DRAM.

The National Semiconductor architecture is very well suited for plane oriented architectures, but can work equally well in pixel oriented architectures. Additionally, it is the first chip set which will provide a complete solution for mixed mode applications.



TL/F/8769–16

FIGURE 16

Interfacing the DP8500 Raster Graphics Processor

National Semiconductor
Application Note 547
Rob Wilson

1.0 INTRODUCTION

A graphics subsystem using National Semiconductor's Advanced Graphics Chip Set (AGCS) requires some interface circuitry between the DP8500 Raster Graphics Processor (RGP) and other devices on the bus. Specifically these devices may include:

- the Frame Buffers (memory) in each plane,
- the Bitblt Processing Unit (BPU) in each plane,
- a data transceiver in each plane,
- other types of memory used in the system, such as EPROM for basic functions and startup,
- memory-mapped I/O devices, including latches for control of color.

In general the interface circuitry required between the RGP and other devices will consist of two main blocks:

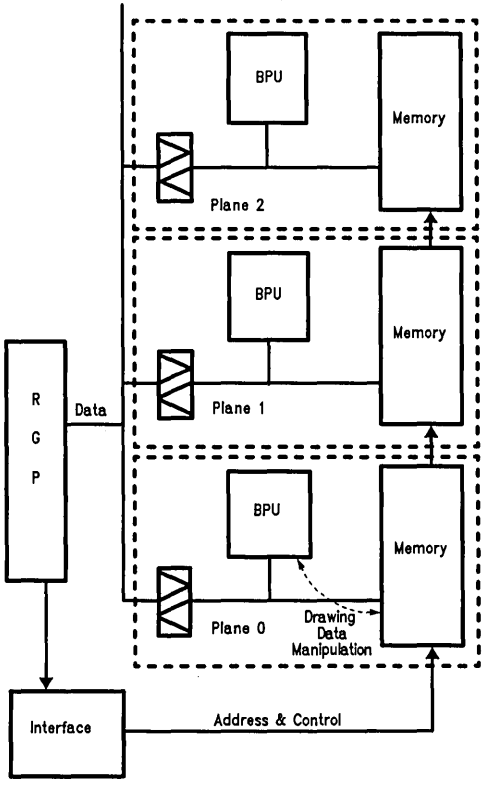
- the Bus State Machine (BSM), which generates memory strobes as required by the particular type of memory being accessed, and transceiver control signals, and
- the Video Plane Controller (VPC), which enables only selected planes of memory, and ensures correct data flow between memory planes.

Additionally an Address Decoder block produces various enable signals according to the address being generated by the RGP.

The RGP's bus interface has been deliberately kept general-purpose to allow flexibility of memory types; this means that the system designer must tailor the interface to suit his requirements. The purpose of this application note is to describe some of the issues and to suggest some solutions.

Memory Architecture and Graphics Operations

The AGCS has an open architecture which permits both planar and pixel operations. The memory is organized in planes (see *Figure 1*), in which the "color value" of a particular pixel is the parallel combination of the corresponding bits in separate words of memory. This requires that the graphics controller be able to access each plane separately; but by dividing the graphics rendering functions between the RGP (address generation) and a BPU on each plane (data manipulation), the AGCS allows parallel graphics processing. Thus the time required to render a particular graphics object is independent of the number of bits per pixel and the



TL/F/9762–1

FIGURE 1

data processing bandwidth is matched to the memory bandwidth with uniform expandability.

Contrast this with the more common, but less powerful, packed-pixel architecture. This requires only a single graphics controller, with access to just one block of memory. Within the memory each word holds the "color value" of a number of pixels (for a 4 plane system, i.e., 4 bits per pixel, a 16-bit memory word would hold the color values of 4 pixels). With this architecture therefore, the time required to render a graphics object does depend on the number of bits per pixel—the system gets slower as the number of bits per pixel increases. Thus the performance is limited by the data processing bandwidth.

In addition to being able to perform planar operations (such as Character Drawing and Bitblt) at high speed, the AGCS can also execute pixel operations (such as Read and Draw Point) efficiently. This is achieved by means of the Pixel Port in each BPU, which allows the RGP, or some other processor, to access data representing a single pixel.

It is important to understand that the RGP is a processor—it fetches instructions from memory and executes them. Specific graphics instructions are "hardwired" rather than microcoded, thus providing the highest performance for rendering operations. During these operations the RGP does not process the data in each plane—this function is handled by the BPU. Thus the RGP does not need to have any "knowledge" of the number of planes attached to it.

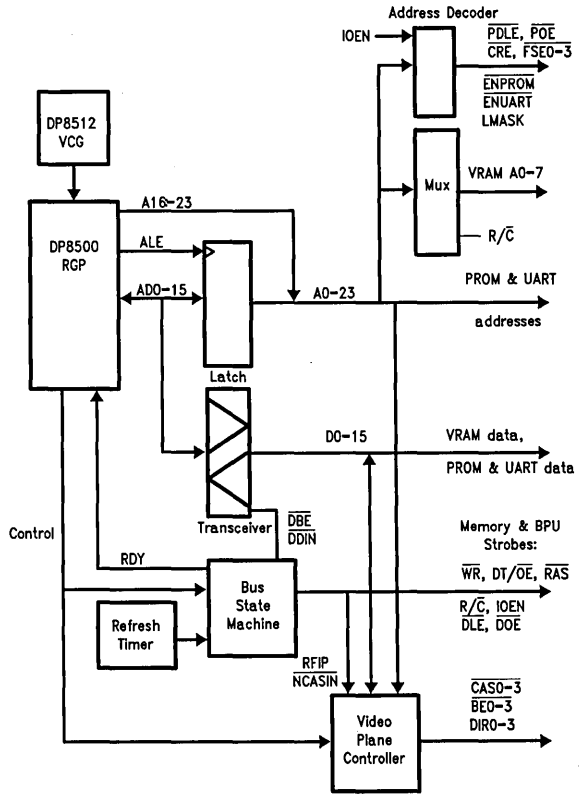
This leads to the concept of addressing duality: during instruction fetches and operand reads and writes, the RGP is accessing just one word in memory, and data passes to or from the RGP—the "linear" type of access. During "drawing" operations, however, the RGP is providing only address and control information to memory. Drawing operations include Line Drawing, Bitblt, and higher level operations which use these, such as Text rendering, and also Screen Refresh.

Thus the system designer needs to build an interface which can recognize these two types of access, and act on memory accordingly. Furthermore, for drawing operations there must exist some mechanism in the interface circuitry to allow the RGP's programmer to select just one or more planes which will take part in the operation. This allows attributes such as color and intensity of the graphics objects to be controlled.

Figure 2 shows the block diagram of the interface logic.

The Pixel Port

The BPU has a multiplexer on-chip, which, in point-wise drawing mode (Line Drawing) where one pixel is modified at a time, selects one of the 16 bits of the destination word and latches it into a single-bit bidirectional port. Conversely a single bit can be latched into this port prior to drawing: the bit is replicated 16 times and presented to the BPU's Logic Unit along with the Destination word. Thus the selected bit of the Destination word can be modified by the latched bit in conjunction with the programmed logic function.



TL/F/9762-2

FIGURE 2

This mechanism is used in the RGP's Read Point and Draw Point instructions, which allow the RGP to read or write the "color value" of a single pixel. In addition to uses in color arithmetic this mechanism is useful in allowing pixel architecture data bases to be easily and rapidly translated to the AGCS's planar architecture.

Local and Interplane Bitblt

For Bitblt and derivative operations it is common for the Source and Destination rectangles to lie in the same plane (Local Bitblt). But it may be a requirement to have a source rectangle in one plane with the Destination lying in multiple planes (Interplane Bitblt). This would commonly be used for text rendering where the font bitmap is stored only once in one plane—perhaps in low-cost DRAM rather than Video DRAM, but will be required to be rendered in different colors by transfer to various Destination planes.

2.0 EXAMPLE SYSTEM

To illustrate the design of an RGP interface a typical small system will be used. The actual example is National's DP850EB, an evaluation board for the RGP. This is a stand-alone 4-plane system with 1M pixels per plane, which has basic system firmware in PROM, and a UART for communications with a Host computer. The main components of the system are:

- One DP8500 RGP
- Four planes, each containing one DP8511 BPU, four 64k x 4 Video DRAMs (VRAMs), a transceiver, and a shift register for parallel to serial conversion
- One NS16450 UART
- Two 2k x 8 87SR193 PROMs for resident firmware.

Memory Map

The RGP will start to execute instructions from address 0 after reset, thus the PROM space must begin at 0. The four planes are allocated separate, but congruent, memory spaces. This simplifies the system design (but systems which need very large amounts of memory for each plane might need to map each plane to the same space). These considerations, together with the desire for simple memory space decoding, result in the following memory map:

BPU Registers

The BPU Control registers must be memory mapped so that, when the RGP automatically loads them (in one access) prior to drawing, the interface logic can generate the required BPU control signal ($\overline{CRE}$). The BPU Base Address (800001 hex) needs to be loaded into the RGP upon Initialization.

Similarly the BPU Function Select registers need to be memory mapped so that the user can load them individually. During the RGP's linear access to each register the interface logic needs to generate the required BPU control signal ($\overline{FSE}$).

Other I/O Devices

The Bus State Machine and Address Decoder produce an Enable signal ($\overline{ENUART}$), which, together with Read ($\overline{R}$) and Write ($\overline{WR}$) strobes, permit RGP access to the UART registers.

Memory

The system uses VRAM in page mode for drawing accesses only. There is negligible increase in performance for page mode during other VRAM accesses. The RGP's Page Break ($\overline{PB}$) output is useful in controlling page mode accesses. When High at the beginning of an access ($\overline{PB}$ becomes valid during the second half of the RGP's T1 cycle) $\overline{PB}$ indicates that the current access is within the same 256-word page as the previous access. A Low on $\overline{PB}$ indicates that the access is to a new "page", or row, of memory.

3.0 BASIC TIMING

The example system uses Video DRAM with the following parameters:

RAS Access Time:	120 ns Max
RAS Pulse Width	120 ns Min
RAS Precharge Time:	90 ns Min
CAS Access Time:	60 ns Max
CAS Pulse Width:	60 ns Min
CAS Precharge Time:	50 ns Min (Page Mode)

Space (Hex)	Address Range in Space	Total Words	Comments
PROM	000000–3FFFFF	4M	Resident Firmware
PLANE 0	400000–40FFFF	64k	Bit-Maps for Each of
PLANE 1	410000–41FFFF	64k	the Four Planes
PLANE 2	420000–42FFFF	64k	
PLANE 3	430000–43FFFF	64k	
BPU $\overline{CRE}$	800001	1	For BPU Control Reg
BPU $\overline{PDLE}$	800002	1	For BPU Pixel Port Load
BPU $\overline{POE}$	800004	1	For BPU Pixel Port Output
BPU0 $\overline{FSE}$	A00001	1	For BPU0 Function Reg
BPU1 $\overline{FSE}$	A00002	1	For BPU1 Function Reg
BPU2 $\overline{FSE}$	A00004	1	For BPU2 Function Reg
BPU3 $\overline{FSE}$	A00008	1	For BPU3 Function Reg
(The RGP can access all BPU FSEs simultaneously at address A0000F)			
UART	C00000–DFFFFF	2M	
VPC	E00000–FFFFFF	2M	For Video Plane Control

At an RGP clock frequency of 20 MHz these parameters can be met by using the following:

RAS Low for 3 Clock Periods

RAS High for 2 Clock Periods

CAS Low for 2 Clock Periods

CAS High for 1 Clock Period (Page Mode)

4.0 ADDRESS DECODER

This uses the BSM's IOEN signal to generate the following "chip selects":

$\overline{CRE}$	BPU Control Reg Load
$\overline{PDLE}$	BPU Pixel Port Latch Enable
$\overline{POE}$	BPU Pixel Port Output Enable
$\overline{ENPROM}$	PROM Output Enable
$\overline{ENUART}$	UART I/O Enable
LMASK	Latch VPC Control Data from RGP
$\overline{FSE0}$	BPU Function Select Reg Load, Plane 0
$\overline{FSE1}$	BPU Function Select Reg Load, Plane 1
$\overline{FSE2}$	BPU Function Select Reg Load, Plane 2
$\overline{FSE3}$	BPU Function Select Reg Load, Plane 3

These signals are derived using straightforward combinational logic. Their timing follows the BSM's IOEN (see next section).

5.0 BUS STATE MACHINE

This generates the following signals:

RDY	RGP Ready Signal
$\overline{RAS}$	RAS signal to VRAM
$\overline{R/C}$	Row/Column Address Selector to Address Multiplexer
$\overline{NCASIN}$	Master $\overline{CAS}$ Signal to VPC
$\overline{WR}$	Write Signal to VRAM and UART
DT/$\overline{OE}$	Data Transfer/Output Enable to VRAM, Read Signal to UART
$\overline{DDIN}$	Data Direction Signal to Transceiver on RGP's Bus
$\overline{DBE}$	Data Buffer Enable to Transceiver on RGP's Bus
$\overline{DLE}$	BPU Data Latch Enable
$\overline{DOE}$	BPU Data Output Enable
RFIP	Refresh in Progress to VPC
IOEN	Linear Access Timing Strobe

5.1 BSM Basics

To derive a scheme for controlling the bus accesses consider that data flow during Drawing accesses can overlap with the start of the next RGP cycle, as shown in *Figure 3*. Indeed, the RGP's BPU FIFO control signals (FRD and FWR) are timed to use this overlap.

This causes no problem with Local Bitblt; for Interplane Bitblt however, since the Source data appears on the common bus during Source Reads, it is necessary to "cut" the RGP's data path for the first part of the overlapped access as this could be a linear access.

BSM TIMING

During each cycle of the RGP the BSM will need to change both its state and its outputs based upon its present state and inputs from the RGP.

To avoid having to use very fast logic the example system uses a pipelined technique for the BSM:

- Input changes occurring during a particular RGP cycle cause the BSM to change state at the beginning of the following cycle. The state is clocked by the rising edge of PH1.
- Output changes which occur as a result of this state change happen at the beginning of the cycle after this, and are clocked by the rising edge of PH1.

Consequences of this are that an input change occurring during cycle "N" will result in an output change in cycle "N + 2"—something that must be remembered when looking at the BSM timing diagrams which follow.

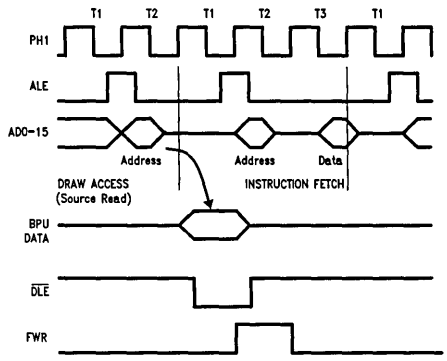
The one exception to this scheme is the signal $\overline{NCASIN}$, which is used by the VPC to selectively generate $\overline{CAS0-3}$ for the memory planes. $\overline{NCASIN}$ is a combinational BSM output, and is clocked by the rising edge of PH1 in the VPC after being processed by more combinational logic (see section 6.0). Thus $\overline{CAS0-3}$ become valid at the beginning of RGP cycles, just like BSM outputs. In the timing diagrams (*Figures 7* to *14*) which follow, $\overline{CASn}$ is shown rather than $\overline{NCASIN}$, the "n" representing any one or more of 0 to 3.

Figure 4 shows the structure of the BSM and the timing relationships between inputs, states and outputs.

BSM Bus Requests

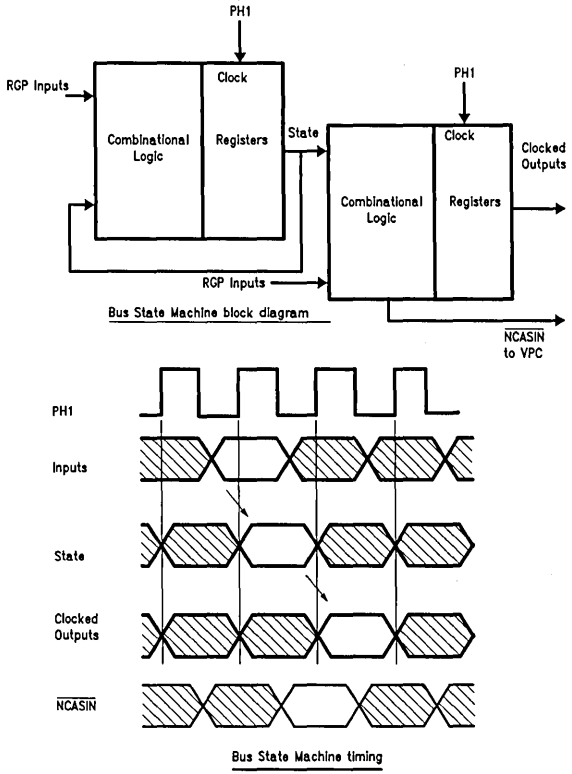
There are two sources of bus access requests: the RGP and the Refresh Timer. The BSM contains two flip flops to denote a bus request from these sources:

RGPRQ: Set by the RGP's ALE, Reset by the BSM
RFRQ: Set by the Refresh Timer, Reset by the BSM.



TL/F/9762-3

FIGURE 3

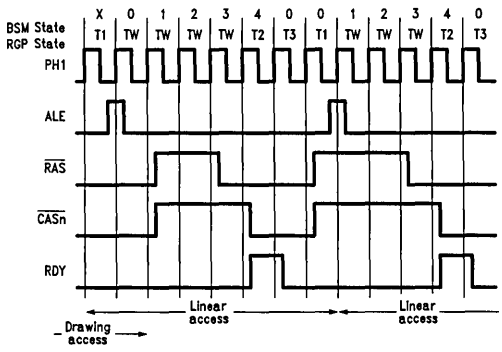


TL/F/9762–4

FIGURE 4. Bus State Machine Timing

The principle of the BSM described here is that, on getting a bus request from one of these sources (with RGPRQ having the higher priority), the BSM counts through a sequence of states, ultimately ending in state 0, the idle state, where it remains until another bus request occurs. The particular sequence used depends on the type of access required, and can be determined by decoding the RGP status lines and the Bus access requests:

Access Type	RGPRQ	RFRQ	BS1	BS0	$\overline{R}$	$\overline{W}$
Linear Read	H	L	L	X	L	H
Linear Write	H	L	L	X	H	L
BitBlt Source Read	H	L	H	L	L	H
BitBlt Dest Write	H	L	H	L	H	L
Draw Read/Mod/Write	H	L	H	L	L	L
VRAM Transfer	H	X	H	H	L	H
VRAM Refresh	H	H	L	X	X	X
or	H	H	X	L	X	X



TL/F/9762–5

FIGURE 5

5.2 BSM Linear Accesses

The linear access is used for Instruction Fetches, Operand Reads and Writes, and general Input/Output. The previous access could have been either a Drawing access ($\overline{RAS}$ ending in the cycle after T1) or another linear access ($\overline{RAS}$ ends in previous T3). Both possibilities are shown in *Figure 5*.

To meet the VRAM timing requirements for the system we need to allow for the worst case (in which the previous access is a Drawing access). Thus $\overline{RAS}$ for the Linear access can start two cycles later as in *Figure 5*.

The above analysis is for a relatively simple Bus State Machine. A more complex design could reduce the impact (1 extra clock cycle) of allowing for a previous Drawing access by recognizing a sequence of Linear accesses. In this case, because only two cycles of RAS precharge are needed, the access can be started one cycle earlier. Additionally, for the example BSM design, the same timing is produced for all linear accesses regardless of the type of memory being accessed—again, a more complex design could vary the timing according to the type and speed of memory being accessed.

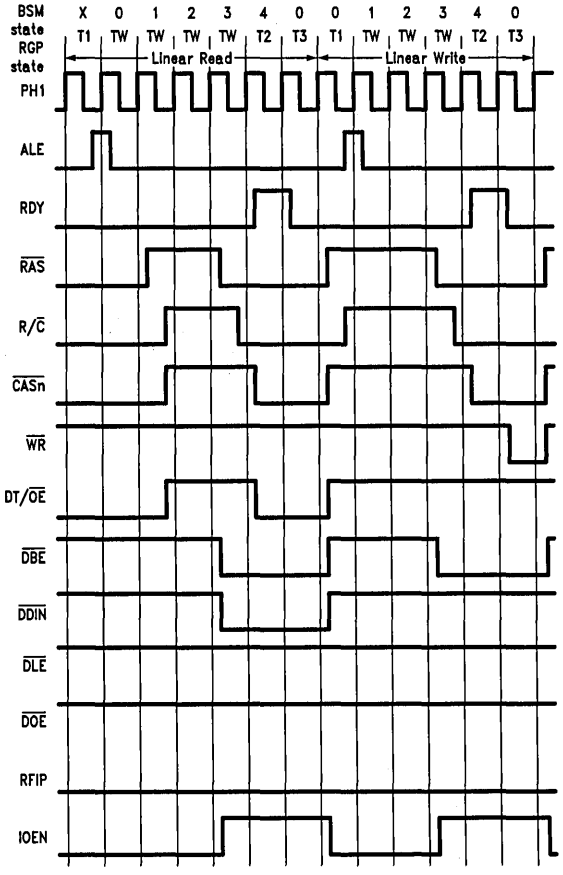
The complete BSM behaviour for a Linear Read access followed by a Linear Write access is shown in *Figure 6*. Once the previous access has completed (i.e., the BSM has reached state 0) the BSM determines that an RGP bus request is pending (RGPRQ has been set by ALE going high), and starts the Linear access by branching to state 1.

In subsequent clock cycles the BSM enters states 2, 3 and 4, and finally state 0. The RGP's RDY input is asserted during state 4 so that the RGP will complete the access, with data becoming valid at the RGP's inputs at the end of T3.

Note that R/$\overline{C}$, which switches the VRAM address lines between Row addresses (when High) and Column addresses (when Low) is generated by delaying the $\overline{RAS}$ signal by half a clock period.

Also, since the RGP will latch the read data from the accessed memory or device at the end of T3 during the Read access and send data out during the write access, the RGP's Data bus transceiver is enabled by $\overline{DBE}$ and its direction controlled by $\overline{DDIN}$. The timing strobe IOEN is produced, with the same timing as $\overline{CASn}$, so that the Address Decoder block can produce the appropriate strobes to the accessed device.

DT/$\overline{OE}$ pulses low to enable data from the accessed memory during the Read access, and $\overline{WR}$ pulses low to write data to memory.



TL/F/9762–6

Conditions for Linear Access: BS1 = L, RGPRQ = H, RFRQ = L

FIGURE 6. Linear Read and Write, Preceded by Draw Access

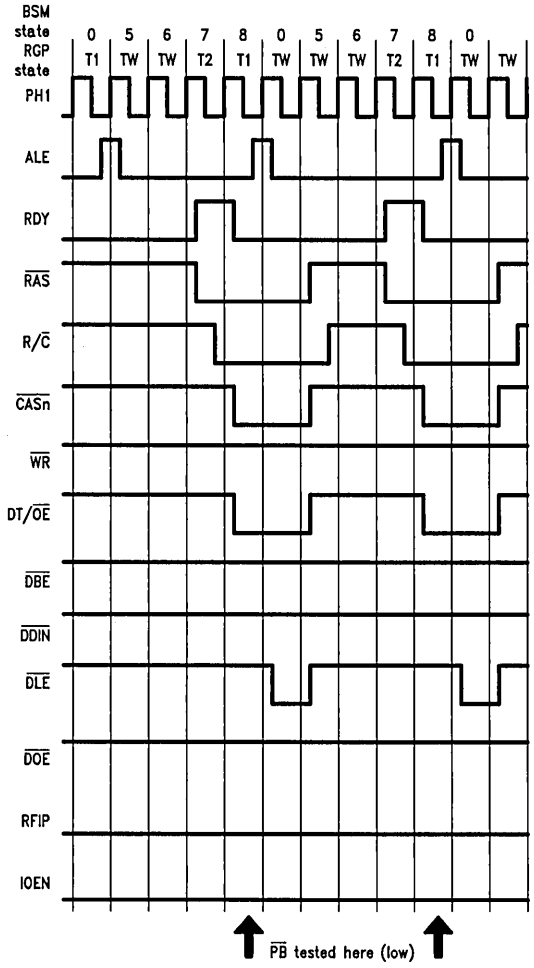
5.3 BITBLT Source Read and Destination Write Accesses

The first type of Drawing access to be considered is the Bitblt Source Read: this occurs when the BPU FIFOs are being filled prior to the Destination Write or Read/Modify/Write accesses during a Bitblt.

Figure 7 shows the BSM behaviour when a Page Break occurs, i.e., page-mode memory cycles are not possible because subsequent accesses are to different rows (or "pages") of memory. During state 8 the RGP's $\overline{PB}$ signal is determined to be Low, so the BSM branches to state 0 to terminate the access (by bringing $\overline{RAS}$ High).

DT/$\overline{OE}$ is produced to enable the data from memory, which is latched into the BPUs with $\overline{DLE}$. Note that for interplane Bitblts only one memory plane is read, but the data may be latched in several BPUs: the VPC logic controls the data routing.

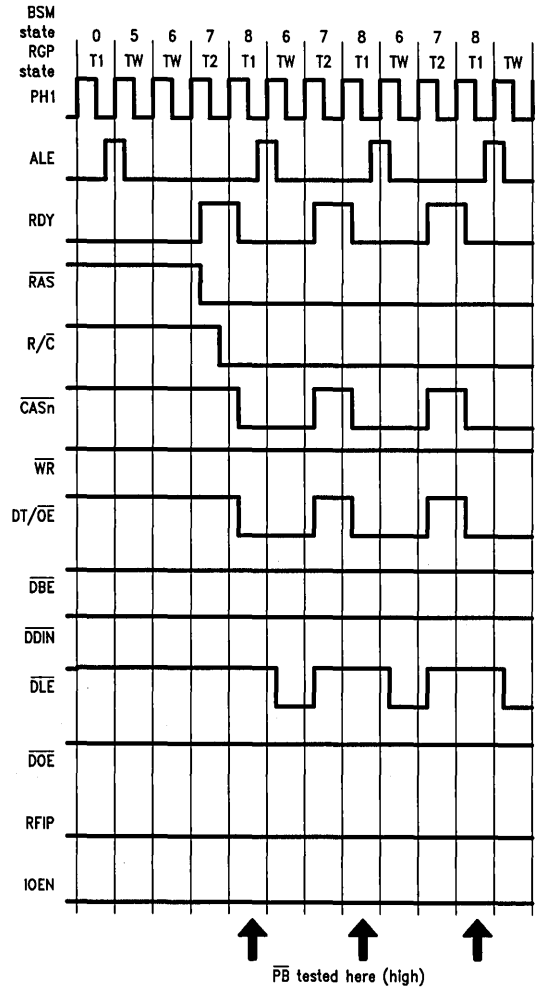
Figure 8 shows the BSM behaviour for page-mode memory accesses.



TL/F/9762–7

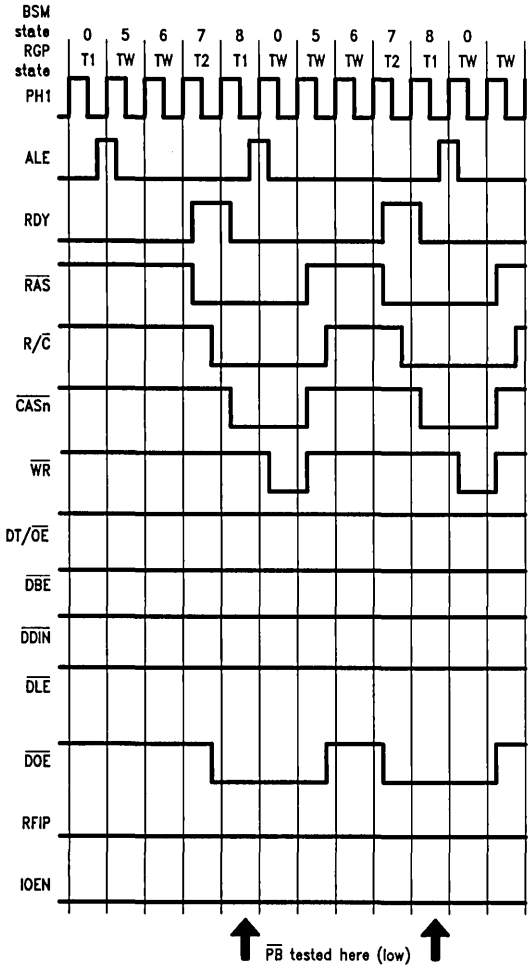
Conditions for Bitblt Source Read: BS1 = H, BS0 = L, RGPRQ = H, RFRQ = L, $\overline{R}$ = L, $\overline{W}$ = H

FIGURE 7. Bitblt Source Read, Non-Page Mode



TL/F/9762–8

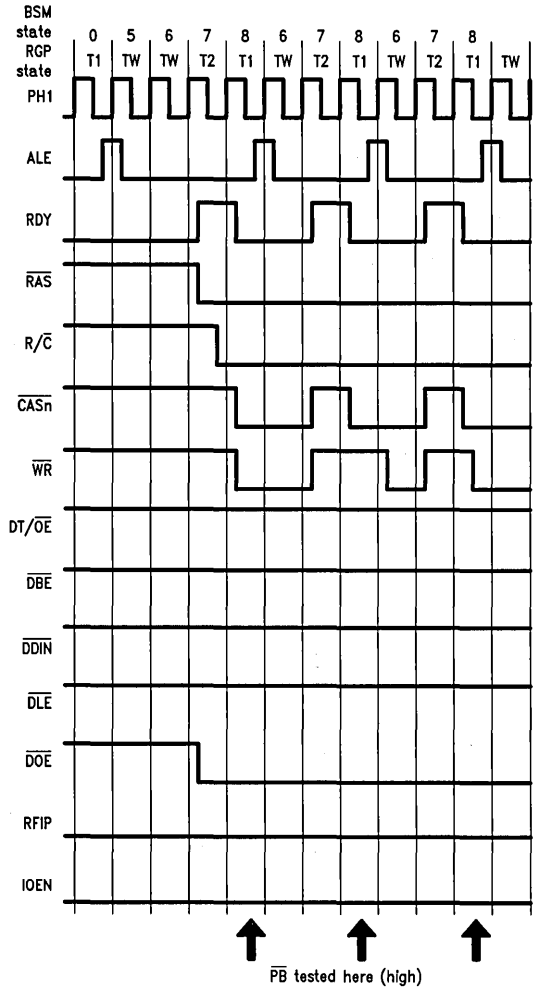
FIGURE 8. BitbIt Source Read, Page Mode



TL/F/9762–9

Conditions for Bitblt Destination Write: BS1 = H, BS0 = L, RGPRQ = H, RFRQ = L, $\overline{R}$ = H, $\overline{W}$ = L

FIGURE 9. Bitblt Destination Write, Non-Page Mode



TL/F/9762–10

FIGURE 10. Bitblt Destination Write, Page Mode

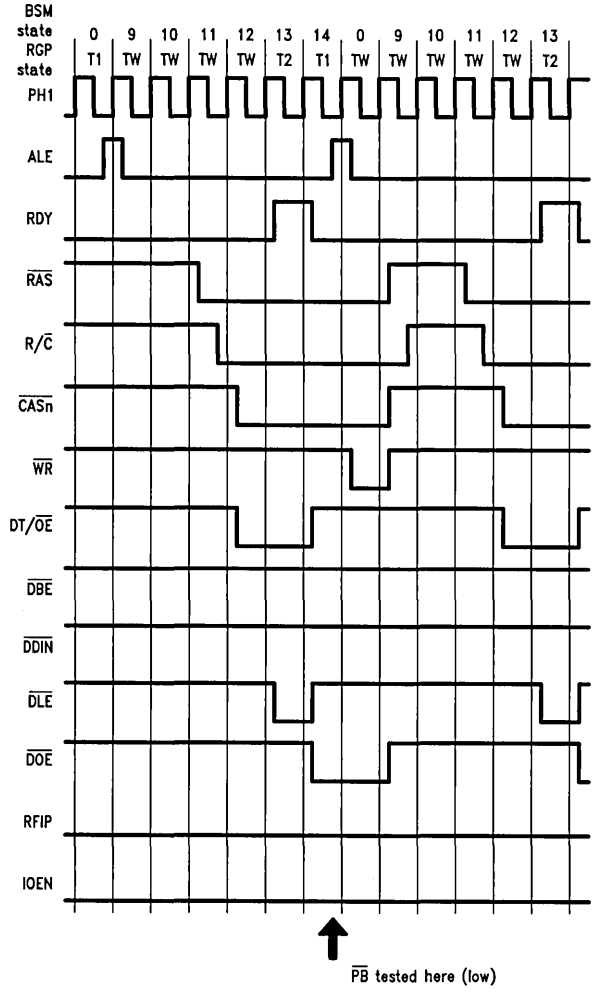
If, during state 8, the BSM finds that the next access is the other basic type of Drawing operation (Read/Modify/Write) and there is no Page Break then a branch will occur to the corresponding point in its state sequence (state 10).

Figures 9 and *10* show the state sequences for Destination Write accesses; these are identical to the states for Source Reads but the outputs differ. In particular the $\overline{DOE}$ output is asserted during the $\overline{RAS}$ pulse to enable data out of the BPUs, and the $\overline{WR}$ output is pulsed at the end of $\overline{CASn}$ to write the data to the VRAM.

5.4 Draw Read/Modify/Write Accesses

This type of access occurs during both Line Drawing (always) and Bitblt (if the Bitblt Combine option is chosen, and for both this and the OverWrite option during modification of boundary Destination words).

Figure 11 shows non-Page mode accesses. The BSM uses states 9 to 14. DT/$\overline{OE}$ is pulsed during the first half of the $\overline{CASn}$ signal to read the memory data into the BPUs, where it is latched with $\overline{DLE}$. (For Bitblt accesses the RGP's FRD signal simultaneously fetches the aligned Source data from the BPU FIFO).



TL/F/9762-11

Conditions for Draw R/M/W: BS1 = H, BS0 = L, RGPRQ = H, RFRQ = L, $\overline{R}$ = L, $\overline{W}$ = L

FIGURE 11. Draw Read/Modify/Write, Non-Page Mode

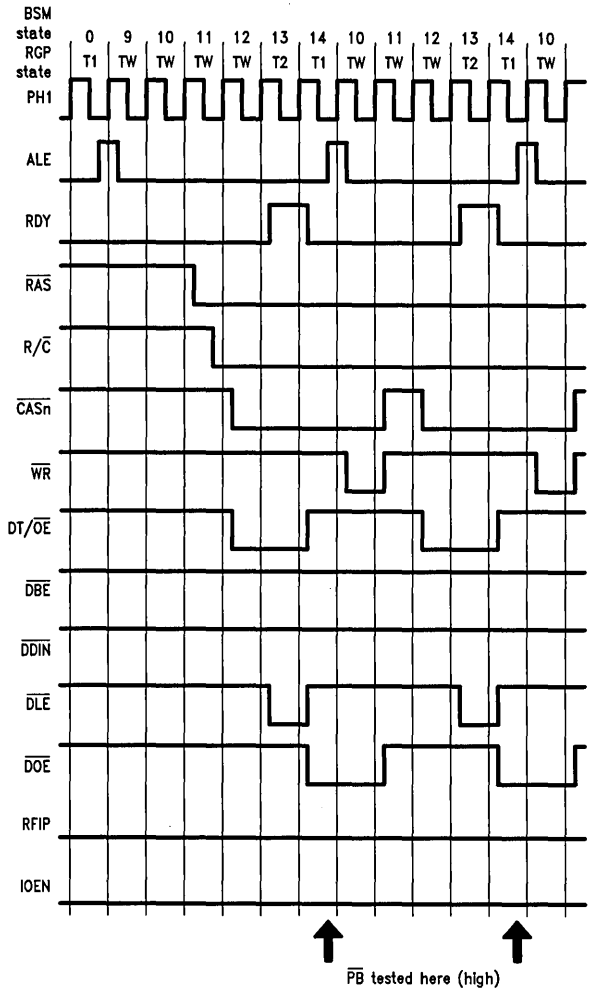
During the second half of $\overline{CASn}$ the BPU's logic unit output data is enabled out to memory by $\overline{DOE}$, and written to memory by $\overline{WR}$.

If, during state 14, the BSM finds that the next access is the other basic type of Drawing operation (Source Read or Destination Write) and there is no Page Break then a branch will occur to the corresponding point in its state sequence (state 6).

Figure 12 shows the same accesses in Page mode.

5.5 VRAM Transfer Access (Screen Refresh)

The RGP, if appropriately programmed, will request a bus access for VRAM data transfer at the beginning of each display scan line, or when the display row address is zero. During this access up to 256 words of data are transferred from the VRAM memory array to the VRAM shift registers, and from there are transferred to the display device.



TL/F/9762–12

Conditions for Draw R/M/W: BS1 = H, BS0 = L, RGPRQ = H, RFRQ = L, $\overline{R}$ = L, $\overline{W}$ = L

FIGURE 12. Draw Read/Modify/Write, Page Mode

The example system uses a display "warp" of 64 words, which avoids the requirement for VRAM transfers in the middle of scan lines. So VRAM transfer accesses occur only at the beginning of scan lines, during blanking time, and well before active video time.

The VRAM performs a transfer when DT/$\overline{OE}$ is Low before $\overline{RAS}$ is asserted. The BSM asserts DT/$\overline{OE}$ in state 16, and then asserts $\overline{RAS}$ in state 17, as shown in *Figure 13*. The remainder of the access is conventional except that the output RFIP is asserted. This tells the VPC that $\overline{CAS}$ outputs to all planes must be asserted.

5.6 VRAM Refresh Access

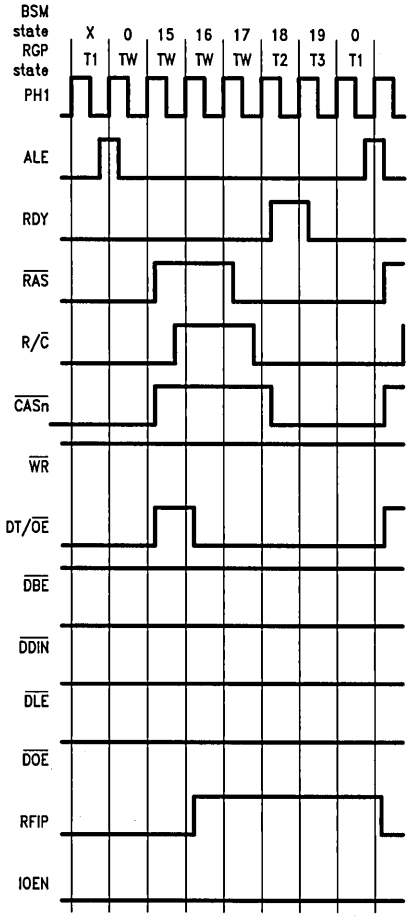
When the Refresh timer causes a bus request, by setting RFRQ, and the current bus access has completed by reaching state 0, the BSM will initiate a VRAM Refresh access. This uses the VRAM's internal refresh row counter by asserting $\overline{CAS}$ Low before $\overline{RAS}$.

The BSM inserts RGP wait states by holding RDY Low until the refresh access is completed—the pending RGP bus access can then continue. RFIP is asserted during the refresh so that the VPC will assert $\overline{CAS}$ to all planes.

Figure 14 shows the BSM's behavior.

6.0 THE VIDEO PLANE CONTROLLER

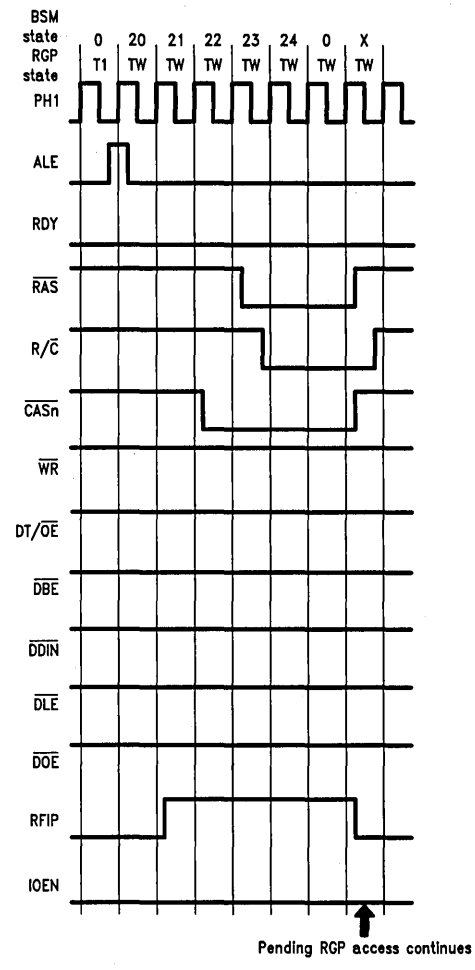
The function of the Video Plane Controller (VPC) is to enable, under program control, some or all of the planes for Drawing operations, and to control the data transceivers on each plane.



TL/F/9762–13

Conditions for VRAM Transfer: BS1 = H, BS0 = H, RGPRQ = H, RFRQ = X, $\overline{R}$ = L, $\overline{W}$ = H

FIGURE 13. VRAM Transfer (Preceded by Draw Access)



Conditons for VRAM Refresh: RGPRQ = H, RFRQ = H, BS1 = L or BS0 = L

FIGURE 14. VRAM Refresh

Plane Memory Control

Several control methods are possible:

- Disabling inactive planes by programming their BPUs to the "Destination = Destination" function. These planes therefore write back their images without any changes. This method does not require additional hardware, but does not allow the use of interplane Bitblt (there will be bus contention during Source reads).
- Steering $\overline{WR}$ to selected planes, so that only active planes can change their data. This method also does not allow the use of interplane Bitblt.
- Steering $\overline{RAS}$ to selected planes. This method could incur extra delay in the $\overline{RAS}$ pulse, which in many designs can not be tolerated. Also this method is not guaranteed to work for all VRAMs.
- Steering $\overline{CAS}$ to selected planes. This method does work satisfactorily, and any extra delay in asserting $\overline{CAS}$ can usually be tolerated.

$\overline{CAS}$ steering is the method used in the example system. By using the CAS timing strobe, $\overline{NCASIN}$, from the BSM prior to clocking on the rising edge of PH1, no additional delay in $\overline{CASn}$ is incurred.

The VPC must be programmed (by an Operand Write from the RGP to address E00007 in the example system) for which plane or planes are to be active—the "Write mask", and if an interplane Bitblt is required. Four RGP data bits, D0–3, correspond to the four plane's Write Mask, and D15 is used for the interplane bit. The signal (LMASK) which latches these bits in the VPC is generated by the Address Decoder logic.

During drawing operations, except for interplane Bitblt Source Reads, plane n is enabled ($\overline{NCASIN}$ from the BSM is routed to $\overline{CASn}$ and clocked on the rising edge of PH1) if its corresponding Write Mask bit is a 1.

During linear accesses (BS1 is Low) and the interplane Bitblt Source Reads (BSE and BS1 are High, BS0 is Low, and the interplane bit is 1) a plane is enabled if the RGP's address lies within the plane's address bounds.

During VRAM Transfer accesses and VRAM Refresh operations (RFIP is High) all $\overline{CAS}$ outputs need to be asserted for the duration of RFIP.

Thus in the example system the VPC needs to decode address lines A17, 18, 22 and 23 to detect the plane being addressed, and decode RFIP, BS1, BS0, BSE and the interplane bit.

It should be noted that during interplane Bitblt Source Reads, however, BS1, BS0 and BSE are not valid during state 8; at this time they will change for the next RGP access. Therefore the VPC must effectively latch their value during these accesses.

Plane Transceiver Control

The VPC also generates the Enable ($\overline{BEn}$) and Direction (DIRn) control signals for the transceiver on each plane. The sense of DIR is that when it is High data is moved from the VRAM to the common bus (i.e., for memory reads).

During linear accesses to VRAM (BS1 and A23 are Low and A22 is High) $\overline{BEn}$ is asserted according to which plane is being addressed (a decode of A17 and A18). DIRn is the inverse of RGP's $\overline{R}$ output.

During linear accesses to the BPU Control registers ($\overline{CRE}$ is Low), all $\overline{BEn}$ are asserted and DIRn is Low.

During linear accesses to the BPU Function Select registers ($\overline{FSEn}$ is Low), $\overline{BEn}$ is asserted according to which one or more registers is being accessed and DIRn is Low.

During Interplane Bitblt Source Reads all $\overline{BEn}$ are asserted. DIRn for the Source plane (the plane being addressed by the RGP) is High, and for the other planes (which will latch the Source plane's data in their BPUs) DIRn is Low.

During all other Drawing accesses the transceivers are disabled ($\overline{BEn}$ are High).

Thus for transceiver control the VPC needs to decode address lines A17, 18, 22 and 23, and BS1, BS0, BSE and the interplane bit. The earlier comment about the validity of the RGP status signals during state 8 of the Bitblt Source Reads applies to the transceiver control logic as well.

7.0 INTERFACING TO AN EXTERNAL PROCESSOR

The open architecture of the Advanced Graphics Chip Set means that an interface to an external or co-processor can be achieved in a number of different ways, depending on the designer's requirements.

The technique offering the highest performance is that of using shared memory, where the external processor can take control of the graphics subsystem's bus and access memory directly.

The interface design described above requires three basic sets of signals from the bus controller.

- Address Signals (Inputs)
- Data Signals (Bidirectional)
- Status Signals (Inputs, Plus RDY Output)

The BSM design could easily be modified to cater for an external processor by adding an input which indicates a bus request by the additional processor. Once the BSM has granted bus access (putting the RGP in HOLD or inserting Wait states), this processor can present its Address, Data and Status signals to the BSM, VPC and Address Decoder, and access the memory. The BPUs can also be controlled, allowing both planar and pixel accesses by the external processor.

8.0 SUMMARY

The implementation of a memory interface for the National Semiconductor DP8500 Raster Graphics Processor is straightforward. The RGP provides sufficient status and timing signals to interface flexibly and efficiently to any variety and mixture of memory and peripheral devices.

This application note has described the implementation of an interface between the RGP and various types of memory, by reference to the DP850EB system.

The LM1823: A High Quality TV Video I.F. Amplifier and Synchronous Detector for Cable Receivers

National Semiconductor
Application Note 391
Martin Giles

INTRODUCTION

The LM1823 is a video I.F. amplifier designed to operate at intermediate carrier frequencies up to 70 MHz, and employ phase locked loops for synchronous detection of amplitude modulation on these carrier frequencies. The high gain, wide AGC range and low noise of the LM1823 make it ideal for use in television receivers, video cassette recorders and in cable TV set-top converters requiring high quality detected base-band video and an audio intercarrier. Typical performance characteristics and features of this I/C are summarized in Table I below.

TABLE I

Maximum system operating frequency	70 MHz
Typical I.F. amplifier Gain (45.75 MHz)	>60 dB
I.F. amplifier gain control range	55 dB
True synchronous detector with a PLL	
Detector conversion gain	34 dB
Detector output bandwidth	9 MHz
Detector differential gain	2%
Detector differential phase	1 degree
Noise averaged AGC system	
Internal AGC gated comparator	
Reverse tuner AGC output	
DC controlled video detection phase	
AFC detector	

THE R.F. SIGNAL FORMAT

Despite the wide variety of signal sources available to the home television receiver—broadcast, cable, satellite, video games etc.—on channel carrier frequencies from 55.25 MHz to 885.25 MHz, the spectral content of each R.F. channel has been established for many years. In the United States the channel bandwidth is fixed at 6 MHz with the picture carrier located 1.25 MHz from the lower end of the band, and an aural carrier placed 4.5 MHz above the picture (pix) carrier. Introduction of color television in the early fifties added another carrier, the chroma sub-carrier, positioned 3.58 MHz above the pix carrier frequency. The pix carrier is amplitude modulated* by the baseband video signal (which includes the synchronization information and the phase and amplitude modulated chroma subcarrier) while the aural carrier is frequency modulated. Television channels in Europe use similar carriers with the refinement of a fluctuating chroma subcarrier phase (P.A.L.).

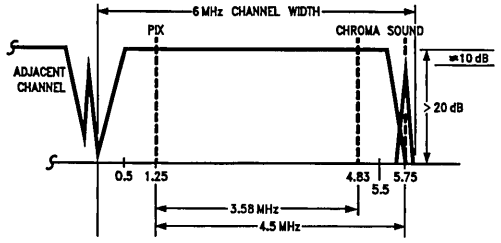
* A more appropriate term is "negative downward modulation" since any modulating signal causes a decrease in the peak carrier amplitude (compared to conventional a.m., where the modulating signal alternately increases and decreases the peak carrier level with the mean carrier level remaining constant). For television carriers, syncs correspond to peak carrier and increasing brightness causes decreasing carrier amplitudes.

The signal coming into the receiver has this general format and the receiver R.F. and I.F. circuits are designed to handle such a signal and reduce it back to the baseband composite video and audio intercarrier. Even where signal scrambling is used to protect the video modulation from unauthorized detection, the R.F. spectrum must remain within this format. For satellite broadcasts with frequency modulation of the video signal, the signal is demodulated and then remodulated onto a low VHF channel for reception by standard television receivers. In connection with this, the LM1823 PLL detector is not suitable for wide-band FM detection—even though the I.F. carrier (70 MHz) is well within the LM1823 I.F. amplifier frequency capability.

Notice again that the pix carrier is located at one end of the occupied bandwidth and only the upper sidebands are being fully transmitted. The lower sidebands are truncated with only frequencies close to the pix carrier frequency modulating the carrier. This method of conserving the frequency spectrum is referred to as vestigial sideband transmission.

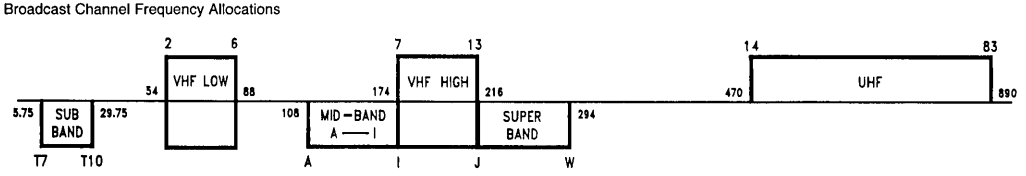
THE CABLE CONNECTION

Originally introduced many years ago as a means for providing broadcast TV to isolated areas or where the terrain made direct reception difficult, cable TV had modest growth in the U.S. and was a stagnating industry until the mid-seventies. Lower cost satellite earth stations were the turning point, allowing cable operators access to many varied program sources from any part of the country.



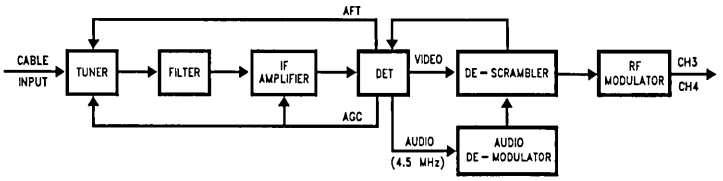
TL/H/8421–1

FIGURE 1. U.S. Broadcast Channel Spectrum



TL/H/8421–2

FIGURE 2. Broadcast and Cable Bands in the U.S.



TL/H/8421–3

FIGURE 3. Cable Set-Top Converter Block Diagram

Standard television receivers in the U.S. tune to VHF channels 2 through 13 and UHF channels 14 through 83, and initially cable operators used the 12 VHF channels for their program material. With increased sources soon all channels were occupied on some systems creating significant demands on television tuner and I.F. amplifier strips. More space yet was needed and rather than using UHF channel allocations starting at 470 MHz because of cable signal attenuation (typically 0.8 dB/100 ft. at 300 MHz), operators turned to the unused spectrum space between VHF channel 13 and UHF channel 14. Naturally, since standard TV receivers could not tune to these channels, the set-top converter came into being. Each of the new channels could be converted to a low VHF channel to be received on the standard TV. Television manufacturers responded, and with the common introduction of varactor tuners were soon able to offer "cable ready" televisions capable of tuning to all the new cable frequencies. This meant that customer conveniences such as remote control of channel selection also became available. Unfortunately it aggravated a problem already confronting the cable operator. Since standard television receivers couldn't tune to the cable channels, operators had been able to offer premium services on some of these frequencies, paid for by subscribers who rented the appropriate set-top converter box. This didn't prove very secure since one operator's "free" channel was another operator's "pay" channel, and the introduction of cable-ready televisions ensured the eventual demise of such systems.

Scrambling the signal, a technique already being used by over-the-air subscription television, has become common in the cable service. The degree of scrambling* is limited since the scrambled signal spectrum must remain within the channel allocation and anything done to the signal must be subsequently undone without noticable degradation of the signal.

Generally for television, scrambling means a pulse or sine wave suppression of the signal horizontal blanking pulse interval so that the sync-tips occur between the black and white levels instead of always below black level. The standard television sync separator does not function well with this signal and the I.F./tuner AGC circuits will not work properly, effectively scrambling the displayed picture. Other techniques include random inversion of the video information to provide an even greater degree of security.

The means used to encode such a scrambled signal gives rise to the terms "in band scrambling" and "out of band scrambling". With cable ready television receivers capable of tuning to the scrambled channel, the decoder can be a simple broad-band gain switch (to change the signal R.F. amplitude during horizontal blanking) with a separate receiver tuned to the decoding data carrier frequency, which is located outside the signal channel. This permits use of the television receiver in a normal way but does require simultaneous switching of the decoder receiver with channel changes.

Also, spectrum space must be reserved for each scrambled channel's data carrier.

A more popular method of scrambling is "in band scrambling" where the data carrier to decode the signal is included inside the transmitted signal channel, usually within the aural carrier. Any number of channels can be scrambled and now different levels of service can easily be added or deleted without the need to rewire the decoder box. This is achieved by including time multiplexed binary "tags" along with the sync information so that special programs can be identified. Individual subscriber boxes can be similarly addressed and turned on or off by the cable operator. In these types of systems, the LM1823 and LM2889 have obvious applications. The LM1823 is able to provide an excellent baseband signal inside the decoder box, which signal is then remodulated on a low VHF channel carrier by the LM2889 for retransmission to the standard television receiver. Clearly, the highest possible performance is desireable to prevent any noticeable difference between a converted channel, whether scrambled or not, and a regular off-air broadcast channel. (For a complete description of the LM2889 modulator I/C see AN402).

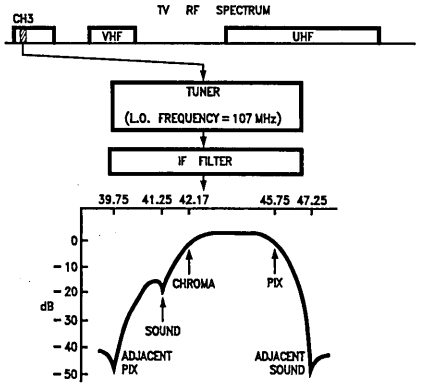
*Other security techniques such as jamming or trapping are used but since jamming is easy to defeat and trapping requires removal or replacement of filters in the cable drop to individual subscribers, scrambling the signal is receiving a lot more attention.

THE RECEIVER FRONT-END

The typical receiver front-end consists of a tuner, I.F. amplifier, I.F. filters and a video/sound intercarrier detector stage. These circuits are designed to provide a number of functions:

1) Select (tune) a specific R.F. channel in a band of frequencies.
2) Provide rejection to adjacent and other channels in the band.
3) Amplify low level R.F./I.F. signals prior to detection of the modulation.
4) Avoid overload on high level R.F. signals.
5) Trap or attenuate specific frequencies within the channel bandwidth to ensure a proper detected frequency response is obtained.
6) Linearly demodulate all desired modulating frequencies on the carrier.
7) Produce a noise-free video signal at the detector.
8) Provide automatic gain control (AGC) to compensate for changing signal strength at the receiver input.
9) Provide automatic frequency control (AFC) to the tuner local oscillator (L.O.) to maintain the carrier intermediate frequency (I.F.).

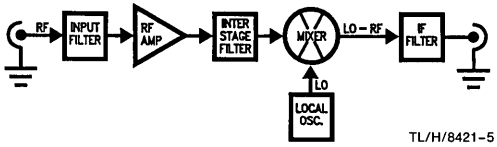
N.B. Items 8) and 9) have previously been provided in part by circuits external to the conventional I.F. amplifier. However, these functions are completely included with the LM1823 leading to overall performance improvements and reduction in external parts count and cost.



TL/H/8421–4

FIGURE 4. R.F. Tuning and I.F. Conversion (Note High Side L.O. Reverses the Relative Position of the Picture Chroma & Sound Carriers. c.f. *Figure 1*).

Although we are not directly concerned with the tuner design in this application note, it is useful to understand the design goals and constraints on the tuner for at least two reasons. First, since the tuner and I.F. amplifier interact very closely to obtain and maintain a noise-free picture, we need to know something about the tuner in order to provide the correct gain distribution and AGC action. Second, when the two functions are finally placed together, we need to know where to look to solve visible problems that may have become apparent. In some instances, either the tuner or the I.F. amplifier may be at fault, and a good understanding of the system interaction is needed to ensure that the appropriate action is taken.



TL/H/8421–5

FIGURE 5. Typical Single Conversion Tuner

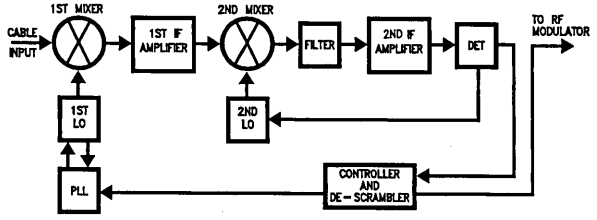
Both single conversion and double conversion techniques are used in cable converter tuners. The single conversion type is similar to the conventional TV receiver tuner and consists essentially of an R.F. stage, mixer stage, and local oscillator. Usually some input filtering is done to help match the cable to the input device and provide some rejection to unwanted signals outside the operating channel. Further rejection to unwanted signals, such as the I.F. frequency radiated back from the I.F. amplifier, is accomplished with interstage filtering between the R.F. amplifier and the mixer, and finally an output filter matches the mixer output to the cable feeding the I.F. amplifier. For convenience, we are assuming the desired output impedance is 75Ω and that the major I.F. amplifier frequency selectivity is determined by a block filter placed between the tuner output and I.F. amplifier input. This is consistent with modern practice using surface acoustic wave filters (SAWF's) and high gain stabilized I/C amplifiers (LM1823). Even so, as noted in more detail later, the LM1823 does provide opportunities for more filtering at the I.F. amplifier output prior to the detector stage.

Dual conversion tuners have been popular for a number of years and use first L.O. frequencies that are above the input R.F. bandwidth, avoiding problems with L.O. leakage back onto the feed cable. The second L.O. and mixer convert the high first I.F. to a Ch 3 or Ch 4 carrier for reception by the TV receiver. The addition of PLL's to control the first L.O. and descrambling networks on the R.F. output have added sufficient complexity to such converters that they are now called "set-top terminals". Also, since the scrambling techniques have become more sophisticated the signal is now frequently converted down to baseband before decoding and remodulation on Ch 3 or Ch 4 carriers. The high first I.F. has the advantage that image signal rejection is achieved without the switchable filters necessary at the input to the single conversion tuner. However, the absence of these filters does mean that care must be exercised to avoid generation of intermodulation products that "talk back" onto the cable (up conversion of the R.F. signal has been proposed as a way to minimize intermodulation components). Another disadvantage of the dual conversion tuner shown in *Figure 6* is that it typically has a very high Noise Figure, often between 14 dB to 16 dB. This is because the signal is applied directly to the first mixer which is a passive, double balanced diode mixer. As discussed in more detail later when we look at SAWF's between the tuner and the I.F. amplifier, a pre-amp in front of the mixer can improve the N.F. to 6 dB to 8 dB, especially in a baseband converter where an AGC voltage is available to help the tuner handle the input signal strength range.

Returning to the single conversion tuner, the major parameters to be considered are as follows:

1) Power gain
2) Noise Figure
3) Good Cross-Modulation rejection
4) VSWR
5) AGC Range
6) Impedance changes with AGC
7) Overload capability
8) Channel 6 beat rejection
9) Curve tilt (tracking)
10) L.O. drift and radiation

For an I.F. amplifier design, items 1), 2), 7), and 8) are the most significant, but if the tuner designer has overlooked the others we may see some problems when the tuner and I.F. amplifier are hooked together.



TL/H/8421–6

FIGURE 6. Dual Conversion Tuner

Crossmodulation describes the condition wherein the modulation information on an adjacent channel (usually) is transferred on to the desired carrier. A typical specification is the undesired carrier level with 30% modulation needed to cause 1% modulation of the desired carrier level.

Crossmodulation is particularly likely to occur in cable systems and is usually observed as sync bars drifting through the picture. In particularly severe cases the interfering picture can actually be seen. High signal levels at the input of the mixer are a frequent cause of crossmodulation, particularly when high gain R.F. stages are used to obtain a low tuner noise figure (N.F.). But when AGC is applied the crossmodulation source often shifts to the R.F. device.

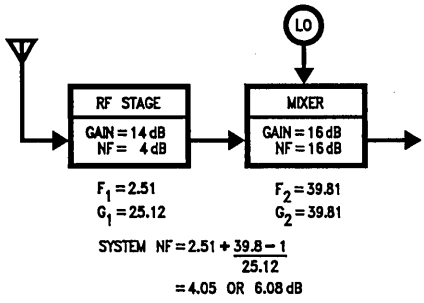
When overload occurs, (measured as the total harmonic distortion of a specified modulation frequency), the peaks of the R.F. carrier waveform become compressed and this will show up at the video detector as a smaller sync pulse amplitude (sync tip to black level). Since the AGC system operates on the sync tip level the effective result is that the black level appears to go blacker than black—i.e. some near black information will be lost and the picture will appear to have too much contrast. Alternatively if the subsequent receiver circuits have black level restoration the screen brightness increases and picture tube blooming on peak whites may occur. As overload increases there is a strong chance that vertical sync will be lost. Generally the tuner mixer device is the first stage to overload, followed by the R.F. stage. While overload is caused by very strong signal strengths and therefore may appear to be of limited concern it can also occur at weak to intermediate signal strengths because of incorrect AGC threshold settings and this will be discussed in detail later.

Channel 6 beat is a phenomenon related to mixer overload and occurs because of the choice in the U.S. of 45.75 MHz as the intermediate frequency. On channel 6, mixing of the sound and pix carriers produces a signal at 171 MHz which is then mixed with the channel 6 L.O. frequency to give 42 MHz. The I.F. sound and pix carriers can also mix with the channel 6 L.O. to produce 42 MHz. Since 42 MHz is only 170.455 kHz from the I.F. chroma subcarrier of 42.17 MHz, after detection wavey lines will appear in colored areas of the picture. Turning down the receiver color level (saturation) control will eliminate the 170 kHz pattern and identify the problem as Channel 6 beat.

Curve tilt or tracking refers to the ability of the tuner filters to track the L.O. frequency as the channel selection is changed. Problems in this area are easily identified at the video detector output (sometimes referred to as the 2nd detector) since the effect is to cause changes in the relative amplitudes of the pix, sound and chroma carriers compared to that expected from the I.F. filter response. When the detector VCO and AFT circuits of the LM1823 are aligned to 45.75 MHz, the chroma burst located on the back porch (or breezeway) portion of the horizontal blanking period in the video signal will normally be −6 dB compared to the sync pulse amplitude. If mistracking is causing a loss of high frequencies on certain channels, the burst amplitude will be lower on these channels and the picture (in severe cases) will have watery and noisy colored areas with smeared off picture detail. When the loss occurs down at the pix carrier frequency, the burst amplitude is increased and the picture will become harsh with excessive overshoots.

Similar problems can occur on any specific channel simply due to mis-tuning or L.O. drift. In particular, as the L.O. frequency drifts high and the chroma subcarrier amplitude increases, the sound carrier also increases and chroma/sound beats will appear in the picture. In the U.S. the chroma/sound carrier beat is at 920 kHz (4.5 MHz—3.58 MHz) and appears as a herringbone pattern while the audio modulates the sound carrier. This 920 kHz beat can also be caused by detector non-linearities, and after the video detector by the detected 4.5 MHz sound intercarrier mixing with the chroma subcarrier in subsequent receiver stages. If turning down the color level control removes the 920 kHz beat then a better 4.5 MHz trap is needed at the video detector output.

These preceding comments are not meant to imply that the tuner is the root cause of all the nasty phenomenae that can be observed in the picture display. Overload, Channel 6 beat and video noise are very dependent of the tuner/I.F./AGC interaction. To understand why this is the case, we need to look at the demands that the input signal field strength puts on the system.



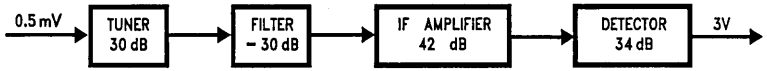
TL/H/8421–7

FIGURE 7. Typical Tuner Gain and Noise Figure

INPUT SIGNAL LEVELS

The smallest input signal is, of course, no signal or simply the noise level generated at the cable drop. To this noise level will be added the input noise of the tuner itself, giving rise to an equivalent noise input defined by the tuner noise figure (N.F.) While a specific design will have to take into account the actual operating parameters of the tuners available, we will assume a typical tuner configuration with an R.F. stage providing 14 dB gain and having a 4 dB N.F., followed by a mixer stage with 16 dB conversion gain and a 16 dB N.F. The N.F. of this combination is 6 dB, a fairly typical number, which will have the effect of increasing the actual input noise by a factor of 2. If our noise source is the cable impedance with a real part of 75Ω, at an ambient temperature of 290k, then the equivalent input noise is 2.2 uVrms (the noise contribution of any matching network or cable termination is ignored as this is included in the tuner N.F.).

Cable signal levels run from −6 dBmV to +15 dBmV with a typical system goal of maintaining a C/N ratio of at least



TL/H/8421–8

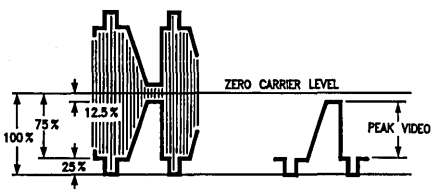
FIGURE 8. System Gain Distribution

43 dB at the cable drop to the subscriber. If a 0.5 mVrms signal is to produce the rated detector output of 3V (o-p)* for the LM1823 then we need a total system gain of at least 75 dB. Usually the SAWF connected between the tuner output and the I.F. input will have an insertion loss of 20 dB to 30 dB so that with the 30 dB tuner gain, the I.F. amplifier/detector is required to provide the remaining 76 dB. If the tuner is simply a diode mixer with a 6-8 dB insertion loss, the gain requirement increases to 114 dB.

*(o-p) means the detected zero carrier voltage level to the detected sync tip voltage level. The actual peak white signal to sync tip excursion at the detector will be 87.5% of this—2.63V (p-p). In the absence of a carrier, thermal noise will be present with amplitude peaks on both sides of the detected zero carrier voltage.

Fortunately the LM1823 has a high conversion gain detector (34 dB) and the I.F. amplifier gain can be set to well over 75 dB at 45.75 MHz (but we will see that some gain prior to the I.F. amplifier filter will be necessary if a good system N.F. is desired). Substantially more gain than necessary should be avoided however, even though there is plenty of AGC range in the I.F. amplifier (from 48 dB to 60 dB depending on external components). While at least 22 dB AGC capability is needed to accommodate the expected input signal strength range, if excessive system gain is used, forcing the I.F. amplifier into early gain reduction, the I.F. amplifier N.F. will begin to increase. With a diode mixer front end, the I.F. amplifier N.F. may contribute directly to the system N.F. and prevent noise-free pictures from being obtained. If a pre-amp or tuner is part of the AGC loop, gain reduction should be limited to the I.F. amplifier as much as possible, transferring gain reduction to the tuner only when the signal strength is high enough to cause distortion or cross modulation problems. The tuner gain will prevent the prior increase in I.F. amplifier N.F. from impacting the system noise performance, but excess system gain causing premature tuner gain reduction will increase the tuner N.F. and hence the system N.F.

Of great interest to us is the R.F.C/N ratio required for the detected output to be considered noise free. Actual television video S/N ratios are a little complicated by the fact that the displayed video signal does not occupy the full R.F. carrier envelope. 25% of the carrier is reserved for the synchronizing pulses and 12 ½% is retained even under conditions of peak white modulation, for the benefit of intercarrier sound detectors. A common definition of the video S/N ratio is the ratio measured in decibels of the peak video signal amplitude to the r.m.s. noise voltage amplitude. In this context peak video refers to the voltage excursion between black and white levels (from 75% peak carrier to 12½% peak carrier). With this definition in mind, it is generally accepted that the subjective effect of imperceptible noise occurs at an S/N ratio of 43 dB. Noise will become perceptible (for most viewers) at an S/N ratio around 38 dB; is clearly visible but not necessarily disturbing at 34 dB and becomes objectionable at 28 dB to 30 dB. Alternatively if we measure the signal amplitude as an r.m.s. sine wave with the same peak to peak amplitude as the R.F. carrier during the sync pulse period, our signal is free of noise for a 47 dB C/N ratio.



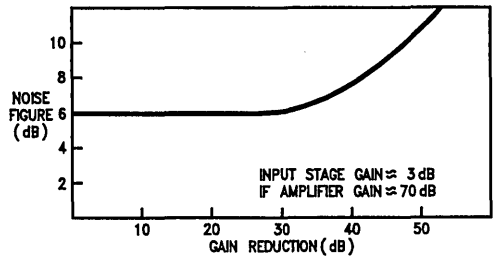
TL/H/8421-9

FIGURE 9. Television R.F. Modulation Envelope

If the input signal were completely noise-free (i.e. no excess noise from head-end amplifiers etc.) then the detected C/N ratio is determined by the equivalent input noise level of the tuner—2.2 uVrms for a 6 dB N.F. With a minimum signal level of 0.5 mVrms the detected C/N ratio will be 47 dB for the converter alone. When the actual signal has noise, for a cable C/N ratio of 43 dB the noise detected at the converter output is now

$$e_n = 10^{-6}\sqrt{(2.2)^2 + (3.5)^2} = 4.13\ \mu V$$

This gives a detected C/N ratio of 41.6 dB, a loss of 1.3 dB compared to the original signal. For most viewers this is the just perceptible level for video noise. On the other hand, if a 14 dB N.F. converter is used, the detected C/N is 32.7 dB which is considered objectionable. A 0 dBmV signal would produce 38.7 dB C/N ratio which would be acceptable. Obviously a low N.F. is important, and any increases in N.F. should be carefully controlled to get the best picture quality possible. *Figure 10* shows the change in N.F. for the LM1823 I.F. amplifier. For over 30 dB gain reduction, the N.F. is unchanged and increases by only 4 dB for the next 20 dB of gain reduction.



TL/H/8421-10

FIGURE 10. Increase in I.F. Amplifier N.F. with Gain Reduction

LM1823-GENERAL CIRCUIT DESCRIPTION

The basic arrangement of the LM1823 is shown in *Figure 11*. A five stage I.F. amplifier provides gain with a low impedance input stage to ensure adequate suppression of triple transit echo in SAW filters, and AGC on the three interstages. The output stage buffers the I.F. signal which is split off into two paths. A linear path takes the modulated signal to a true synchronous detector while a high gain limiter amplifier passes the I.F. carrier waveform to a second phase detector which is part of the PLL for the VCO. The PLL has an externally adjustable filter and locks the oscillator in quadrature with the incoming I.F. carrier. An in-phase component of the oscillator also drives the linear path detector to recover the signal amplitude modulation. An external DC control allows fine adjustment of the detection phase in order to optimize the detector linearity. The output from the detector is coupled back into the AGC comparator input, and is internally gated during the sync pulse period for good nose immunity and a fast response. Two AGC voltages are available; an early AGC for the I.F. amplifiers and a late, or delayed AGC for the tuner. The take-over point between the I.F. AGC and the tuner AGC is set by an external potentiometer. Also included is an AFT output for fine control of the tuner L.O. All these functions are contained in a 28-pin DIP with a pin-out designed to facilitate stable p.c.b. layouts—even with the high system gain of the LM1823 at frequencies up to 70 MHz.

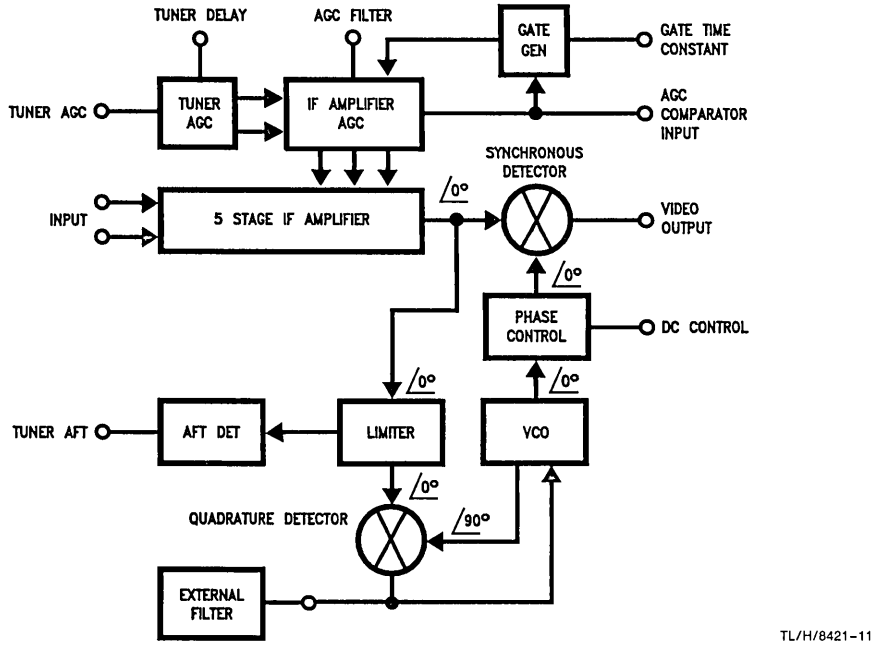


FIGURE 11. Block Diagram of the LM1823

I.F. Amplifier Stages:

The LM1823 I.F. amplifier is composed of five separate stages designed to provide high gain primarily in the frequency range of 35 MHz to 60 MHz, and gain control over a 60 dB range without overload of any stage and without introducing excess noise into the signal.

To achieve this, AGC is applied to the second through fourth stages by a control voltage that is either internally generated from the video detector output or from an externally applied bias voltage at Pin 13. AGC action starts when the voltage at Pin 13 reaches approximately 4 VDC and over 50 dB of gain reduction is obtained by the time Pin 13 voltage reaches 6.5 VDC. For a typical application, the I.F. noise figure is around 6 dB for the first 30 dB of gain reduction, and then begins to increase to above 10 dB by the time the amplifier is gain reduced over 50 dB (see *Figure 10*).

As mentioned earlier, the total system gain desired from the I.F. amplifier input to the video detector output needs to be selected for a specific set of tuner parameters and I.F. filter losses. Excess gain simply means premature AGC action with possible loss of optimum video S/N ratios. To see how and where the LM1823 gain can be adjusted, we will look at each gain stage in turn.

Input Stage:

The input stage is a common-base differential amplifier designed to give good rejection of unwanted I.F. output and detector VCO signals that may be radiated back to the input. The low input impedance of 60Ω ensures that SAW filters are terminated sufficiently to keep the TTE better than 40 dB below the signal level, even with low impedance SAWF's. Because it is a common base stage, the input stage gain is determined by the source impedance presented to the input. An approximate expression for the gain is given by Equation (1)

$$Av = 531/(Zs + 60) \quad (1)$$

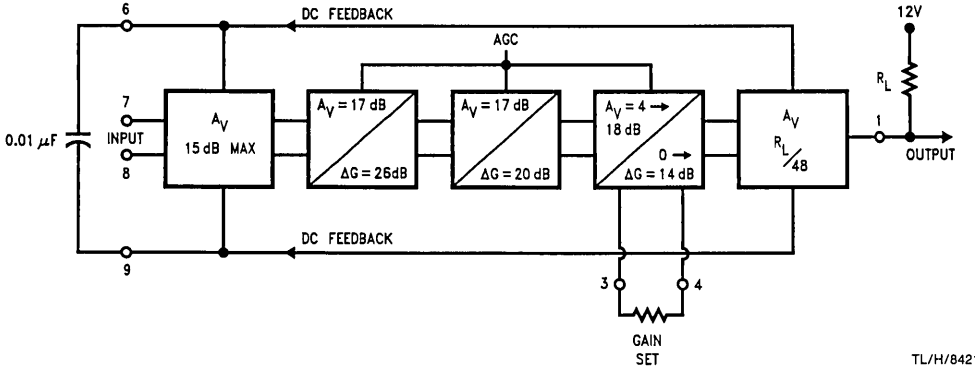
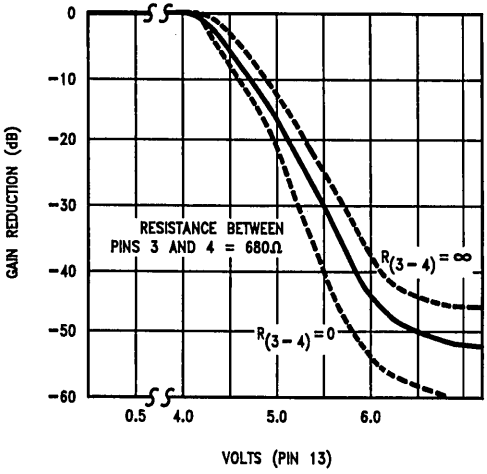


FIGURE 12. Gain Distribution in the I.F. Amplifier



TL/H/8421–13

FIGURE 13. I.F. Amplifier Gain Reduction Characteristic

As an example, if we use a high impedance SAW filter such as the Murata SAF45 MC series with an output impedance that can be modelled as a 2.8 kΩ resistor in parallel with 8 pF capacitance, our input Zs is 345Ω (including 2 pF input stray capacitance) at 45.75 MHz. From (1), the input stage gain is 2.4 dB. If a filter is used that matches to the input stage with 60Ω, then the gain can be as much as 13 dB.

A balanced input is extremely important since the input leads Pins 6–9 are the most sensitive parts in the system to unwanted I.F. coupling. For example, if the I.F. output couples into these pins it can cause changes in the frequency response and can easily promote oscillation. A spectrum analyzer is invaluable for helping determine the system susceptibility to this phenomenon. With the input terminated by the I.F. filter (or an equivalent resistor), the I.F. amplifier output noise spectrum will show if oscillation is likely to occur.

Another signal that can appear at the input is the detector local oscillator waveform. Unlike quasi-synchronous detectors, the LM1823 has a constant (and relatively high) oscillator signal for good linear detection, even with low input signal levels. It is the balance between the input pins to the VCO radiation pick-up that will determine whether the p.c.b. layout is good enough. VCO pick-up can cause AFC skewing and assymetrical oscillator pull-in, but probably the most serious effect is failure of the oscillator to acquire lock at weak signal levels. This is caused by the fact that the PLL phase detector sees two input frequencies—the desired I.F. and the undesired L.O. frequency. As a result the L.O. "chases itself" and is driven outside the loop acquisition range.

Again the spectrum analyzer is a useful tool for measuring the level of VCO pick-up and the degree of improvement that any circuit modification or component relocation makes. A good layout will have symmetrical input leads placed as close together as possible, shielded input coils (where used) and external components mounted as close to the I/C as possible. The DC feedback decoupling capacitor connected between Pins 6 & 9 should be right against the pins. The pcb layout shown later, even though it uses an I/C socket, is able to keep the equivalent VCO input level to under 2 uVrms. To put this number in perspective, it is −97 dB compared to the original VCO level. For the measurements, the spectrum analyzer should be connected through a FET probe at the I.F. output, which is disconnected from the detector stage. The VCO control pin is grounded, the detector input is de-coupled with a 0.01 uF capacitor to ground, and a reference signal CW of the order of 100 uVrms is applied at the filter input.

Second and Third Stages

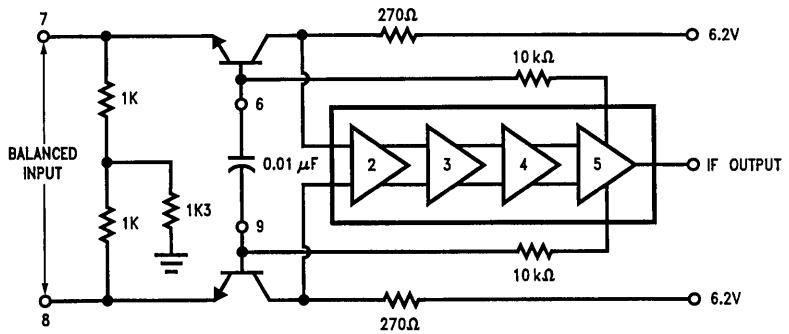
These are easy to handle since they are completely self contained within the LM1823. The maximum gain is fixed at 17 dB each with 26 dB and 20 dB of gain reduction capability respectively.

Fourth Stage

Unlike the preceding stages, the emitters of the fourth differential amplifier are available at Pins 3 & 4. An internal resistance of 1360Ω between these pins sets the minimum stage gain at 4 dB, and under these conditions (Pins 3 & 4 open) the stage does not provide significant gain reduction with AGC action. However, when an external resistor is connected between the emitters, the gain increases. For Pins 3 & 4 shorted together the gain is as much as 18 dB and the stage can provide up to 14 dB gain reduction with AGC action. Because of the way in which the total I.F. amplifier gain reduction is shared between the stages, the effective gain increase obtained by a resistor between Pins 3 & 4 occurs only for signals below the AGC threshold. After 20 dB of system gain reduction the fourth stage is fixed at 4 dB.

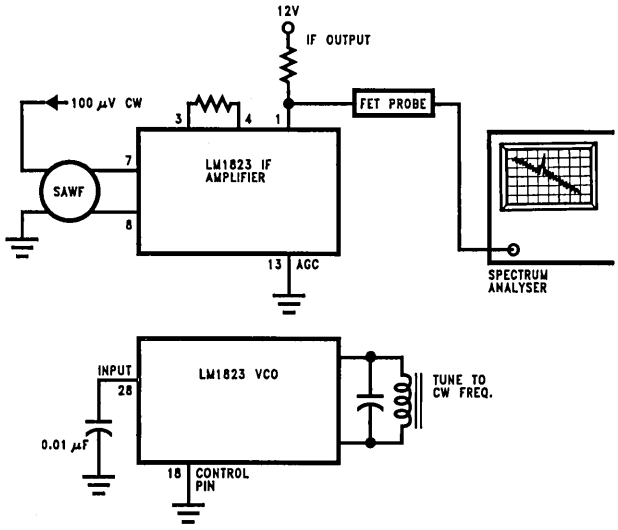
Fifth Stage and I.F. Amplifier Output

The fifth and final I.F. amplifier stage has a single-ended output. There is no internal connection to the detector stage, permitting convenient isolation of the IF amplifier and detector functions. Pin 1 is also a point at which any additional signal filtering may be applied. A resistive load con-



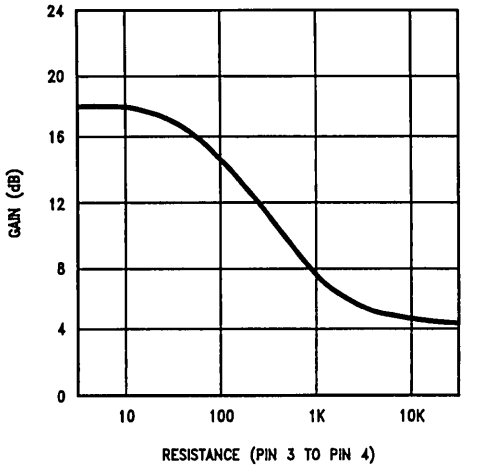
TL/H/8421–14

FIGURE 14. Low Impedance Common Base Input Stage



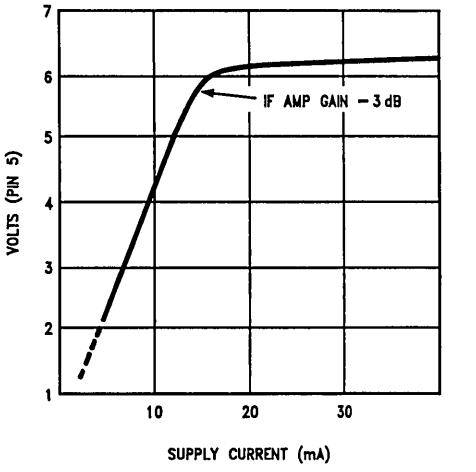
TL/H/8421–16

FIGURE 15. Checking the pcb for Excess VCO Pick-up



TL/H/8421–17

FIGURE 16. Fourth I.F. Amplifier Stage Gain with External Resistor



TL/H/8421–18

FIGURE 17. I.F. Amplifier Voltage Regulator Current Requirement

nected to the 12V power supply can be used, but the maximum value is limited in practice to less than 500Ω at intermediate frequencies because of stray p.c.b. capacitance and the loading of the detector stage input impedance of 3 kΩ. The stage gain for a total load impedance of Z is given by Equation (2)

$$AV = 1Z1/48 \quad (2)$$

The last part of the I.F. amplifier concerns the power supply input at Pin 5. This is a shunt regulated input with a nominal value of 6.3V and the I.F. amplifier current is delivered through a dropping resistor from the 12V rail supplying the remainder of the I/C. The 0.01 μF ceramic r.f. decoupling capacitor at Pin 5 should be grounded through very short leads—preferably on the copper side of the p.c.b. A nominal current level into Pin 5 is 32 mA, set by a 180Ω resistor. This current should not exceed 60 mA and the minimum current is about 20 mA, below which the I.F. amplifier will start to lose gain as Pin 5 voltage drops below the regulated level.

SELECTING THE I.F. GAIN

Clearly the LM1823, with all the gain provided by five I.F. amplifier stages and with 34 dB detector conversion gain, has a more than adequate gain margin to provide signal sensitivity and compensate for interstage filter losses. To show how this gain may be distributed we can look at a first cut design example.

2

If we continue with the 30 dB gain tuner with a 6 dB N.F., using the tuner 75Ω output to misterminate the SAWF input will produce a very high insertion loss for the filter. This can easily be over 30 dB but before using the LM1823 gain capability to compensate for this loss, we must look at another aspect of filter insertion loss—the N.F. goes up Previously we assumed that the tuner N.F. will dominate the system N.F.—and with a tuner amplifier N.F. of 6 dB and 30 dB gain this is indeed true. But when the I.F. amplifier and SAWF are combined the N.F. for the combination exceeds 30 dB. This degrades the system N.F. to 7 dB* and after 50 dB of I.F. amplifier gain reduction the N.F. will be over 8 dB. Frequently this will be alright but it is instructive to consider improving the SAWF N.F. by matching the tuner output impedance to the filter or using an impedance matching pre-amp. For example, the 10 dB gain pre-amp shown in *Figure 18* has a 4 dB N.F. and reduces the filter loss to less than 20 dB. After 50 dB I.F. amplifier gain reduction, the combined N.F. is only 27 dB—for a worst case system N.F. of 6.6 dB. In a dual conversion system with a diode mixer (and already high N.F.), some gain *must* be provided prior to the SAWF.

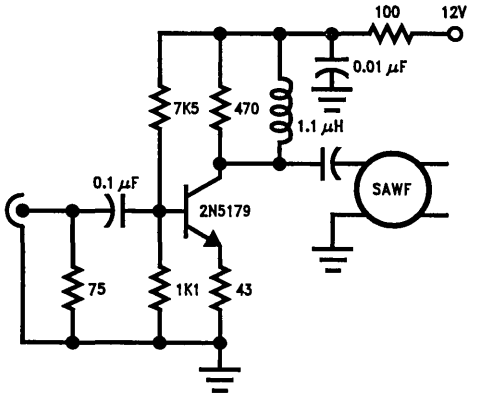
$$*NF_{system} = NF_{tuner} + \frac{NF_{IF}}{(\text{Tuner Gain})}$$

Leaving a 10 dB gain margin over that required to raise a −6 dBmV signal to the rated detector output, the total gain requirement of the I.F. amplifier is

75.6 dB − 30 dB + 30 dB − 34 dB + 10 dB = 51.6 dB

(0.5 mV ⟶ 3V) (tuner) (SAWF) (detector) (gain margin)

(With a 10 dB gain impedance matching amplifier between the tuner and the SAWF, the gain requirement falls by 20 dB to 31.6 dB.) To avoid overload in the high gain tuner, we probably have to start gain reducing the tuner when the input signal reaches +10 dBmV (but certainly not before 0 dBmV in order to preserve the tuner NF) so that the I.F. AGC range requirement is approximately 26 dB. This amount of AGC range can be obtained without a resistor connected between Pins 4 & 5 putting the fourth stage gain



TL/H/8421–19

FIGURE 18. Impedance Matching Pre-amplifier

at 4 dB. The SAWF impedance sets the input stage gain at 3 dB for a total of 41 dB to the input of the final stage. A 180Ω resistor at Pin 1 gives the desired last stage gain of 11 dB, or this resistor is reduced to 50Ω and a 10 dB pad is inserted between the I.F. amplifier output and the detector input when a pre-amp is used.

LM1823 VIDEO DETECTOR

The second major function of the LM1823 is the video detector stage, including the AFT/AFC detector and AGC detector/amplifier.

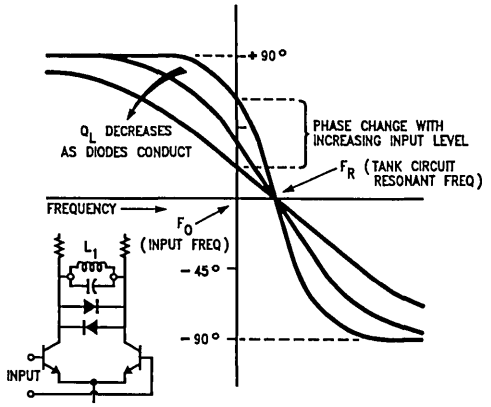
The video detector stage of the LM1823 has a fixed conversion gain of 34 dB—giving a 60 Vrms input level for a 3V (o–p) detected output. This input level is required for AGC action to commence and is well below the input level that can cause intermodulation or catastrophic overload.

Synchronous detection of an amplitude modulated carrier involves a source of constant amplitude CW with the same frequency as the signal carrier, and two phase detectors. One detector is operated in quadrature—i.e. the CW phase and the signal carrier phase have a 90 degree difference at the inputs to the phase detector. This detector operates solely to keep the CW source phase-locked to the signal carrier. The second phase detector has synchronous or in-phase inputs so that the detector output responds to the amplitude difference between the inputs and therefore tracks the signal amplitude modulation.

The benefits of synchronous detection over envelope detection are well known, and most modern receivers incorporate a type of detector known as a quasi-synchronous detector, which is a signal amplitude detector. The I.F. signal is amplified and stripped of modulation in order to be used as the detector CW. The disadvantages of this type of detector are the loss of linearity at very low signal inputs (corresponding to peak video modulation) and a fundamental compromise in the bandwidth of the limiter stage used to strip the modulation. To maintain ease of tuning and a relative immunity from center frequency drift caused by temperature changes and aging, the limiter bandwidth is sufficiently wide that the resulting CW is phase modulated by the information on the original I.F. carrier. Since this can generate intermodulation products, a high Q is desirable and a trade-off in ease of alignment occurs.

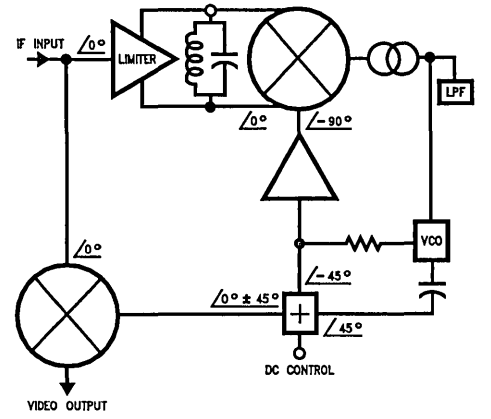
A less obvious problem with this type of detector is the actual static detection phase that is being regenerated. Internal I/C related phase shifts cause the limited carrier waveform applied to the detector to be more or less than 0 degrees phase-shifted with respect to the signal carrier phase. A loss in detector efficiency results, but if the limiter tuning is adjusted to compensate for this, the CW phase from the limiter will depend on the drive to the limiter. The detection phase then changes with amplitude modulation of the original I.F. carrier. The effect of this is observed primarily as differential phase in the chroma subcarrier signal and increased levels of sound buzz. Although, as discussed later, the desired phase difference between the detector CW and signal carrier is not necessarily 0 degrees, the limiter tuning cannot be used to correct the amplitude modulation detector phase—the limiter must be center tuned to avoid carrier phase shifts with modulation level.

The LM1823 overcomes these problems by providing a true synchronous detector system, which, as the block diagram shows, comprises of an internal VCO and in-phase and quadrature phase detectors. The incoming signal from the



TL/H/8421-20

FIGURE 19. Limited I.F. Carrier Phase Shifts with Input Amplitude when the Limiter Tank is Mistuned

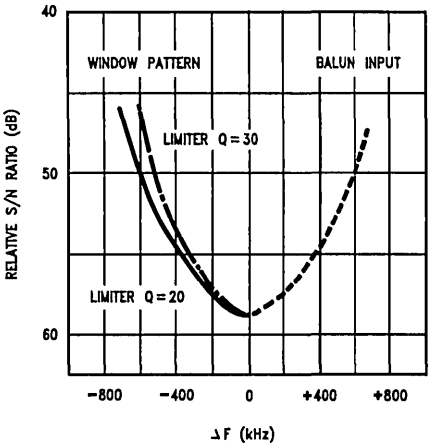


TL/H/8421-21

FIGURE 20. LM1823 Synchronous Detector and DC Controlled Detection Phase

I.F. amplifier is split into two paths. One path is through a high gain limiter stage which strips the amplitude modulation from the CW and applies it to one input of the quadrature phase detector. The other detector input is from the VCO and, once synchronized to the intermediate frequency, if the VCO phase deviates from a 90 degree relationship with the limiter CW phase, a control current is generated by the phase detector and is filtered at Pin 18 to correct the VCO. Even though the limiter stage tuned circuit faces the same compromises of desired narrow bandwidth versus ease and stability of tuning, the filter at Pin 18 can be made to have a very narrow bandwidth. Therefore the VCO can provide a reference signal to the phase detectors with a high degree of spectral purity. The second path for the I.F. signal is directly to the in-phase detector. The VCO output passes through a DC voltage controlled phase shifter before being applied to this detector. The DC phase shifter allows precise adjustment of the synchronized VCO phase for maximum amplitude modulation detection efficiency, and compensates for any internal I/C phase shift variations. At the same time, proper center-tuning of the limiter coil is possible.

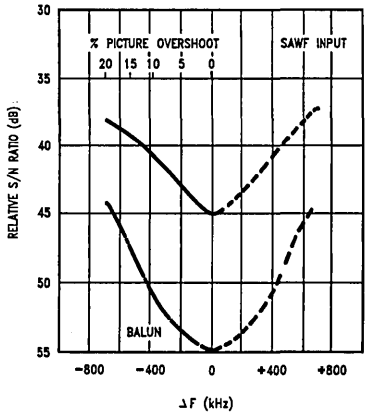
The benefits of center-tuning the limiter are clearly shown by comparing the differential chroma phase of the LM1823



TL/H/8421-22

FIGURE 21. Relative S/N Ratio with Limiter Tuning (No SAWF)

with a conventional quasi-synchronous detector. The LM1823 can consistently produce DP'S of under 1 degree compared with up to 10 degrees for a quasi-synchronous detector. There is also a substantial improvement in the sound carrier S/N ratio. When the limiter is detuned to compensate for internal I/C phase shifts or for detection phase-lags to produce video overshoots (for a subjectively crisper picture), the S/N ratio degrades by 5 dB to 7 dB, depending on the video modulating signal.



TL/H/8421-23

FIGURE 22. Effect of Limiter Retuning with SAWF

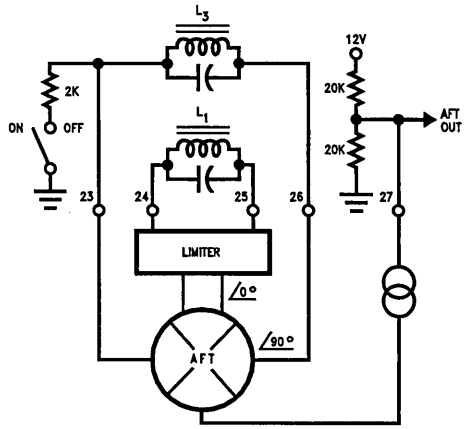
THE LIMITER

The limiter tuned circuit at Pins 24 and 25 is driven by a differential stage with a 6.6 kΩ internal load impedance. A small signal gain of 50 (with a tuned circuit dynamic resistance of 8 KΩ) ensures that full quadrature detector efficiency is obtained with input levels above 10 mVrms, and internal Schottky diodes limit the maximum amplitude at Pins 24 and 25 to about 500 mV (p-p). Tuning is achieved either for a peak amplitude signal measured with an F.E.T. probe (low

capacitance) at Pin 24 or Pin 25 with a 10 mVrms CW input, or by monitoring the video detector and adjusting for minimum differential chroma subcarrier phase. The latter adjustment will require a signal source modulated with a chroma/video ramp or stair-step pattern including a 20 IRE level chroma subcarrier, but does have the advantage that the adjustment can be made at strong signal levels, and does not require dis-connection of the tuner.

AFT/AFC CIRCUIT

The AFT phase detector is a doubly-balanced phase detector with the switching signal provided internally from the limiter stage described previously. The quadrature signal input is obtained by light external capacitative coupling from the limiter tuned circuit to the AFT tuned circuit at Pins 23 and 26. Parallel p.c.b. tracks to the limiter and AFT coils will usually provide sufficient coupling and the 1 pF capacitors on the LM1823 test circuit (see LM1823 data sheet) are shown only to illustrate the level of coupling involved. Since the AFT tuned circuit is driving an amplifier with a differential input resistance of 20 kΩ, it is able to operate close to the unloaded Q of the inductor.

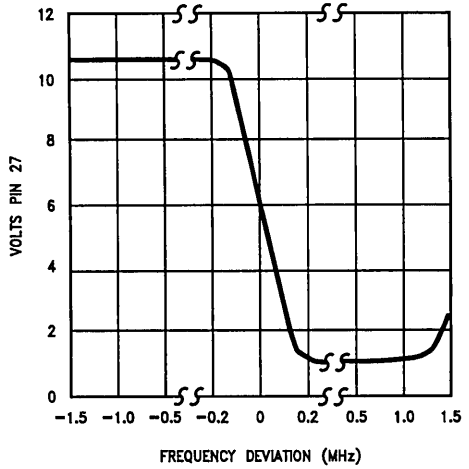


TL/H/8421–24

FIGURE 23. AFT Circuit with pcb Coupling Between the Limiter & AFT Tuned Circuits

The AFT output Pin 27 is driven from a current source so that the output voltage at the proper center frequency is set by an external resistive divider network. The parallel resistance of this divider will determine the voltage swing obtained for a given frequency deviation and in combination with the AFT tuned circuit Q, provides a means to adjust the AFT output slope.

Once outside the desired tuning range the AFT output voltage should stay either close to ground (I.F. frequency high) or close to the positive supply voltage (I.F. frequency low). If the voltage moves back towards the center voltage as the signal moves further away from the desired tuning range, then more coupling from the limiter tank may be needed. Grounding Pin 26 through a 2 kΩ resistor will defeat the AFT circuit for receiver fine-tuning purposes. The 2 kΩ provides isolation of the AFT switch & associated cable from the tuned circuit which has a relatively low dynamic resistance of 1.8 kΩ. Resistor values larger than 2 kΩ may prevent the circuit from being defeated, but either Pin 23 or Pin 26 can be grounded directly without damaging the I/C.



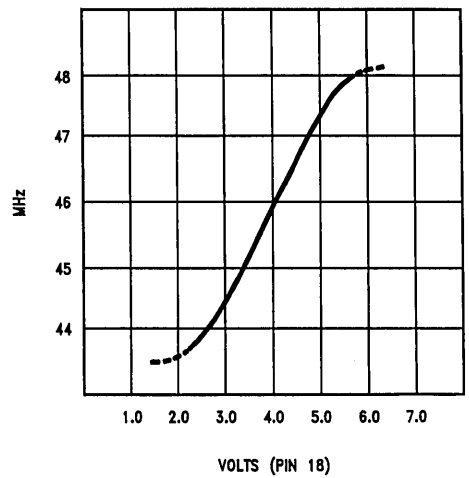
TL/H/8421–25

FIGURE 24. AFT Circuit Output Voltage Characteristic (RLOAD at Pin 27 = 10 kΩ)

THE PHASE LOCKED LOOP (PLL)

For true synchronous operation the LM1823 has an internal VCO operating at the video intermediate frequency of 45.75 MHz.

A parallel tuned circuit between Pins 19 and 20 will set the oscillator free-running center frequency and the tuned circuit dynamic resistance is loaded by an internal 1.5 kΩ resistor. Since the oscillator frequency must be controlled, a basic tradeoff exists between oscillator stability, control sensitivity and control range. To obtain a control range of over 2 MHz, the working Q of the tuned circuit should be around 15. Increasing the Q by raising the capacitative arm of the tuned circuit will improve the oscillator stability. This reduces the change in free-running frequency as a result of temperature effects etc. The control sensitivity will decrease correspondingly and there will be a reduction in the control range. The control range in the application circuit has been chosen to cover the expected deviations in the I.F. carrier that are allowed by AFT circuits. With a coil unloaded Qu of



TL/H/8421–26

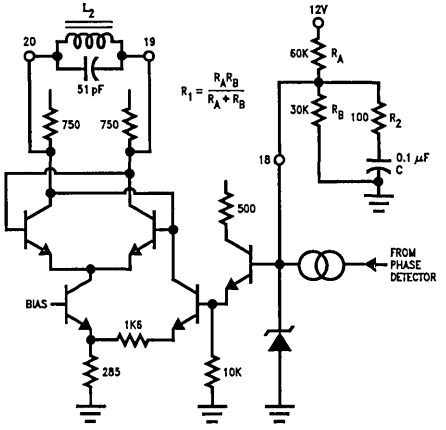
FIGURE 25. VCO Control Sensitivity Characteristic

55, and a working Q of 15, the inductance should be 0.24 uH, which tunes with 51 pF at 45.75 MHz.

The V.C.O. frequency is adjusted by injecting a 60 mVrms CW at Pin 28. If the VCO tuning (L_3) is a long way from being correct, the detector output Pin 16 will show an AC signal of about 4V (p-p) centered around 7.5 VDC. As the oscillator is tuned toward the correct frequency the AC beat note will decrease and abruptly disappear as the oscillator locks to the carrier frequency. Final adjustment of the VCO is done by tuning L_3 until the voltage at the phase detector filter Pin 18 is 4 VDC.

Oscillator control is accomplished by internally phase shifting the currents in a direct cross-coupled differential stage in response to the control voltage developed at Pin 18. Direct cross-coupling of the bases and collectors of this differential stage means that the transistors are operating in a soft-saturated mode, enabling a constant output amplitude to be obtained of about 500 mV (p-p). This output amplitude does not change with coil tuning or over the frequency control range of the oscillator. With the specified tuning components at Pins 19 and 20, the VCO sensitivity is 1.5 MHz/volt. Other general characteristics of the VCO are a negative temperature coefficient of 150 ppm/degree C, and a tendency for the oscillator control sensitivity to decrease with decreasing frequency of operation (below 10 MHz).

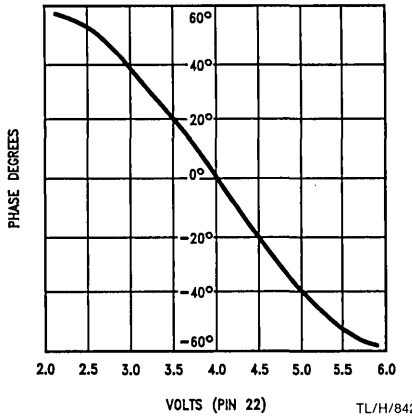
The VCO tuning components are mounted across the I/C package from the I.F. amplifier input. This minimizes inductive coupling and yields approximately 105 dB isolation for the I/C alone. Leads and components connected to the I.F. amplifier input will reduce the VCO isolation (as will higher operating frequencies).



TL/H/8421-27

FIGURE 26. LM1823 VCO Circuit

The quadrature phase detector output is a push-pull current source so that the control voltage at Pin 18 is determined by the parallel resistance of the external divider network, which also sets the quiescent control voltage in the absence of an I.F. signal. This divider voltage should be centered at 4 VDC since the lower voltage swing for controlling the oscillator frequency is 2 VDC, and an internal clamp prevents Pin 18 increasing above 5.6 VDC. By using a 20 kΩ parallel resistance at Pin 18, the phase detector current of 7.5 uA/degree gives a phase detector sensitivity (μ) of 0.15 volts/degree. This parallel resistance is equivalent to R1 in the conventional filter for a 2nd order PLL. The oscillator and phase detector sensitivities given above yield a DC loop gain of 12.9 MHz/radian. For the data sheet value of 100Ω for R2, and a filter capacitor of 0.1 uF, the loop damping factor (K) is 1.01 and the natural resonant frequency (w) is 32 kHz. From this we can calculate that the loop −3 dB bandwidth is 73 kHz which is substantially less than would be practicable with a quasi-synchronous detection system, and this brings the desired benefits of low luma/sound/chroma crosstalk and freedom from quadrature distortion produced by the I.F. filter slope characteristic in the vicinity of the picture carrier frequency. Nevertheless, some signal conditions may cause wider PLL bandwidths to be used. A probable problem is incidental carrier phase modulation (ICPM).



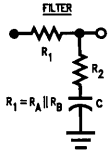
TL/H/8421-28

FIGURE 27. DC Controlled Phase Shifter Characteristic

This describes the shift in carrier phase as the modulation depth changes, and is particularly likely to happen where prior processing of the original carrier waveform has occurred—in distribution or conversion amplifiers employed in MATV and cable systems for example. It is also present to an extent in broadcast transmitters and if the PLL loop bandwidth is too narrow for the VCO to track this phase shift, then the ICPM is transferred to the signal modulation. This can be observed as a tint shift in color bars or a smear

PHASE LOCKED LOOP PARAMETERS

FILTER



$R_1 = R_A \| R_B$

VCO SENSITIVITY (β) = 1.5 MHz/VOLT

PHASE DETECTOR SENSITIVITY (μ) = 0.15V/DEGREE

DC LOOP GAIN ($\mu\beta$) = $^{W_C}/_{2\pi}$

LOOP NATURAL FREQUENCY (F_n) = $^{W_n}/_{2\pi}$

$$W_n = \sqrt{\frac{W_c}{C(R_1 + R_2)}}$$

LOOP DAMPING FACTOR (K) $\approx \frac{R_2}{2}\sqrt{\frac{CW_c}{R_1}}$

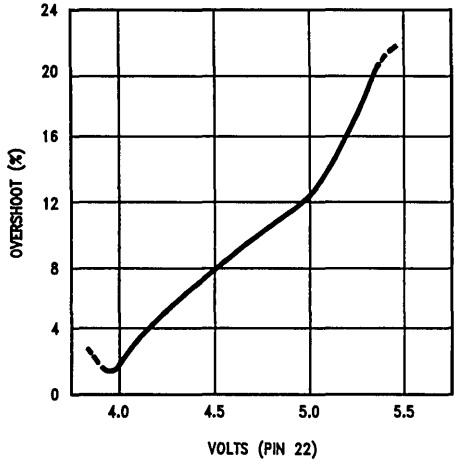
LOOP −3dB FREQUENCY = $^{W_n}/_{2\pi}\left[2K^2 + 1 + \sqrt{(2K^2+1)^2 + 1}\right]^{1/2} \approx \frac{W_n 2K}{\pi}$ (K > 2)

	$R_2 = 100\Omega$	$R_2 = 680\Omega$
$W_c = 81 \times 10^6$ RADS/SEC	K = 1.01	K = 69
$W_n = 2 \times 10^5$ RADS/SEC	$F_{3dB} = 56$ KHz	$F_{3dB} = 440$ KHz

TL/H/8421-29

in the leading edge of a color bar as the VCO belatedly attempts to track the phase change. For these types of signals it is desirable to increase the loop bandwidth to about 500 kHz—changing R2 to 680Ω is an easy fix. The loop damping factor is kept greater than 1 to avoid ringing on the phase transients. Larger loop bandwidths will increase the possibility of luma/sound/chroma crosstalk.

Once the VCO is locked in phase to the I.F. signal, the DC phase shifter Pin 22 is normally around 4 VDC for peak detector efficiency. Usually some extra phase lag will be introduced since a subjectively crisper picture is obtained if picture transients have an overshoot. Between 12% and 20% overshoot without ringing is desirable, corresponding to a 400 mV to 800 mV shift in Pin 22 voltage.



TL/H/8421-30

FIGURE 28. Signal Overshoot Produced by Carrier Detection Phase Shift

VIDEO DETECTOR POST AMPLIFIER

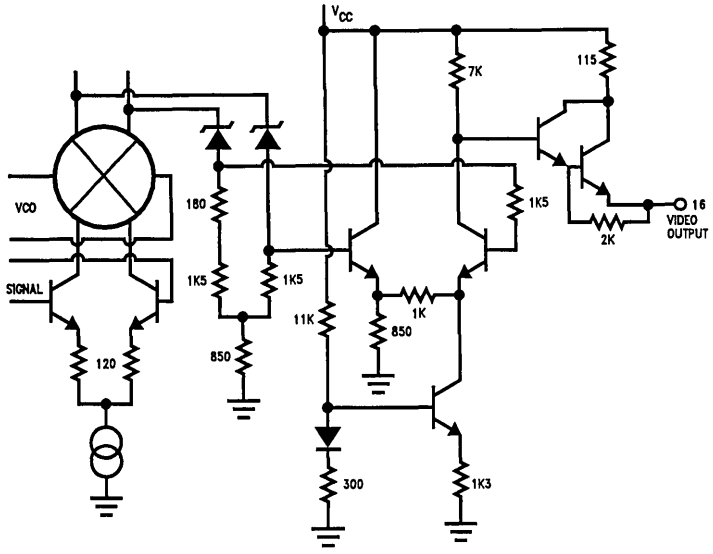
The response of the video amplifier is rolled off above 9 MHz to minimize the amount of the VCO waveform and its harmonics appearing in the output at Pin 16. Typical oscillator products are 40 dB below the desired signal level.

Zener diodes are used in the video amplifiers for level shifting so that the use of PNP transistors is avoided and the detector linearity is preserved. Excellent differential gain characteristics are obtained—typically less than 3%. Pin 16 is a Darlington NPN emitter follower output. With no detector CW input signal, Pin 16 is at 7.6 VDC, representing zero carrier level which is slightly higher than peak white (by 12½%). As the CW input increases, Pin 16 voltage decreases towards black level with the sync pulses producing the most negative detector level.

The level reached by the sync tips is determined by the AGC loop threshold and if the internal AGC comparator is used (Pin 16 is directly connected to Pin 17), the sync tips will be clamped at 4 VDC. This produces a nominal detector output of 3.2V (p-p) but this is subject to variations in the Pin 16 detected zero carrier level. The resistive network shown connected between Pin 16 and Pin 17 in *Figure 30* can be used to change the zero carrier level at Pin 17 for an adjustable recovered video level. For best performance the recovered video level should never be less than 1V (p-p) or greater than 4V (p-p). In suppressed sync systems, the recovered video at Pin 16 is routed to the descrambler for restoration of the sync amplitude before it is applied to Pin 17. Obviously the signal DC content must be preserved through the descrambler if proper AGC action is to be maintained.

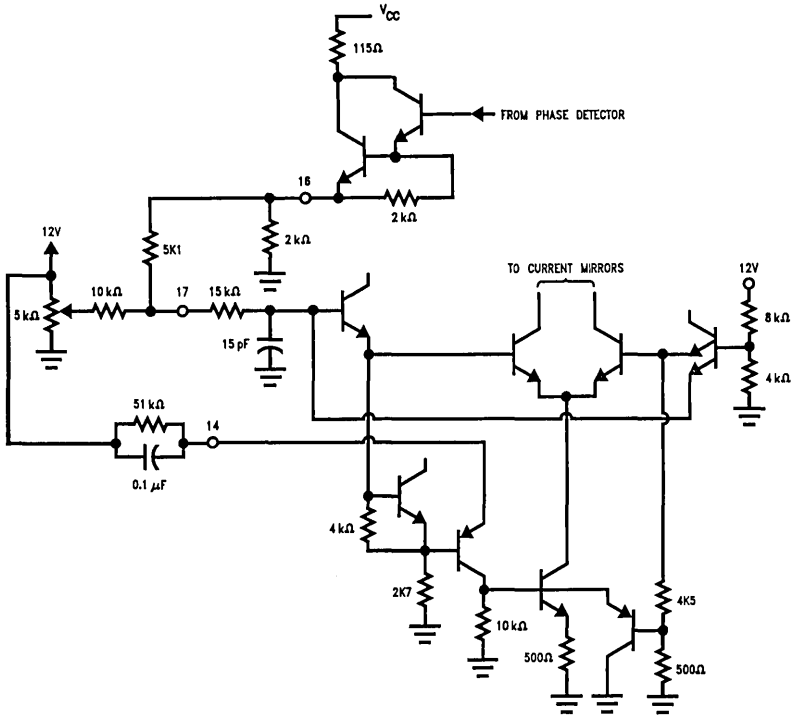
AGC Self Gating Comparator (LM1823)

The AGC comparator input has a low pass filter to protect the AGC loop from noise interference. Conventional detector systems often use noise gates to prevent the AGC system "backing off" on noise peaks that occur below the sync tip level. It is difficult to set the noise gate threshold close enough to the sync tip level for it to provide any benefit without risking AGC lock-out. For the LM1823 however, syn-



TL/H/8421-31

FIGURE 29. LM1823 Detector and Video Amplifier



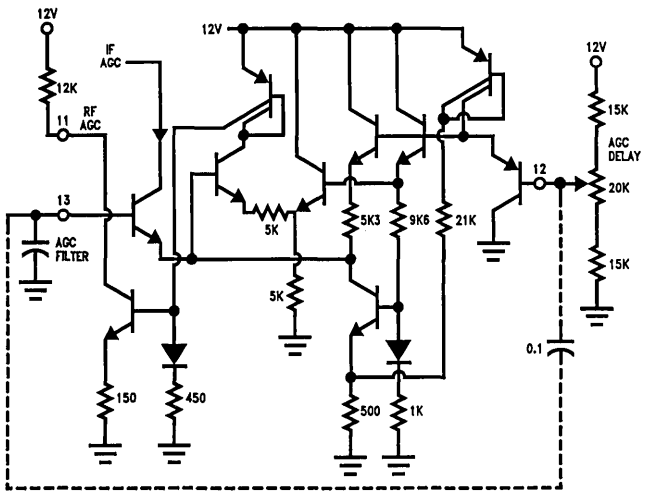
TL/H/8421–32

FIGURE 30. LM1823 Self Gating AGC Comparator

chronous detection allows the noise gate to be eliminated. Since the noise is random phase, the synchronous detector will not rectify the noise voltage and the low pass filter can average out the noise input to the comparator.

Further protection of the AGC comparator is provided by gating the comparator on only during the sync pulse period. The gate pulse is obtained from the input video waveform sync pulses at Pin 16. Essentially an emitter coupled sync stripper circuit, the slice level is set by an external time constant at Pin 14. During the sync pulse period the capacitor at Pin 14 is being charged toward ground potential and the comparator is gated on. Between sync pulses the capacitor discharges towards the positive supply voltage through the resistor and the comparator is off. The sync slice level is determined by the Pin 14 RC time constant and is given in Equation (3) as the number of millivolts the slice level is above the sync tip voltage.

$$V\ SLICE = 1/2\ RC\ (mV) \qquad (3)$$



TL/H/8421–33

FIGURE 31. RF AGC Amplifier

A typical slice level for a 3V (o–p) video signal is between 100 mV and 250 mV. Different slice levels can be obtained with other capacitor values (the resistor should be left unchanged). Small capacitors will allow a faster response to a fluctuating sync tip level but also may cause the consequently deeper slice to include video overshoots.

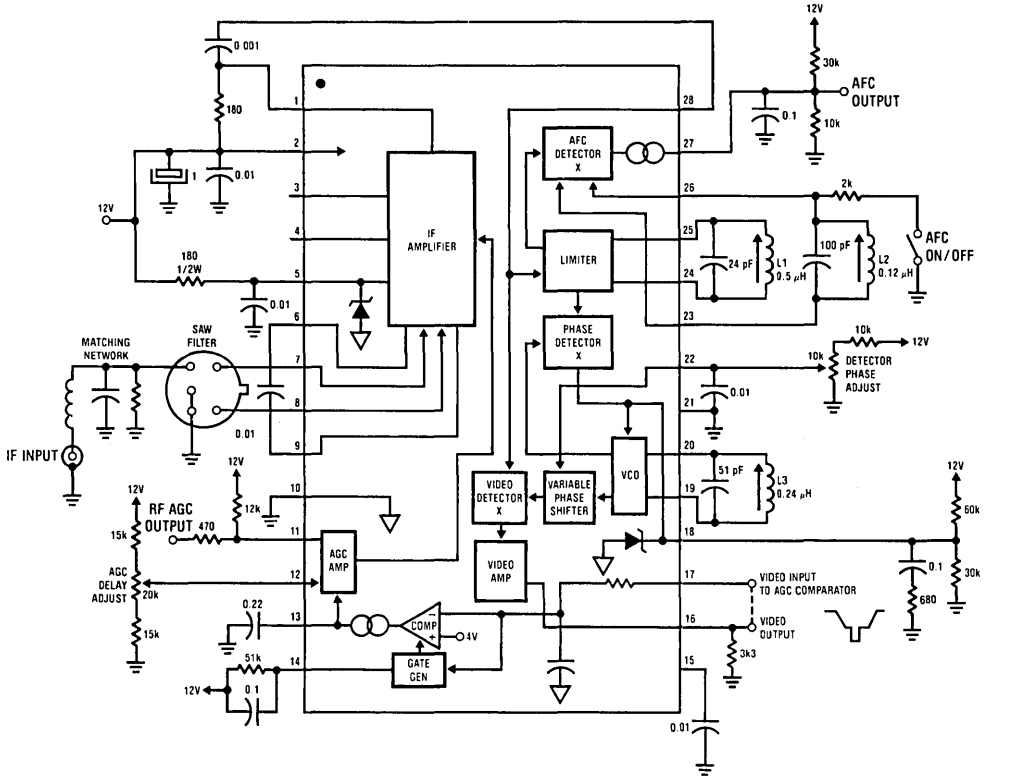
RE AGC DELAY AND OUTPUT AMPLIFIER

The I.F. amplifier is at full gain below 4 VDC on Pin 13. At anywhere from 5.5 VDC to 6.5 VDC we will want to shift gain control into the R.F. stages, and this is accomplished by a delayed AGC threshold control at Pin 12. When the filter voltage on Pin 13 is 0.7V above the pre-set level on Pin 12, the R.F. AGC amplifier at Pin 11 will start to sink current.

The capacitor shown connected between Pins 12 and 13 is optional and intended to provide an increase in AGC action for signal amplitude transients at high R.F. signal levels (tuner in gain reduction). AC changes on Pin 13 are coupled to the threshold level control allowing the I.F. amplifier to gain reduce (or increase) during the signal transient. This happens only during the signal change, so that the detected video returns more rapidly to the proper output levels. Once signal equilibrium is restored, the appropriate gain balance between the R.F. and I.F. amplifiers returns.

CONCLUSION

This note has described a high quality video I.F. amplifier/detector combination that can provide excellent baseband video signals. A complete schematic of the external components required in such an application is shown in *Figure 32*, with a suitable p.c.b. layout in *Figure 33*.



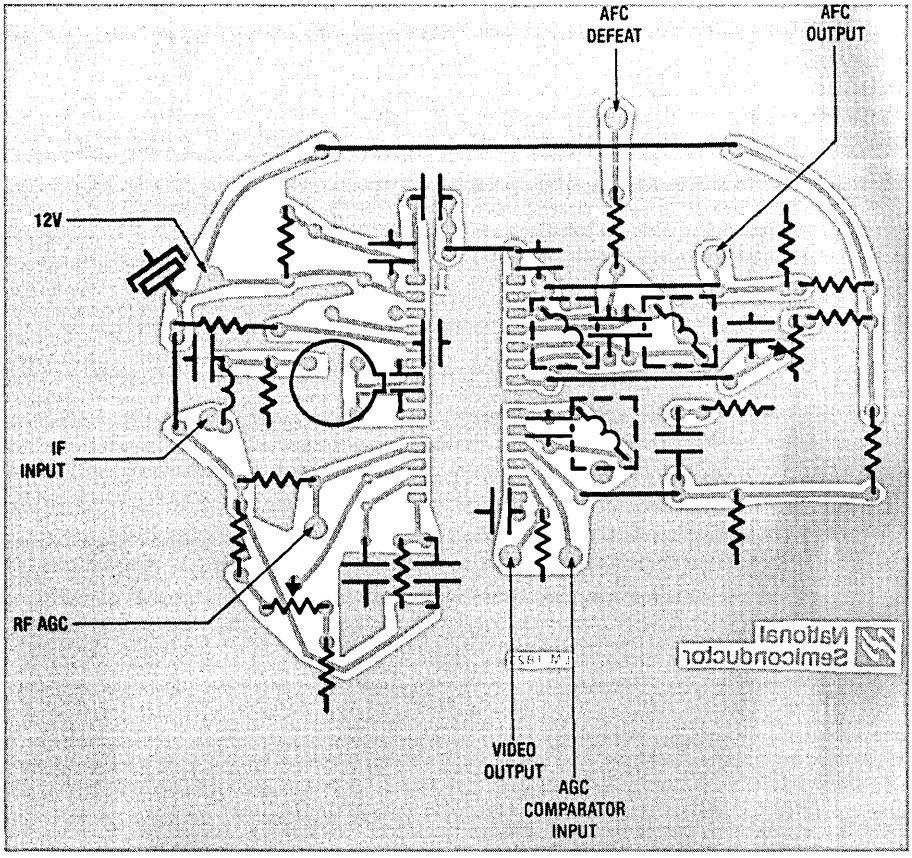
TL/H/8421–34

SAW Filter-MuRata SAF45MC/MA

L1-9 ½T } #22 wire
L2-4 ½T } on 3.16" form with
L3-6 ½T } HF core, shielded

All caps in uF unless noted

FIGURE 32. LM1823 External Circuit Components



TL/H/8421–35

FIGURE 33. LM1823 Printed Circuit Board Layout (Component Side)

LM2889 R.F. Modulator

National Semiconductor
Application Note 402
Martin Giles

Introduction

Two I/C RF modulators are available that have been especially designed to convert a suitable baseband video and audio signal up to a low VHF modulated carrier (Channel 2 through 6 in the U.S., and 1 through 3 in Japan). These are the LM1889 and LM2889. Both I/C's are identical regarding the R.F. modulation function—including pin-outs—and can provide either of two R.F. carriers with dc switch selection of the desired carrier frequency. The LM1889 includes a crystal controlled chroma subcarrier oscillator and balanced modulators for encoding (R-Y) and (B-Y) or (U) and (V) color difference signals. A sound intercarrier frequency L-C oscillator is modulated using an external varactor diode. The LM2889 replaces the chroma subcarrier function of the LM1889 with a video dc restoration clamp and an internally frequency modulated sound intercarrier oscillator.

Modulation Parameters

In the U.S., either of two R.F. channels is made available so that the user can select a vacant channel allocation in his geographic area, thus avoiding co-channel problems with older receivers that have inadequate shielding between the antenna input and the tuner.

The characteristics of the R.F. signal are loosely regulated by the FCC under part 15, subpart H. Basically the signal can occupy the standard T.V. channel bandwidth of 6 MHz, and any spurious (or otherwise) frequency components more than 3 MHz away from the channel limits must be suppressed by more than −30 dB from the peak carrier level. The peak carrier power is limited to 3 mVrms in 75Ω or 6 mVrms in 300Ω, and the R.F. signal must be hard-wired to the receiver through a cable. Most receivers are able to provide noise-free pictures when the antenna signal level exceeds 1 mVrms and so our goal will be to have an R.F. output level above 1 mVrms but less than 3 mVrms. Since the distance from the converter to the receiver is usually only a few feet, cable attenuation will rarely be a problem, but mis-termination can change both the amplitude and relative frequency characteristics of the signal.

The standard T.V. channel spectrum has a picture carrier located 1.25 MHz from the lower band edge. This carrier is amplitude modulated by the video and sync signal. In the

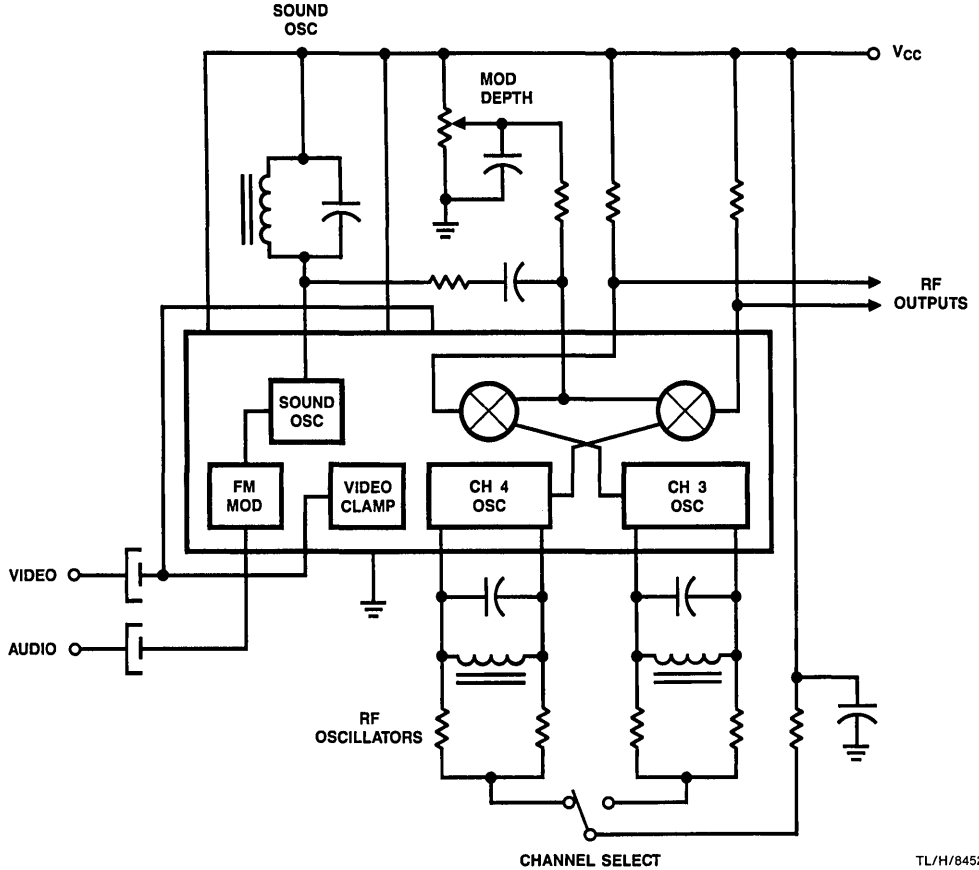


FIGURE 1. The LM2889 Block Diagram With External Components

Modulation Parameters (Continued)

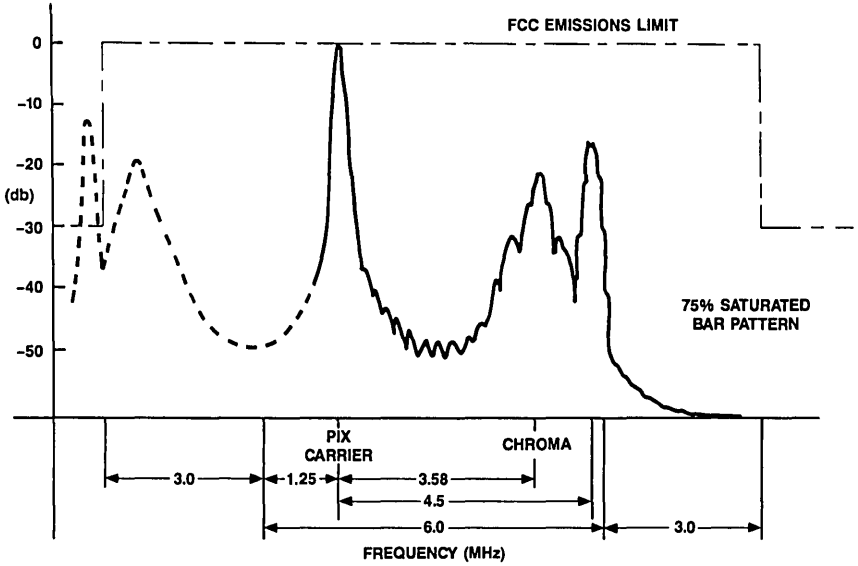


FIGURE 2. Television Channel R.F. Spectrum

case of a color signal, a second subcarrier is added 3.58 MHz above the picture carrier. The sound or aural carrier is 4.5 MHz above the picture carrier and is frequency modulated with the audio signal to a peak deviation of 25 kHz. This audio signal has pre-emphasis above 2.1 kHz (a 75 μs time constant). Similar modulation methods and standards are used in Japan and Europe.

With the picture carrier located near one end of the channel bandwidth, most of the available spectrum is used by the upper sideband modulation components. Only modulating frequencies within 0.75 MHz of the carrier frequency are transmitted double sideband and the lower sideband is truncated by at least −20 dB compared to the peak carrier level by the time the lower channel edge is reached. This is referred to as Vestigial Sideband (VSB) modulation and since most R.F. modulators are double sideband, a VSB filter is used at the transmitter output. A filter is needed for each channel and consists of bandpass and harmonic filter sections. A broadcast transmitter uses a separate modulator for the sound carrier and this is added to the picture carrier via a diplexer before reaching the transmitting antenna. Close control is maintained on the picture and sound carrier frequencies to keep a 4.5 MHz spacing between them. This tight frequency control is used to advantage by the majority of television receivers which employ intercarrier sound circuits. The I.F. amplifier processes both the pix and sound I.F. carriers and detects the 4.5 MHz difference frequency at the video detector stage. This frequency modulated sound intercarrier is then stripped of amplitude modulation by a high gain limiter circuit and a quadrature demodulator recovers the audio.

The LM1889 and LM2889 use a slightly different modulation scheme to that described above for several reasons. For circuit economy L-C oscillators are used to generate the pix

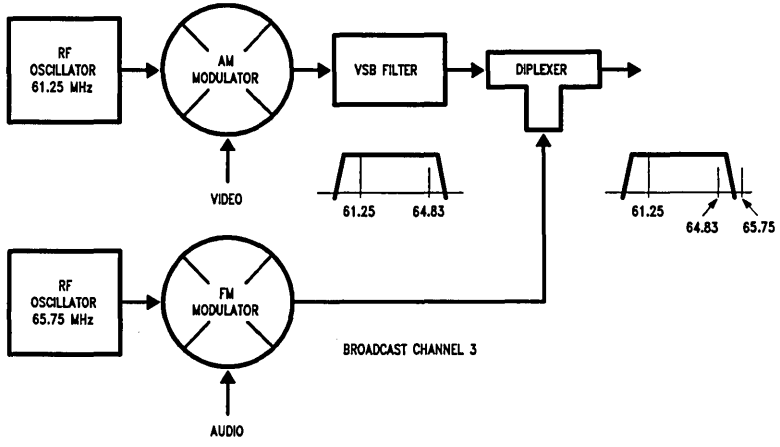


FIGURE 3. Broadcast Transmitter Block Diagram

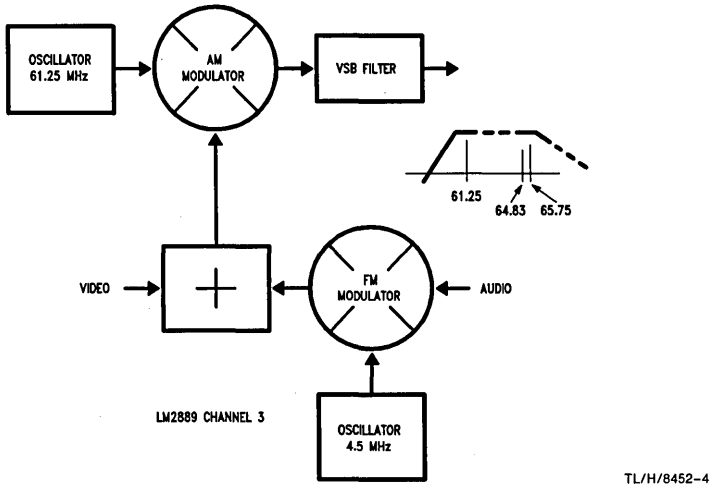


FIGURE 4. LM1889/2889 Sound and Video Modulation

carrier frequencies. The stability of such oscillators is good enough for the AFT circuits in modern receivers to maintain picture quality, but if a separate L-C sound carrier oscillator were used, the relative drift of the two carrier frequencies would be much too great for intercarrier sound receivers. For example, a typical television sound circuit tuned to 4.5 MHz will generate as much as 3% distortion if the difference between the R.F. carriers changes by 15 kHz. Apart from the difficulty of setting the initial frequency with sufficient accuracy, it is unlikely that two L-C oscillators could be kept within 15 kHz of each other at 60 MHz to 100 MHz operating frequencies. However, when the audio signal is modulated onto a 4.5 MHz intercarrier oscillator frequency and this carrier is used to modulate the picture carrier, we have only the 4.5 MHz oscillator drift to worry about.

A less obvious problem, but nevertheless significant if good audio quality is to be obtained, is incidental carrier phase modulation (ICPM). Even broadcast transmitters cannot maintain an invariant carrier phase as the modulation depth changes. Without feedback loops to control ICPM, a broadcast transmitter can produce from 3 degrees to as much as 30 degrees phase change as the carrier modulation decreases from sync tips to peak white. While the separate sound carrier is unaffected by this ICPM of the pix carrier, on reception in the intercarrier sound receiver the phase shift with picture information is transferred onto the 4.5 MHz sound intercarrier. This results in a phenomenon known as sound buzz. Even with exceptionally careful p.c.b. layout, an I/C modulator with L-C oscillators can expect the pix carrier frequency to change with modulation depth. Fortunately, by modulating the sound signal as a 4.5 MHz intercarrier onto the pix carrier, the ICPM occurs equally in both R.F. carriers and will not be detected by the intercarrier receiver.

Video Modulation

The baseband input to the modulator is in an easily recognized composite format and this is a convenient point at which to introduce the I.R.E. scale. This is an oscilloscope scale divided into 140 units. The video portion of the signal representing the scene (picture) brightness levels will occupy the 0 to 100 I.R.E. portion of the scale, with 0 I.R.E. as black level and 100 I.R.E. as peak white level. From 0 to −40 I.R.E. is the synchronization portion of the signal. The usefulness of this scale is that the standard composite video signal will always have a sync amplitude that can be normalized to 40 I.R.E. Similarly the color burst amplitude is always 40 I.R.E. For a 1V (p-p) video signal, an I.R.E. unit is equivalent to 7.5 mV.

Although the video is amplitude modulated on the carrier waveform, the carrier amplitude only decreases from the unmodulated level. This contrasts with standard AM where the carrier level alternately increases and decreases about the unmodulated level. For a television signal, the peak unmodulated level corresponds to sync tip level and increasing brightness levels cause decreasing carrier levels. To prevent complete suppression of the carrier (and consequent loss of the sound intercarrier in the receiver) the peak white signal is limited to a maximum modulation depth of 87.5% of the peak carrier. Returning to our I.R.E. scale we can see that from peak carrier to zero carrier is equivalent to 160 I.R.E. (140/0.875 = 160). One obvious consequence of this modulation scheme is that the video signal MUST BE dc coupled to the modulator. AC coupling will cause the peak carrier level to change with modulation scene brightness (standard AM) and the sync modulation amplitude will change. This spells trouble for the receiver sync circuits and the changing R.F. carrier black level will cause errors in displayed brightness—the picture will "wash out" or disappear into black.

The LM2889 uses doubly balanced modulator circuits with an L-C oscillator switching the upper transistor pairs. The signal is applied across the lower transistor pairs. If the signal input pins 10 and 11 are at the same dc potential, the

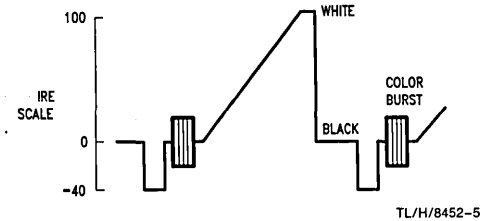
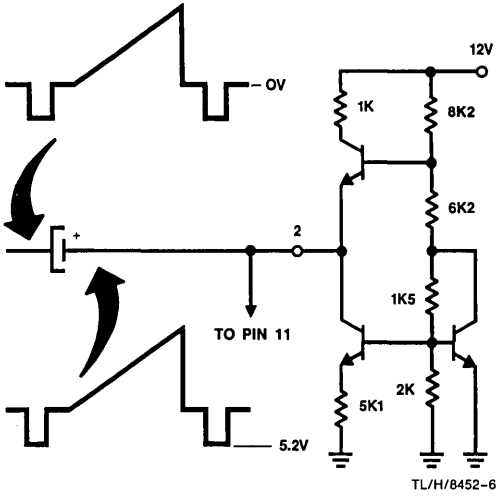


FIGURE 5. Video Modulating Signal (In terms of the I.R.E. Scale)

Video Modulation (Continued)



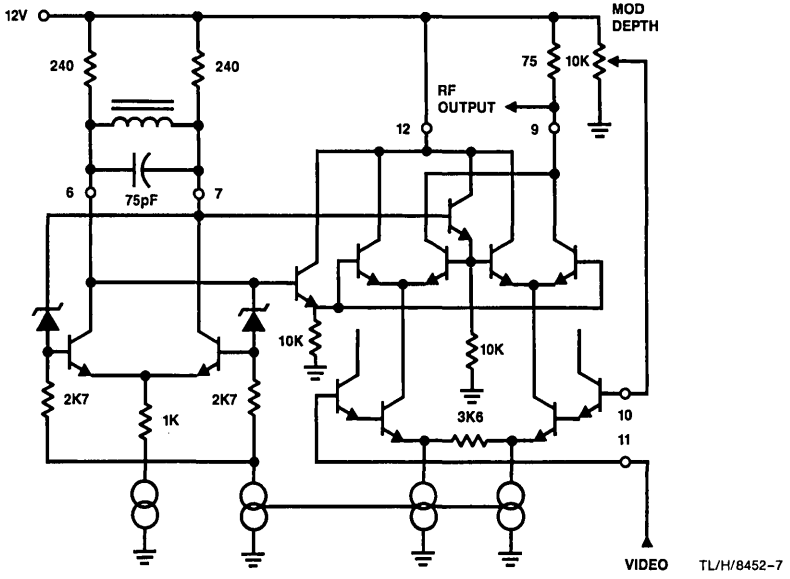
TL/H/8452-6

FIGURE 6. LM2889 Video DC Restoration Clamp

carrier is completely suppressed. As the offset voltage between pins 10 & 11 is increased, the carrier output level increases. With a 75Ω output load resistor, the conversion gain of the R.F. modulator is 20 mVrms/volt. A dc restoration circuit at pin 2 of the LM2889 allows the composite video to be ac coupled from the preceding stages, giving the designer flexibility in the video processing circuits (unless an LM1886 is being used as a video source, it is unlikely that the composite video dc level will be correct, even with dc coupled video sources). On a 12V supply, pin 2 clamps the sync tip of the video waveform to 5.1 VDC. Therefore, if we have a 2V (p-p) signal, one I.R.E. is equivalent to 14.3 mV and 160 I.R.E. is 2.29V. This is the required offset across the modulator input pins and since pin 11 will be clamped to 5.1 VDC by the dc restorer circuit, pin 10 should be biassed at 5.1V + 2.29V = 7.4 VDC. A look at the R.F. carrier output will confirm that now the syncs occupy from 100% to 75% of the peak carrier, and that white modulates the carrier down to 12½% of the peak. To maintain the proper modulation depth the clamp at pin 2 will track with supply voltage changes, allowing the bias at pin 10 to be set with a resistive divider connected between the supply and ground.

If the video signal polarity is reversed with positive syncs, either a dc coupled signal or an external dc restorer should be used that places the signal sync tip voltage towards the upper end of the common-mode input range at pin 11, which is 9 VDC with a 12V supply. Pin 10 is then offset below pin 11 voltage by the required amount for proper modulation. An input level of 2V (p-p) is optimal. Signal amplitudes of less than 1V (p-p) are also useable but internal offset voltages and the potential for carrier feedthrough or leakage to the output stage may make it difficult to maintain good R.F. linearity at peak modulation depths. Signal swings larger than 3V (p-p) should be avoided since this will produce relatively large AC/DC current ratios in the modulator and the resulting modulator non-linearities can cause a 920 kHz beat between the chroma and sound carriers.

Although only one video input is required, the LM2889 has two balanced R.F. modulators and two R.F. carrier frequency oscillators. Selection of the carrier frequency is by dc switching the supply voltage to the relevant oscillator tuned circuit. This automatically shuts off the other oscillator and modulator circuits. For test purposes when an output R.F. VSB filter isn't used, or when only one carrier frequency is needed, the output pins 8 and 9 can be wired together with a common load resistor. Providing two channel operation with two independent oscillator/modulator circuits is much superior to using a single modulator and attempting to change carrier frequency by switching the tuning components of a single L-C oscillator. The latter method involves



TL/H/8452-7

FIGURE 7. LM2889 R.F. Modulator and Oscillator (one channel)

Video Modulation (Continued)

use of isolating diodes (if unbalanced operation with attendant feed through problems is to be avoided) and expensive trimmer capacitors for tuning the second carrier frequency. A further disadvantage is the need to switch the VSB filter at the R.F. output.

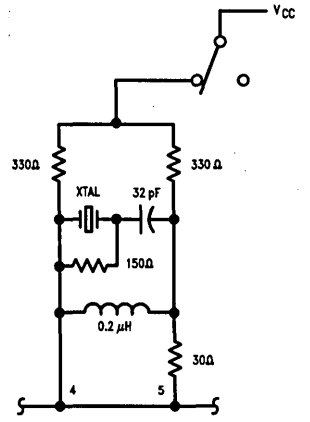
The LM2889 oscillator configuration is the familiar cross coupled differential amplifier type, with level shifting zener diodes used to prevent the transistors from saturating with large oscillator output swings. The oscillator frequency is set by the tuned circuit components ($f = 1/2\pi\sqrt{LC}$), and the load resistors connected to the supply will set the oscillation amplitude and drive level to the modulators as well as determining the circuit working Q.

As might be expected, there are conflicting requirements on the practical range of working Q's. A high Q is desireable from the viewpoint of stability, but higher working Q's (set mainly by larger load resistors) increase the drive level to the modulator. Above 350 mV (p-p) the modulator will have attained full conversion gain and the R.F. output level will be determined by the amplitude of the video input signal. Unfortunately increased drive levels will also increase the carrier frequency second harmonic output from the modulator. Although a fully balanced design is used, parasitic capacitances on the emitters of the switching transistor pairs will rectify the oscillator waveform and this produces high levels of second harmonic. Load resistors much larger than 240Ω can produce a level of second harmonic matching the fundamental. Since relatively small load resistors are required (much smaller than the tuned circuit dynamic resistance) the working Q will be dominated by these resistors.

The acceptable degree of frequency stability will depend on the intended application, but L-C oscillators have proven to be adequate for most purposes. We can gain an idea of the frequency stability that is possible by considering the frequency drift produced by changes in the oscillator internal phase. A change in internal phase shift can be caused either by temperature or supply voltage changes but, as the LM2889 data sheet shows, the supply voltage dependency is low. Between 12V and 15V the frequency is essentially constant and changes by less than 30 kHz over the entire supply voltage range. With temperature, the internal oscillator phase shift changes by about 2 degrees over a 50 degree Celcius temperature range. If the tuned circuit Q is 15, then at 61.25 MHz (Ch 3 pix carrier) the oscillator frequency must change by −92 kHz to produce a compensating 2 degree phase shift. If the Q is 30, then the frequency would change by less than −45 kHz etc.

For high circuit Q, a large capacitance is desireable, but the inductor cannot be made too small if it is to remain the tuning element. This keeps the practical range of capacitance values to between 50 pF and 100 pF. Using a 75 pF capacitance, at 67.25 MHz the required inductance is just under 0.08 μH and the working Q is 15 with 240Ω resistors connected on either side of the tuned circuit to the supply voltage. Depending on the coil type, the number of turns for this inductance will be from 1½ to 3½ giving over 10 MHz tuning range. This is more than enough to compensate for component tolerance and variations in overall internal phase lag from I/C to I/C.

If better frequency stability of the carrier frequency over that provided by an L/C circuit is needed, then crystal control of the oscillators can be used. It is necessary to retain the inductor, since a dc short is required across the oscillator pins to avoid a collector current imbalance off-setting the oscillator differential pair and preventing start-up. The inductor value is chosen to resonate with the capacitor in series with the crystal at slightly less than the desired operating frequency. About 20% less will allow the inductor to be fixed tuned. Close to its series resonant frequency (normally the 3rd overtone) the crystal will provide the additional inductive reactance necessary for the circuit to oscillate. The equivalent resistance of the crystal at the operating frequency will affect the tuned circuit Q and hence the peak-to-peak drive to the modulator circuit. Smaller capacitors in series with the crystal (with corresponding changes in the inductor value) will push the operating frequency closer to anti-resonance and produce large equivalent resistances dropping the oscillator drive level. Larger capacitance values cause the operating frequency to approach series resonance and a lower equivalent resistance (approaching R_S for the crystal, which is of the order of 40Ω to 100Ω at 60 MHz). This can produce higher drive levels but risks operation at the lower overtones. To prevent lower frequency oscillation a resistor can be connected across the crystal. Also a small resistor in series with one of the collector leads will form a low pass filter with the output capacitance and suppress spurious oscillations at higher frequencies. If this is needed, resistor values less than 30Ω should be used, so that dc offsets will not prevent the oscillator from starting. For the circuit of *Figure 8*, capacitor values between 20 pF and 56 pF, with the appropriate inductor value, work well with only slightly reduced oscillator drive compared to the conventional L/C circuit.



TL/H/8452–8

FIGURE 8. R.F. Crystal Oscillator Circuit

The Sound Carrier Oscillator

Before moving to the R.F. output and the VSB requirements, we need to look at another signal that will be added to the baseband video—the aural intercarrier. Both the LM1889 and the LM2889 have L-C sound carrier oscillators operating at 4.5 MHz. Frequency modulation of the LM1889 sound oscillator is achieved by an external varactor diode which alters the tuning capacitance in response to the amplitude of the audio signal. The LM2889 has a similar tuned L-C oscillator but the frequency deviation is obtained by internally phase shifting the oscillator current. This is done by a low pass filter connected to the oscillator which provides a lagging phase voltage component of the oscillator waveform at the input to a differential amplifier. The current output from

Sound Modulation

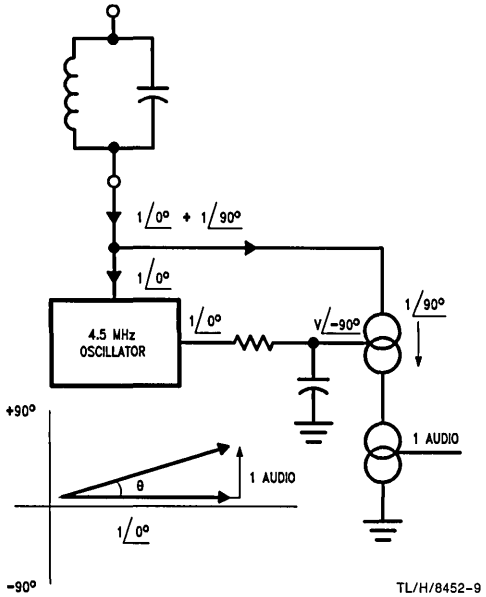


FIGURE 9. LM2889 Sound Carrier FM Modulator

this amplifier is controlled by the audio signal amplitude so that more or less of the current (now in quadrature to the original oscillator current) is added back to the tuned circuit producing the desired shift in the output frequency. Phase offsets of up to +12 degrees with increasing audio input levels will yield very low audio distortion (less than 0.2%). Also the use of a lagging oscillator waveform component reduces harmonic levels within the oscillator and a reduced possibility for undesired signals contaminating the R.F. waveform.

The tuned circuit operating Q is important in two respects. Similar to the R.F. oscillator tuned circuits, the 4.5 MHz tuned circuit should have a high loaded Q for stability, but the circuit bandwidth must also be wide enough to accommodate the FM sidebands produced by the audio modulation. For a maximum frequency deviation (Δf) and maximum modulating frequency f, the minimum bandwidth is given by Equation (1).

$$B\text{-}W \geq \Delta f\,(2.5 + 4f/\Delta f) \qquad (1)$$

The other requirement is that the maximum phase deviation of the oscillator current is able to produce the maximum frequency deviation (Δf) of the carrier. This is given by Equation (2).

$$\Delta f = 4.5 \times 10^6 \times 0.12 / Q \qquad (2)$$

Table I summarizes the results of calculating the maximum circuit Q that satisfies Equations (1) and (2) for the various monaural sound modulating standards used in the U.S. and Europe.

TABLE I

System		Δf	Modulation Bandwidth	Q_{max}	
				Modulation	Deviation
USA	Mono	25 kHz	125 kHz	≤36	≤21
	Stereo	73 kHz	400 kHz	≤12	≤7.4
UK		50 kHz	200 kHz	≤30	≤15
Continental Europe		30 kHz	150 kHz	≤36	≤22

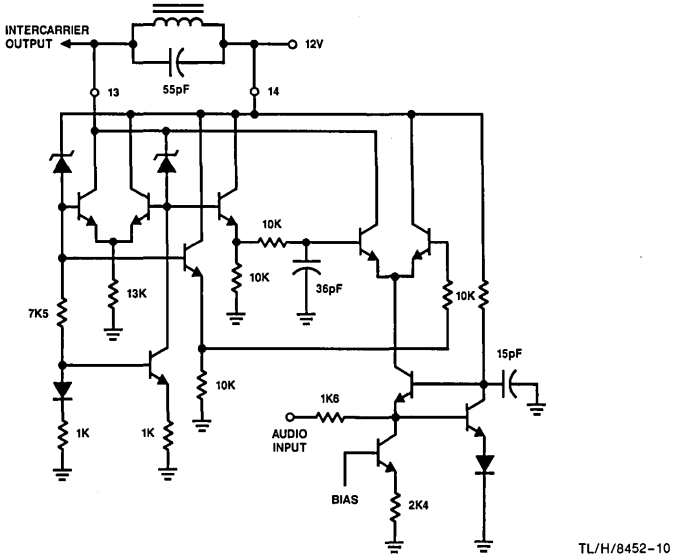


FIGURE 10. LM2889 4.5 MHz Sound Oscillator and Modulator

Sound Modulation (Continued)

Clearly the deviation phase offset dominates the circuit Q requirement.

If we choose a Q of around 10 then the oscillator drift with temperature (assuming a 2 degree phase change in oscillator current with a 50 degree rise in temperature) is of the order of −9 kHz. A typical receiver will generate less than 3% distortion at peak deviations with this much frequency drift but if better performance is required, then the circuit Q can be raised. High modulation linearity will still be retained with a Q of 20 and the oscillator maximum frequency drift will be halved. Alternatively temperature compensated tuning capacitors can be used (between N20 and N75). When higher circuit Q's than 20 are employed, increased audio input levels will produce the desired peak frequency deviations but with the possibility of increased modulation distortion. The actual operating parameters that are selected can be balanced between distortion as a result of modulation, and distortion in the receiver circuits as a result of oscillator frequency drift.

To ensure that we have a sufficient 4.5 MHz oscillator level to provide enough drive to the internal phase shift circuit, the load impedance at pin 13 should be greater than 3.5 kΩ. A second requirement is that we have enough oscillator level to generate the desired aural carrier amplitude when modulated on the picture carrier. This means that load impedances greater than 6 kΩ are desireable. At 4.5 MHz, a typical oscillator coil of 23 μH will have an unloaded Q of 55 and tune with 55 pF. For a working Q of 10, the external damping resistor is 7.5 kΩ.

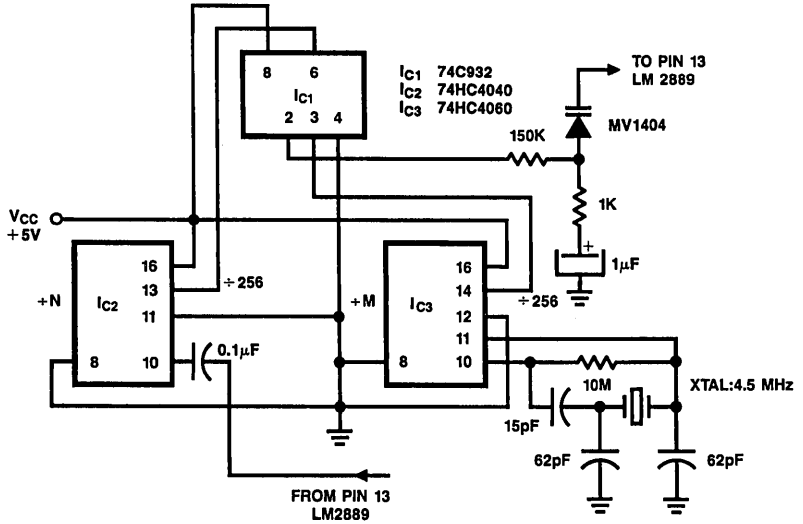
Stereo Sound

The introduction in the U.S. of a multiplex stereo sound system (the BTSC system combining the Zenith MCS proposal with dbx noise reduction in the stereo difference channel) with peak carrier deviations in excess of 73 kHz puts even larger constraints on the tank circuit Q. Following the same rules as before, the maximum allowable Q for low distortion is now less than 7.4—with a loaded Q of 5 being likely. With this loaded Q, maintaining a carrier center frequency accuracy better than 5 kHz with an L/C circuit becomes impractical and other methods to set the oscillator frequency must be used. Since a crystal will provide the necessary temperature and voltage stable reference frequency a PLL is a useful solution (see *Figure 11*). Either the widely available 3.58 MHz crystals or a 4.5 MHz crystal can be used, but in either case, the L/C tank circuit frequency must be divided down before application to the phase detector. This is because frequency modulation of the sound carrier will produce many radians of phase deviation at the phase detector input—for a modulation frequency of 100 Hz and a peak deviation of 73 kHz the carrier phase change is given by Equation 3.

$$\theta = \Delta f/fm = 73 \times 10^3/100 = 730 \text{ rads} \qquad (3)$$

Since the linear input range of most phase detectors is less than 2 π radians, the modulated carrier input must be divided down by at least 233 to keep the phase deviation within this linear range. For a 4.5 MHz crystal, the reference frequency divider M and the sound oscillator divider N are the same. Available ripple counters such as the 74HC4040 and 74HC4060 can easily divide by 128 (for monaural) or by 256 for stereo. If a 3.58 MHz crystal is used the M:N divider ratio is 35:44 requiring substantially more packages, and the odd numbered divider must be followed by an even divide of 2 or 4 to "square up" the input waveform to the phase detector. Also, since the video will include a chroma subcarrier, good isolation is needed to prevent the reference oscillator beating with the chroma sidebands.

A suitable phase detector is the 74C932 Exclusive- Or type with a sensitivity of 1.6 volts/radian. The filter at the detector output prevents the input modulation from reaching the varactor diode and distorting the audio. Even so, the loop filter must have some ac bandwidth for a reasonable acquisition time and other dynamic characteristics. The components shown in *Figure 11* have been chosen such that with a varactor sensitivity of 100 kHz/volt the loop has a hold-in range of over ±150 kHz, with a lock-up time of less than 0.5 seconds. The T.H.D. is less than 1% for a 400 Hz modulating frequency producing 25 kHz deviation of the carrier. The accuracy of the sound carrier frequency is, of course, that of the crystal used for the reference oscillator.

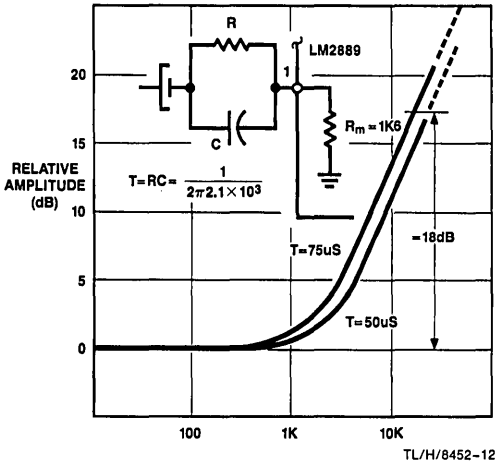


TL/H/8452–11

FIGURE 11. 4.5 MHz Crystal Reference Circuit

Audio Processing For Sound Carrier Modulation

With the proper tuned circuit Q (see Table I), a linear increase in the amplitude of the audio signal will produce a correspondingly linear increase in the frequency deviation. Television receiver sound circuits in the U.S. have a 75 μs de-emphasis and in Europe frequencies above 3.2 kHz (50 μs) are de-emphasized at a 6 dB/octave rate. This is done to help improve the S/N ratio of FM reception and the transmitter incorporates the complementary pre-emphasis characteristic—above 2.1 kHz the audio frequencies are boosted at a 6 dB/octave rate. The consequence of this modulation scheme is that if a 0 dB peak signal amplitude at 15 kHz is capable of producing a 25 kHz deviation than a similar amplitude signal at 400 Hz will produce a peak deviation of only 3 kHz—a loss of some 18 dB in S/N ratio for the midband frequencies. Broadcasters usually employ compressors to enable high modulation levels to be obtained at mid-band frequencies without overmodulating high frequencies. If the audio input to the LM2889 is being sourced from an original broadcast (a scrambled signal decoder output for example) than this audio—without de-emphasis—can be directly applied to pin 1 of the LM2889, and the overall input level is adjusted so that the modulation limits are not exceeded except for brief intervals (less than 10 instances per minute). When the audio has not already been processed a different set of conditions will apply and an audio pre-emphasis network is required at pin 1.



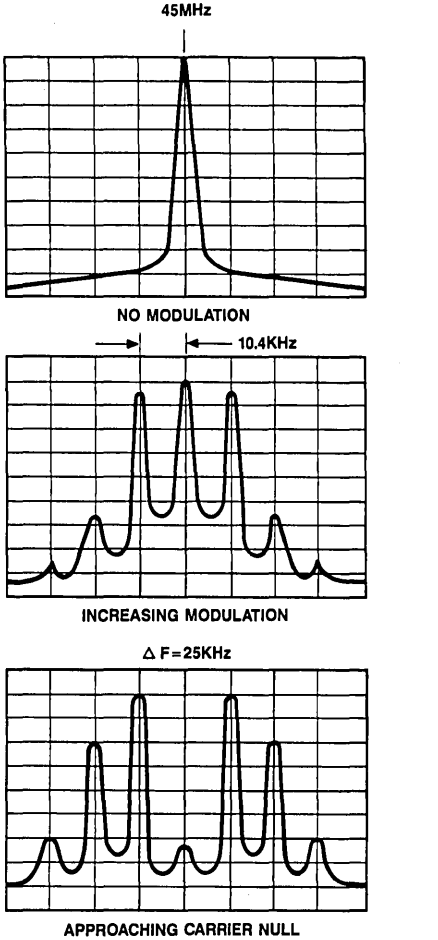
TL/H/8452-12

FIGURE 12. Audio Pre-emphasis

Since the audio source is likely to be at a relatively low impedance (a pre-amplifier output), the pre-emphasis network will also be used to attenuate the level of the average audio input to the LM2889 as well as providing a relative boost to the higher frequencies. The input sensitivity of the audio modulator is 150 Hz/mV which means that 118 mVrms will give a peak deviation of 25 kHz.

Next we have to decide what signal frequency and amplitude to use in calibrating the audio input. Unfortunately the 75 μs time constant for FM broadcasting was chosen at a time when equipment limitations meant there was relatively low spectral energy at higher frequencies. Today, modern audio material is not well suited to boosting above 2.1 kHz since energy peaks at only −6 dB can be obtained at 10 kHz. A further complication is the ability of the audio level meter to predict high energy peaks. If a conventional VU meter is used, peak levels of +10 dB are possible while the meter is indicating OVU. Obviously without processing the audio to keep it within predetermined limits, the input level calibration will be somewhat empirical in nature.

If we assume the decrease in spectral energy above 10 kHz is such that overmodulation peaks above this frequency are unlikely to occur, then we can allow a signal at 10 kHz to produce full modulation deviation. Since the amplitude of most audio signals at 10 kHz is at least 6 dB below the midband frequency level, we can calibrate the audio input with a −6 dB amplitude, 10 kHz tone to produce 100% deviation. As we shall see later, a frequency close to 10 kHz will make the measurement of actual peak deviations very easy indeed. With the standard pre-emphasis network, at signal frequencies less than 2 kHz, the modulating signal amplitude at pin 1 will be −8 dB below the anticipated peak 10 kHz level producing 100% modulation. This corresponds to a modulator input level of 118/2.2 = 45.4 mVrms. The



TL/H/8452-13

FIGURE 13. FM Spectrum with Increasing Audio Amplitude (f mod = 10.4 kHz) 4.5 MHz Sound Carrier Level

Audio Processing For Sound Carrier Modulation (Continued)

input resistance at pin 1 is 1.5 kΩ so R1 = 30 kΩ, if we assume an input source level of 1 Vrms at 400 Hz. For a 2.1 kHz breakpoint, C = 0.0027 μF.

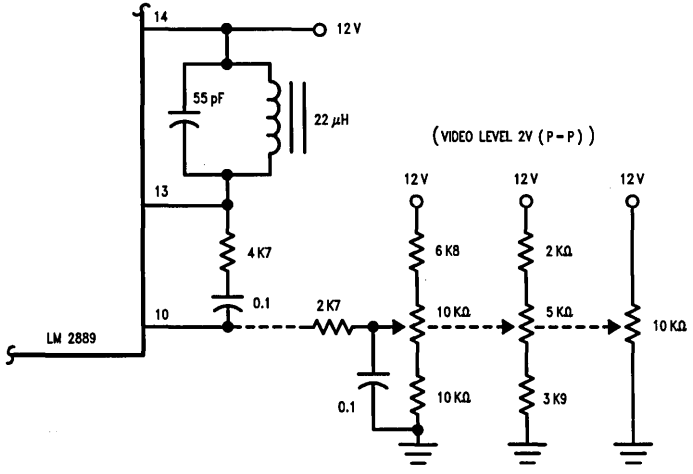
Anyone who has observed the output from an FM circuit with a spectrum analyzer will know that for a fixed modulating frequency the output spectrum will consist of the carrier frequency component and sidebands spaced by the modulating frequency from the carrier. As the modulation amplitude is increased (the modulation index m becomes larger), the carrier decreases to a null and then increases again. The modulation indices for which carrier nulls occur can be calculated and for our purposes it is important to know that the first carrier null occurs at m = 2.4048. For a system maximum deviation of 25 kHz the modulating frequency f is given by:

$$f = 25 \times 10^3/2.4048 = 10.4\ \text{kHz} \qquad (4)$$

Therefore, if we use an input frequency of 10.4 kHz, as the input amplitude is increased the first carrier null will indicate peak deviation. If we continue with our assumption of a −6 dB level at 10 kHz, calibration consists of adjusting the audio input so that a −6 dB, 10.4 kHz signal causes the first carrier null. With the above pre-emphasis network, this should correspond to 500 mVrms at 10.4 kHz.

We have already looked at the tuned circuit parameters at pin 13 in terms of deviation linearity and oscillator stability. With a working Q of 10, the effective load at pin 13 is 6.2 kΩ. The oscillator current is 0.45 mA so that the output amplitude at 4.5 MHz is 3.6V (p-p). Some portion of this oscillator signal level is coupled over to pin 10 to set the sound carrier level and this can be done by splitting the external 7.5 kΩ damping resistor into two parts. The picture carrier level is set by the offset voltage between pins 10 and 11 as described earlier. For a 2V (p-p) video signal this offset is 2.3V. Since the 4.5 MHz signal will be ac coupled over to the bias pin 10, it will amplitude modulate the picture RF carrier. This is conventional AM and a 4.6V (p-p) signal will yield sound carrier sidebands at −6 dB relative to the picture carrier. If we require a sound carrier amplitude at −17 dB, the signal coupled to pin 10 must be 11 dB below 4.6V (p-p), or 1.3V (p-p). This is obtained by using a 4.7 kΩ resistor coupled through a 0.1 μF capacitor to pin 10, and a second 2.7 kΩ resistor connected to the wiper arm of the potentiometer used to set the video modulation depth. The effect of the potentiometer setting on the aural carrier level is eliminated by a 0.1 μF capacitor connected from the wiper arm to ground. However, since the impedance presented by the potentiometer will, for all practical purposes, be relatively constant, the capacitor could be removed and the parallel resistance of the upper and lower arms of the potentiometer network used to provide the second resistor of 2.7 kΩ. If the video input level is well controlled, it may be possible to replace the potentiometer with a fixed divider.

The final part of the design concerns the output stage, and involves meeting the constraints applied by any regulatory agency. In the U.S., apart from the need to restrict the peak carrier output level to less than 3 mVrms in 75Ω, we have two signals present in the output whose level will exceed the spurious emission limit of −30 dB with respect to the peak carrier level. One of these signals is the result of amplitude modulating the 4.5 MHz intercarrier audio on the picture carrier. Apart from the desired −17 dB sound carrier amplitude (upper sideband) an equal amplitude lower sideband will be present. For channel 3 this is at a frequency of 56.75 MHz—which is 250 kHz outside our channel lower limit. Therefore we need to provide at least 13 dB more attenuation at this frequency in the output filter. The second unwanted emission (or emissions) is the result of carrier frequency harmonics—specifically the 2nd harmonic level produced by high modulator drive. To suppress this, from −18 dB to −30 dB attenuation at 123 MHz is required.



TL/H/8452-14

FIGURE 14. Audio Intercarrier Coupling to the Video Modulator R.F. Output and V.S.B. Filter

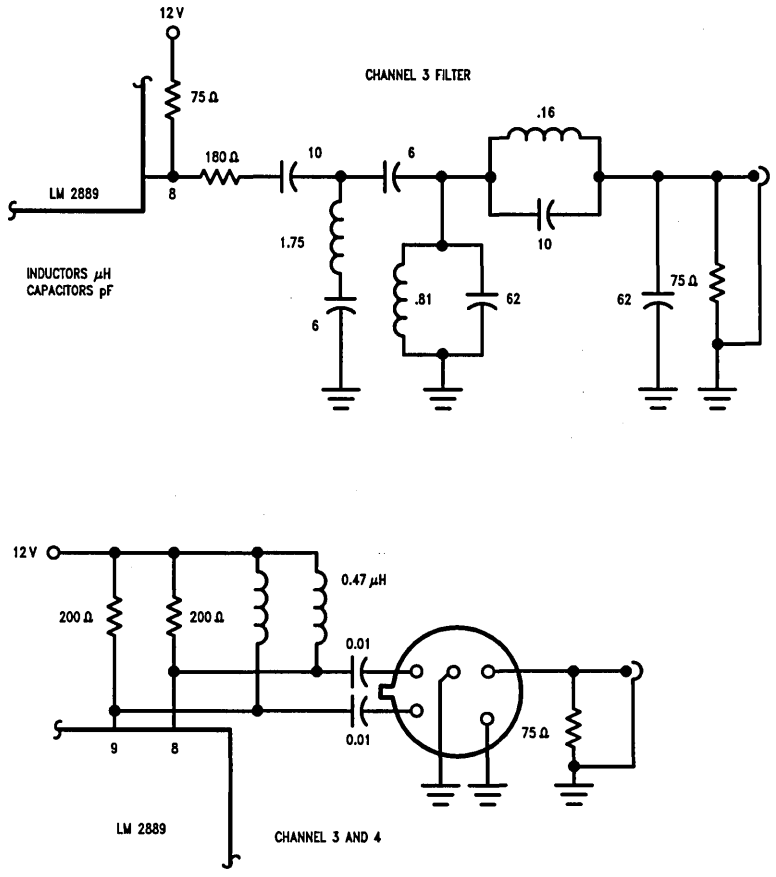
Audio Processing For Sound Carrier Modulation (Continued)

With a properly constituted baseband signal modulating the carrier, these are the only intrinsic unwanted emissions we are concerned with. Normal video modulation components appearing in the lower sideband will not have sufficient amplitude and do not extend beyond the lower channel limit. Even so, the filter requirements are not trivial.

If L-C filters are used, this can be done with three coils per channel but some alignment procedure will be required. Fortunately SAW filters are available from several sources which, although more expensive than the equivalent L-C filter, avoid the cost of production alignment. Usually the SAW filter will have a substantially greater insertion loss, but the LM2889 has enough output level to compensate for this. Both single channel and dual channel filters are available and in the latter case the LM2889 dual oscillator/modulator configuration enables easy dc switching between channels. A coil may be required, connected across the SAWF input, to tune out the SAWF input capacitance.

The load resistors connected to pins 8 and 9 will set the LM2889 conversion gain, which for 75Ω is typically 20 mVrms R.F. carrier per volt offset at the input pins 10 and 11. The actual load will include the input resistance of the filter. Since the output of the filter will normally be terminated in 75Ω to match the cable (and provide triple transit echo suppression for a SAWF), the best way to choose the load resistor is to monitor the output to the cable and apply a dc offset between pin 10 and 11 that is equivalent to the expected video input. The resistor is then chosen to give the desired peak carrier level of 2.5 mVrms. The carrier should be unmodulated since downward modulation will reduce the mean carrier level by as much as 2–3 dB.

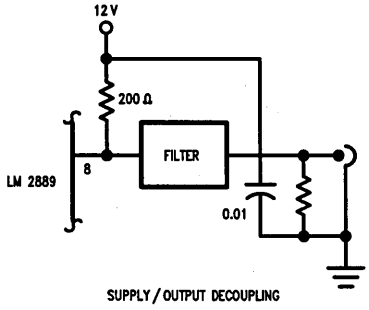
If the offset voltage between pin 10 and 11 is reduced, a check can be made on the residual carrier level at the output. This residual level is the result of oscillator feedthrough in the modulators and external coupling from the oscillator tuned circuits. The residual carrier level is normally better than −26 dB below the peak carrier level, ensuring good modulation linearity. High levels of residual carrier can be caused by coupling through ground or power supply leads. A good technique to minimize the effect of unwanted pick-up is to decouple the supply voltage to pin 8 and 9 load resistors over to the output connector shield ground. This removes at the output any carrier signal on the supply line to the load resistors.



TL/H/8452–15

FIGURE 15. Vestigial Sideband Filters

Audio Processing For Sound Carrier Modulation (Continued)



TL/H/8452–16

FIGURE 16. R.F. Decoupling at the Output

Sources: SAWFs

Crystal Technology, Inc.
1035 E. Meadow Circle
Palo Alto, CA 94303

Kyocera International, Inc.
8611 Balboa Ave.
San Diego, CA 92123

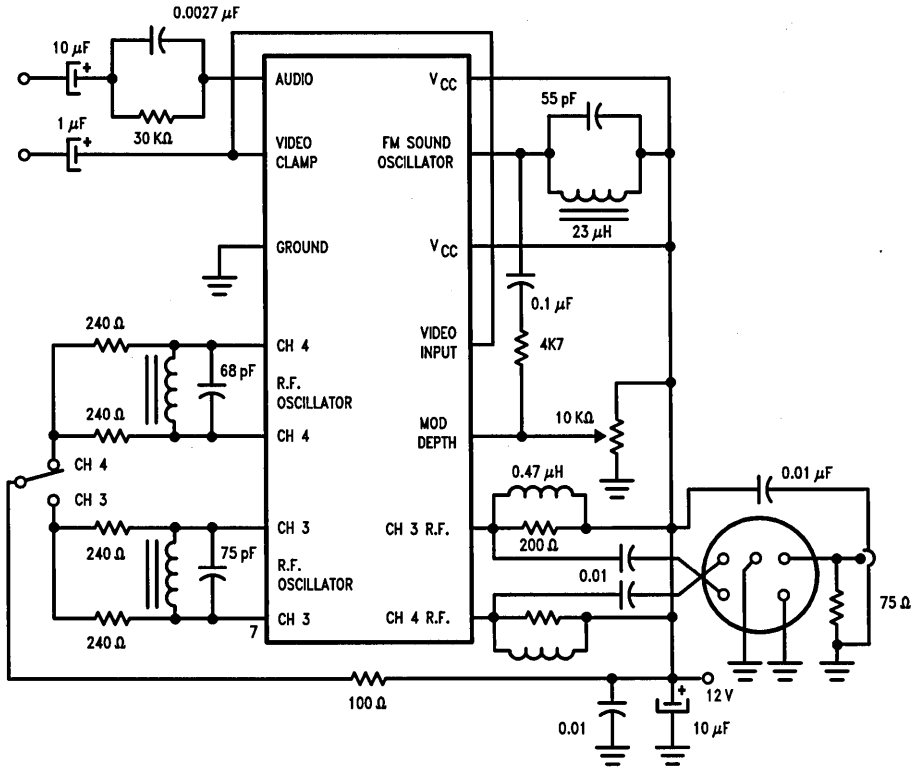
MuRata Corp. of America
1148 Franklin Rd. S.E.
Marietta, GA 30067

CRYSTALS

Saronix
4010 Transport at San Antonio Rd.
Palo Alto, CA 94303

COILS

Toko America, Inc.
5520 W. Touhy Ave.
Skokie, Ill. 60077



TL/H/8452–17

FIGURE 17. Complete R.F. Modulator External Circuit

Section 3

Physical Dimensions/ Appendices

Section 3 Contents

National Semiconductor

APPENDIX A: Related Datasheets

The table below lists a series of other products/functions that may have interest and which are available as datasheets from National Semiconductor.

Product Number	Product Description
DP85101/FVG101	50 MHz Triple 8-Bit VIDEODAC™ Pin Equivalent to Brooktree BT101
DP85108/FVG108	300 MHz 8-Bit VIDEODAC Pin Equivalent to Brooktree BT108
DP85450/FVG450	70 MHz Triple 4-Bit RAMDAC™ with 16 x 12 Color Palette Pin Equivalent to Brooktree BT450
DP85453/FVG453	40 MHz Triple 8-Bit RAMDAC with 256 x 24 Color Palette Pin Equivalent to Brooktree BT453
DP85176-50/DAC0630	50 MHz Triple 6-Bit VIDEODAC Pin Equivalent to INMOS 176
DP85176-35/DAC0631	35 MHz Triple 6-Bit VIDEODAC Pin Equivalent to INMOS 176
NS32CG16	High Performance Printer Processor
LH4002	Wideband Video Buffer
LH4003	Precision RF Closed Loop Buffer
LH4004	Wideband FET Input Buffer Amplifier
LH4101	Wideband High Current Operational Amplifier
LM592	Differential Video Amplifier
LM675	Power Operational Amplifier
LM1203	RGB Video Amplifier System
LM1211	Broadband Demodulator SSC129
LM1578	Switching Regulator
LM1823	Video IF Amplifier/PLL Detection System
LM1875	20W Power Audio Amplifier
LM1881	Video Sync Separator
LM1884	TV Stereo Decoder
LM1886	TV Video Matrix D to A
LM1889	TV Video Modulator
LM2889	TV Video Modulator
LM6161	High Speed Operational Amplifiers
LM6164	High Speed Operational Amplifiers
LM6165	High Speed Operational Amplifiers
LMC555	CMOS Timer

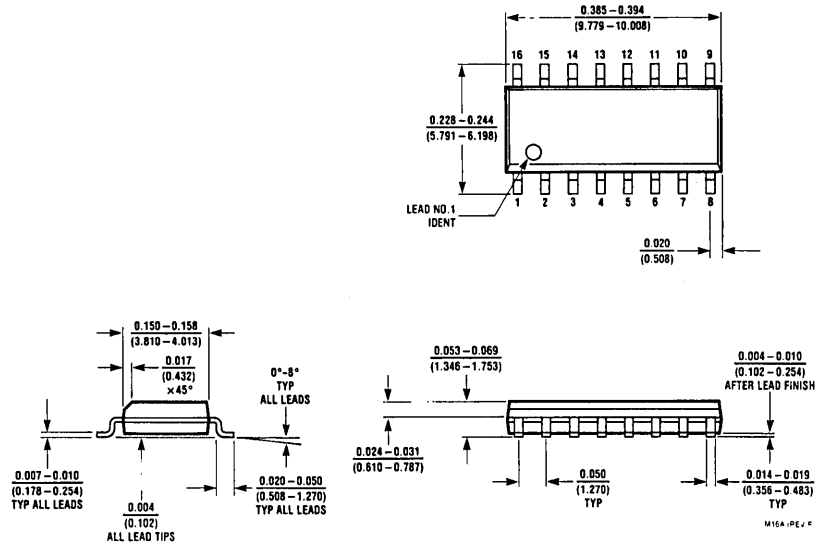
APPLICATION NOTES

Note No.	Description
AN-391	The LM1823—A High Quality TV Video IF Amplifier and Synchronous Detector for Cable Receivers
AN-402	LM2889 R.F. Modulator

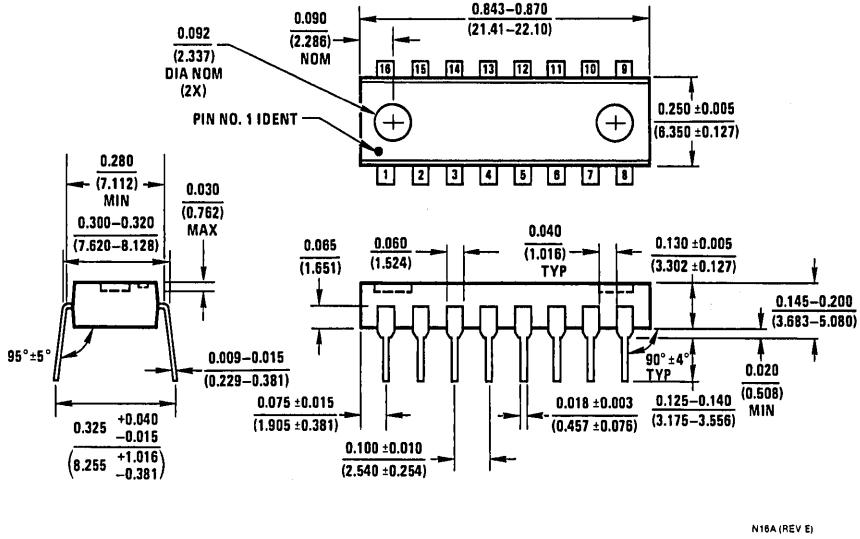
VIDEODAC™ and RAMDAC™ are trademarks of Brooktree Corporation.

National Semiconductor

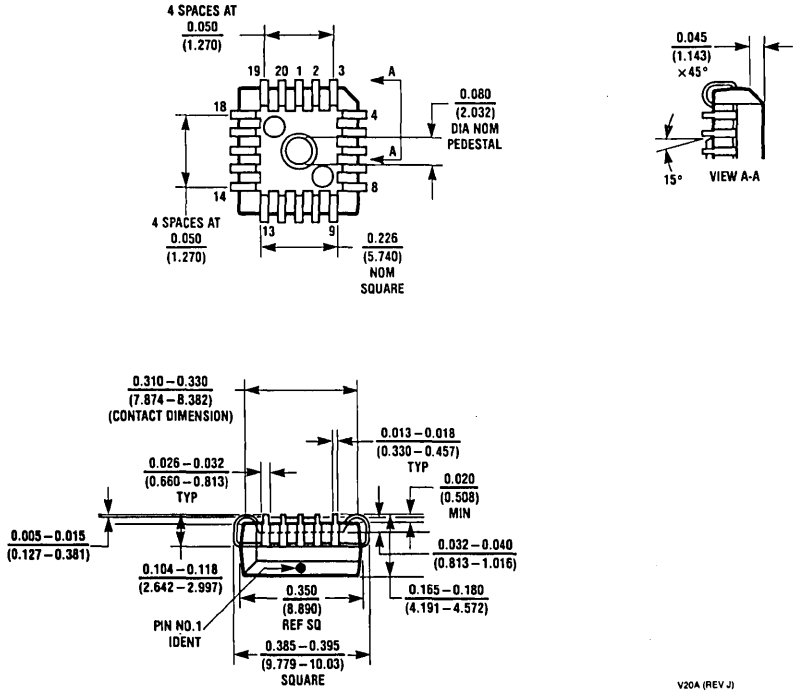
All dimensions are in inches (millimeters)



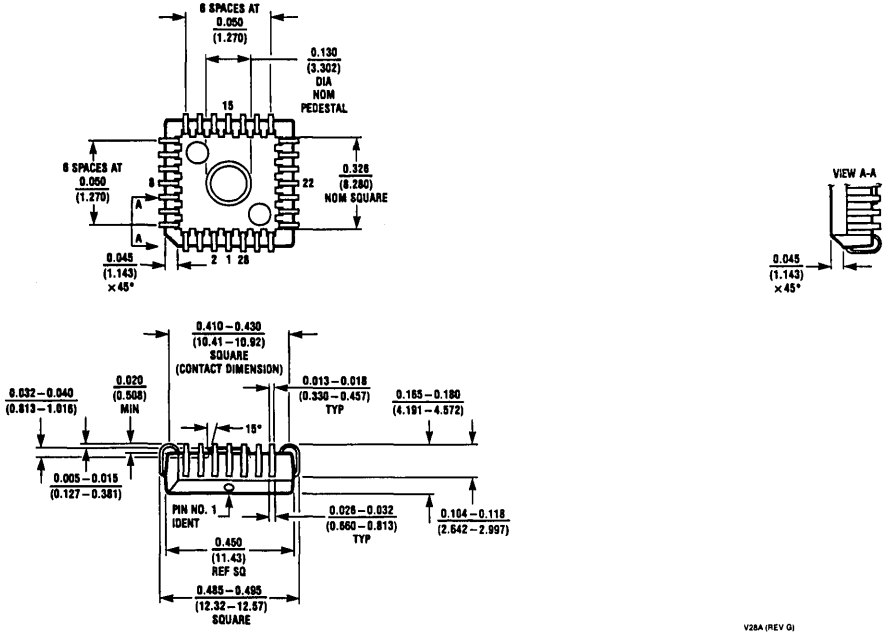
NS Package M16A



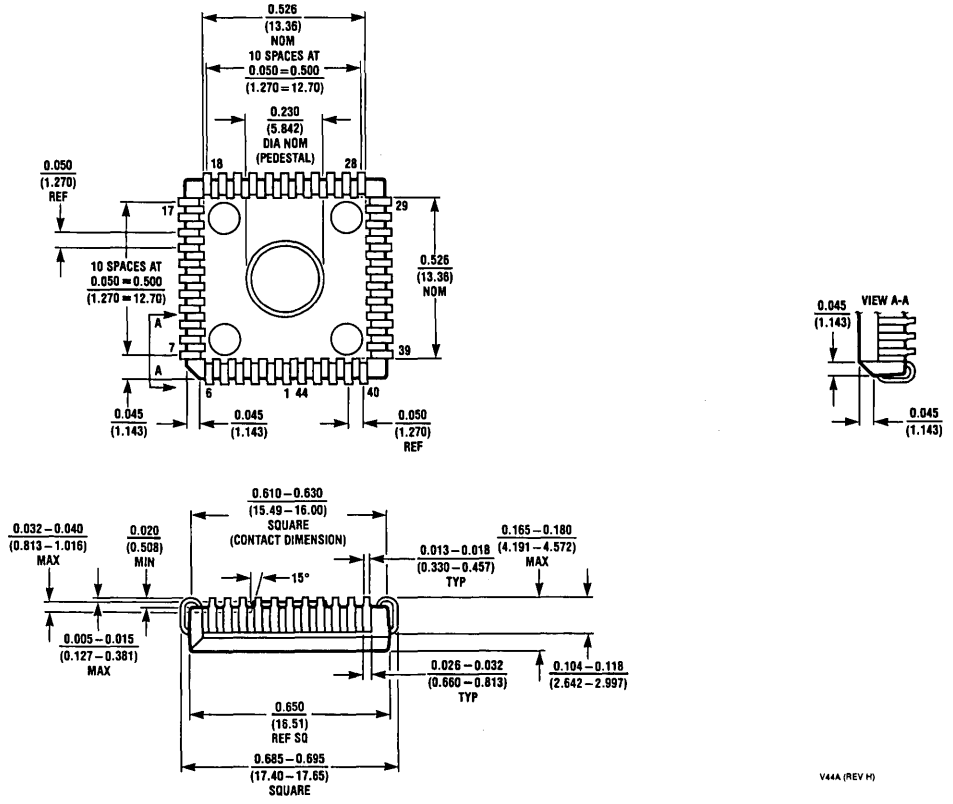
NS Package N16A



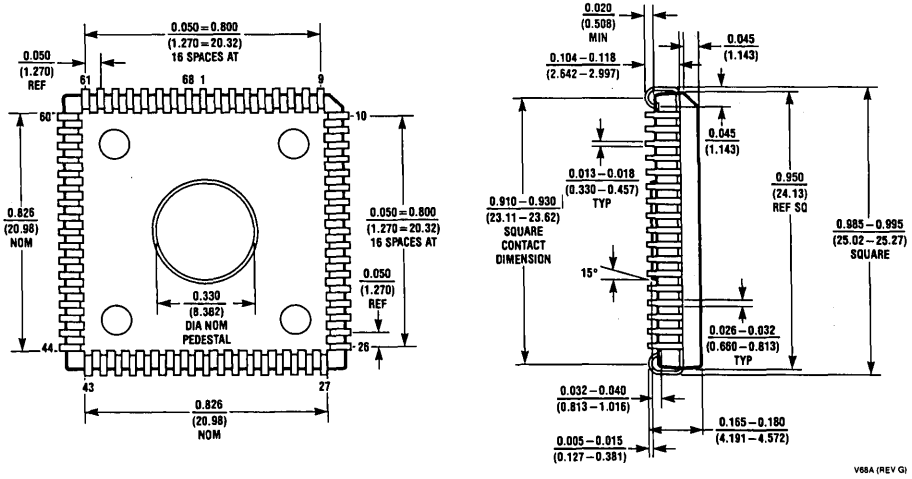
NS Package V20A



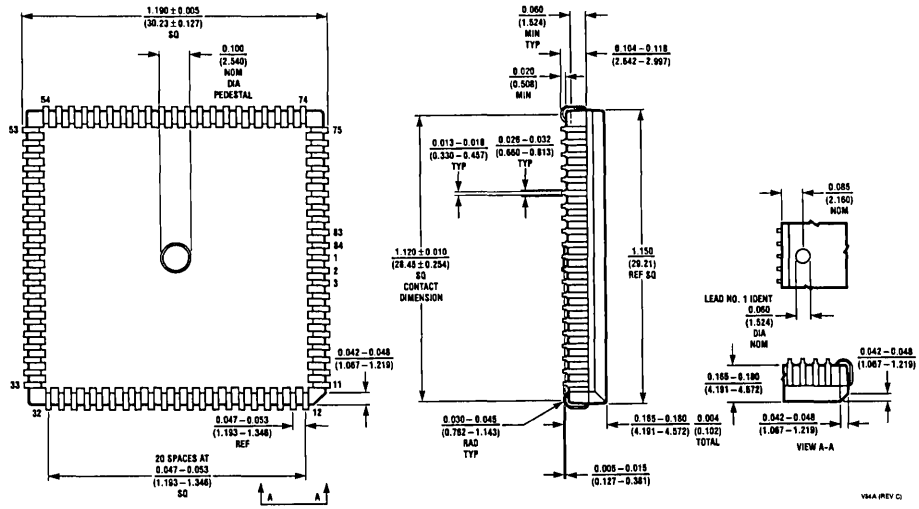
NS Package V28A



NS Package V44A



NS Package V68A



NS Package V84A

NOTES

NOTES

NOTES

NOTES

NOTES

NOTES

National Semiconductor

Bookshelf of Technical Support Information

National Semiconductor Corporation recognizes the need to keep you informed about the availability of current technical literature.

This bookshelf is a compilation of books that are currently available. The listing that follows shows the publication year and section contents for each book.

Please contact your local National sales office for possible complimentary copies. A listing of sales offices follows this bookshelf.

We are interested in your comments on our technical literature and your suggestions for improvement.

Please send them to:

Technical Communications Dept. M/S 23-200
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090

For a recorded update of this listing plus ordering information for these books from National's Literature Distribution operation, please call (408) 749-7378.

ALS/AS LOGIC DATABOOK—1987

Introduction to Bipolar Logic • Advanced Low Power Schottky • Advanced Schottky

ASIC DESIGN MANUAL/GATE ARRAYS & STANDARD CELLS—1987

SSI/MSI Functions • Peripheral Functions • LSI/VLSI Functions • Design Guidelines • Packaging

CMOS LOGIC DATABOOK—1988

CMOS AC Switching Test Circuits and Timing Waveforms • CMOS Application Notes • MM54HC/MM74HC MM54HCT/MM74HCT • CD4XXX • MM54CXXX/MM74CXXX • Surface Mount

DATA CONVERSION/ACQUISITION DATABOOK—1984

Selection Guides • Active Filters • Amplifiers • Analog Switches • Analog-to-Digital Converters Analog-to-Digital Display (DVM) • Digital-to-Analog Converters • Sample and Hold • Sensors/Transducers Successive Approximation Registers/Comparators • Voltage References

DATA COMMUNICATION/LAN/UART DATABOOK—Rev. 1

LAN IEEE 802.3 • High Speed Serial/IBM Data Communications • ISDN Components • UARTs Modems • Transmission Line Drivers/Receivers

INTERFACE DATABOOK—1988

Transmission Line Drivers/Receivers • Bus Transceivers • Peripheral Power Drivers • Display Drivers Memory Support • Microprocessor Support • Level Translators and Buffers • Frequency Synthesis • Hi-Rel Interface

INTERFACE/BIPOLAR LSI/BIPOLAR MEMORY/PROGRAMMABLE LOGIC DATABOOK—1983

Transmission Line Drivers/Receivers • Bus Transceivers • Peripheral/Power Drivers Level Translators/Buffers • Display Controllers/Drivers • Memory Support • Dynamic Memory Support Microprocessor Support • Data Communications Support • Disk Support • Frequency Synthesis Interface Appendices • Bipolar PROMs • Bipolar and ECL RAMs • 2900 Family/Bipolar Microprocessor Programmable Logic

INTUITIVE IC CMOS EVOLUTION—1984

Thomas M. Frederiksen's new book targets some of the most significant transitions in semiconductor technology since the change from germanium to silicon. *Intuitive IC CMOS Evolution* highlights the transition in the reduction in defect densities and the development of new circuit topologies. The author's latest book is a vital aid to engineers, and industry observers who need to stay abreast of the semiconductor industry.

INTUITIVE IC OP AMPS—1984

Thomas M. Frederiksen's new book, *Intuitive IC Op Amps,* explores the many uses and applications of different IC op amps. Frederiksen's detailed book differs from others in the way he focuses on the intuitive groundwork in the basic functioning concepts of the op amp. Mr. Frederiksen's latest book is a vital aid to engineers, designers, and industry observers who need to stay abreast of the computer industry.

LINEAR APPLICATIONS HANDBOOK—1986

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

LINEAR 1 DATABOOK—1988

Voltage Regulators • Operational Amplifiers • Buffers • Voltage Comparators • Instrumentation Amplifiers • Surface Mount

LINEAR 2 DATABOOK—1988

Active Filters • Analog Switches/Multiplexers • Analog-to-Digital • Digital-to-Analog • Sample and Hold
Sensors • Voltage References • Surface Mount

LINEAR 3 DATABOOK—1988

Audio Circuits • Radio Circuits • Video Circuits • Motion Control • Special Functions • Surface Mount

LINEAR SUPPLEMENT DATABOOK—1984

Amplifiers • Comparators • Voltage Regulators • Voltage References • Converters • Analog Switches
Sample and Hold • Sensors • Filters • Building Blocks • Motor Controllers • Consumer Circuits
Telecommunications Circuits • Speech • Special Analog Functions

LS/S/TTL DATABOOK—1987

Introduction to Bipolar Logic • Low Power Schottky • Schottky • TTL • Low Power

MASS STORAGE HANDBOOK—Rev. 2

Winchester Disk Preamplifiers • Winchester Disk Servo Control • Winchester Disk Pulse Detectors
Winchester Disk Data Separators/Synchronizers and ENDECs • Winchester Disk Data Controller
SCSI Bus Interface Circuits • Floppy Disk Controllers

MEMORY SUPPORT HANDBOOK—1986

Dynamic Memory Control • Error Checking and Correction • Microprocessor Interface and Applications
Memory Drivers and Support

NON-VOLATILE MEMORY DATABOOK—1987

CMOS EPROMs • EEPROMs • Bipolar PROMs

SERIES 32000 DATABOOK—1986

Introduction • CPU-Central Processing Unit • Slave Processors • Peripherals • Data Communications and LAN's
Disk Control and Interface • DRAM Interface • Development Tools • Software Support • Application Notes

RANDOM ACCESS MEMORY DATABOOK—1987

Static RAMs • TTL RAMs • TTL FIFOs • ECL RAMs

RELIABILITY HANDBOOK—1986

Reliability and the Die • Internal Construction • Finished Package • MIL-STD-883 • MIL-M-38510
The Specification Development Process • Reliability and the Hybrid Device • VLSI/VHSIC Devices
Radiation Environment • Electrostatic Discharge • Discrete Device • Standardization
Quality Assurance and Reliability Engineering • Reliability and Documentation • Commercial Grade Device
European Reliability Programs • Reliability and the Cost of Semiconductor Ownership
Reliability Testing at National Semiconductor • The Total Military/Aerospace Standardization Program
883B/RETS™ Products • MILS/RETS™ Products • 883/RETS™ Hybrids • MIL-M-38510 Class B Products
Radiation Hardened Technology • Wafer Fabrication • Semiconductor Assembly and Packaging
Semiconductor Packages • Glossary of Terms • Key Government Agencies • AN/ Numbers and Acronyms
Bibliography • MIL-M-38510 and DESC Drawing Cross Listing

TELECOMMUNICATIONS—1987

Line Card Components • Integrated Services Digital Network Components • Modems
Analog Telephone Components • Application Notes

THE SWITCHED-CAPACITOR FILTER HANDBOOK—1985

Introduction to Filters • National's Switched-Capacitor Filters • Designing with Switched-Capacitor Filters
Application Circuits • Filter Design Program • Nomographs and Tables

TRANSISTOR DATABOOK—1982

NPN Transistors • PNP Transistors • Junction Field Effect Transistors • Selection Guides • Pro Electron Series
Consumer Series • NA/NB/NR Series • Process Characteristics Double-Diffused Epitaxial Transistors
Process Characteristics Power Transistors • Process Characteristics JFETs • JFET Applications Notes

VOLTAGE REGULATOR HANDBOOK—1982

Product Selection Procedures • Heat Flow & Thermal Resistance • Selection of Commercial Heat Sink
Custom Heat Sink Design • Applications Circuits and Descriptive Information • Power Supply Design
Data Sheets

48-SERIES MICROPROCESSOR HANDBOOK—1980

The 48-Series Microcomputers • The 48-Series Single-Chip System • The 48-Series Instruction Set
Expanding the 48-Series Microcomputers • Applications for the 48-Series • Development Support
Analog I/O Components • Communications Components • Digital I/O Components • Memory Components
Peripheral Control Components

NATIONAL SEMICONDUCTOR CORPORATION DISTRIBUTORS

ALABAMA

Arrow Electronics
1015 Henderson Rd.
Huntsville, AL 35818
(205) 837-6955

Bell Industries
1031 Putnam Drive, Suite A
Huntsville, AL 35816
(205) 837-1074

Hamilton/Avnet
4940 Research Drive NW
Huntsville, AL 35805
(205) 837-7210
TWX: 810 726 2162

Pioneer Technology
4825 University Square
Huntsville, AL 35805
(205) 837-9300
TWX: 810 726 2197

ARIZONA

Anthem Electronics
1727 E Weber Dr.
Tempe, AZ 85281
(602) 966-6600

Arrow Electronics
4134 East Wood St.
Phoenix, AZ 85040
(602) 437-0750
TWX: 910 951 1550

Bell Industries
1705 W. Fourth St.
Tempe, AZ 85281
(602) 966-7800
TWX: 910 950 0133

Hamilton/Avnet
30 South McKemy
Chandler, AZ 85226
(602) 231-5100
TWX: 66 7450

CALIFORNIA—Northern

Anthem Electronics
1040 East Brokaw Rd.
San Jose, CA 95131
(408) 295-4200
TWX: 910 338 2038

Anthem Electronics
4700 Northgate Blvd.
Suite 165
Sacramento, CA 95834
(916) 922-6800
TWX: 510 101 1419

Arrow Electronics
521 Weddell Drive
Sunnyvale, CA 94089
(408) 745-6600
TWX: 910 339 9371

Bell Industries
1161 North Fairoaks Ave.
Sunnyvale, CA 94086
(408) 734-8570
TWX: 910 339 9378

Bell Industries
500 Giuseppe Ct. Suite 6
Roseville, CA 95678
(916) 969-3100

Hamilton/Avnet
1175 Bordeaux
Sunnyvale, CA 94086
(408) 743-3355
TWX: 910 339 9332

Hamilton/Avnet
4103 Northgate Blvd.
Sacramento, CA 95834
(916) 925-2216

Time Electronics
1339 Moffet Park Dr.
Sunnyvale, CA 94089
(408) 734-9888
TWX: 172233

Zeus Components Inc., Reg 6
N CA/OR/WA/CO/
UT/NE/NM/ & AZ
1580 Old Oakland Rd. #C205
San Jose, CA 95181
(408) 998-5121

CALIFORNIA—Southern

Anthem Electronics
9369 Carroll Park Dr.
San Diego, CA 92121
(619) 453-9005
TWX: 910 335 1515

Anthem Electronics
1 Oldfield Dr.
Irvine, CA 92718
(714) 768-4444
TWX: 910 595 1583

Anthem Electronics
20640 Bahama St.
Chatsworth, CA 91311
(818) 700-1000
TWX: 910 493 2083

Arrow Electronics
9511 Ridgehaven Ct.
San Diego, CA 92123
(619) 565-4800
TWX: 910 335 1195

Arrow Electronics
2961 Dow Ave.
Tustin, CA 92680
(714) 838-5422
TWX: 910 595 2860

Arrow Electronics
19748 Dearborn St.
Chatsworth, CA 91311
(818) 701-7500
TWX: 910 493 2086

Avnet Electronics
350 McCormick Ave.
Irvine Industrial Complex
Costa Mesa, CA 92626
(714) 754-6050
TWX: 910 595 1928

Bell Industries
306 E. Alondra Blvd.
Gardena, CA 90248
(213) 515-1800

Bell Industries
12322 Monarch St.
Garden Grove, CA 92641
(714) 895-7801
TWX: 910 596 2362

Bell Industries
1829 Dehavilland Suite A
Thousand Oaks, CA 91320
(805) 499-6821
TWX: 910 321 3799

Hamilton Electro Sales
3170 Pullman Street
Costa Mesa, CA 92626
(714) 641-4159

Hamilton Electro Sales
9650 DeSoto
Chatsworth, CA 91311
(818) 700-0440

Hamilton/Avnet
1361B West 190th St.
Gardena, CA 90248
(213) 217-6751

Hamilton/Avnet
4545 Viewridge Avenue
San Diego, CA 92123
(619) 571-7510
TWX: 695 415

Hamilton/Avnet
3002 East G Street
Ontario, CA 91764
(714) 989-4602

Time Electronics
370 South Crenshaw Blvd.
Suite E-104
Torrance, CA 90503-1727
(213) 320-0880
TWX: 910 349 6650

Time Electronics
2410 E. Cerritos Ave.
Anaheim, CA 92806
(714) 934-0911
TWX: 910 591 1234

Time Electronics
8525 Arjons Drive
San Diego, CA 92126
(619) 586-1331
TWX: 858902

Time Electronics
9751 Independence Ave.
Chatsworth, CA 91311
(818) 998-7200
TWX: 910 380 6274

Zeus Components Inc., Reg 5
San Fernando Valley
5236 Colodny Drive
Agoura Hills, CA 91301
(818) 889-3838

Zeus Components Inc., Reg 5H
All Hughes
22700 Savy Ranch Pkwy.
Yorba Linda, CA 92686

Zeus Components Inc., Reg 8
S CA, SG VLY, OC, SD CTY
22700 Savy Ranch Pkwy.
Yorba Linda, CA 92686
(714) 921-9000

COLORADO

Anthem Electronics
373 Inverness Dr. South
Englewood, CO 80112
(303) 790-4500

Arrow Electronics
7060 S Tucson Way
Suite 136
Englewood, CO 80112
(303) 790-4444
TWX: 910 931 2626

Bell Industries
8155 W. 48th Avenue
Wheatridge, CO 80033
(303) 424-1985
TWX: 910 938 0393

Hamilton/Avnet
8765 E Orchard Road #708
Englewood, CO 80111
(303) 779-9998
TWX: 910 935 0787

CONNECTICUT

Arrow Electronics
12 Beaumont Rd.
Wallingford, CT 06492
(203) 265-7741
TWX: 710 476 0162

Hamilton/Avnet
Commerce Drive
Commerce Park
Danbury, CT 06810
(203) 797-2800

Anthem Electronics
170 Research Parkway
Meridan, CT 06450
(203) 237-2282

Pioneer Northeast
112 Main St.
Norwalk, CT 06852
(203) 853-1515
TWX: 710 468 3378

Time Electronics
1701 Highland Ave.
Cheshire, CT 06410
(203) 271-3200
TWX: 910 380 6270

FLORIDA

Arrow Electronics
400 Fairway Drive
Deerfield Beach, FL 33441
(305) 429-8200
TWX: 510 955 9456

Arrow Electronics
37 Skyline Drive #3101
Lake Mary, FL 32746
(407) 323-0252

Bell Industries
10810 72nd St. North #201
Suite 201
Largo, FL 33543
(813) 541-4434

Bell Industries
638 South Military Trail
Deerfield Beach, FL 33442
(305) 421-1997

Hamilton/Avnet
6801 N.W. 15th Way
Ft. Lauderdale, FL 33309
(305) 971-2900
TWX: 510 956 3097

Hamilton/Avnet
3197 Tech Drive North
St. Petersburg, FL 33702
(813) 576-3930
TWX: 810 863 0374

Hamilton/Avnet
6947 University Blvd.
Winter Park, FL 32792
(305) 628-3888

Pioneer Technology
221 North Lake Blvd.
Altamonte Springs, FL 32701
(305) 834-9090
TWX: 810 853 0284

Pioneer Technology
674 South Military Trial
Deerfield Beach, FL 33441
(305) 428-8877
TWX: 510 955 9653

NATIONAL SEMICONDUCTOR CORPORATION DISTRIBUTORS (Continued)

FLORIDA (Continued)

Zeus Components Inc., Reg 4
FL, GA, AL, MI, SC & TN
1750 West Broadway
Oviedo, FL 32765
(305) 365-3000

GEORGIA

Arrow Electronics
3155 Northwoods Parkway
Suite A
Norcross, GA 30071
(404) 449-8252
TWX: 810 766 0439

Bell Industries
6690-C Jones Mill Ct.
Norcross, GA 30092
(404) 662-0923

Hamilton/Avnet
5825D Peach Tree Corner E
Norcross, GA 30092
(404) 447-7500

Pioneer Technology
3100F Northwoods Place
Norcross, GA 30071
(404) 448-1711
TWX: 810 766 4515

ILLINOIS

Anthem Electronics
180 Crossen Ave.
Elk Grove Village, IL 60007
(312) 640-6066

Arrow Electronics
1140 West Thorndale Avenue
Itasca, IL 60143
(312) 250-0500
TWX: 910 222 0351

Bell Industries
515 Busse Road
Elk Grove Village, Il 60007
(312) 640-1910
TWX: 910 223 4519

Bell Industries
730 West Kilarney
Urbana, IL 61801
(217) 328-1077

Hamilton/Avnet
1130 Thorndale Ave.
Bensenville, IL 60106
(312) 860-7780

Pioneer Electronics
2171 Executive Dr., Suite 200
Addison, IL 60101
(312) 495-9680
TWX: 910 222 1834

INDIANA

Advent Electronics Inc.
8446 Moller Rd.
Indianapolis, IN 46268
(317) 872-4910
TWX: 810 341 3228

Arrow Electronics
2495 Directors Row
Suite H
Indianapolis, IN 46241
(317) 243-9353
TWX: 810 341 3119

Bell Industries
3606 E. Maumee Ave.
Fort Wayne, IN 46803
(219) 423-3422
TWX: 910 997 0701

Bell Industries—Graham Div.
133 S Pennsylvania St.
Indianapolis, IN 46204
(317) 834-8202
TWX: 810 341 3481

Hamilton/Avnet
485 Gradle Dr.
Carmel, IN 46032
(317) 844-9333
TWX: 810 260 3966

Pioneer-Indiana
6408 Castleplace Drive
Indianapolis, IN 46250
(317) 849-7300

IOWA

Advent Electronics
682 58th Ave. Court S.W.
Cedar Rapids, IA 52404
(319) 363-0221
TWX: 910 525 1337

Arrow Electronics
375 Collins Rd. N.E.
Cedar Rapids, IA 52402
(319) 395-7230
TWX: 910 493 2086

Bell Industries
1221 Park Place N.E.
Cedar Rapids, IA 52402
(319) 395-0730

Hamilton/Avnet
915 33rd Avenue S.W.
Cedar Rapids, IA 52404
(319) 362-4757

KANSAS

Arrow Electronics
8208 Melrose Dr.
Suite 210
Lenexa, KS 66214
(913) 541-9542

Hamilton/Avnet
9219 Quivira Rd
Overland Park, KS 66215
(913) 888-8900

Pioneer Standard
10551 Lackmann Road
Lenexa, KS 66215
(913) 492-0500

MARYLAND

Arrow Electronics
8300 Guilford Dr.
Columbia, MD 21045
(301) 995-0003
TWX: 710 236 9005

Hamilton/Avnet
6822 Oak Hall Lane
Columbia, MD 21045
(301) 995-3500
TWX: 710 862 1861

Anthem Electronics
9020-A Mendenhall Court
Columbia, MD 21045
(301) 964-0040
TWX: 710 862 1909

Pioneer Technology
9100 Gaither Road
Gaithersburg, MD 20877
(301) 921-0660
TWX: 710 828 0545

Time Electronics
9051 Red Branch Rd.
Columbia, MD 21045
(301) 964-3090
TWX: 710 862 2860

Zeus Components Inc., Reg 2
MD, DE, VA, WVA,
NC, RAYTHEON
8930 Route 108
Columbia, MD 21045
(301) 997-1118

MASSACHUSETTS

Arrow Electronics
25 Upton Drive
Wilmington, MA 01887
(617) 935-5134
TWX: 710 393 6770

Gerber Electronics
128 Carnegie Row
Norwood, MA 02062
(617) 769-6000
TWX: 710 336 1987

Hamilton/Avnet
10D Centennial Dr.
Peabody, MA 01960
(617) 531-7430
TWX: 710 393 0382

Anthem Electronics
38 Jonspin Road
Wilmington, MA 01887
(617) 657-5170
TWX: 710 332 1387

Pioneer Northeast
44 Hartwell Avenue
Lexington, MA 02173
(617) 861-9200
TWX: 710 326 6617

Time Electronics
10 A Centennial Drive
Peabody, MA 01960
(617) 532-6200
TWX: 710 393 0171

Zeus Coomponents Inc., Reg 1A
MA, RI, VT, NH, ME & CANADA
429 Marrett Rd.
Lexington, MA 02173
(617) 863-8800

MICHIGAN

Arrow Electronics
3510 Roger Chaffee
Memorial Blvd. S.E.
Grand Rapids, MI 49508
(616) 243-0912

Arrow Electronics
755 Phoenix Dr.
Ann Arbor, MI 48108
(313) 971-8220
TWX: 810 223 6020

Bell Industries
814 Phoenix Dr.
Ann Arbor, MI 48104
(313) 971-9093

Hamilton/Avnet
2215 29th St. S.E.
Grand Rapids, MI 49508
(616) 243-8805
TWX: 810 273 6921

Hamilton/Avnet
32487 Schoolcraft Road
Livonia, MI 48150
(313) 522-4700

Pioneer Standard
4505 Broadmoor S.E.
Grand Rapids, MI 49508
(616) 698-1800
TWX: 510 600 8456

Pioneer Standard
13485 Stanford
Livonia, MI 48150
(313) 525-1800
TWX: 810 242 3271

R. M. Electronics
4310 Roger B Chaffee
Wyoming, MI 49508
(616) 531-9300

MINNESOTA

Anthem Electronics
10025 Valley View Rd. #160
Eden Prairie, MN 55344
(612) 944-5454

Arrow Electronics
5230 73rd Street
Edina, MN 55435
(612) 830-1800
TWX: 910 576 3125

Hamilton/Avnet
12400 Whitewater Dr.
Minnetonka, MN 55343-9421
(612) 932-0600
TWX: 910 572 2867

Pioneer-Twin Cities
7625 Golden Triangle Dr.
Suite G
Eden Prairie, MN 55344
(612) 935-5444
TWx: 910 576 2738

MISSOURI

Arrow Electronics
2380 Schuetz Road
St. Louis, MO 63146
(314) 567-6888
TWX: 910 764 0882

Hamilton/Avnet
13743 Shoreline Ct.-East
Earth City, MO 83045
(314) 344-1200
TWX: 910 762 0627

Time Electronics
330 Sovereign Ct.
St. Louis, MO 63011-4491
(314) 391-6444
TWX: 910 760 1893

NEW HAMPSHIRE

Arrow Electronics
3 Perimeter Rd.
Manchester, NH 03103
(603) 668-6968
TWX: 710 220 1684

Bell Industries—C & H Div.
19 Park Avenue
Hudson, NH 03051
(603) 882-1133
TWX: 710 228 8959

Hamilton/Avnet
444 Industrial Dr.
Manchester, NH 03102
(603) 624-9400

NEW JERSEY—Northern

Arrow Electronics
6 Century Drive
Parsippany, NJ 07054
(201) 575-5300
TWX: 710 734 4403

Hamilton/Avnet
10 Industrial Rd.
Fairfield, NJ 07006
(201) 575-3390
TWX: 710 734 4409

NATIONAL SEMICONDUCTOR CORPORATION DISTRIBUTORS (Continued)

NEW JERSEY—Northern (Continued)

Anthem Electronics
311 Rt. 46 West
Fairfield, NJ 07006
(201) 227-7960
TWX: 710 734 4312

Nu Horizons Electronics
39 Route 46
Pinebrook, NJ 07058
(201) 882-8300

Pioneer
45 Route 46
Pine Brook, NJ 07058
(201) 575-3510
TWX: 710 734 4382

NEW JERSEY—Southern

Arrow Electronics
6000 Lincoln Drive East
Marlton, NJ 08053
(609) 596-8000
TWX: 710 897 0829

Hamilton/Avnet
One Keystone Ave.
Cherry Hill, NJ 08003
(609) 424-0100
TWX: 710 940 0262

NEW MEXICO

Alliance Electronics Inc.
11030 Cochiti S.E.
Albuquerque, NM 87123
(505) 292-3360
TWX: 910 989 1151

Arrow Electronics
2460 Alamo Ave. S.E.
Albuquerque, NM 87106
(505) 243-4566
TWX: 910 989 1679

Bell Industries
11728 Linn N.E.
Albuquerque, NM 87123
(505) 292-2700
TWX: 910 989 0625

Hamilton/Avnet
2524 Baylor Drive S.E.
Albuquerque, NM 87106
(505) 765-1500
TWX: 910 989 1631

NEW YORK—Upstate

Arrow Electronics
3375 Brighton-Henrietta
Townline Rd.
Rochester, NY 14623
(716) 427-0300
TWX: 510 253 4766

Hamilton/Avnet
103 Twin Oaks Drive
Syracuse, NY 13206
(315) 437-2641
TWX: 710 541 1506

Hamilton/Avnet
2060 Town Line Road
Rochester, NY 14623
(716) 475-9130
TWX: 510 253 5470

Pioneer Northeast
68 Corporate Drive
Binghamton, NY 13904
(607) 722-9300
TWX: 510 252 0893

Pioneer Northeast
840 Fairport Rd.
Fairport, NY 14450
(716) 381-7070
TWX: 510 253 7001

Summit Electronics
916 Main Street
Buffalo, NY 14202
(716) 887-2800
TWX: 710 522 1692

Summit Electronics
292 Commerce Drive
Rochester, NY 14623
(716) 334-8110

Time Electronics
6075 Corporate Dr.
East Syracuse, NY 13057
(315) 432-0355
TWX: 510 100 6192

NEW YORK—Metro Area

Arrow Electronics
20 Oser Ave.
Hauppauge, NY 11788
(516) 231-1000
TWX: 510 227 6623

Hamilton/Avnet
833 Motor Parkway
Hauppauge, NY 11788
(516) 434-7413

Hamilton/Avnet Export Div.
1065 Old Country Rd., #211A
Westbury, NY 11590
(516) 997-6868

Anthem Electronics
400 Oser Ave.
Hauppauge, NY 11787
(516) 273-1660
TWX: 510 227 1042

Nu Horizons Electronics
6000 New Horizons Blvd.
Amityville, NY 11701
(516) 226-6000

Pioneer
60 Crossways Park West
Woodbury, NY 11797
(516) 921-8700
TWX: 710 326 6617

Time Electronics
70 Marcus Boulevard
Hauppauge, NY 11788
(515) 273-0100
TWX: 858881

Zeus Components Inc., Reg 1
NY/ROCK/NJ/E PA/ CT
100 Midland Ave.
Port Chester, NY 10573
(914) 937-7400

Zeus Components Inc., Reg 1B
Long Island/NYC
2110 Smithtown Ave.
Ronkonkoma, NY 11779
(516) 737-4500

NORTH CAROLINA

Arrow Electronics
5240 Greens Dairy Rd.
Raleigh, NC 27604
(919) 876-3132
TWX: 510 928 1856

Arrow Electronics
938 Burke Street
Winston-Salem, NC 27101
(919) 725-8711
TWX: 510 931 3169

Hamilton/Avnet
3510 Spring Forest Road
Raleigh, NC 27601
(919) 878-0810
TWX: 510 928 1836

Pioneer Technology
9801-A Southern Pine Blvd.
Charlotte, NC 28210
(704) 527-8188
TWX: 810 621 0366

OHIO

Arrow Electronics
7620 McEwen Rd.
Centerville, OH 45459
(513) 435-5563
TWX: 810 459 1611

Arrow Electronics
6238 Cochran Rd.
Solon, OH 44139
(216) 248-3990
TWX: 810 427 9409

Bell Industries
444 Windsor Park Drive
Dayton, OH 45459
(513) 435-8660

Bell Industries
Micro-Mil Division
118 Westpark Road
Dayton, OH 45459
(513) 434-8231
TWX: 810 459 1615

CAM/OHIO Electronics
749 Miner Road
Highland Heights, OH 44143
(216) 461-4700
TWx: 810 427 2976

Hamilton/Avnet
954 Senate Drive
Dayton, OH 45459
(513) 439-6700
TWX: 810 450 2531

Hamilton/Avnet
30325 Bainbridge Rd., Bldg. A
Solon, OH 44139
(216) 831-3500
TWX: 810 427 9452

Hamilton/Avnet
777 Brooksedge Blvd.
Westerville, OH 43081
(614) 882-7004

Pioneer Standard
4800 East 131st Street
Cleveland, OH 44105
(216) 587-3600
TWX: 810 422 2210

Pioneer Standard
4433 Interpoint Blvd.
Dayton, OH 45424
(513) 236-9900
TWX: 810 459 1683

Zeus Components Inc., Reg 3
Dayton (DESC)
2912 Springboro St., Ste. 106
Dayton, OH 45439
(914) 937-7400

OKLAHOMA

Arrow Electronics
12111 E. 51st Street
Tulsa, OK 74146
(918) 252-7537

Hamilton/Avnet
12121 East 51st St.
Suite 102A
Tulsa, OK 74146
(918) 252-7297

Quality Components
3158 South 108th East Ave.
Suite 274
Tulsa, OK 74146
(918) 664-8812

Radio Inc.
1000 South Main Street
Tulsa, OK 74119
(918) 587-9123
TWX: 49 2429

OREGON

Almac-Stroum Electronics
1885 N.W. 169th Place
Beaverton, OR 97006
(503) 629-8090
TWX: 910 467 8743

Anthem Electronics
9705 S.W. Sunshine Ct.
Suite 900
Beaverton, OR 97005
(503) 643-1114

Arrow Electronics
1800 N.W 167th Place
Suite 145
Beaverton, OR 97006
(503) 645-6456
TWX: 910 464 0007

Bell Industries
6024 S.W. Jean Rd.
Lake Oswego, OR 97034
(503) 241-4115
TWX: 910 455 8177

Hamilton/Avnet
6024 S.W. Jean Rd.
Bldg. C, Suite 10
Lake Oswego, OR 97034
(503) 635-7850

PENNSYLVANIA—Eastern

Arrow Electronics
650 Seco Rd.
Monroeville, PA 15146
(412) 856-7000
TWX: 710 797 3894

CAM/RPC IND Electronics
620 Alpha Drive
RIDC Park
Pittsburgh, PA 15238
(412) 782-3770
TWX: 710 795 3126

Hamilton/Avnet
2800 Liberty Ave.
Pittsburgh, PA 15227
(412) 281-4150

NATIONAL SEMICONDUCTOR CORPORATION DISTRIBUTORS (Continued)

PENNSYLVANIA—Eastern (Continued)

Anthem Electronics
101 Rock Road
Horsham, PA 19044
(215) 443-5150

Pioneer Technology
261 Gibraltar Road
Horsham, PA 19044
(215) 674-4000
TWX: 510 665 6778

Pioneer-Pittsburgh
259 Kappa Drive
Ridgepark
Pittsburgh, PA 15238
(412) 782-2300
TWX: 710 795 3122

Time Electronics
600 Clark Ave.
King of Prussia, PA 19406
(215) 337-0900
TWX: 845317

TENNESSEE

Bell Industries
Instate: (800) 752-2050
Out of State: (800) 433-8301

TEXAS

Arrow Electronics
3220 Commander Dr.
Carrollton, TX 75006
(214) 380-6464
TWX: 910 860 5377

Arrow Electronics
2227 West Braker Lane
Austin, TX 78758
(512) 835-4180
TWX: 910 874 1348

Arrow Electronics
10899 Kinghurst Dr.
Suite 100
Houston, TX 77099
(713) 530-4700
TWX: 910 880 439

Hamilton/Avnet
2111 West Walnut Hill Ln.
Irving, TX 75062
(214) 550-7755
TWX: 07 32359

Hamilton/Avnet
4850 Wright Road #190
Staford, TX 77477
(713) 240-7733
TWX: 910 881 5523

Hamilton/Avnet
1807A West Braker Lane
Austin, TX 78758
(512) 837-8911
TWX: 910 874 1319

Pioneer Electronics
1826 Kramer Lane
Suite D
Austin, TX 78758
(512) 835-4000

Pioneer Standard
13710 Omega Road
Dallas, TX 75240
(214) 386-7300
TWX: 910 860 5563

Pioneer Electronics
5853 Point West Drive
Houston, TX 77036
(713) 988-5555
TWX: 910 881 1606

Quality Components
1005 Industrial Blvd.
Sugarland, TX 77478
(713) 240-2255
TWX: 910 881 7251

Quality Components
2120M Braker Lane
Austin, TX 78758
(512) 835-0220
TWX: 910 874 1377

Quality Components
4257 Kellway Circle
Addison, TX 75001
(214) 733-4300
TWX: 910 660 5459

Zeus Components Inc., Reg 7
TX, AR, OK, LA, KS, MO, IO, NE
1800 N. Glenville Rd.
Richardson, TX 75081
(214) 783-7010

UTAH

Anthem Electronics
1615 West 2200 South #A
Salt Lake City, UT 84119
(801) 973-8555

Arrow Electronics
1946 W. Parkway Blvd.
Salt Lake City, UT 84119
(801) 973-6913

Bell Industries
3639 West 2150 South
Salt Lake City, UT 84120
(801) 972-6969

Hamilton/Avnet
1585 West 2100 South
Salt Lake City, UT 84117
(801) 972-4300
TWX: 910 925 4018

WASHINGTON

Almac-Stroum Electronics
14360 S.E. Eastgate Way
Bellevue, WA 98007
(206) 643-9992
TWX: 910 444 2067

Anthem Electronics
5020 148th Ave. N.E.
Suite 103
Redmond, WA 98052
(206) 881-0850
TWX: 910 997 0118

Arrow Electronics
19450 68th Ave. South
Kent, WA 98032
(206) 575-4420
TWX: 910 444 2034

Hamilton/Avnet
14212 North East 21st
Bellevue, WA 98005
(206) 453-5844

WISCONSIN

Arrow Electronics
200 N. Patrick Blvd.
Brookfield, WI 53005
(414) 792-0150
TWX: 910 262 1193

Bell Industries
W227 N913 Westmound Ave.
Waukesha, WI 53186
(414) 547-8879
TWX: 910 262 1156

Hamilton/Avnet
2975 Moorland Rd.
New Berlin, WI 53151
(414) 784-4516

Taylor Electric
1000 West Donges Bay Road
Mequon, WI 53092
(414) 241-4321
TWX: 910 262 3414

CANADA

Electro Sonic Inc.
1100 Gordon Baker Road
Willowdale, Ontario M2H 3B3
(416) 494-1666
TWX: 06 525295

Hamilton/Avnet
2550 Boundary Rd. #105
Burnaby, B.C., V5M 3Z0
(604) 437-6667

Hamilton/Avnet
2816 21st N.E.
Calgary, Alberta T2E 6Z2
(403) 250-9380
TWX: 03 827642

Hamilton/Avnet
2795 Rue Halpern
St. Laurent, Quebec H4S 1P8
(514) 335-1000
TWX: 610 421 3731

Hamilton/Avnet
6845 Redwood Drive 3, 4, 5
Mississauga, Ontario L4V 1T1
(416) 677-7432
TWX: 610 492 8867

Hamilton/Avnet
190 Colonnade Rd.
Nepean, Ontario K2E 7L5
(613) 226-1700
TWX: 053 4971

Semad Electronics Ltd.
243 Place Frontenac
Pointe Claire, Quebec H9R 4Z7
(514) 694-0860

Semad Electronics Ltd.
3700 Gilmore Way #210
Burnaby, B.C. V5G 4M1
(604) 438-2515

Semad Electronics Ltd.
75 Glendeer Dr. S.E. #210
Calgary, Alberta T2H 2S8
(403) 252-5664

Semad Electronics Ltd.
1827 Woodward Dr. #303
Ottawa, Ontario K2C 0R3
(613) 727-8325

Zentronics
8 Tilbury Ct.
Brampton, Ontario L6T 3T4
(416) 451-9600
TWX: 06 97678

Zentronics
Edmonton Sales Office
Edmonton, Alberta T6N 1B2
(403) 468-8306

Zentronics
11400 Bridgeport Rd., Unit 108
Richmond, B.C. V6X 1T2
(604) 273-5575
TWX: 04 355844

Zentronics
155 Colonade Rd. So.
Units 17 & 18
Nepean, Ontario K2E 7K1
(613) 226-8840

Zentronics
817 McCaffrey St.
Ville St. Laurent, Quebec H4T 1N3
(514) 737-9700

Zentronics
93-1313 Border St.
Winnipeg, Manitoba R3H 0X4
(204) 694-1957

Zentronics
Waterloo Sales Office
Waterloo, Quebec H4T 1N3
(800) 387-2329

Zentronics
Saskatoon Sales Office
Saskatoon, Alberta R3H 0X4
(306) 955-2207

Zentronics
6815 8th St. N.E.
Suite 100
Calgary, Alberta T2E 7H7
(403) 272-1021
TWX: 04 355844

SALES OFFICES

ALABAMA
Huntsville
(205) 837-8960
(205) 721-9367

ARIZONA
Tempe
(602) 966-4563

B.C.
Burnaby
(604) 435-8107

CALIFORNIA
Encino
(818) 888-2602
Inglewood
(213) 645-4226
Roseville
(916) 786-5577
San Diego
(619) 587-0666
Santa Clara
(408) 562-5900
Tustin
(714) 259-8880
Woodland Hills
(818) 888-2602

COLORADO
Boulder
(303) 440-3400
Colorado Springs
(303) 578-3319
Englewood
(303) 790-8090

CONNECTICUT
Fairfield
(203) 371-0181
Hamden
(203) 288-1560

FLORIDA
Boca Raton
(305) 997-8133
Orlando
(305) 629-1720
St. Petersburg
(813) 577-1380

GEORGIA
Atlanta
(404) 396-4048
Norcross
(404) 441-2740

ILLINOIS
Schaumburg
(312) 397-8777

INDIANA
Carmel
(317) 843-7160
Fort Wayne
(219) 484-0722

IOWA
Cedar Rapids
(319) 395-0090

KANSAS
Overland Park
(913) 451-8374

MARYLAND
Hanover
(301) 796-8900

MASSACHUSETTS
Burlington
(617) 273-3170
Waltham
(617) 890-4000

MICHIGAN
W. Bloomfield
(313) 855-0166

MINNESOTA
Bloomington
(612) 835-3322
(612) 854-8200

NEW JERSEY
Paramus
(201) 599-0955

NEW MEXICO
Albuquerque
(505) 884-5601

NEW YORK
Endicott
(607) 757-0200
Fairport
(716) 425-1358
(716) 223-7700
Melville
(516) 351-1000
Wappinger Falls
(914) 298-0680

NORTH CAROLINA
Cary
(919) 481-4311

OHIO
Dayton
(513) 435-6886
Highland Heights
(216) 442-1555
(216) 461-0191

ONTARIO
Mississauga
(416) 678-2920
Nepean
(404) 441-2740
(613) 596-0411
Woodbridge
(416) 746-7120

OREGON
Portland
(503) 639-5442

PENNSYLVANIA
Horsham
(215) 675-6111
Willow Grove
(215) 657-2711

PUERTO RICO
Rio Piedias
(809) 758-9211

QUEBEC
Dollard Des Ormeaux
(514) 683-0683
Lachine
(514) 636-8525

TEXAS
Austin
(512) 346-3990
Houston
(713) 771-3547
Richardson
(214) 234-3811

UTAH
Salt Lake City
(801) 322-4747

WASHINGTON
Bellevue
(206) 453-9944

WISCONSIN
Brookfield
(414) 782-1818
Milwaukee
(414) 527-3800

National Semiconductor

National Semiconductor
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: (408) 721-5000
TWX: (910) 339-9240

SALES OFFICES (Continued)

INTERNATIONAL OFFICES

Electronica NSC de Mexico SA
Juventino Rosas No. 118-2
Col Guadalupe Inn
Mexico, 01020 D.F. Mexico
Tel: 52-5-524-9402

National Semicondutores Do Brasil Ltda.
Av. Brig. Faria Lima, 1409
6 Andar Salas 62/64
01451 Sao Paulo, SP, Brasil
Tel: (55/11) 212-5066
Telex: 391-1131931 NSBR BR

National Semiconductor GmbH
Industriestrasse 10
D-8080 Furstenfeldbruck
West Germany
Tel: 49-08141-103-0
Telex: 527 649

National Semiconductor (UK) Ltd.
301 Harpur Centre
Horne Lane
Bedford MK40 ITR
United Kingdom
Tel: (02 34) 27 00 27
Telex: 826 209

National Semiconductor Benelux
Vorstlaan 100
B-1170 Brussels
Belgium
Tel: (02) 6725360
Telex: 61007

National Semiconductor (UK) Ltd.
1, Bianco Lunos Alle
DK-1868 Fredriksberg C
Denmark
Tel: (01) 213211
Telex: 15179

National Semiconductor
Expansion 10000
28, rue de la Redoute
F-92260 Fontenay-aux-Roses
France
Tel: (01) 46 60 81 40
Telex: 250956

National Semiconductor S.p.A.
Strada 7, Palazzo R/3
20089 Rozzano
Milanofiori
Italy
Tel: (02) 8242046/7/8/9

National Semiconductor AB
Box 2016
Stensatravagen 13
S-12702 Skarholmen
Sweden
Tel: (08) 970190
Telex: 10731

National Semiconductor
Calle Agustin de Foxa, 27
28036 Madrid
Spain
Tel: (01) 733-2958
Telex: 46133

National Semiconductor Switzerland
Alte Winterthurerstrasse 53
Postfach 567
Ch-8304 Wallisellen-Zurich
Switzerland
Tel: (01) 830-2727
Telex: 59000

National Semiconductor
Kauppakartanonkatu 7
SF-00930 Helsinki
Finland
Tel: (0) 33 80 33
Telex: 126116

National Semiconductor Japan Ltd.
Sanseido Bldg. 5F
4-15 Nishi Shinjuku
Shinjuku-ku
Tokyo 160 Japan
Tel: 3-299-7001
Fax: 3-299-7000

National Semiconductor Hong Kong Ltd.
Southeast Asia Marketing
Austin Tower, 4th Floor
22-26A Austin Avenue
Tsimshatsui, Kowloon, H.K.
Tel: 852 3-7243645
Cable: NSSEAMKTG
Telex: 52996 NSSEA HX

National Semiconductor (Australia) PTY, Ltd.
1st Floor, 441 St. Kilda Rd.
Melbourne, 3004
Victory, Australia
Tel: (03) 267-5000
Fax: 61-3-2677458

National Semiconductor (PTE), Ltd.
200 Cantonment Road 13-01
Southpoint
Singapore 0208
Tel: 2252226
Telex: RS 33877

National Semiconductor (Far East) Ltd.
Taiwan Branch
P.O. Box 68-332 Taipei
7th Floor, Nan Shan Life Bldg.
302 Min Chuan East Road,
Taipei, Taiwan R.O.C.
Tel: (86) 02-501-7227
Telex: 22837 NSTW
Cable: NSTW TAIPEI

National Semiconductor (Far East) Ltd.
Korea Office
Room 612,
Korea Fed. of Small Bus. Bldg.
16-2, Yoido-Dong,
Youngdeungpo-Ku
Seoul, Korea
Tel: (02) 784-8051/3 – 785-0696-8
Telex: K24942 NSRKLO

 TL2432 RRD-RRD68M078/Printed in U.S.A.