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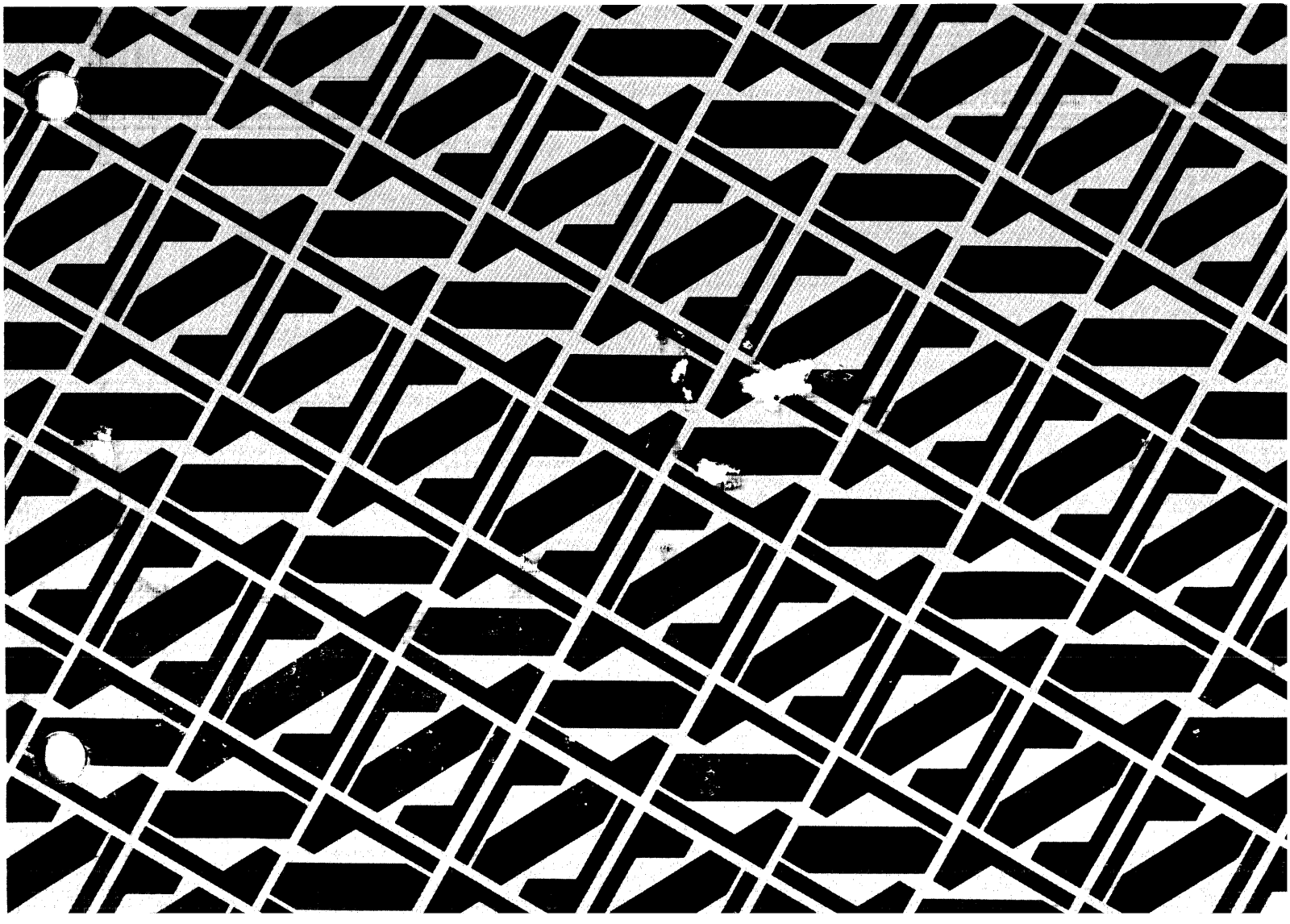
IMP-16P Users Manual

Volume 2



Order Number IMP-16P/937A
Publication Number 4200037A

IMP-16P MICROCOMPUTER

IMP-16P
USERS MANUAL
VOLUME 2

October 1974

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2900 Semiconductor Drive
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PREFACE

Volume 2 of the IMP-16P Users Manual contains detailed block, timing, and schematic diagrams to assist the user in tutorial or maintenance endeavors. The detailed functional descriptions contained in volume 1, chapter 7, of this manual are written to the detailed functional block and timing diagrams contained in volume 2. The small numbers within squares located in the functional blocks of the block diagrams designate the associated schematic sheet number.

Appendix A is a list of all mnemonics used in both volumes 1 and 2. Appendix B is a compilation of the circuit diagrams of the various devices appearing in the schematic diagrams of the IMP-16P. Appendixes A and B follow the illustrations in volume 2.

The material in this manual is subject to change without notice. Circuit details and other data supplied with the engineering documentation that accompany equipment take precedence over the information contained in this manual.

Copies of this manual and other National Semiconductor publications may be obtained from the sales offices listed on the back cover.

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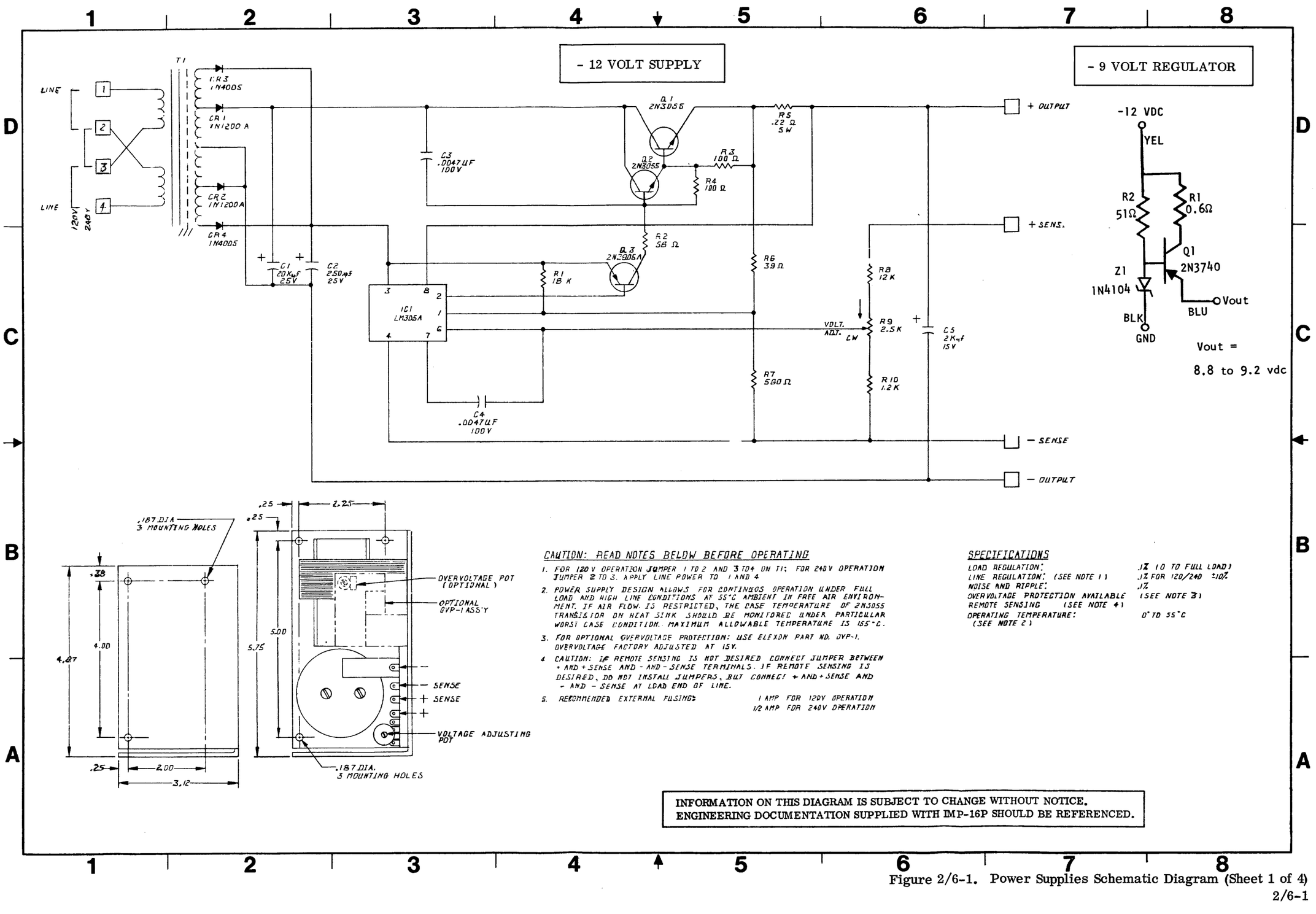


CAUTION: READ NOTES BELOW BEFORE OPERATING

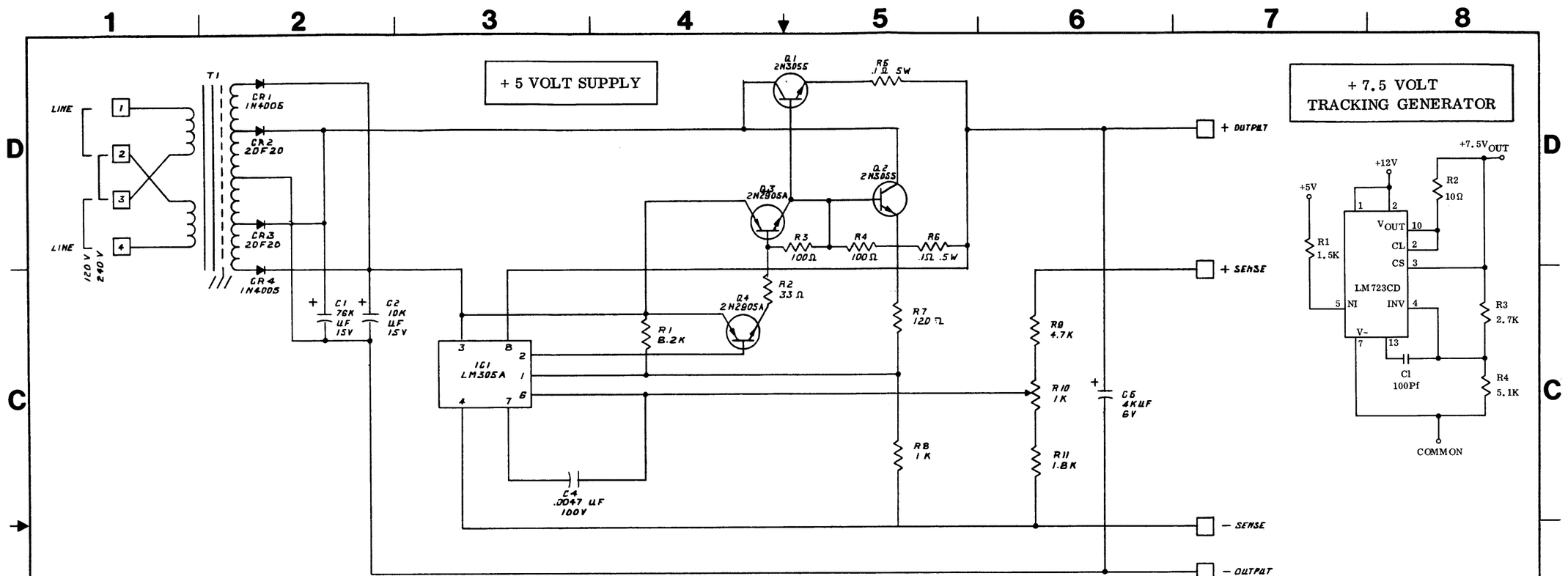
1. FOR 120 V OPERATION JUMPER 1 TO 2 AND 3 TO 4 ON T1; FOR 240V OPERATION JUMPER 2 TO 3. APPLY LINE POWER TO 1 AND 4.
2. POWER SUPPLY DESIGN ALLOWS FOR CONTINUOS OPERATION UNDER FULL LOAD AND HIGH LINE CONDITIONS AT 55°C AMBIENT IN FREE AIR ENVIRONMENT. IF AIR FLOW IS RESTRICTED, THE CASE TEMPERATURE OF 2N3055 TRANSISTOR ON HEAT SINK SHOULD BE MONITORED UNDER PARTICULAR WORST CASE CONDITION. MAXIMUM ALLOWABLE TEMPERATURE IS 155°C.
3. FOR OPTIONAL OVERVOLTAGE PROTECTION: USE ELEXON PART NO. OVP-1. OVERVOLTAGE FACTORY ADJUSTED AT 15V.
4. CAUTION: IF REMOTE SENSING IS NOT DESIRED CONNECT JUMPER BETWEEN + AND + SENSE AND - AND - SENSE TERMINALS. IF REMOTE SENSING IS DESIRED, DO NOT INSTALL JUMPERS, BUT CONNECT + AND + SENSE AND - AND - SENSE AT LOAD END OF LINE.
5. RECOMMENDED EXTERNAL FUSING: 1 AMP FOR 120V OPERATION; 1/2 AMP FOR 240V OPERATION

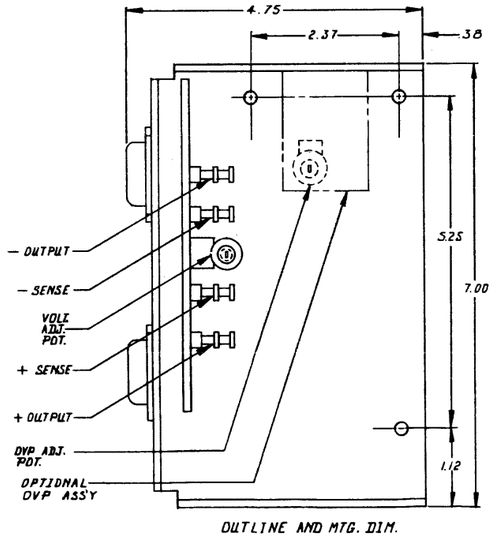
SPECIFICATIONS

LOAD REGULATION:	.1% (0 TO FULL LOAD)
LINE REGULATION: (SEE NOTE 1)	.1% FOR 120/240 ±10%
NOISE AND RIPPLE:	.1%
OVERVOLTAGE PROTECTION AVAILABLE	(SEE NOTE 3)
REMOTE SENSING (SEE NOTE 4)	
OPERATING TEMPERATURE: (SEE NOTE 2)	0° TO 55°C

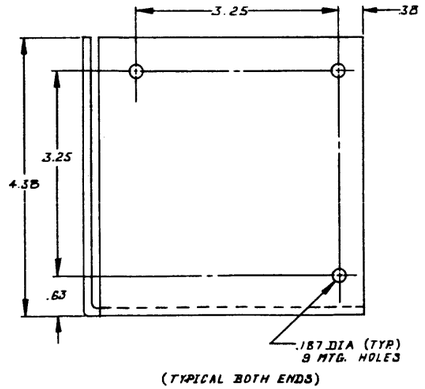
INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE.
ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

Figure 2/6-1. Power Supplies Schematic Diagram (Sheet 1 of 4)





OUTLINE AND MTG. DIM.



(TYPICAL BOTH ENDS)

CAUTION: READ NOTES BELOW BEFORE OPERATING

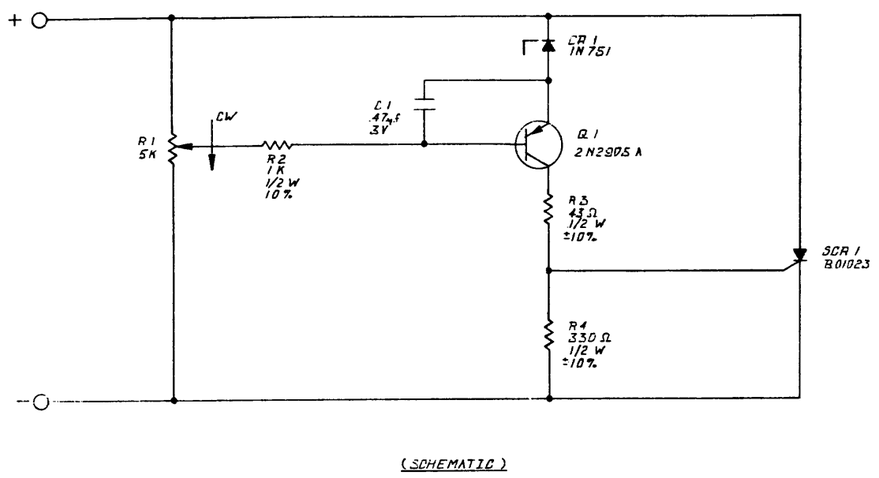
1. FOR 120V OPERATION JUMPER 1 TO 2 AND 3 TO 4 ON T1; FOR 240V OPERATION JUMPER 2 TO 3. APPLY LINE POWER TO 1 AND 4.
2. POWER SUPPLY DESIGN ALLOWS FOR CONTINUOS OPERATION UNDER FULL LOAD AND HIGH LINE CONDITIONS AT 55°C IN AMBIENT IN FREE AIR ENVIRONMENT. IF AIR FLOW IS RESTRICTED THE CASE TEMPERATURE OF 2N3055 TRANSISTOR ON HEAT SINK SHOULD BE MONITORED UNDER PARTICULAR WORST CASE CONDITIONS. MAXIMUM ALLOWABLE TEMPERATURE IS 155°C.
3. FOR OPTIONAL OVERVOLTAGE PROTECTION: USE ELEXON PART NO. OVP 2. OVERVOLTAGE FACTORY ADJUSTED AT 6.V.
4. CAUTION: IF REMOTE SENSING IS NOT DESIRED, CONNECT JUMPER BETWEEN + AND + SENSE AND - AND - SENSE TERMINALS. IF REMOTE SENSING IS DESIRED, DO NOT INSTALL JUMPERS, BUT CONNECT + AND + SENSE AND - AND - SENSE AT LOAD END OF LINE.
5. RECOMMENDED EXTERNAL FUSING:
   1.5 AMP FOR 120V OPERATION
   .75 AMP FOR 240V OPERATION

SPECIFICATIONS

LOAD REGULATION:	.1% (0 TO FULL LOAD)
LINE REGULATION: (SEE NOTE 1)	.1% FOR 120/240 ±10%
NOISE AND RIPPLE:	.1%
OVERVOLTAGE PROTECTION AVAILABLE (SEE NOTE 3)	
REMOTE SENSING	(SEE NOTE 4)
OPERATING TEMPERATURE: (SEE NOTE 2)	0 TO 55°C

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE.
ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

Figure 2/6-1. Power Supplies Schematic Diagram (Sheet 2 of 4)



(SCHEMATIC)

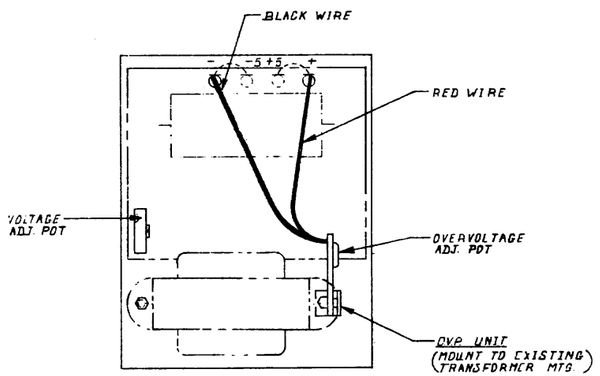
O.V.P-1
OVERVOLTAGE PROTECTION

SPECIFICATIONS:

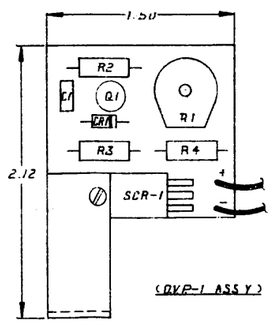
ADJUSTMENT RANGE: 8V TO 30V
CURRENT RATING : 3 AMPS

NOTES:

1. MOUNT TO POWER SUPPLY AS SHOWN IN FIG. 2
2. CONNECT: RED WIRE TO + TERMINAL
   BLACK WIRE TO -TERMINAL
   + TO + SENSE } (CLIP LEAD IF TEMPORARY)
   - TO - SENSE }
3. TURN O.V.P. POT FULL COUNTER-CLOCKWISE.
4. SET POWER SUPPLY OUTPUT VOLTAGE TO DESIRED OVERVOLTAGE LIMIT. (SEE CHART, FIG. 4)
5. TURN O.V.P. POT SLOWLY CLOCKWISE UNTIL SCR FIRES. (VOLTAGE DROPS TO APPROX. 1 VOLT.)
6. TURN POWER OFF.
7. TURN POWER SUPPLY VOLTAGE CONTROL FULL COUNTER-CLOCKWISE.
8. REAPPLY POWER AND READJUST POWER SUPPLY VOLTAGE TO NORMAL OUTPUT.



(O.V.P-1 MTG.)

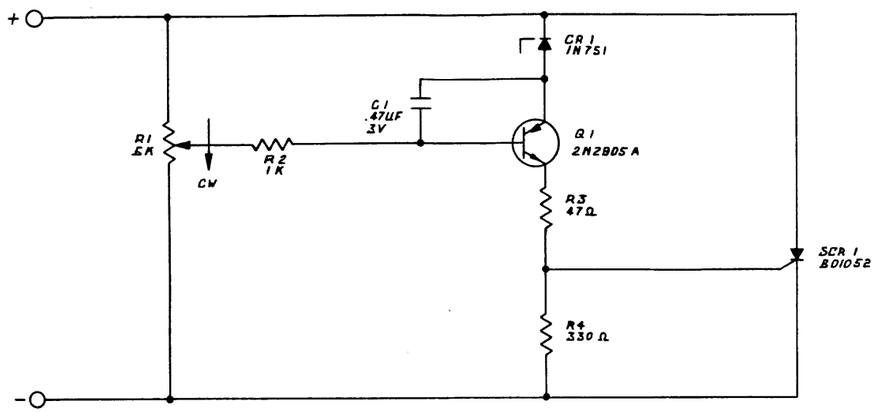


(O.V.P-1 ASS'Y)

RECOMMENDED O.V.P. SETTING			
OUTPUT	O.V.P. LIMIT	OUTPUT	O.V.P. LIMIT
3	6.0	14	17
4	6.0	15	18
5	6.5	16	19
6	7.5	18	21
8	10	20	24
9	11	22	26
10	12.5	24	29
12	15		

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE.
ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

Figure 2/6-1. Power Supplies Schematic Diagram (Sheet 3 of 4)



(SCHEMATIC)

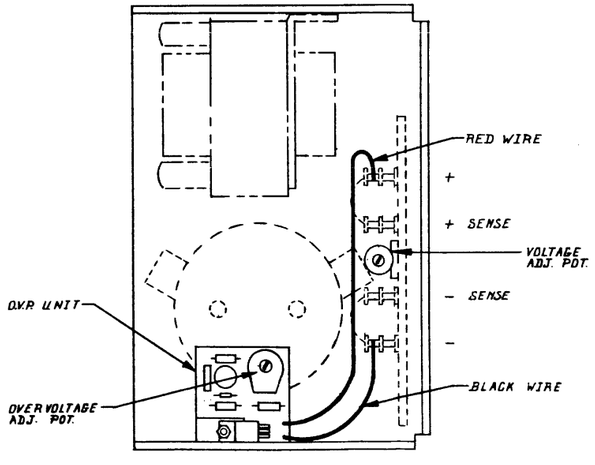
OVP-1
OVERVOLTAGE PROTECTION

SPECIFICATIONS:

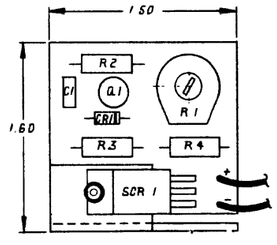
ADJUSTMENT RANGE: 6V TO 30V
CURRENT RATING: 8 AMPS

NOTES:

1. MOUNT TO POWER SUPPLY AS SHOWN IN FIG. 2
2. CONNECT: RED WIRE TO + TERMINAL
   BLACK WIRE TO - TERMINAL
   + TO + SENSE } CLIP LEAD IF TEMPORARY
   - TO - SENSE }
3. TURN OVP POT FULL COUNTER CLOCKWISE
4. SET POWER SUPPLY OUTPUT VOLTAGE TO DESIRED OVERVOLTAGE LIMIT (SEE CHART FIG 4)
5. TURN OVP POT SLOWLY CLOCKWISE UNTIL SCR FIRES. (VOLTAGE DROPS TO APPROX. 1 VOLT.)
6. TURN POWER OFF.
7. TURN POWER SUPPLY VOLTAGE CONTROL FULL COUNTER CLOCKWISE.
8. REAPPLY POWER AND READJUST POWER SUPPLY VOLTAGE TO NORMAL OUTPUT.



(OVP-2 MTG.)

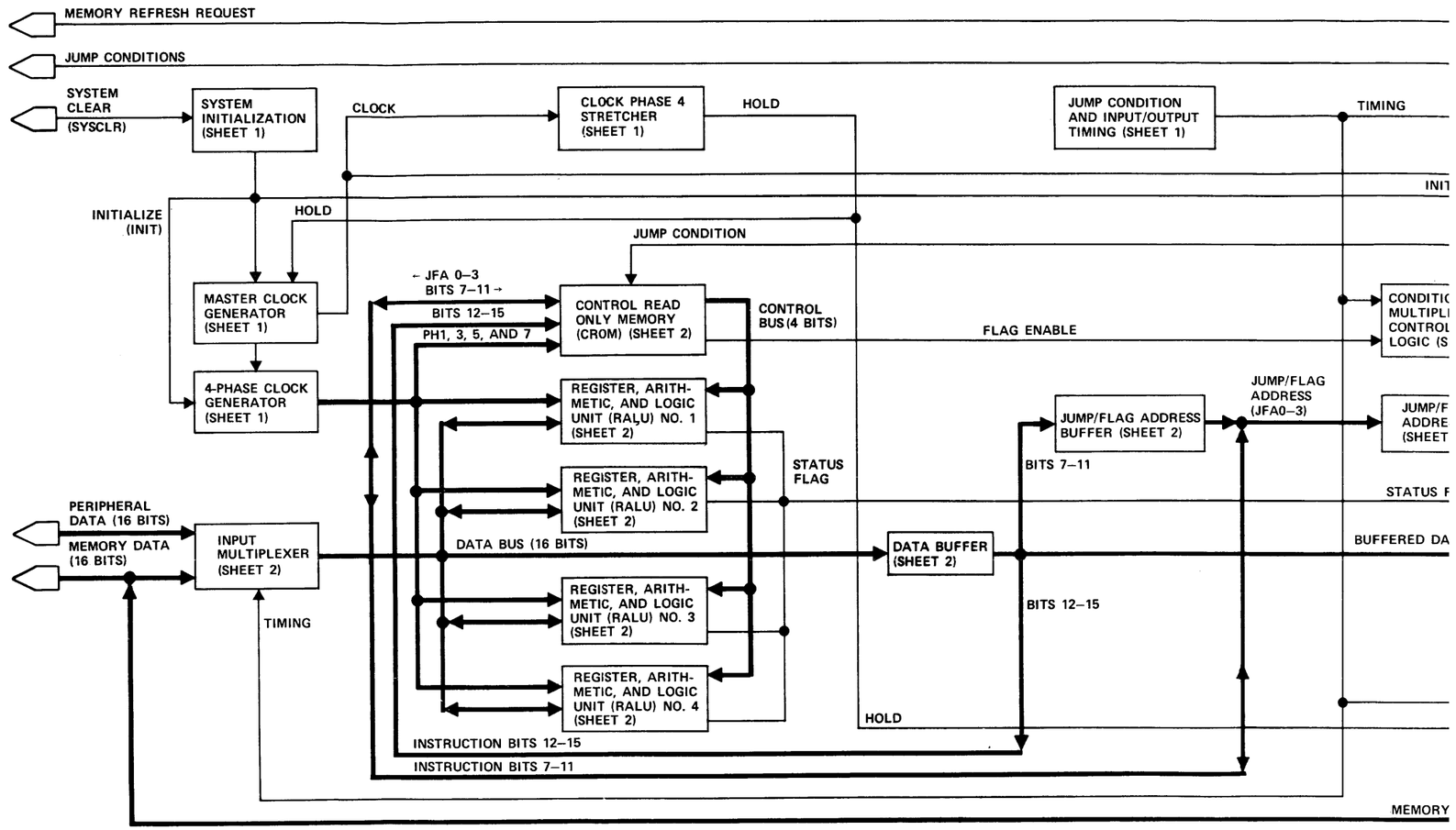


(OVP-2 ASS'Y)

RECOMMENDED OVP SETTINGS			
OUTPUT	OVP LIMIT	OUTPUT	OVP LIMIT
3	5.0	14	17
4	6.0	15	18
5	6.5	16	19
6	7.5	18	21
8	10	20	24
9	11	22	26
10	12.5	24	29
12	15		

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE.
ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

Figure 2/6-1. Power Supplies Schematic Diagram (Sheet 4 of 4)



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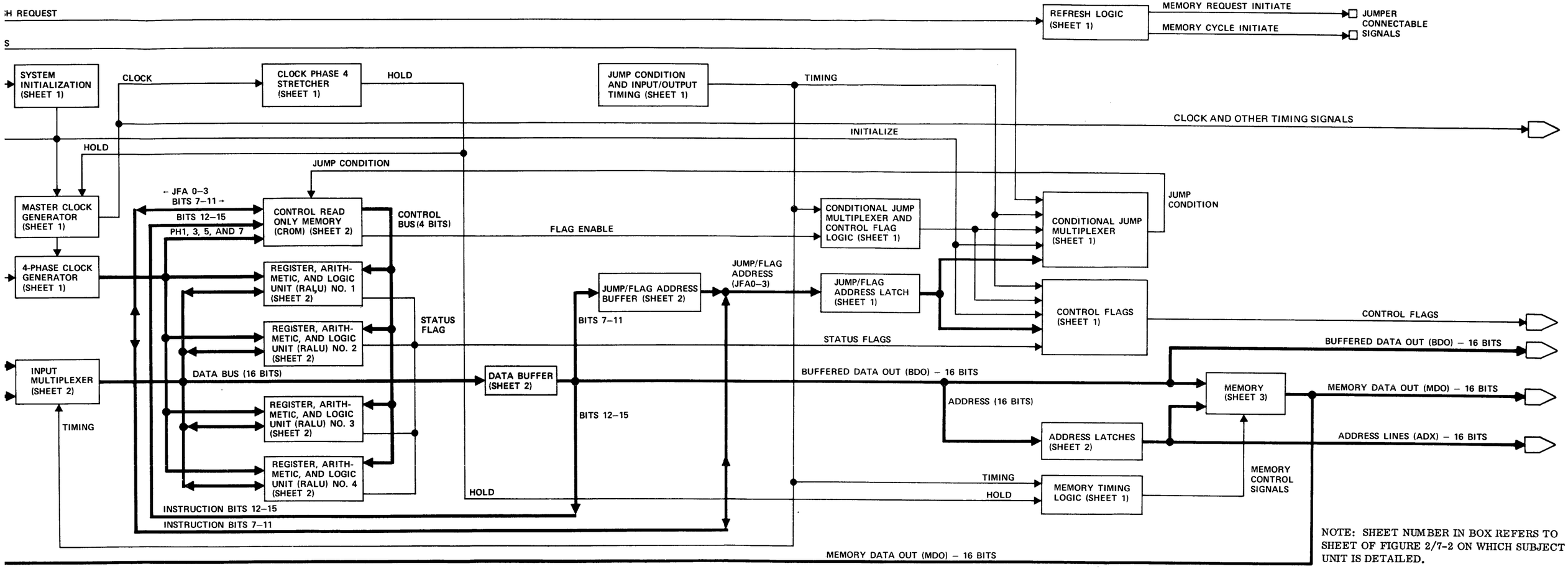
ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REF



NOTE: SHEET NUMBER IN BOX REFERS TO SHEET OF FIGURE 2/7-2 ON WHICH SUBJECT UNIT IS DETAILED.

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE.
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Figure 2/7-1. IMP-16C Functional Block Diagram

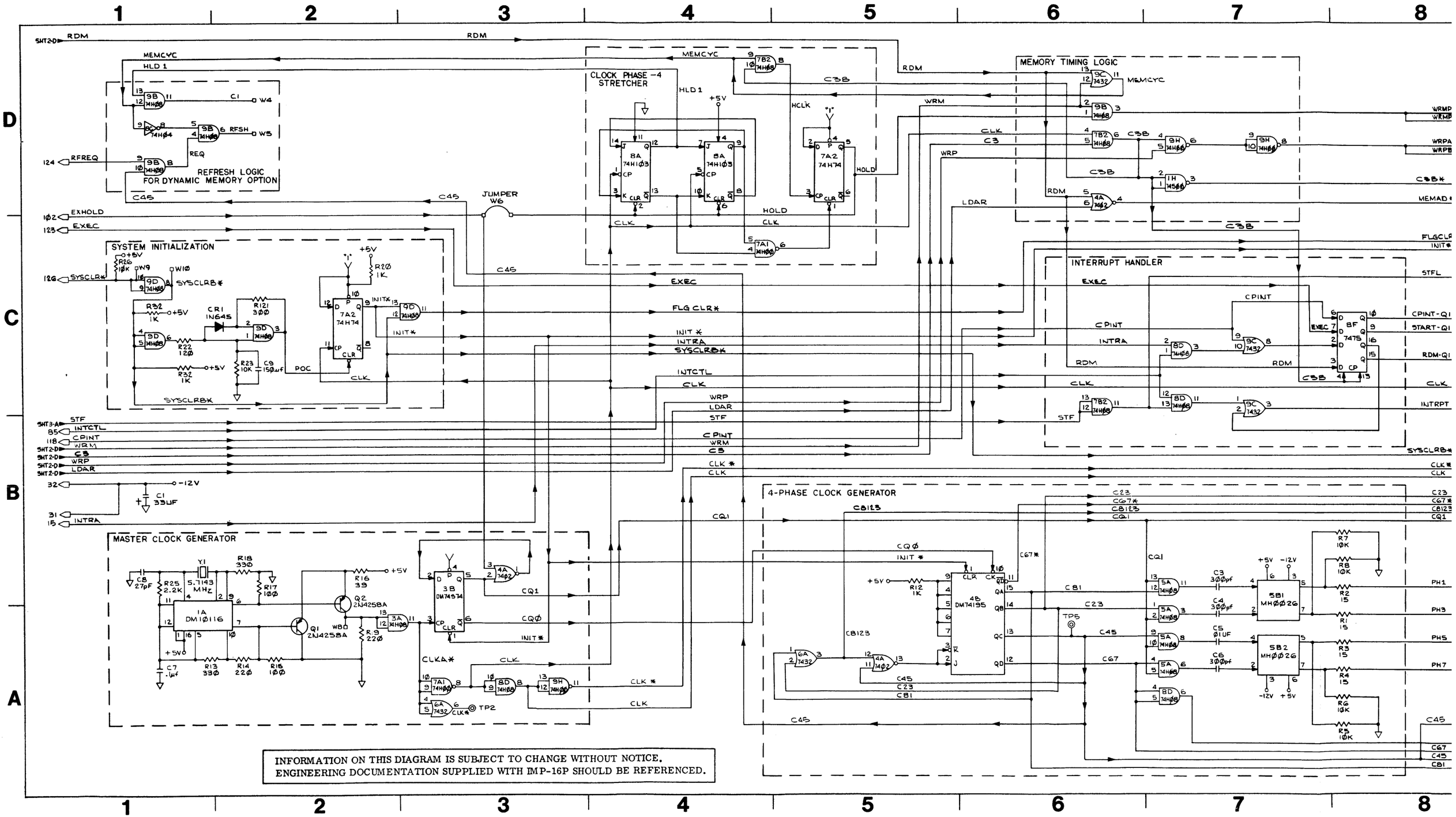
REFRESH LOGIC FOR DYNAMIC MEMORY OPTION
CLOCK PHASE -4 STRETCHER
MEMORY TIMING LOGIC
SYSTEM INITIALIZATION
INTERRUPT HANDLER
MASTER CLOCK GENERATOR
4-PHASE CLOCK GENERATOR
JUMPER W6
INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE.
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Figure 2/7-2.

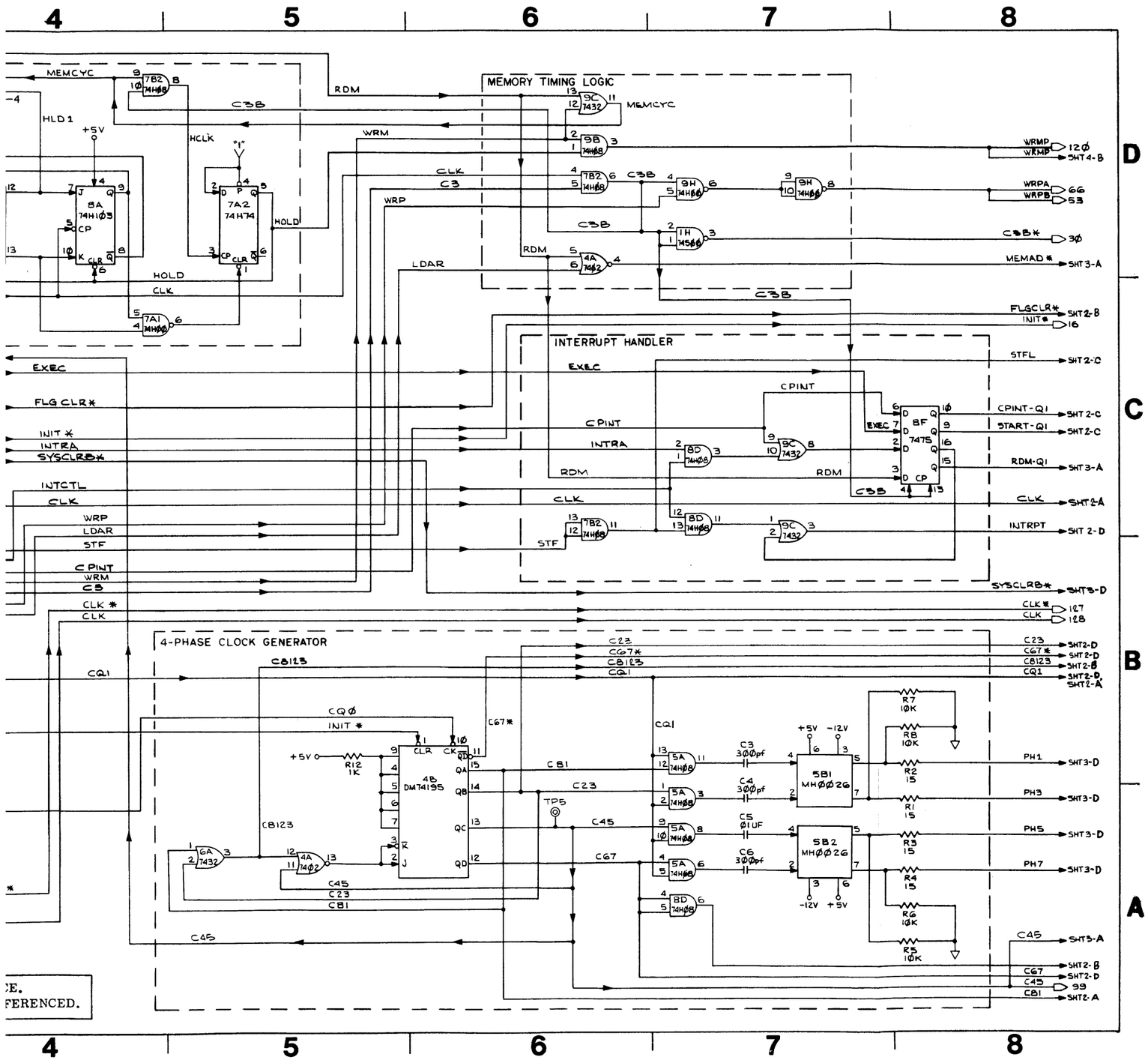


Figure 2/7-2. IMP-16C Schematic Diagram
(Sheet 1 of 4)

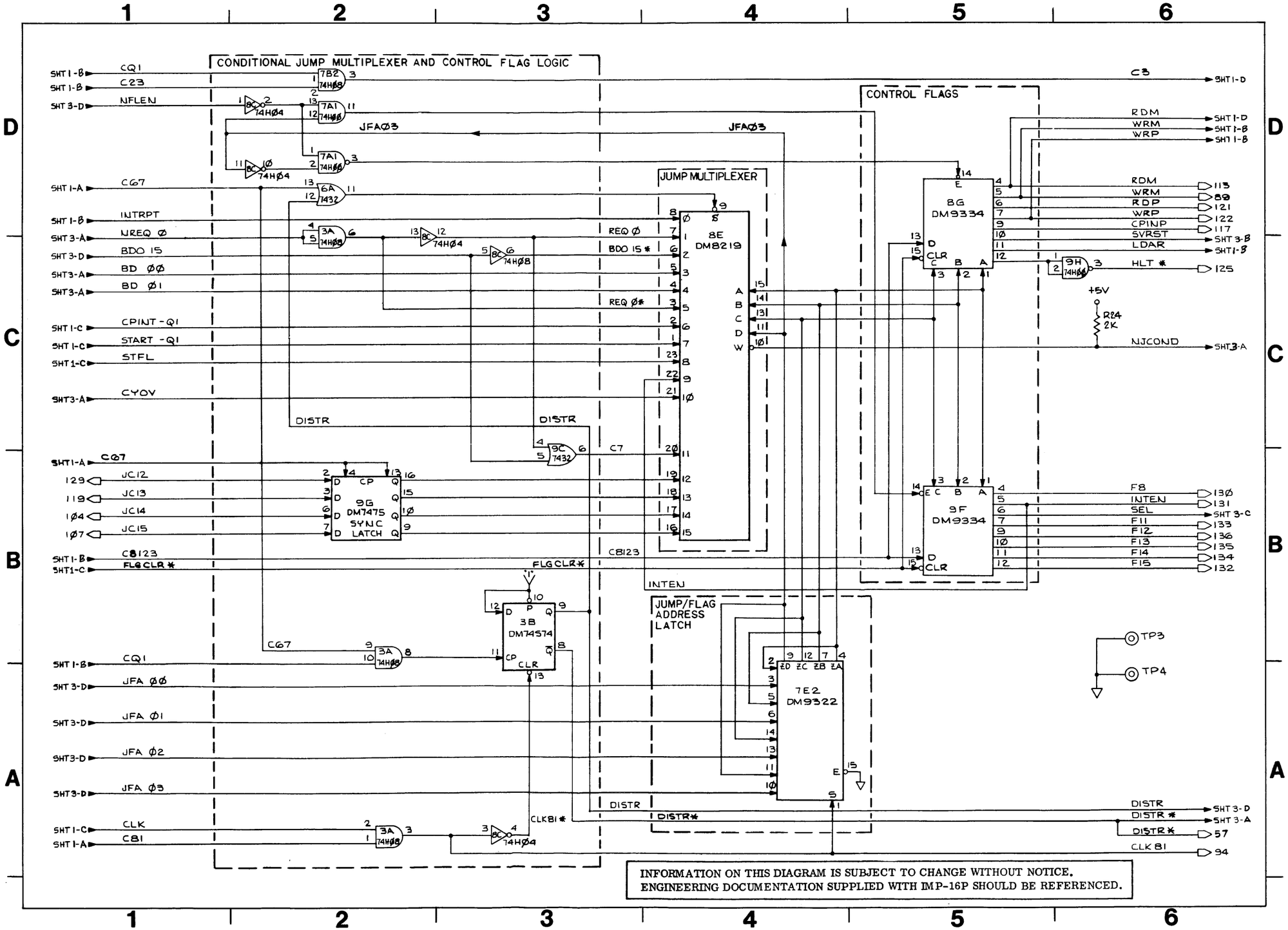


Figure 2/7-2. IMP-16C Schematic Diagram (Sheet 2 of 4)

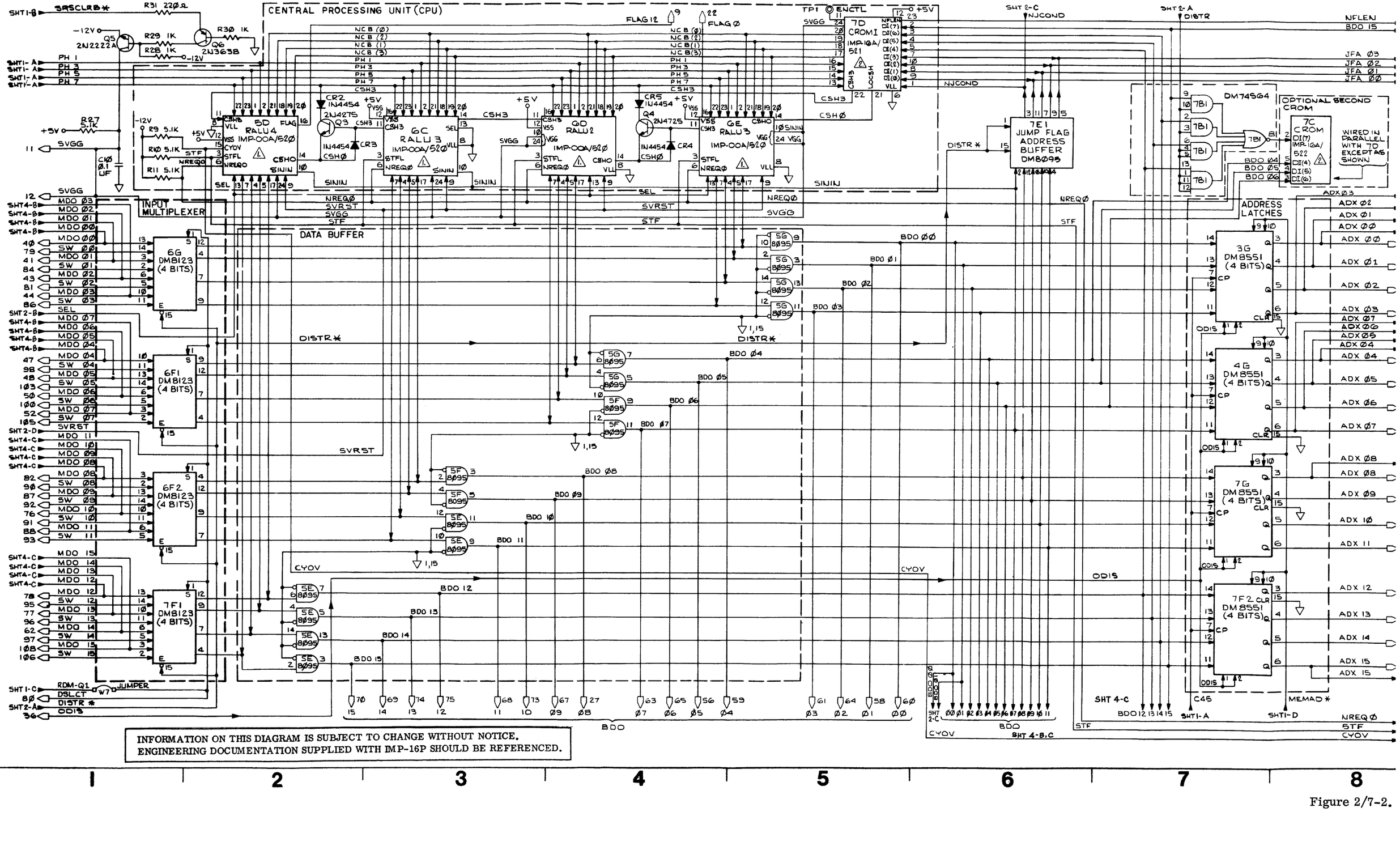

CENTRAL PROCESSING UNIT (CPU)
INPUT MULTIPLEXER
DATA BUFFER
ADDRESS LATCHES
OPTIONAL SECOND CROM
5D RALU4 IMP-00A/52Ø
6C RALU3 IMP-00A/52Ø
6D RALU2 IMP-00A/52Ø
6E RALU3 IMP-00A/52Ø
7D CROMI IMP-16A/521
7E1 JUMP FLAG ADDRESS BUFFER DM8095
7C CROM IMP-16A/522
6G DM8123 (4 BITS)
6F1 DM8123 (4 BITS)
6F2 DM8123 (4 BITS)
7F1 DM8123 (4 BITS)
3G DM8551 (4 BITS)
4G DM8551 (4 BITS)
7G DM8551 (4 BITS)
7F2 DM8551 (4 BITS)
DM74S64
INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE.
ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

Figure 2/7-2.

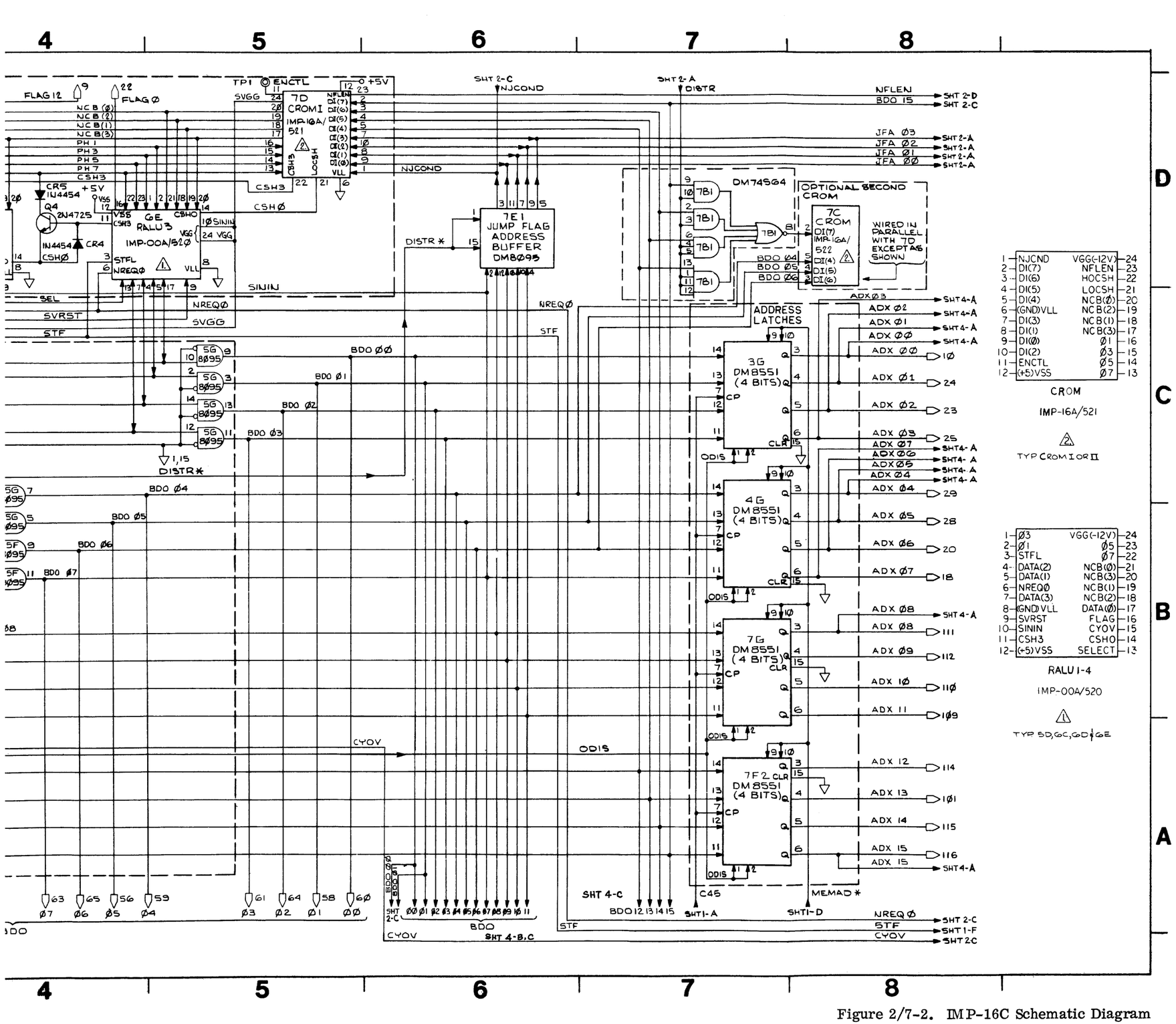


Figure 2/7-2. IMP-16C Schematic Diagram
(Sheet 3 of 4)

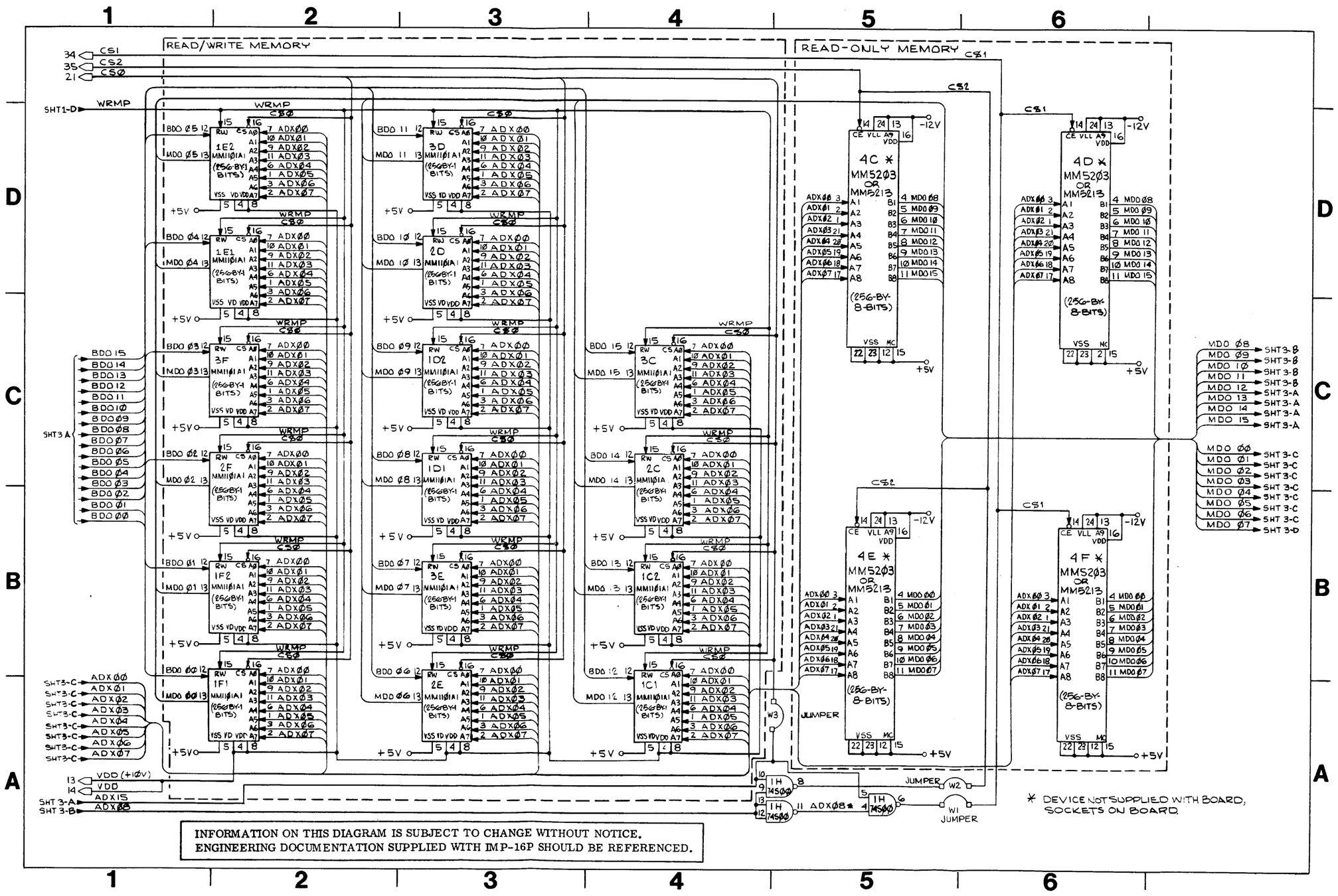
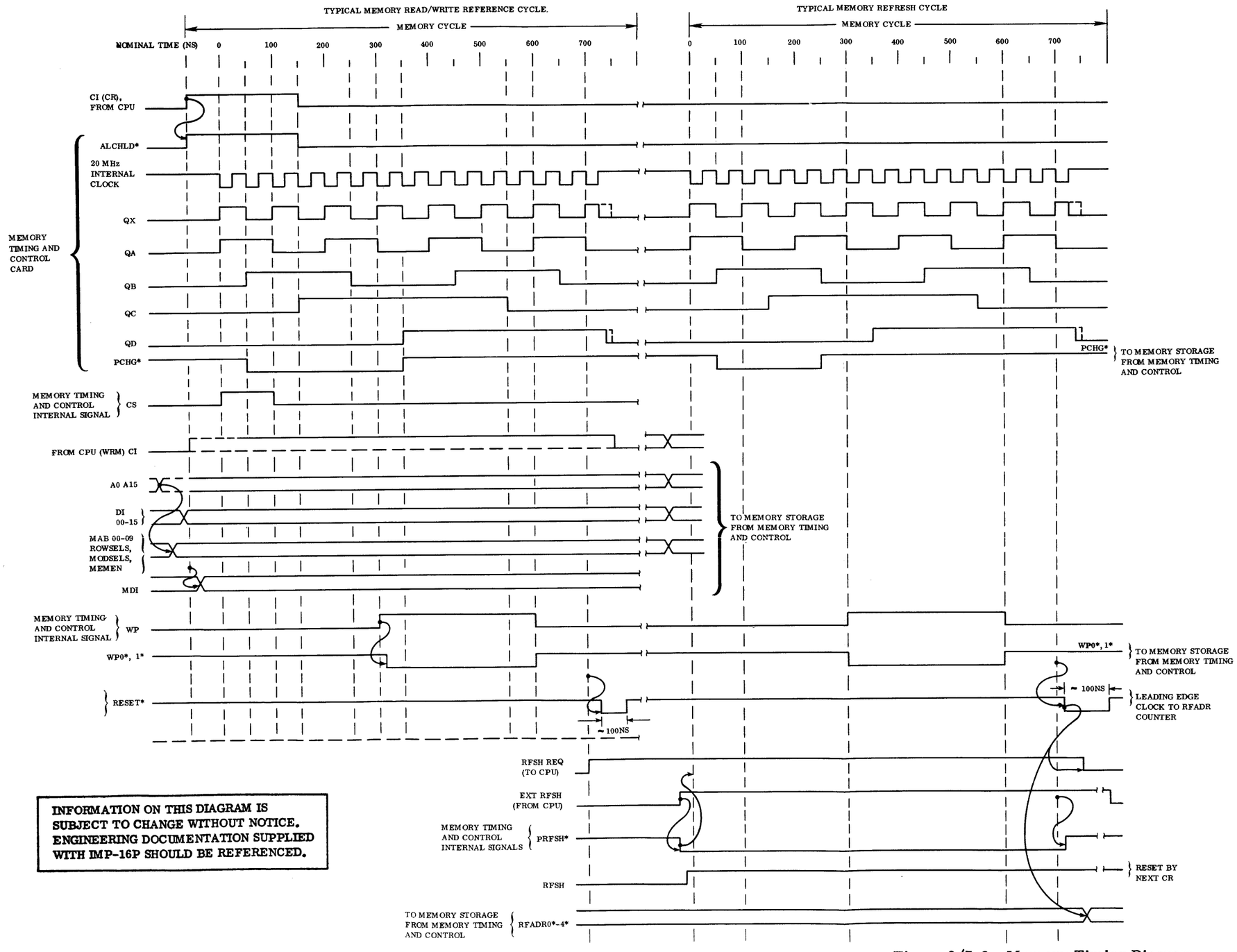
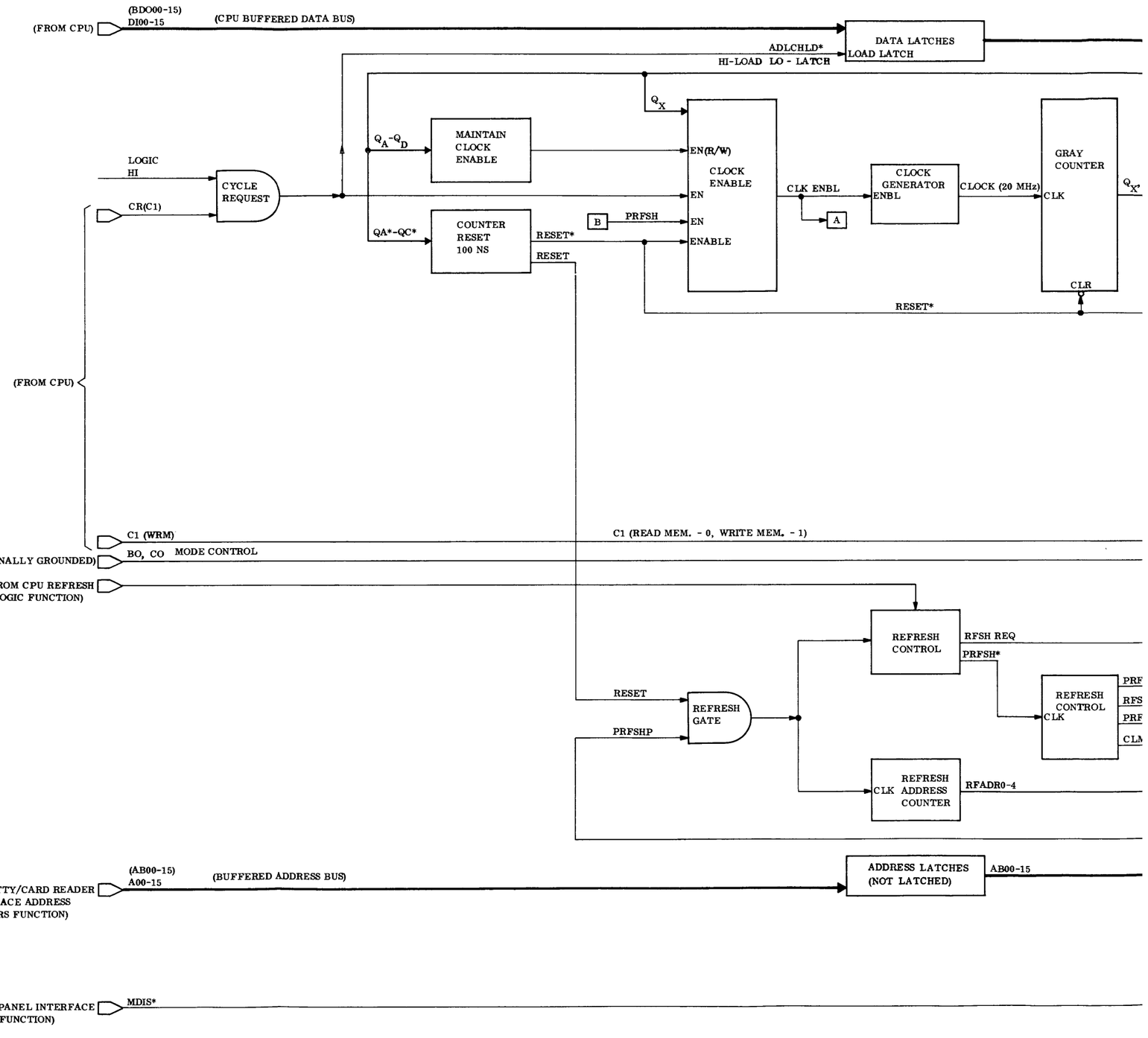


Figure 2/7-2. IMP-16C Schematic Diagram (Sheet 4 of 4)



INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

Figure 2/7-3. Memory Timing Diagram


(FROM CPU)
(BDO00-15)
DI00-15
(CPU BUFFERED DATA BUS)
DATA LATCHES
LOAD LATCH
ADLCHLD*
HI-LOAD LO - LATCH
Q_X
Q_A-Q_D
MAINTAIN
CLOCK
ENABLE
EN(R/W)
CLOCK
ENABLE
EN
ENABLE
LOGIC
HI
CYCLE
REQUEST
CR(C1)
QA*-QC*
COUNTER
RESET
100 NS
B
PRFSH
RESET*
RESET
CLK ENBL
A
CLOCK
GENERATOR
ENBL
CLOCK (20 MHz)
GRAY
COUNTER
CLK
CLR
RESET*
(FROM CPU)
C1 (WRM)
C1 (READ MEM. - 0, WRITE MEM. - 1)
(EXTERNALLY GROUNDED)
BO, CO
MODE CONTROL
(FROM CPU REFRESH
LOGIC FUNCTION)
REFRESH
CONTROL
RFSH REQ
PRFSH*
RESET
REFRESH
GATE
PRFSHP
REFRESH
CONTROL
CLK
REFRESH
CLK ADDRESS
COUNTER
RFADR0-4
(FROM TTY/CARD READER
INTERFACE ADDRESS
BUFFERS FUNCTION)
(AB00-15)
A00-15
(BUFFERED ADDRESS BUS)
ADDRESS LATCHES
(NOT LATCHED)
AB00-15
(FROM PANEL INTERFACE
LOGIC FUNCTION)
MDIS*

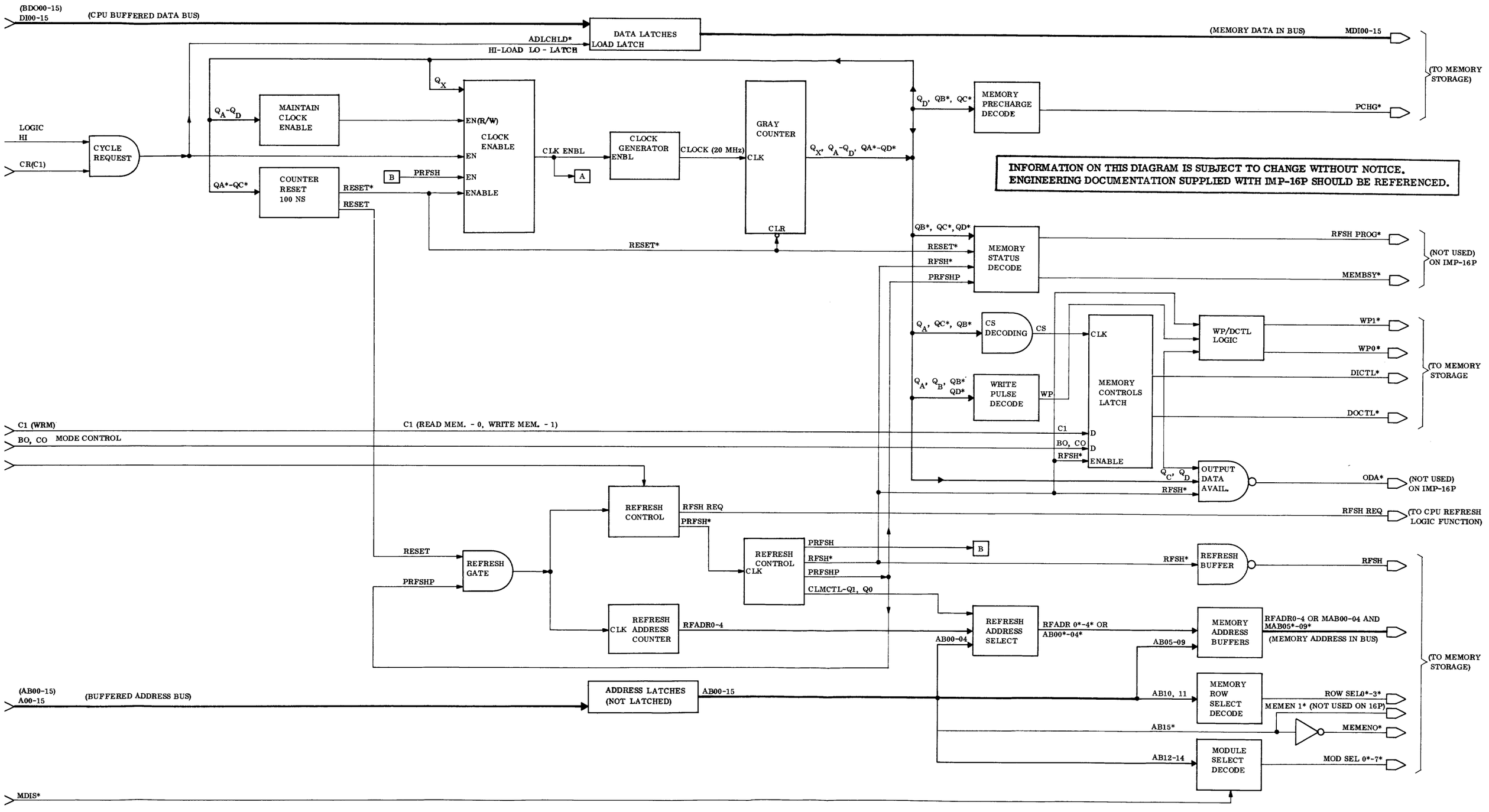


Figure 2/7-4. Memory Timing and Control Card Functional Block Diagram

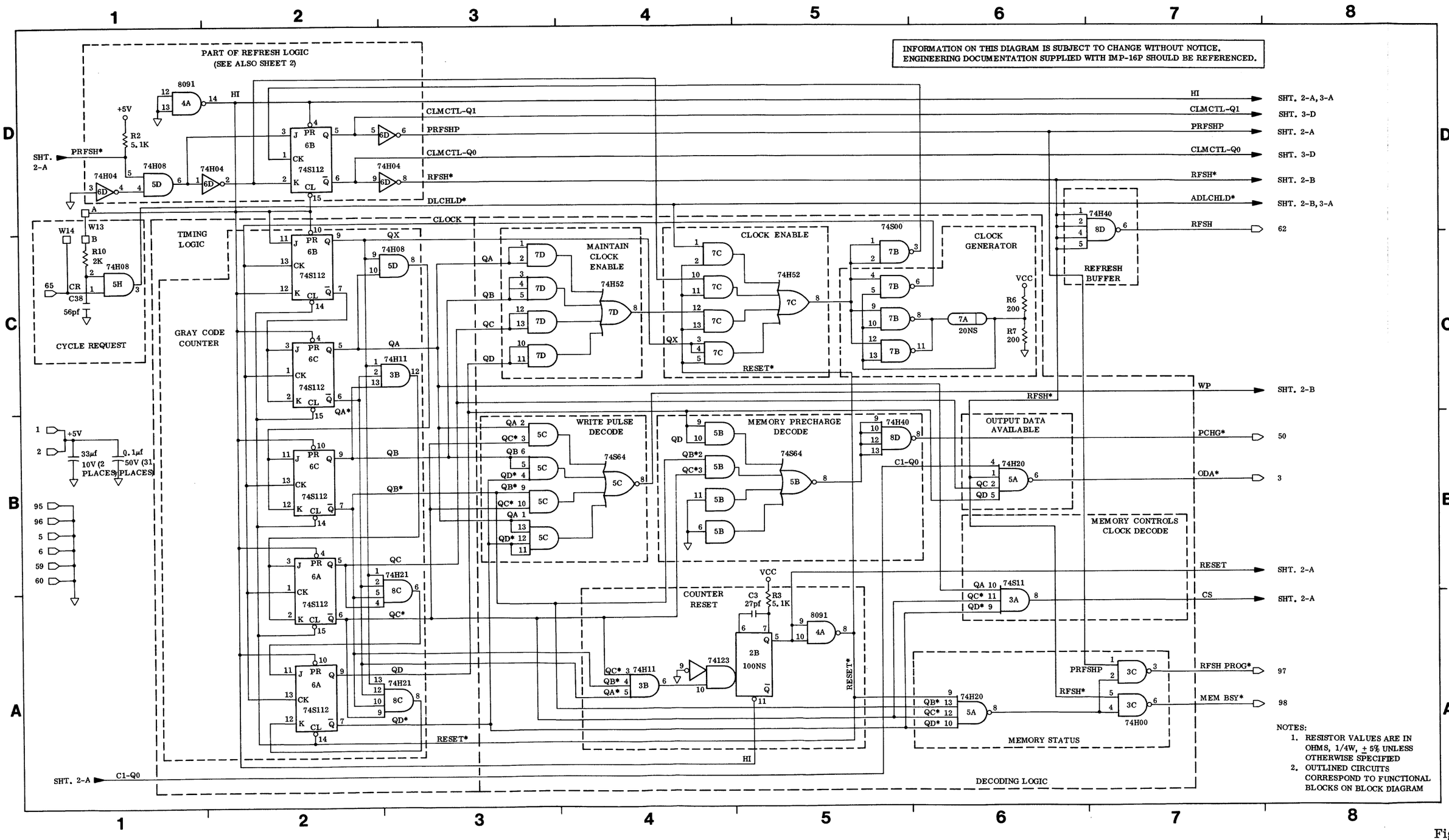

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.
PART OF REFRESH LOGIC (SEE ALSO SHEET 2)
TIMING LOGIC
GRAY CODE COUNTER
CYCLE REQUEST
MAINTAIN CLOCK ENABLE
CLOCK ENABLE
CLOCK GENERATOR
REFRESH BUFFER
WRITE PULSE DECODE
MEMORY PRECHARGE DECODE
OUTPUT DATA AVAILABLE
MEMORY CONTROLS CLOCK DECODE
COUNTER RESET
MEMORY STATUS
DECODING LOGIC
HI
CLMCTL-Q1
PRFSHP
CLMCTL-Q0
RFSH*
DLCHLD*
CLOCK
RESET*
WP
PCHG*
ODA*
RESET
CS
RFSH PROG*
MEM BSY*
ADLCHLD*
RFSH
C1-Q0
SHT. 2-A, 3-A
SHT. 3-D
SHT. 2-A
SHT. 3-D
SHT. 2-B
SHT. 2-B, 3-A
62
SHT. 2-B
50
3
SHT. 2-A
SHT. 2-A
97
98
NOTES:
1. RESISTOR VALUES ARE IN OHMS, 1/4W, ± 5% UNLESS OTHERWISE SPECIFIED
2. OUTLINED CIRCUITS CORRESPOND TO FUNCTIONAL BLOCKS ON BLOCK DIAGRAM

Figure 2/7-5.

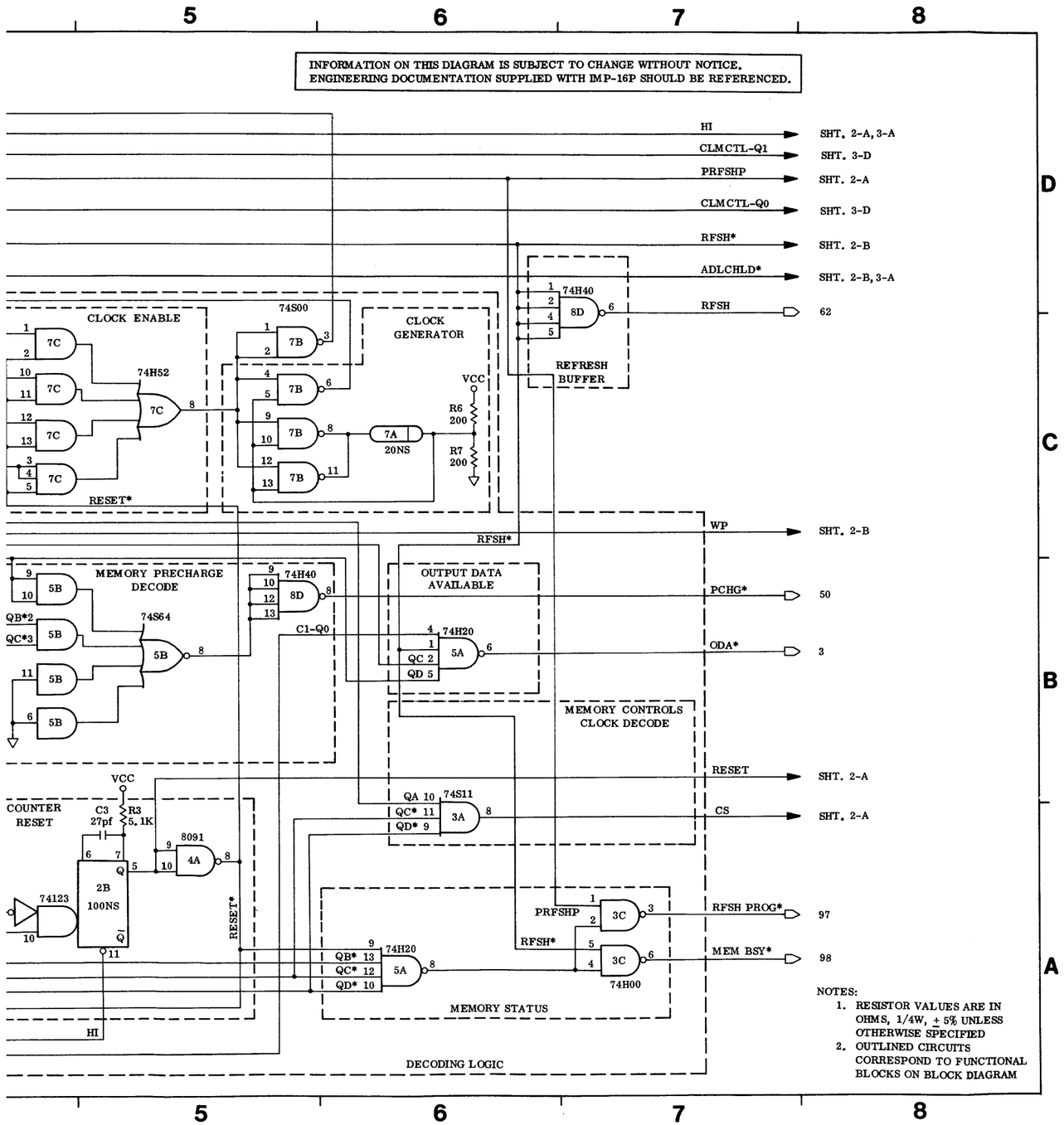


Figure 2/7-5. Memory Timing and Control Card Schematic Diagram (Sheet 1 of 3)

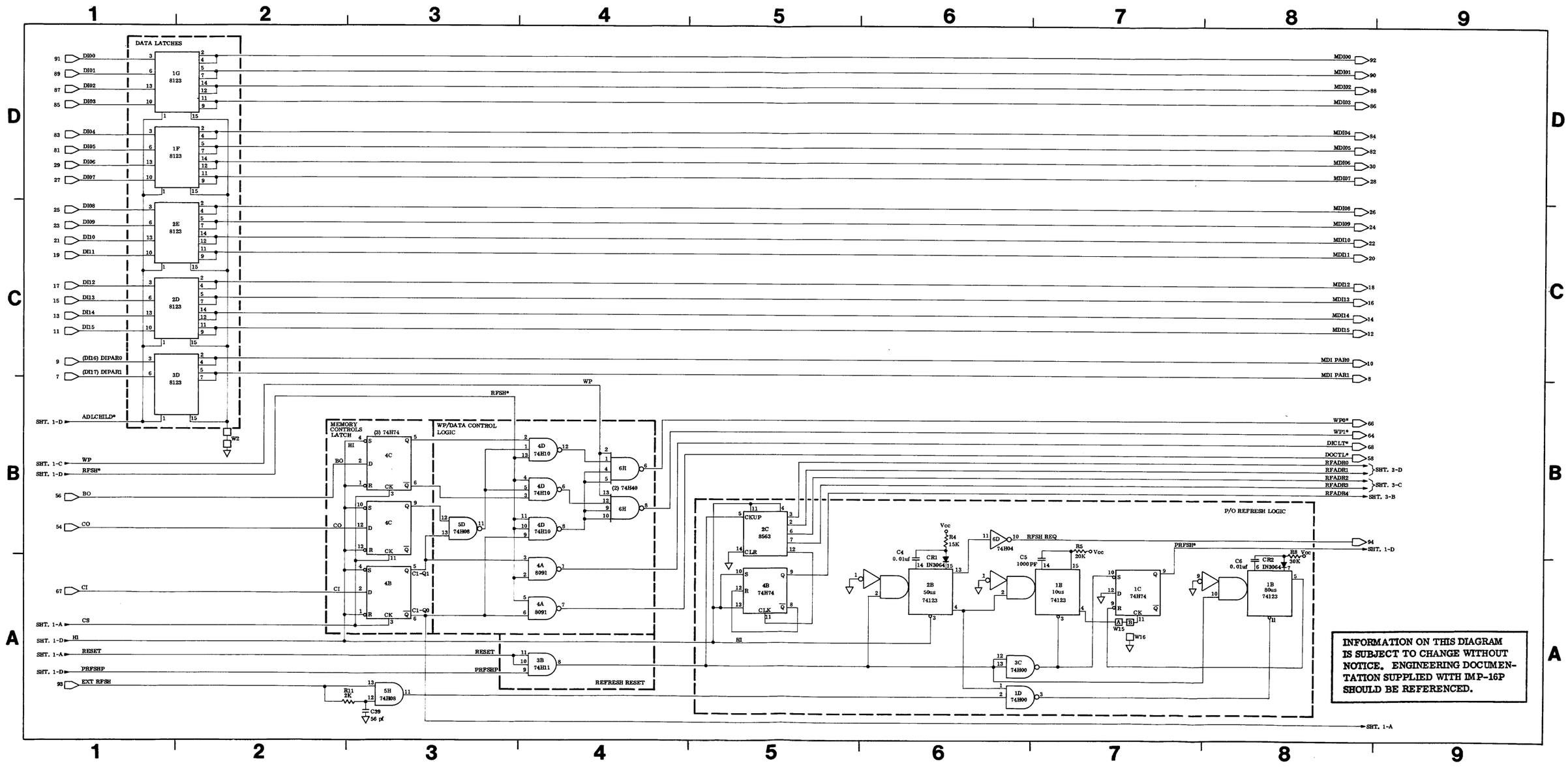


Figure 2/7-5 Memory Timing and Control Card Schematic Diagram (Sheet 2 of 3)

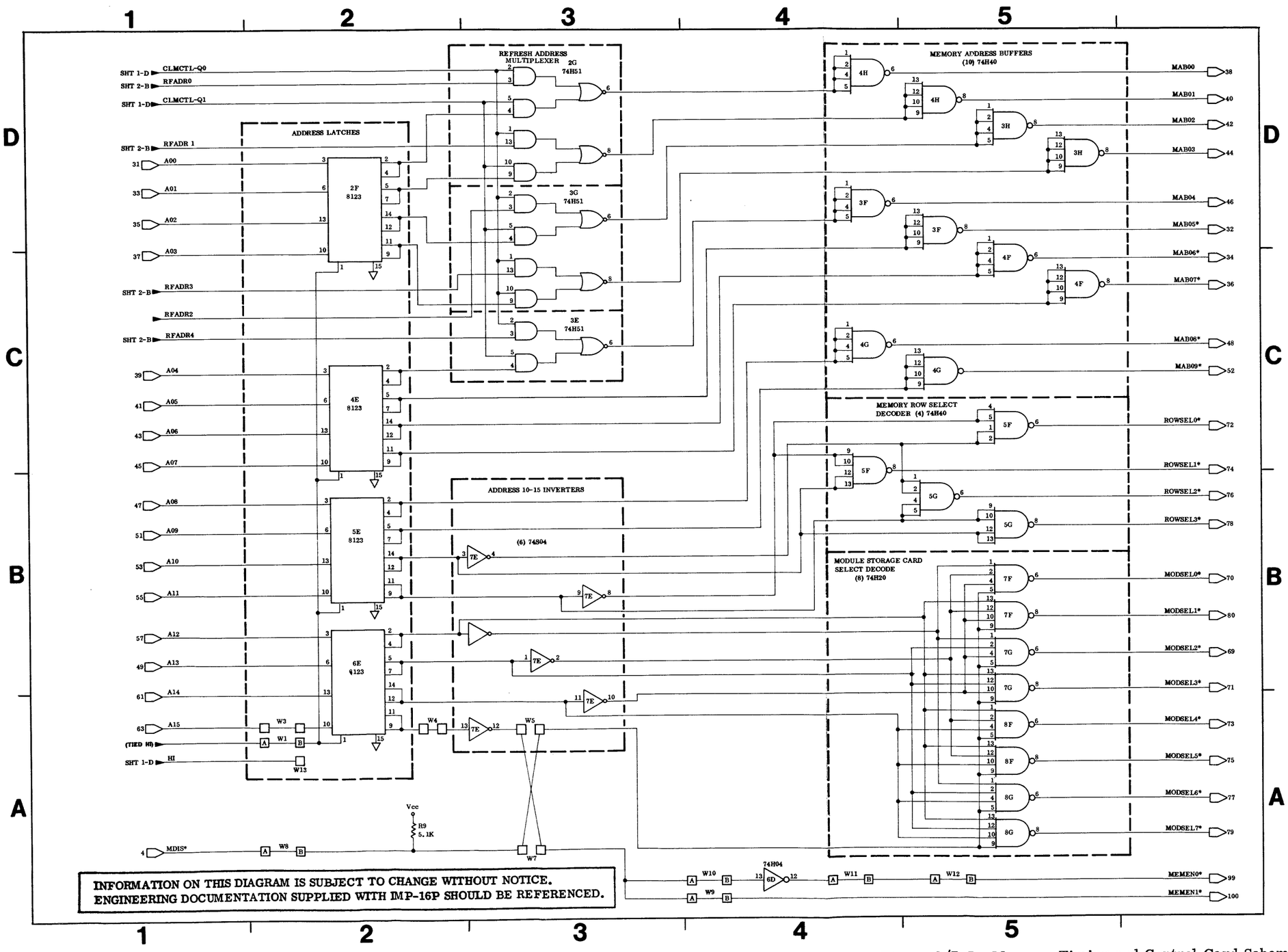
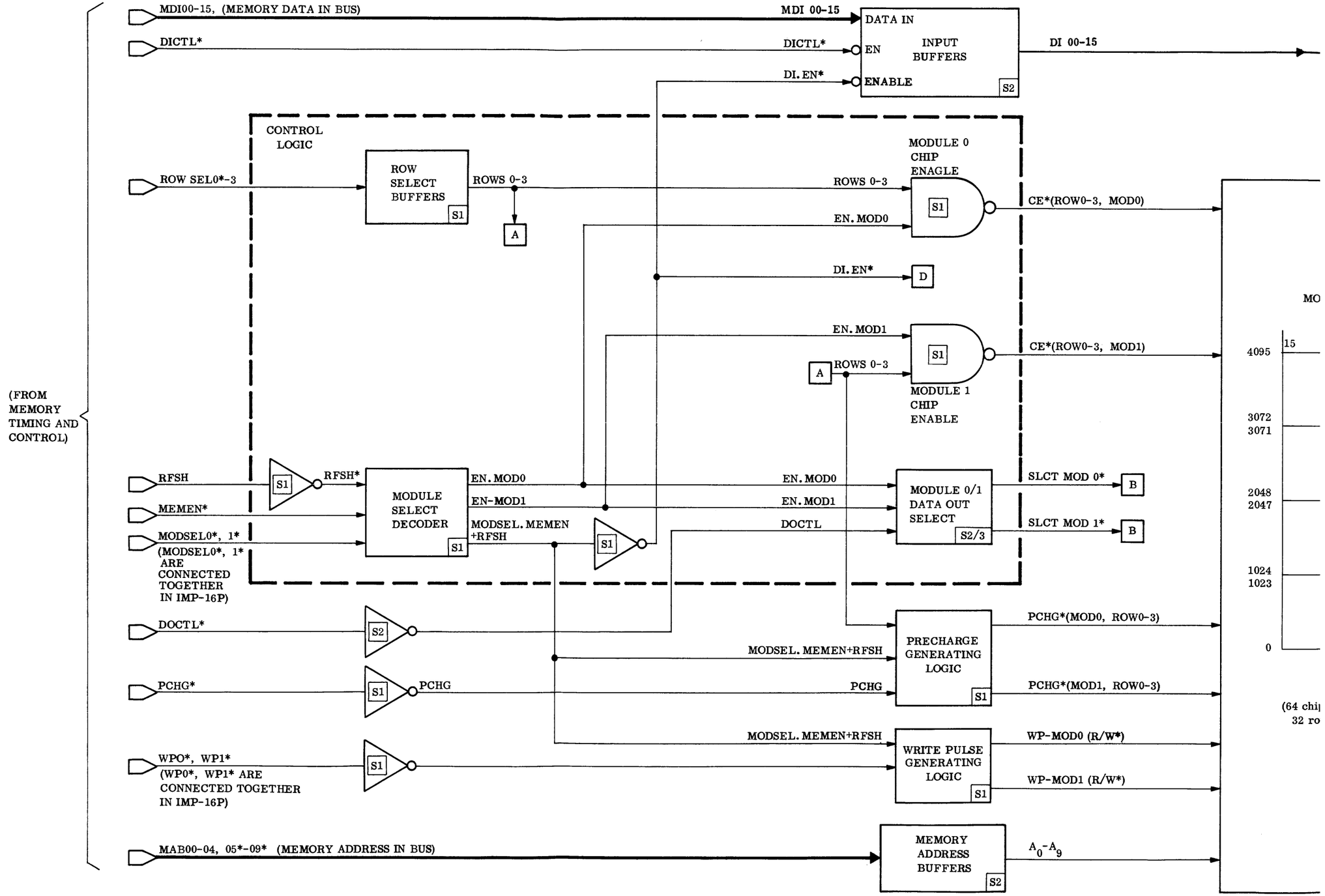
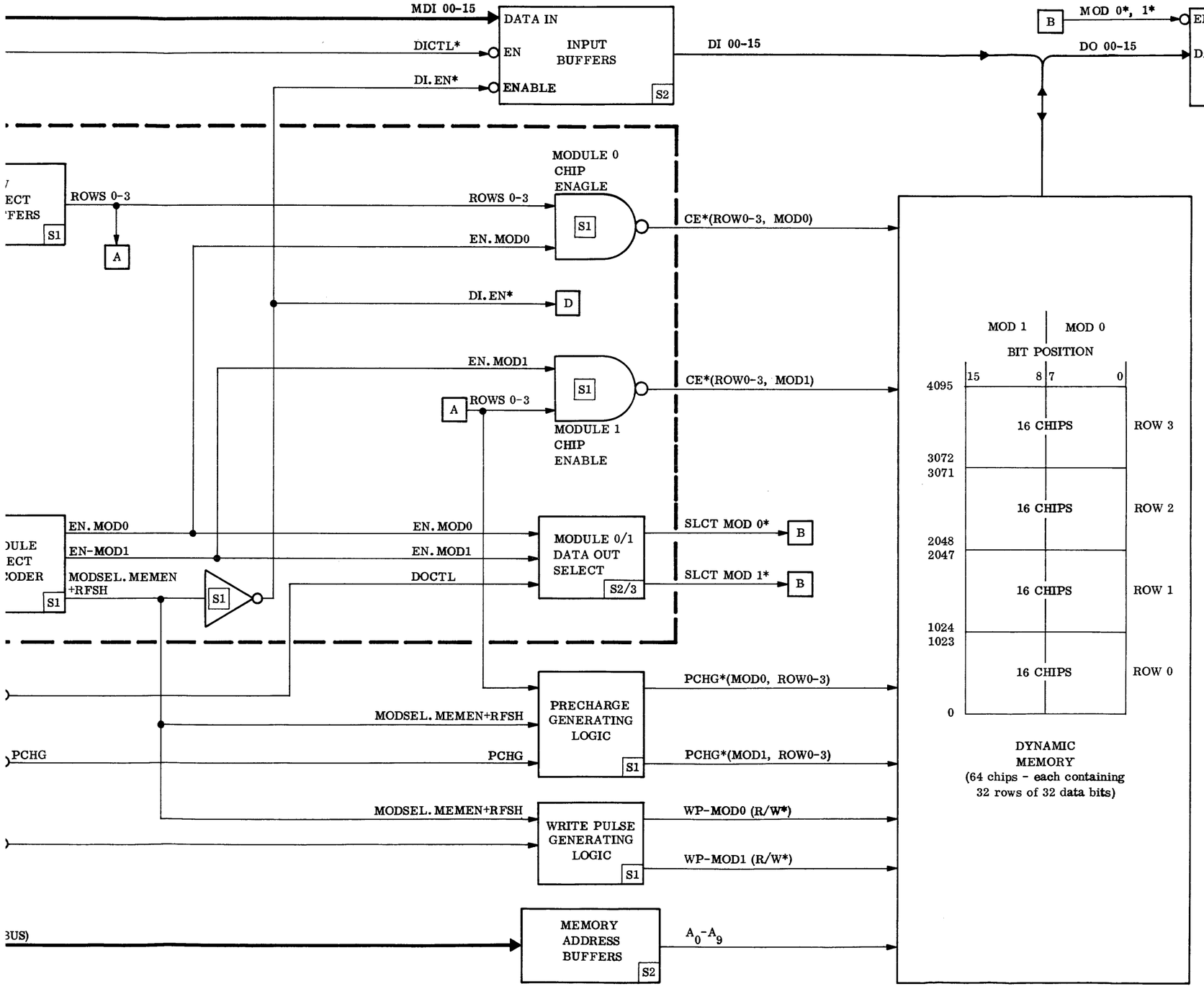


Figure 2/7-5. Memory Timing and Control Card Schematic Diagram (Sheet 3 of 3)


(FROM MEMORY TIMING AND CONTROL)
MDI00-15, (MEMORY DATA IN BUS)
MDI 00-15
DICTL*
DICTL*
DATA IN
EN
INPUT BUFFERS
ENABLE
S2
DI 00-15
DI. EN*
CONTROL LOGIC
ROW SEL0*-3
ROW SELECT BUFFERS
S1
ROWS 0-3
A
MODULE 0 CHIP ENAGLE
ROWS 0-3
EN. MOD0
CE*(ROW0-3, MOD0)
DI. EN*
D
EN. MOD1
CE*(ROW0-3, MOD1)
A
ROWS 0-3
MODULE 1 CHIP ENABLE
RFSH
MEMEN*
MODSEL0*, 1*
(MODSEL0*, 1* ARE CONNECTED TOGETHER IN IMP-16P)
RFSH*
MODULE SELECT DECODER
EN. MOD0
EN-MOD1
MODSEL. MEMEN +RFSH
EN. MOD0
EN. MOD1
DOCTL
MODULE 0/1 DATA OUT SELECT
S2/3
SLCT MOD 0*
SLCT MOD 1*
B
DOCTL*
S2
PCHG*
PCHG
MODSEL. MEMEN+RFSH
PRECHARGE GENERATING LOGIC
PCHG*(MOD0, ROW0-3)
PCHG*(MOD1, ROW0-3)
WPO*, WP1*
(WP0*, WP1* ARE CONNECTED TOGETHER IN IMP-16P)
MODSEL. MEMEN+RFSH
WRITE PULSE GENERATING LOGIC
WP-MOD0 (R/W*)
WP-MOD1 (R/W*)
MAB00-04, 05*-09* (MEMORY ADDRESS IN BUS)
MEMORY ADDRESS BUFFERS
A_0-A_9
4095
3072
3071
2048
2047
1024
1023
0
15



DEFINITIONS OF INCLUDED MNEMONICS/ABBREVIATIONS

MNEMONIC/ABBREVIATION	DEFINITION
A0 - A9	ADDRESS BITS 0-9
CE	CHIP ENABLE
DI 00-15	DATA IN BITS 00-15
DICTL	DATA IN CONTROL
DI. EN	DATA IN ENABLE
DO 00-15	DATA OUT BITS 00-15
DOCTL	DATA OUT CONTROL
EN. MOD 0, 1	MEMORY ENABLE AND MODULE SELECT 0, 1
MAB 00-09	MEMORY ADDRESS BITS 00-09
MDO 00-15	MEMORY DATA OUT BITS 00-15
MDI 00-15	MEMORY DATA IN BITS 00-15
MEMEN	MEMORY ENABLE
MOD SEL 0, 1	MODULE SELECT 0, 1
PCHG	PRECHARGE
RFSH	REFRESH
R/W (MOD 0, 1)	READ/WRITE (MODULE 0, 1)
ROW SEL 0-3	ROW SELECT 0-3
WP 0, 1	WRITE PULSE 0, 1
EN. OUT. MOD 0/1	ENABLE OUTPUT OF MOD 0/1

NOTES:

1. MODULE 0 IS RIGHT (OR LEAST SIGNIFICANT HALF OF 16-BIT WORD)
2. MODULE 1 IS LEFT (OR MOST SIGNIFICANT HALF OF 16-BIT WORD)
3. ROW 0 IS 1st 1024 ADDRESSES
   1 2nd
   2 3rd
   ROW 3 IS 4th 1024 ADDRESSES
4. '*' DENOTES NEGATIVE TRUE SIGNAL STATE
5. NUMBERS WITHIN SQUARES LOCATED IN LOWER RIGHT-HAND CORNER OF FUNCTIONS REFER TO ASSOCIATED SCHEMATIC SHEET NUMBERS.

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

Figure 2/7-6. Memory Storage Card Functional Block Diagram

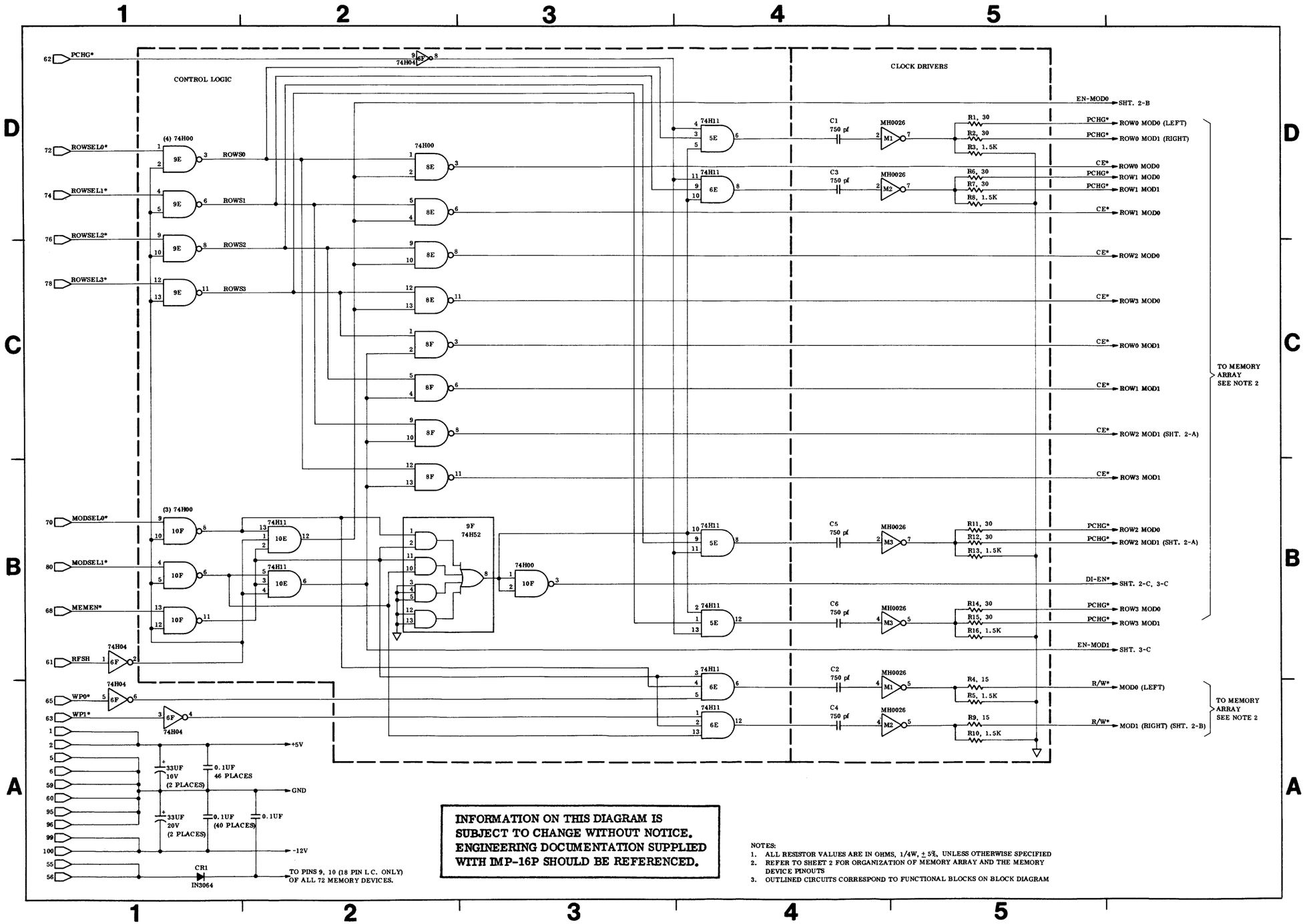
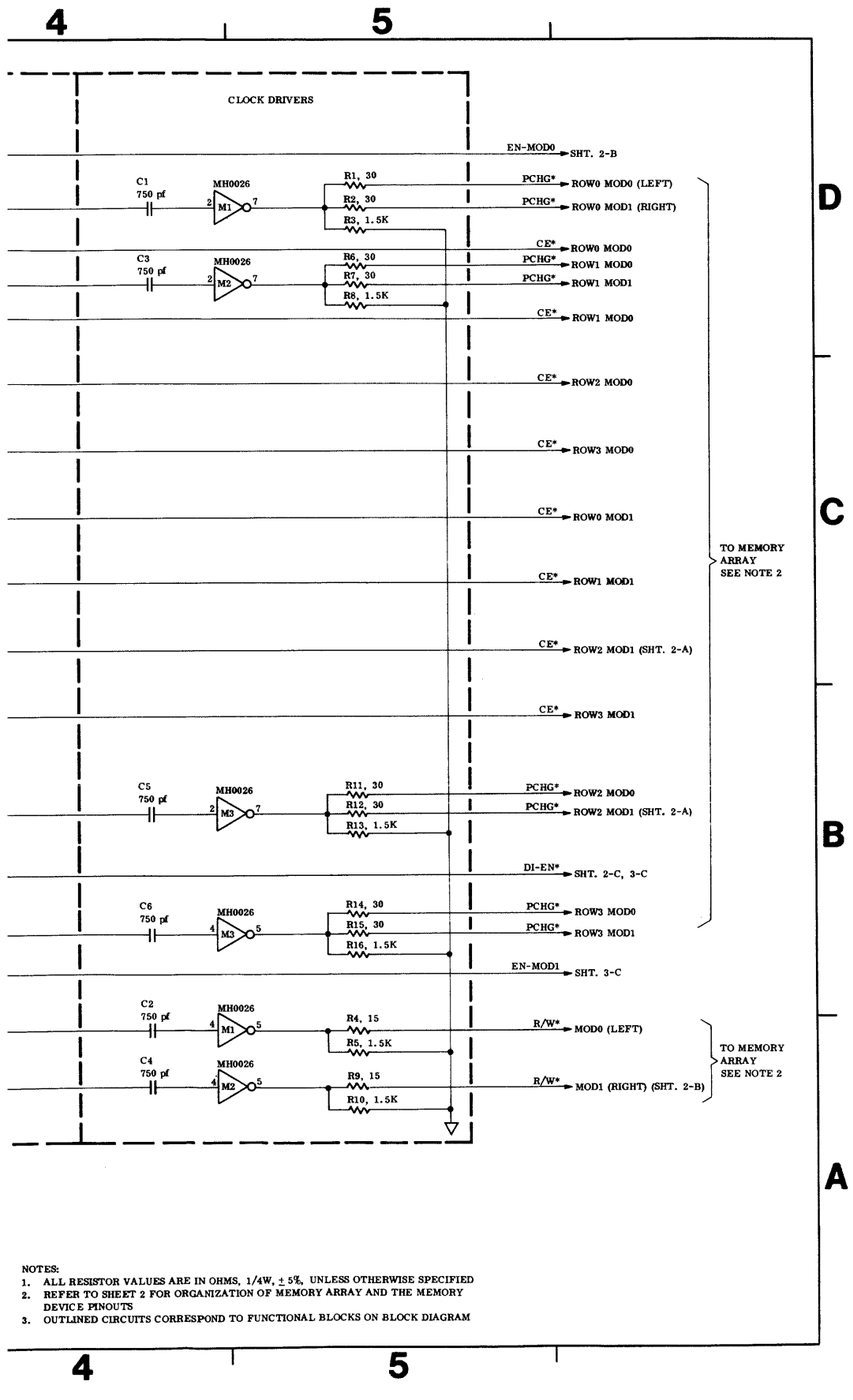

CONTROL LOGIC
CLOCK DRIVERS
PCHG*
ROWSEL0*
ROWSEL1*
ROWSEL2*
ROWSEL3*
MODSEL0*
MODSEL1*
MEMEN*
RFSH
WP0*
WP1*
ROWS0
ROWS1
ROWS2
ROWS3
(4) 74H00
(3) 74H00
74H00
74H04
74H11
9F
74H52
C1 750 pf
C2 750 pf
C3 750 pf
C4 750 pf
C5 750 pf
C6 750 pf
MH0026
R1, 30
R2, 30
R3, 1.5K
R4, 15
R5, 1.5K
R6, 30
R7, 30
R8, 1.5K
R9, 15
R10, 1.5K
R11, 30
R12, 30
R13, 1.5K
R14, 30
R15, 30
R16, 1.5K
EN-MOD0
EN-MOD1
DI-EN*
CE*
PCHG*
R/W*
ROW0 MOD0 (LEFT)
ROW0 MOD1 (RIGHT)
ROW1 MOD0
ROW1 MOD1
ROW2 MOD0
ROW3 MOD0
ROW0 MOD1
ROW1 MOD1
ROW2 MOD1 (SHT. 2-A)
ROW3 MOD1
ROW2 MOD0
ROW3 MOD0
MOD0 (LEFT)
MOD1 (RIGHT) (SHT. 2-B)
SHT. 2-B
SHT. 2-C, 3-C
SHT. 3-C
TO MEMORY ARRAY SEE NOTE 2
+5V
GND
-12V
33UF 10V (2 PLACES)
0.1UF 46 PLACES
33UF 20V (2 PLACES)
0.1UF (40 PLACES)
0.1UF
CR1
IN3064
TO PINS 9, 10 (18 PIN L.C. ONLY) OF ALL 72 MEMORY DEVICES.
INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.
NOTES:
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ± 5%, UNLESS OTHERWISE SPECIFIED
2. REFER TO SHEET 2 FOR ORGANIZATION OF MEMORY ARRAY AND THE MEMORY DEVICE PINOUTS
3. OUTLINED CIRCUITS CORRESPOND TO FUNCTIONAL BLOCKS ON BLOCK DIAGRAM

Figure 2/7-7.



NOTES:
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ± 5%, UNLESS OTHERWISE SPECIFIED
2. REFER TO SHEET 2 FOR ORGANIZATION OF MEMORY ARRAY AND THE MEMORY DEVICE PINOUTS
3. OUTLINED CIRCUITS CORRESPOND TO FUNCTIONAL BLOCKS ON BLOCK DIAGRAM

Figure 2/7-7. Memory Storage Card Schematic Diagram (Sheet 1 of 3)

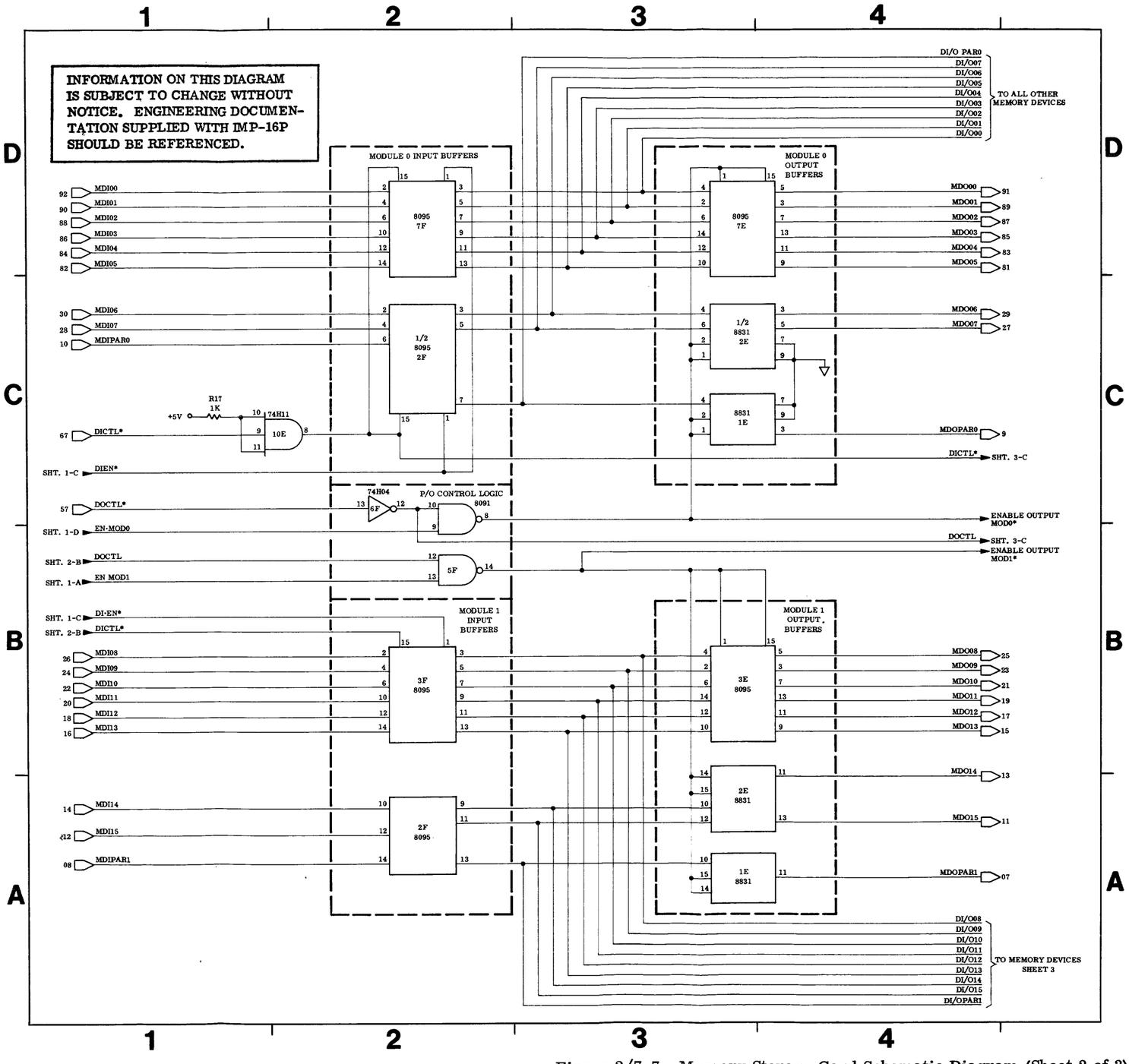


Figure 2/7-7. Memory Storage Card Schematic Diagram (Sheet 2 of 3)

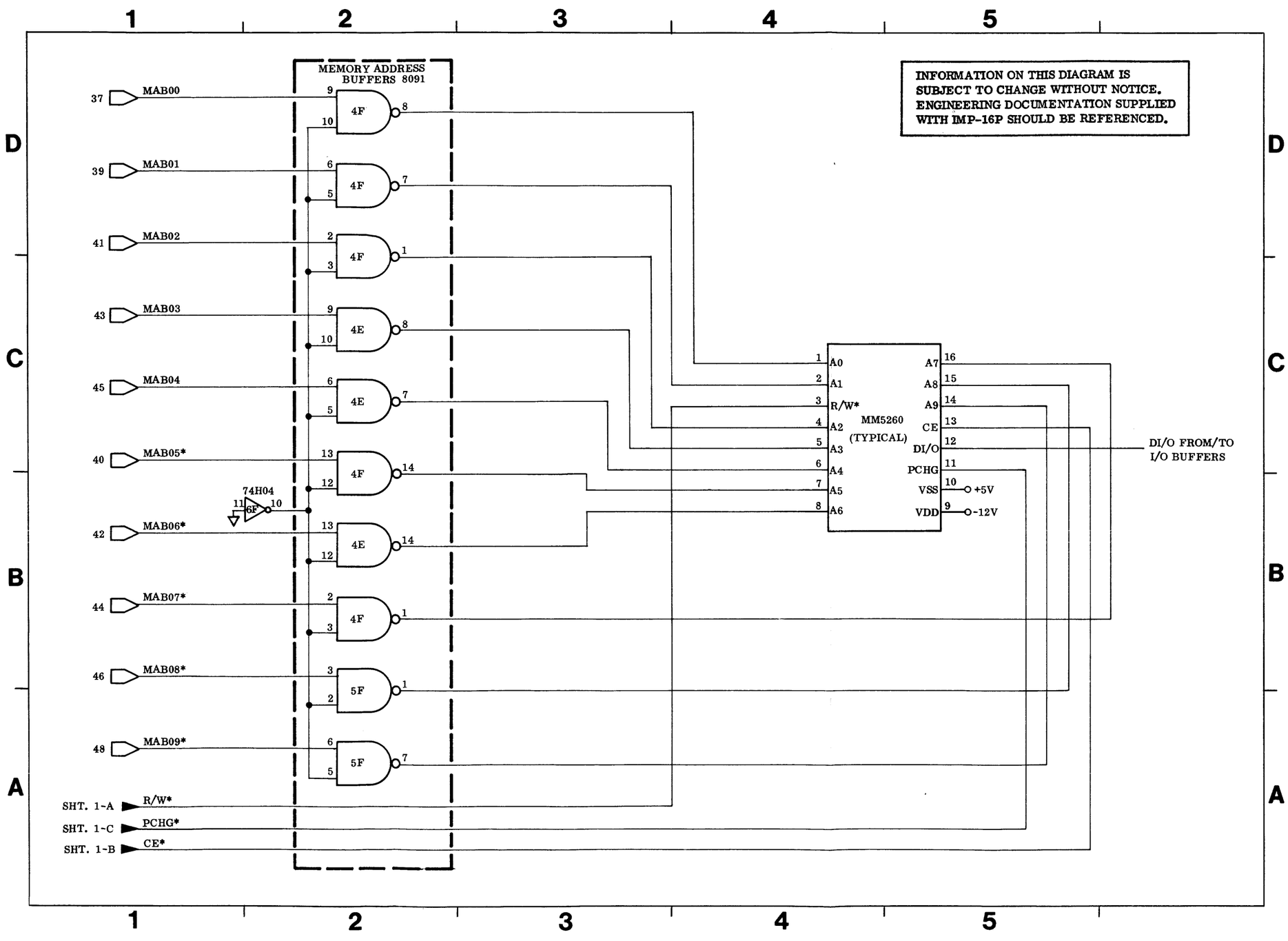


Figure 2/7-7. Memory Storage Card Schematic Diagram (Sheet 3 of 3)

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

ROUT INSTRUCTION (RESET - ORDER 5 SHOWN)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	AB BITS
0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	
DON'T CARE					ADDRESS FIELD								ORDER FIELD			

TYPICAL RIN/ROUT INSTRUCTION FORMATION ON AB00-15 BUS

15	14	08	07	06	00	PD BITS
DATA	MASKED BY GETC		STATUS	MASKED BY GETC		

TTY INTERFACE/OUTPUT WORD FORMAT ON PERIPHERAL DATA BUS

Logical Output States of Reset or Initialized TTY Interface Functions

Function	Output Signal/Logical State (Reset or Initialized)
TTY Interrupt Request	INTREQ/false
TTY Reader Relay Latch	RDRON/false
TTY Status	TTY STAT/false
	DINT/false
	DINT*/false
Transmit Data to TTY	TDOUT/false

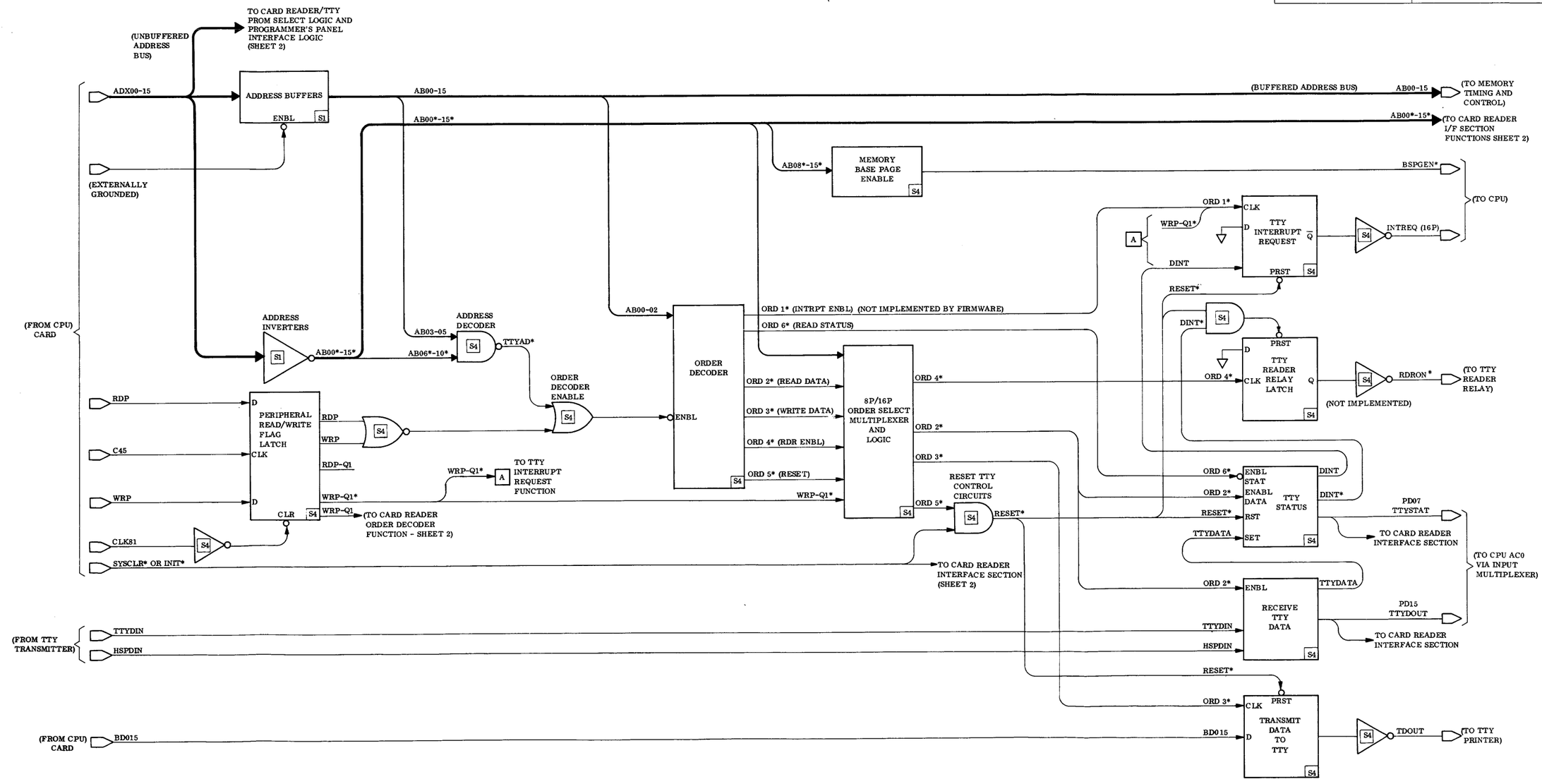


Figure 2/7-8.
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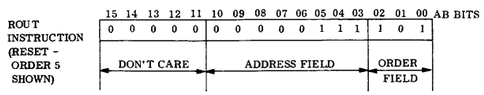
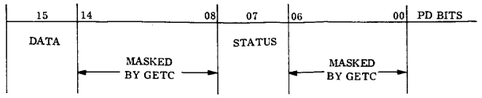
'ORMATION ON THIS DIAGRAM IS
BJECT TO CHANGE WITHOUT NOTICE.
GINEERING DOCUMENTATION SUPPLIED
TH IMP-16P SHOULD BE REFERENCED.



TYPICAL RIN/ROUT INSTRUCTION FORMATION ON AB00-15 BUS



TTY INTERFACE/OUTPUT WORD FORMAT ON PERIPHERAL DATA BUS

Logical Output States of Reset or Initialized TTY Interface Functions

Function	Output Signal/Logical State (Reset or Initialized)
TTY Interrupt Request	INTREQ/false
TTY Reader Relay Latch	RDRON/false
TTY Status	TTY STAT/false
	DINT/false
	DINT*/false
Transmit Data to TTY	TDOUT/false

TTY ABSTTY Program/Subroutine RIN/ROUT Instructions

Type	Function	Order Number
ROUT	Interrupt Enable (see NOTE)	1
RIN	Read TTY Command Code	2
ROUT	Send to TTY Command Code	3
ROUT	Paper Tape Reader Enable	4
ROUT	Reset TTY	6
RIN	Read Interrupt Status	6

NOTE:

USER MUST WRITE AND LOAD AN INTERRUPT SERVICE ROUTINE AND ADD THE APPROPRIATE JUMPERS TO THE BACKPLANE WIRING.

Program and Subroutines Contained in TTY ROMS

Program/Subroutine		
Mnemonic	Name	Memory Address
ABSTTY	Absolute Paper Tape LM Loader	X'7E00
GETC	o Teletype Get Character Subroutine	X'7E3B
PUTC	o Teletype Put Character Subroutine	X'7E59
GECO	o Teletype Get Character with Echo Subroutine	X'7E73
SAV	oo Save Registers Subroutine	X'7E94
DPLX	o Teletype Duplex Subroutine	X'7E9C
MESG	o Message Printing Subroutine	X'7EC3
PUT2C	o Send Two Characters to Teletype Subroutine	X'7ED3
RESET	o Teletype Reset Subroutine	X'7EDA
INTEST	o Teletype In Test Subroutine	X'7EDF
LDM	o Load Multiple Subroutine	X'7EEA
STM	o Store Multiple Subroutine	X'7EFA

DEFINITIONS OF INCLUDED MNEMONICS/ABBREVIATIONS

MNEMONIC/ABBREVIATION	DEFINITION
AB00-15	BUFFERED ADDRESS BITS 00-15
ADX00-15	UNBUFFERED ADDRESS BITS 00-15
AEN1, 2	ADDRESS ENABLE 1 AND 2
BDO 15	BUFFERED DATA OUT, BIT 15
BSPGEN	BASE PAGE ENABLE
C45	CLOCK 45
CLK 81	CLOCK 81
CLK	CLOCK
DINT	DATA INTERRUPT
ENBL	ENABLE
HSPDIN	HIGH SPEED DATA IN
I/F	INTERFACE
INIT	INITIATE
INTREQ	INTERRUPT REQUEST
INTRPT ENBL	INTERRUPT ENABLE
ORD 1-6	ORDER 1-6
PRST	PRESET
RDP	READ PERIPHERAL FLAG
RDRON	READER ON
SYSCLR	SYSTEM CLEAR
TDOUT	TRANSMIT DATA OUT
TTYAD	TTY ADDRESS
TTYDIN	TTY DATA IN
TTYSTAT	TTY STATUS
WRP	WRITE PERIPHERAL FLAG

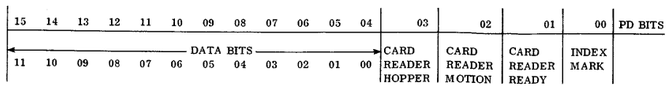
NOTES

1. '*' DENOTES NEGATIVE TRUE SIGNAL STATE.
2. NUMBERS WITHIN SQUARES LOCATED IN FUNCTIONS REFER TO ASSOCIATED SCHEMATIC SHEET NUMBERS.

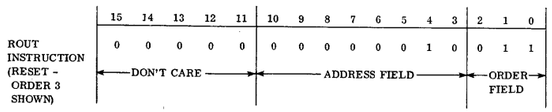
Figure 2/7-8. TTY/Card Reader Interface Card Functional Block Diagram (Sheet 1 of 2)

CARD READER ABSCR PROGRAM RIN/ROUT INSTRUCTIONS

INSTRUCTION		
TYPE	FUNCTION	ORDER NUMBER
RIN	READ DATA	1
ROUT	SET PICK	2
ROUT	RESET (INDEX MARK AND PICK LATCH)	3



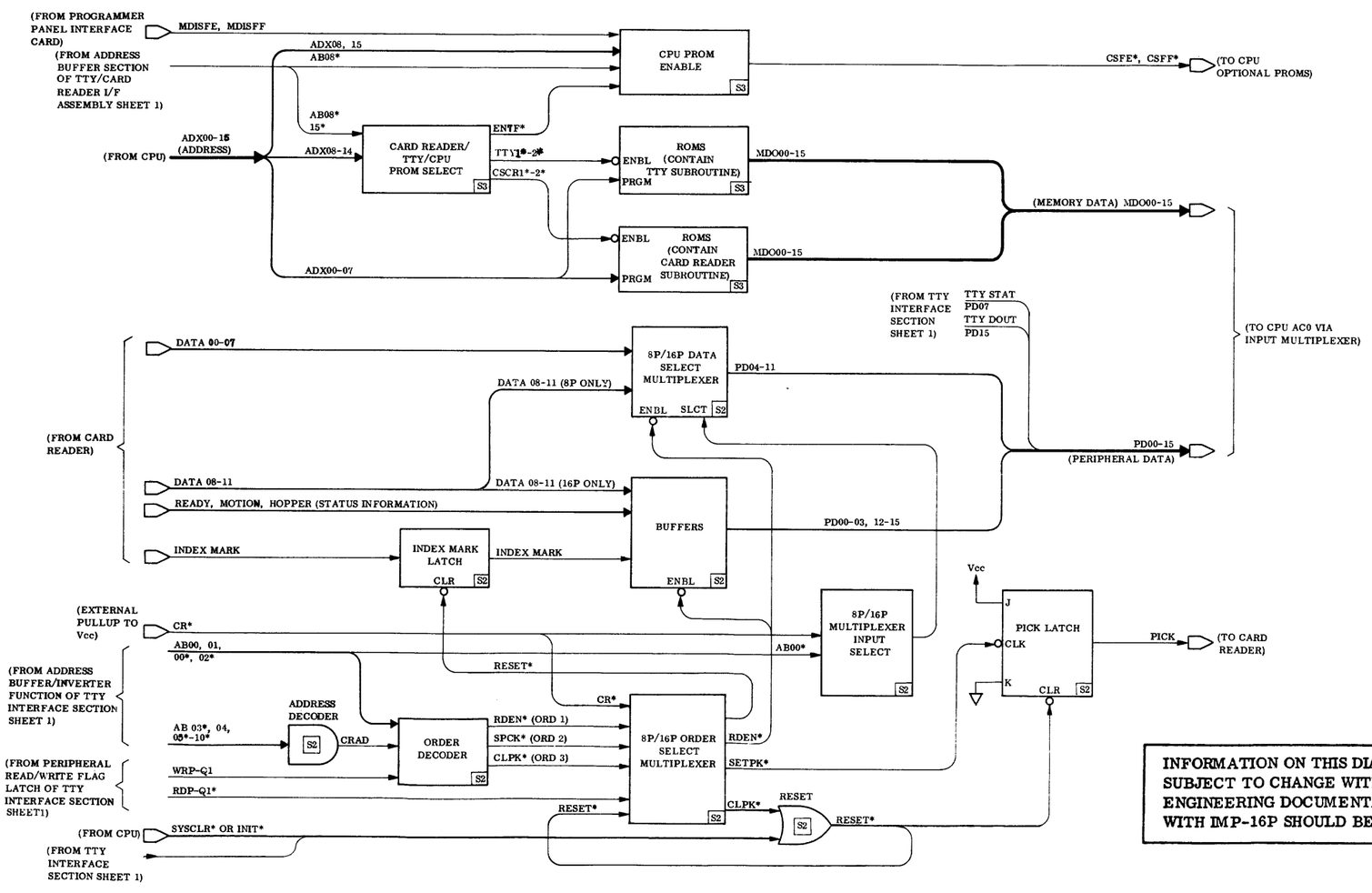
CARD READER INTERFACE OUTPUT WORD FORMAT ON PERIPHERAL DATA BUS



TYPICAL RIN/ROUT INSTRUCTION FORMATION ON AB00-15 BUS

NOTES

1. '*' DENOTES NEGATIVE TRUE SIGNAL STATE
2. NUMBERS WITHIN SQUARES LOCATED IN FUNCTIONS REFER TO ASSOCIATED SCHEMATIC SHEET NUMBERS.



INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

PROGRAMS CONTAINED IN CARD READER PROMS

PROGRAM/SUBROUTINE		
MNEMONIC	NAME	MEMORY ADDRESS
ABSCR	ABSOLUTE CARD READER LOADER PROGRAM	X'7F00
RDCOL	• READ AND CONVERT SINGLE COLUMN SUBROUTINE	X'7F2D
CVT	• CONVERT HOLLERITH TO HEX SUBROUTINE	X'7F41
RDWD	• READ AND CONVERT 16-BIT WORD SUBROUTINE	X'7F7F
ENCRD	• END CARD PROCESSING SUBROUTINE	X'7F96
DTCRD	• DATA CARD PROCESSING SUBROUTINE	X'7FA5
RDCRD	• READCARD SUBROUTINE	X'7FD3
CNVRT	• CONVERT BUFFER TO HEX SUBROUTINE	X'7FF4
	NOTE RDCRD AND CNVRT SUBROUTINES CAN BE IMPLEMENTED BY USER-GENERATED SOFTWARE. THE REMAINING SUBROUTINES ARE IMPLEMENTED BY ABSCR AND ARE NOT INTENDED FOR IMPLEMENTATION BY USER-GENERATED SOFTWARE.	

DEFINITIONS OF INCLUDED MNEMONICS/ABBREVIATIONS

MNEMONIC/ABBREVIATION	DEFINITION
AB00-15	BUFFERED ADDRESS BITS 00-15
ADX00-15	UNBUFFERED ADDRESS BITS 00-15
CLK	CLOCK
CLPK	CLEAR PICK
CLR	CLEAR
CR	CARD READER
CRAD	CARD READER ADDRESS
CSCR1-2	ENABLE CARD READER ROUTINE, PROMS 1 AND 2
EN7F	ENABLE PAGE 7F
ENBL	ENABLE
INIT	INITIATE
MDISFE, FF	MEMORY DISABLE, PAGE FE AND FF
MDO00-15	MEMORY DATA BITS 00-15
PD00-15	PERIPHERAL DATA BITS 00-15
PRGM	PROGRAM
RDEN	READ ENABLE
SLCT	SELECT
SPCK	SET PICK
SYSCLR	SYSTEM CLEAR
TTY 1-2	ENABLE TELETYPE ROUTINE, PROMS 1 AND 2
WRP	WRITE PERIPHERAL

Figure 2/7-8.
Funct

01	00	PD BITS
)		
)ER	INDEX MARK	
)Y		

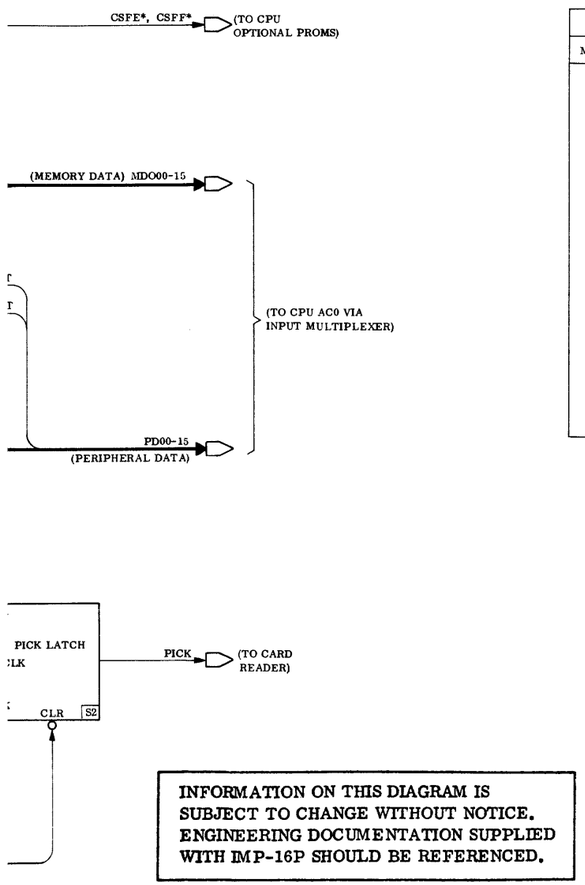
BUS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	AB
ROUT INSTRUCTION (RESET - ORDER 3 SHOWN)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	
	← DON'T CARE →					← ADDRESS FIELD →								← ORDER FIELD →			

TYPICAL RIN/ROUT INSTRUCTION FORMATION ON AB00-15 BUS

NOTES

1. '*' DENOTES NEGATIVE TRUE SIGNAL STATE
2. NUMBERS WITHIN SQUARES LOCATED IN FUNCTIONS REFER TO ASSOCIATED SCHEMATIC SHEET NUMBERS.



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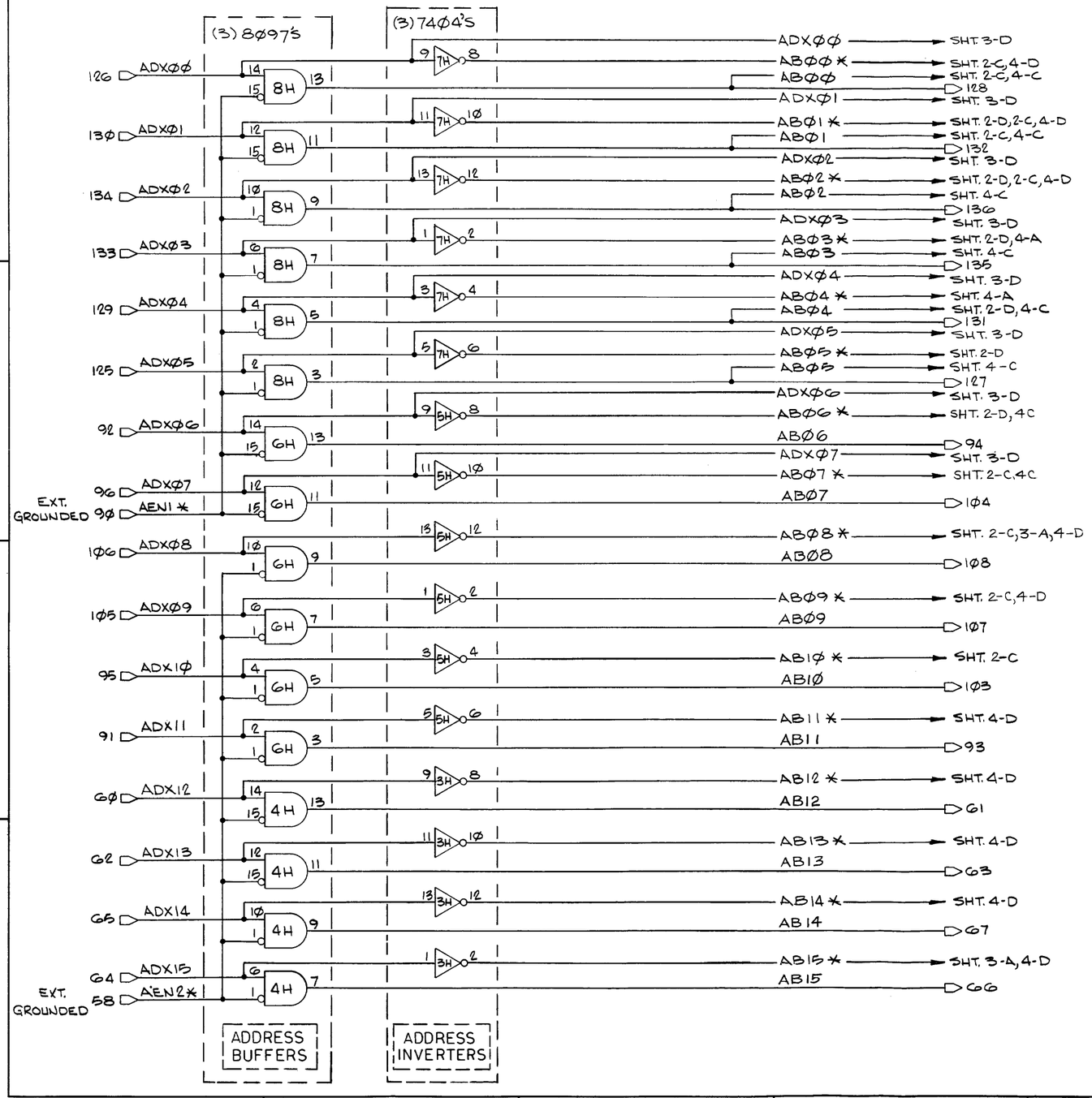
PROGRAMS CONTAINED IN CARD READER PROMS

PROGRAM/SUBROUTINE		
MNEMONIC	NAME	MEMORY ADDRESS
ABSCR	ABSOLUTE CARD READER LOADER PROGRAM	X'7F00
RDCOL	• READ AND CONVERT SINGLE COLUMN SUBROUTINE	X'7F2D
CVT	• CONVERT HOLLERITH TO HEX SUBROUTINE	X'7F41
RDWD	• READ AND CONVERT 16-BIT WORD SUBROUTINE	X'7F7F
ENCRD	• END CARD PROCESSING SUBROUTINE	X'7F96
DTCRD	• DATA CARD PROCESSING SUBROUTINE	X'7FA5
RDCRD	• READCARD SUBROUTINE	X'7FD3
CNVRT	• CONVERT BUFFER TO HEX SUBROUTINE	X'7FF4
	NOTE RDCRD AND CNVRT SUBROUTINES CAN BE IMPLEMENTED BY USER-GENERATED SOFTWARE. THE REMAINING SUBROUTINES ARE IMPLEMENTED BY ABSCR AND ARE NOT INTENDED FOR IMPLEMENTATION BY USER-GENERATED SOFTWARE.	

DEFINITIONS OF INCLUDED MNEMONICS/ABBREVIATIONS

MNEMONIC/ABBREVIATION	DEFINITION
AB00-15	BUFFERED ADDRESS BITS 00-15
ADX00-15	UNBUFFERED ADDRESS BITS 00-15
CLK	CLOCK
CLPK	CLEAR PICK
CLR	CLEAR
CR	CARD READER
CRAD	CARD READER ADDRESS
CSCR1-2	ENABLE CARD READER ROUTINE, PROMS 1 AND 2
EN7F	ENABLE PAGE 7F
ENBL	ENABLE
INIT	INITIATE
MDISFE, FF	MEMORY DISABLE, PAGE FE AND FF
MDO00-15	MEMORY DATA BITS 00-15
PD00-15	PERIPHERAL DATA BITS 00-15
PRGM	PROGRAM
RDEN	READ ENABLE
SLCT	SELECT
SPCK	SET PICK
SYSCLR	SYSTEM CLEAR
TTY 1-2	ENABLE TELETYPE ROUTINE, PROMS 1 AND 2
WRP	WRITE PERIPHERAL

Figure 2/7-8. TTY/Card Reader Interface Card Functional Block Diagram (Sheet 2 of 2)



INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

CONNECTIONS FOR IGP OPERATIONS	REMARKS
PIN 49 TO GROUND	IGP/BPM MULTIPLEXER SELECTION
PINS 27 & 35 TO -12V	TTY VOLTAGE
PIN 78 TO PINS 68, 81	ADDRESSING CR PROMS
PIN 77 TO PINS 80, 124	ADDRESSING TTY PROMS
PIN 55 TO LOGIC "1"	THIS SIGNAL NEEDED FOR 16 BIT SELECTION OF CR DATA
LOGIC "1" AVAILABLE ON PIN 48	

PROGRAMMING NOTES		
	IGP	
TELETYPE	SUBSYSTEM ADDRESS: X'Ø7 ABSOLUTE DEVICE ADDRESS IS X'Ø38	ORDER CODES Ø. NOT USED 1. INTRPT ENAB (ROUT) 2. READ DATA (RIN) 3. WRITE DATA (ROUT) 4. RDR ENABLE (ROUT) 5. RESET (ROUT) 6. READ STATUS (RIN) 7. NOT USED
CARD READER	SUBSYSTEM ADDRESS: X'Ø2 ABSOLUTE DEVICE ADDRESS IS X'Ø1Ø	Ø. NOT USED 1. READ STANDARD (RIN) 2. SET PICK (ROUT) 3. RESET (ROUT)

RDP (READ PERIPHERAL) - RIN
WRP (WRITE PERIPHERAL) - ROUT

15	14	13	12	11	1Ø	Ø9	Ø8	Ø7	Ø6	Ø5	Ø4	Ø3	Ø2	Ø1	ØØ	
																← AB (BUFFERED ADDRESS BITS)
					Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	Ø			← CARD READER
					Ø	Ø	Ø	Ø	Ø	1	1	1				← TELETYPE
DON'T CARE				ADDRESS CODE								ORDER CODE				
												[1]				

NOTES:

[1] ORDER CODE BIT CONFIGURATION CHANGES IN ACCORDANCE WITH ORDER

2. ▷ DENOTES CARD EDGE CONNECTOR FOR CARD READER CABLE

3. ▷ DENOTES CARD EDGE CONNECTOR FOR TTY CABLE.

4. OUTLINED CIRCUITS CORRESPOND TO FUNCTIONAL BLOCKS ON BLOCK DIAGRAM

Figure 2/7-9. TTY/Card Reader Interface Card Schematic Diagram (Sheet 1 of 4)

INFORMATION ON THIS DIAGRAM IS SUBJECT
ENGINEERING DOCUMENTATION SUPPLIED V

Figure 2/7-9.

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE.
ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

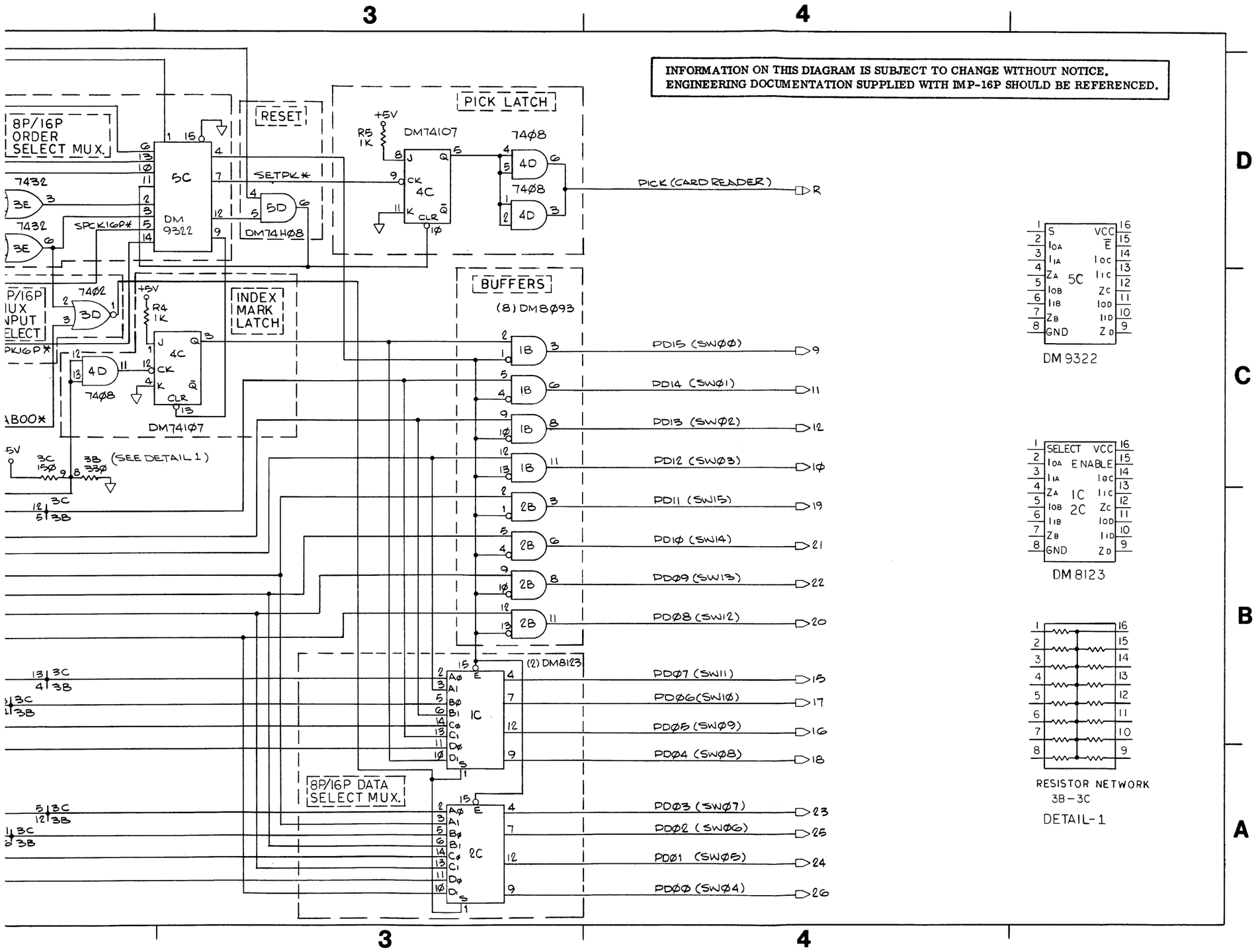


Figure 2/7-9. TTY/Card Reader Interface Card Schematic Diagram (Sheet 2 of 4)

PROMS(CONTAIN TTY SUBROUTINES)

PROMS(CONTAIN CARD READER SUBROUTINES)

CPU PROM ENABLE

CARD READER/TTY/CPU PROM SELECT

7G MM5203 OR MM5213

5G MM5203 OR MM5213

6G MM5203 OR MM5213

4G MM5203 OR MM5213

SHT. 1-D: ADX00 ADX01 ADX02 ADX03

SHT. 1-C: ADX04 ADX05 ADX06 ADX07

124 CSTTY1*

80 CSTTY2*

81 CSCR1*

68 CSCR2*

119 MDISFE*

SHT. 1-B: AB08* AB15*

SHT. 1-A: AD09 AD10 AD11 AD12 AD13 AD14 AD15 AD08 MDISFF*

4E DM74S11 · 5E 74H08 · GE DM74S10 · 7E DM74S20

R10 1K · R9 1K

MDO 08 MDO 09 MDO 10 MDO 11 MDO 12 MDO 13 MDO 14 MDO 15

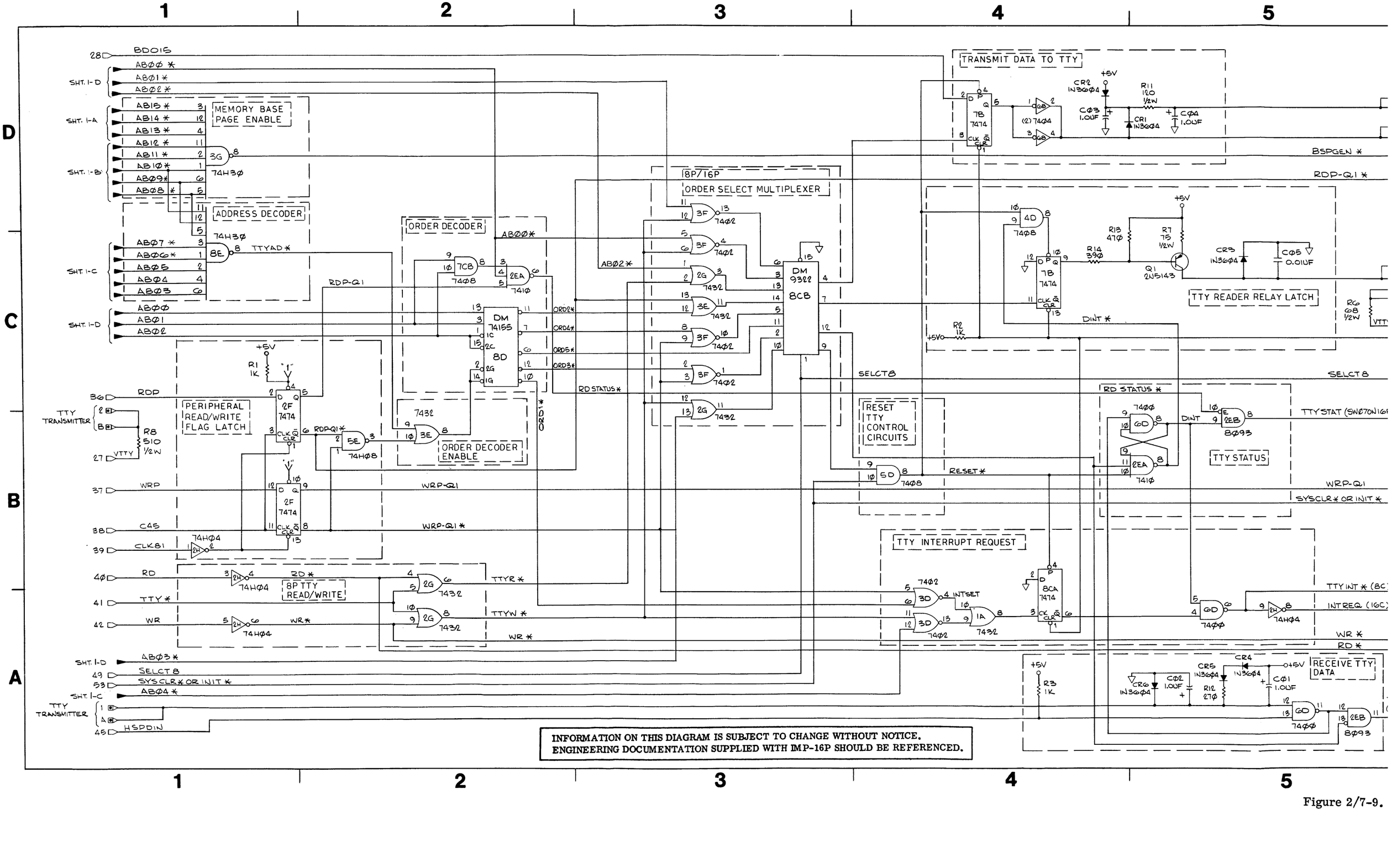
MDO 00 MDO 01 MDO 02 MDO 03 MDO 04 MDO 05 MDO 06 MDO 07

CSFE* 122 · CS7E* 77 · CS7F* 78 · CSFF* 123

MM5203 OR MM5213: VSS CONT PROG VBB · A1 A2 A3 A4 A5 A6 A7 A8 · B1 B2 B3 B4 B5 B6 B7 B8 · CS A9 VDD VLL

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

Figure 2/7-9. TTY/Card Reader Interface Card Schematic Diagram (Sheet 3 of 4)



INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE.
ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

Figure 2/7-9.

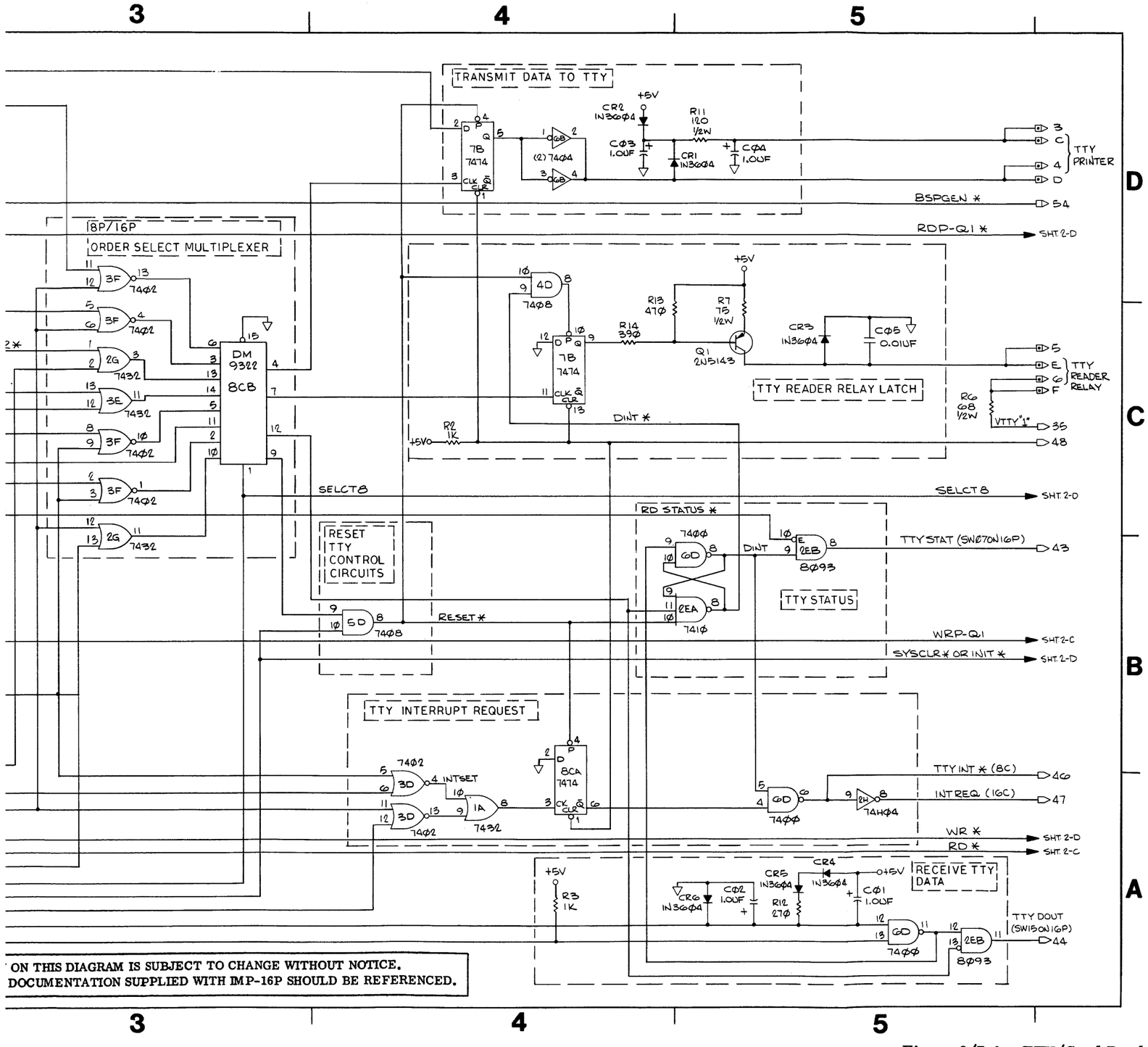


Figure 2/7-9. TTY/Card Reader Interface Card Schematic Diagram (Sheet 4 of 4)

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

FROM SHT 2 ZONE 11C DSI10*

P/O PROGRAM COUNTER MEMORY ADDRESS DISPLAY BUFFER

P/O PROGRAM COUNTER MEMORY ADDRESS DISPLAY INDICATORS/DRIVERS

P/O PROGRAM COUNTER MEMORY ADDRESS DISPLAY BUFFER

P/O PROGRAM COUNTER MEMORY ADDRESS DISPLAY INDICATORS/DRIVERS

DATA SWITCHES

FROM SHT 2 ZONE 11C,D

LPCA
LPCB
DB00*
DB01*
DB02*
DB03*
DB04*
DB05*
DB06*
DB07*
DB08*
DB09*
DB10*
DB11*
DB12*
DB13*
DB14*
DB15*

TO SHT 2 ZONE 7B,C

P/O DATA DISPLAY BUFFERS

P/O DATA DISPLAY INDICATORS/DRIVERS

P/O DATA DISPLAY BUFFERS

P/O DATA DISPLAY INDICATORS/DRIVERS

GND

TYPICAL 1 OF 25 EVEN PINS PIN NO. 2, 4, 6, 8, 10, 12, 14, 16, 18, 20 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48 AND 50

+5V
GND
P

FROM SHT 2 ZONE 9C,D

LSDB
LSDA

Figure 2/7-10. Programmers Panel Card Schematic Diagram (Sheet 1 of 2)

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE.
ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

PROGRAMMER PANEL PRESENT — PPP* → 4,3

DISPLAY BUFFER/DATA SELECT

45 LDS* → R40 180, R39 390 → 74HØ4 6B → LDS

33 DSI0 → R50 180, R49 390 → 74HØ4 3B → 74ØØ 5B

35 DSI1 → R48 180, R47 390 → 74HØØ 4B → DSI11*

74ØØ 5B → 74HØ4 3B → LPCA, LPCB, LSDA, LSDB → TO SHT 1 ZONE 1A,C,B

DSI1Ø* ← 74HØØ 4B

FROM SHT 1 ZONE 6B,C → DBØØ*, DBØ1*, DBØ2*, DBØ3*, DBØ4*, DBØ5*, DBØ6*, DBØ7*, DBØ8*, DBØ9*, DB1Ø* → TO SHT 1 ZONE 6B,C

DISPLAY SELECTION ROTARY SWITCH

NEXT INST, FLAGS, STACK, MEM ADDR, MEM DATA, PROG DATA, LEFT MOST, RIGHT MOST, PC, AC3, AC2, AC1, AC0

R83 1K +5V

DSI11* → 74Ø7 2B

PROGRAMMER PANEL MOMENTARY SWITCHES

TP1 — R4 1K +5V — 74Ø7 2B

TP2 — R10 1K +5V — 74Ø7 2B

TP3 — R11 1K +5V — 74Ø7 2B

NC (UP) / NO (DWN) — LOAD DATA — 74Ø6 1B — R46 180 +5V — SW1* (LOADS*) → 37

INCR MEM ADDR — 74Ø6 1B — R44 180 +5V — SW2* (INCAS*) → 39

SINGLE INST — 74Ø6 1B — R42 180 +5V — SW3* (SINGS*) → 41

R45 330, R36 560, R43 330, R38 560, R41 330, R37 560 → +5V

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, ±10%, 1/4 WATT
2. CAPACITANCE VALUES ARE IN MICROFARADS
3. COMMON CONNECTION CIRCUIT RETURN SYMBOLS ARE AS FOLLOWS:
   - RETURN GROUND
   - 144-PIN EDGE CONNECTOR
   - 12-PIN VIKOM CONNECTOR
   - 50-PIN 3M CONNECTOR

Figure 2/7-10. Programmers Panel Card Schematic Diagram (Sheet 2 of 2)

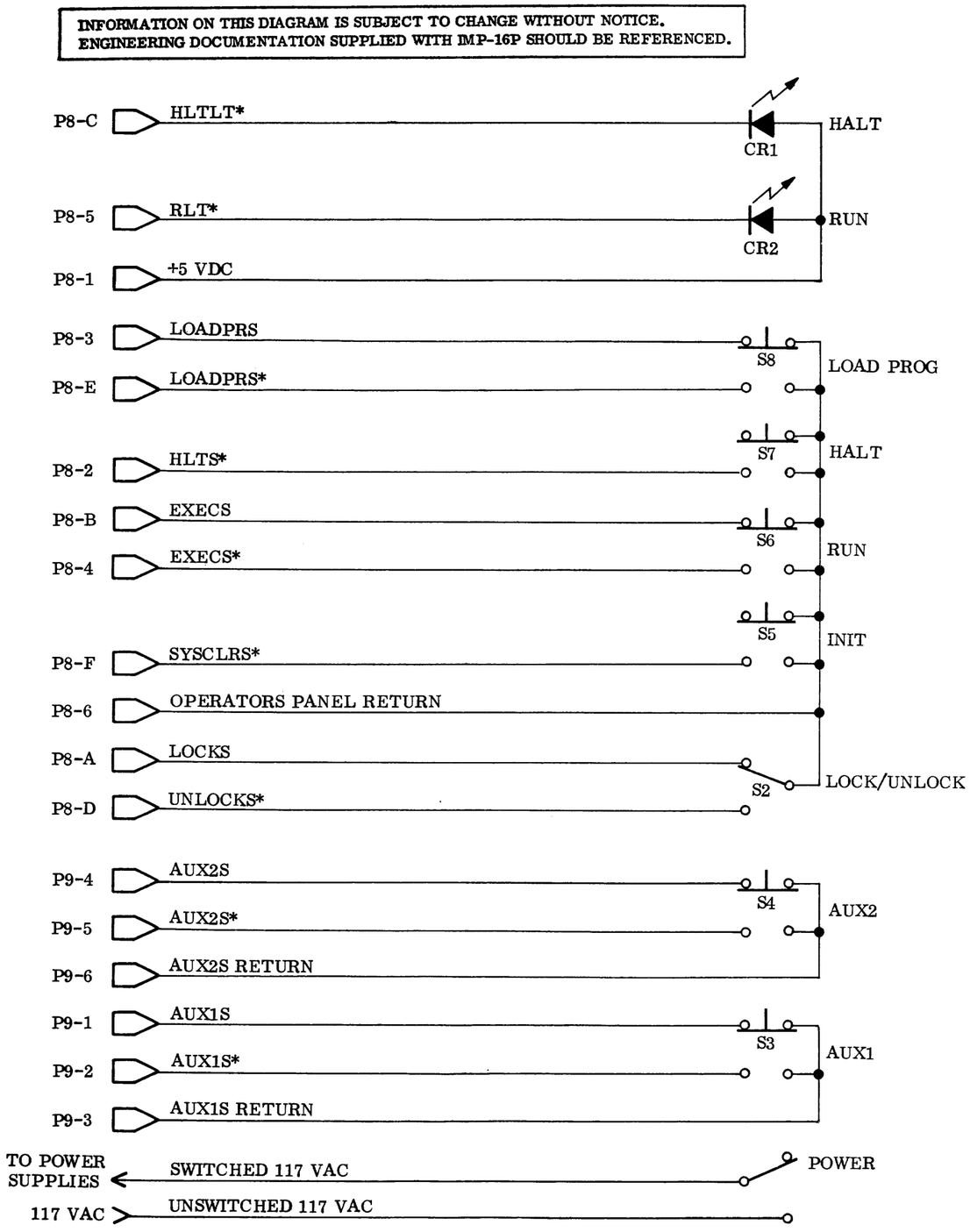


Figure 2/7-11. Operators Control Panel Schematic Diagram

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

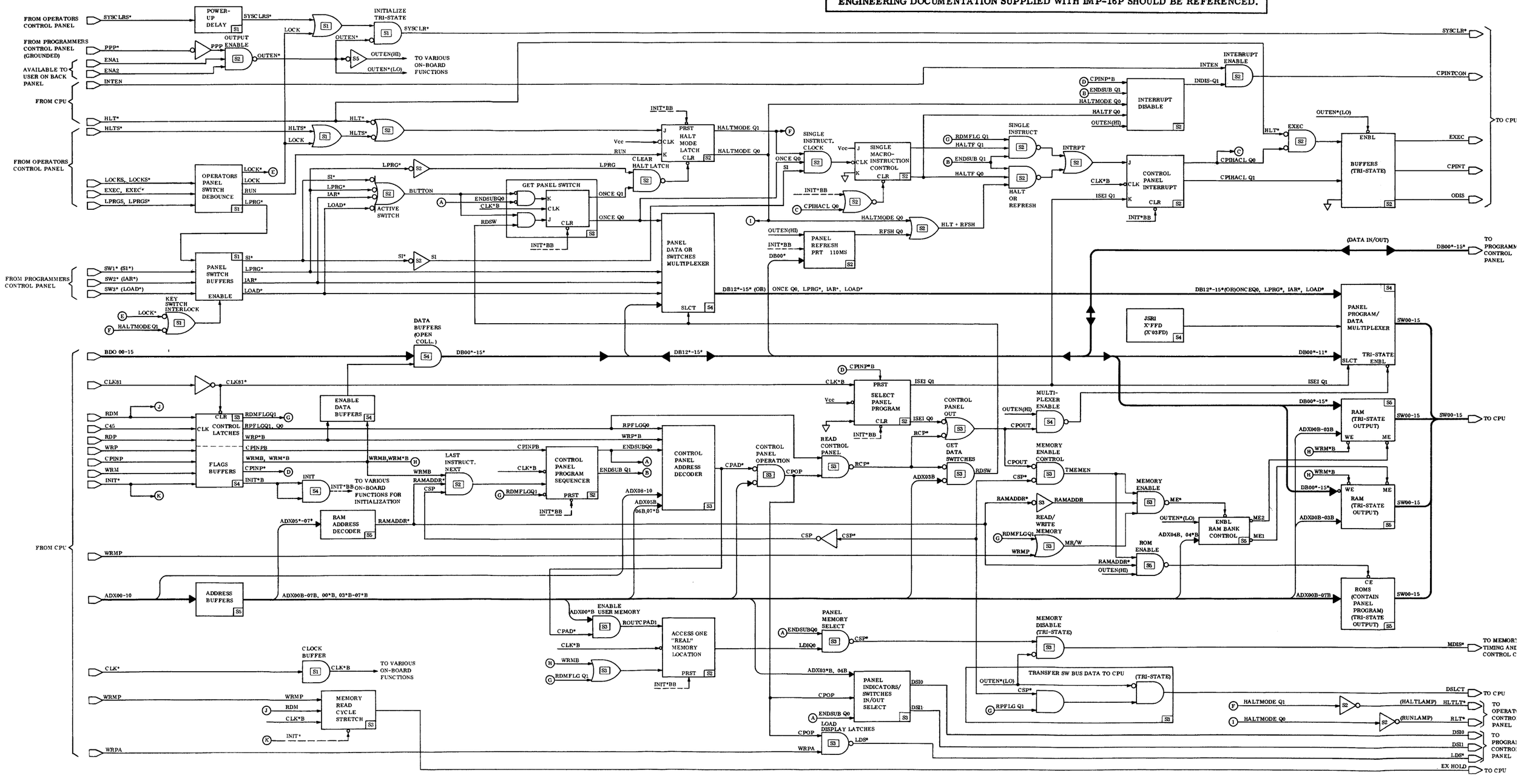
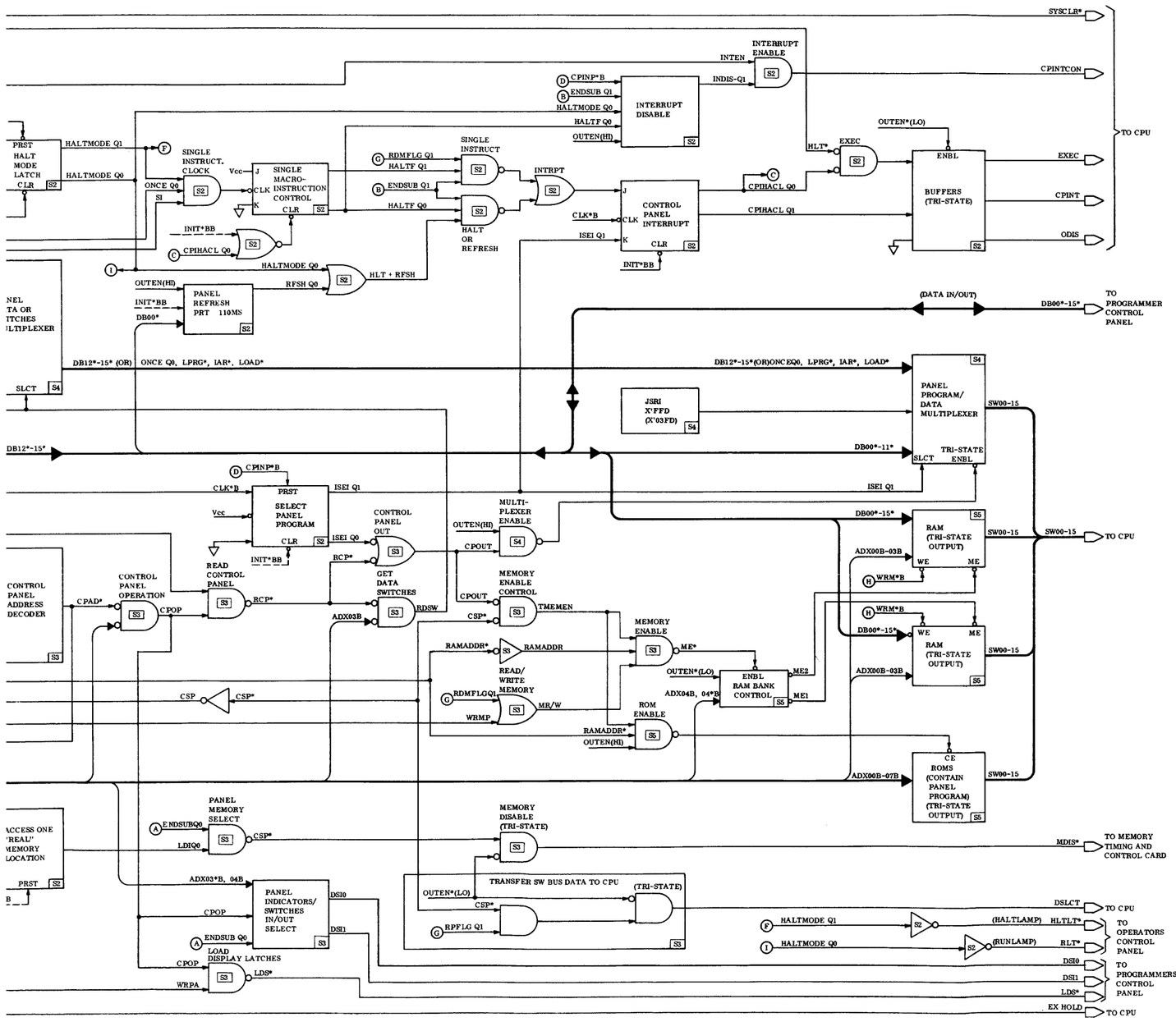


Figure 2/7-12

INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.



DEFINITIONS OF INCLUDED MNEMONICS/ABBREVIATIONS

MNEMONIC/ABBREVIATION	DEFINITION
ADX 00-10	ADDRESS BITS 00-10
BDO 00-15	BUFFERED DATA OUT BITS 00-15
C45	CLOCK 45
CLK	CLOCK
CLK 81	CLOCK 81
CLK*B	CLOCK*BUFFERED
CLR	CLEAR
CPAD	CONTROL PANEL ADDRESS
CPIHACL	CONTROL PANEL INTERRUPT HALT CONTROL
CPINP	CONTROL PANEL INPUT
CPINPB	CONTROL PANEL INPUT BUFFERED
CPINT	CONTROL PANEL INTERRUPT
CPINT CON	CONTROL PANEL INTERRUPT CONTROL
CPOP	CONTROL PANEL OPERATION
CPOUT	CONTROL PANEL OUTPUT
CSP	CHIP SELECT PANEL
DB 00-15	DATA BITS 00-15
DSI 0, 1	DATA SWITCH/INDICATORS 0, 1
ENA 1, 2	ENABLE 1, 2
END SUB	END OF SUBROUTINE (PANEL)
EXEC	EXECUTE
EX HOLD	EXTRA HOLD (CLOCK 4)
HLT	HALT
HLT + RFSH	HALT OR REFRESH
HLT LT	HALT LIGHT
HLTS	HALT SWITCH
IAR	INCREMENT ADDRESS REGISTER
INT	INITIATE
INIT*BB	INITIATE* BUFFERED TWICE
INTEN	INTERRUPT ENABLE
LDI	LOAD IMMEDIATE
LDS	LOAD DISPLAY LATCHES
LOCKS	LOCK SWITCH
LPRG	LOAD PROGRAM
LPRGS	LOAD PROGRAM SWITCH
MDIS	MEMORY DISABLE
ME 1, 2	MEMORY ENABLE 1, 2
MR/W	MEMORY READ/WRITE
ODIS	OUTPUT DISABLE
OUTEN	OUTPUT ENABLE
PPP	PROGRAMMER PANEL CARD IN PLACE
PRST	PRESET
RAMADDR	RAM ADDRESS
RCP	READ CONTROL PANEL
RDM	READ MEMORY
RDMFLG	READ MEMORY FLAG
RDSW	READ SWITCHES
ROUT CPAD 1	REGISTER OUT, CONTROL PANEL ADDRESS, 1
RPFLG	READ PERIPHERAL FLAG
RFSH	REFRESH
SI	SINGLE INSTRUCTION
SLCT	SELECT
SW 00-15	SWITCHED BITS 00-15
SW 1, 2, 3	SWITCH 1, 2, 3
SYSCLRS	SYSTEM CLEAR SWITCH
TMEMEN	TRANSPARENT MEMORY ENABLE
WRM	WRITE MEMORY
WRMB	WRITE MEMORY BUFFERED
WRMP	WRITE MEMORY PERIPHERAL
WRPA	WRITE PERIPHERAL A

NOTES

1. '*' DENOTES NEGATIVE TRUE SIGNAL STATE
2. NUMBERS PRECEDED BY "S" WITHIN FUNCTIONAL BLOCKS DENOTE ASSOCIATED SCHEMATIC SHEET NUMBERS.

DSI0/DSI1 TRUTH TABLE

DSI0	DSI1	OPERATION
LOW	LOW	WRITE DATA INTO PROGRAM COUNTER/MEMORY ADDRESS LATCHES WHEN LDS* TRUE
LOW	HIGH	READ STATUS OF DATA SWITCHES
HIGH	LOW	WRITE DATA INTO DATA DISPLAY LATCHES WHEN LDS* IS TRUE
HIGH	HIGH	READ DISPLAY SELECTOR SWITCH POSITION

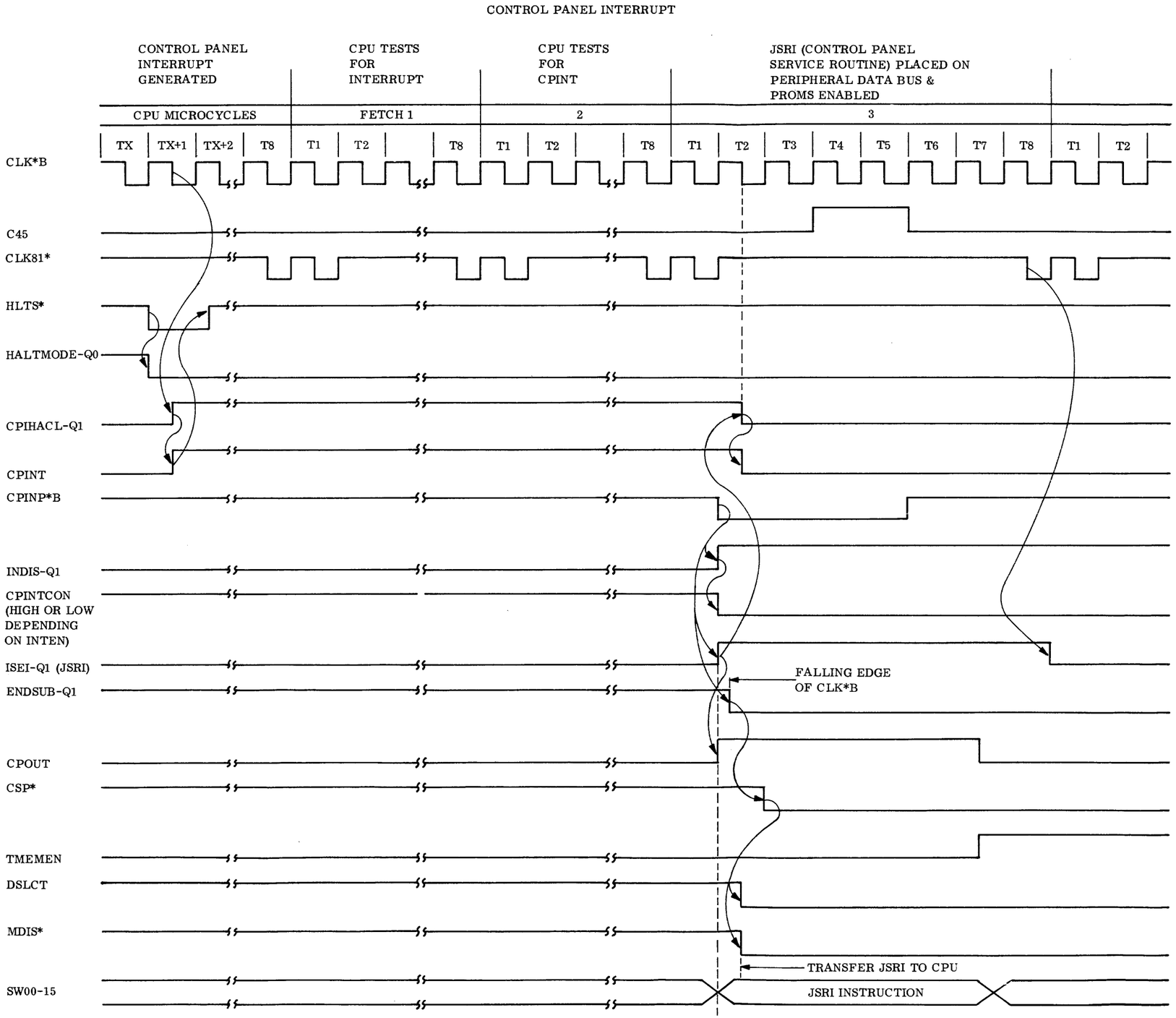
Control Panel Service Routine RIN/ROUT Instructions

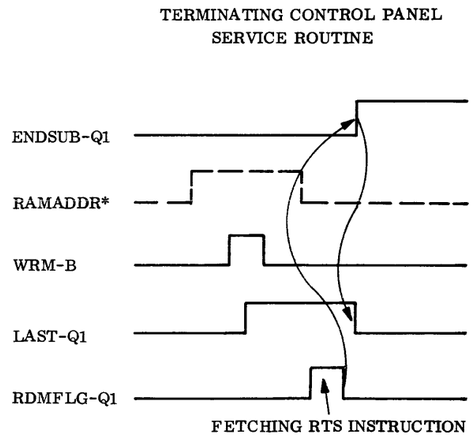
INSTRUCTION			
Type	Function	Mnemonic	Control Field Value
RIN	Get Control Panel Command Switches	GPCS	X'18
RIN	Get Control Panel Data Switches	GDS	X'10
ROUT	Load Control Panel Program Counter Display Register	LPCDR	X'00
ROUT	Load Control Panel Data Register	LDR	X'08
ROUT	Enable User Memory	EUM	X'01

Transparent Memory Locations of Saved CPU Contents

Transparent Memory Location (Hexadecimal)	CPU Contents
FF01	AC0
FF02	AC1
FF03	AC2
FF04	AC3
FF05	Program Counter (current top-of-stack). Displayed PC.
FF06	Previous top-of-stack. Stack display word.
FF07-FF14	Stack 1 through stack 14, respectively
FF15	Displayed flags
FF16	RALU flags
FF17	Memory Address Pointer
FF18-FF1F	Scratch pad (unused)

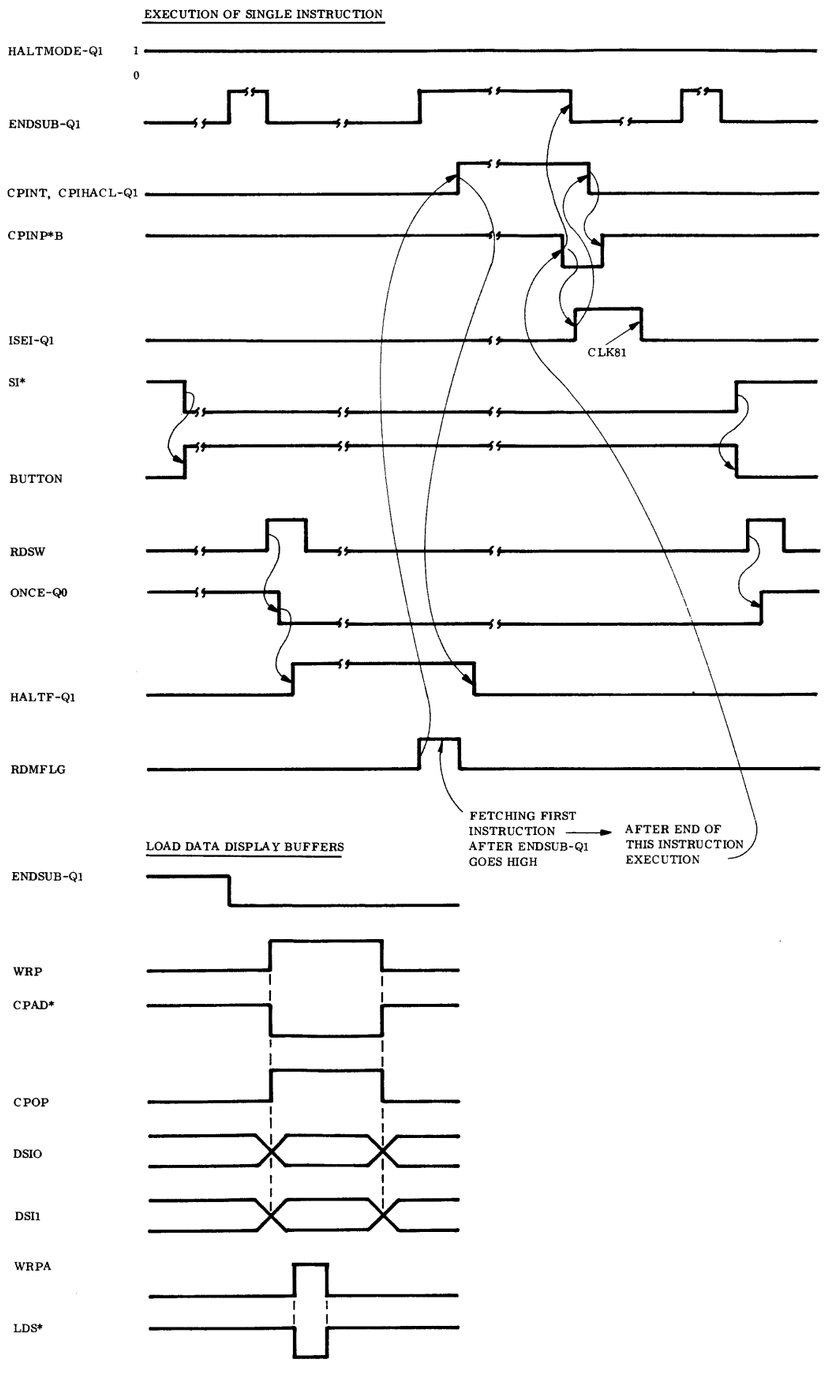
Figure 2/7-12. Control Panel Interface Card Functional Block Diagram

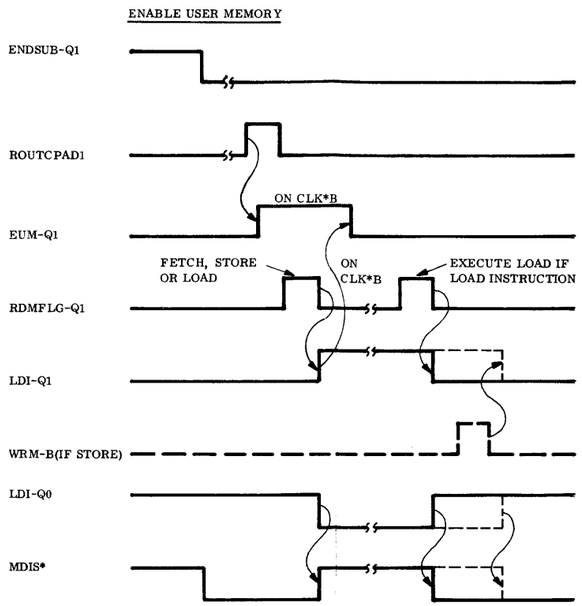




INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

Figure 2/7-13. Control Panel Interface Card Timing Diagram (Sheet 1 of 2)





INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

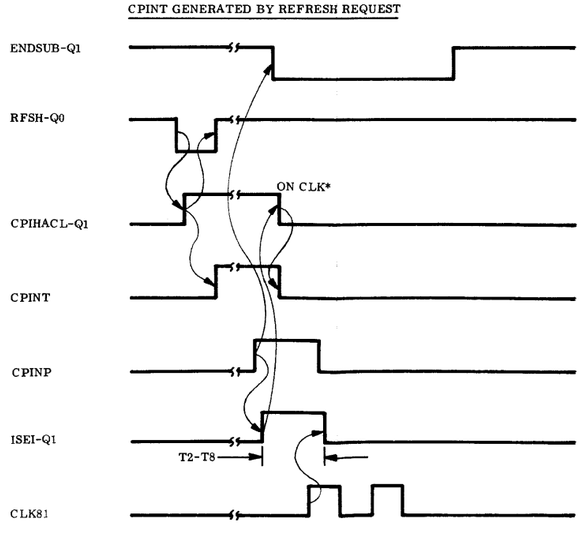
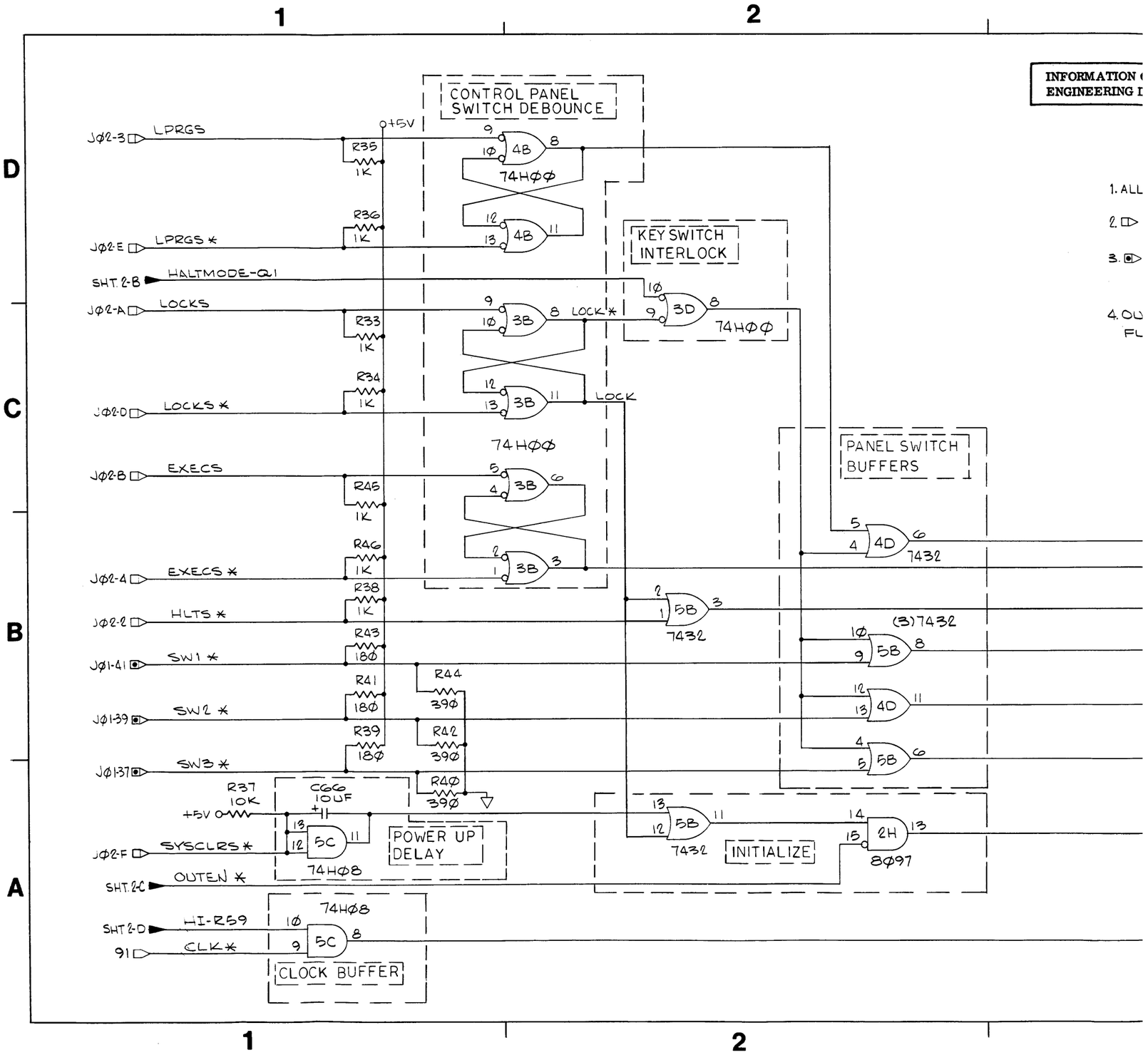


Figure 2/7-13. Control Panel Interface Card Timing Diagram (Sheet 2 of 2)


1
2
D
C
B
A
INFORMATION
ENGINEERING
1. ALL
2.
3.
4. OU
FL
CONTROL PANEL
SWITCH DEBOUNCE
KEY SWITCH
INTERLOCK
PANEL SWITCH
BUFFERS
POWER UP
DELAY
INITIALIZE
CLOCK BUFFER
+5V
J02-3 LPRGS
R35 1K
J02-E LPRGS *
R36 1K
SHT 2-B HALTMODE-Q1
J02-A LOCKS
R33 1K
J02-D LOCKS *
R34 1K
74H00
4B
3B
3D
LOCK *
LOCK
J02-B EXECS
R45 1K
J02-4 EXECS *
R46 1K
J02-2 HLTS *
R38 1K
J01-41 SW1 *
R43 180
J01-39 SW2 *
R41 180
J01-37 SW3 *
R39 180
R44 390
R42 390
R40 390
R37 10K
C66 10UF
J02-F SYSCLRS *
74H08
5C
SHT 2-C OUTEN *
SHT 2-D HI-R59
91 CLK *
5B
7432
4D
(3)7432
4O
2H
8097

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1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5% UNLESS OTHERWISE SPECIFIED
2. ▷ DENOTES CARD EDGE CONNECTOR FOR CABLE TO OPERATORS CONTROL PANEL.
3. ▷ DENOTES CARD EDGE CONNECTOR FOR CABLE TO PROGRAMMERS CONTROL PANEL.
4. OUTLINED CIRCUITRY CORRESPONDS TO FUNCTIONAL BLOCKS ON BLOCK DIAGRAM.

CONTROL PANEL SWITCH DEBOUNCE
KEY SWITCH INTERLOCK
PANEL SWITCH BUFFERS
POWER UP DELAY
INITIALIZE
CLOCK BUFFER

LPRGS
LPRGS *
HALTMODE-Q1
LOCKS
LOCKS *
EXECS
EXECS *
HLTS *
SW1 *
SW2 *
SW3 *
+5V
SYSCLRS *
OUTEN *
HI-R59
CLK *
LOCK *
LOCK
R35 1K
R36 1K
R33 1K
R34 1K
R45 1K
R46 1K
R38 1K
R43 18Ø
R41 18Ø
R39 18Ø
R44 39Ø
R42 39Ø
R4Ø 39Ø
R37 10K
C66 10UF
74HØØ
74HØ8
7432
8Ø97
(3)7432

VCC ▷ JØ2-Ø1
GND ▷ JØ2-Ø6

LPRG * → SHT. 2-B, 4C
RUN → SHT. 2-B
HALTS * → SHT. 2-B
S1 * → SHT. 2-B
IAR * → SHT. 2-A, 4C
LOAD * → SHT. 2-A, 4B
SYSCLR * → 22
CLK*B → SHT. 2-C, 3-A

Figure 2/7-14. Control Panel Interface Card Schematic Diagram (Sheet 1 of 5)

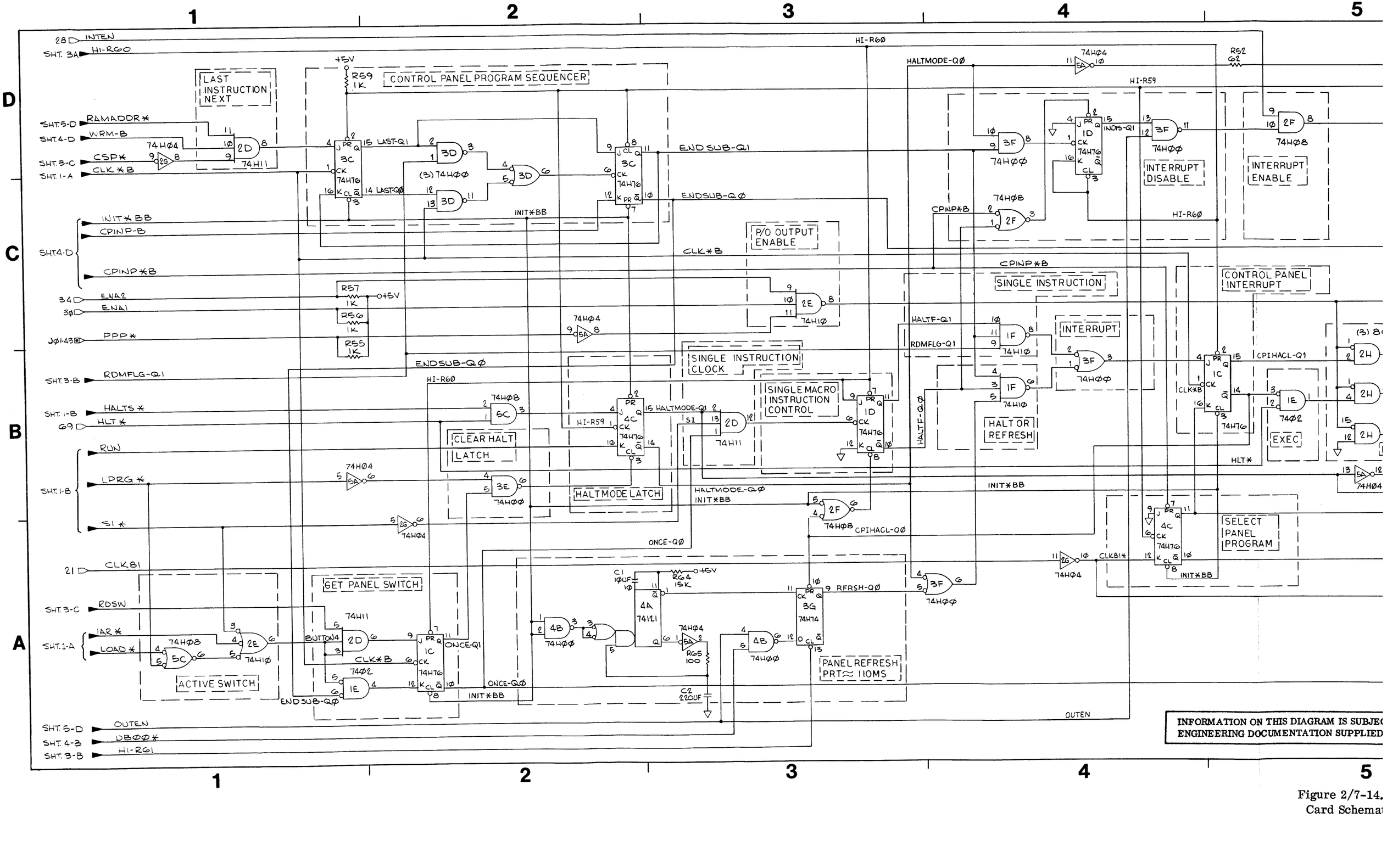
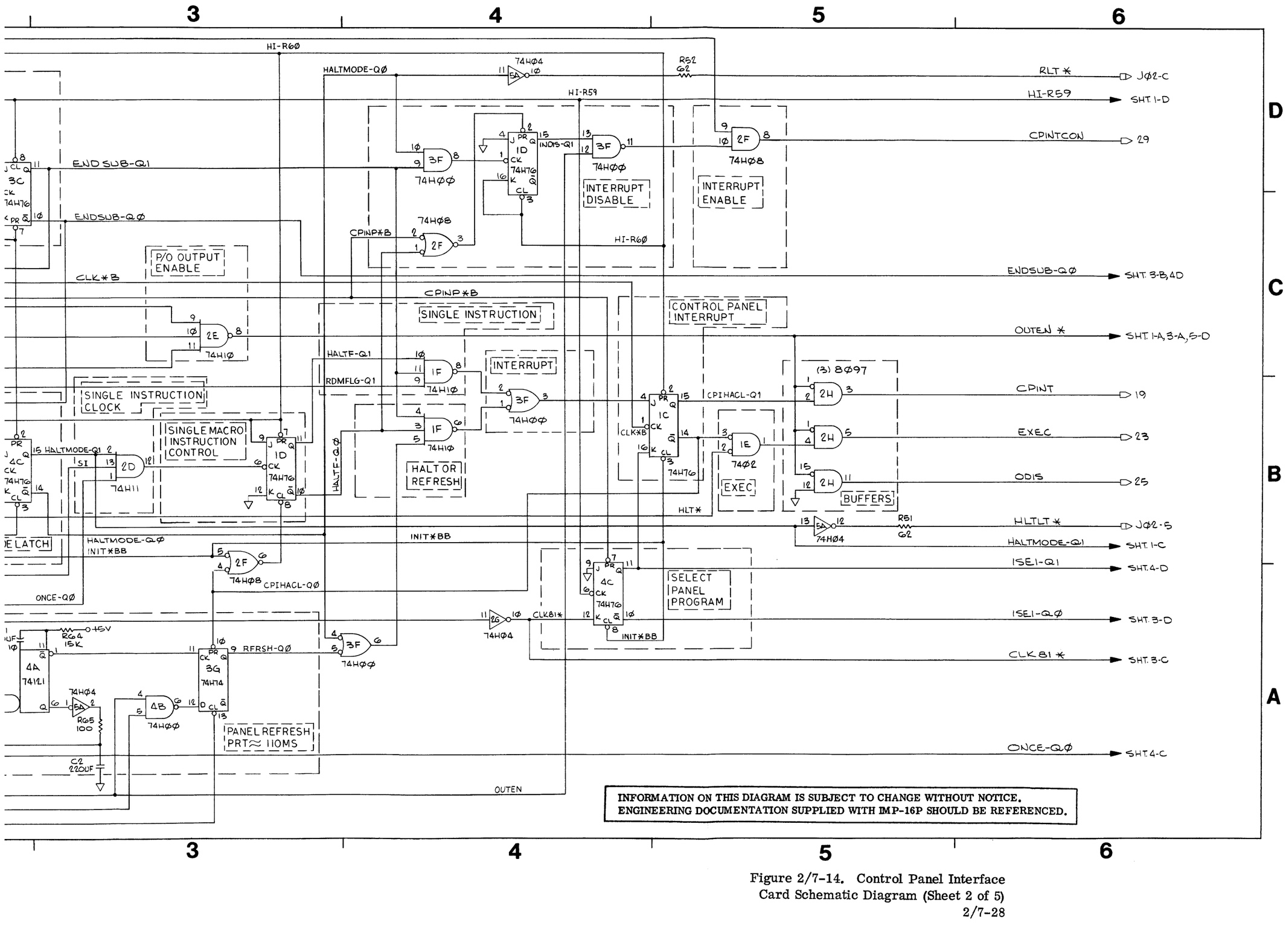
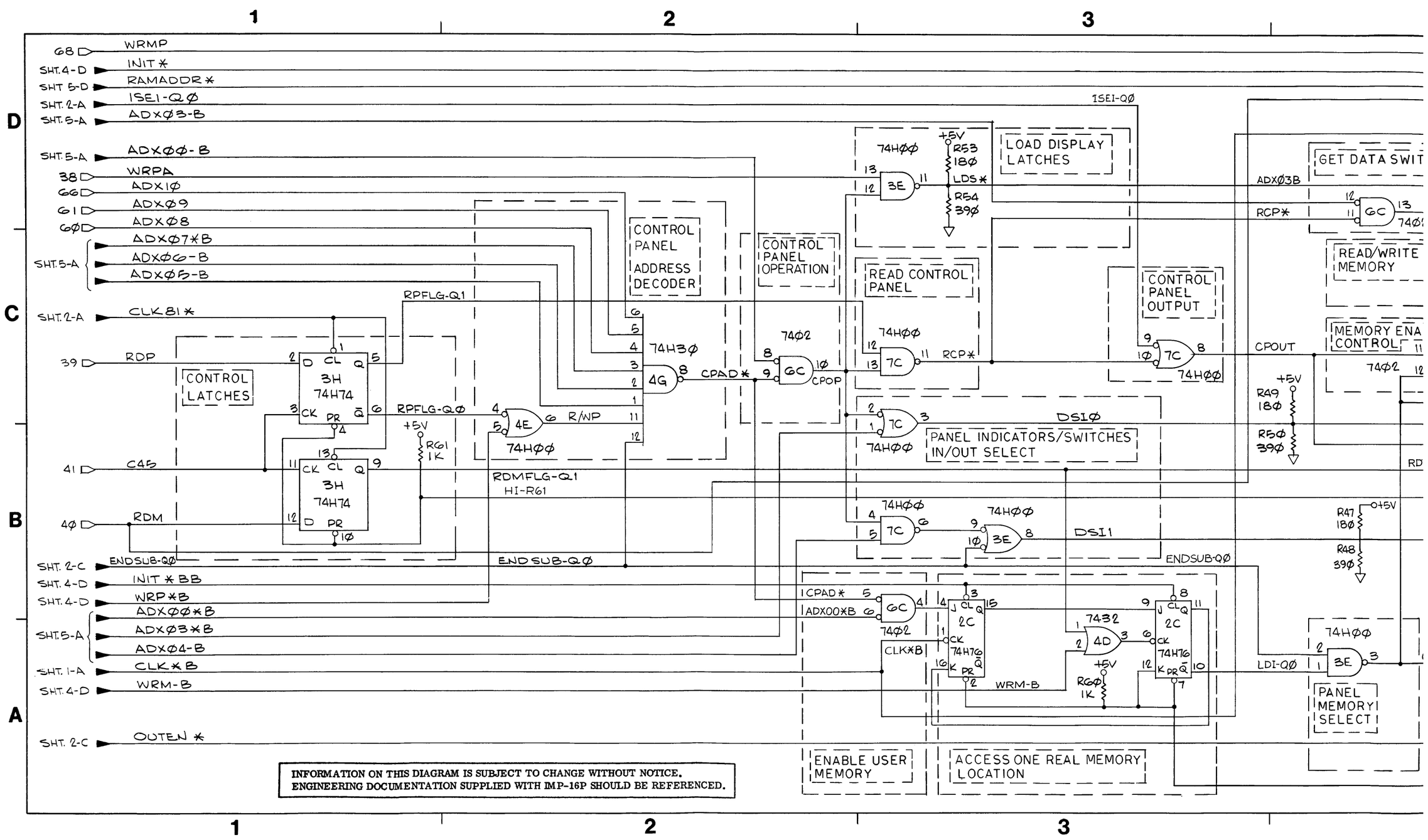


Figure 2/7-14.
Card Schema



INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE. ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.

Figure 2/7-14. Control Panel Interface Card Schematic Diagram (Sheet 2 of 5)



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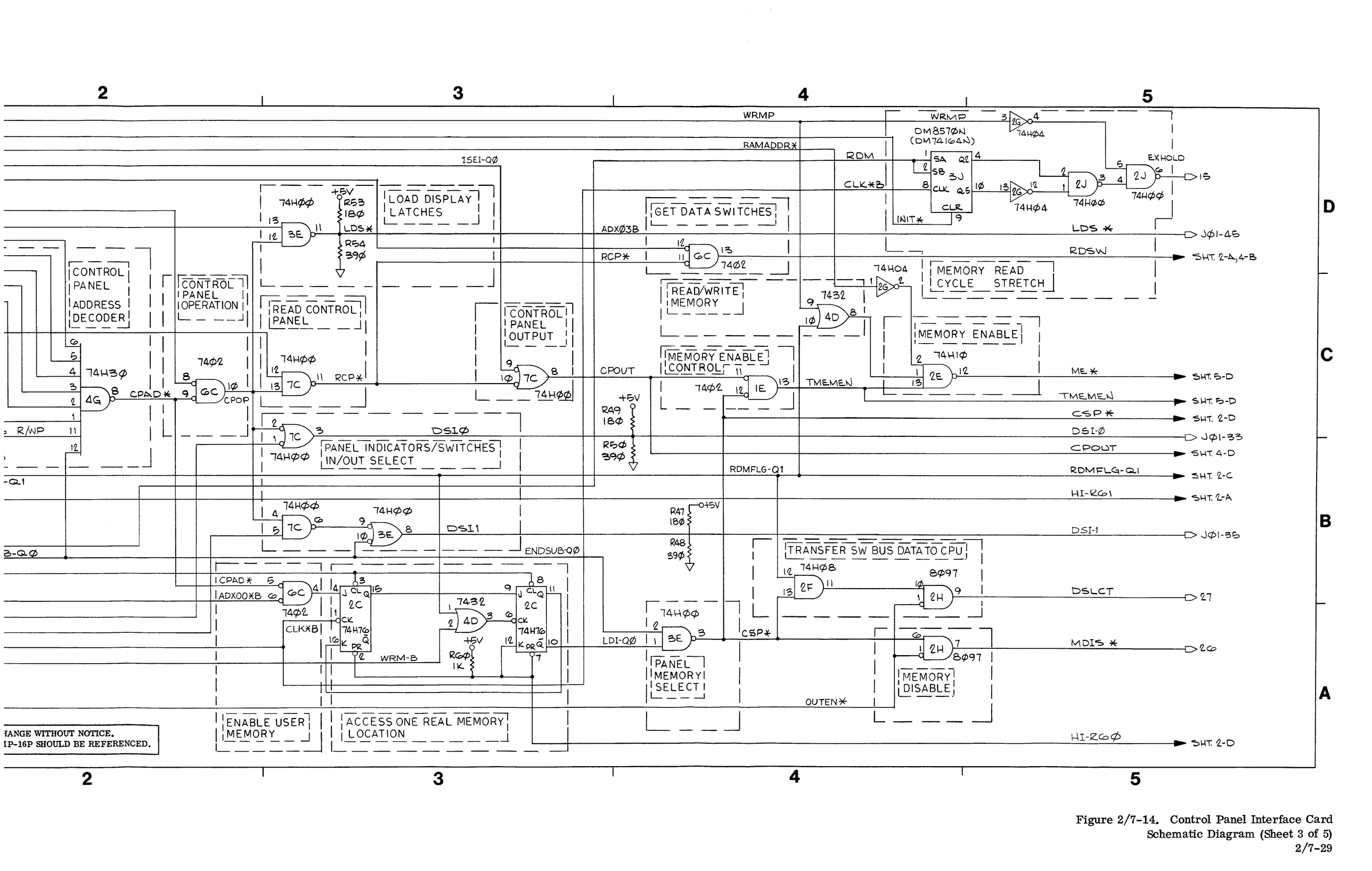
2
3
4
5
D
C
B
A
WRMP
RAMADDR*
ISEI-QØ
CONTROL PANEL ADDRESS DECODER
CONTROL PANEL OPERATION
READ CONTROL PANEL
CONTROL PANEL OUTPUT
LOAD DISPLAY LATCHES
PANEL INDICATORS/SWITCHES IN/OUT SELECT
GET DATA SWITCHES
READ/WRITE MEMORY
MEMORY ENABLE CONTROL
MEMORY READ CYCLE STRETCH
MEMORY ENABLE
TRANSFER SW BUS DATA TO CPU
PANEL MEMORY SELECT
MEMORY DISABLE
ENABLE USER MEMORY
ACCESS ONE REAL MEMORY LOCATION
DM8570N (DM74164N)
74HØØ
74HØ4
74H3Ø
74ØØ
74ØØ
74ØØ

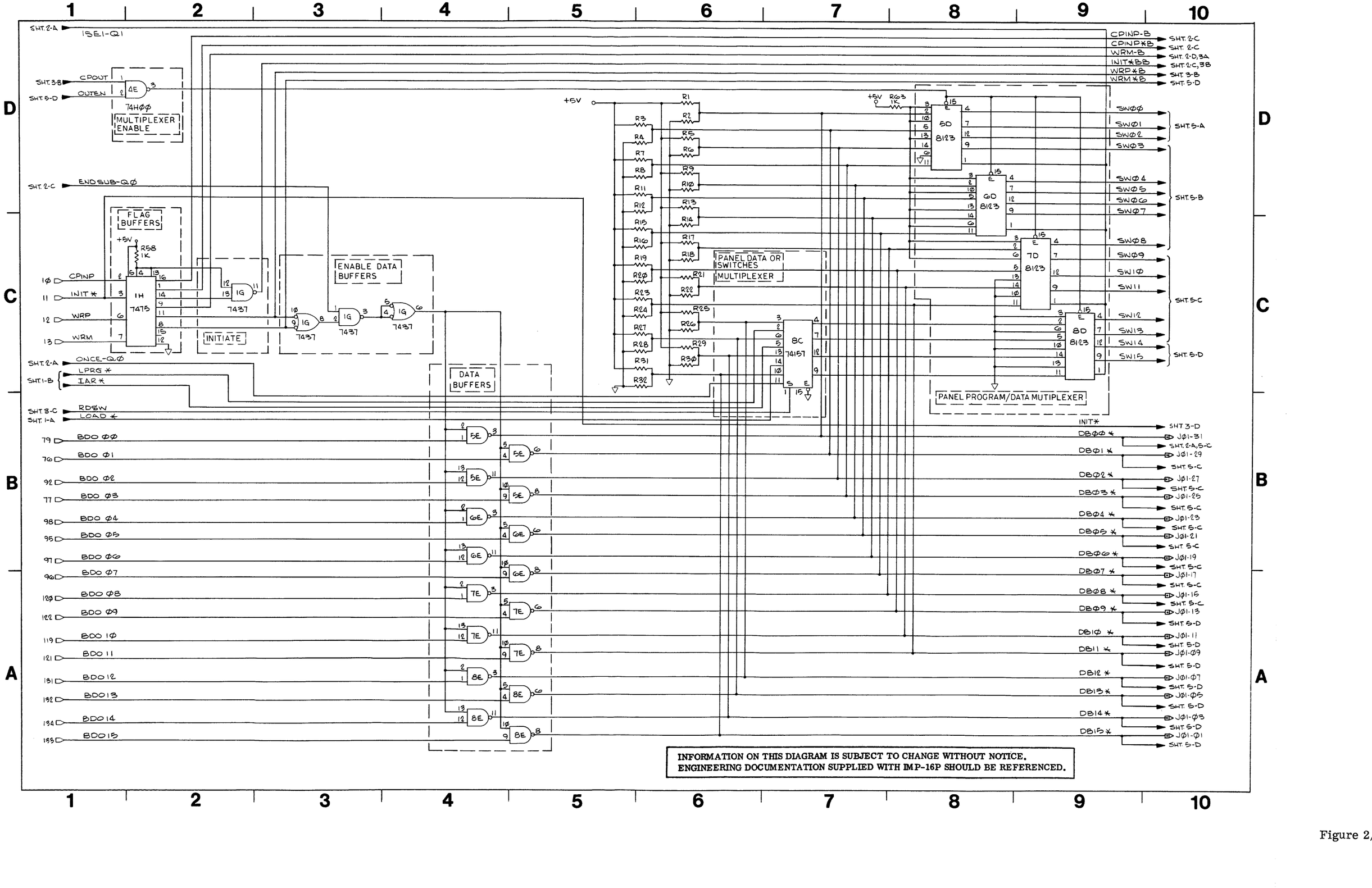
1 2 3 4 5 6 7 8 9 10
SHT. 2-A
1SE1-Q1
SHT. 3-B
CPOUT
SHT. 5-D
OUTEN
4E
74HØØ
MULTIPLEXER ENABLE
SHT. 2-C
ENDSUB-QØ
FLAG BUFFERS
+5V
R58 1K
1Ø CPINP
11 INIT*
12 WRP
13 WRM
1H 7475
INITIATE
1G 7437
ENABLE DATA BUFFERS
SHT. 2-A
ONCE-QØ
SHT. 1-B
LPRG*
IAR*
SHT. 3-C
SHT. 1-A
RDSW
LOAD*
DATA BUFFERS
79 BDO ØØ
76 BDO Ø1
92 BDO Ø2
77 BDO Ø3
98 BDO Ø4
95 BDO Ø5
97 BDO Ø6
96 BDO Ø7
120 BDO Ø8
122 BDO Ø9
119 BDO 1Ø
121 BDO 11
131 BDO 12
132 BDO 13
134 BDO 14
133 BDO 15
5E
6E
7E
8E
+5V
R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32
PANEL DATA OR SWITCHES MULTIPLEXER
8C 74157
+5V R63 1K
5D 8123
6D 8123
7D 8123
8D 8123
SWØØ SWØ1 SWØ2 SWØ3 SHT. 5-A
SWØ4 SWØ5 SWØ6 SWØ7 SHT. 5-B
SWØ8 SWØ9 SW1Ø SW11 SHT. 5-C
SW12 SW13 SW14 SW15 SHT. 5-D
PANEL PROGRAM/DATA MUTIPLEXER
CPINP-B SHT. 2-C
CPINP*B SHT. 2-C
WRM-B SHT. 2-D,3A
INIT*BB SHT. 2-C,3B
WRP*B SHT. 3-B
WRM*B SHT. 5-D
INIT* SHT 3-D
DBØØ* J01-31 SHT. 2-A,5-C
DBØ1* J01-29 SHT. 5-C
DBØ2* J01-27 SHT. 5-C
DBØ3* J01-25 SHT. 5-C
DBØ4* J01-23 SHT. 5-C
DBØ5* J01-21 SHT. 5-C
DBØ6* J01-19 SHT. 5-C
DBØ7* J01-17 SHT. 5-C
DBØ8* J01-15 SHT. 5-C
DBØ9* J01-13 SHT. 5-D
DB1Ø* J01-11 SHT. 5-D
DB11* J01-Ø9 SHT. 5-D
DB12* J01-Ø7 SHT. 5-D
DB13* J01-Ø5 SHT. 5-D
DB14* J01-Ø3 SHT. 5-D
DB15* J01-Ø1 SHT. 5-D
INFORMATION ON THIS DIAGRAM IS SUBJECT TO CHANGE WITHOUT NOTICE.
ENGINEERING DOCUMENTATION SUPPLIED WITH IMP-16P SHOULD BE REFERENCED.
A B C D

Figure 2/7-14

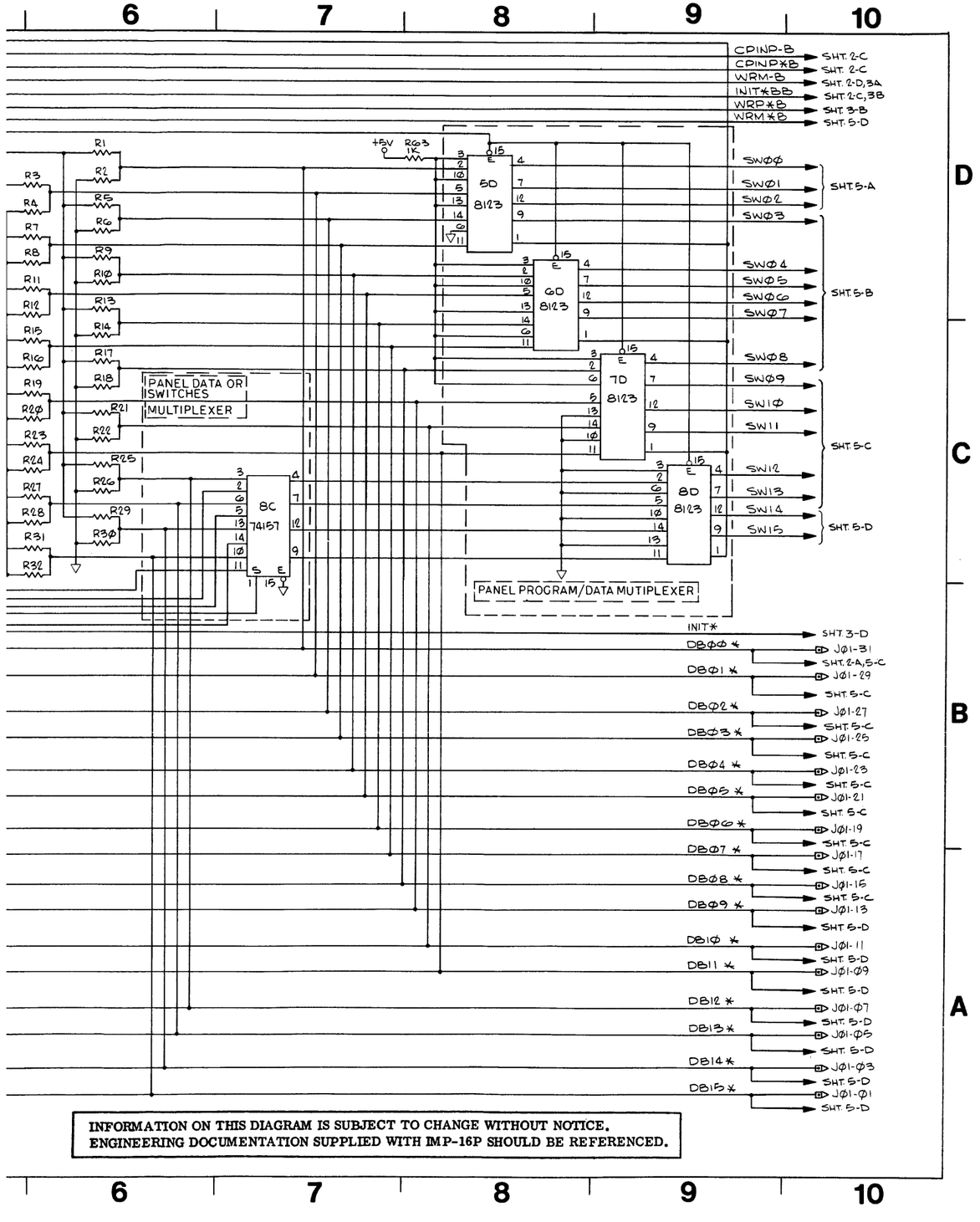

Figure 2/7-14. Control Panel Interface Card Schematic Diagram (Sheet 4 of 5)

SHT. 2-C OUTEN *
SHT. 3-C TMEEN
SHT. 3-C ME *
SHT. 4-D WRM *B
SHT. 4-A DB15 * DB14 * DB13 * DB12 * DB11 * DB10 * DBØ9 * DBØ8 *
SHT. 4-B DBØ7 * DBØ6 * DBØ5 * DBØ4 * DBØ3 * DBØ2 * DBØ1 * DBØØ *

P/O OUTPUT ENABLE — 4F — 74H1Ø — OUTEN * — OUTEN
TMEMEN
RAM ADDRESS DECODER — 4F — 74H1Ø — PROM ENABLE — RAM ADDR *
RAM BANK CONTROL — ADXØ4*B — 1E — 74Ø2 — 4E — 74HØØ — ME1 — ADXØ4-B — 4E — 74HØØ — ME2
ME *

-12V
+5V
C3 33UF, 20V
RG2 1K

82 ADXØØ — 83 ADXØ1 — 87 ADXØ2 — 88 ADXØ3 — 58 ADXØ4 — 59 ADXØ5 — 62 ADXØ6 — 63 ADXØ7

5H 7475 — 16 ADXØØ-B, 1 ADXØØ*B, 15 ADXØ1-B, 1Ø ADXØ2-B, 9 ADXØ3-B, 8 ADXØ3*B
4H 7475 — 16 ADXØ4-B, 1 ADXØ4*B, 15 ADXØ5-B, 14 ADXØ5*B, 1Ø ADXØ6-B, 11 ADXØ6*B, 9 ADXØ7-B, 8 ADXØ7*B

ADDRESS LATCHES

ADXØØ-B ADXØ1-B ADXØ2-B ADXØ3-B ADXØ4-B ADXØ5-B ADXØ6-B ADXØ7-B

7H MM 52Ø3 (LSB) — CE VLL A9 VDD — A1 A2 A3 A4 A5 A6 A7 A8 — B1 B2 B3 B4 B5 B6 B7 B8 — P VBB VSS C — SWØØ SWØ1 SWØ2 SWØ3 SWØ4 SWØ5 SWØ6 SWØ7
6H MM 52Ø3 (MSB) — CE VLL A9 VDD — A1 A2 A3 A4 A5 A6 A7 A8 — B1 B2 B3 B4 B5 B6 B7 B8 — P VBB VSS C — SWØ8 SWØ9 SWIØ SWI1 SWI2 SWI3 SWI4 SWI5

PROMS (CONTAIN PANEL PROGRAM)

99,100 -12V
5-8, 137-140 +5V
1-4,71,72, 141-144 GROUND
C4 33µf 10V
C5 33µf 10V
C6-C65 0.1µf TYPICAL

RAM 1

5F 8599 — ME WE DI D2 D3 D4 — AØ A1 A2 A3 — S1 S2 S3 S4 — SWØØ SWØ1 SWØ2 SWØ3
6F 8599 — SWØ4 SWØ5 SWØ6 SWØ7
7F 8599 — SWØ8 SWØ9

RAM 2

5G 8599 — SWØØ SWØ1 SWØ2 SWØ3
6G 8599 — SWØ4 SWØ5 SWØ6 SWØ7
7G 8599 — SWØ8 SWØ9

INFORMATION ON THIS DIAGRAM IS SUBJECT TO
ENGINEERING DOCUMENTATION SUPPLIED WITH

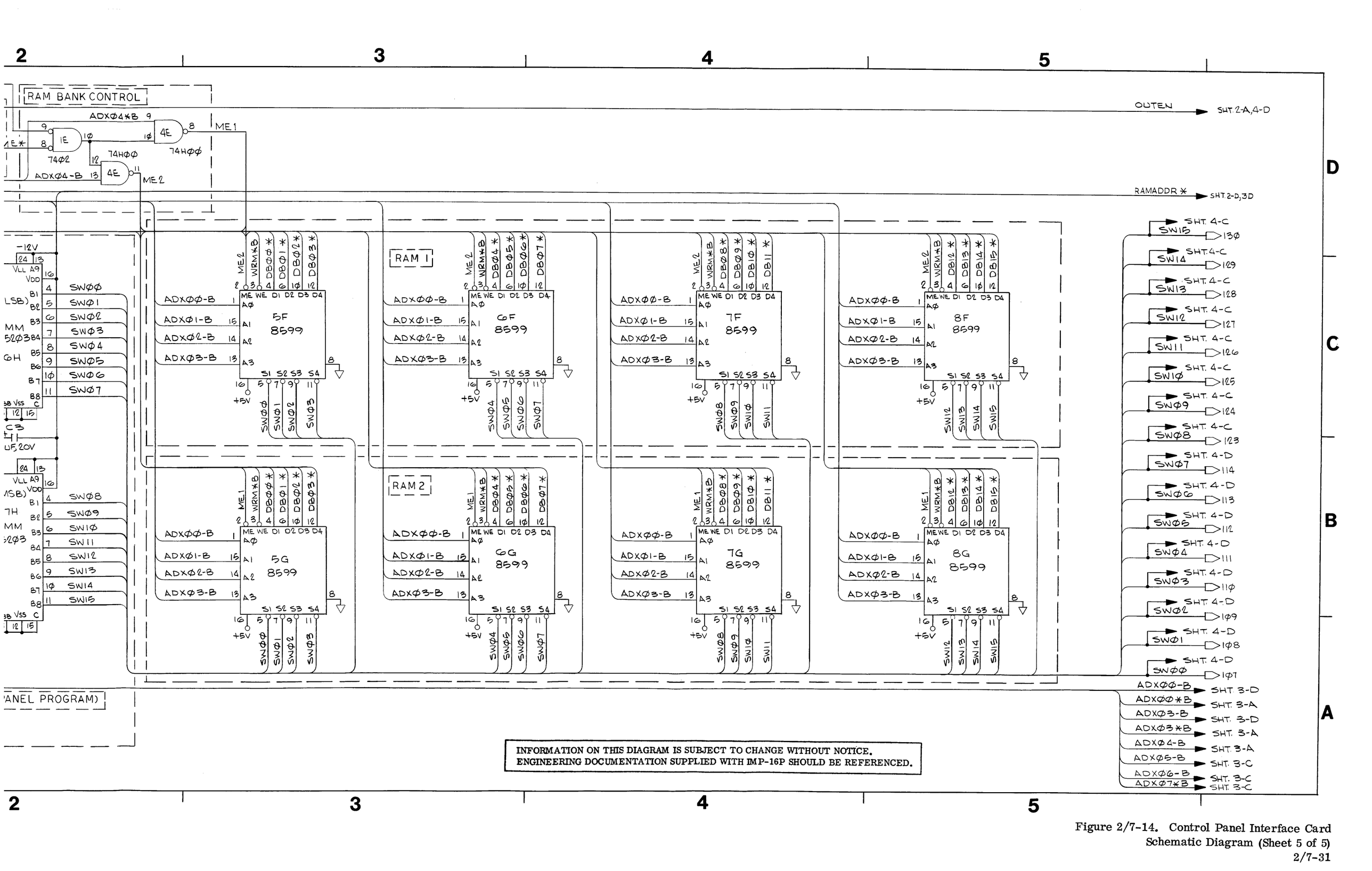

Figure 2/7-14. Control Panel Interface Card Schematic Diagram (Sheet 5 of 5)

Appendix A
LIST OF MNEMONICS/ABBREVIATIONS

Table A-1. IMP-16P Mnemonics/Abbreviations, Definitions and Sources

Mnemonic/ Abbreviation	Definition	Source/Reference
A0-A9	Memory Chip Row Address Bits 0-9	Memory Storage Card
AB00-15	Buffered Address Bits 00-15	TTY/Card Reader Interface Card
ABSCR	Absolute Card Reader Loader Routine	In ROM on TTY/Card Reader Interface Card
ABSTTY	Absolute Paper Tape LM Loader Routine	In ROM on TTY/Card Reader Interface Card
ADLCHLD	Address Latch Load	Memory Timing and Control Card
ADX00-15	Unbuffered Address Bits 00-15	CPU Card
AEN1, 2	Address Enable 1, 2	TTY/Card Reader Interface Card
AUX1, 2	Auxiliary Switches 1, 2	Operators Control Panel
BDO00-15	Buffered Data Out Bits 00-15	CPU Card
BSPGEN	Base Page Enable	TTY/Card Reader Interface Card
C45	Clock 45	CPU Card
CE	Chip Enable	Memory Storage Card
CI	Cycle Initiate	Memory Timing and Control Card
CLK	Clock	- -
CLK81	Clock 81	CPU Card
CLK*B	Clock * Buffered	Control Panel Interface Card
CLKENBL	Clock Enable	Memory Timing and Control Card
CLMCTL	Column Control	Memory Timing and Control Card
CLPK	Clear Pick	TTY/Card Reader Interface Card
CLR	Clear	- -
CNVRT	Convert Buffer to Hex Subroutine	In ROM on TTY/Card Reader Interface Card
CPAD	Control Panel Address	Control Panel Interface Card
CPIHACL	Control Panel Interrupt Halt Control	Control Panel Interface Card
CPINP	Control Panel Input	CPU Card
CPINPB	Control Panel Input Buffered	Control Panel Interface Card

Table A-1. IMP-16P Mnemonics/Abbreviations, Definitions and Sources (Continued)

Mnemonic/ Abbreviation	Definition	Source/Reference
CPINT	Control Panel Interrupt	Control Panel Interface Card
CPINTCON	Control Panel Interrupt Control	Control Panel Interface Card
CPOP	Control Panel Operation	Control Panel Interface Card
CPOUT	Control Panel Output	Control Panel Interface Card
CR	Cycle Request	CPU Card
CRAD	Card Reader Address	TTY/Card Reader Interface Card
CS	Cycle Select	Memory Timing and Control Card
CSCR1, 2	Enable Card Reader Routine ROMs 1 and 2	TTY/Card Reader Interface Card
CSP	Chip Select Panel	Control Panel Interface Card
CVT	Convert Hollerith to Hex Subroutine	In ROM on TTY/Card Reader Interface Card
DB00-15	Data Bits 00-15	Control Panel Interface Card
DI00-15	Data In Bits 00-15	Memory Storage Card
DICTL	Data In Control	Memory Timing and Control Card
DI•EN	Data In and Memory Enable	Memory Storage Card
DINT	Data Interrupt	TTY/Card Reader Interface Card
DO00-15	Data Out Bits 00-15	Memory Storage Card
DOCTL	Data Out Control	Memory Timing and Control Card
DSI0, 1	Data Switch/Indicators 0, 1	Control Panel Interface Card
DTCRD	Data Card Processing Subroutine	In ROM on TTY/Card Reader Interface Card
EN7F	Enable Page 7F	TTY/Card Reader Interface Card
ENA1, 2	Enable 1 and 2	Control Panel Interface Card
ENBL	Enable	- -
ENCRD	End Card Processing Subroutine	In ROM on TTY/Card Reader Interface Card
ENDSUB	End of Subroutine (Panel)	Control Panel Interface Card

Table A-1. IMP-16P Mnemonics/Abbreviations, Definitions and Sources (Continued)

Mnemonic/ Abbreviation	Definition	Source/Reference
EN•MOD0, 1	Memory Enable and Module Select 0, 1	Memory Storage Card
EXEC	Execute	Operators Control Panel
EXHOLD	Extra Hold (Clock 4)	Control Panel Interface Card
GECO	Teletype Get Character with Echo Subroutine	In ROM on TTY/Card Reader Interface Card
GETC	Teletype Get Character Subroutine	In ROM on TTY/Card Reader Interface Card
HLT	Halt	Control Panel Interface Card
HLTLT	Halt Light	Control Panel Interface Card
HLTS	Halt Switch	Operators Control Panel
HLT+RFSH	Halt or Refresh	Control Panel Interface Card
HSPDIN	High Speed Data In	Teletype Transmitter
IAR	Increment Address Register	Control Panel Interface Card
I/F	Interface	- -
INIT	Initiate	CPU Card
INIT*BB	Initiate * Buffered Twice	Control Panel Interface Card
INTEN	Interrupt Enable	CPU Card
INTEST	Teletype In Test Subroutine	In ROM on TTY/Card Reader Interface Card
INTREQ	Interrupt Request	TTY/Card Reader Interface Card
INTRPTENBL	Interrupt Enable	TTY/Card Reader Interface Card
LDI	Load Immediate	Control Panel Interface Card
LDM	Load Multiple Subroutine	In ROM on TTY/Card Reader Interface Card
LDS	Load Display Latches	Control Panel Interface Card
LM	Load Module	- -
LOCKS	Lock Switch	Operators Control Panel
LPRG	Load Program	Control Panel Interface Card

Table A-1. IMP-16P Mnemonics/Abbreviations, Definitions and Sources (Continued)

Mnemonic/ Abbreviation	Definition	Source/Reference
LPRGS	Load Program Switch	Operators Control Panel
MAB0-9	Memory Address Bits 0-9	Memory Timing and Control Card
MDI00-15	Memory Data In Bits 00-15	Memory Timing and Control Card
MDIS	Memory Disable	Control Panel Interface Card
MDISFE, FF	Memory Disable, Page FE and FF	TTY/Card Reader Interface Card
MDO00-15	Memory Data Out, Bits 00-15	Memory Storage Card
ME1, 2	Memory Enable 1, 2	Control Panel Interface Card
MEMBSY	Memory Busy	Memory Timing and Control Card
MEMEN	Memory Enable	Memory Timing and Control Card
MESG	Message Printing Subroutine	In ROM on TTY/Card Reader Interface Card
MODSEL0-7	Module Select 0-7	Memory Timing and Control Card
MR/W	Memory Read/Write	Control Panel Interface Card
ODA	Output Data Available	Memory Timing and Control Card
ODIS	Output Disable	Control Panel Interface Card
ORD1-6	Orders 1-6	TTY/Card Reader Interface Card
OUTEN	Output Enable	Control Panel Interface Card
PCHG	Precharge	Memory Timing and Control Card
PD00-15	Peripheral Data Bits 00-15	TTY/Card Reader Interface Card and Control Panel Interface Card
PPP	Programmers Panel Card In Place	Programmers Panel Card
PRGM	Program	TTY/Card Reader Interface Card
PRST	Preset	- -
PUT2C	Send Two Characters to Teletype Subroutine	In ROM on TTY/Card Reader Interface Card
PUTC	Teletype Put Character Subroutine	In ROM on TTY/Card Reader Interface Card
RAM	Random Access Memory	- -

Table A-1. IMP-16P Mnemonics/Abbreviations, Definitions and Sources (Continued)

Mnemonic/ Abbreviation	Definition	Source/Reference
RAMADDR	RAM Address	Control Panel Interface Card
RCP	Read Control Panel	Control Panel Interface Card
RDCOL	Read and Convert Single Column Subroutine	In ROM on TTY/Card Reader Interface Card
RDCRD	Read Card Subroutine	In ROM on TTY/Card Reader Interface Card
RDEN	Read Enable	TTY/Card Reader Interface Card
RESET	Teletype Reset Subroutine	In ROM on TTY/Card Reader Interface Card
RDM	Read Memory	CPU Card
RDMFLG	Read Memory Flag	CPU Card
RDP	Read Peripheral	CPU Card
RDRON	Reader On	TTY/Card Reader Interface Card
RDSW	Read Switches	Control Panel Interface Card
RDWD	Read and Convert 16-bit Word Subroutine	In ROM on TTY/Card Reader Interface Card
RFADR0-4	Refresh Address 0-4	Memory Timing and Control Card
RFSH	Refresh	Memory Timing and Control Card
RFSHPROG	Refresh In Progress	Memory Timing and Control Card
RFSHREQ	Refresh Required	Memory Timing and Control Card
RLT	Run Light	Control Panel Interface Card
ROM	Read Only Memory	- -
ROUTCPAD1	Register Out, Control Panel Address, 1	Control Panel Interface Card
ROWSEL0-3	Row Select 0-3	Memory Timing and Control Card
RPFLG	Read Peripheral Flag	Control Panel Interface Card
R/W(MOD0, 1)	Read/Write (Module 0, 1)	Memory Storage Card
SAV	Save Registers Subroutine	In ROM on TTY/Card Reader Interface Card

Table A-1. IMP-16P Mnemonics/Abbreviations, Definitions and Sources (Continued)

Mnemonic/ Abbreviation	Definition	Source/Reference
SI	Single Instruction	Control Panel Interface Card
SLCT	Select	- -
SLCTMOD0, 1	Select Module 0, 1	Memory Storage Card
SPCK	Set Pick	TTY/Card Reader Interface Card
STM	Store Multiple Subroutine	In ROM on TTY/Card Reader Interface Card
SW00-15	Switched Bits 00-15	TTY/Card Reader Interface Card and Control Panel Interface Card
SW1, 2, 3	Switch 1, 2, 3	Operators Control Panel
SYSCLR	System Clear	CPU Card
SYSCLRS	System Clear Switch (INIT)	Operators Control Panel
TDOUT	Transmit Data Out	TTY/Card Reader Interface Card
TMEMEN	Transparent Memory Enable	Control Panel Interface Card
TTY	Teletype	- -
TTY1-2	Enable Teletype Routine ROMs 1 and 2	TTY/Card Reader Interface Card
TTYAD	Teletype Address	TTY/Card Reader Interface Card
TTYDIN	Teletype Data In	TTY Transmitter
TTYSTAT	Teletype Status	TTY/Card Reader Interface Card
WP	Write Pulse	Memory Timing and Control Card
WP0, 1	Write Pulse 0, 1	Memory Timing and Control Card
WRM	Write Memory Flag	CPU Card
WRMB	Write Memory Flag Buffered	Control Panel Interface Card
WRMP	Write Memory Peripheral	CPU Card
WRP	Write Peripheral Flag	CPU Card
WRPA	Write Peripheral A	CPU Card

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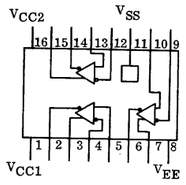

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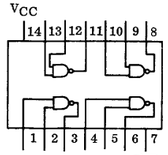

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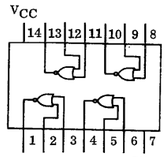

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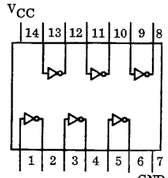

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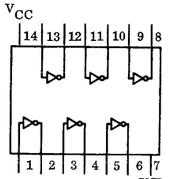

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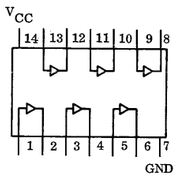

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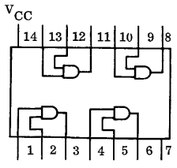

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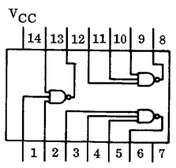

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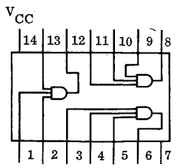

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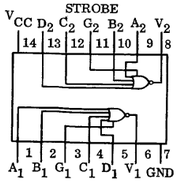

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V = G(A+B+C+D)

TOP VIEW

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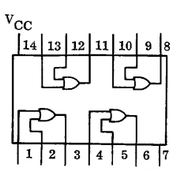

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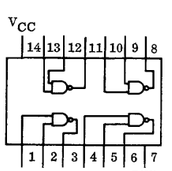

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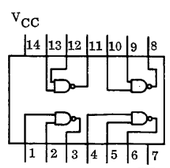

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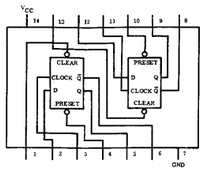

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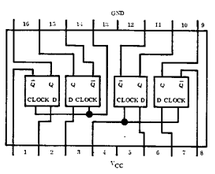

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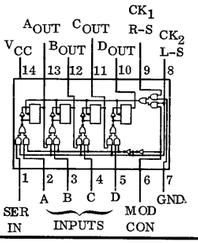

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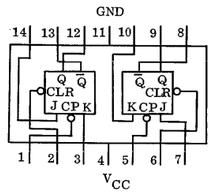

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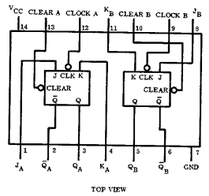

Note: A logic '0' on clear sets Q to logic '0'.

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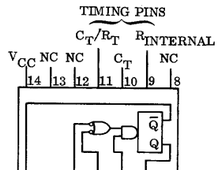

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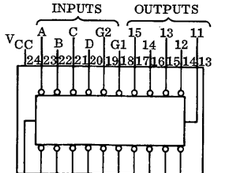

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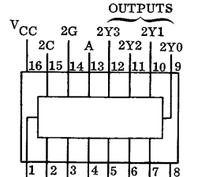

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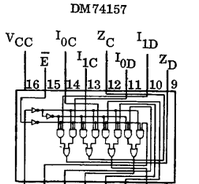

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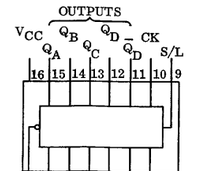

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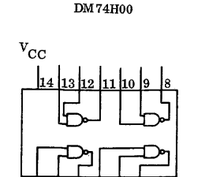

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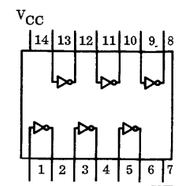

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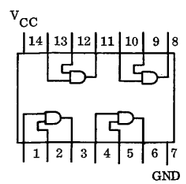

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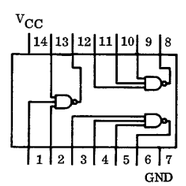

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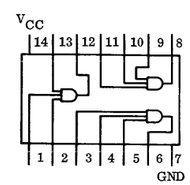

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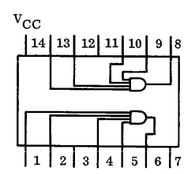

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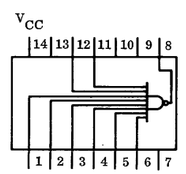

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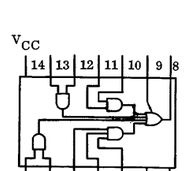

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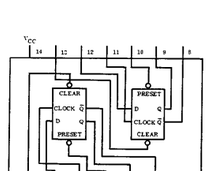

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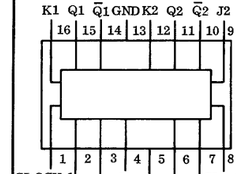

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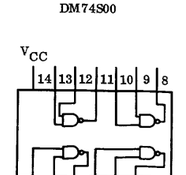

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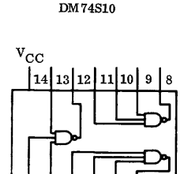

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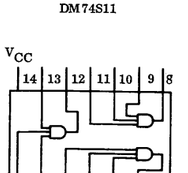

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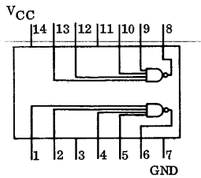

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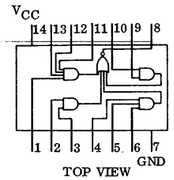

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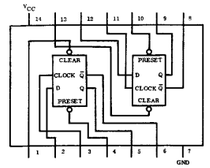

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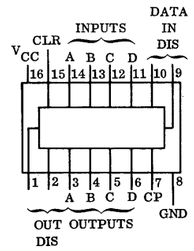

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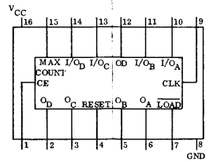

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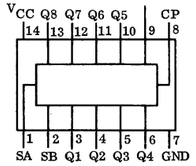

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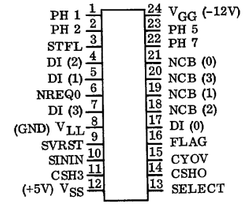

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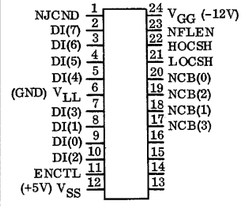

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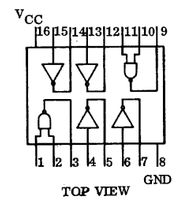

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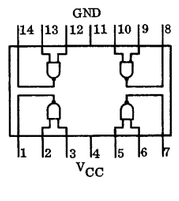

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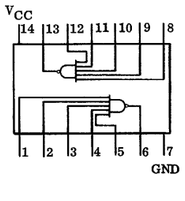

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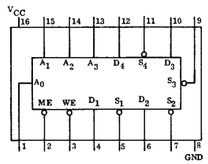

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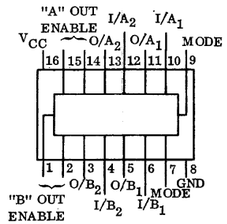

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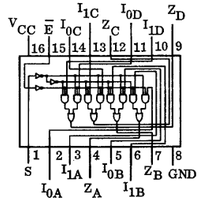

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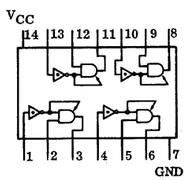

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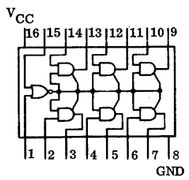

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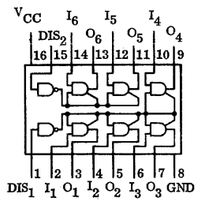

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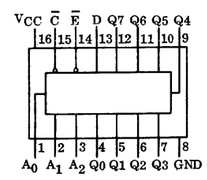

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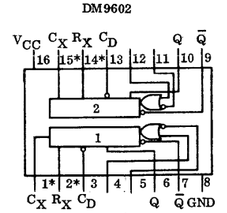

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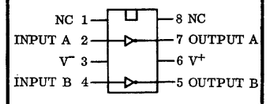

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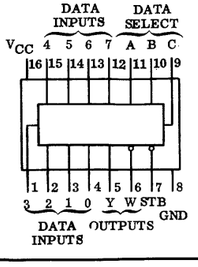

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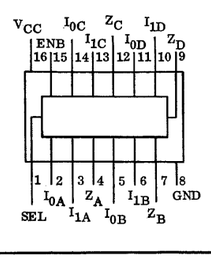

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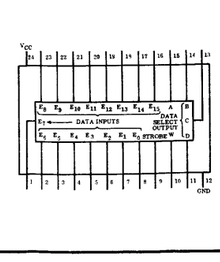

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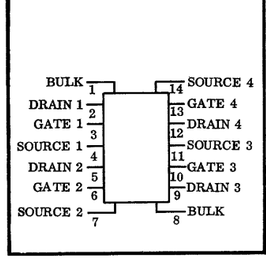

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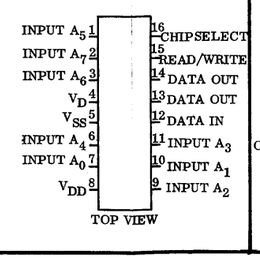

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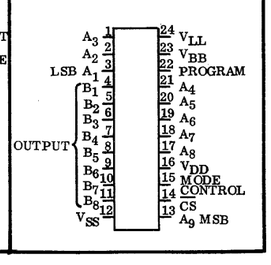

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