NEC

μCOM84/87/78K FAMILIES
70320 (V25)
8/16-BIT MICROCOMPUTER

DATA BOOK

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8/16-BIT MICROCOMPUTER

DATA BOOK

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CHAPTER 1

THE μCOM84 NMOS FAMILY

μPD8041AH/μPD8741A

μPD8035HL/48H

μPD8748H

μPD8039HL/49H/μPD8749H

8-BIT, SINGLE-CHIP NMOS MICROCOMPUTERS WITH UNIVERSAL PPI

DESCRIPTION

The μPD8041AH and μPD8741A are programmable peripheral interface controllers intended for use in master/slave configurations with 8048, 8080A, 8085A, 8086, and other 8- and 16-bit microprocessors. The μPD8041AH/8741A functions as a totally self-sufficient controller with its own program and data memory to effectively unburden the master CPU from I/O handling and peripheral control functions.

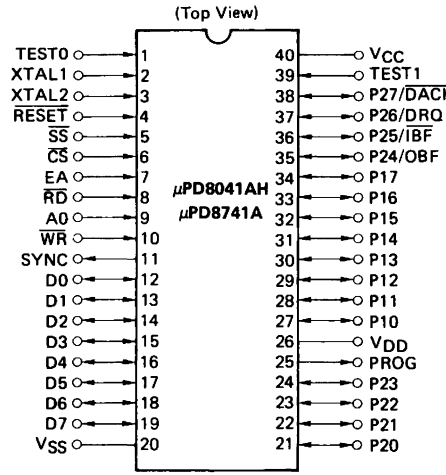
The bus structure and data and status registers of the μPD8041AH/8741A allow easy interface to the master processor bus. This enables the processor to perform control tasks which offload main system processing and more efficiently distribute processing functions.

The μPD8041AH/8741A contains an 8-bit CPU, 1K x 8 program memory, 64 x 8 data memory, 18 I/O lines, a counter/timer, and a clock generator. The program memory for the μPD8041AH is factory maskprogrammed, while program memory for the μPD8741A is UV EPROM for more flexibility.

FEATURES

- Complete single chip microcomputer
  - 8-bit CPU
  - 1K x 8 ROM / UVPROM
  - 64 x 8 RAM
  - 8-bit timer/counter
  - 18 I/O lines
- 8048-, 8080A-, 8085A-, 8086-compatible bus structure
- Asynchronous slave-to-master interface
  - 8-bit status register
  - Two data registers
- Interrupt, DMA, or polled operation
- Expandable I/O
- Single +5V power supply (8041AH)

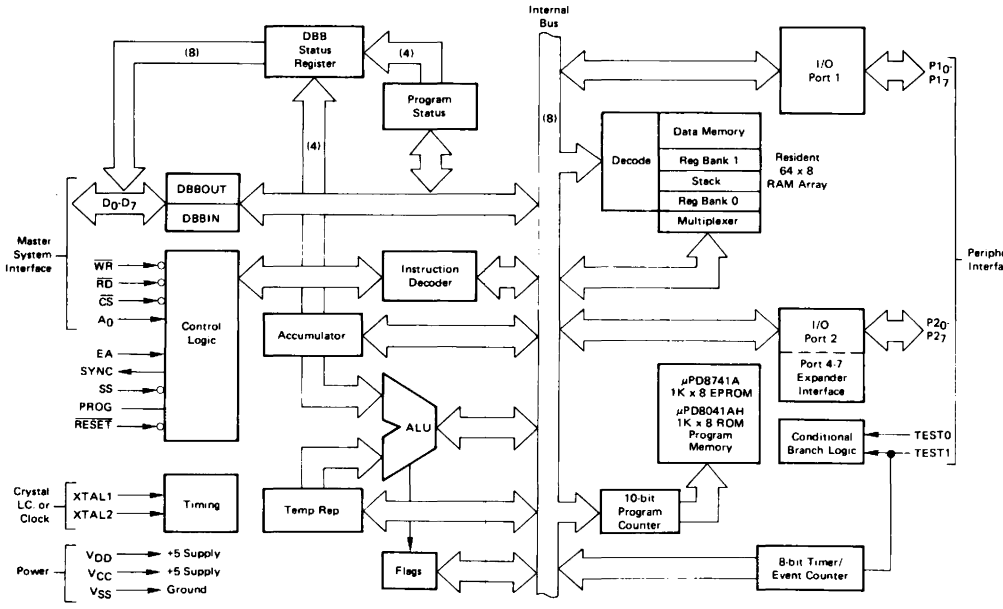
PIN CONFIGURATION



PIN IDENTIFICATION

NO.	SYMBOL	FUNCTION
1	T0	Testable input 0
2	XTAL1	Crystal input 1
3	XTAL2	Crystal input 2
4	$\overline{RESET}$	Reset input
5	$\overline{SS}$	Single step input
6	$\overline{CS}$	Chip select input
7	EA	External access input
8	$\overline{RD}$	Read strobe input
9	A_0	Adress input 0
10	$\overline{WR}$	Write strobe output
11	SYNC	SYNC output
12–19	D_0–D_7	Bidirectional data bus
20	V_{SS}	Ground potential
21–24, 35–38	$P2_0$–$P2_7$	Quasi-bidirectional Port 2
25	PROG	Program pulse output
26	V_{DD}	Programming supply voltage
27–34	$P1_0$–$P1_7$	Quasi-bidirectional Port 1
39	T1	Testable input 1
40	V_{CC}	Primary power supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

Power supply voltage, V_{CC}	−0.5V to +7.0V
Power supply voltage, V_{DD}	−0.5V to +7.0V
Input voltage, V_{IN}	−0.5V to +7.0V
Output voltage, V_O	−0.5V to +7.0V
Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input capacitance	C_I				10	pF
Output Capacitance	C_{IO}				20	pF

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	μPD8741A		μPD8041AH		UNIT
			MIN	MAX	MIN	MAX	
Input voltage low	V_{IL}	All except X1, X2, and $\overline{RESET}$	−0.5	0.8	−0.5	0.8	V
	V_{IL1}	X1, X2, $\overline{RESET}$	−0.5	0.6	−0.5	0.6	V
Input voltage high	V_{IH}	Except X1, X2, and $\overline{RESET}$	2.0	V_{CC}	2.0	V_{CC}	V
	V_{IH1}	X1, X2, $\overline{RESET}$	3.8	V_{CC}	3.8	V_{CC}	V
Output voltage low	V_{OL}	D_0–D_7, SYNC, I_{OL} = 2.0 mA		0.45		0.45	V
	V_{OL1}	Except PROG, I_{OL} = 1.0 mA		0.45		0.45	V
	V_{OL2}	PROG, I_{OL} = 1.0 mA		0.45		0.45	V
Output voltage high	V_{OH}	D_0–D_7, I_{OH} = −400 μA	2.4		2.4		V
	V_{OH1}	All other outputs: I_{OH} = −50 μA	2.4		2.4		V
Input current low	I_{LI}	$P1_0$–$P1_7$, $P2_0$–$P2_7$; V_{IL} = 0.8V		0.5		0.5	mA
	I_{LI1}	$\overline{SS}$, $\overline{RESET}$; V_{IL} = 0.8V		0.2		0.2	mA
Input leakage current	I_{IL}	T0, T1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, EA, A_0, $V_{SS} \leq V_{IN} \leq V_{CC}$		± 10		± 10	μA
Output leakage current	I_{OL}	D_0–D_7, High Z state, V_{SS} +0.45 V ≤ $V_{IN} \leq V_{CC}$		± 10		± 10	μA
Supply current (total)	I_{DD}	V_{DD}		15		15	mA
	$I_{DD} + I_{CC}$			135		125	mA

AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

DBB READ

PARAMETER	SYMBOL	TEST CONDITIONS	μPD8741A		μPD8041AH		UNIT
			MIN	MAX	MIN	MAX	
$\overline{CS}$, A_0 setup to $\overline{RD}$ ↓	t_{AR}		0		0		ns
$\overline{CS}$, A_0 hold after $\overline{RD}$ ↑	t_{RA}		0		0		ns
$\overline{RD}$ pulse width	t_{RR}		250		160		ns
$\overline{CS}$, A_0, to data out delay	t_{AD}	μPD8741A: C_L = 150 pF μPD8041AH: C_L = 100 pF		225		130	ns
$\overline{RD}$ ↓ to data out delay	t_{RD}	μPD8741A: C_L = 150 pF μPD8041AH: C_L = 100 pF		225		130	ns
$\overline{RD}$ ↑ to data float delay	t_{DF}			100		85	
Cycle time	t_{CY}		2.5	15	1.36	15	ns

DBB WRITE

PARAMETER	SYMBOL	TEST CONDITIONS	μPD8741A		μPD8041AH		UNIT
			MIN	MAX	MIN	MAX	
$\overline{CS}$, A_0 setup to $\overline{WR}$ ↓	t_{AW}		0		0		ns
$\overline{CS}$, A_0 hold after $\overline{WR}$ ↑	t_{WA}		0		0		ns
$\overline{WR}$ pulse width	t_{WW}		250		160		ns
Data setup to $\overline{WR}$ ↑	t_{DW}		150		130		ns
Data hold after $\overline{WR}$ ↑	t_{WD}		0		0		ns

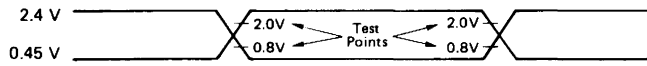
PORT 2

PARAMETER	SYMBOL	TEST CONDITIONS	μPD8741A		μPD8041AH		UNIT
			MIN	MAX	MIN	MAX	
Port control setup to PROG ↓	t_{CP}	μPD8041AH: C_L = 80 pF	110		100		ns
Port control hold after PROG ↓	t_{PC}	μPD8041AH: C_L = 20 pF	100		60		ns
Input data setup to PROG ↓	t_{PR}	μPD8041AH: C_L = 80 pF		810		650	ns
Input data hold time	t_{PF}	μPD8041AH: C_L = 20 pF	0	150	0	150	ns
Output data setup time	t_{DP}	μPD8041AH: C_L = 80 pF	250		200		ns
Output data hold time	t_{PD}	μPD8041AH: C_L = 20 pF	65		65		ns
PROG pulse with	t_{PP}		1200		700		ns

DMA

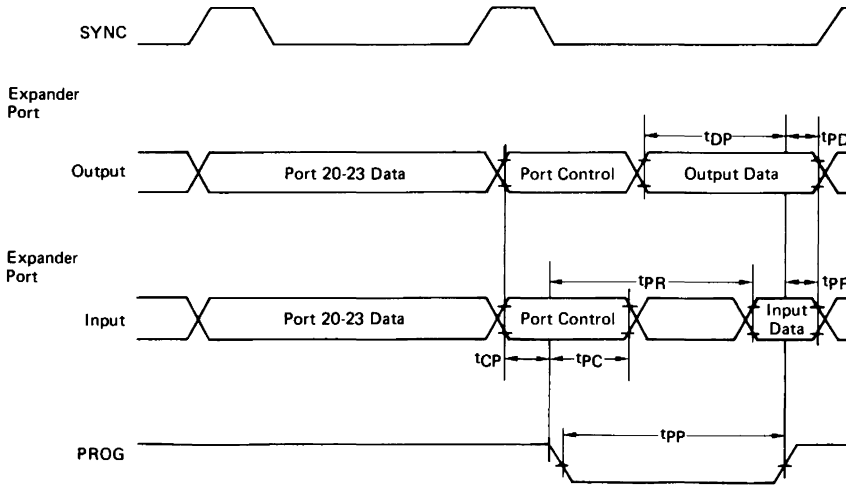
PARAMETER	SYMBOL	TEST CONDITIONS	μPD8741A		μPD8041AH		UNIT
			MIN	MAX	MIN	MAX	
$\overline{DACK}$ setup time to $\overline{RD}$, $\overline{WR}$	t_{ACC}		0		0		ns
$\overline{DACK}$ hold time after $\overline{RD}$, $\overline{WR}$	t_{CAC}		0		0		ns
Data output delay after $\overline{DACK}$	t_{ACD}	μPD8741A: C_L = 150 pF		225		130	ns
DRQ clear delay time after $\overline{RD}$, $\overline{WR}$	t_{CRQ}	μPD8041AH: C_L = 100 pF		200		130	ns

AC TIMING TEST POINTS

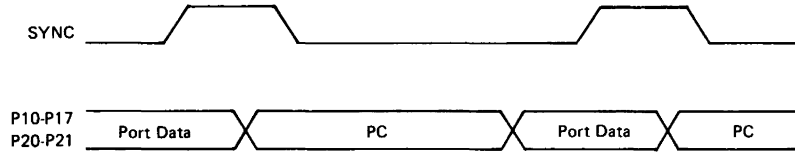


TIMING WAVEFORMS

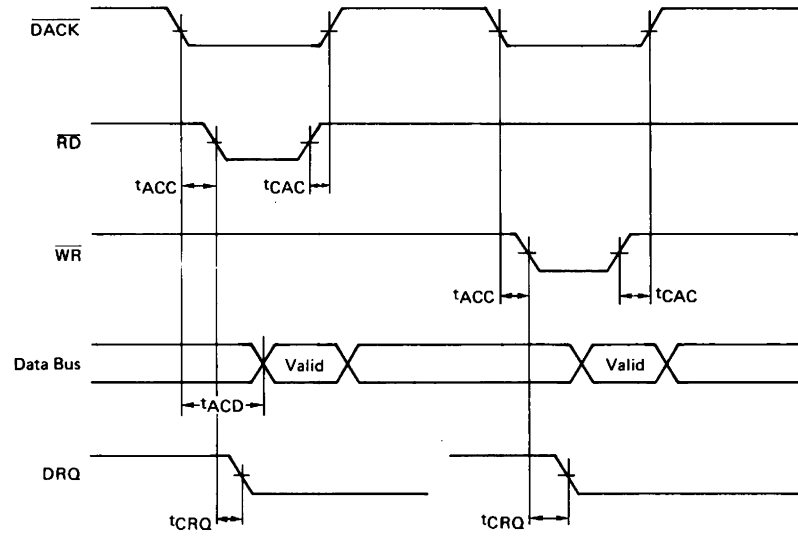
PORT 2



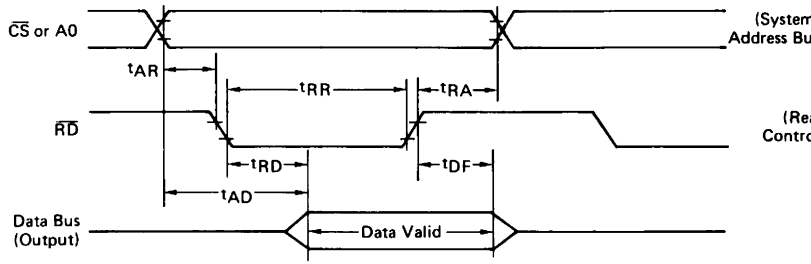
PORT (EA = 1)



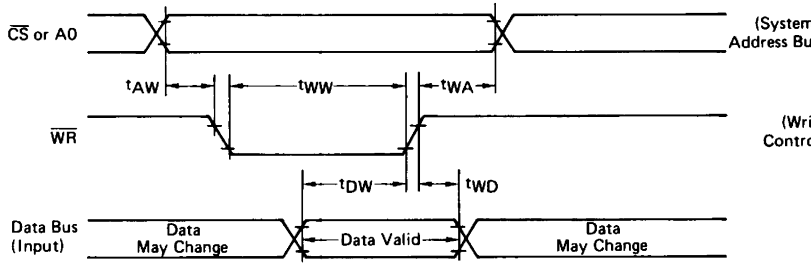
DMA



READ OPERATION (DBBOUT REGISTER)



WRITE OPERATION (DBBIN REGISTER)



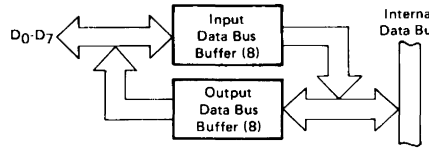
FUNCTIONAL DESCRIPTION

Two data bus buffers, an 8-bit status register, the $\overline{RD}$ and $\overline{WR}$ inputs, and expandable I/O lines enhance the μPD8041AH/8741A. These features enable easier master/slave interface and increased functionality.

DATA BUS BUFFERS

Figure 1 shows how the input and output data bus buffers enable a smooth data flow to and from the master processors.

Figure 1. Data Bus Buffers



STATUS REGISTER

The 8-bit status register includes four user-definable bits, ST_4–ST_7. Use the MOV STS, A instruction (90H) to define bits ST_4–ST_7 by moving accumulator bits 4–7 to bits 4–7 of the status register. Bits ST_0–ST_3 are not affected.

Figure 2 shows the format of the status register.

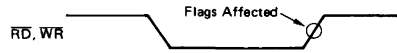
Figure 2. Status register Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
ST_7	ST_6	ST_5	ST_4	F1	F0	IBF	OBF

$\overline{RD}$ AND $\overline{WR}$

The $\overline{RD}$ and $\overline{WR}$ inputs are edge-sensitive. Figure 3 shows that status bits $\overline{IFB}$, OBF, F1, and F0 are affected on the trailing edge at $\overline{RD}$ or $\overline{WR}$.

Figure 3. $\overline{RD}$ and $\overline{WR}$ inputs



PORT 2_4–PORT 2_7

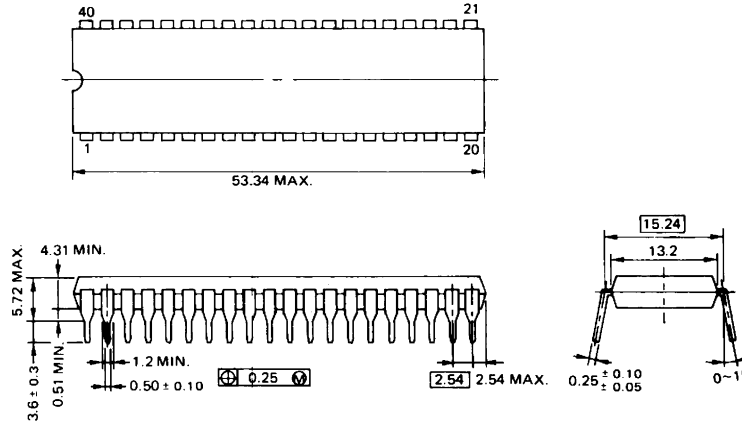
$P2_4$ and $P2_5$ can be used as either port lines or buffer status flag lines. This allows you to make OBF and $\overline{IBF}$ status available externally to interrupt the master processor. Upon execution of the EN FLAGS instruction (F5H), $P2_4$ becomes the OBF pin. When a 1 is written to $P2_4$, the OBF pin is enabled and the status of OBF is output. A0 to $P2_4$ disables the OBF pin AND the pin remains low. This pin indicates valid data is available from the μPD8041AH/8741A.

An EN FLAGS instruction execution also enables $P2_5$ to indicate that the μPD8041AH/8741A is ready to accept data. A1 written to $P2_5$ enables the $\overline{IBF}$ pin and the status of $\overline{IBF}$ is available on $P2_5$. A0 written to $P2_5$ disables the $\overline{IBF}$ pin. If OBF is not true, the data at the data bus is invalid.

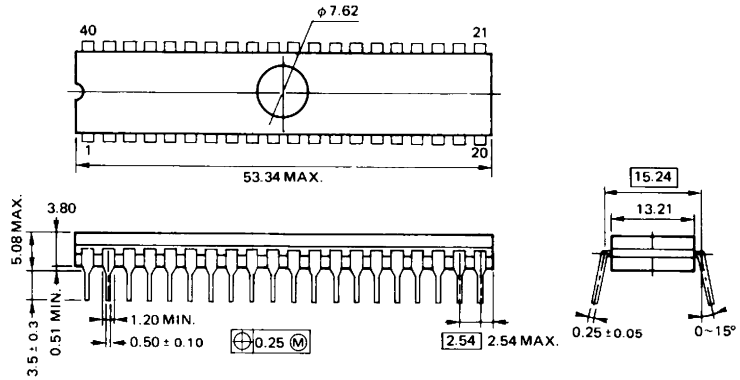
$P2_6$ and $P2_7$ can be used as either port lines or DMA handshake lines to allow DMA interface. The EN DMA instruction (E5H) enables $P2_6$ and $P2_7$ to be used as DRQ (DMA request) and $\overline{DACK}$ (DMA acknowledge), respectively.

When a 1 is written to $P2_6$, DRQ is activated and a DMA request is issued. The EN DMA instruction deactivates DRQ. You can also deactivate DRQ by adding $\overline{DACK}$ with $\overline{RD}$ or $\overline{WR}$. Execution of the EN DMA instruction enables $P2_7$ ($\overline{DACK}$) to function as a chip select input for the data bus buffer registers during DMA transfers.

40-PIN PLASTIC DIP PACKAGE
OUTLINE (Unit : mm)
μPD8041AHC–XXX



40-PIN CERAMIC DIP PACKAGE
OUTLINE (Unit : mm)
μPD8741AD



HIGH-SPEED, 8-BIT, SINGLE-CHIP HMOS MICROCOMPUTERS

DESCRIPTION

The μPD8035HL and the μPD8048H make up the μPD8048H family of single-chip 8-bit microcomputers. The processors in this family differ only in their internal program memory options: the μPD8048H with 1K x 8 bytes of mask ROM and the μPD8035HL with external memory.

The NEC μPD8035HL and μPD8048H are single component, 8-bit, parallel microprocessors using n-channel silicon gate MOS technology. The μPD8048H family of components functions efficiently in control as well as in arithmetic applications. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The μPD8035HL/48H instruction set comprises 1 and 2 byte instructions with over 70 % of them single-byte. Execution requires only 1 or 2 cycles per instruction and over 50 % are single-cycle instructions.

The functions of the μPD8048H series of microprocessors can easily be expanded using standard 8080A/8085A peripherals and memories.

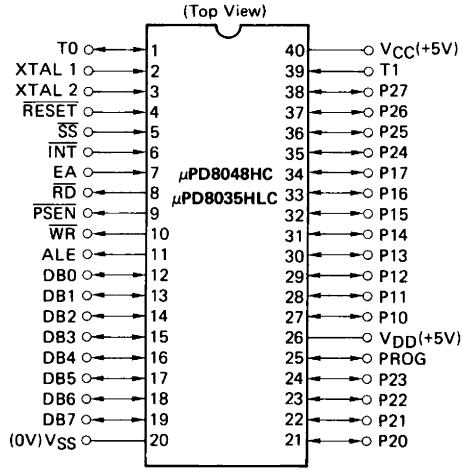
The μPD8048H contains the following functions usually found in external peripheral devices: 1024 x 8 bits of ROM program memory; 64 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

The μPD8035HL is intended for applications using external program memory only. It contains all the features of the μPD8048H except the 1024 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

FEATURES

- Fully compatible with industry standard 8048/8748/8035
- 2.5 μs cycle time: all instructions 1 or 2 bytes
- Interval timer/event counter
- 64 x 8-byte RAM data memory
- External and timer interrupts
- 96 instructions: 70 % single byte
- 27 I/O lines
- Internal clock generator
- 8 level stack
- Compatible with 8080A/8085A peripherals
- HMOS silicon gate technology
- Single +5V power supply

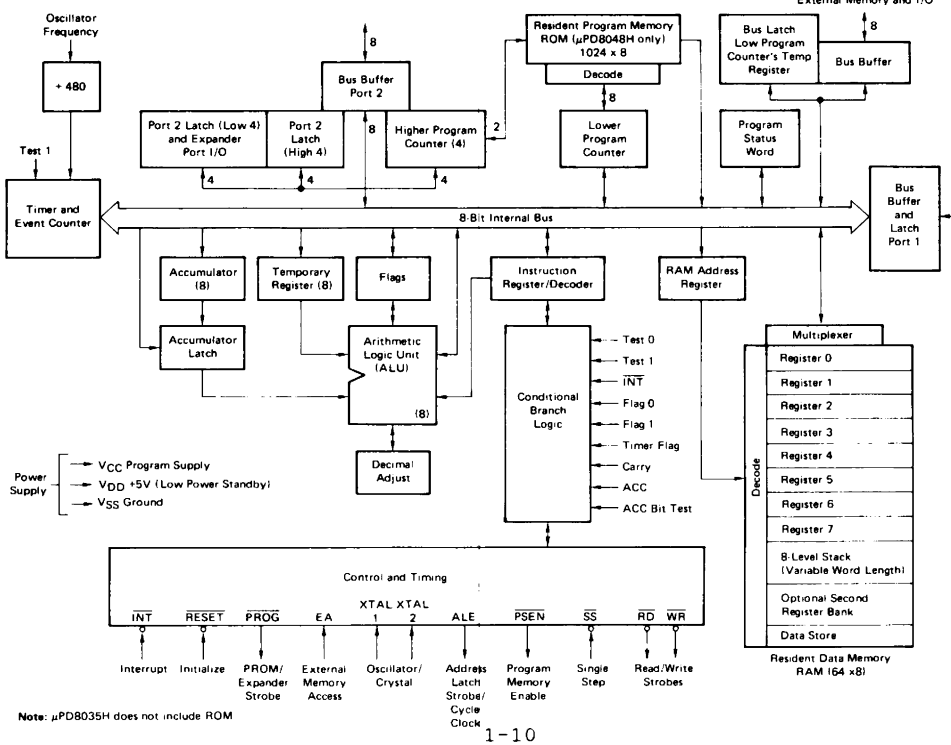
PIN CONFIGURATION



PIN IDENTIFICATION

NO.	SYMBOL	FUNCTION
1	T0	Test 0 input/output
2	XTAL1	Crystal 1 input
3	XTAL2	Crystal 2 input
4	$\overline{\text{RESET}}$	Reset input
5	$\overline{\text{SS}}$	Single step input
6	$\overline{\text{INT}}$	Interrupt input
7	EA	External access input
8	$\overline{\text{RD}}$	Read output
9	$\overline{\text{PSEN}}$	Program store enable output
10	$\overline{\text{WR}}$	Write output
11	ALE	Address latch enable output
12–19	DB_0–DB_7	Bidirectional data bus
20	V_{SS}	Ground
21–24, 35–38	$P2_0$–$P2_7$	Quasi-bidirectional Port 2
25	$\overline{\text{PROG}}$	Program output
26	V_{DD}	RAM power supply
27–34	$P1_0$–$P1_7$	Quasi-bidirectional Port 1
39	T1	Test 1 input
40	V_{CC}	Primary power supply

BLOCK DIAGRAM



Note: μPD8035H does not include ROM

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin, $V_{I/O}$	−0.5V to +7V (Note 1)
Power dissipation, P_D	1.5W

Note:

(1) With respect to ground.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input low voltage (All except XTAL1, XTAL2)	V_{IL}		−0.5		0.8	V
Input low voltage ($\overline{RESET}$, X1, X2)	V_{IL1}		−0.5		0.8	V
Input high voltage (All except XTAL1, XTAL2, $\overline{RESET}$)	V_{IH}		2.0		V_{CC}	V
Input high voltage (XTAL1, XTAL2, $\overline{RESET}$)	V_{IH1}		3.8		V_{CC}	V
Output low voltage (Bus)	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output low voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
Output low voltage ($\overline{PROG}$)	V_{OL2}	I_{OL} = 2.0 mA			0.45	V
Output low voltage (all other outputs)	V_{OL3}	I_{OL} = 2.0 mA			0.45	V
Output high voltage (Bus)	V_{OH}	I_{OH} = −400 μA	2.4			V
Output high voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH1}	I_{OH} = −400 μA	2.4			V
Output high voltage (all other outputs)	V_{OH2}	I_{OH} = −40 μA	2.4			V
Input leakage current (T1, $\overline{INT}$)	I_{LI}	$V_{SS} \leq V_{IN} \leq V_{CC}$			± 10	μA
Input leakage current ($P1_0$–$P1_7$, $P2_0$–$P2_7$, EA, $\overline{SS}$)	I_{LI1}	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V			−500	μA
Output leakage current (Bus T0, high impedance state)	I_{OL}	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V			± 10	μA
Power down supply current	I_{DD}	T_A = 25°C		4	8	mA
Total supply current	I_{DD} + I_{CC}	T_A = 25°C		50	80	mA
RAM standby voltage	V_{DD}	Standby mode. Reset ≤ 0.6V	2.2		5.5	V

AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cycle time	t_{CY}	(Note 1)	2.5		15	μs
ALE pulse width	t_{LL}	(Note 1)	410			ns
Address setup to ALE	t_{AL}	(Note 1)	220			ns
Address hold from ALE	t_{LA}	(Note 1)	120			ns
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	(Note 1)	1050			ns
Control pulse width ($\overline{PSEN}$)	t_{CC2}	(Note 1)	800			ns
Data setup $\overline{WR}$	t_{DW}	(Note 1)	880			ns
Data hold after $\overline{WR}$	t_{WD}	(Note 2)	110			ns
Data hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	(Note 1)	0		220	ns
$\overline{RD}$ to data in	t_{RD1}	(Note 1)			800	ns
$\overline{PSEN}$ to data in	t_{RD2}	(Note 1)			550	ns
Address setup to $\overline{WR}$	t_{AW}	(Note 1)	680			ns
Address setup to data ($\overline{RD}$)	t_{AD1}	(Note 1)			1570	ns
Address setup to data ($\overline{PSEN}$)	t_{AD2}	(Note 1)			1090	ns
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	(Note 1)	290			ns
Address float to $\overline{PSEN}$	t_{AFC2}	(Note 1)	40			ns
ALE to control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	(Note 1)	420			ns
ALE to control ($\overline{PSEN}$)	t_{LAFC2}	(Note 1)	170			ns
Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t_{CA1}	(Note 1)	120			ns
Control to ALE ($\overline{PSEN}$)	t_{CA2}	(Note 1)	620			ns
Port control setup to $\overline{PROG}$	t_{CP}	(Note 1)	210			ns
Port control hold to $\overline{PROG}$	t_{PC}	(Note 1)	460			ns
$\overline{PROG}$ to P2 input valid	t_{PR}	(Note 1)			1300	ns
Input data hold from $\overline{PROG}$	t_{PF}	(Note 1)			250	ns
Output data setup	t_{DP}	(Note 1)	850			ns
Output data hold	t_{PD}	(Note 1)	200			ns
$\overline{PROG}$ pulse width	t_{PP}	(Note 1)	1500			ns
Port 2 I/O data setup to ALE	t_{PL}	(Note 1)	460			ns
Port 2 I/O data hold to ALE	t_{LP}	(Note 1)	150			ns
Port output from ALE	t_{PV}	(Note 1)			850	ns
T0 rep rate	t_{OPRR}	(Note 1)	500			ns

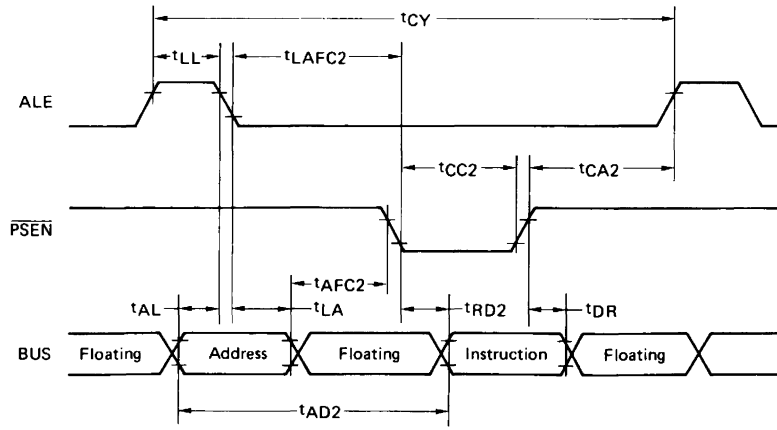
Note:

(1) Control outputs: C_L = 80 pF, bus outputs: C_L = 150 pF

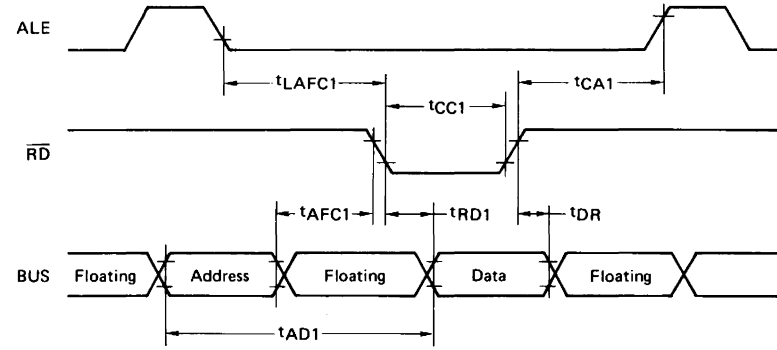
(2) Bus high impedance, load = 20 pF

TIMING WAVEFORMS

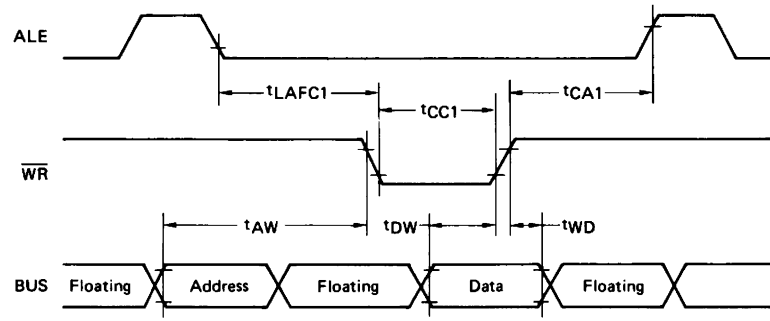
INSTRUCTION FETCH FROM EXTERNAL MEMORY



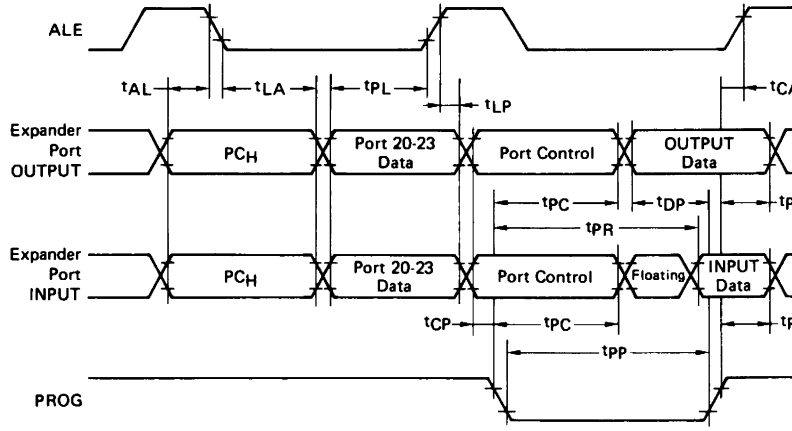
READ FROM EXTERNAL DATA MEMORY



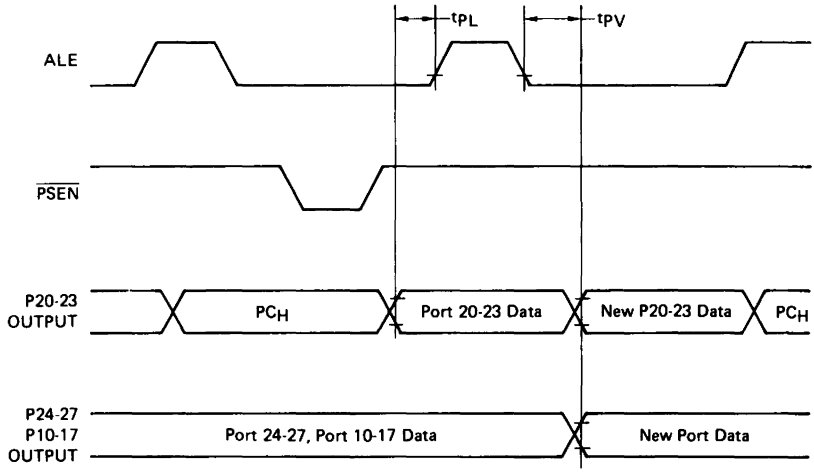
WRITE TO EXTERNAL MEMORY



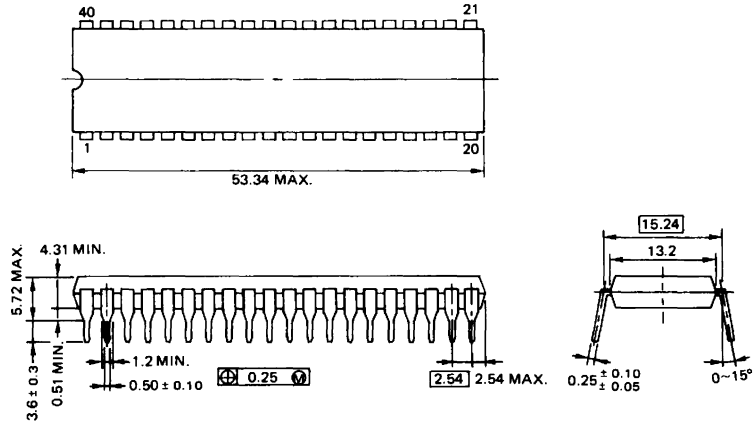
PORT 2 TIMING



I/O PORT TIMING



40-PIN PLASTIC DIP PACKAGE
OUTLINE (UNIT : mm)
μPD8035HLC
μPD8048HC –XXX



HIGH-SPEED, 8-BIT, SINGLE-CHIP NMOS MICROCOMPUTER WITH UV EPROM

DESCRIPTION

The μPD8748H is one of the μPD8048 family of single-chip 8-bit microcomputers. It is a high-speed NMOS processor that functions efficiently in control and arithmetic applications. The flexible instruction set allows you to directly set and reset individual data bits within the accumulator and the I/O ports. The variety of branch and table look-up instructions simplifies the implementation of standard logic functions.

The instruction set is made up of one- and two-byte instructions. Over 70 % are single-byte instructions that require only one or two cycles. Over 50 % require a single cycle.

The μPD8048H functions as a stand-alone microcomputer. You can expand its functions with standard 8080A/8085A peripherals and memories. It contains 1024 x 8 bits of ROM program memory, 64 x 8 bits of RAM data memory, 27 I/O lines, an 8-bit internal timer/event counter, oscillator, and clock circuitry.

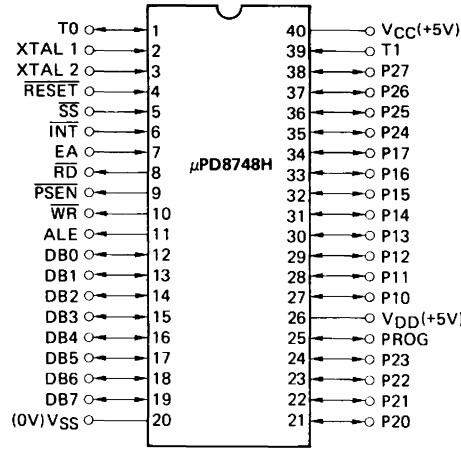
The μPD8748H differs from the μPD8048 in that it has 1K of on-board EPROM. This is useful in preproduction or prototype applications where the software is not complete or in system designs in quantities that do not require a mask ROM. See the μPD8048H/8035HL data sheet for more information.

FEATURES

- Low programming voltage
- Fully compatible with 8048/8748/8035
- NMOS silicon gate technology
- Single +5V supply
- 2.5μs cycle time
- 96 instructions; 70 % single byte
- Internal timer/event counter
- 64 x 8 byte RAM data memory
- Single interrupt level
- 27 I/O lines
- Internal clock generator
- 8-level stack
- Compatible with 8080A/8085A peripherals
- Available in one-time-programmable plastic package

PIN CONFIGURATION

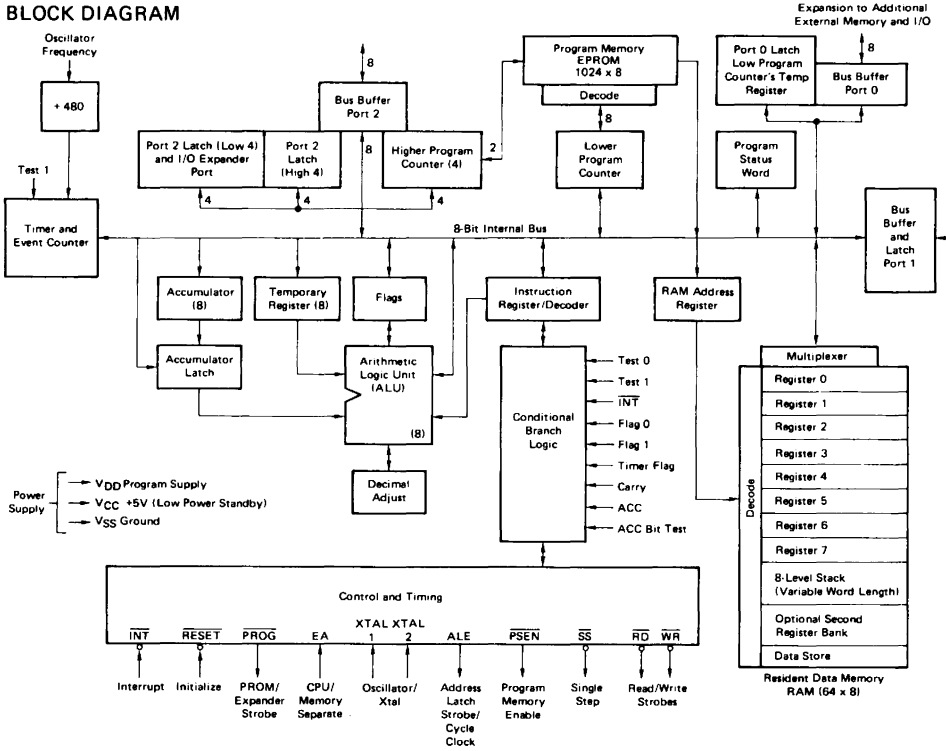
(Top View)



PIN IDENTIFICATION

NO.	SYMBOL	FUNCTION
1, 39	T0, T1	Testable inputs 0 and 1
2, 3	XTAL1, XTAL2	Crystal inputs
4	$\overline{\text{RESET}}$	System reset input
5	$\overline{\text{SS}}$	Single step input
6	$\overline{\text{INT}}$	Interrupt input
7	EA	External access input
8	$\overline{\text{RD}}$	Read strobe output
9	$\overline{\text{PSEN}}$	Program store enable output
10	$\overline{\text{WR}}$	Write strobe output
11	ALE	Address latch enable output
12–19	D_0–D_7	8-bit bidirectional port
20	V_{SS}	Ground
21–24, 35–38	$P2_0$–$P2_7$	8-bit quasibidirectional port 2
25	PROG	Program pulse input
26	V_{DD}	Programming power supply
27–34	$P1_0$–$P1_7$	8-bit quasibidirectional port 1
40	V_{CC}	Primary power supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

Operating temperature, T_{OP}	0°C to +70°C
Storage temperature, T_{ST}	−65°C to +150°C
Output voltage, V_O	−0.5V to +7.0V
Input voltage, V_I	−0.5V to +7.0V
Power supply voltages, V_{CC}, V_{DD}	−0.5V to +7.0V

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input low voltage (except XTAL1, XTAL2, $\overline{\text{RESET}}$)	V_{IL}		−0.5		0.8	V
Input low voltage (XTAL1, XTAL2, $\overline{\text{RESET}}$)	V_{IL1}		−0.5		0.6	V
Input high voltage (except XTAL1, XTAL2, $\overline{\text{RESET}}$)	V_{IH}		2.0		V_{CC}	V
Input high voltage (XTAL1, XTAL2, $\overline{\text{RESET}}$)	V_{IH1}		3.8		V_{CC}	V
Output low voltage (Bus)	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output low voltage ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE)	V_{OL1}	I_{OL} = 1.8 mA			0.45	V
Output low voltage (PROG)	V_{OL2}	I_{OL} = 1.0 mA			0.45	V
Output low voltage (all other outputs)	V_{OL3}	I_{OL} = 1.6 mA			0.45	V
Output high voltage (Bus)	V_{OH}	I_{OH} = −400 μA	2.4			V
Output high voltage ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE)	V_{OH1}	I_{OH} = −100 μA	2.4			V
Output high voltage (all other outputs)	V_{OH2}	I_{OH} = −40 μA	2.4			V
Input leakage current (T1, $\overline{\text{INT}}$)	I_{LI}	$V_{SS} \leq V_I \leq V_{CC}$			± 10	μA
Input leakage current ($P1_0$–$P1_7$, $P2_0$–$P2_7$, EA, $\overline{\text{SS}}$)	I_{LI1}	V_{SS} +0.45V ≤ $V_I \leq V_{CC}$			−500	μA
Output leakage current (Bus, T0, high impedance)	I_{LO}	V_{SS} +0.45V ≤ $V_I \leq V_{CC}$			± 10	μA
Supply current (V_{DD})	I_{DD}			2	5	mA
Total supply current	$I_{DD} + I_{CC}$			85	110	mA

PROGRAMMING DC CHARACTERISTICS

T_A = 25°C ± 5°C, V_{CC} = +5V ± 5 %, V_{DD} = +21V ± 0.5V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} voltage high level	V_{DDH}		20.5		21.5	V
V_{DD} voltage low level	V_{DDL}		4.75		5.25	V
PROG voltage high level	V_{PH}		17.5		18.5	V
PROG voltage low level	V_{PL}		4.0		V_{CC}	V
EA program/verify voltage high level	V_{EAH}		17.5		18.5	V
V_{DD} high voltage supply current	I_{DD}				20.0	mA
PROG high voltage supply current	I_{PROG}				1.0	mA
EA high voltage supply current	I_{EA}				1.0	mA

AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cycle time	t_{CY}		1.36		15.0	μs
ALE pulse width	t_{LL}	(1, 3)	150			ns
Address setup before ALE	t_{AL}	(1, 3)	70			ns
Address hold after ALE	t_{LA}	(1, 3)	50			ns
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	(1, 3)	480			ns
Control pulse width ($\overline{PSEN}$)	t_{CC2}	(1, 3)	350			ns
Data setup before $\overline{WR}$	t_{DW}	(1, 3)	390			ns
Data hold after $\overline{WR}$	t_{WD}	(1, 2, 3)	40			ns
Data hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}	(1, 3)	0		110	ns
$\overline{RD}$ to data in	t_{RD1}	(1, 3)			330	ns
$\overline{PSEN}$ to data in	t_{RD2}	(1, 3)			190	ns
Address setup before $\overline{WR}$	t_{AW}	(1, 3)	300			ns
Address setup before data in ($\overline{RD}$)	t_{AD1}	(1, 3)			730	ns
Address setup before data in ($\overline{PSEN}$)	t_{AD2}	(1, 3)			460	ns
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	(1, 3)	140			ns
Address float to $\overline{PSEN}$	t_{AFC2}	(1, 3)	10			ns
ALE to $\overline{RD}$, $\overline{WR}$ delay time	t_{LAFC1}	(1, 3)	200			ns
ALE to $\overline{PSEN}$ delay time	t_{LAFC2}	(1, 3)	60			ns
$\overline{RD}$, $\overline{WR}$, PROG to ALE delay time	t_{CA1}	(1, 3)	50			ns
$\overline{PSEN}$ to ALE delay time	t_{CA2}	(1, 3)	320			ns
Port 2 Timing						
Port control setup before PROG	t_{CP}	(1, 3)	100			ns
Port control hold after PROG	t_{PC}	(1, 3)	160			ns
Input data setup before PROG	t_{PR}	(1, 3)			650	ns
Input data hold after PROG	t_{PF}	(1, 3)	0		140	ns
Output data setup before PROG	t_{DP}	(1, 3)	400			ns
Output data hold after PROG	t_{PD}	(1, 3)	90			ns
PROG pulse width	t_{PP}	(1, 3)	700			ns
Port 2 I/O data setup before ALE	t_{PL}	(1, 3)	160			ns
Port 2 I/O data setup after ALE	t_{LP}	(1, 3)	15			ns
ALE to port output time	t_{PV}	(1, 3)			510	ns
T0 output cycle time	t_{OPRR}	(1, 3)	270			ns

Note:

(1) Control Output: C_L = 80 pF, Bus Output: C_L = 150 pF

(2) Bus high impedance, load = 20 pF

(3) Clock oscillation frequency, f_{OSC} = 11 MHz

PROGRAMMING AC CHARACTERISTICS

T_A = 25°C ± 5°C, V_{DD} = +21V ± 0.5V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Address setup before $\overline{RESET}$ ↑	t_{AW}		4 t_{CY}			
Address hold after $\overline{RESET}$ ↑	t_{WA}		4 t_{CY}			
Data input setup before PROG ↓	t_{DW}		4 t_{CY}			
Data input hold after PROG ↓	t_{WD}		4 t_{CY}			
$\overline{RESET}$ hold after verify	t_{PH}		4 t_{CY}			
V_{DD} setup before PROG ↑	t_{VDDW}		0		1.0	ms
V_{DD} hold after PROG ↓	t_{VDDH}		0		1.0	ms
PROG pulse width	t_{PW}		50		60	ms
TEST 0 setup before program mode	t_{TW}		4 t_{CY}			
TEST 0 hold after program mode	t_{WT}		4 t_{CY}			
TEST 0 to data output delay (1)	t_{DO}				4 t_{CY}	
$\overline{RESET}$ pulse width to latch address	t_{WW}		4 t_{CY}			
V_{DD} and PROG rise and fall times	t_r, t_f		0.5		100	μs
CPU cycle time	t_{CY}	4.0 μs/3.7 MHz	4.0		15	μs
$\overline{RESET}$ setup before EA ↑	t_{RE}		4 t_{CY}			

Note:

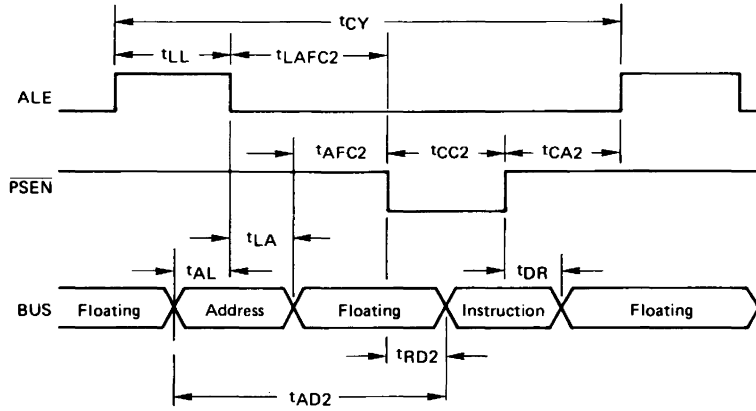
(1) If TEST 0 is high, t_{DO} is triggered by RESET ↑.

BUS TIMING REQUIREMENTS

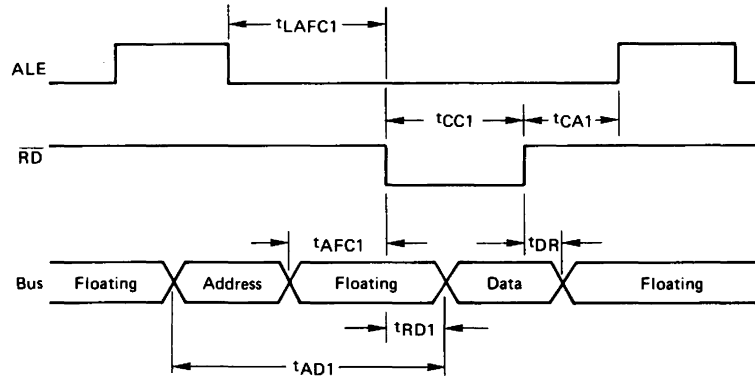
SYMBOL	TIMING FORMULA	MIN/MAX	UNIT
t_{LL}	(7/30) t_{CY} −170	MIN	ns
t_{AL}	(2/15) t_{CY} −110	MIN	ns
t_{LA}	(1/15) t_{CY} − 40	MIN	ns
t_{CC1}	(1/ 2) t_{CY} −200	MIN	ns
t_{CC2}	(2/ 5) t_{CY} −200	MIN	ns
t_{DW}	(13/30) t_{CY} −200	MIN	ns
t_{WD}	(1/15) t_{CY} − 50	MIN	ns
t_{DR}	(1/10) t_{CY} − 30	MAX	ns
t_{RD1}	(11/13) t_{CY} −170	MAX	ns
t_{RD2}	(4/15) t_{CY} −170	MAX	ns
t_{AW}	(1/ 3) t_{CY} −150	MIN	ns
t_{AD1}	(7/10) t_{CY} −220	MAX	ns
t_{AD2}	(1/ 2) t_{CY} −220	MAX	ns
t_{AFC1}	(2/15) t_{CY} − 40	MIN	ns
t_{AFC2}	(1/30) t_{CY} − 40	MIN	ns
t_{LAFC1}	(1/ 5) t_{CY} − 75	MIN	ns
t_{LAFC2}	(1/10) t_{CY} − 75	MIN	ns
t_{CA1}	(1/15) t_{CY} − 40	MIN	ns
t_{CA2}	(4/15) t_{CY} − 40	MIN	ns
t_{CP}	(2/15) t_{CY} − 80	MIN	ns
t_{PC}	(4/15) t_{CY} −200	MIN	ns
t_{PR}	(17/30) t_{CY} −120	MAX	ns
t_{PF}	(1/10) t_{CY}	MAX	ns
t_{DP}	(2/ 5) t_{CY} −150	MIN	ns
t_{PD}	(1/10) t_{CY} − 50	MIN	ns
t_{PP}	(7/10) t_{CY} −250	MIN	ns
t_{PL}	(4/15) t_{CY} −200	MIN	ns
t_{LP}	(1/30) t_{CY} − 30	MIN	ns
t_{PV}	(3/10) t_{CY} + 100	MAX	ns
t_{OPRR}	(1/ 5) t_{CY}	MIN	ns
t_{CY}	(1/f_{OSC}) x 15		μs

TIMING WAVEFORMS

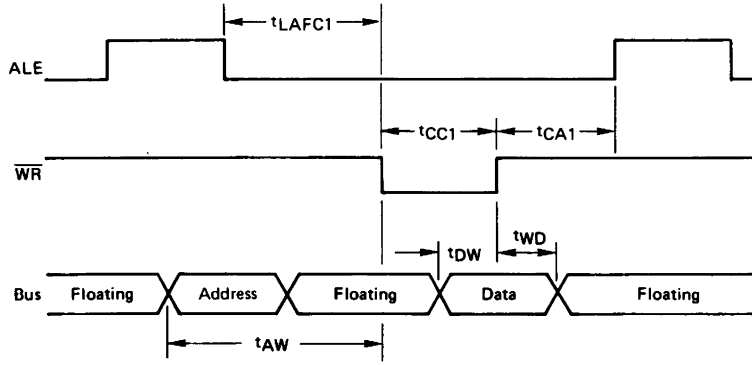
INSTRUCTION FETCH (EXTERNAL PROGRAM MEMORY)



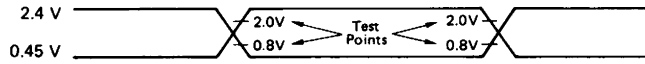
READ (EXTERNAL DATA MEMORY)



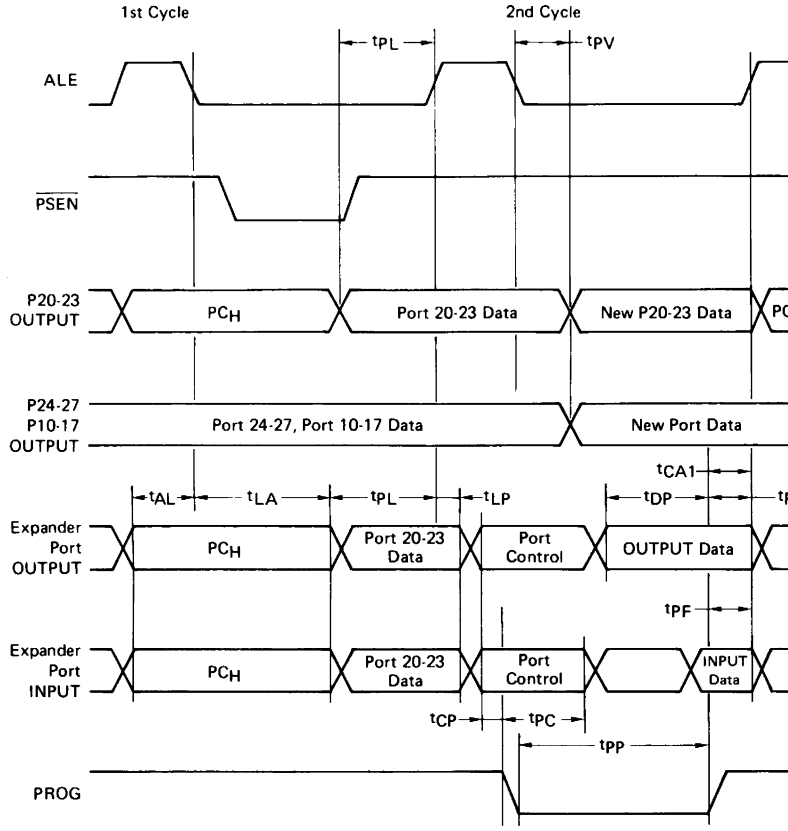
WRITE (EXTERNAL DATA MEMORY)



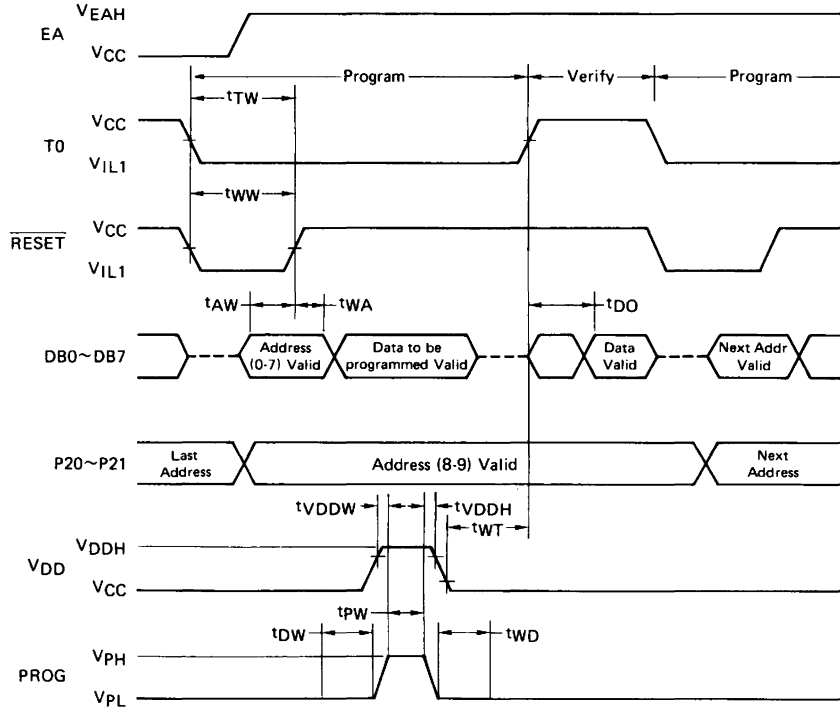
AC TIMING TEST POINTS



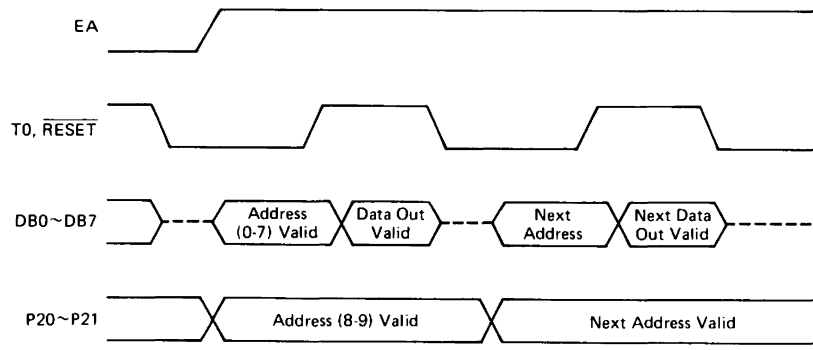
PORT 1/PORT 2


1st Cycle
2nd Cycle
tPL
tPV
ALE
PSEN
P20-23 OUTPUT
PCH
Port 20-23 Data
New P20-23 Data
PCH
P24-27 P10-17 OUTPUT
Port 24-27, Port 10-17 Data
New Port Data
tCA1
tAL
tLA
tPL
tLP
tDP
tPD
Expander Port OUTPUT
PCH
Port 20-23 Data
Port Control
OUTPUT Data
tPF
Expander Port INPUT
PCH
Port 20-23 Data
Port Control
INPUT Data
tCP
tPC
tPP
PROG

PROGRAM/VERIFY



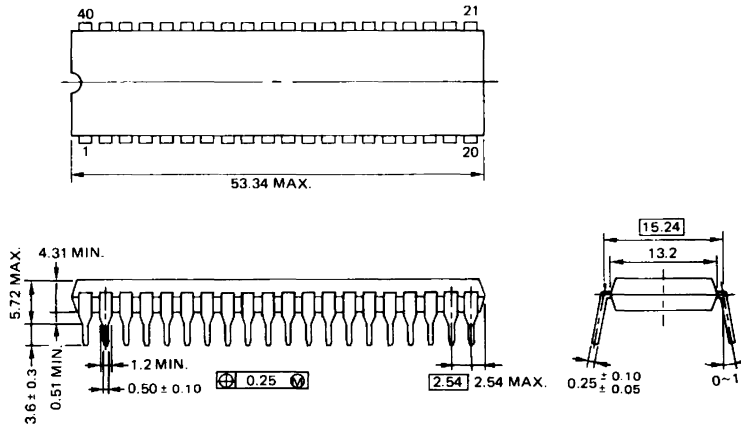
VERIFY



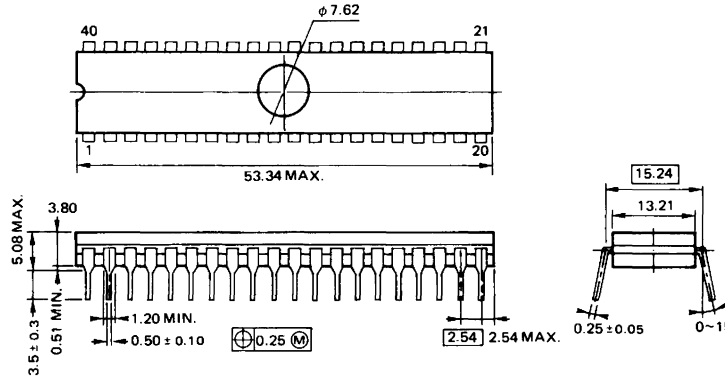
Note:

1. When EA is „low" or T0 = 5V, PROG should be in floating condition (≠ 18V).
2. t_{CY} 4 μs can be achieved using 3.7 MHz frequency at the XTAL1 and XTAL2.

40-PIN PLASTIC DIP PACKAGE
OUTLINE (UNIT : mm)
μPD8748HC



40-PIN CERAMIC DIP PACKAGE
OUTLINE (UNIT : mm)
μPD8748HD



HIGH-SPEED, 8-BIT, SINGLE-CHIP HMOS MICROCOMPUTERS

DESCRIPTION

The NEC μPD8039HL, μPD8049H and the μPD8749H are high performance, single component, 8-bit parallel microcomputers using n-channel silicon gate MOS technology. The processors differ only in their internal program memory options: the μPD8049H has 2K x 8 bytes of mask ROM, the μPD8749H has 2K x 8 of UV erasable EPROM and the μPD8039HL has external program memory.

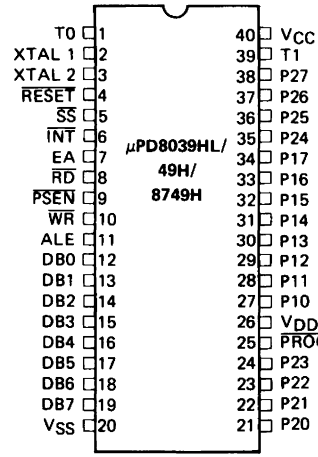
The μPD8049H family functions efficiently in control as well as arithmetic applications. The powerful instruction set eases bit handling applications and provides facilities for binary and BCD arithmetic. Standard logic functions implementation is facilitated by the large variety of branch and table look-up instructions. The instruction set is comprised of 1 and 2 byte instructions, most of which are single-byte. The instruction set requires only 1 or 2 cycles per instruction with over 50 percent of the instructions single-cycle.

The μPD8049H family of microprocessors will function as stand-alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories. The μPD8039HL is intended for applications using external program memory only. It contains all the features of the μPD8049H except for the internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products. The μPD8049H contains the following functions usually found in external peripheral devices: 2048 x 8 bits of mask ROM program memory; 128 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; and oscillator and clock circuitry. The μPD8749H differs from the μPD8049H in its 2048 x 8-bit UV erasable EPROM program memory instead of the mask ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

FEATURES

- High performance 11 MHz operation
- Fully compatible with industry standard 8039/8049/8749
- Pin compatible with the μPD8048/8748
- 1.36 μs cycle time. All instructions 1 or 2 bytes
- Programmable interval timer/event counter
- 2K x 8 bytes of ROM/EPROM, 128 x 8 bytes of RAM
- External and internal interrupts
- 96 instructions: 70 percent single byte
- 27 I/O lines
- Internal clock generator
- Expandable with 8080A/8085A peripherals
- HMOS silicon gate technology
- Single +5V power supply (8039HL/49H)

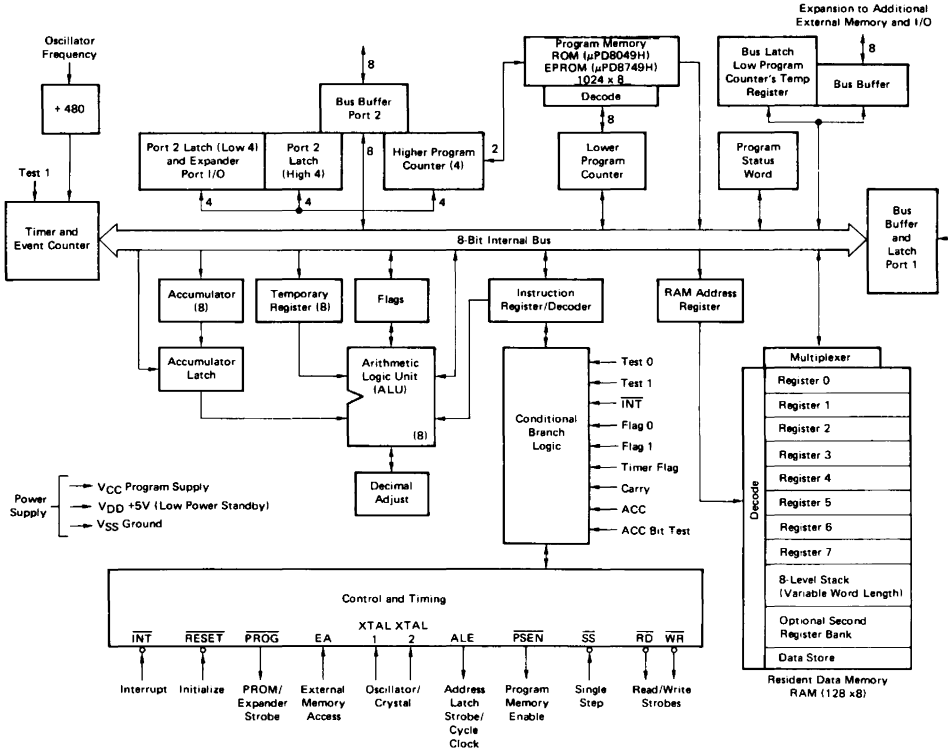
PIN CONFIGURATION



PIN IDENTIFICATION

NO.	SYMBOL	FUNCTION
1	T0	Test 0 input/output
2	XTAL1	Crystal 1 input
3	XTAL2	Crystal 2 input
4	$\overline{\text{RESET}}$	Reset input
5	$\overline{\text{SS}}$	Single step input
6	$\overline{\text{INT}}$	Interrupt input
7	EA	External access input
8	$\overline{\text{RD}}$	Read output
9	$\overline{\text{PSEN}}$	Program store enable output
10	$\overline{\text{WR}}$	Write output
11	ALE	Address latch enable output
12–19	DB_0–DB_7	Bidirectional data bus
20	V_{SS}	Ground
21–24, 35–38	$P2_0$–$P2_7$	Quasi-bidirectional Port 2
25	PROG	Program output
26	V_{DD}	RAM power supply
27–34	$P1_0$–$P1_7$	Quasi-bidirectional Port 1
39	T1	Test 1 input
40	V_{CC}	Primary power supply

BLOCK DIAGRAM



Note: μPD8039HL does not include ROM.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin, $V_{I/O}$	−0.5V to +7.0V (Note 1)
Power dissipation, P_D	1.5W

Note:

(1) With respect to ground.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input low voltage (All except XTAL1, XTAL2, $\overline{RESET}$ for 8749H)	V_{IL}		−0.5		0.8	V
Input low voltage (XTAL1, XTAL2, $\overline{RESET}$)	V_{IL1}	8749H	−0.5		0.6	V
Input high voltage (All except XTAL1, XTAL2, $\overline{RESET}$	V_{IH}		2.0		V_{CC}	V
Input high voltage (XTAL1, XTAL2, $\overline{RESET}$)	V_{IH1}		3.8		V_{CC}	V
Output low voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL}	I_{OL} = 2.0 mA, *1			0.45	V
Output low voltage (All others except PROG)	V_{OL1}	I_{OL} = 2.0 mA, *2			0.45	V
Output low voltage (PROG)	V_{OL2}	I_{OL} = 2.0 mA, *3			0.45	V
Output high voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH}	I_{OH} = −400 μA, *4	2.4			V
Output high voltage (all other outputs)	V_{OH1}	I_{OH} = −40 μA	2.4			V
Input leakage current (T1, INT)	I_{LI}	$V_{SS} \leq V_{IN} \leq V_{CC}$			± 10	μA
Input leakage current ($P1_0$–$P1_7$, $P2_0$–$P2_7$, EA, $\overline{SS}$)	I_{LI1}	V_{SS} +0.45V ≤ $V_{IN} \leq V_{CC}$			−500	μA
Input leakage current ($\overline{RESET}$)	I_{LI2}	V_{SS} +0.45V ≤ $V_{IN} \leq V_{CC}$	−10		−50	μA
Output leakage current (BUS T0, high impedance state)	I_{LO}	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V			± 10	μA
Power down supply current	I_{DD}	T_A = 25°C		5	10	mA
		8749H only		2	5	
Total supply current	$I_{DD} + I_{CC}$	T_A = 25°C		80	110	mA
		8749H only		85	110	
Minimum voltage to maintain RAM contents	V_{DD}	Mins voltage $\overline{RESET} \leq$ 0.6V	2.2		5.5	V

Note:

*1 = for 8749H: I_{OL} = 1.8 mA for $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE;

*2 = for 8749H: I_{OL} = 1.6 mA;

*3 = for 8749H: I_{OL} = 1.0 mA;

*4 = for 8749H: I_{OH} = −100 μA for $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE;

DC PROGRAMMING CHARACTERISTICS

T_A = 25°C ± 5°C, V_{CC} = +5V ± 5 %, V_{DD} = +21V ± 0.5V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} program voltage high level	V_{DDH}		20.5		21.5	V
V_{DD} program voltage low level	V_{DDL}		4.75		5.25	V
PROG program voltage high level	V_{PH}		17.5		18.5	V
PROG voltage low level	V_{PL}		4.0		V_{CC}	V
EA program/verify voltage high level	V_{EAH}		17.5		18.5	V
V_{DD} high voltage supply current	I_{DD}				20.0	mA
PROG high voltage supply current	I_{PROG}				1.0	mA
EA high voltage supply current	I_{EA}				1.0	mA

AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cycle time	t_{CY}		1.36		15	μs
ALE pulse width	t_{LL}		150			ns
Address setup to ALE	t_{AL}		70			ns
Address hold from ALE	t_{LA}		50			ns
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}		480			ns
Control pulse width ($\overline{PSEN}$)	t_{CC2}		350			ns
Data setup before $\overline{WR}$	t_{DW}		390			ns
Data hold after $\overline{WR}$	t_{WD}	(Note 2)	40			ns
Data hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}		0		110	ns
$\overline{RD}$ to data in	t_{RD1}				*350/330	ns
$\overline{PSEN}$ to data in	t_{RD2}				*210/190	ns
Address setup to $\overline{WR}$	t_{AW}		300			ns
Address setup to data ($\overline{RD}$)	t_{AD1}				*750/720	ns
Address setup to data ($\overline{PSEN}$)	t_{AD2}				*490/460	ns
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}		140			ns
Address float to $\overline{PSEN}$	t_{AFC2}		10			ns
ALE to control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}		200			ns
ALE to control ($\overline{PSEN}$)	t_{LAFC2}		60			ns
Control to ALE ($\overline{RD}$, $\overline{WR}$, PROG)	t_{CA1}		50			ns
Control to ALE ($\overline{PSEN}$)	t_{CA2}		320			ns
Port control setup to $\overline{PROG}$	t_{CP}		100			ns
Port control hold to $\overline{PROG}$	t_{PC}		160			ns
$\overline{PROG}$ to P2 input valid	t_{PR}				650	ns
Input data hold from $\overline{PROG}$	t_{PF}		0		140	ns
Output data setup	t_{DP}		400			ns
Output data hold	t_{PD}		90			ns
$\overline{PROG}$ pulse width	t_{PP}		700			ns
Port 2 I/O data setup to ALE	t_{PL}		160			ns
Port 2 I/O data hold to ALE	t_{LP}		40			ns
Port output from ALE	t_{PV}				510	ns
I/O rep rate	t_{OPRR}		270			ns

Note:

(1) Control outputs: C_L = 80 pF, bus outputs: C_L = 150 pF

(2) Bus high impedance, load = 20 pF

(3) Double values are for 8039HL, 8049H/8749H respectively

AC PROGRAMMING CHARACTERISTICS

T_A = 25°C ± 5°C, V_{CC} = +5V ± 5 %, V_{DD} = +21V ± 0.5V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Address setup time to $\overline{RESET}$ ↑	t_{AW}		4 t_{CY}			
Address hold time after $\overline{RESET}$ ↑	t_{WA}		4 t_{CY}			
Data in setup time to PROG ↑	t_{DW}		4 t_{CY}			
Data in hold time after PROG ↓	t_{WD}		4 t_{CY}			
$\overline{RESET}$ hold time to verify	t_{PH}		4 t_{CY}			
V_{DD}	t_{VDDW}		0		1.0	ms
V_{DD} hold time after PROG ↓	t_{VDDH}		0		1.0	ms
PROG pulse width	t_{PW}		50		60	ms
TEST0 setup time for program mode	t_{TW}		4 t_{CY}			
TEST0 hold time after program mode	t_{WT}		4 t_{CY}			
TEST0 to data out delay (1)	t_{D0}				4 t_{CY}	
$\overline{RESET}$ pulse width to latch address	t_{WW}		4 t_{CY}			
V_{DD} and PROG rise and fall times	t_r, t_f		0.5		100	μs
CPU operation cycle time	t_{CY}	4.0 μs / 3.7 Mhz	4.0		15	μs
RESET setup time before EA ↑	t_{RE}		4 t_{CY}			

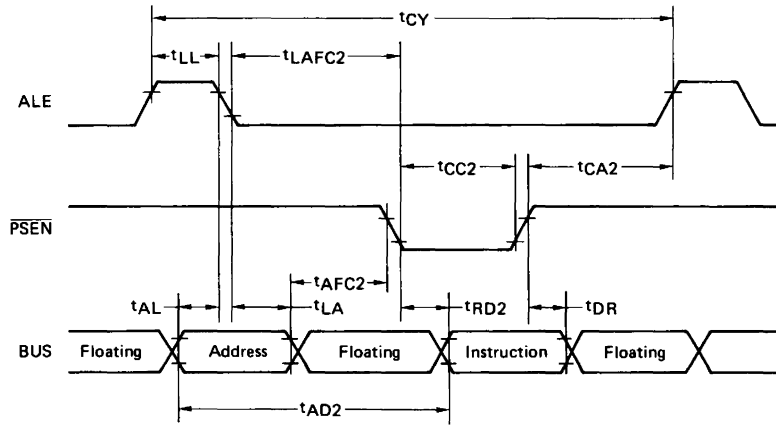
BUS TIMING REQUIREMENTS

SYMBOL	TIMING FORMULA	MIN/MAX	UNIT
t_{LL}	(7/30) t_{CY} −170	MIN	ns
t_{AL}	(2/15) t_{CY} −110	MIN	ns
t_{LA}	(1/15) t_{CY} − 40	MIN	ns
t_{CC1}	(1/ 2) t_{CY} −200	MIN	ns
t_{CC2}	(2/ 5) t_{CY} −200	MIN	ns
t_{DW}	(13/30) t_{CY} −200	MIN	ns
t_{WD}	(1/15) t_{CY} − 50	MIN	ns
t_{DR}	(1/10) t_{CY} − 30	MAX	ns
t_{RD1}	(2/ 5) t_{CY} −200 / (11/30) t_{CY} −170	MAX	ns
t_{RD2}	(3/10) t_{CY} −200 / (4/15) t_{CY} −170	MAX	ns
t_{AW}	(1/ 3) t_{CY} −150	MIN	ns
t_{AD1}	(11/15) t_{CY} −250 / (7/10) t_{CY} −220	MAX	ns
t_{AD2}	(8/15) t_{CY} −250 / (1/ 2) t_{CY} −220	MAX	ns
t_{AFC1}	(2/15) t_{CY} − 40	MIN	ns
t_{AFC2}	(1/30) t_{CY} − 40	MIN	ns
t_{LAFC1}	(1/ 5) t_{CY} − 75	MIN	ns
t_{LAFC2}	(1/10) t_{CY} − 75	MIN	ns
t_{CA1}	(1/15) t_{CY} − 40	MIN	ns
t_{CA2}	(4/15) t_{CY} − 40	MIN	ns
t_{CP}	(1/10) t_{CY} − 40 / (2/15) t_{CY} − 80	MIN	ns
t_{PC}	(4/15) t_{CY} −200	MIN	ns
t_{PR}	(17/30) t_{CY} −120	MAX	ns
t_{PF}	(1/10) t_{CY}	MAX	ns
t_{DP}	(2/ 5) t_{CY} −150	MIN	ns
t_{PD}	(1/10) t_{CY} − 50	MIN	ns
t_{PP}	(7/10) t_{CY} −250	MIN	ns
t_{PL}	(4/15) t_{CY} −200	MIN	ns
t_{LP}	(1/10) t_{CY} −100 / (1/30) t_{CY} − 30	MIN	ns
t_{PV}	(3/10) t_{CY} −100	MAX	ns
t_{OPRR}	(3/15) t_{CY}	MIN	ns
t_{CY}	11 MHz		μs

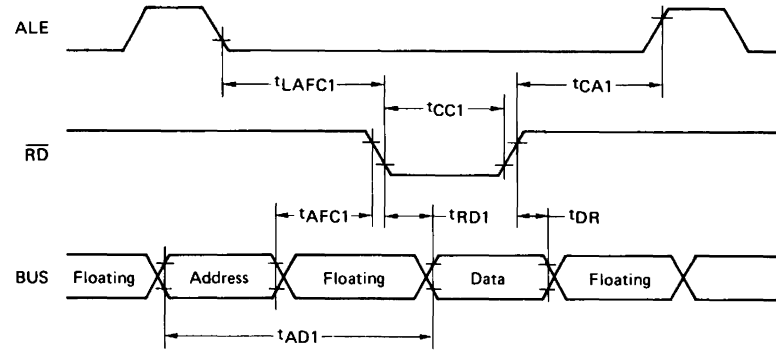
Note: Double values reflect: 8039HL, 49H/8749H

TIMING WAVEFORMS

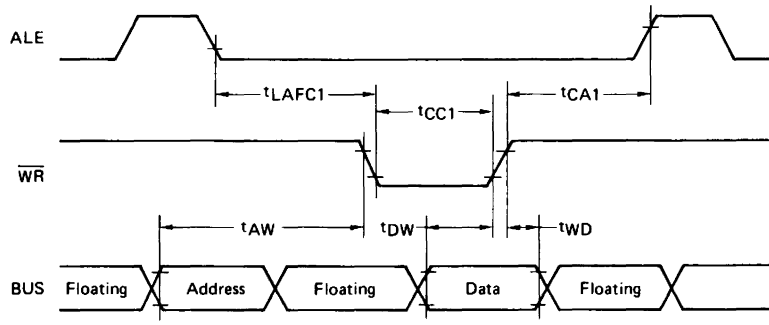
INSTRUCTION FETCH FROM EXTERNAL MEMORY



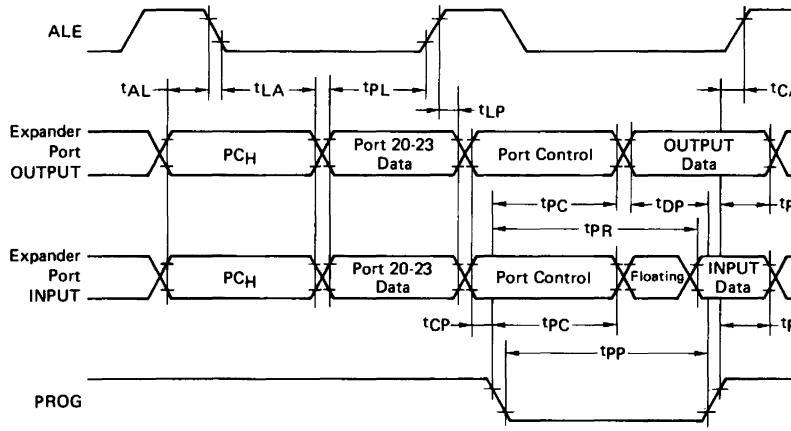
READ FROM EXTERNAL DATA MEMORY



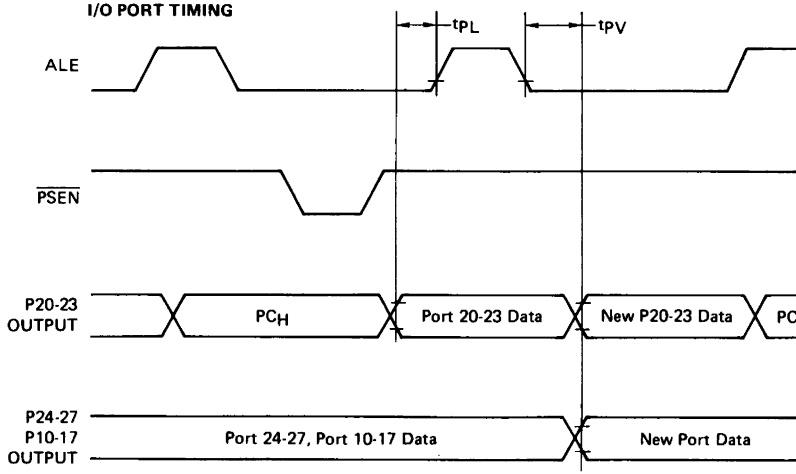
WRITE TO EXTERNAL MEMORY



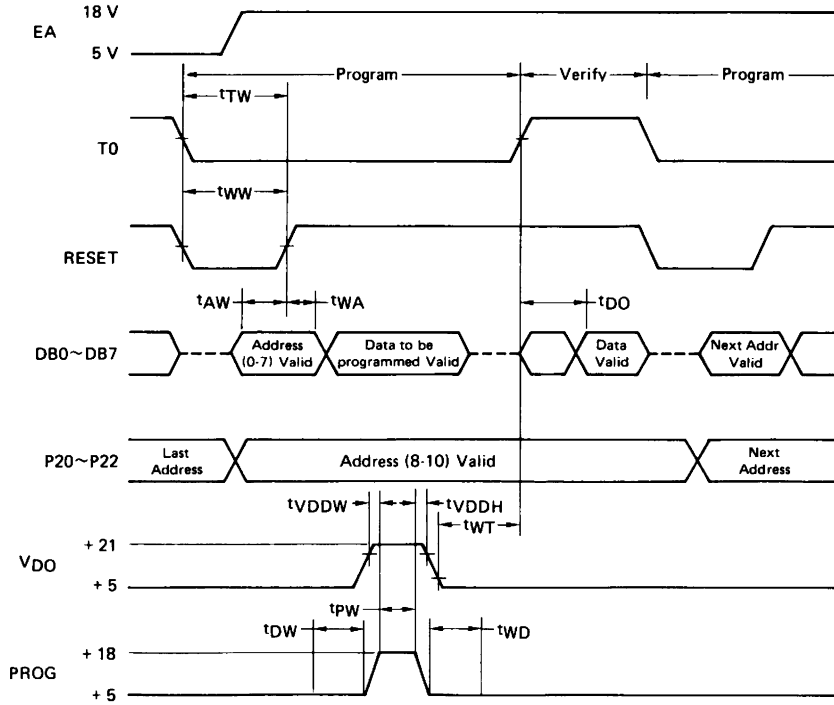
PORT 2 TIMING



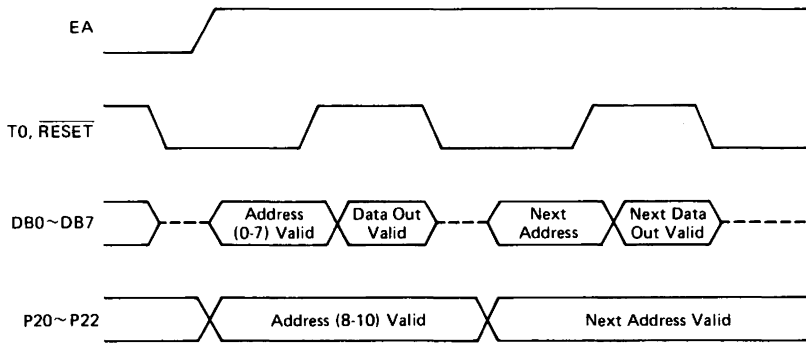
I/O PORT TIMING



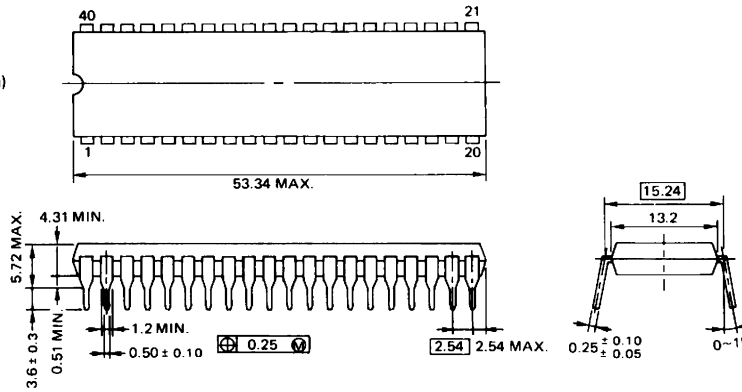
WAVEFORMS FOR PROGRAMMING THE μPD8749H



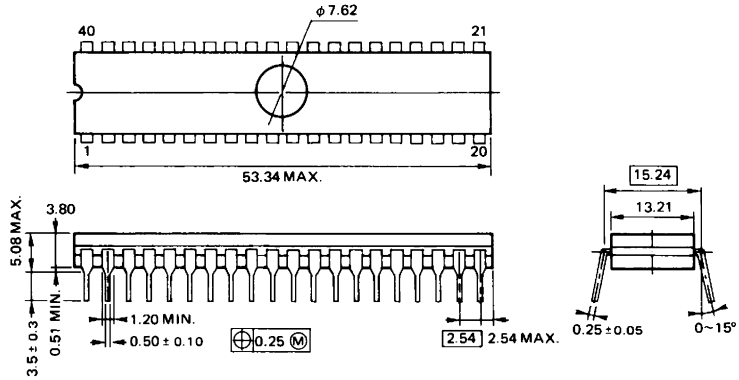
PROGRAM/VERIFY TIMING (ROM/EPROM)



40-PIN PLASTIC
DIP PACKAGE
OUTLINE (Unit : mm)
μPD8039HLC
μPD8049HC–XXX
μPD8749HC



40-PIN CERAMIC
DIP PACKAGE
OUTLINE (Unit : mm)
μPD8749HD



CHAPTER 2

THE μCOM84/87/78KIII FAMILY

μPD8048H(A)

μPD8048H(S)

μPD8049H(A)

μPD80C49HC(S)

μPD80C50HC(A)

μPD78C10G(S)/L(S),μPD78C11G(S)/L(S)

μPD78C14G(A)/L(A)

μPD78310G(A)/L(A),μPD78312G(A)/L(A)

GENERAL INFORMATION

NEC

NMOS MICROCOMPUTER SELECTION GUIDE

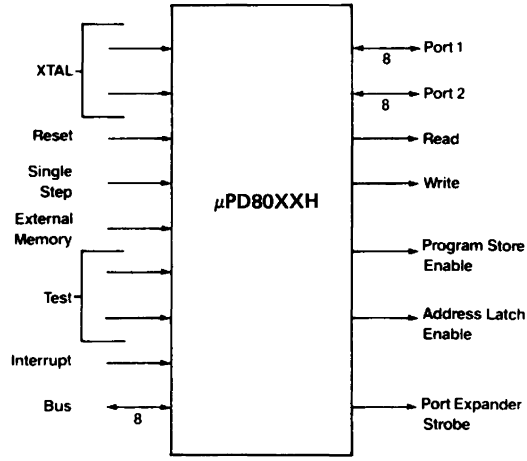
SINGLE CHIP 8-BIT MICROCOMPUTERS

DEVICE	SPECIAL FEATURES	ROM	RAM	I/O	PROCESS	CYCLE	SUPPLY VOLTAGE	PINS
8049H(A)	Temp Range −40°C to +85°C	2048x8	128x8	27	NMOS	1·360 μs	5V±10 %	40
8049H(S)	Temp Range −40°C to +110°C	2048x8	128x8	27	NMOS	1·875 μs	5V±10 %	40
8048H(A)	Temp Range −40°C to +85°C	1024x8	64x8	27	NMOS	2·50 μs	5V±10 %	40
8048H(S)	Temp Range −40°C to +110°C	1024x8	64x8	27	NMOS	3·75 μs	5V±10 %	40

SPECIAL A AND S GRADE

	NORMAL	(A) GRADE	(S) GRADE
1st electrical test	at room temp	at 85 deg c	at 110 deg c
Burn-in	4 hours	16 hours	16 hours
2nd electrical test	at room temp	at room temp	at room temp

LOGIC SYMBOL



INSTRUCTION SET

SYMBOL DEFINITIONS

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0–7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number of Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator
P_p	Port Designator (p–1, 2 or 4–7)
PSW	Program Status Word
Rr	Register Designator (r–0, 1 or 0–7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
S	Program Counters Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location
←	Replaced By

INSTRUCTION SET

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Accumulator																
ADD A, # data	(A) ← (A) + data	Add immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
Add A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 – 1	Add indirect the contents of the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, # data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 – 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 – 1	Add indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, # d8	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 – 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) 1	DECREMENT by 1 the Accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator.	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 – 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_{4-7}) ← $(A_0 – 3)$	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
Branch																
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 If (Rr) = 0 (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 – 7) ← addr If Bb = 1 (PC) ← (PC) + 2 If Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 – 7) ← addr If C = 1 (PC) ← (PC) + 2 If C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC 0 – 7) ← addr If F0 = 1 (PC) ← (PC) + 2 If F0 = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC 0 – 7) ← addr If F1 = 1 (PC) ← (PC) + 2 If F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 – 7) ← addr If C = 0 (PC) ← (PC) + 2 If C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 – 7) ← addr If I = 0 (PC) ← (PC) + 2 If I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

INSTRUCTION SET (Cont.)

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Branch (Cont.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
Control																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 - 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 - 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 - 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 - 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
Data Moves																
MOV A, # data	(A) ← data	Move immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0 – 7	Move immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0 – 1	Move immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ⇄ ((Rr)(0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
Flags																
CPL C	(C) ← NOT (C)	Complement content of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement content of Flag F1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

INSTRUCTION SET (Cont.)

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Input/Output																
ANL BUS, # data	(BUS) ← (BUS) AND data	Logical and Immediate-specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1 – 2	Logical and Immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 – 3) p = 4 – 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1 – 2	Input data from designated port (1 – 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 – 7 (A 4 – 7) ← 0	Move contents of designated port (4 – 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 – 3; p = 4 – 7	Move contents of Accumulator to designated port (4 – 7).	0	0	1	1	1	1	p	p	1	1				
ORL BUS, # data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 – 7	Logical or contents of Accumulator with designated port (4 – 7).	1	0	0	0	1	1	p	p	1	1				
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1 – 2	Logical or Immediate specified data with designated port (1 – 2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A ⑤	(BUS) ← (A)	Output contents of Accumulator onto BUS.	0	0	0	0	0	0	1	0	1	1				
OUTL Pp, A	(Pp) ← (A); p = 1 – 2	Output contents of Accumulator to designated port (1 – 2).	0	0	1	1	1	0	p	p	1	1				
Registers																
DEC Rr, (Rr)	(Rr) ← (Rr) – 1; r = 0 – 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1; r = 0 – 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 – 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
Subroutine																
CALL addr	((SP)) ← (PC), (PSW 4 – 7) (SP) ← (SP) + 1 (PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
Timer/Counter																
EN TCNTI		Enable Internal interrupt Flag for Timer Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
Miscellaneous																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.
⑤ When the Bus is written to with an OUTL instruction the Bus remains an Output Port until either device is reset or a MOVX instruction is executed.

HIGH PERFORMANCE SINGLE CHIP 8-BIT MICROCOMPUTERS

DESCRIPTION

The NEC μPD8048, μPD8748 and μPD8035L are single component, 8-bit, parallel microprocessors using N-channel silicon gate MOS technology. The μPD8048/8748/8035 efficiently function in control as well as arithmetic applications. The flexibility of the instruction set allows for the direct set and reset of individual data bits within the accumulator and the I/O port structure. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The μPD8048/8748/8035L instruction set is comprised of 1 and 2 byte instructions with over 70 % single-byte and requiring only 1 or 2 cycles per instruction with over 50 % single-cycle.

The μPD8048 series of microprocessors will function as stand alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8048 contains the following functions usually found in external peripheral devices: 1024 x 8 bits of ROM program memory; 64 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

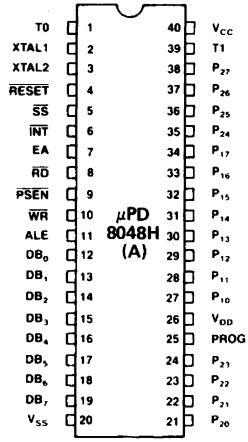
The μPD8748 differs from the μPD8048 only in its 1024 x 8-bit UV erasable EPROM program memory instead of the 1024 x 8-bit ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

The μPD8035L is intended for applications using external program memory only. It contains all the features of the μPD8048 except the 1024 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

FEATURES

- Fully Compatible With Industry Standard 8048
- NMOS Silicon Gate Technology Requiring a Single +5V Supply
- 2.5 μs Cycle Time. All Instruction 1 or 2 Bytes
- Interval Timer/Event Counter
- 64 x 8 bit Ram Data Memory
- Single Level Interrupt
- 96 Instructions: 70 % Single Byte
- 27 I/O Lines
- Internal Clock Generator
- 8 Level Stack
- Compatible With 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40 Pin Packages
- Temp Range −40°C to +85°C

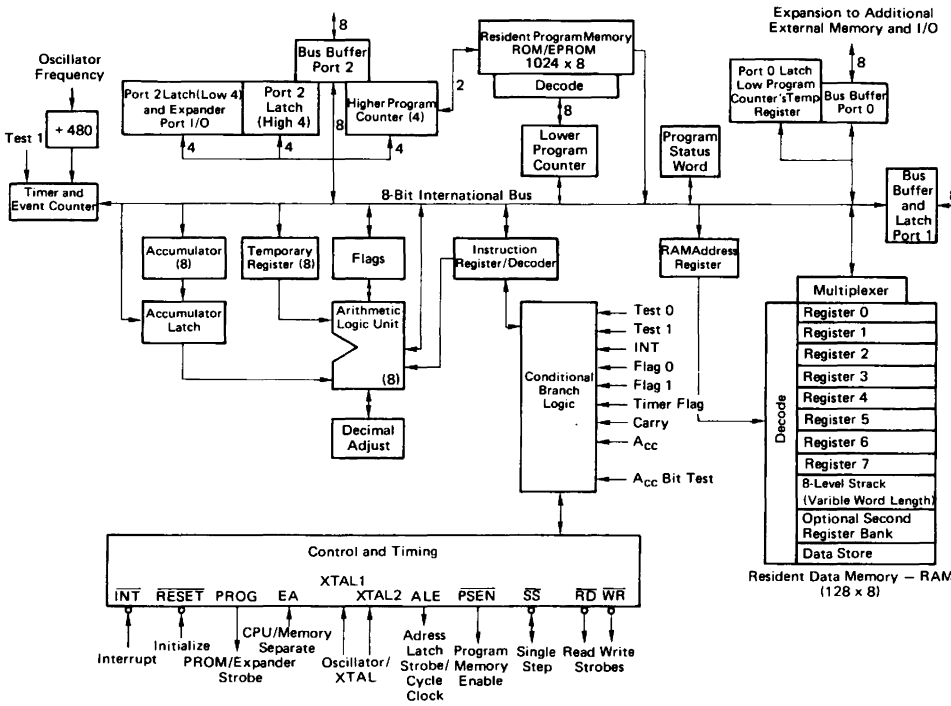
PIN CONFIGURATION



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENT0 CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non-TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{RESET}$	Active low input for processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe output (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occuring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12-19	D_0-D_7 BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the D_0-D_7 BUS can be latched in a static mode. During an external memory fetch, the D_0-D_7 BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the D_0-D_7 BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21-24, 35-38	P_{20}-P_{27}: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in P_{20}-P_{23}. Bits P_{20}-P_{23} are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	Program Pulse. A +25V pulse applied to this input is used for programming the μPD8748. PROG is also used as an output strobe for the μPD8243.
26	V_{DD}	Programming Power Supply. V_{DD} must be set to +25V for programming the μPD8748, and to +5V for the ROM and PROM versions for normal operation. V_{DD} functions as the Low Power Standby input for the μPD8048.
27-34	P_{10}-P_{17}: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power supply. V_{CC} is +5V for programming and operation of the μPD8748, and for operation of the μPD8035L and μPD8048.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature	−40°C to +85°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +150°C
Voltage on Any Pin	−0.5V to +7V ①
Power Dissipation	1.5 W

Note: ① With respect to ground.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated unter conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −40°C to +85°C; V_{CC} = V_{DD} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}		0		0.7	V
Input Low Voltage ($\overline{RESET}$, X1, X2)	V_{IL1}		0		0.7	V
Input High Voltage (All Except XTAL 1, XTAL 2, RESET)	V_{IH}		2.3		V_{CC}	V
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}		3.8		V_{CC}	V
Output Low Voltage (BUS)	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
Output Low Voltage (PROG)	V_{OL2}	I_{OL} = 2.0 mA			0.45	V
Output High Voltage (BUS)	V_{OH}	I_{OH} = −100 μA	2.4			V
Output High Voltage (RD, WR, PSEN, ALE)	V_{OH1}	I_{OH} = −100 μA	2.4			V
Output High Voltage (All Other Outputs)	V_{OH2}	I_{OH} = −30 μA	2.4			V
Input Leakage Current (T_1, EA, INT)	I_{IL}	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$			±10	μA
Input Leakage Current (P_{10}–P_{17}, P_{20}–P_{27}, EA, $\overline{SS}$)	I_{IL1}	$V_{CC} \geqslant V_{IN} \geqslant V_{SS}$ + 0.45V			−700	μA
Output Leakage Current (BUS, T_0–High Impedance State)	I_{OL}	$V_{CC} \geqslant V_{IN} \geqslant V_{SS}$ + 0.45V			±10	μA
Power Down Supply Current	I_{DD}	T_a = 25°C			8	mA
Total Supply Current	$I_{DD}+I_{CC}$	T_a = 25°C			100	mA
RAM Standby Voltage	V_{DD}	Standby Mode. Reset ⩽0.6V	3.0		5.5	V

AC CHARACTERISTICS

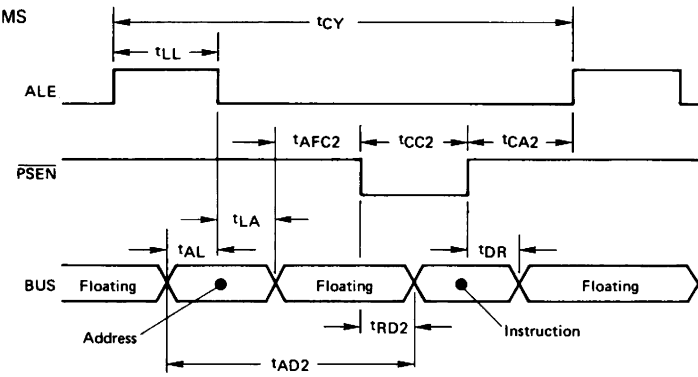
T_a = −40°C to +80°C; V_{CC} = V_{DD} = 5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	f(t_{CY}) and TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
ALE Pulse Width	t_{LL}	7/30 t_{CY} −170	410			ns
Addr Setup to ALE	t_{AL}	2/15 t_{CY} −110	220			ns
Addr Hold from ALE	t_{LA}	1/15 t_{CY} −40	120			ns
Control Pulse Width (RD, WR)	t_{CC1}	1/2 t_{CY} −200	1050			ns
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}	2/5 t_{CY} −200	800			ns
Data Setup $\overline{WR}$	t_{DW}	13/30 t_{CY} −200	880			ns
Data Hold after $\overline{WR}$	t_{WD}	1/15 t_{CY} −50	110			ns
Data Hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	1/10 t_{CY} −30	0		220	ns
$\overline{RD}$ to Data in	t_{RD1}	2/5 t_{CY} −200			800	ns
$\overline{PSEN}$ to Data in	t_{RD2}	3/10 t_{CY} −200			550	ns
Addr Setup to $\overline{WR}$	t_{AW}	1/3 t_{CY} −150	680			ns
Addr Setup to Data ($\overline{RD}$)	t_{AD1}	11/15 t_{CY} −250			1570	ns
Addr Setup to Data ($\overline{PSEN}$)	t_{AD2}	8/15 t_{CY} −250			1090	ns
Addr Float to $\overline{RD}$, $\overline{WD}$	t_{AFC1}	2/15 t_{CY} −40	290			ns
Addr Float to $\overline{PSEN}$	t_{AFC2}	1/30 t_{CY} −40	40			ns
ALE to Control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	1/15 t_{CY} −75	420			ns
ALE to Control ($\overline{PSEN}$)	t_{LAFC2}	1/10 t_{CY} −75	170			ns
Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t_{CA1}	1/15 t_{CY} −40	120			ns
Control to ALE ($\overline{PSEN}$)	t_{CA2}	4/15 t_{CY} −40	620			ns
Port Control Setup to $\overline{PROG}$	t_{CP}	1/10 t_{CY} −40	210			ns
Port Control Hold to $\overline{PROG}$	t_{PC}	4/15 t_{CY} −200	460			ns
PROG to P2 Input Valid	t_{PR}	17/30 t_{CY} −120			1300	ns
Input Data Hold from $\overline{PROG}$	t_{PF}	1/10 t_{CY}			250	ns
Output Data Setup	t_{DP}	2/5 t_{CY} −150	850			ns
Output Data Hold	t_{PD}	1/10 t_{CY} −50	200			ns
$\overline{PROG}$ Pulse Width	t_{PP}	7/10 t_{CY} −250	1500			ns
Port 2 I/O Setup to ALE	t_{PL}	4/15 t_{CY} −200	460			ns
Port 2 I/O Hold to ALE	t_{LP}	1/10 t_{CY} −100	150			ns
Port Output from ALE	t_{PV}	3/10 t_{CY} +100			850	ns
Cycle Time	t_{CY}	6 MHz (max.)	2.5		15	μs
TO Rep Rate	t_{OPRR}	3/15 t_{CY}	500			ns

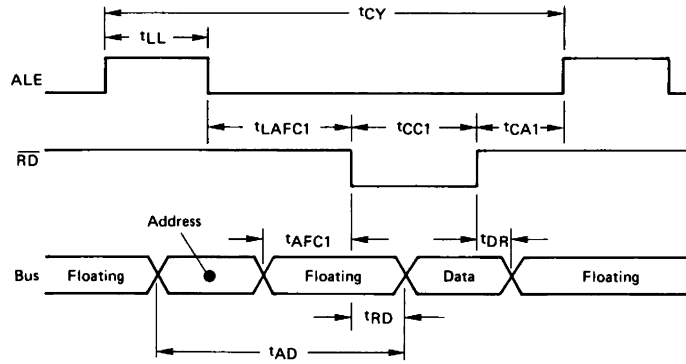
Notes: Control Outputs CL = 80pF
BUS Outputs CL = 150pF
BUS High Impedance Load 20pF

TIMING WAFEFORMS

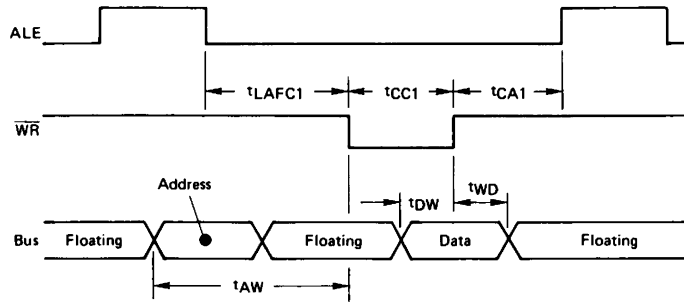
Instruction Fetch from External Memory



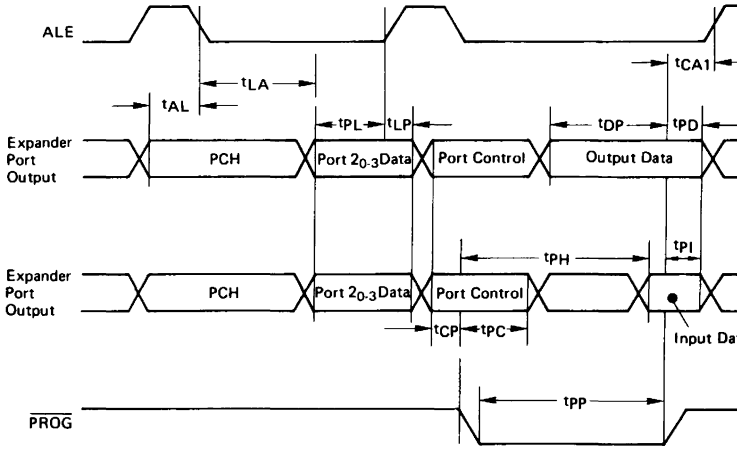
Read from External Data Memory



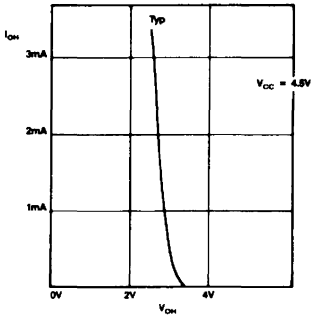
Write to External Memory



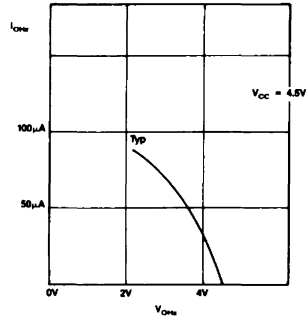
Port 2 Timing



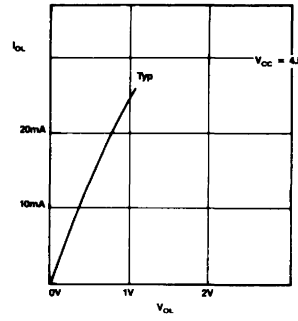
BUS Output High Voltage vs. Source Current



Port P1 and P2 Output
High Voltage vs. Source Current

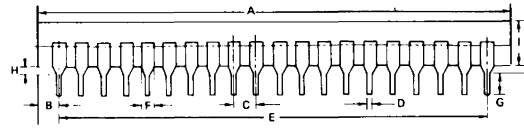


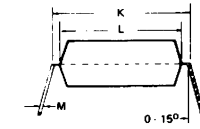
BUS Output Low Voltage vs. Sink Current



40 PIN PLASTIC
μPD8048HC

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.5 MIN	0.06 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$





HIGH PERFORMANCE SINGLE CHIP 8-BIT MICROCOMPUTERS

DESCRIPTION

The NEC μPD8048, μPD8748 and μPD8035L are single component, 8-bit, parallel microprocessors using N-channel silicon gate MOS technology. The μPD8048/8748/8035 efficiently function in control as well as arithmetic applications. The flexibility of the instruction set allows for the direct set and reset of individual data bits within the accumulator and the I/O port structure. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The μPD8048/8748/8035L instruction set is comprised of 1 and 2 byte instructions with over 70 % single-byte and requiring only 1 or 2 cycles per instruction with over 50 % single-cycle.

The μPD8048 series of microprocessors will function as stand alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8048 contains the following functions usually found in external peripheral devices: 1024 x 8 bits of ROM program memory; 64 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

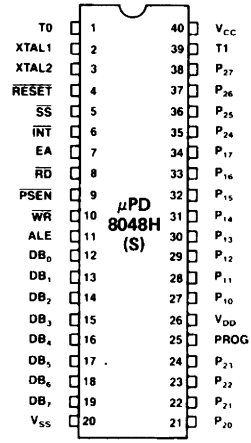
The μPD8748 differs from the μPD8048 only in its 1024 x 8-bit UV erasable EPROM program memory instead of the 1024 x 8-bit ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

The μPD8035L is intended for applications using external program memory only. It contains all the features of the μPD8048 except the 1024 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

FEATURES

- Fully Compatible With Industry Standard 8048
- NMOS Silicon Gate Technology Requiring a Single +5V Supply
- 3.75 μs Cycle Time. All Instruction 1 or 2 Bytes
- Interval Timer/Event Counter
- 64 x 8 bit RAM Data Memory
- Single Level Interrupt
- 96 Instructions: 70 % Single Byte
- 27 I/O Lines
- Internal Clock Generator
- 8 Level Stack
- Compatible With 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40 Pin Packages
- Temp Range −40°C to +110°C

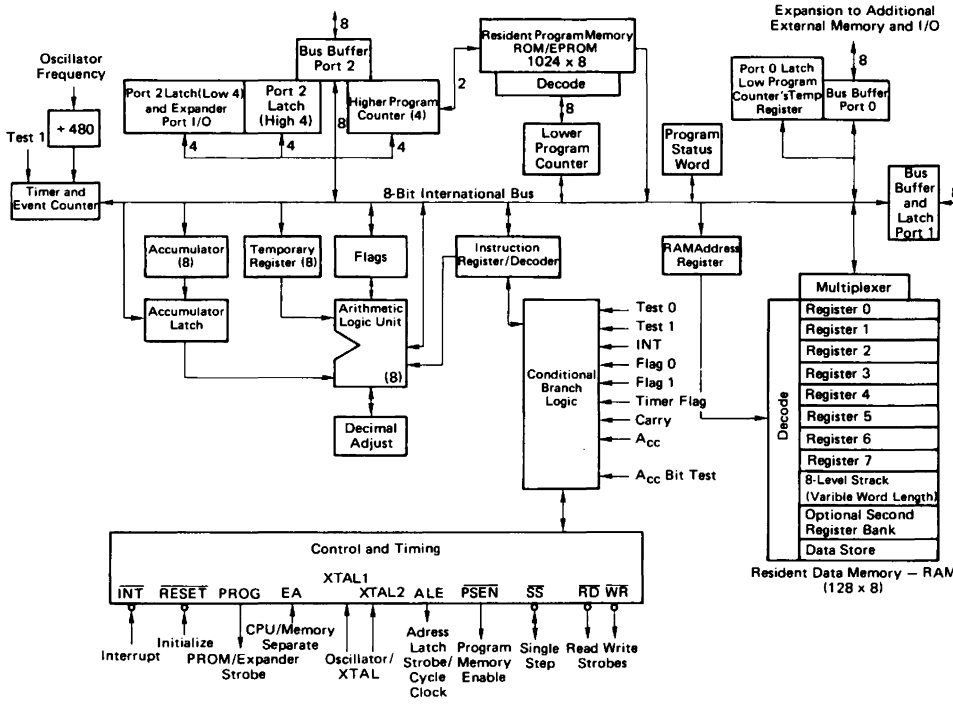
PIN CONFIGURATION



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non-TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{RESET}$	Active low input for processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe output (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occuring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12-19	D_0-D_7 BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the D_0-D_7 BUS can be latched in a static mode. During an external memory fetch, the D_0-D_7 BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the D_0-D_7 BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21-24, 35-38	P_{20}-P_{27}: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in P_{20}-P_{23}. Bits P_{20}-P_{23} are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	Program Pulse. A +25V pulse applied to this input is used for programming the μPD8748. PROG is also used as an output strobe for the μPD8243.
26	V_{DD}	Programming Power Supply. V_{DD} must be set to +25V for programming the μPD8748, and to +5V for the ROM and PROM versions for normal operation. V_{DD} functions as the Low Power Standby input for the μPD8048.
27-34	P_{10}-P_{17}: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power supply. V_{CC} is +5V for programming and operation of the μPD8748, and for operation of the μPD8035L and μPD8048.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature	−40°C to +110°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +150°C
Voltage on Any Pin	−0.5V to +7V ①
Power Dissipation	1.5 W

Note: ① With respect to ground.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated unter conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −40°C to +110°C; V_{CC} = V_{DD} = +5V ± 10 %; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}				0.5	V
Input Low Voltage ($\overline{RESET}$, X1, X2)	V_{IL1}				0.5	V
Input High Voltage (All Except XTAL 1, XTAL 2, RESET)	V_{IH}		2.3			V
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}		3.8			V
Output Low Voltage (BUS)	V_{OL}	I_{OL} = 1.6 mA			0.45	V
Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}	I_{OL} = 1.6 mA			0.45	V
Output Low Voltage (PROG)	V_{OL2}	I_{OL} = 1.6 mA			0.45	V
Output Low Voltage (All Other Outputs)	V_{OL3}	I_{OL} = 1.6 mA			0.45	V
Output High Voltage (BUS)	V_{OH}	I_{OH} = −50 μA	2.4			V
Output High Voltage (RD, WR, PSEN, ALE)	V_{OH1}	I_{OH} = −50 μA	2.4			V
Output High Voltage (All Other Outputs)	V_{OH2}	I_{OH} = −15 μA	2.4			V
Input Leakage Current (T_1, INT)	I_{IL}	$V_{SS} \leq V_{IN} \leq V_{CC}$			±10	μA
Input Leakage Current (P_{10}–P_{17}, P_{20}–P_{27}, EA, $\overline{SS}$)	I_{IL1}	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V			−700	μA
Output Leakage Current (BUS, T_0–High Impedance State)	I_{OL}	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V			±10	μA
Power Down Supply Current	I_{DD}	T_a = 25°C			8	mA
Total Supply Current	$I_{DD}+I_{CC}$	T_a = 25°C			100	mA
RAM Standby Voltage	V_{DD}	Standby Mode. Reset ≤0.5V	4.5		5.5	V

AC CHARACTERISTICS

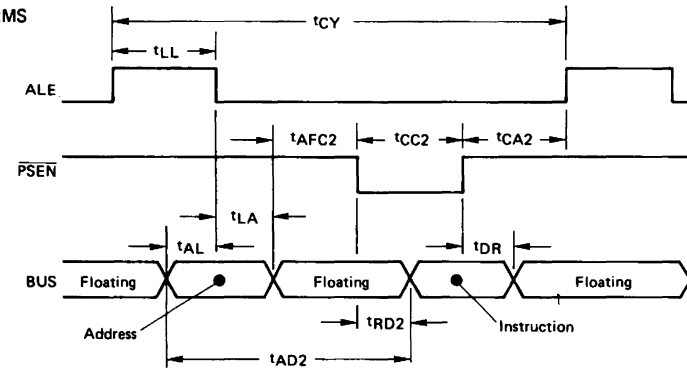
T_a = −40°C to +110°C; V_{CC} = V_{DD} = 5V ± 10 %; V_{SS} = 0V

PARAMETER	SYMBOL	f(t_{CY}) and TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
ALE Pulse Width	t_{LL}	7/30 t_{CY} −170	410			ns
Addr Setup to ALE	t_{AL}	2/15 t_{CY} −110	220			ns
Addr Hold from ALE	t_{LA}	1/15 t_{CY} −40	120			ns
Control Pulse Width (RD, WR)	t_{CC1}	1/2 t_{CY} −200	1050			ns
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}	2/5 t_{CY} −200	800			ns
Data Setup $\overline{WR}$	t_{DW}	13/30 t_{CY} −200	880			ns
Data Hold after $\overline{WR}$	t_{WD}	1/15 t_{CY} −50	110			ns
Data Hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	1/10 t_{CY} −30	0		220	ns
$\overline{RD}$ to Data in	t_{RD1}	2/5 t_{CY} −200			800	ns
$\overline{PSEN}$ to Data in	t_{RD2}	3/10 t_{CY} −200			550	ns
Addr Setup to $\overline{WR}$	t_{AW}	1/3 t_{CY} −150	680			ns
Addr Setup to Data ($\overline{RD}$)	t_{AD1}	11/15 t_{CY} −250			1570	ns
Addr Setup to Data ($\overline{PSEN}$)	t_{AD2}	8/15 t_{CY} −250			1090	ns
Addr Float to $\overline{RD}$, $\overline{WD}$	t_{AFC1}	2/15 t_{CY} −40	290			ns
Addr Float to $\overline{PSEN}$	t_{AFC2}	1/30 t_{CY} −40	40			ns
ALE to Control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	1/15 t_{CY} −75	420			ns
ALE to Control ($\overline{PSEN}$)	t_{LAFC2}	1/10 t_{CY} −75	170			ns
Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t_{CA1}	1/15 t_{CY} −40	120			ns
Control to ALE ($\overline{PSEN}$)	t_{CA2}	4/15 t_{CY} −40	620			ns
Port Control Setup to $\overline{PROG}$	t_{CP}	1/10 t_{CY} −40	210			ns
Port Control Hold to $\overline{PROG}$	t_{PC}	4/15 t_{CY} −200	460			ns
PROG to P2 Input Valid	t_{PR}	17/30 t_{CY} −120			1300	ns
Input Data Hold from $\overline{PROG}$	t_{PF}	1/10 t_{CY}			250	ns
Output Data Setup	t_{DP}	2/5 t_{CY} −150	850			ns
Output Data Hold	t_{PD}	1/10 t_{CY} −50	200			ns
$\overline{PROG}$ Pulse Width	t_{PP}	7/10 t_{CY} −250	1500			ns
Port 2 I/O Setup to ALE	t_{PL}	4/15 t_{CY} −200	460			ns
Port 2 I/O Hold to ALE	t_{LP}	1/10 t_{CY} −100	150			ns
Port Output from ALE	t_{PV}	3/10 t_{CY} +100			850	ns
Cycle Time	t_{CY}	4 MHz (max.)	3.75		15	μs
TO Rep Rate	t_{OPRR}	3/15 t_{CY}	500			ns

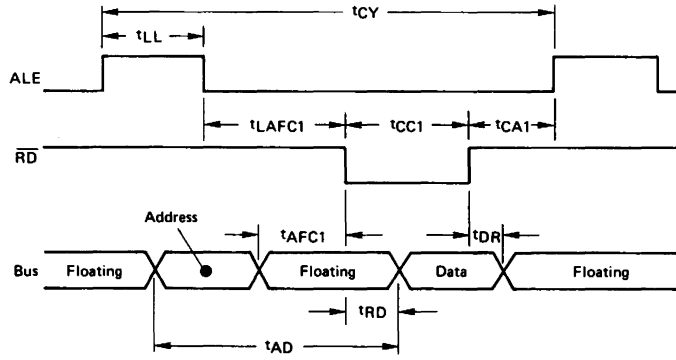
Notes: Control Outputs CL = 80pF
BUS Outputs CL = 150pF
BUS High Impedance Load 20pF

TIMING WAFEFORMS

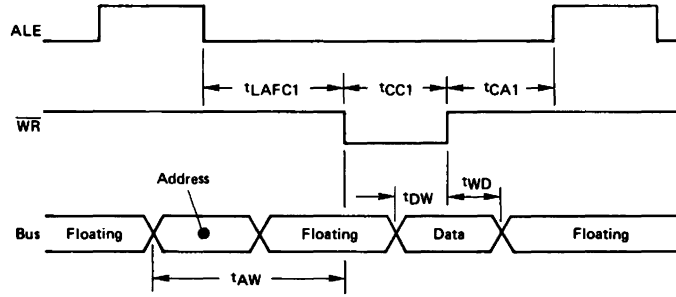
Instruction Fetch from External Memory



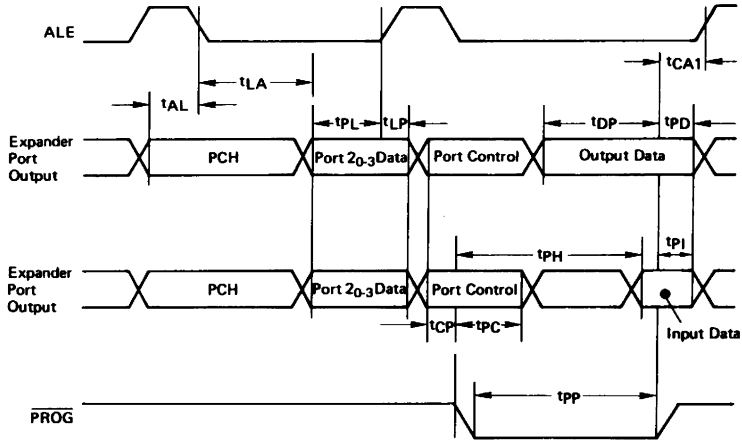
Read from External Data Memory



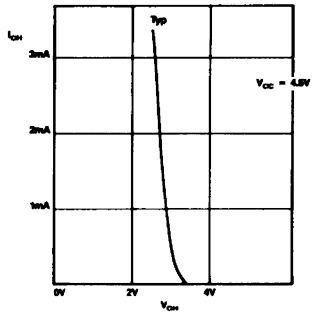
Write to External Memory



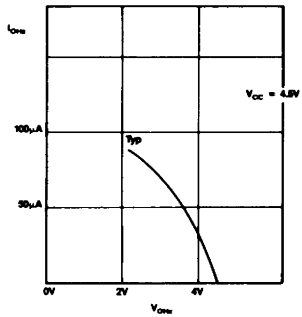
Port 2 Timing



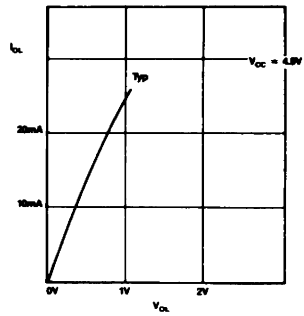
BUS Output High Voltage vs. Source Current



Port P1 and P2 Output
High Voltage vs. Source Current



BUS Output Low Voltage vs. Sink Current



40 PIN PLASTIC
μPD8048HC

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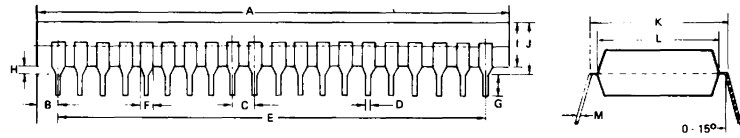
A	51.5 MAX	2.028 MAX
B	1.62 MAX	0.064 MAX
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.5 MIN	0.06 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24 TYP	0.600 TYP
L	13.2 TYP	0.520 TYP
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



HIGH PERFORMANCE SINGLE CHIP 8-BIT MICROCOMPUTERS

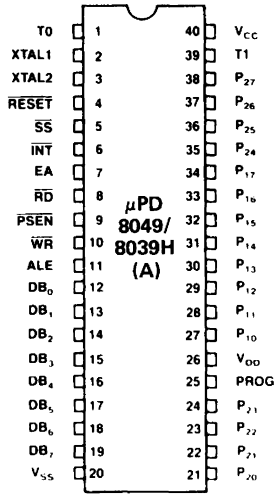
DESCRIPTION

The NEC μPD8049 and μPD8039H are single chip 8-bit microcomputers. The processors differ only in their internal program memory options: the μPD8049 has 2K x 8 bit mask ROM and the μPD8039H has external program memory. Both of these devices feature high performance 11 MHz operation.

FEATURES

- High Performance 11 MHz Operation
- Fully Compatible with Industry Standard 8049/8039
- Pin Compatible with the μPD8048/8748/8035
- NMOS Silicon Gate Technology Requiring a Single +5V ± 10 % Supply
- 1.36 μs Cycle Time. All Instructions 1 or 2 Bytes
- Programmable Interval Timer/Event Counter
- 2K x 8 bit ROM, 128 x 8 bit RAM
- Single Level Interrupt
- 96 Instructions: 70 Percent Single Byte
- 27 I/O Lines
- Internal Clock Generator
- Expandable with 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40-Pin Packages
- Temp Range –40°C to +85°C

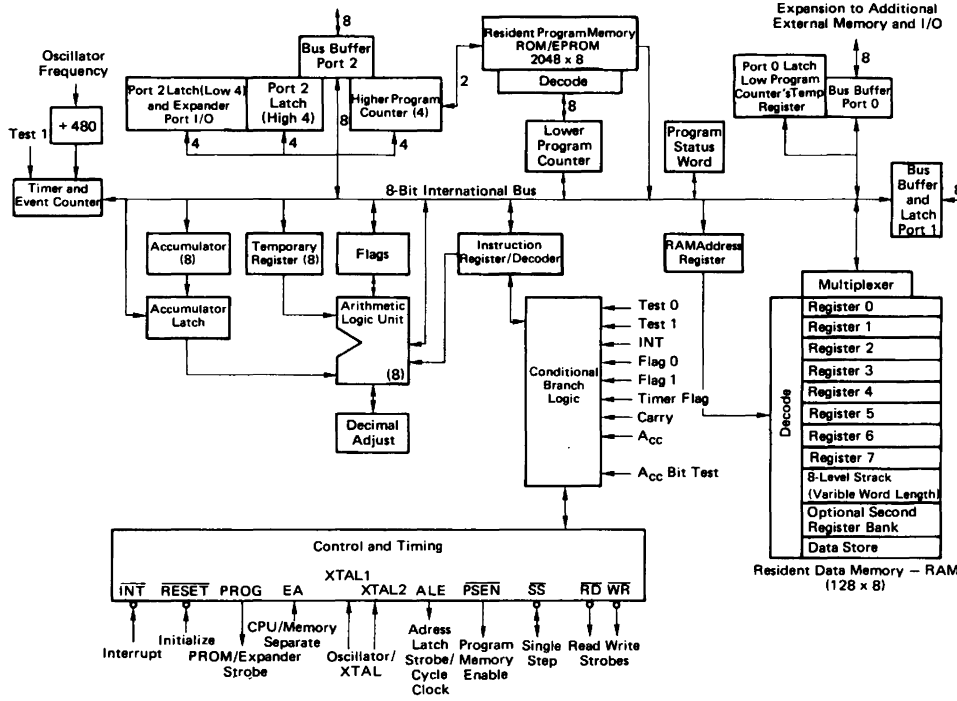
PIN CONFIGURATION



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal, LC, or external frequency source. (Non-TTL compatible V_{IH}.)
3	XTAL 2	The other side of the crystal or LC frequency source. For external sources, XTAL 2 must be driven with the logical complement of the XTAL 1 input.
4	$\overline{RESET}$	Active low input from processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe outputs (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occuring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12-19	D_0-D_7 BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the D_0-D_7 BUS can be latched in a static mode. During an external memory fetch, the D_0-D_7 BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the D_0-D_7 BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21-24, 35-38	P_{20}-P_{27}: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in P_{20}-P_{23}. Bits P_{20}-P_{23} are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	PROG is used as an output strobe for μPD8243's during I/O expansion. When the μPD8049 is used in a stand-alone mode the PROG pan can be allowed to float.
26	V_{DD}	V_{DD} is used to provide +5V to the 128 x 8 bit RAM section. During normal operation V_{CC} must also be +5V to provide power to the other functions in the device. During stand-by operation V_{DD} must remain at +5V while V_{CC} is at ground potential.
27-34	P_{10}-P_{17}: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T_1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power supply. V_{CC} is +5V during normal operation.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature	–40°C to +85°C
Storage Temperature (Ceramic Package)	–65°C to +150°C
Storage Temperature (Plastic Package)	–65°C to +150°C
Voltage on Any Pin	–0.5V to +7V①
Power Dissipation	1.5 W

Note: ① With respect to ground.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated unter conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = -40°C$ to $+85°C$; $V_{CC} = V_{DD} = +5V \pm 10\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}		−0.5		0.7	V
Input Low Voltage ($\overline{RESET}$, X1, X2)	V_{IL1}		−0.5		0.7	V
Input High Voltage (All Except XTAL 1, XTAL 2, RESET)	V_{IH}		2.3		V_{CC}	V
Input High Voltage ($\overline{RESET}$, XTAL 1, XTAL 2)	V_{IH1}		3.8		V_{CC}	V
Output Low Voltage (BUS)	V_{OL}	$I_{OL} = 2.0$ mA			0.45	V
Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}	$I_{OL} = 2.0$ mA			0.45	V
Output Low Voltage (PROG)	V_{OL2}	$I_{OL} = 2.0$ mA			0.45	V
Output Low Voltage (All Other Outputs)	V_{OL3}	$I_{OL} = 2.0$ mA			0.45	V
Output High Voltage (BUS)	V_{OH}	$I_{OH} = -100\ \mu A$	2.4			V
Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, $\overline{ALE}$)	V_{OH1}	$I_{OH} = -100\ \mu A$	2.4			V
Output High Voltage (All Other Outputs)	V_{OH2}	$I_{OH} = -30\ \mu A$	2.4			V
Input Leakage Current (T_1, EA, INT)	I_{IL}	$V_{SS} \leq V_{IN} \leq V_{CC}$			±10	μA
Output Leakage Current (BUS, T_0—High Impedance State)	I_{OL}	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45V$			±10	μA
Power Down Supply Current	I_{DD}	$T_a = 25°C$		5	10	mA
Total Supply Current	$I_{DD}+I_{CC}$	$T_a = 25°C$		80	140	mA

AC CHARACTERISTICS

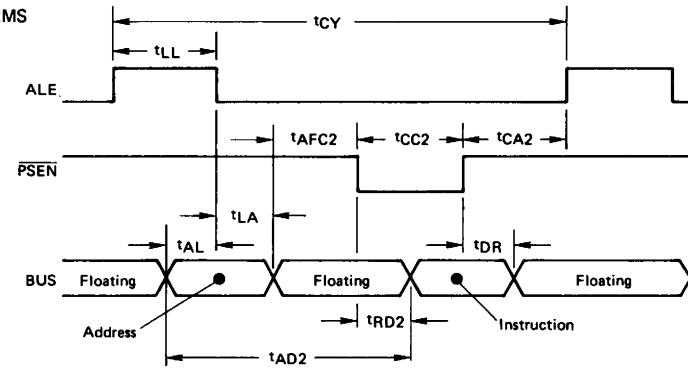
T_a = −40°C to +85°C; V_{CC} = V_{DD} = 5V ± 10 %; V_{SS} = 0V

PARAMETER	SYMBOL	f(t_{CY}) and TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
ALE Pulse Width	t_{LL}	7/30 t_{CY} −170	180			ns
Addr Setup to ALE	t_{AL}	2/15 t_{CY} −110	90			ns
Addr Hold from ALE	t_{LA}	1/15 t_{CY} −40	60			ns
Control Pulse Width (RD, WR)	t_{CC1}	1/2 t_{CY} −200	550 400			ns
Data Setup $\overline{WR}$	t_{DW}	13/30 t_{CY} −200	450			ns
Data Hold after $\overline{WR}$	t_{WD}	1/15 t_{CY} −50	50			ns
Data Hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	1/10 t_{CY} −30	0		120	ns
$\overline{RD}$ to Data in	t_{RD1}	2/5 t_{CY} −200			400	ns
$\overline{PSEN}$ to Data in	t_{RD2}	3/10 t_{CY} −200			250	ns
Addr Setup to $\overline{WR}$	t_{AW}	1/3 t_{CY} −150	350			ns
Addr Setup to Data ($\overline{RD}$)	t_{AD1}	11/15 t_{CY} −250			850	ns
Addr Setup to Data ($\overline{PSEN}$)	t_{AD2}	8/15 t_{CY} −250			550	ns
Addr Float to $\overline{RD}$, $\overline{WD}$	t_{AFC1}	2/15 t_{CY} −40	160			ns
Addr Float to $\overline{PSEN}$	t_{AFC2}	1/30 t_{CY} −40	10			ns
ALE to Control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	1/5 t_{CY} −75	420			ns
ALE to Control ($\overline{PSEN}$)	t_{LAFC2}	1/10 t_{CY} −75	170			ns
Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t_{CA1}	1/15 t_{CY} −40	120			ns
Control to ALE ($\overline{PSEN}$)	t_{CA2}	4/15 t_{CY} −40	620			ns
Port Control Setup to $\overline{PROG}$	t_{CP}	1/10 t_{CY} −40	110			ns
Port Control Hold to $\overline{PROG}$	t_{PC}	4/15 t_{CY} −200	200			ns
PROG to P2 Input Valid	t_{PR}	17/30 t_{CY} −120			730	ns
Input Data Hold from $\overline{PROG}$	t_{PF}	1/10 t_{CY}			150	ns
Output Data Setup	t_{DP}	2/5 t_{CY} −150	450			ns
Output Data Hold	t_{PD}	1/10 t_{Cy} −50	100			ns
$\overline{PROG}$ Pulse Width	t_{PP}	7/10 t_{CY} −250	800			ns
Port 2 I/O Setup to ALE	t_{PL}	4/15 t_{CY} −200	200			ns
Port 2 I/O Hold to ALE	t_{LP}	1/10 t_{CY} −100	50			ns
Port Output from ALE	t_{PV}	3/10 t_{CY} +100			850	ns
Cycle Time	t_{CY}	6 MHz	1.5		15.0	μs
TO Rep Rate	t_{OPRR}	3/15 t_{CY}	500			ns

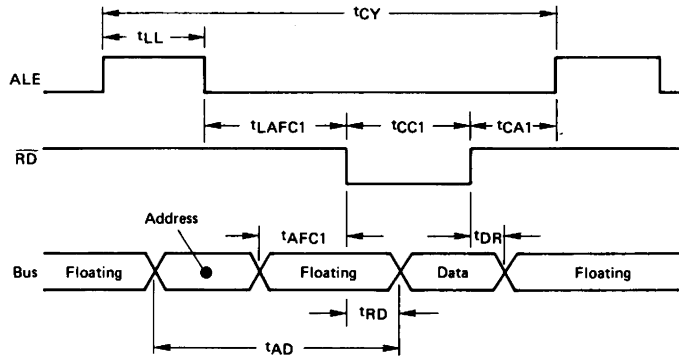
Notes: Output Outputs CL = 80pF
BUS Outputs CL = 150pF
BUS High Impedance Load 20pF

TIMING WAFEFORMS

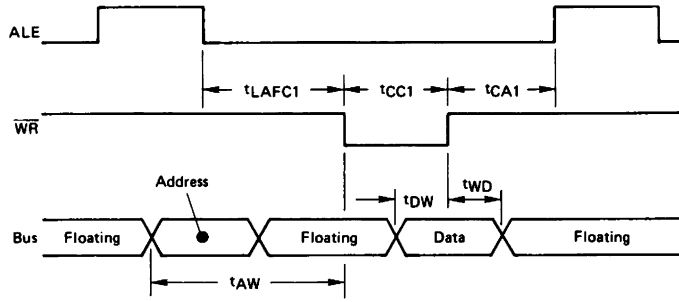
Instruction Fetch from External Memory



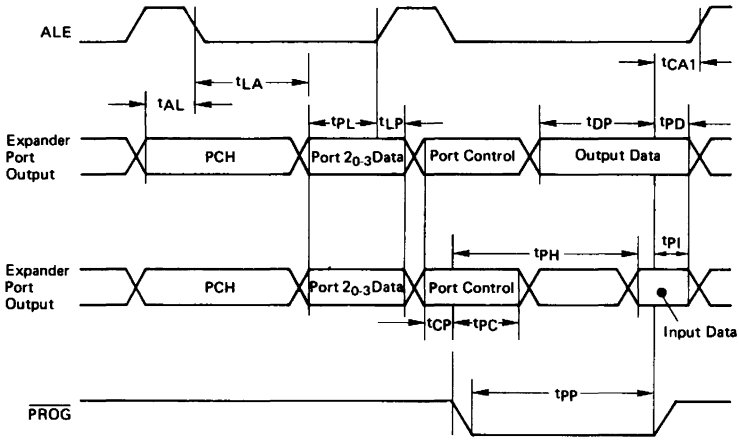
Read from External Data Memory



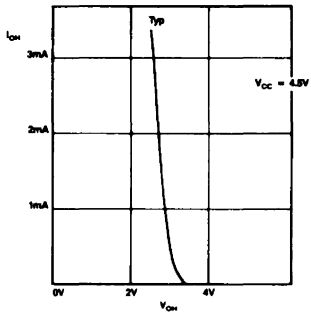
Write to External Memory



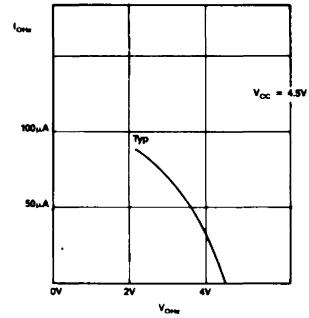
Port 2 Timing



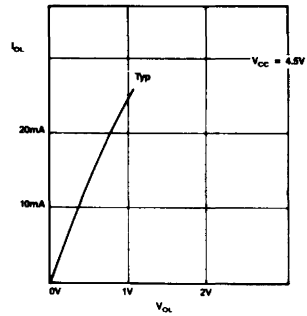
BUS Output High Voltage vs. Source Current



Port P1 and P2 Output
High Voltage vs. Source Current

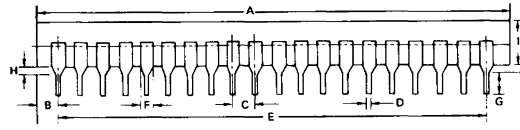


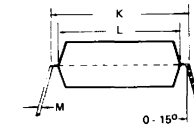
BUS Output Low Voltage vs. Sink Current



40 PIN PLASTIC
μPD8049HC/
μPD8039HLC/
μPD8749HC

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62 MAX	0.064 MAX
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.5 MIN	0.06 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24 TYP	0.600 TYP
L	13.2 TYP	0.520 TYP
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



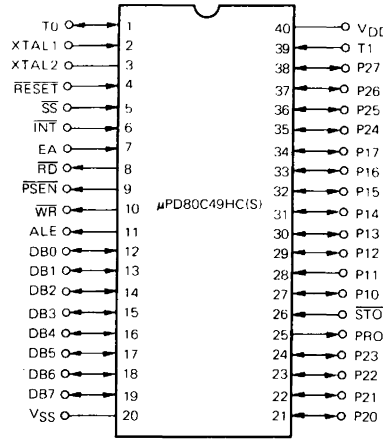


The μPD80C49H is a single chip 8-bit microcomputer having 8-bit parallel processing ALU, ROM, RAM, I/O ports and control circuit on one CMOS chip. This microcomputer is provided with a standby function with consideration for low power consumption

FEATURES

- Extended temperature (T_a = −40 to +110 °C)
- Single chip 8-bit microcomputer
- 98 types of instructions
- Instruction cycle, 1.5 μs/10 MHz
- Operating function
  - Addition, logic operation, and decimal adjust
- ROM 2 K x 8 bits
- RAM 128 x 8 bits
- Stand-by function
- 8-level stack
- Dual Register Banks
- Interrupt capability
- Two test inputs
- On-chip 8 bit Timer/Counters
- Easily expandable Memory and I/O ports
- 27 lines Input/output ports
  - Input/output ports, 8 bits x 2
  - Data bus (common to I/O ports), 8 bits x 1
  - Sense Input (T0, T1, $\overline{INT}$) 1 bits x 3
- Single step function
- On chip Clock oscillator circuit
- CMOS
- Single power supply, +2.5 to +6.0 V
- 40 pin plastic DIP
- μPD8049H pin compatible

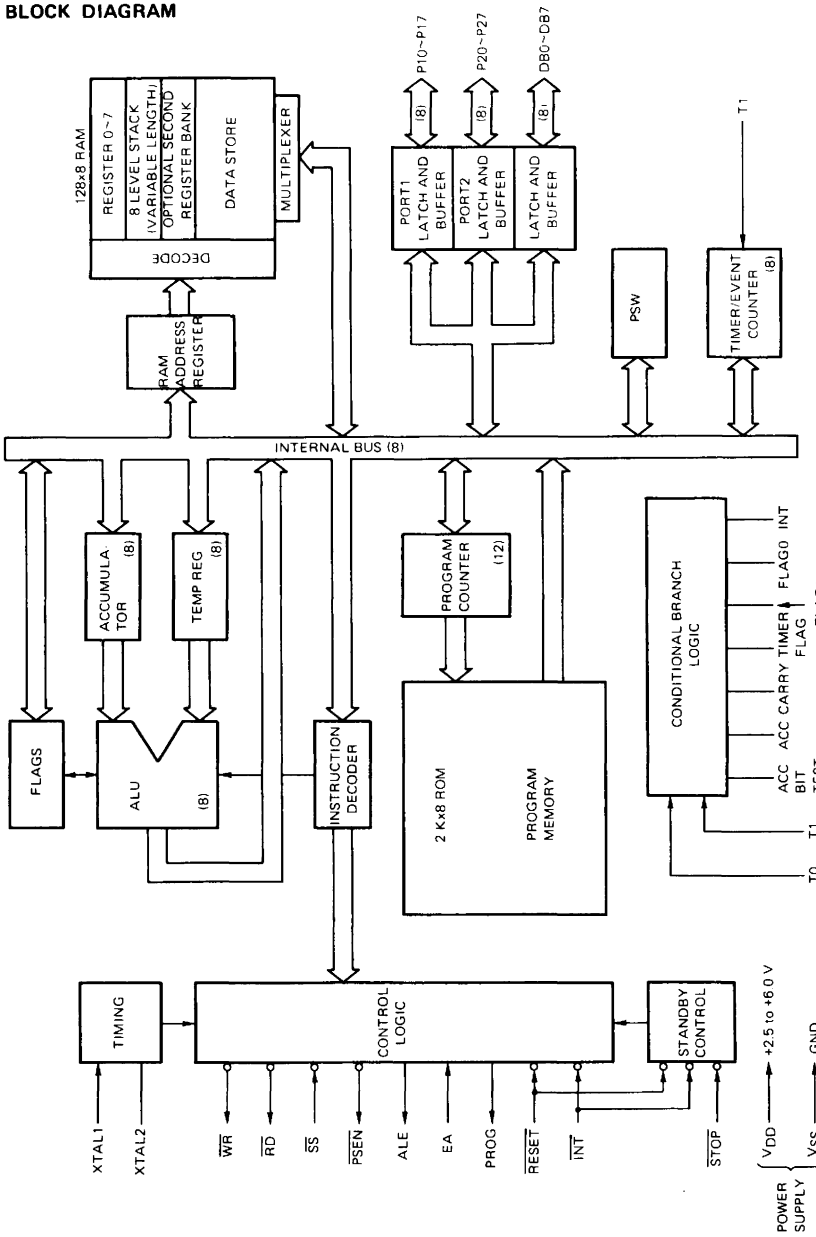
PIN CONFIGURATION (Top View)



PIN FUNCTION

P10 ~ P17	:	Input/output port (PORT 1)
P20 ~ P27	:	Input/output port (PORT 2)
DB0 ~ DB7	:	Data bus (BUS PORT)
T0, T1	:	Test Input
$\overline{INT}$	:	Interrupt Input
$\overline{RD}$	:	Data Read Strobe Output
$\overline{WR}$	:	Data Write Strobe Output
ALE	:	Address Latch Enable Output
$\overline{PSEN}$	:	Program Strobe Enable Strobe Output
$\overline{RESET}$	:	Reset Input
$\overline{SS}$	:	Single step Input
EA	:	External Access Input
XTAL 1, 2	:	Crystal
$\overline{STOP}$	:	Stop Input

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	−0.3 to +7	V
Input Voltage	V_I	−0.3 to V_{DD}+0.3	V
Output Voltage	V_O	−0.3 to V_{DD}+0.3	V
Operating Temperature	T_{opt}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +110	°C

DC CHARACTERISTICS (T_a = −40 °C to +110 °C, V_{DD} = +5 V ± 10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage Low	V_{IL}		−0.3		+0.8	V
Input Voltage High	V_{IH}	Except XTAL1, XTAL2, $\overline{RESET}$, $\overline{SS}$	V_{DD}−2		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$	V_{DD}−1		V_{DD}	V
Output Voltage Low	V_{OL}	I_{OL}=1.2 mA			+0.45	V
Output Voltage High	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0 I_{OH}=−250 μA	2.4			V
	V_{OH1}(1)	I_{OH}=−3 μA (Type 0) PORT1, PORT2	2.4			V
		I_{OH}=−30 μA (Type 1) PORT1, PORT2	2.4			V
	V_{OH2}	All Outputs, I_{OH}=−0.2 μA	V_{DD}−0.5			V
Input Current	I_{ILP}(1)	PORT1, PORT2; $V_I \leq V_{IL}$ (Type 0)		−15	−40	μA
		PORT1, PORT2; $V_I \leq V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leq V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leq V_I \leq V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leq V_I \leq V_{DD}$			±3	μA
Output Leakage Current	I_{LO}	$V_{SS} \leq V_O \leq V_{DD}$ High Impedance, BUS, T0 (3)			±1	μA
Standby Current	I_{DD1}	HALT Mode; t_{CY}=1.5 μs		1.5	3.0	mA
	I_{DD2}	STOP Mode (2)		1	50	μA
Supply Current (Total)	I_{DD}	t_{CY}=1.5 μs		6	15	mA
Data Retention Voltage	V_{DDDR}	at the hardware STOP mode ($\overline{STOP}$, $\overline{RESET}$ ≤ 0.4 V) or RESET ($\overline{RESET}$ ≤ 0.4 V)	2.5			V

DC CHARACTERISTICS (T_a = −40 °C to +110 °C, V_{DD} = +2.5 V to +6.0 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Voltage Low	V_{IL}			−0.3		0.18 V_{DD}	V
Input Voltage High	V_{IH}	Except XTAL1, XTAL2, $\overline{RESET}$, $\overline{SS}$		0.7 V_{DD}		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$		0.8 V_{DD}		V_{DD}	V
Output Voltage Low	V_{OL}	I_{OL}=0.5 mA				0.45	V
Output Voltage High	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0 I_{OH}=50 μA		0.75 V_{DD}			V
	V_{OH1}(1)	I_{OH}=−0.5 μA (Type 0) PORT1, PORT2		0.7 V_{DD}			V
		I_{OH}=−5 μA (Type 1) PORT1, PORT2		0.7 V_{DD}			V
Input Current	I_{LIP}(1)	PORT1, PORT2; $V_I \leq V_{IL}$ (Type 0)			−15	−40	μA
		PORT1, PORT2; $V_I \leq V_{IL}$ (Type 1)				−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leq V_{IL}$				−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leq V_I \leq V_{DD}$				±1	μA
	I_{LI2}	EA; $V_{SS} \leq V_I \leq V_{DD}$				±5	μA
Output Leakage Current	I_{LO}	$V_{SS} \leq V_O \leq V_{DD}$ (3) High Impedance, BUS, T0				±1	μA
Stand-by Current	I_{DD1}	HALT Mode	V_{DD}=3 V; t_{CY}=6 μs		0.3	0.6	mA
			V_{DD}=6 V; t_{CY}=1.5 μs		2.0	4.0	mA
	I_{DD2}	STOP Mode (2)	V_{DD}=3 V		1	50	μA
			V_{DD}=6 V		1	100	μA
Supply Current	I_{DD}	V_{DD}=3 V; t_{CY}=6 μs			2.0	4.0	mA
		V_{DD}=6 V; t_{CY}=1.5 μs			10	20	mA

Note 1: Option specification of type 0 and type 1 is available only for the μPD80C49H.

Note 2: The input pin voltage is $V_I \leq V_{IL}$ or $V_I \leq V_{IH}$.

Note 3: Output pins PORT1 and PORT2 specified as option in the type 2 are also included.

AC CHARACTERISTICS (T_a = 40 to 110 °C, V_{SS} = 0 V)

PARAMETER	SYMBOL	CONDITIONS	V_{DD}=+5 V±10 %		V_{DD}=2.5 to 6.0 V		UNIT
			MIN.	MAX.	MIN.	MAX.	
Cycle Time	t_{CY}		1.5		6		μs
ALE Pulse Width	t_{LL}		180		1230		ns
Address Setup before ALE	t_{AL}		190		1090		ns
Address Hold from ALE	t_{LA}	(4)	60		360		ns
Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}		550		2 800		ns
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}		400		2 200		ns
Data Setup before $\overline{WR}$	t_{DW}		450		2 400		ns
Data Hold after $\overline{WR}$	t_{WD}	(5)	60		360		ns
Data Hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}		0	120	0	400	ns
$\overline{RD}$ to Data in	t_{RD1}			400		2 200	ns
$\overline{PSEN}$ to Data in	t_{RD2}			250		1 600	ns
Address Setup before $\overline{WR}$	t_{AW}		450		2 250		ns
Address Setup before Data in ($\overline{RD}$)	t_{AD1}			900		4 350	ns
Address Setup before Data in ($\overline{PSEN}$)	t_{AD2}	(4)		650		3 350	ns
Address Float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}		135		735		ns
Address Float to $\overline{PSEN}$	t_{AFC2}		10		160		ns
ALE to Control Signal ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}		125		1 125		ns
ALE to Control Signal ($\overline{PSEN}$)	t_{LAFC2}		75		525		ns
Control Signal ($\overline{RD}$, $\overline{WR}$, PROG) to ALE	t_{CA1}		50		350		ns
Control Signal ($\overline{PSEN}$) to ALE	t_{CA2}		350		1 550		ns
Port Control Setup before Falling Edge of PROG	t_{CP}	(6)	110		560		ns
Port Control Hold after Falling Edge of PROG	t_{PC1}	(6) (7)	0	85	0	220	ns
	t_{PC2}	(6) (8)	220		1 400		ns
PROG to Time P2 Input must be Valid	t_{PR}			730		3 280	ns
Input Data Hold Time	t_{PF}		0	150	0	600	ns
Output Data Setup Time	t_{DP}		450		2 250		ns
Output Data Hold Time	t_{PD}		100		550		ns
PROG Pulse Width	t_{PP}	(6)	800		3 950		ns
PORT2 I/O Data Setup Time	t_{PL}		200		1 400		ns
PORT2 I/O Data Hold Time	t_{LP}		10		160		ns
ALE to PORT Output	t_{PV}			550		1 900	ns
T0 Clock Period	t_{OPRR}		300		1 200		ns

Note 4. Control Output: C_L = 80 pF, BUS Output: C_L = 150 pF

Note 5. C_L = 20 pF

Note 6. Control output: C_L = 80 pF

Note 7. At execution of MOVD A, P_p instruction

Note 8. At execution of MOVD P_p, A; ORLD P_p, A instruction

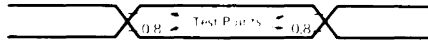
DEFINITION OF t_{CY} DEPENDENT BUS TIMING

PARAMETER	CALCULATION FORMULA	MIN./MAX.	UNIT
t_{LL}	(7/30) T-170	MIN.	ns
t_{AL}	(1/5) T-110	MIN.	ns
t_{LA}	(1/15) T-40	MIN.	ns
t_{CC1}	(1/2) T-200	MIN.	ns
t_{CC2}	(2/5) T-200	MIN.	ns
t_{DW}	(13/30) T-200	MIN.	ns
t_{WD}	(1/15) T-40	MIN.	ns
t_{DR}	(1/10) T-30	MAX.	ns
t_{RD1}	(2/5) T-200	MAX.	ns
t_{RD2}	(3/10) T-200	MAX.	ns
t_{AW}	(2/5) T-150	MIN.	ns
t_{AD1}	(23/30) T-250	MAX.	ns
t_{AD2}	(3/5) T-250	MAX.	ns
t_{AFC1}	(2/15) T-65	MIN.	ns
t_{AFC2}	(1/30) T-40	MIN.	ns
t_{LAFC1}	(1/5) T-75	MIN.	ns
t_{LAFC2}	(1/10) T-75	MIN.	ns
t_{CA1}	(1/15) T-50	MIN.	ns
t_{CA2}	(4/15) T-50	MIN.	ns
t_{CP}	(1/10) T-40	MIN.	ns
t_{PC2}	(4/15) T-200	MIN.	ns
t_{PR}	(17/30) T-120	MAX.	ns
t_{PF}	(1/10) T	MAX.	ns
t_{DP}	(2/5) T-150	MIN.	ns
t_{PD}	(1/10) T-50	MIN.	ns
t_{PP}	(7/10) T-250	MIN.	ns
t_{PL}	(4/15) T-200	MIN.	ns
t_{LP}	(1/30) T-40	MIN.	ns
t_{PV}	(3/10) T+100	MAX.	ns
t_{OPRR}	(1/5) T	MIN.	ns
t_{CY}	$(1/f_{XTAL}) \times 15$		μs

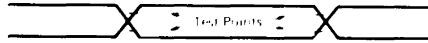
Remarks : $T = t_{CY}$

AC Test Input/Output Waveform

(1) V_{DD} = 5.0 V ± 10%

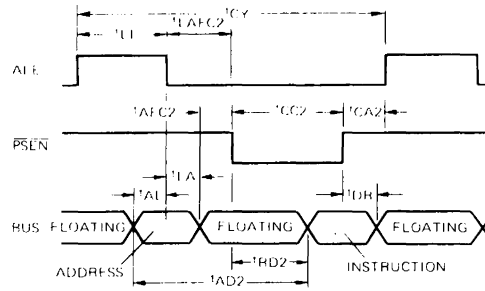


(2) V_{DD} = 2.5 V to 6.0 V

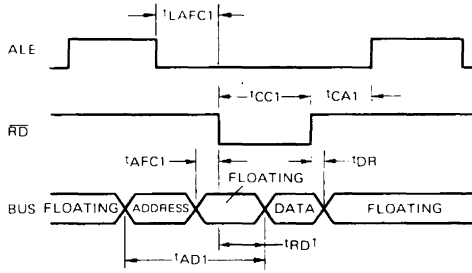


TIMING WAVEFORMS

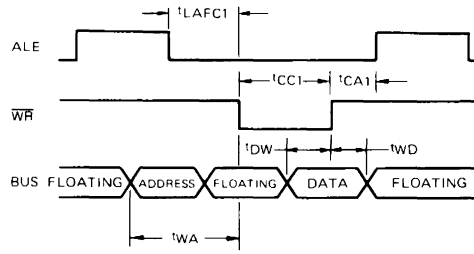
INSTRUCTION FETCH (External Program Memory)



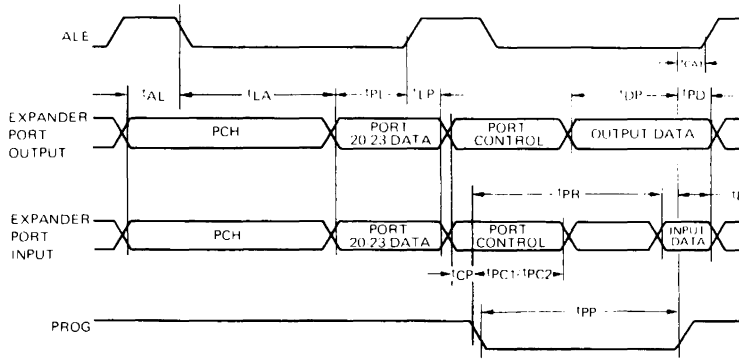
READ (External Data Memory)



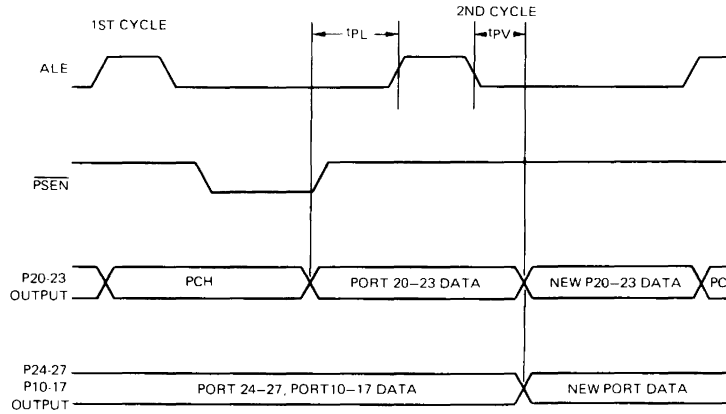
WRITE (External Data Memory)



PORT 2 EXPANSION TIMING



I/O PORT TIMING



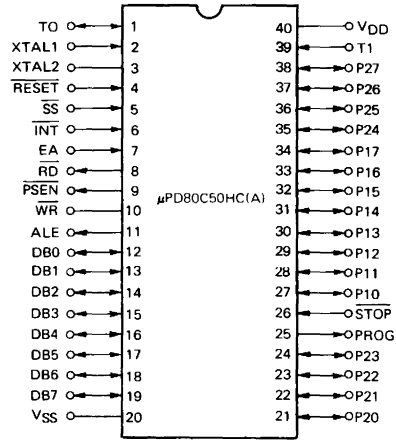
The μPD80C50HC(A) is a single chip microcomputer containing 8-bit CPU, ROM, RAM, I/O ports and control circuit on one CMOS chip.

The μPD80C50HC(A), fabricated by CMOS technology, realizes low power consumption and data retention is also available with less power consumption.

FEATURES

- Single chip 8-bit microcomputer
- 98 instructions
- Instruction cycle: 1.25 μs/12 MHz
- Operating function
  Addition, logic operation, and decimal adjust
- ROM 4 K x 8 bits
- RAM 256 x 8 bits
- Stand-by function
- 8-level stack
- Two sets of working registers
- Interrupt capability
- Two test inputs
- Internal Timer/Event Counter
- Easy expandable Memory and I/O ports
- Input/output ports
  Input/output ports: 8 bits x 2
  Data bus (alternative for I/O ports): 8 bits x 1
- Single step function
- Internal Clock generator
- CMOS
- Single power supply: +2.5 to+6.0 V
- 40 pin plastic DIP

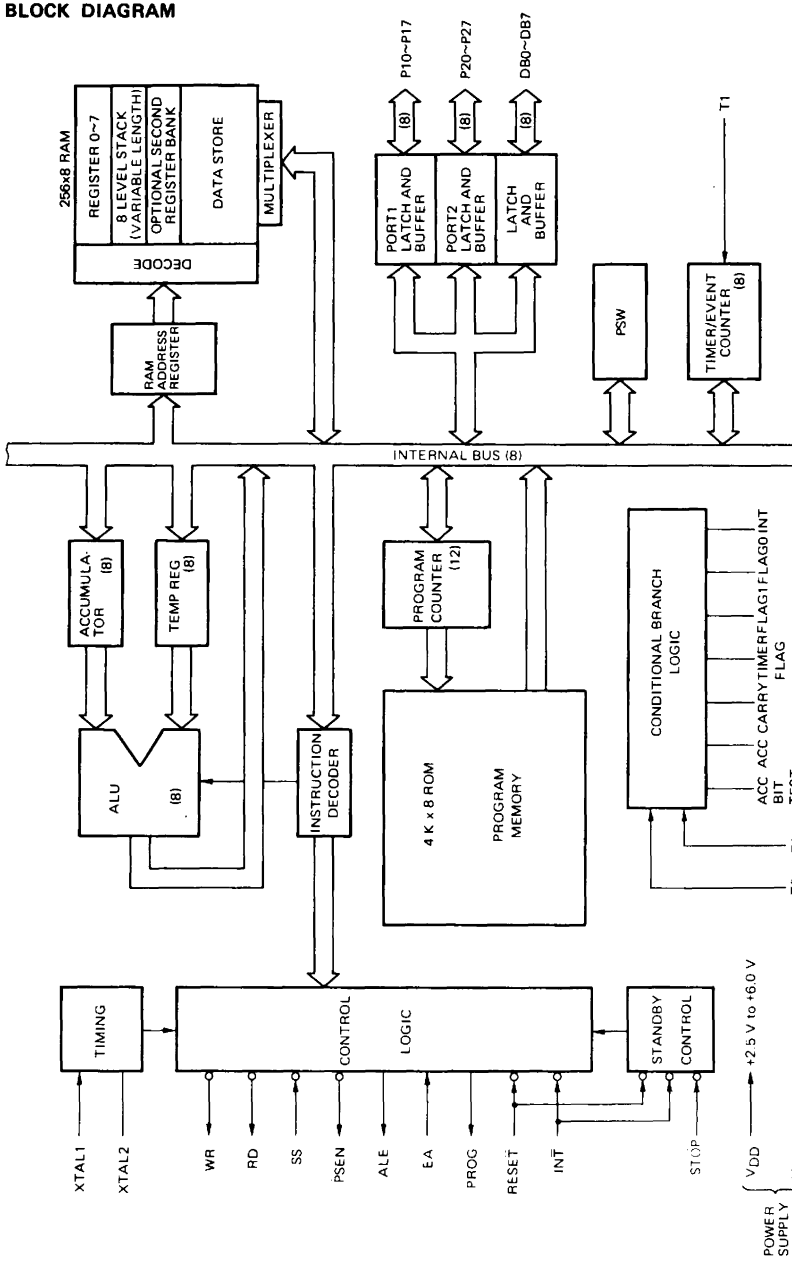
PIN CONNECTION (Top View)



PIN IDENTIFICATIONS

P10~P17	:	Input/output port (PORT 1)
P20~P27	:	Input/output port (PORT 2)
DB0~DB7	:	Data bus (BUS)
T0, T1	:	Test
$\overline{INT}$	:	Interrupt
$\overline{RD}$	:	Read
$\overline{WR}$	:	Write
ALE	:	Address Latch Enable
$\overline{PSEN}$	:	Program Store Enable
$\overline{RESET}$	:	Reset
$\overline{SS}$	:	Single step
EA	:	External Access
XTAL1, 2	:	Crystal
$\overline{STOP}$	:	Stop

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V_{DD}	V_{SS} −0.3 to +7	V
Input Voltage	V_I	V_{SS} −0.3 to V_{DD} +0.3	V
Output Voltage	V_O	V_{SS} −0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input low voltage	V_{IL}		−0.3		0.8	V
Input high voltage	V_{IH}	(All except XTAL1, XTAL2, $\overline{RESET}$ $\overline{SS}$)	V_{DD}−2		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$	V_{DD}−1		V_{DD}	V
Output low voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output high voltage	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, LAE, PROG, T0; I_{OH} = −400 μA	2.4			V
	V_{OH1}	PORT1, PORT2; I_{OH} = −5 μA (Type 0)	2.4			V
		PORT1, PORT2; I_{OH} = 50 μA (Type 1)	2.4			V
	V_{OH2}	All outputs; I_{OH} = −0.2 μA	V_{DD}−0.5			V
Input current	I_{ILP}	PORT1, PORT2; $V_I \leqq V_{IL}$ (Type 0)		−15	−40	μA
		PORT1, PORT2; $V_I \leqq V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqq V_{IL}$			−40	μA
Input leakage current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leqq V_I \leqq V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqq V_I \leqq V_{DD}$			±3	μA
Output leakage current	I_{LO}	BUS, T0, High impedance state (2) $V_{SS} \leqq V_O \leqq V_{DD}$			±1	μA
Standby current	I_{DD1}	HALT mode; t_{CY} = 1.25 μs		1.5	3.0	mA
	I_{DD2}	STOP mode (1)		1	20	μA
Supply current	I_{DD}	t_{CY} = 1.25 μs		6	18	mA
Data holding voltage	V_{DDDR}	Hardware STOP mode ($\overline{STOP}$, $\overline{RESET}$ ≦ 0.4 V) or reset ($\overline{RESET}$ ≦ 0.4 V)	2.0			V

Notes:

1) Input pin voltage $V_I \leqq V_{IL}$ or $V_I \geqq V_{IH}$
2) Includes PORT1 and PORT2 pins optionally specified with type 2.

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = +2.5 V to +6.0 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input low voltage	V_{IL}			−0.3		0.18 V_{DD}	V
Input high voltage	V_{IH}	(All except XTAL1, XTAL2, $\overline{RESET}$, SS)		0.7 V_{DD}		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, SS		0.8 V_{DD}		V_{DD}	V
Input low voltage	V_{OL}	I_{OL} = 1.0 mA				0.45	V
Output high voltage	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −100 μA		0.75 V_{DD}			V
	V_{OH1}	PORT1, PORT2: I_{OH} = −1 μA (Type 0)		0.7 V_{DD}			V
		PORT1, PORT2: I_{OH} = −10 μA (Type 1)		0.7 V_{DD}			V
Input current	I_{ILP}	PORT1, PORT2: $V_I \leqq V_{IL}$ (Type 0)			−15	−40	μA
		PORT1, PORT2: $V_I \leqq V_{IL}$ (Type 1)				−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqq V_{IL}$				−40	μA
Input leakage current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leqq V_I \leqq V_{DD}$				±1	μA
	I_{LI2}	EA; $V_{SS} \leqq V_I \leqq V_{DD}$				±5	μA
Output leakage current	I_{LO}	BUS, T0 High impedance state (3) $V_{SS} \leqq V_O \leqq V_{DD}$				±1	μA
Standby current	I_{DD1}	HALT mode	V_{DD} = 3 V; t_{CY} = 5 μs		0.3	0.6	mA
			V_{DD} = 6 V; t_{CY} = 1.25 μs		2.0	4.0	mA
	I_{DD2}	STOP mode (2)	V_{DD} = 3 V		1	20	μA
			V_{DD} = 6 V		1	50	μA
Supply current	I_{DD}	V_{DD} = 3 V; t_{CY} = 5 μs			2.0	5.0	mA
		V_{DD} = 6 V; t_{CY} = 1.25 μs			10	25	mA

Notes:

1) Type 0, type 1 and type 2 options can be specified in μPD80C50H
2) Input pin voltage $V_I \leqq V_{IL}$ or $V_I \geqq V_{IH}$
3) Includes PORT1 and PORT2 pins optionally specified with type 2.

AC CHARACTERISTICS (T_a = −40 to + 85 ° C, V_{SS} = 0 V)

PARAMETER	SYMBOL	CONDITIONS	V_{DD}=+5 V ±10 %		V_{DD}=+2.5 to +6.0 V		UNIT
			MIN.	MAX.	MIN.	MAX.	
Cycle time	t_{CY}		1.25	150	5	150	μs
ALE pulse width	t_{LL}		125		995		ns
Address setup to ALE	t_{AL}		140		890		ns
Address hold from ALE	t_{LA}	(4)	45		295		ns
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}		425		2 300		ns
Control pulse width ($\overline{PSEN}$)	t_{CC2}		300		1 800		ns
Data setup before $\overline{WR}$	t_{DW}		340		1 965		ns
Data hold after $\overline{WR}$	t_{WD}	(5)	45		295		ns
Data hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}		0	95	0	470	ns
$\overline{RD}$ to data in	t_{RD1}			300		1 800	ns
$\overline{PSEN}$ to data in	t_{RD2}			175		1 300	ns
Address setup to $\overline{WR}$	t_{AW}		350		1 850		ns
Address setup to $\overline{RD}$ data in	t_{AD1}			700		3 585	ns
Address setup to $\overline{PSEN}$ data in	t_{AD2}	(4)		500		2 750	ns
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}		105		600		ns
Address float to $\overline{PSEN}$	t_{AFC2}		5		125		ns
ALE to $\overline{RD}$, $\overline{WR}$ delay	t_{LAFC1}		175		925		ns
ALE to $\overline{PSEN}$ delay	t_{LAFC2}		50		425		ns
$\overline{RD}$, $\overline{WR}$, PROG to ALE delay	t_{CA1}		35		285		ns
$\overline{PSEN}$ to ALE delay	t_{CA2}		280		1 285		ns
Port control setup to PROG	t_{CP}	(6)	85		460		ns
Port control hold from PROG	t_{PC1}	(6) (7)	0	80	0	200 (9)	ns
	t_{PC2}	(6) (8)	135		1 135		ns
Input data setup to PROG	t_{PR}	(6)		585		2 715	ns
Input data hold from PROG	t_{PF}		0	125	0	500	ns
Output data setup to PROG	t_{DP}		350		1 850		ns
Output data hold from PROG	t_{PD}		75		450		ns
PROG pulse width	t_{PP}	(6)	625		3 250		ns
Port 2 I/O data setup to ALE	t_{PL}		135		1 135		ns
Port 2 I/O data hold from ALE	t_{LP}		5		125		ns
ALE to port output	t_{PV}			475		1 600	ns
T0 output cycle time	t_{0PRR}		250		1 000		ns

Notes:

4) Control outputs C_L = 80 pF; BUS output: C_L = 150 pF

5) C_L = 20 pF

6) Control outputs: C_L = 80 pF

7) During execution of MOVD A, P_P

8) During execution of MOVD P_P, A, ANLD P_P, A, ORLD P_P, A

9) See supply voltage and port control hold time characteristic curves

t_{CY}-DEPENDENT BUS TIMING DEFINITIONS

PARAMETER	CALCULATION FORMULA	MIN./MAX.	UNIT
t_{LL}	(7/30) T−170	MIN.	ns
t_{AL}	(1/5) T−110	MIN.	ns
t_{LA}	(1/15) T−40	MIN.	ns
t_{CC1}	(1/2) T−200	MIN.	ns
t_{CC2}	(2/5) T−200	MIN.	ns
t_{DW}	(13/30) T−200	MIN.	ns
t_{WD}	(1/15) T−40	MIN.	ns
t_{DR}	(1/10) T−30	MAX.	ns
t_{RD1}	(2/5) T−200	MAX.	ns
t_{RD2}	(3/10) T−200	MAX.	ns
t_{AW}	(2/5) T−150	MIN.	ns
t_{AD1}	(23/30) T−250	MAX.	ns
t_{AD2}	(3/5) T−250	MAX.	ns
t_{AFC1}	(2/15) T−65	MIN.	ns
t_{AFC2}	(1/30) T−40	MIN.	ns
t_{LAFC1}	(1/5) T−75	MIN.	ns
t_{LAFC2}	(1/10) T−75	MIN.	ns
t_{CA1}	(1/15) T−50	MIN.	ns
t_{CA2}	(4/15) T−50	MIN.	ns
t_{CP}	(1/10) T−40	MIN.	ns
t_{PC2}	(4/15) T−200	MIN.	ns
t_{PR}	(17/30) T−120	MAX.	ns
t_{PF}	(1/10) T	MAX.	ns
t_{DP}	(2/5) T−150	MIN.	ns
t_{PD}	(1/10) T−50	MIN.	ns
t_{PP}	(7/10) T−250	MIN.	ns
t_{PL}	(4/15) T−200	MIN.	ns
t_{LP}	(1/30) T−40	MIN.	ns
t_{PV}	(3/10) T+100	MAX.	ns
t_{0PRR}	(1/5) T	MIN.	ns
t_{CY}	$(1/f_{XTAL})\times 15$		μs

Remarks: $T = t_{CY}$

The μPD78C11 is a 8-bit single chip microcomputer with an A/D converter. In addition, 8-bit CPU, ROM, RAM, A/D converter, multifunctional timer/event counters, general-purpose serial interfaces and I/O ports are also integrated; and the μPD78C11 is capable of controlling external memory directly, or ROM and RAM, which can be expanded freely and accessed in the same manner like the built-in ROM and RAM.

The μPD78C10 is ROM-less version of μPD78C11.

The μPD78C11/10 is CMOS version of μPD7811/10. They are member of μCOM-87AD series.

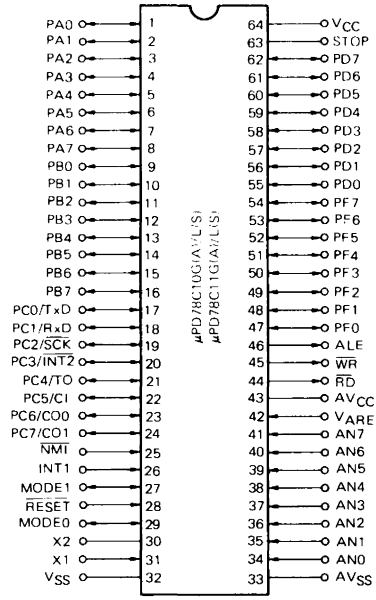
The instruction sets are compatible with the μCOM-87, and moreover involve the 16-bit data operation instructions and multiplication/division instructions to compose a program effectively.

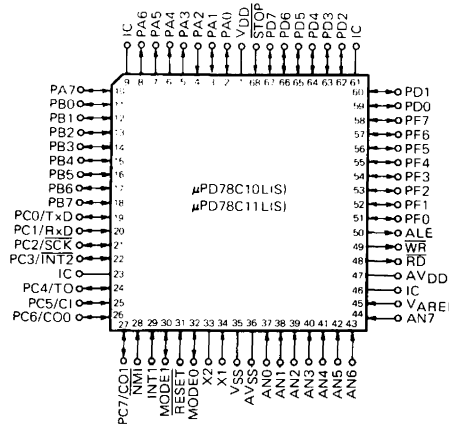
The μCOM-87AD is very suitable in the system control handling analog data, the energy control, process control and automobile, etc.

FEATURES

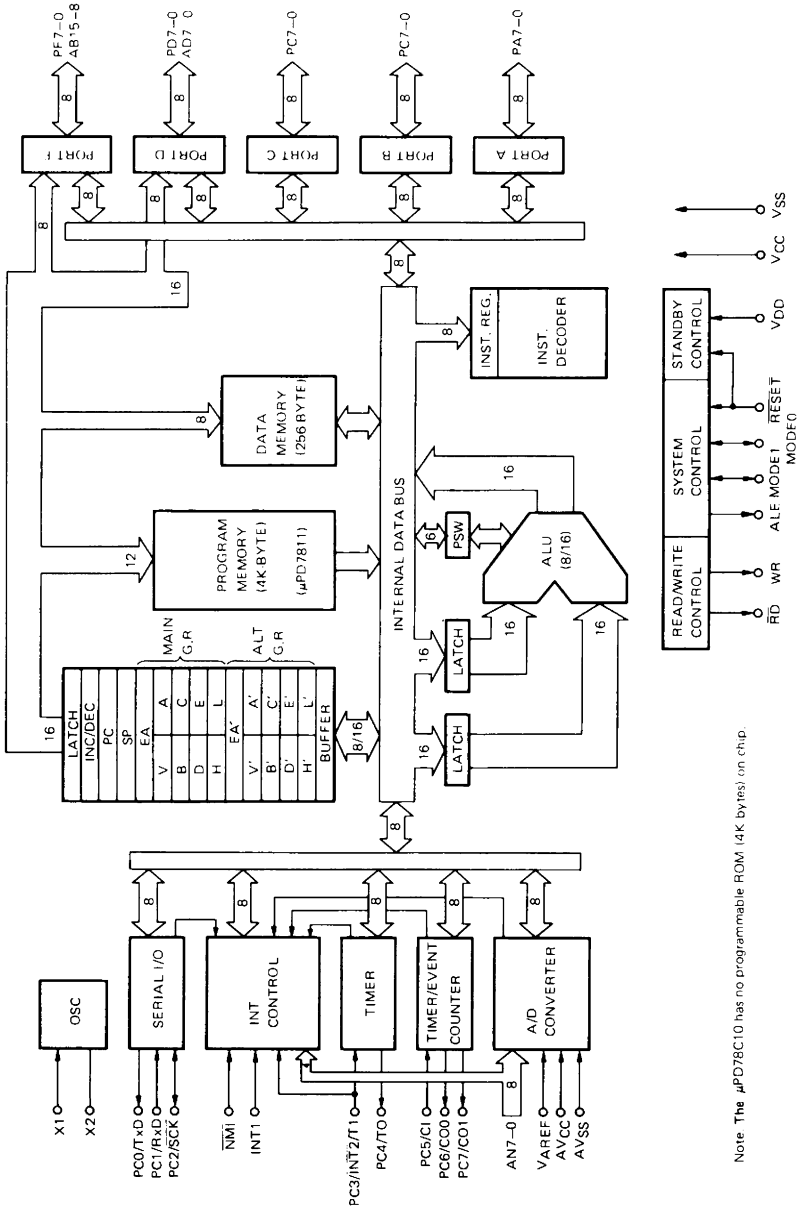
- Extended temperature: (T_a = −40 °C to +110 °C)
- Single chip microcomputer (μCOM-87 AD)
- 158 kinds of abundant instruction sets, μCOM-87 upward compatible, 16-bit operation instruction multiplication/division instruction
- Instruction cycle: 1 μs (12 MHz)
- Program (ROM) capacity: 4 096 words x 8 bits
- Data (RAM) capacity: 256 words x 8 bits
- Direct addressing memories (ROM/RAM) up to 64K bytes
- High-precision 8-bit A/D converter, 8 analog inputs
- General-purpose serial interface
  Asynchronous mode, synchronous mode & I/O interface mode
- Multifunctional 6-bit timer/event counter
- Two 8-bit timers
- Interrupt function (3 external & 8 internal)
- 6 priority levels and the corresponding interrupt address
- I/O ports:
  - 40 bits (μPD78C11G(S)/L(S))
  - 28 bits (μPD78C10G(S)/L(S))
- Edge-sense inputs: 4 inputs
- Zero-cross detection function
- Standby function: HALT mode, Hardware/software STOP mode
- Built-in clock oscillator
- CMOS
- Single power supply (+5 V)
- 64-pin plastic QUIP (μPD78C11G(S)/μPD78C10G(S))
  68-pin PLCC (μPD78C11L(S)/μPD78C10L(S))

PIN CONFIGURATION (Top View)





μPD78C10, μPD78C11 BLOCK DIAGRAM



Note The μPD78C10 has no programmable ROM (4K bytes) on chip.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM (T_a = 25 °C)

PARAMETER	SYMBOL	TEST CONDITION	RATINGS	UNIT
Power Supply Voltage	V_{DD}		−0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD}+0.5	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to V_{DD}+0.5	V
Output Voltage	V_O		−0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−2.0	mA
		All Output Pin Total	−50	mA
Reference Input Voltage	V_{AREF}		−0.5 to AV_{DD}+0.3	V
Operating Temperature	T_{OPT}	$f_{XTAL} \leq 12$ MHz	−40 to +110	°C
Storage Temperature	T_{STG}		−65 to +150	°C

OPERATING CONDITION

PARAMETER / OSC. FREQ.	T_a	V_{DD}, AV_{DD}
$f_{XTAL} \leq 12$ MHz	−40 to 110 °C	+5.0 V ±10 %

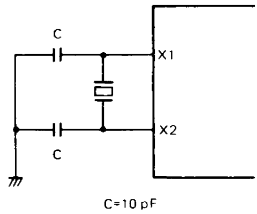
CAPACITANCE (T_a = 25 °C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_I	f_C = 1 MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins are			20	pF
I/O Capacitance	C_{IO}	connected to 0V			20	pF

DC CHARACTERISTICS (T_a = −40 to +110 °C, V_{DD} = +5.0 V ±10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Voltage Low	V_{IL1}	Except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7		0		0.7	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7		0		0.2 V_{DD}	V
Input Voltage High	V_{IH1}	Except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7, X1, X2		2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7, X1, X2 *1		0.8 V_{DD}		V_{DD}	V
Output Voltage Low	V_{OL}	I_{OL}=2.0 mA				0.45	V
Output Voltage High	V_{OH}	I_{OH}=−0.9 mA		V_{DD}−1.0			V
		I_{OH}=−100 μA		V_{DD}−0.5			V
Input Current	I_I	INT1, T1 (PC3); 0 V ≦ V_I ≦ V_{DD}				±200	μA
Input Leakage Current	I_{L1}	Except INT1, TI (PC3); 0 V ≦ V_I ≦ V_{DD}				±10	μA
Output Leakage Current	I_{LO}	0 V ≦ V_O ≦ V_{DD}				±10	μA
AV_{DD} Supply Current	AI_{DD1}				0.3	1.0	mA
	AI_{DD2}	STOP mode			10	20	μA
V_{DD} Supply Current	I_{DD1}	Operating mode f=12 MHz			12 *2	20	mA
	I_{DD2}	HALT mode f=12 MHz			5 *2	10	mA
Data Retention Voltage	V_{DDDR}	Hardware/software STOP mode		2.5			V
Data Retention Current	I_{DDDR}	Hardware/ software STOP mode	V_{DDDR}=2.5 V		1	15	μA
			V_{DDDR}=5 V±10 %		10	50	μA

*1 The following oscillation circuit using crystal is recommended.



C=10 pF

*2 T_a = +25 °C, V_{DD} = 5 V

AC CHARACTERISTICS

(T_a=−40 to +110 °C, V_{DD}=+5.0 V±10 %, V_{SS}=0 V, f_{XTAL}=12 MHz)

READ/WRITE OPERATION

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
X1 Input Cycle Time	t_{CYC}	*1	83	250	ns
Address Setup to ALE↓	t_{AL}	*2	65		ns
Address Hold from ALE↓	t_{LA}	*2	50		ns
Address to $\overline{RD}$↓ Delay Time	t_{AR}	*2	150		ns
$\overline{RD}$↓ to Address Floating	t_{AFR}	*2		20	ns
Address to Data Input	t_{AD}	*2		360	ns
ALE↓ to Data Input	t_{LDR}	*2		215	ns
$\overline{RD}$↓ to Data Input	t_{RD}	*2		180	ns
ALE↓ to $\overline{RD}$↓ Delay Time	t_{LR}	*2	35		ns
Data Hold Time from $\overline{RD}$↑	t_{RDH}	*2	0		ns
$\overline{RD}$↑ to ALE↑ Delay Time	t_{RL}	*2	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read, *2	280		ns
		OP Code Fetch, *2	530		ns
ALE Width High	t_{LL}	*2	125		ns
$\overline{M1}$ Setup Time to ALE↓	t_{ML}		65		ns
$\overline{M1}$ Hold Time from ALE↓	t_{LM}		50		ns
$\overline{IO}$/M Setup Time to ALE↓	t_{IL}		65		ns
$\overline{IO}$/M Hold Time from ALE↓	t_{LI}		50		ns
Address to $\overline{WR}$↓ Delay	t_{AW}	*2	150		ns
ALE↓ to Data Output	t_{LDW}	*2		195	ns
$\overline{WR}$↓ to Data Output	t_{WD}	*2		100	ns
ALE↓ to $\overline{WR}$↓ Delay	t_{LW}	*2	35		ns
Data Setup Time to $\overline{WR}$↑	t_{DW}	*2	230		ns
Data Hold Time from $\overline{WR}$↑	t_{WDH}	*2	95		ns
$\overline{WR}$↑ to ALE↑ Delay Time	t_{WL}	*2	115		ns
$\overline{WR}$ Width Low	t_{WW}	*2	280		ns

*1 Cycle time $t_{CYC} = 1/f_{XTAL}$

*2 Load capacitance: C_L = 100 pF

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*1	1		μs
			*2	500		ns
		$\overline{SCK}$ Output		2		ns
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*1	420		ns
			*2	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*1	420		ns
			*2	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$↑	t_{RXK}	*1		80		ns
RxD Hold Time from $\overline{SCK}$↑	t_{KRX}	*1		80		ns
$\overline{SCK}$↓ to TxD Delay Time	t_{KTX}	*1			210	ns

*1 1 x Baud rate in asynchronous, synchronous, I/O interface mode

*2 16 x, 64 x Baud rate in asynchronous

A/D CONVERTER CHARACTERISTICS

(T_a = −40 to +110 °C, V_{DD} = +5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V
V_{DD}−0.5 V ≦ AV_{DD} ≦ V_{DD}, 4.0 V ≦ V_{AREF} ≦ AV_{DD})

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Resolution			8			Bits
Absolute Accuracy		T_a=−10 to +70 °C, 83 ns ≦ t_{CYC} ≦ 170 ns			0.4 %±1/2	LSB
		83 ns ≦ t_{CYC} ≦ 170 ns, T_a=−40 to +85 °C			0.6 %±1/2	LSB
		3.4 V ≦ V_{AREF} ≦ AV_{DD}, 83 ns ≦ t_{CYC} ≦ 170 ns			0.8 %±1/2	LSB
Conversion Time	t_{CONV}	83 ns ≦ t_{CYC} ≦ 110 ns	576			t_{CYC}
		110 ns ≦ t_{CYC} ≦ 170 ns	432			t_{CYC}
Sampling Time	t_{SAMP}	83 ns ≦ t_{CYC} ≦ 110 ns	96			t_{CYC}
		110 ns ≦ t_{CYC} ≦ 170 ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1 000		MΩ
Reference Voltage	V_{AREF}		AV_{CC}−0.5		AV_{CC}	V
V_{AREF} Current	I_{AREF1}			1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} Current	I_{AVDD1}					
	I_{AVDD2}	STOP mode			1	μA
		V_{IAN} = V_{AREF}	255	255	255	Bit
		V_{IAN} = V_{ASS}	0	0	0	Bit
						Bit

ZERO-CROSS CHARACTERISTICS

(T_a=−40 to +110 °C, V_{CC}=+5.0 V±10 % V_{SS}=0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		±135	mV
ZERO-Cross Detection Input Frequency	f_{ZX}		0.05	1	kHz

OTHER OPERATIONS

(T_a=−40 °C to +110 °C, V_{CC}=+5.0 V±10 %, V_{SS}=0 V)

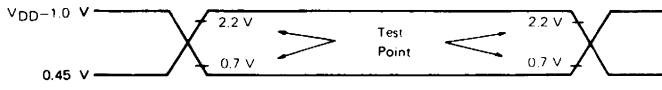
PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
TI Width High, Low	t_{TIH},t_{TIL}		6		t_{CYC}
CI Width High, Low	t_{CI1H},t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H},t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ Width High, Low	t_{NIH},t_{NIL}		10		t_{CYC}
INT1 Width High, Low	t_{I1H},t_{I1L}		36		t_{CYC}
INT2 Width High, Low	t_{I2H},t_{I2L}		36		t_{CYC}
RESET Width High, Low	t_{RSH},t_{RSL}		10		t_{CYC}

EXTERNAL CLOCK TIMING

(T_a=−40 °C to +110 °C, V_{DD}=+5.0 V±10 %, V_{SS}=0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
X1 Input Width High	$t_{\phi H}$		30	250	ns
X1 Input Width Low	$t_{\phi L}$		30	250	ns
X1 Input Rise Time	t_r		0	30	ns
X1 Input Fall Time	t_f		0	30	ns

AC TIMING MESURMENT POINT



BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNIT
t_{AL}	2T − 100	MIN.	ns
t_{LA}	T − 30	MIN.	ns
t_{AR}	3T − 100	MIN.	ns
t_{AD}	7T − 220	MAX.	ns
t_{LDR}	5T − 200	MAX.	ns
t_{RD}	4T − 150	MAX.	ns
t_{LR}	T − 50	MIN.	ns
t_{RL}	2T − 50	MIN.	ns
t_{RR}	4T − 50 (Data Read)	MIN.	ns
	7T − 50 (OP Code Fetch)		
t_{LL}	2T − 40	MIN.	ns
t_{ML}(1)	2T − 100	MIN.	ns
t_{LM}(1)	T − 30	MIN.	ns
t_{IL}(2)	2T − 100	MIN.	ns
t_{LI}(2)	T − 30	MIN.	ns
t_{AW}	3T − 100	MIN.	ns
t_{LDW}	T + 110	MAX.	ns
t_{LW}	T − 50	MIN.	ns
t_{DW}	4T − 100	MIN.	ns
t_{WDH}	2T − 70	MIN.	ns
t_{WL}	2T − 50	MIN.	ns
t_{WW}	4T − 50	MIN.	ns
t_{CYK}	12T ($\overline{SCK}$ Input)(3)	MIN.	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	5T + 5($\overline{SCK}$ Input)(3)	MIN.	ns
	12T − 100 ($\overline{SCK}$ Output)		
t_{KKH}	5T + 5($\overline{SCK}$ Input)(3)	MIN.	ns
	12T − 100 ($\overline{SCK}$ Output)		

NOTE: (1) MODE0, MODE1 pins are connected to V_{CC} through R.

(2) MODE0, MODE1 pins are connected to V_{CC} thorugh R in μPD7810.

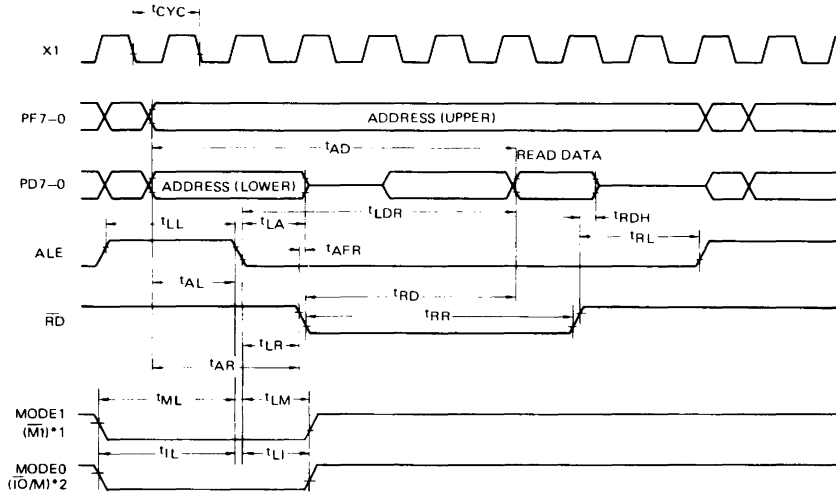
(3) 1x Baud Rate in Asynchronous, Synchronous, I/O interface Mode

(4) $T = t_{CYC} = 1/f_{XTAL}$

(5) The items out of this table are not dependent on f_{XTAL}.

TIMING WAVEFORM

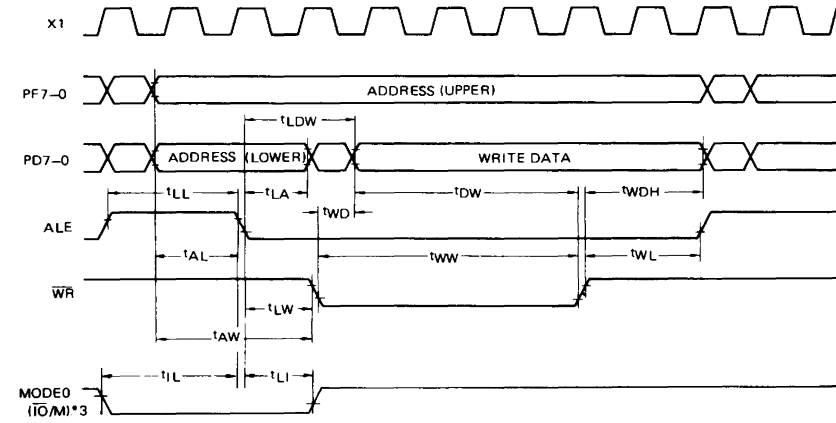
Read Operation



*1 $\overline{M_1}$ is output at the fetch cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

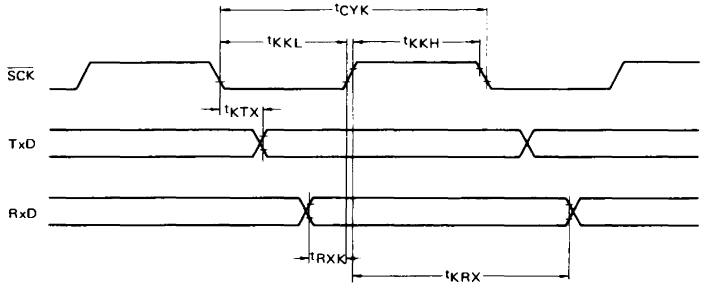
*2 $\overline{IO}$/M is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Write Operation

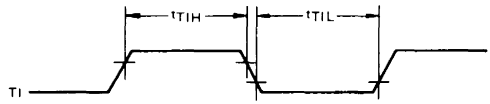


*3 $\overline{IO}$/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Serial Operation

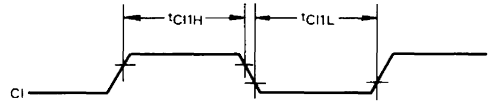


Timer Input Timing

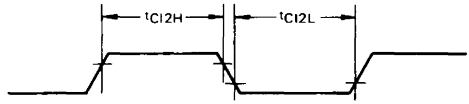


Timer/Event Counter Input Timing

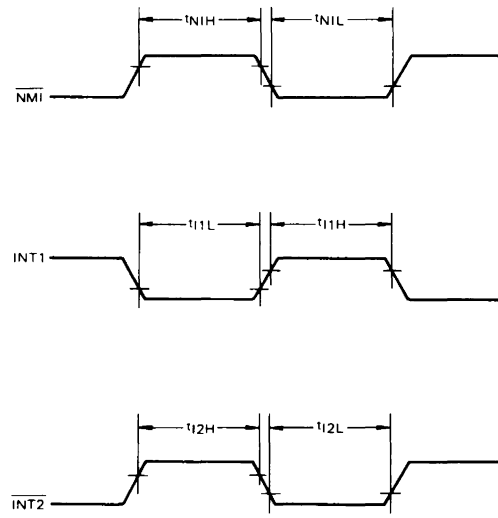
Event Count Mode:



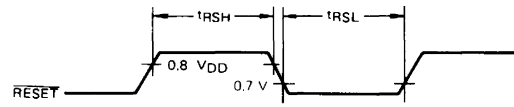
Pulse Width Measurement Mode:



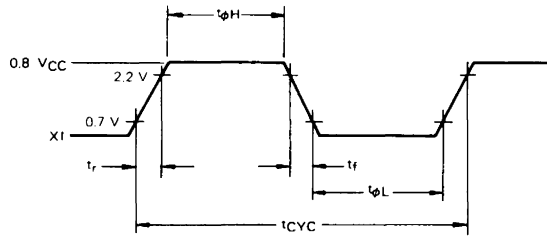
Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



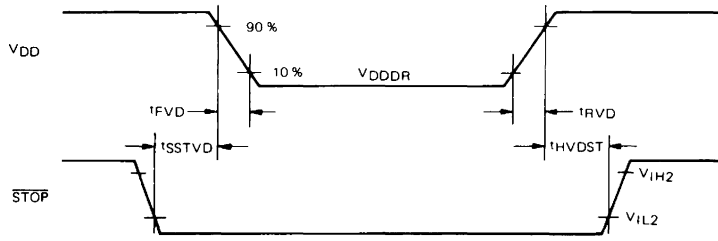
External Clock Timing



STOP MODE LOW VOLTAGE DATA RETENTION CHARACTERISTICS (T_a=−40 to +110 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	V_{DDDR}		2.5		5.5	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR}=2.5 V		1	15	μA
		V_{DDDR}=5 V ±10 %		15	50	μA
V_{DD} Rise and Fall Time	t_{RVD}, t_{FVD}		200			μs
$\overline{STOP}$ Setup Time to V_{DD}↓	t_{SSTVD}		12T+0.5			μs
$\overline{STOP}$ Hold Time after V_{DD}↑	t_{HVDST}		12T+0.5			μs

DATA RETENTION MODE TIMING



The μPD78C14 is a 1-chip 8-bit microcomputer with an A/D converter. In addition, 8-bit CPU, ROM, RAM, A/D converter, multifunctional timer/event counters, general-purpose serial interfaces and I/O ports are also integrated; and the μPD78C14 is capable of controlling external memory directly, or ROM and RAM, which can be expanded freely and accessed in the same manner like the built-in ROM and RAM.

The μPD78C14 is 16 k byte ROM version. They are member of μCOM-87AD series.

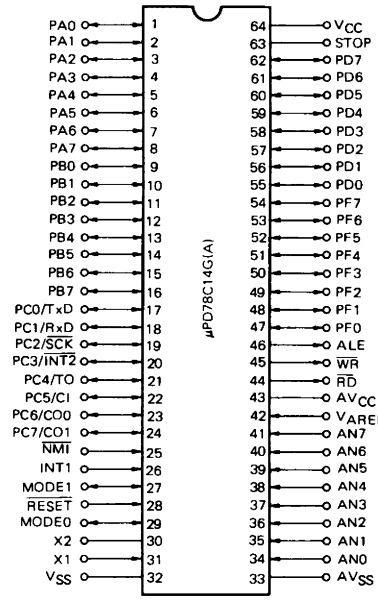
The instruction sets are compatible with the μCOM-87, and moreover involve the 16-bit data operation instructions and multiplication/division instructions to compose a program effectively.

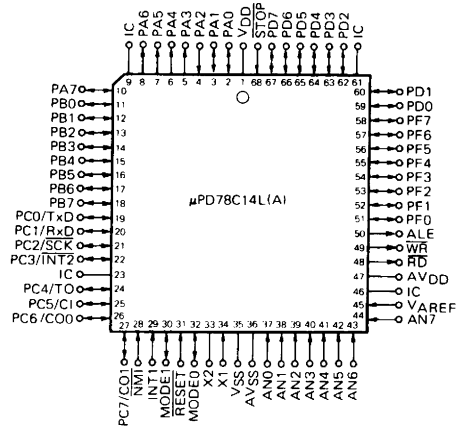
The μCOM-87AD is very suitable in the system control handling analog data, the energy control, process control and automobile, etc.

FEATURES

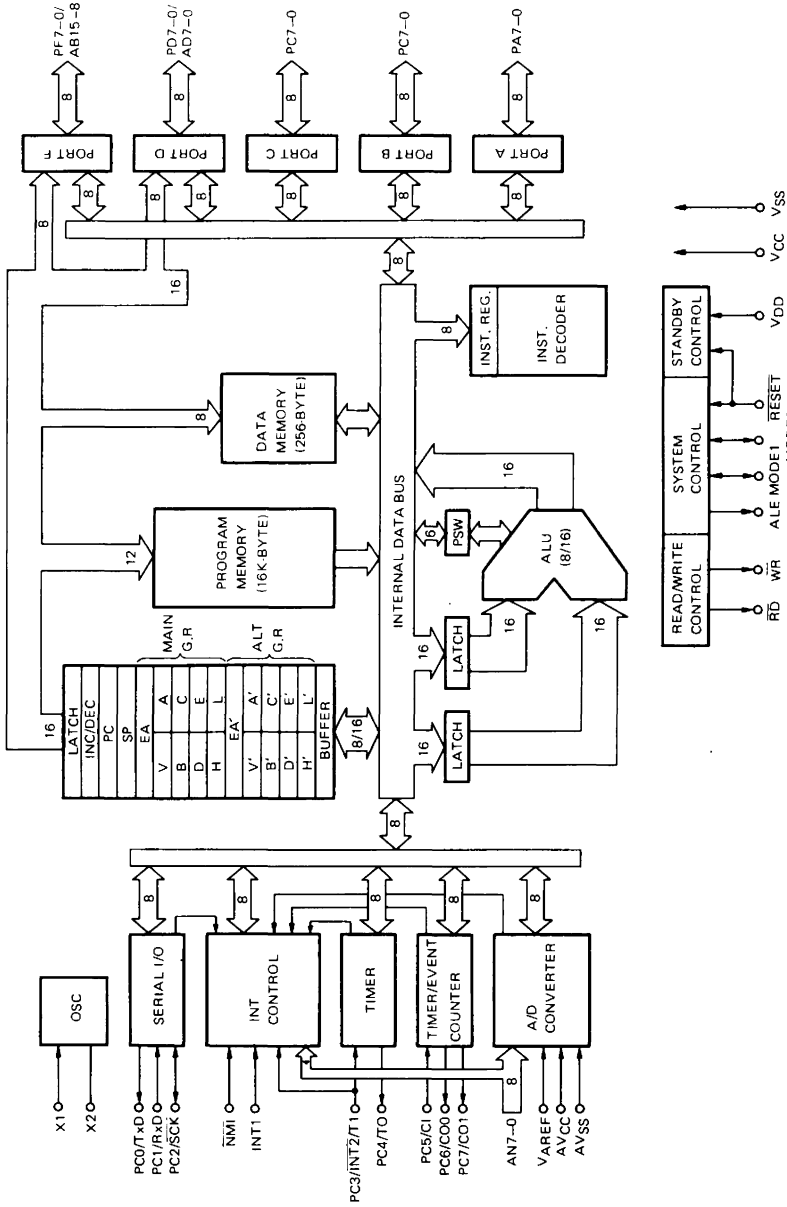
- 1-chip microcomputer (μCOM-87AD)
- 158 kinds of abundant instruction sets, μCOM-87 upward compatible, 16-bit operation instruction multiplication/division instruction
- Instruction cycle: 0.8 μs (15 MHz)
- Program (ROM) capacity: 16 384 words x 8 bits
- Data (RAM) capacity: 256 words x 8 bits
- Direct addressing memories (ROM/RAM) up to 64K bytes
- High-precision 8-bit A/D converter, 8 analog inputs
- General-purpose serial interface
  Asynchronous mode, synchronous mode & I/O interface mode
- Multifunctional 16-bit timer/event counter
- Two 8-bit timers
- Interrupt function (3 external & 8 internal)
- 6 priority levels and the corresponding interrupt address
- I/O ports:
  40 bits (μPD78C14G(A)/L(A))
- Edge-sense inputs: 4 inputs
- Zero-cross detection function
- Standby function: HALT mode, Hardware/Software STOP mode
- Built-in clock oscillator
- CMOS
- Single power supply (+5 V)
- 64-pin plastic QUIP: (μPD78C14G(A))
  68-pin PLCC: (μPD78C14L(A))

PIN CONFIGURATION (Top View)





μPD78C10, μPD78C11 BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM (T_a = 25 °C)

PARAMETER	SYMBOL	TEST CONDITION	RATINGS	UNIT
Power Supply Voltage	V_{DD}		−0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD}+0.5	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to V_{DD}+0.5	V
Output Voltage	V_O		−0.5 to V_{DD}+0.5	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−2.0	mA
		All Output Pin Total	−50	mA
Reference Input Voltage	V_{AREF}		−0.5 to AV_{DD}+0.3	V
Operating Temperature	T_{OPT}	$f_{XTAL} \leqq 12$ MHz	−40 to +85	°C
Storage Temperature	T_{STG}		−65 to +150	°C

OPERATING CONDITION

PARAMETER / OSC. FREQ.	T_a	V_{DD}, AV_{DD}
$f_{XTAL} \leqq 12$ MHz	−40 to 85 °C	+5.0 V ±10 %

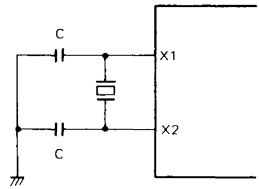
CAPACITANCE (T_a = 25 °C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_I	f_C = 1 MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins are			20	pF
I/O Capacitance	C_{IO}	connected to 0V			20	pF

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = +5.0 V ±10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Voltage	V_{IL1}	Except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7		0		0.8	V
	V_{IL2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to AN7		0		0.2 V_{DD}	V
Input Voltage High	V_{IH1}	Except $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, T1, AN4 to AN7, X1, X2		2.2		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, AN4 to AN7, X1, X2 *1		0.8 V_{DD}		V_{DD}	V
Output Voltage Low	V_{OL}	I_{OL}=2.0 mA				0.45	V
Output Voltage High	V_{OH}	I_{OH}=−1.0 mA		V_{DD}−1.0			V
		I_{OH}=−100 μA		V_{DD}−0.5			V
Input Current	I_I	INT1, T I (PC3); 0 V ≦ V_I ≦ V_{DD}				±200	μA
Input Leakage Current	I_{LI}	Except INT1, TI (PC3) 0 V ≦ V_I ≦ V_{DD}				±10	μA
Output Leakage Current	I_{LO}	0 V ≦ V_O ≦ V_{DD}				±10	μA
AV_{DD} Supply Current	AI_{DD1}	f=15 MHz			0.5	1.3	mA
	AI_{DD2}	STOP mode			10	20	μA
V_{DD} Supply Current	I_{DD1}	Operating mode f=15 MHz			16 *2	30	mA
	I_{DD2}	HALT mode f=15 MHz			8 *2	15	mA
Data Retention Voltage	V_{DDDR}	Hardware/software STOP mode		2.5			V
Data Retention Current	I_{DDDR}	Hardware/ software STOP mode	V_{DDDR}=2.5 V		1	15	μA
			V_{DDDR}=5 V±10 %		10	50	μA

*1 The following oscillation circuit using crystal is recommended.



C=10 pF

*2 T_a = +25 °C, V_{DD} = 5 V

AC CHARACTERISTICS

(T_a=−40 to +85 °C, V_{DD}=+5.0 V± 10 %, V_{SS}=0 V, f_{XTAL}=12 MHz)

READ/WRITE OPERATION

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
X1 Input Cycle Time	t_{CYC}	*1	66	250	ns
Address Setup to ALE↓	t_{AL}	*2	30		ns
Address Hold from ALE↓	t_{LA}	*2	35		ns
Address to $\overline{RD}$↓ Delay Time	t_{AR}	*2	100		ns
$\overline{RD}$↑ to Address Floating	t_{AFR}	*2		20	ns
Address to Data Input	t_{AD}	*2		250	ns
ALE↓ to Data Input	t_{LDR}	*2		135	ns
$\overline{RD}$↓ to Data Input	t_{RD}	*2		120	ns
ALE↓ to $\overline{RD}$↓ Delay Time	t_{LR}	*2	15		ns
Data Hold Time from $\overline{RD}$↑	t_{RDH}	*2	0		ns
$\overline{RD}$↑ to ALE↑ Delay Time	t_{RL}	*2	80		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read, *2	215		ns
		OP Code Fetch, *2	415		ns
ALE Width High	t_{LL}	*2	90		ns
$\overline{M1}$ Setup Time to ALE↓	t_{ML}		30		ns
$\overline{M1}$ Hold Time from ALE↓	t_{LM}		35		ns
$\overline{IO}$/M Setup Time to ALE↓	t_{IL}		30		ns
$\overline{IO}$/M Hold Time from ALE↓	t_{LI}		35		ns
Address to $\overline{WR}$↓ Delay	t_{AW}	*2	100		ns
ALE↓ to Data Output	t_{LDW}	*2		180	ns
$\overline{WR}$↓ to Data Output	t_{WD}	*2		100	ns
ALE↓ to $\overline{WR}$↓ Delay	t_{LW}	*2	15		ns
Data Setup Time to $\overline{WR}$↑	t_{DW}	*2	165		ns
Data Hold Time from $\overline{WR}$↑	t_{WDH}	*2	60		ns
$\overline{WR}$↑ to ALE↑ Delay Time	t_{WL}	*2	80		ns
$\overline{WR}$ Width Low	t_{WW}	*2	215		ns

*1 Cycle time $t_{CYC} = 1/f_{XTAL}$

*2 Load capacitance: C_L = 150 pF

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*1	800		ns
			*2	400		ns
		$\overline{SCK}$ Output		1.6		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*1	335		ns
			*2	160		ns
		$\overline{SCK}$ Output		700		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*1	335		ns
			*2	160		ns
		$\overline{SCK}$ Output		700		ns
RxD Setup Time to $\overline{SCK}$↑	t_{RXK}	*1		80		ns
RxD Hold Time from $\overline{SCK}$↑	t_{KRX}	*1		80		ns
$\overline{SCK}$↓ to TxD Delay Time	t_{KTX}	*1			210	ns

*1 1 x Baud rate in asynchronous, synchronous, I/O interface mode

*2 16 x, 64 x Baud rate in asynchronous

A/D CONVERTER CHARACTERISTICS

(T_a = −40 to +85 °C, V_{DD} = +5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V

V_{DD}−0.5 V ≦ AV_{DD} ≦ V_{DD}, 3.4 V ≦ V_{AREF} ≦ AV_{DD})

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Resolution			8			Bits
Absolute Accuracy		T_a=−10 to +70 °C 4.0 ≦ V_{AREF} ≦ AV_{DD} 66 ns ≦ t_{CYC} ≦ 170 ns			0.4 %±1/2	LSB
		66 ns ≦ t_{CYC} ≦ 170 ns 4.0 V ≦ V_{AREF} ≦ AV_{DD}			0.6 %±1/2	LSB
		66 ns ≦ t_{CYC} ≦ 170 ns			0.8 %±1/2	LSB
Conversion Time	t_{CONV}	66 ns ≦ t_{CYC} ≦ 110 ns	576			t_{CYC}
		110 ns ≦ t_{CYC} ≦ 170 ns	432			t_{CYC}
Sampling Time	t_{SAMP}	66 ns ≦ t_{CYC} ≦ 110 ns	96			t_{CYC}
		110 ns ≦ t_{CYC} ≦ 170 ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1 000		MΩ
Reference Voltage	V_{AREF}		3.4		AV_{CC}	V
V_{AREF} Current	I_{AREF}	Operating mode		1.5	3.0	mA
		Stop mode		0.7	1.5	mA

ZERO-CROSS CHARACTERISTICS

(T_a=−40 °C to +85 °C, V_{CC}=+5.0 V±10 %, V_{SS}=0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		±135	mV
ZERO-Cross Detection Input Frequency	f_{ZX}		0.05	1	kHz

OTHER OPERATIONS

(T_a=−40 °C to +85 °C, V_{CC}=+5.0 V±10 %, V_{SS}=0 V)

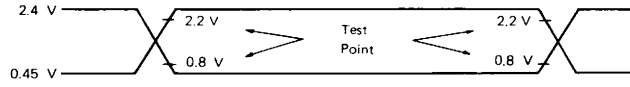
PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
TI Width High, Low	t_{TIH},t_{TIL}		6		t_{CYC}
CI Width High, Low	t_{CI1H},t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H},t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ Width High, Low	t_{NIH},t_{NIL}		10		t_{CYC}
INT1 Width High, Low	t_{I1H},t_{I1L}		36		t_{CYC}
INT2 Width High, Low	t_{I2H},t_{I2L}		36		t_{CYC}
RESET Width High, Low	t_{RSH},t_{RSL}		10		t_{CYC}

EXTERNAL CLOCK TIMING

(T_a=−40 °C to +85 °C, V_{DD}=+5.0 V±10 %, V_{SS}=0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
X1 Input Width High	$t_{\phi H}$		20	250	ns
X1 Input Width Low	$t_{\phi L}$		20	250	ns
X1 Input Rise Time	t_r		0	20	ns
X1 Input Fall Time	t_f		0	20	ns

AC TIMING MESURMENT POINT



BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNIT
t_{AL}	2T – 100	MIN.	ns
t_{LA}	T – 30	MIN.	ns
t_{AR}	3T – 100	MIN.	ns
t_{AD}	7T – 220	MAX.	ns
t_{LDR}	5T – 200	MAX.	ns
t_{RD}	4T – 150	MAX.	ns
t_{LR}	T – 50	MIN.	ns
t_{RL}	2T – 50	MIN.	ns
t_{RR}	4T – 50 (Data Read)	MIN.	ns
	7T – 50 (OP Code Fetch)		
t_{LL}	2T – 40	MIN.	ns
t_{ML}	2T – 100	MIN.	ns
t_{LM}	T – 30	MIN.	ns
t_{IL}	2T – 100	MIN.	ns
t_{LI}	T – 30	MIN.	ns
t_{AW}	3T – 100	MIN.	ns
t_{LDW}	T + 110	MAX.	ns
t_{LW}	T – 50	MIN.	ns
t_{DW}	4T – 100	MIN.	ns
t_{WDH}	2T – 70	MIN.	ns
t_{WL}	2T – 50	MIN.	ns
t_{WW}	4T – 50	MIN.	ns
t_{CYK}	12T ($\overline{SCK}$ Input)(1)	MIN.	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	5T + 5($\overline{SCK}$ Input)(1)	MIN.	ns
	12T – 100 ($\overline{SCK}$ Output)		
t_{KKH}	5T + 5($\overline{SCK}$ Input)(1)	MIN.	ns
	12T – 100 ($\overline{SCK}$ Output)		

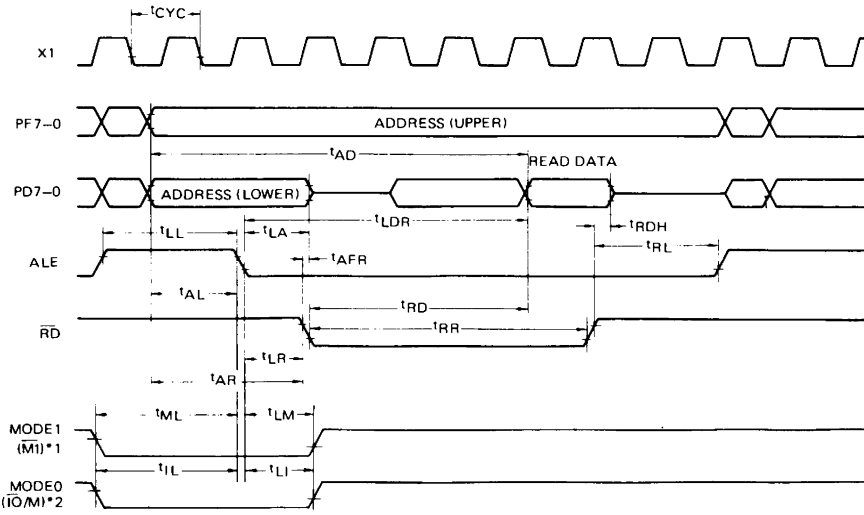
NOTE: (1) 1x Baud Rate in Asynchronous, Synchronous, I/O interface Mode

(2) $T = t_{CYC} = 1/f_{XTAL}$

(3) The items out of this table are not dependent on f_{XTAL}.

TIMING WAVEFORM

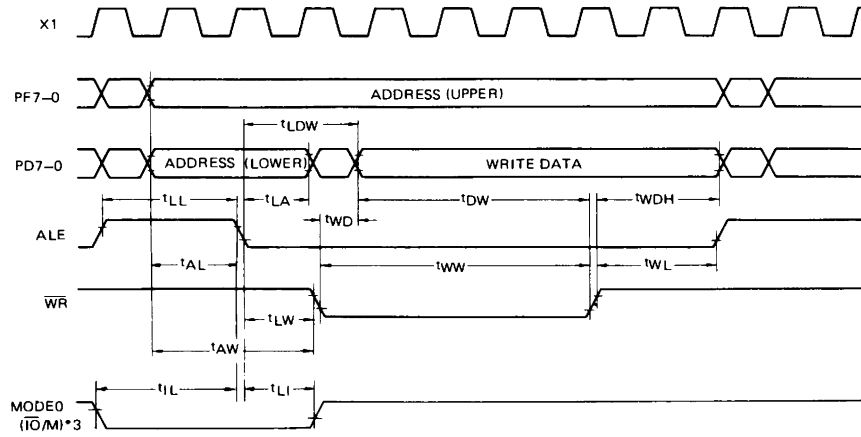
Read Operation



*1 $\overline{M_1}$ is output at the fetech cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

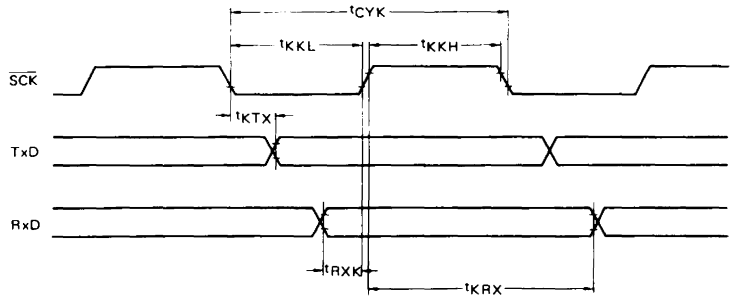
*2 $\overline{IO}$/M is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Write Operation

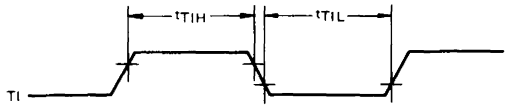


*3 $\overline{IO}$/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Serial Operation

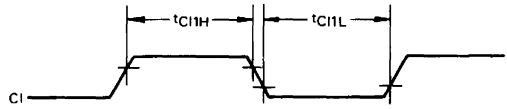


Timer Input Timing

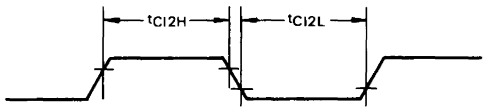


Timer/Event Counter Input Timing

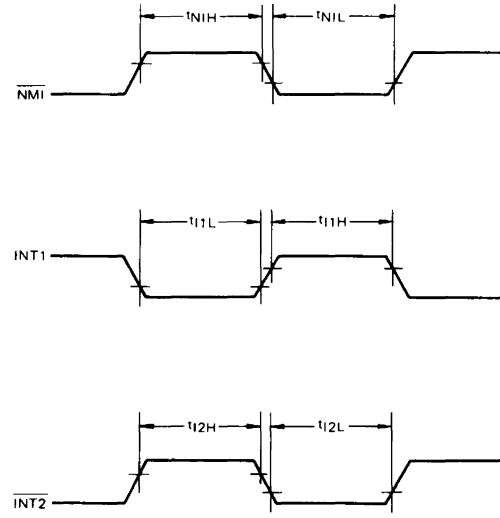
Event Count Mode:



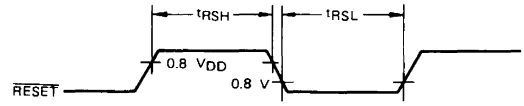
Pulse Width Measurement Mode:



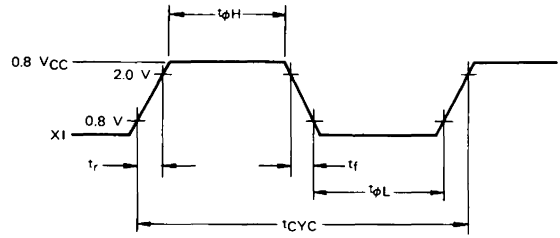
Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



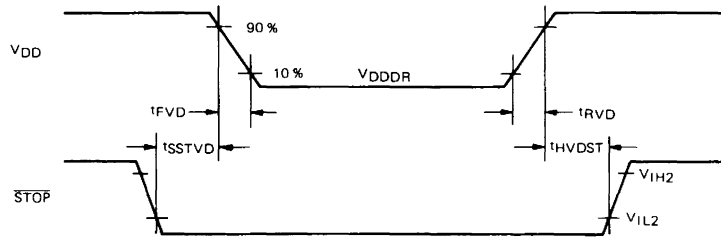
External Clock Timing



STOP MODE LOW VOLTAGE DATA RETENTION CHARACTERISTICS (T_a=−40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	V_{DDDR}		2.5		5.5	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR}=2.5 V		1	15	μA
		V_{DDDR}=5 V ±10 %		15	50	μA
V_{DD} Rise and Fall Time	t_{RVD}, t_{FVD}		200			μs
$\overline{STOP}$ Setup Time to V_{DD}↓	t_{SSTVD}		12T+0.5			μs
$\overline{STOP}$ Hold Time after V_{DD}↑	t_{HVDST}		12T+0.5			μs

DATA RETENTION MODE TIMING



The μPD78312 is a CMOS 16/8-bit single-chip microcomputer which is a member of μCOM-78K/III series. It contains 16-bit CPU, ROM, RAM, A/D converter, powerful multifunctional pulse input/output unit and general-purpose serial communication interface. Moreover, the μPD78312 contains new concept hardware which calls macro service function.

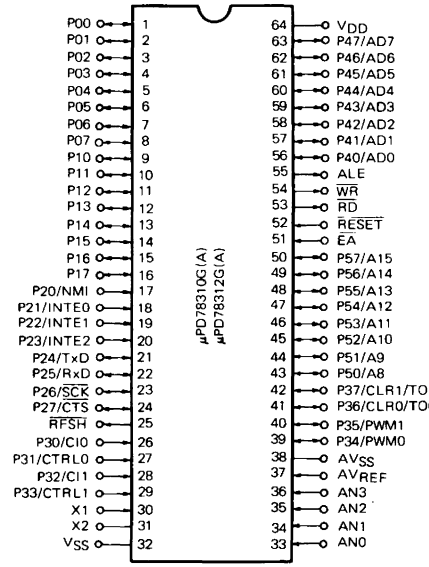
The μPD78310 is a ROM-less version of the μPD78312.

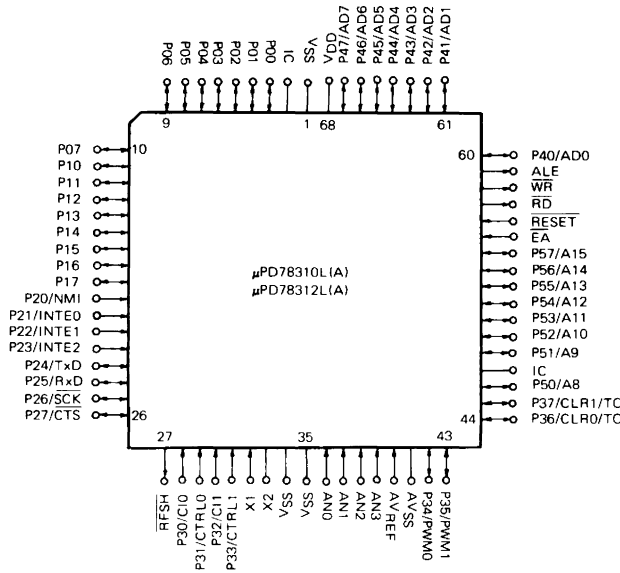
The μPD78312 is very suitable in the servo motor control, the total engine control, robot, NC and printer.

FEATURES

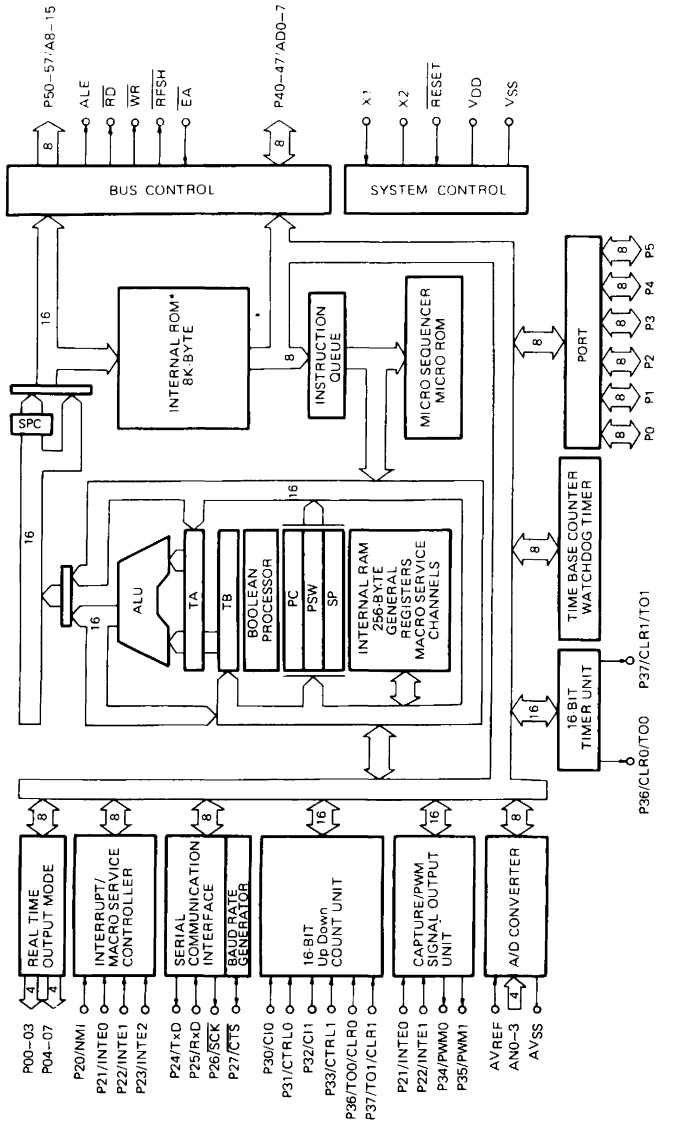
- Single-chip microcomputer (μCOM-78K/III)
- 96 instructions with abundant addressing modes
  16-bit operation instructions, bit manipulation instructions, multiplication/division instructions, string instructions, user stack manipulation instructions
- Instruction cycle: 0.55 μs (11 MHz)
- Internal ROM: 8 192 words x 8 bits (μPD78312)
- Internal RAM: 256 words x 8 bits
- Direct addressing memories (ROM/RAM) up to 64K bytes.
- Memory mapping of on-chip peripheral hardware (SFR: Special Function Register)
- Multifunctional pulse input/output units
  - Two 16-bit presettable up/down counters
  - Two 16-bit capture units
  - Two high-accuracy PWM outputs
  - Two 16-bit interval timers
  - Two 4-bit real-time output ports
- Four high-precision 8-bit A/D converters
- I/O ports
  - 8 input lines
  - 40 I/O lines (μPD78312)
  - 24 I/O lines (μPD78310)
- General-purpose serial communication interface (with dedicated Baud rate generator)
  - Asynchronous mode, I/O interface mode
- Interrupt request controller (External x 4, Internal x 13)
  - 8-level programmable priority
- Three types of interrupt request service
  - Vector interrupt function
  - Context switching function
  - Macro service function (the effect of DMA function)
- Pseudo static memory refresh pulse output function
- Watchdog timer, time base counter
- Standby function (STOP/HALT)
- CMOS
- Single power supply (+5 V)
- 64-pin plastic QUIP: (μPD78310G(A), μPD78312G(A))
  68-pin PLCC: (μPD78310L(A), μPD78312L(A))

PIN CONFIGURATION





μPD78310, μPD78312 BLOCK DIAGRAM



* Note: The μPD78310 has no programmable ROM (8K Bytes) on chip.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM (T_a = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Supply Voltage	V_{DD}		−0.5 to +7.0	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to +7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−1	mA
		All Output Pin Total	−25	mA
Reference Input Voltage	V_{AREF}		−0.5 to V_{DD}	V
Operating Temperature	T_{OPT}	$f_{XX} \leqq 11$ MHz	−40 to +85	°C
Storage Temperature	T_{STG}		−65 to +150	°C

OPERATING CONDITION

PARAMETER / OSC. FREQ.	T_a	V_{DD}, AV_{DD}
$f_{XTAL} \leqq 12$ MHz	- 40 to +85 °C	+5.0 V ± 10 %

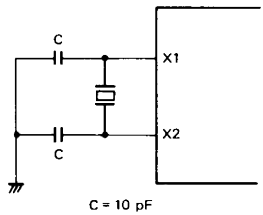
CAPACITANCE (T_a = 25 °C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_I	f_C = 1 MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins are			20	pF
I/O Capacitance	C_{IO}	connected to 0 V			20	pF

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = +5.0 V ± 10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Voltage Low	V_{IL1}	Except $\overline{EA}$		0		0.75	V
	V_{IL2}	$\overline{EA}$		0		0.4	V
Input Voltage High	V_{IH1}	Except P20/NMI, X1, X2, $\overline{RESET}$		2.3		V_{DD}	V
	V_{IH2}	P20/NMI, X1 X2, $\overline{RESET}$ *1		3.9		V_{DD}	V
Output Voltage Low	V_{OL}	I_{OL}=1.9 mA				0.45	V
Output Voltage High	V_{OH}	I_{OH}=−380 μA		2.4			V
Input Current	I_I	P20/NMI, $\overline{RESET}$, 0.45 V < V_I < V_{DD}				±10	μA
Input Leakage Current	I_{LI}					±10	μA
Output Leakage Current	I_{LO}	0 V ≦ V_O ≦ V_{DD}				±10	μA
Reference Input Current	AI_{REF}				1.5	5.5	mA
V_{DD} Supply Current	I_{DD1}	Operating mode, f_{CLK}=5.5 MHz			30 *2	85	mA
	I_{DD2}	HALT mode, f_{CLK}=5.5 MHz			5 *2	17	mA
Data Retention Voltage	V_{DDDR}	Hardware/software STOP mode					V
Data Retention Current	I_{DDDR}	Hardware/ software STOP mode	V_{DDDR}=2.5 V		1	15	μA
			V_{DDDR}=5 V±10 %		10	50	μA

*1 The following oscillation circuit using crystal is recommended.



f_{XX} : Crystal frequency
f_X : External clock frequency
f_{CLK} : Internal system clock

*2 T_a = +25 °C, V_{DD} = 5 V

AC CHARACTERISTICS

(T_a = −40 to +85 °C, V_{DD} = +5.0 V ± 10 %, V_{SS} = 0 V, f_{XX} = 11 MHz)

READ/WRITE OPERATION

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
X1 Input Cycle Time	t_{CYC}	*1	189	400	ns
		*2	724	1600	ns
Address Setup Time to ALE↓	t_{AL}	*3	160		ns
Address Hold Time from ALE↓	t_{LA}	*3	20		ns
Address to $\overline{RD}$↓ Delay Time	t_{AR}	*3	250		ns
$\overline{RD}$↓ to Address Floating Time	t_{AFR}	*3		0	ns
Address to Data Input Time	t_{AD}	*3		440	ns
ALE↓ to Data Input Time	t_{LDR}	*3		250	ns
$\overline{RD}$↓ to Data Input Time	t_{RD}	*3		190	ns
ALE↓ to $\overline{RD}$↓ Delay Time	t_{LR}	*3	60		ns
Data Hold Time from $\overline{RD}$↓	t_{RDH}	*3	0		ns
$\overline{RD}$↑ to Address Active Time	t_{RA}		50		ns
$\overline{RD}$↑ to ALE↑ Delay Time	t_{RL}	*3	120		ns
$\overline{RD}$ Width Low	t_{RR}	*3	210		ns
ALE Width High	t_{LL}	*3	130		ns
Address to $\overline{WR}$↓ Delay Time	t_{AW}	*3	250		ns
ALE↓ to Data Output Time	t_{LDW}	*3		220	ns
$\overline{WR}$↓ to Data Output Time	t_{WD}	*3		110	ns
ALE↓ to $\overline{WR}$↓ Delay Time	t_{LW}	*3	60		ns
	t_{LW1}	*3 Refresh pulse mode	120		ns
Data Setup Time to $\overline{WR}$↑	t_{DW}	*3	160		ns
Data Setup Time to $\overline{WR}$↓	t_{DWS}	*3 Refresh pulse mode	30		ns
Data Hold Time from $\overline{WR}$↑	t_{WDH}	*3	20		ns
$\overline{WR}$↑ to ALE↑ Delay Time	t_{WL}	*3	120		ns
$\overline{WR}$ Width Low	t_{WW}	*3	210		ns

*1 Cycle time $t_{CYC} = 2/f_{XX}$ (Normal mode)

*2 Cycle time $t_{CYC} = 8/f_{XX}$ (Low speed mode)

*3 Load capacitance: C_L = 100 pF, Load resistor: R_L = 2 kΩ

SERIAL OPERATION (T_a = −40 °C to +85 °C, V_{DD} = +5.0 ± 10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITION			MIN.	MAX.	UNIT
Serial Clock Cycle Time	t_{CYK}	Output	$\overline{SCK}$	*1	1.46		μs
			$\overline{CTS}$	*2	1.46		μs
		Input	$\overline{CTS}$	*3	1.09		μs
Serial Clock Low Level Width	t_{KKL}	Output	$\overline{SCK}$	*1	645		ns
			$\overline{CTS}$	*2	645		ns
		Input	$\overline{CTS}$	*3	465		ns
Serial Clock High Level Width	t_{KKH}	Output	$\overline{SCK}$	*1	645		ns
			$\overline{CTS}$	*2	645		ns
		Input	$\overline{CTS}$	*3	465		ns
$\overline{CTS}$ High & Low Level Width	t_{CTSH}, t_{CTSL}			*4	3		t_{CLK}
RxD Setup Time to $\overline{CTS}$↑	t_{RXK}				90		ns
RxD Hold Time to $\overline{CTS}$↑	t_{KRX}				90		ns
$\overline{SCK}$↓ to TxD Delay Time	t_{KTX}					230	ns

*1: I/O interface mode, transmittion rate = 687 kbps

*2: I/O interface mode, receiving rate = 687 kbps

*3: I/O interface mode, receiving rate = 916 kbps

*4: Asynchronous mode

A/D CONVERTER CHARACTERISTICS (T_a = −40 °C to +85 °C, V_{DD} = +5 V ± 10 %, 4.0 V ≦ AV_{REF} ≦ V_{DD}, AV_{SS} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Resolution			8			bit
Full Scale Error		V_{DD} = −10 °C to +70 °C			±0.4	%
					±0.6	%
Quantization Error					±1/2	LSB
Conversion Time	t_{CONV}	200 ns ≦ t_{CLK} ≦ 250 ns	180			t_{CLK}
		250 ns ≦ t_{CLK} ≦ 1600*	120			t_{CLK}
Sampling Time	t_{SAMP}	200 ns ≦ t_{CLK} ≦ 250 ns	36			t_{CLK}
		250 ns ≦ t_{CLK} ≦ 1600*	24			t_{CLK}
Analog Input Voltage	V_{IAN}		0		AV_{REF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
Reference Voltage	AV_{REF}		3.4		V_{DD}	V
AV_{REF} Current	IV_{REF}	f_{CLK} = 5 MHz		1.5	5.5	mA

* $f_{CLK} = f_{XX}/8$

COUNTER UNIT OPERATION (T_a = −40 °C to +85 °C, V_{DD} = +5.0 V ± 10 %, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
CI0, CI1 High, Low Level Width	t_{CIH}, t_{CIL}		3		t_{CLK}
CTRL0, CTRL1 High, Low Level Width	t_{CTLH}, t_{CTLL}		3		t_{CLK}
CTRL0, CTRL1 Setup Time to CI↑	t_{CTCIS}	• Mode 3 • Select the rising edge of CI	2		t_{CLK}
CTRL0, CTRL1 Hold Time to CI↑	t_{CICTH}	• Mode 3 • Select the rising edge of CI	5		t_{CLK}
CLR0, CLR1 High, Low Level Width	t_{CLRH}, t_{CLRL}		3		t_{CLK}

OTHER OPERATION (T_a = −40 °C to +85 °C, V_{DD} = +5.0 V ± 10 %, V_{SS} = 0 V)

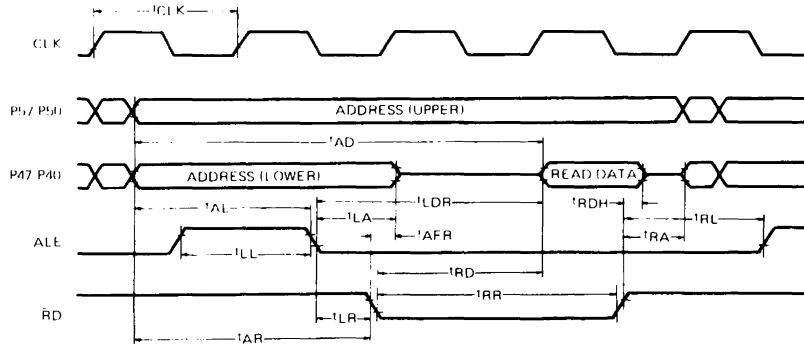
PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
NMI High, Low Level Width	t_{NIH}, t_{NIL}		10		μs
INTE0 High, Low Level Width	t_{I0H}, t_{I0L}		3		t_{CLK}
INTE1 High, Low Level Width	t_{I1H}, t_{I1L}		3		t_{CLK}
INTE2 High, Low Level Width	t_{I2H}, t_{I2L}		3		t_{CLK}
$\overline{\text{RESET}}$ High, Low Level Width	t_{RSH}, t_{RSL}		10		μs

EXTERNAL CLOCK TIMING (T_a = −40 °C to +85 °C, V_{DD} = +5.0 V ± 10 %, V_{SS} = 0 V)

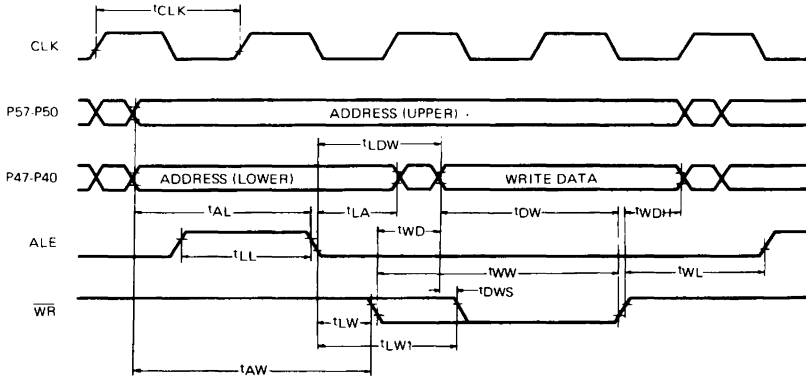
PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
X1 Input Width High	$t_{\phi H}$		30	100	ns
X1 Input Width Low	$t_{\phi L}$		30	100	ns
X1 Input Rise Time	t_r		0	20	ns
X1 Input Fall Time	t_f		0	20	ns
X1 Input Cycle Time	t_x		90	200	ns

TIMING WAVEFORM

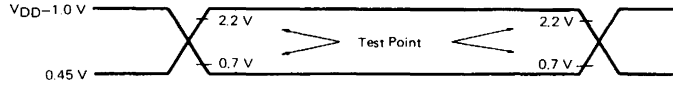
Read Operation



Write Operation

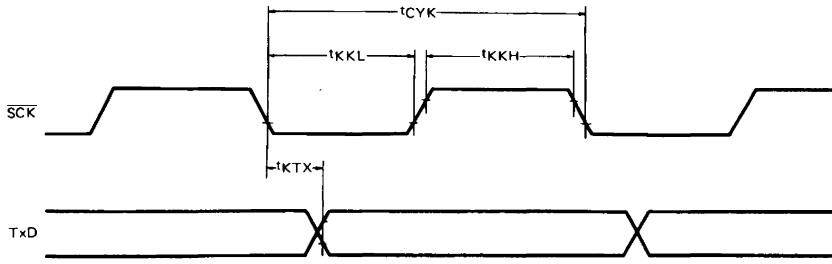


AC TIMING MEASUREMENT POINT

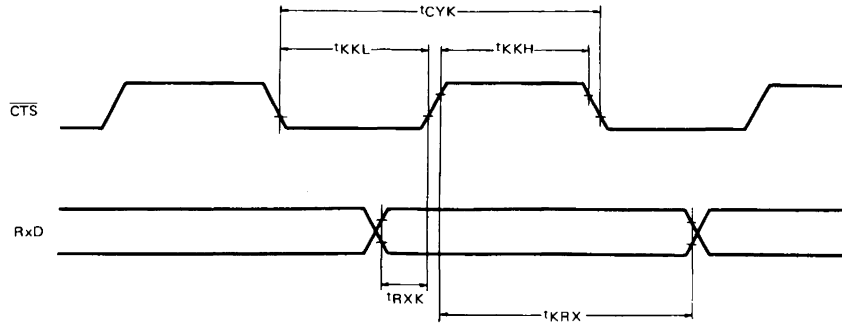


SERIAL OPERATION

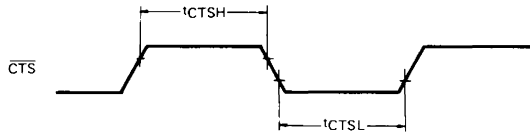
I/O Interface Mode (Transmission)



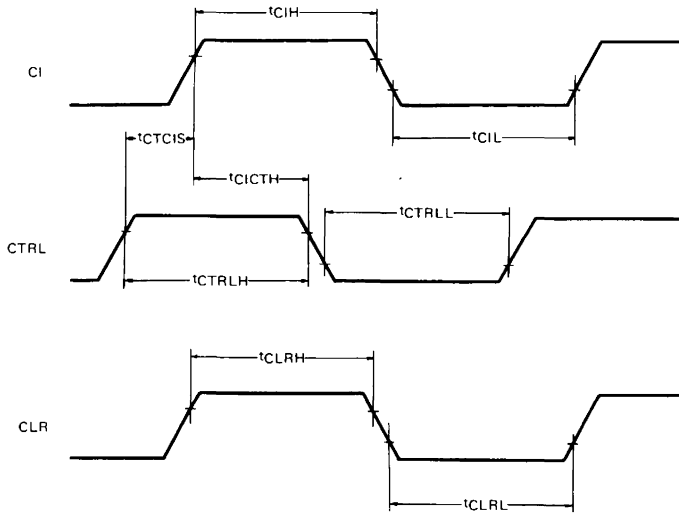
I/O Interface Mode (Reception)



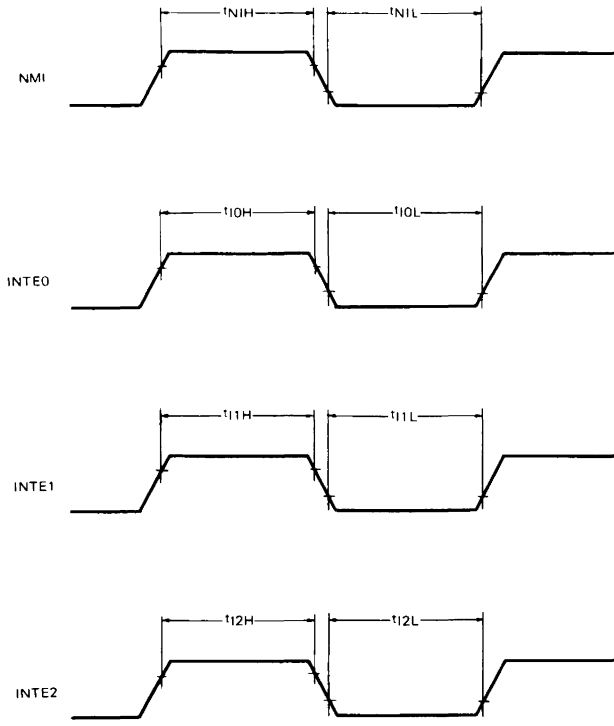
Asynchronous Mode (Transmission enable input timing)



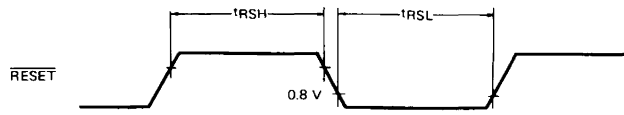
COUNTER UNIT INPUT/OUTPUT TIMING



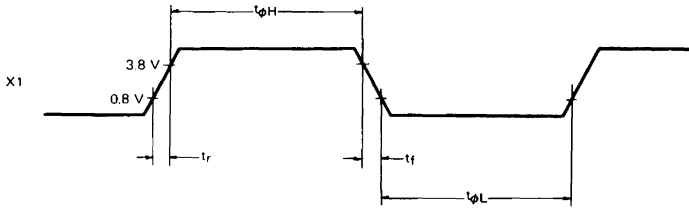
INTERRUPT TIMING



RESET INPUT TIMING

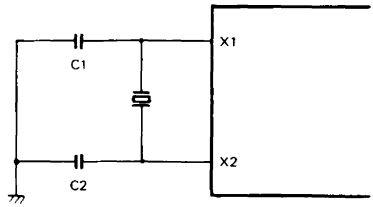


EXTERNAL CLOCK TIMING

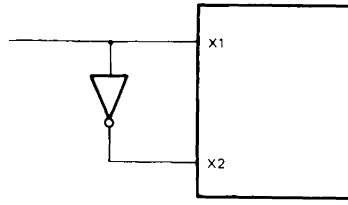


RECOMMENDED OSCILLATION CIRCUIT

(1) Crystal



(2) External clock



STOP MODE LOW VOLTAGE DATA RETENTION CHARACTERISTICS (T_a = −40 °C to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	V_{DDDR}		2.0			V
Data Retention Supply Current	I_{DDDR}	V_{DDDR} = 2.0 V		1	15	μA
		V_{DDDR} = 5 V ± 10 %		15	50	μA

QUALITY AND RELIABILITY OF NEC MICROPROCESSORS

INTRODUCTION

As large-scale integration reaches a higher level of density, reliability of devices imposes a profound impact on system reliability. And as device reliability becomes a major factor, test methods to assure acceptable reliability become more complicated. Simply performing a reliability test according to a conventional method cannot satisfy the demanding requirements for higher reliability: at these new, higher levels of LSI density, it is increasingly difficult to activate all the elements in the internal circuits. A different philosophy and methodology is needed for reliability assurance in microprocessors and family products. Moreover, as integration density increases, the degradation of internal elements in an LSI device is seldom detected by measuring characteristics across external terminals.

In order to improve and guarantee a certain level of reliability for large-scale integrated circuits, it is essential to build quality and reliability into the product. Then the conventional reliability tests are followed to ensure that the product demonstrates an acceptable level of reliability.

NEC has introduced the concept of Total Quality Control (TQC) across its entire semiconductor production line. By adopting TQC, NEC can build quality into the product and thus assure higher reliability. The concept and methodology of Total Quality Control are companywide activities – involving workers, engineers, quality control staffs, and all levels of management.

NEC has also introduced a prescreening method into the production line that helps eliminate most of the potentially defective units. The combination of building quality in and screening projected early failures out has resulted in superior quality and excellent reliability.

This Reliability Report describes the philosophy and methodology used by NEC to attain a higher level of reliability for microprocessors and family products.

TECHNOLOGY DESCRIPTION

Most microprocessors and family products are produced utilizing high performance, high density, N-channel MOS technology. State-of-the-art high performance has been achieved by introducing fine line generation techniques. The data presented in this report shows that this advanced technology yields products as reliable as those from previous technologies.

By reducing physical parameters, circuit density and performance were increased while active circuit power dissipation decreased. Current state-of-the-art N-channel MOS technology utilizes 2–4μm channel length and a gate oxide thickness of 300–500 Å. This advanced process yields integration densities of 400–800 gates/mm^2 with a speed-power product of 1pJ or less.

Technology evolution

Technology evolved from early P-channel MOS to current state-of-the-art high performance, high density, N-channel MOS during the past decade. This evolution is expected to continue in the future. As a result, even more high level functions will be included in a small area, as past history demonstrates.

RELIABILITY TESTING

Reliability is defined as the characteristics of an item expressed by the probability that it will perform a required function under stated conditions for a stated period of time. This involves the concept of probability, definition of a required function(s), and the critical time used in defining the reliability.

Definition of a required function, by implication, treats the definition of a failure. Faulure is defined as the termination of the ability of a device to perform its required function(s). Futhermore, a device is said to have failed if it shows inability to perform within guaranteed parameters as given in an electrical specification.

Discussion of reliability and failure can be approached in two ways: with respect to systems or to individual devices. The accumulation of normal device failure rates constitutes the expected failure rate of the system hardware. Important considerations here are the constant failure period, the early failure (infant mortality) period, and overall reliability level. With regard to individual devices, areas of prime interest include specific failure mechanisms, failures in accellerated tests, and screening tests.

Some of these failure considerations pertain to both systems and devices. The probalility of no failures in a system is the product of the probability of no failure in each of its components. The failure rate of system hardware is then the sum of the failure rates of the components used to construct the system.

Life distribution

The fundamental principles of Reliability Engineering predict that the failure rate of a group of devices will follow the wellknown Bathtub curve in Figure 1. The curve is divided into three regions: Infant Mortality, Random Failures, and Wearout Failures.

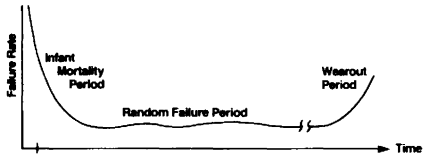


Figure 1. Reliability Life (Bathtub) Curve

Infant mortality, as the name implies, represents the early life failures of devices. These failures are usually associated with one or more manufacturing defects.

After some period of time, the failure rate reaches a low value. This is the random failure portion of the curve, representing the useful portion of the life of a device. During this random failure period there is a decline in the failure rate due to the depletion of potential random failures from the general population.

The wearout failures occur at the end of the device's useful life. They are characterized by a rapidly rising failure rate over time as devices wear out both physically and electrically. Thus, for devices which have very long life expectancies compared to those of systems, the areas of concern will be the infant mortality and the random failure portions of the population.

The system failure rates are related to the collective device failure rates. In a given sytem, after elimination of the early failures, the system will be left to the failure rate of its components. In order to make proper projections of the failure rate in the operating environment, time-to-failure must be accelerated in tests in a predictable way.

Failure distribution at NEC

MOS and Bipolar integrated circuits returned to NEC from the field underwent extensive failure analysis at NEC's Integrated Circuit Division.

First, approximately 50 percent of the field returns were found to be damaged either from improper handling or misuse of the devices. These units were eliminated from the analysis. The remaining failed units were classified by their failure mechanisms, as depicted in Figure 2. These failures were then related to the major integrated circuit failure mechanisms and to their origins in a particular manufacturing step.

As shown in Figure 2, the first four failure mechanisms accounted for more than 90 percent of total failures. As a result, NEC improved processes and material to reduce these failures. Additionally, NEC introduced screening procedures to detect and eliminate defective devices.

Temperature, humidity, and bias tests are used for testing the moisture resistance of plastic encapsulated integrated circuits. NEC developed a special process to improve the plastic encapsulation material. As a result, moisture-related – thus packaging-related – failures have been drastically reduced.

As a preventive measure, NEC hat introduced a special screening procedure embedded in the production line. A burn-in at an elevated temperature is performed for 100 percent of the lots. This burn-in effectively removes the potentially defective units. In addition, improvement of the plastic encapsulation material has lowered the failures in a high temperature and high humidity environment.

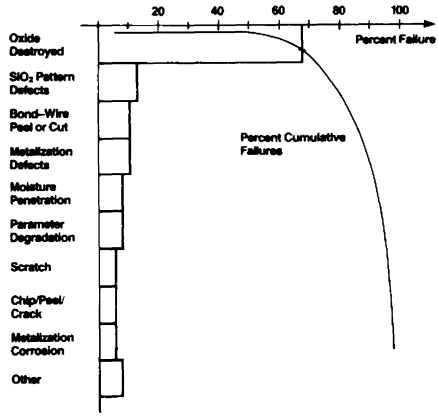


Figure 2. Failure Distribution of MOS Integrated Circuits

Accelerated reliability testing

As an example, assume that an electronic system contains 1000 integrated circuits and can tolerate 1 percent system failures per month. The failure rate per component is:

$$\frac{0.01 \text{ Failures}}{720\text{K Device Hours}} = 13.888 \times 10^{-9} \text{ Failures/Hour}$$

or 13.8888 FITs

Where: FIT = Failure unit per 10^9 device hours

To demonstrate this failure rate, note that 13.8888 FITs correspond to one failure in about 7,000 devices in an operating test of 10,000 hours. It is quickly apparent that a test condition is required to accelerate the time-to-failure in a predictable and understandable way. The implicit requirement for the accelerated stress test is that the relationship between the accelerated stress testing condition and the condition of actual use be known.

A most common time-to-failure relationship involves the effect of temperature, which accelerates many physiochemical reactions leading to device failure. Other environmental conditions are voltage, current, humidity, vibration, or some combination of these. Table 2 lists the Reliability Assurance Tests performed at NEC for the N-channel MOS devices.

TABLE 1. MONTHLY NEC RELIABILITY TESTS

TEST	METHOD	TEST CONDITIONS
Life Test High Temperature, Operating	*MIL-STD-883B* 1005A, D	T_a = 100°C to 125°C for 1000 hrs
High Temperature, Storage	1008C	T_a = 150°C for 1000 hrs
High Temperature, High Humidity Test	–	T_a = 85°C @ 85 % RH for 1000 hrs
Pressure Cooker Test	–	T_a = 125°C @ 2.3 Atm for 168 hrs
Environmental Test Soldering Heat Test	2031*	T = 260°C for 10s without flux
Temperature Cycle	1010C	T = −65°C to +150°C for 10 cycles
Thermal Shock	1011A	T = 0°C to 100°C for 15 cycles
Lead Fatigue	2004B2	@ 250gm: 3 leads, 3 bends
Solderability	2003	T = 230°C for 5s with flux

Note: *MIL-STD-750A

Temperature Effect: The effect of temperature that concerns us is that which responds to the Arrhenius relationship. This relates the reaction rate to temperature.

$$R = Ro\ Exp[-Ea/kT]$$

Where: Ro = Constant
Ea = Activation energy in eV
k = Boltzmann's constant
= 8.617*10** (−5) eV/degrees K
T = Absolute temperature in degrees K

The significance of this relationship is that the failure mechanisms of semiconductor devices are directly applicable to it. A linear relationship between failure mechanism and time is assumed.

Activation Energy: Associated with each failure mechanism is an activation energy value. Table 3 lists some of the more common failure mechanisms and the associated activation energy of each.

TABLE 2. ACTIVATION ENERGY AND DETECTION OF FAILURE MECHANISMS

FAILURE MECHANISM	ACTIVATION ENERGY	DETECTION
Oxide Defect	0.3eV	High Temperature Operating Life Test
Silicon Defect	0.3eV	
Ionic Contamination	1.0–1.35eV	
Electromigration	0.4–0.8eV	
Charge Injection	1.3eV	
Gold-Aluminium Interface	0.8eV	
Metal Corrosion	0.7eV	High Humidity Operating Life Test

High Temperature Operating Life Test: his test is used to accelerate failure mechanism

High Temperature Operating Life Test: This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature. For N-channel MOS microprocessors and their family products, the operating temperature is 125°C. The data obtained is translated to a lower temperature by using the Arrhenius relationship.

High Temperature and High Humidity Test: Semiconductor integrated circuits are highly sensitive to the general accelerating effect of humidity in causing electrolytic corrosion between biased lines. The high temperature and high humidity test is performed to detect failure mechanisms which are accelerated by these conditions. This test is effective in accelerating leakage-related failures and drifts in device parameters due to process instability.

High Temperature Storage Test: Another common test is the high temperature storage test in which devices are subjected to elevated temperatures with no applied bias. This test is used to detect mechanical problems and process instability.

Environmental Test: Other environmental tests are performed to detect problems related to the package, material, susceptibility to extremes in environment, and problems related to usage of the devices.

FAILURE RATE CALCULATION AND PREDICTION

Analysis of integrated circuit failure rates can serve many useful purposes. For example, the early life failure rate helps establish a warranty period, while the mature life failure rate aids in estimating repair costs, spare parts stock requirements, or product downtime. Accurate prediction of failure rates can also be used for process control.

The following sections describe the failure rate calculation and prediction methods used by NEC's Integrated Circuit Division.

The Arrhenius model
Most integrated circuit failure mechanisms depend, to some degree, on temperature. This relastionship can be represented by the Arrhenius model, which includes the effects of temperature and activation energy of the failure mechanisms.

As applied to accelerated life testing of integrated circuits, the Arrhenius model assumes that degradation of a performance parameter is linear with time. Temperature dependence is taken to be the exponential function that defines the probability of occurrence. The relationship of failure rate to temperature is expressed as:

$$F_1 = F_2 * Exp[(Ea/k) * (1/T_1 - 1/T_2)]$$

Where: F_2 = Failure rate at T_2
F_1 = Failure rate at T_1
Ea = Activation energy
k = Boltzmann's constant
T = Operating junction temperature in degrees K

This equation explains the thermal dependence of integrated circuit failure rates and is used for derating the resulting failure rate to a more realistic temperature.

Acceleration factor

The acceleration factor is the factor by which the failure rate can be accelerated by increased temperature. This factor is derived from the Arrhenius failure rate expression, resulting in the following form:

$$A = F_1/F_2 = Exp[(Ea/k) * (1/T_1 - 1/T_2)]$$

Where: A = Acceleration factor
F_2 = Failure rate at T_2
F_1 = Failure rate at T_1

In calculating the field reliability of an integrated circuit, it is necessary to calculate the junction temperature. In general, the junction temperature will depend on the ambient temperature, cooling, package type, operating cycle time, and power dissipation of the circuit itself. In these terms, the junction temperature (T_j) is expressed as:

$$T_j = T_a + Pd * Af * \theta jA$$

Where: T_j = Junction temperature
T_a = Ambient temperature
Pd = Power dissipation
Af = Air flow factor
θjA = Package thermal resistance

Table 4 lists derating factors of various failure mechanisms. This table is generated assuming that an accelerated test is performed at a junction temperature of 125°C. The result is then derated to 55°C junction temperature. The acceleration factor may then be obtained by taking the inverse of the derating factor.

TABLE 3. DERATING FACTORS OF FAILURE MECHANISMS

FAILURE MECHANISM	ACTIVATION ENERGY	DERATING FACTOR
Oxide Defect	0.3eV	0.1546
Silicon Defect	0.3eV	0.1546
Ionic Contamination	1.0eV	0.001984
Electromigration	0.4eV	0.08307
Charge Injection	1.3eV	0.0003067
Metal Corrosion	0.7eV	0.01315
Gold-Aluminium Interface	0.8eV	0.006886

The acceleration of failure mechanisms in a high humidity and high temperature environment must be expressed as a function not only of temperature but also of humidity.

According to the reliability test statistics, the acceleration factor in such an environment can best be approximated with Peck's model as follows:

$$A = Exp[(Ea/k) * (1/T_1 - 1/T_2)] * [H_2/H_1]^{**} 4.5$$

Where: Ea = Activation energy
k = Boltzmann's constant
T = Junction temperature
H = Relative humidity

For example, the acceleration factor for high humidity and high temperature or pressure cooker tests ranges from 100 to 1000 times that of the normal operating environment.

Failure rate calculation

As an example, suppose that NEC's microprocessors and family product samples are submitted to a 1000-hour life test at 125°C junction temperature and encounter two failures: one oxide and one metalization defect. The sample size is 885 units.

Thus, the oxide failure rate is 0.11 percent per 1000 hours and the metalization failure rate is 0.11 percent per 1000 hours. Therefore, the total failure rate at 125°C sums to 0.22 percent per 1000 hours at 1K hours.

Failure rate prediction

To derate these failure rates to a normal operating environment, use the derating factors listed in Table 4.

Oxide Failures = 0.11 * 0.1546 = 0.01701 % per 1K hrs
Metal Failures = 0.11 * 0.01315 = 0.00145 % per 1K hrs
Total Failures = 0.01846 % per 1K hrs

Note that the example above is a snapshot of the high temperature life test performed on a particular lot. It is not accumulated data that can be used to represent overall reliability. This conservative illustration, however, shows that the failure rate in a normal operating environment is approximately 12 times lower than that of a higher temperature environment.

The failure rate prediction takes different activation energies into account whenever the causes of failures are known through performing failure analysis. In some cases, however, an average activation energy is assumed in order to accomplish a quick first-order approximation: NEC assumes an average activation energy of 0.7eV whenever the exact failure mechanism is not known, to yield a convervative estimate of failure rates.

RELIABILITY TEST RESULTS

Before introducing new technologies of products, NEC's internal reliability goals must be attained. Several categories of testing are used in the internal qualification program to assure that product reliability meets NEC's reliability goals. Once the product is qualified, its reliability level is regularly monitored in a monthly reliability test.

NEC's GOALS ON FAILURE RATES

NEC's approach to achieving high reliability is to build quality into the product, as opposed to merely screening out defective units. The use of distributed control methods embedded in the production line, in conjunction with conventional screening methods, results in the highest reliability at the lowest cost.

NEC currently maintains failure rates for infant mortality and long-term device operation as listed in Table 4.

TABLE 4. INFANT MORTALITY AND LONG-TERM FAILURE RATES

	PERCENT FAILURE RATE GOALS
Infant Mortality Failure Rate	0.10/1K hrs
Long-term Life failure Rate	
1.2M Device Hour Average	0.02/1K hrs
3.0M Device Hour Average	0.01/1K hrs

Infant mortality process average goals

The infant mortality goal for each product group is set at 0.10 percent. When a failure rate exceeds this level, there is prompt remedial action to reduce this rate.

Long-term failure rate goals

The long-term failure rate goal is based on the following conditions:

- A minimum of 1.2 million device hours at 125°C is accumulated to resolve 0.02 percent per 1000 hours at 55°C with a 60 percent confidence level.
- A minimum of 3 million device hours at 125°C is accumulated to resolve 0.01 percent per 1000 hours at 55°C with a 60 percent confidence level.

INFANT MORTALITY FAILURE SCREENING

It is logical to assume that the integrated circuit that fails at one temperature would also fail at another temperature, except that it would fail sooner at a higher temperature. As can be expected, the failure rate is a function of its associated activation energy. Establishing infant mortality screening, therefore, requires knowledge of the likely failure mechanisms and their associated activation energy.

The most likely mechanisms associated with infant mortality failures are generally manufacturing defects and process anomalies. These generally consist of contamination, cracked chips, wire bond shorts, or bad wire bonds. Since these describe a number of possible mechanisms, any one of which might predominate at a given time, the activation energy for infant mortality might be expected to vary considerably.

The effectiveness of a screening condition, preferably at some stress level in order to shorten the time, varies greatly with the failure mechanism being screened for. Another factor is the economics of the screening process introduced into the production line. Optimal conditions and duration of a screening process will be a compromise of these two factors.

For example, failures due to ionic contamination have an activation energy of approximately 1.0eV. Therefore, a 15-hour stress at 125°C junction temperature would be the equivalent of approximately 90 days of operation at a junction temperature of 55°C. On the other hand, failures due to oxide defects have an activation energy of approximately 0.3eV, and a 15-hour stress at 125°C junction temperature would be the equivalent of approximately one week's operation at 55°C junction temperature. As indicated by this, the condition and duration of infant mortality screening would be a strong function of the allowable component failures, hence the system failure, in the field.

Empirical data, gathered over more than a year at NEC, indicates that early failure does occur after less than 4 hours of stress at 125°C ambient temperature. This fact is supported by the life test of the same lot, where the failure rate shows random distribution, as opposed to a decreasing failure rate which then runs into the random failure region.

NEC has adopted the initial infant mortality burn-in at 125°C as a standard production screening procedure. As a result, the field reliability of NEC devices is an order of magnitude higher than the goals set for NEC's integrated circuit products.

LIFE TESTS

The most significant difference between NEC's products and those of other integrated circuit manufacturers is the fact that NEC's have been prescreened for their infant mortality defects. The products delivered to customers are operating at the beginning of the random failure region of the life curve. The life test data also reflect this fact, as will be shown in the following sections.

The failure mechanism distribution from field failures, as previously shown in Figure 2, also contains a very low percentage due to infant mortality. The majority of failures are longterm life failures, and these can be eliminated by stringent process control. Usually, these failure mechanisms have low activation energy associated with them.

Another significant improvement devised by NEC is plastic encapsulation and passivation. As a result, NEC products show excellent reliability in both high humidity and high temperature environments. Following is life test data accumulated over more than a year for N-channel microprocessors and family products.

High temperature operating life test

This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature. For microprocessors and family products, the failure rate is 0.242 percent per 1000 hours at 125°C. This is equivalent to 0.0071 percent per 1000 hours in an operating environment of 55°C (Table 5).

TABLE 5. HIGH TEMPERATURE OPERATING LIFE TEST

NUMBER OF SAMPLES	NUMBER OF FAILURES AT				
	48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
3317	0	0	1	4	3

Total Number of Failures at 1K hrs = 8
Failure Rate at 1K hrs at 125°C = 0.242 % per 1K hrs
Projected Failure Rate at 55°C = 0.007 % per 1K hrs

High temperature and high humidity life test

This test is used to accelerate failure mechanisms by operating the devices at high temperature and high humidity. Leakage-related failures and device parameter drift are accelerated by this test. For microprocessors and family products, the failure rate is 0.091 percent per 1000 hours. This is equivalent to 0.0027 percent per 1000 hours in an operating environment of 55°C. The test conditions are T_a = 85°C and relative humidity (RH) = 80 % (Table 6).

TABLE 6. HIGH TEMPERATURE AND HIGH HUMIDITY LIFE TEST

NUMBER OF SAMPLES	NUMBER OF FAILURES AT				
	48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
2190	0	0	0	0	2

Total Number of Failures at 1K hrs = 2
Failure Rate at 1K hrs at 85°C 85 % RH = 0.091 % per 1K hrs
Projected Failure Rate at 55°C 60 % RH = 0.003 % per 1K hrs

High temperature storage life test

This test is effective in accelerating the failure mechanisms related to mechanical reliability problems and process instability. For microprocessors and family products, the failure rate is 0.207 percent per 1000 hours at 125°C. This is equivalent to 0.0061 percent per 1000 hours in an operating environment of 55°C (Table 7).

TABLE 7. HIGH TEMPERATURE STORAGE LIFE TEST

NUMBER OF SAMPLES	NUMBER OF FAILURES AT				
	48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
2410	0	0	0	1	4

Total Number of Failures at 1K hrs = 5
Failure Rate at 1K hrs at 125°C = 0.207 % per 1K hrs
Projected Failure Rate at 55°C = 0.006 % per 1K hrs

Pressure cooker test

This test is effective in accelerating failure mechanisms related to metalization corrosion due to moisture. The failure rate is 0.52 percent per 1000 hours at T_a = 125°C and 2.3 Atm at 100 percent humidity. This is equivalent to 0.0013 percent per 1000 hours at 55°C and an environment of 60 percent humiditiy (Table 8).

TABLE 8. PRESSURE COOKER TEST

NUMBER OF SAMPLES	NUMBER OF FAILURES AT				
	48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
1718	0	4	5	No Test Performed	

Total Number of Failures at 168 hrs = 9
Failure Rate at 125°C = 0.54 % per 1K hrs
Projected Failure Rate at 55°C = 0.001 % per 1K hrs

Life test data summary

Table 9 summarizes the liefe test results and projected failure rates in the normal operating environment. The failure rate shows random distribution as opposed to a decreasing failure rate. This is a result of infant mortality screening.

TABLE 9. LIFE TEST DATA

TEST ITEM	NUMBER OF SAMPLES	NUMBER OF FAILURES AT				TOTAL NUMBER OF FAILURES
		96 hrs	168 hrs	500 hrs	1K hrs	
High Temperature Life Test	3317	0	1	4	3	8
High Humidity Life Test	2190	0	0	0	2	2
High Temperature Storage Life Test	2410	0	0	1	4	5
Pressure Cooker Test	1718	4	5	*	*	9
Total	9635	4	6	5	9	24

Note: * = No test performed

The projected failure rate in the normal operating environment is calculated assuming that the average activation energy is 0.7eV.

Figure 3 shows the life distribution of NEC integrated circuits as a form of the Bathtub curve.

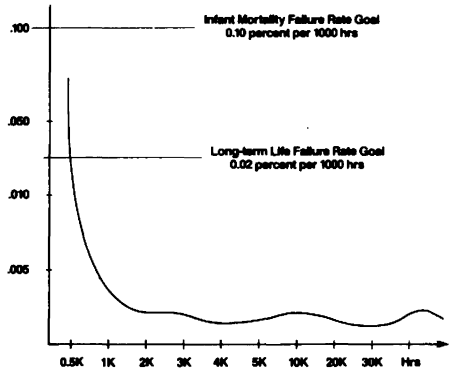


Figure 3. Plot of Life Test Results

This life test data shows improvements of approximately an order of magnitude better than NEC's goal. The hours of operation are equivalent to the normal operating environment. Wear-out failures, which had been the main target for reliability improvement, have also been significantly reduced. This result comes mainly from process improvements and stringent manufacturing process control.

NEC's main goal has been to improve reliability with respect to infant mortality and long-term life failures. This can be achieved by introducing an effective screening method for infant mortality and building quality into the product.

Thermal stress tests

Temperature cycling and thermal shock test the thermal compatibility of material and metal used to make integrated circuits. Table 10 lists the reliability test results of thermal stress tests.

TABLE 10. THERMAL STRESS RESULTS

TEST ITEM	NUMBER OF SAMPLES	NUMBER OF FAILURES
Soldering Heat Test T_a = 260°C for 10 seconds	1891	0
Temperature Cycle T_a = −65°C to +150°C, 10 cycles	1891	0
Thermal Shock Test T_a = 0°C to +100°C, 15 cycles	1891	0

Mechanical stress tests

In addition to the device life test, NEC performs mechanical stress tests to detect reliability problems related to the package, material, and device susceptibility to an extreme environment. Table 11 lists mechanical stress test results.

TABLE 11. MECHANICAL STRESS RESULTS

TEST ITEM		NUMBER OF SAMPLES	NUMBER OF FAILURES
Mechanical Shock Test	@ 15 kg, 3 axis	315	0
Vibration Test	@ 100 Hz to 2 kHz, 20 g	315	0
Constant Acceleration	@ 20 kg, 3 axis	315	0
Lead Fatigue Test	@ 250 gms	638	0
Solderability Test	@ 230°C for 5 seconds	638	0

BUILT-IN QUALITY AND RELIABILITY

As large-scale integration reaches even higher levels of density, simple quality inspections cannot assure adequate levels of product quality and reliability. In order to ensure the reliability of state-of-the-art, very large-scale integrated circuits, NEC has adopted another approch. Highest reliability and superior quality of a device can be achieved by building these characteristics into the product at each process step. NEC, therefore, has introduced the notion of Total Quality Control (TQC) into its entire semiconductor production line. Quality control is distributed into each process step and then all are summed to form a consolidated system.

APPROACHES TO TOTAL QUALITY CONTROL

First, the quality control function is embedded into each process. This method enables early detection of possible causes of failure and immediate feedback.

Second, the reliability and quality assurance policy is an integral part of the entire organization. This enables a companywide quality control activity. At NEC, everyone in the company is involved with the concept and methodology of Total Quality Control.

Third, there is an on-going research and development effort to set even higher standards of device quality and reliability.

Fourth, extensive failure analysis is performed periodically and corrective actions are taken as preventive measures. Process control is based on statistical data gathered from this analysis.

The goal is to maintain the superior product quality and reliability that has become synonymous with the NEC name. The new standard is continuously upgraded and the iterative process continues.

Implementation of distributed quality control

Building quality into a product requires early detection of possible cause of failure at each process step. Then, immediate feedback to remove the cause of failure is a must. A fixed station quality inspection is often lacking in immediate feedback. It is, therefore, necessary to distribute quality control functions to each process step, including the conceptual stage. NEC has implemented a distributed quality control function at each step of the process. Following is a breakdown of the significant steps:

- Product development phase
- Wafer processing
- Chip mounting and packaging
- Electrical testing and thermal aging
- Incoming material inspection

Product Development Phase: The product development phase includes conception of a product, review of the device proposal, organization and physical element design, engineering evaluation, and finally, transfer of the product to manufacturing. Quality and reliability are considered at every step. More significantly, at the design review stage and prior to product transfer, the quality and reliability requirements have to be examined and determined to be satisfactory. This often adds two to three months to the product development cycle. Building in high reliability, however, cannot be sacrificed.

Wafer Processing Stage Inspection: The in-process quality inspections that occur at the wafer fabrication stage are listed in Table 12.

TABLE 12. WAFER FABRICATION INSPECTION

PROCESS	INSPECTION ITEM
Wafer	Resistivity, Dimension, and Appearance, Lot Sampling Inspection
Mask	
Photo-Lithography	Alignment and Etching, 100 Percent Inspection
Cleaning	
Diffusion and Oxidation	Oxide Thickness, Sheet Resistivity, Lot Sampling Inspection
Metalization and Passivation	Thickness, V_{th}, C-V Characteristics, and Lot Sampling
Wafer Sort and Scribe	DC Parameters, 100 Percent Inspection
Die Sort	100 Percent Visual Inspection

Chip Mounting and Packaging: The in-process quality inspections that are done at the chip mounting and packaging stage are listed in Table 13.

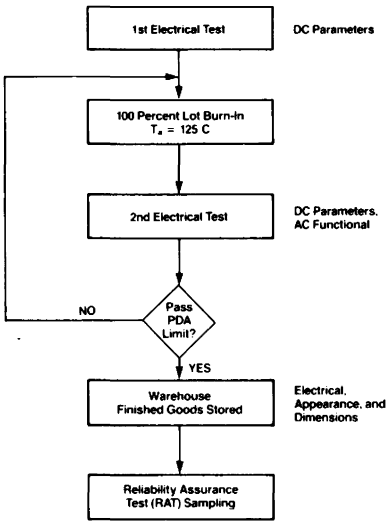
TABLE 13. CHIP MOUNTING AND PACKAGING INSPECTION

PROCESS	INSPECTION ITEM
Die	Incoming Material Inspection
Die Attach	Appearance, Lot Sampling Inspection
Wire Bonding	Bond Strength, Appearance, Lot Sampling
Packaging	100 Percent Appearance Inspection
Fine Leak*	Lot Sampling
Gross Leak*	100 Percent Inspection

Note: *For ceramic package devices only.

Electrical Testing and Screening: Electrical testing and infant mortality screening are performed at this stage. A flowchart of the process is depicted in Figure 4.

Figure 4. Electrical Testing and Screening



At the first electrical test, DC parameters are tested, according to the electrical specifications, on 100 percent of each lot. This is a prescreening prior to the infant mortality test. At the second electrical test, AC functional as well as DC parameter tests are performed on 100 percent of the subjected lot. If the percentage of defective units exceeds the limit, the lot is subjected to an additional burn-in. As this defective lot is being subjected to an additional burn-in, the defective units are undergoing a failure analysis, the results of which are then fed back into the process for corrective action.

Incoming Material Inspection: Prior to warehouse storage, lots are subjected to an incoming inspection according to the following sampling plan:

- Electrical test: DC parameters LTPD 3 %
  Functional test LTPD 3 %
- Appearance LTPD 3 %

Reliability assurance test

Samples are continually taken from the warehouse and subjected to monthly reliability tests as discussed in the previous section. They are taken from similar process groups so that it can be assumed that any device is representative of the reliability of that group.

In-process screening

Perhaps the most significant preventive measure that NEC has implemented is the introduction of 100 percent burn-in as an integral part of the standard production process. Most of the potential infant failures are effectively screened from every lot, thereby improving reliability. Assuming average activation energy of 0.7eV, burn-in at T_a = 125°C for four hours is equivalent to a week's operation in a normal operating environment. This appears to be ample time for accelerating the time-to-failure mechanisms for early failures.

Process automation, as previously mentioned, has also contributed a great deal in improving reliability. Since its introduction, assembly related failure mechanisms have been substantially reduced. And, in combination with in-process screening and materials improvement, it has helped establish quality and reliability above NEC's initial goals.

SUMMARY AND CONCLUSION

As has been discussed, building quality and reliability into products is the most efficient way to ensure product reliability. NEC's approach of distributing quality control functions to process steps, then forming a consolidated quality control system, has produced superior quality and excellent reliability.

Prescreening, introduced as an integral part of large-scale integrated circuit production, has been a major facor in improving reliability. The most recent year's production clearly demonstrates continuation of NEC's high reliability and the effectiveness of this method.

Reliability Assurance Tests (RATs), performed monthly, have ensured high outgoing quality levels. The combination of building quality into products, effective prescreening of potential failures, and the reliability assurance test has established a singularly high standard of quality and reliability for NEC's large-scale integrated circuits.

With a companywide quality control program, NEC is committed to building superior quality and highest reliability into all its products. Through continuous research and development activities, extensive failure analysis, and process improvements, a higher standard of quality and reliability will continuously be set and maintained.

CHAPTER 3

THE μCOM84 CMOS FAMILY

μPD80C48/μPD80C35/μPD48
μPD80C49/μPD80C39/μPD49
μPD80C49H/μPD80C39H/μPD49H
μPD80C42
μPD80C50H/μPD80C40H

GENERAL INFORMATION

CMOS MICROCOMPUTER SELECTION GUIDE

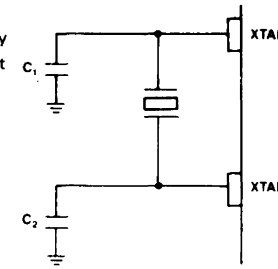
SINGLE CHIP 8-BIT MICROCOMPUTERS

DEVICE	SPECIAL FEATURES	ROM	RAM	I/O	PROCESS	CYCLE	SUPPLY VOLTAGE	PINS
μPD80C35	CMOS 8035	External	64x8	27	CMOS	6 MHz	+2.5 to 6	40/52
μPD80C48	CMOS 8048	1024x8	64x8	27	CMOS	6 MHz	+2.5 to 6	40/44/52
μPD80C39	CMOS 8039	External	128x8	27	CMOS	8 MHz	+2.5 to 6	40/52
μPD80C39H	CMOS 8039H	External	128x8	27	CMOS	12 MHz	+2.5 to 6	40
μPD80C49	CMOS 8049	2048x8	128x8	27	CMOS	8 MHz	+2.5 to 6	40/44/52
μPD80C49H	CMOS 8049H	2048x8	128x8	27	CMOS	12 MHz	+2.5 to 6	40/44
μPD80C49H (S)	CMOS 8049H (S)*	2048x8	128x8	27	CMOS	10 MHz	+2.5 to 6	40
μPD80C42	INTERFACE WITH SLAVE BUS	2048x8	128x8	18	CMOS	12 MHz	+2.5 to +6	40
μPD80C40H	LARGE MEMORY	4096x8	256x8	16	CMOS	12 MHz	2.5 to +6	40
μPD80C50H	LARGE MEMORY	4096x8	256x8	16	CMOS	12 MHz	2.5 to +6	40/44

NOTE SPECIAL S GRADE VERSION

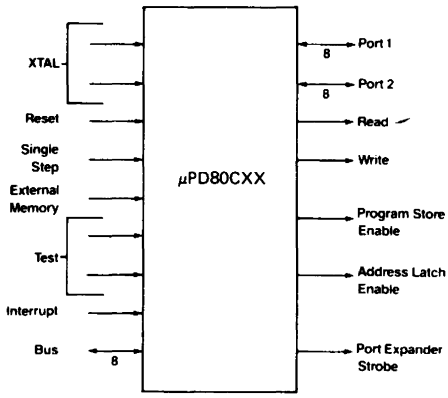
*	NORMAL	(S) GRADE
1st electrical test	at room temp	at 110°C
burn in	4 hours	16 hours
2nd electrical test	at room temp	at room temp

Crystal Resonator Frequency Reference Circuit

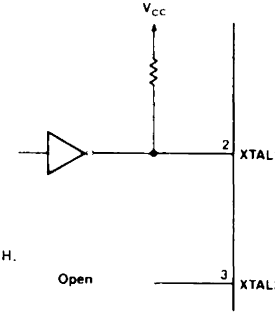


① Crystal oscillator constants of f_{OSC} = 6 MHz / R_{max} = 50Ω / C_L = 16 ± 0.2 pF / P = 1 ± 0.2 mW
② Operating frequency less than 4 MHz / $0 < C_1 \leq 20$ pF / $0 < C_2 \leq 20$ pF / $|C_2 - C_1| \leq 10$ pF
③ Operating frequency more than 4 MHz / $0 < C_1 \leq 10$ pF / $0 < C_2 \leq 10$ pF / $|C_2 - C_1| \leq 5$ pF

MAJOR INPUT AND OUTPUT SIGNALS



External Clock Frequency Reference Circuit



Note: A minimum voltage of V_{CC}-1 is required for XTAL1 to go HIGH.

INSTRUCTION SET

INSTRUCTION SET SYMBOL DEFINITIONS

SYMBOL	DESCRIPTION
A	Accumulator
AC	Auxiliary Carry Flag
addr	Program or data memory address (a_0–a_7) or (a_0–a_{10})
b	Accumulator bit (b = 0–7)
BS	Bank Swith
BUS	Bus
C	Carry Flag
CLK	Clock
CNT	Counter
data	8-bit binary data (d_0–d_7)
DBF	Memory Bank Flip-Flop
F0, F1	Flag 0, Flag 1
INT	Interrupt pin
	Indicates the hex number of the specified register or port
PC	Program Counter
P_p	Port 1, Port 2, or Port 4–7 ($_p$ = 1, 2, or 4–7)
PSW	Program Status Word
R_r	Register R_0–R_7 ($_r$ = 0–7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T0, T1	Test 0, Test 1 pin
#	Immediate data indication
@	Indirect address indication
x	Indicates the hex number corresponding to the accumulator bit or page number specified in the operand
(x)	Contents of RAM
((x))	Contents of memory addressed by (x)
←	Transfer direction, result
∧	Logical product (logical AND)
∨	Logical sum (logical OR)
∀	Exclusive OR
–	Complement

Mnemonic	Function	Description	Hex Code	Instruction Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Accumulator													
ADD A, # data	(A) ← (A) + data	Adds immediate data d_0–d_7 to the accumulator. Sets or clears both carry flags. 2	03	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADD A, R$_r$	(A) ← (A) + (R$_r$) r = 0–7	Adds the contents of register R$_r$ to the accumulator. Sets or clears both carry flags. 2	6n	0	1	1	0	1	r	r	r	1	1
ADD A, @ R$_r$	(A) ← (A) + ((R$_r$)) r = 0–1	Adds the contents of the internal data memory location specified by bits 0–5 of register R$_r$ to the accumulator. Sets or clears both carry flags. 2	6n	0	1	1	0	0	0	0	r	1	1
ADDC A, # data	(A) ← (A) + data + (C)	Adds, with carry, immediate data d_0–d_7 to the accumulator. Sets or clears both carry flags. 2	13	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADDC A, R$_r$	(A) ← (A) + (R$_r$) + (C) r = 0–7	Adds, with carry, the contents of register R$_r$ to the accumulator. Sets or clears both carry flags. 2	7n	0	1	1	1	1	r	r	r	1	1
ADDC A, @ R$_r$	(A) ← (A) + ((R$_r$)) + (C) r = 0–1	Adds, with carry, the contents of the internal data memory location specified by bits 0–5 of register R$_r$, to the accumulator. Sets or clears both carry flags. 2	7n	0	1	1	1	0	0	0	r	1	1
ANL A, # data	(A) ← (A)∧data	Takes the logical product (logical AND) of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	53	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ANL A, R$_r$	(A) ← (A)∧(R$_r$) r = 0–7	Takes the logical product (logical AND) of the contents of register R$_r$ and the accumulator, and stores the result in the accumulator.	5n	0	1	0	1	1	r	r	r	1	1
ANL A, @ R$_r$	(A) ← (A)∧((R$_r$)) r = 0–1	Takes the logical product (logical AND) of the contents of the internal data memory location specified by bits 0–5 of register R$_r$, and the accumulator, and stores the result in the accumulator.	5n	0	1	0	1	0	0	0	r	1	1
CPL A	(A) ← $\overline{(A)}$	Takes the complement of the contents of the accumulator.	37	0	0	1	1	0	1	1	1	1	1
CLR A	(A) ← 0	Clears the contents of the accumulator.	27	0	0	1	0	0	1	1	1	1	1
DA A		Converts the contents of the accumulator to BCD. Sets or clears the carry flags. When the lower 4 bits (A_{0-3}) are greater than 9, or if the Auxiliary Carry Flag has been set, adds 6 to A_{0-3}. When the upper 4 bits (A_{4-7}) are greater than 9 or if the Carry Flag (C) has been set, adds 6 to A_{4-7}. If an overflow occurs at this point, C is set. 2	57	0	1	0	1	0	1	1	1	1	1
DEC A	(A) ← (A) – 1	Decrements the contents of the accumulator by 1.	07	0	0	0	0	0	1	1	1	1	1
INC A	(A) ← (A) + 1	Increments the contents of the accumulator by 1.	17	0	0	0	1	0	1	1	1	1	1
ORL A, # data	(A) ← (A)∨data	Takes the logical sum (logical OR) of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	43	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ORL A, R$_r$	(A) ← (A)∨(R$_r$) r = 0–7	Takes the logical sum (logical OR) of register R$_r$ and the contents of the accumulator, and stores the result in the accumulator.	4n	0	1	0	0	1	r	r	r	1	1
ORL A, @ R$_r$	(A) ← (A)∨((R$_r$)) r = 0–1	Takes the logical sum (logical OR) of the contents of the internal data memory location specified by bits 0–5 in register R$_r$, and the contents of the accumulator, and stores the result in the accumulator.	4n	0	1	0	0	0	0	0	r	1	1
RL A	(Ab + 1) ← (Ab) (A_0) ← (A_7) b = 0–6	Rotates the contents of the accumulator one bit to the left. The MSB is rotated into the LSB.	E7	1	1	1	0	0	1	1	1	1	1
RLC A	(Ab + 1) ← (Ab) (A_0) ← (C) (C) ← (A_7) b = 0–6	Rotates the contents of the accumulator one bit to the left through carry.	F7	1	1	1	1	0	1	1	1	1	1
RR A	(Ab) ← (Ab + 1) (A_7) ← (A_0) b = 0–6	Rotates the contents of the accumulator one bit to the right. The LSB is rotated into the MSB.	77	0	1	1	1	0	1	1	1	1	1
RRC A	(Ab) ← (Ab + 1) (A_7) ← (C) (C) ← (A_0) b = 0–6	Rotates the contents of the accumulator one bit to the right through carry.	67	0	1	1	0	0	1	1	1	1	1
SWAP A	(A_{4-7}) ↔ (A_{0-3})	Exchanges the contents of the lower 4 bits of the accumulator with the upper 4 bits of the accumulator.	47	0	1	0	0	0	1	1	1	1	1
XRL A, # data	(A) ← (A)⊻data	Takes the exclusive OR of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	D3	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
XRL A, R$_r$	(A) ← (A)⊻(R$_r$) r = 0–7	Takes the exclusive OR of the contents of register R$_r$ and the accumulator, and stores the result in the accumulator.	Dn	1	1	0	1	1	r	r	r	1	1
XRL A, @ R$_r$	(A) ← (A)⊻((R$_r$)) r = 0–1	Takes the exclusive OR of the contents of the location in data memory specified by bits 0–5 in register R$_r$, and the accumulator, and stores the result in the accumulator.	Dn	1	1	0	1	0	0	0	r	1	1
Branch													
DJNZ R$_r$, addr	(R$_r$) ← (R$_r$) – 1 If (R$_r$) ≠ 0, then (PC$_{0-7}$) ← addr r = 0–7	Decrements the contents of register R$_r$ by 1, and if the result is not equal to 0, jumps to the address indicated by a_0–a_7.	En	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2
JBb addr	(PC$_{0-7}$) ← addr if b = 1 (PC) = (PC) + 2 if b = 0	Jumps to the address specified by a_0–a_7 if the bit in the accumulator specified by b_0–b_2 is set.	x2	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Branch (Cont.)													
JC addr	$(PC_{0-7}) \leftarrow$ addr if C = 1 $(PC) \leftarrow (PC) + 2$ if C = 0	Jumps to the address specified by a_0-a_7 if the Carry Flag is set.	F6	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF0 addr	$(PC_{0-7}) \leftarrow$ addr if F0 = 1 $(PC) \leftarrow (PC) + 2$ if F0 = 0	Jumps to the address specified by a_0-a_7 if F0 is set.	B6	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF1 addr	$(PC_{0-7}) \leftarrow$ addr if F1 = 1 $(PC) \leftarrow (PC) + 2$ if F1 = 0	Jumps to the address specified by a_0-a_7 if F1 is set.	76	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JMP addr	$(PC_{8-10}) \leftarrow$ addr$_{8-10}$ $(PC_{0-7}) \leftarrow$ addr$_{0-7}$ $(PC_{11}) \leftarrow$ DBF	Jumps directly to the address specified by a_0-a_{10} and the DBF.	x4④	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
JMPP (@ A	$(PC_{0-7}) \leftarrow ((A))$	Replaces the lower 8 bits of the Program Counter with the contents of program memory specified by the contents of the accumulator, producing a jump to the specified address within the current page.	B3	1	0	1	1	0	0	1	1	2	1
JNC addr	$(PC_{0-7}) \leftarrow$ addr if C = 0 $(PC) \leftarrow (PC) + 2$ if C = 1	Jumps to the address specified by a_0-a_7 if the Carry Flag is not set.	E6	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNI addr	$(PC_{0-7}) \leftarrow$ addr if I = 0 $(PC) \leftarrow (PC) + 2$ if I = 1	Jumps to the address specified by a_0-a_7 if the Interrupt Flag is not set.	86	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT0 addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 0 $(PC) \leftarrow (PC) + 2$ if T0 = 1	Jumps to the address specified by a_0-a_7 if Test 0 is LOW.	26	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT1 addr	$(PC_{0-7}) \leftarrow$ addr if T1 = 0 $(PC) \leftarrow (PC) + 2$ if T1 = 1	Jumps to the address specified by a_0-a_7 if Test 1 is LOW.	46	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNZ addr	$(PC_{0-7}) \leftarrow$ addr if A ≠ 0 $(PC) \leftarrow (PC) + 2$ if A = 0	Jumps to the address specified by a_0-a_7 if the contents of the accumulator are not equal to 0.	96	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JTF addr	$(PC_{0-7}) \leftarrow$ addr if TF = 1 $(PC) \leftarrow (PC) + 2$ if TF = 0	Jumps to the address specified by a_0-a_7 if the Timer Flag is set. The Timer Flag is cleared after the instruction is executed.	16	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT0 addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 1 $(PC) \leftarrow (PC) + 2$ if T0 = 0	Jumps to the address specified by a_0-a_7 if Test 0 is HIGH.	36	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT1 addr	$(PC_{0-7}) \leftarrow$ addr if T1 = 1 $(PC) \leftarrow (PC) + 2$ if T1 = 0	Jumps to the address specified by a_0-a_7 if Test 1 is HIGH.	56	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JZ	$(PC_{0-7}) \leftarrow$ addr if A = 0 $(PC) \leftarrow (PC) + 2$ if A = 1	Jumps to the address specified by a_0-a_7 if the contents of the accumulator are equal to 0.	C6	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
Control													
EN I		Enables external interrupts. When external interrupts are enabled, a low-level input to the INT pin causes the processor to vector to the interrupt service routine.	05	0	0	0	0	0	1	0	1	1	1
DIS I		Disables external interrupts. When external interrupts are disabled, low-level inputs to the INT pin have no effect on program execution.	15	0	0	0	1	0	1	0	1	1	1
ENT0 CLK		Enables clock output to pin T0.	75	0	1	1	1	0	1	0	1	1	1
SEL MB0	(DBF) ← 0	Clears the Memory Bank Flip-Flop, selecting Program Memory Bank 0 [program memory addresses $0-2047_{(10)}$]. Clears PC_{11} after the next JMP or CALL instruction.	E5	1	1	1	0	0	1	0	1	1	1
SEL MB1	(DBF) ← 1	Sets the Memory Bank Flip-Flop, selecting Program Memory Bank 1 [program memory addresses $2048-4095_{(10)}$]. Sets PC_{11} after the next JMP or CALL instruction.	F5	1	1	1	1	0	1	0	1	1	1
SEL RB0	(BS) ← 0	Selects Data Memory Bank 0 by clearing bit 4 (Bank Switch) of the PSW. Specifies data memory addresses $0-7_{(10)}$ as registers 0–7 of Data Memory Bank 0.	C5	1	1	0	0	0	1	0	1	1	1
SEL RB1	(BS) ← 1	Selects Data Memory Bank 1 by setting bit 4 (Bank Switch) of the PSW. Specifies data memory $24-31_{(10)}$ as registers 0–7 of Data Memory Bank 1.	D5	1	1	0	1	0	1	0	1	1	1
HALT		Initiates Halt mode.	01	0	0	0	0	0	0	0	1	1	1
STOP	(not all devices)	Initiates Software Stop mode	82	1	0	0	0	0	0	1	0	1	1
Data Moves													
MOV A, # data	(A) ← data	Moves immediate data d_0-d_7 into the accumulator.	23	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
MOV A, R,	(A) ← (R_r) r = 0–7	Moves the contents of register R_r into the accumulator.	Fn④	1	1	1	1	1	r	r	r	1	1
MOV A, @ R,	(A) ← ((R_r)) r = 0–1	Moves the contents of internal data memory specified by bits 0–5 in register R_r, into the accumulator.	Fn④	1	1	1	1	0	0	0	r	1	1
MOV A, PSW	(A) ← (PSW)	Moves the contents of the Program Status Word into the accumulator.	C7	1	1	0	0	0	1	1	1	1	1
MOV R_r, # data	(R_r) ← data r = 0–7	Moves immediate data d_0-d_7 into register R_r.	Bn④	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2
MOV R_r, A	(R_r) ← (A) r = 0–7	Moves the contents of the accumulator into register R_r.	An④	1	0	1	0	1	r	r	r	1	1
MOV @ R_r, A	((R_r)) ← (A) r = 0–1	Moves the contents of the accumulator into the data memory location specified by bits 0–5 in register R_r.	An④	1	0	1	0	0	0	0	r	1	1
MOV @ R_r, # data	((R_r)) ← data r = 0–1	Moves immediate data d_0-d_7 into the data memory location specified by bits 0–5 in register R_r.	Bn④	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2
MOV PSW, A	(PSW) ← (A)	Moves the contents of the accumulator into the Program Status Word.	D7	1	1	0	1	0	1	1	1	1	1

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Data Moves (Cont.)													
MOVP A, @ A	$(PC_{8-7}) \leftarrow (A)$ $(A) \leftarrow ((PC))$	Moves the contents of the program memory location specified by PC_{8-11} concatenated with the contents of the accumulator, into the accumulator.	A3	1	0	1	0	0	0	1	1	2	1
MOVP3 A, @ A	$(PC_{8-7}) \leftarrow (A)$ $(PC_{8-11}) \leftarrow 0011$ $(A) \leftarrow ((PC))$	Moves the contents of the program memory location specified by 0011 (PC_{8-11}, page 3 of Program Memory Bank 0) and the contents of the accumulator, into the accumulator.	E3	1	1	1	0	0	0	1	1	2	1
MOVX A, @ R	$(A) \leftarrow ((R_r))$ $r = 0-1$	Moves the contents of the external data memory location specified by register R_r, into the accumulator.	8nⓇ	1	0	0	0	0	0	0	r	2	1
MOVX @ R, A	$((R_r)) \leftarrow (A)$ $r = 0-1$	Moves the contents of the accumulator into the external data memory location specified by register R_r.	9nⓇ	1	0	0	1	0	0	0	r	2	1
XCH A, R,	$(A) \leftrightarrow (R_r)$ $r = 0-7$	Exchanges the contents of the accumulator and register R_r.	2nⓇ	0	0	1	0	1	r	r	r	1	1
XCH A, @ R,	$(A) \leftrightarrow ((R_r))$ $r = 0-1$	Exchanges the contents of the accumulator and the contents of the data memory location specified by bits 0–5 in register R_r.	2nⓇ	0	0	1	0	0	0	0	r	1	1
XCHD A, @ R_r	$(A_{3-0}) \leftrightarrow ((R_{r_{3-0}}))$ $r = 0-1$	Exchanges the contents of the lower 4 bits of the accumulator with the contents of the lower 4 bits of the internal data memory location specified by bits 0–5 in register R_r.	3nⓇ	0	0	1	1	0	0	0	r	1	1
Flags													
CPL C	$(C) \leftarrow \overline{(C)}$	Takes the complement of the Carry bit.	A7	1	0	1	0	0	1	1	1	1	1
CPL F0	$(F0) \leftarrow \overline{(F0)}$	Takes the complement of Flag 0.	95	1	0	0	1	0	1	0	1	1	1
CPL F1	$(F1) \leftarrow \overline{(F1)}$	Takes the complement of Flag 1.	B5	1	0	1	1	0	1	0	1	1	1
CLR C	$(C) \leftarrow 0$	Clears the Carry bit.	97	1	0	0	1	0	1	1	1	1	1
CLR F0	$(F0) \leftarrow 0$	Clears Flag 0.	85	1	0	0	0	0	1	0	1	1	1
CLR F1	$(F1) \leftarrow 0$	Clears Flag 1.	A5	1	0	1	0	0	1	0	1	1	1
Input/Output													
ANL BUS, # data	$(BUS) \leftarrow (BUS) \wedge data$	Takes the logical AND of the contents of the bus and immediate data d_0–d_7, and sends the result to the bus.	98	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ANL P_p, # data	$(P_p) \leftarrow (P_p) \wedge data$ $p = 1-2$	Takes the logical AND of the contents of designated port P_p and immediate data d_0–d_7, and sends the result to port P_p for output.	9nⓈ	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
ANLD P_p, A	$(P_p) \leftarrow (P_p) \wedge (A_{3-0})$ $p = 4-7$	Takes the logical AND of the contents of designated port P_p and the lower 4 bits of the accumulator, and sends the result to port P_p for output.	9nⓈ	1	0	0	1	1	1	p	p	2	1
IN A, P_p	$(A) \leftarrow (P_p)$ $p = 1-2$	Loads the accumulator with the contents of designated port P_p.	0nⓈ	0	0	0	0	1	0	p	p	2	1
INS A, BUS	$(A) \leftarrow (BUS)$	Loads the contents of the bus into the accumulator on the rising edge of RD.	08	0	0	0	0	1	0	0	0	2	1
MOVD A, P_p	$(A_{3-0}) \leftarrow (P_p)$ $(A_{7-7}) \leftarrow 0$ $p = 4-7$	Moves the contents of designated port P_p to the lower 4 bits of the accumulator, and clears the upper 4 bits.	0nⓈ	0	0	0	0	1	1	p	p	2	1
MOVD P_p, A	$(P_p) \leftarrow (A_{3-0})$ $p = 4-7$	Moves the lower 4 bits of the accumulator to designated port P_p. The upper 4 bits of the accumulator are not changed.	3nⓈ	0	0	1	1	1	1	p	p	2	1
ORL BUS, # data	$(BUS) \leftarrow (BUS) \vee data$	Takes the logical OR of the contents of the bus and immediate data d_0–d_7, and sends the result to the bus.	88	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ORLD P_p, A	$(P_p) \leftarrow (P_p) \vee (A_{3-0})$ $p = 4-7$	Takes the logical OR of the contents of designated port P_p and the lower 4 bits of the accumulator, and sends the result to port P_p for output.	8nⓈ	1	0	0	0	1	1	p	p	2	1
ORL P_p, # data	$(P_p) \leftarrow (P_p) \vee data$ $p = 1-2$	Takes the logical OR of the contents of designated port P_p and immediate data d_0–d_7, and sends the result to port P_p for output.	9nⓈ	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
OUTL BUS, A	$(BUS) \leftarrow (A)$	Latches the contents of the accumulator onto the bus on the rising edge of $\overline{WR}$. **Note:** Never use the OUTL BUS instruction when using external program memory, as this will permanently latch the bus.	02	0	0	0	0	0	0	1	0	2	1
OUTL P_p, A	$(P_p) \leftarrow (A)$ $p = 1-2$	Latches the contents of the accumulator into designated port P_p for output.	3nⓈ	0	0	1	1	1	0	p	p	2	1
Registers													
DEC R,	$(R_r) \leftarrow (R_r) - 1$ $r = 0-7$	Decrements the contents of register R_r by 1.	CnⒺ	1	1	0	0	1	r	r	r	1	1
INC R,	$(R_r) \leftarrow (R_r) + 1$ $r = 0-7$	Increments the contents of register R_r by 1.	1nⒺ	0	0	0	1	1	r	r	r	1	1
INC @ R,	$((R_r)) \leftarrow ((R_r)) + 1$ $r = 0-1$	Increments by 1 the contents of the data memory location specified by bits 0–5 in register R_r.	1nⒺ	0	0	0	1	0	0	0	r	1	1

Mnemonic	Function	Description	Hex Code	Instruction Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Subroutine													
CALL addr	((SP)) ← (PC), (PSW$_{4-7}$) (SP) ← (SP) + 1 (PC$_{8-10}$) ← addr$_{8-10}$ (PC$_{0-7}$) ← addr$_{0-7}$ (PC$_{11}$) ← DBF	Stores the contents of the Program Counter and the upper 4 bits of the PSW in the address indicated by the Stack Pointer, and increments the contents of the Stack Pointer, calling the subroutine specified by address a_0–a_{10} and the DBF.	x4④	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
RET	(SP) ← (SP) − 1 (PC) ← ((SP))	Decrements the contents of the Stack Pointer by 1 and stores, in the Program Counter, the contents of the location specified by the Stack Pointer, executing a return from subroutine without restoring the PSW.	83	1	0	0	0	0	0	1	1	2	1
RETR	(SP) ← (SP) − 1 (PC) ← ((SP)) (PSW$_{4-7}$) ← ((SP))	Decrements the contents of the Stack Pointer by 1 and stores, in the Program Counter, the contents of the upper 4 bits of the PSW and the contents of the location specified by the Stack Pointer, executing a return from subroutine with restoration of the PSW.	93	1	0	0	1	0	0	1	1	2	1
Timer/Counter													
EN TCNTI		Enables internal interrupt of timer/event counter. If an overflow condition occurs, then an interrupt will be generated.	25	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disables internal interrupt of timer/event counter.	35	0	0	1	1	0	1	0	1	1	1
MOV A, T	(A) ← (T)	Moves the contents of the timer/counter into the accumulator.	42	0	1	0	0	0	0	1	0	1	1
MOV T, A	(T) ← (A)	Moves the contents of the accumulator into the timer/counter.	62	0	1	1	0	0	0	1	0	1	1
STOP TCNT		Stops the operation of the timer/event counter.	65	0	1	1	0	0	1	0	1	1	1
STRT CNT		Starts the event counter operation of the timer/counter when T1 changes from a low-level input to a high-level input.	45	0	1	0	0	0	1	0	1	1	1
STRT T		Starts the timer operation of the timer/counter. The timer is incremented every 32 machine cycles.	55	0	1	0	1	0	1	0	1	1	1
Miscellaneous													
NOP		Uses one machine cycle without performing any operation.	00	0	0	0	0	0	0	0	0	1	1

Notes: ① Binary instruction code designations a_p and b_p represent encoded values of the lowest-order bit value of specified registers and ports, respectively.

② Execution of the ADD, ADDC, and DA instructions affect the carry flags, which are not shown in the respective function equations. These instructions set the carry flags when there is an overflow in the accumulator (the Auxiliary Carry Flag is set when there is an overflow of bit 3 of the accumulator) and clear the carry flags when there is no overflow. Flags that are specifically addressed by flag instructions are shown in the function equations for those instructions.

③ References to addresses and data are specified in byte 1 and/or 2 in the opcode of the corresponding instruction.

④ The hex value of n for specific registers is as follows:

a) Direct addressing

R_0: n = 8 R_2: n = A R_4: n = C R_6: n = E
R_1: n = 9 R_3: n = B R_5: n = D R_7: n = F

b) Indirect addressing

@R_0: n = 0 @R_1: n = 1

⑤ The hex value of n for specific ports is as follows:

P_1: n = 9 P_4: n = C P_6: n = E
P_2: n = A P_5: n = D P_7: n = F

⑥ The hex value of x for specific accumulator or address bits is as follows:

a) JBb instruction

B_0: x = 1 B_2: x = 5 B_4: x = 9 B_6: x = D
B_1: x = 3 B_3: x = 7 B_5: x = B B_7: x = F

b) JMP instruction

Page 0: x = 0 Page 2: x = 4 Page 4: x = 8 Page 6: x = C
Page 1: x = 2 Page 3: x = 6 Page 5: x = A Page 7: x = E

c) CALL instruction

Page 0: x = 1 Page 2: x = 5 Page 4: x = 9 Page 6: x = D
Page 1: x = 3 Page 3: x = 7 Page 5: x = B Page 7: x = F

CMOS 8-BIT
SINGLE-CHIP
MICROCOMPUTER

CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

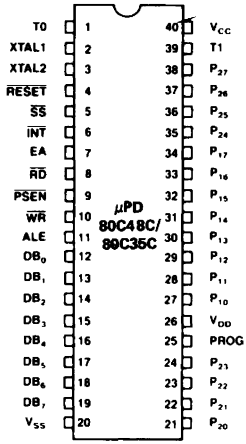
The NEC μPD80C48 is a true stand-alone 8-bit microcomputer fabricated using CMOS technology. All of the functional blocks necessary for an integrated microcomputer are incorporated, including a 1K-byte ROM, a 64-byte RAM, 27 I/O lines, an 8-bit timer/event counter, and a clock generator. This integrated capability permits use in stand-alone applications. For designs requiring extra capability, the μPD80C48 can be expanded using peripherals and memory compatible with industry-standard 8080A/8085A processors. A version of the μPD80C48 without ROM is offered by the μPD80C35.

Providing compatibility with industry-standard 8048, 8748, and 8035 processors, the μPD80C48 features significant savings in power consumption. In addition to the power savings gained through CMOS technology, the μPD80C48 is distinct in offering two standby modes (Halt mode and Stop mode) to further minimize power drain.

FEATURES

- 8-bit CPU with ROM, RAM, and I/O on a single chip
- Hardware/software-compatible with industry-standard 8048, 8748, and 8035 processors
- 1K x 8 ROM
- 64 x 8 RAM
- 27 I/O lines
- 2.5 μs cycle time (6 MHz crystal)
- All instructions executable in 1 or 2 cycles
- 97 instructions: 70 percent are single-byte instructions
- Internal timer/event counter
- 2 interrupts (an external interrupt and a timer interrupt)
- Easily expandable memory and I/O
- Bus compatible with 8080A/8085A peripherals
- Power-efficient CMOS technology requiring a single +2.5V to +6V power supply
- Available in 40-pin DIP, 44-pin flat pack, and 52-pin flat pack
- Halt mode
  - 1 mA typical supply current
  - Maintenance of internal logic values and control states
  - Mode initialization via HALT instruction
  - Mode release via external interrupt or reset
- Stop mode
  - 1 μA typical supply current
  - Disabling of internal clock generation and internal logic
  - Maintenance of RAM contents
  - Mode initialization via hardware (V_{DD})
  - Mode release via reset

PIN CONFIGURATION μPD80C48C/μPD80C35C (40 PIN PLASTIC DIP)



PIN IDENTIFICATION

A.
μPD80C48C/μPD80C35C
(40 PIN PLASTIC DIP)

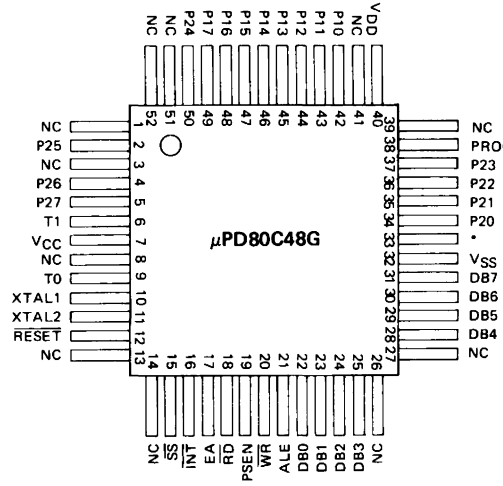
B.
μPD80C48G/μPD80C35G
(52 PIN PLASTIC
FLAT PACK)

C.
μPD48G
(44 PIN PLASTIC
FLAT PACK)

PIN					FUNCTION
C.	B.	A.	SYMBOL	NAME	
18	9	1	T0	Test 0	Testable input using conditional jump instructions JT0 and JNT0. Also enables clock output via the ENT0 CLK instruction.
19	10	2	XTAL1	Crystal 1	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. May also be used as an input for external clock signals. (Non-TTL-compatible V_{IH}.)
20	11	3	XTAL2	Crystal 2	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. (Non-TTL-compatible V_{IH}.)
22	12	4	$\overline{RESET}$	Reset	Active-low input line that initializes the processor. Also used to release both the Halt and Stop modes. ①
23	15	5	$\overline{SS}$	Single Step	Active-low input line, that, in conjunction with ALE, causes the processor to single-step through a program one instruction at a time.
24	16	6	$\overline{INT}$	Interrupt	Active-low input line that causes an interrupt if an enable instruction has been executed. A reset disables the interrupt. May be used as a testable input with a conditional jump instruction. Can also be used to release the Halt mode.
25	17	7	EA	External Access	Input line that inhibits internal program memory fetches and initiates access of external program memory. Essential for system testing and may also be used for program debugging.
26	18	8	$\overline{RD}$	Read	Active-low output strobe line that is used to read data from external data memory.
27	19	9	$\overline{PSEN}$	Program Store Enable	Active-low output line that is used to fetch instructions from external program memory.
28	20	10	$\overline{WR}$	Write	Active-low output strobe line that is used to write data into external data memory.
29	21	11	ALE	Address Latch Enable	Output line for address latch enable. At the falling edge of ALE, the address of either external data memory or external program memory is available on the bus.
30-37	22-25, 28-31	12-19	DB_0-DB_7	Bus	These I/O lines constitute an 8-bit bidirectional data/address bus. Synchronous read and write operations can be performed on this bus using $\overline{RD}$ and $\overline{WR}$ signals. Data driven out on the bus by an OUTL BUS instruction is statically latched. The address of external memory is available on the bus at the falling edge of ALE when reading from external program memory or writing to and reading from external data memory. During external program memory fetches, the least-significant 8 bits of the external program memory address are driven out on the bus and the addressed instruction is fetched using $\overline{PSEN}$. When no external memory is used, the bus can serve as a true bidirectional 8-bit port. Information is strobed in or out by the $\overline{RD}$ and $\overline{WR}$ signals.
38	32	20	V_{SS}	Ground	Ground potential.
39-42, 11, 13-15	34-37, 50, 2, 4, 5	21-24, 35-38	P_{20}-P_{27}	Port 2	These lines constitute Port 2, an 8-bit quasi-bidirectional port. During external program memory fetches P_{20}-P_{23} output the most-significant 4 bits of the external program memory address. Lines P_{20}-P_{23} can also be used as a 4-bit I/O expander bus to interface with the optional μPD82C43 I/O expander.
43	38	25	PROG	Program Pulse	This line is used as an output strobe when interfacing with the optional μPD82C43 I/O expander.
1	40	26	V_{DD}	Oscillator Control Voltage Line	This input line is used to control oscillator stopping and restarting in Stop mode. Stop mode is enabled by forcing V_{DD} Low during a reset.
2- 7, 9-10	42-49	27-34	P_{10}-P_{17}	Port 1	These lines constitute Port 1, an 8-bit, generalpurpose quasi-bidirectional port.
16	6	39	T1	Test 1	Testable input using conditional jump instructions JT1 and JNT1. Can also be used as the timer/counter input line via the STRT CNT instruction.
17	7	40	V_{CC}	Primary Power Supply	Power supply. V_{CC} must be between +2.5V to +6V for normal operation. In Stop mode, V_{CC} must be at least +2V to ensure data retention.

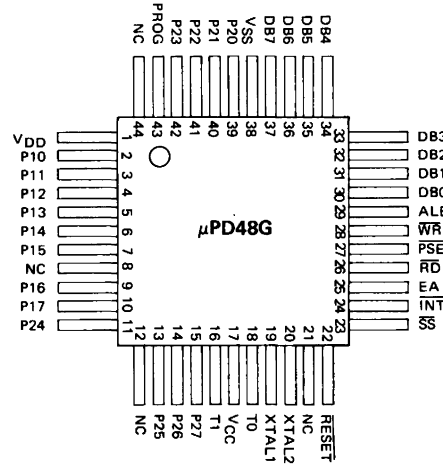
Note: ①The pulse width of $\overline{RESET}$ must be a minimum of 5 machine cycles in length following oscillator stabilization to reinitialize the processor and stabilize CPU operation. At power-up, the states of the output lines are undefined until completion of reset.

PIN CONFIGURATION
μPD80C48G/μPD80C35G
(52 PIN FLAT PACKAGE)

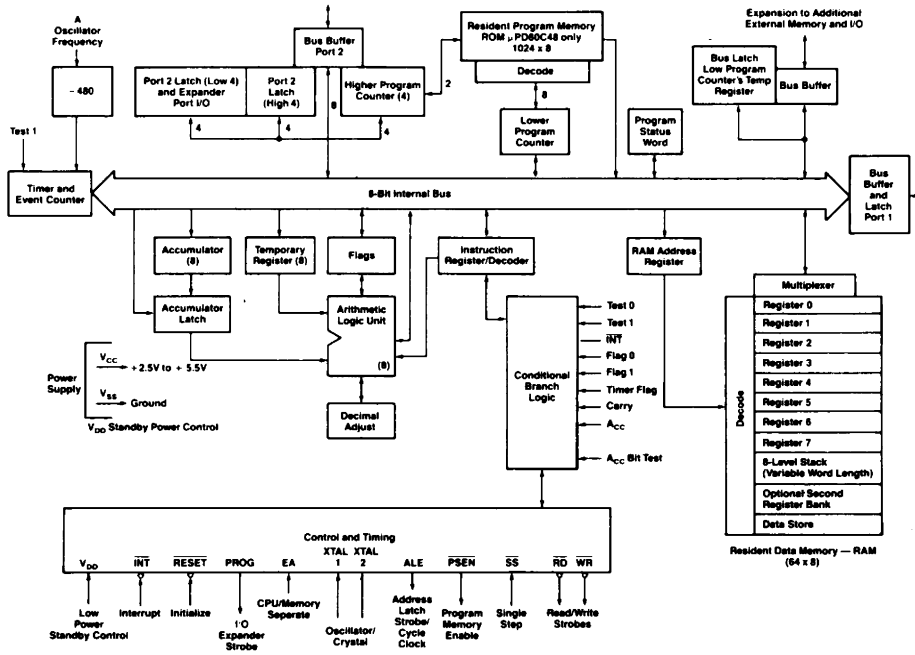


* INTERNAL CONNECTION, IT IS PROHIBITED TO USE PIN 33

PIN CONFIGURATION
μPD48G
(44 PIN FLAT PACKAGE)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature, T_{opt}	−40°C to +85°C
Storage Temperature (Plastic Package), T_{stg}	−65°C to +150°C
Voltage on Any Pin, $V_{I/O}$	V_{SS} −0.3V to V_{CC} +0.3V
Supply Voltage, V_{CC}	V_{SS} −0.3 to +10V
Power Dissipation, P_D with I_{CC} = max. 8 mA and V_{CC} = 5V nominal P_D = 40 mW	40 mW

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS **Standard Voltage Range**

T_a = −40°C to +85°C; V_{CC} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.8	V
Input High Voltage	V_{IH}	All except XTAL1, XTAL2, $\overline{RESET}$	V_{CC} −2		V_{CC}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2	V_{CC} −1		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output High Voltage	V_{OH}	Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −100 μA	2.4			V
	V_{OH1}④	Port 1, Port 2; I_{OH} = −5 μA (Type 0)	2.4			V
		Port 1, Port 2; I_{OH} = −50 μA (Type 1)				
	V_{OH2}	All outputs; I_{OH} = −0.2 μA	V_{CC} −0.5			V
Input Current	I_{ILP}④	Port 1, Port 2; $V_{IN} \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		Port 1, Port 2; $V_{IN} \leqslant V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_{IN} \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, V_{DD}; $V_{SS} \leqslant V_{IN} \leqslant V_{CC}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_{IN} \leqslant V_{CC}$			±3	μA
Output Leakage Current	I_{LO}	Bus, T0, High-Impedance State; $V_{SS} \leqslant V_O \leqslant V_{CC}$			±1	μA
Standby Current	I_{CC1}	Halt mode; t_{CY} = 2.5 μs		0.4	0.8	mA
	I_{CC2}	Stop mode②		1	20	μA
Supply Current	I_{CC}	t_{CY} = 2.5 μs		4	8	mA
Data Retention Voltage	V_{CCDR}	Stop mode (V_{DD}, $\overline{RESET} \leqslant$0.4V)	2.0			V

DC CHARACTERISTICS **Extended Voltage Range**

$T_a = -40°C$ to $+85°C$; $V_{CC} = +2.5V$ to $+6V$; $V_{SS} = 0V$

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.18 V_{CC}	V
Input High Voltage (All Except XTAL 1, XTAL 2)	V_{IN}		0.7 V_{CC}		V_{CC}	V
Input High Voltage (XTAL 1, XTAL 2)	V_{IH1}		0,8 V_{CC}		V_{CC}	V
Output Low Voltage	V_{OL}	$I_{OL} = 1.0$ mA			0.45	V
Output High Voltage (Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0	V_{OH}	$I_{OH} = -100\ \mu A$	0.75 V_{CC}			V
Output High Voltage (All other Outputs)	V_{OH1}	Port 1, Port 2; $I_{OH} = -1\mu A$ (Type 0)	0.7 V_{CC}			V
		Port 1, Port 2; $I_{OH} = -10\ \mu A$ (Type 1)				
Output High Voltage (All Outputs)	V_{OH2}	$I_{OH} = -0.2\ \mu A$	V_{CC} −0.5			V
Input Leakage Current (Port 1, Port 2)	I_{ILP}	$V_{IN} \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		$V_{IN} \leqslant V_{IL}$ (Type 1)			−500	μA
Input Leakage Current ($\overline{SS}$, $\overline{RESET}$)	I_{ILC}	$V_{IN} \leqslant V_{IL}$			−40	μA
Input Leakage Current (T1, $\overline{INT}$)	I_{IL1}	$V_{SS} < V_{IN} < V_{CC}$			±1	μA
Input Leakage Current (EA)	I_{IL2}	$V_{SS} < V_{IN} < V_{CC}$			±3	μA
Output Leakage Current (Bus, T0 – High Impedance State)	I_{OL}	$V_{SS} < V_O < V_{CC}$			±1	μA
Supply Current	I_{CC}	$V_{CC} = 3V$, $t_{CY} = 10\ \mu s$		0.8	1.6	mA
		$V_{CC} = 6V$, $t_{CY} = 2.5\ \mu s$		6	12	mA
Halt Mode Standby Current	I_{CC1}	$V_{CC} = 3V$, $t_{CY} = 10\ \mu s$		100	200	μA
		$V_{CC} = 6V$, $t_{CY} = 2.5\ \mu s$		0.6	1.2	mA
Stop Mode Standby Current	I_{CC2}	$V_{CC} = 3V$		1	20	μA
		$V_{CC} = 6V$		1	50	μA

Notes: (1.) Type 0 and type 1 options apply only to the μPD80C48; the μPD80C35 is type 0 only. Input Pin Voltage is V_{IN}, V_{IL}, or V_{IN}, V_{IH}.

(2.) Type 0 is mask version with $I_{OH} = -5\ \mu A$ for each Port Line.
Type 1 is mask version with $I_{OH} = -50\ \mu A$ for each Port Line.

AC CHARACTERISTICS Read, Write and Instruction Fetch: External Data and Program Memory

T_a = −40°C to +85°C; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = +5V ± 10%			V_{CC} = +2.5V to 6V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ALE Pulse Width	t_{LL}	①	400			2160			ns
Address Setup before ALE	t_{AL}		120			1620			ns
Address Hold from ALE	t_{LA}		80			330			ns
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}		700			3700			ns
Data Setup before $\overline{WR}$	t_{DW}		500			3500			ns
Data Hold after $\overline{WR}$	t_{WD}	②	120			370			ns
Cycle Time	t_{CY}	①	2.5		150	10		150	μs
Data Hold	t_{DR}		0		200	0		950	ns
$\overline{PSEN}$, $\overline{RD}$ to Data in	t_{RD}				500			2750	ns
Address Setup before $\overline{WR}$	t_{AW}		230			3230			ns
Address Setup before Data in	t_{AD}				950			5450	ns
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}		0			500			ns
Control Pulse to ALE	t_{CA}		10			10			ns

AC CHARACTERISTICS Port 2 Timing

T_a = −40°C to +85°C; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = +5V ± 10%			V_{CC} = +2.5V to 6V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Port Control Setup before Falling Edge of PROG	t_{CP}	③	110			860			ns
Port Control Hold after Falling Edge of PROG	t_{PC1}	③, ⑤	0		80	0		200 ④	ns
	t_{PC2}	③, ⑥	460			2400			ns
PROG to Time P2 Input must be Valid	t_{PR}	③			810			5310	ns
Output Data Setup Time	t_{DP}		250			3250			ns
Output Data Hold Time	t_{PD}		65			820			ns
Input Data Hold Time	t_{PF}		0		150	0		900	ns
PROG Pulse Width	t_{PP}		1200			6450			ns
Port 2 I/O Data Setup	t_{PL}		350			2100			ns
Port 2 I/O Data Hold	t_{LP}		150			1400			ns

Notes: ① For Control Outputs: C_L = 80 pF; for Bus Outputs: C_L = 150 pF.
② C_L = 20 pF
③ For Control Outputs: C_L = 80 pF
④ Refer to the operating characteristic curves for Supply Voltage and Port Control Hold.
⑤ t_{CY} = 2.5 μs with V_{CC} = 5V ± 10%
⑥ t_{CY} = 10 μs with V_{CC} = +2.5V to +5.5V

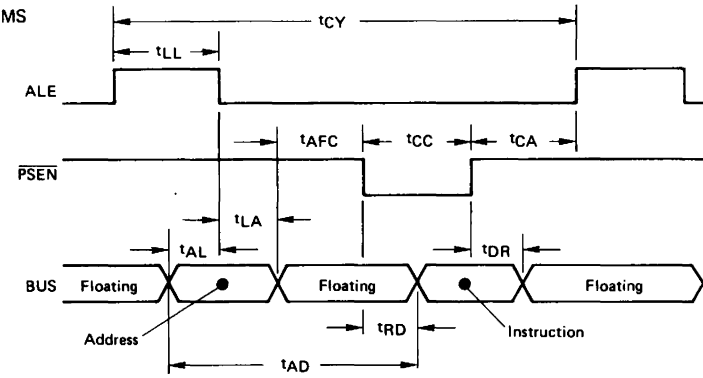
BUS Timing Requirements

SYMBOL	TIMING FORMULA	MIN	MAX	UNIT
t_{LL}	(7/30) T – 170	•		ns
t_{AL}	(1/5) T – 380	•		ns
t_{LA}	(1/30) T	•		ns
t_{CC}	(2/5) T – 300	•		ns
t_{DW}	(2/5) T – 500	•		ns
t_{WD}	(1/30) T + 40	•		ns
t_{DR}	(1/10) T – 50		•	ns
t_{RD}	(3/10) T – 250		•	ns
t_{AW}	(2/5) T – 770	•		ns
t_{AD}	(3/5) T – 550		•	ns
t_{AFC}	(1/15) T – 165	•		ns
t_{CP}	(1/10) T – 140	•		ns
t_{PR}	(3/5) T – 690		•	ns
t_{PF}	(1/10) T – 100		•	ns
t_{DP}	(2/5) T – 750	•		ns
t_{PD}	(1/10) T – 180	•		ns
t_{PP}	(7/10) T – 550	•		ns
t_{PL}	(7/30) T – 230	•		ns
t_{LP}	(1/6) T – 265	•		ns

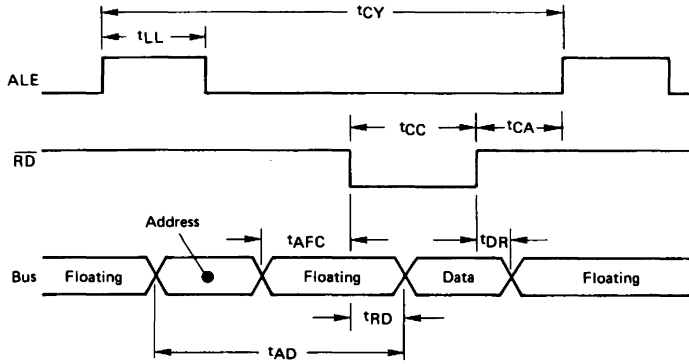
Notes: T = t_{CY}
Unlisted parameters are not affected by cycle time
$t_{CY} = (1/f_{XTAL}) \times 15$

TIMING WAFEFORMS

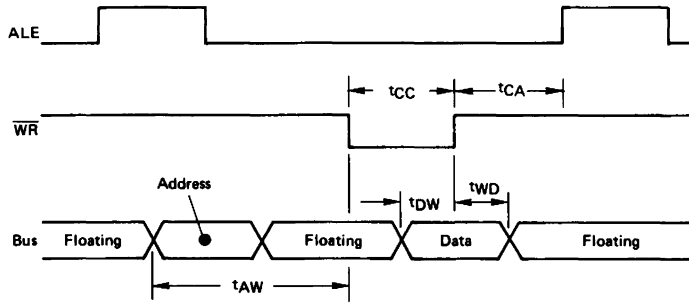
Instruction Fetch from External Memory



Read from External Data Memory

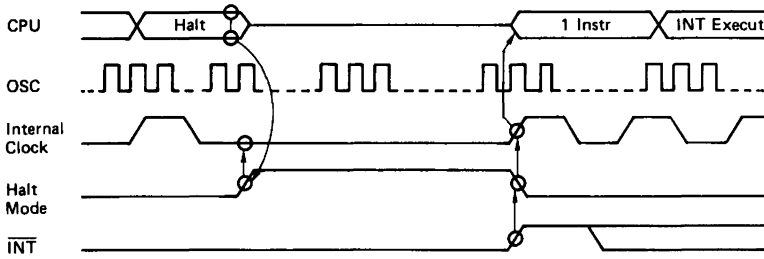


Write to External Memory

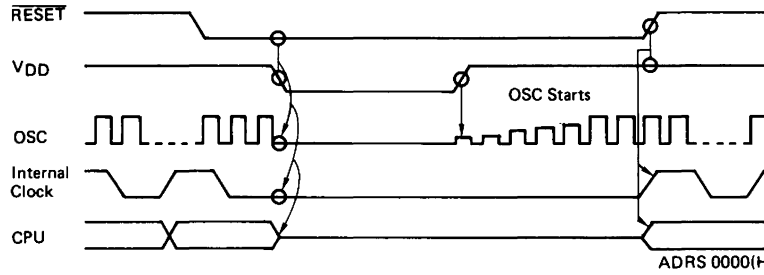


Low Power Standby Operation

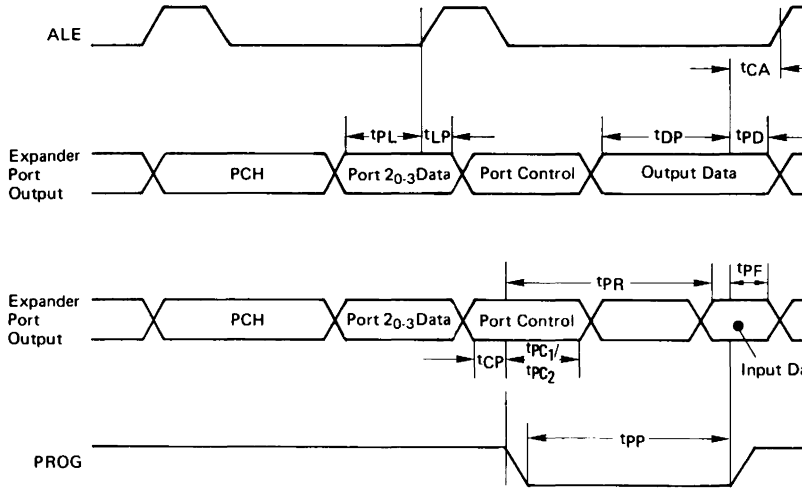
1) Halt Mode (When EI)



2) Stop Mode

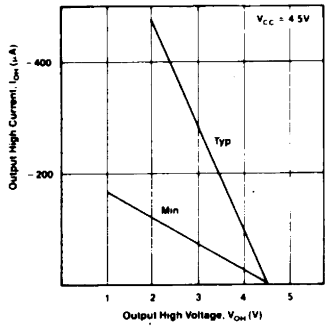


Port 2 Timing

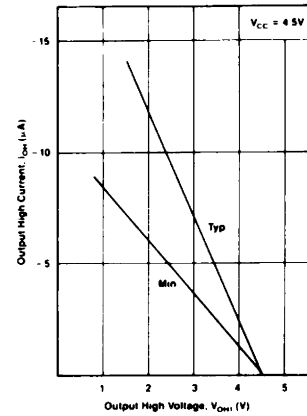


OPERATING CHARACTERISTIC CURVES

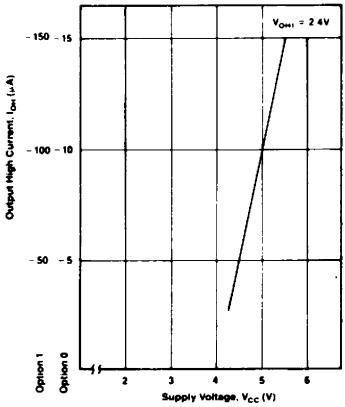
Output High Current vs. Output High Voltage



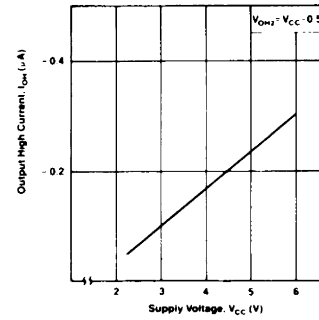
Output High Current vs. Output High Voltage



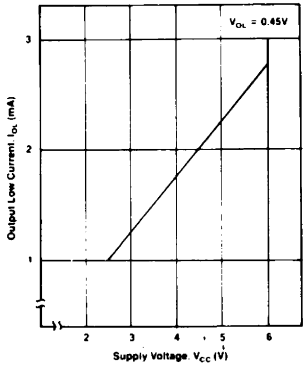
Output High Current vs. Supply Voltage



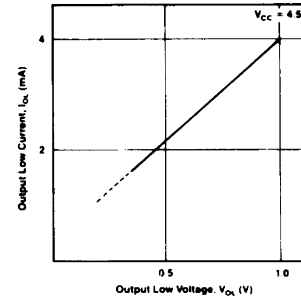
Output High Current vs. Supply Voltage



Output Low Current vs. Supply Voltage

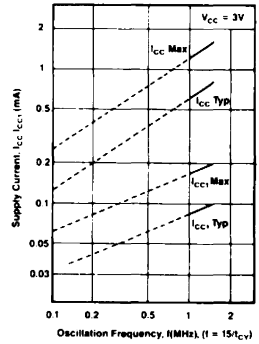


Output Low Current vs. Output Low Voltage

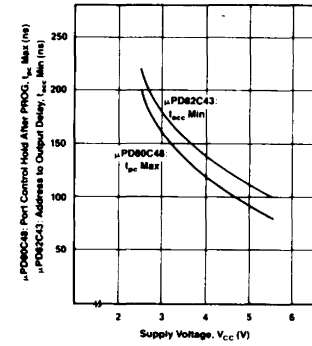


OPERATING CHARACTERISTIC CURVES (Cont.)

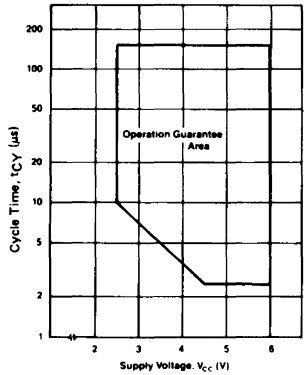
Supply Current vs. Oscillation Frequency



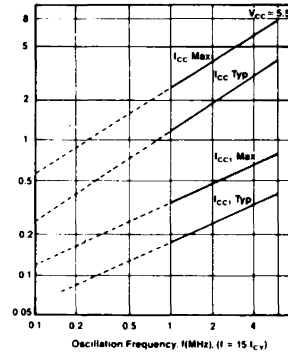
Port Control Hold After PROG, t_{PC} Max (μPD80C48), and Address to Output Delay, t_{ACC} Min (μPD82C43), vs. Supply Voltage



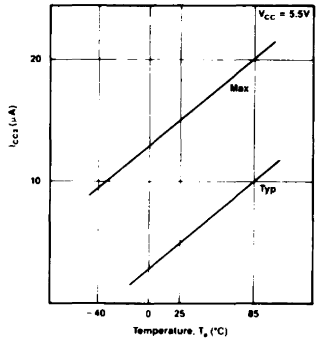
Cycle Time vs. Supply Voltage



Supply Current vs. Oscillation Frequency ①



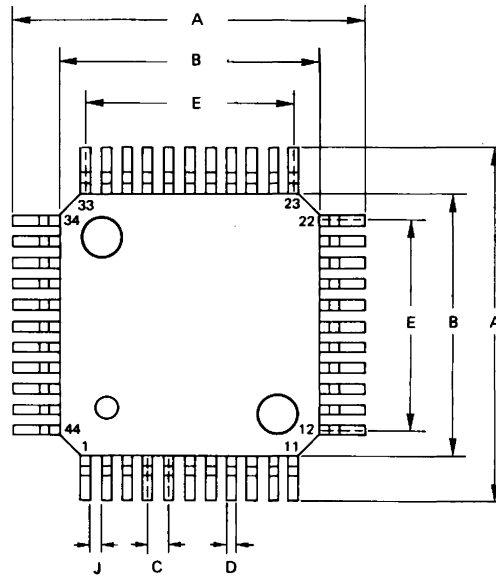
Current Consumption as a Function of Temperature – Stop Mode

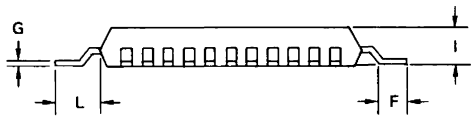


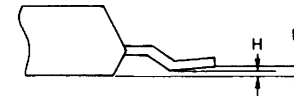
Note: ① External oscillation is assumed for frequency less than 1 MHz. Internal oscillation requires more power.

PACKAGE DIMENSIONS
μPD48G
44 PIN PLASTIC
FLAT PACK

ITEM	MILLIMETERS	INCHES
A	13.6 ± 0.4	0.54 ± 0.016
B	10	.394
C	0.8 ± 0.15	.03 ± 0.006
D	.35 $^{+0.3}_{-0.1}$	.014 $^{+.01}_{-.004}$
E	8.0 ± 0.3	.315 ± .012
F	1.0 ± 0.2	.39 ± .008
G	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
H	0.0 ± 0.1	0.0 ± .004
I	1.4 $^{+0.2}_{-0.1}$	0.06 $^{+0.008}_{-0.004}$
J	0.2 min	0.008 min
K	0.0 ± 0.2	0.0 ± 0.008
L	1.8 ± 0.2	0.071 ± 0.008



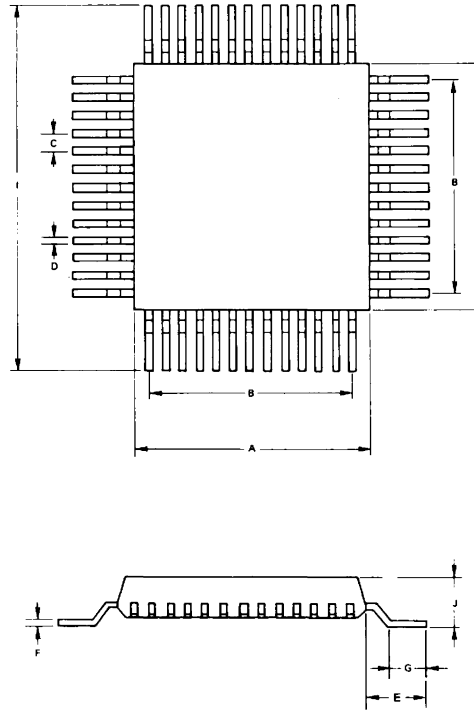




Lead bend (enlarged view)

PACKAGE DIMENSIONS
μPD80C48G/C35G
52 PIN FLAT PACK

ITEM	MILLIMETERS	INCHES
A	14.0 $^{+0.3}_{-0.2}$	.55
B	12.0 ± 0.3	.472 ± .012
C	1.0 ± 0.15	.039 ± .006
D	0.4 $^{+0.2}_{-0.1}$	.016 $^{+.008}_{-.004}$
E	3.5 ± 0.2	0.14 ± 0.008
F	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
G	2.2 ± 0.2	.087 ± .008
I	21.0 ± 0.4	.811 ± 0.16
J	2.8 max	.110 max

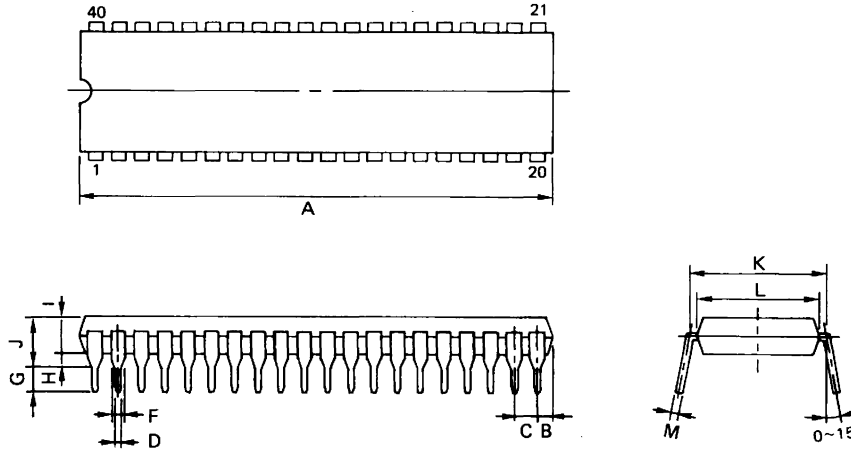


PACKAGE DIMENSIONS
μPD80C35C/C48C
40 PIN PLASTIC DIP

ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T. P.)	0.100 (T. P.)
D	0.50 ± 0.10	0.020 $^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6 ± 0.3	0.142 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T. P.)	0.600 (T. P.)
L	13.2	0.520
M	0.25 $^{+0.10}_{-0.05}$	0.010 $^{+0.004}_{-0.003}$
N	0.25	0.01

Notes: 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T. P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.



CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

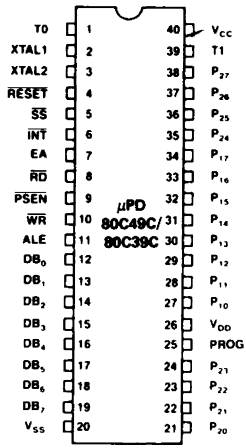
The NEC μPD80C49 is a true stand-alone 8-bit microcomputer fabricated using CMOS technology. All of the functional blocks necessary for an integrated microcomputer are incorporated, including a 2K-byte ROM, a 128-byte RAM, 27 I/O lines, an 8-bit timer/event counter, and a clock generator. This integrated capability permits use in stand-alone applications. For designs requiring extra capability, the μPD80C49 can be expanded using peripherals and memory compatible with industry-standard 8080A/8085A processors. A version of the μPD80C48 without ROM is offered by the μPD80C39.

Providing compatibility with industry-standard 8049, 8749, and 8039 processors, the μPD80C49 features significant savings in power consumption. In addition to the power savings gained through CMOS technology, the μPD80C49 is distinct in offering two standby modes (Halt mode and Stop mode) to further minimize power drain.

FEATURES

- 8-bit CPU with ROM, RAM, and I/O on a single chip
- Hardware/software-compatible with industry-standard 8049, 8749, and 8039 processors
- 2K x 8 ROM
- 128 x 8 RAM
- 27 I/O lines
- 1.875 μs cycle time (8 MHz crystal)
- All instructions executable in 1 or 2 cycles
- 97 instructions: 70 percent are single-byte instructions
- Internal timer/event counter
- 2 interrupts (an external interrupt and a timer interrupt)
- Easily expandable memory and I/O
- Bus compatible with 8080A/8085A peripherals
- Power-efficient CMOS technology requiring a single +2.5V to +6V power supply
- Available in 40-pin DIP, 44-pin flat pack (80C49 only), and 52-pin flat pack
- Halt mode
  - 1 mA typical supply current
  - Maintenance of internal logic values and control states
  - Mode initialization via HALT instruction
  - Mode release via external interrupt or reset
- Stop mode
  - 1 μA typical supply current
  - Disabling of internal clock generation and internal logic
  - Maintenance of RAM contents
  - Mode initialization via hardware (V_{DD})
  - Mode release via reset

PIN CONFIGURATION μPD80C49C/μPD80C39C (40 PIN PLASTIC DIP)



PIN IDENTIFICATION

A.
μPD80C49C/μPD80C39C
(40 PIN PLASTIC DIP)

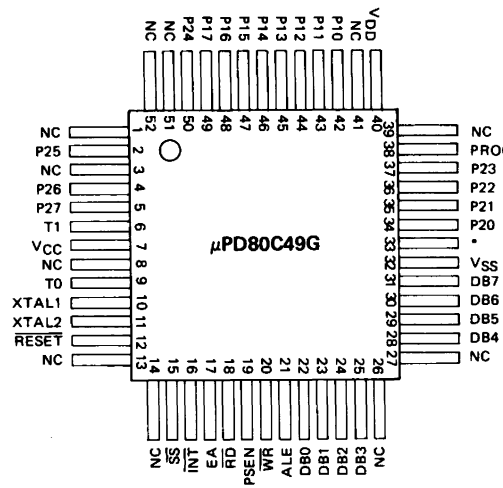
B.
μPD80C49G/μPD80C39G
(52 PIN PLASTIC
FLAT PACK)

C.
μPD49G
(44 PIN PLASTIC
FLAT PACK)

PIN					
C.	B.	A.	SYMBOL	NAME	FUNCTION
18	9	1	T0	Test 0	Testable input using conditional jump instructions JT0 and JNT0. Also enables clock output via the ENT0 CLK instruction.
19	10	2	XTAL1	Crystal 1	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. May also be used as an input for external clock signals. (Non-TTL-compatible V_{IH}.)
20	11	3	XTAL2	Crystal 2	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. (Non-TTL-compatible V_{IH}.)
22	12	4	$\overline{RESET}$	Reset	Active-low input line that initializes the processor. Also used to release both the Halt and Stop modes. ①
23	15	5	$\overline{SS}$	Single Step	Active-low input line, that, in conjunction with ALE, causes the processor to single-step through a program one instruction at a time.
24	16	6	$\overline{INT}$	Interrupt	Active-low input line that causes an interrupt if an enable instruction has been executed. A reset disables the interrupt. May be used as a testable input with a conditional jump instruction. Can also be used to release the Halt mode.
25	17	7	EA	External Access	Input line that inhibits internal program memory fetches and initiates access of external program memory. Essential for system testing and may also be used for program debugging.
26	18	8	$\overline{RD}$	Read	Active-low output strobe line that is used to read data from external data memory.
27	19	9	$\overline{PSEN}$	Program Store Enable	Active-low output line that is used to fetch instructions from external program memory.
28	20	10	$\overline{WR}$	Write	Active-low output strobe line that is used to write data into external data memory.
29	21	11	ALE	Address Latch Enable	Output line for address latch enable. At the falling edge of ALE, the address of either external data memory or external program memory is available on the bus.
30-37	22-25, 28-31	12-19	DB_0-DB_7	Bus	These I/O lines constitute an 8-bit bidirectional data/address bus. Synchronous read and write operations can be performed on this bus using $\overline{RD}$ and $\overline{WR}$ signals. Data driven out on the bus by an OUTL BUS instruction is statically latched. The address of external memory is available on the bus at the falling edge of ALE when reading from external program memory or writing to and reading from external data memory. During external program memory fetches, the least-significant 8 bits of the external program memory address are driven out on the bus and the addressed instruction is fetched using $\overline{PSEN}$. When no external memory is used, the bus can serve as a true bidirectional 8-bit port. Information is strobed in or out by the $\overline{RD}$ and $\overline{WR}$ signals.
38	32	20	V_{SS}	Ground	Ground potential.
39-42, 11, 13-15	34-37, 50, 2, 4, 5	21-24, 35-38	P_{20}-P_{27}	Port 2	These lines constitute Port 2, an 8-bit quasi-bidirectional port. During external program memory fetches P_{20}-P_{23} output the most-significant 4 bits of the external program memory address. Lines P_{20}-P_{23} can also be used as a 4-bit I/O expander bus to interface with the optional μPD82C43 I/O expander.
43	38	25	PROG	Program Pulse	This line is used as an output strobe when interfacing with the optional μPD82C43 I/O expander.
1	40	26	V_{DD}	Oscillator Control Voltage Line	This input line is used to control oscillator stopping and restarting in Stop mode. Stop mode is enabled by forcing V_{DD} Low during a reset.
2- 7, 9-10	42-49	27-34	P_{10}-P_{17}	Port 1	These lines constitute Port 1, an 8-bit, generalpurpose quasi-bidirectional port.
16	6	39	T1	Test 1	Testable input using conditional jump instructions JT1 and JNT1. Can also be used as the timer/counter input line via the STRT CNT instruction.
17	7	40	V_{CC}	Primary Power Supply	Power supply. V_{CC} must be between +2.5V to +6V for normal operation. In Stop mode, V_{CC} must be at least +2V to ensure data retention.

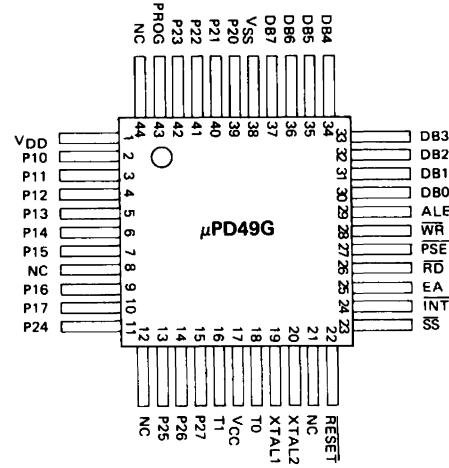
Note: ①The pulse width of $\overline{RESET}$ must be a minimum of 5 machine cycles in length following oscillator stabilization to reinitialize the processor and stabilize CPU operation. At power-up, the states of the output lines are undefined until completion of reset.

PIN CONFIGURATION
μ80C49G/μPD80C39G
(52 PIN FLAT PACKAGE)

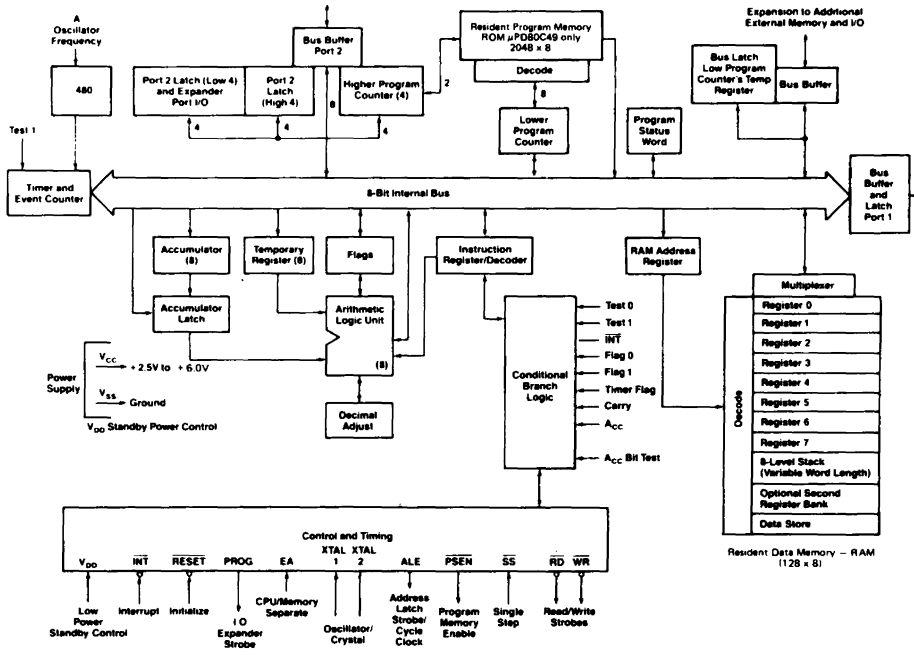


• INTERNAL CONNECTION, IT IS PROHIBITED TO USE PIN 33

PIN CONFIGURATION
μPD49G
(44 PIN FLAT PACKAGE)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature, T_{opt}	−40°C to +85°C
Storage Temperature (Plastic Package), T_{stg}	−65°C to +150°C
Voltage on Any Pin, $V_{I/O}$	V_{SS} −0.3V to V_{CC} +0.3V
Supply Voltage, V_{CC}	V_{SS} −0.3 to +10V
Power Dissipation, P_D with I_{CC} = max. 8 mA and V_{CC} = 5V nominal P_D = 40 mW	40 mW

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS **Standard Voltage Range**

T_a = −40°C to +85°C; V_{CC} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.8	V
Input High Voltage	V_{IH}	All except XTAL1, XTAL2, $\overline{RESET}$	V_{CC} −2		V_{CC}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2	V_{CC} −1		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output High Voltage	V_{OH}	Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −100 μA	2.4			V
	V_{OH1}①	Port 1, Port 2; I_{OH} = −5 μA (Type 0)	2.4			V
		Port 1, Port 2; I_{OH} = −50 μA (Type 1)				
	V_{OH2}	All outputs; I_{OH} = −0.2 μA	V_{CC} −0.5			V
Input Current	I_{ILP}①	Port 1, Port 2; $V_{IN} \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		Port 1, Port 2; $V_{IN} \leqslant V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_{IN} \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, V_{DD}; $V_{SS} \leqslant V_{IN} \leqslant V_{CC}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_{IN} \leqslant V_{CC}$			±3	μA
Output Leakage Current	I_{LO}	Bus, T0, High-Impedance State; $V_{SS} \leqslant V_O \leqslant V_{CC}$			±1	μA
Standby current	I_{CC1}	Halt mode; t_{CY} = 2.5 μs		0.4	0.8	mA
	I_{CC1}	Halt mode; t_{CY} = 1.875 μs		0.5	1.0	mA
	I_{CC2}	Stop mode ②		1	20	μA
Supply Current	I_{CC}	t_{CY} = 2.5 μs		5	10	mA
	I_{CC}	t_{CY} = 1.875 μs		6	12	mA
Data Retention Voltage	V_{CCDR}	Stop mode (V_{DD}, $\overline{RESET} \leqslant$ 0.4V)	2.0			V

DC CHARACTERISTICS Extended Voltage Range

T_a = −40°C to +85°C; V_{CC} = +2.5V to 6.0V; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.18 V_{CC}	V
Input High Voltage (All Except XTAL 1, XTAL 2)	V_{IN}		0.7 V_{CC}		V_{CC}	V
Input High Voltage (XTAL 1, XTAL 2)	V_{IH1}		0.8 V_{CC}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 1.0 mA			0.45	V
Output High Voltage (Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, $\overline{PROG}$, T0	V_{OH}	I_{OH} = −100 μA	0.75 V_{CC}			V
Output High Voltage (All other Outputs)	V_{OH1}	Port 1, Port 2; I_{OH} = −1 μA (Type 0)	0.7 V_{CC}			V
		Port 1, Port 2: I_{OH} = −10 μA (Type 1)				
Input Leakage Current (Port 1, Port 2)	I_{ILP}	$V_{IN} \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		$V_{IN} \leqslant V_{IL}$ (Type 1)			−500	μA
Input Leakage Current ($\overline{SS}$, $\overline{RESET}$)	I_{ILC}	$V_{IN} \leqslant V_{IL}$			−40	μA
Input Leakage Current (T1, $\overline{INT}$)	I_{IL1}	$V_{SS} < V_{IN} < V_{CC}$			±1	μA
Input Leakage Current (EA)	I_{IL2}	$V_{SS} < V_{IN} < V_{CC}$			±5	μA
Output Leakage Current (Bus, T0 – High Impedance State)	I_{OL}	$V_{SS} < V_O < V_{CC}$			±1	μA
Supply Current	I_{CC}	V_{CC} = 3V, t_{CY} = 10 μs		0.8	1.6	mA
		V_{CC} = 6V, t_{CY} = 2.5 μs		8	15	mA
		V_{CC} = 6V, t_{CY} = 1.875 μs		10	20	mA
Halt Mode Standby Current	I_{CC1}	V_{CC} = 3V, t_{CY} = 10μs		100	200	μA
		V_{CC} = 6V, t_{CY} = 2.5 μs		0.6	1.2	mA
		V_{CC} = 6V, t_{CY} = 1.875 μs		0.7	1.4	mA
Stop Mode Standby Current	I_{CC2}	V_{CC} = 3V		1	20	μA
		V_{CC} = 6V		1	50	μA

Notes: (1.) Type 0 and type 1 options apply only to the μPD80C49; the μPD80C39 is type 0 only. Input Pin Voltage is V_{IN}, V_{IL}, or V_{IN}, V_{IH}.

(2.) Type 0 is mask version with I_{OH} = −5 μA for each Port Line. Type 1 is mask version with I_{OH} = −50 μA for each Port Line.

AC CHARACTERISTICS Read, Write and Instruction Fetch: External Data and Program Memory

T_a = −40°C to +85°C; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = +5V ± 10%			V_{CC} = +2.5V to 6V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ALE Pulse Width	t_{LL}	①	270			2160			ns
Address Setup before ALE	t_{AL}	①	90			1620			ns
Address Hold from ALE	t_{LA}	①	60			330			ns
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}	①	450			3700			ns
Data Setup before $\overline{WR}$	t_{DW}	①	250			3500			ns
Data Hold after $\overline{WR}$	t_{WD}	②	100			370			ns
Cycle Time	t_{CY}	①	1.875		150	10		150	μs
Data Hold	t_{DR}	①	0		130	0		950	ns
$\overline{PSEN}$, $\overline{RD}$ to Data in	t_{RD}	①			310			2750	ns
Address Setup before $\overline{WR}$	t_{AW}	①	150			3230			ns
Address Setup before Data in	t_{AD}	①			575			5450	ns
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	①	0			500			ns
Control Pulse to ALE	t_{CA}	①	10			10			ns

AC CHARACTERISTICS Port 2 Timing

T_a = −40°C to +85°C; V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = +5V ± 10%			V_{CC} = +2.5V to 6V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Port Control Setup before Falling Edge of PROG	t_{CP}	③	110			860			ns
Port Control Hold after Falling Edge of PROG	t_{PC1}	③, ⑤	0		80	0		200 ⑤	ns
	t_{PC2}	③, ⑥	300			2400			ns
PROG to Time P2 Input must be Valid	t_{PR}	③			650			5310	ns
Output Data Setup Time	t_{DP}	③	200			3250			ns
Output Data Hold Time	t_{PD}	③	20			820			ns
Input Data Hold Time	t_{PF}	③	0		85	0		900	ns
PROG Pulse Width	t_{PP}	③	760			6450			ns
Port 2 I/O Data Setup	t_{PL}	③	205			2100			ns
Port 2 I/O Data Hold	t_{LP}	③	45			1400			ns

Notes: ① For Control Outputs: C_L = 80 pF; for Bus Outputs: C_L = 150 pF.
② C_L = 20 pF
③ For Control Outputs: C_L = 80 pF
④ Refer to the operating characteristic curves for Supply Voltage and Port Control Hold.
⑤ t_{CY} = 2.5 μs with V_{CC} = 5V ± 10%
⑥ t_{CY} = 10 μs with V_{CC} = +2.5V to +5.5V

BUS Timing Requirements

SYMBOL	TIMING FORMULA	MIN	MAX	UNIT
t_{LL}	(7/30) T – 167	•		ns
t_{AL}	(1/5) T – 285	•		ns
t_{LA}	(1/30) T	•		ns
t_{CC}	(2/5) T – 300	•		ns
t_{DW}	(2/5) T – 500	•		ns
t_{WD}	(1/30) T + 40	•		ns
t_{DR}	(1/10) T – 50		•	ns
t_{RD}	(3/10) T – 250		•	ns
t_{AW}	(2/5) T – 600	•		ns
t_{AD}	(3/5) T – 550		•	ns
t_{AFC}	(1/15) T – 125	•		ns
t_{CP}	(1/10) T – 87	•		ns
t_{PR}	(3/5) T – 475		•	ns
t_{PF}	(1/10) T – 100		•	ns
t_{DP}	(2/5) T – 550	•		ns
t_{PD}	(1/10) T – 167	•		ns
t_{PP}	(7/10) T – 550	•		ns
t_{PL}	(7/30) T – 230	•		ns
t_{LP}	(1/6) T – 265	•		ns

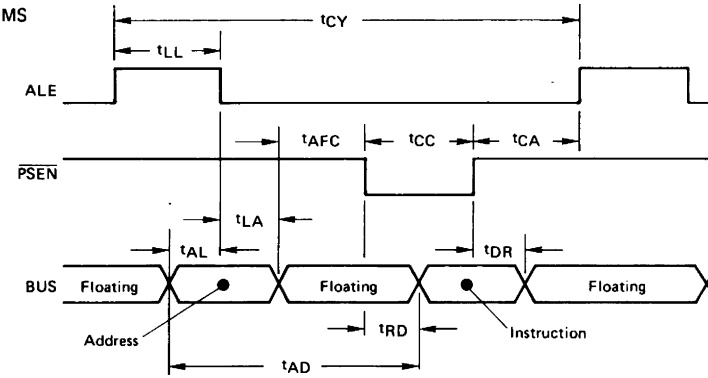
Notes: $T = t_{CY}$

Unlisted parameters are not affected by cycle time

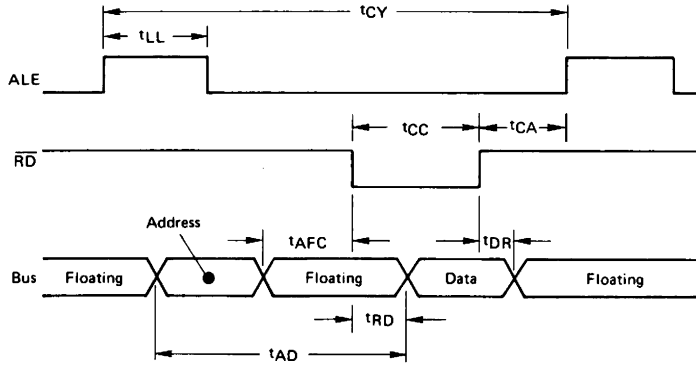
$t_{CY} = (1/f_{XTAL}) \times 15$

TIMING WAFEFORMS

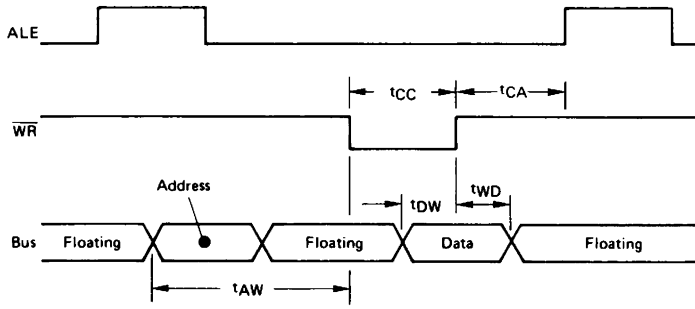
Instruction Fetch from External Memory



Read from External Data Memory

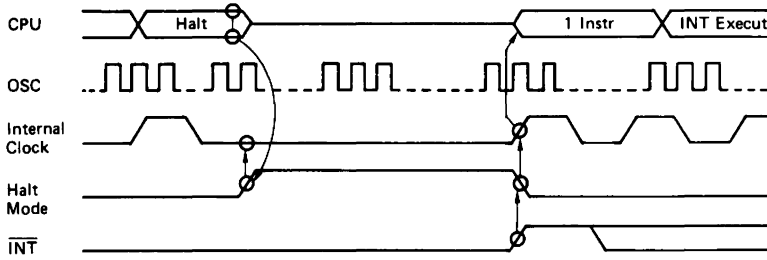


Write to External Memory

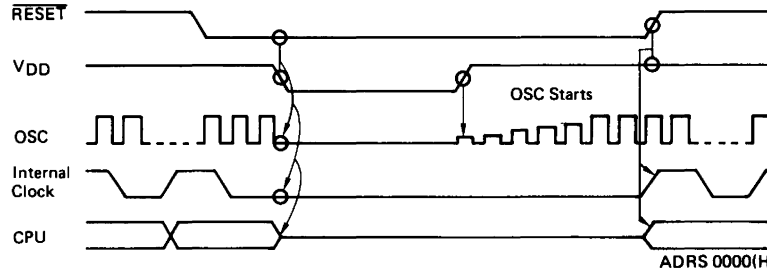


Low Power Standby Operation

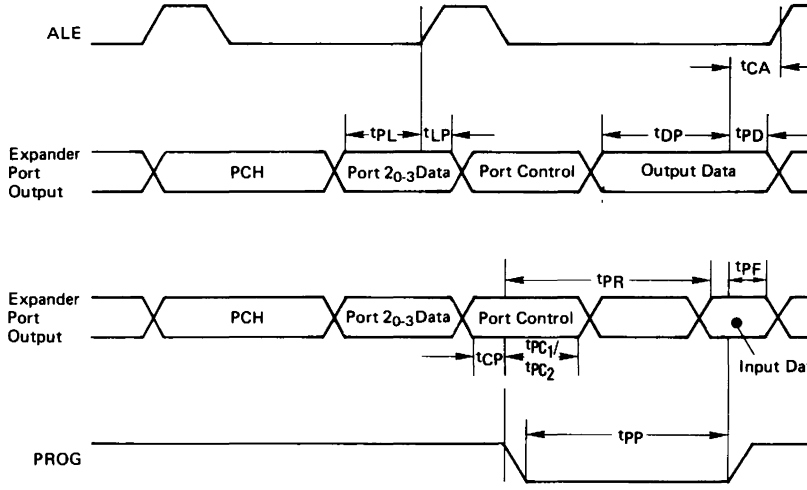
1) Halt Mode (When EI)



2) Stop Mode

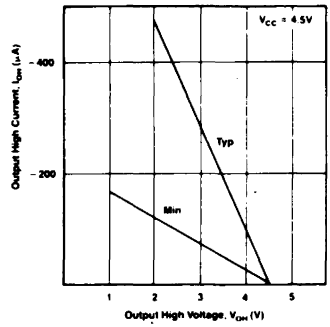


Port 2 Timing

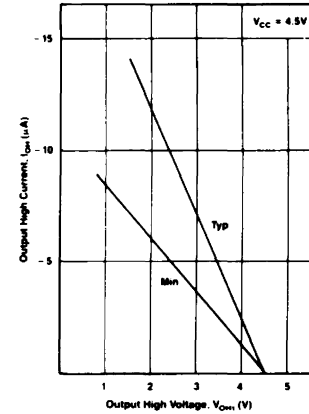


OPERATING CHARACTERISTIC CURVES

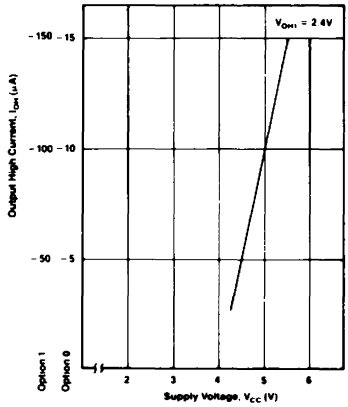
Output High Current vs. Output High Voltage



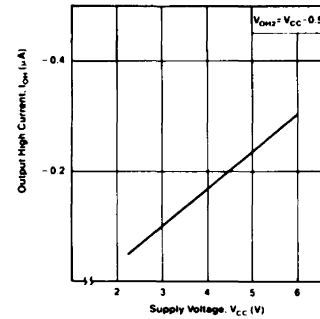
Output High Current vs. Output High Voltage



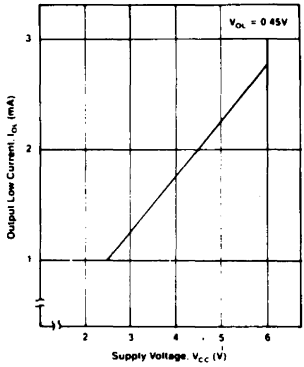
Output High Current vs. Supply Voltage



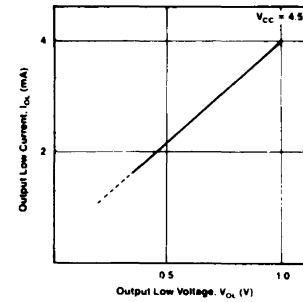
Output High Current vs. Supply Voltage



Output Low Current vs. Supply Voltage

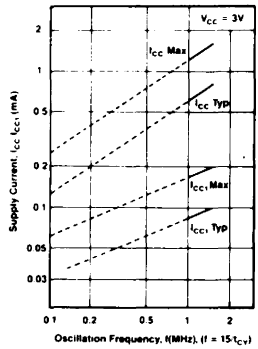


Output Low Current vs. Output Low Voltage

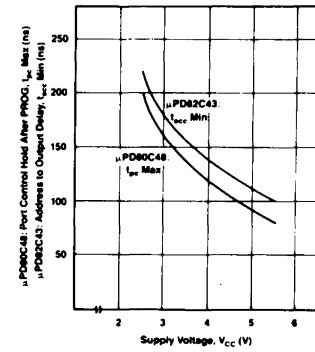


OPERATING CHARACTERISTIC CURVES (Cont.)

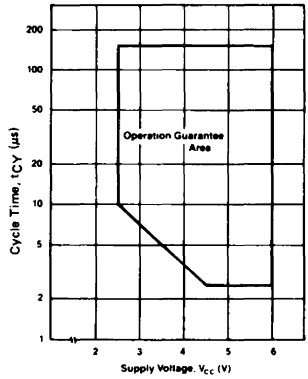
Supply Current vs. Oscillation Frequency



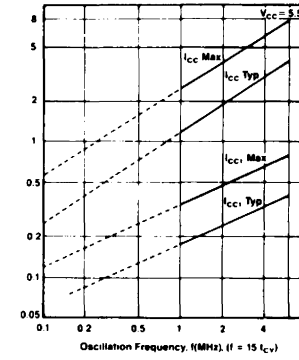
Port Control Hold After PROG, t_{PC} Max (μPD80C48), and Address to Output Delay, t_{ACC} Min (μPD82C43), vs. Supply Voltage



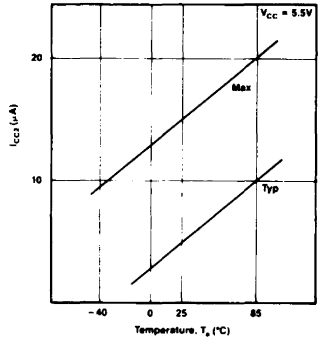
Cycle Time vs. Supply Voltage



Supply Current vs. Oscillation Frequency ①



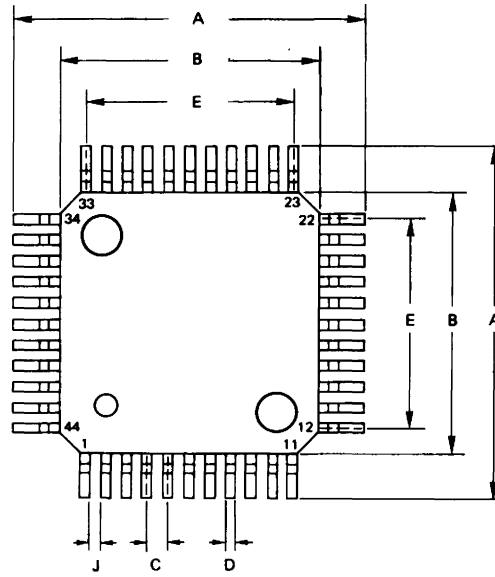
Current Consumption as a Function of Temperature — Stop Mode

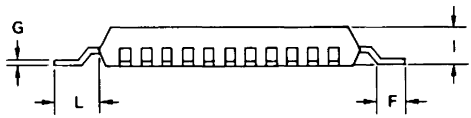


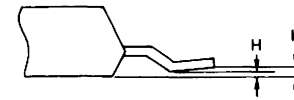
Note: ① External oscillation is assumed for frequency less than 1 MHz. Internal oscillation requires more power.

PACKAGE DIMENSIONS
μPD49G
44 PIN PLASTIC
FLAT PACK

ITEM	MILLIMETERS	INCHES
A	13.6 ± 0.4	0.54 ± 0.016
B	10	.394
C	0.8 ± 0.15	.03 ± 0.006
D	.35 $^{+0.3}_{-0.1}$	.014 $^{+.01}_{-.004}$
E	8.0 ± 0.3	.315 ± .012
F	1.0 ± 0.2	.39 ± .008
G	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
H	0.0 ± 0.1	0.0 ± .004
I	1.4 $^{+0.2}_{-0.1}$	0.06 $^{+0.008}_{-0.004}$
J	0.2 min	0.008 min
K	0.0 ± 0.2	0.0 ± 0.008
L	1.8 ± 0.2	0.071 ± 0.008



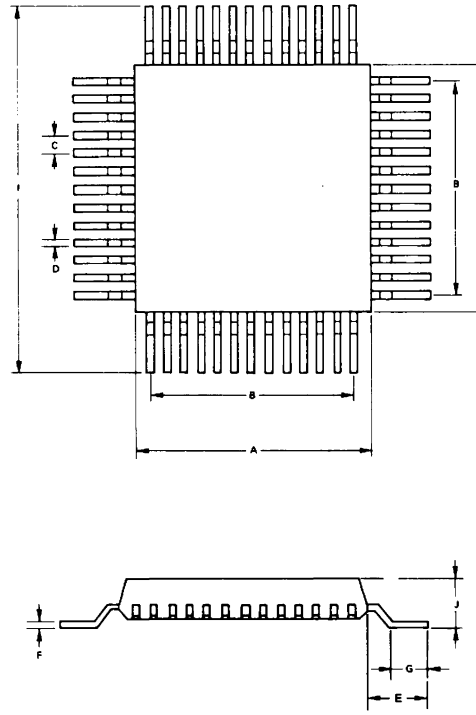




Lead bend (enlarged view)

PACKAGE DIMENSIONS
μPD80C49G/C39G
52 PIN PLASTIC
FLAT PACK

ITEM	MILLIMETERS	INCHES
A	14.0 $^{+0.3}_{-0.2}$	.55
B	12.0 ± 0.3	.472 ± .012
C	1.0 ± 0.15	.039 ± .006
D	0.4 $^{+0.2}_{-0.1}$	.016 $^{+.008}_{-.004}$
E	3.5 ± 0.2	0.14 ± 0.008
F	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
G	2.2 ± 0.2	.087 ± .008
I	21.0 ± 0.4	.811 ± 0.16
J	2.8 max	.110 max

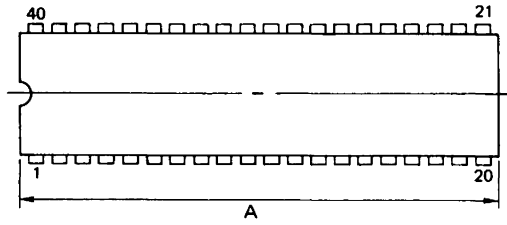


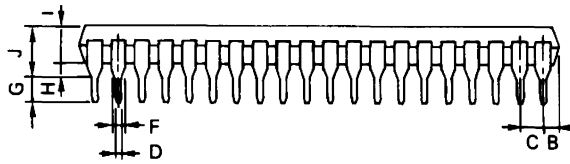
PACKAGE DIMENSIONS
μPD80C49C/C39C
40 PIN PLASTIC

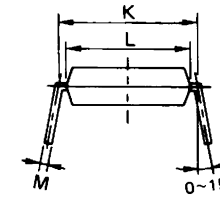
ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T. P.)	0.100 (T. P.)
D	0.50 ± 0.10	0.020 $^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6 ± 0.3	0.142 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T. P.)	0.600 (T. P.)
L	13.2	0.520
M	0.25 $^{+0.10}_{-0.05}$	0.010 $^{+0.004}_{-0.003}$
N	0.25	0.01

Notes: 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T. P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.







CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

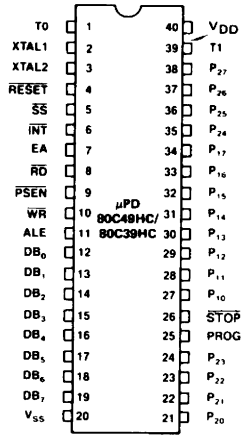
The NEC μPD80C49H is a true stand-alone 8-bit microcomputer fabricated using CMOS technology. All of the functional blocks necessary for an integrated microcomputer are incorporated, including a 2K-byte ROM, a 128-byte RAM, 27 I/O lines, an 8-bit timer/event counter, and a clock generator. This integrated capability permits use in stand-alone applications. For designs requiring extra capability, the μPD80C49H can be expanded using peripherals and memory compatible with industry-standard 8080A/8085A processors. A version of the μPD80C49H without ROM is offered by the μPD80C39H.

Providing compatibility with industry-standard 8049, 8749, and 8039 processors, the μPD80C49H features significant savings in power consumption. In addition to the power savings gained through CMOS technology, the μPD80C49H is distinct in offering two standby modes (HALT mode and STOP mode) to further minimize power drain.

FEATURES

- 8-bit CPU with ROM, RAM, and I/O on a single chip
- Hardware/software-compatible with industry-standard 8049, 8749, and 8039 processors
- 2K x 8 ROM
- 128 x 8 RAM
- 27 I/O lines
- 1.25 μs cycle time (12 MHz crystal)
- All instructions executable in 1 or 2 cycles
- 97 instructions: 70 percent are single-byte instructions
- Internal timer/event counter
- 2 interrupts (an external interrupt and a timer interrupt)
- Easily expandable memory and I/O
- Bus compatible with 8080A/8085A peripherals
- Power-efficient CMOS technology requiring a single +2.5V to 6V power supply
- Available in 40-pin DIP, 44-pin flat pack (80C49H only)
- Halt mode
  - 1 mA typical supply current
  - Maintenance of internal logic values and control states
  - Mode initialization via HALT instruction
  - Mode release via external interrupt or reset
- Stop mode
  - 1 μA typical supply current
  - Disabling of internal clock generation and internal logic
  - Maintenance of RAM contents
  - Mode initialization via hardware ($\overline{STOP}$)
  - Mode release via reset

PIN CONFIGURATION μPD80C49HC/ μPD80C39HC (40 PIN PLASTIC DIP)



PIN IDENTIFICATION

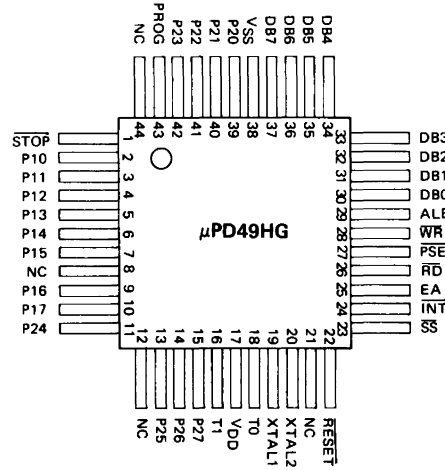
A.
μPD80C49HC/
μPD80C39HC
(40 PIN PLASTIC DIP)

B.
μPD49HG
(44 PIN PLASTIC
FLAT PACK)

PIN				FUNCTION
B.	A.	SYMBOL	NAME	
18	1	T0	Test 0	Testable input using conditional jump instructions JT0 and JNT0. Also enables clock output via the ENT0 CLK instruction.
19	2	XTAL1	Crystal 1	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. May also be used as an input for external clock signals. (Non-TTL-compatible V_{IH}.)
20	3	XTAL2	Crystal 2	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. (Non-TTL-compatible V_{IH}.)
22	4	$\overline{RESET}$	Reset	Active-low input line that initializes the processor. Also used to release both the Halt and Stop modes. ①
23	5	$\overline{SS}$	Single Step	Active-low input line, that, in conjunction with ALE, causes the processor to single-step through a program one instruction at a time.
24	6	$\overline{INT}$	Interrupt	Active-low input line that causes an interrupt if an enable instruction has been executed. A reset disables the interrupt. May be used as a testable input with a conditional jump instruction. Can also be used to release the Halt mode.
25	7	EA	External	Input line that inhibits internal program memory fetches and initiates access of external program memory. Essential for system testing and may also be used for program debugging.
26	8	$\overline{RD}$	Read	Active-low output strobe line that is used to read data from external data memory.
27	9	$\overline{PSEN}$	Program Store Enable	Active-low output line that is used to fetch instructions from external program memory.
28	10	$\overline{WR}$	Write	Active-low output strobe line that is used to write data into external data memory.
29	11	ALE	Address Latch Enable	Output line for address latch enable. At the falling edge of ALE, the address of either external data memory or external program memory is available on the bus.
30-37	12-19	DB_0-DB_7	Bus	These I/O lines constitute an 8-bit bidirectional data/address bus. Synchronous read and write operations can be performed on this bus using $\overline{RD}$ and $\overline{WR}$ signals. Data driven out on the bus by an OUTL BUS instruction is statically latched. The address of external memory is available on the bus at the falling edge of ALE when reading from external program memory or writing to and reading from external data memory. During external program memory fetches, the least-significant 8 bits of the external program memory address are driven out on the bus and the addressed instruction is fetched using $\overline{PSEN}$. When no external memory is used, the bus can serve as a true bidirectional 8-bit port. Information is strobed in or out by the $\overline{RD}$ and $\overline{WR}$ signals.
38	20	V_{SS}	Ground	Ground potential.
39-42, 11, 13-15	21-24, 35-38	P_{20}-P_{27}	Port 2	These lines constitute Port 2, an 8-bit quasi-bidirectional port. During external program memory fetches P_{20}-P_{23} output the most-significant 4 bits of the external program memory address. Lines P_{20}-P_{23} can also be used as a 4-bit I/O expander bus to interface with the optional μPD82C43 I/O expander.
43	25	PROG	Program Pulse	This line is used as an output strobe when interfacing with the optional μPD82C43 I/O expander.
1	26	$\overline{STOP}$	Stop	Used to control the hardware STOP mode.
2- 7, 9-10	27-34	P_{10}-P_{17}	Port 1	These lines constitute Port 1, an 8-bit, generalpurpose quasi-bidirectional port.
16	39	T1	Test 1	Testable input using conditional jump instructions JT1 and JNT1. Can also be used as the timer/counter input line via the STRT CNT instruction.
17	40	V_{DD}	Primary Power Supply	Power supply. V_{CC} must be between +2.5V to +6V for normal operation. In Stop mode, V_{CC} must be at least +2V to ensure data retention.

Note: ① The pulse width of RESET must be a minimum of 5 machine cycles in length following oscillator stabilization to reinitialize the processor and stabilize CPU operation. At power-up, the states of the output lines are undefined until completion of reset.

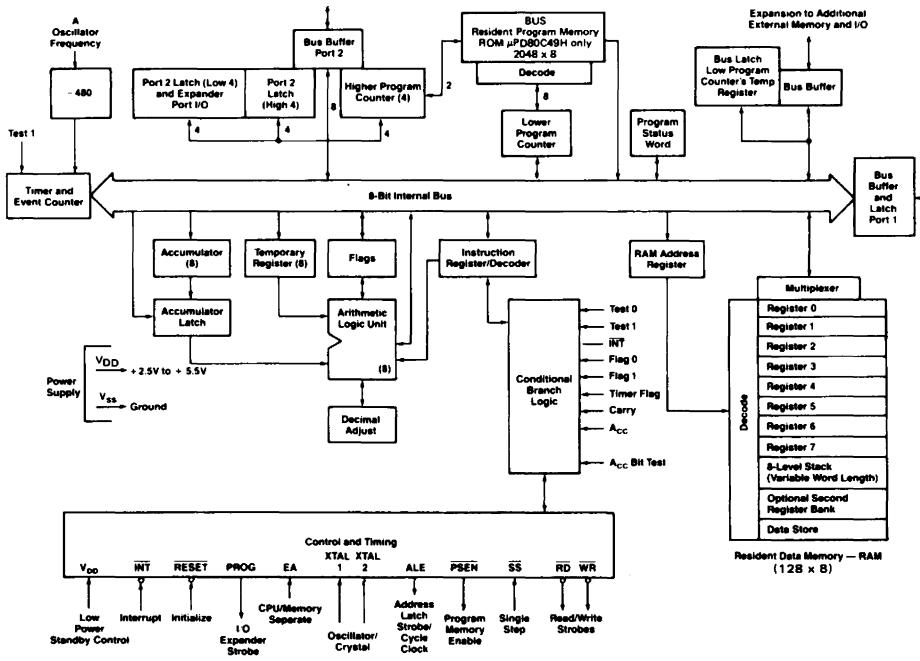
PIN CONFIGURATION
μPD49HG
(44 PIN FLAT PACKAGE)



DIFFERENCES BETWEEN μPD49H and μPD49

Item \ Type	μPD49H	μPD49
Instruction set	98 instructions (including an additional STOP instruction)	97 instructions
Instruction cycle	1.25 μs/12 MHz	1.875 μs/8 MHz
Standby facility	Three modes; HALT, hardware STOP and software STOP	Two modes; HALT and STOP
	Stops inactive in the same timing in all of the HALT, hardware STOP, and software STOP modes, regardless of control signals executing internal ROM or external ROM (with ALE being high level).	Stops in different timings between the HALT and STOP modes.
Port option (pull-up resistance)	• Type 0 (I_{OH} = −5 μA: V_{DD} = 5V ± 10%) • Type 1 (I_{OH} = −50 μA: V_{DD} = 5V ± 10%) • Type 2 (without pull-up resistance)	− Type 0 (I_{OH} = −5 μA: V_{DD} = 5V ± 10%) − Type 1 (I_{OH} = −50 μA: V_{DD} = 5V ± 10%)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature, T_{opt}	−40°C to +85°C
Storage Temperature (Plastic Package), T_{stg}	−65°C to +150°C
Voltage on Any Pin, $V_{I/O}$	V_{SS} −0.3V to V_{DD} +0.3V
Supply Voltage, V_{DD}	V_{SS} −0.3 to +7V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS T_a = −40 to +85°C, V_{DD} = +5V ± 10 %, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.8	V
Input High Voltage	V_{IH}	(All except XTAL1, XTAL2, $\overline{RESET}$ $\overline{SS}$)	V_{DD} −2		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$	V_{DD} −1		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output High Voltage	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −400 μA	2.4			V
	V_{OH1} ③	PORT1, PORT2; I_{OH} = −5 μA (Type 0)	2.4			V
	V_{OH1} ③	PORT1, PORT2; I_{OH} = 50 μA (Type 1)	2.4			V
	V_{OH2}	All outputs; I_{OH} = −0.2 μA	V_{DD} −0.5			V
Input Current	I_{ILP} ③	PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±3	μA
Output Leakage Current	I_{LO}	BUS, T0, High impedance state (2) $V_{SS} \leqslant V_O \leqslant V_{DD}$			±1	μA
Standby Current	I_{DD1}	HALT mode; t_{CY} = 1.25 μs		1.5	3.0	mA
	I_{DD2}	STOP mode (1)		1	20	μA
Supply Current	I_{DD}	t_{CY} = 1.25 μs		6	15	mA
Data Holding Voltage	V_{DDDR}	Hardware STOP mode ($\overline{STOP}$, $\overline{RESET}$ ⩽0.4V) or reset ($\overline{RESET}$ ⩽0.4V)	2.0			V

Notes:

(1) Input pin voltage $V_I \leqslant V_{IL}$ or $V_I \geqslant V_{IH}$.

(2) Includes PORT1 and PORT2 pins optionally specified with type 2.

(3) Type 0 and Type 1 options apply only to the μPD80C49H; the μPD80C39H is type 0 only.

DC CHARACTERISTICS $T_a = -40$ to $+85°C$, $V_{DD} = +2.5V$ to $+6.0V$, $V_{SS} = 0V$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.18 V_{DD}	V
Input High Voltage	V_{IH}	(All except XTAL1, XTAL2, $\overline{RESET}$, $\overline{SS}$)	0.7 V_{DD}		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, SS	0.8 V_{DD}		V_{DD}	V
Input Low Voltage	V_{OL}	$I_{OL} = 1.0$ mA			0.45	V
Output High Voltage	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; $I_{OH} = -100\ \mu A$	0.75 V_{DD}			V
	V_{OH1} ③	PORT1, PORT2; $I_{OH} = -1\ \mu A$ (Type 0)	0.7 V_{DD}			V
		PORT1, PORT2; $I_{OH} = -10\ \mu A$ (Type 1)	0.7 V_{DD}			V
Input Current	I_{ILP} ③	PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±5	μA
Output Leakage Current	I_{LO}	BUS, T0, High impedance state (2) $V_{SS} \leqslant V_O \leqslant V_{DD}$			±1	μA
Standby Current	I_{DD1}	HALT mode $V_{DD} = 3V$; $t_{CY} = 5\ \mu s$		0.3	0.6	mA
		HALT mode $V_{DD} = 6V$; $t_{CY} = 1.25\ \mu s$		2.0	4.0	mA
	I_{DD2}	STOP mode (1) $V_{DD} = 3V$		1	20	μA
		STOP mode (1) $V_{DD} = 6V$		1	50	μA
Supply Current	I_{DD}	$V_{DD} = 3V$; $t_{CY} = 5\ \mu s$		2.0	4.0	mA
		$V_{DD} = 6V$; $t_{CY} = 1.25\ \mu s$		10	20	mA

Notes:

(1) Input pin voltage $V_I \leqslant V_{IL}$ or $V_I \geqslant V_{IH}$.

(2) Includes PORT1 and PORT2 pins optionally specified with type 2.

(3) Type 0 and Type 1 options apply only to the μPD80C49H; the μPD80C39H is type 0 only.

AC CHARACTERISTICS

T_a = −40 to +85°C, V_{SS} = 0V

PARAMETER	SYMBOL	CONDITION	V_{DD} = +5V ±10%			V_{DD} = +2.5 to +6.0V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Cycle Time	t_{CY}		1.25		150	5		150	μs
ALE Pulse Width	t_{LL}	③	125			995			ns
Address Setup to ALE	t_{AL}		140			890			ns
Address Hold from ALE	t_{LA}		45			295			ns
Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}		425			2300			ns
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}		300			1400			ns
Data Setup before $\overline{WR}$	t_{DW}		340			1965			ns
Data Hold after $\overline{WR}$	t_{WD}	④	45			295			ns
Data Hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}	③	0		95	0		470	ns
$\overline{RD}$ to Data in	t_{RD1}				300			1800	ns
$\overline{PSEN}$ to Data in	t_{RD2}				175			1300	ns
Address Setup to $\overline{WR}$	t_{AW}		350			1850			ns
Address Setup to $\overline{RD}$ Data in	t_{AD1}				700			3585	ns
Address Setup to $\overline{PSEN}$ data in	t_{AD2}				500			2750	ns
Address Float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}		105			600			ns
Address Float to $\overline{PSEN}$	t_{AFC2}		5			125			ns
ALE to $\overline{RD}$, $\overline{WR}$ delay	t_{LAFC1}		175			925			ns
ALE to $\overline{PSEN}$ delay	t_{LAFC2}		50			425			ns
$\overline{RD}$, $\overline{WR}$, PROG to ALE delay	t_{CA1}		35			285			ns
$\overline{PSEN}$ to ALE delay	t_{CA2}		280			1285			ns
Port Control Setup to PROG	t_{CP}	⑤	85			460			ns
Port Control Hold from PROG	t_{PC1}	⑤, ⑥	0		80	0		200 ⑧	ns
	t_{PC2}	⑤, ⑦	135			1135			ns
Input Data Setup to PROG	t_{PR}	⑤			585			2715	ns
Input Data Hold from PROG	t_{PF}		0		125	0		500	ns
Output Data Setup to PROG	t_{DP}		350			1850			ns
Output Data Hold from PROG	t_{PD}		75			450			ns
PROG Pulse Width	t_{PP}		625			3250			ns
Port 2 I/O Data Setup to ALE	t_{PL}		135			1135			ns
Port 2 I/O Data Hold from ALE	t_{LP}		5			125			ns
ALE to Port Output	t_{PV}				475			1600	ns
T0 Output Cycle Time	t_{OPRR}		250			1000			ns

Notes:

③ Control Outputs C_L = 80 pF; BUS Output: C_L = 150 pF

④ C_L = 20 pF

⑤ Control Outputs: C_L = 80 pF

⑥ During Execution of MOVD A, Pp

⑦ During Execution of MOVD Pp, A, ANLD Pp, A, ORLD Pp, A

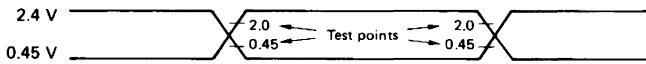
⑧ See supply voltage and port Control hold time characteristic curves

t_{CY}-DEPENDENT BUS TIMING DEFINITIONS

PARAMETER	CALCULATION FORMULA	MIN	MAX	UNIT
t_{LL}	(7/30) T – 170	●		ns
t_{AL}	(1/ 5) T – 110	●		ns
t_{LA}	(1/15) T – 40	●		ns
t_{CC1}	(1/ 2) T – 200	●		ns
t_{CC2}	(2/ 5) T – 200	●		ns
t_{DW}	(13/30) T – 200	●		ns
t_{WD}	(1/15) T – 40	●		ns
t_{DR}	(1/10) T – 30		●	ns
t_{RD1}	(2/ 5) T – 200		●	ns
t_{RD2}	(3/10) T – 200		●	ns
t_{AW}	(2/ 5) T – 150	●		ns
t_{AD1}	(23/30) T – 250		●	ns
t_{AD2}	(3/ 5) T – 250		●	ns
t_{AFC1}	(2/15) T – 65	●		ns
t_{AFC2}	(1/30) T – 40	●		ns
t_{LAFC1}	(1/ 5) T – 75	●		ns
t_{LAFC2}	(1/10) T – 75	●		ns
t_{CA1}	(1/15) T – 50	●		ns
t_{CA2}	(4/15) T – 50	●		ns
t_{CP}	(1/10) T – 40	●		ns
t_{PC2}	(4/15) T – 200	●		ns
t_{PR}	(17/30) T – 120		●	ns
t_{PF}	(1/10) T		●	ns
t_{DP}	(2/ 5) T – 150	●		ns
t_{PD}	(1/10) T – 50	●		ns
t_{PP}	(7/10) T – 250	●		ns
t_{PL}	(4/15) T – 200	●		ns
t_{LP}	(1/30) T – 40	●		ns
t_{PV}	(3/10) T + 100		●	ns
t_{OPRR}	(1/ 5) T	●		ns
t_{CY}	$(1/f_{XTAL}) \times 15$			μs

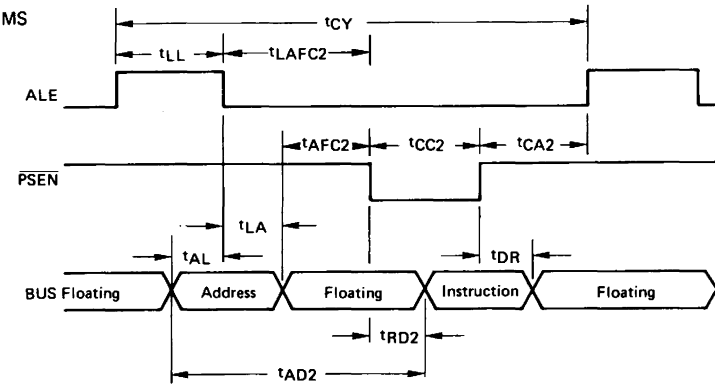
Remarks: T = t_{CY}

AC TEST I/O WAVEFORM

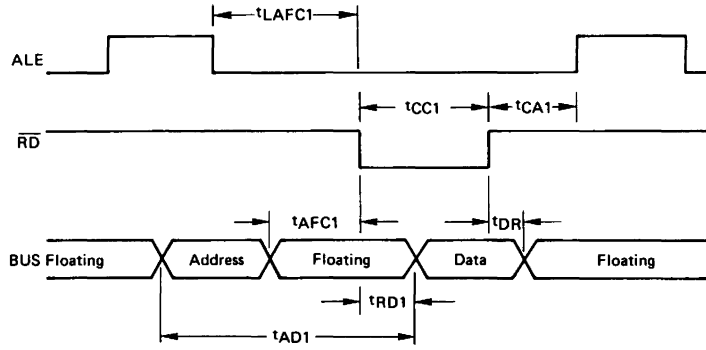


TIMING WAFEFORMS

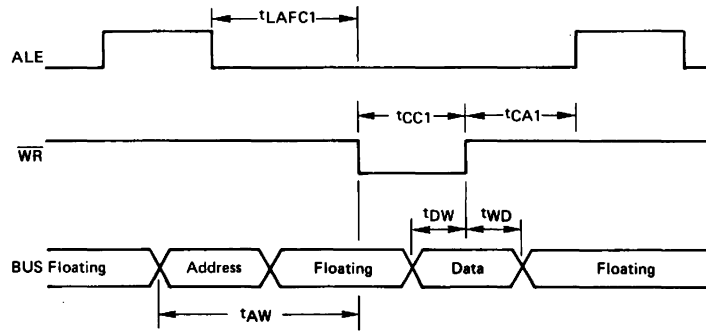
Instruction fetch from external program memory



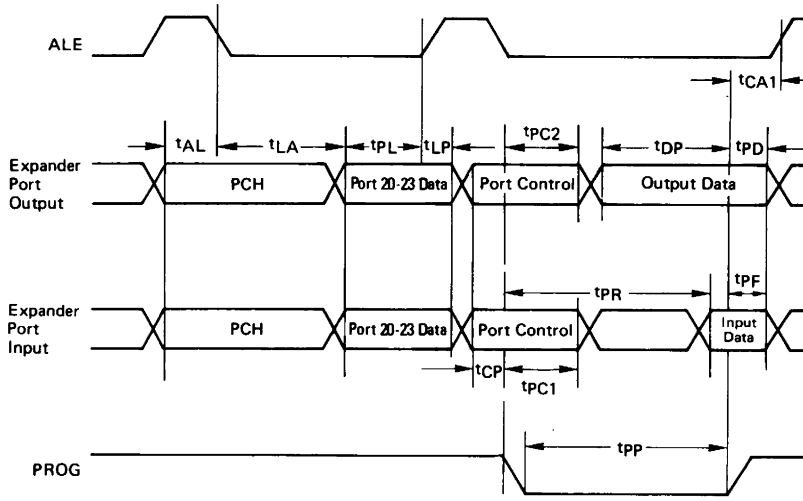
Read from external data memory



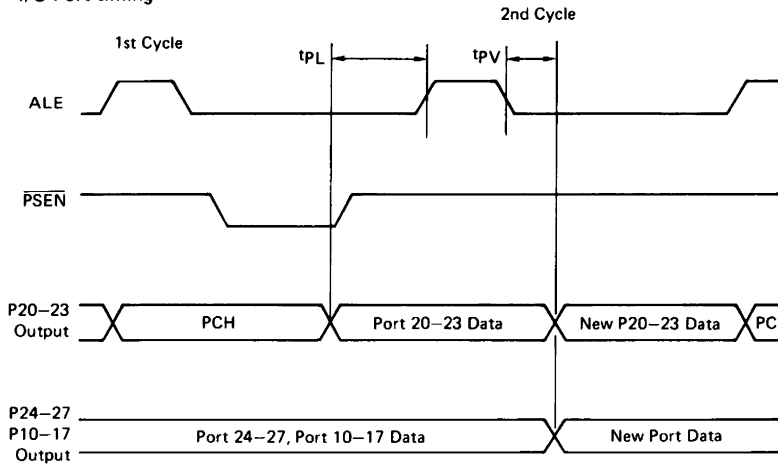
Write to external data memory



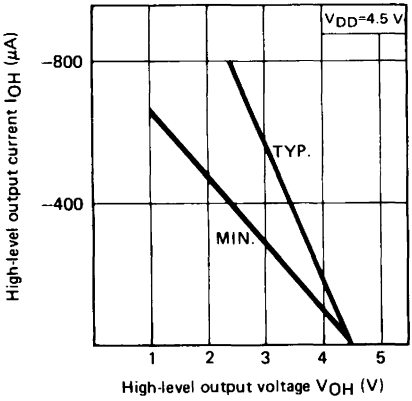
Port 2 extended timing

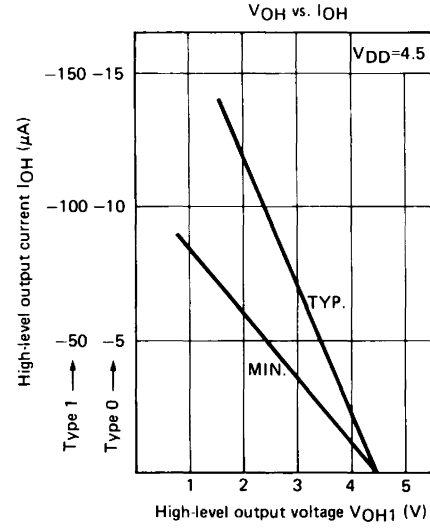


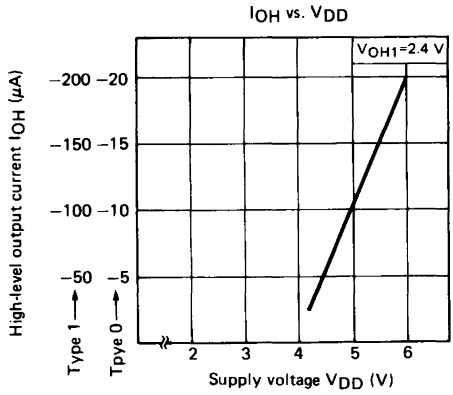
I/O Port timing

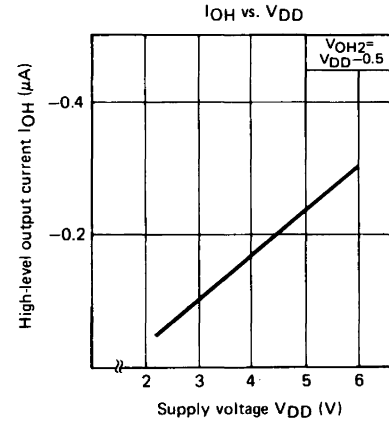


CHARACTERISTIC CURVES (T_a = 25° C)



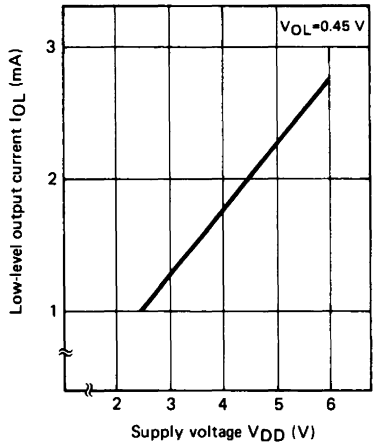




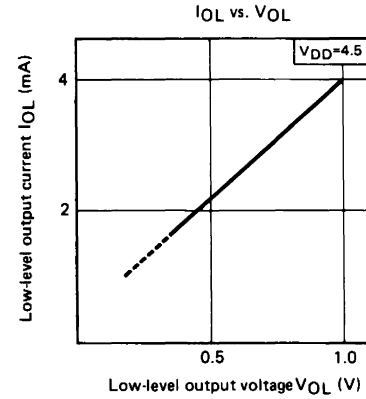


CHARACTERISTIC CURVES (Continued)

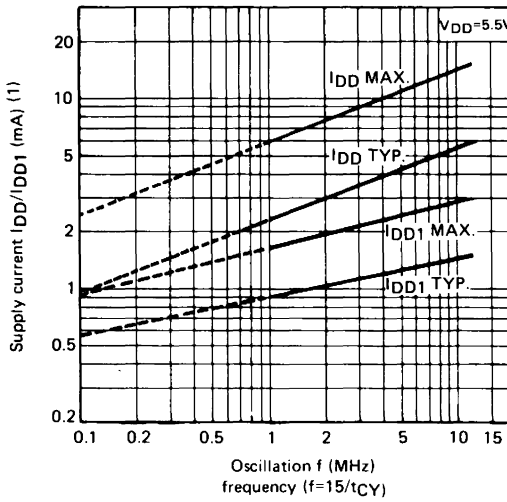
I_{OL} vs. V_{DD}



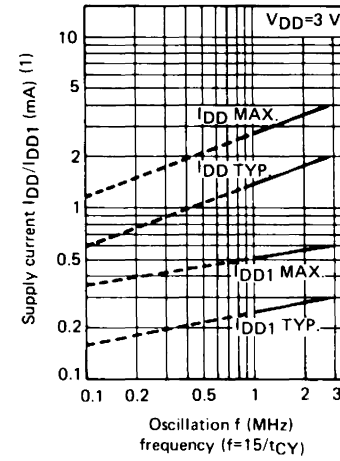
I_{OL} vs. V_{OL}



I_{DD}/I_{DD1} vs. f



I_{DD}/I_{DD1} vs. f

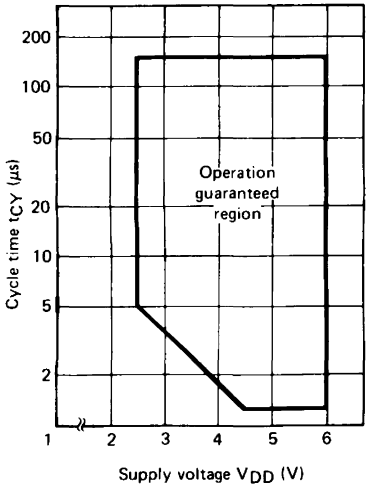


Note:
1) Less than 1 MHz for external oscillation. Power consumption is larger with internal oscillation than with external oscillation.

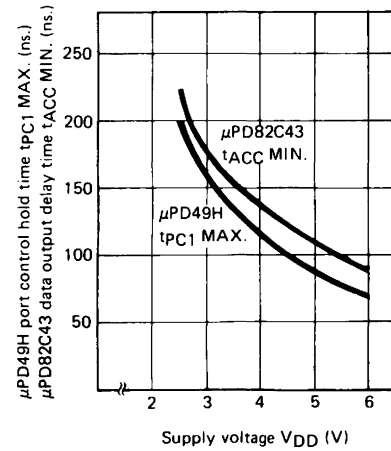
CHARACTERISTIC CURVES (Continued)

t_{CY} vs. V_{DD}

(T_a=−40~+85°C)



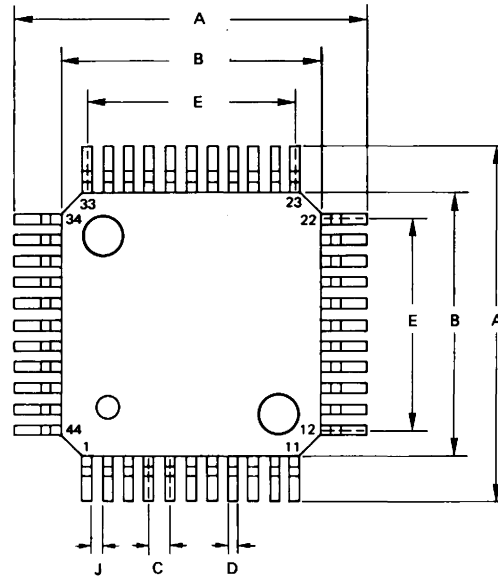
t_{PC1} MAX. (μPD49H)/t_{ACC} MIN. (μPD82C43) vs. V_{DD}

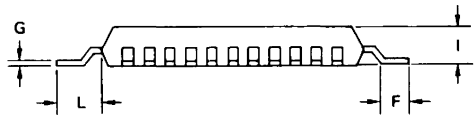


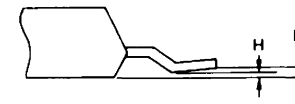
Remarks: The operation guaranteed region and characteristics curves not shown are all reference values.

PACKAGE DIMENSIONS
μPD49HG
44 PIN PLASTIC
FLAT PACK

ITEM	MILLIMETERS	INCHES
A	13.6 ± 0.4	0.54 ± 0.016
B	10	.394
C	0.8 ± 0.15	.03 ± 0.006
D	.35 $^{+0.3}_{-0.1}$	.014 $^{+.01}_{-.004}$
E	8.0 ± 0.3	.315 ± .012
F	1.0 ± 0.2	.39 ± .008
G	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
H	0.0 ± 0.1	0.0 ± .004
I	1.4 $^{+0.2}_{-0.1}$	0.06 $^{+0.008}_{-0.004}$
J	0.2 min	0.008 min
K	0.0 ± 0.2	0.0 ± 0.008
L	1.8 ± 0.2	0.071 ± 0.008







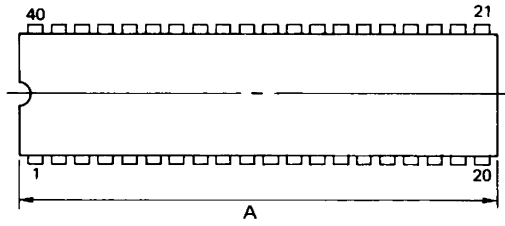
Lead bend (enlarged view)

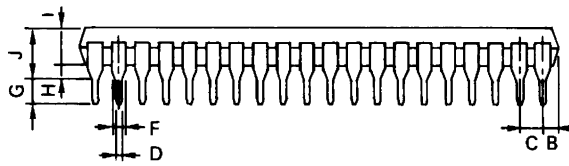
PACKAGE DIMENSIONS
μPD80C49HC/
μPD80C39HC
40 PIN PLASTIC DIP

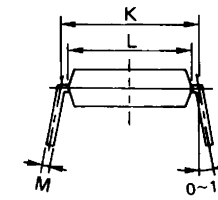
ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T. P.)	0.100 (T. P.)
D	0.50 ± 0.10	0.020 $^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6 ± 0.3	0.142 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T. P.)	0.600 (T. P.)
L	13.2	0.520
M	0.25 $^{+0.10}_{-0.05}$	0.010 $^{+0.004}_{-0.003}$
N	0.25	0.01

Notes: 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T. P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.







CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

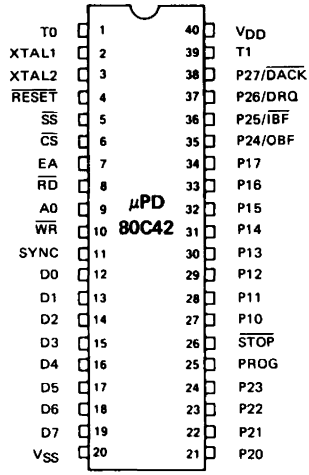
DESCRIPTION

The μPD80C42 is designed to function as a slave CPU, particularly as an intelligent peripheral controller in the microcomputer system using the μCOM84/84C or μCOM85 as a master CPU. Interface with the system data bus can be easily made via the internal interface register (data bus buffer register, status register). The program memory is 2K x 8 bits. The data memory is 128 x 8 bits. 16 I/O ports (2 x 8 bits) compatible with TTL can be easily extended by using the μPD82C43 that is directly connectable to the μPD80C42.

FEATURES

- Single-chip microcomputer
- Compatible with the μCOM84/84C and μCOM85
- Instruction cycle: 1.25 μs/12 MHz
- Program memory (ROM) : 2K x 8 bits
- Data memory (RAM) : 128 x 8 bits
- Input/output port (P_{10-17}, P_{20-27}) : 2 x 8 bits
- Asynchronous slave – Master interface
  2 data registers: DBBIN, DBBOUT
  8-bit status
- Internal timer/counter: 8 bits
- 2 pairs of working registers (2 x 8 x 8 bits)
- 8-level stack
- Internal clock generator
- Interrupt function
- DMA function
- Easy expandable I/O port
- Single-step operation available
- Standby function
- CMOS
- Single power supply: +2.5V ~ +6.0V
- Intel 8042 pin compatible
- 40-pin plastic DIP

PIN CONFIGURATION

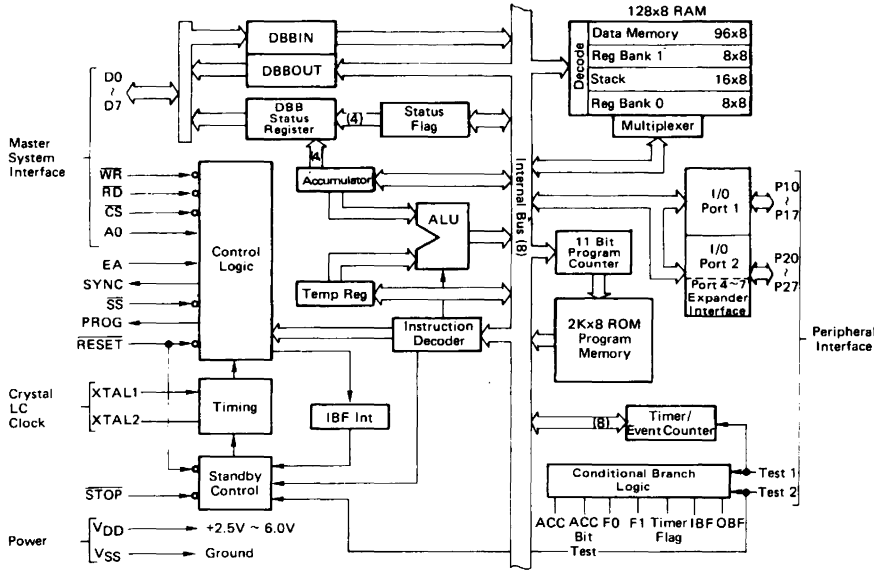


PIN IDENTIFICATION

NO.	PIN SYMBOL	PIN NAME	FUNCTION
1	T0	Test 0	Testable input using conditional jump instructions JT0 and JNT0. Also enables clock output via the ENT0 CLK instruction.
2	XTAL1	Crystal 1	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. May also be used as an input for external clock signals. (Non-TTL-compatible V_{IH}.)
3	XTAL2	Crystal 2	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. (Non-TTL-compatible V_{IH}.)
4	$\overline{RESET}$	Reset	Active-low input line that initializes the processor. Also used to release both the Halt and Stop modes.
5	$\overline{SS}$	Single Step	Active-low input line, that, in conjunction with ALE, causes the processor to single-step through a program one instruction at a time.
6	$\overline{CS}$	Chip Select	This is an input for chip select signal. When 0 (low-level) is input to this pin, the data bus is enabled.
7	EA	External Access	Input line that inhibits internal program memory fetches and initiates access of external program memory. Essential for system testing and may also be used for program debugging.
8	$\overline{RD}$	Read	Active-low output strobe line that is used to read data from external data memory.
9	A0		Indicates the address input from the master CPU and the kind of data on the data bus. • Read cycle A0 = 0: Data A0 = 1: Status • Write cycle A0 = 0: Data A0 = 1: Command
10	$\overline{WR}$	Write	Active-low output strobe line that is used to write data into external data memory.
11	SYNC		This is an output pin for a signal output at each machine cycle, and used for strobe of external circuit or single-step operation.
12-19	DB_0-DB_7	Bus	These I/O lines constitute an 8-bit bidirectional data/address bus. Synchronous read and write operations can be performed on this bus using $\overline{RD}$ and $\overline{WR}$ signals. Data driven out on the bus by an OUTL BUS instruction is statically latched. The address of external memory is available on the bus at the falling edge of ALE when reading from external program memory or writing to and reading from external data memory. During external program memory fetches, the least-significant 8 bits of the external program memory address are driven out on the bus and the addressed instruction is fetched using $\overline{PSEN}$. When no external memory is used, the bus can serve as a true bidirectional 8-bit port. Information is strobed in or out by the $\overline{RD}$ and $\overline{WR}$ signals.
20	V_{SS}	Ground	Ground potential.
21-24, 35-38	P_{20}-P_{27}	Port 2	These lines constitute Port 2, an 8-bit quasi-bidirectional port. During external program memory fetches P_{20}-P_{23} output the most-significant 4 bits of the external program memory address. Lines P_{20}-P_{23} can also be used as a 4-bit I/O expander bus to interface with the optional μPD82C43 I/O expander.
25	PROG	Program Pulse	This line is used as an output strobe when interfacing with the optional μPD82C43 I/O expander.
26	$\overline{STOP}$	Stop	Used for controlling the hardware STOP mode.
27-34	P_{10}-P_{17}	Port 1	These lines constitute Port 1, an 8-bit, generalpurpose quasi-bidirectional port.
39	T1	Test 1	Testable input using conditional jump instructions JT1 and JNT1. Can also be used as the timer/counter input line via the STRT CNT instruction.
40	V_{DD}	Primary Power Supply	Power supply. V_{CC} must be between +2.5V to +6V for normal operation. In Stop mode, V_{CC} must be at least +2V to ensure data retention.

Note: $\overline{CS}$, A0, $\overline{RD}$, $\overline{WR}$, TEST0 and TEST1 pins must not be floated to prevent a malfunction.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature, T_{opt}	−40°C to +85°C
Storage Temperature (Plastik Package), T_{stg}	−65°C to +150°C
Voltage on Any Pin, $V_{I/O}$	V_{SS} −0.3V to V_{DD} +0.3V
Supply Voltage, V_{DD}	V_{SS} −0.3 to +7V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS $T_a = -40°C \sim +85°C$, $V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Low	V_{IL}		−0.3		+0.8	V
Input Voltage High	V_{IH}	Except $\overline{RESET}$, XTAL1, XTAL2	2.2		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2	V_{DD} −1		V_{DD}	V
Output Voltage Low	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output Voltage High	V_{OH}	D0-D7, SYNC, PROG I_{OH} = −400 μA	2.4			V
	V_{OH1}	PORT1, PORT2, I_{OH} = −50 μA	2.4			V
	V_{OH2}	All Outputs, I_{OH} = −0.2 μA	V_{DD} −0.5			V
Input Current	I_{ILP}	PORT1, PORT2; $V_I \leqslant V_{IL}$			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T0, T1, $\overline{STOP}$, $\overline{CS}$, A0, $\overline{RD}$, $\overline{WR}$; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±3	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqslant V_O \leqslant V_{DD}$ High Impedance, D0-D7, PORT			±1	μA
Standby Current	I_{DD1}	HALT Mode; t_{CY} = 1.25 μs		1.5	3.0	mA
	I_{DD2}	STOP Mode*		1	20	μA
Supply Current	I_{DD}	t_{CY} = 1.25 μs		10	20	mA
Data Retention Voltage	V_{DDDR}	$\overline{STOP}$ mode ($\overline{STOP}$, $\overline{RESET} \leqslant 0.4V$) or RESET ($\overline{RESET} \leqslant 0.4V$)	2.0			V

Note *: The input pin voltage is $V_I \leqslant V_{IL}$ or $V_I \geqslant V_{IH}$.

AC CHARCTERISTICS $T_a = -40$ to $+85°C$, $V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

DBB READ:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$, A0 Setup to $\overline{RD}$ ↓	t_{AR}		0			ns
$\overline{CS}$, A0 Hold from $\overline{RD}$ ↑	t_{RA}		0			ns
$\overline{RD}$ Pulse Width	t_{RR}		200			ns
$\overline{CS}$, A0 to Data Output Delay	t_{AD}	*1			150	ns
$\overline{RD}$ ↓ to Data Output Delay	t_{RD}	*1			140	ns
$\overline{RD}$ ↑ to Data Float Delay	t_{DF}				85	ns
Cycle Time	t_{CY}		1.25		15	μs

DBB WRITE:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$, A0 Setup to $\overline{WR}$ ↓	t_{AW}		0			ns
$\overline{CS}$, A0 Hold from $\overline{WR}$ ↑	t_{WA}		0			ns
$\overline{WR}$ Pulse Width	t_{WW}		200			ns
Data Setup to $\overline{WR}$ ↑	t_{DW}		130			ns
Data Hold from $\overline{WR}$ ↑	t_{WD}		0			ns

PORT2:

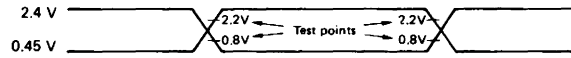
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Port Control Setup to PROG ↓	t_{CP}	*2	100			ns
Port Control Hold from PROG ↓	t_{PC}	*3	0		80	ns
Input Data Setup to PROG ↓	t_{PR}	*2			650	ns
Input Data Hold from PROG ↑	t_{PF}	*3	0		150	ns
Output Data Setup to PROG ↑	t_{DP}	*2	200			ns
Output Data Hold from PROG ↑	t_{PD}	*3	60			ns
PROG Pulse Width	t_{PP}		700			ns

DMA:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{DACK}$ Setup to $\overline{RD}$, $\overline{WR}$	t_{ACC}		0			ns
$\overline{DACK}$ Hold from $\overline{RD}$, $\overline{WR}$	t_{CAC}		0			ns
$\overline{DACK}$ to Data Output Delay	t_{ACD}				140	ns
$\overline{RD}$, $\overline{WR}$ to DRQ Clear Delay	t_{CRQ}	*4			130	ns

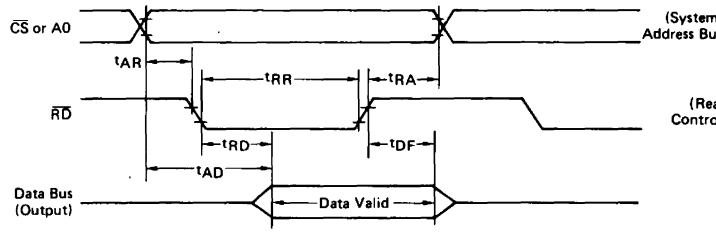
*1: $C_L = 100$ pF
*2: $C_L = 80$ pF
*3: $C_L = 20$ pF
*4: $C_L = 150$ pF

AC TEST INPUT/OUTPUT WAVEFORM

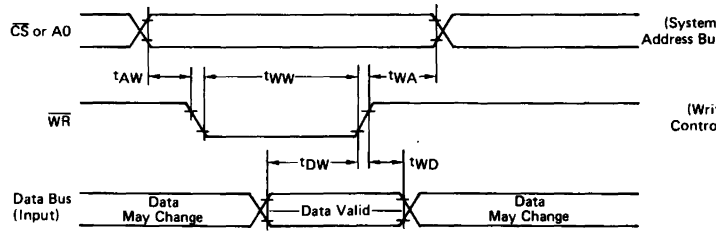


TIMING WAVEFORMS

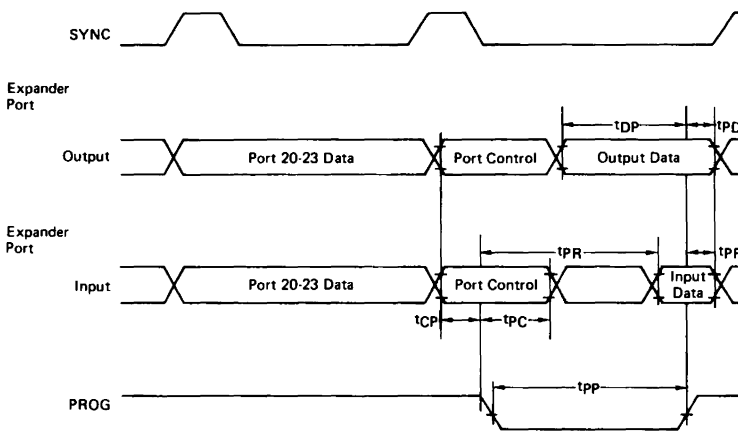
Read Operation (DBBOUT Register)



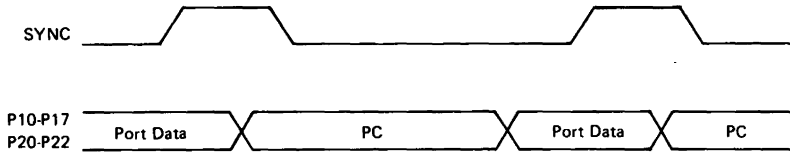
Write Operation (DBBIN Register)



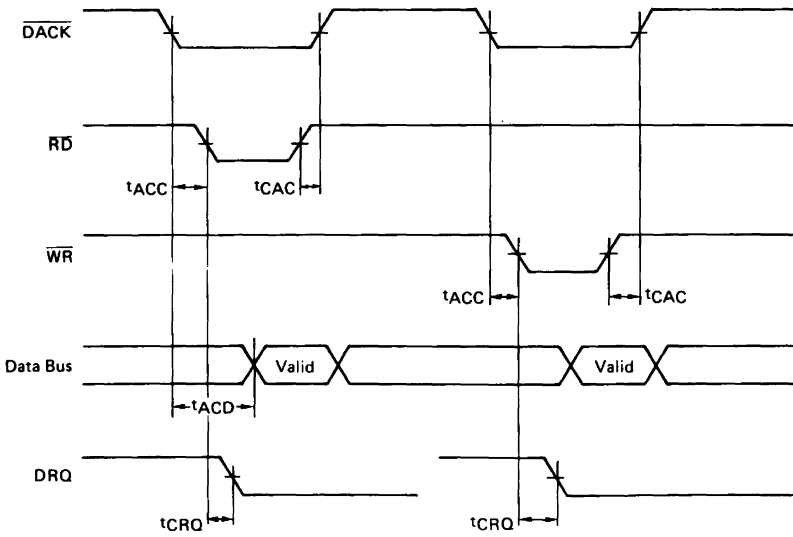
Port 2



Port (EA=1)


SYNC
P10-P17
P20-P22
Port Data
PC
Port Data
PC

DMA

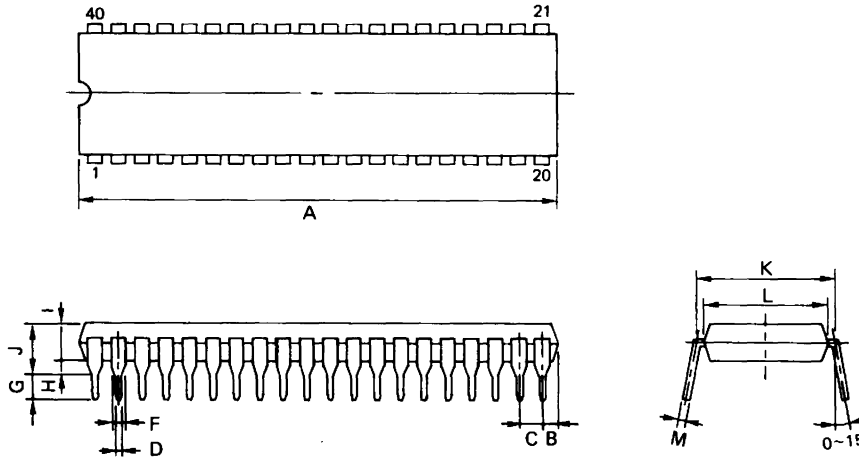

DACK
RD
tACC
tCAC
WR
tACC
tCAC
Data Bus
Valid
Valid
tACD
DRQ
tCRQ
tCRQ

PACKAGE DIMENSIONS
μPD80C42C
40 PIN PLASTIC DIP

ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T. P.)	0.100 (T. P.)
D	0.50 ± 0.10	0.020 $^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6 ± 0.3	0.142 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T. P.)	0.600 (T. P.)
L	13.2	0.520
M	0.25 $^{+0.10}_{-0.05}$	0.010 $^{+0.004}_{-0.003}$
N	0.25	0.01

Notes: 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T. P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.



CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

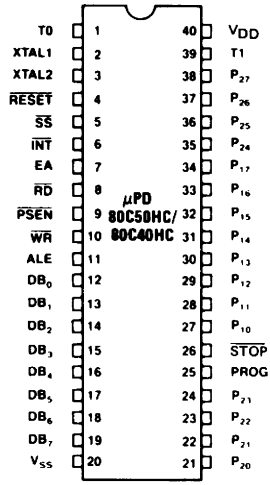
DESCRIPTION

The μPD80C50H is a single chip 8-bit microcomputer containing 8-bit CPU, ROM, RAM, I/O ports and control circuit on one CMOS chip. The μPD80C40H is the product in which the ROM is eliminated from the μPD80C50H. The μPD80C50H/40H, fabricated by CMOS technology, realizes low power consumption and data retention is also available with less power consumption.

FEATURES

- Single chip 8-bit microcomputer
- 98 instructions
- Instruction cycle: 1.25 μs/12 MHz
- Operating function
  Addition, logic operation, and decimal adjust
- ROM 4K x 8 bits (μPD80C50H)
- RAM 256 x 8 bits
- Stand-by function
- 8-level stack
- Two sets of working registers
- Interrupt capability
- Two test inputs
- Internal Timer/Event Counter
- Easy expandable Memory and I/O ports
- Input/Output ports
  Input/Output ports: 8 bits x 2
  Data bus (alternative for I/O ports): 8 bits x 1
- Single step function
- Internal Clock generator
- CMOS
- Single power supply: +2.5 ~ +6.0V
- 40 pin plastic DIP (μPD80C50HC/80C40HC) and 44 pin plastic FLAT Pack (μPD80C50HG)
- Intel 8050H, 8040H pin compatible

PIN CONFIGURATION



PIN IDENTIFICATION

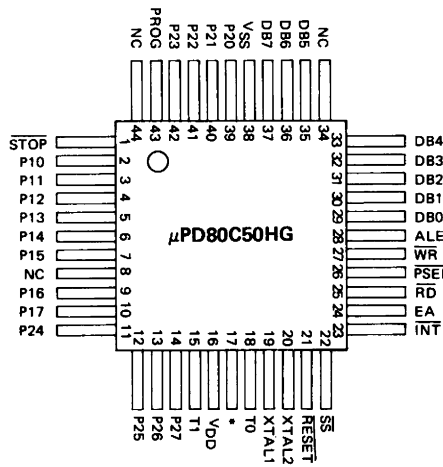
A.
μPD80C50HC/
μPD80C40HC
(40 PIN PLASTIC DIP)

B.
μPD80C50HG
(44 PIN PLASTIC
FLAT PACK)

PIN				
B.	A.	SYMBOL	NAME	FUNCTION
18	1	T0	Test 0	Testable input using conditional jump instructions JT0 and JNT0. Also enables clock output via the ENT0 CLK instruction.
19	2	XTAL1	Crystal 1	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. May also be used as an input for external clock signals. (Non-TTL-compatible V_{IH}.)
20	3	XTAL2	Crystal 2	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. (Non-TTL-compatible V_{IH}.)
21	4	$\overline{RESET}$	Reset	Active-low input line that initializes the processor. Also used to release both the Halt and Stop modes. ①
22	5	$\overline{SS}$	Single Step	Active-low input line, that, in conjunction with ALE, causes the processor to single-step through a program one instruction at a time.
23	6	$\overline{INT}$	Interrupt	Active-low input line that causes an interrupt if an enable instruction has been executed. A reset disables the interrupt. May be used as a testable input with a conditional jump instruction. Can also be used to release the Halt mode.
24	7	EA	External	Input line that inhibits internal program memory fetches and initiates access of external program memory. Essential for system testing and may also be used for program debugging.
25	8	$\overline{RD}$	Read	Active-low output strobe line that is used to read data from external data memory.
26	9	$\overline{PSEN}$	Program Store Enable	Active-low output line that is used to fetch instructions from external program memory.
27	10	$\overline{WR}$	Write	Active-low output strobe line that is used to write data into external data memory.
28	11	ALE	Address Latch Enable	Output line for address latch enable. At the falling edge of ALE, the address of either external data memory or external program memory is available on the bus.
29-33, 35-37	12-19	DB_0-DB_7	Bus	These I/O lines constitute an 8-bit bidirectional data/address bus. Synchronous read and write operations can be performed on this bus using $\overline{RD}$ and $\overline{WR}$ signals. Data driven out on the bus by an OUTL BUS instruction is statically latched. The address of external memory is available on the bus at the falling edge of ALE when reading from external program memory or writing to and reading from external data memory. During external program memory fetches, the least-significant 8 bits of the external program memory address are driven out on the bus and the addressed instruction is fetched using $\overline{PSEN}$. When no external memory is used, the bus can serve as a true bidirectional 8-bit port. Information is strobed in or out by the $\overline{RD}$ and $\overline{WR}$ signals.
38	20	V_{SS}	Ground	Ground potential.
39-42, 11-14	21-24, 35-38	P_{20}-P_{27}	Port 2	These lines constitute Port 2, an 8-bit quasi-bidirectional port. During external program memory fetches P_{20}-P_{23} output the most-significant 4 bits of the external program memory address. Lines P_{20}-P_{23} can also be used as a 4-bit I/O expander bus to interface with the optional μPD82C43 I/O expander.
43	25	PROG	Program Pulse	This line is used as an output strobe when interfacing with the optional μPD82C43 I/O expander.
1	26	$\overline{STOP}$	Stop	Used to control the hardware STOP mode.
2- 7,	27-34	P_{10}-P_{17}	Port 1	These lines constitute Port 1, an 8-bit, generalpurpose quasi-bidirectional port.
15	39	T1	Test 1	Testable input using conditional jump instructions JT1 and JNT1. Can also be used as the timer/counter input line via the STRT CNT instruction.
16	40	V_{DD}	Primary Power Supply	Power supply. V_{CC} must be between +2.5V to +6V for normal operation. In Stop mode, V_{CC} must be at least +2V to ensure data retention.

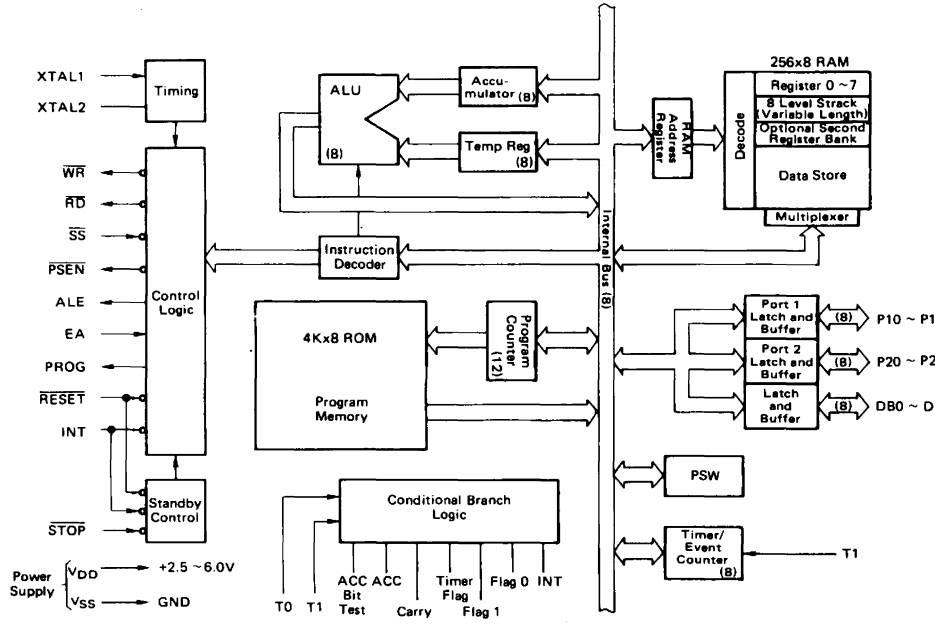
Note: ① The pulse width of RESET must be a minimum of 5 machine cycles in length following oscillator stabilization to reinitialize the processor and stabilize CPU operation. At power-up, the states of the output lines are undefined until completion of reset.

PIN CONFIGURATION
μPD80C50HG
(44 PIN FLAT PACKAGE)



* INTERNAL CONNECTION IT IS PROHIBITED TO USE PIN 17

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

T_a = 25°C	
Operating Temperature, T_{opt}	−40°C to +85°C
Storage Temperature (Plastic Package), T_{stg}	−65°C to +150°C
Voltage on Any Pin, $V_{I/O}$	V_{SS} −0.3V to V_{DD} +0.3V
Supply Voltage, V_{DD}	V_{SS} −0.3 to +7V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS $T_a = -40°C \sim +85°C$, $V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		+0.8	V
Input High Voltage	V_{IH}	Except XTAL1, XTAL2, $\overline{RESET}$, $\overline{SS}$	$V_{DD}-2$		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$	$V_{DD}-1$		V_{DD}	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.0$ mA			+0.45	V
Output High Voltage	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; $I_{OH} = -400\ \mu A$	2.4			V
	V_{OH1} ①	PORT1, PORT2; $I_{OH} = -5\ \mu A$ (Type 0)	2.4			V
		PORT1, PORT2; $I_{OH} = -50\ \mu A$ (Type 1)	2.4			V
Input Current	I_{ILP} ①	PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±3	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqslant V_O \leqslant V_{DD}$ High Impedance, BUS, T0 ③			±1	μA
Standby Current	I_{DD1}	HALT mode; $t_{CY} = 1.25\ \mu s$		1.5	3.0	mA
	I_{DD2}	STOP Mode ②		1	20	μA
Supply Current (Total)	I_{DD}	$t_{CY} = 1.25\ \mu s$		6	18	mA
Data Retention Voltage	V_{DDDR}	at the hardware STOP mode ($\overline{STOP}$, $\overline{RESET} \leqslant 0.4V$) or or $\overline{RESET}$ ($\overline{RESET} \leqslant 0.4V$)	2.0			V

DC CHARACTERISTICS $T_a = -40°C \sim +85°C$, $V_{DD} = +2.5V \sim +6.0V$, $V_{SS} = 0V$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL}		−0.3		0.18 V_{DD}	V
Input High Voltage	V_{IH}	Except XTAL1, XTAL2, $\overline{RESET}$, $\overline{SS}$	0.7 V_{DD}		V_{DD}	V
	V_{IH1}	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$	0.8 V_{DD}		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 1.0 mA			0.45	V
Output High Voltage	V_{OH}	BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −100 μA	0.75 V_{DD}			V
	V_{OH1} ①	PORT1, PORT2; I_{OH} = −1 μA (Type 0)	0.7 V_{DD}			V
		PORT1, PORT2; I_{OH} = −10 μA (Type 1)	0.7 V_{DD}			V
Input Current	I_{ILP} ①	PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 0)		−15	−40	μA
		PORT1, PORT2; $V_I \leqslant V_{IL}$ (Type 1)			−500	μA
	I_{ILC}	$\overline{SS}$, $\overline{RESET}$; $V_I \leqslant V_{IL}$			−40	μA
Input Leakage Current	I_{LI1}	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±1	μA
	I_{LI2}	EA; $V_{SS} \leqslant V_I \leqslant V_{DD}$			±5	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqslant V_O \leqslant V_{DD}$ ③ High Impedance, BUS, T0			±1	μA
Standby Current	I_{DD1}	HALT mode; V_{DD} = 3V; t_{CY} = 5 μs		0.3	0.6	mA
		HALT mode; V_{DD} = 6V; t_{CY} = 1.25 μs		2.0	4.0	mA
	I_{DD2}	STOP Mode ②; V_{DD} = 3V		1	20	μA
		STOP Mode ②; V_{DD} = 6V		1	50	μA
Supply Current	I_{DD}	V_{DD} = 3V; t_{CY} = 5 μs		2.0	5.0	mA
		V_{DD} = 6V; t_{CY} = 1.25 μs		10	25	mA

Notes:

① Option specification of type 0 and type 1 is available only for the μPD80C50H. The μPD80C40H has the type 0 only.

② The input pin voltage is $V_I \leqslant V_{IL}$ or $V_I \geqslant V_{IH}$.

③ Output pins of PORT1 and PORT2 specified as the type 2 are also included.

AC CHARACTERISTICS T_a = −40 to +85°C, V_{SS} = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	V_{DD} = +5V ±10%			V_{DD} = 2.5 to 6.0V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Cycle Time	t_{CY}		1.25		150	5		150	μs
ALE Pulse Width	t_{LL}		125			995			ns
Address Setup before ALE	t_{AL}		140			890			ns
Address Hold from ALE	t_{LA}		45			295			ns
Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	④	425			2300			ns
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}		300			1800			ns
Data Setup before $\overline{WR}$	t_{DW}		340			1965			ns
Data Hold after $\overline{WR}$	t_{WD}	⑤	45			295			ns
Data Hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}		0		95	0		470	ns
$\overline{RD}$ to Data in	t_{RD1}				300			1800	ns
$\overline{PSEN}$ to Data in	t_{RD2}				175			1300	ns
Address Setup before $\overline{WR}$	t_{AW}		350			1850			ns
Address Setup before Data in ($\overline{RD}$)	t_{AD1}				700			3585	ns
Address Setup before Data in ($\overline{PSEN}$)	t_{AD2}				500			2750	ns
Address Float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	④	105			600			ns
Address Float to $\overline{PSEN}$	t_{AFC2}		5			125			ns
ALE to Control Signal ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}		175			925			ns
ALE to Control Signal ($\overline{PSEN}$)	t_{LAFC2}		50			425			ns
Control Signal ($\overline{RD}$, $\overline{WR}$, PROG) to ALE	t_{CA1}		35			285			ns
Control Signal ($\overline{PSEN}$) to ALE	t_{CA2}		280			1285			ns
Port Control Setup before Falling Edge of PROG	t_{CP}	⑥	85			460			ns
Port Control Hold after Falling Edge of PROG	t_{PC1}	⑥, ⑦	0		80	0		200 ⑧	ns
	t_{PC2}	⑥, ⑧	135			1135			ns
PROG to Time P2 Input must be Valid	t_{PR}				585			2715	ns
Input Data Hold Time	t_{PF}		0		125	0		500	ns
Output Data Setup Time	t_{DP}		350			1850			ns
Output Data Hold Time	t_{PD}		75			450			ns
PROG Pulse Width	t_{PP}	⑥	625			3250			ns
PORT2 I/O Data Setup Time	t_{PL}		135			1135			ns
PORT2 I/O Data Hold Time	t_{LP}		5			125			ns
ALE to PORT Output	t_{PV}				475			1600	ns
T0 Clock Period	t_{OPRR}		250			1000			ns

④ Control Output: C_L = 80 pF, BUS Output: C_L = 150 pF
⑤ C_L = 20 pF
⑥ Control Output: C_L = 80 pF
⑦ At execution of MOVD A, Pp instruction
⑧ At execution of MOVD Pp, A; ANLD Pp, A; ORLD Pp, A instruction

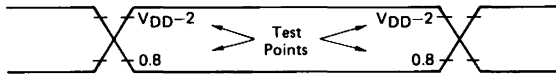
t_{CY}-DEPENDENT BUS TIMING DEFINITIONS

PARAMETER	CALCULATION FORMULA	MIN	MAX	UNIT
t_{LL}	(7/30) T – 170	●		ns
t_{AL}	(1/ 5) T – 110	●		ns
t_{LA}	(1/15) T – 40	●		ns
t_{CC1}	(1/ 2) T – 200	●		ns
t_{CC2}	(2/ 5) T – 200	●		ns
t_{DW}	(13/30) T – 200	●		ns
t_{WD}	(1/15) T – 40	●		ns
t_{DR}	(1/10) T – 30		●	ns
t_{RD1}	(2/ 5) T – 200		●	ns
t_{RD2}	(3/10) T – 200		●	ns
t_{AW}	(2/ 5) T – 150	●		ns
t_{AD1}	(23/30) T – 250		●	ns
t_{AD2}	(3/ 5) T – 250		●	ns
t_{AFC1}	(2/15) T – 65	●		ns
t_{AFC2}	(1/30) T – 40	●		ns
t_{LAFC1}	(1/ 5) T – 75	●		ns
t_{LAFC2}	(1/10) T – 75	●		ns
t_{CA1}	(1/15) T – 50	●		ns
t_{CA2}	(4/15) T – 50	●		ns
t_{CP}	(1/10) T – 40	●		ns
t_{PC2}	(4/15) T – 200	●		ns
t_{PR}	(17/30) T – 120		●	ns
t_{PF}	(1/10) T		●	ns
t_{DP}	(2/ 5) T – 150	●		ns
t_{PD}	(1/10) T – 50	●		ns
t_{PP}	(7/10) T – 250	●		ns
t_{PL}	(4/15) T – 200	●		ns
t_{LP}	(1/30) T – 40	●		ns
t_{PV}	(3/10) T + 100		●	ns
t_{OPRR}	(1/ 5) T	●		ns
t_{CY}	$(1/f_{XTAL}) \times 15$			μs

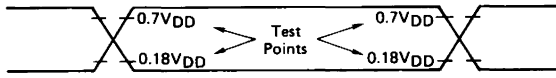
Remarks: $T = t_{CY}$

AC TIMING TEST POINTS (Except $\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$)

(a) V_{DD} = +5V ± 10 %

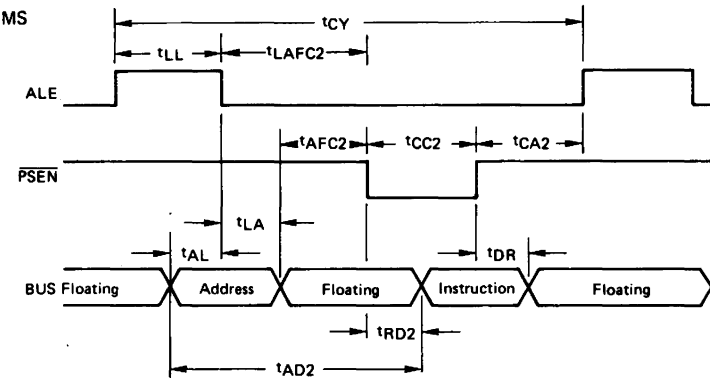


(b) V_{DD} = +2.5 to 6.0V

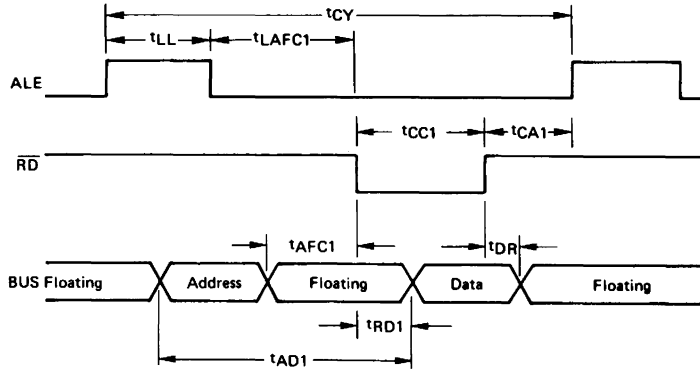


TIMING WAFEFORMS

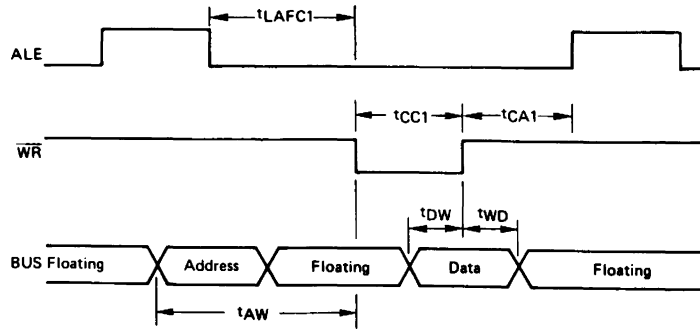
Instruction fetch from external program memory



Read from external data memory

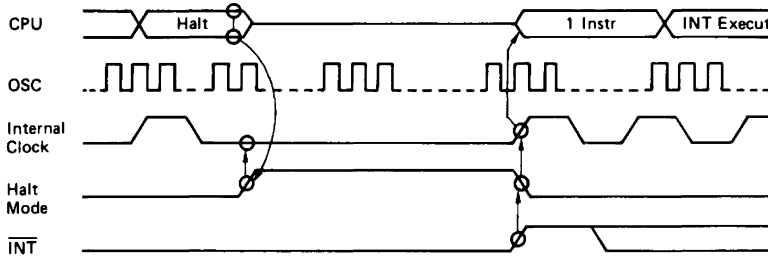


Write to external data memory

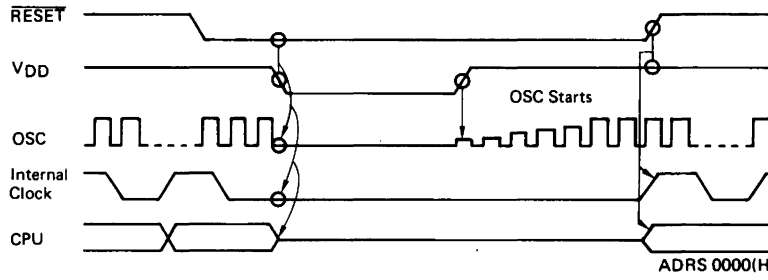


Low Power Standby Operation

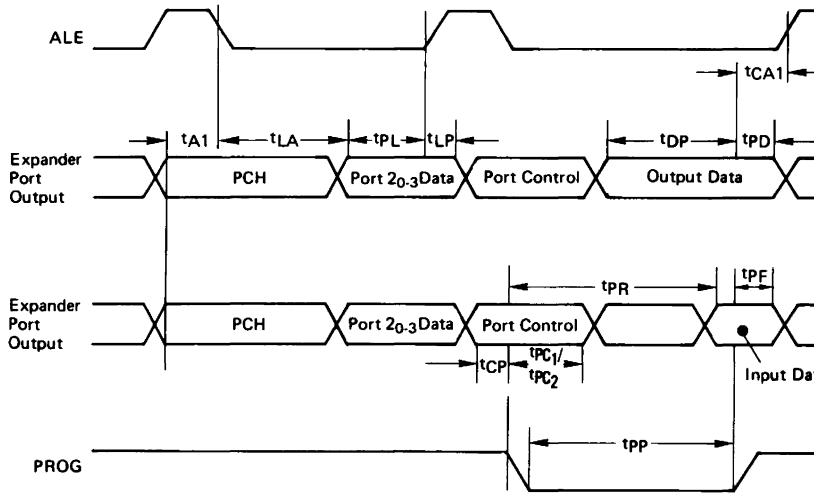
1) Halt Mode (When EI)



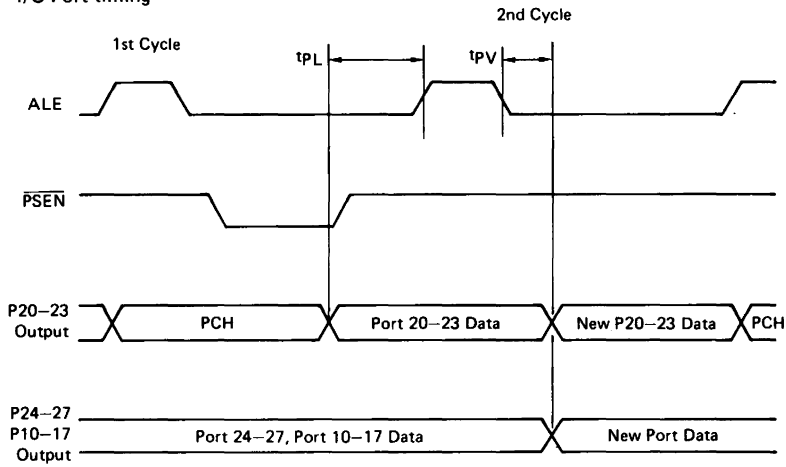
2) Stop Mode



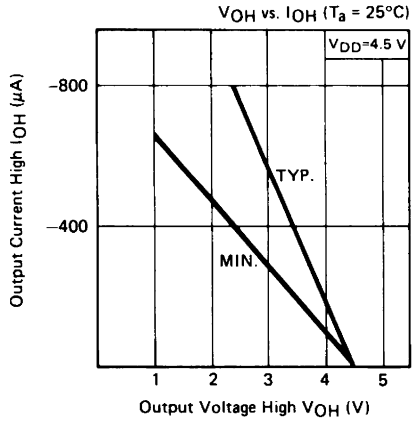
Port 2 Timing

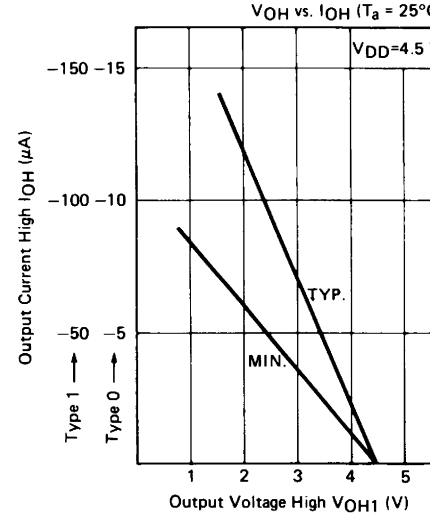


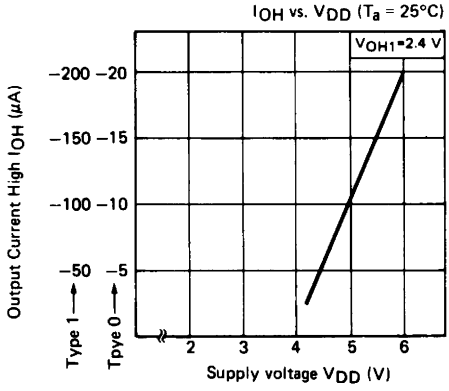
I/O Port timing

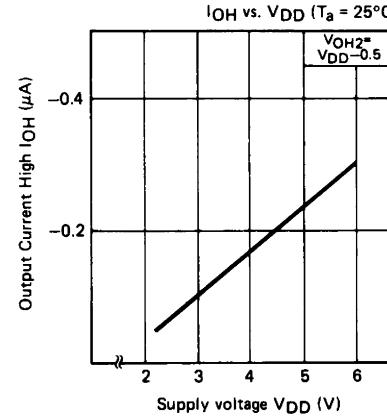


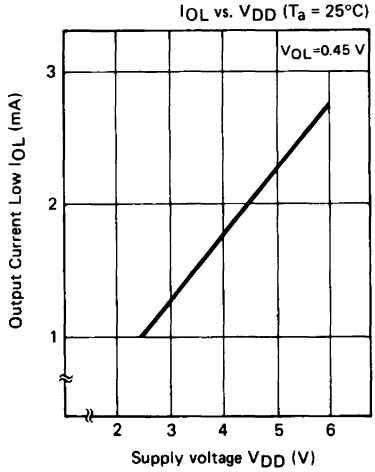
CHARACTERISTICS CURVES

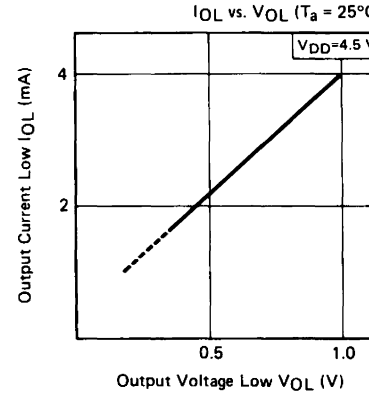


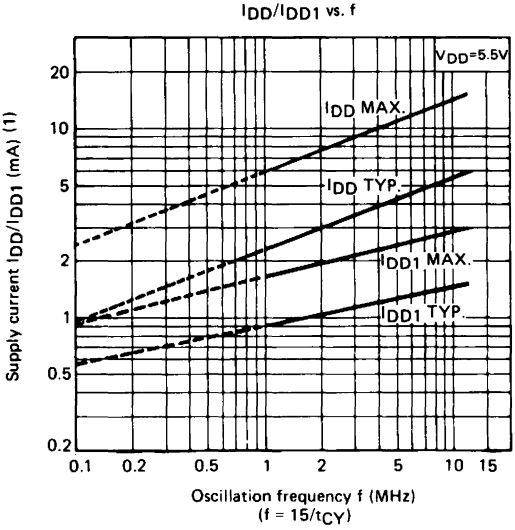


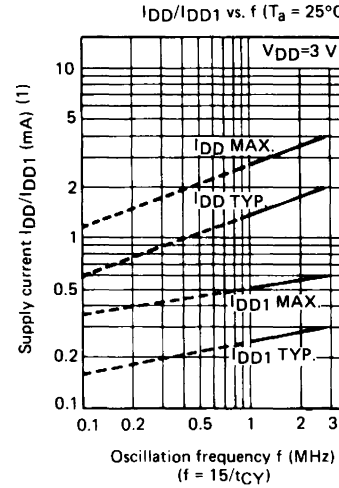










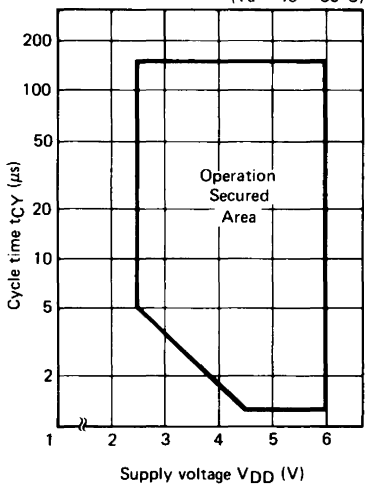


Note:

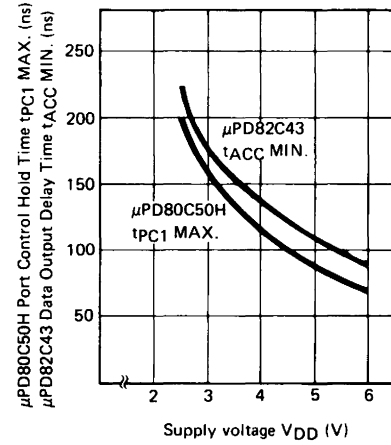
1) Curves below 1 MHz show characteristics for external oscillation.

t_{CY} vs. V_{DD}

(T_a=−40~+85°C)



t_{PC1} MAX. (μPD80C50H)/t_{ACC} MIN. (μPD82C43) vs. V_{DD} (T_a = 25°C)



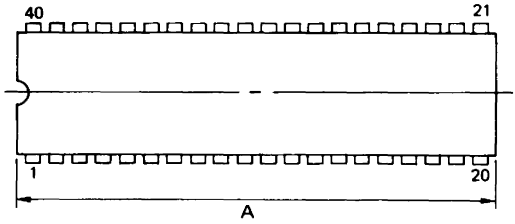
Note: Curves without "operation secured area" show reference data.

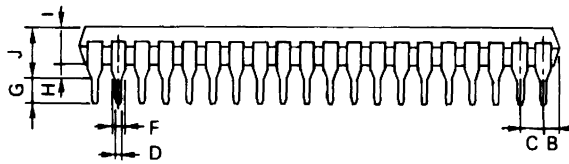
PACKAGE DIMENSIONS
μPD80C50HC/
μPD80C40HC
40 PIN PLASTIC DIP

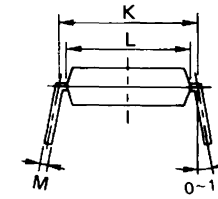
ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T. P.)	0.100 (T. P.)
D	0.50 ± 0.10	0.020 $^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6 ± 0.3	0.142 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T. P.)	0.600 (T. P.)
L	13.2	0.520
M	0.25 $^{+0.10}_{-0.05}$	0.010 $^{+0.004}_{-0.003}$
N	0.25	0.01

Notes: 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T. P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

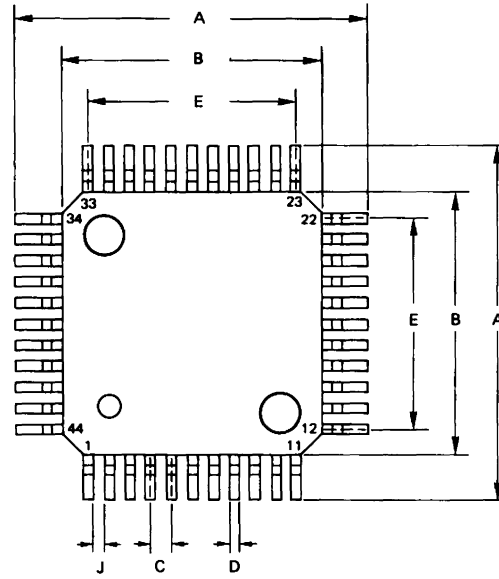


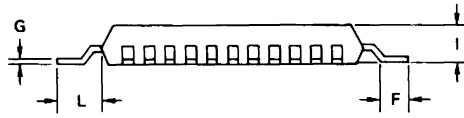


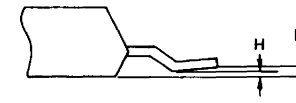


PACKAGE DIMENSIONS
μPD80C50HG
44 PIN PLASTIC
FLAT PACK

ITEM	MILLIMETERS	INCHES
A	13.6 ± 0.4	0.54 ± 0.016
B	10	.394
C	0.8 ± 0.15	.03 ± 0.006
D	.35 $^{+0.3}_{-0.1}$	.014 $^{+.01}_{-.004}$
E	8.0 ± 0.3	.315 ± .012
F	1.0 ± 0.2	.39 ± .008
G	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
H	0.0 ± 0.1	0.0 ± .004
I	1.4 $^{+0.2}_{-0.1}$	0.06 $^{+0.008}_{-0.004}$
J	0.2 min	0.008 min
K	0.0 ± 0.2	0.0 ± 0.008
L	1.8 ± 0.2	0.071 ± 0.008







Lead bend (enlarged view)

CMOS-DESIGN RECOMMENDATIONS

In order to maximize circuit reliability please note the general CMOS design rules.

For example:

1) Don't leave unused pins open, except they are outputs or not connected.

2) Never exceed the max. voltage range.

3) Avoid accurance of very fast voltage spikes or transission rate on the power supply pin.

CHAPTER 4

THE μCOM87 FAMILY

μPD7800
μPD7801
μPD7802
μPD78C05A
μPD78C06A
μPD7809
μPD7808
μPD7807
μPD78P09
μPD7810,H
μPD7811,H
μPD78PG11,E
μPD78C10
μPD78C11
μPD78C14

THE μCOM 87 FAMILY

8-BIT SINGLE CHIP MICROCOMPUTER

μPD7800 μPD7801 μPD7802 μPD78C05A
μPD78C06A μPD7807 μPD7808 μPD7809
μPD78P09 μPD7810 μPD7811 μPD78PG11E
μPD7810H μPD7811H μPD78C10 μPD78C11 μPD78C14

PRODUCT	PACKAGE	ROM RAM	INSTRUCTIONS I/O LINES	INTERRUPTS – EXTERNAL – INTERNAL	SPECIAL FEATURES
μPD7800	64 QUIL	– 128	140 48	3 2	EVACHIP FOR μPD7801/02
μPD7801	64 QUIL	4096 128	140 48	3 2	
μPD7802	64 QUIL	6144 64	140 48	3 2	
μPD78C05A	64 QUIL	– 128	101 46	2 1	EVACHIP FOR μPD78C06A CMOS-TECHNOLOGY
μPD78C06A	64 FLAT 64 QUIL	4096 128	101 46	2 1	CMOS
μPD7807	64 QUIL 64 SDIP	– 256	157 40	3 8	EVACHIP FOR μPD7809
μPD7808	64 QUIL 64 SDIP	4096 256	157 40	3 8	4K VERSION OF 7809
μPD7809	64 QUIL 64 SDIP	8192 256	157 40	3 8	8 COMPARATOR INPUTS, TWO 8-BIT TIMERS, ONE 16-BIT TIMER / COUNTER
μPD78P09	64 QUIL	8192 256	157 40	3 8	EPROM-VERSION OF μPD7809
μPD7810	64 QUIL 64 SDIP	– 256	157 44	3 8	EVACHIP FOR μPD7811
μPD7811	64 QUIL 64 SDIP	4096 256	157 44	3 8	8 A/D-CONVERTER INPUTS, TWO 8-BIT TIMERS, ONE 16-BIT TIMER / COUNTER
μPD78PG11E	64 QUIL	4096 256	157 44	3 8	PIGGY BACK VERSION OF μPD7811
μPD7810H	64 QUIL 64 SDIP	– 256	157 44	3 8	HIGH SPEED VERSION OF μPD7810 (15 MH_Z)
μPD7811H	64 QUIL 64 SDIP	4096 256	157 44	3 8	HIGH SPEED VERSION OF μPD7811 (15 MH_Z)
μPD78C10	64 QUIL 64 FLAT 64 SDIP	– 256	158 44	3 8	CMOS VERSION OF μPD7810
μPD78C11	64 QUIL 64 FLAT 64 SDIP	4096 256	158 44	3 8	CMOS VERSION OF μPD7811
μPD78C14	64 QUIL 64 FLAT 64 SDIP	16384 256	158 44	3 8	CMOS VERSION OF μPD7811

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER ROM-LESS DEVELOPMENT DEVICE

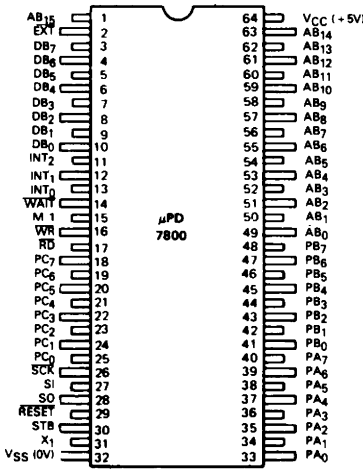
DESCRIPTION

The NEC μPD7800 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-channel Silicon Gate MOS Technology. Intended as a ROM-less development device for NEC μPD7801/7802 designs, the μPD7800 can also be used as a powerful microprocessor in volume production enabling program memory flexibility. Basic on-chip functional blocks include 128 bytes of RAM data memory, 8-bit ALU, 16-bit adress bus, 32 I/O lines, Serial I/O port, and 12-bit timer. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of 8080A/8085A peripheral and memory products. Total memory address space is 64K bytes.

FEATURES

- NMOS Silicon Gate Technology Requiring Single +5V Supply
- Single-Chip Microcomputer with On-Chip ALU, RAM and I/O
  - 128 Bytes RAM
  - 32 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five-Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 64K Byte Memory Address Range
- Wait State Capability
- Alternate Z80™ Type Register Set
- 140 powerful instructions
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack-Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities (DMA)

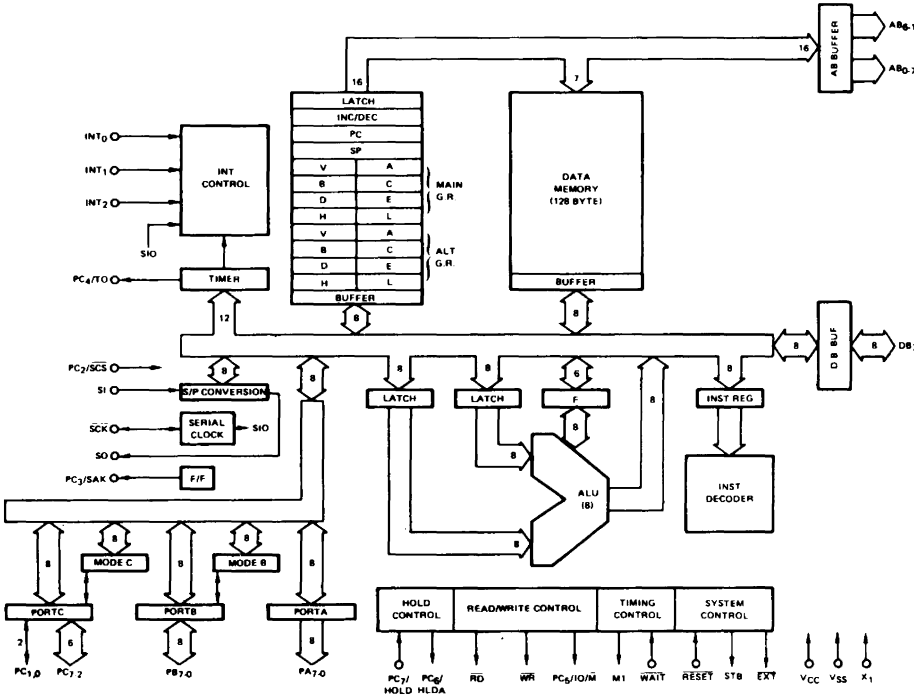
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
1, 49-63	AB_0-AB_{15}	(Tri-State, Output) 16-bit address bus.
2	$\overline{EXT}$	(Output) $\overline{EXT}$ is used to simulate μPD7801/7802 external memory reference operation. $\overline{EXT}$ distinguishes between internal and external memory references, and goes low when locations 4096 through 65407 are accessed.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state TW and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices on the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of $\overline{SCK}$.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of $\overline{SCK}$, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7800.
30	STB	(Output) Used to simulate μPD7801/7802 Port E operation, indicating that a Port E operation is being performed when active.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Architecturally consistent with μPD7801/7802 devices, the μPD7800 uses a slightly different pin-out to accommodate for the address bus and lack of on-chip clock generator. For complete μPD7800 functional operation, please refer to μPD7801 product information. Listed below are functional differences that exist between μPD7800 and μPD7801 devices.

μPD7800/7801 Functional Differences

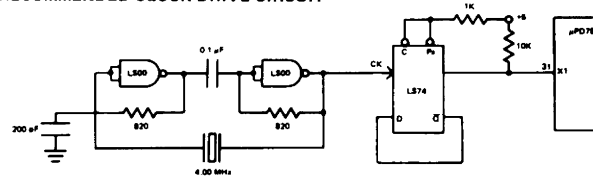
1. The functionality of μPD7801 Port E is somewhat different on the μPD7800. Because the μPD7800 contains no program memory, the address bus is made accessible to address external program memory. Thus, lines normally used for Port E operation with the μPD7801 are used as the address bus on the μPD7800. AB_0-AB_{15} is active during memory access 0 through 4095.
2. Consequently Port E instructions (PEX, PEN, and PER) have different functionality.

   PEX Instruction – The contents of B and C register are output to the address bus. The value 01H is output to the data bus. STB becomes active.

   PEN Instruction – B and C register contents are output to the address bus. The value 02H is output to the data bus. STB becomes active.

   PER Instruction – The address bus goes to the high impedance state. The value 04H is output to the data bus. STB becomes active.
3. ON-CHIP CLOCK GENERATOR. The μPD7800 contains no internal clock generator. An external clock source is input to the X_1 input.
4. PIN 30. This pin functions as the X_2 crystal connection on the μPD7801. On the μPD7800, pin 30 functions as a strobe output (STB) and becomes active when a Port E instruction is executed. This control signal is useful in simulating μPD7801 Port E operation – indicating that a port E operation is being performed.
5. PIN 2. Functions as the Φ out clock output used for synchronizing system external memory and I/O devices, on the μPD7801. On the μPD7800, this pin is used to simulate external memory reference operation of the μPD7801. $\overline{EXT}$ is used to distinguish between internal and external memory references and goes low when location 4096 through 65407 are accessed.

RECOMMENDED CLOCK DRIVE CIRCUIT



HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 4K ROM

PRODUCT DESCRIPTION

The NEC μPD7801 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-Channel Silicon Gate MOS technology.

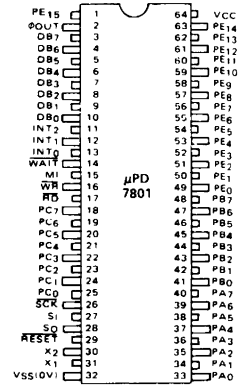
The NEC μPD7801 is intended to serve a broad spectrum of 8-bit designs ranging from enhanced single chip applications extending into the multi-chip microprocessor range. All the basic functional blocks – 4096 x 8 of ROM program memory, 128 x 8 of RAM data memory, 8-bit ALU, 48 I/O lines, Serial I/O port, 12-bit timer, and clock generator are provided on-chip to enhance standalone applications. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of the 8080A/ 8085A peripherals and memory products. Total memory space can be increased to 64K bytes.

The powerful 140 instructions coupled with 4K bytes of ROM program memory and 128 bytes of RAM data memory greatly extends the range of single chip microcomputer applications. Five level vectored interrupt capability combined with a 2 microsecond cycle time enable the μPD7801 to compete with multi-chip microprocessor systems with the advantage that most of the support functions are on-chip.

FEATURES

- NMOS Silicon Gate Technology Requiring +5V Supply
- Complete Single-Chip Microcomputer with On-Chip ROM, RAM and I/O
  - 4K Bytes ROM
  - 128 Bytes RAM
  - 48 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 60K Bytes External Memory Address Range
- On-Chip Clock Generator
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instructions
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities (DMA)

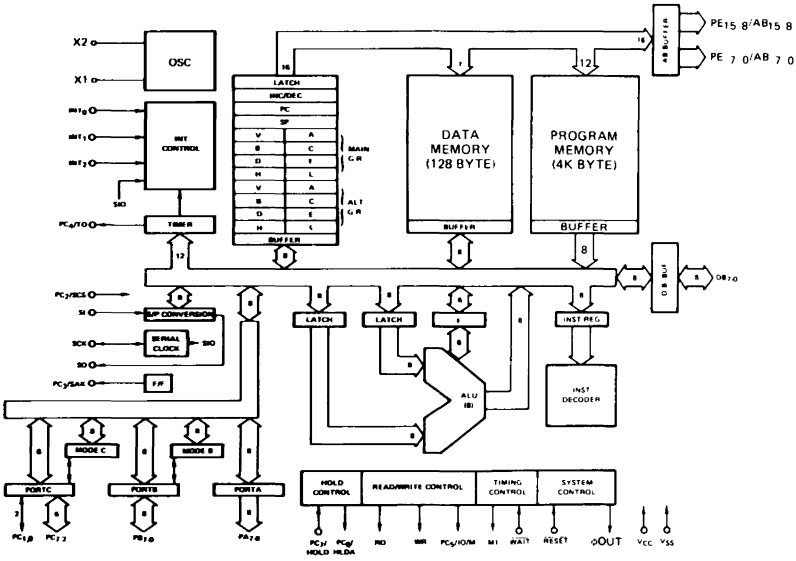
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
1, 49-63	PE_0/AB_0-PE_{15}/AB_{15}	(Tri-State, Output) 16-bit address bus.
2	ϕOUT	(Output) ϕOUT provides a prescaled output clock for use with external I/O devices or memories. ϕOUT frequency is $f_{XTAL}/2$.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state TW and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7801.
30	X_2	(Output) Oscillator output.
31	X_1	(Input) Clock Input.
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

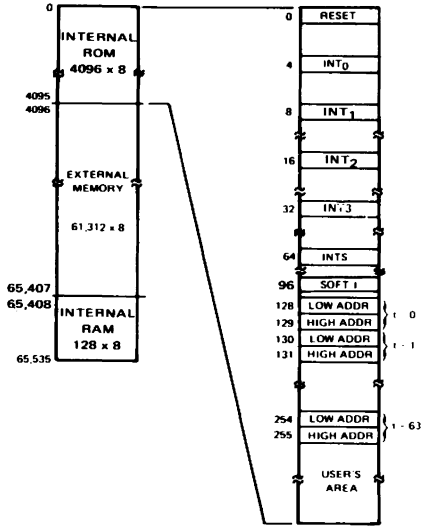
BLOCK DIAGRAM



Memory Map

FUNCTIONAL DESCRIPTION

The μPD7801 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-4096) and RAM (65.408-65.535), any memory location can be used as either ROM or RAM. The following memory map defines the 0-64K byte memory space for the μPD7801 showing that the Reset Start Address, Interrupt Start Address, Call Tables, etc., are located in the Internal ROM area.



HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 6K ROM

PRODUCT DESCRIPTION

The NEC μPD7802 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-Channel Silicon Gate MOS technology.

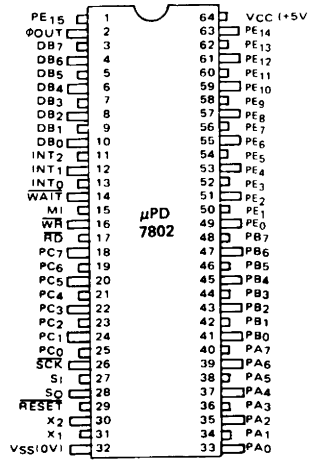
The NEC μPD7802 is intended to serve a broad spectrum of 8-bit designs ranging from enhanced single chip applications extending into the multi-chip microprocessor range. All the basic functional blocks – 6144 x 8 of ROM program memory, 64 x 8 of RAM data memory, 8-bit ALU, 48 I/O lines, Serial I/O port, 12-bit timer, and clock generator are provided on-chip to enhance standalone applications. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of the 8080A/8085A peripherals and memory products. Total memory space can be increased to 64K bytes.

The powerful 140 instruction set coupled with 6K bytes of ROM program memory and 64 bytes of RAM data memory greatly extends the range of single chip microcomputer applications. Five level vectored interrupt capability combined with a 2 microsecond cycle time enable the μPD7802 to compete with multi-chip microprocessor systems with the advantage that most of the support functions are on-chip.

FEATURES

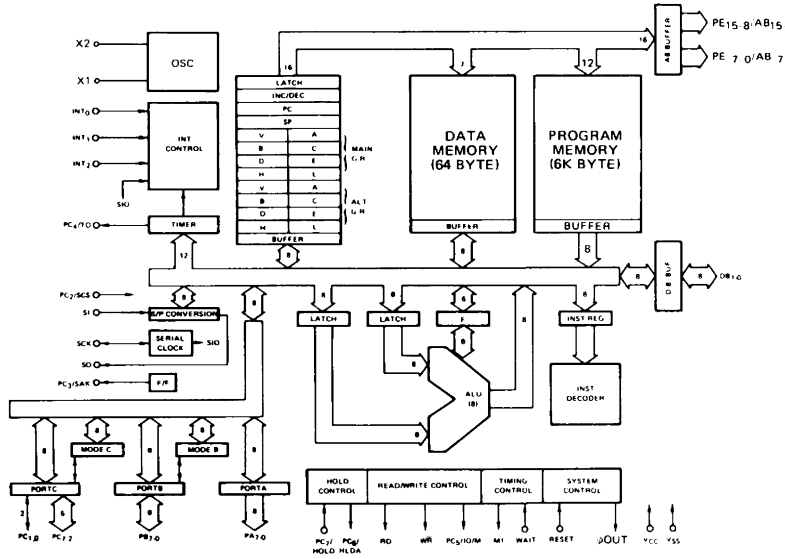
- NMOS Silicon Gate Technology Requiring +5V Supply
- Complete Single-Chip Microcomputer with On-Chip ROM, RAM and I/O
  - 6K Bytes ROM
  - 64Bytes RAM
  - 48 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 58K Bytes External Memory Address Range
- On-Chip Clock Generator
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instructions
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities (DMA)

PIN CONFIGURATION



PIN NO.	DESIGNATION	FUNCTION
1, 49-63	PE_0/AB_0-PE_{15}/AB_{15}	(Tri-State, Output) 16-bit address bus.
2	ϕOUT	(Output) ϕOUT provides a prescaled output clock for use with external I/O devices or memories. ϕOUT frequency is $f_{XTAL}/2$.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state T_W and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7802.
30	X_2	(Output) Oscillator output.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

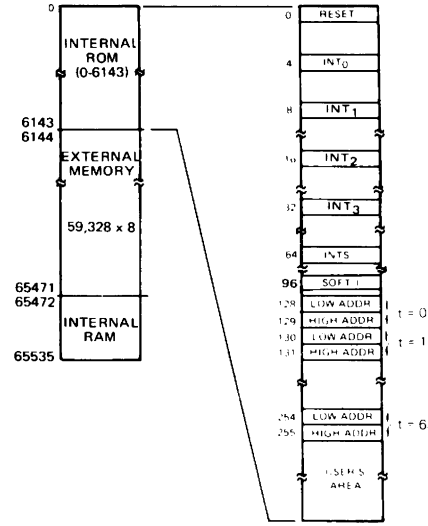
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Memory Map

The μPD7802 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-6143) and RAM(65.472-65.535), any memory location can be used as either ROM or RAM. The following memory map defines the 0-64K byte memory space for the μPD7802 showing that the Reset Start Address, Interrupt Start Address, Call Tables, etc., are located in the Internal ROM area.



FUNCTIONAL DESCRIPTION

I/O PORTS

PORT	FUNCTIONS
Port A	8-bit output port with latch
Port B	8-bit programmable Input/Output port w/latch
Port C	8-bit nibble I/O or Control port
Port E	16-bit Address/Output Port

Port A

Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using Arithmetic and Logic instructions. Data remains latched at Port A unless acted on by another Port A instruction or a RESET is issued.

Port B

Port B is an 8-bit I/O port. Data is latched at Port B in both the Input or Output modes. Each bit of Port B can be independently set to either Input or Output modes. The Mode B register programs the individual lines of Port B to be either an Input (Mode $B_n = 1$) or an Output (Mode $B_n = 0$).

Port C

Port C is an 8-bit I/O port. The Mode C register is used to program the upper 6 bits of Port C to provide control functions or to set the I/O structure per the following table.

	MODE $C_n = 0$	MODE $C_n = 1$
PC_0	Output	Input
PC_1	Output	Input
PC_2	$\overline{SCS}$ Input	Input
PC_3	SAK Output	Output
PC_4	To Output	Output
PC_5	IO/$\overline{M}$ Output	Output
PC_6	HLDA Output	Output
PC_7	HOLD Input	Input

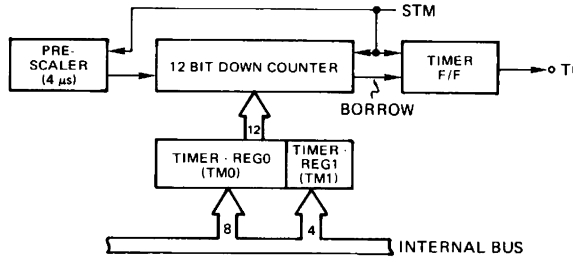
Port E

Port E is a 16-bit address bus/output port. It can be set to one of three operating modes using the PER, PEN, or PEX instructions.

- 16-Bit Address Bus – the PER instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).
- 4-Bit Output Port/12 Bit Address Bus – the PEN instruction sets this mode which allows for memory expansion of an additional 4K bytes, externally, plus the transfer of 4-bit nibbles.
- 16-Bit Output Port – the PEX instructions sets Port E to a 16-bit output port. The contents of B and C registers appear on PE_{8-15} and PE_{0-7}, respectively.

FUNCTIONAL DESCRIPTION (CONT.)

TIMER OPERATION



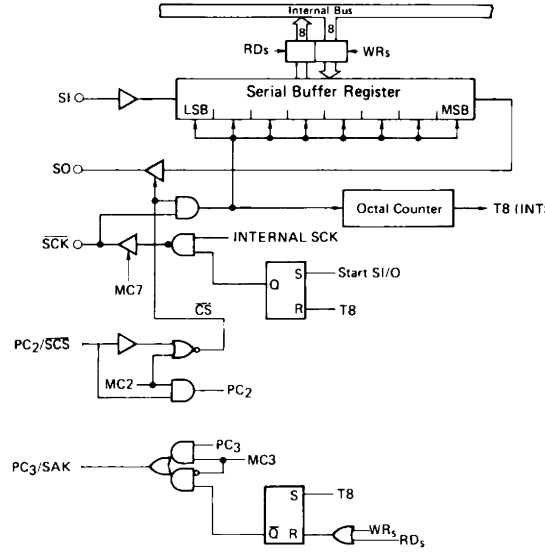
TIMER BLOCK DIAGRAM

A programmable 12-bit timer is provided on-chip for measuring time intervals, generating pulses, and general time-related control functions. It is capable of measuring time intervals from 4 μs to 16 ms in duration. The timer consists of a prescaler which decrements a 12-bit counter at a fixed 4 μs rate. Count pulses are loaded into the 12-bit down counter through timer register (TM0 and TM1). Count-down operation is initiated upon extension of the STM instruction when the contents of the down counter are fully decremented and a borrow operation occurs, an interval interrupt (INTT) is generated. At the same time, the contents of TM0 and TM1 are reloaded into the down-counter and countdown operation is resumed. Count operation may be restarted or initialized with the STM instruction. The duration of the timeout may be altered by loading new contents into the down counter.

The timer flip flop is set by the STM instruction and reset on a countdown operation. Its output (TO) is available externally and may be used in a single pulse mode or general external synchronization.

Timer interrupt (INTT) may be disabled through the interrupt.

SERIAL PORT OPERATION



SERIAL PORT BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION (CONT.)

The on-chip serial port provides basic synchronous serial communication functions allowing the NEC μPD7801/02 to serially interface with external devises.

Serial Transfers are synchronized with either the internal clock or an external clock input ($\overline{SCK}$). The transfer rate is fixed at 1 Mbit/second if the internal clock is used or is variable between DC and 1 Mbit/second when an external clock is used. The Clock Source Select is determined by the Mode C register. The serial clock (internal or external $\overline{SCK}$) is enabled when the Serial Chip Select Signal ($\overline{SCS}$) goes low. At this time receive and transmit operations through the Serial Input port (SI)/Serial Output port (SO) are enabled. Receive and transmit operations are performed MSB first.

Serial Acknowledge (SAK) goes high when data transfers between the accumulator and Serial Register is completed. SAK goes low when the buffer becomes full after the completion of serial data receive or transmit operations. While SAK is low, no further data can be received.

INTERRUPT STRUCTURE

The μPD7801/02 provides a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from six different sources; three external interrupts, two internal interrupts, and a non-maskable software interrupt. Each interrupt when activated branches to a designated memory vector location for that interrupt.

INT	VECTORED MEMORY LOCATION	PRIORITY	TYPE
INTT	8	3	Internal, Timer Overflow
INTS	64	6	Internal, Serial Buffer Full/Empty
INT0	4	2	Ext., level sensitive
INT1	16	4	Ext., Rising edge sensitive
INT2	32	5	Ext., Rising/Falling edge sensitive
SOFTI	96	1	Software Interrupt

$\overline{RESET}$ (Reset)

An active low-signal on this input for more than 4 μs forces the μPD7801/02 into a Reset condition. $\overline{RESET}$ affects the following internal functions:

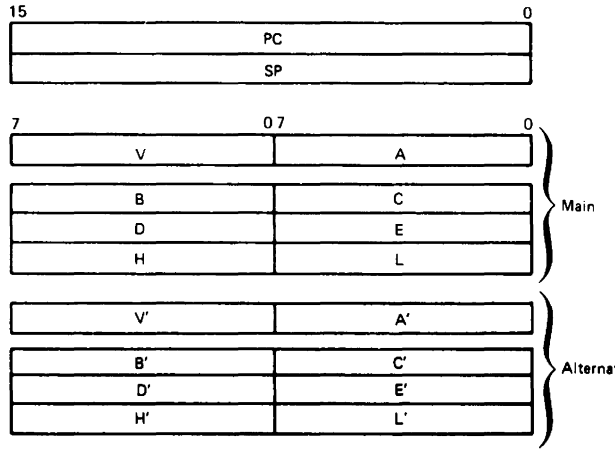
- The Interrupt Enable Flags are reset, and Interrupts are inhibited.
- The Interrupt Request Flag ist reset.
- The HALT flip flop is reset, and the Halt-state is released.
- The contents of the MODE B register are set to FF_H, and Port B becomes an input port.
- The contents of the MODE C register are set to FF_H. Port C becomes an I/O port and output lines go low.
- All Flags are reset to 0.
- The internal COUNT register for timer operation is set to FFF_H and the timer F/F is reset.
- The ACK F/F is set.
- The HLDA F/F is reset.
- The contents of the Program Counter are set to 0000_H.
- The Address Bus ($PE_{0\text{-}15}$), Data Bus ($DB_{0\text{-}7}$), $\overline{RD}$, and $\overline{WR}$ go to a high impedance state.

Once the $\overline{RESET}$ input goes high, the program is started at location 0000_H.

FUNCTIONAL DESCRIPTION (CONT.)

REGISTERS

The μPD7801/02 contains sixteen 8-bit registers and two 16-bit registers.



General Purpose Registers (B, C, D, E, H. L)

There are two sets of general purpose registers (Main: B, C, D, E, H, L: Alternate: B', C', D', E' H', L'). They can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL, B'C', D'E', H'L'). Auto Increment and Decrement adressing mode capabilities extend the uses for the DE, HL, D'E', and H'L' register-pairs. The contents of the BC, DE, and HL register-pairs can be exchanged with their Alternate Register counterparts using the EXX instruction.

Vector Register (V)

When defining a scratch pad area in the memory space, the upper 8-bit memory address is defined in the V-register and the lower 8-bits is defined by the immediate data of an instruction. Also the scratch pad indicated by the V-Register can be used as 256 x 8-bit working registers for storing software flags, parameters and counters immediately or directly.

Accumulator (A)

All data important data treatments on μPD7801/02 are done through the accumulator. The contents of the Accumulator and Vector Register can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents comes from another register or an instruction's immediate data. A reset sets the PC to 0000_H.

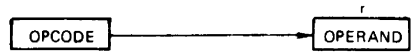
Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

ADDRESS MODES

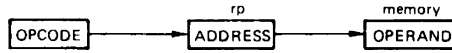
Register Addressing
Register Indirect Addressing
Auto-Increment Addressing
Auto-Decrement Addressing
Working Register Addressing
Direct Addressing
Immediate Addressing
Immediate Extended Addressing
Accumulator Indirect Adressing

Register Addressing



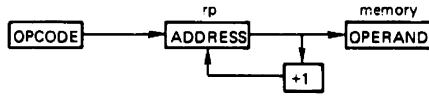
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



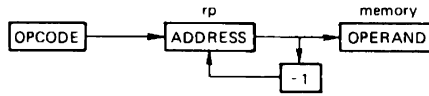
The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

Auto-Increment Addressing

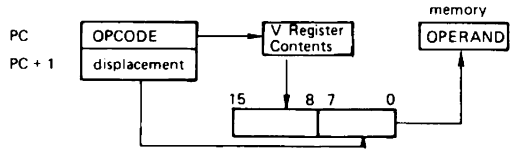


The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

Auto Decrement Addressing



Working Register Addressing

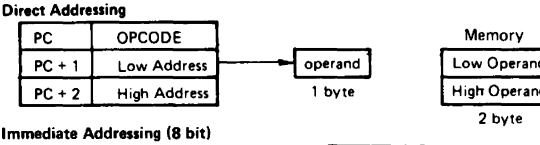


The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. The memory contents can be influenced directly or immediately. Mnemonics with a W suffix ending this address mode.

ADDRESS MODES (CONT.)

The two bytes following the opcode specify an address of a location containing the operand.

Direct Addressing



Immediate Addressing (8 bit)

Immediate Extended Addressing (16 bit)

Accumulator Indirect Adressing (Select Table)

C ← (PC + 2 + A)

B ← (PC + 2 + A + 1)

Operand Description

INSTRUCTION SET

OPERAND	DESCRIPTION
r	V, A, B, C, D, E, H, L
r1	B, C, D, E, H, L
r2	A, B, C
sr	PA PB PC MK MB MC TM0 TM1 S
sr1	PA PB PC MK S
sr2	PA PB PC MK
rp	SP, B, D, H
rp1	V, B, D, H
rpa	B, D, H, D+, H+, D−, H−
rpa1	B, D, H
wa	8 bit immediate data
word	16 bit immediate data
byte	8 bit immediate data
bit	3 bit immediate data
f	F0, F1, F2, FT, FS,

Notes:

1. When special register operands sr, sr1, sr2 are used; PA = Port A, PB = Port B, PC = Port C, MK = Mask Register, MB = Mode B Register, MC = Mode C Register, TM0 = Timer Register 0, TM1 = Timer Register 1, S = Serial Register.
2. When register pair operands rp, rp1 are used; SP = Stack Pointer, B = BC, D = DE, H = HL, V = VA.
3. Operands rpa, rpa1, wa are used in indirect addressing and auto-increment/auto-decrement addressing modes.
   B = (BC), D = (DE), H = (HL)
   D+ = (DE)+, H+ = (HL)+, D− = (DE)−, H− = (HL)−.
4. When the interrupt operand f is used; F0 = INTF0, F1 = INTF1, F2 = INTF2, FT = INTFT, FS = INTFS.

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
8-BIT DATA TRANSFER							
MOV	r1, A	1	4	r1 ← A			
MOV	A, r1	1	4	A ← r1			
MOV	sr, A	2	10	sr ← A			
MOV	A, sr1	2	10	A ← sr1			
MOV	r, word	4	17	r ← (word)			
MOV	word, r	4	17	(word) ← r			
MVI	r, byte	2	7	r ← byte			
MVIW	wa, byte	3	13	(V, wa) ← byte			
MVIX	rpa1, byte	2	10	(rpa1) ← byte			
STAW	wa	2	10	(V, wa) ← A			
LDAW	wa	2	10	A ← (V, wa)			
STAX	rpa	1	7	(rpa) ← A			
LDAX	rpa	1	7	A ← (rpa)			
EXX		1	4	Exchange register sets			
EX		1	4	V, A ↔ V', A'			
BLOCK		1	13 (C+1)	(DE) ← (HL), C ← C − 1 DE ← DE + 1 HL ← HL + 1			
16-BIT DATA TRANSFER							
SBCD	word	4	20	(word) ← C, (word + 1) ← B			
SDED	word	4	20	(word) ← E, (word + 1) ← D			
SHLD	word	4	20	(word) ← L, (word + 1) ← H			
SSPD	word	4	20	(word) ← SP_L, (word + 1) ← SP_H			
LBCD	word	4	20	C ← (word), B ← (word + 1)			
LDED	word	4	20	E ← (word), D ← (word + 1)			
LHLD	word	4	20	L ← (word), H ← (word + 1)			
LSPD	word	4	20	SP_L ← (word), SP_H ← (word + 1)			
PUSH	rp1	2	17	(SP − 1) ← $rp1_H$, (SP − 2) ← $rp1_L$			
POP	rp1	2	15	$rp1_L$ ← (SP) $rp1_H$ ← (SP + 1), SP ← SP + 2			
LXI	rp, word	3	10	rp ← word			
TABLE		1	19	C ← (PC + 2 + A) B ← (PC + 2 + A + 1)			

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
ARITHMETIC							
ADD	A, r	2	8	A ← A + r		↕	↕
ADD	r, A	2	8	r ← r + A		↕	↕
ADDX	rpa	2	11	A ← A + (rpa)		↕	↕
ADC	A, r	2	8	A ← A + r + CY		↕	↕
ADC	r, A	2	8	r ← r + A + CY		↕	↕
ADCX	rpa	2	11	A ← A + (rpa) + CY		↕	↕
SUB	A, r	2	8	A ← A - r		↕	↕
SUB	r, A	2	8	r ← r - A		↕	↕
SUBX	rpa	2	11	A ← A - (rpa)		↕	↕
SBB	A, r	2	8	A ← A - r - CY		↕	↕
SBB	r, A	2	8	r ← r - A - CY		↕	↕
SBBX	rpa	2	11	A ← A - (rpa) - CY		↕	↕
ADDNC	A, r	2	8	A ← A + r	No Carry	↕	↕
ADDNC	r, A	2	8	r ← r + A	No Carry	↕	↕
ADDNCX	rpa	2	11	A ← A + (rpa)	No Carry	↕	↕
SUBNB	A, r	2	8	A ← A - r	No Borrow	↕	↕
SUBNB	r, A	2	8	r ← r - A	No Borrow	↕	↕
SUBNBX	rpa	2	11	A ← A - (rpa)	No Borrow	↕	↕
LOGICAL							
ANA	A, r	2	8	A ← A ∧ r			↕
ANA	r, A	2	8	r ← r ∧ A			↕
ANAX	rpa	2	11	A ← A ∧ (rpa)			↕
ORA	A, r	2	8	A ← A ∨ r			↕
ORA	r, A	2	8	r ← r ∨ A			↕
ORAX	rpa	2	11	A ← A ∨ (rpa)			↕
XRA	A, r	2	8	A ← A ∨ r			↕
XRA	r, A	2	8	A ← r ∨ A			↕
XRAX	rpa	2	11	A ← A ∨ (rpa)			↕
GTA	A, r	2	8	A - r - 1	No Borrow	↕	↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
LOGICAL (CONT.)							
GTAX	rpa	2	11	A (rpa) - 1	No Borrow	↕	↕
LTA	A, r	2	8	A - r	Borrow	↕	↕
LTA	r, A	2	8	r - A	Borrow	↕	↕
LTAX	rpa	2	11	A - (rpa)	Borrow	↕	↕
ONA	A, r	2	8	A∧r	No Zero		↕
ONAX	rpa	2	11	A∧(rpa)	No Zero		↕
OFFA	A, r	2	8	A∧r	Zero		↕
OFFAX	rpa	2	11	A∧(rpa)	Zero		↕
NEA	A, r	2	8	A - r	No Zero	↕	↕
NEA	r, A	2	8	r - A	No Zero	↕	↕
NEAX	rpa	2	11	A - (rpa)	No Zero	↕	↕
EQA	A, r	2	8	A - r	Zero	↕	↕
EQA	r, A	2	8	r - A	Zero	↕	↕
EQAX	rpa	2	11	A - (rpa)	Zero	↕	↕
IMMEDIATE DATA TRANSFER (ACCUMULATOR)							
XRI	A, byte	2	7	A ← A∨byte			↕
ADINC	A, byte	2	7	A ← A + byte	No Carry	↕	↕
SUINB	A, byte	2	7	A ← A - byte	No Borrow	↕	↕
ADI	A, byte	2	7	A ← A + byte		↕	↕
ACI	A, byte	2	7	A ← A + byte + CY		↕	↕
SUI	A, byte	2	7	A ← A - byte		↕	↕
SBI	A, byte	2	7	A ← A - byte - CY		↕	↕
ANI	A, byte	2	7	A ← A∧byte			↕
ORI	A, byte	2	7	A ← A∨byte			↕
GTI	A, byte	2	7	A - byte - 1	No Borrow	↕	↕
LTI	A, byte	2	7	A - byte	Borrow	↕	↕
ONI	A, byte	2	7	A∧byte	No Zero		↕
OFFI	A, byte	2	7	A∧byte	Zero		↕
NEI	A, byte	2	7	A - byte	No Zero	↕	↕
EQI	A, byte	2	7	A - byte	Zero	↕	↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER							
XRI	r, byte	3	11	r ← r ∨ byte			↕
ADINC	r, byte	3	11	r ← r + byte	No Carry	↕	↕
SUINB	r, byte	3	11	r ← r − byte	No Borrow	↕	↕
ADI	r, byte	3	11	r ← r + byte		↕	↕
ACI	r, byte	3	11	r ← r + byte + CY		↕	↕
SUI	r, byte	3	11	r ← r − byte		↕	↕
SBI	r, byte	3	11	r ← r − byte − CY		↕	↕
ANI	r, byte	3	11	r ← r ∧ byte		↕	↕
ORI	r, byte	3	11	r ← r ∨ byte			↕
GTI	r, byte	3	11	r − byte − 1	No Borrow	↕	↕
LTI	r, byte	3	11	r − byte	Borrow	↕	↕
ONI	r, byte	3	11	r ∧ byte	No Zero		↕
OFFI	r, byte	3	11	r ∧ byte	Zero		↕
NEI	r, byte	3	11	r ≠ byte	No Zero	↕	↕
EQI	r, byte	3	11	r − byte	Zero	↕	↕
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER)							
XRI	sr2, byte	3	17	sr2 ← sr2 ∨ byte			↕
ADINC	sr2, byte	3	17	sr2 ← sr2 + byte	No Carry	↕	↕
SUINB	sr2, byte	3	17	sr2 ← sr2 − byte	No Borrow	↕	↕
ADI	sr2, byte	3	17	sr2 ← sr2 + byte		↕	↕
ACI	sr2, byte	3	17	sr2 ← sr2 + byte + CY		↕	↕
SUI	sr2, byte	3	17	sr2 ← sr2 − byte		↕	↕
SBI	sr2, byte	3	17	sr2 ← sr2 − byte − CY		↕	↕
ANI	sr2, byte	3	17	sr2 ← sr2 ∧ byte			↕
ORI	sr2, byte	3	17	sr2 ← sr2 ∨ byte			↕
GTI	sr2, byte	3	14	sr2 − byte − 1	No Borrow	↕	↕
LTI	sr2, byte	3	14	sr2 − byte	Borrow	↕	↕
ONI	sr2, byte	3	14	sr2 ∧ byte	No Zero		↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER) (CONT.)							
OFFI	sr2, byte	3	14	sr2 ∧ byte	Zero		↕
NEI	sr2, byte	3	14	sr2 - byte	No Zero	↕	↕
EQI	sr2, byte	3	14	sr2 - byte	Zero	↕	↕
WORKING REGISTER							
XRAW	wa	3	14	A ← A ∀ (V, wa)			↕
ADDNCW	wa	3	14	A ← A + (V, wa)	No Carry	↕	↕
SUBNBW	wa	3	14	A ← A - (V, wa)	No Borrow	↕	↕
ADDW	wa	3	14	A ← A + (V, wa)		↕	↕
ADCW	wa	3	14	A ← A + (V, wa) + CY		↕	↕
SUBW	wa	3	14	A ← A - (V, wa)		↕	↕
SBBW	wa	3	14	A ← A - (V, wa) - CW		↕	↕
ANAW	wa	3	14	A ← A ∧ (V, wa)			↕
ORAW	wa	3	14	A ← A ∨ (V, wa)			↕
GTAW	wa	3	14	A ← (V, wa) - 1	No Borrow	↕	↕
LTAW	wa	3	14	A - (V, wa)	Borrow	↕	↕
ONAW	wa	3	14	A ∧ (V, wa)	No Zero		↕
OFFAW	wa	3	14	A ∧ (V, wa)	Zero		↕
NEAW	wa	3	14	A - (V, wa)	No Zero	↕	↕
EQAW	wa	3	14	A - (V, wa)	Zero	↕	↕
ANIW	wa, byte	3	16	(V, wa) ← (V, wa) ∧ byte			↕
ORIW	wa, byte	3	16	(V, wa) ← (V, wa) ∨ byte			↕
GTIW	wa, byte	3	13	(V, wa) - byte - 1	No Borrow	↕	↕
LTIW	wa, byte	3	13	(V, wa) - byte	Borrow	↕	↕
ONIW	wa, byte	3	13	(V, wa) ∧ byte	No Zero		↕
OFFIW	wa, byte	3	13	(V, wa) ∧ byte	Zero		↕
NEIW	wa, byte	3	13	(V, wa) - byte	No Zero	↕	↕
EQIW	wa, byte	3	13	(V, wa) - byte	Zero	↕	↕
INCREMENT/DECREMENT							
INR	r2	1	4	r2 ← r2 + 1	Carry		↕
INRW	wa	2	13	(V, wa) ← (V, wa) + 1	Carry		↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
INCREMENT/DECREMENT (CONT.)							
DCR	r2	1	4	r2 ← r2 - 1	Borrow		↕
DCRW	wa	2	13	(V, wa) ← (V, wa) - 1	Borrow		↕
INX	rp	1	7	rp ← rp + 1			
DCX	rp	1	7	rp ← rp - 1			
DAA		1	4	Decimal Adjust Accumulator		↕	↕
STC		2	8	CY ← 1		1	
CLC		2	8	CY ← 0		0	
ROTATE AND SHIFT							
RLD		2	17	Rotate Left Digit			
RRD		2	17	Rotate Right Digit			
RAL		2	8	Am + 1 ← Am, A_0 ← CY, CY ← A_7		↕	
RCL		2	8	Cm + 1 ← Cm, C_0 ← CY, CY ← C_7		↕	
RAR		2	8	Am - 1 ← Am, A_7 ← CY, CY ← A_0		↕	
RCR		2	8	Cm - 1 ← Cm, C_7 ← CY, CY ← C_0		↕	
SHAL		2	8	Am + 1 ← Am, A_0 ← 0, CY ← A_7		↕	
SHCL		2	8	Cm + 1 ← CM, C_0 ← 0, CY ← C_7		↕	
SHAR		2	8	Am - 1 ← Am, A_7 ← 0, CY ← A_0		↕	
SHCR		2	8	Cm - 1 ← Cm, C_7 ← 0, CY ← C_0		↕	
JUMP							
JMP	word	3	10	PC ← word			
JB		1	4	PC_H ← B, PC_L ← C			
JR	word	1	13	PC ← PC + 1 + jdisp1			
JRE	word	2	13	PC ← PC + 2 + jdisp			
CALL							
CALL	word	3	16	(SP - 1) ← (PC - 3)$_H$, (SP - 2) ← (PC - 3)$_L$, PC ← word			
CALB		1	13	(SP - 1) ← (PC - 1)$_H$, (SP - 2) ← (PC - 1)$_L$, PC_H ← B, PC_L ← C			
CALF	word	2	16	(SP-1)← (PC-2)$_H$, (SP-2)← (PC-2)$_L$ PC15 ~ 11 ← 00001, PC10 ~ 0 ← fa			
CALT	word	1	19	(SP-1)←(PC-1)$_H$,(SP-2)← (PC-1)$_L$ PC_L←(128-2ta), PC_H← (129+2ta)			
SOFTI		1	19	(SP - 1) ← PSW, SP - 2, (SP - 3) ← PC PC ← 0060_H, SIRQ ← 1			

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
RETURN							
RET		1	11	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$ $SP \leftarrow SP+2$			
RETS		1	11+a	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$, $SP \leftarrow SP+2, PC \leftarrow PC+n$			
RETI		1	15	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$ $PSW \leftarrow (SP+2), SP \leftarrow SP+3, SIRQ \leftarrow 0$			
SKIP							
BIT	bit, wa	2	10	Bit test	$(V, wa)_{bit} = 1$		
SKC		2	8	Skip if Carry	CY = 1		
SKNC		2	8	Skip if No Carry	CY = 0		
SKZ		2	8	Skip if Zero	Z = 1		
SKNZ		2	8	Skip if No Zero	Z = 0		
SKIT	f	2	8	Skip if INT X = 1, then reset INT X	f = 1		
SKNIT	f	2	8	Skip if No INT X otherwise reset INT X	f = 0		
CPU CONTROL							
NOP		1	4	No Operation			
EI		2	8	Enable Interrupt			
DI		2	8	Disable Interrupt			
HLT		1	6	Halt			
SERIAL PORT CONTROL							
SIO		1	4	Start (Trigger) Serial I/O			
STM		1	4	Start Timer			
INPUT/OUTPUT							
IN	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow$ byte $A \leftarrow DB_{7-0}$			
OUT	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow$ byte $DB_{7-0} \leftarrow A$			
PEX		2	11	$PE_{15-8} \leftarrow B, PE_{7-0} \leftarrow C$			
PEN		2	11	$PE_{15-12} \leftarrow B_{7-4}$			
PER		2	11	Port E AB Mode			

Program Status Word (PSW) Operation

OPERATION						D6	D5	D4	D3	D2	D0
REG, MEMORY			IMMEDIATE		SKIP	Z	SK	HC	L1	L0	CY
ADD ADC SUB SBB	ADDW ADCW SUBW SBBW	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			↕	0	↕	0	0	↕
ANA ORA XRA	ANAW ORAW XRAW	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		↕	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCW SUBNBW GTAW LTAW	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	 GTIW LTIW		↕	↕	↕	0	0	↕
ONA OFFA	ONAW OFFAW	ONAX OFFAX	ONI OFFI	ONIW OFFIW		↕	↕	•	0	0	•
NEA EQA	NEAW EQAW	NEAX EQAX	NEI EQI	NEIW EQIW		↕	↕	↕	0	0	↕
INR DCR	INRW DCRW					↕	↕	↕	0	0	•
DAA						↕	0	↕	0	0	↕
RAL, RAR, RCL, RCR SHAL, SHAR, SHCL, SHCR						•	0	•	0	0	↕
RLD, RRD						•	0	•	0	0	•
STC						•	0	•	0	0	1
CLC						•	0	•	0	0	0
			MVI A, byte			•	0	•	1	0	•
			MVI L, byte LXI H, word			•	0	•	0	1	•
					BIT SKC SKNC SKZ SKNZ SKIT SKNIT	•	↕	•	0	0	•
					RETS	•	1	•	0	0	•
All other instructions						•	0	•	0	0	•

↕ Flag affected according to result of operation
1 Flag set
0 Flag reset
• Flag not affected

ELECTRICAL SPECIFICATIONS AND PACKAGE OUTLINES FOR

μPD7800/μPD7801/μPD7802

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... −10°C to +70°C
Storage Temperature ..... −65°C to +125°C
Voltage On Any Pin ..... −0.3V to +7.0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10 ~ +70°C, V_{CC} = +5.0V ± 10 %

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	200	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

CLOCK TIMING

T_a = −10 to +70°C, V_{CC} = +5.0V ± 10 %, $f_{osz\ max}$ = 2 MHz, not devided internally

AC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X_{OUT} Cycle Time	t_{CYX}	454	2000	ns	t_{CYX}
X_{OUT} Low Level Width	t_{XXL}	212		ns	t_{XXL}
X_{OUT} High Level Width	t_{XXH}	212		ns	t_{XXH}

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → X_{OUT} L.E.	t_{RX}	20		ns	t_{CYX} = 500 ns
Address (PE_{0-15}) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	200(T3); 700(T4)		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address (PE_{0-15}) → WAIT L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from X_{OUT} L.E.)	t_{WTS}	180		ns	
$\overline{WAIT}$ Hold Time (Referenced from X_{OUT} L.E.)	t_{WTH}	0		ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
X_{OUT} L.E. → WR L.E.	t_{XW}		270	ns	
Address (PE_{0-15}) → X_{OUT} T.E.	t_{AX}		300	ns	
Address (PE_{0-15}) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address (PE_{0-15}) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

AC CHARACTERISTICS (CONT.)

SERIAL I/O OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		900	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

PEN, PEX, PER OPERATION

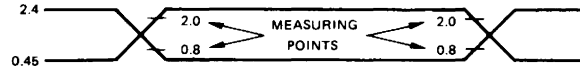
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
X_1 L.E. → $\overline{EXT}$	t_{XE}		250	ns	
Address (AB_{0-15}) → STB L.E.	t_{AST}	200			
Data (DB_{0-7}) → STB L.E.	t_{DST}	200			t_{CYX} = 500 ns
STB Hold Time	t_{STST}	300			
STB → Data	t_{STD}	400			

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from X_{OUT} L.E.)	t_{HDS_1}	100		ns	
	t_{HDS_2}	100		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	100		ns	
X_{OUT} L.E. → HLDA	t_{XHA}		100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

AC CHARACTERISTICS (CONT.)

t_{CYX} DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
t_{RX}	(1/25) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
t_{XW}	(27/50) T	MAX	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns
t_{AST}	(2/5) T	MIN	ns
t_{DST}	(2/5) T	MIN	ns
t_{STST}	(3/5) T	MIN	ns
t_{STD}	(4/5) T	MIN	ns

Notes: ① N = Number of Wait States

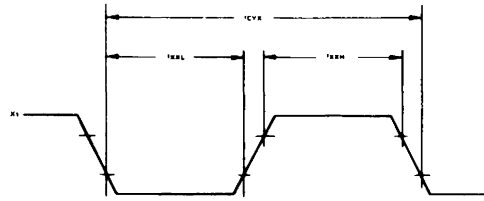
② T = t_{CYX}

③ Only above parameters are t_{CYX} dependent

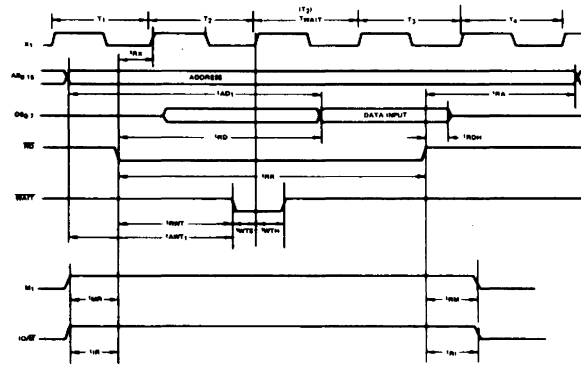
④ When a crystal frequency other than 4 MHz is used (t_{CYX} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

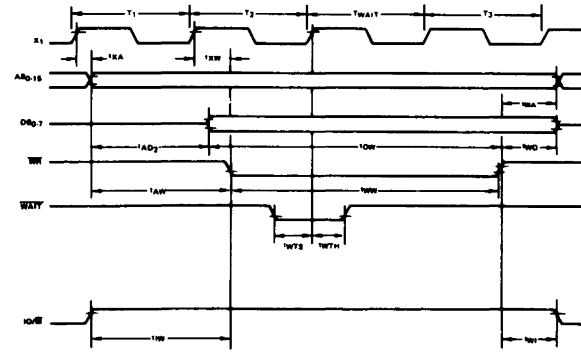
CLOCK TIMING



READ OPERATION

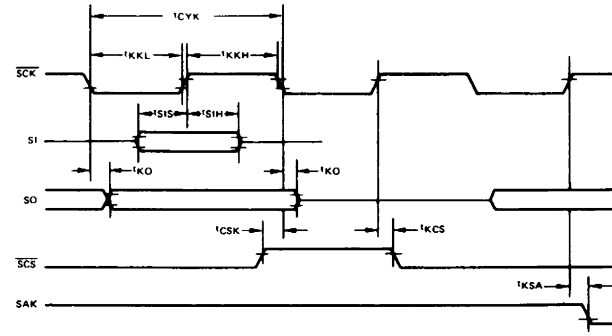


WRITE OPERATION

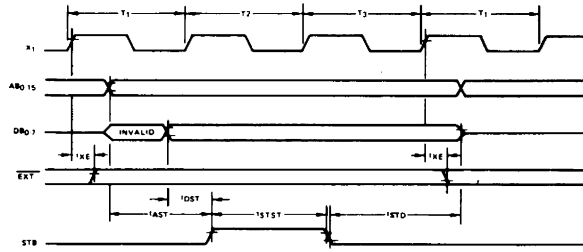


TIMING WAVEFORMS
(CONT.)

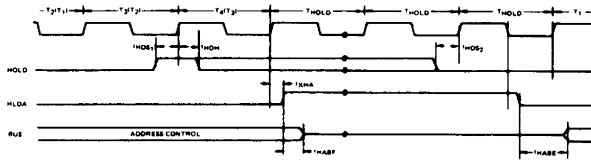
SERIAL I/O OPERATION



PEN, PEX, PER OPERATION



HOLD OPERATION



PACKAGE OUTLINES

Plastic Quil, μPD7800G

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C

Storage Temperature . . . . . −65°C to +125°C

Voltage On Any Pin . . . . . −0.3V to +7.0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10 to + 70°C, V_{CC} = +5.0V ± 10 %

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	200	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

CLOCK TIMING

−10 to +70°C, V_{CC} = +5.0V ± 10 %, $f_{osz\ max}$ = 4 MHz, internally devided (1:2)

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X1 Input Cycle Time	t_{CYX}	227	1000	ns	
X1 Input Low Level Width	t_{XXL}	106		ns	
X1 Input High Level Width	t_{XXH}	106		ns	
ϕ_{OUT} Cycle Time	$t_{CY\phi}$	454	2000	ns	
ϕ_{OUT} Low Level Width	$t_{\phi\phi L}$	150		ns	
ϕ_{OUT} High Level Width	$t_{\phi\phi H}$	150		ns	
ϕ_{OUT} Rise/Fall Time	$t_{r,tf}$		40	ns	

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → ϕ_{OUT} L.E.	$t_{R\phi}$	100		ns	
Address (PE_{0-15}) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	200(T3); 700(T4)		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address (PE_{0-15}) → $\overline{WAIT}$ L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from ϕ_{OUT} L.E.)	t_{WTS}	290		ns	
$\overline{WAIT}$ Hold Time (Referenced from ϕ_{OUT} L.E.)	t_{WTH}	0	120	ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	$t_{CY\phi}$ = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
ϕ_{OUT} L.E. → $\overline{WR}$ L.E.	$t_{\phi W}$	40	125	ns	
Address (PE_{0-15}) → ϕ_{OUT} T.E.	$t_{A\phi}$	100		ns	
Address (PE_{0-15}) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address (PE_{0-15}) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

SERIAL I/O OPERATION

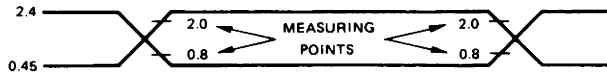
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		900	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	80		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from ϕ_{OUT} L.E.)	t_{HDS_1}	200		ns	$t_{CY\phi}$ = 500 ns
	t_{HDS_2}	200		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	0		ns	
ϕ_{OUT} L.E. → HLDA	$t_{\phi HA}$	−110	100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

AC CHARACTERISTICS (CONT.)

$t_{CY\phi}$ DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
$t_{R\phi}$	(1/5) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
$t_{\phi W}$	(1/4) T	MAX	ns
$t_{A\phi}$	(1/5) T	MIN	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns
t_{KKH} ($\overline{SCK}$ Output)	(1/2) (2T - 109)	MIN	ns
t_{KKL} ($\overline{SCK}$ Output)	(1/2) (2T - 109)	MIN	ns

Notes: ① N = Number of Wait States

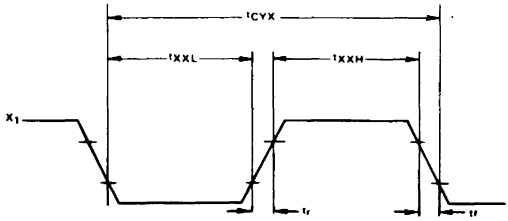
② T = $t_{CY\phi}$

③ Only above parameters are t_{CY_ϕ} dependent

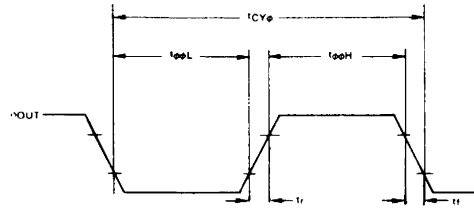
④ When a crystal frequency other than 4 MHz is used (t_{CY_ϕ} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

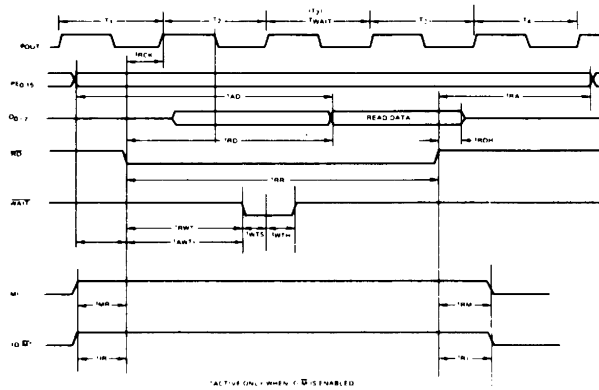
CLOCK TIMING



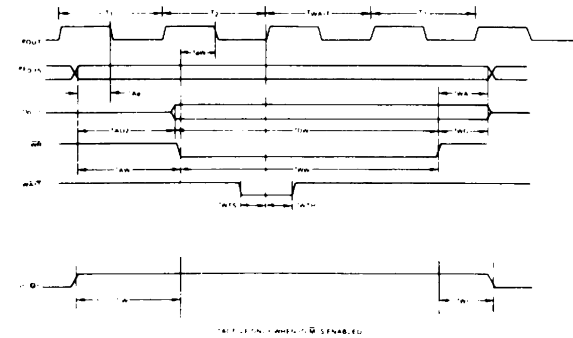
TIMING WAVEFORMS (CONT.)



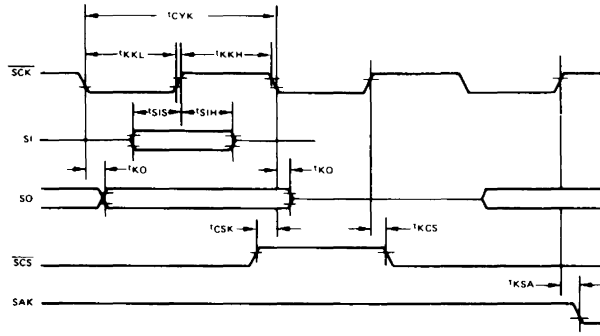
READ OPERATION



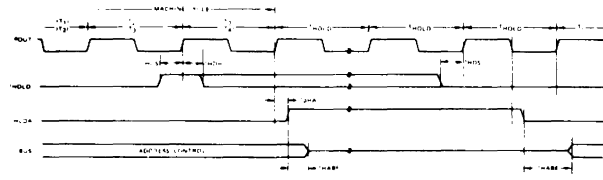
WRITE OPERATION



SERIAL I/O OPERATION



HOLD OPERATION



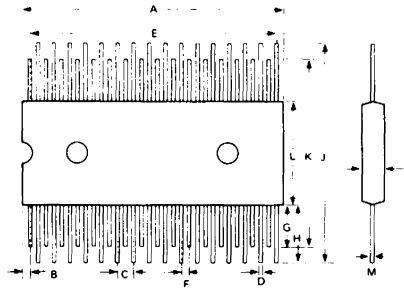
PACKAGE OUTLINES

Plastic Quil, μPD7801G/02G
Plastic Shrinkdip, μPD7801CW, μPD7802CW

64-PIN QUIL, STRAIGHT LEADS

PACKAGE OUTLINE

μPD7801G-xxx-37
μPD7802G-xxx-37

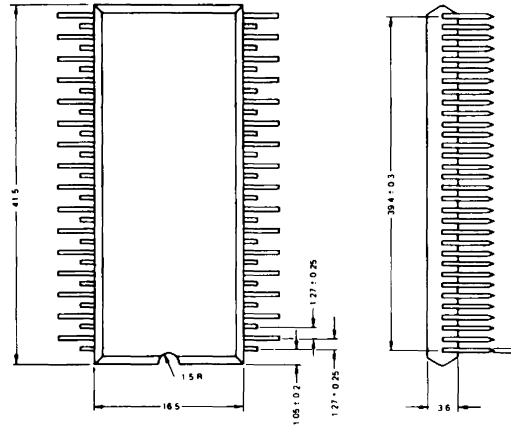


(Plastic)

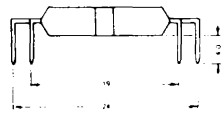
ITEM	MILLIMETERS	INCHES
A	41.8 MAX	1.65
B	1.22	0.05
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	38.37	1.56
F	1.27	0.05
G	6.75	0.27
H	8.3	0.37
I	3.6	0.14
J	36.1	1.38
K	30.0	1.18
L	16.5	0.65
M	0.25 ± 0.05	0.01 ± 0.002

64-PIN QUIL, BENT LEADS

μPD7800G-36
μPD7801G-xxx-36
μPD7802G-xxx-36



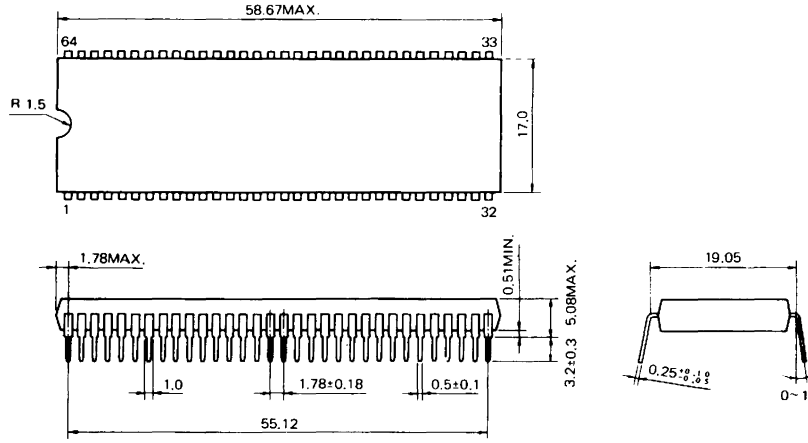
(Unit:mm)



PACKAGE OUTLINE

64-PIN SHRINK DIP

μPD7801CW-xxx
μPD7802CW-xxx



ELECTRICAL SPECIFICATIONS FOR EXTENDED TEMPERATURE RANGE OF -40 °C TO +85 °C

μPD7800/μPD7801/μPD7802

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... −40°C to +85°C
Storage Temperature ..... −65°C to +125°C
Voltage On Any Pin ..... −0.3V to +7.0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −40 ~ +85°C, V_{CC} = +5.0V ± 10 %

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.7	V	
Input High Voltage	V_{IH1}	2.3		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	220	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

AC CHARACTERISTICS

CLOCK TIMING

T_a = −10 to +70°C, V_{CC} = +5.0V ± 10 %

PARAMETER	SYMBOL	LIMITS MIN	MAX	UNITS	TEST CONDITIONS
X_{OUT} Cycle Time	t_{CYX}	666	2000	ns	t_{CYX}
X_{OUT} Low Level Width	t_{XXL}	256		ns	t_{XXL}
X_{OUT} High Level Width	t_{XXH}	256		ns	t_{XXH}

READ/WRITE OPERATION

AC CHARACTERISTICS (CONT.)

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → X_{OUT} L.E.	t_{RX}	20		ns	
Address (PE_{0-15}) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	200(T3); 700(T4)		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address (PE_{0-15}) → $\overline{WAIT}$ L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from X_{OUT} L.E.)	t_{WTS}	180		ns	
$\overline{WAIT}$ Hold Time (Referenced from X_{OUT} L.E.)	t_{WTH}	0		ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	t_{CYX} = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
X_{OUT} L.E. → $\overline{WR}$ L.E.	t_{XW}		270	ns	
Address (PE_{0-15}) → X_{OUT} T.E.	t_{AX}		300	ns	
Address (PE_{0-15}) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address (PE_{0-15}) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

AC CHARACTERISTICS (CONT.)

SERIAL I/O OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		700	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		300		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		300		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

PEN, PEX, PER OPERATION

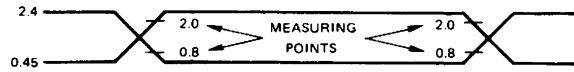
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
X_1 L.E. → $\overline{EXT}$	t_{XE}		250	ns	t_{CYX} = 500 ns
Address (AB_{0-15}) → STB L.E.	t_{AST}	200			
Data (DB_{0-7}) → STB L.E.	t_{DST}	200			
STB Hold Time	t_{STST}	300			
STB → Data	t_{STD}	400			

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from X_{OUT} L.E.)	t_{HDS_1}	100		ns	
	t_{HDS_2}	100		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	100		ns	
X_{OUT} L.E. → HLDA	t_{XHA}		100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

AC CHARACTERISTICS (CONT.)

t_{CYX} DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
t_{RX}	(1/25) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
t_{XW}	(27/50) T	MAX	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns
t_{AST}	(2/5) T	MIN	ns
t_{DST}	(2/5) T	MIN	ns
t_{STST}	(3/5) T	MIN	ns
t_{STD}	(4/5) T	MIN	ns

Notes: ① N = Number of Wait States

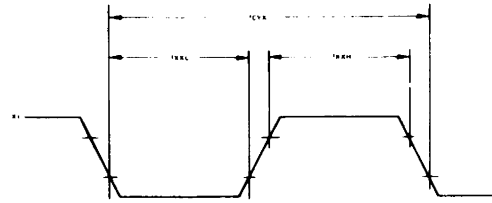
② T = t_{CYX}

③ Only above parameters are t_{CYX} dependent

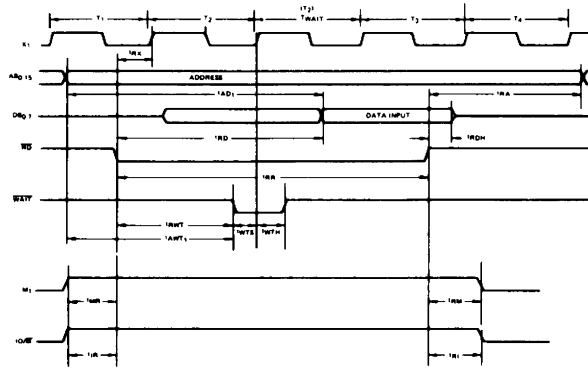
④ When a crystal frequency other than 4 MHz is used (t_{CYX} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

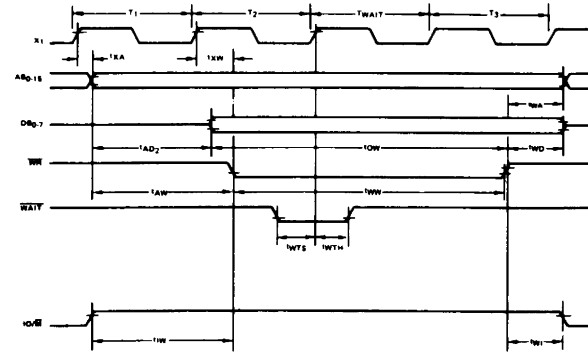
CLOCK TIMING



READ OPERATION



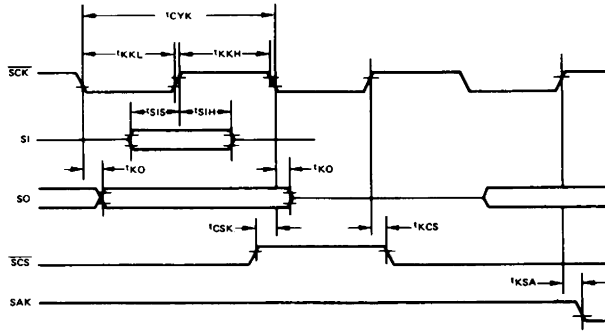
WRITE OPERATION



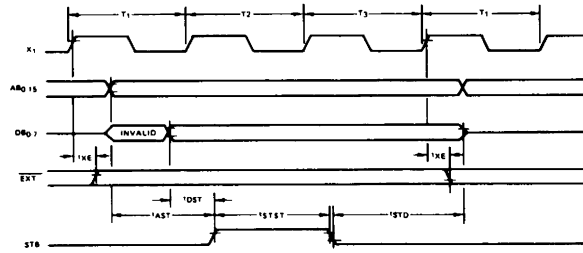
** $\overline{WAIT}$ should be supplied with VOH or VOL during t_{WTS} and t_{WTH}, otherwise malfunction may occur.

TIMING WAVEFORMS (CONT.)

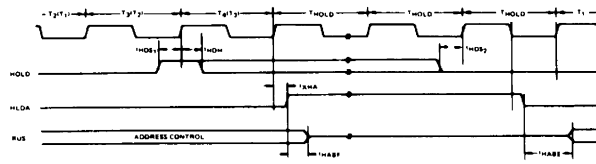
SERIAL I/O OPERATION



PEN, PEX, PER OPERATION



HOLD OPERATION



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... −40°C to +85°C

Storage Temperature ..... −65°C to +125°C

Voltage On Any Pin ..... −0.3V to +7.0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above thos indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

−10 to +70°C, V_{CC} = +5.0V ± 10 %

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.7	V	
Input High Voltage	V_{IH1}	2.3		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	220	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

CLOCK TIMING

AC CHARACTERISTICS

-10 to $+70°C$, $V_{CC} = +5.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X1 Input Cycle Time	t_{CYX}	333	1000	ns	
X1 Input Low Level Width	t_{XXL}	159		ns	
X1 Input High Level Width	t_{XXH}	159		ns	
Φ_{OUT} Cycle Time	$t_{CY\Phi}$	666	2000	ns	
Φ_{OUT} Low Level Width	$t_{\Phi\Phi L}$	256		ns	
Φ_{OUT} High Level Width	$t_{\Phi\Phi H}$	256		ns	
Φ_{OUT} Rise/Fall Time	$t_{r,tf}$		40	ns	

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → Φ_{OUT} L.E.	$t_{R\Phi}$	100		ns	
Address ($PE_{0\text{-}15}$) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	200(T3); 700(T4)		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address ($PE_{0\text{-}15}$) → $\overline{WAIT}$ L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from Φ_{OUT} L.E.)	t_{WTS}	290		ns	
$\overline{WAIT}$ Hold Time (Referenced from Φ_{OUT} L.E.)	t_{WTH}	0		ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	$t_{CY\Phi} = 500$ ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
Φ_{OUT} L.E. → $\overline{WR}$ L.E.	$t_{\Phi W}$	40	125	ns	
Address ($PE_{0\text{-}15}$) → Φ_{OUT} T.E.	$t_{A\Phi}$	100	300	ns	
Address ($PE_{0\text{-}15}$) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address ($PE_{0\text{-}15}$) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

SERIAL I/O OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		700	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		300		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		300		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from ϕ_{OUT} L.E.)	t_{HDS_1}	200		ns	$t_{CY\phi}$ = 500 ns
	t_{HDS_2}	200		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	0		ns	
ϕ_{OUT} L.E. → HLDA	t_{DHA}	110	100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)

② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

AC CHARACTERISTICS (CONT.)

$t_{CY\phi}$ DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
$t_{R\phi}$	(1/5) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
$t_{\phi W}$	(1/4) T	MAX	ns
$t_{A\phi}$	(1/5) T	MIN	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns

Notes: ① N = Number of Wait States

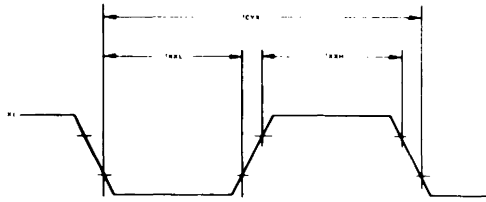
② $T = t_{CY\phi}$

③ Only above parameters are t_{CY_ϕ} dependent

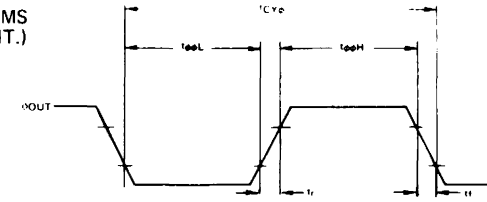
④ When a crystal frequency other than 4 MHz is used (t_{CY_ϕ} = 500 ns) the above equations can be used to calculate AC parameter values.

CLOCK TIMING

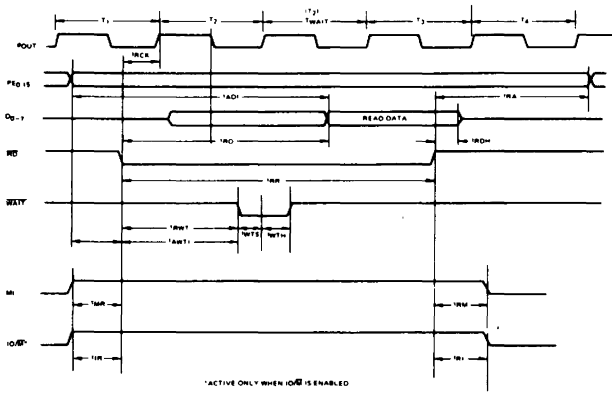
TIMING WAVEFORMS



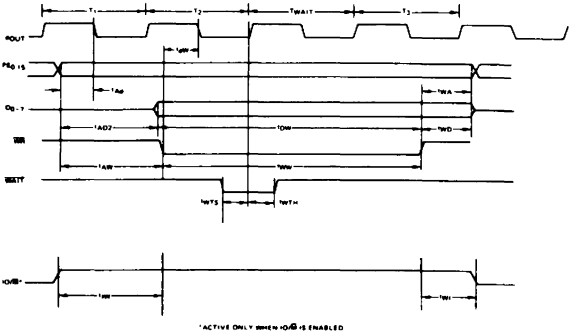
TIMING WAVEFORMS (CONT.)



READ OPERATION

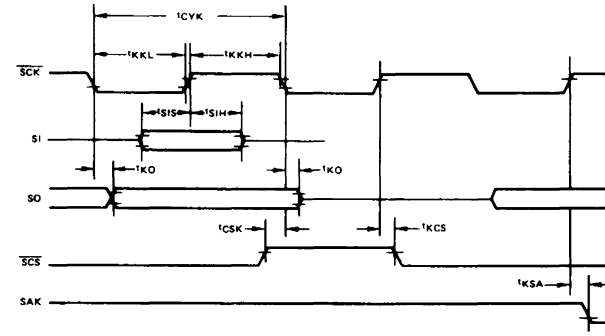


WRITE OPERATION

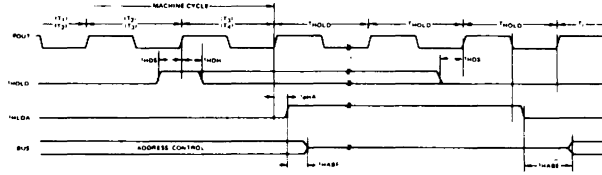


** $\overline{\text{WAIT}}$ should be supplied with VOH or VOL during t_{WTS} and t_{WTH}, otherfrise malfunctii may occur.

SERIAL I/O OPERATION



HOLD OPERATION



HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER ROM-LESS DEVELOPMENT DEVICE IN CMOS TECHNOLOGY

DESCRIPTION

The μPD78C05A is a high-performance 8-bit microcomputer fabricated with CMOS technology. The μPD78C05A contains an 8-bit ALU, a 128 x 8 RAM, two 8-bit I/O ports, a 6-bit I/O port, an 8-bit timer/event counter with 4-bit prescaler, a serial I/O port, and three (two external and one internal) source vectored interrupt structure. It also contains a 16-bit Address bus and an 8-bit data bus for external memory (program memory, data memory, or memory mapped I/O) up to 64K bytes.

The μPD78C05A has stand-by capability (STOP/HALT) for its power-down.

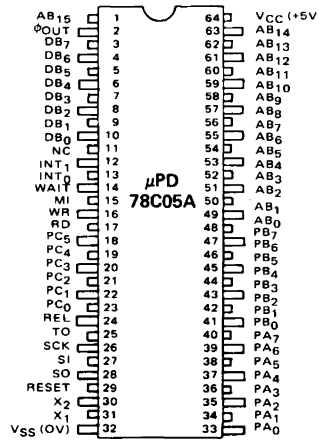
The μPD78C05A is applicable for hand-held computer, etc. requiring low power consumption.

The μPD78C05A is compatible with the μPD78C06A (μCOM-87LC-family) and used as evaluation chip for μCOM-87LC-series.

FEATURES

- Powerful 101 Instructions
- Instruction Cycle Time: 2,6 μs for 78C05A,
- Data Memory: 128W x 8
- Direct Addressing Capability up to 64kB External Memory
- Powerful Addressing Modes Capability
- Multi-level Stack
- Vectored Interrupts (External: 2, Internal: 1)
- On-chip 8-bit Timer with 4-bit Prescaler
- 46 I/O Ports
- Serial I/O Ports
- Stand-by Capability (STOP/HALT mode)
- Fully Bus Compatible with 8080A
- On-chip Clock Generator with 6 MHz crystal
- Single Supply, CMOS Technology
- Low Power Consumption
- 64 pin QUIL
- μPD78C06A Evaluation chip

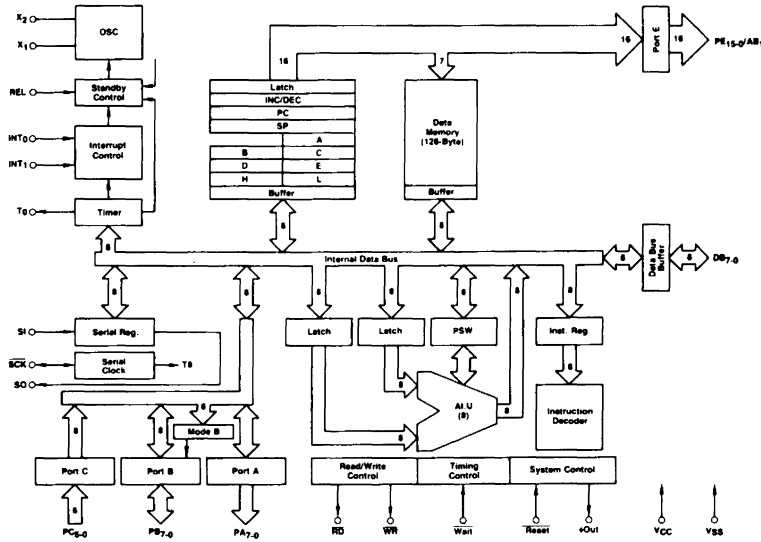
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
1, 49-63	AB_0-AB_{15}	(Output), 16 bit address bus and output port.
2	ϕOUT	(Output) The clock of system clock frequency (1/4 of crystal frequency or X_1 external clock frequency) is placed out from this line. It is still placed out in HALT mode, but it is fixed to high in STOP mode.
3-10	DB_7-DB_0	(Tri-State Input/Output) This is an 8-bit bi-directional data bus. The data move between an external memory or I/O STOP, and accumulator is done through this data bus. During an input, HALT, and RESET, the output of the data bus goes a high impedance state. Input/Output level are TTL compatible.
12	INT_0	(Input) It is a level-sensitive interrupt input line which is high level active.
13	INT_1	(Input) It is a rising-edge sensitive interrupt line, and it becomes valid when INT_1 input goes low to high. Subsequently, if users want to perform another interrupt on this line after an interrupt on this line is accepted, they must take it into consideration that INT_1 input should be maintained at low state a little while, and then it should go high. Unless, it does not enable another interrupt.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state T_W and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-23	PC_0-PC_5	(Input) This is a 6-bit input port with pull-up resistors. Input data to this port can be test by test instruction, and also moved to least significant 6-bit of accumulator. Input level is CMOS compatible. This port is fit for key-input port.
24	REL	(Input) This is an input to release the STOP mode of stand-by function. STOP mode is released by raising the REL input high, then clock generator which has been stopped will restart. During REL input is high, the bit 3 of Stand-by Control Register (SC3) is set to one, and it is reset to zero after REL signal returns low. Pull-down resistor is built in.
25	TO	(Output) The square wave is output from this line. Its cycle time is half of a count time of the internal timer. It goes on low level after reset.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD78C05A
30	X_2	(Output) Oscillator output.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

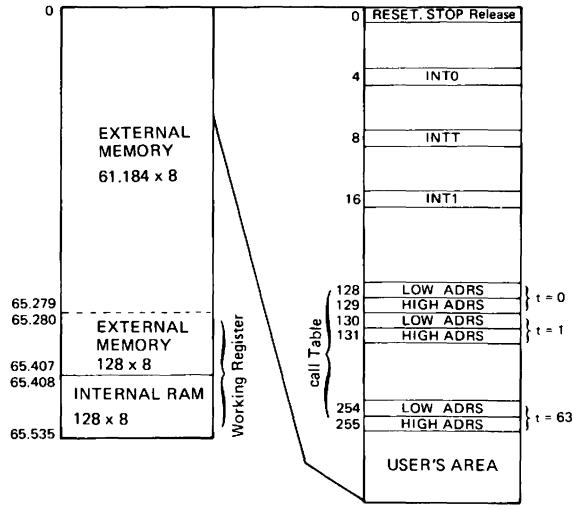
BLOCK DIAGRAM



Memory Map

The μPD78C05A can directly address the memory up to 64k bytes. Except on-chip RAM (65.408-65.535) any memory location can be used as either of RAM or ROM, freely. The memory map of the μPD78C05A is shown on the next page. In the specific memory area, the Reset/Stop mode Restart Address, Interrupt Start Address, Call Table etc. are involved. External memory (ROM), and/or working registers, freely.

FUNCTIONAL DESCRIPTION



HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 4K ROM IN CMOS TECHNOLOGY

DESCRIPTION

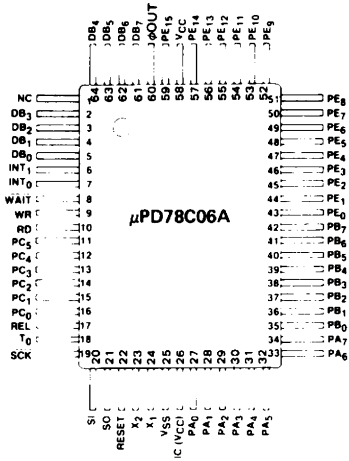
The NEC μPD78C06A is a general purpose single-chip microcomputer. The μPD78C06A is fabricated with CMOS technology.

This contains the functional blocks of program memory, data memory, ALU, I/O ports, on-chip timer, serial I/O and internal clock generator. It can extend external memory capacity (ROM, RAM) up to 60k bytes.

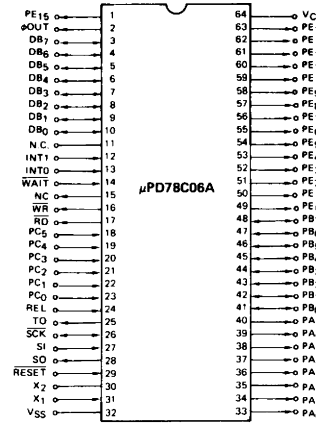
FEATURES

- Single-chip Microcomputer (μCOM-87LC)
- Powerful 101 Instructions
- Instruction Cycle Time: 4 μs (on-chip ROM); 2,6 μs (external memory & on-chip RAM) } for 78C06A
- Program Memory (ROM): 4096W x 8
- Data Memory (RAM): 128W x 8
- Direct Addressing Capability up to 60kB External Memory
- Powerful Addressing Modes Capability
- Multi-level Stack
- Vectored Interrupts (External: 2, Internal: 1)
- On-chip 8-bit Timer with 4-bit Prescaler
- 46 I/O Ports
- Serial I/O Ports
- Stand-by Capability (STOP/HALT mode)
- Fully Bus Compatible with 8080A
- On-chip Clock Generator
- Single Supply, CMOS Technology
- Low Power Consumption
- 64 pin Plastic Flat Package
- 64 pin Quil

PIN CONFIGURATION



(Top View)

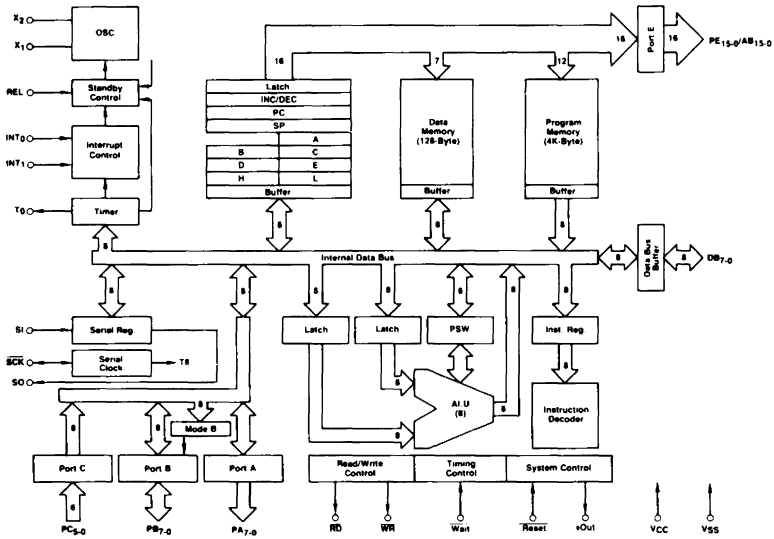


NC: Non-connection

PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
2-5 61-64	DB_0-DB_7	(Input/Output) This is an 8-bit bi-directional data bus. The data move between an external memory or I/O, and accumulator is done through this data bus. During an input, HALT, STOP mode, and RESET, the output of the data bus goes a high impedance state. Input/Output level are TTL compatible.
6	INT_1	(Input) It is a rising-edge sensitive interrupt line, and it becomes valid when INT_1 input goes low to high. Subsequently, if users want to perform another interrupt on this line after an interrupt on this line is accepted, they must take it into consideration that INT_1 input should be maintained at low state a little while, and then it should go high. Unless, it does not enable another interrupt.
7	INT_0	(Input) It is a level-sensitive interrupt input line which is high level active.
8	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state T_W and remains in that state as long as $\overline{WAIT}$ is active.
9	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
10	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
11-16	PC_0-PC_5	(Input) This is a 6-bit input port with pull-up resistors. Input data to this port can be test by test instruction, and also moved to least significant 6-bit of accumulator and higher 2-bit of accumulator is lodaded with "0". Input level is CMOS compatible. This port is fit for key-input port.
17	REL	(Input) This is an input to release the STOP mode of stand-by function. STOP mode is released by raising the REL input high, then clock generator which has been stopped will restart. During REL input is high, the bit 3 of Stand-by Control Register (SC3) is set to one, and it is reset to zero after REL signal returns low. Pull-down resistor is built in.
18	TO	(Output) The square wave is output from this line. Its cycle time is half of a count time of the internal timer. It goes on low level after reset.
19	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
20	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
22	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
22	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD78C06A.
23	X_2	(Output) Oscillator output.
24	X_1	(Input) Clock Input
27-34	PA_0-PA_7	(Output) 8-bit output port with latch capability.
35-42	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.
43-57,59	PE_0-PE_{15}	(Output) 16-bit address bus and output port.
64	ϕOUT	(Output) The Clock of system clock frequency (1/8 of crystal frequency or X_1 external clock frequency) is placed out from this line. It is still placed out in HALT mode, but it is fixed to high in STOP mode.

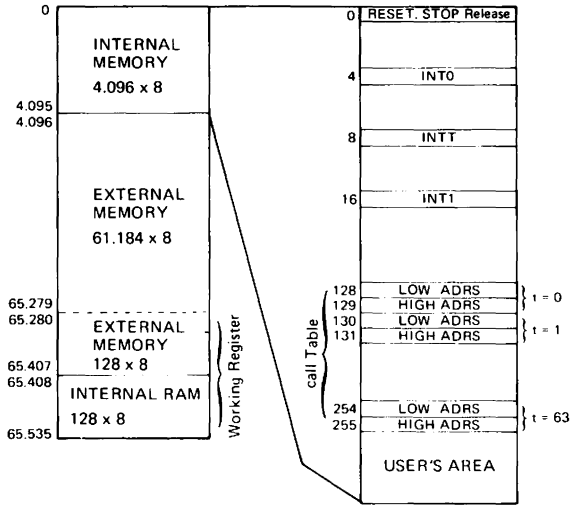
BLOCK DIAGRAM



Memory Map

FUNCTIONAL DESCRIPTION

The μPD78C06A can directly address the memory up to 64k bytes. Except on-chip ROM (0-4095) and RAM (65.408-65.535), and memory location can be used as either of RAM or ROM, freely. In the internal ROM area, the Reset/Stop mode Restart Address, Interrupt Start Address, Call Table etc. are involved. External memory and on-chip RAM area can be used as data memory (RAM), program memory (ROM), and/or working registers, freely.



FUNCTIONAL DESCRIPTION

I/O PORTS

PORT	FUNCTIONS
Port A	8-bit output port with latch
Port B	8-bit programmable Input/Output port w/latch
Port C	6-bit input port with pull up resistors
Port E	16-bit Address bus/Output Port

Port A

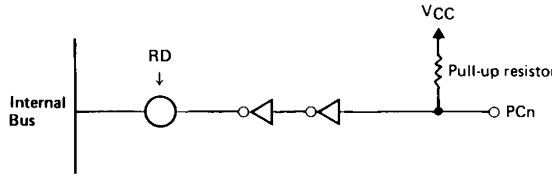
Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using Arithmetic and Logic instructions. Data remains latched at Port A unless acted on by another Port A instruction or a RESET is issued.

Port B

Port B is an 8-bit I/O port. Data is latched at Port B in both the Input or Output modes. Each bit of Port B can be independently set to either Input or Output mode. The Mode B register programs the individual lines of Port B to be either an Input (Mode $B_n = 1$) or an Output (Mode $B_n = 0$).

Port C

This is a 6-bit input port with pull-up resistors. Input data to this port can be test by instruction, and also moved to least significant 6-bit of accumulator and higher 2-bit of accumulator is loaded with "0". Input level is CMOS compatible. This port is fit for key-input port.



Port E (μPD78C06A)

Port E is a 16-bit address bus/output port. There are two ways to use these lines:

a) 16-Bit Address Bus – the PER instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).

b) 16-Bit Output Port – the PEX instruction sets Port E to a 16-bit output port. The contents of B and C registers appear on PE_{8-15} and PE_{0-7}, respectively.

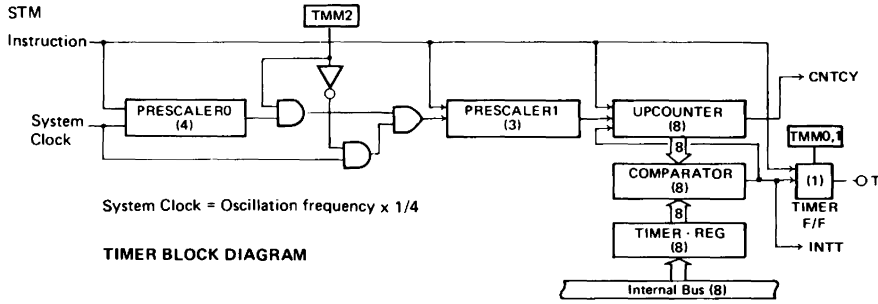
Address bus AB_{15}–AB_0 (μPD78C05A)

These lines are the 16 bit-to-bit address bus to the main memory. The μPD78C05A, having no internal ROM, must address the area from 0 to 4096 as external ROM.

The μPD78C05A AB lines are unlike the μPD78C06A PE lines; they have no internal latches. When the Port E output instruction PEX is executed in a μPD78C05A, the register pair BC is output to the AB lines for only one clock cycle during the third machine cycle. This is provided to allow external hardware to emulate the Port E operation of the μPD78C06A.

FUNCTIONAL DESCRIPTION (CONT.)

TIMER OPERATION



System Clock = Oscillation frequency x 1/4

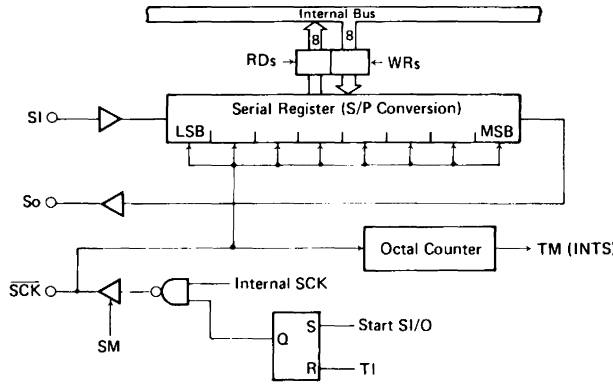
TIMER BLOCK DIAGRAM

This is a programmable 8-bit interval timer with prescaler. It consists of TIMER-REG (8-bit), PRESCALER0 (4-bit), PRESCALER1 (3-bit), UPCOUNTER (8-bit), COMPARATOR (8-bit), and TIMER F/F.

Count time and TO output are controlled by Timer Mode Register (TMM). It can count 5,3 μsec to 1,3 msec with resolution of 5,3 μsec (TMM2 = 0), or 85,3 μsec to 21,3 msec with resolution of 85,3 μsec (TMM2 = 1).

At first set the count value to the TIMER REG by MOV TM, A instruction, then initialize the PRESCALER0, 1, TIMER F/F, UPCOUNTER and start timer by STM instruction. UPCOUNTER is incremented at every 5,3 μs (TMM2 = 0) or 85,3 μs (TMM2 = 1(. COMPARATOR always compares the contents of UPCOUNTER with TIMER-REG, and it generates match signal (internal interrupt; INTT) when they are matched. The match signal clears the content of UPCOUNTER, and restarts the countup. Accordingly, this timer operates as the interval timer which generates repetitive interrupts with the interval of count time specified by count value of TIMER-REG. When a timer interrupt is generated in HALT mode, the HALT mode is released.

SERIAL PORT OPERATION



The Block Diagram of Serial Ports

FUNCTIONAL DESCRIPTION (CONT.)

Serial interface section consists of Serial Input (SI) line, Serial Output (SO) Line, Serial Clock ($\overline{SCK}$) input/output line, an 8-bit Serial Register (S/P), an octal counter, a R-S flip-flop used for transfer control, and some gates. When the bit 6 of Serial Mode Register (SM6) is 0, $\overline{SCK}$ becomes internal clock mode fixed to 1/8 of oscillator frequency (if fosc = 6MHz, then $\overline{SCK}$ is fixed to 780KHz), however, when the SM6 is 1, it becomes external clock mode, and operates with DC to 780KHz external clock. Accordingly, the transfer operation in internal clock mode is performed synchronously with constant frequency, and in external clock mode it performed synchronously with variable frequency.

A transmitting data is set to serial register by MOV S, A instruction, then the octal counter is reset and serial transfer is triggered by SIO instruction. At every falling edge of $\overline{SCK}$, the contents of serial register are shift, and shift-out data are placed to SO line with MSB as starting bit.

While the $\overline{SCK}$ is low the data on SI line is loaded in continuously, and then latched to serial register at the rising edge of the $\overline{SCK}$. Like this both the input and output of serial data are performed by same $\overline{SCK}$.

After occuring eight $\overline{SCK}$ pulses and completing 8-bit serial data transfer, the carry T8 is generated from the octal counter and it sets the interrupt request flag (INTFS). But μPD78C05A/06A has no serial interrupt, then INTFS is checked by only test instruction (SKNIT FS).

In internal $\overline{SCK}$ mode, as T8 signal resets the control flip-flop, the following transfer after completing 8-bit transfer are disabled until next SIO instruction will be given.

Accordingly, the data transfer should be restarted by SIO instruction with the next conditions. In case of data reception, after receiving the data from serial register by MOV A,S instruction, and in case of data transmission, after setting the data to serial register by MOV S,A instruction, data transmittion must be done by SIO instructions.

INTERRUPT STRUCTURE

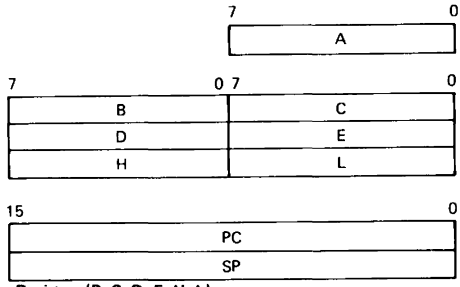
The μPD78C05A/06A provides a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from 3 different sources; two external interrupts and one internal interrupt. Each interrupt when activated branches to a designated memory vector location.

INT	VECTORED MEMORY LOCATION	PRIORITY	TYPE
INT_0	4	1	External, level sensitive
INT_1	16	3	External, rising edge sensitive
INTT	8	2	Internal, match on timer comparator

REGISTERS

FUNCTIONAL DESCRIPTION (CONT.)

This mainly consists of the seven 8-bit registers and two 16-bit registers as below.



General Purpose Registers (B, C, D, E, H, L)

They can function as auxilliary registers to the accumulator (A) or in pairs as data pointers (BC, DE, HL). Auto increment and decrement addressing mode capabilities extend the uses for the DE and HL register pairs.

Accumulator (A)

All data transfers between the μPD78C05A/06A and external memory or I/O are done through the accumulator. The contents of the Accumulator and Vector Registers can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A Reset sets the PC to 0000_H.

Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

STAND-BY OPERATION

Stand-by function is used to lower the power consumption in stand-by condition, and there are two types of it: HALT mode and STOP mode.

In HALT mode the masking functions are active, so that programmer can chose an interrupt source, $\overline{RESET}$ or T8-signal for release use.

STOP mode can be released by REL or RESET signal. In both cases, program will start at location 0 again.

HALT AND STOP MODE

FUNCTION	HALT MODE	STOP MODE
Oscillator	Run	
Internal System Clock	Stop	Stop
Timer	Run	
Timer Register	Hold	Set
Upcounter, Prescaler Q, I	Run	Cleared
Serial Interface		Run [1]
Serial Clock	Hold	Hold
Interrupt Control Circuit	Run	Stop
Interrupt Enable Flag	Hold	Reset
INT_0, INT_1 Input	Active	Inactive
INT_T		
T8 (INTFS)		
Mask Register	Hold	Set
Pending Interrupts (INTFX)		Reset
REL Input	Inactive	Active
$\overline{RESET}$ Input	Active	

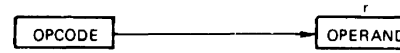
FUNCTION	HALT MODE	STOP MODE
On chip RAM	Hold	Hold
Output Latch in Ports A, B, E		
Address Bus AB0 ... 15		Low
Program Counter (PC)		Cleared
Stack Pointer (SP)		Unknown
General Registers (A, B, C, D, E, F, L)		
Program Status Word (PSW)	Hold	Reset
Mode B Register		Hold
Standby Control Register (SC_0 ... SC_3)		
Standby Control Register (SC_4)		Set
Timer Mode Register (TMM_0 - TMM_1)		Hold
Timer Mode Register (TMM_1)		Set
Serial Mode Register (SM)		Hold
Data Bus (DB_0 ... DB_7)	High Z	High-Z
$\overline{RD}$, $\overline{WR}$ Output	High	High

Note: 1. Serial clock counter is running and T8 is generated, however, there are no effects from it

ADDRESS MODES

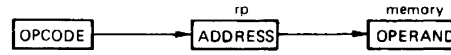
Register Addressing	Working Register Addressing
Register Indirect Addressing	Direct Addressing
Auto-Increment Addressing	Immediate Addressing
Auto-Decrement Addressing	Immediate Extended Addressing

Register Addressing



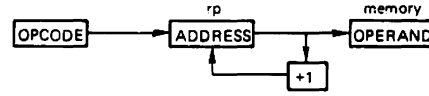
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

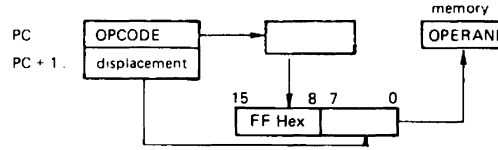
Auto-Increment Addressing



The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

Auto Decrement Addressing

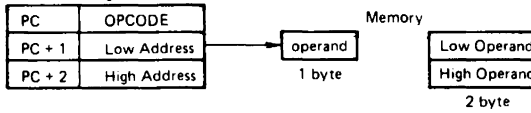
Working Register Addressing



The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix ending this address mode.

ADDRESS MODES (CONT.)

Direct Addressing



The two bytes following the opcode specify an address of a location containing the operand.

Immediate Addressing

Immediate Extended Addressing

PROGRAM STATUS WORD (PSW) OPERATION

OPERATION					D6	D5	D4	D3	D2	D0
REG. MEMORY		IMMEDIATE		SKIP	Z	SK	HC	L1	I0	CY
ADD ADC SUB SBB	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			↕	0	↕	0	0	↕
ANA ORA XRA	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		↕	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	LTIW		↕	↕	↕	0	0	↕
	ONAX OFFAX	ONI OFFI	ONIW OFFIW		↕	↕	•	0	0	•
NEA EQA	NEAX EQAX	NEI EQI	NEIW EQIW		↕	↕	↕	0	0	↕
INR DCR	INRW DCRW				↕	↕	↕	0	0	•
DAA					↕	0	↕	0	0	↕
RLL, RLR					•	0	•	0	0	↕
RLD – RRD					•	0	•	0	0	•
STC					•	0	•	0	0	1
CLC					•	0	•	0	0	0
		MVI A, byte			•	0	•	1	0	•
		MVI L, byte LXI H, word			•	0	•	0	1	•
				SKNC SKNZ SKNIT	•	↕	•	0	0	•
				RETS	•	1	•	0	0	•
All other instructions					•	0	•	0	0	•

Notes: ↕ Flag affected according to result op operation
1 Flag set
0 Flag reset
• Flag not affected.

Symbols/Description on Operand

SYMBOLS	DESCRIPTIONS
r	A, B, C, D, E, H, L
r1	B, C, D, E, H, L
r2	A, B, C
sr	PA PB MK MB TM S TMM SM SC
sr1	PA PB PC MK S TMM SC
sr2	PA PB PC MK
rp	SP, B, D, H
rp1	V, B, D, H
rpa	B, D, H, D+, H+, D−, H−
wa	8-bit immediate data
word	16-bit immediate data
byte	8-bit immediate data
bit	3-bit immediata data
if	F0, F1, FT, FS
f	CY, Z

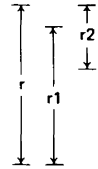
Notes:

1. At sr ~ sr2, the symbols of 'PA', 'PB', etc. stand for the following, respectively:
   PA = PORTA, PB = PORTB, PC = PORTC, MK = MASK-reg, MB = MODE-B,
   TM = TIMER-REG, S = SERIAL I/O, TMM = TIMER MODE REG,
   SM = SERIAL MODE REG, SC = STANDBY CONTROL REG
2. At rp ~ rp1, the 'SP', 'B', etc stand for the following, respectively;
   SP = STACK POINTER, B = BC, D = DE, H = HL, V = FFH-A
3. At rpa, the 'B', 'D', etc. stand for the following respectively:
   B = (BC), D = (DE), H = (HL), D+ = $(DE)^{+}$, H+ = $(HL)^{+}$, D− = $(DE)^{-}$,
   H− = $(HL)^{-}$
4. At if, the 'F0', 'F1', etc. stand for the following, respectively:
   F0 = INTF0, F1 = INTF1, FT = INTFT, FS = INTFS
5. At f, the 'CY', 'Z', stand for the following, respectively:
   CY = CARRY, Z = ZERO

The description of the symbols on Operation Codes is as follows:

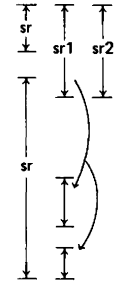
r

R_2	R_1	R_0	reg
0	0	0	
0	0	1	A
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L



sr

S_3	S_2	S_1	S_0	special reg
0	0	0	0	PORT A
0	0	0	1	PORT B
0	0	1	0	PORT C
0	0	1	1	MASK
0	1	0	0	MODE-B
0	1	0	1	–
0	1	1	0	TIMER-REG
0	1	1	1	–
1	0	0	0	SERIAL-I/O
1	0	0	1	TIMER MODE REG
1	0	1	0	SERIAL MODE REG
1	0	1	1	STANDBY CONTROL REG

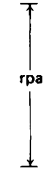


rp

P_1	P_0	reg-pair
0	0	SP
0	1	BC
1	0	DE
1	1	HL

rpa

A_2	A_1	A_0	addressing
0	0	0	–
0	0	1	(BC)
0	1	0	(DE)
0	1	1	(HL)
1	0	0	$(DE)^+$
1	0	1	$(HL)^+$
1	1	0	$(DE)^-$
1	1	1	$(HL)^-$



rp1

Q_1	Q_0	reg-pair
0	0	FFH.A
0	1	BC
1	0	DE
1	1	HL

if

I_2	I_1	I_0	INTF
0	0	0	INTF0
0	0	1	INTFT
0	1	0	INTF1
0	1	1	–
1	0	0	INTFS

f

F_2	F_1	F_0	flag
0	1	0	CY
1	0	0	Z

INSTRUCTION GROUPS

8-BIT DATA TRANSFER

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
MOV	r1, A	6	r1 ← A	
MOV	A, r1	6	A ← r1	
MOV	sr, A	14	sr ← A	
MOV	A, sr1	14	A ← sr1	
MOV	r, word	25	r ← (word)	
MOV	word, r	25	(word) ← r	
MVI	r, byte	11	r ← byte	
STAW	wa	14	(FFH, wa) ← A	
LDAW	wa	14	A ← (FFH, wa)	
STAX	rpa	9	(rpa) ← A	
LDAX	rpa	9	A ← (rpa)	
SBCD	word	28	(word) ← C, (word+1) ← B	
SDED	word	28	(word) ← E, (word+1) ← D	
SHLD	word	28	(word) ← L, (word+1) ← H	
SSPD	word	28	(word) ← SP_L, (word+1) ← SP_H	

16-BIT DATA TRANSFER

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
LBCD	word	28	C ← (word), B ← (word+1)	
LDED	word	28	E ← (word), D ← (word+1)	
LHLD	word	28	L ← (word), H ← (word+1)	
LSPD	word	28	SP_L ← (word), SP_H ← (word+1)	
PUSH	rp1	21	(SP−1) ← $rp1_H$, (SP−2) ← $rp1_L$	
POP	rp1	18	$rp1_L$ ← (SP), $rp1_H$ ← (SP+1) SP ← SP+2	
LXI	rp, word	16	rp ← word	

ARITHMETIC INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
ADD	A, r	12	A ← A+r	
ADDX	rpa	15	A ← A+(rpa)	
ADC	A, r	12	A ← A+r+CY	
ADCX	rpa	15	A ← A+(rpa)+CY	
SUB	A, r	12	A ← A−r	
SUBX	rpa	15	A ← A−(rpa)	
SBB	A, r	12	A ← A−r− CY	
SBBX	rpa	15	A ← A−(rpa)−CY	
ADDNC	A, r	12	A ← A+r	No Carry
ADDNCX	rpa	15	A ← A+(rpa)	No Carry
SUBNB	A, r	12	A ← A−r	No Borrow
SUBNBX	rpa	15	A ← A−(rpa)	No Borrow

LOGIC INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
ANA	A, r	12	A ← A∧r	
ANAX	rpa	15	A ← A∧(rpa)	
ORA	A, r	12	A ← A∨r	
ORAX	rpa	15	A ← A∨(rpa)	
XRA	A, r	12	A ← A∨r	
XRAX	rpa	15	A ← A∨(rpa)	
GTA	A, r	12	A−r−1	No Borrow
GTAX	rpa	15	A−(rpa)−1	No Borrow
LTA	A, r	12	A−r	Borrow
LTAX	rpa	15	A−(rpa)	Borrow
ONAX	rpa	15	A∧(rpa)	No Zero
OFFAX	rpa	15	A∧(rpa)	Zero
NEA	A, r	12	A−r	No Zero
NEAX	rpa	15	A−(rpa)	No Zero
EQA	A, r	12	A−r	Zero
EQAX	rpa	15	A−(rpa)	Zero

IMMEDIATE OPERATION INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
XRI	A, byte	11	A ← AVbyte	
DINC	A, byte	11	A ← A + byte	No Carry
SUINB	A, byte	11	A ← A−byte	No Borrow
ADI	A, byte	11	A ← A+byte	
ACI	A, byte	11	A ← A+byte+CY	
SUI	A, byte	11	A ← A−byte	
SBI	A, byte	11	A ← A−byte −CY	
ANI	A, byte	11	A ← A∧byte	
ORI	A, byte	11	A ← AVbyte	
GTI	A, byte	11	A−byte−1	No Borrow
LTI	A, byte	11	A−byte	Borrow
ONI	A, byte	11	A∧byte	No Zero
OFFI	A, byte	11	A∧byte	Zero
NEI	A, byte	11	A−byte	No Zero
EQI	A, byte	11	A−byte	Zero

SPECIAL REGISTER

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
ANI	sr2, byte	23	sr2 ← sr2∧byte	
ORI	sr2, byte	23	sr2 ← sr2Vbyte	
ONI	sr2, byte	20	sr2∧byte	No Zero
OFFI	sr2, byte	20	sr2∧byte	Zero

WORKING REGISTER OPERATIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
ANIW	wa, byte	22	(FFH.wa) ← (FFH.wa)∧byte	
ORIW	wa, byte	22	(FFH.wa) ← (FFH.wa)Vbyte	
GTIW	wa, byte	19	(FFH.wa)−byte−1 No Borrow	No Borrow
LTIW	wa, byte	19	(FFH.wa)−byte	Borrow
ONIW	wa, byte	19	(FFH.wa)∧byte	No Zero
OFFIW	wa, byte	19	(FFH.wa)∧byte	Zero
NEIW	wa, byte	19	(FFH.wa)−byte	No Zero
EQIW	wa, byte	19	(FFH.wa)−byte	Zero

INCREMENT/DECREMENT INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
INR	r2	6	r2 ← r2+1	Carry
INRW	wa	17	(FFH.wa) ← (FFH.wa)+1	Carry
DCR	r2	6	r2 ← r2−1	Borrow
DCRW	wa	17	(FFH.wa) ← (FFH.wa)−1	Borrow
INX	rp	9	rp ← rp+1	
DCX	rp	9	rp ← rp−1	

OTHER OPERATIONAL INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
DAA		6	Decimal Adjust Accumulator	
STC		12	CY ← 1	
CLC		12	CY ← 0	

ROTATION INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
RLD		21	Rotate Left Digit	
RRD		21	Rotate Right Digit	
RLL	A	12	Am+1 ← Am, A_0 ← CY, CY ← A_7	
RLR	A	12	Am−1 ← Am, A_7 ← CY, CY ← A_0	

JUMP INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
JMP	word	16	PC ← word	
JB		6	PC_H ← B PC_L ← C	
JR	word	12	PC ← PC+1+jdisp1	
JRE	word	17	PC ← PC+2+jdisp	

CALL INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
CALL	word	22	(SP−1) ← $(PC+3)_H$, (SP−2) ← $(PC+3)_L$, PC ← word	
CALF	word	17	(SP−1) ← $(PS+2)_H$, (SP−2) ← $(PC+2)_L$ PC15~11 ← 00001, PC10~0 ← 1a	
CALT	word	21	(SP−1) ← $(PC+1)_H$, (SP−2) → $(PC+1)_L$ PC_L ← (128+21a), PC_H ← (129+21a)	

RETURN INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
RET		12	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$ $SP \leftarrow SP+2$	
RETS		12+n	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, $SP \leftarrow SP+2$ $PC \leftarrow PC+n$	Uncon-ditional Skip
RETI		15	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$ $PSW \leftarrow (SP+2)$, $SI' \leftarrow SP+3$	

SKIP INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
SKN	CY	12	Skip if No Carry	CY = 0
SKN	Z	12	Skip if No Zero	Z = 0
SKNIT	if	12	Skip if No INTX Reset INTX if INTX = 1	f = 0

CPU CONTROL INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
NOP		6	No Operation	
EI		12	Enable Interrupt	
DI		12	Disable Interrupt	

REGISTER CONTROL INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
SIO		6	Start (Trigger) Serial I/O	
STM		6	Start Timer	

INPUT/OUTPUT INSTRUCTIONS

MNEMONICS	OPERAND	CLOCK CYCLE	FUNCTIONS	SKIP CONDITION
PEX		15	$PE_{15-8} \leftarrow B$, $PE_{7-0} \leftarrow C$	
PER		12	Port E AB Mode	

(Note)

The clock cycles shown here are indicated about in care of that the program are located in the on-chip ROM, and the other data are located in the on-chip RAM or external memory requiring no wait. If the programs were located in the on-chip RAM or external memory, then the clock cycles are shortened by two clock cycles per one-byte fetch.

Ex. PER instruction (2-byte instruction)

In case of the on-chip ROM access: 12 clock cycles

In case of the on-chip RAM or external memory access: 12– (2x2) = 8 clock cycles

1 clock cycle = 4/fosz

ELECTRICAL SPECIFICATIONS AND PACKAGE OUTLINES FOR μPD78C05A/μPD78C06A

for extended temperature range
T_a = −40 to +85°C

μPD78C05AG ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Supply Voltage	V_{CC}		−0.3 to +7.0	V
Input Voltage	V_I		−0.3 to V_{CC} + 0.3	V
Output Voltage	V_O		−0.3 to V_{CC} + 0.3	V
Output High Current	I_{OH}	Device Total	−5	mA
Output Low Current	I_{OL}	Device Total	43.5	mA
Operating Temperature	T_{opt}		-40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

DC CHARACTERISTICS

(T_a = −40 to +85°C, V_{CC} = +5.0V ± 10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH1}	$\overline{INT}_{0-1}$, $\overline{WAIT}$, PB_{0-7}, PC_{0-5}	0.7 V_{CC}		V_{CC}	V
	V_{IH2}	$\overline{RESET}$, SCK, REL, SI	0.75 V_{CC}		V_{CC}	V
	V_{IH3}	DB_{0-7}	V_{CC} −2.0		V_{CC}	V
	V_{IH4}	X1	V_{CC} −0.5		V_{CC}	V
Input Low Voltage	V_{IL1}	$\overline{INT}_{0-1}$, $\overline{WAIT}$, PB_{0-7}, PC_{0-5}	0		0.3 V_{CC}	V
	V_{IL2}	$\overline{RESET}$, SCK, REL, SI	0		0.25 V_{CC}	V
	V_{IL3}	DB_{0-7}	0		0.8	V
	V_{IL4}	X1	0		0.5	V
Output High Voltage	V_{OH1}	I_{OH} = −100 μA	2.4			V
	V_{OH2}	I_{OH} = −50 μA	V_{CC} −0.5			V
Output Low Voltage	V_{OL}	I_{OL} = 1.8 mA			0.45	V
Input High Current	I_{IH1}	V_{IN} = V_{CC} (REL)	7		100	μA
	I_{IH2}	V_{IN} = V_{CC} (X1)			45	μA
Input Low Current	I_{IL1}	V_{IN} = 0V ($\overline{WAIT}$, PC_{0-5})	−7		−100	μA
	I_{IL2}	V_{IN} = 0V (X1)			−45	μA
Input High Leakage Current	I_{LIH}	V_{IN} = V_{CC} (Except REL, X1)			3.2	μA
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0V (Except $\overline{WAIT}$, PC_{0-5}, X1)			−3.2	μA
	I_{LIL2}	V_{IN} = 0V (STOP Mode, X1)			−3.2	μA
Output High Leakage Current	I_{LOH}	V_{OUT} = V_{CC}			3.2	μA
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0V			−3.2	μA
V_{CC} Supply Current	I_{CC1}	Operation Mode		4.0	7.5	mA
	I_{CC2}	HALT Mode		1.2	2.7	mA
	I_{CC3}	STOP Mode (X1 = 0V, X2 = Open)		1	20	μA

CAPACITANCE

(T_a = 25°C, V_{CC} = GND = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_C = 1MHz Unmeasured Pins returned to 0V			15	pF
Output Capacitance	C_O				15	pF
I/O Capacitance	$C_{I/O}$				15	pF

(T_a = −40 to +85°C, V_{CC} = +5.0V ± 10 %)

AC CHARACTERISTICS CLOCK TIMING

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
X1 Input Cycle Time	t_{CYX}		160		10000	ns
X1 Input Low Time	t_{XXL}		75			ns
X1 Input High Time	t_{XXH}		75			ns
ϕ_{OUT} Cycle Time	$t_{CY\phi}$		640		40000	ns
ϕ_{OUT} Low Time	$t_{\phi\phi L}$		195			ns
ϕ_{OUT} High Time	$t_{\phi\phi H}$		195			ns
ϕ_{OUT} Rise/Fall Time	t_r, t_f				120	ns

READ/WRITE OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RD}$ L. E. to ϕ_{OUT} L. E.	$t_{R\phi}$	$t_{CY\phi}$ = 660 ns	180			ns
Address (PE_{0-15}) to Data Input	t_{AD1}				790 +660xN	ns
$\overline{RD}$ T. E. to Address	t_{RA}		180(T3) 840(T4)			ns
$\overline{RD}$ L. E. to Data Input	t_{RD}				460 +660xN	ns
$\overline{RD}$ T. E. to Data Hold Time	t_{RDH}		0			ns
$\overline{RD}$ Low Time	t_{RR}		1070 +660xN			ns
$\overline{RD}$ L. E. to $\overline{WAIT}$ L. E.	t_{RWT}				460	ns
Address (PE_{0-15}) to $\overline{WAIT}$ L. E.	t_{AWT1}				790	ns
$\overline{WAIT}$ Set Up Time to ϕ_{OUT} L. E.	t_{WTS}		370			ns
$\overline{WAIT}$ Hold Time after ϕ_{OUT} L. E.	t_{WTH}		0			ns
M1 to RD L. E.	t_{MR}		108			ns
RD T. E. to M1	t_{RM}		130			ns
ϕ_{OUT} L. E. to $\overline{WR}$ L. E.	$t_{\phi W}$				175	ns
Address (PE_{0-15}) to ϕ_{OUT} T. E.	$t_{A\phi}$		90			ns
Address (PE_{0-15}) to Data Output	t_{AD2}		510			ns
Data Output to $\overline{WR}$ T. E.	t_{DW}		740 +660xN			ns
$\overline{WR}$ T. E. to Data Stable Time	t_{WD}		130			ns
Address (PE_{0-15}) to $\overline{WR}$ L. E.	t_{AW}		460			ns
$\overline{WR}$ T. E. to Address Stable Time	t_{WA}		180			ns
$\overline{WR}$ Low Time	t_{WW}		690 +660xN			ns
$\overline{WR}$ L. E. to $\overline{WAIT}$ L. E.	t_{WWT}				110	ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	1270			ns
		$\overline{SCK}$ Output	1280		80000	ns
$\overline{SCK}$ Low Time	t_{KKL}	$\overline{SCK}$ Input	515			ns
		$\overline{SCK}$ Output	520			ns
$\overline{SCK}$ High Time	t_{KKH}	$\overline{SCK}$ Input	515			ns
		$\overline{SCK}$ Output	520			ns
SI Set Up Time to $\overline{SCK}$ T. E.	t_{SIS}		200			ns
SI Hold Time after $\overline{SCK}$ T. E.	t_{SIH}		250			ns
$\overline{SCK}$ L. E. to SO Delay Time	t_{KO}				300	ns

Note: 1) Input timings are measured at V_{IHMIN} and V_{ILMAX}.

2) Output timings are measured at V_{OH} = 2.4 V and V_{OL} = 0.45 V with 1TTL + 200 pF load.

3) L. E. = Leading Edge, T. E. = Trailing Edge

4) N is number of T_{WAIT}.

BUS TIMING DEPENDING ON tCYC

(T_a = −40 to + 85°C)

SYMBOL	CALCULATING EXPRESSION	MIN/MAX	UNITS
$t_{R\phi}$	(1/2)T − 150	MIN	ns
t_{AD1}	(3/2+N)T − 200	MAX	ns
$t_{RA(T3)}$	(1/2)T − 150	MIN	ns
$t_{RA(T4)}$	(3/2)T − 150	MIN	ns
t_{RD}	(1+N)T − 200	MAX	ns
t_{RR}	(2+N)T − 250	MIN	ns
t_{RWT}	T − 200	MAX	ns
t_{AWT1}	(3/2)T − 200	MAX	ns
t_{WTS}	(1/3)T + 150	MIN	ns
t_{MR}	(3/8)T − 140	MIN	ns
t_{RM}	(1/2)T − 200	MIN	ns
$t_{A\phi}$	(1/2)T − 240	MIN	ns
t_{AD2}	T − 150	MIN	ns
t_{DW}	(3/2+N)T − 250	MIN	ns
t_{WD}	(1/2)T − 200	MIN	ns
t_{AW}	T − 200	MIN	ns
t_{WA}	(1/2)T − 150	MIN	ns
t_{WW}	(3/2+N)T − 300	MIN	ns
t_{WWT}	(1/2)T − 220	MAX	ns
t_{CYK}	2T	MIN	ns
t_{KKL}	T − 120	MIN	ns
t_{KKH}	T − 120	MIN	ns

Note: 1) N = Number of T_{WAIT}.

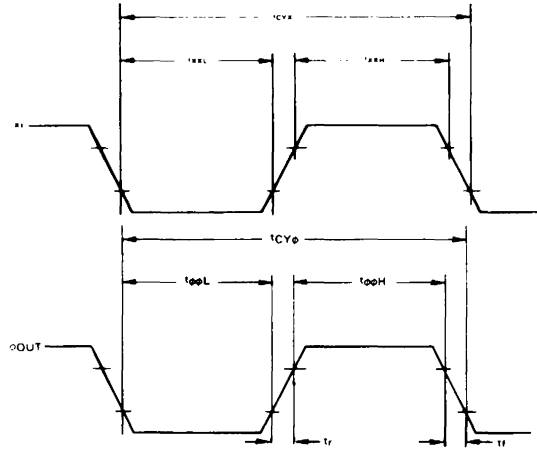
2) T = $T_{CY\phi}$.

3) t_{CY} assumes 50 % duty cycle on X1.

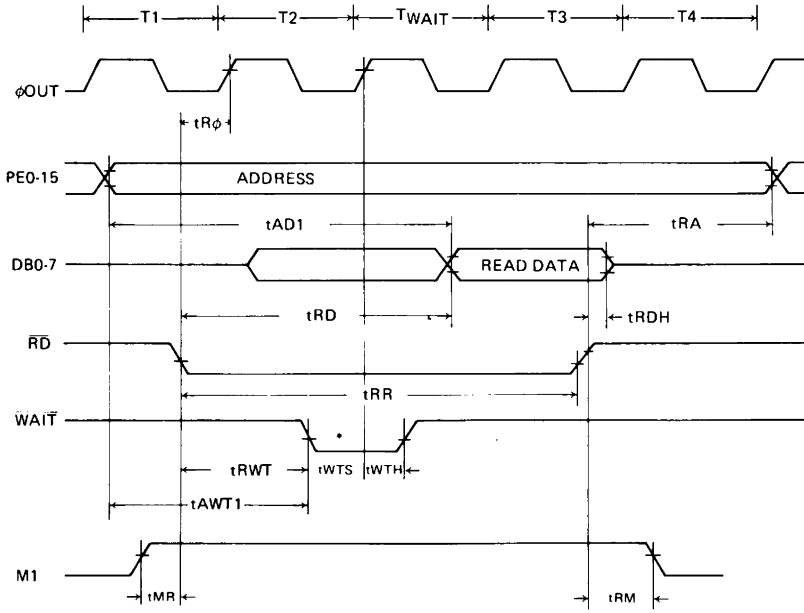
4) The items out of this table are not dependent on t_{CY}.

TIMING WAVEFORMS

CLOCK TIMING

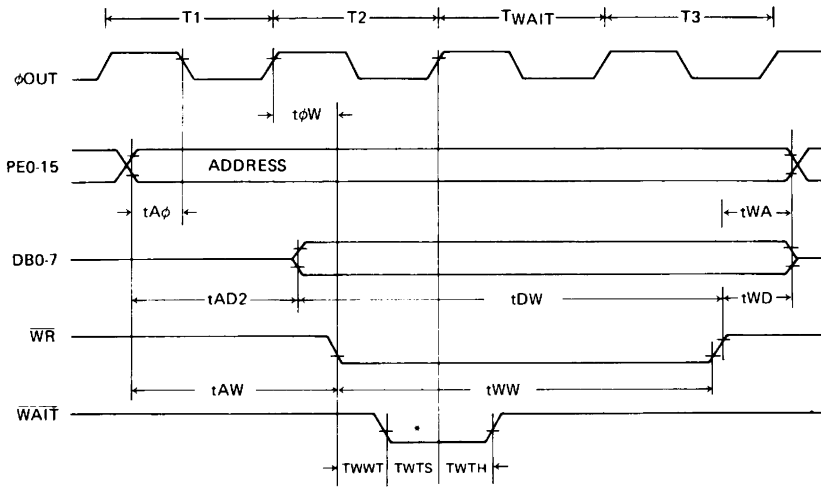


READ OPERATION



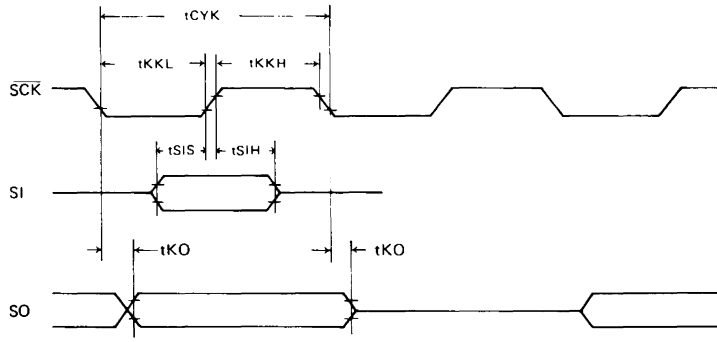
* WAIT signal must be remained stable during t_{WTS} and t_{WTH}.
If it is unstable, misoperation may occur.

WRITE OPERATION



* WAIT signal must be remained stable during t_{WTS} and t_{WTH}.
If it is unstable, misoperation may occur.

SERIAL OPERATION



Low Power Data Memory Retention Characteristics for STOP Mode Operation

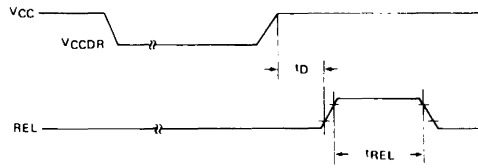
(T_a = −40 to +85°C)

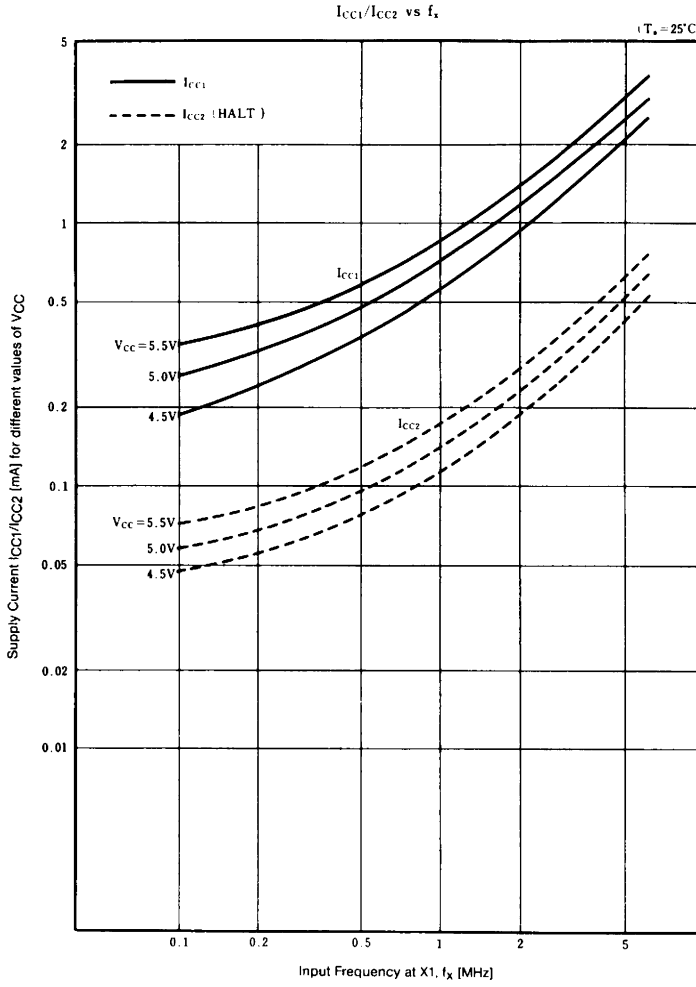
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{CCDR}		2.0			V
Data Retention Supply Current	I_{CCDR}	V_{CCDR} = 2.0V, X1 = 0V, X2 = Open		0.8	20	μA
Data Retention Input Low REL Voltage	V_{ILDR}		0		0.2 V_{CCDR}	V
Data Retention Input High $\overline{RESET}$ Voltage	V_{IHDR}		0.8 V_{CCDR}		V_{CCDR}	V
REL Input Delay Time	t_D		500			μs
REL Input High Time	t_{REL}		10			μs

Note: In data retention mode,

1) Input voltages to $\overline{WAIT}$ and PC_{0-5} pins (with pull-up resisters) should be maintained same as V_{CCDR} level.

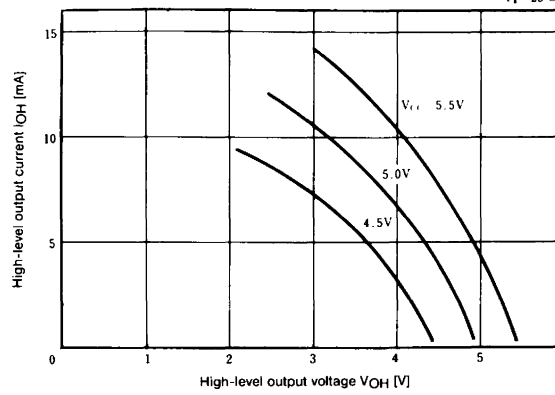
2) Other input voltages should be kept less than V_{CCDR} level.




I_{CC1}/I_{CC2} vs f_x
(T_a=25°C)
I_{CC1}
I_{CC2} (HALT)
I_{CC1}
V_{CC}=5.5V
5.0V
4.5V
I_{CC2}
V_{CC}=5.5V
5.0V
4.5V
Supply Current I_{CC1}/I_{CC2} [mA] for different values of V_{CC}
5
2
1
0.5
0.2
0.1
0.05
0.02
0.01
0.1
0.2
0.5
1
2
5
10
Input Frequency at X1, f_X [MHz]

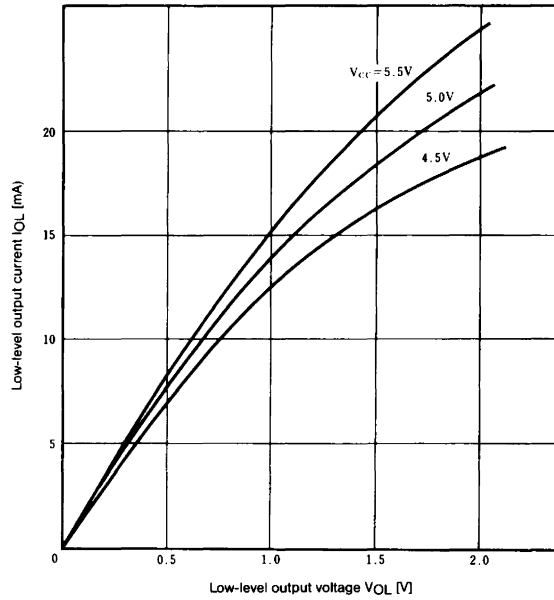
I_{OH} vs V_{OH}

(T_A = 25°C)



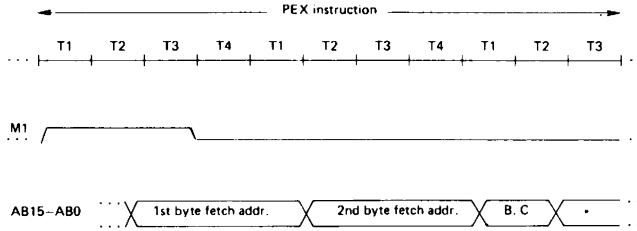
I_{OL} vs V_{OL}

(T_A = 25°C)



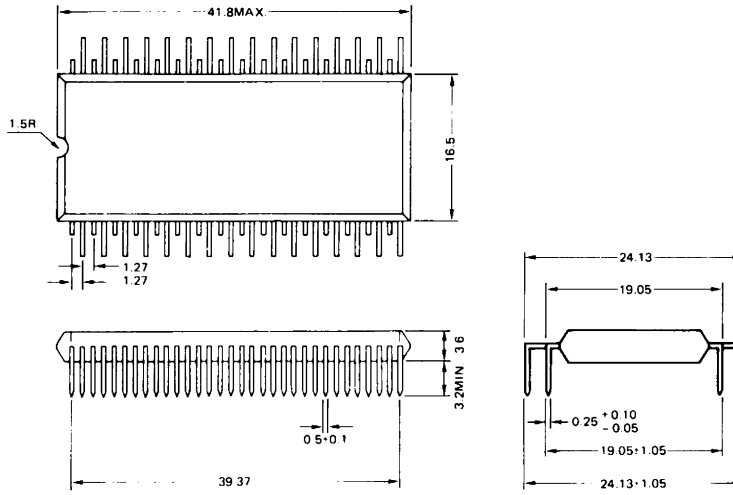
PORT E OPERATION μPD78C05A

The following diagram is the timing at PEX instruction execution.



*: 2nd byte fetch addr.

64 PIN PLASTIC QUIP OUTLINE (Unit : mm) for μPD78C05AG



Differences between μPD78C06A and μPD78C05A

Parameter		μPD78C06A	μPD78C05A
4K-byte built-in ROM		Yes	No
Internal WAIT of built-in ROM		2 WAIT cycle	No
Port E (Address bus)	After reset	Port mode	Address bus mode
	Latch function	Yes	No
	PEX instruction	PE15 - 8⇔B and PE7 - 0⇔C are executed and latched at M3T1 timing. Output is unchanged until the next PEX or PER instruction is executed.	AB15 - 8⇔B and AB7 - 0⇔C are executed only at M3T1 timing and the contents of the internal address bus are output at the other timing.
$\overline{RD}$/$\overline{WR}$ signal		Output against the address space of 1000H - FF7FH (4096 - 65407).	Output against the address space of 000H - FF7FH (0 - 65407).
M1 output		No	Yes
Pin connection		Difference	
Package		64 pin Flat 64 pin QUIP	64 pin QUIP

μPD78C06AG ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Supply Voltage	V_{CC}		−0.3 to +7.0	V
Input Voltage	V_I		−0.3 to V_{CC} + 0.3	V
Output Voltage	V_O		−0.3 to V_{CC} + 0.3	V
Output High Current	I_{OH}	Device Total	−5	mA
Output Low Current	I_{OL}	Device Total	45	mA
Operating Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

DC CHARACTERISTICS

(T_a = −40 to +85°C, V_{CC} = +5.0V ± 10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH1}	INT_{0-1}, $\overline{WAIT}$, PB_{0-7}, PC_{0-5}	0.7 V_{CC}		V_{CC}	V
	V_{IH2}	$\overline{RESET}$, SCK, REL, SI	0.75 V_{CC}		V_{CC}	V
	V_{IH3}	DB_{0-7}	V_{CC} −2.0		V_{CC}	V
	V_{IH4}	X1	V_{CC} −0.5		V_{CC}	V
Input Low Voltage	V_{IL1}	INT_{0-1}, $\overline{WAIT}$, PB_{0-7}, PC_{0-5}	0		0.3 V_{CC}	V
	V_{IL2}	$\overline{RESET}$, SCK, REL, SI			0.25 V_{CC}	V
	V_{IL3}	DB_{0-7}	0		0.8	V
	V_{IL4}	X1	0		0.5	V
Output High Voltage	V_{OH1}	I_{OH} = −100 μA	2.4			V
	V_{OH2}	I_{OH} = −50 μA	V_{CC} −0.5			V
Output Low Voltage	V_{OL}	I_{OL} = 1.8 mA			0.45	V
Input High Current	I_{IH1}	V_{IN} = V_{CC} (REL)	7		100	μA
	I_{IH2}	V_{IN} = V_{CC} (X1)			45	μA
Input Low Current	I_{IL1}	V_{IN} = 0V ($\overline{WAIT}$, PC_{0-5})	−7		−100	μA
	I_{IL2}	V_{IN} = 0V (X1)			−45	μA
Input High Leakage Current	I_{LIH}	V_{IN} = V_{CC} (Except REL, X1)			3.2	μA
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0V (Except $\overline{WAIT}$, PC_{0-5}, X1)			−3.2	μA
	I_{LIL2}	V_{IN} = 0V (STOP Mode, X1)			−3.2	μA
Output High Leakage Current	I_{LOH}	V_{OUT} = V_{CC}			3.2	μA
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0V			−3.2	μA
V_{CC} Supply Current	I_{CC1}	Operation Mode		4.0	7.5	mA
	I_{CC2}	HALT Mode		1.2	2.7	mA
	I_{CC3}	STOP Mode (X1 = 0V, X2 = Open)		1	20	μA

DC CHARACTERISTICS

(T_a = −40 to +85°C, V_{CC} = +2.5V to +6.0V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage High	V_{IH1}	Except DB_{0-7}, X1		0.8V_{CC}		V_{CC}	V
	V_{IH2}	DB_{0-7}		0.7V_{CC}		V_{CC}	V
	V_{IH3}	X1	(1)	0.9V_{CC}		V_{CC}	V
			(2)	V_{CC}−0.5		V_{CC}	V
Input Voltage Low	V_{IL1}	Except DB_{0-7}, X1		0		0.2V_{CC}	V
	V_{IL2}	DB_{0-7}	(1)	0		0.18V_{CC}	V
			(2)	0		0.8	V
	V_{IL3}	X1	(1)	0		0.1V_{CC}	V
			(2)	0		0.5	V
Output Voltage	V_{OH}	I_{OH} = −50μA		V_{CC}−0.5			V
Output Voltage Low	V_{OL}	I_{OL} = 400μA				0.45	V
Input Current High	I_{IH1}	V_{IN} = V_{CC} (REL)		2.5		110	μA
	I_{IH2}	V_{IN} = V_{CC} (X1)				50	μA
Input Current Low	I_{IL1}	V_{IN} = 0V ($\overline{WAIT}$, PC_{0-5})		−2.5		−110	μA
	I_{IL2}	V_{IN} = 0V (X1)				−50	μA
Input Leakage Current High	I_{LIH}	V_{IN} = V_{CC} (Except REL, X1)				3.5	μA
Input Leakage Current Low	I_{LIL1}	V_{IN} = 0V (Except $\overline{WAIT}$, PC_{0-5}, X1)				−3.5	μA
	I_{LIL2}	V_{IN} = 0V (STOP Mode, X1)				−3.5	μA
Output Leakage Current High	I_{LOH}	V_{OUT} = V_{CC}				3.5	μA
Output Leakage Current Low	I_{LOL}	V_{OUT} = 0V				−3.5	μA
V_{CC} Supply Current	I_{CC1}	Operation Mode	V_{CC} = 3V, t_{CYO} = 8μs		0.7	1.5	mA
			V_{CC} = 6V, t_{CYO} = 1.32μs		5.0	9.0	mA
	I_{CC2}	HALT Mode	V_{CC} = 3V, t_{CYO} = 8μs		0.2	0.5	mA
			V_{CC} = 6V, t_{CYO} = 1.32μs		1.5	3.0	mA
	I_{CC3}	STOP Mode	(X1 = 0V, X2 = Open)		1	20	μA

Notes 1 2.5V ≤ V_{CC} ≤ 4.5V
2 4.5V ≤ V_{CC} ≤ 6.0V

CAPACITANCE

(T_a = 25°C, V_{CC} = GND = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_C = 1MHz			15	pF
Output Capacitance	C_O	Unmeasured Pins returned to 0V			15	pF
I/O Capacitance	$C_{I/O}$				15	pF

AC CHARACTERISTICS CLOCK TIMING:

(T_a = −40°C to +85°C)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} = 5.0V ± 10%			V_{CC} = 2.5V to +6.0V		
				MIN	MAX	UNIT	MIN	MAX	UNIT
X1 Input Cycle Time	t_{CYX}			160	10000	ns	1.65	10	μs
X1 Input Low Level Width	t_{XXL}			75		ns	0.78		μs
X1 Input High Level Width	t_{XXH}			75		ns	0.78		μs
ϕ_{OUT} Cycle Time	t_{CYO}			1280	80000	ns	13.2	80	μs
ϕ_{OUT} Low Level Width	t_{OOL}			515		ns	6.35		μs
ϕ_{OUT} High Level Width	t_{OOH}			515		ns	6.35		μs
ϕ_{OUT} Rise/Fall Time	t_r, t_f				120	ns		250	ns
Clock Oscillation Frequency (X1, X2)	f_{OSC}	Crystal oscillation	4.5V ≦ V_{CC} ≦ 6.0V				3.5	6.25	MHz
		Ceramic oscillation	4.5V ≦ V_{CC} ≦ 6.0V				0.1	6.25	MHz
			V_{CC} = 3.5V				0.1	4.0	MHz
			V_{CC} = 2.7V				0.1	0.6	MHz

READ/WRITE OPERATION

(T_a = −40°C to +85°C)

PARAMETER	SYMBOL	V_{CC} = +5.0V ± 10%				V_{CC} = 2.5V to +6.0V			
		TEST CONDITIONS	MIN	MAX	UNIT	TEST CONDITIONS	MIN	MAX	UNIT
$\overline{RD}$ L.E. to ϕ_{OUT} L.E.	t_{RO}		180		ns		3.1		μs
Address (PE_{0-15}) to Data Input	t_{AD1}			790 +660xN	ns			9.7 +6.6xN	μs
$\overline{RD}$ T.E. to Address	t_{RA}		180(T3) 840(T4)		ns		3.05(T3) 9.65(T4)		μs
$\overline{RD}$ L.E. to Data Input	t_{RD}			460 +660xN	ns			6.4 +6.6xN	μs
$\overline{RD}$ T.E. to Data Hold Time	t_{RDH}		0		ns		0		μs
$\overline{RD}$ Low Level Width	t_{RR}		1070 +660xN		ns		12.93 +6.6xN		μs
$\overline{RD}$ L.E. to $\overline{WAIT}$ L.E.	t_{RWT}			460	ns			6.4	μs
Address (PE_{0-15}) to $\overline{WAIT}$ L.E.	t_{AWT1}			790	ns			9.7	μs
$\overline{WAIT}$ Set Up Time to ϕ_{OUT} L.E.	t_{WTS}		370		ns		2.35		μs
$\overline{WAIT}$ Hold Time after ϕ_{OUT} L.E.	t_{WTH}	t_{CYO} = 1320ns	0		ns	t_{CYO} = 13.2μs	0		μs
ϕ_{OUT} L.E. to $\overline{WR}$ L.E.	t_{OW}			175	ns			0.25	μs
Address (PE_{0-15}) to ϕ_{OUT} T.E.	t_{AO}		420		ns		6.1		μs
Address (PE_{0-15}) to Data Output	t_{AD2}		510		ns		6.4		μs
Data Output to $\overline{WR}$ T.E.	t_{DW}		740 +660xN		ns		9.35 +6.6xN		μs
$\overline{WR}$ T.E. to Data Stable Time	t_{WD}		130		ns		3.05		μs
Address (PE_{0-15}) to $\overline{WR}$ L.E.	t_{AW}		460		ns		6.35		μs
$\overline{WR}$ T.E. to Address Stable Time	t_{WA}		180		ns		3.05		μs
$\overline{WR}$ Low Level Width	t_{WW}		690 +660xN		ns		9.5 +6.6xN		μs
$\overline{WR}$ L.E. to $\overline{WAIT}$ L.E.	t_{WWT}			110	ns			3.08	μs

N: Number of T_{WAIT}

SERIAL OPERATION

(T_a = −40°C to +85°C)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} = +5.0V ± 10% MIN	MAX	UNIT	V_{CC} = +2.5V to + 6.0V MIN	MAX	UNIT
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	1270		ns	13.2		μs
		$\overline{SCK}$ Output	1280	80000	ns	13.2	80	μs
$\overline{SCK}$ Low Level Width	t_{KKL}	$\overline{SCK}$ Input	515		ns	6.35		μs
		$\overline{SCK}$ Output	520		ns	6.35		μs
$\overline{SCK}$ High Level Width	t_{KKH}	$\overline{SCK}$ Input	515		ns	6.35		μs
		$\overline{SCK}$ Output	520		ns	6.35		μs
SI Set Up Time to $\overline{SCK}$ T.E.	t_{SIS}		200		ns	0.3		μs
SI Hold Time after $\overline{SCK}$ T.E.	t_{SIH}		250		ns	0.5		μs
$\overline{SCK}$ L.E. to SO Delay Time	t_{KO}			300	ns		0.8	μs

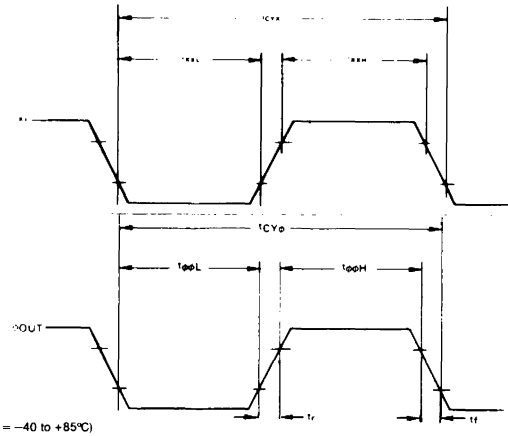
Notes 1. Input timings are measured at V_{IHMIN} and V_{ILMAX}

2. Output timings are measured at with 1TTL + 200pF load. V_{OH} = 2.4V and V_{OL} = 0.45V (V_{CC} = 5.0V ± 10%); V_{OH} = 0.7V_{CC} and V_{OL} = 0.3V_{CC} (V_{CC} = 2.5V to +6.0V)

3. L.E. = Leading Edge, T.E. = Trailing Edge

4. Use the following table (on same page) to calculate AC parameters in $t_{CY\Phi}$ 1320ns (V_{CC} = 5.0V ± 10%) resp. $t_{CY\Phi}$ 13.2 μs (V_{CC} = 2.5V to + 6.0V)

TIMING WAVEFORMS CLOCK TIMING



BUS TIMING DEPENDING ON $t_{CY\Phi}$

(T_a = −40 to +85°C)

SYMBOL	V_{CC} = +5.0V ± 10% CALCULATING EXPRESSION	MIN/MAX	UNIT	V_{CC} = +2.5V to +6.0V CALCULATING EXPRESSION	MIN/MAX	UNIT
$t_{R\Phi}$	(1/2)T − 150	MIN	ns	(1/2)T − 200	MIN	ns
t_{AD1}	(3/2+N)T − 200	MAX	ns	(3/2+N)T − 200	MAX	ns
$t_{RA(T3)}$	(1/2)T − 150	MIN	ns	(1/2)T − 250	MIN	ns
$t_{RA(T4)}$	(3/2)T − 150	MIN	ns	(3/2)T − 250	MIN	ns
t_{RD}	(1+N)T − 200	MAX	ns	(1+N)T − 200	MAX	ns
t_{RR}	(2+N)T − 250	MIN	ns	(2+N)T − 270	MIN	ns
t_{RWT}	T − 200	MAX	ns	T − 200	MAX	ns
t_{AWT1}	(3/2)T + 200	MAX	ns	(3/2)T − 200	MAX	ns
t_{WTS}	(1/3)T + 150	MIN	ns	(1/3)T + 150	MIN	ns
$t_{A\Phi}$	T − 240	MIN	ns	T − 500	MIN	ns
t_{AD2}	T − 150	MIN	ns	T − 200	MIN	ns
t_{DW}	(3/2+N)T − 250	MIN	ns	(3/2+N)T − 550	MIN	ns
t_{WD}	(1/2)T − 200	MIN	ns	(1/2)T − 250	MIN	ns
t_{AW}	T − 200	MIN	ns	T − 250	MIN	ns
t_{WA}	(1/2)T − 150	MIN	ns	(1/2)T − 250	MIN	ns
t_{WW}	(3/2+N)T − 300	MIN	ns	(3/2+N)T − 400	MIN	ns
t_{WWT}	(1/2)T − 220	MAX	ns	(1/2)T − 220	MAX	ns
t_{CYK}	2T	MIN	ns	2T	MIN	ns
t_{KKL}	T − 120	MIN	ns	T − 250	MIN	ns
t_{KKH}	T − 120	MIN	ns	T − 250	MIN	ns

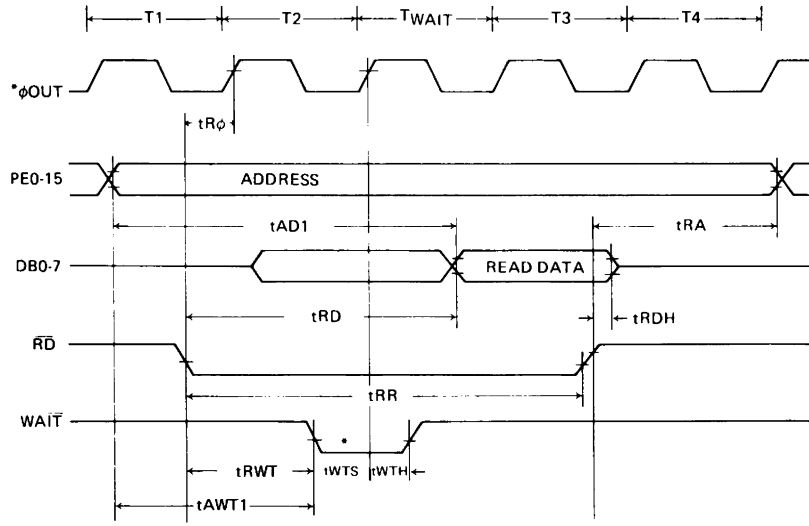
Notes 1. N = Number of T_{WAIT}

2. T = $t_{CY\Phi}$/2

3. For external clock, 50% duty cycle on X1 is assumed.

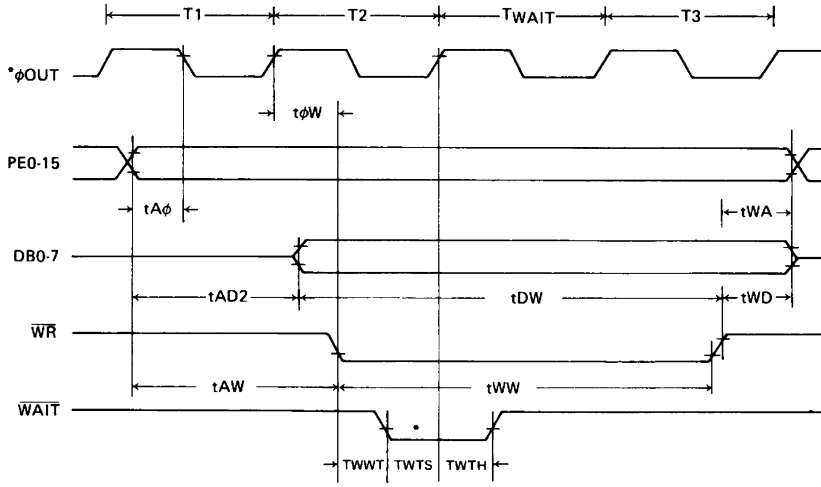
4. The items not included in this table are not dependent on $t_{CY\Phi}$

READ OPERATION



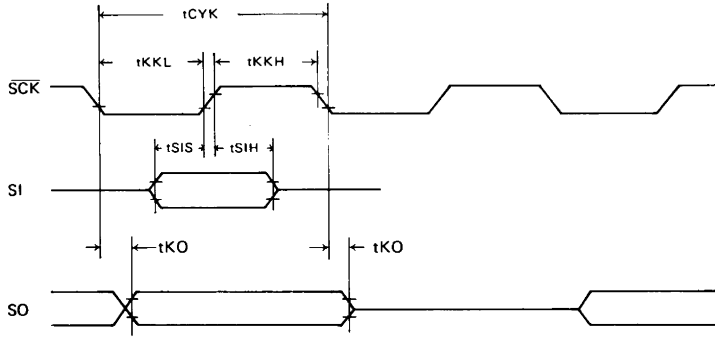
* WAIT signal must be remained stable during t_{WTS} and t_{WTH}.
If it is unstable, misoperation may occur.

WRITE OPERATION



* WAIT signal must be remained stable during t_{WTS} and t_{WTH}.
If it is unstable, misoperation may occur.

SERIAL OPERATION



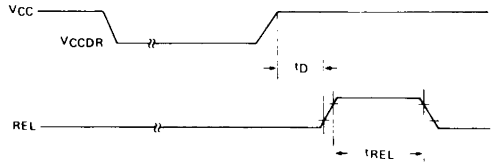
Low Power Data Memory Retention Characteristics for STOP Mode Operation

(T_a = −40 to +85°C)

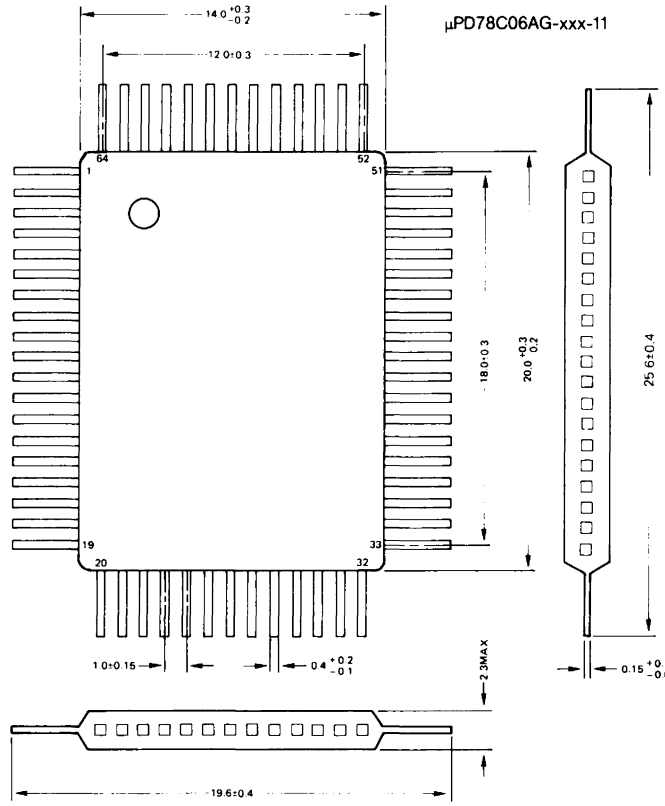
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{CCDR}		2.0			V
Data Retention Supply Current	I_{CCDR}	V_{CCDR} = 2.0V, X1 = 0V, X2 = Open		0.8	20	μA
Data Retention Input Low RES Voltage	V_{ILDR}		0		0.2 V_{CCDR}	V
Data Retention Input High $\overline{RESET}$ Voltage	V_{IHDR}		0.8 V_{CCDR}		V_{CCDR}	V
REL Input Delay Time	t_D		500			μs
REL Input High Time	t_{REL}		10			μs

Note: In data retention mode,

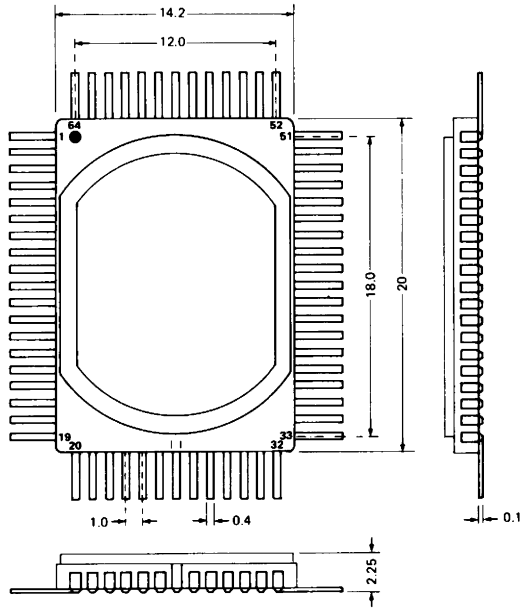
1) Input voltages to $\overline{WAIT}$ and PC_{0-5} pins (with pull-up resistors) should be maintained same as V_{CCDR} level,
2) Other input voltages should be kept less than V_{CCDR} level.

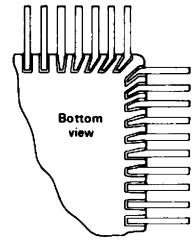


64-PIN PLASTIC FLAT PACKAGE OUTLINE, STRAIGHT LEADS (Unit : mm)
for μPD78C06AG



64-PIN CERAMIC FLAT PACKAGE OUTLINE FOR ES – REFERENCE – (Unit : mm)
for μPD78C06AG



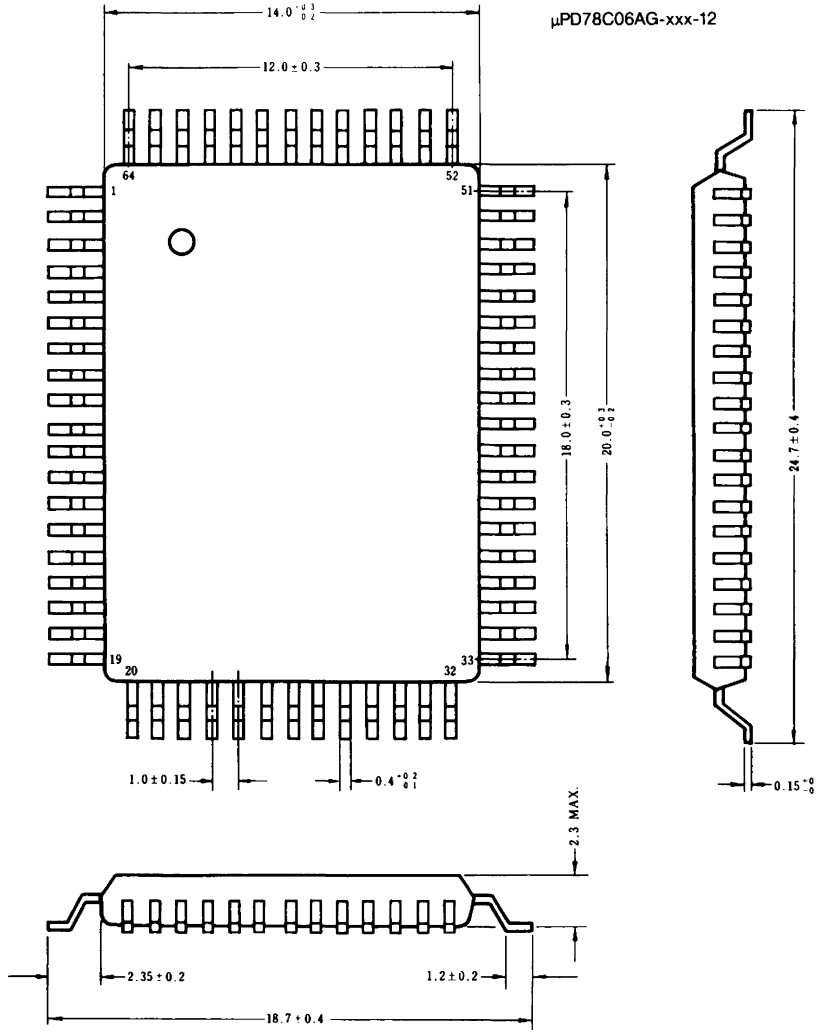


Note:

The metal cap of the device has V_{DD} (positive power supply) level because the metal cap is connected to pin No. 26 (i. e. V_{DD} pin).

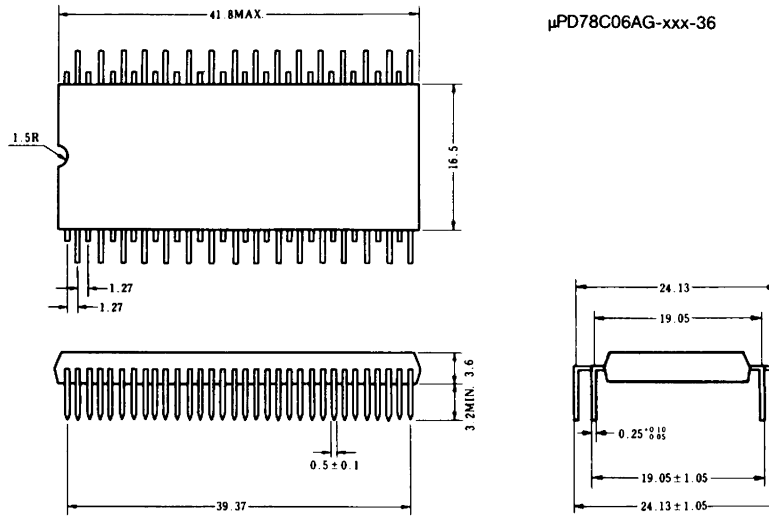
The leads of the welding part at bottom of this device are formed in slant and have a chance of shorting the other lines of printed wiring board.

64-PIN PLASTIC FLAT PACKAGE, BENT LEADS (Unit : mm)
for μPD78C06A

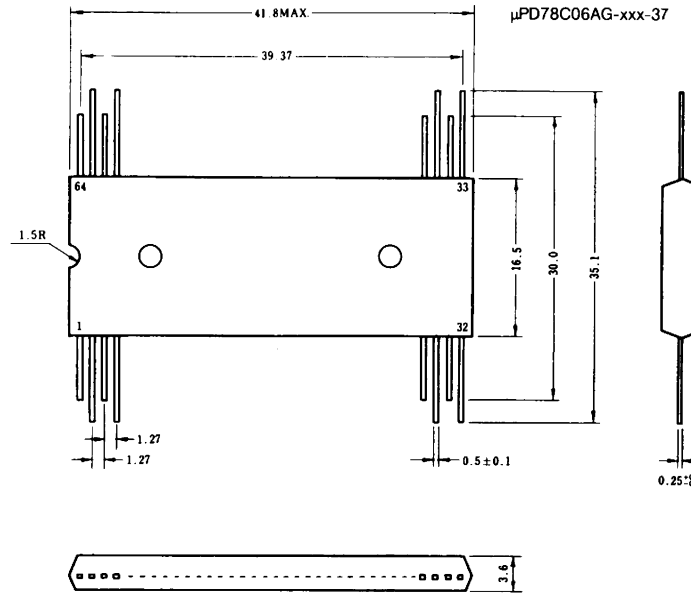


64-PIN PLASTIC QUAD-IN-LINE PACKAGE (QUIL), BENT LEADS
for μPD78C06A (Unit : mm)

μPD78C06AG-xxx-36



64-PIN PLASTIC QUAD-IN-LINE PACKAGE (QUIL) BENT LEADS (Unit : mm)
for μPD78C06AG



HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH COMPARATOR INPUTS, 8K ROM

DESCRIPTION

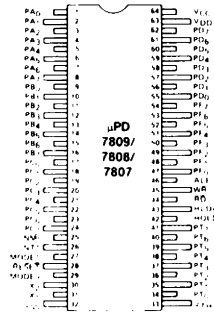
The μPD7809/7808/7807/78P09 single chip microcomputer augments the high-end in NEC's family of 8-bit microcomputers with sophisticated on-chip peripheral functionality. Like its nearest relative in the family, the μPD7811, this device has a fast internal 16-bit ALU and data paths, 256 bytes of RAM, multifunction 16-bit timer/event counter, two 8-bit timers, a USART, and two zero-cross detect inputs. Features that distinguish this device in the NEC 8-bit family are: 8K ROM, programmable threshold comparator (8 inputs), programmable WAIT function, watchdog timer, hold and hold acknowledge for DMA interface, and bit test/write instructions for both RAM and I/O.

The μPD7809 is the 8K Byte ROM version with the customers program on chip. The μPD7808 is a 4K Byte ROM version. The μPD7807 is the ROM-less version for prototyping and small volume applications. The μPD78P09 is an EPROM version of the 8K ROM μPD7809.

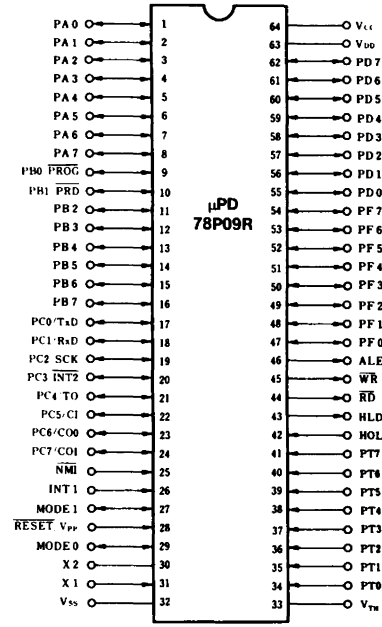
FEATURES

- NMOS silicon gate technology requiring + 5V supply
- Complete single chip microcomputer
  - 16-bit ALU
  - 8K ROM
  - 256 bytes RAM
- Large I/O capability
  - 40 I/O port lines (μPD7809/7808)
  - 24 I/O port lines (μPD7807)
  - 8 input lines
- Two zero-cross detect inputs
- Expansion capability (total of 64K memory access)
  - 8085A bus compatible
  - 56K bytes external memory address range
- Programmable threshold comparator
  - 8 inputs, 1 of 16 software selectable levels
- Full duplex USART
  - Synchronous, asynchronous and I/O mode
- 165 powerful instructions
  - 16-bit arithmetic, multiply and divide
- 1 μs instruction cycle time
- Prioritized interrupt structure
  - 3 external
  - 8 internal
- Hold, hold acknowledge for DMA interface
- Programmable WAIT function
- Watchdog timer
- Standby function
- On-chip clock generator
- 64-pin QUIL package/SDIP package

PIN CONFIGURATION



PIN CONFIGURATION μPD78P09R



PIN DESCRIPTION
μPD7809/08/07

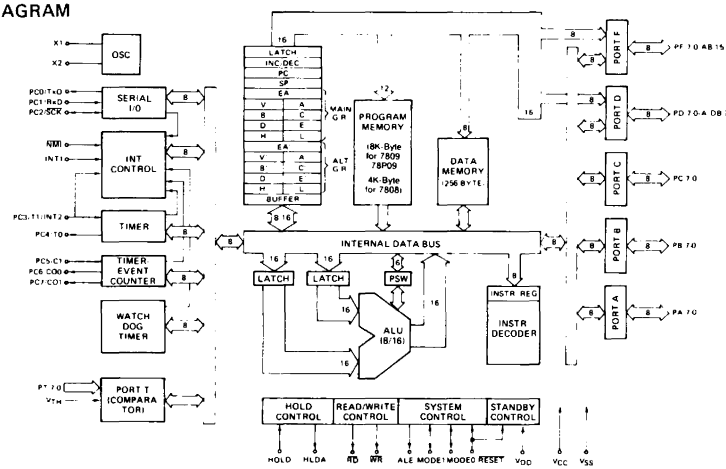
PIN NO.	PIN SYMBOL	FUNCTION	
1–8	PA_0–PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode.	
9–16	PB_0–PB_7	Port B: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port B in input mode.	
17	PC_0	Port C: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer counter and interrupt. Reset puts Port C in Port mode and all lines in input mode.	Transmit Data (TxD): Serial data output terminal.
18	PC_1		Receive Data (RxD): Serial data input terminal.
19	PC_2		Serial Clock (SCK): Serial clock input/output terminal. When internal clock is used, the output can be selected; when an external clock is used, the input can be selected.
20	PC_3		Timer Input ((TI)/interrupt request input (INT_2): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4		Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5		Counter Input (CI): External pulse input terminal to the timer/event counter.
23–24	PC_6, PC_7		Counter Outputs 0, 1 (CO_0–CO_1): Programmable rectangular wave output terminal based on timer/event counter.
25	NMI	Falling-edge, nonmaskable interrupt (NMI) input.	
26	INT_1	This signal is a rising-edge, maskable interrupt input. This input is also used to make the zero-cross detection AC input.	
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 Signal during each opcode fetch.	
28	RESET	(Input, active low), RESET initializes the μPD7809.	
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to output IO/M.	
30–31	X_2, X_1 (crystal)	This is a crystal connection terminal for system clock oscillation. When an external clock is supplied X_1 is the input.	
32	V_{SS}	Power supply ground potential.	
33	V_{TH}	V_{TH} threshold voltage input. Reference voltage for variable threshold input, Port T. Threshold voltage to each Port T input is software programmable to 16 different levels.	

PIN DESCRIPTION (cont.)

PIN NO.	PIN SYMBOL	FUNCTION
34–41	PT_1–PT_7	Eight variable threshold input ports. Ports T_0–T_7 inputs are each connected internally to comparators where the other input is the threshold voltage.
42	HOLD	HOLD request input. When high, CPU is in a HOLD state until HOLD goes low.
43	HLDA	HOLD Acknowledge output by CPU when HOLD state is accepted; goes low when HOLD is released.
44	RD	(Three-state output, active low) RD is used as a strobe to gate data from external devices onto the data bus. RD goes high during Reset.
45	WR	(Three-state output, active low) WR, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. WR goes high during Reset.
46	ALE	The strobe signal is for latching the address signal to the output from PD_7–PD_0 when accessing external expansion memory.
47–54	PF_0–PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55–62	PD_0–PD_7	Port D: 8-bit programmable I/O port. This byte can be designated as either input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	V_{DD}	This is a backup power terminal for on-chip RAM.
64	V_{CC}	+5V power supply.

Notes: 1 clock cycle = 1 CL = 3/f.
1 machine cycle = 3 or 4 clock cycles.
1 instruction cycle = 1 to 19 machine cycles.
f: System clock frequency (MHz).

BLOCK DIAGRAM



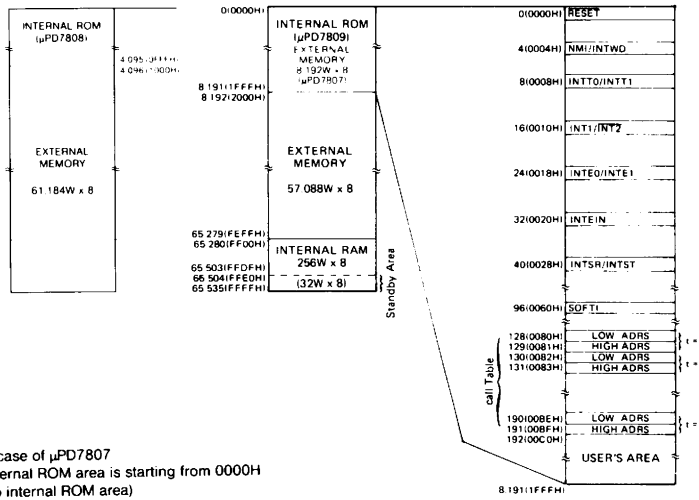
Note: The μPD7807 has no on chip ROM

INSTRUCTION SET

In addition to the basic 7800 family instruction set, the following instructions are incorporated in the μPD7809/7808/7807

- 16-bit data transfer between memory, registers, and extended accumulator
- 16-bit addition and subtraction
- 16-bit comparison and skip
- 16-bit and, or, ex-or operation
- 16-bit data shift and rotation
- Multiply
  8-bit by 8-bit, 16-bit product
  Less than 8 μs execution-time
- Divide
  16-bit by 8-bit, 16-bit quotient, 8-bit remainder
  Less than 14 μs execution-time
- Working register instructions for efficient RAM addressing, testing and manipulating
- Direct bit addressing for code-efficient addressing, testing and manipulating bits in RAM, port lines and mode registers

MEMORY MAP



In case of μPD7807
external ROM area is starting from 0000H
(no internal ROM area)

FUNCTIONAL DESCRIPTION

Please refer to the section of μPD7811 for description of the following functions which are the same as on this device:

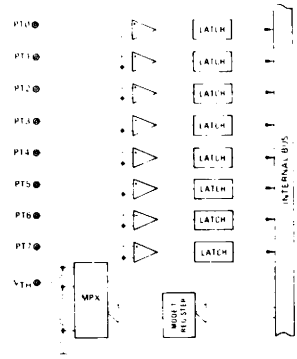
1. Memory expansion (except 56K bytes maximum for μPD7809)
2. USART
3. Reset
4. External memory access and timing

Variable Threshold Input Port (Port T)

- 8 input lines
- 16 levels – from 1/16 of reference voltage (V_{TH}) to 16/16 V_{TH}
- Level selected by software write to Mode T register
- Input at Port bit reads 0 until voltage at pin exceeds selected level
- Comparison execution time: 12 μs

FUNCTIONAL DESCRIPTION (CONT.)

Block Diagram of Treshold Variable Input Port



Format of MODE T Register

7	6	5	4	3	2	1	0
				MT3	MT2	MT1	MT0

Specification of 16 Threshold Levels

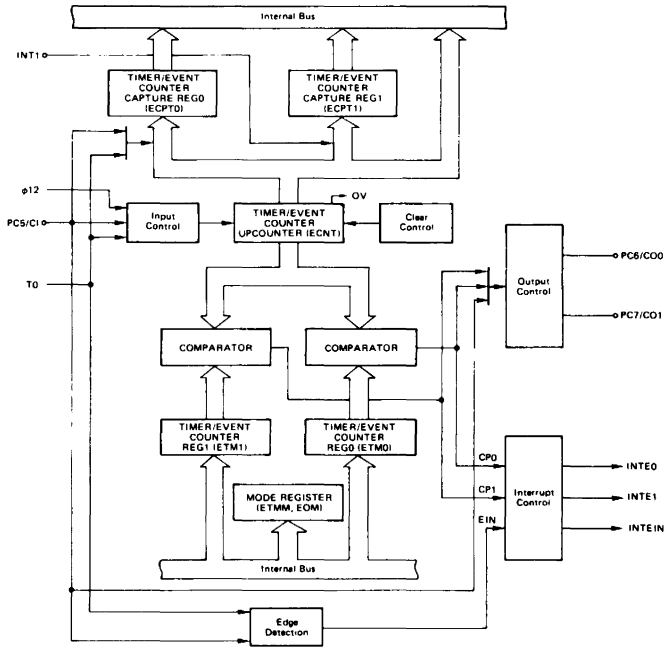
0	0	0	0	$V_{TH} \times 16/16$
0	0	0	1	$V_{TH} \times 1/16$
0	0	1	0	$V_{TH} \times 2/16$
0	0	1	1	$V_{TH} \times 3/16$
0	1	0	0	$V_{TH} \times 4/16$
0	1	0	1	$V_{TH} \times 5/16$
0	1	1	0	$V_{TH} \times 6/16$
0	1	1	1	$V_{TH} \times 7/16$
1	0	0	0	$V_{TH} \times 8/16$
1	0	0	1	$V_{TH} \times 9/16$
1	0	1	0	$V_{TH} \times 10/16$
1	0	1	1	$V_{TH} \times 11/16$
1	1	0	0	$V_{TH} \times 12/16$
1	1	0	1	$V_{TH} \times 13/16$
1	1	1	0	$V_{TH} \times 14/16$
1	1	1	1	$V_{TH} \times 15/16$

Input/Output

- 40 digital I/O lines – Five 8-bit ports (Port A, Port B, Port C, Port D, Port F)
- Port operation for Ports A, B, C and F: Each line of these ports can be individually programmed as an input or as an output
- Port D can be programmed as a byte input or a byte output
- Control lines: Under software control, each line of Port C can be configured individually to provide control lines for serial interface timer and timer/counter and interrupt.

FUNCTIONAL DESCRIPTION (CONT.)

TIMER / EVENT COUNTER – BLOCK DIAGRAM



Note: $\phi 12 = f_{XTAL} \times 1/12$,

f_{XTAL} : oscillation frequency

Input Clock of TIMER/EVENT COUNTER: Internal (φ12)
External (CI)
Timer out (TO)

Operations:

a) Interval Timer:
Counter repeats interruptions due to a present count time.

b) Event Count Mode:
CI inputs are synchr. by the internal clock. 250ns noise detection.

c) Frequency Measurement Mode:
CI inputs while TO is kept at high level.

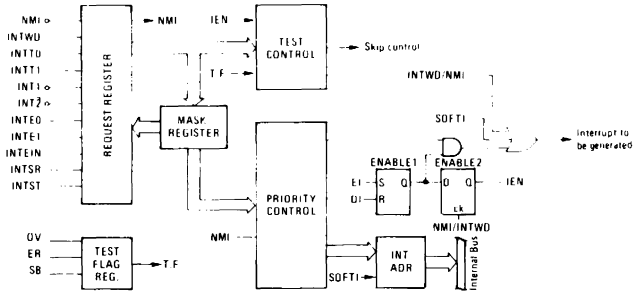
d) Puls with Meaurement Mode:
Counting up the upcounter during CI is high or low.

e) Programmable Square Wave:
Comperator 0 signal sets $CO_{0/1}$. Comperator 1 signal reset $CO_{0/1}$.

f) Single Pulse Generation:
CI is trigger input 16 bit counter free running output Flip-Flop toggled two times.

FUNCTIONAL DESCRIPTION (CONT.)

INTERRUPT CONTROL CIRCUITRY – BLOCK DIAGRAM



Mask register: Masking the interrupts

Priority control: Accepts only the interrupt with the highest priority if more than one request at the same time.

Test Flag register: 3 kinds of test flags which doesn't bring any interrupt request:

OV: set to 1 by overflow of the timer/event counter
ER: set to 1 by priority error
SB: set to 1 by rise input of V_{DD} terminal

INTERRUPT

11 Interrupt Sources

3 External Interrupts – Including non maskable interrupt
8 Internal Interrupts

6 Priority Levels and 6 Interrupt Vectors

11 Interrupt sources are divided into 6 priority levels.

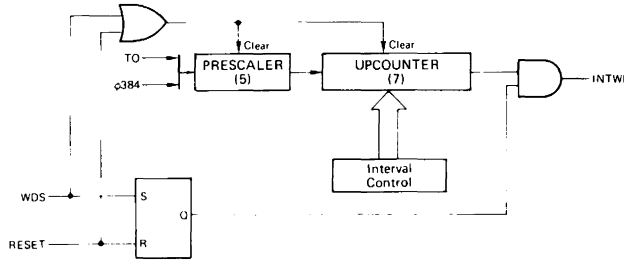
PRIORITY	INTERRUPT ADDRESS	INTERRUPT SOURCE		INTERNAL/ EXTERNAL
1	4 (0004H)	$\overline{\text{NMI}}$	falling edge	external
		INTWD	output signal of watchdog timer	internal
2	8 (0008H)	INTT0	coincidence signal from TIMER0	internal
		INTT1	coincidence signal from TIMER1	
3	16 (0010H)	INT1	rising edge	external
		$\overline{\text{INT2}}$	falling edge	
4	24 (0018H)	INTE0	coincidence signal from timer/ event counter	internal
		INTE1	coincidence signal from timer/ event counter	
5	32 (0020H)	INTEIN	falling edge of CI or TO	internal
6	40 (0028H)	INTSR	serial receive interrupt	internal
		INTST	serial transmit interrupt	

FUNCTIONAL DESCRIPTION (CONT.)

WATCHDOG TIMER

Used for software safety check or overall performance safety check. Watchdog, if enabled, must be cleared at regular intervals in program execution to avoid watchdog interrupt or by Reset. Intervals are software selectable.

BLOCK DIAGRAM OF WATCHDOG TIMER



Note: $\phi 384 \quad f_{XTAL} \times 1\ 384$

HOLD/HLDA

To perform all sorts of DMA-applications a Hold-request signal can be applied to the μPD7809; it puts Address- and Databus and RD/WR signal lines to the high impedance state. Then HLDA goes high as a response to the hold request.

MODE0/MODE1-TERMINALS

The logic level applied to M0/M1-Terminals determines the memory map of μPD7807/08/09 and the use of Port D/F as multiplexed Address/Data Bus.

M0	M1	MEMORY	ADDRESSES	LOCATION
0	1	8K/4K	0 . . . . . 0FFFH/1FFFH	internal*
0	0	4K	0 . . . . . .OFFFH	external
0	1	16K	0 . . . . . 3FFFH	external
1	0	64K	0 . . . . . FEFFH	external

* M0, M1 = 0,1 realizes the ROM version (access of internal ROM), all others represent access of external memory only In case external memory is used in addition to internal, memory mapping register has to be programmed then (see below)

MEMORY EXPANDES MODES	MEMORY MAPPING REGISTER MM2	MM1	MM0	NUMBER OF I/O LINES
Port Mode	0	0	X	44
256 Expanded	0	1	0	36
4K Expanded	1	0	0	32
16K Expanded	1	1	0	30
56K/60K* Expanded	1	1	1	28

*56K for 7809, 60K for 7808

FUNCTIONAL DESCRIPTIONS (CONT.)

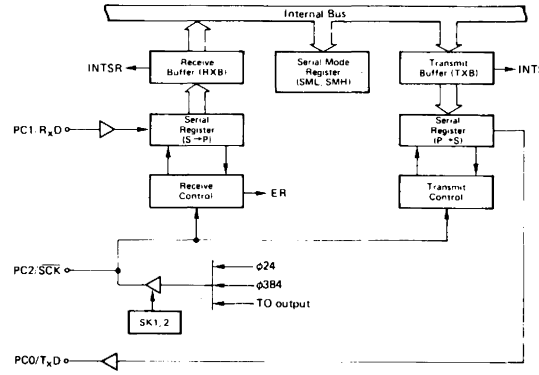
STANDBY FUNCTION

The μPD7809/08/07/P09 offers a standby function that allows the user to save up to 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On powerup the μPD7809 checks whether recovery was made from standby mode or from cold start.

UNIVERSAL SERIAL INTERFACE

The serial interface can operate in any of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first for ease of communication with certain peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception. In the search mode, data is transferred one bit at a time from serial register to receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from serial register to transmit buffer occurs 8 bits at a time.

UNIVERSIAL SERIAL INTERFACE BLOCK DIAGRAM



Note: $\phi 24 = f_{XTAL} \times 1/24$

$\phi 384 = f_{XTAL} \times 1/384$ f_{XTAL}: oscillation frequency (MHz)

- Asynchronous Mode
  - Full-Duplex, Double Buffering
  - 7, 8-Bit/Character
  - Start/Stop Bit
  - Even/Odd Parity
  - Programmable Clock Rate X1, X16, X64
- Synchronous Mode
  - Search/Receive Mode
- I/O Interface Mode (μPD7801 Serial Mode)
- Programmable Communication Rate
  - 2μsec, 32μsec, Timer and External

FUNCTIONAL DESCRIPTION (CONT.)

ZERO-CROSSING DETECTOR

The INT1 and INT2 terminals (used common to TI and PC_3) can be used to detect the zero-crossing point of slow moving AC signals. When driven directly, these pins respond as a normal digital input.

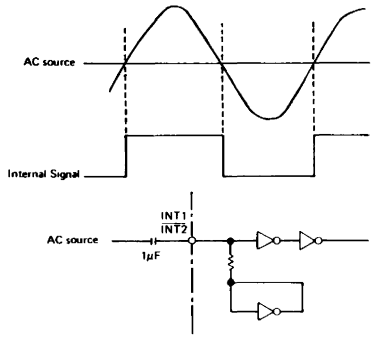
To utilize the zero-cross detection mode, an AC signal of approximately 1–3V AC peak-to-peak magnitude and a maximum frequency of 1kHz is coupled through an external capacitor to these pins.

For the INT1 pin, the internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one and INT1 interrupt is generated.

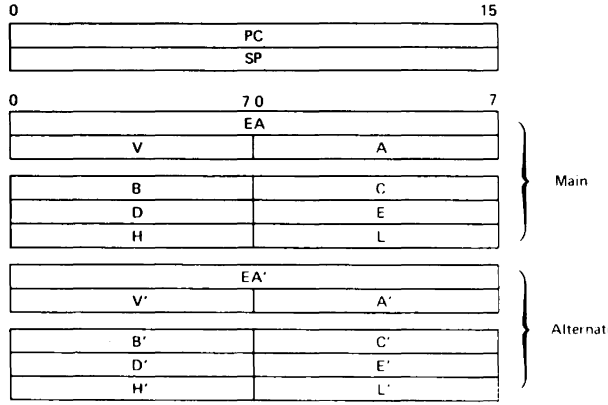
For the INT2 pin, the state is sensed as a one until the falling edge crosses the DC average level, when it becomes a zero and INT2 interrupt is generated.

The zero-cross detection capability allows the user to make the 50–60Hz power signal the basis for system timing and to control voltage phase sensitive devices.

ZERO-CROSSING DETECTION CIRCUIT



REGISTERS



FUNCTIONAL DESCRIPTION (CONT.)

General Purpose Registers (B, C, D, E, H, L)

There are two sets of general purpose registers (Main: B, C, D, E, H, L: Alternate: B', C', D', H', L'). They can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL, B'C', D'E', H'L'). Auto Increment and Decrement addressing mode capabilities extend the uses for the DE, HL, D'E', and H'L' register-pairs. The contents of the BC, DE, and HL register-pairs can be exchanged with their Alternate Register counterparts using the EXX instruction.

Vector Register (V)

When defining a scratch pad area in the memory space, the upper 8-bit memory address is defined in the V-register and the lower 8-bits is defined by the immediate data of an instruction. Also the scratch pad indicated by the V-register can be used as 256 x 8-bit working registers for storing software flags, parameters and counters.

Accumulator (A)

All data transfers between the μPD7809 and external memory of I/O are done through the accumulator. The contents of the Accumulator and Vector Registers can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A reset sets the PC to 0000_H.

Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

Extended Accumulator (EA)

The data processings of 16-bit arithmetic and logical operation instructions are mainly handled in the extended accumulator.

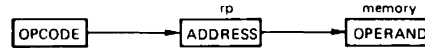
ADDRESS MODES

Register Addressing	Working Register Addressing
Register Indirect Addressing	Direct Addressing
Auto-Increment Addressing	Immediate Addressing
Auto-Decrement Addressing	Immediate Extended Addressing
Double Auto-Increment Addressing	Base Addressing
Relative Addressing	Base-Index-Addressing

Register Addressing

The instruction opcode specifies a register r which contains the operand.

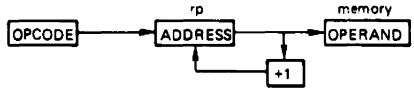
Register Indirect Addressing



The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

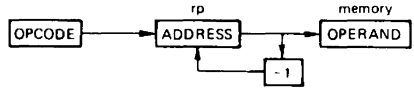
FUNCTIONAL DESCRIPTION (CONT.)

Auto-Increment Addressing

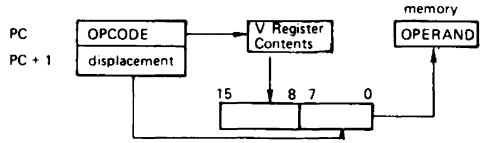


The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

Auto Decrement Addressing

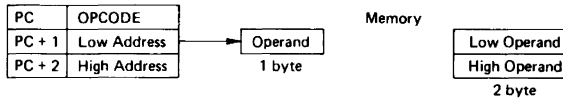


Working Register Addressing



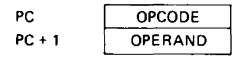
The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix ending this address mode.

Direct Addressing

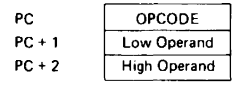


The two bytes following the opcode specify an address of a location containing the operand.

Immediate Addressing

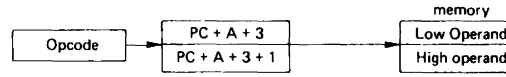


Immediate Extended Addressing



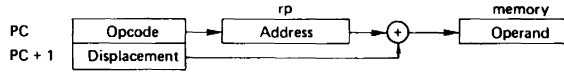
FUNCTIONAL DESCRIPTIONS (CONT.)

Relative Addressing



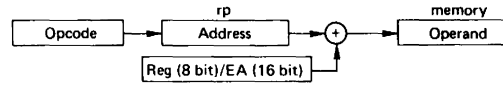
This addressing mode is used by the "Table"-command. It transfers the contents of 2 memory cells – addressed relatively to PC via the Accu A – into BC register-pair (TABLE-command). Application: Table look-up

Base-Addressing



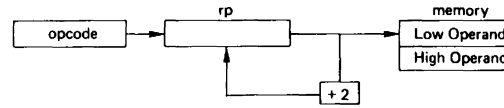
Register Pair DE or HL used as base pointer to the memory; immediate data (8 bit) or displacement added to the base.

Base-Index-Addressing



Register pair DE or HL used as base pointers to the memory; Register (8 bit) or Extended Accumulator (EA) as displacement added to the base.

Double auto increment



The opcode specifies the register pair which contains the memory address of the operand (16-bit). The contents of the register pair is automatically incremented by two to point to a new 16-bit operand.

FUNCTIONAL DESCRIPTION (CONT.)

BIT ADDRESS INSTRUCTIONS

The following bits may be addressed directly with certain instructions:

- Any bit in a 16-byte group in RAM
- Any bit in the five 8-bit I/O ports (A, B, C, D, F)
- Any bit in the variable threshold port
- Any bit in the following special registers:

  9-bit interrupt mask register, serial mode register, timer mode register, timer/event counter output register

An addressed bit may be tested, set, cleared, or complemented.
An addressed bit may be moved to or from the carry flag.
An addressed bit may be ANDed, ORed, X-ORed with the carry flag.

Difference between the μPD7801, μPD7811, μPD7807, and μPD7809

		μPD7801	μPD7811	μPD7807	μPD7809
Number of Instructions		134	158	165	165
16-Bit Operation Instruction		No	Yes	Yes	Yes
Multipy/Divide Instruction		No	Yes	Yes	Yes
Instruction Cycle		2μs/4MHz	1μs/12MHz	1μs/12MHz	1μs/12MHz
Number of General-purpose Registers		16	16	16	16
On-chip ROM Capacity		4K Bytes	4K Bytes	No	8K Bytes
On-chip RAM Capacity		128 Bytes	256 Bytes	256 Bytes	256 Bytes
Direct-Addressable External Memory Capacity		60K Bytes	60K Bytes	64K Bytes	56K Bytes
Interrupt Source	Internal	2	8	8	8
	External	3	3	3	3
I/O Lines		48	40+4	28*	40
Threshold Variable Port		No	No	8 Bits	8 Bits
Timer/Counter	Timer	12 Bits	8 Bits x 2	8 Bits x 2	8 Bits x 2
	Counter	No	16 Bits	16 Bits	16 Bits
Watchdog Timer		No	No	Yes	Yes
Serial Interface	Asynchronous	No	Yes	Yes	Yes
	Synchronous	No	Yes	Yes	Yes
	I/O Interface	Yes	Yes	Yes	Yes
A/D Converter		No	Yes	No	No
Standby Function		No	Yes	Yes	Yes
Hold Function		Yes	no	Yes	Yes
Technology		NMOS	NMOS	NMOS	NMOS
Package		64-Pin QUIP	64-Pin QUIP	64-Pin QUIP	64-Pin QUIP

* at 4K-byte Access

OPERAND FORMAT/DESCRIPTION

FORMAT	DESCRIPTION
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, PD, PF, MKH, MKL, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TXB, TM0, TM1, WDM, MT
sr1	PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM, PT, RXB, WDM
sr2	PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM
sr3	ETM0, ETM1
sr4	ECNT, ECPT0, ECPT1
sr5	PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM, PT
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
rpa	B, D, H, D+, H+, D-, H-
rpa1	B, D, H
rpa2	B, D, H, D+, H+, D-, H-, D+byte, H+A, H+B, H+EA, H+byte
rpa3	D, H, D++, H++, D+byte, H+A, H+B, H+EA, H+byte
wa	8 bit immediate data
word	16 bit immediate data
byte	8 bit immediate data
bit	8 bit immediate data
f	CY, HC, Z
irf	FNMI, FT0, FT1, F1, F2, FE0, FE1, FEIN, FSR, FST, ER, OV, IFE2, SB

REMARKS

1. sr ~ sr5 (special register)

PA	:	PORT A
PB	:	PORT B
PC	:	PORT C
PD	:	PORT D
PF	:	PORT F
PT	:	PORT T
MA	:	MODE A
MB	:	MODE B
MC	:	MODE C
MCC	:	MODE CONTROL C
MF	:	MODE F
MM	:	MEMORY MAPPING
MT	:	MODE T
TM0	:	TIMER REG0
TM1	:	TIMER REG1
TMM	:	TIMER MODE
ETM0	:	TIMER/EVENT COUNTER REG0
ETM1	:	TIMER/EVENT COUNTER REG1
ECNT	:	TIMER/EVENT COUNTER UPCOUNTER
ECPT0	:	TIMER/EVENT COUNTER CAPTURE0
ECPT1	:	TIMER/EVENT COUNTER CAPTURE1
ETMM	:	TIMER/EVENT COUNTER MODE
EOM	:	TIMER/EVENT COUNTER OUTPUT MODE
WDM	:	WATCHDOG TIMER MODE
TXB	:	Tx BUFFER
RXB	:	Rx BUFFER
SMH	:	SERIAL MODE High
SML	:	SERIAL MODE Low
MKH	:	MASK High
MKL	:	MASK Low

2. rp ~ rp3 (register pair)

SP	:	STACK POINTER
B	:	BC
D	:	DE
H	:	HL
V	:	VA
EA	:	EXTENDED ACCUMULATOR

3. rpa ~ rpa3 (rp addressing)

B	:	(BC)
D	:	(DE)
H	:	(HL)
D+	:	(DE)+
H+	:	(HL)+
D−	:	(DE)−
H−	:	(HL)−
D++	:	(DE)++
H++	:	(HL)++
D+byte	:	(DE+byte)
H+A	:	(HL+A)
H+B	:	(HL+B)
H+EA	:	(HL+EA)
H+byte	:	(HL+byte)

4. f (flag)

CY	:	CARRY
HC	:	HALF CARRY
Z	:	ZERO

5. irf (interrupt flag)

FMMI	:	INTFNMI
FT0	:	INTFT0
FT1	:	INTFT1
F1	:	INTF1
F2	:	INTF2
FE0	:	INTFE0
FE1	:	INTFE1
FEIN	:	INTFEIN
FSR	:	INTFSR
FST	:	INTFST
ER	:	ERROR
OV	:	OVERFLOW
IEF2	:	INTERRUPT ENABLE F/F2
SB	:	STANDBY

Parts of this material may be changed without prior notice due to the introduction of new functions of products under development.

INSTRUCTION SET

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
8-BIT DATA TRANSFER			r1, A	0 0 0 1 1 T_2 T_1 T_0				4	r1 ← A	
			A, r1	0 0 0 0 1 T_2 T_1 T_0				4	A ← r1	
		*	sr, A	0 1 0 0 1 1 0 1	1 1 S_5 S_4 S_3 S_2 S_1 S_0			10	sr ← A	
		*	A, sr1	0 1 0 0 1 1 0 0	1 1 S_5 S_4 S_3 S_2 S_1 S_0			10	A ← sr1	
	MOV		r, word	0 1 1 1 0 0 0 0	0 1 1 0 1 R_2 R_1 R_0	Low Adrs	High Adrs	17	r ← (word)	
			word, r	0 1 1 1 0 0 0 0	0 1 1 1 1 R_2 R_1 R_0	Low Adrs	High Adrs	17	(word) ← r	
		*	r, byte	0 1 1 0 1 R_2 R_1 R_0	Data			7	r ← byte	
	MVI		sr2, byte	0 1 1 0 0 1 0 0	S_3 0 0 0 0 S_2 S_1 S_0	Data		14	sr2 ← byte	
	MVIW	*	wa, byte	0 1 1 1 0 0 0 1	Offset	Data		13	(V.wa) ← byte	
	MVIX	*	rpa1, byte	0 1 0 0 1 0 A_1 A_0	Data			10	(rpa1) ← byte	
	STAW	*	wa	0 1 1 0 0 0 1 1	Offset			10	(V.wa) ← A	
	LDAW	*	wa	0 0 0 0 0 0 0 1	Offset			10	A ← (V.wa)	
	STAX	*	rpa2	A_3 0 1 1 1 A_2 A_1 A_0	Data (*1)			7/13	(rpa2) ← A	
	LDAX	*	rpa2	A_3 0 1 0 1 A_2 A_1 A_0	Data (*1)			7/13	A ← (rpa2)	
	EXX			0 1 0 0 1 0 0 0	1 0 1 0 1 1 1 1			8	B ↔ B', C ↔ C', D ↔ D', E ↔ E', H ↔ H', L ↔ L'	
	EXA			0 1 0 0 1 0 0 0	1 0 1 0 1 1 0 0			8	V, A ↔ V', A', EA ↔ EA'	
	EXH			0 1 0 0 1 0 0 0	1 0 1 0 1 1 1 0			8	H, L ↔ H', L'	
	EXR			0 1 0 0 1 0 0 0	1 0 1 0 1 1 0 1			8	V ↔ V', A ↔ A', B ↔ B', C ↔ C', D ↔ D', E ↔ E', H ↔ H', L ↔ L', EA ↔ EA'	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
16-BIT DATA TRANSFER	BLOCK		D+	0 0 0 1 0 0 0 0				13* (C+1)	(DE)+ ← (HL)+, C ← C−1 End if borrow	
			D−	0 0 0 1 0 0 0 1				13* (C+1)	(DE)− ← (HL)−, C ← C−1 End if borrow	
	DMOV		rp3, EA	1 0 1 1 0 1 P_1 P_0				4	$rp3_L$ ← EAL, $rp3_H$ ← EAH	
			EA, rp3	1 0 1 0 0 1 P_1 P_0				4	EAL ← $rp3_L$, EAH ← $rp3_H$	
			sr3, EA	0 1 0 0 1 0 0 0	1 1 0 1 0 0 1 U_0			14	sr3 ← EA	
			EA, sr4	↓ ↓ ↓ ↓	1 1 0 0 0 0 V_1 V_0			14	EA ← sr4	
	SBCD		word	0 1 1 1 0 0 0 0	0 0 0 1 1 1 1 0	Low Adrs	High Adrs	20	(word) ← C, (word+1) ← B	
	SDED		word	↓ ↓ ↓ ↓	0 0 1 0 1 1 1 0	↓ ↓	↓ ↓	20	(word) ← E, (word+1) ← D	
	SHLD		word	↓ ↓ ↓ ↓	0 0 1 1 1 1 1 0	↓ ↓	↓ ↓	20	(word) ← L, (word+1) ← H	
	SSPD		word	↓ ↓ ↓ ↓	0 0 0 0 1 1 1 0	↓ ↓	↓ ↓	20	(word) ← SP_L, (word+1) ← SP_H	
	STEAX		rpa3	0 1 0 0 1 0 0 0	1 0 0 1 C_3 C_2 C_1 C_0	Data (*2)		14/20	(rpa3) ← EAL, (rpa3+1) ← EAH	
	LBCD		word	0 1 1 1 0 0 0 0	0 0 0 1 1 1 1 1	Low Adrs	High Adrs	20	C ← (word), B ← (word+1)	
	LDED		word	↓ ↓ ↓ ↓	0 0 1 0 1 1 1 1	↓ ↓	↓ ↓	20	E ← (word), D ← (word+1)	
	LHLD		word	↓ ↓ ↓ ↓	0 0 1 1 1 1 1 1	↓ ↓	↓ ↓	20	L ← (word), H ← (word+1)	
	LSPD		word	↓ ↓ ↓ ↓	0 0 0 0 1 1 1 1	↓ ↓	↓ ↓	20	SP_L ← (word), SP_H ← (word+1)	
	LDEAX		rpa3	0 1 0 0 1 0 0 0	1 0 0 0 C_3 C_2 C_1 C_0	Data (*2)		14/20	EAL ← (rpa3), EAH ← (rpa3+1)	
	PUSH		rp1	1 0 1 1 0 Q_2 Q_1 Q_0				13	(SP−1) ← $rp1_H$, (SP−2) ← $rp1_L$ SP ← SP−2	
	POP		rp1	1 0 1 0 0 Q_2 Q_1 Q_0				10	$rp1_L$ ← (SP), $rp1_H$ ← (SP+1) SP ← SP+2	
	LXI	*	rp2, word	0 P_2 P_1 P_0 0 1 0 0	Low Byte	High Byte		10	rp2 ← word	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
8-BIT ARITHMETIC (REGISTER)	TABLE		01001000	10101000			17	C ← (PC+3+A) B ← (PC+3+A+1)	
	ADD	A, r	01100000	11000 R_2 R_1 R_0			8	A ← A+r	
		r, A		01000 R_2 R_1 R_0			8	r ← r+A	
	ADC	A, r		11010 R_2 R_1 R_0			8	A ← A+r+CY	
		r, A		01010 R_2 R_1 R_0			8	r ← r+A+CY	
	ADDNC	A, r		10100 R_2 R_1 R_0			8	A ← A+r	No Carry
		r, A		00100 R_2 R_1 R_0			8	r ← r+A	No Carry
	SUB	A, r		11100 R_2 R_1 R_0			8	A ← A−r	
		r, A		01100 R_2 R_1 R_0			8	r ← r−A	
	SBB	A, r		11110 R_2 R_1 R_0			8	A ← A−r−CY	
		r, A		01110 R_2 R_1 R_0			8	r ← r−A−CY	
	SUBNB	A, r		10110 R_2 R_1 R_0			8	A ← A−r	No Borrow
		r, A		00110 R_2 R_1 R_0			8	r ← r−A	No Borrow
	ANA	A, r		10001 R_2 R_1 R_0			8	A ← A ∧ r	
		r, A		00001 R_2 R_1 R_0			8	r ← r ∧ A	
	ORA	A, r		10011 R_2 R_1 R_0			8	A ← A ∨ r	
		r, A		00011 R_2 R_1 R_0			8	r ← r ∨ A	
	XRA	A, r		10010 R_2 R_1 R_0			8	A ← A ∨ r	
		r, A		00010 R_2 R_1 R_0			8	r ← r ∨ A	
	GTA	A, r		10101 R_2 R_1 R_0			8	A−r−1	No Borrow
		r, A		00101 R_2 R_1 R_0			8	r−A−1	No Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
8-BIT ARITHMETIC (REG.)	LTA	A, r	01100000	10111 R_2 R_1 R_0			8	A−r	Borrow
		r, A		00111 R_2 R_1 R_0			8	r−A	Borrow
	NEA	A, r		11101 R_2 R_1 R_0			8	A−r	No Zero
		r, A		01101 R_2 R_1 R_0			8	r−A	No Zero
	EQA	A, r		11111 R_2 R_1 R_0			8	A−r	Zero
		r, A		01111 R_2 R_1 R_0			8	r−A	Zero
	ONA	A, r		11001 R_2 R_1 R_0			8	A ∧ r	No Zero
	OFFA	A, r		11011 R_2 R_1 R_0			8	A ∧ r	Zero
8-BIT ARITHMETIC (MEMORY)	ADDX	rpa	01110000	11000 A_2 A_1 A_0			11	A ← A+ (rpa)	
	ADCX	rpa		11010 A_2 A_1 A_0			11	A ← A+ (rpa)+CY	
	ADDNCX	rpa		10100 A_2 A_1 A_0			11	A ← A+ (rpa)	No Carry
	SUBX	rpa		11100 A_2 A_1 A_0			11	A ← A− (rpa)	
	SBBX	rpa		11110 A_2 A_1 A_0			11	A ← A− (rpa)−CY	
	SUBNBX	rpa		10110 A_2 A_1 A_0			11	A ← A− (rpa)	No Borrow
	ANAX	rpa		10001 A_2 A_1 A_0			11	A ← A ∧ (rpa)	
	ORAX	rpa		10011 A_2 A_1 A_0			11	A ← A ∨ (rpa)	
	XRAX	rpa		10010 A_2 A_1 A_0			11	A ← A ∨ (rpa)	
	GTAX	rpa		10101 A_2 A_1 A_0			11	A− (rpa)−1	No Borrow
	LTAX	rpa		10111 A_2 A_1 A_0			11	A− (rpa)	Borrow

	MNEMONIC	OPERAND	OP CODE B1	B2	B3	B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	NEAX	rpa	01110000	11101 A_2 A_1 A_0			11	A– (rpa)	No Zero
	EQAX	rpa		11111 A_2 A_1 A_0			11	A– (rpa)	Zero
	ONAX	rpa		11001 A_2 A_1 A_0			11	A ∧ (rpa)	No Zero
	OFFAX	rpa	↓ ↓	11011 A_2 A_1 A_0			11	A ∧ (rpa)	Zero
	ADI *	A, byte	01000110	← Data →			7	A ← A+byte	
		r, byte	01110100	01000 R_2 R_1 R_0	Data		11	r ← r+byte	
		sr2, byte	01100100	S_3 1000 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	
	ACI *	A, byte	01010110	← Data →			7	A ← A+byte+CY	
		r, byte	01110100	01010 R_2 R_1 R_0	Data		11	r ← r+byte+CY	
		sr2, byte	01100100	S_3 1010 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte+CY	
	ADINC *	A, byte	00100110	← Data →			7	A ← A+byte	No Carry
		r, byte	01110100	00100 R_2 R_1 R_0	Data		11	r ← r+byte	No Carry
		sr2, byte	01100100	S_3 0100 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	No Carry
	SUI *	A, byte	01100110	← Data →			7	A ← A–byte	
		r, byte	01110100	01100 R_2 R_1 R_0	Data		11	r ← r–byte	
		sr2, byte	01100100	S_3 1100 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte	
	SBI *	A, byte	01110110	← Data →			7	A ← A–byte–CY	
		r, byte	01110100	01110 R_2 R_1 R_0	Data		11	r ← r–byte–CY	
		sr2, byte	01100100	S_3 1110 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte–CY	

	MNEMONIC	OPERAND	OP CODE B1	B2	B3	B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	SUINB *	A, byte	00110110	← Data →			7	A ← A–byte	No Borrow
		r, byte	01110100	00110 R_2 R_1 R_0	Data		11	r ← r–byte	No Borrow
		sr2, byte	0110 ↓	S_3 0110 S_2 S_1 S_0	↓		20	sr2 ← sr2–byte	No Borrow
	ANI *	A, byte	00000111	← Data →			7	A ← A ∧ byte	
		r, byte	01110100	00001 R_2 R_1 R_0	Data		11	r ← r ∧ byte	
		sr2, byte	01100100	S_3 0001 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∧ byte	
	ORI *	A, byte	00010111	← Data →			7	A ← A ∨ byte	
		r, byte	01110100	00011 R_2 R_1 R_0	Data		11	r ← r ∨ byte	
		sr2, byte	0110 ↓	S_3 0011 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨ byte	
	XRI *	A, byte	00010110	← Data →			7	A ← A ∨̄ byte	
		r, byte	01110100	00010 R_2 R_1 R_0	Data		11	r ← r ∨̄ byte	
		sr2, byte	0110 ↓	S_3 0010 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨̄ byte	
	GTI *	A, byte	00100111	← Data →			7	A–byte–1	No Borrow
		r, byte	01110100	00101 R_2 R_1 R_0	Data		11	r–byte–1	No Borrow
		sr5, byte	0110 ↓	S_3 0101 S_2 S_1 S_0	↓		14	sr5–byte–1	No Borrow
	LTI *	A, byte	00110111	← Data →			7	A–byte	Borrow
		r, byte	01110100	00111 R_2 R_1 R_0	Data		11	r–byte	Borrow
		sr5, byte	0110 ↓	S_3 0111 S_2 S_1 S_0	↓		14	sr5–byte	Borrow

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	NEI	*	A, byte	01100111	← Data →			7	A – byte	No Zero
			r, byte	01110100	01101 R_2 R_1 R_0	Data		11	r – byte	No Zero
			sr5, byte	0110 ↓	S_3 1101 S_2 S_1 S_0	↓		14	sr5 – byte	No Zero
	EQI	*	A, byte	01110111	← Data →			7	A – byte	Zero
			r, byte	01110100	01111 R_2 R_1 R_0	Data		11	r byte	Zero
			sr5, byte	0110 ↓	S_3 1111 S_2 S_1 S_0	↓		14	sr5 – byte	Zero
	ONI	*	A, byte	01000111	← Data →			7	A ∧ byte	No Zero
			r, byte	01110100	01001 R_2 R_1 R_0	Data		11	r ∧ byte	No Zero
			sr5, byte	0110 ↓	S_3 1001 S_2 S_1 S_0	↓		14	sr5 ∧ byte	No Zero
	OFFI	*	A, byte	01010111	← Data →			7	A ∧ byte	Zero
			r, byte	01110100	01011 R_2 R_1 R_0	Data		11	r ∧ byte	Zero
			sr5, byte	0110 ↓	S_3 1011 S_2 S_1 S_0	↓		14	sr5 ∧ byte	Zero
WORKING REGISTER	ADDW		wa	01110100	11000000	Offset		14	A ← A+(V.wa)	
	ADCW		wa	↓ ↓	1101	↓		14	A ← A+(V.wa)+CY	
	ADDNCW		wa	↓ ↓	1010	↓		14	A ← A+(V.wa)	No Carry
	SUBW		wa	↓ ↓	1110	↓		14	A ← A–(V.wa)	
	SBBW		wa	↓ ↓	1111	↓		14	A ← A–(V.wa)–CY	
	SUBNBW		wa	↓ ↓	1011	↓		14	A ← A–(V.wa)	No Borrow
	ANAW		wa	↓ ↓	10001000	↓		14	A ← A ∧ (V.wa)	
	ORAW		wa	↓ ↓	1001	↓		14	A ← A ∨ (V.wa)	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
WORKING REGISTER	XRAM		wa	01110100	10010000	Offset		14	A ← A ∨ (V.wa)	
	GTAW		wa	↓ ↓	10101000	↓		14	A–(V.wa)–1	No Borrow
	LTAW		wa	↓ ↓	1011	↓		14	A–(V.wa)	Borrow
	NEAW		wa	↓ ↓	1110	↓		14	A–(V.wa)	No Zero
	EQAW		wa	↓ ↓	1111	↓		14	A–(V.wa)	Zero
	ONAW		wa	↓ ↓	1100	↓		14	A ∧ (V.wa)	No Zero
	OFFAW		wa	↓ ↓	1101 ↓	↓		14	A ∧ (V.wa)	Zero
	ANIW	*	wa, byte	00000101	← Offset →	Data		19	(V.wa) ← (V.wa) ∧ byte	
	ORIW	*	wa, byte	0001	↓	↓		19	(V.wa) ← (V.wa) ∨ byte	
	GTIW	*	wa, byte	0010	↓	↓		13	(V.wa)–byte–1	No Borrow
	LTIW	*	wa, byte	0011	↓	↓		13	(V.wa)–byte	Borrow
	NEIW	*	wa, byte	0110	↓	↓		13	(V.wa)–byte	No Zero
	EQIW	*	wa, byte	0111	↓	↓		13	(V.wa)–byte	Zero
	ONIW	*	wa, byte	0100	↓	↓		13	(V.wa) ∧ byte	No Zero
	OFFIW	*	wa, byte	0101 ↓	↓	↓		13	(V.wa) ∧ byte	Zero
16-BIT ARITHMETIC	EADD		EA, r2	01110000	010000 R_1 R_0			11	EA ← EA+r2	
	DADD		EA, rp3	0100	110001 P_1 P_0			11	EA ← EA+rp3	
	DADC		EA, rp3	↓	1101			11	EA ← EA+rp3+CY	
	DADDNC		EA, rp3	↓	1010			11	EA ← EA+rp3	No Carry
	ESUB		EA, r2	↓ 0000	011000 R_1 R_0			11	EA ← EA–r2	

	MNEMONIC	OPERAND	OP CODE B1	B2	B3	B4	STATE	OPERATION	SKIP CONDITION
16-BIT ARITHMETIC	DSUB	EA, rp3	01110100	111001 P_1 P_0			11	EA ← EA−rp3	
	DSBB	EA, rp3		1111			11	EA ← EA−rp3−CY	
	DSUBNB	EA, rp3		1011			11	EA ← EA−rp3	No Borrow
	DAN	EA, rp3		100011 P_1 P_0			11	EA ← EA ∧ rp3	
	DOR	EA, rp3		1001			11	EA ← EA ∨ rp3	
	DXR	EA, rp3		100101 P_1 P_0			11	EA ← EA ∨̄ rp3	
	DGT	EA, rp3		101011 P_1 P_0			11	EA−rp3−1	No Borrow
	DLT	EA, rp3		1011			11	EA−rp3	Borrow
	DNE	EA, rp3		1110			11	EA−rp3	No Zero
	DEQ	EA, rp3		1111			11	EA−rp3	Zero
	DON	EA, rp3		1100			11	EA ∧ rp3	No Zero
	DOFF	EA, rp3		1101			11	EA ∧ rp3	Zero
MULTIP/ DIVIDE	MUL	r2	01001000	001011 P_1 P_0			32	EA ← A × r2	
	DIV	r2		0011			59	EA ← EA÷r2, r2 ← surplus	
INCREMENT/ DECREMENT	INR	r2	010000 R_1 R_0				4	r2←r2+1	Carry
	INRW *	wa	00100000	← Offset →			16	(V.wa) ← (V.wa)+1	Carry
	INX	rp	00 P_1 P_0 0010				7	rp ← rp+1	
		EA	10101000				7	EA ← EA+1	
	DCR	r2	010100 R_1 R_0				4	r2 ← r2−1	Borrow
	DCRW *	wa	00110000	← Offset →			16	(V.wa) ← (V.wa)−1	Borrow

	MNEMONIC	OPERAND	OP CODE B1	B2	B3	B4	STATE	OPERATION	SKIP CONDITION
	DCX	rp	00 P_1 P_0 0011				7	rp ← rp−1	
		EA	10101001				7	EA ← EA−1	
BIT MANIPULATION	MOV *	CY, bit	01011111	Bit Adrs			10	CY ← (bit)	
		bit,CY	01011010				13	(bit) ← CY	
	AND *	CY, bit	00110001				10	CY ← CY ∧ (bit)	
	OR *	CY, bit	01011100				10	CY ← CY ∨ (bit)	
	XOR *	CY, bit	01011110				10	CY ← CY ∨̄ (bit)	
	SETB *	bit	01011000				13	(bit) ← 1	
	CLR *	bit	01011011				13	(bit) ← 0	
	NOT *	bit	01011001				13	(bit) ← $\overline{(bit)}$	
	SK *	bit	01011101				10	Skip if (bit)=1	(bit)=1
	SKN *	bit	01010000				10	Skip if (bit)=0	(bit)=0
OTHERS	DAA		01100001				4	Decimal Adjust Accumulator	
	STC		01001000	00101011			8	CY ← 1	
	CLC			00101010			8	CY ← 0	
	CMC		01001000	10101010			8	CY ← $\overline{CY}$	
	NEGA			00111010			8	A ← A+1	
ROTAT. SHIFT	RLD		01001000	00111000			17	Rotate Left Digit	
	RRD			1001			17	Rotate Right Digit	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
ROTATE AND SHIFT	RLL	r2	01001000	001101 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow CY$, $CY \leftarrow r2_7$	
	RLR	r2		00 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow CY$, $CY \leftarrow r2_0$	
	SLL	r2		001001 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	
	SLR	r2		00 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	
	SLLC	r2		000001 R_1 R_0			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	Carry
	SLRC	r2		00 R_1 R_0			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	Carry
	DRLL	EA		10110100			8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow CY$, $CY \leftarrow EA_{15}$	
	DRLR	EA		0000			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow CY$, $CY \leftarrow EA_0$	
	DSLL	EA		10100100			8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow 0$, $CY \leftarrow EA_{15}$	
	DSLR	EA		0000			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow 0$, $CY \leftarrow EA_0$	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
JUMP	JMP *	word	01010100	← Low Adrs →	High Adrs		10	PC ← word	
	JB		00100001				4	$PC_H \leftarrow B$, $PC_L \leftarrow C$	
	JR	word	11 ← jdispl →				10	PC ← PC+1+jdispl	
	JRE *	word	0100111 ←	→ jdisp →			10	PC ← PC+2+jdispl	
	JEA		01001000	00101000			8	PC ← EA	
CALL	CALL *	word	01000000	← Low adrs →	High Adrs		16	(SP−1) ← $(PC+3)_H$, (SP−2) ← $(PC+3)_L$, PC ← word, SP ← SP−2	
	CALB		01001000	00101001			17	(SP−1) ← $(PC+2)_H$, (SP−2) ← $(PC+2)_L$, $PC_H \leftarrow B$, SP ← SP−2	
	CALF *	word	01111 ←	→ fa →			13	(SP−1) ← $(PC+2)_H$, (SP−2) ← $(PC+2)_L$, $PC_{15-11} \leftarrow 00001$, $PC_{10-0} \leftarrow fa$, SP ← SP−2	
	CALT	word	100 ← ta →				16	(SP−1) ← $(PC+1)_H$, (SP−2) ← $(PC+1)_L$, $PC_L \leftarrow (128+2ta)$, $PC_H \leftarrow (129+2ta)$, SP ← SP−2	
	SOFTI		01110010				16	(SP−1) ← PSW, (SP−2) ← $(PC+1)_H$, (SP−3) ← $(PC+1)_L$, PC ← 0060H, SP ← SP−3	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
RETURN	RET		10111000				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, SP ← SP+2	
	RETS		1001				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, SP ← SP+2, PC ← PC+n	
	RETI		01100010				13	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, PSW ← (SP+2), SP ← SP+3	Unconditional Skip
SKIP	SK	f	01001000	00001 F_2 F_1 F_0			8	Skip if f=1	f=1
	SKN	f		0001			8	Skip if f=0	f=0
	SKIT	irf		010 I_4 I_3 I_2 I_1 I_0			8	Skip if irf=1, then reset irf	irf=1
	SKNIT	irf		011 I_4 I_3 I_2 I_1 I_0			8	Skip if irf=0 Reset irf, if irf=1	irf=0
CPU CONTROL	NOP		00000000				4	No Operation	
	EI		10101010				4	Enable Interrupt	
	DI		10111010				4	Disable Interrupt	
	HLT		01001000	00111011			11	Halt	

Notes:

(*1) B2(Data) : rpa2 = D+byte, H+byte
(*2) B3(Data) : rpa3 = D+byte, H+byte
(*3) : right side of slash (/) in states indicates case rpa2, rpa3 = D+byte, H+A, H+B, H+EA, H+byte
(*4) : in the case of skip condition, the idle states are as follows.

1 byte instruction : 4 states
2 byte instruction : 8 states
3 byte instruction : 11 states
2 byte instruction (with *) : 7 states
3 byte instruction (with *) : 10 states
4 byte instruction : 14 states

ELECTRICAL SPECIFICATIONS

AND PACKAGE OUTLINES FOR

μPD7807/μPD7808

ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Threshold Voltage	V_{TH}		−0.5 to V_{CC} + 0.1	V
Operating Temperature	T_{opt}	10 MHz < f_{XTAL} ≤ 12 MHz	−10 to +70	°C
		f_{XTAL} ≤ 10 MHz	−40 to +85	°C
Storage Temperature	T_{stg}		−65 to + 150	°C

OPERATING CONDITION

PARAMETER / OSC. FREQ.	T_a	V_{CC}, AV_{CC}
10 MHz < f_{XTAL} ≤ 12 MHz *1	−10°C to +70°C	+5.0V ± 5 %
f_{XTAL} ≤ 10 MHz *1	−40°C to +85°C	+5.0V ± 10 %

CAPACITANCE

(T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_C = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except SCK, RESET, X1	2.0		V_{CC}	V
	V_{IH2}	SCK, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	RESET	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3), +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤ V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2*2	0.5	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.2	mA
V_{CC} Supply Current	I_{CC}			150*2	200	mA

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = 10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} − 0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE ↓	t_{AL}	*3, *5	65		ns
Address Hold from ALE ↓	t_{LA}	*3, *5	50		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*3, *5	150		ns
RD ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*3, *5		360	ns
ALE ↓ to Data Input	t_{LDR}	*3, *5		215	ns
RD ↓ to Data Input	t_{RD}	*3, *5		180	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*3, *5	35		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*3, *5	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *3, *5	280		ns
		OP Code Fetch *3, *5	530		ns
ALE Width High	t_{LL}	*3, *5	125		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*3	65		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*3	50		ns
IO/$\overline{M}$ Setup Time to ALE ↓	t_{IL}	*3	65		ns
IO/$\overline{M}$ Hold Time from ALE ↓	t_{LI}	*3	50		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*3, *5	150		ns
ALE ↓ to Data Output	t_{LDW}	*3, *5		195	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*3, *5	35		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*3, *5	230		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*3, *5	95		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*3, *5	115		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *5	280		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1		μs
			*7	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	420		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	420		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

DC CHARACTERISTICS

(T_a = −40°C to +70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3), +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3), 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤ V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2*2	0.6	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.5	mA
V_{CC} Supply Current	I_{CC}			150*2	220	mA

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −40°C to + 85°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		100	250	ns
Address Setup to ALE ↓	t_{AL}	*4, *5	100		ns
Address Hold from ALE ↓	t_{LA}	*4, *5	70		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*4, *5	200		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*4, *5		480	ns
ALE ↓ to Data Input	t_{LDR}	*4, *5		300	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*4, *5		250	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*4, *5	50		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*4, *5	150		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *4, *5	350		ns
		OP Code Fetch *4, *5	650		ns
ALE Width High	t_{LL}	*4, *5	160		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*4	100		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*4	70		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*4	100		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*4	70		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*4, *5	200		ns
ALE ↓ to Data Output	t_{LDW}	*4, *5		210	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*4, *5	50		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*4, *5	300		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*4, *5	130		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*4, *5	150		ns
$\overline{WR}$ Width Low	t_{WW}	*4, *5	350		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1.2		μs
			*7	500		ns
		$\overline{SCK}$ Output		2.4		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	505		ns
			*7	200		ns
		$\overline{SCK}$ Output		1.1		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	505		ns
			*7	200		ns
		$\overline{SCK}$ Output		1.1		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

HOLD OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

(T_a = −40°C to + 85°C V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HOLD ↑ Setup Time to ALE ↑	t_{SHDL}		2T + 150			ns
ALE ↑ to HLDA ↑ Delay	t_{DLHA}				T + 150	ns
HLDA ↑ to BUS Floating	t_{FBHA}		0			ns
HOLD ↓ to HLDA ↓ Delay	t_{HDDA}		T −50		4T + 150	ns
HLDA ↓ to Bus Enable Time	t_{EHAB}		0			ns
Bus Setup Time to ALE	t_{BL}		2T 100			ns

COMPARATOR CHARACTERISTICS

(T_a = -10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} - 0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = -40°C to +85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} - 0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Comparison Accuracy	V_{ACOMP}				± 100	mV
Threshold Voltage	V_{TH}		0		V_{CC}+0.1	V
Comparison Time	t_{COMP}		144		145	T_{CYC}
PT Input Voltage	V_{IPT}		0		V_{CC}	V

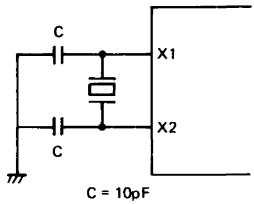
ZERO-CROSS CHARACTERISTICS

(T_a = -10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} -0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = -40°C to + 85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} -0.8V ≤ V_{DD} ≤ V_{CC})

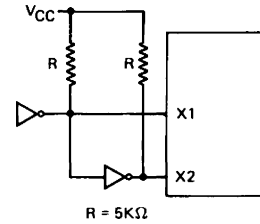
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	18	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

*1: XTAL oscillation circuit



C = 10pF

*8: External clock drive circuit



R = 5KΩ

*2: T_a = +25°C, V_{CC} = V_{DD} = 5V

*3: f_{XTAL} = 12 MHz

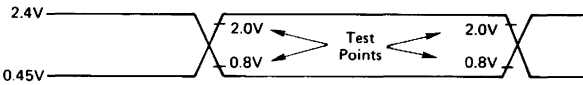
*4: f_{XTAL} = 10 MHz

*5: Load Capacitance: C_L = 150 pF

*6: Asynchronous mode with 1x baud rate, synchronous, I/O interface mode

*7: Asynchronous mode with 16x or 64x baud rate

AC TIMING TEST POINTS



EXTERNAL CLOCK

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = −40 C to + 85 C V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
High Level Width	$t_{\phi H}$		30	250	ns
Low Level Width	$t_{\phi L}$		30	250	ns
Rising Time	t_r		0	30	ns
Falling Time	t_f		0	30	ns

DATA RETENTION CHARACTERISTICS

(T_a = −10 to +70°C, V_{CC} = 0V, V_{DD} = V_{DDDR})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{DDDR}	RESET = V_{IL}	3.2		5.5	V
Data Retention Supply Current	I_{DDDR}	RESET = V_{IL}, V_{DDDR} = 3.2 V		1.3	3.0	mA

BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220 *1	MAX	ns
t_{LDR}	5T − 200 *1	MAX	ns
t_{RD}	4T − 150 *1	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read) *1 7T − 50 (OP Code Fetch) *1	MIN	ns
t_{LL}	2T − 40	MIN	ns
t_{ML}	2T − 100	MIN	ns
t_{LM}	T − 30	MIN	ns
t_{IL}	2T − 100	MIN	ns
t_{LI}	T − 30	MIN	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100 *1	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50 *1	MIN	ns
t_{CYK}	12T (SCK Input) *2 24T (SCK Output)	MIN	ns
t_{KKL}	5T + 5 (SCK Input) *2 12T − 100 (SCK Output)	MIN	ns
t_{KKH}	5T + 5 (SCK Input) *2 12T − 100 (SCK Output)	MIN	ns

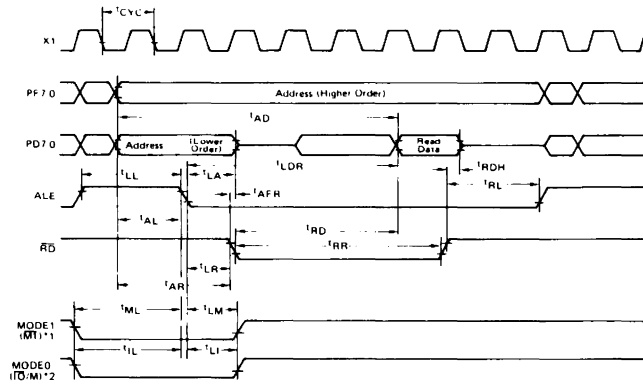
*1: Add 3T to each parameter in the case of external memory access using program WAIT function.

*2: Asynchronous mode with 1x baud rate, Synchronous, I/O Interface Mode

*3: T = t_{CYC} = 1/f_{XTAL}

*4: The items out of this table are not dependent on f_{XTAL}

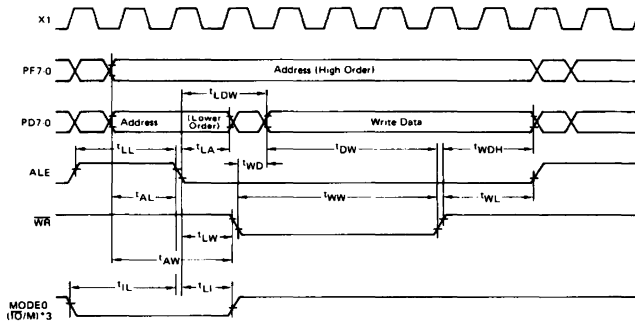
READ OPERATION



*1: $\overline{M1}$ signal is output to the MODE1 pin at 1st OP code fetch cycle when MODE 1 pin is pulled-up to V_{CC}.

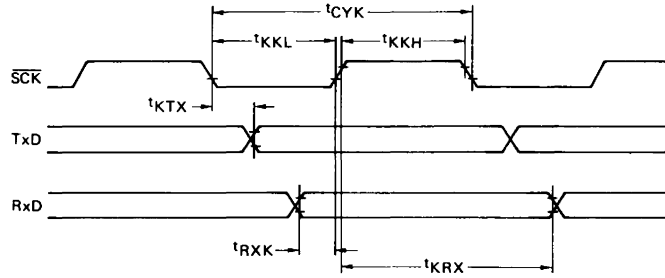
*2: $\overline{IO}$/M signal is output to the MODE0 pin at sr to sr2 register read timing when MODE0 pin is pulled-up to V_{CC}.

WRITE OPERATION

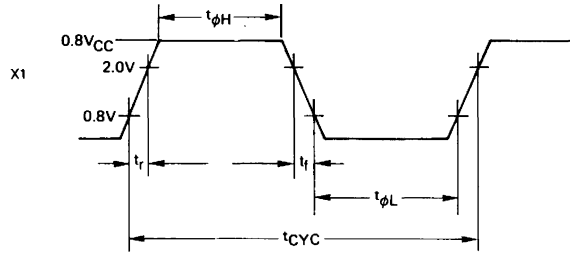


*3: $\overline{IO}$/M signal is output to the MODE0 pin at sr to sr2 register write timing when MODE0 pin is pulled-up to V_{CC}.

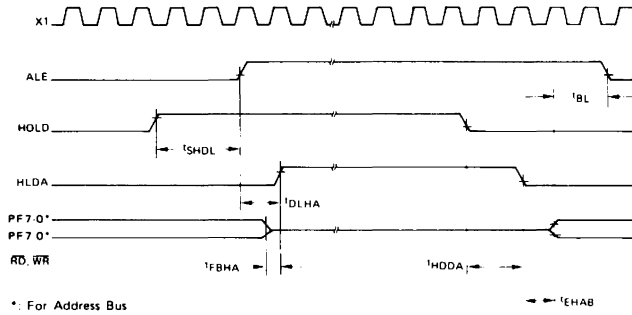
SERIAL OPERATION



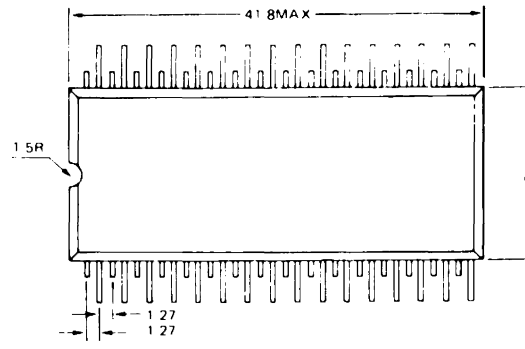
X1 INPUT WAVEFORM

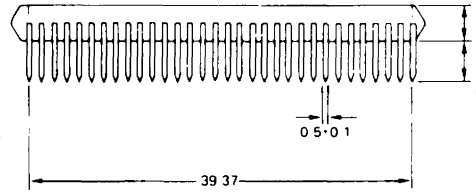


HOLD OPERATION

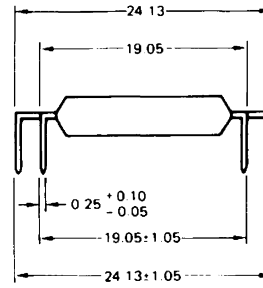


64 PIN PLASTIC
QUIP OUTLINE BENT LEADS
(Unit : mm)
μPD7807G/μPD7808G

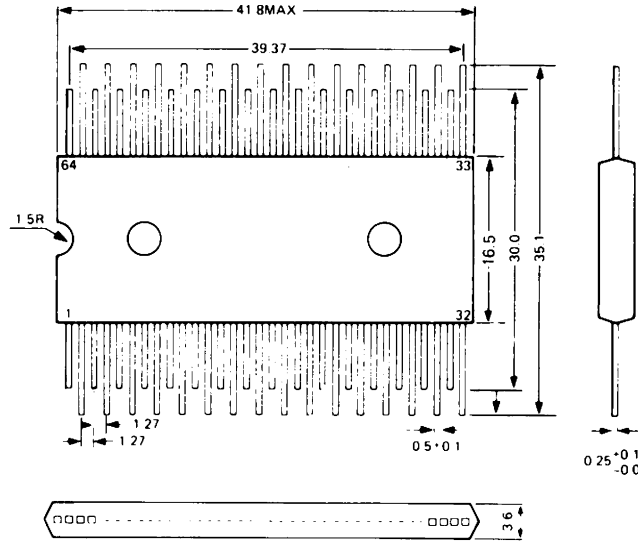




When ordering this package, specify as follows:
μPD7807G-36
μPD7808G-xxx-36



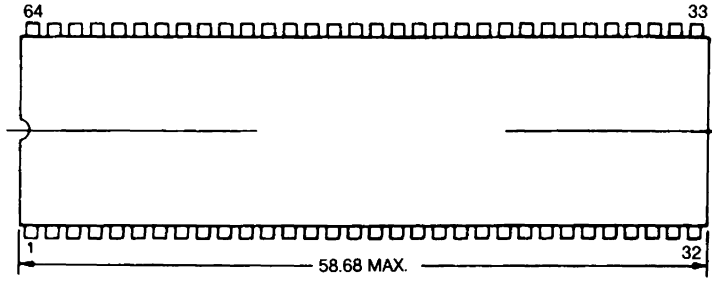
64 PIN PLASTIC QUIP
PACKAGE OUTLINE
STRAIGHT LEADS
(Unit : mm)
μPD7808



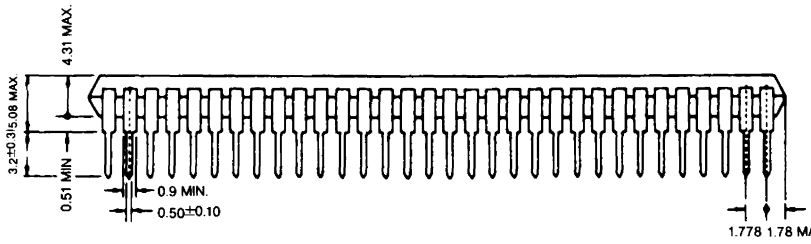
When ordering this package, specify as follows μPD7808G-xxx-37

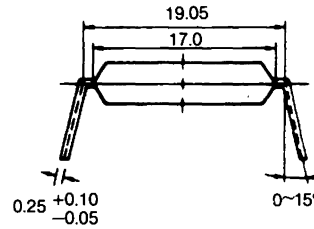
PACKAGE OUTLINE
μPD7807CW
μPD7808CW

64-PIN SHRINK DIP



When ordering this package, specify as follows:
μPD7807CW
μPD7808CW-xxx





ELECTRICAL SPECIFICATIONS

AND PACKAGE OUTLINES FOR

μPD7809

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Power Supply Voltage	V_{CC}		-0.5 to +7.0	V
	V_{DD}		-0.5 to +7.0	V
Input Voltage	V_I		-0.5 to +7.0	V
Output Voltage	V_O		-0.5 to +7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	-0.5	mA
		All Output Pin Total	-20	mA
Threshold Voltage	V_{TH}		-0.5 to V_{CC} + 0.1	V
Operating Temperature	T_{opt}	10 MHz < f_{XTAL} < 12 MHz	-10 to +70	°C
		f_{XTAL} ≤ 10 MHz	-10 to +70	°C
Storage Temperature	T_{stg}		-40 to +125	°C

OPERATING CONDITION

OSC. FREQ. \ PARAMETER	T_a	V_{CC}, AV_{CC}
10 MHz < f_{XTAL} ≤ 12 MHz *1	-10°C to +70°C	+5.0V ± 5 %
f_{XTAL} ≤ 10 MHz *1	-10°C to +70°C	+5.0V ± 10 %

CAPACITANCE

(T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_c = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = -10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} -0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = -200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤ V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2*2	0.5	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.2	mA
V_{CC} Supply Current	I_{CC}			150*2	200	mA

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE ↓	t_{AL}	*3, *5	65		ns
Address Hold from ALE ↓	t_{LA}	*3, *5	50		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*3, *5	150		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*3, *5		360	ns
ALE ↓ to Data Input	t_{LDR}	*3, *5		215	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*3, *5		180	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*3, *5	35		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*3, *5	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *3, *5	280		ns
		OP Code Fetch *3, *5	530		ns
ALE Width High	t_{LL}	*3, *5	125		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*3	65		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*3	50		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*3	65		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*3	50		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*3, *5	150		ns
ALE ↓ to Data Output	t_{LDW}	*3, *5		195	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*3, *5	35		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*3, *5	230		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*3, *5	95		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*3, *5	115		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *5	280		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1		μs
			*7	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	400		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	400		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

DC CHARACTERISTICS

(T_a = −40°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except $\overline{SCK}$, $\overline{RESET}$, X1	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3), +0.45V ≤ V_I ≤ V_{CC}			±200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3), 0V ≤ V_I ≤ V_{CC}			±10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤ V_{CC}			±10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2	0.6	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.5	mA
V_{CC} Supply Current	I_{CC}			150*2	220	mA

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} − 0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		100	250	ns
Address Setup to ALE ↓	t_{AL}	*4, *5	100		ns
Address Hold from ALE ↓	t_{LA}	*4, *5	70		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*4, *5	200		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*4, *5		480	ns
ALE ↓ to Data Input	t_{LDR}	*4, *5		300	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*4, *5		250	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*4, *5	50		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*4, *5	150		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *4, *5	350		ns
		OP Code Fetch *4, *5	650		ns
ALE Width High	t_{LL}	*4, *5	160		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*4	100		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*4	70		ns
$\overline{IO}$ M Setup Time to ALE ↓	t_{IL}	*4	100		ns
$\overline{IO}$ M Hold Time from ALE ↓	t_{LI}	*4	70		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*4, *5	200		ns
ALE ↓ to Data Output	t_{LDW}	*4, *5		210	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*4, *5	50		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*4, *5	300		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*4, *5	130		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*4, *5	150		ns
$\overline{WR}$ Width Low	t_{WW}	*4, *5	350		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1.2		μs
			*7	500		ns
		$\overline{SCK}$ Output		2.4		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	500		ns
			*7	200		ns
		$\overline{SCK}$ Output		1.1		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	500		ns
			*7	200		ns
		SCK Output		1.1		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

HOLD OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HOLD ↑ Setup Time to ALE ↑	t_{SHDL}		2T + 150			ns
ALE ↑ to HLDA ↑ Delay	t_{DLHA}				T + 150	ns
HLDA ↑ to BUS Floating	t_{FBHA}		0			ns
HOLD ↓ to HLDA ↓ Delay	t_{HDDA}		T −50		4T + 150	ns
HLDA ↓ to Bus Enable Time	t_{EHAB}		0			ns
Bus Setup Time to ALE	t_{BL}		2T −100			ns

COMPARATOR CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Comparison Accuracy	V_{ACOMP}				± 100	mV
Threshold Voltage	V_{TH}		0		V_{CC}+0.1	V
Comparison Time	t_{COMP}		144		145	T_{CYC}
PT Input Voltage	V_{IPT}		0		V_{CC}	V

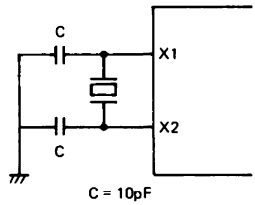
ZERO-CROSS CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

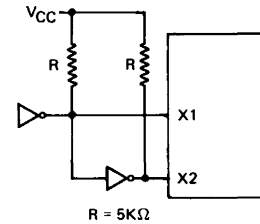
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	18	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

*1: XTAL oscillation circuit



C = 10pF

*8: External clock drive circuit



R = 5KΩ

*2: T_a = +25°C, V_{CC} = V_{DD} = 5V

*3: f_{XTAL} = 12 MHz

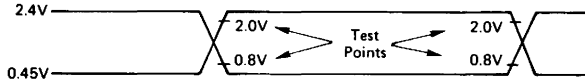
*4: f_{XTAL} = 10 MHz

*5: Load Capacitance: C_L = 150 pF

*6: Asynchronous mode with 1x baud rate, synchronous, I/O interface mode

*7: Asynchronous mode with 16x or 64x baud rate

AC TIMING TEST POINTS



EXTERNAL CLOCK

(T_a = 10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} = 0.8V ≤ V_{DD} ≤ V_{CC})

(T_a = 10°C to +70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} = 0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
High Level Width	$t_{\phi H}$		30	250	ns
Low Level Width	$t_{\phi L}$		30	250	ns
Rising Time	t_r		0	30	ns
Falling Time	t_f		0	30	ns

DATA RETENTION CHARACTERISTICS

(T_a = −10 to +70°C, V_{CC} = 0V, V_{DD} = V_{DDDR})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{DDDR}	$\overline{RESET}$ = V_{IL}	3.2		5.5	V
Data Retention Supply Current	I_{DDDR}	$\overline{RESET}$ = V_{IL}, V_{DDDR} = 3.2 V		1.3	3.0	mA

BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220 *1	MAX	ns
t_{LDR}	5T − 200 *1	MAX	ns
t_{RD}	4T − 150 *1	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read) *1 7T − 50 (OP Code Fetch) *1	MIN	ns
t_{LL}	2T − 40	MIN	ns
t_{ML}	2T − 100	MIN	ns
t_{LM}	T − 30	MIN	ns
t_{IL}	2T − 100	MIN	ns
t_{LI}	T − 30	MIN	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100 *1	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50 *1	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ Input) *2 24T ($\overline{SCK}$ Output)	MIN	ns
t_{KKL}	5T + 5 (SCK Input) *2 12T − 100 ($\overline{SCK}$ Output)	MIN	ns
t_{KKH}	5T + 5 (SCK Input) *2 12T − 100 ($\overline{SCK}$ Output)	MIN	ns

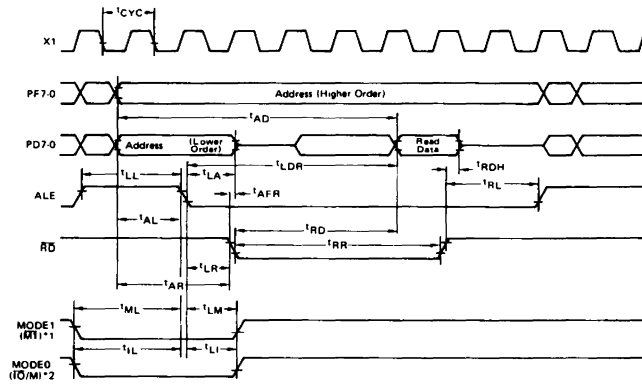
*1: Add 3T to each parameter in the case of external memory access using program WAIT function.

*2: Asynchronous mode with 1x baud rate, Synchronous, I/O Interface Mode

*3: T = t_{CYC} = $1/f_{XTAL}$

*4: The items out of this table are not dependent on f_{XTAL}.

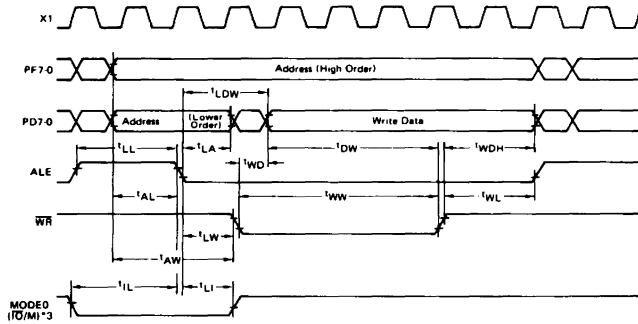
READ OPERATION



*1: $\overline{M1}$ signal is output to the MODE1 pin at 1st OP code fetch cycle when MODE 1 pin is pulled-up to V_{CC}.

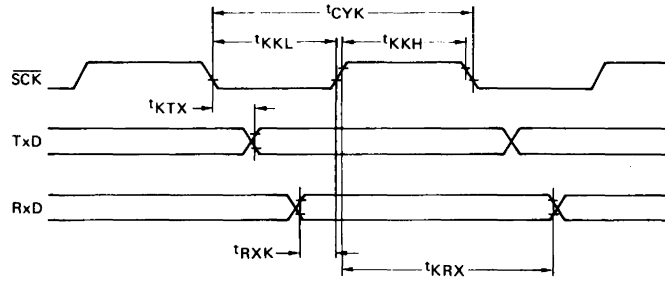
*2: $\overline{IO}$/M signal is output to the MODE0 pin at sr to sr2 register read timing when MODE0 pin is pulled-up to V_{CC}.

WRITE OPERATION

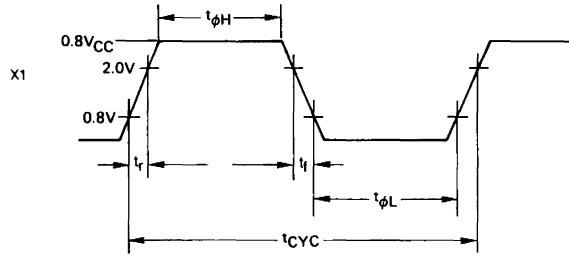


*3: $\overline{IO}$/M signal is output to the MODE0 pin at sr to sr2 register write timing when MODE0 pin is pulled-up to V_{CC}.

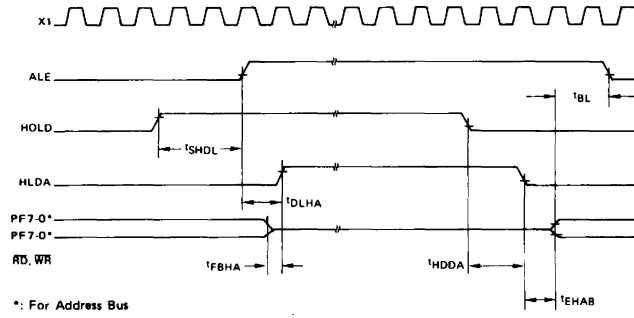
SERIAL OPERATION



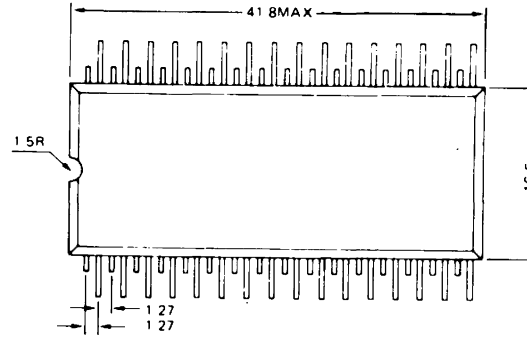
X1 INPUT WAVEFORM

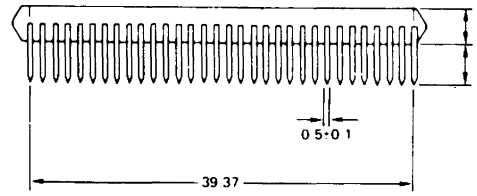


HOLD OPERATION



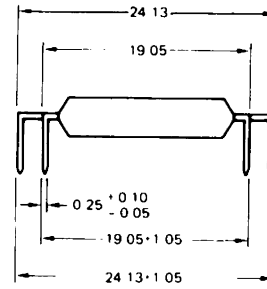
64 PIN PLASTIC
QUIP OUTLINE BENT LEADS
(Unit : mm)
μPD7809G



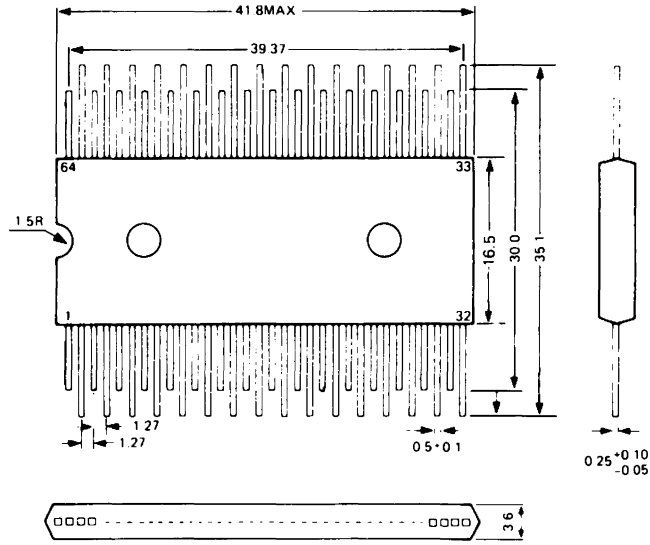


When ordering this package, specify as follows:

μPD7809G-xxx-36



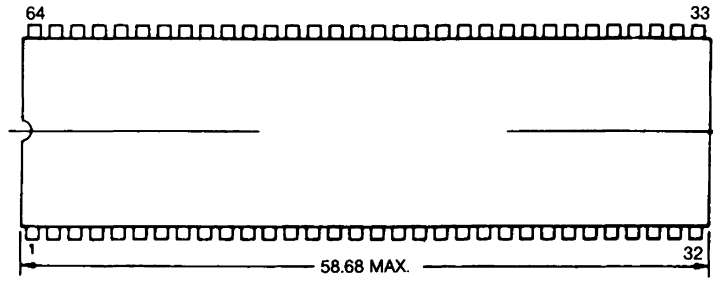
64 PIN PLASTIC
PACKAGE OUTLINE
STRAIGHT LEADS
(Unit : mm)
μPD7809



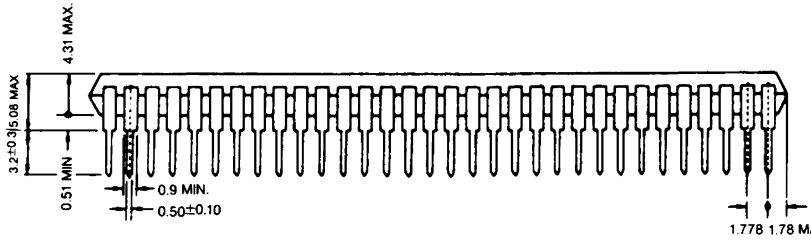
When ordering this package, specify as follows: μPD7809G-xxx-37

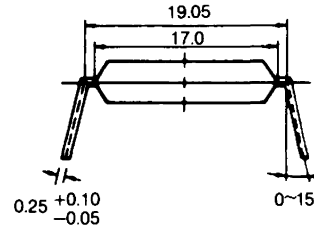
PACKAGE OUTLINE
μPD7809CW

64-PIN SHRINK DIP



When ordering this package, specify as follows:
μPD7807CW
μPD7808CW-xxx





ELECTRICAL SPECIFICATIONS

AND PACKAGE OUTLINES FOR

μPD78P09

ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Threshold Voltage	V_{TH}		−0.5 to V_{CC} + 0.1	V
Operating Temperature	T_{opt}	4 MHz < f_{XTAL} < 12 MHz	−10 to +50	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

OSC. FREQ. \ PARAMETER	T_a	V_{CC}, AV_{CC}
4 MHz ≤ f_{XTAL} ≤ 12 MHz	−10°C to +70°C	+5.0V ± 5 %

CAPACITANCE

T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_C = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except SCK, RESET, X1	2.0		V_{CC}	V
	V_{IH2}	SCK, X1 *8	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	RESET	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3), +0.45V ≤ V_I ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_I ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	+0.45V ≤ V_O ≤ V_{CC}			± 10	μA
V_{TH} Input Current	I_{TH}	V_{TH} = V_{CC}		0.2*2	0.5	mA
V_{DD} Supply Current	I_{DD}			1.5 *2	3.2	mA
V_{CC} Supply Current	I_{CC}			240*2	320	mA

AC CHARACTERISTICS
READ/WRITE OPERATION

(T_a 10°C to +50°C, V_{CC} +5.0V ± 5%, V_{SS} 0V, V_{CC} 0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE ↓	t_{AL}	*3, *5	65		ns
Address Hold from ALE ↓	t_{LA}	*3, *5	50		ns
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	*3, *5	150		ns
$\overline{RD}$ ↓ to Address Floating	t_{AFR}	*5		20	ns
Address to Data Input	t_{AD}	*3, *5		360	ns
ALE ↓ to Data Input	t_{LDR}	*3, *5		215	ns
$\overline{RD}$ ↓ to Data Input	t_{RD}	*3, *5		180	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	*3, *5	35		ns
Data Hold Time from $\overline{RD}$ ↑	t_{RDH}	*5	0		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	*3, *5	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read *3, *5	280		ns
		OP Code Fetch *3, *5	530		ns
ALE Width High	t_{LL}	*3, *5	125		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*3	65		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*3	50		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*3	65		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*3	50		ns
Address to $\overline{WR}$ ↓ Delay	t_{AW}	*3, *5	150		ns
ALE ↓ to Data Output	t_{LDW}	*3, *5		195	ns
$\overline{WR}$ ↓ to Data Output	t_{WD}	*5		100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time	t_{LW}	*3, *5	35		ns
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	*3, *5	230		ns
Data Hold Time from $\overline{WR}$ ↑	t_{WDH}	*3, *5	95		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	*3, *5	115		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *5	280		ns

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*6	1.66		μs
			*7	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*6	750		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*6	750		ns
			*7	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*6		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*6		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*6			210	ns

HOLD OPERATION

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HOLD ↑ Setup Time to ALE ↑	t_{SHDL}		2T + 150			ns
ALE ↑ to HLDA ↑ Delay	t_{DLHA}				T + 150	ns
HLDA ↑ to BUS Floating	t_{FBHA}		0			ns
HOLD ↓ to HLDA ↓ Delay	t_{HDOA}		T −50		4T + 150	ns
HLDA ↓ to Bus Enable Time	t_{EHAB}		0			ns
Bus Setup Time to ALE	t_{BL}		2T −100			ns

COMPARATOR CHARACTERISTICS

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} − 0.8V ≤ V_{DD} ≤ V_{CC})

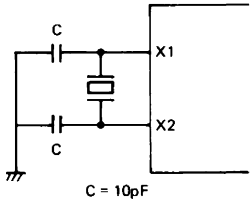
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Comparison Accuracy	V_{ACOMP}				± 100	mV
Threshold Voltage	V_{TH}		0		V_{CC}+0.1	V
Comparison Time	t_{COMP}		144		145	T_{CYC}
PT Input Voltage	V_{IPT}		0		V_{CC}	V

ZERO-CROSS CHARACTERISTICS

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} − 0.8V ≤ V_{DD} ≤ V_{CC})

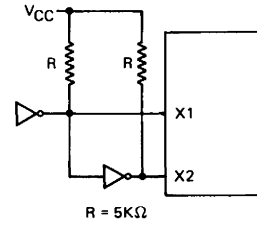
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

*1: XTAL oscillation circuit



C = 10pF

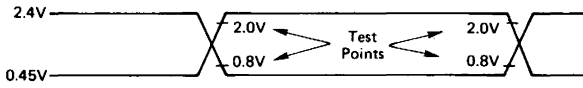
*8: External clock drive circuit



R = 5KΩ

*2: T_a = +25°C, V_{CC} = V_{DD} = 5V
*3: f_{XTAL} = 12 MHz
*4: f_{XTAL} = 10 MHz
*5: Load Capacitance: C_L = 150 pF
*6: Asynchronous mode with 1x baud rate, synchronous, I/O interface mode
*7: Asynchronous mode with 16x or 64x baud rate

AC TIMING TEST POINTS



EXTERNAL CLOCK

(T_a = −10°C to +50°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
High Level Width	$t_{\phi H}$		30	250	ns
Low Level Width	$t_{\phi L}$		30	250	ns
Rising Time	t_r		0	30	ns
Falling Time	t_f		0	30	ns

DATA RETENTION CHARACTERISTICS

(T_a = −10 to +50°C, V_{CC} = 0V, V_{DD} = V_{DDDR})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Voltage	V_{DDDR}	RESET = V_{IL}	3.2		5.5	V
Data Retention Supply Current	I_{DDDR}	RESET = V_{IL}, V_{DDDR} = 3.2 V		1.3	3.0	mA

BUS TIMING DEPENDING ON tCYC

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220 *1	MAX	ns
t_{LDR}	5T − 200 *1	MAX	ns
t_{RD}	4T − 150 *1	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read) *1 7T − 50 (OP Code Fetch) *1	MIN	ns
t_{LL}	2T − 40	MIN	ns
t_{ML}	2T − 100	MIN	ns
t_{LM}	T − 30	MIN	ns
t_{IL}	2T − 100	MIN	ns
t_{LI}	T − 30	MIN	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100 *1	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50 *1	MIN	ns
t_{CYK}	20T (SCK Input) *2 24T (SCK Output)	MIN	ns
t_{KKL}	10T − 80 (SCK Input) *2 12T − 100 (SCK Output)	MIN	ns
t_{KKH}	10T − 80 (SCK Input) *2 12T − 100 (SCK Output)	MIN	ns

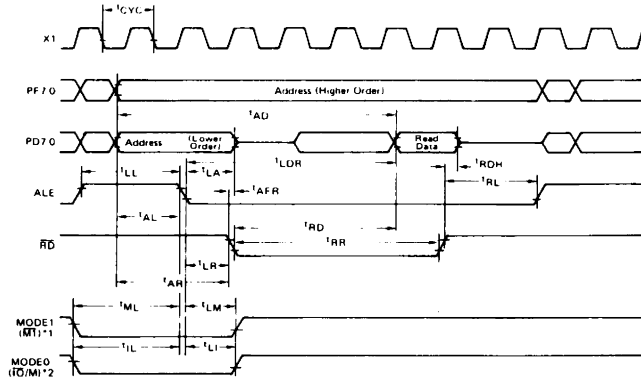
*1: Add 3T to each parameter in the case of external memory access using program WAIT function.

*2: Asynchronous mode with 1x baud rate, Synchronous, I/O Interface Mode

*3: T = t_{CYC} = $1/f_{XTAL}$

*4: The items out of this table are not dependent on f_{XTAL}

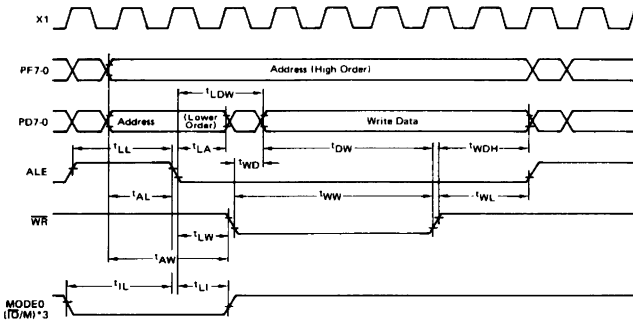
READ OPERATION



*1: $\overline{M1}$ signal is output to the MODE1 pin at 1st OP code fetch cycle when MODE 1 pin is pulled-up to V_{CC}.

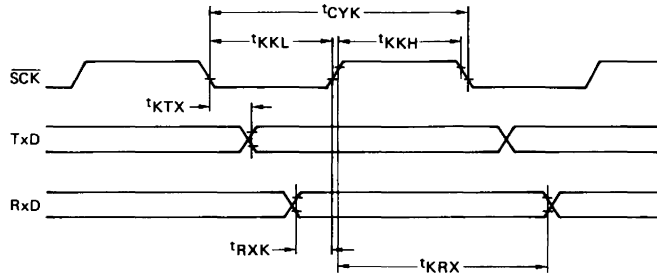
*2: $\overline{IO}/M$ signal is output to the MODE0 pin at sr to sr2 register read timing when MODE0 pin is pulled-up to V_{CC}.

WRITE OPERATION

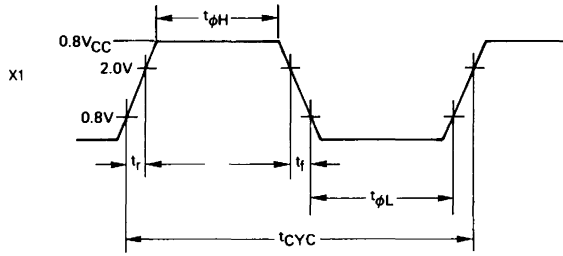


*3: $\overline{IO}/M$ signal is output to the MODE0 pin at sr to sr2 register write timing when MODE0 pin is pulled-up to V_{CC}.

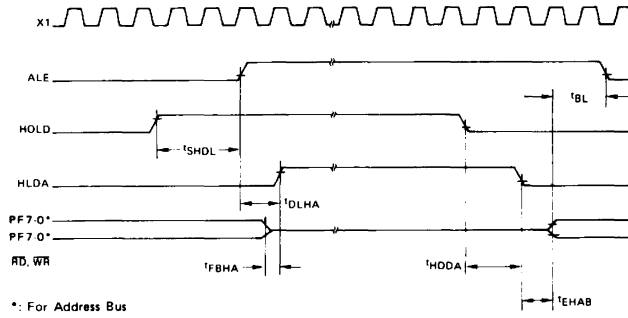
SERIAL OPERATION



X1 INPUT WAVEFORM



HOLD OPERATION



DC PROGRAMMING CHARACTERISTICS

(T_a = +25°C ± 5°C, V_{CC} = +5V ± 10%, V_{PP} = +21V ± 0.5V, V_{SS} = 0V, V_{CC} − 0.8 ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current All except INT1, TI(PC3)	I_{LI}	0V ≤ V_{IN} ≤ V_{CC}			±10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −200μA	2.4			V
V_{CC} Supply Current	I_{CC}			200	300	mA
Input Low Level (All Inputs)	V_{IL}		0		0.8	V
Input High Level	V_{IH1}	All except $\overline{SCK}$, RESET and X1	2.0		V_{CC}	V
	V_{IH2}	SCK, X1	0.8 V_{CC}		V_{CC}	V
V_{PP} Supply Current	I_{PP}	$\overline{PGM}$ = V_{IL}			30	mA

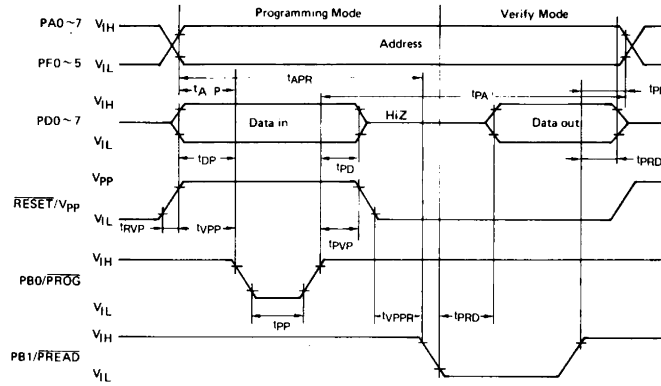
AC PROGRAMMING CHARACTERISTICS

(T_a = +25°C ± 5°C, V_{CC} = +5V ± 10%, V_{PP} = +21V ± 0.5V, V_{SS} = 0V, V_{CC} − 0.8 ≤ V_{DD} ≤ V_{CC})

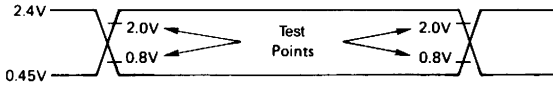
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Address Setup Time	Programming Mode	t_{AP}		2			μs
	Verify Mode	t_{APR}		2			μs
V_{PP} Setup Time		t_{VPP}		2			μs
Data Setup Time		t_{DP}		2			μs
Address Hold Time	Programming Mode	t_{PA}		2			μs
	Verify Mode	t_{PRA}		0			μs
V_{PP} Hold Time		t_{PVP}		2			μs
Data Hold Time		t_{PD}		2			μs
$\overline{READ}$ to Output Float Delay		t_{PRDR}		0		130	ns
Data Valid from $\overline{READ}$		t_{PRD}				1	μs
$\overline{PROG}$ Pulse Width During Programming		t_{PP}		45	50	55	ms
V_{PP} Pulse Rise Time During Programming		t_{RVP}		50			ns
V_{PP} Recovery Time		t_{VPPR}		2			μs
Input Rise/Fall Time		t_{IR} t_{IF}				20	ns

TIMING WAVEFORM

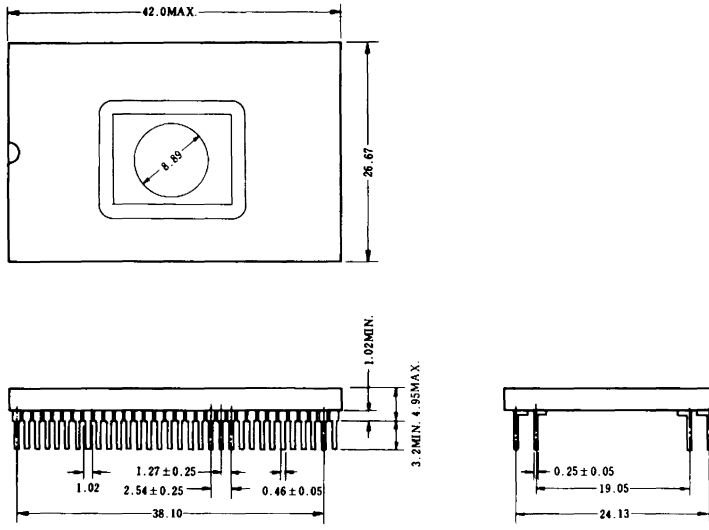
PROGRAMMING



AC TIMING MEASUREMENT POINTS



64 PIN CERAMIC QUIP OUTLINE (Unit : mm)
μPD78P09R



Note: The μPD78P09 is programmable on NEC programmer PG 1000 together with programmer module PG 1003.

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH ON CHIP A/D CONVERTER

DESCRIPTION

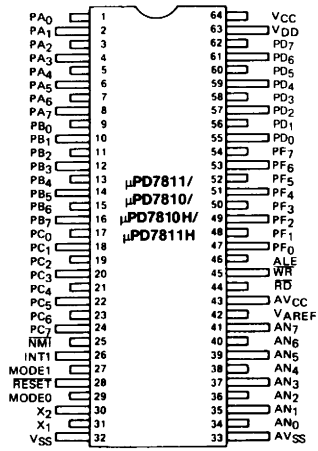
The NEC μPD7810/7811 is a high-performance single-chip microcomputer integrating sophisticated on-chip peripheral functionality normally provided by external components. The devices's internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make the μPD7810/7811 appropriate in data processing as well as control applications. The device integrates a 16-bit ALU, 4K-ROM, 256-byte RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART and two zero-cross detect inputs on a single die, to direct the device into fast, high-end processing applications involving analog signal interface and processing.

The μPD7811 is the mask-ROM high volume production device embedded with customer program. The μPD7810 is a ROM-less version for prototyping and small volume production. The μPD78PG11E is a piggy-back EPROM version for design development.
The μPD7810H/11H is a high speed version of the μPD7810/11 (15 MHz operation)

FEATURES

- Powerful Instruction Set Including 16-bit Multiply and Divide, 158 instructions
- High-Speed 1μsec Cycle Time-12 MHz Operation (0.85 μsec for 7810H/11H, 15 MHz)
- On-Chip 4K-Byte ROM (7811), 256-Byte RAM
- 44 I/O Lines
- Easily Expandable Memory up to 60K Bytes (externally)
- On-Chip 8-Bit A/D Converter-8 Input Channels
- Multi-Functional 16-Bit Timer/Counter
- Two Programmable 8-Bit Timers
- Full-Duplex Serial Communication Interface, synchronous and asynchronous
- Zero-Cross Detection Capability
- Vectored Interrupts, 3 external/8 internal
- Low Power Standby Operation
- 8085A Bus Compatible
- Single Power Supply +5V, N-MOS Technology
- Available in 64 Pin Package
- Standby function
- On-chip clock generator
- 64K-Byte total memory address range

PIN CONFIGURATION



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION	
1–8	PA_0–PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode.	
9–16	PB_0–PB_7	Port B: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port B in input mode.	
17	PC_0	Port C: (Three-state input/output) 8-bit programmable I/O port. Each line independently pro-programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer, event-counter and external interrupts. Reset puts Port C in Port mode and all lines in input mode.	Transmit Data (TxD): Serial data output terminal.
18	PC_1		Receive Data (RxD): Serial data input terminal.
19	PC_2		Serial Clock ($\overline{SCK}$): Serial clock input/output terminal. When internal clock is used, the output can be selected; when an external clock is used, the input can be selected.
20	PC_3		Timer Input ((TI)/interrupt request input (INT2): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4		Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5		Counter Input (CI): External pulse input terminal to the timer/event counter.
23–24	PC_6, PC_7		Counter Outputs 0, 1 (CO_0–CO_1): Programmable rectangular wave output terminal based on timer/event counter.
25	$\overline{NMI}$	Falling-edge, nonmaskable interrupt ($\overline{NMI}$) input.	
26	INT1	This signal is a rising-edge, maskable interrupt input. This input is also used to make the zero-cross detection AC input.	
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 Signal during each opcode fetch.	
28	$\overline{RESET}$	(Input, active low), $\overline{RESET}$ initializes the μPD7811.	
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to output $\overline{IO}$/M.	
30–31	X_2, X_1 (crystal)	This is a crystal connection terminal for system clock oscillation. When an external clock is supplied X_1 is the input.	
32	V_{SS}	Power supply ground potential.	
33	AV_{SS}	A/D converter power supply ground potential. Sets conversion's range lower limit.	

PIN IDENTIFICATION (cont.)

PIN NO.	PIN SYMBOL	FUNCTION
34–41	AN_0–AN_7	Eight analog inputs to the A/D converter. AN_7–AN_4 can also be used as a digital input port for falling edge detection.
42	V_{AREF}	Reference voltage for A/D converter. Sets conversion's range upper limit.
43	AV_{CC}	Power supply voltage for A/D converter.
44	$\overline{RD}$	(Three-state output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes high during Reset.
45	$\overline{WR}$	(Three-state output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes high during Reset.
46	ALE	The strobe signal is for latching the address signal to the output from PD_7–PD_0 when accessing external expansion memory.
47–54	PF_0–PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55–62	DB_0–DB_7	Port D: 8-bit programmable I/O port. This byte can be designated as either input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	V_{DD}	This ia a second power supply line for on-chip RAM back-up
64	V_{CC}	+5V power supply.

Notes: 1 clock cycle = 1 CL = 3/f.
1 machine cycle = 3 or 4 clock cycles.
1 instruction cycle = 1 to 19 machine cycles.
f: System clock frequency (MHz).

NEW INSTRUCTIONS

In addition to the existing instruction set for μPD7801, the following new instructions are incorporated in the μPD7810/11:

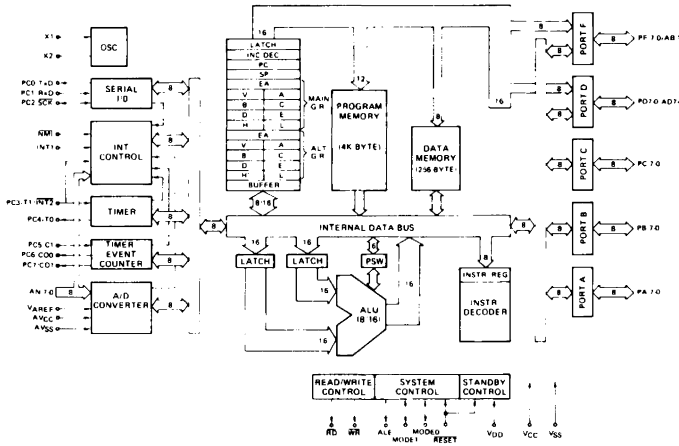
16-bit data transfer between memory and extended accumulator
16-bit data arithmetic and logical operation.

16-bit data addition and subtraction and 16-bit comparsion.
16-bit data shift and rotation
direct multiply and divide instructions.

8-bit by 8-bit division less then 8 μsec execution time.

16-bit divided by 8-bit less than 15 μsec execution
table look-up operation.
Register pair HL and DE are used as base register. Accumulator, B-register and extended accumulator are used as index register.

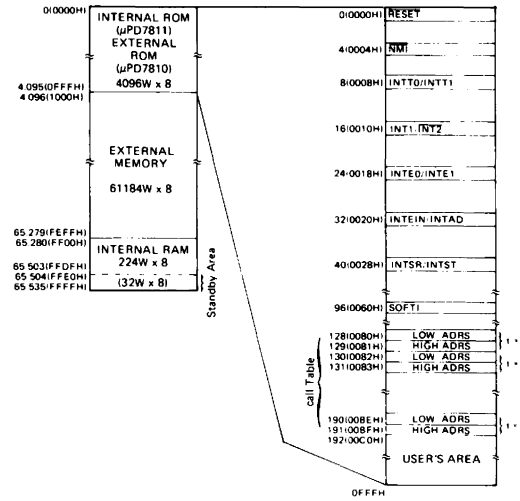
BLOCK DIAGRAM



Note: the μPD7810/10H has no programmable ROM (4K bytes) on chip.

MEMORY MAP

The μPD7811 can directly address up to 64K-bytes of memory. Except for the on-chip ROM (0-4095) and RAM (65280–65535), any memory location can be used as ROM or RAM. The following memory map defines the 0-64K-byte memory space for the μPD7811.



INPUT/OUTPUT

8 Analog Input Lines
44 Digital I/O Lines: five 8-bit ports (Port A, Port B, Port C, Port D, Port F) and 4 input lines (AN_4–AN_7)

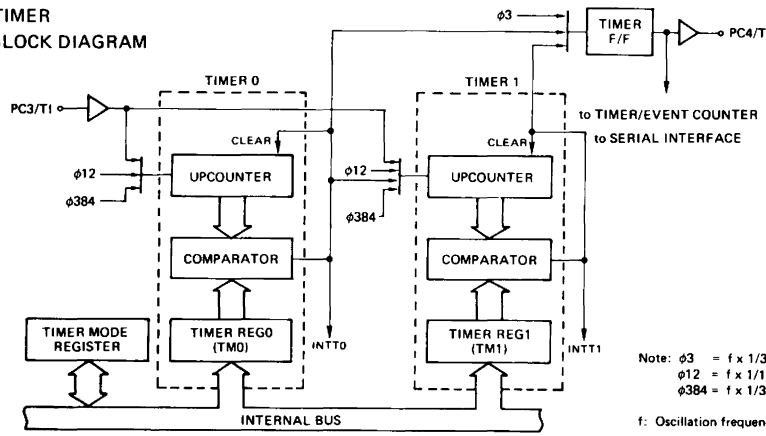
1. Analog Input Lines
   AN_0–AN_7 are configured as analog input lines for on-chip A/D converter.
2. Port Operation
   - Port A, Port B, Port C, Port F
     Each line of these ports can be individually programmed as an input or as an output. When used as I/O ports, all have latches outputs, high-impedance inputs.
   - Port D
     Port D can be programmed as a byte input or a byte output.
   - AN_4–AN_7
     The high-order analog input lines, AN_4–AN_7 can be used as digital input lines for falling edge detection.
3. Control Lines
   Under software control, each line of Port C can be configured individually to provide control lines for serial interface, timer and timer/counter, and interrupts.
4. Memory Expansion
   In addition to the single-chip operation mode the μPD7811 has 4 memory expansion modes. Under software control, Port D can provide multiplexed low-order address and data bus and Port F can provide high-order address bus. The relation between memory expansion modes and the pin configurations of Port D and Port F is shown in the table that follows.

MEMORY EXPANSION		PORT CONFIGURATION
None	Port D Port F	I/O Port I/O Port
256 Bytes	Port D Port F	Multiplexed Address/Data Bus I/O Port
4K Bytes	Port D Port F_0–F_3 Port F_4–F_7	Multiplexed Address/Data Bus Address Bus I/O Port
16K Bytes	Port D Port F_0–F_5 Port F_6–F_7	Multiplexed/Data Bus Address Bus I/O Port
60K Bytes	Port D Port F	Multiplexed Address/Data Bus Address Bus

TIMERS

The timer/event counter consists of two 8-bit timers. The timers may be programmed independently or may be cascaded and used as a 16-bit timer. The timer can be set by software to increment at intervals of 4 machine cycles (1μs at 12MHz operation) or 128 machine cycles (32μs at 12MHz), or to increment on receipt of a pulse at TI.

TIMER BLOCK DIAGRAM



Note: φ3 = f x 1/3
φ12 = f x 1/12
φ384 = f x 1/384

f: Oscillation frequency

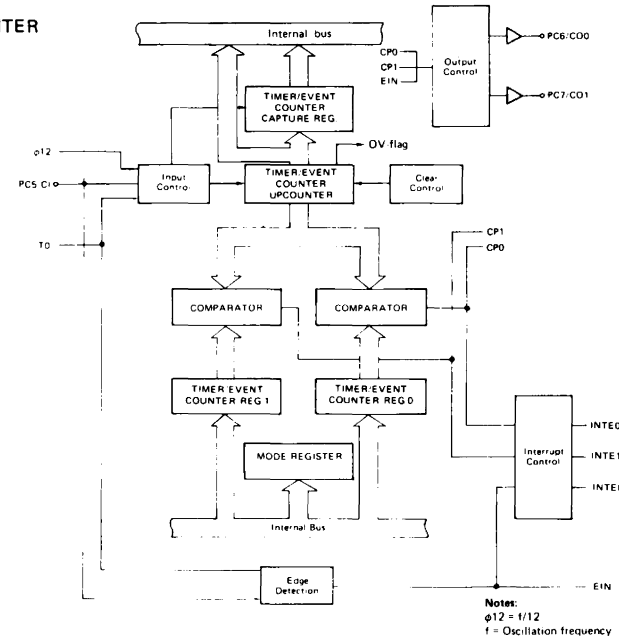
FUNCTIONAL DESCRIPTION (CONT.)

TIMER/EVENT COUNTER

The 16-bit Multifunctional timer/event counter can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse width measurement
- Programmable square-wave output
- Single pulse generation

TIMER/EVENT COUNTER BLOCK DIAGRAM



ANALOG/DIGITAL CONVERTER

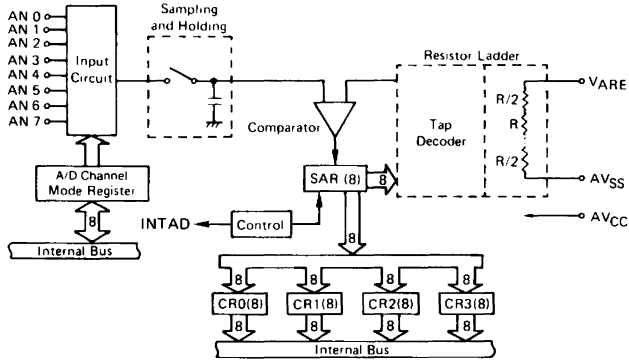
8 Input Channels
4 Conversion Result Registers
2 Powerful Operation Modes
  Auto Scan Mode
  Channel Select Mode
Successive Approximation Technique

Absolute Accuracy	± 1.5 LSB (± 0.6%)
Conversion Range	0 ~ 5V
Conversion Time	48 μs

Interrupt Generation

The μPD7810/7811 features an 8-bit, high-speed, high accuracy A/D converter. The A/D converter comprises a 256-Resistor Ladder and Successive Approximation Register (SAR). There are four conversion result registers (CR_0–CR_3). The 8-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR_0–CR_3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers.

A/D CONVERTER BLOCK DIAGRAM

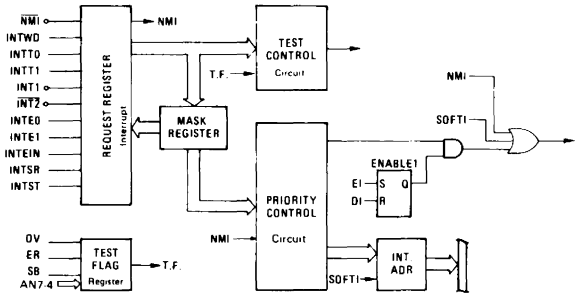


INTERRUPT STRUCTURE

There are 11 interrupt sources. Three are external interrupts and 8 are internal. These 11 interrupt sources are divided into 6 priority levels as shown in the table below.

INTERRUPT REQUEST	INTERRUPT VECTOR	TYPE OF INTERRUPT		IN/EXT
IRQ0	4	NMI	(Non-maskable interrupt)	External
IRQ1	8	INTT0 INTT1	(Coincidence signal from timer 0) (Coincidence signal from timer 1)	Internal
IRQ2	16	INT1 INT2	(Maskable intrrupt) (Maskable interrupr)	External
IRQ3	24	INTE0 INTE1	(Coincidence signal from timer/ event counter) Coincidence signal from timer/ event counter)	Internal
IRQ4	32	INTEIN INTAD	(Falling signal of C1 and T0 counter) (A/D converter interrupt)	In/External
IRQ5	40	INTSR INST	(Serial receive interrupt) (Serial send interrupt)	Internal

INTERRUPT CONTROL BLOCK DIAGRAM



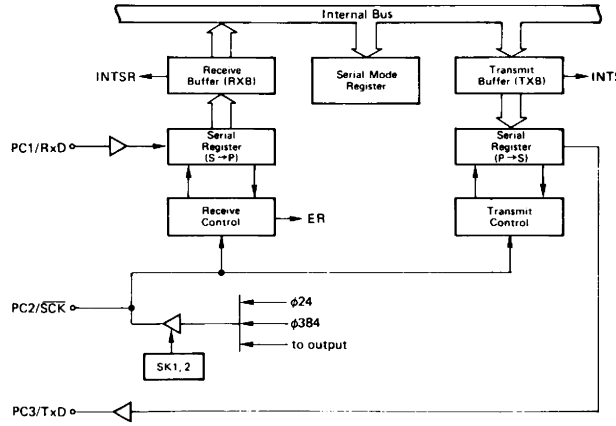
STANDBY FUNCTION

The μPD7810/7811 offers a standby function that allows the user to save up to 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On powerup the μPD7811 checks whether recovery was made from standby mode or from cold start.

UNIVERSAL SERIAL INTERFACE

The serial interface can operate in any of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first for ease of communication with certain peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception. In the search mode, data are transferred one bit at a time from serial register to receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from serial register to transmit buffer occurs 8 bits at a time.

UNIVERSAL SERIAL INTERFACE BLOCK DIAGRAM



Note: $\phi 24 = \frac{1}{24}$

f: oscillation frequency (MHz)

$\phi 384 = \frac{1}{384}$

ZERO-CROSSING DETECTOR

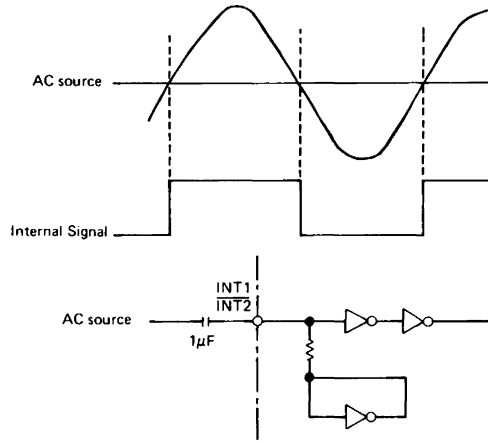
The INT1 and INT2 terminals (used also as TI and PC_3) can be used to detect the zero-crossing point of slow moving AC signals. When driven directly, these pins respond as a normal digital input.

To utilize the zero-cross detection mode, an AC signal of approximately 1 – 1.8V peak-to-peak magnitude and a maximum frequency of 1kHz is coupled through an external capacitor to these pins.

For the INT1 pin, the internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one and INT1 interrupt is generated.

For the INT2 pin, the state is sensed as a one until the falling edge crosses the DC average level, when it becomes a zero and INT2 interrupt is generated.

The zero-cross detection capability allows the user to make the 50–60Hz power signal the basis for system timing and to control voltage phase sensitive devices.



ZERO-CROSSING
DETECTION CIRCUIT

MODE0/MODE1-TERMINALS

The logic level applied to M0/M1-Terminals determines the memory map of μPD7810/7811 and the use of Port D/F as multiplexed Address/Data Bus.

M0	M1	MEMORY	ADDRESSES	LOCATION
0	1	4K	0 . . . . . FFFH	internal*
0	0	4K	0 . . . . . FFFH	external
0	1	16K	0 . . . . . 3FFFH	external
1	0	64K	0 . . . . . FEFFH	external

* M0, M1 = 0,1 realizes the ROM version (access of internal ROM), all others represent access of external memory only. In case external memory is used in addition to internal, memory mapping register has to be programmed then (see below).

MEMORY EXPANDES MODES	MEMORY MAPPING REGISTER			NUMBER OF I/O LINES
	MM2	MM1	MM0	
Port Mode	0	0	X	44
256 Expanded	0	1	0	36
4K Expanded	1	0	0	32
16K Expanded	1	1	0	30
60K Expanded	1	1	1	28

(using μPD7811)

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH ON CHIP A/D CONVERTER

DESCRIPTION

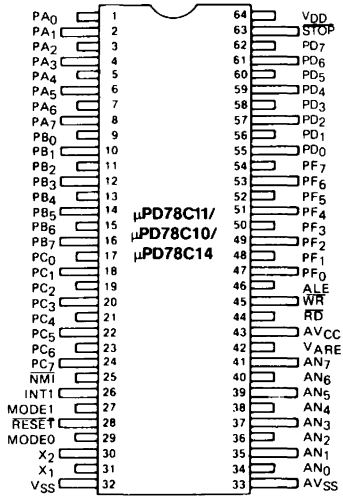
The NEC μPD78C10/C11/C14 is the CMOS version of the μPD7810/11 respectively.
The NEC μPD78C10/C11/C14 is a high-performance single-chip microcomputer integrating sophisticated on-chip peripheral functionality normally provided by external components. The devices's internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make up μPD78C10/C11/C14 appropriate in data processing as well as control applications. The device integrates a 16-bit ALU, 4K-ROM, 256-byte RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART and two zero-cross detect inputs on a single die, to direct the device into fast, high-end processing applications involving analog signal interface and processing.

The μPD78C11/C14 are the mask-ROM high volume production devices embedded with customer program. The μPD78C10 is a ROM-less version for prototyping and small volume production.

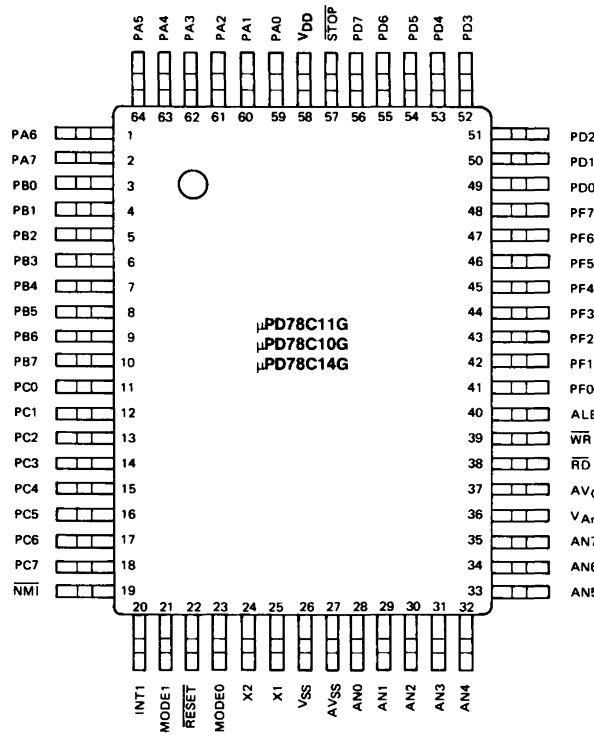
FEATURES

- Powerful Instruction Set Including 16-bit Multiply and Divide, 158 instructions
- High-Speed 1 μsec Cycle Time-12 MHz Operation
- On-Chip 4K-Byte ROM (78C11), 16K-Byte ROM (78C14), 256-Byte RAM
- 44 I/O Lines
- Easily Expandable Memory up to 60K Bytes/48K Bytes (externally)
- On-Chip 8-Bit A/D Converter-8 Input Channels
- Multi-Functional 16-Bit Timer/Counter
- Two Programmable 8-Bit Timers
- Full-Duplex Serial Communication Interface, synchronous and asynchronous
- Zero-Cross Detection Capability
- Vectored Interrupts, 3 external/8 internal
- Low Power Standby Operation
- 8085A Bus Compatible
- Singel Power Supply +5V, CMOS Technology
- Available in 64 Pin/68 Pin Packages (QUIL, FLAT, SHRINK DIP, PLCC)
- Standby functions
- On-chip clock generator
- 64K-Byte total memory address range

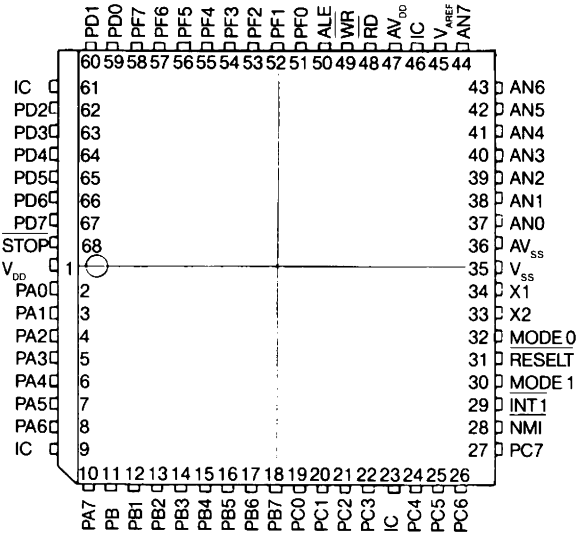
PIN CONFIGURATION
QUIL, SHRINK DIP



PIN CONFIGURATION FLAT PACKAGE



PIN CONFIGURATION
68-PIN PLCC PACKAGE



Note: IC = keep this pin open because of internal connection (external connection prohibited)

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION	
1–8	PA_0–PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode.	
9–16	PB_0–PB_7	Port B: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port B in input mode.	
17	PC_0	Port C: (Three-state input/output) 8-bit programmable I/O port. Each line independently pro-programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer, event-counter and external interrupts. Reset puts Port C in Port mode and all lines in input mode.	Transmit Data (TxD): Serial data output terminal.
18	PC_1		Receive Data (RxD): Serial data input terminal.
19	PC_2		Serial Clock ($\overline{SCK}$): Serial clock input/output terminal. When internal clock is used, the output can be selected; when an external clock is used, the input can be selected.
20	PC_3		Timer Input ((TI)/interrupt request input (INT2): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4		Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5		Counter Input (CI): External pulse input terminal to the timer/event counter.
23–24	PC_6, PC_7		Counter Outputs 0, 1 (CO_0–CO_1): Programmable rectangular wave output terminal based on timer/event counter.
25	$\overline{NMI}$	Falling-edge, nonmaskable interrupt ($\overline{NMI}$) input.	
26	INT1	This signal is a rising-edge, maskable interrupt input. This input is also used to make the zero-cross detection AC input.	
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 Signal during each opcode fetch.	
28	$\overline{RESET}$	(Input, active low), $\overline{RESET}$ initializes the μPD7811.	
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to output $\overline{IO}$/M.	
30–31	X_2, X_1 (crystal)	This is a crystal connection terminal for system clock oscillation. When an external clock is supplied X_1 is the input.	
32	V_{SS}	Power supply ground potential.	
33	AV_{SS}	A/D converter power supply ground potential. Sets conversion's range lower limit.	

PIN IDENTIFICATION (cont.)

PIN NO.	PIN SYMBOL	FUNCTION
34–41	AN_0–AN_7	Eight analog inputs to the A/D converter. AN_7–AN_4 can also be used as a digital input port for falling edge detection.
42	V_{AREF}	Reference voltage for A/D converter. Sets conversion's range upper limit.
43	AV_{CC}	Power supply voltage for A/D converter.
44	$\overline{RD}$	(Three-state output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes high during Reset.
45	$\overline{WR}$	(Three-state output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes high during Reset.
46	ALE	The strobe signal is for latching the address signal to the output from PD_7–PD_0 when accessing external expansion memory.
47–54	PF_0–PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55–62	DB_0–DB_7	Port D: 8-bit programmable I/O port. This byte can be designated as either input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	$\overline{STOP}$	Input pin for hardware stop mode
64	V_{DD}	+5V power supply.

Notes: 1 clock cycle = 1 CL = 3/f.
1 machine cycle = 3 or 4 clock cycles.
1 instruction cycle = 1 to 19 machine cycles.
f: System clock frequency (MHz).

NEW INSTRUCTIONS

In addition to the existing instruction set for μPD7801, the following new instructions are incorporated in the μPD78C10/C11/C14:

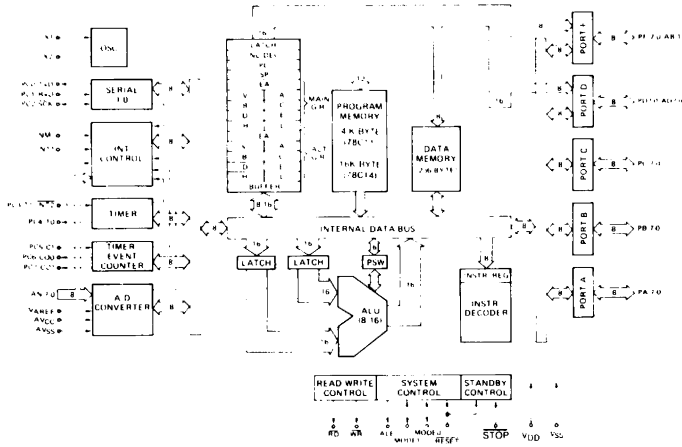
16-bit data transfer between memory and extended accumulator
16-bit data arithmetic and logical operation.

16-bit data addition and subtraction and 16-bit comparsion.
16-bit data shift and rotation
direct multiply and divide instructions.

8-bit by 8-bit division less then 8 μsec execution time.

16-bit divided by 8-bit less than 15 μsec execution
table look-up operation.
Register pair HL and DE are used as base register. Accumulator, B-register and extended accumulator are used as index register.
In addition to the 7811 instruction set, a STOP instruction is available.

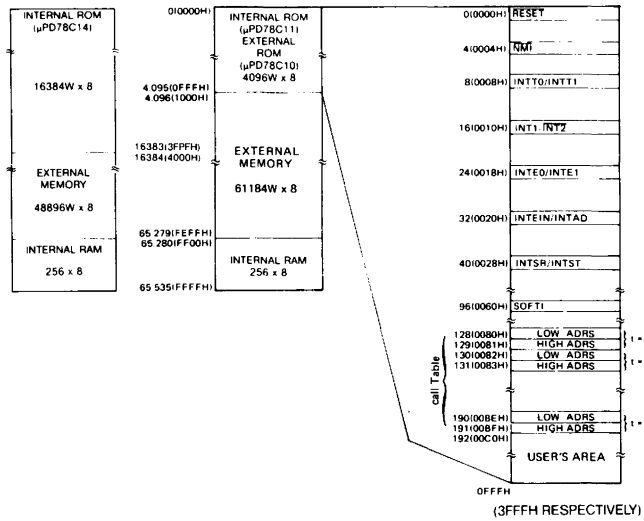
BLOCK DIAGRAM



Note: the μPD78C10 has no programmable ROM

MEMORY MAP

The μPD78C11 can directly address up to 64K-bytes of memory. Except for the on-chip ROM (0-4095) and RAM (65280-65535), any memory location can be used as ROM or RAM. The following memory map defines the 0-64K-byte memory space for the μPD78C11.



FUNCTIONAL DESCRIPTION

INPUT/OUTPUT

8 Analog Input Lines
44 Digital I/O Lines: five 8-bit ports (Port A, Port B, Port C, Port D, Port F) and 4 input lines (AN_4–AN_7)

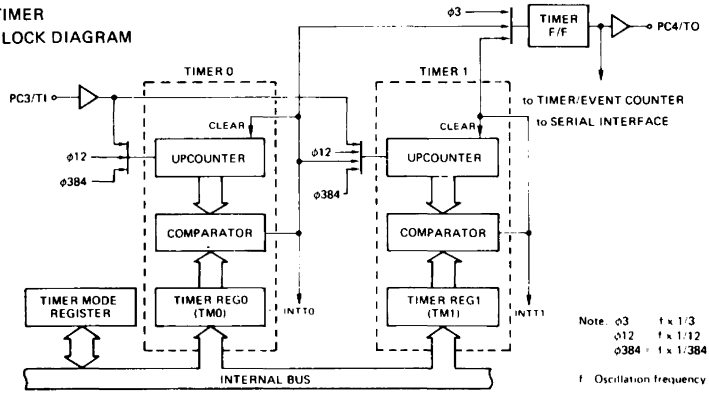
1. Analog Input Lines
   AN_0–AN_7 are configured as analog input lines for on-chip A/D converter.
2. Port Operation
   - Port A, Port B, Port C, Port F
     Each line of these ports can be individually programmed as an input or as an output. When used as I/O ports, all have latches outputs, high-impedance inputs.
   - Port D
     Port D can be programmed as a byte input or a byte output.
   - AN_4–AN_7
     The high-order analog input lines, AN_4–AN_7 can be used as digital input lines for falling edge detection.
3. Control Lines
   Under software control, each line of Port C can be configured individually to provide control lines for serial interface, timer and timer/counter, and interrupts.
4. Memory Expansion
   In addition to the single-chip operation mode the μPD78C11 has 4 memory expansion modes. Under software control, Port D can provide multiplexed low-order address and data bus and Port F can provide high-order address bus. The relation between memory expansion modes and the pin configurations of Port D and Port F is shown in the table that follows.

MEMORY EXPANSION		PORT CONFIGURATION
None	Port D	I/O Port
	Port F	I/O Port
256 Bytes	Port D	Multiplexed Address/Data Bus
	Port F	I/O Port
4K Bytes	Port D	Multiplexed Address/Data Bus
	Port F_0–F_3	Address Bus
	Port F_4–F_7	I/O Port
16K Bytes	Port D	Multiplexed/Data Bus
	Port F_0–F_5	Address Bus
	Port F_6–F_7	I/O Port
60K Bytes	Port D	Multiplexed Address/Data Bus
	Port F	Address Bus

TIMERS

The timer/event counter consists of two 8-bit timers. The timers may be programmed independently or may be cascaded and used as a 16-bit timer. The timer can be set by software to increment at intervals of 4 machine cycles (1μs at 12MHz operation) or 128 machine cycles (32μs at 12MHz), or to increment on receipt of a pulse at TI.

TIMER BLOCK DIAGRAM



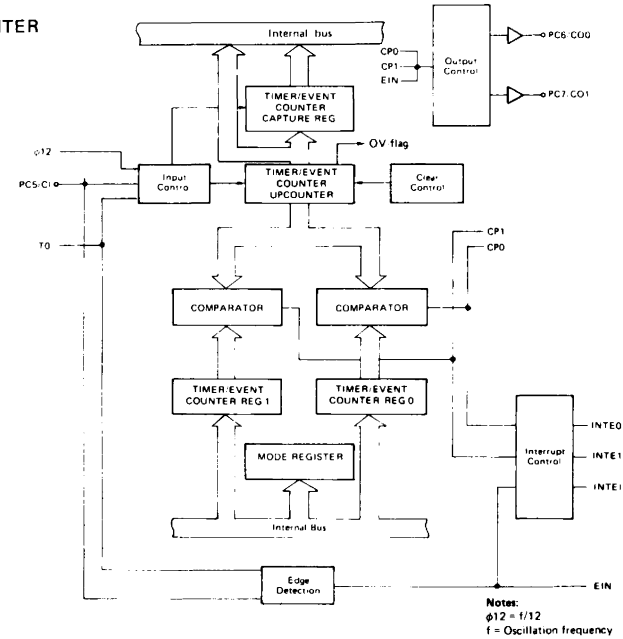
FUNCTIONAL DESCRIPTION (CONT.)

TIMER/EVENT COUNTER

The 16-bit Multifunctional timer/event counter can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse width measurement
- Programmable square-wave output
- Single pulse generation

TIMER/EVENT COUNTER BLOCK DIAGRAM

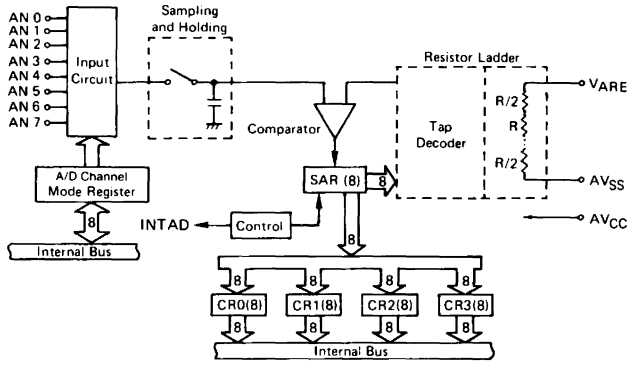


ANALOG/DIGITAL CONVERTER

- 8 Input Channels
- 4 Conversion Result Registers
- 2 Powerful Operation Modes
  - Auto Scan Mode
  - Channel Select Mode
- Successive Approximation Technique
- Absolute Accuracy ± 1.5 LSB (± 0.6%)
- Conversion Range 0 ~ 5V
- Conversion Time 50 μs
- Interrupt Generation

The μPD78C10/C11 features an 8-bit, high speed, high accuracy A/D converter. The A/D converter comprises a 256-Resistor Ladder and Successive Approximation Register (SAR). There are four conversion result registers (CR_0–CR_3). The 8-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR_0–CR_3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers.

A/D CONVERTER
BLOCK DIAGRAM



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There are 11 interrupt sources. Three are external interrupts and 8 are internal. These 11 interrupt sources are divided into 6 priority levels as shown in the table below.

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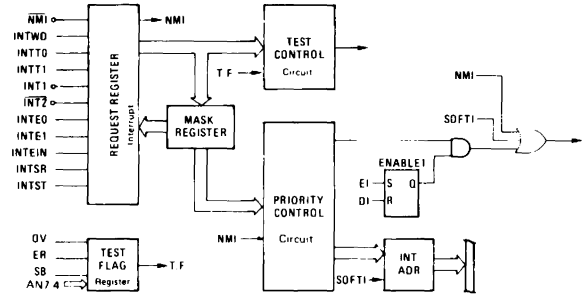
IRQ0	4	NMI	(Non-maskable interrupt)	External
IRQ1	8	INTT0 INTT1	(Coincidence signal from timer 0) (Coincidence signal from timer 1)	Internal
IRQ2	16	INT1 INT2	(Maskable intrrupt) (Maskable interrupr)	External
IRQ3	24	INTE0 INTE1	(Coincidence signal from timer/ event counter) Coincidence signal from timer/ event counter)	Internal
IRQ4	32	INTEIN INTAD	(Falling signal of C1 and T0 counter) (A/D converter interrupt)	In/External
IRQ5	40	INTSR INST	(Serial receive interrupt) (Serial send interrupt)	Internal

INTERRUPT CONTROL
BLOCK DIAGRAM



STANDBY FUNCTION

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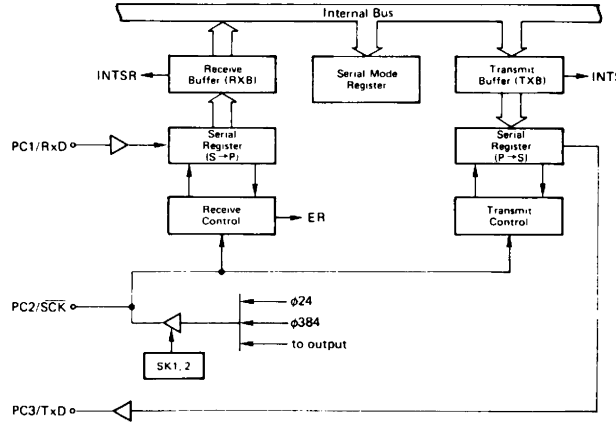
UNIVERSAL SERIAL INTERFACE

The serial interface can operate in any of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first for ease of communication with certain peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception. In the search mode, data are transferred one bit at a time from serial register to receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from serial register to transmit buffer occurs 8 bits at a time.

UNIVERSAL SERIAL INTERFACE BLOCK DIAGRAM



Note: $\phi 24 = \frac{1}{24}$

f: oscillation frequency (MHz)

$\phi 384 = \frac{1}{384}$

ZERO-CROSSING DETECTOR

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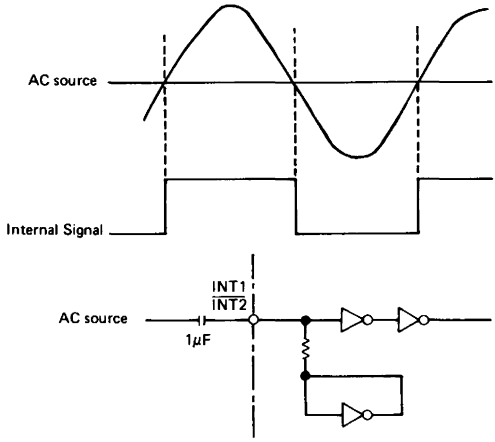
To utilize the zero-cross detection mode, an AC signal of approximately 1 – 1.8V peak-to-peak magnitude and a maximum frequency of 1kHz is coupled through an external capacitor to these pins.

For the INT1 pin, the internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one and INT1 interrupt is generated.

For the $\overline{INT2}$ pin, the state is sensed as a one until the falling edge crosses the DC average level, when it becomes a zero and $\overline{INT2}$ interrupt is generated.

The zero-cross detection capability allows the user to make the 50–60Hz power signal the basis for system timing and to control voltage phase sensitive devices.

In addition to the 7810/11 a register is implemented (ZCM = Zero Cross Mode Register) to allow to switch of the internal zero-cross detection circuit to reduce power consumption, especially during standby.



ZERO-CROSSING
DETECTION CIRCUIT

MODE0/MODE1-TERMINALS

The logic level applied to M0/M1-Terminals determines the memory map of μPD78C10/C11/C14 and the use of Port D/F as multiplexed Address/Data Bus.

M0	M1	MEMORY	ADDRESSES	LOCATION
0	1	4K	0 . . . . . FFFH	internal*
0	0	4K	0 . . . . . FFFH	external
0	1	16K	0 . . . . . 3FFFH	external
1	0	64K	0 . . . . . FEFFH	external

* M0, M1 = 0,1 realizes the ROM version (access of internal ROM), all others represent access of external memory only. In case external memory is used in addition to internal, memory mapping register has to be programmed then (see below).

MEMORY EXPANDES MODES	MEMORY MAPPING REGISTER MM2	MM1	MM0	NUMBER OF I/O LINES
Port Mode	0	0	X	44
256 Expanded	0	1	0	36
4K Expanded	1	0	0	32
16K Expanded	1	1	0	30
48K/60K Expanded	1	1	1	28

(using μPD7811)

Difference Between μPD78C11 and μPD7811

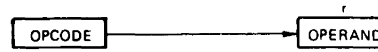
Item \ Product	μPD78C11	μPD7811
No. of instructions	159 (STOP instruction was added.)	158
No. of special registers	28 (ZCM register was added.)	27
Standby function	HALT MODE, software STOP mode, hardware STOP mode. In addition, in the software/hardware STOP mode, the internal RAM data (256 bytes) are retained at the power supply voltage as low as 2.5V	32 bytes of the 256-byte internal RAM data are retained at power supply voltage as low as 3.2V.
Control of zerocross detection circuit's selfbias	Available by setting the ZCM register	Not available
No. of states of the HLT instruction	12	11
Device construction	CMOS	NMOS
Power consumption: Operating	75mW TYP.	750mW TYP.
Power consumption: Standby	5μW TYP.	4.8mW TYP.
Pin configuration	V_{DD} : Pin 64 $\overline{STOP}$: Pin 63	V_{CC}: Pin 64 V_{DD}: Pin 63

ADDRESSING MODES AND INSTRUCTION SET
μCOM 87AD
(μPD7810/7811/78PG11/7810H/7811H/ 78C10/78C11/78C14)

ADDRESS MODES

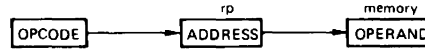
Register Addressing
Register Indirect Addressing
Auto-Increment Addressing
Auto-Decrement Addressing
Working Register Addressing
Direct Addressing
Immediate Addressing
Immediate Extended Addressing
Relative Addressing
Base Addressing
Base Index Addressing
Double Auto Increment Addressing

Register Addressing



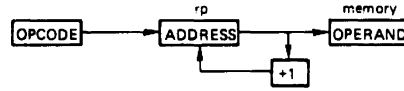
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are using this address mode.

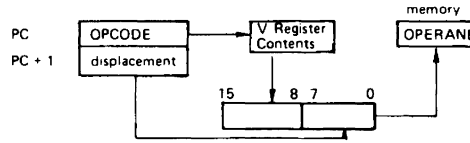
Auto-Increment Addressing



The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

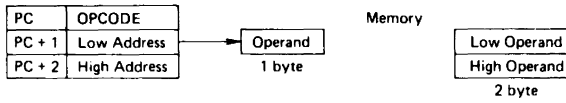
Auto Decrement Addressing

Working Register Addressing



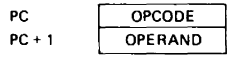
The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix are using this address mode.

Direct Addressing

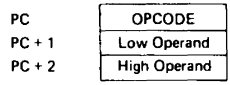


The two bytes following the opcode specify an address of a location containing the operand.

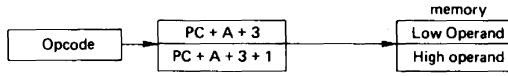
Immediate Addressing



Immediate Extended Addressing

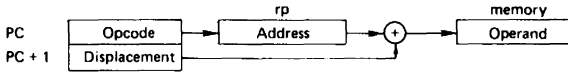


Relative Addressing



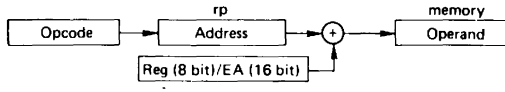
This addressing mode is used by the "Table"-command. It transfers the contents of 2 memory cells – addressed relatively to PC via the Accu A – into BC register-pair.
Application: Table look-up

Base-Addressing



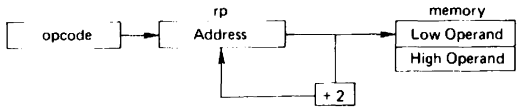
Register Pair DE or HL used as base pointer to the memory; immediate data (8 bit) or displacement added to the base.

Base-Index-Addressing



Register pair DE or HL used as base pointers to the memory; Register (8 bit) or Extended Accumulator (EA) as displacement added to the base.

Double auto increment



The opcode specifies the register pair which contains the memory address of the operand (16 bit). The contents of the register pair is automatically incremented by two to point to a new 16-bit operand.

μCOM 87 AD Instructionset

Operand Expression/Description

EXPRESSION	DESCRIPTION
r r1 r2	V, A, B, C, D, E, H, L EAH, EAL, B, C, D, E, H, L A, B, C
sr sr1 sr2 sr3 sr4	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TXB, TMO, TM1, ZCM (CMOS ONLY) PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM, RXB, CR0, CR1, CR2, CR3 PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM ETM0, ETM1 ECNT, ECPT
rp rp1 rp2 rp3	SP, B, D, H V, B, D, H, EA SP, B, D, H, EA B, D, H
rpa rpa1 rpa2 rpa3	B, D, H, D+, H+, D–, H– B, D, H B, D, H, D+, H+, D–, H–, D+byte, H+A, H+B, H+EA, H+byte D, H, D++, H++, D+byte, H+A, H+B, H+EA, H+byte
wa	8 bit immediate data
word byte bit	16 bit immediate data 8 bit immediate data 3 bit immediate data
f	CY, HC, Z
if	FNMI, FTO, FT1, F1, F2, FEO, FE1, FEIN, FAD, FSR, FST ER, OV, AN4, AN5, AN6, AN7, SB

Note 1

1. sr ~ sr4 (special register)

PA	:	PORT A	ECNT	:	TIMER/EVENT COUNTER UPCOUNTER
PB	:	PORT B			
PC	:	PORT C	ECPT	:	TIMER/EVENT COUNTER CAPTURE
PD	:	PORT D			
PF	:	PORT F	ETMM	:	TIMER/EVENT COUNTER MODE
MA	:	MODE A			
MB	:	MODE B	EOM	:	TIMER/EVENT COUNTER OUTPUT MODE
MC	:	MODE C			
MCC	:	MODE CONTROL C	ANM	:	A/D CHANNEL MODE
MF	:	MODE F	CRO	:	A/D CONVERSION RESULTO ~ 3
MM	:	MEMORY MAPPING	/		
TMO	:	TIMER REGO	CR3		
TM1	:	TIMER REG1	TXB	:	Tx BUFFER
TMM	:	TIMER MODE	RXB	:	Rx BUFFER
ETM0	:	TIMER/EVENT COUNTER REG0	SMH	:	SERIAL MODE High
			SML	:	SERIAL MODE Low
ETM1	:	TIMER/EVENT COUNTER REG1	MKH	:	MASK High
			MKL	:	MASK Low
ZCM	:	ZERO CROSS MODE (CMOS ONLY)			

2. rp ~ rp3 (register pair)

SP	:	STACK POINTER
B	:	BC
D	:	DE
H	:	HL
V	:	VA
EA	:	EXTENDED ACCUMULATOR

3. rpa ~ rpa3 (rp addressing)

B	:	(BC)
D	:	(DE)
H	:	(HL)
D+	:	$(DE)^{+}$
H+	:	$(HL)^{+}$
D−	:	$(DE)^{-}$
H−	:	$(HL)^{-}$
D++	:	$(DE)^{++}$
H++	:	$(HL)^{++}$
D+byte	:	(DE+byte)
H+A	:	(HL+A)
H+B	:	(HL+B)
H+EA	:	(HL+EA)
H+byte	:	(HL+byte)

4. f (flag)

CY	:	CARRY
HC	:	HALF CARRY
Z	:	ZERO

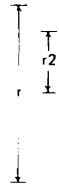
5. if (interrupt flag)

FNMI	:	INTFNMI
FT0	:	INTFT0
FT1	:	INTFT1
F1	:	INTF1
F2	:	INTF2
FE0	:	INTFE0
FE1	:	INTFE1
FEIN	:	INTFEIN
FAD	:	INTFAD
FSR	:	INTFSR
FST	:	INTFST
ER	:	ERROR
OV	:	OVERFLOW
AN4	:	ANALOG INPUT 4~7
/		
AN7	:	
SB	:	STANDBY

Description of Instruction Code Symbols

r

R_2	R_1	R_0	reg
0	0	0	V
0	0	1	A
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

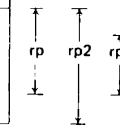


r1

T_2	T_1	T_0	reg
0	0	0	EAH
0	0	1	EAL
0	1	0	B
0	1	1	C
1	0	0	D
1	0	1	E
1	1	0	H
1	1	1	L

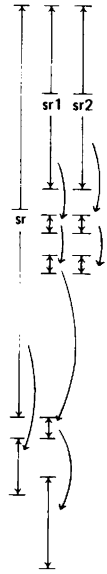
rp

P_2	P_1	P_0	reg-pair
0	0	0	SP
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA



sr

S_5	S_4	S_3	S_2	S_1	S_0	Special-reg
0	0	0	0	0	0	PA
0	0	0	0	0	1	PB
0	0	0	0	1	0	PC
0	0	0	0	1	1	PD
0	0	0	1	0	1	PF
0	0	0	1	1	0	MKH
0	0	0	1	1	1	MKL
0	0	1	0	0	0	ANM
0	0	1	0	0	1	SMH
0	0	1	0	1	0	SML
0	0	1	0	1	1	EOM
0	0	1	1	0	0	ETMM
0	0	1	1	0	1	TMM
0	1	0	0	0	0	MM
0	1	0	0	0	1	MCC
0	1	0	0	1	0	MA
0	1	0	0	1	1	MB
0	1	0	1	0	0	MC
0	1	0	1	1	1	MF
0	1	1	0	0	0	TXB
0	1	1	0	0	1	RXB
0	1	1	0	1	0	TM0
0	1	1	0	1	1	TM1
1	0	1	0	0	0	ZCM (CMOS)
1	0	0	0	0	0	CR0
1	0	0	0	0	1	CR1
1	0	0	0	1	0	CR2
1	0	0	0	1	1	CR3

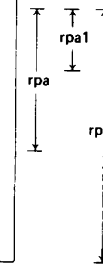


rp1

Q_2	Q_1	Q_0	reg-pair
0	0	0	VA
0	0	1	BC
0	1	0	DE
0	1	1	HL
1	0	0	EA

rpa

A_3	A_2	A_1	A_0	addressing
0	0	0	0	–
0	0	0	1	(BC)
0	0	1	0	(DE)
0	0	1	1	(HL)
0	1	0	0	$(DC)^+$
0	1	0	1	$(HL)^+$
0	1	1	0	$(DC)^-$
0	1	1	1	$(HL)^-$
1	0	1	1	(DE+byte)
1	1	0	0	(HL+A)
1	1	0	1	(HL+B)
1	1	1	0	(HL+EA)
1	1	1	1	(HL+byte)



rpa3

C_3	C_2	C_1	C_0	addressing
0	0	0	0	(DE)
0	0	0	1	(HL)
0	0	1	0	$(DE)^{++}$
0	0	1	1	$(HL)^{++}$
1	0	1	1	(DE+byte)
1	1	0	0	(HL+A)
1	1	0	1	(HL+B)
1	1	1	0	(HL+EA)
1	1	1	1	(HL+byte)

sr3

U_0	Special-reg
0	ETM0
1	ETM1

sr4

V_0	Special-reg
0	ECNT
1	ECPT

List of Mode Registers

MODE REGISTER	READ/WRITE	FUNCTION
MA register (Mode A)	W	An 8 bit register for designating the input/output of the port A in units of bit.
MB register (Mode B)	W	An 8 bit register for designating the input/output of the port B in units of bit.
MCC register (Mode Control C)	W	An 8 bit register for designating the port/control mode of the port C in units of bit.
MC register (Mode C)	W	An 8 bit register for designating the input/output of the port C in units of bit.
MM register (Memory Mapping)	W	A 4 bit register for designating the port/expansion mode od port D and port F.
MF register (Mode F)	W	An 8 bit register for designating the input of port F in units of bit.
TMM register (Timer Mode Reg.)	R/W	An 8 bit register for designating the operation mode of timer.
ETMM register (Timer/Event Counter Mode Reg.)	W	An 8 bit for designating the operation mode of timer/event counter.
EOM register (Timer/Event Counter Output Mode Reg.)	R/W	An 8 bit register for controlling the ouput level of CO0, CO1.
SMH register	R/W	7 bit and 8 bit registers for designating the operation mode of serial interface.
SML	W	
ANM register (A/D Channel Mode Reg.)	R/W	An 5 bit register for designating the operation mode of A/D converter and for indicating the input channel during A/D conversion.
ZCM register (Zero Cross Mode Reg.) CMOS only	W	A 2 bit register for switching on/off the internal zero cross detection circuit.

f

F_2	F_1	F_0	INTF
0	0	0	–
0	1	0	CY
0	1	1	HC
1	0	0	Z

if

I_4	I_3	I_2	I_1	I_0	INTF
0	0	0	0	0	INTENMI
0	0	0	0	1	INTFT0
0	0	0	1	0	INTFT1
0	0	0	1	1	INTF1
0	0	1	0	0	INTF2
0	0	1	0	1	INTFE0
0	0	1	1	0	INTFE1
0	0	1	1	1	INTFEIN
0	1	0	0	0	INTFAD
0	1	0	0	1	INTFSR
0	1	0	1	0	INTFST
0	1	0	1	1	ER
0	1	1	0	0	OV
1	0	0	0	0	AN4
1	0	0	0	1	AN5
1	0	0	1	0	AN6
1	0	0	1	1	AN7
1	0	1	0	0	SB

INSTRUCTION SET

	MNEMONIC		OPERAND	B1	OP CODE B2	B3	B4	STATE	OPERATION	SKIP CONDITION
8-BIT DATA TRANSFER			r1, A	00011 r_2 r_1 r_0				4	r1 ← A	
			A, r1	00001 r_2 r_1 r_0				4	A ← r1	
		*	sr, A	01001101	11 s_5 s_4 s_3 s_2 s_1 s_0			10	sr ← A	
		*	A, sr1	01001100	11 s_5 s_4 s_3 s_2 s_1 s_0			10	A ← sr1	
	MOV		r, word	01110000	01101 r_2 r_1 r_0	Low Adrs	High Adrs	17	r ← (word)	
			word, r	01110000	01111 r_2 r_1 r_0	Low Adrs	High Adrs	17	(word) ← r	
		*	r, byte	01101 r_2 r_1 r_0	Data			7	r ← byte	
	MVI		sr2, byte	01100100	$s_3$0000 s_2 s_1 s_0	Data		14	sr2 ← byte	
	MVIW	*	wa, byte	01110001	Offset	Data		13	(V, wa) ← byte	
	MVIX	*	rpa1, byte	01001 a_1 a_0	Data			10	(rpa1) ← byte	
	STAW	*	wa	01100011	Offset			10	(V, wa) ← A	
	LDAW	*	wa	00000001	Offset			10	A ← (V, wa)	
	STAX	*	rpa2	$a_3$0111 a_2 a_1 a_0	Data (*1)			7/13	(rpa2) ← A	
	LDAX	*	rpa2	$a_3$0101 a_2 a_1 a_0	Data (*1)			7/13	A ← (rpa2)	
	EXX			00010001				4	B ↔ B', C ↔ C', D ↔ D', E ↔ E', H ↔ H', L ↔ L'	
	EXA			00010000				4	V, A ↔ V', A', EA ↔ EA'	
	EXH			01010000				4	H, L ↔ H', L'	

	MNEMONIC		OPERAND	B1	OP CODE B2	B3	B4	STATE	OPERATION	SKIP CONDITION
16-BIT DATA TRANSFER	BLOCK		D*	00110001				13 x (C+1)	(DE)* ← (HL)*, C ← C−1 End if borrow	
	DMOV		rp3, EA	101101 p_1 p_0				4	$rp3_L$ ← EAL, $rp3_H$ ← EAH	
			EA, rp3	101001 p_1 p_0				4	EAL ← $rp3_L$, EAH ← $rp3_H$	
			sr3, EA	01001000	1101001 u_0			14	sr3 ← EA	
			EA, sr4	↓ ↓	1100000 v_0			14	EA ← sr4	
	SBCD		word	01110000	00011110	Low Adrs	High Adrs	20	(word) ← C, (word+1) ← B	
	SDED		word		00101110			20	(word) ← E, (word+1) ← D	
	SHLD		word		00111110			20	(word) ← L, (word+1) ← H	
	SSPD		word	↓ ↓	00001110	↓	↓	20	(word) ← SP_L, (word+1) ← SP_H	
	STEAX		rpa3	01001000	1001 c_3 c_2 c_1 c_0	Data (*2)		14/20	(rpa3) ← EAL, (rpa3+1) ← EAH	
	LBCD		word	01110000	00011111	Low Adrs	High Adrs	20	C ← (word), B ← (word+1)	
	LDED		word		00101111			20	E ← (word), D ← (word+1)	
	LHLD		word		00111111			20	L ← (word), H ← (word+1)	
	LSPD		word	↓ ↓	00001111	↓	↓	20	SP_L ← (word), SP_H ← (word+1)	
	LDEAX		rpa3	01001000	1000 c_3 c_2 c_1 c_0	Data (*2)		14/20	EAL ← (rpa3), EAH ← (rpa3+1)	
	PUSH		rp1	10110 q_2 q_1 q_0				13	(SP−1) ← $rp1_H$, (SP−2) ← $rp1_L$ SP ← SP−2	
	POP		rp1	10100 q_2 q_1 q_0				10	$rp1_L$ ← (SP), $rp1_H$ ← (SP+1) SP ← SP+2	
	LXI	*	rp2, word	0 p_2 p_1 p_0 0100	Low Byte	High Byte		10	rp2 ← word	

	MNEMONIC	OPERAND	OP CODE B1	B2	B3	B4	STATE	OPERATION	SKIP CONDITION
8 BIT ARITHMETIC (REGISTER)	TABLE		01001000	10101000			17	C ← (PC+3+A) B ← (PC+3+A+1)	
	ADD	A, r	01100000	11000 R_2 R_1 R_0			8	A ← A+r	
		r, A		01000 R_2 R_1 R_0			8	r ← r+A	
	ADC	A, r		11010 R_2 R_1 R_0			8	A ← A+r+CY	
		r, A		01010 R_2 R_1 R_0			8	r ← r+A+CY	
	ADDNC	A, r		10100 R_2 R_1 R_0			8	A ← A+r	No Carry
		r, A		00100 R_2 R_1 R_0			8	r ← r+A	No Carry
	SUB	A, r		11100 R_2 R_1 R_0			8	A ← A−r	
		r, A		01100 R_2 R_1 R_0			8	r ← r−A	
	SBB	A, r		11110 R_2 R_1 R_0			8	A ← A−r−CY	
		r, A		01110 R_2 R_1 R_0			8	r ← r−A−CY	
	SUBNB	A, r		10110 R_2 R_1 R_0			8	A ← A−r	No Borrow
		r, A		00110 R_2 R_1 R_0			8	r ← r−A	No Borrow
	ANA	A, r		10001 R_2 R_1 R_0			8	A ← A ∧ r	
		r, A		00001 R_2 R_1 R_0			8	r ← r ∧ A	
	ORA	A, r		10011 R_2 R_1 R_0			8	A ← A ∨ r	
		r, A		00011 R_2 R_1 R_0			8	r ← r ∨ A	
	XRA	A, r		10010 R_2 R_1 R_0			8	A ← A ∨̄ r	
		r, A		00010 R_2 R_1 R_0			8	r ← r ∨̄ A	
	GTA	A, r		10101 R_2 R_1 R_0			8	A−r−1	No Borrow
		r, A		00101 R_2 R_1 R_0			8	r−A−1	No Borrow

	MNEMONIC	OPERAND	OP CODE B1	B2	B3	B4	STATE	OPERATION	SKIP CONDITION
8 BIT ARITHMETIC (REG.)	LTA	A, r	01100000	10111 R_2 R_1 R_0			8	A−r	Borrow
		r, A		00111 R_2 R_1 R_0			8	r−A	Borrow
	NEA	A, r		11101 R_2 R_1 R_0			8	A−r	No Zero
		r, A		01101 R_2 R_1 R_0			8	r−A	No Zero
	EQA	A, r		11111 R_2 R_1 R_0			8	A−r	Zero
		r, A		01111 R_2 R_1 R_0			8	r−A	Zero
	ONA	A, r		11001 R_2 R_1 R_0			8	A ∧ r	No Zero
	OFFA	A, r		11011 R_2 R_1 R_0			8	A ∧ r	Zero
8 BIT ARITHMETIC (MEMORY)	ADDX	rpa	01110000	11000 A_2 A_1 A_0			11	A ← A+ (rpa)	
	ADCX	rpa		11010 A_2 A_1 A_0			11	A ← A+ (rpa)+CY	
	ADDNCX	rpa		10100 A_2 A_1 A_0			11	A ← A+ (rpa)	No Carry
	SUBX	rpa		11100 A_2 A_1 A_0			11	A ← A− (rpa)	
	SBBX	rpa		11110 A_2 A_1 A_0			11	A ← A− (rpa)−CY	
	SUBNBX	rpa		10110 A_2 A_1 A_0			11	A ← A− (rpa)	No Borrow
	ANAX	rpa		10001 A_2 A_1 A_0			11	A ← A ∧ (rpa)	
	ORAX	rpa		10011 A_2 A_1 A_0			11	A ← A ∨ (rpa)	
	XRAX	rpa		10010 A_2 A_1 A_0			11	A ← A ∨̄ (rpa)	
	GTAX	rpa		10101 A_2 A_1 A_0			11	A− (rpa) −1	No Borrow
	LTAX	rpa		10111 A_2 A_1 A_0			11	A− (rpa)	Borrow

	MNEMONIC	OPERAND	B1	B2	B3	B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	NEI	A, byte	01100111	← Data →			7	A byte	No Zero
		r, byte	01110100	01101 R_2 R_1 R_0	Data		11	r byte	No Zero
		sr2, byte	0110	S_3 1101 S_2 S_1 S_0			14	sr2 byte	No Zero
	EQI	A, byte	01110111	← Data →			7	A byte	Zero
		r, byte	01110100	01111 R_2 R_1 R_0	Data		11	r byte	Zero
		sr2, byte	0110	S_3 1111 S_2 S_1 S_0			14	sr2 byte	Zero
	ONI	A, byte	01000111	← Data →			7	A ∧ byte	No Zero
		r, byte	01110100	01001 R_2 R_1 R_0	Data		11	r ∧ byte	No Zero
		sr2, byte	0110	S_3 1001 S_2 S_1 S_0			14	sr2 ∧ byte	No Zero
	OFFI	A, byte	01010111	← Data →			7	A ∧ byte	Zero
		r, byte	01110100	01011 R_2 R_1 R_0	Data		11	r ∧ byte	Zero
		sr2, byte	0110	S_3 1011 S_2 S_1 S_0			14	sr2 ∧ byte	Zero
WORKING REGISTER	ADDW	wa	01110100	11000000	Offset		14	A ← A+(V wa)	
	ADCW	wa		1101			14	A ← A+(V wa)+CY	
	ADDNCW	wa		1010			14	A ← A+(V wa)	No Carry
	SUBW	wa		1110			14	A ← A−(V wa)	
	SBBW	wa		1111			14	A ← A−(V wa)−CY	
	SUBNBW	wa		1011			14	A ← A−(V wa)	No Borrow
	ANAW	wa		10001000			14	A ← A ∧ (V wa)	
	ORAW	wa		1001			14	A ← A ∨ (V wa)	

	MNEMONIC	OPERAND	B1	B2	B3	B4	STATE	OPERATION	SKIP CONDITION
WORKING REGISTER	XRAM	wa	01110100	10010000	Offset		14	A ← A ∨ (V wa)	
	GTAW	wa		10101000			14	A−(V wa)−1	No Borrow
	LTAW	wa		1011			14	A−(V wa)	Borrow
	NEAW	wa		1110			14	A−(V wa)	No Zero
	EQAW	wa		1111			14	A−(V wa)	Zero
	ONAW	wa		1100			14	A ∧ (V wa)	No Zero
	OFFAW	wa		1101			14	A ∧ (V wa)	Zero
	ANIW	wa, byte	00000101	← Offset →	Data		19	(V wa) ← (V wa) ∧ byte	
	ORIW	wa, byte	0001				19	(V wa) ← (V wa) ∨ byte	
	GTIW	wa, byte	0010				13	(V wa)−byte−1	No Borrow
	LTIW	wa, byte	0011				13	(V wa)−byte	Borrow
	NEIW	wa, byte	0110				13	(V wa)−byte	No Zero
	EQIW	wa, byte	0111				13	(V wa)−byte	Zero
	ONIW	wa, byte	0100				13	(V wa) ∧ byte	No Zero
	OFFIW	wa, byte	0101				13	(V wa) ∧ byte	Zero
16-BIT ARITHMETIC	EADD	EA, r2	01110000	010000 R_1 R_0			11	EA ← EA+r2	
	DADD	EA, rp3	0100	110001 P_1 P_0			11	EA ← EA+rp3	
	DADC	EA, rp3		1101			11	EA ← EA+rp3+CY	
	DADDNC	EA, rp3		1010			11	EA ← EA+rp3	No Carry
	ESUB	EA, r2	0000	011000 R_1 R_0			11	EA ← EA−r2	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	NEAX		rpa	01110000	11101 A_2 A_1 A_0			11	A ← (rpa)	No Zero
	EQAX		rpa		11111 A_2 A_1 A_0			11	A ← (rpa)	Zero
	ONAX		rpa		11001 A_2 A_1 A_0			11	A ∧ (rpa)	No Zero
	OFFAX		rpa	↓ ↓	11011 A_2 A_1 A_0			11	A ∧ (rpa)	Zero
	ADI	*	A, byte	01000110	← Data →			7	A ← A+byte	
			r, byte	01110100	01000 R_2 R_1 R_0	Data		11	r ← r+byte	
			sr2, byte	0110 ↓	S_3 1000 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	
	ACI	*	A, byte	01010110	← Data →			7	A ← A+byte+CY	
			r, byte	01110100	01010 R_2 R_1 R_0	Data		11	r ← r+byte+CY	
			sr2, byte	0110 ↓	S_3 1010 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte+CY	
	ADINC	*	A, byte	00100110	← Data →			7	A ← A+byte	No Carry
			r, byte	01110100	00100 R_2 R_1 R_0	Data		11	r ← r+byte	No Carry
			sr2, byte	0110 ↓	S_3 0100 S_2 S_1 S_0	↓		20	sr2 ← sr2+byte	No Carry
	SUI	*	A, byte	01100110	← Data →			7	A ← A−byte	
			r, byte	01110100	01100 R_2 R_1 R_0	Data		11	r ← r−byte	
			sr2, byte	0110 ↓	S_3 1100 S_2 S_1 S_0	↓		20	sr2 ← sr2−byte	
	SBI	*	A, byte	01110110	← Data →			7	A ← A−byte−CY	
			r, byte	01110100	01110 R_2 R_1 R_0	Data		11	r ← r−byte−CY	
			sr2, byte	0110 ↓	S_3 1110 S_2 S_1 S_0	↓		20	sr2 ← sr2−byte−CY	

	MNEMONIC		OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
IMMEDIATE DATA	SUINB	*	A, byte	00110110	← Data →			7	A ← A−byte	No Borrow
			r, byte	01110100	00110 R_2 R_1 R_0	Data		11	r ← r−byte	No Borrow
			sr2, byte	0110 ↓	S_3 0110 S_2 S_1 S_0	↓		20	sr2 ← sr2−byte	No Borrow
	ANI	*	A, byte	00000111	← Data →			7	A ← A ∧ byte	
			r, byte	01110100	00001 R_2 R_1 R_0	Data		11	r ← r ∧ byte	
			sr2, byte	01100100	S_3 0001 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∧ byte	
	ORI	*	A, byte	00010111	← Data →			7	A ← A ∨ byte	
			r, byte	01110100	00011 R_2 R_1 R_0	Data		11	r ← r ∨ byte	
			sr2, byte	0110 ↓	S_3 0011 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨ byte	
	XRI	*	A, byte	00010110	← Data →			7	A ← A ∨ byte	
			r, byte	01110100	00010 R_2 R_1 R_0	Data		11	r ← r ∨ byte	
			sr2, byte	0110 ↓	S_3 0010 S_2 S_1 S_0	↓		20	sr2 ← sr2 ∨ byte	
	GTI	*	A, byte	00100111	← Data →			7	A −byte−1	No Borrow
			r, byte	01110100	00101 R_2 R_1 R_0	Data		11	r −byte−1	No Borrow
			sr2, byte	0110 ↓	S_3 0101 S_2 S_1 S_0	↓		14	sr2 −byte 1	No Borrow
	LTI	*	A, byte	00110111	← Data →			7	A byte	Borrow
			r, byte	01110100	00111 R_2 R_1 R_0	Data		11	r −byte	Borrow
			sr2, byte	0110 ↓	S_3 0111 S_2 S_1 S_0	↓		14	sr2 byte	Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
16-BIT ARITHMETIC	DSUB	EA, rp3	01110100	111001 P_1 P_0			11	EA ← EA − rp3	
	DSBB	EA, rp3		1111			11	EA ← EA − rp3 − CY	
	DSUBNB	EA, rp3		1011			11	EA ← EA − rp3	No Borrow
	DAN	EA, rp3		100011 P_1 P_0			11	EA ← EA ∧ rp3	
	DOR	EA, rp3		1001			11	EA ← EA ∨ rp3	
	DXR	EA, rp3		100101 P_1 P_0			11	EA ← EA ∨ rp3	
	DGT	EA, rp3		101011 P_1 P_0			11	EA − rp3 − 1	No Borrow
	DLT	EA, rp3		1011			11	EA − rp3	Borrow
	DNE	EA, rp3		1110			11	EA − rp3	No Zero
	DEQ	EA, rp3		1111			11	EA − rp3	Zero
	DON	EA, rp3		1100			11	EA ∧ rp3	No Zero
	DOFF	EA, rp3		1101			11	EA ∧ rp3	Zero
MULTIP. DIVIDE	MUL	r2	01001000	001011 R_1 R_0			32	EA ← A × r2	
	DIV	r2		0011			59	EA ← EA ÷ r2, r2 ← surplus	
INCREMENT/ DECREMENT	INR	r2	010000 R_1 R_0				4	r2 ← r2+1	Carry
	INRW *	wa	00100000	← Offset →			16	(V.wa) ← (V.wa)+1	Carry
	INX	rp	00 P_1 P_0 0010				7	rp ← rp+1	
		EA	10101000				7	EA ← EA+1	
	DCR	r2	010100 R_1 R_0				4	r2 ← r2 − 1	Borrow
	DCRW *	wa	00110000	← Offset →			16	(V.wa) ← (V.wa) − 1	Borrow

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
ROTATE AND SHIFT	DCX	rp	00 P_1 P_0 0011				7	rp ← rp − 1	
		EA	10101001				7	EA ← EA − 1	
	RLL	r2	01001000	001101 R_1 R_0			8	$r2_{m+1}$ ← $r2_m$, $r2_0$ ← CY, CY ← $r2_7$	
	RLR	r2		00 R_1 R_0			8	$r2_{m-1}$ ← $r2_m$, $r2_7$ ← CY, CY ← $r2_0$	
	SLL	r2		001001 R_1 R_0			8	$r2_{m+1}$ ← $r2_m$, $r2_0$ ← 0, CY ← $r2_7$	
	SLR	r2		00 R_1 R_0			8	$r2_{m-1}$ ← $r2_m$, $r2_7$ ← 0, CY ← $r2_0$	
	SLLC	r2		000001 R_1 R_0			8	$r2_{m+1}$ ← $r2_m$, $r2_0$ ← 0, CY ← $r2_7$	Carry
	SLRC	r2		00 R_1 R_0			8	$r2_{m-1}$ ← $r2_m$, $r2_7$ ← 0, CY ← $r2_0$	Carry
	DRLL	EA		10110100			8	EA_{n+1} ← EA_n, EA_0 ← CY, CY ← EA_{15}	
	DRLR	EA		0000			8	EA_{n-1} ← EA_n, EA_{15} ← CY, CY ← EA_0	
	DSLL	EA		10100100			8	EA_{n+1} ← EA_n, EA_0 ← 0, CY ← EA_{15}	
	DSLR	EA		0000			8	EA_{n-1} ← EA_n, EA_{15} ← 0, CY ← EA_0	
	DAA		01100001				4	Decimal Adjust Accumulator	
	STC		01001000	00101011			8	CY ← 1	
	CLC			00101010			8	CY ← 0	
	NEGA			00111010			8	A ← A+1	
	RLD		01001000	00111000			17	Rotate Left Digit	
	RRD			1001			17	Rotate Right Digit	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
JUMP	JMP *	word	01010100	← Low Adrs →	High Adrs		10	PC ← word	
	JB		00100001				4	PC_H ← B, PC_L ← C	
	JR	word	11 ← jdispl →				10	PC ← PC+1+jdispl	
	JRE *	word	0100111 ←	jdisp →			10	PC ← PC+2+jdispl	
	JEA		01001000	00101000			8	PC ← EA	
CALL	CALL *	word	01000000	← Low adrs →	High Adrs		16	$(SP-1) \leftarrow (PC+3)_H$, $(SP-2) \leftarrow (PC+3)_L$, PC ← word, SP ← SP−2	
	CALB		01001000	00101001			17	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$, PC_H ← B, SP ← SP−2, PC_L ← C	
	CALF *	word	01111 ←	fa →			13	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$, PC_{15-11} ← 00001, PC_{10-0} ← fa, SP ← SP−2	
	CALT	word	100 ← ta →				16	$(SP-1) \leftarrow (PC+1)_H$, $(SP-2) \leftarrow (PC+1)_L$, $PC_L \leftarrow (128+2ta)$, $PC_H \leftarrow (129+2ta)$, SP ← SP−2	
	SOFTI		01110010				16	$(SP-1) \leftarrow PSW$, $(SP-2) \leftarrow (PC+1)_H$, $(SP-3) \leftarrow (PC+1)_L$, PC ← 0060H, SP ← SP−3	

	MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
RETURN	RET		10111000				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, SP ← SP+2	
	RETS		1001				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, SP ← SP+2, PC ← PC+n	
	RETI		01100010				13	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, PSW ← (SP+2), SP ← SP+3	Unconditional
SKIP	SK *	f	01001000	00001 F_2 F_1 F_0			8	Skip if f=1	f=1
	SKN *	f		0001			8	Skip if f=0	f=0
	SKIT *	irf		010 I_4 I_3 I_2 I_1 I_0			8	Skip if irf=1, then reset irf	irf=1
	SKNIT *	irf		011 I_4 I_3 I_2 I_1 I_0			8	Skip if irf=0 Reset irf, if irf=1	irf=0
CPU CONTROL	NOP		00000000				4	No Operation	
	EI		10101010				4	Enable Interrupt	
	DI		10111010				4	Disable Interrupt	
	HLT		01001000	00111011			11	Halt	

Notes:

(*1) B2(Data) rpa2 = D+byte, H+byte
(*2) B3(Data) rpa3 = D+byte, H+byte
(*3) right side of slash (/) in states indicates case rpa2, rpa3 = D+byte, H+A, H+B, H+EA, H+byte
(*4) in the case of skip condition, the idle states are as follows

1-byte instruction	4 states	2-byte instruction (with *1	7 states
2-byte instruction	8 states	3-byte instruction (with *1	10 states
3-byte instruction	11 states	4 byte instruction	14 states

Additional instruction for μPD78C10/C11/C14:

MNEMONIC	OPERAND	OP CODE B1	OP CODE B2	OP CODE B3	OP CODE B4	STATE	OPERATION	SKIP CONDITION
STOP		01001000	10111011			12	Stop	

ELECTRICAL SPECIFICATIONS

AND PACKAGE OUTLINES FOR

μPD7810/7811/78PG11E

ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
	AV_{CC}		−0.5 to +7.0	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Reference Input Voltage	V_{AREF}		−0.5 to V_{CC}	V
Operating Temperature	T_{opt}	10 MHz < f_{XTAL} ≤ 12 MHz	−10 to +70	°C
		f_{XTAL} ≤ 10 MHz	−40 to + 85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

PARAMETER / OSC. FREQ.	T_a	V_{CC}, AV_{CC}
10 MHz < f_{XTAL} ≤ 12 MHz	−10°C to +70°C	+5.0V ± 5 %
f_{XTAL} ≤ 10 MHz	−40°C to +85°C	+5.0V ± 10 %

CAPACITANCE

(T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_c = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except SCK, RESET, X1 and X2	2.0		V_{CC}	V
	V_{IH2}	SCK, X1, X2 *1	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	RESET	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3): 0.45V ≤ V_{IN} ≤ V_{CC}			±200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_{IN} ≤ V_{CC}			±10	μA
Output Leakage Current	I_{LO}	0.45V ≤ V_O ≤ V_{CC}			±10	μA
AV_{CC} Supply Current	AI_{CC}			6	12	mA
V_{DD} Supply Current	I_{DD}	μPD7811, 7810		15 *2	32	mA
		μPD78PG11E		15 *2	32	mA
V_{CC} Supply Current	I_{CC}	μPD7811,7810		150 *2	200	mA
		μPD78PG11E		140 *2	230	mA
Data Retention Voltage	V_{DDDR}	V_{CC} = 0V, RESET = V_{IL}	3.2			V

*2 T_a = 25 C, V_{CC} = V_{DD} = +5.0V

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE ↓	t_{AL}		65		ns
Address Hold from ALE ↓	t_{LA}		50		ns
Address to RD ↓ Delay Time	t_{AR}		150		ns
RD ↑ to Address Floating	t_{AFR}			20	ns
Address to Data Input	t_{AD}			360	ns
ALE ↓ to Data Input	t_{LDR}			215	ns
RD↓ to Data Input	t_{RD}			180	ns
ALE ↓ to RD ↓ Delay Time	t_{LR}		35		ns
Data Hold Time from RD ↑	t_{RDH}		0		ns
RD ↑ to ALE↑ Delay Time	t_{RL}		115		ns
RD Width Low	t_{RR}	Data Read	280		ns
		OP Code Fetch	530		ns
ALE Width High	t_{LL}		125		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*3, *6	65		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*3, *6	50		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*3, *7	65		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*3, *7	50		ns
Adress to WR ↓ Delay	t_{AW}		150		ns
ALE ↓ to Data Output	t_{LDW}			195	ns
WR ↓ to Data Output	t_{WD}			100	ns
ALE ↓ to WR ↓ Delay Time	t_{LW}		35		ns
Data Setup Time to WR ↑	t_{DW}		230		ns
Data Hold Time from WR ↑	t_{WDH}		95		ns
WR ↑ to ALE ↑ Delay Time	t_{WL}		115		ns
WR Width Low	t_{WW}		280		ns
Address to Data Input Delay	t_{ACC}	78PG11E only		360	ns

Note 1: f_{XTAL} = 10 MHz

2: Load Capacitance, C_L = 150pF

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
SCK Cycle Time	t_{CYK}	SCK Input	*8	1.66		μs
			*9	500		ns
		SCK Output		2		μs
SCK Width Low	t_{KKL}	SCK Input	*8	750		ns
			*9	200		ns
		SCK Output		900		μs
SCK Width High	t_{KKH}	SCK Input	*8	750		ns
			*9	200		ns
		SCK Output		900		ns
RxD Setup Time to SCK ↑	t_{RXK}	*8		80		ns
RxD Hold Time from SCK ↑	t_{KRX}	*8		80		ns
SCK ↓ to TxD Delay Time	t_{KTX}	*8			210	ns

*8: 1x Baud Rate in Asynchronous, Synchronous, I/O Interface Mode

*9: 16x Baud Rate or 64x Baud Rate in Asynchronous

ZERO-CROSS CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

A/D CONVERTER CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = AV_{CC} = +5.0V ± 5 %, V_{SS} = AV_{SS} = 0V, AV_{CC} −0.5 ≤ V_{AREF} ≤ AV_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	Min	TYP		UNITS
Resolution			8			Bits
Absolute Accuracy		T_a = −10°C to +50°C 83ns ≤ t_{CYC} ≤ 170ns			0.4% ± 1/2	LSB
		83ns ≤ t_{CYC} ≤ 170ns			0.6% ± 1/2	LSB
Conversion Time	t_{CONV}	83ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	83ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
V_{AREF} Current	I_{AREF}		0.2	0.5	1.5	mA

DC CHARACTERISTICS

(T_a = -40°C to +85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} − 0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except SCK, RESET, X1, X2	2.0		V_{CC}	V
	V_{IH2}	$\overline{SCK}$, X1, X2 *1	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	$\overline{RESET}$	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3); +0.45V ≤ V_{IN} ≤ V_{CC}			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) 0V ≤ V_{IN} ≤ V_{CC}			± 10	μA
Output Leakage Current	I_{LO}	0.45V≤V_O≤V_{CC}			± 10	μA
AV_{CC} Supply Current	AI_{CC}			6	12	mA
V_{DD} Supply Current	I_{DD}	μPD7811, 7810		1.5 *2	3.5	mA
		μPD78PG11E		1.5 *2	3.5	mA
V_{CC} Supply Current	I_{CC}	μPD7811,7810		150 *2	220	mA
		μPD78PG11E		140 *2	250	mA
Data Retention Voltage	V_{DDDR}	V_{CC} = 0V, $\overline{RESET}$ = V_{IL}	3.2			V

AC CHARACTERISTICS READ/WRITE OPERATION

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		100	250	ns
Address Setup to ALE ↓	t_{AL}		100		ns
Address Hold from ALE ↓	t_{LA}		70		ns
Address to RD ↓ Delay Time	t_{AR}		200		ns
RD ↑ to Address Floating	t_{AFR}			20	ns
Address to Data Input	t_{AD}			480	ns
ALE ↓ to Data Input	t_{LDR}			300	ns
RD↓ to Data Input	t_{RD}			250	ns
ALE ↓ to RD ↓ Delay Time	t_{LR}		50		ns
Data Hold Time from RD ↑	t_{RDH}		0		ns
RD ↑ to ALE↑ Delay Time	t_{RL}		150		ns
RD Width Low	t_{RR}	Data Read	350		ns
		OP Code Fetch	650		ns
ALE Width High	t_{LL}		160		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}	*6	100		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}	*6	70		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}	*7	100		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}	*7	70		ns
Adress to WR ↓ Delay	t_{AW}		200		ns
ALE ↓ to Data Output	t_{LDW}			210	ns
WR ↓ to Data Output	t_{WD}			100	ns
ALE ↓ to WR ↓ Delay Time	t_{LW}		50		ns
Data Setup Time to WR ↑	t_{DW}		300		ns
Data Hold Time from WR ↑	t_{WDH}		130		ns
WR ↑ to ALE ↑ Delay Time	t_{WL}		150		ns
WR Width Low	t_{WW}		350		ns
Address to Data Input Delay	t_{ACC}	78PG11E only		480	ns

Note 1 t_{XTAL} = 10 MHz

2 Load Capacitance, C_L = 150pF

SERIAL OPERATION

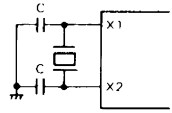
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*8	2.0		μs
			*9	500		ns
		$\overline{SCK}$ Output		2.4		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*8	920		ns
			*9	200		ns
		$\overline{SCK}$ Output		1.1		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*8	920		ns
			*9	200		ns
		$\overline{SCK}$ Output		1.1		μs
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*8		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*8		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*8			210	ns

ZERO-CROSS CHARACTERISTICS

(T_a = −40°C to +85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

*1 The following oscillation circuit using XTAL is recommended



C: 10 pF

*2 T_a = +25 °C, V_{CC} = V_{DD} = 5 V

*3 f_{XTAL} = 12 MHz

*4 f_{XTAL} = 10 MHz

*5 Load capacitance : C_L = 150 pF

*6 MODE0, MODE1 pins are connected to V_{CC} through R in μPD7810, μPD7811, μPD78PG11E

*7 MODE0, MODE1 pins are connected to V_{CC} through R in μPD7810

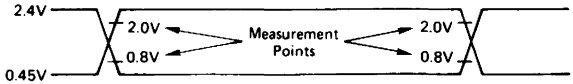
*8 1xBaud Rate in Asynchronous, Synchronous, I/O Interface Mode

*9 16x, 64x Baud Rate in Asynchronous

A/D CONVERTER CHARACTERISTICS

(T_a = −40°C to +85°C, V_{CC} = AV_{CC} = +5.0V ± 10%, V_{SS} = AV_{SS} = 0V, AV_{CC} − 0.5V ≤ V_{AREF} ≤ AV_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	Min	TYP		UNITS
Resolution			8			Bits
Absolute Accuracy		T_a = −10°C to +50°C 100ns ≤ t_{CYC} ≤ 170ns			0.4% ± 1/2	LSB
		100ns ≤ t_{CYC} ≤ 170ns			0.6% ± 1/2	LSB
Conversion Time	t_{CONV}	100ns ≤ t_{CYC} ≤ 170ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	100ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
V_{AREF} Current	I_{AREF}		0.2	0.5	1.5	mA



AC TIMING MEASUREMENT POINT

BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220	MAX	ns
t_{LDR}	5T − 200	MAX	ns
t_{RD}	4T − 150	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read) 7T − 50 (OP Code Fetch)	MIN	ns
t_{LL}	2T − 40	MIN	ns
t_{ML} *2	2T − 100	MIN	ns
t_{LM} *2	T − 30	MIN	ns
t_{IL} *3	2T − 100	MIN	ns
t_{LI} *3	T − 30	MIN	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50	MIN	ns
t_{CYK}	20T ($\overline{SCK}$ Input) *1 24T ($\overline{SCK}$ Output)	MIN	ns
t_{KKL}	10T − 80 ($\overline{SCK}$ Input) *1 12T − 100 ($\overline{SCK}$ Output)	MIN	ns
t_{KKH}	10T − 80 ($\overline{SCK}$ Input) *1 12T − 100 ($\overline{SCK}$ Output)	MIN	ns

*1 1x Baud Rate in Asynchronous, Synchronous, I/O Interface Mode
*2 MODE0, MODE1 pins are connected to V_{CC} through R
*3 MODE0, MODE1 pins are connected to V_{CC} through R in μPD7810

Note T = t_{CYC} = $1/f_{XTAL}$

OTHER OPERATIONS

(T_a = -10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} -0.8V ≤ V_{DD} ≤ V_{CC})
(T_a = -40°C to +85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} -0.8V ≤ V_{DD} ≤ V_{CC})

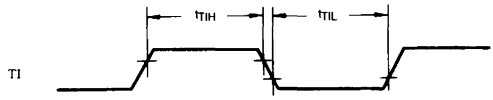
Parameter	Symbol	Conditions	MIN	MAX	UNITS
TI width high, low	t_{TIH}, t_{TIL}		6		t_{CYC}
CI width high, low	t_{CI1H}, t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ width high, low	t_{NIH}, t_{NIL}		36		t_{CYC}
INT1 width high, low	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ width high, low	t_{I2H}, t_{I2L}		36		t_{CYC}
$\overline{RESET}$ width high, low	t_{RSH}, t_{RSL}		60		t_{CYC}

EXTERNAL CLOCK TIMING

(T_a = -10°C to +70°C, V_{CC} = +5.0V ± 5%, V_{SS} = 0V, V_{CC} -0.8V ≤ V_{DD} ≤ V_{CC})
(T_a = -40°C to +85°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} -0.8V ≤ V_{DD} ≤ V_{CC})

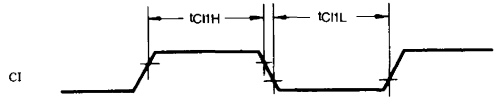
Parameter	Symbol	Twst Conditions	MIN	MAX	UNITS
X1 input width high	t_{OH}		30	250	ns
X1 input width low	t_{OL}		30	250	ns
X1 input rise time	t_r		0	30	ns
X1 input fall time	t_f		0	30	ns

TIMER INPUT TIMING

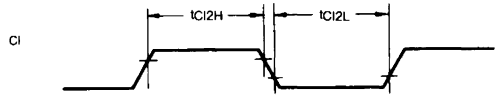


TIMER/EVENT COUNTER INPUT TIMING

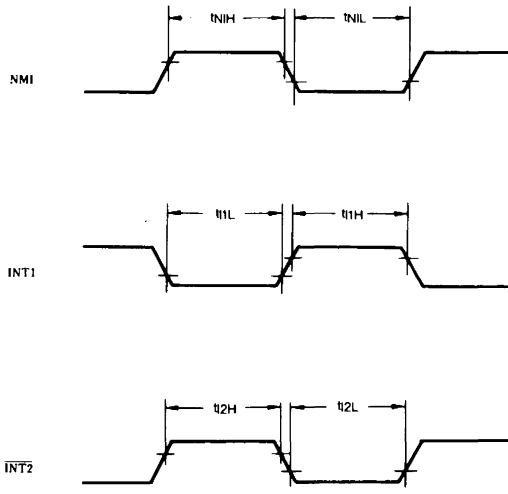
EVENT COUNT MODE



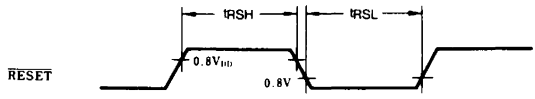
PULSE WIDTH MEASUREMENT MODE



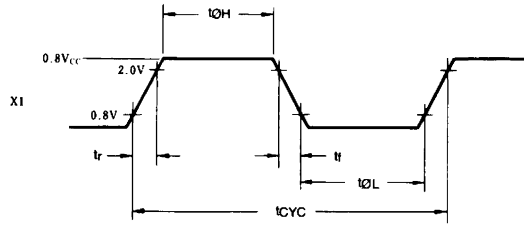
INTERRUPT INPUT TIMING



RESET INPUT TIMING



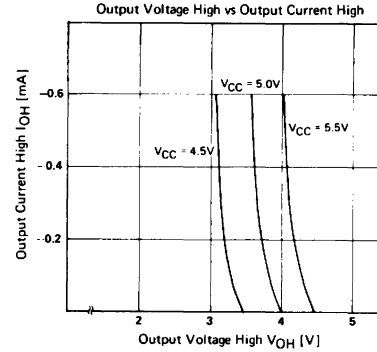
EXTERNAL CLOCK TIMING



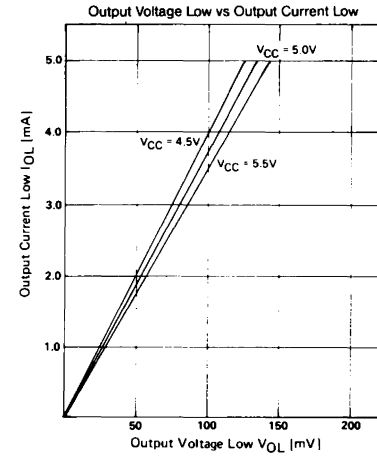
CHARACTERISTICS CURVE
– REFERENCE –

(T_a = 25°C)

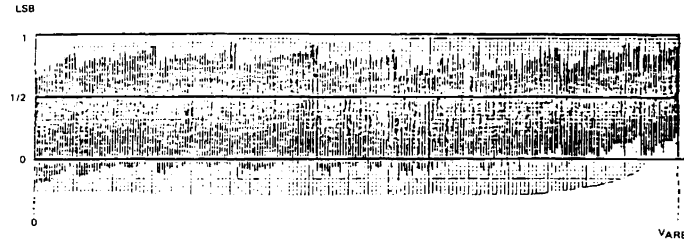
Output Voltage High vs Output Current High



Output Voltage Low vs Output Current Low

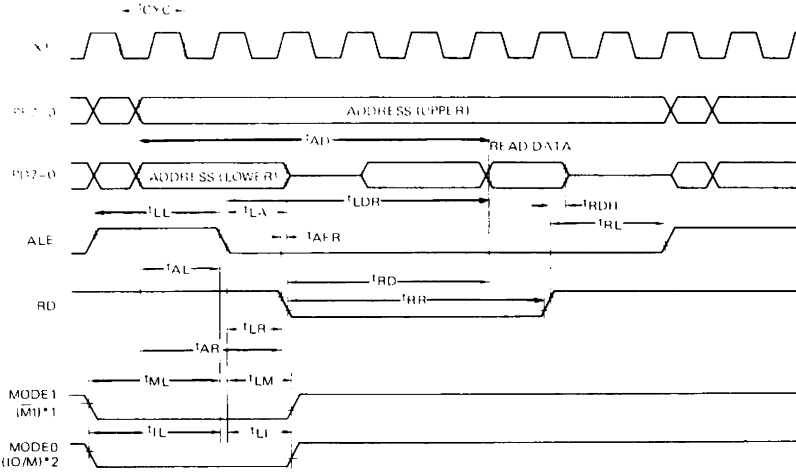


CHARACTERISTIC OF A/D CONVERTER



TIMING WAVEFORM

Read Operation

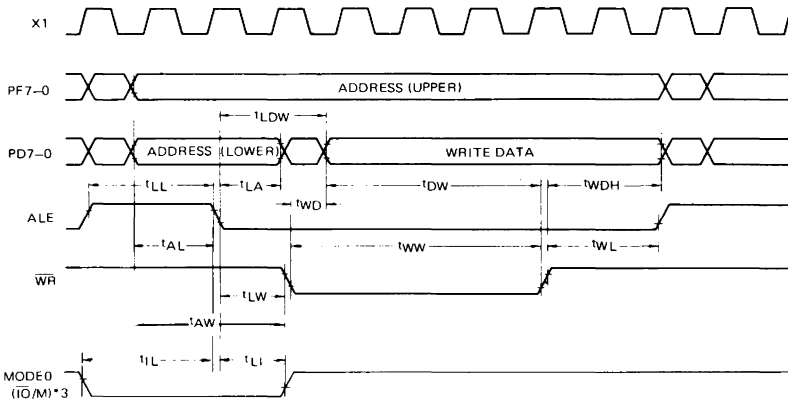


*1 $\overline{M_1}$ is output at the fetch cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

*2 $\overline{IO}$/M is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

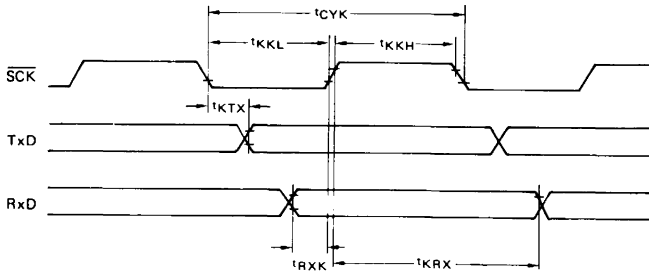
TIMING WAVEFORM

Write Operation

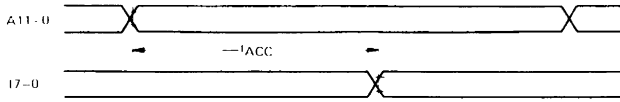


*3 $\overline{IO}$/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

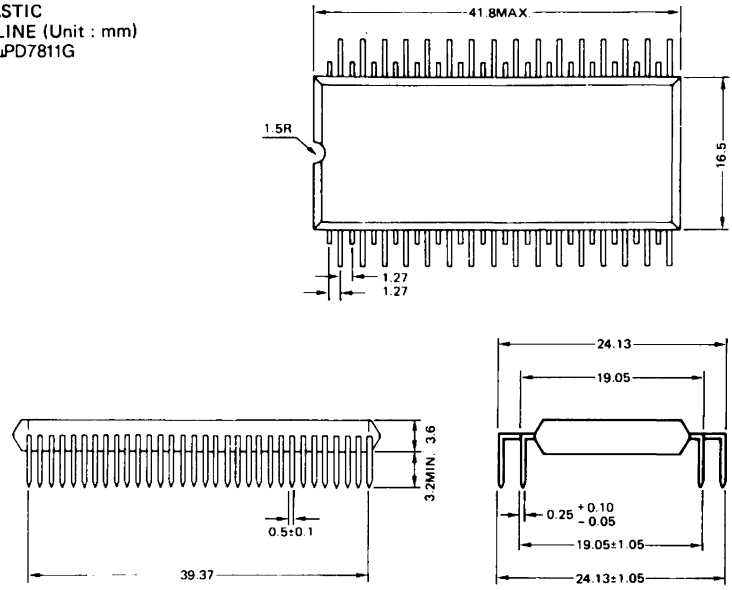
Serial Operation



EPROM Timing (for μPD78PG11E)

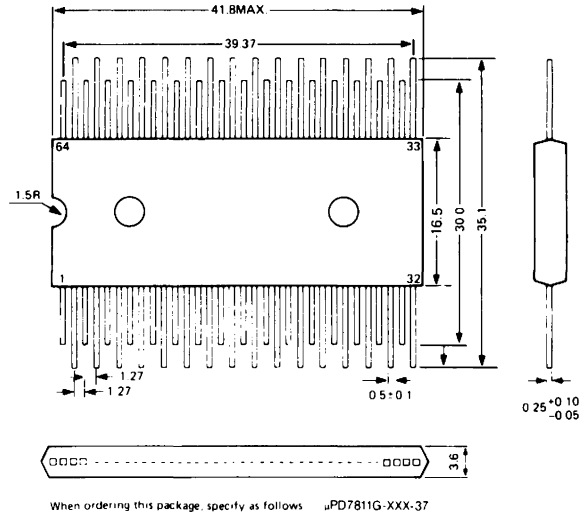


64 PIN PLASTIC
QUIP OUTLINE (Unit : mm)
μPD7801G/μPD7811G



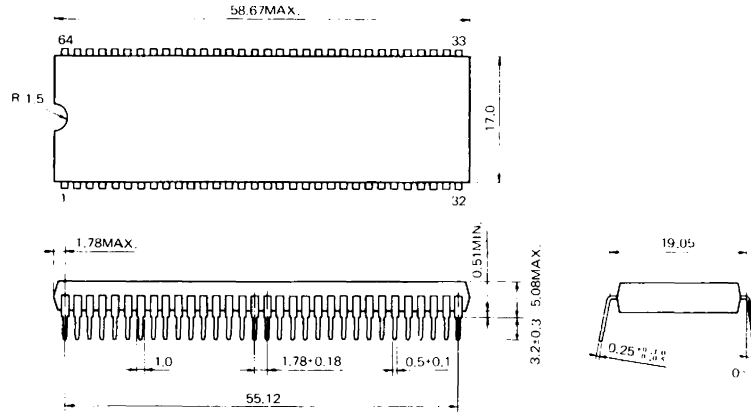
When ordering this package, specify as follows:
μPD7810G-36
μPD7811G-xxx-36

64 PIN PLASTIC QUIP OUTLINE
FLAT LEADS
(Unit : mm)
μPD7811G



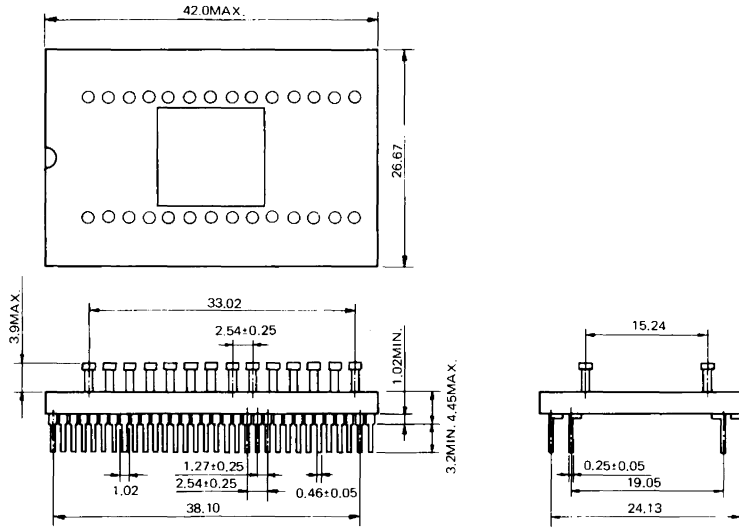
When ordering this package, specify as follows μPD7811G-XXX-37

64 PIN PLASTIC
SHRINK DIP OUTLINE (Unit : mm)
μPD 7810CW/μPD7811CW

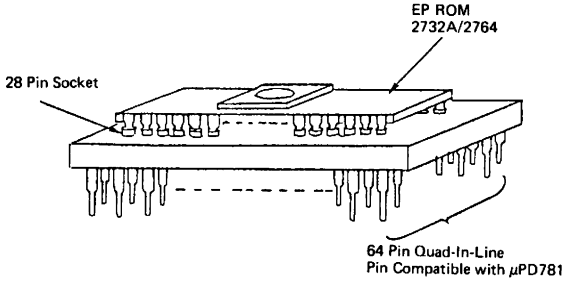


When ordering this package, specify as follows:
μPD7810CW
μPD7811CW-xxx

64 PIN CERAMIC
PIGGY BACK QUIP OUTLINE (Unit : mm)
μPD78PG11E



QUIL CERAMIC PIGGY BACK
PACKAGE OUTLINE
μPD78PG11E



- μPD78PG11E can access eprom when addressing 0 to 4095
- All memory of the 2732A memory (4K-Byte memory)
- Lower 4K-Byte of the 2764 memory (8K-Byte memory)

PRELIMINARY

ELECTRICAL SPECIFICATIONS

AND PACKAGE OUTLINES FOR

μPD7810H/7811H

ABSOLUTE MAXIMUM RATINGS

(T_a = 25° C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{DD}		−0.5 to +7.0	V
	AV_{CC}		−0.5 to +7.0	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to +7.0	V
Output Voltage	V_O		−0.5 to + 7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−0.5	mA
		All Output Pin Total	−20	mA
Reference Input Voltage	V_{AREF}		−0.5 to V_{CC}	V
Operating Temperature	T_{opt}	$f_{XTAL} \leq 15$ MHz	−10 to +70	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

PARAMETER / OSC. FREQ.	T_a	V_{CC}, AV_{CC}
$f_{XTAL} \leq 15$ MHz	−10°C to +70°C	+5.0V ± 10 %

CAPACITANCE

(T_a = 25°C, $V_{CC} = V_{DD} = V_{SS} = 0V$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	f_c = 1 MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	$C_{I/O}$				20	pF

DC CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, $V_{CC} - 0.8V \leq V_{DD} \leq V_{CC}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except SCK, RESET, X1	2.0		V_{CC}	V
	V_{IH2}	SCK, X1	0.8 V_{CC}		V_{CC}	V
	V_{IH3}	RESET	0.8V_{DD}		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −200μA	2.4			V
Input Current	I_I	INT1, TI (PC3), $+0.45V \leq V_I \leq V_{CC}$			± 200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3) $0V \leq V_I \leq V_{CC}$			± 10	μA
Output Leakage Current	I_{LO}	$0.45V \leq V_O \leq V_{CC}$			± 10	μA
AV_{CC} Supply Current	AI_{CC}			6	12	mA
V_{DD} Supply Current	I_{DD}			1.5 *1	3.2	mA
V_{CC} Supply Current	I_{CC}			150 *1	200	mA
Data Retention Voltage	V_{DDDR}	$V_{CC} = 0$, RESET = V_{IL}	3.2			V

*1 T_a = 25°C, $V_{CC} = V_{DD}$ = +5.0V

AC CHARACTERISTICS
READ/WRITE OPERATION

(T_a = 10°C to +70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
X1 Input Cycle Time	t_{CYC}		66	250	ns
Address Setup to ALE ↓	t_{AL}		30		ns
Address Hold from ALE ↓	t_{LA}		35		ns
Address to RD ↓ Delay Time	t_{AR}		100		ns
RD ↓ to Address Floating	t_{AFR}			20	ns
Address to Data Input	t_{AD}			250	ns
ALE ↓ to Data Input	t_{LDR}			135	ns
RD ↓ to Data Input	t_{RD}			120	ns
ALE ↓ to RD ↓ Delay Time	t_{LR}		15		ns
Data Hold Time from RD ↑	t_{RDH}		0		ns
RD ↑ to ALE ↑ Delay Time	t_{RL}		80		ns
RD Width Low	t_{RR}	Data Read	215		ns
		OP Code Fetch	415		ns
ALE Width High	t_{LL}		90		ns
$\overline{M1}$ Setup Time to ALE ↓	t_{ML}		30		ns
$\overline{M1}$ Hold Time from ALE ↓	t_{LM}		35		ns
$\overline{IO}$/M Setup Time to ALE ↓	t_{IL}		30		ns
$\overline{IO}$/M Hold Time from ALE ↓	t_{LI}		35		ns
Adress to WR ↓ Delay	t_{AW}		100		ns
ALE ↓ to Data Output	t_{LDW}			180	ns
WR ↓ to Data Output	t_{WD}			100	ns
ALE ↓ to WR ↓ Delay Time	t_{LW}		15		ns
Data Setup Time to WR ↑	t_{DW}		165		ns
Data Hold Time from WR ↑	t_{WDH}		60		ns
WR ↑ to ALE ↑ Delay Time	t_{WL}		80		ns
WR Width Low	t_{WW}		215		ns

Note 1. f_{XTAL} = 12 MHz
2. Load Capacitance, C_L = 150pF

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNITS
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*2	800		ns
			*3	500		ns
		$\overline{SCK}$ Output		1.6		μs
SCK Width Low	t_{KKL}	$\overline{SCK}$ Input	*2	335		ns
			*3	200		ns
		$\overline{SCK}$ Output		700		μs
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*2	335		ns
			*3	200		ns
		$\overline{SCK}$ Output		700		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*2		80		ns
RxD Hold Time from $\overline{SCK}$ ↑	t_{KRX}	*2		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*2			210	ns

*2: 1x Baud Rate in Asynchronous, Synchronous, I/O Interface Mode
*3: 16x Baud Rate or 64x Baud Rate in Asynchronous

ZERO-CROSS CHARACTERISTICS

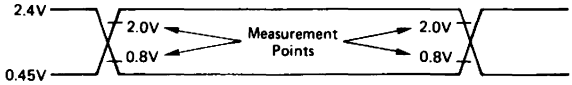
(T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10 %, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60 Hz Sine Wave		± 135	mV
Zero-Cross Detextion Input Frequency	f_{ZX}		0.05	1	kHz

A/D CONVERTER CHARACTERISTICS

(T_a = −10°C to +70°C, V_{CC} = AV_{CC} = +5.0V ± 10%, V_{SS} = AV_{SS} = 0V, AV_{CC} − 0.5 ≤ V_{AREF} ≤ AV_{CC})

PARAMETER	SYMBOL	TEST CONDITIONS	Min	TYP		UNITS
Resolution			8			Bits
Absolute Accuracy		T_a = 0°C to +70°C, 66ns ≤ t_{CYC} ≤ 170ns			0.4% ± 1/2	LSB
Conversion Time	t_{CONV}	66ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	66ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
V_{AREF} Current	I_{AREF}		0.1	2.0	5.0	mA



AC TIMING MEASUREMENT POINT

BUS TIMING DEPENDING ON t_{CYC}

SYMBOL	CALCULATING EXPRESSION	MIN./MAX.	UNITS
t_{AL}	2T − 100	MIN	ns
t_{LA}	T − 30	MIN	ns
t_{AR}	3T − 100	MIN	ns
t_{AD}	7T − 220	MAX	ns
t_{LDR}	5T − 200	MAX	ns
t_{RD}	4T − 150	MAX	ns
t_{LR}	T − 50	MIN	ns
t_{RL}	2T − 50	MIN	ns
t_{RR}	4T − 50 (Data Read)	MIN	ns
	7T − 50 (OP Code Fetch)		
t_{LL}	2T − 40	MIN	ns
t_{ML} *2	2T − 100	MIN	ns
t_{LM} *2	T − 30	MIN	ns
t_{IL} *3	2T − 100	MIN	ns
t_{LI} *3	T − 30	MIN	ns
t_{AW}	3T − 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T − 50	MIN	ns
t_{DW}	4T − 100	MIN	ns
t_{WDH}	2T − 70	MIN	ns
t_{WL}	2T − 50	MIN	ns
t_{WW}	4T − 50	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ Input) *1	MIN	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	5T + 5 ($\overline{SCK}$ Input) *1	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		
t_{KKH}	5T + 5 ($\overline{SCK}$ Input) *1	MIN	ns
	12T − 100 ($\overline{SCK}$ Output)		

*1. 1x Baud Rate in Asynchronous, Synchronous, I/O Interface Mode

Note 1. T = t_{CYC} = $1/f_{XTAL}$

2. The items out of this table are not dependent on f_{XTAL}

OTHER OPERATIONS

(T_a = −10°C to + 70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

Parameter	Symbol	Conditions	MIN	MAX	UNITS
TI width high, low	t_{TIH}, t_{TIL}		6		t_{CYC}
CI width high, low	t_{CI1H}, t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ width high, low	t_{NIH}, t_{NIL}		36		t_{CYC}
INT1 width high, low	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ width high, low	t_{I2H}, t_{I2L}		36		t_{CYC}
$\overline{RESET}$ width high, low	t_{RSH}, t_{RSL}		60		t_{CYC}

EXTERNAL CLOCK TIMING

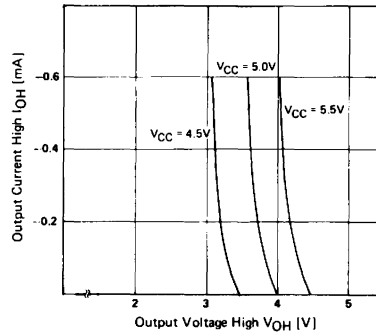
(T_a = −10°C to + 70°C, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC})

Parameter	Symbol	Test Condition	MIN	MAX	UNITS
X1 input width high	$t_{\Phi H}$		20	250	ns
X1 input width low	$t_{\Phi L}$		20	250	ns
X1 input rise time	t_r		0	20	ns
X1 input fall time	t_f		0	20	ns

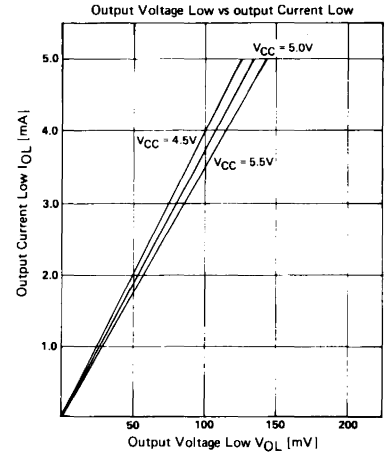
CHARACTERISTICS CURVE
– REFERENCE –

(T_a = 25°C)

Output Voltage High vs Output Current High

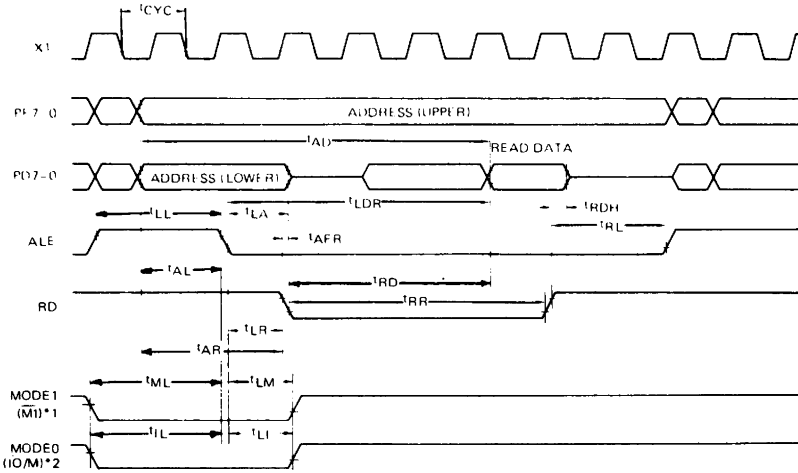


Output Voltage Low vs output Current Low



TIMING WAVEFORM

Read Operation

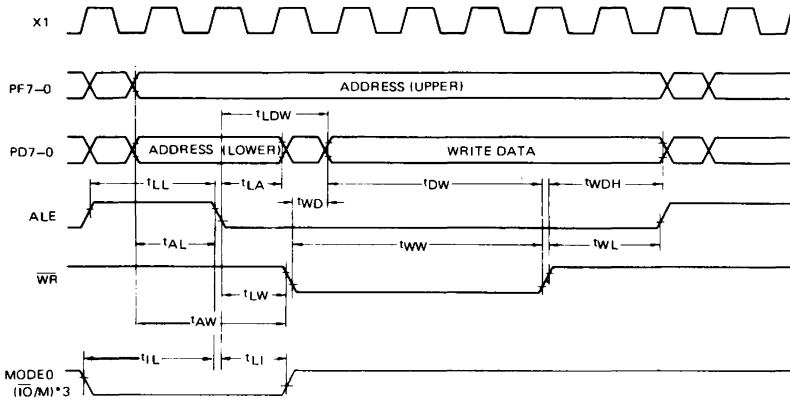


*1 $\overline{M_1}$ is output at the fetch cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

*2 $\overline{IO}$/M is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

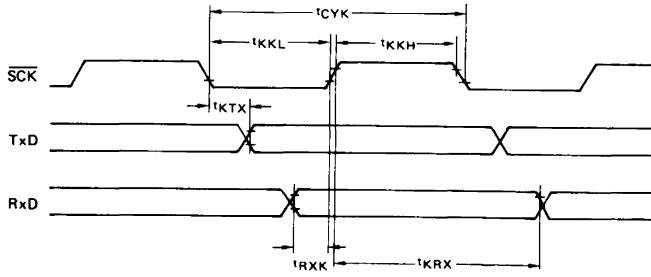
TIMING WAVEFORM

Write Operation

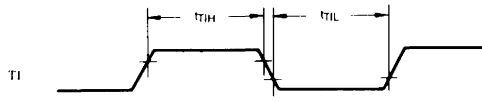


*3 IO/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Serial Operation

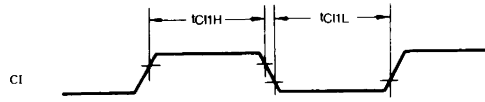


TIMER INPUT TIMING



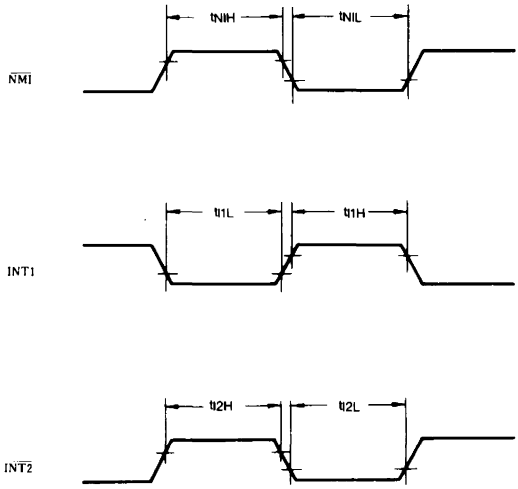
TIMER/EVENT COUNTER INPUT TIMING

EVENT COUNT MODE

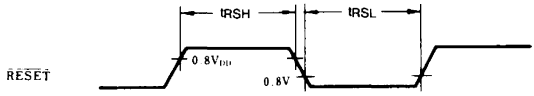


PULSE WIDTH MEASUREMENT MODE

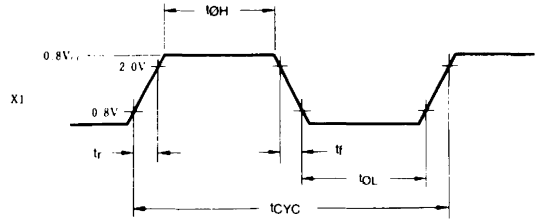
INTERRUPT INPUT TIMING



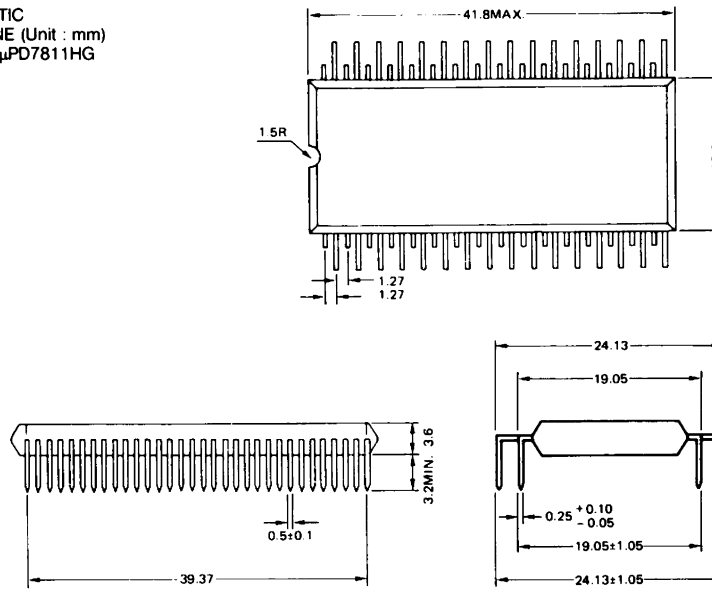
RESET INPUT TIMING



EXTERNAL CLOCK TIMING

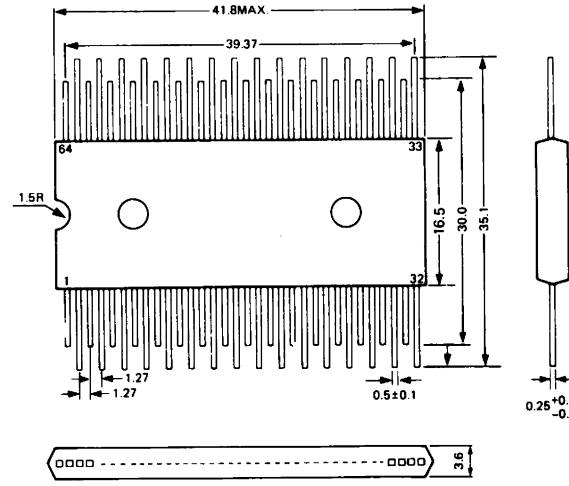


64 PIN PLASTIC
QUIP OUTLINE (Unit : mm)
μPD7810HG/μPD7811HG



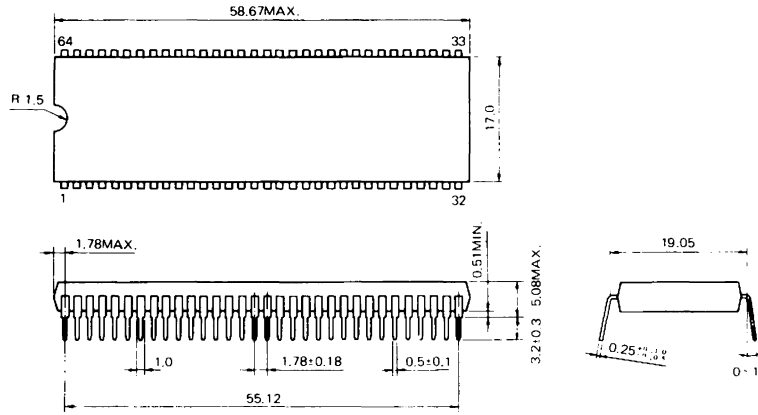
When ordering this package, specify as follows:
μPD7810HG-36
μPD7811HG-xxx-36

64 PIN PLASTIC
QUIP PACKAGE OUTLINE
(Unit : mm)
μPD7811HG



When ordering this package, specify as follows: μPD7811HG-XXX-37

64 PIN PLASTIC
SHRINK DIP OUTLINE (Unit : mm)
μPD7810HCW/μPD7811HCW



When ordering this package, specify as follows:
μPD7810HCW
μPD7811HCW-xxx

PRELIMINARY

ELECTRICAL SPECIFICATIONS

AND PACKAGE OUTLINES FOR

μPD78C10/78C11/78C14*

* Note: For μPD78C14 this specification is only target and some parameters, especially DC Characteristics and Absolute Ratings, may change without notice

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

Parameter	Symbol	Test Condition	Ratings	Unit
Power Supply Voltage	V_{DD}		−0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD} + 0.5	V
	AV_{SS}		−0.5 to +0.5	V
Input Voltage	V_I		−0.5 to V_{DD} +0.5	V
Output Voltage	V_O		−0.5 to V_{DD} +0.5	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	−2.0	mA
		All Output Pin Total	−50	mA
Reference Input Voltage	VAREF		−0.5 to AV_{DD} +0.3	V
Operating Temperature	T_{opt}	$f_{XTAL} \leq$ 12MHz	−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

OPERATING CONDITION

Parameter / OSC frequency	Ta	V_{DD}, AV_{DD}
$f_{XTAL} \leq$ 12MHz	−40°C to +85°C	+5.0V ± 10%

CAPACITANCE

(T_a = 25°C, V_{DD} = V_{SS} = 0V)

Paramater	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Input Capacitance	C_I	f_C = 1MHz Unmeasured Pins Returned to 0V			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	C_{IO}				20	pF

(T_a = -40°C to +85°C, V_{DD} = +5.0V ±10%, V_{SS} = 0V)

DC CHARACTERISTICS

Parameter	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL1}	All except RESET, STOP, NMI, SCK, INT 1, TI, AN4 to 7	0		0.8	V
	V_{IL2}	RESET, STOP, NMI, SCK, INT1, TI, AN4 to 7	0		$0.2V_{DD}$	V
Input High Voltage	V_{IH1}	All except RESET, STOP, NMI, SCK, INT1, TI, AN4 to 7, X1, X2	2.2		V_{DD}	V
	V_{IH2}	RESET, STOP, NMI, SCK, INT1, TI, AN4 to 7, X1, X2	$0.8V_{DD}$		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	V_{DD}-1.0			V
		I_{OH} = -100μA	V_{DD}-0.5			V
Input Current	I_I	INT1, TI (PC3); $0V \leq V_I \leq V_{DD}$			±200	μA
Input Leakage Current	I_{LI}	All except INT1, TI (PC3), $0V \leq V_I \leq V_{DD}$			±10	μA
Output Leakage Current	I_{LO}	$0V \leq V_O \leq V_{DD}$			±10	μA
AV_{DD} Supply Current	AI_{DD}			0.3	1.0	mA
V_{DD} Supply Current	I_{DD1}	Operation mode f=12MHz		15	30	mA
	I_{DD2}	HALT MODE f=12MHz		10	20	mA
Data Retention Voltage	V_{DDDR}	Hardware/Software STOP MODE	2.5			V
Data Retention Current	I_{DDDR}	Hardware/Software STOP Mode, V_{DDDR} = 2.5V		1	15	μA
		V_{DDDR} = 5V±10%		10	50	μA

AC CHARACTERISTICS
READ/WRITE
OPERATION

(T_a = -40°C to +85°C, V_{DD} = + 5.0 V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	MIN	MAX	Unit
X1 Input Cycle Time	t_{CYC}		83	250	ns
Address Setup to ALE↓	t_{AL}	*3, *4	65		ns
Adress Hold after ALE↓	t_{LA}	*3, *4	50		ns
Adress to $\overline{RD}$↓ Delay Time	t_{AR}	*3, *4	150		ns
$\overline{RD}$↑ to Address Floating	t_{AFR}	*4		20	ns
Adress to Data Input	t_{AD}	*3, *4		360	ns
ALE↓ to Data Input	t_{LDR}	*3, *4		215	ns
$\overline{RD}$↓ to Data Input	t_{RD}	*3, *4		180	ns
ALE to $\overline{RD}$↓ Delay Time	t_{LR}	*3, *4	35		ns
Data Hold after $\overline{RD}$↑	t_{RDH}	*4	0		ns
$\overline{RD}$↑ to ALE↑ Delay Time	t_{RL}	*3, *4	115		ns
$\overline{RD}$ Width Low	t_{RR}	Data Read, *3, *4	280		ns
		OP code Fetch, *3, *4	530		ns
ALE Width High	t_{LL}	*3, *4	125		ns
$\overline{M1}$ Setup time to ALE↓	t_{ML}	*3	65		ns
$\overline{M1}$ Hold Time after ALE↓	t_{LM}	*3	50		ns
$\overline{IO}$/M Setup Time to ALE↓	t_{IL}	*3	65		ns
$\overline{IO}$/M Hold Time after ALE↓	t_{LI}	*3	50		ns
Address to $\overline{WR}$↓ Delay	t_{AW}	*3, *4	150		ns
ALE↓ to Data Output	t_{LDW}	*3, *4		195	ns
$\overline{WR}$↓ to Data Output	t_{WD}	*4		100	ns
ALE to $\overline{WR}$↓ Delay	t_{LW}	*3, *4	35		ns
Data Setup Time to $\overline{WR}$↑	t_{DW}	*3, *4	230		ns
Data Hold Time after $\overline{WR}$↑	t_{WDH}	*3, *4	95		ns
$\overline{WR}$↑ to ALE↑ Delay Time	t_{WL}	*3, *4	115		ns
$\overline{WR}$ Width Low	t_{WW}	*3, *4	280		ns

AC CHARACTERISTICS
SERIAL OPERATION

Parameter	Symbol	Test Condition		MIN	MAX	UNIT
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	*5	1		μs
			*6	500		ns
		$\overline{SCK}$ Output		2		μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	*5	420		ns
			*6	200		ns
		$\overline{SCK}$ Output		900		ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	*5	420		ns
			*6	200		ns
		$\overline{SCK}$ Output		900		ns
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	*5		80		ns
RxD Hold Time After $\overline{SCK}$ ↑	t_{KRX}	*5		80		ns
$\overline{SCK}$ ↓ to TxD Delay Time	t_{KTX}	*5			210	ns

(T_a = -40°C to +85°C, V_{DD} = +5.0V ± 10%, V_{SS} = AV_{SS} = 0V, V_{DD} -0.5V ≤ AV_{DD} ≤ V_{DD}, 4.0V ≤ V_{AREF} ≤ AV_{DD})

A/D CONVERTER
CHARACTERISTICS

Parameter	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Resolution			8			Bits
Absolute Accuracy		Ta = -10°C to +50°C, 83ns ≤ t_{CYC} ≤ 170ns			0.4%±1/2	LSB
		83ns ≤ t_{CYC} ≤ 170ns			0.6%±1/2	LSB
		3.4V ≤ V_{AREF} ≤ AV_{DD} 83ns ≤ t_{CYC} ≤ 170ns			0.8%±1/2	LSB
Conversion time	t_{CONV}	83ns ≤ t_{CYC} ≤ 110ns	576			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	432			t_{CYC}
Sampling Time	t_{SAMP}	83ns ≤ t_{CYC} ≤ 110ns	96			t_{CYC}
		110ns ≤ t_{CYC} ≤ 170ns	72			t_{CYC}
Analog Input Voltage	V_{IAN}		0		V_{AREF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
V_{AREF} Current	I_{AREF}			1.5	3.0	mA

ZERO-CROSS CHARACTERISTICS

(T_a = -40°C to +85°C, V_{DD} = +5.0V±10%, V_{SS} = 0V)

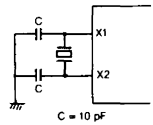
Parameter	Symbol	Test Condition	MIN	MAX	UNIT
Zero-Cross Detection Input	V_{ZX}	AC Coupled	1	1.8	VAC_{p-p}
Zero-Cross Accuracy	A_{ZX}	60Hz Sine Wave		±135	mV
Zero-Cross Detection Input Frequency	f_{ZX}		0.05	1	kHz

OTHER OPERATIONS

(T_a = -40°C to +85°C, V_{DD} = +5.0V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	MIN	MAX	UNIT
TI width high, low	t_{TIH}, t_{TIL}		6		t_{CYC}
CI width high, low	t_{CI1H}, t_{CI1L}	Event Count Mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	Pulse Width Measurement Mode	48		t_{CYC}
$\overline{NMI}$ width high, low	t_{NIH}, t_{NIL}		10		μs
INT1 width high, low	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ width high, low	t_{I2H}, t_{I2L}		36		t_{CYC}
$\overline{RESET}$ width high, low	t_{RSH}, t_{RSL}		10		μs

*1. For XTAL oscillation, following circuit is recommended.



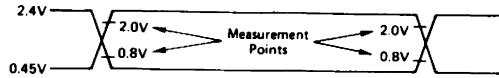
*2. T_a = +25°C, V_{DD} = 5 V

*3. f_{XTAL} = 12MHz

*4. Load Capacitance: C_L = 150pF

*5. x1 Clock Rate in Asynchronous Mode, Synchronous Mode, I/O Interface Mode

*6. x16, x64 Clock Rate in Asynchronous Mode



AC TIMING
MEASUREMENT POINT

$(T_a = -40°C$ to $+85°C$, $V_{DD} = +5.0V \pm 10\%)$

EXTERNAL CLOCK
TIMING

Parameter	Symbol	Test Condition	MIN	MAX	UNIT
X1 input width high	$t_{\Phi H}$		30	250	ns
X1 input width low	$t_{\Phi L}$		30	250	ns
X1 input rise time	t_r		0	30	ns
X1 input fall time	t_f		0	30	ns

BUS TIMING DEPENDING ON t_{CYC}

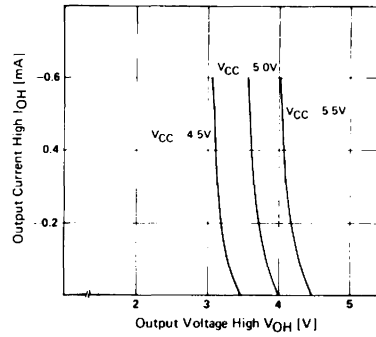
Symbol	Calculating Expression	MIN./MAX.	units
t_{AL}	2T - 100	MIN	ns
t_{LA}	T - 30	MIN	ns
t_{AR}	3T - 100	MIN	ns
t_{AD}	7T - 220	MAX	ns
t_{LDR}	5T - 200	MAX	ns
t_{RD}	4T - 150	MAX	ns
t_{LR}	T - 50	MIN	ns
t_{RL}	2T - 50	MIN	ns
t_{RR}	4T - 50 (Data Read) 7T - 50 (OP Code Fetch)	MIN	ns
t_{LL}	2T - 40	MIN	ns
t_{ML}	2T - 100	MIN	ns
t_{LM}	T - 30	MIN	ns
t_{IL}	2T - 100	MIN	ns
t_{LI}	T - 30	MIN	ns
t_{AW}	3T - 100	MIN	ns
t_{LDW}	T + 110	MAX	ns
t_{LW}	T - 50	MIN	ns
t_{DW}	4T - 100	MIN	ns
t_{WDH}	2T - 70	MIN	ns
t_{WL}	2T - 50	MIN	ns
t_{WW}	4T - 50	MIN	ns
t_{CYK}	12T ($\overline{SCK}$ Input) *1 24T ($\overline{SCK}$ Output)	MIN	ns
t_{KKL}	5T + 5 ($\overline{SCK}$ Input) *1 12T - 100 ($\overline{SCK}$ Output)	MIN	ns
t_{KKH}	5T + 5 ($\overline{SCK}$ Input) *2 12T - 100 ($\overline{SCK}$ Output)	MIN	ns

Note 1. In case of x1 clock rate in asynchronous mode, synchronous mode, or I/O interface mode.
2. $T = t_{CYC} = 1/f_{XTAL}$
3. Parameters which can't be found in this table don't depend on oscillation frequency (f_{XTAL}).

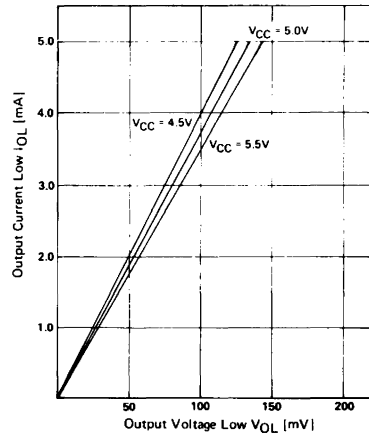
CHARACTERISTICS CURVE
– REFERENCE –

(T_a = 25°C)

Output Voltage High vs Output Current High

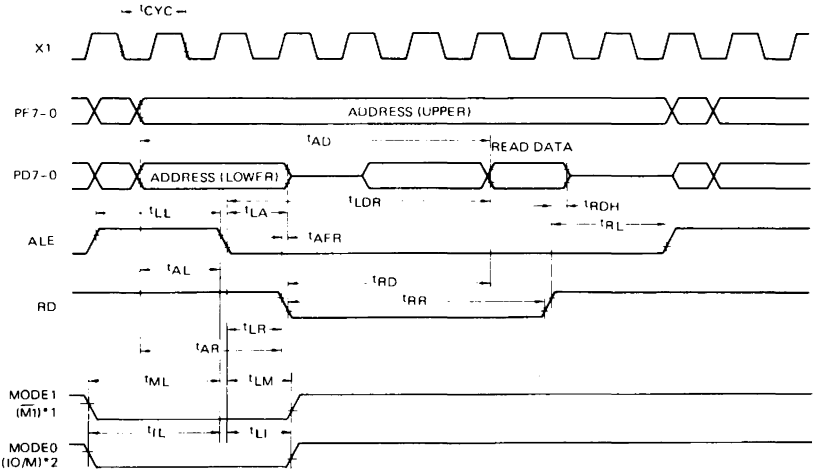


Output Voltage Low vs Output Current Low



TIMING WAVEFORM

Read Operation

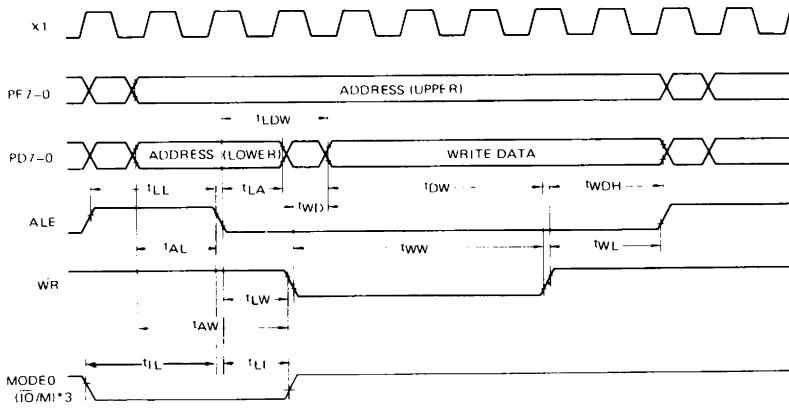


*1 $\overline{M_1}$ is output at the fetech cycle of the 1st byte of the instruction in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

*2 $\overline{IO}$/M is output only when registers (sr-sr2) are read in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

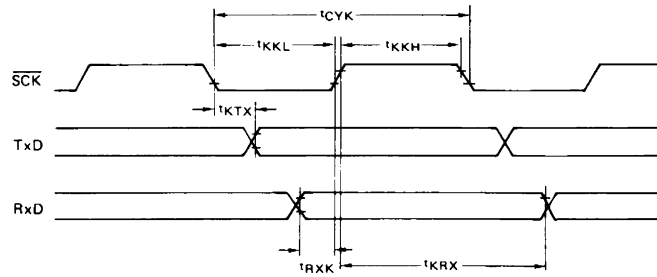
TIMING WAVEFORM

Write Operation

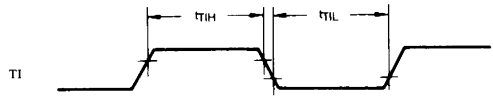


*3 $\overline{IO}$/M is output only when registers (sr-sr2) are written in case that MODE0 and MODE1 pins are connected to V_{CC} through R.

Serial Operation

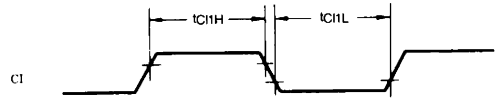


TIMER INPUT TIMING

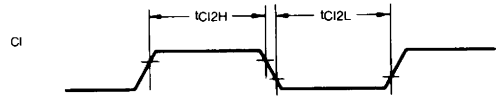


TIMER/EVENT COUNTER INPUT TIMING

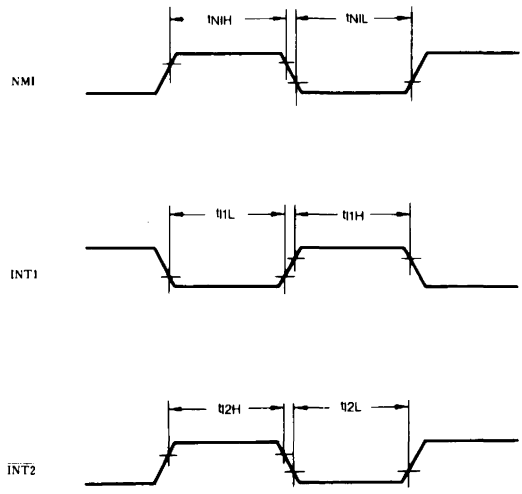
EVENT COUNT MODE



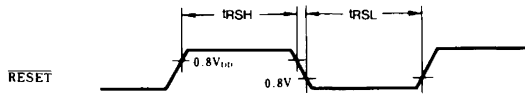
PULSE WIDTH MEASUREMENT MODE



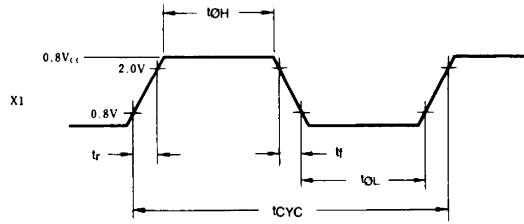
INTERRUPT INPUT TIMING



RESET INPUT TIMING



EXTERNAL CLOCK TIMING

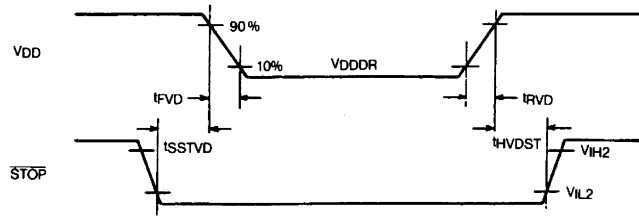


DATA MEMORY STOP MODE DATA RETENTION CHARACTERISTICS

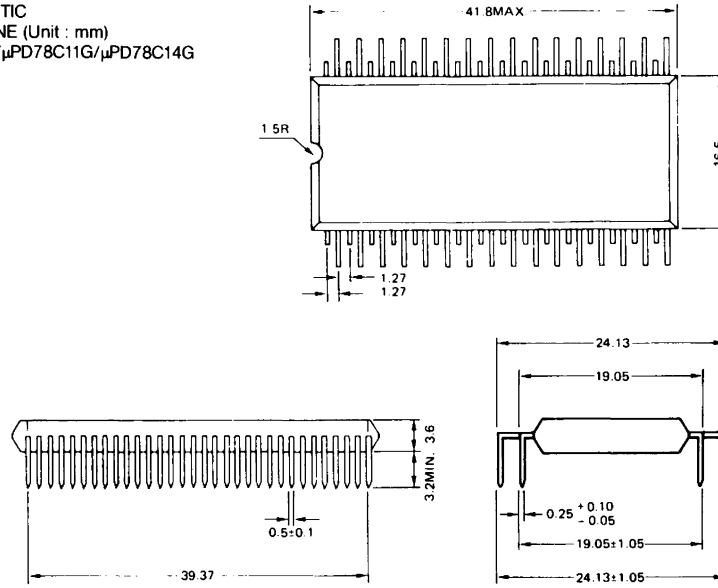
(T_a = −40°C to + 85°C)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	UNIT
Data retention power supply voltage	V_{DDDR}		2.5		5.5	V
Data retention power supply current	I_{DDR}	V_{DDDR} = 2.5 V		1	15	μA
		V_{DDDR} = 5 V ±10%		15	50	μA
V_{DD} rise, fall time	t_{RVD} t_{FVD}		200			μs
$\overline{STOP}$ setup time to V_{DD}	t_{SSTVD}		12T +0.5			μs
$\overline{STOP}$ hold time from V_{DD}	t_{HVDST}		12T +0.5			μs

DATA RETENTION TIMING

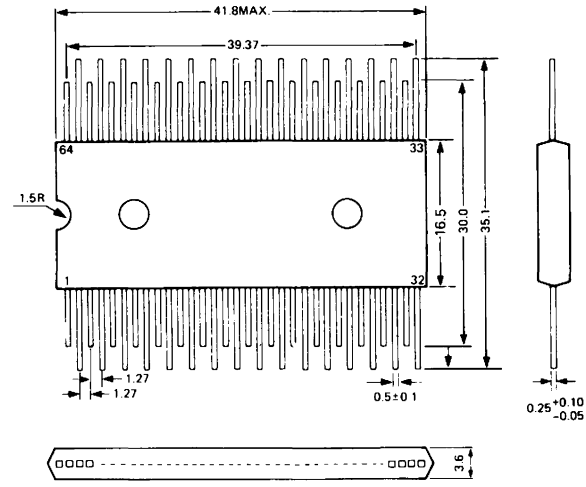


64 PIN PLASTIC
QUIP OUTLINE (Unit : mm)
μPD78C10G/μPD78C11G/μPD78C14G



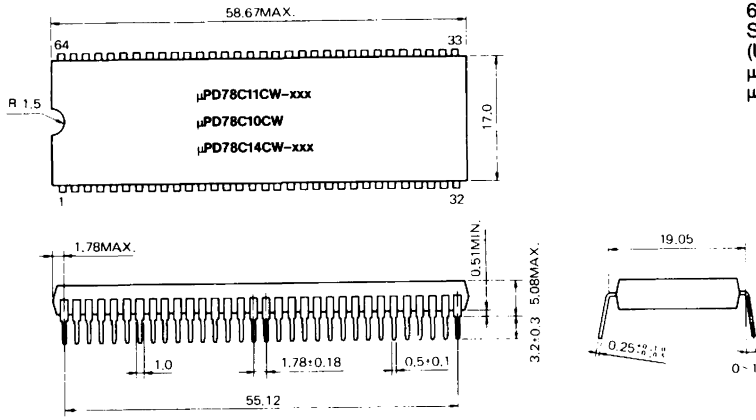
When ordering this package, specify as follows:
μPD78C10G-36
μPD78C11G-xxx-36
μPD78C14G-xxx-36

64 PIN PLASTIC
FLAT PACKAGE OUTLINE
(Unit : mm)
μPD78C11G/μPD78C14G

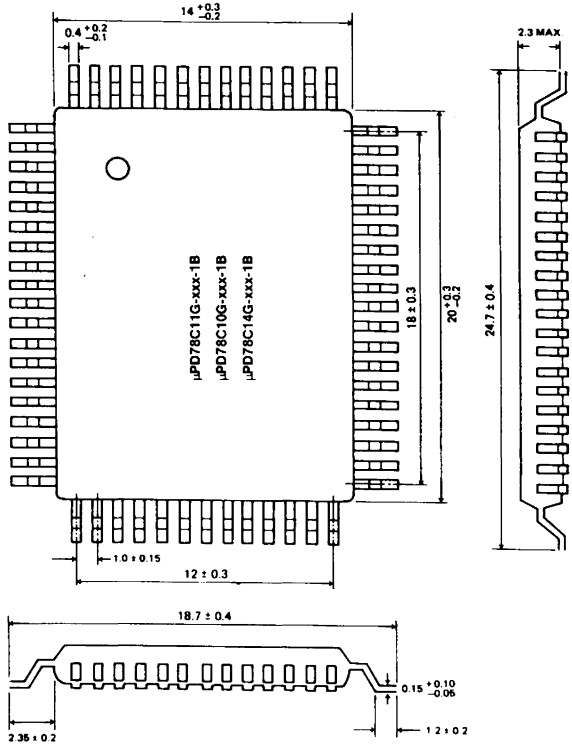


When ordering this package, specify as follows: μPD78C11G-XXX-37
μPD78C14G-XXX-37

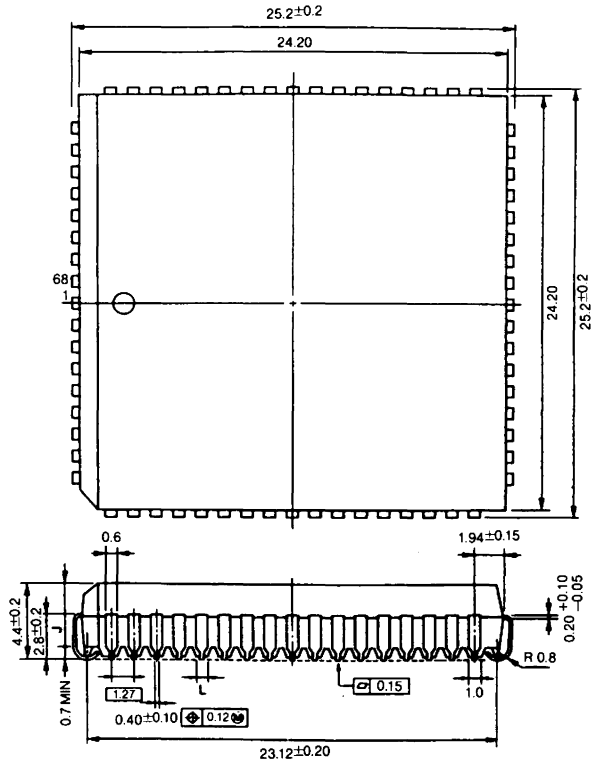
64 PIN PLASTIC
SHRINK DIP OUTLINE
(Unit : mm)
μPD78C10CW/C11CW
μPD78C14CW



64 PIN PLASTIC
FLAT PACK OUTLINE
(Unit : mm)
μPD78C10G/C11G
μPD78C14G



68 PIN PLASTIC LCC
PACKAGE OUTLINE
μPD78C10L/C11L/C14L



CMOS-DESIGN RECOMMENDATIONS

In order to maximize circuit reliability please note the general CMOS design rules.

For example:

1) Don't leave unused pins open, except they are outputs or no connected.

2) Never exceed the max. voltage range.

3) Avoid accurance of very fast voltage spikes or transission rate the power supply pin.

CHAPTER 5

THE μCOM78K FAMILY

μPD78310, 78312

μPD78224

PRELIMINARY

μPD78310, μPD78312

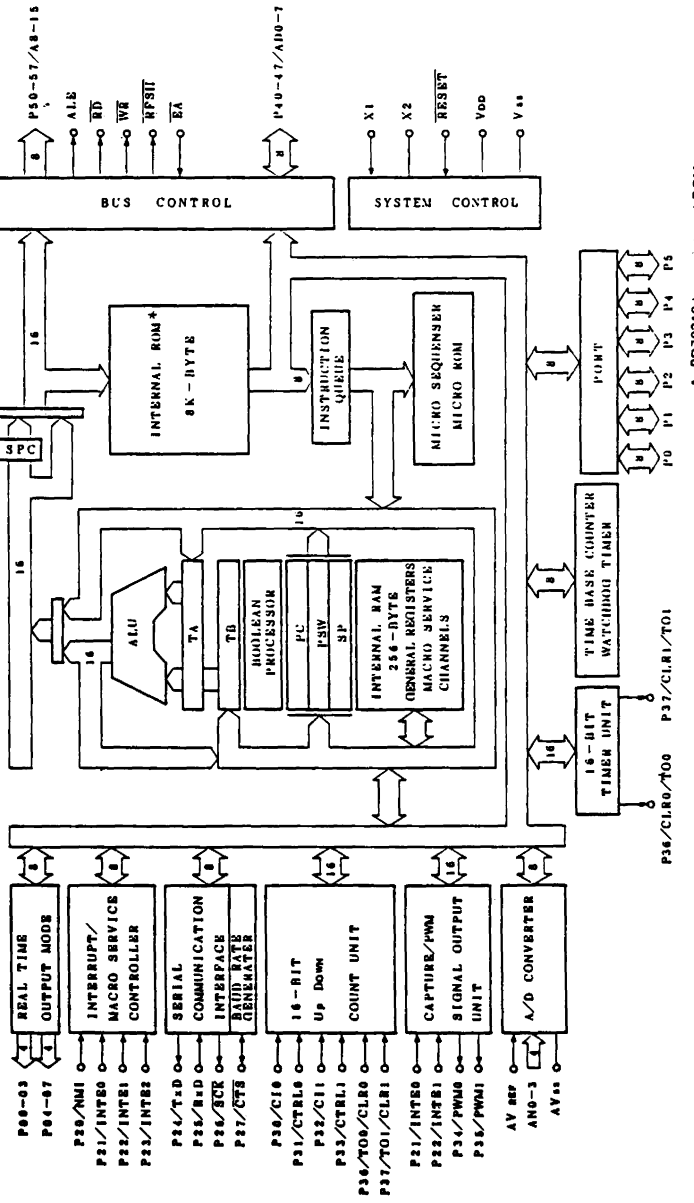
INTRODUCTION

The uPD78312 is a CMOS single-chip 8-bit microcomputer, designed for real-time control applications. It includes a 16-bit CPU, ROM, RAM, an A/D converter, a general-purpose serial communication interface, and a multipurpose pulse input/output unit. In addition, the uPD78312 can be interfaced to external memory, either ROM or RAM. There is also available a ROM-less version, the uPD78310, which can be used with up to 64K bytes of external memory.

FEATURES

- Single-chip microcomputer (uCOM-78K series)
- 96 instructions with many addressing modes
  - 16-bitarithmetic and move instructions, bit manipulation instructions, multiplication/division instructions, string instructions, user stack manipulation instructions.
- Instruction cycle: 500 nsec at 12 MHz input
- Internal ROM: 8,192 x 8 bits
- Internal RAM: 256 x 8 bits
- Capable of directly addressing external (ROM/RAM) up 60 64K bytes
- Memory mapping of on-chip peripheral hardware (special function registers)
- Multipurpose pulse input/output unit
  - Two 16-bit presetable up/down counters
  - Two 16-bit internal timers
  - Two high-accuracy pulse-width-modulated outputs
  - Two 4-bit real-time output port channels
- 8-bit A/D converter with 4 input channels and sample-and-hold
- I/O ports
  - 8 dedicated input lines
  - up to 32 I/O lines (uPD78312)
  - up to 20 I/O lines (uPD78310) (for 4K-bytes of external memory)
- General-purpose serial communication interface (with dedicated baud rate generator)
  - Asynchronous mode, I/O interface mode
- Interrupt request controller
  - Vectored interrupts
  - Context switching
  - Macro service function
- Pseudo static memory refresh pulse output
- Watchdog timer
- Time base counter
- Standby function (STOP/HALT)
- CMOS circuitry
- Single power supply

1.2 uPD78312, 78310 Block Diagram



GENERAL DESCRIPTION OF THE PROCESSOR

The uPD78312 is a powerful single chip microcomputer designed for use in process control. It can perform all the usual process control functions and is particularly well suited for driving motors, both DC motors in servo loops and stepping motors. The processor includes on-chip memory, timers, input/output registers, and a particularly powerful interrupts handling facility. It is constructed of high speed CMOS circuitry and operates from a 5 volt power supply. Program memory is 8K bytes of ROM, and data memory is 256 bytes of static RAM. The uPD78312 uses mask-programmable ROM, but a romless version, the uPD78310 is also available, and an EPROM version, the uPD78P312, is planned. The uPD78312 and the uPD78310 are available in 64 pin flat pack, QUIL, and shrink dip.

The maximum input frequency is 12 MHz, derived from either a crystal or an external oscillator. The internal processor clock is two phase, and therefore machine states are executed at a rate of 6 MHz. The shortest instructions require 3 states, making the minimum instruction time 500 nanoseconds. The CPU contains a three bytes instruction pre-fetch queue which allows a subsequent instruction to be fetched during the execution o an instruction which does not reference memory.

The CPU includes 16 general purpose 8-bit registers which can be used in pairs to form eight 16-bit registers. Memory access and I/O paths are 8-bits wide, but all of the arithmetic can be performed to a precision of either 8 or 16 bits. In addition the timer registers are all 16 bits wide. On-chip features designed to facilitate process control include two 16 bit timers, two 16 bit up/down counters, two pulse width modulated outputs, a free running counter with two capture registers, two 4-bit realtime (timer controlled) output ports, an 8-bit A/D converter with 4 input channels, a timebase counter to generate widely spaced interrupts, and a watchdog timer to guard against infinite program loops. In addition there is a serial I/O port which can be used in either an interface mode or an asynchronous communication mode. HALT and STOP modes are provided to conserve power at times when the action of the CPU is not required. All I/O, timer, and control registers are defined as special functions registers and assigned addresses in the top 256 bytes of memory. The special functions registers may be operated on directly by many of the arithmetic, logic, and move instructions of the CPU.

There is a total of 14 different addressing modes. The CPU registers and the special function registers are addressed directly. Most of the RAM locations can be addressed by a "short direct memory" (SDMEM) mode which adds a one-byte displacement to a base address of OFE20H. This reduces both the memory required to store the instruction and its execution time. There are both one and two byte immediate operands, and any location in memory can be addressed by any one of ten different modes. These include register indirect, base, indexed, and double indexed modes. Most general memory references are limited to one byte transfers.

The instruction set consists of 85 basic instructions which, when combined with the 14 addressing modes and the 14 conditions for branching, produce a total of 451 instructions. All of the arithmetic instructions operate on either bytes or 16 bit words. Included are a 16 x 16 bit multiply and a divide with a 32 bit dividend and 16 bit divisor. Logical instructions operate on either bytes or individual bits, and there are branch instructions which test individual bits in SDMEM locations, in the special functions registers, and in the A and X registers. Multiple-bit shift instructions for the general CPU registers, operating either a single bytes or as 16-bit words, facilitate arithmetic operations. There are also instructions to move, exchange, and test strings of up to 256 bytes located anywhere in memory. The length of the string is specified by a count in the C register. The last are very useful for manipulating character data sent or received on the serial line.

Interrupt requests may, under program control, be handled in any one of three ways. The first is normal vectoring, the second is a hardware context switch in which all the registers are saved by the hardware and new set selected, and the third a macro program function which has the same effect as DMA. The context switch is usually preferred to normal vectoring because of the time saved by the automatic register saving hardware. The macro service function is useful whenevr a string of data is to be transferred to or from an external device at that device's own speed. There are eight complete sets of general registers stored in RAM, and each may be assigned, under program control, to one of the hardware interrupt levels. There are 8 hardware priority levels which may be assignedd by software to any one of the 5 groups of maskable interrupt sources.

CPU REGISTERS

There are 16 8-bit general registers which may be used in pairs to form 8 16-bit registers. When considered as 8-bit registers they are referred to as R0 though R15, and when considered as 16-bit registers they are referred to as RP0 through RP7. Thus RP0 consists of R0 and R1, RP1 consists of R2 and R3, and so on. In addition RP0 is referred to as AX, RP1 as BC, RP4 as VP, RP5 as UP, RP6 as DE, and RP7 as HL. A (R0) is the 8-bit accumulator, and AX (A combined with X) the 16-bit accumulator. B and C are often used as counters, UP and VP as address pointers, and DE and HL as index registers. UP (RP5) is also used as the user stack pointer for the instructions PUSHU and POPU. All can be used to hold operands and results for both 8-bit and 16-bit arithmetic. RP2 and RP3 each have two special purposes. The SWRS (switch register set) instruction toggles the RSS (register set select) bit in the program status word. If the RSS bit is set to 1, RP2 becomes AX, and RP3 becomes BC, thus making it possible dto save AX and BC very rapidly. In addition, after a context switch the old program counter is saved in RP2 and the old program status word in RP3. For this reason routines entered from a context switch must save RP2 and RP3 elsewhere (e.g. on the stack) before setting the RSS bit.

MEMORY ORGANIZATION

The total address space of the uPD78312 is 64K bytes. The bottom 8K bytes are occupied by internal ROM, and the rop 512 bytes are occupied by internal RAM and the special function registers. The remaining addresses are available for external memory. Interrupt vectors occupy the bottom 64 bytes (addresses 0000H to 0040H). The next 64 bytes (addresses 0040H to 007FH) are used as a call table area. This area stores up to 32 pointers to subroutines which are used by the 1-byte subroutine call instruction, CALLT. The 2K byte area from 0800H to OFFFH is known as the "fixed area" and can be used for subroutines called by the 2 byte CALLF instruction. The remainder of the 8K ROM is available for user program.

The address space from 2000H through FDFFH is available for external memory, which may be either ROM or RAM. If memory has been installed at 8000H and subsequent locations, it is possible to specify an alternate interrupt vector and call table area from 8000H to 807FH. This is done by setting bit 1 of the CPU control register (CCW) to a 1. This makes it possible to use two different programs if the processor is to be used in two different modes of operation. If external memory is installed, I/O Port 4 is used for data lines multiplexed with the low order 8 address bits. Portions of Port 5 are used for the high order address bits as required for the amount of memory installed. The memory mapping register (MM) is used to specify 256 byte, 4K, 16K or 56K byte expansion. Any Port 5 bits not required for addressing remain available for either output or input.

Internal RAM extends from FE00H to FEFFH. The top half of internal RAM (FE80H to FEFFH) is used for general register storage, and the top 32 bytes of this area (FEE0H to FEFFH) are used, if specified by the program, for storage of the pointers and counters used by the macro service function. This overlays the top two register bank save areas, and therefore if all of the macro service channels are in use, automatic context switching cannot be used for priority levels 0 and 1. The remaining 128 bytes of internal RAM (FE00H to FE7FH) are available for the stack and for use by the application program. Finally the top 256 addresses (FF00H to FFFFH) are reserved for the special function registers.

ADDRESSING MODES

The uPD78312 uses an extremely flexible addressing structure. The general registers and the special function registers can be addressed directly by arithmetic, logical, and bit test instructions. Most of the locations in internal RAM (all except the first 0020H) can also be directly addressed by the use of the short direct memory method (SDMEM). A single byte of address data is added to FE20H to form the effective memory address. In most cases this address mode requires no more cycles than addressing the general registers.

Both words and bytes of immediate data are also available. All byte instructions using an immediate source and the A register as a destination operate in the minimum time of three machine states.

There are ten different methods of addressing any location in memory. Registers DE, HL, VP and UP can be used for indirect addresses, and in addition DE and HL can be used in either the auto-increment of auto-decrement before is is used. In the remaining modes the register contents are not altered. Two base-index modes allow either a byte (from A or B) or a word (from VP) to be added to a base (from DE or HL) and the resulting sum to be used as the effective address. Double indexing, which facilitates array manipulation, is thus possible. In the base mode a byte of address data from the instruction is added to a base register (DE, HL, UP or VP) to form the effective address. In addition the stack pointer can be used as the base register to facilitate the passing of subroutine arguments on the stack. The two index modes allow a word of address data from the instruction to be added to either a byte register (A or B) or to a word register (DE or HL) to form the effective address. Finally a RAM location addressed by the SDMEM method may be used as an indirect address pointing to any location in memory.

THE INSTRUCTION SET

The mnemonics used for the instruction set are based on an IEEE standard. There are 77 basic instructions ranging in length from one to five bytes, with two and three bytes being the most common. Execution times range from 3 states for many of the register instructions to 2818 states for the maximum-length string instruction. Most of the instructions which operate on single words are the multiply (18 states for bytes and 27 states for words), divide (18 states for bytes and 50 states for words), and shift (25 states for a 7 bit shift). The execution times for the shift instructions are a function of the number of bits shifted. Instruction have zero, one or two operands depending upon the requirements of the function to be performed. In the two operand case the destination is specified first, followed by the source.

Both move and exchange instructions are provided for both bytes and words. Operands include immediate data, SDMEM locations, and all of the registers, but general memory reference operands are limited to moves of single bytes to and from the A register. PUSH and POP can move multiple registers to or from the system stack. The registers to be moved are specified by individual bits in the byte of the instruction. Also included are instructions to PUSH and POP the program status word on the system stack and PUSHU and POPU. The last two transfer registers to and from a user stack specified by RP5. Bit 5 of the selector byte of these instructions selects the PSW, in not being useful to PUSH RP5 when it is being used as a stack pointer. There is also a specia move immediate instruction to lead the two protected locations, the standby control register (STBC) and the watchdog timer control (WDM).

Call instructions push the PC on the system stack and jump to a subroutine specified by a vector in the 32 word call table (one byte CALL), to a subroutine located within the 2K byte fixed area (two byte call), or to a subroutine specified as a 16 bit absolute address (three byte CALL). Subroutine addresses may also be specified by a register pair or by a register pair indirect. Finally subroutines may be entered through a break with context switch (BRKCS) which specifies a new register set. Return instructions include RET which pops the PC from the system stack, RTI which pops both the PC and the PSW, and RETCS which switches the register set back to that previously in use. The last includes 16 bits of immediate data which are placed in RP2 of the current register set. The data must be the entry address of the interrupt service routine just completed. This is necessary because the entry address is overlaid by the old PC at the time of the initial context switch.

Addresses for unconditional branch instructions may be relative to the PC or absolute (address included in the instruction), contained in a register pair, or indirect from a register pair. Conditional branch instructions use relative addresses and test the condition codes in the PSW or individual bits in the A and X registers, the PSW, the special function registers, and the SDMEM locations. A "decrement and branch relative if not zero" (DBNZ) instruction operates on the B and C registers, special function registers, and SDMEM locations.

Arithmetic and logical instructions operating on bytes include ADD, ADDC (add with carry), SUB, SUBC (subtract with borrow), the logic operations AND, OR and XOR and CMP (compare). Add, subtract and compare instructions operate on words. All of these instructions operate on CPU register, special function registers, and SDMEM locations; all may have immediate source operands. Multiply and divide are unsigned and require the operands to be in CPU registers. They operate on bytes (16 bit product or dividend) or on words (32 bit product or dividend). Multiple-bit shift and rotate instructions are specified by bit count in the instruction. General byte registers may be shifted, rotated, or rotated with the carry bit, either left of right, and general word registers may be shifted or be rotated with the low order 4 bits of the A register, either left or right. These last rotates facilitate the manipulation of data in the packed decimal format.

A powerful set of bit manipulation instructions allows individual bits of the A and X registers, the PSW, the special function registers, and the SDMEM locations to be set, cleared, complimented, moved to or from the carry bit, or operated on logically by the carry bit.

String instructions operate on multiple bytes in memory. All of the string instructions use two operands, either both in memory or one in memory and one in the A register. Memory addresses are specified by DE or by DE and HL operating in either the auto-increment or auto-decrement mode. Counts are specified in the C register. The operations are move, exchange, or compare. The compare includes a test for equal, no eqal, carry, or not carry.

If the specified condition is met, the instruction is terminated and the registers are left pointing to the next byte.

General registers R0 through R7 may be incremented or decremented as bytes, and general register pairs RP4 through RP7 as words. All of the special function registers and SDMEM locations may be incremented or decremented, either as bytes or words, and the stack pointer may be incremented or decremented as a word. Maskable interrupts may be enabled or disabled, a new register bank may be selected, and finally there is a NOP instruction.

INTERRUPT HANDLING

There are two non-maskable and 15 maskable interrupt sources. The non-maskable sources are the watchdog timer and the external NMI. The latter is normally used for catastrophic events, such as a power failure, or to "wake up" the CPU after it has been placed in the STOP state. The relative priority of the two is under program control. Both of these are always handled as vectored interrupts, saving the PC and PSW on the stack and branching to the routine indicated by the associated vector.

The 15 maskable interrupts each have an associated interrupt control register. Each register contains a request bit, a mask bit, and bits to specify context switch and/or the macro service function. Interrupt sources can be assigned to hardware priority levels in groups, and the first interrupt control register in each group includes 3 bits to specify the priority. Priorities range from zero to seven, with zero the highest and seven the lowest. The context switch is valid for all 15 sources, but the macro service is valid for 11 of them only. The macro service facility transfer either a byte or a word between a special function register and a specified location in memory. After each transfer a counter is decremented, and when the count reaches zero the interrupt service routine is entered, either by a vectored interrupt or by a context switch, as specified in the interrupt control register. There are eight macro service channels, and each has a 4 byte area in RAM for the storage of its pointers and counter. The first two bytes are a pointer to the buffer in memory (MSP), the third byte is a pointer to the special function register (SFRP), and the last byte is the counter (MSC). Each of the 11 interrupt sources which can use the macro service facility has an associated macro service control register. This register specifies whether or not the MSP is to be incremented after each transfer, whether bytes or words are to be transferred, the direction of the transfer, and the number of the macro service channel. The facility thus functions as eight direct memory access channels without requiring any external circuity.

INPUT/OUTPUT PORTS

Six 8-bit input/output ports are defined, but because the processor is packaged with only 64 pins, the port pins must be shared with other signals. As a result some of the port bits are always dedicated to other funtions and are therefore never available for general I/O. The availability of the remainder is dependent upon what other functions of the processsor are being used. When the ports are being used for standard input/output, the direction of transfer is determined on a bit-by-bit basis by the associated port mode control register (PMn). Latches are provided for output, but input is not latched. In the input mode the pins are in a high impedance state. If a pin is being used for a purpose other than simple input/output, the associated bit in PMn must be set to 1 to indicate input and therefore high impedance to avoid interfering with the other function.

Port 0 is shared with the real-time output. In the real time output mode the eight bits are treated either as a byte or as two seperate nibbles. Output information is first loaded into buffer registers and then transferred to the output latches upon receipt of signals from the timer outputs TF1 and TF0. The transfer can also be made by software command. The entire Port 1 is available for bit-selectable input or output. The low nibbles of Ports 2 and 3 are never available for I/O because the pins are dedicated to external interrupt inputs and to inputs for the up/down counters. The high nibble of Port 2 may be available for I/O, but is shared with the serial interface, while the high nibble of Port 3 is shared with timer signal lines. Ports 4 and 5 are available if no external memory is used. All 8 bits of Port 4 are selected by individual bits. If external memory is used, Port 4 is used for data lines multiplexed with the low order 8 address bits. High order address bits are taken from Port 5 as required for the amount of external memory specified in the memory mapping register (MM). Any remaining bits from Port 5 can be used for either input or output.

A block of 16 addresses within the special function register area (FFB0H trhough FFBFH) has been reserved for external circuity. If external memory has been specified and not all the available addresses occupied by memory, external device registers can be mapped into this area and then treated as special function registers. This means that it is possible to use the macro service facility to transfer data to or from these external devices.

TIMERS AND COUNTERS

Included on the chip are two 16 bit interval timers which can run at either 1 MHz or 46.875 KHz. Associated with each is a 16 bit modulus register. In the normal mode of operation each timer is loaded from the modulus register and then counted down to zero. The associated timer flag (TF0 or TF2) is then set and the timer reloaded for another cycle. The timer flags can be used to generate interrupts.

There are two timer output flip-flops (T00 and T01), which are complimented whenever a timer flag is set. T00 is associated with TF0, and T01 is associated with TF2. The flip-flop outputs are available for use by external devices. Alternatively timer 0 (but not timer 1) can be used as two one-shot timers. Both timer 0 and its modulus register can be loaded by the program and then counted down at either 500 KHz or 46.875 KHz. Completion of the count sets either TF0 or TF1. These flags may then be used to transfer the real time output buffer contents to the output port latches, as described below or to generate interrupt requests. Program intervention is then required before any further action.

There are also two 16-bit up/down counters, each with two associated compare/capture registers. The counters may be driven either by the internal clock divided by 3 (2 MHz) or by external counts, the latter in any one of several modes. The counters may be programmed to clear and re-cycle after a true comparison, and interrupts may be generated by true compare or by capture events. Each counter has an associated clear input (CLR0 and CLR1) which causes the capture of its contents in the first capture register (CR00 and CR10) and clears the counter. Because CLR0 and CLR1 share output pins with T00 and T01 respectively, these events may be triggered either by the timer flags or by external events. Capture of the counter contents in the other capture registers (CR01 and CR11) may be initiated by the output of the timebase counter. In the last cases the counters are not cleared. The ability to capture the counter contents at specific times makes it very easy to measure the frequency of external signals. Up/down discrimincation at the inputs is available, so the counters are suitable for monitoring 2-phase pulsed shaft-encoders.

The processor also includes a 20-bit free running counter (FRCP) which counts down the system clock (6 MHz if a 12 MHz crystal is used). Associated with this counter are two 16-bit capture registers. Capture events can be triggered either by two of the external interrupts (INTE0 and INTE1) or by the counter clocks of the up/down counters. They may be programmed to capture either bits 2 to 17 or bits 4 to 19, so the effective counter frequency may be either SCLK/4 or SCLK/16 (1.5 MHz or 375 KHz). It is thus possible to make precise measurements of the time between external events.

Three other functions are timed by the output of program-selected bits from FRCP. The timebase counter is used to generate widely spaced interrupts, ranging in four steps from 170 usec. to 175 msec. The timebase counter output can also be used to trigger a capture event from either of the up/down counters as descrived in the preceding paragraph. The watchdog timer, used to guard against infinite program loops, is also driven from the FRCP. If not reset, it will cause a non-maskable interrupt at one of six program-selected intervals ranging from 343 usec. to 349.5 msec.

Finally it is possible to generate a signal to time the refresh of pseudo-static RAM, if the latter is used as external memory. There are four allowable frequencies ranging from SCLK/16 to SCLK/128. Once the refresh mode register has been loaded, the refresh is completely transparent and independent of the program.

PULSE-WIDTH MODULATED OUTPUTS

The processor contains two independent pulse-width modulated output lines whose signals may be amplified to drive DC motors or integrated to provide analog signals for other purposes. Each output consists of a latch, a storage register, and a down counter. The latch is set at any one of four intervals ranging from 42.7 usec. to 10.9 msec. At the same time the down counter is loaded from the storage register and then counted down by the system clock. When the counter reaches zero, the latch is reset. The contents of the storage register therefore control the "on" time of the output, which can be set with a resolution of 167 nsec.

REALTIME OUTPUT PORTS

Input/output Port 0 may, under program control, be used for timer-controlled output. Data are located into buffer registers and transferred to the output latches at the completion of a timer count or on software command. Either the high or low nibble, each one independently, or the entire byte as a unit, may be treated lin this manner. Timer flag TF0, TFl, or both are used to initiate the transfer. If only one nibble is used, the remaining one is available for normal input/output.

A/D CONVERTER

The chip also contains an 8 bit successive approximantion A/D converter with an on-chip sample-and-hold amplifier. There are four multiplexed input channels, and the converter can be commanded either to select a specified channel or to scan continuously the first "n" channels. Conversion may be initiated either by the program or by an external command on input line INTE2. If a 12 MHz system clock is used, the aperture time is 3us and the total conversion time is 30us. An interrupt may be requested at the completion of each conversion. There is a single result register, ADCR, and therefore in the scan mode the macro service function is useful to transfer the result of each conversion to a buffer in memory.

SERIAL INTERFACE

The uPD78312 contains a serial interface which may be used in either an I/O inteface mode or in an asynchronous communication mode. A dedicated baud rate generator is included so that the timers are available for other uses. The system clock is divided by powers of two, specified by the serial communication control register (SCC), and by the contents of the baud rate generator register (BRG). In this manner all of the common baud rates can be generated with a maximum error of 0.16%. In this asynchronous communication mode character length (7 or 8 bits), parity, and the number of stop bits (1 or 2) are specified in the serial communication mode register (SCM). The same clock is used for both transmit and receive. The CTS line is used to control transmission; the external receiving device may raise the line to signal that it is unable to receive, and thus disable the transmission. It is thus very easy to interface the uPD78312 either to a terminal or to a host processor.

In the I/O interface mode transmission is accomplished by clocking 8 bits out to the transmit buffer (TXB) under the control of the clock from the baud rate generator. The clock is available for external devices on SCK line. Reception is accomplished by clocking 8 bits into the receive buffer (RXB). In the receive case only, there is the option of using an external clock which is received on the CTS line. Used in this mode, the serial outputs (e.g. additional A/D converters) or to another processor.

In both modes simultaneous transmission and reception are possible. Interrupts may be generated when the transmit buffer is empty and when the receive buffer is full, and the macro service facility may be used to control the transfer of the data to or from memory.

THE WATCHDOG TIMER

The watchdog timer is provided to guard against inadvertent program loops. The timer can be programmed to generate non-maskable interrupts at any one of four different intervals ranging from 4.56 msex. to 349.5 msec. The program, if running properly, then resets the timer before the expiration of the selected interval. In addition, to guard against tight loops which contain the reset instruction, the interrupt is also generated if the timer is reset before the expiration of 1/16 of the selected interval. Finally the watchdog mode register is a protected location and can be written only by a special instruction.

MEMORY MAPPING AND REFRESH

The memory mapping register (MM) is used to specify the use of external memory. 256 byte, 4K byte, 16K byte or 56K byte expansion may be selected. If external memory is used, I/O Port 4 is used as the Address/Data bus. High order address bits are taken, as required, from the low order end of Port 5. The remaining Port 5 bits (0, 2, 4 or 8) can be used for standard I/O. If required for slow memory, 0, 1, 2 or 3 additional wait states can be specified to be included in instructions which read and write to external memory.

Refresh pulses may be generated to allow the use of pseude-static DRAM as external memory. The refresh mode register (RFM) is used to specify whether or not the refresh pulse is enabled, one of 4 intervals ranging from 16 to 128 cycles of the system clock. The refresh pulses are timed to follow read or write operations in order to avoid interference and possible malfunction of the DRAM.

STANDBY MODES

Two standby modes are provided to conserve power when the attention of the CPU is not required. In the first, the HALT mode, the CPU is stoppped, but the clock is allowed to continue running. Any interrupt request of a priority higher than the current one will re-start the processor immediately. In the second, the STOP mode, both the processor and the clock are stopped. In this case either a system RESET or an external non-maskable interrupt is required to re-start the system. It is then necessary to wait for the clock to stabilize before the CPU may be re-started. The watchdog timer is used to time the necessary wait, and the program is re-started at either the reset vector or the non-maskable interrupt vector.

Either of these modes can be entered by setting the appropriate bit in the standby control register (STBC). The register also contains a flag (SBF) which should be set by the program when the stop mode is entered. This bit is cleared at initial power-up , so the reset routine is able to determine whether the system has been started after power-down or is merely being re-started from the stop mode. There is one additional method of saving power. If the CK1 bit of the STBC is set, the system clock is slowed by a factor of 4, i.e. SCLK becomes one eighth of the crystal frequency instead of half. The CK1 bit is set by external RESET, and therefore the software must clear it before the processor and peripheral clocks will run at full speed. Like the watchdog mode register, the standby control register is a protected location and can only be written by a special instruction.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}		-0.5~+7.0	V
	V_{REF}		-0.5~V_{DD}	V
	AVSS		-0.5~+0.5	V
Input Voltage	V_I		-0.5~+7.0	V
Output Voltage	V_O		-0.5~+7.0	V
Output Current Low	I_{OL}	All Output Pin	4.0	mA
		All Output Pin Total	100	mA
Output Current High	I_{OH}	All Output Pin	- 1	mA
		All Output Pin Total	-25	mA
Operating Temperature	T_{opt}		-10~+70	°C
Storage Temperature	T_{stg}		-65~150	°C

OPERATNG CONDITION

Parameter / Osc. Freq.	Condition	Ta	V_{DD}
fxx≦12MHz		-10~+70°C	+5.0V±5%
fxx≦ 9MHz	With Refresh Mode		

CAPACITANCE

(T_a=25°C, V_{DD}=V_{SS}=0V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C_I	f=1MHz			10	pF
Output Capacitance	C_O				20	pF
I/O Capacitance	C_{IO}				20	pF

($T_a = -40°C$ to $+85°C$, $V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$)

DC CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Low Voltage	V_{IL}	EXCEPT $\overline{EA}$	0		0.8	V
	V_{IL2}	$\overline{EA}$	0		0.5	V
Input High Voltage	V_{IH1}	All except X2, X1, $\overline{RESET}$, P20/NMI	2.2		V_{DD}	V
	V_{IH2}	X2, X1, $\overline{RESET}$, P20/NMI	3.8		V_{DD}	V
Ouptput Low Voltage	V_{OL}	$I_{OL} = 2.0mA$			0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu A$	2.4			V
Input Current	I_I	$\overline{RESET}$, P20/NMI, $0.45V < V_I < V_{CC}$			±10	μA
Input Leakage Current	I_{LI}				±10	μA
Output Leakage Current	I_{LO}				±10	μA
AV_{REF}	AI_{REF}	$f_{CLK} = 6MHz$		1.5	5	mA
V_{DD} Power Current	I_{DD1}	Running Mode, $f_{CLK} = 6MHz$		30	90	mA
V_{DD} Halt Current	I_{DD2}	Halt Mode, $f_{CLK} = 6MHz$		5	15	mA
V_{DD} Stop Current	I_{DDDR}	$V_{DDDR} = 2.0V$		0.1	0.4	mA
		$V_{DDDR} = 5.0V \pm 5\%$		1	4	mA
Data Retention Voltage	V_{DDDR}	Stop Mode	2.0			V

READ/WRITE OPERATION ($T_a = -40°C$ to $+85°C$, $V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$)

AC CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Max.	Units
Internal System Clock *1	tCLK		166		ns
		in Refresh Mode	222		ns
Address Setup to ALE ↓	tAL		150		ns
Address Hold from ALE ↓	tLA	*3, $C_L = 100pF$, $R_L = 2k\Omega$	30		ns
Address to $\overline{RD}$ ↓ delay time	tAR		230		ns
$\overline{RD}$ ↑ to Address floating	tAFR			0	ns
Address to Data output	tAD			410	ns
ALE ↓ to Data Input	tLDR			230	ns
$\overline{RD}$ ↓ to Data Input	tRD			180	ns
ALE ↓ to $\overline{RD}$ ↓ Delay Time	tLR		60		ns
Data Hold Time from $\overline{RD}$ ↑	tRDH		0		ns
$\overline{RD}$ ↑ to Address active	tRA		50		ns
$\overline{RD}$ ↑ to ALE ↑ Delay Time	tRL		100		ns
$\overline{RD}$ Width Low	tRR		200		ns
ALE Width High	tLL		120		ns
Address to $\overline{WR}$ ↓ Delay	tAW		300		ns
ALE ↓ to Data Output	tLDW			190	ns
$\overline{WR}$ ↓ to Data Output	tWD			100	ns
ALE ↓ to $\overline{WR}$ ↓ Delay Time *2	tLW		30		ns
	tLW1	in Refresh Mode	110		ns
Data Setup Time to $\overline{WR}$ ↑	tDW		150		ns
Data Setup Time to $\overline{WR}$ ↓	tDWS		30		ns
Data Hold Time from $\overline{WR}$ ↑	tWDH	*3	20		ns
$\overline{WR}$ ↑ to ALE ↑ Delay Time	tWL		110		ns
$\overline{WR}$ Width Low	tWW		200		ns

Notes:

*1. Internal System Clock is derived from f_{XTAL} by dividing by 2 or 8, selectable with the STBC register Table above are for following conditions:
$f_{XTAL} = 12$ MHz, SCLK = $f_{XTAL}/2$, $t_{cyc} = 1/f_{XTAL}$

*2. During Refresh pulse generation the falling edge of WR is delayed for 1/2 cycle

*3. t_{AL} speciefied also for Halt Mode, with condition V_{OH}, V_{OL} held during Halt Mode

SERIAL OPERATION

(T_a = −40°C to +85°C, V_{DD} = 5.0V±5%, V_{SS} = 0V)

AC CHARACTERISTICS

Parameter	Symbol	Test Conditions			Min.	Max.	Units
$\overline{SCK}$ Cycle Time	tCYK	Output	$\overline{SCK}$	*1	1.33		μs
			$\overline{CTS}$	*2	1.33		μs
		Input	$\overline{CTS}$	*3	1		μs
$\overline{SCK}$ Width Low	tKKL	Output	$\overline{SCK}$	*1	580		ns
			$\overline{CTS}$	*2	580		ns
		Input	$\overline{CTS}$	*3	420		ns
$\overline{SCK}$ Width High	tKKH	Output	$\overline{SCK}$	*1	580		ns
			$\overline{CTS}$	*2	580		ns
		Input	$\overline{CTS}$	*3	420		ns
$\overline{CTS}$ Width High/Low	tCTSH, tCTSL			*4	3		tCLK
RxD Setup Time to $\overline{SCK}$ ↑	tRXK				80		ns
RxD Hold Time from $\overline{SCK}$ ↑	tKRX				80		ns
$\overline{SCK}$ ↑ to TxD Delay Time	tKTX					210	ns

A/D CONVERTER CHARACTERISTICS

(T_a = −40°C to +85°C, V_{SS} = AV_{SS} = 0V, 3.4V ≤ V_{AREF} ≤ V_{DD}, V_{DD} = +5V ± 5%

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Resolution			8			Bit
Absolute Accuracy		T_a = −10°C to 70° 83ns ≤ t_{cyc} ≤ 170ns			0.4%±1/2	LSB
		83ns ≤ t_{cyc} ≤ 170ns			0.6%±1/2	LSB
		3.4V ≤ V_{REF} ≤ V_{DD}			0.8%±1/2	LSB
Conversion Time	TCONV	83ns ≤ t_{cyc} ≤ 125ns	360			t_{cyc}
		125ns ≤ t_{cyc} ≤ 250ns	240			t_{cyc}
Sampling Time	TSAMP	83ns ≤ t_{cyc} ≤ 125ns	72			t_{cyc}
		125ns ≤ t_{cyc} ≤ 250ns	48			t_{cyc}
Input Voltage	VIAN		0		V_{AREF}	V
Analog Input Impedance	RAN			1000		MΩ
Analog Reference Voltage	AVREF		3.4		V_{DD}	V
AV_{REF} Current	IVREF	t_{cyc} = 12MHz		1.5	5.0	mA

AC CHARACTERISTICS

UP/DOWN COUNTER INPUT (T_a = −40°C to +85°C, V_{DD} = 5.0V±5%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	Min.	Max.	Units
CI0, CI1 High/Low Time	tCIH, tCIL		3		tCLK
CTRL0, CTRL1 High/Low Time	tCTLH, tCTLL		3		tCLK
CTRL0, CTRL1 Setup Time against CI ↑	tCTCIS	in Mode 3, CI programmed on rising edge	2		tCLK
CTRL0, CTRL1 Hold Time against CI ↑	tCICTH	in Mode 3, CI programmed on rising edge	5		tCLK
CLRØ, CLR1 High/Low Time	tCLRH, tCLRL		3		tCLK

INTERRUPT INPUT (T_a = −40°C to +85°C, V_{DD} = 5.0V±5%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	Min.	Max.	Units
NMI Input High/Low	tNIH, tNIL		10		μs
INTE0 Input High/Low	tI0H, tI0L		3		tCLK
INTE1 Input High/Low	tI1H, tI1L		3		tCLK
INTE2 Input High/Low	tI2H, tI2L		3		tCLK
$\overline{\text{RESET}}$ Input High/Low	tRSH, tRSL		10		μs

X1 INPUT (T_a = −40°C to +85°C, V_{DD} = 5.0V±5%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	Min.	Max.	Units
X1 Input High	tXH		30	130	ns
X1 Input Low	tXL		30	130	ns
X1 Rise Time	tr		0	30	ns
X1 Fall Time	tf		0	30	ns
X1 Cycle Time	tX		83	250	ns

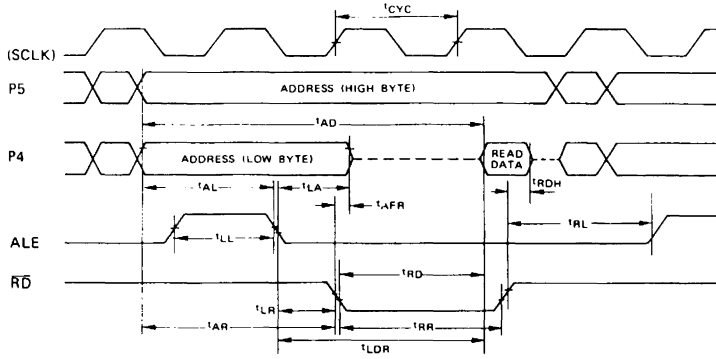
AC CHARACTERISTICS

BUS TIMING DEPENDING ON t_{cyc} ($T = 1/SCLK = 2\ t_{cyc}$ min)

Symbol	Calculation Expression	Min./Max.	Units
t_{AL}	3T/2 – 100	Min	ns
t_{AR}	2T – 100	Min	ns
t_{AD}	7T/2 – 170	Max	ns
t_{LDR}	(2+n) T – 100	Max	ns
t_{RD}	(3/2 + n) T – 70	Max	ns
t_{LR}	T/2 – 20	Min	ns
t_{RL}	T – 50	Min	ns
t_{RA}	0,5T – 30	Min	ns
t_{RR}	(3/2 + n) T – 50	Min	ns
t_{LL}	T – 40	Min	ns
t_{AW}	2. T – 100	Min	ns
t_{LDW}	0.5T + 110	Max	ns
t_{LW}	T/2 – 20	Min	ns
t_{LW1}	T – 50	Min	ns
t_{DW}	3T/2 – 100	Min	ns
t_{LW1}	T – 50	Min	ns
t_{WDH}	T/2 – 60	Min	ns
t_{WL}	T – 50	Min	ns
t_{WW}	(3/2 + n) T – 50	Min	ns

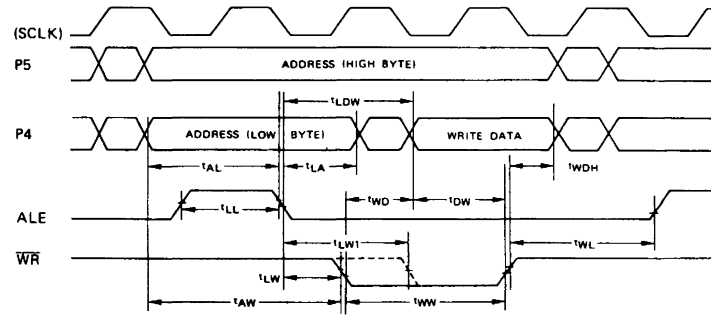
Notes:
1. n = number of Wait cycles programmed in MM register (Memory Mapping Register)
2. T = 1/SCLK (SCLK is internal system clock)
   T = a) 2 t_{cyc}
   b) 8 t_{cyc} depending on STBC register
   calculation above is done for case a)
3. items not appearing above are not depending on SCLK

READ OPERATION (NO WAIT)



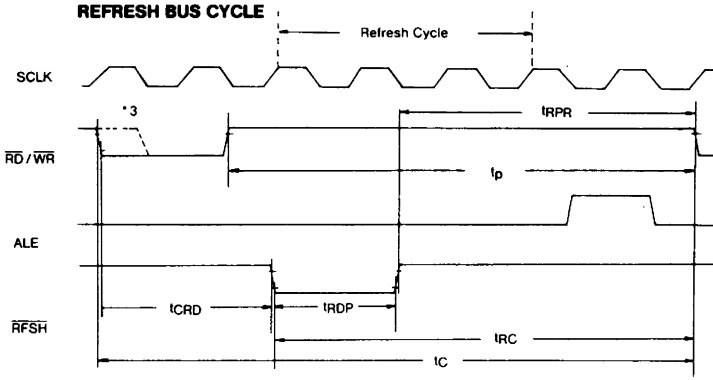
TIMING CHARTS

WRITE OPERATION (NO WAIT)



TIMING WAVEFORMS (CONTINUED)

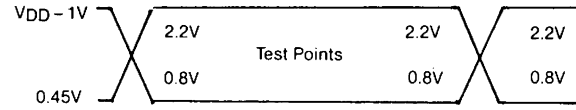
REFRESH BUS CYCLE



Symbol	Calculating Expr.	fXTAL = 6MHz		fXTAL = 8MHz		fXTAL = 10MHz		Units
		Min	Max	Min	Max	Min	Max	
tCRD	(1.5+n) tcyc - 40	210		147		110		ns
tRDP	1.5 tcyc - 40	210		147		110		ns
tp	5.5 tcyc - 40	840		647		510		ns
tRPR	3.5 tcyc - 40	540		397		310		ns
tC	(7+n) tcyc - 40	1120		835		660		ns
tRC	5 tcyc - 40	760		585		460		ns

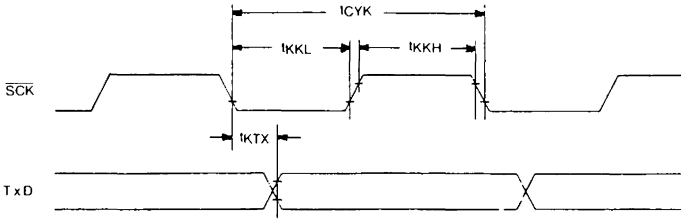
Notes:
1. $t_{cyc} = 1/f_{XTAL}$, Divide ratio internally: SCLK = 1/2 f_{XTAL}
2. n = Number of Wait cycles programmed in the MM register (Bits PW1, PW0)
3. for $\overline{WR}$ signal the dotted line is valid

AC TIMING TEST POINTS

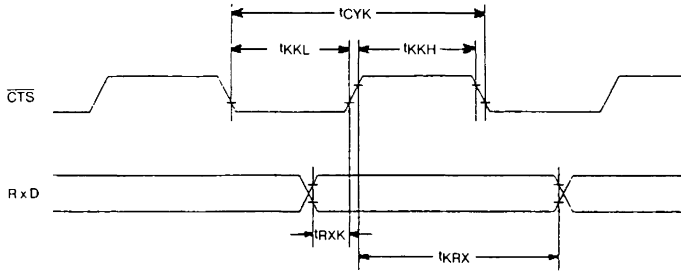


TIMING WAVEFORMS

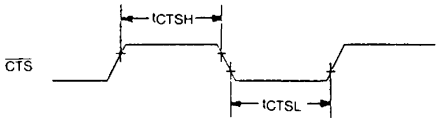
I/O INTERFACE MODE



I/O INTERFACE MODE

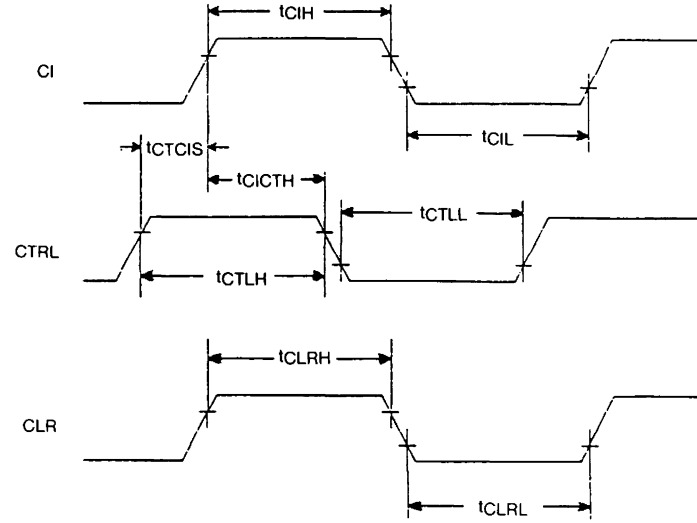


CTS HANDSHAKE SIGNAL



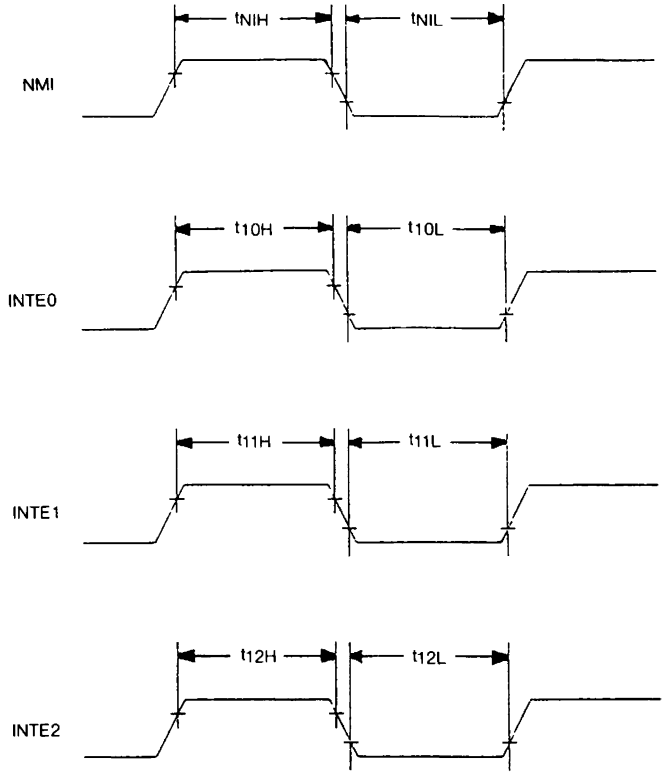
TIMING WAVEFORMS

UP/DOWN COUNTER INPUT

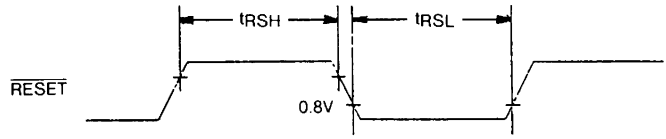


TIMING WAVEFORMS

INTERRUPT INPUT

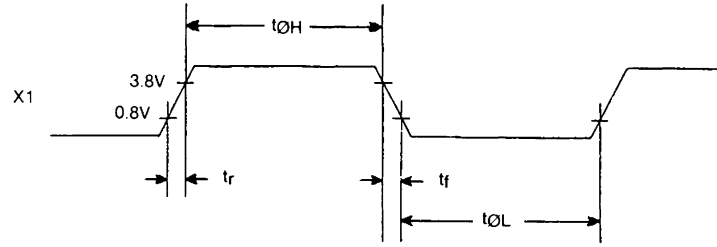


RESET INPUT



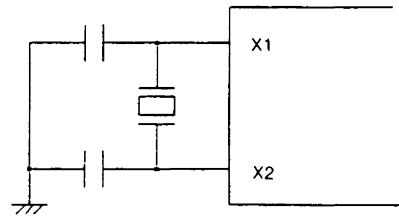
TIMING WAVEFORMS

X1 CLOCK INPUT

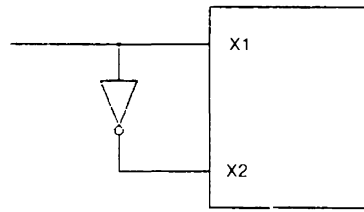


X1, X2 INPUT CONNECTION

A.) CRYSTAL CONNECTION



B.) EXTERNAL CLOCK SUPPLY



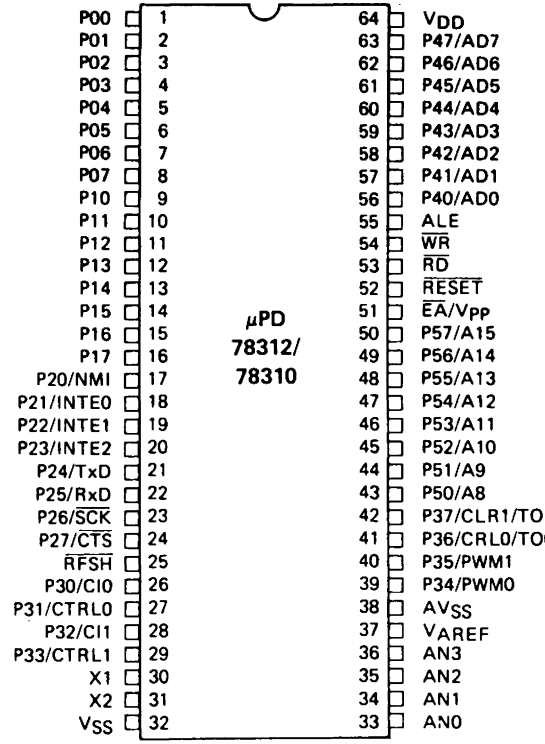
(T_a = −40°C to + 85°C)

DATA RETENTION DURING STOP

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Data Retention Voltage	V_{DDDR}		2.0			V
V_{DD} Stop Current	I_{DDDR}	V_{DDDR} = 2.0V		0.1	0.4	mA
		V_{DDDR} = 5.0V ± 5%		1	4	mA

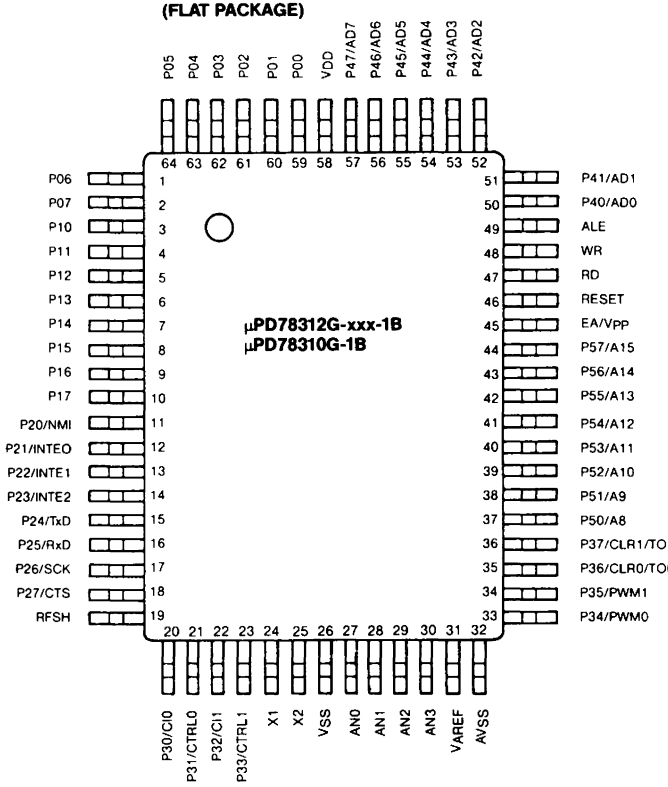
PINNING OUTLINE

(QUIL AND SHRINK DIP)



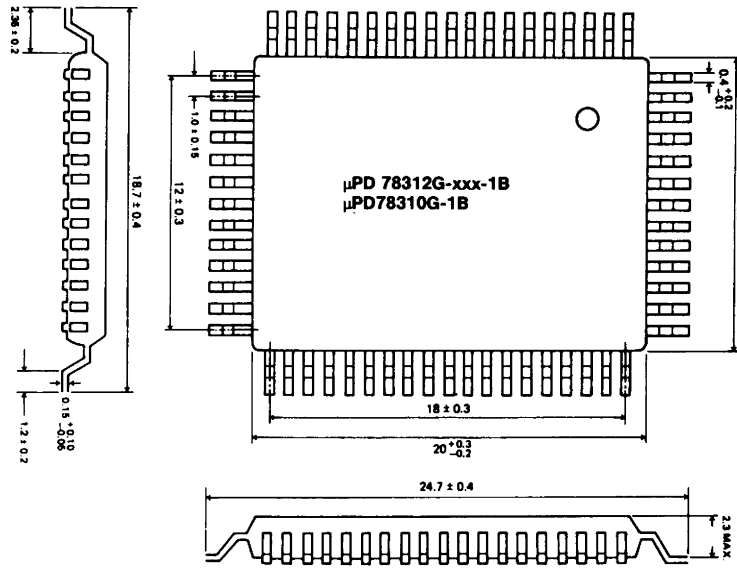
PINNING OUTLINE

(FLAT PACKAGE)



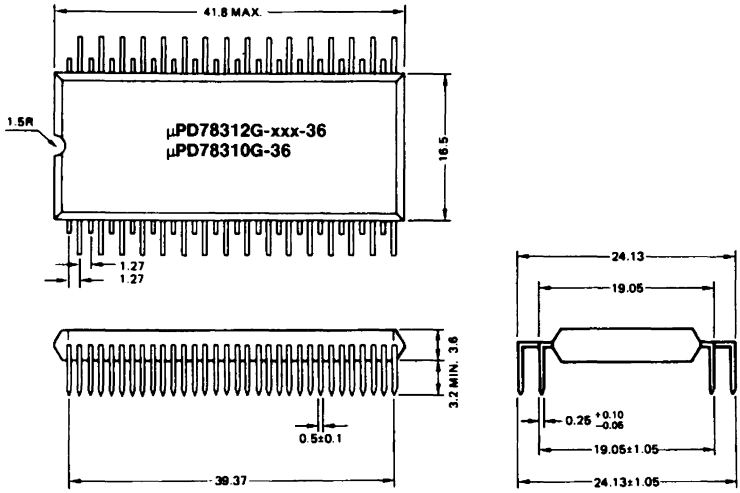
PACKAGE DIMENSIONS,

64-pin FLAT PACK



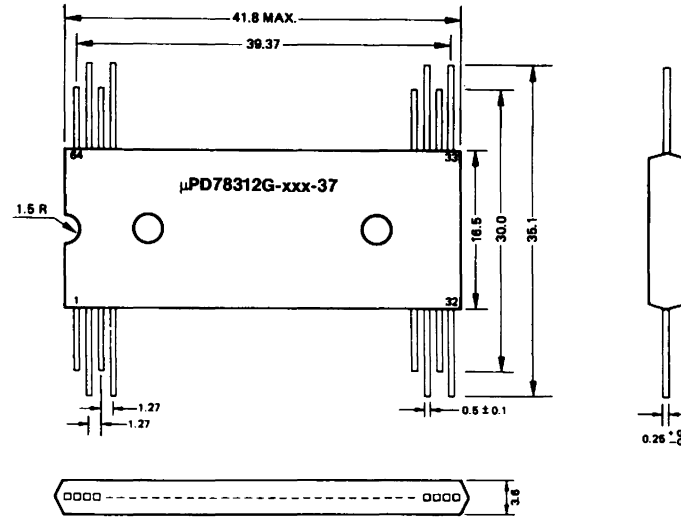
PACKAGE DIMENSIONS,

64-pin QUIL, bent leads



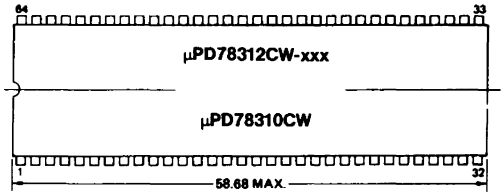
PACKAGE DIMENSIONS,

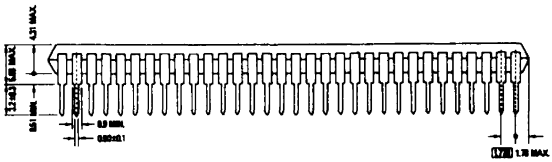
64-pin QUIL, flat leads

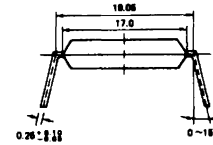


PACKAGE DIMENSIONS,

64-pin SHRINK DIP



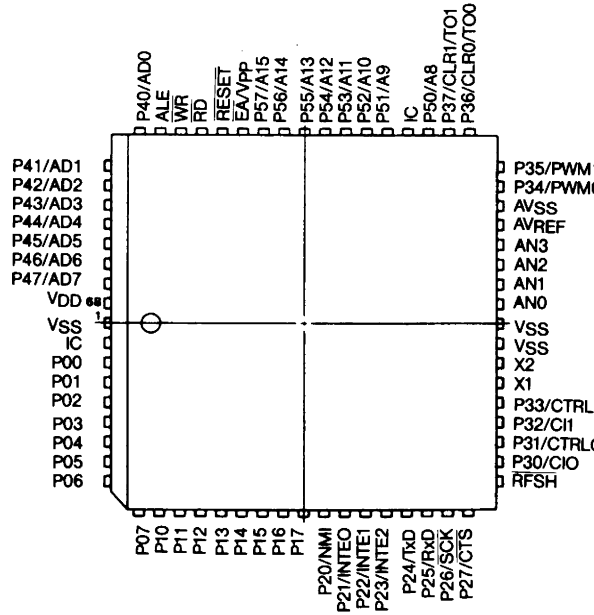




PINNING OUTLINE

μPD78310/312L

68PIN PLCC



Appendix

Differences between μPD78P312 and μPD78312, 78310

The μPD78P312 is a product which has replaced masked ROM of the μPD78312 with the EPROM. Table 2-1 shows the differences between these products.
However, see the μPD78312, 78310 User's Manual for the details of CPU function and on-chip peripherals.

Table 2-1

Items	μPD78P312	μPD78312	μPD78310
On-chip Program Memory	● EPROM ● 8192 x 8-bit	● Masked ROM ● 8192 x 8-bit	Not on chip
No. 7 pin	P06 / $\overline{PGM}$	P06	
No. 8 pin	P07 / $\overline{OE}$	P07	
No. 51 pin	$\overline{EA}$ / V_{PP}	$\overline{EA}$	
Supply Voltage Range	V_{DD} = 5 V ± 10 %	V_{DD} = 2.5 V to 6.0 V	
Packages	● 64-pin ceramic Shrink DIP with window (DW) ● 64-pin ceramic QUIP with window (R) ● as OTPROM also in plastic QUIL (G), SDIP (CW) and PLCC (L)	● 64-pin plastic shrink DIP (CW) ● 64-pin plastic QUIP (G) ● 64-pin plastic flat package (G) ● 68-pin plastic LCC (L)	

A.1. EPROM Write and Verify

The μPD78P312 has internal UV erasable and electrically programmable read only memory (EPROM). For write and verify the EPROM, these pins in the following table are used.

Pin names	Functions
V_{PP}	High voltage input (for write)
P_{17}-P_{10}	Address inputs (lower 8-bit)
P_{54}-P_{50}	Address inputs (upper 5-bit)
P_{47}-P_{40}	Data inputs (for write), Data outputs (for verify)
$\overline{PGM}$ / P_{06}	Program pulse input
$\overline{OE}$ / P_{07}	Output enable input
V_{DD}	Supply voltage input V_{DD} = 5 V ± 10% at normal operation V_{DD} = 6 V at EPROM write / verify

A.2. EPROM write / verify operation mode

The μPD78P312 enters program write / verify mode when "V_{DD} = + 6 V, V_{PP} = + 12.5 V" are set. There are three operation modes by setting of the $\overline{PGM}$ and $\overline{OE}$ pins. (other pins must be pulled down to V_{SS} by pull-down resistors.)

Specify operation mode				Operation mode
V_{PP}	V_{DD}	$\overline{PGM}$	$\overline{OE}$	
+ 12.5 V	+ 6 V	L	H	Write mode
		H	L	Verify mode
		H	H	Program Inhibit mode

A.3 EPROM Write operation

Fast EPROM data write operation is done in the following procedure.

(1) Pull down unused pins to the V_{SS} by pull-down resistors. Supply + 6 V to V_{DD} and + 12.5 V to V_{PP}.
(2) Set initial address.
(3) Set write data.
(4) Supply program pulse (active low) of 1-ms to the $\overline{PGM}$ pin.
(5) Verify. If written data is right, go to (7), otherwise repeat (3) to (5).
If the right data is not given even 25 times repetition, go to (6).
(6) Stop the write operation. That device is bad.
(7) Additional write. Set the same data and supply program pulse as long as the "number of repeat-times at (3) to (5)" x 3 ms.
(8) Increment the address.
(9) Repeat (3) to (8) until the end address.

A.4. Timing Chart

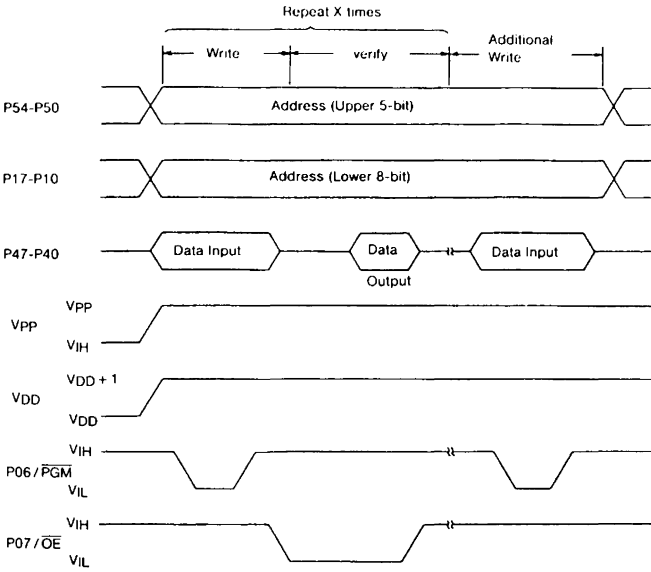


Fig. 3-1 EPROM Write / Verify Timing

PRELIMINARY

μPD78224

8-BIT CPU FAMILY BOOSTS THROUGHPUT.

STREAMLINED CONTROLLERS UP INSTRUCTION RATES

DAVE BURSKY

As embedded control applications that rely on 8-bit microcontrollers get more challenging, current generation single-chip microcontrollers are starting to bog down as applications demand more processing in less time. And, due to system cost constraints, most applications can't afford to move to the more powerful and costlier 16-bit all-in-one processors. To solve that processing dilemma, a forthcoming family of 8-bit controllers from NEC manages to boost the throughput by moving to an architecture that resembles the latest reduced-instruction-set computers.

The NEC family processors have more efficient instructions that require just two clock cycles to execute, rather than the typical 8 to 16 cycles needed by such popular chips as the Intel 8051 and the Motorola 68HC11. However, rather than use its existing 8-bit microcontroller architecture, NEC decided to create a new, more streamlined family—the 78K2 series—which can execute its 65 commands at a rate of one instruction every two clock cycles. Consequently, with a 12-MHz clock, NEC's controllers have a minimum instruction execution time of 333 ns. That time will shrink to 250 ns when the clock frequency goes up to 16 MHz in an upgraded version already slated for early 1990.

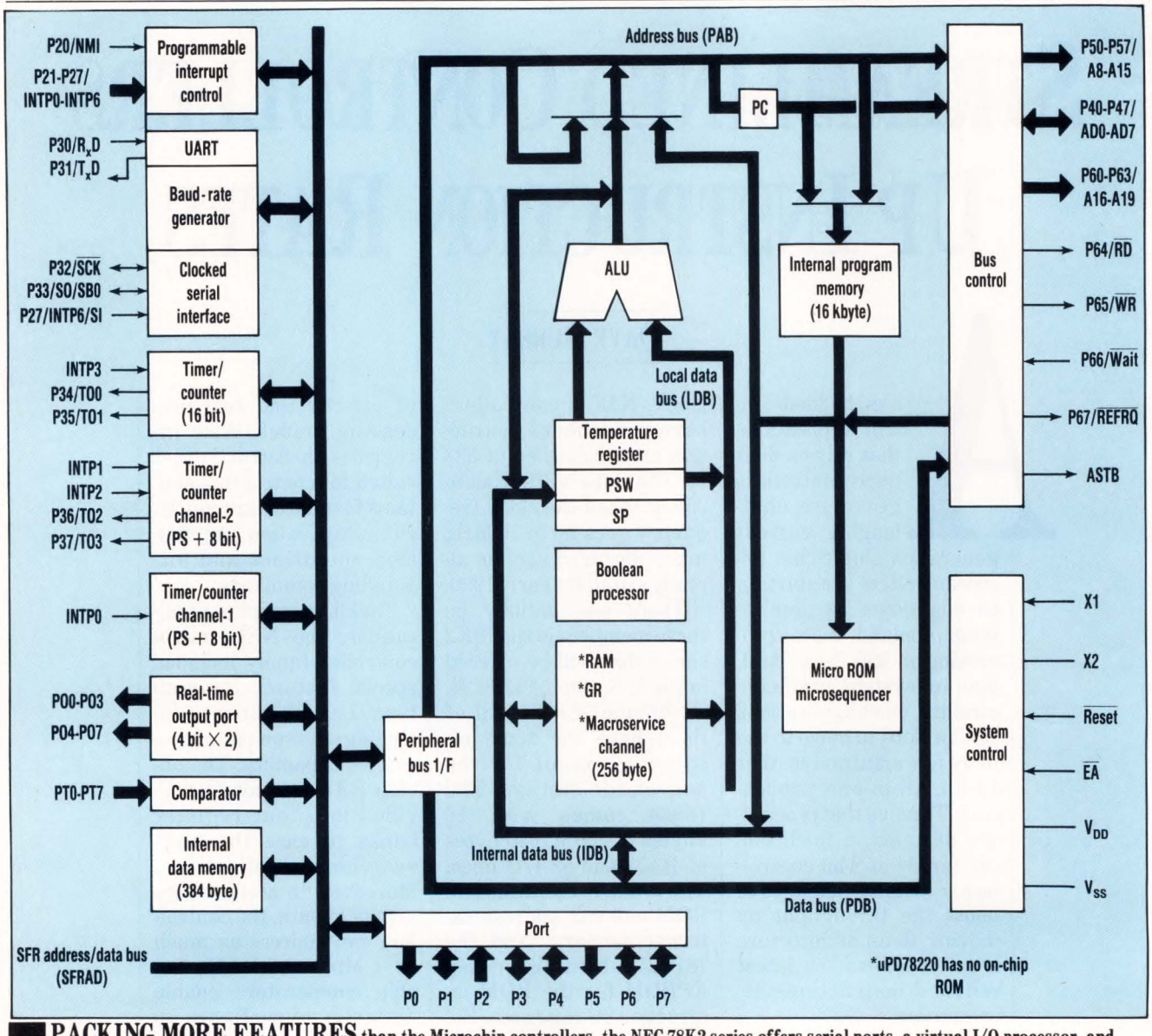
There will initially be three members in the 78K2 series that will be offered in the U.S., the μPD78224, 78220, and 78P224. All of them have the same resources, except for the nonvolatile storage. The 78224 comes with 16 kbytes of ROM, 640 bytes of RAM and 63 I/O lines. The 78220 contains no ROM and can address external memory. And the 78P224 substitutes on-chip EPROM for the ROM instruction storage area. Beyond those chips, NEC plans to release the 78233 and 78234, which are ROM-less and ROM-based versions of the 7822x series that include dual-channel 8-bit digital-to-analog converters and the ability to build an 8-channel, 8-bit a-d converter *(see the figure)*.

Common resources beyond the memory include a clocked serial channel, a full serial UART port, three counter-timers (one 16-bit and a pair of 8-bit units), and an on-chip interrupt controller capable of two programmable levels of priority and two processing modes. Also included is an instruction set suited for control that contains fast hardware-assisted multiplication and division operations and bit-handling commands.

Tackling complex applications, the NEC microcontroller family includes special features for real-time I/O operations, including an unusual microservice capability. The on-chip RAM can also be divided into four register banks to ease the task-switching applications. Moreover, to access large arrays of data, the controllers can address as much as 1 Mbyte of RAM. On-chip comparators enable designers to configure up to eight-channel 8-bit a-d converters, two-channel d-a converters, and 8-channel analog comparators.

The macroservice routine aspect of the I/O channels makes it possible for bit, nibble, or byte-wide data to be transferred automatically from memory to a real-time output port. This ability frees designers to come up with such applications as eight-variable frequency-duty-cycle pulse-width modulated controllers to stepper-motor acceleration-deceleration patterns. The

ENHANCED 8-BIT CPU FAMILY



PACKING MORE FEATURES than the Microchip controllers, the NEC 78K2 series offers serial ports, a virtual I/O processor, and analog-interface circuits that implement a-d converters, pulse-width modulated controllers, and d-a converters.

PRICE AND AVAILABILITY

The PIC 16C54 and C55 will come in 18- or 28-lead one-time programmable plastic or windowed reprogrammable ceramic packages. The 16C54 sells for $2.40 (2500); the 16C55 costs $2.95. Production quantities are immediately available. The NEC 78K2 comes in plastic leadless packages and costs $6.70 in lots of 10,000.

NEC Electronics Inc., 401 Ellis St., P.O. Box 7241, Mountain View, CA 94039; Ian Olsen, (415) 960-6000. **CIRCLE 512**

macroservice capability can be compared to a virtual I/O processor because the service feature operates somewhat behind the scenes to transfer either individual bytes or blocks of data, which can be transferred between any combination of memory and peripherals.

Macroservice ports can handle the rapid output of tabular information, such as information for nonlinear PWM systems. Associated with the I/O lines, the processors have 256 kbytes of special function registers. Those registers aid the implementation of logic operations associated with an I/O line. The tabular transfers can calculate the ΔF (change in force) and ΔT (change in time), as required by a stepper motor. Future family members will include versions with more EPROM and I/O lines, as well as some advanced analog features. The newly released devices, though, can implement 8-bit 8-channel a-d converters, eight 4-bit analog comparators, or dual 8-bit d-a converters.□

HOW VALUABLE?	CIRCLE
HIGHLY	562
MODERATELY	563
SLIGHTLY	564

uPD78224 REALTIME CONTROL ORIENTED 8-BIT SINGLE-CHIP MICROCOMPUTER

The 8-bit single-chip microcomputer uPD78224 is a control oriented microcomputer that contains a 16k-byte masked ROM, a 640-byte RAM, a multifunction pulse I/O, variable threshold input port, and various other hardware peripherals.

Major Features

* High-performance CPU

The uPD78224's internal 8-bit ALU and data paths, enable high-speed program execution with low power consumption.

The instruction set is tuned for control applications, including 16/8-bit divide, 8x8-bit multiply. In addition, built-in boolean processor enhances the performance of the bit manipulate instructions.

* Multifunction pulse I/O

The multifunction pulse I/O consists of four units. The first unit is composed of a 16-bit timer, two 16-bit compare registers and a 16-bit capture register. The second unit is composed of an 8-bit timer with pre-scaler, an 8-bit compare register and an 8-bit capture/compare register. The third unit is composed of an 8-bit timer/counter with pre-scaler, two 8-bit compare registers and an 8-bit capture register. Fourth unit is a twox4-bit realtime output port. These units enable direct interface with various types of external sensors and actuators, and realize the high precision and flexible control system all by uPD78224 itself.

* Macro service function

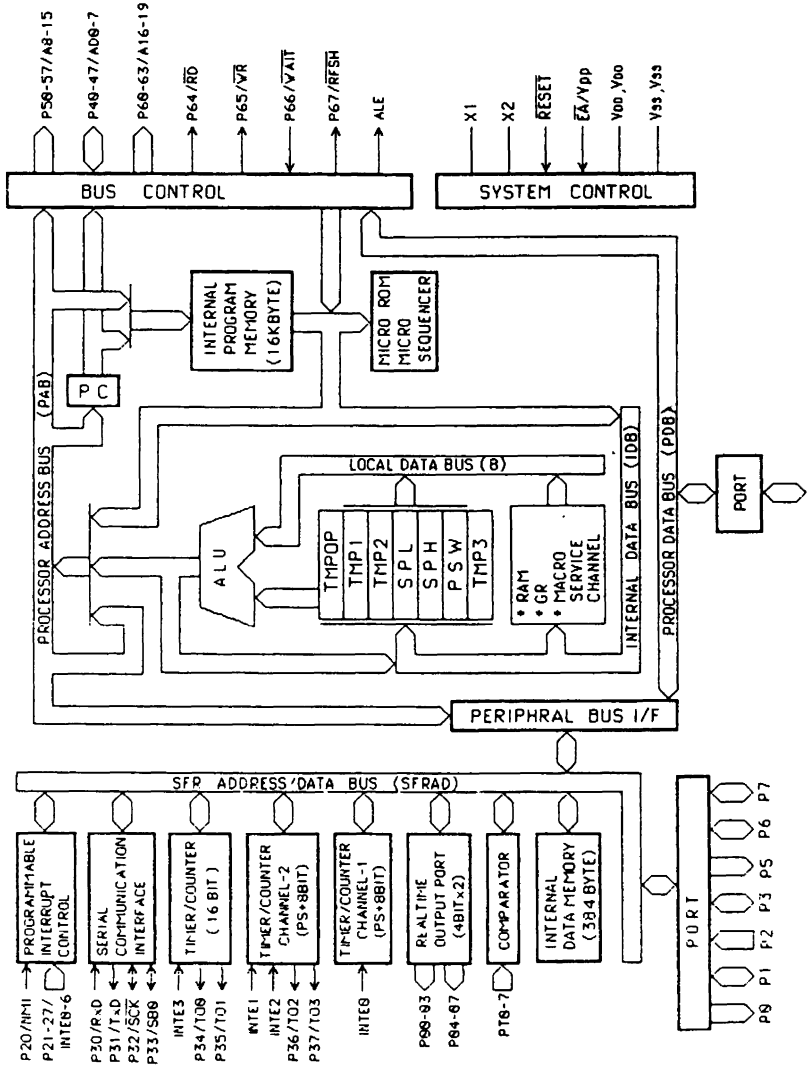
The macro service function is one of the characteristic features of the uPD78224. By using this function, the macro service controller, upon recognizing an interrupt request, automatically executes necessary processing to service the request on behalf of the CPU.

In the past, interrupt handling, register return, and register save processing, associated with the interrupt service by the CPU, accounted for a major proportion of CPU time. Macro service facilitates faster interrupt handling by eliminating such related processing operations.

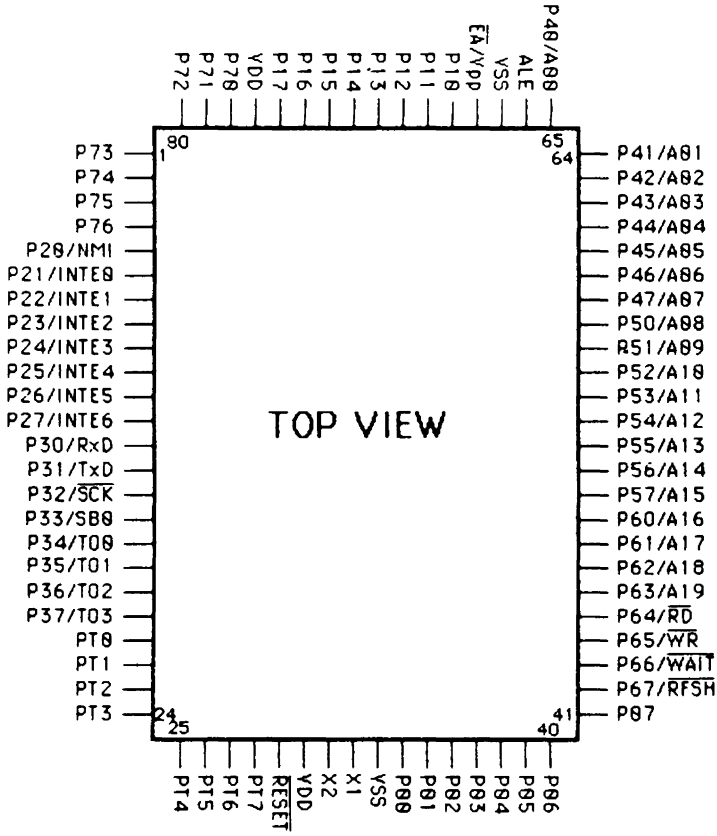
1. Features

* Control Oriented Instruction Set
  - 16-bit Data Transfer & Arithmetic
  - Powerful Bit Manipulations
* Instruction Cycle : min. 2 system clocks
* 16k-byte ROM, 640-byte RAM
* Expansion Capabilities
  - Program Memory : Up to 64k-bytes
  - Data Memory : Up to 1M-bytes
* Multifunction Pulse Input/Output
  - Two 8-bit Timer
  - One 16-bit Timer
  - Two 4-bit Realtime Output Port
* Variable Threshold Input Port
* Asynchronous Serial Communication Interface (UART)
* Clocked Serial Interface (CSI)
  - I/O expansion Mode
  - Serial Bus Interface (SBI)
* Interrupt Controller
  - Two Priority and Two-level Nesting Control
  - Eight External Interrupt Sources
  - Nine Internal Interrupt Sources
* Macro Service Controller
  - 6 Macro Service Channel
* Programmable Wait Control
* Pseudo-static RAM refresh function
* Standby Operation
* CMOS
* 80-pin Flat Package / 84-pin PLCC

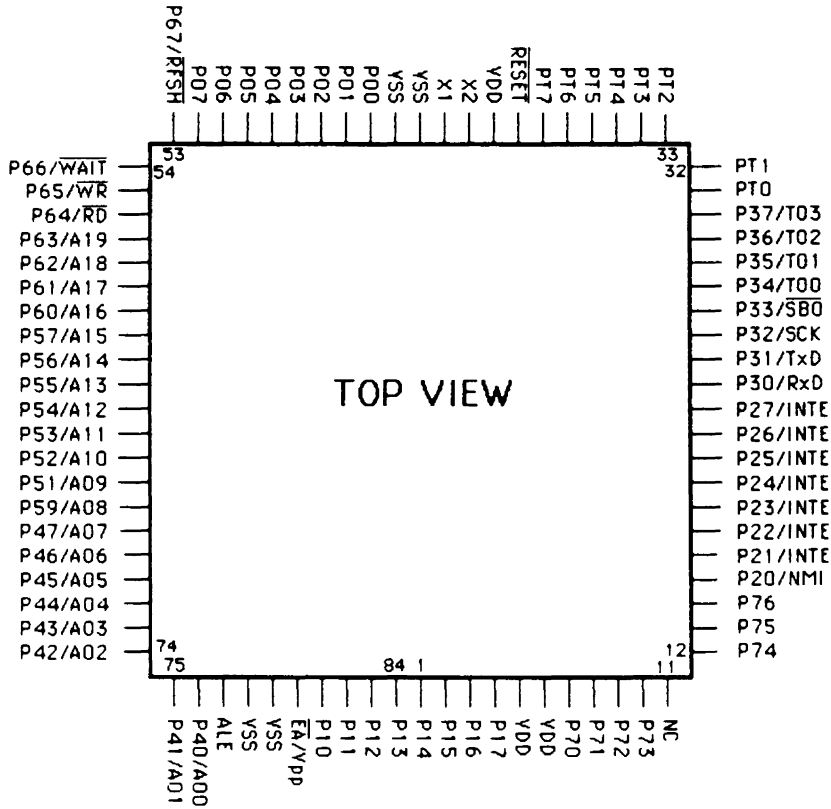
2. Block diagram of uPD78224



μPD78224 PIN CONFIGURATION (80 PIN FLAT)



μPD78224 PIN CONFIGURATION
(84 PIN PLCC)



PINS DESCRIPTION (1)

X1,X2	CRYSTAL INPUT
$\overline{\text{RESET}}$	POWER-ON H/W RESET
V_{DD}	+5V ± 10%
V_{ss}	GND
ALE	ADDRESS LATCH ENABLE
$\overline{\text{EA}}$/Vpp	EXTERNAL ACCESS / PROGRAM POWER SUPPLY

PINS DESCRIPTION (2)

PT0-T7	8-BIT INPUT PORT with COMPARATOR
P00-07	8-BIT OUTPUT PORT or 2x4BIT REALTIME OUTPUT PORT
P10-17	8-BIT GENERAL I/O PORT (Iol=8mA EACH OUTPUT)
P20-27	8-BIT INPUT PORT or INPUTS INDIVIDUALLY PROGRAMABLE as INTERRUPT NMI,INTE0,INTE1,INTE2,INTE3,INTE4,INTE5,INTE6
P30-37	8-BIT GENERAL I/O PORT or 8-BIT CONTROL SIGNALS
	P30/RxD (INPUT)
	P31/TxD (OUTPUT)
	P32/$\overline{SCK}$ (INPUT/OUTPUT)
	P33/SB0 (INPUT/OUTPUT)
	P34/TO0 (OUTPUT)
	P35/TO1 (OUTPUT)
	P36/TO2 (OUTPUT)
	P37/TO3 (OUTPUT)
P40-47	8-BIT GENERAL I/O PORT or ADDRESS/DATA BUS
P50-57	8-BIT OUTPUT PORT or UPPER 8-BIT ADDRESS BUS
P60-67	8-BIT GENERAL I/O PORT or CONTROL SIGNAL
	P60/A16 (OUTPUT)
	P61/A17 (OUTPUT)
	P62/A18 (OUTPUT)
	P63/A19 (OUTPUT)
	P64/$\overline{RD}$ (OUTPUT)
	P65/$\overline{WR}$ (OUTPUT)
	P66/$\overline{WAIT}$ (INTPUT)
	P67/$\overline{RFSH}$ (OUTPUT)
P70-76	7-BIT GENERAL I/O PORT

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Condition	Ratings	Unit
Power Supply Voltage	V_{DD}		- 0.5 to + 7.0	V
Input Voltage	V_I		- 0.5 to V_{DD} + 0.5	V
Output Voltage	V_O		- 0.5 to V_{DD} + 0.5	V
High Level Output Current	I_{OH}	One Output Pin	- 2	mA
		All Output Pin Total	- 50	mA
Low Level Coutput Current	I_{OL}	One Output Pin	Peak 30	mA
			Average 15	mA
		All Output Pin Total	Peak 150	mA
			Average 100	mA
Operating Temparature	T_{OPT}	$f_{XTAL} \leq 10$ MHz	- 40 to + 85	°C
Storage Temparature			- 65 to + 150	°C

Recommended Operating Conditions

Parameter		Ta	V_{DD}, AV_{DD}
OSC frequency	$f_{XTAL} \leq 10$ MHz	- 40°C to + 85°C	+ 5.0V ± 10%

Capacitance (Ta = 25°C, $V_{DD} = V_{SS} = 0V$)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Capacitance	C_I	fC = 1 MHz			10	pF
Output Capacitance	C_O	Unmeasured Pins			20	pF
In/Output Capacitance	C_{IO}	Returned to 0V			20	pF

DC Characteristics (Ta = - 40 to + 85°C, VDD = + 5.0 V ± 10%, VSS = 0V)

Parameter	Symbol	Test Condition	MIN	Typ	Max	Unit
Input Low Voltage	V_{IL}	except PTn	0		0.8	V
Input High Voltage	V_{IH1}	except note1 and PTn	2.2		V_{DD}	V
	V_{IH2}	note1 Pins	0.8V_{DD}		V_{DD}	V
Output Low Voltage	V_{OL1}	I_{OL} = 2.0mA, except Port1			0.45	V
	V_{OL2}	I_{OL} = 8.0mA, Port1			1.0	V
Output High Voltage	V_{OH1}	I_{OH} = -1.0mA	V_{DD} -1.0			V
	V_{OH2}	I_{OH} = 100μA	V_{DD} -0.5			V
Input Leak. Current	I_{L1}	$0V \leq V_I \leq V_{DD}$			±10	μA
Output Leak. Current	I_{LO}	$0V \leq V_O \leq V_{DD}$			±10	μA
VDD Supply Current	I_{DD1}	Operation Mode		20	40	mA
	I_{DD2}	HALT Mode		10	20	mA
	I_{DD3}	STOP Mode		15	50	μA

note1: $\overline{\text{RESET}}$, NMI, INT0 to INT6, X1, X2 pins

AC Characteristics (Ta = -40°C to +85°C, V_{DD} = +5.0V±10%, V_{SS}=0V)
Memory Read/Write Operation

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
X1 Input Cycle Time	t_{CY}		100			ns
ALE Width High	t_{LL}		70			ns
Address Setup to ALE↓	t_{AL}		50			ns
Address Hold After ALE	t_{LA}		20			ns
ALE to $\overline{RD}$ Delay Time	t_{LR}		70			ns
$\overline{RD}$ Width Low	t_{RR}		165			ns
$\overline{RD}$ to Data Input	t_{RD}				140	ns
Data Hold after $\overline{RD}$	t_{RDH}		0			ns
ALE to $\overline{WR}$ Delay Time	t_{LW}		70			ns
$\overline{WR}$ Width Low	t_{WW}		260			ns
$\overline{WR}$ to Data Output	t_{WD}				66	ns
Data Hold Time after $\overline{WR}$	t_{WDH}		20			ns
ALE to $\overline{WAIT}$ Delay Time	t_{LWT}				90	ns
$\overline{WAIT}$ Rise after X1↑	t_{XWT}		0			ns
$\overline{WAIT}$ Rise before X1↓	t_{WTX}		0			ns

External Clock Timing (Ta = -40°C to +85°C, VDD = +5.0V±10%, VSS = 0V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
X1 Input Width High	$t_{ØH}$		45		250	ns
X1 Input Width Low	$t_{ØL}$		45		250	ns
X1 Input Rise Time	tr		0		30	ns
X1 Input Fall Time	tf		0		30	ns

Other Operations (Ta = -40°C to +85°C, V_{DD} = +5.0V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
NMI Width High, Low	t_{NMIH} t_{NMIL}		10			μs
INTO-6 Width High, Low	t_{INTH} t_{INTL}		12			t_{CY}
$\overline{RESET}$ Width High, Low	t_{RSTH} t_{RSTL}		10			μs

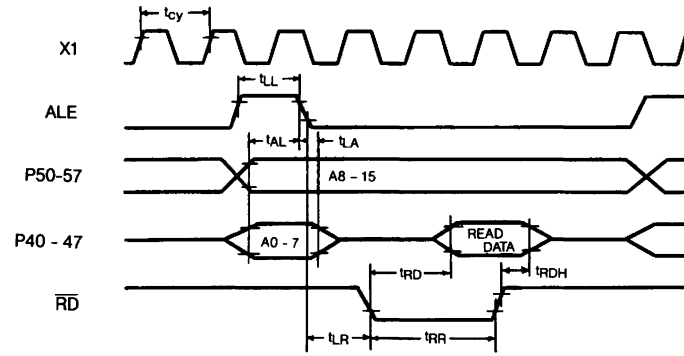
Serial Operation:

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
$\overline{SCK}$ Cycle Time	t_{CYK}	$\overline{SCK}$ Input	500			ns
		$\overline{SCK}$ Output	1.1			μs
$\overline{SCK}$ Width Low	t_{KKL}	$\overline{SCK}$ Input	200			ns
		$\overline{SCK}$ Output	500			ns
$\overline{SCK}$ Width High	t_{KKH}	$\overline{SCK}$ Input	200			ns
		$\overline{SCK}$ Output	500			ns
$\overline{SCK}$ to SIO Delay Time	t_{KTX}	C-MOS Output			300	ns
		O.D. RL = 1KΩ, CL = 100 pF			800	ns
SIO Setup Time To $\overline{SCK}$	t_{RXK}		80			ns
SIO Hold Time After $\overline{SCK}$	t_{KRX}		80			ns
Wake-Up Width High	t_{WKH}		8			t_{CY}
Wake-Up Width Low	t_{WKL}		8			t_{CY}
Command Setup to $\overline{SCK}\downarrow$	t_{CMK}		8			t_{CY}
Command Hold After $\overline{SCK}$	t_{KCM}		20			ns

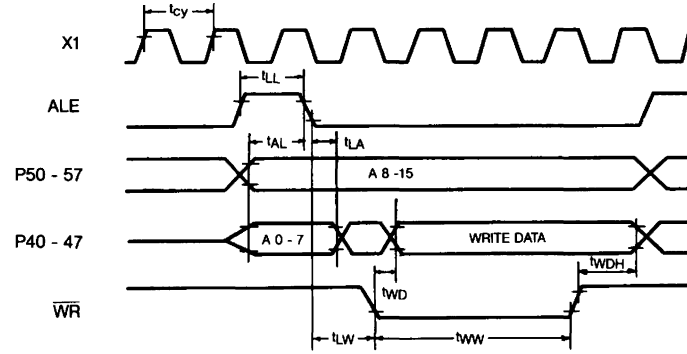
Comparator Characteristics (Ta = -40°C to +85°C, V_{DD} = 5.0V ± 10%)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Compare Accuracy	V_{ACOMP}				±100	mV
Compare Time	t_{COMP}		128			t_{CY}
PT Input Voltage	V_{PTI}		0		V_{DD}	V

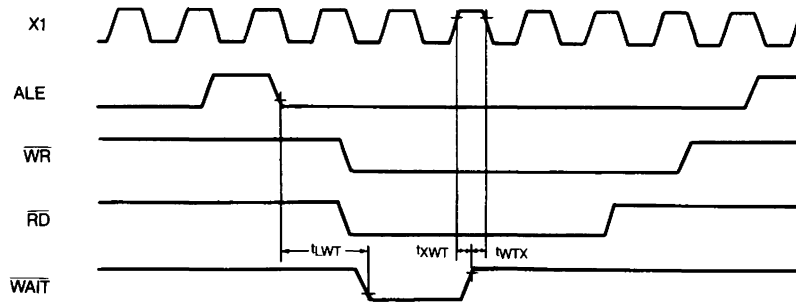
Read Timming



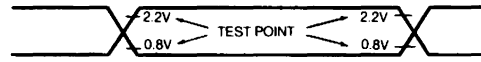
Write Timming



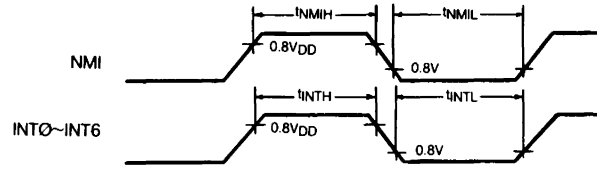
EXTERNAL WAIT TIMING



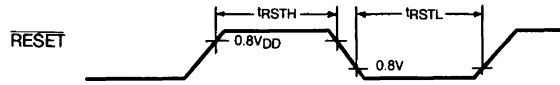
AC TIMING TEST POINTS



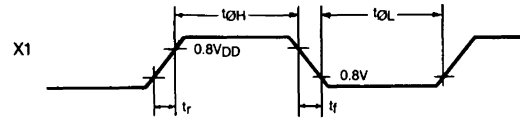
INTERRUPT TIMING



RESET TIMING

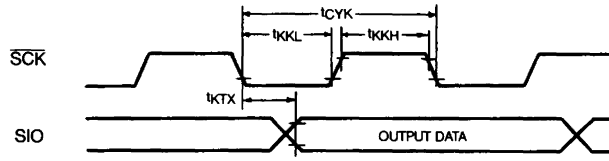


EXTERNAL CLOCK TIMING

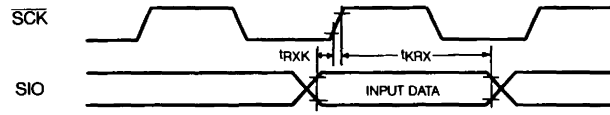


SERIAL BUS INTERFACE TIMING

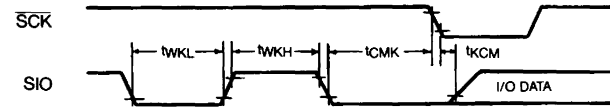
TRANSMIT



RECEIVE



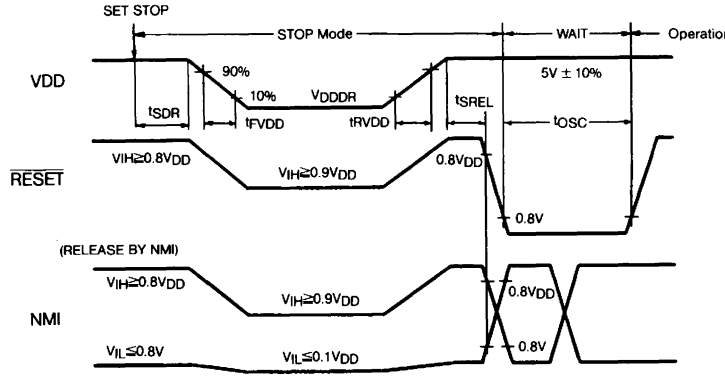
WAKE-UP



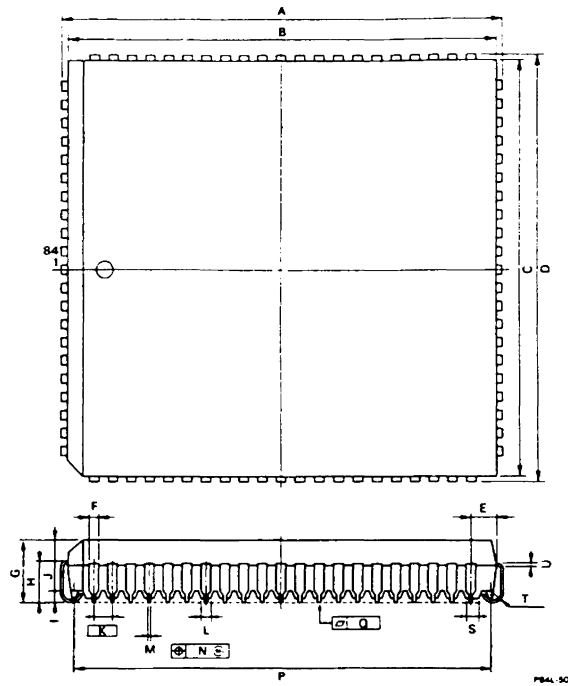
Memory Data Retention Characteristics (Ta = -40 to +85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Data retention Power supply voltage	V_{DDDR}		2.5			V
Data retention Power supply current	I_{DDDR}	VDDDR = 2.5V			15	μA
VDD rise, fall time	t_{RVDD} t_{FVDD}		200			μs
Set Data retention Time	t_{SDR}		0			ms
Set Release Signal Time	t_{SREL}		0			ms
OSC Stabilization Time	t_{OSC}		T.B.D.			ms
Input Low Voltage	V_{IL}	note1 Pins	0		$0.1V_{DD}$	V
Input High Voltage	V_{IH}	note1 Pins	$0.9V_{DD}$		V_{DD}	V

DATA RETENTION TIMING



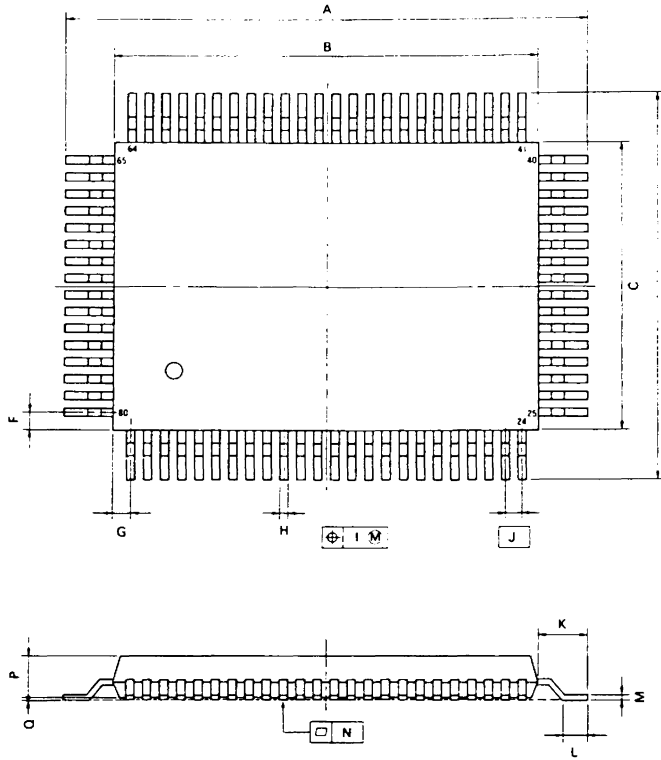
84PIN PLCC



NOTE
Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	$30.2^{\pm 0.2}$
B	29.28
C	29.28
D	$30.2^{\pm 0.2}$
E	$1.94^{\pm 0.15}$
F	0.6
G	$4.4^{\pm 0.2}$
H	$2.8^{\pm 0.2}$
I	0.7 MIN
J	3.6
K	1.27(T.P.)
L	0.7
M	$0.40^{\pm 0.10}$
N	0.12
P	$28.20^{\pm 0.20}$
Q	0.15
S	1.0
T	R0.8
U	$0.20^{+0.10}_{-0.05}$

80PIN PLASTIC FLAT PACKAGE



P80G-80-12

NOTE
Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	$24.7^{\pm 0.4}$
B	$20^{\pm 0.2}$
C	$14^{\pm 0.2}$
D	$18.7^{\pm 0.4}$
F	1.0
G	0.8
H	$0.35^{\pm 0.10}$
I	0.15
J	0.8(T.P.)
K	$2.35^{\pm 0.2}$
L	$1.2^{\pm 0.2}$
M	$0.15^{+0.10}_{-0.05}$
N	0.15
P	$2.05^{0.2}_{0.1}$
Q	$0.1^{\pm 0.1}$

CHAPTER 6

THE V-SERIES SINGLE CHIP

μPD70320/322

μPD70320/70322

EDN January 22, 1987

SINGLE-CHIP μCs

- *Software compatible with the 8086 and 8088*
- *Reduce power requirements*

Two CMOS-processed 1-chip microcomputers combine 8086/8088 compatibility with internal peripheral features. The μPD70320 and μPD70322, members of the manufacturer's V25 Series, provide serial and parallel I/O ports, a comparator, timers, a DMA controller, and 256 bytes of RAM. These peripheral functions previously required chips external to the 8086/8088 μP. Other features include a 16/32-bit temporary register/shifter, a 16-bit loop counter, a program counter and prefetch pointer, and a dual data bus that allows fetching two operands simultaneously. The μPD70322 differs from the μPD70320 in that it contains 16k bytes of mask-programmable ROM. In 80-pin plastic miniflat packages or 84-pin plastic LCCs, each device costs $25 (OEM qty).

NEC Electronics Inc, Literature-MS4580, 401 Ellis St, Mountain View, CA 94039. Phone (415) 965-6144. TWX 910-379-6985.

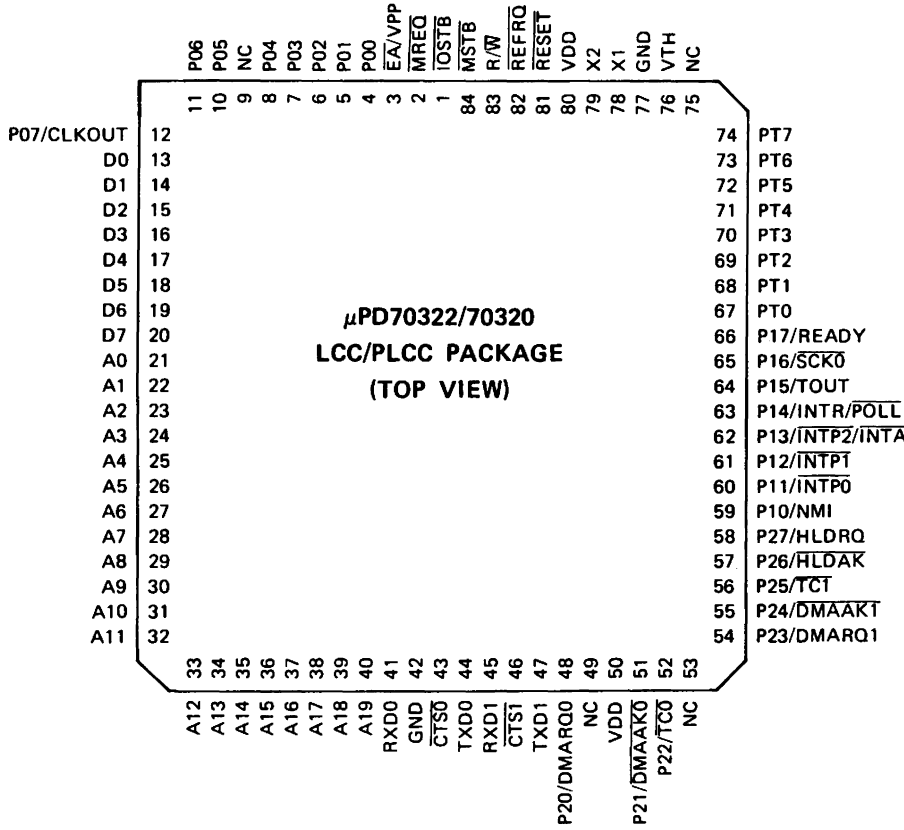
NEC MOS Integrated Circuit
μPD70322, μPD70320G/L One Chip Microcomputer

The μPD70322 (also known as V25™) is a one -chip microcomputer which features one-chip integration of 16-bit CPU, ROM, RAM, serial interface, timer, DMA controller, interrupt controller and others. The μPD70322 is software-compatible with the 8/16-bit microprocessor μPD70108/70116 (also known as V20™/V30™). The μPD70320 is a μPD70322 without ROM.

Features

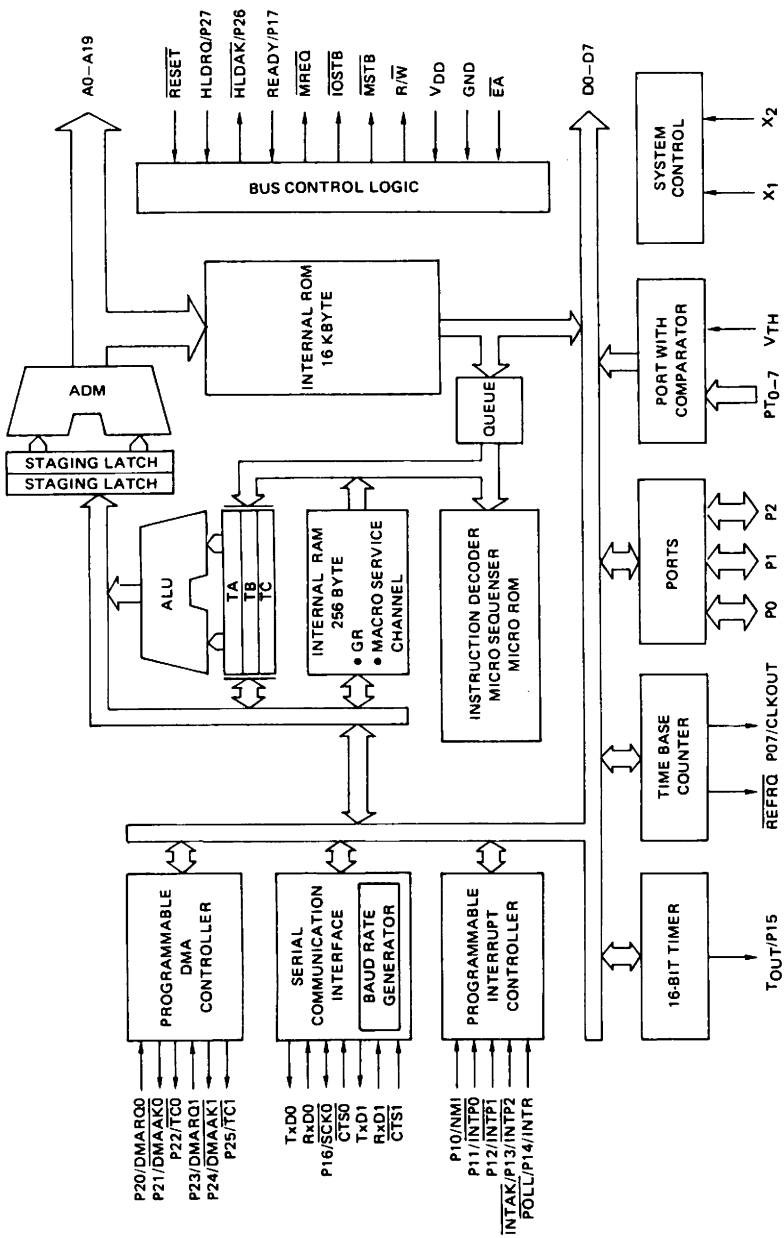
- internal 16-bit architecture, external 8-bit data bus.
- software-compatible with μPD70108/70116 (in native mode) (additional instructions available).
- minimum instruction cycle: 400 ns (10MHz, 5V).
- internal ROM: 16383W x 8 (μPD70322).
- internal RAM: 256W x 8.
- one-chip peripheral hardware memory mapping (special function register).
- input port (port T) with a comparator: 8 channels.
- I/O lines (input ports: 4; input/output ports: 20).
- serial interface (with a built-in dedicated baud rate generator): 2 ch; asynchronous mode, I/O interface mode.
- interrupt controller
  - programmable priority (8 levels)
  - vector interrupt function
  - register bank switching function
  - macro-service function
- DRAM, pseudo SRAM refresh function
- DMA controller
- input/output instructions, FPO instruction interrupt function.
- 16-bit timers: 2.
- time base counter.
- built-in clock generator circuit.
- programmable wait function.
- standby function (STOP/HALT).
- variable instruction cycles: 400ns, 800ns, 1.6μs (10MHz, 5V).
- CMOS.
- single power supply.
- 80-pin plastic flat package (μPD70322G, μPD70320G).
- 84-pin PLCC (Plastic Leaded Chip Carrier) μPD70322L, μPD70320L).

(2) 84-pin PLCC (top view)



Note: IC terminal should be fixed at the high level.

μPD70322/70320 block diagram



1. Pin functions

1.1 Port Pins

Pin Name	I/O	Port functions	Control functions
P00-P06	I/O	8-bit I/O port whose I/O can be	–
P07/CLKOUT	I/O/O	specified at bit level	system clock output
P10/NMI	I/I	nonmaskable interrupt request input and input port	–
P11/$\overline{\text{INTP0}}$		external interrupt request input	
P12/$\overline{\text{INTP1}}$		and input port	
P13/$\overline{\text{INTP2}}$/$\overline{\text{INTAK}}$	I/I/O		INT acknowledge signal output
P14/$\overline{\text{POLL}}$/INT	I/O/, I,I	input/output port whose I/O can be specified and POLL input	external interrupt request input
P15/TOUT	I/O, O	I/O port whose I/O can be	timer output
P16/$\overline{\text{SCK0}}$		specified at bit level	serial clock output
P17/READY	I/O, I		READY input
P20/DMARQ0	I/O, I	8-bit I/O port whose I/O can be	DMA request input (CH0)
P21/$\overline{\text{DMAAK0}}$	I/O, O	specified at bit level	DMA acknowledgement output (CH0)
P22/$\overline{\text{TC0}}$			DMA end output (CH1)
P23/DMARQ1	I/O, I		DMA request input (CH1)
P24/$\overline{\text{DMAAK1}}$	I/O, O		DMA acknowledgement output (CH1)
P25/$\overline{\text{TC1}}$			DMA end output (CH1)
P26/$\overline{\text{HLDAK}}$	I/O, O		HOLD acknowledgement output
P27/HLDRQ	I/O, I		HOLD input
PT0-PT7	I	input port with 8-bit comparator	–

1.2 Non-port Pins

Pin Name	I/O	Function
TXD0	output	serial data output
TXD1		
RXD0	input	serial data input
RXD1		
$\overline{CTS0}$	I/O	CTS input in asynchronous mode; receive clock input in I/O interface mode
$\overline{CTS1}$	input	CTS input
$\overline{REFRQ}$	output	DRAM refresh pulse output
V_{TH}	input	comparator reference voltage input
$\overline{RESET}$		reset signal input
$\overline{EA}$		Input for setting ROM-less mode
X1		connector for crystal system clock oscillation. External clock input is carried out by
X2		Internal connection. Should be fixed to the high level from the outside.
D0-D7	I/O	8-bit data bus
A0-A19	output	20-bit address output
$\overline{MREQ}$		output indicating start of memory bus cycle.
$\overline{MSTB}$		Strobe output for memory read or memory write.
R/$\overline{W}$		Read cycle and write cycle identification signal output
$\overline{IOSTB}$		I/O read or I/O write strobe output
V_{DD}		Positive power supply pin
GND		GND pin
I.C.		Internal connection. Should be fixed to the high level from the outside.

2. CPU

The μPD70322/70320 has a CPU which is software-compatible with the native-mode operation of the μPD70116/70108.

2.1 Registers

The μPD70322/70320 CPU has a general-purpose register set compatible with the μPD70116/70108. It also has special function registers for the control of on-chip peripheral hardware. These registers are all mapped in the memory space. The general-purpose register set also serves as built-in RAM, providing a maximum 8-bank register set in the internal RAM.

The addresses of the registers are relocatable in 4-kilobyte units. These addresses are specified using the internal data area base register (IDB) which is one of the special function registers (see 2.4.2).

2.1.1 Register Bank

The general purpose register set is mapped in the built-in RAM area. The general purpose register set is bank-formatted. Up to 8 banks of it can be installed. Each bank uses 32 bytes. Of these 8 banks, banks 0 and 1 can also be used for macro-service channel (see 2.4.2) and DMA service channel (see 5.3.3). They can also be accessed as data memory (see 2.4.4).

Normally the CPU runs programs by using register bank 7, switching automatically to other register banks through the use of interrupts. Return to the original register bank from a register bank switched by interrupt is carried out only by a return instruction – the RETRBI instruction (additional instruction from μPD70108/70116) from the interrupt.

Fig. 2-1 shows the configuration of the register bank. The (+00H)-(+01H) in the register bank become reserve areas when the register bank is used. The general purpose register set is mapped in the area of (+08H)-(+1FH) by an offset from a initial address from each register bank. The area (+02H)-(+07H) is not for general use as it is used for the switching of register banks.

Area (+02H) holds the value which the register bank loads to the PC during register bank switching, an offset of the interrupt processing routine starting address.

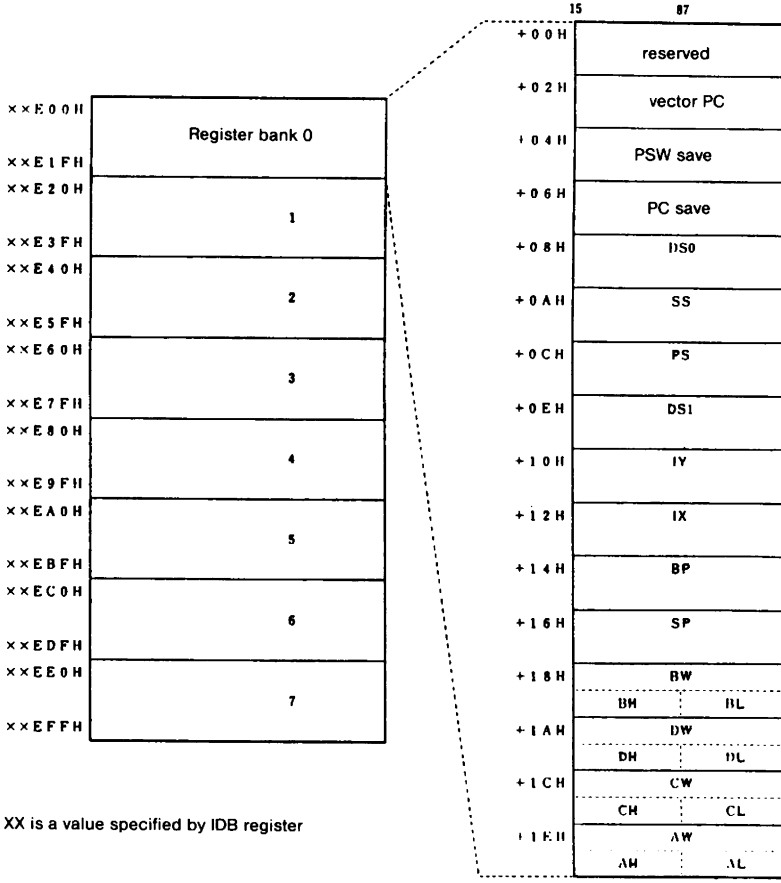
(+04H) is an area for saving the PSW when register banks are switched.

(+06H) is an area for saving the PC when register banks are switched.

After reset, register bank 7 is automatically selected.

Initialization of segment register (see 2.1.4) after reset is executed only in the register of register bank 7.

Fig. 2-1 Configuration of Register Bank



XX is a value specified by IDB register

(offset from starting address of each register bank)

2.1.2 General purpose registers (AW, BW, CW, DW)

Four 16-bit registers are used as general purpose registers; each register can be accessed as a 16-bit register as well as 8-bit registers by dividing it into higher and lower 8-bits (AH, AL, BH, BL, CH, CL, DH, DL).

These can be used as either 8-bit or 16-bit registers for a wide range of instructions including transfer, arithmetic, and logical operation instructions.

Each register is used as a default register for specific instruction processing as follows:

AW: word multiplication/division, word input/output, data conversion.

AL: byte multiplication/division, byte input/output, translation, BCD rotation, data conversion.

AH: byte multiplication/division.

BW: translation.

CW: loop control branching, repeat prefixing.

CL: shift instruction, rotation instruction, BCD operation.

DW: word multiplication/division, indirect addressing input/output.

These registers are mapped in the internal RAM. Their addresses are determined by adding the offset of each register to (IDB register* value* x 4096) + (0E00H) + (register bank number x 32). *See 2.4.2 for information on IDB register.

Fig. 2-1 Offset values for general purpose registers

Register	Offset value	Register	Offset value
AW	1EH	AL	1EH
		AH	1FH
BW	18H	BL	18H
		BH	19H
CW	1CH	CL	1CH
		CH	1DH
DW	1AH	DL	1AH
		DH	1BH

2.1.3 Pointers (SO, BP) and Index Registers (IX, IY)

Base pointers or index registers are used during memory access using based addressing (BP), indexed addressing (IX, IY), or based indexed addressing (BP, IX, IY). They are also used as pointers during stack operations (SP). Like the general purpose registers they are used for instructions for transfer, arithmetic operations, and logical operations; however, in this case they cannot be used as 8-bit registers. Each of the registers is used as a default register for specific processing as follows:

SP: stack operations

IX: block transfer, source side of BCD string operations

IY: block transfer, destination side of BCD string operations.

These registers are mapped in internal RAM. Their addresses are determined by adding the offset of each register to (IDB register value x 4096) + (0E00H) + (register bank number x 32). Offset values for each register are indicated in Figure 2-2. *See 2.4.2 for information on IDB register.

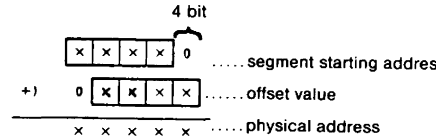
Fig. 2-2 Offset values for pointers and index registers

Register	Offset value
SP	16H
BP	14H
IX	12H
IY	10H

2.1.4 Segment registers (PS, SS, DS0, DS1)

The CPU divides the memory space into logical segments of 64 kilobytes each, the starting address of each segment is specified by the segment register and the offset part of the initial address is specified by another register or by the effective address.

The physical address therefore is created in the following way:



There are four types of segment registers; PS (Program Segment), SS (Stack Segment), DS0 (Data Segment 0), and DS1 (Data Segment 1). The respective segments are used in the following cases:

PS: Program fetch

SS: Stack operation instructions, addressing using the BP as the base register.

DS0: general variable access, source block data access for block transfer instructions.

DS1: destination block data access for block transfer instructions.

However, other segments can be used instead of DS0 by using a segment override prefix, or other segments instead of SS may be used in the same way in addressing with BP base register.

During reset, the PS of register 7 is initialized for FFFFH and SS, DS0, and DS1 can be initialized for 000H. These registers are mapped using internal RAM and their addresses are determined by adding the offset of each register to (IDB register* value x 4096) + (0E00H) + (register bank number x 32) as indicated in Figure 2-3.

*See 2.4.2 for explanation of IDB register.

Fig. 2-3 Offset values for segment registers

Register	Offset value
DS0	08H
DS1	0EH
SS	0AH
PS	0CH

2.1.5 Internal data area base register (IDB)

The IDB register is an 8-bit register for determining the address of the internal data area (2.4.1) which is the area for the special function register (See 2.4.3) for controlling the internal RAM (also used with the general purpose register) and the on-chip peripheral hardware. These registers can be referenced by using FFFFFH or their own value x 4096 + FFFH (See 2.4.2)

2.1.6 Special function registers

The μPD70320/70322 has a group of register with special functions for setting up and controlling on-chip peripheral hardware modes. These register groups are memory mapped in the special function register areas inside the internal data areas and Read/Write is carried out in the same way as with regular memory (see 2.4.3).

The additional BTCLR instructions (See 13.1) can be used only for these special function registers.

2.2 Program Counter (PC)

This is a 16-bit binary counter for holding the offset information on the memory addresses of a program to be executed by the CPU.

The program counter is incremented each time instruction bytes are fetched from the instruction queue. A new location is loaded while executing branch, call, return, and break instructions.

0000H is loaded while resetting. PS is initialized or FFFFH during reset so that the CPU starts execution from FFFF0H after reset.

2.3 PSW (Program Status Word)

PSW is comprised of six types of status flags and five types of control flags as well as user flags.

Status Flags

- V (Overflow)
- S (Sign)
- Z (Zero)
- AC (Auxiliary Carry)
- P (Parity)
- CY (Carry)

Control Flags

- RB0-RB2 (Register Bank 0-2)
- DIR (Direction)
- IE (Interrupt Enable)
- BRK (Break)
- IBRK (I/O Break)

User flags

- F0 (User Flag 0)
- F1 (User Flag 1)

The status flags are automatically set (1) and reset (0) according to a number of instruction executions (data value). The CY flags can be set directly, reset, and reserved by instructions.

The control flags are set and reset by instructions controlling the CPU operations. The IE and BRK flags are always reset whenever an interrupt processing is started.

The user flags can be set, reset, and tested by instructions and can be freely used by the user.

When the PSW is processed in byte or word units, it is executed in the following way.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	RB2	RB1	RB0	V	DIR	IE	BRK	S	Z	F1	AC	F0	P	$\overline{\text{IBRK}}$	CY

The least significant 8-bit PSW can be stored in the AH register and restored using MOV instructions. PSW can be saved separately and returned to stack using PUSH PSW and POP PSW instructions. The upper 4 bits of PSW are not affected by POP PSW instruction. The method of changing the upper 4 bits of the PSW is using the RETI or the RETRBI instruction. The others are automatically returned before the control flag is changed using interrupt generation. RESET input is used to initialize PSW at F002H using word image. The IBRK and RB0-RB2 flags are set (1) and the others are reset (0).

2.3.1 CY (Carry Flag)

(1) Binary addition and subtraction

When carrying out byte operations, the flag is set when there is a carry or a borrow from operation result bit 7; otherwise, it is reset.

When word operations are carried out, it is set when there is a carry or a borrow from operation result bit 15; otherwise, it is reset.

The flag is not changed by increment and decrement instructions.

(2) Logical operations

The flag is reset regardless of the results of the operations.

(3) Binary multiplication

The flag is reset when an unsigned byte operation gives 0 for AH; otherwise it is set. The flag is reset when a signed byte operation gives a sign expansion of AL for AH; otherwise it is set.

The flag is reset when an unsigned word operation gives 0 for DW; otherwise it is set. The flag is reset when a signed word operation gives a signed expansion of AW for DW; otherwise it is set.

With 8-bit immediate operations, it is reset when the product is within 16 bits and is set when it exceeds 16 bits.

(4) Binary division

Undefined

(5) Shift/Rotate

With shift and rotate which include CY, it is set if the bit shifted to CY is 1, and is reset if 0.

2.3.2 P (Parity Flag)

(1) Binary addition and subtraction, logical operation, shift.

This flag is set when the number of "1" bits in the lower 8 bits, representing the results of an operation, is even; it is reset when the number is odd.

When results are all 0, it is set.

(2) Binary Multiplication and Division undefinied

2.3.3 AC (Auxiliary Flag)

When working with byte operations, the flag is set when there is a carry from the lower 4 bits to the higher 4 bits or when there is a borrow from the higher 4 bits to the lower 4 bits; and is reset in all other cases.

In word operations, the same operations are carried out for the lower byte as for byte operations.

(2) Logical operations, binary multiplication and division, shift/rotate undefined

2.3.4. Z (Zero Flag)

(1) Binary addition and substraction, logical operations, shift/rotate.

For byte operations, the flag is set if the resulting 8 bits are 0; it is reset for all other values. For word operations, it is set if the resulting 16 bits are 0; it is reset for all other values.

(2) Binary multiplication and division undefined

2.3.5 S (Sign Flag)

(1) Binary addition/subtraction, logical operations, shift/rotate.

For byte operations, it is set when the resulting bit 7 is 1, and reset when 0.

For word operations, it is set when resulting bit 15 is 1, and reset when 0.

(2) Binary multiplication and division

undefined

2.3.6 V (Overflow Flag)

(1) Binary addition and subtraction

For byte operations, it is set if the carries from bits 7 and 6 are different and reset if the same. For word operations, it is set if the carries from bits 15 and 14 are different and reset if the same.

(2) Binary multiplication

The flag is reset when an unsigned byte operation gives 0 for AH; otherwise it is set. The flag is reset when a signed byte operation gives a sign expansion of AL for AH; otherwise it is set.

The flag is reset when an unsigned word operation gives 0 for DW; otherwise it is set. The flag is reset when a signed word operation, gives a signed expansion of AW for DW; otherwise it is set.

With 8-bit immediate operations, it is reset when the product is within 16 bits and is set when it exceeds 16 bits.

(3) Binary division

Reset.

(4) Logical operation

Reset.

(5) Shift/Rotate

In the case of left 1 bit shift/rotate,

when CY = most significant bit, is reset

when CY = most significant bit, is set in the operational results.

In the case of right 1 bit shift/rotate,

when most significant bit = next least significant bit after most significant bit, is reset

when most significant bit = next least significant bit after most significant bit, is set.

Undefined in the case of multibit shift/rotate

2.3.7 IBRK (I/O Break Flag)

Controls the software interrupt generation during input/output instructions.

When the execution of an I/O instruction is attempted with IBRK = 0, a software interrupt is automatically generated (interrupt vector 20), enabling a software simulation of the I/O instruction.

When IBRK = 1, input/output instructions are executed in the normal manner and software interrupts do not take place.

2.3.8 BRK (Break Flag)

Only in a condition where it is saved to the stack as a part of PSW can it be set using memory operation instruction and is effective after setting when it is restored in the PSW.

If BRK flag is set, software interrupt (interrupt vector 1) automatically takes place when one instruction is executed making it possible to trace each instruction.

2.3.9 IE (Interrupt Enable Flag)

It is set by the EI instruction, to enable the interrupt; it is reset by the DI instruction to disable the interrupt.

2.3.10 DIR (Direction Flag)

It is set by the SET1 DIR instruction and reset by the CLR1 DIR instruction.

When the DIR flag is set, processing is executed from the higher address to the lower address in block transfer/input output group instructions; when it is reset, processing is executed from lower addresses to higher addresses.

2.3.11 RB0-RB2 (Register Bank 0-2 Flag)

The RB0-RB2 is used to specify currently used register banks from among the eight register banks installed in the internal RAM.

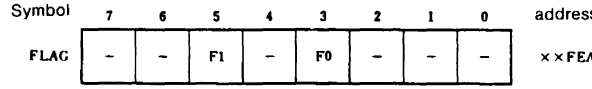
2.3.12 F0, F1 (User Flag 0, 1 Flag)

Can be freely used by users.

The setting and resetting of these flags can be executed by instructions for PSW and can be used to execute set, reset, and test by using special function register flags.

User flags F0, F1 operate in the following way when operated by flag register.

Fig. 2-2 Format for user flag register (FLAG)



2.4 Memory Space

The μPD70322/70320 has a 1-megabyte memory space. A memory map is indicated in Fig. 2-3. The space up to 00000H-003FF is used as a vector area. However, it can be used for other purposes if it is not used for vectors. XXE00H-XXFFFH (XX indicates IDB register value) is internal data area. The location of this area can be changed in units of 4 kilobytes. The 4 byte FFFFCH-FFFFFH is reserved. In FFFFFH, IDB register is assigned. Wait cycles can be inserted in the memory space, programmable in each 128 kilobytes segment.

The 1 megabyte physical address space is designated by the offset value for the segment initiator location which is indicated by a segment starting address which is indicated by segment register and other register or effective address.

Fig. 2-3 Memory Map

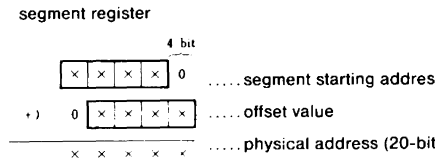
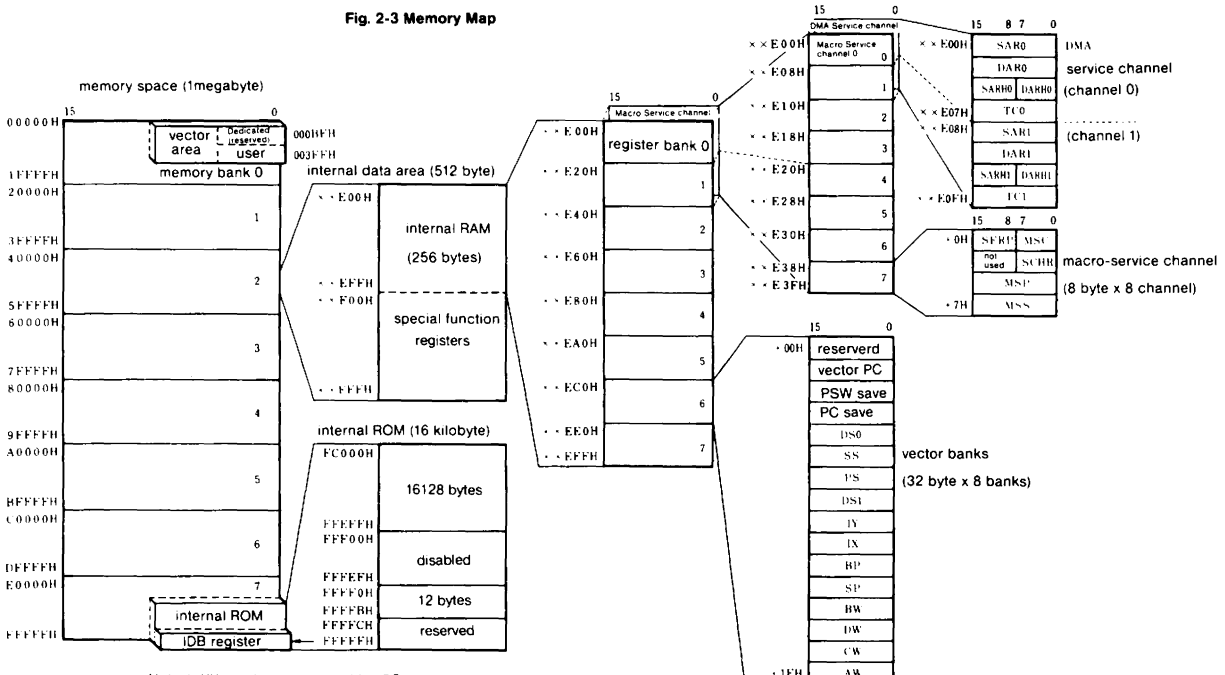


Fig. 2-3 Memory Map



Note 1. XX is value designated by IDB register

2. ±H is the offset value of the address, the value which adds the initiator adress of the register bank or the macro-service channel is the real address

3. Internal ROM is for the μPD70322 only.

4. Macro-servic channel is overlapped and assigned to register banks 0,1; DMA service is overlapped and assigned to macro-service channel 0,1

2.4.1 Internal Data Areas

The internal data areas are a 512 byte area containing internal RAM and special function register areas. 1-megabyte memory space can be divided in 4 kilobyte units. The internal data area base addresses are set up using the IDB register (internal data area base register). The higher 8 bits of the 20-bit internal data base address are set up using the IDB register and the lower 12 bits are fixed at E00H (beginning of area).

The internal data area is operated by memory operation instructions.

The internal data areas overlap the external memory space or the internal ROM areas (μPD70322 only).

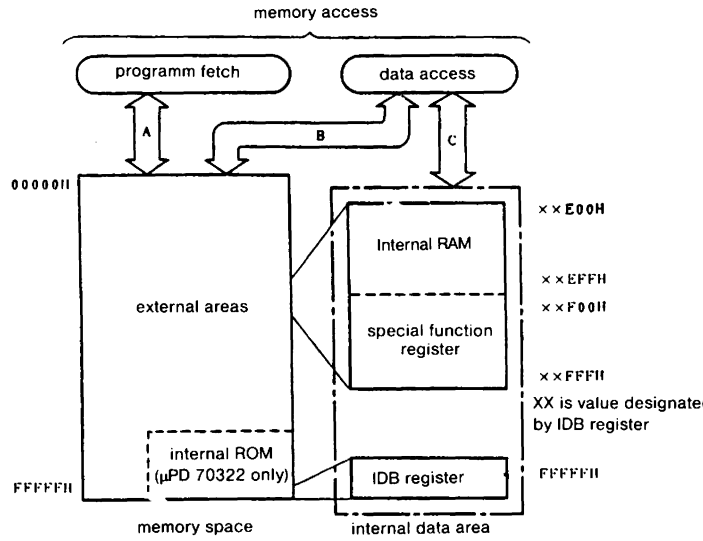
Memory access for all operations except program fetch can access internal data areas. It should be noted that internal data areas cannot be accessed by program fetch.

The least significant 256 byte of internal data areas (in XXE00H-XXEFFH, XX is the value specified by IDB register) is in the internal RAM area. In addition to the use as an ordinary RAM, the internal RAM has been assigned functionally register bank, macro-service channel and DMA service channel use. The internal RAM can be used in a way to disable access as ordinary RAM by resetting (0) bit 6 (RAMEN) of the processor control register (PRC) which is a special function register. In this case it still can be accessed as Register Banks.

The higher 256 byte of the internal areas (in XXF00H-XXFFFH, XX is the value specified by the IDB register) is a special function register area. The special function register has a register group that is mapped and has special functions assigned such as on-chip peripheral hardware mode registers and control registers.

The internal data areas are located in the FFE00H-FFFFFH location using RESET input, from the initialization of IDB register to FFH.

Fig. 2-4 Access Conditions for Memory Space



A. program fetch can access everything except the internal data areas.

B. data access outside of internal data areas or address data access corresponding to internal RAM areas during internal RAM access disable.

C. if it does not meet conditions in B, data access to the internal data areas takes precedence.

2.4.2 Internal Data Base Register (IDB)

This is a register for determining the physical address of internal data areas (areas for internal RAM and special function register) which can be located in 4 kilobyte steps. The higher 8-bit internal data area base address is designated by the IDB and the lower 12 bits are fixed at E00H (beginning address).

The IDB has two addresses assigned: XXFFFH inside the special function register (XX is the value of the IDB register itself) and the FFFFFH fixed address. The IDB can be modified or referenced by memory access to either of these two adresses with the same effect.

The IDB is set to FFH at reset time so that the internal data area base address is FFE00H.

2.4.3 Special Function Register Areas

A group of registers with special functions for on-chip peripheral hardware mode registers and control registers assigned are mapped to XXF00H-XXFFFH (XX is the value designated by the IDB register). The IDB register is specially assigned to both XXFFFH (XX is the value designated by IDB register) and FFFFFH fixed adresses. Program fetches cannot be executed from these areas.

The special function register is operated by memory access. The additional BTCLR instruction (additional to the μPD70108/70116) is a special instruction used exclusively for this area and applies to the bit in the areas no matter where the area is located in the memory space.

Charts 2-4 and 2-5 show a list of special function registers. Meanings of individual items in the chart are as follows:

- SYMBOL . . . . . symbol which indicates internally stored special function addresses coded in the instruction operand column.
- R/W . . . . . indicates whether a given function register is Read/Write-capable
  - R/W: Read/Write-capable
  - R: Read only
  - W: Write only
- Operational method . . . . . each register indicates whether 16-bit operations, 8-bit operations or 1-bit operations are possible.
- RESET condition . . . . . indicates condition of each register after RESET input XX in the higher 8 bits of an address is specified by IDB register.

The address part which is not mentioned is reserved. Contents during Read are undefined. Operations during Write have no significance.

Table 2-4 Special Function Registers

address	name of special function register	Symbol	R/W	operation method (bit)	RESET CONDITION
XX F00H	port 0	P0			undefined
XX F01H	port 0 mode register	PM0			FFH
XX F02H	port 0 mode control register	PMC0			00H
XX F08H	port 1	P1			undefined
XX F09H	port 1 mode register	PM1	R/W	8/1	FFH
XX F0AH	port 1 mode control register	PMC1			00H
XX F10H	port 2	P2			undefined
XX F11H	port 2 mode register	PM2			FFH
XX F12H	port 2 mode control register	PMC2			00H
XX F38H	port T	PT	R	8	undefined
XX F3BH	port T mode register	PMT	R/W	8/1	00H
XX F40H	external interrupt mode register	INTM			00H
XX F44H	external interrupt macro-service control register 0	EMS0			
XX F45H	external interrupt macro-service control register 1	EMS1			undefined
XX F46H	external interrupt macro-service control register 2	EMS2	R/W	8/1	
XX F4CH	external interrupt request control register 0	EXIC0			
XX F4DH	external interrupt request control register 1	EXIC1			47H
XX F4EH	external interrupt request control register 2	EXCI2			
XX F60H	receive buffer register 0	RxB0	R	8	undefined
XX F62H	transmit buffer register 0	TxB0	W		
XX F65H	serial receive macro-service control register 0	SRMS0			undefined
XX F66H	serial trasmit macro-service control register 0	STMS0			
XX F68H	serial mode register 0	SCM0	R/W	8/1	
XX F69H	serial control register 0	SCC0			00H
XX F6AH	baud rate generator register 0	BRG0			
XX F6BH	serial error register 0	SCE0	R	8	00H
XX F6CH	serial error interrupt request control register 0	SEIC0			
XX F6DH	serial receive interrupt request control register 0	SRIC0	R/W	8/1	47H
XX F6EH	serial transmit interrupt request control register 0	STIC0			

Table 2-5 Special Function Registers (cont.)

address	name of special function register	Symbol	R/W	operation method (bit)	RESET CONDITION
XX F70H	receive buffer register 1	RxB1	R	8	undefined
XX F72H	transmit buffer register 1	TxB1	W		
XX F75H	serial receive macro-service control register 1	SRMS1	R/W	8/1	undefined
XX F76H	serial transmit macro-service control register 1	STMS1			undefined
XX F78H	serial mode register 1	SCMO1			00H
XX F79H	serial control register 1	SCC1			
XX F7AH	baud rate generator register 1	BRG1			
XX F7BH	serial error register 1	SCE1	R	8	00H
XX F7CH	serial error interrupt request control register 1	SEIC1	R/W	8/1	47H
XX F7DH	serial receive interrupt request control register 1	SRIC1			
XX F7EH	serial transmit interrupt request control register 1	STIC1			
XX F80H	timer register 0	TM0	R/W	16	undefined
XX F82H	modulo/timer register 0	MD0			
XX F88H	timer register 1	TM1			
XX F8AH	modulo/timer register 1	MD1			
XX F90H	timer control register 0	TMC0	R/W	8/1	00H
XX F91H	timer control register 1	TMC1			
XX F94H	timer unit macro-service control register 0	TMMS0	R/W	8/1	undefined
XX F95H	timer unit macro-service control register 1	TMMS1			
XX F96H	timer unit macro-service control register 2	TMMS2			
XX F9CH	timer unit interrupt request control register 0	TMIC0			47H
XX F9DH	timer unit interrupt request control register 1	TMIC1			
XX F9EH	timer unit interrupt request control register 2	TMIC2			
XX FA0H	DMA control register 0	DMAC0	R/W	8/1	undefined
XX FA1H	DMA mode register 0	DMAM0			00H
XX FA2H	DMA control register 1	DMAC1			undefined
XX FA3H	DMA mode register 1	DMAM1			00H
XX FACH	DMA interrupt request control register 0	DIC0			47H
XX FADH	DMA interrupt request control register 1	DIC1			
XX FE0H	standby control register	STBC	R/W	8/1	*undefined
XX FE1H	refresh mode register	RFM	R/W	8/1	FCH
XX FE8H	wait control register	WTC	R/W	16/8	FFFFH
XX FEAH	user flag register **	FLAG	R/W	8/1	00H
XX FEBH	processor control register	PRC	R/W	8/1	4EH
XX FECH	time base interrupt request control register	TBIC			00H
XX FFFH	internal data area base register	IDB			FFH

* If the standby control register (SB) is set once, it cannot be reset by instruction. It is cleared by power supply voltage.

** Bit operations exclusive of bit 3 and bit 5 of the user flag register (FLAG) are of no significance. Also, the content of user flag 0, 1 (F0, F1) of the flag register can also vary according to the F0, F1 operation of PSW (See 2.3.12)

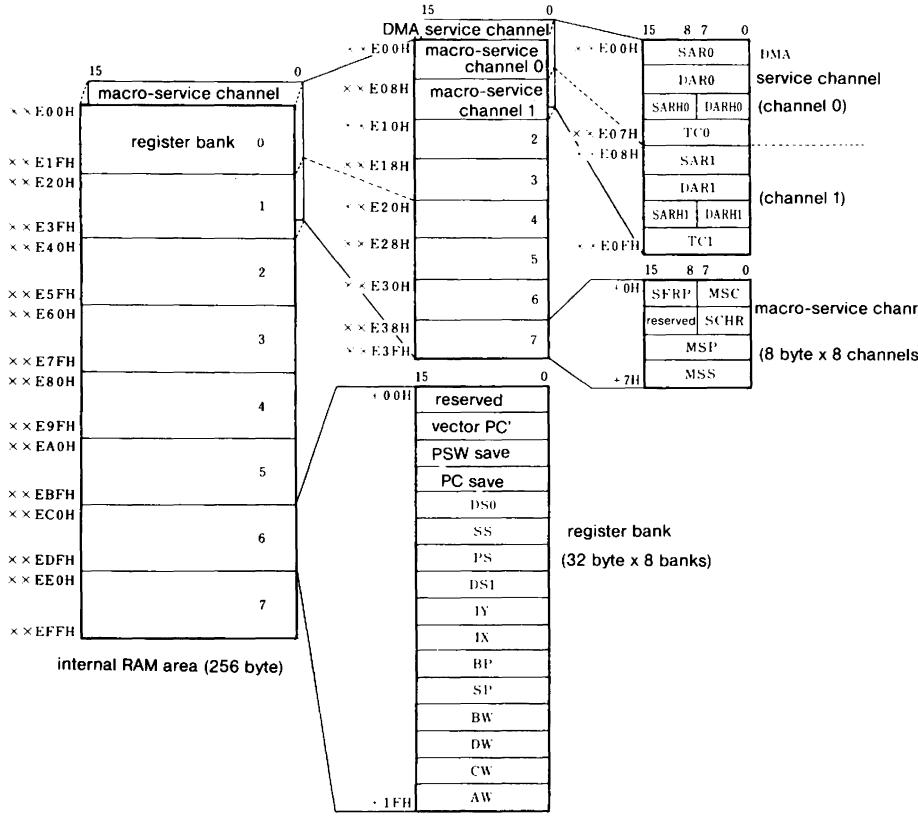
2.4.4 Internal RAM Areas

256 byte RAM is stored in XXE00H-XXEFFH (XX is the value designated by IDB)
The internal RAM is accessed by 16-bit units which enable high-speed processing.

8 register banks are assigned to the internal RAM. The macro-service channel and the DMA service are also overlapped and assigned.

The internal RAM makes it possible to disable memory access by resetting (0) bit 6 (RAMEN) of processor control register (PRC). It is also impossible to carry out program fetch from the internal RAM. When memory access has been disabled no access other than access as register is possible.

Fig. 2-5 Internal RAM Area Map



2.4.5 Vector Table Areas

In the 1 kilobyte area of 00000H-003FFH, the interrupt requests and the interrupt routine starting addresses corresponding to the break instructions are retained by the 256 vector portion (using 4 bytes for each vector)

vector 0 (00000H) : divide error
vector 1 (00004H) : single step
vector 2 (00008H) : NMI input
vector 3 (0000CH) : BRK 3 instruction
vector 4 (00010H) : BRKV instruction
vector 5 (00014H) : CHKIND instruction
vector 6 (00018H) : reserved
vector 7 (0001CH) : FPO instruction
vector 8 (00020H) : reserved
vector 19 (0004CH) : reserved
vector 20 (00050H) : input/output instruction
vector 21 (00054H) : reserved
vector 27 (0006CH) : reserved
vector 28 (00070H) : INTSER0
vector 29 (00074H) : INTSR0
vector 30 (00078H) : INTST0
vector 31 (0007CH) : reserved
vector 32 (00080H) : INTSER1
vector 33 (00084H) : INTSR1
vector 34 (00088H) : INTST1
vector 35 (0008CH) : reserved
vector 36 (00090H) : INTD0
vector 37 (00094H) : INTD1
vector 38 (00098H) : reserved
vector 39 (0009CH) : reserved
vector 40 (000A0H) : INTP0
vector 41 (000A4H) : INTP1
vector 42 (000A8H) : INTP2
vector 43 (000ACH) : reserved
vector 44 (000B0H) : INTTUOI
vector 45 (000B4H) : INTTU1
vector 46 (000B8H) : INTTU2
vector 47 (000BCH) : INTTB
vector 48 (000C0H) : user area
vector 255 (003FCH) : BRK imm8 instruction / INT input

In vectors 0-47, the interrupt vectors are designated (part of reserved area) and are not available for general use.

In vectors 48-255, they are for general use and can be used with 2 byte break instructions and the INT input. In the unused portions, they can be available for uses other than vectors.

The vectors are comprised of 4 bytes and the higher 2 bytes are loaded to the program segment PS while the lower 2 bytes are loaded to the program counter PC.

Example Vector 0

000H	001H
002H	003H

PC · (000H. 001H)

PS· (002H. 003H)

2.4.6 External Memory Areas

The μPD70322 can expand the external memory (ROM, RAM, and others) to the 00000H-FBFFFH areas.

The μPD70320 connects external memory (ROM, RAM, and others) to the 00000H-FFFFEH areas. However, the FFF00H-FFFEFH and the FFFFCH-FFFFEH areas are reserved.

The external memory is accessed by using address bus (A0-A19), data bus (D0-D7), and the $\overline{MREQ}$, $\overline{MSTB}$, and R/$\overline{W}$ signals. It also provides a refresh pulse output terminal (REFRQ) for pseudo-static memory refresh use. A pseudo-static memory can easily be connected, due to a function for automatic outputting of refresh address for dynamic memory refresh use; also the dynamic memory may be easily connected. It is also possible to insert wait cycles during the memory cycles in 128 kilobyte steps using software (See 4.1).

2.4.7 Internal ROM Areas

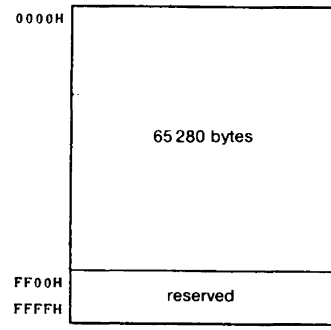
The μPD70322 has an internal mask ROM in the FC000H-FFFFFH areas. However, the FFF00H-FFFEFH area is used for testing internally and is not available for general use. The 4 byte FFFFCH-FFFFH are reserved. As a result, total 16140bytes can be utilized as a ROM area.

The internal ROM has an exclusive bus between the instruction queue so that the external memory space can carry out prefetch separately and rapidly which makes possible rapid instruction execution (Prefetch is possible with one clock, while external memories require a minimum of two clocks).

2.5 I/O Space

The μPD70322/70320 has a 64 kilobyte I/O space in addition to a 1 megabyte memory space. Fig. 2-6 shows a map of I/O space. The I/O space is accessed by using address bus (A0-A15), data bus (D0-D7) and $\overline{IOSTB}$, R/$\overline{W}$, $\overline{DMAAK0}$, and $\overline{DMAAK1}$ signals. 0 is output from the unused address bus's higher 4 bit (A16-A19). Insertion of wait cycles in the I/O cycle is software-specified.

Fig. 2-6 I/O Map (64 kilobyte)



3. INTERRUPTS

3.1 Interrupt Controller

The μPD70322/70320 has a high performance interrupt controller which controls multiprocessing of interrupts arising from 17 possible sources. The 17 interrupt sources in this interrupt controller are divided into a group of five external and 12 internal sources for control which carry out programmable multiprocessing control in groups. It is also possible to select from three types of response methods according to the characteristics of the interrupt sources: vector interrupt function, register bank switching function, and macro-service function.

External interrupts can be easily expanded by connecting the interrupt controllers like the μPD71059 and others.

Instructions of the interrupt controller are defined by the interrupt control register which is provided for each interrupt source and by the macro-service control register.

EI and DI instructions are for all the interrupts, RETI and RETRBI instructions are for return from interrupt, and FINT instruction is used to indicate that interrupt processing for interrupt controller is completed.

3.2 Interrupt Sources

The μPD70322/70320 has 5 external and 12 internal sources. The 17 interrupt sources are divided into eight groups and are managed by the interrupt controller. The configuration inside this group is fixed by hardware. For the 8 groups of interrupts priority from 0-7 (0 being the highest), excluding NMI and INTR, and 5 groups of interrupts except INTTB can be arbitrarily set using software. The function supported by the interrupt controller differs according to interrupt source.

Interrupt sources are listed in Table 3-1.

Table 3-1 Interrupt Sources

Interrupt Source	Internal/ External	vector	macro-service	bank-switching	priority			multi-processing control
					register	between groups	inside group	
NMI (Non Maskable Interrupt)	E	2	none	none	no	0	–	no
INTR (INTerrupt Request)	E	external input	none	none	no	7	–	no
INTTU0 (INTerrupt from Timer Unit0)	I	44	yes	yes	yes	1	1	yes
INTTU1 (INTerrupt from Timer Unit1)		45					2	
INTTU2 (INTerrupt from Timer Unit2)		46					3	
INTD0 (INTerrupt from DMA channel0)	I	36	no	yes	yes	2	1	yes
INTD1 (INTerrupt from DMA channel1)		37					2	
INTP0 (INTerrupt from Peripheral 0)	E	40	yes	yes	yes	3	1	yes
INTP1 (INTerrupt from Peripheral 1)		41					2	
INTP2 (INTerrupt from Peripheral 2)		42					3	
INTSER0 (INTerrupt from Serial ERror of channel0)	I	28	no	yes	yes	4	1	yes
INTSR0 (INTerrupt from Serial Receiver of channel0)		29	yes				2	
INTST0 (INTerrupt from Serial Transmitter of channel0)		30	yes				3	
INTSER1 (INTerrupt from Serial ERror of channel1)	I	32	no	yes	yes	5	1	yes
INTSR1 (INTerrupt from Serial Receiver of channel1)		33	yes				2	
INTST1 (INTerrupt from Serial Transmitter of channel1)		34	yes				3	
INTTB (INTerrupt from Time Base counter)	I	47	no	no	no (fixed at 7)	6	–	yes

3.3 Interrupt Controller Functions

The interrupt controller regulates the priority among interrupts when interrupts with same priority occur simultaneously.

3.3.1 Multi-interrupt Priority Control

Multi-interrupt priority control is carried out in group units for interrupt excluding interrupt response using NMI and INTR, as well as macro-service.

Interrupt multiprocessing control is carried out in EI condition. As a result, when allowing multiprocessing it is necessary to change to EI condition during interrupt processing routine. In multiprocessing control, if interrupt requests with a higher priority than the interrupt being processed are received, the interrupt being processed is discontinued, and processing of interrupts with higher priority is carried out. If the priority is below the priority of the interrupt being processed, that interrupt is held. If, for the interrupt held the interrupt mask bit of the interrupt control register (provided for each interrupt source) is not set during the interrupt processing routine being executed and if the interrupt request flag is not reset, the interrupt being held will be accepted at the end of the current interrupt.

In interrupt response exclusive of NMI, INTR and software interrupt (incl. trap), it is necessary to execute the FINT instruction in order to indicate to the interrupt controller that the interrupt processing routine has been completed at the very last part of the interrupt processing routine. If this instruction is not executed, all succeeding interrupts will be received as having a priority not higher than the interrupt for which the FINT instruction has not been executed. The FINT is not necessary at the end of the NMI and INTR service routine. Interrupt response using NMI and INTR as well as macro-service functions do not contain multiprocessing control so that it can be received if it is in an enable mode (always for NMI).

The eight priority levels from 0 to 7 (0 has the highest priority) can be set up arbitrarily for each interrupt group. The priority simultaneously indicates the number of switching destination register banks when using the register bank switching function which will be described later. Priority is established by using the three bits PR0-2 in the interrupt control register which is provided for each maskable interrupt source. However, when setting this up, only the interrupt control registers of the interrupt sources which have the highest default priority inside the interrupt groups can be programmed, the others are ignored and use the default values inside the group.

3.3.2 Priority Control during Simultaneous Generation of Interrupts

NMI is the highest and INTR is the lowest of the priorities possible during simultaneous generation of interrupts. Priority exclusive of NMI and INTR is exactly the same as for the priority of multi-interrupts. Among the groups with the same priority, it complies with the priorities fixed by hardware (default priority). Even in an identical group, it complies in exactly the same way with the priority inside the group.

3.4 Interrupt Response Method

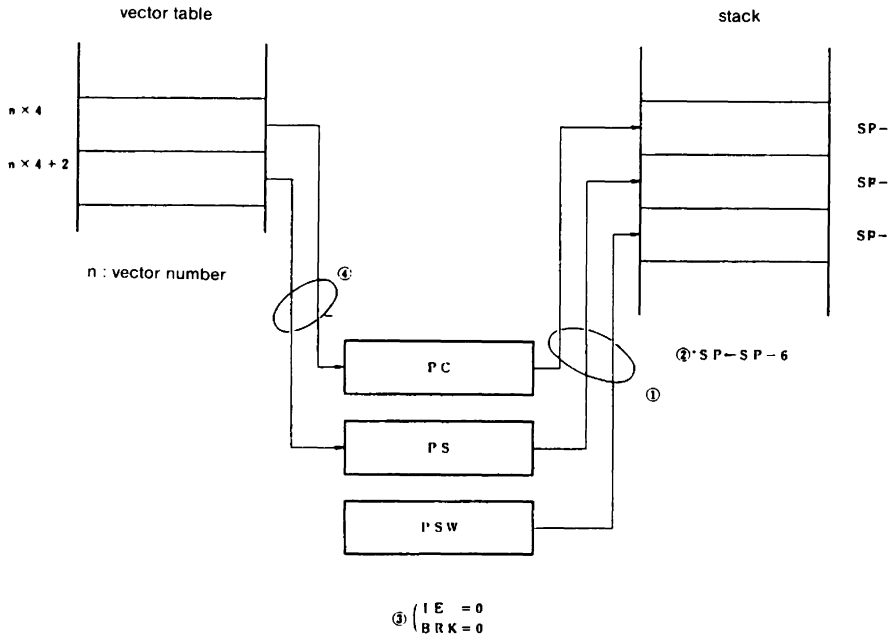
The μPD70322/70320 has three types of interrupt response method: vector interrupt function, bank switching function, and macro-service function. All of these functions can be selected to fit the purpose of the interrupt. The interrupt controller reacts to the interrupt requests according to the response method set up by the interrupt control register.

When receiving an interrupt using a vector interrupt function and a register bank switching function, the contents of PC, PS, and PSW are saved using the method applied to that functions. After PSW has been saved, each BRK flag is reset. As a result, single step interrupt and interrupt exclusive of interrupt response using NMI and macro-service are disabled (software interrupt exclusive of single step interrupt takes place) (See 3.9).

3.4.1 Vector Interrupt

When interrupt is received using vector interrupt, present contents of PSW as well as PC and PS contents are saved to the stack, a vector is selected from the vector table and is executed as an interrupt processing routine from the address indicated by the vector. All vectors are fixed except the INTR vector. When working with an INTR interrupt, an acknowledge cycle takes place and an interrupt vector is taken from the data bus (See 3.6 INTR). Interrupt vectors exclusive of INTR are indicated in Table 3-1. Return from interrupt is carried out by RETI instruction, however, when carrying out return from interrupts exclusive of NMI and INT, it is necessary to execute the FINT instruction. When carrying out return from interrupt, PC, PS, and PSW are returned from the stack.

Fig. 3-1 Operations for Interrupt Receive carried out in 1-4 order



3.4.2 Register Bank Switching Function

In the μPD70322/70320, the general purpose register sets are mapped in internal RAM and can contain a maximum of 8 register banks. These register banks are switched automatically during interrupt response and it is not necessary to carry out save processing to the stack of register groups which until now have been carried out using software and so it is now possible to respond to interrupt requests very fast.

When using register bank switching function, the ENCS bit of the interrupt control register which has been provided for each maskable interrupt source is set (1). One register bank can be designated for each interrupt group and it has the same number like the multiprocessing priority and is designated by PR0-2 of the interrupt control register.

The register bank switching sequence is carried out in the following way (Fig. 3-2)

(1) PSW contents are saved to a temporary register.
(2) register bank is switched.
(3) IE = 0, BRK = 0.
(4) the PC contents and the PSW in the temporary register are saved respectively to the save areas of the new register bank.
(5) the offset of the start address of the interrupt processing routine is loaded from the vector PC area to PC.

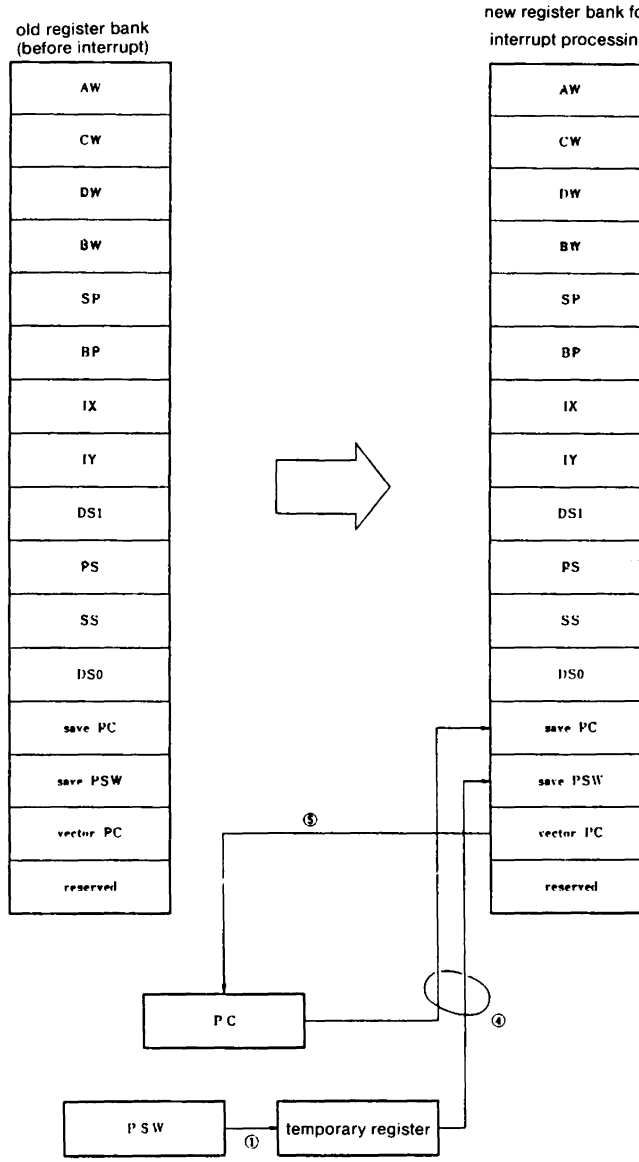
The register banks are thus switched and the interrupt processing routine is executed.

Return from register bank switching interrupt is carried out by executing RETRBI instruction after executing FINT instruction (the use of register bank switching function is limited to receiving of maskable interrupts). When RETRBI instruction is executed, PC and PSW are respectively reloaded from the save areas of the register banks as indicated in Fig. 3-3. (recovery of register banks is not carried out using RETI instruction so that return to main program can normally not be executed.

When using the register bank switching function, it is necessary to initialize beforehand the PS from the register bank of the switching destination, the vectors PC, SS, and SP. The other registers should be initialized as needed. However, care must be taken with PC when modifying during the interrupt processing routine.

The register bank switching function can be used only for one interrupt in each interrupt group with the same priority. (See 3.7 (1) IF).

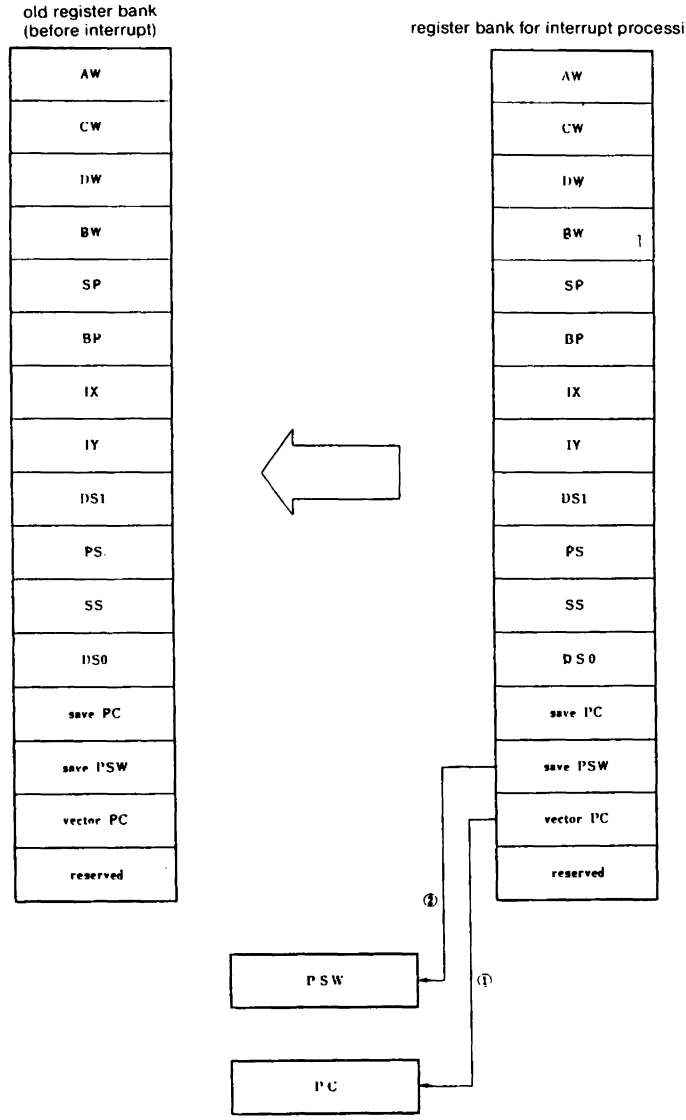
Fig. 3-2 Register bank switching sequence



(2) register bank switching

(3) IE-0, BRK=0

Fig. 3-3 Register bank return sequence



The macro-service function is a function which carries out data transfer between special function register areas and the memory space depending on the interrupt request. The function makes is possible to reduce the overhead (operations for save, initialization, and return of registers) on interrupt processing making it unnecessary to carry out simple processing of simple data transmission by interrupt processing using software. It is also unnecessary to execute program when processing with macro-service and it is now possible to process a portion of data with effective programming results which have traditionally been processed in 1 byte units using software. The macro-service function differs from other interrupt response modes in that the IMK bit (interrupt mask bit) of the interrupt control register which has been provided for every interrupt source is reset and macro service will be operated if the MS/INT bit (macro-service enable bit) is set whether it is in EI or in DI condition (See 3.7).

There are two types of operational mode for the macro-service function as follows:

(1) Normal mode

a pre-established number of data transfers are carried out, one byte or one word for every interrupt request occurrence.

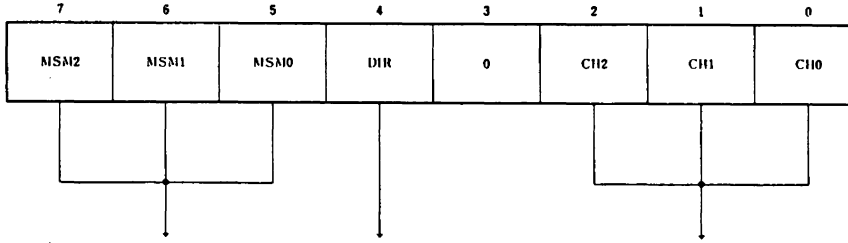
(2) Character search mode

One byte of data transfer is carried out for each interrupt request occurrence until a pre-established number of bytes has been transferred or the data coincide with pre-established 8-bit data.

The macro-service function is controlled by macro-service channels specified by macro-service control registers; a macro-service control register is provided for each interrupt source for which macro-service is possible.

The macro-service control register is configured as indicated in Fig. 3-4 and are within the special function register area.

Fig. 3-4 Format of Macro-Service Control Register



macro service mode specification

000: normal mode (8-bit transfer)

001: normal mode (16-bit transfer)

100: character search mode (8-bit transfer) use of other combinations is prohibited

specifies the direction of data transfer

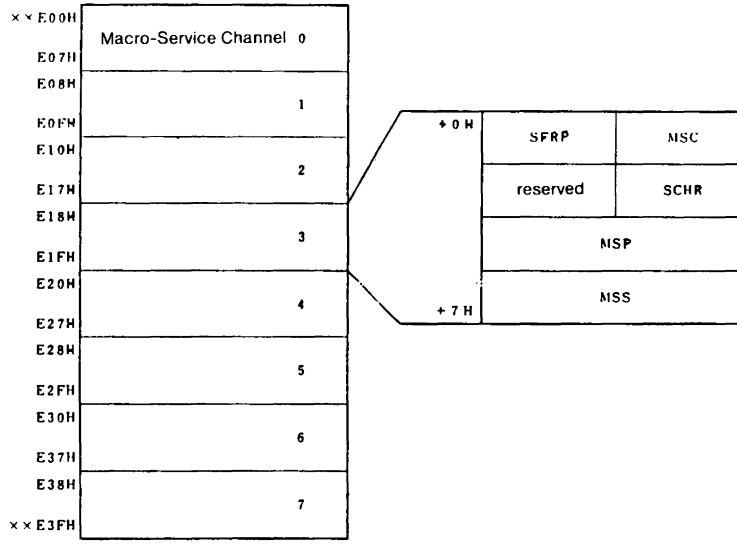
0: memory-special function register

1: special function register--memory

macro-service channel (0-7) specification

The macro-service channel is assigned to the XXE00H-E3FH (XX is value designated by IDB) of internal RAM, as shown in Figure 3-5. The macro-service channel is used to define the transfer destination, transfer source, number of transfers, search character for the macro-service data and one can use a maximum of eight channels.

Fig. 3-5 Configuration of Macro-Service Channel



MSC (+0H): Number of transfers carried out by macro-service.

SFRP (+1H): Offset value of special function register address, XXF00H+SFRP (XX is specified by IDB) is special function register address.

SCHR (+2H): 8-bit data compared during character search mode

MSP (+4H): Offset value of memory address which is object of macro service data transfer

MSS (+6H): value of memory address segment which is object of data transfer in macro-service. The memory address which is the object of data transfer is MSS x 16 +MSP.

The MSC of the macro-service channel is decremented (−1) after each data transfer (8-bit/16-bit), MSP is incremented (+1). Afterwards the interrupt request flags are cleared unless when MSC is 0 or when the transferred data is equal with the search data (only during character search mode), the interrupt request flags force an interrupt by not being cleared.

3.5 NMI (Non-Maskable Interrupt)

The NMI is the highest priority interrupt which cannot be disabled. This interrupt is edge-detected. The direction of the edge is selected by the special function register INTM register bit 0 the ESNMI bit. When ESNMI bit is 0 and when the completion edge is 1, interrupt is generated by the starting edge. This interrupt is capable of vector response only and the vector type is fixed at 2. This input is used in conjunction with terminal P10 and the level can be checked by reading P10. When NMI is received it causes the DI condition and disables other interrupts.

3.6 INTR (Interrupt)

INTR is a maskable interrupt and the interrupt is detected by level (active high). INTR does not receive multiprocessing control by using interrupt controller and if it is an interrupt enable condition (IE = 1) it can be received at any time. However, its priority when there is a simultaneous generation of interrupts is the lowest. The INTR is capable of vector response and the vector address is supplied from the data bus by the interrupt acknowledge cycle. The interrupt acknowledge cycle is defined via INTAK ouput. The INTR terminal is used in conjunction with P14 and POLL and is selected by bit 4 of the special function register port 1 mode control register (PMC 1). As a result, interrupt does not take place even in interrupt enable condition (IE = 1) when the INTR function is not selected. INTAK is used in conjunction with P13 and INTP2 and the function is selected using PMC1 bit 3.

The external interrupt input can be expanded to a maximum of 64 by connecting the μPD71059 interrupt controller. When the interrupt is received, it causes the interrupt disable condition (IE = 0)

3.7 Interrupts other than NMI and INTR

The interrupts other than NMI and INTR receives multiprocessing control using the interrupt controller. When the interrupt is accepted, the interrupt is automatically set in disable condition (IE = 0). However, when an interrupt with a priority higher than that of the interrupt being processed is generated, that interrupt can be accepted by setting it in an interrupt disable condition during interrupt processing routine. When an interrupt is generated with lower or with same priority, the interrupt is held over.

The 15 interrupt sources are divided into six priority groups. It is possible to set up arbitrarily 8 levels from 0 to 7 (0 being the highest) of priorities for each group. However, the priority for INTTB (Time Base Counter Interrupt) is fixed at level 7 by hardware. These priority levels also express the numbers of switching destination banks when using the bank switching function. The priorities are initialized at level 7 by resetting.

When interrupts are generated simultaneously, the interrupt in a group established with higher priority is accepted. When interrupts which have been set up on the same level are generated simultaneously, the one with the highest priority among the groups which are fixed by hardware and software and inside the same group with the highest priority inside that group which is fixed by hardware, is accepted.

Each interrupt source has a register for interrupt control used inside the special function registers. The bit configuration of this control register is indicated in Fig. 3-6.

Fig. 3-6 Format of Interrupt Request Control Register

7	6	5	4	3	2	1	0
IF	IMK	MS/INT	ENCS	0	PR2	PR1	PR0

(1) IF (Interrupt Flag)

Flag indicates that there is an interrupt request. It indicates that there is an interrupt request and indicates that it is not served. This flag is set by the generation of the interrupt requests and is reset by interrupt acceptance, by BTCLR instruction (an instruction additional to the μPD70108/70116), and by other instructions.

(2) IMK (Interrupt Mask)

A bit which sets up interrupt mask. 1 indicates that interrupt is masked, 0 indicates that mask has been released.

(3) MS/INT (Macro-Service/Interrupt)

This is a bit which specifies whether an interrupt response is processed by macro-service or by vector interrupt or register bank switching function; 1 is used for macro-service function, 0 for vector interrupt or register bank switching function.

(4) ENCS (Enable Context Switching)

This is a bit which specifies whether the register bank switching function is used or not; 1 indicates that register bank switching function is used; 0 indicates that vector interrupt is used.

(5) PRO-2 (Priority 0-2)

This are the bits which indicate the priority of the interrupt group with specifications from 0 through 7. This specification is possible only for the interrupt registers which have the highest priority within the group and specification by other interrupt control registers is invalid. (During Read, 7 is fixed).

These priorities indicate the number of the register banks for switching destination within the register bank switching function.

3.8 External Interrupt

There are five external interrupt sources. Among these INTR is detected by level and all others are detected by edge. For the interrupts which are detected by edge exclusive of INTR the respective effective edges are designated by the external interrupt mode register (INTM) of the special function registers.

Fig. 3-7 Format of External Interrupt Mode Register (INTM)

Symbol: INTM

7	6	5	4	3	2	1	0	Address
0	ES2	0	ES1	0	ES0	0	ESNMI	××F40H

ESNMI: Designation of effective edge for NMI input

ESO-2: Designation of effective edge of iNTPO--2 input

Effective edge: 0: falling edge

1: rising edge

3.9 Software-Activated Interrupts

The μPD70322/70320 has a total of eight types of interrupts using software (Table 3-2). Six types are compatible with interrupts for μPD70108/70116 software (there is no interrupt for emulation mode, however). The other two types of interrupts have a special function for the μPD70322/70320.

The vectors for these interrupts are predefined.

When conditions for generation of that interrupt are realized – exclusive of BRK interrupt (single step interrupt) – it is accepted as usual (it has a greater priority than hardware interrupt). However, the BRK flag interrupt is generated when BRK = 1 (with no distinction made for hardware or software) and when the interrupt is accepted the BRK flag is automatically reset so that it has a lower priority than the other interrupts (for both hardware and software) and the BRK flag interrupt is not generated during interrupt processing.

Table 3-2 Software Interrupt

interrupt source	vector	priority
DIVU divide error	0	1
DIV divide error		
CHKIND boundary overflow	5	
BRKV	4	
BRK 3	3	
BRK imm8	48-255	
BRK flag (single step)	1	2
input/output instruction (IBRK flag)	20	1
FPO instruction	7	

3.9.1 General Software Interrupts

The execution sequence for receiving of software interrupt exclusive of input/output instruction interrupt and FPO instruction interrupt is identical to that of the vector interrupt. In other words, the address information for the following instruction (PC) and PSW are saved to the stack, IE = BRK = 0, and vector contents are loaded to PS and PC.

Each software interrupt is described as follows:

(1) DIVU divide error, DIV divide error.

Always occurs when a quotient overflow occurs due to the execution of a division instruction.

(2) CHKIND boundary overflow.

Takes place when it is determined whether the index value has exceeded the boundary by executing instruction (CHKIND) which checks to see if the index value has exceeded the boundary of predefined arrays.

(3) BRKV

Occurs when V (overflow flag) is set during execution of BRKV instruction.

(4) BRK3

Occurs with execution of BRK3 instruction.

(5) BRK imm

Occurs with execution of BRK imm instruction.

(6) BRK flag (single step)

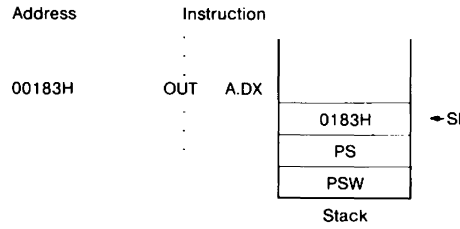
When BRK is set at 1, occurs every time one instruction is executed.

3.9.2 Input/Output Instruction Interrupt

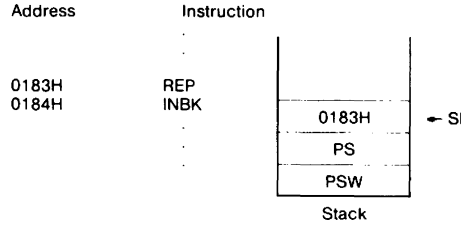
When IBRK = 0, interrupt takes place when an input/output instruction is attempted. The address information which is saved to stack when this interrupt is accepted differs from ordinary interrupt using software (see 3.91) in that it goes to the address where the input/output instructions are located. When the prefix is added to that input/output instruction, it goes to the address where the prefix is located. The other operations are the same as for ordinary interrupt using software. When returning from input/output instruction interrupt, it is necessary to adjust the PC value in the stack in order to return to normal. It is possible to use software to find out exactly which instructions have been executed to cause interrupt generation by making the address information which has been saved to stack the lead address. This function facilitates the transplantation of programs which have previously been used with the μPD70108/70116.

The contents of PSW are saved to stack immediately before interrupt has taken place and afterwards the flags are set automatically so that IE=BRK=0 and IBRK=1. IBRK is set to 1 so that the input/output instruction/during interrupt processing are executed as input/output instructions and it is automatically returned to the original condition (IBRK=0) by return from interrupt

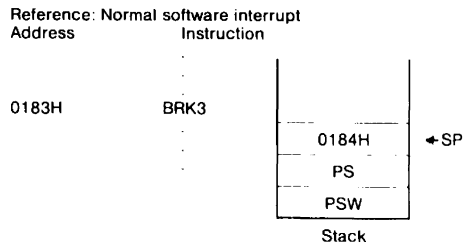
Example 1: I/O instruction without prefix



Example 2: I/O instruction with prefix



Reference: Normal software interrupt



3.9.3 FPO Instruction Interrupt

The external bus configuration of the μPD70322/70320 differs from that of the μPD70108/70116 in that the coprocessor for use in floating point operations can not be connected. As a result, when the use of the FPO instruction is attempted with this coprocessor, an interrupt is generated for the purpose of emulating the operation of the instruction. The PC value of this interrupt which is saved to stack becomes the starting address (see 3.9.2 for input/output instruction interrupt) (the prefix lead address when the prefix has been attached). As a result, the FPO instruction is decoded and software emulation is possible. It is necessary to adjust the PC value which has been saved to stack when returning from FPO instruction interrupt just as with the input/output instruction interrupt.

4. Bus Control

The μPD70322/70320 has bus control pins as shown in Table 4.
When using a multi-function pin, it is necessary to select the desired function by means of the port mode control register (PMCn).

Chart 4-1 Pin Functions for Bus Control

Name of Pin	Input/ Output	Function	Comments
A0–A19	Output	address bus	
D0-D8	Input/ Output	data bus	
R/W	Output	read/write identification	
MREQ	Output	indicates memory cycle	
MSTB	Output	strobe signal for memory read/memory write	
IOSTB	Output	strobe signal for I/O cycle	
REFRQ	Output	indicates memory refresh cycle	
HLDRQ	Input	bus hold request signal	for use with P27
HILDAK	Output	bus hold acknowledgement signal	use with P26
DMAAK0	Output	indicates DMA acknowledgement cycle	for use with P21
DMAAK1	Output	indicates DMA acknowledgement cycle	for use with P24
READY	Input	insert wait in external bus cycle	for use with P17
INTAK	Output	indicates interrupt acknowledgement cycle	for use with P13 and INTP2
POLL	Input	polling input	for use with P14 and INTR

4.1 Programmable Wait Function

The μPD70322/70320 insertion of wait state during bus cycle (exclusive of the memory refresh cycle) can be specified by software. It specifies a 1 megabyte memory space in 8 units of 128 kilobyte and I/O space using the wait control register (WTC) as shown in Fig. 4-1. However, memory space block 6 (C000H-DFFFH) and block 7 (E000H-FFFFFH) and are set up in the same way.

The wait state specification can easily be programmed independent for each block with one out of four possibilities using READY pin with 0,1, 2 and more cycles, as indicated in Chart 4-2. When using READY pin control, the READY pin is used in conjunction with P17 so that bit 7 of port 1 mode control register (PMC1) must be set at 1. When bit 7 of PMC1 is 0, READY condition or wait state always goes to 2 state. If control by READY terminal is selected 2 wait states are inserted regardless of the READY pin condition. The READY pin is level-triggered and in case of a low level wait states are inserted.

Accessing of internal ROM (μPD70322 only) and internal data areas is not influenced by the programmable wait functions. This set-up applies to access of everything in the external areas with the exception of refresh time.

The WTC register is initialized to FFFFH at reset time.

Fig. 4-1 Format of Wait control Register (WTC)

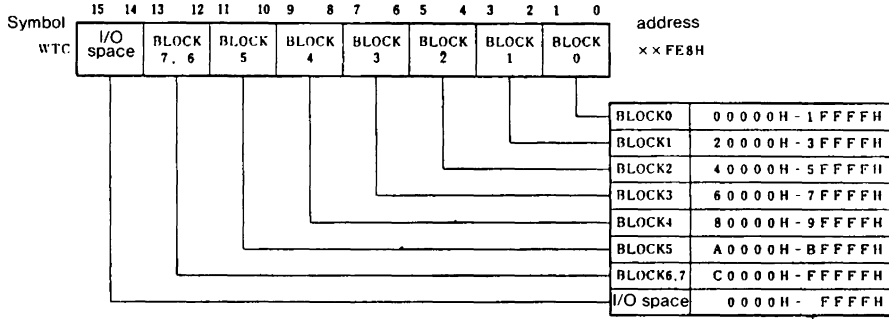


Table 4-2 Designation of wait State

BLOCKn/I/O space	Wait state
0 0	0 state
0 1	1 state
1 0	2 state
1 1	2 state + READY pin

4.2 Bus Hold Function

The μPD70322/70320 has a bus hold function. Input of external high level to HLDRQ terminal indicates that the external element wants to use the bus. When the μPD70322/70320 detects that the HLDRQ terminal is high level, it puts all of the A0-A19, D0-7, MREO, MSTB, and IOSTB outputs on high impedance, puts the HLDAK terminal on low level, and indicates that the external elements have been opened to the buses and switches to the hold mode. During the hold mode, the μPD70322/70320 stops execution of instructions and reception of prefetch data. Only the on-chip peripheral hardware which does not use a bus is operated. When the HLDRQ pin is checked and a low level is detected during hold mode, the HLDAK signal is placed on high level, this is an indication that the bus is not opened any more to the external elements, and execute is restarted after a one clock interval.

Even during HALT mode (one type of standby function: see 11.2), the bus hold requirement can be received and when the hold mode is released (if the HLDRQ signal is low level), it returns to HALT mode. The hold mode conditions is the same as normal mode.

During execution of one instruction following BUSLOCK prefix and during interrupt acknowledge operation, bus hold requests are not accepted.

The μPD70322/70320 can execute insertion of memory refresh cycle during hold mode and it is executed by setting refresh mode (RFM) register HLDRF (bit 6). The HLDAK signal is forced to a high level for each refresh timing and the refresh cycle is carried out after confirming that HLDRQ has gone to low level. Afterwards, if the HLDRQ signal reaches high level, it again shifts to the hold mode. If the HLDRQ signal remains at low level, the hold mode is released and instruction execution is restarted. Since HLDRQ pin is combined with P27 and HLDAK with P26, to use the bus hold function it is necessary to set bits 6 and 7 of the PORT 2 mode control register (PMC2) to 1.

4.3 Refresh Function

The μPD70322/70320 has a number of functions for refreshing of DRAM and the pseudo-SRAM. There are functions for insertion of refresh cycle on a regular basis for a series of bus cycles, for outputting of refresh address for the support of the DRAM and pseudo-SRAM power down self refresh mode, a function which generates a refresh cycle during HALT mode and a function for the insertion of wait state during refresh cycle.

4.3.1 Refresh Mode Register (RFM)

The RFM register is an 8-bit register which enables refresh function control. It can be accessed with 8/1-bit Read/Write operations using memory access.

The RFM register is initialized at FCH during reset.

The RFM register has the following bit functions and configuration:

address	7	6	5	4	3	2	1	0	symbol
RFM	RFLV	HLDRF	HLTRF	RFEN	RFW1	RFW0	RFT1	RFT0	××FE1H

RFT0 RFT1 are bits which specify refresh synchronization.

Refresh synchronization is selected from time base counter (see 7.1) output taps 3-6. Refresh cycle is generated at synchronous intervals as shown in Table 4-3.

Table 4-3 Refresh Synchronization

f_{CLK} = 5 MHZ (= ½ fx; fx = 10MHz)

RFT 1	RFT 0	refresh cycle
0	0	$2^4/f_{CLK}$ (3.2μs)
0	1	$2^5/f_{CLK}$ (6.4μs)
1	0	$2^6/f_{CLK}$ (12.8μs)
1	1	$2^7/f_{CLK}$ (25.6μs)

RFW0 RFW1 -- are bits which specify the number of wait states to be inserted during refresh cycle.

The number of wait states during refresh cycle is defined by designation of RFW0, 1 independently of previously descr bed programmable wait function (see 4.1) as shown in Table 4-4.

Table 4-4 Wait State during Refresh Cycle

RFW 1	RFW 0	wait state
0	0	0 state
0	1	1 state
1	0	2 state
1	1	2 state

RFEN is a bit which enables automatic insertion of refresh cycles

When it is 1, it permits automatic insertion of refresh cycles, when it is 0, it disables automatic insertion of refresh cycles, REFRQ pin output is controlled by RFLV bit contents (for further details, see description of RFLV bit).

HLTRF is a bit which enables automatic insertion of refresh cycles during HALT mode.

1 indicates enabling of automatic insertion, and 0 indicates disable. However, when RFEN bit=0, it is disabled regardles of the HLTRF bit contents.

HLDRF is a bit which enables automatic insertion of refresh cycles during hold mode.

1 indicates enable, 0 indicates disable. When in enable condition (1), it is forced to start HLDAK output at high level for each refresh timing, and inserts refresh cycle automatically.

RFLV is a bit which defines the output level for REFRQ signal.

Fig. 4-2 indicates the circuit configuration. Output is determined logically as in Chart 4-5.

The RFLV bit becomes master RFLV output at read time and is written for RFLV slave. Writing of master RFLV is carried out when refresh timing takes places.

Use of the RFLV bit enables support of power down self refresh mode for pseudo-SRAM.

Fig. 4-2 Control Circuitry Using RFLV Bit

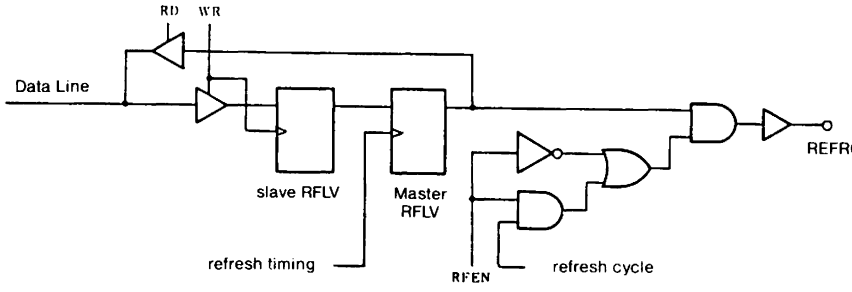


Table 4-5 Output Level for REFRQ Signal

RFLV	RFEN	**REFRQ condition**
0	0	0
0	1	0
1	0	1
1	1	**refresh pulse output**

Insertion of refresh cycle is carried out when RFEN bit goes to 1. At this time, MREQ, MSTB, and IOSTB go to high level, refresh address is output to A0-A8 and the high level is output to A9-A19, and refresh pulse is output from REFRQ pin.

Care must be taken when using the bit operation instructions as the RFLV bit does not go to read data up to the following refresh timing even with write.

4.4 Bus Usage Privileges

The priority for bus usage privileges for the μPD70322/70320 is as follows:

(1) Refresh cycle (see 4.3)

The refresh cycle will always take place if insertion of the refresh cycle is enabled. However, if insertion of refresh cycle at time of hold mode is enabled during hold mode, HLDAK signal is forced to high level and refresh cycle is carried out while waiting for HLDRQ signal to go to low level.

(2) Hold mode (see 4.2)

The system goes into the hold mode except during execution of one instruction following BUSLOCK prefix and during interrupt acknowledgement cycle.

(3) DMA cycle (see 5)

(4) Normal bus cycle

However, other requests are temporarily retained in the following cases:

- During execution of interrupt acknowledgement cycle and processing related to it.
- During execution of instructions with BUSLOCK prefix. Bus will not operate during stop mode. (See 11, Chart 11-2 for bus conditions).

4.5 Bus Timing

Figs. 4-3 through 4-10 show principal bus timings (exept for DMA)

Fig. 4-3 Memory Read Cycle

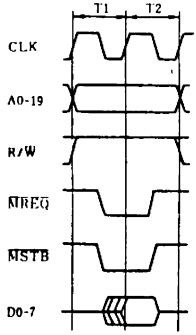


Fig. 4-4 Memory Write Cycle

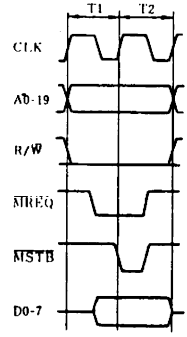


Fig. 4-5 I/O Read Cycle

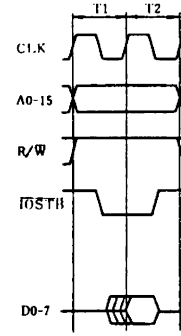


Fig. 4-6 I/O Write Cycle

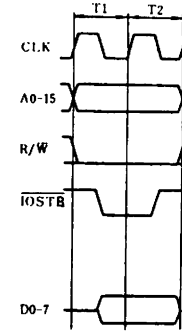


Fig. 4-7 Memory Read Cycle (During insertion of 1 wait state)

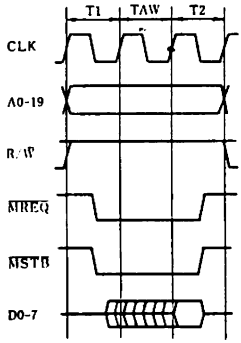


Fig. 4-8 Refresh Cycle (During 2 Wait State)

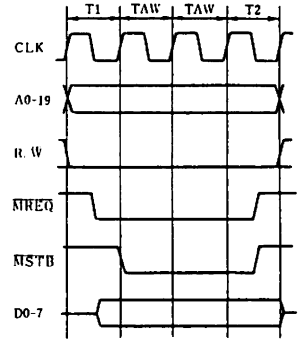


Fig. 4-9 Memory Write Cycle (During operation with READY terminal)

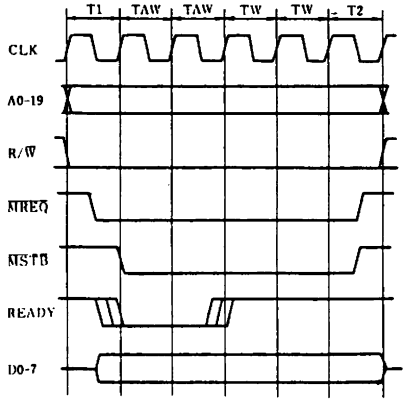


Fig. 4-10 Refresh Cycle (During insertion of 1 wait state)

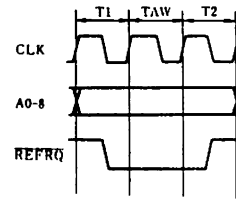


Fig. 4-11 Bus Hold Accept and Release Timing

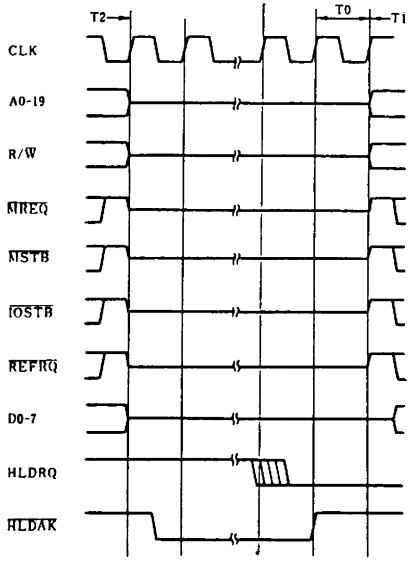


Fig. 4-12 Refresh Cycle during Hold Mode (0 number of wait states)

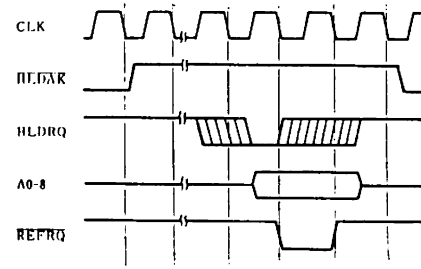
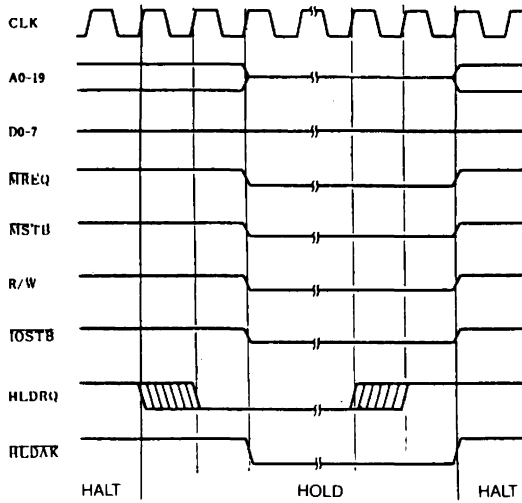


Fig. 4-13 HOLD Accept and Release during HALT Mode



5 DMA Controller

There is a built-in two-channel DMA controller which can directly specify 1 megabyte memory space in the μPD70322/70320.

5.1 Pin Functions

The DMA controller provides pins with the following functions. These pins can all be used in conjunction with the port; therefore it is necessary to put the bit of the corresponding port 2 mode control register (PMC2) during use to 1.

(1) DMARQ 0, DMARQ 1 (P20, P23).

Active high DMA request input pin.

(2) DMAAK 0, DMAAK 1 (P21, P24).

An active low DMA response signal pin. However, there is no output during memory-to-memory DMA transfer (burst mode, single step mode).

(3) TC 0, TC 1 (P22, P25).

An active low DMA completion signal output terminal. It is output when TC0 or TC1 of the DMA service channel are 0.

5.2 DMA Operation

Thera are four types of DMA transmit mode in the μPD70322/70320. Functions of each transfer mode are indicated in Table 5-1.

Table 5-1 Transfer Mode Functions

Mode	Transfer type	Function	DMA start	DMA Stop	Interrupts	During HALT	DMA request during DMA operation
single step	memory to memory	alternately repeats execution of 1 instruction and 1 DMA transfer for a specified number of times only using 1 DMA request	○ DMA rising edge ○ setting TDMA bit of DMA control register	software	receive all	carries out specified number of DMA transfers	DMA channel 1 is either retained or interrupted and then carries out channel 0 DMA
burst	memory to memory	carries out successively a specified number of DMA transfers using 1 DMA request	○ DMARY rising edge ○ setting of TDMA bit of DMA control register	NMI input only	can receive NMI only	carries out specified number of DMA transfers	New DMA'S are held until DMA transfer is finished
single transfer	memory to I/O	carries out one DMA transfer each time DMA requests are generated	○ DMARQ rising edge	software control	receive all	same as usual	DMA request is processed after current DMA transfer is completed
demand release	memory to I/O	carries out transfer during high level period of DMARQ pin	○ DMARQ high level	○ stopped at low level of DMARQ during DMA transfer ○ all others use software control	○ not accepted during DMA transfer ○ in all other cases, all interrupts accepted	same as usual	New DMAs are held until DMA transfer is finished

In memory-to-memory DMA transfer, DMAAK signal is not output. In memory-to-I/O DMA transfer, DMAAK signal is output for every 1 DMA cycle.

The programmable wait function (see 4.1) is effective even during DMA transfer. In memory-to-memory transfer the specified wait state is inserted at every transfer destination and transfer source. In memory-to-I/O transfer a wait state which is slow between memory and I/O is inserted so as to complete one transfer in one bus cycle.

The bus hold function and refresh function are effective even during DMA transfer and DMA transfer is interrupted by them.

All interrupts which were generated and could not be received during DMA transfer are reatained.

DMA transfer during HALT mode can be carried out if there are requests. When DMA transfer has ended, it returns to HALT mode. If DMA transfer end interrupt occurs when it returns to HALT mode, the HALT mode is released.

Channel 0 is given priority when DMA requests are generated at the same time.

When DMA transfer is ended (when a specific number of DMA transfers is executed), it can generate an interrupt.

5.3 DMA Control Registers

The DMA mode register and DMA control register help to program the specification of DMA transfer mode. The DMA service channels are mapped in internal RAM in order to specify transfer destination, transfer source and number of transfers. There are also registers for interrupt control and they are provided for each channel.

5.3.1 DMA Mode Registers (DMAM0, DMAM1)

These are bit registers which designate DMA transfer mode. The DMAMn register (n=0,1) can be accessed with 8/1-bit Read/Write operations by memory access.

Symbol	7	6	5	4	3	2	1	0	address
(channel 0) DMAM0	MD2	MD1	MD0	W	EDMA	TDMA	0	0	FFA1H
(channel 1) DMAM1									FFA3H

MD2, MD1, MD0 are bits which specify transfer mode

MD 2	MD 1	MD 0	Transfer Mode
0	0	0	single step mode
0	0	1	demand release mode (I/O--Memory)
0	1	0	demand release mode (Memory--I/O)
0	1	1	disable
1	0	0	burst mode
1	0	1	single transfer mode (I/O--Memory)
1	1	0	single transfer mode (Memory--I/O)
1	1	1	disable

W A bit which specifies whether transfer processing is to be carried out by byte or by word.

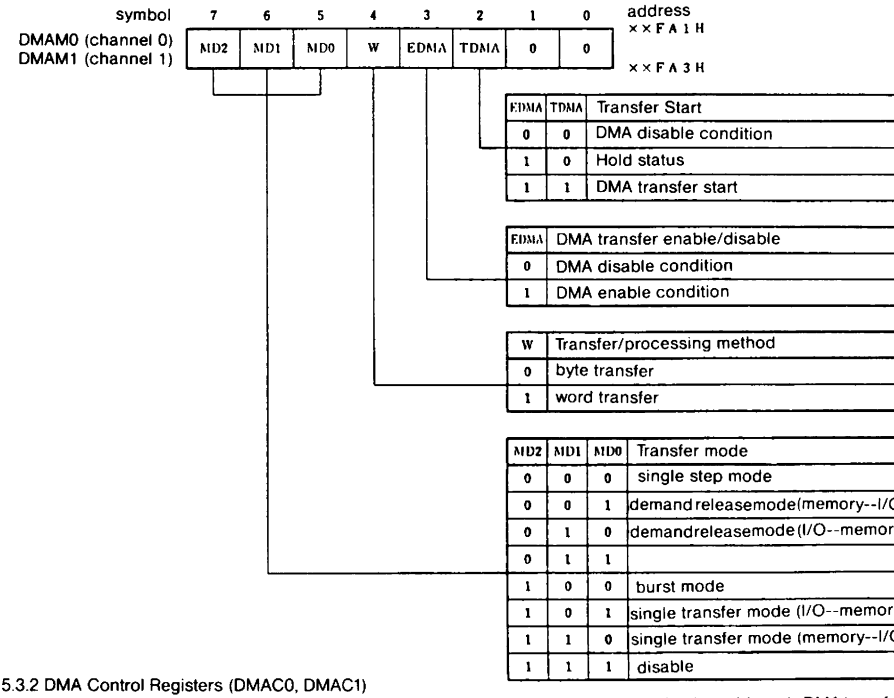
EDMA A bit which specifies enable or disable for DMA transfer.

1 indicates enable, 0 enable disable. This bit is automatically cleared (0) when the DMA service channel terminal counter (TC) is 0.

TDMA Transfer Start Bit

This is effective only with single step mode or burst mode. DMA is started up when 1 is written into this bit. (However, only when EDMA is set (1)). Read level for this bit is always 0. It is insignificant with demand release mode and single transfer mode.

Fig. 5-1 Format for DMA Mode Registers (DMAM0, DMAM1)



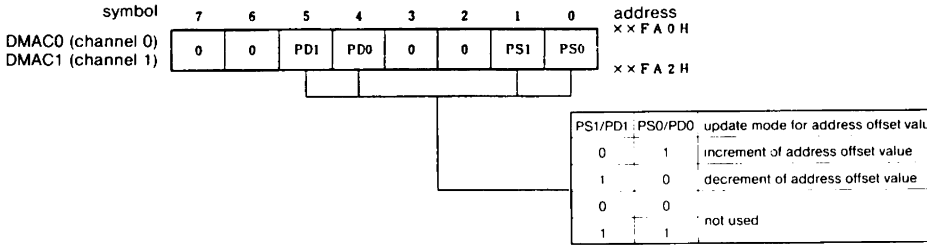
5.3.2 DMA Control Registers (DMAC0, DMAC1)

These are 8-bit registers which specify the influence on the source address and destination address in DMA transfer. The DMAC register (n=0,1) can be accessed with 8/1-bit Read/Write operations using memory access.

DMACn register contents are retained during RESET and are undefined.

As fig. 5-2 indicates, bit 1,0 (PS1, PS0) of DMACn register specifies the influence on the source side address offset value.

Fig. 5-2 Format of DMA Control Register (DMAC0, DMAC1)

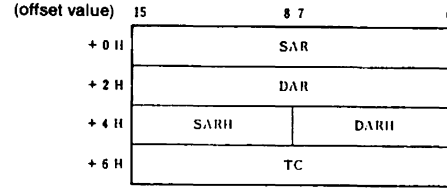


5.3.3 DMA Service Channel

This is used to specify transfer source, transfer destination, and number of transfers used in DMA transfer and it is mapped in internal RAM. The internal RAM addresses are assigned as follows: channel 0 to XXE00H-XXE07H and channel 1 to XXE08H-XXE0FH (XX is the value designated by IDB register). Care must be taken with these areas as they are assigned to the same areas as macro-service channel 0 and 1 as well as register bank 0.

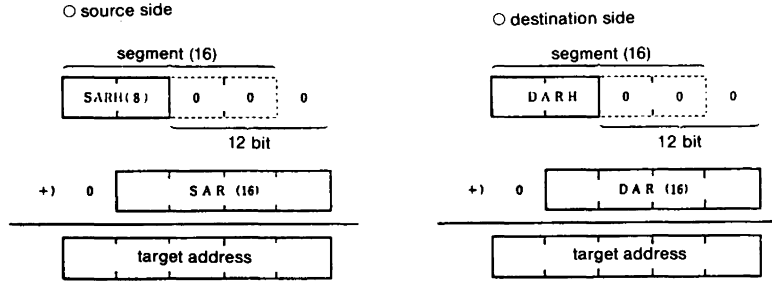
Designation of addresses for DMA source side and destination side is the same as the method for normal memory access and is specified by offset from segment and segment. However, only the higher 8 bits of the segments can be specified and the lower 8 bits are fixed to 0. Only this offset can be changed when changing the address using DMA transfer. As a result, a 64K-byte transfer is possible as far as any number of transfers goes, and when DMA transfer of data exceeds 61441 bytes (61441 times during byte transfer, 30720 times during word transfer), and care must be taken as there are cases in which it cannot be processed by a series of DMA transfers using addresses of transfer source and transfer destination. However, it is wise to be cautious even in cases in which data do not exceed 61441 bytes when segment and offset value are initialized. Fig. 5-3 shows configuration of DMA service channel; Fig. 5-4 shows method generation of DMA addresses.

Fig. 5-3 Format of DMA Service Channel



- SAR (+0H): specifies offset (least significant 16-bit of address of DMA transfer source side.
- DAR (+2H): specifies offset (least significant 16-bit) of address of DMA transfer destination side.
- DARH (+4H): specifies most significant 8-bit of segment value of DMA transfer destination side.
- SARH (+5H): specifies most significant 8-bit of segment value of DMA transfer source side address. However, the least significant 8-bit for the segment value is 0 fixed.
- TC (+6H): specifies number of DMA transfers.

Fig. 5-4 Method of DMA Address Generation



DMA service channel 0 is assigned to XXE00H and DMA service channel 1 is assigned to XXE08H (XX is value designated by IDB register).

The DMA service channel is automatically changed by DMA operations. TC value is decremented by 1 for every DMA transfer (byte data and word data are the same.).

Address offset value is changed in accordance with mode specified by DMA control register (DMACn): ±1 or unchanged for byte data, ±2 or unchanged for word data.

5.3.4 DMA Interrupt Request Control Registers (DIC0, DIC1).

These are 8-bit registers for control of interrupts generated by completion of a DMA transfer. Interrupt is generated when terminal counter (TC)=0.

The DICn (n=0,1) registers can be accessed with 8/1-bit Read/Write operations using memory access. The DICn register is initialized at 47H at reset time.

The macro-service functions are not supported in these interrupts. The DMA transfer completion interrupt of channel 0 (INTD0) and channel 1 (INTD1) form one group, the channel 0 taking a higher interrupt priority. INTD0 control is carried out by using the DIC0 register and the vector is 36. INTC1 control is carried out by DIC1 and the vector is 37 (see 2.4.5).

Fig. 5-5 Format of DMA Interrupt Request Registers (DIC0, DIC1).

(interrupt priority DF0>DF1)

symbol	7	6	5	4	3	2	1	0	address
DIC0	DF0	DMK0	0	ENCS	0	PR2	PR1	PR0	××FACH
DIC1	DF1	DMK1	0	ENCS	0	1	1	1	××FADH

(Note) The DIC1 register bit 2-0 is fixed at '1' using hardware. Bit 2-0 is a bit field (PR2-0) which specifies interrupt request priority by group and forms one group with the DIC0 register. The priority of the DIC1 register interrupt requests conforms to the setting of the PR2-0 bit of the DIC0 register.

The DF0/DF1 bit is an interrupt request flag for DMA transfer completion and the DMK0/DMK1 are masked bits for DMA transfer completion interrupt.
For description of other bit fields, see 3.7.

5.4 DMA Transfer Timing

Fig. 5-6 through 5-9 illustrate principal DMA transfer timing.

Fig. 5-6 Timing of burst mode (timing for 1 wait state insertion for transfer destination and no wait state insertion for transfer source when starting DMA using DMARQ signal when TC=1).

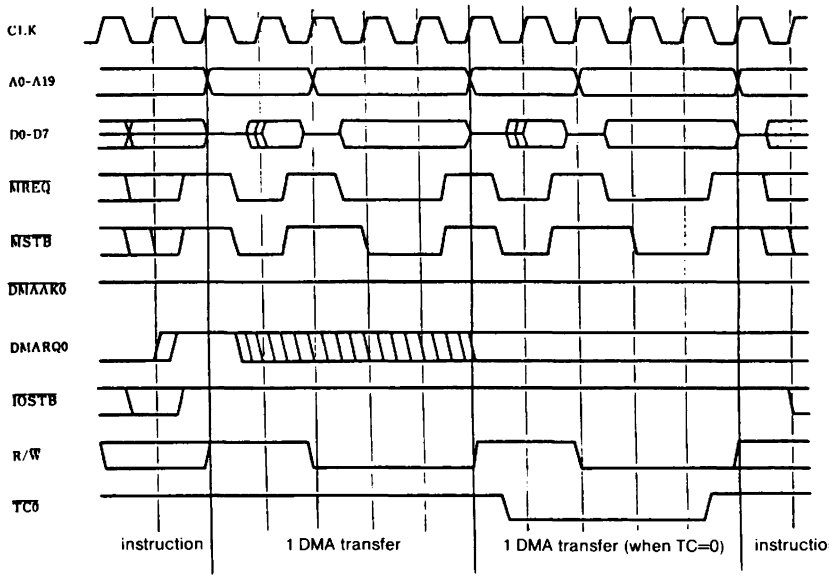


Fig. 5-7 Single Step Mode

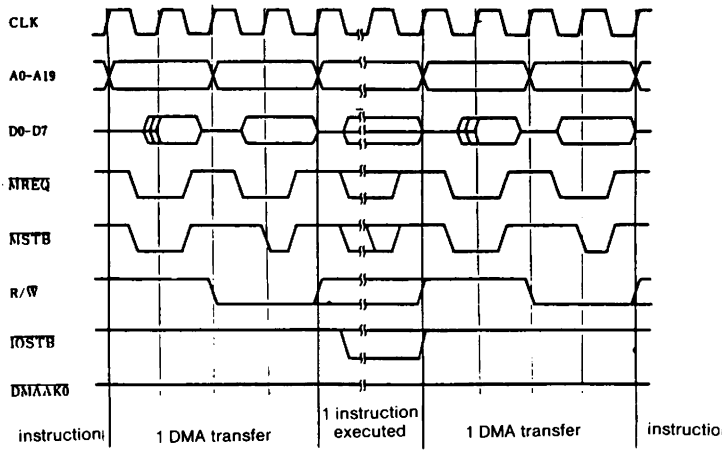


Fig. 5-8 Single transfer mode
(memory--I/O, no wait)

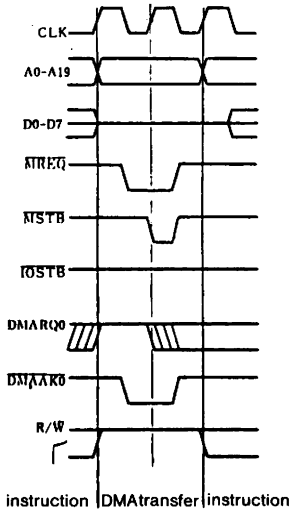


Fig. 5-9 Demand Release mode
(I/O--memory I/O; 1 wait, memory: no wait)

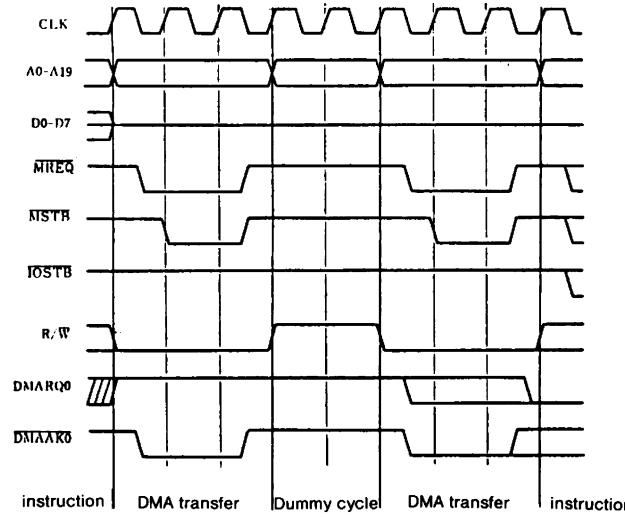
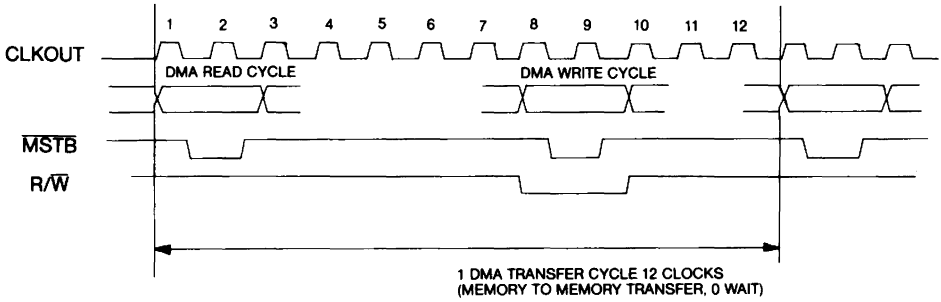


Fig. 5-10 Memory to Memory transfer mode



DMA TRANSFER CYCLE

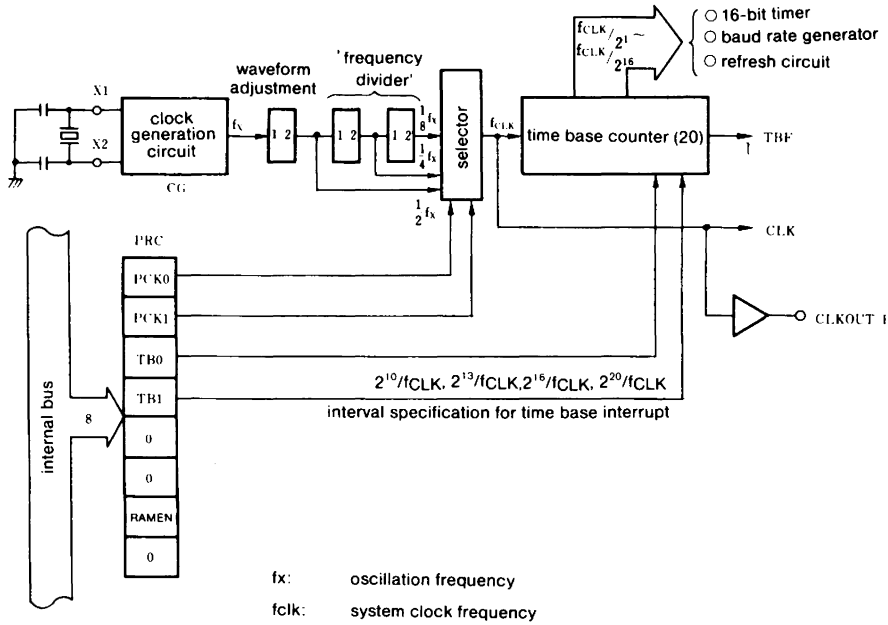
0 WAIT → 12 CLOCKS
1 WAIT → 12 CLOCKS
2 WAIT → 14 CLOCKS

6. Clock Generation Circuit

The Clock generation circuit supplies all types of clock to the CPU and to peripheral hardware and is a circuit which controls the CPU's operation mode. 6.1 Configuration of clock generation circuitry

Clock generation circuit is configured as in Fig. 6-1

Fig. 6-1 Block diagram of clock generation circuit



fx: oscillation frequency

fclk: system clock frequency

PRC: processor control register

TBF: time base interrupt request flag

CLKOUT: system clock output flag

The clock generation circuit uses a crystal oscillator connected to X1 and X2 pins or a ceramic oscillator. Clock generation circuit output undergoes a „waveform adjustment" (1/2 „frequency division"), selects „frequency division" ratio and is used as a system clock (CLK).

The CLK „frequency division" ratio can select oscillation frequencies of 1/2, 1/4, and 1/8 by specifying bit 0, 1 (PCK0, PCK1) of the processor control register (PRC).

Low-speed use of clock guarantees long periods of stable operation even if the voltage of a battery-driven system decreases.

6.2 Processor Control Register (PRC)

The PRC register is an 8-bit register which carries out concentrated control of CPU operations clock, time base interrupt periods, internal RAM access and other items related to the CPU and internal system control.

The PRC register can be accessed with 8/1-bit Read/Write operations using memory access.

It is initialized at 4EH using RESET input.

The PCK0,1 bits determine the system clock „frequency division" ratio. After „frequency division" of the frequency of the oscillator via PCK0,1, it is used as system clock (CLK).

The TB0,1 bits specify the time base interrupt interval. Four types of long interval time can be selected by using the TB0,1 bit.

The RAMEN bit controls enable for internal RAM access. It makes no distinction of internal RAM address in disable conditions (RAMEN bit „0") and accessing is always the object of external memory. When RAM is referenced as a register, internal RAM is always the object of accessing.

Fig. 6-2 Format of Processor Control Register (PRC)

ıbol	7	6	5	4	3	2	1	0	address
PRC	0	RAMEN	0	0	TB1	TB0	PCK1	PCK0	××FEBH

PCK1	PCK0	'frequency division' ratio specification of system clock (CLK)
0	0	f_{CLK} = oscillation frequency (fx) x ½
0	1	f_{CLK} = oscillation frequency (fx) x ¼
1	0	f_{CLK} = oscillation frequency (fx) x 1/8
1	1	disabled

TB1	TB0	interval designation for time base interrupt
0	0	generation of interrupt each $2^{10}/f_{CLK}$ interval
0	1	$2^{13}/f_{CLK}$
1	0	$2^{16}/f_{CLK}$
1	1	$2^{20}/f_{CLK}$

RAMEN	specification of internal RAM enable
0	internal RAM disable
1	internal RAM enable

7 Time Base Counter

The μPD70322/70320 stores a long interval timer function for clock function.

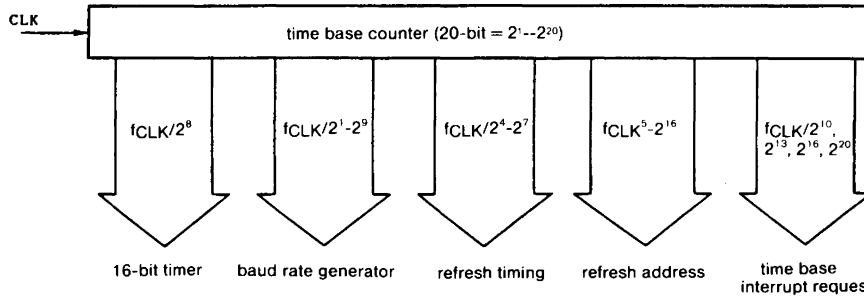
7.1 Configuration of Time Base Counter

Configuration of time base counter is illustrated in Fig. 7-1.

The time base counter is configured of 20 „frequency dividers" which divide the frequency of the system clock (CLK). The „frequency divider's lower side of the tap output is used for time count clock, baud rate generation input clock, refresh timing generation and refresh address generation. Of the 20 tap outputs, output taps 9, 12, 15, and 19 are used for time base interrupts.

The time base counter is cleared 00H only by RESET input and afterwards it is always incremented continnously.

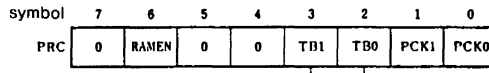
Fig. 7-1 Configuration of Time Base Counter



7.2 Specification of Time Base Interval

The interrupt request interval time which is generated from the time base counter can be selected from four types (as indicated in Fig. 7-2) using bit 2,3 (TB0,1) of the processor control register (PRC).

Fig. 7-2 Interval Timer Mode of the Processor Control Register (PRC)



fCLK= 5MHz (=½ fx, fx = 10MHz)

TB1	TB0	interval time
0	0	$2^{10}/f_{CLK}$ (205μs)
0	1	$2^{13}/f_{CLK}$ (1.64ms)
1	0	$2^{16}/f_{CLK}$ (13.1ms)
1	1	$2^{20}/f_{CLK}$ (210ms)

Note: time immediately after setting TB0, 1 bit until generation of initial interrupt request is undefined.

7.3 Time Base Interrupt Request Control Register (TBIC)

The TBIC is an 8-bit register used to carry out mask control for interrupt requests generated from the time base counter.

TBIC can be accessed with 8/1-bit Read/Write operations using memory access.

TBIC is initialized at 07H using RESET input.

Fig. 7-3 Format of time base interrupt request control register (TBIC)

symbol	7	6	5	4	3	2	1	0	address
TBIC	TBF	TBMK	0	0	0	1	1	1	××FECH

Interrupt requests are generated once the output tap of the time base counter specified by processor control register (PRC) has gone to high level and the interrupt request flag (TBF) is set.

The TBIC bit 4.5 is fixed „0" and there is no context-switching function or macro-service function using the timer base counter interrupt. The TBIC bit 0-2 are fixed at „1", priority of time base interrupt (INTTB) is „7" fixed, and is fixed at the lowest position even among the other interrupts which have priority 7. Multiprocessing control, is accepted, however.

8. Serial Interface

8.1 Configuration of Serial Interface

The μPD70322/μPD70320 has two serial interface channels with built-in special baud rate generators. The serial interface has two types of operational mode: an asynchronous (start/stop transmission) mode which takes data bit synchronization and charakter synchronization using start bit in the asynchronous mode and an I/O interface mode which carries out data transmission by synchronizing in the serial clock which has been controlled in the same way as the μCOM-87 group and other serial data transmission modes.

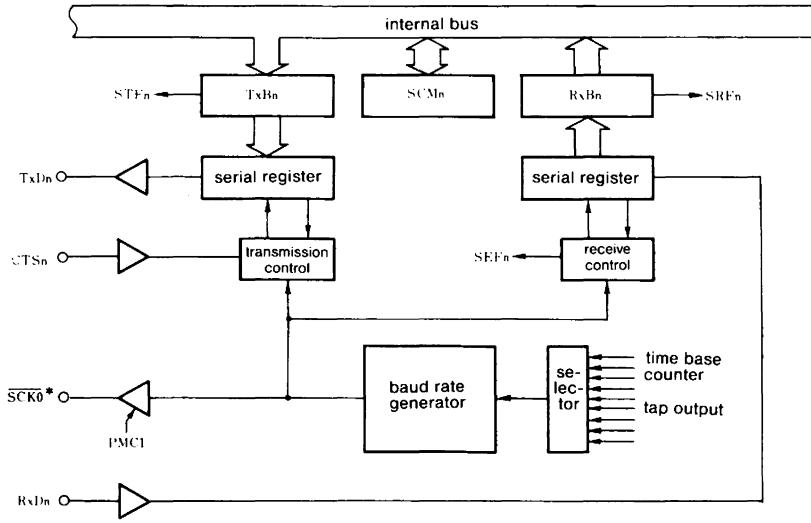
Fig. 8-1 gives a configuration diagram once for setting of serial interface asynchronous mode and once for I/O interface set-up.

The serial interface part is comprised of serial data input (RxDn), serial data output (TxDn), serial clock output (SCKO) transmission-enabling control input terminal (CTSn1), a transmission controller, an 8-bit serial register for send/receive, a transmission buffer (TxBn), a receive buffer (RxBn) and a baud rate generator.

It has serial registers and serial buffers for each transmission and receiving so that the transmission and reception can be carried out independently (all overlapping operations are possible). The CTSn terminal has functions for the receive clock input/output terminal during I/O interface mode so that all serial operations are possible and may overlap, even in I/O interface mode.

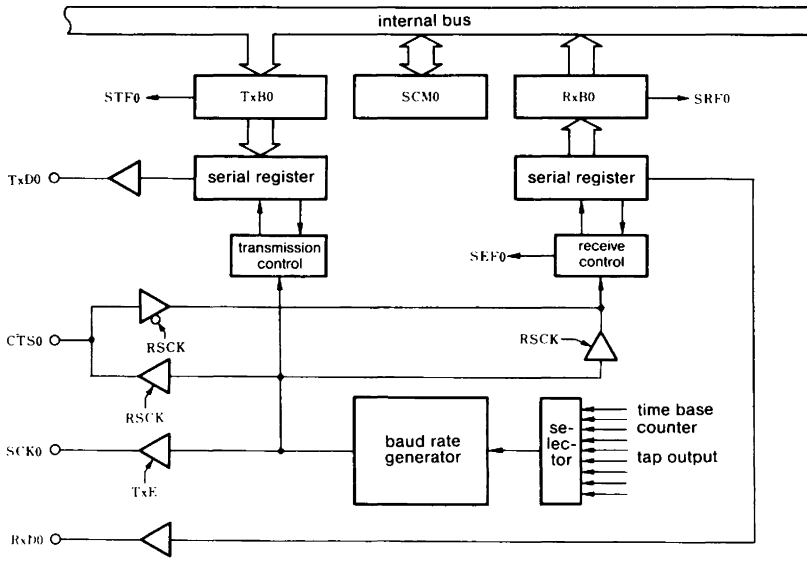
Fig. 8-1 Configuration of Serial Interface

(a) when asynchronous mode is set up (n-0, 1)



*(channel 0)

(b) when I/O interface mode is set up (channel 0 only)



8.2 Asynchronous Mode

During asynchronous mode, the specification of character length, number of stop bits, parity enable, odd/even parity is made by the serial mode register (SCMn).

(1) Transmission

In transmission operations bit 7 (TxRDY) of serial mode register (SCMn) is set (1) and the CTSn terminal goes to transmit enable condition at active time (0).

There are three methods of transmission start:

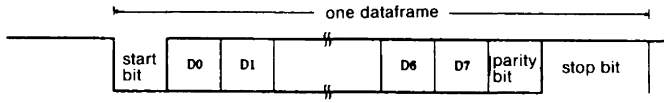
(i) transmission buffer (TxB) is set up in transmission condition when empty which generates transmission completion interrupt requests and carries out transmission data write operations to the transmission buffer within interrupt processing.

(ii) when transmission data are transmitted to transmission buffer at transmission enable condition, this transmission data are continuosly sent after the preceding transmission operation has ended.

(iii) in transmission disable condition, transmission data are writen beforehand in transmission buffer and the data reatined in the transmission buffer are sent afterwards when it is put in transmission enable condition.

*: there are no restrictions as such in the procedure for setting up the transmission enable condition; it is possible to make TxRDY=„1" active and set it at TxRDY=„1".

In the transmission data format, one data frame is comprised of start bit, character bit, parity bit and stop bit as the following figure indicates; the data transmitted is sent from the TxDn terminal starting with least significant bit (LSB). The TxDn terminal is in mark condition (1) during transmit disable or when it has no data which it is transmitting to serial register.



start bit ..... 1 bit
character bit ..... 7/8 bit
parity bit odd/even/0/unattached
stop bit ..... 1/2 bit

When the transmission buffer becomes empty the interrupt request for transmission completion is immediately generated and the transmission buffer goes to empty condition due to RESET input. When it is set to transmission enable condition at this time, the interrupt requests for transmission completion are generated. When transmit data from the transmit buffer are sent to the shift register by starting transmission operations, the transmission buffer goes to empty condition and there interrupt requests for transmission completion are generated.

Each time an interrupt request for transmission completion is generated continuous data transmission is possible by writing the transmission data in the transmission buffer without the mark condition (1) becoming inserted.

While transmission operations are being carried out the data being transmitted are sent one frame at a time until the end of the data or when switched to transmit disable condition. However, when new transmission data have already been written into the transmission buffer, sending from transmission buffer to shift register is disabled and transmission buffer contents are retained as they are. When it is again set to transmit enable condition, the transmission buffer contents coinciding with this timing are sent to shift register and interrupt request for transmission completion are generated at the same time that transmission has started.

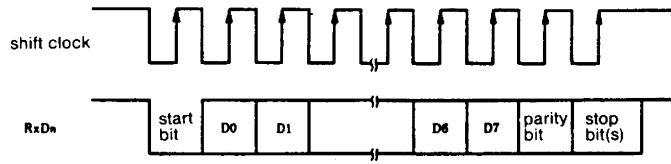
(2) Receiving

In receiving operations, it goes to receive enable condition when bit 6 (RxE) of serial mode register (SCMn) is set (1). (In receive disable condition (RxE=0) the hardware for receive is in a standby condition).

Sampling is carried out on the RxDn terminal input using the input clock to the baud rate generator; when the trailing edge is detected, receive operations are started up and a receive baud rate generator is started. When a RxDn pin input low level is detected using the initial timing signal from the receive baud rate generator, receiving operations are carried out after they have been recognized as a start bit. When high level has been detected by the initial timing signal, the baud rate generator is initialized without having recognized a start bit and operations are suspended.

Sampling of receiving data is carried out through synchronization with rise of a shift clock after the start bit has been detected, as indicated in the following figure.

Sampling timing of receive data



The receive interrupt requests are generated when the receive data from the shift register are sent to receive buffer (RxBn) when reception of data whose character length has been specified by serial mode register bit 3 (CL) has ended. During reception, receive error flag is set and receive error interrupt requests are generated, a parity check of even and odd numbers is carried out (when parity 1 bit=1*), and if they do not match (parity error), or when stop bit is low level (framing error), or when receive buffer is full and the subsequent data are sent to receive buffer (overrun error). (See 8.6).
Note: The PRTY1 bit is Bit 5 of the serial mode register.

8.3 I/O Interface Mode

I/O interface mode is identical to the μCOM-87 serial interface and is effective either when expanding I/O to external parts or when connecting peripheral controllers (A/D converter, LCD controller).

When using I/O interface mode, data transmission is carried out starting with the most significant bit (MSB) with 8-bit fixed character length and without parity bit. I/O interface mode is used on channel 0.

(1) Transmission

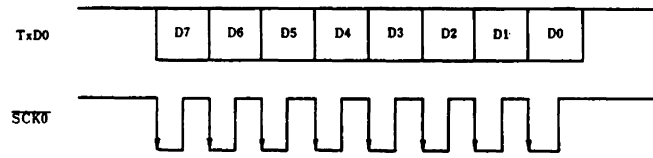
Transmission operations go to transmit enable condition when bit 7 (TxE) of serial mode register is set.

The SCKO terminal becomes transmission clock output pin in I/O interface mode. As with asynchronous mode, there are three types of transmission operation start-ups as follows:

(i) when transmission buffer (TxBO) is in empty condition, an interrupt request for transmission completion is generated by setting the buffer in transmit enable condition, and transmission data write operations to transmission buffer are carried out.

(ii) when transmission data are sent to transmission buffer (TxBO) in transmit enable condition, when the preceding transmission operation is completed, this transmission is continuously sent.

(iii) in transmit disable condition, transmission data are written in transmission buffer beforehand and when buffer is later put in transmit enable condition, the data retained in transmission buffer (TxBO) are sent.



Interrupt requests for transmission completion are generated as soon as transmission buffer (TxBO) is empty. Transmission buffer (TxBO) goes to empty condition due to RESET input. At this time, when it is set at transmit enable condition, interrupt requests for transmission completion are generated. When transmission data from transmission buffer (TxBO) are sent by starting transmission operations, the transmission buffer goes to empty condition and an interrupt request for transmission is generated.

(2) Receive

In receive operations, when bit 6 (RxE) in the serial mode register is set (1), it goes to receive enable condition. Receive data are input to serial register on receive clock rising edge. When the serial register receives 8-bit data, data are sent from the serial register to the receive buffer (RxBO) and an interrupt request for receive completion is generated.

Receive clocks in I/O interface mode are selected from both the external receive clocks and from the internal receive clocks by specifying bit 2 (RSCK) of the serial mode register (SCM0).

The CTSO terminal also functions as an input/output pin during I/O interface mode. Receive error flag is set and the interrupt request for receive error are generated at receive time when the receive buffer is full (RxBO) and when the following data have been sent to the receive buffer.

8.4 Serial Mode Register (SCM0, SCM1)

The SCMn register (n = 0, 1) is an 8-bit register which specifies the transmission mode for the serial interface and is set up at both channel 0 (SCM0) and channel 1 (SCM1). The assigned meanings of bits 7 to 2 on the SCMn vary according to specification of bits 1, 0 (MD1, MD0)

symbol	7	6	5	4	3	2	1	0	address
(channel 0) SCM0							MD 1	MD 0	××F68H
(channel 1) SCM1									××F78H

MD1, MD0=0,1 (asynchronous mode)

	7	6	5	4	3	2	1	0
SCM0	TxRDY	RxE	PRTY 1	PRTY 0	CL	SL	0	1
SCM1								

MD1, MD0=0, 0 (I/O interface mode)

	7	6	5	4	3	2	1	0
SCM0	TxE	RxE	0	0	TSK	RSCK	0	0

MD1 and MD0 bits are bit fields which specify transmission mode of serial interface. When they are set at MD1, MD0 = 0, 1, they go to asynchronous mode; when set at MD1, MD0 = 0, 0, they go to I/O interface mode. However, I/O interface mode can be set up only in SCM0.

SCMn can be accessed by 8/1-bit Read/Write operations by using memory access.

These registers are cleared to 00H by RESET input.

(1) Setting up of asynchronous mode

RxE a bit which carries out receive enable control.

When placed in receive disable condition (RxE = 0) during receive operations, receive processing is interrupted and no interrupt requests for receive completion are generated.

SL a bit which specifies stop bit

When SL bit is reset (0), the stop bit is 1 bit and it is 2 bits when set (1).

CL a bit which specifies character length.

When CL bis is reset (0) it is 7 characters long and 8 characters long when set (1).

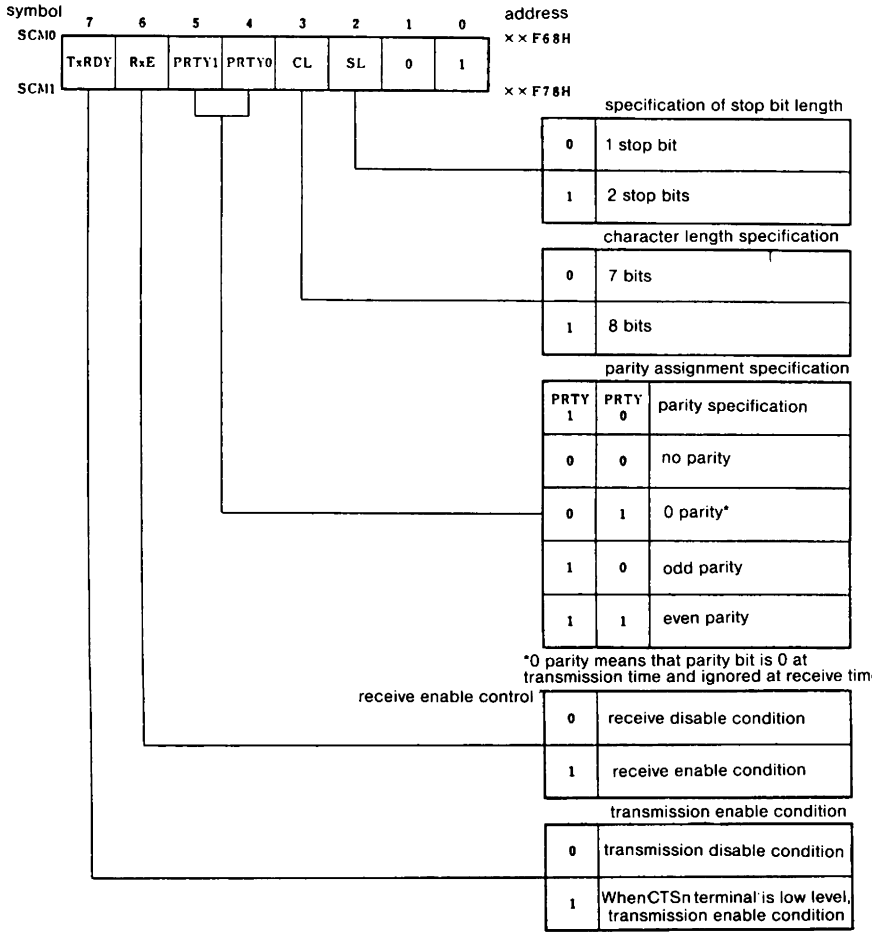
PRTY0 PRTY1 bits which specify parity assignment.

PRTY0, 1 bits specify no parity, odd and even number parity, and 0 parity. 0 parity makes parity bit "0" during transmission and ignores it during receive.

TxRDY is a bit which controls transmission enable condition.

When CTSn pin is low level and when TxRDY = 1, it causes the transmit enable condition.

Fig. 8-2 Format for Serial Mode Register (SCM0, SCM1) ... when setting up Asynchronous Mode



(2) Setting up of I/O Interface Mode

RSCK a bit which specifies source of serial receive clocks

When RSCK bit is reset (0), receive operations are carried out by external receive clock; when RSCK bit is set (1), receive operations are carried out by internal receive clock. Input/output for receive clock is carried out by CTSO pin.

TSK an output trigger bit for receive clock.

This is effective only when RSCK bit is set (1) and eight receive shift clocks are output from CTSO terminal by write operation of 1 to TSK bit.

RxE a bit which carries out receive enable control.

When RxE bit is set (1), it goes to receive enable condition; when reset (0), it goes to receive disable condition. When put in receive disable condition during receive operations, receive processing is interrupted at that point, and no interrupt requests for receive completion are generated.

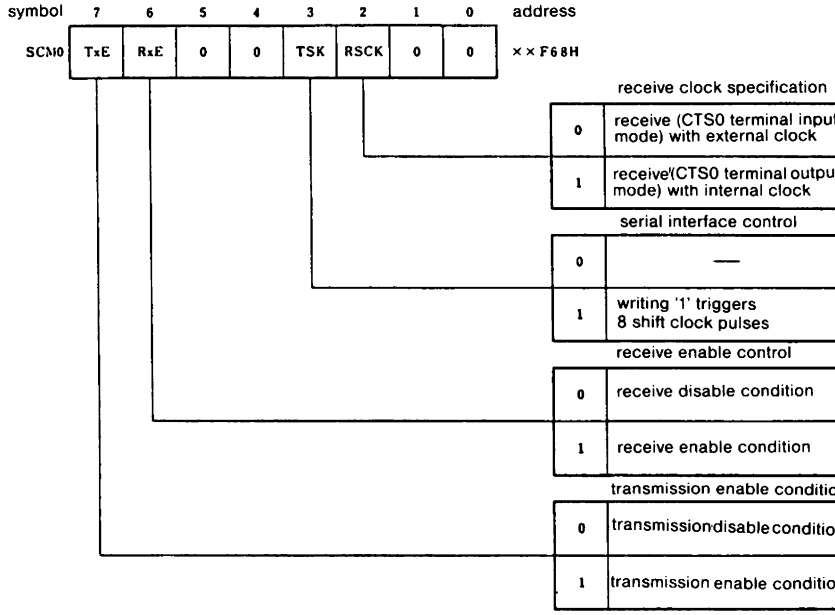
TxE a bit which carries out transmission enable control.

When TxE bit is set (1), it goes to transmission enable condition; when is is reset (0), it goes to transmission disable condition.

When transmission data are written into transmission buffer during transmission enable condition (TxE = 1), corresponding serial transmission is started after completion of running transmisson, and started immediately if no transmission is being carried out. When transmission data are written into transmission buffer during transmission disable condition (TxE = 0), serial transmission is not carried out, and data in the transmission buffer is retained unchanged. Afterwards, transmission processing of transmission data retained in the buffer is started at the same time when switching to transmission enable condition takes place.

Even if the TxE bit is reset (0) (transmission disable condition) during transmission operations, transmission operations are carried out until completion. However, the next transmission data which have already been stored in the transmission buffer at the point when it has been set to disable condition, the transmission following this transmission is omitted and the data are remaining in the buffer.

Fig. 8-3 Format for Serial Mode Register (SCM0) .... I/O Interface Mode



8.5 Baud Rate Generator

The baud rate generator is an 8-bit timer for the serial interface which generates shift clocks for transmission and receive. Each channel is provided with an own baud rate generator for transmission and receiving. The baud rate is the same both transmission and receiving and the baud rate is determined by writing the value to the baud rate generator register (BRGn).

The specification of the input clock for the baud rate generator is done by selecting the time base counter (see 7.1) output tap using the PRS3-0 bits of the serial control register (SCCn). The serial interface shift clock uses the baud rate generator output signals which have been divided by two. Setting up the baud rate generator for the transmit rate the parameter values satisfy the following formula:

$$B \times G = 10^6 \times \frac{CLK}{2n+1}$$

Where the parameters are defined as follows:

B: transmission baud rate (bps)
B = 110, ... 9600, 19200 . . .

G: set value for baud rate register (BRGn)
(1--G--255)

n: Input clock specification number (0--n--7)
for baud rate generator specified by serial control register (SCC).

CLK: system clock frequency (MHz)

Based on the above formula, the set values for the baud rate generator for all standard transmission baud rates when using a 10MHz crystal attached to the outside are as follows.

Chart 8-1 Set values for Baud Rate Generator (for reference)

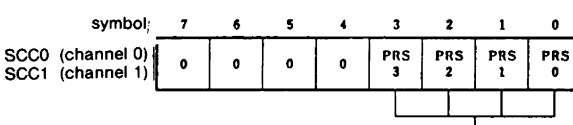
f_{CLK} = 5MHz (=½ fx; fx = 10 MHz)

transfer baud rate	n	set value G for BRGn register	error (%)
110	7	178	0.25
150	7	130	0.16
300	6	130	0.16
600	5	130	0.16
1200	4	130	0.16
2400	3	130	0.16
4800	2	130	0.16
9600	1	130	0.16
19200	0	130	0.16
38400	0	65	0.16
1.25M	0	2	0

n: input clock specification number of baud rate generator

8.5.1 Serial Control Registers (SCC0, SCC1)
The SCCn register (n=0, 1) is a register which controls serial interface transmission rate.
SCCn can be accessed by 8/1-bit Read/Write operations using memory access.
It is initialized at 00H using RESET input.
It specifies the output tap of the time base counter which is input to the baud rate generator in the PRS3-0 bit field.

Fig. 8-4 Format for Serial Control Registers (SCC0, SCC1)



PRS 3	PRS 2	PRS 1	PRS 0	input clock to baud rate generator
0	0	0	0	f_{CLK}
0	0	0	1	$f_{CLK}/2$
0	0	1	0	$f_{CLK}/4$
0	0	1	1	$f_{CLK}/8$
0	1	0	0	$f_{CLK}/16$
0	1	0	1	$f_{CLK}/32$
0	1	1	0	$f_{CLK}/64$
0	1	1	1	$f_{CLK}/128$
1	0	0	0	$f_{CLK}/256$

f_{CLK}: system clock frequency

8.6 Serial Error Processing

The following three types of serial interface errors during reception can be detected.

(i) Parity error (asynchronous mode)
Transmit parity and receive parity are different.

(ii) Framing error (asynchronous mode)
Stop bit is not detected.

(iii) Overrun error (asynchronous mode, I/O interface mode).

Before taking over the previous receive data from RxB, the following reception is completed.

8.6.1 Serial Error Registers (SCE0, SCE1)

These are 8-bit registers which indicate three types of error flag conditions corresponding to each receive error. Both channel 0 and channel 1 are provided with them.

SCEn (n=0, 1) can be accessed only by 8-bit Read operations using memory access.

SCEn is initialized with 00H during RESET.

ERPn Parity error flag

ERP flag is set when transmit parity and receive parity do not agree and is reset (1) during receive data read from receive buffer.

ERFn Framing error flag

ERF flag is set (1) when stop bit is not detected and reset (0) during receive data read from receive buffer.

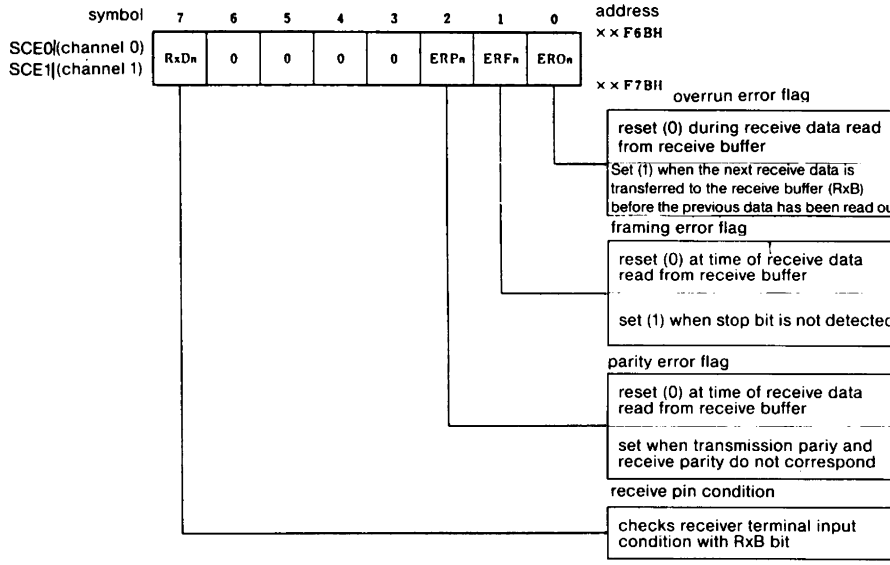
EROn Overrun error flag

ERO flag is set (1) when before receiving the preceding receive data from RxB the next receive is completed, and reset (0) during receive data read from receive buffer.

RxDn is a bit which checks receiver terminal input condition using RxB bit.

The serial error register (SCEn) is initialized at 00H using RESET input.

Fig. 8-5 Format of Serial Error Registers (SCE0, SCE1)



8.7 Break Detection Function

The μPD70322/70320 can be used to detect circuit break condition using software processing (asynchronous-mode only). Procedures for detecting a break condition are as follows:

(1) generation of receive error interrupt using the first framing error.

Receive data are checked inside receive error processing routine and are confirmed to be 00H.

At the same time, receive error flag is checked and the framing error is confirmed.

(2) generation of receive error interrupt using second framing error.

Framing error is again generated during break condition.

Receive data is again 00H, and continuous reception of 00H data which accompany framing error as well as confirmation of direct pin condition using bit 7 (RxDn) of serial error register (SCEn) are used to decide that the circuit is in break condition.

8.8 Interrupt Requests for Serial Interface

There are three types of interrupt requests which are generated by the serial interface and which correspond to the two channels: interrupt requests for transmission completion, for receive completion, and for receive error.

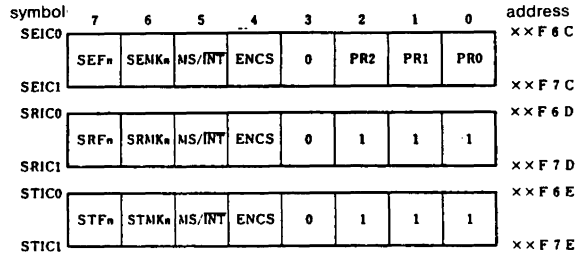
8.8.1 Control Registers for Interrupt Requests (SEICn, SRICn, STICn) n=0, 1

These are registers which control three types of interrupt requests generated from the serial interface: interrupt requests for receive error (SERn), for receive completion (SRFn), and for transmission completion (STFn). The three control registers for interrupt requests form one group and can be applied a priority specified for the serial interface interrupt request. The priorities inside the group are decided using hardware in the following way:

SEFn > SRFn > STFn

when SEF = 1, SRF is always set.

Fig. 8-6 Interrupt Control Registers (SEICn, SRICn, STICn) (n=0,1)



(Note) The SRICn and STICn bits 2-0 are fixed at '1' using hardware. Bit 2-0 is a bit field (PR2-0) which specifies priority of interrupt requests according to group and form a group within SEICn. Interrupt request priority for SRICn and STICn conform to set-up of PRs-0 of SEICn.

Bits SEFn, SRFn, and STFn are interrupt request flags and are all set (1) respectively according to generation of receive error, receive completion, and transmission completion, and are reset, by acceptance of interrupt requests or by software.

See 3.7 for description of other bit fields.

SEICn, SRICn, and STICn can be accessed by 8/1-bit Read/write operations using memory access. SEICn, SRICn, and STICn are initialized at 47H using RESET input.

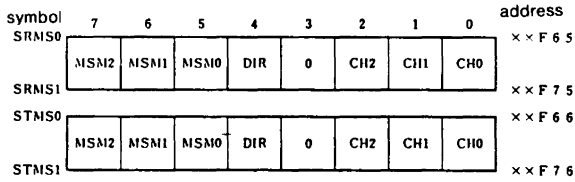
8.8.2 Macro-Service Control Registers (SRMSn, STMSn) n=0,1

SRMSn is an 8-bit register which specifies macro-service processing mode which accompanies receive completion of serial interface. STMSn is an 8-bit register which specifies the macro-service processing mode and the channel which accompany the transmission completion of the serial interface. SRMSn and STMSn correspond to the two serial interface channels.

SRMSn and STMSn can be accessed by 8/1-bit Read/Write operations using memory access.

See 3.4.3 for description of each macro-service regsiter bit.

Fig. 8-7 Format of Macro-Service Control Register (SRMSn, STMSn) n=0,1



9. Timer Unit

The μPD70322/70320 timer unit can be used as an interval timer, a one shot timer, and as a square wave output.

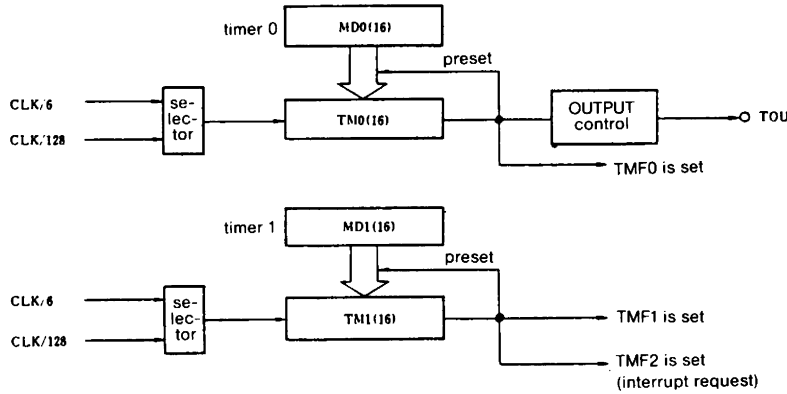
9.1 Configuration and Operation of Timer Unit

The timer unit is comprised of two 16-bit timer registers, two 16-bit modulo/timer registers and an 8-bit timer control register. Configuration and operation of each operational mode are described as follows.

(1) Interval timer mode

When timer unit is set up in interval timer mode, both timers 0 and 1 can be used as in Fig. 9-1.

Fig. 9-1 Configuration of Timer Unit during Interval Timer Mode



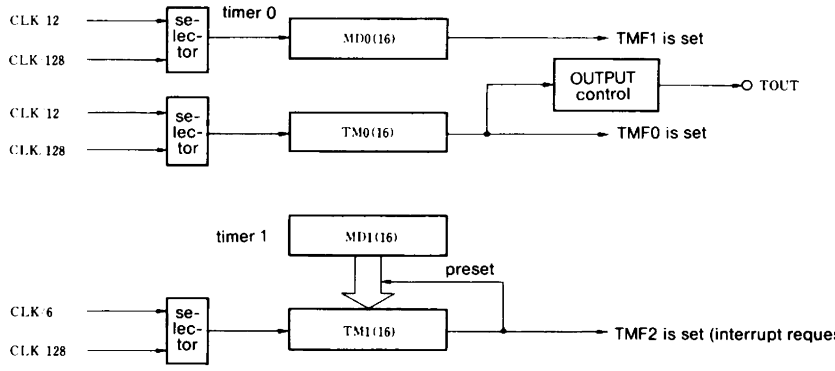
Interval timer mode is specified by timer control register (TMCO) and when TSO bit is set (1), the MDO register value is loaded into the TMO register, and the clock specified by TCLKO is down counted. When an underflow is generated during down count, the MDO register value is again reloaded into the TMO register and the down count is again repeated.

The same down count operations are executed for register of timer 1.

(2) One shot timer mode

When timer unit is set up in one shot timer mode, channel 0 is used as indicated in Fig. 9-2. However, it is still possible to operate timer 1 (channel 1) simultaneously as an interval timer.

Fig. 9-2 Configuration of Timer Unit during One Shot Timer Mode



The one shot timer mode is specified by the timer control register (TMCO) and when TSO/MSO bit is set (1), the TMO/MDO register down counts clocks specified by TCLKO/MCLKO bit. When an underflow is generated during counting, the count operations are suspended. TMO/MDO register is suspended while retaining 000H.

9.2 Timer Control Registers (TMC0, TMC1)

The TMC0 register is an 8-bit register which controls operations of TM0 and MD0 registers. The TMC1 register is an 8-bit register which controls operations of TM1 and MD1 registers.

TMC0 and TMC1 registers can be accessed by 8/1-bit Read/Write operations using memory access. They are initialized at 00H using RESET input. TMC0 and IMC1 registers have different formats as shown in the following figures.

(interval timer mode, one shot timer mode)

symbol	7	6	5	4	3	2	1	0	address
TMC0	TS0	TCLK0	MS0	MCLK0	ENTO	ALV	MOD1	MOD0	××F90H

(interval timer mode)

	7	6	5	4	3	2	1	0	
TMC1	TS1	TCLK1	0	0	0	0	0	0	××F91H

Operational mode for timer 0 and timer 1 which are comprised respectively of TM0 and MD0, and TM1 and MD1 are specified by bits 0, 1 (MOD0, 1) of TMC0 and TMC1 registers.

MOD0 and MOD1 are bits which specify the operational modes for timer 0 and timer 1.

When MOD0 = 0 and MOD1 = 0, the interval timer operation mode is set. When MOD0 = 1 and MOD1 = 0, the one-shot timer mode is set.

During the interval timer operation mode, TM0 and TM1 work as timer registers which down-count the set values, where as MD0 and MD1 work as modulo registers which retain the set values for the intervals. Under the one-shot timer operation mode both TMO and MDO work as timer registers down counting the set values. The timer 1, however has ists TMC1 bits 0 and 1 fixed as "0", capable of operating only as an interval timer.

As a result, timer 0 can operate as a 16-bit interval timer or as two 16-bit one shot timers comprised of TMO and MDO using TMCO register. Timer 1 can be operated as a 16-bit interval timer comprised of TM1 and MD1 using TMC1 register.

Timer 0 can also output rectangular waves to the TOUT pin using the TMCO register. However, TOUT pin used with P15 to output rectangular waves to TOUT pin so that bit 5 (PMC15) of port 1 mode control register must be put on control mode.

ALV is a bit which specifies the active level for TOUT pin output.

The active level of TOUT pin output when ENTO bit is reset (0) goes to low level when ALV bit is reset (0) and high active when set (1).

ENTO is a bit which specifies operations for square waves output to TOUT pin.

When ENTO bit is reset (0), the TOUT pin level is specified by ALV bit. When ENTO bit is set (1), the TOUT pin level is reserved every time the interrupt request flag of the timer unit is set.

Descriptions of other bits of TMC0 and TMC1 registers are given according to operational mode as follows.

TCLK is a bit which specifies TMn register count clock.

Chart 9-1 gives reference values for system clocks with 5MHz frequency.

TSn is a bit which controls the operations of timer n.

When TSn bit is set (1), the value of the MDn register is set into the TMn regsiter and the down count of TMn register is started. When the TSn bit is cleared (0) the TMn register down count is suspended with TMn and MDn register contents retained unchanged.

During down count, underflow is generated and when TSn bit is set (1) again, the value of MDn register is again reloaded into the TMn register and down count operations are restarted.

Chart 9-1 Count Time (n=0,1) for Timer Register (TMn) During Interval Timer Mode (f_{CLK} = 5 MHz (=½ fx; fx = 10MHz)

TCLKn	count clock	resolution	full count
0	$f_{CLK}/6$	1.2 μs	78.6 ms
1	$f_{CLK}/128$	25.6 μs	1.7 s

(2) One Shot Timer MOde (MOD0=1, MOD1=0) However, timer 0 only.

TCLK is a bit which specifies TMO register count clock.

Table 9-2 indicates reference values when system clock frequency (TCLK) is 5MHz.

TSO is a bit which controls TMO register operations.

When TSO bit is set, it is down counted from values of TMO register which have been retained at that time; TSO bit is cleared (0) by underflow generation, and count operations are suspended. When TSO is cleared (0), count is suspended while retaining TMO register value unchanged.

MCLKO is a bit which specifies MDO register count clocks.

Table 9-2 indicates reference values when system clock frequency (CLK) is 5MHz. When it is specified in interval timer mode, the MCLKO does not affect the count operation.

MSO is a bit which controls count operations for MD register.

When MSO bit is set (0), it is down counted from the MDO register values which are retained at that time; MSO bit is cleared (0) by underflow generation and count operations are suspended. When MSO bit is cleared (0), count is suspended while MDO register values are retained unchanged.

The MSO bit does not affect count operations during interval timer operations.

Chart 9-2 Count Time for Timer Register 0 (TM0) and Modulo Timer Register 0 (MD0) During One Shot Timer Mode f_{CLK} = 5MHz(=½ fx ; fx = 10 MHz)

TCLK0 / MCLK0	count clock	resolution	full count
0	$f_{CLK}/12$	2.4 μs	157.3 ms
1	$f_{CLK}/128$	25.6 μs	1.7 s

Note: the TM0 register has different count clocks depending on whether it has been specified in interval timer mode or specified in one shot time mode.

Fig. 9-3 Format of Timer Control Register 0 (TMC0)

ibol	7	6	5	4	3	2	1	0	address
MC0	TS 0	TCLK 0	MS 0	MCLK 0	ENTO	ALV	MOD 1	MOD 0	××F90H

operational mode specifications

MOD 1*	MOD 0	specification
0	0	interval timer mode
0	1	one shot timer mode
1	x	disable

*'0' must be written in MOD1

effective level specification for TOUT pin

0	TOUT pin active level is specified at low level
1	TOUT pin active level is specified at high level

operation specification for TOUT pin

0	TOUT pin level fixed at ALV bit
1	TOUT pin level reversed by TMF0 set timing

clock source specified for MD0 register (during one shot timer mode)

0	CLK/12 specified as MD0 register count clock
1	CLK/128 specified as MD0 register count clock

operation control for MD0 register (during one shot timer mode)

0	count stopped (MD0 retained)
1	MD0 down count started

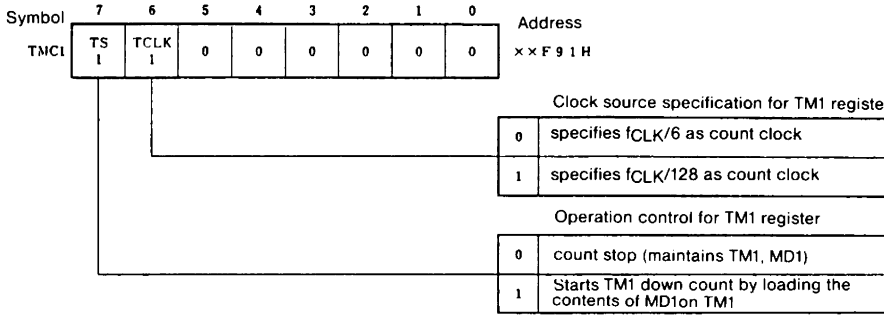
clock source specification for TM0 register

during interval timer	0	$f_{CLK}/6$ specified as TM0 count clock
	1	$f_{CLK}/128$ specified as MD0 count clock
during one shot mode	0	$f_{CLK}/12$ specified as TM0 count clock
	1	$f_{CLK}/128$ specified as TM0 count clock

operation control for TM0 register

during interval timer mode	0	count stopped (TM0, MD0 retained)
	1	MD0 contents loaded to TM0; TM0 down count started
during one shot timer mode	0	count stopped (TM0 retained)
	1	TM0 down count started

Fig. 9-4 Format of Timer Control Register 1 (TMC1)



9.3 Timer Unit Interrupt Requests

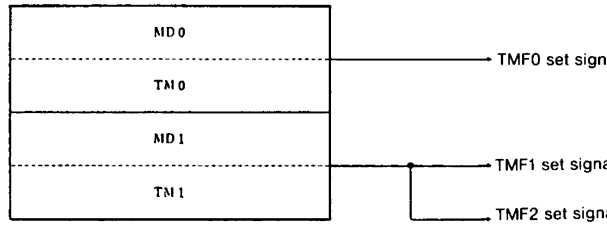
Three interrupt requests (TMF0-2) are generated from the timer unit. The generation condition for the interrupt requests coming from the timer unit differ according to the specification of the timer operation mode.

When they are set up to interval timer mode, the TMF0 is set (1) by the timing of underflow generated by the TM0 register countdown, and TMF1 and TMF2 are set (1) by underflow generated by TM1 register countdown (Fig. 9-5a).

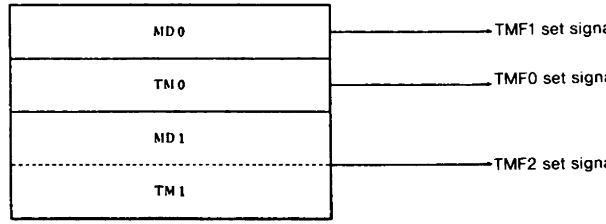
When TM0 and MD0 registers are set up in one shot timer mode, TMF0 is set (1) by underflow generated by TMO register countdown and TMF1 is set (1) by underflow generated by MD0 register countdown. In this case, TMF2 is set (1) by the underflow generated by TM1 regsiter countdown which operates as an interval timer.

Fig. 9-5 Interrupt Requests from Timer Unit

a. when TM0 and MD0 are specified as Interval Timer Mode



b. when TM0 and MD0 are specified as One Shot Timer Mode



TMF0-2 timer unit interrupt request flag 0-2

9.3.1 Interrupt Request Control Registers for Timer Unit (TMIC0, TMIC1, TMIC2)

The TMICn (n=0-2) register is an 8-bit register which controls three interrupt requests which are generated from the timer unit. These three interrupts requests form one group and priority for the timer unit interrupt requests as specified by program. Within that group, priority is fixed using hardware as follows.

TMF0 > TMF1 > TMF2

Fig. 9-6 Format of Interrupt Request Control Registers for Timer Units (TMICO, TMIC1, TMIC2)

Symbol	7	6	5	4	3	2	1	0	Address
TMIC0	TMF0	TMMK0	MS/$\overline{INT}$	ENCS	0	PR2	PR1	PR0	××F9CH
TMIC1	TMF1	TMMK1	MS/$\overline{INT}$	ENCS	0	1	1	1	××F9DH
TMIC2	TMF2	TMMK2	MS/$\overline{INT}$	ENCS	0	1	1	1	××F9EH

(Note) Bit 2-0 for TMIC1 and TMIC2 are fixed at "1" by hardware. Bit 2-0 is a bit field (PR2-0) which specifies the priority of interrupt requests in the group and it forms one group with TMIC0. Priority for TMCI1 and TMIC2 interrupt requests conforms with setting of PR2-0 for TMIC0.

See 3.7 for explanation of each of the TMICn register bits.

The TMICn regsiter can be accessed by 8/1 bit Read/Write operations using memory access.

The TMICn regsiter is initialized at 07H by RESET input.

9.3.2 Macro-Service Control Registers for Timer Unit (TMMS0, TMMS1, TMMS2)

These are 8-bit registers which control macro-service started by the three types of interrupt requests generated from the timer unit.

The TMMS0 register controls macro-service started by the TMF0 flag. The TMMS1 and TMMS2 both control macro-service which is started by TMF1 flag (for TMMS1) and TMF2 flag (for TMMS2).

TMMSn (n=0-2) can be accessed by 8/1-bit Read/Write operations using memory access.

Fig. 9-7 Format of Macro-Service Control Registers for Timer Unit (TMMS0, TMMS1, TMMS2).

Symbol	7	6	5	4	3	2	1	0	Address
TMMS0	MSM 2	MSM 1	MSM 0	DIR	0	CH 2	CH 1	CH 0	××F94H
TMMS1									××F95H
TMMS2									××F96H

See 3.4 for explanation of TMMSn regiter bits.

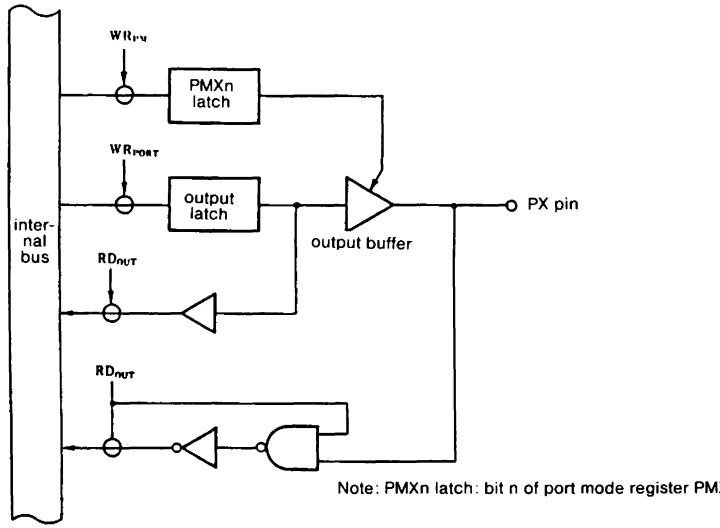
10 PORT FUNCTIONS

10.1 Port 0-2

10.1.1 Hardware Configuration

The μPD70322/μPD70320 ports 0-2 are basically comprised of three state bidirectional ports as indicated in Fig. 10-1. Each port mode register bit is set (1) by RESET input and thus specified as input port. All port pins are placed in a high impedance condition. The output latch contents are not influenced by RESET input.

Fig. 10-1 Configuration of Port 0-2

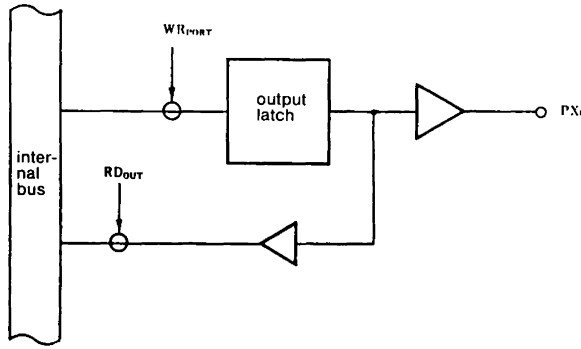


Note: PMXn latch: bit n of port mode register PMX

(1) When specified as output port (PMXn = 0)

The output latch is effective and data exchange between output latch and accumulator can be carried out by transfer instructions. Output latch contents can be set without restriction by logical operation instructions. Once data are written into the output latch, they are retained until the next instruction to operate the port is executed.

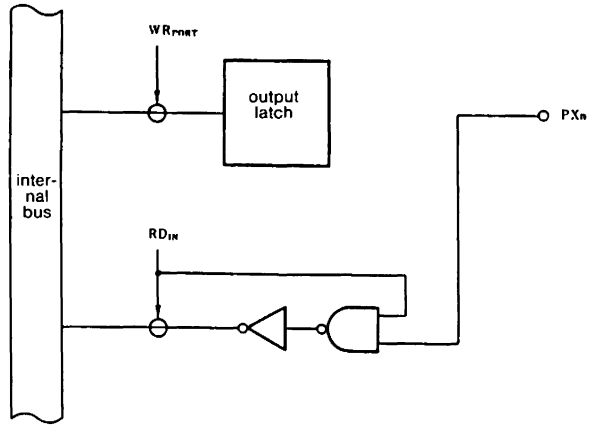
Fig. 10-2 Port for Output Port Specification



(2) when specified as input port (PMXn = 1)

Port pin level can be loaded to the accumulator using transfer instructions. Even in this case writing into the output latch is possible and data sent from accumulator using transfer instructions are latched completely by the output latch regardless of port input/output specification. However, the bit output buffer specified at input port goes to high impedance condition so that there is no output to the port pin. (When the bit for input/output specification has been switched to the output port the contents of the output latch are not output to the port terminal). The contents of the output latch of the bit specified as input port can not be loaded to the accumulator. (Fig. 10-3)

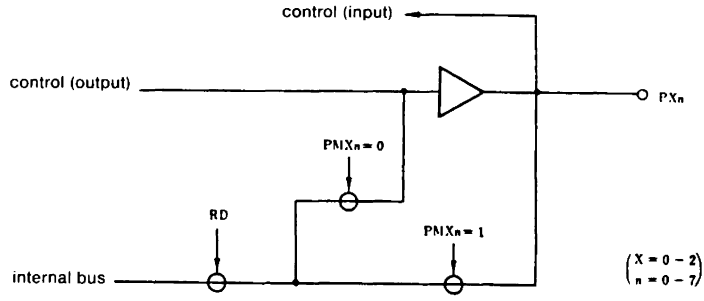
Fig. 10-3 Port for Input Port Specification



(3) with control specification (PMCXn = 1)

In working with port 0-2, the bit of port mode control register (PMCX) is set (1) so that it can be used as input or output for control signals in units of bits regardless of the port mode register (PMX) set up. When a pin is used for a control signal the condition of the control signal can be checked by executing the port access instructions.

Fig. 10-4 Port for Control Signal Specification



(ii) when port is control signal output

When the port mode register (PMXn) is set (1) it is possible to read the control signal pin condition when the port read instruction is executed.

When the port mode register is reset (0) it is possible to read the condition of the internal control signal.

(ii) When port is control signal input

When the port mode register is set (1), it is possible to read the pin condition of the control signal when the port read instruction is executed.

10.1.2 Port Functions

(1) P00-07 (port 0) . . . . . three state input/output

This is a special 8-bit input/output port. Besides functioning as a general purpose input/output port whose input/output can be specified in bit units, it can also function as a system clock pin (for use with P07). Switching for these can be carried out in bit units by specifying the port 0 mode register (PM0) as well as the port 0 mode control register (PMC0).

Chart 10-1 Port 0 Operation (n=0-7)

	PMC0n = 1	PMC0n = 0	
		PM0n = 1	PM0n = 0
P00		input port	output port
P01		input port	output port
P02		input port	output port
P03		input port	output port
P04		input port	output port
P05		input port	output port
P06		input port	output port
P07	CLKOUT output	input port	output port

(i) Port 0 mode control register (PMC0)

This is an 8-bit register used to define the use as port/system clock output for port 0 in bit units. As a result, the PMC0 register can be accessed by 8/1-bit Read/Write operations using memory access. If the corresponding bit of the PMC0 register is set (1) it defines the system clock output mode (P07), if reset, they go to port mode. All the bits of the PMC0 register during RESET input are reset (0) and it goes to port mode.

Fig. 10-5 Format for Port 0 Mode Control Register (PMC0)

Symbol	7	6	5	4	3	2	1	0	Address
PMC0	PMC0 7	0	0	0	0	0	0	0	××F02H

0	P0n=port mode
1	P07=system clock output

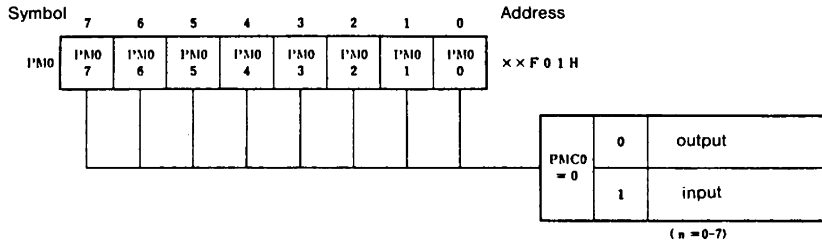
(ii) port 0 mode register (PM0)

PM0 is an 8-bit register which specifies input/output for port 0 using bit units.

PM0 can be accessed by 8/1-bit Read/Write operations using memory access. When the corresponding bit in PMC0 is "0", the PM0 becomes valid.

All bits are set (1) using RESET inout

Fig. 10-6 Format of Port 0 Mode Register (PM0)



(2) P10-17 (Port 1) . . . . . three state input/output

This is a special 8-bit input/output port. Besides functioning as a general-purpose input/output port whose input and output can be specified in bit units, it functions as a number of control pins. Switching for these can be carried out in bit units by specifying the port 1 mode register (PM1) as well as port 1 mode control register (PMC1).

The P10-P13 terminals can read the pin levels by direct accessing of port 1 (P1).

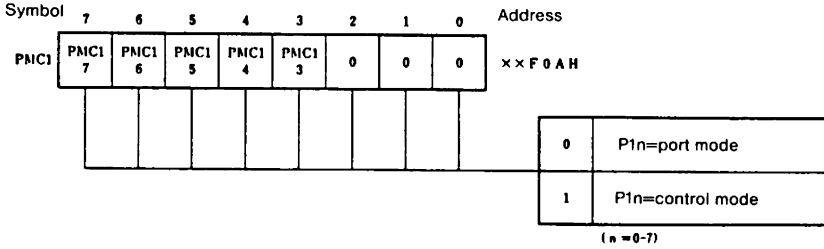
Table 10-2 Port 1 Operations (n=0-7)

	PMC1n=1	PMC1n=0	
		PM1n=1	PM1n=0
P10		NMI input	
P11		$\overline{\text{INTP0}}$ input	
P12		$\overline{\text{INTP1}}$ input	
P13	$\overline{\text{INTAK}}$ output	$\overline{\text{INTP2}}$ input	
P14	INTR input	input port (POLL input)	output port
P15	TOUT output	input port	output port
P16	$\overline{\text{SCKO}}$ output	input port	output port
P17	READY input	input port	output port

(i) Mode control register (PMC1) for port 1

This is an 8-bit register which can specify in bit units the use of port 1 for port-control signals or as input/output. As a result, the PMC1 register can be accessed by 8/1-bit Read/Write operations using memory access. When the corresponding bit in PMC1 register is set (1) it defines the control signal input/output mode, if it is reset (0), it is in the port mode. However, the P10-P12 pins are fixed in port mode.

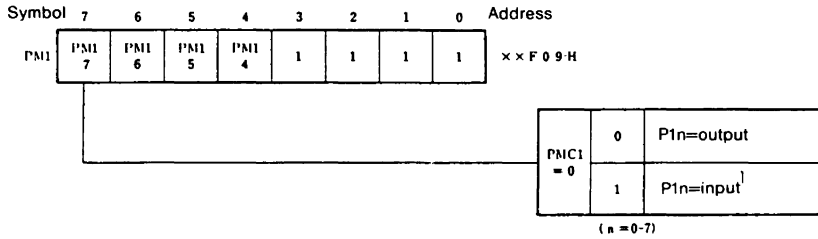
Fig. 10-7 Format for port 1 mode control register (PMC1)



(ii) Port 1 mode register (PM1)

The PM1 is an 8-bit register which specifies input or output for port 1 in bit units. As a result, the PM1 can be accessed by 8/1 bit Read/Write operations using memory access. When the corresponding bit of PMC1 is "0" PM1 becomes valid.

Fig. 10-8 Format of port 1 mode register (PPM1)



(3) P20-27 (port 2) . . . . . three state input/output.

This is a special 8-bit input/output port. A side from functioning as a general-purpose input/output port for which input/output can be specified in bit units it also functions as a number of control pins. Switching for these can be carried out in bit units by specifying the port 2 mode register (PM2) as well as the port 2 mode control register (PMC2).

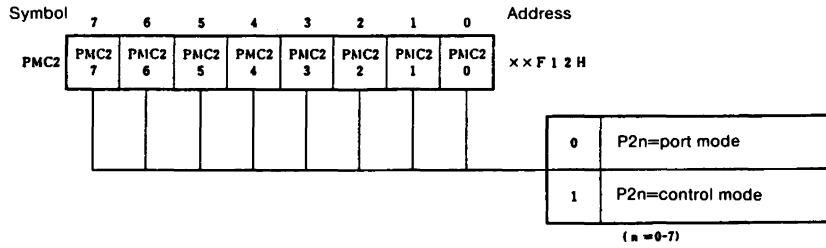
Chart 10-3 port 2 operations

	PMC2=1	PMC2=0	
		PM2n=1	PM2n=0
P20	DMARQO input	input	output port
P21	$\overline{\text{DMAAK0}}$ output	input	output port
P22	$\overline{\text{TC0}}$ output	input	output port
P23	DMARQ1 input	input	output port
P24	$\overline{\text{DMAAK1}}$ output	input	output port
P25	$\overline{\text{TC1}}$ output	input	output port
P26	$\overline{\text{HLDAK}}$ output	input	output port
P27	HLDRQ input	input	output port

(i) Port 2 Mode Control Register (PMC2)

This is an 8-bit register which can specify the use of port 2 for port/control signals or as input/output port for port 2 in bit units. If the corresponding bit of the PM2 is set (1) it defines the control signal input/output mode, if it reset (0), it goes to port mode. During reset input, the PMC2 register is reset (0), and it goes to port mode.

Fig. 10-9 Format of Port 2 Mode Control Register (PMC2)

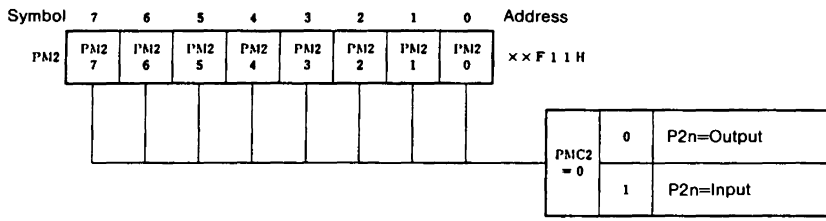


(ii) Port 2 Mode Register (PM2)

The PM2 is an 8-bit register which specifies input/output for port 2 in bit units. As a results, the PM2 can be accessed by 8/1 bit Read/Write operations using memory access. When the corresponding bit in PMC2 is 0, PM2 becomes valid.

All bits are set (1) by RESET input.

Fig. 10-10 Format of Port 2 Mode Register (PM2)



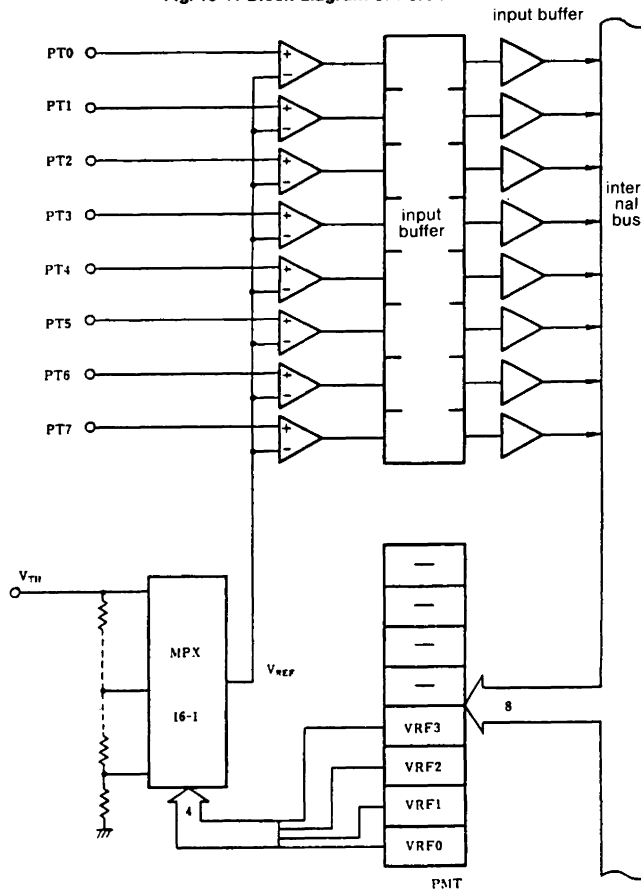
10.2 Port T (PT0-PT7)

Port T is an 8-bit input port which can vary the threshold voltage (reference voltage) in 16 stages. Comparator operations are carried out by analog input.

10.2.1 Hardware Configurations

Port T contains a multiplex circuitry (MPX) which selects one of PT0-PT7 comparator inputs, a V_{th} pin for standard power supply input to generate a matching voltage (V_{ref}) in 16 steps ranging from 1/16 X V_{th} up to 16/16 X V_{th}, of a port mode T register (PMT) which controls MPX and of 8 latches (Fig. 10-11). The V_{ref} and PT0-PT7 input (selected by setting up PMT) are compared using a comparator and the result is then latched into the port T input latch.

Fig. 10-11 Block diagram of Port T



10.2.2 Port T Mode Register (PMT)

PMT sets up the comparison voltage (V_{ref}) for the comparator as one of the 16 steps as indicated in Fig. 10-12.

PMT can be accessed by 8/1 bit Read/Write operations using memory access. All of the PMT bits are reset (0) by RESET input.

Fig. 10-12 Format of Port T Mode Register (PMT)

Symbol	7	6	5	4	3	2	1	0	Address
PMT	–	–	–	–	VREF 3	VREF 2	VREF 1	VREF 0	××F3BH

VREF 3	VREF 2	VREF 1	VREF 0	V_{REF}
0	0	0	0	$V_{TH}\times 16/16$
0	0	0	1	$V_{TH}\times 1/16$
0	0	1	0	$V_{TH}\times 2/16$
0	0	1	1	$V_{TH}\times 3/16$
0	1	0	0	$V_{TH}\times 4/16$
0	1	0	1	$V_{TH}\times 5/16$
0	1	1	0	$V_{TH}\times 6/16$
0	1	1	1	$V_{TH}\times 7/16$
1	0	0	0	$V_{TH}\times 8/16$
1	0	0	1	$V_{TH}\times 9/16$
1	0	1	0	$V_{TH}\times 10/16$
1	0	1	1	$V_{TH}\times 11/16$
1	1	0	0	$V_{TH}\times 12/16$
1	1	0	1	$V_{TH}\times 13/16$
1	1	1	0	$V_{TH}\times 14/16$
1	1	1	1	$V_{TH}\times 15/16$

11 STANDBY FUNCTIONS

The μPD70322/70320/70320 has two standby function modes which control the clock operation.

- HALT mode . . . . . a mode which suspends clock supply for the CPU. However, a number of CPU status data and RAM are all retained and peripheral hardware continues operation. Intermittent operation by combination with normal operation mode is used to lower total system power consumption.
- STOP mode . . . . . a mode which stops the oscillator which leads to a complete stop of the entire system. Internal RAM and port output data are retained as they require only very low power consumption.

Setting up of various modes is carried out using the HALT and STOP instructions.

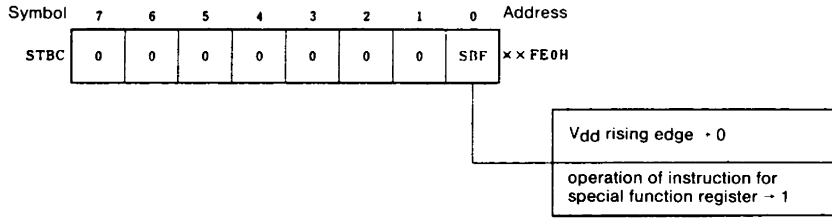
11.1 Standby Control Register (STBC)

The STBC is an 8-bit register which controls the standby flag (SBF).

SBF is used for the return decision from STOP condition. SBF is reset (0) only by starting power supply voltage (V_{dd}) and set (1) only by instruction execution for special function registers. SBF can be tested to distinguish whether there is a release after reset or return from STOP mode.

STBC is initialized by reset.

Fig. 11-1 Format for Standby Control Register (STBC)



11.2 HALT Mode

This is a mode which suspends clock supply for the CPU.

Setting up the HALT mode during CPU empty time reduces the overall power consumption for the system. When the HALT instruction is executed, it goes into HALT condition.

In HALT mode, the CPU clock is suspended, program execution is stopped and the contents of all of the registers and the internal RAM immediately before the suspension are retained. Table 11-2 illustrates conditions of all relevant hardware blocks.

11.2.1 Release from the HALT Mode

HALT mode is released by a nonmaskable interrupt (NMI) request, unmasked maskable interrupt request and RESET input. (Fig. 11-12) It goes from HALT mode to macro-service and DMA processing using macro-service requests or DMA processing requests (Fig. 11-3). When macro-service and DMA processing are completed, it again returns to HALT mode. However, if conditions such as those illustrated in Chart 11-1 appear during macro-service and DMA processing, the HALT mode is released.

(1) Release from HALT mode through an interrupt request

(i) when a HALT mode is set during an interrupt processing routine, it is released by generating unmasked maskable interrupt requests with a priority higher than that of the interrupt under processing or the generation of nonmaskable interrupt requests.

(ii) in all other cases

The HALT mode is released by generating a nonmaskable interrupt request or by generation of unmasked maskable interrupt requests regardless of their priority.

(2) Release by RESET input

Identical to normal reset operations

Fig. 11-2 Release from HALT Mode using Interrupt Requests

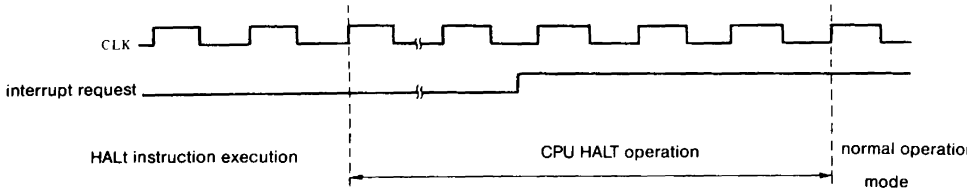


Fig. 11-3 Starting Macro-Service/DMA During HALT Mode

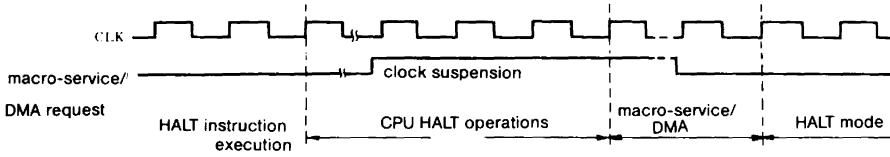


Chart 11-1 Operations after releasing HALT mode using interrupt requests

Release Source	EI Condition	DI Condition
Nonmaskable interrupt requests	branches to vector address after release	branches to vector address after release
maskable interrupt request	branches to vector address after release	executes next instruction after release
macro-service request	when macro-service is started and macro-service counter is OH, it branches to vector address. If macro-service counter does not reach OH, it goes to HALT condition a second time.	when macro-service starts and macro-service counter is OH, HALT mode is released and the next instruction is executed
DMA request	when DMA starts and terminal counter is at OH, it branches to vector address. If terminal counter does not reach OH, it goes to HALT condition a second time	when DMA starts, and terminal counter is OH, HALT mode is released and the next instruction is executed

11.3 STOP Mode

This is a mode which suspends the oscillator. It results in a very low power consumption as the complete system is suspended. Execution of STOP instruction causes it to go into STOP condition. In STOP mode, all of the clocks are suspended. Program execution is suspended and all of the register values immediately before suspension and the contents of the internal RAM are retained. Table 11-2 illustrates the condition of all hardware blocks.

11.3.1 Release from STOP Mode

STOP mode is released by using NMI request or by RESET input.

(1) Release by NMI Request (Fig. 11-4)

When the effective edge is input via the NMI pin, oscillation is restarted. The time base counter (TBC) starts operation and measures a period of several tens of milliseconds until the oscillation stabilizes.

As a result, after release from the stop mode, clocks are not immediately supplied, but the clock supply starts after the computed time of transmission stability using TBC.

(2) Release by RESET Input

Identical to normal reset operation.

Fig. 11-4 Release from STOP Mode Using NMI Input

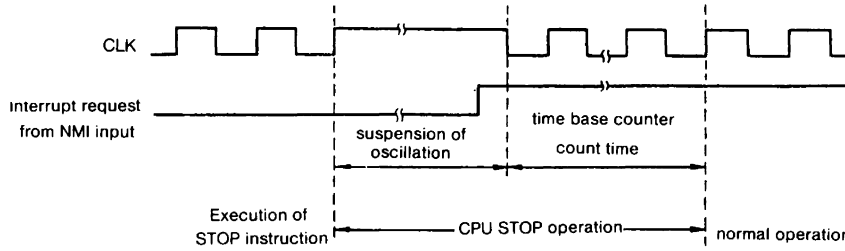


Table 11-2 HALT Mode/STOP Mode

Item		HALT Mode	STOP Mode
Oscillation		Operation	Stops
Internal System Clock		Stops	
16-Bit timer		Operation	Stops
Time base counter			
HOLD circuitry			
Serial interface			
Interrupt request controller			
DMA controller			
I/O lines		Retained	Retained
Bus lines	A0-A19	Retained	Retained
	D0-D7	High impedance	High impedance
R/W output		High level	High level
Refresh operation		Operation/Stop	Stopped
Data retention		CPU status, RAM contents and internal data are all retained	CPU status, RAM contents and internal data are all retained
Released by		○ nonmaskable interrupt ○ maskable interrupt request ○ RESET input ○ macro-service request* ○ DMA*	○ nonmaskable interrupt request ○ RESET input

* again returns to HALT mode after processing of macro service and DMA

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Test Condition	Ratings	Unit
Power Supply Voltage	VDD		−0.5 to +7.0	V
	VTH		−0.5 to VDD+0.5 ≤+7.0	V
Input Voltage	VI		−0.5 to VDD+0.5 ≤+7.0	V
Output Voltage	VO		−0.5 to VDD+0.5 ≤+7.0	V
Output Current Low	IOL	All Output Pin	4.0	mA
		All Output Pin Total	50	mA
Output Current High	IOH	All Output Pin	−2.0	mA
		All Output Pin Total	−20	mA
Operating Temperature	Topt		−40 to +85	°C
Storage Temperature	Tstg		−65 to +150	°C

Capacitance (Ta = 25°C, VDD = OV)

Parameter	Symbol	Test Condition	Min.	Typ	Max.	Unit
Input Capacitance	CI	fc = 1MHz			10	PF
Output Capacitance	CO	Unmeasured Pins			20	PF
I/O Capacitance	CIO	Returned to OV			20	PF

DC Charcteristics (Ta = −10°C to +70°C, VDD = +5.0V ± 10%)

Parameter	Symbol	Test Condition	Min.	Typ	Max.	Unit
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH1}	All except RESET P10/NMI, X1, X2	2.2		V_{DD}	V
	V_{IH2}	RESET, P10/NMI, X1, X2	0.8 V_{DD}		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output High Voltage	V_{OH}	I_{OH} = −0.4mA	V_{DD}−1.0			V
Input Current	I_I	EA, P10/NMI $0 \leqq V_I \leqq V_{DD}$			±20	μA
Input Leakage Current	I_{LI}	All Except EA, P10/NMI; $0 \leqq V_I \leqq V_{DD}$			±10	μA
Output Leakage Current	I_{LO}	$0 \leqq V_O \leqq V_{DD}$			±10	μA
VTH Supply Current	I_{TH}	$0 \leqq V_{TH} \leqq V_{DD}$		0.5	1.0	mA
VDD Supply Current	I_{DD1}	Operation Mode f_{CLKOUT} = 5MHz/8MHz		50/85	100/120	mA
	I_{DD2}	HALT Mode f_{CLKOUT} = 5MHz/8MHz		20/25	40/50	mA
	I_{DD3}	STOP Mode		10	30	μA

Comparator Characteristics (Ta = −10°C to + 70°C, BDD = +5.0V±10%)

Parameter	Symbol	Test Condition	Min.	Typ	Max.	Unit
Camparison Accuracy	V_{ACOMP}				±100	mV
Threshold Voltage	V_{TH}		0		V_{DD}+0.1	V
Comparison Time	t_{COMP}		64		65	TCYK
PT Input Voltage	V_{IPT}		0		V_{DD}	V

A.C. Characteristics (Ta = − 10°C to +70°C, VDD = +5.0V ± 10%)

Parameter	Symbol	Test Condition	Min.	Max.	Unit
Input Rise Time	t_{IR}	Except X1, X2 RESET, NMI		20	ns
Input Fall Time	t_{IF}			20	ns
Input Rise Time (SCHMITT)	t_{IRS}	RESET, NMI		30	ns
Input Fall Time (SCHMITT)	t_{IFS}			30	ns
Output Rise Time	t_{OR}	Except CLKOUT		20	ns
Output Fall Time	t_{OF}	Except CLKOUT		20	ns
X1 Input Cycle Time	t_{CYX}	f_{CLK}=5MHz/8MHz	98/62	250	ns
X1 Width Low	t_{WXL}	f_{CLK}=5MHz/8MHz	35/20		ns
X1 Width High	t_{WXH}	f_{CLK}=5MHz/8MHz	35/20		ns
X1 Rise Time	t_{XR}	f_{CLK}=5MHz/8MHz		10	ns
X1 Fall Time	t_{XF}	f_{CLK}=5MHz/8MHz		10	ns
CLKOUT Cycle Time	t_{CYK}	f_{OSC}/2	200/125	2000	ns
CLKOUT Width Low	t_{WKL}	f_{CLK}=5MHz/8MHz	0.5T−15		ns
CLKOUT Width High	t_{WKH}	f_{CLK}=5MHz/8MHz	0.5T−15		ns
CLKOUT Rise Time	t_{KR}			15	ns
CLKOUT Fall Time	t_{KF}			15	ns
Address Delay Time	t_{DKA}			90	ns
Address Valid to Input Data Valid	t_{DADR}			(n+1.5)T−120	ns
MREQ to Data Delay Time	t_{DMRD}			(n+1)T−90	ns
MSTB to Data Delay Time	t_{DMSD}			(n+0.5)T−90	ns
MREQ to MSTB Delay Time	t_{DMRMS}		0.5T−50	0.5T+50	ns
MREQ Width Low	t_{WMRL}		(n+1)T−40		ns
Address Hold Time	t_{HMA}		0.5T−50		ns
Input Data Hold Time	t_{HMDR}		0		ns
Next Control Setup Time	t_{SCC}		T−25		ns
MREQ to TC Delay Time	t_{DMRTC}			0.5T+50	ns

A. C. Characteristics (Continued)

Parameter	Symbol	Test Condition	Min.	Max.	Unit
Address to Data Output	t_{DADW}			0.5T+50	ns
$\overline{MREQ}$ Delay Time	t_{DAMR}		0.5T−50		ns
$\overline{MSTB}$ Delay Time	t_{DAMS}		T−50		ns
$\overline{MREQ}$ to MSTB Delay Time	t_{DMRMS}		0.5T−50		ns
$\overline{MSTB}$ Width Low	t_{WMSL}		(n+0.5)T−40		ns
Data Output Setup time	t_{SDM}		(n+1)T−50		ns
Data Output Hold Time	t_{HMDW}		0.5T−50		ns
$\overline{IOSTB}$ Delay Time	t_{DAIS}		0.5T−50		ns
$\overline{IOSTB}$ to Data Input	t_{DISD}			(n+1)T−120	ns
$\overline{IOSTB}$ Width Low	t_{WISL}		(n+1)T−40		ns
Address Hold Time	t_{HISA}		0.5T−50		ns
Data Input Hold Time	t_{HISDR}		0		ns
Output Data Setup Time	t_{SDIS}		(n+1)T−50		ns
Output Data Hold Time	t_{HISDW}		0.5T−50		ns
Next DMARQ Setup Time	t_{SDADQ}	Demand Mode		1T	ns
DMARQ Hold Time	t_{HDADQ}	Demand Mode	0		ns
$\overline{DMAAK}$ Read Width Low	t_{WDMRL}		(n+1.5)T−40		ns
$\overline{DMAAK}$ to TC Delay Time	t_{DDATC}			0.5T+50	ns
$\overline{TC}$ Width Low	t_{WTCL}		2T−40		ns
$\overline{DMAAK}$ Write Width Low	t_{WDMWL}		(n+1)T−40		ns
$\overline{REFRQ}$ Delay Time	t_{DARF}		0.5T−50		ns
$\overline{REFRQ}$ Width Low	t_{WRFL}		(n+1)T−40		ns
Address Hold Time	t_{HRFA}		0.5T−50		ns

A. C. Characteristics (Continued)

Parameter	Symbol	Test Condition	Min.	Max.	Unit
$\overline{\text{RESET}}$ Width Low (STOP/POR.)	t_{WRSL1}		30		ms
$\overline{\text{RESET}}$ Width Low (System Reset)	t_{WRSL2}		5		μs
MREQ, IOSTB to READY Setup Time	t_{SCRY}	$n \geq 2$		(n-1) T-100	ns
MREQ, IOSTB to READY Hold Time	t_{HCRY}	$n \geq 2$	(n-1) T		ns
HLDRQ Setup Time	t_{SHQK}		30		ns
$\overline{\text{HLDAK}}$ Output Delay Time	t_{DKHA}			80	ns
Bus Control Float to $\overline{\text{HLDAK}}\downarrow$	t_{CFHA}		1T-50		ns
$\overline{\text{HLDAK}}\uparrow$ to Control Output Time	t_{HAC}		1T-50		ns
HLDRQ to $\overline{\text{HLDAK}}$ Delay Time	t_{DHQHA}			3T+160	ns
HLDRQ↓ to Control Float	t_{DHQC}		3T+30		ns
HLDRQ Width Low	t_{WHQL}		1,5T		ns
$\overline{\text{HLDAK}}$ Width Low	t_{WHAL}		1T		ns
INTP, DMARQ Setup Time	t_{SIQK}		30		ns
INTP, DMARQ Width High	t_{WIQH}		8T		ns
INTP, DMARQ Width Low	t_{WIQL}		8T		ns
$\overline{\text{POLL}}$ Setup Time	t_{SPLK}		30		ns
NMI Width High	t_{WNIH}		5		μs
NMI width Low	t_{WNIL}		5		μs
$\overline{\text{CTS}}$ Width Low	t_{WCTL}		2T		ns
INTR Setup Time	t_{SIRK}		30		ns
$\overline{\text{INTAK}}$ Delay Time	t_{DKIA}			80	ns
INTR Hold Time	t_{HIAIQ}		0		ns
$\overline{\text{INTAK}}$ Width Low	t_{WIAL}		2T-40		ns
$\overline{\text{INTAK}}$ Width High	t_{WIAH}		1T-40	2T-130	ns
$\overline{\text{INTAK}}$ to DATA Delay Time	t_{DIAD}			0.5T	ns
$\overline{\text{INTAK}}$ to DATA Hold Time	t_{HIAD}		0		ns

A. C. Characteristics (Continued)

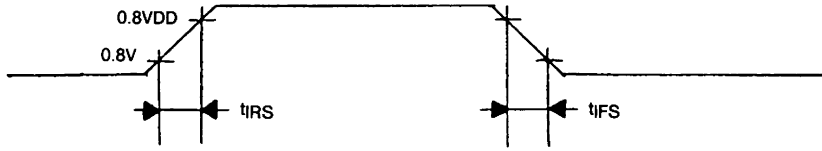
Parameter	Symbol	Test Condition	Min.	Max.	Unit
SCKO Cycle Time	tCYTK		1000		ns
SCKO (TSCK) Width High	tWSTH		450		ns
SCKO (TSCK) Width Low	tWSTL		450		ns
TXD Delay Time	tDTKD			210	ns
$\overline{CTSO}$ (RSCK) Cycle Time	tCYRK		1000		ns
$\overline{CTSO}$ (RSCK) Width High	tWSRH		420		ns
$\overline{CTSO}$ (RSCK) Width Low	tWSRL		420		ns
RXD Setup Time	tSRDK		80		ns
RXD Hold Time	tHKRD		80		ns

CL = 100 pF

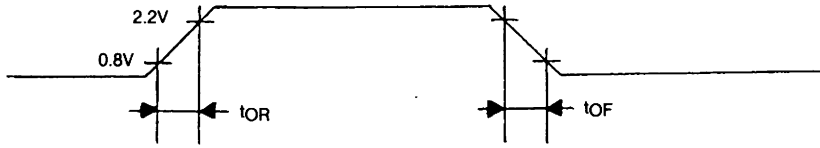
Timing Waveforms

AC Input Waveform (1) (Except X1, X2, $\overline{\text{RESET}}$, $\overline{\text{NMI}}$)

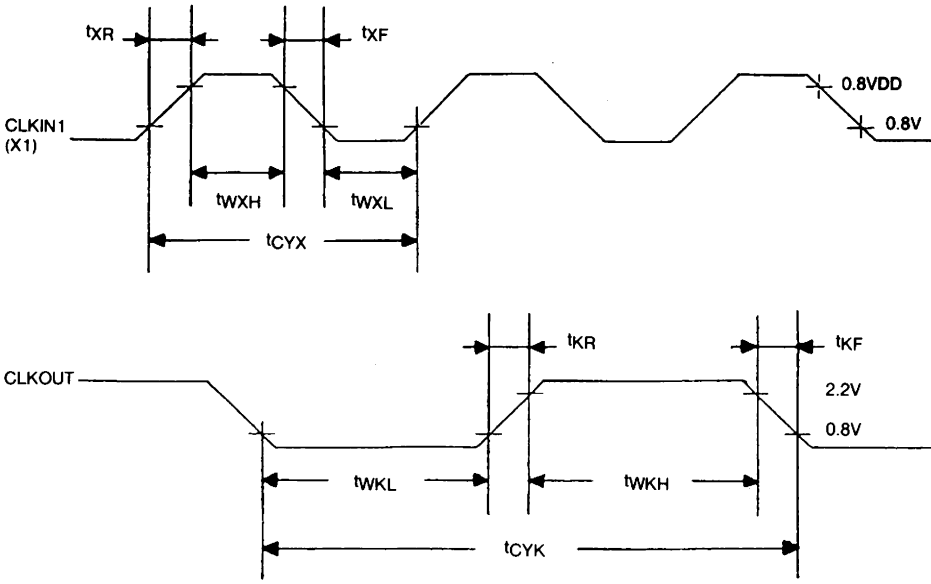
AC Input Waveform (2) ($\overline{\text{RESET}}$, $\overline{\text{NM}}$



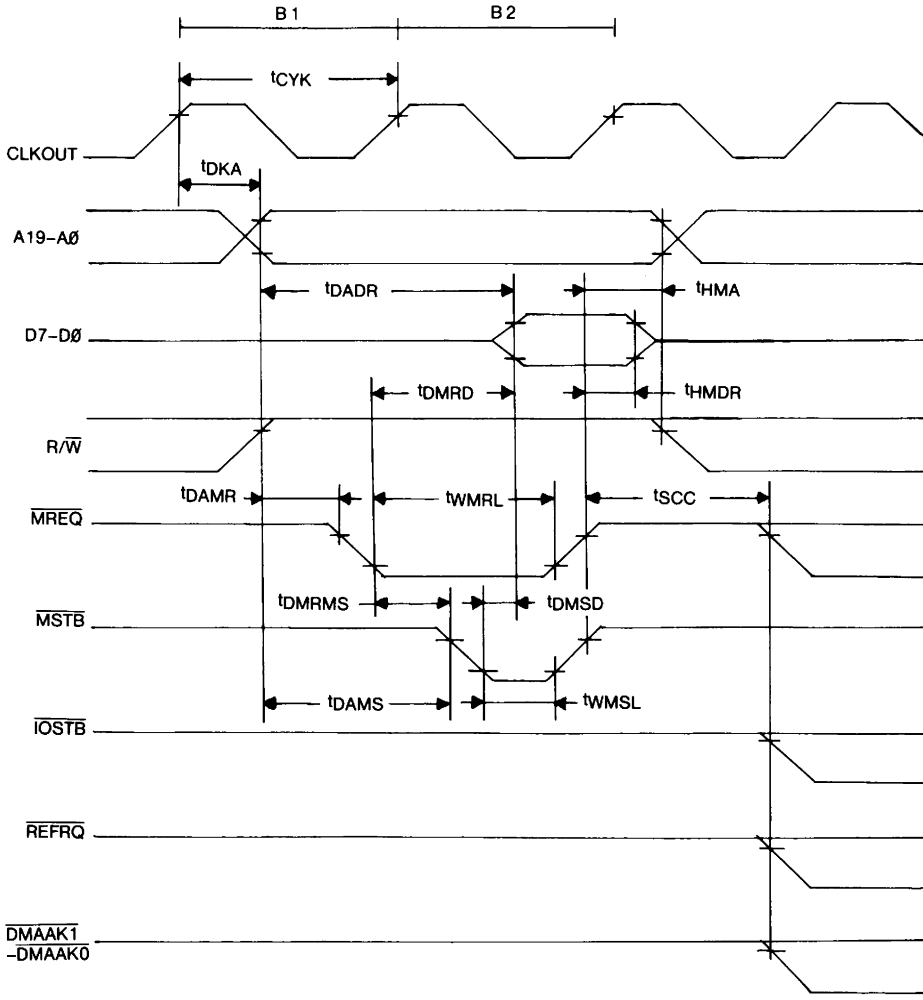
AC Output Test Point (Except CLKOUT)



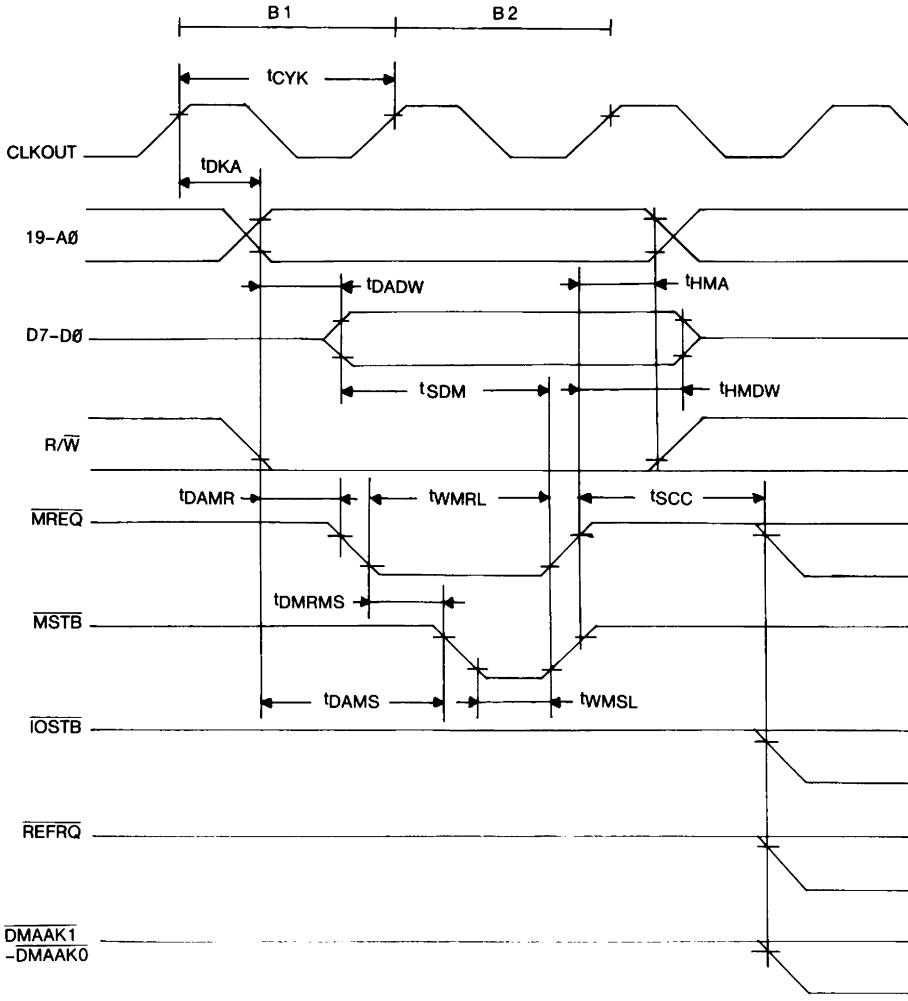
Clock Timing



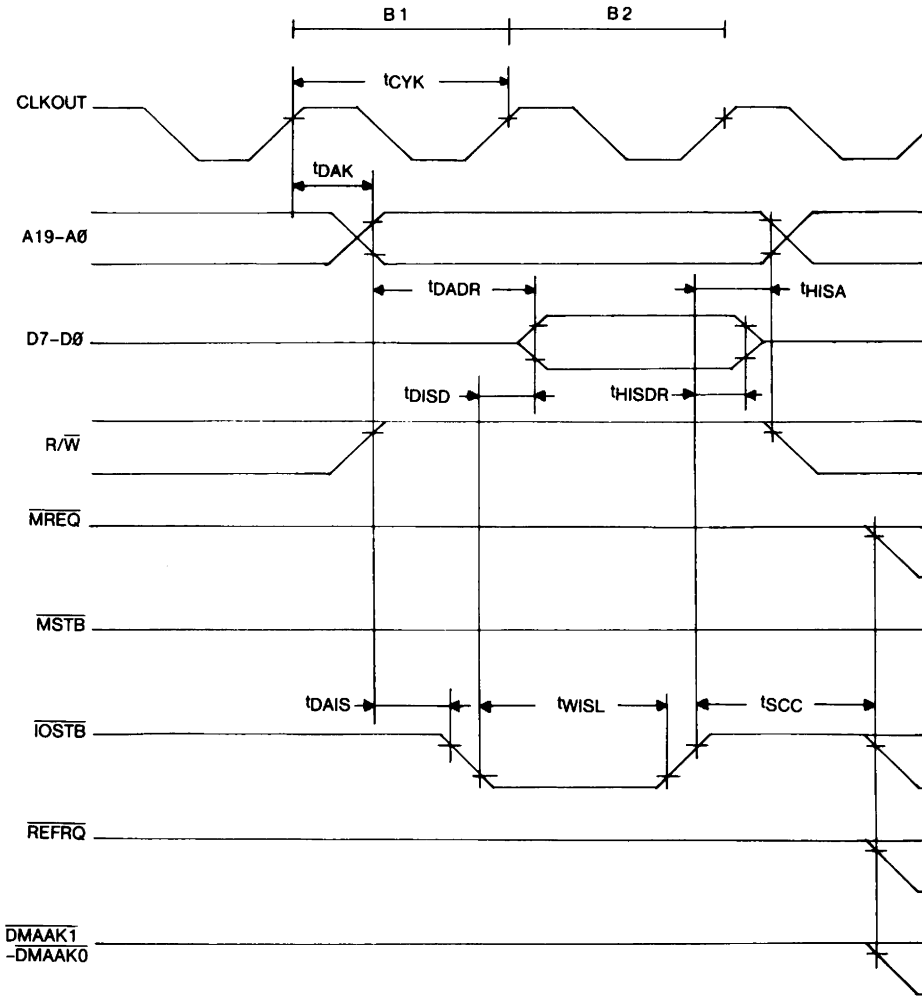
Memory Read Timing



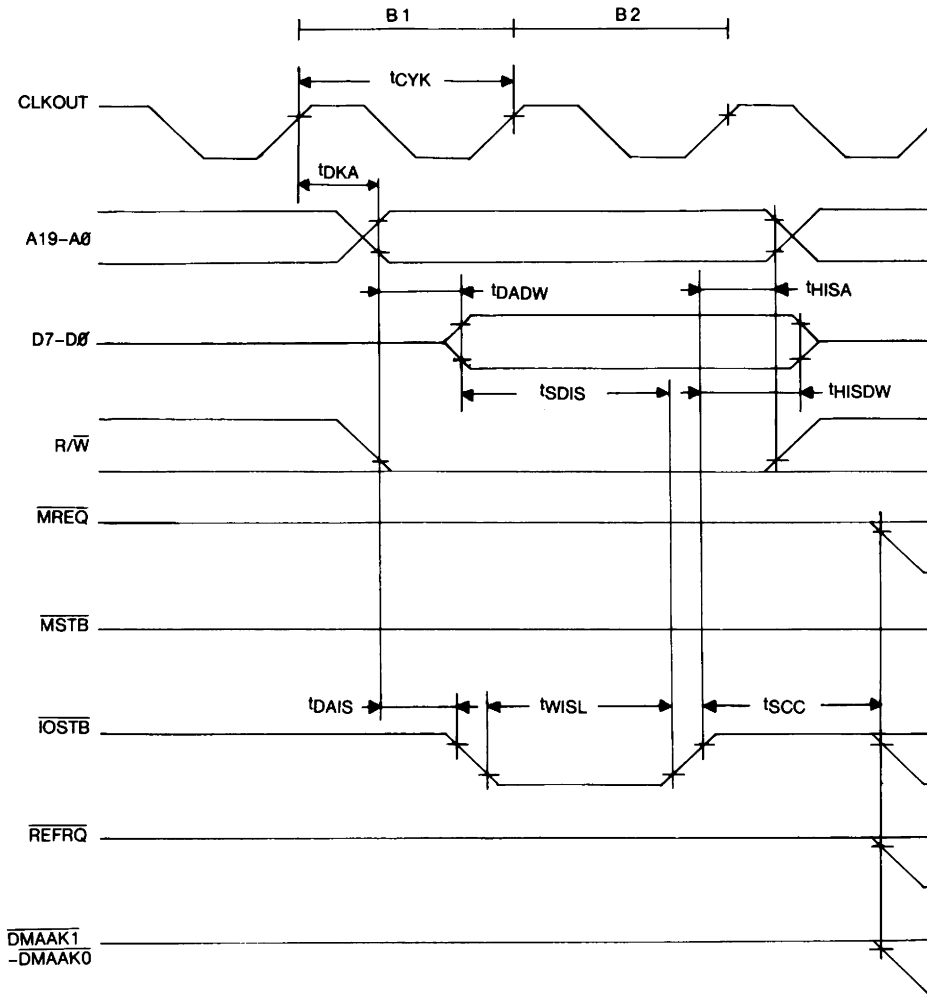
Memory Write Timing



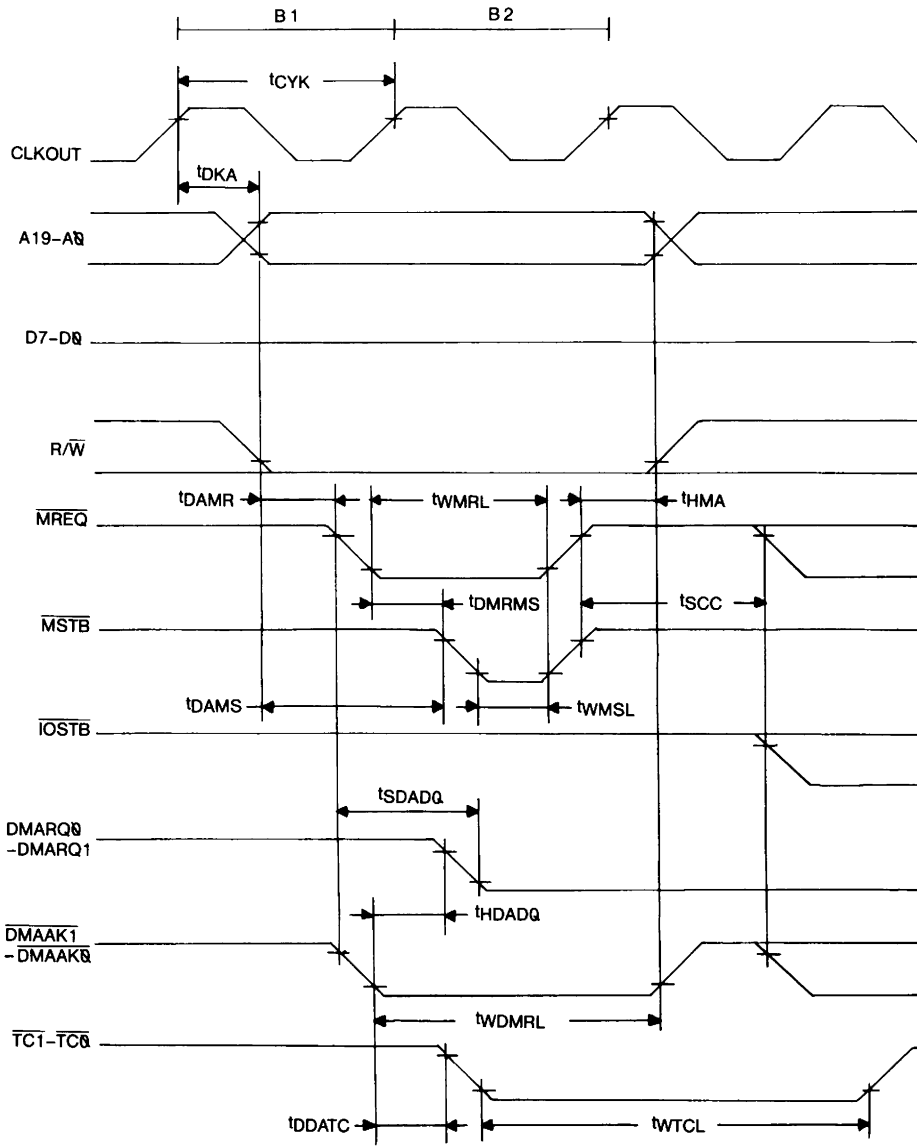
I/O Read Timing



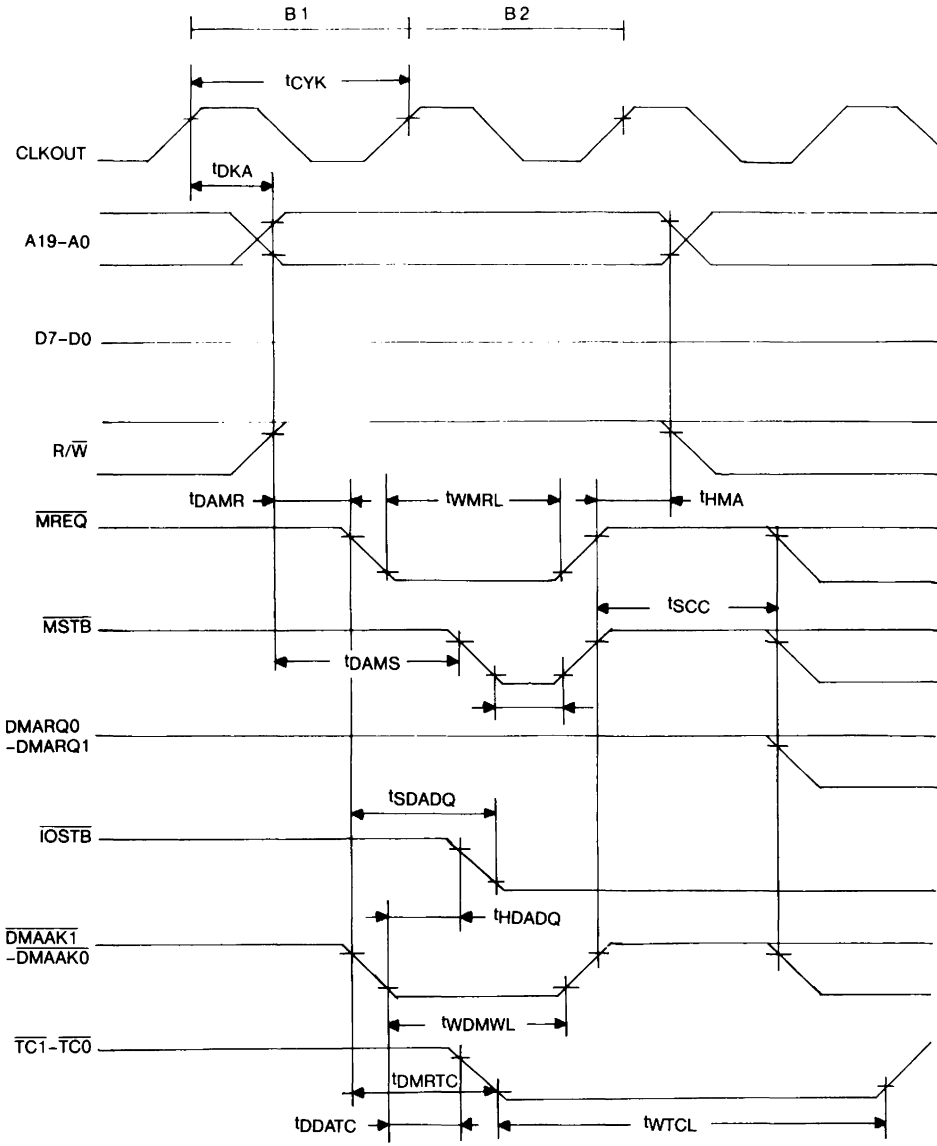
I/O Write Timing



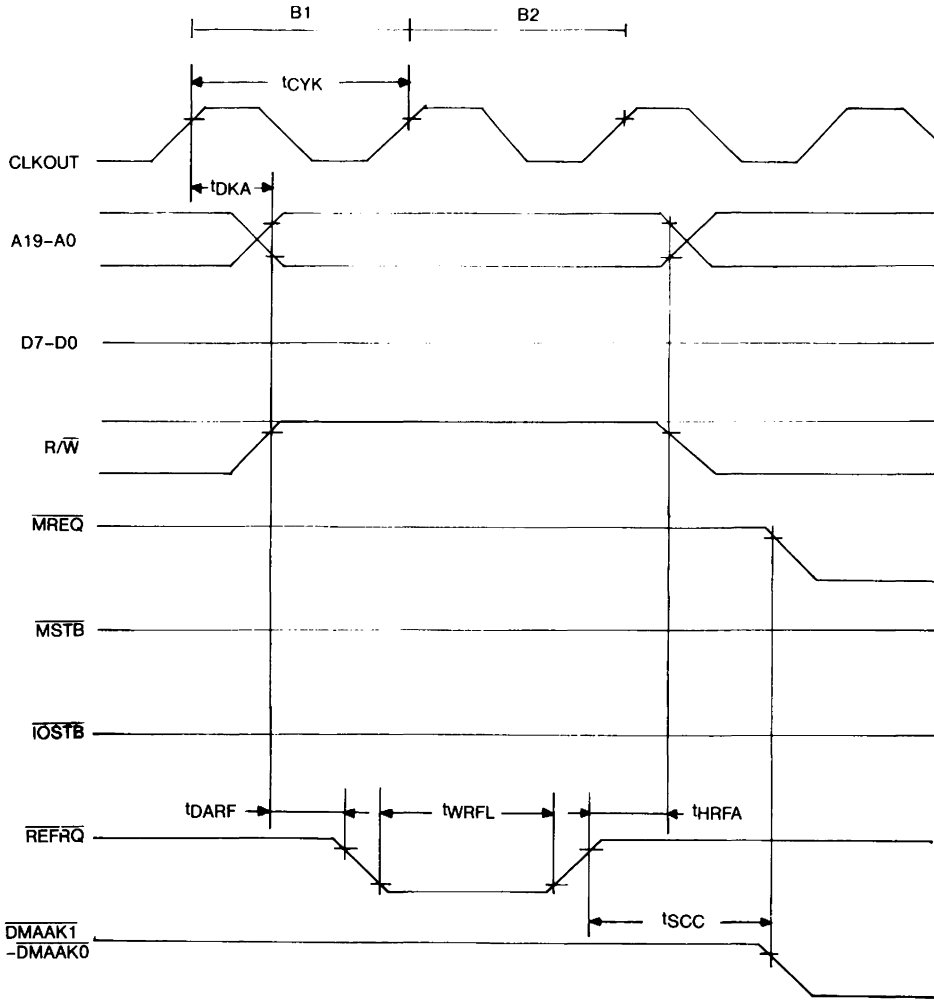
DMA(I/O→M) Timing



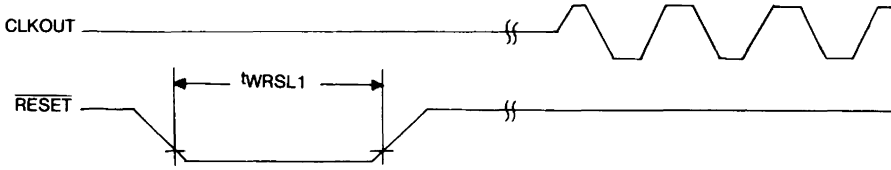
DMA(M ·I/O) Timing



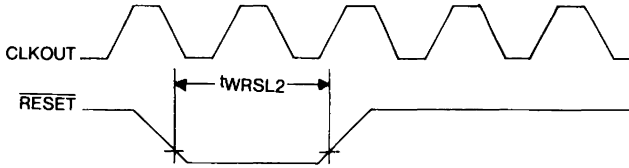
Refresh Timing



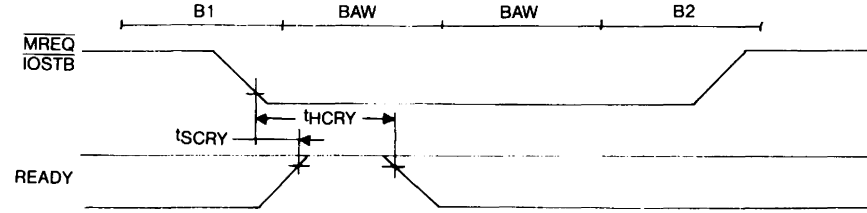
$\overline{\text{RESET}}$ Timing (1)



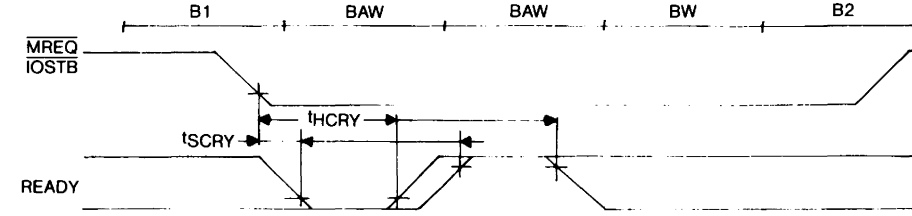
$\overline{\text{RESET}}$ Timing (2)



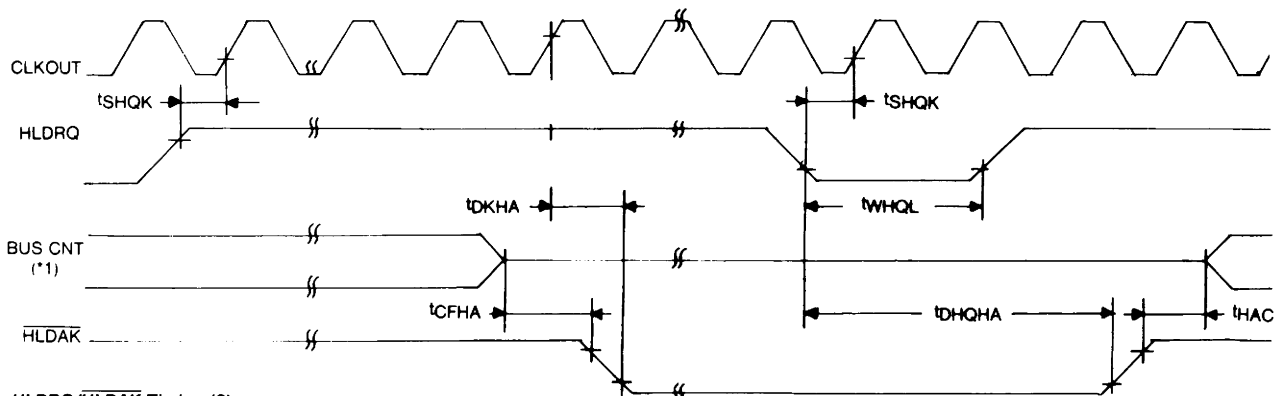
READY Timing (1)



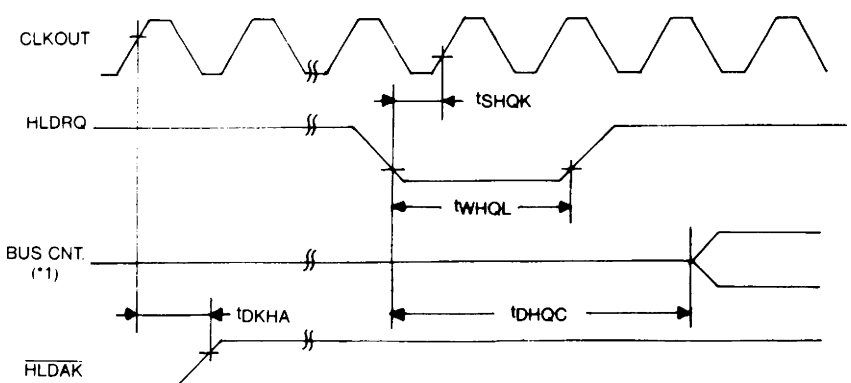
READY Timing (2)



HLDRQ/$\overline{\text{HLDAK}}$ Timing (1)



HLDRQ/$\overline{\text{HLDAK}}$ Timing (2)

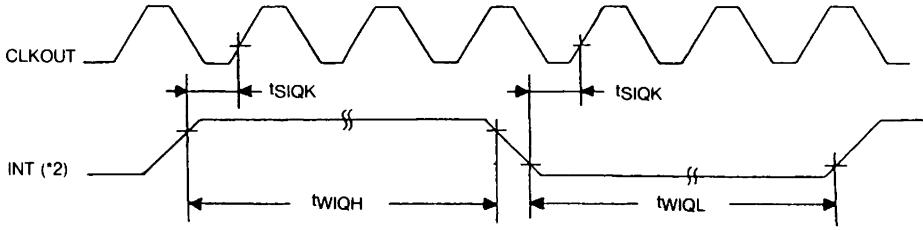


*1: A19–A0
D7–D0
$\overline{\text{MREQ}}$
$\overline{\text{MSTB}}$
$\overline{\text{IOSTB}}$
R/$\overline{\text{W}}$

NEC

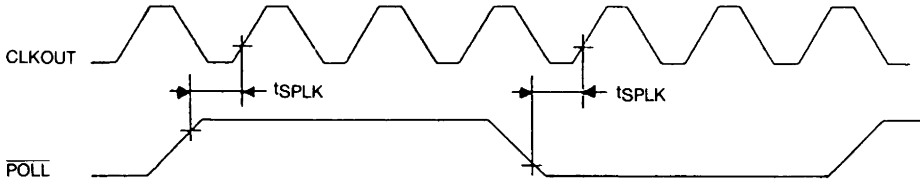
Timing Waveforms

$\overline{INTP2}$–$\overline{INTP0}$, DMARQ1–DMARQ0 Input Timing

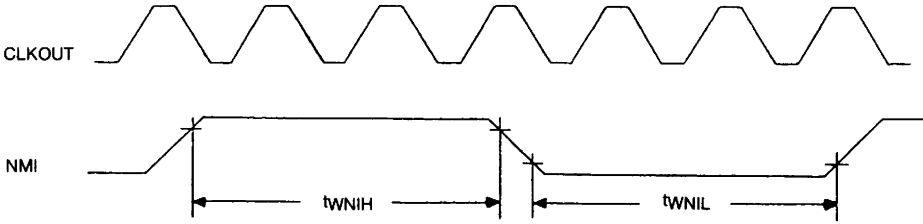


*2: $\overline{INTP2}$–$\overline{INTP0}$, DMARQ1–DMARQ0

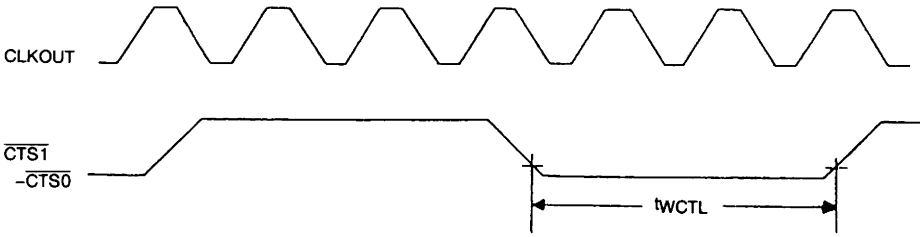
$\overline{POLL}$ Input Timing



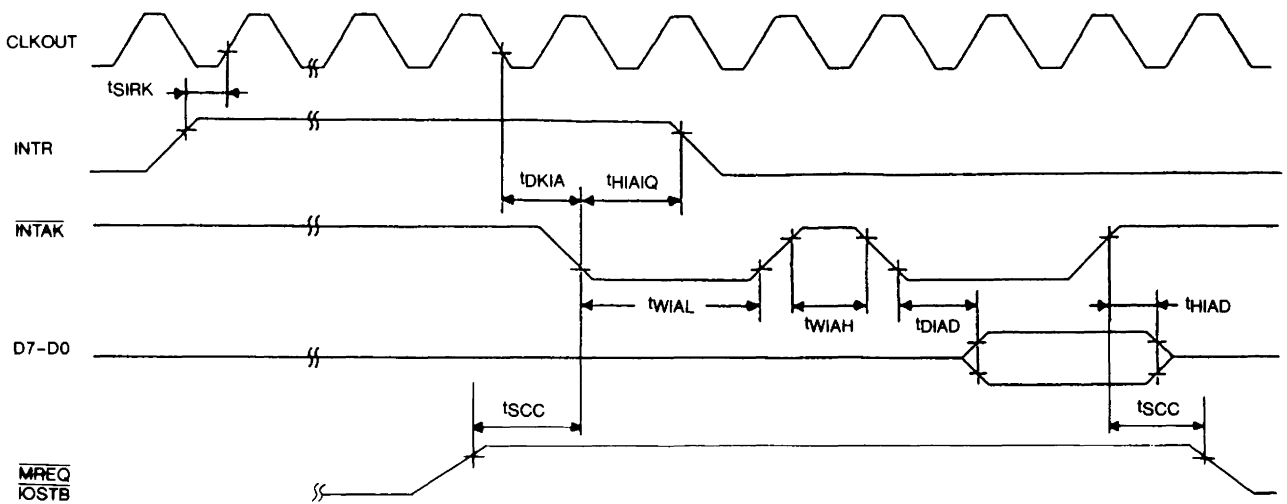
NMI Input Timing



$\overline{CTS1}$–$\overline{CTS0}$ Input Timing

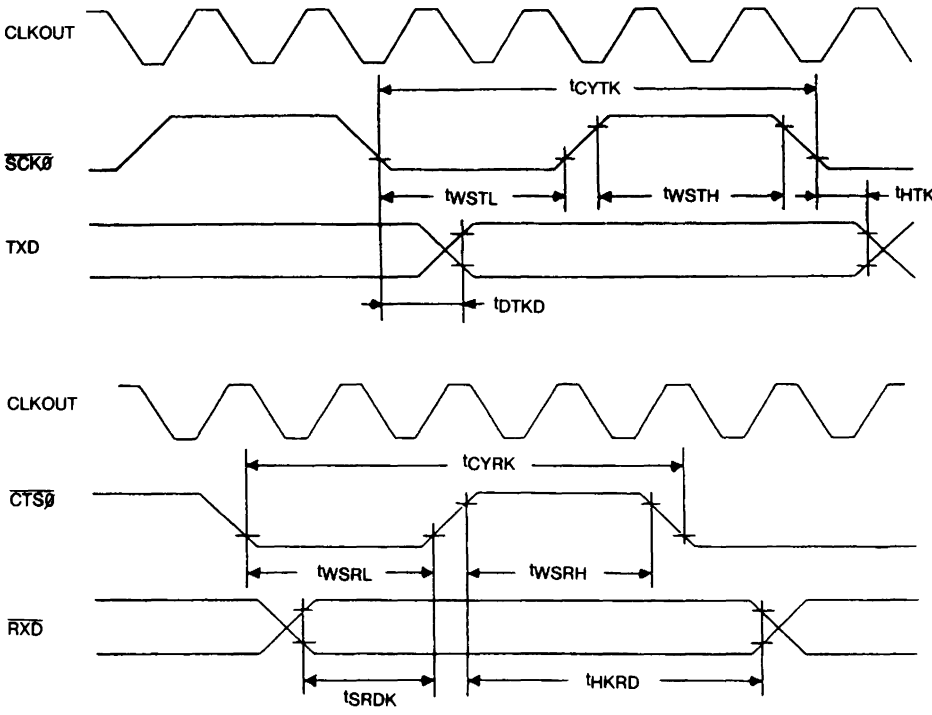


INTR/$\overline{\text{INTAK}}$ Timing



Timing Waveforms

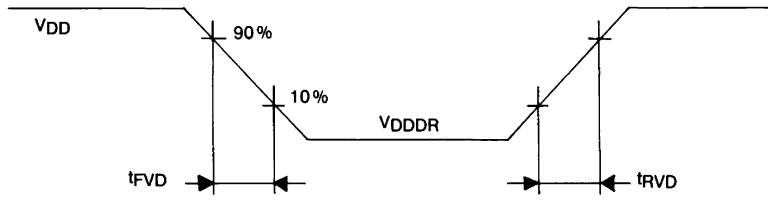
SIO Timing



Stop Mode Data Retaintion Characteristics
(Ta = −10°C to +70°C)

Parameter	Symbol	Test Condition	Min.	Max.	Unit
Data Retaintion Voltage	V_{DDDR}		2.5	5.5	V
V_{DD} Rise Time V_{DD} Fall Time	t_{RVD} t_{FVD}		200		μS

Stop Mode Data Retaintion Timing



APPENDIX

New Mask Versions from Mask E onwards have a new vector table against old mask versions (K).

OLD VECTOR TABLE	VECTOR NO. DEC	VECTOR NO. HEX	NEW VECTOR TABLE	MEANING OF SYMBOL
DIVIDE ERROR	0	00	DIVIDE ERROR	
SINGLE STEP	1	01	SINGLE STEP	
NMI	2	02	NMI	(NON MASKABLE INTERRUPT)
BRK	3	03	BRK	(BRK3 INSTRUCTION)
BRKV	4	04	BRKV	(BRKV INSTRUCTION)
CHKIND	5	05	CHKIND	(CHKIND INSTRUCTION)
–	6	06	–	
FPO	7	07	FPO	(FLOATING POINT OPERATION INSTR.)
–	8	08	–	
–	9	09	–	
–	10	0A	–	
–	11	0B	–	
	12	0C	INTSERO	(INTERRUPT FROM SERIAL ERROR OF CHANNEL 0)
–	13	OD	INTSTRO	(INTERRUPT FROM SERIAL RECEIVER OF CHANNEL 0)
–	14	OE	INTSTO	(INTERRUPT FROM SERIAL TRANSMITTER OF CHANNEL 0)
–	15	OF	–	
	16	10	INTSER1	(INTERRUPT FROM SERIAL ERROR OF CHANNEL 1)
–	17	11	INTSR1	(INTERRUPT FROM SERIAL RECEIVER OF CHANNEL 1)
–	18	12	INTST1	(INTERRUPT FROM SERIAL TRANSMITTER OF CHANNEL1)
–	19	13	I/O	(I/O INSTRUCTIONS)
I/O	20	14	INTD0	(INTERRUPT FROM DMA CHANNEL 0)
	21	15	INTD1	(INTERRUPT FROM DMA CHANNEL 1)
–	22	16	–	
–	23	17	–	
–	24	18	INTP0	(INTERRUPT FROM PERIPHERAL 0)
–	25	19	INTP1	(INTERRUPT FROM PERIPHERAL 1)
–	26	1A	INTP2	(INTERRUPT FROM PERIPHERAL 2)
–	27	1B	–	
INTSERO	28	1C	INTTU0	(INTERRUPT FROM TIMER UNIT 0)
INTSRO	29	1D	INTTU1	(INTERRUPT FROM TIMER UNIT 1)
INTSTO	30	1E	INTTU2	(INTERRUPT FROM TIMER UNIT 2)
–	31	1F	INTTB	(INTERRUPT FROM TIMER BASE COUNTER)
INTSER1	32	20		
INTSR1	33	21		
INTST1	34	22		
–	35	23		
INTDO	36	24		
INTD1	37	25		
–	38	26		
–	39	27		
INTPO	40	28		
INTP1	41	29		
INTP2	42	2A		
–	43	2B		
INTTUO	44	2C		
INTTU1	45	2D		
INTTU2	46	2E		
INTTB	47	2F		

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