MEMORY PRODUCTS

DATA BOOK

Fall 1995

Dynamic

RAM

Modules

NEC

DYNAMIC RAM MODULES DATA BOOK

FALL 1995

NEC

Dynamic RAM Module

Fall 1995 Data Book

Document No. M10584EJ1V0DBU1

Printed in the United States of America.

Index

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

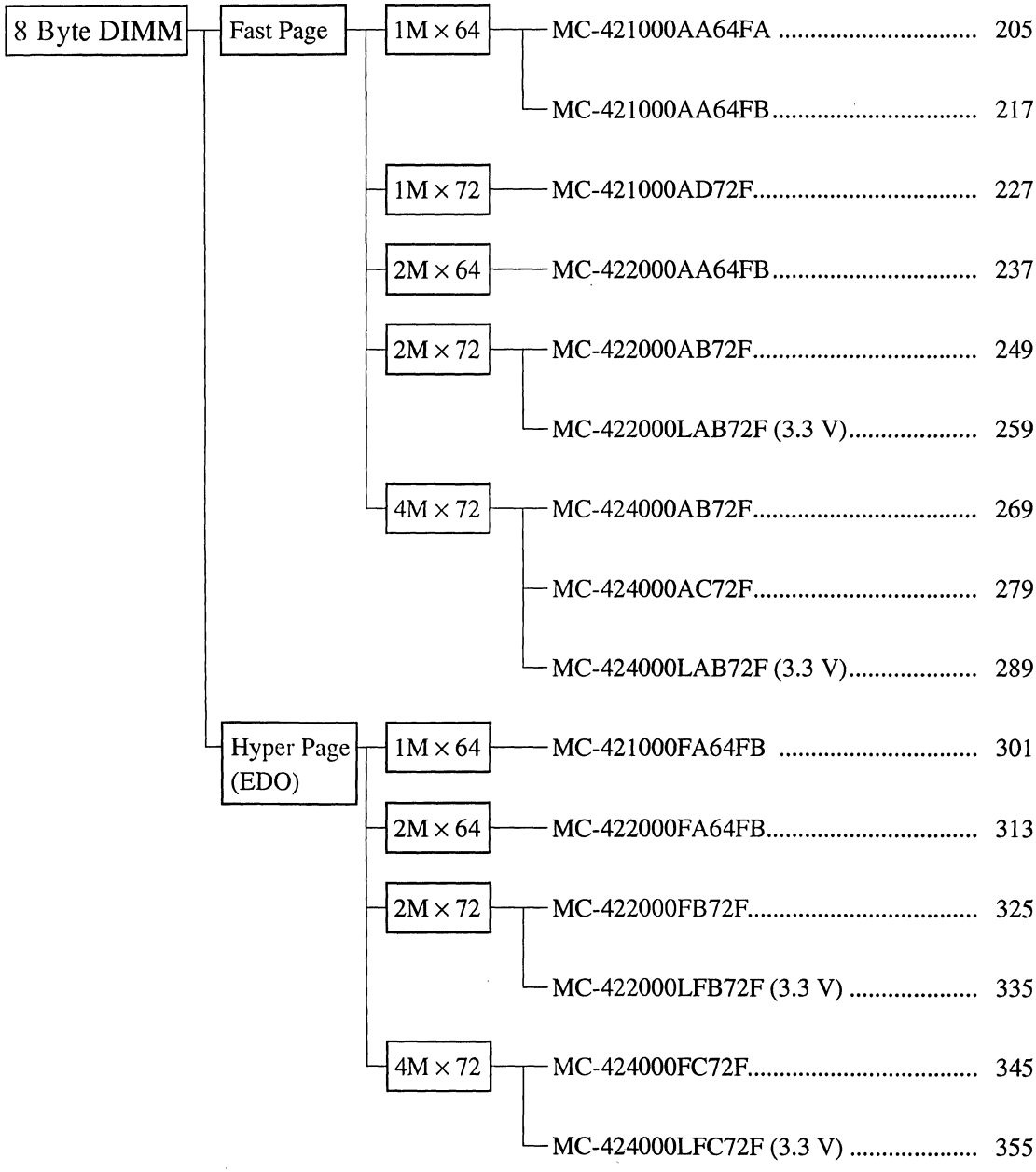
② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

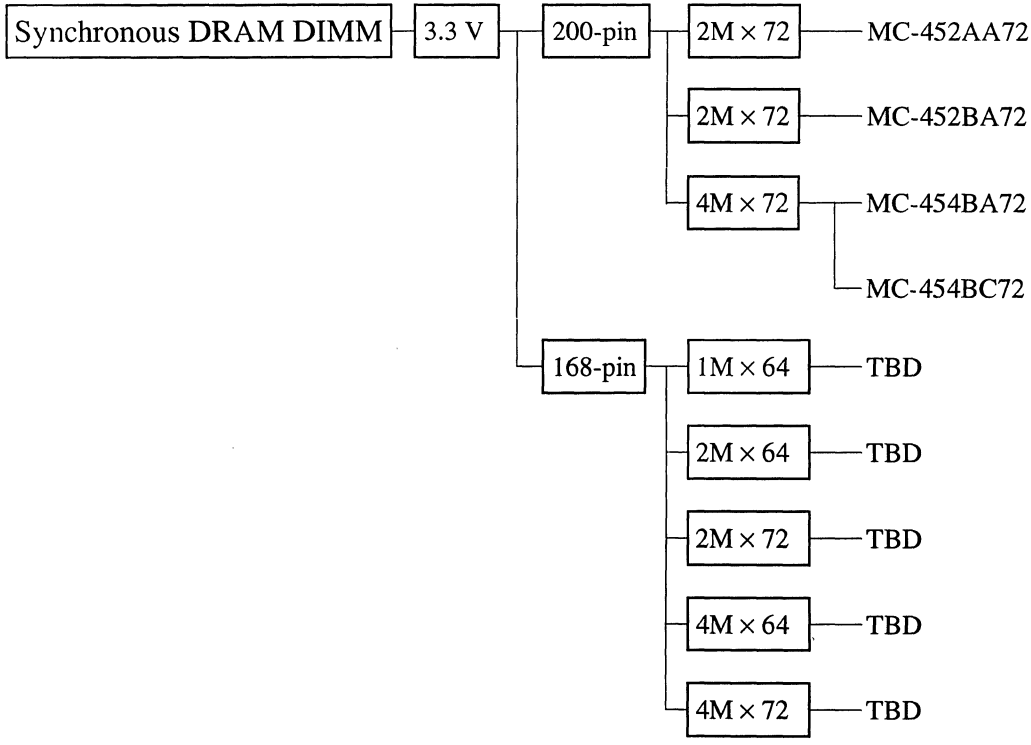
③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Contents



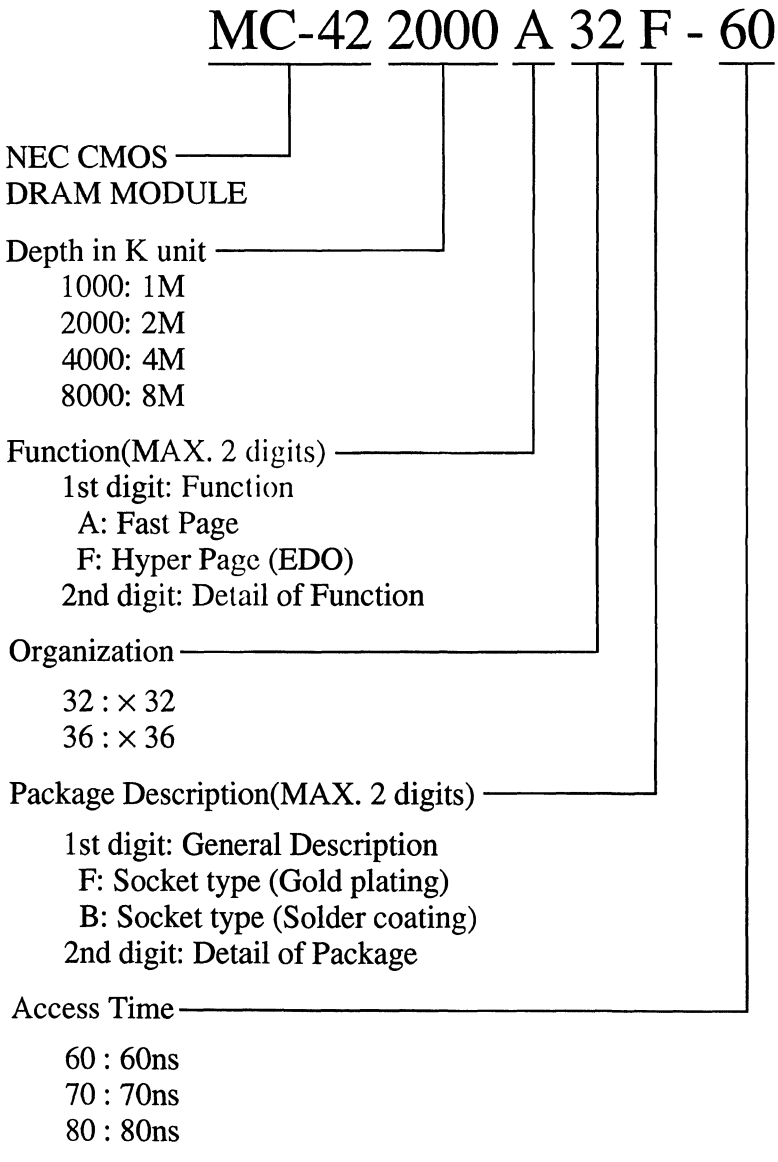
Synchronous DRAM DIMM.....TBD



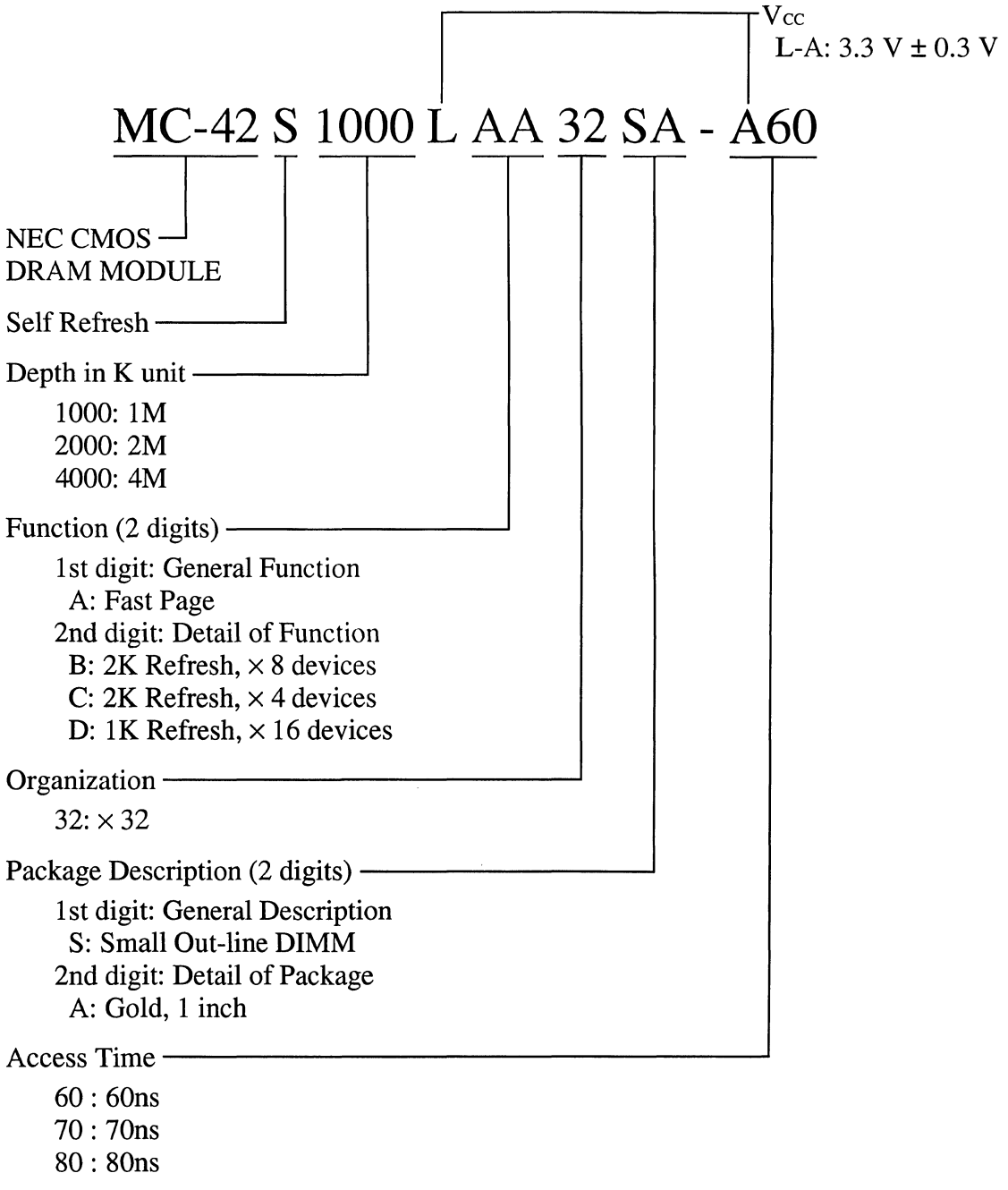
Selection Guide

Part Number

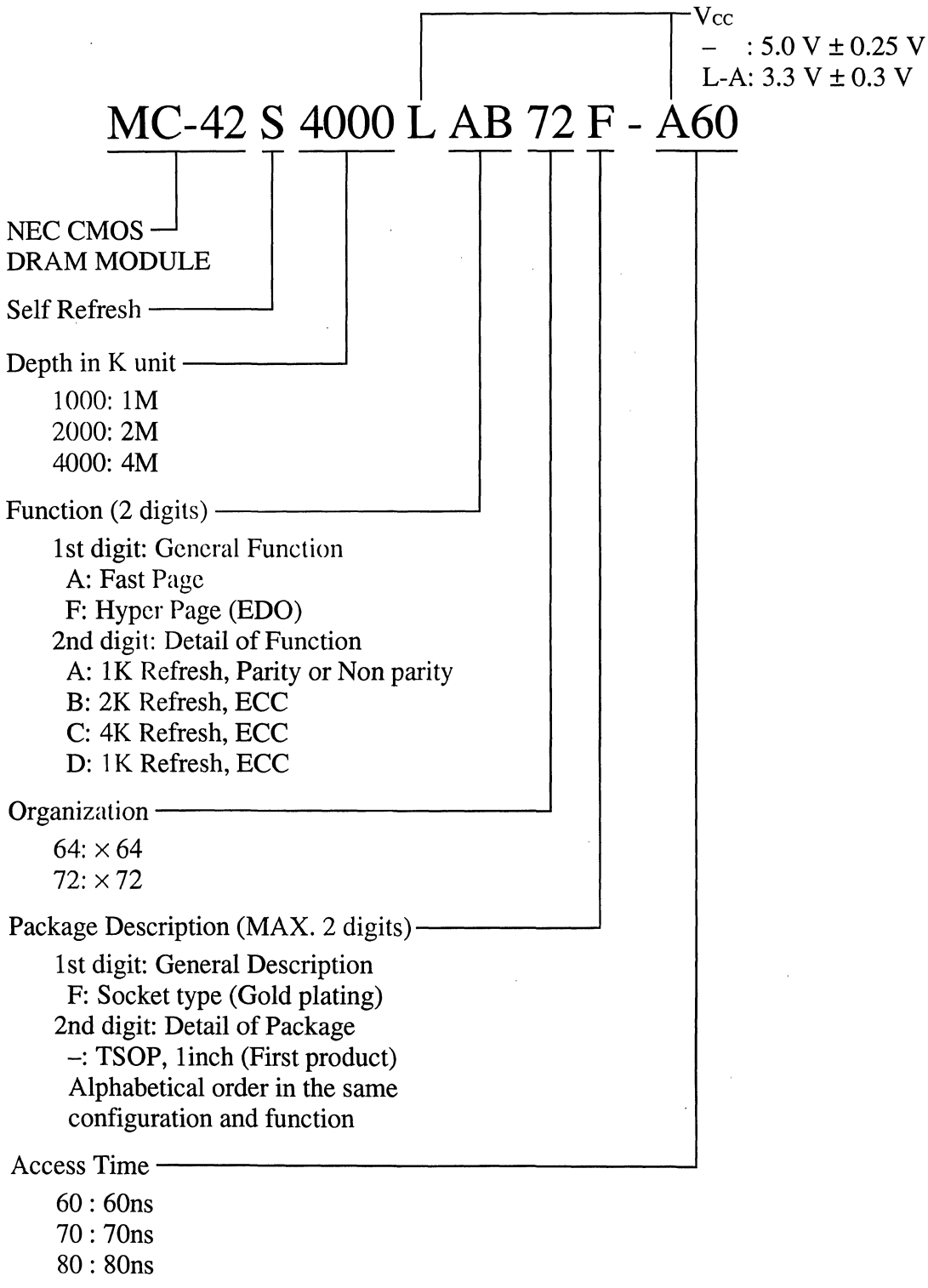
72-pin SIMM



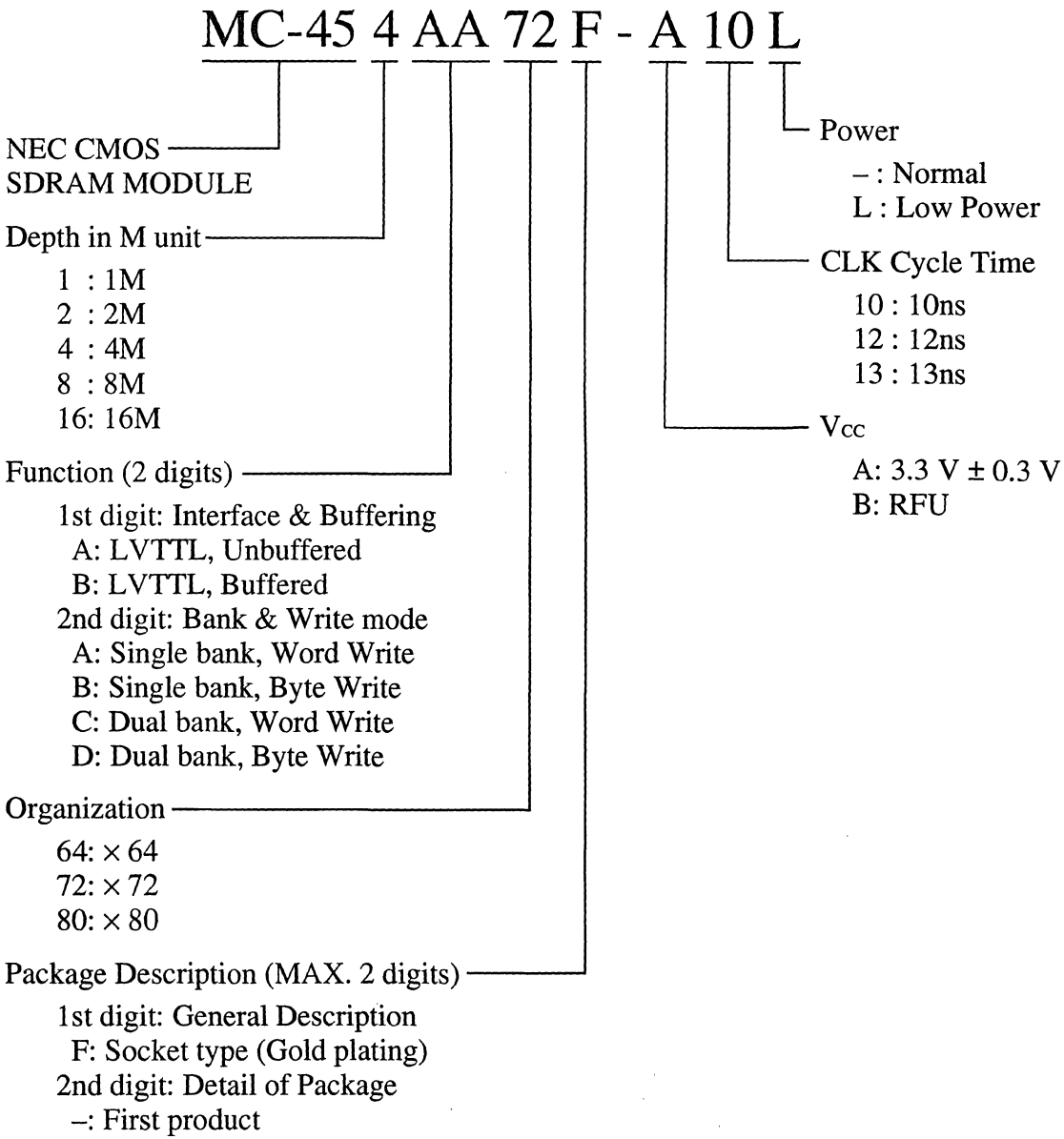
72-pin SO DIMM



168-pin 8 Byte DIMM



200-pin 8 Byte SDRAM DIMM



72-pin SIMM Fast Page Line-up (× 32)

Organization	Part Number	Access Time (ns)	Refresh Cycle	Supply Voltage	Package			Monolithic Device			Remark
					Mounted side	Edge connector	Height	Org.	Pkg.	Amt.	
1M × 32	MC-421000A32B	60, 70, 80, 100	1 K/16 ms	5.0 ± 0.5 V	Single side	S/C	1 inch	1M × 4	300 mil SOJ	8	
	MC-421000A32F					G/P					
	MC-421000A32BA	60, 70, 80			Single side	S/C		1M × 16	400 mil SOJ	2	
	MC-421000A32FA					G/P					
2M × 32	MC-422000A32B	60, 70, 80 100			Double side	S/C		1M × 4	300 mil SOJ	16	
	MC-422000A32F					G/P					
	MC-422000A32BA	60, 70, 80			Double side	S/C		1M × 16	400 mil SOJ	4	
	MC-422000A32FA					G/P					
4M × 32	MC-424000A32B	60, 70, 80	2 K/32 ms		Single side	S/C		4M × 4	300 mil SOJ	8	
	MC-424000A32F					G/P					
8M × 32	MC-428000A32B	60, 70, 80			Double side	S/C		4M × 4	300 mil SOJ	16	
	MC-428000A32F					G/P					

S/C: Solder Coated, G/P: Gold Plated

72-pin SIMM Fast Page Line-up (× 36)

Organization	Part Number	Access Time (ns)	Refresh Cycle	Supply Voltage	Package			Monolithic Device			Remark
					Mounted side	Edge connector	Height (inch)	Org.	Pkg.	Amt.	
1M × 36		70, 80, 100	1K/16 ms	5.0 ± 0.5 V							
	MC-421000A36BJ				Single side	S/C	1.25	1M × 4 1M × 1	300 mil SOJ 300 mil SOJ	8 4	
	MC-421000A36FJ					G/P					
	MC-421000A36BE				Double side	S/C	1.0	1M × 4 1M × 1	300 mil SOJ 300 mil SOJ	8 4	
	MC-421000A36FE					G/P					
2M × 36		70, 80, 100									
	MC-422000A36BJ				Double side	S/C	1.25	1M × 4 1M × 1	300 mil SOJ 300 mil SOJ	16 8	
	MC-422000A36FJ					G/P					
4M × 36	MC-424000A36BJ	60, 70, 80	2K/32 ms		Single side	S/C	1.25	4M × 4 4M × 1	300 mil SOJ 300 mil SOJ	8 4	
	MC-424000A36FJ					G/P					
	MC-424000A36BE				Double side	S/C	1.0	4M × 4 4M × 1	300mil SOJ 300mil SOJ	8 4	
	MC-424000A36FE					G/P					
8M × 36	MC-428000A36BJ	60, 70, 80			Double side	S/C	1.25	4M × 4 4M × 1	300 mil SOJ 300 mil SOJ	16 8	
	MC-428000A36FJ					G/P					

S/C: Solder Coated, G/P: Gold Plated

72-pin SIMM Hyper Page (EDO) Line-up

Organization	Part Number	Access Time (ns)	Refresh Cycle	Supply Voltage	Package			Monolithic Device			Remark
					Mounted side	Edge connector	Height	Org.	Pkg.	Amt.	
1M × 32	MC-421000F32BA	60, 70	1 K/16 ms	5.0 ± 0.5 V	Single side	S/C	1 inch	1M × 16	400 mil SOJ	2	
	MC-421000F32FA					G/P					
2M × 32	MC-422000F32BA	60, 70			Double side	S/C		1M × 16	400 mil SOJ	4	
	MC-422000F32FA					G/P					
4M × 32	MC-424000A32B	60, 70	2 K/32 ms		Single side	S/C		4M × 4	300 mil SOJ	8	
	MC-424000A32F					G/P					
8M × 32	MC-428000A32B	60, 70			Double side	S/C		4M × 4	300 mil SOJ	16	
	MC-428000A32F					G/P					

S/C: Solder Coated, G/P: Gold Plated

72-pin Small Outline DIMM Line-up

Organization	Part Number	Access Time (ns)	Supply Voltage	Refresh Cycle	Bank org.	Package	Monolithic Device			Remark
							Org.	Pkg.	Amt.	
1M × 32	MC-42S1000LAD32SA	60, 70, 80	3.3 ± 0.3 V	1 K/128 ms	1	72-pin SOD Gold plated	1M × 16	400 mil TSOP	2	
2M × 32	MC-42S2000LAB32SA	60, 70, 80		2 K/128 ms	1		2M × 8	400 mil TSOP	4	
	MC-42S2000LAD32SA			1 K/128 ms	2		1M × 16	400 mil TSOP	4	
4M × 32	MC-42S4000LAB32SA	60, 70, 80		2 K/128 ms	2		2M × 8	400 mil TSOP	8	
	MC-42S4000LAC32SA				1		4M × 4	300 mil TSOP	8	

168-pin 8 Byte DIMM Fast Page Line-up

Organization	Part Number	Access Time (ns)	Refresh Cyc'e	Supply Voltage	Package		Monolithic Device			Remark
					Edge connector	Height	Org.	Pkg.	Amt.	
1M × 64	MC-421000AA64FA	60, 70, 80	1 K/16 ms	5.0 ± 0.25 V	Gold plated	1 inch	1M × 4	300 mil SOJ	16	
	MC-421000AA64FB	60, 70, 80					1M × 16	400 mil SOJ	4	
2M × 64	MC-422000AA64FB	60, 70, 80					1M × 16	400 mil SOJ	8	
1M × 72 ECC	MC-421000AD72F	60, 70, 80					1M × 16 1M × 4	400 mil TSOP 300 mil TSOP	4 2	
2M × 72 ECC	MC-422000AB72F	60, 70, 80	2 K/32 ms				2M × 8	400 mil TSOP	9	
	MC-422000LAB72F	60, 70, 80		3.3 ± 0.3 V			2M × 8	400 mil TSOP	9	
4M × 72 ECC	MC-424000AB72F	60, 70, 80		5.0 ± 0.25 V			4M × 4	300 mil TSOP	18	
	MC-424000LAB72F	60, 70, 80		3.3 ± 0.3 V			4M × 4	300 mil TSOP	18	
	MC-424000AC72F	60, 70, 80	4 K/64 ms	5.0 ± 0.25 V			4M × 4	300 mil TSOP	18	

168-pin 8 Byte DIMM Hyper Page (EDO) Line-up

Organization	Part Number	Access Time (ns)	Refresh Cycle	Supply Voltage	Package			Monolithic Device			Remark
					Mounted side	Edge connector	Height	Org.	Pkg.	Amt.	
1M × 64	MC-421000FA64FB	60, 70	1 K/16 ms	5.0 ± 0.5 V	Single side	Gold plated	1 inch	1M × 16	400 mil SOJ	2	
2M × 64	MC-422000FA64FB	60, 70			Double side			1M × 16	400 mil SOJ	4	
2M × 72	MC-422000FB72F	60, 70	2 K/32 ms	5.0 ± 0.5 V	Double side			2M × 8	400 mil TSOP	9	
	MC-422000LFB72F			3.3 ± 0.3 V							
4M × 72	MC-424000FC72F	60, 70	4 K/64 ms	5.0 ± 0.5 V	Double side			4M × 4	300 mil TSOP	18	
	MC-424000LFC72F			3.3 ± 0.3 V							

200-pin SDRAM DIMM Line-up

	Organization	Part Number	Bank Org.	Min.Cycle time (ns)	Supply Voltage	Package		Monolithic Device		Remark
						Edge connector	Height	Org.	Amt.	
Unbuffered	2M × 72	MC-452AA72F	Single	10 (100 MHz) 12 (83 MHz) 13 (77 MHz)	3.3 ± 0.3 V	Gold plated	29.2 mm	2M × 8	9	TBD
Buffered	2M × 72	MC-452BA72F	Single				38.1 mm	2M × 8	9	TBD
	4M × 72	MC-454BA72F	Single					4M × 4	18	TBD
		MC-454BC72F	Dual					2M × 8	18	TBD

4 Byte SIMM
[Fast Page]

NEC

MOS INTEGRATED CIRCUIT

MC-421000A32BA, 421000A32FA

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000A32BA, 421000A32FA are 1,048,576 words by 32 bits dynamic RAM module on which 2 pieces of 16 M DRAM: μPD4218160 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000A32-60	60 ns	110 ns	1,760 mW	11 mW (CMOS level input)
MC-421000A32-70	70 ns	130 ns	1,650 mW	
MC-421000A32-80	80 ns	150 ns	1,540 mW	

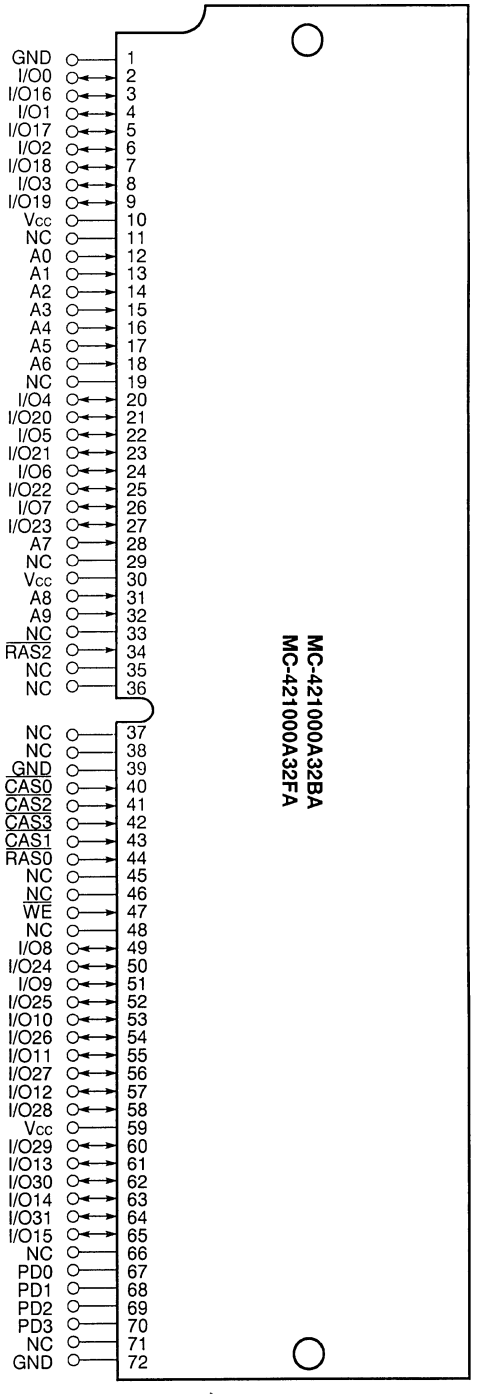
- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A32BA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	2 pieces of μPD4218160LE (400 mil SOJ) [Single side]
MC-421000A32BA-70	70 ns		
MC-421000A32BA-80	80 ns		
MC-421000A32FA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000A32FA-70	70 ns		
MC-421000A32FA-80	80 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



A0 - A9	:	Address Inputs
I/O0 - I/O31	:	Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	:	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	:	Row Address Strobe
$\overline{WE}$	:	Write Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	GND	GND	GND
PD1	68	GND	GND	GND
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

Block Diagram

Remark D0, D1: μPD4218160

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		2	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			30	pF
	C_{I2}	$\overline{WE}$			34	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			22	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			22	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		320	mA	3, 4, 7
			t_{RAC} = 70 ns		300		
			t_{RAC} = 80 ns		280		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		4	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		2		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		320	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		300		
			t_{RAC} = 80 ns		280		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		180	mA	3, 4, 6
			t_{RAC} = 70 ns		160		
			t_{RAC} = 80 ns		140		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		320	mA	3, 4
			t_{RAC} = 70 ns		300		
			t_{RAC} = 80 ns		280		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

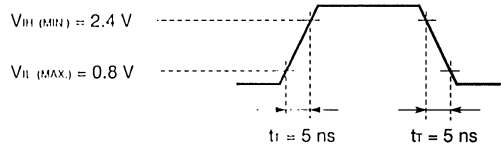
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		16		16		16	ms	

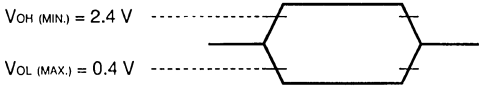
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

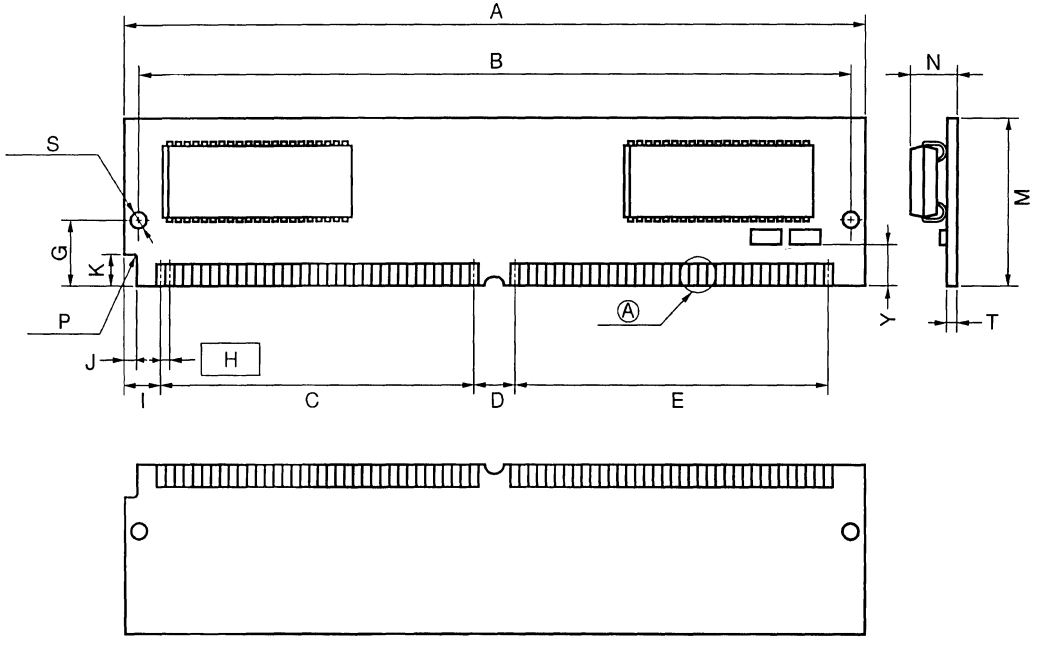
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{OFF\ (MAX.)}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}$/$\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

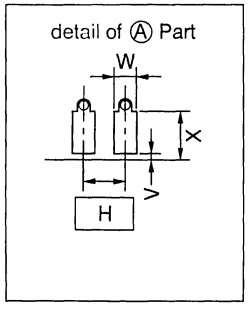
Timing Chart

Please refer to Timing Chart 1, page 365.

Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.

M72B-50A46

NEC

MOS INTEGRATED CIRCUIT

MC-421000A32, 421000A36 SERIES

1 M-WORD BY 32-BIT, 1 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000A32 series is a 1,048,576 words by 32 bits dynamic RAM module on which 8 pieces of 4 M DRAM: μPD424400 are assembled.

The MC-421000A36 series is a 1,048,576 words by 36 bits dynamic RAM module on which 8 pieces of 4 M DRAM: μPD424400 and 4 pieces of 1 M DRAM: μPD421000 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 32 bits organization (MC-421000A32 series)
- 1,048,576 words by 36 bits organization (MC-421000A36 series)
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000A32-60	60 ns	120 ns	5,280 mW	44 mW (CMOS level input)
MC-421000A32-70	70 ns	140 ns	4,400 mW	
MC-421000A32-80	80 ns	160 ns	3,960 mW	
MC-421000A32-10	100 ns	190 ns	3,520 mW	
MC-421000A36-70	70 ns	140 ns	6,160 mW	66 mW (CMOS level input)
MC-421000A36-80	80 ns	160 ns	5,500 mW	
MC-421000A36-10	100 ns	190 ns	4,840 mW	

- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

[MC-421000A32 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μPD424400LA (300 mil SOJ) [Single side]
MC-421000A32B-70	70 ns		
MC-421000A32B-80	80 ns		
MC-421000A32B-10	100 ns		
MC-421000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000A32F-70	70 ns		
MC-421000A32F-80	80 ns		
MC-421000A32F-10	100 ns		

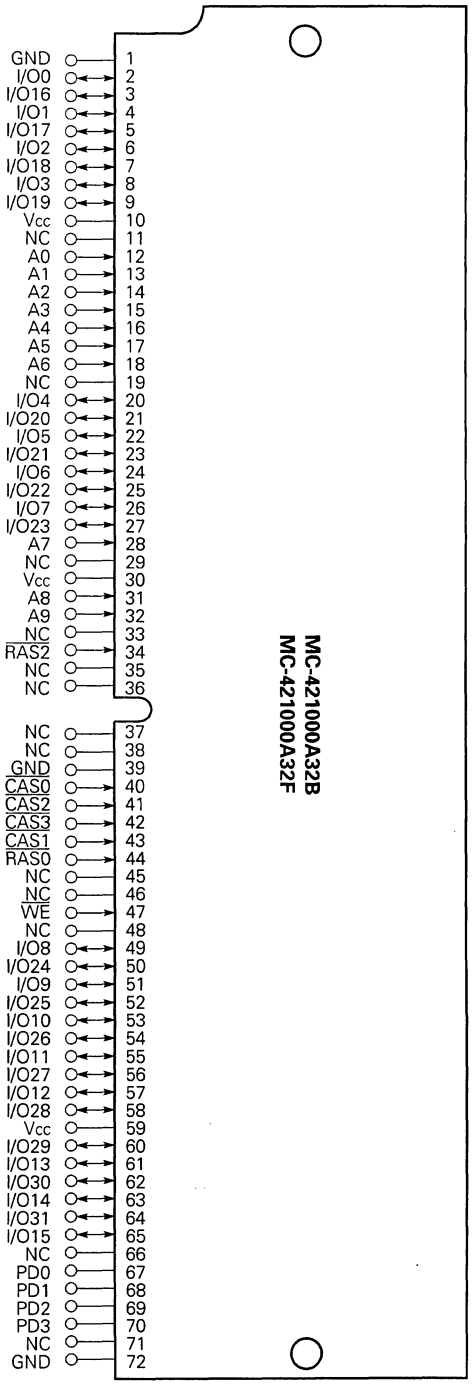
[MC-421000A36 series]

Part number	Access time (MAX.)	Package	Mounted devices
		72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μPD424400LA (300 mil SOJ) 4 pieces of μPD421000LA (300 mil SOJ) [Double side]
MC-421000A36BE-70	70 ns		
MC-421000A36BE-80	80 ns		
MC-421000A36BE-10	100 ns		
		72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000A36FE-70	70 ns		
MC-421000A36FE-80	80 ns		
MC-421000A36FE-10	100 ns		
		72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μPD424400LA (300 mil SOJ) 4 pieces of μPD421000LA (300 mil SOJ) [Single side]
MC-421000A36BJ-70	70 ns		
MC-421000A36BJ-80	80 ns		
MC-421000A36BJ-10	100 ns		
		72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000A36FJ-70	70 ns		
MC-421000A36FJ-80	80 ns		
MC-421000A36FJ-10	100 ns		

Pin Configuration

[MC-421000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



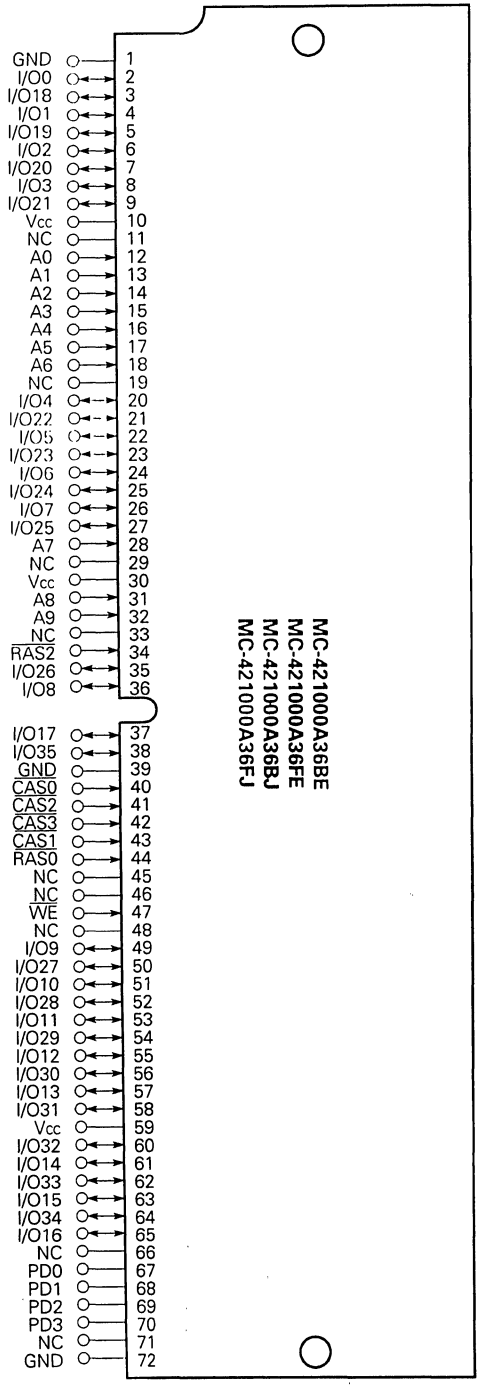
A0 - A9	: Address Inputs
I/O0 - I/O31	: Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	GND	GND	GND	GND
PD1	68	GND	GND	GND	GND
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

[MC-421000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



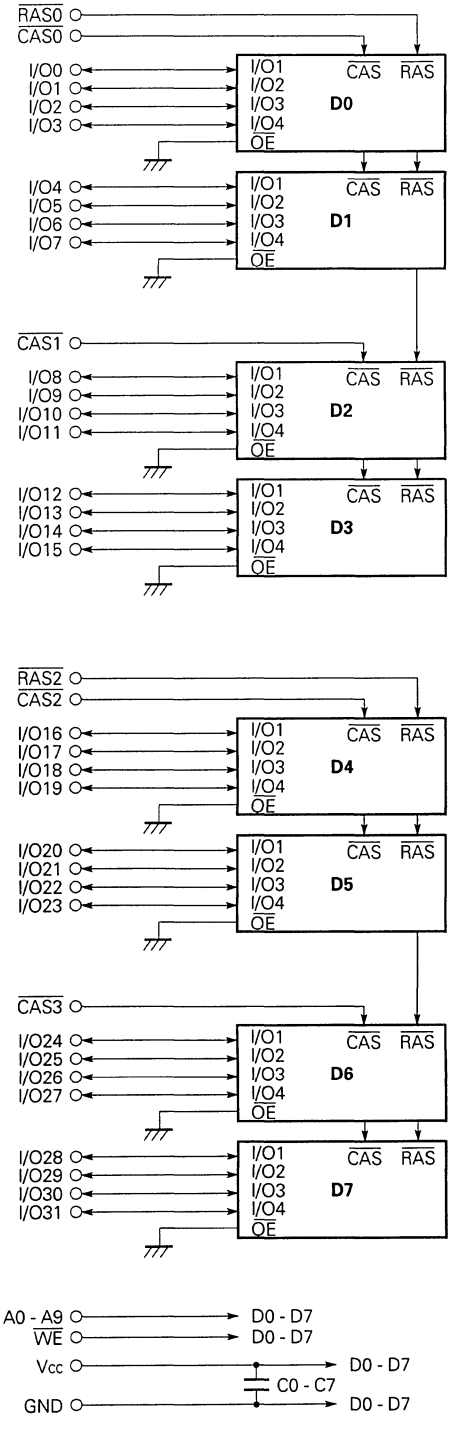
A0 - A9	: Address Inputs
I/O0 - I/O35	: Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
			70 ns	80 ns	100 ns
PD0	67	GND	GND	GND	GND
PD1	68	GND	GND	GND	GND
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

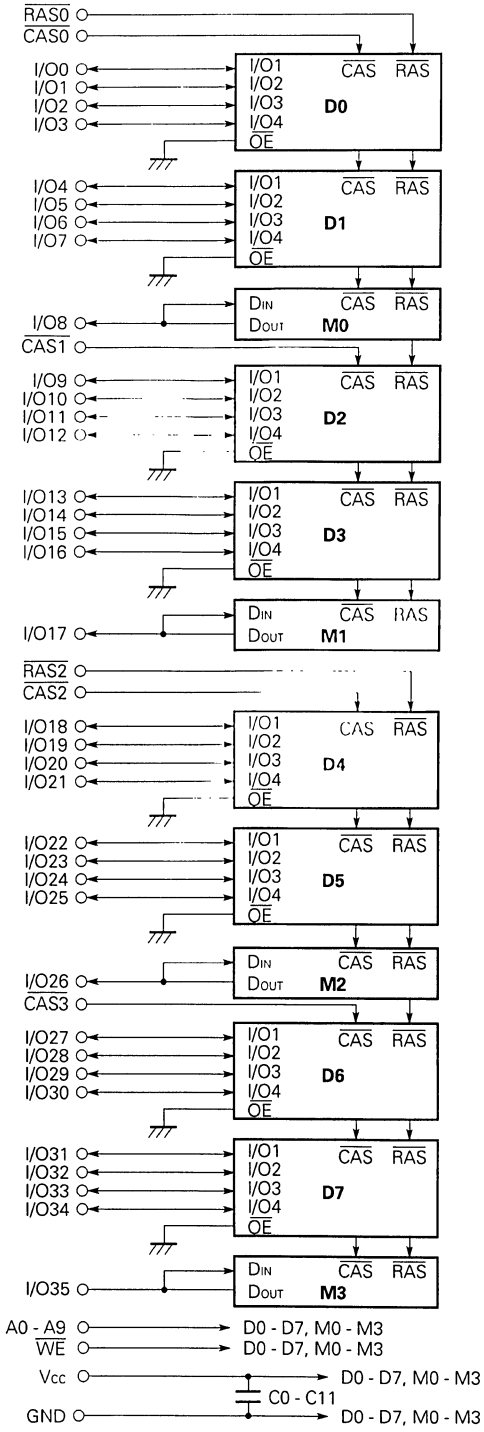
Block Diagram

[MC-421000A32 series]



Remark D0 - D7 : μPD424400

[MC-421000A36 series]



Remark D0 - D7 : μPD424400
M0 - M3 : μPD421000

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-421000A32	8	W
		MC-421000A36	12	
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

[MC-421000A32 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			68	pF
	C_{I2}	$\overline{WE}$			76	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			43	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			17	pF

[MC-421000A36 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			88	pF
	C_{I2}	$\overline{WE}$			104	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			57	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			36	
Data Input/Output capacitance	$C_{I/O1}$	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			17	pF
	$C_{I/O2}$	I/O8, I/O17, I/O26, I/O35			22	

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-421000A32 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		960	mA	3, 4, 7
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		720		
			t_{RAC} = 100 ns		640		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		16	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		8		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		960	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		720		
			t_{RAC} = 100 ns		640		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		720	mA	3, 4, 6
			t_{RAC} = 70 ns		640		
			t_{RAC} = 80 ns		560		
			t_{RAC} = 100 ns		480		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		960	mA	3, 4
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		720		
			t_{RAC} = 100 ns		640		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

[MC-421000A36 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA				mA	3, 4, 7
			t_{RAC} = 70 ns		1,120		
			t_{RAC} = 80 ns		1,000		
			t_{RAC} = 100 ns		880		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		24	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		12		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA				mA	3, 4, 5, 7
			t_{RAC} = 70 ns		1,120		
			t_{RAC} = 80 ns		1,000		
			t_{RAC} = 100 ns		880		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA				mA	3, 4, 6
			t_{RAC} = 70 ns		920		
			t_{RAC} = 80 ns		800		
			t_{RAC} = 100 ns		680		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA				mA	3, 4
			t_{RAC} = 70 ns		1,120		
			t_{RAC} = 80 ns		1,000		
			t_{RAC} = 100 ns		880		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

[MC-421000A32 series]

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	120		140		160		190		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		60		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20		25	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40		50	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45		55	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	17	50	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		20		20		25		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	25	75	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		10		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		50		ns	
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		15		20		ns	15
Data-in Setup Time	t_{DS}	0		0		0		0		ns	16
Data-in Hold Time	t_{DH}	15		15		15		20		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	15		15		15		20		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		20		ns	
Refresh Time	t_{REF}		16		16		16		16	ms	

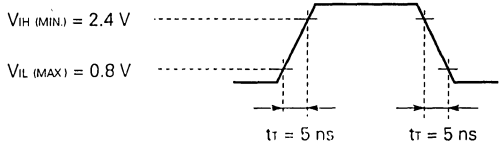
[MC-421000A36 series]

Parameter	Symbol	t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	140		160		190		ns	
Fast Page Mode Cycle Time	t_{PC}	45		50		60		ns	
Access Time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		50	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		55	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	17	40	17	50	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60		70		80		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	70	125,000	80	125,000	100	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70		80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	25	60	25	75	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		55		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		12		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	17		20		20		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	35		40		50		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		20		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	15		20		20		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	15		15		20		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		20		ns	
Refresh Time	t_{REF}		16		16		16	ms	

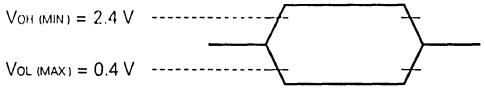
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 2 TTLs and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

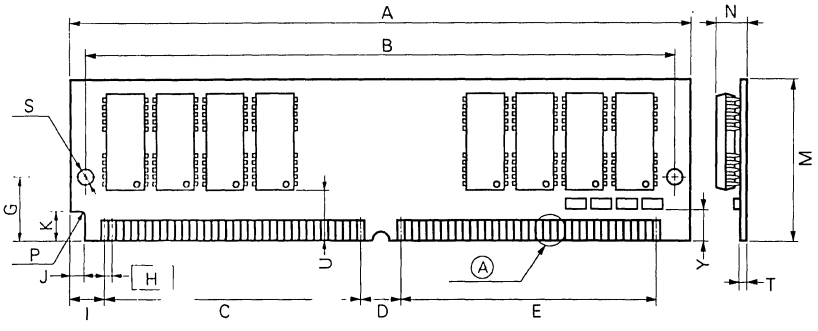
Timing Chart

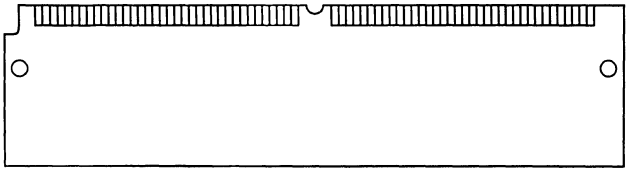
Please refer to Timing Chart 2, page 375.

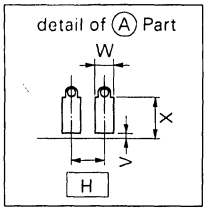
Package Drawings

[MC-421000A32B, 421000A32F]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





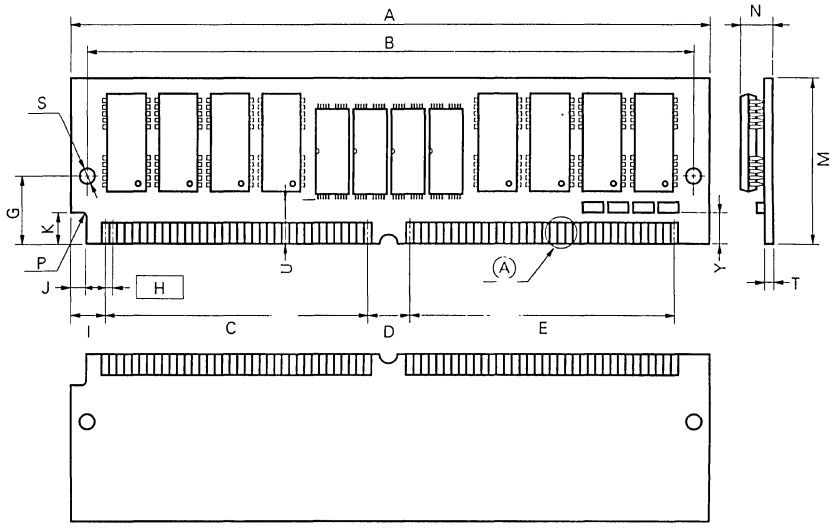


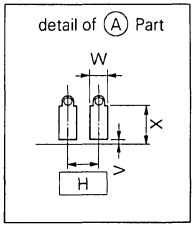
M72B-50A21-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	φ3.18	φ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	6.5 MIN.	0.255 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

(Not Applicable)

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



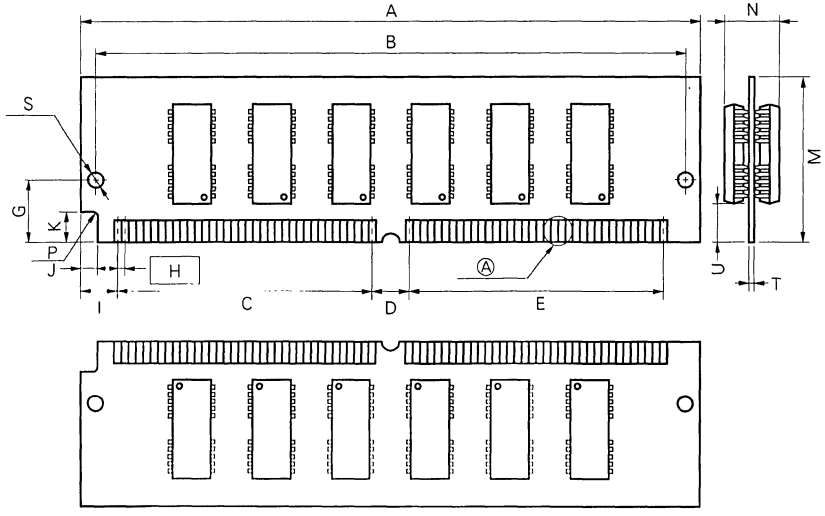


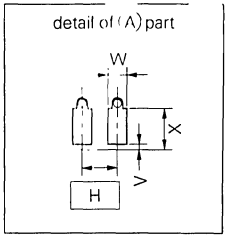
M72B-50A19-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.32 MIN.	0.209 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

[MC-421000A36BE, 421000A36FE]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



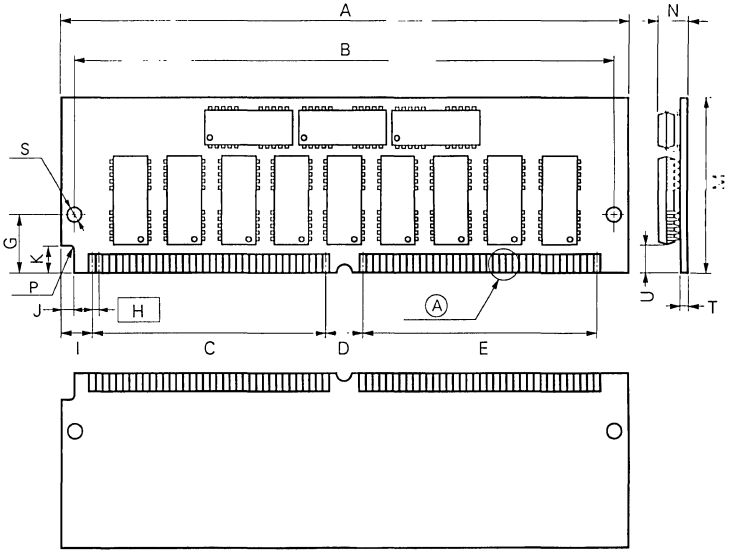


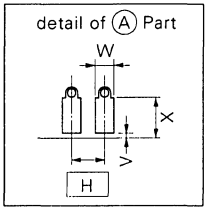
M72B-50A33-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R 1.57	R 0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	6.0 MIN.	0.236 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

[MC-421000A36BJ, 421000A36FJ]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





M72B-50A23-2

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0 400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	31.75	1 250
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	3.78 MIN.	0.148 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

NEC

MOS INTEGRATED CIRCUIT

MC-422000A32BA, 422000A32FA

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-422000A32BA, 422000A32FA are 2,097,152 words by 32 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μPD4218160 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000A32-60	60 ns	110 ns	1,782 mW	22 mW (CMOS level input)
MC-422000A32-70	70 ns	130 ns	1,672 mW	
MC-422000A32-80	80 ns	150 ns	1,562 mW	

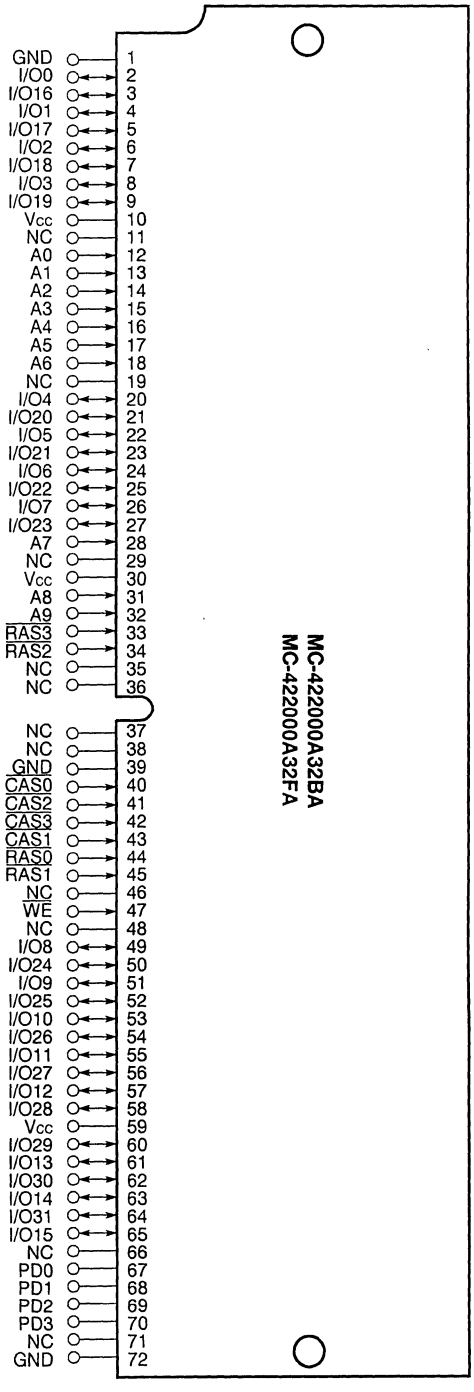
- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000A32BA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	4 pieces of μPD4218160LE (400 mil SOJ) [Double side]
MC-422000A32BA-70	70 ns		
MC-422000A32BA-80	80 ns		
MC-422000A32FA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-422000A32FA-70	70 ns		
MC-422000A32FA-80	80 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)

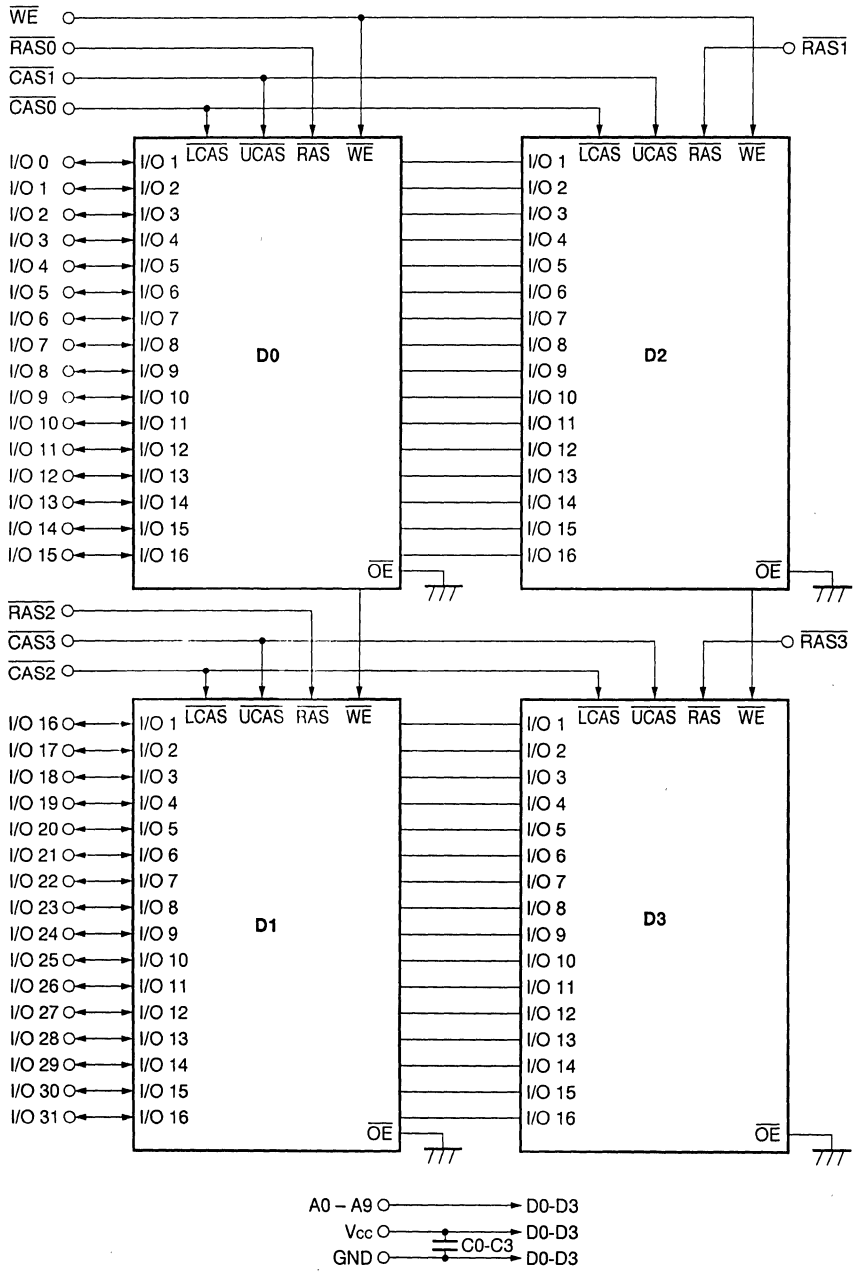


A0 - A9	:	Address Inputs
I/O0 - I/O31	:	Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	:	Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$	:	Row Address Strobe
$\overline{WE}$	:	Write Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	NC	NC	NC
PD1	68	NC	NC	NC
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

Block Diagram



Remark D0 - D3: μPD4218160

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		4	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			40	pF
	C_{I2}	$\overline{WE}$			48	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			22	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			26	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		324	mA	3, 4, 7
			t_{RAC} = 70 ns		304		
			t_{RAC} = 80 ns		284		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		8	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		4		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		324	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		304		
			t_{RAC} = 80 ns		284		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		184	mA	3, 4, 6
			t_{RAC} = 70 ns		164		
			t_{RAC} = 80 ns		144		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		324	mA	3, 4
			t_{RAC} = 70 ns		304		
			t_{RAC} = 80 ns		284		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

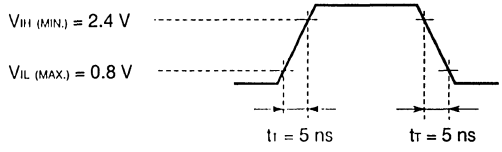
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		16		16		16	ms	

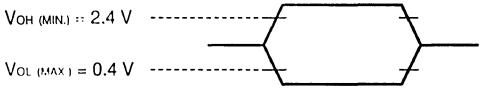
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

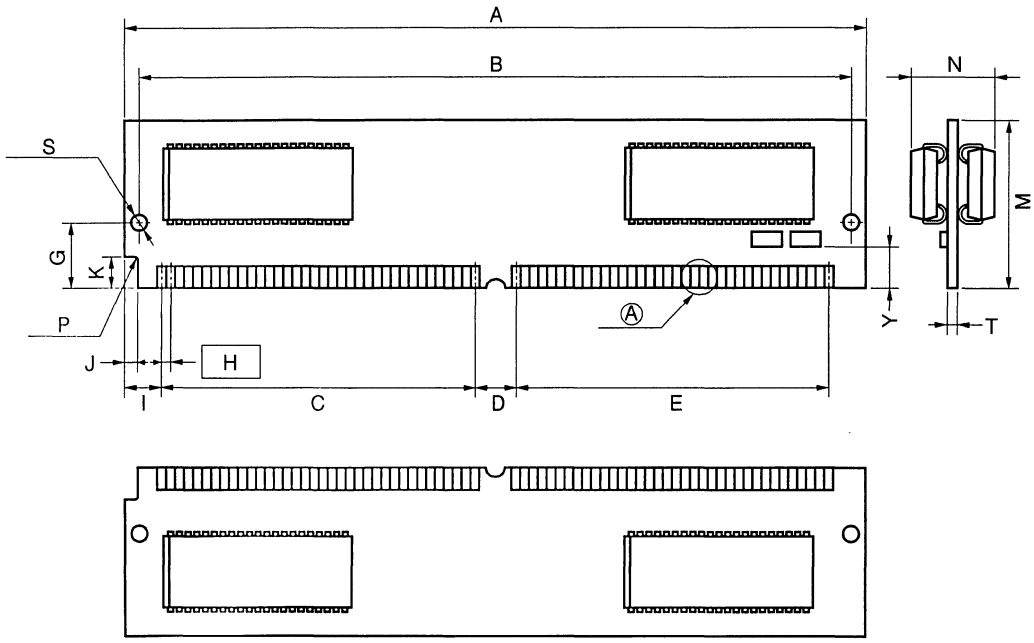
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{OFF\ (MAX.)}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}$/$\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

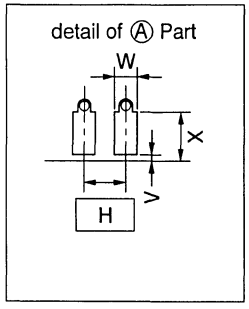
Timing Chart

Please refer to Timing Chart 1, page 365.

Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.

M72B-50A45

NEC

MOS INTEGRATED CIRCUIT

MC-422000A32, 422000A36 SERIES

2 M-WORD BY 32-BIT, 2 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-422000A32 series is a 2 097 152 words by 32 bits dynamic RAM module on which 16 pieces of 4 M DRAM (μPD424400) are assembled.

The MC-422000A36 series is a 2 097 152 words by 36 bits dynamic RAM module on which 16 pieces of 4 M DRAM (μPD424400) and 8 pieces of 1 M DRAM (μPD421000) are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2 097 152 words by 32 bits organization (MC-422000A32 series)
- 2 097 152 words by 36 bits organization (MC-422000A36 series)
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000A32-60	60 ns	120 ns	5 355 mW	84 mW
MC-422000A32-70	70 ns	140 ns	4 515 mW	
MC-422000A32-80	80 ns	160 ns	4 095 mW	
MC-422000A32-10	100 ns	190 ns	3 675 mW	
				126 mW
MC-422000A36-70	70 ns	140 ns	6 195 mW	
MC-422000A36-80	80 ns	160 ns	5 565 mW	
MC-422000A36-10	100 ns	190 ns	4 935 mW	

- 1 024 refresh cycles/16 ms
- Three refresh modes are available: $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- All inputs and outputs are TTL compatible
- Single +5.0 V ± 5 % power supply
- Access time can be distinguished with characteristics of PD-pins(PD0 to PD3)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	16 pieces of μPD424400LA (300 mil SOJ) [Double side]
MC-422000A32B-70	70 ns		
MC-422000A32B-80	80 ns		
MC-422000A32B-10	100 ns		
MC-422000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-422000A32F-70	70 ns		
MC-422000A32F-80	80 ns		
MC-422000A32F-10	100 ns		
		72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	16 pieces of μPD424400LA (300 mil SOJ) 8 pieces of μPD421000LA (300 mil SOJ) [Double side]
MC-422000A36BJ-70	70 ns		
MC-422000A36BJ-80	80 ns		
MC-422000A36BJ-10	100 ns		
		72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-422000A36FJ-70	70 ns		
MC-422000A36FJ-80	80 ns		
MC-422000A36FJ-10	100 ns		

Quality Grade

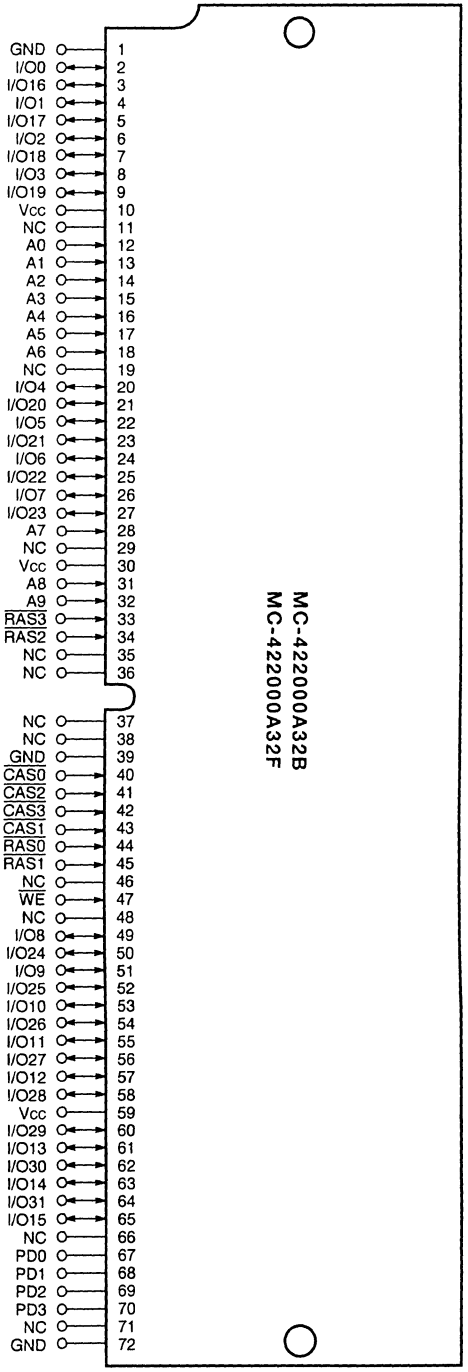
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations (Front view)

[MC-422000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



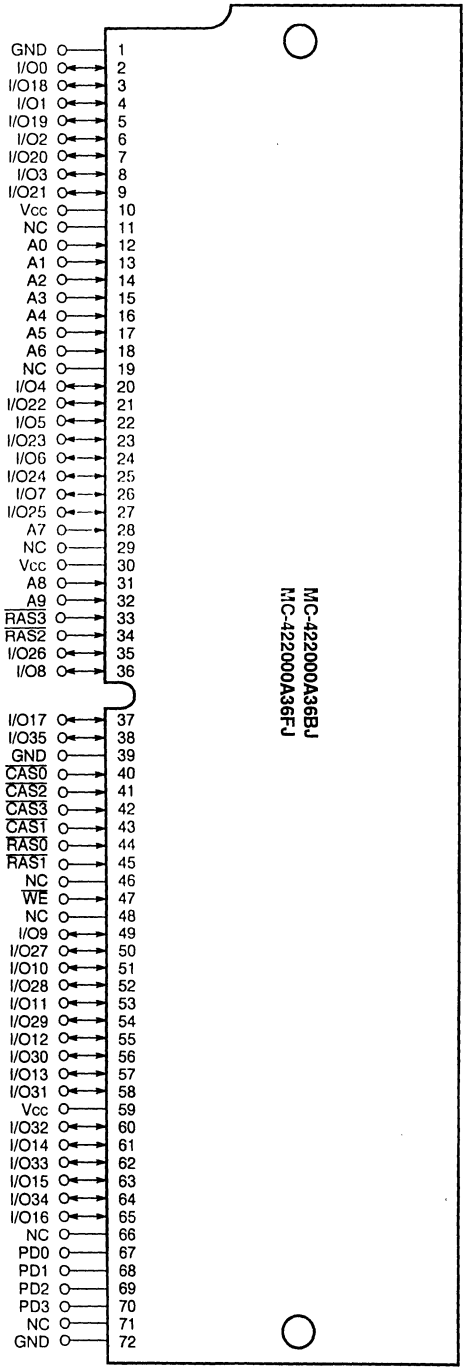
A0-A9	: Address Inputs
I/O0-I/O31	: Data Inputs/Outputs
$\overline{CAS0}$-$\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$-$\overline{RAS3}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	NC	NC	NC	NC
PD1	68	NC	NC	NC	NC
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

[MC-422000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



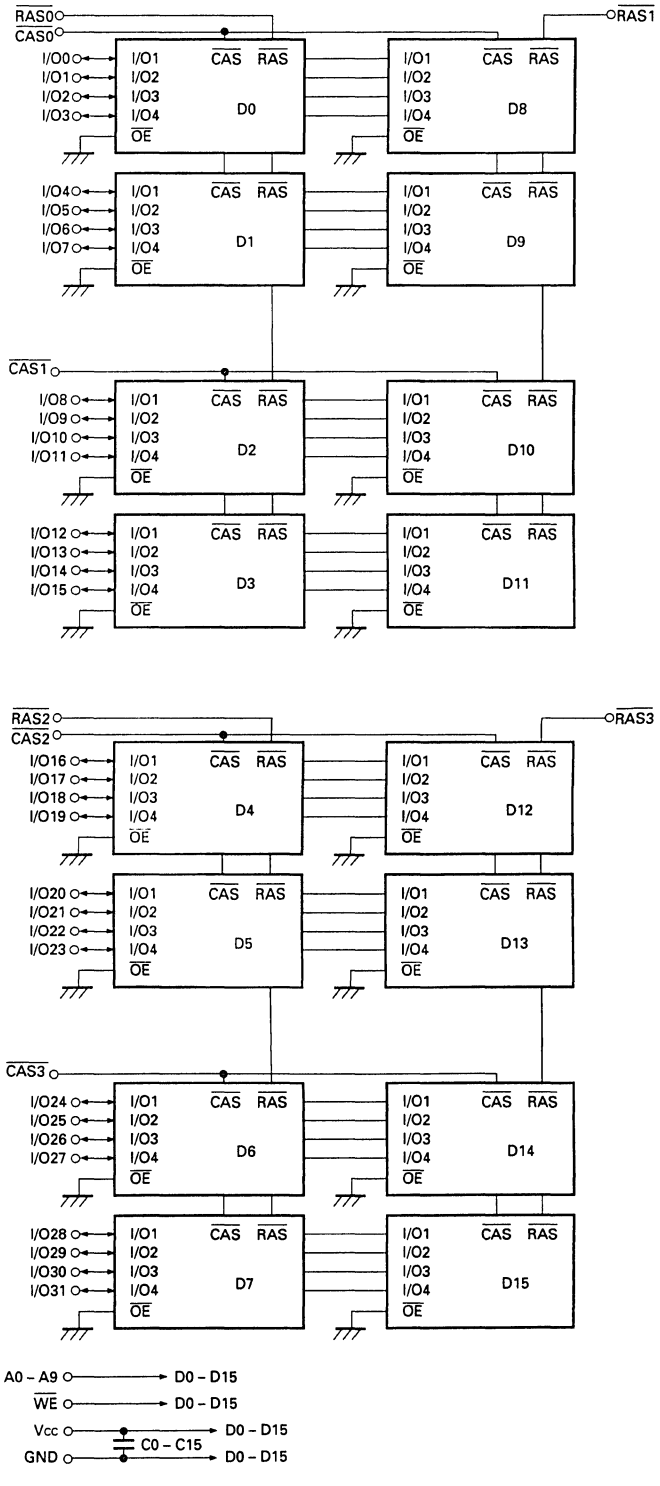
A0-A9	: Address Inputs
I/O0-I/O35	: Data Inputs/Outputs
$\overline{CAS0}$-$\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$-$\overline{RAS3}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
			70 ns	80 ns	100 ns
PD0	67	NC	NC	NC	NC
PD1	68	NC	NC	NC	NC
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

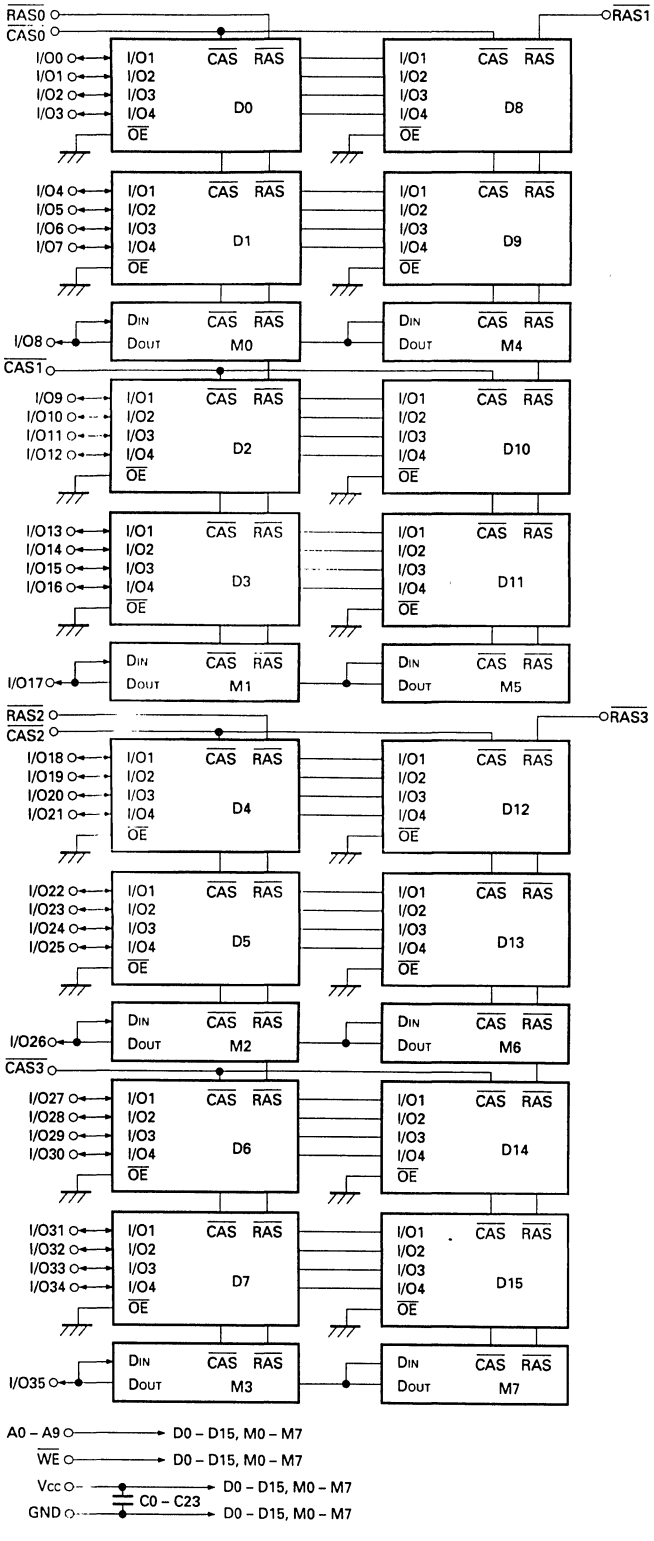
Block Diagrams

[MC-422000A32 series]



Remark D0-D15 : μPD424400

[MC-422000A36 series]



Remark D0-D15 : μPD424400

M0-M7 : μPD421000

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-422000A32	16	W
		MC-422000A36	24	
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} +1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance (T_a = +25 °C, f = 1 MHz)

[MC-422000A32 series]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			121	pF
	C_{I2}	$\overline{WE}$			137	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			48	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			48	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			29	pF

[MC-422000A36 series]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			161	pF
	C_{I2}	$\overline{WE}$			193	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			62	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			62	
Data Input/Output capacitance	$C_{I/O1}$	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			29	pF
	$C_{I/O2}$	I/O8, I/O17, I/O26, I/O35			39	

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-422000A32 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1 020	mA	3,4,7
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		780		
			t_{RAC} = 100 ns		700		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$	I_O = 0 mA		32	mA	
		$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$–0.2 V	I_O = 0 mA		16		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geqq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1 020	mA	3,4,5,7
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		780		
			t_{RAC} = 100 ns		700		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		780	mA	3,4,6
			t_{RAC} = 70 ns		700		
			t_{RAC} = 80 ns		620		
			t_{RAC} = 100 ns		540		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1 020	mA	3,4
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		780		
			t_{RAC} = 100 ns		700		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	I/O0 to I/O31 is disabled (Hi-Z) V_O = 0 to 5.5 V		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

[MC-422000A36 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		1 180	mA	3,4,7
			t_{RAC} = 80 ns		1 060		
			t_{RAC} = 100 ns		940		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH (MIN.)}$	I_O = 0 mA		48	mA	
		$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$–0.2 V	I_O = 0 mA		24		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geqq V_{IH (MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		1 180	mA	3,4,5,7
			t_{RAC} = 80 ns		1 060		
			t_{RAC} = 100 ns		940		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leqq V_{IL (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		980	mA	3,4,6
			t_{RAC} = 80 ns		860		
			t_{RAC} = 100 ns		740		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		1 180	mA	3,4
			t_{RAC} = 80 ns		1 060		
			t_{RAC} = 100 ns		940		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	I/O0 to I/O35 is disabled (Hi-Z) V_O = 0 to 5.5 V		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

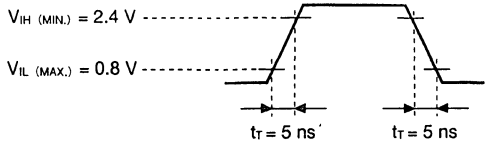
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9, 18

Parameter		Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read or Write Cycle Time		t_{RC}	120		140		160		190		ns	
Fast Page Mode Cycle Time (Read or Write)		t_{PC}	40		45		50		60		ns	
Access Time from $\overline{RAS}$		t_{RAC}		60		70		80		100	ns	10,11
Access Time from $\overline{CAS}$ (Falling Edge)	MC-422000A32	t_{CAC}		15		20		20		25	ns	10,11
	MC-422000A36											
Access Time from Column Address		t_{AA}		30		35		40		50	ns	10,11
Access Time from $\overline{CAS}$ Precharge		t_{ACP}		35		40		45		55	ns	11
$\overline{RAS}$ to Column Address Delay Time		t_{RAD}	15	30	15	35	17	40	17	50	ns	10
$\overline{CAS}$ to Data Setup Time		t_{CLZ}	0		0		0		0		ns	11
Output Buffer Turn-off Delay Time ($\overline{CAS}$)		t_{OFF}	0	15	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)		t_T	3	50	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time		t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ Pulse Width (Random Read, Write Cycle)		t_{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)		t_{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
$\overline{RAS}$ Hold Time		t_{RSH}	20		20		20		25		ns	
$\overline{CAS}$ Pulse Width		t_{CAS}	20	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{CAS}$ Hold Time		t_{CSH}	60		70		80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	MC-422000A32	t_{RCD}	20	40	20	50	25	60	25	90	ns	10
	MC-422000A36									75		
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	10		10		10		10		ns	13
$\overline{CAS}$ Precharge Time		t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)		t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time		t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35		40		45		55		ns	
Row Address Setup Time		t_{ASR}	0		0		0		0		ns	
Row Address Hold Time		t_{RAH}	10		10		12		12		ns	
Column Address Setup Time		t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	MC-422000A32	t_{CAH}	15		15		15		20		ns	
	MC-422000A36				17		20					
Column Address Lead Time Referenced to $\overline{RAS}$		t_{RAL}	30		35		40		50		ns	
Read Command Setup Time		t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	10		10		10		10		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$		t_{RCH}	0		0		0		0		ns	14
Write Command Hold Time Referenced to $\overline{CAS}$		t_{WCH}	15		15		15		20		ns	15
Data-in Setup Time		t_{DS}	0		0		0		0		ns	16
Data-in Hold Time	MC-422000A32	t_{DH}	15		15		15		20		ns	16
	MC-422000A36						20					
Write Command Setup Time		t_{WCS}	0		0		0		0		ns	17
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh		t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh		t_{CHR}	15		15		15		20		ns	
$\overline{WE}$ Setup Time		t_{WSR}	10		10		10		10		ns	
$\overline{WE}$ Hold Time		t_{WHR}	15		15		15		20		ns	
Refresh Time		t_{REF}		16		16		16		16	ms	

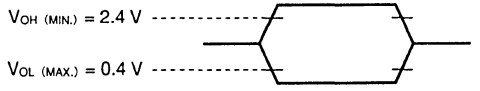
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL}$ (MAX.) and $\overline{CAS} \geqq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows :

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD}$ (MAX.), $t_{RCD} \leqq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.), $t_{RCD} \leqq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

t_{RAD} (MAX.) and t_{RCD}(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD}$ (MAX.) and $t_{RCD} \geqq t_{RCD}$ (MAX.) will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirement should be applied for $\overline{RAS}$ / $\overline{CAS}$ cycles preceded by any cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geqq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
18. The column "trac = 60 ns" is not applicable to MC-422000A36.

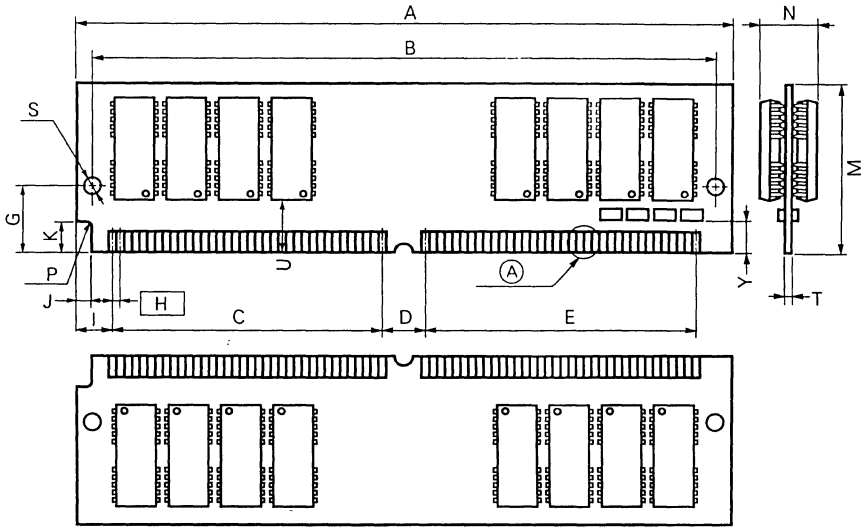
Timing Chart

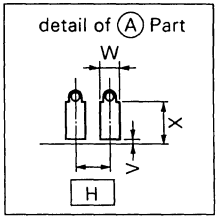
Please refer to Timing Chart 2, page 375.

Package Drawings

MC-422000A32B, 422000A32F

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



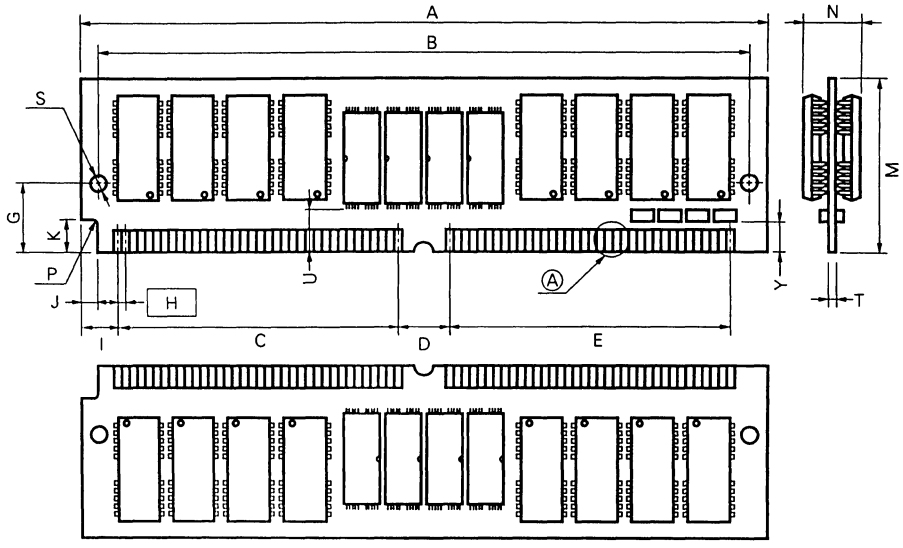


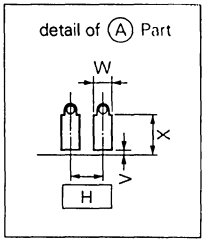
M72B-50A22-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R 2.0	R 0.079
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	6.5 MIN.	0.255 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

(Not Applicable)

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



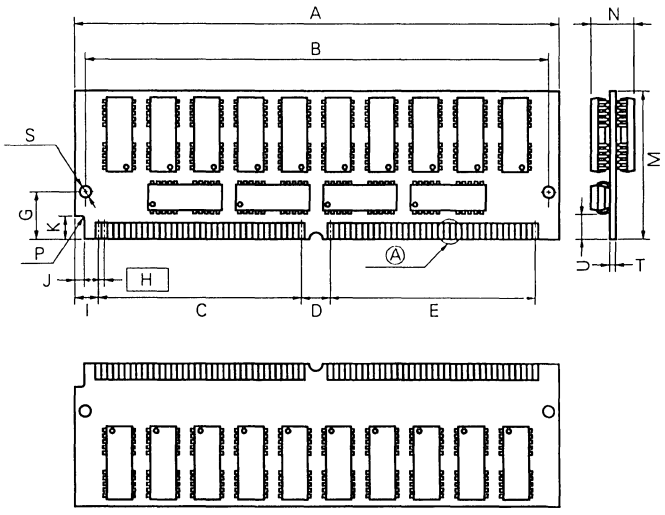


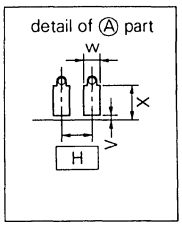
M72B-50A20-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.354 MAX.
P	R 2.0	R 0.079
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.32 MIN.	0.209 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

MC-422000A36BJ, 422000A36FJ

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





M72B-50A44

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	31.75	1.250
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	3.17 MIN.	0.124 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.

NEC

MOS INTEGRATED CIRCUIT

MC-424000A32, 424000A36 SERIES

4 M-WORD BY 32-BIT, 4 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-424000A32 series is a 4,194,304 words by 32 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μPD4217400 are assembled.

The MC-424000A36 series is a 4,194,304 words by 36 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μPD4217400 and 4 pieces of 4 M DRAM: μPD424100 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 32 bits organization (MC-424000A32 series)
- 4,194,304 words by 36 bits organization (MC-424000A36 series)
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000A32-60	60 ns	110 ns	4,840 mW	44 mW (CMOS level input)
MC-424000A32-70	70 ns	130 ns	4,400 mW	
MC-424000A32-80	80 ns	150 ns	3,960 mW	
MC-424000A36-60	60 ns	110 ns	7,480 mW	66 mW (CMOS level input)
MC-424000A36-70	70 ns	130 ns	6,600 mW	
MC-424000A36-80	80 ns	150 ns	5,940 mW	

- 2,048 refresh cycles/32 ms
- 2,048 refresh cycles/16 ms (MC-424000A36 burst refesh)
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

[MC-424000A32 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μPD4217400LA (300 mil SOJ) [Single side]
MC-424000A32B-70	70 ns		
MC-424000A32B-80	80 ns		
MC-424000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-424000A32F-70	70 ns		
MC-424000A32F-80	80 ns		

[MC-424000A36 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000A36BE-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μPD4217400LA (300 mil SOJ) 4 pieces of μPD424100LA (300 mil SOJ) [Double side]
MC-424000A36BE-70	70 ns		
MC-424000A36BE-80	80 ns		
MC-424000A36FE-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-424000A36FE-70	70 ns		
MC-424000A36FE-80	80 ns		
MC-424000A36BJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μPD4217400LA (300 mil SOJ) 4 pieces of μPD424100LA (300 mil SOJ) [Single side]
MC-424000A36BJ-70	70 ns		
MC-424000A36BJ-80	80 ns		
MC-424000A36FJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-424000A36FJ-70	70 ns		
MC-424000A36FJ-80	80 ns		

Quality Grade

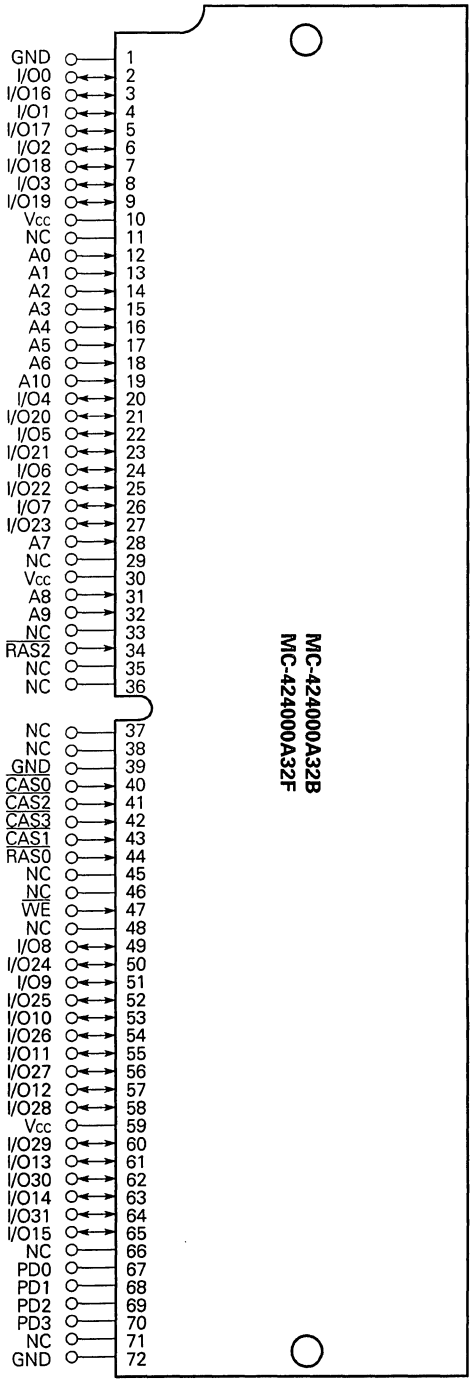
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration

[MC-424000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



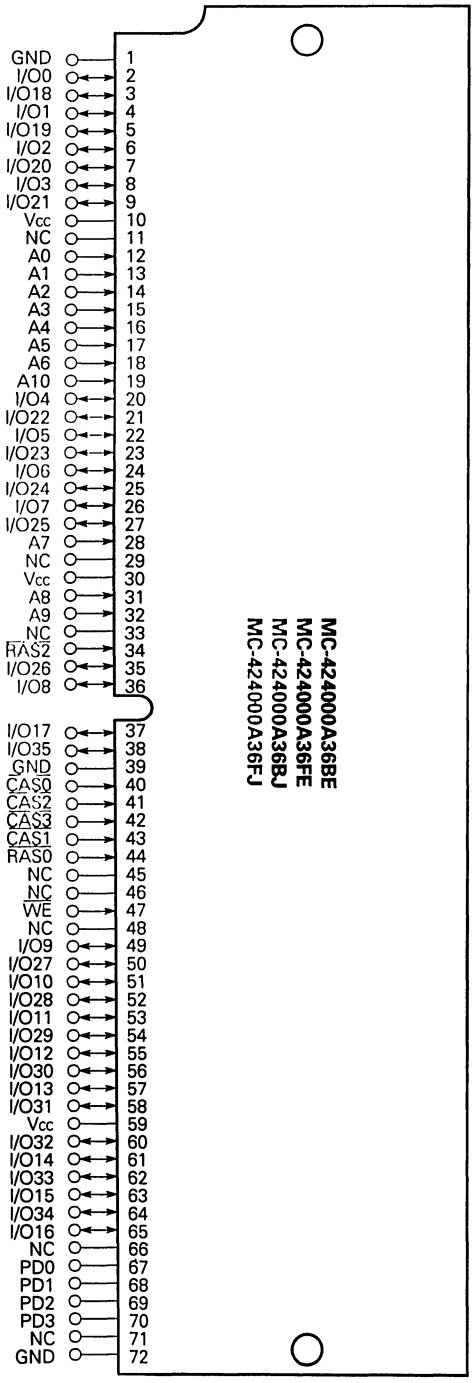
A0 - A10	: Address Inputs
I/O0 - I/O31	: Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	GND	GND	GND
PD1	68	NC	NC	NC
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

[MC-424000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



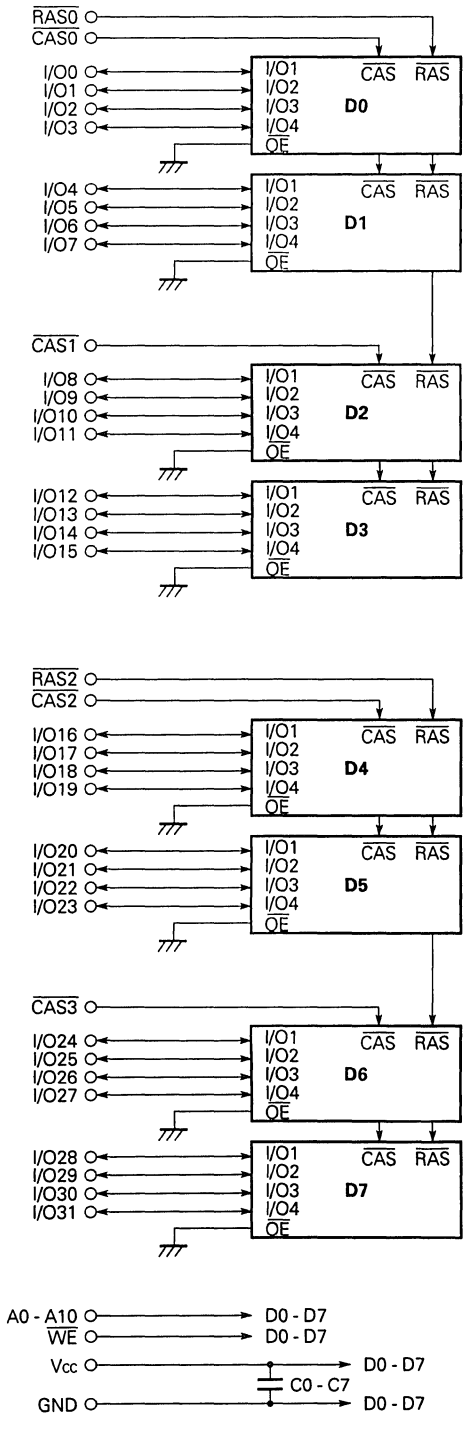
A0 - A10	:	Address Inputs
I/O0 - I/O35	:	Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	:	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	:	Row Address Strobe
$\overline{WE}$	:	Write Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	GND	GND	GND
PD1	68	NC	NC	NC
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

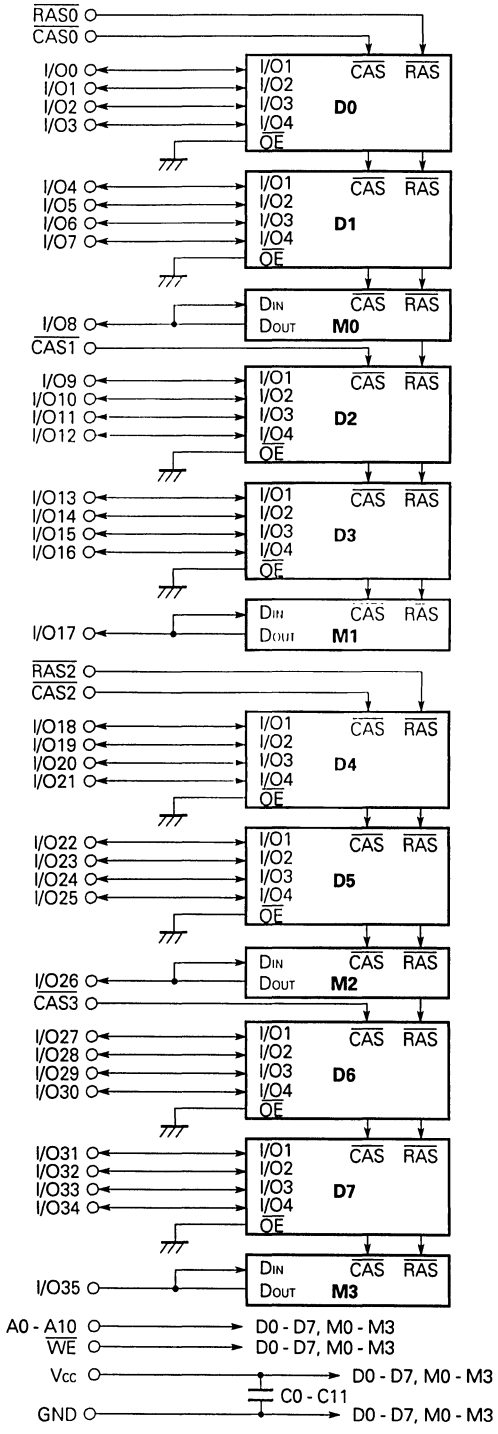
Block Diagram

[MC-424000A32 series]



Remark D0 - D7 : μPD4217400

[MC-424000A36 series]



Remark D0 - D7 : μPD4217400
M0 - M3 : μPD424100

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-424000A32	8	W
		MC-424000A36	12	
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance (T_a = +25 °C, f = 1 MHz)

[MC-424000A32 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			68	pF
	C_{I2}	$\overline{WE}$			76	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			43	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			17	pF

[MC-424000A36 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			88	pF
	C_{I2}	$\overline{WE}$			104	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			57	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			36	
Data Input/Output capacitance	$C_{I/O1}$	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			17	pF
	$C_{I/O2}$	I/O8, I/O17, I/O26, I/O35			22	

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-424000A32 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		880	mA	3, 4, 7
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		720		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		16	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		8		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		880	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		720		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		560	mA	3, 4, 6
			t_{RAC} = 70 ns		480		
			t_{RAC} = 80 ns		400		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		880	mA	3, 4
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		720		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

[MC-424000A36 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,360	mA	3, 4, 7
			t_{RAC} = 70 ns		1,200		
			t_{RAC} = 80 ns		1,080		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		24	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		12		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,360	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		1,200		
			t_{RAC} = 80 ns		1,080		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		920	mA	3, 4, 6
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		680		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,360	mA	3, 4
			t_{RAC} = 70 ns		1,200		
			t_{RAC} = 80 ns		1,080		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

[MC-424000A32 series]

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		32		32		32	ms	

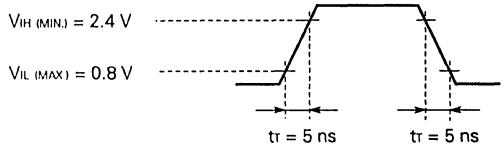
[MC-424000A36 series]

Parameter		Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time		t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time		t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$		t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$		t_{CAC}		15		20		20	ns	10, 11
Access Time Column Address		t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge		t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time		t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time		t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$		t_{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)		t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time		t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width		t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)		t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time		t_{RSH}	20		20		20		ns	
$\overline{CAS}$ Pulse Width		t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time		t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	10		10		10		ns	13
$\overline{CAS}$ Precharge Time		t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)		t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time		t_{RPC}	10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35		40		45		ns	
Row Address Setup Time		t_{ASR}	0		0		0		ns	
Row Address Hold Time		t_{RAH}	10		10		12		ns	
Column Address Setup Time		t_{ASC}	0		0		0		ns	
Column Address Hold Time		t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$		t_{RAL}	30		35		40		ns	
Read Command Setup Time		t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$		t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$		t_{WCH}	15		15		15		ns	15
Data-in Setup Time		t_{DS}	0		0		0		ns	16
Data-in Hold Time		t_{DH}	15		15		15		ns	16
Write Command Setup Time		t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time		t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time		t_{WHR}	15		15		15		ns	
Refresh Time	Distributed refresh	t_{REF}		32		32		32	ms	
	Burst refresh			16		16		16	ms	

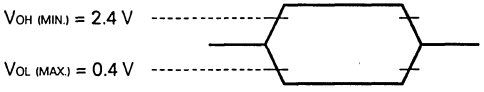
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 2 TTLs and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}$/$\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

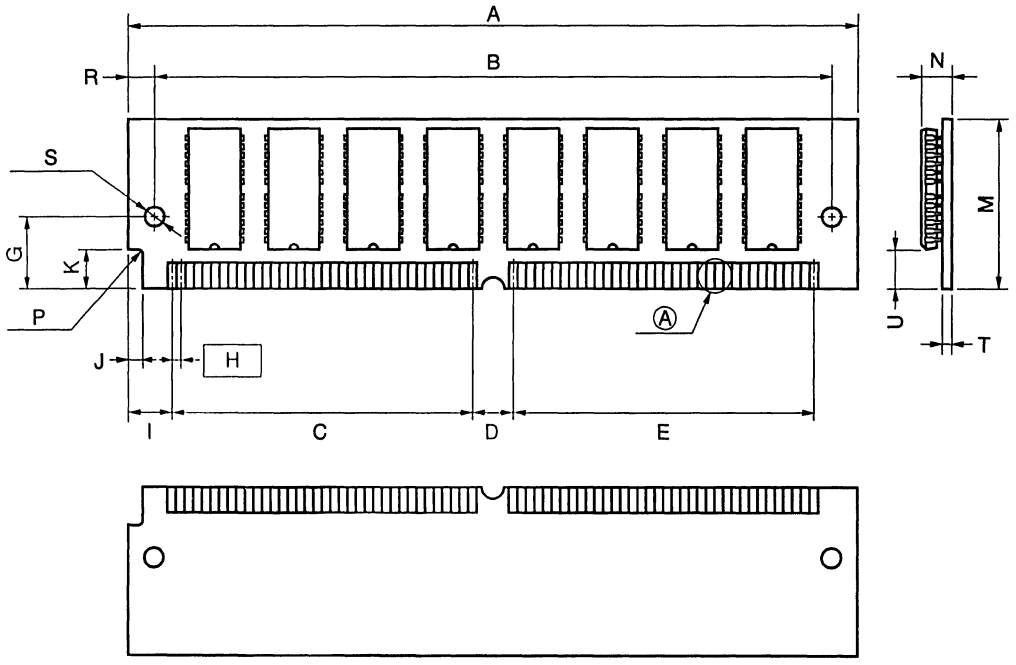
Timing Chart

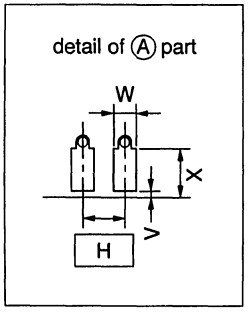
Please refer to Timing Chart 2, page 375.

Package Drawings

[MC-424000A32B, 424000A32F]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



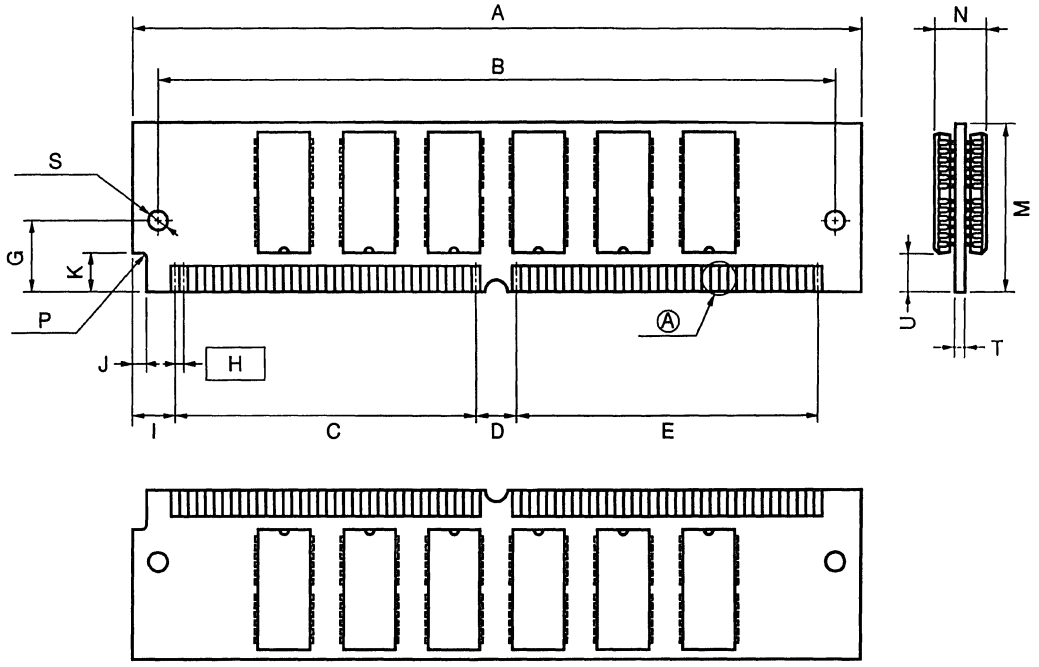


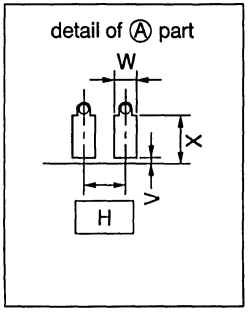
ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	$3.984^{+0.005}_{-0.006}$
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
R	3.38±0.13	$0.133^{+0.006}_{-0.005}$
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.5 MIN.	0.216 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A54

[MC-424000A36BE, 424000A36FE]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



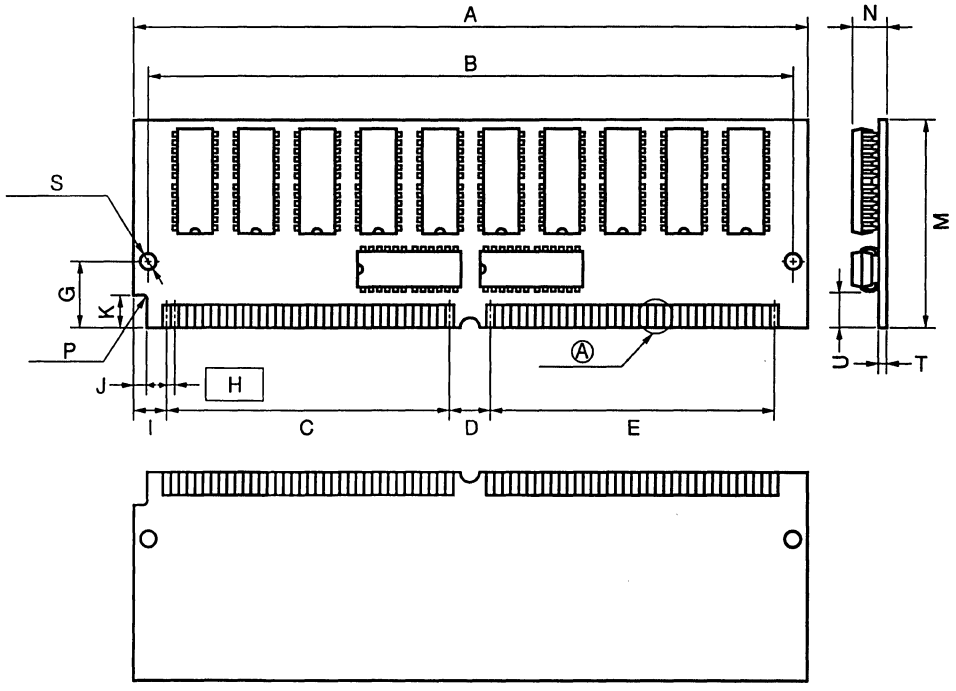


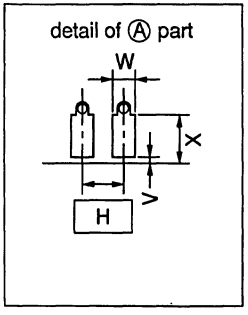
ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.08 MIN.	0.200 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.

M72B-50A47

[MC-424000A36BJ, 424000A36FJ]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	31.75	1.250
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
S	φ3.18	φ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	3.17 MIN.	0.124 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.

M72B-50A51-1

NEC

MOS INTEGRATED CIRCUIT

MC-428000A32, 428000A36 SERIES

8 M-WORD BY 32-BIT, 8 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-428000A32 series is a 8,388,608 words by 32 bits dynamic RAM module on which 16 pieces of 16 M DRAM: μPD4217400 are assembled.

The MC-428000A36 series is a 8,388,608 words by 36 bits dynamic RAM module on which 16 pieces of 16 M DRAM: μPD4217400 and 8 pieces of 4 M DRAM: μPD424100 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8,388,608 words by 32 bits organization (MC-428000A32 series)
- 8,388,608 words by 36 bits organization (MC-428000A36 series)
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-428000A32-60	60 ns	110 ns	5,170 mW	88 mW (CMOS level input)
MC-428000A32-70	70 ns	130 ns	4,730 mW	
MC-428000A32-80	80 ns	150 ns	4,290 mW	
MC-428000A36-60	60 ns	110 ns	7,810 mW	132 mW (CMOS level input)
MC-428000A36-70	70 ns	130 ns	6,930 mW	
MC-428000A36-80	80 ns	150 ns	6,270 mW	

- 2,048 refresh cycles/32 ms
- 2,048 refresh cycles/16 ms (MC-428000A36 burst refesh)
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

[MC-428000A32 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-428000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	16 pieces of μPD4217400LA (300 mil SOJ) [Double side]
MC-428000A32B-70	70 ns		
MC-428000A32B-80	80 ns		
MC-428000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-428000A32F-70	70 ns		
MC-428000A32F-80	80 ns		

[MC-428000A36 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-428000A36BJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	16 pieces of μPD4217400LA (300 mil SOJ) 8 pieces of μPD424100LA (300 mil SOJ) [Double side]
MC-428000A36BJ-70	70 ns		
MC-428000A36BJ-80	80 ns		
MC-428000A36FJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-428000A36FJ-70	70 ns		
MC-428000A36FJ-80	80 ns		

Quality Grade

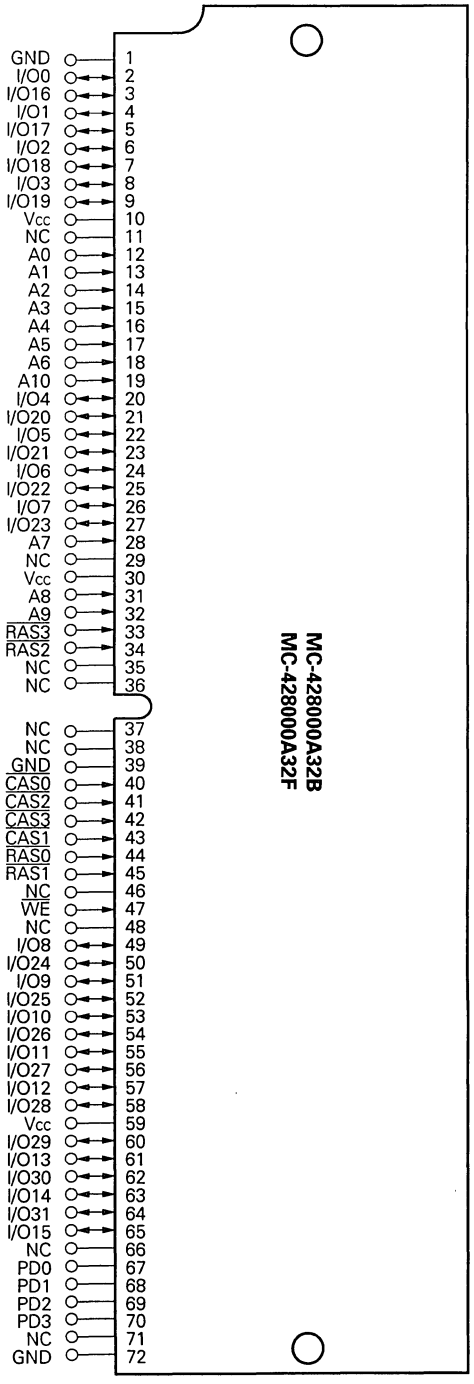
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations

[MC-428000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



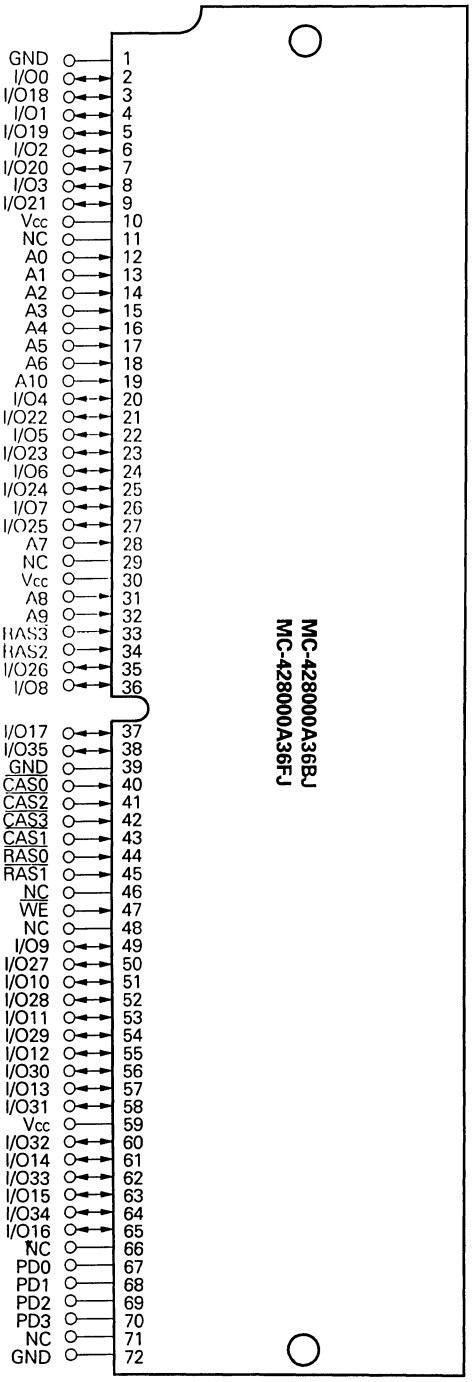
A0 - A10	: Address Inputs
I/O0 - I/O31	: Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	NC	NC	NC
PD1	68	GND	GND	GND
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

[MC-428000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



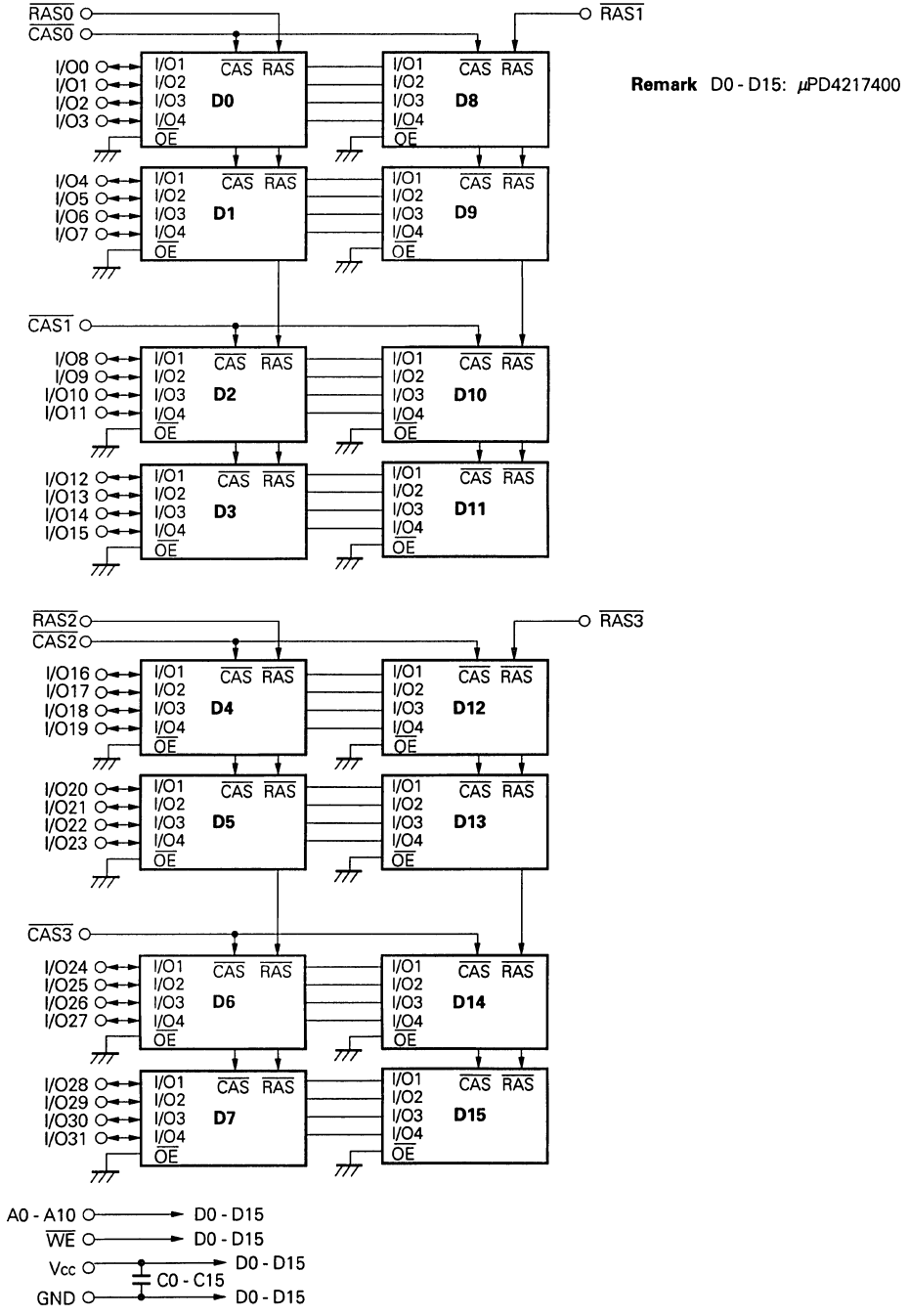
A0 - A10	: Address Inputs
I/O0 - I/O35	: Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply.
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	NC	NC	NC
PD1	68	GND	GND	GND
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

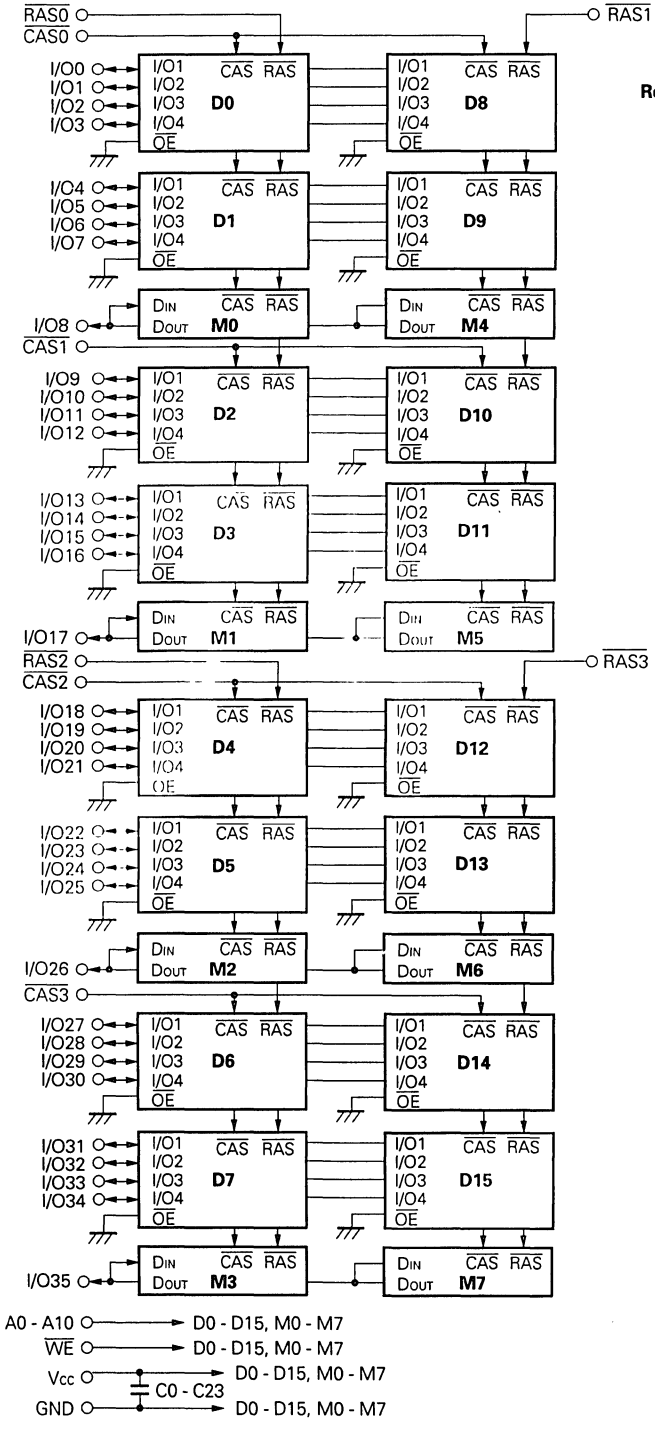
Block Diagrams

[MC-428000A32 series]



Remark D0 - D15: μPD4217400

[MC-428000A36 series]



Remark D0 - D15: μPD4217400
M0 - M7: μPD424100

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-428000A32	16	W
		MC-428000A36	24	
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

[MC-428000A32 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			121	pF
	C_{I2}	$\overline{WE}$			137	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			48	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			48	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			29	pF

[MC-428000A36 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			161	pF
	C_{I2}	$\overline{WE}$			193	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			62	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			62	
Data Input/Output capacitance	$C_{I/O1}$	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			29	pF
	$C_{I/O2}$	I/O8, I/O17, I/O26, I/O35			39	

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-428000A32 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	3, 4, 7
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		780		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		32	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		16		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		780		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		620	mA	3, 4, 6
			t_{RAC} = 70 ns		540		
			t_{RAC} = 80 ns		460		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	3, 4
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		780		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

[MC-428000A36 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,420	mA	3, 4, 7
			t_{RAC} = 70 ns		1,260		
			t_{RAC} = 80 ns		1,140		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		48	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		24		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,420	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		1,260		
			t_{RAC} = 80 ns		1,140		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		980	mA	3, 4, 6
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		740		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,420	mA	3, 4
			t_{RAC} = 70 ns		1,260		
			t_{RAC} = 80 ns		1,140		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

[MC-428000A32 series]

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		32		32		32	ms	

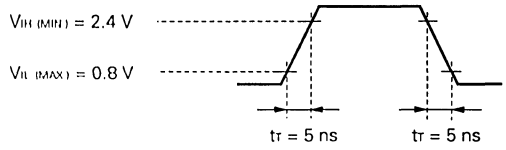
[MC-428000A36 series]

Parameter		Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time		t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time		t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$		t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$		t_{CAC}		15		20		20	ns	10, 11
Access Time Column Address		t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge		t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time		t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time		t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$		t_{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)		t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time		t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width		t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)		t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time		t_{RSH}	20		20		20		ns	
$\overline{CAS}$ Pulse Width		t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time		t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	10		10		10		ns	13
$\overline{CAS}$ Precharge Time		t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)		t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time		t_{RPC}	10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35		40		45		ns	
Row Address Setup Time		t_{ASR}	0		0		0		ns	
Row Address Hold Time		t_{RAH}	10		10		12		ns	
Column Address Setup Time		t_{ASC}	0		0		0		ns	
Column Address Hold Time		t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$		t_{RAL}	30		35		40		ns	
Read Command Setup Time		t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$		t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$		t_{WCH}	15		15		15		ns	15
Data-in Setup Time		t_{DS}	0		0		0		ns	16
Data-in Hold Time		t_{DH}	15		15		15		ns	16
Write Command Setup Time		t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time		t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time		t_{WHR}	15		15		15		ns	
Refresh Time	Distributed refresh	t_{REF}		32		32		32	ms	
	Burst refresh			16		16		16	ms	

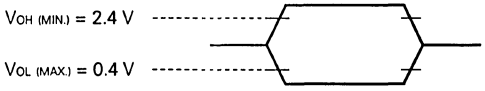
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

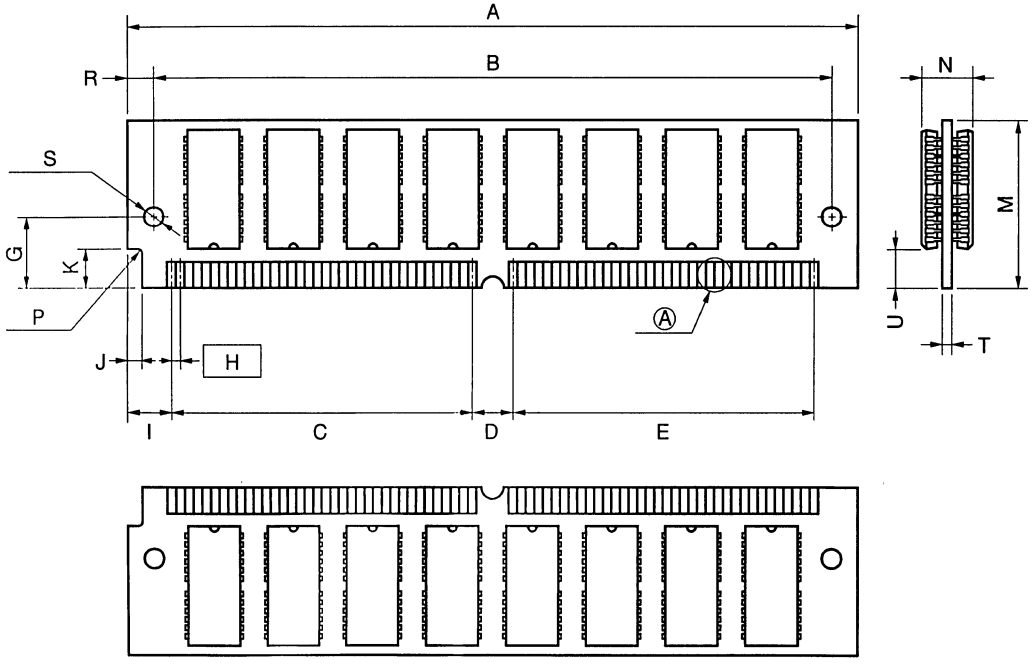
Timing Chart

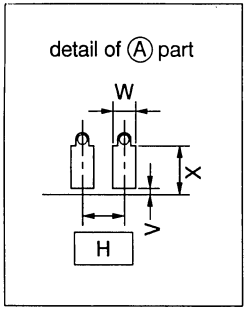
Please refer to Timing Chart 2, page 375.

Package Drawings

[MC-428000A32B, 428000A32F]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



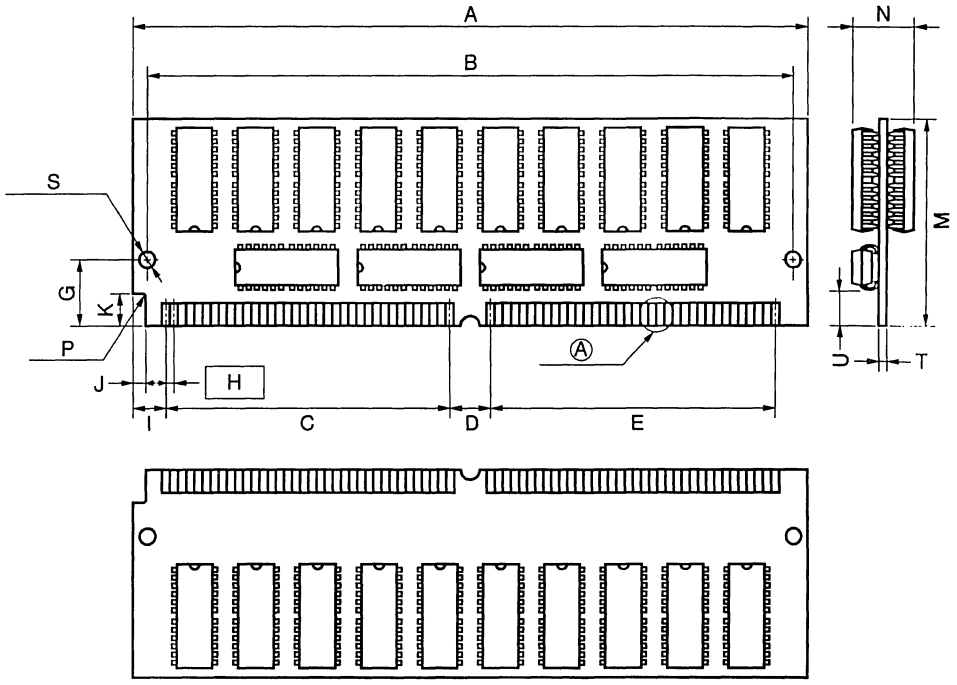


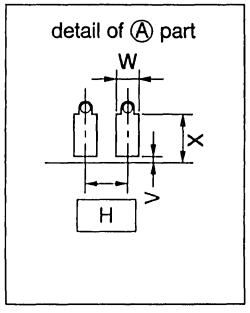
ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	$3.984^{+0.005}_{-0.006}$
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
R	3.38±0.13	$0.133^{+0.006}_{-0.005}$
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.5 MIN.	0.216 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A55

[MC-428000A36BJ, 428000A36FJ]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	31.75	1.250
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	3.17 MIN.	0.124 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.

M72B-50A50

4 Byte SIMM
[Hyper Page (EDO)]

NEC

CMOS INTEGRATED CIRCUIT

MC-421000F32

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-421000F32 is a 1,048,576 words by 32 bits dynamic RAM module on which 2 pieces of 16M DRAM: μPD4218165 are assembled.

These modules provide hige density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 1,048,576 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-421000F32-60	60 ns	104 ns	25 ns	1,760 mW	11 mW
MC-421000F32-70	70 ns	124 ns	30 ns	1,650 mW	(CMOS level input)

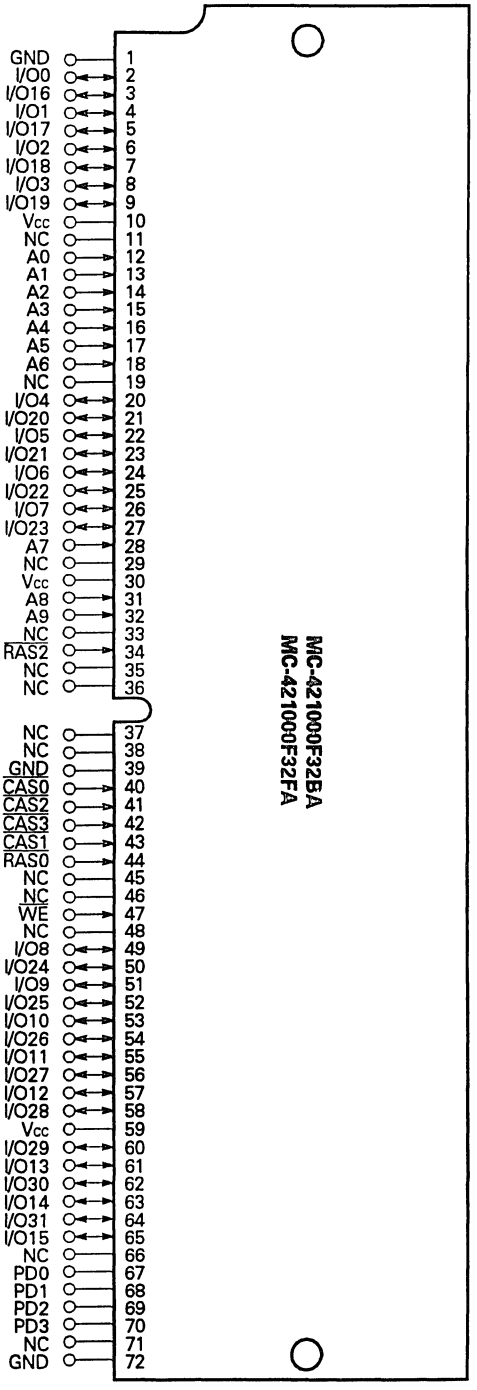
- 1,024 refresh cycle / 16ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000F32BA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating(HAL)	2 pieces of μ PD4218165LE (400mil SOJ) [Single side]
MC-421000F32BA-70	70 ns		
MC-421000F32FA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000F32FA-70	70 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector : Solder coating, Gold plating)



A0-A9	: Address Inputs
I/O0-I/O31	: Data Inputs/Outputs
$\overline{CAS0}$-$\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$,$\overline{RAS2}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access times.

Pin Name	Pin No.	Access Time	
		60ns	70ns
PD0	67	GND	GND
PD1	68	GND	GND
PD2	69	NC	GND
PD3	70	NC	NC

Block Diagram

Remark D0, D1: μPD4218165

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		−1.0 to +7.0	V
Supply Voltage	V_{CC}		−1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		2	W
Operating Ambient Temperature	T_A		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Caution **Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.** Exposure to **Absolute Maximum Rating conditions for extended periods may affect device reliability.**

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		V_{CC} +1.0	V
Low Level Input Voltage	V_{IL}		−1.0		+0.8	V
Operating Ambient Temperature	T_A		0		70	°C

Capacitance (T_a = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	A0 - A9			30	pF
	C_{I2}	$\overline{WE}$			34	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			22	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			22	
Data Input/Output Capacitance	$C_{I/O}$	I/O0 - I/O31			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

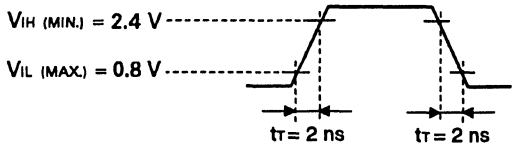
Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		320	mA	1,2,3
			t_{RAC} = 70 ns		300		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$, I_O = 0 mA			4	mA	
		$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$ – 0.2 V, I_O = 0 mA			2		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geqq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		320	mA	1,2,3,4
			t_{RAC} = 70 ns		300		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$ $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		220	mA	1,2,5
			t_{RAC} = 70 ns		200		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		320	mA	1,2
			t_{RAC} = 70 ns		300		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

Notes
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).
2. Specified values are obtained with outputs unloaded.
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

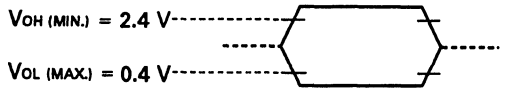
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTLs.

Common to Read, Write Cycle

Parameter	Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tRC	104	—	124	—	ns	
$\overline{RAS}$ Precharge Time	tRP	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	tCPN	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	tRAS	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width	tCAS	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	tCSH	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	—	5	—	ns	2
Row Address Setup Time	tASR	0	—	0	—	ns	
Row Address Hold Time	tRAH	10	—	10	—	ns	
Column Address Setup Time	tASC	0	—	0	—	ns	
Column Address Hold Time	tCAH	10	—	12	—	ns	
$\overline{CAS}$ to Data Setup Time	tCLZ	0	—	0	—	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
Refresh Time	tREF	—	16	—	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	18	ns	1
Access Time from Column Address	t_{AA}	—	30	—	35	ns	1
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	—	10	—	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	—	0	—	ns	1
Data-in Setup Time	t_{DS}	0	—	0	—	ns	2
Data-in Hold Time	t_{DH}	10	—	10	—	ns	2

Notes 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

2. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	—	30	—	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125 000	70	125000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	ns	
Data Output Hold Time	t_{DHC}	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	2,3
$\overline{WE}$ Pulse Width	t_{WPZ}	10	—	10	—	ns	3
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	2.3
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	2.3

Notes 1. $t_{HPC(MIN.)}$ is applied to access time from $\overline{CAS}$

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ as follows. The effective specification depends on state of each signal.

   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are Inactive (at the end of read cycle)

   $\overline{WE}$: inactive

   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive(at the end of read cycle)

   $\overline{WE}$: active and either t_{RRH} or t_{RCH} must be met··· t_{WEZ} and t_{WPZ} is effective.

Refresh Cycle

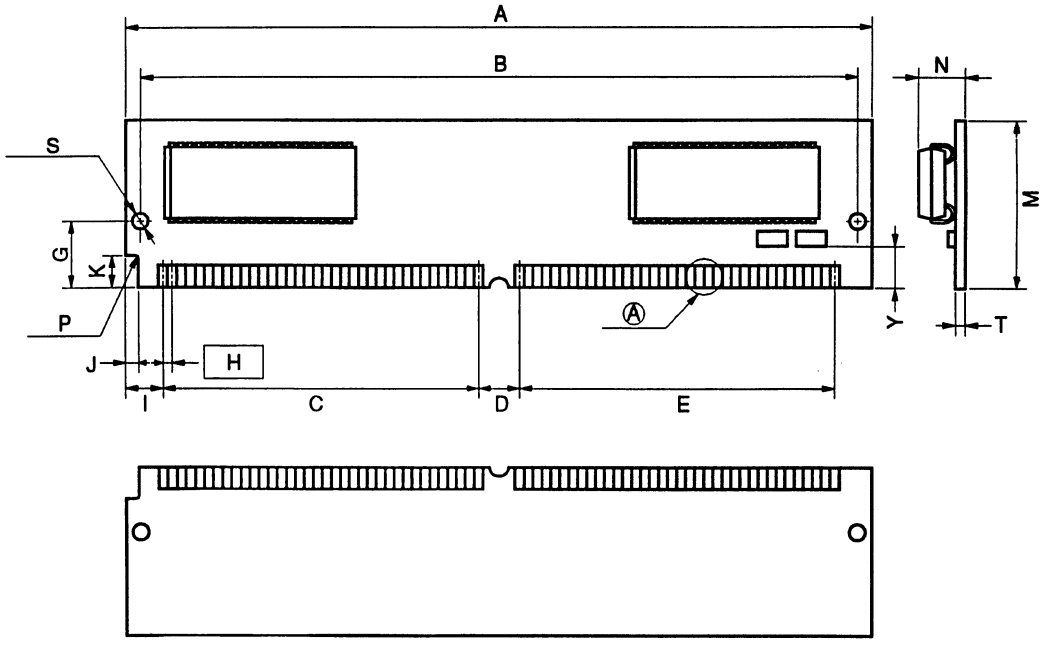
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	—	5	—	ns	
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t_{WHR}	15	—	15	—	ns	

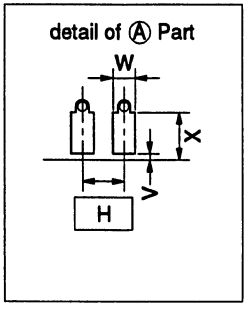
Timing Chart

Please refer to Timing Chart 3, page 385.

Package Drawings

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.

M72B-50A46

NEC

CMOS INTEGRATED CIRCUIT

MC-422000F32

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-422000F32 is a 2,097,152 words by 32 bits dynamic RAM module on which 4 pieces of 16M DRAM: μPD4218165 are assembied.

These modules provide hige density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-422000F32-60	60 ns	104 ns	25 ns	1,782 mW	22 mW (CMOS level input)
MC-422000F32-70	70 ns	124 ns	30 ns	1,122 mW	

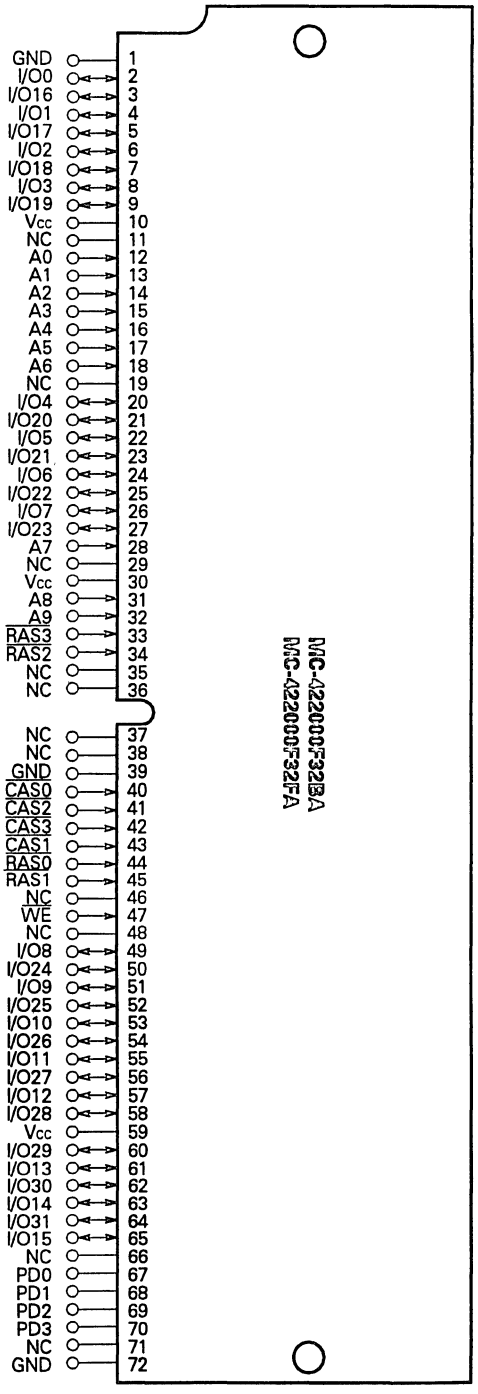
- 1,024 refresh cycle / 16ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000F32BA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating(HAL)	4 pieces of μ PD4218165LE (400mil SOJ) [Single side]
MC-422000F32BA-70	70 ns		
MC-422000F32FA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-422000F32FA-70	70 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector : Solder coating, Gold plating)



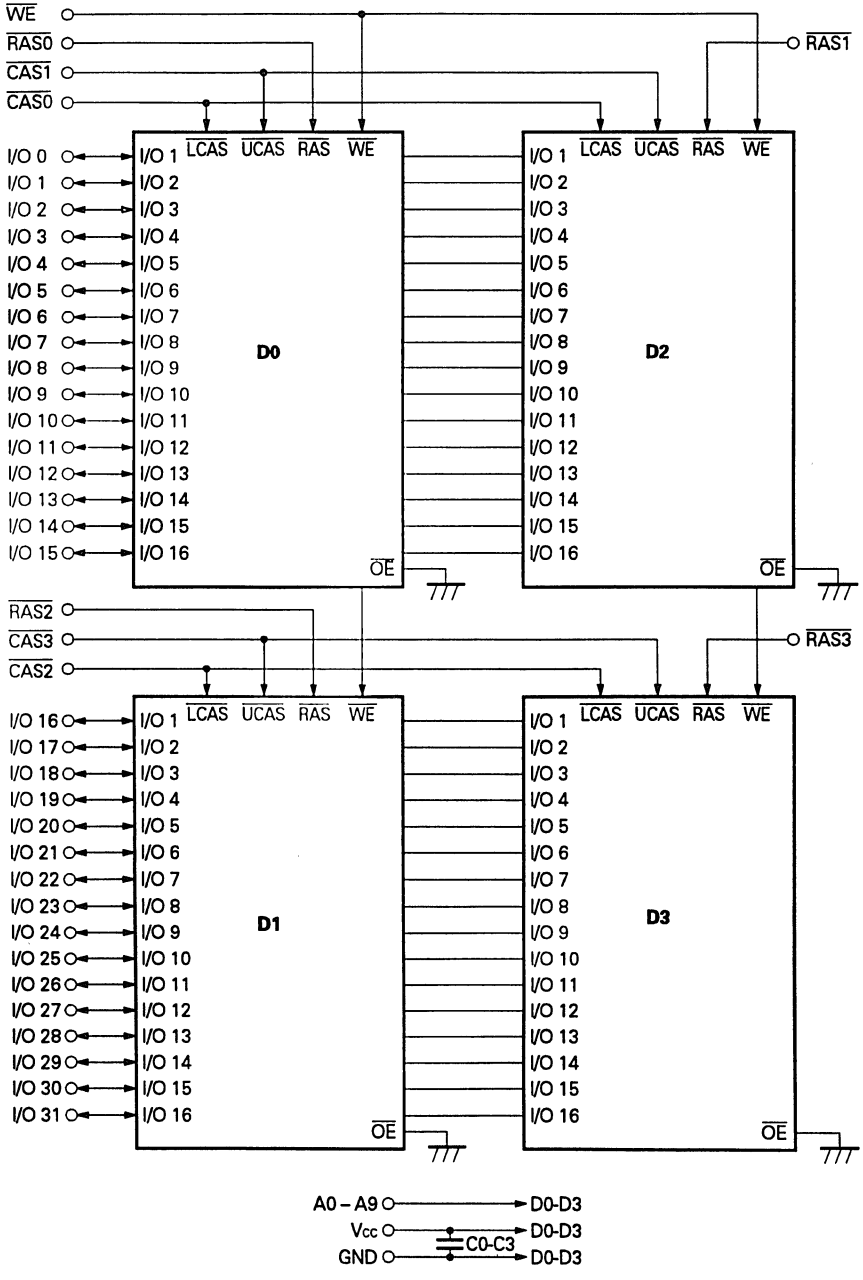
A0-A9	: Address Inputs
I/O0-I/O31	: Data Inputs/Outputs
$\overline{CAS0}$-$\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$-$\overline{RAS3}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access times.

Pin Name	Pin No.	Access Time	
		60ns	70ns
PD0	67	NC	NC
PD1	68	NC	NC
PD2	69	NC	GND
PD3	70	NC	NC

Block Diagram

Remark D0-D3 : μPD4218165



Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		−1.0 to +7.0	V
Supply Voltage	V_{CC}		−1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		4	W
Operating Ambient Temperature	T_A		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		V_{CC} +1.0	V
Low Level Input Voltage	V_{IL}		−1.0		+0.8	V
Operating Ambient Temperature	T_A		0		70	°C

Capacitance (T_a = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	A0 - A9			40	pF
	C_{I2}	$\overline{WE}$			48	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			22	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data Input/Output Capacitance	$C_{I/O}$	I/O0 - I/O31			26	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

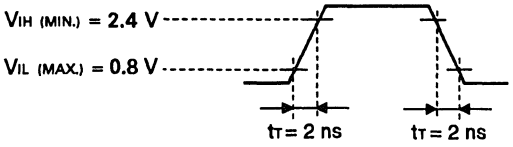
Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		324	mA	1,2,3
			t_{RAC} = 70 ns		304		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$, I_O = 0 mA			8	mA	
		$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$ – 0.2 V, I_O = 0 mA			4		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geqq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		324	mA	1,2,3,4
			t_{RAC} = 70 ns		304		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$ $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		224	mA	1,2,5
			t_{RAC} = 70 ns		204		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		324	mA	1,2
			t_{RAC} = 70 ns		304		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage Low	V_{OH}	I_O = –2.5 mA		2.4		V	
level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

Notes
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).
2. Specified values are obtained with outputs unloaded.
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

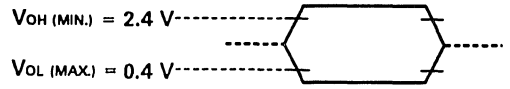
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTLs.

Common to Read, Write Cycle

Parameter	Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tRC	104	—	124	—	ns	
$\overline{RAS}$ Precharge Time	tRP	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	tCPN	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	tRAS	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width	tCAS	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	tCSH	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	—	5	—	ns	2
Row Address Setup Time	tASR	0	—	0	—	ns	
Row Address Hold Time	tRAH	10	—	10	—	ns	
Column Address Setup Time	tASC	0	—	0	—	ns	
Column Address Hold Time	tCAH	10	—	12	—	ns	
$\overline{CAS}$ to Data Setup Time	tCLZ	0	—	0	—	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
Refresh Time	tREF	—	16	—	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	18	ns	1
Access Time from Column Address	t_{AA}	—	30	—	35	ns	1
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	—	10	—	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	—	0	—	ns	1
Data-in Setup Time	t_{DS}	0	—	0	—	ns	2
Data-in Hold Time	t_{DH}	10	—	10	—	ns	2

Notes 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

2. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	—	30	—	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125 000	70	125000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	ns	
Data Output Hold Time	t_{DHC}	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	2,3
$\overline{WE}$ Pulse Width	t_{WPZ}	10	—	10	—	ns	3
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	2.3
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	2.3

Notes 1. $t_{HPC(MIN.)}$ is applied to access time from $\overline{CAS}$

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.
3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ as follows. The effective specification depends on state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are Inactive (at the end of read cycle)
   $\overline{WE}$: inactive
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive(at the end of read cycle)
   $\overline{WE}$: active and either t_{RRH} or t_{RCH} must be met··· t_{WEZ} and t_{WPZ} is effective.

Refresh Cycle

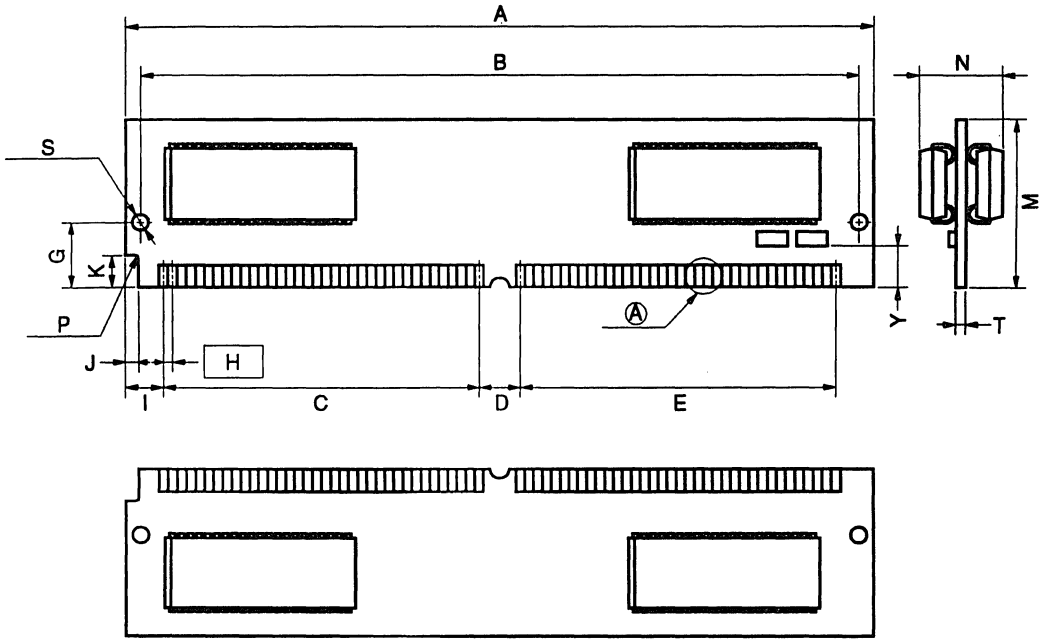
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	—	5	—	ns	
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t_{WHR}	15	—	15	—	ns	

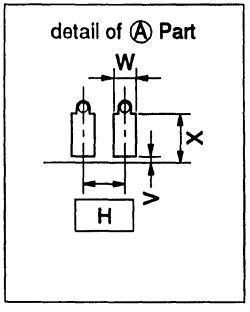
Timing Chart

Please refer to Timing Chart 3, page 385.

Package Drawings

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	φ3.18	φ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.

M72B-50A45

NEC

CMOS INTEGRATED CIRCUIT

MC-424000F32

4 M-WORD BY 32-BIT DYNAMIC RAM MODULE
HYPER PAGE MODE (EDO)

Description

The MC-424000F32 is a 4,194,304 words by 32 bits dynamic RAM module on which 8 pieces of 16M DRAM: μPD4217405 are assembied.

These modules provide hige density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 4,194,304 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-424000F32-60	60 ns	104 ns	25 ns	4,840 mW	44 mW (CMOS level input)
MC-424000F32-70	70 ns	124 ns	30 ns	4,400 mW	

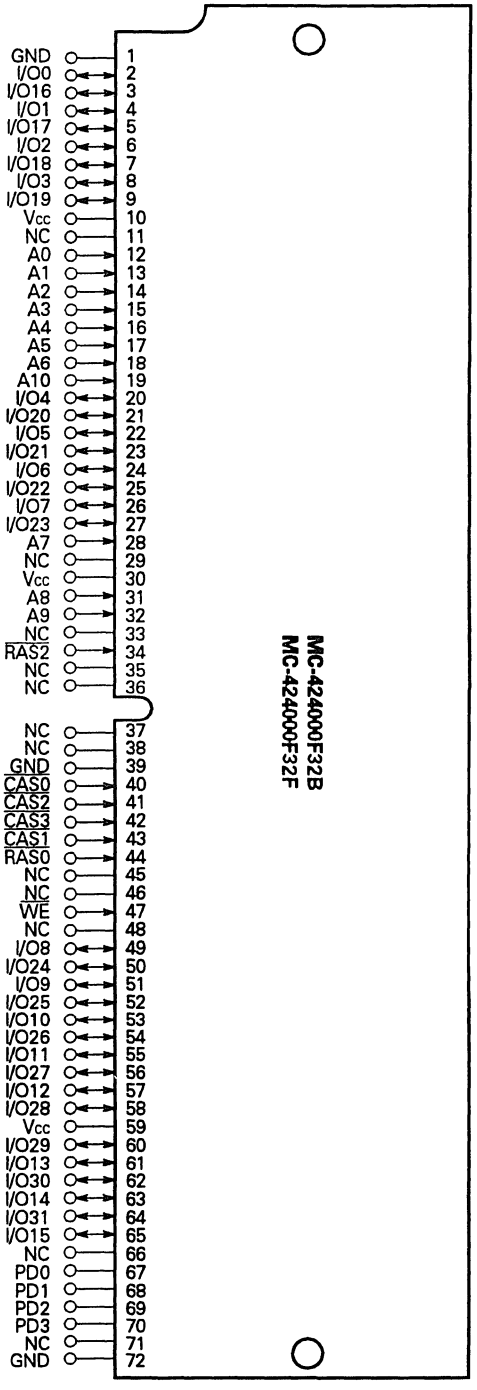
- 2,048 refresh cycle / 32ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000F32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating(HAL)	8 pieces of μ PD4217405LA (300mil SOJ) [Single side]
MC-424000F32B-70	70 ns		
MC-424000F32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-424000F32F-70	70 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector : Solder coating, Gold plating)

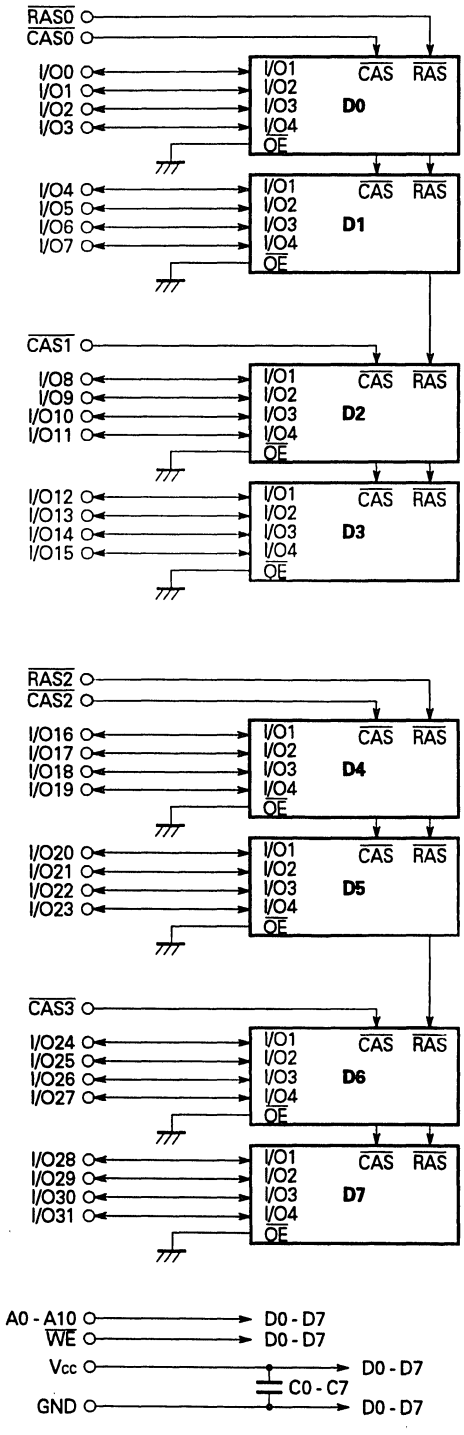


A0-A10	: Address Inputs
I/O0-I/O31	: Data Inputs/Outputs
$\overline{CAS0}$-$\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$,$\overline{RAS2}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access times.

Pin Name	Pin No.	Access Time	
		60ns	70ns
PD0	67	GND	GND
PD1	68	NC	NC
PD2	69	NC	GND
PD3	70	NC	NC

Block Diagram



Remark D0 - D7 : μPD4217405

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		−1.0 to +7.0	V
Supply Voltage	V_{CC}		−1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		8	W
Operating Ambient Temperature	T_A		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		V_{CC} +1.0	V
Low Level Input Voltage	V_{IL}		−1.0		+0.8	V
Operating Ambient Temperature	T_A		0		70	°C

Capacitance (T_a = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	A0 - A10			68	pF
	C_{I2}	$\overline{WE}$			76	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			43	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data Input/Output Capacitance	$C_{I/O}$	I/O0 - I/O31			17	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

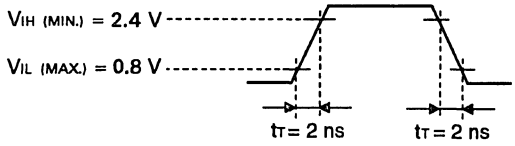
Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		880	mA	1,2,3
			t_{RAC} = 70 ns		800		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$, I_O = 0 mA			16	mA	
		$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$ – 0.2 V, I_O = 0 mA			8		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geqq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		880	mA	1,2,3,4
			t_{RAC} = 70 ns		800		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$ $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		720	mA	1,2,5
			t_{RAC} = 70 ns		640		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		880	mA	1,2
			t_{RAC} = 70 ns		800		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

Notes
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).
2. Specified values are obtained with outputs unloaded.
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

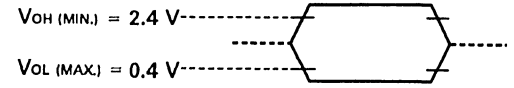
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 2 TTLs.

Common to Read, Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{RC}	104	—	124	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	ns	2
Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	10	—	12	—	ns	
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	1	50	1	50	ns	
Refresh Time	t_{REF}	—	16	—	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	18	ns	1
Access Time from Column Address	t_{AA}	—	30	—	35	ns	1
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	—	10	—	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	—	0	—	ns	1
Data-in Setup Time	t_{DS}	0	—	0	—	ns	2
Data-in Hold Time	t_{DH}	10	—	10	—	ns	2

Notes 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

2. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	—	30	—	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125 000	70	125000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	ns	
Data Output Hold Time	t_{DHC}	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	2,3
$\overline{WE}$ Pulse Width	t_{WPZ}	10	—	10	—	ns	3
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	2.3
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	2.3

Notes 1. $t_{HPC(MIN.)}$ is applied to access time from $\overline{CAS}$

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are Inactive (at the end of read cycle)

$\overline{WE}$: inactive

t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive(at the end of read cycle)

$\overline{WE}$: active and either t_{RRH} or t_{RCH} must be met··· t_{WEZ} and t_{WPZ} is effective.

Refresh Cycle

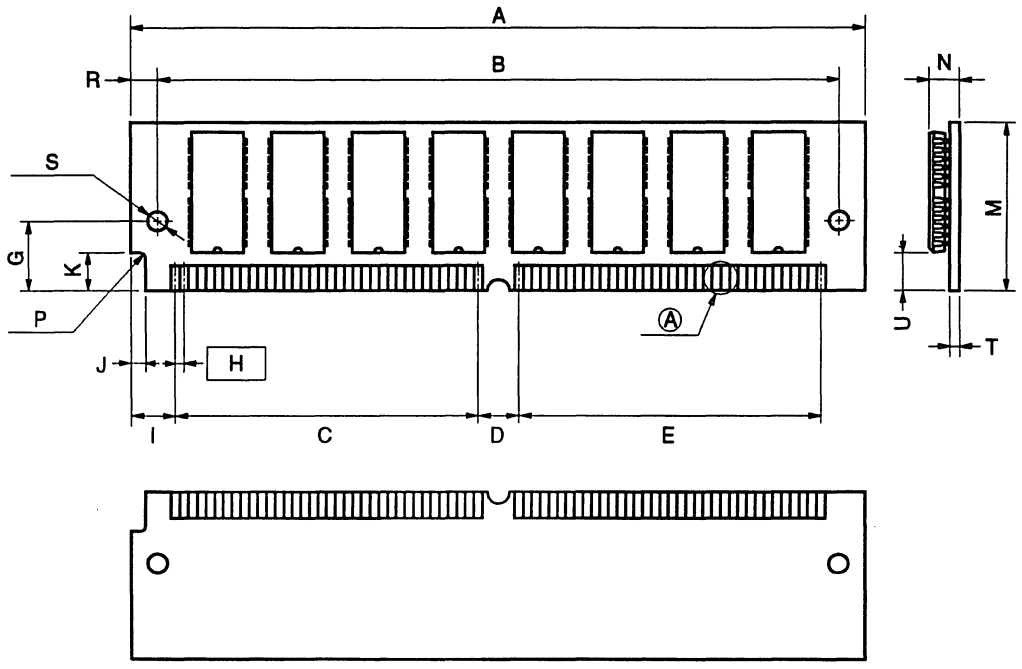
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	—	5	—	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	—	15	—	ns	
$\overline{WE}$ Setup Time	t_{WSR}	10	—	10	—	ns	

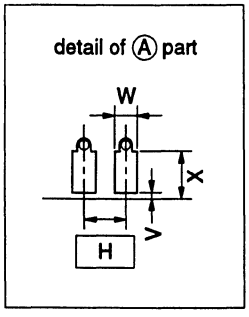
Timing Chart

Please refer to Timing Chart 4, page 397.

Package Drawings

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	$3.984^{+0.005}_{-0.006}$
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
R	3.38±0.13	$0.133^{+0.006}_{-0.005}$
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.5 MIN.	0.216 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A54

NEC

CMOS INTEGRATED CIRCUIT

MC-428000F32

8 M-WORD BY 32-BIT DYNAMIC RAM MODULE
HYPER PAGE MODE (EDO)

Description

The MC-428000F32 is a 8,388,608 words by 32 bits dynamic RAM module on which 16 pieces of 16M DRAM: μPD4217405 are assembled.

These modules provide hige density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 8,388,608 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-428000F32-60	60 ns	104 ns	25 ns	5,170 mW	88 mW (CMOS level input)
MC-428000F32-70	70 ns	124 ns	30 ns	4,730 mW	

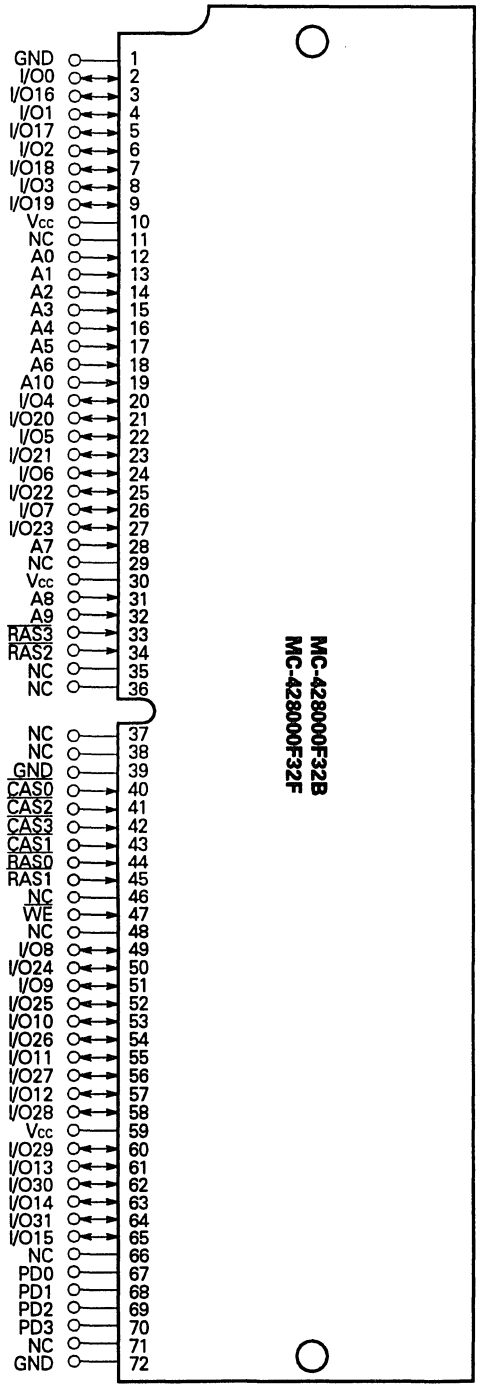
- 2,048 refresh cycle / 32ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-428000F32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating(HAL)	16 pieces of μ PD4217405LA (300mil SOJ) [Single side]
MC-428000F32B-70	70 ns		
MC-428000F32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-428000F32F-70	70 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector : Solder coating, Gold plating)

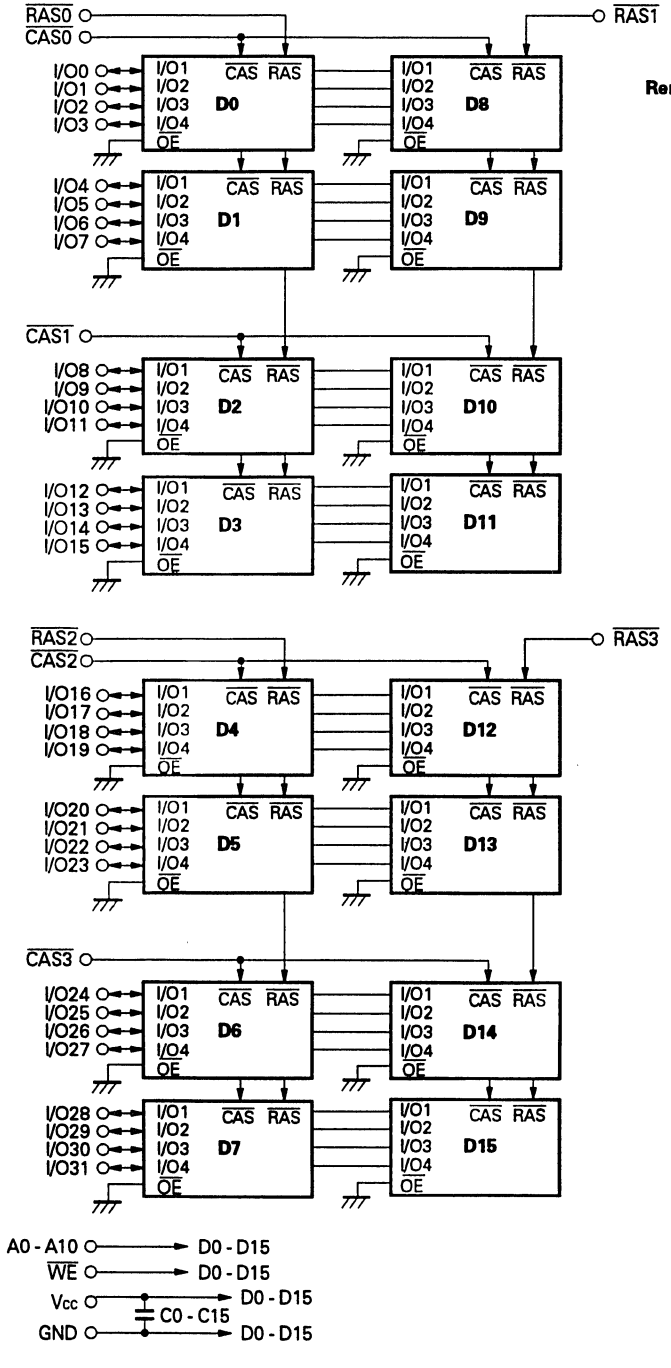


A0-A10	: Address Inputs
I/O0-I/O31	: Data Inputs/Outputs
$\overline{CAS0}$-$\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$-$\overline{RAS3}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access times.

Pin Name	Pin No.	Access Time	
		60ns	70ns
PD0	67	NC	NC
PD1	68	GND	GND
PD2	69	NC	GND
PD3	70	NC	NC

Block Diagram



Remark D0 - D15: μPD4217405

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		−1.0 to +7.0	V
Supply Voltage	V_{CC}		−1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		16	W
Operating Ambient Temperature	T_A		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		V_{CC} +1.0	V
Low Level Input Voltage	V_{IL}		−1.0		+0.8	V
Operating Ambient Temperature	T_A		0		70	°C

Capacitance (T_a = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	A0 - A10			121	pF
	C_{I2}	$\overline{WE}$			137	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			48	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			48	
Data Input/Output Capacitance	$C_{I/O}$	I/O0 - I/O31			29	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	1,2,3
			t_{RAC} = 70 ns		860		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$, I_O = 0 mA			32	mA	
		$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$ – 0.2 V, I_O = 0 mA			16		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geqq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	1,2,3,4
			t_{RAC} = 70 ns		860		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$ $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		780	mA	1,2,5
			t_{RAC} = 70 ns		700		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	1,2
			t_{RAC} = 70 ns		860		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.

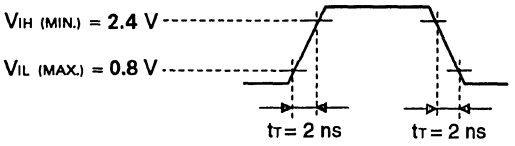
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

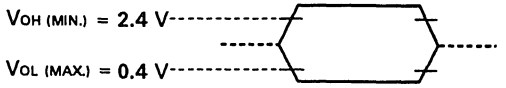
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 2 TTLs.

Common to Read, Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{RC}	104	—	124	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	ns	2
Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	10	—	12	—	ns	
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	1	50	1	50	ns	
Refresh Time	t_{REF}	—	16	—	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	18	ns	1
Access Time from Column Address	t_{AA}	—	30	—	35	ns	1
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	—	10	—	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	—	0	—	ns	1
Data-in Setup Time	t_{DS}	0	—	0	—	ns	2
Data-in Hold Time	t_{DH}	10	—	10	—	ns	2

Notes 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

2. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	—	30	—	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125 000	70	125000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	ns	
Data Output Hold Time	t_{DHC}	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	2,3
$\overline{WE}$ Pulse Width	t_{WPZ}	10	—	10	—	ns	3
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	2.3
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	2.3

Notes 1. $t_{HPC(MIN.)}$ is applied to access time from $\overline{CAS}$

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are Inactive (at the end of read cycle)

$\overline{WE}$: inactive

t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive(at the end of read cycle)

$\overline{WE}$: active and either t_{RRH} or t_{RCH} must be met··· t_{WEZ} and t_{WPZ} is effective.

Refresh Cycle

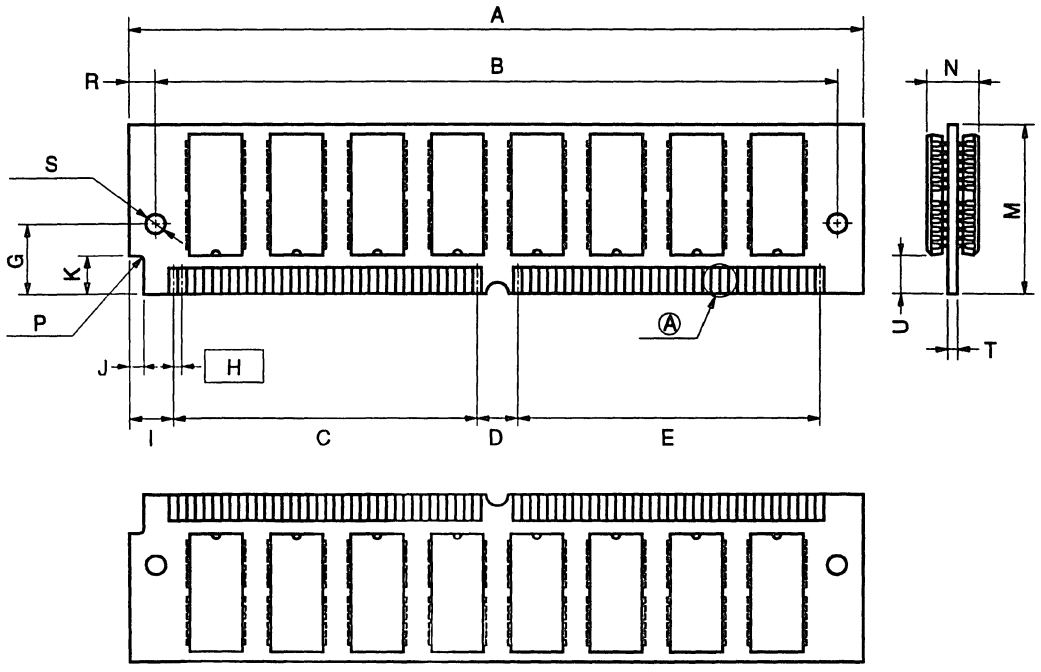
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	—	5	—	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	—	15	—	ns	
$\overline{WE}$ Setup Time	t_{WSR}	10	—	10	—	ns	

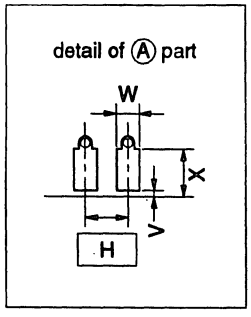
Timing Chart

Please refer to Timing Chart 4, page 397.

Package Drawings

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	$3.984^{+0.005}_{-0.006}$
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
R	3.38±0.13	$0.133^{+0.006}_{-0.005}$
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.5 MIN.	0.216 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A55

Small Outline DIMM

NEC

MOS INTEGRATED CIRCUIT

MC-42S1000LAD32S SERIES

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S1000LAD32S series is a 1,048,576 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 2 pieces of 16 M DRAM: μPD42S18160L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 1,048,576 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S1000LAD32S-A60	60 ns	110 ns	1,080 mW	1.08 mW (CMOS level input)
MC-42S1000LAD32S-A70	70 ns	130 ns	1,008 mW	
MC-42S1000LAD32S-A80	80 ns	150 ns	936 mW	

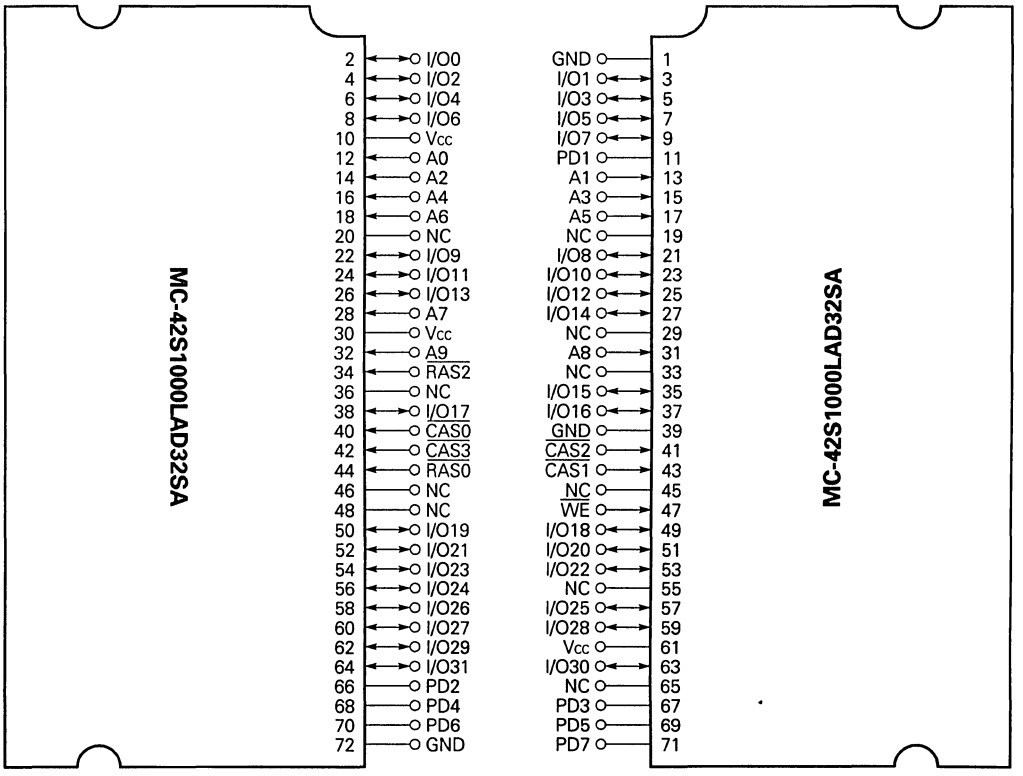
- 1,024 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S1000LAD32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	2 pieces of μPD42S18160LG5 (400 mil TSOP (II)) [Single side]
MC-42S1000LAD32SA-A70	70 ns		
MC-42S1000LAD32SA-A80	80 ns		

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



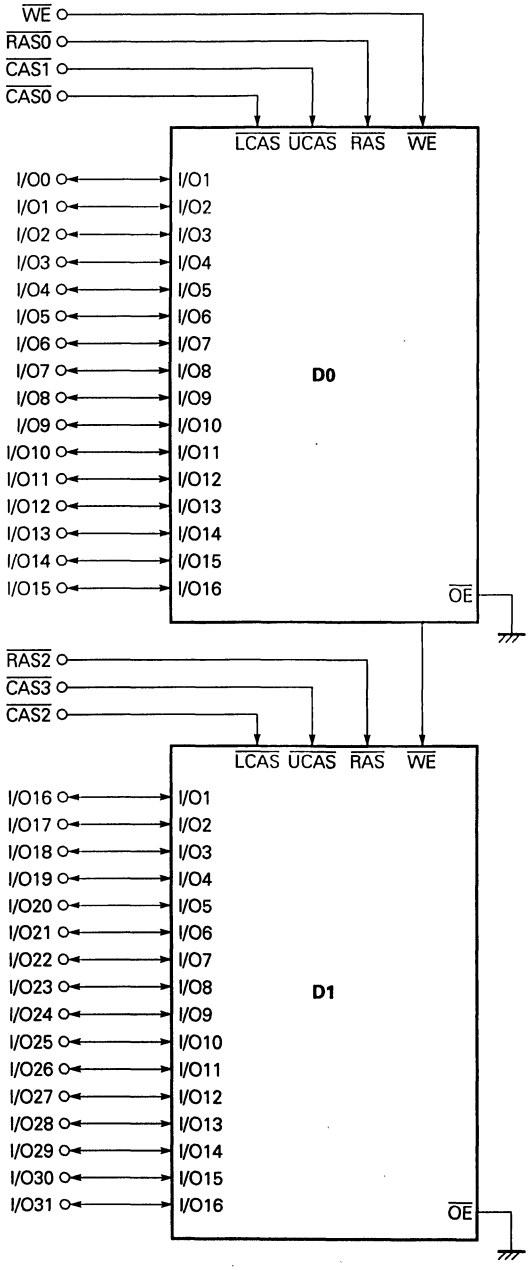
A0 - A9	:	Address Inputs
I/O0 - I/O31	:	Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$	:	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
PD1 - PD7	:	Presence Detect Pins
Vcc	:	Power Supply
GND	:	Ground
NC	:	No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	NC	NC	NC
PD2	66	GND	GND	GND
PD3	67	GND	GND	GND
PD4	68	NC	NC	NC
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram

Remark D0, D1 : μPD42S18160L (TSOP (II))



Electrical Specifications [Notes 1, 2]

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		2	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			29	pF
	C_{I2}	$\overline{WE}$			29	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			23	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			17	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			12	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		300	mA	3, 4, 7
			t_{RAC} = 70 ns		280		
			t_{RAC} = 80 ns		260		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		1.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		0.3		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		300	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		280		
			t_{RAC} = 80 ns		260		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		180	mA	3, 4, 6
			t_{RAC} = 70 ns		160		
			t_{RAC} = 80 ns		140		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		300	mA	3, 4
			t_{RAC} = 70 ns		280		
			t_{RAC} = 80 ns		260		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 125.0 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} –0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ –0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		360	μA	3, 4
$\overline{CAS}$ before $\overline{RAS}$ self refresh current	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} –0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			300	μA	4
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

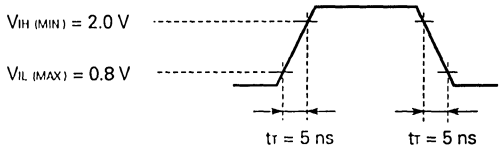
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RPS}	110		130		150		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{CHS}	-50		-50		-50		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		128		128		128	ms	

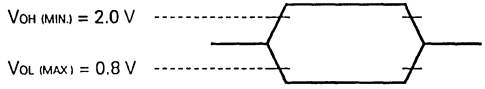
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

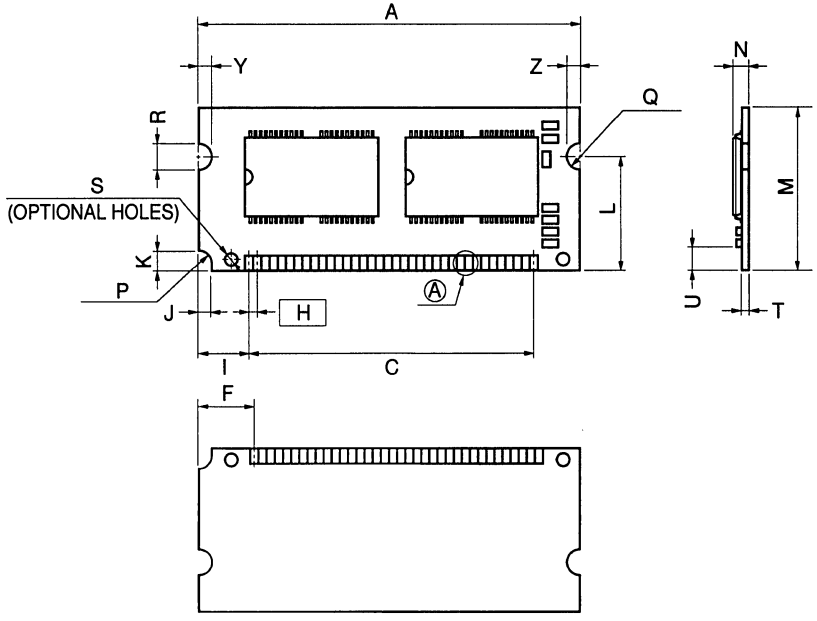
    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 1 TTL and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}$/$\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

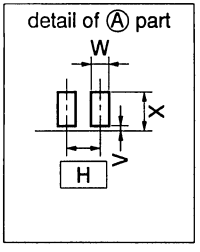
Timing Chart

Please refer to Timing Chart 5, page 409.

Package Drawing

72 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.0	0.079
K	3.18	0.125
L	17.78	0.700
M	25.4	1.000
N	2.45 MAX.	0.097 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ1.8	ϕ0.071
T	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U	3.18 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54 MIN.	0.100 MIN.
Y	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.

M72S-50A4

NEC

MOS INTEGRATED CIRCUIT

MC-42S2000LAB32S SERIES

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S2000LAB32S series is a 2,097,152 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 4 pieces of 16 M DRAM: μPD42S17800L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S2000LAB32S-A60	60 ns	110 ns	1,440 mW	2.16 mW (CMOS level input)
MC-42S2000LAB32S-A70	70 ns	130 ns	1,296 mW	
MC-42S2000LAB32S-A80	80 ns	150 ns	1,152 mW	

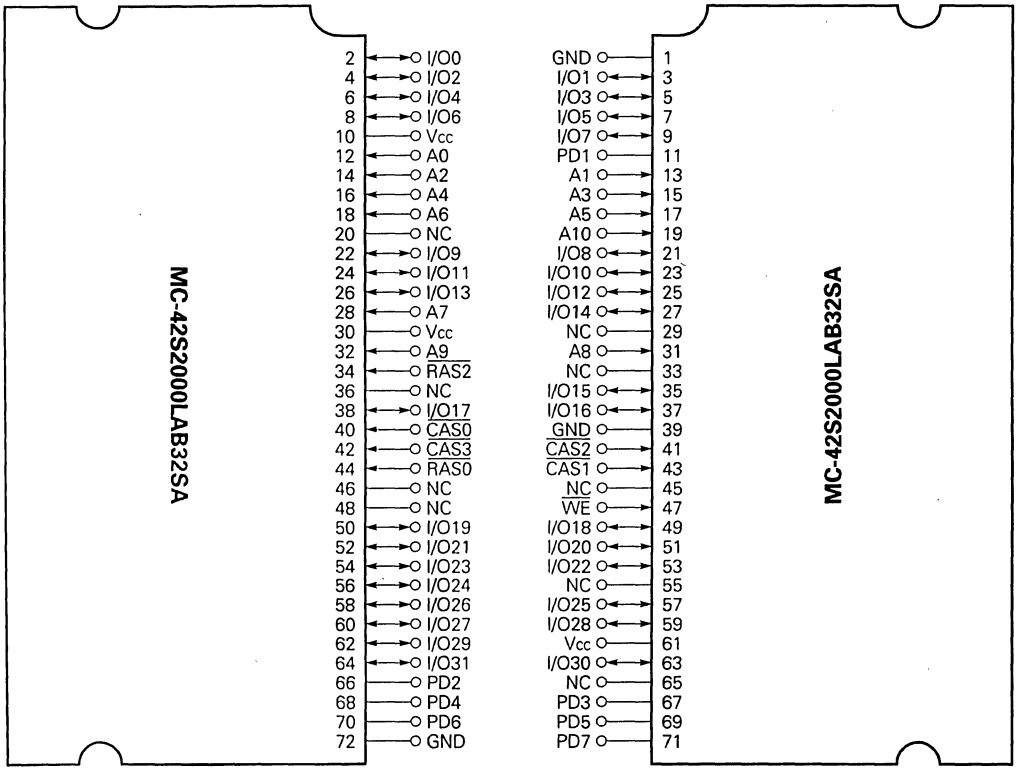
- 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S2000LAB32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μPD42S17800LG5 (400 mil TSOP (II)) [Single side]
MC-42S2000LAB32SA-A70	70 ns		
MC-42S2000LAB32SA-A80	80 ns		

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)

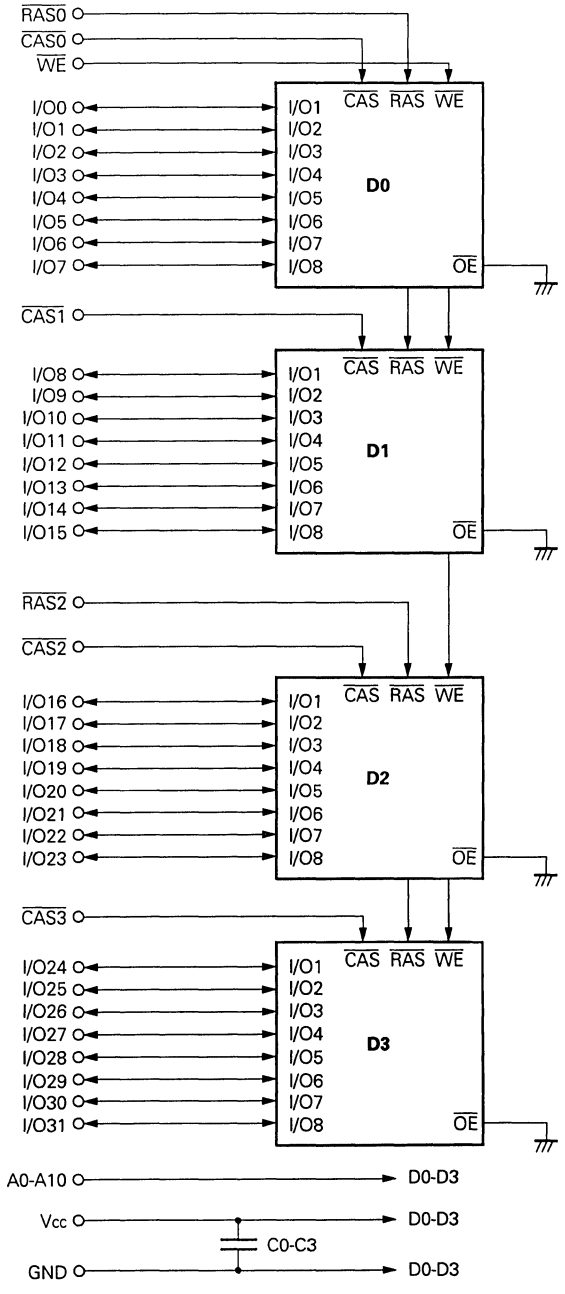


A0 - A10	: Address Inputs
I/O0 - I/O31	: Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$	: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{WE}$	: Write Enable
PD1 - PD7	: Presence Detect Pins
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	GND	GND	GND
PD2	66	NC	NC	NC
PD3	67	GND	GND	GND
PD4	68	NC	NC	NC
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram



Remark D0-D3 : μPD42S17800LG5 (TSOP (II))

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		4	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			35	pF
	C_{I2}	$\overline{WE}$			43	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			30	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			17	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			12	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		400	mA	3, 4, 7
			t_{RAC} = 70 ns		360		
			t_{RAC} = 80 ns		320		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		2.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		0.6		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		400	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		360		
			t_{RAC} = 80 ns		320		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		280	mA	3, 4, 6
			t_{RAC} = 70 ns		240		
			t_{RAC} = 80 ns		200		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		400	mA	3, 4
			t_{RAC} = 70 ns		360		
			t_{RAC} = 80 ns		320		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} –0.2 V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$ 0 V ≤ $V_{IL} \leq$ 0.2 V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ –0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq$ 1 μs		800	μA	3, 4
$\overline{CAS}$ before $\overline{RAS}$ self refresh current	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} –0.2 V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$ 0 V ≤ $V_{IL} \leq$ 0.2 V I_O = 0 mA			600	μA	4
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

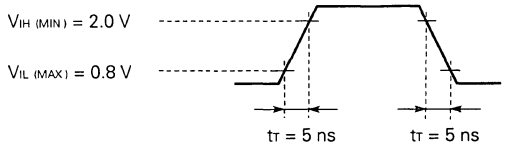
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RPS}	110		130		150		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{CHS}	–50		–50		–50		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		128		128		128	ms	

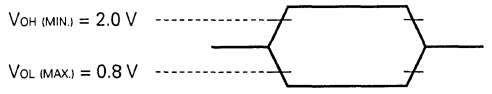
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

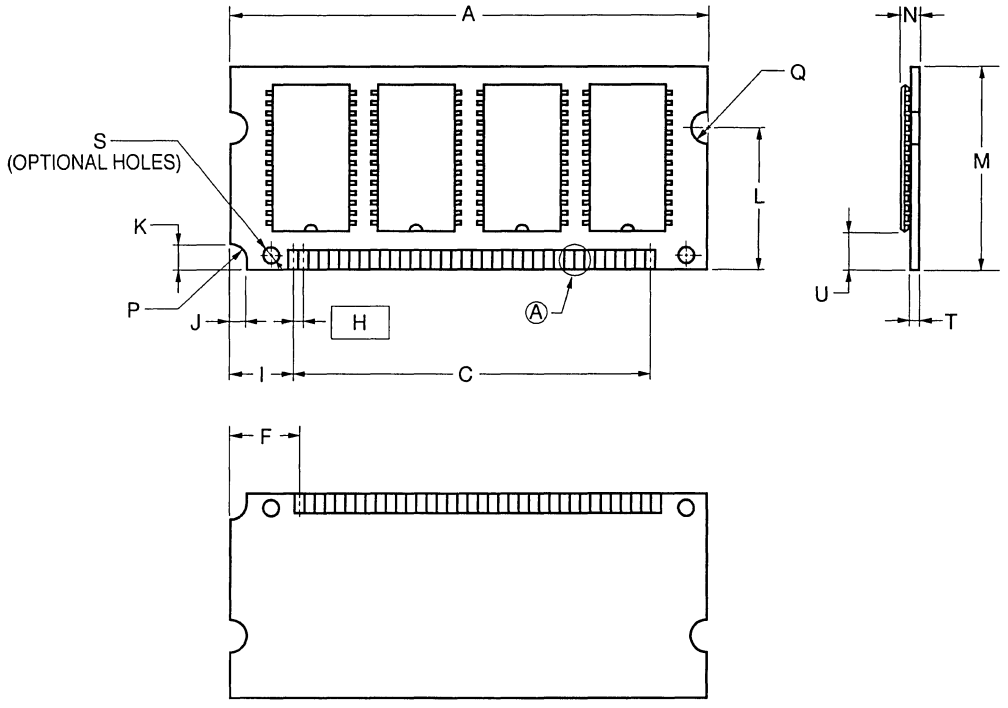
    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 1 TTL and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}$/$\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

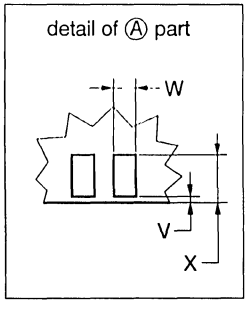
Timing Chart

Please refer to Timing Chart 6, page 419.

Package Drawing

72PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.03±0.13	$0.080^{+0.005}_{-0.006}$
K	3.175±0.13	0.125±0.006
L	17.78	0.700
M	25.4±0.13	1.000±0.006
N	2.463 MAX.	0.097 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
S	ϕ1.8	ϕ0.071
T	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U	3.175 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72S-50A1-2

NEC

MOS INTEGRATED CIRCUIT

MC-42S2000LAD32S SERIES

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S2000LAD32S series is a 2,097,152 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 4 pieces of 16 M DRAM: μPD42S18160L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S2000LAD32S-A60	60 ns	110 ns	1,083.6 mW	2.16 mW (CMOS level input)
MC-42S2000LAD32S-A70	70 ns	130 ns	1,011.6 mW	
MC-42S2000LAD32S-A80	80 ns	150 ns	939.6 mW	

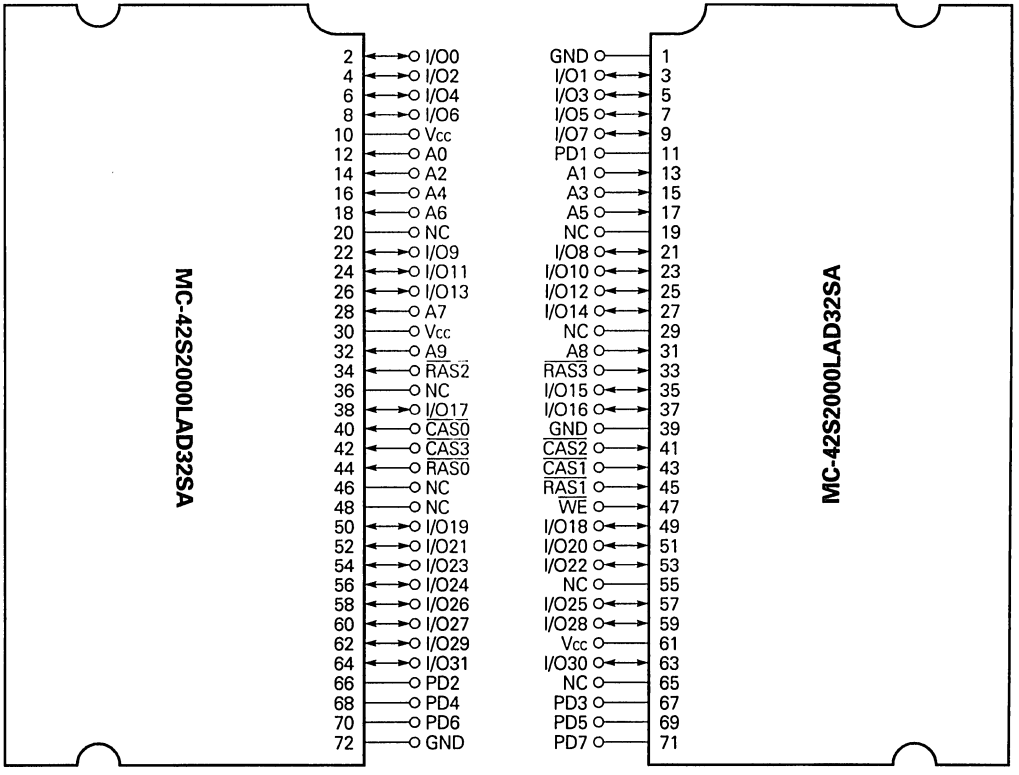
- 1,024 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S2000LAD32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μPD42S18160LG5 (400 mil TSOP (II)) [Double side]
MC-42S2000LAD32SA-A70	70 ns		
MC-42S2000LAD32SA-A80	80 ns		

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)

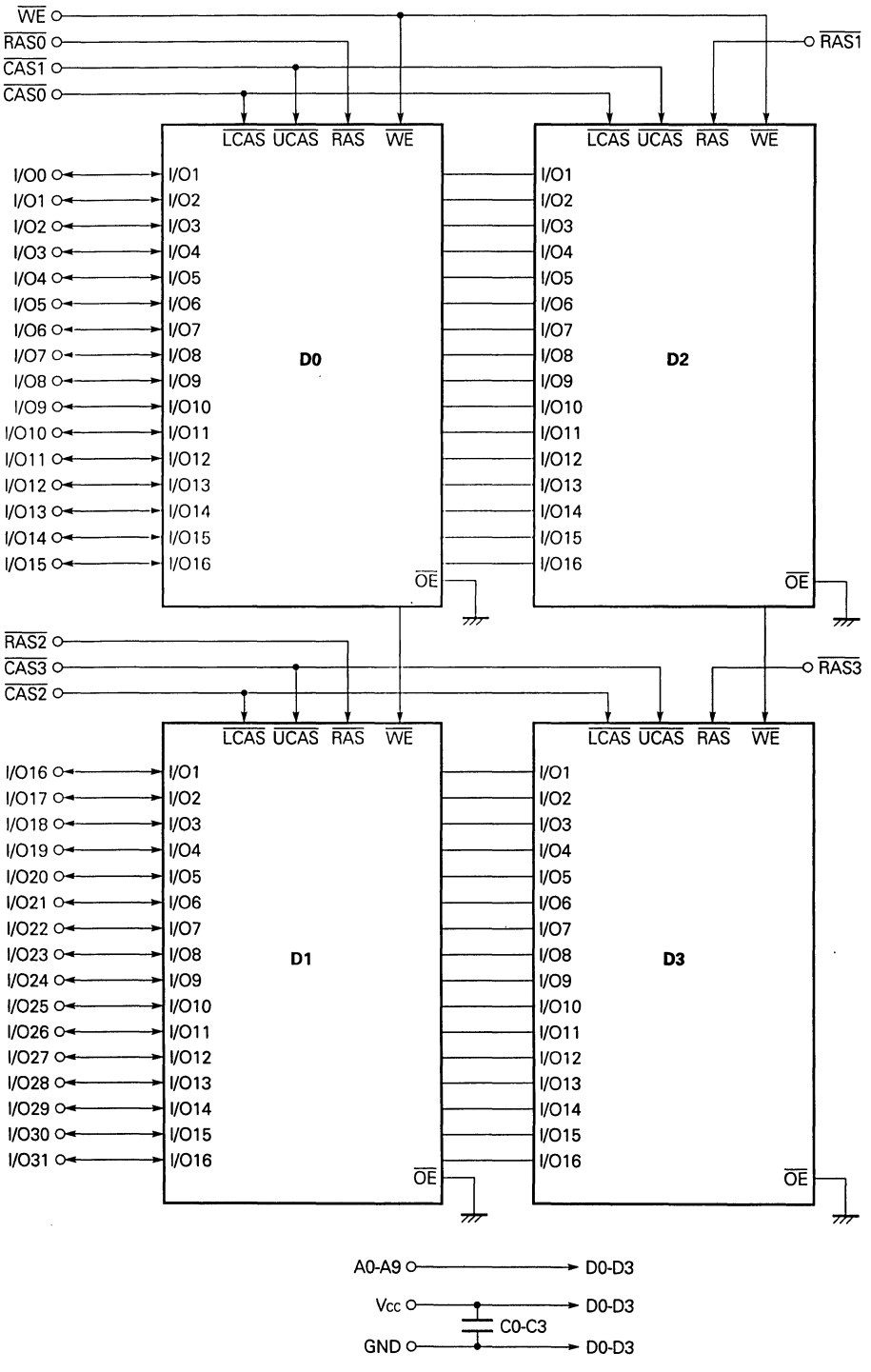


A0 - A9	: Address Inputs
I/O0 - I/O31	: Data Inputs/Outputs
$\overline{RAS0}$ - $\overline{RAS3}$	: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{WE}$	: Write Enable
PD1 - PD7	: Presence Detect Pins
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD1 – PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	NC	NC	NC
PD2	66	GND	GND	GND
PD3	67	GND	GND	GND
PD4	68	GND	GND	GND
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram



Remark D0-D3 : μPD42S18160LG5 (TSOP (II))

Electrical Specifications [Notes 1, 2]

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 – A9			35	pF
	C_{I2}	$\overline{WE}$			43	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			23	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			24	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			19	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		301	mA	3, 4, 7
			t_{RAC} = 70 ns		281		
			t_{RAC} = 80 ns		261		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		2.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		0.6		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		301	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		281		
			t_{RAC} = 80 ns		261		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		181	mA	3, 4, 6
			t_{RAC} = 70 ns		161		
			t_{RAC} = 80 ns		141		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		301	mA	3, 4
			t_{RAC} = 70 ns		281		
			t_{RAC} = 80 ns		261		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 125.0 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} –0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ –0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		720	μA	3, 4
$\overline{CAS}$ before $\overline{RAS}$ self refresh current	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} –0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			600	μA	4
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

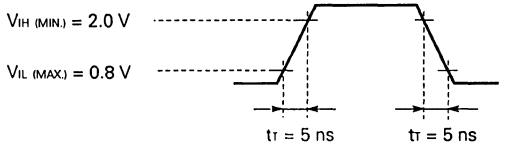
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RPS}	110		130		150		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{CHS}	−50		−50		−50		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		128		128		128	ms	

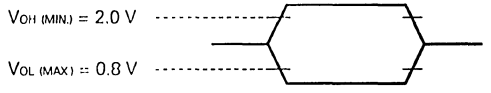
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

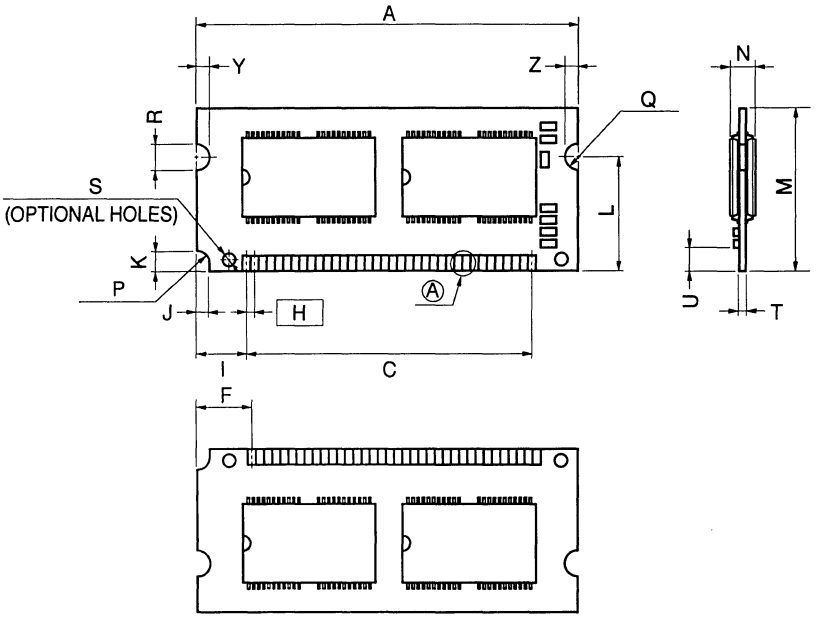
    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 1 TTL and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}$/$\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

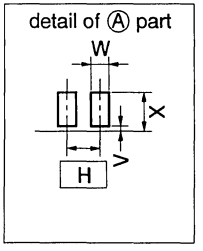
Timing Chart

Please refer to Timing Chart 5, page 409.

Package Drawing

72 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.0	0.079
K	3.18	0.125
L	17.78	0.700
M	25.4	1.000
N	3.8 MAX.	0.150 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ1.8	ϕ0.071
T	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U	3.18 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54 MIN.	0.100 MIN.
Y	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.

M72S-50A3

NEC

MOS INTEGRATED CIRCUIT

MC-42S4000LAB32S SERIES

4 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S4000LAB32S series is a 4,194,304 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 8 pieces of 16 M DRAM: μPD42S17800L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 4,194,304 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S4000LAB32S-A60	60 ns	110 ns	1,458 mW	4.32 mW (CMOS level input)
MC-42S4000LAB32S-A70	70 ns	130 ns	1,314 mW	
MC-42S4000LAB32S-A80	80 ns	150 ns	1,170 mW	

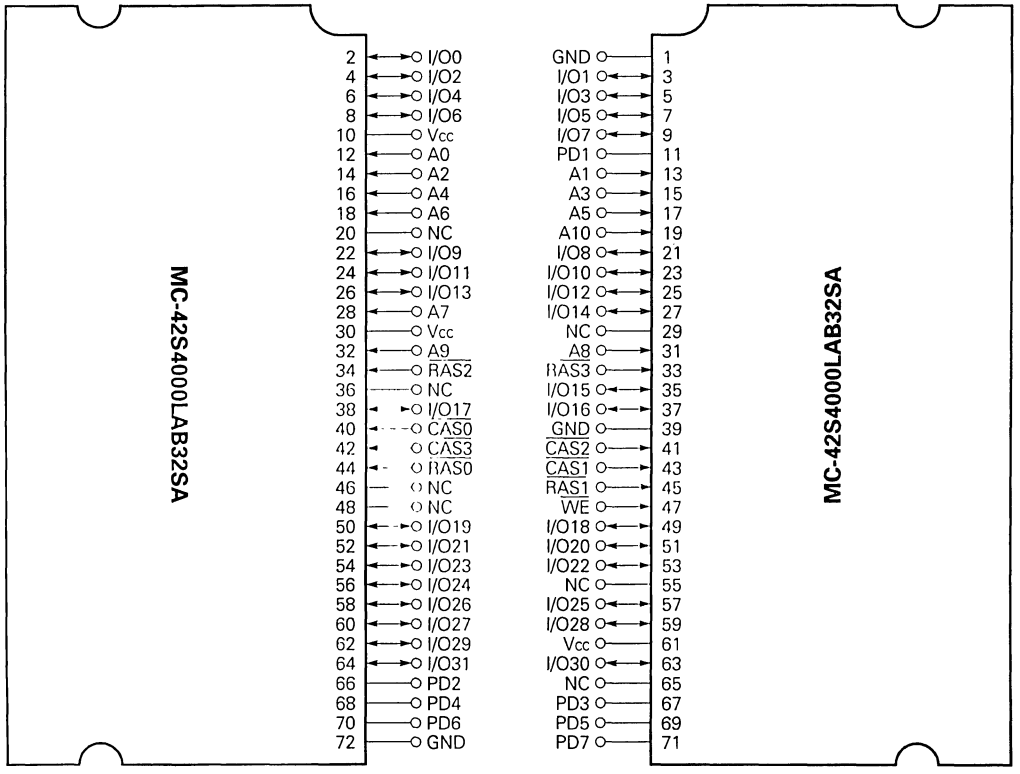
- 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S4000LAB32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	8 pieces of μPD42S17800LG5 (400 mil TSOP (II)) [Double side]
MC-42S4000LAB32SA-A70	70 ns		
MC-42S4000LAB32SA-A80	80 ns		

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)

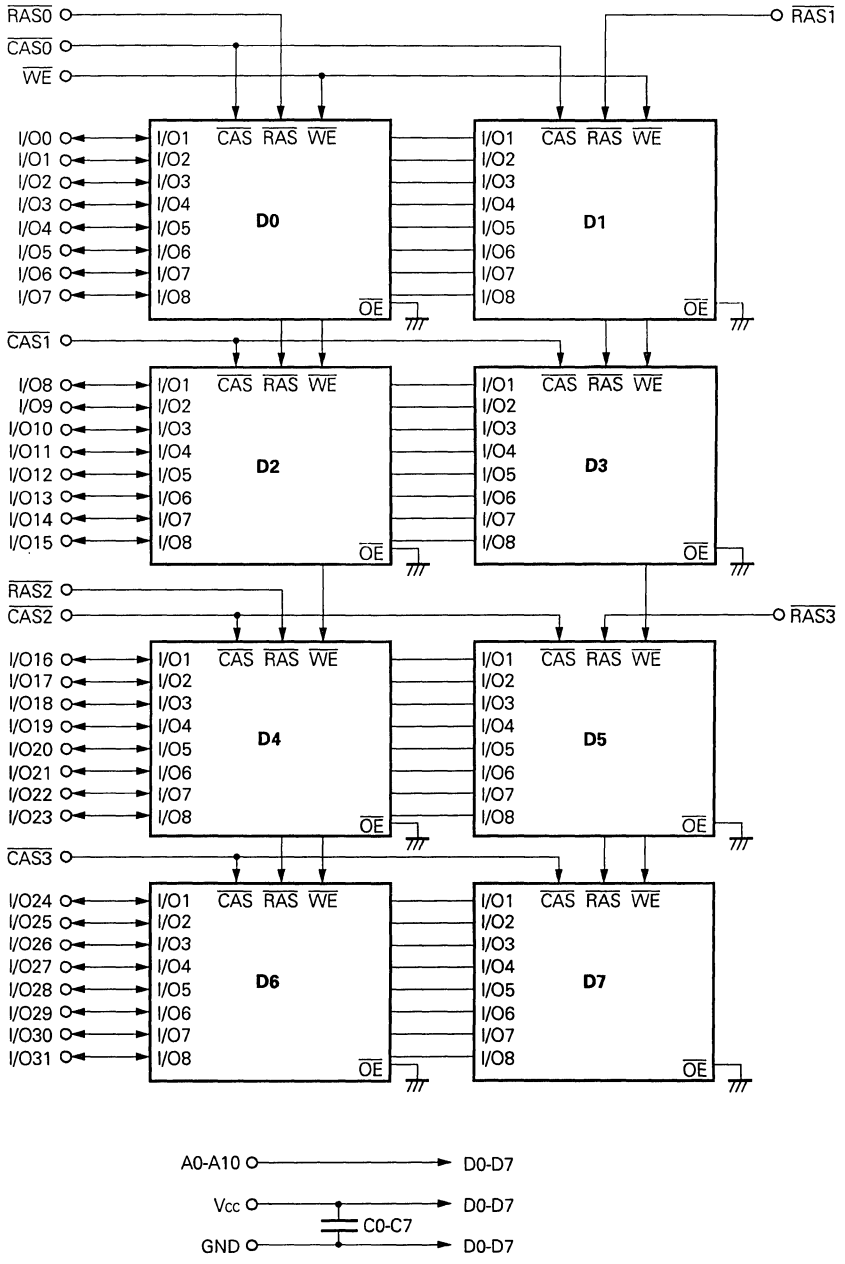


A0 - A10	:	Address Inputs
I/O0 - I/O31	:	Data Inputs/Outputs
$\overline{RAS0}$ - $\overline{RAS3}$	:	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
PD1 - PD7	:	Presence Detect Pins
Vcc	:	Power Supply
GND	:	Ground
NC	:	No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	GND	GND	GND
PD2	66	NC	NC	NC
PD3	67	GND	GND	GND
PD4	68	GND	GND	GND
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram



Remark D0-D7 : μPD42S17800LG5 (TSOP (II))

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			55	pF
	C_{I2}	$\overline{WE}$			71	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			30	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			24	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			19	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		405	mA	3, 4, 7
			t_{RAC} = 70 ns		365		
			t_{RAC} = 80 ns		325		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		4.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		1.2		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		405	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		365		
			t_{RAC} = 80 ns		325		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		285	mA	3, 4, 6
			t_{RAC} = 70 ns		245		
			t_{RAC} = 80 ns		205		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		405	mA	3, 4
			t_{RAC} = 70 ns		365		
			t_{RAC} = 80 ns		325		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} =62.5 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} –0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤0.2 V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ –0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$: V_{IH} I_O = 0 mA	t_{RAS} ≤ 1 μs		1.6	mA	3, 4
$\overline{CAS}$ before $\overline{RAS}$ self refresh current	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} –0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤0.2 V I_O = 0 mA			1.2	mA	4
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

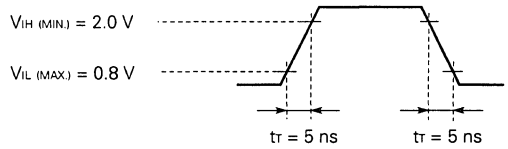
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RPS}	110		130		150		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{CHS}	–50		–50		–50		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		128		128		128	ms	

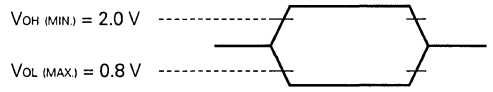
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

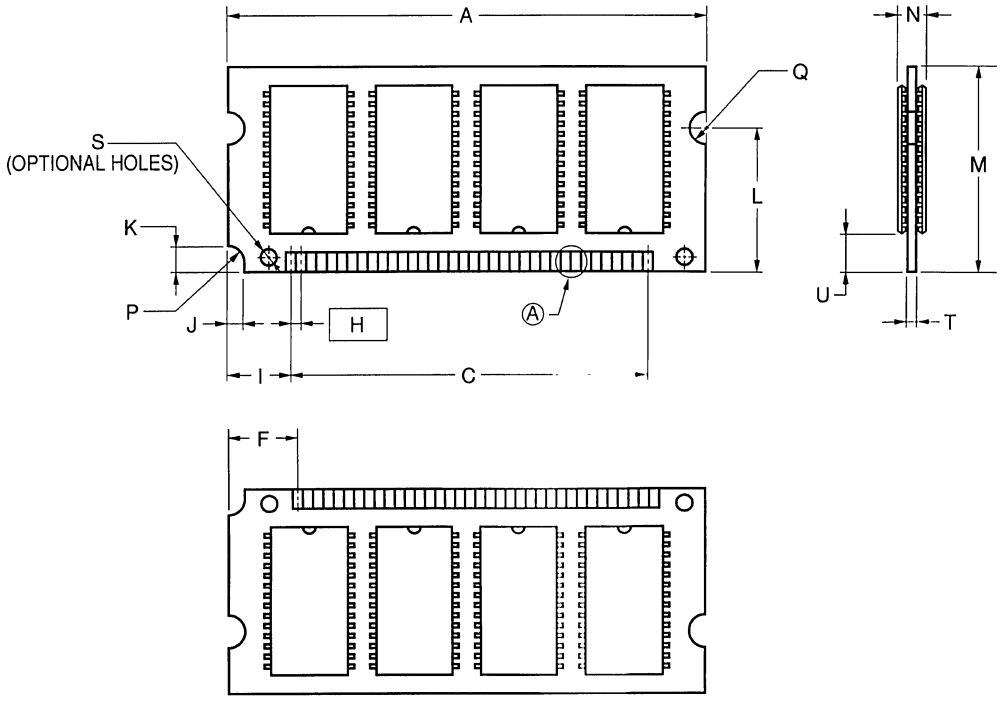
    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 1 TTL and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}$/$\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

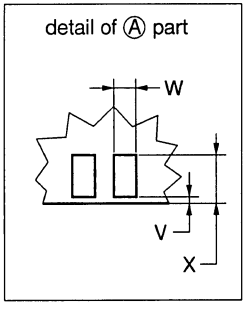
Timing Chart

Please refer to Timing Chart 6, page 419.

Package Drawing

72PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.03±0.13	$0.080^{+0.005}_{-0.006}$
K	3.175±0.13	0.125±0.006
L	17.78	0.700
M	25.4±0.13	1.000±0.006
N	3.81 MAX.	0.150 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
S	ϕ1.8	ϕ0.071
T	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U	3.175 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72S-50A2-2

NEC

MOS INTEGRATED CIRCUIT

MC-42S4000LAC32S SERIES

4 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S4000LAC32S series is a 4,194,304 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 8 pieces of 16 M DRAM: μPD42S17400LG3 (TSOP (II)) are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 4,194,304 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S4000LAC32S-A60	60 ns	110 ns	2,880 mW	4.32 mW (CMOS level input)
MC-42S4000LAC32S-A70	70 ns	130 ns	2,592 mW	
MC-42S4000LAC32S-A80	80 ns	150 ns	2,304 mW	

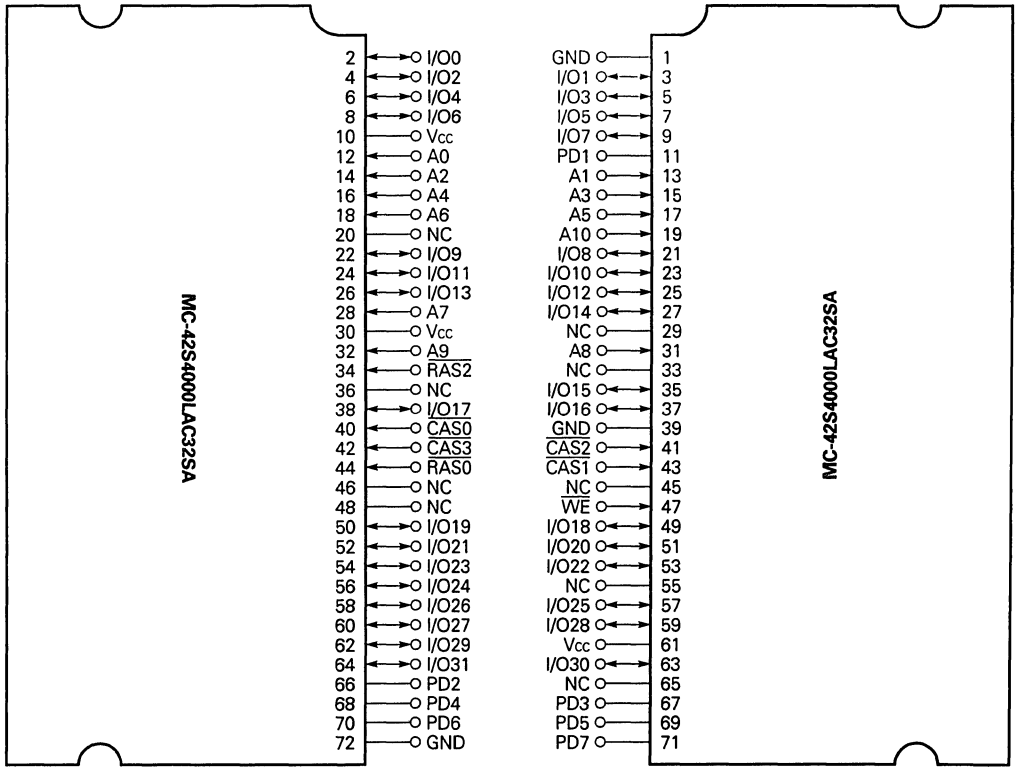
- 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S4000LAC32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	8 pieces of μPD42S17400LG3 (300 mil TSOP (II)) [Double side]
MC-42S4000LAC32SA-A70	70 ns		
MC-42S4000LAC32SA-A80	80 ns		

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



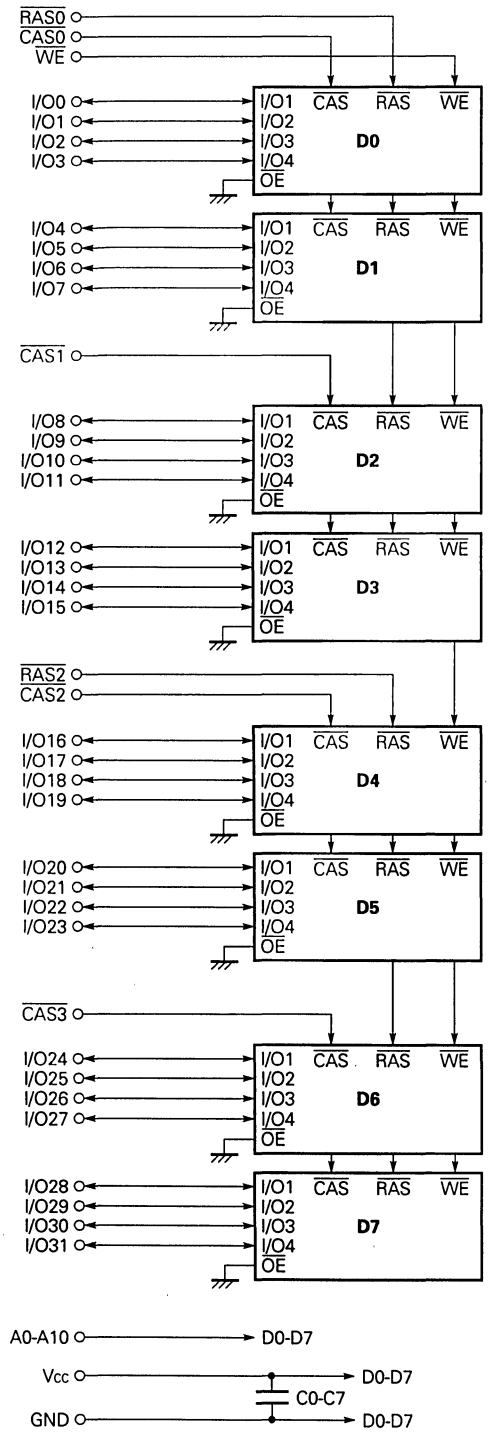
A0 - A10	: Address Inputs
I/O0 - I/O31	: Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$	: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{WE}$	: Write Enable
PD1 - PD7	: Presence Detect Pins
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	NC	NC	NC
PD2	66	NC	NC	NC
PD3	67	GND	GND	GND
PD4	68	NC	NC	NC
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram

Remark D0-07 : μPD42S17400LG3 (TSOP (II))



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			55	pF
	C_{I2}	$\overline{WE}$			71	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			36	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			19	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			10	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		800	mA	3, 4, 7
			t_{RAC} = 70 ns		720		
			t_{RAC} = 80 ns		640		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		4	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		1.2		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		800	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		720		
			t_{RAC} = 80 ns		640		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		560	mA	3, 4, 6
			t_{RAC} = 70 ns		480		
			t_{RAC} = 80 ns		400		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		800	mA	3, 4
			t_{RAC} = 70 ns		720		
			t_{RAC} = 80 ns		640		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} –0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V Standby: $\overline{RAS} \geq V_{CC}$ –0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		1.6	mA	3, 4
$\overline{CAS}$ before $\overline{RAS}$ self refresh current	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} –0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			1.2	mA	4
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

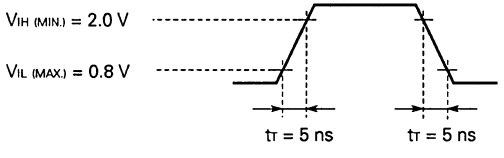
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{HPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{HRCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RPS}	110		130		150		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{CHS}	−50		−50		−50		ns	
Refresh Time	t_{REF}		128		128		128	ms	

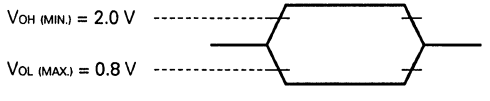
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.

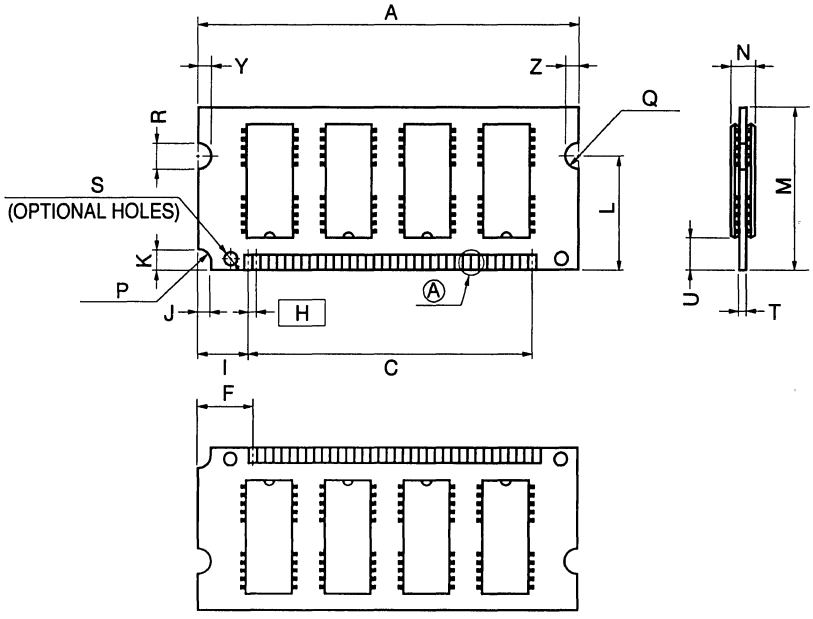
11. Loading conditions are 1 TTL and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

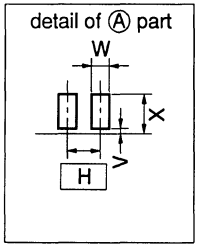
Timing Chart

Please refer to Timing Chart 6, page 419.

Package Drawing

72 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.0	0.079
K	3.18	0.125
L	17.78	0.700
M	25.4	1.000
N	3.8 MAX.	0.150 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ1.8	ϕ0.071
T	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U	3.18 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54 MIN.	0.100 MIN.
Y	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.

M72S-50A5

8 Byte DIMM
[Fast Page]

NEC

MOS INTEGRATED CIRCUIT

MC-421000AA64FA

1 M-WORD BY 64-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000AA64FA is a 1,048,576 words by 64 bits dynamic RAM module on which 16 pieces of 4 M DRAM: μPD424400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000AA64-60	60 ns	110 ns	10.42 W	420 mW (CMOS level input)
MC-421000AA64-70	70 ns	130 ns	8.74 W	
MC-421000AA64-80	80 ns	150 ns	7.90 W	

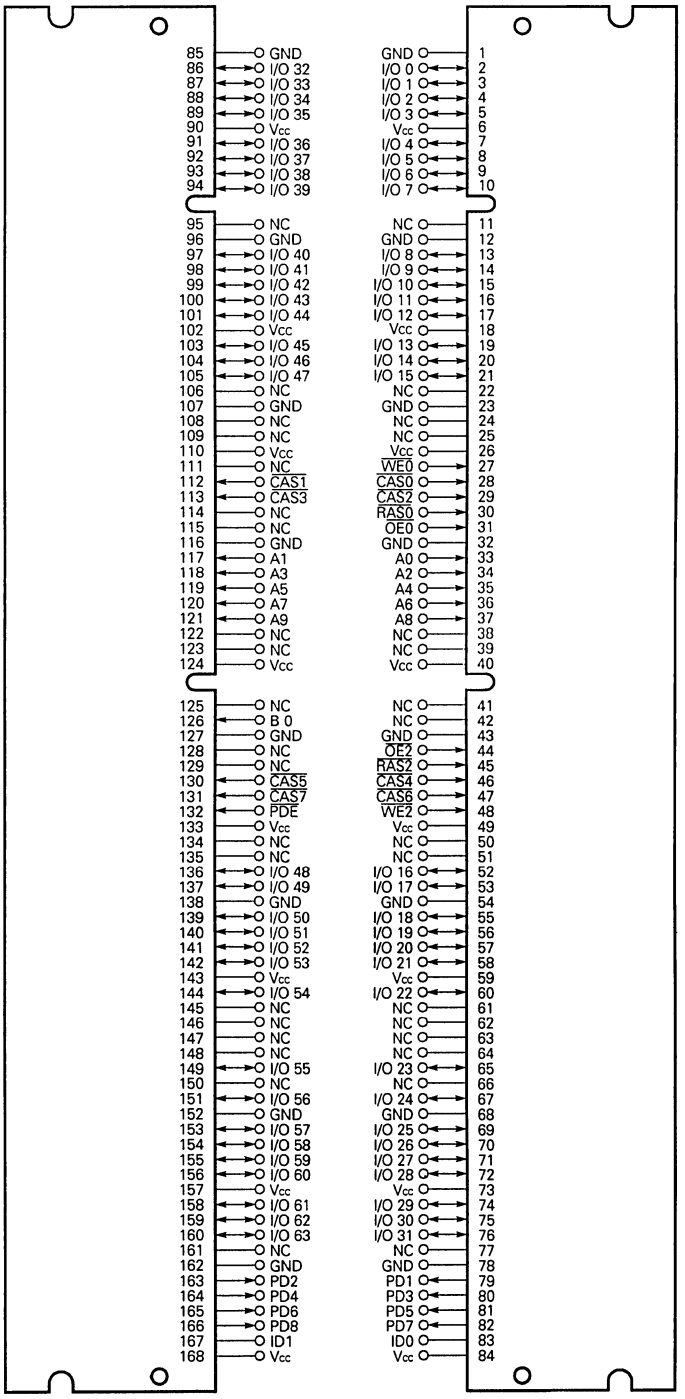
- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000AA64FA-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	16 pieces of μPD424400LA (300 mil SOJ) [Double side]
MC-421000AA64FA-70	70 ns		
MC-421000AA64FA-80	80 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



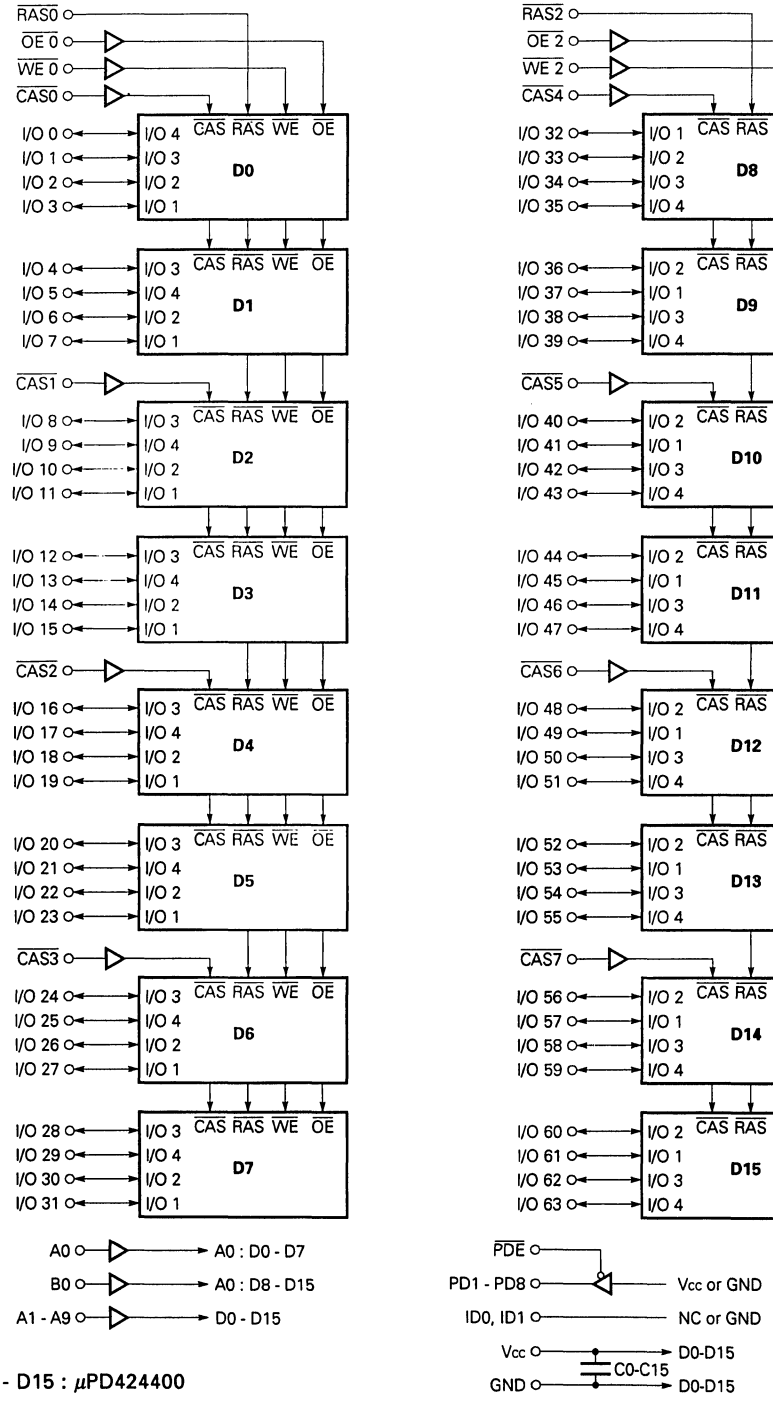
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	L	L	L
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	H	H	H
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 63 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D15 : μPD424400

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		18	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS7}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O63			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,984	mA	3, 4, 7
			t_{RAC} = 70 ns		1,664		
			t_{RAC} = 80 ns		1,504		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		96	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		80		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,984	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		1,664		
			t_{RAC} = 80 ns		1,504		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,504	mA	3, 4, 6
			t_{RAC} = 70 ns		1,344		
			t_{RAC} = 80 ns		1,184		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,984	mA	3, 4
			t_{RAC} = 70 ns		1,664		
			t_{RAC} = 80 ns		1,504		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V	$\overline{RAS}$	–10	+10	μA	
			Others	–5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

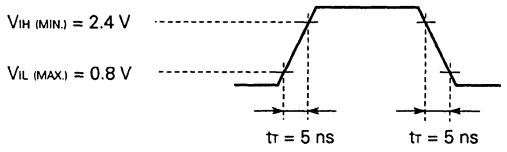
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		160		ns	
Read Modify Write Cycle Time	t_{RWC}	165		190		225		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	80		90		100		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		25		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		70		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		10		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	15		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35		40		45		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	90		100		115		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	55		60		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55		60		70		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	20		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		15		ns	
$\overline{WE}$ Setup Time	t_{WSR}	0		0		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	10		10		15		ns	
Refresh Time	t_{REF}		16		16		16	ms	

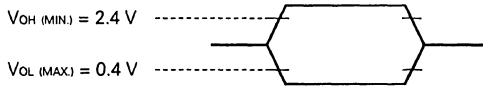
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. t_{OFF} (MAX.) and t_{OEZ} (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. t_{WP} (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH} (MIN.) should be met.

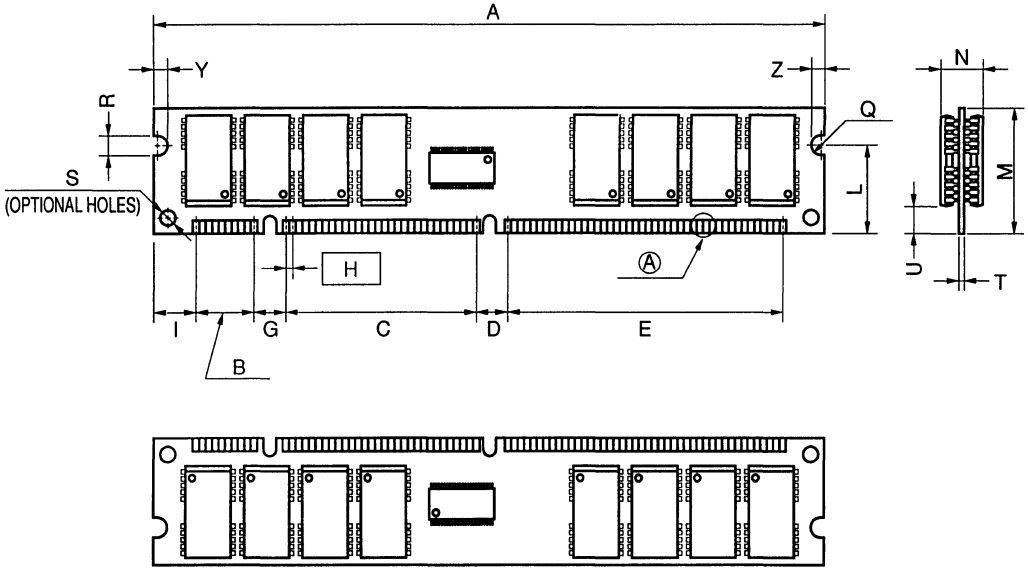
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

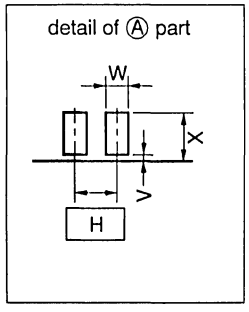
Timing Chart

Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
L	17.78	0.700
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A1

NEC

MOS INTEGRATED CIRCUIT
MC-421000AA64FB

1 M-WORD BY 64-BIT DYNAMIC RAM MODULE
FAST PAGE MODE

Description

The MC-421000AA64FB is a 1,048,576 words by 64 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μPD4218160 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000AA64-60	60 ns	110 ns	3.68 W	336 mW (CMOS level input)
MC-421000AA64-70	70 ns	130 ns	3.47 W	
MC-421000AA64-80	80 ns	150 ns	3.26 W	

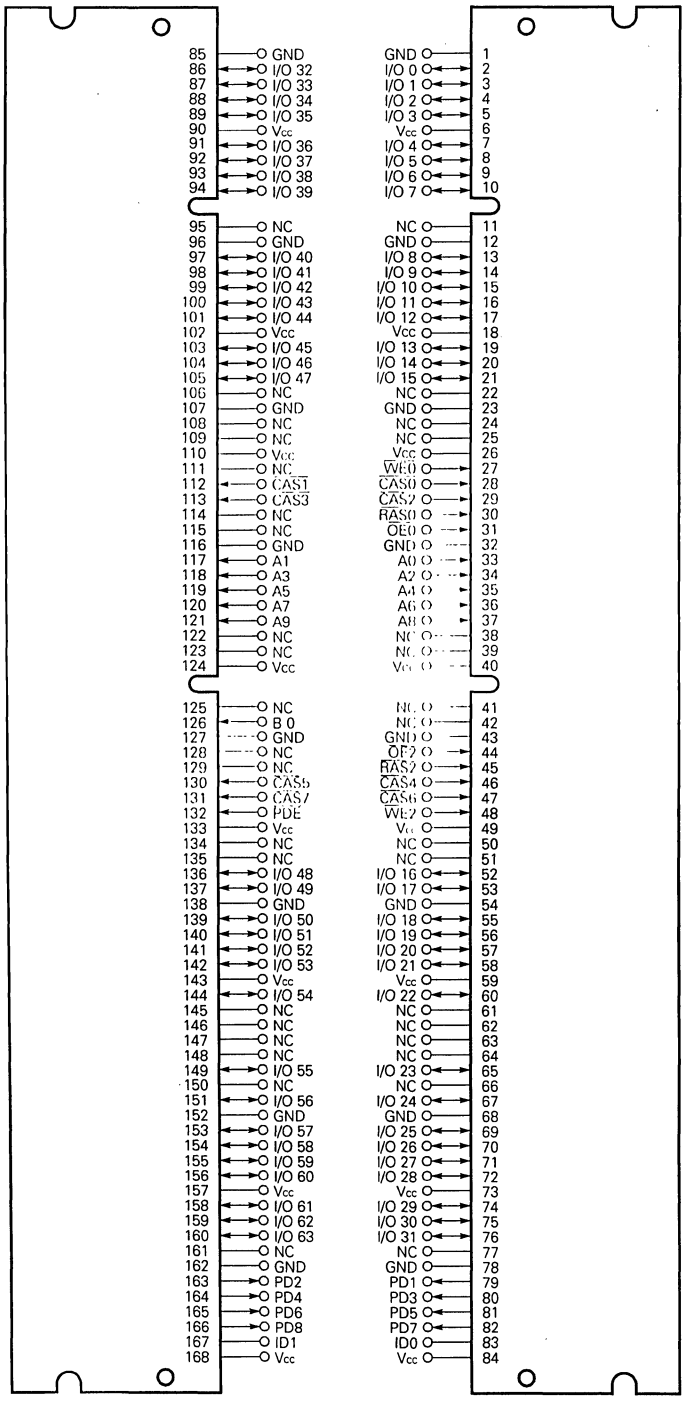
- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000AA64FB-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μPD4218160LE (400 mil SOJ) [Single side]
MC-421000AA64FB-70	70 ns		
MC-421000AA64FB-80	80 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



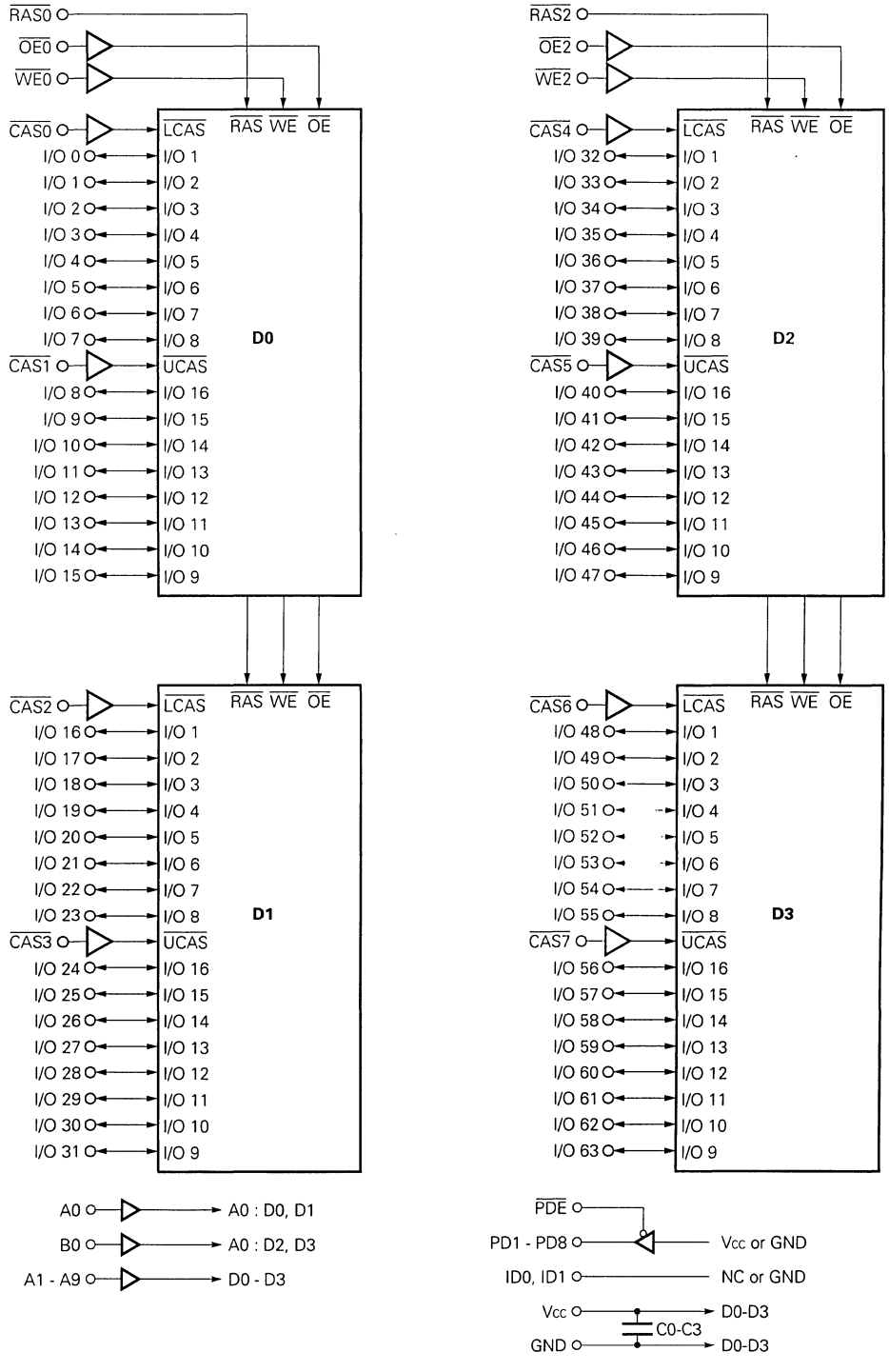
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	L	L	L
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	H	H	H
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 63 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D3 : μPD4218160

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		6	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			45	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS7}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O63			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		700	mA	3, 4, 7
			t_{RAC} = 70 ns		660		
			t_{RAC} = 80 ns		620		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		68	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		64		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		700	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		660		
			t_{RAC} = 80 ns		620		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		420	mA	3, 4, 6
			t_{RAC} = 70 ns		380		
			t_{RAC} = 80 ns		340		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		700	mA	3, 4
			t_{RAC} = 70 ns		660		
			t_{RAC} = 80 ns		620		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V	$\overline{RAS}$	−10	+10	μA	
			Others	−5	+1		
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

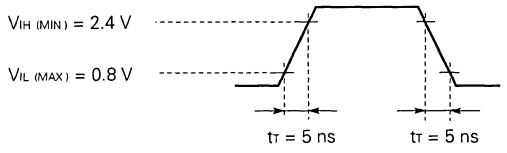
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	173		195		215		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		105		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		25		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	13		15		15		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	15	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	38		40		45		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	93		105		115		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	60		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	58		65		70		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		15		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		16		16		16	ms	

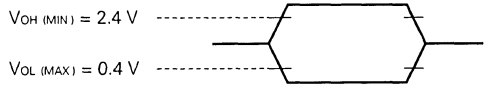
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

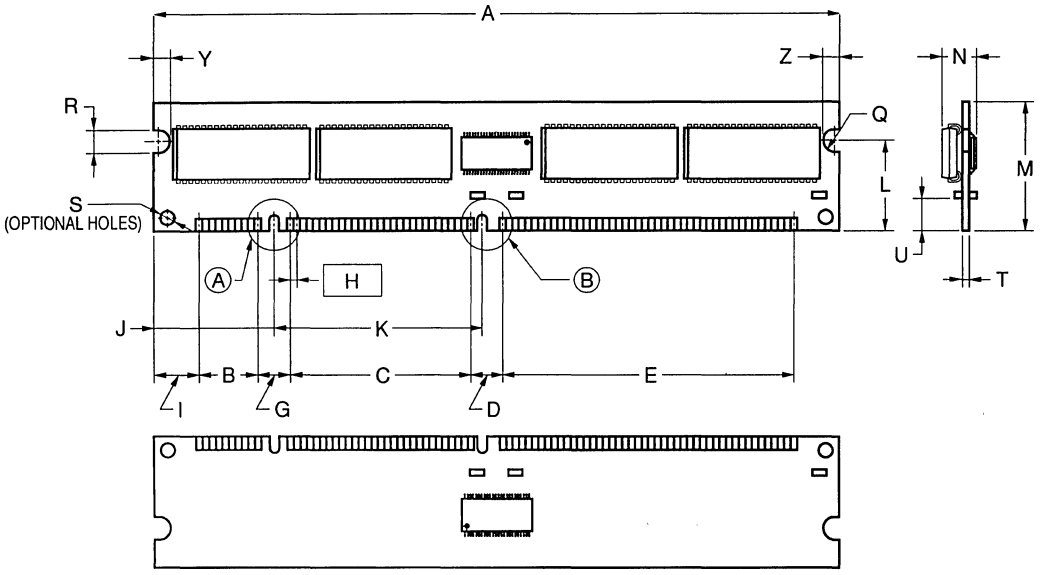
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

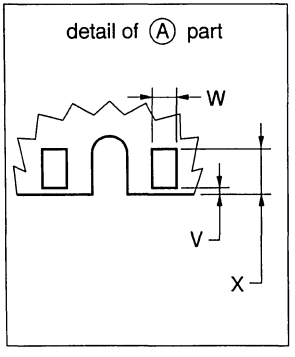
Timing Chart

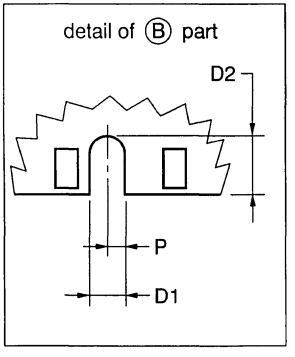
Please refer to Timing Chart 8, page 443.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.1230
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.05 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.7000
M	25.4±0.13	1.000±0.006
N	9.0 MAX.	0.355 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A5

NEC

MOS INTEGRATED CIRCUIT

MC-421000AD72F

1 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-421000AD72F is a 1,048,576 words by 72 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μPD4218160 and 2 pieces of 4 M DRAM: μPD424400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000AD72-60	60 ns	110 ns	4.94 W	347 mW (CMOS level input)
MC-421000AD72-70	70 ns	130 ns	4.52 W	
MC-421000AD72-80	80 ns	150 ns	4.20 W	

- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

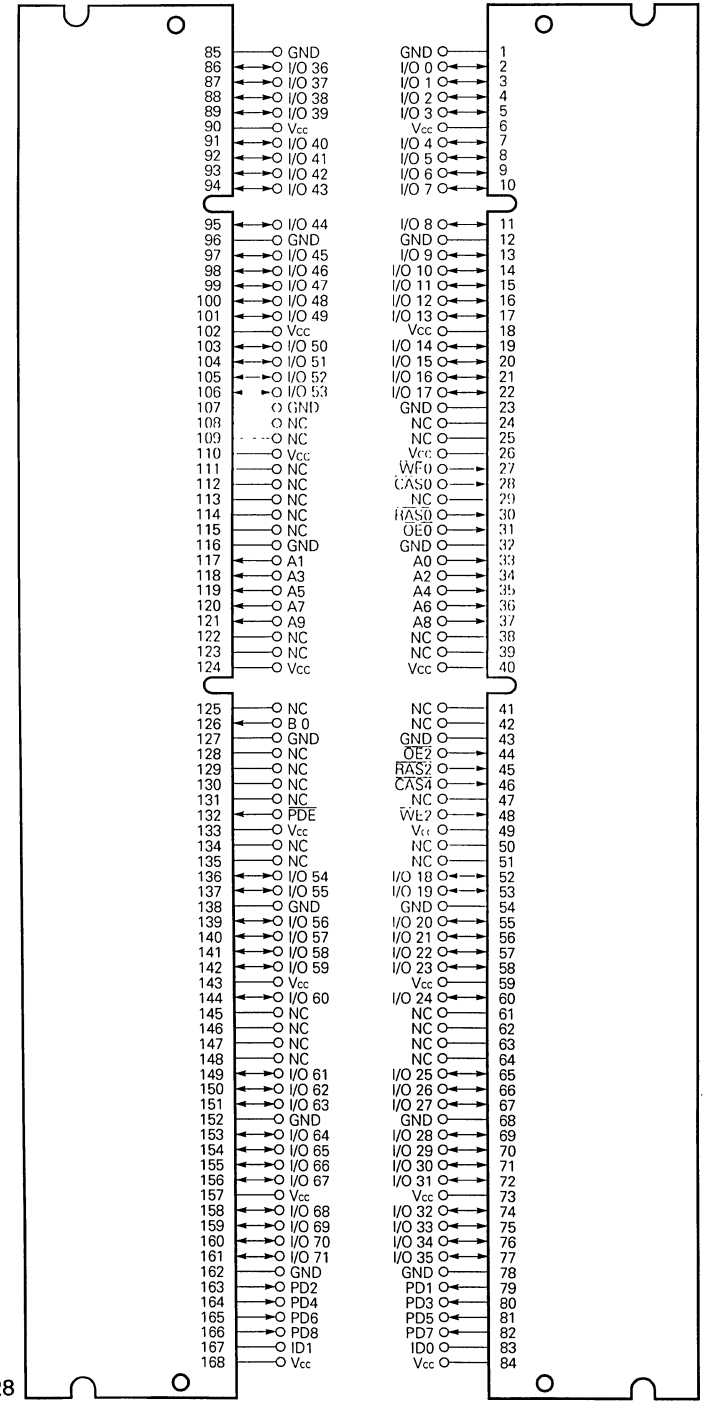
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000AD72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μPD4218160G5 (400 mil TSOP(II)) and 2 pieces of μPD424400G3 (300 mil TSOP(II)) [Double side]
MC-421000AD72F-70	70 ns		
MC-421000AD72F-80	80 ns		

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



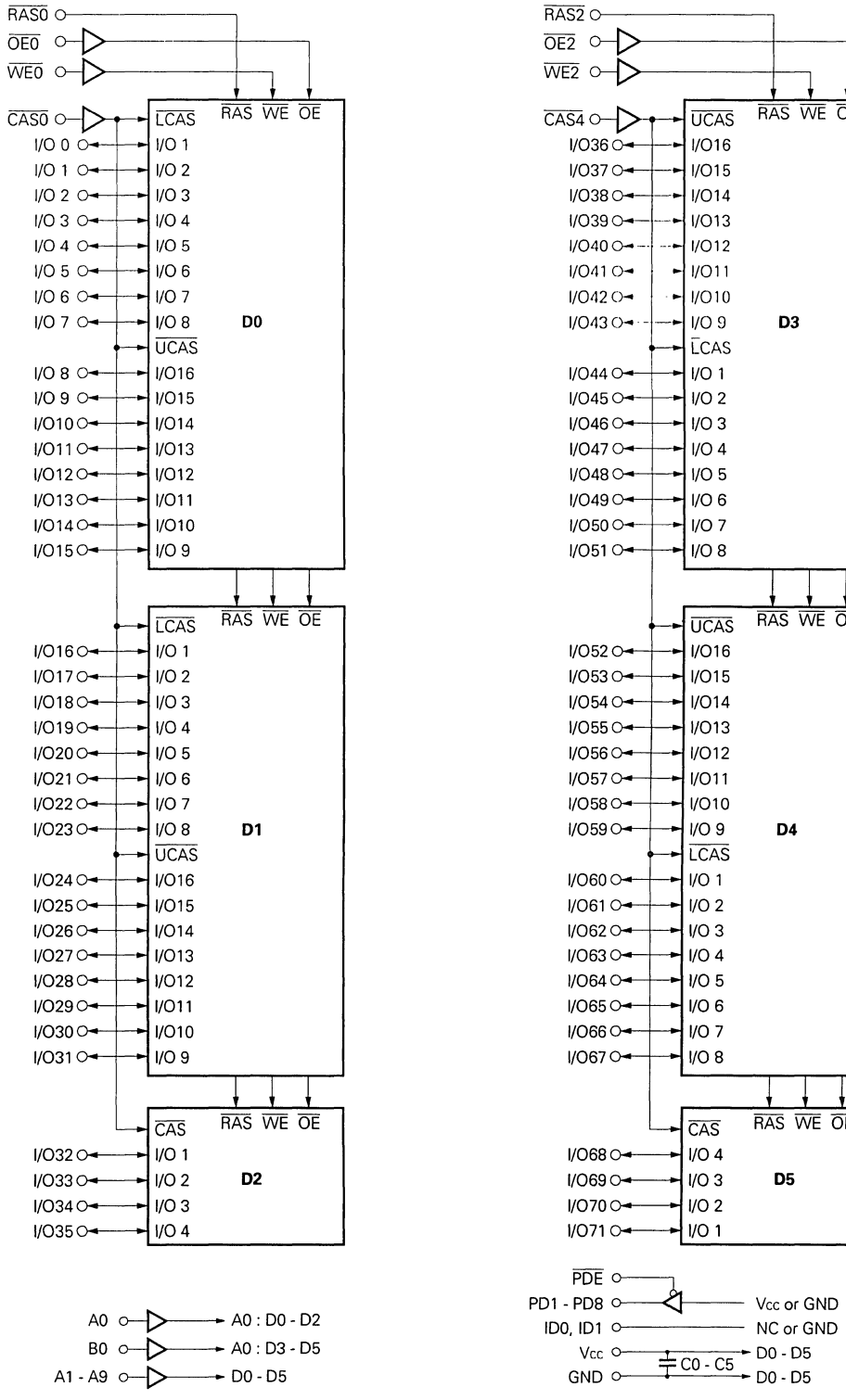
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	L	L	L
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0, D1, D3, D4: μPD4218160 D2, D5: μPD424400

Electrical Specifications [Notes 1, 2]

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		-1.0 to +7.0	V
Supply voltage	V_{CC}		-1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		-1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			36	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	3, 4, 7
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		800		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		72	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		66		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		800		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		600	mA	3, 4, 6
			t_{RAC} = 70 ns		540		
			t_{RAC} = 80 ns		480		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	3, 4
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		800		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V	RAS	10	+10	μA	
			Others	5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

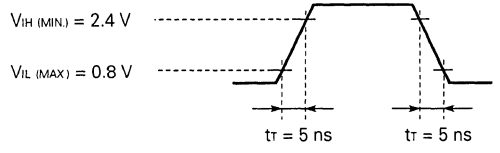
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		160		ns	
Read Modify Write Cycle Time	t_{RWC}	173		195		225		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		105		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		25		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		70		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		10		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	38		40		45		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	93		105		115		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	60		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	58		65		70		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		16		16		16	ms	

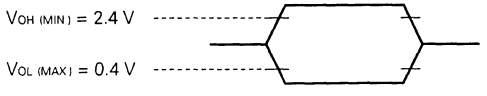
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

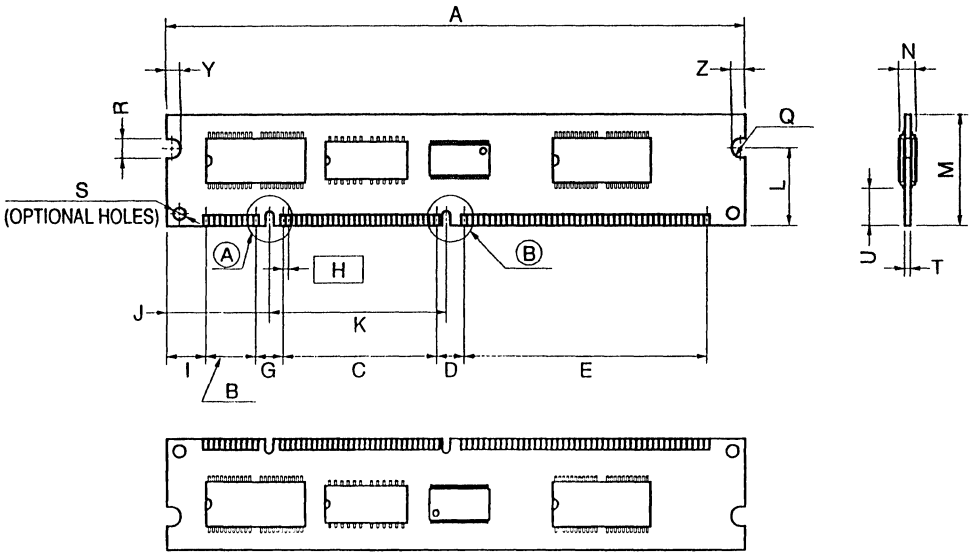
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

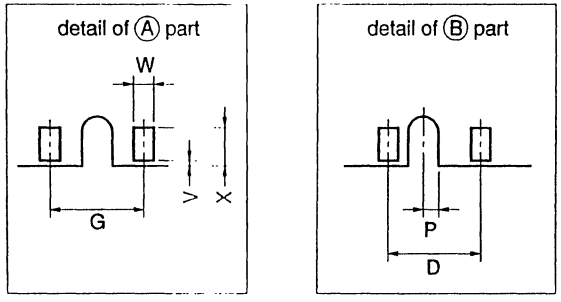
Timing Chart

Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R 2.0	R 0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54	0.100
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A4

MOS INTEGRATED CIRCUIT

MC-422000AA64FB

2M -WORD BY 64-BIT DYNAMIC RAM MODULE

FAST PAGE MODE

Description

The MC-422000AA64FB is a 2 097 152 words by 64 bits dynamic RAM module on which 8 pieces of 16M DRAM (μPD 4218160) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2 097 152 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC- 422000AA64-60	60ns	110ns	3.74 w	378 mW (CMOS level)
MC- 422000AA64-70	70ns	130ns	3.53 w	
MC- 422000AA64-80	80ns	150ns	3.32 w	

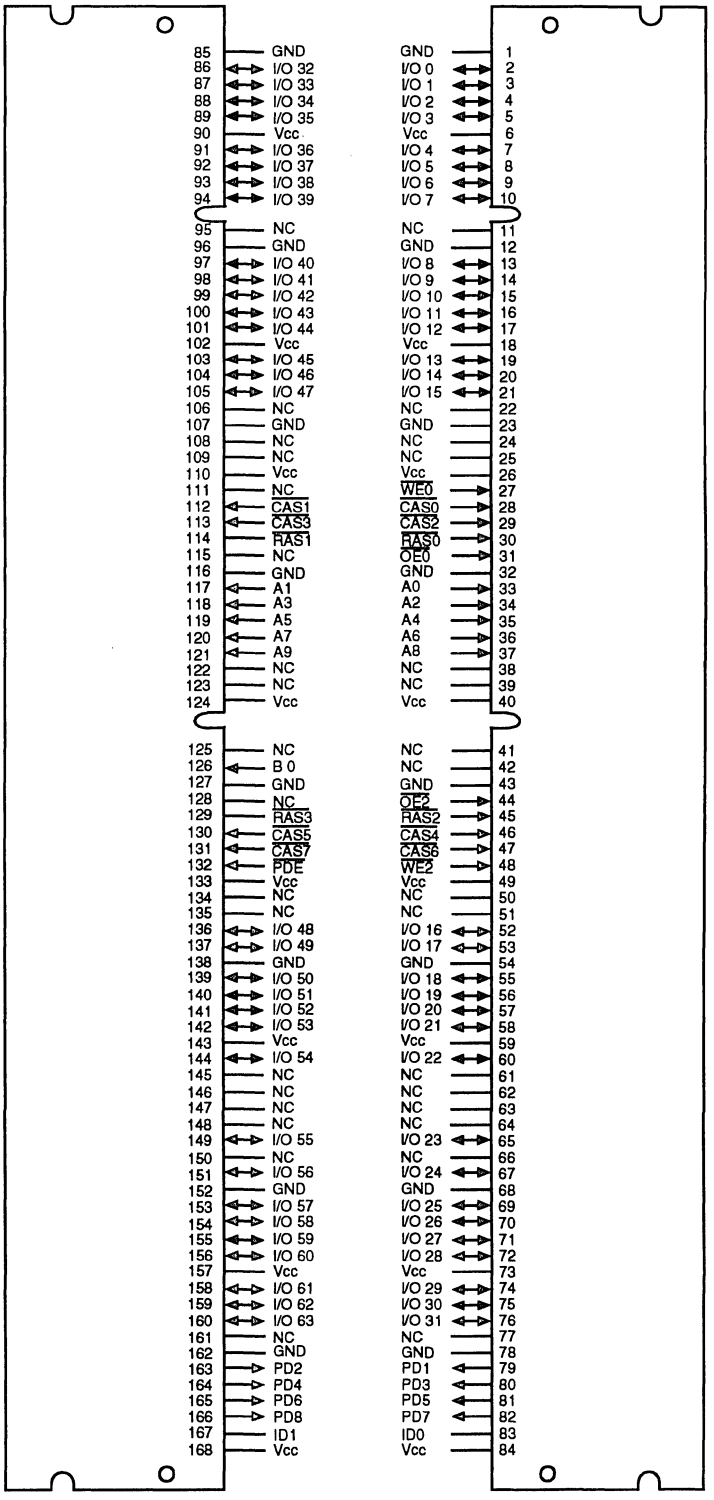
- 1 024 refresh cycles/16 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh , $\overline{\text{RAS}}$ only refresh , Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +5.0V±0.25V power supply

Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 422000AA64FB-60	60ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	8 pieces of uPD 4218160LE (400mil SOJ) [Single side]
MC- 422000AA64FB-70	70ns		
MC- 422000AA64FB-80	80ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



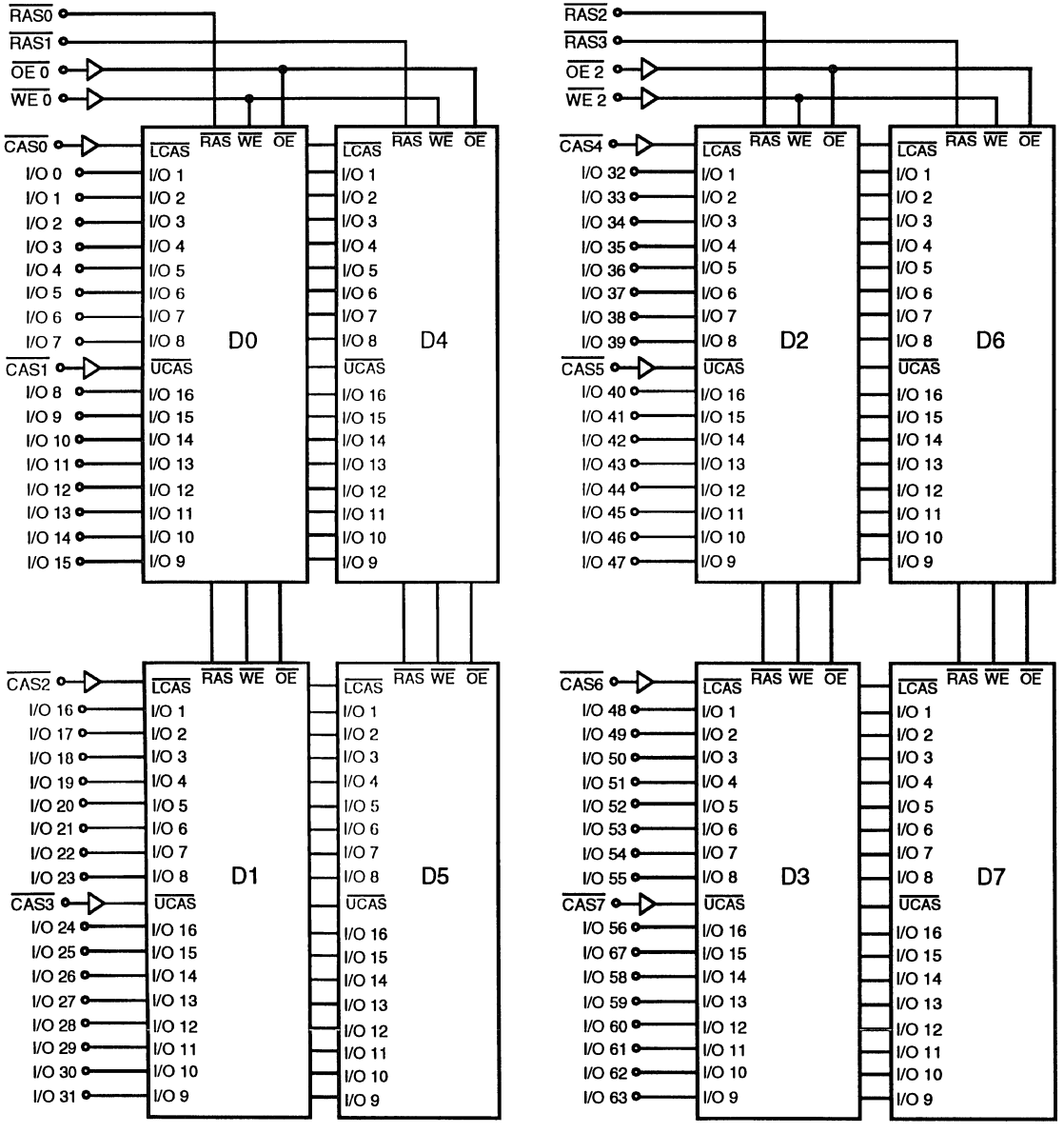
PD and ID Table

Pin Name	Pin No.	Accsess Time		
		60ns	70ns	80ns
PD1	79	H	H	H
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	H	H	H
I D0	83	GND	GND	GND
I D1	167	GND	GND	GND

Note) H : VOH, L : VOL

A0 - A9 , B0 : Address Inputs
I/O 0-I/O 63 : Data Inputs / Outputs
$\overline{RAS0}$-$\overline{RAS3}$: Row Address Strobe
$\overline{CAS0}$-$\overline{CAS7}$: Column Address Strobe
$\overline{WE0}$,$\overline{WE2}$: Write Enable
$\overline{OE0}$,$\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1- PD8 : Presence Detect Pins
ID0,ID1 : Identity pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-1.0 to +7.0	V
Supply voltage	VCC		-1.0 to +7.0	V
Output current	IO		50	mA
Power dissipation	PD		10	W
Operating temperature	Topt		0 to +70	℃
Storage temperature	Tstg		-55 to +125	℃

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device in not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES : 1, 2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		4.75	5.0	5.25	V
High level input voltage	VIH		2.4		Vcc + 1.0	V
Low level input voltage	VIL		-1.0		+0.8	V
Ambient temperature	Ta		0		70	℃

CAPACITANCE (Ta=25℃, f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C I 1	A0 - A9, B0			20	pF
	C I 2	$\overline{WE0}$, $\overline{WE2}$			20	pF
	C I 3	$\overline{RAS0}$ - $\overline{RAS3}$			45	pF
	C I 4	$\overline{CAS0}$ - $\overline{CAS7}$			20	pF
	C I 5	$\overline{OE0}$, $\overline{OE2}$			20	pF
Data Input/ Output capacitance	C I/O	I/O 0 - I/O 63			20	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
Operating Current	Icc1	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}=t_{RC\ (MIN.)}$, IO=0mA	t_{RAC}=60ns		712	mA	3, 4, 7
			t_{RAC}=70ns		672		
			t_{RAC}=80ns		632		
Standby Current	Icc2	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH\ (MIN.)}$			80	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ Vcc-0.2V			72		
$\overline{RAS}$ only refresh current	Icc3	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≧ V_{IH} $t_{RC}=t_{RC\ (MIN.)}$, IO=0mA	t_{RAC}=60ns		712	mA	3, 4, 7
			t_{RAC}=70ns		672		
			t_{RAC}=80ns		632		
Operating Current (Fast Page Mode)	Icc4	$\overline{RAS}$ ≦ VIL, $\overline{CAS}$ Cycling tPC=tPC MIN., IO=0mA	t_{RAC}=60ns		432	mA	3, 4, 6
			t_{RAC}=70ns		392		
			t_{RAC}=80ns		352		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	Icc5	$t_{RC}=t_{RC\ (MIN.)}$ IO=0mA	t_{RAC}=60ns		712	mA	3, 4
			t_{RAC}=70ns		672		
			t_{RAC}=80ns		632		
Input Leakage Current	$I_{I(L)}$	VI=0 to 5.5V all other pins not under test = 0V	$\overline{RAS}$	-10	+10	μA	
			others	-5	+1		
Output Leakage Current	$I_{O(L)}$	Outputs are disabled (Hi - Z) VO=0 to 5.5V		-10	+10	μA	
High level output voltage	V_{OH}	IO=-5mA		2.4		V	
Low level output voltage	V_{OL}	IO=+4.2mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Notes 8, 9

(1/2)

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		tRAC = 80ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	tRC	110	-	130	-	150	-	ns	
Read Modify Write Cycle Time	tRWC	173	-	195	-	215	-	ns	
Fast Page Mode Cycle Time (Read or Write)	tPC	40	-	45	-	50	-	ns	
Read Modify Write Cycle Time (Fast Page Mode)	tPRWC	85	-	90	-	105	-	ns	
Access Time from $\overline{RAS}$	tRAC	-	60	-	70	-	80	ns	10, 11
Access Time from $\overline{CAS}$	tCAC	-	20	-	25	-	25	ns	10, 11
Access Time from Column Address	tAA	-	35	-	40	-	45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	tACP	-	40	-	45	-	50	ns	11
Access Time from $\overline{OE}$	tOEA	-	20	-	25	-	25	ns	11
$\overline{RAS}$ to Column Address Delay Time	tRAD	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	tCLZ	0	-	0	-	0	-	ns	11
$\overline{OE}$ to Data Setup Time	tOLZ	0	-	0	-	0	-	ns	11
Output Buffer Turn-off Delay Time($\overline{CAS}$)	tOFF	0	13	0	15	0	15	ns	12
$\overline{OE}$ to Data Delay Time	tOED	13	-	15	-	15	-	ns	
Output Buffer Turn-off Delay Time($\overline{OE}$)	tOEZ	0	13	0	15	0	15	ns	12
$\overline{OE}$ Command Hold Time	tOEH	0	-	0	-	0	-	ns	
$\overline{OE}$ to $\overline{RAS}$ inactive Setup Time	tOES	0	-	0	-	0	-	ns	
Transition Time (Rise and Fall)	tT	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	tRP	40	-	50	-	60	-	ns	
$\overline{RAS}$ Pulse Width(Random Read, Write Cycle)	tRAS	60	10 000	70	10 000	80	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	tRASP	60	125 000	70	125 000	80	125 000	ns	
$\overline{RAS}$ Hold Time	tRSH	15	-	18	-	20	-	ns	
$\overline{CAS}$ Pulse Width	tCAS	15	10 000	20	10 000	20	10 000	ns	
$\overline{CAS}$ Hold Time	tCSH	60	-	70	-	80	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	-	5	-	5	-	ns	13
$\overline{CAS}$ Precharge Time	tCPN	10	-	10	-	10	-	ns	
$\overline{CAS}$ Precharge Time(Fast Page Mode)	tCP	10	-	10	-	10	-	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	tRPC	5	-	5	-	5	-	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	tRHCP	40	-	45	-	50	-	ns	
Row Address Set Up Time	tASR	5	-	5	-	5	-	ns	
Row Address Hold Time	tRAH	10	-	10	-	12	-	ns	
Column Address Set Up Time	tASC	0	-	0	-	0	-	ns	
Column Address Hold Time	tCAH	15	-	15	-	15	-	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	tRAL	30	-	35	-	40	-	ns	
Lead Command Setup Time	tRCS	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0	-	0	-	0	-	ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0	-	0	-	0	-	ns	14
Write Command Hold Time Referenced to $\overline{CAS}$	tWCH	10	-	10	-	15	-	ns	15

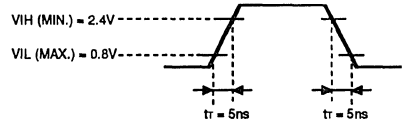
(2/2

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		tRAC = 80ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Comand Set-Up Time	tWP	10	-	10	-	15	-	ms	15
Data-in Seup Time	tDS	0	-	0	-	0	-	ns	16
Data-in Hold Time	tDH	10	-	15	-	15	-	ns	16
Write Comand Setup Time	tWCS	0	-	0	-	0	-	ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	tCWD	38	-	40	-	45	-	ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	tRWD	93	-	105	-	115	-	ns	17
$\overline{CAS}$ Precharge Delay Time Referenced to $\overline{WE}$ (Fast Page Mode)	tCPWD	60	-	65	-	70	-	ns	17
Column Address Delay Time Referenced to $\overline{WE}$	tAWD	58	-	65	-	70	-	ns	17
Write Command Lead Time Referenced to $\overline{RAS}$	tRWL	25	-	25	-	25	-	ns	
Write Command Lead Time Referenced to $\overline{CAS}$	tCWL	15	-	15	-	15	-	ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCSR	5	-	5	-	5	-	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCHR	10	-	10	-	10	-	ns	
$\overline{WE}$ Hold Time	tWHR	15	-	15	-	15	-	ns	
Refresh Time	tREF	-	16	-	16	-	16	ms	

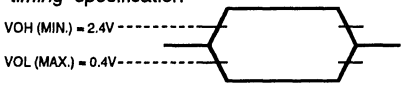
Notes:

1. All voltages are referenced to GND .
2. After power up, wait more than 100 µs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}) .
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.
8. AC measurements assume t_T =5ns .
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

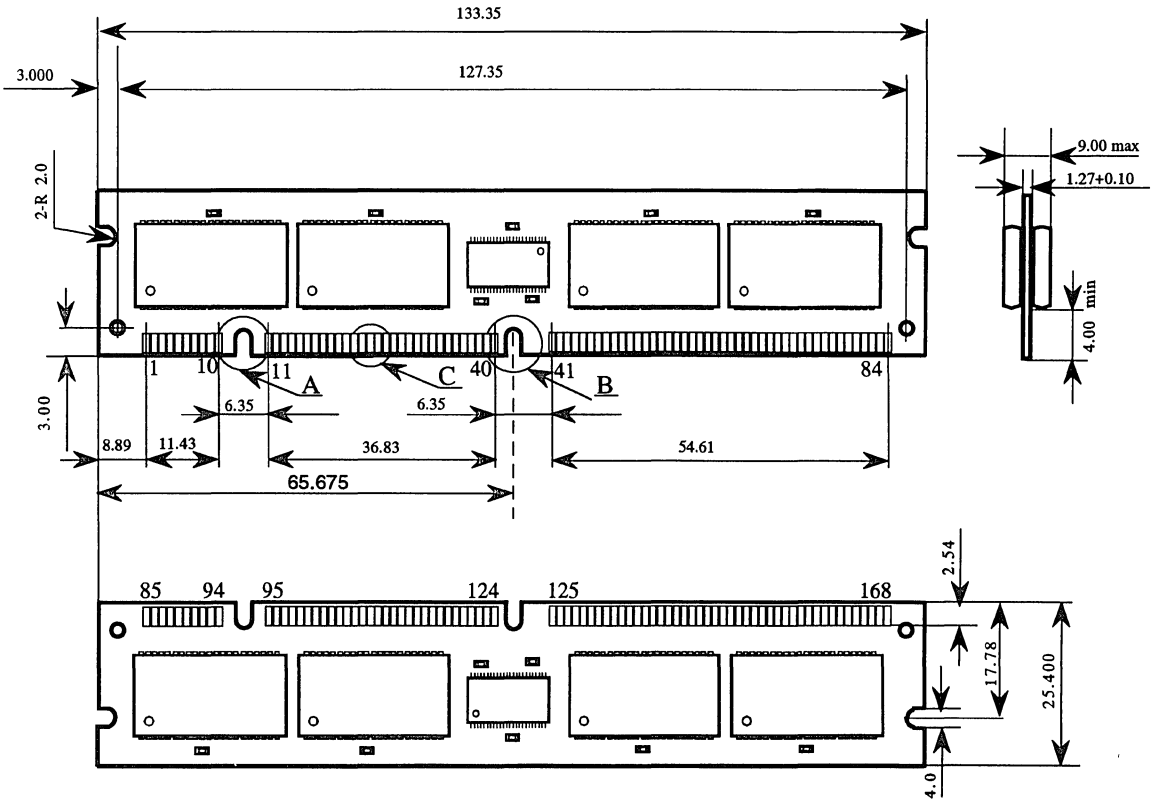
    $t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.
11. Loading conditions are 1 TTLs and 100 pF.
12. $t_{OFF(MAX.)}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP(MIN.)}$ requirement should be applied to $\overline{RAS}$ / $\overline{CAS}$ cycles.
14. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
15. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.
16. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle . If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$ and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

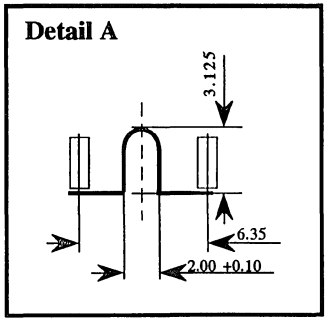
Timing Chart

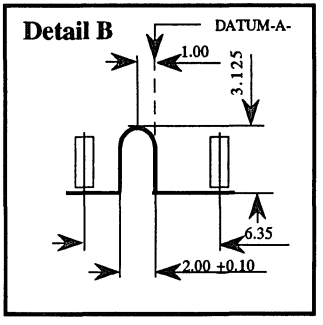
Please refer to Timing Chart 8, page 443.

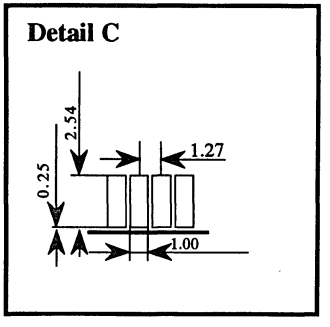
Package Drawing

UNIT: mm









NEC

MOS INTEGRATED CIRCUIT

MC-422000AB72F

2 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-422000AB72F is a 2,097,152 words by 72 bits dynamic RAM module on which 9 pieces of 16 M DRAM: μPD4217800 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2,097,152 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000AB72-60	60 ns	110 ns	5.53 W	383 mW (CMOS level input)
MC-422000AB72-70	70 ns	130 ns	5.06 W	
MC-422000AB72-80	80 ns	150 ns	4.59 W	

- 2,048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

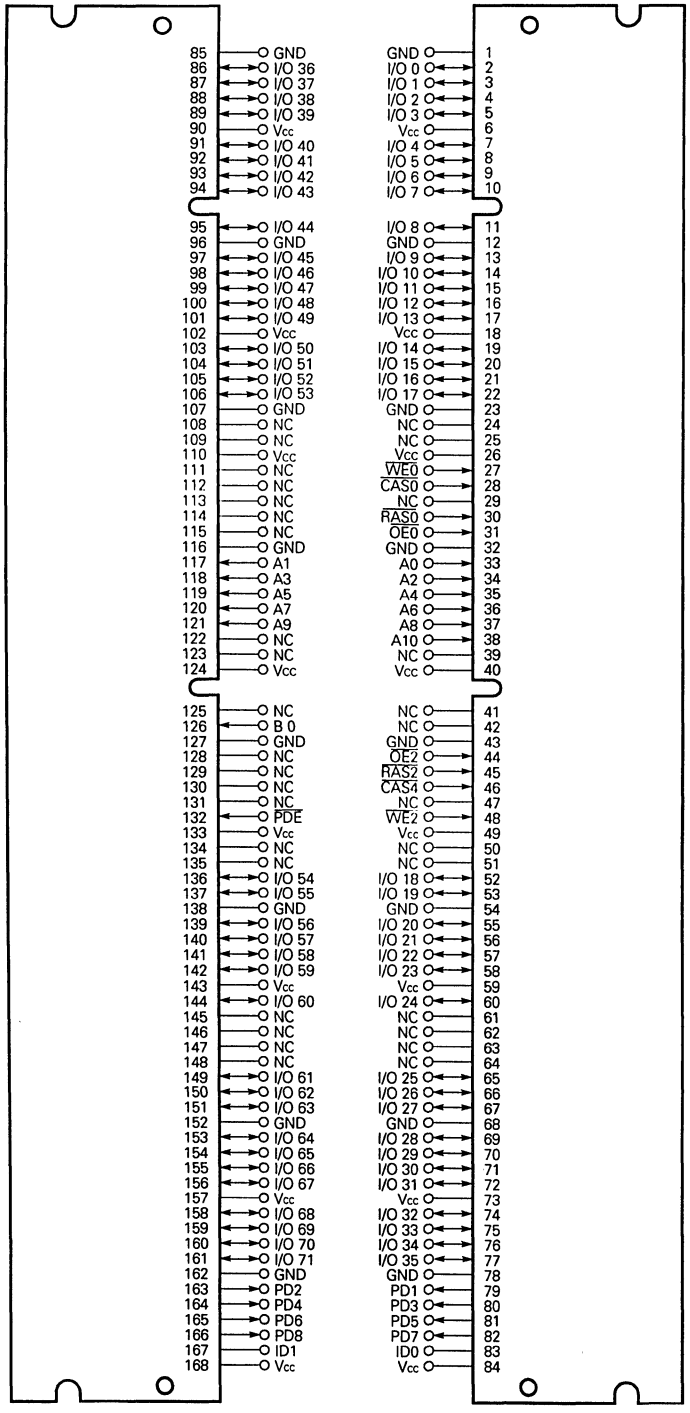
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000AB72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	9 pieces of μPD4217800G5 (400 mil TSOP(II)) [Double side]
MC-422000AB72F-70	70 ns		
MC-422000AB72F-80	80 ns		

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



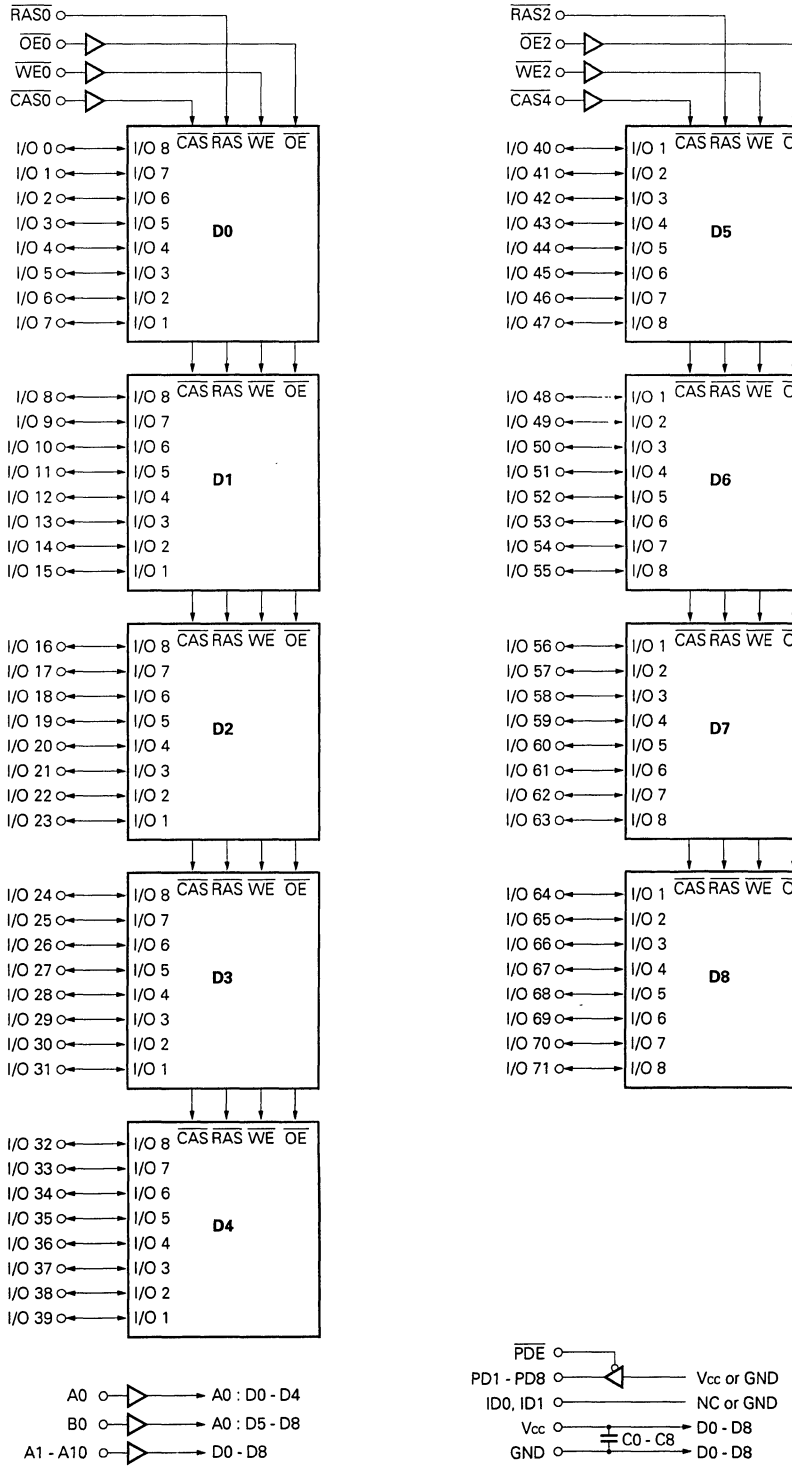
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	L	L	L
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A10, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D8 : μPD4217800

Electrical Specifications [Notes 1, 2]

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		11	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			50	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,054	mA	3, 4, 7
			t_{RAC} = 70 ns		964		
			t_{RAC} = 80 ns		874		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		82	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		73		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,054	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		964		
			t_{RAC} = 80 ns		874		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		694	mA	3, 4, 6
			t_{RAC} = 70 ns		604		
			t_{RAC} = 80 ns		514		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,054	mA	3, 4
			t_{RAC} = 70 ns		964		
			t_{RAC} = 80 ns		874		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V	$\overline{RAS}$	−10	+10	μA	
			Others	−5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

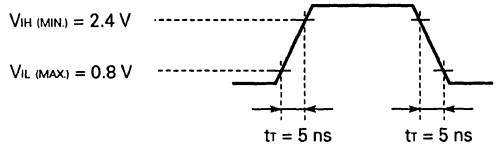
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	173		195		215		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		100		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		23		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	13		15		15		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	15	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	38		43		45		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	93		105		115		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	58		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	58		65		70		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		32		32		32	ms	

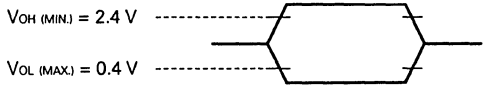
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

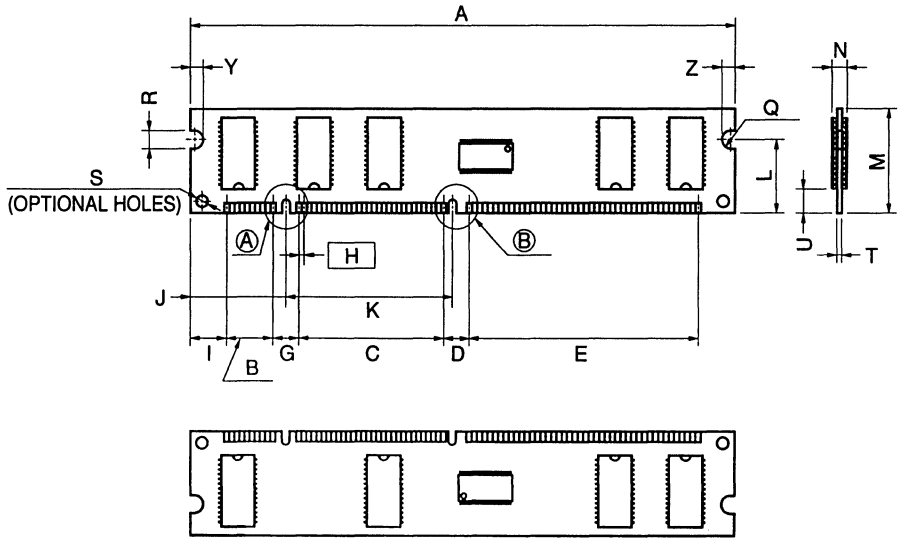
11. Loading conditions are 2 TTLs and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

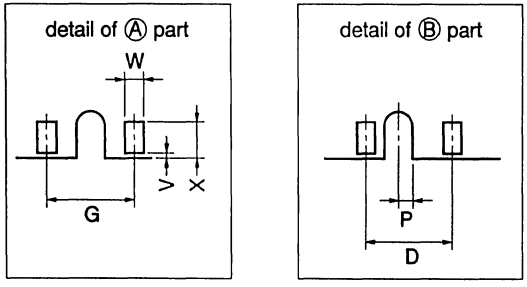
Timing Chart

Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54	0.100
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A6

NEC

MOS INTEGRATED CIRCUIT

MC-422000LAB72F

3.3 V OPERATION 2 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-422000LAB72F is a 2,097,152 words by 72 bits dynamic RAM module on which 9 pieces of 16 M DRAM: μPD4217800L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2,097,152 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000LAB72-A60	60 ns	110 ns	3.28 W	147.6 mW (CMOS level input)
MC-422000LAB72-A70	70 ns	130 ns	2.95 W	
MC-422000LAB72-A80	80 ns	150 ns	2.63 W	

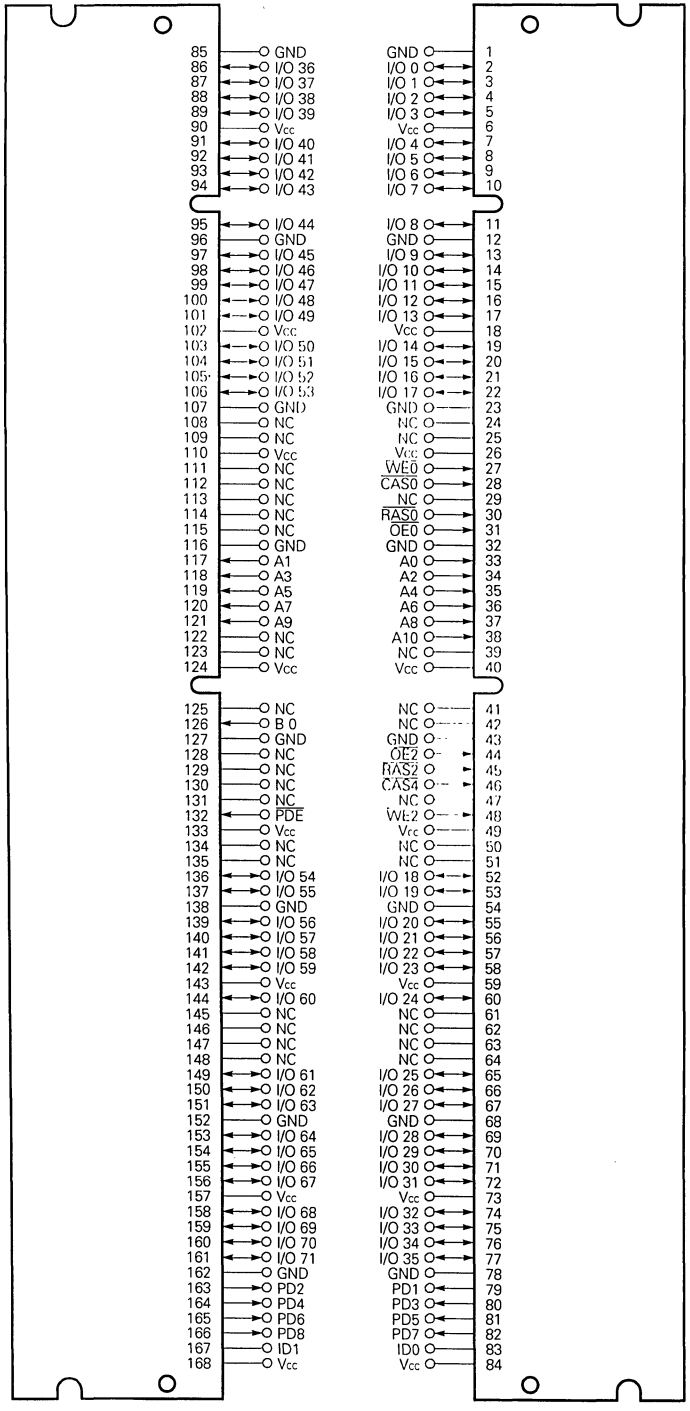
- 2,048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000LAB72F-A60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	9 pieces of μPD4217800LG5 (400 mil TSOP(II)) [Double side]
MC-422000LAB72F-A70	70 ns		
MC-422000LAB72F-A80	80 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



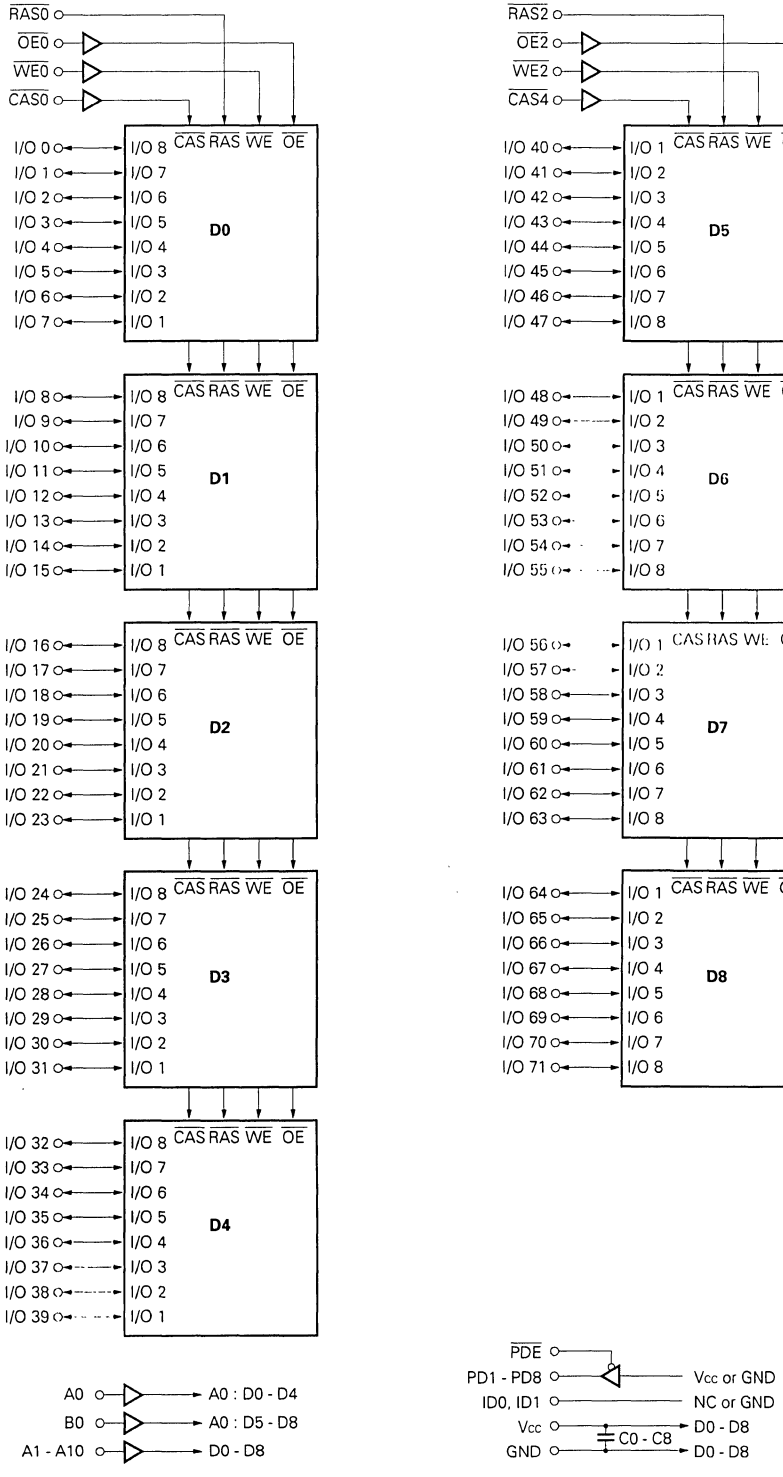
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	L	L	L
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A10, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D8 : μPD4217800L

Electrical Specifications [Notes 1, 2]

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		11	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			50	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		910	mA	3, 4, 7
			t_{RAC} = 70 ns		820		
			t_{RAC} = 80 ns		730		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		82	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		41		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		910	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		820		
			t_{RAC} = 80 ns		730		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		640	mA	3, 4, 6
			t_{RAC} = 70 ns		550		
			t_{RAC} = 80 ns		460		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		910	mA	3, 4
			t_{RAC} = 70 ns		820		
			t_{RAC} = 80 ns		730		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V	$\overline{RAS}$	−5	+5	μA	
			Others	−5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		−5	+5	μA	
High level output voltage	V_{OH}	I_O = −2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

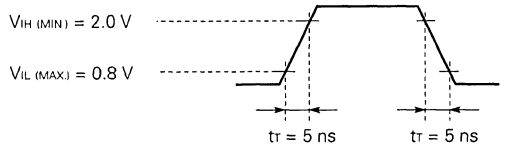
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	173		195		215		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		100		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		23		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	13		15		15		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	15	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	38		43		45		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	93		105		115		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	58		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	58		65		70		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		32		32		32	ms	

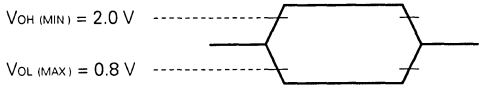
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

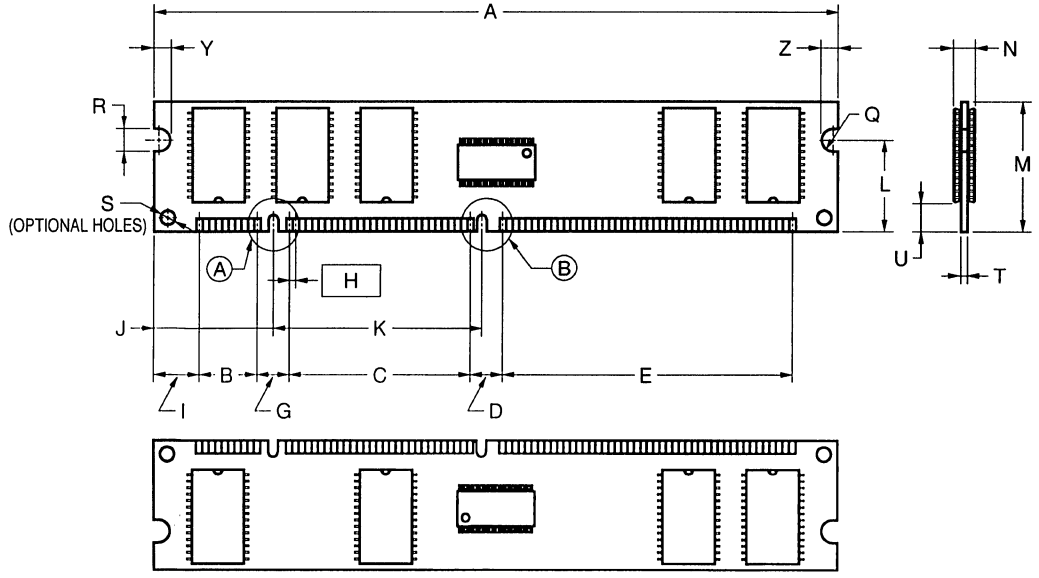
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

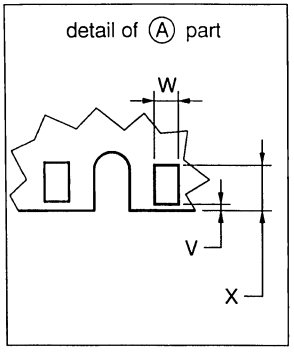
Timing Chart

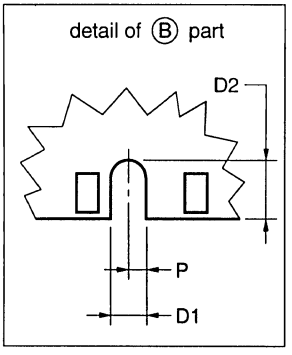
Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.123
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.50	0.925
K	43.18	1.70
L	17.78	0.700
M	25.4±0.13	1.000±0.006
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A8

NEC

MOS INTEGRATED CIRCUIT

MC-424000AB72F

4 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-424000AB72F is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μPD4217400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000AB72-60	60 ns	110 ns	10.73 W	430 mW (CMOS level input)
MC-424000AB72-70	70 ns	130 ns	9.79 W	
MC-424000AB72-80	80 ns	150 ns	8.84 W	

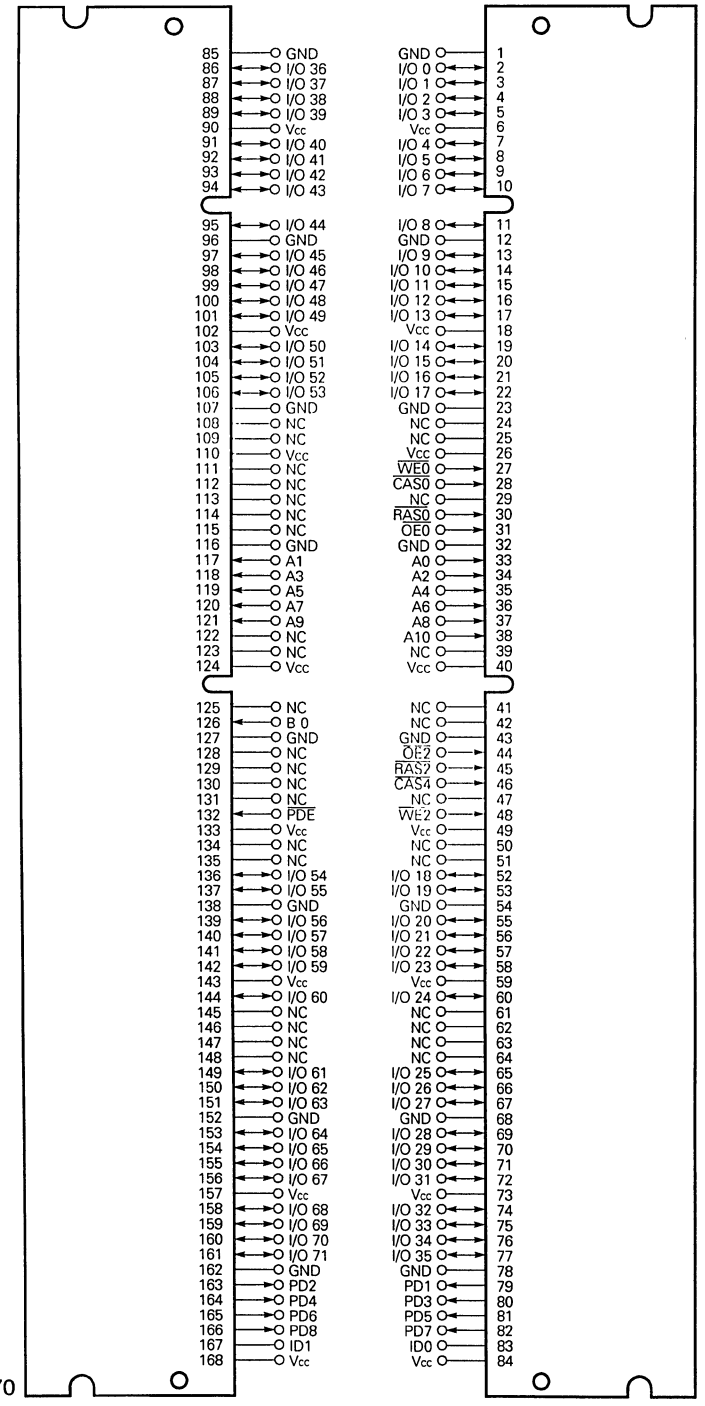
- 2,048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000AB72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of μPD4217400G3 (300 mil TSOP(II)) [Double side]
MC-424000AB72F-70	70 ns		
MC-424000AB72F-80	80 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



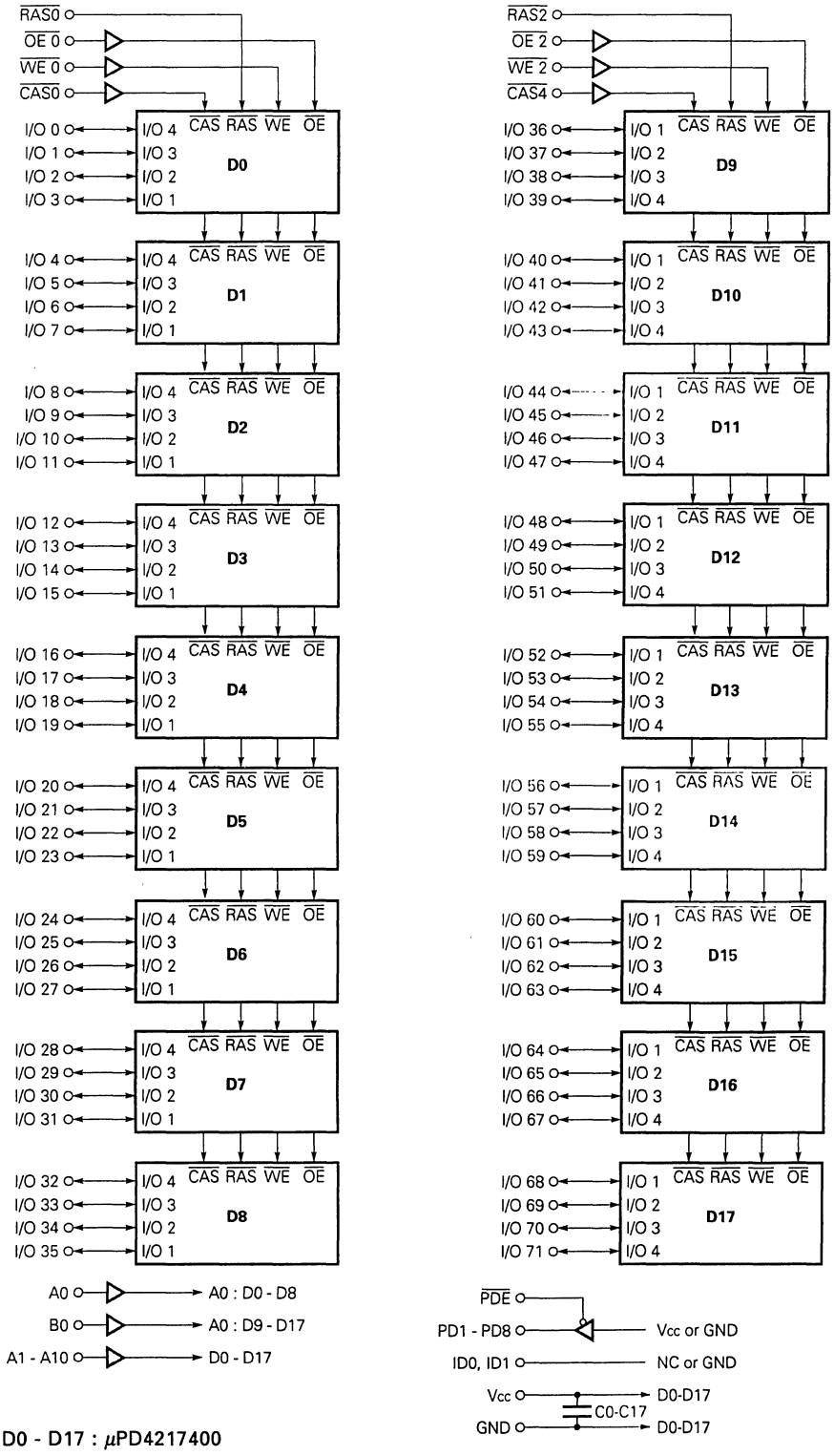
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	H	H	H
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A10, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D17 : μPD4217400

Electrical Specifications [Notes 1, 2]

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		20	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		2,044	mA	3, 4, 7
			t_{RAC} = 70 ns		1,864		
			t_{RAC} = 80 ns		1,684		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		100	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		82		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		2,044	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		1,864		
			t_{RAC} = 80 ns		1,684		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,324	mA	3, 4, 6
			t_{RAC} = 70 ns		1,144		
			t_{RAC} = 80 ns		964		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		2,044	mA	3, 4
			t_{RAC} = 70 ns		1,864		
			t_{RAC} = 80 ns		1,684		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V	$\overline{RAS}$	–10	+10	μA	
			Others	–5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

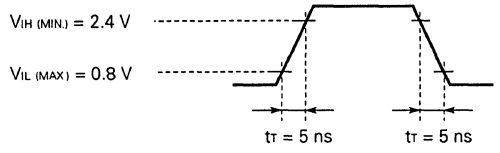
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	175		195		220		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		105		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		23		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40		43		50		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95		105		120		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	58		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60		65		75		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		32		32		32	ms	

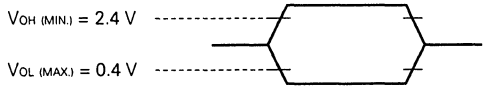
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

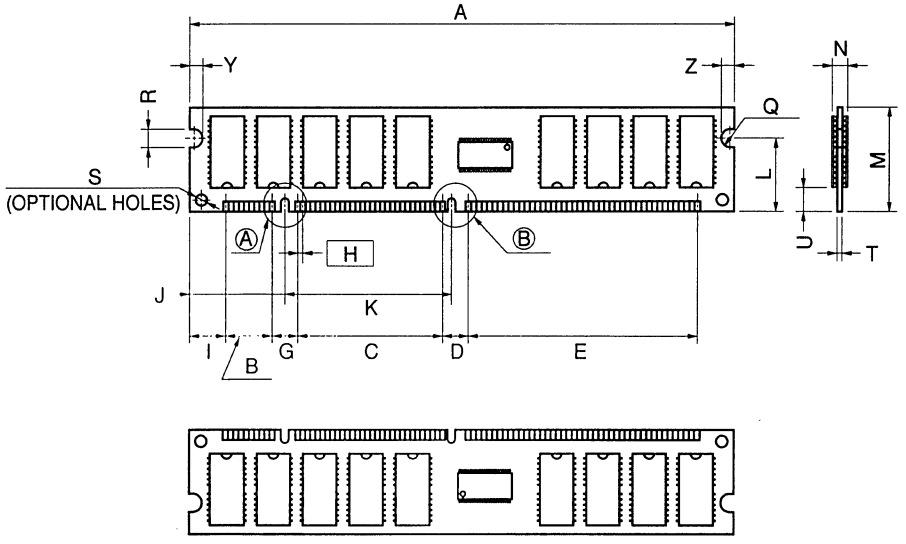
11. Loading conditions are 2 TTLs and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

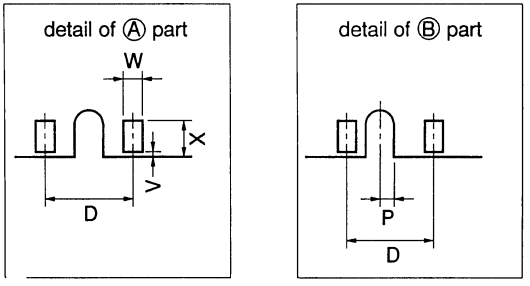
Timing Chart

Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A2

NEC

MOS INTEGRATED CIRCUIT

MC-424000AC72F

4 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-424000AC72F is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μPD4216400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000AC72-60	60 ns	110 ns	8.84 W	430 mW (CMOS level input)
MC-424000AC72-70	70 ns	130 ns	7.90 W	
MC-424000AC72-80	80 ns	150 ns	6.95 W	

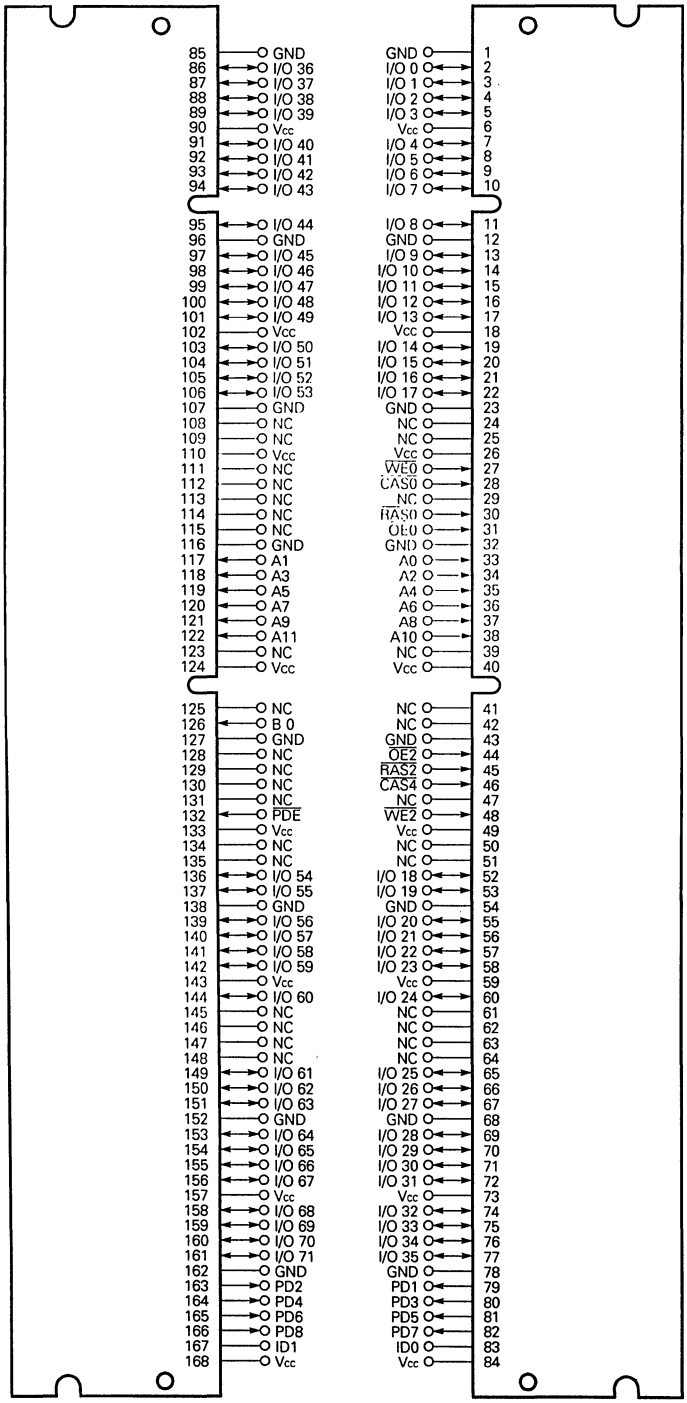
- 4,096 refresh cycles/64 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000AC72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of μPD4216400G3 (300 mil TSOP(II)) [Double side]
MC-424000AC72F-70	70 ns		
MC-424000AC72F-80	80 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



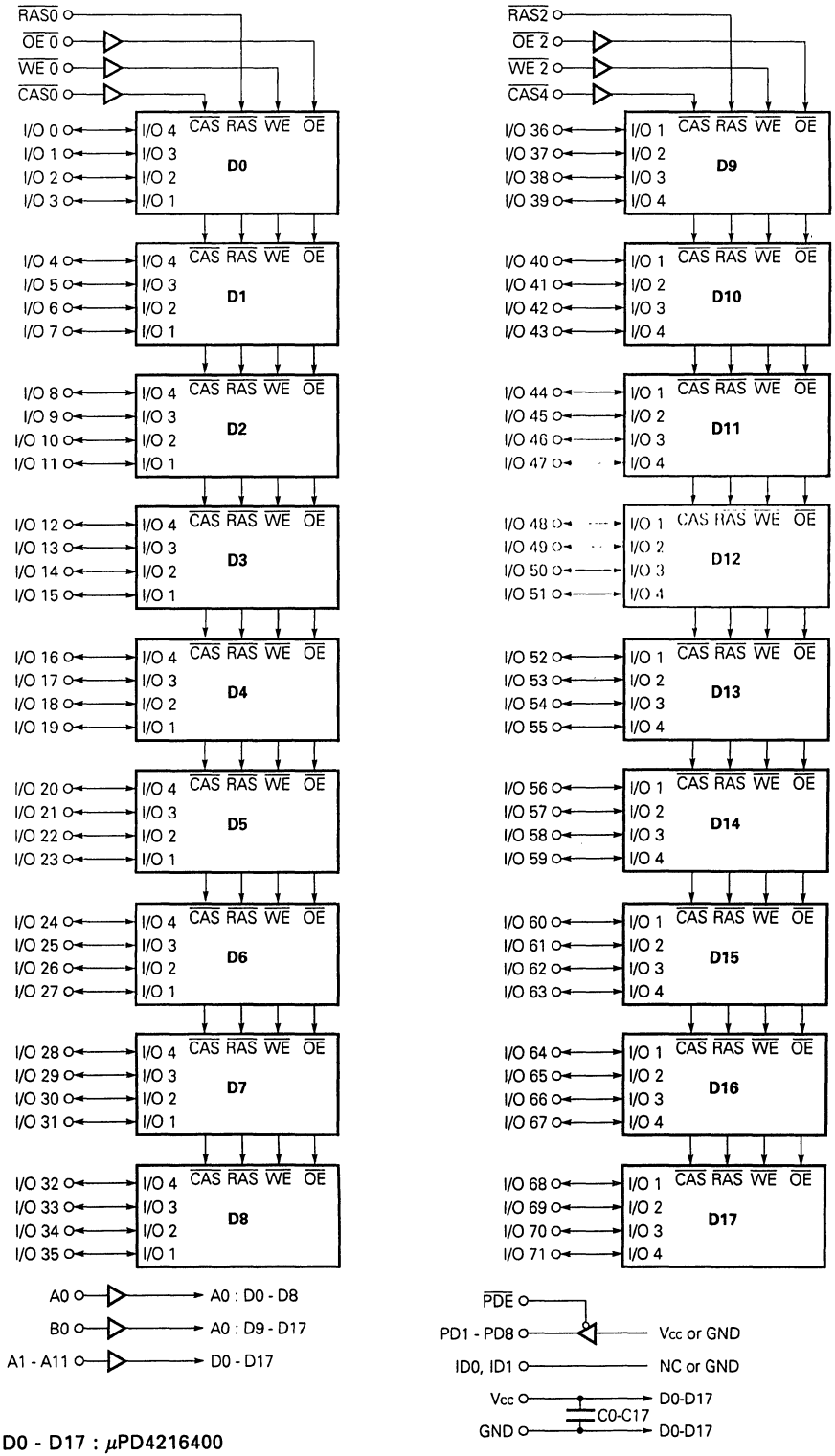
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	H	H	H
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A11, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D17 : μPD4216400

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		20	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = t_{RC} (MIN.) I_O = 0 mA	t_{RAC} = 60 ns		1,684	mA	3, 4, 7
			t_{RAC} = 70 ns		1,504		
			t_{RAC} = 80 ns		1,324		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.)	I_O = 0 mA		100	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V	I_O = 0 mA		82		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS}$ ≥ V_{IH} (MIN.) t_{RC} = t_{RC} (MIN.) I_O = 0 mA	t_{RAC} = 60 ns		1,684	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		1,504		
			t_{RAC} = 80 ns		1,324		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS}$ ≤ V_{IL} (MAX.), $\overline{CAS}$ Cycling t_{PC} = t_{PC} (MIN.) I_O = 0 mA	t_{RAC} = 60 ns		1,324	mA	3, 4, 6
			t_{RAC} = 70 ns		1,144		
			t_{RAC} = 80 ns		964		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling t_{RC} = t_{RC} (MIN.) I_O = 0 mA	t_{RAC} = 60 ns		1,684	mA	3, 4
			t_{RAC} = 70 ns		1,504		
			t_{RAC} = 80 ns		1,324		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V	RAS	–10	+10	μA	
			Others	–5	+1		
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

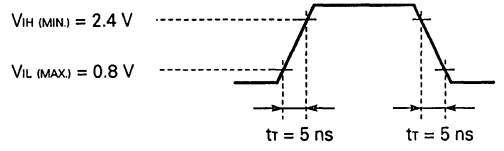
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	175		195		220		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		105		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		23		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40		43		50		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95		105		120		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	58		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60		65		75		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		64		64		64	ms	

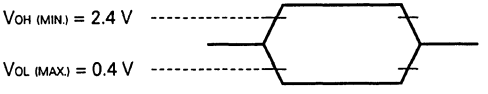
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

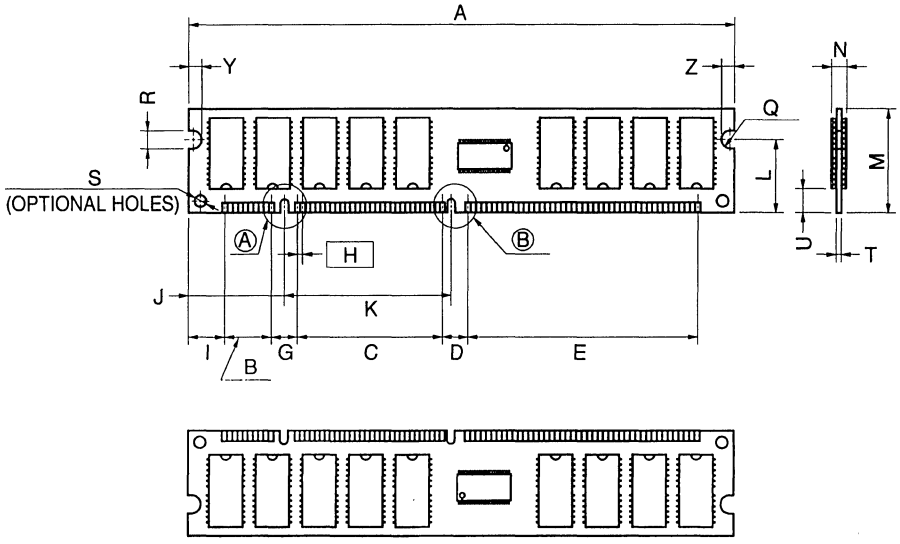
11. Loading conditions are 2 TTLs and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

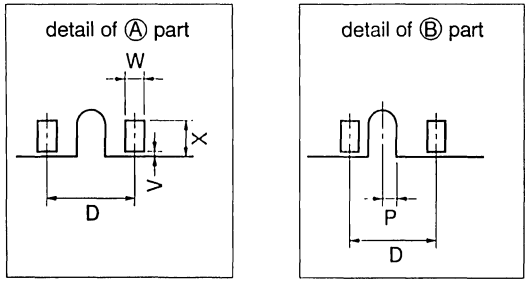
Timing Chart

Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A2

NEC

MOS INTEGRATED CIRCUIT

MC-424000LAB72F

3.3 V OPERATION 4 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-424000LAB72F is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μPD4217400L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000LAB72-A60	60 ns	110 ns	6.52 W	180 mW (CMOS level input)
MC-424000LAB72-A70	70 ns	130 ns	5.87 W	
MC-424000LAB72-A80	80 ns	150 ns	5.22 W	

- 2,048 refresh cycles/32 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

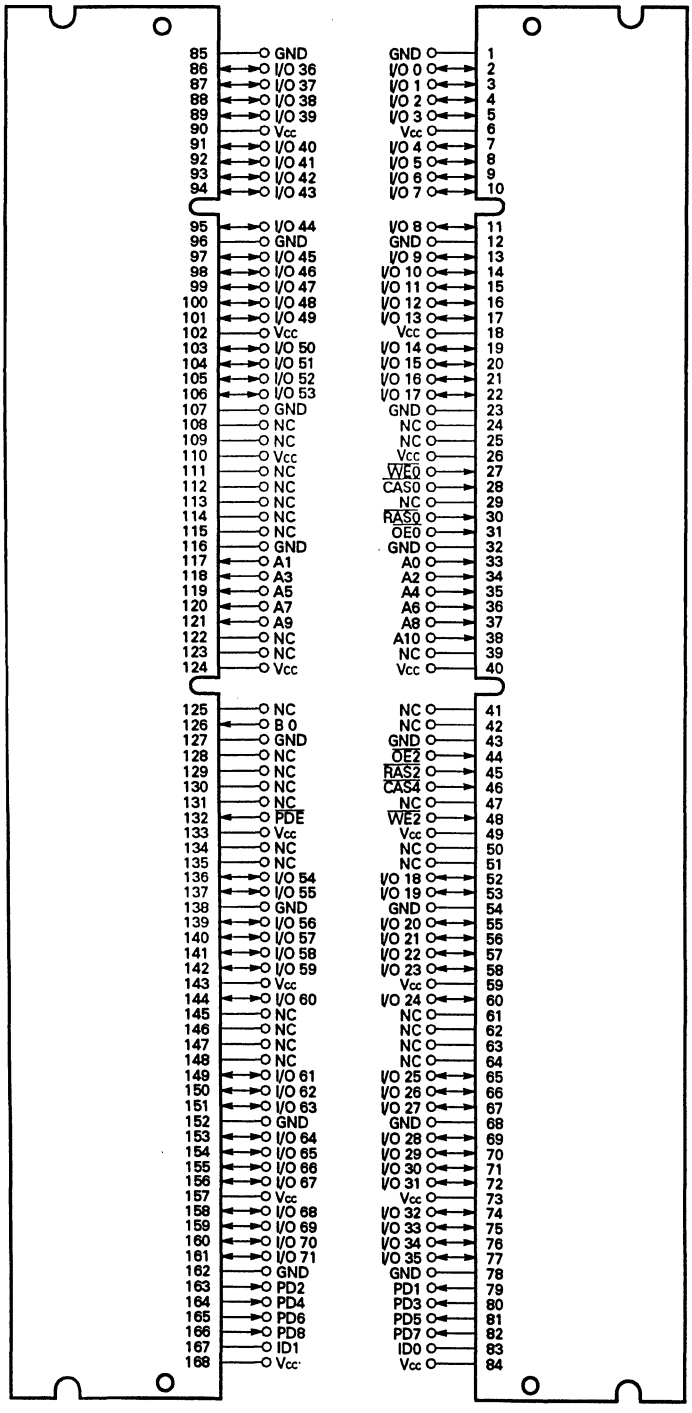
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000LAB72F-A60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of μPD4217400LG3 (300 mil TSOP(II)) [Double side]
MC-424000LAB72F-A70	70 ns		
MC-424000LAB72F-A80	80 ns		

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



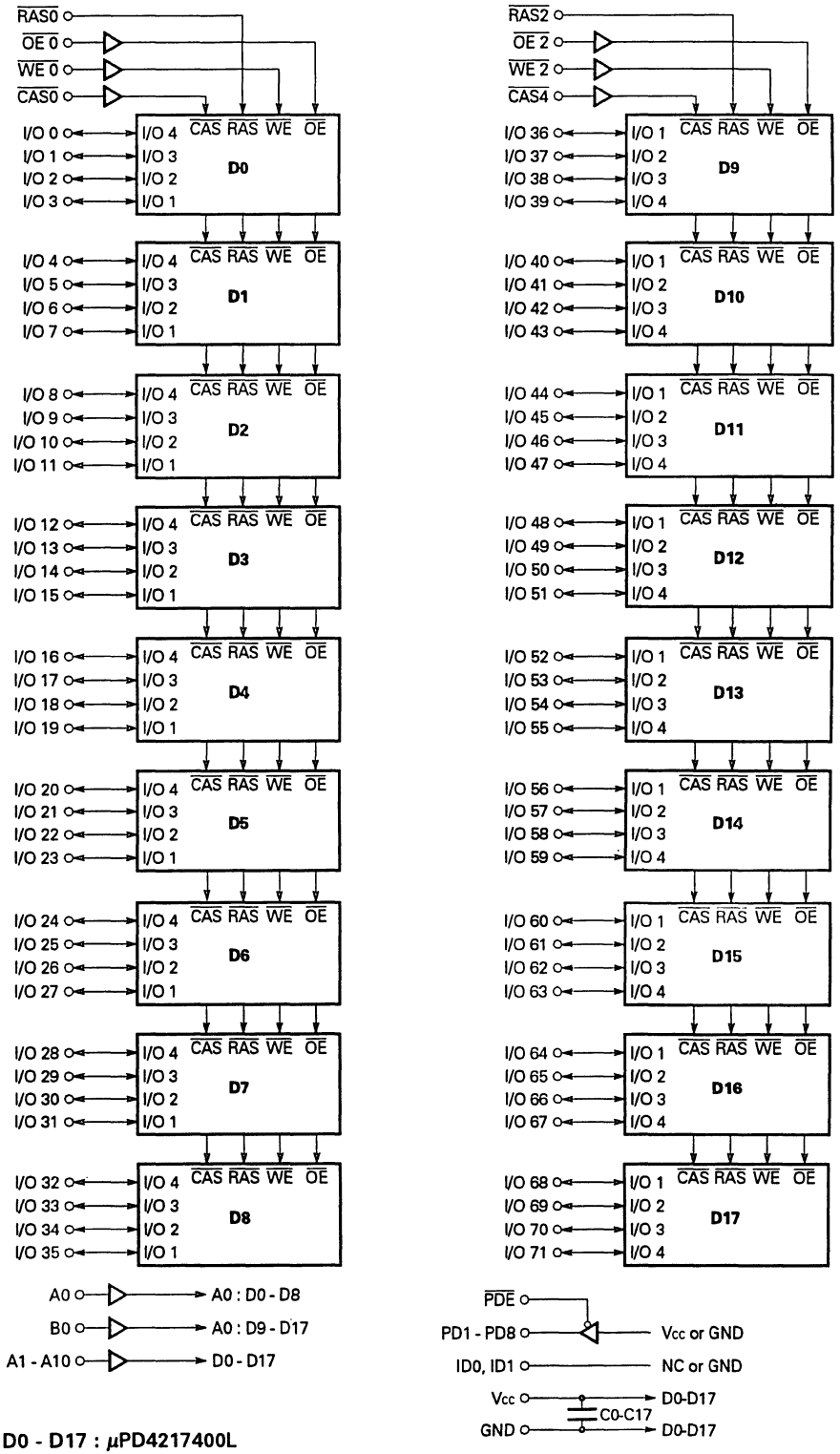
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	H	H	H
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A10, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D17 : μPD4217400L

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		–0.5 to +4.6	V
Supply voltage	V_{CC}		–0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		20	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,810	mA	3, 4, 7
			t_{RAC} = 70 ns		1,630		
			t_{RAC} = 80 ns		1,450		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		100	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		50		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,810	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		1,630		
			t_{RAC} = 80 ns		1,450		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,270	mA	3, 4, 6
			t_{RAC} = 70 ns		1,090		
			t_{RAC} = 80 ns		910		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,810	mA	3, 4
			t_{RAC} = 70 ns		1,630		
			t_{RAC} = 80 ns		1,450		
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V	$\overline{RAS}$	–5	+5	μA	
			Others	–5	+1		
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

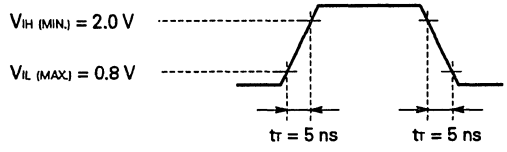
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	175		195		220		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		105		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		15		18		20	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OEB}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40		43		50		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95		105		120		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	58		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60		65		75		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		32		32		32	ms	

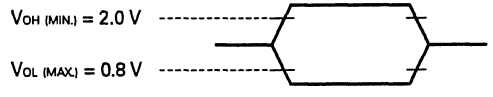
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

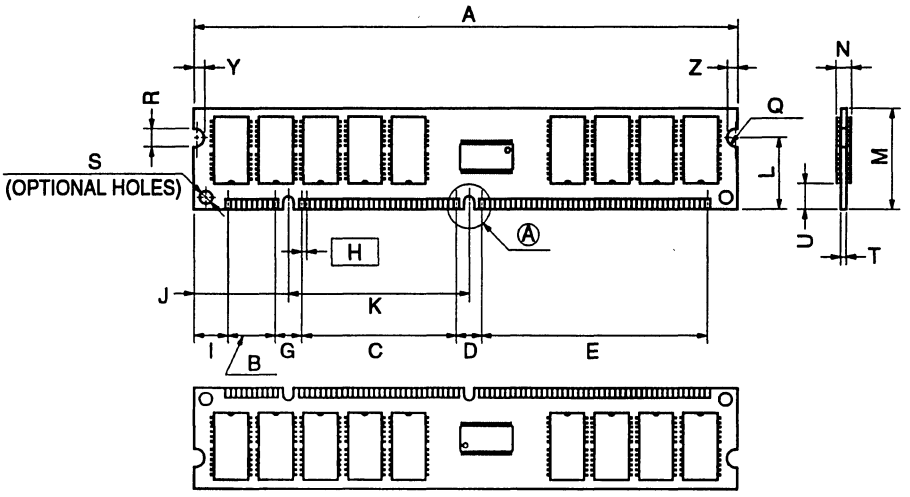
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP(MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
15. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.
16. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$ and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

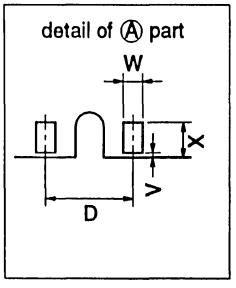
Timing Chart

Please refer to Timing Chart 7, page 429.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	43.18	1.700
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A3

8 Byte DIMM
[Hyper Page (EDO)]

NEC

MOS INTEGRATED CIRCUIT

MC-421000FA64FB

1 M-WORD BY 64-BIT DYNAMIC RAM MODULE HYPER PAGE MODE

Description

The MC-421000FA64FB is a 1,048,576 words by 64 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μPD4218165 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 1,048,576 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle Time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-421000FA64-60	60 ns	104 ns	25 ns	3.89 W	336 mW (CMOS level input)
MC-421000FA64-70	70 ns	124 ns	30 ns	3.68 W	

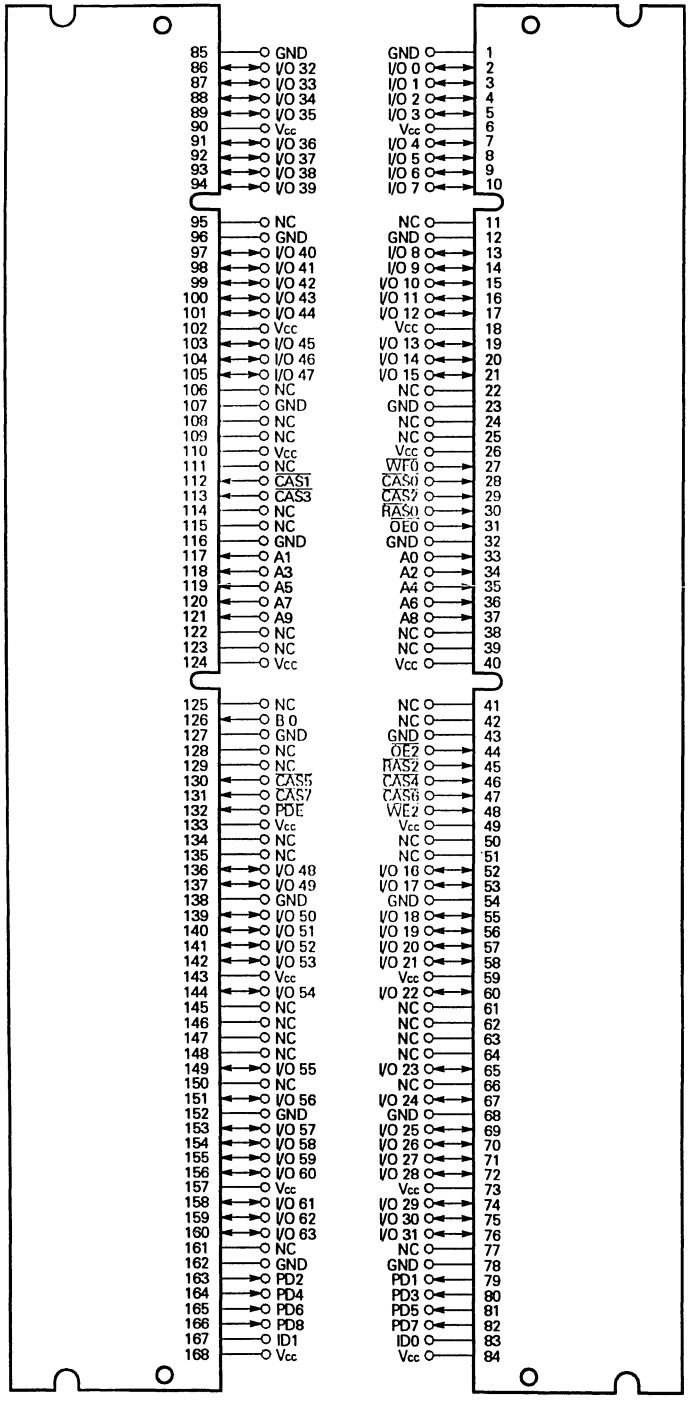
- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000FA64FB-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μPD4218165LE (400 mil SOJ) [Single side]
MC-421000FA64FB-70	70 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



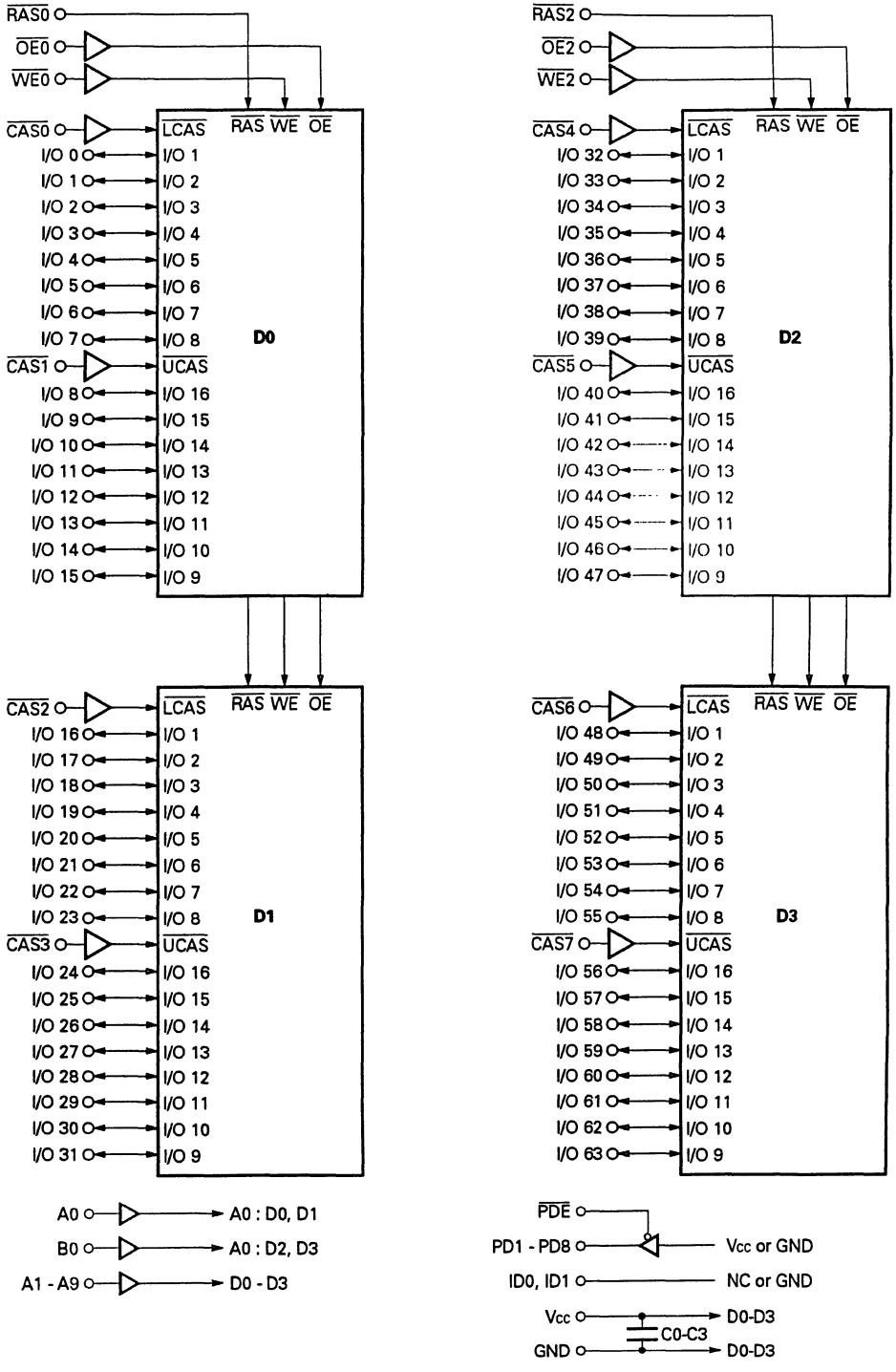
PD and ID Table

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD1	79	L	L
PD2	163	L	L
PD3	80	H	H
PD4	164	L	L
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	H	H
ID0	83	GND	GND
ID1	167	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 63 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D3 : μPD4218165

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		6	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			45	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS7}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O63			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		700	mA	1,2,3
			t_{RAC} = 70 ns		660		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$, I_O = 0 mA			68	mA	
		$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$ – 0.2 V, I_O = 0 mA			64		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geqq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		700	mA	1,2,3,4
			t_{RAC} = 70 ns		660		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$ $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		500	mA	1,2,5
			t_{RAC} = 70 ns		460		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		700	mA	1,2
			t_{RAC} = 70 ns		660		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V	$\overline{RAS}$	–10	+10	μA	
			others	–5	+1		
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.

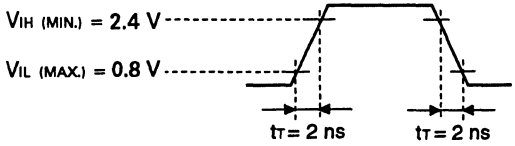
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

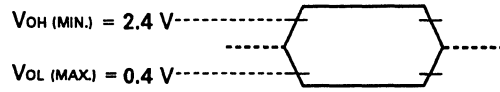
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write Cycle

Parameter	Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tRC	104	—	124	—	ns	
$\overline{RAS}$ Precharge Time	tRP	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	tCPN	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	tRAS	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width	tCAS	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	tCSH	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	—	5	—	ns	2
Row Address Setup Time	tASR	5	—	5	—	ns	
Row Address Hold Time	tRAH	10	—	10	—	ns	
Column Address Setup Time	tASC	0	—	0	—	ns	
Column Address Hold Time	tCAH	10	—	12	—	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	—	0	—	ns	
$\overline{CAS}$ to Data Setup Time	tCLZ	0	—	0	—	ns	
$\overline{OE}$ to Data Setup Time	tOLZ	0	—	0	—	ns	
$\overline{OE}$ to Data Delay Time	tOED	13	—	15	—	ns	
Masked Byte Write Hold Time Referenced to $\overline{RAS}$	tMRH	0	—	0	—	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
Refresh Time	tREF	—	16	—	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	23	ns	1
Access Time from Column Address	t_{AA}	—	35	—	40	ns	1
Access Time from $\overline{OE}$	t_{OEA}	—	20	—	23	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	2
Output buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	—	5	—	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not refernced V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	—	10	—	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	10	—	10	—	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	15	—	17	—	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	10	—	12	—	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	—	0	—	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	—	0	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	3
Data-in Hold Time	t_{DH}	10	—	10	—	ns	3

Notes 1. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	133	—	157	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	87	—	99	—	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	32	—	37	—	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	52	—	59	—	ns	1

Note 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$ the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	—	30	—	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125 000	70	125 000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	52	—	59	—	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	ns	
Read Modify Write Cycle Time	t_{HPRWC}	66	—	75	—	ns	
Data Output Hold Time	t_{DHC}	5	—	5	—	ns	
$\overline{OE}$ to CAS Hold Time	t_{OCH}	5	—	5	—	ns	
$\overline{OE}$ Precharge Time	t_{OEP}	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	10	—	10	—	ns	4
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3.4
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3.4

Notes 1. $t_{HPC(MIN.)}$ is applied to access time from $\overline{CAS}$

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
3. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.
4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.
   (1) $\overline{RAS}$, $\overline{CAS}$: Inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: inactive ··· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$,$\overline{OE}$:active and either t_{RRH} or t_{RCH} must be met··· t_{WEZ}, t_{WPZ} are effective.

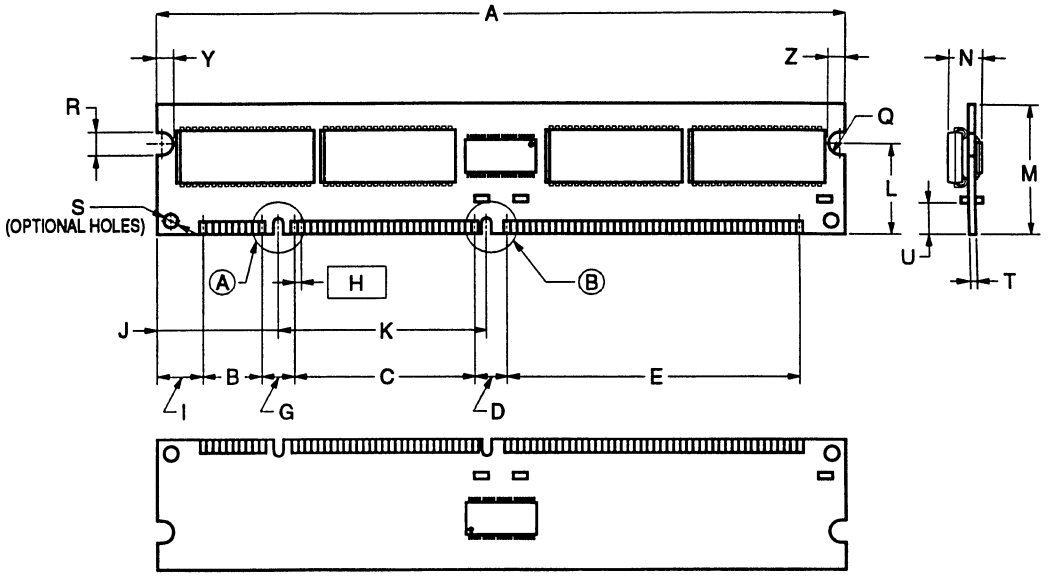
Refresh Cycle

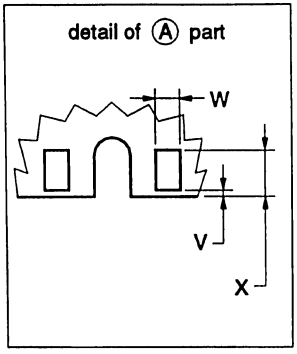
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	—	5	—	ns	
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t_{WHR}	15	—	15	—	ns	

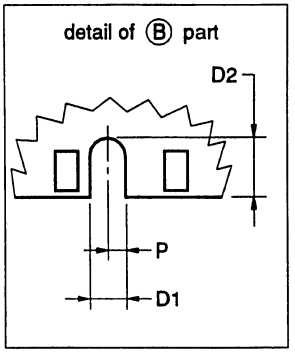
Timing Chart

Please refer to Timing Chart 9, page 457.

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.1230
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.05 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.7000
M	25.4±0.13	1.000±0.006
N	9.0 MAX.	0.355 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A5

NEC

MOS INTEGRATED CIRCUIT

MC-422000FA64FB

2 M-WORD BY 64-BIT DYNAMIC RAM MODULE HYPER PAGE MODE

Description

The MC-422000FA64FB is a 1,048,576 words by 64 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μPD4218165 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 2,096,152 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle Time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-422000FA64-60	60 ns	104 ns	25 ns	3.73 W	357 mW (CMOS level input)
MC-422000FA64-70	70 ns	124 ns	30 ns	3.52 W	

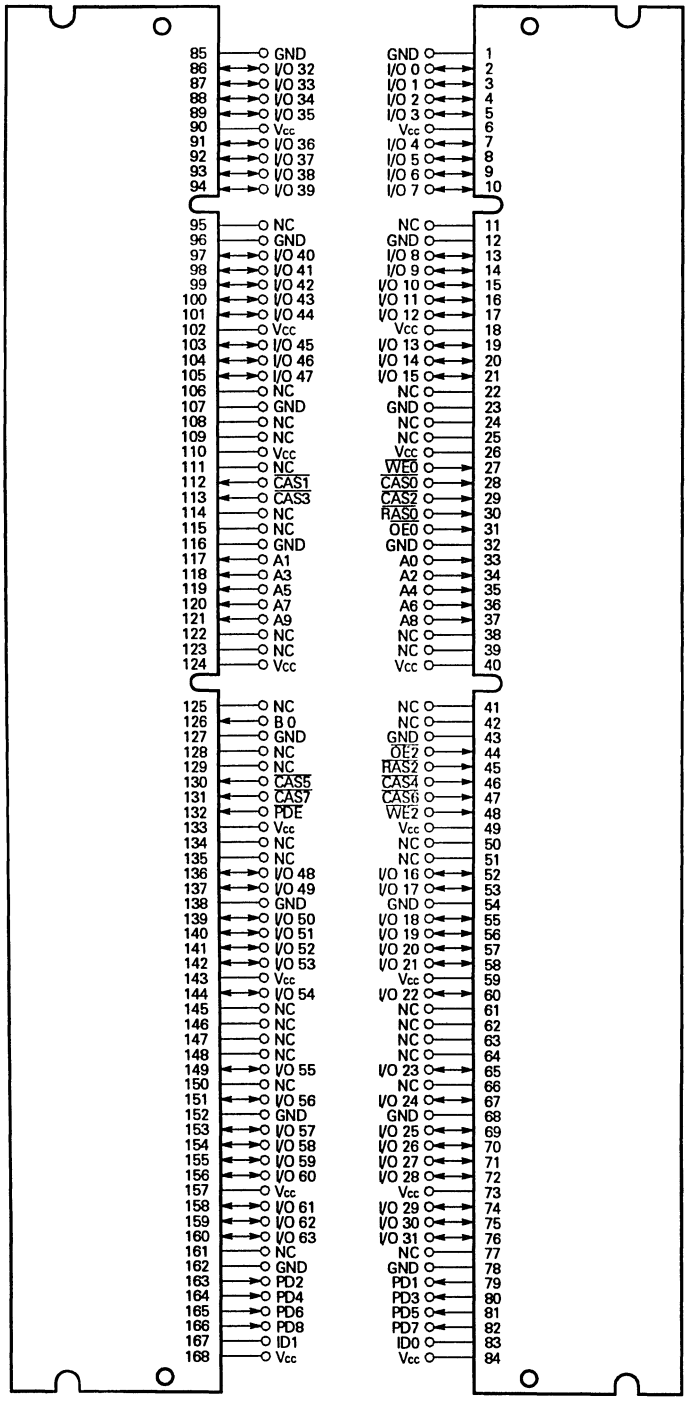
- 1,024 refresh cycles/16 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000FA64FB-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	8 pieces of μPD4218165LE (400 mil SOJ) [Single side]
MC-422000FA64FB-70	70 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



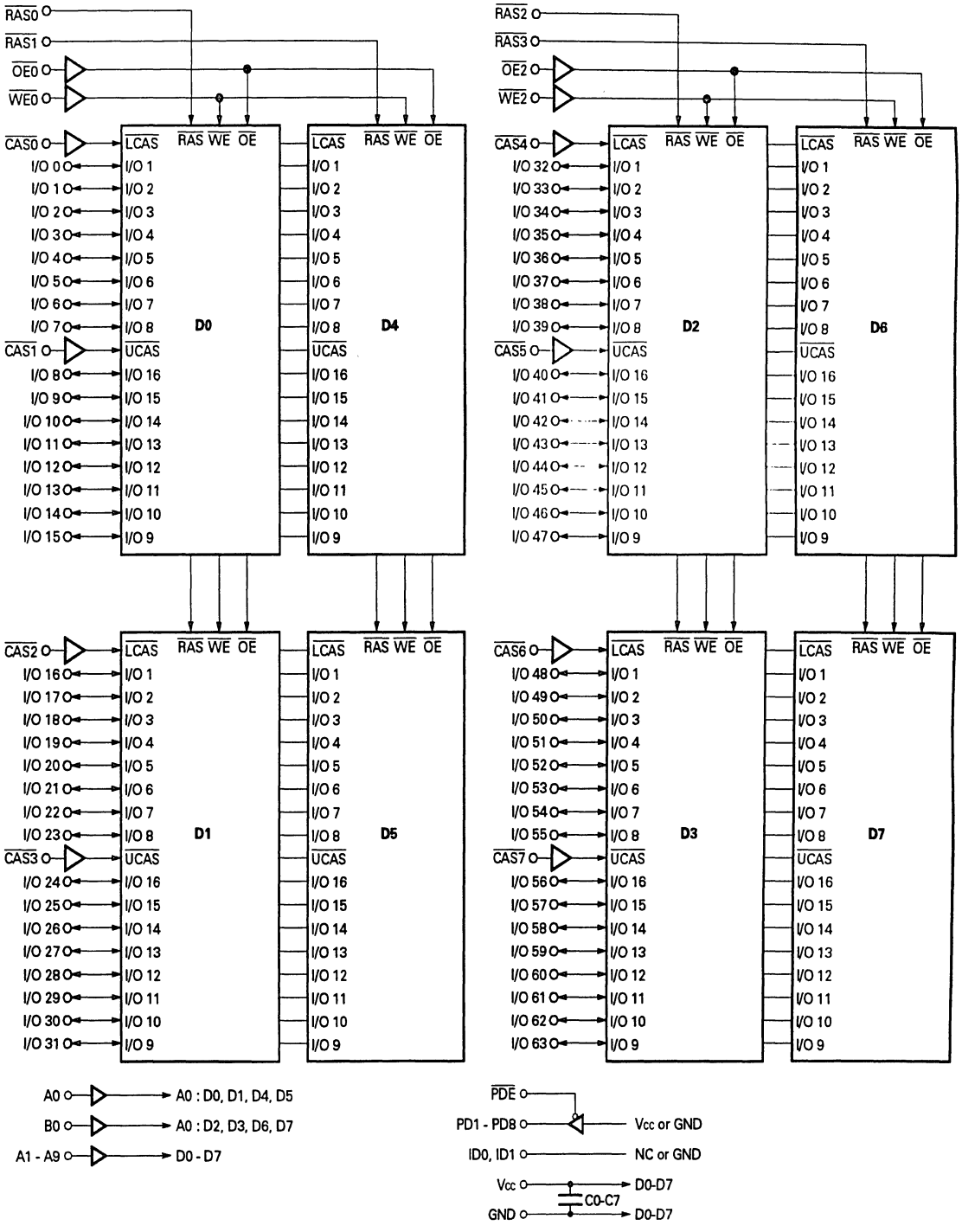
PD and ID Table

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD1	79	H	H
PD2	163	L	L
PD3	80	H	H
PD4	164	L	L
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	H	H
ID0	83	GND	GND
ID1	167	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 63 : Data Inputs/Outputs
$\overline{RAS0}$ - $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D7 : μPD4218165

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		6	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS2}$			45	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS7}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O63			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

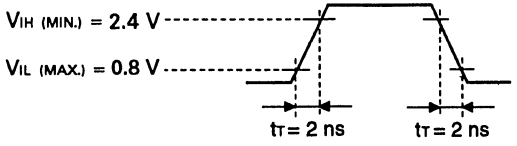
Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		710	mA	1,2,3
			t_{RAC} = 70 ns		670		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$, I_O = 0 mA			76	mA	
		$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$ – 0.2 V, I_O = 0 mA			68		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geqq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		710	mA	1,2,3,4
			t_{RAC} = 70 ns		670		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$ $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		510	mA	1,2,5
			t_{RAC} = 70 ns		470		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		710	mA	1,2
			t_{RAC} = 70 ns		670		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V	$\overline{RAS}$	–10	+10	μA	
			others	–5	+1		
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

Notes
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).
2. Specified values are obtained with outputs unloaded.
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

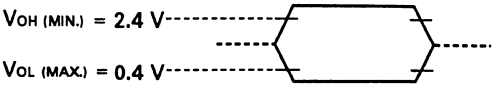
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write Cycle

Parameter	Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tRC	104	—	124	—	ns	
$\overline{RAS}$ Precharge Time	tRP	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	tCPN	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	tRAS	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width	tCAS	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	tCSH	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	—	5	—	ns	2
Row Address Setup Time	tASR	5	—	5	—	ns	
Row Address Hold Time	tRAH	10	—	10	—	ns	
Column Address Setup Time	tASC	0	—	0	—	ns	
Column Address Hold Time	tCAH	10	—	12	—	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	—	0	—	ns	
$\overline{CAS}$ to Data Setup Time	tCLZ	0	—	0	—	ns	
$\overline{OE}$ to Data Setup Time	tOLZ	0	—	0	—	ns	
$\overline{OE}$ to Data Delay Time	tOED	13	—	15	—	ns	
Masked Byte Write Hold Time Referenced to $\overline{RAS}$	tMRH	0	—	0	—	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
Refresh Time	tREF	—	16	—	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	23	ns	1
Access Time from Column Address	t_{AA}	—	35	—	40	ns	1
Access Time from $\overline{OE}$	t_{OEA}	—	20	—	23	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	2
Output buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	—	5	—	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not refernced V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	—	10	—	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	10	—	10	—	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	15	—	17	—	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	10	—	12	—	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	—	0	—	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	—	0	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	3
Data-in Hold Time	t_{DH}	10	—	10	—	ns	3

Notes 1. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	133	—	157	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	87	—	99	—	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	32	—	37	—	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	52	—	59	—	ns	1

Note 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$ the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	—	30	—	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125 000	70	125 000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	52	—	59	—	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	ns	
Read Modify Write Cycle Time	t_{HPRWC}	66	—	75	—	ns	
Data Output Hold Time	t_{DHC}	5	—	5	—	ns	
$\overline{OE}$ to CAS Hold Time	t_{OCH}	5	—	5	—	ns	
$\overline{OE}$ Precharge Time	t_{OEP}	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	10	---	10	—	ns	4
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3.4
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3.4

Notes 1. $t_{HPC(MIN.)}$ is applied to access time from $\overline{CAS}$

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

   (1) $\overline{RAS}$, $\overline{CAS}$: Inactive (at the end of read cycle)

   $\overline{WE}$: inactive, $\overline{OE}$: active

   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)

   $\overline{WE}$: inactive, $\overline{OE}$: inactive ··· t_{OEZ} is effective.

   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)

   $\overline{WE}$,$\overline{OE}$:active and either t_{RRH} or t_{RCH} must be met··· t_{WEZ}, t_{WPZ} are effective.

Refresh Cycle

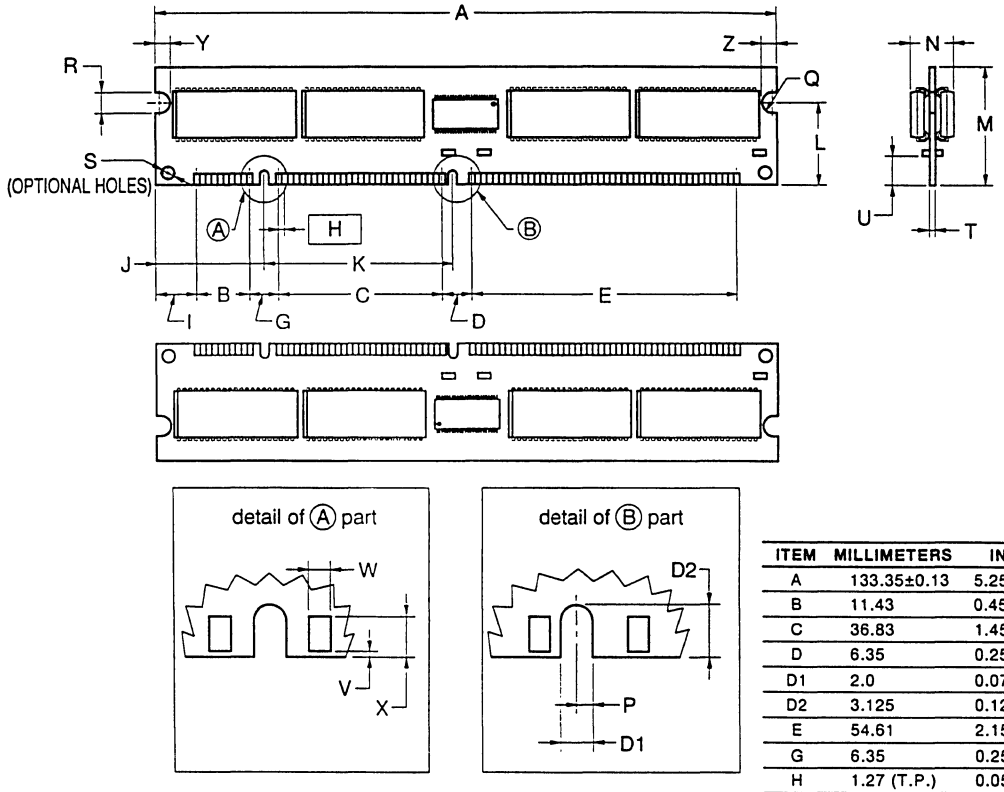
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	—	5	—	ns	
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t_{WHR}	15	—	15	—	ns	

Timing Chart

Please refer to Timing Chart 9, page 457.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.1230
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.05 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.7000
M	25.4±0.13	1.000±0.006
N	9.0 MAX.	0.355 MAX.
P	1.0	0.039
Q	R 2.0	R 0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ø3.0	ø0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A7

MC-422000FB72F

2M -WORD BY 72-BIT DYNAMIC RAM MODULE

HYPER PAGE MODE (ECC)

Description

The MC-422000FB72F is a 2 097 152 words by 72 bits dynamic RAM module on which 9 pieces of 16M DRAM (μPD 4217805) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 2 097 152 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC- 422000FB72-60	60 ns	104 ns	25 ns	5.51w	368mw (CMOS level)
MC- 422000FB72-70	70 ns	124 ns	30 ns	5.04w	

- 2 048 refresh cycles/32 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh , $\overline{\text{RAS}}$ only refresh , Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +5.0 V±0.25V power supply

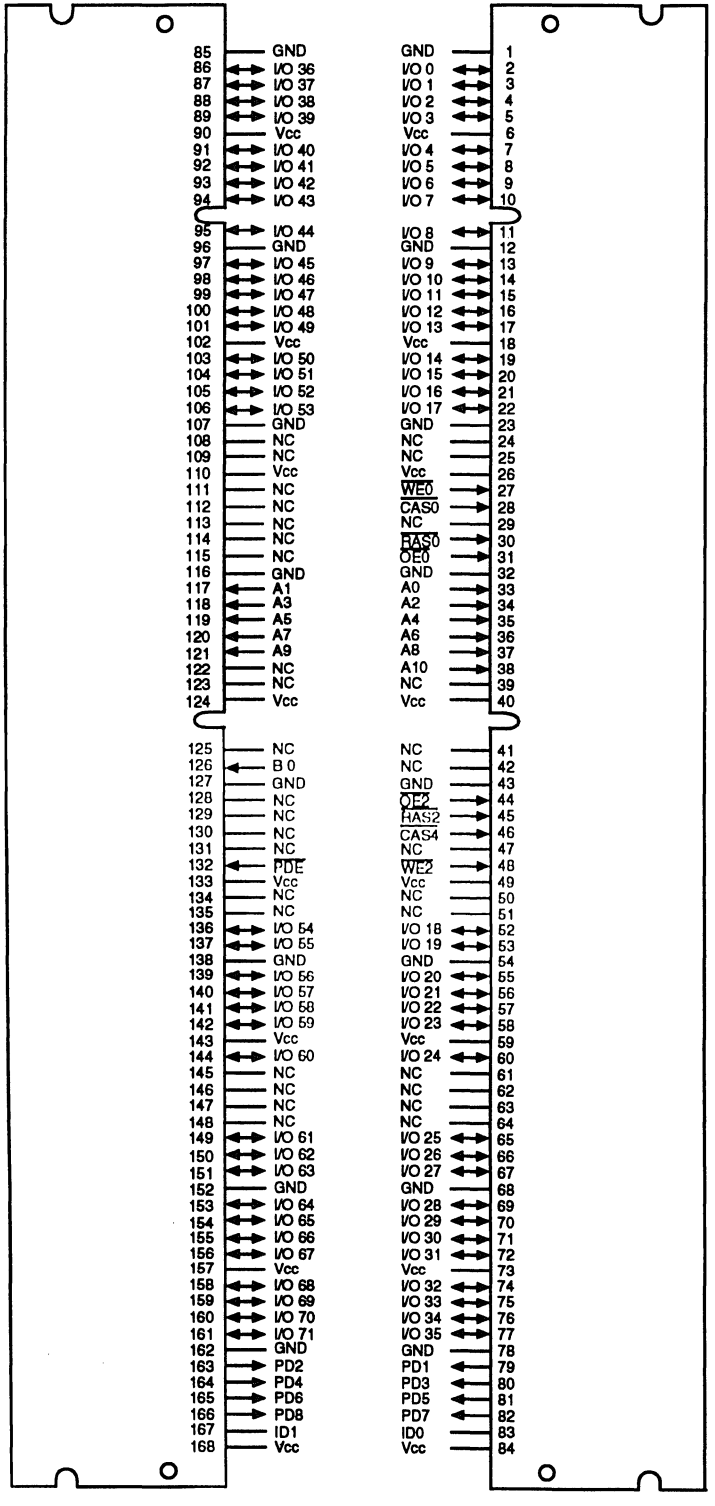
Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 422000FB72F-60	60ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	9 pieces of uPD 4217805G5 (400mil TSOP) [Double side]
MC- 422000FB72F-70	70ns		

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



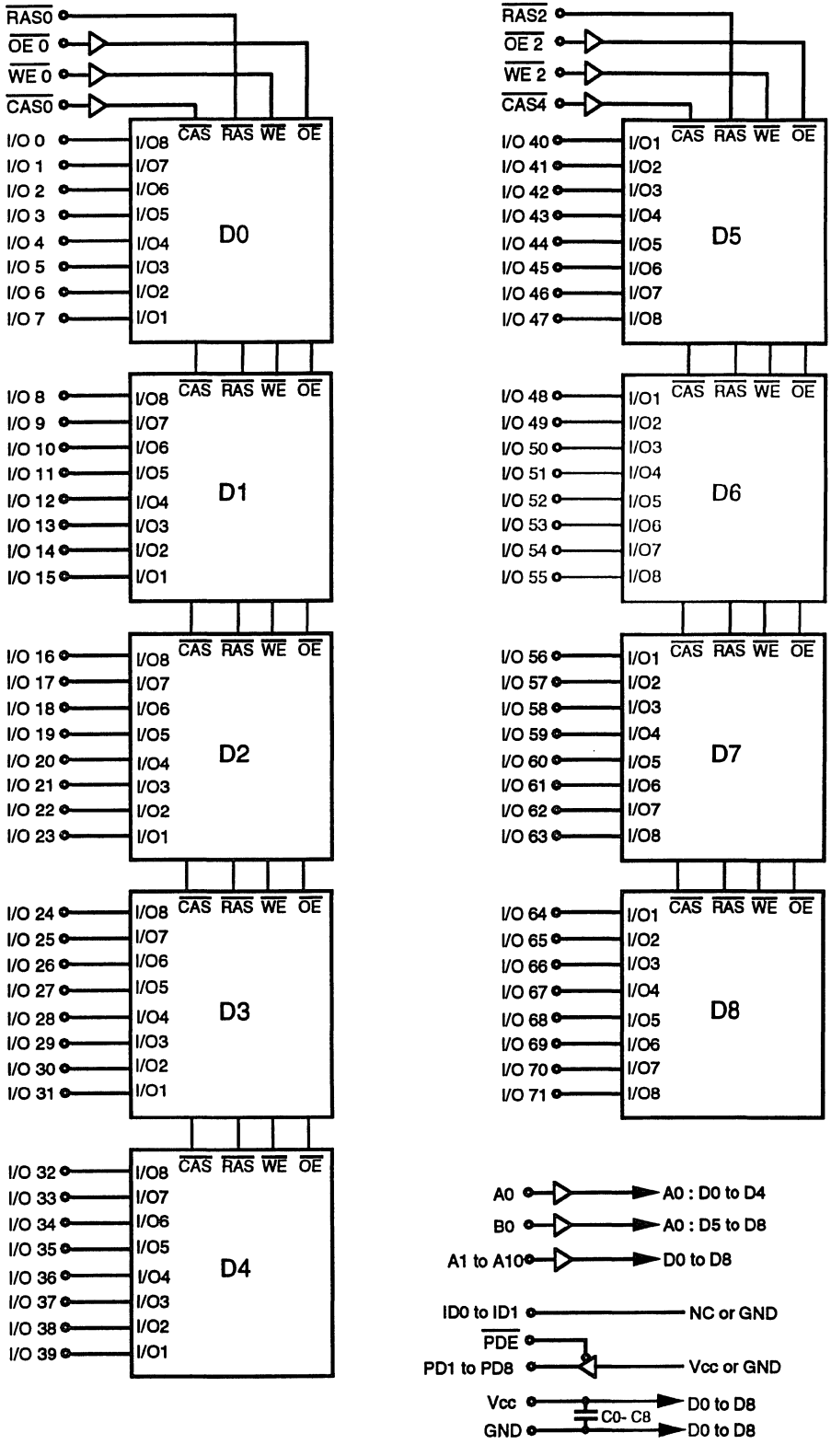
PD and ID Table

Pin Name	Pin No.	Accsess Time	
		60ns	70ns
PD1	79	H	H
PD2	163	L	L
PD3	80	L	L
PD4	164	H	H
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	L	L
I D0	83	GND	GND
I D1	167	GND	GND

Note) H : VOH, L : VOL

A0 - A10, B0 : Address Inputs
I/O 0-I/O 71 : Data Inputs / Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1- PD8 : Presence Detect Pins
ID0, ID1 : Identity pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-1.0 to +7.0	V
Supply voltage	VCC		-1.0 to +7.0	V
Output current	IO		50	mA
Power dissipation	PD		11	W
Operating temperature	Topt		0 to +70	℃
Storage temperature	Tstg		-55 to +125	℃

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device in not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES: 1, 2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		4.75	5.0	5.25	V
High level input voltage	VIH		2.4		Vcc + 1.0	V
Low level input voltage	VIL		-1.0		+0.8	V
Ambient temperature	Ta		0		70	℃

CAPACITANCE (Ta=25℃, f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI1	A0 - A10, B0			20	pF
	CI2	$\overline{WE0}$, $\overline{WE2}$			20	pF
	CI3	$\overline{RAS0}$, $\overline{RAS2}$			50	pF
	CI4	$\overline{CAS0}$, $\overline{CAS4}$			20	pF
	CI5	$\overline{OE0}$, $\overline{OE2}$			20	pF
Data Input/ Output capacitance	CI/O	I/O 0 - I/O 71			20	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
Operating Current	Icc1	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}=t_{RC(MIN.)}$, IO=0mA	t_{RAC}=60ns		1 050	mA	3, 4, 7
			t_{RAC}=70ns		960		
Standby Current	Icc2	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH(MIN.)}$			90	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ Vcc-0.2V			70		
$\overline{RAS}$ only refresh current	Icc3	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≧ V_{IH} $t_{RC}=t_{RC(MIN.)}$, IO=0mA	t_{RAC}=60ns		1 050	mA	3, 4, 5, 7
			t_{RAC}=70ns		960		
Operating Current (Hyper Page Mode)	Icc4	$\overline{RAS}$ ≦ VIL, $\overline{CAS}$ Cycling tHPC=tHPC (MIN.), IO=0mA	t_{RAC}=60ns		870	mA	3, 4, 6
			t_{RAC}=70ns		780		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	Icc5	$t_{RC}=t_{RC(MIN.)}$ IO=0mA	t_{RAC}=60ns		1 050	mA	3, 4
			t_{RAC}=70ns		960		
Input Leakage Current	$I_{I(L)}$	VI=0 to 5.25V all other pins not under test = 0V	$\overline{RAS}$	-10	+10	μA	
			others	-5	+1		
Output Leakage Current	$I_{O(L)}$	Outputs are disabled (Hi - Z) VO=0 to 5.25V		-10	+10	μA	
High level output voltage	V_{OH}	IO=-5.0mA		2.4		V	
Low level output voltage	V_{OL}	IO=+4.2mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Notes 8,9

(1/2)

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	tRC	104	-	124	-	ns	
Read Modify Write Cycle Time	tRWC	133	-	157	-	ns	
Access Time from $\overline{RAS}$	tRAC	-	60	-	70	ns	10,11
Access Time from $\overline{CAS}$	tCAC	-	20	-	23	ns	10,11
Access Time from Column Address	tAA	-	35	-	40	ns	10,11
Access Time from $\overline{CAS}$ Precharge	tACP	-	40	-	45	ns	11
Access Time from $\overline{OE}$	tOEA	-	20	-	23	ns	11
$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	10
$\overline{CAS}$ to Data Setup Time	tCLZ	0	-	0	-	ns	11
$\overline{OE}$ to Data Setup Time	tOLZ	0	-	0	-	ns	11
$\overline{OE}$ to Data Delay Time	tOED	13	-	15	-	ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	tOEZ	0	13	0	15	ns	12
$\overline{OE}$ Hold Time	tOEH	0	-	0	-	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	-	0	-	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
$\overline{RAS}$ Precharge Time	tRP	40	-	50	-	ns	
$\overline{RAS}$ Pulse Width	tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	-	12	-	ns	
$\overline{CAS}$ Pulse Width	tCAS	10	10,000	12	10,000	ns	
$\overline{CAS}$ Hold Time	tCSH	40	-	50	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	52	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	-	5	-	ns	13
$\overline{CAS}$ Precharge Time	tCPN	10	-	10	-	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	tRPC	5	-	5	-	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	tRHCP	40	-	45	-	ns	
Row Address Setup Time	tASR	5	-	5	-	ns	
Row Address Hold Time	tRAH	10	-	10	-	ns	
Column Address Setup Time	tASC	0	-	0	-	ns	
Column Address Hold Time	tCAH	10	-	12	-	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	tRAL	30	-	35	-	ns	
Read Command Setup Time	tRCS	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0	-	0	-	ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0	-	0	-	ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	tWCH	10	-	10	-	ns	15
$\overline{WE}$ Pulse Width	tWP	10	-	10	-	ns	15
Data-in Setup Time	tDS	0	-	0	-	ns	16
Data-in Hold Time	tDH	10	-	10	-	ns	16
Write command Setup Time	tWCS	0	-	0	-	ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	tCWD	32	-	37	-	ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	tRWD	87	-	99	-	ns	17
Column Address to $\overline{WE}$ Delay Time	tAWD	52	-	59	-	ns	17

(2/2)

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	tRWL	15	-	17	-	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	tCWL	10	-	12	-	ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCSR	5	-	5	-	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCHR	10	-	10	-	ns	
$\overline{WE}$ Setup Time	tWSR	10	-	10	-	ns	
$\overline{WE}$ Hold Time	tWHR	15	-	15	-	ns	
Refresh Time	tREF	-	32	-	32	ms	

HYPER PAGE MODE

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tHPC	25	-	30	-	ns	
$\overline{RAS}$ Pulse Width	tRASP	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	tHCAS	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	tCP	10	-	10	-	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	tCPWD	52	-	59	-	ns	17
Read Modify Write Cycle Time	tHPRWC	66	-	75	-	ns	
Data Output Hold Time	tDHC	5	-	5	-	ns	
$\overline{OE}$ to CAS Hold Time	tOCH	5	-	5	-	ns	18
$\overline{OE}$ Precharge Time	tOEP	5	-	5	-	ns	
$\overline{CAS}$ Hold Time to $\overline{OE}$	tCHO	5	-	5	-	ns	18
Output Buffer Turn-off Delay from $\overline{WE}$	tWEZ	0	13	0	15	ns	12, 18
$\overline{WE}$ Pulse Width	tWPZ	10	-	10	-	ns	18
Output Buffer Turn-off Delay from $\overline{RAS}$	tOFR	0	13	0	15	ns	12, 18
Output Buffer Turn-off Delay from $\overline{CAS}$	tOFC	0	13	0	15	ns	12, 18

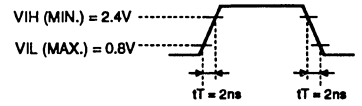
Notes:

1. All voltages are referenced to GND.
2. After power up, wait more than 100 µs and then, execute eight CAS before RAS or RAS only refresh cycles as dummy cycles to initialize internal circuit.
3. ICC1, ICC3, ICC4 and ICC5 depend on cycle rates (tRC and tHPC).
4. Specified values are obtained with outputs unloaded.
5. ICC3 is measured assuming that all column address inputs are held at either high or low.
6. ICC4 is measured assuming that all column address inputs are switched only once during each Hyper page cycle.
7. ICC1 and ICC3 are measured assuming that address can be changed once or less during RAS≦VIL(MAX.) and CAS≧VIH(MIN.).
8. AC measurements assume tT =2ns.

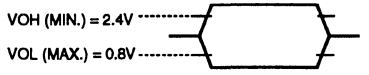
Notes:

9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
tRAD ≦ tRAD(MAX.) and tRCD ≦ tRCD(MAX.)	tRAC(MAX.)	tRAC(MAX.)
tRAD > tRAD(MAX.) and tRCD ≦ tRCD(MAX.)	tAA(MAX.)	tRAD + tAA(MAX.)
tRCD > tRCD(MAX.)	tCAC(MAX.)	tRCD + tCAC(MAX.)

tRAD(MAX.) and tRCD(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (tRAC, tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions tRAD≧tRAD(MAX.) and tRCD≧tRCD(MAX.) will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. tOFC (MAX.), tOFR(MAX.), tWEZ (MAX.) and tOEZ(MAX.) defines the time when the output achieves the condition of Hi-Z and are not referenced to VOH or VOL.
13. tCRP(MIN.) requirement is applied to $\overline{RAS}$ / $\overline{CAS}$ cycles preceded by any cycles.
14. Either tRCH(MIN.) or tRRH(MIN.) should be met in read cycles.
15. tWP(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, tWCH (MIN.) should be met.
16. tDS(MIN.) and tDH(MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If tWCS≧tWCS (MIN.), the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If tRWD≧tRWD (MIN.), tCWD≧tCWD(MIN.), tAWD≧tAWD(MIN.) and tCPWD≧tCPWD(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
18. To make I/O to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) $\overline{RAS}$, $\overline{CAS}$: inactive (at the end of read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
tOFC is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
tOFR is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

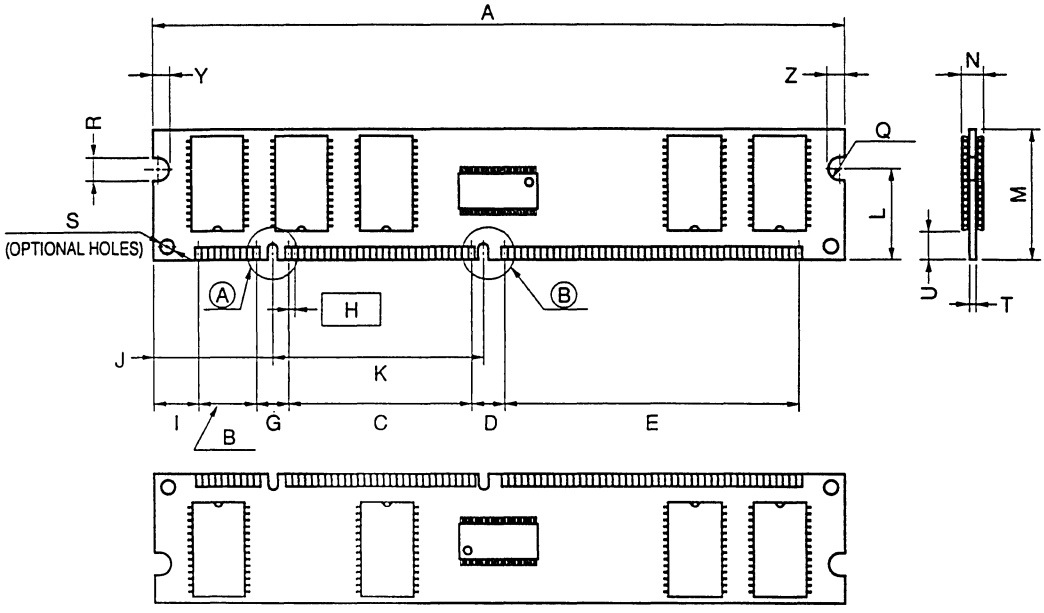
(2) Both RAS and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$: active, $\overline{OE}$: active...tWEZ, tWPZ are effective.
$\overline{WE}$: inactive, $\overline{OE}$: inactive...tOEZ is effective.

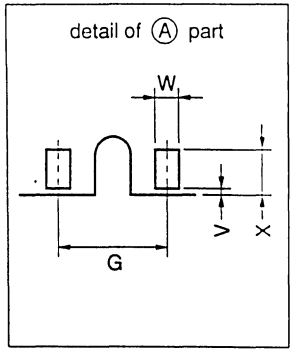
Timing Chart

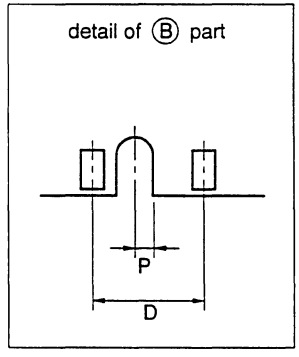
Please refer to Timing Chart 10, page 473.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE) OUTLINE DRAWINGS







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54	0.100
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A6

MOS INTEGRATED CIRCUIT

MC-422000LFB72F

3.3 V OPERATION 2M -WORD BY 72-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (ECC)

Description

The MC-422000LFB72F is a 2 097 152 words by 72 bits dynamic RAM module on which 9 pieces of 16M DRAM (μPD 4217805L) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 2 097 152 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC- 422000LFB72-A60	60 ns	104 ns	25 ns	3.28 w	147.6mw (CMOS level)
MC- 422000LFB72-A70	70 ns	124 ns	30 ns	2.95 w	

- 2 048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh , $\overline{RAS}$ only refresh , Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +3.3 V±0.3V power supply

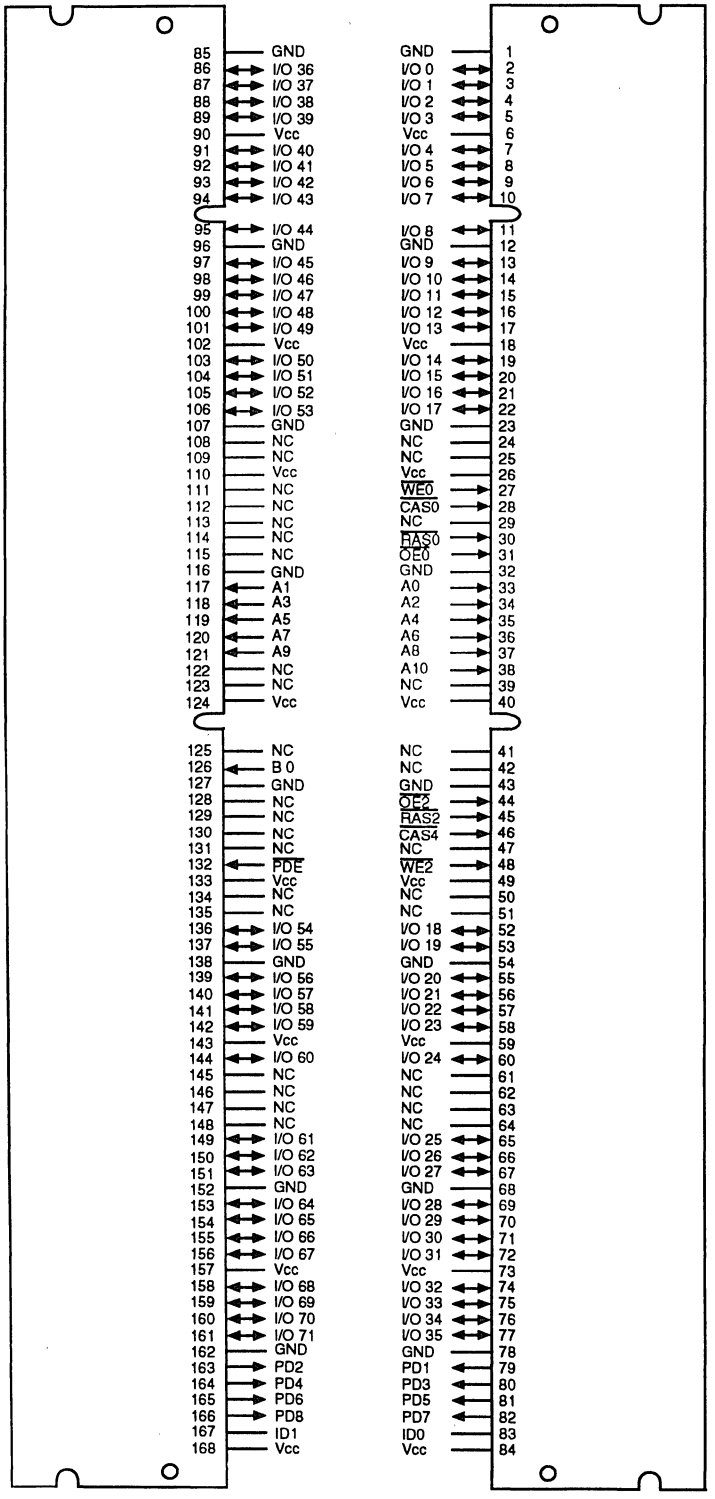
Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 422000LFB72F-A60	60ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	9 pieces of uPD 4217805LG5 (400mil TSOP) [Double side]
MC- 422000LFB72F-A70	70ns		

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



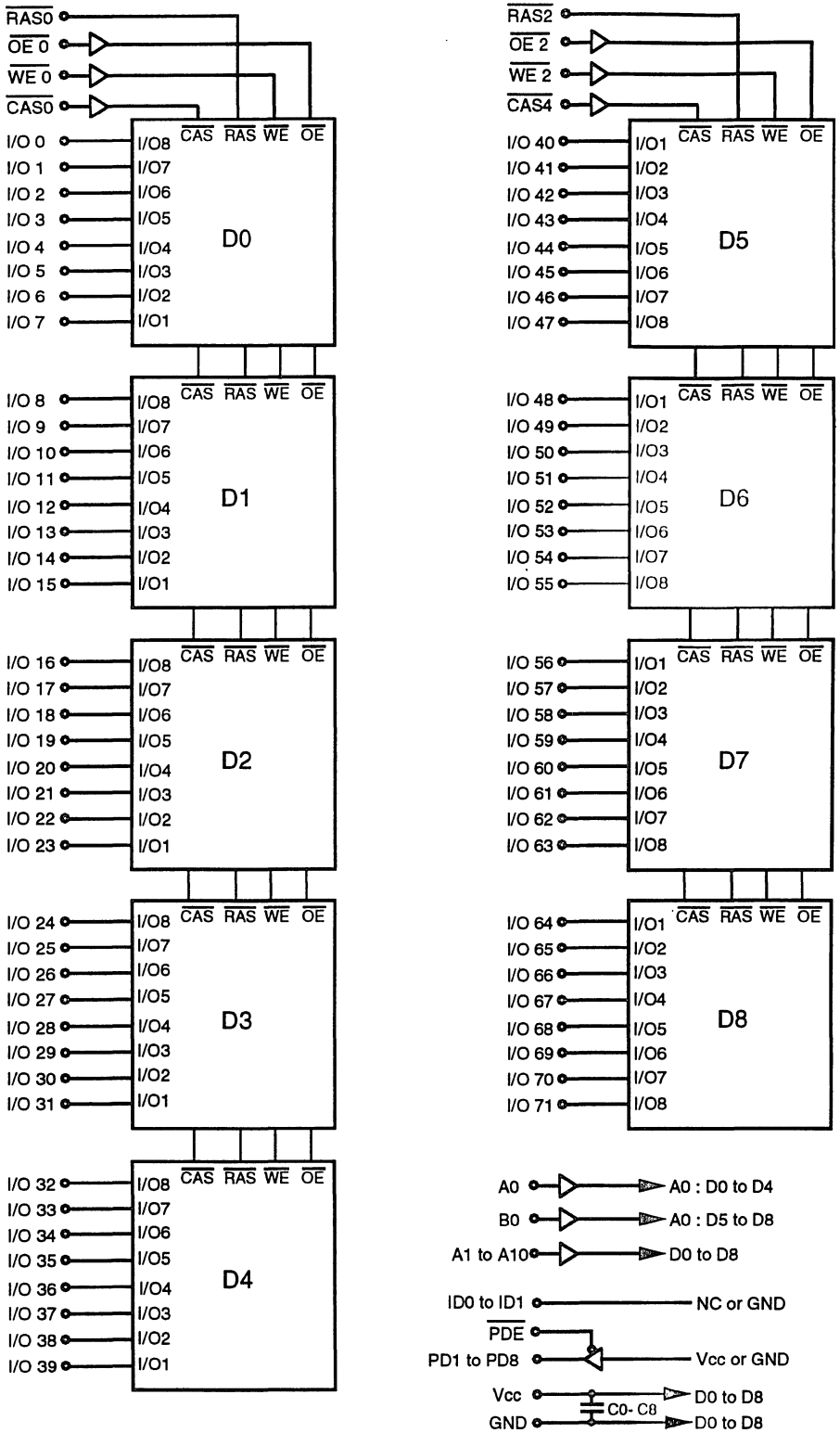
PD and ID Table

Pin Name	Pin No.	Accsess Time	
		60ns	70ns
PD1	79	H	H
PD2	163	L	L
PD3	80	L	L
PD4	164	H	H
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	L	L
ID0	83	GND	GND
ID1	167	GND	GND

Note) H : VOH, L : VOL

A0 - A10, B0 : Address Inputs
I/O 0-I/O 71 : Data Inputs / Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1- PD8 : Presence Detect Pins
ID0, ID1 : Identity pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-0.5 to +4.6	V
Supply voltage	VCC		-0.5 to +4.6	V
Output current	IO		20	mA
Power dissipation	PD		11	W
Operating temperature	Topt		0 to +70	℃
Storage temperature	Tstg		-55 to +125	℃

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device in not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES : 1, 2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		3.0	3.3	3.6	V
High level input voltage	VIH		2.0		Vcc + 0.3	V
Low level input voltage	VIL		-0.3		+0.8	V
Ambient temperature	Ta		0		70	℃

CAPACITANCE (Ta=25℃, f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI1	A0 - A10, B0			20	pF
	CI2	$\overline{WE0}$, $\overline{WE2}$			20	pF
	CI3	$\overline{RAS0}$, $\overline{RAS2}$			50	pF
	CI4	$\overline{CAS0}$, $\overline{CAS4}$			20	pF
	CI5	$\overline{OE0}$, $\overline{OE2}$			20	pF
Data Input/ Output capacitance	CI/O	I/O 0 - I/O 71			20	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
Operating Current	Icc1	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}=t_{RC\,(MIN.)}$, IO=0mA	t_{RAC}=60ns		910	mA	3, 4, 7
			t_{RAC}=70ns		820		
Standby Current	Icc2	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH\,(MIN.)}$			82	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ Vcc-0.2V			41		
$\overline{RAS}$ only refresh current	Icc3	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≧ V_{IH} $t_{RC}=t_{RC\,(MIN.)}$, IO=0mA	t_{RAC}=60ns		910	mA	3, 4, 5, 7
			t_{RAC}=70ns		820		
Operating Current (Hyper Page Mode)	Icc4	$\overline{RAS}$ ≦ VIL, $\overline{CAS}$ Cycling tHPC=tHPC (MIN.), IO=0mA	t_{RAC}=60ns		820	mA	3, 4, 6
			t_{RAC}=70ns		730		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	Icc5	$t_{RC}=t_{RC\,(MIN.)}$ IO=0mA	t_{RAC}=60ns		910	mA	3, 4
			t_{RAC}=70ns		820		
Input Leakage Current	$I_{I(L)}$	VI=0 to 3.6V all other pins not under test = 0V	$\overline{RAS}$	-5	+5	μA	
			others	-5	+1		
Output Leakage Current	$I_{O(L)}$	Outputs are disabled (Hi - Z) VO=0 to 3.6V		-5	+5	μA	
High level output voltage	V_{OH}	IO=-2.0mA		2.4		V	
Low level output voltage	V_{OL}	IO=+2.0mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Notes 8,9

(1/2)

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	tRC	104	-	124	-	ns	
Read Modify Write Cycle Time	tRWC	133	-	157	-	ns	
Access Time from $\overline{RAS}$	tRAC	-	60	-	70	ns	10,11
Access Time from $\overline{CAS}$	tCAC	-	20	-	23	ns	10,11
Access Time from Column Address	tAA	-	35	-	40	ns	10,11
Access Time from $\overline{CAS}$ Precharge	tACP	-	40	-	45	ns	11
Access Time from $\overline{OE}$	tOEA	-	20	-	23	ns	11
$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	10
$\overline{CAS}$ to Data Setup Time	tCLZ	0	-	0	-	ns	11
$\overline{OE}$ to Data Setup Time	tOLZ	0	-	0	-	ns	11
$\overline{OE}$ to Data Delay Time	tOED	13	-	15	-	ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	tOEZ	0	13	0	15	ns	12
$\overline{OE}$ Hold Time	tOEH	0	-	0	-	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	-	0	-	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
$\overline{RAS}$ Precharge Time	tRP	40	-	50	-	ns	
$\overline{RAS}$ Pulse Width	tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	-	12	-	ns	
$\overline{CAS}$ Pulse Width	tCAS	10	10,000	12	10,000	ns	
$\overline{CAS}$ Hold Time	tCSH	40	-	50	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	52	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	-	5	-	ns	13
$\overline{CAS}$ Precharge Time	tCPN	10	-	10	-	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	tRPC	5	-	5	-	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	tRHCP	40	-	45	-	ns	
Row Address Setup Time	tASR	5	-	5	-	ns	
Row Address Hold Time	tRAH	10	-	10	-	ns	
Column Address Setup Time	tASC	0	-	0	-	ns	
Column Address Hold Time	tCAH	10	-	12	-	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	tRAL	30	-	35	-	ns	
Read Command Setup Time	tRCS	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0	-	0	-	ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0	-	0	-	ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	tWCH	10	-	10	-	ns	15
$\overline{WE}$ Pulse Width	tWP	10	-	10	-	ns	15
Data-in Setup Time	tDS	0	-	0	-	ns	16
Data-in Hold Time	tDH	10	-	10	-	ns	16
Write command Setup Time	tWCS	0	-	0	-	ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	tCWD	32	-	37	-	ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	tRWD	87	-	99	-	ns	17
Column Address to $\overline{WE}$ Delay Time	tAWD	52	-	59	-	ns	17

(2/2)

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	tRWL	15	-	17	-	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	tCWL	10	-	12	-	ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCSR	5	-	5	-	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCHR	10	-	10	-	ns	
$\overline{WE}$ Setup Time	tWSR	10	-	10	-	ns	
$\overline{WE}$ Hold Time	tWHR	15	-	15	-	ns	
Refresh Time	tREF	-	32	-	32	ms	

HYPER PAGE MODE

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tHPC	25	-	30	-	ns	
$\overline{RAS}$ Pulse Width	tRASP	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	tHCAS	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	tCP	10	-	10	-	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	tCPWD	52	-	59	-	ns	17
Read Modify Write Cycle Time	tHPRWC	66	-	75	-	ns	
Data Output Hold Time	tDHC	5	-	5	-	ns	
$\overline{OE}$ to CAS Hold Time	tOCH	5	-	5	-	ns	18
$\overline{OE}$ Precharge Time	tOEP	5	-	5	-	ns	
$\overline{CAS}$ Hold Time to $\overline{OE}$	tCHO	5	-	5	-	ns	18
Output Buffer Turn-off Delay from $\overline{WE}$	tWEZ	0	13	0	15	ns	12, 18
$\overline{WE}$ Pulse Width	tWPZ	10	-	10	-	ns	18
Output Buffer Turn-off Delay from $\overline{RAS}$	tOFR	0	13	0	15	ns	12, 18
Output Buffer Turn-off Delay from $\overline{CAS}$	tOFC	0	13	0	15	ns	12, 18

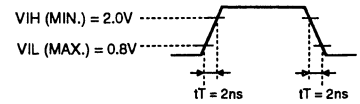
Notes:

1. All voltages are referenced to GND.
2. After power up, wait more than 100 µs and then, execute eight CAS before RAS or RAS only refresh cycles as dummy cycles to initialize internal circuit.
3. ICC1, ICC3, ICC4 and ICC5 depend on cycle rates (tRC and tHPC).
4. Specified values are obtained with outputs unloaded.
5. ICC3 is measured assuming that all column address inputs are held at either high or low.
6. ICC4 is measured assuming that all column address inputs are switched only once during each Hyper page cycle.
7. ICC1 and ICC3 are measured assuming that address can be changed once or less during RAS≤VIL(MAX.) and CAS≧VIH(MIN.).
8. AC measurements assume tT =2ns.

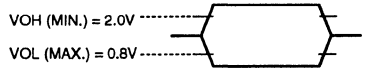
Notes:

9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
tRAD ≦ tRAD(MAX.) and tRCD ≦ tRCD(MAX.)	tRAC(MAX.)	tRAC(MAX.)
tRAD > tRAD(MAX.) and tRCD ≦ tRCD(MAX.)	tAA(MAX.)	tRAD + tAA(MAX.)
tRCD > tRCD(MAX.)	tCAC(MAX.)	tRCD + tCAC(MAX.)

tRAD(MAX.) and tRCD(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (tRAC, tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions tRAD≧tRAD(MAX.) and tRCD≧tRCD(MAX.) will not cause any operation problems.

11. Loading conditions are 1 TTLs and 100 pF.
12. tOFC (MAX.), tOFR(MAX.), tWEZ (MAX.) and tOEZ(MAX.) defines the time when the output achieves the condition of Hi-Z and are not referenced to VOH or VOL.
13. tCRP(MIN.) requirement is applied to $\overline{RAS}$ / $\overline{CAS}$ cycles preceded by any cycles.
14. Either tRCH(MIN.) or tRRH(MIN.) should be met in read cycles.
15. tWP(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, tWCH (MIN.) should be met.
16. tDS(MIN.) and tDH(MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If tWCS≧tWCS (MIN.) , the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If tRWD≧tRWD (MIN.) , tCWD≧tCWD(MIN.) , tAWD≧tAWD(MIN.) and tCPWD≧tCPWD(MIN.) , the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

18. To make I/O to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

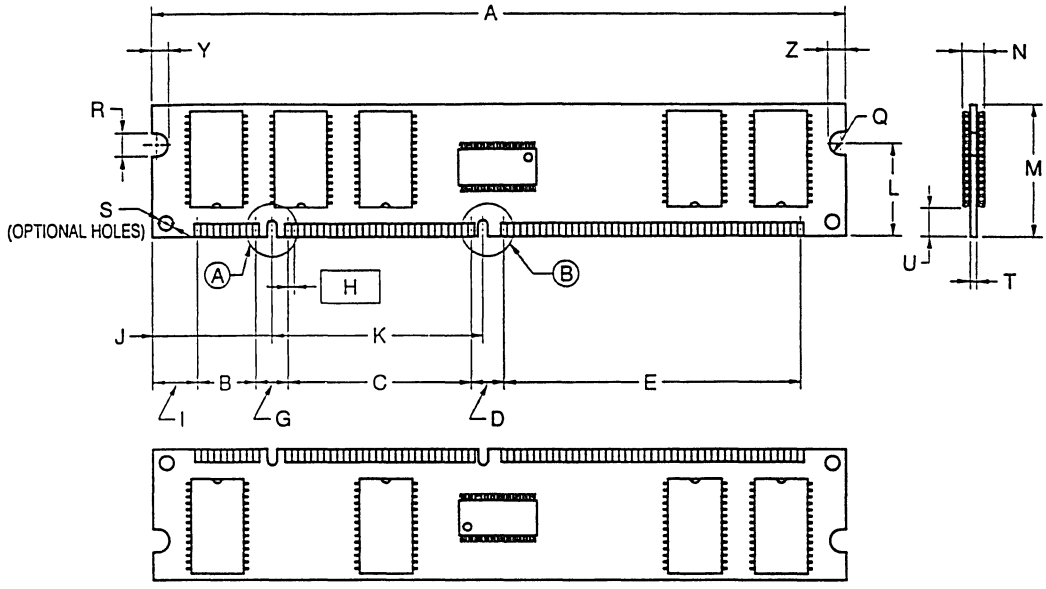
(1) $\overline{RAS}$, $\overline{CAS}$: inactive (at the end of read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
tOFC is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
tOFR is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

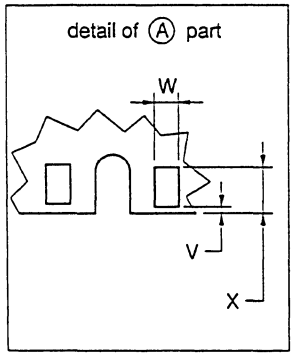
(2) Both RAS and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$: active, $\overline{OE}$: active...tWEZ, tWPZ are effective.
$\overline{WE}$: inactive, $\overline{OE}$: inactive...tOEZ is effective.

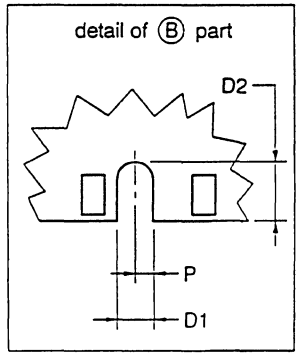
Timing Chart

Please refer to Timing Chart 10, page 473.

Package Drawing







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.123
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.50	0.925
K	43.18	1.70
L	17.78	0.700
M	25.4±0.13	1.000±0.006
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A8

MC-424000FC72F

4M -WORD BY 72-BIT DYNAMIC RAM MODULE

HYPER PAGE MODE (ECC)

Description

The MC-424000FC72F is a 4 194 304 words by 72 bits dynamic RAM module on which 18 pieces of 16M DRAM (μPD 4216405) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 4 194 304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC- 424000FC72-60	60 ns	104 ns	25 ns	8.82w	106mw (CMOS level)
MC- 421000FC72-70	70 ns	124 ns	30 ns	7.88w	

- 4 096 refresh cycles/64 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh , $\overline{RAS}$ only refresh , Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +5.5 V±0.25V power supply

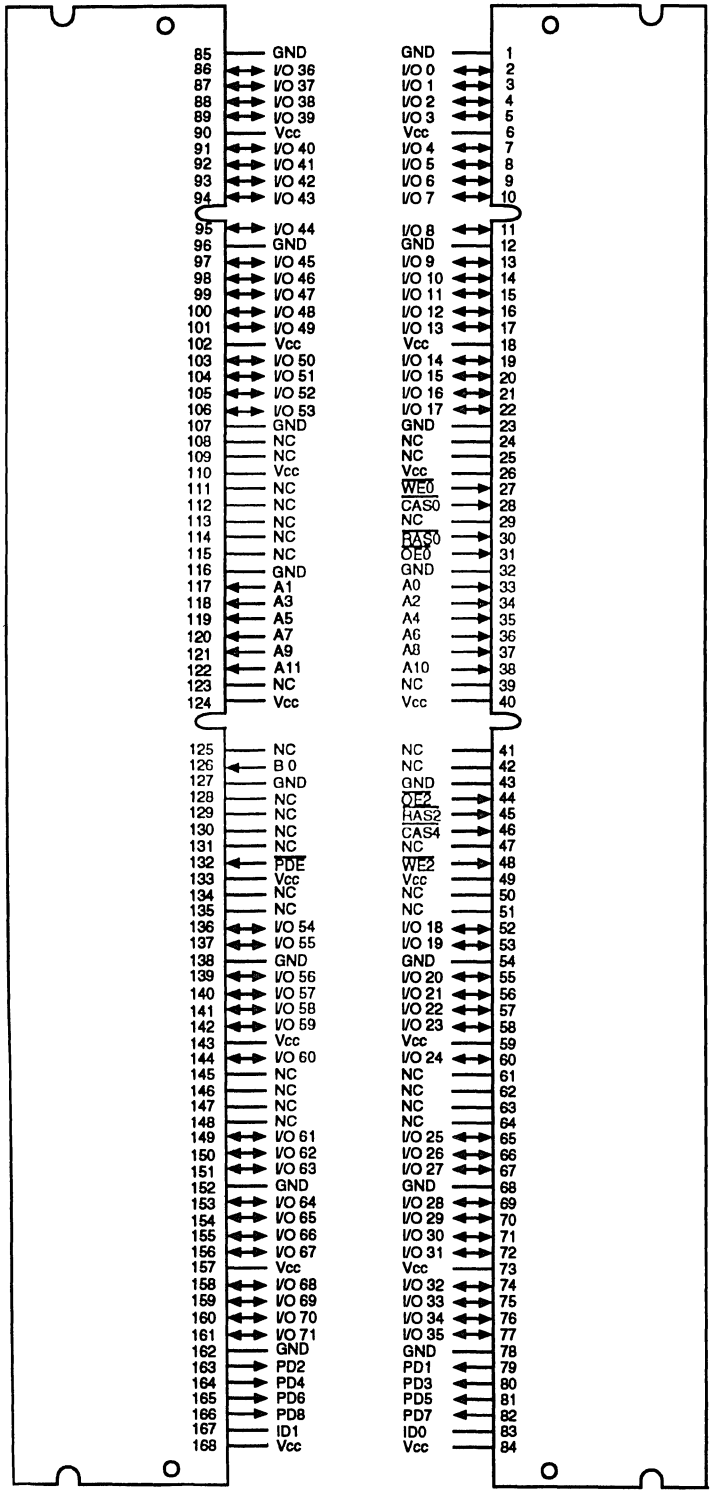
Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 424000FC72F-60	60ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of uPD 4216405G3 (300mil TSOP) [Double side]
MC- 424000FC72F-70	70ns		

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



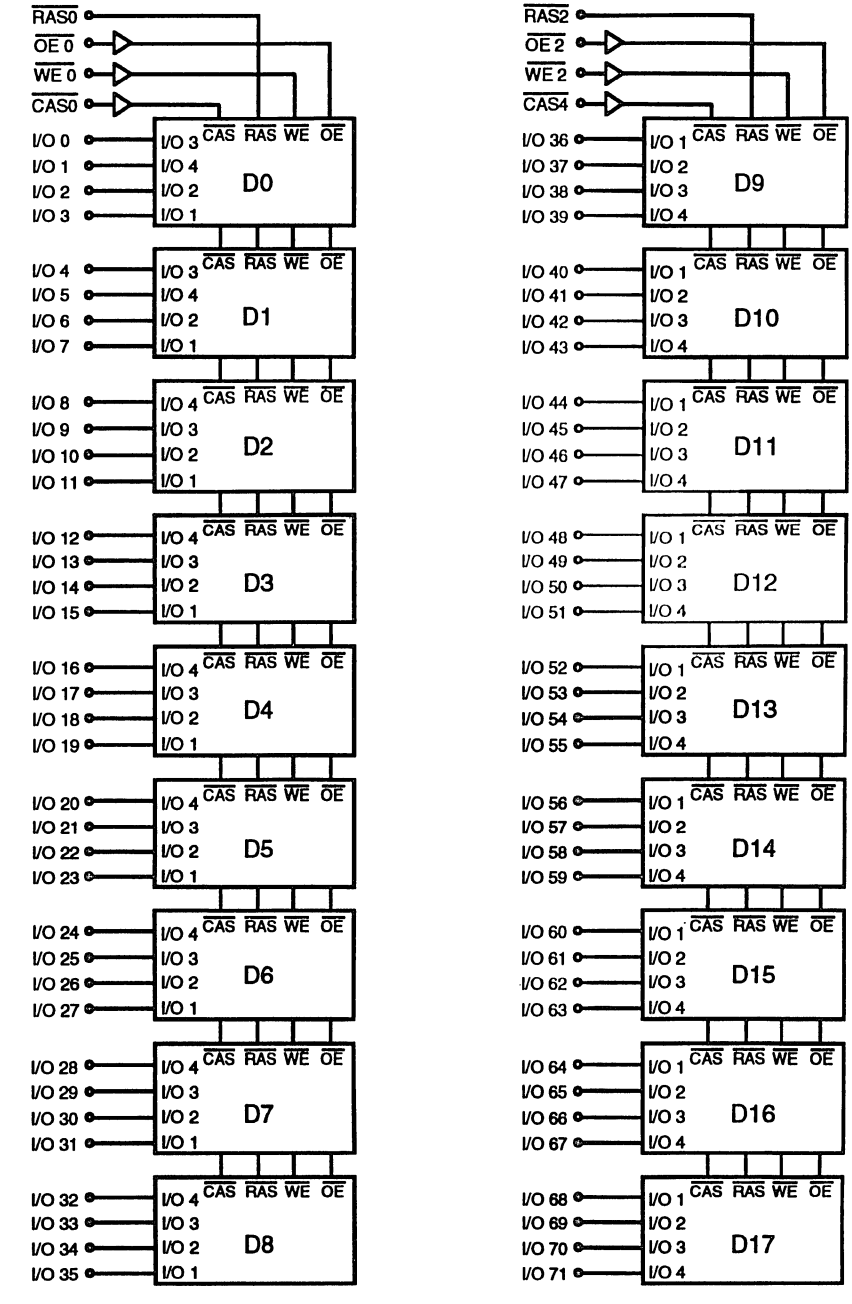
PD and ID Table

Pin Name	Pin No.	Accsess Time	
		60ns	70ns
PD1	79	H	H
PD2	163	H	H
PD3	80	L	L
PD4	164	H	H
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	L	L
ID0	83	GND	GND
ID1	167	GND	GND

Note) H : VOH, L : VOL

A0 - A11, B0 : Address Inputs
I/O 0-I/O 71 : Data Inputs / Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1- PD8 : Presence Detect Pins
ID0, ID1 : Identity pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-1.0to +7.0	V
Supply voltage	VCC		-1.0to +7.0	V
Output current	IO		50	mA
Power dissipation	PD		20	W
Operating temperature	Topt		0 to +70	℃
Storage temperature	Tstg		-55 to +125	℃

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device in not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES : 1, 2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		4.75	5.0	5.25	V
High level input voltage	VIH		2.4		Vcc + 1.0	V
Low level input voltage	VIL		-1.0		+0.8	V
Ambient temperature	Ta		0		70	℃

CAPACITANCE (Ta=25℃, f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI1	A0 - A10, B0			20	pF
	CI2	$\overline{WE0}$, $\overline{WE2}$			20	pF
	CI3	$\overline{RAS0}$, $\overline{RAS2}$			78	pF
	CI4	$\overline{CAS0}$, $\overline{CAS4}$			20	pF
	CI5	$\overline{OE0}$, $\overline{OE2}$			20	pF
Data Input/ Output capacitance	CI/O	I/O 0 - I/O 71			20	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
Operating Current	Icc1	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}=t_{RC\,(MIN.)}$, IO=0mA	t_{RAC}=60ns		1 680	mA	3, 4, 7
			t_{RAC}=70ns		1 500		
Standby Current	Icc2	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH\,(MIN.)}$			100	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ Vcc-0.2V			82		
$\overline{RAS}$ only refresh current	Icc3	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≧ V_{IH} $t_{RC}=t_{RC\,(MIN.)}$, IO=0mA	t_{RAC}=60ns		1 680	mA	3, 4, 5, 7
			t_{RAC}=70ns		1 500		
Operating Current (Hyper Page Mode)	Icc4	$\overline{RAS}$ ≦ VIL, $\overline{CAS}$ Cycling tHPC=tHPC (MIN.), IO=0mA	t_{RAC}=60ns		1 680	mA	3, 4, 6
			t_{RAC}=70ns		1 500		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	Icc5	$t_{RC}=t_{RC\,(MIN.)}$ IO=0mA	t_{RAC}=60ns		1 680	mA	3, 4
			t_{RAC}=70ns		1 500		
Input Leakage Current	$I_{I(L)}$	VI=0 to 5.25V all other pins not under test = 0V	$\overline{RAS}$	-10	+10	µA	
			others	-5	+1		
Output Leakage Current	$I_{O(L)}$	Outputs are disabled (Hi - Z) VO=0 to 5.25V		-10	+10	µA	
High level output voltage	V_{OH}	IO=-5.0mA		2.4		V	
Low level output voltage	V_{OL}	IO=+4.2mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Notes 8,9

(1/2)

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	tRC	104	-	124	-	ns	
Read Modify Write Cycle Time	tRWC	133	-	157	-	ns	
Access Time from $\overline{RAS}$	tRAC	-	60	-	70	ns	10,11
Access Time from $\overline{CAS}$	tCAC	-	20	-	23	ns	10,11
Access Time from Column Address	tAA	-	35	-	40	ns	10,11
Access Time from $\overline{CAS}$ Precharge	tACP	-	40	-	45	ns	11
Access Time from $\overline{OE}$	tOEA	-	20	-	23	ns	11
$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	10
$\overline{CAS}$ to Data Setup Time	tCLZ	0	-	0	-	ns	11
$\overline{OE}$ to Data Setup Time	tOLZ	0	-	0	-	ns	11
$\overline{OE}$ to Data Delay Time	tOED	13	-	15	-	ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	tOEZ	0	13	0	15	ns	12
$\overline{OE}$ Hold Time	tOEH	0	-	0	-	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	-	0	-	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
$\overline{RAS}$ Precharge Time	tRP	40	-	50	-	ns	
$\overline{RAS}$ Pulse Width	tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	-	12	-	ns	
$\overline{CAS}$ Pulse Width	tCAS	10	10,000	12	10,000	ns	
$\overline{CAS}$ Hold Time	tCSH	40	-	50	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	52	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	-	5	-	ns	13
$\overline{CAS}$ Precharge Time	tCPN	10	-	10	-	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	tRPC	5	-	5	-	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	tRHCP	40	-	45	-	ns	
Row Address Setup Time	tASR	5	-	5	-	ns	
Row Address Hold Time	tRAH	10	-	10	-	ns	
Column Address Setup Time	tASC	0	-	0	-	ns	
Column Address Hold Time	tCAH	10	-	12	-	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	tRAL	30	-	35	-	ns	
Read Command Setup Time	tRCS	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0	-	0	-	ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0	-	0	-	ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	tWCH	10	-	10	-	ns	15
$\overline{WE}$ Pulse Width	tWP	10	-	10	-	ns	15
Data-in Setup Time	tDS	0	-	0	-	ns	16
Data-in Hold Time	tDH	10	-	10	-	ns	16
Write command Setup Time	tWCS	0	-	0	-	ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	tCWD	32	-	37	-	ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	tRWD	87	-	99	-	ns	17
Column Address to $\overline{WE}$ Delay Time	tAWD	52	-	59	-	ns	17

(2/2)

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	tRWL	15	-	17	-	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	tCWL	10	-	12	-	ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCSR	5	-	5	-	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCHR	10	-	10	-	ns	
$\overline{WE}$ Setup Time	tWSR	10	-	10	-	ns	
$\overline{WE}$ Hold Time	tWHR	15	-	15	-	ns	
Refresh Time	tREF	-	64	-	64	ms	

HYPER PAGE MODE

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tHPC	25	-	30	-	ns	
$\overline{RAS}$ Pulse Width	tRASP	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	tHCAS	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	tCP	10	-	10	-	ns	
$\overline{CAS}$ Precharge to WE Delay Time	tCPWD	52	-	59	-	ns	17
Read Modify Write Cycle Time	tHPRWC	66	-	75	-	ns	
Data Output Hold Time	tDHC	5	-	5	-	ns	
$\overline{OE}$ to CAS Hold Time	tOCH	5	-	5	-	ns	18
$\overline{OE}$ Precharge Time	tOEP	5	-	5	-	ns	
$\overline{CAS}$ Hold Time to $\overline{OE}$	tCHO	5	-	5	-	ns	18
Output Buffer Turn-off Delay from $\overline{WE}$	tWEZ	0	13	0	15	ns	12, 18
$\overline{WE}$ Pulse Width	tWPZ	10	-	10	-	ns	18
Output Buffer Turn-off Delay from $\overline{RAS}$	tOFR	0	13	0	15	ns	12, 18
Output Buffer Turn-off Delay from $\overline{CAS}$	tOFC	0	13	0	15	ns	12, 18

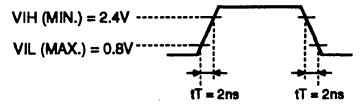
Notes:

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight CAS before RAS or RAS only refresh cycles as dummy cycles to initialize internal circuit.
3. ICC1, ICC3, ICC4 and ICC5 depend on cycle rates (tRC and tHPC).
4. Specified values are obtained with outputs unloaded.
5. ICC3 is measured assuming that all column address inputs are held at either high or low.
6. ICC4 is measured assuming that all column address inputs are switched only once during each Hyper page cycle.
7. ICC1 and ICC3 are measured assuming that address can be changed once or less during RAS≦VIL(MAX.) and CAS≧VIH(MIN.).
8. AC measurements assume tT =2ns.

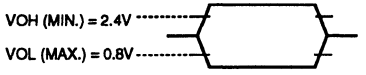
Notes:

9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
tRAD ≦ tRAD(MAX.) and tRCD ≦ tRCD(MAX.)	tRAC(MAX.)	tRAC(MAX.)
tRAD > tRAD(MAX.) and tRCD ≦ tRCD(MAX.)	tAA(MAX.)	tRAD + tAA(MAX.)
tRCD > tRCD(MAX.)	tCAC(MAX.)	tRCD + tCAC(MAX.)

tRAD(MAX.) and tRCD(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (tRAC, tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions tRAD≧tRAD(MAX.) and tRCD≧tRCD(MAX.) will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. tOFC (MAX.), tOFR(MAX.), tWEZ (MAX.) and tOEZ(MAX.) defines the time when the output achieves the condition of Hi-Z and are not referenced to VOH or VOL.
13. tCRP(MIN.) requirement is applied to $\overline{RAS}$ / $\overline{CAS}$ cycles preceded by any cycles.
14. Either tRCH(MIN.) or tRRH(MIN.) should be met in read cycles.
15. tWP(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, tWCH (MIN.) should be met.
16. tDS(MIN.) and tDH(MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If tWCS≧tWCS (MIN.), the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If tRWD≧tRWD (MIN.), tCWD≧tCWD(MIN.), tAWD≧tAWD(MIN.) and tCPWD≧tCPWD(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
18. To make I/O to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) $\overline{RAS}$, $\overline{CAS}$: inactive (at the end of read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
tOFC is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
tOFR is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

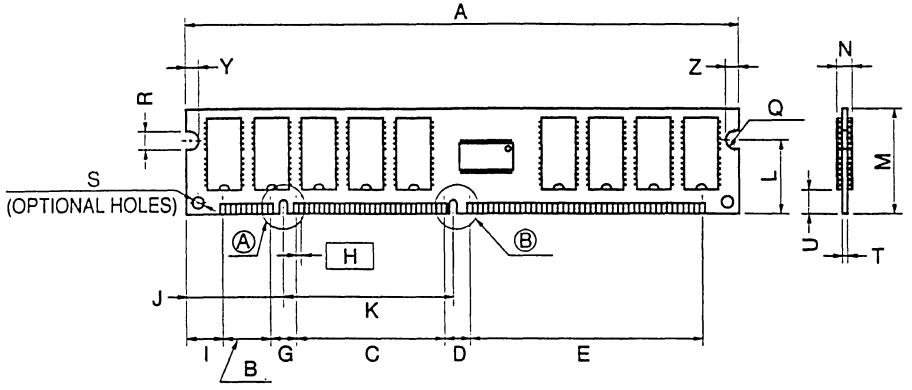
(2) Both RAS and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$: active, $\overline{OE}$: active...tWEZ, tWPZ are effective.
$\overline{WE}$: inactive, $\overline{OE}$: inactive...tOEZ is effective.

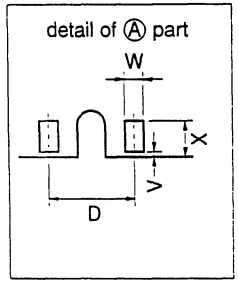
Timing Chart

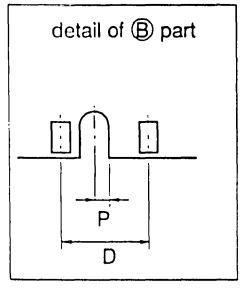
Please refer to Timing Chart 10, page 473.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE) OUTLINE DRAWINGS







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A2

MC-424000LFC72F

3.3 V OPERATION 4M -WORD BY 72-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (ECC)

Description

The MC-424000LFC72F is a 4 194 304 words by 72 bits dynamic RAM module on which 18 pieces of 16M DRAM (μPD 4216405L) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 4 194 304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC- 424000LFC72-A60	60 ns	104 ns	25 ns	5.87 w	180 mw (CMOS level)
MC- 424000LFC72-A70	70 ns	124 ns	30 ns	5.22 w	

- 4 096 refresh cycles/64 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh , $\overline{\text{RAS}}$ only refresh , Hidden refresh.
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +3.3 V$\pm$0.3V power supply

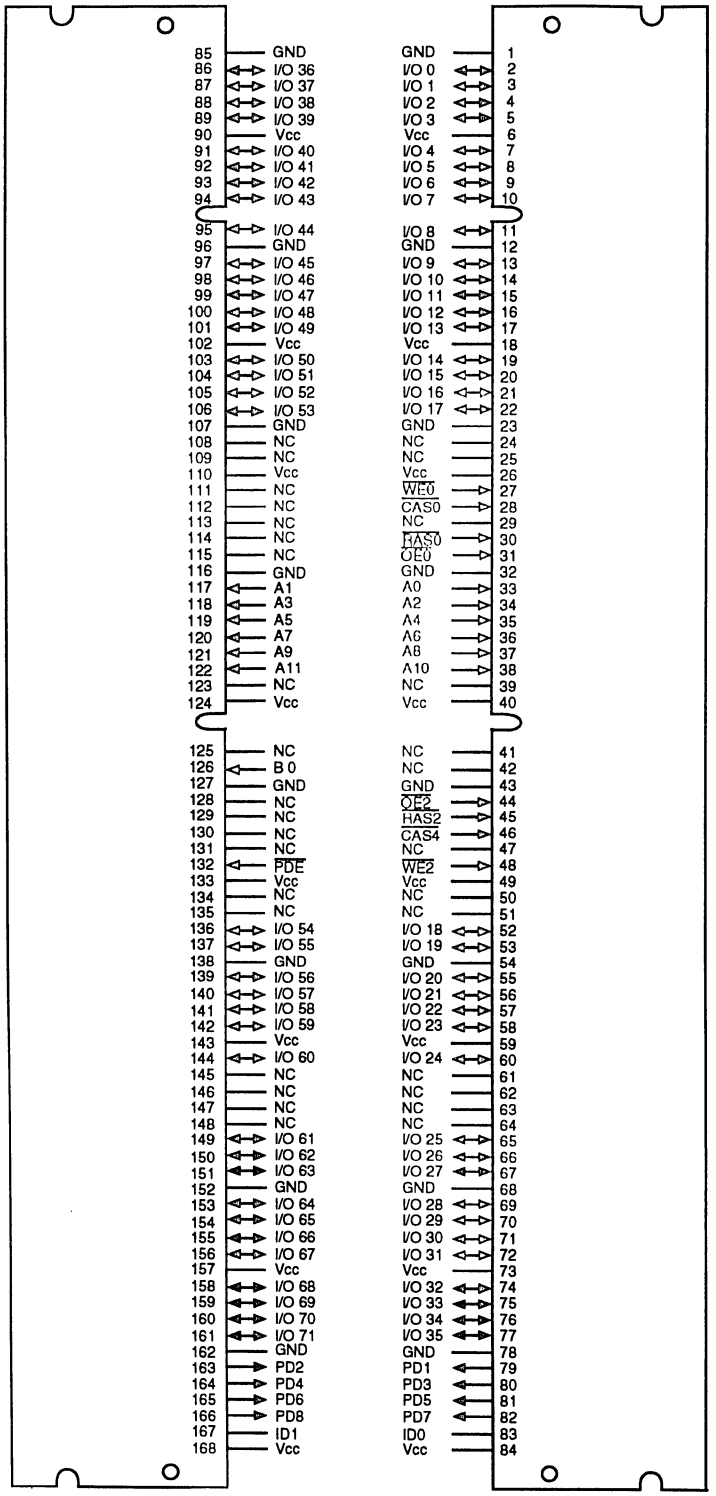
Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 424000LFC72F-A60	60ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of uPD 4216405LG3 (300mil TSOP) [Double side]
MC- 424000LFC72F-A70	70ns		

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



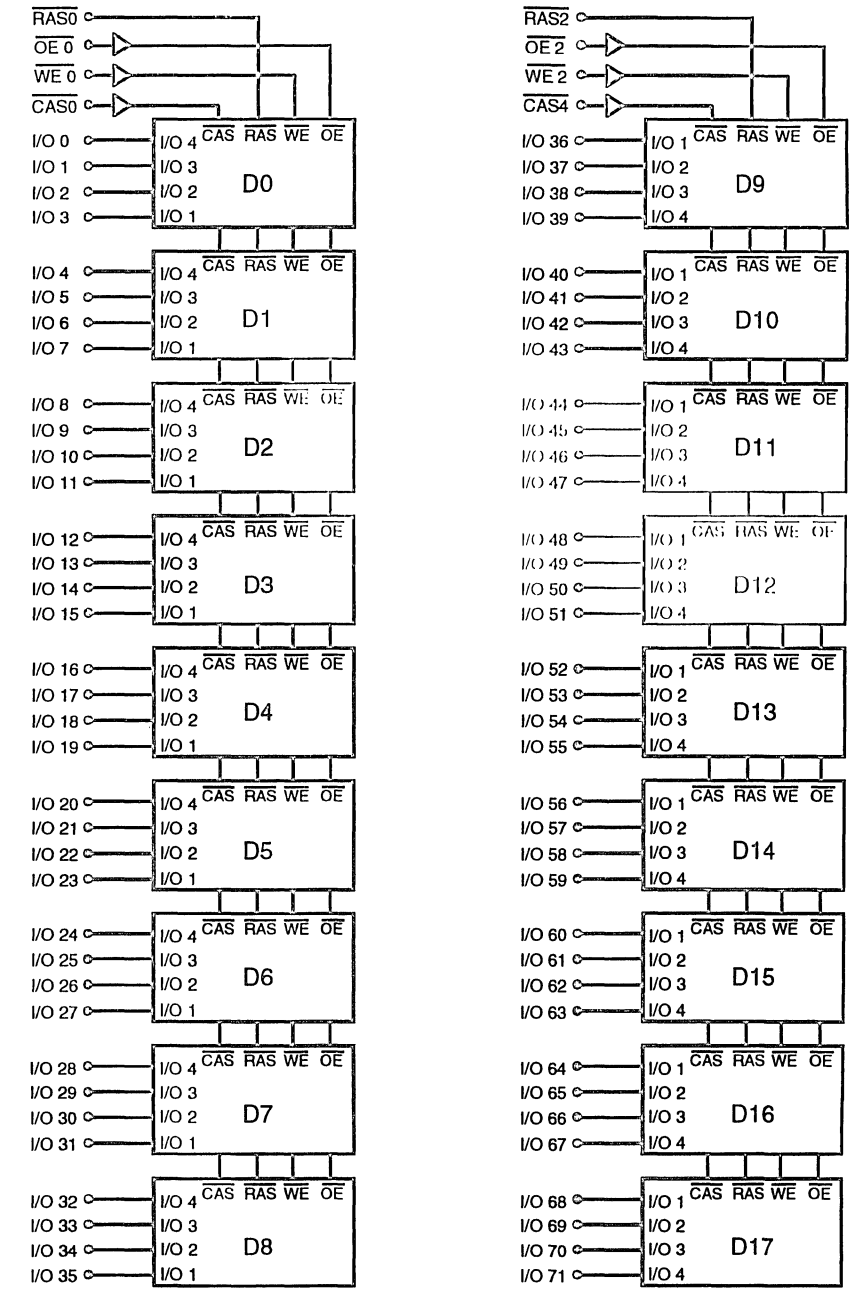
PD and ID Table

Pin Name	Pin No.	Accsess Time	
		60ns	70ns
PD1	79	H	H
PD2	163	H	H
PD3	80	L	L
PD4	164	H	H
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	L	L
ID0	83	GND	GND
ID1	167	GND	GND

Note) H : VOH, L : VOL

A0 - A11, B0 : Address Inputs
I/O 0-I/O 71 : Data Inputs / Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1- PD8 : Presence Detect Pins
ID0, ID1 : Identity pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-0.5 to +4.6	V
Supply voltage	VCC		-0.5 to +4.6	V
Output current	IO		20	mA
Power dissipation	PD		20	W
Operating temperature	Topt		0 to +70	℃
Storage temperature	Tstg		-55 to +125	℃

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device in not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES : 1 , 2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		3.0	3.3	3.6	V
High level input voltage	VIH		2.0		Vcc + 0.3	V
Low level input voltage	VIL		-0.3		+0.8	V
Ambient temperature	Ta		0		70	℃

CAPACITANCE (Ta=25℃ , f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI1	A0 - A11, B0			20	pF
	CI2	$\overline{WE0}$, $\overline{WE2}$			20	pF
	CI3	$\overline{RAS0}$, $\overline{RAS2}$			78	pF
	CI4	$\overline{CAS0}$, $\overline{CAS4}$			20	pF
	CI5	$\overline{OE0}$, $\overline{OE2}$			20	pF
Data Input/ Output capacitance	CI/O	I/O 0 - I/O 71			20	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
Operating Current	Icc1	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}=t_{RC(MIN.)}$, IO=0mA	t_{RAC}=60ns		1 450	mA	3, 4, 7
			t_{RAC}=70ns		1 270		
Standby Current	Icc2	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH(MIN.)}$			100	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ Vcc-0.2V			50		
$\overline{RAS}$ only refresh current	Icc3	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≧ V_{IH} $t_{RC}=t_{RC(MIN.)}$, IO=0mA	t_{RAC}=60ns		1 450	mA	3, 4, 5, 7
			t_{RAC}=70ns		1 270		
Operating Current (Hyper Page Mode)	Icc4	$\overline{RAS}$ ≦ VIL, $\overline{CAS}$ Cycling tHPC=tHPC (MIN.), IO=0mA	t_{RAC}=60ns		1 630	mA	3, 4, 6
			t_{RAC}=70ns		1 450		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	Icc5	$t_{RC}=t_{RC(MIN.)}$ IO=0mA	t_{RAC}=60ns		1 450	mA	3, 4
			t_{RAC}=70ns		1 270		
Input Leakage Current	$I_{I(L)}$	VI=0 to 3.6V all other pins not under test = 0V	$\overline{RAS}$	-5	+5	µA	
			others	-5	+1		
Output Leakage Current	$I_{O(L)}$	Outputs are disabled (Hi - Z) VO=0 to 3.6V		-5	+5	µA	
High level output voltage	V_{OH}	IO=-2.0mA		2.4		V	
Low level output voltage	V_{OL}	IO=+2.0mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Notes 8,9

(1/2)

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	tRC	104	-	124	-	ns	
Read Modify Write Cycle Time	tRWC	133	-	157	-	ns	
Access Time from $\overline{RAS}$	tRAC	-	60	-	70	ns	10,11
Access Time from $\overline{CAS}$	tCAC	-	20	-	23	ns	10,11
Access Time from Column Address	tAA	-	35	-	40	ns	10,11
Access Time from $\overline{CAS}$ Precharge	tACP	-	40	-	45	ns	11
Access Time from $\overline{OE}$	tOEA	-	20	-	23	ns	11
$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	10
$\overline{CAS}$ to Data Setup Time	tCLZ	0	-	0	-	ns	11
$\overline{OE}$ to Data Setup Time	tOLZ	0	-	0	-	ns	11
$\overline{OE}$ to Data Delay Time	tOED	13	-	15	-	ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	tOEZ	0	13	0	15	ns	12
$\overline{OE}$ Hold Time	tOEH	0	-	0	-	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	-	0	-	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
$\overline{RAS}$ Precharge Time	tRP	40	-	50	-	ns	
$\overline{RAS}$ Pulse Width	tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	-	12	-	ns	
$\overline{CAS}$ Pulse Width	tCAS	10	10,000	12	10,000	ns	
$\overline{CAS}$ Hold Time	tCSH	40	-	50	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	52	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	-	5	-	ns	13
$\overline{CAS}$ Precharge Time	tCPN	10	-	10	-	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	tRPC	5	-	5	-	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	tRHCP	40	-	45	-	ns	
Row Address Setup Time	tASR	5	-	5	-	ns	
Row Address Hold Time	tRAH	10	-	10	-	ns	
Column Address Setup Time	tASC	0	-	0	-	ns	
Column Address Hold Time	tCAH	10	-	12	-	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	tRAL	30	-	35	-	ns	
Read Command Setup Time	tRCS	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0	-	0	-	ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0	-	0	-	ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	tWCH	10	-	10	-	ns	15
$\overline{WE}$ Pulse Width	tWP	10	-	10	-	ns	15
Data-in Setup Time	tDS	0	-	0	-	ns	16
Data-in Hold Time	tDH	10	-	10	-	ns	16
Write command Setup Time	tWCS	0	-	0	-	ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	tCWD	32	-	37	-	ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	tRWD	87	-	99	-	ns	17
Column Address to $\overline{WE}$ Delay Time	tAWD	52	-	59	-	ns	17

(2/2)

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	tRWL	15	-	17	-	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	tCWL	10	-	12	-	ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCSR	5	-	5	-	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCHR	10	-	10	-	ns	
$\overline{WE}$ Setup Time	tWSR	10	-	10	-	ns	
$\overline{WE}$ Hold Time	tWHR	15	-	15	-	ns	
Refresh Time	tREF	-	64	-	64	ms	

HYPER PAGE MODE

PARAMETER	SYMBOL	tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tHPC	25	-	30	-	ns	
$\overline{RAS}$ Pulse Width	tRASP	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	tHCAS	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	tCP	10	-	10	-	ns	
$\overline{CAS}$ Precharge to WE Delay Time	tCPWD	52	-	59	-	ns	17
Read Modify Write Cycle Time	tHPRWC	66	-	75	-	ns	
Data Output Hold Time	tDHC	5	-	5	-	ns	
$\overline{OE}$ to CAS Hold Time	tOCH	5	-	5	-	ns	18
$\overline{OE}$ Precharge Time	tOEP	5	-	5	-	ns	
$\overline{CAS}$ Hold Time to $\overline{OE}$	tCHO	5	-	5	-	ns	18
Output Buffer Turn-off Delay from $\overline{WE}$	tWEZ	0	13	0	15	ns	12, 18
$\overline{WE}$ Pulse Width	tWPZ	10	-	10	-	ns	18
Output Buffer Turn-off Delay from $\overline{RAS}$	tOFR	0	13	0	15	ns	12, 18
Output Buffer Turn-off Delay from $\overline{CAS}$	tOFC	0	13	0	15	ns	12, 18

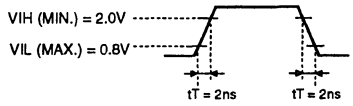
Notes:

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight CAS before RAS or RAS only refresh cycles as dummy cycles to initialize internal circuit.
3. ICC1, ICC3, ICC4 and ICC5 depend on cycle rates (tRC and tHPC).
4. Specified values are obtained with outputs unloaded.
5. ICC3 is measured assuming that all column address inputs are held at either high or low.
6. ICC4 is measured assuming that all column address inputs are switched only once during each Hyper page cycle.
7. ICC1 and ICC3 are measured assuming that address can be changed once or less during RAS≦VIL(MAX.) and CAS≧VIH(MIN.).
8. AC measurements assume tT =2ns.

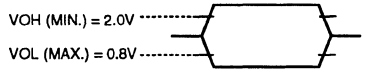
Notes:

9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
tRAD ≦ tRAD(MAX.) and tRCD ≦ tRCD(MAX.)	tRAC(MAX.)	tRAC(MAX.)
tRAD > tRAD(MAX.) and tRCD ≦ tRCD(MAX.)	tAA(MAX.)	tRAD + tAA(MAX.)
tRCD > tRCD(MAX.)	tCAC(MAX.)	tRCD + tCAC(MAX.)

tRAD(MAX.) and tRCD(MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (tRAC, tAA or tCAC) is to be used for finding out when output data will be available. Therefore, the input conditions tRAD≧tRAD(MAX.) and tRCD≧tRCD(MAX.) will not cause any operation problems.

11. Loading conditions are 1 TTLs and 100 pF.
12. tOFC (MAX.), tOFR(MAX.), tWEZ (MAX.) and tOEZ(MAX.) defines the time when the output achieves the condition of Hi-Z and are not referenced to VOH or VOL.
13. tCRP(MIN.) requirement is applied to $\overline{RAS}$ / $\overline{CAS}$ cycles preceded by any cycles.
14. Either tRCH(MIN.) or tRRH(MIN.) should be met in read cycles.
15. tWP(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, tWCH (MIN.) should be met.
16. tDS(MIN.) and tDH(MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If tWCS≧tWCS (MIN.) , the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If tRWD≧tRWD (MIN.) , tCWD≧tCWD(MIN.) , tAWD≧tAWD(MIN.) and tCPWD≧tCPWD(MIN.) , the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
18. To make I/O to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

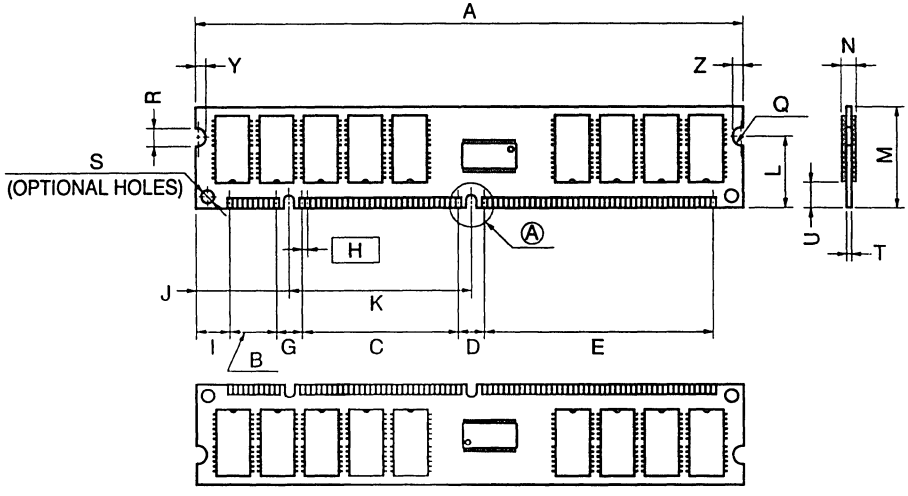
(1) $\overline{RAS}$, $\overline{CAS}$: inactive (at the end of read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
tOFC is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
tOFR is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

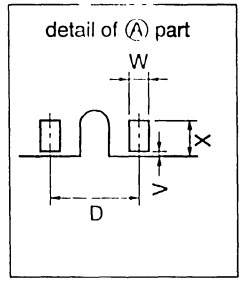
(2) Both RAS and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$: active, $\overline{OE}$: active...tWEZ, tWPZ are effective.
$\overline{WE}$: inactive, $\overline{OE}$: inactive...tOEZ is effective.

Timing Chart

Please refer to Timing Chart 10, page 473.

Package Drawing



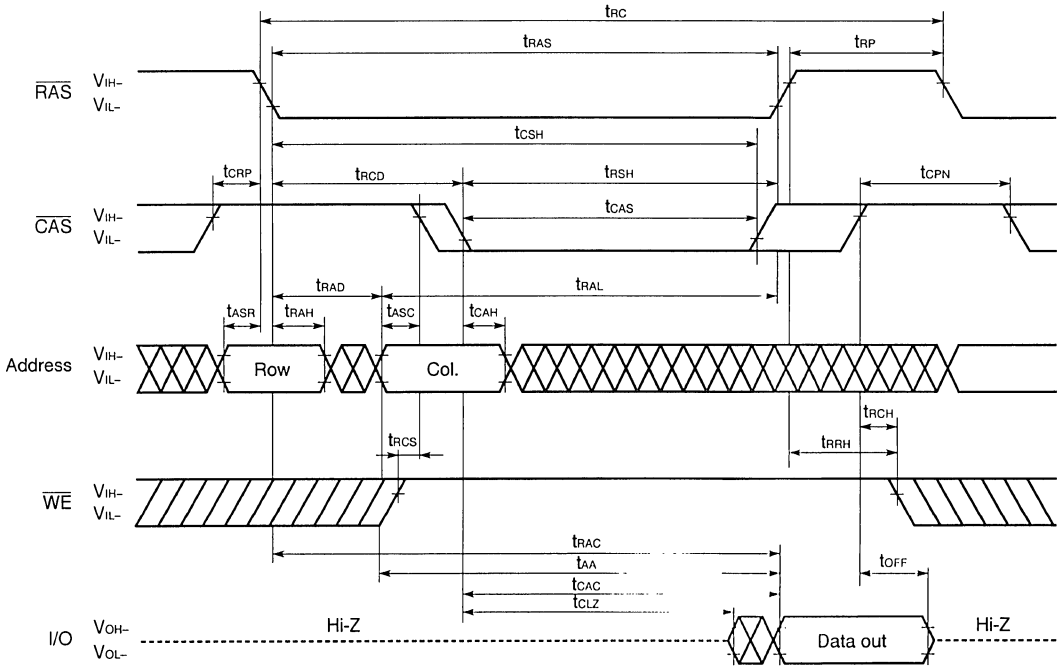


ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	43.18	1.700
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

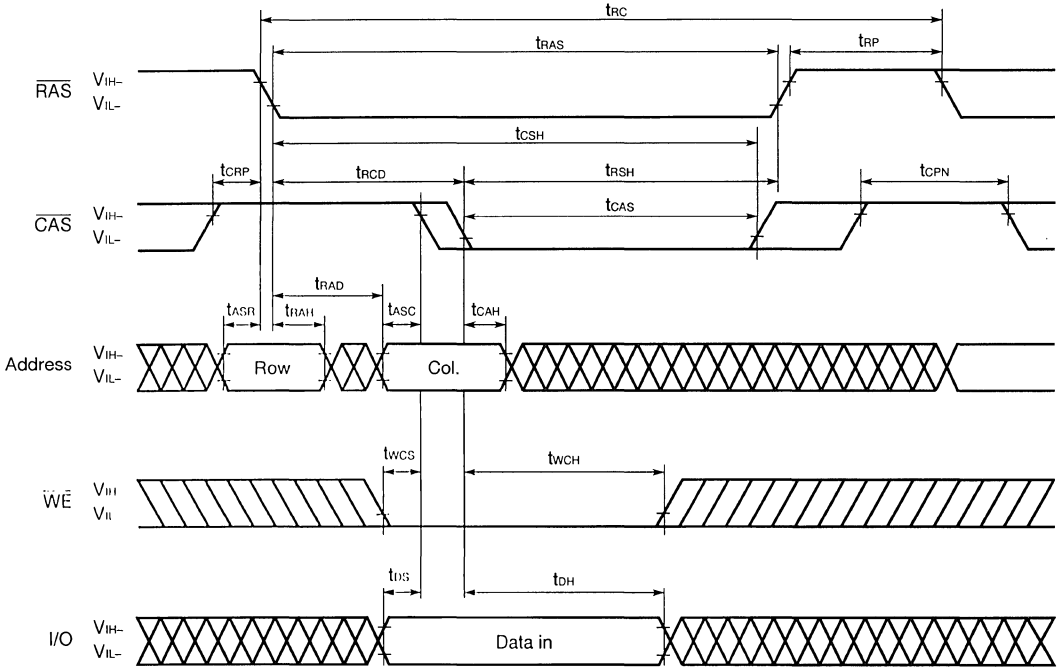
M168S-50A3

Timing Chart 1

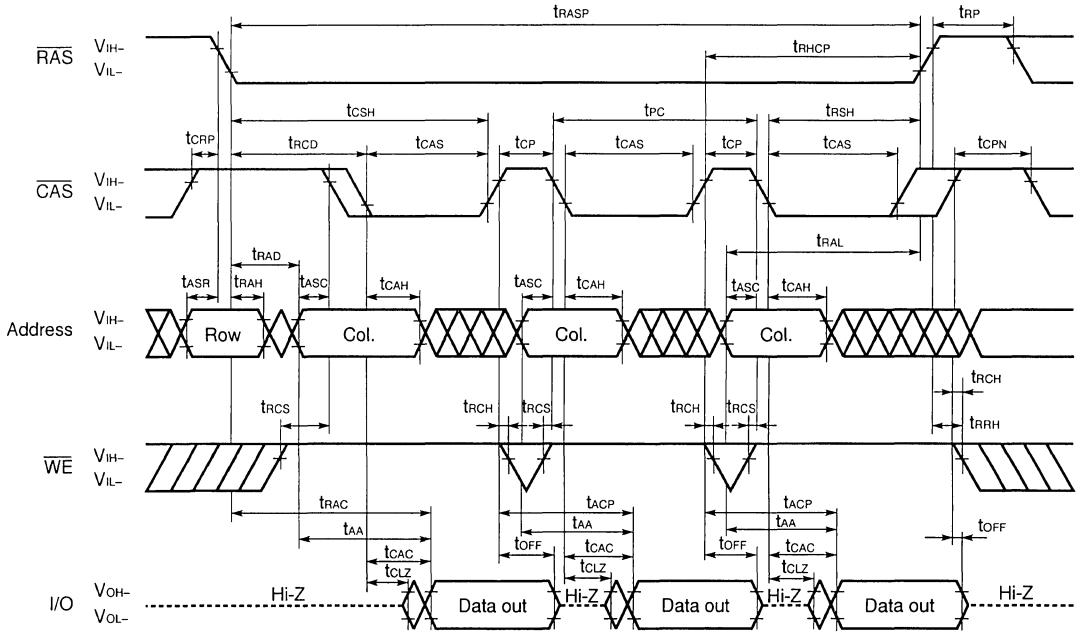
Read Cycle


tRC
tRAS
tRP
RAS
VIH-
VIL-
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
VIH-
VIL-
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
VIH-
VIL-
Row
Col.
tRCH
tRCS
tRRH
WE
VIH-
VIL-
tRAC
tAA
tOFF
tCAC
tCLZ
I/O
VOH-
VOL-
Hi-Z
Data out
Hi-Z

Early Write Cycle

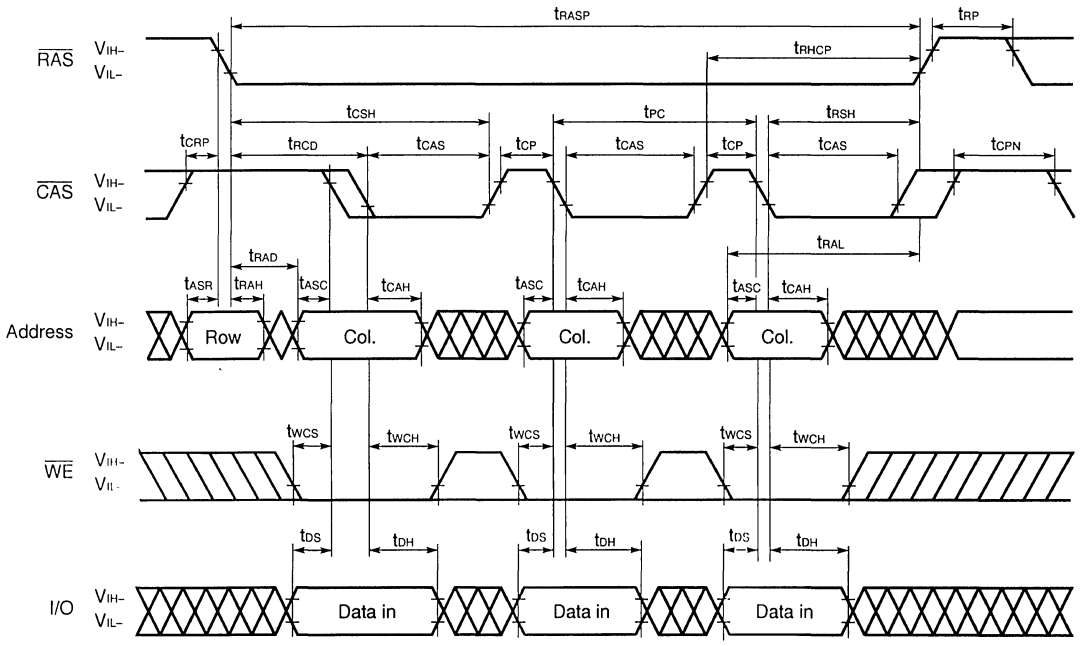


Fast Page Mode Read Cycle



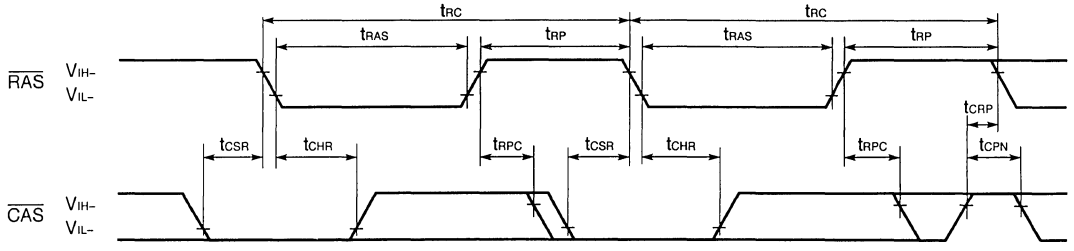
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle



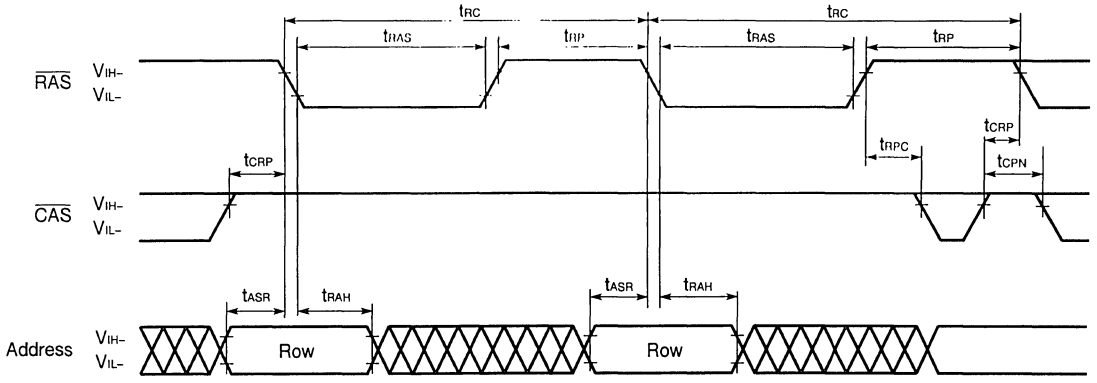
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



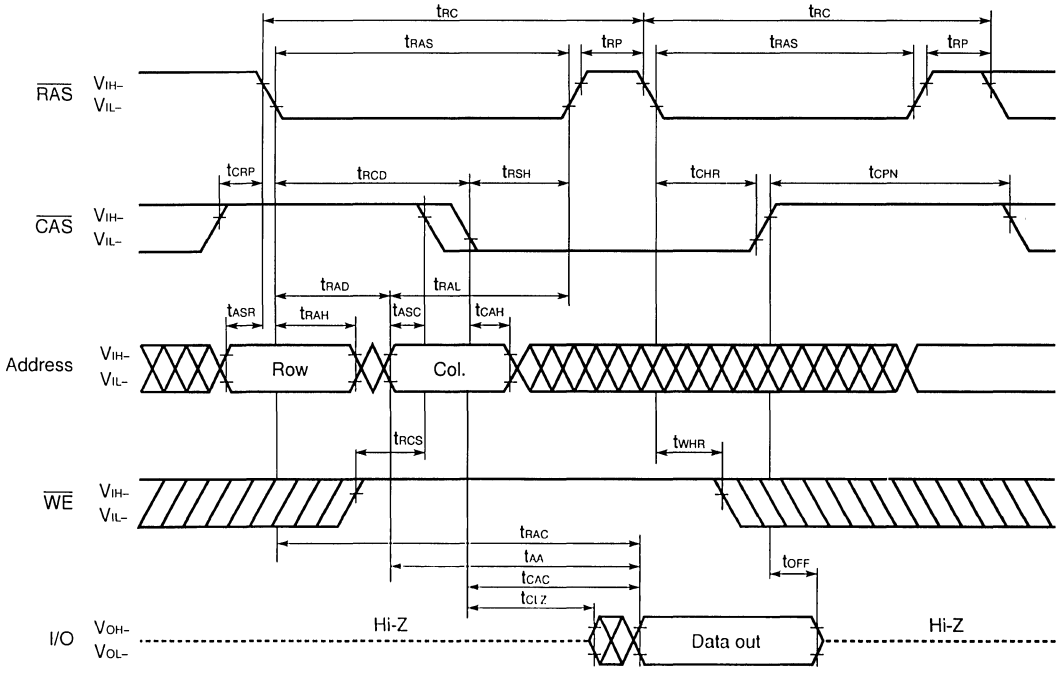
Remark Address, $\overline{WE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

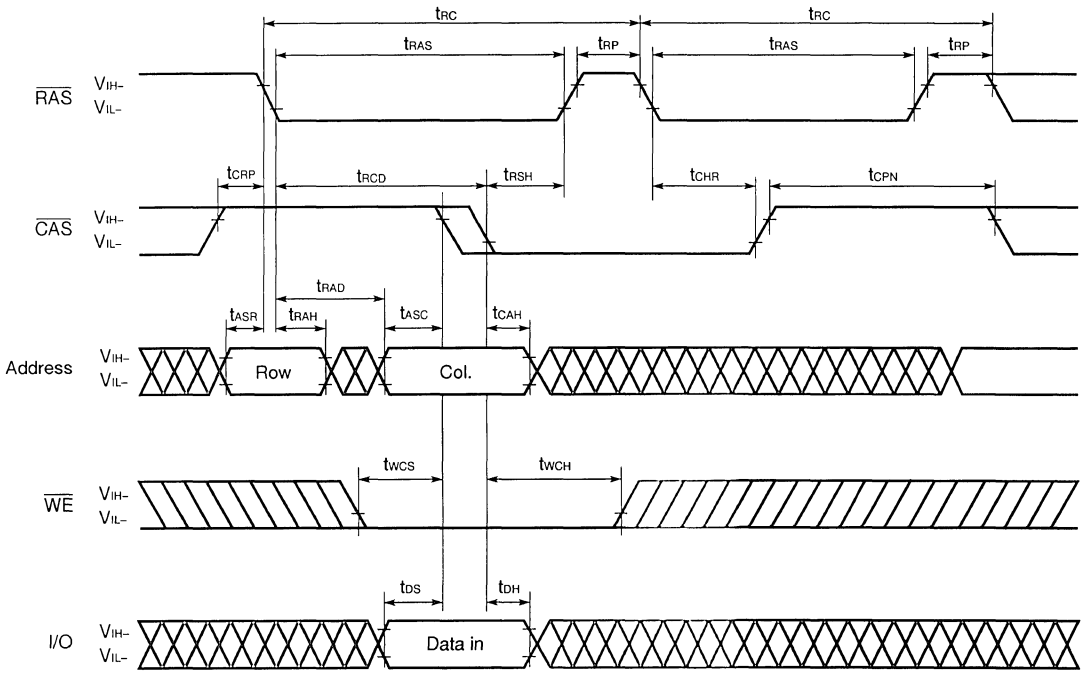


Remark $\overline{WE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

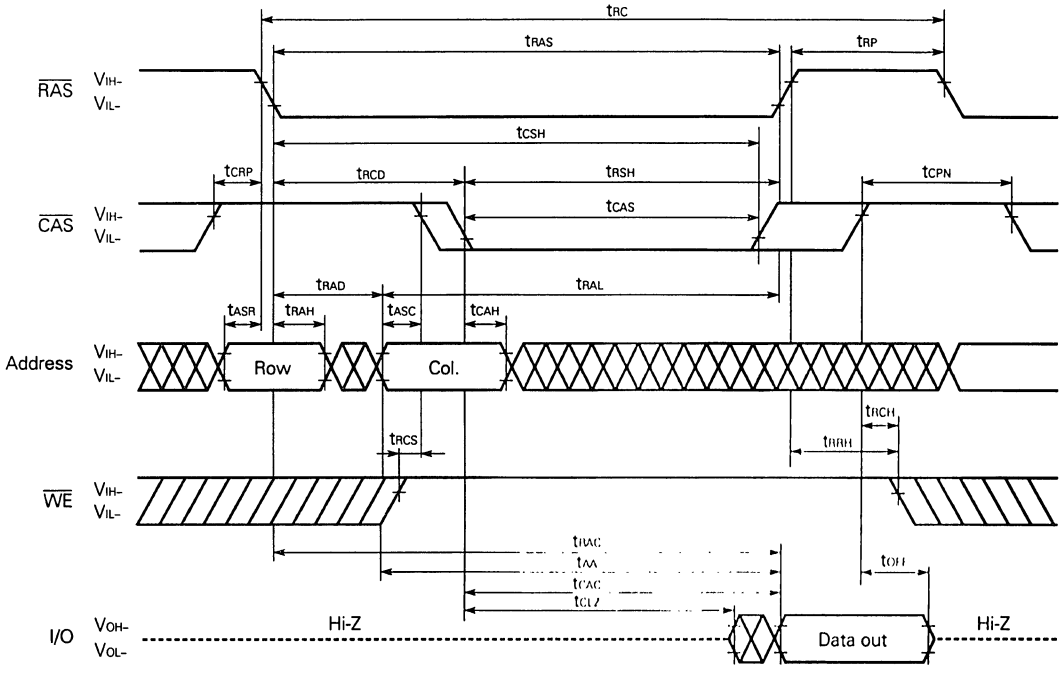


Hidden Refresh Cycle (Write)

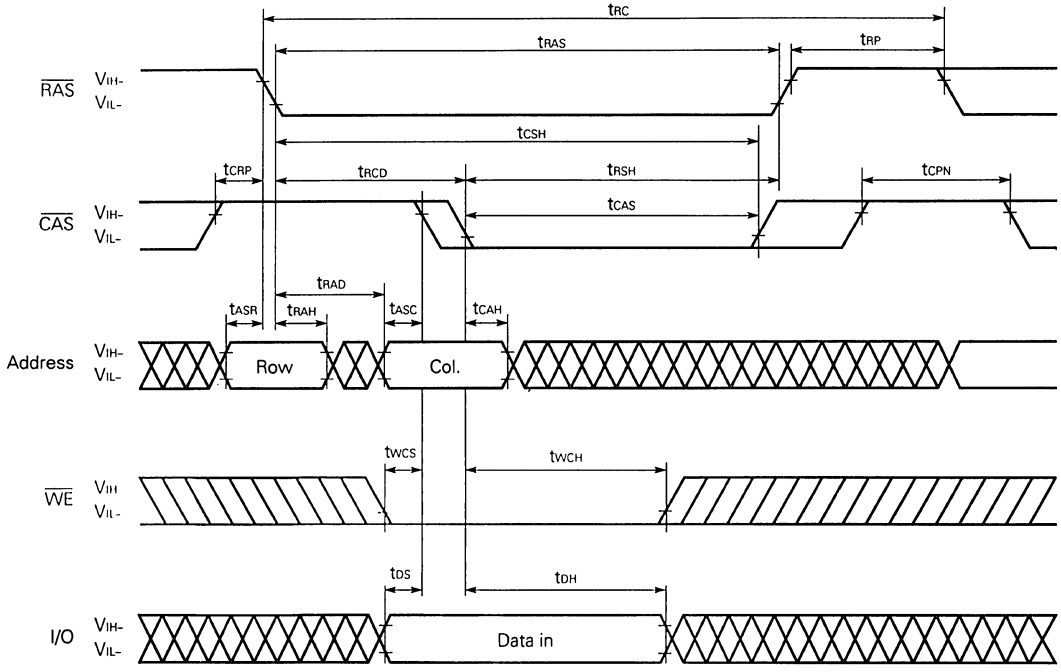


Timing Chart 2

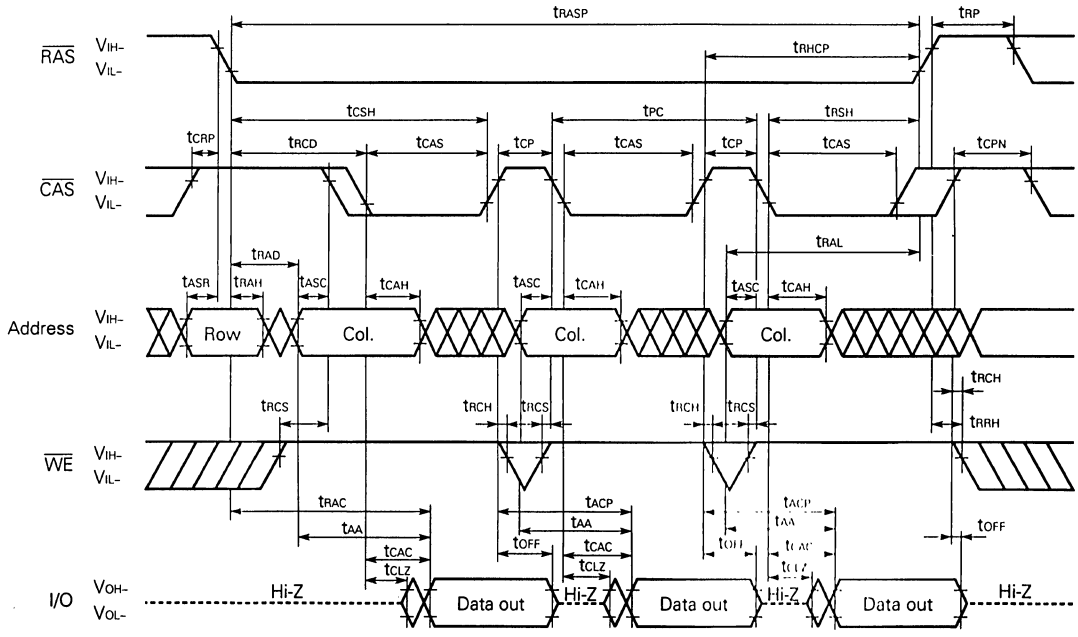
Read Cycle


tRC
tRAS
tRP
RAS
VIH-
VIL-
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
VIH-
VIL-
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
VIH-
VIL-
Row
Col.
tRCH
tRCS
tRRH
WE
VIH-
VIL-
tOFF
I/O
VOH-
VOL-
Hi-Z
Data out
Hi-Z

Early Write Cycle

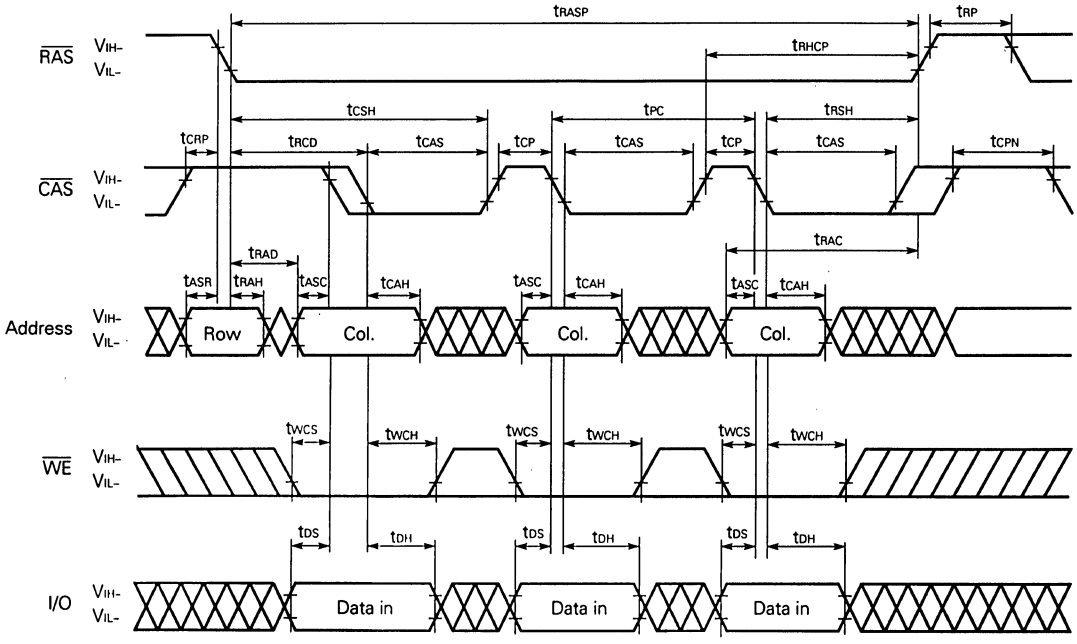


Fast Page Mode Read Cycle



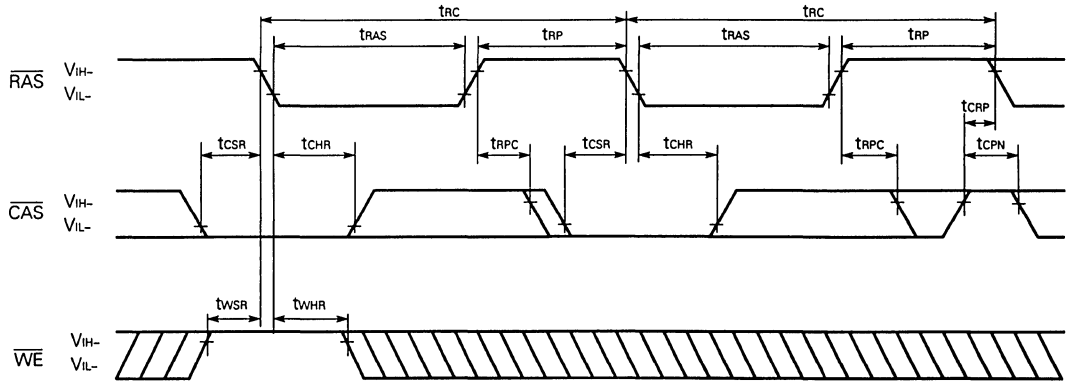
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle



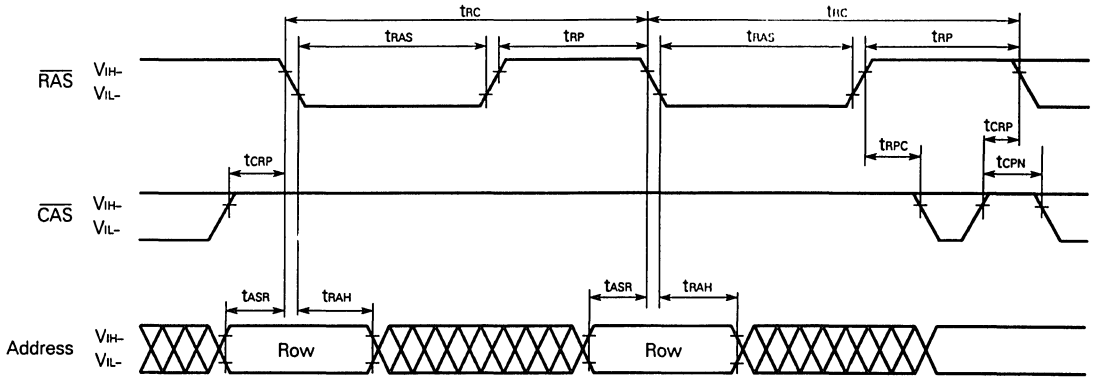
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



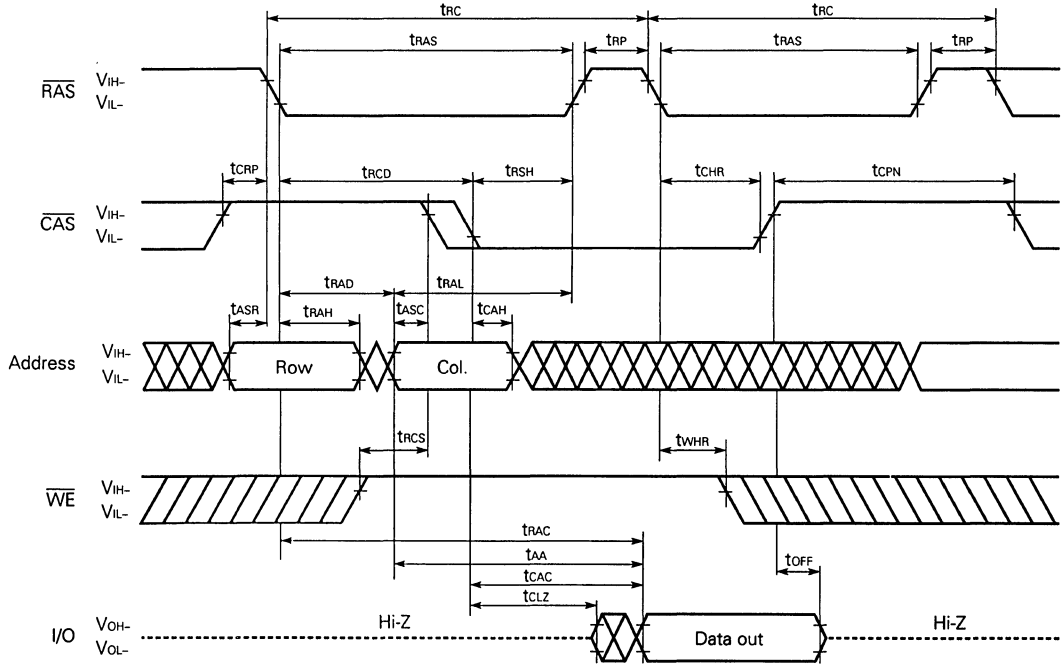
Remark Address: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

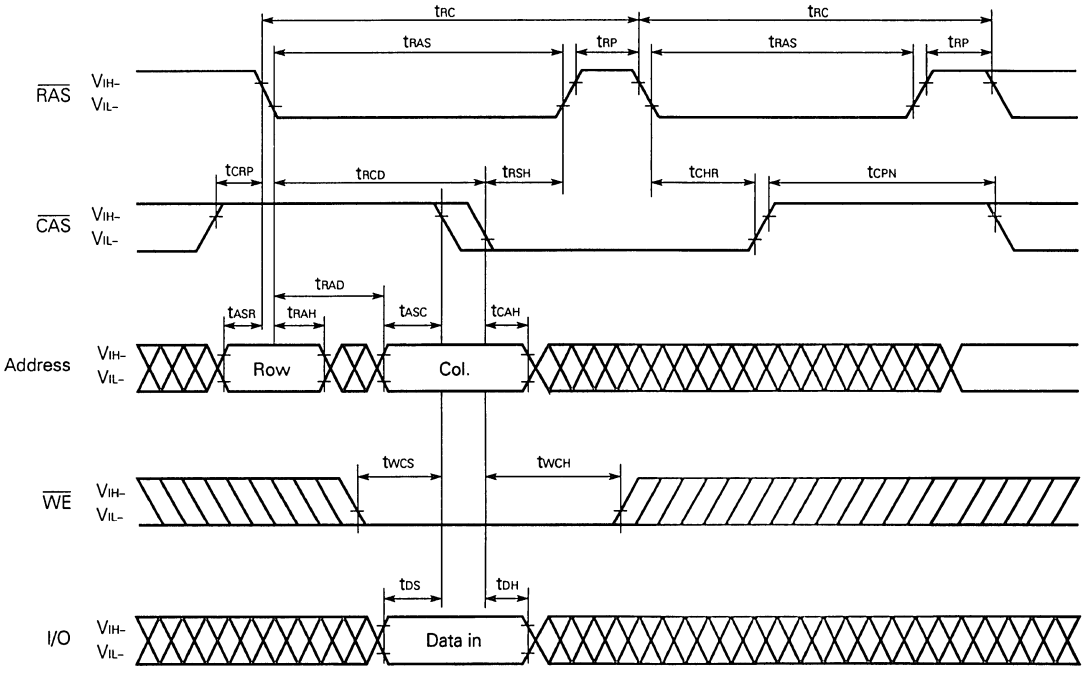


Remark $\overline{WE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

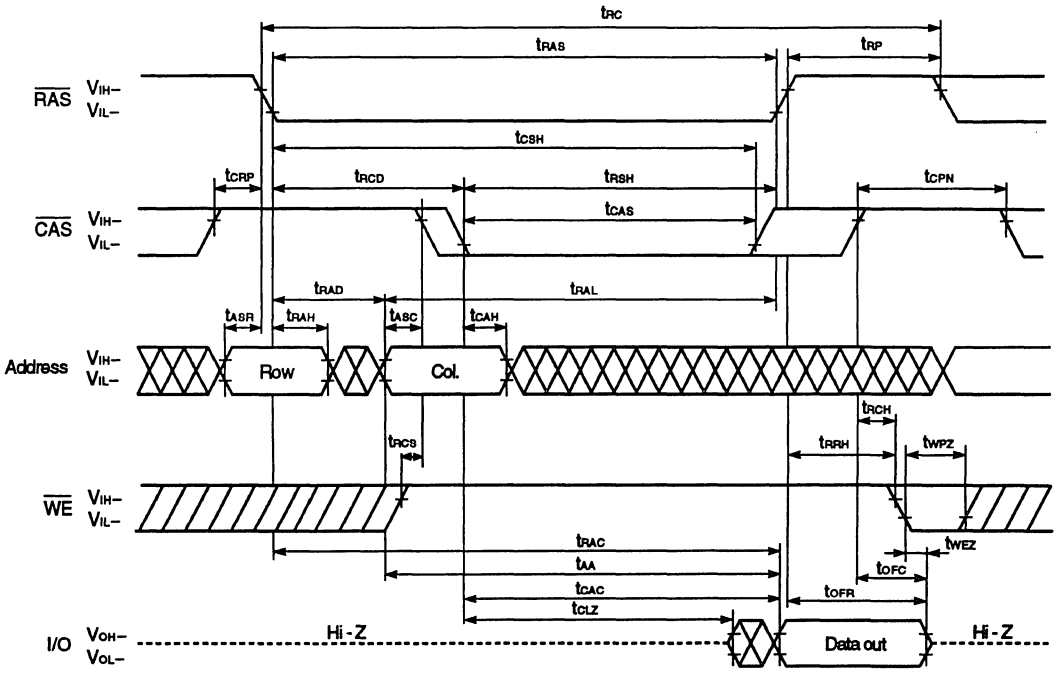


Hidden Refresh Cycle (Write)

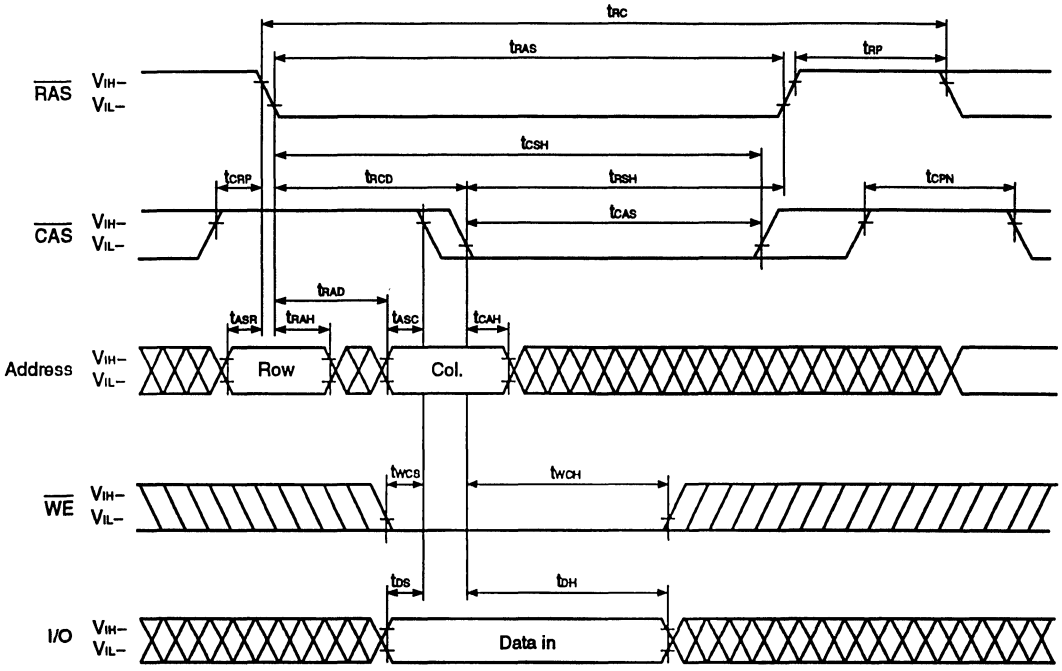


Timing Chart 3

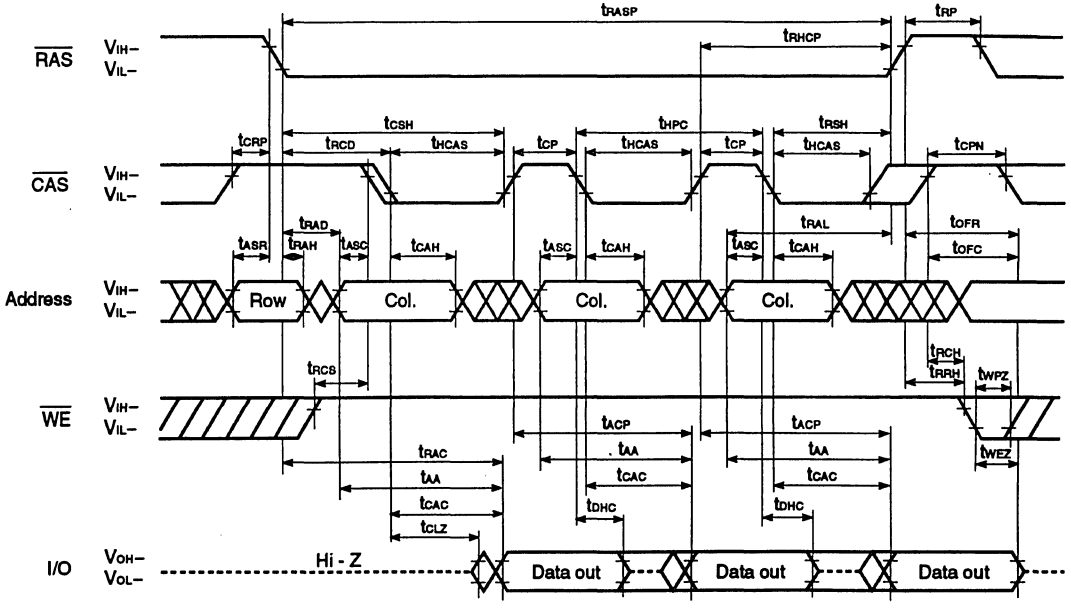
Read Cycle


tRC
tRAS
tRP
RAS VIH– VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS VIH– VIL–
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address VIH– VIL–
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE VIH– VIL–
tRAC
tAA
tWEZ
tOFC
tCAC
tOFR
tCLZ
I/O VOH– VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

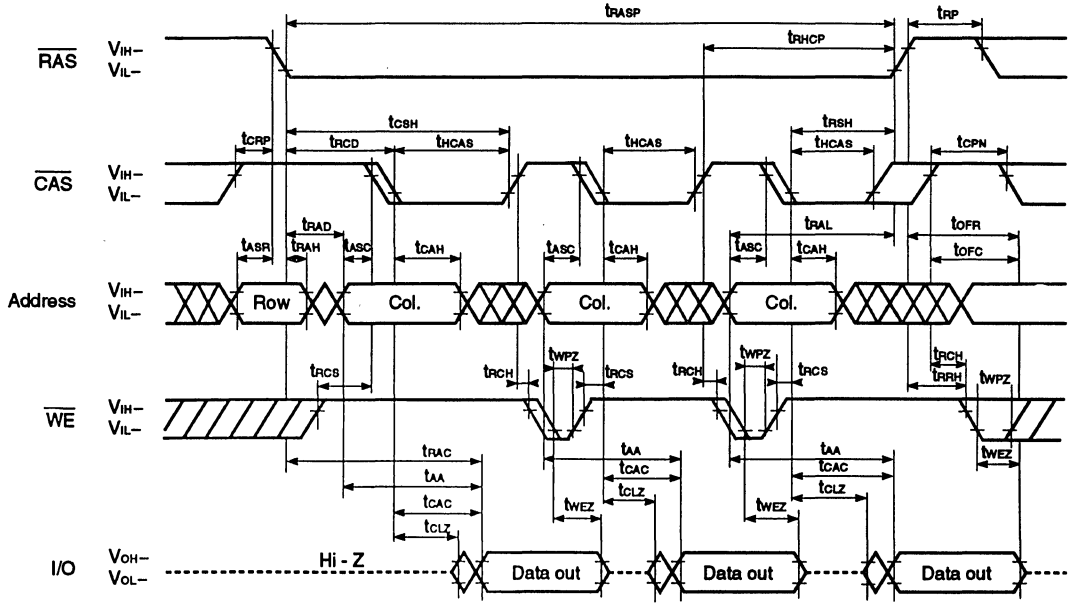


Hyper Page Mode Read Cycle



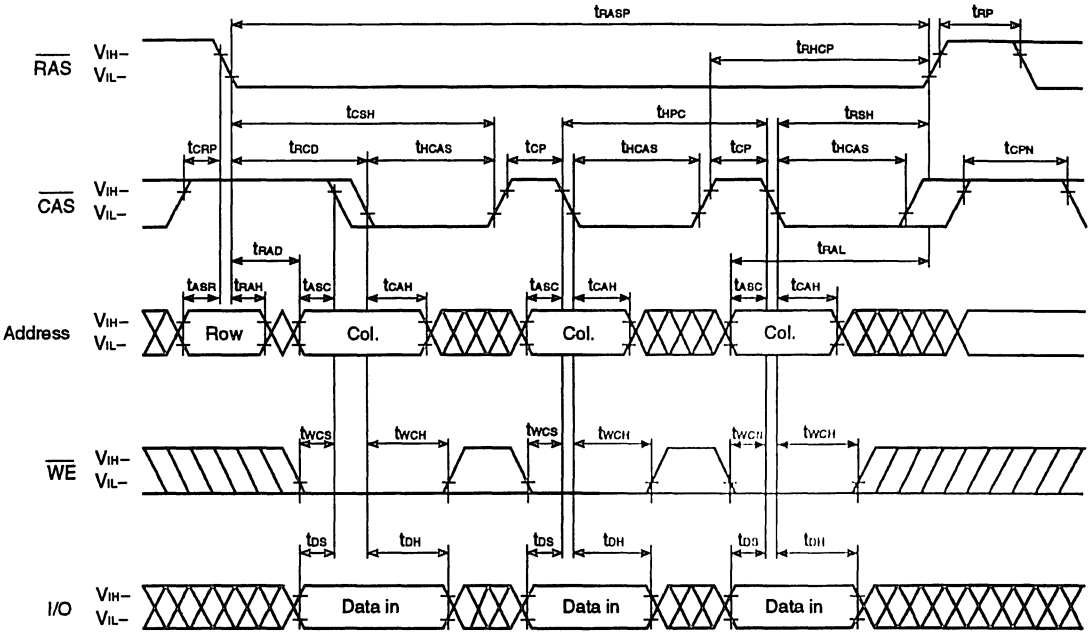
Remark In the hyper page mode,read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{WE}$ Control)



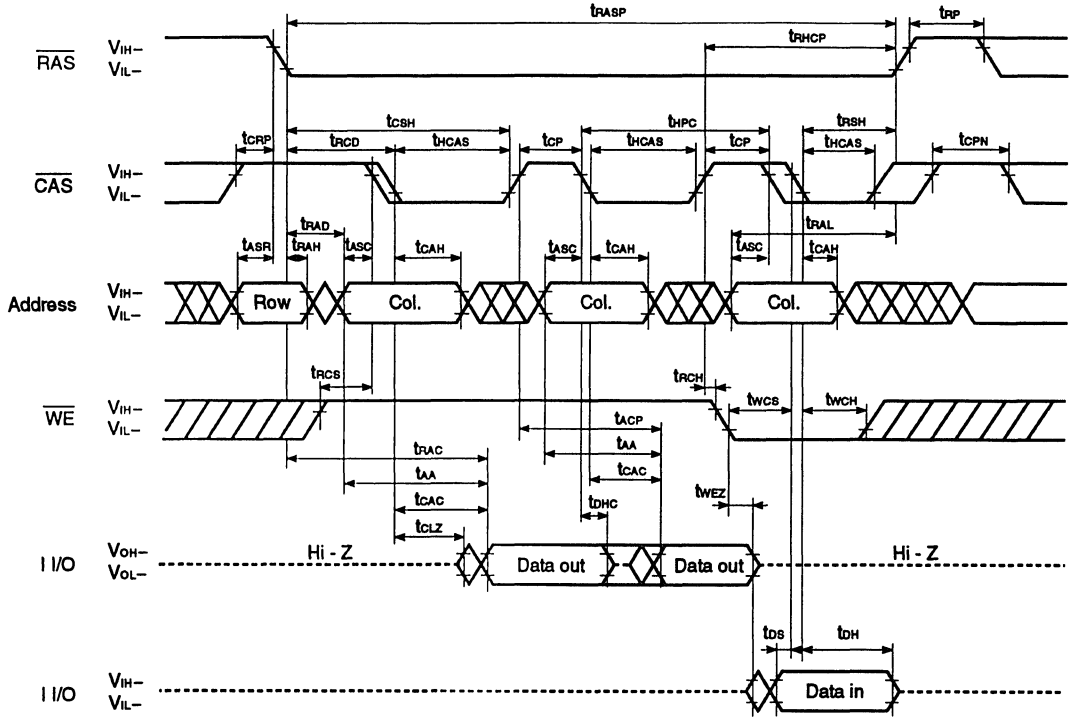
Remark In the hyper page mode,read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Early Write Cycle



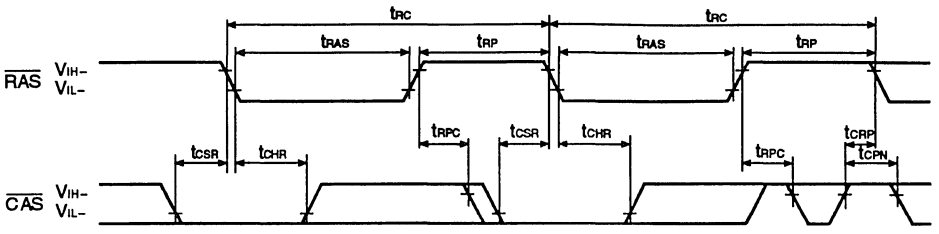
Remark In the hyper page mode,read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read and Write Cycle



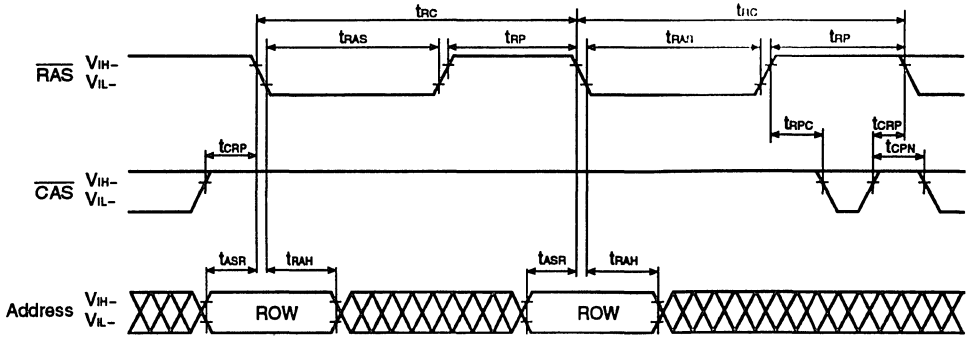
Remark In the hyper page mode,read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



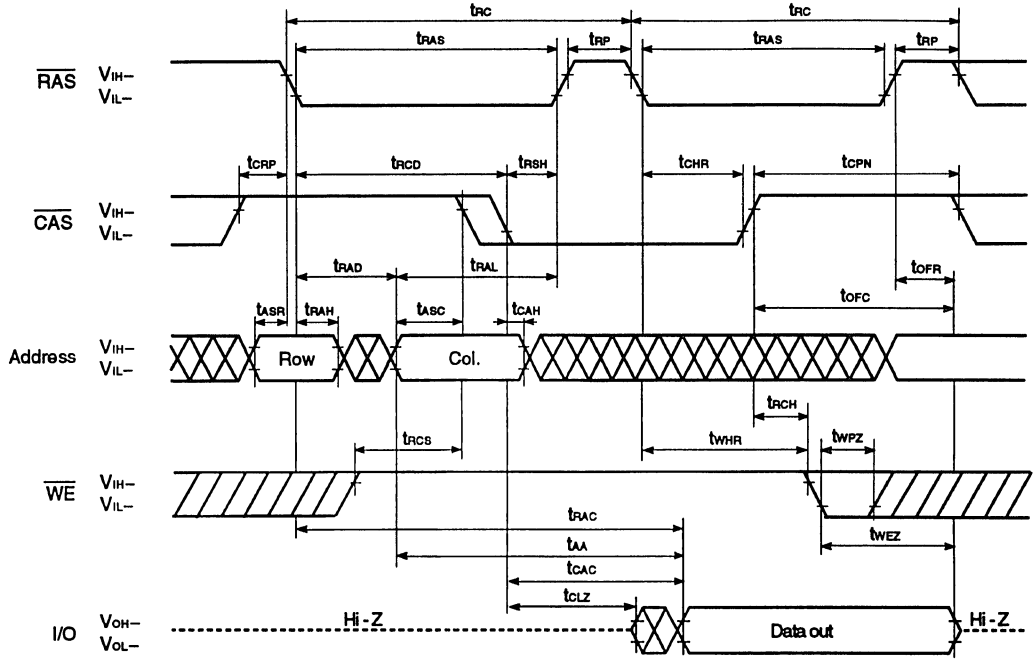
Remark Address,$\overline{WE}$ = Don't care I/O = Hi - Z

$\overline{RAS}$ Only Refresh Cycle

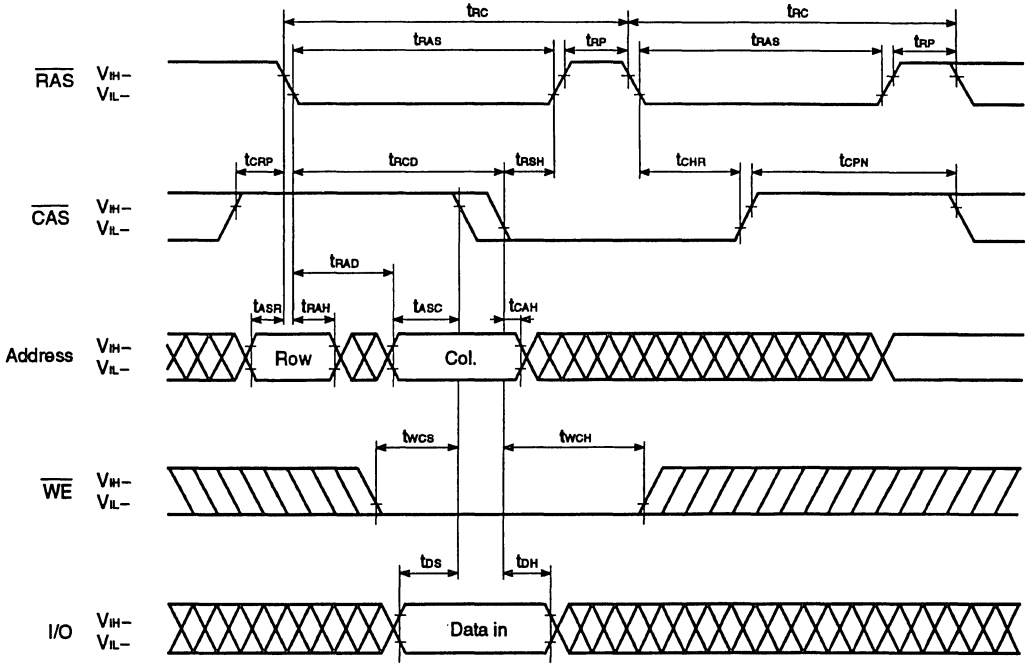


Remark $\overline{WE}$ = Don't care , I/O = Hi - Z

Hidden Refresh Cycle (Read)

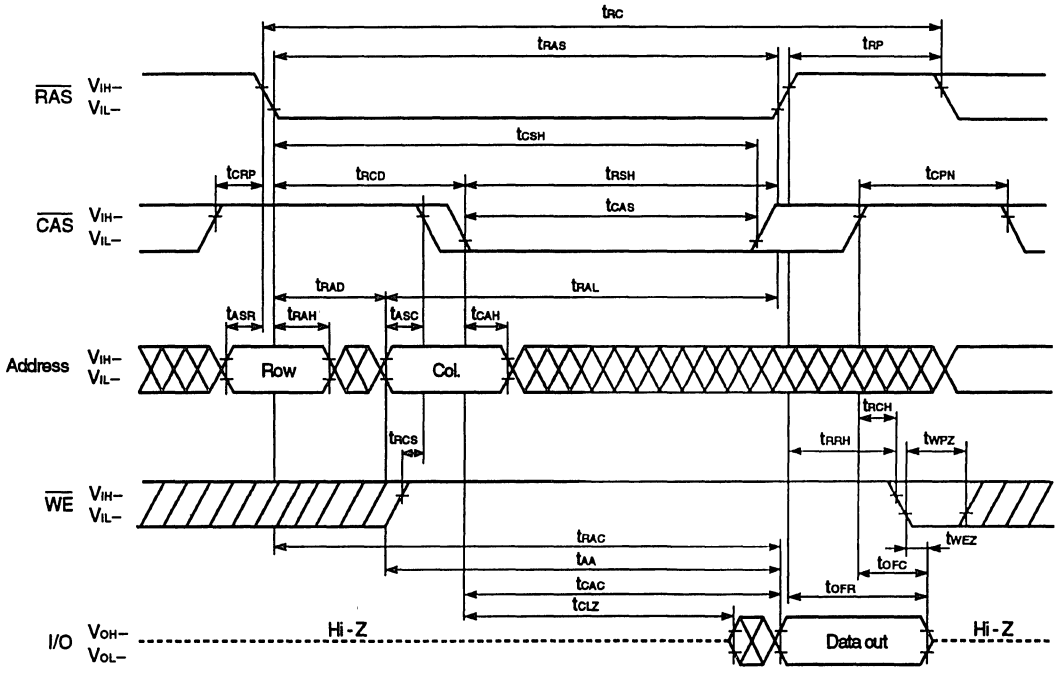


Hidden Refresh Cycle (Write)

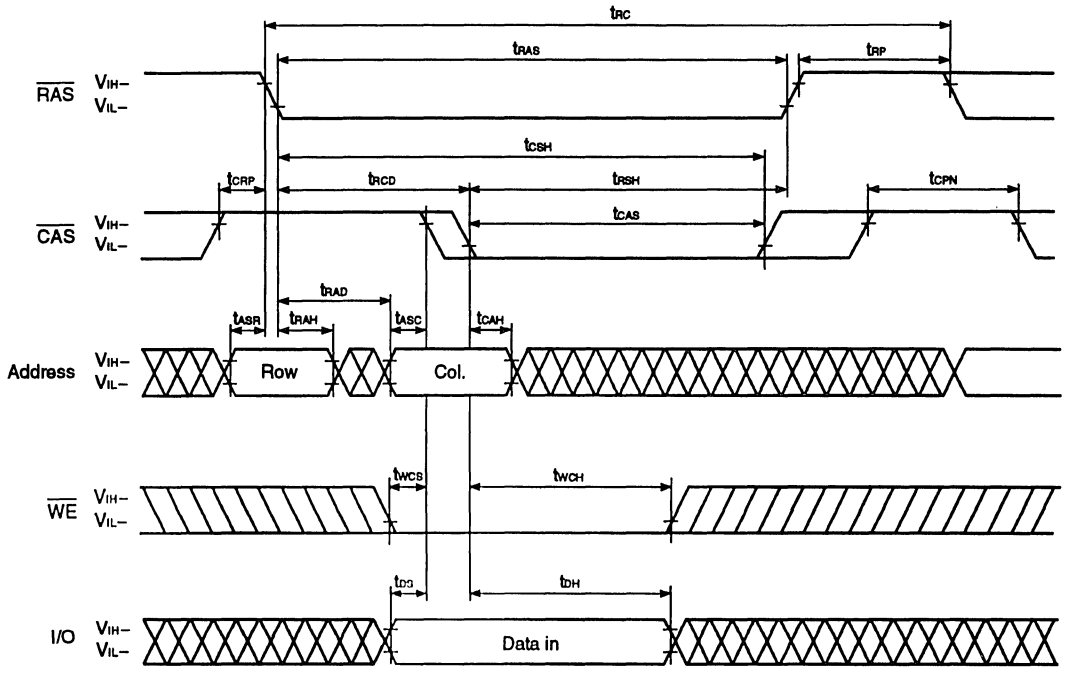


Timing Chart 4

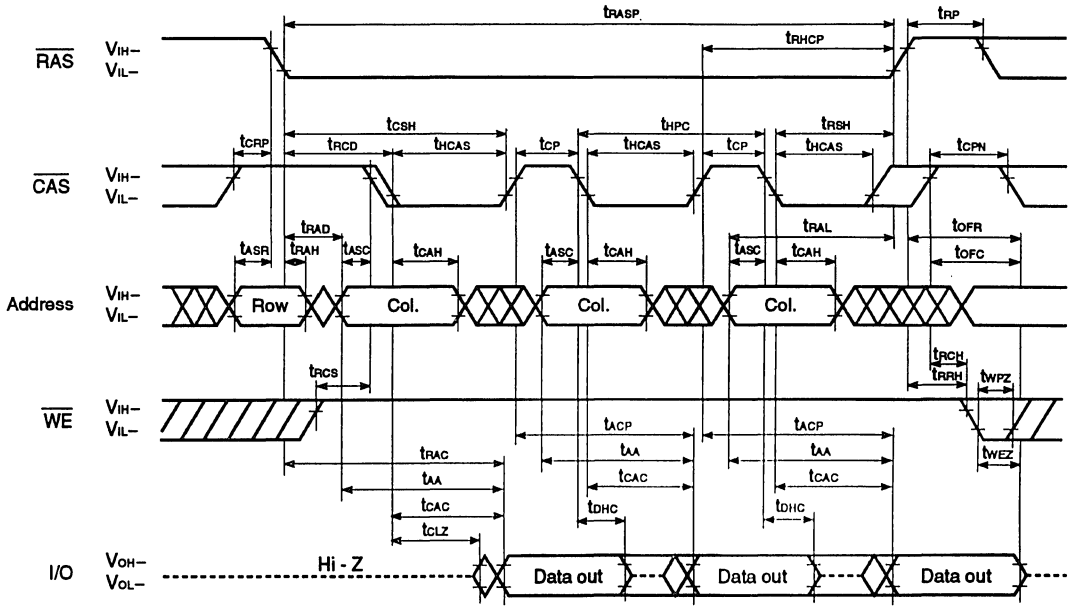
Read Cycle


tRC
tRAS
tRP
RAS VIH– VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS VIH– VIL–
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address VIH– VIL–
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE VIH– VIL–
tRAC
tAA
tWEZ
tOFC
tCAC
tOFR
tCLZ
I/O VOH– VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

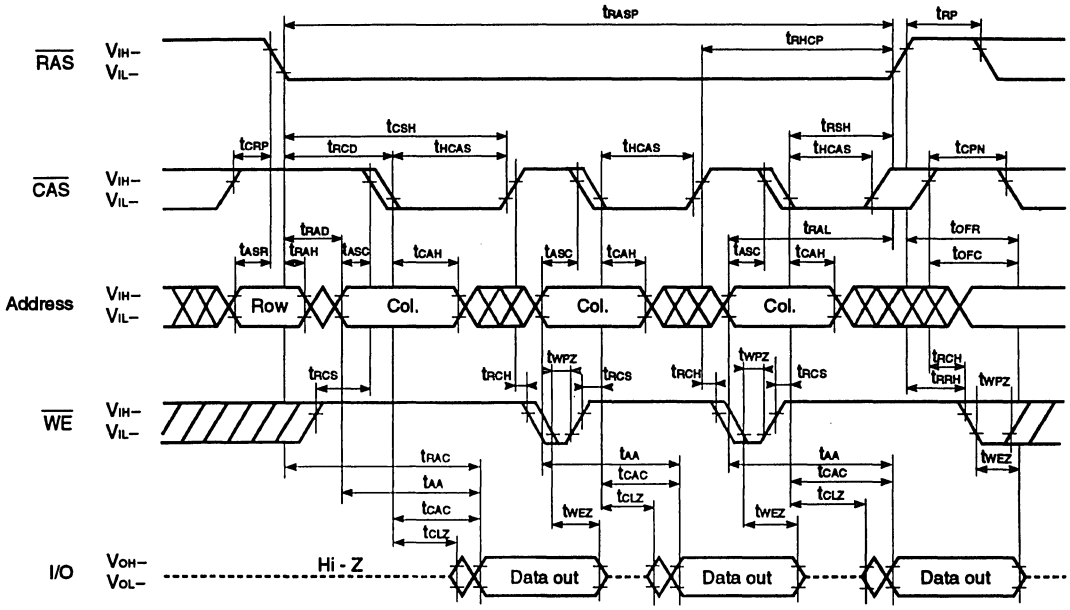


Hyper Page Mode Read Cycle



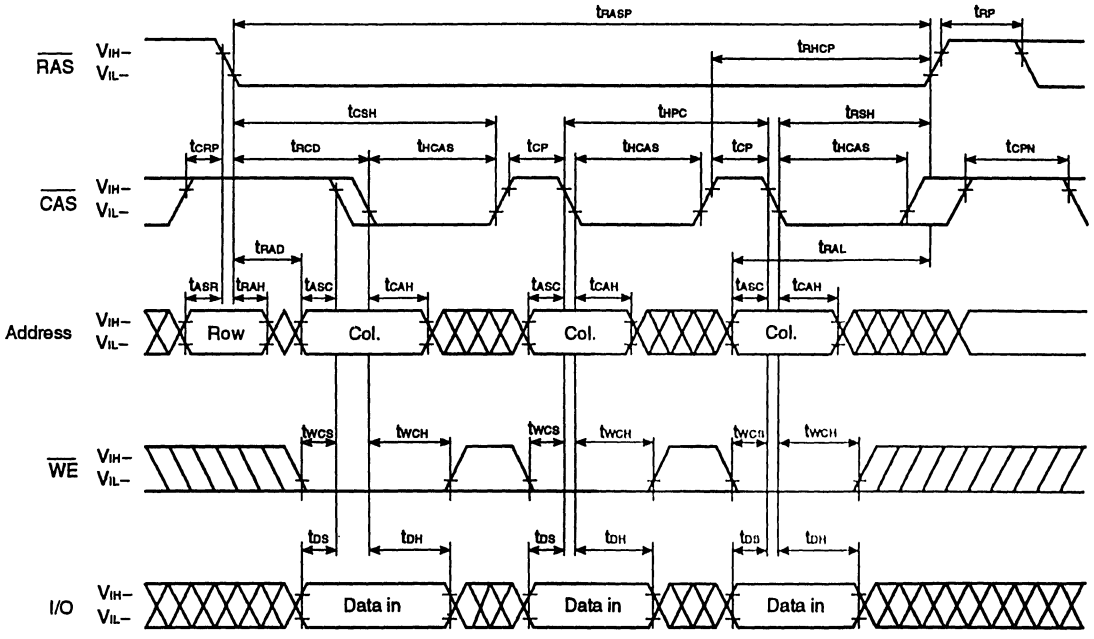
Remark In the hyper page mode,read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{WE}$ Control)



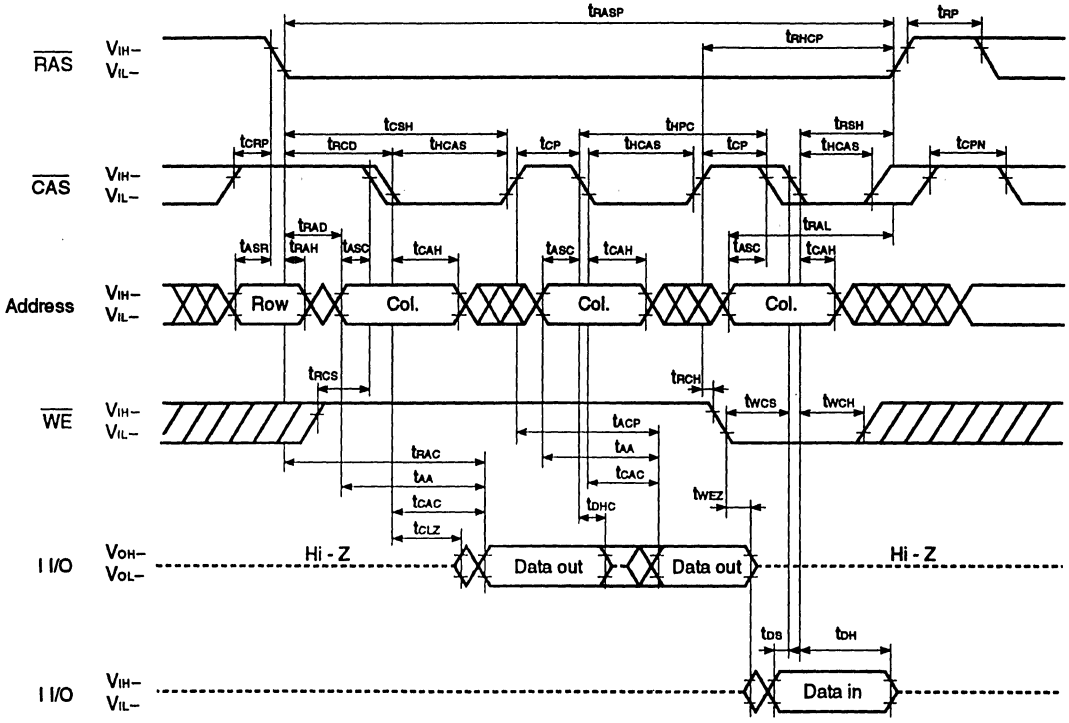
Remark In the hyper page mode,read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Early Write Cycle



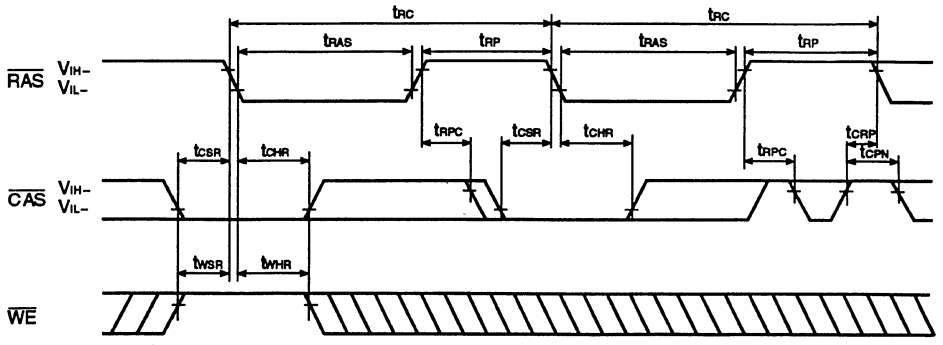
Remark In the hyper page mode,read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read and Write Cycle



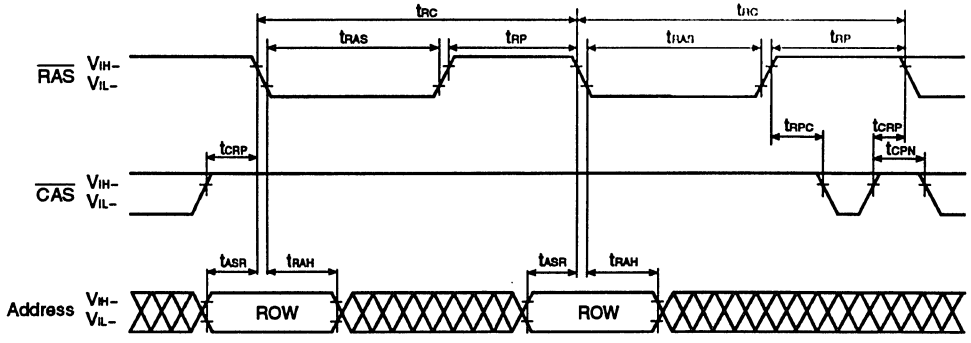
Remark In the hyper page mode,read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



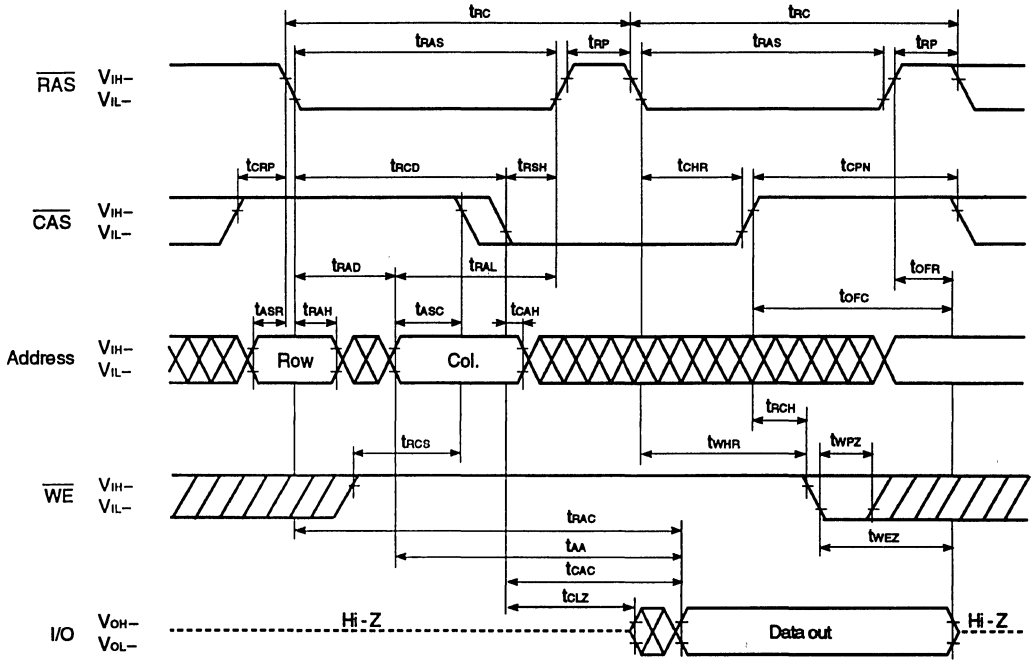
Remark Address = Don't care I/O = Hi - Z

$\overline{RAS}$ Only Refresh Cycle

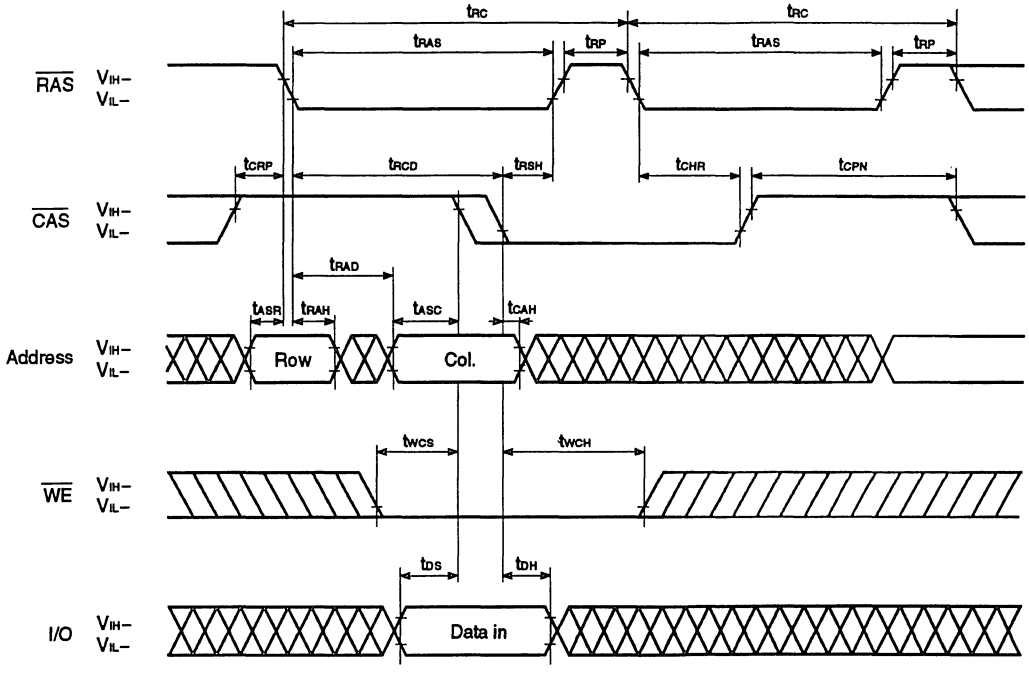


Remark $\overline{WE}$ = Don't care , I/O = Hi - Z

Hidden Refresh Cycle (Read)

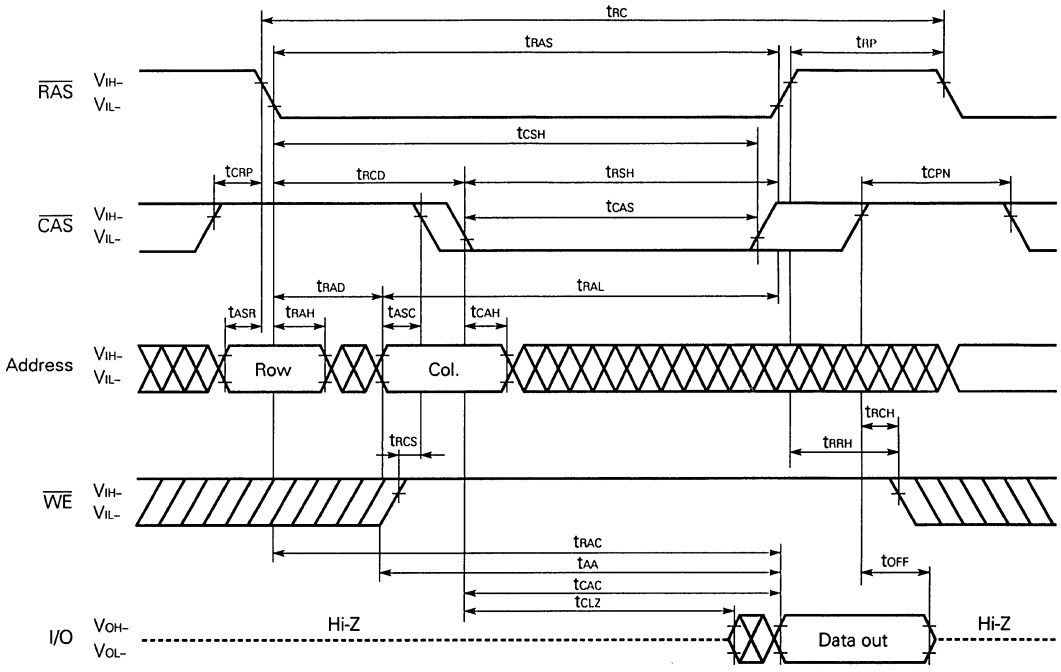


Hidden Refresh Cycle (Write)

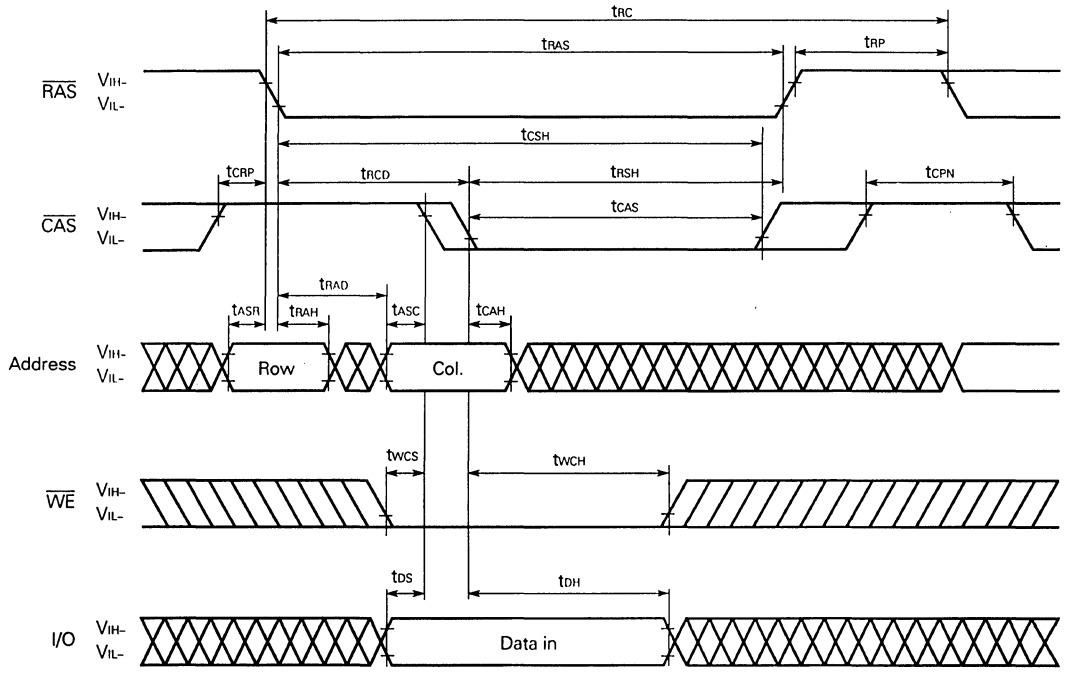


Timing Chart 5

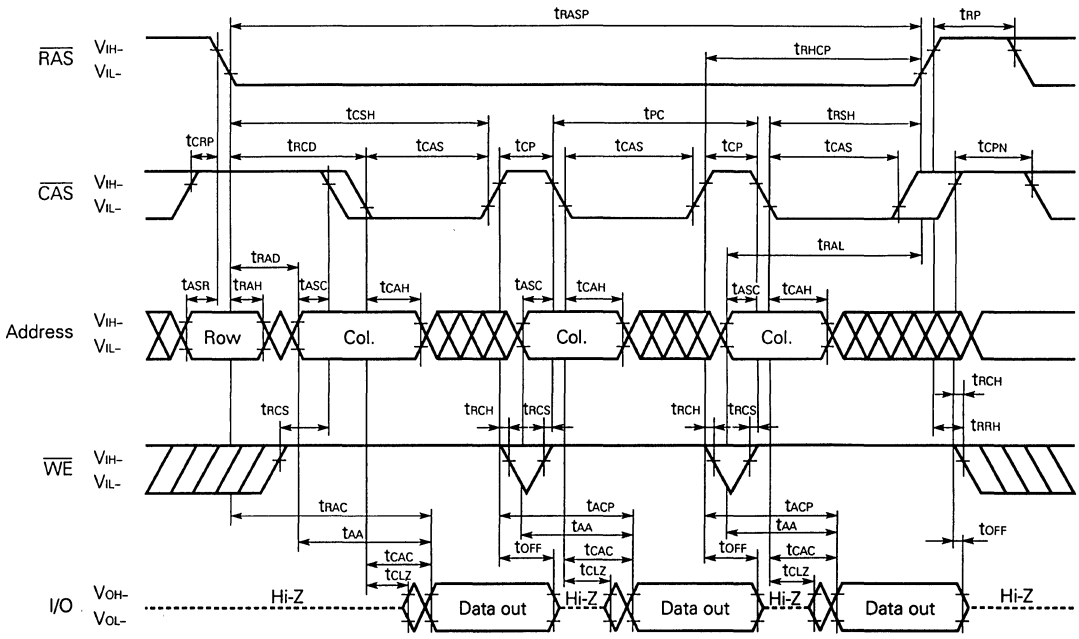
Read Cycle


tRC
tRAS
tRP
RAS
VIH-
VIL-
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
VIH-
VIL-
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
VIH-
VIL-
Row
Col.
tRCH
tRCS
tRRH
WE
VIH-
VIL-
tRAC
tAA
tOFF
tCAC
tCLZ
I/O
VOH-
VOL-
Hi-Z
Data out
Hi-Z

Early Write Cycle

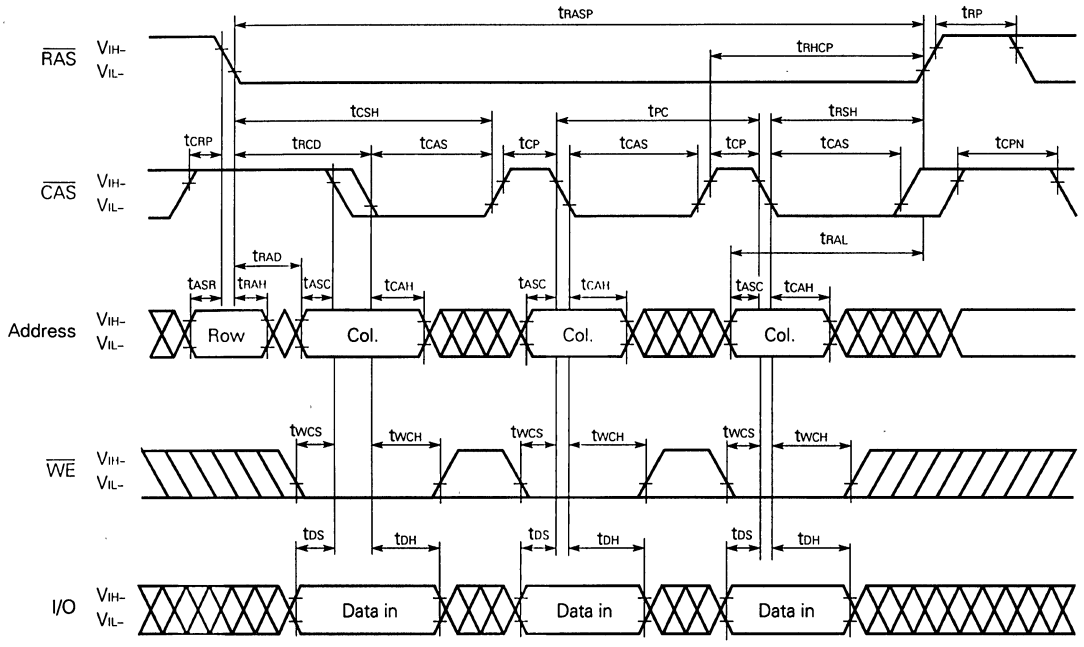


Fast Page Mode Read Cycle



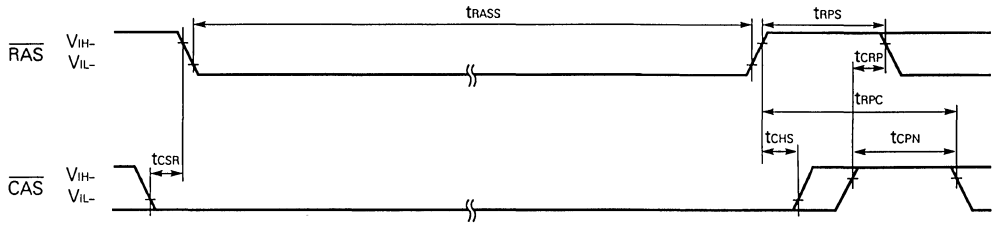
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle



Remark Address, $\overline{WE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

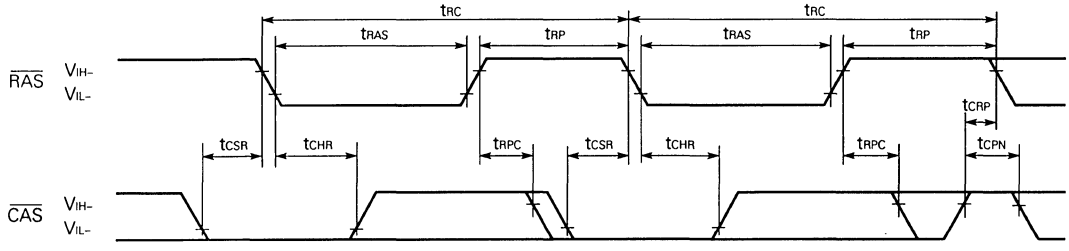
$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with burst long $\overline{RAS}$ only refresh, the following cautions must be observed.

(1) **Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh**
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 1,024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) **Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst Long $\overline{RAS}$ Only Refresh**
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 1,024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

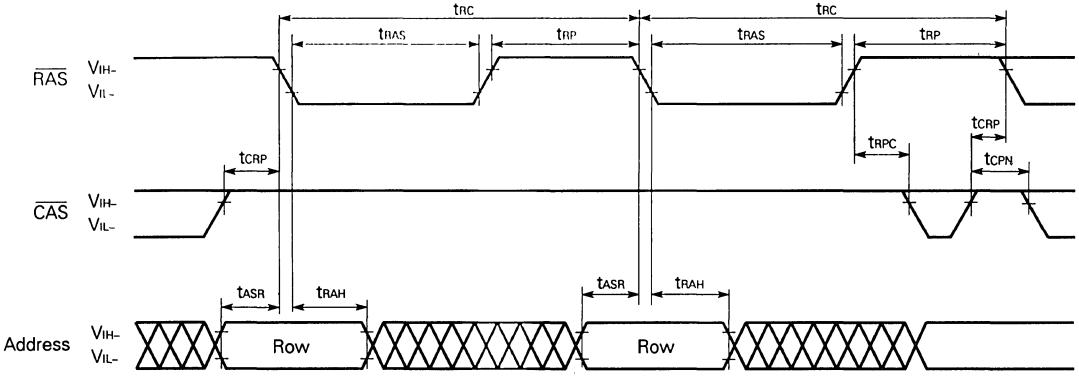
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



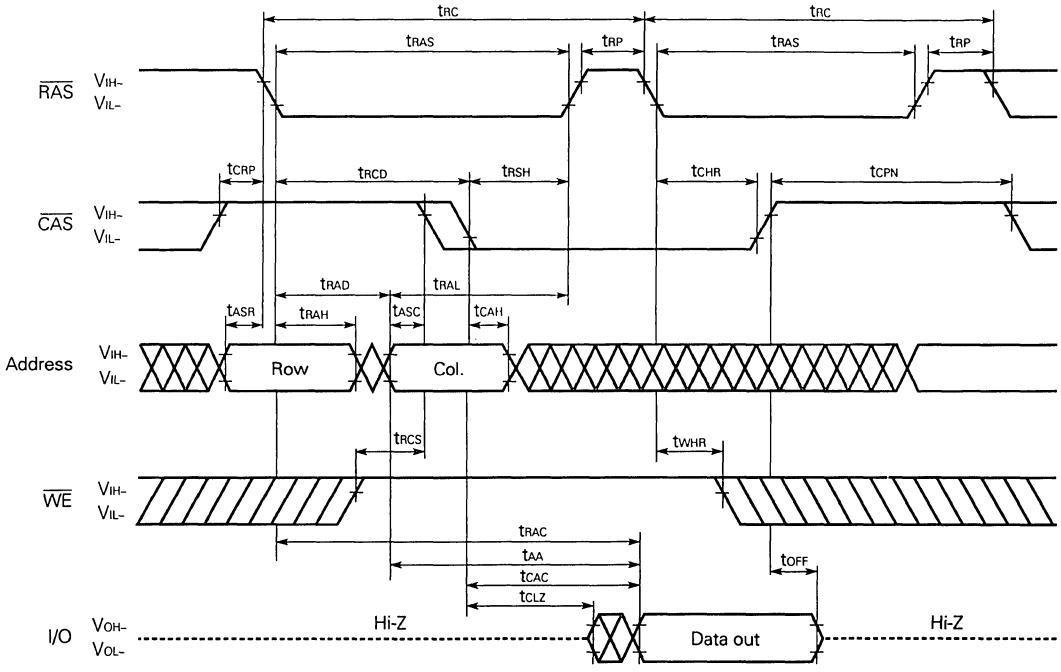
Remark Address, $\overline{WE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

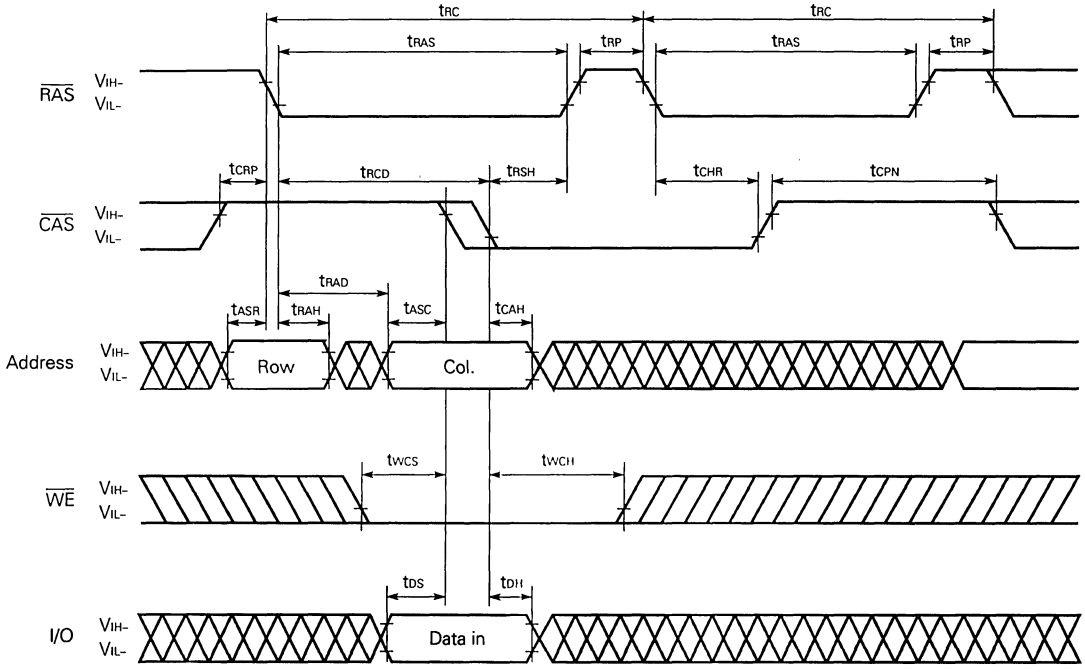


Remark $\overline{WE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

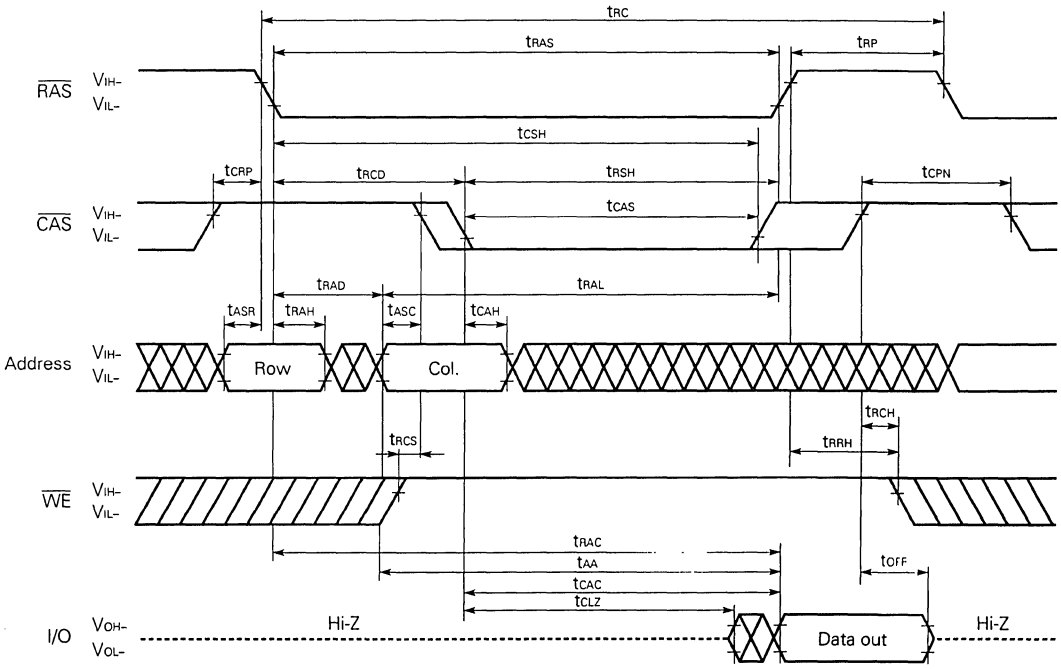


Hidden Refresh Cycle (Write)

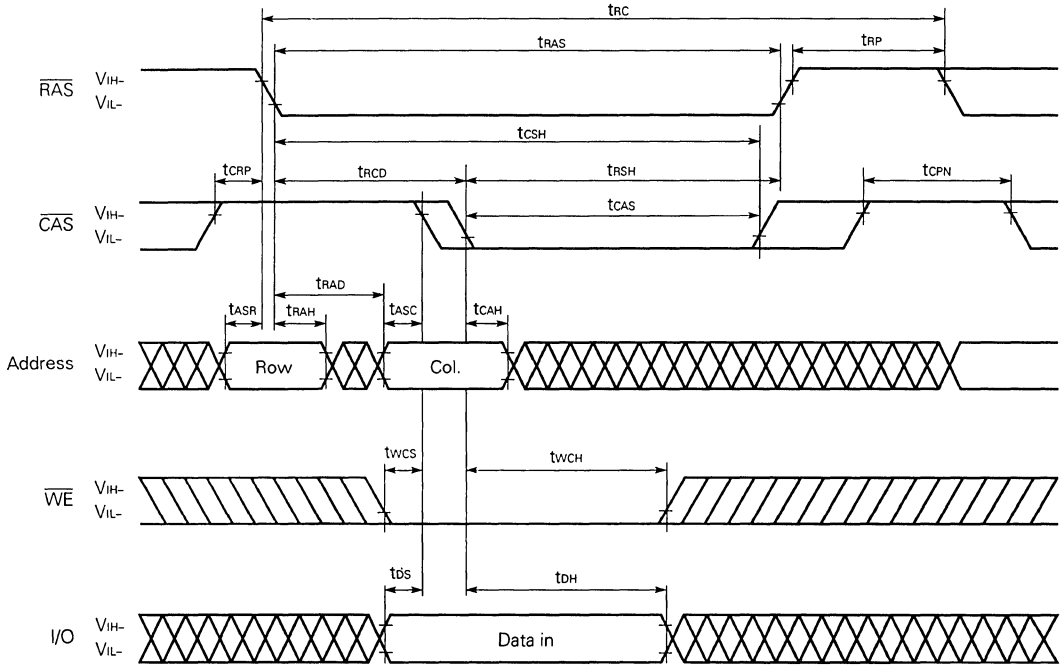


Timing Chart 6

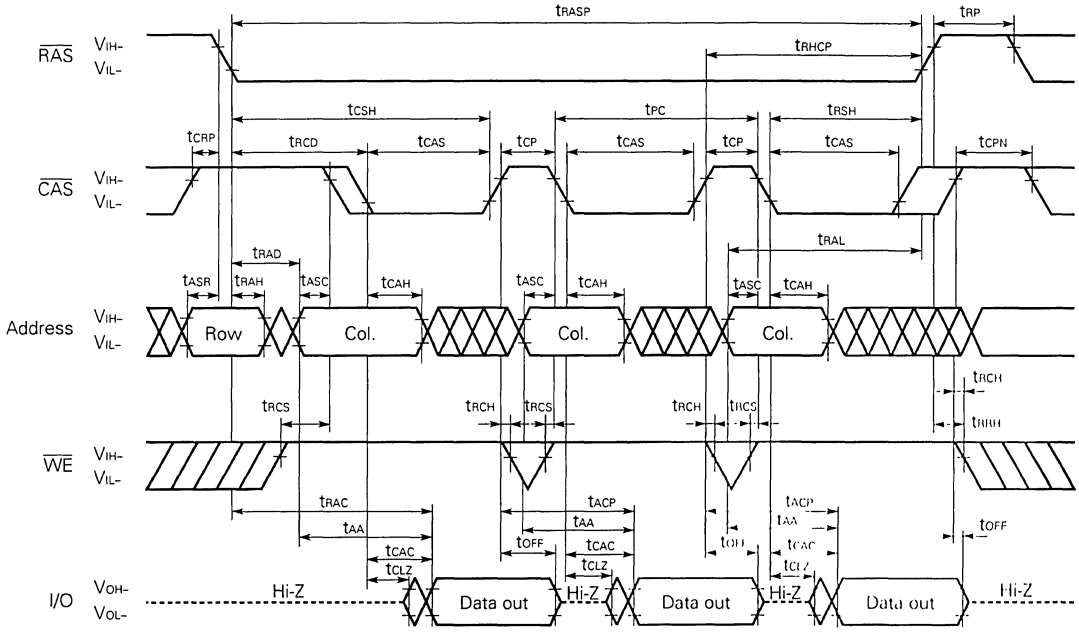
Read Cycle


tRC
tRAS
tRP
RAS
VIH-
VIL-
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
VIH-
VIL-
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
VIH-
VIL-
Row
Col.
tRCH
tRCS
tRRH
WE
VIH-
VIL-
tRAC
tAA
tOFF
tCAC
tCLZ
I/O
VOH-
VOL-
Hi-Z
Data out
Hi-Z

Early Write Cycle

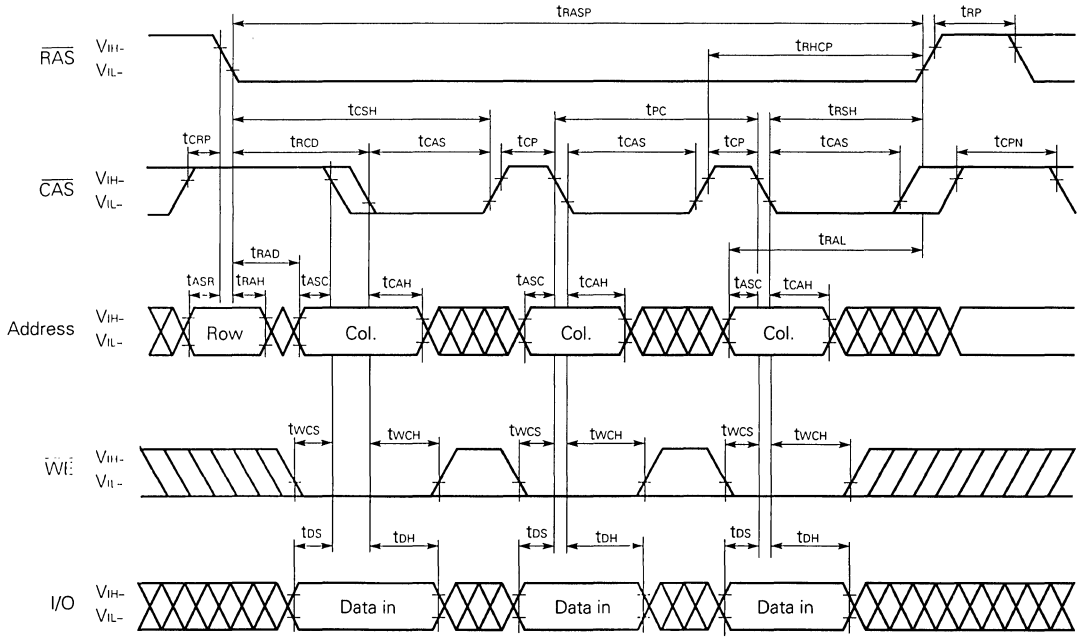


Fast Page Mode Read Cycle



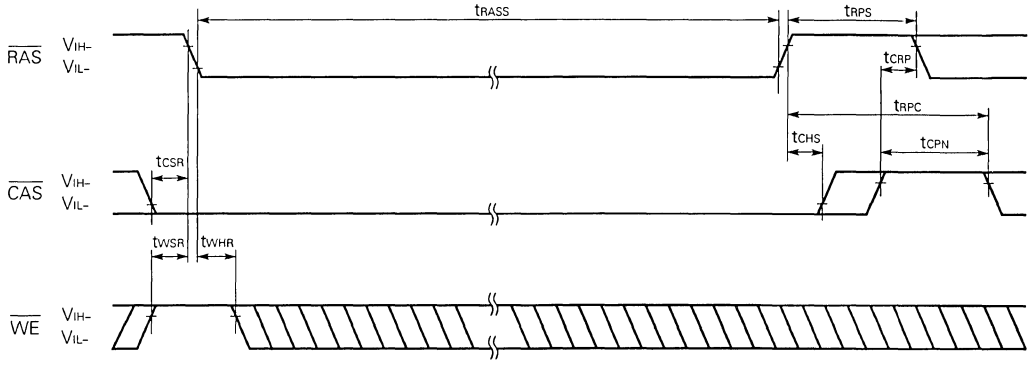
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle



Remark Address : Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh

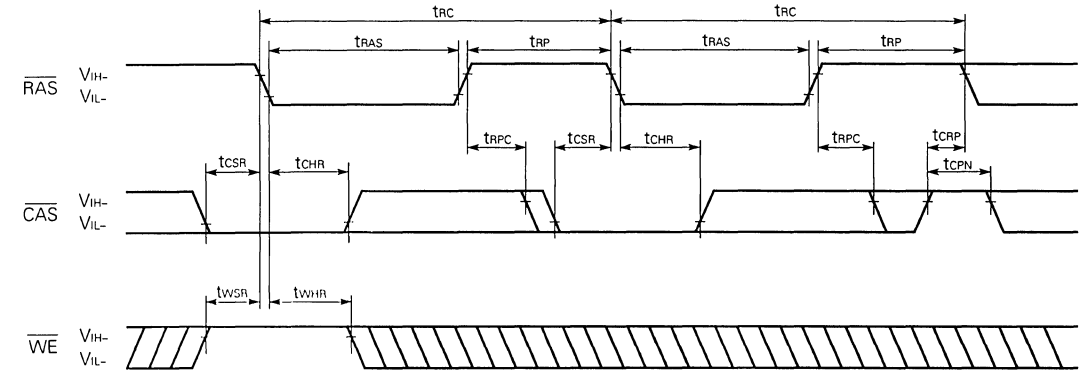
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh

When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

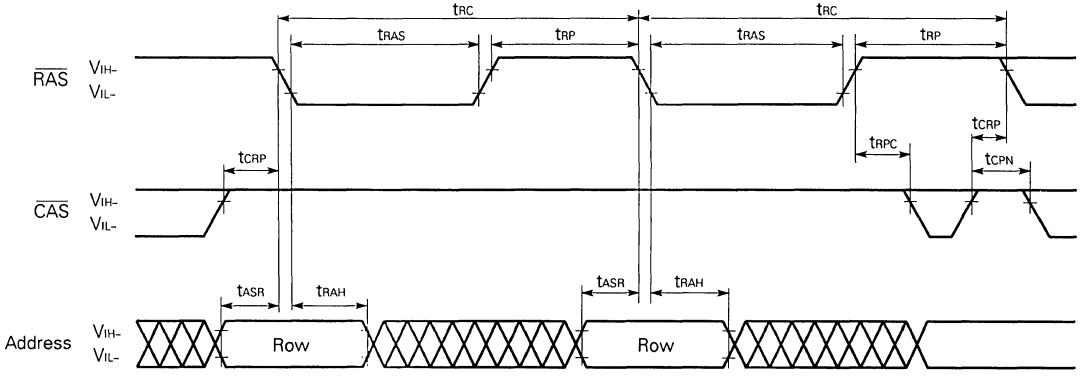
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



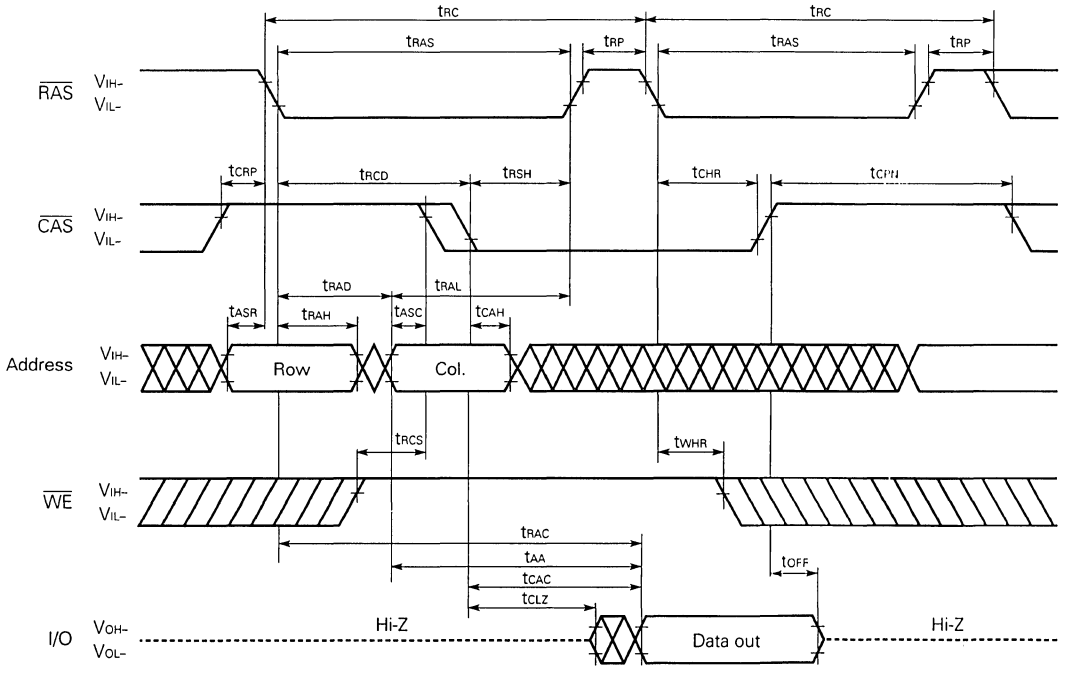
Remark Address : Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

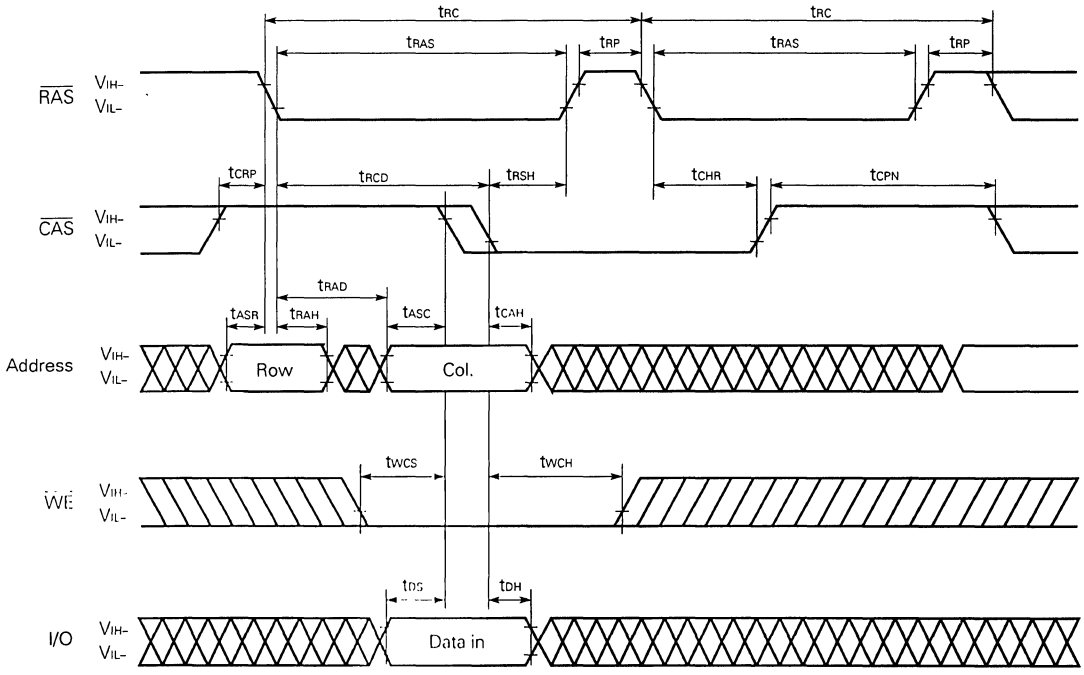


Remark $\overline{WE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

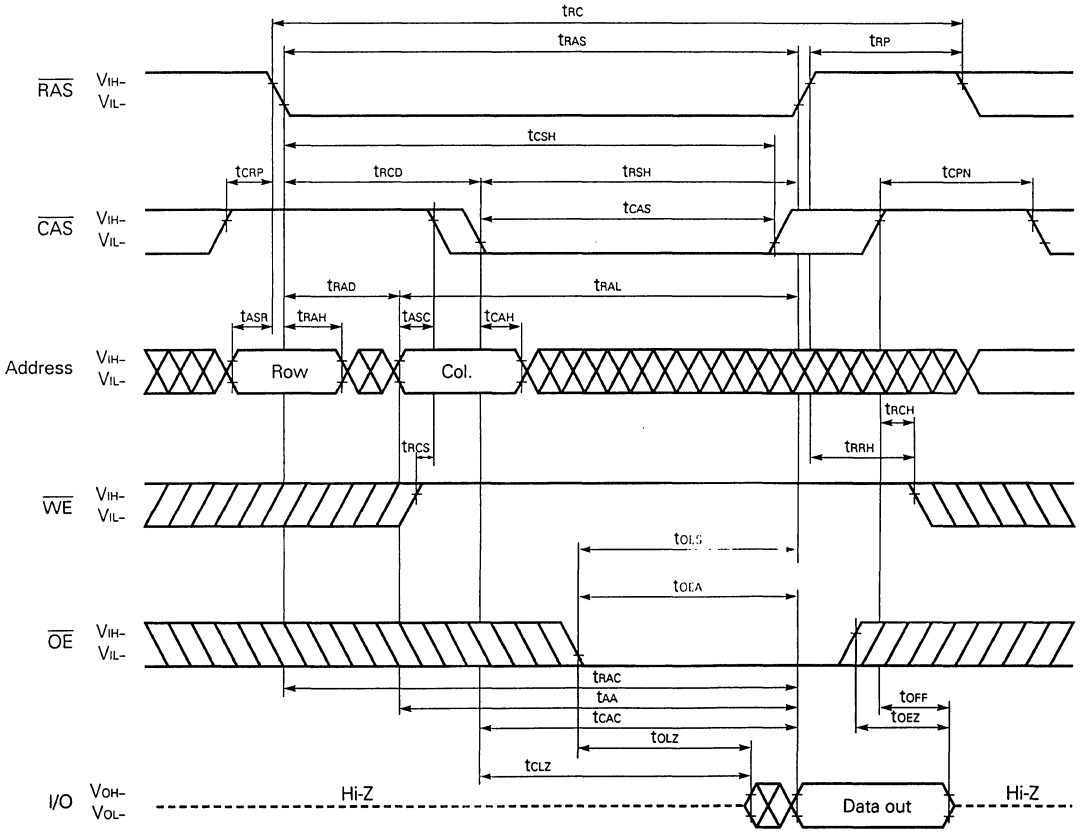


Hidden Refresh Cycle (Write)

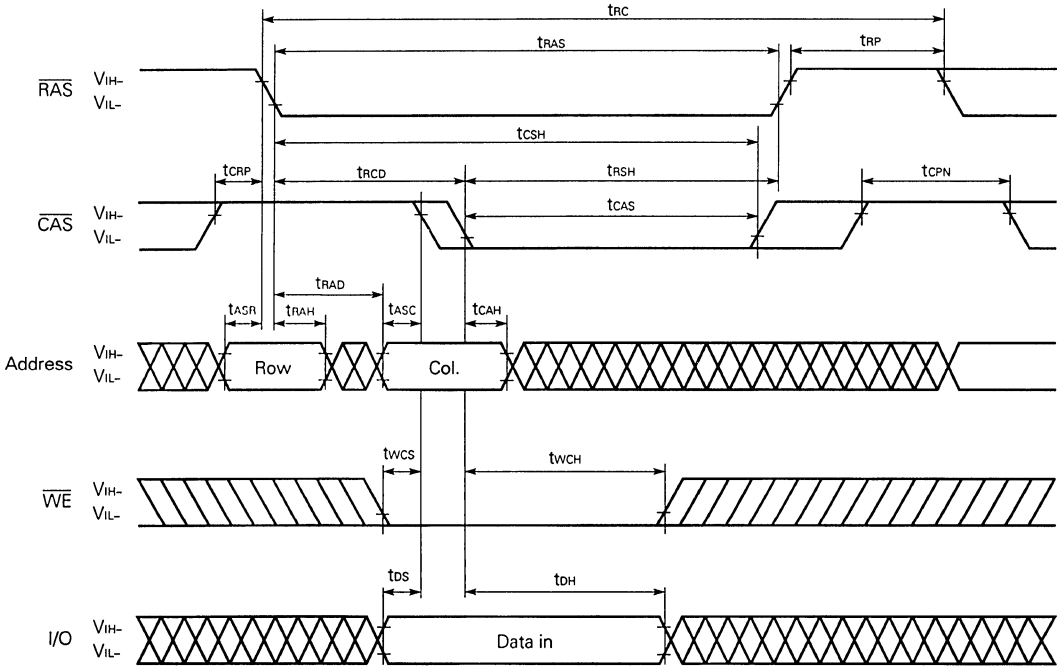


Timing Chart 7

Read Cycle

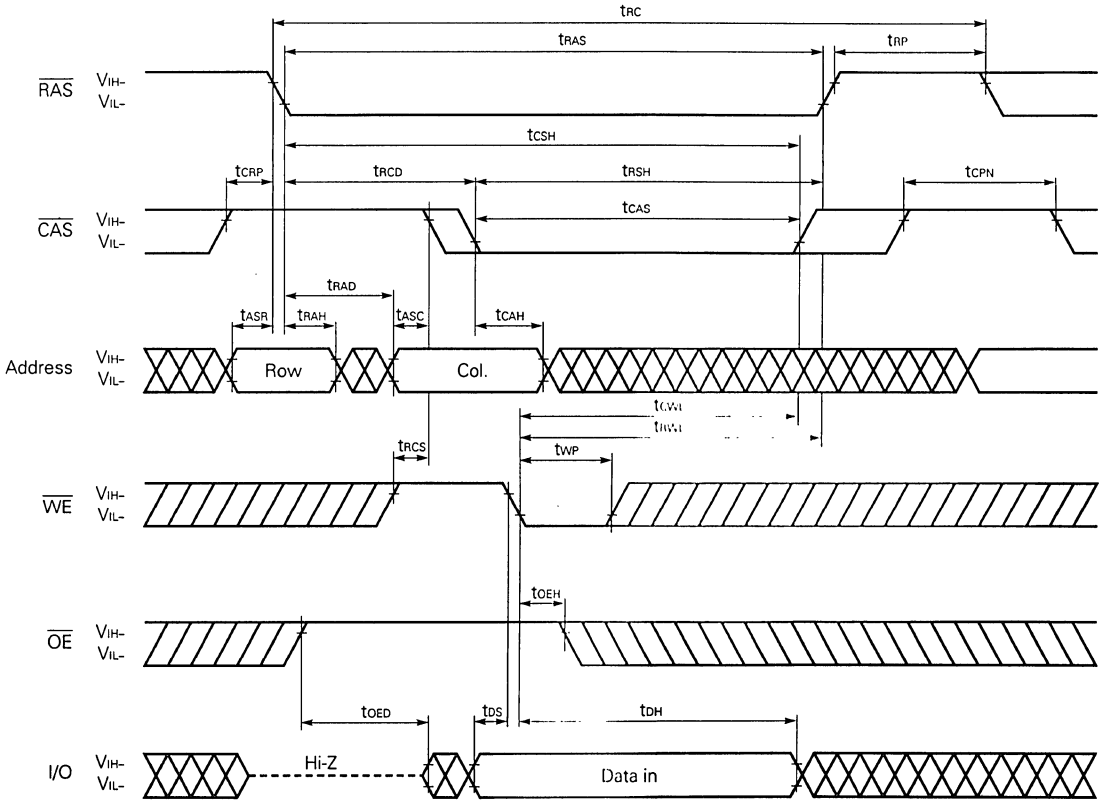

tRC
tRAS
tRP
RAS
VIH-
VIL-
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOLS
tOEA
OE
tRAC
tAA
tOFF
tOEZ
tCAC
tOLZ
tCLZ
I/O
VOH-
VOL-
Hi-Z
Data out
Hi-Z

Early Write Cycle

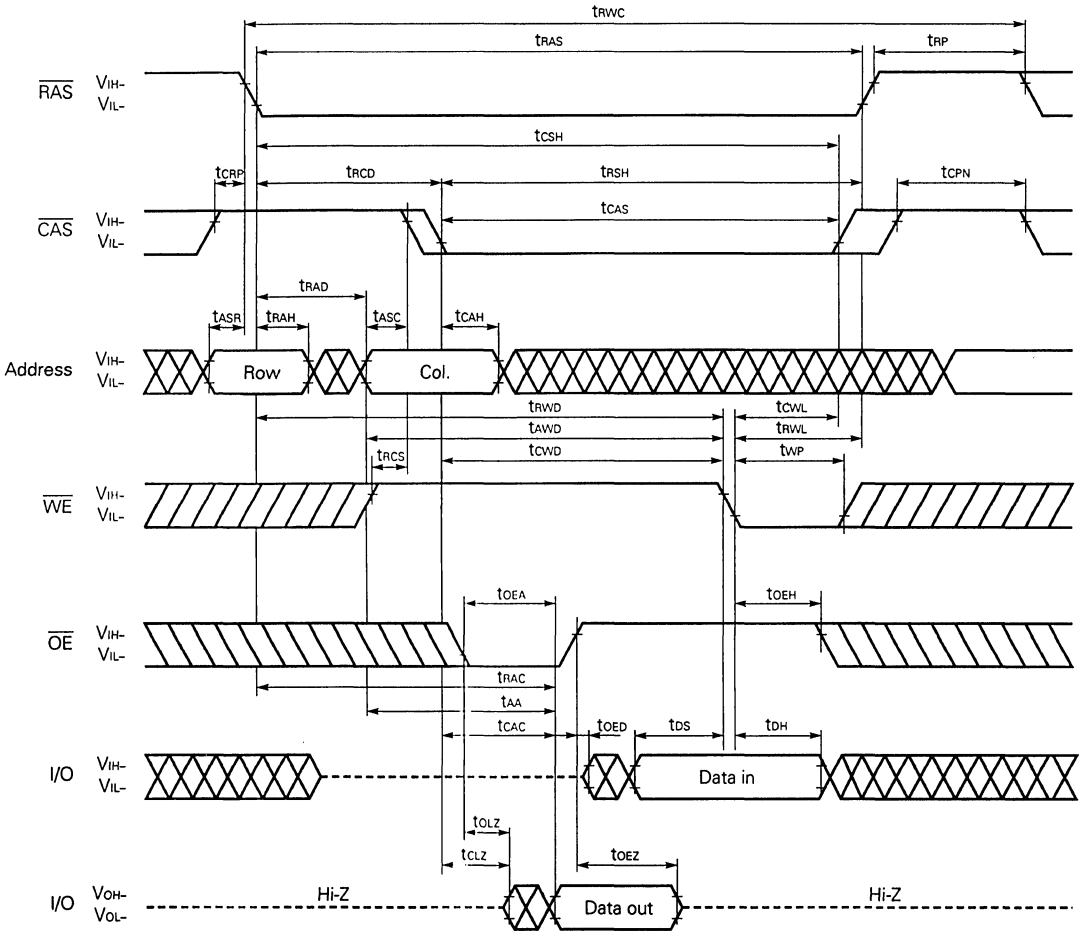


Remark $\overline{OE}$: Don't care

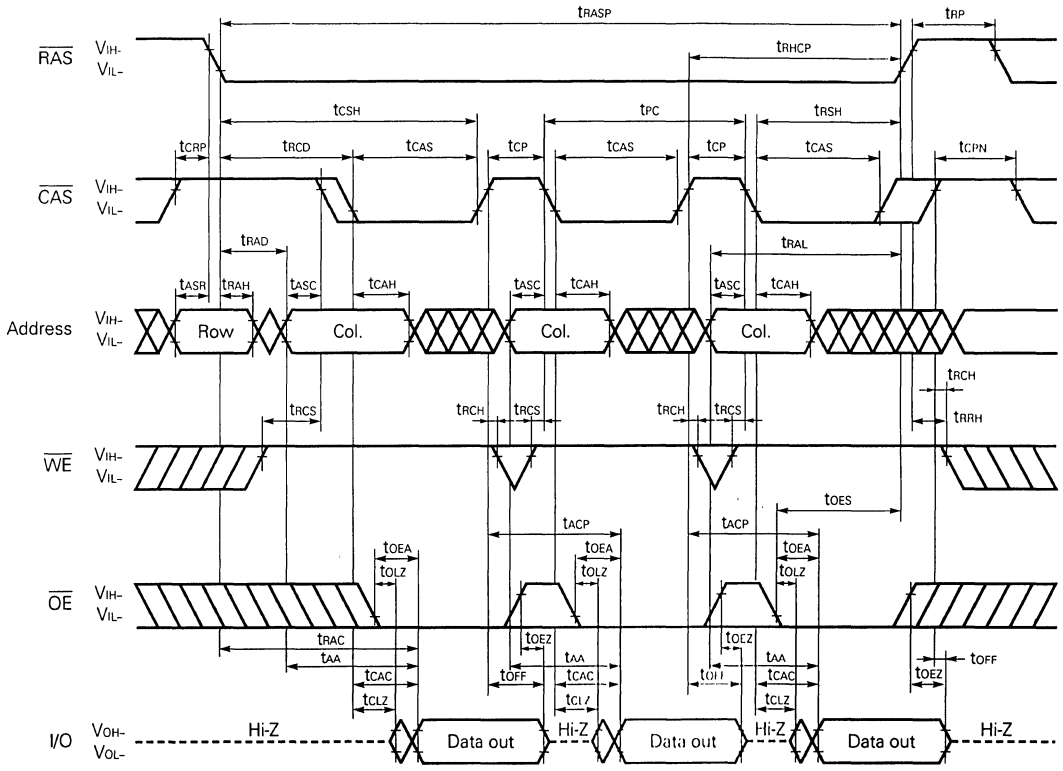
Late Write Cycle



Read Modify Write Cycle

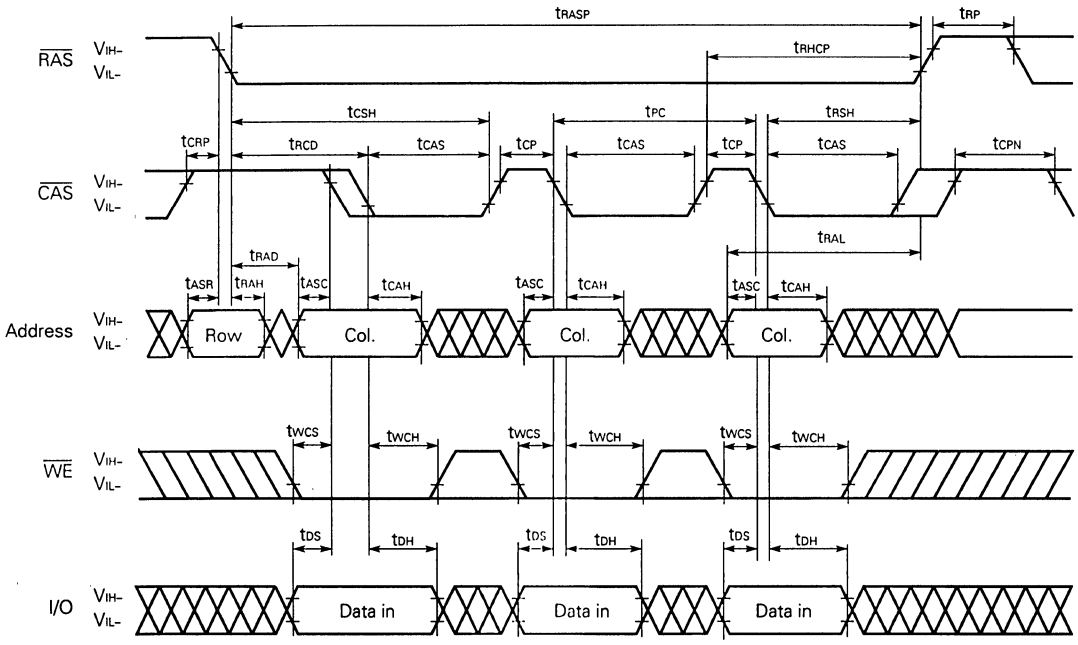


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

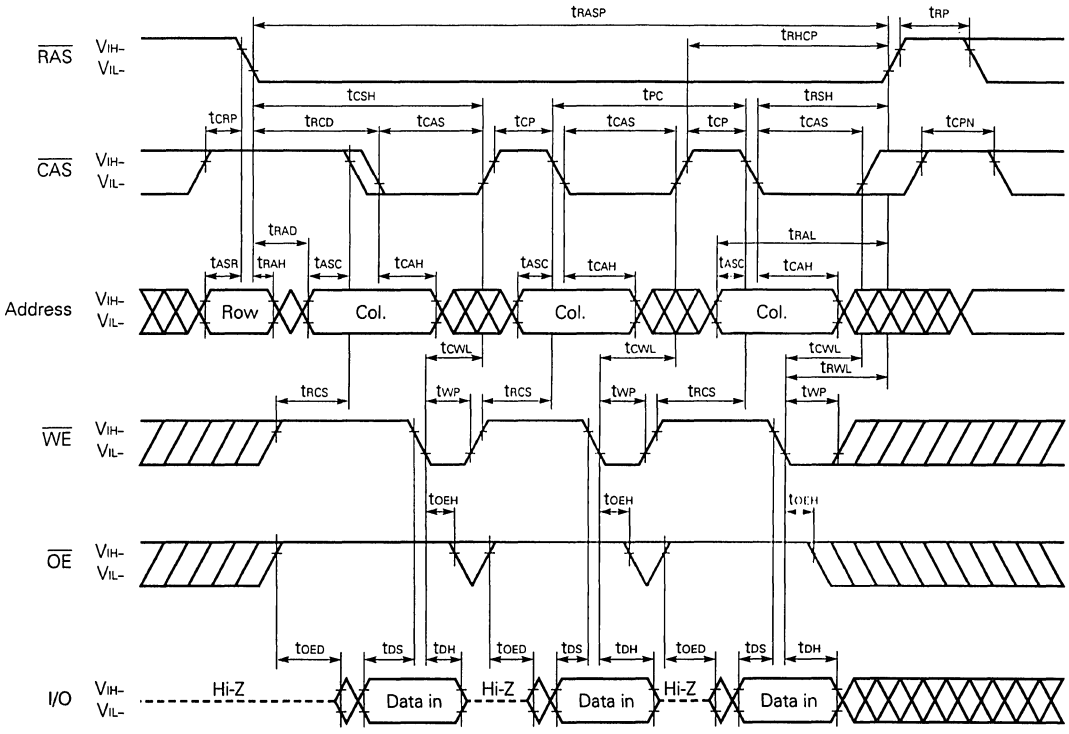
Fast Page Mode Early Write Cycle



Remark $\overline{OE}$: Don't care

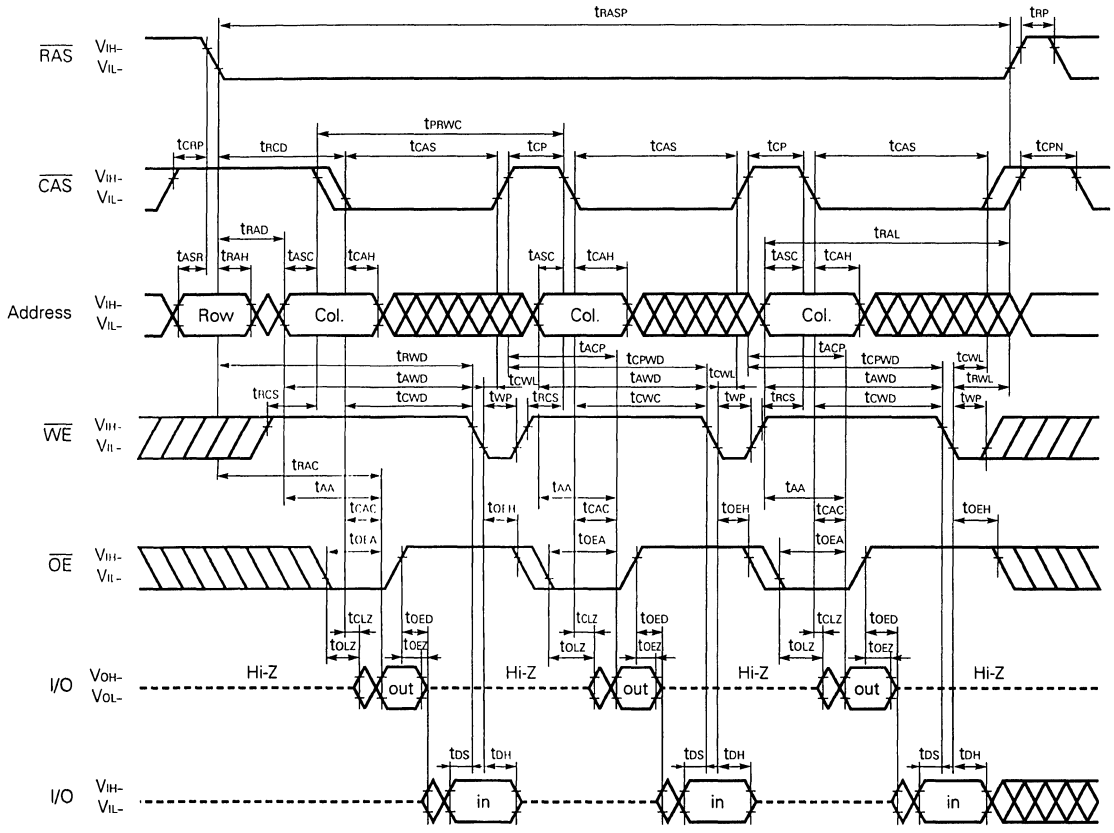
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



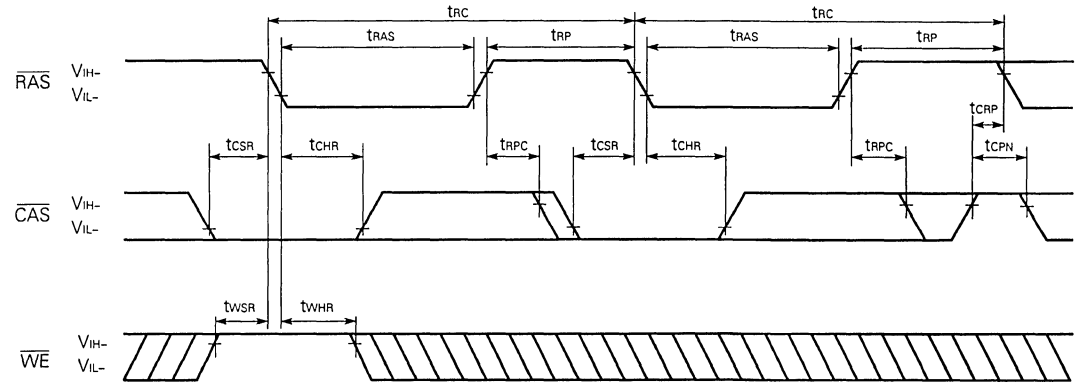
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



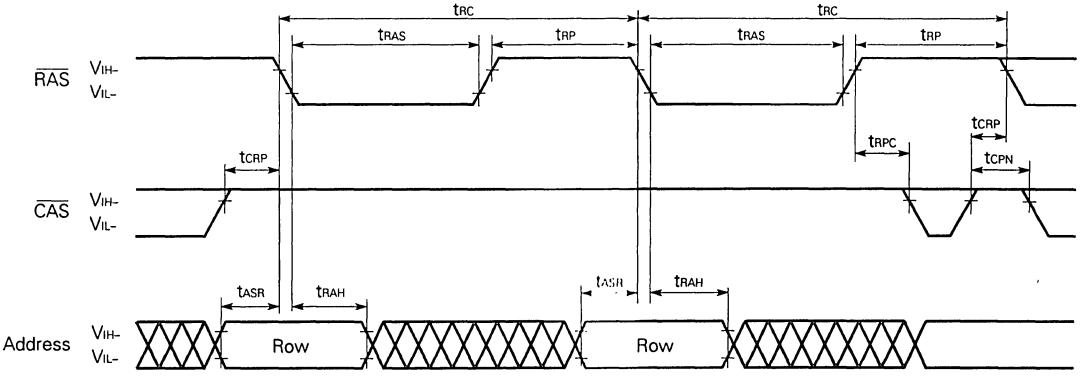
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



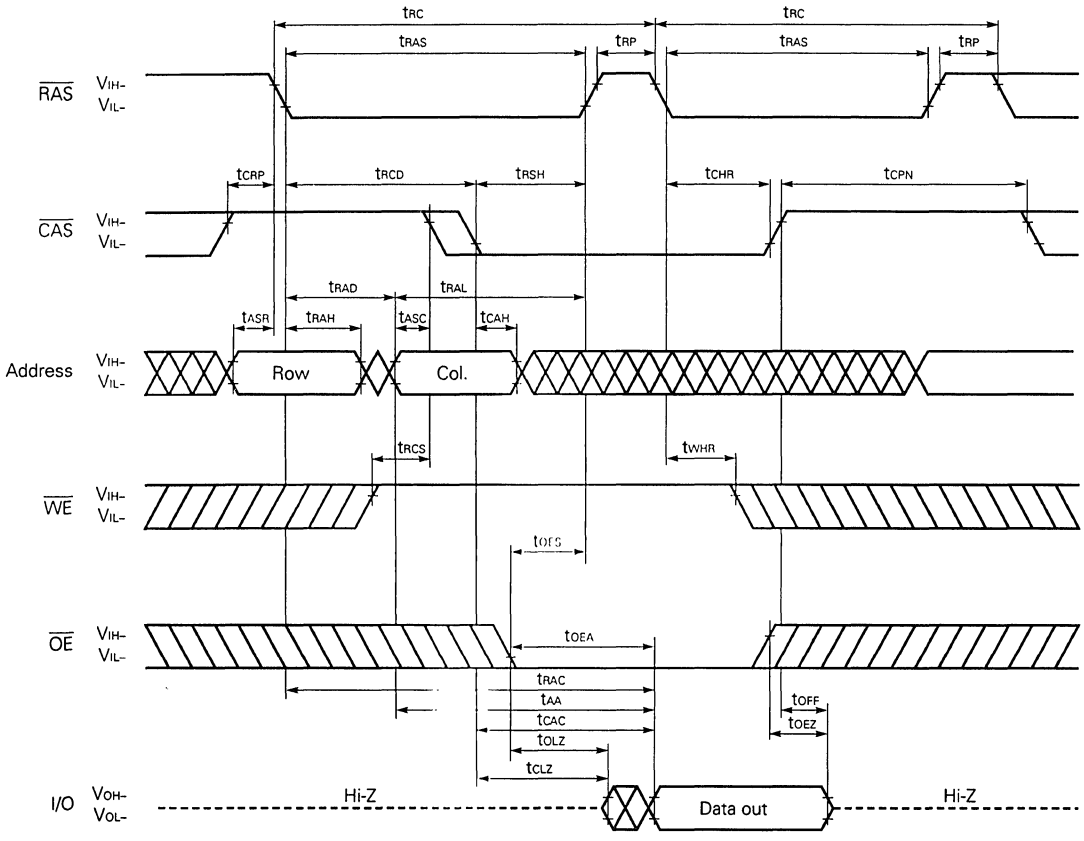
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

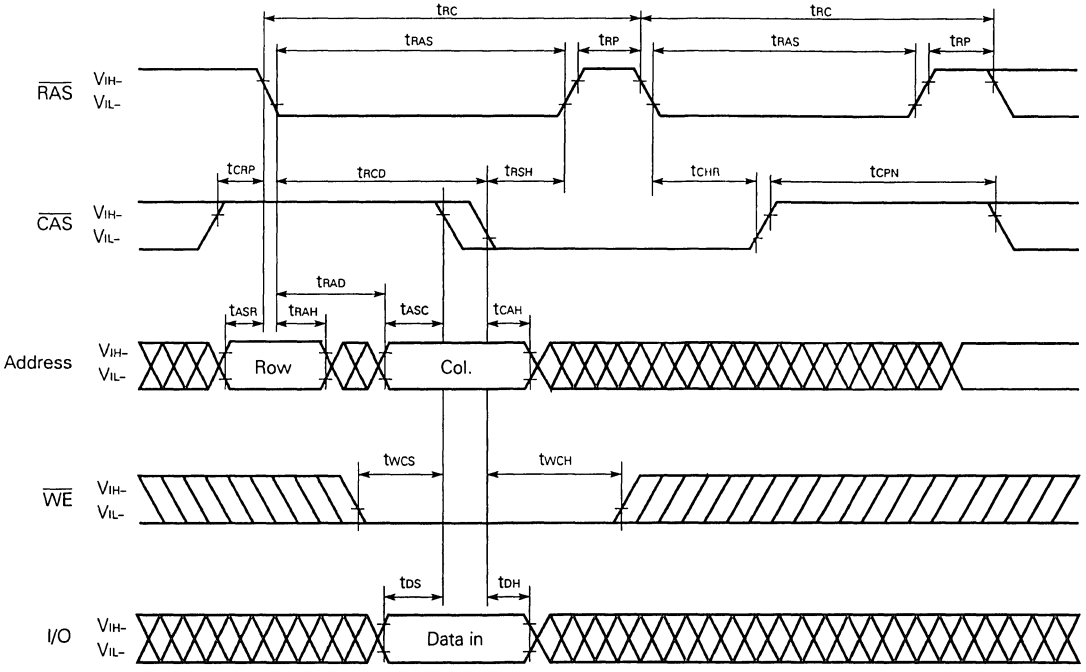


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



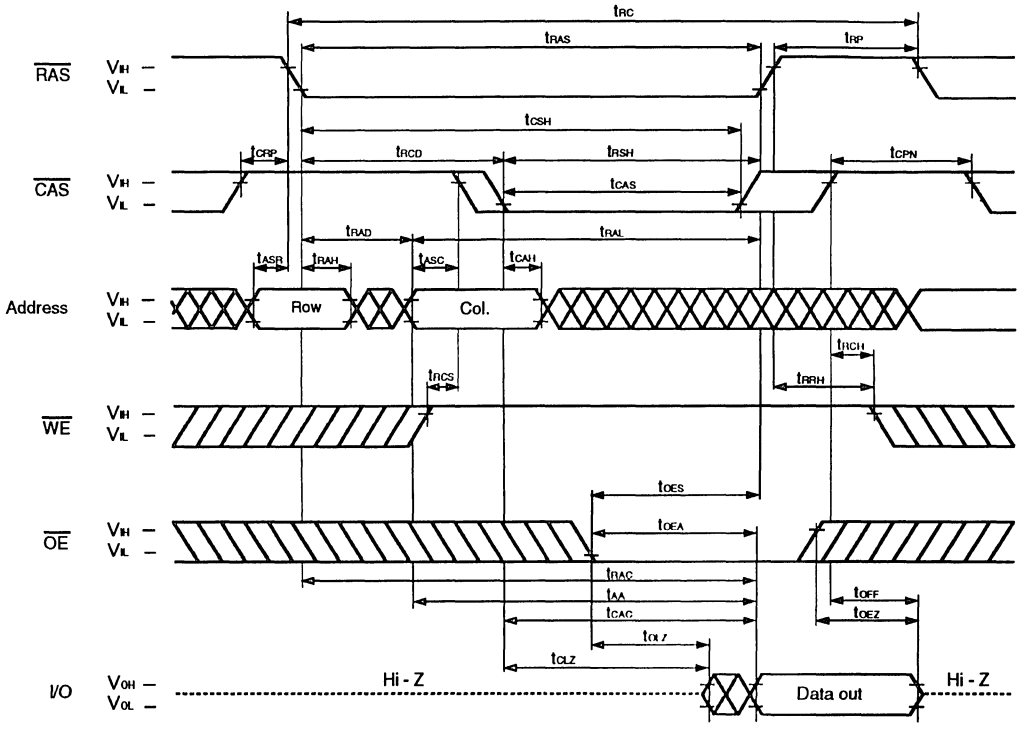
Hidden Refresh Cycle (Write)



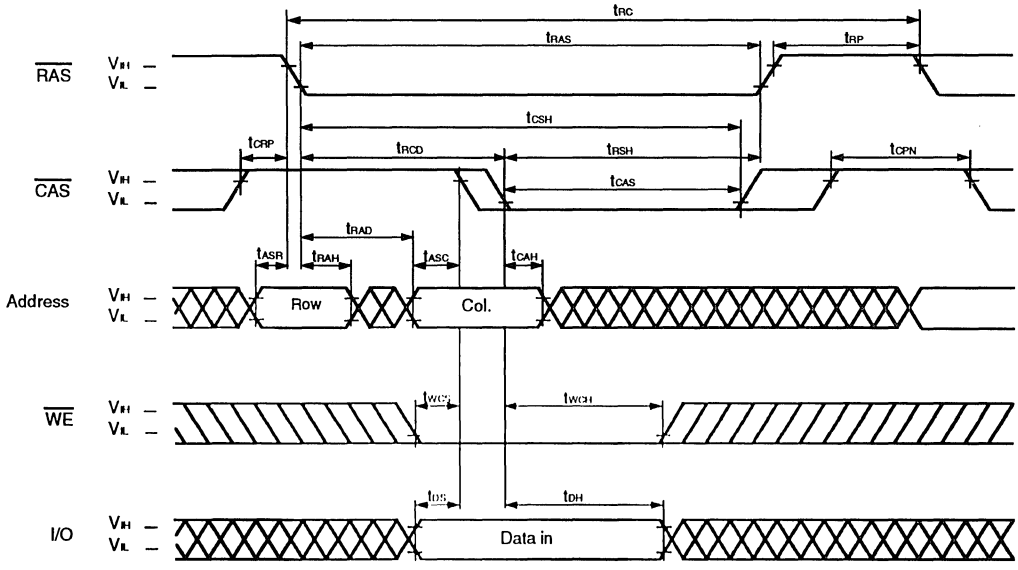
Remark $\overline{OE}$: Don't care

Timing Chart 8

Read Cycle

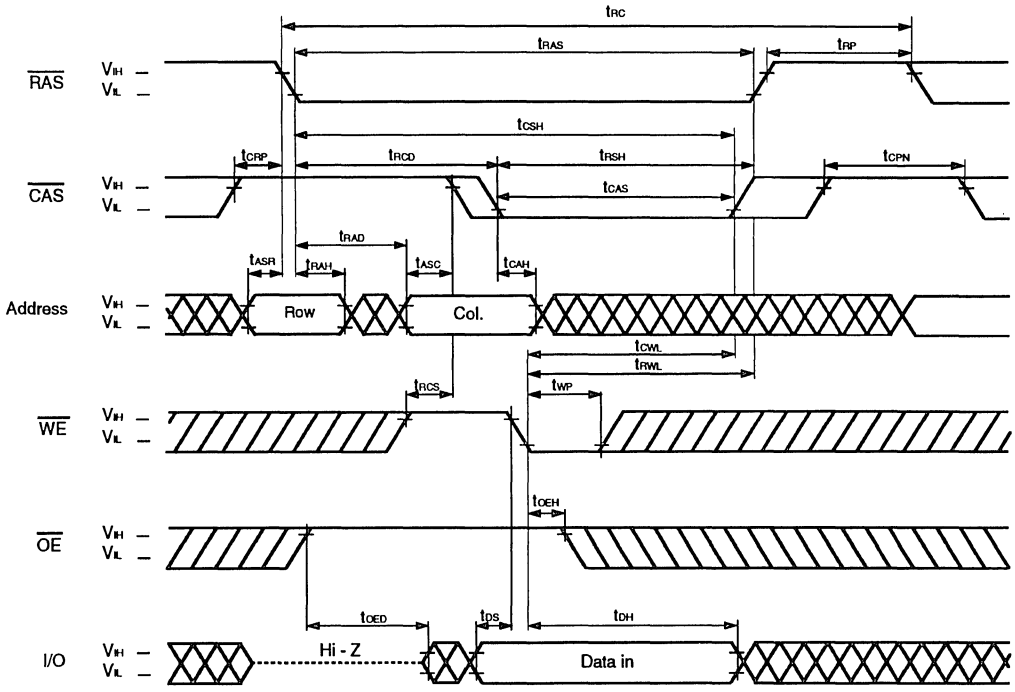

tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCS
tRCH
tRRH
WE
tOES
OE
tOEA
tRAC
tAA
tOFF
tOEZ
tCAC
tOLZ
tCLZ
I/O
VOH
VOL
Hi - Z
Data out
Hi - Z

Early Write Cycle

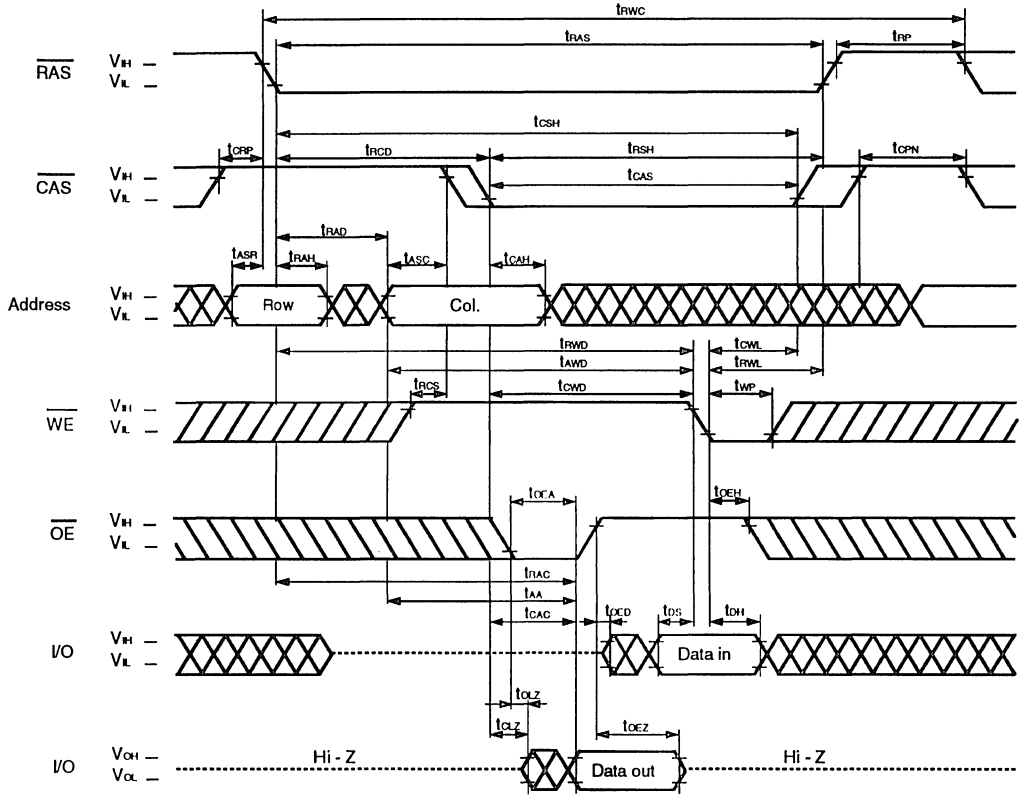


Remark $\overline{OE}$: Don't care

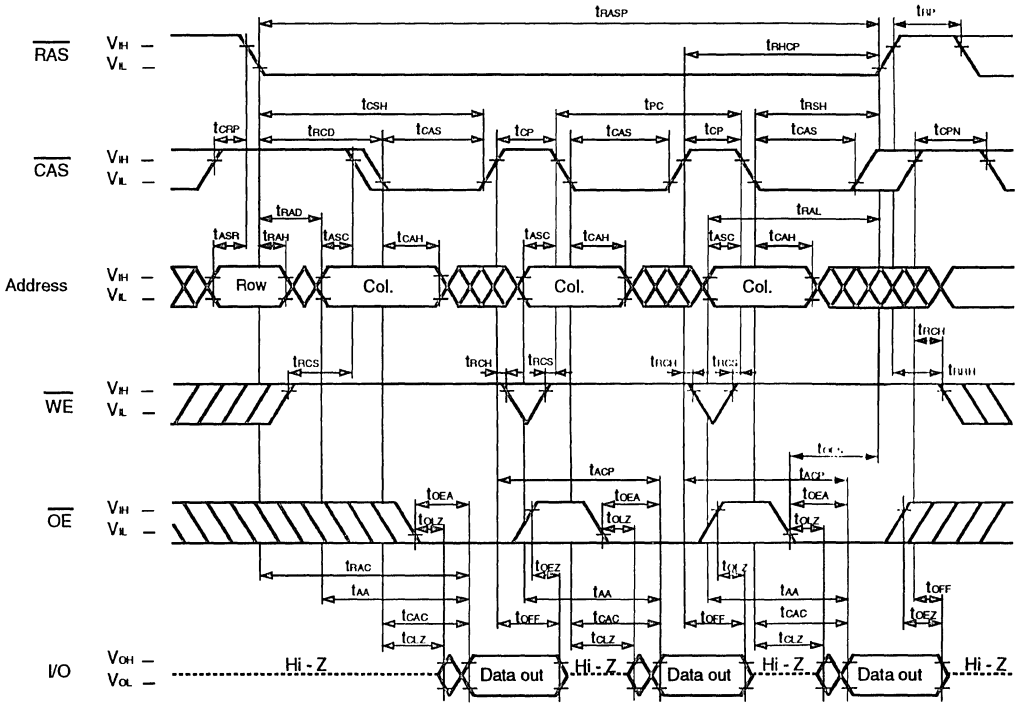
Late Write Cycle



Read Modify Write Cycle

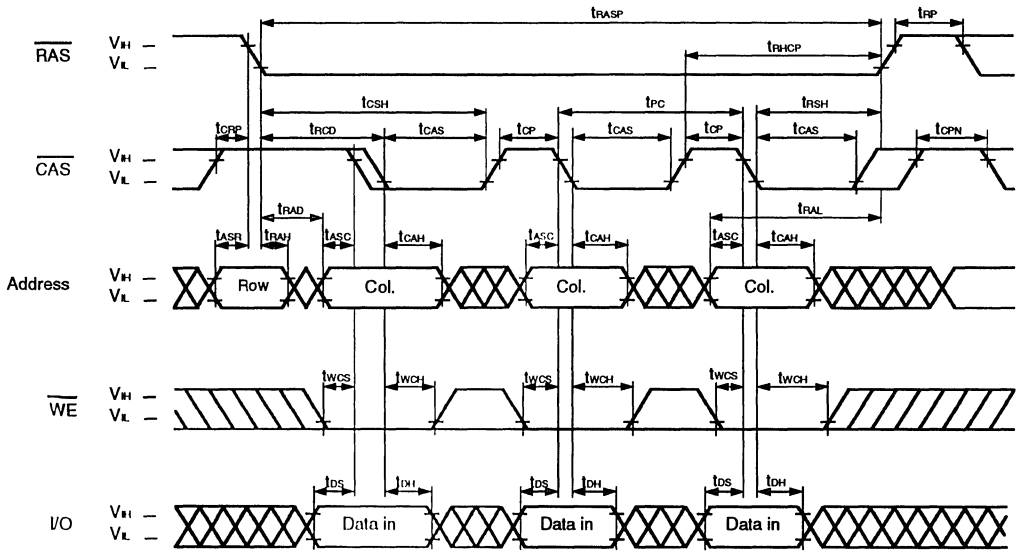


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

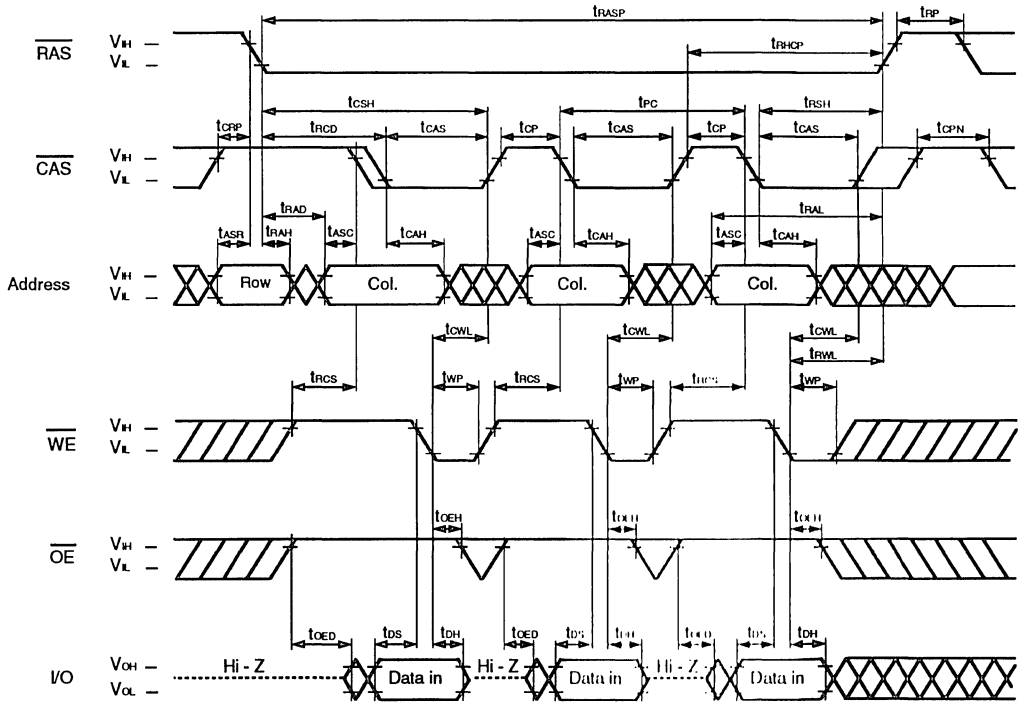
Fast Page Mode Early Write Cycle



Remark $\overline{OE}$: Don't care

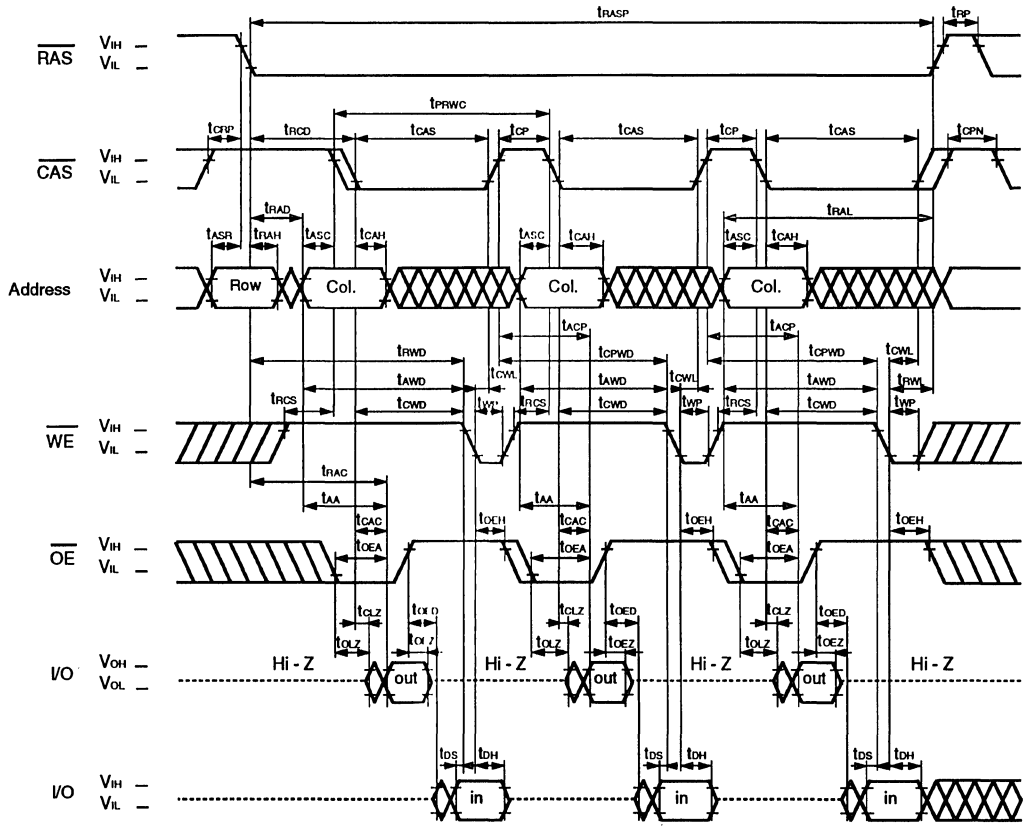
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



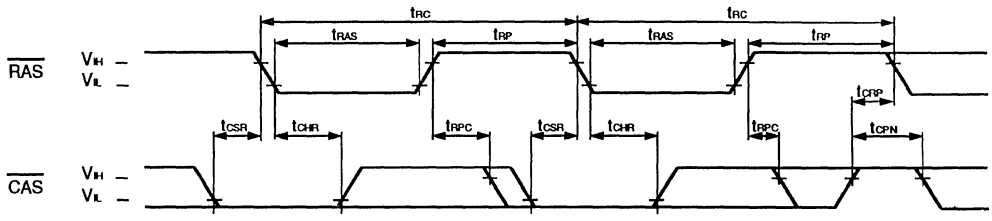
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



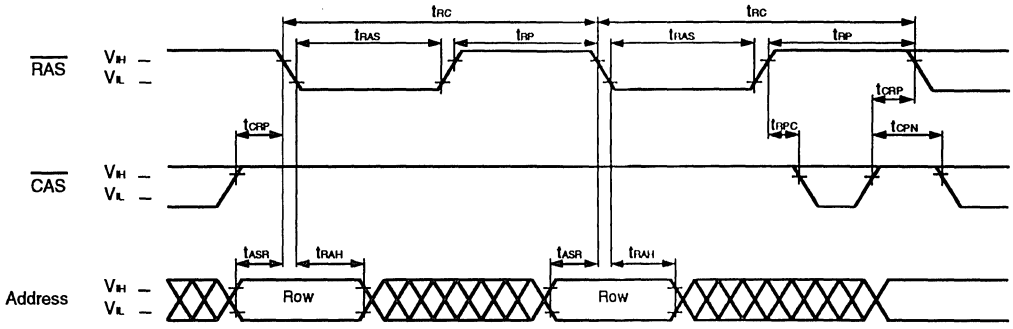
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



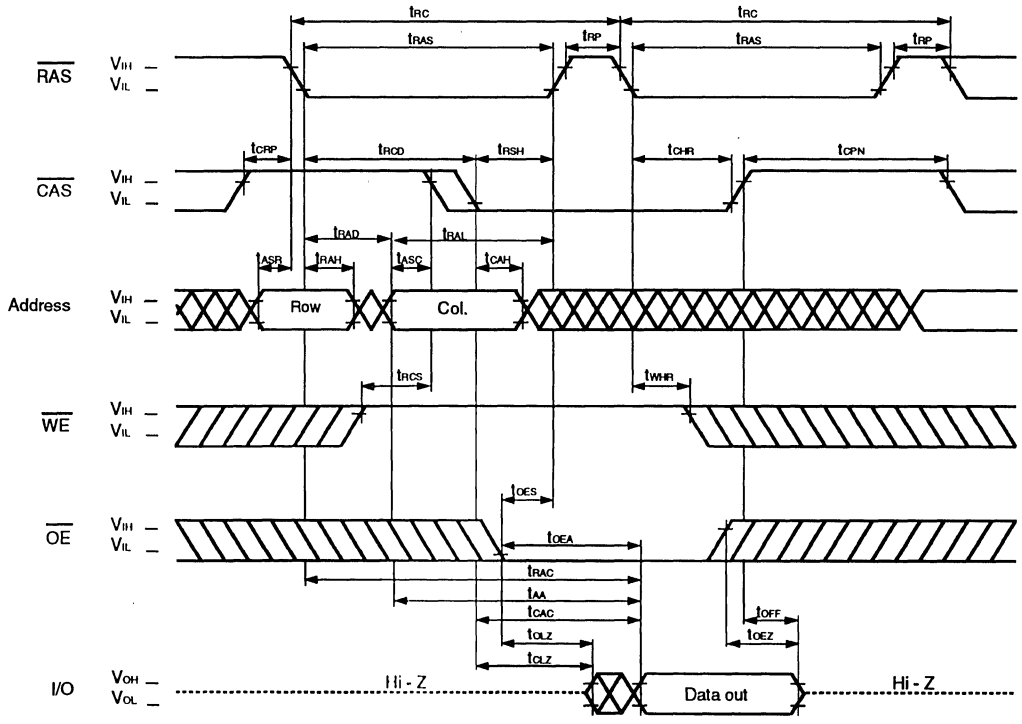
Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O : Hi - Z

$\overline{\text{RAS}}$ Only Refresh Cycle

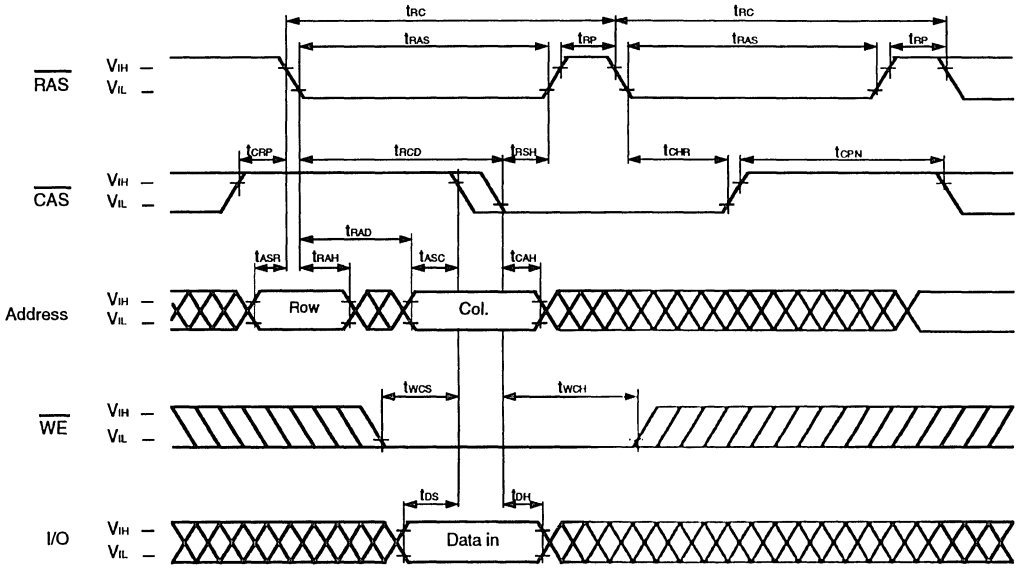


Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O : Hi - Z

Hidden Refresh Cycle (Read)



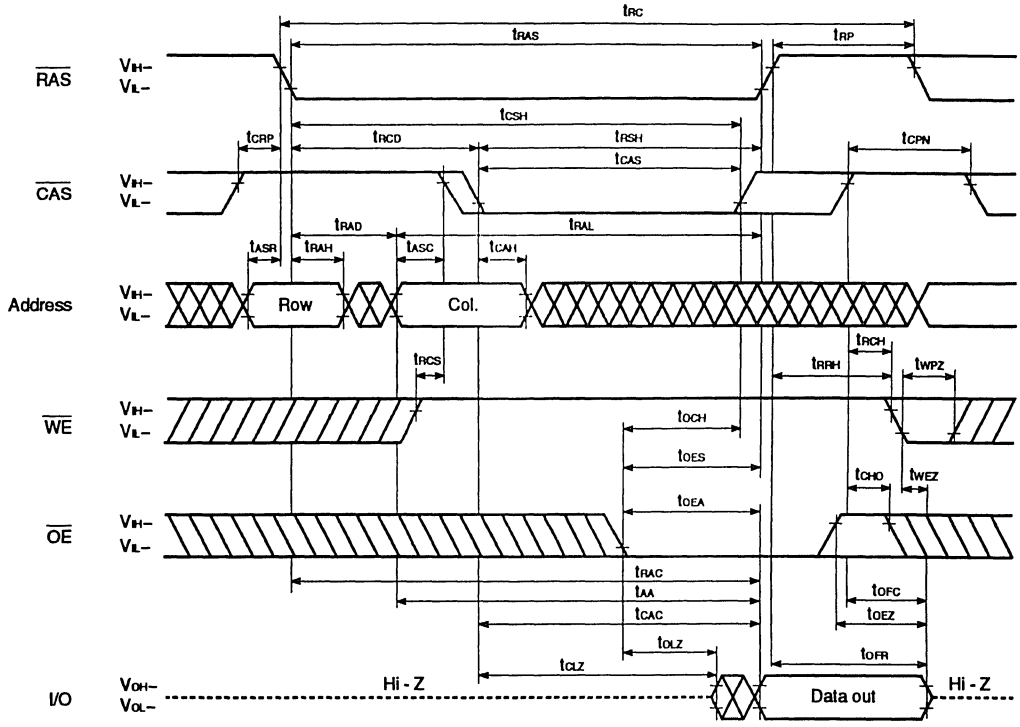
Hidden Refresh Cycle (Write)



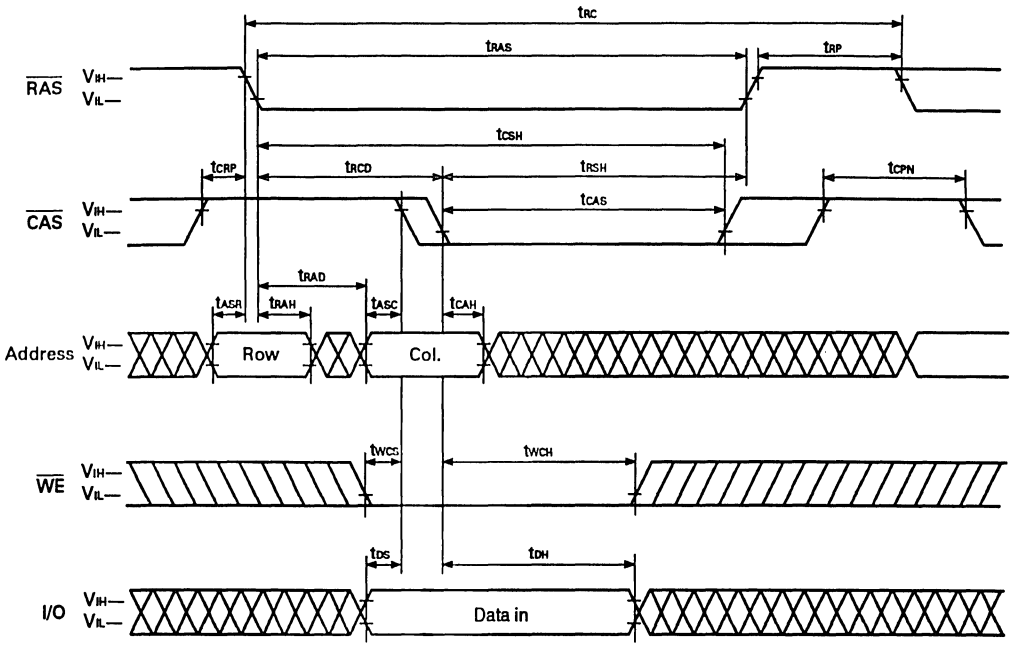
Remark OE : Don't care

Timing Chart 9

Read Cycle

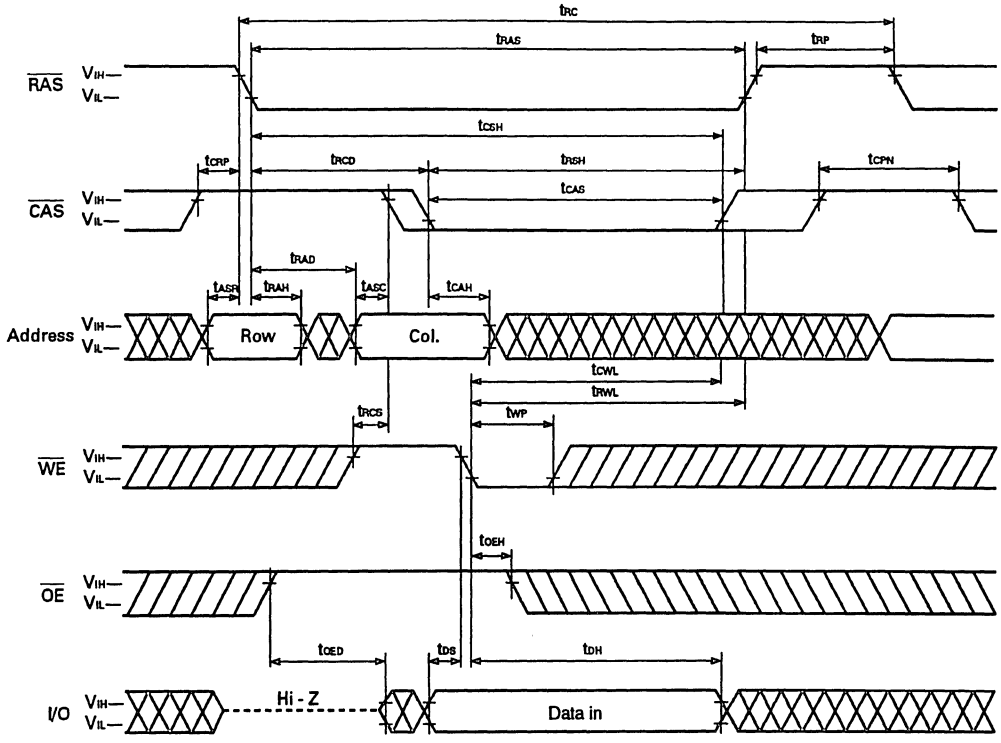

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRRH
tWPZ
tRCS
WE
tOCH
tOES
tCHD
tWEZ
tOEA
OE
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Early Write Cycle

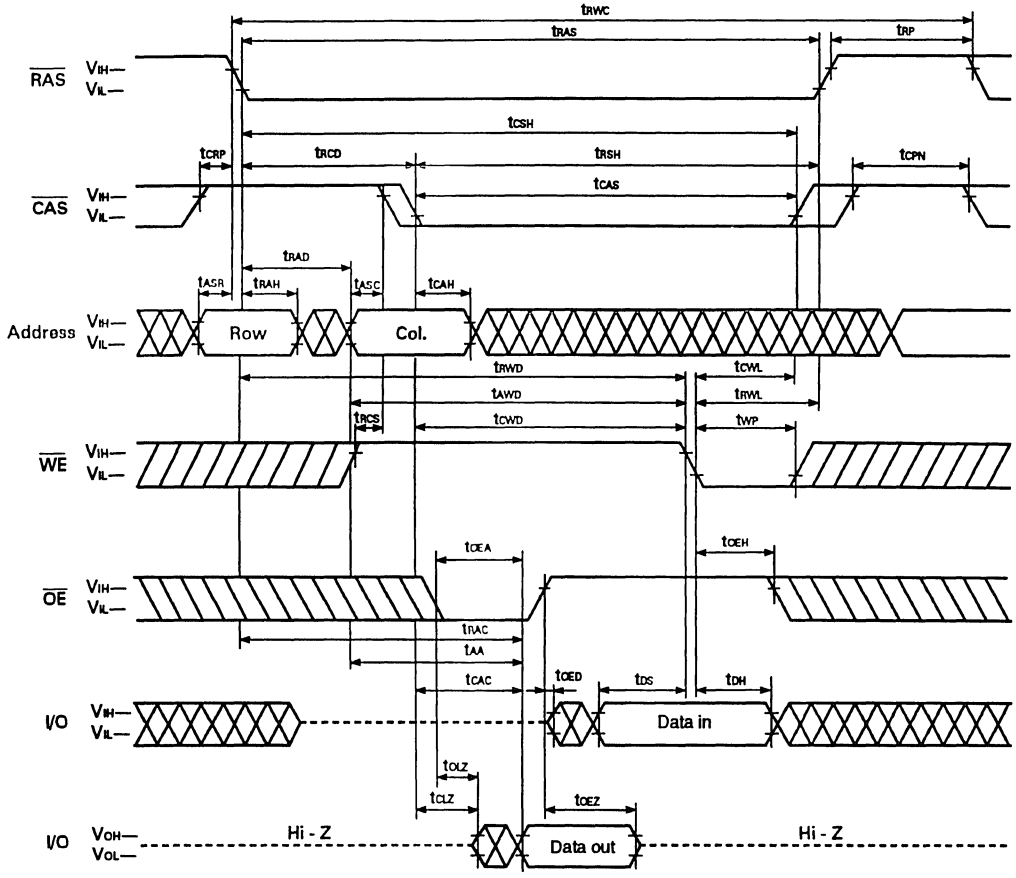


Remark $\overline{OE}$: Don't care

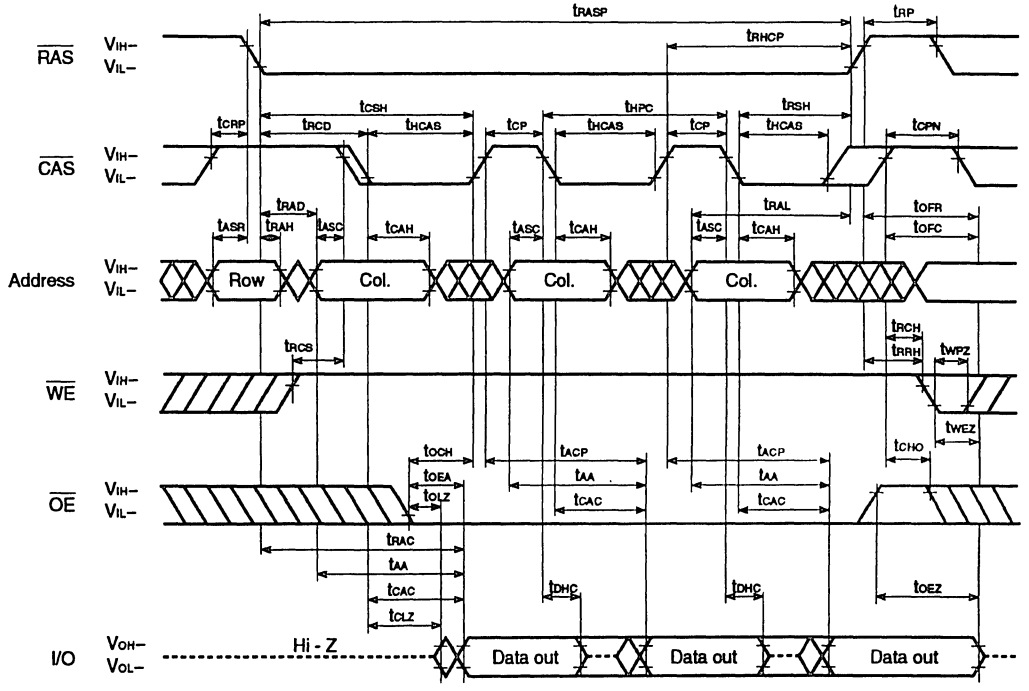
Late Write Cycle



Read Modify Write Cycle

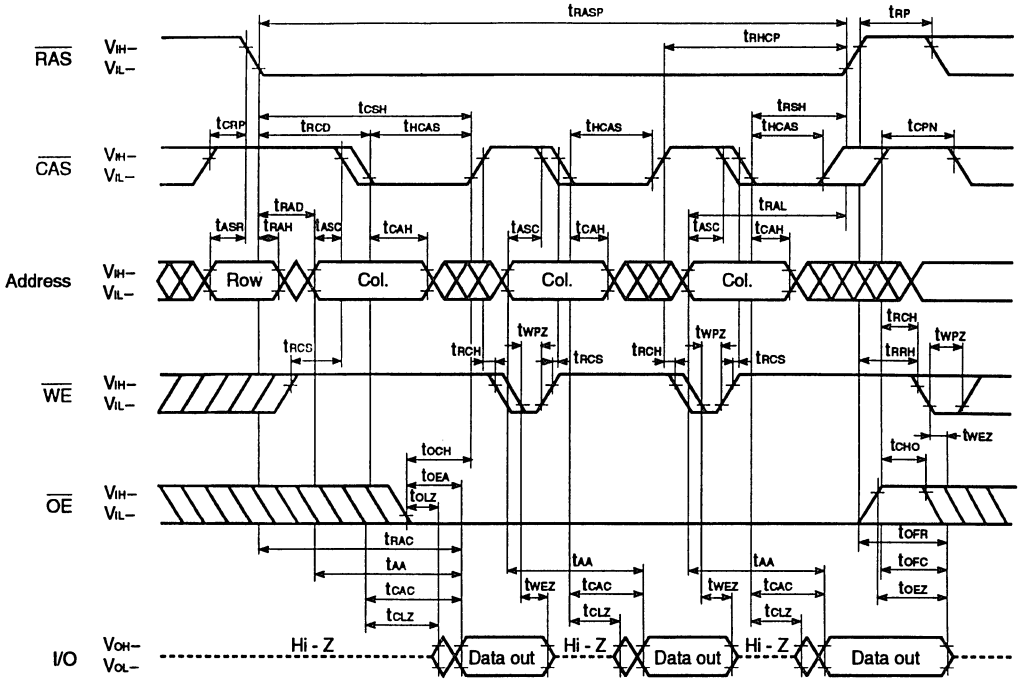


Hyper Page Mode Read Cycle



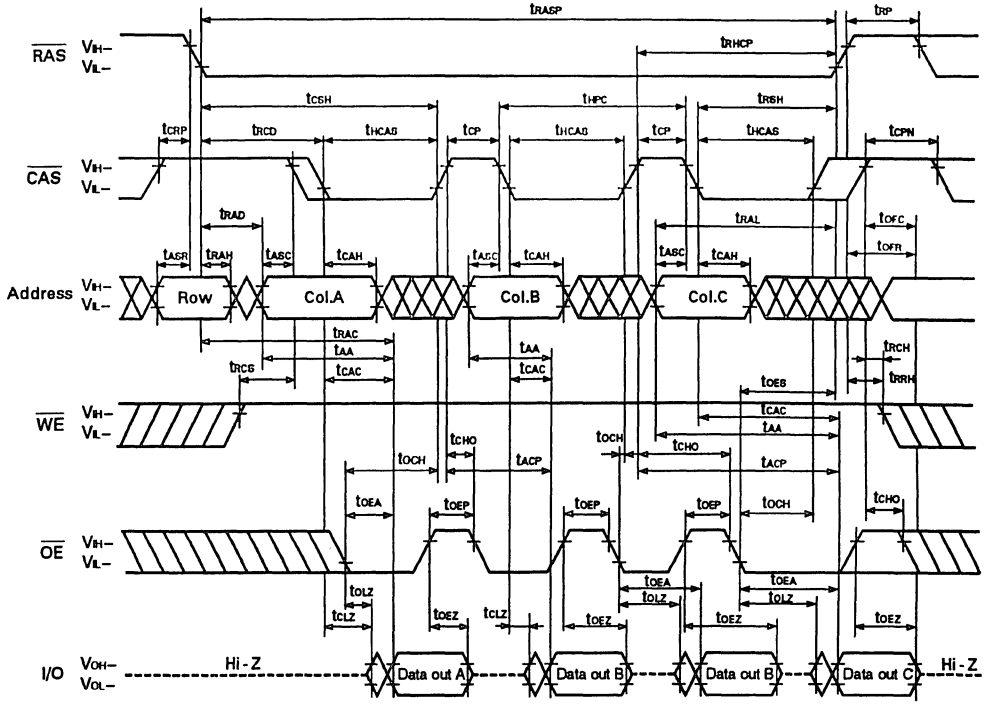
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{WE}$ Control)



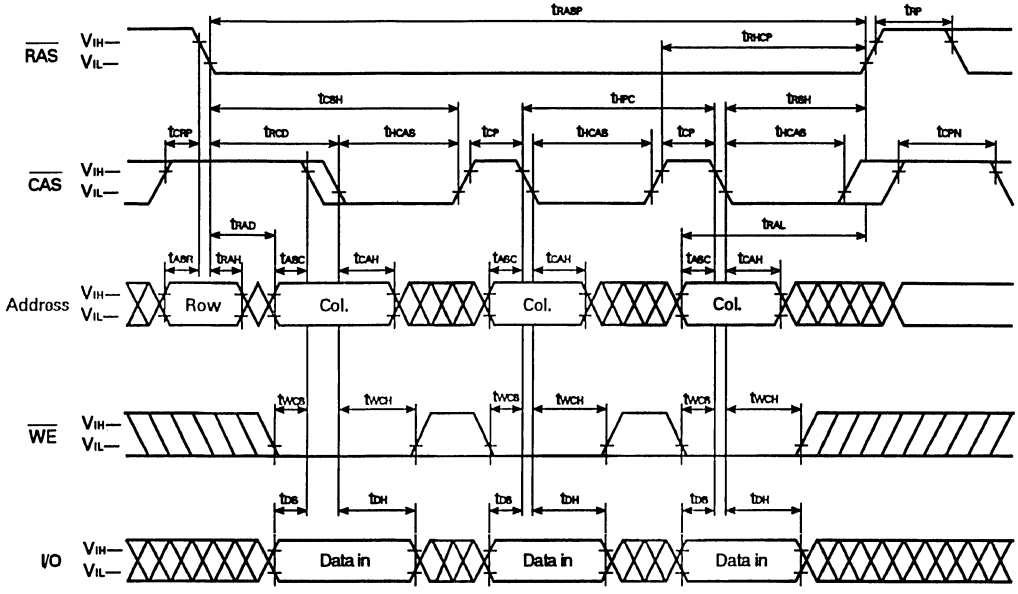
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

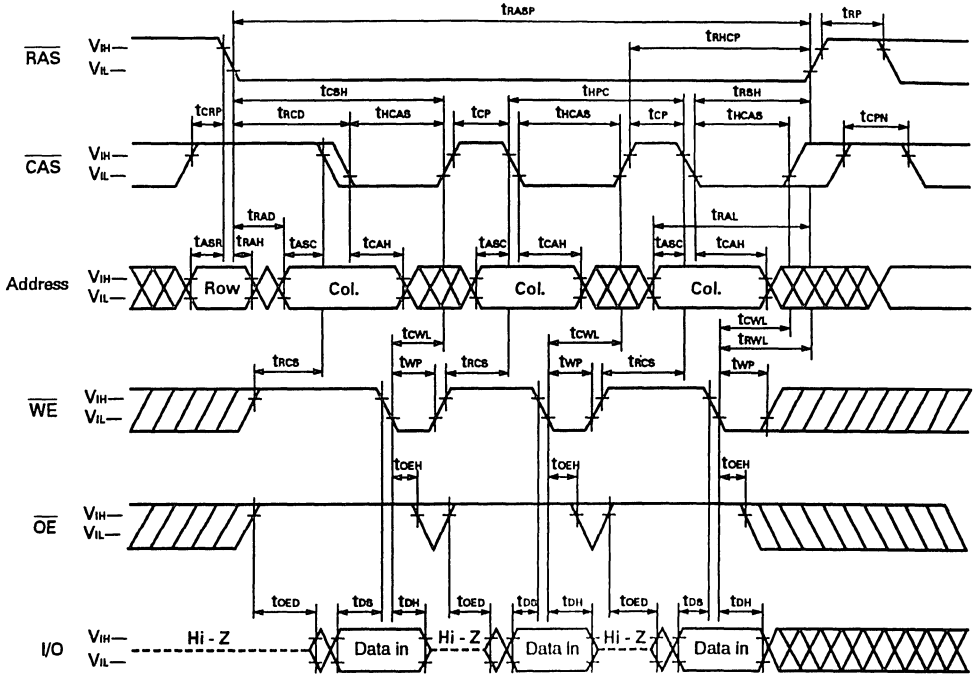
Hyper Page Mode Early Write Cycle



Remark 1. $\overline{OE}$: Don't care

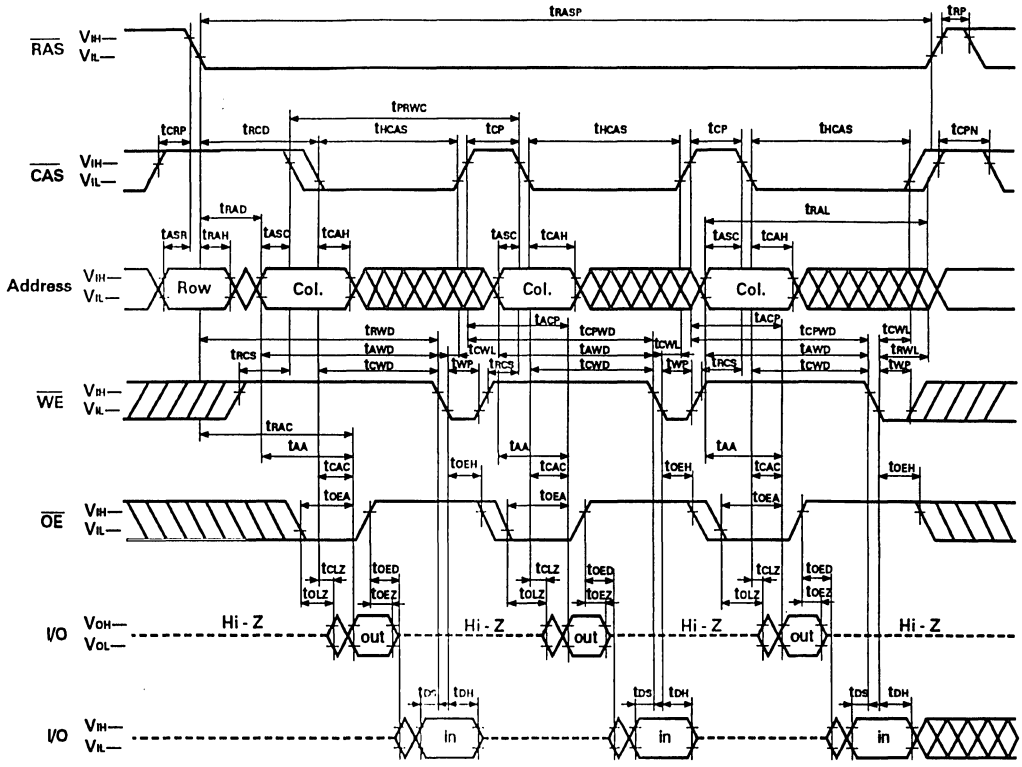
2. In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Late Write Cycle



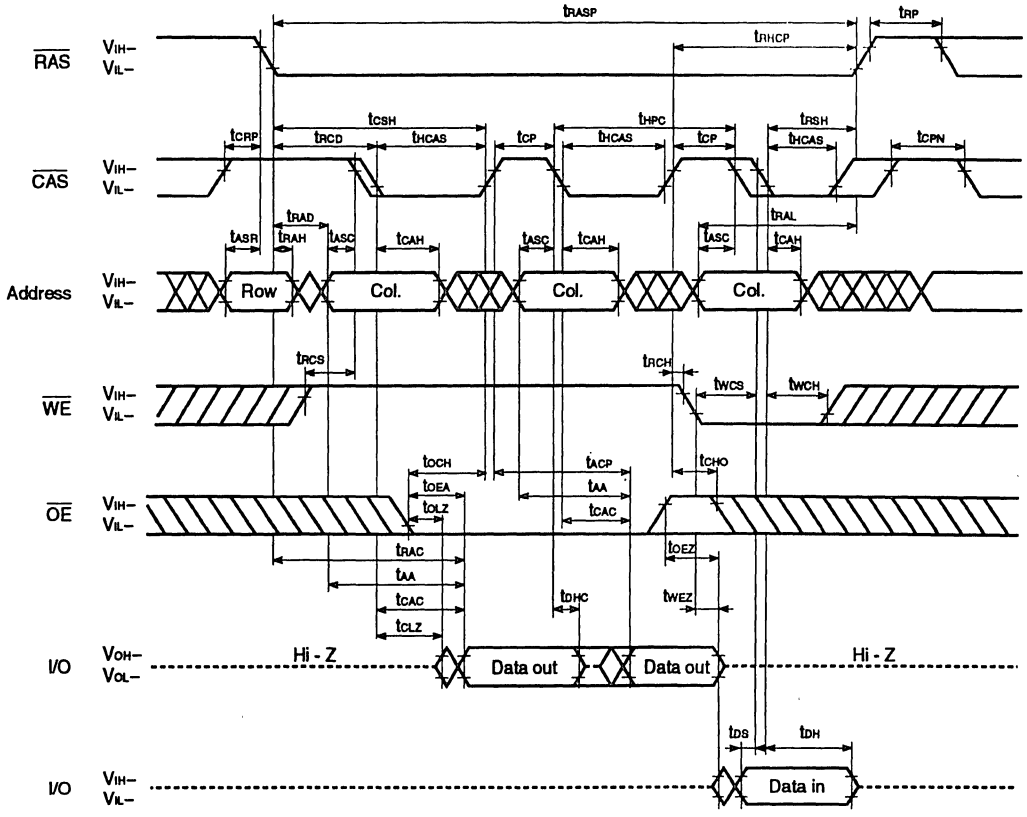
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Modify Write Cycle



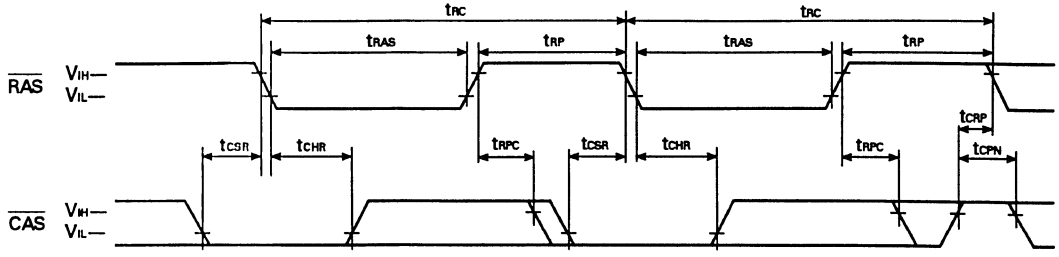
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read and Write Cycle



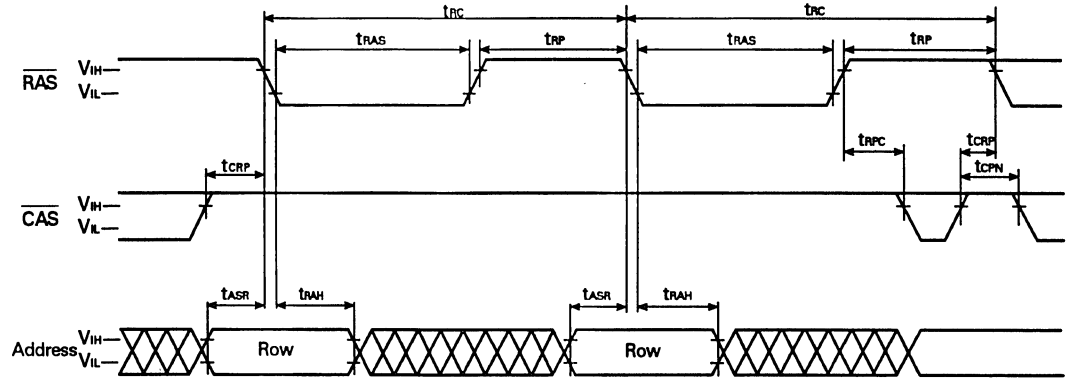
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



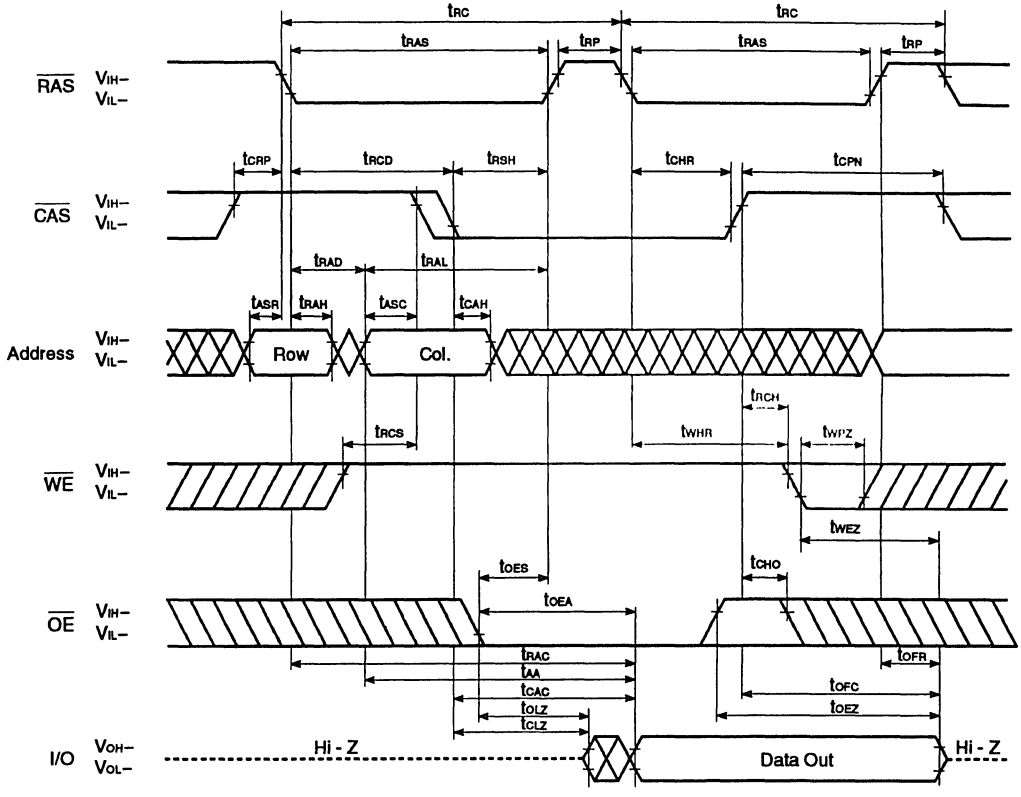
Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O : Hi-Z

$\overline{\text{RAS}}$ Only Refresh Cycle

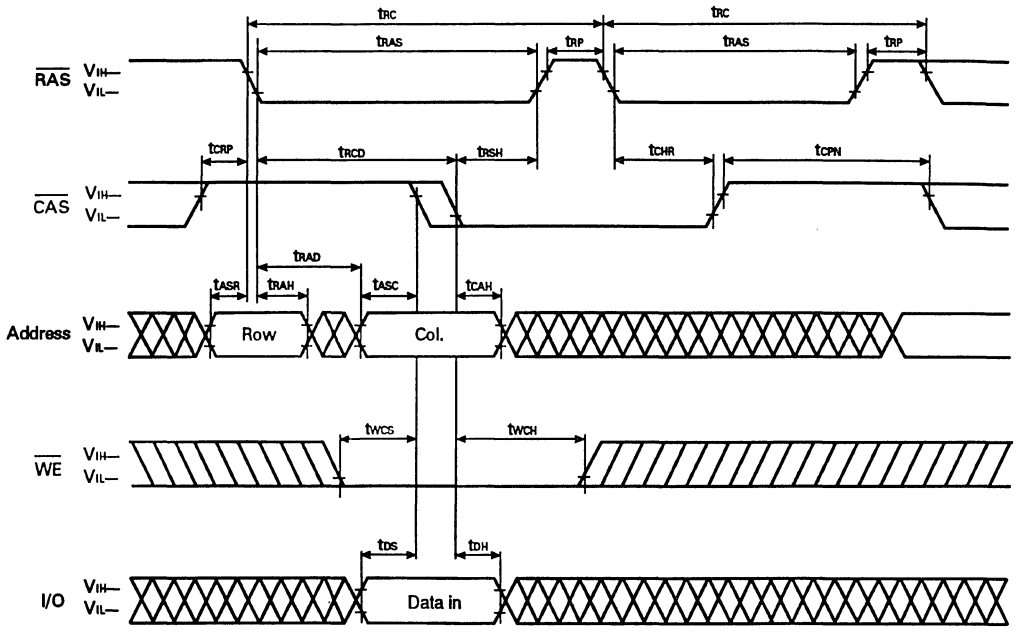


Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care I/O : Hi-Z

Hidden Refresh Cycle (Read)



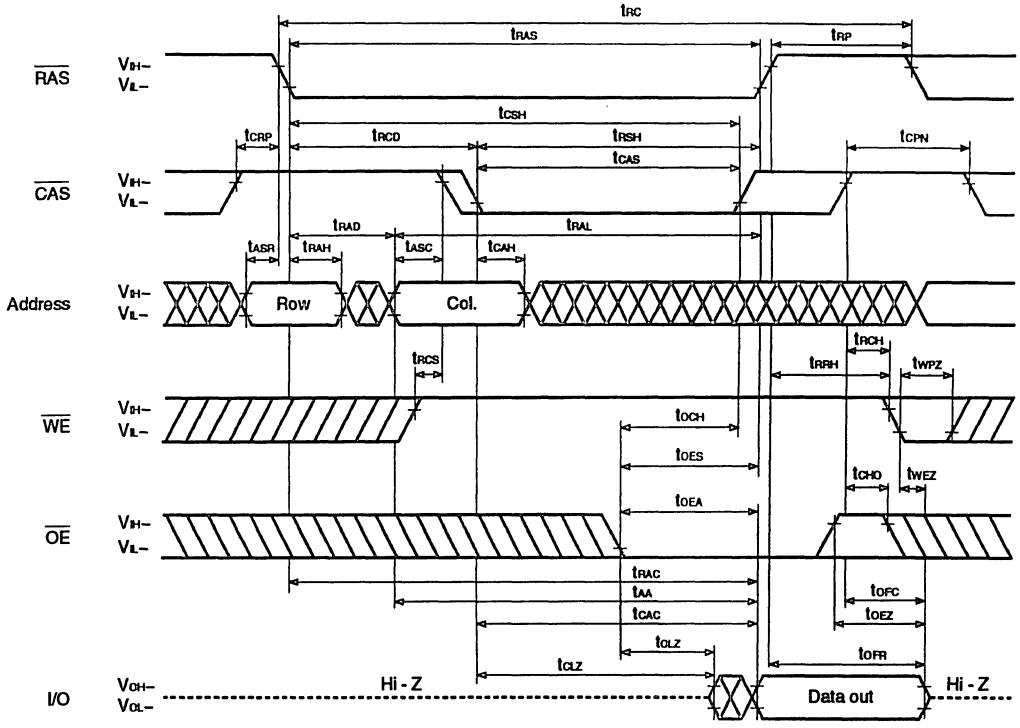
Hidden Refresh Cycle (Write)



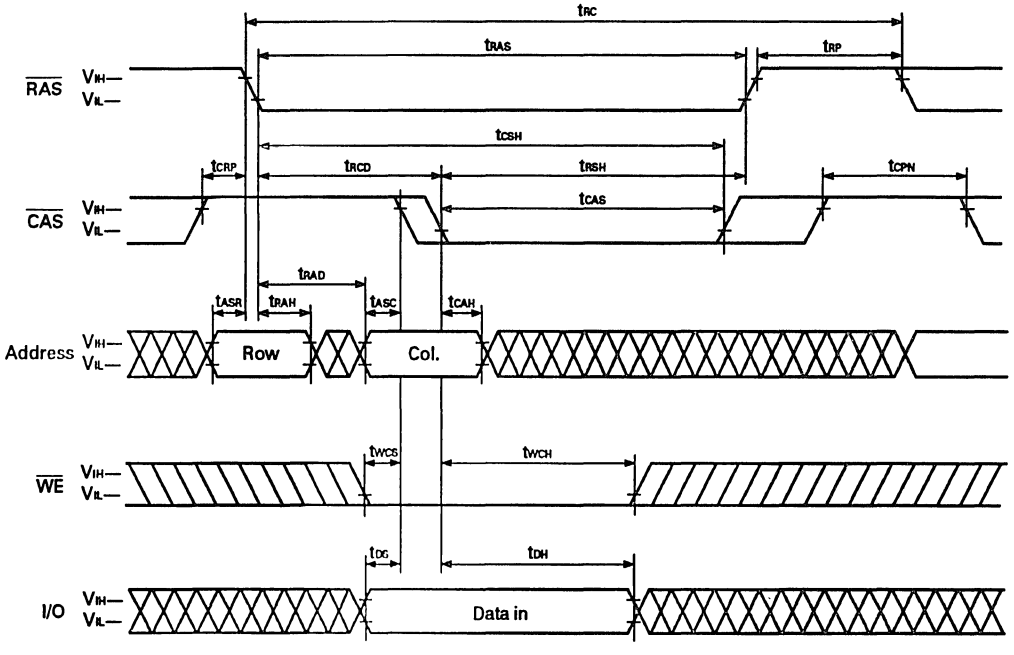
Remark $\overline{OE}$: Don't care

Timing Chart 10

Road Cycle

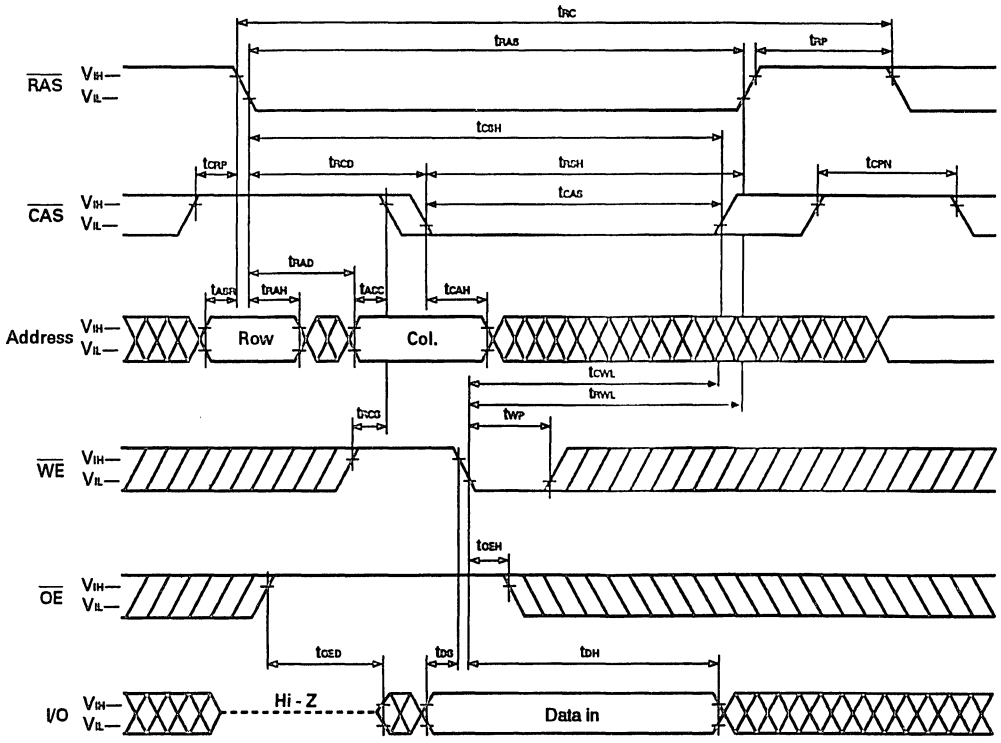

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCS
tRCH
tRRH
tWPZ
WE
tOCH
tOES
tCHD
tWEZ
tOEA
OE
tRAC
tAA
tCAC
tOFC
tOEZ
tCLZ
tOFR
tCLZ
I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Early Write Cycle

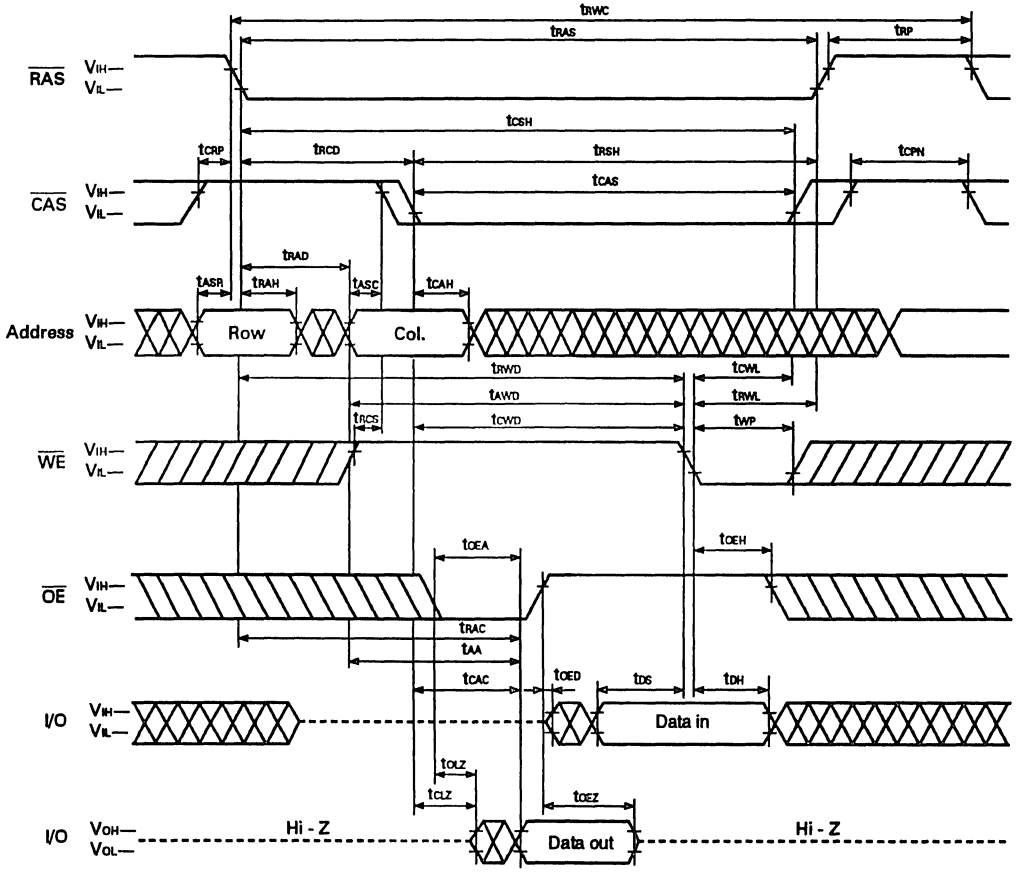


Remark $\overline{OE}$: Don't care

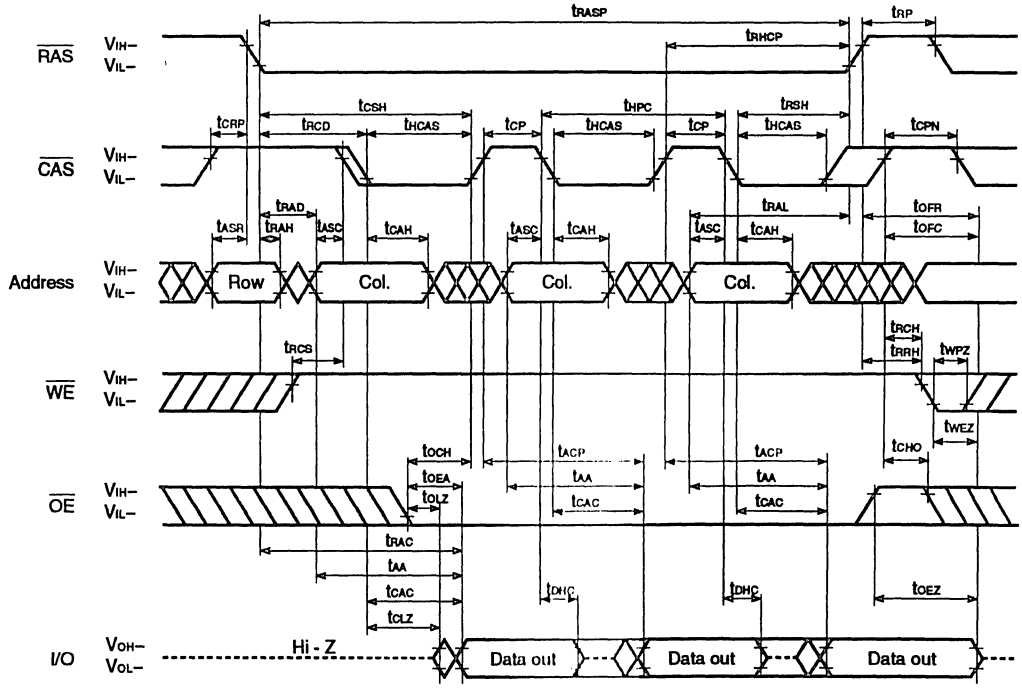
Late Write Cycle



Read Modify Write Cycle

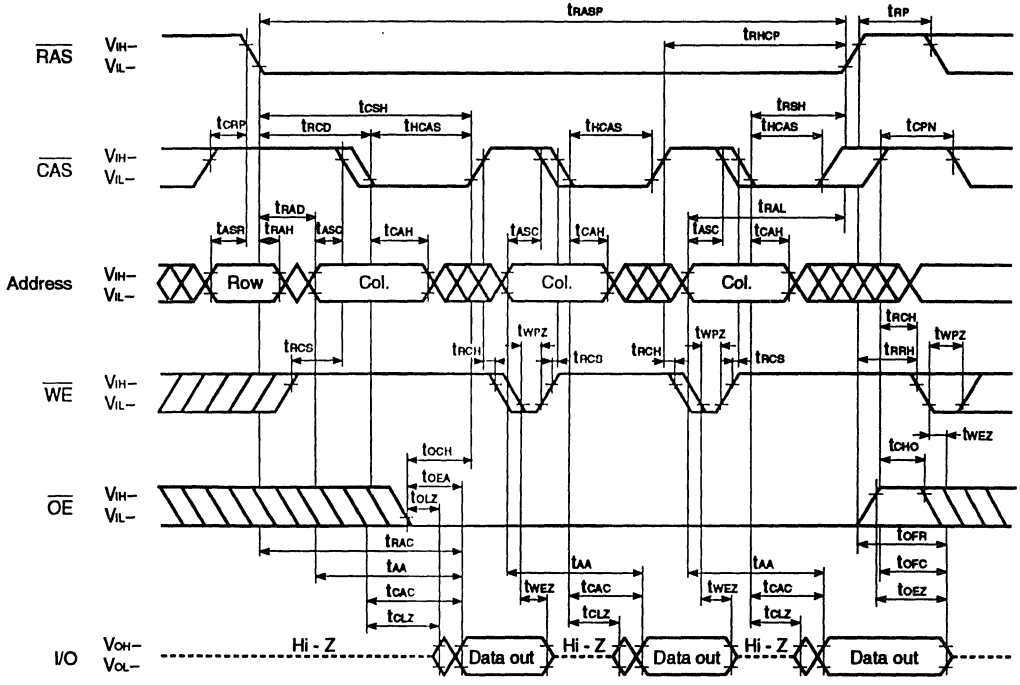


Hyper Page Mode Read Cycle



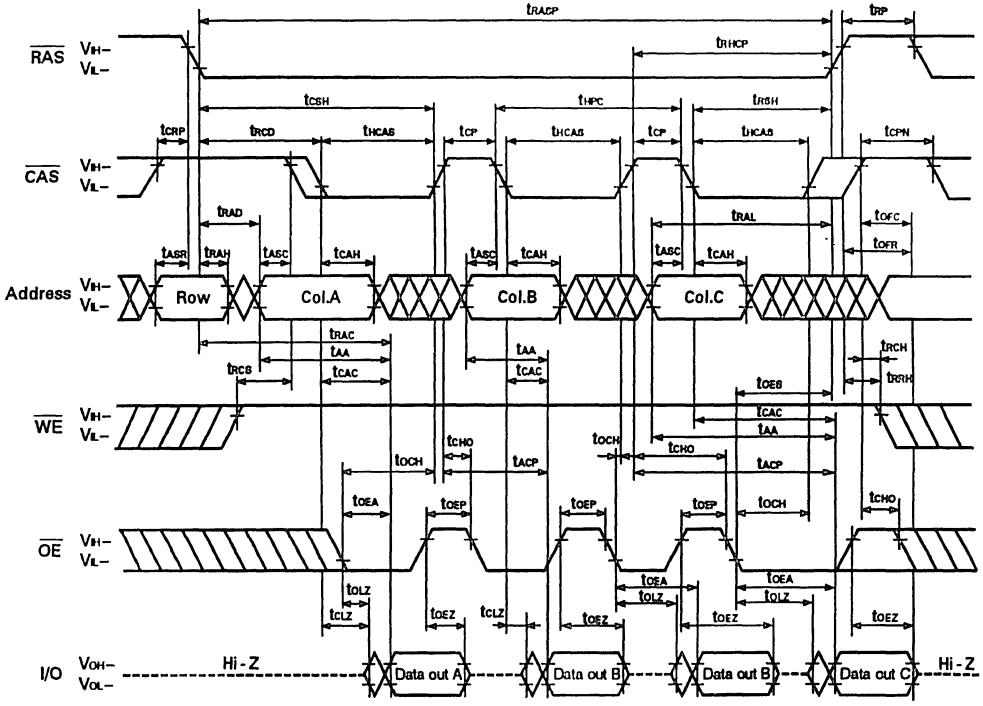
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{WE}$ Control)



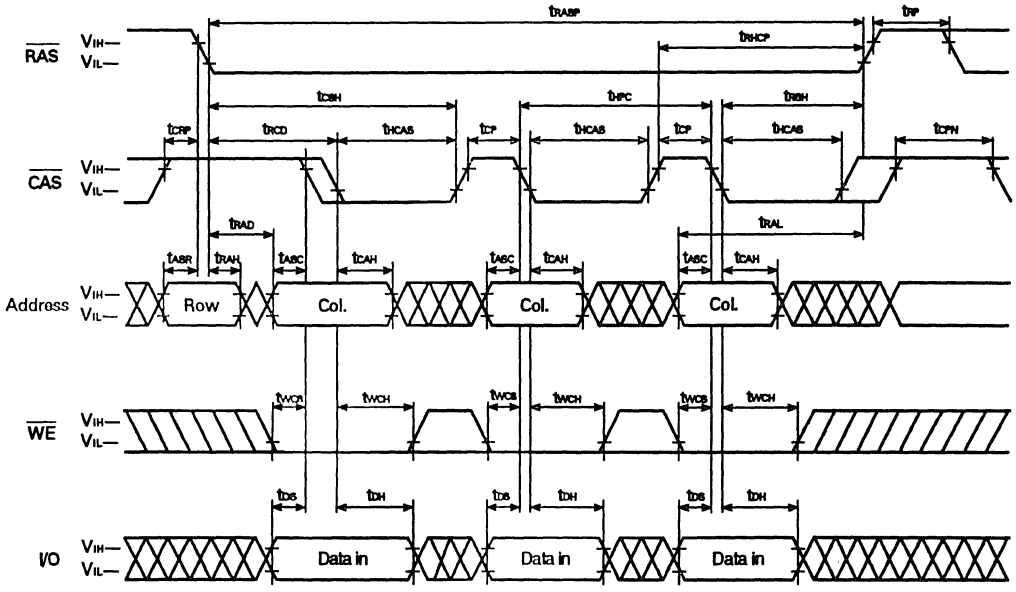
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

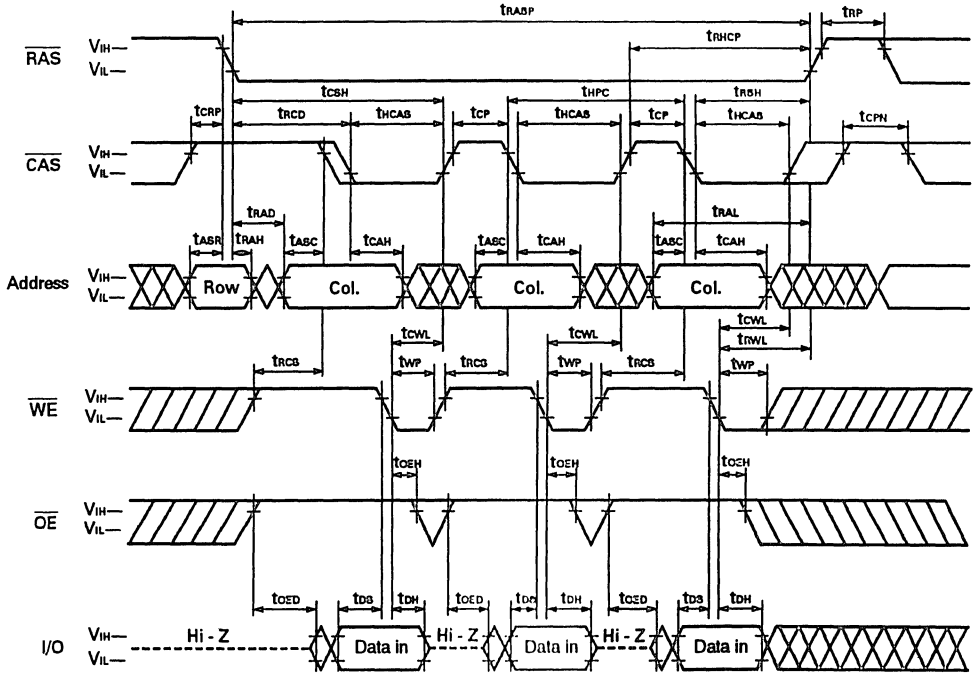
Hyper Page Mode Early Write Cycle



Remark 1. $\overline{OE}$: Don't care

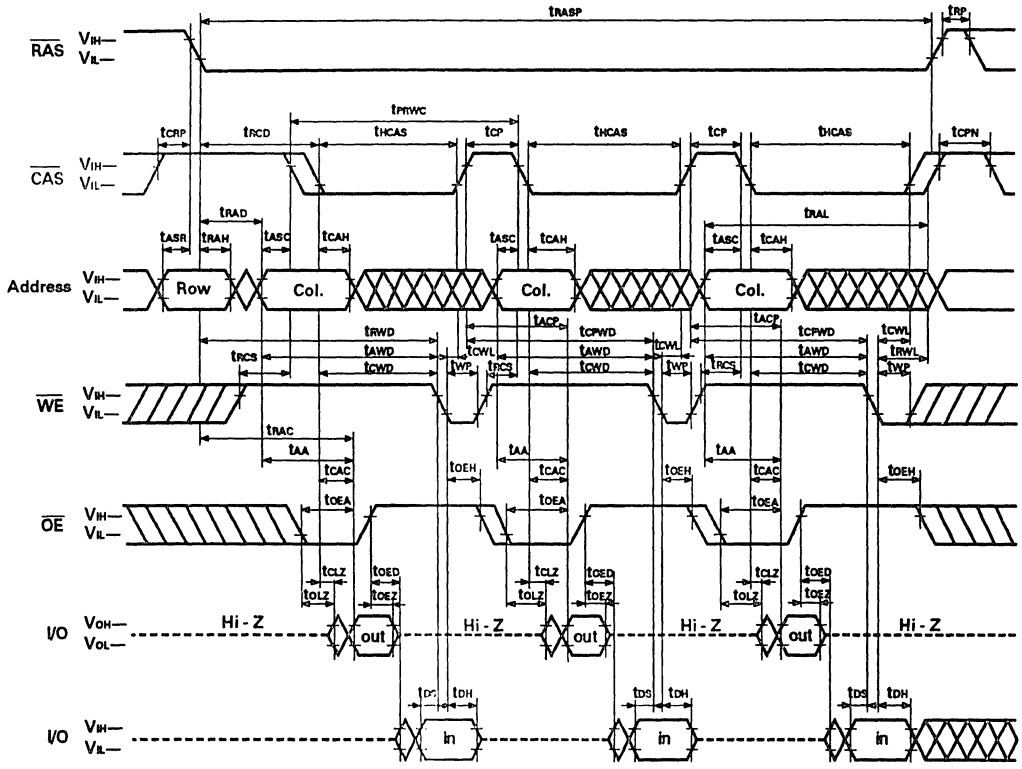
2. In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hypor Pago Mode Late Writo Cyclo



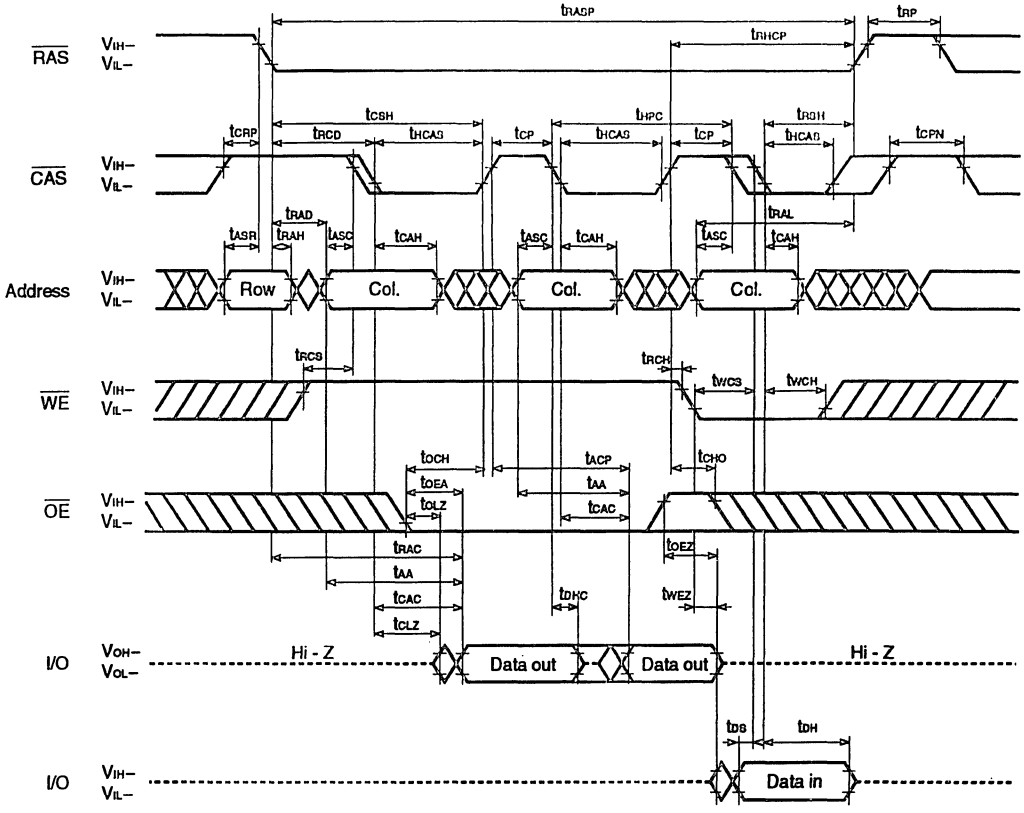
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Modify Write Cycle



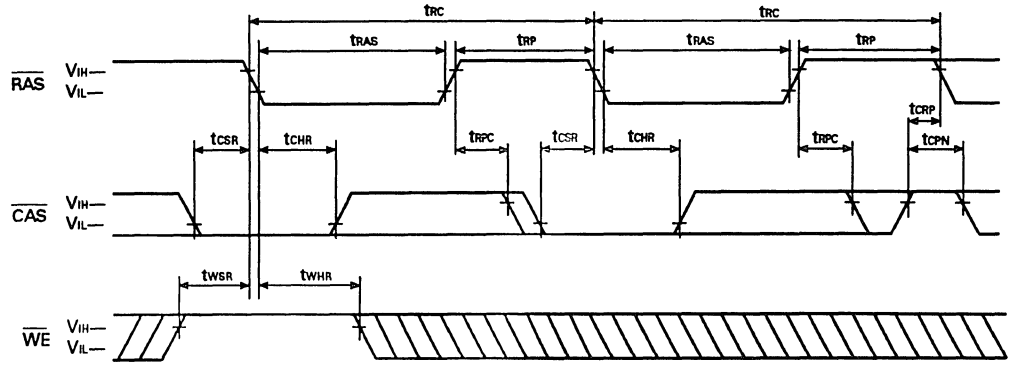
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read and Write Cycle



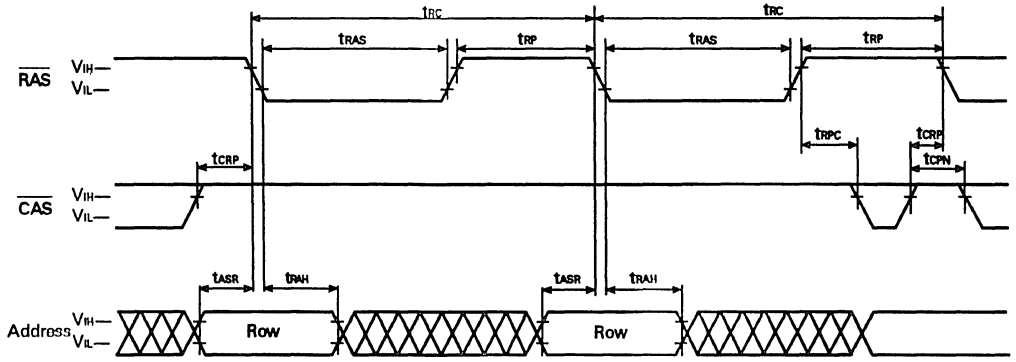
Remark In the hyper page mode, read,write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



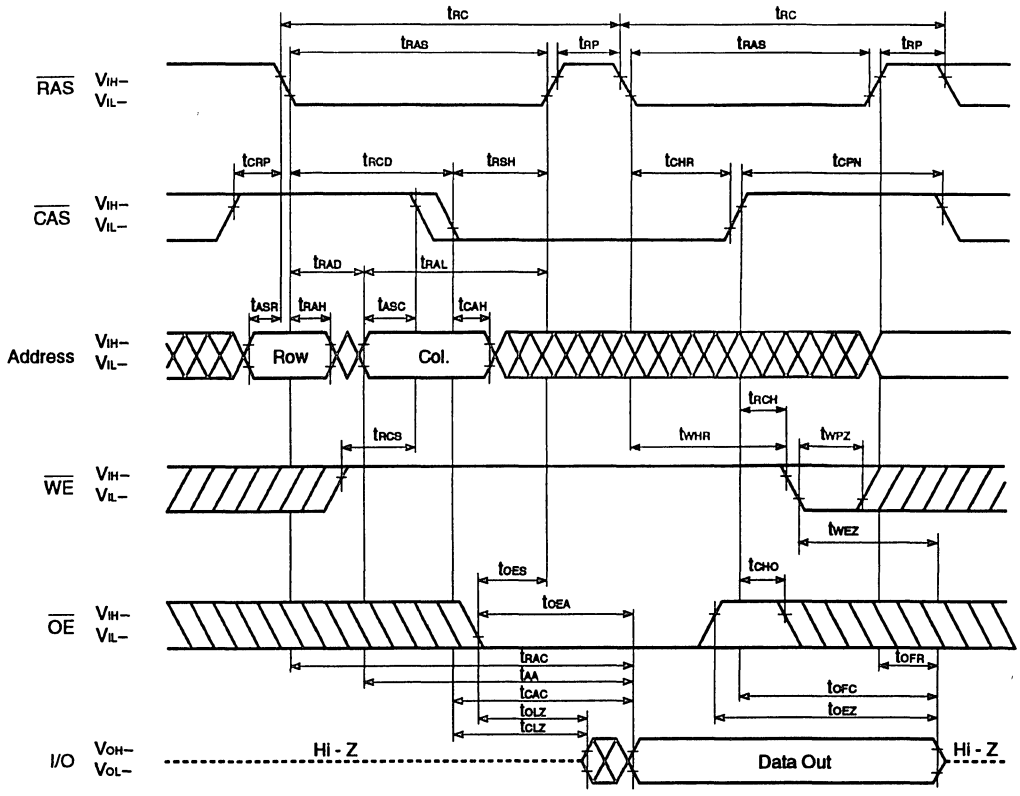
Remark 1. Address, $\overline{OE}$: Don't care
2. I/O : Hi-Z

$\overline{RAS}$ Only Refresh Cycle

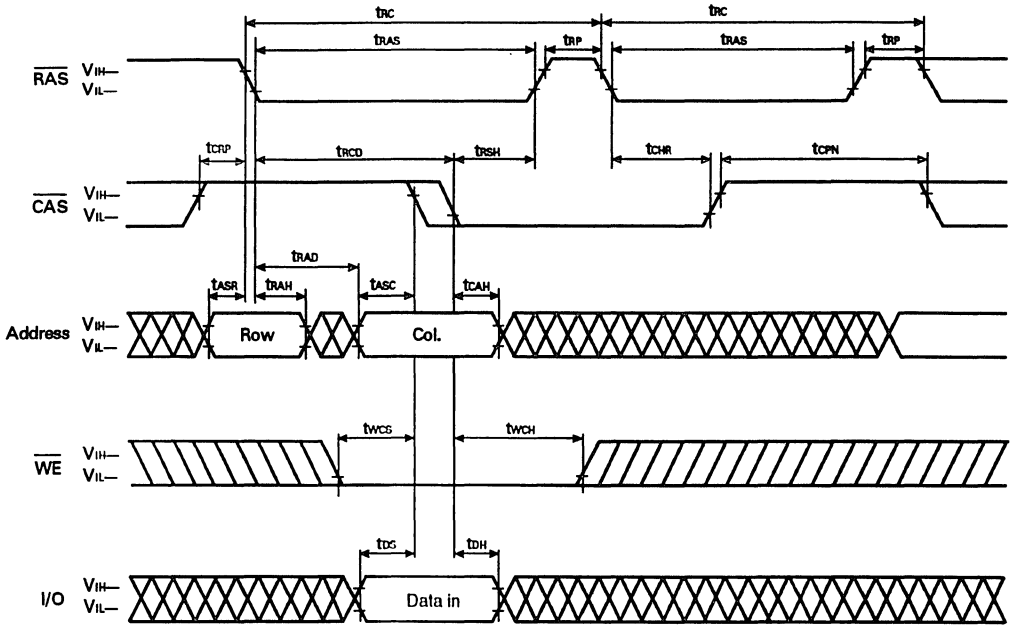


Remark 1. $\overline{OE}$: Don't care
2. I/O : Hi-Z

Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

NEC

NEC Electronics Inc.

Corporate Headquarters
475 Ellis Street
Mountain View, CA 94043
Telephone: 415-960-6000
Fax: 415-965-6130

New Corporate Headquarters
(Spring 1996)
2880 Scott Blvd.
Santa Clara, CA 95050

For literature, call toll-free 8 a.m. to 4 p.m., Pacific time: 1-800-366-9782

Doc. No. M10584EJ1V0DBU1