OPTi®

82C852

16-Bit PC Card Controller

Preliminary Data Book

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OPTi Inc.
888 Tasman Drive
Milpitas, CA 95035
Tel: (408) 486-8000
Fax: (408) 486-8001
WWW: http://www.opti.com/

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PCMCIA Controller

1.0 Features

- DMA and 3.3V card support
- Integrated DMA support - programmable to any channel
- Full IRQ selection
  - Select any of ten IRQs
- Licensed industry standard Intel® ’365 core
  - Core upgraded for full PC Card 95 compliance
- “Compact ISA” reduces pin count, eliminates ISA conflicts
- Low cost single slot controller
- Packaged in 100-pin TQFP (Thin Quad Flat Pack)

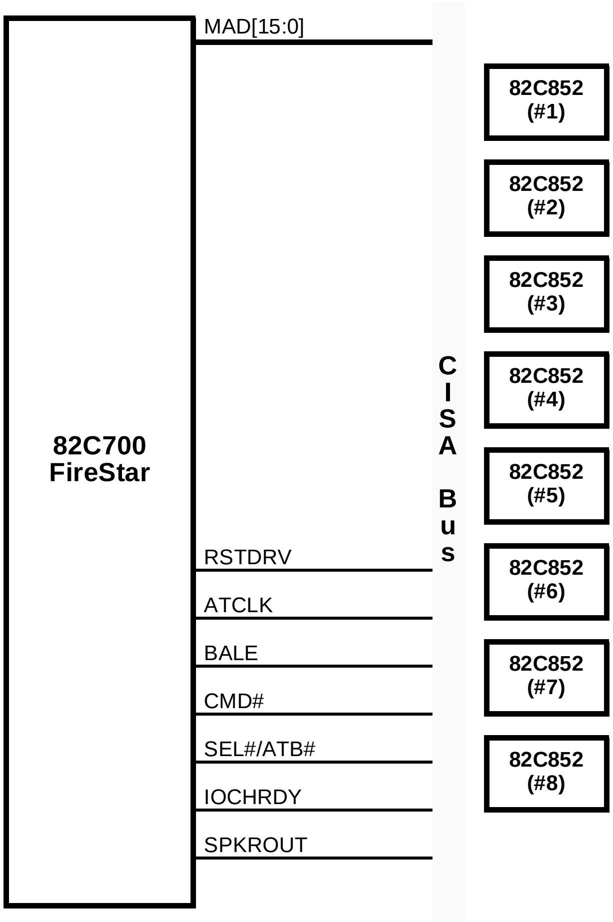
2.0 Overview

This data book describes a new OPTi interface chipset, the 82C852 PCMCIA Controller, that provides a single, fully compliant PCMCIA interface in a very compact form factor. The PCMCIA interface is handled in a straightforward manner using a modified Intel 82365SL PCMCIA core.

Throughout this data book, the term “R2” is used to indicate that the 82C852 part implements a Rev. 2.x compliant PCMCIA slot. The 82C852 logic also incorporates the additional features needed to bring the interface to “PC Card 95” standards (DMA and 3.3V support).

The OPTi 82C852 PCMCIA Controller is based on an OPTi standard called Compact ISA (CISA). The CISA interface is derived from ISA, but uses a proprietary scheme to reduce the required number of interface pins from 80 to 23. The CISA interface is described in the “Compact ISA Specification” appendix to this document.

Figure 2-1 82C852 Interface with FireStar



3.0 Signal Definitions

3.1 Terminology/Nomenclature Conventions

The “#” symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “#” is not present after the signal name, the signal is asserted when at the high voltage level.

The terms “assertion” and “negation” are used extensively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term “assert”, or “assertion” indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term “negate”, or “negation” indicates that a signal is inactive.

The 82C852 has some pins that have multiple functions (denoted by “+” in the pin name). These functions are either:

- cycle-multiplexed (always enabled and available when a particular cycle is in progress),
- a strap option (configured at reset),
- or selected via register programming.

The tables in this section use several common abbreviations. Table 3-1 lists the mnemonics and their meanings.

Table 3-1 Signal Definitions Legend

Mnemonic	Description
CMOS	CMOS-level compatible
Dcdr	Decoder
Ext	External
G	Ground
I	Input
I/O	Input/Output
Int	Internal
Mux	Multiplexer
O	Output
OD	Open drain (open-collector) CMOS-level compatible
P	Power
PD	Pull-down resistor
PU	Pull-up resistor
S	Schmitt-trigger TTL-level compatible
TTL	TTL-level compatible

Figure 3-1 Pin Diagram

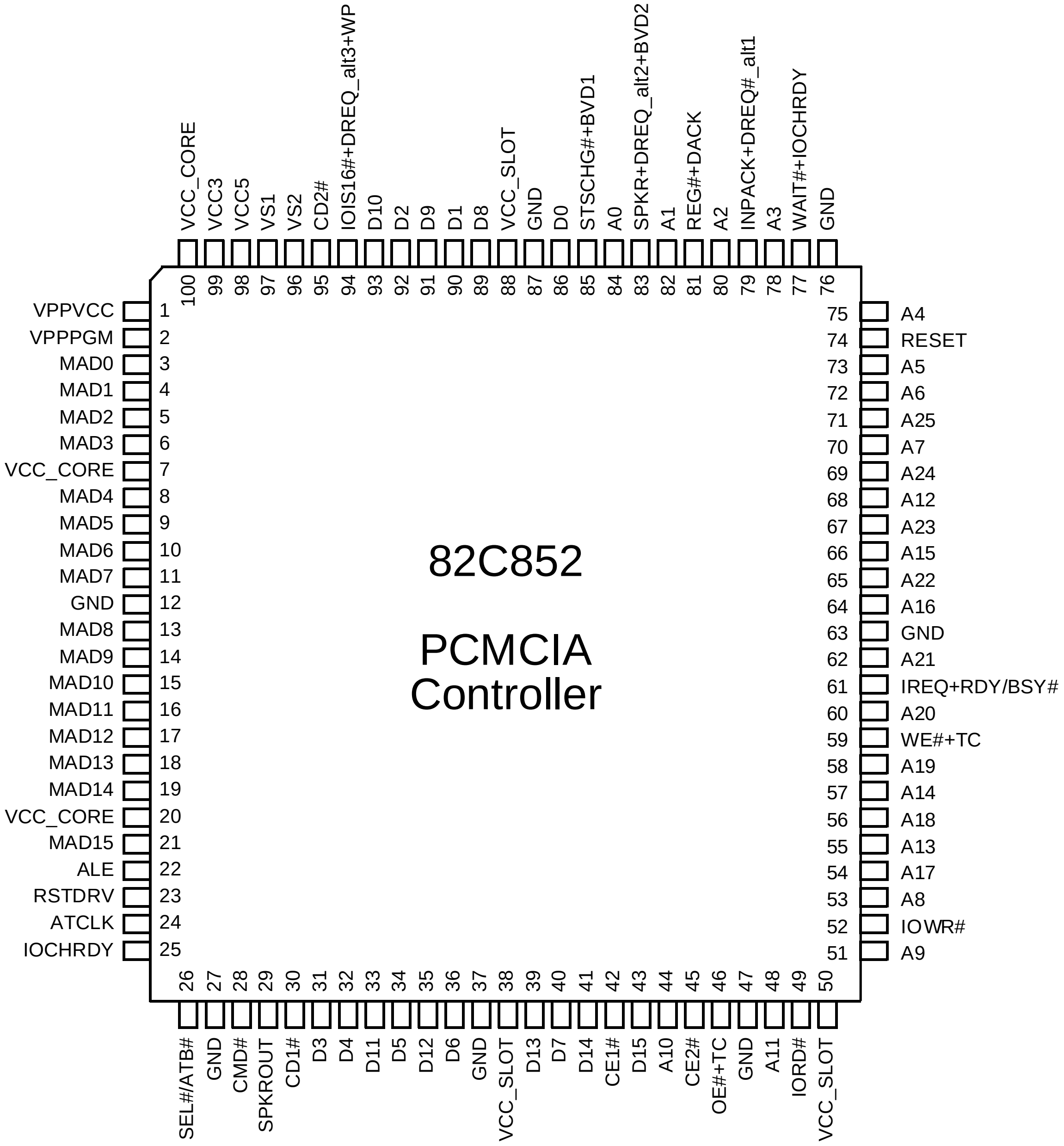


Table 3-2 Numerical Pin Cross-Reference List

Pin No.	Pin Name	Pin Type
1	VPPVCC	O
2	VPPPGM	O
3	MAD0	I/O
4	MAD1	I/O
5	MAD2	I/O
6	MAD3	I/O
7	VCC_CORE	P
8	MAD4	I/O
9	MAD5	I/O
10	MAD6	I/O
11	MAD7	I/O
12	GND	G
13	MAD8	I/O
14	MAD9	I/O
15	MAD10	I/O
16	MAD11	I/O
17	MAD12	I/O
18	MAD13	I/O
19	MAD14	I/O
20	VCC_CORE	P
21	MAD15	I/O
22	ALE	I
23	RSTDRV	I
24	ATCLK	I
25	IOCHRDY	O-TS
26	SEL#/ATB#	O-TS
27	GND	G
28	CMD#	I
29	SPKROUT	O
30	CD1#	I
31	D3	I/O
32	D4	I/O
33	D11	I/O
34	D5	I/O
35	D12	I/O
36	D6	I/O
37	GND	G
38	VCC_SLOT	P
39	D13	I/O
40	D7	I/O
41	D14	I/O
42	CE1#	I
43	D15	I/O
44	A10	I
45	CE2#	I
46	OE#	O
	TC	
47	GND	G
48	A11	I
49	IORD#	O
50	VCC_SLOT	P
51	A9	I
52	IOWR#	O
53	A8	I
54	A17	I
55	A13	I
56	A18	I
57	A14	I
58	A19	I
59	WE#	O
	TC	
60	A20	I
61	IREQ	I
	RDY/BSY#	
62	A21	I
63	GND	G
64	A16	I
65	A22	I
66	A15	I
67	A23	I
68	A12	I
69	A24	I
70	A7	I
71	A25	I
72	A6	I
73	A5	I
74	RESET	O
75	A4	I
76	GND	G
77	WAIT#	I
	IOCHRDY	
78	A3	I
79	INPACK	I
	DREQ#_alt1	
80	A2	I
81	REG#	O
	DACK	
82	A1	I
83	SPKR	I
	DREQ#_alt2	
	BVD2	
84	A0	I
85	STSCHG#	I
	BVD1	
86	D0	I/O
87	GND	G
88	VCC_SLOT	P
89	D8	I/O
90	D1	I/O
91	D9	I/O
92	D2	I/O
93	D10	I/O
94	IOIS16#	I
	DREQ#_alt3	
	WP	
95	CD2#	I
96	VS2	I
97	VS1	I
98	VCC5	O
99	VCC3	O
100	VCC_CORE	I

Table 3-3 Alphabetical Pin Cross-Reference List

Pin Name	Pin No.	Pin Type
A0	84	I
A1	82	I
A2	80	I
A3	78	I
A4	75	I
A5	73	I
A6	72	I
A7	70	I
A8	53	I
A9	51	I
A10	44	I
A11	48	I
A12	68	I
A13	55	I
A14	57	I
A15	66	I
A16	64	I
A17	54	I
A18	56	I
A19	58	I
A20	60	I
A21	62	I
A22	65	I
A23	67	I
A24	69	I
A25	71	I
ALE	22	I
ATCLK	24	I
CD1#	30	I
CD2#	95	I
CE1#	42	I
CE2#	45	I
CMD#	28	I
D0	86	I/O
D1	90	I/O
D2	92	I/O
D3	31	I/O
D4	32	I/O
D5	34	I/O
D6	36	I/O
D7	40	I/O
D8	89	I/O
D9	91	I/O
D10	93	I/O
D11	33	I/O
D12	35	I/O
D13	39	I/O
D14	41	I/O
D15	43	I/O
GND	12	G
GND	27	G
GND	37	G
GND	47	G
GND	63	G
GND	76	G
GND	87	G
INPACK+DREQ#_alt1	79	I
IOCHRDY	25	O-TS
IOIS16#+DREQ#_alt3+WP	94	I
IORD#	49	O
IOWR#	52	O
IREQ+RDY/BSY#	61	I
MAD0	3	I/O
MAD1	4	I/O
MAD2	5	I/O
MAD3	6	I/O
MAD4	8	I/O
MAD5	9	I/O
MAD6	10	I/O
MAD7	11	I/O
MAD8	13	I/O
MAD9	14	I/O
MAD10	15	I/O
MAD11	16	I/O
MAD12	17	I/O
MAD13	18	I/O
MAD14	19	I/O
MAD15	21	I/O
OE#+TC	46	O
RESET	74	O
REG#+DACK	81	O
RSTDRV	23	I
SEL#/ATB#	26	O-TS
SPKR+DREQ#_alt2+BVD2	83	I
SPKROUT	29	O
STSCHG#+BVD1	85	I
VCC3	99	O
VCC5	98	O
VCC_CORE	7	P
VCC_CORE	20	P
VCC_CORE	100	P
VCC_SLOT	38	P
VCC_SLOT	50	P
VCC_SLOT	88	P
VPPVCC	1	O
VPPPGM	2	O
VS1	97	I
VS2	96	I
WAIT#+IOCHRDY	77	I
WE#+TC	59	O

3.2 Signal Descriptions

The 82C852 chip runs CISA cycles on the host side, and PCMCIA cycles on the slot interface side.

3.2.1 Host Interface Signals

The table below lists the signals that link the 82C852 chip to the system CISA bus.

Compact ISA (CISA) Interface Signals

Signal Name	Pin No.	Pin Type	Signal Description
MAD[15:0]	21, 19-13, 11-8, 6-3	I/O	**Multiplexed Address Bus:** This multiplexed bus is used to transfer address, command, data, IRQ, DRQ, DACK information.
ATCLK	24	I	**Standard ISA Clock:** CISA device uses rising edge to clock in the first (address) phase.
ALE	22	I	**Standard ISA Address Latch Enable:** CISA peripheral device uses rising edge of ALE to latch the second (address and command) phase. CISA host uses falling edge of ALE to latch CMD# from peripheral device.
CMD#	28	I	**Command Indication:** Common to host and all devices on the CISA bus. The CISA host asserts CMD# during the data phase of the cycle to time the standard ISA command (IORD#/WR#, MRD#/WR#), and also asserts CMD# to acknowledge SEL#ATB#.
SEL#/ATB#	26	O-TS	**Device Selected / ISA Bus Back-off Request:** Common to all peripheral devices on the CISA bus. When ALE is high, the CISA device asserts SEL# to indicate to the host that it is claiming the cycle. When ALE is low, the CISA device drives this signal to indicate that it has an interrupt and/or DMA request to make; the host acknowledges by asserting CMD#.
IOCHRDY	25	O-TS	**Standard ISA Cycle Extension Request Signal during Memory and I/O Cycles:** During IRQ and DRQ drive-back cycles, the CISA device uses this signal as a command output to run the drive-back cycle to the host.
RSTDRV	23	I	**Standard ISA Bus Reset Signal**
SPKROUT	29	O	**Speaker Output from Slot Interface:** This signal is driven according to the CISA specification.

3.2.2 Power Control Signals

The power control bus signals select the correct VCC and VPP voltages to the PCMCIA card. A power control chip such as the Micrel 2560 can be used to interpret these signals to apply the correct voltage levels to the PCMCIA card.

These pins are also strap options. Refer to the Section 3.4 "Strap-Selected Interface Options" on page 8 for details.

Slot Power Control Signals

Signal Name	Pin No.	Pin Type	Signal Description
VCC5	98	O	**5.0V VCC Enable**
VCC3	99	O	**3.3V VCC Enable**
VPPPGM	2	O	**12V VPP Enable**
VPPVCC	1	O	**VPP Enable as currently selected VCC**

3.2.3 Slot Interface Signals

The slot interface is a complete set of buffered signals to the PCMCIA card slot as listed below.

82C852 Slot Interface Bus

Signal Name	Pin No.	Pin Type	Signal Description
CD1#	30	I	**Card Detect 1**
CD2#	95	I	**Card Detect 2**
VS1	97	I	**Voltage Sense 1**
VS2	96	I	**Voltage Sense 2**
SPKR	83	I	**Speaker Input** (SPKR - R2 I/O card)
DREQ#_alt2			**DREQ# alternative 2**
BVD2			**Battery Low Voltage Detect pin 2** (BVD2 - R1 or R2 memory card)
STSCHG#	85	I	**Status Change Interrupt** (active low) (STSCHG# - R2 I/O card)
BVD1			**Battery Low Voltage Detect pin 1** (BVD1 - R1 or R2 memory card)
IREQ	61	I	**Interrupt Request** (IREQ - R2 I/O card)
RDY/BSY#			**Ready/Busy** (RDY/BSY# - R1 or R2 memory card)
RESET	74	O	**Card Reset** (active high) (R2 cards)
A[25:0]	71, 69, 67, 65, 62, 60, 58, 56, 54, 64, 66, 57, 55, 68, 48, 44, 51, 53, 70, 72, 73, 75, 78, 80, 82, 84	I	**Address Bus Lines 25 through 0**
D[15:0]	43, 41, 39, 35, 33, 93, 91, 89, 40, 36, 34, 32, 31, 92, 90, 86	I/O	**Data Bus Lines 15 through 0**
WAIT#	77	I	**Wait**
IOCHRDY			**I/O Channel Ready**
IOIS16#	94	I	**16-Bit I/O Indication** (I/O card)
DREQ#_alt3			**DREQ# alternative 3** (DMA I/O card)
WP			**Write Protect** (memory only card)
IORD#	49	O	**I/O Read**
IOWR#	52	O	**I/O Write**
CE2#	45	I	**Upper Byte Enable**
CE1#	42	I	**Lower Byte Enable**
WE#	59	O	**Memory Write**
TC			**Terminal Count** (along with IOWR#)
OE#	46	O	**Memory Read**
TC			**Terminal Count** (along with IORD#)

82C852 Slot Interface Bus (cont.)

Signal Name	Pin No.	Pin Type	Signal Description
REG#	81	O	**Attribute Register Space Select**
DACK			**DMA Acknowledge**
INPACK	79	I	**Input acknowledge**
DREQ# alt.1			**DREQ# alternative 1**

3.2.4 Power and Ground Signals

VCC_CORE and VCC_SLOT can be individually selected to be either 3.3V or 5.0V. However, only VCC_SLOT can be changed dynamically. The VCC_CORE level must be indicated to the logic at reset time through ALE, as described in the CISA Specification (Appendix A).

Power and Ground Signals

Name	Pin No.	Pin Type	Description
VCC_CORE	7, 20, 100	P	**Power Connection:** To CISA interface and core logic of chip.
VCC_SLOT	38, 50, 88	P	**Power Connection:** To PCMCIA slot interface
GND	12, 27, 37, 47, 63, 76, 87	G	**Ground Connection**

3.3 Internal pull-up Resistors

The 82C852 slot interfaces are provided with pull-up resistors internal to the chip. The pull-ups are active at the times indicated in Table 3-4.

Table 3-4 Internal pull-up Resistor Scheme

Signal Name	Control Register Bit	Pull-up Scheme
CD1#, CD2#	3Fh[5]	Card Detect lines are pulled up to core VCC by default. After card insertion, these lines will be pulled low by the card. These resistors can be disabled to save power by setting configuration register bit 3Fh[5].
VS1, VS2	3Fh[5]	Voltage sense lines are pulled up to core VCC by default. After card insertion, these lines will be pulled low by a low voltages card. These resistors can be disabled to save power by setting configuration register bit 3Fh[5].
BVD1, BVD2	3Fh[4]	Battery Voltage Detect line pull-ups should be enabled only for memory-only interface cards.
RDY/BSY#	3Fh[4]	Ready/Busy line pull-up should be enabled only for memory-only interface cards.
INPACK#	3Fh[3]	Input acknowledge line pull-up should be enabled only for I/O interface cards.
WAIT#	3Fh[3]	Wait line pull-up should be enabled only for I/O interface cards.
VPPPGM	--	VPP program voltage control is pulled up only at reset time to sense the slot options.
VPPVCC	--	VCC program voltage control is pulled up only at reset time to sense the slot options.

3.4 Strap-Selected Interface Options

The 82C852 PCMCIA Controller can be strapped to operate in one of several different modes depending on its implementation in the system.

Strap options are registered at chip reset time. While a tristate buffer could be used to drive these signals only at reset, in most designs the selection straps are normally 10k ohm resistors engaged full-time. The cost of this approach is as follows. During actual use the resistors consume power only while programming voltage is selected to the cards, at which time the additional current draw for a 5.0V system would only be as high as 5V/10k ohm = 0.5mA.

The VPPPGM and VPPVCC power control pins will go high as long as the RSTDRV input to the chip is active. At this time, the VCC5 and VCC3 power control pins stay low, so no VPP will be enabled for power control devices such as Micrel 2560 part. However, if another power control device is used, it *must* disable card VPP when card VCC is disabled. Otherwise, damage to the PCMCIA card could occur.

The strap on VCC5 is a special case. It must pull *high* at reset to select the secondary I/O ports 3E2h and 3E3h. However, this action can cause a card plugged into the slot to be momentarily powered up. If this situation is undesirable, use RSTDRV to gate VCC5 to the power control device.

The slot strapping possibilities are listed in Table 3-7.

3.5 Test Mode

The chip provides several test modes that are selected at reset time through a strap option. Table 3-5 illustrates the strapping needed to enter Test Mode.

Table 3-6 shows the various tests selectable when Test Mode is enabled. Most modes are intended for factory testing only. The “tristate all outputs” mode may be useful for testing a finished board by allowing the component to effectively disappear from the circuit.

Table 3-5 Strap Option for 82C852 Test Mode

To Select:	Need pull up at reset on this line:
Normal Operation	None
Test Mode	VCC3

Table 3-6 Strap Options for Test Functions

To Select:	Need pull down at reset on these lines:
NAND Gate	None
Drive alternate lines high/low	VPPPGM
Drive alternate lines low/high	VPPVCC
Tristate all outputs	VPPPGM and VPPVCC

Table 3-7 Strap Options for 82C852 Slot Configurations

To Select:	So that 82C852 responds to I/O accesses at 3E1h (3E3h) for this range of values written to 3E0h (3E2h):	These lines must be strapped at reset:
Primary Slot A	3E0/1h, 00-3Fh	None
Primary Slot B	3E0/1h, 40-7Fh	Pull VPPPGM low
Primary Slot C	3E0/1h, 80-BFh	Pull VPPVCC low
Primary Slot D	3E0/1h, C0-FFh	Pull VPPPGM, VPPVCC low
Secondary Slot A	3E2/3h, 00-3Fh	Pull VCC5 high
Secondary Slot B	3E2/3h, 40-7Fh	Pull VCC5 high, VPPPGM low
Secondary Slot C	3E2/3h, 80-BFh	Pull VCC5 high, VPPVCC low
Secondary Slot D	3E2/3h, C0-FFh	Pull VCC5 high, VPPPGM + VPPVCC low

4.0 Functional Description

4.1 Interface Overview

The OPTi 82C852 PCMCIA Controller chipset uses two external interfaces. The terms *host interface* and *slot interface* are used throughout this document to describe these interfaces.

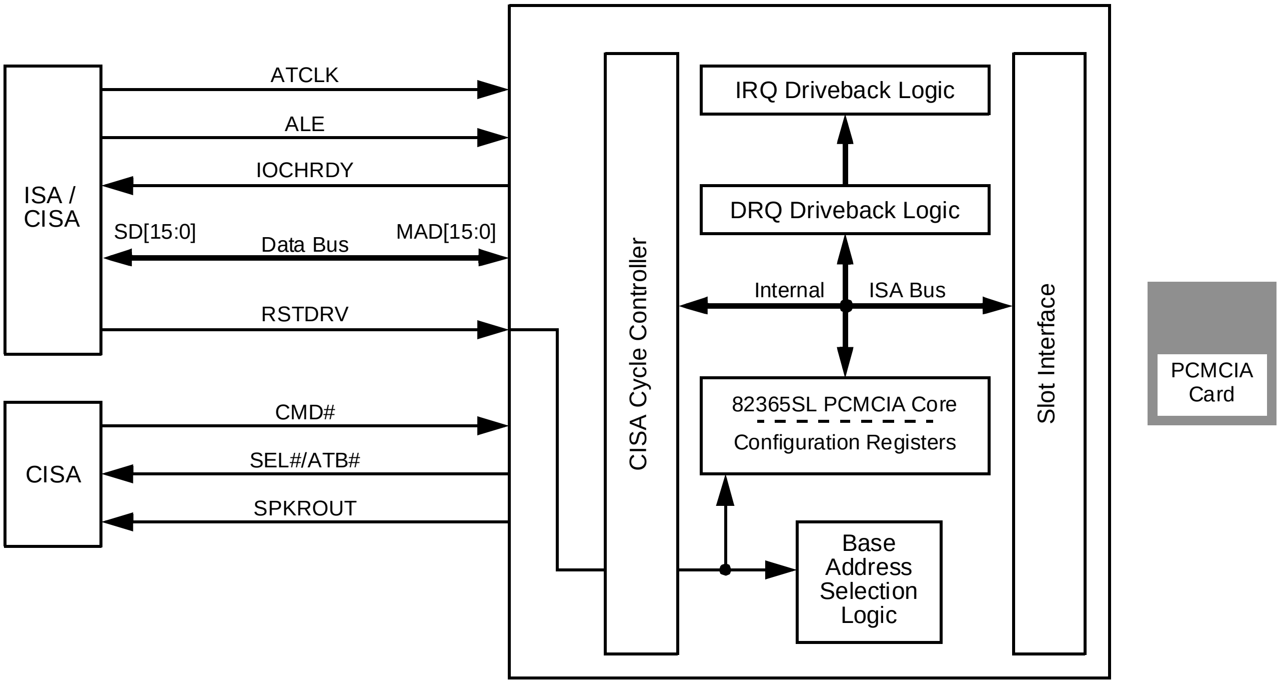
- The **host interface** provides CISA signals to the host system.
- The **slot interface** accommodates a single PCMCIA card, operating at either 5.0V or 3.3V.

The interface signal groups used to integrate the OPTi 82C852 PCMCIA Controller chipset into the standard system are described in the following sections. Figure 4-1 illustrates the interaction of the components of the OPTi 82C852 PCMCIA Controller chipset.

- The **CISA Cycle Controller** latches the address and data strobed in on the three phases of a CISA cycle and reassembles them in the proper format for the **Internal ISA Bus**, as needed by the 82365SL-standard core.
- The **PCMCIA 82365SL Core** is accessed from the Internal ISA Bus. The PCMCIA Configuration Registers are integral to the core and consist of the 82365SL-standard PCMCIA registers accessed at 64 register indexes. This register set is accessed through an index/data method, with the index register fixed at 3E0h and the data register fixed at 3E1h. A strapping option allows this decoding to take place at 3E2h and 3E3h instead.
- The **Base Address Selection** logic allows the base address of the registers to be changed, if desired, through external strapping options. In this way, up to eight separate chips can occupy the CISA bus in parallel yet each one will respond only to the cycles intended for it.
- The **IRQ Driveback** logic allows the chip to request control of the CISA bus in order to return interrupt request line change information to the host system. Likewise, the **DRQ Driveback** logic allows the chip to request control of the CISA bus in order to return DMA request line change information to the host system.

The logic subsystems of the 82C852 PCMCIA Controller are described in detail in the following sections.

Figure 4-1 82C852 Organization



4.2 CISA Cycle Controller

The CISA Cycle Controller has many responsibilities:

- Latching the address and data strobed in on the three phases of a CISA cycle.
- Claiming of configuration cycles, by decoding I/O accesses at 3E0h (3E2h) and 3E1h (3E3h).
- Claiming of memory and I/O cycles as programmed in the 82365SL-compatible registers for the card inserted.
- Inserting wait states by dropping and raising IOCHRDY for the correct number of cycles, and with the correct timing (asynchronously or synchronously), for each cycle type.

The CISA Cycle Controller handles these responsibilities as described in the following subsections.

4.2.1 Latching Address/Data

Command, address, and data are strobed in through the CISA interface in three phases on separate signal edges, as described in Appendix A. By the end of the second phase, the CISA Cycle Controller has latched enough address and command information to determine whether to claim the cycle by asserting the SEL#(/ATB#) signal.

4.2.2 Claiming of Configuration Cycles

The 82C852 chip always tracks cycles to I/O Ports 3E0h and 3E1h (optionally 3E2h and 3E3h), the port addresses that have become a de facto standard for PCMCIA configuration register access. However, since up to four 82C852 chips (for PCMCIA slots A, B, C, and D) can respond to the index/data pair, the 82C852 chip adheres to very strict rules about which chip responds in each circumstance.

Index Port 3E0h (3E2h) I/O Writes - Only the Slot A chip in the system asserts SEL# after decoding a Port 3E0h (3E2h) I/O write. All other chips track the cycle, and latch the index number written to this port.

Data Port 3E1h (3E3h) I/O Reads and Writes - Only the chip responsible for the index previously written to port 3E0h (3E2h) asserts SEL# after decoding a Port 3E1h (3E3h) I/O read or write. All other chips ignore the cycle.

Index Port 3E0h (3E2h) I/O Read - Only the Slot A chip in the system asserts SEL# after decoding a Port 3E0h (3E2h) I/O read, and then returns the last value written to this port. All other chips ignore the cycle.

This approach ensures that only one chip will assert SEL# at any time, avoiding contention.

4.2.3 Claiming PCMCIA Memory and I/O Cycles

The CISA Cycle Controller claims memory and I/O cycles by asserting SEL# according to the settings of the I/O Window registers and Memory Window registers of the 82365SL-compatible core. Refer to the “82C852 Register Set” section for a description of these registers.

4.2.4 Inserting Wait States

The CISA Cycle Controller is pre-programmed to insert different numbers of wait states according to the host cycle being driven and the target PCMCIA card inserted. Table 4-1 lists the cycle length and the timing for de-assertion/assertion of IOCHRDY for each possible combination.

The 82C365SL core is ISA-based. Therefore, the CISA Cycle Controller converts cycles as necessary to generate 16-bit-only CISA cycles to 8- or 16-bit ISA cycles. The effect of this conversion on cycle duration is seen in the table.

Table 4-1 Wait State (WS) Control

Host Cycle Type	WS Requested by Host	PCMCIA Card Bus Width	PCMCIA Card WS	WS Inserted	Total Cycle Size (ATCLKs)	IOCHRDY Release	IOCHRDY Sampling by Host
Memory Fast CISA ISA# = 1	0	16-bit	0	0	2	Synchronous	Direct
	0	16-bit		1	3	Synchronous	Direct
	0	8-bit	0	1	3	Synchronous	Direct
	0	8-bit		4	6	Synchronous	Direct
Memory ISA compatible ISA# = 0		16-bit	0	0	3	Asynchronous	Resynchronized
		16-bit		0	3	Asynchronous	Resynchronized
		8-bit	0	0	3	Asynchronous	Resynchronized
		8-bit		3	6	Asynchronous	Resynchronized
I/O		16-bit		0	3	Asynchronous	Resynchronized
		8-bit	0	0	3	Asynchronous	Resynchronized
		8-bit		3	6	Asynchronous	Resynchronized
DACK		16-bit		0	3	Never Asserted	Resynchronized
		8-bit		0	6	Never Asserted	Resynchronized

Note: Zero wait state cycles are selected by bit 11[6] for memory cycles and by bits 07h[6,2] for I/O cycles.

4.3 PCMCIA 82365SL Core

The Intel 82365SL core is used in the 82C852 chip to assure compatibility with most popular PCMCIA card and socket services. The PCMCIA Configuration Registers are integral to the core and consist of the industry-standard 82365SL PCMCIA registers accessed at 64 register indexes. This register set is accessed through an index/data method, with the index register fixed at 3E0h (3E2h) and the data register fixed at 3E1h (3E3h).

Some register functions have been modified slightly, while in other cases additional functionality has been added to formerly “reserved” bits. Additions and changes to the 82365SL core are noted in Section 5.0 "82C852 Register Set" on page 12.

4.4 Base Address Selection Logic

The Base Address Selection logic provides selection signals as inputs to the CISA Cycle Controller to allow the controller to claim only the appropriate cycles as explained in Section 4.2 "CISA Cycle Controller" on page 10. The base address is selected according to strap options listed in Section 3.4 "Strap-Selected Interface Options" on page 8.

4.5 IRQ and DRQ Driveback Logic

The 82C852 sends interrupt requests and DRQ status change information back to the system by way of the CISA IRQ/DRQ Driveback Cycle as described in Appendix A.

Since the IRQ information arrives at the CISA host before it is used to generate an ISA IRQ, the host can redefine any of the IRQ signals to select other functions. For example, IRQ13, which is not on the ISA bus, could be redefined as Ring Indicator (RI) by the host.

Included in the Driveback circuitry is the Stop Clock logic. When the CISA Cycle Controller decodes a Stop Clock cycle, the Driveback circuitry state machine must switch ATB# from a synchronous signal to a product of combinatorial logic. In this way, the next interrupt that arrives from the PCMCIA card can be fed directly to ATB# without clock synchronization, and used to restart the host clock. Once the Driveback circuitry begins to receive clocks again, it will generate a synchronous interrupt signal on ATB#.

5.0 82C852 Register Set

The 82C852 PCMCIA Controller chip provides programming registers grouped as General Purpose, I/O Mapping Window, Memory Mapping Window, and Special. The 82C852 PCMCIA Socket Configuration Registers are addressed for slot A, B, C, or D. The index addresses to which the registers respond are determined by a strapping option, described in the Strapping Options section of this document.

Table 5-1 82C852 General Purpose Register Group

7	6	5	4	3	2	1	0
Index 00h, 40h, 80h, C0h			**Identification Register (RO)**				**Default = 8Fh**
Interface Type - indicates supported interfaces. 00 = I/O only 01 = Memory only 10 = Memory & I/O (always) 11 = Reserved		Chip revision level (RO): 00 = 1st revision		Revision number bits [3:0] (RO): 1111 = OPTi 82C852 PCMCIA Controller 0111 = OPTi 82C824 CardBus Controller (always) 0100 = Intel 82C365SL 0010 = Cirrus 672x			
Index 01h, 41h, 81h, C1h			**Interface Status Register (RO)**				**Default = 33h**
Reserved	Card power status: 0 = Off 1 = On	RDY/BSY# status: 0 = Busy 1 = Ready	WP status: 0 = Not write protected 1 = Write protected	CD2# status: 0 = High 1 = Low	CD1# status: 0 = High 1 = Low	BVD2/ SPKR status: 0 = Low 1 = High	BVD1/ STSCHG# status: 0 = Low 1 = High
Index 02h, 42h, 82h, C2h			**Power Control Register**				**Default = 00h**
Socket signals: 0 = Disable 1 = Enable (tristate or drive low)	Reserved: Write bit as read.	Auto card power-up on insertion (RO): 0 = Disable (always)	Card VCC control - Sets VCC5-VCC3 to these bit values. Refer to Table 5-2.		Slot VCC threshold scaling: 0 = 3.3V 1 = 5.0V	Card VPP Control - Sets VPP-PGM-VPP3/5 to these bit values. Refer to Table 5-2.	
Index 03h, 43h, 83h, C3h			**Reset and General Control Register**				**Default = 00h**
Reserved: Write bit as read.	RESET signal status: 0 = Active (high) 1 = Inactive	PCMCIA card interface: 0 = Memory 1 = I/O	Reserved: Write bit as read.	IREQ routing: 0000 = None 0001 = Reserved* 0010 = Reserved* 0011 = IRQ3 0100 = IRQ4 0101 = IRQ5 0110 = Reserved* 0111 = IRQ7 1000 = Reserved* 1001 = IRQ9 1010 = IRQ10 1011 = IRQ11 1100 = IRQ12 1101 = Reserved* 1110 = IRQ14 1111 = IRQ15			
*These IRQs are driven back to the host, but the host may not recognize them.							
Index 04h, 44h, 84h, C4h			**Card Status Change Register**				**Default = 00h**
Reserved: Write bits as read.				CDx# status change or software interrupt: 0 = No 1 = Yes	RDY/BSY# has gone high: 0 = No 1 = Yes = 0 for I/O cards	BVD2 has gone low: 0 = No 1 = Yes = 0 for I/O cards	BVD1/ STSCHG# has gone low: 0 = No 1 = Yes

Table 5-1 82C852 General Purpose Register Group (cont.)

7	6	5	4	3	2	1	0
Index 05h, 45h, 85h, C5h		**STSCHG# Interrupt Configuration Register**					**Default = 00h**
STSCHG# routing: 0000 = None 0001 = Reserved 0010 = Reserved 0011 = IRQ3 0100 = IRQ4 0101 = IRQ5 0110 = Reserved 0111 = IRQ7 1000 = Reserved 1001 = IRQ9 1010 = IRQ10 1011 = IRQ11 1100 = IRQ12 1101 = Reserved 1110 = IRQ14 1111 = IRQ15				STSCHG# on CD1-2# change: 0 = Disable 1 = Enable	STSCHG# on RDY/BSY# low-to-high change: 0 = Disable 1 = Enable	STSCHG# on battery warning BVD2 high-to-low change: 0 = Disable 1 = Enable	STSCHG# on battery dead BVD1 high-to-low change: 0 = Disable 1 = Enable
Index 06h, 46h, 86h, C6h		**Address Window Enable Register**					**Default = 00h**
I/O Window 1: 0 = Disable 1 = Enable	I/O Window 0: 0 = Disable 1 = Enable	Internal MEMCS16 decode: 0 = A[23:17] 1 = A[21:12]	Memory Window 4: 0 = Disable 1 = Enable	Memory Window 3: 0 = Disable 1 = Enable	Memory Window 2: 0 = Disable 1 = Enable	Memory Window 1: 0 = Disable 1 = Enable	Memory Window 0: 0 = Disable 1 = Enable

5.1 Power Control

Index 02h[4:3] set the external VCC5-VCC3 pin levels directly. Index 02h[1:0] set the external VPPPGM-VPPVCC pin levels directly. The interpretation of these signals depends on the external logic used. Socket services must be aware of the hardware design in order to make the proper selections.

Table 5-2 below shows how the external control signals are interpreted by a typical power control chip, the Micrel 2560. Using this device allows the power control to be compatible with the Intel 82365SL definition. In the table, 'Disabled' = high impedance; 'Ground' indicates that the voltage source is actively clamped to ground.

Table 5-2 Voltage Control Pin Interpretations using Micrel 2560 Chip

VCC5 Index 02h[4]	VCC3 Index 02h[3]	Card Vcc Selection	VPPPGM Index 02h[1]	VPPVCC Index 02h[0]	Card Vpp Selection
0	0	Disabled	0	0	Disabled
			0	1	Disabled
			1	0	Disabled
			1	1	Ground
0	1	3.3V	0	0	Disabled
			0	1	3.3V
			1	0	12V
			1	1	Ground
1	0	5V(1)	0	0	Disabled
			0	1	5V
			1	0	12V
			1	1	Ground
1	1	3.3V	0	0	Disabled
			0	1	3.3V
			1	0	5V
			1	1	Ground

(1) If the VS2 (5VDET) pin from the card is grounded, VCC5-VCC3 stay low when Index 02h[4:3] = 10. This feature prevents 5V from being applied to a 3.3V-only card.

Slot VCC Threshold Scaling - The threshold level of the chip input buffers is controlled by Index 02h[2] and is independent of the voltage control pin settings. This independent selection feature allows the designer to choose a voltage control chip with different control pin selection definitions than the Micrel 2560 part. The voltage threshold should be set by software according to the card voltage being enabled.

5.2 I/O Mapping Window Register Group

The I/O Window Registers contain bits that maintain Cirrus 6722 compatibility. Only the window address offset is shown. See below for calculation of base index address for each of the two available windows.

Table 5-3 I/O Mapping Window Register Group - Offset +7h-+Bh

7	6	5	4	3	2	1	0
Offset +7h			**I/O Window Control Register**				**Default = 00h**
Window 1 additional wait states: 0 = None 1 = One	Window 1 zero-wait 8-bit cycles: 0 = No 1 = Yes	Window 1 size select: 0 = Use bit 4 1 = Use IOIS16#	Window 1 data size: 0 = 8 bits 1 = 16 bits	Window 0 additional wait states: 0 = None 1 = One	Window 0 zero-wait 8-bit cycles: 0 = No 1 = Yes	Window 0 size select: 0 = Use bit 0 1 = Use IOIS16#	Window 0 data size: 0 = 8 bits 1 = 16 bits
Offset +8h			**I/O Window Start Address Register - Byte 0**				**Default = 00h**
			Window Start Address bits IOS[7:0]				
Offset +9h			**I/O Window Start Address Register - Byte 1**				**Default = 00h**
			I/O Window Start Address bits IOS[15:8]				
Offset +Ah			**I/O Window Stop Address Register - Byte 0**				**Default = 00h**
			I/O Window Stop Address bits IOST[7:0]				
Offset +Bh			**I/O Window Stop Address Register - Byte 1**				**Default = 00h**
			I/O Window Stop Address bits IOST[15:8]				

Table 5-4 Index Addresses for I/O Window Registers

I/O Window Index Address for:	**I/O Window Control**	**I/O Window 0**				**I/O Window 1**			
		Start Address		**Stop Address**		**Start Address**		**Stop Address**	
		Byte 0	**Byte 1**	**Byte 0**	**Byte 1**	**Byte 0**	**Byte 1**	**Byte 0**	**Byte 1**
Slot A	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh
Slot B	47h	48h	49h	4Ah	4Bh	4Ch	4Dh	4Eh	4Fh
Slot C	87h	88h	89h	8Ah	8Bh	8Ch	8Dh	8Eh	8Fh
Slot D	C7h	C8h	C9h	CAh	CBh	CCh	CDh	CEh	CFh

5.3 Memory Mapping Window Register Group

Only the window address offset is shown in Table 5-5. To calculate the addresses for all memory windows:

- Add the offset to the index base (as shown in Table 5-6) for the desired slot and window.

Zero Wait States - This setting enables shorter cycles for faster PCMCIA cards. Refer to Section 4.2 "CISA Cycle Controller" on page 10 to determine the effect of this bit.

Command Length - This value selects the command length for both 8-bit and 16-bit windows. In the 82365SL part, this value controls only 16-bit windows.

Table 5-5 Memory Mapping Window Register Group - Offset +0h-+5h

7	6	5	4	3	2	1	0
Offset +0h	**Memory Window Start Address Register - Byte 0**						**Default = 00h**
Memory Mapping Window Start Address bits MS[19:12]							
Offset +1h	**Memory Window Start Address Register - Byte 1**						**Default = 00h**
Data path: 0 = 8 bits 1 = 16 bits	Zero wait states: 0 = No 1 = Yes	Reserved: Write bits as read.		Memory Mapping Window Start Address bits MS[23:20]			
Offset +2h	**Memory Window Stop Address Register - Byte 0**						**Default = 00h**
Memory Mapping Window Stop Address bits MST[19:12]							
Offset +3h	**Memory Window Stop Address Register - Byte 1**						**Default = 00h**
Command Length (ATCLKs): 00 = Two 01 = Three 10 = Four 11 = Five		Reserved: Write bit as read.		Memory Mapping Window Stop Address bits MST[23:20]			
Offset +4h	**Memory Window Offset Address Register - Byte 0**						**Default = 00h**
Memory Mapping Window Offset Address bits MOFST[19:12]							
Offset +5h	**Memory Window Offset Address Register - Byte 1**						**Default = 00h**
Window write control: 0 = Enable 1 = Disable	Memory access: 0 = Common 1 = Attribute	Memory Mapping Window Offset Address bits MOFST[25:20]					

Table 5-6 Index Base Addresses for Memory Windows

Index Base For:	Start Address		Stop Address		Offset Address	
	Byte 0	Byte 1	Byte 0	Byte 1	Byte 0	Byte 1
Memory Window 0#						
Slot A	10h	11h	12h	13h	14h	15h
Slot B	50h	51h	52h	53h	54h	55h
Slot C	90h	91h	92h	93h	94h	95h
Slot D	D0h	D1h	D2h	D3h	D4h	D5h
Memory Window 1#						
Slot A	18h	19h	1Ah	1Bh	1Ch	1Dh
Slot B	58h	59h	5Ah	5Bh	5Ch	5Dh
Slot C	98h	99h	9Ah	9Bh	9Ch	9Dh
Slot D	D8h	D9h	DAh	DBh	DCh	DDh
Memory Window 2#						
Slot A	20h	21h	22h	23h	24h	25h
Slot B	60h	61h	62h	63h	64h	65h
Slot C	A0h	A1h	A2h	A3h	A4h	A5h
Slot D	E0h	E1h	E2h	E3h	E4h	E5h
Memory Window 3#						
Slot A	28h	29h	2Ah	2Bh	2Ch	2Dh
Slot B	68h	69h	6Ah	6Bh	6Ch	6Dh
Slot C	A8h	A9h	AAh	ABh	ACh	ADh
Slot D	E8h	E9h	EAh	EBh	ECh	EDh
Memory Window 4#						
Slot A	30h	31h	32h	33h	34h	35h
Slot B	70h	71h	72h	73h	74h	75h
Slot C	B0h	B1h	B2h	B3h	B4h	B5h
Slot D	F0h	F1h	F2h	F3h	F4h	F5h

5.4 Special PCMCIA/82C852 PCMCIA Registers

The 82C852 logic provides compatibility with the Intel 82365SL PCMCIA chipset. In addition, certain Cirrus 6722 PCMCIA chipset features are implemented. Since there are register conflicts between these two devices in certain locations, the 82C852 logic implements the register features as noted below.

5.4.1 DMA on the PCMCIA Interface

DMA operations are described with respect to system memory access. During a DMA write, data is transferred from a PC Card to system memory. During a DMA read, data is transferred from system memory to a PC Card. Address lines to the PC Card are ignored during DMA operations. DMA signals are defined as follows for the PCMCIA interface.

DREQ# - The DMA Request signal DREQ# is only available when a PC Card and socket are configured for DMA operations. Note that DREQ# is active low, opposite to the traditional ISA bus sense of the signal. A PC Card asserts DREQ# to indicate to the host that it is requesting service. The PC Card asserts DREQ# until the host responds by asserting DACK. A PC Card may use any one of the following three pins for DREQ#: SPKR, INPACK, or IOIS16#. The PC Card indicates the pin used for DREQ# in the Miscellaneous Features Field of the card configuration header (CIS).

DACK - A DMA transfer is indicated when DACK is active along with either IORD# or IOWR#. Note that DACK is active high, opposite to the traditional ISA bus sense of the signal. The 82C852 chip uses the card REG# pin to indicate a DMA operation. The card must be programmed for an I/O interface before the DMA interface can be enabled. The REG#+DACK signal is then used to distinguish between a DMA cycle and a normal I/O cycle. For a normal I/O cycle, REG#+DACK is held low for the complete bus cycle. For a DMA transfer, REG#+DACK is held high during the entire DMA bus cycle.

TC - The 82C852 chip signals terminal count for DMA read operations by asserting WE# along with IOWR#, and for DMA write operations by asserting OE# along with IORD#.

5.4.2 DMA Control Register

The DMA Control Register uses a similar format to that available in the Cirrus 6722 register set at Index 3Fh for its upper 3 bits; however, bits [4:0] are different. Bits [2:0] select the DMA channel because, unlike the Cirrus controller, the 82C852 controller generates all DMA channel requests directly (it does not depend on the host to redirect the DREQ/ DACK lines). Bits [4:3] allow enabling of built-in pull-up resistors that are not available on the Cirrus part.

DREQ# Select - These bits select the pin that will be used to provide the DREQ# signal to the PCMCIA card. Most PCMCIA cards will be able to sacrifice INPACK for the DREQ# function; the IOIS16# and SPKR pins are offered as alternatives. The "No DMA function" disables the DMA feature altogether and eliminates the need for Index 1Eh[6] used by the Cirrus 6722 to enable DMA operation.

CD1-2# and VS1-2 Pull-ups - The PCMCIA card detect (CD1-2#) and voltage sense (VS1-2) lines are normally pulled up internal to the 82C852 chip to avoid the need for external resistors. The control bit is provided to disable these resistors during power-down situations.

DMA Channel - These bits indicate the system DMA channel to which the DREQ will be directed. DRQ0-3 are 8-bit channels; DRQ5-7 are 16-bit channels. These bits are **not** present in the Cirrus 6722 part.

Table 5-7 DMA Control Register

7	6	5	4	3	2	1	0
Index 3Fh, 7Fh, BFh, FFh			**DMA Control Register**				**Default = 00h**
DREQ# select: 00 = No DMA function 01 = Use INPACK 10 = Use IOIS16# 11 = Use SPKR		CD1-2# and VS1-2 pull-ups: 0 = Enable 1 = Disable	BVD1-2, RDY/BSY# pull-ups: 0 = Disable (default) 1 = Enable	INPACK, WAIT# pull-ups: 0 = Disable (default) 1 = Enable	DMA channel: 000 = DRQ0 001 = DRQ1 010 = DRQ2 011 = DRQ3 100 = Rsvd 101 = DRQ5 110 = DRQ6 111 = DRQ7		

5.4.3 ATA Interface

The ATA Control Register is provided to allow a minor redefinition of the interface to accommodate ATA interface devices, normally IDE types of devices such as disk drives and flash EEPROM cards. This register is not strictly compatible with the register at offset 26h in the Cirrus 6722 register set.

Interface Mode - Selecting ATA mode changes operation as follows:

1) Index 3Eh[7:3] are enabled to manually control address bits A[25:21] to the card.
2) CE1# takes on the IDE function of CS1# which goes low when address bit A9 is low (address range 1F0-1F7h or 170-177h).
3) CE2# takes on the IDE function of CS3# which goes low when address bit A9 is high (address range 3F6-3F7h or 376-377h).

For proper operation of a card with this type of interface, it is also necessary to program the I/O Mapping Windows to the 1F0-1F7h (or 170-177h) range and to the 3F6-3F7h (or 376-377h) range.

5.4.4 Control Registers

The 82C852 slot interface implements the VS1 and VS2 signals. The new PCMCIA specification allows VS1-2 to be used in determining whether a card can be powered up at 5.0V or not, according to Table 5-9. This information pertains to the Miscellaneous Control Register at Index 16h, described below.

Table 5-8 ATA Control Register

7	6	5	4	3	2	1	0
Index 3Eh, 7Eh, BEh, FEh			**ATA Control Register**				**Default = 00h**
A25 (CSEL control)	A24 (M/S# control)	A23 (VU control)	A22 (Misc. control)	A21 (Misc. control)	Card RESET polarity: 0 = Normal 1 = Inverted	Card IREQ# polarity: 0 = Normal 1 = Inverted	Interface mode: 0 = PCMCIA 1 = ATA

Table 5-9 VS1-2 Status Indication for PCMCIA Cards.

VS2	VS1	Key on PC Card	PCMCIA Card Type Indicated
Open	Open	5.0V	5.0V R2 card
Open	Ground	Low Voltage	3.3V R2 card
Open	Ground	5.0V	3.3V or 5.0V R2 card
Ground	Open	Low Voltage	Low Voltage R2 card
Ground	Ground	Low Voltage	Low Voltage or 3.3V R2 card
Ground	Ground	5.0V	Low Voltage, 3.3V, or 5.0V R2 card

5.4.4.1 Miscellaneous Control Register

At Index 16h, the Intel 82365SL implements the Card Detect and General Control Register, while the Cirrus 6722 part implements Miscellaneous Control Register 1. The 82C852 controller register at this offset incorporates bits from both of these registers and is therefore **not** strictly compatible with either.

Back-to-Back 8-bit Timing - Index 16h[7] provides control over bus conversion timing. The default setting separates the second half of a 16-to-8-bit conversion from the first by three ATCLKs. Since this issue is not strictly dealt with in the PCMCIA specification, 8-bit cards that have no back-to-back restrictions can provide better performance by setting this bit to 1 for a single intervening clock.

TC Timing - Index 16h[6] is provided to control the duration of Terminal Count (TC) to the PCMCIA DMA card. While the PCMCIA specification requires that TC be taken away before command, the Cirrus data book shows TC asserted even after the command edge. DMA cards designed to latch TC on the rising edge of command must set 16h[6]=1.

5.4.4.2 Global Control Register

Only one bit of this Intel 82365SL register is implemented. The other bits correspond to IRQ manipulation that is unnecessary in the 82C852 chip.

Reset Change Status - Index 1Eh[2] selects the mode used to clear status change events in the Card Status Change Register at Index 04h. In its default setting of 1Eh[2] = 0, the status change events are all cleared at once every time the register at Index 04h is read. If 1Eh[2] = 1, reading the register at Index 04h does not clear any events. To clear each event, software must write a 1 to the bit position at Index 04h that indicated status change event. Effectively, writing back the same value read will clear the status change event.

5.4.4.3 Miscellaneous Control Register 2 (Not Implemented)

The Cirrus 6722 part provides a different register at offset 1Eh. Its bit functions are not needed in the 82C852 chipset for the following reasons.

IRQ15, IRQ12 Assignment - The assignment of an interrupt line to signals such as RI (ring indicator) is a function of the host chipset in OPTi architecture.

Port 3F7 bit 7 Sharing - The conflict between these ports is resolved by the host chipset in OPTi architecture.

Core Voltage - Core voltage threshold selection is a strap option on the 82C852 chip.

Clock Source - The timing on the 82C852 part is provided only by ATCLK.

Table 5-10 Miscellaneous and Global Control Registers

7	6	5	4	3	2	1	0
Index 16h, 56h, 96h, D6h			**Miscellaneous Control Register**				**Default = 03h**
Back-to-back 8-bit timing (ATCLKs): 0 = 3 1 = 1	TC timing: 0 = PCMCIA standard 1 = Stays active past end of cmd.	Reset Cfg. Registers if CD1-2# go high: 0 = No 1 = Yes	SPKROUT: 0 = Tristated 1 = Driven	SPKROUT drive option: 0 = Shared (CISA) 1 = Always driven	Reserved: Write as read.	VS1 status (RO): 0 = Low 1 = High	VS2 status (RO): 0 = 3.3V 1 = 5.0V
Index 1Eh, 5Eh, 9Eh, DEh			**Global Control Register**				**Default = 00h**
IRQ driveback: 0 = Normal Mode 1 = Show inactive IRQ	Reserved: Write as read.	Zoom video Mode: 0 = Disable (Normal Mode) 1 = Enable	Reserved: Write as read.		Reset change status: 0 = On status change reg read 1 = On write to bit	Reserved: Write as read.	

6.0 Maximum Ratings

Stresses above those listed in the following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied.

6.1 Absolute Maximum Ratings

Symbol	Parameter	5.0 Volt		3.3 Volt		Unit
		Min	Max	Min	Max	
VCC	5.0V Supply Voltage		6.5			V
VDD	3.3V Supply Voltage				4.0	V
VI	Input Voltage	–0.5	VCC + 0.3	–0.5	VDD + 0.5	V
VO	Output Voltage	–0.5	VCC + 0.5	–0.5	VDD + 0.5	
TOP	Operating Temperature	0	+70	0	+70	°C
TSTG	Storage Temperature	–40	+125	–40	+125	°C

6.2 DC Characteristics: 5.0 Volt (VCC = 5.0V ±5%, TA = 0°C to +70°C)

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input low Voltage	–0.5	0.8	V	
VIH	Input high Voltage	2.0	VCC + 0.5	V	
VOL	Output low Voltage		0.4	V	IOL = 4.0mA
VOH	Output high Voltage	2.4		V	IOH = –1.6mA
IIL	Input Leakage Current		10	µA	VIN = VCC
IOZ	Tristate Leakage Current		10	µA	
CIN	Input Capacitance		10	pF	
COUT	Output Capacitance		10	pF	
ICC	Power Supply Current	2.72	12	mA	

6.3 DC Characteristics: 3.3 Volt (VDD = 3.3V ±5%, TA = 0°C to +70°C)

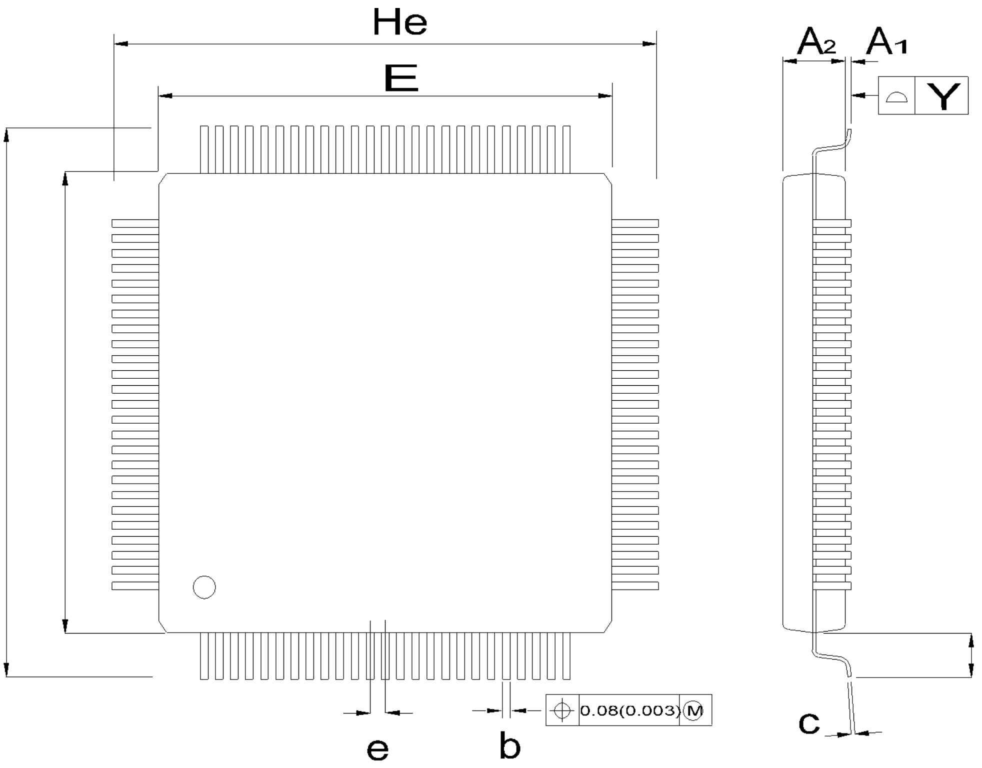
Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input low Voltage	–0.5	0.8	V	
VIH	Input high Voltage	2.0	VCC + 0.5	V	
VOL	Output low Voltage		0.4	V	IOL = 4.0mA
VOH	Output high Voltage	2.4		V	IOH = –1.6mA
IIL	Input Leakage Current		10	µA	VIN = VDD
IOZ	Tristate Leakage Current		10	µA	
CIN	Input Capacitance		10	pF	
COUT	Output Capacitance		10	pF	
ICC	Power Supply Current	0.34	4	mA	

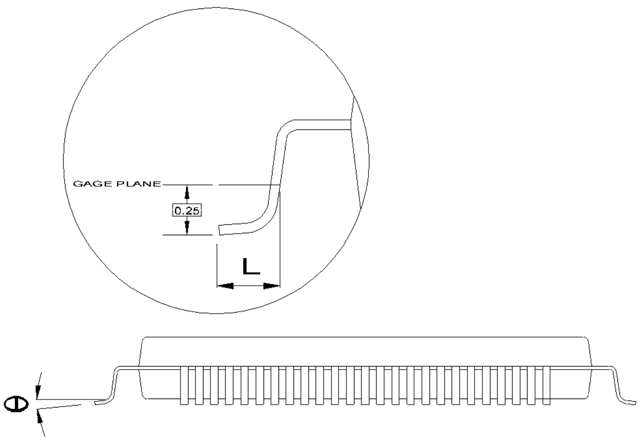
6.4 AC Characteristics (TBD)

6.5 AC Timing Diagrams (TBD)

7.0 Mechnical Package Outline

Figure 7-1 100-Pin Thin Quad Flat Package (TQFP)





SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A_1	0.05	0.10	0.15	0.002	0.004	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.090		0.200	0.004		0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	13.90	14.00	14.10	0.547	0.551	0.555
e		0.50			0.020	
Hd	15.90	16.00	16.10	0.626	0.630	0.634
He	15.90	16.00	16.10	0.626	0.630	0.634
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00			0.039	
Y			0.08			0.003
θ	0		7	0		7

Dwg. No.: AS100TQFP-001	
Dwg. Rev.: A0	Unit: MM/INCH

Appendix A. Compact ISA Specification

This document describes a new OPTi interface that will be used to interface the 82C852 PCMCIA Controller to OPTi system controller chipsets. This interface may also be used to interface OPTi peripheral products in the future. The interface is OPTi-proprietary, and may be licensed to others in the future.

A.1 Compact ISA Overview

The Compact ISA interface coexists with the standard ISA interface. Chips that support the Compact ISA interface enjoy a reduced ISA pin count because address signals and command information are strobed in on the SD[15:0] bus. ISA pins eliminated are:

- SA[23:0] (24 pins)
- IORD#, IOWR#, MRD#, MWR#, SMRD#, SMWR#, SBHE#, NOWS#, AEN, IO16#, M16# (11 pins)
- IRQ3, 4, 5, 6, 7, 10, 11, 12, 14, 15; DRQ/DACK#0, 1, 2, 3, 5, 6, 7, and TC (25 pins)

Compact ISA defines only two new signals, CMD# and SEL#/ATB#, for a total requirement of 22 pins. The pin count reduction over standard ISA is 58 pins. Compact ISA performance is comparable with that of 16-bit ISA bus peripheral devices. Moreover, Compact ISA does **not** interfere with standard ISA operations. The complete signal set of Compact ISA, referred to in the descriptions as CISA, is shown below.

Table A-1 Compact ISA (CISA) Interface Signals

Name	Type*	Description
MAD[15:0]	I/O	**Multiplexed Bus:** Used to transfer address, command, data, IRQ, DRQ, DACK information.
ATCLK	I	**Standard ISA Clock:** CISA device uses rising edge to clock in the first (address) phase.
ALE	I	**Standard ISA Address Latch Enable:** CISA peripheral device uses rising edge of ALE to latch the second (address and command) phase. CISA host uses falling edge of ALE to latch CMD# from peripheral device.
CMD#	I	**Command Indication:** Common to host and all devices on the CISA bus. The CISA host asserts CMD# during the data phase of the cycle to time the standard ISA command (IORD#/WR#, MRD#/WR#), and also asserts CMD# to acknowledge SEL#ATB#.
SEL#/ATB# (also CLKRUN#)	O Tristate	**Device Selected / ISA Bus Backoff Request:** Common to all peripheral devices on the CISA bus. When ALE is high, the CISA device asserts SEL# to indicate to the host that it is claiming the cycle. When ALE is low, the CISA device drives this signal to indicate that it has an interrupt and/or DMA request to make; the host acknowledges by asserting CMD#. After the host has preset the CISA device in a Stop Clock mode, the device can assert this signal asynchronously to restart the clock.
IOCHRDY	O Tristate	**Standard ISA Cycle Extension Request:** Used during memory and I/O cycles.
RSTDRV	I	**Standard ISA Bus Reset**

*Peripheral side

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A.2 Compact ISA Cycle Definition

The MAD[15:0] lines contain different information for each phase of the bus cycle. The use of these lines varies according to whether a memory cycle or an I/O cycle is being run. Certain cycle definition bits are common to all cycles, as shown in Table A-2.

Retained Values

Entries marked "Same" retain the same value as in the previous phase, in order to reduce transitions where possible. However, the CISA peripheral device decode logic must **not** assume that these values will be stable. The bits may be reassigned in the future.

A.2.1 Memory Cycle

The MAD[15:0] bit meanings for each phase of a memory cycle are shown in Table A-3. The M/IO# bit is always 1 for memory cycles.

The general structure of Compact ISA memory cycles is shown in Figure A-1 and Figure A-2.

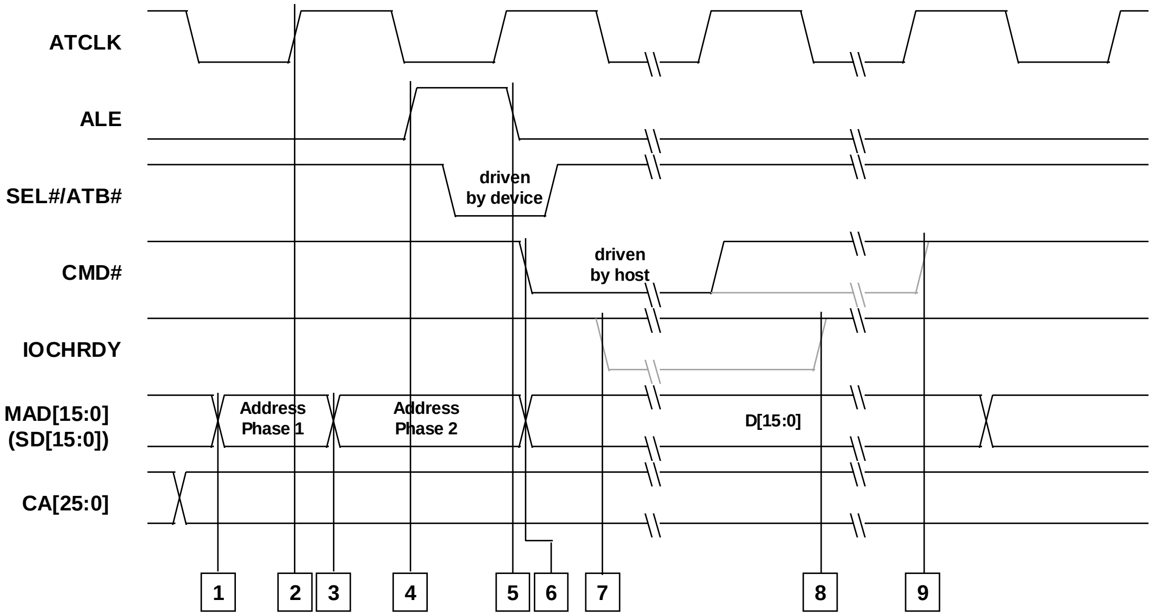
Table A-2 Common MAD Bit Usage

Signal	Phase 1	Phase 2
MAD0	M/IO# indication bit; used to determine the cycle type.	W/R# indication bit
MAD1	I/D# indication bit. It is always 0 if M/IO# = 1, and selects between I/O and DMA cycles if M/IO# = 0.	SBHE# indication bit
MAD2	Usage varies.	ISA# timing indication bit; described in the "Performance Control" section of this document.

Table A-3 MAD Bits During Memory Cycles

Phase	MAD15	MAD14	MAD13	MAD12	MAD11	MAD10	MAD9	MAD8	MAD7	MAD6	MAD5	MAD4	MAD3	MAD2	MAD1	MAD0
1	SA23	SA22	SA21	SA20	SA19	SA18	SA17	SA16	SA15	SA14	SA13	SA12	SA11	SA10	I/D# = 0	M/IO# = 1
2	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	Same	Same	Same	ISA#	SBHE#	W/R#
3	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

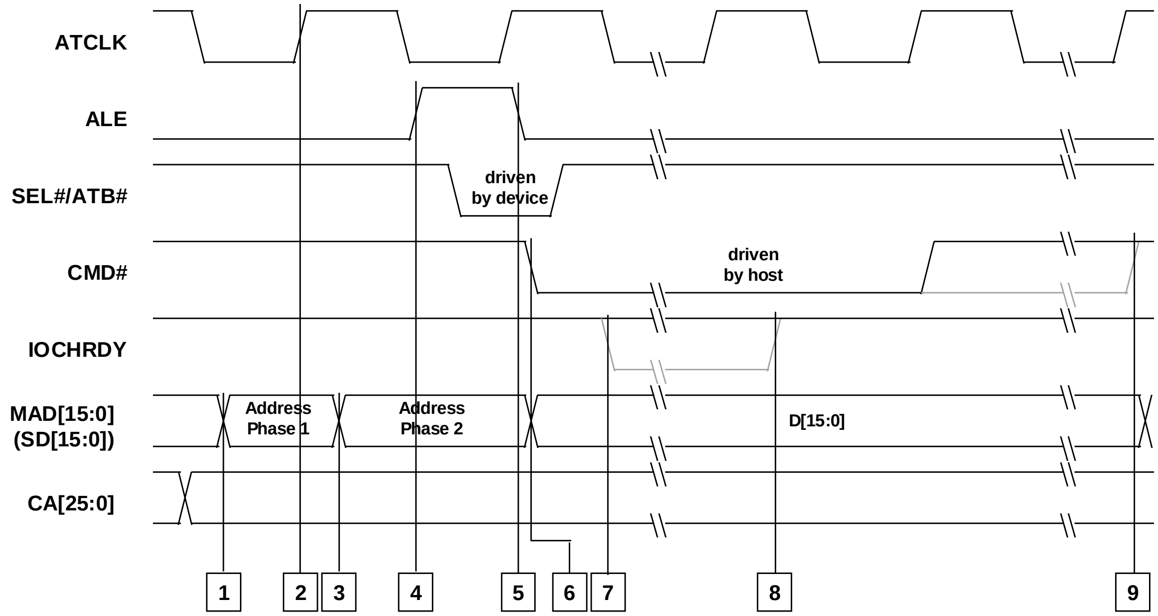
Figure A-1 Compact ISA Memory Cycle Operation, Fast CISA Timing*



*Cycle optionally extended by IOCHRDY shown in gray.

1. CISA host gets address from the CPU address lines and byte enable lines. The host then drives out A[23:10] + M/IO# on MAD[15:0] with M/IO# high (memory).
2. CISA peripheral device latches address and M/IO# on the rising edge of ATCLK and decodes the information.
3. Host drives out remaining address + Command on MAD[15:0].
4. Host asserts ALE. If cycle belongs to CISA peripheral device, it asserts SEL# and latches the address and command from MAD[15:0] on the rising edge of ALE. Device latches ISA# = 1 at this time.
5. Host and other CISA devices recognize the SEL# function of SEL#/ATB# by seeing ALE high when sampling SEL#/ATB# low on the rising edge of ATCLK. Host de-asserts ALE and stops driving address on this rising ATCLK edge.
6. For reads, the host tristates the MAD[15:0] buffers. For writes, it drives the write data onto MAD[15:0]. Host asserts CMD# synchronous to the rising edge of ATCLK and can optionally inhibit its MRD#/MWR# lines.
7. Cycle is 0 wait states as indicated by ISA# = 1. CISA peripheral device can bring IOCHRDY low asynchronously after CDM# goes active to extend the cycle.
8. Device brings IOCHRDY high synchronous to the falling edge of ATCLK to allow cycle completion.
9. Host de-asserts CMD# on the same rising edge where it samples IOCHRDY high.

Figure A-2 Compact ISA Memory Cycle Operation, Standard ISA Timing*



*Cycle optionally extended by IOCHRDY shown in gray.

1. CISA host gets address from the CPU address lines and byte enable lines. The host then drives out A]23:10] + M/IO# on MAD[15:0] with M/IO# high (memory).
2. CISA peripheral device latches address and M/IO# on the rising edge of ATCLK and decodes the information.
3. Host drives out remaining address + Command on MAD[15:0].
4. Host asserts ALE. If cycle belongs to CISA peripheral device, it asserts SEL# and latches the address and command from MAD[15:0] on the rising edge of ALE. Device latches ISA# = 0 at this time.
5. Host and other CISA devices recognize the SEL# function of SEL#/ATB# by seeing ALE high when sampling SEL#/ATB# low on the rising edge of ATCLK. Host de-asserts ALE and stops driving address on this rising ATCLK edge.
6. For reads, the host tristates the MAD[15:0] buffers. For writes, it drives the write data onto MAD[15:0]. Host asserts CMD# synchronous to the rising edge of ATCLK and can optionally inhibit its MRD#/MWR# lines.
7. Cycle is not zero wait states, as indicated by ISA# = 0. CISA peripheral device can bring IOCHRDY low asynchronously after CDM# goes active to extend the cycle further.
8. Device brings IOCHRDY high asynchronously to allow cycle completion.
9. Host de-asserts CMD# on the next rising edge of ATCLK after the rising edge ATCLK edge on which it samples IOCHRDY high.

A.2.2 I/O Cycle

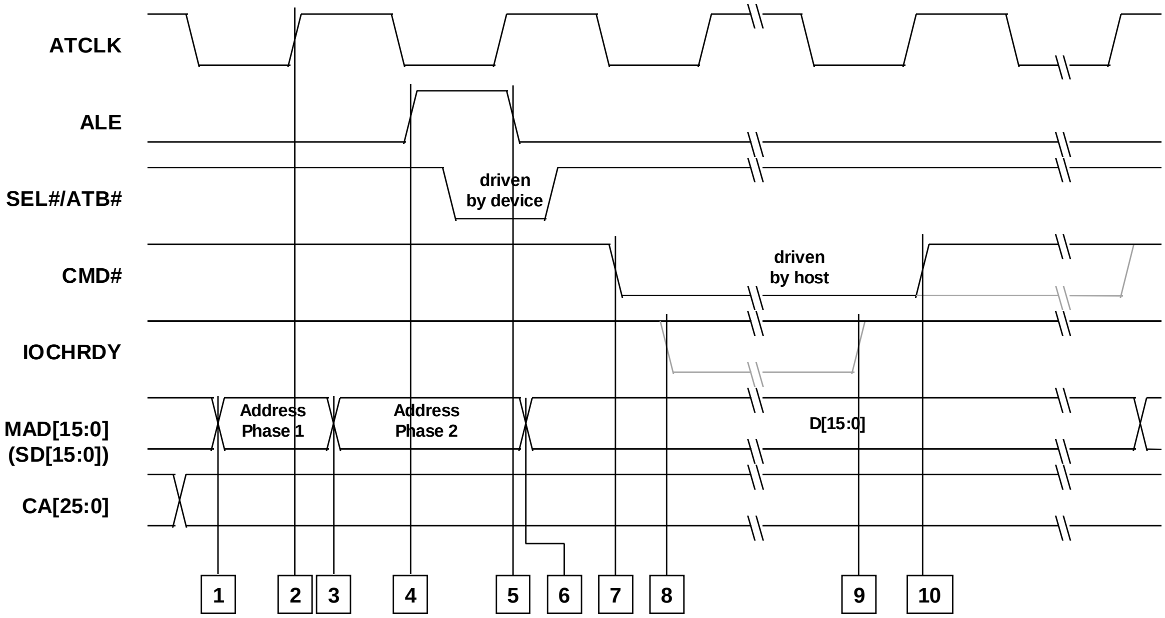
The MAD[15:0] bit meanings for each phase of an I/O cycle are shown below. The M/IO# bit is always 0, and the I/D# bit is always 1, for an I/O cycle.

The general structure of Compact ISA I/O cycles is shown in Figure A-3.

Table A-4 MAD Bits During I/O Cycles

Phase	MAD15	MAD14	MAD13	MAD12	MAD11	MAD10	MAD9	MAD8	MAD7	MAD6	MAD5	MAD4	MAD3	MAD2	MAD1	MAD0
1	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA15	SA14	SA13	SA12	SA11	SA10	I/D# = 1	M/IO# = 0
2	Same	Same	Same	Same	Same	Same	Same	Same	SA1	SA0	Same	Same	Same	ISA# = 0	SBHE#	W/R#
3	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

Figure A-3 Compact ISA I/O Cycle Operation*



*Cycle optionally extended by IOCHRDY shown in gray.

1. CISA host gets address from the CPU address lines and byte enable lines. The host then drives out A[15:2] + I/D# = 1 + M/IO# = 0 (I/O cycle).
2. CISA peripheral device latches address and M/IO# on the rising edge of ATCLK and decodes the information.
3. Host drives out remaining address + Command on MAD[15:0].
4. Host asserts ALE. If cycle belongs to CISA peripheral device, it asserts SEL# and latches the address and command from MAD[15:0] on the rising edge of ALE.
5. Host and other CISA devices recognize the SEL# function of SEL#/ATB# by seeing ALE high when sampling SEL#/ATB# low on the rising edge of ATCLK. Host de-asserts ALE and stops driving address on this rising ATCLK edge.
6. For reads, the host tristates the MAD[15:0] buffers. For writes, it drives the write data onto MAD[15:0].
7. Host asserts CMD# synchronous to the falling edge of ATCLK to run the command and can optionally inhibit its IOR#/IOW# lines.
8. Cycle is never zero wait state. CISA peripheral device can bring IOCHRDY low asynchronously after CDM# goes active, using standard ISA setup timing, to extend the cycle further. Note that if CISA peripheral device provides a bridge to another device (a PCMCIA slot, for example), the device on the secondary bus must be able to return IOCHRDY soon enough to meet setup timing on the CISA interface.
9. Device brings IOCHRDY high asynchronously to allow cycle completion.
10. Host de-asserts CMD# on the next falling edge of ATCLK after the rising edge ATCLK edge on which it samples IOCHRDY high.

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A.2.3 DMA on the CISA/ISA Bus

DMA operations are handled very specifically for CISA peripheral devices. Both CISA memory devices and CISA DMA devices can be involved in a DMA transfer, possibly at the same time. The CISA host must handle each situation.

The central consideration is that the CISA host must be able to distinguish between the DMA channels that are on the ISA bus and those that are on the CISA bus. This is a simple matter when the host also incorporates the DMA controller: because the host is responsible for latching the DRQ driveback information, it can determine on a cycle-by-cycle basis whether the DMA device being serviced is on CISA or on ISA according to whether it latched DRQ active for that channel from a CISA driveback cycle.

Because the host has this knowledge, the CISA DMA device does **not** need to assert SEL# on a DACK# cycle. The host already knows the cycle belongs to a CISA DMA device and does not need to see SEL# for the I/O portion of the cycle. This inhibition of SEL# is most important when a CISA memory device is responding to the memory portion of the cycle: the CISA memory device must respond as always with SEL#, and there would be contention (on deassertion) if the CISA DMA device asserted SEL# as well.

The host must foresee the following two situations.

- **DMA transfer between ISA DMA device and any memory device (system DRAM, ISA memory, or CISA memory) -** The host runs a standard CISA memory cycle (I/D# = 0, M/IO# = 1) along with the ISA memory-I/O cycle. If the selected memory is present on CISA, the device will respond to the access with SEL# as usual. The host **must** drop ALE if SEL# is returned.
- **DMA transfer between CISA DMA device and memory -** The host runs a CISA DACK# cycle (I/D# = 0, M/IO# = 0). If a CISA memory device claims this cycle it responds with SEL# as usual. The memory device can drive IOCHRDY low to extend the cycle if desired.

The CISA DACK# cycle is described below.

A.2.4 DACK# Cycle

The DACK# cycle is unique in that it has properties of a memory cycle but is directed to an I/O device. Basically, the DACK# cycle is a memory cycle whose address must be decoded by any CISA memory device on the bus. SBHE# and W/R# reference the memory device, not the I/O device; the I/O device must assume the opposite sense of W/R# for its portion of the cycle. Only the memory device responds with SEL#; the DMA (I/O) device never responds. The CMD# timing will be the wider pulse of MEMW#/IOR# or MEMR#/IOW#.

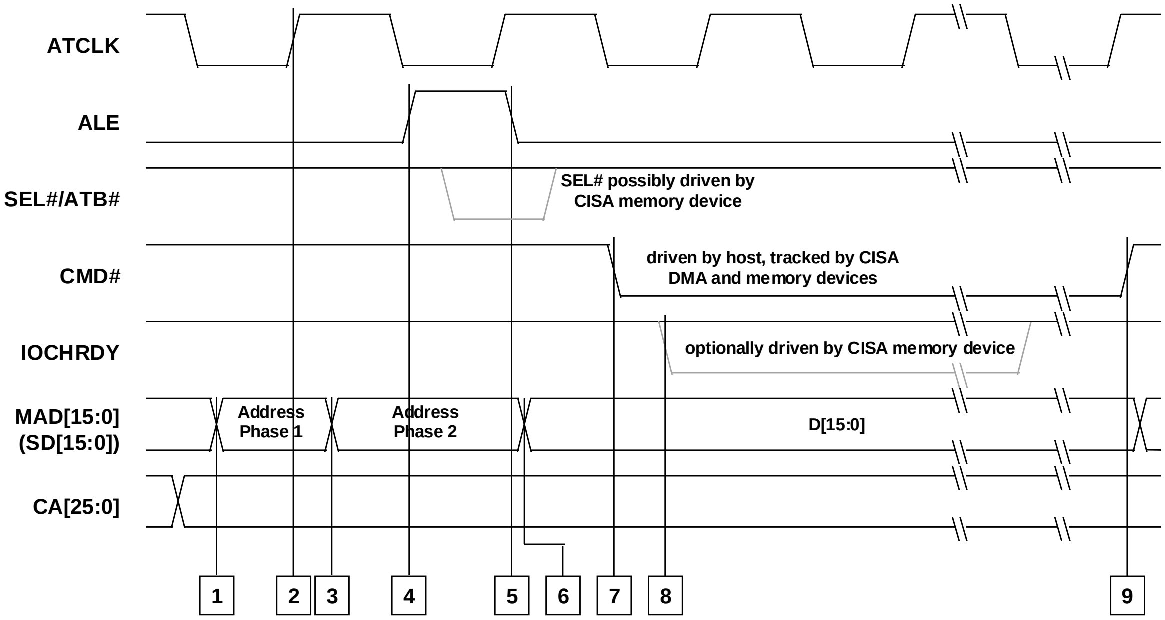
The MAD[15:0] bit meanings for each phase of a DMA acknowledge cycle are shown in Table A-5. The M/IO# bit is always 0, and the I/D# bit is always 0, for a DACK# cycle. DMX2-0 encode the number of the DACK#. For example, DMX2-0 = 010 indicate DACK2# active. TC is high if the DACK# is being returned with the Terminal Count indication. Note that there is no ISA# bit, since there is no fast cycle possible.

The general structure of Compact ISA DACK# cycles is shown in Figure A-4.

Table A-5 MAD Bits During DMA Acknowledge Cycles

Phase	MAD15	MAD14	MAD13	MAD12	MAD11	MAD10	MAD9	MAD8	MAD7	MAD6	MAD5	MAD4	MAD3	MAD2	MAD1	MAD0
1	SA23	SA22	SA21	SA20	SA19	SA18	SA17	SA16	SA15	SA14	SA13	SA12	SA11	SA10	I/D# = 0	M/IO# = 0
2	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	DMX2	DMX1	DMX0	TC	SBHE#	W/R#
3	SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

Figure A-4 Compact ISA DACK# Cycle Operation



1. CISA host gets address form the CPU address lines and byte enable lines. The host then drives out A[23:0] + I/D# = 0 + M/IO# = 0 (DACK# cycle).
2. CISA DAM device, and possibly CISA memory device, latches address and cycle type information on the rising edge of TACLK and decodes the information.
3. Host drives out remaining command information on MAD[15:0].
4. Host asserts ALE. CISA DMA device does not assert SEL# but latches the address and command from MAD[15:0] on the rising edge of ALE. Any CISA memory device present latches address and command, decodes them, and asserts SEL# if appropriate.
5. Host de-asserts ALE and stops driving address on this rising ATCLK edge. Note that in a normal ISA cycle the host would keep ALE high.
6. For DMA I/O read, the host tristates the MAD[15:0] buffers. For DMA I/O write, it drives the write data onto MAD[15:0].
7. Host asserts CMD# synchronous to the falling edge of ATCLK to run the command and is required to inhibit its IOR#/IOW# lines.
8. Only CISA memory devices can extend the cycle with IOCHRDY.
9. DACK# cycle is minimum 1.5 ATCLK. Host de-asserts CMD# synchronous to the rising edge of ATCLK.

A.2.5 Configuration Cycle

The CISA Configuration Cycle is a special cycle reserved for future expansion of CISA. The only configuration cycle currently defined is the Broadcast cycle; the only type of Broadcast cycle specified at this moment is the Stop Clock cycle.

The Stop Clock cycle indicates that the host will immediately put the CISA peripheral devices into a low-power mode in which they will no longer receive clocks. Therefore, the CISA peripheral device must enter into a state in which it can asynchronously signal that it needs the clocks restarted. CISA devices might need to generate an interrupt back to the system, which they cannot do if not receiving clocks.

The MAD[15:0] bit meanings for each phase of the Stop Clock configuration cycle are shown below.

In phase 1, the M/IO# bit is always 1, and the I/D# bit is always 1, for any configuration cycle. BRD is 1 to indicate a Broadcast cycle, and will always be zero for any other configuration cycle. The STP# bit is 0 to indicate a Stop Clock cycle, and will be 1 for all other cycles. Bits CC2:0 are the Clock Count bits that indicate to the CISA peripheral device how many rising clock edges to expect after CMD# goes high before the clock is actually stopped. The other bits of phase 1 are reserved and should not be decoded.

In phase 2, ISA# = 1 indicating that this will be a fast cycle. SBHE# = 0 to indicate 16 bits of data. W/R# = 1 because the Stop Clock Broadcast cycle is always a write cycle.

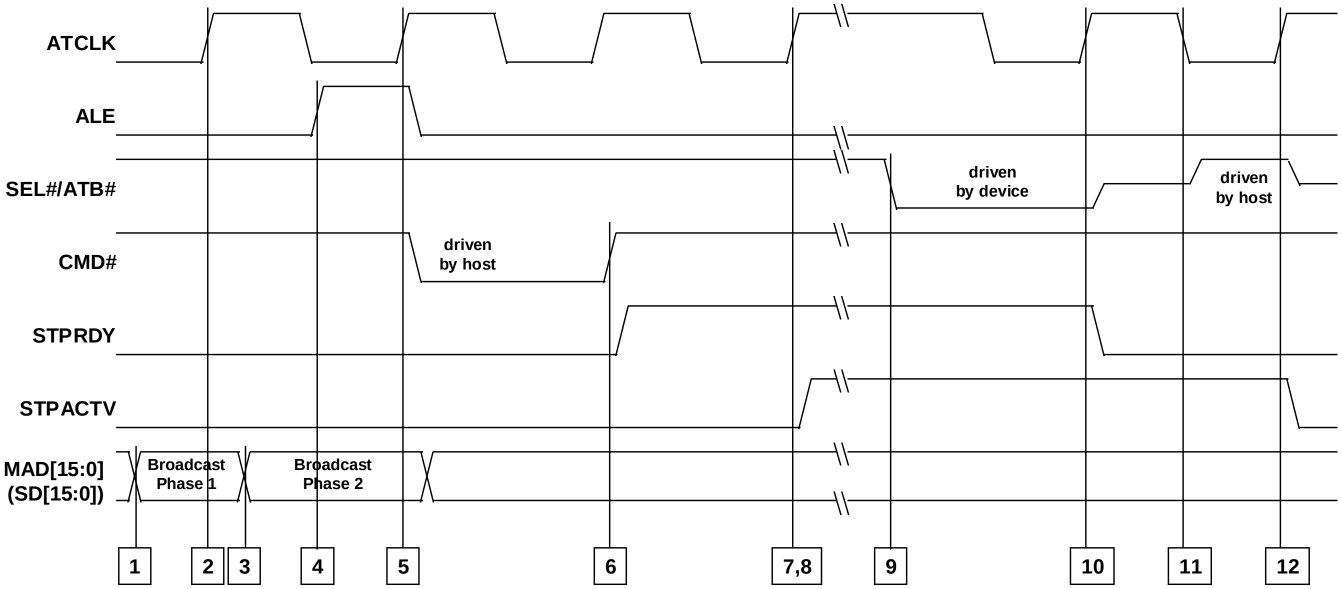
The data phase of the Stop Clock cycle contains no useful data and should not be latched.

The general structure of Compact ISA Broadcast cycles is shown in Figure A-5.

Table A-6 MAD Bits During Stop Clock Configuration Cycles

Phase	MAD15	MAD14	MAD13	MAD12	MAD11	MAD10	MAD9	MAD8	MAD7	MAD6	MAD5	MAD4	MAD3	MAD2	MAD1	MAD0
1	BRD = 1	STP# = 0	CC2	CC1	CC0	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	I/D# = 1	M/IO# = 1
2	Same	Same	Same	Same	Same	Same	Same	Same	Same	Same	Same	Same	Same	ISA# = 1	SBHE#	W/R# = 1
3	Same	Same	Same	Same	Same	Same	Same	Same	Same	Same	Same	Same	Same	Same	Same	Same

Figure A-5 Compact ISA Configuration Cycle Operation



This example describes the Broadcast configuration cycle

1. CISA host initiates the Configuration cycle; it is not generate form ISA commands. The host drives out BRD = 1 + I/D# = 1 + M/IO# = 0 (Broadcast configuration cycle).
2. CISA peripheral latches the command data on the rising edge of ATCLK and decodes the information.
3. Host drives out Clock Count, Stop Clock cycle indicator, and remaining command information on MAD[15:0].
4. Host asserts ALE. CISA devices latch clock count. CISA peripheral devices must NOT respond with SEL#.
5. Host asserts CMD# synchronous to the rising edge of ATCLK to run the command. The Broadcast configuration cycle is always zero wait states so it completes in one ATCLK.
6. After the host de-asserts CMD#, the CISA peripheral device is internally in STPRDY state.
7. After the number of clocks specified by CC[2:0], the host stops the clock in its high state. In the example, CC[2:0] = 001 (the minimum allowed) so the host will stop the clock on the next rising ATCLK edge. Each additional count requires the host to wait one more clock.
8. The CISA peripheral device is also counting clocks while in STPRDY state. On the specified ATCLK edge the device is in STPACTV state. In STPACTV state, the CISA peripheral device gives SEL#/ATB# a third meaning: CLKRUN#. The device can assert CLKRUN# asynchronously at any time while in this mode to get the host to restart its clocks.
9. CISA peripheral device asserts CLKRUN# (SEL#/ATB#) on receipt of an interrupt to restart the clocks.
10. On next rising ATCLK clock edge, CISA peripheral device de-asserts CLKRUN# (SEL#/ATB#) but must not drive it high. Device has left STPRDY state but is still in STPACTV state and cannot initiate or respond to any cycle.
11. On next falling ATCLK edge, the host drives SEL#/ATB# high for ½ ATCLK.
12. On next rising ATCLK edge, the host stops driving SEL#/ATB#. The CISA peripheral device leaves STPACTV state on this clock edge and can either generate an interrupt driveback cycle or can respond to cycles from the host.

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A.3 Interrupt and DMA Request Drive-Back

Compact ISA provides the signal SEL#/ATB# to give the CISA peripheral device limited ownership of the bus. The SEL#/ATB# signal acts as ATB# (AT backoff) when asserted with ALE low. When the device asserts ATB# to the host, the host inhibits further AT bus operations and asserts the CMD# line to the CISA peripheral device to acknowledge that the device now owns the bus. The peripheral device can only drive two types of information onto the bus: interrupt requests and DMA requests.

Figure A-6 illustrates the synchronous IRQ/DRQ driveback cycle.

A.3.1 Interrupt Requests

To drive interrupt requests, the CISA peripheral device drives the MAD[15:0] lines low for each IRQ line it wishes to assert. The host side IRQ generation circuitry samples ATB# and CMD# active on the rising ATCLK edge and latches the IRQ information on MAD[15:0].

The IRQ generation circuitry, whether external or built into the host, determines how to treat IRQ information. For pulse-type interrupts it could latch the IRQs and enable tristate buffers to drive the lines low for 1-3 ATCLKs, for example.

A.3.2 DMA Requests

The CISA device must always precede the DRQ drive-back cycle with an IRQ drive-back cycle, even if no IRQs have changed state.

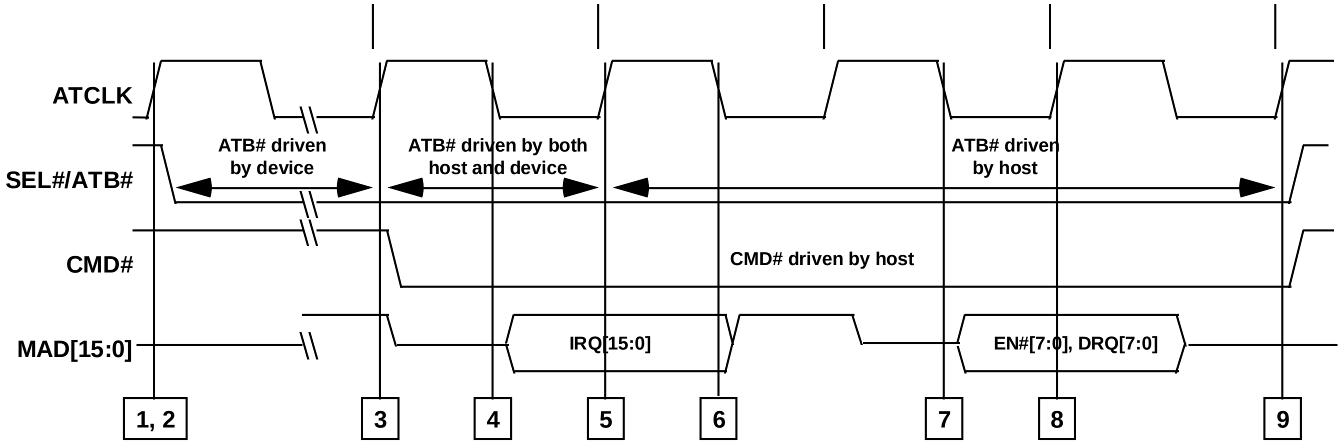
To make DMA requests, the CISA peripheral device drives the MAD[15:8] lines low for each DRQ it wishes to change. The device then sets the state of each MAD[7:0] line to correspond to the DRQ state desired. The host side DRQ generation circuitry samples ATB# and CMD# active on the next rising ATCLK edge after the edge on which IRQs were sampled, and latches the DRQ information on MAD[7:0] for the channels selected on MAD[15:8].

The desired DMA request line states are latched by the host and will remain in that state until cleared by another DRQ drive-back cycle. This scheme allows both DMA single transfer and DMA block transfer modes to be used. The CISA peripheral device must assert SEL#/ATB# immediately any time a DRQ line changes state (assuming the current cycle is finished). The CISA host, in turn, must immediately deassert all DRQ inputs to its DMA controller until the drive-back cycle is complete.

Table A-7 IRQ/DRQ Drive Back Cycle

Phase	MAD15	MAD14	MAD13	MAD12	MAD11	MAD10	MAD9	MAD8	MAD7	MAD6	MAD5	MAD4	MAD3	MAD2	MAD1	MAD0
IRQ	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
DRQ	EN7#	EN6#	EN5#	Rsvd	EN3#	EN2#	EN1#	EN0#	DRQ7	DRQ6	DRQ5	Rsvd	DRQ3	DRQ2	DRQ1	DRQ0

Figure A-6 Compact ISA Interrupt and DMA Request Drive-Back Cycle



1. CISA Peripheral device must sample SEL#/ATB# and CMD# high, and ALE low, on TWO consecutive rising edges of ATCLK.
2. CISA peripheral device asserts ATB# on rising edge of ATCLK to request AT backoff. If host was starting a cycle and was about to assert ALE on the next falling edge of ATCLK, it must abort the cycle and retry it later. Even if host is busy and cannot respond to drive back request immediately, it inhibits initiation of all I/O and DMA operations (EOI to PCI is blocked, for example).
3. As soon as AT bus operations have been completed and bus is available, host drives MAD[15:0] high for ½ ATCLK from a falling edge of ATCLK, then asserts CMD# after the next rising edge of ATCLK. The host drives ATB# low at this time.
4. CISA peripheral device(s) can drive interrupt data onto bus on next falling edge of ATCLK, driving low only those lines with IRQ activity and not actively driving high the other lines. In this way, multiple CISA devices can drive the lines in parallel.
5. Host IRQ generation circuitry uses rising edge of ATCLK, qualified by ATB# and CMD# low, to latch IRQs. The CISA device stops driving ATB# at this time. The host controls ATB# throughout the rest of the cycle.
6. CISA peripheral device drives any MAD[15:-0] lines it was driving low high for ½ ATCLK, then tristates the lines for ½ ATCLK.
7. CISA peripheral device drives DRQ information onto MAD[7:0] and at the same time drives low the corresponding lines MAD[15:8] to indicate which DRQ channels have a status change to be transferred.
8. Host DRQ generation circuitry uses next rising edge of ATLCK, qualified by ATB# and CMD# low AND previous IRQ cycle, to latch DRQs. The host DRQ generation circuitry ORs the DRQs with other system DRQs.
9. Host de-asserts CMD# and ATB# on rising edge of ATCLK.

A.4 Performance Control

Compact ISA performance is comparable with that of 16-bit ISA bus peripheral devices. In its simplest implementation, the CMD# signal is simply an AND of MRD#, MWR#, IOR#, and IOW# from the standard AT controller state machine.

Memory cycles are always assumed to be **zero wait state**. The CISA host detects a NOWS# command every time SEL# is generated. The CISA peripheral device can use its IOCHRDY line to extend the cycle and override the NOWS# status. All of this functionality is consistent with standard ISA operation.

I/O cycles cannot be made zero-wait-state cycles on the ISA bus, so by default are not zero-wait-state cycles on the CISA bus. However, performance improvement is possible if the CMD# duration is shortened to one ATCLK. Future PCMCIA I/O devices may be able to complete their cycles this quickly, for example. For zero-wait-state CISA I/O operation, the cycle timing would have to change from the standard ISA timing. The host can implement fast CISA timing as an option. However, all CISA slave devices are **required** to be able to accept fast CISA timing.

Fast CISA timing on the host side is defined as follows. If the CISA host is driving CMD# as derived from the logical AND of ISA command lines IOR#, IOW#, MRD#, and MWR#, it sets ISA# = 0 to indicate that the CISA peripheral device must assume ISA timing. If the host is capable of performing fast CISA cycles, it can set ISA# = 1. In this case, the CISA peripheral device must deassert IOCHRDY early to lengthen cycles.

Fast CISA timing on the device side is defined as follows. If the CISA host drives the ISA# bit low, the CISA peripheral device assumes normal ISA timing for CMD# and IOCHRDY. If the CISA host drives ISA# high, the CISA peripheral device must drop IOCHRDY low immediately upon receiving CMD# to lengthen the cycle; this is different from ISA timing.

The CISA peripheral device will have a programmable option to determine how IOCHRDY is deasserted. By default, the device might drop IOCHRDY on every cycle. For the example of a PCMCIA controller on the CISA bus, only when a fast PCMCIA card is inserted (as indicated in the CIS header of the card) would Card Services be allowed to enable the fast CISA timing option on the CISA peripheral device side.

A.5 Compatibility and Host Responsibilities

Compact ISA does **not** interfere with standard ISA operations or limit compatibility. This statement can be made with only the following restrictions:

- No device can drive the SD bus between ISA cycles. Devices capable of driving the SD bus must stay tristated at this time.
- ATCLK can be stopped only after a Stop Clock Broadcast configuration cycle. Slower-than-standard clock speeds are allowed if interrupt latency is not an issue.
- ISA bus masters cannot access CISA devices. Standard ISA masters are simply ignored by CISA devices since these masters cannot generate CMD# and so cannot run a CISA cycle. ISA bus masters can still take bus control and communicate with other ISA peripherals. CISA interrupt latency may be an issue if a bus master prevents the CISA host from responding to ATB# for an interrupt driveback cycle.
- No CISA bus master capability is currently defined. However, the presence of the SEL#/ATB# signal and its AT backoff feature leave open the possibility of future bus master capabilities.
- On receipt of an ATB# request, the CISA host must immediately inhibit all system DRQ activity (possibly by deasserting all DRQs to the DMA controller) until the drive-back cycle is complete. Otherwise, unwanted DMA cycles could occur.

A.6 Shared Speaker Signal Support (Optional)

Compact ISA provides a new scheme for the digital speaker output signal common to PCs and PCMCIA controllers. This scheme allows all digital audio outputs to be tied together without the XOR logic usually required.

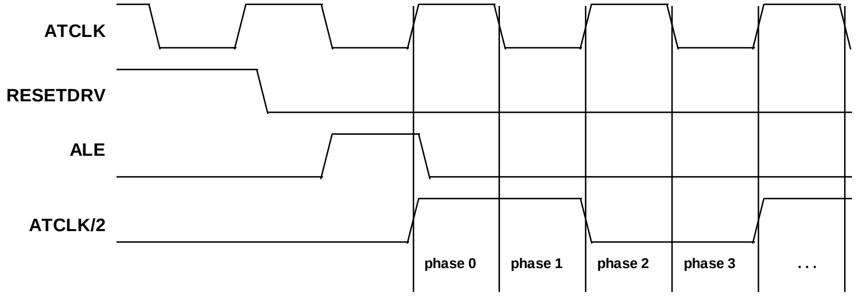
The standard specification for the speaker data output is a signal driven in both the low-to-high and high-to-low directions. The output cannot simply be respecified as open-collector, since there is no guarantee that software will leave the speaker output line from the system chipset in a high or tristated condition. If it leaves the signal driven low, no other open-collector devices connected on the line could toggle the signal. Moreover, open collector outputs tend to consume excessive power.

Compact ISA provides an efficient solution to the problem as described in the following sections.

A.6.1 Initial Synchronization

All CISA slave devices must tristate their SPKR outputs at hard reset time and remain tristated until individually enabled. On the first ALE generated by the host, all participating CISA devices will synchronize to ATCLK and derive the signal ATCLK/2 that is in phase as shown in Figure A-7. Four distinct phases, 0 through 3, are the result. CISA slave SPKR outputs are still tristated at this point.

Figure A-7 Synchronizing to ATCLK at 1st ALE



A.6.2 SPKR Sharing During Active Mode

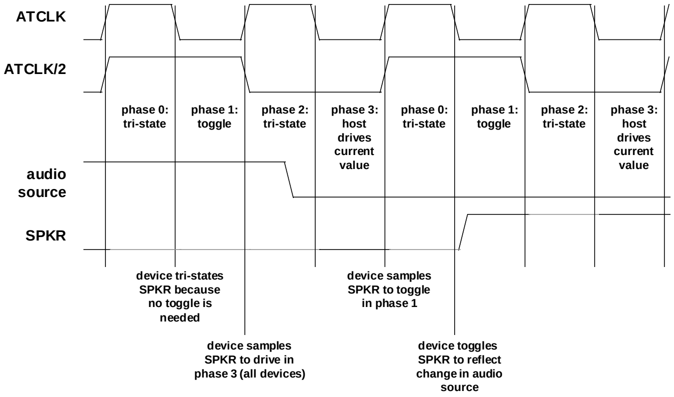
The activities performed in each phase by the CISA host and the CISA slaves are as given in Table A-8.

Figure A-8 illustrates the SPKR handling requirements.

Table A-8 SPKR Sharing During Active Mode

Phase	Slave	Host
On the rising ATCLK edge starting phase 0	Sample the state of SPKR.	Sample the state of SPKR. Tristate SPKR output.
During phase 0:	Maintain SPKR output tristated (as it was from previous phase).	Maintain SPKR output tristated.
On the falling ATCLK edge starting phase 1:	Sample digital audio source input.	
During phase 1:	If digital audio source input sampled on ATCLK edge has changed state since the previous phase 1 in which it was sampled, toggle SPKR. SPKR is toggled by driving the opposite of the SPKR value sampled in phase 0 onto the SPKR output.	
On the rising ATCLK edge starting phase 2:	Tristate SPKR output.	Tristate SPKR output. Sample the state of SPKR.
During phase 2:	Slave and host: Maintain SPKR output tristated.	
On the falling ATCLK edge starting phase 3:	No activity on this edge.	Drive SPKR pin to the value of SPKR sampled in phase 2.
During phase 3:	Maintain SPKR output tristated (as it was from previous phase).	Maintain SPKR output driven.

Figure A-8 Shared SPKROUT Signal Management



A.6.3 SPKR Sharing During Stop Clock Mode

During Stop Clock mode, CISA devices handle SPKR as follows.

Slave: Tristate SPKR. Referring to Figure A-5, the exact period during which CISA slaves keep SPKR tristated is defined as the period during which both STPACTV and STPRDY are high.

Host: Drive or tristate SPKR. It is recommended that the host drive SPKR low.

Note that even while CISA slave devices are in Stop Clock mode, they must remain synchronized to the correct phase of ATCLK. They do **not** resynchronize on the next ALE.

A.6.4 Audio Output Circuit Recommendations

The SPKR output must **never** be connected directly to a speaker or other low-impedance transducer. The shared SPKR implementation depends on an R-C time constant large enough that the signal will never change its level any appreciable amount across a period of 1.5 ATCLKs, the maximum number of clocks for which no device will be driving the SPKR line.

Three ATCLKs last for approximately 188ns. The R-C time constant of the design must be significantly larger than this value. Connecting an 8 ohm speaker directly would cause the line to begin a transition when it was tristated. Therefore, either capacitive coupling or an amplifier circuit with a high-impedance input is recommended.

A.7 Automatic Voltage Threshold Detection

Compact ISA devices are intended to work on either a traditional 5.0V ISA bus or on a local 3.3V ISA bus. Compact ISA designs are very power-conscious, so using external strap options on each CISA device to select the input buffer threshold may not be the best option.

Therefore, the Compact ISA host is required to use the ALE pin at reset to indicate the ISA bus voltage to CISA slaves. The correspondence is as follows.

- For a 5.0V ISA bus, the host must assert the ALE signal **high** when RSTDRV goes high, and must keep it asserted for at least 1/2 ATCLK and at most 1 ATCLK after RSTDRV goes low.
- For a 3.3V ISA bus, the host must keep the ALE signal **low** when RSTDRV goes high, and must maintain ALE low for at least 1/2 ATCLK after RSTDRV goes low.

This performance is **required** for CISA hosts, but CISA slave devices are not required to use the feature.

Sales Information

HEADQUARTERS:

OPTi Inc.
888 Tasman Drive
Milpitas, CA 95035
tel: 408-486-8000
fax: 408-486-8011

SALES OFFICES:

Japan

OPTi Japan KK
Murata Building 6F, 2-22-7
Ohhashi Meguro-ku
Tokyo 153, Japan
tel: + 81-3-5454-0178
fax: + 81-3-5454-0168

Taiwan

OPTi Inc.
9F, No 303, Sec 4, Hsin Yih Road
Taipei, Taiwan, ROC
tel: + 886-2-325-8520
fax: + 886-2-325-6520

United Kingdom & Europe

OPTi Inc.
Bicester Business Center
Market Court, Victoria Road
Bicester, Oxon OX6 7QB
U.K.
tel: + 44-1-869-321-622
fax: + 44-1-869-241-448

United States

OPTi Inc.
8 Corporate Park, Ste. #300
Irvine, CA 92714-5117
tel: 714-838-0589
fax: 714-838-9753

OPTi Inc.
4400 N. Federal Highway, Ste. #120
Boca Raton, FL 33431
tel: 407-395-4555
fax: 407-395-4554

OPTi Inc.
20405 State Highway 249, Ste. #220
Houston, TX 77070
tel: 713-257-1856
fax: 713-257-1825

REPRESENTATIVES:

United States

Alabama/Mississippi

Concord Component Reps
190 Line Quarry Rd., Ste. #102
Madison, AL 35758
tel: 205-772-8883
fax: 205-772-8262

California - Southern

Jones & McGeoy Sales
5100 Campus Dr., Ste. #300
Newport Beach, CA 92660
tel: 714-724-8080
fax: 714-724-8090

Florida

Engineered Solutions Ind., Inc.
1000 E. Atlantic Blvd., Ste. #202
Pompano Beach, FL 33060
tel: 305-784-0078
fax: 305-781-7722

Georgia

Concord Component Reps
6825 Jimmy Carter Blvd., Ste. #1303
Norcross, GA 30071
tel: 404-416-9597
fax: 404-441-0790

Illinois

Micro-Tex, Inc.
1870 North Roselle Rd., Ste. #107
Schaumburg, IL 60195-3100
tel: 708-885-8200
fax: 708-885-8210

Massachusetts

S-J New England
40 Mall Road, Suite 202
Burlington, MA 01803
tel: 617-272-5552
fax: 617-272-5515

Michigan

Jay Marketing
44752 Helm Street., Ste. A
Plymouth, MI 48170
tel: 313-459-1200
fax: 313-459-1697

New Jersey

S-J Associates, Inc.
131-D Gaither Dr.
Mt. Laurel, NJ 08054
tel: 609-866-1234
fax: 609-866-8627

New York

S-J Associates, Inc.
265 Sunrise Highway
Rockville Centre, NY 11570
tel: 516-536-4242
fax: 516-536-9638

North & South Carolina

Concord Component Reps
10608 Dunhill Terrace
Raleigh, NC 27615
tel: 919-846-3441
fax: 919-846-3401

Ohio/W. Pennsylvania

Lyons Corp.
4812 Fredrick Rd., Ste. #101
Dayton, OH 45414
tel: 513-278-0714
fax: 513-278-3609

Lyons Corp.
4615 W. Streetsboro
Richfield, OH 44286
tel: 216-659-9224
fax: 216-659-9227

Lyons Corp.
248 N. State St.
Westerville, OH 43081
tel: 614-895-1447
fax: Same

Texas

Axxis Technology Marketing, Inc.
100 Hester Hollow
Georgetown, TX 78628
tel: 512-930-0075
fax: Same

Virginia

S-J Associates, Inc.
900 S. Washington St., Ste. #307
Falls Church, VA 22046
tel: 703-533-2233
fax: 703-533-2236

Wisconsin

Micro-Tex, Inc.
22660 Broadway, Ste. #4A
Waukesha, WI 53186
tel: 414-542-5352
fax: 414-542-7934

International

Australia

Braemac Pty. Ltd.
Unit 6, 111 Moore St., Leichhardt
Sydney, 2040 Australia
tel: 61-2-550-6600
fax: 61-2-550-6377

China

Legend Electronic Components. Ltd.
Unit 413, Hong Kong Industrial
Technology Centre
72 Tat Chee Avenue
Kow loon Tong, Hong Kong
tel: 852-2776-7708
fax: 852-2652-2301

France

Tekelec Airtronic, France
5, Rue Carle Vernet
92315 Sevres Cedex
France
tel: 33 (1) 46-23-24-25
fax: 33 (1) 45-07-21-91

India

Spectra Innovation
Unit S-822 Manipal Centre
47 Dickenson Road
Bangalore 560 042
Karnataka, India
tel: 91-80-558-8323/3977
fax: 91-80-558-6872

Korea

Woo Young Tech Co., Ltd.
5th Floor Koami Bldg
13-31 Yoido-Dong
Youngdeungpo-Ku
Seoul, Korea
tel: (02) 369-7099
fax: (02) 369-7091

Singapore

Instep Microsolutions Pte Ltd.
629 Aljunied Road #05-15
Cititech Industrial Building
Singapore 1438
tel: 65-741-7507
65-741-7530
fax: 65-741-1478

South America

Uniao Digital
Rua Georgia, 69-Brooklin Novo
04559-010-Sao Paulo-Brazil
tel: 55-11-536-4121
fax: 55-11-533-6780

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OPTi Inc.
888 Tasman Drive
Milpitas, CA 95035
Tel: (408) 486-8000
Fax: (408) 486-8001
WWW: http://www.opti.com/