

FireLink/FireBlast PCI-to-USB Bus Bridges

1.0 Features

Features of FireLink

- Pin compatibility with the CMD[®] USB0670 PCI-USB Controller
- Adds optional I²C interface if full pin compatibility is not required
- Implements CLKRUN# pin to support low power portable applications
- Supports OPTi IRQ Driveback Cycle to improve pin utilization and increase interrupt selection flexibility
- Core operates at either 5.0V or 3.3V, strap-selectable
- Two package types available:
 - 100-pin LQFP (Low-profile Quad Flat Pack)
 - 100-pin QFP (Quad Flat Pack)

Additional Features of FireBlast

- Pin-compatible upgrade to FireLink
- Integrates digital audio controller
- Connects to either OPTi compact 28-pin codec or AC97-standard 44-pin codec

- · Supports both one-wire and two-wire serial IRQ option
- Offers push-button volume control
- Provides MIDI interface

2.0 Overview

This document describes OPTi's FireLink (82C861) and Fire-Blast (82C871) PCI-to-USB Bus Bridges. It details:

- 1. How FireLink can be used as a direct replacement for the CMD USB0670.
- 2. The advantages of FireLink over the USB0670 and how it can be used to allow for future upgrading to FireBlast.
- 3. The additional benefits that FireBlast can bring to a system design.

Figure 2-1 shows a block diagram when FireLink is used in a in a CMD-based system.

To help show the advantages of FireLink over the CMD part and the ease of upgrading to FireBlast, Figure 2-2 shows how the pins have been functionally grouped.



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Figure 2-2 Functional Grouping



Key: The <signal names> denote the additional functions of the pin if FireBlast is used in a system.

FireLink is a pin-compatible replacement for the CMD USB device, even though some of FireLink's pins are called out as NIC (No Internal Connection).

Pin 46 (CLKRUN#) can be a connected to VCC if FireLink in a CMD-based system.



2.1 FireLink

FireLink (82C861) is a direct pin-compatible upgrade for the CMD USB0670 USB Controller. Like the CMD part, FireLink implements two independent USB ports. FireLink additionally offers the following possibilities for feature enhancement by minor changes to the USB0670 pinout.

- Two-wire I²C interface, ideal for communication with SO-DIMM DRAM to determine the DRAM type and capacity.
- CLKRUN# pin, which allows the host chipset to keep the part in a very low power state most of the time. Start-up latency from this state is negligible.
- The pinout of FireLink is predisposed for later substitution by the FireBlast chip, which incorporates Sound Blastercompatible audio.
- By utilizing the built-in IRQ driveback logic with OPTi host chips, pins can be freed up so that provisions can be made to connect to the PC card zoomed video port.

Figure 2-3 shows a block diagram which incorporates the feature enhancements that FireLink has over the CMD part.



Figure 2-3 FireLink Block Diagram



2.2 FireBlast

FireBlast (82C871) can be substituted for the FireLink part to allow an efficient upgrade path to PCI-based audio. It is also

possible to use FireBlast in a stand-alone application. Figure 2-4 shows a block diagram for FireBlast.

Figure 2-4 FireBlast Block Diagram





3.0 Signal Definitions

3.1 Terminology/Nomenclature Conventions

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms "assertion" and "negation" are used extensively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signals. The term "assert", or "assertion" indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term "negate", or "negation" indicates that a signal is inactive.

The tables in this section use several common abbreviations. Table 3-1 lists the mnemonics and their meanings. Note that TTL/CMOS/Schmitt-trigger levels pertain to inputs only. Outputs are driven at CMOS levels.

Table 3-1	Signal Definitions Legend
Mnemonic	Description
Analog	Analog-level compatible
CMOS	CMOS-level compatible
Dcdr	Decoder
Ext	External
G	Ground
1	Input
Int	Internal
1/0	Input/Output
Mux	Multiplexer
NIC	No Internal Connection
0	Output
OD	Open drain
Р	Power
PD	Pull-down resistor
PU	Pull-up resistor
S	Schmitt-trigger
S/T/S	Sustain Tristate
ΠL	TTL-level compatible



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Key: Pins that are shaded black highlight the pin differences between FireLink and FireBlast. The <signal names> denote the additional functions of the pin if FireBlast is used in a system.

FireLink is a pin-compatible replacement for the CMD USB device, even though some of FireLink's pins are called out as NIC (No Internal Connection).

Pin 46 (CLKRUN#) can be a connected to VCC if FireLink is used in a CMD-based system.

Note: Figure 3-1 shows a pin diagram of the 82C861/82C871 packaged in an LQFP (Low-profile Quad Flat Pack, square). The devices are also available in a QFP (Quad Flat Pack, rectangular). The pin assignment remains the same each in package except for pin 53. If the QFP is chosen, the assignment for pin 53 is NIC.

Refer to Section 7.0, "Mechanical Package Outlines" for details regarding packaging.



Pin	Signal	Name				
No.	FireLink	FireBlast				
1	NIC	LR2				
2	A	02				
3	AĽ	01				
4	A	00				
5	GI	١D				
6	USB	CLK				
7	VC	xc				
8	NIC	VOLUP				
		SIN#				
9	PWF	ION1				
10	PWR	FLT1				
11	PWRGD1	PWRGD1				
		VOLDN				
		SOUT#				
12	VC	C3				
13	VE	01+				
14	VC	VD1-				
15	G	GND				
16	G	GND				
17	VC	C3				
18	V	VD2+				
19	V	VD2-				
20	G	ND				
21	TESTO	TEST0				
	I2CCLK	I2CCLK				
		RXD				
22	PWRGD2	PWRGD2				
		IRQSER				
		SPKRIN				
23	PWF	RFLT2				
24	PW	RON2				
25	TEST1	TEST1				
	I2CDATA	I2CDATA				
		TXD				
26	VCC	C_ISA				
27	IRQ1	IRQ1				
		ZVSDI				
28	IRQ12	IRQ12				
		ZVSDO				

Table 3-2 Numerical Pin Cross-Reference List

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Din	Signal Name						
No.	FireLink	FireBlast					
29	SMI#	SMI#					
		ZVFSYNC					
30	INTA#	INTA#					
		ZVSCLK					
31	RES	SET#					
32	PCI	CLK					
33	GI	ND					
34	V	cc					
35	GN	IT#					
36	RE	Q#					
37	AC	031					
38	AC	030					
39	A	029					
40	G	ND					
41	V	cc					
42	A	028					
43	A	AD27					
44	A	AD26					
45	A	AD25					
46	CLK	CLKRUN#					
47	G	GND					
48	A	AD24					
49	C/E	C/BE3#					
50	ID	IDSEL					
51	A	AD23					
52	A	D22					
53	LQFF	P = VCC					
	QFP	= NIC					
54	G	ND					
55	A	D21					
56	A	D20					
57	A	D19					
58	A	D18					
59		ND					
60	V						
61	A	D17					
62	A	D16					
63	C/	BE2#					
64	FRAME#						

	Signal Name					
Pin						
NO.	FIRELINK	FireBlast				
65	V	20				
66	GI	ND				
67	IRC	DY#				
68	TRU	DY#				
69	DEV	SEL#				
70	STO	DP#				
71	PEI	R#				
72	GI	ND				
73	NIC	SDO				
74	NIC	SDI				
75	SE	RR#				
76	P	AR				
77	C/E	E1#				
78	A	015				
79	A	014				
80	G	ND				
81	V	VCC				
82	AI	AD13				
83	A	AD12				
84	A	D11				
85	G	ND				
86	AI	AD10				
87	A	AD9				
88	A	D8				
89	C/I	3E0#				
90	G	ND				
91	NIC	FSYNC				
92	V	CC				
93	A	\D7				
94	A	ND6				
95	A	D5				
96	G	ND				
97	NIC	SCLK				
98	V	/CC				
99	ļ A	AD4				
100	AD3					



3.2 Signal Descriptions

In the tables that follow, <signal name> applies only to FireBlast.

Signal Name	Pin No.	Pin Type	Signal Description
PCICLK	32	I	PCI Clock: This input provides timing for all cycles on the host PCI bus; normally 33MHz. All other PCI signals are sampled on the rising edge of PCLK (timing parameters refer to this edge).
USBCLK	6	I	USB Clock: This input provides timing for USB data signals; normally 48MHz
RESET#	31	0	Reset: If RESET# is asserted for a minimum of 1µs, it causes the 82C861/ 82C871 to enter its default state (all registers are set to their default values).
			AD[31:0], C/BE[3:0]#, and PAR are always driven low by the 82C861/82C871 syn- chronously from the leading edge of RESET# and are always tristated from the trailing edge of RESET#.
			FRAME#, IRDY#, TRDY#, STOP#, and DEVSEL# are tristated from the leading edge of RESET# and remain so until driven as either a master or slave by the 82C861/82C871.
			RESET# may be asynchronous to PCLK when asserted or negated, however, negation must occur with a clean, bounce-free edge.

3.2.1 Clock and Reset Interface Signals

3.2.2 PCI Bus Interface Signals

Signal Name	Pin No.	Pin Type	Signal Description
AD[31:0]	37:39, 42:45, 48, 51, 52, 55:58, 61, 62,	1/O	Address and Data Lines 31 through 0: This bus carries the address and/or data during a PCI bus cycle. A PCI bus cycle has two phases - an address phase which is followed by one or more data phases. During the initial clock of the bus cycle, the AD bus contains a 32-bit physical byte address. AD[7:0] is the least significant byte (LSB) and AD[31:24] is the most significant byte (MBS). After the first clock of the cycle, the AD bus contains data.
	78, 79, 82:84, 86:88,		When the 82C861/82C871 is the target, AD[31:0] are inputs during the address phase. For the data phase(s) that follow, the 82C861/82C871 may supply data on AD[31:0] in the case of a read or accept data in the case of a write.
	93.95, 99, 100, 2:4		When the 82C861/82C871 is the master, it drives a valid address on AD[31:2] dur- ing the address phase, and drives write or accepts read data on AD[31:0] during the data phase. As a master, the 82C861/82C871 always drives AD[1:0] low.
C/BE[3:0]#	49, 63, 77, 89	I/O	Bus Command and Byte Enables 3 through 0: These signals provide the com- mand type information during the address phase and carry the byte enable infor- mation during the data phase. C/BE0# corresponds to byte 0, C/BE1# to byte 1, C/BE2# to byte 2, and C/BE3# to byte 3.
			If the 82C861/82C871 is the initiator of a PCI bus cycle, it drives C/BE[3:0]#. When it is the target, it samples C/BE[3:0]#.



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Signal Name	Pin No.	Pin Type	Signal Description
PAR	76	0	"Even" Parity: The 82C861/82C871 calculates PAR for both the address and data phases of PCI cycles. PAR is valid one PCI clock after the associated address or data phase, but may or may not be valid for subsequent clocks. It is calculated based on 36 bits - AD[31:0] plus C/BE[3:0]#. "Even" parity means that the sum of the 36 bit values plus PAR is always an even number, even if one or more bits of C/BE[3:0]# indicate invalid data.
FRAME#	64	I/O (s/t/s)	Cycle Frame: This signal is driven by the current PCI bus master to indicate the beginning and duration of an access. The master asserts FRAME# at the beginning of a bus cycle, sustains the assertion during data transfers, and then negates FRAME# in the final data phase.
			FRAME# is an input when the 82C861/82C871 is the target and an output when it is the initiator.
			FRAME# is tristated from the leading edge of RESET# and remains tristated until driven as either a master or slave by the 82C861/82C871.
IRDY#	67	I/O (s/t/s)	Initiator Ready: IRDY#, along with TRDY#, indicates whether the 82C861/ 82C871 is able to complete the current data phase of the cycle. IRDY# and TRDY# are both asserted when a data phase is completed.
			During a write, the 82C861/82C871 asserts IRDY# to indicate that it has valid data on AD[31:0]. During a read, the 82C861/82C871 asserts IRDY# to indicate that it is prepared to accept data.
			IRDY# is an input when the 82C861/82C871 is a target and an output when it is the initiator.
			IRDY# is tristated from the leading edge of RESET# and remains tristated until driven as either a master or a slave by the 82C861/82C871.
TRDY#	68	I/O (s/t/s)	Target Ready: TRDY#, along with IRDY#, indicates whether the &2C861/82C871 is able to complete the current data phase of the cycle. TRDY# and IRDY# are both asserted when a data phase is completed.
			When the 82C861/82C871 is acting as the target during read and write cycles, it performs in the following manner:
			1. During a read, the 82C861/82C871 asserts TRDY# to indicate that it has placed valid data on AD[31:0].
			2. During a write, the 82C861/82C871 asserts TRDY# to indicate that is pre- pared to accept data.
			TRDY# is an input when the 82C861/82C871 is the initiator and an output when it is the target.
			TRDY# is tristated from the leading edge of RESET# and remains so until driven as either a master or a slave by the 82C861/82C871.
STOP#	70	1/O (s/t/s)	Stop: STOP# is an output when the 82C861/82C871 is the target and an input when it is the initiator. As the target, the 82C861/82C871 asserts STOP# to request that the master stop the current cycle. As the master, the assertion of STOP# by a target forces the 82C861/82C871 to stop the current cycle.
			STOP# is tristated from the leading edge of RESET# and remains so until driven by the 82C861/82C871 acting as a slave.

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Signal Name	Pin No.	Pin Type	Signal Description
DEVSEL#	69	I/O (s/t/s)	Device Select: The 82C861/82C871 claims a PCI cycle via positive decoding by asserting DEVSEL#. As an output, the 82C861/82C871 drives DEVSEL# for two different reasons:
			 If the 82C861/82C871 samples IDSEL active in configuration cycles, DEVSEL# is asserted.
			2. When the 82C861/82C871 decodes an internal address or when it subtrac- tively decodes a cycle, DEVSEL# is asserted
			When DEVSEL# is an input, it indicates the target's response to an 82C861/ 82C871 master-initiated cycle.
			DEVSEL# is tristated from the leading edge of RESET# and remains so until driven by the 82C861/82C871 acting as a slave.
IDSEL	50	I	Initialization Device Select: This signal is the "chip select" during configuration read and write cycles. IDSEL is sampled by the 82C861/82C871 during the address phase of a cycle. If IDSEL is found to be active and the bus command is a configuration read or write, the 82C861/82C871 claims the cycle with DEVSEL#.
PERR#	71	I/O	Parity Error: The 82C861/82C871 uses this line to report data parity errors during any PCI cycle except a Special Cycle.
SERR#	75	I	System Error: The 82C861/82C871 uses this line to report address parity errors and data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
REQ#	36	0	Bus Request: REQ# is asserted by the 82C861/82C871 to request ownership of the PCI bus.
GNT#	35	1	Bus Grant: GNT# is sampled by the 82C861/82C871 for an active low assertion, which indicates that it has been granted use of the PCI bus.
CLKRUN#	46	1/0	Clock Run: The CLKRUN# function is available on this pin and can be used to reduce chip power consumption during idle periods. It is an I/O sustained tristate signal and follows the PCI 2.1 defined protocol.
VCC]	Р	Power: If FireLink is being used in a CMD-based system, this pin can be connected to VCC.

3.2.3 USB Interface Signals

Signal Name	Pin No.	Pin Type	Signal Description
VD1+	13	1/0	Port 1 Positive Data Line
VD1	14	I/O	Port 1 Negative Data Line
VD2+	18	I/O	Port 2 Positive Data Line
VD2	19	1/0	Port 2 Negative Data Line
PWRON1, PWRON2	9, 24	0	Power On Lines 1 and 2: These outputs are used to turn on the respective USB port's VCC power.
PWRFLT1, PWRFLT2	10, 23	I	Power Fault Lines 1 and 2: These inputs indicate that an over-current fault on each of the USB ports has occurred. Their polarity can be software controlled: strap low for active high, strap high for active low.



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Signal Name	Pin No.	Pin Type	Signal Description
SMI#/NC	29	0	System Management Interrupt: This signal is used to request a System Man- agement Mode (SMM) interrupt. It can be connected to a spare EPMI pin on the host chipset.
			If FireLink is used with an OPTi IRQ driveback-capable chipset, this connection is not needed.
<zvfsync></zvfsync>		0	Zoomed Video Frame Synchronization: Connection to PC Card ZV Port.
INTA#/NC	30	0	PCI Interrupt A: This signal can be connected to a PCI interrupt line.
			If FireLink is used with an OPTi IRQ driveback-capable chipset, this connection is not needed.
<zvsclk></zvsclk>			Zoomed Video Sample Clock for DAC2: Connection to PC Card ZV Port.
IRQ1/NC	27	0	Interrupt Request 1: This pin should be tied to the keyboard interrupt from the keyboard controller.
			If FireLink is used with an OPTi IRQ driveback-capable chipset, this connection is not needed.
<zvsdi></zvsdi>		1	Zoomed Video Serial Data Input: Connection to PC Card ZV Port.
IRQ12/NC	28	0	Interrupt Request 12: This pin should be tied to the mouse interrupt from the key- board controller.
			If FireLink is used with an OPTi IRQ driveback-capable chipset, this connection is not needed.
<zvsdo></zvsdo>		0	Zoomed Video Serial Data Output: Connection to PC Card ZV Port.

3.2.4 Interrupt and Zoomed Video Port Interface Signals

3.2.5 USB Power and Misc. Signals

Signal Name	Pin No.	Pin Type	Signal Description
PWRGD1	11	l, Analog (S)	Power Good Line 1: This schmitt-trigger analog input is used to sense the supply VCC power on USB port 1. (For VCC power greater than 4.0V, this line can be a logic input, on/off, or a resistor divider.)
			This pin is also used as a strap option for chip/board level test configuration. Refer to Table 3-3.
<voldn></voldn>		0	Volume Down: Interface for push-button volume control. Used to decrease vol- ume.
<sout#></sout#>	1	0	Serial Output: Serial interrupt output line for Intel style of serial IRQs.
PWRGD2	22	l, Analog (S)	Power Good Line 2: This schmitt-trigger analog input is used to sense the supply VCC power on USB port 2. (For VCC power greater than 4.0V, this line can be a logic input, on/off, or a resistor divider.)
<irqser></irqser>		I/O	Serial Interrupt Request: Bidirectional interrupt line for Compaq style of serial IRQs.
<spkrin></spkrin>	1	1	Speaker Input: Chipset digital speaker input signal.



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Signal Name	Pin No.	Pin Type	Signal Description
GND/NIC	8		Ground: In a CMD-based system, this pin can remain connected to GND.
			No Internal Connection: FireLink makes this pin a "No Internal Connection" to allow future upgrade to FireBlast.
<volup></volup>]	0	Volume Up: Interface for push-button volume control. Used to increase volume.
<sin#></sin#>		1	Serial Input: Serial interrupt return line for Intel style of serial IRQs.
TEST0	21	1	Test Line 0: Strap option used for chip/board level test configuration. Refer to Table 3-3.
I2CCLK		I/O	I ² C Bus Clock Signal: FireLink and FireBlast use this pin for optional connection as the clock line for the I ² C interface.
<rxd></rxd>	1	I	Receive Data: FireBlast provides the option of a MIDI interface on this pin.
TEST1	25	ł	Test Line 1: Strap option used for chip/board level test configuration. Refer to Table 3-3.
I2CDATA		1/0	I^2C Bus Data Signal: FireLink and FireBlast use this pin for optional connection as the data line for the I^2C interface
<txd></txd>	1	0	Transmit Data: FireBlast provides the option of a MIDI interface on this pin.

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3.2.6 Audio CODEC Interface Signals

Signal Name	Pin No.	Pin Type	Signal Description
VCC/NIC	1		Power: In a CMD-based system, this pin can remain connected to VCC.
			No Internal Connection: FireLink makes this pin a "No Internal Connection" to allow future upgrade to FireBlast.
<lr2></lr2>]	0	Serial Clock: Clock connection to serial CODEC for second DAC on FireBlast.
GND/NIC	73		Ground: In a CMD-based system, this pin can remain connected to GND.
			No Internal Connection: FireLink makes this pin a "No Internal Connection" to allow future upgrade to FireBlast.
<sdo></sdo>		0	Serial Data Output: Connection to serial CODEC on FireBlast.
VCC/NIC	74		Power: In a CMD-based system, this pin can remain connected to VCC.
			No Internal Connection: FireLink makes this pin a "No Internal Connection" to allow future upgrade to FireBlast.
<sdi></sdi>		I	Serial Data Input: Connection to serial CODEC on FireBlast.
VCC/NIC	91		Power: In a CMD-based system, this pin can remain connected to VCC.
			No Internal Connection: FireLink makes this pin a "No Internal Connection" to allow future upgrade to FireBlast.
<fsync></fsync>		0	Frame Synchronization: Connection to serial CODEC on FireBlast.
GND/NIC	97		Ground: In a CMD-based system, this pin can remain connected to GND.
			No Internal Connection: FireLink makes this pin a "No Internal Connection" to allow future upgrade to FireBlast.
<sclk></sclk>		0	Serial Clock: Free running clock for external codec on FireBlast.



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Signal Name	Pin No.	Pin Type	Signal Description	
VCC	7, 34, 41, 53, 60, 65, 81, 92, 98	Р	5.0V or 3.3V Power Connection: Core voltage is linked to the PCI interface voltage; either 3.3V or 5.0V is acceptable, however, 3.3V is recommended for lowest power consumption. Core voltage is indicated to the chip through a strap option, refer to Table 3-3.	
			Note: If QFP packaging is selected, pin 53 becomes NIC (No Internal Connection).	
VCC_ISA	26	Р	ISA Reference Voltage: Supplies the reference voltage for pins 27 (IRQ1) and 28 (IRQ12). If IRQ1 and IRQ12 are not used, connect VCC_ISA to the VCC power plane.	
VCC3	12, 17	Р	3.3V Power Connection	
GND	5, 15, 16, 20, 33, 40, 47, 54, 59, 66, 72, 80, 85, 90, 96	G	Ground Connection	

3.2.7 Power and Ground Pins



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PWRGD1 (Pin 11)	TEST1 (Pin 25)	TEST0 (Pin 21)	Mode
0	0	0	NAND tree test
0	0	1	Tristate test
0	1	0	Drive even pins high and odd pins low
0	1	1	Drive odd pins high and even pins low
1	0	0	PCI 5.0V (default)
1	0	1	PCI 3.3V
1	1	0	Test mode to bring out internal TXDSE0 signal on TEST1 pin (pin 25) and internal TXD signal on TEST0 pin (pin 21), PCI 5.0V.
1	1	1	Test mode to bring out internal TXDSE0 signal on TEST1 pin (pin 25) and internal TXD signal on TEST0 pin (pin 21), PCI 3.3V.

Table 3-3 82C861/82C871 Strap Options



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4.0 Functional Description

4.1 Universal Serial Bus (USB)

The 82C861/82C871 supports a PCI-based implementation of Universal Serial Bus utilizing the OpenHCI standard developed by Compaq, Microsoft, and National Semiconductor.

The USB core contains an integrated root hub that can support up to two downstream USB hubs or devices. The USB implementation consists of the root hub, PCI interface controller, and USB host controller. Keyboard and mouse legacy support are also included for DOS compatibility with USB devices.

This document must be used along with the following public domain reference documents to get the complete functional description of the USB core implementation.

- USB Specification, Revision 1.0
- OpenHCI Specification, Revision 1.0a
- PCI Specification, Version 2.1

A functional block diagram of the USB core implementation is given in Figure 4-1.



Figure 4-1 USB Functional Block Diagram



4.1.1 PCI Controller

The PCI controller interfaces the host controller to the PCI bus. As a master, the PCI controller is responsible for running cycles on the PCI bus on behalf of the host controller. As a target, the PCI controller monitors the cycles on the PCI bus and determines when to respond to these cycles. The USB core is a PCI target when it decodes cycles to its internal PCI configuration registers or to its internal PCI memory mapped I/O registers. The PCI USB controller asserts DEVSEL# in medium decode timing to claim a PCI transaction.

The configuration space of the PCI controller is accessed through Mechanism #1 as Bus #0, Device #X (Device # depends on which AD line is connected to the IDSEL input), Function #0, hereafter referred to as PCICFG.

Table 4-1 gives a register map for the PCICFG register space. Refer to Section 5.1, "PCICFG Register Space" for detailed bit information.

Table 4-1	PCI Controller Register Map			
PCICFG	R/W	Register Name		
00h-01h	RO	Vendor ID		
02h-03h	RO	Device ID		
04h-05h	R/W	Command		
06h-07h	R/W	Status		
08h	RO	Revision ID		
09h-0Bh	RO	Class Code		
0Ch	R/W	Cache Line Size		
0Dh	R/W	Master Latency Timer		
0Eh	RO	Header Type		
0Fh		Reserved		
10h-13h	R/W	Base Address Register 0		
14h-2Bh		Reserved		
2Ch-2Dh	RO	Subsystem Vendor		
2Eh-2Fh	RO	Subsystem ID		
30h-3Bh		Reserved		

PCICFG	R/W	Register Name
3Ch	R/W	Interrupt Line
3Dh	R/W	Interrupt Pin
3Eh	R/W	Minimum Grant
3Fh	R/W	Maximum Latency
40h-43h		Reserved
44h-4Dh		Reserved
4Eh	R/W	I ² C Control
4Fh		Reserved
50h	R/W	PCI Host Feature Control
51h	R/W	Interrupt Assignment
52h-53h		Reserved
54h-57h	R/W	IRQ Driveback Address
58h-6Bh		Reserved
6Ch-6Fh	R/W	Test Mode Enable



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4.1.2 Host Controller

This block is the operational control block in the USB core. It is responsible for the host controller operational states (Suspend, Disabled, Enabled), special USB signaling (Reset, Resume), status, interrupt control, and host controller configuration information. The host controller (HC) interface registers are PCI memory mapped I/O, hereafter referred to as MEMOFST. Table 4-2 gives a register map for the MEMOFST register space. Refer to Section 5.2, "Host Controller Register Space" for detailed bit information.

MEMOFST	R/W	Register Name
00h-03h	RO	HcRevision
04h-07h	R/W	HcControl
08h-0Bh	R/W	HcCommandStatus
0Ch-0Fh	R/W	HcinterruptStatus
10h-13h	R/W	HcInterrupt Enable
14h-17h	R/W	HcInterrupt Disable
18h-1Bh	R/W	HcHCCA
1Ch-1Fh	R/W	HcPeriodCurrentED
20h-23h	R/W	HcControlHeadED
24h-27h	R/W	HcControlCurrentED
28h-2Bh	R/W	HcBulkHeadED
2Ch-2Fh	R/W	HcBulkCurrentED

 Table 4-2
 Host Controller Register Map

MEMOFST	R/W	Register Name
30h-33h	R/W	HcDoneHead
34h-37h	R/W	HcFminterval
38h-3Bh	R/W	HcFrameRemaining
3Ch-3Fh	R/W	HcFmNumber
40h-43h	R/W	HcPeriodicStart
44h-47h	R/W	HcLSThreshold
48h-4Bh	R/W	HcRhDescriptorA
4Ch-4Fh	R/W	HcRhDescriptorB
50h-53h	R/W	HcRhStatus
54h-57h	R/W	HcRhPort1Status
58h-5Bh	R/W	HcRhPort2Status



4.1.2.1 Legacy Support

Four registers are provided for legacy support:

- HceControl
 - Used to enable and control the emulation hardware and report various status information.
- HceInput
 - Emulation side of the legacy Input Buffer register.
- HceOutput
 - Emulation side of the legacy Output Buffer register where keyboard and mouse data is to be written by software.
- HceStatus
 - Emulation side of the legacy Status register.

These registers are located in the Host Controller Register Space; from MEMOFST 100h through 10Fh. Table 4-3 shows a register map of these registers. Refer to Section 5.2.1, "Legacy Support Registers" for detailed bit information.

Table 4-3 Legacy Support Register Map

MEMOFST	R/W	Register Name	
100h-103h	R/W	HceControl	
104h-107h	R/W	HceInput	
108h-10Bh	R/W	HceOutput	
10Ch-10Fh	R/W	HceStatus	

Intercept Port 60h and 64h Accesses

The HceStatus, HceInput, and HceOutput registers are accessible at I/O Ports 60h and 64h when emulation is enabled. Reads and writes to these registers using the I/O Ports does have some side effects as shown in Table 4-4. However, accessing these registers directly through their memory address produces no side effects.

When emulation is enabled, I/O accesses of Ports 60h and 64h must be handled by the Host Controller (HC). The HC must be positioned in the system so that it can do a positive decode of accesses to Ports 60h and 64h on the PCI bus. If a keyboard controller is present in the system, it must either use subtractive decode or have provisions to disable its decode of Ports 60h and 64h. If the legacy keyboard controller uses positive decode and is turned off during emulation, it must be possible for the emulation code to quickly re-enable and disable the legacy keyboard controller's Port 60h and 64h decode. This is necessary to support a mixed operating environment.

Register Contents Accessed/Modified	Side Effect
HceOutput	A read from Port 60h will set the Output Full bit (MEMOFST 10Ch[0]) to 0.
HceInput	A write to Port 60h will set the Input Full bit (MEMOFST 10Ch[1]) to 1 and the Cmd Data bit (MEMOFST 10Ch[3]) to 0.
	• A write to Port 64h will set the: Input Full bit (MEMOFST 10Ch[1]) to 0 and the Cmd Data bit (MEMOFST 10Ch[3]) to 1.
HceStatus	A read from Port 64h returns the current value of the HceSta- tus register

 Table 4-4
 Emulated Registers and Side Effects



5.0 Register Descriptions

The 82C861/82C871 has three types of register spaces:

- 1. PCI Configuration Register Space
- 2. Host Controller Register Space
- 3. I/O Register Space

The subsections that follow detail the locations and access mechanisms for the registers located within these register spaces.

2. All reserved bits/registers MUST be written to 0 unless otherwise specified.

5.1 PCICFG Register Space

The configuration space of the PCI USB controller is accessed through Mechanism #1 as Bus #0, Device #X (Device # depends on which AD line is connected to the IDSEL input), Function #0, hereafter referred to as PCICFG. The bit formats for these registers are described in Table 5-1.

Table 5-1	PCICFG 00h-I	FFh					
7	6	5	4	3	2	1	0
PCICFG 00h PCICFG 01h			Vendor Identifica	ation Register (RC)		Default = 45h Default = 10h
PCICFG 02h PCICFG 03h			Device Identifica	ation Register (RC))		Default = 61h Default = C8h
PCICFG 04h	A Cashington (1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1		Command R	egister - Byte 0	sintin energiante e	and a second	Default = 00h
Wait cycle control: USB core does not need to insert a wait state between address and data on the AD lines. This bit is always 0.	PERR# (response) detection enable bit: 0 = PERR# not asserted 1 = USB core asserts PERR# when it is the receiv- ing data agent and it detects a data parity error.	VGA palette snooping: This bit is always 0.	Postable memory write command: Not used when USB core is a master. This bit is always 0.	Special Cycles: USB core does not run Special Cycles on PCI. This bit is always 0.	USB core can run PCI master cycles: 0 = Disable 1 = Enable	USB core responds as a target to memory cycles. 0 = Disable 1 = Enable	USB core responds as a target to I/O cycles: 0 = Disable 1 = Enable
PCICFG 05h	· · · · · · ·		Command R	legister - Byte 1	· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·	Default = 00h
		Reserved: These	e bits a <i>r</i> e always ().		Back-to-back enable: USB core only acts as a mas- ter to a single device, so this functionality is not needed. This bit is always 0.	SERR# (response) detection enable bit: 0 = SERR# not asserted 1 = USB core asserts SERR#



Notes: 1. All bits/registers are read/write and their default value is 0 unless otherwise specified.

Table 5-1 PCICFG 00h-FFh (cont.)

7	6	5	4	3	2	1	0			
PCICFG 06h	Status Register - Byte 0 Default = 80h									
Fast back-to- back capability: USB core sup- ports fast back- to-back transac- tions when transactions are not to same agent. This bit is always 1			Reserved	d: These bits are a	ılways 0.					
PCICFG 07h			Status Reg	ister - Byte 1	·	<u></u>	Default = 02h			
Detected parity error: This bit is set to 1 whenever the USB core detects a parity error, even if PCICFG 04h[6] is disabled. Write 1 to clear.	SERR# status: This bit is set to 1 whenever the USB core detects a PCI address parity error. Write 1 to clear.	Received master abort status: Set to 1 when the USB core, acting as a PCI master, aborts a PCI bus mem- ory cycle. Write 1 to clear.	Received target abort status: This bit is set to 1 when a USB core generated PCI cycle (USB core is the PCI master) is aborted by a PCI target. Write 1 to clear.	Signaled target abort status: This bit is set to 1 when the USB core signals tar- get abort. Write 1 to clear.	DEVSEL Indicates DEVS performing a po Since DEVSEL meet the mediu bits are encode	timing (RO): EL# timing when sitive decode. # is asserted to m timing, these d as 01.	Data parity reported: Set to 1 if PCICFG 04h[6] is set and the USB core detects PERR# asserted while acting as PCI master (whether PERR# was driven by USB core or not.)			
PCICFG 09h			Class Code	Register (RO)		TRUTAL CONTRACTOR	Default = 10			
PCICFG UAN PCICFG 0Bh							Default = 03h Default = 0Ch			
DOIOEC ACh			Cooke Line	Cine Degister		and Constraints				
PCICFG 0Dh			Master Latence	y Timer Register	1		Default = 00h			
PCICFG 0Eh			Header Type	e Register (RO)			Default = 00h			
	and the second se						Defective det			
PCICEG OFh			Re	served			Detault = 00h			
PCICFG 10h-13	PCICFG 10h-13h Base Address Register 0 Default = 00h									
Porcered run-ran Base Address Hegister 0 Default = 00n This register identifies the base address of a contiguous memory space in main memory.POST will write all 1s to this register, then read back the value to determine how big of a memory space is requested. After allocating the requested memory, POST will write the upper bytes with the base address. Bits [31:0] correspond to: 10h = [7:0], 11h = [15:8], 12h = [23:16], 13h = [31:24]. Bits [0] - Indicates that the operational registers are mapped into memory space. Always = 0. Bits [2:1] - Indicates that the base register is 32 bits wide and can be placed anywhere in 32-bit memory space. Always = 0. Bits [3] - Indicates a 4K byte address range is requested, Always = 0. Bits [11:4] - Indicates a 4K byte address range is requested, Always = 0. Bits [31:12] - Base Address: Post writes the value of the memory base address to this register. Bits register.										



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able 5-1	PCICFG 00h-i	Fh (cont.)					
7	6	5	4	3	2	1	0
PCICFG 14h-2B	h		Rese	erved			Default = 00h
PCICFG 2Ch-2E Subsystem V - The chipset	Dh endor - Bits [15:0] t normally respond	correspond to: 20 Is to reads of this	Subsystem Venc Ch = [7:0], 2Dh = [1 read-only register v	dor Register (RO) 5:8]. with 00h.	and an and a second		Default = 00h
PCICFG 2Eh-2F Subsystem IE - The chipse	h D - Bits [15:0] corre t normally respond	espond to: 2Eh = [Is to reads of this	Subsystem ID 7:0], 2Fh = [15:8]. read-only register	Register (RO)		an a	Default = 00h
PCICFG 30h-3B	line and a second s		Res	erved			Default = 00h
PCICFG 3Ch This register used by device	identifies which of	the system intern	Interrupt Li upt controllers the o	ine Register device's interrupt p	oin is connected to	o. The value of this	Default = 00h register is
PCICFG 3Dh This register	identifies which in	terrupt pin a devic	Interrupt P ce uses. Since the	Pin Register USB core usesINT	A#, this value is s	et to 01h.	Default = 01h
PCICFG 3Eh			Minimum Grar Rese	nt Register (RO) erved			Default = 00h
PCICFG 3Fh			Maximum Later Rese	ncy Register (RO) erved		<u> Soldin a jedne</u>	Default = 00h
PCICFG 40h-43 These regist	3h ers are for interna	I testing purposes	Res . Do not write to th	erved ese registers.			Defauit = 00f
PCICFG 44h-4l	Dh		Res	erved			Default = 001
PCICEG 4Eb			l ² C Cont	rol Register			Default - 00
	Reserved		Reads back I ² C data output bit (bit 2) (RO)	Reads back I ² C clock out- put bit (bit 1) (RO)	$I^{2}C$ data output: 0 = Output 0 1 = Output 1	$I^{2}C$ clock output: 0 = Output 0 1 = Output 1	l ² C control: 0 = Disable 1 = Enable
PCICFG 4Fh			Res	served			Default = 00I
PCICFG 50h			PCI Host Featur	re Control Registe	er		Default = 00
	Res	served		Subsystem Vendor ID Register (PCICFG 2Ch) control: 0 = Writable 1 = Read-Only	CLKRUN# on host interface): 0 = Disabled, CLKRUN# tristated 1 = Enabled per PCI	Port 2 output: 0 = Enable 1 = Disable (Controls USB I/O cells to save power)	Port 1 output: 0 = Enable 1 = Disable (Controls USB I/O cells to save power)



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7	6	5	4	3	2	1	0	
PCICFG 51h	· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·	Interrupt Assig	gnment Register	r		Default = 01h	
Host controller type: 0 = Viper-N+ (send sin- gle data phase on IRQ drive- back) 1 = FireStar (burst two data phases)	IRQ Driveback: 0 = Disable 1 = Enable	Reserved	Interrupt Assignment (PCIRQ0# Default) - Interrupts from the USB are mapped to thi interrupt. Note that if an IRQ (an edge-mode interrupt) is selected, this IRQ must be p grammed to Level mode on the host chipset. Level Mode: 00000 = Disabled 00110 = ACPI1 01011 = ACPI6 00000 = Disabled 00110 = ACPI2 01100 = ACPI7 00010 = PCIRQ0# (Default) 00111 = ACPI2 01100 = ACPI7 00010 = PCIRQ1# 01000 = ACPI3 01101 = ACPI8 00011 = PCIRQ2# 01001 = ACPI4 01110 = ACPI9 00100 = PCIRQ3# 01010 = ACPI5 01111 = ACPI10 00101 = ACPI0 Edge Mode: 10000 = IRQ0 10110 = IRQ6 11011 = IRQ11 10000 = IRQ0 10110 = IRQ6 11011 = IRQ11 10001 = IRQ12 10000 = IRQ12 10001 = IRQ1 10111 = IRQ7 11100 = IRQ13 11011 = IRQ13 10011 = IRQ14 10010 = IRQ2 11000 = IRQ9 11110 = IRQ14 11010 = IRQ14 11010 = IRQ15					
PCICFG 52h-53	h		Res	served			Default = 00h	
PCICFG 54h-57	'n	IRQ Driveba	ack Address Regi	ister - Byte 0: A	ddress Bits [7:0]	Def	ault = 33333330h	
IRQ Drivebad - When the F REQ# line host interru - Bits 1:0 are	ck Protocol Addres FireLink/FireBlast I to the host. Once upt controller claim e reserved to be 0	ss Bits: Bits [31:0] logic must genera it has the bus, it w is this cycle and k 0 and are read-or	correspond to: 54 tte an interrupt from vrites the changed atches the new IR nly.	h = [7:0], 55h = [n any source, it fo IRQ information Q values.	[15:8], 56h = [23:16 ollows the IRQ Driv to the 32-bit I/O ac	5], 57h = [31:24]. eback Protocol ar Idress specified in	nd toggles the this legister. The	
PCICFG 58h-6E	3h		Re	served	Sector and the sector of the	the second s	Default = 00h	
PCICFG 6Ch-6	Fh		Test Mode E	Enable Register	onninitrijeli je se	ogo com en e paragonada	Default = 00h	
	-		Res	erved				





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5.2 Host Controller Register Space

This register space is the operational control block in the USB core. It is responsible for the host controller operational states (Suspend, Disabled, Enabled), special USB signaling (Reset, Resume), status, interrupt control, and host controller configuration information.

The host controller (HC) interface registers are PCI memory mapped I/O, hereafter referred to as MEMOFST. The bit formats for these registers are described in Table 5-2.

7 6 5 4 3 2 1 0 MEMOFST 0th-03h HcRevision Register (RO) Default = 1 Bits [31:0] correspond to: 00h = [7:0], 01h = [15:8], 02h = [23:16], 03h = [31:24] Default = 0 Bits [31:0] correspond to: 00h = [7:0], 01h = [15:8], 02h = [23:16], 03h = [31:24] Default = 0 Bits [31:0] correspond to: 00h = [7:0], 01h = [15:8], 02h = [23:16], 03h = [31:24] Default = 0 Bits [31:0] correspond to: 00h = [7:0], 01h = [15:8], 02h = [23:16], 03h = [31:24] Default = 0 Bits [31:0] correspond to: 00h = [7:0], 01h = [15:8], 02h = [23:16], 03h = [31:24] Default = 0 Bits [31:3] Reserved Processing of Data to the processing of 0 = USB Reset Default = 0 HEMOFST 04h HcControl Register - Byte 0 Default = 0 D = USB Reset Di LSB (Departional 1 = Disable Default = 0 10 = USB Reset 0 = Disable 1 = Enable Easite is enabled. ⁽¹⁾ 0 = Yes Processing of 0 = notrol 1 ending is N-1 whith is the number of control ending is N-1 whith is the number of control ending is N-1 whith is the number of control ending is N-1 whith is the number of control ending is N-1 whith is the number of control ending is N-1 whith is the number of control ending is N-1 whith is the number of control ending is N-1 whith is the number of control ending is N-1 whith is the number of control ending is N-1 whith is the number of control ending is N-1 whith is the number of control ending is N-1 whith is the number of control ending is N-1 whith is the number of control e	Table 5-2 M	EMOFST 00	h-5Ch			_		
MEMOFST 00h HcRevision Register (RO) Default = 1 Bits [31:0] correspond to: 00h = [7:0], 01h = [15:8], 02h = [23:16], 03h = [31:24] - - - Bits [31:3] Revision - Indicates the Open HCI Specification revision number implemented by hardware (X.Y = XYh). FireLink and FireBlast support Specification 1.0. - Bits [31:3] Reserved MEMOFST 04h HcControl Register - Byte 0 Default = 0 MEMOFST 04h HcControl List: 0 = Disable Processing of 0 = USB Resume Processing of 0 = Disable Processing of 0 = Disable Processing of 0 = Disable Control Bulk Service Ratio: Specifies the number of control omous List when Periodic List is enabled: ⁽¹⁾ Control Bulk Service Ratio: Specifies the number of control omous List is the number of control omous Dist when Periodic List is enabled: ⁽¹⁾ Processing of 0 = Disable Control Bulk Service Ratio: Specifies the number of control onous List is the number of control onous Dist when Periodic List is enabled: ⁽¹⁾ Processing of 0 = Disable Control Bulk Service All or every nonus List is the number of control onous Dist is the number of control end points (i.e., 00 = 1	7	6	5	4	3	2	1	0
Bits [31:0] correspond to: 00h = [7:0], 01h = [15:8], 02h = [23:16], 03h = [31:24] Bits [7:0] Revision - Indicates the Open HCI Specification revision number implemented by hardware (X.Y = XYh). FireLink and FireBlast support Specification 1.0. Bits [31:8] Reserved MEMOFST 04h HcControl Register - Byte 0 Default = 0 MEMOFST 04h HcControl Register - Byte 0 Control Buk Service Ratio: 01 = USB Resume 10 = USB Questional 11 = Los Bus 11 = Enable 11 = No	MEMOFST 00h MEMOFST 01h-03	h		HcRevision	Register (RO)		De	Default = 10h fault = 000001h
MEMOFST 04h HcControl Register - Byte 0 Default = 0 HC Functional State: Processing of Bulk List: Processing of Control List: Processing of Control List: Processing of Disable Isoch- ronous List Control Bulk Service Ratio: Specifies the number of control endpoints serviced for every bi andpoint. Encoding is N-1 with the number of control endpoints serviced for every bi andpoint. Encoding is N-1 with the number of control endpoints serviced for every bi andpoint. Encoding is N-1 with the number of control endpoints serviced for every bi andpoint. Encoding is N-1 with the number of control end- point; (i.e., 00 = 1 contro	Bits [31:0] corres - Bits [7:0] R Fi - Bits [31:8] R	spond to: 00h = tevision - Indicat ireLink and Fire teserved	[7:0], 01h = [15:8] les the Open HCt Blast support Spe	, 02h = [23:16], 0 Specification revis cification 1.0.	3h = [31:24] ion number imple	mented by hardwa	are (X.Y = XYh).	
MEMOFST 04h HcControl Register - Byte 0 Default = (HC Functional State: 00 = USB Reset 01 = USB Resume 01 = USB Resume 01 = USB Qperational 11 = Enable Processing of Bulk List: 0 = Disable 1 = Enable Processing of Oonto List: 0 = Disable 1 = Enable Processing of Disable Isoch- rupt and isoch- rupt and isochronous andpoint descriptor. Control Bulk Service Ratic rupt and isoch- rupt and isoch- rupt and isochronous and isochronous andpoint descriptor. Control end point; 11 = 4 control end poin								
HC Functional State: 00 = USB Reset 01 = USB Resume 10 = USB Operational 11 = Enable Processing of Bulk List: 0 = Disable 11 = Enable Processing of Control List: 0 = Disable Disable Isoch ronous List 1 = Enable Processing of Bulk List: 0 = Disable Control Bulk Service Ratio: Specifies the number of control nonus List 0 = Disable 11 = USB Operational 11 = USB Suspend 1 = Enable 1 = Enable 1 = Enable Disable Isoch ronous List 1 = Enable 0 = Disable 1 = Enable Processing of ronous List 1 = Enable Processing of ronous List 1 = Enable Control Bulk Service Ratio: Specifies the number of control end points serviced for every b endpoint Service for e	MEMOFST 04h			HcControl Re	egister - Byte 0			Default = 00h
(1) Disabling the Isochronous List when the Periodic List is enabled allows interrupt endpoint descriptors to be serviced. Whileprocessing Period List, the HC will check bit 3 when it finds an isochronous endpoint descriptor. Default = MEMOFST 05h HcControl Register - Byte 1 Default = Reserved Remote Wakeup Connected Enable: Remote Wakeup Connected (RO): Interrupt Routing: 0 = Interrupt to it is used this bit is used to its is used to its is used to enable that operation. Signal. This is used to enable that operation. Indicates Since there is no remote wakeup signal signal. This is used to enable that operation. Since there is is oported, this bit is used to enable that operation. Signal. The bit is hardcoded to 0. MEMOFST 06h-07h HcControl Register - Bytes 2 & 3 Default =	HC Functional State:Processing of Bulk List:Processing of Control List:Disable Isoc ronous List01 = USB Resume0 = Disable0 = Disable1 = Disable1 = Disable10 = USB Operational1 = Enable1 = Enable1 = EnableList is enabled11 = USB SuspendThe HC may force a state change from USB Suspend to USB Resume after detecting resume signaling from a downstream port.Disable processing of Bulk List:Disable Control List: 0 = Disable 1 = EnableDisable control List: enable			Disable Isoch- ronous List when Periodic List is enabled: ⁽¹⁾ 0 = Yes 1 = No	Processing of Periodic (inter- rupt and isoch- ronous) List: 0 = Disable 1 = Enable The HC checks this bit prior to attempting any periodic trans- fers in a frame.	Control Bulk S Specifies the nurr endpoints service endpoint. Encodir N is the number of points (i.e., 00 = 1 point; 11 = 4 cont	ervice Ratio: aber of control d for every bulk ig is N-1 where if control end- control end- rol endpoints).	
MEMOFST 05h HcControl Register - Byte 1 Default = Reserved Remote Remote Remote Interrupt Wakeup Connected Enable: Indicates routed to 0 = Interrupt If a remote Indicates whether the HC normal interrupt Is supported, supported, supports a interrupt It is bit is used remote wakeup signal. This interrupt Image: Supported, supported, supports a interrupt Image: Supported, supported, supports a interrupt Image: Supported, supported, supports a interrupt Image: Supported, supported, supported, supportag Image: Supported, supported, supportag SMI Also see PCICFG 511 Also see PCICFG 511 MEMOFST 06h-07h HcControl Register - Bytes 2 & 3 Default =	(1) Disabling the Is Period List, the	sochronous List HC will check t	when the Periodic bit 3 when it finds	: List is enabled al an isochronous er	lows interrupt end adpoint descriptor	point descriptors t	o be serviced. Whi	leprocessing the
Reserved Remote Remote Remote Remote Interrupt Wakeup Con- nected Enable: Wakeup Con- nected (RO): 0 = Interrupt 0 = Interrupt If a remote Indicates whether the HC normal interrupt is supported, supports a remote wakeup interrupt this bit is used remote wakeup interrupt to enable that signal. This (INTA#) operation. implementation 1 = Interrup Since there is operation. signal. The bit is supported, this signal. The bit is SMI Also see PCICFG 511 MEMOFST 06h-07h HcControl Register - Bytes 2 & 3 Default =	MEMOFST 05h			HcControl R	egister - Byte 1			Default = 00h
MEMOFST 06h-07h HcControl Register - Bytes 2 & 3 Default = Reserved			Reserved			Remote Wakeup Con- nected Enable: If a remote wakeup signal is supported, this bit is used to enable that operation. Since there is no remote wakeup signal supported, this bit is ignored.	Remote Wakeup Con- nected (RO): Indicates whether the HC supports a remote wakeup signal. This implementation does not sup- port any such signal. The bit is hardcoded to 0.	Interrupt Routing: 0 = Interrupts routed to normal interrupt mechanism (INTA#) 1 = Interrupts routed to SMI Also see PCICFG 51h
Beserved	MEMOFST 06h-07	7h		HcControl Reg	ister - Bytes 2 &	3		Default = 00
				Res	erved			



Table 5-2 MEMOFST 00h-5Ch

	6	5	4	3	2	1	0	
MEMOFST 08h		н	cCommandStatu	is Register - Byte	e 0		Default = 00h	
	Rese	rved		Ownership Change Request: When set by software, this bit sets the Owner- ship Change bit (MEMOFST 0Fh[6]). Cleared by soft- ware.	Bulk List has an active endpoint descriptor? ⁽¹⁾ 0 = No 1 = Yes	Control List has an active endpoint descriptor?(1) 0 = No 1 = Yes	HC Reset: Writing a 1 ini- tiates a soft- ware reset. This bit is cleared by the HC upon com- pletion of reset operation.	
(1) The bit may b bit 2, Control	e set by either so List for bit 1)	ftware or the HC.	It is cleared by the	e HC each time it	begins processing) the head of the l	ist(Bulk List for	
MEMOFST 09h HcCommandStatus Register - Byte 1 Default = 00								
	<u> </u>		Rese	erved			·	
MEMOFST 0Ah		ΗΗ	IcCommandStatu	us Register - Byte	e 2		Default = 00h	
		Schedule O This field increm the Scheduling ((MEMOFST 0Ch count wraps from	verrun Count: ients every time Overrun bit i[0] is set. The n 11 to 00.					
MEMOFST 0Bh		ŀ	IcCommandState	us Register - Byt	e 3	<u> </u>	Default = 00h	
			Rese	erved				
NEWOFOT och								
MEMORSIUCH		ł	Icinterrupt Statu	s Register - Byte	• 0*		Default = 00h	
Reserved	Root Hub Status Change: This bit is set when the con- tent of HcRh Status (50h- 53h) or the con- tent of any HcRhPort Sta- tus Register (54h-5Bh) has changed.	Frame Number Overflow: This bit is set when MEMOFST 3Ch[15] (Frame Num- ber Register) changes from 0-to-1 or from 1-to-0.	IcInterrupt Statu Unrecoverable Error: This event is not imple- mented and is hardcoded to 0. All writes are ignored.	s Register - Byte Detected: This bit is set when the HC detects resume signaling on a downstream port.	Start of Frame: This bit is set when the Frame Management block signals a "Start of Frame" event.	Writeback Done Head: This bit is set after the Host Controller has written HcDone- Head to Hcca- DoneHead.	Default = 00h Scheduling Overrun occurred? 0 = No 1 = Yes	
MEMOFST 0Dh-	Root Hub Status Change: This bit is set when the con- tent of HcRh Status (50h- 53h) or the con- tent of any HcRhPort Sta- tus Register (54h-5Bh) has changed.	Frame Number Overflow: This bit is set when MEMOFST 3Ch[15] (Frame Num- ber Register) changes from 0-to-1 or from 1-to-0.	IcInterrupt Statu Unrecoverable Error: This event is not imple- mented and is hardcoded to 0. All writes are ignored.	s Register - Byte Resume Detected: This bit is set when the HC detects resume signaling on a downstream port. Register - Bytes	Start of Frame: This bit is set when the Frame Management block signals a "Start of Frame" event.	Writeback Done Head: This bit is set after the Host Controller has written HcDone- Head to Hcca- DoneHead.	Default = 00h Scheduling Overrun occurred? 0 = No 1 = Yes Default = 00h	
MEMOFST 0Dh-	Root Hub Status Change: This bit is set when the con- tent of HcRh Status (50h- 53h) or the con- tent of any HcRhPort Sta- tus Register (54h-5Bh) has changed.	Frame Number Overflow: This bit is set when MEMOFST 3Ch[15] (Frame Num- ber Register) changes from 0-to-1 or from 1-to-0.	IcInterrupt Statu Unrecoverable Error: This event is not imple- mented and is hardcoded to 0. All writes are ignored. CInterruptStatus Res	s Register - Byte Resume Detected: This bit is set when the HC detects resume signaling on a downstream port. Register - Bytes erved	Start of Frame: This bit is set when the Frame Management block signals a "Start of Frame" event.	Writeback Done Head: This bit is set after the Host Controller has written HcDone- Head to Hcca- DoneHead.	Default = 00h	
MEMOFST 0Dh-	Root Hub Status Change: This bit is set when the con- tent of HcRh Status (50h- 53h) or the con- tent of any HcRhPort Sta- tus Register (54h-5Bh) has changed.	Frame Number Overflow: This bit is set when MEMOFST 3Ch[15] (Frame Num- ber Register) changes from 0-to-1 or from 1-to-0. Ho	IcInterrupt Statu Unrecoverable Error: This event is not imple- mented and is hardcoded to 0. All writes are ignored. CInterruptStatus Res	s Register - Byte Resume Detected: This bit is set when the HC detects resume signaling on a downstream port. Register - Bytes erved	Start of Frame: This bit is set when the Frame Management block signals a "Start of Frame" event.	Writeback Done Head: This bit is set after the Host Controller has written HcDone Head to Hcca- DoneHead.	Default = 00h Scheduling Overrun occurred? 0 = No 1 = Yes Default = 00h	



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7	6	5	4	3	2	1	0		
dagaalaa taga liiidaa			anan ta Yaran an gala		MPROS <mark>EEDING AN</mark>		<u>115 VIRGANA P</u>		
MEMOFST 10h		F	icinterruptEnable	Register - Byte	0*		Default = 00h		
Reserved	Allow interrupt generation due to Root Hub Status Change:	Allow interrupt generation due to Frame Num- ber Overflow:	Reserved All writes to this bit are ignored.	Allow interrupt generation due to Resume Detected:	Albw interrupt generation due to Start of Frame:	Allow interrupt generation due to Writeback Done Head:	Allow interrupt generation due to Scheduling Overrun:		
	0 = Ignore 1 = Enable	0 = Ignore 1 = Enable		0 = Ignore 1 = Enable	0 = Ignore 1 = Enable	0 = Ignore 1 = Enable	0 = Ignore 1 = Enable		
MEMOFST 11h-1	l2h	Hc	InterruptEnable F	Register - Bytes	1&2		Default = 00h		
			Rese	erved					
MEMOFST 13h		ł	IcinterruptEnable	e Register - Byte	3*		Default = 00h		
Master inter- rupt generation: 0 = Ignore 1 = Allows all interrupts to be enabled in 10h-13h.	Albw interrupt generation due to Ownership Change: 0 = Ignore 1 = Enable		Reserved						
* Writing a 1 to a	bit in this register	sets the correspo	onding bit, while w	riting a 0 leaves t	he bit unchanged.	····			
			en i fransk spans	orași de rești de			and the state of the		
MEMOFST 14h		I	HcInterruptDisab	le Register - Byte	∋ 0*		Default = 00h		
Reserved	Allow interrupt generation due to Root Hub Status Change: 0 = Ignore 1 = Disable	Allow interrupt generation due to Frame Num- ber Overflow: 0 = Ignore 1 = Disable	Reserved All writes to this bit are ignored.	Allow interrupt generation due to Resume Detected: 0 = Ignore 1 = Disable	Albw interrupt generation due to Start of Frame: 0 = Ignore 1 = Disable	Allow interrupt generation due to Writeback Done Head: 0 = Ignore 1 = Disable	Allow interrupt generation due to Scheduling Overrun: 0 = Ignore 1 = Disable		
MEMOFST 15h-	16h	Hc	InterruptDisable	Register - Bytes	1&2	L	Default = 00h		
			Res	erved					
MEMOFST 17h			HcInterruptDisab	le Register - Bvt	e 3*		Default = 00h		
Master inter- rupt generation: 0 = Ignore	Allow interrupt generation due to Ownership Chappe:			Res	erved				
1 = Allows all interrupts to be dis- abled in 10h-13h.	0 = Ignore 1 = Disable								
* Writing a 1 to a	a bit in this registe	r clears the corres	sponding bit, while	writing a 0 leaves	s the bit unchange	d.	5-1100-100-100-100-0-10-10-1-1		
MEMOEST 18b	-1Bh		HeHCC	A Register			Default = 00F		
Bits [31:0] co	rrespond to: 18h =	= [7:0], 19h = [15:	8], 1Ah = [23:16]	1Bh = [31:24]			50,44K - 001		
- Bits [7:0]	Reserved	[],	-,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	[
- Bits [31:8]	Pointer to HCCA	A base address							
The second second									

Table 5-2 MEMOFST 00h-5Ch

Table 5-2 MEMOFST 00h-5Ch

7	6	5	4	3	2	1	0
MEMOFST 1Ch-	1Fh	<u> </u>	HcPeriodCurr	entED Register			Default = 00h
Bits [31:0] corr	respond to: 1Ch =	= [7:0], 1Dh = [15:	8], 1Eh = [23:16], 1	1Fh = [31:24].			
- Bits [3:0]	Reserved						
- Bits [31:4]	Pointer to curren	t Periodic List End	l Descriptor		The second state and a state of the second sta	ANNAL OF LEVEL AND	and the state of the process of the
MEMOFST 20h-2	23h		HcControlHe	adED Register	Marikhet (pilledel-pilled (d. 1977)		Default = 00h
Bits [31:0] con	respond to: 20h =	- [7:0], 21h = [15:8	i], 22h = [23:16], 2	3h = [31:24].			
- Bits [3:0]	Reserved						
- Bits [31:4]	Pointer to curren	t Control List Hea	d End Descriptor				
MEMOEST 24h-	27h		HcBulkHoa	dED Begister			Default = 00h
Bite [31:0] cor	respond to: 24h -	- (7·0) 25h [15·8	10001Kilea	7h - [31.34]			Default = 001
- Bits [3:0]	Reserved	- [7:0], 2011 – [10:0	y, 2011 – (20.10), 2	.71 - [91.24].			
- Bits [31:4]	Pointer to currer	nt Bulk List Head B	End Descriptor				
	882- 1. 1. Ser 9. A.						en finnen tradition i MAN States a
MEMOFST 2Ch-	2Fh		HcBulkCurre	entED Register			Default = 00h
Bits [31:0] cor	respond to: 2Ch	= [7:0], 2Dh = [15:	8], 2Eh = [23:16],	2Fh = [31:24].			
- Bits [3:0]	Reserved						
- Bits [31:4]	Pointer to currer	nt Bulk List End D	escriptor				
MEMOFST 30h-	33h	in a state of the second s	HcDoneH	ead Register		<u></u>	Default = 00h
Bits [31:0] cor	respond to: 30h =	= [7:0], 31h = [15:8	3], 32h = [23:16], 3	33h = [31:24].			
- Bits [3:0]	Reserved						
- Bits [31:4]	Pointer to currer	nt Done List Head	End Descriptor				
MEMOFST 34h-	37h		HcFminte	rval Register			Default=
Bits [31:0] cor	rrespond to: 34h	= [7:0], 35h = [15:	8], 36h = [23:16], 3	37h = [31:24].			
- Bits [13:0]	Frame Interval - is stored here. (These bits specif Default = 2EDFh)	y the length of a fra	ame as (bit times -	- 1). For 12,000 b	t times in a frame,	, a value of 11,999
- Bits [15:14]	Reserved						
- Bits [30:16]	FS Largest Data of each frame.	a Packet: These b	its specify a value	which is loaded in	nto the Largest Da	ita Packet Counte	r at the beginning
- Bit 31	Frame Interval	Toggle - This bit is	s toggled by HCD	whenever it loads	a new value into	the Frame Interva	I bits (bits [130]).
MEMOFST 38h-	-3Bh		HcFrameRen	naining Register			Default = 00h
Bits [31:0] co	rrespond to: 38h	= [7:0], 39h = [15:	8], 3Ah = [23:16],	3Bh = [31:24].			
- Bits [13:0]	Frame Remaini state, the count The counter rel transitions into	ng (RO) - This 14 er decrements ea oads with Frame I the USB Operation	bit decrementing ch 12MHz clock p nterval (MEMOFS nal state.	counter is used to eriod. When the c T 34h[13:0]) at the	time a frame. Wh ount reaches 0, tl at time. In addition	en the HC is in th he end of a frame h, the counter load	e USB Operational has been reached. ds when the HC
- Bits [30:14]	Reserved	T 1 (BA)					_
- Bit 31	Frame Remaini (bits [13:0]) is lo	ng Toggle (RO) - baded.	This bit is loaded w	vith Frame Interval	I Toggle (MEMOF	ST 34h[31]) when	Frame Remaining



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Table 5-2	MEMOFST 00	h-5Ch				_	
7	6	5	4	3	2	1	0
MEMOFST 3Ch	-3Fh		HcFmNum	ber Register			Default = 00h
Bits [31:0] co	rrespond to: 3Ch =	= [7:0], 3Dh = [15:	:8], 3Eh = [23:16], 3	8Fh = [31:24].			
- Bits [15:0]	Frame Number ((MEMOFST 38h	RO) - This 16-bit [13:0]). The coun	incrementing count t will roll over from	ter is incremented FFFh to 0h.	coincident with th	ne load of Frame R	emaining
- Bits [31:16] Reserved						
NENOERT 405			He Deviedief			an a	Defeult - 00b
Bite [21:0] or	-43n	(7·0) 4th - [15·		2h - [21.24]			Delaunt = 00h
- Bits [13:0] cc	Periodic Start - 1 begin.	These bits are use	ed by the List Proce	essor to determine	where in a frame	the Periodic List p	rocessing must
- Bits [31:14] Reserved		navasharara sha biyin kina si i	m minin (1971) - Charles and States (1971) -	COLUMN IN THE STREET OF STREET		
MEMOEST 44h	-47h		HcLSTbres	hold Register	nie he oppositent te oost, daar hie he oppositent te oost, daar		Default = 00h
Bits [31:0] co	prrespond to: 44h :	= [7:0] 45h = [15:	(8) 46b = [23.16] 4	7h = [31·24]			
- Bits [11:0]	LS Threshold - transaction can	These bits contair be started in the	a value used by th current frame.	ne Frame Manage	ment Block to det	ermine whether or	not a low speed
- Bits [31:12	2] Reserved						
MEMOFST 48h	1	H	IcRhDescriptorA	Register - Byte 0	(RO)		Default = 02h
Number Dov	wnstream Ports - T	he USB core sup	ports two downstre	am ports.			
MEMOFST 49h	ו 		HcRhDescriptor	A Register - Byte	1		Default = 00h
(1) Bits 4 and 1 MEMOFST 4A	Reserved I should be written h	to support the ex	No Over-current Protection: ⁽¹⁾ 0 = Over-cur- rent status is reported 1 = Over-cur- rent status is not reported	Over-current Protection Mode: 0 = Global over- current 1 = Individual Over-Cur- rent This bit is only valid when bit 4 is cleared. This bit should be written to 0. over-current and s	Device Type (RO): The USB core is not a com- pound device.	No Power Switching: ⁽¹⁾ 0 = Ports are powered switched 1 = Ports are always pow- ered on	Power Switch- ing Mode: 0 = Global switching 1 = Individual switching This bit is only valid when bit 1 is cleared. This bit should be written to 0.
			Res	erved			
MEMOFST 4B	h		HcRhDescripto	rA Register - Byte	e 3		Default = 01
Power-On to	o Power-Good Tim	е					
- The USB	core power switch	ing is effective wit	thin 2ms. The field	value is represente	ed as the number	of 2ms intervals. T	his field should be

written to support the system implementation. This field should always be written to a non-zero value.



Table 5-2	MEMOFST 00)h-5Ch								
7	6	5	4	3	2	1	0			
MEMOFST 4Ch	-4Dh		RhDescriptorB	Register - Bytes	0&1		Default = 00h			
Bits [15:0] co	rrespond to: 4Ch =	= [7:0], 4Dh = [15:8	3].							
- Bits [15:1]	Device Remova 0 = Device not r 1 = Device remo Bit 15 correspor	ble - USB core po ernovable ovable nds to Port 15, Bit	ts default to remo 14 corresponds to	vable devices:	aining bits follow si	uit. Unimplemented	d ports are			
MEMOEST 4Eb	-4Fh	H	BhDescriptorB	Register- Bytes	2&3		Default - 00h			
Bits [15:0] co	rrespond to: 4Eh :	= [7:0], 4Fh = [15:8		negiater- bytea	240		Delaun - oon			
- Bit O	Reserved		•							
- Bits [15:1]	Port Power Con Unimplemented 0 = Device not r 1 = Global powe	Port Power Control Mask: Bit 15 corresponds to Port 15, Bit 14 corresponds to Port 14, the remaining bits follow sit. Unimplemented ports are reserved. 0 = Device not removable 1 = Global power mask								
	This field is only valid if No Power Switching bit (MEMOFST 49h[1]) is cleared and Power Switching Mode Bit (MEMOFST 49h[0]) is set (individual port switching). When set, the port only responds to individual port power switching commands (Set/ ClearPortPower, MEMOFST 54h[1:0] and 58h[1:0]). When cleared, the port only responds to global power switching com- mands (Set/ClearGlobalPower, MEMOFST 52h[0] and 50h[0]).									
MEMOFST 50h		HENDALT AL ARADOLES DE L	HcRhStatus	Register - Byte 0			Default = 00h			
		Res	erved			Over-current Indicator	<u>Read:</u> Local Power Status			
						(RO): ⁽¹⁾ Reflects state of OVCR pin. 0 = No over-cur- rent condi-	Not supported. Always read 0. <u>Write:</u> Clear Global Power			
						tion 1 = Over-cur- rent condi- tion	1 = Issue Clear Global Power com- mand to ports			
(1) Bit 1 is only cleared.	valid if the No Ov	ver-current Protect	ion (MEMOFST 4	9h[4]) and Over-c	urrent Protection N	lode (MEMOFST 4	9h[3]) bits are			
MEMOFST 51h)		HcRhStatus	Register - Byte 1			Default = 00h			
Read: Device Remote Wake- up Enable ⁽¹⁾ 0 = Disabled 1 = Enabled <u>Write</u> : Set Remote Wake- up Enable 0 = No effect 1 = Sets Device Remote Wakeup Enable				Reserved						
(1) Allows port	s' Connect Status	Change Bit (MEN	IOFST 56h[0] for	Port 1 and MEMC	OFST 59h[0] for Po	ort 2) as a remote v	vakeup event.			
·				·····						



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MEMOFST 52h HcRhStatus Register - Byte 2 Default = 0 Reserved Reserved Derauter Derauter Reserved Change This bit is est Not supporter With MEMOFST 53h HcRhStatus Register - Byte 3 Default = 0 MEMOFST 53h HcRhStatus Register - Byte 3 Default = 0 MEMOFST 53h HcRhStatus Register - Byte 3 Default = 0 MEMOFST 53h HcRhStatus Register - Byte 3 Default = 0 MEMOFST 53h HcRhPort1Status Register - Byte 3 Default = 0 MEMOFST 53h HcRhPort1Status Register - Byte 3 Default = 0 MEMOFST 53h HcRhPort1Status Register - Byte 3 Default = 0 MEMOFST 54h HcRhPort1Status Register - Byte 0 Default = 0 MEMOFST 54h HcRhPort1Status Register - Byte 0 Default = 0 MEMOFST 54h HcRhPort1Status Register - Byte 0 Ead: Port Suspended MEMOFST 54h HcRhPort1Status Register - Byte 0 Ead: Port Status MEMOFST 54h HcRhPort1Status Register - Byte 0 Ead: Port Status MEMOFST 54h HcRhPort1Status Register - Byte 0 Ead: Port Status 0 = Port reset signal active (MEMOFST 50h (1) = Port reset signal active (Part condi- ant or ant or ant or ant or ant or ant or bo = No effect 1 = Port is selective resume sequence for the port Not effect 1 = Sets Po	7	6	5	4	3	2	1	0
Reserved Over-current Indicator Change Badzi Local Change Badzi Local Change Not supporte when the Over. Change Not supporte when the Over. Change Not supporte tor bit bit is set when the Over. Change Not supporte tor bit bit is set when the Over. Change Not supporte tor bit bit is set when the Over. Change Not supporte tor bit changes. Not supporte tor bit bit is 1 to clear Not supporte tor bit changes. Not support tor bit changes. Not	MEMOFST 52h			HcRhStatus Re	egister - Byte 2			Default = 00h
MEMOFST 53h HcRhStatus Register - Byte 3 Default = 0 Clear Remote Wakeup Enable (WO) Reserved Reserved Reserved 0 = No effect 1 = Clear Device Remote Wakeup Enable bit (MEMOFST 51h(7)) Read: Port Reserved Read: Port Reset Status 1 = Ort reset status sig- nal not active Read: Port sus- rent condi- signal active Read: Port sus- rent condi- tus Read: Port sus- enable dit (MEMOFST 54h Read: Port sus- rent condi- tion cator ¹⁰ 0 = Port reset status sig- nal not active Read: Port sus- rent condi- tion suspended 1 = Port dis- suspended Read: Port dis- abled 0 = No dectively write: Set Port Enable Status 0 = No effect 1 = Sets Port 1 = Sets Port tus Read: Port enabled 1 = Port as- tus Read: Port sus- rent condi- tion suspended 0 = No effect 1 = Sets Port tus Read: Port enabled 1 = Port as- tus Read: Port enable 1 = Port as- tus Read: Port enabled 1 = Port as- tus Read: Port enable tus- tus Read: Port enabled 1 =			Rese	erved			Over-current Indicator Change This bit is set when the Over- current Indica- tor bit (MEMOFST 50h[1]) changes. Write 1 to clear	Bead: Local Power Status Change Not supported. Always read 0 <u>Write:</u> Set Glo- bal Power 0 = No effect 1 = Issue Set Global Power com- mand to ports
Clear Remote Wakeup Enable (WO) Reserved 0 = No effect 1 = Clear Device Remote Wakeup Enable bit (MEMOFST 54h HeRhPortIStatus Register - Byte 0 Default = MEMOFST 54h HeRhPortIStatus Register - Byte 0 Default = Reserved Read: Port Reset Status 0 = Port reset status sig- nal not active Read: Port Reset Status Read: Port over-cur- inal not active Read: Port is suspended tion Read: Port is suspended tion Read: Port is suspended tion Read: Port is suspended 0 = No effect Read: Or discus 0 = Port discus 0 = Port discus 0 = No effect Read: Or discus 0 = No effect 0 = No effect 1 = Device resume sequence for the port Read: Port is suspended 0 = No effect Read: Port is suspended	MEMOFST 53h			HcRhStatus R	egister - Byte 3			Default = 00h
MEMOFST 54h HcRhPort1Status Register - Byte 0 Default = Reserved Read: Port Reset Status 0 = Port reset status sig- nal not active Read: Port 0 = Port reset status sig- nal not active Read: Port 0 = Port reset signal active Read: Port 0 = No over-cur- rent condi- tion Read: Port Sus- pend Status 0 = Port is not suspended Read: Port Enable Status 0 = Port dis- selectively Read: Cort Enable Status 0 = Port dis- selectively Read: Cort Enable Status 0 = Port dis- suspended 0 = No devic abled 0 = No devic connect Status 1 = Port reset signal active 1 = Port reset signal active 1 = Over-cur- rent condi- tion Suspended 1 = Port enabled 1 = Device of nected.0 Write: Set Port Reset 0 = No effect 1 = Over-cur- rent condi- tion Suspend 0 = No effect 0 = No effect 1 = Sets Port Suspend 0 = No effect 1 = Clears F enable 1 = Clears F enable <td>Enable (WO) 0 = No effect 1 = Clear Device Remote Wakeup Enable bit (MEMOFST 51h[7])</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>a day in the second</td>	Enable (WO) 0 = No effect 1 = Clear Device Remote Wakeup Enable bit (MEMOFST 51h[7])							a day in the second
ReservedBead: Port Reset StatusRead: Port Reset StatusRead: Port Over-currentRead: Port Sus- pend StatusRead: Port Enable StatusRead: Curre Connect Status0 = Port reset status sig- nal not active0 = Port reset tionIndicator ⁽¹⁾ 0 = No over-cur- rent condi- active0 = Port is not suspended0 = Port dis- abled0 = No devia connect Status1 = Port signal active Write; Set Port Reset1 = Port reset signal active1 = Over-cur- rent condi- tionsuspended Suspend1 = Port enabled1 = Device of nected.0Write; Set Port Reset0 = No effect Port Suspend1 = Over-cur- suspendedSuspend 0 = No effect0 = No effect 1 = Sets Port0 = No effect 1 = Sets Port1 = Clears F Enable1 = Sets Port Reset Sta- tus1 = Initiates sequence for the portStatusStatus1 = Clears f tus bit reflects the state of the OVECUB pin dedicated to this port. This bit is port(1) The USB core supports global over-current reporting. This bit reflects the state of the OVECUB pin dedicated to this port. This bit is portThis bit reflects the state of the OVECUB pin dedicated to this port. This bit is port	MEMOFST 54h			HcRhPort1Statu	s Register - Byte	0	·····	Default = 00h
LLU The USB core supports global over-current reporting. This bit reflects the state of the OVHCUB bin dedicated to this port. This bit is 6		Reserved		Bead: Port Reset Status 0 = Port reset status sig- nal not active 1 = Port reset signal active Write: Set Port Reset 0 = No effect 1 = Sets Port Reset Sta- tus	Bead: Port Over-current Indicator ⁽¹⁾ 0 = No over-cur- rent condi- tion 1 = Over-cur- rent condi- tion Write: Clear Port Suspend 0 = No effect 1 = Initiates selective resume sequence for the port	Read: Port Sus- pend Status 0 = Port is not suspended 1 = Port is selectively suspended Write: Set Port Suspend 0 = No effect 1 = Sets Port Suspend Status	Head: Port Enable Status 0 = Port dis- abled 1 = Port enabled Write: Set Port Enable 0 = No effect 1 = Sets Port Enable Sta- tus	Head: Current Connect Status 0 = No device connected 1 = Device con- nected. ⁽²⁾ Write: Clear Port Enable 0 = No effect 1 = Clears Port Enable Sta- tus bit (bit 1
valid if the No Over-current Protection (MEMOFST 49h[4]) bit is cleared and Over-current Protection Mode (MEMOFST 49h[3]) bit is	(1) The USB co valid if the N	re supports globa lo Over-current P	al over-current repo rotection (MEMOF	orting. This bit refle ST 49h[4]) bit is cl	cts the state of th leared and Over-c	e OVRCUR pin d current Protection	edicated to this po Mode (MEMDFST	ort. This bit is only 49h[3]) bit is set.

Table 5-2 MEMOFST 00h-5Ch



Table 5-2 MEMOFST 00h-5Ch

7	6	5	4	3	2	1	0
MEMOFST 55h			HcRhPort1Status	s Register - Byte	1		Default = 00h
 Bit 1 defines Bit 0 reflects bit 0 is alway 	the speed (and b the power state o x read as 1	Rese us idle) of the atta of the port regardle	ched device. It is c ss of the power sv	onty valid when Cu vitching mode. If th	urrent Connect Sta ne No Power Swit	Bead: Low Speed Device Attached ⁽¹⁾ 0 = Full speed device 1 = Low speed device <u>Write:</u> Clear Port Power 0 = No effect 1 = Clears Port Power Sta- tus (bit 0) atus (MEMOFST 5 ching (MEMOFST 5	Bead: Port Power Status ⁽²⁾ 0 = Port power is off 1 = Port power is on Write: Set Port Power 0 = No effect 1 = Sets Port Power Sta- tus 64h[0])bit is set. 49h[1] bit is set,
MEMOFST 56h			HcRhPort1Statu	s Register - Byte	2		Default = 00h
	Reserved		Port Reset Status Change 0 = Port reset is not com- plete 1 = Port reset is complete	Port Over- current Indica- tor Change This bit is set when the Over- current Indica- tor (MEMOFST 50h[1]) bit changes. Write 1 to clear	Port Suspend Status Change Indicates the completion of the selective resume sequence for the port. 0 = Port is not resumed 1 = Port resume is complete	Port Enable Status Change Indicates that the port has been disabled due to a hard- ware event (cleared Port Enable Status, MEMOFST 54h[1]). 0 = Port has not been dis- abled 1 = Port Enable Status has been cleared	Connect Status Change Indicates a con- nect or discon- nect event has been detected. 0 = No connect disconnect event 1 = Hardware detection of connect/dis connect event ⁽¹⁾ Write 1 to clear
(1) If the Devic	e Removable Bits	6 (MEMOFST 4Ch	[15:1]) are set, bit	0 resets to 1.			Default - 00
			Res	erved	- 3		Delaun = 00



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7	6	5	4	3	2	1	0
MEMOFST 58h			HcRhPort2Statu	s Register - Byte	0		Default = 00h
	Reserved		Read: Port Reset Status	<u>Bead:</u> Port Over-current	Read: Port Sus- pend Status	<u>Bead</u> : Port Enable Status	Read: Current Connect Status
(1) The USB cd	pre supports global	over-current repo	0 = Port reset status sig- nal not active 1 = Port reset signal active Write: Set Port Reset 0 = No effect 1 = Sets Port Reset Sta- tus	Indicator ⁽¹⁾ 0 = No over-cur- rent condi- tion 1 = Over-cur- rent condi- tion Write: Clear Port Suspend 0 = No effect 1 = Initiates selective resume sequence for the port cts the state of the	0 = Port is not suspended 1 = Port is selectively suspended <u>Write:</u> Set Port Suspend 0 = No effect 1 = Sets Port Suspend Status	0 = Port dis- abled 1 = Port enabled Write: Set Port Enable 0 = No effect 1 = Sets Port Enable Sta- tus	0 = No device connected 1 = Device con- nected. ⁽²⁾ Write: Clear Port Enable 0 = No effect 1 = Clears Port Enable Sta- tus bit (bit 1)
valid if the M (2) If the Device	lo Over-current Pro e Removable bits (I	tection (MEMOF	ST 49h[4]) bit is cl [5:0]) are set (not i	eared and Over-c removable), bit 0 is	urrent Protection s always 1.	Mode (MEMDFST	49h[3]) bit is set.
MEMOFST 59h)		HcRhPort2Statu	s Register - Byte	1		Default = 00h
		Res	served			Bead; Low Speed Device Attached ⁽¹⁾ 0 = Full speed device 1 = Low speed device Write: Clear Port Power 0 = No effect 1 = Clears Port Power Sta- tus (bit 0)	Bead: PortPower Status(2)0 = Port poweris off1 = Port poweris onWrite: Set PortPower0 = No effect1 = Sets PortPower Statustus
(1) Bit 1 define(2) Bit 0 reflectbit 0 is always	s the speed (and b is the power state o ays read as 1.	us idle) of the att f the port regard	ached device. It is less of the power s	only valid when C witching mode. If t	turrent Connect S the No Power Swi	tatus (MEMOFST	54h[0])bit is set. Γ 49h[1) bit is set,

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Table 5-2 MEMOFST 00h-5Ch



Table 5-2 MEMOFST 00h-5Ch

7	6	5	4	3	2	1	0
MEMOFST 5Ah			HcRhPort2Statu	s Register - Byte	2		Default = 00h
	Reserved		Port Reset Status Change 0 = Port reset is not com- plete 1 = Port reset is complete	Port Over- current Indica- tor Change This bit is set when the Over- current Indica- tor (MEMOFST 50h[1]) bit changes. Write 1 to clear	Port Suspend Status Change Indicates the completion of the selective resume sequence for the port. 0 = Port is not resumed 1 = Port resume is complete	Port Enable Status Change Indicates that the port has been disabled due to a hard- ware event (cleared Port Enable Status, MEMOFST 54h[1]). 0 = Port has not been dis- abled 1 = Port Enable Status has been cleared	Connect Status Change Indicates a con- nect or discon- nect event has been detected. 0 = No connect/ disconnect event 1 = Hardware detection of connect/dis- connect event ⁽¹⁾ Write 1 to clear
(1) If the Device	e Removable Bits	(MEMOFST 4Ch	[15:1]) are set, bit	0 resets to 1.			
MEMOFST 5Bh			HcRhPort2 State	us Register - Byte	e 3		Default = 00h
			Res	erved			



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5.2.1 Legacy Support Registers

Four registers are provided for legacy support:

- HceControl
 - Used to enable and control the emulation hardware and report various status information.
- HceInput
 - Emulation side of the legacy Input Buffer register.
- HceOutput
 - Emulation side of the legacy Output Buffer register where keyboard and mouse data is to be written by software.

HceStatus

- Emulation side of the legacy Status register.

These registers are located in the Host Controller Register Space; from MEMOFST 100h through 10Fh. The bit formats for these registers are described in Table 5-3.

Refer to Section 4.1.2.1, "Legacy Support" for information when accessing these registers when emulation is enabled.

Table 5-3	MEMOFST	100h-1Fh	(Legacy	y Support	Registers)
-----------	---------	----------	---------	-----------	--------------------

7	6	5	2	1	0		
MEMOFST 100h			HceControl R	egister - Byte 0			Default = 00h
IRQ12 Active Indicates that a positive transi- tion of IRQ12 from kybrd con- troller has occurred. Writing a 1 clears this bit, while writing a 0 leaves it unchanged.	IRQ1 Active Indicates that a positive transi- tion of IRQ1 from kybrd con- troller has occurred. Writing a 1 clears this bit, while writing a 0 leaves it unchanged.	GateA20 Sequence Set by HC when a data value of D1h is written to Port 64h. Cleared by HC on write to Port 64h of any value other than D1h.	External IRQEn IRQ1 and IRQ12 from kybrd controller causes emula- tion interrupt: 0 = Disable 1 = Enable This bit is inde- pendent of the Emulation Enable bit (bit 0) setting.	IRQEn If the Output Full bit (MEMOFST 10Ch[0]) = 1, HC generates IRQ1 or IRQ12. If the Aux Out- put Full bit (MEMOFST 10Ch[5]) = 0, HC generates IRQ1; if = 1, HC generates IRQ12. 0 = Disable 1 = Enable	Character Pending HC generates emulation inter- rupt when the Output Full bit (MEMOFST 10Ch(0)) = 0. 0 = Disable 1 = Enable	Emulation Interrupt (RO) A static decode of the emula- tion interrupt condition.	Emulation Enable HC is enabled for legacy emu- lation? 0 = No $1 = Yes^{(1)}$
(1) The HC deco lation interru	odes accesses to l pt at appropriate t	Ports 60h/64h and imes to invoke the	l generates IRQ1 a emulation softwa	and/or IRQ12 when ure.	n appropriate. Add	ditionally, the HC g	enerates an emu-
MEMOFST 101h	1		HceControl F	legister - Byte 1			Default = 00h
			Reserved				A20 State: Indicates cur- rent state of Gate A20 on kybrd control- ler. Used to compare against value written to Port 60h when GateA20 Sequence is active.
MEMOFST 102	h-103h		HceControl Re	gister - Bytes 2 &	3		Default = 00h
			Res	served	an and has the second of the second		ana ang ang ang ang ang ang ang ang ang



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7 6 5 4 3 2 1 0 MEMOFST 104h Default = 00h Input Data: Default = 00h • // Odata that is written to Ports 60h and 64h is captured in this register . Default = 00h Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled. MEMOFST 105h-107h Default Register - Bytes 1-3 Default = 00h Number Site of the Site Site of th	Table 5-3	MEMOFST 10	0h-1Fh (Lega	cy Support Re	egisters)							
MEMOFST 104h Hcelnput Register - Bytes 0 Default = 00h Input Data: - VO data that is written to Ports 60h and 64h is captured in this register. Befault = 00h MEMOFST 105h-107h Hcelnput Register - Bytes 1-3 Reserved Default = 00h MEMOFST 105h-107h Hcelnput Register - Bytes 1-3 Reserved Default = 00h MEMOFST 108h HceOutput Register - Bytes 0 Default = 00h Output Data: - This register hosts data that is returned when an I/O read of Port 60h is performed by application software. Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled.) MEMOFST 109h-108h HceOutput Register - Bytes 1-3 Reserved Default = 00h MEMOFST 109h-108h HceOutput Register - Bytes 1-3 Reserved Default = 00h MEMOFST 100h HceOutput Register - Bytes 1-3 Reserved Default = 00h MEMOFST 100h LocOutput Register - Bytes 1-3 Reserved Default = 00h MEMOFST 100h HceStatus Register - Bytes 1-3 Reserved Default = 00h MEMOFST 100h Used Higher Bytes 1-3 Reserved Nominally used Nominally used the Kphotes this bit Output Full HC sets this bit	7	6	5	4	3	2	1	0				
Input Data: Or data that is written to Ports 60h and 64h is captured in this register. Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled. MEMOFST 105h-107h Default = 00h Default Register - Bytes 1-3 Default = 00h Output Data: Default and Point 60h is performed by application software. Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled.) MEMOFST 108h HecoUnput Register - Bytes 1-3 Default = 00h MEMOFST 109h-10Bh HecoStatus Register - Bytes 1-3 Default = 00h Parity Time-out Aux Output Full MethorST 100h Default = 00h Parity Time-out Aux Output Full bit (MEMOFST 100h[3]) = 1 MethorSS 10ah Colspan= Register - Bytes 0 Default = 00h Output State MethorSST 100h Aux Output Full bit (MEMOFST 100h[3]) = 1 0 = Norito Aux Output Full bit (MEMOFST 100h[3]) = 1 Aux Output Full bit (MEMOFST 100h[3]) = 1 Aux Output Full bit (MEMOFST 100h	MEMOFST 104h HceInput Register - Bytes 0											
 Votati that is written to Ports 60h and 64h is captured in this register. Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled. MEMOFST 105h-107h HceOutput Register - Bytes 1-3 Cutput Data: This register hosts data that is returned when an I/O read of Port 60h is performed by application software. Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled.) MEMOFST 109h-10Bh HceOutput Register - Bytes 1-3 Reserved MEMOFST 109h-10Bh HceStatus Register - Byte 1-3 MEMOFST 100h-10Bh HceStatus Register - Byte 0 Default = 00h Reserved MEMOFST 100h-10Bh HceStatus Register - Byte 0 Default = 00h Reserved MEMOFST 100h-10Bh Assert IRO12 II (MEMOFST 102h) Houtput Full Inhibit Switch: (MEMOFST 100h-101A, at ime-out at ime-out bor(h0(3)) = 1; at and IRO2En bit (MEMOFST 100h(3)) = 1; and IRO2En bit (MEMOFST 100h(3)) = 1 and Aux Output Full bit; (MEMOFST 100h(3)) = 1 and Aux Output Full bit; (MEMOFST 100h(5)) = 0; IRO1 is generated. If the IRO2En bit (MEMOFST 100h(3)) = 1 and Aux Output Full bit; (MEMOFST 100h(5)) = 0; IRO1 is generated. If the IRO2En bit (MEMOFST 100h(3)) = 1 and Aux Output Full bit; (MEMOFST 100h(5)) = 0; IRO1 is generated. If the IRO2En bit; (MEMOFST 100h(5)) = 1 and Aux Output Full bit; (MEMOFST 100h	Input Data:											
Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled. MEMOFST 105h-107h Default = 00h Reserved MEMOFST 108h HceOutput Register - Bytes 1-3 Default = 00h Colspan="2">Default = 00h MEMOFST 109h-108h HceOutput Register - Bytes 0 Default = 00h Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled.) MEMOFST 109h-108h HceOutput Register - Bytes 1-3 Default = 00h REMOFST 109h-108h HceOutput Register - Bytes 1-3 Default = 00h REMOFST 109h-108h HceOutput Register - Bytes 0 Default = 00h REMOFST 109h-108h HceOutput Register - Bytes 0 Default = 00h Parity Time-out Aux Output Full Inhibit Switch Cmd Data Flag Input Full Output Full Indicate parity Used to indicate Assert IRO12 if Reserved Secont full bit (MEMOFST Output Full bit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRO1 is generated. Withis se	- I/O data tha	t is written to Port	s 60h and 64h is c	aptured in this reg	gister.							
MEMOFST 105h-107h Hcelnput Register - Bytes 1-3 Reserved Default = 00h MEMOFST 108h HceOutput Register - Bytes 0 Default = 00h Output Data: - - Default = 00h Output Data: - - Default = 00h Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled.) Default = 00h MEMOFST 109h-10Bh HceOutput Register - Bytes 1-3 Default = 00h Reserved Reserved Default = 00h Parify Time-out Aux Output Full Inhibits witch Reserved MEMOFST 109h-10Bh HceStatus Register - Bytes 1-3 Default = 00h Parify Inne-out Aux Output Full Inhibits witch Cmd Data Input Full HC cests this bit 0n I/O writes to Port Befault = 00h Parify Used to indicate Assert HR0721f Inhibited Cmd Data Input Full HC cests this bit 0n I/O writes to Port Boh or 6Ah HC cests this bit 10 nan I/O Default = 00h Bata InfoCher bit Inhibited 1 = Not inhibited 0 = Port 60h Nrite set of 10h(P)(2) = 1, 1 = Port 64h Sate A20 Sate A20	Note: Refer to 1	able 4-4, "Emulate	ed Registers and s	Side Effects," on p	age 18 if emulation	on is enabled.		<u> </u>				
Reserved MEMOFST 108h MceOutput Register - Bytes 0 Default = 00h Output Data: - This register hosts data that is returned when an I/O read of Port 60h is performed by appication software. Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled.) MEMOFST 109h-108h Default = 00h Reserved MEMOFST 109h-108h HecOutput Register - Bytes 1-3 Default = 00h Parity Imme-out Aux Output Full Nohibit Register - Bytes 1-3 Default = 00h Parity Used to indicate a time-out Aux Output Full Nohibit Register - Bytes 1-3 Default = 00h Parity Used to indicate a time-out Aux Output Full Reflects state of UN Kinkinth: Crud Data Nominally used as a system flag Input Full Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2" MemOFST Used to indicate a time-out Aux Output Full Reflects state of Inhibited and IRQEn bit (MEMOFST 100h(3)) = 1 and Register and Side Effects, "on page 18 if mutation is enabled. Inindicate a warm or cold bool. Gotte A20 <td colspan="12">MEMOFST 105h-107h HceInput Register - Bytes 1-3</td>	MEMOFST 105h-107h HceInput Register - Bytes 1-3											
MEMOFST 108h HceOutput Register - Bytes 0 Default = 00h Output Data: - This register hosts data that is returned when an I/O read of Port 60h is performed by application software. Note: Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled.) MEMOFST 109h-108h HceOutput Register - Bytes 1-3 Reserved Default = 00h MEMOFST 102h HceStatus Register - Byte 0 Default = 00h MEMOFST 102h HceStatus Register - Byte 0 Default = 00h Parity Time-out at me-out board/mouse Aux Output Full (MEMOFST 10Ch Inhibit Switch the keyboard on I/O writes to board/mouse Flag Input Full bit 1 on an I/O ports 60h and board/mouse Input Full bit 100 no r 64h Output Full the seyboard on I/O writes to board/mouse Flag Input Full bit 1 on an I/O bo on r 64h Input Full bit 0 on a read of bo on r 64h Output Full bit 0 on a read of boot. Output Full bit 00h(2) = 1, an emulation interrupt condi- tion exists. Output Full bit 00h(2) = 1, an emulation interrupt condi- tion exists. Inhibit switch: I an emulation interrupt condi- tion exists. Sequence. Vinhie set to 1 an emulation interrupt condi- tion exists. (1) If the IRQEn bit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. If the IRQEn bit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. It will gener- ate either IRQ				Rese	rved							
Output Data: • This register hosts data that is returned when an I/O read of Port 60h is performed by application software. Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled.) MEMOFST 109h-10Bh Default = 00h Reserved MEMOFST 109h-10Bh HecOutput Register - Bytes 1-3 Default = 00h MEMOFST 100h Netest is bit of an advector of the keyboard in this switch is bit is on advector of the keyboard in this switch is bit is on an t/O move bar for on key-board/mouse data. Aux Output Full Inhibited if the keyboard in this switch: O = Inhibited data. Flag Input Full Output Full Output Full data. at ime-out data. Aux Output Full Inhibited if the keyboard in this is witch: O = Inhibited data. Cmd Data is a system flag is on are add in this is bit is 0 and the keyboard in	MEMOFST 108h			HceOutput Re	aister - Bytes 0	<u> 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997</u>	in an	Default = 00h				
- This register hosts data that is returned when an I/O read of Port 60h is performed by application software. Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled.) MEMOFST 109h-10Bh HceOutput Register - Bytes 1-3 Reserved MEMOFST 10Ch HceStatus Register - Byte 0 Default = 00h Parity Indicates parity Used to indicate a time-out Indicates parity 100h(7) = 1 and IROE hbit (MEMOFST 10Ch(7)) = 1 and IROE hbit (MEMOFST 10Ch(7)) = 1 and Aux Output Full bit (MEMOFST 10Ch(7)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 Orbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 If the IROE hbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 If the IROE hbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 If the IROE hbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 If the IROE hbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 If the IROE hbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 If the IROE hbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 If the IROE hbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 If the IROE hbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 If the IROE hbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 If the IROE hbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 If the IROE hbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5)) = 0: IRQ1 is generated. 1 If the IROE hbit (MEMOFST 100h(3)) = 1 and Aux Output Full bit (MEMOFST 10Ch(5	Output Data:			•	.							
Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled.) Default = 00h MEMOFST 109h-10Bh Recourput Register - Bytes 1-3 Default = 00h Reserved MEMOFST 10Ch Network Default = 00h Parity Indicates parity Indicates parity Indicates parity Indicates parity Indicates parity Ioor Ney- board/mouse data. Aux Output Full Inhibit Switch Indicates parity Ioor N(D) = 1 and IPOEn bit (MEMOFST 100h(3) = 1? Inhibit Switch Inhibited Flag Inhibit Switch Inhibited Inhibit Switch Indicates a system flag boat Input Full Inhibit Switch Indicate a a merulation inhibit switch: I OCh(D) = 1 and IPOEn bit (MEMOFST 100h(3) = 1? Output Full Inhibit Switch: I Not inhibited Flag Inhibit Switch I = Not inhibited Colspan="2">Output Full I = Not inhibited 64h: I = Not inhibited I = Not inhibited I = Not inhibited I = Port 64h I on Flag Interrupt condi- interrupt condi- interrupt condi- interrupt condi- ition exists. I on Port Ioon (2) I = 1 I = Port 64h I on IQUID I Ioon (2) I = 1 I = Not Simite I Ioon (3) I = 1 and Aux Output Full bit (MEMOFST 10Ch(5)] = 0: IRQ1 is generated. IOON(1) II = 1	- This registe	r hosts data that i	s returned when a	n I/O read of Port	60h is performed	by application soft	tware.					
MEMOFST 109h-10Bh HccOutput Register - Bytes 1-3 Reserved Default = 00h MEMOFST 10ch HccStatus Register - Byte 0 Default = 00h Parity Indicates parity error on key- board/mouse data. Time-out a time-out a time-out Aux Output Full (MEMOFST 10Ch[0] = 1 and IRQEn bit (MEMOFST 10Ch[0]) = 1 and IRQEn bit (MEMOFST Aux Output Full Inhibits witch: 0 = Inhibited 1 = Not inhibits witch: 0 = Not 1 = Yes Cmd Data bit No writes to enhibited 1 = Not inhibits witch: 0 = Not 1 = Yes Mominally used to 1 on an I/C Ports 60h and 0 = Port 60h 1 = Port 60h Indicate a system flag by software to indicate a Indicate a except for the case of a except for the case of a enhibits witch: 0 = No fi 1 = Yes Output Full Not inhibits witch: 0 = No fi 1 = Yes Mellocts ate of 0 = No 1 = Yes Inhibited (MEMOFST 100h[3]) = 1 and Aux Output Full bit (MEMOFST 10Ch[5]) = 0: IRQ1 is generated. If the IRQEn bit (MEMOFST 100h[3]) = 1 and Aux Output Full bit (MEMOFST 10Ch[5]) = 1: IRQ12 is generated. Setting this bit is on alloc. (1) If the IRQEn bit (MEMOFST 100h[3]) = 1 and Aux Output Full bit (MEMOFST 10Ch[5]) = 0: IRQ1 is generated. Not initig ever- erate either IRQ1 or IRQ12 under certain condi- tions(i). (1) If the IRQEn bit (MEMOFST 100h[3]) = 1 and Aux Output Full bit (MEMOFST 10Ch[5]) = 0: IRQ1 is generated. Not ivil gene- rated. (1) If the IRQEn bit (MEMOFST 100h[3]) = 1 and Aux Output Full bit (MEMOFST 10Ch[5]) = 0: IRQ1 is generated. Default = 001 (1) If the IRQEn bit (MEMOFST 100h[3]) = 1 and Aux Output Full bit (MEMOFST 10Ch[5]) = 1: IRQ12 is gen	Note: Refer to 1	Table 4-4, "Emulat	ed Registers and	Side Effects," on p	age 18 if emulation	on is enabled.)						
Reserved MEMOFST 10Ch Default = colspan="2">Default = colspan="2">Default = colspan="2">Default = colspan="2">Default = colspan="2">Default = colspan="2">Colspan="2">Default = colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2"	MEMOFST 109h	10Bh		HceOutput Reg	gister - Bytes 1-3			Default = 00h				
MEMOFST 10ch HceStatus Register - Byte 0 Default = 00h Parity Indicates parity error on key- board/mouse data. Time-out a time-out a time-out data. Aux Output Full Assert IRQ12 if Output Full Output Full Output Full Output Full Output Full Output Full Output Full Coutput Full Coutput Full Coutput Full Do on a read of Port 60h or 64h 1 = Not inhibited 1 = Port 60h 1				Rese	erved							
Parity Indicates parity error on key- board/mouse data. Time-out used to indicate a time-out Aux Output Full Assert IRQ12 if Output Full bit (MEMOFST 10Ch[0] = 1 and IRQEn bit (MEMOFST 100h[3]) = 1? Inhibit Switch the keyboard inhibit switch: 0 = Inhibited Cmd Data HC sets this bit on I/O writes to Ports 60h and 64h: 0 = Port 60h Flag HC sets this bit to 1 on an I/O by software to indicate a Input Full HC sets this bit to 0 on a read of port 60h. While warm or cold boot. 10 10 10 10 1 Nominally used inhibit switch: 0 Nominally used as a system flag by software to indicate a HC sets this bit to 1 on an I/O by software to indicate a HC sets this bit to 0 on a read of except for the case of a 10 10 10 1 Nominally used and IRQEn bit (MEMOFST 1 Nominally used inhibited HC sets this bit to 1 on an I/O by software to indicate a HC sets this bit to 0 on a read of except for the case of a HC sets this bit to 0 no a read of except for the case of a 1 Port 64h 1 Not inhibited 1 Port 64h Warm or cold boot. Warm or cold boot. Setting this bit to 0 no read of except for the case of a (1) If the IRQEn bit (MEMOFST 100h[3]) = 1 and Aux Output Full bit (MEMOFST 10Ch[5]) = 0: IRQ1 is generated. Inhibit switch (MEMOFST 10Ch[5]) = 1: IRQ12 is generated. Inhibit switch (to ns ⁽¹⁾). (1) If the IRQEn bit (MEMOFST 100h[3]	MEMOFST 10C	n N		HceStatus Re	egister - Byte 0		na an a	Default = 00h				
Indicates parity error on key- board/mouse Used to indicate a time-out Assert IRQ12 if Output Full bit (MEMOFST Medicets state of the keyboard inhibit switch: 10Ch[0] = 1 and IRQEn bit (MEMOFST HC sets this bit to 1 on an I/O HC sets this bit to 1 on an I/O HC sets this bit to 1 on an I/O 0 ata. a time-out Medicets state of the keyboard HC sets this bit to 0 rest 60h and 1 = Not inhibited HC sets this bit to 1 on an I/O HC sets this bit to 0 on a read of ports 60h and 1 = Port 60h 0 = No 1 = Yes 1 = Not inhibited 0 = Port 60h 1 = Port 64h Medicets at to 0 = Port 60h 1 = Port 64h Medicets at an emulation indicate a and emulation is enabled Medicets at to 0 on a read of to 1 on exists. (1) If t	Parity	Time-out	Aux Output Full	Inhibit Switch	Cmd Data	Flag	Input Full	Output Full				
(1) If the IRQEn bit (MEMOFST 100h[3]) = 1 and Aux Output Full bit (MEMOFST 10Ch[5]) = 0: IRQ1 is generated. If the IRQEn bit (MEMOFST 100h[3]) = 1 and Aux Output Full bit (MEMOFST 10Ch[5]) = 1: IRQ12 is generated. Note: Refer to Table 4-4, "Emulated Registers and Side Effects," on page 18 if emulation is enabled. MEMOFST 10Dh-10Fh HceStatus Register - Bytes 1-3 Reserved	Indicates parity error on key- board/mouse data.	Used to indicate a time-out	Assert IRQ12 if Output Full bit (MEMOFST 10Ch[0]) = 1 and IRQEn bit (MEMOFST 100h[3]) = 1? 0 = No 1 = Yes	Reflects state of the keyboard inhibit switch: 0 = Inhibited 1 = Not inhibited	HC sets this bit on I/O writes to Ports 60h and 64h: 0 = Port 60h 1 = Port 64h	Nominally used as a system flag by software to indicate a warm or cold boot.	HC sets this bit to 1 on an I/O write to Port 60h or 64h except for the case of a GateA20 Sequence. While set to 1 and emulation is enabled (MEMOFST 100h[0] = 1), an emulation interrupt condi- tion exists.	HC sets this bit to 0 on a read of Port 60h. While this bit is 0 and the Character Pending bit (MEMOFST 100h[2]) = 1, an emulation interrupt condi- tion exists. Setting this bit to 1 will gener- ate either IRQ1 or IRQ12 under certain condi- tions ⁽¹⁾ .				
MEMOFST 10Dh-10Fh HceStatus Register - Bytes 1-3 Default = 001 Reserved	(1) If the IRQEr If the IRQEn Note: Refer to	bit (MEMOFST 1 bit (MEMOFST 1 Table 4-4, "Emula	00h[3]) = 1 and Au 00h[3]) = 1 and Au ted Registers and	ux Output Full bit (ux Output Full bit (Side Effects," on j	MEMOFST 10Ch MEMOFST 10Ch page 18 if emulat	[5]) = 0: IRQ1 is g [5]) = 1: IRQ12 is ion is enabled.	enerated. generated.	ul				
Reserved	MEMOFST 10D	h-10Fh		HceStatus Re	gister - Bytes 1-3	3		Default = 00h				
				Res	erved							



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6.0 Electrical Ratings

Stresses above those listed in the following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied.

6.1 Absolute Maximum Ratings

		5.	0 Volt	3.		
Symbol	Parameter	Min	Max	Min	Мах	Unit
VCC	Supply Voltage		+6.5		+4.0	V
VI	Input Voltage	-0.5	VCC + 0.5	-0.5	VCC + 0.5	ν
vo	Output Voltage	-0.5	VCC + 0.5	-0.5	VCC + 0.5	V
ТОР	Operating Temperature	0	+70	0	+70	°C
TSTG	Storage Temperature	-40	+125	-40	+125	°C

6.2 DC Characteristics: VCC = 3.3V or 5.0V ±5%, TA = 0°C to +70°C

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input low Voltage	-0.5	+0.8	v	
VIH	Input high Voltage	+2.0	VCC + 0.5	V	
VOL	Output low Voltage		+0.4	V	IOL = 4.0mA
VOH	Output high Voltage	+2.4 V		V	IOH = -1.6mA
IIL	Input Leakage Current		+10.0	μA	VIN = VCC
IOZ	Tristate Leakage Current		+10.0	μA	
CIN	Input Capacitance		+10.0	pF	
COUT	Output Capacitance		+10.0	pF	
ICC	Power Supply Current: 3.3V Core	45mA ty below 1	pical during Norma mA at Standby		



6.3 AC Characteristics (Preliminary)

6.3.1 PCI Bus AC Timings

Sym	Parameter	Min	Max	Unit	Figure
t100	C/BE[3:0]#, AD[31:0], FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, LOCK#, PAR, SERR#, PERR# setup time to PCICLK rising	7		ns	6-1
t101	C/BE[3:0]#, AD[31:0], FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, LOCK#, PAR, SERR#, PERR# hold time from PCICLK rising	0		ns	6-2
t102	C/BE[3:0]#, AD[31:0], FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, LOCK#, PAR, SERR#, PERR# valid delay from PCICLK rising	2	11	ns	6-3
t103	REQ# setup time to PCICLK rising	12		ns	6-1
t104	REQ# hold time from PCICLK rising	0		ns	6-2
t105	GNT# valid delay from PCICLK rising	2	12	ns	6-3

Figure 6-1 Setup Timing Waveform



Figure 6-2 Hold Timing Waveform



Figure 6-3 Output Delay Timing Waveform



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Sym	Parameter	Min	Мах	Unit	Figure	Condition (Notes 1, 2, and 3)								
Driver Cha	Driver Characteristics													
tR tF	Transition Time: Rise Time Fall Time	4 4	20 20	ns ns		CL = 50pF, Notes 5 and 6								
tRFM	Rise/Fall Time Matching	90	110	%		(tR/tF)								
vCRS	Output Signal Crossover Voltage	1.3	2.0	V										
zDRV	Driver Output Resistance	28	43	ohm		Steady state drive								
Data Sour	Data Source Timings													
tDRATE	Full Speed Data Rate	11.97	12.03	Mb/s		Average bit rate = 12Mb/s ±0.25%								
tFRAME	Frame Interval	0.9995	1.0005	ms		1.0ms ±0.05%								
tDJ1 tDJ2	Source Differential Driver Jitter: To Next Transition For Paired Transitions	3.5 4.0	3.5 4.0	ns ns		Notes 7 and 8								
tEOPT	Source EOP Width	160	175	ns		Note 8								
tDEOP	Differential to EOP Transition Skew	-2	5	ns		Note 8								
tJR1 tJR2	Receiver Data Jitter Tolerance: To Next Transition For Paired Transitions	-18.5 -9	18.5 9	ns ns		Note 8								
tEOPR1 tEOPR2	EOP Width at Receiver: Must Reject at EOP Must Accept as EOP	40 82		ns ns		Note 8								

6.3.2 USB AC Timings: Full Speed Source



6.3.3 USB AC Timings: Low Speed Source

Sym	Parameter	Min	Max	Unit	Figure	Condition (Notes 1, 2, and 4)
Driver Ch	aracteristics					
tR tF	Transition Time: Rise Time Fall Time	75 75	300 300	ns ns		Notes 5 and 6 Min# measured with: CL = 50pF Max# measured with: CL = 350pF
tRFM	Rise/Fall Time Matching	80	120	%		(tR/tF)
vCRS	Output Signal Crossover Voltage	1.3	2.0	v		
Data Sou	rce Timings					
tDRATE	Low Speed Data Rate	1.4775	1.5225	Mb/s		Average bit rate = 1.5Mb/s ±1.5%
tDDJ1 tDDJ2	Source Differential Driver Jitter, At Host (Downstream): To Next Transition For Paired Transitions	-75 -45	75 45	ns ns		Notes 7 and 8
tUDJ1 tUDJ2	Source Differential Driver Jitter, At Function (Upstream): To Next Transition For Paired Transitions	-95 -150	95 150	ns ns		Notes 7 and 8
tEOPT	Source EOP Width	1.25	150	μs	6-5	Note 8
tDEOP	Differential to EOP Transition Skew	-40	100	ns	6-5	Note 8
tUJR1 tUJR2	Receiver Data Jitter Tolerance, At Host (Upstream): To Next Transition For Paired Transitions	152 200	152 200	ns ns	6-6	
tDJR1 tDJR2	Receiver Data Jitter Tolerance, At Function (Downstream): To Next Transition For Paired Transitions	75 45	75 45	ns ns	6-6	
tEOPR1 tEOPR2	EOP Width at Receiver: Must Reject at EOP Must Accept as EOP	330 675		ns ns	6-6	Note 8

Notes: 1. All voltages measured from the local ground potential, unless otherwise specified.

- 2. All timings use a capacitive load (CL) to ground of 50pF, unless otherwise specified.
- 3. Full speed timings have a 1.5 kohm pull-up to 2.8V on the D+ data line.
- 4. Low speed timings have a 1.5 kohm pull-up to 2.8V on the D- line.
- 5. Measured from 10% to 90% of the data signal.
- 6. The rising and falling edges should be smoothly transitioning (monotonic).
- 7. Timing difference between the differential data signals.
- 8. Measured at crossover point of differential data signals.
- 9. The maximum load specification is the maximum effective capacitive load allowed that meets the target hub Vbus droop of 330mV.



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Figure 6-4 Differential Data Jitter













7.0 Mechanical Package Outlines

Figure 7-1 100-Pin Low-Profile Quad Flat Pack (LQFP)



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Dwg Rev: A0 Unit MM INCH															Figure 7-2 100-Pin Quad Flat Pack (Q	
	W	ILLIME	TER		INCH			¢					m	T	FP)	
SYMBOL	MIN.	NOM.	MAX	MIN.	NOM.	MAX.		T						0		
A1	0.25	0.35	0.45	0.010	0.014	0.018		4 				and the second sec	s i del l'interes en resource en esp	A Contraction and the second		
A2	2.57	2.72	2.87	0.101	0.107	0.113						3		and the second states		
b	0.20	0.30	0.40	0 008	0.012	0.016		U.134						A CONTRACTOR OF		
c	0.10	0.15	0.20	0.004	0.005	0.008				· · · · · · · · · · · · · · · · · · ·	*****	Barrows and the second se	!			
D	13.90	14.00	14.10	0.547	0.551	0.655	l.	3					and a second state	Ĵ		
E	19.90	20.00	20.10	0.783	0.787	0.791	*	1	9							
e	Arrows & California	0.65			0.026											6
Hd	17.00	17.20	17.40	0.669	0.677	0.685			,							
He	23.00	23.20	23.40	0.905	0.913	0.921		o) مېسى				24	>		١ <u></u>
L	0.65	0.80	0.95	0.025	0.031	0.037		۱ <u> </u>								61 10
L1		1.60	****		0.063			T				,				182 182
Y		- A loss of a second second	0.08		No. of Manager	0.003			L				~			O
0	0		7	Q	And a function of the state of	7			L							1 <i>ar</i>
L	4		*	. <u></u>												ーしん

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