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**USB 2.0**

**82C871**

**On-The-Go Controller**

**Data Book**

912-2003-001  
Revision 1.1  
25 March 2003

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## 1 DESCRIPTION

The 82C871 is an USB 2.0 compliant On-The-Go device controller LSI that supports Full Speed (12Mbps) mode. In addition to the Host and the Function functions, it integrates the On-The-Go function to a single chip, making the LSI a dual-role device.

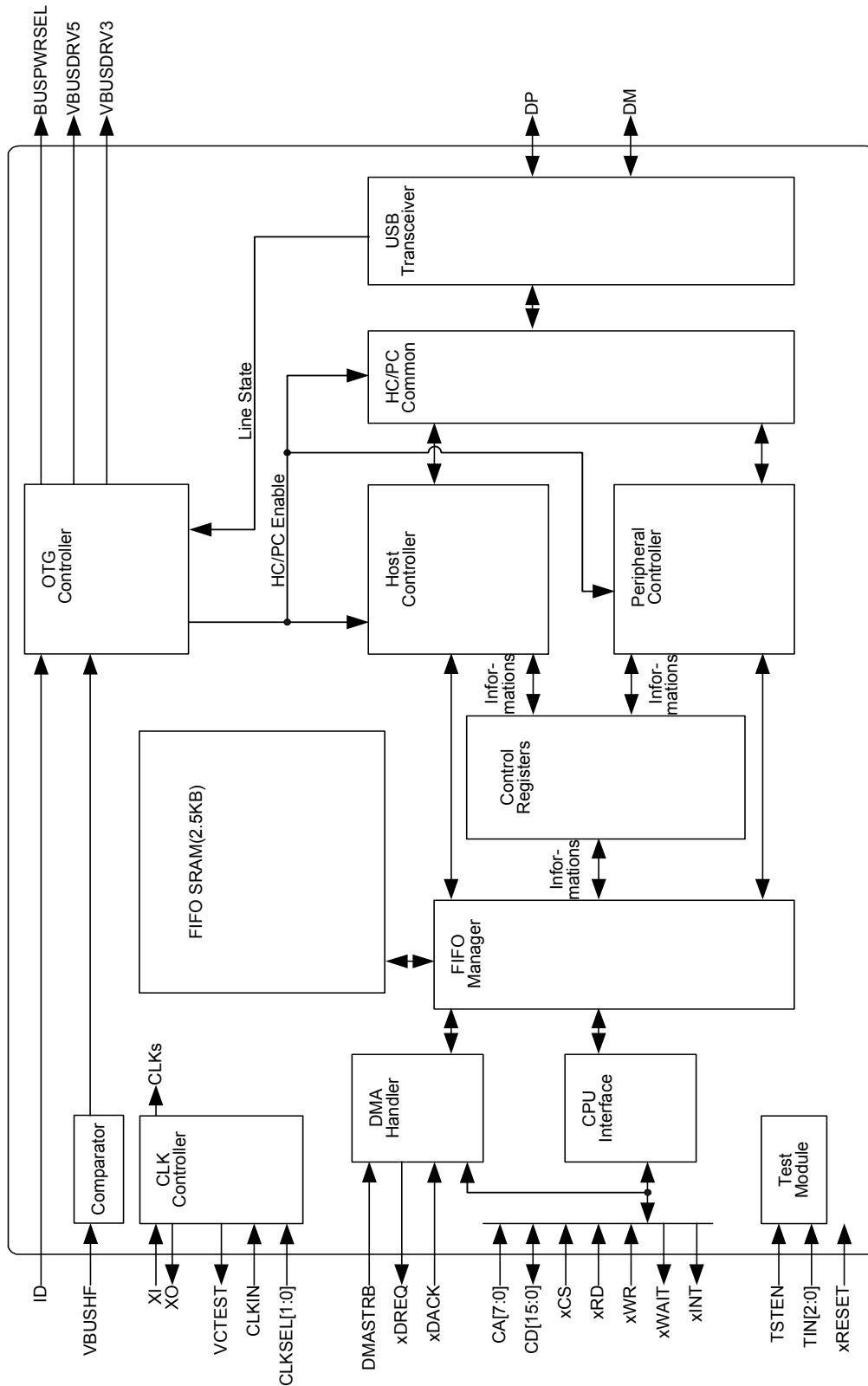
It provides not only a general connectivity between the USB device and the PC, but also an unlimited connectivity between two USB devices.

## 2 FEATURES

- Integrates the Host, the Function and the On-The-Go functions into a single chip.
- Compliant with On-The-Go (Supplement to the USB2.0) version 1.0.
- Supports USB2.0 Full Speed (12Mbps) mode.
- Equipped with one On-The-Go port.
- Supports control, bulk, interrupt and Isochronous transfers.
- Is a controller interface that achieves lower CPU load and high throughput during USB transfer.
- Supports five general Endpoint and Endpoint 0.
- Has built-in 2.5KByteFIFO for data transfer.
- FIFO uses ring buffer method.
- Installed with 16-bit width generic CPU Interface.
- Operates as 16-bit width generic DMA slave (shares bus with CPU Interface).
- Supports clock input 12 MHz oscillator (built-in oscillation circuit).
- Has built-in multiplier PLL circuit.
- Supports external clock input of 12MHz, 27MHz and 48MHz from the crystal oscillator.
- Has low power consumption which is achieved through thorough clock control.
- Is two-power operated (3.3 V and 2.5 V. I/O power supply: 3.3V, internal operation power: 2.5V).
- 81-pin CSP package or 64-pin QFP package.

※ No anti-radiation design

3 BLOCK DIAGRAM



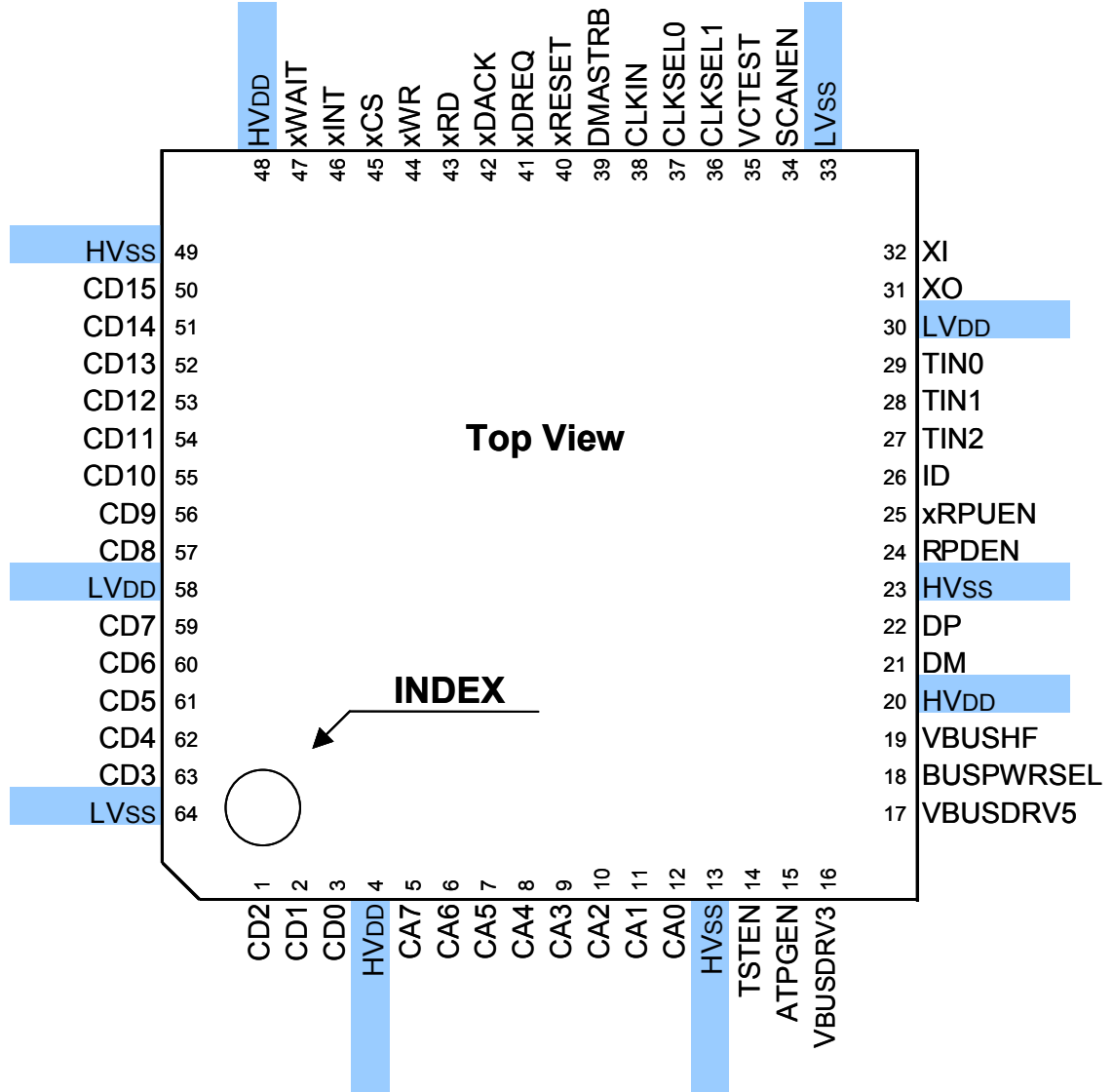
## 4 PIN ASSIGNMENT

### 4.1 CSP Package

J	—	V <sub>BUS</sub> DRV5	V <sub>BUS</sub> HF	DM	RPDEN	ID	LV <sub>DD</sub>	XI	—
H	V <sub>BUS</sub> DRV3	HV <sub>SS</sub>	BUS PWRSEL	DP	HV <sub>SS</sub>	TIN2	XO	TIN0	LV <sub>SS</sub>
G	TSTEN	ATPGEN	HV <sub>DD</sub>	—	TEST PAD0	TIN1	CLKSEL1	SCANEN	VCTEST
F	CA2	CA1	CA0	VTEST11	XRPDEN	—	—	CLKIN	CLKSEL0
E	CA3	CA4	CA5	VTEST01	—	COMPIN 22	DMA STRB	XRESET	XDREQ
D	CA7	CA6	—	—	—	COMPIN 10	XWR	XRD	XDACK
C	CD0	CD1	HV <sub>DD</sub>	CD6	CD10	—	CD13	XWAIT	XINT
B	CD2	CD5	CD3	CD7	CD9	CD11	CD15	XCS	HV <sub>DD</sub>
A	—	LV <sub>SS</sub>	CD4	LV <sub>DD</sub>	CD8	CD12	CD14	HV <sub>SS</sub>	—
	1	2	3	4	5	6	7	8	9

Bottom View

4.2 QFP Package



## 5 PIN DESCRIPTION

### 5.1 CPU Interface

Symbol	Pin name	Pin number		Pin type	Description
		CSP	QFP		
DMASTRB	DMA Strobe	E7	39	I (Gated CMOS)	Strobe signal for burst DMA transfer. Connect to GND (HVss) when not in use.
xDREQ	DMA Request	E9	41	O (3-state 3mA)	DMA transfer request. Initial state is HiZ. Select either low active or high active from register setting.
xDACK	DMA Acknowledge	D9	42	I (Gated CMOS)	DMA transfer permission.
xRD	Read Strobe	D8	43	I (Gated CMOS)	CPU read strobe.
xWR	Write Strobe	D7	44	I (Gated CMOS)	CPU write strobe.
xCS	Chip Select	B8	45	I (CMOS)	Chip select signal.
xINT	Interrupt signal	C9	46	O (3-state 3mA)	Interruption signal to the CPU. Initial state is HiZ. Select either HiZ/0 or 1/0 from register setting.
xWAIT	Wait signal	C8	47	O (3-state 3mA)	Wait signal to the CPU. Initial state is HiZ. Select either HiZ/0 or 1/0 from register setting.
CD15 CD14 CD13 CD12 CD11 CD10 CD9 CD8 CD7 CD6 CD5 CD4 CD3 CD2 CD1 CD0	CPU Data	B7 A7 C7 A6 B6 C5 B5 A5 B4 C4 B2 A3 B3 B1 C2 C1	50 51 52 53 54 55 56 57 59 60 61 62 63 1 2 3	I/O (Gated CMOS 3mA)	CPU data bus. Initial state is Input mode. Outputs register data during read, and sets register data from the CPU during write. Shares with DMA data bus.
CA7 CA6 CA5 CA4 CA3 CA2 CA1 CA0	CPU Address	D1 D2 E3 E2 E1 F1 F2 F3	5 6 7 8 9 10 11 12	I (Gated CMOS)	CPU address bus. Specifies the register address.



## 5.2 USB Interface

Symbol	Pin name	Pin number		Pin type	Description
		CSP	QFP		
VBUSDRV3	Vbus Drive	H1	16	O (3mA)	Enables VBUS3.3V drive. 0: disable, 1: enable Initial state is disable. Open when not in use.
VBUSDRV5	Vbus Drive	J2	17	O (3mA)	Enables VBUS5V drive (Max. 8mA). 0: disable, 1: enable Initial state is disable.
BUSPWRSEL	Vbus Drive	H3	18	O (3mA)	Enables VBUS5V drive (over 8mA). 0: disable, 1: enable Initial state is disable.
COMPIN10	1.0V level Detection signal	D6	—	I (CMOS 120kΩ with pull down)	Vbus/2 level detection result (1.0V). 0:Vbus/2 < 1.0V, 1:Vbus/2 ≥ 1.0V Connect to GND when using internal comparator.
COMPIN22	2.2V level Detection signal	E6	—	I (CMOS 120kΩ with pull down)	Vbus/2 level detection result (2.2V). 0:Vbus/2 < 2.2V, 1:Vbus/2 ≥ 2.2V Connect to GND when using internal comparator.
DM	USB negative pole signal	J4	21	I/O (special)	USB data line D-
DP	USB positive pole signal	H4	22	I/O (special)	USB data line D+
RPDEN	Rpd Enable	J5	24	O (3mA)	Enable D+ pull down. 0: disable, 1: enable Open when internal resistor is not in use.
xRPUEN	Rpu Enable	F5	25	O (3mA)	Enable D+ pull up. 0: enable, 1: disable Open when internal resistor is not in use.
ID	ID signal	J6	26	I (CMOS Schmitt 120kΩ with pull up)	ID signal 0: A-Device, 1: B-Device
VBUSHF	Vbus/2	J3	19	I (special)	Vbus/2 level Connect to GND when using external comparator.

### 5.3 System

Symbol	Pin name	Pin number		Pin type	Description
		CSP	QFP		
XO	Oscillator output	H7	31	O (special)	Output for built-in oscillation circuit. Open when not in use.
XI	Oscillator input	J8	32	I (special)	Input for built-in oscillation circuit. Connect to GND (LVss) through pull down resistor when not in use.
VCTEST	PLL filter test	G9	35	O (special)	PLL filter circuit test pin
CLKSEL1 CLKSEL0	Clock selection	G7 F9	36 37	I (CMOS Schmidt)	Selection pin for oscillator or external clock use. CLKSEL[1:0] Uses 00: 12MHz oscillator. Uses 01: external 27MHz clock input. Uses 10: external 48MHz clock input. 11: not used.
CLKIN	External clock input	F8	38	I (TTL)	External clock input. Connect to GND (HVss) when not in use. When using external clock input, clock supply should be stable before reset release.
XRESET	Chip reset	E8	40	I (CMOS Schmidt 120kΩ with pull up)	Chip reset

### 5.4 Test Signals

Symbol	Pin name	Pin number		Pin type	Description
		CSP	QFP		
TIN2 TIN1 TIN0	Test mode	H6 G6 H8	27 28 29	I (CMOS Schmidt 120kΩ with pull down)	Mode setting input pin 000: Normal Others: Internal test mode Connect to GND (HVss) during normal use.
TSTEN	Test enable	G1	14	I (TEST I/O)	Test enable pin 0: Normal, 1: Test Connect to GND (HVss) during normal use.
TESTPAD0	Internal pull up resistor 2 measurement pin	G5	—	O (special)	Test pin Open when not in use.
VTEST01	Reference voltage monitor	E4	—	O (special)	Test pin Open when not in use.

VTEST11	Reference voltage monitor	F4	—	O (special)	Test pin Open when not in use.
ATPGEN	Test ATPG	G2	15	I (CMOS Schmitt 120k $\Omega$ with pull down)	Test pin Connect to GND (HVss) during normal use.
SCANEN	Test SCAN	G8	34	I (CMOS Schmitt 120k $\Omega$ with pull down)	Test pin Connect to GND (HVss) during normal use.

## 5.5 Power Supply, GND, etc.

Symbol	Pin name	Pin number		Pin type	Description
		CSP	QFP		
HVDD	Power Supply for I/O Part	C3 G3 B9	4 20 48	P	3.3V power supply pin for I/O
HVss	Ground for I/O Part	H2 H5 A8	13 23 49	P	Ground pin for I/O
LVDD	Power Supply for Logic part	J7 A4	30 58	P	2.5V power supply pin for internal use
LVss	Ground for Logic part	H9 A2	33 64	P	Ground pin for internal use
NC	None Connect	C6 D3 D4 D5 E5 F6 F7 G4 A1 A9 J1 J9	—	—	Unused pin Open during normal use.

## 6 FUNCTIONAL DESCRIPTION

### 6.1 Host Controller (HC)

- Arbitrates multiple transactions, manages time frame, schedules transfers and manages retransmission.
- Manages transactions.
- Generates/disassembles packets.
- Indicates suspend/resume reset state generation.

### 6.2 Peripheral Controller (PC)

- Manages end point operation information via register.
- Manages transactions.
- Generates/disassembles packets.
- Indicates remote wakeup signal generation.

### 6.3 OTG Controller

- Monitors USB data line state (including connect and disconnect).
- Monitors VBUS level.
- Monitors ID.
- Controls VBUS drive/stop, pull up/pull down resistor (D+) connect/disconnect and HC/PC enable and disable for OTG operation.

### 6.4 HC/PC Common

- Indicates USB data line state generation.
- Switches connection between HC or the PC for the USB Transceiver.

### 6.5 USB Transceiver

- Processes parallel/serial conversion.
- Processes bit stuffing/unstuffing.
- Performs NRZI encode/decode process.
- Sends and receives USB data signals.
- Generates USB data line state.

### 6.6 Control Registers

- Holds register group related to transaction and end point control.

## 6.7 FIFO Manager

- Manages FIFO access address of the CPU/DMA and USB.
- Manages FIFO access arbitration of the CPU/DMA and USB.

## 6.8 FIFO SRAM

- Uses it as FIFO for data transfer (total: 2.5KByte).

## 6.9 CPU Interface

- Controls PIO transfer.
- Generates interrupt signal to the CPU.

## 6.10 DMA Handler

- Controls DMA transfer (DMA slave).

## 6.11 CLK Controller

- Generates various clocks used internally from the multiplier PLL (when an oscillator is used) or from the external input clock.
- Controls clock operation that is used per block.

## 6.12 Test Module

- Performs internal operation verification test.

## 7 ELECTRICAL CHARACTERISTICS

### 7.1 Absolute Maximum Ratings

(V<sub>SS</sub>=0V)

Item	Symbol	Rated values	Unit
Power supply voltage	HVDD*	-0.3 to +4.0	V
	LVDD*	-0.3 to +3.0	V
Input voltage	HVI	-0.3 to HVDD+0.5	V
	LVI	-0.3 to LVDD+0.5	V
Output voltage	HVO	-0.3 to HVDD+0.5	V
	LVO	-0.3 to LVDD+0.5	V
Output current/pin	I <sub>OUT</sub>	±30	mA
Storage temperature	T <sub>stg</sub>	-65 to +150	°C

\*HV<sub>DD</sub> ≥ LV<sub>DD</sub>

### 7.2 Recommended operating condition

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	HVDD	3.00	3.30	3.60	V
	LVDD	2.30	2.50	2.70	V
Input voltage	HVI	V <sub>SS</sub>	—	HVDD	V
	LVI	V <sub>SS</sub>	—	LVDD	V
Ambient temperature	T <sub>a</sub>	-20	25	85	°C

### 7.3 DC Characteristics

#### DC Characteristics (on recommended operating condition) (1)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption						
Power supply current	I <sub>DDH</sub>	HV <sub>DD</sub> = 3.6V	—	—	20	mA
	I <sub>DDL</sub>	LV <sub>DD</sub> = 2.7V	—	—	40	mA
Static current (static current between HV <sub>DD</sub> and V <sub>SS</sub> )						
Power supply current	I <sub>DDSH</sub>	V <sub>IN</sub> = HV <sub>DD</sub> or LV <sub>DD</sub> or V <sub>SS</sub> HV <sub>DD</sub> = 3.6V LV <sub>DD</sub> = 2.7V	—	—	30	μA
Static current (static current between LV <sub>DD</sub> and V <sub>SS</sub> )						
Power supply current	I <sub>DDSL</sub>	V <sub>IN</sub> = HV <sub>DD</sub> or LV <sub>DD</sub> or V <sub>SS</sub> HV <sub>DD</sub> = 3.6V LV <sub>DD</sub> = 2.7V	—	—	120	μA
Input leak						
Input leak current	I <sub>L</sub>	V <sub>IN</sub> = HV <sub>DD</sub> or LV <sub>DD</sub> or V <sub>SS</sub>  HV <sub>DD</sub> = 3.6V LV <sub>DD</sub> = 2.7V H <sub>VIH</sub> = HV <sub>DD</sub> L <sub>VIL</sub> = LV <sub>DD</sub> V <sub>IL</sub> = V <sub>SS</sub>	-5	—	5	μA

## DC Characteristics (on recommended operating condition) (2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input characteristics (CMOS) Pin name: CA7..CA0, CD15..CD0, TESTEN,xCS, xDACK, xRD, xWR, DMASTRB, COMPIN10, COMPIN22						
HIGH level input voltage	V <sub>IH1H</sub>	HV <sub>DD</sub> = 3.6V	2.2	—	—	V
LOW level input voltage	V <sub>IL1H</sub>	HV <sub>DD</sub> = 3.0V	—	—	0.8	V
Schmitt input characteristics (CMOS) Pin name: ID, xRESET, CLKSEL1, CLKSEL0, TIN2, TIN1, TIN0, SCANEN, ATPGEN						
HIGH level trigger voltage	V <sub>T1+</sub>	HV <sub>DD</sub> = 3.6V	1.4	—	2.7	V
LOW level trigger voltage	V <sub>T1-</sub>	HV <sub>DD</sub> = 3.0V	0.6	—	1.8	V
Hysteresis voltage	ΔV <sub>1</sub>	HV <sub>DD</sub> = 3.0V	0.3	—	—	V
Input characteristics (LVTTTL) Pin name: CLKIN						
HIGH level input voltage	V <sub>IH2H</sub>	HV <sub>DD</sub> = 3.6V	2.0	—	—	V
LOW level input voltage	V <sub>IL2H</sub>	HV <sub>DD</sub> = 3.0V	—	—	0.8	V
Schmitt input characteristics (USB: FS) Pin name: DP, DM						
HIGH level trigger voltage	V <sub>T+(USB)</sub>	HV <sub>DD</sub> = 3.6V	1.1	—	1.8	V
LOW level trigger voltage	V <sub>T-(USB)</sub>	HV <sub>DD</sub> = 3.0V	1.0	—	1.5	V
Hysteresis voltage	ΔV <sub>(USB)</sub>	HV <sub>DD</sub> = 3.0V	0.1	—	—	V
Input characteristics (USB: FS difference input) Pin name: DP and DM pair						
Sensitivity of difference input	V <sub>DS(USB)</sub>	HV <sub>DD</sub> = 3.0V Difference input voltage 0.8V to 2.5V	—	—	0.2	V
Input pull up characteristics Pin name: ID, xRESET						
Pull up resistance value	R <sub>PU2</sub>	HV <sub>DD</sub> = 3.3V V <sub>IH</sub> = V <sub>SS</sub>	60	120	288	kΩ
Input pull down characteristics Pin name: SCANEN, ATPGEN, TIN2, TIN1, TIN0, COMPIN10, COMPIN22						
Pull down resistance value	R <sub>PD2</sub>	HV <sub>DD</sub> = 3.3V V <sub>IH</sub> = V <sub>SS</sub>	60	120	288	kΩ



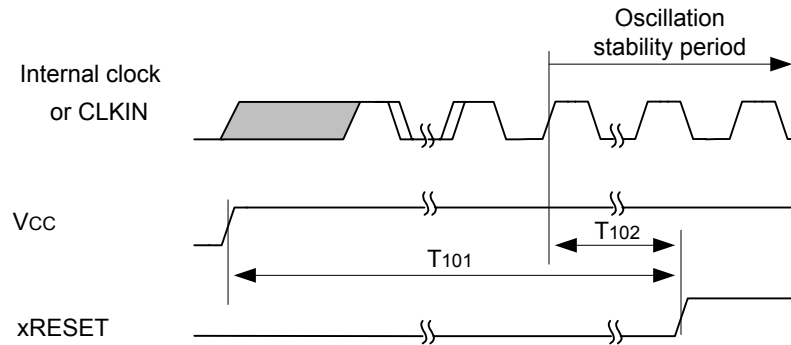
## DC Characteristics (on recommended operating condition) (3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output characteristics						
Pin name: xRPUEN, RPDEN, VBUSDRV3, VBUSDRV5, BUSPWRSEL, CD15..CD0, xINT, xWAIT, xDREQ,						
HIGH level output voltage	VOH1H	HVDD = 3.0V IOH = -3mA	VDD-0.4	—	—	V
LOW level output voltage	VOL1H	HVDD = 3.0V IOL = 3mA	—	—	0.4	V
Output characteristics (USB: FS)						
Pin name: DP, DM						
HIGH level output voltage	VOH(USB)	HVDD = 3.0V	2.8	—	—	V
LOW level output voltage	VOL(USB)	HVDD = 3.6V	—	—	0.3	V
Output characteristics						
Pin name: xRPUEN, RPDEN, VBUSDRV3, VBUSDRV5, BUSPWRSEL, CD15..CD0, xINT, xWAIT, xDREQ						
OFF-STATE leak current	IOZ1H	HVDD = 3.6V VOH = VDD VOL = VSS	-5	—	5	μA
Pin capacity						
Pin name: all input pins						
Input pin capacity	CI	f = 1MHz VDD = VSS	—	—	8	pF
Pin capacity						
Pin name: all output pins						
Output pin capacity	CO	f = 1MHz VDD = VSS	—	—	8	pF
Pin capacity						
Pin name: all input and output pins						
Input and output pin capacity	CIO	f = 1MHz VDD = VSS	—	—	8	pF

7.4 AC Characteristics

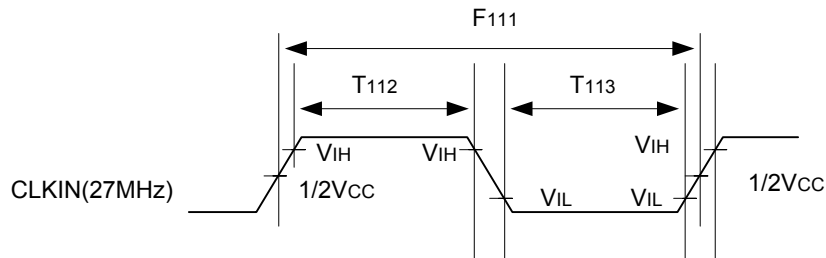
7.4.1 Clock timing

7.4.1.1 Oscillation Stability Time During Power On



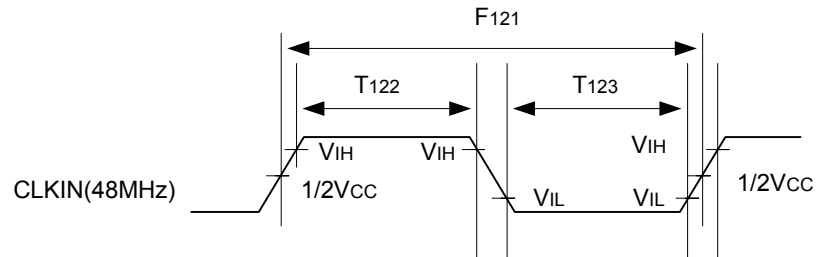
Symbol	Description	Min.	Typ.	Max.	Unit
T101	Oscillation stability time during power on	10	—	—	ms
T102	xRESET setup time	200	—	—	μs

7.4.1.2 CLKIN (27MHz) Clock Input Timing



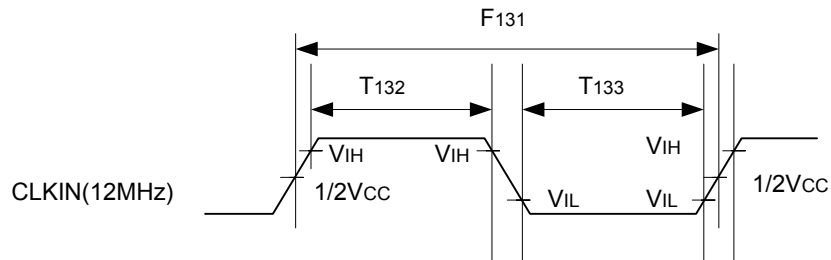
Symbol	Description	Min.	Typ.	Max.	Unit
F111	Clock input frequency	26.9973	27	27.0027	MHz
T112	Clock input HIGH level pulse width	12	—	23	ns
T113	Clock input LOW level pulse width	12	—	23	ns

## 7.4.1.3 CLKIN (48MHz) Clock Input Timing



Symbol	Description	Min.	Typ.	Max.	Unit
F <sub>121</sub>	Clock input frequency	47.9952	48	48.0048	MHz
T <sub>122</sub>	Clock input HIGH level pulse width	7	—	13	ns
T <sub>123</sub>	Clock input LOW level pulse width	7	—	13	ns

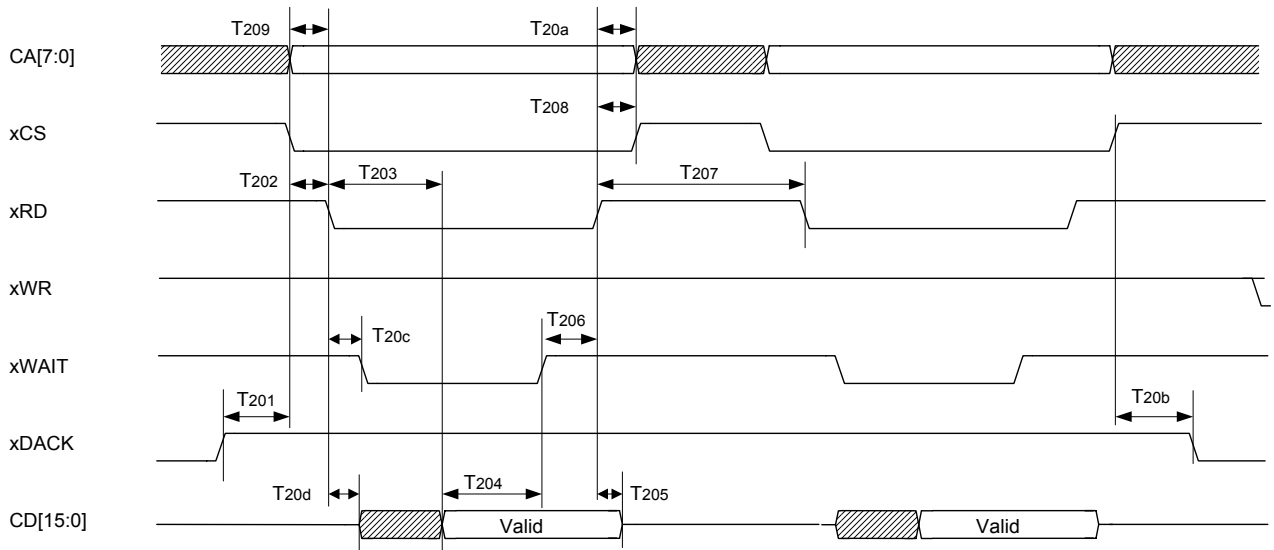
## 7.4.1.4 CLKIN (12MHz) Clock Input Timing



Symbol	Description	Min.	Typ.	Max.	Unit
F <sub>131</sub>	Clock input frequency	11.9988	12	12.0012	MHz
T <sub>132</sub>	Clock input HIGH level pulse width	28	—	52	ns
T <sub>133</sub>	Clock input LOW level pulse width	28	—	52	ns

## 7.4.2 CPU Interface Access Timing

### 7.4.2.1 Register Read Timing

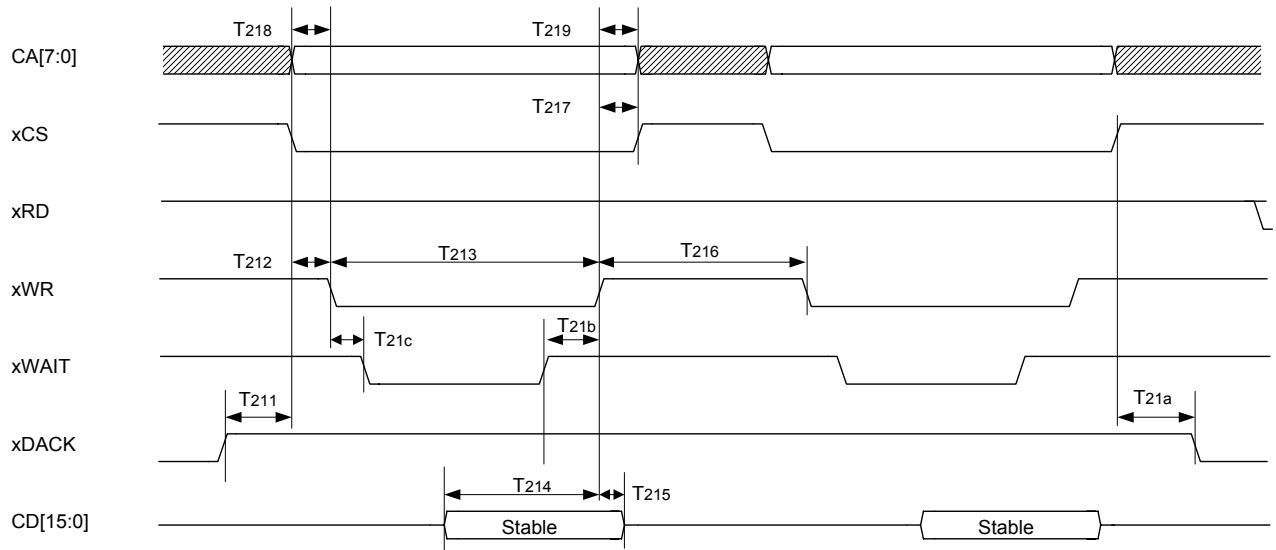


Symbol	Description	Min.	Typ.	Max.	Unit
T201	xCS assert time for xDACK negate	10	—	—	ns
T202	xRD assert time for xCS assert	0	—	—	ns
T203	CD output delay time (note 1) for xRD assert	42	—	62.5	ns
T204	xWAIT negate time for CD output	20	—	22	ns
T205	CD output hold time for xRD negate	2.5	—	18	ns
T206	xRD negate time for xWAIT negate	0	—	—	ns
T207	xRD negate period	42	—	—	ns
T208	xCS negate time for xRD negate	0	—	—	ns
T209	CA setup time for xRD assert	0	—	—	ns
T20a	CA hold time for xRD negate	0	—	—	ns
T20b	xDACK assert time for xCS negate	10	—	—	ns
T20c	xWAIT assert time for xRD assert	—	—	8	ns
T20d	CD bus valid delay time for xRD assert	—	—	8	ns

(Note 1)

This is a regulation during normal register access (except for access to FIFO forCPU register). During access to FIFO forCPU register, the time to data output is delayed depending on the state of access contention to internal FIFO memory.

## 7.4.2.2 Register Write Timing



Symbol	Description	Min.	Typ.	Max.	Unit
T211	xCS assert time for xDACK negate	10	—	—	ns
T212	xWR assert time for xCS assert	0	—	—	ns
T213	xWR assert pulse width	32	—	—	ns
T214	CD setup time for xWR negate	10	—	—	ns
T215	CD hold time for xWR negate	0	—	—	ns
T216	xWR negate period	42	—	—	ns
T217	xCS negate time for xWR negate	0	—	—	ns
T218	CA setup time for xWR assert	0	—	—	ns
T219	CA hold time for xWR negate	0	—	—	ns
T21a	xDACK assert time for xCS negate	10	—	—	ns
T21b	xWR negate time for xWAIT negate	0	—	—	ns
T21c	xWAIT assert time for xWR assert (Note 2)	—	—	8	ns

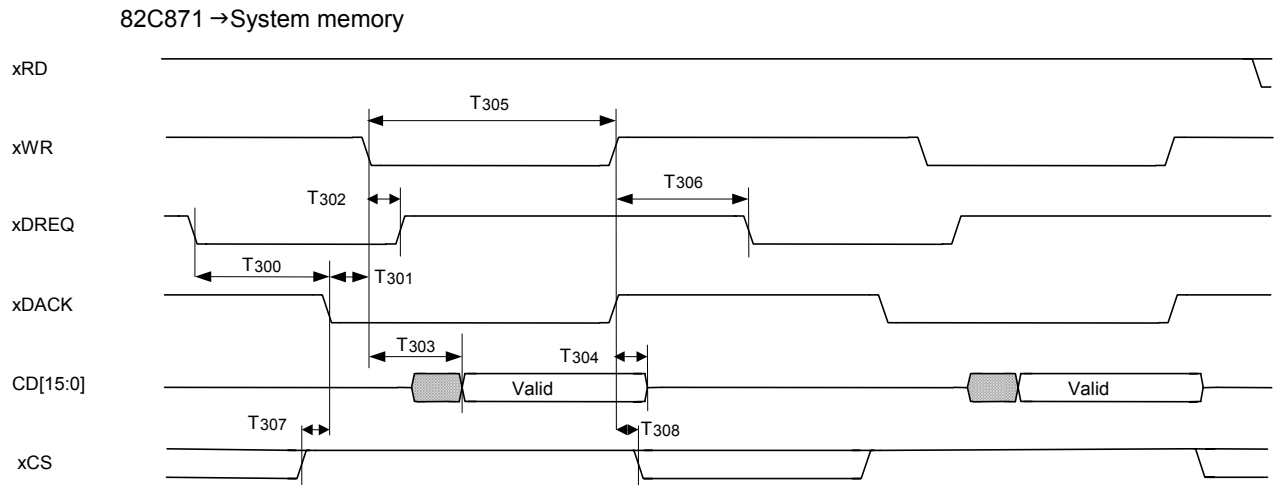
(Note 2)

xWAIT is not output for normal register access.

It may be output when there is successive access to FIFO for CPU register.

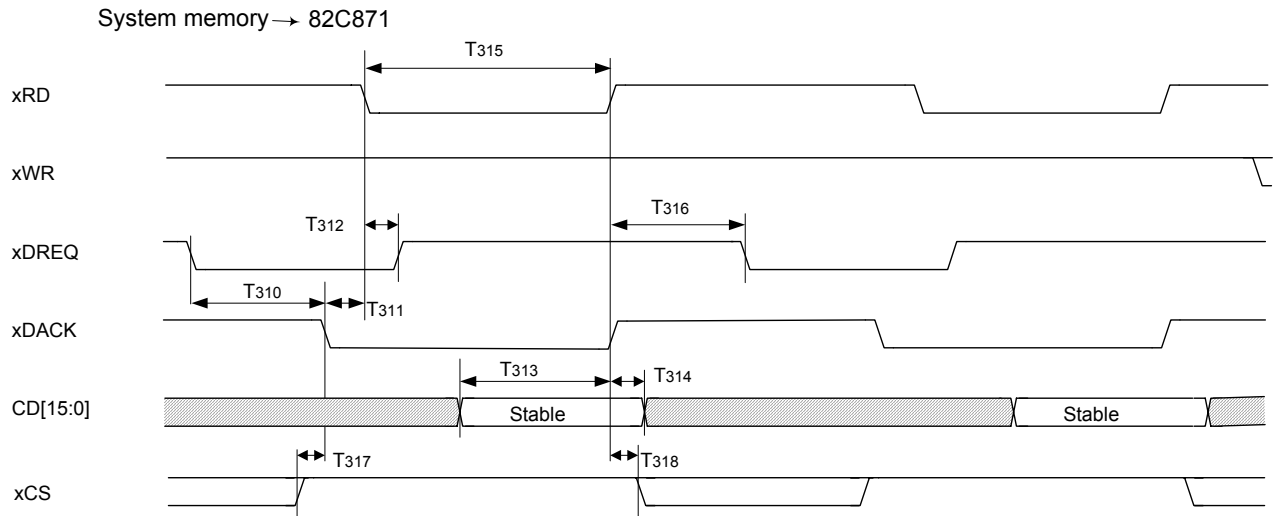
### 7.4.3 DMA Timing

#### 7.4.3.1 xRD/xWR Strobe Mode (DMAOUT)



Symbol	Description	Min.	Typ.	Max.	Unit
T300	xDACK assert time for xDREQ assert	0	—	—	ns
T301	xWR assert time for xDACK assert	0	—	—	ns
T302	xDREQ negate time for xWR assert	—	—	10	ns
T303	Data output delay time for xWR assert	—	—	8	ns
T304	Data hold time for xWR negate	2	—	—	ns
T305	xWR assert pulse width	42	—	—	ns
T306	xDREQ assert time for xWR negate	160	—	—	ns
T307	xDACK assert time for xCS negate	0	—	—	ns
T308	xCS assert time for xDACK negate	0	—	—	ns

7.4.3.2 xRD/xWR Strobe Mode (DMAIN)

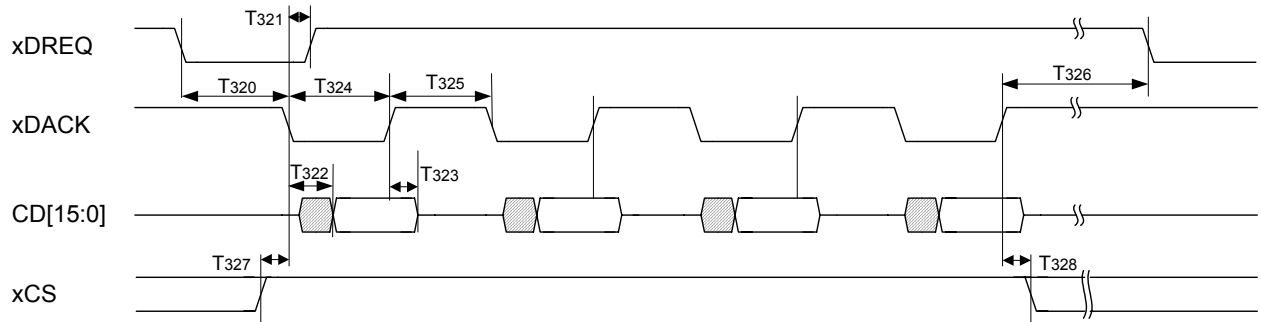


Symbol	Description	Min.	Typ.	Max.	Unit
T310	xDACK assert time for xDREQ assert	0	—	—	ns
T311	xRD assert time for xDACK assert	0	—	—	ns
T312	xDREQ negate time for xRD assert	—	—	10	ns
T313	Data setup time for xRD negate	10	—	—	ns
T314	Data hold time for xRD negate	0	—	—	ns
T315	xRD assert pulse width	42	—	—	ns
T316	xDREQ assert time for xRD negate	160	—	—	ns
T317	xDACK assert time for xCS negate	0	—	—	ns
T318	xCS assert time for xDACK negate	0	—	—	ns

## 7.4.3.3 DACK Strobe Mode (DMAOUT)

82C871 → System memory

BurstLength=4



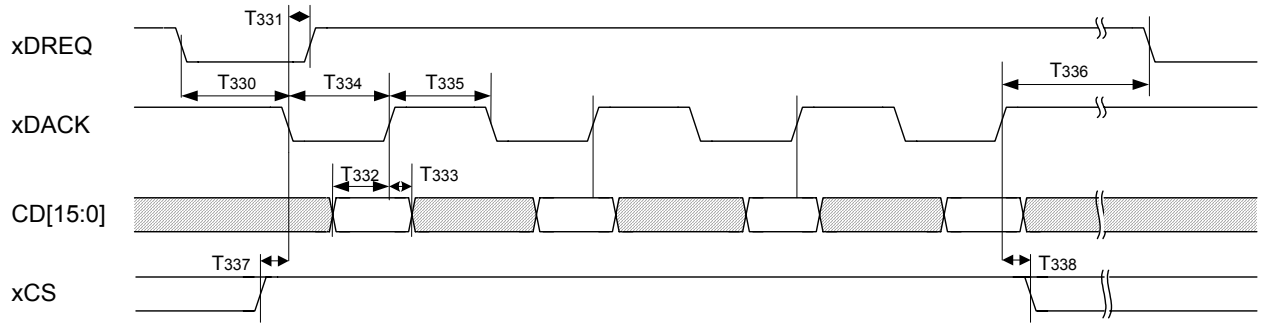
Symbol	Description	Min.	Typ.	Max.	Unit
T320	xDACK assert time for xDREQ assert	0	—	—	ns
T321	xDREQ negate time for xDACK assert	—	—	10	ns
T322	Data output delay time for xDACK assert	—	—	7	ns
T323	Data hold time for xDACK negate	2	—	—	ns
T324	xDACK assert pulse width	42	—	—	ns
T325	xDACK negate pulse width	42	—	—	ns
T326	xDREQ assert time for xDACK negate	160	—	—	ns
T327	xDACK assert time for xCS negate	0	—	—	ns
T328	xCS assert time for xDACK negate	0	—	—	ns



7.4.3.4 DACK Strobe Mode (DMAIN)

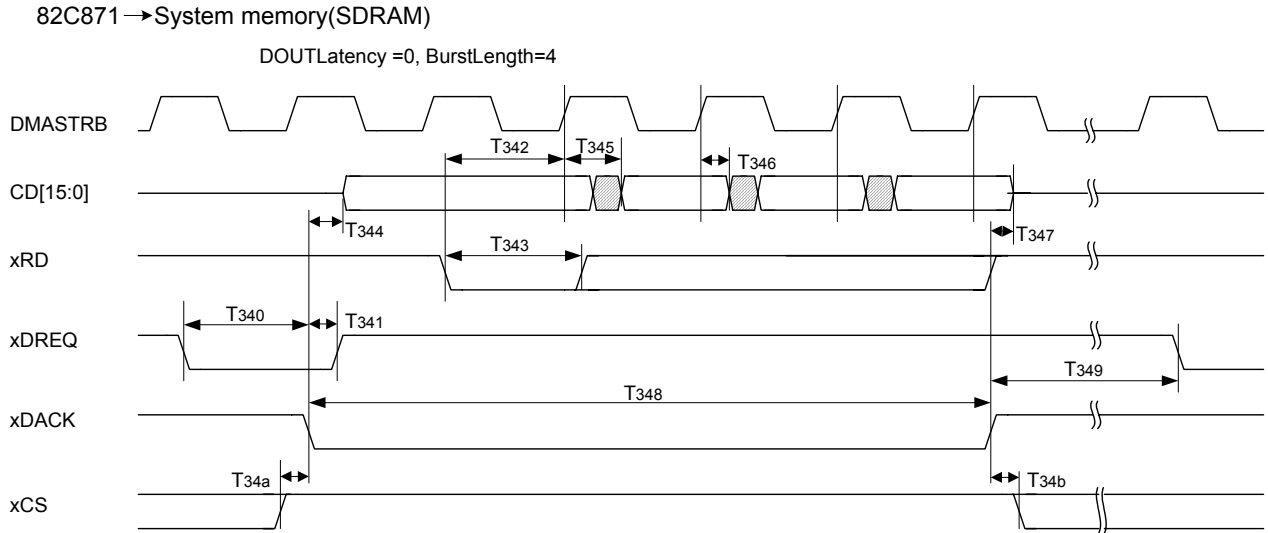
System memory → 82C871

BurstLength=4



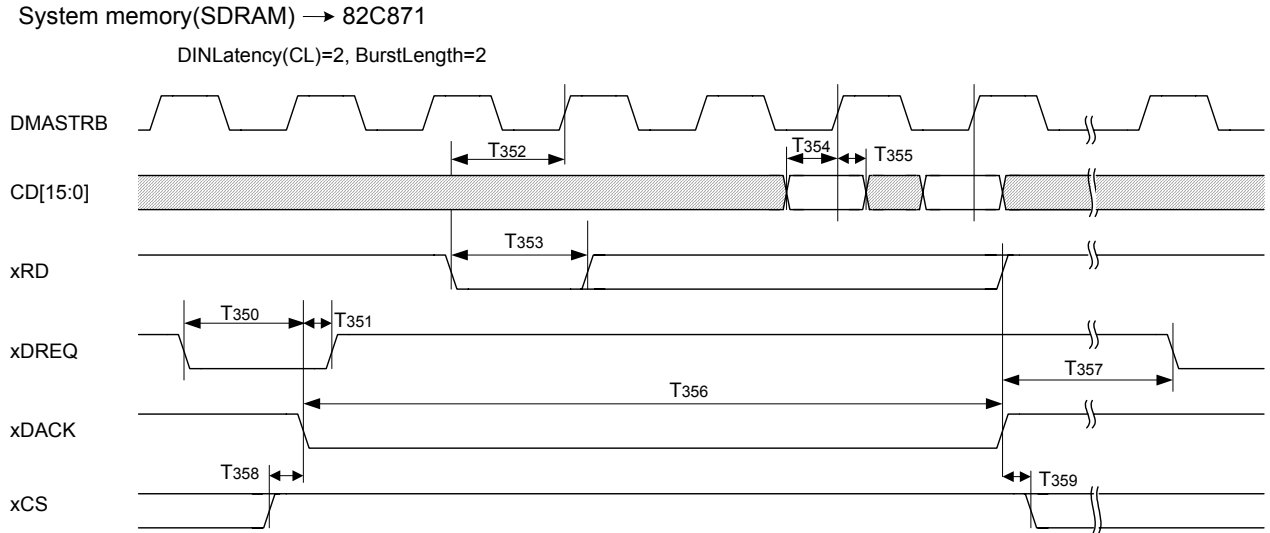
Symbol	Description	Min.	Typ.	Max.	Unit
T330	xDACK assert time for xDREQ assert	0	—	—	ns
T331	xDREQ negate time for xDACK assert	—	—	10	ns
T332	Data setup time for xDACK negate	10	—	—	ns
T333	Data hold time for xDACK negate	0	—	—	ns
T334	xDACK assert pulse width	42	—	—	ns
T335	xDACK negate pulse width	42	—	—	ns
T336	xDREQ assert time for xDACK negate	160	—	—	ns
T337	xDACK assert time for xCS negate	0	—	—	ns
T338	xCS assert time for xDACK negate	0	—	—	ns

7.4.3.5 DMASTRB SDRAM Mode (DMAOUT)



Symbol	Description	Min.	Typ.	Max.	Unit
T340	xDACK assert time for xDREQ assert	0	—	—	ns
T341	xDREQ negate time for xDACK assert	—	—	10	ns
T342	DMASTRB valid edge time for xRD (to CAS) assert	3	—	—	ns
T343	xRD (to CAS) assert pulse width	1T (DMASTRB)	—	—	ns
T344	Data output delay time for xDACK assert	—	—	7	ns
T345	Data output delay time for DMASTRB valid edge	—	—	9	ns
T346	Data hold time for DMASTRB valid edge	4	—	—	ns
T347	Data hold time for xDACK negate	2	—	—	ns
T348	xDACK assert pulse width	42	—	—	ns
T349	xDREQ assert time for xDACK negate	160	—	—	ns
T34a	xDACK assert time for xCS negate	0	—	—	ns
T34b	xCS assert time for xDACK negate	0	—	—	ns

7.4.3.6 DMASTRB SDRAM Mode (DMAIN)

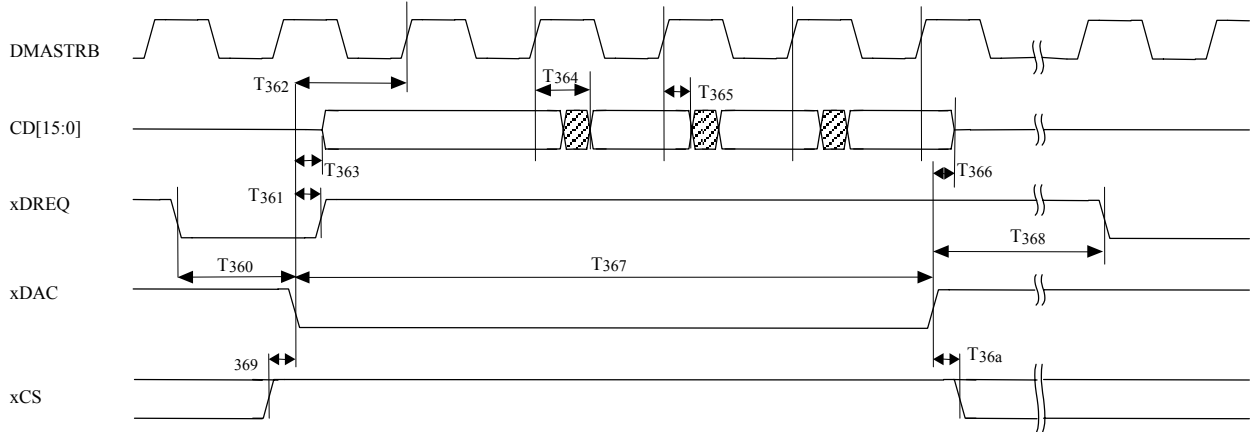


Symbol	Description	Min.	Typ.	Max.	Unit
T350	xDACK assert time for xDREQ assert	0	—	—	ns
T351	xDREQ negate time for xDACK assert	—	—	10	ns
T352	DMASTRB valid edge time for xRD (to CAS) assert	3	—	—	ns
T353	xRD (to CAS) assert pulse width	1T (DMASTRB)	—	—	ns
T354	Data setup time for DMASTRB valid edge	10	—	—	ns
T355	Data hold time for DMASTRB valid edge	0	—	—	ns
T356	xDACK assert pulse width	42	—	—	ns
T357	xDREQ assert time for xDACK negate	160	—	—	ns
T358	xDACK assert time for xCS negate	0	—	—	ns
T359	xCS assert time for xDACK negate	0	—	—	ns

7.4.3.7 DMASTRB General Mode (DMAOUT)

82C871 → Ssystem

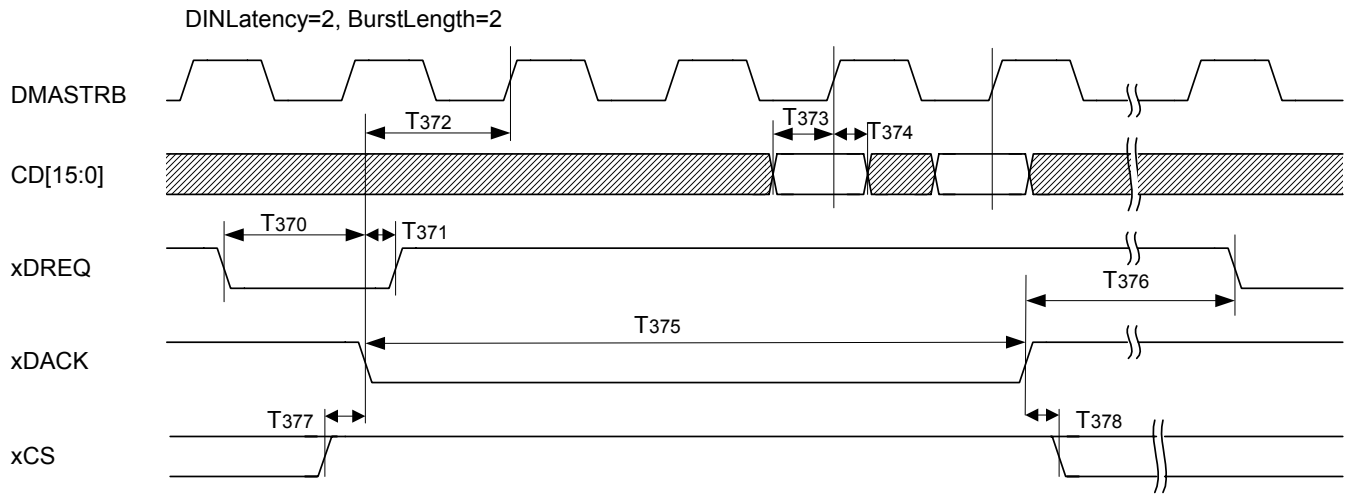
DOUTLatency=1, BurstLength=4



Symbol	Description	Min.	Typ.	Max.	Unit
T360	xDACK assert time for xDREQ assert	0	—	—	ns
T361	xDREQ negate time for xDACK assert	—	—	10	ns
T362	DMASTRB valid edge time for xDACK assert	3	—	—	ns
T363	Output data delay time for xDACK assert	—	—	7	ns
T364	Output data delay time for DMASTRB valid edge	—	—	9	ns
T365	Output data hold time for DMASTRB valid edge	4	—	—	ns
T366	Data hold time for xDACK negate	2	—	—	ns
T367	xDACK assert pulse width	42	—	—	ns
T368	xDREQ assert time for xDACK negate	160	—	—	ns
T369	xDACK assert time for xCS negate	0	—	—	ns
T36a	xCS assert time for xDACK negate	0	—	—	ns

7.4.3.8 DMASTRB General Mode (DMAIN)

System memory → 82C871



Symbol	Description	Min.	Typ.	Max.	Unit
T370	xDACK assert time for xDREQ assert	0	—	—	ns
T371	xDREQ negate time for xDACK assert	—	—	10	ns
T372	DMASTRB valid edge time for xDACK assert	3	—	—	ns
T373	Data setup time for DMASTRB valid edge	10	—	—	ns
T374	Data hold time for DMASTRB valid edge	0	—	—	ns
T375	xDACK assert pulse width	42	—	—	ns
T376	xDREQ assert time for T376xDACK negate	160	—	—	ns
T377	xDACK assert time for xCS negate	0	—	—	ns
T378	xCS assert time for xDACK negate	0	—	—	ns

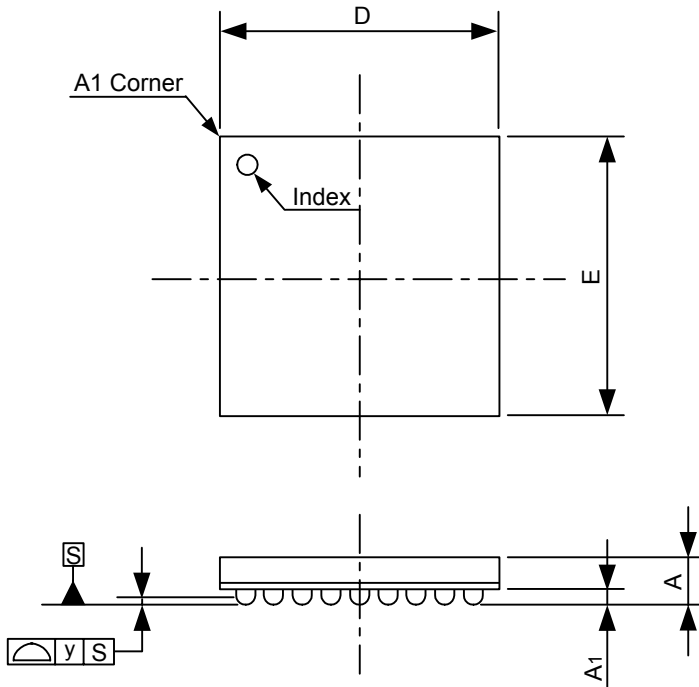
#### **7.4.4 USB Interface Timing**

The 82C871 conforms to USB 2.0 standard.

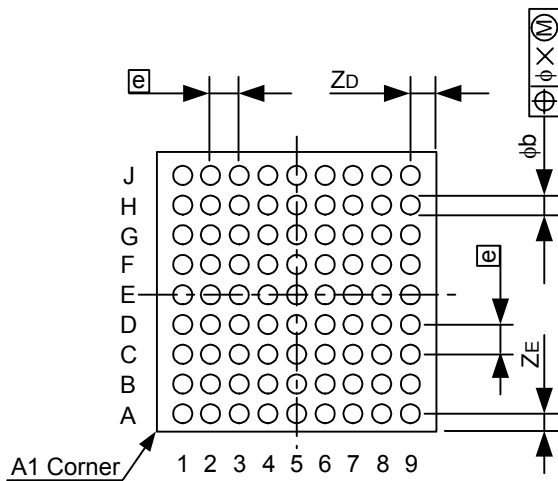
8 8. EXTERNAL DIMENSIONS DRAWING

8.1 8.1 CSP Package

Top View



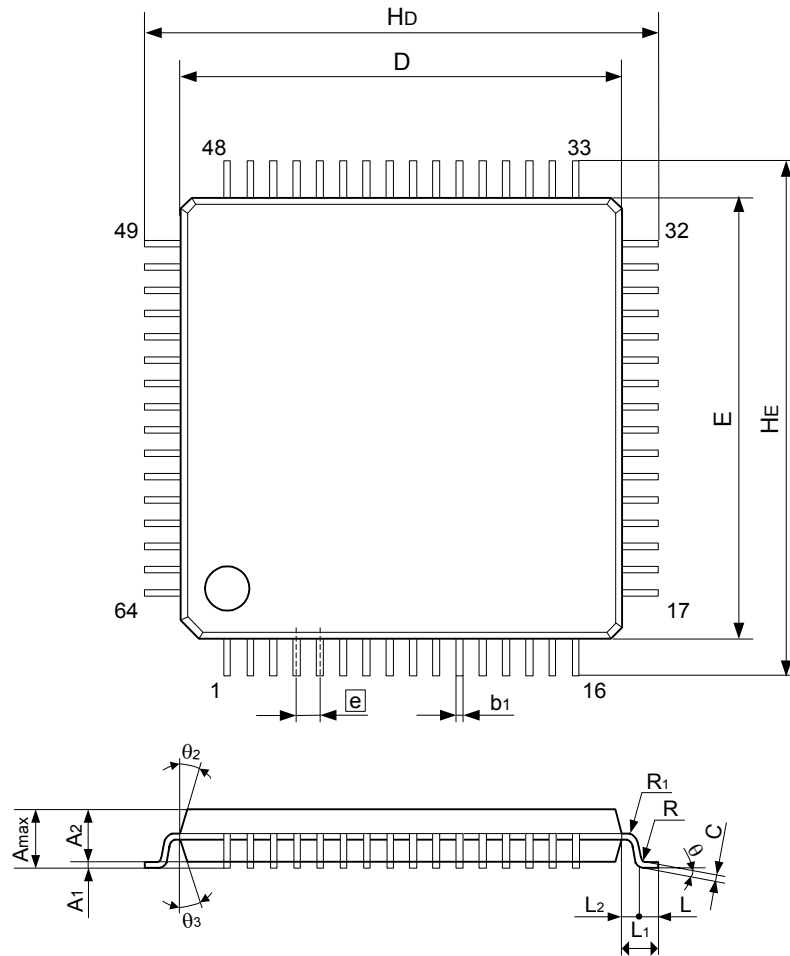
Bottom View



Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	7.80	8.0	8.2
E	7.80	8.0	8.2
A			1.20
A1	0.25	0.30	0.35
e		0.80	
b	0.38	0.43	0.48
X			0.08
Y			0.10
ZD		0.80	
ZE		0.80	

1 = 1mm

8.2 QFP Package



Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
E	9.9	10	10.1
D	9.9	10	10.1
Amax			1.7
A1		0.1	
A2	1.3	1.4	1.5
e		0.5	
b1	0.13	0.18	0.28
C1	0.1	0.125	0.175
$\theta$	0°		10°
L	0.3	0.5	0.7
L1		1	
L2		0.5	
HE	11.6	12	12.4
Hd	11.6	12	12.4
$\theta_2$		12°	
$\theta_3$		12°	
R		0.2	
R1		0.2	

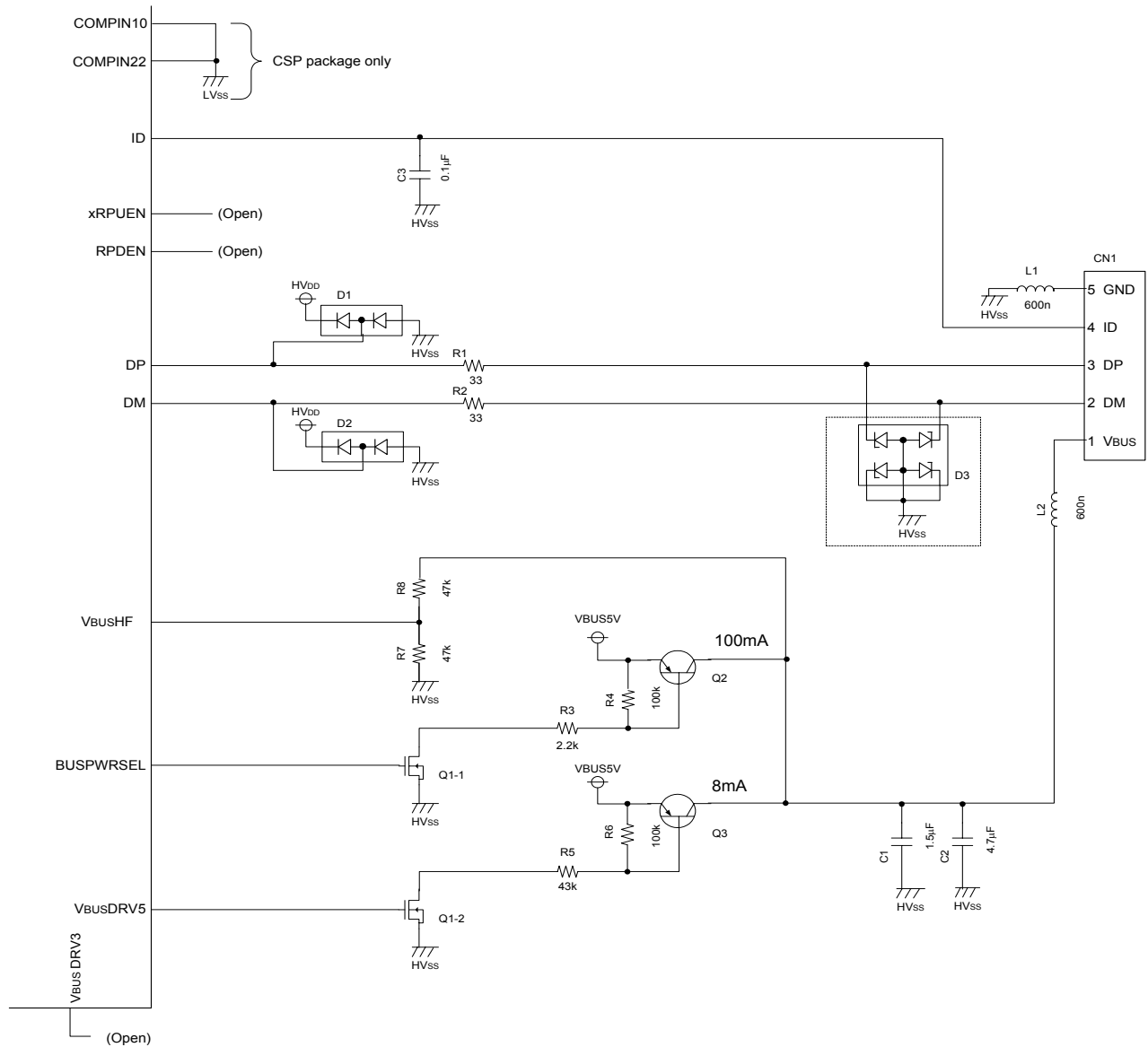


## 9 CONNECTION EXAMPLES

Above is the connection example (reference) for the external peripheral circuitry.

(Note) The connection example is for reference only. It does not guarantee operation in your product. Users should examine the details of the circuit structure and select parts.

### 9.1 OTG Interface Pin Connection (Example)



## (Note on connection)

- In order to protect the LSI from static electricity, set D1 and D2 diode protection circuits. Select the diodes according to their characteristics and ratings.
- For further protection from static electricity, use the D3 diode.
- Wire the DP and DM lines so that they are of the same length and are short.
- Do not wire other lines near or under the OTG Interface wiring.

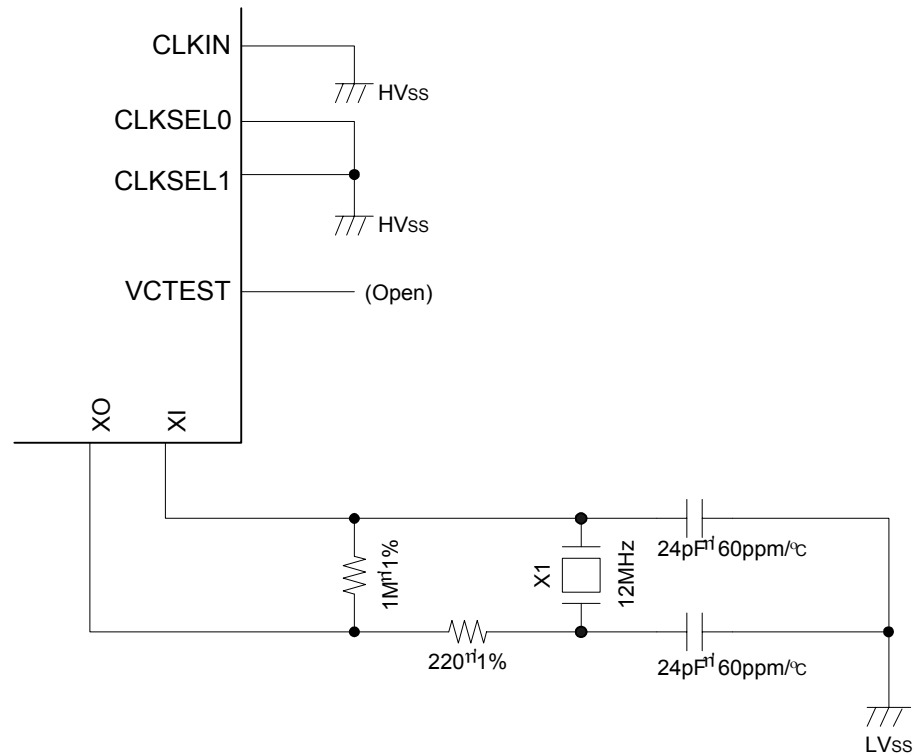
## Example of connection parts

(Note) The parts table is for reference only. It does not guarantee operation in your product. Users should select the individual parts carefully.

Section	Symbol	Parts name	Model number	Specification (rating)	Operating temperature (°C)	Manufacturer	Units
1	C1	Ceramic condenser	GRM31MR11C155ZC01	16V 1.5 $\mu$ F	-55 to +125	Murata Manufacturing	1
2	C2	Ceramic condenser	GRM31MF11C475ZA12B	16V 4.7 $\mu$ F	-25 to +85	Murata Manufacturing	1
3	C3	Ceramic condenser	GRM40F104Z50PT	0.1 $\mu$ F	-25 to +85	Murata Manufacturing	1
4	L1, L2	EMI Filter	BLM21PG600SN1	600nH	-55 to +125	Murata Manufacturing	2
5	R1, R2	Resistor	RK73H1JTD33F	33 $\Omega$	-55 to +125	KOA	2
6	R3	Resistor	RK73H1JTD2.2kD	2.2k $\Omega$	-55 to +125	KOA	1
7	R4, R6	Resistor	RK73H1JTD100kD	100k $\Omega$	-55 to +125	KOA	2
8	R5	Resistor	RK73H1JTD43kD	43k $\Omega$	-55 to +125	KOA	1
9	R7, R8	Resistor	RK73H2BTD47kF	47k $\Omega$	-55 to +125	KOA	2
10	Q1	FET	TPCS8205		-55 to +150	Toshiba	1
11	Q2, Q3	Transistor	2SA1121	PNP	-55 to +125	Toshiba	2
12	D1, D2	Diode	1SS396		-40 to +100	Toshiba	2
13	D3	Diode	NNCD5.6LG		-40 to +100	NEC	1
14	CN1	USBReceptacle	MNE20	USB miniAB	—	ACON	1

## 9.2 Clock Pin Connection (Example)

<When using crystal oscillator>

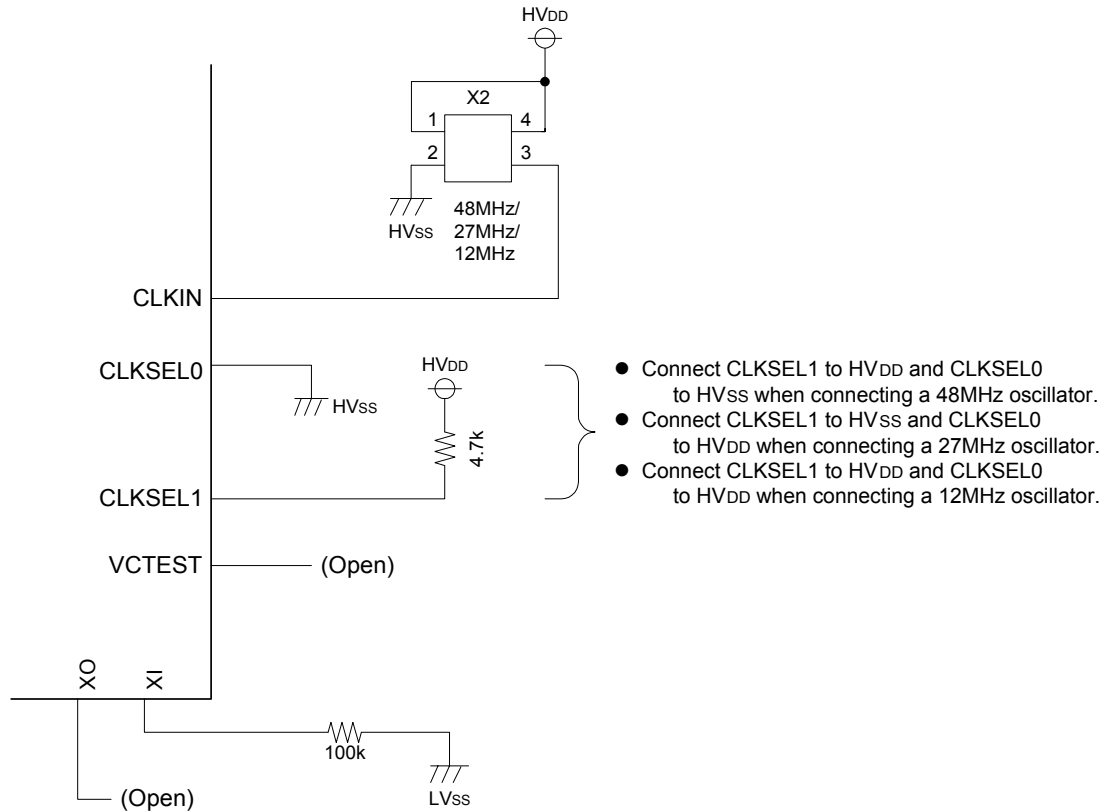


X1\*: 12MHz 10pF 30ppm

(Note on connection)

- Do not wire other lines near or under the clock wiring.
- For XI and XO circuits and ratings, refer to connection example for crystal oscillator X1.
- Wire the XI and XO circuits using minimum length of wires.
- Make sure that a disused pattern is not connected to the VCTEST pin.

<When using crystal oscillator (external clock input)>



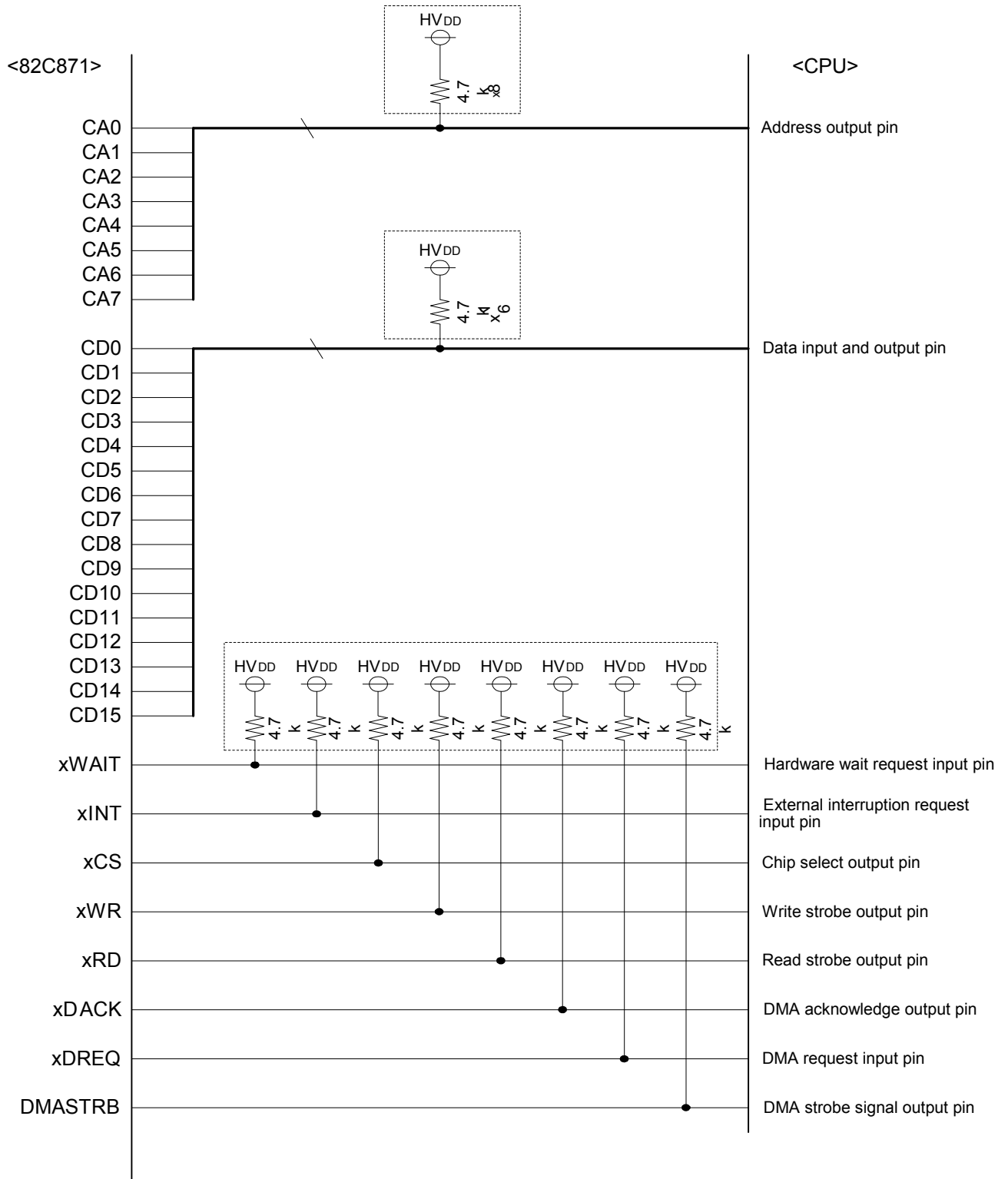
X2\*: 48MHz±50ppm

Crystal oscillator of center frequency of ±50ppm or lower is recommended.  
The PLL device is not recommended due to its high amount of jitter.

(Note on connection)

- Do not wire other lines near or under the clock wiring.
- For CLKIN circuit, refer to connection example for crystal oscillator X2.
- Wire the CLKIN circuit using minimum length of wires.
- Follow the HV<sub>I</sub> input voltage standard value of the operation requirement for the CLKIN input voltage.
- Make the XI wiring as short as possible.
- Make the XO wiring as short as possible, and leave it open.
- Make sure that a disused pattern is not connected to the VCTEST pin.

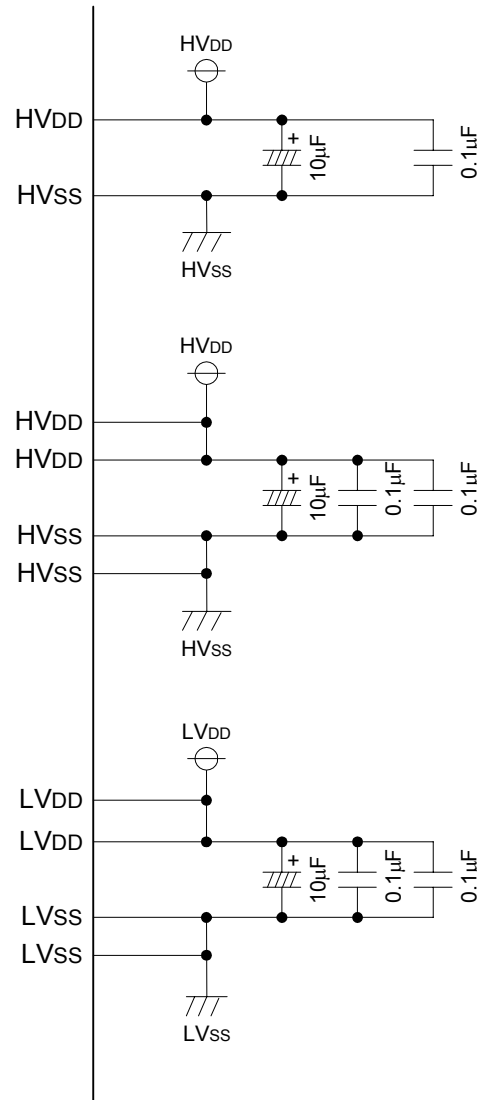
9.3 CPU Interface Pin Connection (Example)



(Note on connection)

- Use the pull up resistor if it is necessary in your system.
- When the 82C871's DMASTRB pin is not used, connect this pin to HVss.

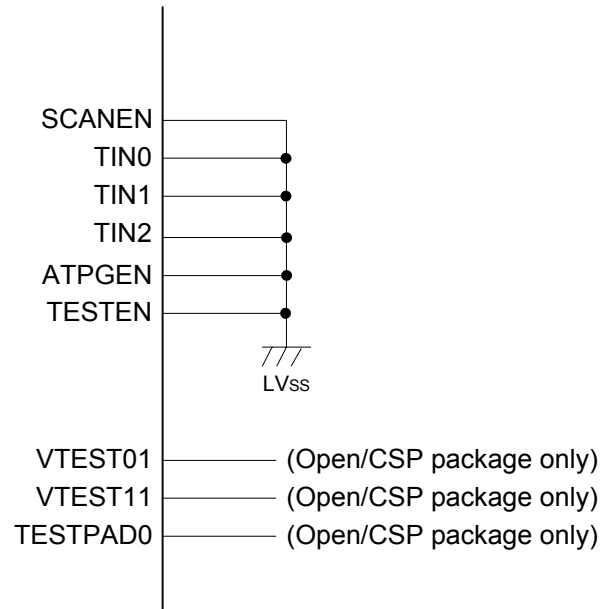
#### 9.4 Power Supply and Ground Pin Connection (Example)



#### (Caution on connection)

- Use a common grounding for the HV<sub>SS</sub> and the UV<sub>SS</sub>. Also, use the common grounding for the CPU's I/O grounding.
- Connect an exclusive condenser (see the top diagram) for the HV<sub>DD</sub> (CSP: G3, QFP: 20-pin) and HV<sub>SS</sub> (CSP: H5, QFP: 23-pin) placed on the USB I/O.

## 9.5 Test Pin Connection (Example)







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