Panasonic®

CMOS Digital IC
CMOS Logic
MN4000B

CMOS Logic MN4000B Series

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PREFACE

The CMOS logic IC MN4000B series data book has been published to meet consummer needs as the revised edition of the current MN4000B series by expanding the range and adding rew products. The MN4000B series are general purpose CMOS devices which provide various functions and find applications in both consumer and industrial fields.

General purpose CMOS LOGICS have features such as low power dissipation, single power supply, wide operation range of power supply, high noise immunity and high integration, all of which are superior to conventional DTL, TTL and LS-TTL.

The increase of CMOS suppliers in recent years resulted in the necessity for compatibility with respect to electric characteristics and functions. We have begun to market the MN4000B series for the general purpose CMOS LOGICS stipulated by IEC/JEDED. We hope you will make use of these devices as well as other Matsushita semiconductors.

July, 1984

Matsushita Electronics Corporation

Semiconductor Division

The application circuits in this book have been chosen as examples of the characteristics and performance of our products. The information contained herein is believed to be reliable. However, no responsibility is assumed for any consequence of its use, nor for patent liability with respect to the use of the information.
The device specifications are subject to change without prior notice.

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Index Table

Selection Guide by Function

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Explanation

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Explanation

1. General descriptions of MN4000B series data

The MN4000B series are fully buffered digital ICs which meet IEC/JEDEC stipulations. The MN4000B series are designed for pin compatibility with CMOS4000 and 4500 which are used over a wide range.

The MN4000B series make system designing simple beause output characteristics are standardized.

CMOS features

- Low power dissipation: 10 nW typ./gate (static)
- Wide range of operating voltage: +3V ~ 15V
- Wide range of operating temperature: −40 ~ +85°C
- High DC − fanout: 50 typ.
- All series include the output buffer (capable of driving 1 LS-TTL)
- Protection circuit for static voltage to input and output
- High speed (higher than conventional CMOS4000B)
- High integration
- High noise immunity

2. CMOS Basic circuit • Cross-sectional view

As a representative of the MN4000B series, basic conceptions of the inverter are described below.

The CMOS inverter is constructed with a MOS P-channel transistor (P_1) and N-channel transistor (N_1) of the enhancement type; the connecting gates are for input and the connecting drains are for output (illustrated in Fig. 1). The source of the P-channel MOS transistor is connected to V_{DD} (+) and that of the N-channel MOS transistor is connected to V_{SS} (−).

Let us consider the output voltage (V_O) if the input voltage (V_I) changes between V_{SS} and V_{DD}.

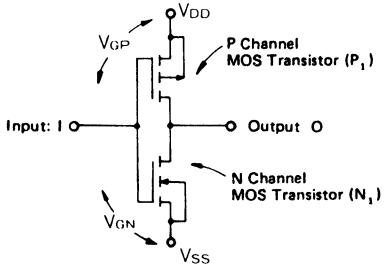


Fig. 1 CMOS Inverter

2.1 If input is V_{SS} level

P_1 switches on because the V_{GP} of P_1 (gate-source voltage) is deep negative bias. N_1 switches off because the V_{GN} of N_1 (gate-source voltage) is zero.

Though the output voltage is determined by the ratio of P_1 and N_2 resistance, it almost becomes V_{DD} due to some kΩ for the ON-side transistor and hundreds of MΩ for the OFF-side transistor. Less current flows between V_{DD} and V_{SS}.

2.2 For intermediate voltage between V_{SS} and V_{DD}. V_{DD}

The output (0) is a medium level divided by both P_1 and N_1 ON resistor values. In this case, the output level goes nearly to V_{DD} when the input voltage (V_I) is around V_{SS}, and it comes down to V_{SS} when around V_{DD}. Current flows between V_{DD} ~ V_{SS}.

2.3 If input is V_{DD} level

P_1 switches off because the V_{GP} of P_1 is zero and P_2 switches on because the V_{GN} is V_{DD} ~ V_{SS}. This is a counter-action of 2.1 and the output (0) voltage is almost V_{SS}.

Less current flows between V_{DD} and V_{SS}. Fig. 2 shows that current flows only at the transient time shown by the dotted line when the state of the inverter changes where the horizontal axis represents the input voltage and the vertical axis represents the output voltage.

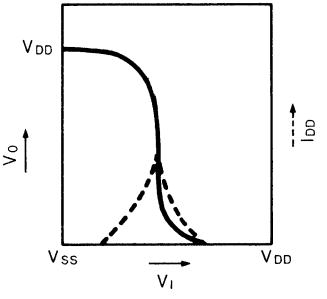


Fig. 2 Inverter Input/Output Voltage Characteristics

Fig.3 shows the cross-sectional view of the CMOS inverter. The P-N junction is used for isolation between P-channel and N-channel MOS transistors to make the CMOS inverter on a single silicon substrate.

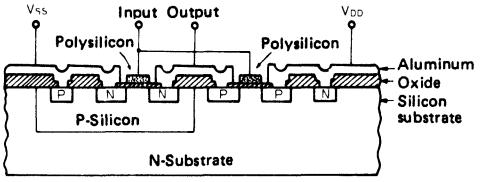
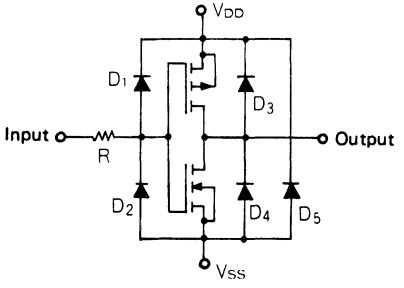


Fig. 3 CMOS Inverter Cross-Sectional View

Fig. 3 shows the views to make an N-channel MOS transistor in a P-well region after making it on an N-type silicon substrate.

Because the N-type substate is connected to V_{DD} and the P-well to V_{SS}, each P-channel and N-channel transistor can be operated electrically independent due to reverse biases when the power is applied. This construction of the CMOS circuit form the parasitic diode shown in Fig. 4. It is important to use with in the maximum rating because exceeding the forward current of the diode may damage the IC.



R : Input Protection Resistor
D_1 : Input Protection Diode
D_2 : Input Protection Diode
D_3 : P-channel Transistor Parasitic Diode by Forming Drain
D_4 : N-channel Transistor Parasitic Diode by Forming Drain
D_5 : Parasitic Diode by Forming P-well

Fig. 4 Equivalent circuit of CMOS Inverter with Parasitic Element

Input protection diodes D_1 and D_2 in the equivalent circuit are to protect CMOS inputs against static electrical damage; these are included in all MN4000B series.

3. Designing notes

CMOS logic which has an integration as large as SSI or MSI finds applications in an extensive area. There are specific circuits such as bidirectional analog switches in CMOS technology and many LSIs developed due to small chip size and high integration.

Table 1 Characteristic Comparison Between TTL and CMOS

Item	Normal TTL	LS-TTL	CMOS 4000		
			5V	10V	15V
Transfer Time (C_L = 15pF)	10 ns	10 ns	40 ns	20 ns	15 ns
Flip-Flop Clock Frequency	35 MHz	45MHz	8 MHz	16 MHz	20 MHz
Quiescent Power	10 mW	2 mW	10 nW	10 nW	10 nW
Noise Immunity	1V	0.8V	2.25V	4.5V	6.75V
Fan-out	10	10	50	50	50

3.1 Supply Voltage Range

CMOS logic of MN4000B series is guaranteed to function ranging from 3V to 15V. It is not guaranteed under 3V because of the increase of propagation delay time (decrease of speed), the increase of output impedance and the loss of noise immunity. It is also not guaranteed over 15V becuse of the increase of dynamic power dissipation, the spike noise exceeding tolerable voltages and other causes which may cause the latch-up and result in damage to the device unless the current is restricted to minimum. Please refrain from using at over 15V.

The level conversion between TTL and CMOS which have different supply voltages can be realized by using the MN4049B or MN4050B.

3.2 Output with Buffer

The MN4000B series have fully buffered output in order to shorten the propagation delay time and to standardize the propagation delay time and characteristics of output driving (Fig. 5). Buffered outputs increase the voltage gain, the static noise immunity and can improve the dynamic noise margin because they have ideal transfer characteristics and low impedance at the output (Fig. 6). The high gain also provides good pulse shaping due to less effect of the input rise or fall time. (Fig. 7 (a) (b).

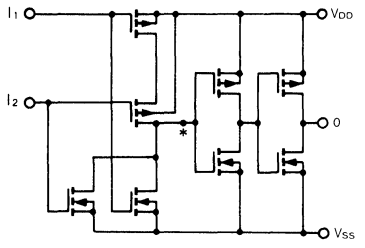


Fig. 5 Typical 2 Input NOR Gate Incorporating Buffer Output Circuit
(*Output for the types without buffer)

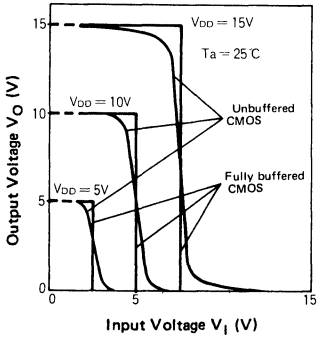


Fig. 6 Transfer Characteristics
Buffered CMOS shows better transfer characteristic.

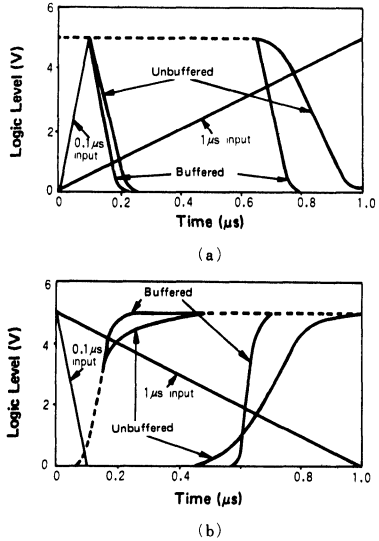


Fig. 7 Output Transfer Characteristics Not Affected by Rise (a) and Fall (b) of Input

3.3 Power Consumption

The CMOS is an ideal logic circuit for battery operation because the power consumption in the static state is very low and its operation ranges are very wide.

In the static state, only leakage currents flow through the V_{DD} to V_{SS} because the P-channel transistors are not ON simultaneously. The leakage currents are 0.5nA for each gate and the power consumptions are only 2.5nW (5V operation).

It is estimated that more energy is consumed to charge or discharge capacitances (on-ship parasitic capacitances and load capacitances) when the input data or input clock changes during CMOS operations. Actually there is a time when both P-channel and N-channel transistors are ON simultaneously. The dynamic power consumption P_{DYN} may increase proportionally to the product by the factors of the input clock frequency, loading capacitance (C_L) and the square of supply voltage (V_{DD}). (Refer to formula (1).)

$$P_{DYN} = f \cdot C_L \cdot V_{DD}^2 \quad \ldots\ldots\ldots (1)$$

The power consumption of CMOS gate is higher than that of LS-TTL in the range from 500 kHz to 2 MHz shown in Fig. 8. However, it is not so much higher for high-integrated CMOS ICs (MSI). The gates switched actually are so few that the power consumption does not increase because most gates are driven at lower clock frequency. It is necessary to analyse or consider the switching speeds of each gate in the circuit when you are to compare the power consumption of the logic devices which have various kinds of process technology. The maximum of static currents (I_{DD}) is limited in the general or individual specifications. Total power consumption mean the sum during both static and dynamic operations.

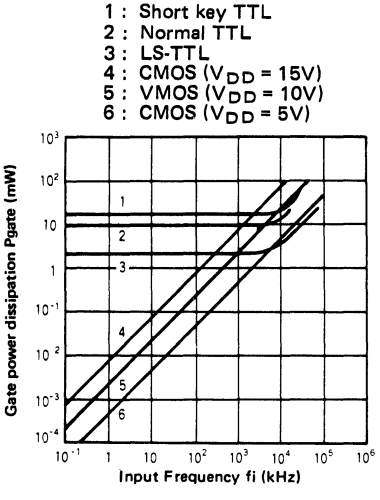


Fig. 8 Power Dissipation per gate – Input Frequency

3.4 Static power consumption

There are no drain currents because one input transistor is always OFF when the input voltages of CMOS logic IC are lower than the threshold voltage (V_T) of a N-channel transistor or higher than the difference between the supply voltage and the threshold voltage ($V_{DD} - V_T$) of a P-channel transistor. The drain currents flow because the N-channel transistor is ON when the input voltage is about the threshold voltage (1.5V typ.) of an N-channel transistor.

Fig. 9 shows the drain currents as a function of CMOS logic input voltage. The drain currents reach maximum value at 1/2 V_{DD}, and peak depends upon the squareness of the transistor use. The currents increase in proportion to V_{DD}^{n} if $n > 2$.

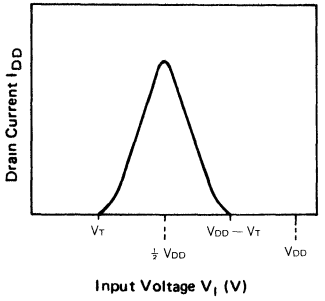


Fig. 9 Drain Current — Input Voltage

3.5 Propagation Delay Time (Transfer Time)

Compared to the TTL and LS-TTL, all CMOS devices are slow and very sensitive to capacitive loading (Fig. 10).

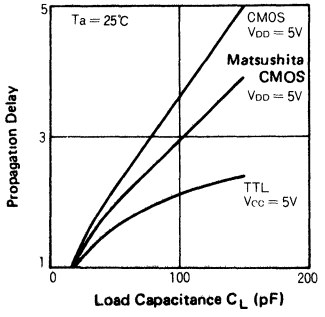


Fig. 10 Propagation Delay — Loading Capacitance (TTL, Other CMOS, Matsushita CMOS)

The MN4000B series use both Matsushita's original Processing and improved circuit design to achieve propagation delays and output rise time that are superior to any other junction-isolated CMOS device.

Matsushita's original processing achieves lower parastic capacitances, which reduce the on-chip delay and increase the maximum clock frequency of flipflops, registers and counters. Buffering all outputs even on gates results in lower output impedance and thus reduces the effect of capacitive loading.

You should pay attention to design the system that the speed is important since propagation delay is affected by three parameters: capacitive loading, supply voltage, and temperature.

3.6 Capacitive Loading Effect

A TTL with an output impedance 25Ω typ. in the low state is little affected by an increase in capacitive loading. A CMOS, however, with an output impedance of 250Ω typ. (5V operation), is 10 times more sensitive to capacitive loading. Fig. 11 shows the propagation delay time of the MN4011B as a function of load capacitance. Fig. 12 also shows the positive and negative-going delays as a function of load capacitance. It is limited in detail in general and individual specifications. The output with unbuffered gates has a higher output impedance and is more sensitive to capacitive loading.

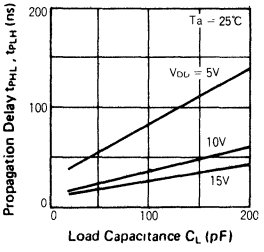


Fig. 11 Propagation Delay — Loading Capacitance

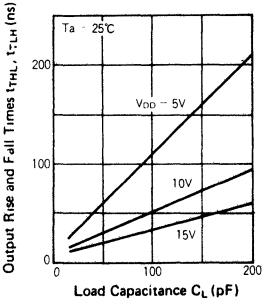


Fig. 12 Output Rise and Fall Times — Loading Capacitance (output transient times)

3.7 Supply Voltage Effect

3.7.1 Speed

Fig. 13 shows propagation delay as a function of supply voltage. The best choice for slow applications is 5V. For reasonably fast systems, choose 10 or 12V. Any application requiring 15V to achieve less delays and fast operation should be weighed against an LS-TTL approach.

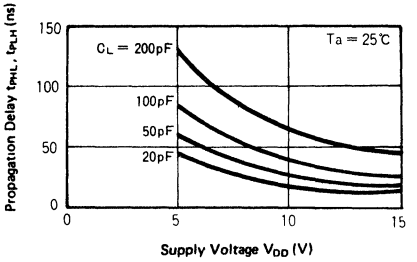


Fig. 13 Propagation Delay Versus Supply Voltage of MN4011B

3.7.2 Noise Immunity

The noise immunity is improved according to the increase of supply voltage.

3.8 Temperature Effect

The temperature dependence of the CMOS is much less than for the TTL. For the TTL there are three factors: increase of β with temperature, increase of resistor value with temperature and decrease of junction forward voltage drop with increasing temperature. For the CMOS, essentially only the carrier mobility changes, thus increasing the impedance and the delay with temperature. Please refer to the common and individual specifications in detail.

Fig. 14 shows propagation delay of the MN4011B as a function of ambient temperature.

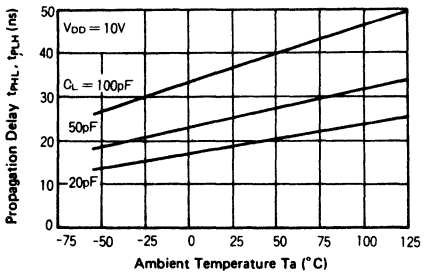


Fig. 14 Propagation Delay Versus Ambient Temperature at V_{DD} = 10V of MN4011B

3.9 Noise immunity

One of the most advertised and also misunderstood CMOS features is noise immunity. The input threshold of a CMOS gate is approximately 50% of the supply voltage and the voltage transfer curve is almost ideal. As a result, the CMOS can claim very good voltage noise immunity. Its typical values are 2.25V in a 5V system, 4.5V in a 10V system and 6.75V in a 15V system.

Fig. 15 shows the transfer comparison with the TTL. This implies the 1V noise immunity in a lightly loaded system and only 0.4V in the worst case. Fig. 16 shows the transfer characteristics at ambient temperatures ranging from −55°C to +125°C.

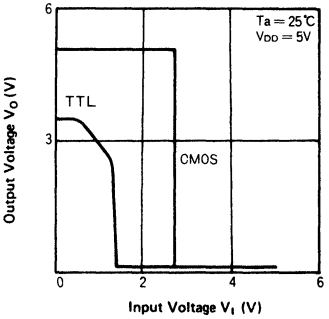


Fig. 15 Standard Transfer Characteristics of TTL and CMOS

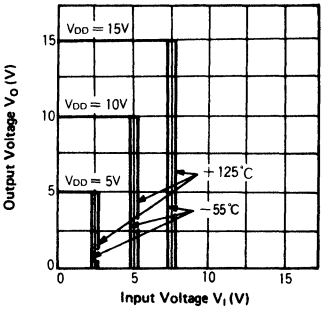


Fig. 16 Voltage Transfer Characteristics at Ta = −55°C to +125°C

Since the CMOS output impedance, output voltage and input threshold voltage are symmetrical with respect to the supply voltage, the Low and High level noise immunity are practically equal. Therefore, a CMOS system can tolerate ground or V_{DD} drops and noise on these supply lines of more than 1V, even in a 5V system. Moreover, the inherent CMOS delays act as a noise filter; 10ns spikes tend to disappear in a chain of CMOS gates, but are amplified in a chain of TTL gates. Because of these features, the CMOS is very popular with designers of industrial control equipment that must operate in an electrically and electromagnetically "polluted" environment.

The output impedance of the CMOS is 3 to 10 times higher than that of the TTL. CMOS interconnections are less stiff and much more susceptible to capacitively coupled noise. In terms of such current injected crosstalk from high noise voltages through small coupling capacitances, Table 2 shows a comparison of the CMOS with the TTL. It is apparent that the dynamic noise immunity of the CMOS at 10V operation is almost equal to the TTL and is 3 times higher than that of the LS-TTL.

The CMOS is less affected by noise immunity due to ideal transfer characteristics and comparatively slow speeds, but the TTL/LS-TTL is 5 times more sensitive to noise immunity than the CMOS.

Table 2 Dynamic Noise Immunity for CMOS, TTL and LS-TTL

V_{DD}	5V	10V	15V
CMOS/TTL	0.5	1	2
CMOS/LS-TTL	1	3	5

3.10 Input Protection

The gate input to any MOS transistor appears like a small (< 1pF) very low leakage (< 10^{-12}A) capacitor which is isolated from the substrate by an about 1000A thick SiO_2. Without special precautions, these inputs could be electrically charged to a high voltage, causing a destructive breakdown of the dielectric and permanently damaging the device. Therefore, all CMOS inputs are protected by a combination of series resistor and shunt diodes. Various manufacturers have used different approaches; some use a single diode, others use two diodes, and some use a resistor with a parasitic substrate diode.

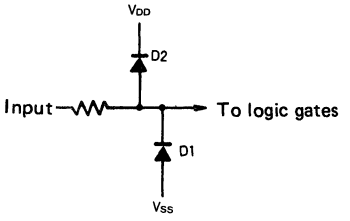


Fig. 17 Standard Input Protection Circuit of MN4000B series

Except for some devices, the MN4000B series utilize a series resistor, nominally 400 to 500Ω, and two diodes, one to V_{DD}, and another to V_{SS}. The resistor is a polysilicon true resistor without a parasitic substrate diode. This ensures that the input impedance is always over 400Ω under all biasing conditions. The diode (D_1) is connected to V_{SS} in parallel, and exhibits typical forward voltage drops of 0.9V at 1mA and reverse breakdown of 20V. For certain special applications such as oscillators, the diodes actually conduct during normal operation. In this case, the input currents might be limited to under 1mA. Currents over 10mA might damage the device.

Fig. 18 shows the input protection circuit of the MN4049B and MN4050B. The diode (D_1) is a drain against V_{SS} of the protection device.

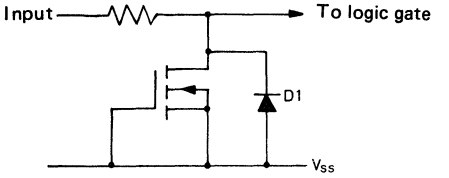


Fig. 18 Input Protection Circuit of MN4049B and MN4050B

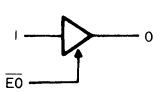
3.11 Power Supply Regulation and Decoupling

Since the CMOS has a wide operation range of 3V to 15V, it is considered that there is no need to regulate the power supply. However, the supply voltage strongly affects the system speed, noise immunity and power dissipation, so please refer to another text with respect to this value. There are some cases when voltage spikes generated by other systems override on the power line. These spikes affect noise immunity and damage the circuit at worst or adversely affect operation. It is necessary to connect a decoupling capacitance on the power line. A few μF of electrolytic capacitance per ten devices is generally adequate. But careful attention should be paid in special cases.
cases.

- **MN4511B:** BCD-7 segment Latch/Decoder/Driver; Connecting 3μF electrolytic capacitance to each device, it is necessary to avoid abnormal voltage spikes due to high di/dt.
- **MN4528B:** Trigger/Resettable Dual Monostable multivibrator; an appropriate decoupling capacitance should be used for this kind of circuit.
- The supply voltage of min. 4V is required for the circuit of Liner operation like RC or Xtal oscillator.

3.12 Tristate Output

In the case of the control input (EO) High, outputs are enabled and both P_4 and N_4 transistors function as a transmission gate, and connect two gates of output transistors. In the case of the control input (EO) Low, outputs are high impedance state (OFF) and P_3 transistors are pull-up, N_3 transistors pull-down respectively. (Refer to Fig. 19, Fig. 20)



Input		Output
I	$\overline{EO}$	O
X	L	Z
L	H	L
H	H	H

Z: High impedance
X: Don't care

Fig. 19 Tristate Logic Symbol and Truth Table

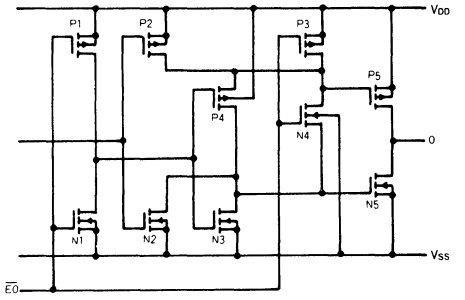


Fig. 20 Tristate Output Circuit

3.13 Latch Up

There is a latch-up phenomenon in the CMOS as the specific problem. The latch-up is (thyristor) phenomenon which comes from the parastics PNP and NPN transistors which are physical contruction of CMOS though it does not occur within maximum rating. This phenomenon results in much current between V_{DD} ~ V_{SS} with ON state of parasitics thyristor because input or output currents abnormally reverse if there are unexpected surges exceeding maximum rating, ripples of power supply, noises and some differences of the rising time when the IC is operated by two power supplies. While this phenomenon is positive feedback, it cannot be avoided unless the power is turned off or the current is limited under an appropriate value.

If the latch-up occurs when the set is operating, it possively aires the set crucial damage after damaging the IC in the worst case.

It is accordingly necessary to give sufficient consideration to not causing the latch-up during set design. It is necessary to design so as not to cause a forward current through the input protection diode or output parasitic diode which become the trigger of latch-up when the input voltage is higher than V_{DD} or lower than V_{SS}. or lower than V_{SS}.

We intend to design so as not to cause the latch-up by considering the β of the parasitic transistor and the depth of a diffusion. We assure that there are no problems in normal usage, according to evaluations of the level which occurs the latch-up shown in Fig. 21.

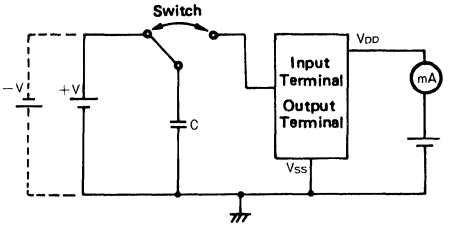


Fig. 21 Measurement of Latch-up

Let us explain in general how to protect against, the latch-up.

A. Insert the capacitor (0.1μ ~ 10μF) between V_{DD} ~ V_{SS}.

B. Limit the charging current to less than 10mA inserting dumper registers into shunt diodes if the load capacitor is large, though it is desiable to be under 1000pF. (Fig. 22)

C. It is recommended not to apply the input signal prior to V_{DD}; otherwise insert dumper resistors to the input.

D. Insert an appropiate value of resistors in series with to input in order to be under 10mA for the input current.

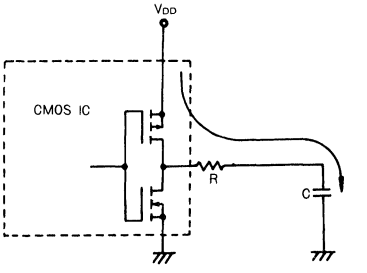


Fig. 22 Less Output Capacitance and Output Current Under 10mA

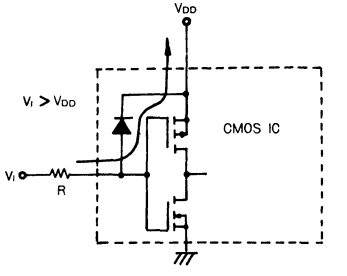


Fig. 23 If Input is Applied Earlier than Power Supply

3.14 How to Terminate Unused Input

If the input is open, the output is unsteady due to indefinite input potential, because CMOS input impedance is very high. It is recommended that unused inputs be connected to V_{DD} in case of NAND gates or are to V_{SS} in case of NOR gates directly or through resistors ranging from 10kΩ to 100kΩ.

3.15 Parallel Connection

The fan-outs can be increased by connecting in parallel with the same kind of gate. The switching speeds are improved by this means.

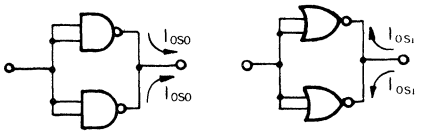


Fig. 24 Expansion of Fan-Out by Parallel Connection

3.16 It is not recommended to used a wired OR.

Fig. 25 shows that the correct logic level cannot be obtained from the outputs of which voltage becomes about a half level ($V_{DD} \sim V_{SS}$) because, when $I_1 = I_2$ is Low and $I_3 = I_4$ is High, the output voltage is determined by the ratio of P-channel and N-channel MOS transistors being ON.

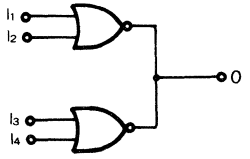


Fig. 25 Wired OR Connection (Inhibit)

3.17 Output short

Do not short the outputs (V_{DD} or V_{SS}) as there are no protection circuits that limit output currents. A long duration of output short may damage the device. Considering steady operation and reliability, it is advised that the maximum output currents should be within 1.5 times those at V_{DD} = 15V

4. How to Handle The MOS Device

All our MOS IC devices contain circuitry to protect the input against damage due to high static voltages or electric fields; however care should be taken so avoid chance accidents.

4.1 Human Body

The operators who test or handle the device should be careful to ground themselves through the registers (1 ~ 10MΩ).

4.2 Storing and Transportation

Store and transport the devices in the original cases which we offer. A conductive material or special magazine rail is suitable for use. These are used so all leads of ICs are shorted or isolated from external fields.

4.3 Testing and Handling

The testing or transfer from the carrier to another place should be done on a conductive board (metall board, etc.). The operators should be grounded electrically to a conductive table (for instance, through metarllic cords or chains) while testing or handling. The earth terminals of instruments for testing or handling should be connected to the same table. Do not apply the signal while the device power is OFF.

4.4 Attachment

To protect against defects in production, MOS ICs should be attached to the PC board after attaching all other parts and the ICs, metallic parts of the board, instruments and operators are connected to the same potential (earth). If earthing is not possible, operators should touch the PC board before attaching MOS ICs to it.

4.5 Soldering

The tip of the soldering iron, including low voltage ones, and the solder pot should be kept at the same potential as the MOS IC and PC board.

4.6 Static Electric Field

Operators should wear clothing which is unlikely to generate static electricity. (Wool, silk and synthetic fibers are unsuitable.) After attaching the MOS IC to the PC board, it is recommended that a conductive clip or tape should be connected to the PC board in order to protect against static electricity, because the PC board is a part of the leads from the IC until the appropriate voltage is applied to the completed PC board.

4.7 Terminal Voltage

Do not insert or remove the PC board (including CMOS devices) with the power applied, in order to avoid permanent damage by excessive voltage.

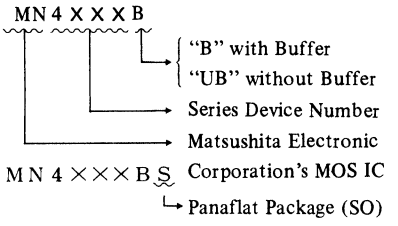
4.8 Surge Voltage

Surge voltage such as power ON-OFF, relay, etc. should be removed.

5. Ordering and Marking

Matsushita CMOS devices may be ordered by using a simplified purchasing code.

Device Name



Note: SO=Small Outline Package

• Current

Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

I_I	Input Current	The current flowing into a device at specified input voltage and V_{DD}.
I_{OH}	Output High Current	The drive current flowing out of the device at specified High output voltage and V_{DD}.
I_{OL}	Output Low Current	The drive current flowing into the device at specified Low output voltage and V_{DD}.
I_{DD}	Quiescent Power Supply Current	The current flowing into the V_{DD} lead at specified input and V_{DD} conditions.
I_{OZ}	Output OFF Current High	The leakage current flowing into the output of a 3-state device in the "OFF" state at a specified High output voltage and V_{DD}.
I_{IL}	Input Current Low	The current flowing into a device at a specified Low level input voltage and a specified V_{DD}.
I_{IH}	Input Current High	The current flowing into a device at a specified High level input voltage and a specified V_{DD}.
I_{DDL}	Quiescent Power Supply Current Low	The current flowing into the V_{DD} lead with a specified Low level input voltage on all inputs and specified V_{DD} conditions.
I_{DDH}	Quiescent Power Supply Current	The current flowing into the V_{DD} lead with a specified High level input voltage on all inputs and specified V_{DD} conditions.

• Voltages

All voltage are referenced to the V_{SS} which is the most negative potential applied to the device.

V_{DD}	Drain Voltage	The most positive potential on the device.
V_{SS}	Source Voltage	For device with a single negative power supply, the most negative power supply, used as the reference level for other voltages. Typically ground.
V_{EE}	Source Voltage	One of two negative power supplies, the most negative power supply used as a reference level for other voltages.
V_{IH}	Input High Voltage	The range of input voltages that represents a logic High level in the system.
V_{IL}	Input Low Voltage	The range of input voltages that represents a logic Low level in the system.
V_{OH}	Output High Voltage	The range of voltages at an output terminal with specified output loading and supply voltage.
V_{OL}	Output Low Voltage	The range of voltages at an output terminal with specified output loading and supply voltage.

• Analog Terms

R_{ON}	ON Resistance	The effective "ON" state resistance of an analog transmission gate, at specified input voltage, output load and V_{DD}.
ΔR_{ON}	"Δ" ON Resistance	The difference in effective "ON" resistance between any two transmission gates of an analog device at specified input voltage, output load and V_{DD}.

• AC Switching • Parameters

f_i	Input Frequency	t_w	Pull Width
f_o	Output Frequency	t_{hold}	Hold Time
f_{max}	Maximum Clock Frequency	t_{su}	Set-Up Time
t_r, t_f	Clock Input Rise, Fall Time	t_{PHZ}	3-State Output Disable Time H → Z
t_{PLH}	Transfer Delay (Propagation Delay Time)	t_{PLZ}	3-State Output Disable Time L → Z
t_{PHL}	Transfer Delay (Propagation Delay Time)	t_{PZH}	3-State Output Enable Time Z → "H"
t_{TLH}	Rise Time L → H	t_{PZL}	3-State Output Enable Time Z → "L"
t_{THL}	Fall Time H → L	t_R	Recovery Time

General Specifications

GENERAL SPECIFICATIONS CONTENTS

MN4000B Series General Specifications

The MN4000B series operate in the range that V_{DD} is +3 ~ +15V (V_{SS} = 0V) but all ratings are guaranteed at the 3 points of 5V, 10V and 15V. Because the CMOS logic has wide operation range as mentioned above, it is not so critical on source regulation as conventional logic ICs (TTL, LS-TTL, etc.) If speed, noise margin, interface to other systems, etc. are not a concern, it operates at V_{DD} = +3V (min). If power consumption and interface to other systems are not a concern, it operates at V_{DD} = +15V (max.). Connect unused input terminals to V_{DD}, V_{CC} or other input terminals. Although treatment against static electricity is conducted on I/O terminals of CMOS logic ICs, precautions against static electricity during handling are recommended.

Ratings are described in individual data sheets. However, to assist understanding the outline of the MN4000B series' CMOS logic ICs, specifications which are common in general are shown hereunder.

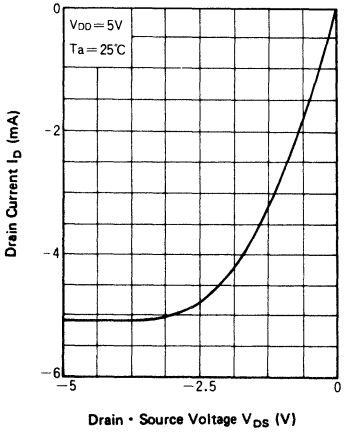
1. Absolute Maximum Ratings (V_{SS} = 0V)

Item			Symbol	Rating	Unit
Supply Voltage			V_{DD}	−0.5~+18	V
Input Voltage			V_I	−0.5~V_{DD}+0.5*	V
Output Voltage			V_O	−0.5~V_{DD}+0.5*	V
Peak Input • Output Current			±I	max. 10	mA
Power Dissipation	MN4XXXXB (DIL Package)	Ta=−40~+60℃	P_D**	max. 400	mW
		Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	mW
	MN4XXXXBS (DIL Package)	Ta=−40~+60℃	P_D	max. 275	mW
		Ta=+60~+85℃		Decrease up to 200mW rating at 3.8mW/°C	mW
Power Dissipation (Per output terminal)			P_D	max. 100	mW
Operating Ambient Temperature			Topr	−40~+85	℃
Storage Temperature			Tstg	−65~+150	℃

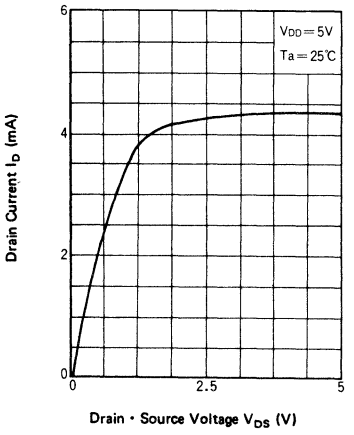
*V_{DD} + 0.5V should be under 18V. **Individual specifications are described in DIL package type.

2. Main Characteristics Figures

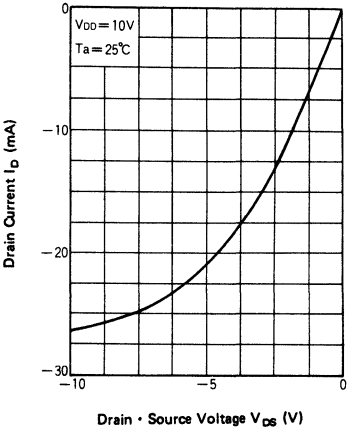
$I_D - V_{DS}$ (P channel)



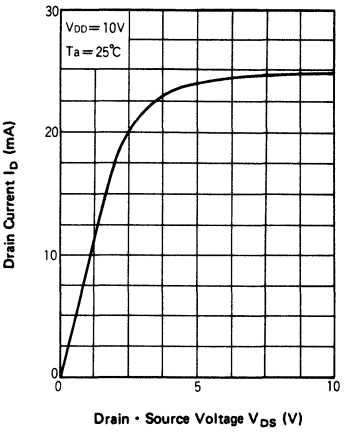
$I_D - V_{DS}$ (N channel)



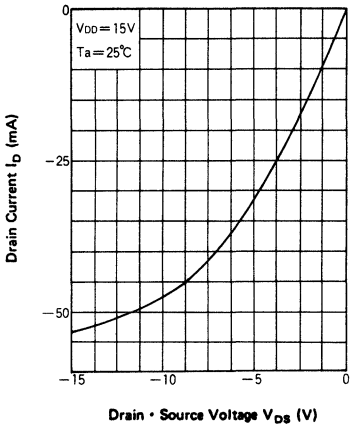
$I_D - V_{DS}$ (P channel)



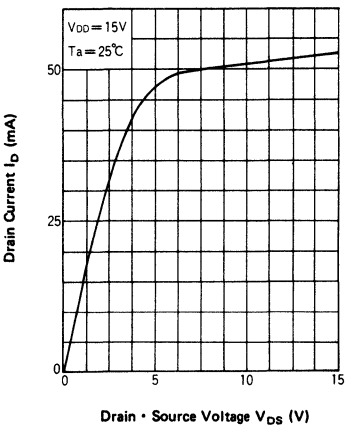
$I_D - V_{DS}$ (N channel)



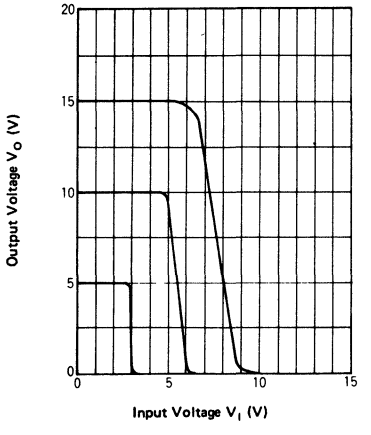
$I_D - V_{DS}$ (P channel)



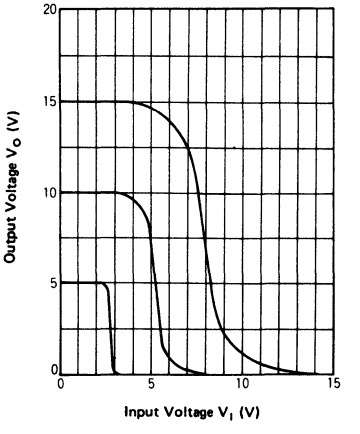
$I_D - V_{DS}$ (N channel)



Transfer Characteristics (With Buffer)



Transfer Characteristics (Without Buffer)



3. DC Characteristics

DC Characteristics (V_{SS} = 0V; Implicit case)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current										
Gates	5	I_{DD}	all valid input combinations, $V_I=V_{SS}$ or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	μA
	15			—	4	—	4	—	30	μA
Buffers, flip-flops	5	I_{DD}		—	4	—	4	—	30	μA
	10			—	8	—	8	—	60	μA
	15			—	16	—	16	—	120	μA
MSI	5	I_{DD}		—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	μA
	15			—	80	—	80	—	600	μA
Output Voltage Low Level	5	V_{OL}	$V_I=V_{SS}$ or V_{DD}, $\|I_O\|<1\mu A$	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	V
	15			—	0.05	—	0.05	—	0.05	V
Output Voltage High Level	5	V_{OH}	$V_I=V_{SS}$ or V_{DD}, $\|I_O\|<1\mu A$	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	V
	15			14.95	—	14.95	—	14.95	—	V
Input Voltage Low Level (Only for Buffer)	5	V_{IL}	V_O=0.5V or 4.5V, $\|I_O\|<1\mu A$	—	1.5	—	1.5	—	1.5	V
	10		V_O=1.0V or 9.0V, $\|I_O\|<1\mu A$	—	3	—	3	—	3	V
	15		V_O=1.5V or 13.5V, $\|I_O\|<1\mu A$	—	4	—	4	—	4	V
Input Voltage High Level (Only for Buffer)	5	V_{IH}	V_O=0.5V or 4.5V, $\|I_O\|<1\mu A$	3.5	—	3.5	—	3.5	—	V
	10		V_O=1.0V or 9.0V, $\|I_O\|<1\mu A$	7	—	7	—	7	—	V
	15		V_O=1.5V or 13.5V, $\|I_O\|<1\mu A$	11	—	11	—	11	—	V
Input Voltage Low Level (Except for Buffer)	5	V_{IL}	V_O=0.5V or 4.5V, $\|I_O\|<1\mu A$	—	1	—	1	—	1	V
	10		V_O=1.0V or 9.0V, $\|I_O\|<1\mu A$	—	2	—	2	—	2	V
	15		V_O=1.5V or 13.5V, $\|I_O\|<1\mu A$	—	2.5	—	2.5	—	2.5	V
Input Voltage High Level (Except for Buffer)	5	V_{IH}	V_O=0.5V or 4.5V, $\|I_O\|<1\mu A$	4	—	4	—	4	—	V
	10		V_O=1.0V or 9.0V, $\|I_O\|<1\mu A$	8	—	8	—	8	—	V
	15		V_O=1.5V or 13.5V, $\|I_O\|<1\mu A$	12.5	—	12.5	—	12.5	—	V
Output (sink) Current Low Level	5	I_{OL}	V_O= 0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O= 0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	mA
	15		V_O= 1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	mA
Output (source) Current High Level	5	$-I_{OH}$	V_O= 4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O= 9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	mA
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	mA
Output Current High Level	5	$-I_{OH}$	V_O= 2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I = 0 or 15V	—	0.3	—	0.3	—	1	μA
3-State Output Pin: Leakage Current High Level	15	I_{OZH}	output returned to V_{DD}	—	1.6	—	1.6	—	12	μA
3-State Output Pin: Leakage Current Low Level	15	$-I_{OZL}$	output returned to V_{SS}	—	1.6	—	1.6	—	12	μA

4. Switching Characteristics

• Clock Rise, Fall Times (t_r, t_f)

The upper limit of t_r, t_f will depend on the device or supply voltage. Input clock rise and fall times are less than 15μs at 5V operation, less than 4μs at 10V operation, and less than 1μs at 15V operation if not specified in individual data sheets.

• Output Rise, Fall Time (t_{TLH}, t_{THL})

V_{SS} = 0V, Ta = 25°C, C_L = 50pF, Input Rise • Fall Time ⩽ 20ns.

Item	V_{DD} (V)	Symbol	min.	typ.	max.		External Capacitance
Output Fall Time HIGH → LOW	5	t_{THL}	—	60	120	ns	10ns+(1.0ns/pF)C_L
	10		—	30	60	ns	9ns+(0.42ns/pF)C_L
	15		—	20	40	ns	6ns+(0.28ns/pF)C_L
Output Rise Time LOW → HIGH	5	t_{TLH}	—	60	120	ns	10ns+(1.0ns/pF)C_L
	10		—	30	60	ns	9ns+(0.42ns/pF)C_L
	15		—	20	50	ns	6ns+(0.28ns/pF)C_L

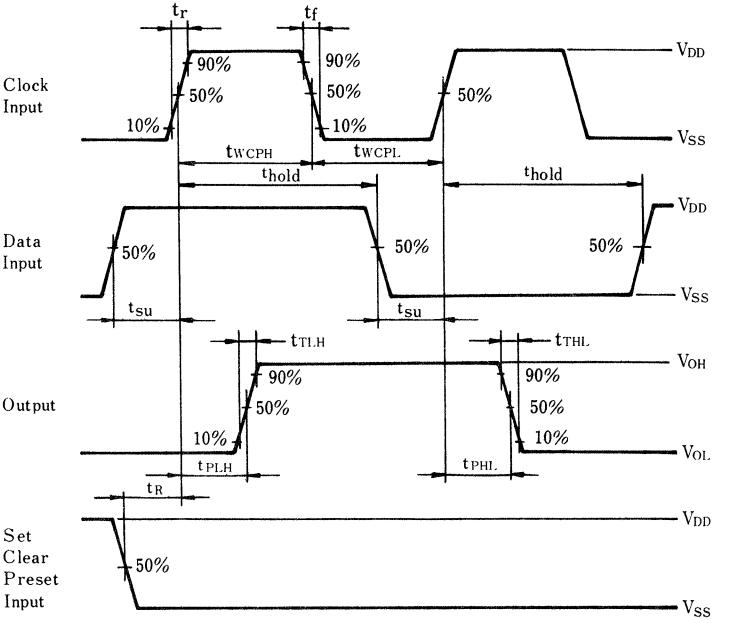
• Temperature Coefficient (Typical)

Transfer Delay (Propagation Delay Time)	+0.35%/°C
Output Rise, Fall Time	+0.35%/°C

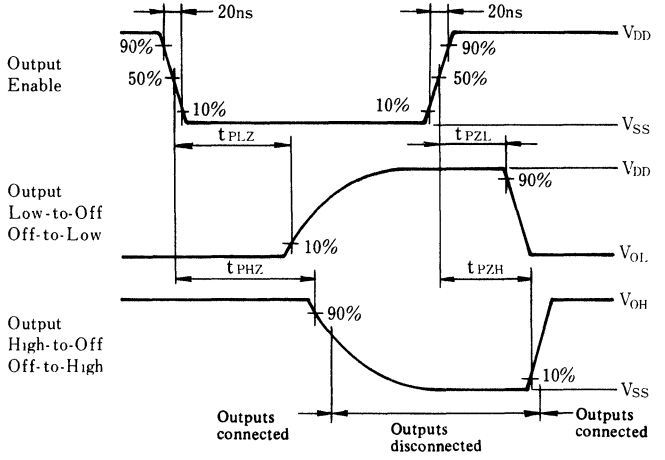
• Input Capacitance (Digital Input)

Maximum Input Capacitance C_I = 7.5pF

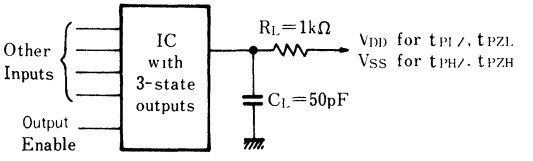
• Setup Time, Hold Time, Transfer Delay, Recovery Time, Rise and Fall Time



- **Transfer Delay of Tristate Output**



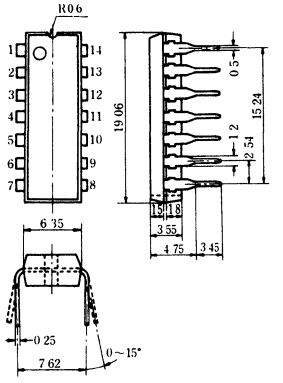
- **Test Circuit of Tristate Output IC**



5. Mechanical Data

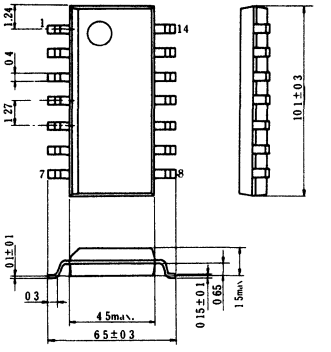
Unit: mm

P-1



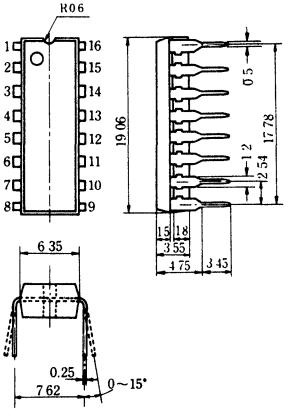
14-Pin • Plastic DIL Package

P-2



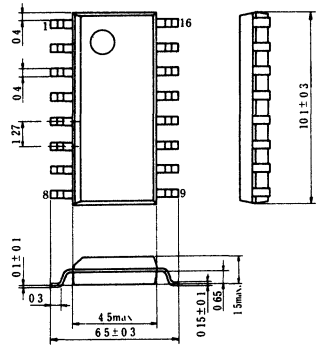
14-Pin • Panaflat Package (SO-14D)

P-3



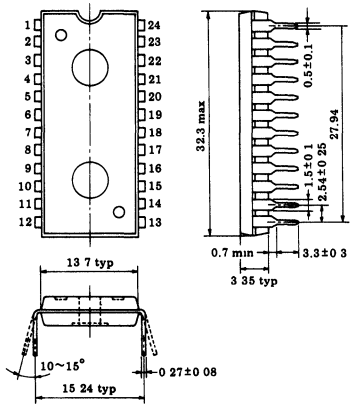
16-Pin • Plastic DIL Package

P-4



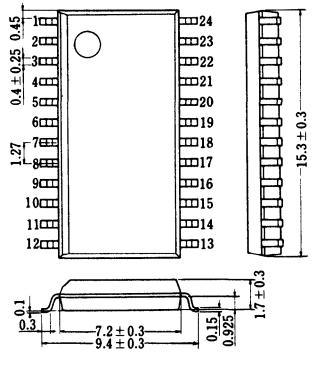
16-Pin • Panaflat Package (SO-16D)

P-5



24-Pin • Plastic DIL Package

P-6



24-Pin • Panaflat Package (SO-24D)

Individual Specifications

Index Table

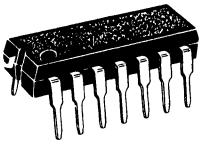
MN4000B/MN4000BS

Dual 3-Input NOR Gates and Inverters

■ Description

The MN4000B/S are dual 3-input NOR gate and inverters.
Their primary use is where low power dissipation and/or high noise immunity is desired.

P-1

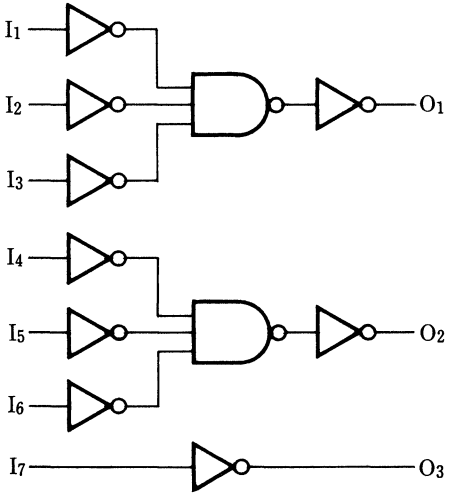


14-Pin • Plastic DIL Package

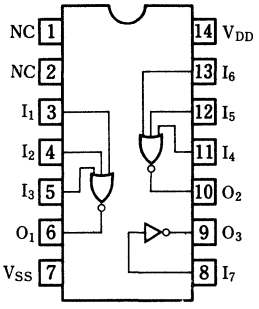
P-2

14-Pin • Panaflat Package (SO-14D)

■ Logic Diagram



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

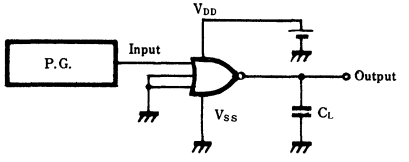
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0V or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0V or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0V or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0V or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0V or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0V or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0V or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0V or 15V	—	0.3	—	0.3	—	1	μA

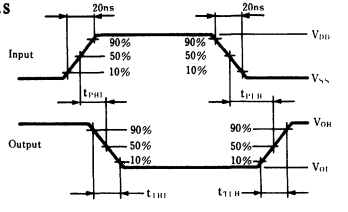
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time I_1~I_6→O_1, O_2	5	t_{PHL}	—	70	210	ns
	10	t_{PLH}	—	35	105	
	15		—	30	90	
Propagation Delay Time I_7→O_3	5	t_{PHL}	—	45	135	ns
	10	t_{PLH}	—	25	75	
	15		—	20	60	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



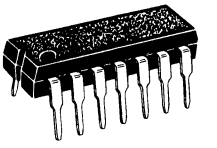
MN4001B/MN4001BS

Quad 2-Input NOR Gates

■ Description

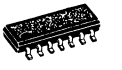
The MN4001B/S are positive 2-input NOR gates and have 4 circuits in a package.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time.
The MN4001B/S are equivalent to MOTOROLA MC14001B and RCA CD4001B.

P-1



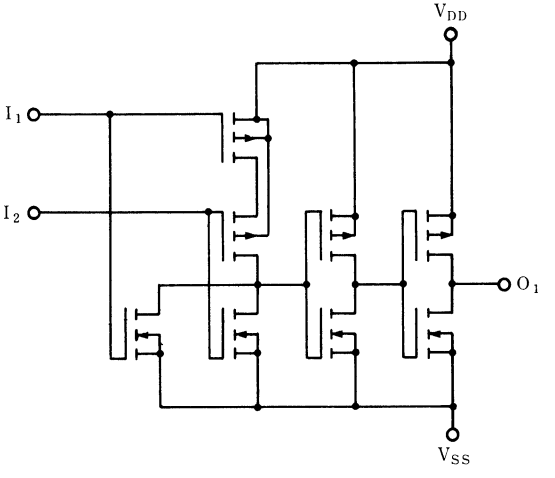
14-Pin • Plastic DIL Package

P-2

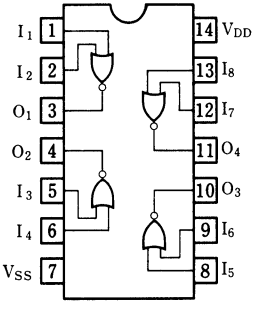


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/4)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

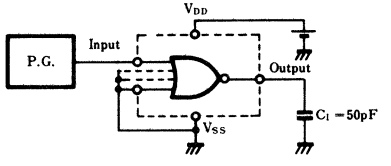
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0V or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0V or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0V or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0V or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0V or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0V or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0V or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0V or 15V	—	0.3	—	0.3	—	1	μA

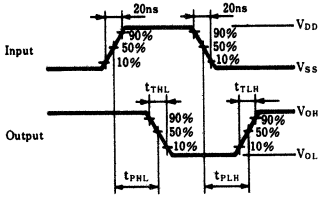
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	50	150	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time	5	t_{PHL}	—	60	180	ns
	10		—	25	75	
	15		—	20	60	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



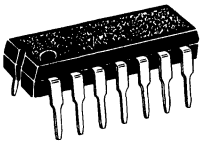
MN4002B/MN4002BS

Dual 4-Input NOR Gates

■ Description

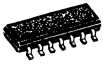
The MN4002B/S are positive 4-input NOR gates and have 2 circuits in a package.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
The MN4002B/S are equivalent to MOTOROLA MC14002B and RCA CD4002B.

P-1



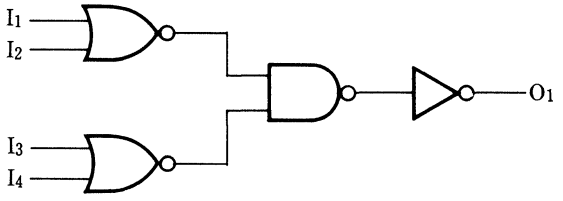
14-Pin • Plastic DIL Package

P-2

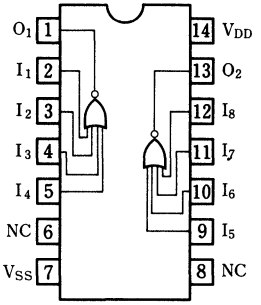


14-Pin • Panaflat Package (SO-14D)

■ Logic Diagram (1/2)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

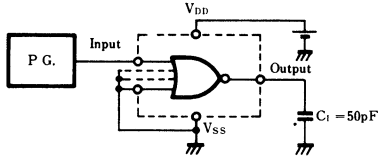
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0V or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0V or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0V or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0V or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0V or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0V or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0V or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0V or 15V	—	0.3	—	0.3	—	1	μA

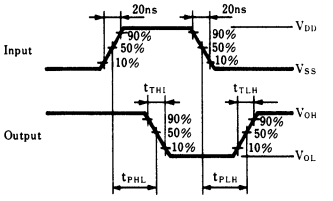
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	50	150	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time	5	t_{PHL}	—	60	180	ns
	10		—	25	75	
	15		—	20	60	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



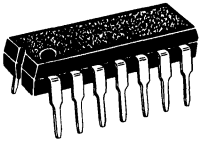
MN4006B/MN4006BS

18-Bit Static Shift Registers

■ Description

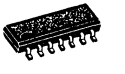
The MN4006B/S are maximum 18-bit static shift registers composed of two 4-bit shift registers and five 5-bit shift registers. Clock pulses for all registers are input through the common CP.
By properly combining input and output, shift registers with the arbitrary stages of 4, 5, 8, 9, 10, 12, 13, 14, 16 and 17 are enabled.
The MN4006B/S are equivalent to MOTOROLA MC14006B and RCA CD4006B.

P- 1



14-Pin • Plastic DIL Package

P- 2



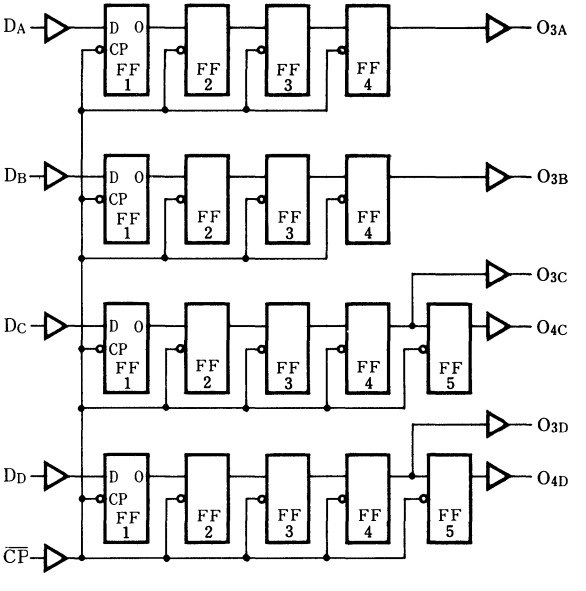
14-Pin • Panaflat Package (SO-14D)

■ Truth Table

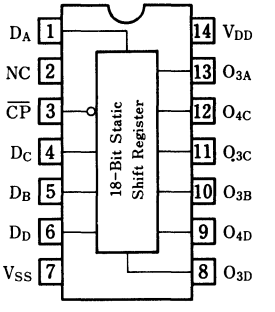
D_n	$\overline{CP}$	O_{n+1}
D_1	↓	D_1
×	↑	no change

Note) × : don't care

■ Logic Diagram



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

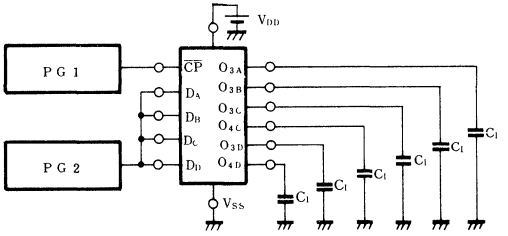
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\lvert I_O \rvert$<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\lvert I_O \rvert$<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O \rvert$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O \rvert$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0V or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0V or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0V or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0V or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0V or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0V or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0V or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0V or 15V		—	0.3	—	0.3	—	1	μA

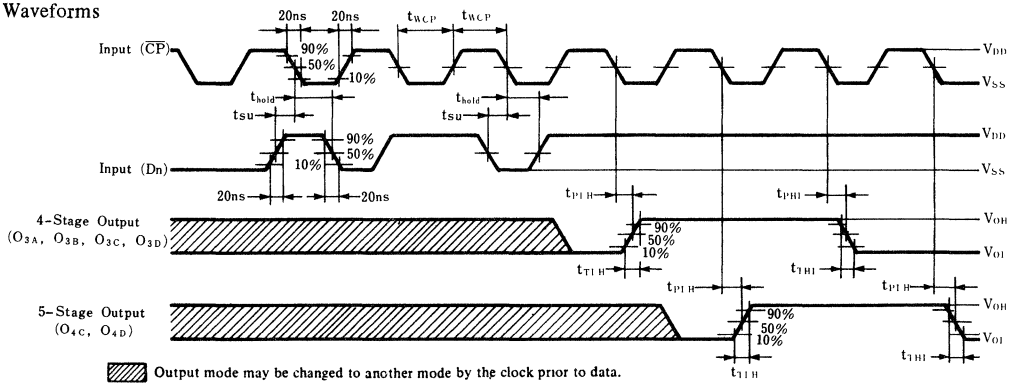
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $\overline{CP}$→On (H→L)	5	t_{PHL}	—	90	270	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time $\overline{CP}$→On (L→H)	5	t_{PLH}	—	90	270	ns
	10		—	40	120	
	15		—	35	105	
Minimum Clock Pulse Width	5	t_{WCPH}	—	30	90	ns
	10		—	20	60	
	15		—	15	45	
Set-up Time Dn→$\overline{CP}$	5	tsu	—	10	30	ns
	10		—	5	15	
	15		—	0	10	
Hold Time Dn→$\overline{CP}$	5	t_{hold}	—	−5	10	ns
	10		—	0	10	
	15		—	0	10	
Maximum Clock Frequency	5	f_{max}	9	18	—	MHz
	10		15	30	—	
	15		18	36	—	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



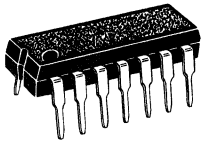
MN4007UB/MN4007UBS

Dual Complementary Pairs and Inverters

■ Description

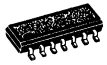
The MN4008UB/S are inverters in which a pair of the same 3-element N channel enhancement MOS FETs as 3-element P channel enhancement MOS FETs are incorporated in a package. One pair is the inverter and the other two are the complementary pair; source and drain are differently output.
The MN4007UB/S have been widely applied to inverters, pulse-shaping circuits, NAND (NOR) gates, linear amplifiers, clock gates, transmission gates, high fan-out buffers, etc.
The MN4007UB/S are equivalent to RCA CD4007UB.

P-1



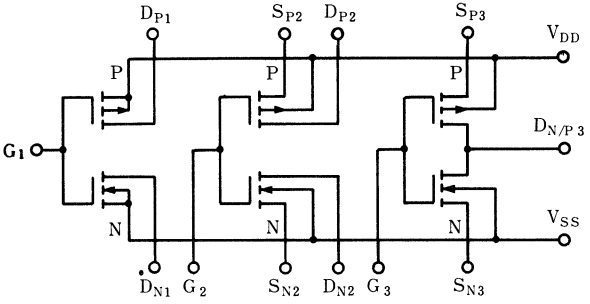
14-Pin • Plastic DIL Package

P-2

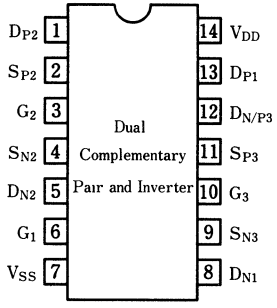


14-Pin • Panaflat Package (SO-14D)

■ Segment Configuration



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

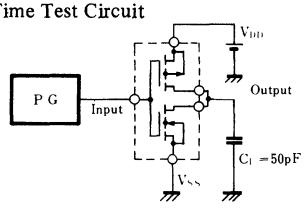
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0V or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0V or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0V or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0V or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0V or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0V or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0V or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0V or 15V	—	0.3	—	0.3	—	1	μA

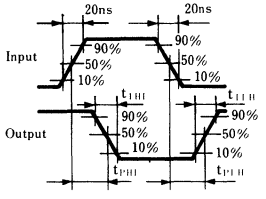
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time Gn—D_N; D_P (H→L)	5	t_{PHL}	—	40	120	ns
	10		—	20	60	
	15		—	15	45	
Propagation Delay Time Gn—D_N; D_P (L→H)	5	t_{PLH}	—	40	120	ns
	10		—	20	60	
	15		—	15	45	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



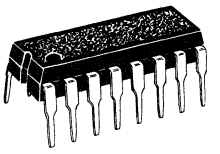
MN4008B / MN4008BS

4-Bit Full Adders

■ Description

The MN4008B/S are 4-bit parallel processing full adders with a high-speed parallel carry circuit.
Summation of 4 added data input ($A_0 \sim A_3$), another 4 adding data inputs ($B_0 \sim B_3$) and binary input added to carry input (C_{IN}) from low row can be obtained by the binary code which is same as adding data outputs ($S_0 \sim S_3$) and carry output (C_{OUT}).
4 X n-bit addition by cascade connection and addition and subtraction circuit by external circuit can easily be composed.

P- 3



16-Pin • Plastic DIL Package

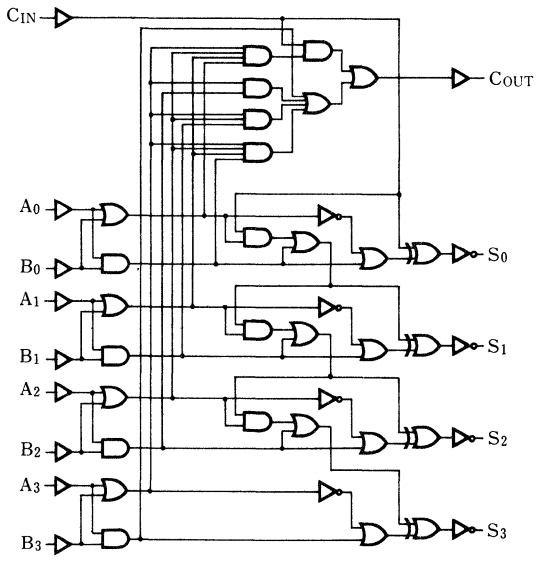
P- 4

16-Pin • Panaflat Package (SO-16D)

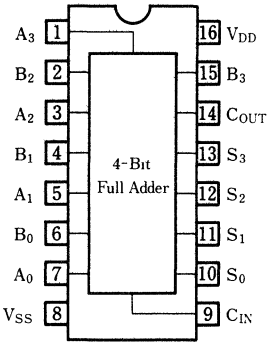
■ Truth Table

Input			Output	
C_{IN}	A	B	C_{OUT}	S
L	L	L	L	L
L	L	H	L	H
L	H	L	L	H
L	H	H	H	L
H	L	L	L	H
H	L	H	H	L
H	H	L	H	L
H	H	H	H	H

■ Logic Diagram



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

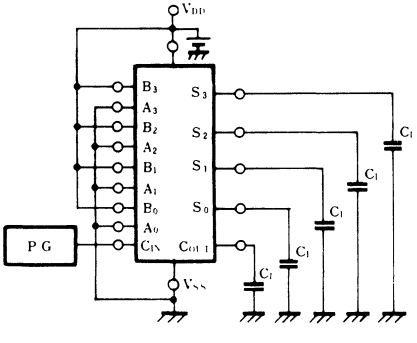
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0V or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0V or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0V or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0V or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0V or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0V or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0V or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0V or 15V		—	0.3	—	0.3	—	1	μA

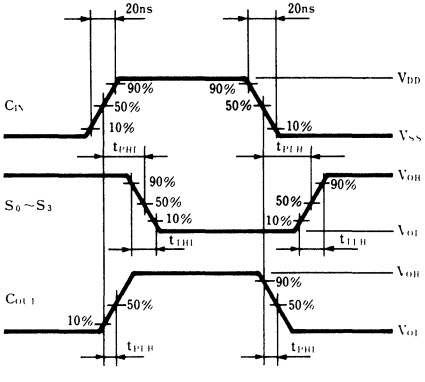
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time Sum in→Sum out (L→H)	5	t_{PLH}	—	135	405	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time Sum in→Sum out (H→L)	5	t_{PHL}	—	150	450	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time Sum in→Cout (L→H)	5	t_{PLH}	—	100	300	ns
	10		—	45	135	
	15		—	30	90	
Propagation Delay Time Sum in→Cout (H→L)	5	t_{PHL}	—	125	375	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time C_{IN}→Sum out (L→H)	5	t_{PLH}	—	115	345	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time C_{IN}→Sum out (H→L)	5	t_{PHL}	—	130	390	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time C_{IN}→Cout (L→H)	5	t_{PLH}	—	75	225	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time C_{IN}→Cout (H→L)	5	t_{PHL}	—	90	270	ns
	10		—	35	105	
	15		—	25	75	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



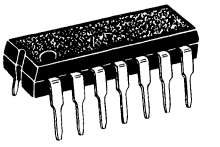
MN4011B/MN4011BS

Quad 2-Input NAND Gates

■ Description

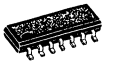
The MN4011B/S are positive 2-input NAND gates and have 4 circuits in a package.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing of load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
The MN4011B/S are equivalent to MOTOROLA MC14011B and RCA CD4011B.

P-1



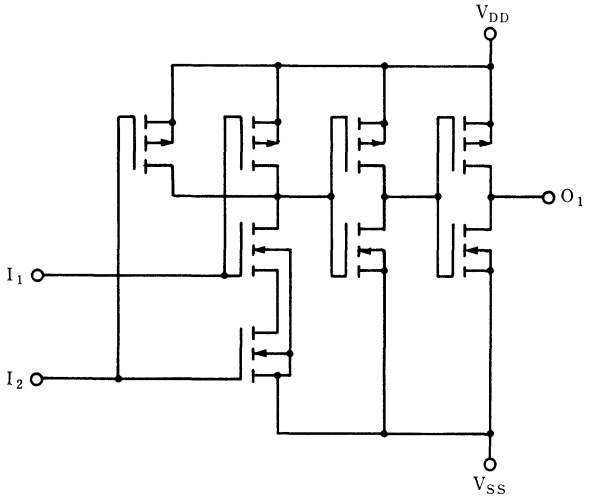
14-Pin • Plastic DIL Package

P-2

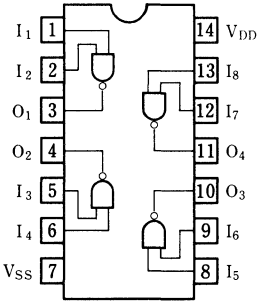


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/4)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

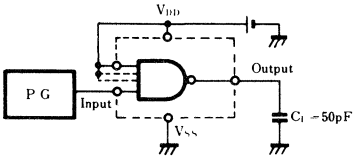
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		| I_O | <1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		| I_O | <1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0V or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0V or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0V or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0V or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0V or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0V or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0V or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0V or 15V	—	0.3	—	0.3	—	1	μA

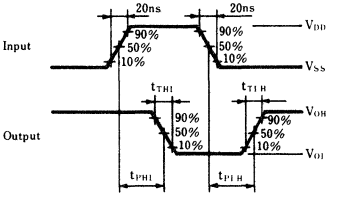
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	55	165	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time	5	t_{PHL}	—	55	165	ns
	10		—	25	75	
	15		—	20	60	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



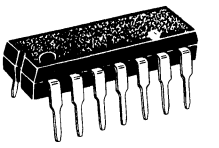
MN4012B/MN4012BS

Dual 4-Input NAND Gates

■ Description

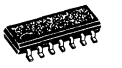
The MN4012B/S are positive 4-input NAND gates and have 2 circuits in a package.
The outputs are fully buffered to improve propagation characteristics between the input and output which are affected by increasing of load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
The MN4012B/S are equivalent to MOTOROLA MC14012B and RCA CD4012B.

P-1



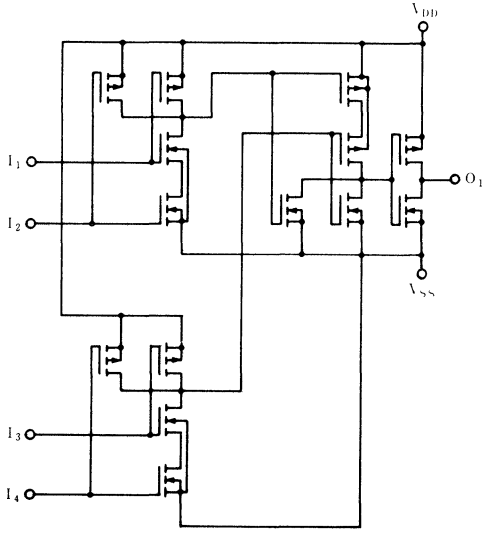
14-Pin • Plastic DIL Package

P-2

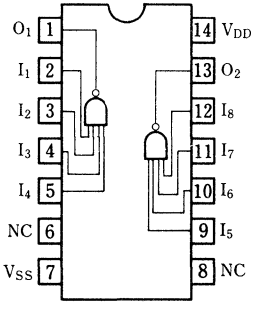


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/2)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

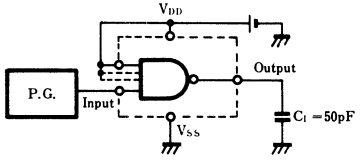
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0V or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0V or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0V or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0V or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0V or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0V or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0V or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0V or 15V	—	0.3	—	0.3	—	1	μA

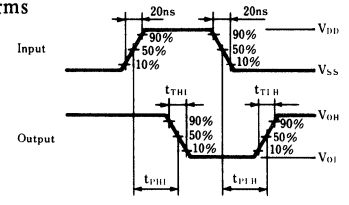
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	70	210	ns
	10		—	30	90	
	15		—	25	75	
Propagation Delay Time	5	t_{PHL}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



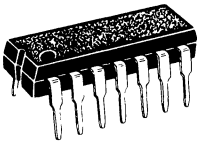
MN4013B / MN4013BS

Dual D-Type Flip-Flops

■ Description

The MN4013B/S are dual D flip-flop. Each flip-flop has independent data, set, clear and clock inputs and complementary outputs (0, $\overline{0}$) only on the positive going edge of the clock.
Logic states are retained either High or Low according to the clock level.
The MN4013B/S are equivalent to MOTOROLA MC14013B and RCA CD4013B.

P-1



14-Pin • Plastic DIL Package

P-2

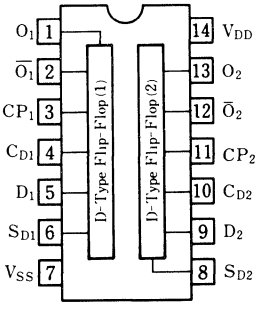
14-Pin • Panaflat Package (SO-14D)

■ Truth Table

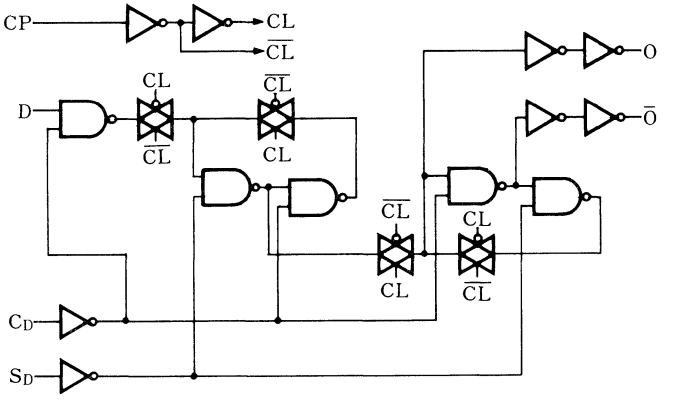
Input				Output	
S_D	C_D	CP	D	O_{n+1}	$\overline{O}_{n+1}$
H	L	×	×	H	L
L	H	×	×	L	H
H	H	×	×	H	H
L	L	↓	×	O_n	$\overline{O}_n$
L	L	↑	L	L	H
L	L	↑	H	H	L

Note) × : don't care

Pin Configuration



■ Logic Diagram (1/2)



Pin Explanation

S_D : Data-set input
C_D : Data-clear input
D : Data input
CP : Clock input
O, $\overline{O}$: Output (complementary)

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

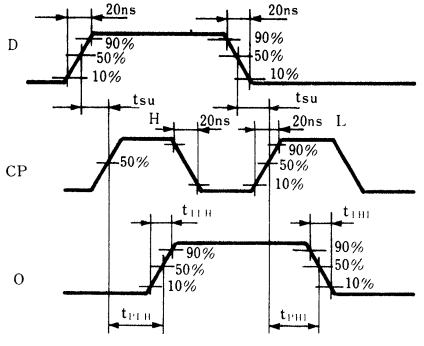
Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	4	—	4	—	30	μA
	10				—	8	—	8	—	60	
	15				—	16	—	16	—	120	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0V or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0V or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0V or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0V or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0V or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0V or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0V or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0V or 15V		—	0.3	—	0.3	—	1	μA

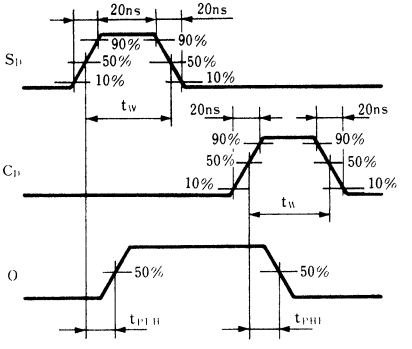
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time (Fig. 1)	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time (Fig. 2)	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Minimum Date Set-up Time	5	t_{SU}	—	30	90	ns
	10		—	10	30	
	15		—	10	30	
Maximum Clock Rise Time Maximum Clock Fall Time	5	$tr\phi$, $tf\phi$	20	—	—	μs
	10		2.5	—	—	
	15		1	—	—	
Maximum Clock Frequency	5	f_{max}	6	12	—	MHz
	10		12	25	—	
	15		18	36	—	
Propagation Delay Time (Fig. 1) (CP−O, $\overline{O}$)	5	t_{PLH}	—	100	300	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time (Fig. 2) (CP−O, $\overline{O}$)	5	t_{PHL}	—	110	330	ns
	10		—	45	135	
	15		—	30	90	
Propagation Delay Time (Fig. 1) (C_D, S_D−O, $\overline{O}$)	5	t_{PLH}	—	135	405	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time (Fig. 2) (C_D, S_D−O, $\overline{O}$)	5	t_{PHL}	—	100	300	ns
	10		—	40	120	
	15		—	30	90	
Minimum Clear Pulse Width (Fig. 2) Minimum Preset Pulse Width (Fig. 2)	5	t_{WCD} t_{WSD}	—	45	135	ns
	10		—	20	60	
	15		—	20	60	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms

(Fig. 1) t_{TLH}, t_{THL}, t_{PLH}(CP-O, $\overline{O}$), t_{PHL}(CP-O, $\overline{O}$) (Fig. 2) t_{PLH}(S_D-O, C_D-$\overline{O}$), t_{PHL}(S_D-O, C_D-$\overline{O}$), t_{WCD}, t_{WSD}





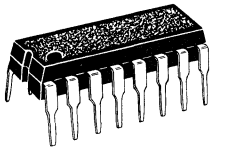
MN4015B / MN4015BS

Dual 4-Stage Static Shift Registers

■ Description

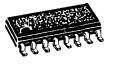
The MN4015B/S are dual 4-bit static shift registers.
Each register of D type flip-flop has a common reset input and can be cleared asynchronously, and triggered on the positive going edge of the clock.
A High on the reset input clears all registers and forces the outputs (O_0 ~ O_3) Low, independent of the clock and data inputs.
The MN4015B/S are equivalent to MOTOROLA MC14015B and RCA CD4015B.

P-3



16-Pin • Plastic DIL Package

P-4



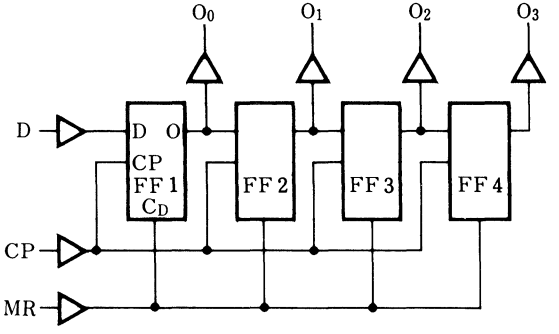
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

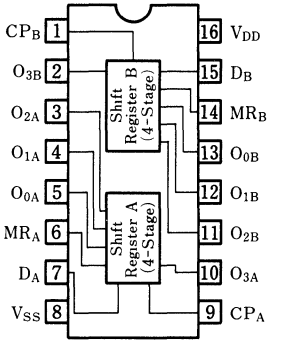
Input				Output			
n	CP	D	MR	O_0	O_1	O_2	O_3
1	↗	D_1	L	D_1	×	×	×
2	↗	D_2	L	D_2	D_1	×	×
3	↗	D_3	L	D_3	D_2	D_1	×
4	↗	D_4	L	D_4	D_3	D_2	D_1
	↘	×	L	no change			
	×	×	H	L	L	L	L

Note) X : don't care
D_n : High or Low
n : Clock pulse count

■ Logic Diagram (1/2)



Pin Configuration



Pin Explanation

D : Data input
CP : Clock input (↗)
MR : Reset input
O_0~O_3 : Output (4 Bits)

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

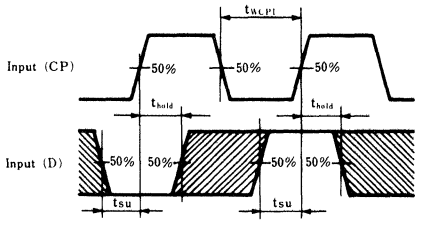
Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0V or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0V or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0V or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0V or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0V or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0V or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0V or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0V or 15V		—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP—On(H→L)	5	t_{PHL}	—	145	435	ns
	10		—	60	180	
	15		—	40	120	
Propagation Delay Time CP—On(L→H)	5	t_{PLH}	—	120	360	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time MR→On(H→L)	5	t_{PHL}	—	185	555	ns
	10		—	70	210	
	15		—	40	120	
Set-up Time (Fig. 1) D→CP	5	t_{su}	—	55	166	ns
	10		—	15	45	
	15		—	10	30	
Hold Time (Fig. 1) D→CP	5	t_{hold}	—	20	60	ns
	10		—	10	30	
	15		—	8	24	
(Fig. 1) Minimum Clock Pulse Width	5	t_{WCPL}	—	50	150	ns
	10		—	20	60	
	15		—	15	45	
(Fig. 2) Minimum Reset Pulse Width	5	t_{WMRH}	—	55	165	ns
	10		—	20	60	
	15		—	15	45	
Reset Recovery Time (Fig. 2)	5	t_{RMR}	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
Maximum Clock Frequency	5	f_{max}	4	9	—	MHz
	10		12	23	—	
	15		17	34	—	
Input Capacitance		C_I	—	—	7.5	pF

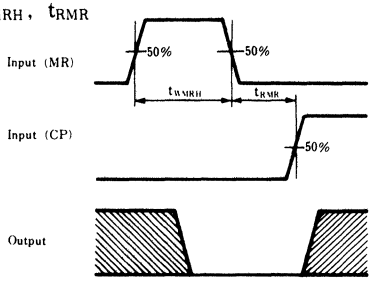
• Dynamic Signal Waveforms

(Fig. 1) t_{su}, t_{hold}, t_{WCPL}



Waveforms showing set-up times, hold times and minimum clock pulse width

(Fig. 2) t_{WMRH}, t_{RMR}



Waveforms showing recovery time for MR and minimum MR pulse width

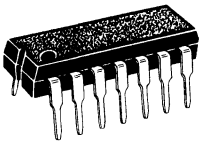
MN4016B/MN4016BS

Quad Analog Switches

■ Description

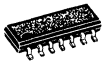
The MN4016B/S have 4 independent analog switches. A High on the enable input establishes a low impedance state (ON stage) between input and output of the switch.
A Low produces a high impedance (OFF state).
This can be utilized for analog or digital signal switching and for choppers, modulators and demodulators.
The MN4016B/S are equivalent to MOTOROLA MC14016B and RCA CD4016B.

P-1



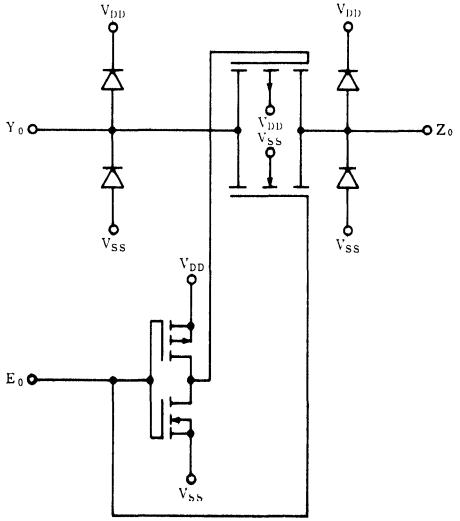
14-Pin • Plastic DIL Package

P-2

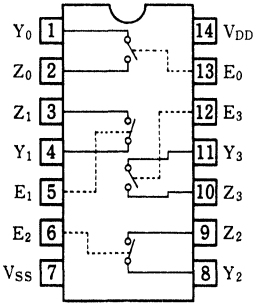


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/4)



Pin Configuration



Pin Explanation

$E_0 \sim E_3$: Enable input $Z_0 \sim Z_3$: Analog input/output
$Y_0 \sim Y_3$: Analog input/output

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	1	—	1	—	7.5	μA
	10				—	2	—	2	—	15	
	15				—	4	—	4	—	30	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ DC Characteristics (Ta=25℃, V_{SS}=0V)

Item	V_{DD}(V)	Symbol	Conditions	min.	typ.	max.	Unit
On Resistance	5	R_{ON}	V_{SS}=0V, V_I=5V	—	200	—	Ω
			V_{SS}=0V, V_I=2.5V	—	8000	—	
			V_{SS}=0V, V_I=0.25V	—	200	—	
	10	R_{ON}	V_{SS}=0V, V_I=10V	—	150	700	Ω
			V_{SS}=0V, V_I=5V	—	250	1500	
			V_{SS}=0V, V_I=0.25V	—	150	700	
	15	R_{ON}	V_{SS}=0V, V_I=15V	—	100	500	Ω
			V_{SS}=0V, V_I=7.5V	—	200	950	
			V_{SS}=0V, V_I=0.25V	—	100	500	
	5	R_{ON}	V_{SS}=−5V, V_I=5V	—	150	700	Ω
			V_{SS}=−5V, V_I=±0.25V	—	250	1500	
			V_{SS}=−5V, V_I=−5V	—	150	700	
	7.5	R_{ON}	V_{SS}=−7.5V, V_I=7.5V	—	100	500	Ω
			V_{SS}=−7.5V, V_I=±0.25V	—	200	950	
			V_{SS}=−7.5V, V_I=−7.5V	—	100	500	
Input/Output of leakage current	10	I_{OFF}	V_I=10V, V_O=0V	—	30	125	nA
			V_I=0V, V_O=10V	—	30	125	
	15		V_I=15V, V_O=0V	—	60	250	nA
			V_I=0V, V_O=15V	—	60	250	

■ Switching Characteristics (Ta=25℃, V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	min.	typ.	max.	Unit
Propagation Delay Time (Fig. 1) (Vis→Vos)	5	t_{PHL}	R_L=10kΩ, C_L=50pF, En=V_{DD}	—	25	75	ns
	10			—	10	30	
	15			—	5	15	
Propagation Delay Time (Fig. 1) (Vis→Vos)	5	t_{PLH}		—	20	60	ns
	10			—	10	30	
	15			—	5	15	
Propagation Delay Time (Fig. 1) (En→Vos) (H)	5	t_{PHZ}	R_L=10kΩ, C_L=50pF, Vis=V_{DD}, R_L→V_{SS}	—	95	285	ns
	10			—	85	255	
	15			—	85	255	
Propagation Delay Time (Fig. 1) (En→Vos) (L)	5	t_{PLZ}	R_L=10kΩ, C_L=50pF, Vis=V_{SS}, R_L→V_{DD}	—	50	150	ns
	10			—	55	165	
	15			—	60	180	
Propagation Delay Time (Fig. 1) (En→Vos) (H)	5	t_{PZH}	R_L=10kΩ, C_L=50pF, Vis=V_{DD}, R_L→V_{SS}	—	35	105	ns
	10			—	20	60	
	15			—	15	45	
Propagation Delay Time (Fig. 1) (En→Vos) (L)	5	t_{PZL}	R_L=10kΩ, C_L=50pF, Vis=V_{SS}, R_L→V_{DD}	—	35	105	ns
	10			—	15	45	
	15			—	10	30	
Sine Wave Distortion (Fig. 2)	5		R_L=10kΩ, C_L=15pF, En=V_{DD}, f=1 kHz, Vis=$\frac{1}{2}V_{DD(P-P)}$	—	—	—	%
	10			—	0.1	—	
	15			—	0.1	—	
Crosstalk (Fig. 3) (Between 2 Channels)	5		R_L=1 kΩ, Vis=$\frac{1}{2}V_{DD\ P-P}$	—	—	—	MHz
	10			—	1	—	
	15			—	—	—	
Crosstalk (Fig. 1) (En→Vos)	5		R_L=10kΩ, C_l=15pF, En=V_{DD}	—	—	—	mV
	10			—	80	—	
	15			—	—	—	
Feedthrough (Fig. 2) (OFF)	5		R_L=1 kΩ, C_l=5 pF, En=V_{SS}, Vis=$\frac{1}{2}V_{DD\ P-P}$	—	—	—	kHz
	10			—	700	—	
	15			—	—	—	
Input Capacitance		C_I		—	—	7.5	pF

Fig. 1 Propagation Crosstalk Test Circuit

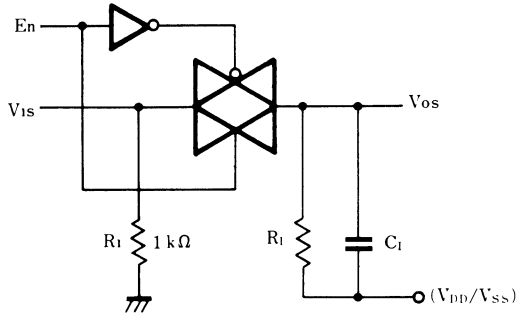
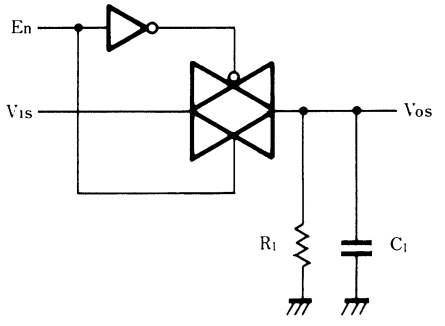
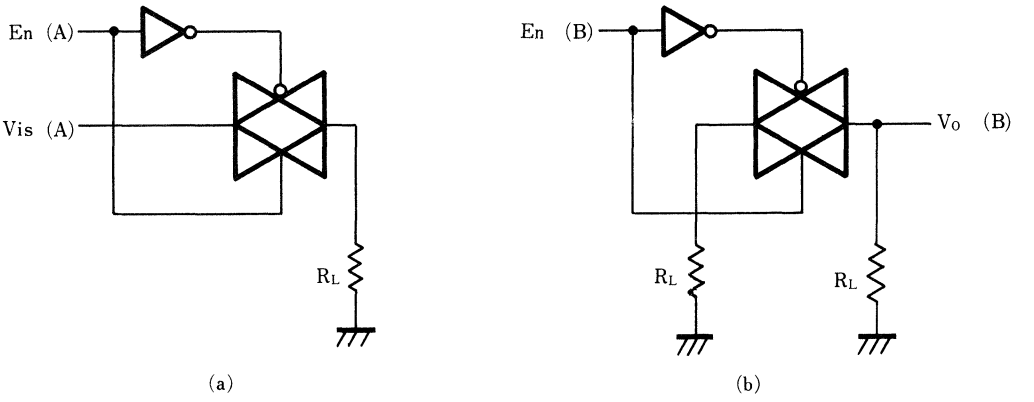


Fig. 2 Sine Wave Distortion, Feedthrough Test Circuit



(Note) $20\log\frac{Vos}{Vis}=-50dB$

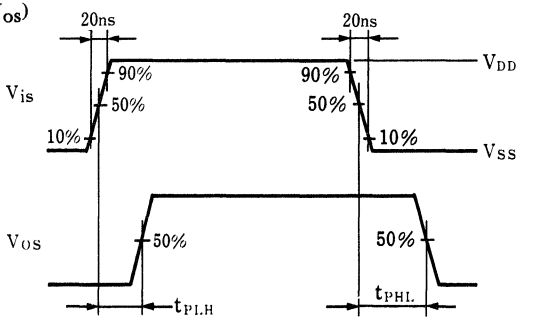
Fig. 3 Crosstalk Test Circuit



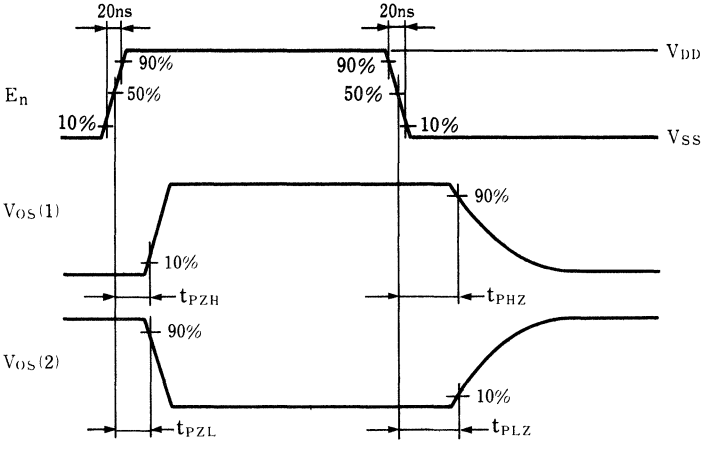
(Note) $20\log\frac{Vos\ (B)}{Vis\ (A)} = -50dB$

■ Timing Diagram

• Delay Timing ($V_{is} \rightarrow V_{os}$)



• Chip Enable Timing Diagram



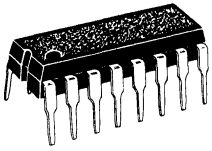
MN4017B/MN4017BS

5-Stage Johnson Counters

■ Description

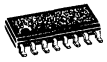
The MN4017B/S are 5-stage Johnson decade counters constructed with five D-type flip-flops. One of the outputs (O_0 ~ O_9) becomes High level according to the number of counter pulses applied to CP_0 or $\overline{CP}_1$. The counter is advanced by either a positive going edge of CP_0 while $\overline{CP}_1$ is Low or a negative going edge of $\overline{CP}_1$ while CP_0 is High. A High on the reset input (MR) resets the counter to zero ($O_0 = \overline{O}_{5-9}$ = High, $O_1 \sim O_9$ = Low) independent of the clock inputs (CP_0, $\overline{CP}_1$).
These are equivalent to MOTOROLA MC14017B and RCA CD4017B.

P-3



16-Pin • Plastic DIL Package

P-4



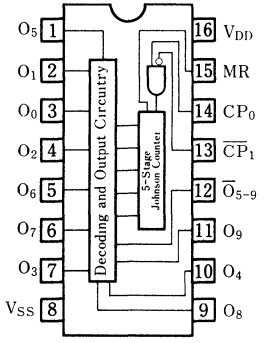
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

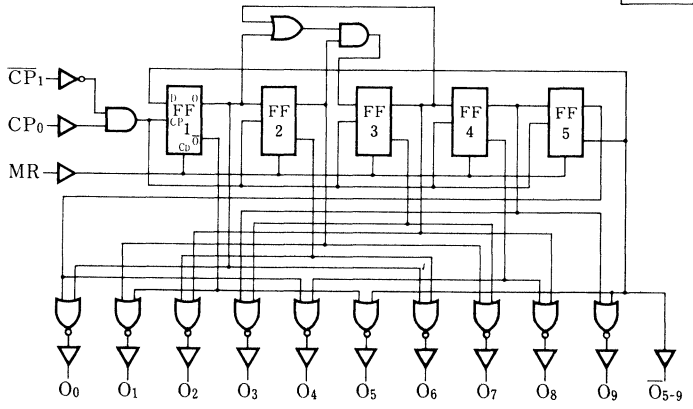
MR	CP_0	$\overline{CP}_1$	Mode
H	×	×	$O_0 = \overline{O}_{5-9} = H$, $O_1 \sim O_9 = L$
L	H	↘	Counter Advances
L	↗	L	
L	L	×	No Change
L	×	H	
L	H	↗	
L	↘	L	

Note) × : don't care

Pin Configuration



■ Logic Diagram



Pin Explanation

CP_0 : Positive clock input (↗)
$\overline{CP}_1$: Negative clock input (↘)
MR : Reset input
$O_0 \sim O_9$: Output (10 Bits)

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

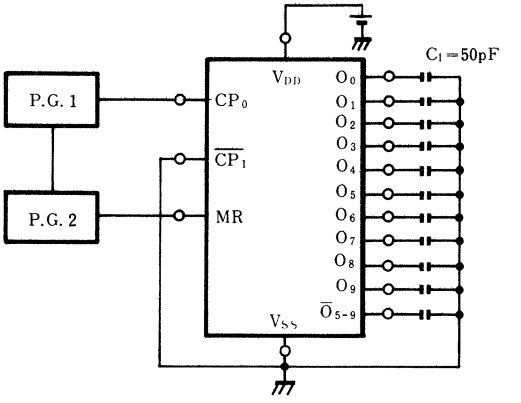
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

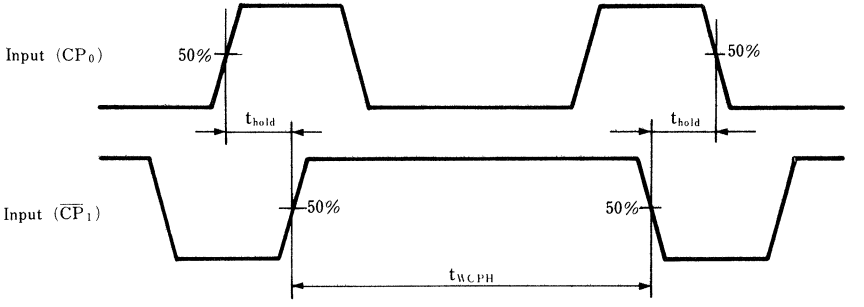
■ **Switching Characteristics** (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THI}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow O_0$ to O_9 (H→L)	5	t_{PHI}	—	195	585	ns
	10		—	75	225	
	15		—	50	150	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow O_0$ to O_9 (L→H)	5	t_{PLH}	—	245	735	ns
	10		—	95	285	
	15		—	60	180	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow \overline{O}_{5-9}$ (H→L)	5	t_{PHL}	—	245	735	ns
	10		—	90	270	
	15		—	60	180	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow \overline{O}_{5-9}$ (L→H)	5	t_{PLH}	—	190	570	ns
	10		—	75	225	
	15		—	50	150	
Propagation Delay Time MR→O_1 to O_9 (H→L)	5	t_{PHL}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time MR→$\overline{O}_{5-9}$ (L→H)	5	t_{PLH}	—	110	330	ns
	10		—	45	135	
	15		—	35	105	
Propagation Delay Time MR→O_0 (L→H)	5	t_{PLH}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Hold Time $CP_0 \rightarrow \overline{CP}_1$	5	t_{hold}	—	70	210	ns
	10		—	25	75	
	15		—	15	45	
Hold Time $\overline{CP}_1 \rightarrow CP_0$	5	t_{hold}	—	85	255	ns
	10		—	30	90	
	15		—	20	60	
Minimum Clock Pulse Width	5	t_{WCP}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Minimum Reset Pulse Width	5	t_{WMRH}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Reset Recovery Time	5	t_{RMR}	—	25	75	ns
	10		—	10	40	
	15		—	10	30	
Maximum Clock Frequency	5	f_{max}	3	6	—	ns
	10		8	16	—	
	15		12	24	—	
Input Capacitance		C_I	—	—	7.5	pF

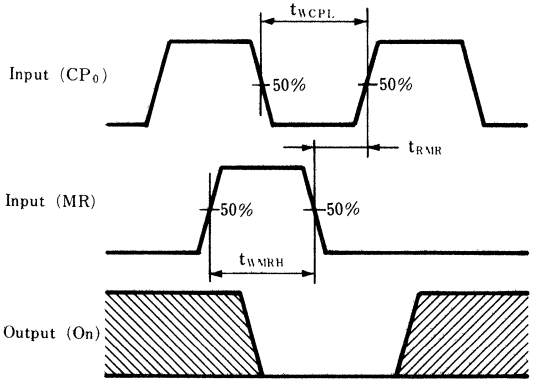
1. Switching Time Test Circuit



2. Waveforms

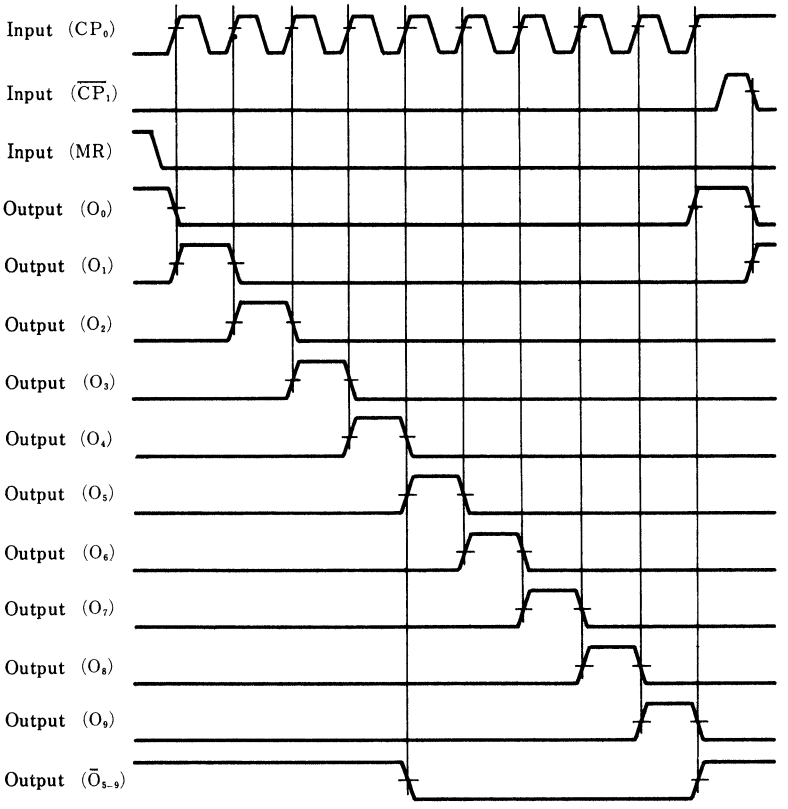


Waveforms showing hold times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0
Hold times are shown as positive values, but may be specified as negative values.



Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths
Conditions: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW to HIGH transition; t_{WCP} and t_{RMR} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH to LOW transition.

■ Timing Diagram



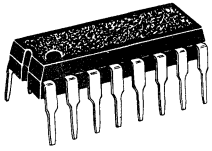
MN4018B/MN4018BS

Presettable Divide-by-N Counters

■ Description

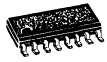
The MN4018B/S are presettable divide-by-N counters composed of a 5-bit Johnson counter.
Frequency is divided into 1/2, 1/4, 1/6, 1/8 and 1/10 by connecting the output of $\overline{O}_0 \sim \overline{O}_4$ to D input, and frequency is also divided into 1/3, 1/5, 1/7 and 1/9 by connecting the output of $\overline{O}_0 \sim \overline{O}_4$ to the D input through gate.
MR and PL are asynchronous. When MR = "H", $\overline{O}_0 \sim \overline{O}_4$ are all "H"; when PL = "H", On is contradiction of Pn.
Counter advances by one on the going edge of CP input. Proper counter sequence is given since the lock protection gate is available.
The MN4018B/S are equivalent to MOTOROLA MC14018B and RCA CD4018B.

P-3



16-Pin • Plastic DIL Package

P-4



16-Pin • Panaflat Package (SO-16D)

■ Truth Table

CP	MR	PL	$P_0 \sim P_4$	$\overline{O}_n$
↘	L	L	×	$\overline{O}_n$
↗	L	L	×	$\overline{D}_n$
×	L	H	L	H
×	L	H	H	L
×	H	×	×	H

Note) × : don't care

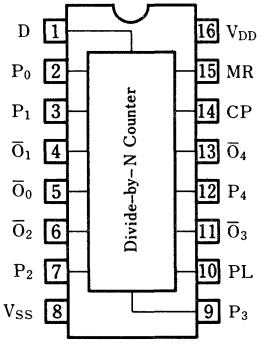
■ Functional Selection Table

Dividing number	Output to D	Remarks
10	$\overline{O}_4$	External connection is not necessary
8	$\overline{O}_3$	
6	$\overline{O}_2$	
4	$\overline{O}_1$	
2	$\overline{O}_0$	
9	$\overline{O}_3 \cdot \overline{O}_4$	External AND gate is necessary
7	$\overline{O}_2 \cdot \overline{O}_3$	
5	$\overline{O}_1 \cdot \overline{O}_2$	
3	$\overline{O}_0 \cdot \overline{O}_1$	

Pin Explanation

PL : Load input
$P_0 \sim P_4$: 4-bit input
D : Data input
CP : Clock input (↗)
MR : Reset input
$\overline{O}_0 \sim \overline{O}_4$: Output (4 bit)

Pin Configuration



■ Maximum Ratings (Ta=25℃)

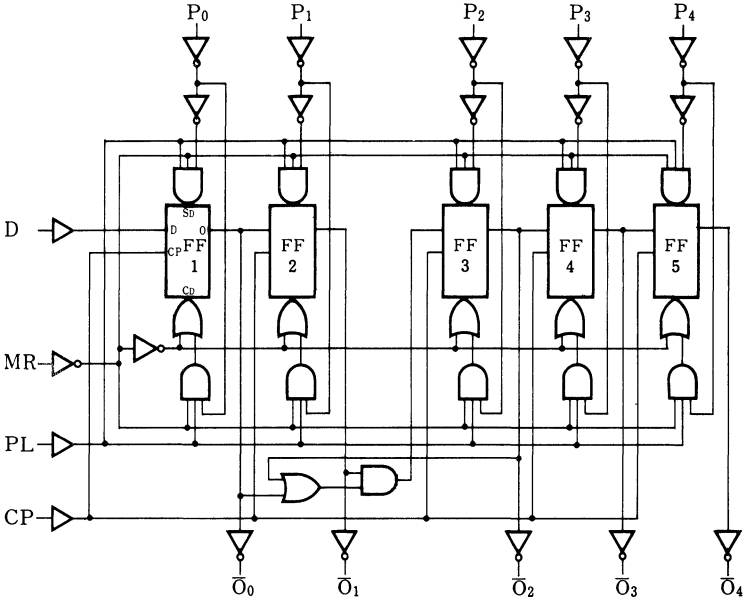
Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

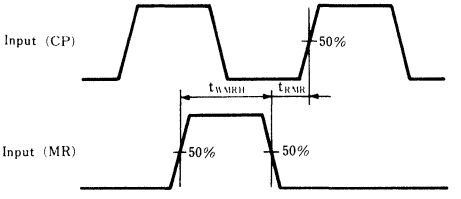
■ Logic Diagram



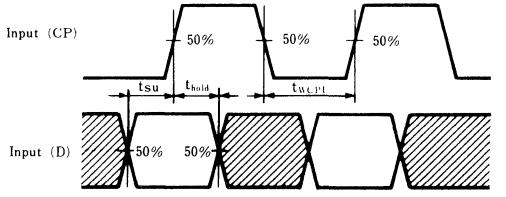
■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→$\overline{O}$ (H→L)	5	t_{PHL}	—	185	555	ns
	10		—	65	195	
	15		—	50	150	
Propagation Delay Time CP→$\overline{O}$ (L→H)	5	t_{PLH}	—	145	435	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time PL→$\overline{O}$ (H→L)	5	t_{PHL}	—	205	615	ns
	10		—	70	210	
	15		—	50	150	
Propagation Delay Time PL→$\overline{O}$ (L→H)	5	t_{PLH}	—	175	525	ns
	10		—	65	195	
	15		—	50	150	
Propagation Delay Time MR→$\overline{O}$ (L→H)	5	t_{PLH}	—	140	420	ns
	10		—	55	165	
	15		—	40	120	
Set-up Time D→CP	5	t_{su}	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
Hold Time D→CP	5	t_{hold}	—	−45	30	ns
	10		—	−15	10	
	15		—	−10	10	
Minimum Clock Pulse Width	5	t_{WCPL}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Minimum MR Pulse Width	5	t_{WMRH}	—	50	150	ns
	10		—	20	60	
	15		—	15	45	
Minimum PL Pulse Width	5	t_{WPLH}	—	75	225	ns
	10		—	25	75	
	15		—	20	60	
MR Recovery Time	5	t_{RMR}	—	70	210	ns
	10		—	20	60	
	15		—	15	45	
PL Recovery Time	5	t_{RPL}	—	85	255	ns
	10		—	30	90	
	15		—	20	60	
Maximum Clock Frequency	5	fmax	2	4	—	MHz
	10		6	11	—	
	15		8	16	—	
Input Capacitance		C_I	—	—	7.5	pF

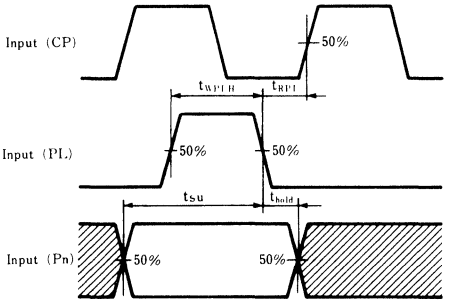
• Dynamic Signal Waveforms



Waveforms showing minimum MR pulse width and MR recovery time

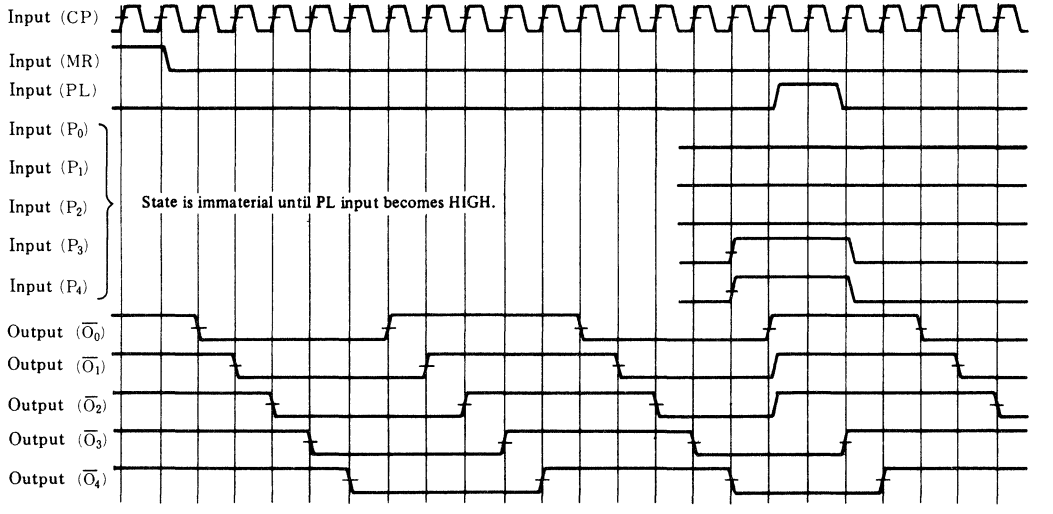


Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D



Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL; set-up and hold times are shown as positive values but may be specified as negative values.

■ Timing Diagram



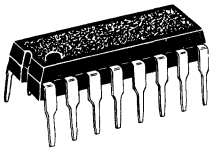
MN4019B/MN4019BS

Quad 2-Input Multiplexers

■ Description

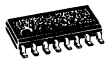
The MN4019B/S are quad 2-input multiplexers composed of two 2-input AND gates and OR gate with its two outputs.
The inputs applied to A and B are output to X selected by select input (S_A, S_B) common to 4 circuits.
These are equivalent to RCA CD4019B.

P-3



16-Pin • Plastic DIL Package

P-4



16-Pin • Panaflat Package (SO-16D)

■ Truth Table

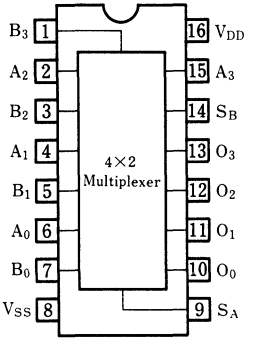
Select Input		Input		Output
S_A	S_B	A	B	O
L	L	×	×	L
H	L	L	×	L
H	L	H	×	H
L	H	×	L	L
L	H	×	H	H
H	H	H	×	H
H	H	×	H	H
H	H	L	L	L

Note) × : don't care

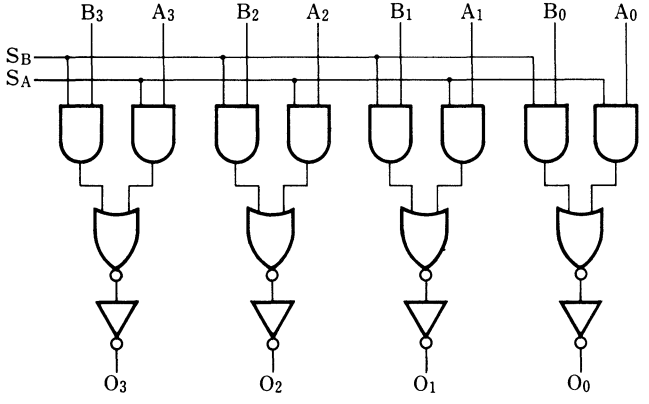
Pin Explanation

S_A, S_B : Select input
$A_0 \sim A_3$: Input
$B_0 \sim B_3$: Input
$O_0 \sim O_3$: Output

Pin Configuration



■ Logic Diagram



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

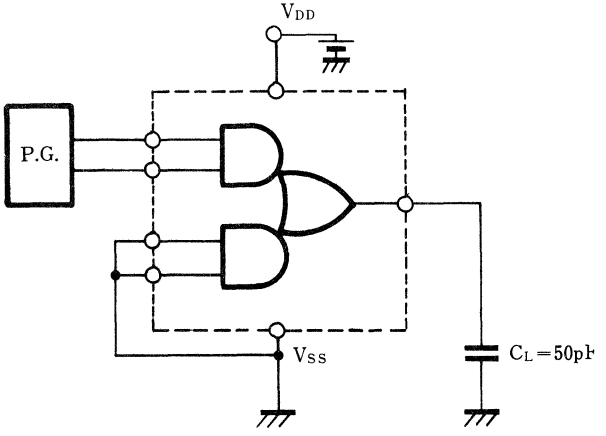
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		|I_O|<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		|I_O|<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	|I_O|<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	|I_O|<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

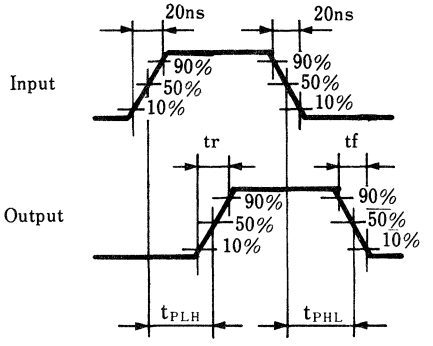
■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time (An, Bn, S_A, S_B—On)	5	t_{PLH}	—	60	180	ns
	10		—	25	75	
	15		—	15	45	
Propagation Delay Time (An, Bn, S_A, S_B—On)	5	t_{PHL}	—	70	210	ns
	10		—	30	90	
	15		—	25	75	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



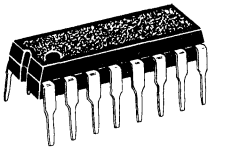
MN4020B / MN4020BS

14-Stage Binary Counters

■ Description

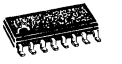
The MN4020B/S are binary counters in which an input-shaping circuit and 14-Stage flip-flops are built in.
Count is performed on the negative going edge of clock input.
The MN4020B/S are equivalent to MOTOROLA MC14020B and RCA CD4020B.

P- 3



16-Pin • Plastic DIL Package

P- 4



16-Pin • Panaflat Package (SO-16D)

■ Truth Table

$\overline{CP}$	MR	Mode
⌐‾	L	No Change
‾⌐	L	Counter Advance
×	H	$O_0 \sim O_{13}$ = All "L"

Note) × : don't care

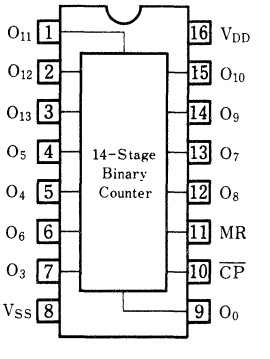
Pin Explanation

$\overline{CP}$: Negative clock input

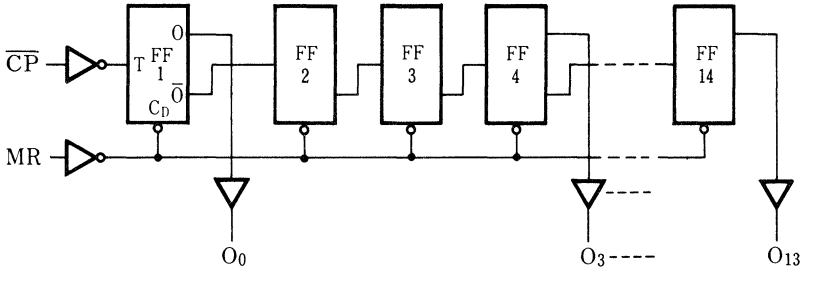
MR : Reset input

$O_0, O_3 \sim O_{13}$: Parallel output

Pin Configuration



■ Logic Diagram



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

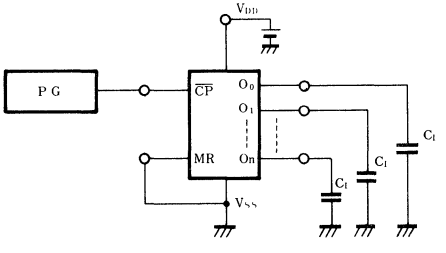
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		|I_O|<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		|I_O|<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	|I_O|<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	|I_O|<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

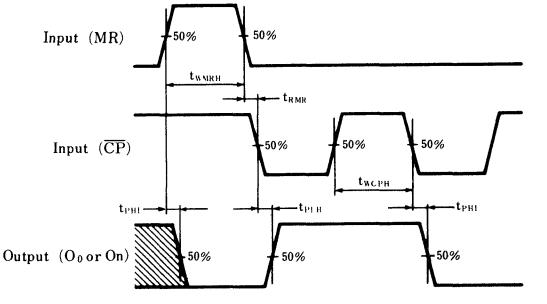
■ Switching Characteristics ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $\overline{CP}\rightarrow O_0$ (H→L)	5	t_{PHL}	—	105	315	ns
	10		—	45	135	
	15		—	30	90	
Propagation Delay Time $\overline{CP}\rightarrow O_0$ (L→H)	5	t_{PLH}	—	105	315	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time $On\rightarrow On_{+1}$ (H→L)	5	t_{PHL}	—	80	270	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $On\rightarrow On_{+1}$ (L→H)	5	t_{PLH}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time MR→On (H→L)	5	t_{PHL}	—	180	540	ns
	10		—	90	270	
	15		—	70	210	
Minimum Clock Pulse Width	5	t_{WCPH}	—	25	75	ns
	10		—	15	45	
	15		—	10	30	
Minimum MR Pulse Width	5	t_{WMRH}	—	65	195	ns
	10		—	50	150	
	15		—	45	135	
Reset Recovery Time	5	t_{RMR}	—	60	180	ns
	10		—	35	105	
	15		—	25	75	
Maximum Clock Frequency	5	fmax	5	10	—	MHz
	10		13	25	—	
	15		18	35	—	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit

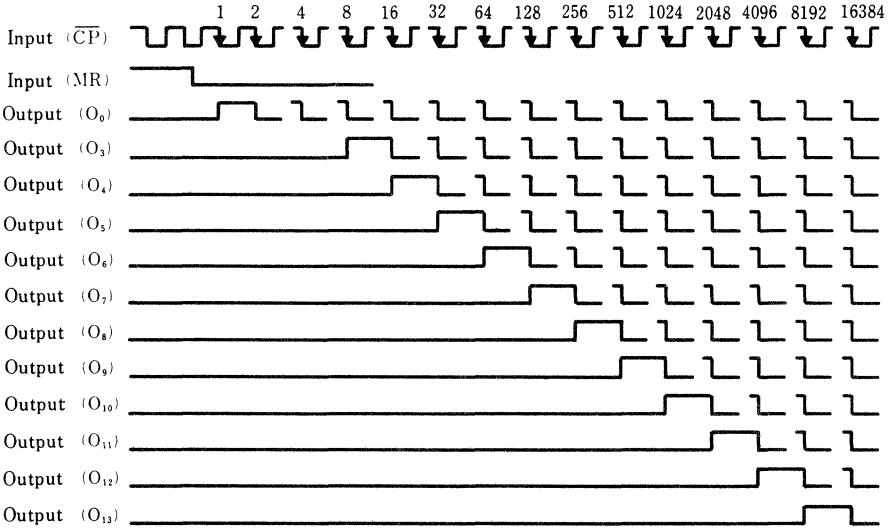


2. Waveforms



Waveforms showing propagation delays for MR to O_n and $\overline{CP}$ to O_0, minimum MR and $\overline{CP}$ pulse widths

Timing Diagram



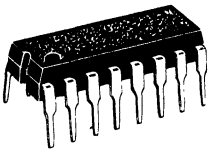
MN4021B/MN4021BS

8-Bit Static Shift Registers

■ Description

The MN4021B/S are 8-bit static shift registers composed of 8 register cells with its own parallel input.
Parallel input/series output and parallel input-series output conversion are enabled on the clock synchronization by controlling parallel/series control input (PL).

P-3



16-Pin • Plastic DIL Package

P-4

16-Pin • Panaflat Package (SO-16D)

■ Truth Table

Serial Action

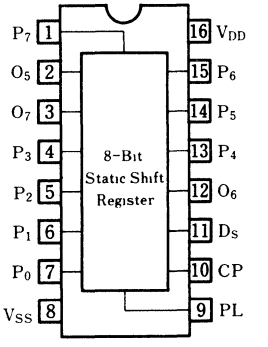
	Input			Output		
n	CP	Ds	PL	O_5	O_6	O_7
1	↑	D_1	L	×	×	×
2	↑	D_2	L	×	×	×
3	↑	D_3	L	×	×	×
6	↑	×	L	D_1	×	×
7	↑	×	L	D_2	D_1	×
8	↑	×	L	D_3	D_2	D_1
	↓	×	L	no change		

Parallel Action

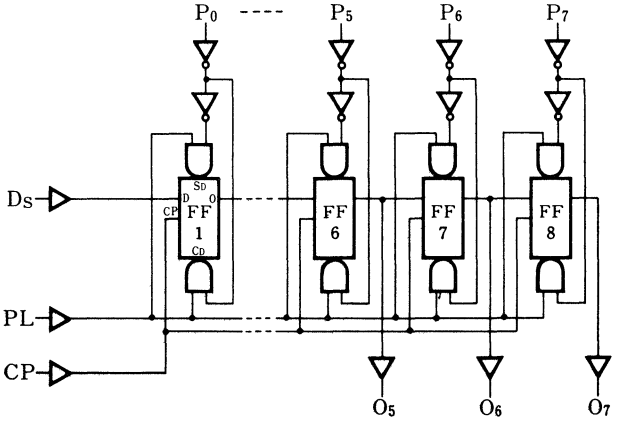
	Input			Output		
n	CP	Ds	PL	O_5	O_6	O_7
	×	×	H	P_5	P_6	P_7

Note) × : don't care
D_n : H or L
n : Clock pulse number

Pin Configuration



■ Logic Diagram



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

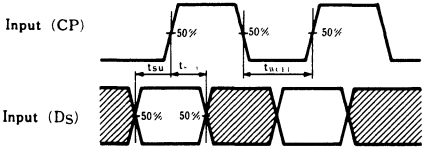
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	

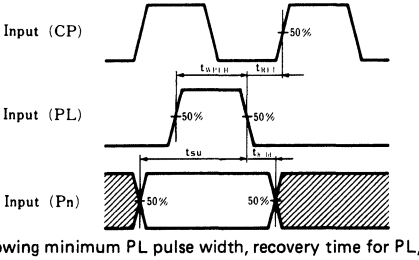
■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$) (Continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	170	510	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time PL→On (H→L)	5	t_{PHL}	—	240	720	ns
	10		—	90	270	
	15		—	60	180	
Propagation Delay Time PL→On (L→H)	5	t_{PLH}	—	175	525	ns
	10		—	70	210	
	15		—	50	150	
Set-up Time Ds→CP	5	t_{su}	—	45	135	ns
	10		—	15	45	
	15		—	10	30	
Set-up Time Pn→PL	5	t_{su}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Hold Time Ds→CP	5	t_{hold}	—	20	60	ns
	10		—	10	30	
	15		—	8	24	
Hold Time Pn→PL	5	t_{hold}	—	−10	24	ns
	10		—	0	24	
	15		—	0	24	
Minimum Clock Pulse Width	5	t_{WCPL}	—	55	165	ns
	10		—	20	60	
	15		—	15	45	
Minimum PL Pulse Width	5	t_{WPLH}	—	75	225	ns
	10		—	25	75	
	15		—	20	60	
PL Recovery Time	5	t_{RPL}	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
Maximum Clock Frequency	5	fmax	4	9	—	MHz
	10		12	25	—	
	15		18	37	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D_S



Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL; set-up and hold times are shown as positive values but may be specified as negative values.

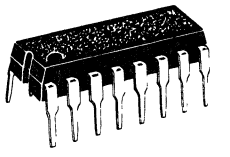
MN4022B / MN4022BS

4-Stage Divide-by-8 Johnson Counters

■ Description

The MN4022B/S are octal Johnson counters constructed with 4-stage D-type flip-flops.
The built-in decoder converts output to the coal number.
One output of 8 outputs ($O_0 \sim O_7$) becomes "H" by the count pulse added to CP_0 and $\overline{CP}_1$.
Count advances the count on the positive going edge of CP_0 at" $\overline{CP}_1$ = "L" or on the negative going edge of $\overline{CP}_1$ at CP_0 = "H".
MR input of the "H" level resets counter to O_0 = "H" and $O_1 \sim O_7$ = "L" regardless of CP_0 and $\overline{CP}_1$.
The MN4022B/S are equivalent to MOTOROLA MC14022B and RCA CD4022B.

P- 3



16-Pin • Plastic DIL Package

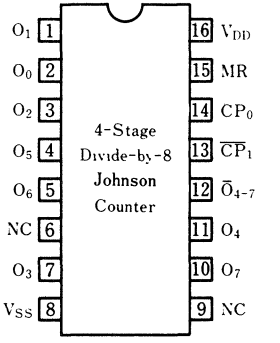
P- 4

16-Pin • Panaflat Package (SO-16D)

■ Truth Table

MR	CP_0	$\overline{CP}_1$	Mode
H	×	×	$O_0=\overline{O}_{4\text{-}7}=H$, $O_1 \sim O_7=L$
L	H	↘	Counter Advance
L	↗	L	
L	L	×	No Change
L	×	H	
L	H	↗	
L	↘	L	

Pin Configuration



■ Maximum Ratings (Ta=25℃)

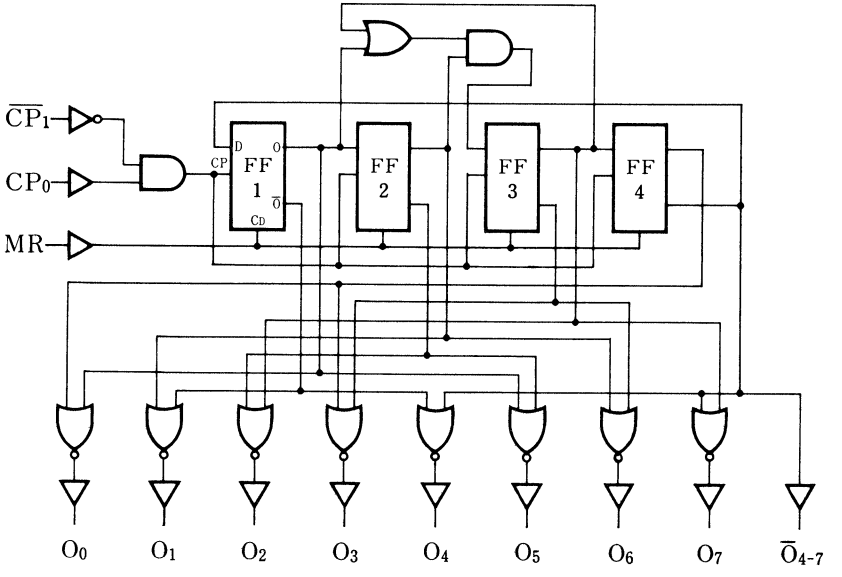
Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

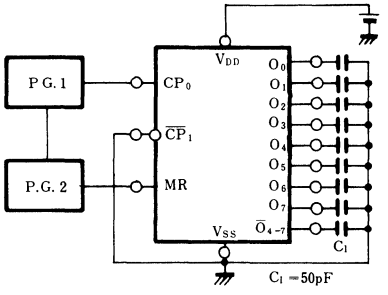
■ Logic Diagram



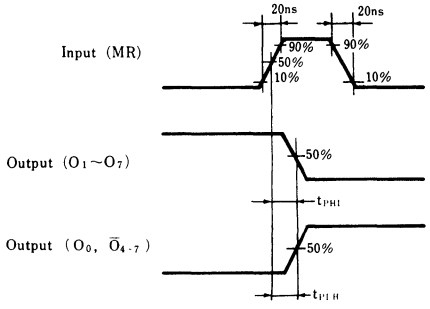
■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

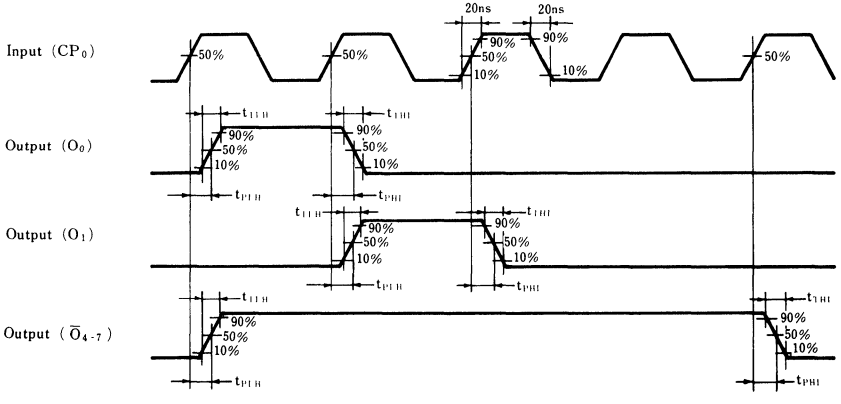
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow On$ (H→L)	5	t_{PHL}	—	195	585	ns
	10		—	75	225	
	15		—	50	150	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow On$ (L→H)	5	t_{PLH}	—	245	735	ns
	10		—	95	285	
	15		—	60	180	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow \overline{O}_{4-7}$ (H→L)	5	t_{PHL}	—	245	735	ns
	10		—	90	270	
	15		—	60	180	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow \overline{O}_{4-7}$ (L→H)	5	t_{PLH}	—	190	570	ns
	10		—	75	225	
	15		—	50	150	
Propagation Delay Time $MR \rightarrow O_1$ to O_7 (H→L)	5	t_{PHL}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time $MR \rightarrow O_0$ (L→H)	5	t_{PLH}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time $MR \rightarrow \overline{O}_{4-7}$ (L→H)	5	t_{PLH}	—	110	330	ns
	10		—	45	135	
	15		—	35	105	
Hold Time $CP_0 \rightarrow \overline{CP}_1$	5	t_{hold}	—	70	210	ns
	10		—	25	75	
	15		—	15	45	
Hold Time $\overline{CP}_1 \rightarrow CP_0$	5	t_{hold}	—	85	255	ns
	10		—	30	90	
	15		—	20	60	
Minimum Clock Pulse Width	5	t_{WCP}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Minimum Reset Pulse Width	5	t_{WMRH}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Reset Recovery Time	5	t_{RMR}	—	10	30	ns
	10		—	5	15	
	15		—	5	15	
Maximum Clock Frequency	5	fmax	3	6	—	ns
	10		8	16	—	
	15		12	24	—	
Input Capacitance		C_I	—	—	7.5	pF

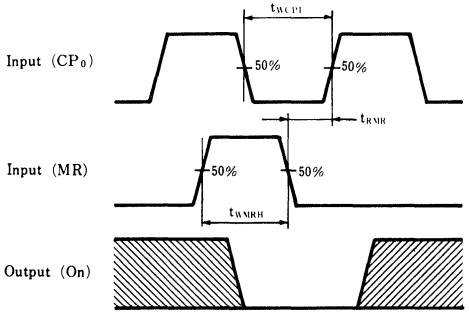
1. Switching Time Test Circuit



2. Waveforms



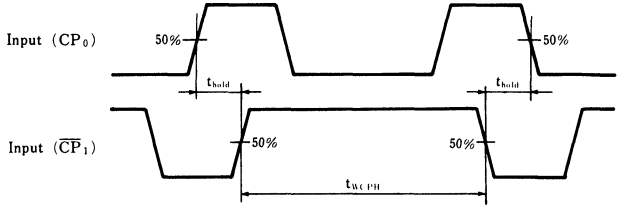




Waveforms showing recovery time for MR, minimum CP_0 and MR pulse widths

Conditions: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW to HIGH transition.

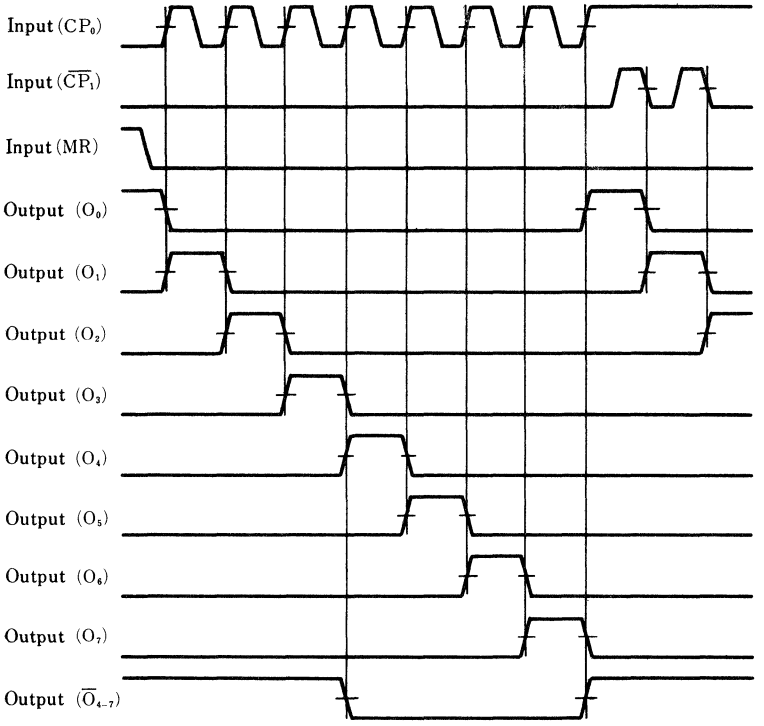
t_{WCP} and t_{RMR} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH to LOW transition



Waveforms showing hold times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0

Hold times are shown as positive values, but may be specified as negative values.

Timing Diagram



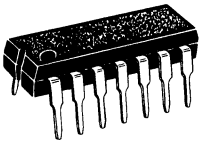
MN4023B / MN4023BS

Triple 3-Input NAND Gates

■ Description

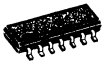
The MN4023B/S are positive 3-input NAND gates and have 3 circuits in a package.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
The MN4023B/S are equivalent to MOTOROLA MC14023B and RCA CD4023B.

P-1



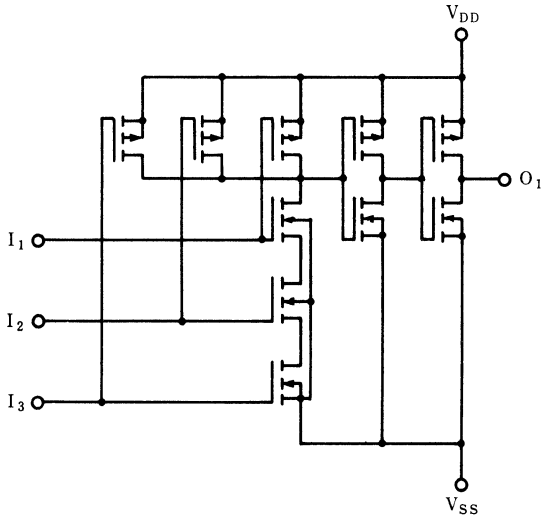
14-Pin • Plastic DIL Package

P-2

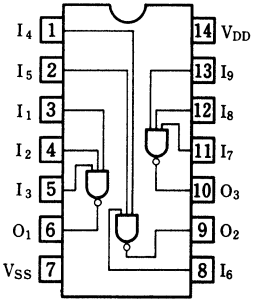


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/3)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

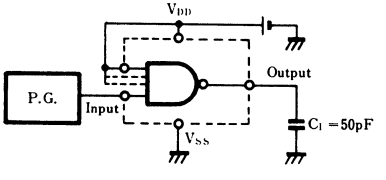
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

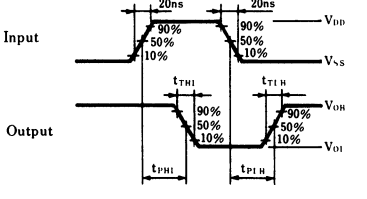
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	65	195	ns
	10		—	30	90	
	15		—	25	75	
Propagation Delay Time	5	t_{PHL}	—	65	195	ns
	10		—	25	75	
	15		—	15	45	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



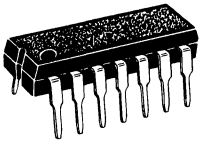
MN4024B / MN4024BS

7-Stage Binary Counters

■ Description

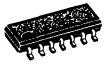
The MN4024B/S are 7-stage binary ripple counters composed of master-slave flip-flops.
The counter advances on the negative going edge of the clock input. A High on the reset input (MR) clears all flip-flops and forces all outputs (O_0 ~ O_6) Low, independent of the clock input.
The MN4024B/S are equivalent to MOTOROLA MC14024B and RCA CD4024B.

P-1



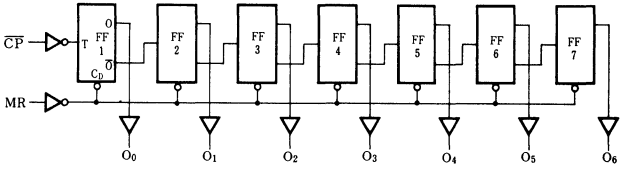
14-Pin • Plastic DIL Package

P-2

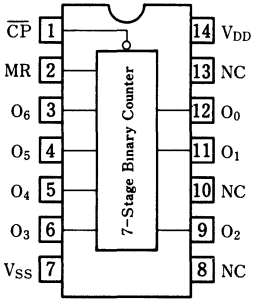


14-Pin • Panaflat Package (SO-14D)

■ Logic Diagram



Pin Configuration



Pin Explanation

$\overline{CP}$: Clock input (⌝⌞)
MR : Reset input
O_0~O_6 : Output (7 Bits)

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

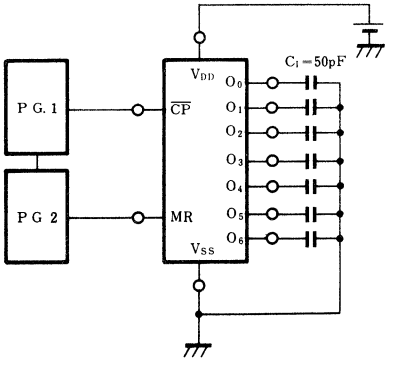
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $\overline{CP}$→O_0 (L→H)	5	t_{PLH}	—	105	315	ns
	10		—	45	135	
	15		—	30	90	
Propagation Delay Time $\overline{CP}$→O_0 (H→L)	5	t_{PHL}	—	100	300	ns
	10		—	40	120	
	15		—	25	75	
Propagation Delay Time O_n→O_{n+1} (L→H)	5	t_{PLH}	—	50	150	ns
	10		—	25	75	
	15		—	15	45	
Propagation Delay Time O_n→O_{n+1} (H→L)	5	t_{PHL}	—	60	180	ns
	10		—	25	75	
	15		—	20	60	

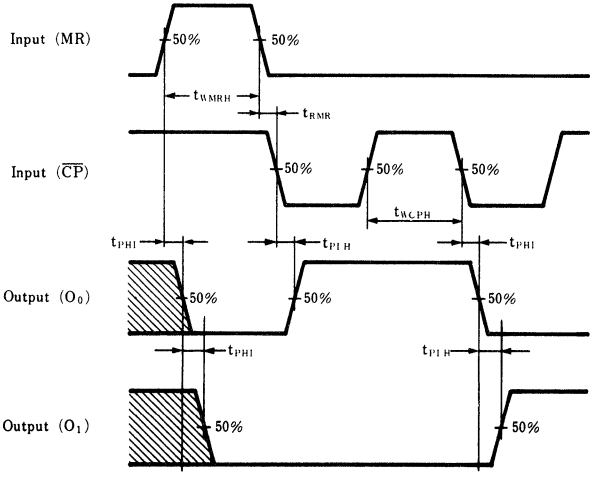
■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$) (Continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Propagation Delay Time MR→On (H→L)	5	t_{PHI}	—	120	360	ns
	10		—	45	135	
	15		—	30	90	
Minimum Clock Pulse Width	5	t_{WCPH}	—	30	90	ns
	10		—	15	45	
	15		—	10	30	
Minimum Reset Pulse Width	5	t_{WMRH}	—	40	120	ns
	10		—	20	60	
	15		—	15	45	
Reset Recovery Time	5	t_{RMR}	—	10	30	ns
	10		—	5	20	
	15		—	5	20	
Maximum Clock Frequency	5	fmax	5	10	—	ns
	10		13	25	—	
	15		18	35	—	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



Waveforms showing propagation delays for MR to O_n and $\overline{CP}$ to O_0, minimum MR and $\overline{CP}$ pulse widths and recovery time for MR

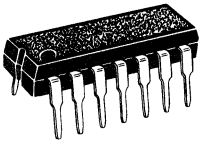
MN4025B / MN4025BS

Triple 3-Input NOR Gates

■ Description

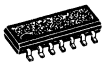
The MN4025B/S are positive 3-input NOR gates and have 3 circuits in a package.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increase of load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
The MN4025B/S are equivalent to MOTOROLA MC14025B and RCA CD4025B.

P-1



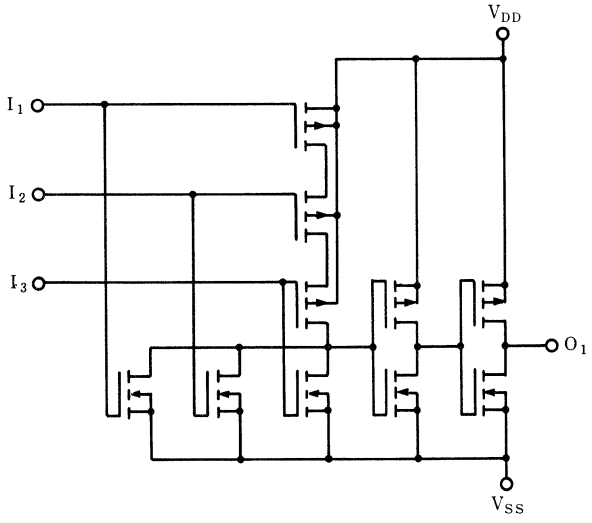
14-Pin • Plastic DIL Package

P-2

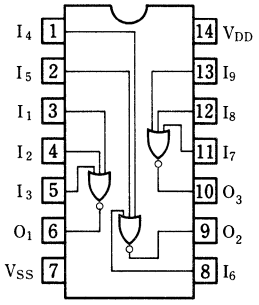


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/3)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

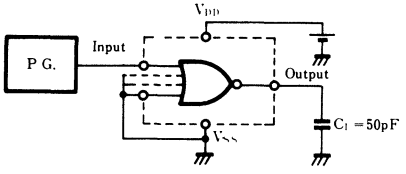
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		| I_O | <1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		| I_O | <1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

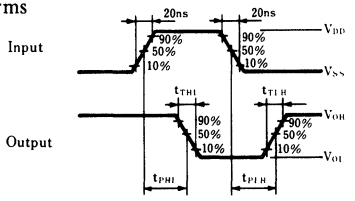
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	60	180	ns
	10		—	25	75	
	15		—	15	45	
Propagation Delay Time	5	t_{PHL}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



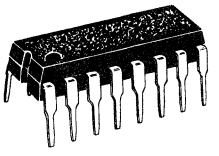
MN4027B / MN4027BS

Dual J-K Flip-Flops

■ Description

The MN4027B/S are dual J-K flip-flops. Each flip-flop has independent J, K, set, clear and clock inputs and complementary outputs (0, $\overline{0}$).
For the J-K mode, both logic levels of clear and set are Low and the information is transferred to the output on the positive going edge of the clock pulse according to the state of J and K.
These are equivalent to MOTOROLA MC14027B and RCA CD4027B.

P- 3



16-Pin • Plastic DIL Package

P- 4

16-Pin • Panaflat Package (SO-16D)

■ Truth Table

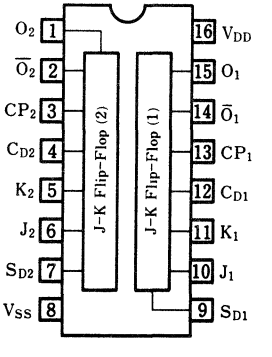
Input					Output	
S_D	C_D	CP	J	K	O_{n+1}	$\overline{O}_{n+1}$
L	L	↑	L	L	no change	
L	L	↑	H	L	H	L
L	L	↑	L	H	L	H
L	L	↑	H	H	$\overline{O}_n$	O_n
H	L	×	×	×	H	L
L	H	×	×	×	L	H
H	H	×	×	×	H	H
L	L	↓	×	×	no change	

Note) × : don't care

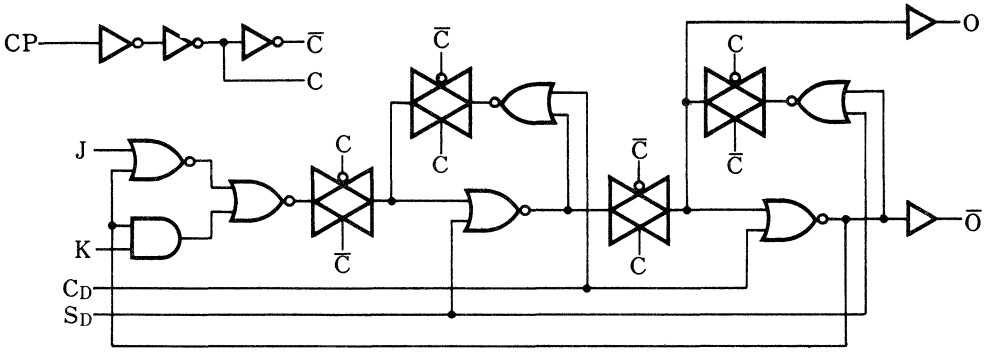
Pin Explanation

J, K : Synchronous input
CP : Clock input (↑)
S_D : Asynchronous set direct input
C_D : Asynchronous clear direct input
O, $\overline{O}$: Output

Pin Configuration



■ Logic Diagram (1/2)



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	4	—	4	—	30	μA
	10				—	8	—	8	—	60	
	15				—	16	—	16	—	120	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OI}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ Switching Characteristics ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

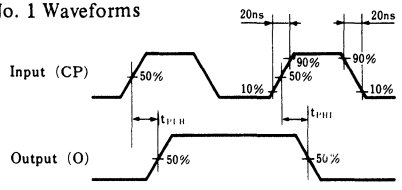
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time (CP→O, $\overline{O}$) (H→L)	5	t_{PLH}	—	115	345	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time (CP→O, $\overline{O}$) (L→H)	5	t_{PHL}	—	115	345	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time (S_D→O)	5	t_{PLH}	—	75	225	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time (C_D→O)	5	t_{PHL}	—	130	390	ns
	10		—	50	150	
	15		—	35	105	
Minimum Set-up Time (J, K→CP)	5	tsu	—	50	150	ns
	10		—	15	45	
	15		—	10	30	
Minimum Clear Pulse Width Minimum Preset Pulse Width	5	t_{WSDH} t_{WCDH}	—	40	120	ns
	10		—	20	60	
	15		—	15	45	
Maximum Clock Frequency	5	fmax	3	6	—	MHz
	10		7	15	—	
	15		11	22	—	
Input Capacitance		C_I	—	—	7.5	pF

• Switching Time Test Circuit

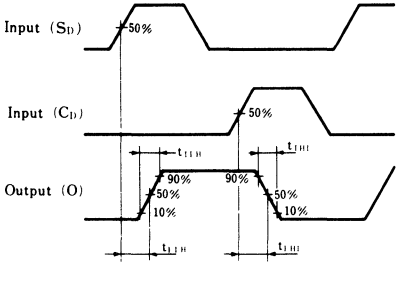
Test No.	J	K	C_D	S_D	CP
1	H	H	L	L	P.G.1
2	H	H	P.G. 1	P.G. 2	H
3	P.G. 1	P.G. 1	L	L	P.G. 2

Note: P.G. = Pulse Generator

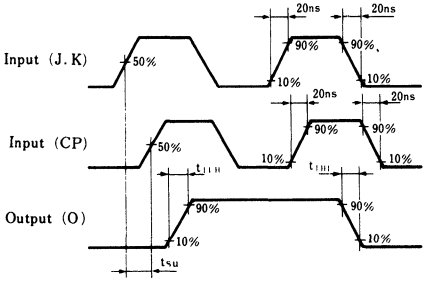
Test No. 1 Waveforms



Test No. 2 Waveforms



Test No. 3 Waveforms



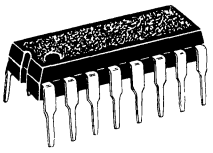
MN4028B / MN4028BS

BCD-to-Decimal / Binary-to-Octal Decoders

■ Description

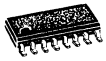
The MN4028B/S are 4-bit BCD-to-decimal decoders. A BCD code applied to inputs A_0 through A_2 causes the selected output ($O_0 \sim O_9$) to be High, the other nine remain Low.
This may be used as a 1-OF-8 decoder with active low enable input for A_3.
The MN4028B/S are equivalent to MOTOROLA MC14028B and RCA CD4028B.

P- 3



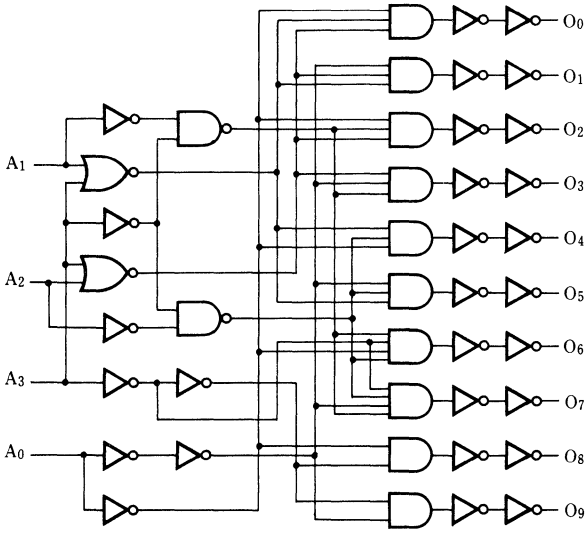
16-Pin • Plastic DIL Package

P- 4

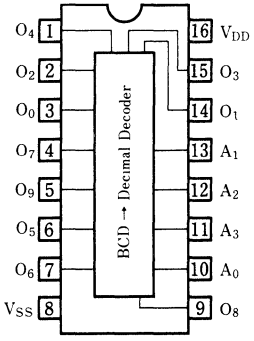


16-Pin • Panaflat Package (SO-16D)

■ Logic Diagram



Pin Configuration



Pin Explanation

$A_0 \sim A_3$: Output, 1-2-4-8BCD

$O_0 \sim O_9$: Address input

■ Truth Table

Input				Output									
A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9
L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	L	L	H	L	H	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L
L	H	L	H	L	L	L	L	L	H	L	L	L	L
L	H	H	L	L	L	L	L	L	L	H	L	L	L
L	H	H	H	L	L	L	L	L	L	L	H	L	L
H	L	L	L	L	L	L	L	L	L	L	L	H	L
H	L	L	H	L	L	L	L	L	L	L	L	L	H
H	L	H	L	L	L	L	L	L	L	L	L	H	L
H	L	H	H	L	L	L	L	L	L	L	L	L	H
H	H	L	L	L	L	L	L	L	L	L	L	H	L
H	H	L	H	L	L	L	L	L	L	L	L	L	H
H	H	H	L	L	L	L	L	L	L	L	L	H	L
H	H	H	H	L	L	L	L	L	L	L	L	L	H

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃		Ta=25℃		Ta=85℃		Unit
				min.	max.	min.	max.	min.	max.	
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	

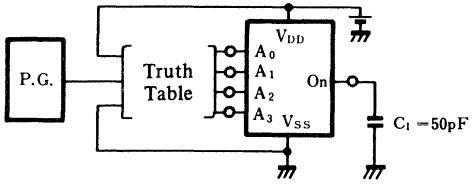
■ DC Characteristics (V_{SS}=0V) (continued)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Input Voltage Low Level	5	V_{IL}	$\|I_O\|<1\mu A$ V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|<1\mu A$ V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

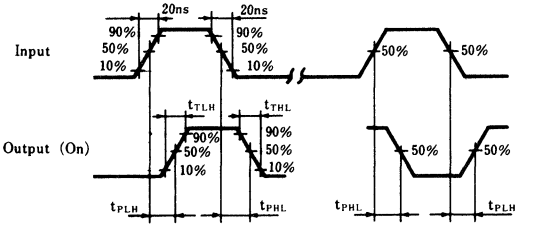
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	100	300	ns
	10		—	45	135	
	15		—	30	90	
Propagation Delay Time	5	t_{PHL}	—	110	330	ns
	10		—	50	150	
	15		—	35	105	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



(Positive) (Negative)

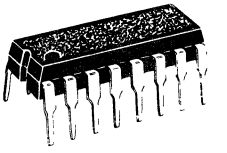
MN4029B / MN4029BS

4-Bit Presettable Up/Down Counters

■ Description

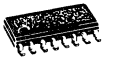
The MN4029B/S are synchronous up/down counters which can be used for either binary or decade counting.
An appropriate value of the counter is presettable by setting data inputs ($P_0 \sim P_3$) while the load input is High.
The counter advances on the positive going edge of the clock input when the $\overline{CE}$ and PL are Low.
The selection of binary or decade is determined by BIN/$\overline{DEC}$ input (High level is binary, Low level is decade) and Up or Down counter depends on UP/$\overline{DN}$ input (up at High level, down at Low level).
These are equivalent to MOTOROLA MC14029B and RCA CD4029B.

P-3



16-Pin • Plastic DIL Package

P-4

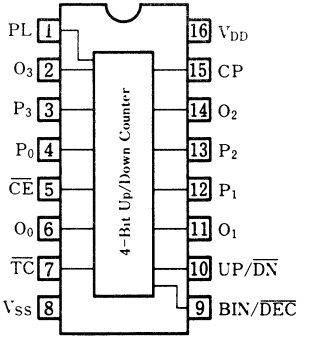


16-Pin • Panaflat Package (SO-16D)

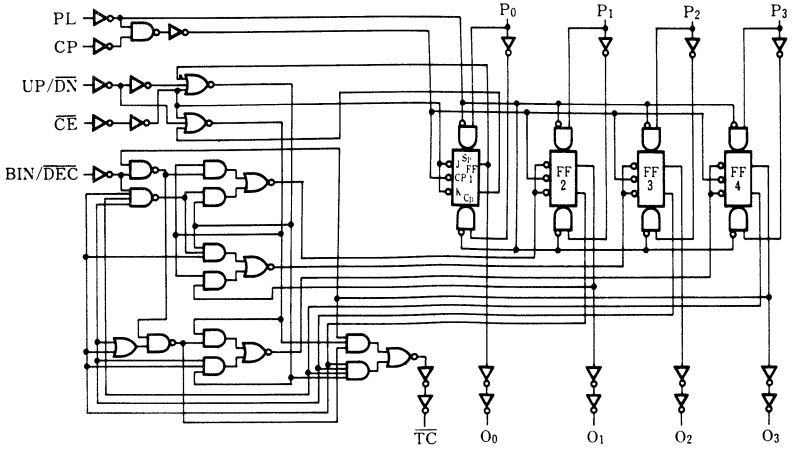
Pin Explanation

$P_0 \sim P_3$: Data input (4 Bits)
$O_0 \sim O_3$: Output (4 Bits)
CP : Clock input (⌐‾)
PL : Load input
$\overline{CE}$: Enable input
UP/$\overline{DN}$: Up/down input
BIN/$\overline{DEC}$: Binary/decade input

Pin Configuration



■ Logic Diagram



■ Truth Table

PL	BIN/$\overline{DEC}$	UP/$\overline{DN}$	$\overline{CE}$	CP	Mode
H	×	×	×	×	parallel load
L	×	×	H	×	no change
L	L	L	L	↓	count-down
L	L	H	L	↓	count-up
L	H	L	L	↓	count-down, binary
L	H	H	L	↓	count-up, binary

Note) × : don't care

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

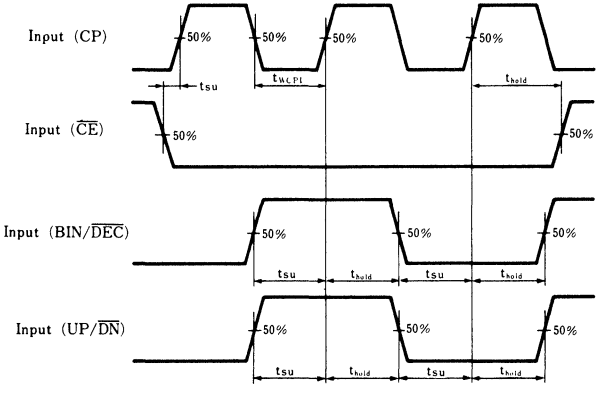
■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	145	435	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	160	480	ns
	10		—	60	180	
	15		—	40	120	
Propagation Delay Time CP→$\overline{TC}$ (H→L)	5	t_{PHL}	—	280	840	ns
	10		—	105	315	
	15		—	70	210	
Propagation Delay Time CP→$\overline{TC}$ (L→H)	5	t_{PLH}	—	195	585	ns
	10		—	75	225	
	15		—	55	165	
Propagation Delay Time PL→On (H→L)	5	t_{PHL}	—	120	360	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time PL→On (L→H)	5	t_{PLH}	—	170	510	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time $\overline{CE}$→$\overline{TC}$ (H→L)	5	t_{PHL}	—	180	540	ns
	10		—	70	210	
	15		—	50	150	
Propagation Delay Time $\overline{CE}$→$\overline{TC}$ (L→H)	5	t_{PLH}	—	170	510	ns
	10		—	65	195	
	15		—	50	150	
Minimum Clock Pulse Width	5	t_{WCPL}	—	55	165	ns
	10		—	20	60	
	15		—	15	45	
Minimum PL Pulse Width	5	t_{WPLH}	—	80	240	ns
	10		—	25	75	
	15		—	15	45	
PL Recovery Time	5	t_{RPL}	—	75	225	ns
	10		—	25	75	
	15		—	20	60	
Set-up Time BIN/$\overline{DEC}$→CP	5	tsu	—	135	405	ns
	10		—	45	135	
	15		—	30	90	
Set-up Time UP/$\overline{DN}$→CP	5	tsu	—	150	450	ns
	10		—	55	165	
	15		—	35	105	

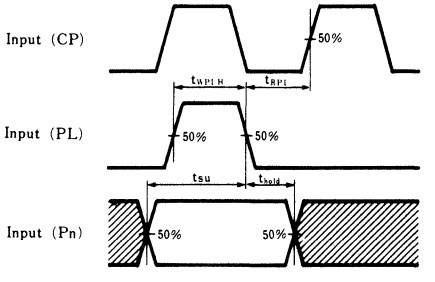
■ **Switching Characteristics** ($Ta = 25℃$, $V_{SS} = 0V$, $C_L = 50pF$) (continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Set-up Time $\overline{CE}$→CP	5	tsu	—	60	180	ns
	10		—	25	75	
	15		—	20	60	
Set-up Time Pn→PL	5	tsu	—	35	105	ns
	10		—	10	30	
	15		—	5	15	
Hold Time BIN/$\overline{DEC}$→CP	5	t_{hold}	—	− 90	45	ns
	10		—	− 30	15	
	15		—	− 20	10	
Hold Time UP/$\overline{DN}$→CP	5	t_{hold}	—	−135	15	ns
	10		—	− 50	0	
	15		—	− 35	−5	
Hold Time $\overline{CE}$→CP	5	t_{hold}	—	− 30	30	ns
	10		—	− 10	10	
	15		—	− 10	5	
Hold Time Pn→PL	5	t_{hold}	—	− 20	15	ns
	10		—	− 10	0	
	15		—	− 5	0	
Maximum Clock Frequency	5	fmax	4	8	—	MHz
	10		12	25	—	
	15		18	35	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms

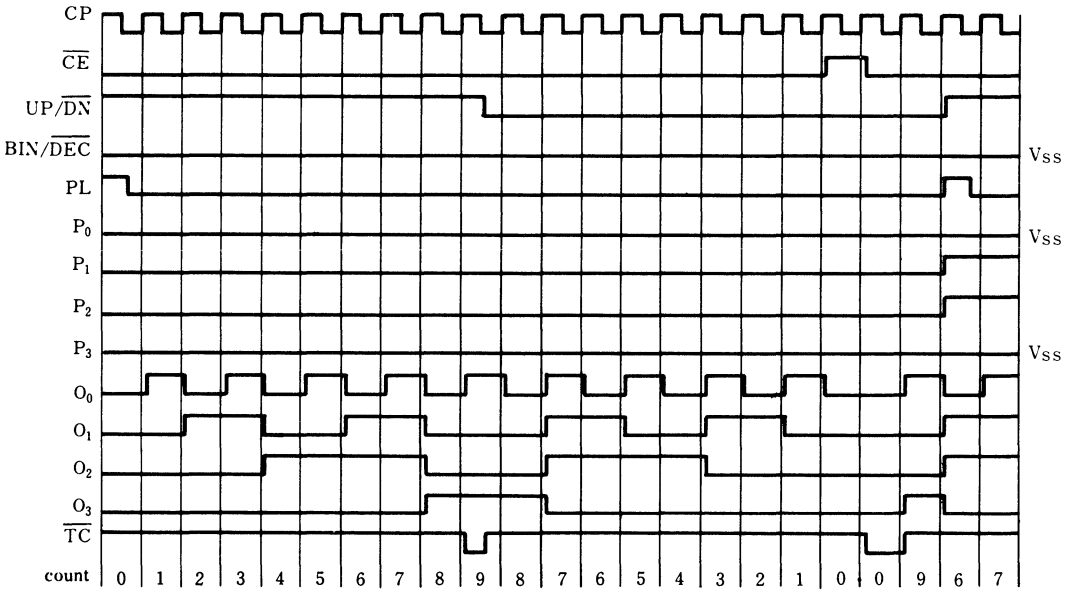


Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP, BIN/$\overline{DEC}$ to CP and UP/$\overline{DN}$ to CP. set up and hold times are shown as positive values but may be specified as negative values.

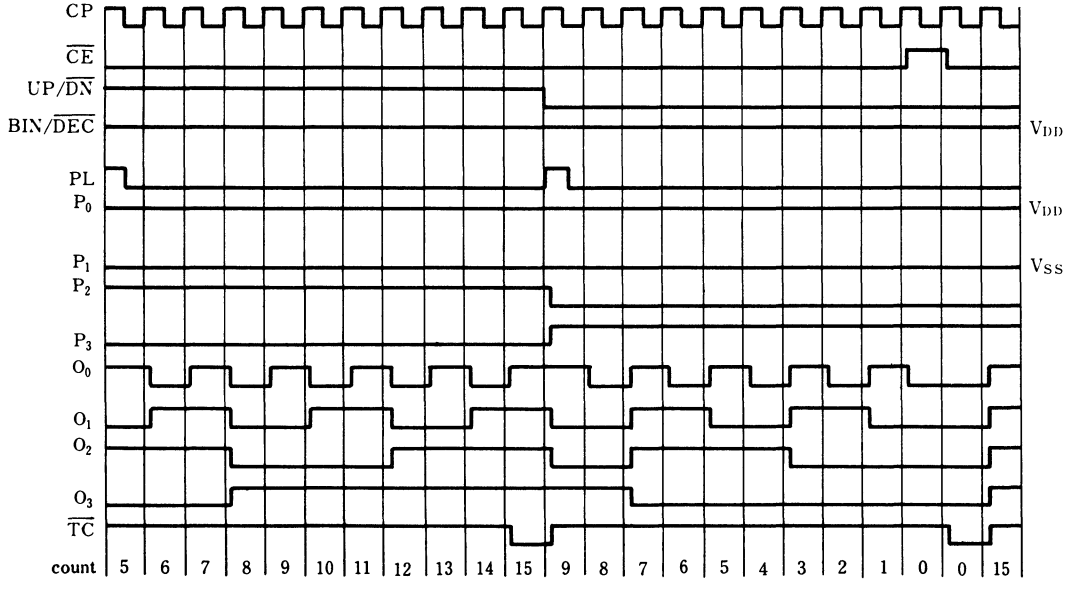


Waveforms showing minimum pulse width for PL, recovery time for PL, and set-up and hold times for P_n to PL, set up and hold times are shown as positive values but may be specified as negative values.

■ Timing Diagrams



Decade: (P_0=L, P_3=L, BIN/$\overline{DEC}$=L)



Binary: P_0=H, P_1=L, BIN/$\overline{DEC}$=H

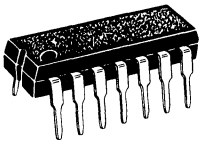
MN4030B/S, MN4070B/S

Quad Exclusive-OR Gates

■ Description

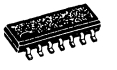
The MN4030B/S and MN4070B/S are EXCLUSIVE-OR gates and have 4 circuits in a package.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
Typical applications include digital comparators and parity checkers.
These are equivalent to MOTOROLA MC14070B and RCA CD4070B.

P-1



14-Pin • Plastic DIL Package

P-2

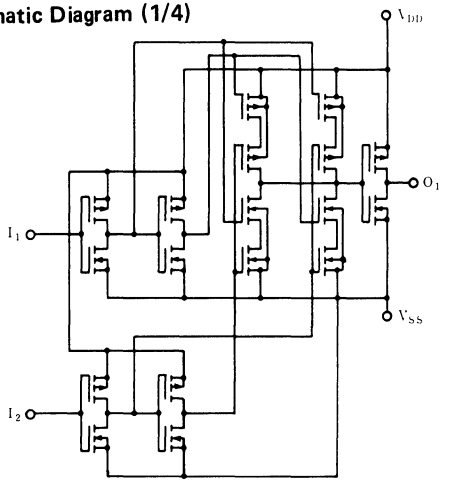


14-Pin • Panaflat Package (SO-14D)

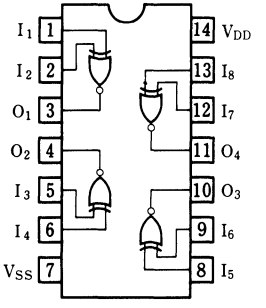
■ Truth Table

I_1	I_2	O_1
L	L	L
H	L	H
L	H	H
H	H	L

■ Schematic Diagram (1/4)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

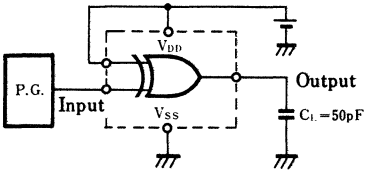
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

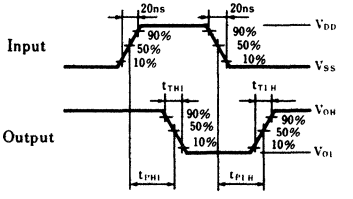
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	75	225	ns
	10		—	30	90	
	15		—	25	75	
Propagation Delay Time	5	t_{PHL}	—	85	255	ns
	10		—	35	105	
	15		—	30	90	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



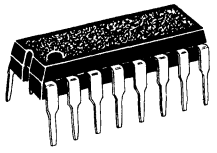
MN4035B / MN4035BS

4-Bit Universal Shift Registers

■ Description

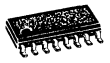
The MN4035B/S are edge-triggered 4-bit shift registers with both serial and parallel inputs.
Data is loaded into the register from parallel inputs when parallel enable is High or from serial JK inputs when it is Low and data is shifted one position on the positive going edge of the clock input.
The outputs are non-inverting when the T/$\overline{C}$ input is High and inverting when the T/$\overline{C}$ input is Low. A High on the MR input resets all registers, independent of any other input conditions.
These are equivalent to MC14035B and RCA CD4035B.

P-3



16-Pin • Plastic DIL Package

P-4



16-Pin • Panaflat Package (SO-16D)

■ Truth Table

Serial Action (First Stage)

Input				Output	Mode
CP	J	$\overline{K}$	MR	O_0	
↑	H	H	L	H	D flip-flop
↑	L	L	L	L	
↑	H	L	L	$\overline{O_0}$	toggle
↑	L	H	L	O_0	no change
×	×	×	H	L	reset

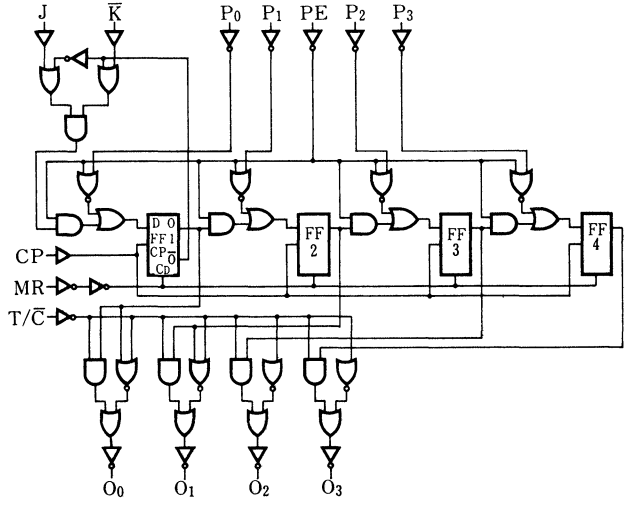
Note) T/C = H, PE = L

Parallel Action

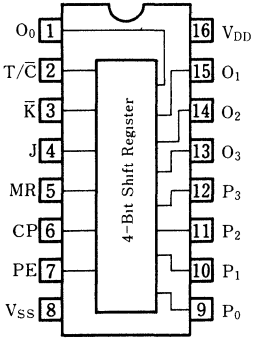
CP	Input				Output			
	P_0	P_1	P_2	P_3	O_0	O_1	O_2	O_3
↑	H	H	H	H	H	H	H	H
↑	L	L	L	L	L	L	L	L

Note) T/$\overline{C}$ = H, RE = H, MR = L

■ Logic Diagram



Pin Configuration



Pin Explanation

$P_0 \sim P_3$: Data input
$O_0 \sim O_3$: Output
CP : Clock input
MR : Reset input
PE : Enable input

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

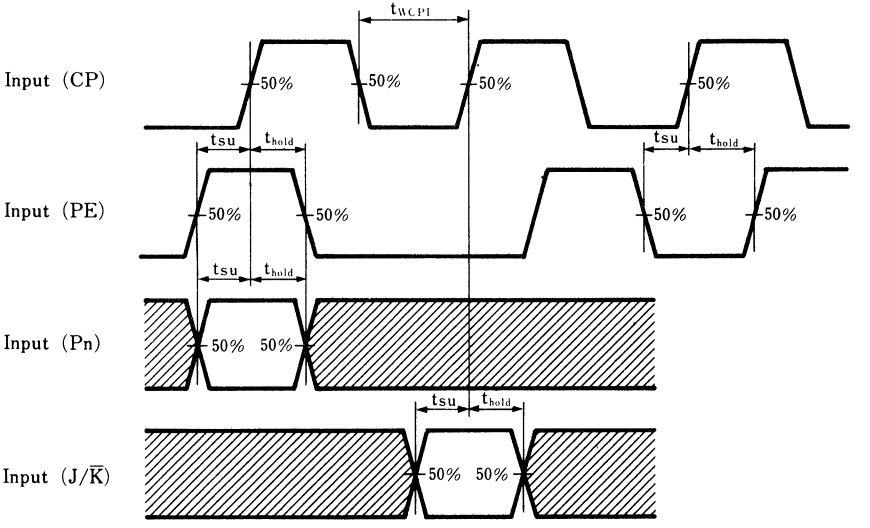
■ **Switching Characteristics** ($Ta = 25℃$, $V_{SS} = 0V$, $C_L = 50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	170	510	ns
	10		—	70	210	
	15		—	50	150	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	150	450	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time MR→On (H→L)	5	t_{PHL}	—	175	525	ns
	10		—	70	210	
	15		—	50	150	
Propagation Delay Time MR→On (L→H)	5	t_{PLH}	—	160	480	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time T/$\overline{C}$→On (H→L)	5	t_{PHL}	—	115	345	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time T/$\overline{C}$→On (L→H)	5	t_{PLH}	—	110	330	ns
	10		—	50	150	
	15		—	35	105	
Minimum Clock Pulse Width	5	t_{WCPL}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	
Minimum Reset Pulse Width	5	t_{WMRH}	—	30	90	ns
	10		—	15	45	
	15		—	10	30	
Reset Recovery Time	5	t_{RMR}	—	55	165	ns
	10		—	20	60	
	15		—	15	45	
Set-up Time Pn→CP	5	tsu	—	105	315	ns
	10		—	40	120	
	15		—	25	75	
Set-up Time PE→CP	5	tsu	—	100	300	ns
	10		—	40	120	
	15		—	25	75	
Set-up Time J, $\overline{K}$→CP	5	tsu	—	105	315	ns
	10		—	40	120	
	15		—	25	75	
Hold Time Pn→CP	5	t_{hold}	—	10	35	ns
	10		—	10	30	
	15		—	10	30	

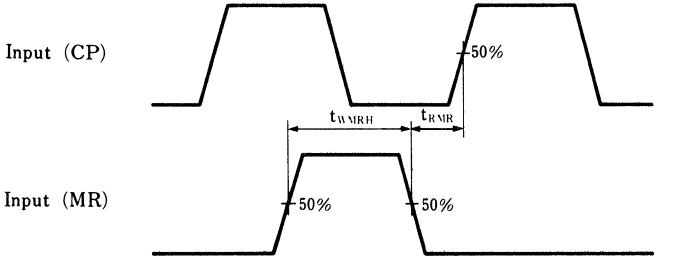
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Hold Time PE→CP	5	t_{hold}	—	−5	30	ns
	10		—	−5	20	
	15		—	−5	10	
Hold Time J, $\overline{K}$→CP	5	t_{hold}	—	−5	20	ns
	10		—	0	20	
	15		—	0	20	
Maximum Clock Frequency	5	fmax	5	10	—	MHz
	10		12	25	—	
	15		18	35	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



Waveforms showing minimum clock pulse width, set-up times, hold times. Set-up times and hold times are shown as positive values but may be specified as negative values.



Waveforms showing minimum MR pulse width and MR recovery time.

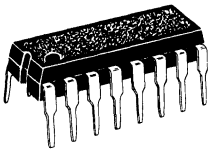
MN4040B / MN4040BS

12-Stage Binary Counters

■ Description

The MN4040B/S are 12-stage binary ripple counters with a clock input. The reset input and outputs are fully buffered. The counter advances on the negative going edge of the clock input.
A High on the MR input clears all counter stages and forces all outputs ($O_0 \sim O_{11}$) Low, independent of the clock input.
These are suitable for frequency dividers and center-control circuits, and are equivalent to MOTOROLA MC14040B and RCA CD4040B.

P-3

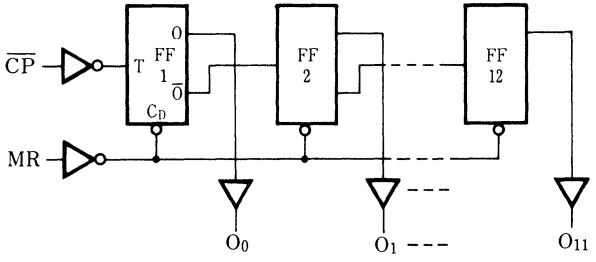


16-Pin • Plastic DIL Package

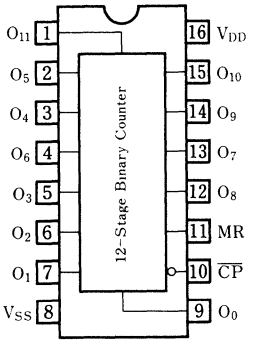
P-4

16-Pin • Panaflat Package (SO-16D)

■ Logic Diagram



Pin Configuration



Pin Explanation

$\overline{CP}$: Clock input (⌝)
MR : Reset input
$O_0 \sim O_{11}$: Output (12 Bits)

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

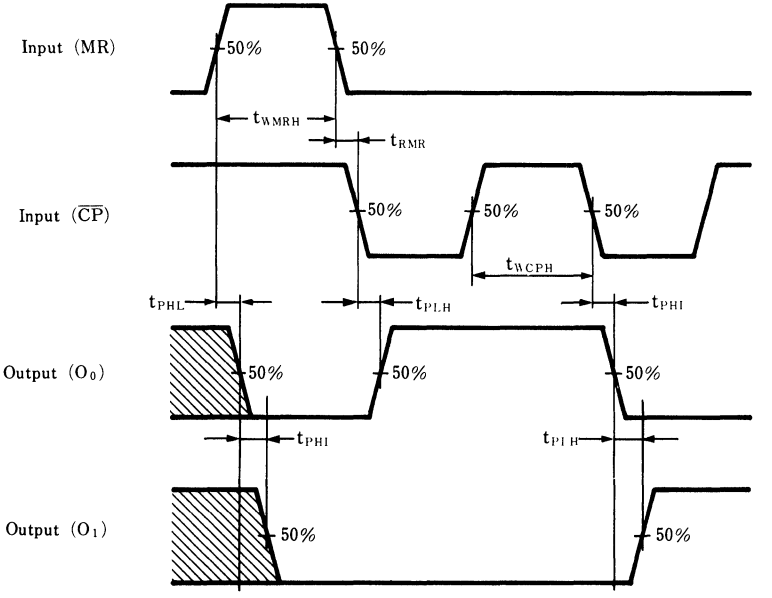
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $\overline{CP}$→O_0 (L→H)	5	t_{PLH}	—	105	315	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time $\overline{CP}$→O_0 (H→L)	5	t_{PHL}	—	105	315	ns
	10		—	45	135	
	15		—	30	90	
Propagation Delay Time O_n→O_{n+1} (L→H)	5	t_{PLH}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time O_n→O_{n+1} (H→L)	5	t_{PHL}	—	80	240	ns
	10		—	30	90	
	15		—	20	60	

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Propagation Delay Time MR→On (H→L)	5	t_{PHL}	—	180	540	ns
	10		—	90	270	
	15		—	70	210	
Minimum Clock Pulse Width	5	t_{WCPH}	—	25	75	ns
	10		—	15	45	
	15		—	10	30	
Minimum Reset Pulse Width	5	t_{WMRH}	—	65	195	ns
	10		—	50	150	
	15		—	45	135	
Reset Recovery Time	5	t_{RMR}	—	60	180	ns
	10		—	35	105	
	15		—	25	75	
Maximum Clock Frequency	5	fmax	5	10	—	MHz
	10		13	25	—	
	15		18	35	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



Waveforms showing propagation delays for MR to O_n and $\overline{CP}$ to O_0, minimum MR and $\overline{CP}$ pulse widths and recovery time for MR

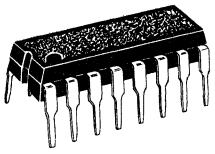
MN4042B / MN4042BS

Quad D Latches

■ Description

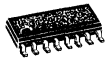
The MN4042B/S are quad D latches which have a common clock line and different data input terminals.
When the input (El) is "H" level, the output (O) shows the input (D) while input (E_0) is on the positive going edge; when the input (E_0) is on the negative going edge, output (O) maintains the input (D).
When the input (E_0) is on the negative going edge, the output (D) does not change even if input (D) changes.
When input (E_1) is at the "L" level, input (D) appears on the output (O) while input (E_0) is at the "L" level, and while input (E_0) is at the "H" level, Latch operates.
The MN4042B/S are equivalent to MOTOROLA MC14042B and RCA CD4042B.

P- 3



16-Pin • Plastic DIL Package

P- 4

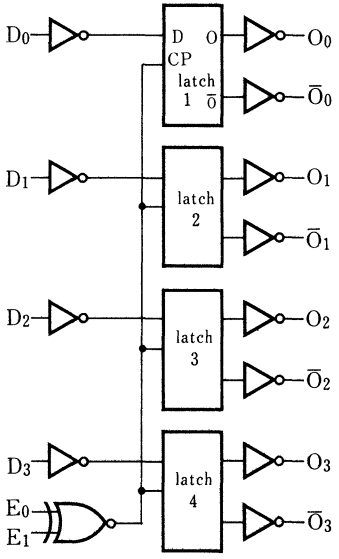


16-Pin • Panaflat Package (SO-16D)

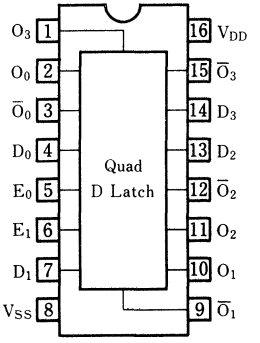
■ Tructh Table

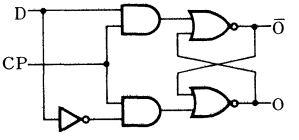
Input		Output
E_0	E_1	O
L	L	D
L	H	latch
H	L	latch
H	H	D

■ Logic Diagram



Pin Configuration





(One latch)

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

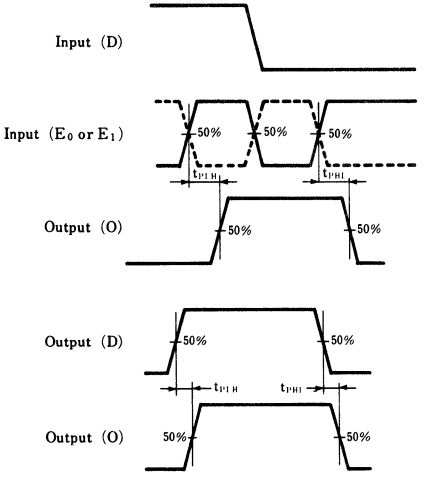
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	4	—	4	—	30	μA
	10				—	8	—	8	—	60	
	15				—	16	—	16	—	120	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O|<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O|<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O|<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O|<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

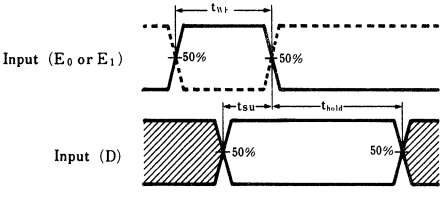
■ Switching Characteristics ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time D→O, $\overline{O}$ (H→L)	5	t_{PHL}	—	95	285	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time D→O, $\overline{O}$ (L→H)	5	t_{PLH}	—	85	255	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time E→O, $\overline{O}$ (H→L)	5	t_{PHL}	—	130	390	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time E→O, $\overline{O}$ (L→H)	5	t_{PLH}	—	120	360	ns
	10		—	50	150	
	15		—	35	105	
Minimum Enable Pulse Width	5	t_{WE}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	
Set-up Time D→E	5	tsu	—	10	30	ns
	10		—	5	20	
	15		—	5	20	
Hold Time D→E	5	t_{hold}	—	−5	15	ns
	10		—	0	15	
	15		—	0	15	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



Waveforms showing propagation delays for D to O, with latch enabled



Waveforms showing minimum enable pulse width, set-up time and hold time for E and D
Set-up and hold-times are shown as positive values but may be specified as negative values.

MN4043B / MN4043BS

Quad R/S Latches

■ Description

The MN4043B/S are latches composed of quad independent R/S flip-flop.
They are suitable for 4-bit data processing due to the combination of NOR gates.
Four outputs can be high impedance by the common input (EO) = L regardless of latch contents, and can easily be connected to the bus line.
The MN4043B/S are equivalent to MOTOROLA MC14043B and RCA CD4043B.

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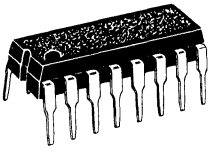


16-Pin • Plastic DIL Package

P- 4

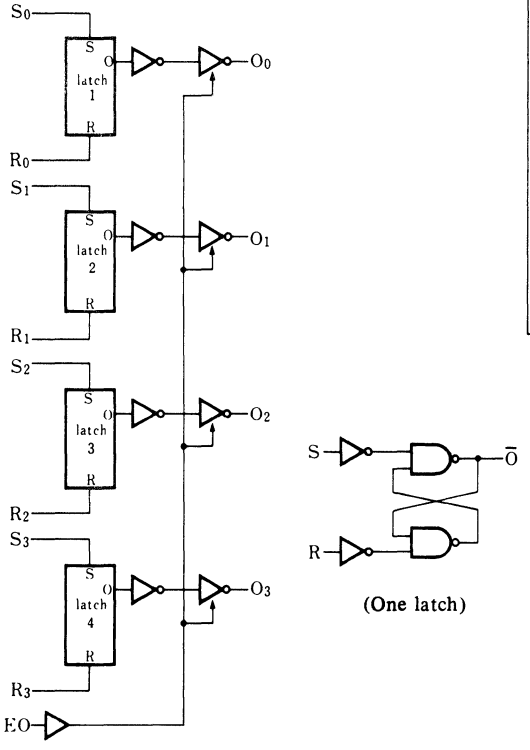
16-Pin • Panaflat Package (SO-16D)

■ Tructh Table

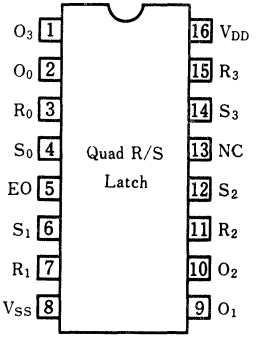
Input			Output
	S	R	O
L	×	×	Z
H	L	H	L
H	H	×	H
H	L	L	latch

Note) × : don't care
Z : high impedance

■ Logic Diagram



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

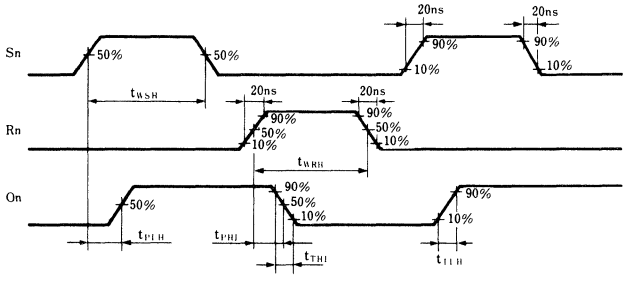
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Sym-bol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	4	—	4	—	30	μA
	10				—	8	—	8	—	60	
	15				—	16	—	16	—	120	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I= 0 or 5 V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I= 0 or15V		—	0.3	—	0.3	—	1	μA
3-State Output Pin: Leakage Current High Level	15	I_{OZH}	V_O=V_{DD}		—	1.6	—	1.6	—	12	μA
3-State Output Pin: Leakage Current Low Level	15	$-I_{OZL}$	V_O=V_{SS}		—	1.6	—	1.6	—	12	

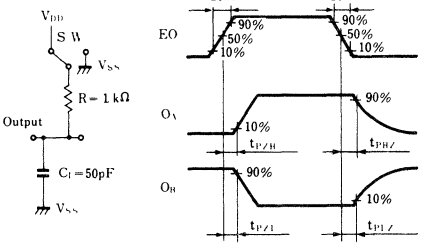
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time Rn→On (H→L)	5	t_{PHL}	—	90	270	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time Sn→On (L→H)	5	t_{PLH}	—	65	195	ns
	10		—	25	75	
	15		—	15	45	
High Level Output Disable Time EO→On (H)	5	t_{PHZ}	—	45	135	ns
	10		—	20	60	
	15		—	10	30	
Low Level Output Disable Time EO→On (L)	5	t_{PLZ}	—	50	150	ns
	10		—	20	60	
	15		—	10	30	
High Level Output Enable Time EO→On (H)	5	t_{PZH}	—	25	75	ns
	10		—	15	45	
	15		—	10	30	
Low Level Output Enable Time EO→On (L)	5	t_{PZL}	—	40	120	ns
	10		—	20	60	
	15		—	15	45	
Low Level Minimum Sn Pulse Width	5	t_{WSH}	—	15	45	ns
	10		—	10	30	
	15		—	8	24	
Low Level Minimum Rn Pulse Width	5	t_{WRH}	—	15	45	ns
	10		—	10	30	
	15		—	8	24	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



Item	S	R	S W	O
t_{PHZ}	V_{DD}	V_{SS}	V_{SS}	A
t_{PLZ}	V_{SS}	V_{DD}	V_{DD}	B
t_{PZH}	V_{DD}	V_{SS}	V_{SS}	A
t_{PZL}	V_{SS}	V_{DD}	V_{DD}	B



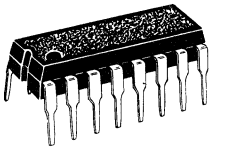
MN4044B / MN4044BS

Quad R/S Latches

■ Description

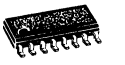
The MN4044B/S have built-in quad independent R/S flip-flops. They are suitable for 4-bit data processing due to the combination of NAND gates.
Four outputs can be high impedance by common input (EO) = L regardless of the latch contents.
These are equivalent to MOTOROLA MC14044 and RCA CD4044B.

P- 3



16-Pin • Plastic DIL Package

P- 4



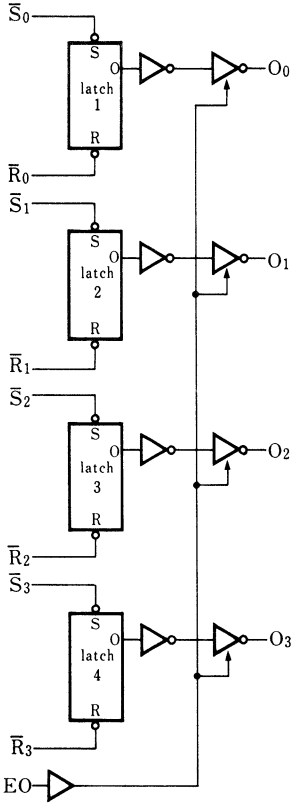
16-Pin • Panaflat Package (SO-16D)

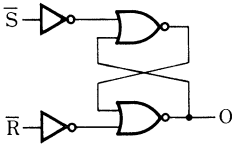
■ Truth Table

Input			Output
EO	S	R	O
L	×	×	Z
H	L	H	H
H	×	L	L
H	H	H	latch

Note) X : don't care
Z : high impedance

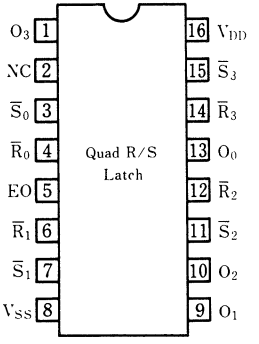
■ Logic Diagram





(One latch)

Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

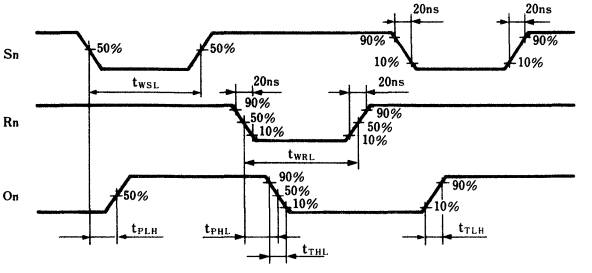
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	4	—	4	—	30	μA
	10				—	8	—	8	—	60	
	15				—	16	—	16	—	120	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=2.5V, V_I= 0 or 5 V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I= 0 or15V		—	0.3	—	0.3	—	1	μA
3-State Output Pin: Leakage Current High Level	15	I_{OZH}	V_O=V_{DD}		—	1.6	—	1.6	—	12	μA
3-State Output Pin: Leakage Current Low Level	15	−I_{OZL}	V_O=V_{SS}		—	1.6	—	1.6	—	12	

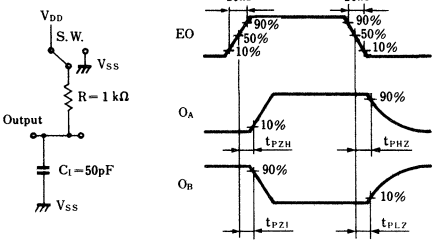
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $\overline{R}n \rightarrow On$ (H→L)	5	t_{PHL}	—	90	270	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time $\overline{S}n \rightarrow On$ (L→H)	5	t_{PLH}	—	90	270	ns
	10		—	40	120	
	15		—	30	90	
High Level Output Disable Time EO→On (H)	5	t_{PHZ}	—	50	150	ns
	10		—	30	90	
	15		—	25	75	
Low Level Output Disable Time EO→On (L)	5	t_{PLZ}	—	30	90	ns
	10		—	25	75	
	15		—	20	60	
High Level Output Enable Time EO→On (H)	5	t_{PZH}	—	50	150	ns
	10		—	25	75	
	15		—	20	60	
Low Level Output Enable Time EO→On (L)	5	t_{PZL}	—	50	150	ns
	10		—	25	75	
	15		—	20	60	
Low Level Minimum Sn Pulse Width	5	t_{WSL}	45	15	—	ns
	10		30	10	—	
	15		24	8	—	
Low Level Minimum Rn Pulse Width	5	t_{WRL}	45	15	—	ns
	10		30	10	—	
	15		24	8	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



Item	S	R	S W.	O
t_{PHZ}	V_{DD}	V_{SS}	V_{SS}	A
t_{PLZ}	V_{SS}	V_{DD}	V_{DD}	B
t_{PZH}	V_{DD}	V_{SS}	V_{SS}	A
t_{PZL}	V_{SS}	V_{DD}	V_{DD}	B



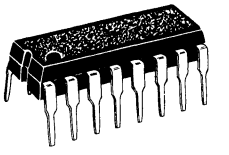
MN4046B / MN4046BS

Phase-Locked Loops

■ Description

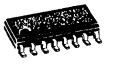
This MN4046B/S are phase-locked loop circuits composed of two phase comparators, VCO, source follower and zener diode.
The two comparators have common signal inputs $SIGN_{IN}$ and $COMP_{IN}$.
$SIGN_{IN}$ should be used by directly connecting to large voltage signals or by connecting small voltage signal through serial capacitors.
Small voltage signals are adjusted to the linear area of the amplifier by the self-bias circuit.
Phase comparator 1 is an Exclusive-OR gate which outputs digital error signal $PC1_{OUT}$, and shifts phase by 90° with the central frequency between $SIGN_{IN}$ signal and $COMP_{IN}$ signal (50% duty cycle)
Phase comparator 2 outputs digital error signals PC_{OUT} and PCP_{OUT} and phase shifts between $SIGN_{IN}$ and $COMP_{IN}$ (duty cycle is arbitrary) is 0°.
The frequency of signal VCO_{OUT} obtained by the linear VCO is defined by the voltage of input VCO_{IN} and the constant of the resistor and capacitor connected to R_1, R_2, C_{1A} and C_{1B}.
When VOC_{IN} signal is necessary and there is no space for loading, source follower output SF_{OUT} together with an external resistor is used. When inhibit input INH is "1" level, stand-by power dissipation can be minimized because the VCO and source follower are disabled.
A zener diode should be used to adjust the power supply source.
The MN4046B/S can be widely used for modulation and demodulation of FM and FSK, composition and discrimination of frequencies, tone decoding, synchronization and adjustment of data, and conversion of voltage and frequencies.

P- 3



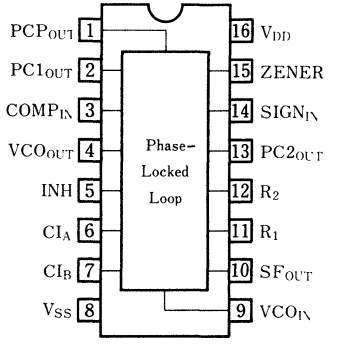
16-Pin • Plastic DIL Package

P- 4

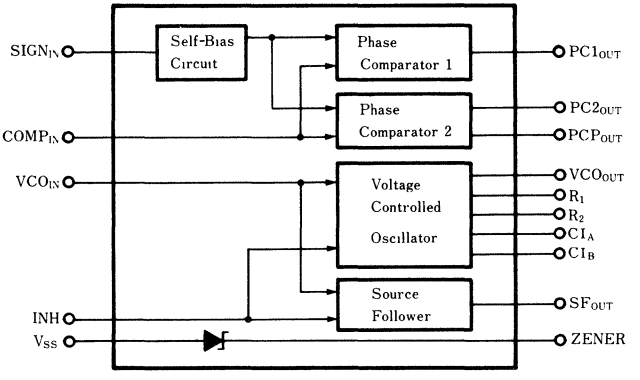


16-Pin • Panaflat Package (SO-16D)

Pin Configuration



■ Block Diagram



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	INH = H, $SIGN_{IN}$ = H		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA
Input Capacitance		C_I			—	—	—	7.5	—	—	pF

■ Electrical Characteristics

• Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}		—	60	180	ns
	10			—	30	90	
	15			—	20	60	
Output Fall Time	5	t_{THL}		—	60	180	ns
	10			—	30	90	
	15			—	20	60	

• Phase · Comparator

Item		V_{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Input Resistance	$SIGN_{IN}$	5	R_{IN}		—	750	—	kΩ
		10			—	220	—	
		15			—	140	—	
	$COMP_{IN}$	15			—	—	—	
Minimum Input Sensitivity		5	V_{IN}	AC Couple-$SIGN_{IN}$	—	150	—	mV_{P-P}
		10		R_1=10kΩ, R_2=∞	—	150	—	
		15		C_I=100pF	—	200	—	
DC Couple-$SIGN_{IN}$: $COMP_{IN}$ Low Level		5	V_{IL}		—	—	1.5	V
		10			—	—	3	
		15			—	—	4	
DC Couple-$SIGN_{IN}$: $COMP_{IN}$ High Level		5	V_{IH}		3.5	—	—	V
		10			7	—	—	
		15			11	—	—	

• Voltage Control Oscillator

Item	V_{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Maximum Frequency	5	fmax	$VCO_{IN}=V_{DD}$	0.5	1	—	MHz
	10		R_1=10kΩ, R_2=∞	1	2	—	
	15		C_1=50pF	1.3	2.7	—	
Temperature-Frequency Stability	5		R_2=∞	—	0.12	—	%/℃
	10			—	0.04	—	
	15			—	0.015	—	
Linearity	5		R_2=∞, VCO_{IN}=2.50V±0.30V, R_1>10kΩ	—	0.50	—	%
	10		R_2=∞, VCO_{IN}=5.00V±2.50V, R_1>400kΩ	—	0.25	—	
	15		R_2=∞, VCO_{IN}=7.50V±5.00V, R_1=1MΩ	—	0.25	—	
Output Duty Cycle	5 ~ 15	δ		—	50	—	%
Input Resistance (VCO_{IN})	5 ~ 15	R_{IN}		—	10^6	—	MΩ

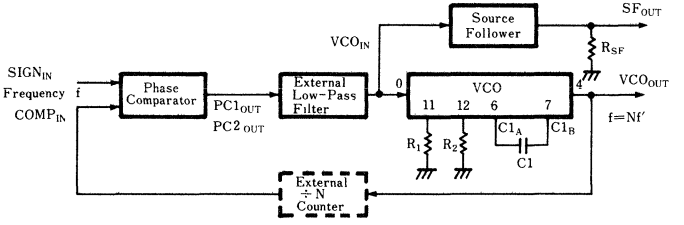
• Source · Follower

Item	V_{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Offset Voltage	5		$VCO_{IN}-SF_{OUT}$, R_{SF}=50kΩ	—	1.5	—	V
	10			—	1.7	—	
	15			—	1.8	—	
Linearity	5		VCO_{IN}=2.50V±0.30V, R_{SF}>50kΩ	—	0.3	—	%
	10		VCO_{IN}=5.00V±2.50V, R_{SF}>50kΩ	—	1.0	—	
	15		VCO_{IN}=7.50V±5.00V, R_{SF}>50kΩ	—	1.3	—	

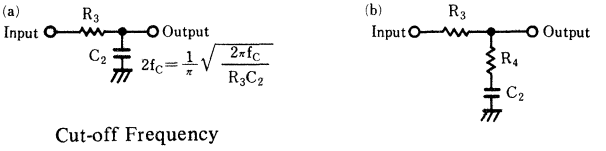
• Zener Diode

Item	V_{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Zener Voltage		V_Z	$I_Z = 50\mu A$	—	7.3	—	V
Action Resistance		R_Z	$I_Z = 1$ mA	—	25	—	Ω

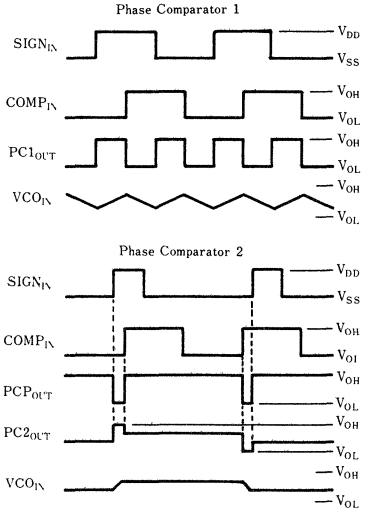
(Fig. 1) General PLL Connections



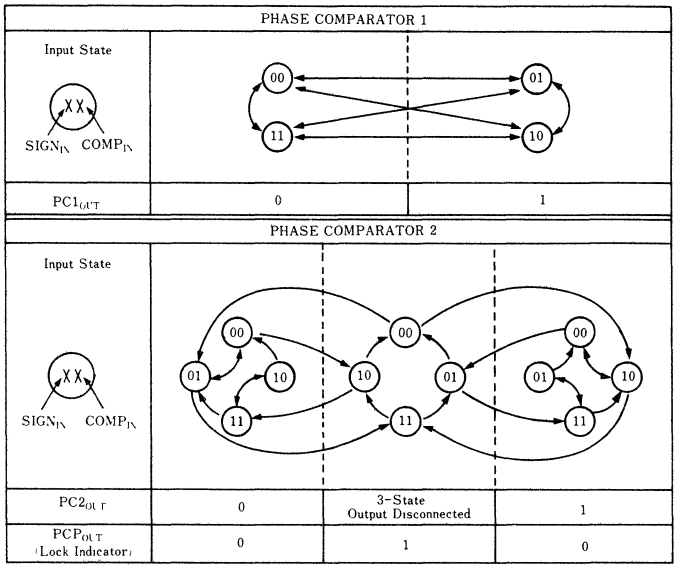
Typical Low-Pass Filters



Cut-off Frequency



(Fig. 2) Phase · Comparator Mode Diagrams



MN4049B / MN4049BS

Hex Inverting Buffers

■ Description

The MN4049B/S are hex inverting buffers and can be used to convert the logic level. These devices provide high output current to drive TTLs and DTL directly, and are used as CMOS-to-TTL converters with two normal-TTL drive capability. They have good switching characteristics due to triple inverting circuits.
The MN4049B/S are equivalent to MOTOROLA MC14049B and RCA CD4049B.

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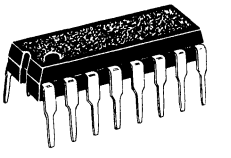
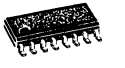


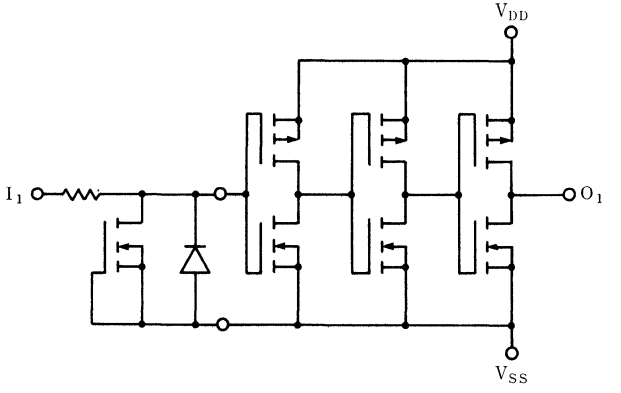
16-Pin • Plastic DIL Package

P- 4

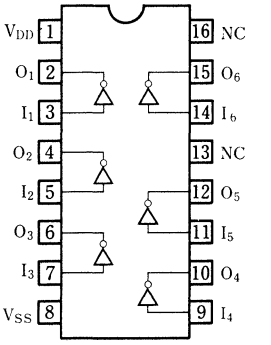


16-pin • Panaflat Package (SO-16D)

■ Schematic Diagram (1/6) & Input Protection Circuit



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～+18	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 40	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ Guaranteed Fan-Out for Logic Circuit Series

Drive IC	Guaranteed Fan-Out
Normal TTL	2
74LS	9
74L	16

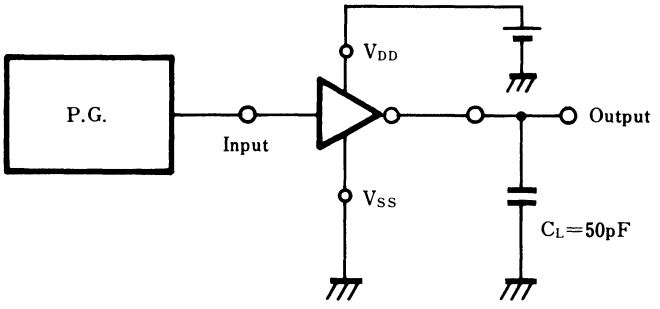
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	4	—	4	—	30	μA
	10			—	8	—	8	—	60	
	15			—	16	—	16	—	120	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	4.75	I_{OL}	V_O=0.4V,	3.5	—	2.9	—	2.3	—	mA
	10		V_O=0.5V, V_I=0 or 10V	12	—	10	—	8	—	
	15		V_O=1.5V, V_I=0 or 15V	24	—	20	—	16	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

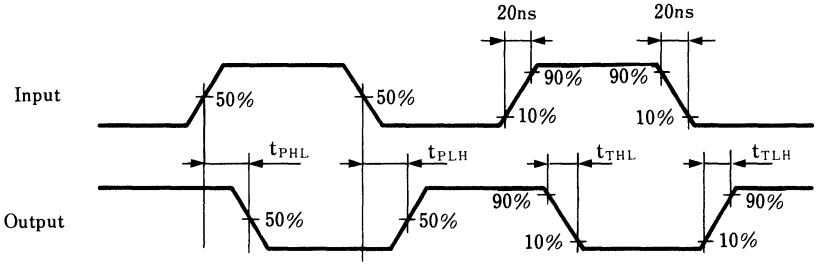
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	25	75	ns
	10		—	10	30	
	15		—	7	21	
Propagation Delay Time	5	t_{PLH}	—	60	180	ns
	10		—	30	90	
	15		—	25	75	
Propagation Delay Time	5	t_{PHL}	—	50	150	ns
	10		—	20	60	
	15		—	15	45	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



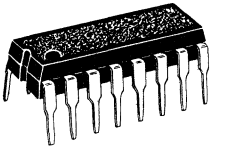
MN4050B/MN4050BS

Hex Non-Inverting Buffers

■ Description

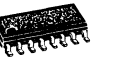
The MN4050B/S are hex non-inverting buffers which can be used to convert the logic level.
These devices provide high output current to drive TTLs and DTL directly, and are used as CMOS-to-TTL converters with two normal-TTL drive capability. They have good switching characteristics due to double inverting circuits.
The MN4050B/S are equivalent to MOTOROLA MC14050B and RCA CD4050B.

P-3



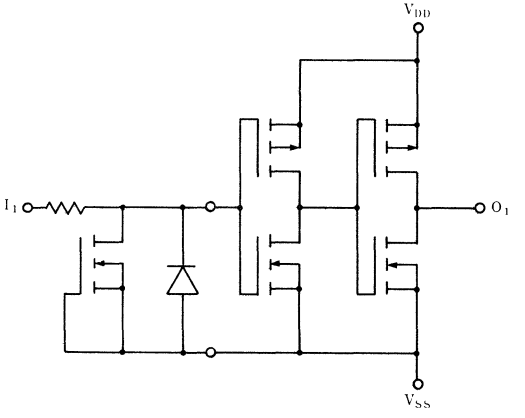
16-Pin • Plastic DIL Package

P-4

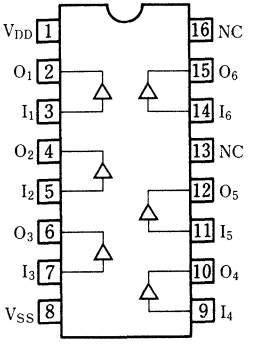


16-Pin • Panaflat Package (SO-16D)

■ Schematic Diagram (1/6) & Input Protection Circuit



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～+18	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 40	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ Guaranteed Fan-Out for Logic Circuit Series

Drive IC	Guaranteed Fan-Out
Normal TTL	2
74LS	9
74L	16

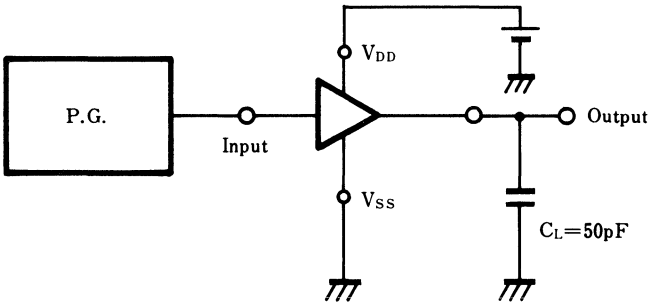
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	4	—	4	—	30	μA
	10				—	8	—	8	—	60	
	15				—	16	—	16	—	120	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	4.75	I_{OL}	V_O=0.4V		3.5	—	2.9	—	2.3	—	mA
	10		V_O=0.5V, V_I=0 or 10V		12	—	10	—	8	—	
	15		V_O=1.5V, V_I=0 or 15V		24	—	20	—	16	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

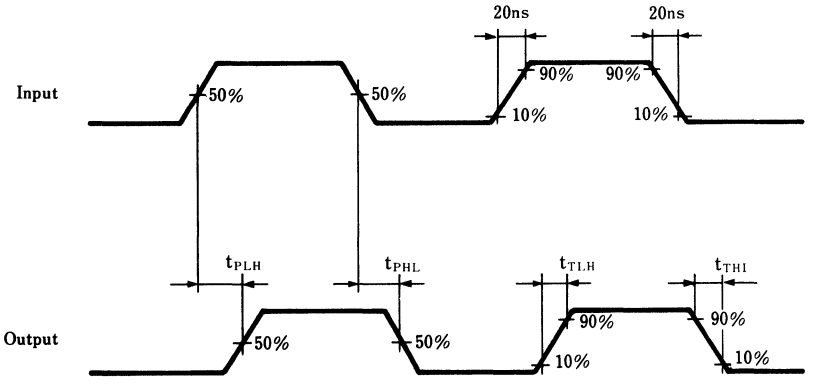
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	25	75	ns
	10		—	10	30	
	15		—	7	21	
Propagation Delay Time	5	t_{PLH}	—	55	165	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time	5	t_{PHL}	—	35	105	ns
	10		—	20	60	
	15		—	15	45	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



MN4051B/MN4051BS

8-Channel Analog Multiplexers

■ Description

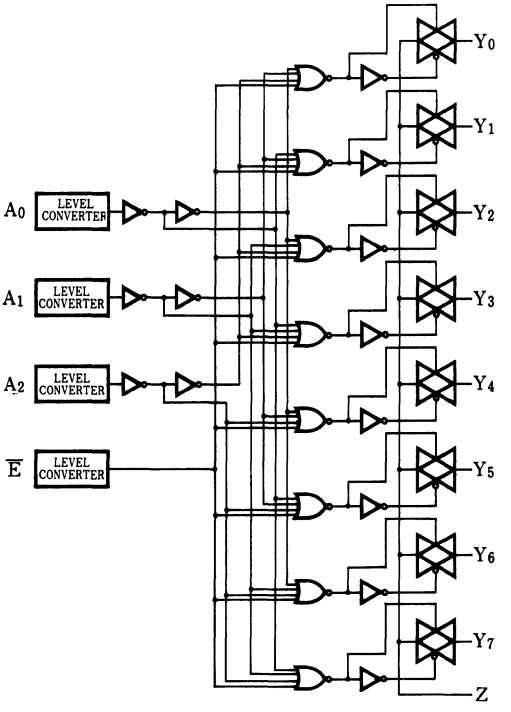
The MN4051B/S are analog multiplexer which control 8-channel analog switching by 3-input digital signals.
ON/OFF output voltage ratio is high and cross-talk between analog switches is low.
The MN4051B/S are equivalent to MOTOROLA MC14051B and RCA CD4051B.

■ Truth Table

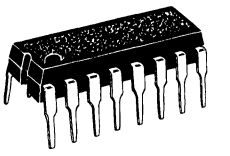
Input				Channel
$\overline{E}$	A_2	A_1	A_0	ON
L	L	L	L	Y_0-Z
L	L	L	H	Y_1-Z
L	L	H	L	Y_2-Z
L	L	H	H	Y_3-Z
L	H	L	L	Y_4-Z
L	H	L	H	Y_5-Z
L	H	H	L	Y_6-Z
L	H	H	H	Y_7-Z
H	×	×	×	All OFF

Note) × : don't care

■ Logic Diagram



P- 3

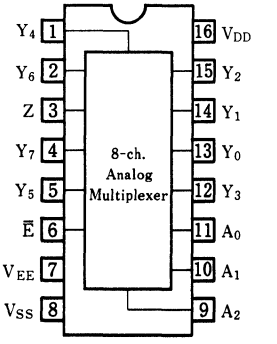


16-Pin • Plastic DIL Package

P- 4

16-Pin • Panaflat Package (SO-16D)

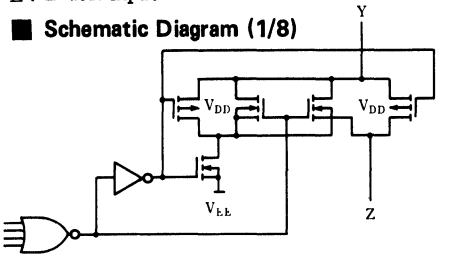
Pin Configuration



Pin Explanation

$Y_0 \sim Y_7$: Analog input/output
$A_0 \sim A_2$: Address input
Z : Common input/output
$\overline{E}$: Enable input

■ Schematic Diagram (1/8)



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ DC Characteristics (Ta=25℃, V_{SS}=0V)

Item	V_{DD}−V_{EE} (V)	Symbol	Conditions	min.	typ.	max.	Unit
On Resistance	5	R_{ON}	V_I=5V	—	200	800	Ω
			V_I=2.5V	—	550	1300	
			V_I=0.25V	—	200	800	
On Resistance	10	R_{ON}	V_I=10V	—	80	300	Ω
			V_I=5V	—	100	350	
			V_I=0.25V	—	80	300	
On Resistance	15	R_{ON}	V_I=15V	—	60	200	Ω
			V_I=7.5V	—	80	250	
			V_I=0.25V	—	60	200	

■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$)

Item	V_{DD} (V)	Symbol	Conditions	min.	typ.	max.	Unit
Propagation Delay Time (Fig. 1) Vis→V_{OS} (H→L)	5	t_{PHL}	$R_L=10k\Omega$, $C_L=50pF$, $\overline{E}=V_{SS}$	—	15	45	ns
	10			—	5	15	
	15			—	5	15	
Propagation Delay Time (Fig. 1) Vis→V_{OS} (L→H)	5	t_{PLH}		—	15	45	ns
	10			—	5	15	
	15			—	5	15	
Propagation Delay Time (Fig. 1) An→V_{OS} (H→L)	5	t_{PHL}	$R_L=10k\Omega$, $C_L=50pF$, $\overline{E}=V_{SS}$	—	170	510	ns
	10			—	65	195	
	15			—	50	150	
Propagation Delay Time (Fig. 1) An→V_{OS} (L→H)	5	t_{PLH}		—	160	480	ns
	10			—	65	195	
	15			—	45	135	
Output Disable Time (Fig. 1) $\overline{E}$→V_{OS} (H)	5	t_{PHZ}	$R_L=10k\Omega$, $C_L=50pF$, $\overline{E}=V_{DD}$	—	125	375	ns
	10			—	90	270	
	15			—	85	255	
Output Disable Time (Fig. 1) $\overline{E}$→V_{OS} (L)	5	t_{PLZ}		—	155	465	ns
	10			—	120	360	
	15			—	115	345	
Output Enable Time (Fig. 1) $\overline{E}$→V_{OS} (H)	5	t_{PZH}	$R_L=10k\Omega$, $C_L=50pF$, $\overline{E}=V_{DD}$	—	190	570	ns
	10			—	75	225	
	15			—	50	150	
Output Enable Time (Fig. 1) $\overline{E}$→V_{OS} (L)	5	t_{PZL}		—	195	585	ns
	10			—	75	225	
	15			—	50	150	
Sine Wave Distortion (Fig. 2)	5		$R_L=10k\Omega$, $C_L=15pF$, fis = 1 kHz, Vis = $\frac{1}{2}V_{DD(P-P)}$	—	0.25	—	%
	10			—	0.04	—	
	15			—	0.04	—	
Crosstalk (Fig. 3) (Between 2 Channels)	5		$R_L=1k\Omega$, Vis = $\frac{1}{2}V_{DD(P-P)}$	—	—	—	MHz
	10			—	1	—	
	15			—	—	—	
Crosstalk (Fig. 1) (Address Input → Output)	5		$R_L=10k\Omega$, $C_L=15pF$, $\overline{E}$ or An = V_{DD}	—	—	—	mV
	10			—	50	—	
	15			—	—	—	
Feedthrough (Fig. 2) (Note. 1) (OFF)	5		$R_L=1k\Omega$, $C_L=5pF$, Vis = $\frac{1}{2}V_{DD(P-P)}$	—	—	—	MHz
	10			—	1	—	
	15			—	—	—	
Propagation Frequency (Fig. 2) (Note. 2)	5		$R_L=1k\Omega$, $C_L=5pF$, Vis = $\frac{1}{2}V_{DD(P-P)}$	—	13	—	MHz
	10			—	40	—	
	15			—	70	—	
Input Capacitance (Control)		C_I		—	—	7.5	pF
Input Capacitance (Switch)		C_I		—	10	—	pF

Fig. 1 Propagation Delay Time, Output Disable/Enable Time, Crosstalk Test Circuit

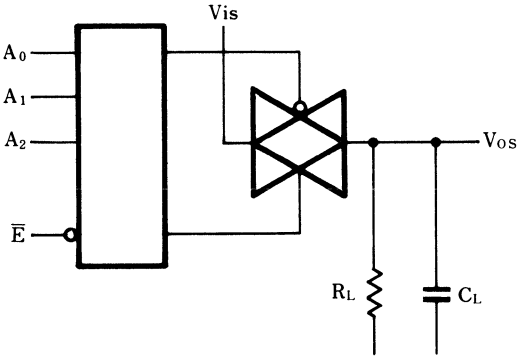
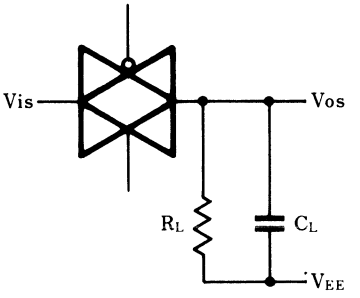


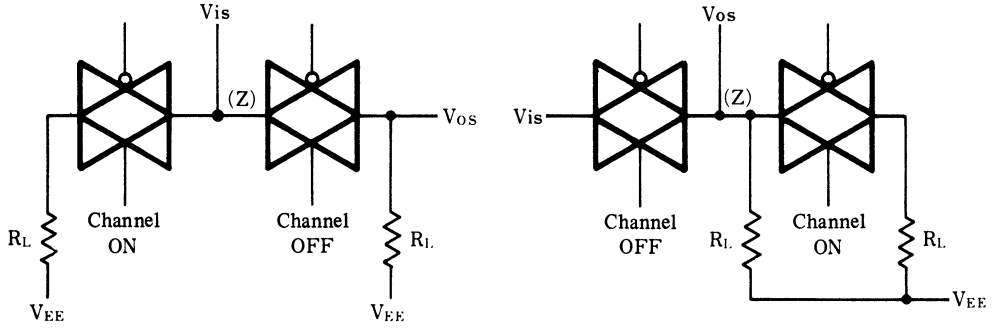
Fig. 2 Sine Wave Distortion, Feedthrough, Frequency Response, Test Circuit



(注1) $20 \log \frac{Vos}{Vis} = -50dB$

(注2) $20 \log \frac{Vos}{Vis} = -3\,dB$

Fig. 3 Crosstalk Test Circuit



$$20 \log \frac{Vos}{Vis} = -50\,dB$$

MN4052B / MN4052BS

Dual 4-Channel Analog Multiplexers

■ Description

The MN4052B/S are dual 4-channel analog multiplexer/demultiplexers which enable selection of digital or analog signals and their complexes.

Each channel is established by controlling signals of the enable input (E). The inputs/outputs can swing between V_{DD} and V_{EE} ($\leqq$ 15V) even if the amplitude of control signals is below V_{DD}.

It can be controlled to low impedance circuit because the impedance of the switch is very low. The MN4052B/S are equivalent to MOTOROLA MC14052B and RCA CD4052B.

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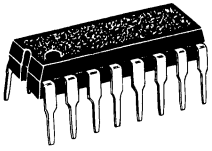


16-Pin • Plastic DIL Package

P-4

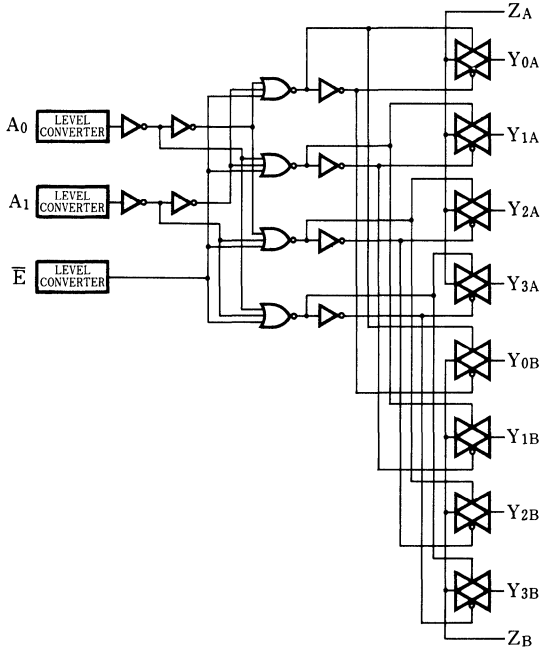
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

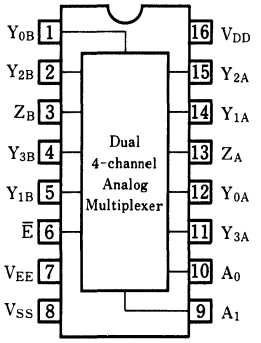
Input			Channel ON
$\overline{E}$	A_1	A_0	
L	L	L	$Y_{0A}-Z_A$; $Y_{0B}-Z_B$
L	L	H	$Y_{1A}-Z_A$; $Y_{1B}-Z_B$
L	H	L	$Y_{2A}-Z_A$; $Y_{2B}-Z_B$
L	H	H	$Y_{3A}-Z_A$; $Y_{3B}-Z_B$
H	×	×	All OFF

Note) × : don't care

■ Logic Diagram



Pin Configuration



Pin Explanation

Y_{0A}~Y_{3A} : Analog input/output

Y_{0B}~Y_{3B} : Analog input/output

A_0, A_1 : Address input

$\overline{E}$: Enable input

Z_A, Z_B : Common input/output

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ DC Characteristics (Ta=25℃, V_{SS}=0V)

Item	$V_{DD}-V_{EE}$ (V)	Symbol	Conditions	min.	typ.	max.	Unit
On Resistance	5	R_{ON}	V_I=5V	—	200	800	Ω
			V_I=2.5V	—	550	1300	
			V_I=0.25V	—	200	800	
On Resistance	10	R_{ON}	V_I=10V	—	80	300	Ω
			V_I=5V	—	100	350	
			V_I=0.25V	—	80	300	
On Resistance	15	R_{ON}	V_I=15V	—	60	200	Ω
			V_I=7.5V	—	80	250	
			V_I=0.25V	—	60	200	

■ Switching Characteristics (Ta=25℃, V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	min.	typ.	max.	Unit
Propagation Delay Time (Fig. 1) Vis→Vos (H→L)	5	t_{PHL}	R_L=10kΩ, C_L=50pF, $\overline{E}$=V_{SS}	—	10	30	ns
	10			—	5	15	
	15			—	5	15	
Propagation Delay Time (Fig. 1) Vis→Vos (L→H)	5	t_{PLH}		—	10	30	ns
	10			—	5	15	
	15			—	5	15	
Propagation Delay Time (Fig. 1) An→Vos (H→L)	5	t_{PHL}	R_L=10kΩ, C_L=50pF, $\overline{E}$=V_{SS}	—	150	450	ns
	10			—	65	195	
	15			—	50	150	
Propagation Delay Time (Fig. 1) An→Vos (L→H)	5	t_{PLH}		—	75	225	ns
	10			—	35	105	
	15			—	30	90	
Output Disable Time (Fig. 1) $\overline{E}$→Vos (H)	5	t_{PHZ}	R_L=10kΩ, C_L=50pF, $\overline{E}$=V_{DD}	—	100	300	ns
	10			—	90	270	
	15			—	90	270	
Output Disable Time (Fig. 1) $\overline{E}$→Vos (L)	5	t_{PLZ}		—	95	285	ns
	10			—	90	270	
	15			—	90	270	
Output Enable Time (Fig. 1) $\overline{E}$→Vos (H)	5	t_{PZH}	R_L=10kΩ, C_L=50pF, $\overline{E}$=V_{DD}	—	130	390	ns
	10			—	55	165	
	15			—	45	135	
Output Enable Time (Fig. 1) $\overline{E}$→Vos (L)	5	t_{PZL}		—	120	360	ns
	10			—	50	150	
	15			—	35	105	
Sine Wave Distortion (Fig. 2)	5		R_L=10kΩ, C_L=15pF, fis=1 kHz, Vis=$\frac{1}{2}V_{DD\,(P\text{-}P)}$	—	0.25	—	%
	10			—	0.04	—	
	15			—	0.04	—	
Crosstalk (Fig. 3) (Between 2 Channels)	5		R_L=1 kΩ, Vis=$\frac{1}{2}V_{DD\,(P\text{-}P)}$	—	—	—	MHz
	10			—	1	—	
	15			—	—	—	
Crosstalk (Fig. 1) (Address Input→ Output)	5		R_L=10kΩ, C_L=15pF, $\overline{E}$ or An=V_{DD}	—	—	—	mV
	10			—	50	—	
	15			—	—	—	
Propagation Frequency (Fig. 2) (Note 2)	5		R_L=1 kΩ, C_L=5 pF, Vis=$\frac{1}{2}V_{DD\,(P\text{-}P)}$	—	—	—	MHz
	10			—	1	—	
	15			—	—	—	
Feedthrough (Fig. 2) (Note 1) (OFF)	5		R_L=1 kΩ, C_L=5 pF, Vis=$\frac{1}{2}V_{DD\,(P\text{-}P)}$	—	13	—	MHz
	10			—	40	—	
	15			—	70	—	
Input Capacitance		C_I		—	—	7.5	pF

Fig. 1 Propagation Delay Time, Output Disable/Enable Time, Crosstalk Test Circuit

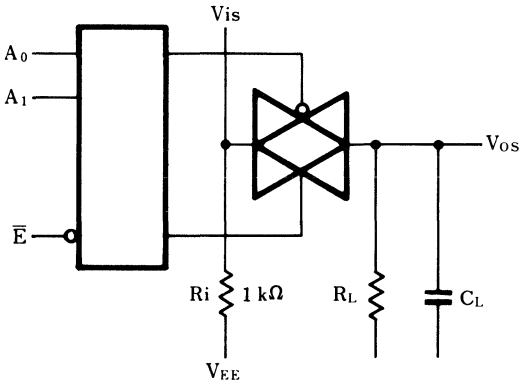
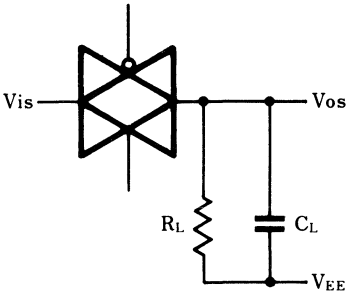


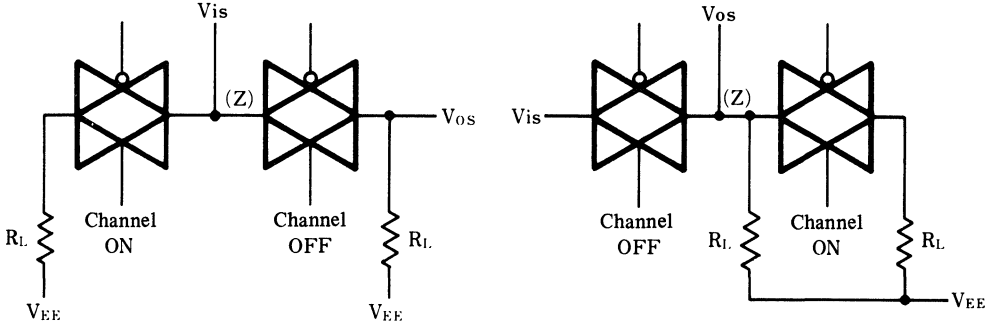
Fig. 2 Sine Wave Distortion, Feedthrough, Frequency Response, Test Circuit



(注1) $20 \log \frac{Vos}{Vis} = -50\,dB$

(注2) $20 \log \frac{Vos}{Vis} = -3\,dB$

Fig. 3 Crosstalk Test Circuit



$$20 \log \frac{V_{OS}}{Vis} = -50\,dB$$

MN4053B/MN4053BS

Triple 2-Channel Analog Multiplexers

■ Description

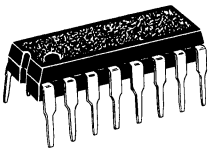
The MN4053B/S are triple 2-channel analog multiplexer/demultiplexers which enable selection of digital or analog signals and their complexes.

Each channel is established by controlling signals of the enable input (E). The inputs/outputs can swing between V_{DD} and V_{EE} ($\leqq$ 15V) even if the amplitude of control signals is below V_{DD}.

It can be controlled to low impedance circuit because the impedance of the switch is very low.

The MN4053B/S are equivalent to MOTOROLA MC14053B and RCA CD4052B.

P-3



16-Pin • Plastic DIL Package

P-4

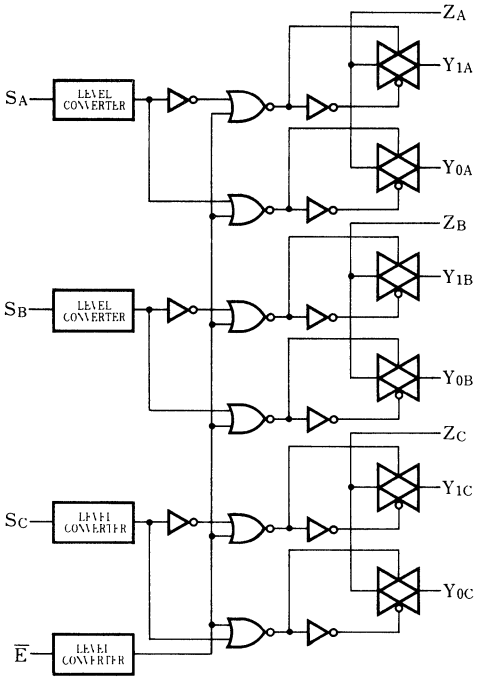
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

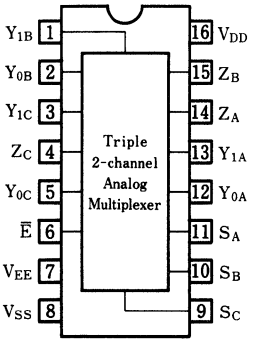
Input		Channel ON
$\overline{E}$	S_A	
L	L	$Y_{0A}-Z_A$
L	H	$Y_{1A}-Z_A$
H	×	All OFF

Note) X : don't care

■ Logic Diagram



Pin Configuration



Pin Explanation

$Y_{0A}\sim Y_{0C}$: Analog input/output
$Y_{1A}\sim Y_{1C}$: Analog input/output
$S_A\sim S_C$: Select input
$\overline{E}$: Enable input
$Z_A\sim Z_C$: Common input/output

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ DC Characteristics (Ta=25℃, V_{SS}=0V)

Item	V_{DD}−V_{EE} (V)	Symbol	Conditions	min.	typ.	max.	Unit
On Resistance	5	R_{ON}	V_I=5V	—	200	800	Ω
			V_I=2.5V	—	550	1300	
			V_I=0.25V	—	200	800	
On Resistance	10	R_{ON}	V_I=10V	—	80	300	Ω
			V_I=5V	—	100	350	
			V_I=0.25V	—	80	300	
On Resistance	15	R_{ON}	V_I=15V	—	60	200	Ω
			V_I=7.5V	—	80	250	
			V_I=0.25V	—	60	200	

■ **Switching Characteristics** (Ta=25℃, V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	min.	typ.	max.	Unit
Propagation Delay Time (Fig. 1) Vis→Vos (H→L)	5	t_{PHL}	R_L=10kΩ, C_L=50pF, $\overline{E}$=V_{DD}	—	10	30	ns
	10			—	5	15	ns
	15			—	5	15	ns
Propagation Delay Time (Fig. 1) Vis→Vos (L→H)	5	t_{PLH}		—	10	30	n
	10			—	5	15	ns
	15			—	5	15	n
Propagation Delay Time (Fig. 1) Sn→Vos (H→L)	5	t_{PHL}	R_L=10kΩ, C_L=50pF, $\overline{E}$=V_{SS}	—	200	600	n
	10			—	85	255	ns
	15			—	65	195	n
Propagation Delay Time (Fig. 1) Sn→Vos (L→H)	5	t_{PLH}		—	275	725	%
	10			—	100	300	ns
	15			—	65	195	
Output Disable Time (Fig. 1) $\overline{E}$→Vos (H)	5	t_{PHZ}	R_L=10kΩ, C_L=50pF, $\overline{E}$=V_{DD}	—	200	600	ns
	10			—	115	345	
	15			—	110	330	
Output Disable Time (Fig. 1) $\overline{E}$→Vos (L)	5	t_{PLZ}		—	200	600	ns
	10			—	120	360	
	15			—	110	330	
Output Enable Time (Fig. 1) $\overline{E}$→Vos (H)	5	t_{PZH}	R_L=10kΩ, C_L=50pF, $\overline{E}$=V_{DD}	—	260	780	ns
	10			—	95	285	
	15			—	65	195	
Output Enable Time (Fig. 1) $\overline{E}$→Vos (L)	5	t_{PZL}		—	280	840	ns
	10			—	105	315	
	15			—	70	210	
Sine Wave Distortion (Fig. 2)	5		R_L=10kΩ, C_L=15pF, fis=1 kHz	—	0.25	—	%
	10			—	0.04	—	
	15			—	0.04	—	
Crosstalk (Fig. 3) (Between 2 Channels)	5		R_L=1 kΩ, Vis=$\frac{1}{2}V_{DD\ (P-P)}$	—	—	—	MHz
	10			—	1	—	
	15			—	—	—	
Crosstalk (Fig. 1) (Address Input → Output)	5		R_L=10kΩ, C_L=15pF, $\overline{E}$n or Sn=V_{DD}	—	—	—	mV
	10			—	50	—	
	15			—	—	—	
Feedthrough (Fig. 2) (Note 1) (OFF)	5		R_L=1 kΩ, C_L=5 pF, Vis=$\frac{1}{2}V_{DD\ (P-P)}$	—	—	—	MHz
	10			—	1	—	
	15			—	—	—	
Propagation (Fig. 2) (Note 2) Frequency	5			—	13	—	MHz
	10			—	40	—	
	15			—	70	—	
Input Capacitance		C_I		—	—	7.5	pF

Fig. 1 Propagation Delay Time, Output Disable/Enable Time, Crosstalk Test Circuit

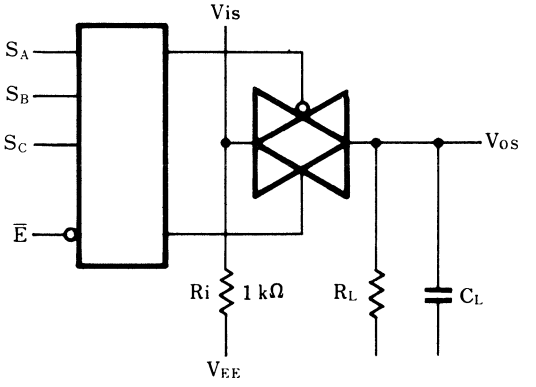
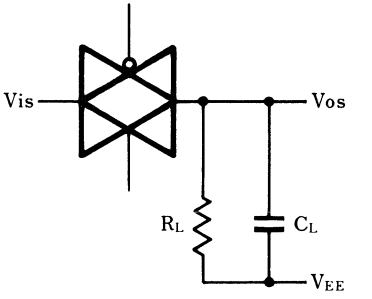


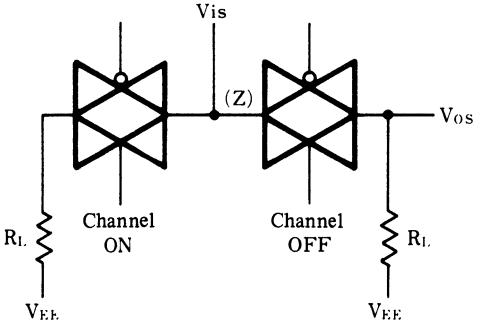
Fig. 2 Sine Wave Distortion, Feedthrough, Frequency Response, Test Circuit



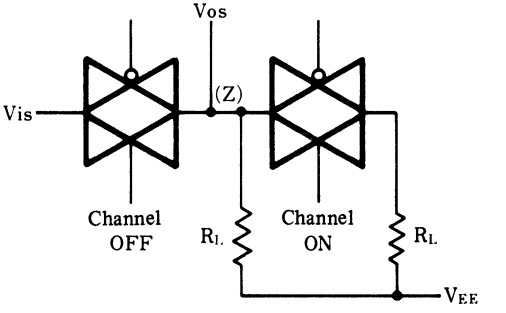
(注1) $20 \log \frac{Vos}{Vis} = -50\,dB$

(注2) $20 \log \frac{Vos}{Vis} = -3\,dB$

Fig. 3 Crosstalk Test Circuit



(a)



(b)

$$20 \log \frac{Vos}{Vis} = -50\,dB$$

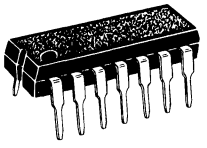
MN4066B / MN4066BS

Quad Analog Switches

■ Description

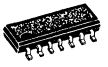
The MN4066B/S have 4 independent analog switches. A High on the enable input establishes a low impedance state (ON stage) between input and output of the switch. A Low establishes a high impedance (OFF stage).
MN4066B is pin-compatible to MN4016B. But MN4066B has low R_{ON} and better transfer characteristics. So applications are for analog/digital switching and chopper modulation and demodulation.
The MN4066B/S are equivalent to MOTOROLA MC14066B and RCA CD4066B.

P-1



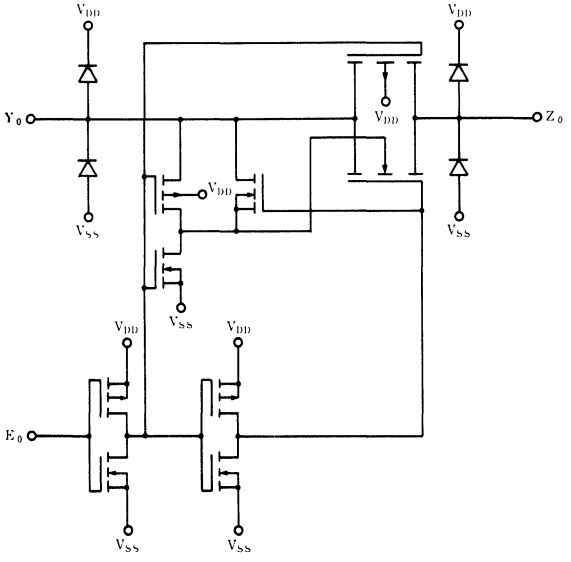
14-Pin • Plastic DIL Package

P-2

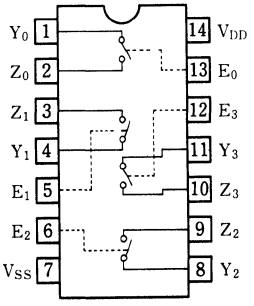


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/4)



Pin Configuration



Pin Explanation

$E_0 \sim E_3$: Enable input
$Y_0 \sim Y_3$: Analog input/output
$Z_0 \sim Z_3$: Analog input/output

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	1	—	1	—	7.5	μA
	10				—	2	—	2	—	15	
	15				—	4	—	4	—	30	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V.		—	0.3	—	0.3	—	1	μA

■ DC Characteristics (Ta=25℃, V_{SS}=0V)

Item	V_{DD}(V)	Symbol	Conditions	min.	typ.	max.	Unit
On Resistance	5	R_{ON}	V_{SS}=0V, V_I=5V	—	150	450	Ω
			V_{SS}=0V, V_I=2.5V	—	380	1140	
			V_{SS}=0V, V_I=0.25V	—	150	450	
	10	R_{ON}	V_{SS}=0V, V_I=10V	—	80	250	Ω
			V_{SS}=0V, V_I=5V	—	100	300	
			V_{SS}=0V, V_I=0.25V	—	100	300	
	15	R_{ON}	V_{SS}=0V, V_I=15V	—	60	180	Ω
			V_{SS}=0V, V_I=7.5V	—	70	210	
			V_{SS}=0V, V_I=0.25V	—	60	180	
	5	R_{ON}	V_{SS}=−5V, V_I=5V	—	100	300	Ω
			V_{SS}=−5V, V_I=±0.25V	—	100	300	
			V_{SS}=−5V, V_I=−5V	—	100	300	
	7.5	R_{ON}	V_{SS}=−7.5V, V_I=7.5V	—	70	210	Ω
			V_{SS}=−7.5V, V_I=±0.25V	—	70	210	
			V_{SS}=−7.5V, V_I=−7.5V	—	70	210	
Input Output of Leakage Current	10	I_{OFF}	V_I=10V, V_O=0V	—	30	125	nA
			V_I=0V, V_O=10V	—	30	125	
	15		V_I=15V, V_O=0V	—	60	250	nA
			V_I=0V, V_O=15V	—	60	250	

■ Switching Characteristics (Ta=25℃, V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	min.	typ.	max.	Unit
Propagation Delay Time (Fig. 1) Vis→Vos	5	t_{PHL}	R_L=10kΩ, C_L=50pF, En=V_{DD}	—	10	30	ns
	10			—	5	15	
	15			—	5	15	
Propagation Delay Time (Fig. 1) Vis→Vos	5	t_{PLH}		—	10	30	ns
	10			—	5	15	
	15			—	5	15	
Propagation Delay Time (Fig. 1) En→Vos	5	t_{PHZ}	R_L=10kΩ, C_L=50pF, Vis=V_{DD}, R_L→V_{SS}	—	80	240	ns
	10			—	65	195	
	15			—	60	180	
Propagation Delay Time (Fig. 1) En→Vos	5	t_{PLZ}	R_L=10kΩ, C_L=50pF, Vis=V_{SS}, R_L→V_{DD}	—	80	240	ns
	10			—	70	210	
	15			—	70	210	
Propagation Delay Time (Fig. 1) En→Vos	5	t_{PZH}	R_L=10kΩ, C_L=50pF, Vis=V_{DD}, R_L→V_{SS}	—	40	120	ns
	10			—	20	60	
	15			—	15	45	
Propagation Delay Time (Fig. 1) En→Vos	5	t_{PZL}	R_L=10kΩ, C_L=50pF, Vis=V_{SS}, R_L→V_{DD}	—	45	135	ns
	10			—	20	60	
	15			—	15	45	
Sine Wave Distortion (Fig. 2)	5		R_L=10kΩ, C_L=50pF, En=V_{DD}, f=1 kHz, Vis=$\frac{1}{2}V_{DD(P\text{-}P)}$	—	—	—	%
	10			—	0.1	—	
	15			—	0.1	—	
Crosstalk (Fig. 3) (Between 2 Channels)	5		R_L=1 kΩ, Vis=$\frac{1}{2}V_{DD(P\text{-}P)}$	—	—	—	MHz
	10			—	1	—	
	15			—	—	—	
Crosstalk (Fig. 1) En→V_{SS}	5		R_L=1 kΩ, C_L=15pF, En=V_{DD}	—	—	—	mV
	10			—	80	—	
	15			—	—	—	
Feedthrough (Fig. 2) (Note) (OFF)	5		R_L=1 kΩ, C_L=50pF, En=V_{SS}, Vis=$\frac{1}{2}V_{DD(P\text{-}P)}$	—	—	—	kHz
	10			—	700	—	
	15			—	—	—	
Input Capacitance		C_I		—	—	7.5	pF

Fig. 1 Propagation Delay Time, Crosstalk Test Circuit

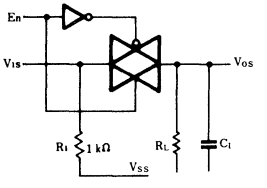
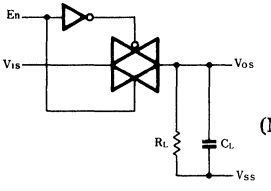
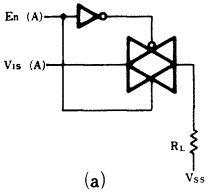


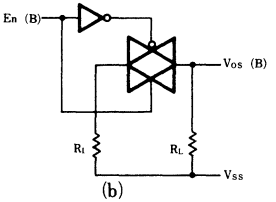
Fig. 2 Sine Wave Distortion, Feedthrough Test Circuit



(Note) $20 \log \frac{Vos}{Vis} = -50dB$

Fig. 3 Crosstalk Test Circuit





$20 \log \frac{Vos\ (B)}{Vis\ (A)} = -50dB$

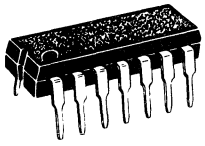
MN4068B/MN4068BS

8-Input NAND Gates

Description

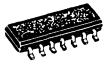
The MN4068B/S are positive 8-input NAND gates.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time.

P-1



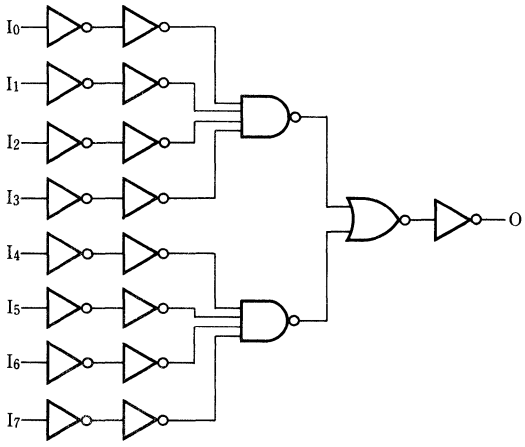
14-Pin • Plastic DIL Package

P-2

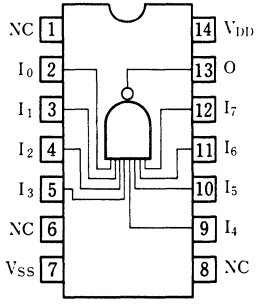


14-Pin • Panaflat Package (SO-14D)

Logic Diagram



Pin Configuration



Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

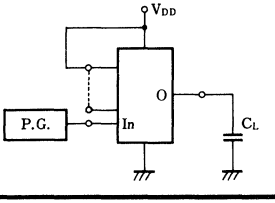
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		| I_O | <1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		| I_O | <1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

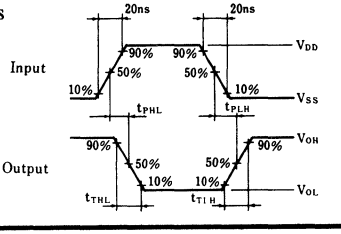
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time I−O (H→L)	5	t_{PHL}	—	95	285	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time I−O (L→H)	5	t_{PLH}	—	80	240	ns
	10		—	35	105	
	15		—	30	90	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



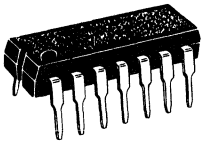
MN4069UB/MN4069UBS

Hex Inverters

■ Description

The MN4069UB/S have hex inverters without buffers. The MN4069UB has a single-stage gate and therefore a short transient time.
They are equivalent to MOTOROLA MC14069UB and RCA CD4069UB.

P-1

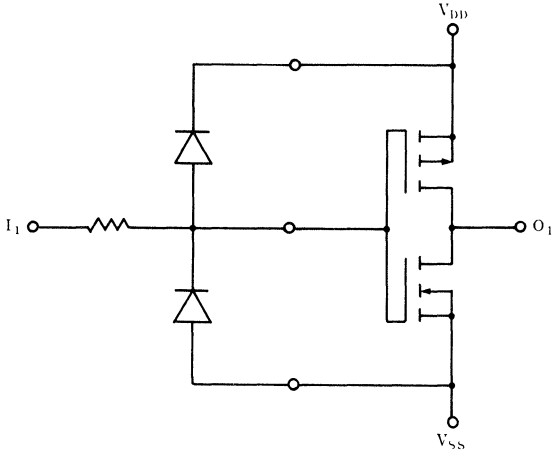


14-Pin • Plastic DIL Package

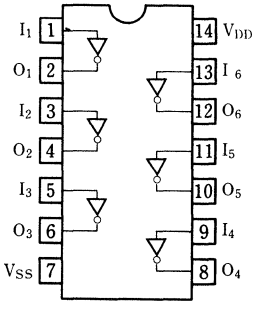
P-2

14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/6) & Input Protection Circuit



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

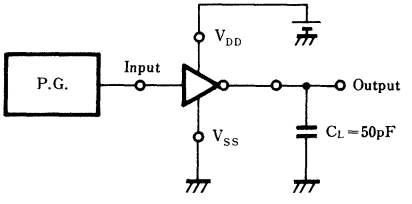
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		| I_O | <1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		| I_O | <1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

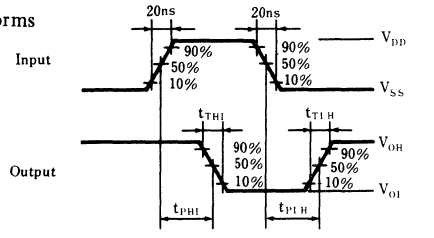
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	40	120	ns
	10		—	20	60	
	15		—	15	45	
Propagation Delay Time	5	t_{PHL}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



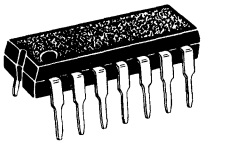
MN4071B / MN4071BS

Quad 2-Input OR Gates

■ Description

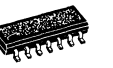
The MN4071B/S are positive 2-input OR gates and have 4 circuits in a package.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
The MN4071B/S are equivalent to MOTOROLA MC14071B and RCA CD4071B.

P-1



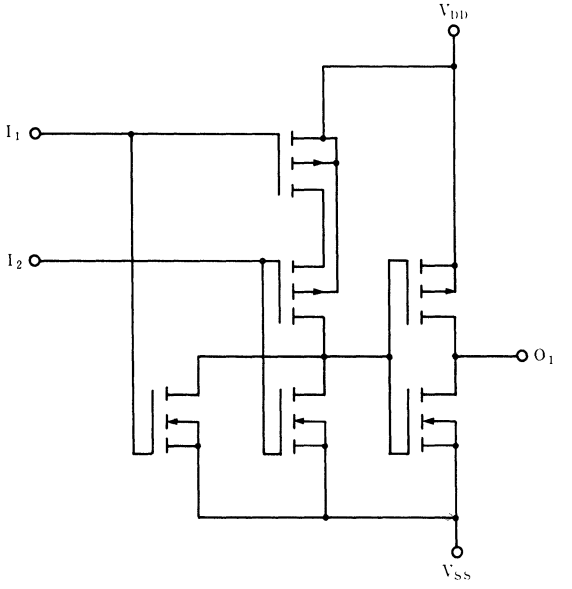
14-Pin • Plastic DIL Package

P-2

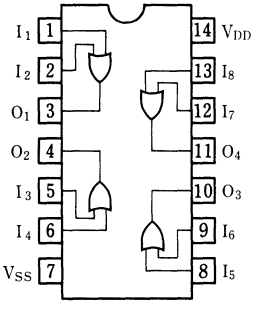


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/4)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

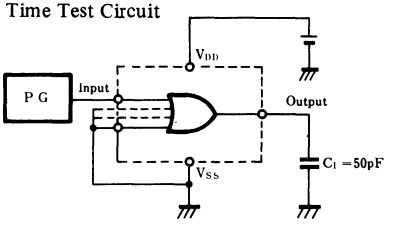
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

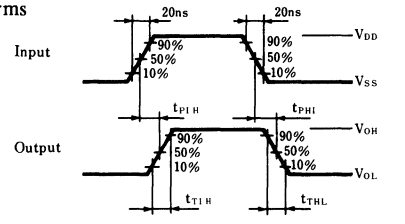
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	55	165	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time	5	t_{PHL}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



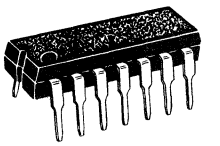
MN4072B / MN4072BS

Dual 4-Input OR Gates

■ Description

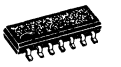
The MN4072B/S are positive 4-input OR gates and have 2 circuits in a package.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
The MN4072B/S are equivalent to MOTOROLA MC14072B and RCA CD4072B.

P-1



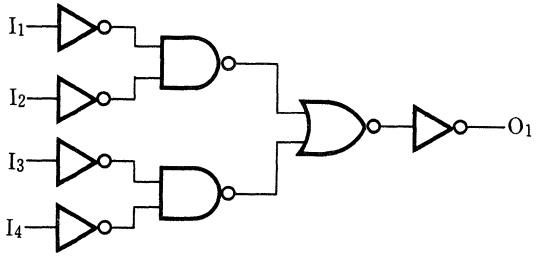
14-Pin • Plastic DIL Package

P-2

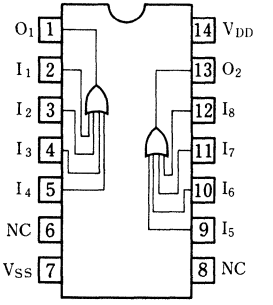


14-Pin • Panaflat Package (SO-14D)

■ Logic Diagram (1/2)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

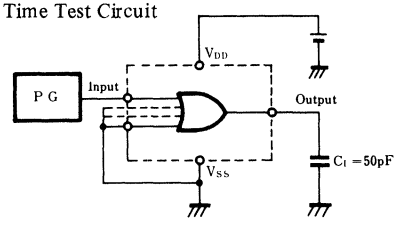
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

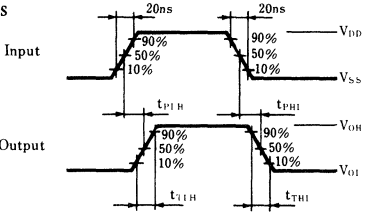
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	75	225	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time	5	t_{PHL}	—	80	240	ns
	10		—	35	105	
	15		—	25	75	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



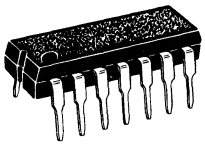
MN4073B / MN4073BS

Triple 3-Input AND Gates

■ Description

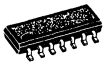
The MN4073B/S are positive 3-input AND gates and have 3 circuits in a package.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
The MN4073B/S are equivalent to MOTOROLA MN14073B and RCA CD4073B.

P-1



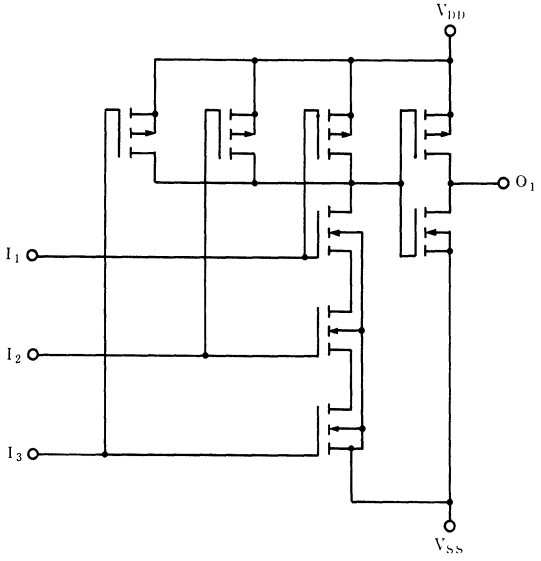
14-Pin • Plastic DIL Package

P-2

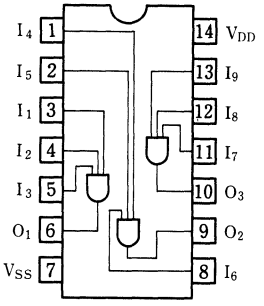


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/3)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

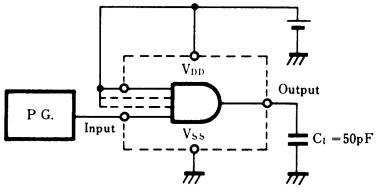
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

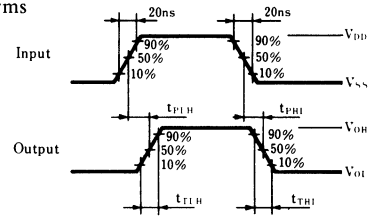
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	55	165	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time	5	t_{PHL}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



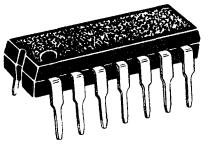
MN4075B/MN4075BS

Triple 3-Input OR Gates

■ Description

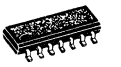
The MN4075B/S are positive 3-input OR gates and have 3 circuits in a package.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
The MN4075B/S are equivalent to MOTOROLA MC14075B and RCA CD4075B.

P-1



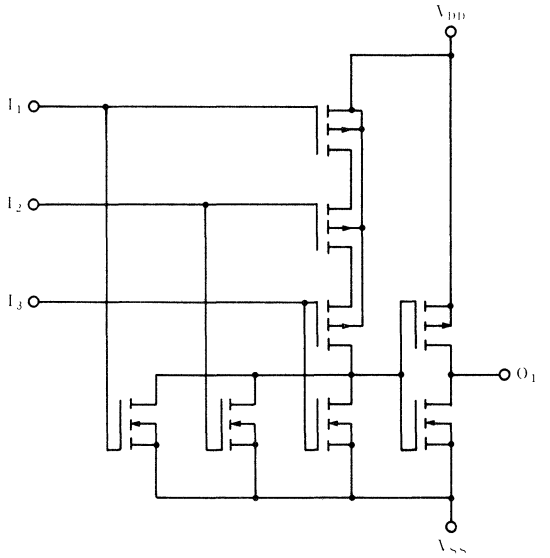
14-Pin • Plastic DIL Package

P-2

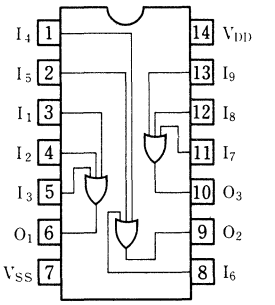


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/3)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

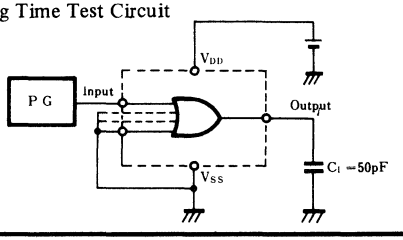
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

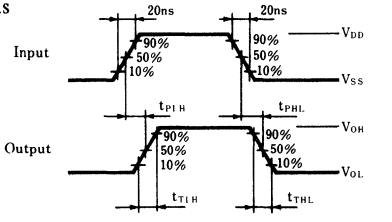
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	65	195	ns
	10		—	30	90	
	15		—	25	75	
Propagation Delay Time	5	t_{PHL}	—	65	195	ns
	10		—	30	90	
	15		—	20	60	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



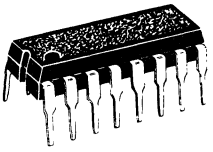
MN4076B / MN4076BS

4-Bit D-Type Registers

■ Description

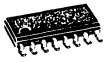
The MN4076B/S are 4-bits registers composed of quad D-type flip-flops with tristate outputs and controlled by the common clock and reset inputs.
All inputs ($D_0 \sim D_3$) are stored in four flip-flops on the positive going edge of the clock, when the data enable inputs ($\overline{EO}_0$, $\overline{ED}_1$) are Low.
In other combinations of the data enable inputs, 4 flip-flops hold the previous stage even after the going edge of the clock.
When output enable inputs ($\overline{EO}_0$, $\overline{EO}_1$) are Low, each flip-flop's outputs are from $O_0 \sim O_3$.
In other combinations of the output enable inputs, all outputs are High impedance.
A High on the reset input makes outputs Low asynchronously.
The MN4076B/S are equivalent to MOTOROLA MN14076B and RCA CD4076B.

P-3



16-Pin • Plastic DIL Package

P-4



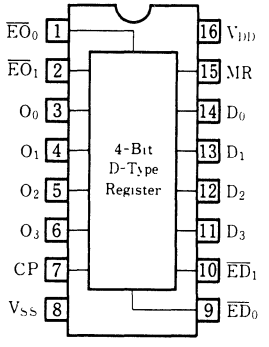
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

Input							Output
MR	CP	$\overline{ED}_0$	$\overline{ED}_1$	D_0	$\overline{EO}_0$	$\overline{EO}_1$	O_{0n+1}
	×	×	×	×	H	×	Z
×	×	×	×	×	×	H	Z
H	×	×	×	×	L	L	L
L	↓	H	×	×	L	L	no change
L	↓	×	H	×	L	L	no change
L	↓	L	L	H	L	L	H
L	↓	L	L	L	L	L	L
L	↑	×	×	×	L	L	no change
L	×	×	×	×	L	L	no change

Note) X : don't care
Z : high impedance

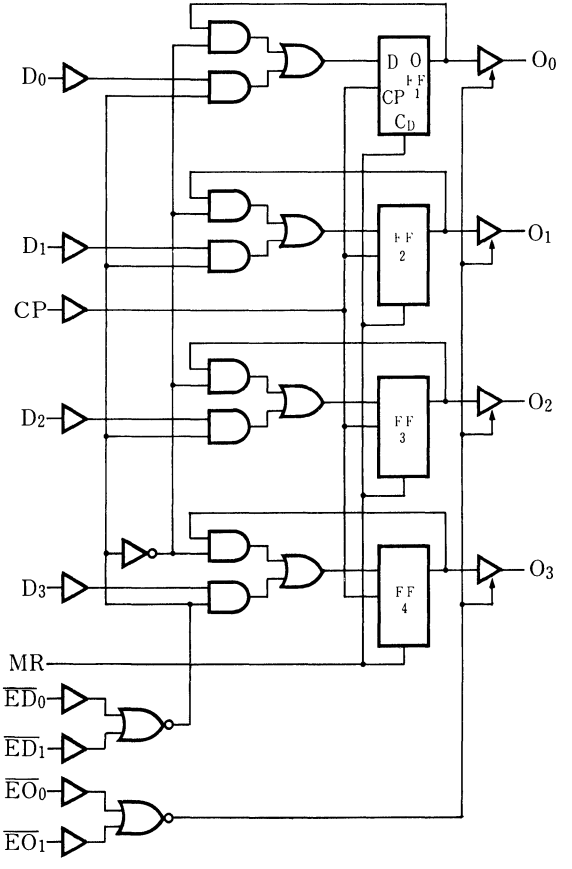
Pin Configuration



Pin Explanation

$D_0 \sim D_3$: Data input (4 Bits)
$\overline{ED}_0$, $\overline{ED}_1$: Data enable input
$\overline{EO}_0$, $\overline{EO}_1$: Output enable input
CP : Clock input
MR : Reset input
$O_0 \sim O_3$: Data output (4 Bits)

■ Logic Diagram



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA
3-State Output Pin: Leakage Current High Level	15	I_{OZH}	V_O=V_{DD}	—	1.6	—	1.6	—	12	μA
3-State Output Pin: Leakage Current Low Level	15	$-I_{OZL}$	V_O=V_{SS}	—	1.6	—	1.6	—	12	

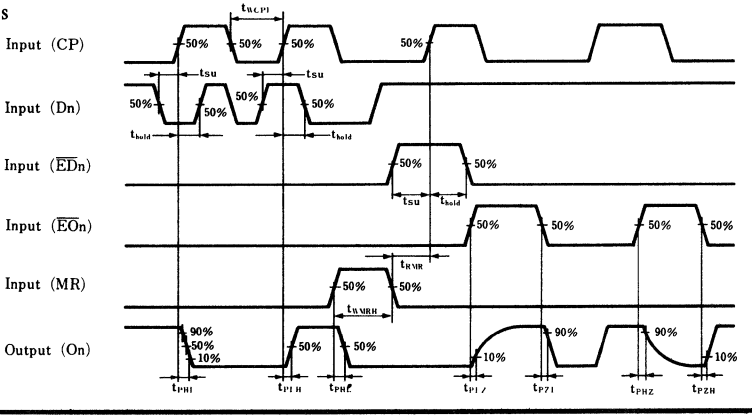
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	150	450	ns
	10		—	60	180	
	15		—	45	135	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	160	480	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time MR→On (H→L)	5	t_{PHL}	—	95	285	ns
	10		—	40	120	
	15		—	30	90	

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
High Level Output Disable Time $\overline{EO}n \rightarrow On$ (H)	5	t_{PHZ}	—	50	150	ns
	10		—	35	105	
	15		—	30	90	
Low Level Output Disable Time $\overline{EO}n \rightarrow On$ (L)	5	t_{PLZ}	—	45	135	ns
	10		—	30	90	
	15		—	30	90	
High Level Output Enable Time $\overline{EO}n \rightarrow On$ (H)	5	t_{PZH}	—	65	195	ns
	10		—	30	90	
	15		—	20	60	
Low Level Output Enable Time $\overline{EO}n \rightarrow On$ (L)	5	t_{PZL}	—	60	180	ns
	10		—	25	75	
	15		—	20	60	
Set-up Time Dn→CP	5	t_{su}	—	−15	10	ns
	10		—	−10	0	
	15		—	− 5	0	
Set-up Time $\overline{ED}n \rightarrow CP$	5	t_{su}	—	−50	0	ns
	10		—	−20	0	
	15		—	−15	0	
Hold Time Dn→CP	5	t_{hold}	—	30	55	ns
	10		—	10	20	
	15		—	10	15	
Hold Time $\overline{ED}n \rightarrow CP$	5	t_{hold}	—	−25	25	ns
	10		—	−10	10	
	15		—	− 5	5	
Low Level Minimum Clock Pulse Width	5	t_{WCPL}	—	60	180	ns
	10		—	20	60	
	15		—	15	45	
High Level Minimum MR Pulse Width	5	t_{WMRH}	—	25	75	ns
	10		—	15	45	
	15		—	10	30	
Maximum Clock Frequency	5	fmax.	4	8	—	MHz
	10		11	22	—	
	15		16	32	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



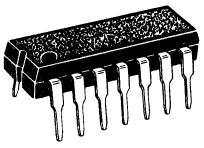
MN4078B/MN4078BS

8-Input NOR Gates

■ Description

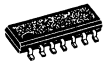
The MN4078B/S are positive 8-input NOR gates.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
The MN4078B/S are equivalent to MOTOROLA MC14078B and RCA CD4078B.

P-1



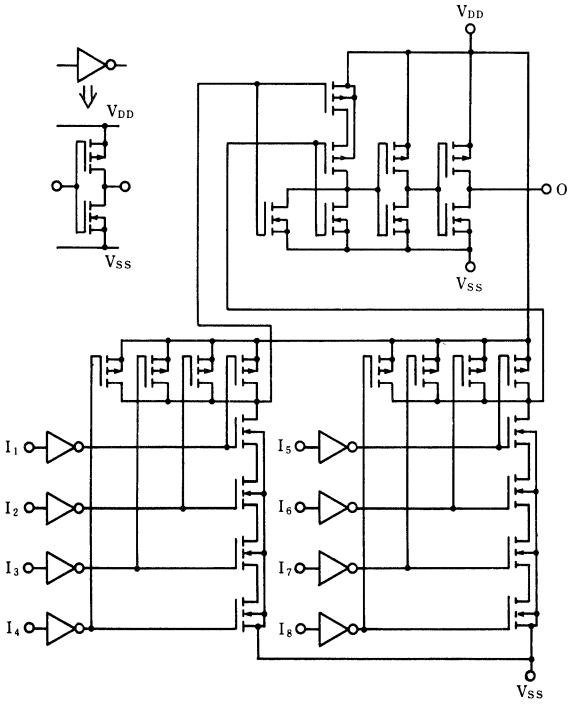
14-Pin • Plastic DIL Package

P-2

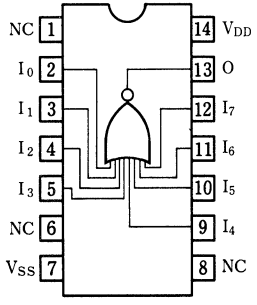


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

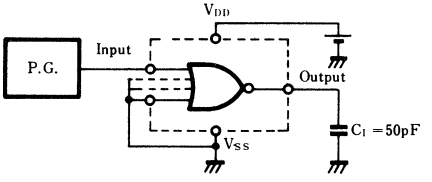
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	1	—	1	—	7.5	μA
	10				—	2	—	2	—	15	
	15				—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

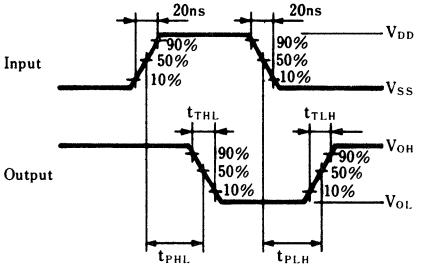
■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	80	240	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time	5	t_{PHL}	—	80	240	ns
	10		—	35	105	
	15		—	25	75	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



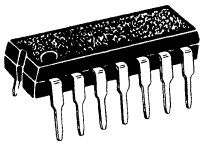
MN4081B / MN4081BS

Quad 2-Input AND Gates

■ Description

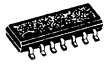
The MN4081B/S are positive 2-input AND gates and have 4 circuits in a package.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
The MN4081B/S are equivalent to MOTOROLA MC14081B and RCA CD4081B.

P-1



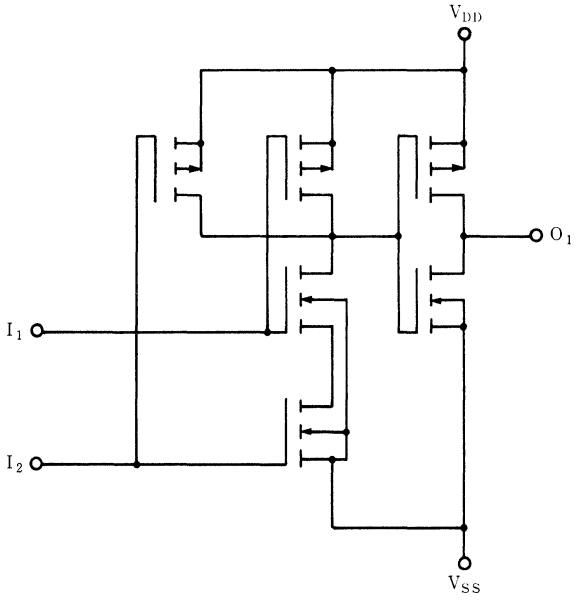
14-Pin • Plastic DIL Package

P-2

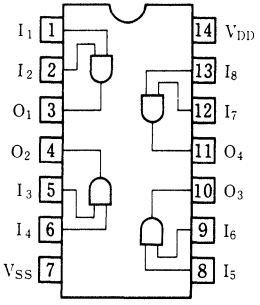


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/4)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

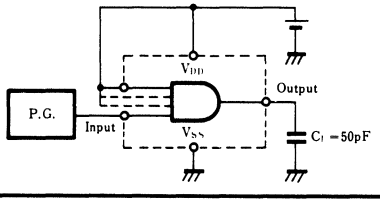
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

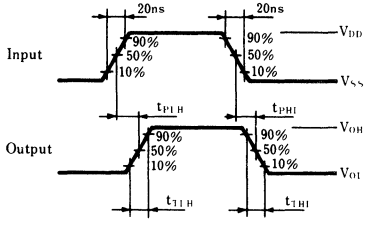
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	
Propagation Delay Time	5	t_{PHL}	—	55	165	ns
	10		—	25	75	
	15		—	20	60	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



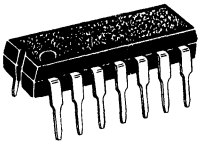
MN4082B/MN4082BS

Dual 4-Input AND Gates

■ Description

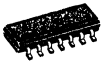
The MN4082B/S are dual 4-input AND gates.
The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.
The MN4082B/S are equivalent to MOTOROLA MC14082B and RCA CD4082B.

P-1



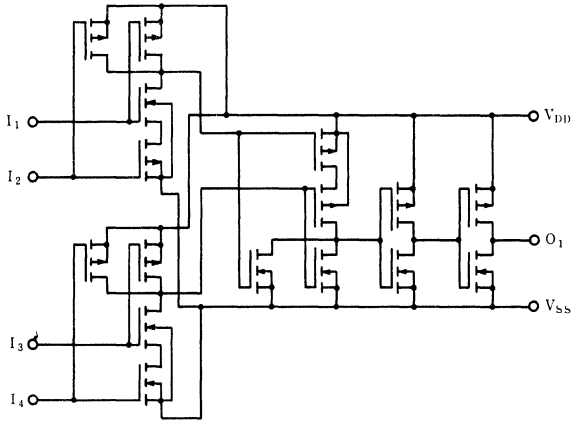
14-Pin • Plastic DIL Package

P-2

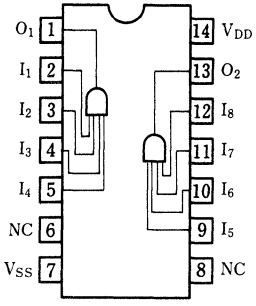


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/2)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

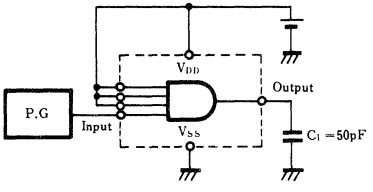
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		| I_O | <1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		| I_O | <1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

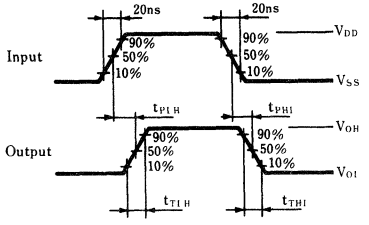
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	65	195	ns
	10		—	30	90	
	15		—	25	75	
Propagation Delay Time	5	t_{PHL}	—	65	195	ns
	10		—	30	90	
	15		—	25	75	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



MN4085B / MN4085BS

Dual 2-Wide 2-Input AND-OR-Invert Gates

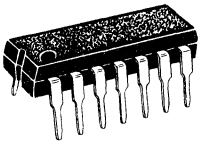
■ Description

The MN4085B/S are dual 2-wide 2-input AND-OR-inverters.
Their circuit is composed of two 2-input AND gates and a NOR gate.
Its logical expressions are

$$O_A = \overline{A_0 \cdot A_1 + A_2 \cdot A_3 + A_4}$$
$$O_B = \overline{B_0 \cdot B_1 + B_2 \cdot B_3 + A_4}$$

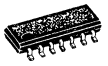
A High on the A_4, B_4 inputs inhibits the selecting action and force the outputs Low.
The MN4085B/S can be used where low power dissipation and high noise immunity is desired. The MN4085B is equivalent to RCA CD4085B.

P-1



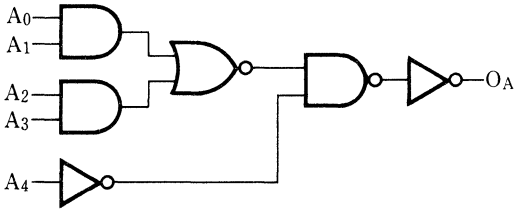
14-Pin • Plastic DIL Package

P-2

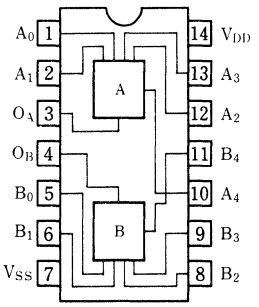


14-Pin • Panaflat Package (SO-14D)

■ Logic Diagram (1/2)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

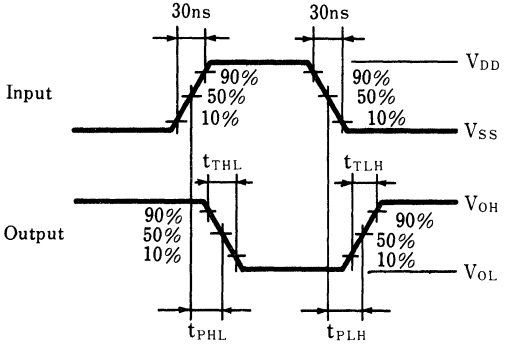
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	65	195	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PHL}	—	75	225	ns
	10		—	30	90	
	15		—	20	60	
Input Capacitance		C_I	—	—	7.5	pF

- Switching Time Test Circuit and Waveform

1. Measurement Condition

Test No.	Input Condition				
	A_0	A_1	A_2	A_3	A_4
1	P.G.	H	L	L	L
2	H	P.G.	L	L	L
3	L	L	P.G.	H	L
4	L	L	H	P.G.	L
5	P.G.	P.G.	P.G.	P.G.	L
6	L	L	L	L	P.G.

2. Waveforms



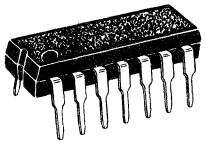
MN4086B / MN4086BS

Expandable 4-Wide 2-Input AND-OR-Invert Gates

■ Description

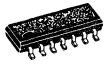
The MN4086B/S are AND-OR select gates composed of four 2-input AND gates, an OR gate and an expansion input. Output can be obtained by inversion.

P-1



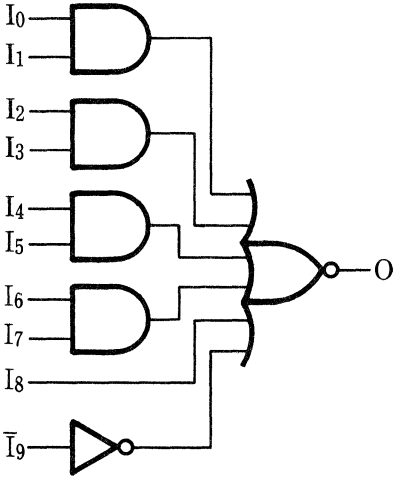
14-Pin • Plastic DIL Package

P-2

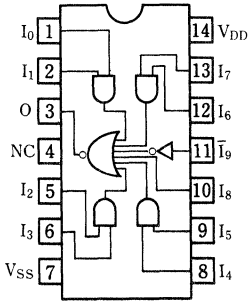


14-Pin • Panaflat Package (SO-14D)

■ Logic Diagram



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	1	—	1	—	7.5	μA
	10				—	2	—	2	—	15	
	15				—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

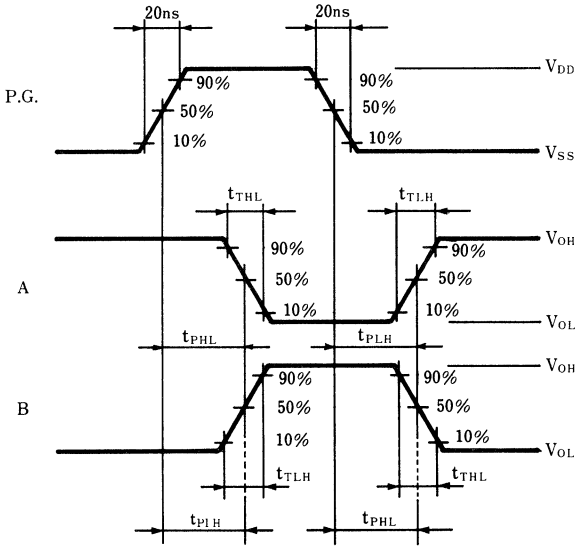
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time I_0~I_7→O (H→L)	5	t_{PHL}	—	90	270	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time I_0~I_7→O (L→H)	5	t_{PLH}	—	80	240	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time I_8→O (H→L)	5	t_{PHL}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time I_8→O (L→H)	5	t_{PLH}	—	55	165	ns
	10		—	20	60	
	15		—	15	45	

■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$) (Continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Propagation Delay Time $\overline{I_9}\rightarrow O$ (H→L)	5	t_{PHL}	—	55	165	ns
	10		—	20	60	
	15		—	15	45	
Propagation Delay Time $\overline{I_9}\rightarrow O$ (L→H)	5	t_{PLH}	—	45	135	ns
	10		—	15	45	
	15		—	10	30	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms

	Input Condition					
	I_0, I_1	I_2, I_3	I_4, I_5	I_6, I_7	I_8	$\overline{I_9}$
A	P.G.	L	L	L	L	H
	L	P.G.	L	L	L	H
	L	L	P.G.	L	L	H
	L	L	L	P.G.	L	H
	L	L	L	L	P.G.	H
B	L	L	L	L	L	P.G.



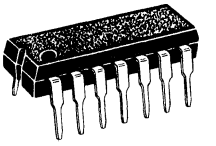
MN4093B / MN4093BS

Quad 2-Input NAND Schmitt Triggers

■ Description

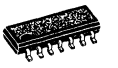
The MN4093B/S are quad 2-input NANDs with inputs which have the schmitt trigger function.
They are used for applications such as line drivers, reforming signals, multi-vibrators and so on because the two thresholds (V_{IH}, V_{IL}) are different for the rising and the falling edges of the input signal.
They have same pin outputs and may be replaced by the MN4011B.
The MN4093B/S are equivalent to MOTOROLA MC14093B and RCA CD4093B.

P-1



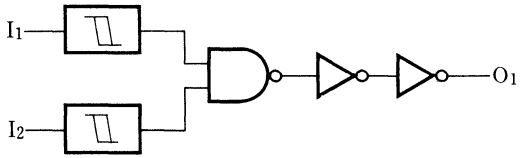
14-Pin • Plastic DIL Package

P-2

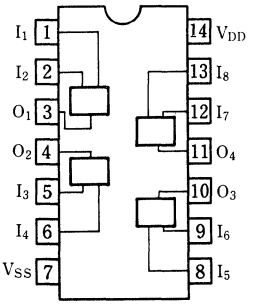


14-Pin • Panaflat Package (SO-14D)

■ Schematic Diagram (1/4)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		| I_O | <1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		| I_O | <1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

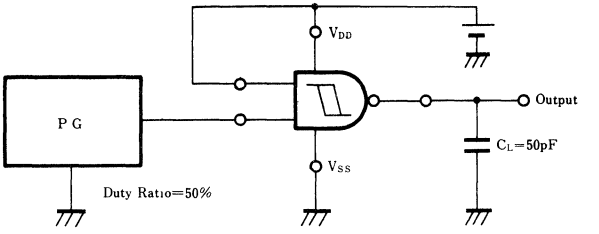
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time (Fig. 1)	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time (Fig. 1)	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time (Fig. 1)	5	t_{PLH}	—	85	255	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time (Fig. 1)	5	t_{PHL}	—	90	270	ns
	10		—	40	120	
	15		—	30	90	
Threshold Voltage (Fig. 2)	5	V_{IH}	—	2.9	3.5	V
	10		—	5.2	7	
	15		—	7.3	11	
Threshold Voltage (Fig. 2)	5	V_{IL}	1.5	2.2	—	V
	10		3	4.2	—	
	15		4	6	—	

■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$) (continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Hysteresis Voltage (Fig. 2)	5	V_H	0.4	0.7	—	V
	10		0.6	1	—	
	15		0.7	1.3	—	
Input Capacitance		C_I	—	—	7.5	pF

Fig. 1 Switching Time Test Circuit and Waveforms

1. Test Circuit



2. Waveforms

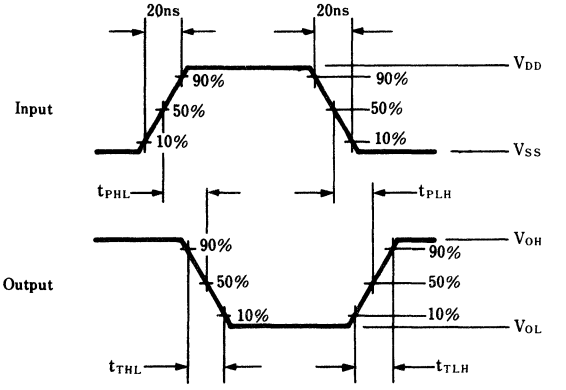
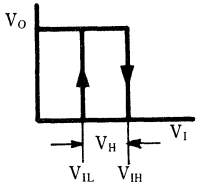
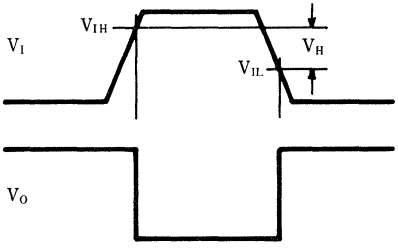


Fig. 2 Transfer Characteristics



Transfer Characteristics



The upper waveform shows its definition rating 30%, to 70% limit

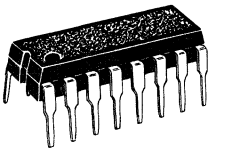
MN4094B / MN4094BS

8-Stage Shift-and-Store Bus Registers

■ Description

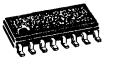
The MN4094B/S are shift-and-store bus registers composed of an 8-bit shift register and an 8-bit latch.
The data read-in to the shift register can be taken into the latch by asynchronous strobe input, and output can be held in the data transfer mode.
Directly connected to an 8-bit bus line since the parallel output is 3-state construction.
They are suitable for series-parallel converters and data receivers. ceiver.

P-3



16-Pin • Plastic DIL Package

P-4



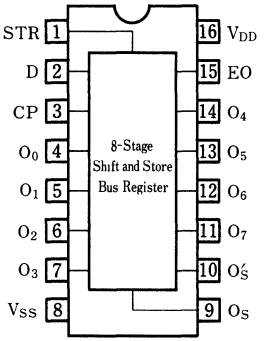
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

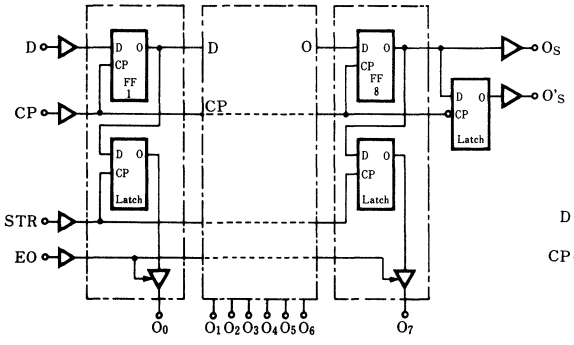
Input				Parallel Output		Serial Output	
CP	EO	STR	D	O_0	O_n	O_S	O'_S
↑	L	×	×	Z	Z	O'_6	nc
↓	L	×	×	Z	Z	nc	O_7
↑	H	L	×	nc	nc	O'_6	nc
↑	H	H	L	L	O_{n-1}	O'_6	nc
↑	H	H	H	H	O_{n-1}	O'_6	nc
↓	H	H	H	nc	nc	nc	O_7

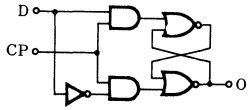
Note) X : don't care
Z : high impedance
nc : no change
O'_6 : 7-stage shift register mode

Pin Configuration



■ Logic Diagram





(One latch)

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA
3-State Output Pin: Leakage Current High Level	15	I_{OZH}	V_O=V_{DD}		—	1.6	—	1.6	—	12	μA
3-State Output Pin: Leakage Current Low Level	15	$-I_{OZL}$	V_O=V_{SS}		—	1.6	—	1.6	—	12	

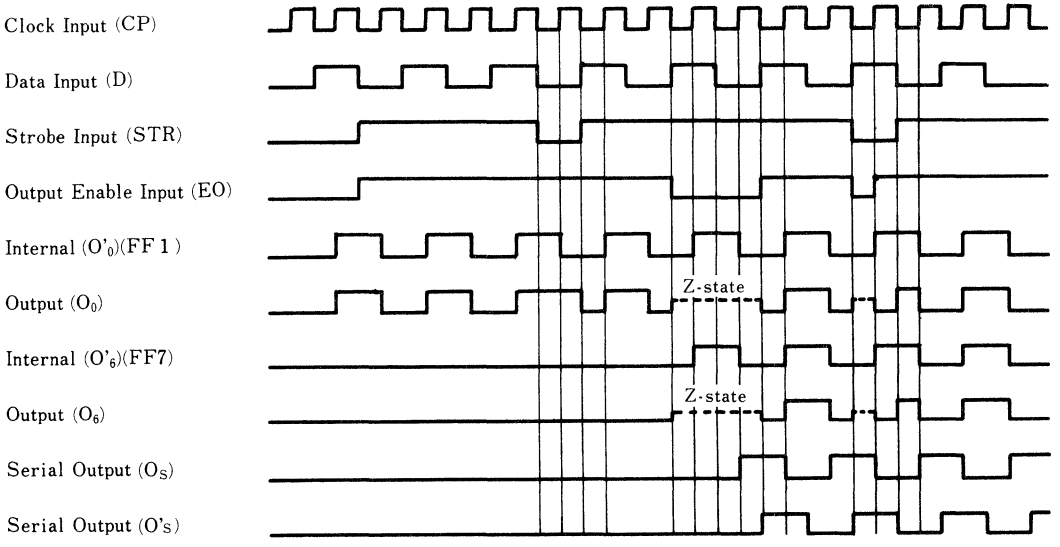
■ **Switching Characteristics** (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→Os (H→L)	5	t_{PHL}	—	135	405	ns
	10		—	65	195	
	15		—	50	150	
Propagation Delay Time CP→Os (L→H)	5	t_{PLH}	—	105	315	ns
	10		—	50	150	
	15		—	40	120	
Propagation Delay Time MR→O's (H→L)	5	t_{PHL}	—	105	315	ns
	10		—	50	150	
	15		—	40	120	
Propagation Delay Time MR→O's (L→H)	5	t_{PLH}	—	105	315	ns
	10		—	50	150	
	15		—	40	120	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	165	495	ns
	10		—	75	225	
	15		—	55	165	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	150	450	ns
	10		—	70	210	
	15		—	55	165	
Propagation Delay Time STR→On (H→L)	5	t_{PHL}	—	110	330	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time STR→On (L→H)	5	t_{PLH}	—	100	300	ns
	10		—	45	135	
	15		—	35	105	
High Level Output Disable Time EO→On (H)	5	t_{PHZ}	—	75	225	ns
	10		—	40	120	
	15		—	30	90	
Low Level Output Disable Time EO→On (L)	5	t_{PLZ}	—	80	240	ns
	10		—	40	120	
	15		—	30	90	
High Level Output Enable Time EO→On (H)	5	t_{PZH}	—	40	120	ns
	10		—	25	75	
	15		—	20	60	
Low Level Output Enable Time EO→On (L)	5	t_{PZL}	—	40	120	ns
	10		—	25	75	
	15		—	20	60	
Set-up Time D→CP	5	tsu	—	30	90	ns
	10		—	10	30	
	15		—	5	15	

■ **Switching Characteristics** (Ta = 25℃, V_{SS} = 0V, C_I = 50pF) (continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Hold Time D→CP	5	t_{hold}	—	−15	5	ns
	10		—	5	20	
	15		—	5	20	
Minimum Clock Pulse Width	5	t_{WCPL}	—	20	90	ns
	10		—	15	45	
	15		—	12	36	
Minimum Strobe Pulse Width	5	t_{WSTRH}	—	20	60	ns
	10		—	15	45	
	15		—	12	36	
Maximum Clock Frequency	5	fmax	5	10	—	MHz
	10		11	22	—	
	15		14	28	—	
Input Capacitance		C_I	—	—	7.5	pF

■ **Timing Diagram**



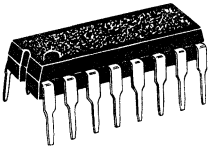
MN4502B / MN4502BS

Hex Strobed Inverting Buffers

■ Description

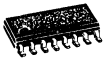
The MN4502B/S are 3-state output inverting buffers with a strobe terminal, and can drive 1 TTL in the 74 series.

P-3



16-Pin • Plastic DIL Package

P-4



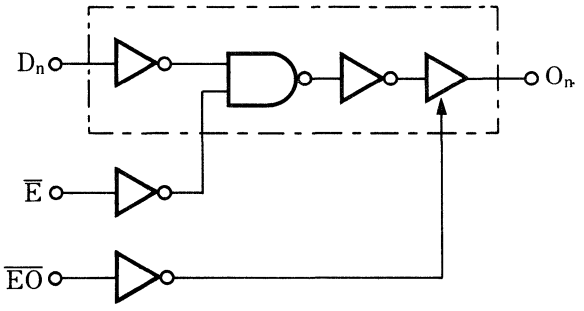
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

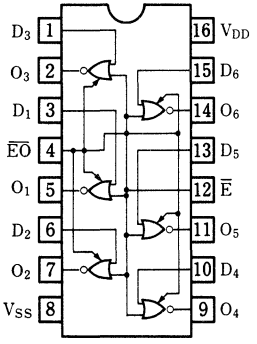
Input			Output
D_n	$\overline{E}$	$\overline{EO}$	O_n
L	L	L	H
H	L	L	L
×	H	L	L
×	×	H	Z

Note) X : don't care
Z : high impedance

■ Logic Diagram (1/6)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Input Current		$\pm I_I$	max. 10	mA
Output Current		$\pm I_I$	max. 30	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	4	—	4	—	30	μA
	10			—	8	—	8	—	60	
	15			—	16	—	16	—	120	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		| I_O | <1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		| I_O | <1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	4.75	I_{OL}	V_O=0.4V, V_I=0 or 5V	3.5	—	2.9	—	2.3	—	mA
	10		V_O=0.5V, V_I=0 or 10V	12	—	10	—	8	—	
	15		V_O=1.5V, V_I=0 or 15V	24	—	20	—	16	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	1.2	—	1	—	0.8	—	mA
	10		V_O=9.5V, V_I=0 or 10V	3.8	—	3.2	—	2.5	—	
	15		V_O=13.5V, V_I=0 or 15V	12	—	10	—	8	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	3.8	—	3.2	—	2.5	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA
3-State Output Pin: Leakage Current High Level	15	I_{OZH}	V_O=V_{DD}	—	1.6	—	1.6	—	12	μA
3-State Output Pin: Leakage Current Low Level	15	$-I_{OZL}$	V_O=V_{SS}	—	1.6	—	1.6	—	12	

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

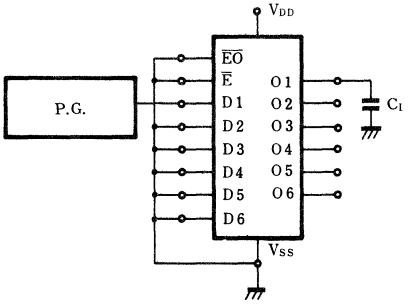
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	30	90	ns
	10		—	15	45	
	15		—	12	36	
Output Fall Time	5	t_{THL}	—	25	75	ns
	10		—	12	36	
	15		—	8	24	
Propagation Delay Time Dn, $\overline{E}$→On (H→L)	5	t_{PHL}	—	85	255	ns
	10		—	40	120	
	15		—	35	105	
Propagation Delay Time Dn, $\overline{E}$→On (L→H)	5	t_{PLH}	—	80	240	ns
	10		—	35	105	
	15		—	30	90	
High Level Output Disable Time $\overline{EO}$→On (H)	5	t_{PHZ}	—	60	180	ns
	10		—	55	165	
	15		—	55	165	

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

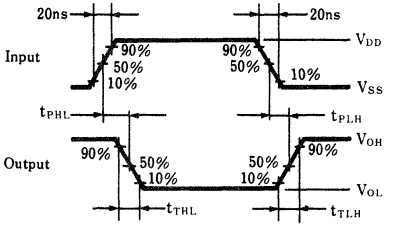
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Low Level Output Disable Time $\overline{EO}$→On (L)	5	t_{PLZ}	—	50	150	ns
	10		—	35	105	
	15		—	30	90	
High Level Output Enable Time $\overline{EO}$→On (H)	5	t_{PZH}	—	60	180	ns
	10		—	35	105	
	15		—	30	90	
Low Level Output Enable Time $\overline{EO}$→On (L)	5	t_{PZL}	—	55	165	ns
	10		—	25	75	
	15		—	20	60	
Input Capacitance		C_I	—	—	7.5	pF

• Switching Time Test Circuit and Waveforms

1. Test Circuit



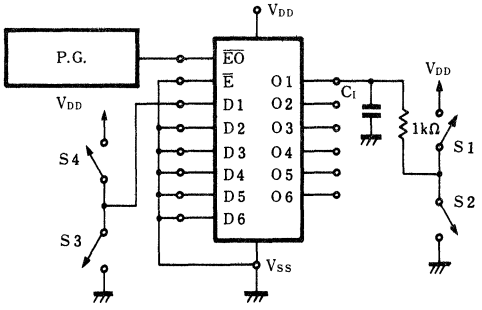
2. Waveforms



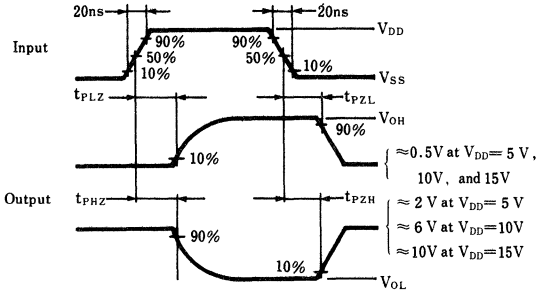
• 3-State Test Circuit and Waveforms

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

1. Test Circuit



2. Waveforms



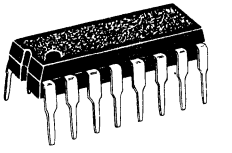
MN4503B / MN4503BS

Hex Non-Inverting 3-State Buffers

■ Description

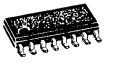
The MN4503B/S are non-inverting tristate buffers which have a high current source and sink capability. There are two disable inputs (EO_2, EO_4) which enable control of 2 or 4 circuits independently. A High on the EO_4 makes outputs 1 through 4 High impedance, and the EO_2 makes outputs 5, 6 High impedance.
MN4503B/S are equivalent to MOTOROLA MC14503B.

P-3



16-Pin • Plastic DIL Package

P-4



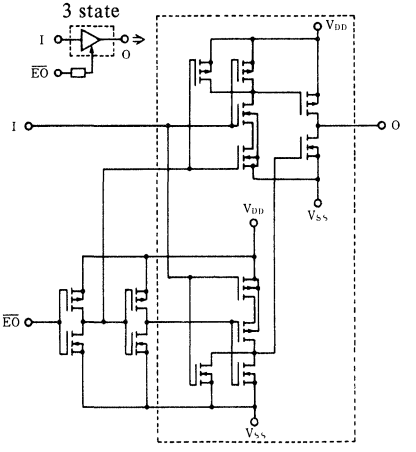
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

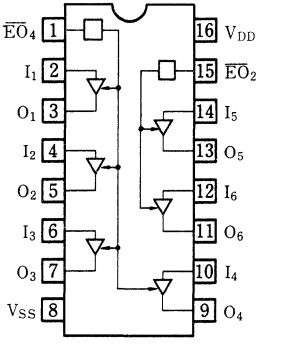
Input		Output
I	$\overline{EO}$	O
L	L	L
H	L	H
×	H	Z

Note) X: don't care; Z: high impedance (OFF mode)

■ Schematic Diagram (3 state 1/6)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 25	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	4	—	4	—	30	μA
	10			—	8	—	8	—	60	
	15			—	16	—	16	—	120	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	4.75	I_{OL}	V_O=0.4V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
	10		V_O=0.5V, V_I=0 or 10V	4.8	—	4	—	3.2	—	
	15		V_O=1.5V, V_I=0 or 15V	12	—	10	—	8	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	1	—	0.88	—	0.7	—	mA
	10		V_O=9.5V, V_I=0 or 10V	2.4	—	2.2	—	1.8	—	
	15		V_O=13.5V, V_I=0 or 15V	6.6	—	6	—	4.8	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA
3-State Output Pin: Leakage Current High Level	15	I_{OZH}	V_O=V_{DD}	—	1.6	—	1.6	—	12	μA
3-State Output Pin: Leakage Current Low Level	15	$-I_{OZL}$	V_O=V_{SS}	—	1.6	—	1.6	—	12	

Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time (Fig. 1)	5	t_{TLH}	—	35	105	ns
	10		—	20	60	
	15		—	15	45	
Output Fall Time (Fig. 1)	5	t_{THL}	—	30	90	ns
	10		—	15	45	
	15		—	10	30	
Propagation Delay Time (Fig. 1)	5	t_{PLH}	—	60	180	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time (Fig. 1)	5	t_{PHL}	—	70	210	ns
	10		—	30	90	
	15		—	25	75	
3-State Propagation Delay Time O (H) → High Impedance (Fig. 2)	5	t_{PHZ}	—	45	135	ns
	10		—	35	105	
	15		—	30	90	
3-State Propagation Delay Time O (L) → High Impedance (Fig. 3)	5	t_{PLZ}	—	60	180	ns
	10		—	35	105	
	15		—	25	75	

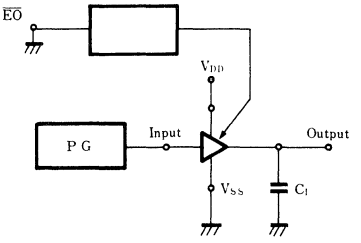
■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$) (continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
3-State Propagation Delay Time High Impedance → O (H) (Fig. 2)	5	t_{PZH}	—	75	225	ns
	10		—	35	105	
	15		—	30	90	
3-State Propagation Delay Time High Impedance → O (L) (Fig. 3)	5	t_{PZL}	—	95	285	ns
	10		—	40	120	
	15		—	30	90	
Imput Capacitance		C_I	—	—	7.5	pF

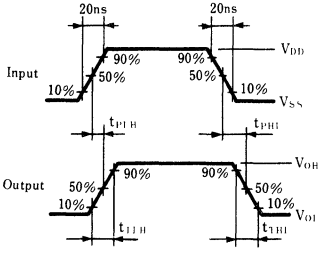
• Switching Time Test Circuit and Waveforms

(Fig. 1) t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Test Circuit

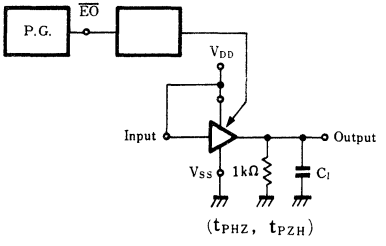


2. Waveforms

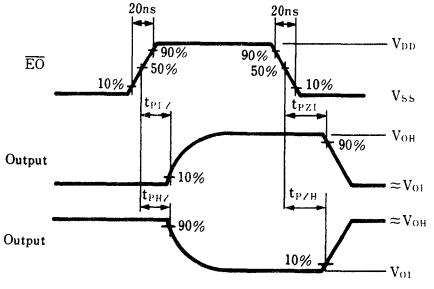


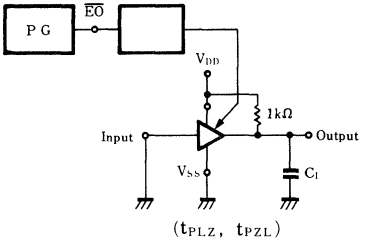
(Fig. 2) t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL}

1. Test Circuit



2. Waveforms





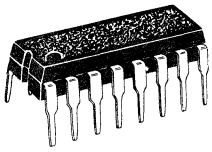
MN4510B / MN4510BS

BCD Up/Down Counters

■ Description

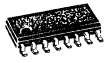
The MN4510B/S are BCD up/down counters composed of a gate circuit with the function of D-flip-flop 4-stage and T-flip-flop.
The counter is cleared when MR is "H". High speed operation is possible due to internal synchronization.
The MN4510B/S are suitable for up/down counters, frequency synthesizers which need low power dissipation and high noise immunity, and also for A/D and D/A converters.
They are equivalent to MOTOROLA MC14510B and RCA CD4510B.

P-3



16-Pin • Plastic DIL Package

P-4

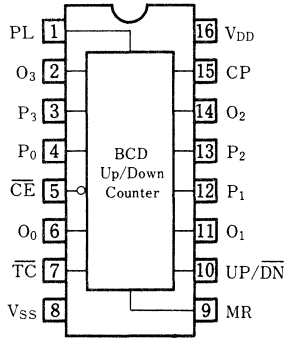


16-Pin • Panaflat Package (SO-16D)

■ Truth Table

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	Mode
L	H	×	×	×	load
L	L	×	H	×	no change
L	L	L	L	⎍	count down
L	L	H	L	⎍	count up
H	×	×	×	×	leset

Pin Configuration



■ Maximum Ratings (Ta=25℃)

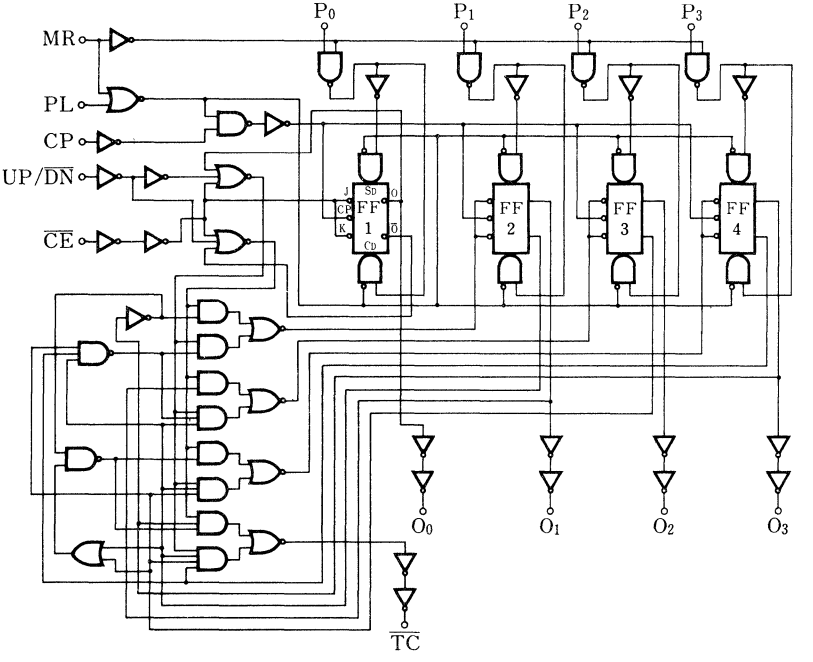
Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

■ Logic Diagram



■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

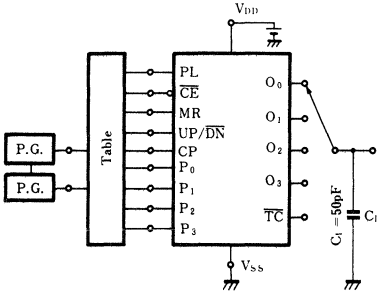
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	155	465	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time CP→$\overline{TC}$ (H→L)	5	t_{PHL}	—	260	780	ns
	10		—	105	315	
	15		—	75	225	
Propagation Delay Time CP→$\overline{TC}$ (L→H)	5	t_{PLH}	—	180	540	ns
	10		—	75	225	
	15		—	55	165	
Propagation Delay Time PL→On (H→L)	5	t_{PHL}	—	125	375	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time PL→On (L→H)	5	t_{PLH}	—	170	510	ns
	10		—	70	210	
	15		—	50	150	
Propagation Delay Time PL→$\overline{TC}$ (H→L)	5	t_{PHL}	—	250	750	ns
	10		—	110	330	
	15		—	80	240	
Propagation Delay Time PL→$\overline{TC}$ (L→H)	5	t_{PLH}	—	250	750	ns
	10		—	110	330	
	15		—	80	240	
Propagation Delay Time $\overline{CE}$→$\overline{TC}$ (H→L)	5	t_{PHL}	—	165	495	ns
	10		—	65	195	
	15		—	50	150	
Propagation Delay Time $\overline{CE}$→$\overline{TC}$ (L→H)	5	t_{PLH}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Propagation Delay Time MR→On, $\overline{TC}$ (H→L)	5	t_{PHL}	—	205	615	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time MR→$\overline{TC}$ (L→H)	5	t_{PLH}	—	225	675	ns
	10		—	75	225	
	15		—	50	150	
Minimum Clock Pulse Width	5	t_{WCPL}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	

■ **Switching Characteristics** (Ta=25℃, V_{SS}=0V, C_L=50pF) (continued)

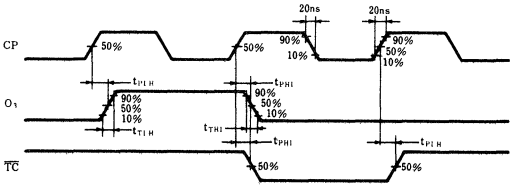
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Minimum PL Pulse Width	5	t_{WPLH}	—	55	165	ns
	10		—	25	75	
	15		—	15	45	
Minimum Reset Pulse Width	5	t_{WMRH}	—	60	180	ns
	10		—	25	75	
	15		—	20	60	
Reset Recovery Time	5	t_{RMR}	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
PL Recovery Time	5	t_{RPL}	—	75	225	ns
	10		—	25	75	
	15		—	15	45	
Set-up Time Pn→PL	5	t_{su}	—	50	150	ns
	10		—	25	75	
	15		—	20	60	
Set-up Time UP/$\overline{DN}$→CP	5	t_{su}	—	125	375	ns
	10		—	50	150	
	15		—	35	105	
Set-up Time $\overline{CE}$→CP	5	t_{su}	—	60	180	ns
	10		—	20	60	
	15		—	10	30	
Hold Time Pn→PL	5	t_{hold}	—	−40	10	ns
	10		—	−20	5	
	15		—	−20	0	
Hold Time UP/$\overline{DN}$→CP	5	t_{hold}	—	−90	35	ns
	10		—	−35	15	
	15		—	−25	15	
Hold Time $\overline{CE}$→CP	5	t_{hold}	—	−40	20	ns
	10		—	−15	5	
	15		—	−10	5	
Maximum Clock Frequency	5	fmax	5	10	—	MHz
	10		12	24	—	
	15		17	34	—	
Input Capacitance		C_I	—	—	7.5	pF

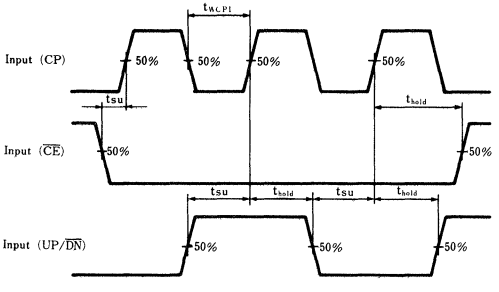
- Switching Time Test Circuit and Waveforms

1. Test Circuit

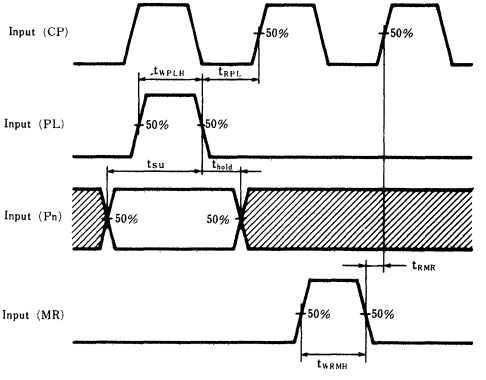


2. Waveforms



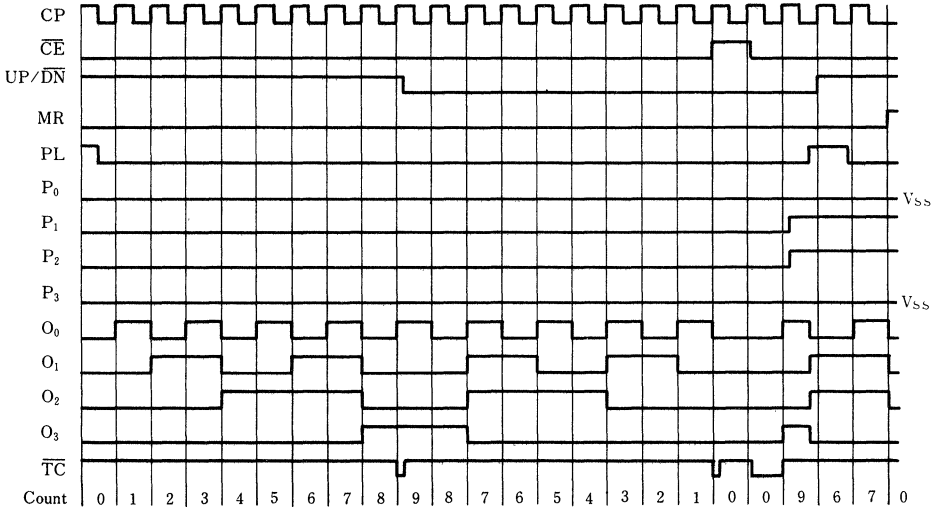


Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP and UP/$\overline{DN}$ to CP



Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for P_n to PL

■ Timing Diagram



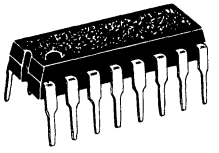
MN4511B/MN4511BS

BCD-to-7-Segment Decoder/Drivers

■ Description

The MN4511B/S are decoder/drivers which convert from 4-bit latch and 4-bit BCD code input to 7-segment output.
Features are lamp test input ($\overline{LT}$) for display tests, blanking input ($\overline{BI}$) to adjust turn-off at pulse drive and brightness, and latch enable input ($\overline{EL}$) to latch BCD input tentatively.
Output is obtained by driving directly or through driver element LED, LCD and fluorescent lamp since an NPN bipolar transistor and N-channel MOS transistor are connected complementarily.
Application examples are measuring equipment, clocks and timers.
They are equivalent to MOTOROLA MC14511B.

P-3

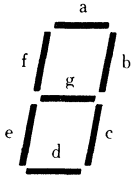


16-Pin • Plastic DIL Package

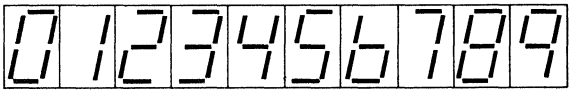
P-4

16-Pin • Panaflat Package (SO-16D)

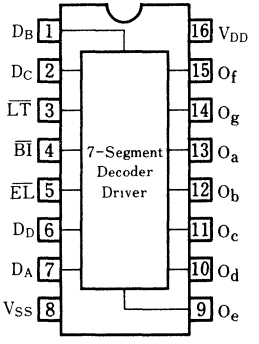
■ Segment Configuration



■ Display



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*1	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*1	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Maximum Output Driving Current		$I_{OH\ max}$	25	mA
Maximum Output Power*2		$P_{OH\ max.}$	50	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* 1 V_{DD}+0.5V should be under 18V * 2 $P_{OH\ max}=I_{OH}(V_{DD}-V_{OH})$

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

■ DC Characteristics (V_{SS}=0V)

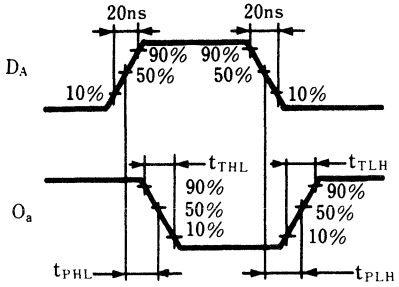
Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Output Driving Voltage	5	V_{OH}	I_{OH}=0mA	4.10	—	4.10	4.40	4.10	—	V
	10			9.10	—	9.10	9.40	9.10	—	
	15			14.10	—	14.10	14.40	14.10	—	
	5	V_{OH}	I_{OH}=5mA	—	—	—	4.30	—	—	V
	10			—	—	—	9.30	—	—	
	15			—	—	—	14.30	—	—	
	5	V_{OH}	I_{OH}=10mA	3.60	—	3.60	4.25	3.30	—	V
	10			8.75	—	8.75	9.25	8.45	—	
	15			13.75	—	13.75	14.25	13.45	—	
	5	V_{OH}	I_{OH}=15mA	—	—	—	4.20	—	—	V
	10			—	—	—	9.20	—	—	
	15			—	—	—	14.20	—	—	
	5	V_{OH}	I_{OH}=20mA	2.80	—	2.80	4.20	2.50	—	V
	10			8.10	—	8.10	9.20	7.80	—	
	15			13.10	—	13.10	14.20	12.80	—	
	5	V_{OH}	I_{OH}=25mA	—	—	—	4.15	—	—	V
	10			—	—	—	9.20	—	—	
	15			—	—	—	14.20	—	—	

■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time (Fig. 1)	5	t_{TLH}	—	18	54	ns
	10		—	11	33	
	15		—	9	27	
Output Fall Time (Fig. 1)	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time (Fig. 1) Dn→On (H→L)	5	t_{PHL}	—	155	465	ns
	10		—	60	180	
	15		—	40	120	
Propagation Delay Time (Fig. 1) Dn→On (L→H)	5	t_{PLH}	—	135	405	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time (Fig. 2) $\overline{EL}$→On (H→L)	5	t_{PHL}	—	160	480	ns
	10		—	60	180	
	15		—	45	135	
Propagation Delay Time (Fig. 2) $\overline{EL}$→On (L→H)	5	t_{PLH}	—	160	480	ns
	10		—	60	180	
	15		—	45	135	
Propagation Delay Time (Fig. 3) $\overline{BI}$→On (H→L)	5	t_{PHL}	—	120	360	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time (Fig. 3) $\overline{BI}$→On (L→H)	5	t_{PLH}	—	105	315	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time (Fig. 4) $\overline{LT}$→On (H→L)	5	t_{PHL}	—	65	195	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time (Fig. 4) $\overline{LT}$→On (L→H)	5	t_{PLH}	—	50	150	ns
	10		—	25	75	
	15		—	20	60	
Minimum EL Pulse Width (Fig. 2)	5	t_{WELL}	—	25	75	ns
	10		—	10	30	
	15		—	8	24	
Set-up Time (Fig. 2) Dn→$\overline{EL}$	5	tsu	—	15	45	ns
	10		—	5	15	
	15		—	5	15	
Hold Time (Fig. 2) Dn→$\overline{EL}$	5	t_{hold}	—	10	30	ns
	10		—	5	15	
	15		—	5	15	
Input Capacitance		C_I	—	—	7.5	pF

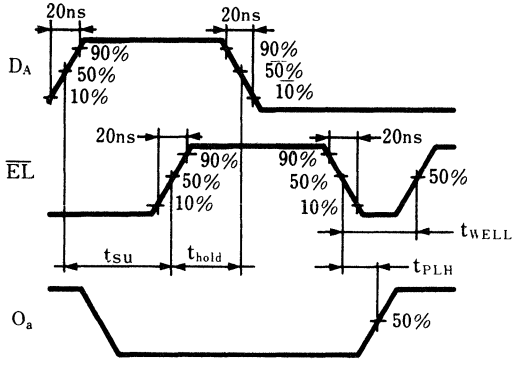
• Dynamic Signal Waveforms

(Fig. 1) t_{TLH}, t_{THL}, t_{PHL} (Dn→On), t_{PLH}(Dn→On)



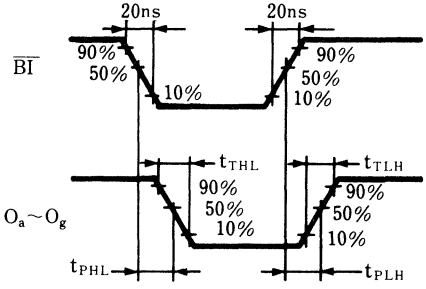
Input D_B, D_C, D_D and $\overline{EL}$= "L"
Input $\overline{BI}$ and $\overline{LT}$= "H"

(Fig. 2) $t_{PHL}(\overline{EL}\rightarrow On)$, $t_{PLH}(\overline{EL}\rightarrow On)$, t_{WELL}, t_{SU}, t_{hold}



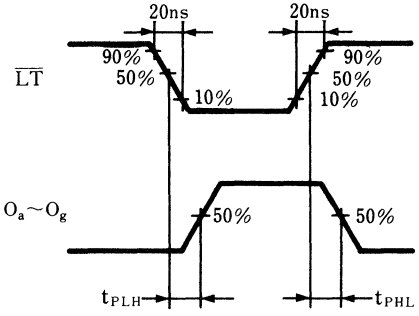
Input D_B, D_C and D_D= "L"
Input $\overline{BI}$ and $\overline{LT}$= "H"

(Fig. 3) $t_{PHL}(\overline{BI}\rightarrow On)$, $t_{PLH}(\overline{BI}\rightarrow On)$



Input D_A, D_B, D_C and $\overline{EL}$= "L"
Input D_D and $\overline{LT}$= "L"

(Fig. 4) $t_{PHL}(\overline{LT}\rightarrow On)$, $t_{PLH}(\overline{LT}\rightarrow On)$



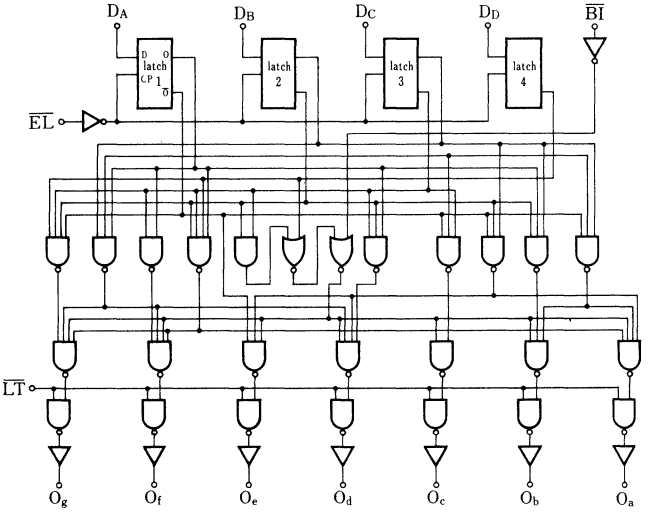
Input D_A, D_B and $\overline{EL}$= "L"
Input D_C, D_D and $\overline{BI}$= "H"

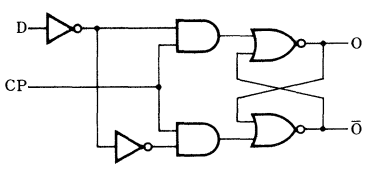
■ Truth Table

Input							Output							Display
$\overline{EL}$	$\overline{BI}$	$\overline{LT}$	D_D	D_C	D_B	D_A	Oa	Ob	Oc	Od	Oe	Of	Og	
×	×	L	×	×	×	×	H	H	H	H	H	H	H	8
×	L	H	×	×	×	×	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	×	×	×	×				*				*

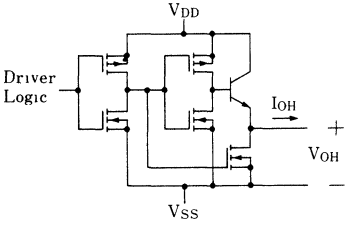
Note) × : don't care * : defined by the added BCD code at EL = L

■ Logic Diagram





(One latch)



(Output Stage Schematic Diagram)

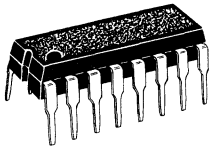
MN4512B/MN4512BS

8-Input Multiplexers

■ Description

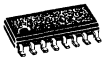
The MN4512B/S are 8-channel data selectors which select data inputs ($I_0 \sim I_7$) by select inputs (S_0, S_1, S_2). A High on the output enable forces the output high impedance (tristate), independent of any other conditions.
A High on the inhibit input ($\overline{E}$) and a Low on the enable output ($\overline{EO}$) inhibits the data select, and the output ($\overline{O}$) becomes Low.
The MN4513B/S are equivalent MOTOROLA MC14512B and RCA CD4512B.

P- 3



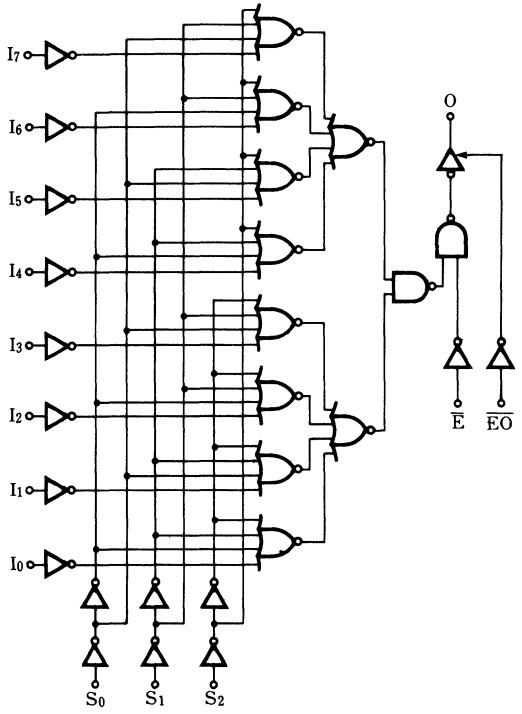
16-Pin • Plastic DIL Package

P- 4

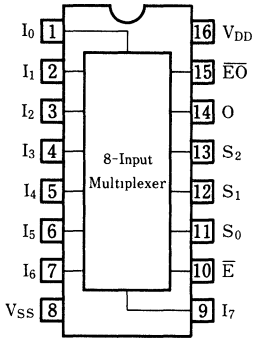


16-Pin • Panaflat Package (SO-16D)

■ Logic Diagram



Pin Configuration



Pin Explanation

S_0, S_1, S_2 : Select input
$\overline{EO}$: Output enable input
$\overline{E}$: Inhibit input
$I_0 \sim I_7$: Multiplexer input
O : Multiplexer output

■ Truth Table

Input													Output
$\overline{EO}$	$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	O
L	H	×	×	×	×	×	×	×	×	×	×	×	L
L	L	L	L	L	L	×	×	×	×	×	×	×	L
L	L	L	L	L	H	×	×	×	×	×	×	×	H
L	L	L	L	H	×	L	×	×	×	×	×	×	L
L	L	L	L	H	×	H	×	×	×	×	×	×	H
L	L	L	H	L	×	×	L	×	×	×	×	×	L
L	L	L	H	L	×	×	H	×	×	×	×	×	H
L	L	L	H	H	×	×	×	L	×	×	×	×	L
L	L	L	H	H	×	×	×	H	×	×	×	×	H
L	L	H	L	L	×	×	×	×	L	×	×	×	L
L	L	H	L	L	×	×	×	×	H	×	×	×	H
L	L	H	L	H	×	×	×	×	×	L	×	×	L
L	L	H	L	H	×	×	×	×	×	H	×	×	H
L	L	H	H	L	×	×	×	×	×	×	L	×	L
L	L	H	H	L	×	×	×	×	×	×	H	×	H
L	L	H	H	H	×	×	×	×	×	×	×	L	L
L	L	H	H	H	×	×	×	×	×	×	×	H	H
H	×	×	×	×	×	×	×	×	×	×	×	×	Z

Note) X : don't care
Z : high impedance (OFF Mode)

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		$\|I_O\|$<1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		$\|I_O\|$<1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA
3-State Output Pin: Leakage Current High Level	15	I_{OZH}	V_O=V_{DD}	—	1.6	—	1.6	—	12	μA
3-State Output Pin: Leakage Current Low Level	15	$-I_{OZL}$	V_O=V_{SS}	—	1.6	—	1.6	—	12	

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time In→O (L→H)	5	t_{PLH}	—	100	300	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time In→O (H→L)	5	t_{PHL}	—	100	300	ns
	10		—	40	120	
	15		—	30	90	

■ **Switching Characteristics** (Ta=25℃, V_{SS}=0V, C_L=50pF) (continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Propagation Delay Time Sn→O (L→H)	5	t_{PLH}	—	150	450	ns
	10		—	60	180	
	15		—	40	120	
Propagation Delay Time Sn→O (H→L)	5	t_{PHL}	—	140	420	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time $\overline{E}$→O (L→H)	5	t_{PLH}	—	55	165	ns
	10		—	25	75	
	15		—	20	60	
Propagation Delay Time $\overline{E}$→O (H→L)	5	t_{PHL}	—	60	180	ns
	10		—	25	75	
	15		—	20	60	
High Level Output Disable Time $\overline{EO}$→O (H)	5	t_{PHZ}	—	35	105	ns
	10		—	20	60	
	15		—	15	45	
Low Level Output Disable Time $\overline{EO}$→O (L)	5	t_{PLZ}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
High Level Output Enable Time $\overline{EO}$→O (H)	5	t_{PZH}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Low Level Output Enable Time $\overline{EO}$→O (L)	5	t_{PZL}	—	35	105	ns
	10		—	20	60	
	15		—	15	45	
Input Capacitance		C_I	—	—	7.5	pF

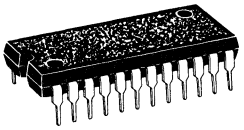
MN4514B / MN4514BS

4-Bit Latch / Line Decoders (High)

■ Description

The MN4514B/S are decoders which convert 4-bit input to 16-bit output with the function of latching the input data.
Only the selected output becomes "H".
The latch is an R-S type flip-flop and input data is held immediately before the strobe input changes from "H" to "L".

P- 5



24-Pin • Plastic DIL Package

P- 6

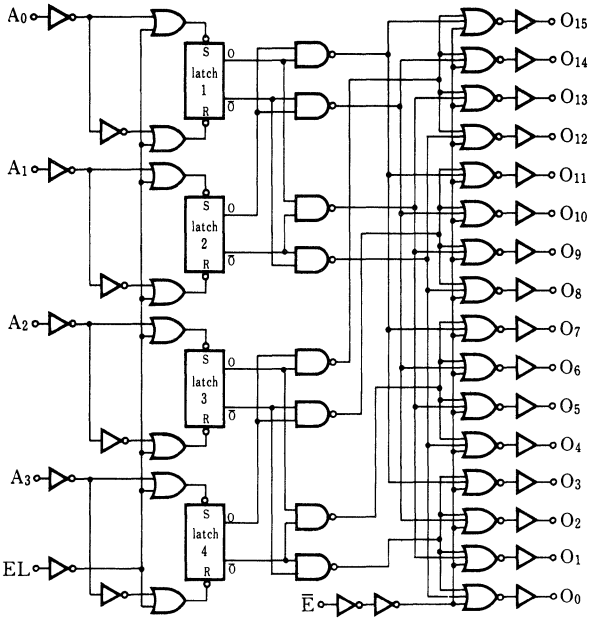
24-Pin • Panaflat Package (SO-24D)

■ Truth Table

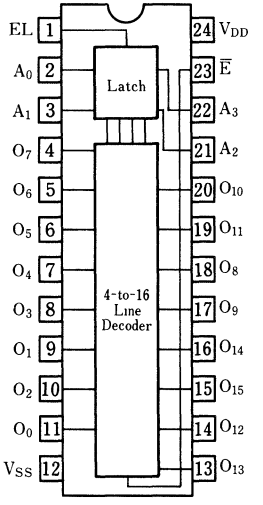
Input					Output															
E	A_0	A_1	A_2	A_3	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	O_{10}	O_{11}	O_{12}	O_{13}	O_{14}	O_{15}
H	×	×	×	×	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

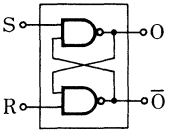
Note) EL = H; X : don't care

■ Logic Diagram



Pin Configuration





(One latch)

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

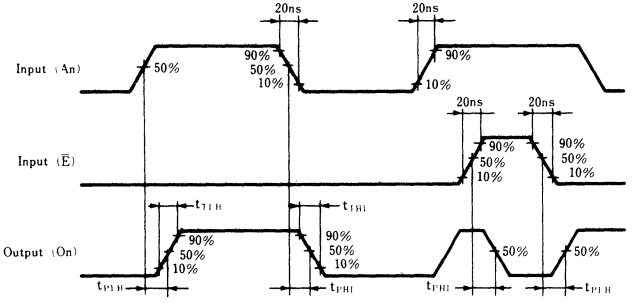
Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

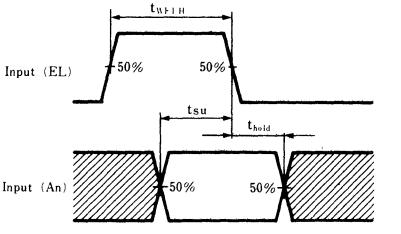
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time (Fig. 1)	5	t_{TLH}	—	85	255	ns
	10		—	35	105	
	15		—	25	75	
Output Fall Time (Fig. 1)	5	t_{THL}	—	90	270	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time (Fig. 1) An, EL→On (L→H)	5	t_{PLH}	—	270	810	ns
	10		—	95	285	
	15		—	65	195	
Propagation Delay Time (Fig. 1) An, EL→On (H→L)	5	t_{PHL}	—	260	780	ns
	10		—	95	285	
	15		—	65	195	
Propagation Delay Time (Fig. 1) $\overline{E}$→On (L→H)	5	t_{PLH}	—	200	600	ns
	10		—	70	210	
	15		—	50	150	
Propagation Delay Time (Fig. 1) $\overline{E}$→On (H→L)	5	t_{PHL}	—	175	525	ns
	10		—	65	195	
	15		—	45	135	
Minimum EL Pulse Width (Fig. 2)	5	t_{WELH}	—	60	180	ns
	10		—	20	60	
	15		—	15	45	
Set-up Time (Fig. 2) An→EL	5	t_{su}	—	60	180	ns
	10		—	20	60	
	15		—	15	45	
Hold Time (Fig. 2) An→EL	5	t_{hold}	0	60	—	ns
	10		0	20	—	
	15		0	15	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms

(Fig. 1) t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}



(Fig. 2) t_{WELH}, t_{su}, t_{hold}



Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL
Set-up and hold times are shown as positive values but may be specified as negative values.

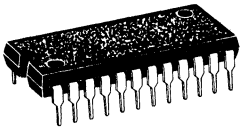
MN4515B/MN4515BS

4-Bit Latch/Line Decoders (Low)

Description

The MN4515B/S are decoders which convert 4-bit input to 16-bit output with the function of latching the input data.
Only the selected output becomes "L".
The latch is an R-S type flip-flop and input data is held immediately before the strobe input changes from "H" to "L".

P-5



24-Pin • Plastic DIL Package

P-6

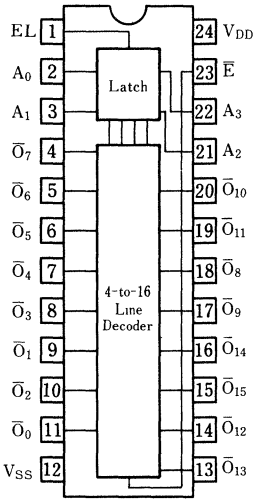
24-Pin • Panaflat Package (SO-24D)

Truth Table

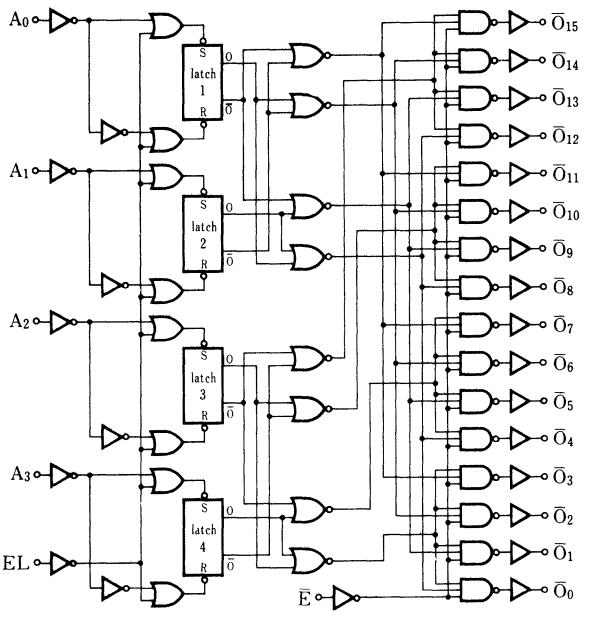
Input					Output														
E	A_0	A_1	A_2	A_3	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$	$\overline{O}_{10}$	$\overline{O}_{11}$	$\overline{O}_{12}$	$\overline{O}_{13}$	$\overline{O}_{14}$	$\overline{O}_{15}$
H	×	×	×	×	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

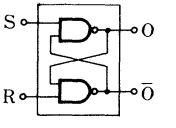
Note) EL = H; X : don't care

Pin Configuration



Logic Diagram





(One latch)

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

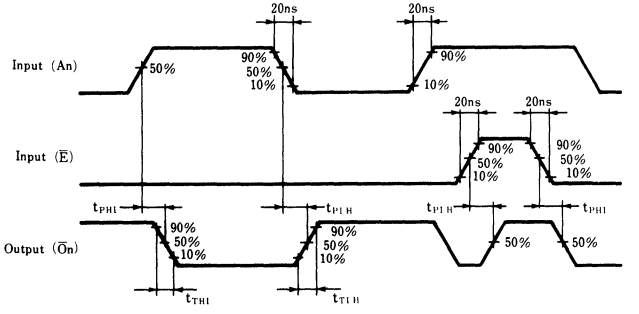
Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

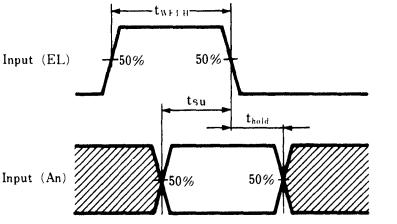
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time (Fig. 1)	5	t_{TLH}	—	85	255	ns
	10		—	35	105	
	15		—	25	75	
Output Fall Time (Fig. 1)	5	t_{THL}	—	90	270	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time (Fig. 1) An, EL→$\overline{On}$ (L→H)	5	t_{PLH}	—	270	810	ns
	10		—	95	285	
	15		—	65	195	
Propagation Delay Time (Fig. 1) An, EL→$\overline{On}$ (H→L)	5	t_{PHL}	—	260	780	ns
	10		—	95	285	
	15		—	65	195	
Propagation Delay Time (Fig. 1) $\overline{E}$→$\overline{On}$ (L→H)	5	t_{PLH}	—	200	600	ns
	10		—	70	210	
	15		—	50	150	
Propagation Delay Time (Fig. 1) $\overline{E}$→$\overline{On}$ (H→L)	5	t_{PHL}	—	175	525	ns
	10		—	65	195	
	15		—	45	135	
Minimum EL Pulse Width (Fig. 2)	5	t_{WELH}	—	60	180	ns
	10		—	20	60	
	15		—	15	45	
Set-up Time (Fig. 2) An→EL	5	t_{su}	—	60	180	ns
	10		—	20	60	
	15		—	15	45	
Hold Time (Fig. 2) An→EL	5	t_{hold}	0	60	—	ns
	10		0	20	—	
	15		0	15	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms

(Fig. 1) t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}



(Fig. 2) t_{WELH}, t_{su}, t_{hold}



Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL; set-up and hold times are shown as positive values but may be specified as negative values.

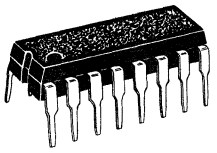
MN4516B / MN4516BS

4-Bit Binary Up/Down Counters

■ Description

The MN4516B/S are 4-bit synchronous up/down counters. An appropriate value of the counter is presettable by setting data inputs ($P_0 \sim P_3$) while the reset input is Low and the load input High.
The counter advances on the positive going edge of the clock input when the load and the counter inputs are low.
A High on the reset input resets all the outputs ($O_0 \sim O_3$) Low.
The UP/$\overline{DN}$ input determines whether the counter functions up or down (H = UP, L = DOWN).
The MN4516B/S are equivalent to MOTOROLA MC14516B and RCA CD4516B.

P-3



16-Pin • Plastic DIL Package

P-4

16-Pin • Panaflat Package (SO-16D)

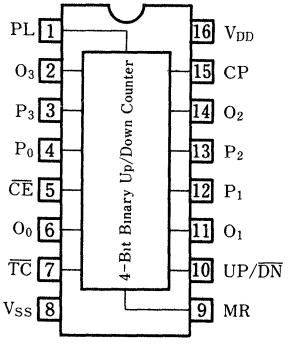
■ Truth Table

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	Mode
L	H	×	×	×	parallel load
L	L	×	H	×	no change
L	L	L	L	⎍	count down
L	L	H	L	⎍	count up
H	×	×	×	×	liset

Pin Explanation

CP : Clock input
UP/$\overline{DN}$: Up, Down designate input
PL : Counter load input
$\overline{CE}$: Counter enable input
MR : Reset input
$P_0 \sim P_3$: Data input
$O_0 \sim O_3$: Counter output
$\overline{TC}$: Carry output

Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

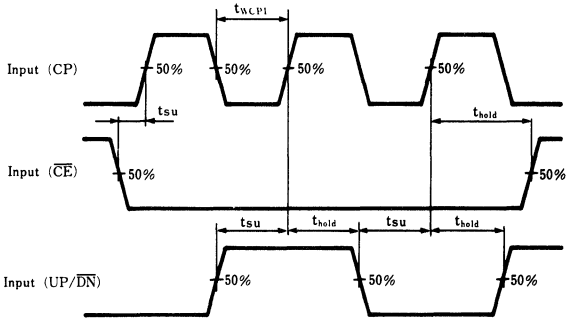
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	155	465	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time CP→$\overline{TC}$ (H→L)	5	t_{PHL}	—	260	780	ns
	10		—	105	315	
	15		—	75	225	
Propagation Delay Time CP→$\overline{TC}$ (L→H)	5	t_{PLH}	—	180	540	ns
	10		—	75	225	
	15		—	55	165	
Propagation Delay Time PL→On (H→L)	5	t_{PHL}	—	125	375	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time PL→On (L→H)	5	t_{PLH}	—	170	510	ns
	10		—	70	210	
	15		—	50	150	
Propagation Delay Time PL→$\overline{TC}$ (H→L)	5	t_{PHL}	—	250	750	ns
	10		—	110	330	
	15		—	80	240	
Propagation Delay Time PL→$\overline{TC}$ (L→H)	5	t_{PLH}	—	250	750	ns
	10		—	110	330	
	15		—	80	240	
Propagation Delay Time $\overline{CE}$→$\overline{TC}$ (H→L)	5	t_{PHL}	—	165	495	ns
	10		—	65	195	
	15		—	50	150	
Propagation Delay Time $\overline{CE}$→$\overline{TC}$ (L→H)	5	t_{PLH}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Propagation Delay Time MR→On, $\overline{TC}$ (H→L)	5	t_{PHL}	—	205	615	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time MR→$\overline{TC}$ (L→H)	5	t_{PLH}	—	225	675	ns
	10		—	75	225	
	15		—	50	150	
Minimum Clock Pulse Width (Fig. 1)	5	t_{WCPL}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	

■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$) (countinued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Minimum PL Pulse Width (H) (Fig. 2)	5	t_{WPLH}	—	55	165	ns
	10		—	25	75	
	15		—	15	45	
Minimum Reset Pulse Width (H) (Fig. 2)	5	t_{WMRH}	—	60	180	ns
	10		—	25	75	
	15		—	20	60	
Reset Recovery Time (Fig. 2)	5	t_{RMR}	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
PL Recovery Time (Fig. 2)	5	t_{RPL}	—	75	225	ns
	10		—	25	75	
	15		—	15	45	
Set-up Time (Fig. 2) Pn→PL	5	t_{su}	—	50	150	ns
	10		—	25	75	
	15		—	20	60	
Set-up Time (Fig. 1) UP/$\overline{DN}$→CP	5	t_{su}	—	125	375	ns
	10		—	50	150	
	15		—	35	105	
Set-up Time (Fig. 1) $\overline{CE}$→CP	5	t_{su}	—	60	180	ns
	10		—	20	60	
	15		—	10	30	
Hold Time (Fig. 2) Pn→PL	5	t_{hold}	—	−40	10	ns
	10		—	−20	5	
	15		—	−20	0	
Hold Time (Fig, 1) UP/$\overline{DN}$→CP	5	t_{hold}	—	−90	35	ns
	10		—	−35	15	
	15		—	−25	15	
Hold Time (Fig. 1) $\overline{CE}$→CP	5	t_{hold}	—	−40	20	ns
	10		—	−15	5	
	15		—	−10	5	
Maximum Clock Frequency	5	fmax	5	10	—	MHz
	10		12	24	—	
	15		17	34	—	
Input Capacitance		C_I	—	—	7.5	pF

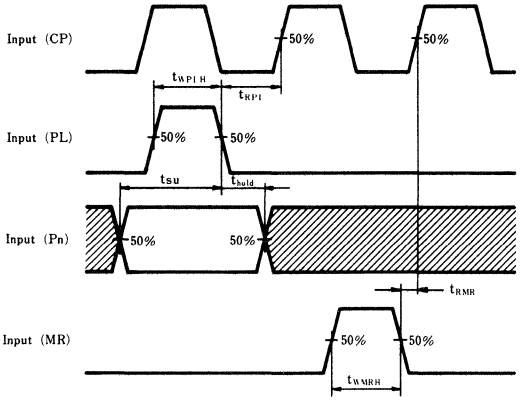
• Dynamic Signal Waveforms

(Fig. 1) t_{WCPL}, t_{su}(UP/$\overline{DN}$→CP · $\overline{CE}$→CP), t_{hold}(UP/$\overline{DN}$→CP · $\overline{CE}$→CP)



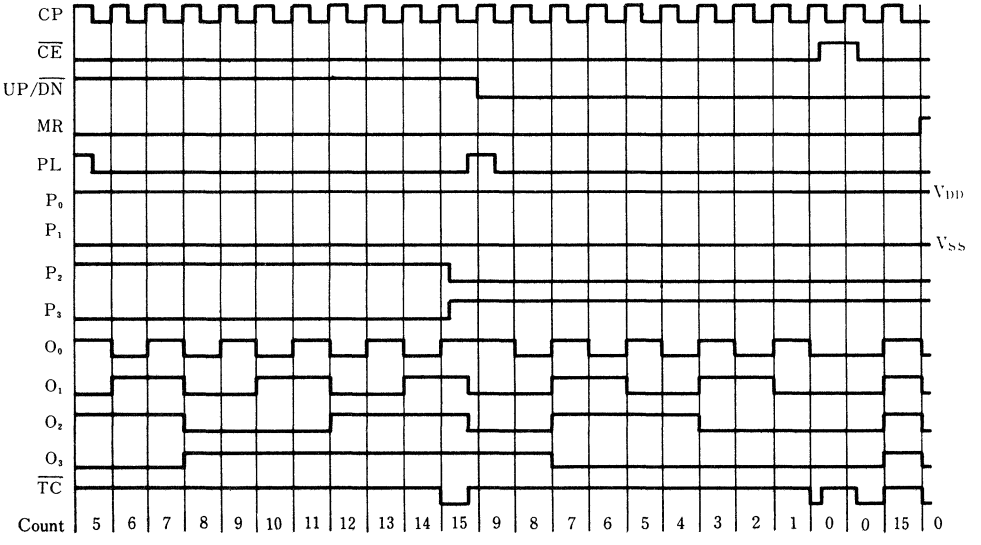
Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP and UP/$\overline{DN}$ to CP

(Fig. 2) t_{WPLH}, t_{RPL}, t_{RMR}, t_{WMRH}, $t_{SU}(Pn \rightarrow PL)$, $t_{hold}(Pn \rightarrow PL)$



Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR, and set-up and hold times for P_n to PL

■ Timing Diagram



New Product Indormation

Type No.	Function	Pins
MN4014B/S	8-Stage Static Shift Register	16
MN4031B/S	64-Stage Static Shift Register	16
MN4041B/S	Quad True Complement Buffer	14
MN4047B/S	Monostable Astable Multivibrator	14
MN4060B/S	14-Stage Ripple-Carry Binary Counter/Divider and Oscillator	16
MN4077B/S	Quad Exclusive-NOR Gate	14
MN4104B/S	Quad Low Voltage to High Voltage Translator with 3/5	16
MN4505B/S	64×1-Bit Static RAM	14
MN4521B/S	24-Stage Frequency Divider	16
MN4522B/S	Programmable BCD Divide-by-N Counter	16
MN4527B/S	BCD Rate Multiplier	16
MN4532B/S	8-Bit Priority Encoder	16
MN4555B/S	Dual Binary to 1-of-4 Decoder/Demultiplexer	16
MN4557B/S	1-of-64-Bit Variable Length Shift Register	16
MN4720B/S	256-Bit, 1-Bit-per-Word RAM	16
MN4731B/S	Quad 64-Bit Static Shift Register	14
MN40162B/S	Decade Counter with Synchronous Clear	16
MN40163B/S	4-Bit Binary Counter with Synchronous Clear	16
MN40192B/S	4-Bit Up/Down Decade Counter	16
MN40193B/S	4-Bit Up/Down Binary Counter	16
MN40194B/S	4-Bit Bidirectional Universal Shift Register	16
MN40195B/S	4-Bit Universal Shift Register	16

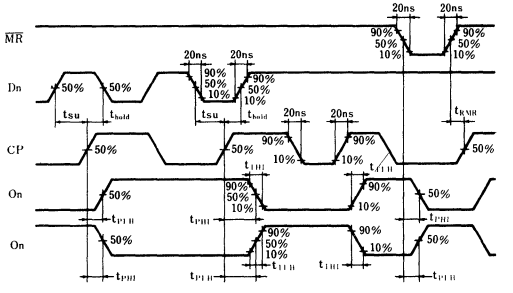
Note) Under development

New Product Information

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On, $\overline{On}$ (H→L)	5	t_{PHL}	—	80	240	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time CP→On, $\overline{On}$ (L→H)	5	t_{PLH}	—	70	210	ns
	10		—	30	90	
	15		—	25	75	
Propagation Delay Time $\overline{MR}$→On (H→L)	5	t_{PHL}	—	75	225	ns
	10		—	30	90	
	15		—	25	75	
Propagation Delay Time $\overline{MR}$→$\overline{On}$ (L→H)	5	t_{PLH}	—	70	210	ns
	10		—	30	90	
	15		—	25	75	
Set-up Time Dn→CP	5	t_{su}	—	30	90	ns
	10		—	10	30	
	15		—	5	15	
Hold Time Dn→CP	5	t_{hold}	—	− 5	30	ns
	10		—	0	15	
	15		—	0	15	
Minimum Clock Pulse Width	5	t_{WCPL}	—	45	135	ns
	10		—	15	45	
	15		—	10	30	
Minimum Reset Pulse Width	5	t_{WMRL}	—	40	120	ns
	10		—	15	45	
	15		—	10	30	
Reset Recovery Time	5	t_{RMR}	—	−30	0	ns
	10		—	−20	0	
	15		—	−15	0	
Maximum Clock Frequency	5	fmax	5	11	—	MHz
	10		15	30	—	
	15		20	45	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

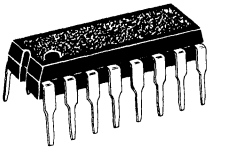
MN40175B/MN40175BS

Quad D-Type Flip-Flops

■ Description

The MN40175B/S have quad D-type flip-flop which have common CP and $\overline{MR}$ pins
D_n input is transferred to O_n output on the positive going edge of clock input.
When the $\overline{MR}$ input becomes "L" level, the quad flip-flop can be reset at the same time.
These are equivalent to MOTOROLA MC14715B.

P-3



16-Pin • Plastic DIL Package

P-4

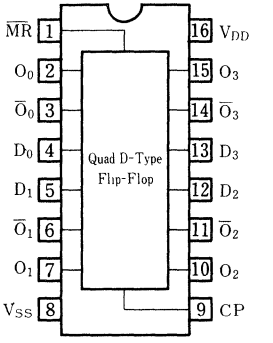
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

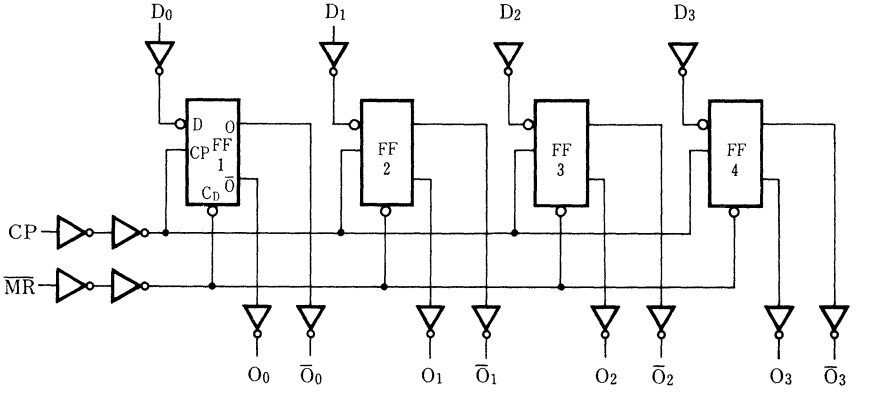
Input			Output	
CP	D	$\overline{MR}$	O	$\overline{O}$
↑	H	H	H	L
↑	L	H	L	H
↓	×	H	no change	no change
×	×	L	L	H

Note) X : don't care

Pin Configuration



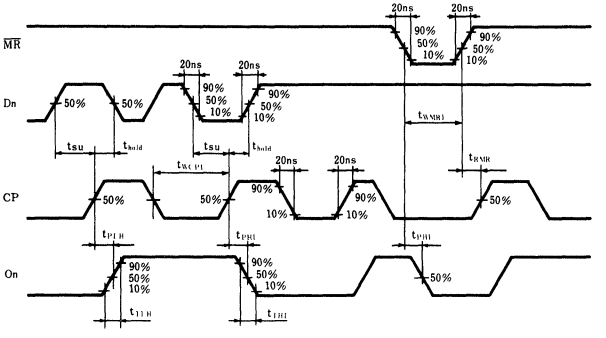
■ Logic Diagram



■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	75	225	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	75	225	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $\overline{MR}$→On (H→L)	5	t_{PHL}	—	85	255	ns
	10		—	35	105	
	15		—	25	75	
Set-up Time Dn→CP	5	t_{su}	—	10	30	ns
	10		—	5	15	
	15		—	5	15	
Hold Time Dn→CP	5	t_{hold}	—	0	20	ns
	10		—	0	10	
	15		—	0	10	
Minimum Clock Pulse Width	5	t_{WCPL}	—	35	100	ns
	10		—	15	45	
	15		—	10	30	
Minimum $\overline{MR}$ Pulse Width	5	t_{WMRL}	—	35	100	ns
	10		—	15	45	
	15		—	10	30	
Reset Recovery Time	5	t_{RMR}	—	25	75	ns
	10		—	10	30	
	15		—	5	15	
Maximum Clock Frequency	5	fmax	5	11	—	MHz
	10		15	30	—	
	15		20	45	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

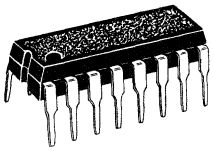
MN40174B/MN40174BS

Hex D-Type Flip-Flops

■ Description

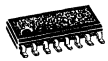
The MN40174B/S have hex D-type flip-flops with common CP and MR pins.
D_n input is transferred to O_n output on the positive going edge of clock input.
When the MR input level becomes "L", hex flip-flop can be reset at the same time.
The MN40174B/S are equivalent to MOTOROLA MC14174B and RCA CD40174B.

P-3



16-Pin • Plastic DIL Package

P-4



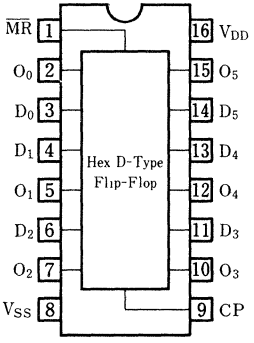
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

Input			Output
CP	D	$\overline{MR}$	O
↑	H	H	H
↑	L	H	L
↓	×	H	no change
×	×	L	L

Note) X : don't care

Pin Configuration



■ Logic Diagram

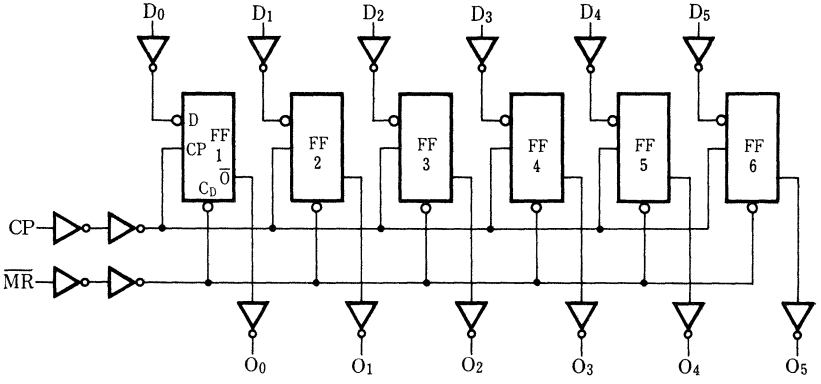
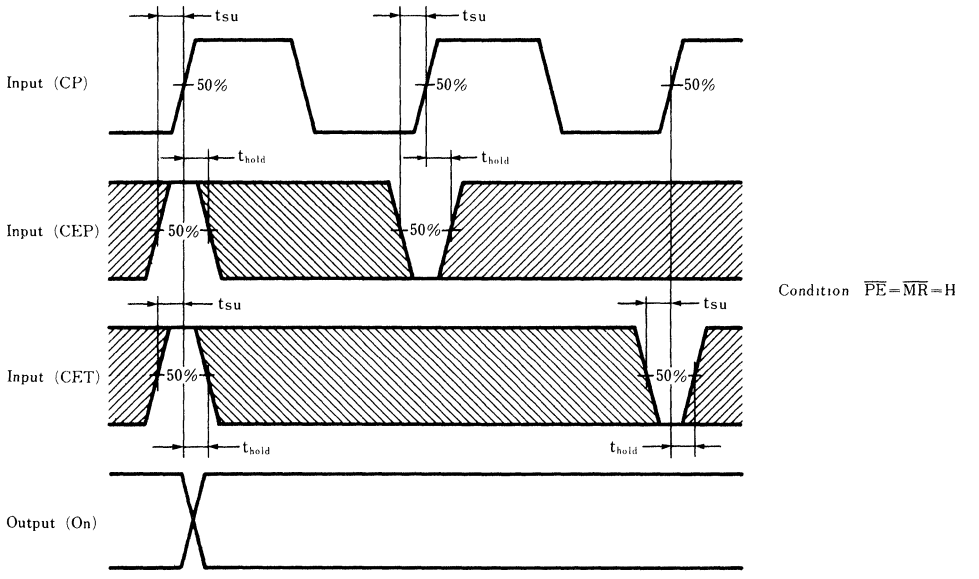


Fig. 4 Dynamic Signal Waveforms (CEP, CET → CP)



■ Timing Diagram

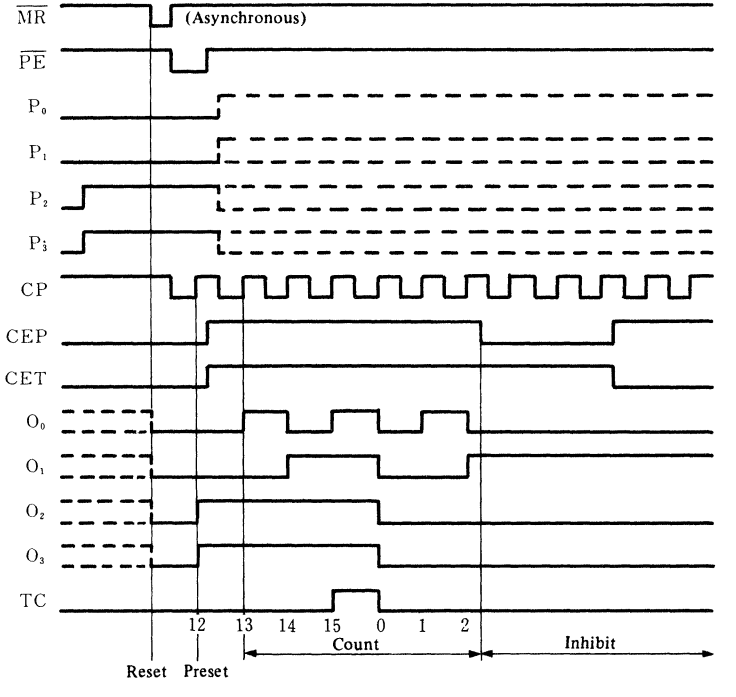


Fig. 1 Dynamic Signal Waveforms (CP, MR)

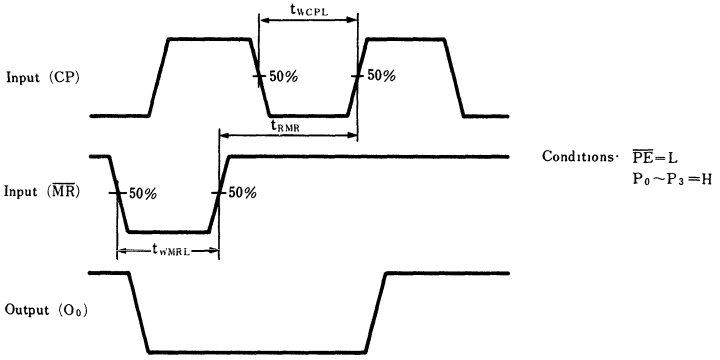


Fig. 2 Dynamic Signal Waveforms ($P_n \rightarrow CP$)

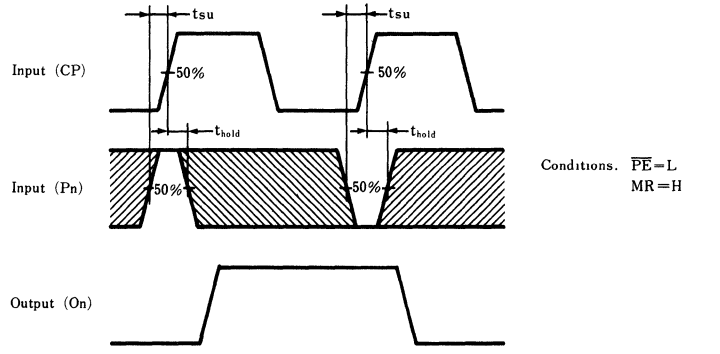
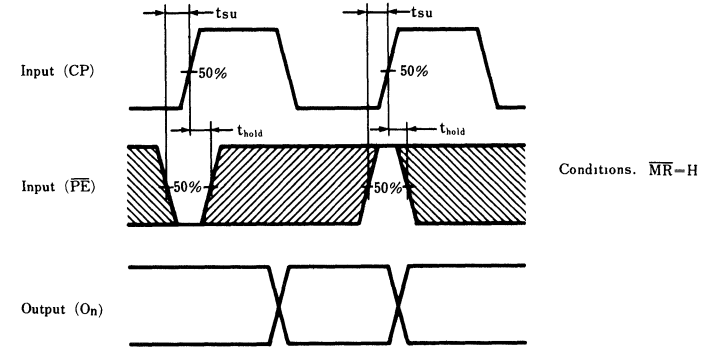


Fig. 3 Dynamic Signal Waveforms (PE → CP)



■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$) (continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	115	345	ns
	10		—	45	135	
	15		—	35	105	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	110	330	ns
	10		—	45	135	
	15		—	30	90	
Propagation Delay Time CP→TC (L→H)	5	t_{PLH}	—	140	420	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time CP→TC (H→L)	5	t_{PHL}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time CET→TC (L→H)	5	t_{PLH}	—	90	270	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time CET→TC (H→L)	5	t_{PHL}	—	105	315	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time $\overline{MR}$→On (H→L)	5	t_{PHL}	—	120	360	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time $\overline{MR}$→TC (H→L)	5	t_{PHL}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Minimum Clock Pulse Width (Fig. 1)	5	t_{WCPL}	—	50	150	ns
	10		—	20	60	
	15		—	15	45	
Minimum Reset Pulse Width (Fig. 1)	5	t_{WMRL}	—	50	150	ns
	10		—	20	60	
	15		—	15	45	
Reset Recovery Time (Fig. 1) $\overline{MR}$	5	t_{RMR}	—	0	50	ns
	10		—	0	30	
	15		—	0	20	
Set-up Time (Fig. 2) Pn→CP	5	tsu	—	55	165	ns
	10		—	20	60	
	15		—	15	45	
Set-up Time (Fig. 3) $\overline{PE}$→CP	5	tsu	—	60	180	ns
	10		—	20	60	
	15		—	10	30	
Set-up Time (Fig. 4) CEP, CET→CP	5	tsu	—	130	390	ns
	10		—	50	150	
	15		—	35	105	
Maximum Clock Frequency (Fig. 1)	5	fmax	5	10	—	MHz
	10		12	25	—	
	15		17	35	—	
Input Capacitance		C_I	—	—	7.5	pF

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissiption (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	

MN40161B/MN40161BS

4-Bit Binary Counters

■ Description

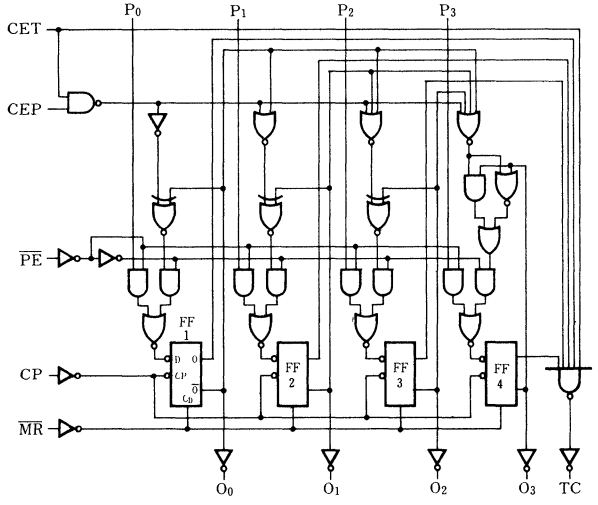
The MN40161B/S are synchronous programmable 4-bit binary counters.
The reset functions asynchronously, causing all flip-flop outputs to reset.
The counter advances on the positive going edge of the clock input when both CEP and CET inputs are High and the PE input is also High.
The MN40161B/S are equivalent to MOTOROLA MC14161B and RCA CD40161B.

■ Truth Table

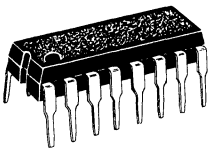
Input				Mode
$\overline{MR}$	$\overline{PE}$	CEP	CET	
H	L	×	×	parallel load
H	H	L	×	no change
H	H	×	L	
H	H	H	H	counter advance
L	×	×	×	reset ($O_0 \sim O_3 = L$)

Note) × : don't care

■ Logic Diagram

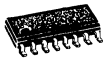


P-3



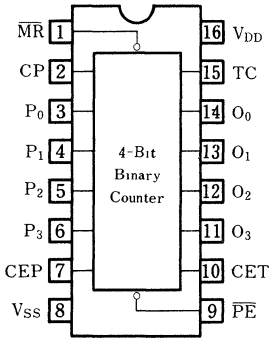
16-Pin • Plastic DIL Package

P-4



16-Pin • Panaflat Package (SO-16D)

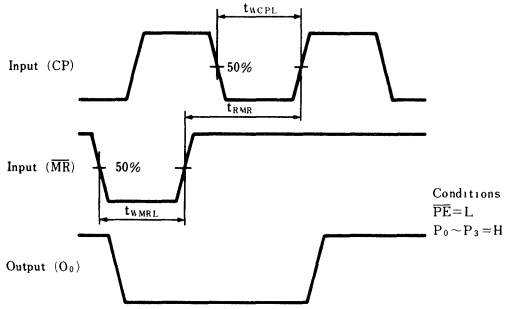
Pin Configuration



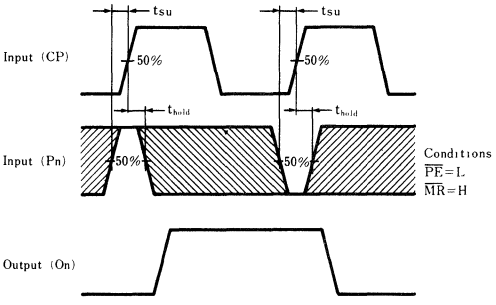
Pin Explanation

$\overline{PE}$: Parallel enable input
$P_0 \sim P_3$: Parallel data input
CEP : Count enable parallel input
CET : Count enable triple input
CP : Clock input (⎍)
$\overline{MR}$: Master reset input
$O_0 \sim O_3$: Parallel output
TC : Carry output

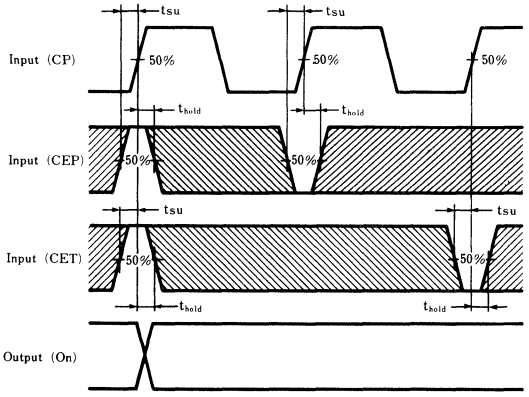
• Dynamic Signal Waveforms



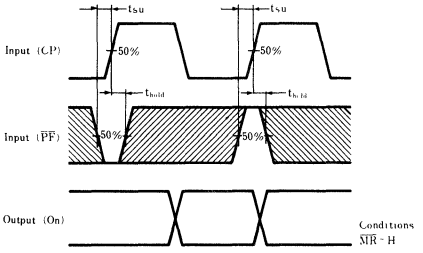
Waveforms showing minimum CP and $\overline{MR}$ pulse widths and $\overline{MR}$ to CP recovery time



Waveforms showing set-up times and hold times for P_n inputs

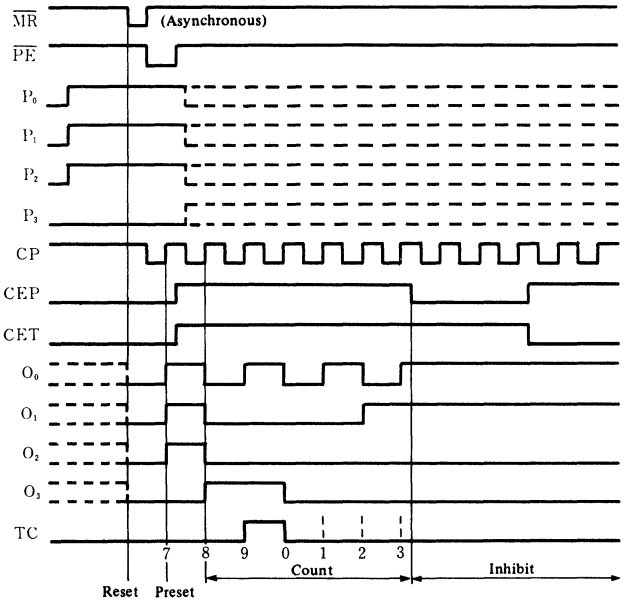


Waveforms showing set-up times and hold times for CEP and CET inputs



Waveforms showing set-up times and hold times for $\overline{PE}$ inputs.

■ Timing Diagram



■ **Switching Characteristics** (Ta=25℃, V_{SS}=0V, C_L=50pF) (continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Propagation Delay Time CET→TC (L→H)	5	t_{PLH}	—	90	270	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time CET→TC (H→L)	5	t_{PHL}	—	105	315	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time $\overline{MR}$→On (H→L)	5	t_{PHL}	—	120	360	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time $\overline{MR}$→TC (H→L)	5	t_{PHL}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Minimum Clock Pulse Width	5	t_{WCPL}	—	50	150	ns
	10		—	20	60	
	15		—	15	45	
Minimum Reset Pulse Width	5	t_{WMRL}	—	50	150	ns
	10		—	20	60	
	15		—	15	45	
Reset Recovery Time	5	t_{RMR}	—	0	50	ns
	10		—	0	30	
	15		—	0	20	
Set-up Time Pn→CP	5	t_{su}	—	55	165	ns
	10		—	20	60	
	15		—	15	45	
Set-up Time $\overline{PE}$→CP	5	t_{su}	—	60	180	ns
	10		—	20	60	
	15		—	10	30	
Set-up Time CEP, CET→CP	5	t_{su}	—	130	390	ns
	10		—	50	150	
	15		—	35	105	
Hold Time Pn→CP	5	t_{hold}	—	−35	30	ns
	10		—	−10	15	
	15		—	−10	10	
Hold Time $\overline{PE}$→CP	5	t_{hold}	—	−45	20	ns
	10		—	−15	10	
	15		—	−10	10	
Hold Time CEP, CET→CP	5	t_{hold}	—	−105	35	ns
	10		—	− 35	25	
	15		—	− 25	15	
Minimum Clock Frequency	5	fmax	5	10	—	MHz
	10		12	25	—	
	15		17	35	—	
Input Capacitance		C_I	—	—	7.5	pF

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		| I_O | <1μA, V_O=1V or 9V	—	3	—	3	—	3	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		| I_O | <1μA, V_O=1V or 9V	7	—	7	—	7	—	
	15		| I_O | <1μA, V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	115	345	ns
	10		—	45	135	
	15		—	35	105	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	110	330	ns
	10		—	45	135	
	15		—	30	90	
Propagation Delay Time CP→TC (L→H)	5	t_{PLH}	—	140	420	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time CP→TC (H→L)	5	t_{PHL}	—	130	390	ns
	10		—	55	165	
	15		—	35	105	

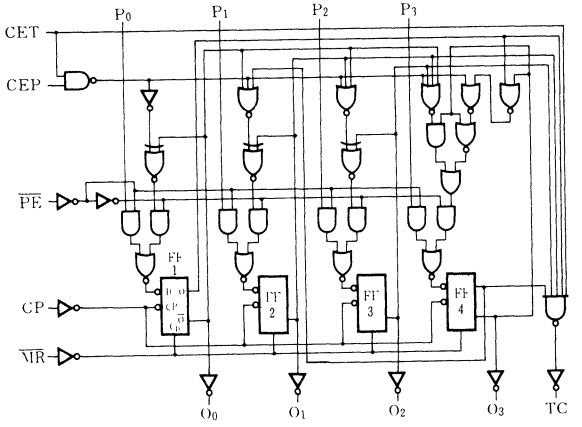
MN40160B/MN40160BS

4-Bit Decade Counters

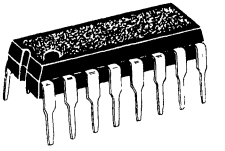
■ Description

The MN40160B/S are 4-bit decade counters which have asynchronous clear input.

■ Logic Diagram

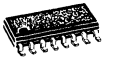


P-3



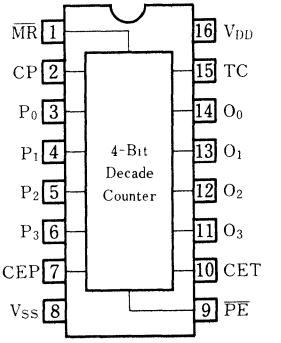
16-Pin • Plastic DIL Package

P-4



16-Pin • Panaflat Package (SO-16D)

Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

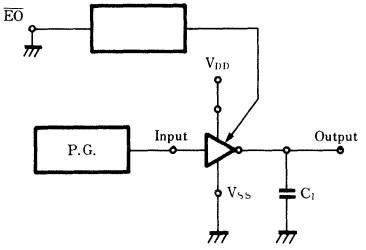
■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$) (continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Low Level Output Disable Time $\overline{EO}_2$, $\overline{EO}_4 \rightarrow$On (L)	5	t_{PLZ}	—	65	195	ns
	10		—	40	120	
	15		—	35	105	
High Level Output Enable Time $\overline{EO}_2$, $\overline{EO}_4 \rightarrow$On (H)	5	t_{PZH}	—	70	210	ns
	10		—	35	105	
	15		—	30	90	
Low Level Output Enable Time $\overline{EO}_2$, $\overline{EO}_4 \rightarrow$On (L)	5	t_{PZL}	—	90	270	ns
	10		—	40	120	
	15		—	35	105	
Input Capacitance		C_I	—	—	7.5	pF

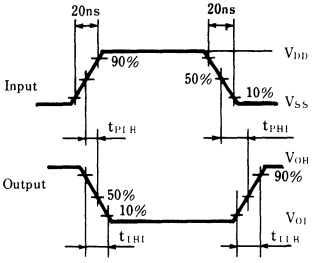
• Switching Time Test Circuit and Waveforms

〔1〕 t_{PLH}, t_{PHL}, t_{THL}, t_{TLH}

1. Test Circuit

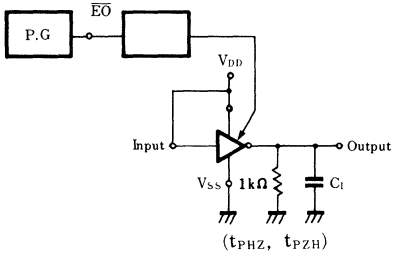


2. Waveforms

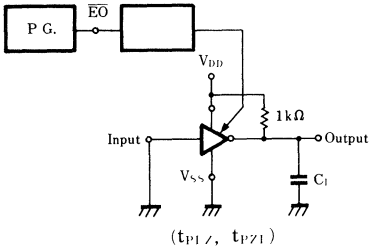


〔2〕 t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL}

1. Test Circuits

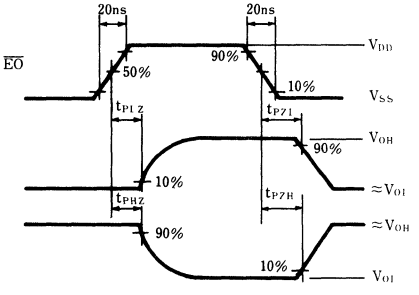


(t_{PHZ}, t_{PZH})



(t_{PLZ}, t_{PZL})

2. Waveforms



■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	4	—	4	—	30	μA
	10			—	8	—	8	—	60	
	15			—	16	—	16	—	120	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	4.75	I_{OL}	V_O=0.4V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
	10		V_O=0.5V, V_I=0 or 10V	4.8	—	4	—	3.2	—	
	15		V_O=1.5V, V_I=0 or 15V	12	—	10	—	8	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	1	—	0.88	—	0.7	—	mA
	10		V_O=9.5V, V_I=0 or 10V	2.4	—	2.2	—	1.8	—	
	15		V_O=13.5V, V_I=0 or 15V	6.6	—	6	—	4.8	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA
3-State Output Pin: Leakage Current High Level	15	I_{OZH}	V_O=V_{DD}	—	1.6	—	1.6	—	12	μA
3-State Output Pin: Leakage Current Low Level	15	$-I_{OZL}$	V_O=V_{SS}	—	1.6	—	1.6	—	12	

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	35	105	ns
	10		—	20	60	
	15		—	15	45	
Output Fall Time	5	t_{THL}	—	30	90	ns
	10		—	15	45	
	15		—	10	30	
Propagation Delay Time In→On (H→L)	5	t_{PHL}	—	80	240	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time In→On (L→H)	5	t_{PLH}	—	65	195	ns
	10		—	30	90	
	15		—	25	75	
High Level Output Disable Time $\overline{EO_2}$, $\overline{EO_4}$→On (H)	5	t_{PHZ}	—	45	135	ns
	10		—	35	105	
	15		—	30	90	

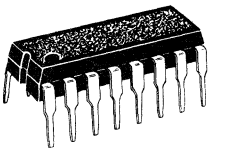
MN40098B/MN40098BS

Hex Inverting 3-State Buffers

■ Description

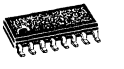
The MN40098B/S are hex inverting 3-state buffers which take large source and sink currents.
Two enable pins ($\overline{EO_2}$, $\overline{EO_4}$) are available which control 2 and 4 circuits independently.
When $\overline{EO_4}$ is "H", the output of buffers 1 ~ 4 becomes high impedance, adn when $\overline{EO_2}$ becomes "H", the output of buffers 5 ~ 6 becomes high impedance.

P-3



16-Pin • Plastic DIL Package

P-4



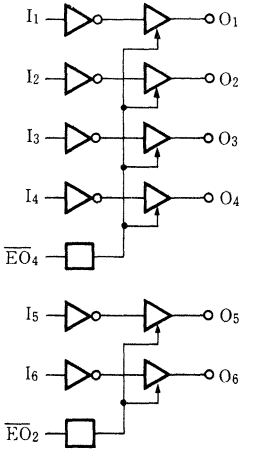
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

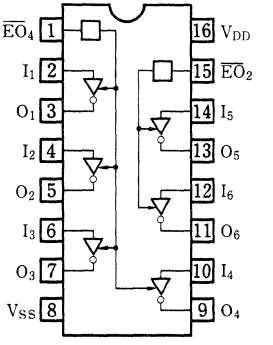
Input		Output
I	$\overline{EO}$	O
L	L	H
H	L	L
×	H	high impedance

Note) X : don't care

■ Logic Diagram



Pin Configuration



■ Maximum Ratings (Ta=25℃)

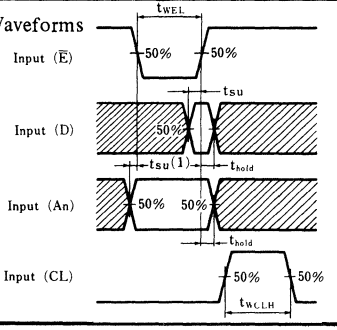
Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Input Current		$\pm I_I$	max. 10	mA
Output Current		$\pm I_I$	max. 25	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

■ **Switching Characteristics** ($Ta = 25℃$, $V_{SS} = 0V$, $C_L = 50pF$) (continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Propagation Delay Time $\overline{E}$→On (L→H)	5	t_{PLH}	—	95	285	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time D→On (H→L)	5	t_{PHL}	—	95	285	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time D→On (L→H)	5	t_{PLH}	—	85	255	ns
	10		—	35	105	
	15		—	25	75	
Propagation Delay Time An→On (H→L)	5	t_{PHL}	—	110	330	ns
	10		—	45	135	
	15		—	35	105	
Propagation Delay Time An→On (L→H)	5	t_{PLH}	—	95	285	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time CL→On (H→L)	5	t_{PHL}	—	85	255	ns
	10		—	35	105	
	15		—	25	75	
Set-up Time D→$\overline{E}$	5	t_{su}	—	20	60	ns
	10		—	5	20	
	15		—	0	15	
Set-up Time An→$\overline{E}$	5	t_{su}	—	20	60	ns
	10		—	10	25	
	15		—	5	20	
Hold Time D→$\overline{E}$	5	t_{hold}	—	5	30	ns
	10		—	5	20	
	15		—	5	20	
Hold Time An→$\overline{E}$	5	t_{hold}	—	25	75	ns
	10		—	10	30	
	15		—	5	15	
Minimum $\overline{E}$ Pulse Width	5	t_{WEL}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Minimum CL Pulse width	5	t_{WCLH}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



(1) The address to enable set-up time is the time before the HIGH to LOW enable transition that the address must be stable so that the correct latch is addressed and the other latches are not affected.

Waveforms showing minimum $\overline{E}$ and CL pulse widths, set-up times, hold times, set-up and hold times are shown as positive values but may be specified as negative values.

■ Maximum Ratings (Ta=25℃)

* V_{DD} + 0.5V should be under 18V

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} |I_O|<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} |I_O|<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	|I_O|<1μA V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	|I_O|<1μA V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $\overline{E}$→On (H→L)	5	t_{PHL}	—	115	345	ns
	10		—	50	150	
	15		—	35	105	

MN4724B/MN4724BS

8-Bit Addressable Latches

■ Description

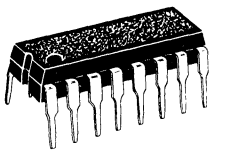
The MN4724B/S are 8-bit addressable latches which have 1 common DATA input and 8 independent outputs. Each latch is controlled by 3-bit address input (A_0, A_1, A_2).

When enable input ($\overline{E}$) and clear input (CL) are "L", DATA is written in the bit selected by address input, and other bits maintain the previous mode.

When enable input ($\overline{E}$) becomes "H", write-in to all bits is inhibited.

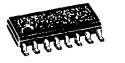
When enable input ($\overline{E}$) and clear input (CL) are "H", all bits are reset to "L".

P- 3



16-Pin • Plastic DIL Package

P- 4



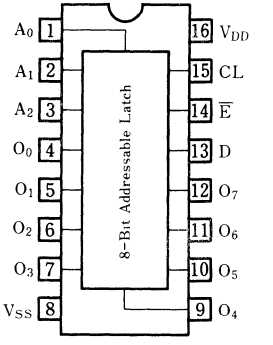
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

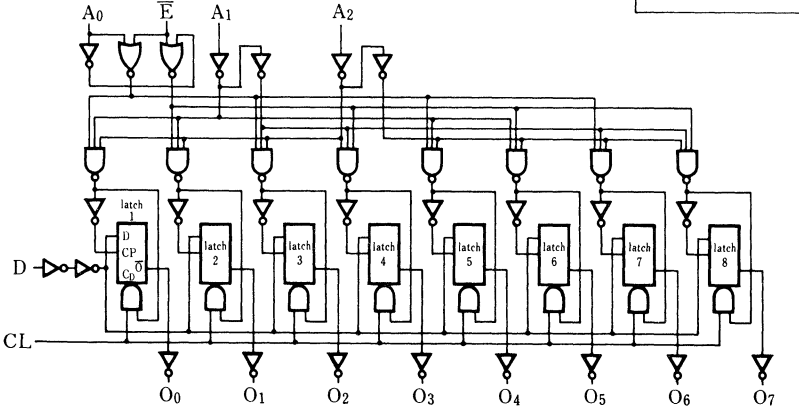
CL	$\overline{E}$	D	A_0	A_1	A_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	Mode
H	H	×	×	×	×	L	L	L	L	L	L	L	L	Clear
H	L	D_1	L	L	L	D_1	L	L	L	L	L	L	L	
H	L	D_1	H	L	L	L	D_1	L	L	L	L	L	L	
H	L	D_1	L	H	L	L	L	D_1	L	L	L	L	L	Non-specified latch is cleared.
H	L	D_1	H	H	L	L	L	L	D_1	L	L	L	L	
H	L	D_1	L	L	H	L	L	L	L	D_1	L	L	L	
H	L	D_1	H	L	H	L	L	L	L	L	D_1	L	L	
H	L	D_1	L	H	H	L	L	L	L	L	L	D_1	L	
H	L	D_1	H	H	H	L	L	L	L	L	L	L	D_1	
L	H	×	×	×	×	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	Memory
L	L	D_1	L	L	L	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	H	L	L	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	L	H	L	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	Non-specified latch holds previous mode.
L	L	D_1	H	H	L	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	L	L	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	H	L	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	
L	L	D_1	L	H	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	
L	L	D_1	H	H	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	

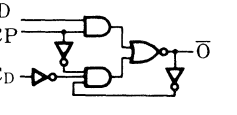
Note) × : don't care; O_{n-1} : Mode before positive change of E
D_1 : H or L

■ Pin Configuration



■ Truth Table



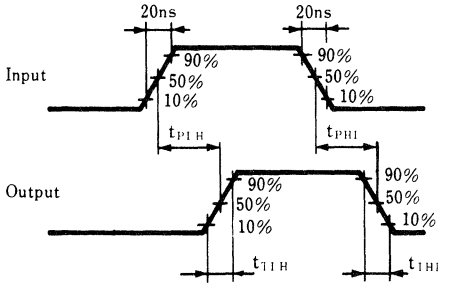


(One latch)

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time An, Bn→On (L→H)	5	t_{PLH}	—	150	450	ns
	10		—	60	180	
	15		—	45	135	
Propagation Delay Time An, Bn→On (H→L)	5	t_{PHL}	—	160	480	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time In→On (L→H)	5	t_{PIH}	—	120	360	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time In→On (H→L)	5	t_{PHI}	—	110	330	ns
	10		—	45	135	
	15		—	30	90	
Input Capacitance		C_I	—	—	7.5	pF

- Waveforms at Switching Time Test



Condition Table (Example)

TEST	P.G.	H	L	Output
An, Bn—On	B_0	$I_{A>B}$ $I_{A=B}$	Other Input	$O_{A<B}$
In—On	$I_{A<B}$	—	Other Input	$O_{A<B}$

P.G. : Pulse Generator

■ Truth Table

Input							Output		
Compare				Cascade					
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$1_{A>B}$	$1_{A<B}$	$1_{A=B}$	$0_{A>B}$	$0_{A<B}$	$0_{A=B}$
$A_3>B_3$	×	×	×	H	×	×	H	L	L
$A_3<B_3$	×	×	×	×	×	×	L	H	L
$A_3=B_3$	$A_2>B_2$	×	×	H	×	×	H	L	L
$A_3=B_3$	$A_2<B_2$	×	×	×	×	×	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	×	H	×	×	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	×	×	×	×	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	H	×	×	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	×	×	×	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	×	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	×	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	×	H	H	L	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	L	L	L

Note) × : don't care

■ DC Characteristics ($V_{SS}=0V$)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	$V_I=V_{SS}$ or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	$V_I=V_{SS}$ or V_{DD} $\lvert I_O\rvert<1\mu A$		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	$V_I=V_{SS}$ or V_{DD} $\lvert I_O\rvert<1\mu A$		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O\rvert<1\mu A$	$V_O=0.5V$ or $4.5V$	—	1.5	—	1.5	—	1.5	V
	10			$V_O=1V$ or $9V$	—	3	—	3	—	3	
	15			$V_O=1.5V$ or $13.5V$	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O\rvert<1\mu A$	$V_O=0.5V$ or $4.5V$	3.5	—	3.5	—	3.5	—	V
	10			$V_O=1V$ or $9V$	7	—	7	—	7	—	
	15			$V_O=1.5V$ or $13.5V$	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	$V_O=0.4V$, $V_I=0$ or $5V$		0.52	—	0.44	—	0.36	—	mA
	10		$V_O=0.5V$, $V_I=0$ or $10V$		1.3	—	1.1	—	0.9	—	
	15		$V_O=1.5V$, $V_I=0$ or $15V$		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O=4.6V$, $V_I=0$ or $5V$		0.52	—	0.44	—	0.36	—	mA
	10		$V_O=9.5V$, $V_I=0$ or $10V$		1.3	—	1.1	—	0.9	—	
	15		$V_O=13.5V$, $V_I=0$ or $15V$		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_O=2.5V$, $V_I=0$ or $5V$		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	$V_I=0$ or $15V$		—	0.3	—	0.3	—	1	μA

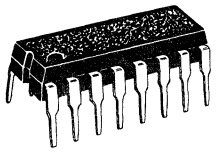
MN4585B/MN4585BS

4-Bit Magnitude Comparators

■ Description

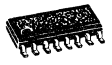
The MN4585B/S are magnitude comparators which compare 4-bit input data $A_0 \sim A_4$ and $B_0 \sim B_3$.
By using the MN4585B/S, large, small or equal signals can be obtained on the 3 output lines by the input (A<B, A = B, A>B).
For the input more than 4-bit, a 4 X N bit comparator circuit can be composed by connecting a cascade input (A<B, A = B, A>B) of the MSB side and the output of LSB side.
They are equivalent to MOTOROLA MC14585B.

P-3



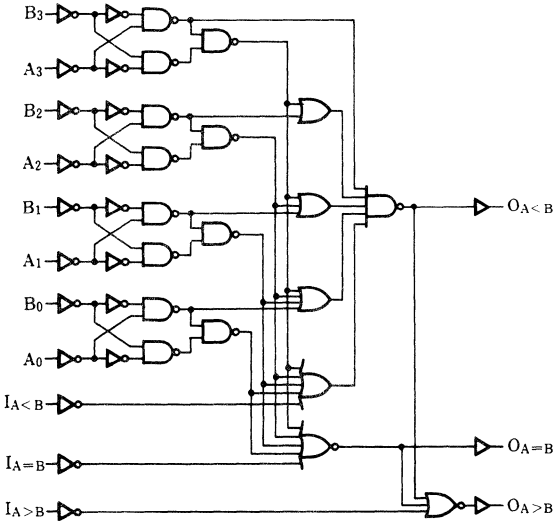
16-Pin • Plastic DIL Package

P-4

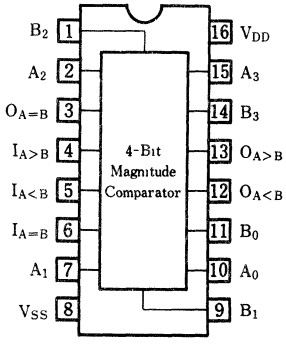


16-Pin • Panaflat Package (SO-16D)

■ Logic Diagram



Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

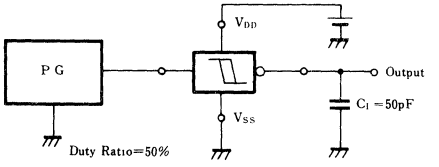
* V_{DD} + 0.5V should be under 18V

■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$) (continued)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Threshold Voltage (Fig. 2)	5	V_{IL}	1.5	2.2	—	V
	10		3	4.5	—	
	15		4	6.5	—	
Hysteresis Voltage (Fig. 2)	5	V_H	0.5	0.8	—	V
	10		0.7	1.3	—	
	15		0.9	1.8	—	
Input Capacitance		C_I	—	—	7.5	pF

Fig. 1 Switching Time Test Circuit and Waveforms

1. Test Circuit



2. Waveforms

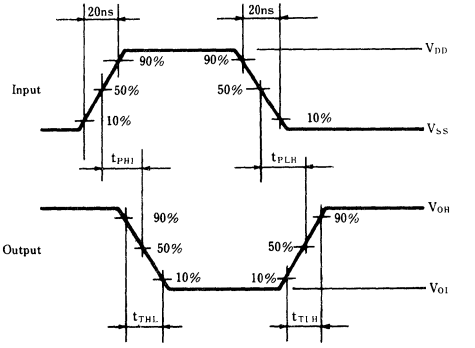
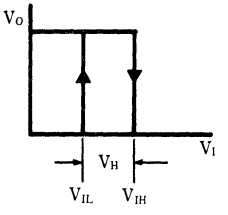
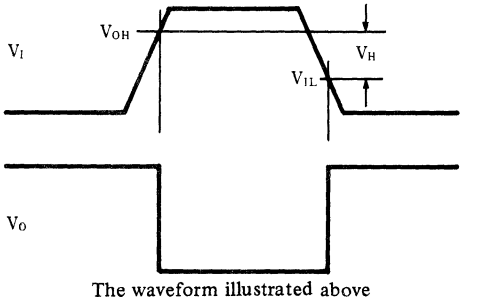


Fig. 2 Transfer Characteristics



Transfer Characteristics



The waveform illustrated above shows its definition rating 30%, to 70% limit.

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time (Fig. 1)	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time (Fig. 1)	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time (Fig. 1)	5	t_{PLH}	—	75	225	ns
	10		—	35	105	
	15		—	30	90	
Propagation Delay Time (Fig. 1)	5	t_{PHL}	—	90	270	ns
	10		—	35	105	
	15		—	30	90	
Threshold Voltage (Fig. 2)	5	V_{IH}	—	3.0	3.5	V
	10		—	5.8	7	
	15		—	8.3	11	

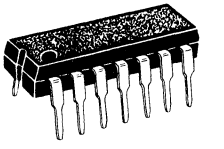
MN4584B/MN4584BS

Hex Schmitt Triggers

■ Description

The MN4584B/S have hex waveform shaping circuits.
They are used when high noise immunity is desired, and as waveform-shaping circuits to make late rise and fall time input.
The MN4548B/S are equivalent to MOTOROLA MC14584B.

P-1

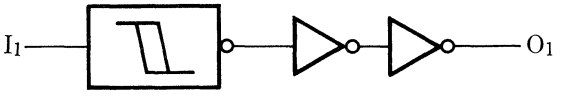


14-Pin • Plastic DIL Package

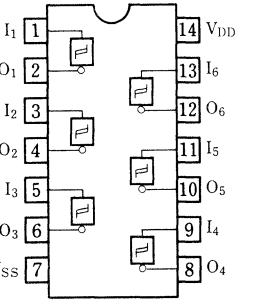
P-2

14-Pin • Panaflat Package (SO-14D)

■ Logic Diagram (1/6)



Pin Configuration



■ Maximum Ratings (Ta=25℃)

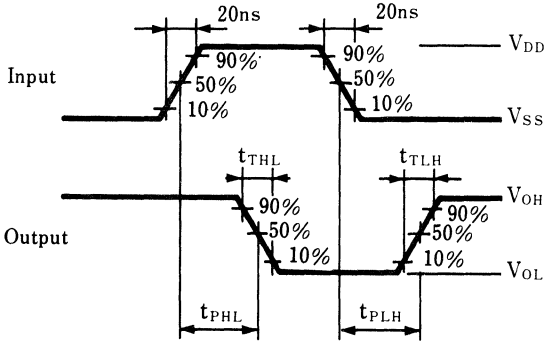
Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time An→$\overline{On}$ (H→L)	5	t_{PHL}	—	130	390	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time An→$\overline{On}$ (L→H)	5	t_{PLH}	—	105	315	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time $\overline{En}$→$\overline{On}$ (H→L)	5	t_{PHL}	—	120	360	ns
	10		—	45	135	
	15		—	30	90	
Propagation Delay Time $\overline{En}$→$\overline{On}$ (L→H)	5	t_{PLH}	—	105	315	ns
	10		—	40	120	
	15		—	30	90	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

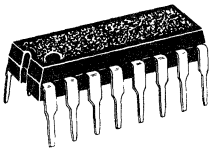
MN4556B/MN4556BS

Dual Binary to 1-of-4 Decoders

■ Description

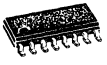
The MN4556B/S have dual decoder/demultiplexers. When enable input $\overline{E}$ = L, one output of 4 ($\overline{O}_0$, $\overline{O}_1$, $\overline{O}_2$ and $\overline{O}_3$) is selected by two binary inputs (A_0 and A_1).
When enable input E = H, selection is inhibited and all outputs become "H".
Four-bit binary is decoded to hexadecimal by bit expanision, and also converted to many kind of codes.
The MN4556B/S are equivalent to MOTOROLA MC14556B and RCA CD4556B.

P- 3



16-Pin • Plastic DIL Package

P- 4



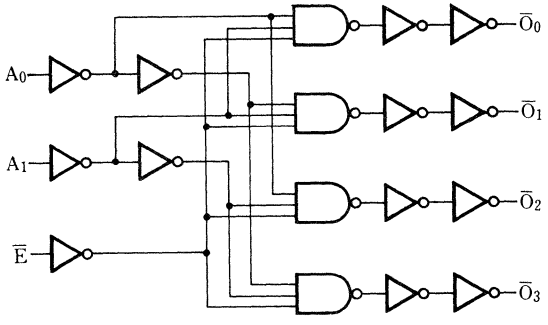
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

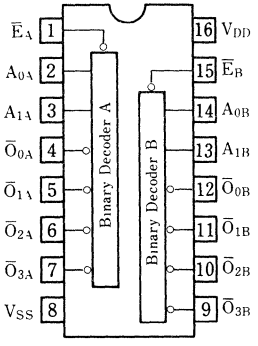
Input			Output			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	×	×	H	H	H	H

Note) × : don't care

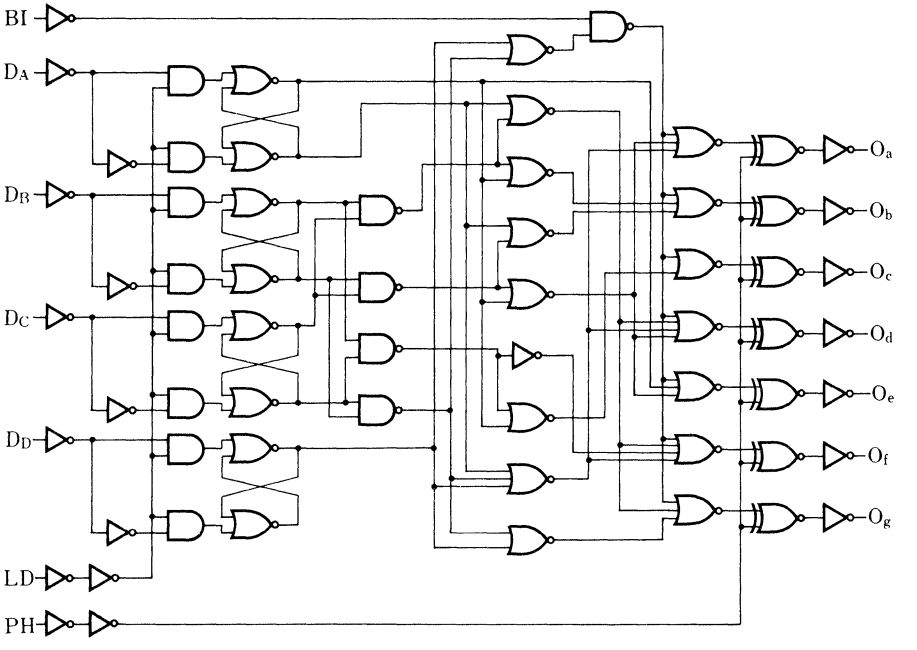
■ Logic Diagram (1/2)



Pin Configuration



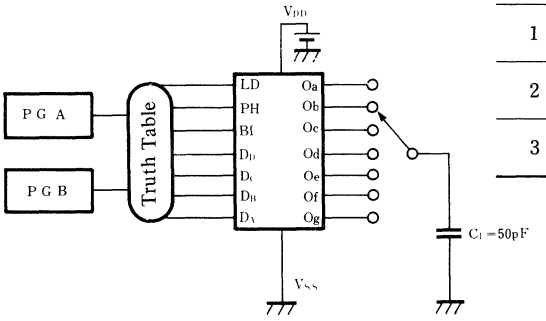
Logic Diagram



■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time Dn→On (H→L)	5	t_{PHL}	—	180	540	ns
	10		—	75	225	
	15		—	55	165	
Propagation Delay Time Dn→On (L→H)	5	t_{PLH}	—	180	540	ns
	10		—	75	225	
	15		—	55	165	
Propagation Delay Time BI→On (H→L)	5	t_{PHL}	—	145	435	ns
	10		—	65	195	
	15		—	45	135	
Propagation Delay Time BI→On (L→H)	5	t_{PLH}	—	125	375	ns
	10		—	55	165	
	15		—	40	120	
Set-up Time Dn→LD	5	t_{su}	—	20	60	ns
	10		—	5	20	
	15		—	0	15	
Hold Time Dn→LD	5	t_{hold}	—	−15	0	ns
	10		—	0	15	
	15		—	5	20	
Minimum LD Pulse Width	5	t_{WLDH}	—	30	90	ns
	10		—	15	45	
	15		—	10	30	
Input Capacitance		C_I	—	—	7.5	pF

• Switching Time Test Circuit



Condition Table (Example)

Test No.	Item	P.G. A	P.G. B	"H"	"L"
1	D_{A-D}—On	D_C	—	D_A, D_B, LD	D_D, BI, PH
2	t_{WLDH} t_{su}, t_{hold}	D_C	LD	D_A, D_B	D_D, BI, PH
3	BI—On	BI	—	D_A, D_B, LD	D_C, D_D, PH

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

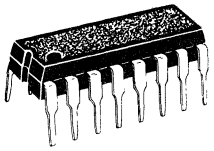
MN4543B/MN4543BS

BCD-to-Seven Segment Decoder/Drivers

■ Description

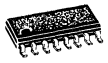
The MN4543B/S are BCD-to-seven segment decoder/drivers for liquid crystal display with BLANKING input, PHASE input and LATCH DISABLE input.
The combination of output logic level can be reversed.
PH (input), BI (blanking input) and LD (latch disable input) are available in addition to the BCD input.
PH performs phase reverse of the truth value table.
BI performs blanking display.
LD performs BCD code storage.
In order to perform liquid crystal display (LCD), a common square-wave pulse is applied to the back plane of the display device and phase input of the MN4543B/S, and the output pins should be connected to the LCD segment.
The display diagram in this catalog should be referred to for in formation regarding connection to an LED, incandescent lamp, gas discharge tube, fluorescnet lamp, etc. (except the LCD).
The MN4543B/S are used for the display driver of counters, DVM computers and calculators, watches and timers.
They are equivalent to MOTOROLA MC14543B.

P-3



16-Pin • Plastic DIL Package

P-4



16-Pin • Panaflat Package (SO-16D)

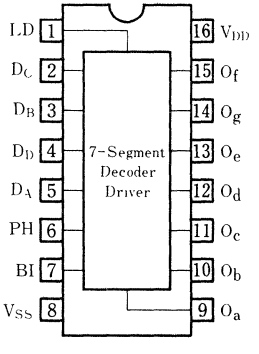
■ Truth Table

Input							Output							Display
LD	BI	PH	D_D	D_C	D_B	D_A	Oa	Ob	Oc	Od	Oe	Of	Og	
×	H	L	×	×	×	×	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	×	×	×	×	**	**	**	**	**	**	**	**
ditto		H	ditto				Opposite of above table							ditto

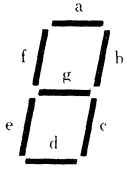
Note) × : don't care

* For LCD, square waveform is applied to PH. For a cathode common to LED, PH = L. PH = H at anode common LED.
** Previously added BCD defines at LD = H.

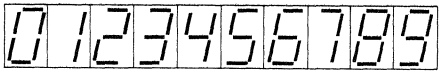
Pin Configuration



■ Segment Configuration



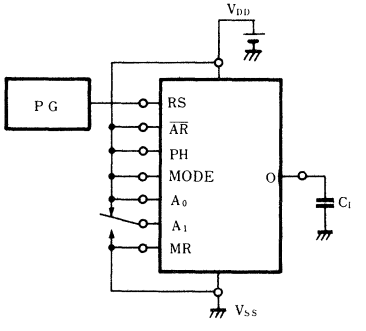
■ Display



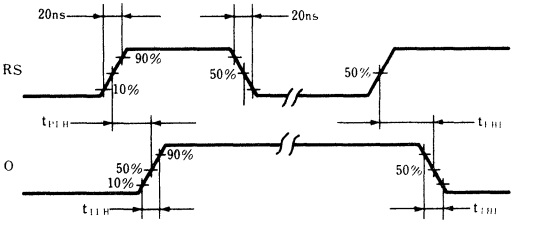
■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time RS→O 2^8 selected	5	t_{PHL} t_{PLH}	—	375	1125	ns
	10		—	150	450	
	15		—	110	330	
Propagation Delay Time RS→O 2^{10} selected	5	t_{PHL} t_{PLH}	—	425	1275	ns
	10		—	165	495	
	15		—	120	360	
Propagation Delay Time RS→O 2^{13} selected	5	t_{PHL} t_{PLH}	—	510	1530	ns
	10		—	190	570	
	15		—	135	405	
Propagation Delay Time RS→O 2^{16} selected	5	t_{PHL} t_{PLH}	—	575	1725	ns
	10		—	210	630	
	15		—	150	450	
Minimum Clock Pulse Width	5	t_{WRSL}	—	30	90	ns
	10		—	15	45	
	15		—	12	36	
Minimum Reset Pulse Width	5	t_{WMRH}	—	30	90	ns
	10		—	15	45	
	15		—	12	36	
Maximum Clock Frequency	5	fmax	8	16	—	MHz
	10		15	30	—	
	15		18	36	—	
Oscillation Frequency Rt= 5 kΩ Ct= 1 nF Rs=10kΩ	5	f_{OSC}	—	90	—	kHz
	10		—	90	—	
	15		—	90	—	
Oscillation Frequency Rt=56kΩ Ct= 1 nF Rs=120kΩ	5	f_{OSC}	—	8	—	kHz
	10		—	8	—	
	15		—	8	—	
Input Capacitance		C_I	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	Pin 5 =High Auto Reset Disabled		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Quiescent Power Supply Current	5	I_D	Pin 5 =Pin 6 =Low Power On Reset Enabled		—	80	—	80	—	230	μA
	10				—	750	—	600	—	700	
	15				—	1600	—	1300	—	1500	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\|I_O\|$<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level (C_{TC}=R_{TC}=Low)	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.33	—	0.27	—	0.20	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.00	—	0.85	—	0.68	—	
	15		V_O=1.5V, V_I=0 or 15V		3.20	—	2.70	—	2.30	—	
Output Current High Level (C_{TC}=R_{TC}=High)	5	−I_{OH}	V_O=4.6V, V_I=0 or 5V		0.5	—	0.4	—	0.3	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.4	—	1.2	—	0.95	—	
	15		V_O=13.5V, V_I=0 or 15V		4.8	—	4,0	—	3.2	—	
Output Current High Level	5	−I_{OH}	V_O=2.5V, V_I=0 or 5V		1.4	—	1.2	—	0.95	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

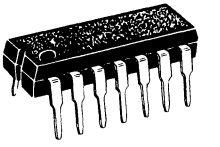
MN4541B/MN4541BS

Programmable Timers

■ Description

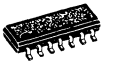
The MN4541B/S are programmable timers composed of a 16-stage binary counter, oscillator, automatic power-on reset circuit, output control and logic.
Timing starts at power ON. Counter starts its operation by the automatic reset when V_{DD} is in the specified range.
When the power is ON, external reset pulses can be applied. When the initial reset command is released, the oscillator operates by the frequency defined by the external RC network.
Each stage of the 16-stage counter divides the oscillator frequency into 2^N squares.
The external master reset operates independently of automatic reset, and rise and fall of clock time is very late operation due to the built-in clock circuit.
They are equivalent to MOTOROLA MC14541B.

P-1



14-Pin • Plastic DIL Package

P-2



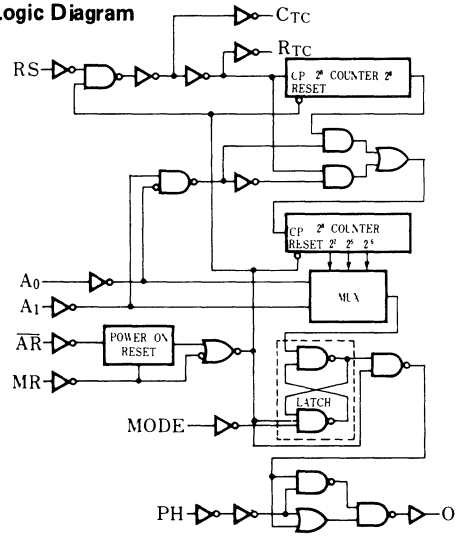
14-Pin • Panaflat Package (SO-14D)

■ Truth Table

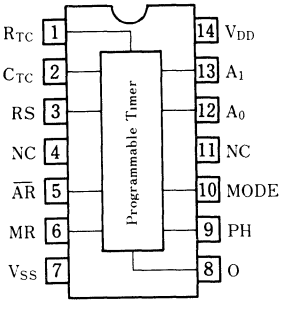
Input				Mode
$\overline{AR}$	MR	PH	MODE	
H	L	×	×	auto reset impossible
L	L	×	×	auto reset
×	H	×	×	reset
×	L	×	H	recycle mode
×	L	×	L	single cycle mode
×	L	L	×	first "L" output after reset
×	L	H	×	first "H" output after reset

Note) × : don't care

■ Logic Diagram



Pin Configuration



Pin Explanation

A_0, A_1 : Address input
MODE : Mode select input
$\overline{AR}$: Reset input
MR : Reset input
PH : Phase input
R_{TC} : External resistor (R_t) connection pin
C_{TC} : External capacitance (C_t) connection pin
RS : External resistor (R_S), or external clock input

■ Frequency Table

A_0	A_1	Count Stage Number (n)	Count (2^n)
L	L	13	8,192
L	H	10	1,024
H	L	8	256
H	H	16	65,536

■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time In→On (L→H)	5	t_{PLH}	—	120	360	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time In→On (H→L)	5	t_{PHL}	—	120	360	ns
	10		—	45	135	
	15		—	30	90	
Propagation Delay Time Sn→On (L→H)	5	t_{PLH}	—	155	465	ns
	10		—	60	180	
	15		—	40	120	
Propagation Delay Time Sn→On (H→L)	5	t_{PHL}	—	165	495	ns
	10		—	65	195	
	15		—	40	120	
Propagation Delay Time $\overline{En}$→On (L→H)	5	t_{PLH}	—	100	300	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time $\overline{En}$→On (H→L)	5	t_{PHL}	—	100	300	ns
	10		—	40	120	
	15		—	30	90	
Input Capacitance		C_I	—	—	7.5	pF

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0 5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

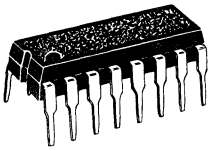
MN4539B/MN4539BS

Dual 4-Input Multiplexers

■ Description

The MN4539B/S are 4-channel data selectors which select data inputs by common select inputs (S_0, S_1).
Each input of the two circuits appears at the outputs by the combination of select inputs during High enable input.
A Low at enable input forces outputs Low, independent of any other inputs. Applications are such areas as signal synthesizers and parallel-to-serial conversions.
The MN4539B/S are equivalent to MOTOROLA MC14539B.

P- 3



16-Pin • Plastic DIL Package

P- 4

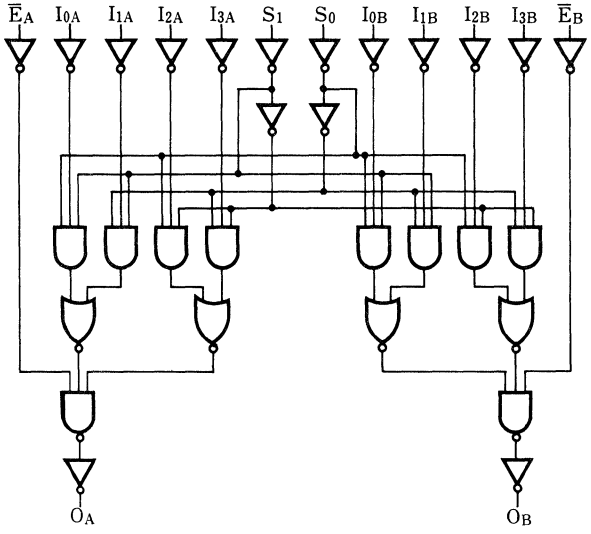
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

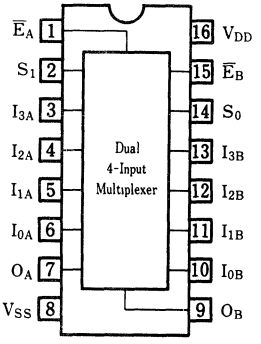
Input			Output
S_0	S_1	$\overline{E}$	O
×	×	H	L
L	L	L	I_0
H	L	L	I_1
L	H	L	I_2
H	H	L	I_3

Note) × : don't care

■ Logic Diagram



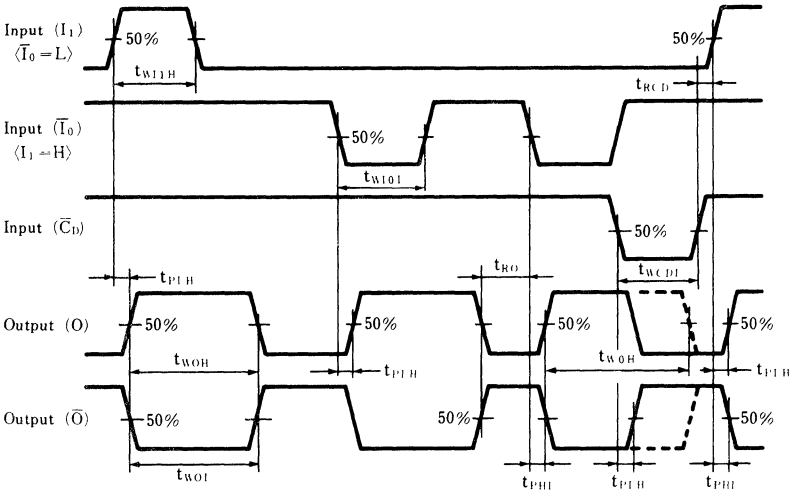
Pin Configuration



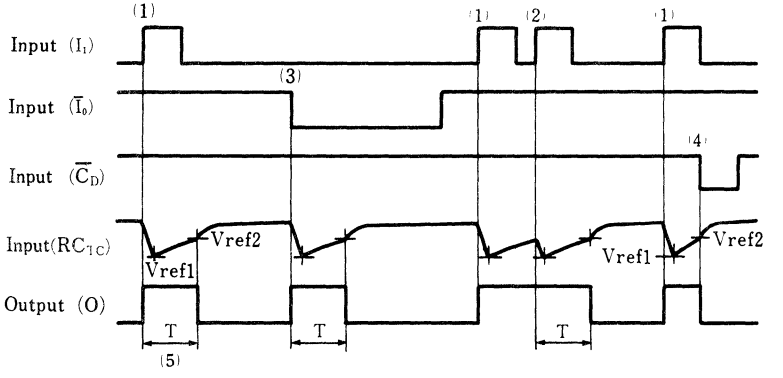
Pin Explanation

I_{0A}, I_{1A}, I_{2A}, I_{3A} : Multiplexer input
I_{0B}, I_{1B}, I_{2B}, I_{3B} : Multiplexer input
S_0, S_1 : Select input
$\overline{E}_A$, $\overline{E}_B$: Enable input
O_A, O_B : Multiplexer output

• Dynamic Signal Waveforms



■ Timing Diagram



(1) Positive edge triggering
(2) Positive edge re-triggering(pulse lengthening)
(3) Negative edge triggering
(4) Reset (pulse shortening)
(5) T=Rt×Ct

Switching Characteristics ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $\overline{I_0}$, $I_1 \rightarrow O$	5	t_{PHL}	—	150	450	ns
	10		—	70	210	
	15		—	40	120	
Propagation Delay Time $\overline{I_0}$, $I_1 \rightarrow \overline{O}$	5	t_{PLH}	—	150	450	ns
	10		—	70	210	
	15		—	40	120	
Propagation Delay Time $\overline{C_D} \rightarrow O$	5	t_{PHL}	—	150	450	ns
	10		—	70	210	
	15		—	40	120	
Propagation Delay Time $\overline{C_D} \rightarrow \overline{O}$	5	t_{PLH}	—	150	450	ns
	10		—	70	210	
	15		—	40	120	
Recovery Time $\overline{C_D} \rightarrow \overline{I_0}$, I_1	5	t_{RCD}	—	0	—	ns
	10		—	0	—	
	15		—	0	—	
Recovery Time O, $\overline{O} \rightarrow \overline{I_0}$, I_1	5	t_{RO}	—	0	—	ns
	10		—	0	—	
	15		—	0	—	
Minimum Pulse Width $\overline{I_0}$	5	t_{WI0l}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Minimum Pulse Width I_1	5	t_{WI1L}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Minimum Pulse Width $\overline{C_D}$	5	t_{WCDL}	—	40	120	ns
	10		—	20	60	
	15		—	15	45	
Output Pulse Width ($Rt=100k\Omega$, $Ct=0.002\mu F$)	5	t_{WO}	—	208	—	μs
	10		—	208	—	
	15		—	208	—	
Output Pulse Width ($Rt=100k\Omega$, $Ct=0.1\mu F$)	5	t_{WO}	—	10.4	—	ns
	10		—	10.4	—	
	15		—	10.4	—	
Output Pulse Width ($Rt=100k\Omega$, $Ct=10\mu F$)	5	t_{WO}	—	1.04	—	s
	10		—	1.04	—	
	15		—	1.04	—	
Input Capacitance		C_I	—	—	7.5	pF
External Timing Resistance		Rt	5	—	1000	kΩ
External Timing Capacitance		Ct	2000	—	no limit	pF

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

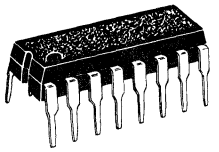
MN4538B/MN4538BS

Dual Precision Monostable Multivibrators

■ Description

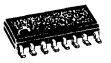
The MN4538B/S are monostable multivibrators with the capability of reset and re-trigger.
Trigger can be performed from both the positive and negative going edge of the input pulse.
A wide range of precise output pulses can be obtained since the width and precision of the output pulse are defined by external C_t and R_t.
Output pulse width control is more precisely performed, due to linear CMOS technology.
Total power supply voltage range is obtained as $t_{WO} = R_r \cdot C_t$ and no other coefficient is included.
The MN4538B/S are equivalent to MOTOROLA MC14538B.

P-3



16-Pin • Plastic DIL Package

P-4

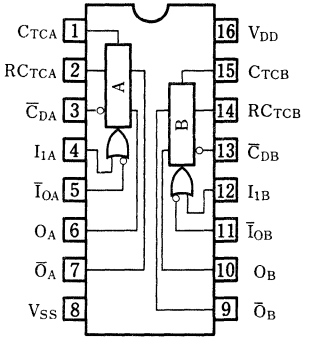


16-Pin • Panaflat Package (SO-16D)

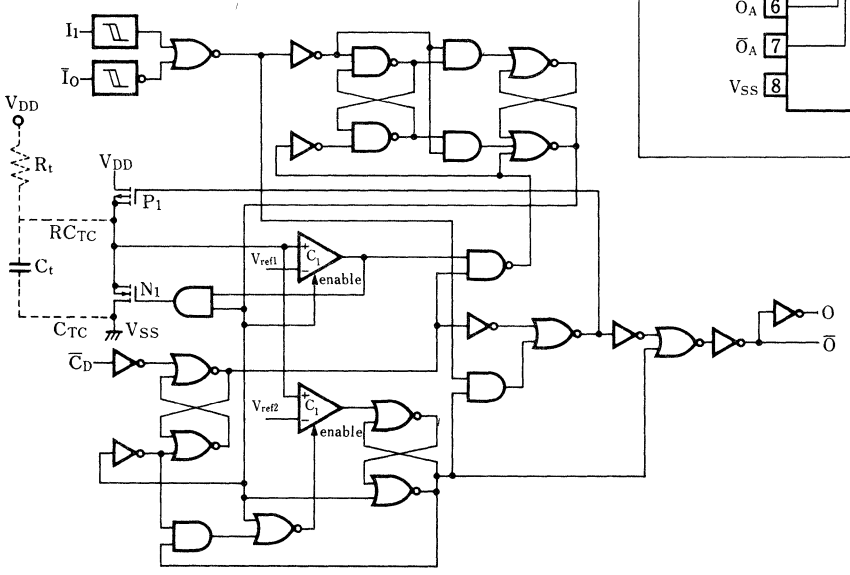
■ Truth Table

Input			Output	
$\bar{I}_0$	I_1	$\bar{C}_D$	O	$\bar{O}$
↓	L	H	⎍	⎎
H	↑	H	⎍	⎎
×	×	L	L	H

Pin Configuration



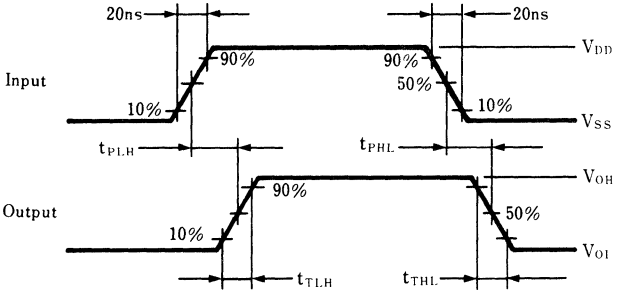
■ Logic Diagram (1/2)



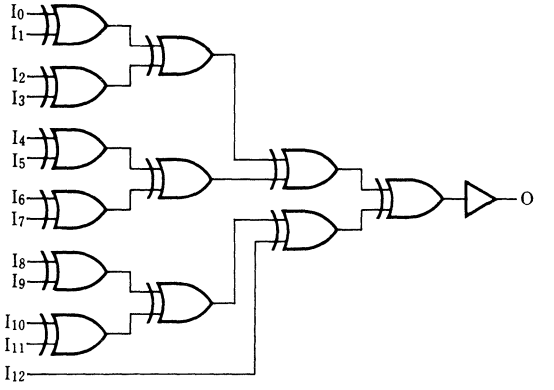
■ Switching Characteristics ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $I_0 \sim I_{11} \rightarrow O$ (H→L)	5	t_{PHL}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Propagation Delay Time $I_0 \sim I_{11} \rightarrow O$ (L→H)	5	t_{PLH}	—	135	405	ns
	10		—	55	165	
	15		—	45	135	
Propagation Delay Time $I_{12} \rightarrow O$ (H→L)	5	t_{PHL}	—	105	315	ns
	10		—	45	135	
	15		—	35	105	
Propagation Delay Time $I_{12} \rightarrow O$ (L→H)	5	t_{PLH}	—	85	255	ns
	10		—	35	105	
	15		—	25	75	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



■ Logic Diagram



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

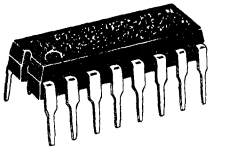
MN4531B/MN4531BS

12-Bit Parity Trees

■ Description

The MN4531B/S are 12-bit parity trees constructed with P and N channel enhancement modes.
The circle is composed of 12 data bit input ($I_0 \sim I_{11}$) and an odd or even parity selection input (I_{12}) and output (O).
This parity selection bit input is an added bit.
For words less than 12 bits, either even or odd parity output can be obtained depending on whether the other input is odd or even.
When the MN4531B/S are cascade-connected by using I_{12} input, more than 13-bit words can be processed.
The MN4531B/S are widely used for error detection/correction systems of data, controllers for remote digital sensors, miuti arithmetic units without carry, etc.

P-3



16-Pin • Plastic DIL Package

P-4

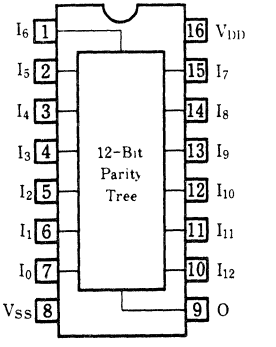
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

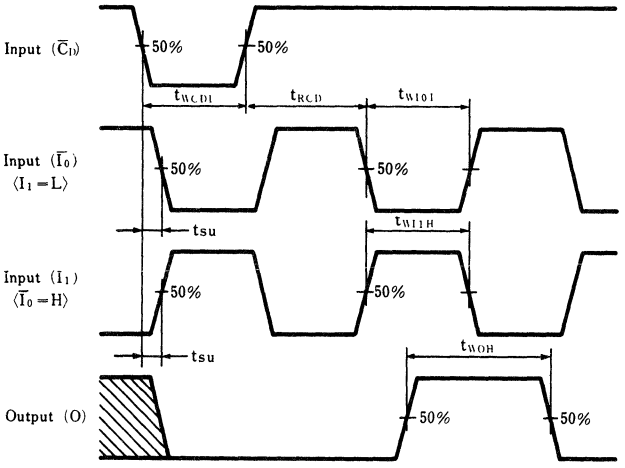
Input								Output
I_{12}	I_{11}	I_{10}	·····	I_2	I_1	I_0	Binary (Octodecimal)	0*
0	0	0	·····	0	0	0	0 (0)	0
0	0	0	·····	0	0	1	1 (1)	1
0	0	0	·····	0	1	0	2 (2)	1
0	0	0	·····	0	1	1	3 (3)	0
0	0	0	·····	1	0	0	4 (4)	1
0	0	0	·····	1	0	1	5 (5)	0
0	0	0	·····	1	1	0	6 (6)	0
0	0	0	·····	1	1	1	7 (7)	1
⋮	⋮	⋮	····· ·····	⋮	⋮	⋮	⋮	⋮
1	1	1	·····	0	0	0	8184 (17770)	0
1	1	1	·····	0	0	1	8185 (17771)	1
1	1	1	·····	0	1	0	8186 (17772)	1
1	1	1	·····	0	1	1	8187 (17773)	0
1	1	1	·····	1	0	0	8188 (17774)	1
1	1	1	·····	1	0	1	8189 (17775)	0
1	1	1	·····	1	1	0	8190 (17776)	0
1	1	1	·····	1	1	1	8191 (17777)	1

Note) * 0 = Even Parity; 1 = Odd Parity

Pin Configuration



• Dynamic Signal Waveforms



Waveforms showing minimum $\overline{I}_0$, I_1 and O pulse widths, set-up and recovery times; set-up and recovery times are shown as positive values but may be specified as negative values.

■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time I_0, $I_1 \rightarrow O$	5	t_{PLH}	—	155	465	ns
	10		—	60	180	
	15		—	40	120	
Propagation Delay Time I_0, $I_1 \rightarrow \overline{O}$	5	t_{PHL}	—	140	420	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time $C_D \rightarrow O$	5	t_{PHL}	—	105	315	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time $C_D \rightarrow \overline{O}$	5	t_{PLH}	—	120	360	ns
	10		—	50	150	
	15		—	35	105	
Minimum Pulse Width I_0	5	t_{WI0L}	—	25	75	ns
	10		—	15	45	
	15		—	10	30	
Minimum Pulse Width I_1	5	t_{WI1L}	—	25	75	ns
	10		—	15	45	
	15		—	10	30	
Minimum Pulse Width C_D	5	t_{WCDL}	—	30	90	ns
	10		—	15	45	
	15		—	10	30	
Output Pulse Width (Rt= 5 kΩ, Ct=15pF)	5	t_{WOH}	—	235	—	ns
	10		—	155	—	
	15		—	140	—	
Output Pulse Width (Rt=10kΩ, Ct=1000pF)	5	t_{WOH}	—	5.45	—	μs
	10		—	4.95	—	
	15		—	4.85	—	
Input Capacitance		C_I	—	—	7.5	pF
External Timing Resistance		Rt	5	—	1000	kΩ
External Timing Capacitance (Note)		Ct	—	—	10	μF

(Note) It is recommended to use the silicon diode (cathode toward V_{DD}) in parallel with R_t when C_t is large capacity (ranging from 0.1μF to 10μF).

Truth Table

Input			Output		Mode
I_1	$\overline{I}_0$	$\overline{C}_D$	O	$\overline{O}$	
↑	H	H	↑	↓	output pulse
↑	L	H	L	H	inhibit
H	↓	H	L	H	
L	↓	H	↑	↓	output pulse
×	×	L	L	H	inhibit

Note) X : don't care

Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		|I_O|<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		|I_O|<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	|I_O|<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	|I_O|<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

MN4528B/MN4528BS

Dual Monostable Multivibrators

■ Description

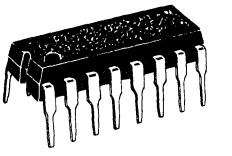
The MN4528B/S are retriggerable, resettable monostable multivibrators and have 2 circuits in a package. The monostable pulse over a wide range of widths is determined by the external resistance and capacitance.

A negative going edge of the $\overline{I_0}$ input when I_1 is Low or a positive going edge of the I_1 input when $\overline{I_0}$ is High produces a positive pulse at the O output and a negative pulse at the O output if the $\overline{C_D}$ input is High.

A Low at the $\overline{C_D}$ input forces the O output Low and the $\overline{O}$ output High.

The MN4528B/S are equivalent to MOTOROLA MC14528B.

P- 3



16-Pin • Plastic DIL Package

P- 4

16-Pin • Panaflat Package (SO-16D)

Pin Explanation

$\overline{I}_{0A}$, $\overline{I}_{0B}$: Input (⌝⌞)

I_{1A}, I_{1B} : Input (⌞⌜)

$\overline{C}_{DA}$, $\overline{C}_{DB}$: Direct Clear Input

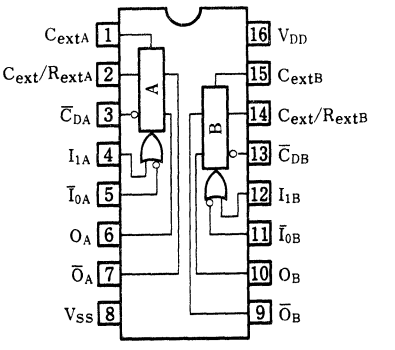
$Cext_A$, $Cext_B$: External capacitance connection

$Cext/Rext_A$, $Cext/Rext_B$: External capacitance, External resistance

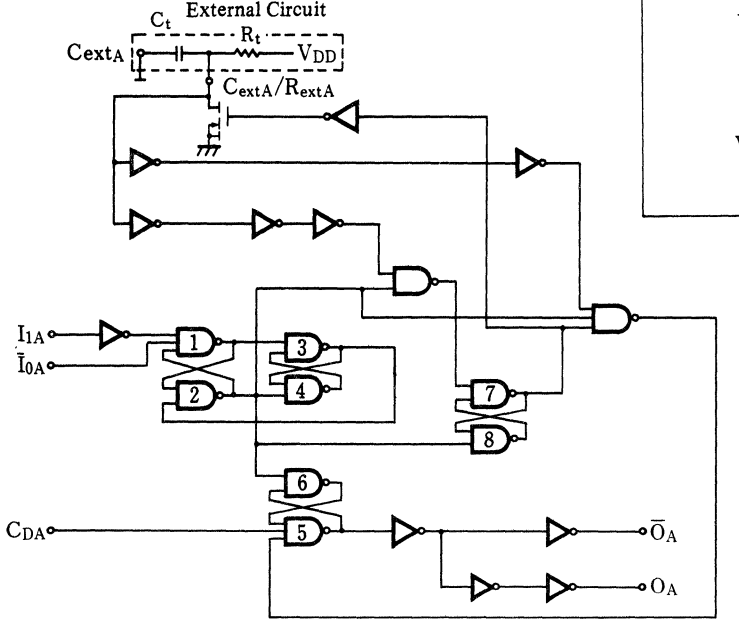
O_A, O_B : Positive output

$\overline{O}_A$, $\overline{O}_B$: Negative output

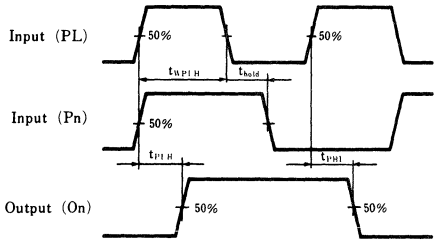
Pin Configuration



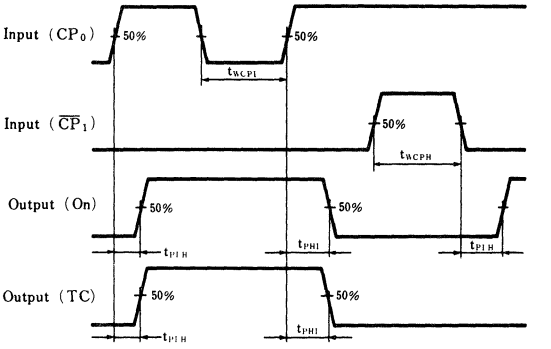
■ Logic Diagram (1/2)



• Dynamic Signal Waveforms

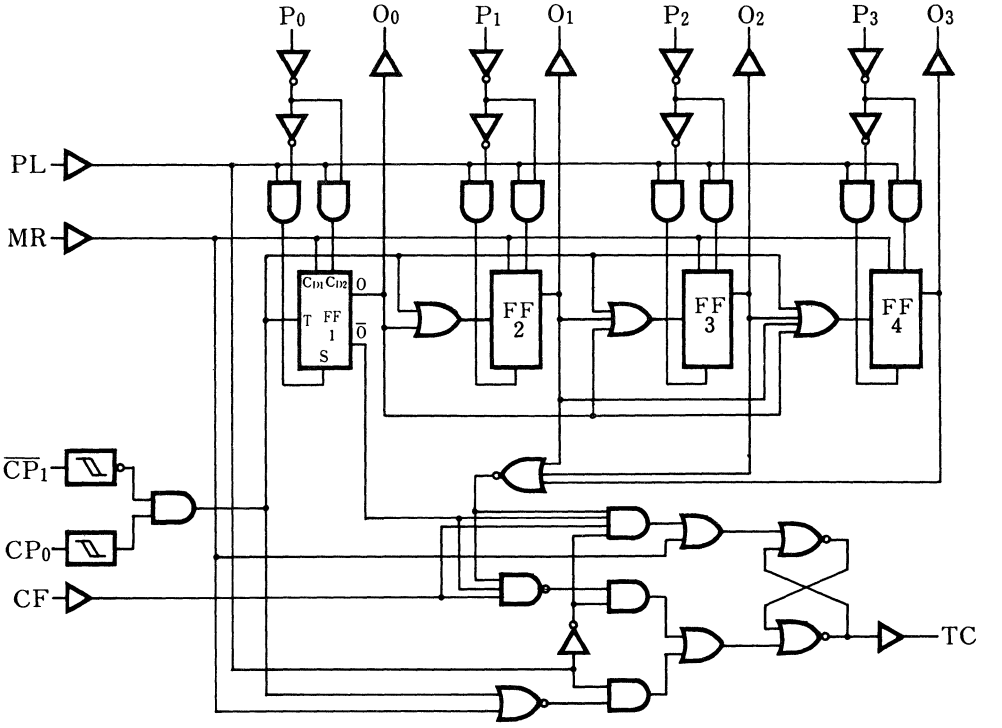


Waveforms showing minimum PL pulse width, propagation delays for PL, P_n to O_n and hold time for PL to P_n



Waveforms showing minimum CP_0 and $\overline{CP}_1$ pulse widths, propagation delays for CP_0, $\overline{CP}_1$ to O_n and TC

■ Logic Diagram



■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP_0, $\overline{CP}_1 \rightarrow On$ (H→L)	5	t_{PHL}	—	150	450	ns
	10		—	65	195	
	15		—	50	150	
Propagation Delay Time CP_0, $\overline{CP}_1 \rightarrow On$ (L→H)	5	t_{PLH}	—	150	450	ns
	10		—	65	195	
	15		—	50	150	
Propagation Delay Time CP_0, $\overline{CP}_1 \rightarrow TC$ (H→L)	5	t_{PHL}	—	210	630	ns
	10		—	90	270	
	15		—	70	210	
Propagation Delay Time CP_0, $\overline{CP}_1 \rightarrow TC$ (L→H)	5	t_{PLH}	—	210	630	ns
	10		—	90	270	
	15		—	70	210	
Propagation Delay Time PL→On (H→L)	5	t_{PHL}	—	200	600	ns
	10		—	80	240	
	15		—	60	180	
Propagation Delay Time PL→On (L→H)	5	t_{PLH}	—	180	540	ns
	10		—	70	210	
	15		—	50	150	
Propagation Delay Time MR→On (H→L)	5	t_{PHL}	—	140	420	ns
	10		—	55	165	
	15		—	40	120	
Minimum CP_0 Pulse Width	5	t_{WCPL}	—	40	120	ns
	10		—	20	60	
	15		—	15	45	
Minimum CP_1 Pulse Width	5	t_{WCPH}	—	40	120	ns
	10		—	20	60	
	15		—	15	45	
Minimum PL Pulse Width	5	t_{WPLH}	—	50	150	ns
	10		—	20	60	
	15		—	16	48	
Minimum MR Pulse Width	5	t_{WMRH}	—	65	195	ns
	10		—	25	75	
	15		—	20	60	
Hold Time Pn→ PL	5	t_{hold}	—	35	105	ns
	10		—	30	90	
	15		—	25	75	
Maximum Clock Frequency (PL=L)	5	fmax	6	12	—	MHz
	10		12	25	—	
	15		16	32	—	
Input Capacitance		C_I	—	—	7.5	pF

Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

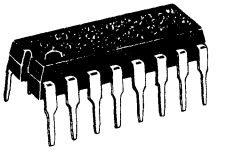
MN4526B/MN4526BS

Programmable 4-Bit Binary Counters

Description

The MN4526B/S are programmable 4-bit binary counters.
Cascade N dividing action can be performed by the cascade feedback input without an external gate.
They offer synchronization start of the N division cycle by a master reset function and disable of the pulse count function by the clock inhibit input.
The MN4526B/S are suitable for frequency division where low power dissipation and high noise immunity are desired, such as for frequency synthesizers and PLLs.

P-3



16-Pin • Plastic DIL Package

P-4

16-Pin • Panaflat Package (SO-16D)

Count Mode

Count	Output			
	O_3	O_2	O_1	O_0
15	H	H	H	H
14	H	H	H	L
13	H	H	L	H
12	H	H	L	L
11	H	L	H	H
10	H	L	H	L
9	H	L	L	H
8	H	L	L	L
7	L	H	H	H
6	L	H	H	L
5	L	H	L	H
4	L	H	L	L
3	L	L	H	H
2	L	L	H	L
1	L	L	L	H
0	L	L	L	L

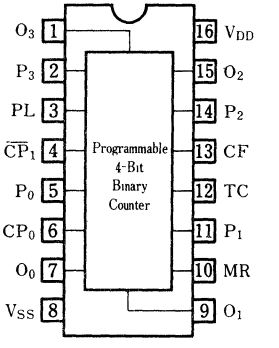
Note) CF = H; PL = L; MR = L

Truth Table

MR	PL	CP_0	$\overline{CP}_1$	Mode
H	×	×	×	reset (sync.)
L	H	×	×	preset (sync.)
L	L	↑	H	no change
L	L	L	↓	
L	L	↓	×	
L	L	×	↑	
L	L	↑	L	counter advance
L	L	H	↓	

Note) X : don't care

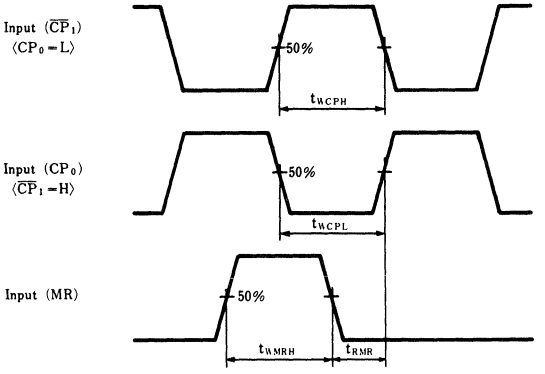
Pin Configuration



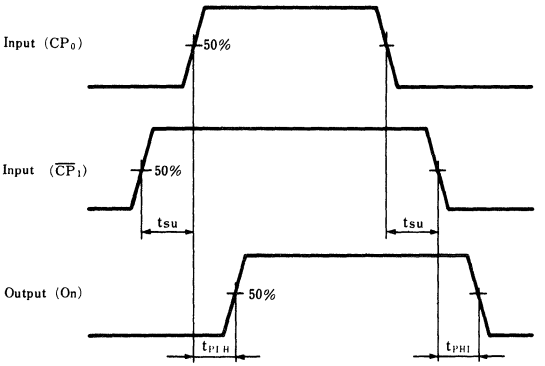
Pin Explanation

PL : Parallel load input
P_0~P_3: Parallel input
CF : Cascade feedback input
CP_0 : Clock input (L → H)
$\overline{CP}_1$: Clock input (H → L)
MR : Asynchronous master reset input
TC : Pin count output
O_0~O_3: Buffer parallel output

• Dynamic Signal Waveforms

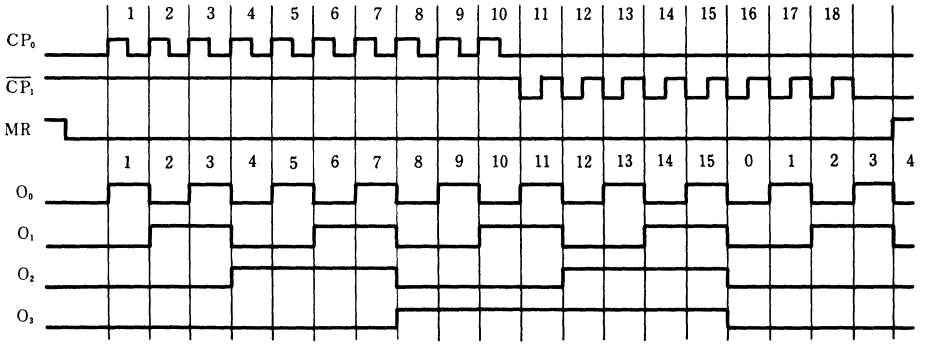


Waveforms showing recovery time for MR; minimum CP_0, $\overline{CP}_1$ and MR pulse widths



Waveforms showing set-up times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0, and propagation delays

■ Timing Diagram



■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP_0, $\overline{CP}_1$→On (L→H)	5	t_{PLH}	—	145	435	ns
	10		—	65	195	
	15		—	50	150	
Propagation Delay Time CP_0, $\overline{CP}_1$→On (H→L)	5	t_{PHL}	—	170	510	ns
	10		—	75	225	
	15		—	50	150	
Propagation Delay Time MR→On (H→L)	5	t_{PHL}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Low Level Minimum Clock CP_0 Pulse Width	5	t_{WCPL}	—	85	255	ns
	10		—	30	90	
	15		—	25	75	
High Level Minimum Clock $\overline{CP}_1$ Pulse Width	5	t_{WCPH}	—	85	255	ns
	10		—	30	90	
	15		—	25	75	
High Level Minimum Reset Pulse Width	5	t_{WMRH}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	
Reset Recovery Time	5	t_{RMR}	—	25	75	ns
	10		—	15	45	
	15		—	10	30	
Set-up Time CP_0→$\overline{CP}_1$	5	tsu	—	90	270	ns
	10		—	35	105	
	15		—	25	75	
Set-up Time $\overline{CP}_1$→CP_0	5	tsu	—	75	225	ns
	10		—	30	90	
	15		—	20	60	
Maximum Clock Frequency	5	fmax	3	6	—	MHz
	10		7	15	—	
	15		10	21	—	
Input Capacitance		C_I	—	—	7.5	pF

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

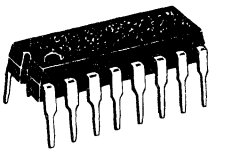
MN4520B / MN4520BS

Dual 4-Bit Binary Counters

■ Description

The MN4520B/S are dual 4-bit binary counters.
The counter advances on the positive going edge of the CP_0 when $\overline{CP}_1$ is High or on the negative going edge of the $\overline{CP}_1$ when the CP_0 is Low.
A High on the reset input clears the counter ($O_0 \sim O_3$ = L).
The MN4520B/S are equivalent to MOTOROLA MC14520B and RCA CD4520B.

P-3



16-Pin • Plastic DIL Package

P-4

16-Pin • Panaflat Package (SO-16D)

■ Truth Table

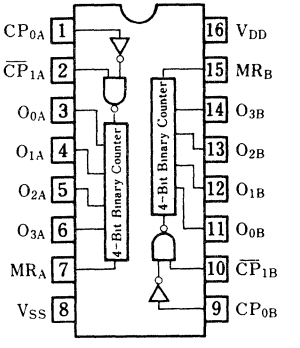
CP_0	$\overline{CP}_1$	MR	Mode
↑	H	L	counter advance
L	↓	L	
↓	×	L	no change
×	↑	L	
↑	L	L	
H	↓	L	
×	×	H	$O_0 \sim O_3$ = L

Note) × : don't care

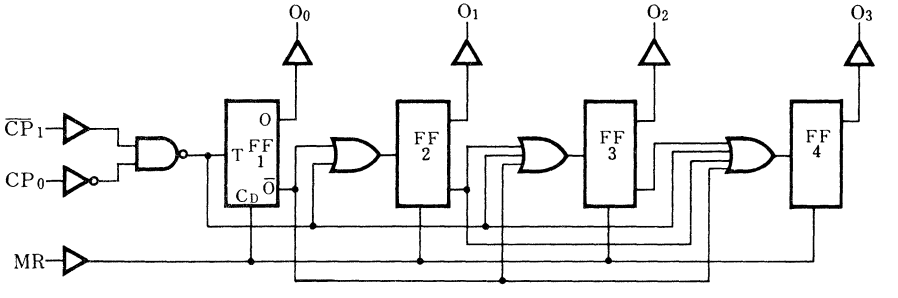
Pin Explanation

CP_{0A}, CP_{0B} : Positive clock input (↑)
$\overline{CP}_{1A}$, $\overline{CP}_{1B}$: Negative clock input (↓)
MR_A, MR_B : Reset input
$O_{0A} \sim O_{3A}$: BCD output (4 Bits)
$O_{0B} \sim O_{3B}$: BCD output (4 Bits)

Pin Configuration



■ Logic Diagram (1/2)



■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time An, Bn→On (H→L)	5	t_{PHL}	—	100	300	ns
	10		—	45	135	
	15		—	35	105	
Propagation Delay Time An, Bn→On (L→H)	5	t_{PLH}	—	90	270	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time S_A, S_B→On (H→L)	5	t_{PHL}	—	95	285	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time S_A, S_B→On (L→H)	5	t_{PLH}	—	85	255	ns
	10		—	40	120	
	15		—	30	90	
Input Capacitance		C_I	—	—	7.5	pF

■ Maximum Ratings (Ta=25℃)

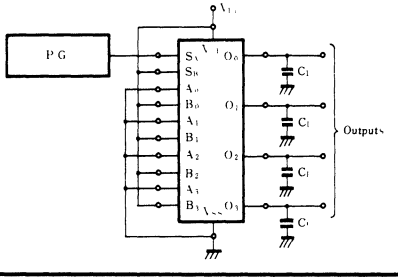
Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

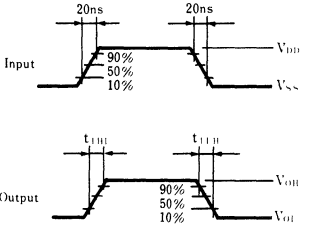
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

1. Switching Time Test Circuit



2. Waveforms



MN4519B/MN4519BS

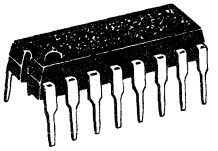
Quad 2-Input Multiplexers

■ Description

The MN4519B/S have following functions in one package.

* 4-Bit AND/OR selector
* Quad 2-input data selector
* Quad Exclusive-NOR gate

P- 3



16-Pin • Plastic DIL Package

P- 4

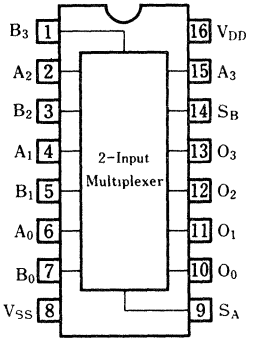
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

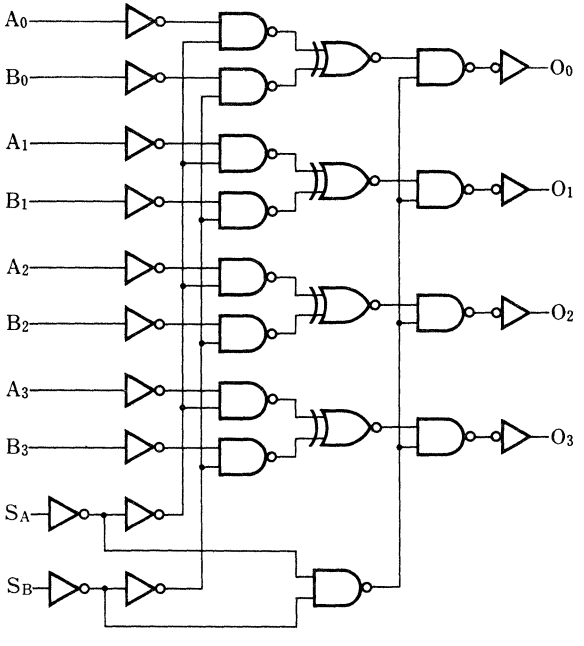
Input				Output
S_A	S_B	A_n	B_n	O_n
L	L	×	×	L
H	L	A_n	×	A_n
L	H	×	B_n	B_n
H	H	L	L	H
H	H	H	L	L
H	H	L	H	L
H	H	H	H	H

Note) X : don't care

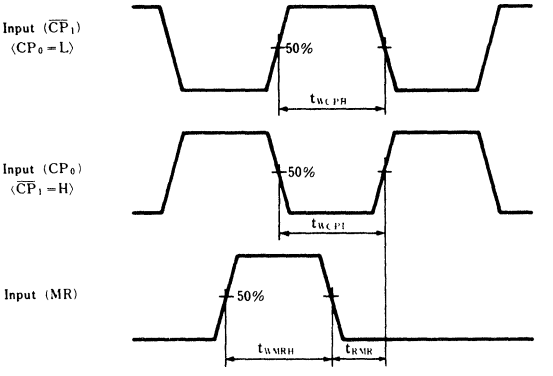
■ Pin Configuration



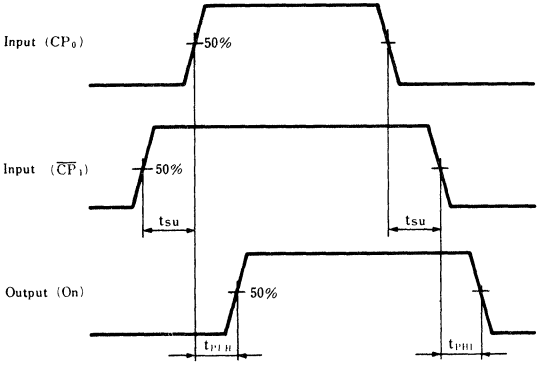
■ Logic Diagram



• Dynamic Signal Waveforms

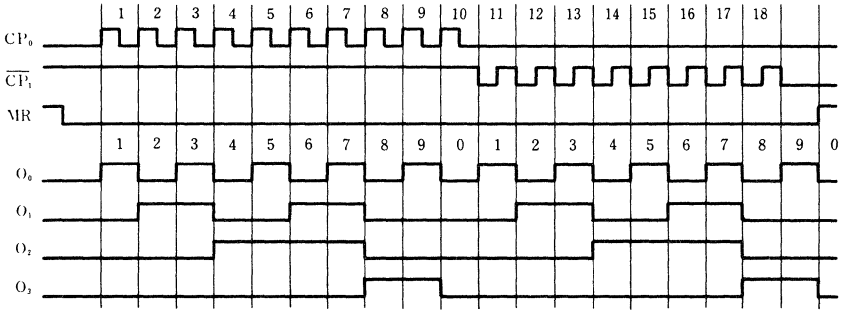


Waveforms showing recovery time for MR; minimum CP_0, $\overline{CP}_1$ and MR pulse widths



Waveforms showing set-up times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0, and propagation delays

■ Timing Diagram



■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow On$ (H→L)	5	t_{PHL}	—	170	510	ns
	10		—	75	225	
	15		—	50	150	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow On$ (L→H)	5	t_{PLH}	—	145	335	ns
	10		—	65	195	
	15		—	50	150	
Propagation Delay Time MR→On (H→L)	5	t_{PHL}	—	145	335	ns
	10		—	60	180	
	15		—	45	135	
Minimum Clock CP_0 Pulse Width	5	t_{WCPL}	—	85	255	ns
	10		—	30	90	
	15		—	25	75	
Minimum Clock CP_1 Pulse Width	5	t_{WCPH}	—	85	255	ns
	10		—	30	90	
	15		—	25	75	
Minimum Reset Pulse Width	5	t_{WMRH}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	
Reset Recovery Time	5	t_{RMR}	—	25	75	ns
	10		—	15	45	
	15		—	10	30	
Set-up Time $CP_0 \rightarrow \overline{CP}_1$	5	tsu	—	90	270	ns
	10		—	35	105	
	15		—	25	75	
Set-up Time $\overline{CP}_1 \rightarrow CP_0$	5	tsu	—	75	225	ns
	10		—	30	90	
	15		—	20	60	
Maximum Clock Frequency	5	fmax	3	6	—	MHz
	10		7	15	—	
	15		10	21	—	
Input Capacitance		C_I	—	—	7.5	pF

■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} | I_O | <1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} | I_O | <1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	| I_O | <1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	| I_O | <1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

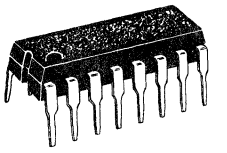
MN4518B / MN4518BS

Dual 4-Bit BCD Counters

■ Description

The MN4518B/S are dual BCD UP counters which enable count up to the second order of the BCD and division of the frequency.
All outputs ($O_0 \sim O_3$) become low during 1 High on the reset input, independent of the clock input. The counter advances on the positive going edge of the CP_0 when the $\overline{CP}_1$ is High or on the negative going edge of the $\overline{CP}_1$ when the CP_0 is Low.
The MN4516B/S are equivalent to MOTOROLA MC14518B and RCA DE4518B.

P-3



16-Pin • Plastic DIL Package

P-4

16-Pin • Panaflat Package (SO-16D)

■ Truth Table

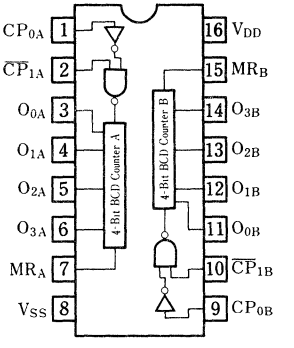
CP_0	$\overline{CP}_1$	MR	Mode
↑	H	L	counter advance
L	↓	L	
↓	×	L	no change
×	↑	L	
↑	L	L	
H	↓	L	
×	×	H	$O_0 \sim O_3 = L$

Note) X : don't care

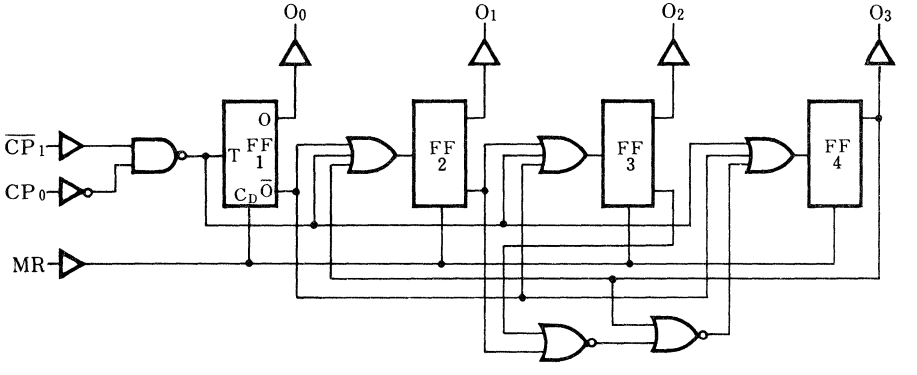
Pin Explanation

CP_{0A}, CP_{0B} : Positive clock input (↑)
$\overline{CP}_{1A}$, $\overline{CP}_{1B}$: Negative clock input (↓)
MR_A, MR_B : Reset input
$O_{0A} \sim O_{3A}$: BCD output (4 Bits)
$O_{0B} \sim O_{3B}$: BCD output (4 Bits)

Pin Configuration



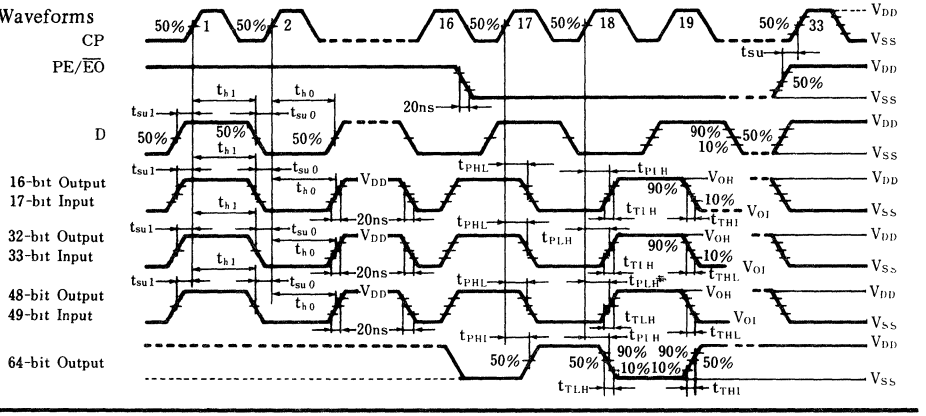
■ Logic Diagram (1/2)



■ Switching Characteristics (Ta=25℃, V_{SS}=0V, C_L=50pF)

Item	V_{DD}(V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time CP→On (H→L)	5	t_{PHL}	—	220	660	ns
	10		—	85	255	
	15		—	60	180	
Propagation Delay Time CP→On (L→H)	5	t_{PLH}	—	190	570	ns
	10		—	75	225	
	15		—	50	150	
High Level Output Disable Time PE/$\overline{EO}$→On (H)	5	t_{PHZ}	—	40	120	ns
	10		—	30	90	
	15		—	25	75	
Low Level Output Disable Time PE/$\overline{EO}$→On (L)	5	t_{PLZ}	—	50	150	ns
	10		—	30	90	
	15		—	25	75	
High Level Output Enable Time PE/$\overline{EO}$→On (H)	5	t_{PZH}	—	45	135	ns
	10		—	25	75	
	15		—	20	60	
Low Level Output Enable Time PE/$\overline{EO}$→On (L)	5	t_{PZL}	—	60	180	ns
	10		—	30	90	
	15		—	25	75	
Set-up Time On, D→CP	5	tsu	—	10	30	ns
	10		—	5	25	
	15		—	5	20	
Hold Time On, D→CP	5	t_{hold}	—	15	45	ns
	10		—	10	30	
	15		—	10	25	
Maximum Clock Frequency	5	fmax	2	5	—	MHz
	10		6	12	—	
	15		8	16	—	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		±I_I	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	50	—	50	—	375	μA
	10				—	100	—	100	—	700	
	15				—	200	—	200	—	1500	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		|I_O|<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		|I_O|<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	|I_O|<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	|I_O|<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	−I_{OH}	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	±I_I	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA
3-State Output Pin: Leakage Current High Level	15	I_{OZH}	V_O=V_{DD}		—	1.6	—	1.6	—	12	μA
3-State Output Pin: Leakage Current Low Level	15	−I_{OZL}	V_O=V_{SS}		—	1.6	—	1.6	—	12	

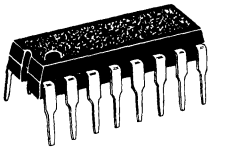
MN4517B / MN4517BS

Dual 64-Bit Static Shift Registers

■ Description

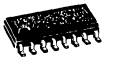
The MN4517B/S are dual 64-bit static shift registers which have two independent 64-bit registers.
Each register can be used independently since they have their own clock input and write enable.
Outputs of 16, 32, 48 and 64 bits are available.
Data added in the data input is input to the register by clock regardless of the write enable input mode.
When wire enable input becomes "H" level, output becomes disable (high impedance mode), and when the clock pulse is applied, it is input to the input data 16, 32 and 48-bit tapes.
Accordingly, the contents of 64 bit is filled by 16 clock pulses.
Tap output at every 16 bits can also be used for bus•logic.
The MN4517B/S are used in time-delay circuits, tentative memory circuits, etc.

P- 3



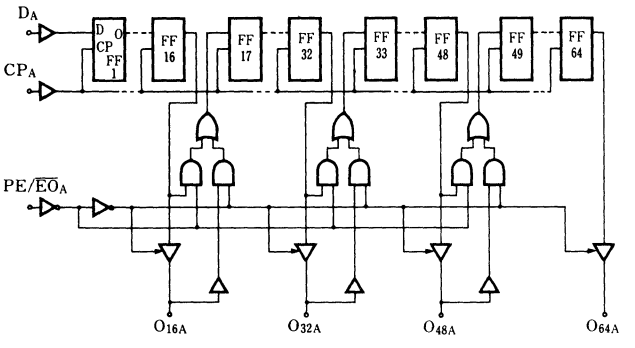
16-Pin • Plastic DIL Package

P- 4

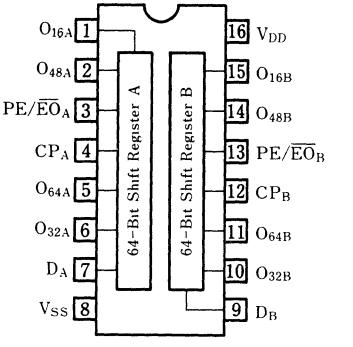


16-Pin • Panaflat Package (SO-16D)

■ Logic Diagram



Pin Configuration

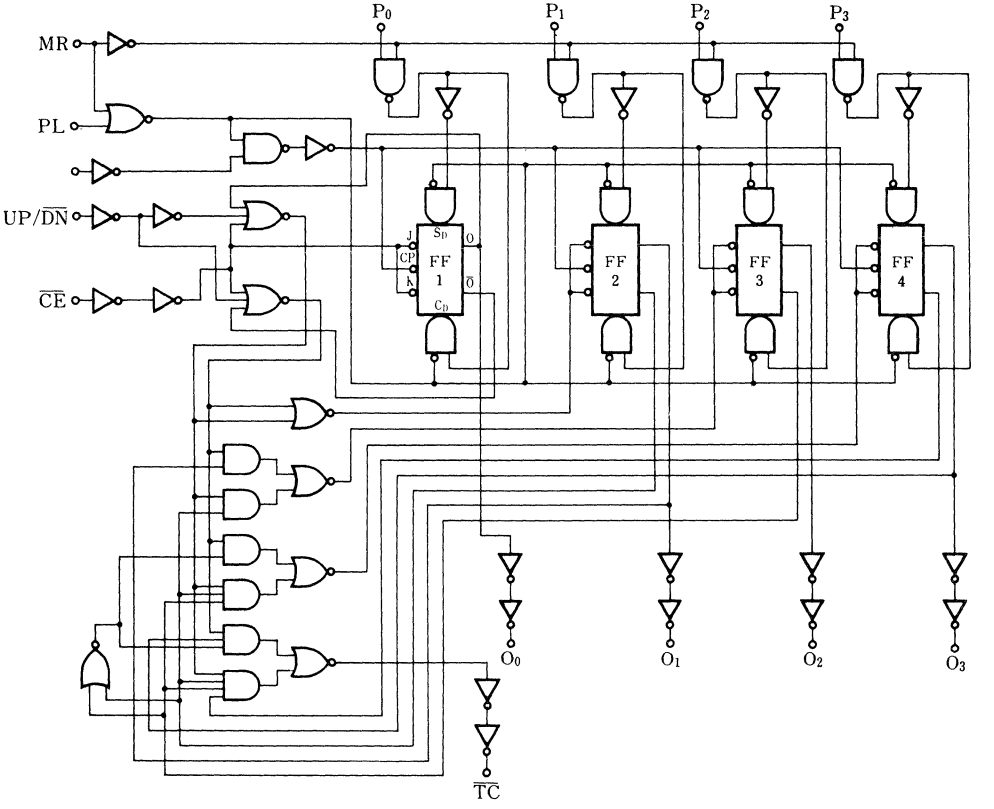


■ Truth Table

CP	PE/$\overline{EO}$	D	O_{16}	O_{32}	O_{48}	O_{64}
0	0	×	Contents of 16-bit display	Contents of 32-bit display	Contents of 48-bit display	Contents of 64-bit display
0	1	×	High impedance	High impedance	High impedance	High impedance
1	0	×	Contents of 16-bit display	Contents of 32-bit display	Contents of 48-bit display	Contents of 64-bit display
1	1	×	High impedance	High impedance	High impedance	High impedance
↑	0	Enter into first bit	Contents of 16-bit display	Contents of 32-bit display	Contents of 48-bit dispaly	Conternts of 64-bit display
↑	1	Enter into first bit	Data entering into 17th bit	Data entering into 33rd bit	Data entering into 49th bit	High impedance
↓	0	×	Contents of 16-bit display	Contents of 32-bit display	Contents of 48-bit display	Contents of 64-bit display
↓	1	×	High impedance	High impedance	High impedance	High impedance

Note) × : don't care

Logic Diagram



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Panasonic
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SALES OFFICES

HEADQUARTERS
Panasonic Industrial Company
Electronic Components Division
Division of Matsushita Electric
Corporation of America
One Panasonic Way
Secaucus, NJ 07094
(201) 348-5269

NORTHEASTERN REGION
Panasonic Industrial Company
Electronic Components Division
Division of Matsushita Electric
Corporation of America
333 Meadowlands Parkway
Secaucus, NJ 07094
(201) 348-5233

MIDWESTERN REGION
Panasonic Industrial Company
Electronic Components Division
Division of Matsushita Electric
Corporation of America
425 East Algonquin Road
Arlington Heights, IL 60005
(312) 981-4837

SOUTHERN REGION
Panasonic Industrial Company
Electronic Components Division
Division of Matsushita Electric
Corporation of America
4405 C International Boulevard
Suite 102
Norcross, GA 30093
(404) 923-9700

WESTERN REGION
Panasonic Industrial Company
Electronic Components Division
Division of Matsushita Electric
Corporation of America
6550 Katella Avenue
Cypress, CA 90630
(714) 895-7200

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