High Speed CMOS Logic MN74HC Series Panasonic

Panasonic

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Introduction to the CMOS Logic Family

The standard CMOS Logic Family has excellent characteristics such as low power dissipation, a wider range of operating power supply voltage, high noise margin, etc.; however, it has popularly been thought of as a medium speed element because the upper limit of the operating frequency is a few MHz at 5 V supply voltage compared to other standard logic families.

Matsushita Electronics Corporation has been conducting research and development of high-speed CMOS for application to high-speed electronic equipment as well, and has succeeded in the development of a new CMOS Logic family, the MN74HC Series, which has a pin configuration and operating speed in accordance with LS TTL.

Because of the standardized design of output drive characteristics, customers find system design easy by using the MN74HC Series, and the series will be expanded for applications to all electronic equipments for consumer and industry use.

For further applications of small and thin equipments, we have succeeded in supplying the Pana-flat package as the MN74HC00S Series. We are continually developing and introducing new products of high quality, high performance and high reliability, and we sincerely hope you will find this catalog for design engineers useful.

October, 1986

International Marketing Division
Semiconductor Group
Matsushiata Electronics Corporation

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Numerical and Functional Index

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Functions		Type No.				
Gates Buffers	NAND	MN74HC00,	MN74HC03,	MN74HC10,	MN74HC20,	MN74HC30,
		MN74HC133				
	NOR	MN74HC02,	MN74HC27,	MN74HC4002,	MN74HC4078	
	AND	MN74HC08,	MN74HC11,	MN74HC21		
	OR	MN74HC32,	MN74HC4075			
	Buffer	MN74HC125,	MN74HC126,	MN74HC241,	MN74HC244,	MN74HC365,
		MN74HC367,	MN74HC540,	MN74HC541,	MN74HC4050,	MN74HC4306
	Inverter	MN74HC04,	MN74HCU04,	MN74HCT04,	MN74HC240,	MN74HC366,
		MN74HC368,	MN74HC4049,	MN74HC4305		
	Exclusive-OR	MN74HC86,	MN74HC386			
	Exclusive-NOR	MN74HC266				
	Complex-Gate	MN74HC51				
	Schmidt Trigger	MN74HC14,	MN74HC132			
Transceivers		MN74HC242,	MN47HC243,	MN74HC245,	MN74HC640,	MN74HC643
Flip-Flops		MN74HC73,	MN74HC74,	MN74HC76,	MN74HC107,	MN74HC109,
		MN74HC112,	MN74HC173,	MN74HC174,	MN74HC175,	MN74HC273,
		MN74HC374,	MN74HC377,	MN74HCT377,	MN74HC534,	MN74HC564,
		MN74HC574,	MN74HC4303,	MN74HC4304		
Latches		MN74HC75,	MN74HC77,	MN74HC373,	MN74HC375,	MN74HC533,
		MN74HC563,	MN74HC573,	MN74HC4301,	MN74HC4302	
Decoders		MN74HC42,	MN74HC137,	MN74HC138,	MN74HC139,	MN74HC155,
		MN74HC237,	MN74HC238,	MN74HCT238		
Shift-Registers		MN74HC164,	MN74HC165,	MN74HC166,	MN74HC194,	MN74HC195,
		MN74HC4015,	MN74HC40104	MN74HCT40104		
Counters	Binary	MN74HC161,	MN74HC163,	MN74HC393,	MN74HC4020,	MN74HC4024,
		MN74HC4040,	MN74HC4060,	MN74HCT4060,	MN74HC4520	
	Decade	MN74HC160,	MN74HC162,	MN74HC390		
Multiplexers	Analog	MN74HC4051,	MN74HC4052,	MN74HC4053,	MN74HC4066	
	Digital	MN74HC151,	MN74HC153,	MN74HC157,	MN74HC158,	MN74HC251,
		MN74HC253,	MN74HC257,	MN74HC258,	MN74HC352,	MN74HC353
Encoders		MN74HC147,	MN74HC148			
Multivibrator		MN74HC221				
Comparator		MN74HC688				
Others		MN74HC183,	MN74HC280,	MN74HCT280		

Descriptions

Descriptions

Descriptions

1. Outline of MN74HC Series

The MN74HC Series is designed to be used in systems where low-power dissipation, a wider range of supply voltage and high noise margins are required, featuring basic logical functions and complete compatibility with LS TTL in pin configuration and operating speed.
Easy system design is possible because of the standardized design of output drive characteristics. The MN74HC Series consists of the MN74HCOO Series standard DIL package, and the MN74HCOOS Series, which has enabled smaller and thinner electronic equipment by adopting a small Pana-flat package.

*** Features of the MN74HC Series**

(1) High-speed operation (V_{CC} 5V)
Typical gate propagation delay times:
t_{pd1} = 6 ns typ. (C_L = 15 pF)
t_{pd2} = 8 ns typ. (C_L = 50 pF)
Typical flip-flop operating frequency:
f_{max} = 60MHz typ. (C_L = 50 pF)
(2) Wider range of operating power supply voltage = 1.4 ~ 6 V
(3) Low power dissipation:
1.0 mW/Gate (V_{CC}=5 V, f_i=1MHz, C_L=15 pF)
(4) Wider operating temperature range: –40 ~ +85°C
(5) High noise margin
(6) Direct drive of LS TTL 10-input
(7) Same function and same pin configuration as LS TTL 54/74 Series. Some have the same function and pin configuration as the CMOS 4000 Series.
(8) Built-in static electricity protection circuitry

2. Comparison with Other Logic Families

Comparison between MN74HCOO (Quad 2-Input NAND Gates) and other logic families with same functions.

Table 1 2-Input NAND Gate Comparison Chart

Parameter	H CMOS	LS TTL	TTL	B-Type CMOS	Remarks
Power Supply Voltage	1.4~6V	5±5%V	5±5%V	3~15V	
Power Dissipation (typ.)	1mW/Gate	2mW/Gate	10mW/Gate	1mW/Gate	V_{CC}=5V, C_L=15pF f_i=1MHz
Quiescent Power (max.)	100μW/Gate	22mW/Gate	110mW/Gate	40μW/Gate	V_{CC}=5V, V_I=GND
Propagation Delay Time (typ.)	6ns	10ns	10ns	50~100ns	V_{CC}=5V, C_L=15pF
Output Current (I_{OL}) (min.)	2.5mA	8mA	16mA	0.36mA	V_{CC}=5V
Noise Margin	1V	0.4V	0.4V	1V	V_{CC}=5V
Operating Temperature	−40~+85℃	0~+70℃	0~+70℃	−40~+85℃	

3. Ordering and Numbering System

The following indications information is needed for orders.

(Type Number)

MN 74 HC XX(X) S

- S → S: Pana-flat package (small package) / Empty: Standard plastic DIL package
- XX(X) → Device No. / XX(X): Same function and pin configuration as 74LS TTL / 4XXX: Same function and pin configuration as CMOS 4000.
- HC → High-speed COMS
- 74 → 74HCOO Series
- MN → MOS Integrated Circuit manufactured by Matsushita Electronics Corporation

4. Basic Circuitry and Construction of MN74HC MOS

The basic explanation gives, as an example, the inverter of the MN74HC Series.

As shown in Figure 1, the 74HC MOS inverter consists of a p-channel enhancement type MS transistor (P_1) and an n-channel enhancement type MOS transistor (N_1). Input is made by commonly connecting each gate, and output is made by commonly connecting each drain.

V_{CC} (+), is the source of the p-channel MOS transistor, and GND(–) is the source of the n-channel MOS transistor. In this figure, the voltage (V_O) of the output (O) is considered when the voltage (V_I) of input (I) changes from V_{CC} to GND

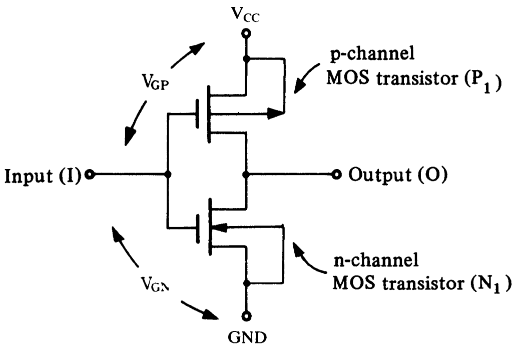


Fig. 1 74HC MOS Inverter

4.1 When input (1) is GND level

V_{GP} (voltage between gate and source) of P_1 is $-(V_{CC}-GND)$,and P_1 switches ON because negative deep bias is applied to the gate. V_{GN} (voltage between gate and source) of N_1 is O, and N_1 becomes OFF. Output (O) becomes partial pressured level by the resistor ratio P_1 and N_1 but output voltage (V_O) becomes approximately V_{CC} because ON and OFF resistance become, respectively, tens of ohms and several hundreds of M ohms. In this instance, no current flows from V_{CC} to GND

4.2 When the input (1) is an intermediate level between V_{CC} and GND

P_1 and N_1 become ON and output (O) becomes intermediate level partially pressured by P_1 ON and N_1 ON resistors. In this instance, output voltage (V_O) becomes approximately V_{CC} and GND when the input voltage (V_I) is near the level of GND and V_{CC}, respectively.

Current flows from V_{CC} to GND.

4.3 When the input (1) is V_{CC} level

When V_{GP} of P_1 and V_{GP} of N_1 are zero and ($V_{CC}-$GND), P_1 and N_1 become OFF and ON, respectively. Accordingly, the operation becomes completely the reverse of the order in 4.1, the voltage (V_O) of output (O) becomes approximately GND level, and no current flows from V_{CC} to GND. The quadrature axis shows an input voltage and the axis of ordinates shows an output voltage in Fig. 2. The dotted line of the axis of ordinates shows current flowing from V_{CC} to GND; current flows (I_{CC}) only when the inverter changes.

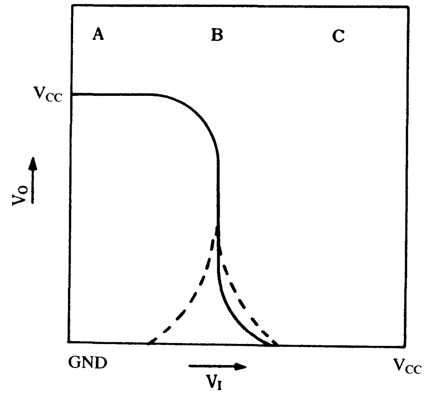


Fig. 2 74HC MOS Inverter Input/output Voltage Characteristics

A sectional view of the 74HC MOS inverter is shown in Fig. 3. There should be perfect separation between the p-channel and n-channel MOS transistors in order for the 74HC MOS inverter to be used on the signal silicon substrate; for this purpose, a pn conjunction is used.

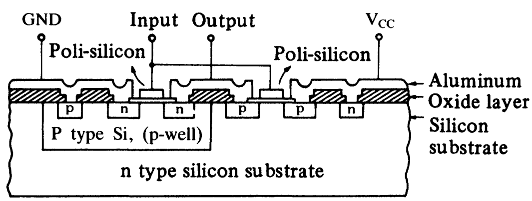
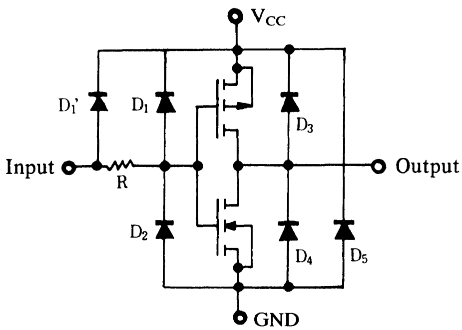


Fig. 3 Sectional view of the 74HC MOS inverter

In this figure, the p-channel MOS transistor is grown on the n type silicon substrate and the n-channel MOS transistor is grown on the p-well in the substrate. When power is switched on, the substrate and p-well become in a condition of reverse bias of (V_{CC}−GND), because the n-type substrate and p-well are connected to V_{CC} and GND respectively. Therefore, the p- and n-channel transistors can operate independently of each other. A parastic diode is inserted into the 74HC MOS circuit, as shown in Fig. 4, and, when the rating at each terminal is exceeded, excessive forward current may flow to these diodes, and the IC may be damaged. For this reason, absolute maximum ratings must be maintained.



R : Input protection diode
D_1 :
D_1' : Input protection diode
D_2 :
D_3 : p-channel transistor
Parasitic diode by drain growth
D_4 : n-channel transistor
Parasitic diode by drain growth
D_5 : Parasitic diode by p-well growth

Fig. 4. 74HC MOS inverter equivalent circuit considering parasitic element

As shown in Fig. 4, input protection diodes such as D_1, D_1' and D_2 are used for the protection of the CMOS input gate from static electricity. These diodes are used in all products of the MN74HCOO Series (although only D_2 is used in the MN74HC4049/S and MN74HC4050/S).

5. Handling of the MOS Device

Circuits for protection against static electricity are used in all MEC MOS ICs; however, the IC will be damaged by accidental excessively high voltage.
Accordingly, the following cautions should be followed in order to handle the device safely.

(1) During use

Be sure to ground the person (by a resistor of 1MΩ) handling the ICs and also any charged materials on the work discharged.

(2) For storage and transport

It is necessary to use an MEC – specified container and/or conductive material. These containers are used to either short or insulate ICs.

(3) Test and Handling

When testing and moving an IC from one carrier to another, be sure to handle it on a conductive board (metal table, etc.) Also be sure to ground the person to the conduction table (by a metal chain or lead wire). Testing and handling equipment should also be grounded to the metal table. A signal should not be input when the devices is in the OFF mode.

(4) Securing

It is necessary to secure the MOS IC after all parts have been secured, and it is best to ground the IC, the metal portion of the printed-circuit board, the jigs, tools and workers in order to prevent a failure in the process line.
If the printed-circuit board can't be grounded, the worker should first touch the printed-circuit board before he touches the MOS IC to the printed-circuit board.

(5) Soldering

The soldering iron, even a low-voltage one, and the soldering bath should also be grounded.

(6) Static electricity

Workers should wear clothes which do not attract static elecricity (avoid using work clothing made of nylon or other synthetic fibers). Care should be taken even after the MOS IC is secured to the printed-circuit board. Conductive clips or tape should be connected to the terminals of the circuit board in order to protect from static electricity through the board, because the board is only an extension of the lead wire of the device secured to the board until the assembled board is installed in the system and the appropriate voltage is applied.

6. Symbols and Terms

● Current

+ is current flowing into an element and – is current flowing out from the element.

Symbol	Term	Description
I_I	Input current	Sink current at the specified input voltage and V_{CC}
I_{OH}	Output HIGH current	Sink driving current at the specified output HIGH voltage and V_{CC}
I_{OL}	Output LOW current	Sink driving current at specified output LOW voltage and V_{CC}
I_{CC}	Quiescent power supply current	Sink current into the V_{CC} terminal at the specified input voltage V_{CC}
I_{OZ}	Output OFF current	Current which flows into or out from an off-state tri-state output when the output is connected to V_{CC} or GND
I_{IL}	Input LOW current	Current which flows into an element at the specified input LOW voltage and V_{CC}
I_{IH}	Input HIGH current	Current which flows into an element at the specified input HIGH voltage and V_{CC}
I_{CCL}	Quiescent LOW power supply current	Current which flows into the V_{CC} terminal at the specified input LOW voltage and V_{CC} against all inputs
I_{CCH}	Quiescent HIGH power supply current	Current which flows into the V_{CC} terminal at the specified input HIGH voltage and V_{CC} against all terminals

● Voltage

GND is the lowest voltage which is applied to an element; all voltages are relative in value to GND.

Symbol	Term	Description
V_{CC}	Power supply voltage	Highest positive (+) voltage
GND	Power supply voltage	Highest negative (–) voltage of a single power supply; reference voltage level to others; GND
V_{EE}	Power supply voltage	One of the negative power supply voltages and highest negative power supply voltage which is a reference voltage to others
V_{IH}	Input HIGH voltage	Input voltage range showing logical HIGH of the system
V_{IL}	Input LOW voltage	Input voltage range showing logical LOW of the system
V_{OH}	Output HIGH voltage	Voltage range of the output terminal at the specified output load and power supply voltage
V_{OL}	Output LOW voltage	Voltage range of the output terminal at the specified output load and power supply voltage

● Analog symbol

Symbol	Term	Description
R_{ON}	ON resistance	Effective ON resistance of analog-transmission gate at the specified input voltage, output load and V_{CC}
ΔR_{ON}	Δ ON resistance	Difference of effective ON resistance between the two transmission gates of the analog-switch at the specified input voltage, output load and V_{CC}

Common Specifications

Common Specifications

Common Specifications

High-speed CMOS logic IC MN74HCOO Series operates in the range of V_{CC} = + 1.4 ~ 6.0 V(GND=0V), and each specification is guaranteed at V_{CC}=2.0V, 4.5V and 6.0V.
The high-speed CMOS logic IC operates in the wider range; therefore, it is not so critical relative to power supply regulation as the conventional logic IC (TTL, LS TTL).
It operates at V_{CC} = +1.4 V (min.) if the noise margin and interfacing problem with other equipment are not considered.

In addition, it operates at V_{CC} = +6.0 V (max.) if power dissipation and interface are not considered. Unused terminals should be connected to V_{CC}, GND or other input terminals. Countermeasures against static electricity are taken for the input/output terminals of the high-speed CMOS logic IC; however, we recommend careful handling even so.
Individual specifications are described in the individual data sheets; common specifications are summarized as follows.

1. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

<table>
<tr><th colspan="3">Parameter</th><th>Symbol</th><th>Rating</th><th>Unit</th></tr>
<tr><td colspan="3">Supply voltage</td><td>V_{CC}</td><td>−0.5~+7.0</td><td>V</td></tr>
<tr><td colspan="3">Input/output voltage</td><td>V_I, V_O</td><td>−0.5~V_{CC}+0.5</td><td>V</td></tr>
<tr><td colspan="3">Input protection diode current</td><td>I_{IK}</td><td>±20</td><td>mA</td></tr>
<tr><td colspan="3">Output parasitic diode current</td><td>I_{OK}</td><td>±20</td><td>mA</td></tr>
<tr><td colspan="3">Output current</td><td>I_O</td><td>±25 (STD), ±35 (Bus driver)</td><td>mA</td></tr>
<tr><td colspan="3">Supply current</td><td>I_{CC}, I_{GND}</td><td>±50 (STD), ±70 (Bus driver)</td><td>mA</td></tr>
<tr><td colspan="3">Storage temperature range</td><td>Tstg</td><td>−65~+150</td><td>°C</td></tr>
<tr><td rowspan="4">Power dissipation</td><td rowspan="2">MN74HCXX</td><td>Ta=−40~+60°C</td><td rowspan="2">P_D</td><td>400</td><td rowspan="2">mW</td></tr>
<tr><td>Ta=+60~+85°C</td><td>Decrease to 200mW at the rate of 8mW/°C</td></tr>
<tr><td rowspan="2">MN74HCXXS</td><td>Ta=−40~+60°C</td><td rowspan="2">P_D</td><td>275</td><td rowspan="2">mW</td></tr>
<tr><td>Ta=+60~+85°C</td><td>Decrease to 200mW at the rate of 3.8mW/°C</td></tr>
</table>

■ Operating Conditions

<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th colspan="3">Rating</th><th rowspan="2">Unit</th></tr>
<tr><th>HC</th><th>HCU</th><th>HCT</th></tr>
<tr><td>Operating supply voltage</td><td>V_{CC}</td><td>1.4~6.0</td><td>1.4~6.0</td><td>4.5~5.5</td><td>V</td></tr>
<tr><td>Input/output voltage</td><td>V_I, V_O</td><td>0~V_{CC}</td><td>0~V_{CC}</td><td>0~V_{CC}</td><td>V</td></tr>
<tr><td>Operating temperature range</td><td>Ta</td><td>−40~+85</td><td>−40~+85</td><td>−40~+85</td><td>°C</td></tr>
<tr><td>Input rise and fall time</td><td>t_r, t_f</td><td>(V_{CC})
2.0V 0~1000
4.5V 0~500
6.0V 0~400</td><td>(V_{CC})
2.0V 0~1000
4.5V 0~500
6.0V 0~400</td><td>0~500</td><td>ns</td></tr>
</table>

2. Main Characteristic Figures

Necessary main characteristics are shown by the example of MN74HCOO (Quad 2-Input NAND Gates)

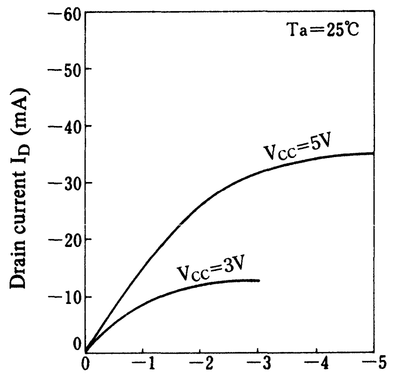


Fig. 5 I_D-V_{DS} characteristics (p-channel)

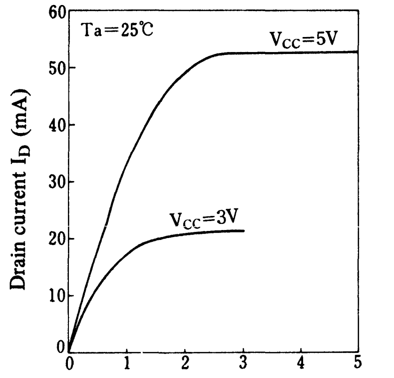


Fig. 6 I_D-V_{DS} characteristics (n-channel)

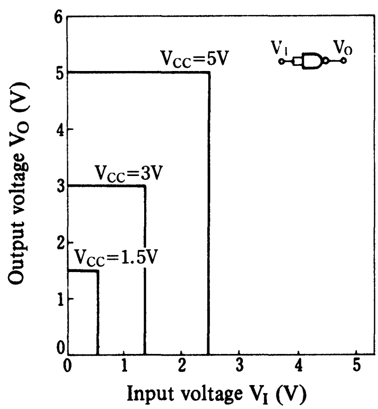


Fig. 7 Propagation characteristics (with buffer)

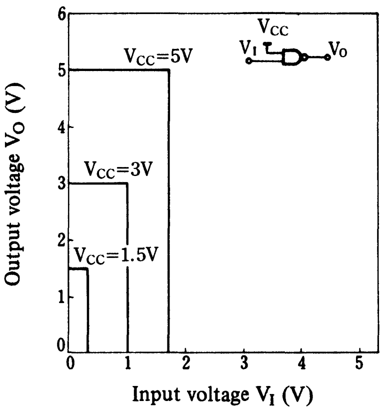


Fig. 8 Propagation characteristics (with buffer)

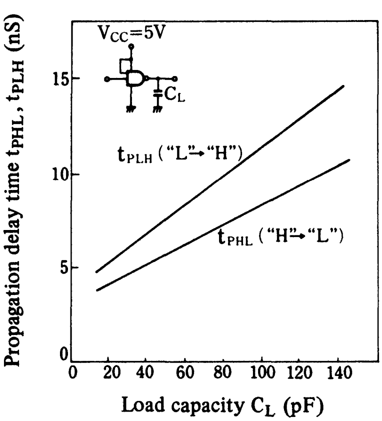


Fig. 9 Load capacity vs. propagation delay characteristics

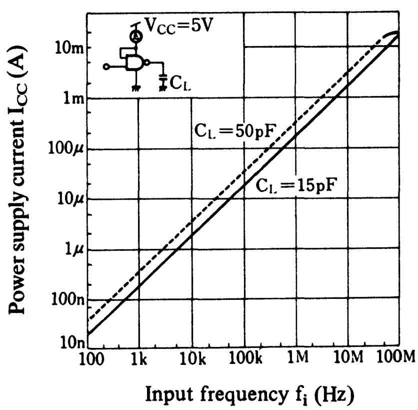


Fig. 10 Power dissipation vs. input frequency characteristics

3. DC characteristics (GND=0V)

Table 3 Characteristics

Parameter		Type	Symbol	V_{CC} (V)	Test Conditions V_I	I_O STD	I_O BUS	I_O Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage		HC	V_{IH}	2.0					1.5			1.5		V
				4.5					3.15			3.15		V
				6.0					4.2			4.2		V
		HCT		4.5 ~ 5.5					2.0			2.0		V
Input LOW voltage		HC	V_{IL}	2.0							0.3		0.3	V
				4.5							0.9		0.9	V
				6.0							1.2		1.2	V
		HCT		4.5 ~ 5.5							0.8		0.8	V
Output HIGH voltage		HC	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	−20.0	μA	1.9	2.0		1.9		V
				4.5		−20.0	−20.0	μA	4.4	4.5		4.4		V
				6.0		−20.0	−20.0	μA	5.9	6.0		5.9		V
				4.5		−4.0	−6.0	mA	3.86			3.76		V
				6.0		−5.2	−7.8	mA	5.36			5.26		V
		HCT		4.5	V_{IH} or V_{IL}	−20.0	−20.0	μA	4.4	4.5		4.4		V
				4.5		−4.0	−6.0	mA	3.86			3.76		V
Output LOW voltage		HC	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	20.0	μA		0.0	0.1		0.1	V
				4.5		20.0	20.0	μA		0.0	0.1		0.1	V
				6.0		20.0	20.0	μA		0.0	0.1		0.1	V
				4.5		4.0	6.0	mA			0.32		0.37	V
				6.0		5.2	7.8	mA			0.32		0.37	V
		HCT		4.5	V_{IH} or V_{IL}	20.0	20.0	μA		0.0	0.1		0.1	V
				4.5		4.0	6.0	mA			0.32		0.37	V
Input current		HC	I_I	6.0	$V_I = V_{CC}$ or GND						±0.1		±1.0	μA
		HCT		5.5							±0.1		±1.0	μA
Analog switch OFF current		HC	I_S	6.0	$V_I = V_{IH}$ or V_{IL}						±0.1		±1.0	μA
		HCT		5.5	$\lvert V_S \rvert = V_{CC}$ or GND						±0.1		±1.0	μA
3-state output Off state current		HC	I_{OZ}	6.0	$V_I = V_{IH}$ or V_{IL}						±0.5		±5.0	μA
		HCT		5.5	$V_O = V_{CC}$ or GND						±0.5		±5.0	μA
Quiescent supply current	SSI	HC	I_{CC}	6.0	$V_I = V_{CC}$ or GND, $I_O = 0$						2.0		20.0	μA
		HCT		5.5							2.0		20.0	μA
	FF	HC		6.0							4.0		40.0	μA
		HCT		5.5							4.0		40.0	μA
	MSI	HC		6.0							8.0		80.0	μA
		HCT		5.5							8.0		80.0	μA

4. AC Characteristics

Table 4 AC Switching · Parameter

Symbol	Description	Symbol	Description
f_i	Input frequency	t_W	Pulse width
f_o	Output frequency	t_{hold}	Hold time
$f_{max.}$	Maximum clock frequency	t_{su}	Set-up time
t_r, t_f	Clock input rise & fall time	t_{PHZ}	3-state output disable time H→Z
t_{PLH}	Propagation time (propagation delay time) L→H	t_{PLZ}	3-state output disable time L→Z
t_{PHL}	Propagation time (propagation delay time) H→L	t_{PZH}	3-state output enable time Z→H
t_{TLH}	Rise time L→H	t_{PZL}	3-state output enable time Z→L
t_{THL}	Fall time H→L	t_R	Recovery time

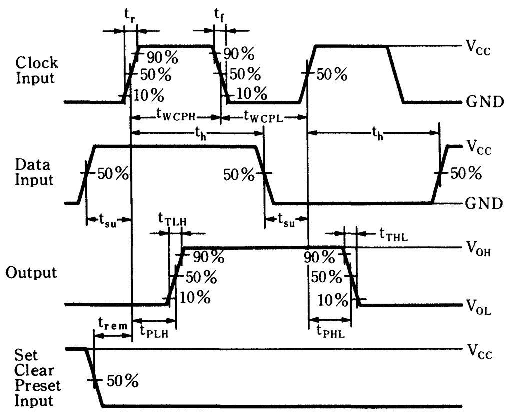


Fig. 11 Set-up time, hold time, propagation time, recovery time, rise time fall time for MN74HC

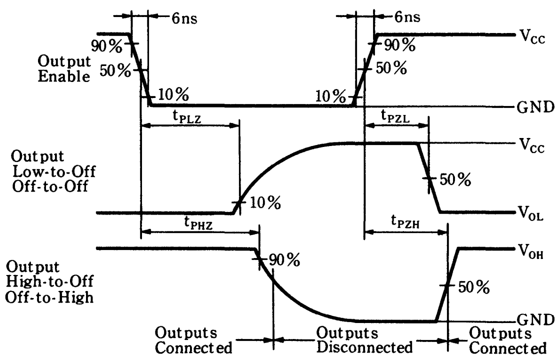


Fig. 12 3-State output propagation time for MN74HC

● **Clock rise, fall time (t_r, t_f)**

The upper limit of t_r and t_f changes depending on the device and power supply voltage.
Unless otherwise specified in the individual data sheet, clock input rise and fall times are less than 6 ns.

● **Output rise, fall time (t_{TLH} & t_{THL})**

Table 5 t_{TLH} and t_{THL} Characteristics Table (GND=0V, Ta=25°C, t_r, t_f≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Min.	Typ.	Max.	Unit
Output rise time	t_{TLH}	2.0		25	75	ns
		4.5		8	15	
		6.0		7	13	
Output fall time	t_{THL}	2.0		20	75	ns
		4.5		7	15	
		6.0		6	13	

5. External Diagrams of Package

Unit:mm

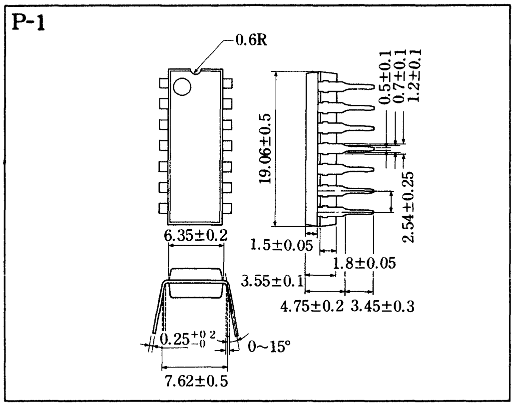


Fig. 13 Plastic DIL-14 pin

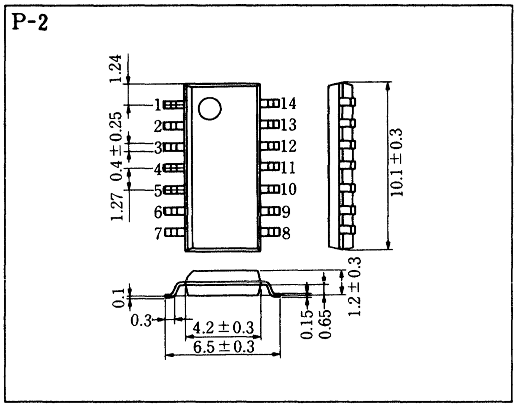


Fig. 14 14-pin Panaflat package (SO-14D)

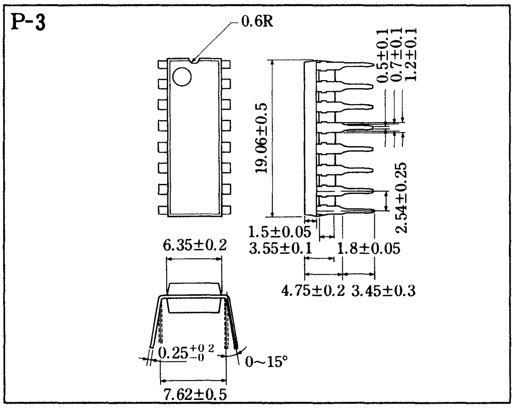


Fig. 15 Plastic DIL-16 pin

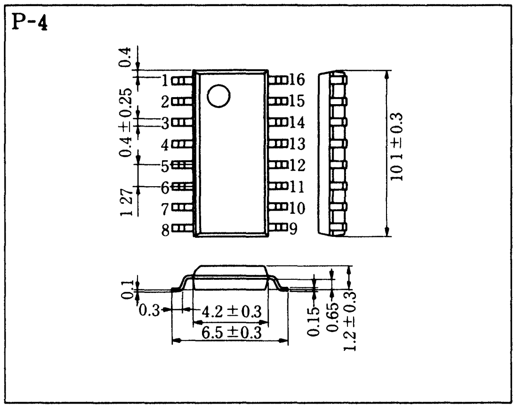


Fig. 16 16-pin Panaflat package (SO-16D)

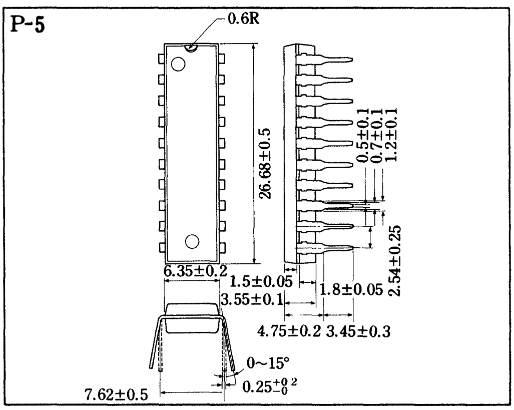


Fig. 17 Plastic DIL-20 pin

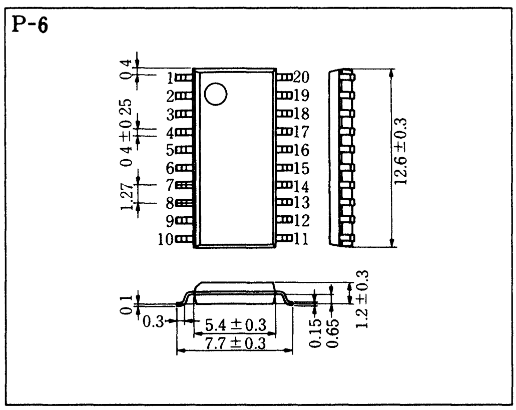


Fig. 18 20-pin Panaflat package (SO-20D)

Individual Specifications

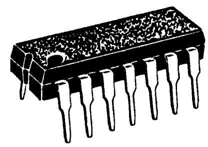
MN74HC00/MN74HC00S

Quad 2-Input NAND Gates

■ Description

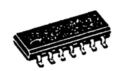
MN74HC00/MN74HC00S contain four 2-input positive isolation NAND gate circuits.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for the protection of the input/output against damage by static electricity.
Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



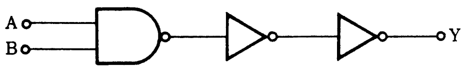
14-pin plastic DIL package

P-2

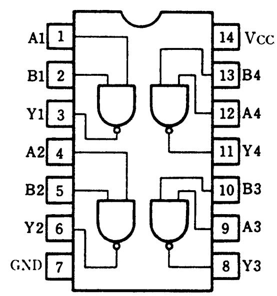


14-pin Panaflat package (SO-14D)

■ Logic diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input/output voltage			V_I, V_O	−0.5~V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65~+150	℃
Power dissipation	MN74HC00	Ta=−40~+60℃	P_D	400	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC00S	Ta=−40~+60℃	P_D	275	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25℃			Ta=−40～+85℃		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40～+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

MN74HC02/MN74HC02S

Quad 2-Input NOR Gates

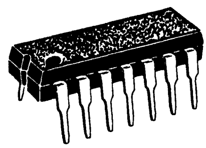
■ Description

MN74HC02/MN74HC02S contain four 2-input isolation NOR gate circuits.

Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

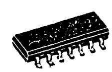
Resistors and diodes are provided in V_{CC} and GND for the protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



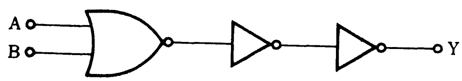
14-pin plastic DIL package

P-2

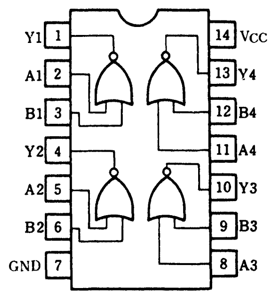


14-pin Panaflat package (SO-14D)

■ Logic diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input/output voltage			V_I, V_O	−0.5~V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65~+150	℃
Power dissipation	MN74HC02	Ta=−40~+60℃	P_D	400	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC02S	Ta=−40~+60℃	P_D	275	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

Panasonic

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

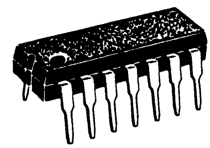
MN74HC03/MN74HC03S

Quad 2-Input NAND Gates (Open Drain)

■ Description

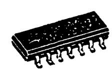
MN74HC03/MN74HC03S contain four 2-input open drain positive isolation NAND gate circuits. Input transfer characteristics have been improved by applying a buffer to the gate output, and flutuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND for the protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P- 1



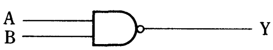
14-pin plastic DIL package

P- 2

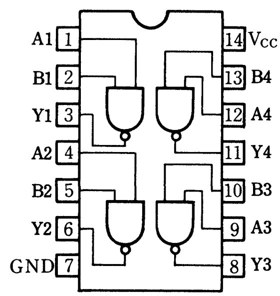


14-pin Panaflat package (SO-14D)

■ Logic Diagram (1 gate)



Pin Configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	°C
Power dissipation	MN74HC03	Ta=−40～+60°C	P_D	400	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC03S	Ta=−40～+60°C	P_D	275	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input voltage	V_I		0~V_{CC}	V
Output voltage	V_O		*) 0~8.0	V
Operating temperature range	T_A		−40~+85	°C
Input rise and fall time	t_r, t_f	V_{CC}=2.0V	0~1000	ns
		V_{CC}=4.5V	0~500	ns
		V_{CC}=6.0V	0~400	ns

*) Even if output voltage V_O is less than the absolute maximum rating, Output current I_O might happen to be oven the absolute maximum rating.
In this case, pull-up resistance R(≧390Ω), which is within the absolute maximum rating, is needed to connect with the output pin.

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25°C min.	typ.	max.	Ta=−40~+85°C min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		V
		6.0				4.2			4.2		V
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	V
		6.0						1.2		1.2	V
Output Low voltage	V_{OL}	2.0	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	V
		6.0		20.0	μA		0.0	1.0		0.1	V
		4.5		4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Ouiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20	μA
Output current	I_{OZ}	6.0	V_{IH}, V_{IL}, V_O=V_{CC} or GND					±0.5		±5	μA

■ AC Characteristics (GND=0V, Input Transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25°C min.	typ.	max.	Ta=−40~+85°C min.	max.	Unit
Output fall time	t_{THL}	2.0			18	75		95	
		4.5			6	15		19	ns
		6.0			5	13		16	ns
Propagation time (L→Z)	t_{PLZ}	2.0			13	125		155	
		4.5			10	25		31	ns
		6.0			9	21		26	ns
Propagation time (Z←L)	t_{PZL}	2.0			14	75		95	
		4.5			7	15		19	ns
		6.0			6	13		16	

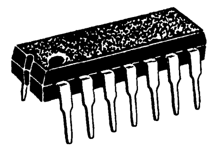
MN74HC04/MN74HC04S

Hex Inverters

■ Description

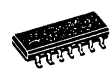
MN74HC04/MN74HC04S contain six inverter circuits.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity.
Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



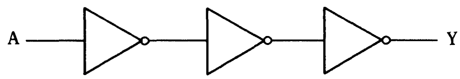
14-pin plastic DIL package

P-2

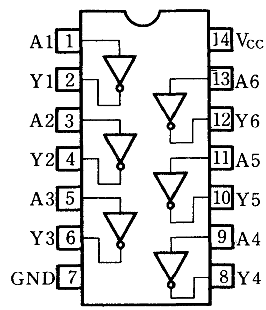


14-pin Panaflat package (SO-14D)

■ Logic diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5〜+7.0	V
Input/output voltage			V_I, V_O	−0.5〜V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65〜+150	℃
Power dissipation	MN74HC04	Ta=−40〜+60℃	P_D	400	mW
		Ta=+60〜+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC04S	Ta=−40〜+60℃	P_D	275	mW
		Ta=+60〜+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Propagation time (L→H)	t_{PLH}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Propagation time (H→L)	t_{PHL}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	

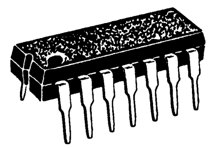
MN74HCT04/MN74HCT04S

Hex Inverters(TTL Input)

■ Description

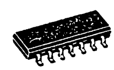
MN74HCT04/MN74HCT04S contain six inverter circuits. All inputs are compatible with TTL logic level: 0.8V or less is logic "0" input and 2.0V or more is logic "1".
Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity.
Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



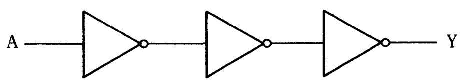
14-pin plastic DIL package

P-2

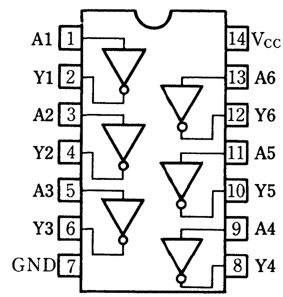


14-pin Panaflat package (SO-14D)

■ Logic Diagram



Pin Configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input/output voltage			V_I, V_O	−0.5~V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65~+150	°C
Power dissipation	MN74HCT04	Ta=−40~±60°C	P_D	400	mW
		Ta=+60~+85°C		Decrease to 200m Watt the rate of 8mW/°C	
	MN74HCT04S	Ta=−40~+60°C	P_D	275	mW
		Ta=+60~+85°C		Decrease to 200m Watt the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operation supply voltage	V_{CC}		4.5~5.5	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	°C
Input rise and fall time	t_r, t_f	4.5	0~500	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25°C			Ta=−40~+85°C		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	4.5				1.5			1.5		V
		≀				2.0			2.0		V
		5.5				4.2			4.2		
Input LOW voltage	V_{IL}	4.5						0.3		0.3	
		≀						0.8		0.8	V
		5.5						1.2		1.2	
Output HIGH voltage	V_{OH}	4.5	V_{IL}	−20.0	μA	4.4	4.5		4.4		V
		4.5		−4.0	mA	3.86			3.76		
Output LOW voltage	V_{OL}	4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		4.5		4.0	mA			0.32		0.37	
Input current	I_I	5.5	V_I=V_{CC}or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	5.5	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transistion time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25°C			Ta=−40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	4.5			4	15		19	ns
Output fall time	t_{THL}	4.5			4	15		19	ns
Propagation time (L←H)	t_{PLH}	4.5			7	20		25	ns
Propagation time (H←L)	t_{PHL}	4.5			6	20		25	ns

MN74HCU04/MN74HCU04S

Hex Inverters (Unbuffered)

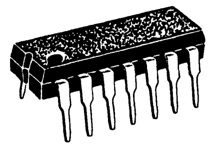
■ Description

MN74HC04/MN74HC04S contain six inverter circuits without buffer.

Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven.

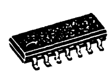
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



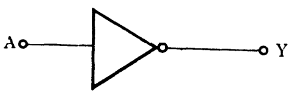
14-pin plastic DIL package

P-2

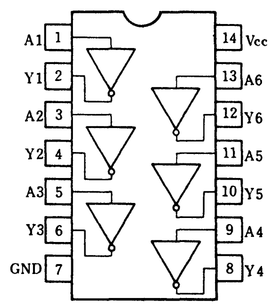


14-pin Panaflat package (SO-14D)

■ Logic diagram (1 gate)



Pin Configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}.I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HCU04	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HCU04S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	°C
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.7			1.7		V
		4.5				3.6			3.6		
		6.0				4.8			4.8		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.8		0.8	
		6.0						1.1		1.1	
Output HIGH voltage	V_{OH}	2.0	V_{IL}	−20.0	μA	1.8	2.0		1.8		V
		4.5		−20.0	μA	4.0	4.5		4.0		
		6.0		−20.0	μA	5.5	6.0		5.5		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH}	20.0	μA		0.0	0.2		0.2	V
		4.5		20.0	μA		0.0	0.5		0.5	
		6.0		20.0	μA		0.0	0.5		0.5	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I= V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND,I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			20	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
Propagation time (H→L)	t_{PHL}	2.0			20	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	

MN74HC08/MN74HC08S

Quad 2-Input AND Gates

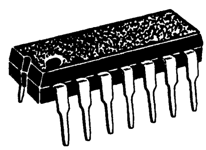
■ Description

MN74HC08/MN74HC08S contain four 2-input positive isolation AND gate circuits.

Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

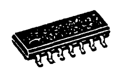
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



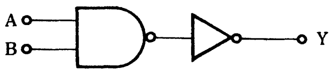
14-pin plastic DIL package

P-2

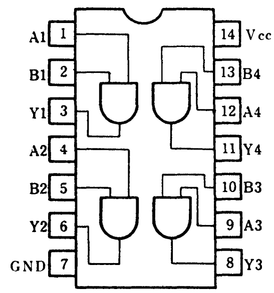


14-pin Panaflat package (SO-14D)

■ Logic diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC08	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC08S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	Test Conditions I_O	I_O Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

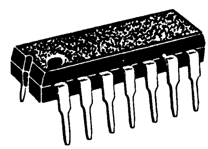
MN74HC10/MN74HC10S

Triple 3-Input NAND Gates

■ Description

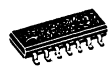
MN74HC10/MN74HC10S contain three 3-input positive isolation AND gate circuits.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



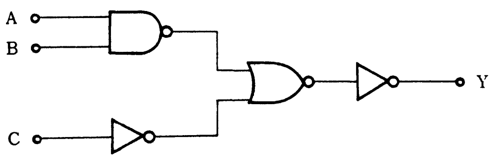
14-pin plastic DIL package

P-2

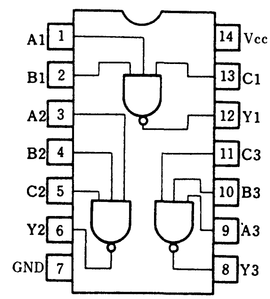


14-pin Panaflat package (SO-14D)

■ Logic diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5〜+7.0	V
Input/output voltage			V_I, V_O	−0.5〜V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65〜+150	℃
Power dissipation	MN74HC10	Ta=−40〜+60℃	P_D	400	mW
		Ta=+60〜+85℃		Decrease to 200mW at the rate of 8mW/℃	
	MN74HC10S	Ta=−40〜+60℃	P_D	275	mW
		Ta=+60〜+85℃		Decrease to 200mW at the rate of 3.8mW/℃	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	I_O Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

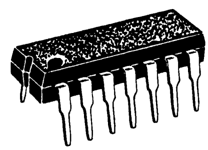
MN74HC11/MN74HC11S

Triple 3-Input AND Gates

■ Description

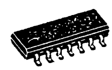
MN74HC11/MN74HC11S contain three 3-input positive isolation AND gate circuits.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



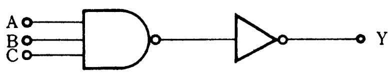
14-pin plastic DIL package

P-2

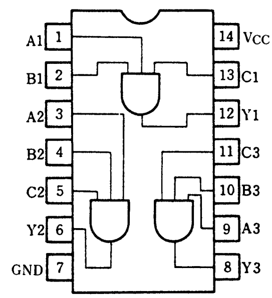


14-pin Panaflat package (SO-14D)

■ Logic Diagram



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	± 20	mA
Output parasitic diode current			I_{OK}	± 20	mA
Output current			I_O	± 25	mA
Supply current			I_{CC}, I_{GND}	± 50	mA
Storage temperature range			Tstg	$-65 \sim +150$	℃
Power dissipation	MN74HC11	Ta=$-40 \sim +60$℃	P_D	400	mW
		Ta=$+60 \sim +85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC11S	Ta=$-40 \sim +60$℃	P_D	275	mW
		Ta=$+60 \sim +85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	Test Conditions I_O	I_O Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

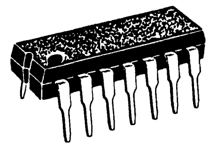
MN74HC14/MN74HC14S

Hex Inverting Schmitt Triggers

■ Description

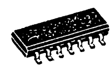
MN74HC14/MN74HC14S contains six inverter circuits with Schmitt triggers at all input terminals.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Because the circuit threshold voltage differs (V_{IH} V_{IL}) when the input waveform rises and falls, wider applications are possible for the line receiver, waveform shaping and multi-vibrator in addition to the normal inverter.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

P-1



14-pin plastic DIL package

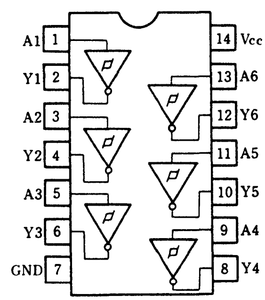
P-2



14-pin Panaflat package (SO-14D)

■ Logic Diagram (1 Gate)

Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC14	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC14S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	I_O Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA
Input threshold voltage	V_T^+	2.0				0.7	1.10	1.50	0.7	1.5	V
		4.5				1.55	2.46	3.15	1.55	3.15	
		6.0				2.1	3.25	4.2	2.1	4.2	
	V_T^-	2.0				0.3	0.80	1.0	0.3	1.0	V
		4.5				0.9	2.00	2.45	0.9	2.45	
		6.0				1.2	2.60	3.2	1.2	3.2	
Hysteresis voltage	V_H	2.0				0.2	0.3	1.2	0.2	1.2	V
		4.5				0.4	0.5	2.1	0.4	2.1	
		6.0				0.5	0.7	2.5	0.5	2.5	

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

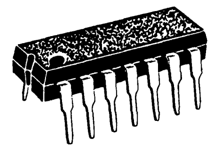
MN74HC20/MN74HC20S

Dual 4-Input NAND Gates

■ Description

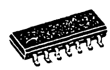
MN74HC20/MN74HC205 contain two 4-input positive isolation NAND gate circuits.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



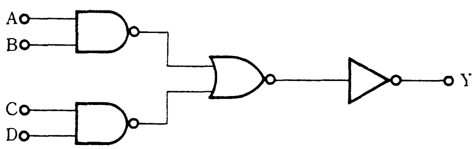
14-pin plastic DIL package

P-2

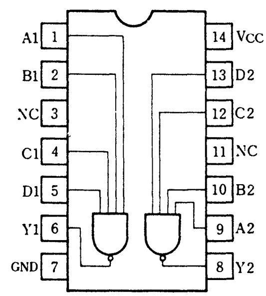


14-pin Panaflat package (SO-14D)

■ Logic diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5∼+7.0	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65∼+150	℃
Power dissipation	MN74HC20	Ta=−40∼+60℃	P_D	400	mW
		Ta=+60∼+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC20S	Ta=−40∼+60℃	P_D	275	mW
		Ta=+60∼+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

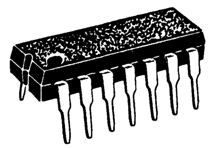
MN74HC21/MN74HC21S

Dual 4-Input AND Gates

■ Description

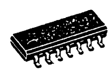
MN74HC21/MN74HC21S contain two 4-input positive isolation AND gate circuits.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



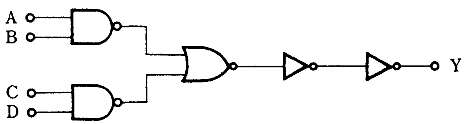
14-pin plastic DIL package

P-2

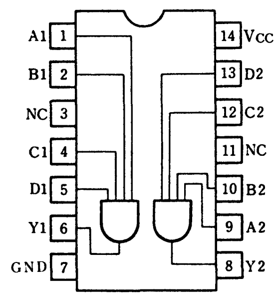


14-pin Panaflat package (SO-14D)

■ Logic diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC},I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC21	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC21S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

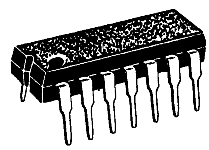
MN74HC27/MN74HC27S

Triple 3-Input NOR Gates

■ Description

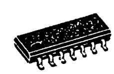
MN74HC27/MN74HC27S contain three 3-input positive isolation NOR gate circuits.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



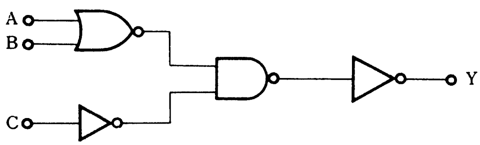
14-Pin plastic DIL package

P-2

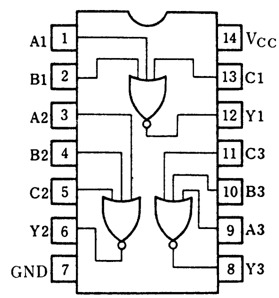


14-Pin Panaflat package (SO-14D)

■ Logic diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC27	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC27S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

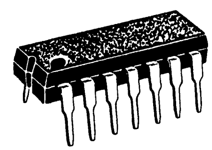
MN74HC30/MN74HC30S

8-Input NAND Gates

■ Description

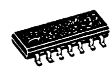
MN74HC30/MN74HC30S contain one 8-input positive isolation NAND gate circuits.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



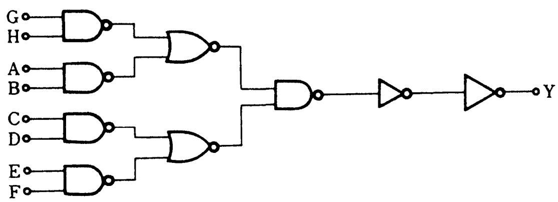
14-pin plastic DIL package

P-2

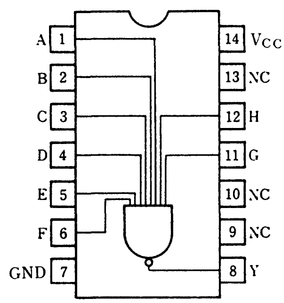


14-pin Panaflat package (SO-14D)

■ Logic diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC30	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC30S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

Panasonic

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			43	150		190	ns
		4.5			16	30		38	
		6.0			12	26		33	
Propagation time (H→L)	t_{PHL}	2.0			35	125		155	ns
		4.5			14	25		31	
		6.0			7	21		26	

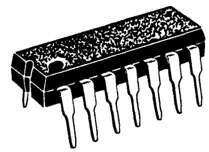
MN74HC32/MN74HC32S

Quad 2-Input OR Gates

■ Description

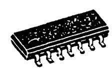
MN74HC32/MN74HC32S contain four 2-input positive isolation OR gate circuits.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



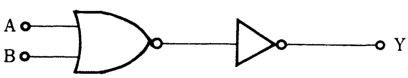
14-pin plastic DIL package

P-2

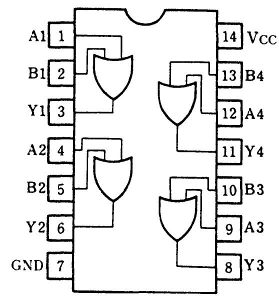


14-pin Panaflat package (SO-14D)

■ Logic diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC32	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC32S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

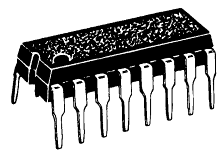
MN74HC42/MN74HC42S

BCD-to-Decimal Decoder

■ Description

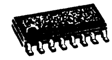
MN74HC42/MN74HC42S are BCD-to-Decimal Decorder. Only outputs from 10 outputs (Y0~Y9) corresponding to inputs (A~D) become "L". All other outputs become "H". When input becomes over 9, all outputs become "H".
Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent ot CMOS, and an operation speed of LS TTL. Each output can directly drive LS TTL 10-inputs. A Resistors and diode are provided between the V_{CC} and GND to protect the input and output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4

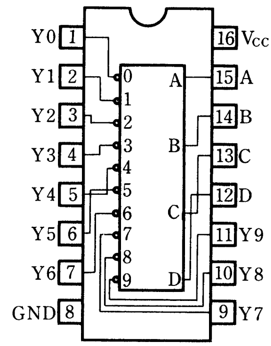


16-pin Panaflat package (SO-16D)

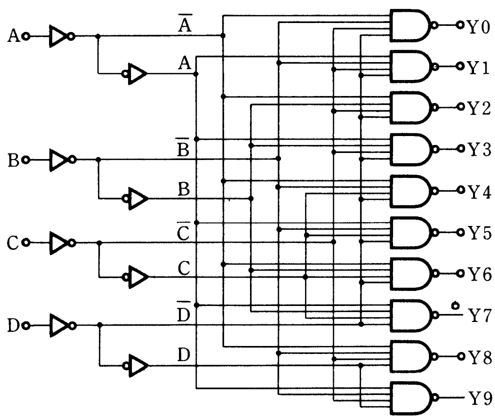
■ Truth table

No.	Input				Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
Ineffective output	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input/output voltage			V_I, V_O	−0.5~V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65~+150	℃
Power dissipation	MN74HC42	Ta=−40~+60℃	P_D	400	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC42S	Ta=−40~+60℃	P_D	275	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

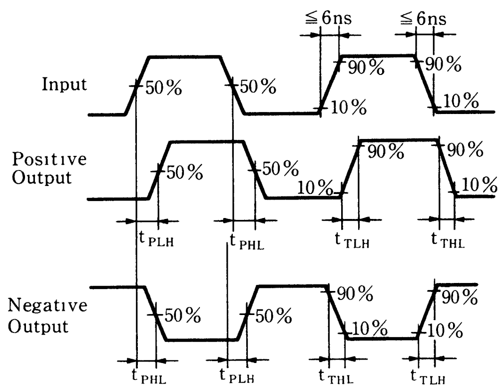
■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			26	75		95	ns
		4.5			11	15		19	
		6.0			8	13		16	
Output fall time	t_{THL}	2.0			21	75		95	ns
		4.5			8	15		19	
		6.0			6	13		16	
Propagation time A, B, C, D→Y (L→H)	t_{PLH}	2.0			39	125		155	ns
		4.5			18	25		31	
		6.0			13	21		26	
Propagation time A, B, C, D→Y (H→L)	t_{PHL}	2.0			36	125		155	ns
		4.5			15	25		31	
		6.0			11	21		26	

■ AC Characteristics Measuring Waveforms



MN74HC51/MN74HC51S

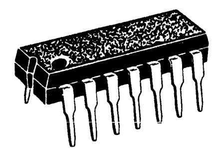
Dual AND-OR Invert Gates

■ Description

MN74HC51/MN74HC51S contain two AND-OR-INVERT gates. Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

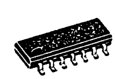
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



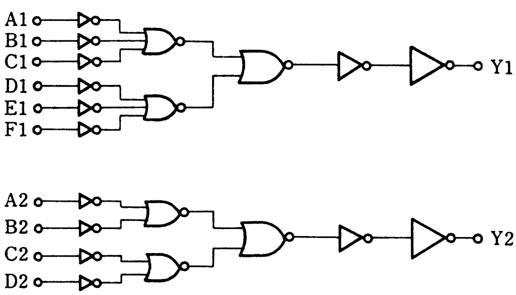
14-pin plastic DIL package

P-2

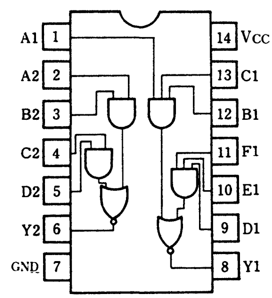


14-pin Panaflat package (SO-14D)

■ Logic diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC51	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC51S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			40	150		190	ns
		4.5			16	30		38	
		6.0			11	26		33	
Propagation time (H→L)	t_{PHL}	2.0			39	125		155	ns
		4.5			13	25		31	
		6.0			10	21		26	

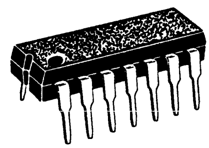
MN74HC73/MN74HC73S

Dual J-K Flip-Flops with Clear

■ Description

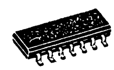
MN74HC73/MN74HC73S contain two J-K flip-flop circuits with clear. Each flip-flop has independent clear, J-K, clock input and complementary Q and $\overline{Q}$ outputs. Input data is transferred to the output on the negative going edge of the clock pulse. Clear operates at LOW level regardless of the clock. Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to CMOS, and an operation speed of LS TTL. Each output can directly drive LS TTL 10-inputs.
Resistors and diode are provided between the V_{CC} GND to protect the input and output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



14-pin plastic DIL package

P-2



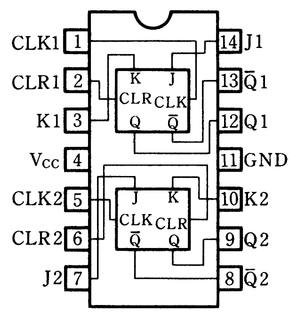
14-pin Panaflat package (SO-14D)

■ Truth Table

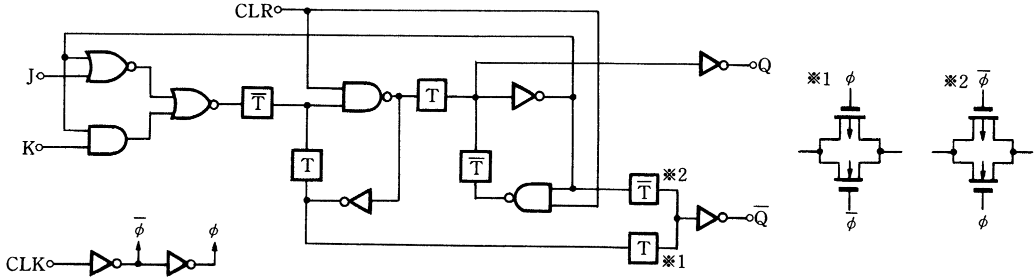
Input				Output	
CLR	CLK	J	K	Q	$\overline{Q}$
L	×	×	×	L	H
H	↘	L	L	Q0	$\overline{Q}$0
H	↘	H	L	H	L
H	↘	L	H	L	H
H	↘	H	H	Toggle	
H	H	×	×	Q0	$\overline{Q}$0

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ↘: Rise of negative direction
3. Q_O: Q level prior to determination of input condition shown in table
4. $\overline{Q}_O$: Q level prior to determination of input condition shown in table
5. Toggle: With ↘ change, output becomes a complement of the previous condition

Pin configuration (top view)



■ Logic diagram (1 gate)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5∼+7.0	V
Input/output voltage			V_I, V_O	−0.5∼V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65∼+150	℃
Power dissipation	MN74HC73	Ta=−40∼+60℃	P_D	400	mW
		Ta=+60∼+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC73S	Ta=−40∼+60℃	P_D	275	mW
		Ta=+60∼+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4∼6.0	V
Input/output voltage	V_I, V_O		0∼V_{CC}	V
Operating temperature range	T_A		−40∼+85	℃
Input rise and fall time	t_r, t_f	2.0	0∼1000	ns
		4.5	0∼500	ns
		6.0	0∼400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=−40∼+85℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					4.0		40.0	μA

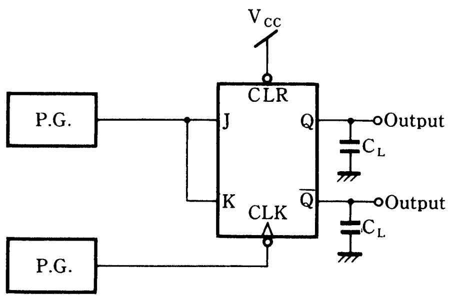
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time CLK→Q, $\overline{Q}$ (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
Propagation time CLK→Q, $\overline{Q}$ (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	
Propagation time CLR→$\overline{Q}$ (L→H)	t_{PLH}	2.0				175		220	ns
		4.5			22	35		44	
		6.0				30		37	
Propagation time CLR→Q (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
Minimum pulse width CLR	t_W	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			6	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5			2	15		19	
		6.0				13		16	
Maximum clock frequency	$f_{max.}$	2.0		6			4		MHz
		4.5		30	72		24		
		6.0		35			28		

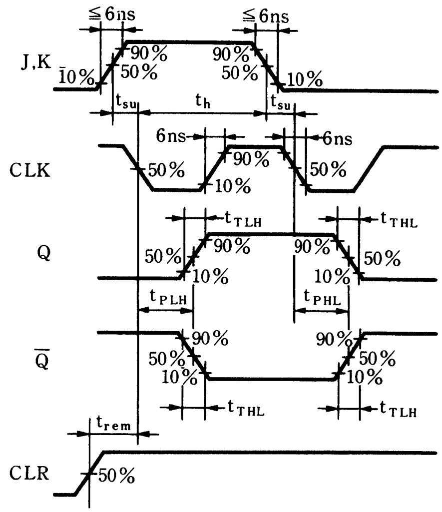
• Switching Time Measuring Circuit and Waveforms

[1] t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL} (CLK→Q, $\overline{Q}$), t_{rem}, t_h

1. Measuring Circuit (t_{PLH}, t_{PHL})

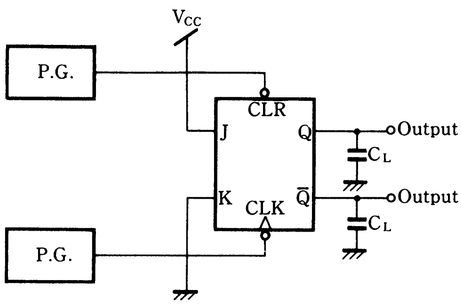


2. Waveforms

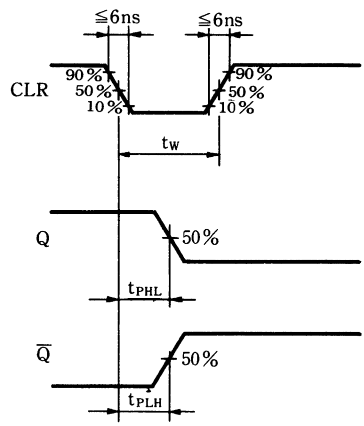


[2] t_{PLH}/t_{PHL} (CLR→Q, $\overline{Q}$), t_W

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



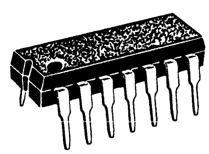
MN74HC74/MN74HC74S

Dual D-Type Flip-Flops with Preset and Clear

■ Description

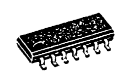
MN74HC74/MN74HC74S contain two D-type flip-flop circuits with preset and clear. Each flip-flop has independent clear, preset, data, clock input and complementary Q and $\overline{Q}$ outputs. Input data is transferred to the output on the positive going edge of the clock pulse. Preset and clear operate at LOW level regardless of the clock. Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to CMOS, and an operation speed of LS TTL. Each output can directly drive LS TTL 10-inputs.
Resistors and diodes are provided between the V_{CC} GND to protect of the input and output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



14-pin plastic DIL package

P-2



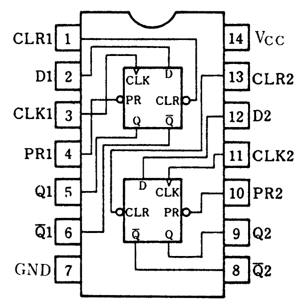
14-pin Panaflat package (SO-14D)

■ Truth table

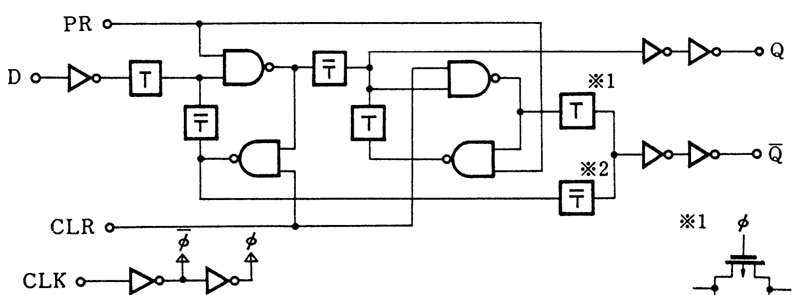
Input				Output	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	×	Q_0	$\overline{Q}_0$

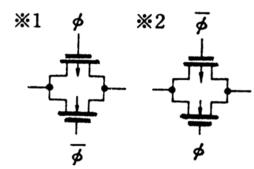
Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ↑: Rise of positive direction
3. Q_O: Q level prior to determination of input condition shown in table
4. $\overline{Q}_O$: Q level prior to determination of input condition shown in table
5. H*: When preset and clear are low, Q and $\overline{Q}$ are HIGH; however, when preset and clear simultaneously change to HIGH, requirements of Q and $\overline{Q}$ cannot be predicted.

Pin configuration (top view)



■ Logic Diagram (1 Gate)





■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input/output voltage			V_I, V_O	−0.5~V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65~+150	℃
Power dissipation	MN74HC74	Ta=−40~+60℃	P_D	400	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC74S	Ta=−40~+60℃	P_D	275	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25℃			Ta=−40~+85℃		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					4.0		40.0	μA

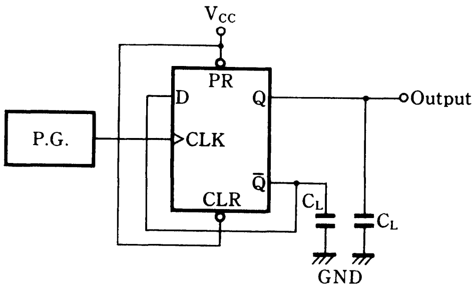
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time CLK→Q,$\overline{Q}$ (L→H)	t_{PLH}	2.0			32	150		190	ns
		4.5			14	30		38	
		6.0			11	26		33	
Propagation time CLK→Q,$\overline{Q}$ (H→L)	t_{PHL}	2.0			32	150		190	ns
		4.5			14	30		38	
		6.0			11	26		33	
Propagation time PR,CLR→Q,$\overline{Q}$ (L→H)	t_{PLH}	2.0			32	150		190	ns
		4.5			14	30		38	
		6.0			10	26		33	
Propagation time PR,CLR→Q,$\overline{Q}$ (H→L)	t_{PHL}	2.0			32	150		190	ns
		4.5			13	30		38	
		6.0			10	26		33	
Minimum Set-up time	t_{su}	2.0			7	75		95	ns
		4.5			4	15		19	
		6.0			3	13		16	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum pulse width PR, CLR	t_w	2.0			26	75		95	ns
		4.5			9	15		19	
		6.0			7	13		16	
Minimum recovery time PR, CLR	t_{rem}	2.0			5	75		95	ns
		4.5			4	15		19	
		6.0			2	13		16	
Maximum clock frequency	$f_{max.}$	2.0		6	20		4		MHz
		4.5		30	58		24		
		6.0		35	70		28		

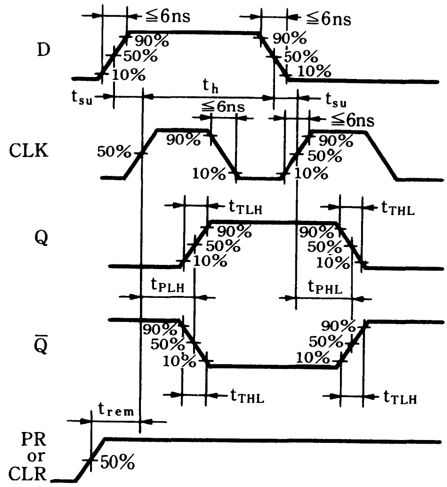
● Switching Time Measuring Circuit and Waveforms

[1] t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL} (CLK→Q, $\overline{Q}$), t_{rem}, t_h

1. Measuring Circuit (t_{PLH}, t_{PHL})

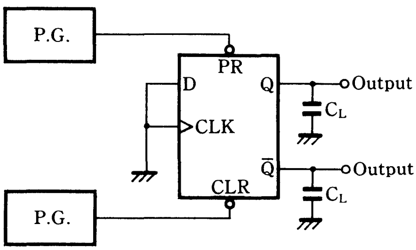


2. Waveforms

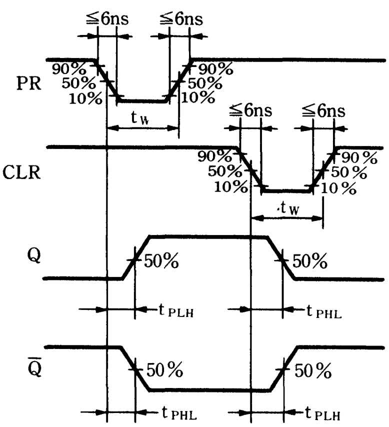


[2] t_{PLH}/t_{PHL} (CLR→Q, $\overline{Q}$), t_W

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



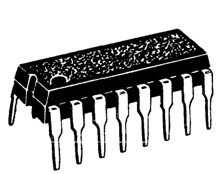
MN74HC75/MN74HC75S

4-Bit Bistable Latch

■ Description

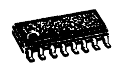
MN74HC75/MN74HC75S are 4-bit bistable latches with Q, $\overline{Q}$ output. These are suited for temporary binary data memory circuits between the data processing unit and the I/O, or between display units. Data at data input (D) is transferred to output Q, when enable pin (G) is "H"; output Q follows the data input state so long as the enable is "H". When the enable becomes "L", output is maintained as is until when the enable becomes "H". Output Q indicates the data input state when the enable changes from "H" to "L".
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



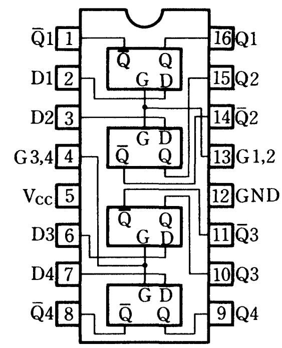
16-pin Panaflat package (SO-16D)

■ Truth table

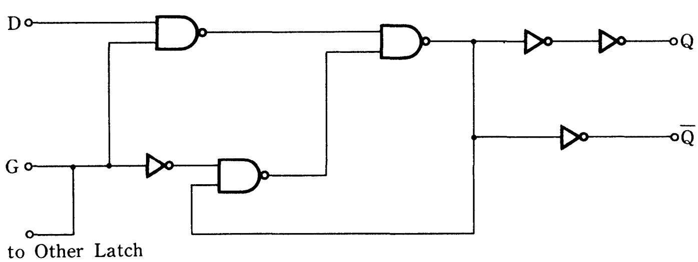
Input		Output	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
×	L	Q0	$\overline{Q}$0

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Q_O: Q level prior to determination of input condition shown in table
3. $\overline{Q}_O$: $\overline{Q}$ level prior to determination of input condition shown in table

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC75	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC75S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					4.0		40.0	μA

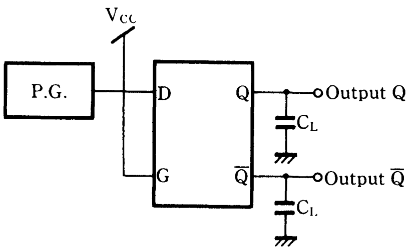
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			8	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	t_w	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time D→Q (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time D→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time D→$\overline{Q}$ (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			14	20		25	
		6.0				17		21	
Propagation time D→$\overline{Q}$ (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			14	20		25	
		6.0				17		21	
Propagation time G→Q (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			16	25		31	
		6.0				21		26	
Propagation time G→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			17	25		31	
		6.0				21		26	
Propagation time G→$\overline{Q}$ (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			17	25		31	
		6.0				21		26	
Propagation time G→$\overline{Q}$ (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	

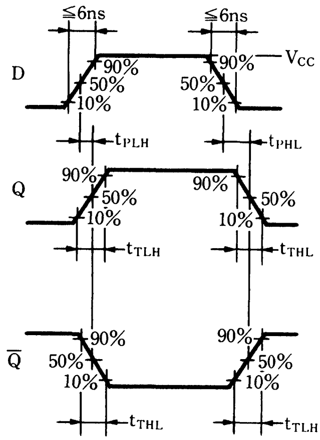
- Switching Time Measuring Circuit and Waveforms

[1] t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL} (CLK→Q, $\overline{Q}$), t_{rem}, t_h

1. Measuring Circuit (t_{PLH}, t_{PHL})

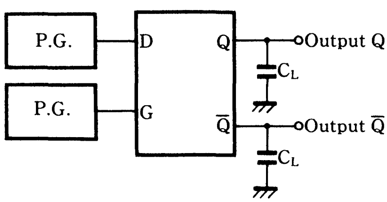


2. Waveforms

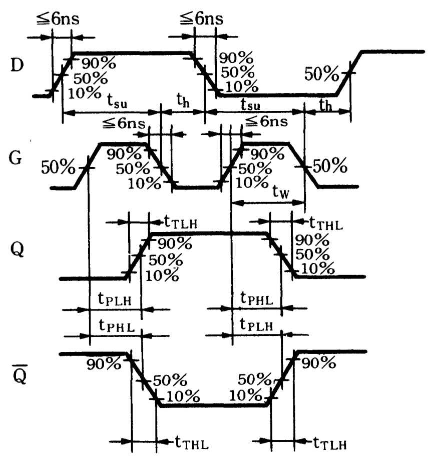


[2] t_{PLH}/t_{PHL} (CLR→Q, $\overline{Q}$), t_W

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



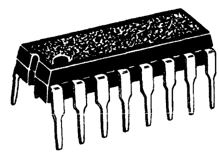
MN74HC76/MN74HC76S

Dual J-K Flip-Flops with Preset and Clear

■ Description

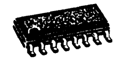
MN74HC76/MN74HC76S contain two J-K flip-flop circuits with preset and clear. Each flip-flop has independent J, K, clear, preset, clock input and complementary Q and $\overline{Q}$ outputs. Input data is transferred to the output on the negative going edge of the clock pulse. Preset and clear operate at low level regardless of the clock. Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to CMOS, and an operation speed of LS TTL. Each output can directly drive LS TTL 10-inputs. Resistor and diode are provided between the V_{CC} and GND to protect the input and output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



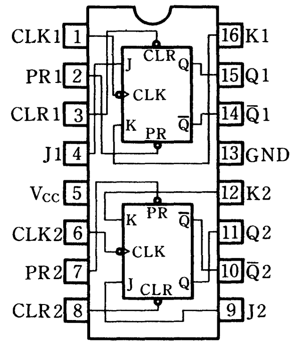
16-pin Panaflat package (SO-16D)

■ Truth table

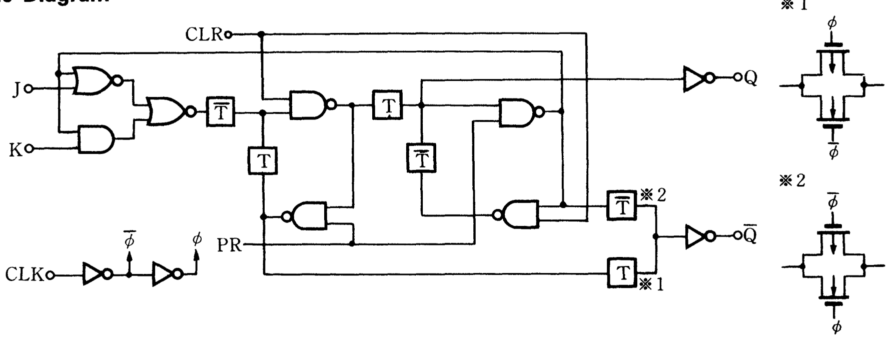
Input					Output	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↘	L	L	Q0	$\overline{Q}$0
H	H	↘	H	L	H	L
H	H	↘	L	H	L	H
H	H	↘	H	H	Toggle	
H	H	H	×	×	Q0	$\overline{Q}$0

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ↘: Rise of negative direction
3. Q_O: Q level prior to determination of input condition shown in table
4. $\overline{Q}_O$: $\overline{Q}$ level prior to determination of input condition shown in table
5. Toggle: With ↘ change, output becomes a complement of the previous condition
5. H*: When preset and clear are low, Q and $\overline{Q}$ are HIGH; however, when preset and clear simultaneously change to HIGH, requirements of Q and $\overline{Q}$ cannot be predicted.

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5∼+7.0	V
Input/output voltage			V_I, V_O	−0.5∼V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65∼+150	℃
Power dissipation	MN74HC76	Ta=−40∼+60℃	P_D	400	mW
		Ta=+60∼+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC76S	Ta=−40∼+60℃	P_D	275	mW
		Ta=+60∼+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4∼6.0	V
Input/output voltage	V_I, V_O		0∼V_{CC}	V
Operating temperature range	T_A		−40∼+85	℃
Input rise and fall time	t_r, t_f	2.0	0∼1000	ns
		4.5	0∼500	ns
		6.0	0∼400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40∼+85℃ min.	Ta=−40∼+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					4.0		40.0	μA

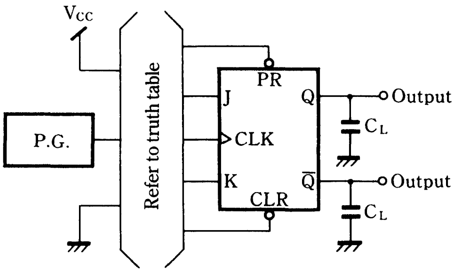
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time CLK→Q, $\overline{Q}$ (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			18	30		38	
		6.0				26		33	
Propagation time CLK→Q, $\overline{Q}$ (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		30	
Propagation time PR,CLR→Q,$\overline{Q}$ (L→H)	t_{PLH}	2.0				175		220	ns
		4.5			20	35		44	
		6.0				30		37	
Propagation time PR,CLR→Q,$\overline{Q}$ (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			19	35		44	
		6.0				30		37	
Propagation time PR,CLR	t_W	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			9	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			–	0		0	ns
		4.5			–	0		0	
		6.0			–	0		0	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5			1	15		19	
		6.0				13		16	
Maximum clock frequency	$f_{max.}$	2.0		6			4		MHz
		4.5		30	50		24		
		6.0		35			28		

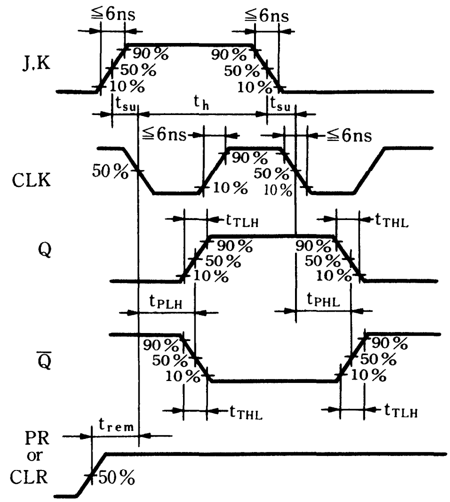
- Switching Time Measuring Circuit and Waveforms

[1] t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL} (CLK→Q, $\overline{Q}$), t_{rem}, t_h

1. Measuring Circuit (t_{PLH}, t_{PHL})

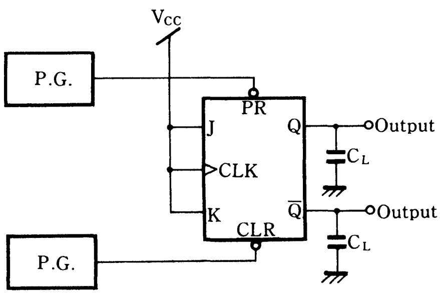


2. Waveforms

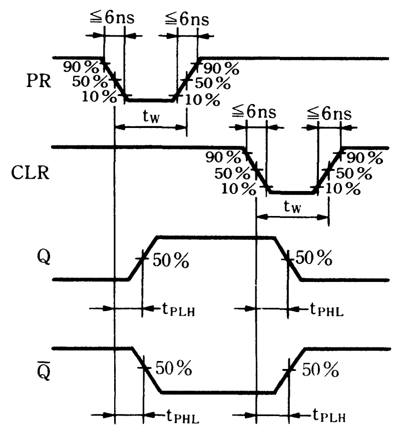


[2] t_{PLH}/t_{PHL} (CLR→Q, $\overline{Q}$), t_W

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



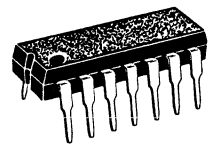
MN74HC77/MN74HC77S

4-Bit Bistable Latch

■ Description

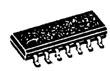
MN74HC77/MN74HC77S are 4-bit bistable latches. These are suited for temporary binary data memory circuits between the data processing unit and the I/O, or between display units. Data at data input (D) are transferred to output Q, when enable pin (G) is "H"; output Q follows the data input state so long as the enable is "H". When the enable becomes "L", output is maintained as is until when the enable becomes "H". Output Q indicates the data input state when the enable changes from "H" to "L".
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



14-pin plastic DIL package

P-2



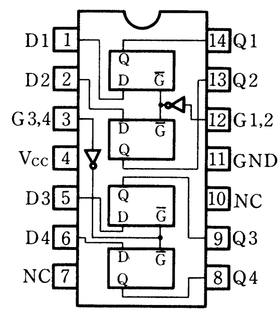
14-pin Panaflat package (SO-14D)

■ Truth table

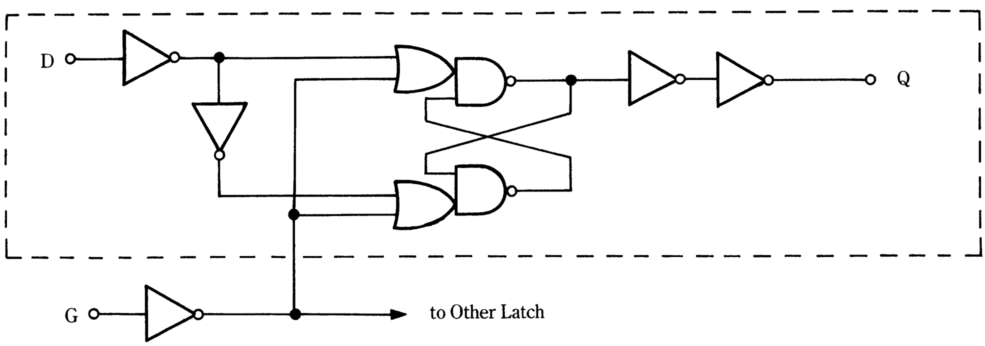
Input		Output
D	G	Q
L	H	L
H	H	H
×	L	Q0

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Q_O: Q level prior to determination of input condition shown in table

Pin configuration (top view)



■ Logic Diagram (1 gate)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC77	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC77S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=$-40\sim+85$℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	-20.0	μA	1.9	2.0		1.9		V
		4.5		-20.0	μA	4.4	4.5		4.4		
		6.0		-20.0	μA	5.9	6.0		5.9		
		4.5		-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					4.0		40.0	μA

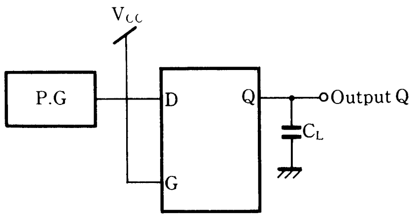
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			2	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum pulse width	t_W	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time D→Q (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
Propagation time D→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time G→Q (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			11	25		31	
		6.0				21		26	
Propagation time G→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	

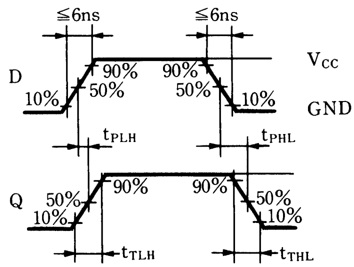
● Switching Time Measuring Circuit and Waveforms

[1] t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL} (CLK→Q, $\overline{Q}$), t_{rem}, t_h

1. Measuring Circuit (t_{PLH}, t_{PHL})

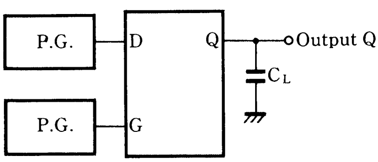


2. Waveforms

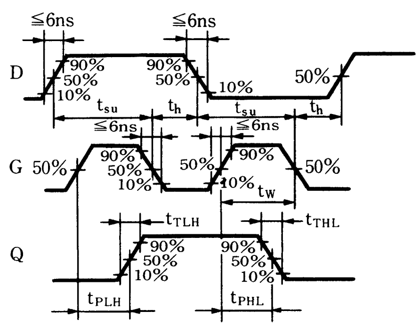


[2] t_{PLH}/t_{PHL} (CLR→Q, $\overline{Q}$), t_W

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



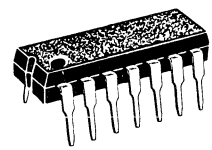
MN74HC86/MN74HC86S

Quad 2-Input Exclusive OR Gate

■ Description

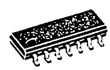
MN74HC86/MN74HC86S contain quad 2-input exclusive OR (XOR) gate.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL; LS TTL 10-inputs can be directly driven.
A resistor and diode are provided in V_{CC} and GND to protect the input/output from damge by static electricity. Same pin configuration and function as the standard 54LS/74LS.

P-1



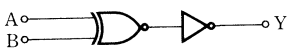
14-pin plastic DIL package

P-2

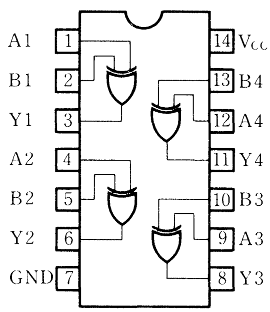


14-pin Panaflat package (SO-14D)

■ Logic Diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC86	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC86S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	Vcc (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

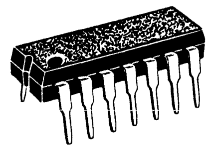
MN74HC107/MN74HC107S

Dual J-K Flip-Flops with Clear

■ Description

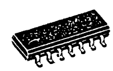
MN74HC107/MN74HC107S contain dual J-K flip-flop with clear, and each flip-flop has independent J, K, clock, clear input and complementary output Q and $\overline{Q}$. Input data is transferred to the output on the negative-going edge of the clock pulse. Clear operates on the low level regardless of the clock.
Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL; LS TTL 10-inputs can be directly driven.
A resistor and diode are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS.

P-1



14-pin plastic DIL package

P-2



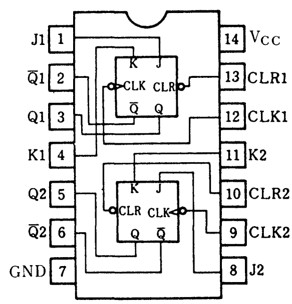
14-pin Panaflat package (SO-14D)

■ Truth table

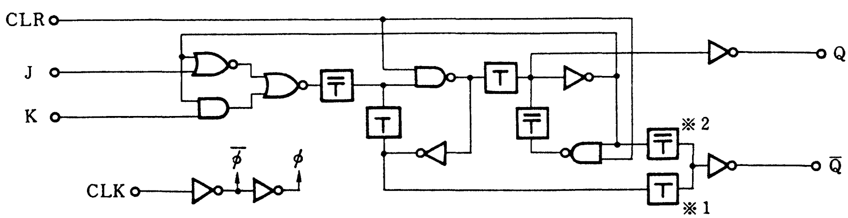
Input				Output	
CLR	CLK	J	K	Q	$\overline{Q}$
L	×	×	×	L	H
H	↓	L	L	Qo	$\overline{Q}$o
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	×	×	Qo	$\overline{Q}$o

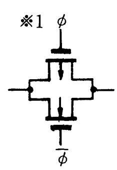
Note:
1. ↓: Data input is transferred to output on the negative-going edge from HIGH to LOW of the clock
2. ×: Either HIGH or LOW; it doesn't matter
3. Q_O: ($\overline{Q}_O$): Q ($\overline{Q}$) level prior to determination of input condition shown in table
4. Toggle: With ↓ change, output becomes a complement of the previous condition

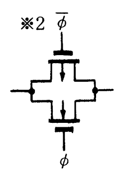
Pin configuration (top view)



■ Logic Diagram







■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	± 20	mA
Output parasitic diode current			I_{OK}	± 20	mA
Output current			I_O	± 25	mA
Supply current			I_{CC}, I_{GND}	± 50	mA
Storage temperature range			Tstg	$-65 \sim +150$	℃
Power dissipation	MN74HC107	Ta$=-40 \sim +60$℃	P_D	400	mW
		Ta$=+60 \sim +85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC107S	Ta$=-40 \sim +60$℃	P_D	275	mW
		Ta$=+60 \sim +85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4 \sim 6.0$	V
Input/output voltage	V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature range	T_A		$-40 \sim +85$	℃
Input rise and fall time	t_r, t_f	2.0	$0 \sim 1000$	ns
		4.5	$0 \sim 500$	ns
		6.0	$0 \sim 400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25℃			Ta$=-40 \sim +85$℃		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OL}	2.0	V_{IH} or V_{IL}	-20.0	μA	1.9	2.0		1.9		V
		4.5		-20.0	μA	4.4	4.5		4.4		
		6.0		-20.0	μA	5.9	6.0		5.9		
		4.5		-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					± 0.1		± 1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					4.0		40.0	μA

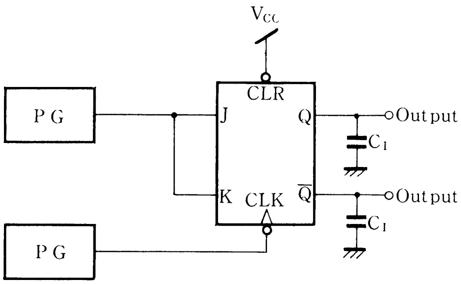
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time CLK→Q, $\overline{Q}$ (L→H)	t_{PLH}	2.0			34	125		155	ns
		4.5			14	25		31	
		6.0			11	21		26	
Propagation time CLK→Q, $\overline{Q}$ (H→L)	t_{PHL}	2.0			37	125		155	ns
		4.5			13	25		31	
		6.0			10	21		26	
Propagation time CLR→$\overline{Q}$ (L→H)	t_{PLH}	2.0			48	150		190	ns
		4.5			19	30		38	
		6.0			15	26		33	
Propagation time CLR→Q (H→L)	t_{PHL}	2.0			42	125		155	ns
		4.5			15	25		31	
		6.0			13	21		26	
Minimum Set-up time	t_{su}	2.0			16	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum pulse width CLR	t_w	2.0			17	75		95	ns
		4.5			8	15		19	
		6.0			6	13		16	
Minimum recovery time	t_{rem}	2.0			15	75		95	ns
		4.5			4	15		19	
		6.0			2	13		16	
Maximum clock frequency	$f_{max.}$	2.0		6	24		4		MHz
		4.5		30	64		24		
		6.0		35	83		28		

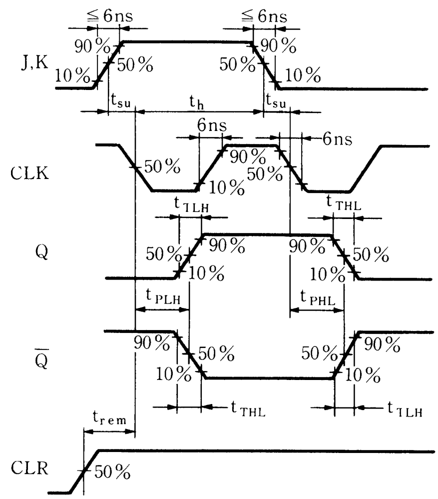
- Switching Time Measuring Circuit and Waveforms

[1] t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL} (CLK→Q, $\overline{Q}$), t_{rem}, t_h

1. Measuring Circuit (t_{PLH}, t_{PHL})

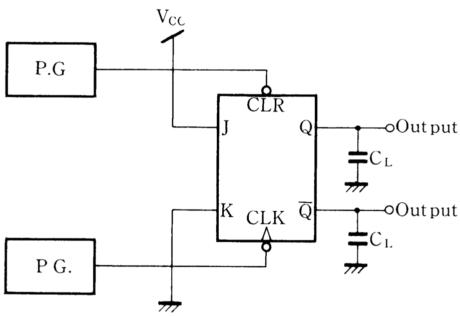


2. Waveforms

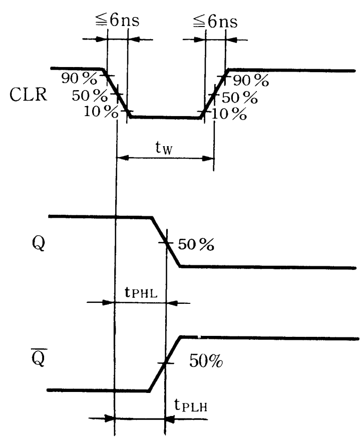


[2] t_{PLH}/t_{PHL} (CLR→Q, $\overline{Q}$), t_W

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



MN74HC109/MN74HC109S

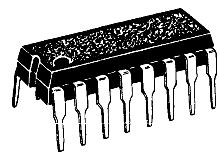
Dual J-$\overline{K}$ Flip-Flops with Preset and Clear

■ Description

MN74HC109/MN74HC109S contain dual J-$\overline{K}$ flip-flop with preset and clear and each flip-flop has independent J, $\overline{K}$, clock, clear, preset input and complementary output Q and $\overline{Q}$. Input data is transferred to the output on the rising edge of the clock pulse. Clear and preset operatate on the low level regardless of the clock. Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL; LS TTL 10-inputs can be directly driven.

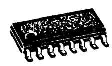
A Resistors and diode are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



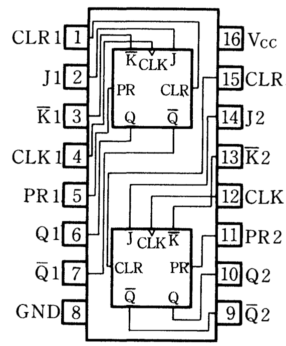
16-pin Panaflat package (SO-16D)

■ Truth Table

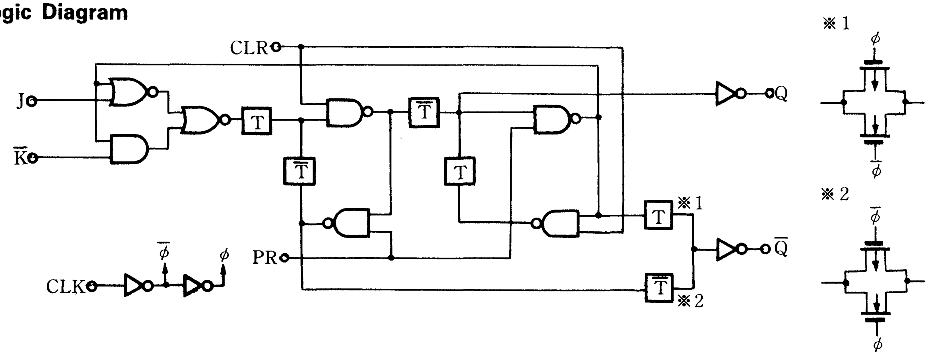
Input					Output	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	×	×	Q_0	$\overline{Q}_0$

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ↑: Rise of positive direction
3. Q_O: Q level prior to determination of input condition shown in table
4. $\overline{Q}_O$: Q level prior to determination of input condition shown in table
5. Toggle: With ↑ change, output becomes a complement of the previous condition
5. H*: When preset and clear are low, Q and $\overline{Q}$ are HIGH; however, when preset and clear simultaneously change to HIGH, requirements of Q and $\overline{Q}$ cannot be predicted.

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5∼+7.0	V
Input/output voltage			V_I, V_O	−0.5∼V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65∼+150	℃
Power dissipation	MN74HC109	Ta=−40∼+60℃	P_D	400	mW
		Ta=+60∼+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC109S	Ta=−40∼+60℃	P_D	275	mW
		Ta=+60∼+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4∼6.0	V
Input/output voltage	V_I, V_O		0∼V_{CC}	V
Operating temperature range	T_A		−40∼+85	℃
Input rise and fall time	t_r, t_f	2.0	0∼1000	ns
		4.5	0∼500	ns
		6.0	0∼400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40∼+85℃ min.	Ta=−40∼+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					4.0		40.0	μA

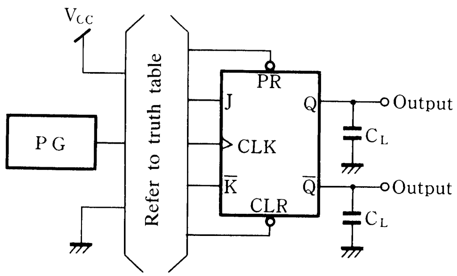
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40∼+85℃ min.	Ta=−40∼+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Propagation time CLK→Q, $\bar{Q}$ (L→H)	t_{PLH}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	
Propagation time CLK→Q, $\bar{Q}$ (H→L)	t_{PHL}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	
Propagation time PR, CLR→Q, $\bar{Q}$ (L→H)	t_{PLH}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	
Propagation time PR, CLR→Q, $\bar{Q}$ (H→L)	t_{PHL}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	
Minimum pulse width PR, CLR	t_W	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30			24		
		6.0		35			28		

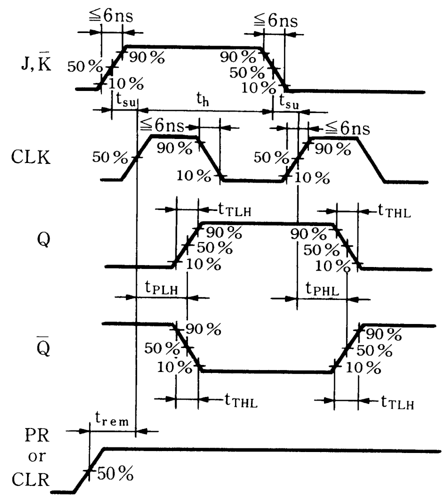
● Switching Time Measuring Circuit and Waveforms

[1] t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL} (CLK→Q, $\overline{Q}$), t_{rem}, t_h

1. Measuring Circuit (t_{PLH}, t_{PHL})

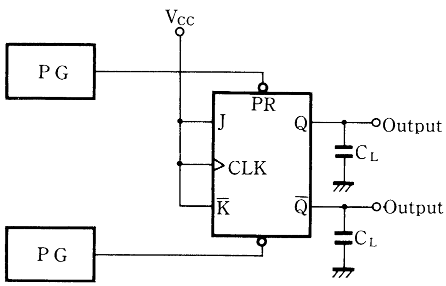


2. Waveforms

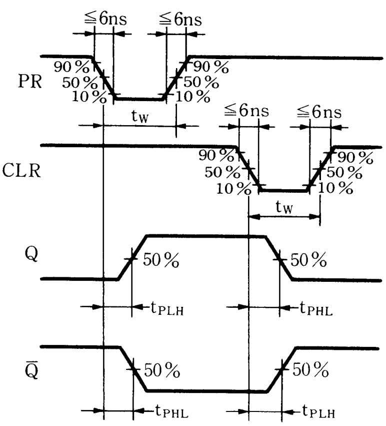


[2] t_{PLH}/t_{PHL} (CLR→Q, $\overline{Q}$), t_W

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



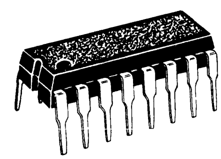
MN74HC112/MN74HC112S

Dual J-K Flip-Flops with Preset and Clear

■ Description

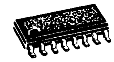
MN74HC112/MN74HC112S contain dual J-K flip-flop with clear, and each flip-flop has independent J, K, preset, clock, clear input and complementary output Q and $\overline{Q}$. Input data is transferred to the output on the negative going edge of the clock pulse. Clear operates on the low level regardless of the clock. Adoption of the silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL; LS TTL 10-inputs can be directly driven.
A Resistors and diode are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



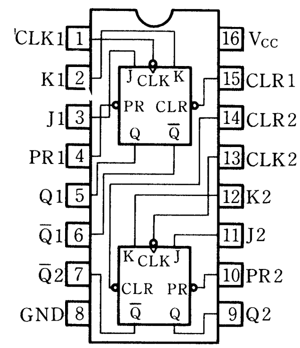
16-pin Panaflat package (SO-16D)

■ Truth Table

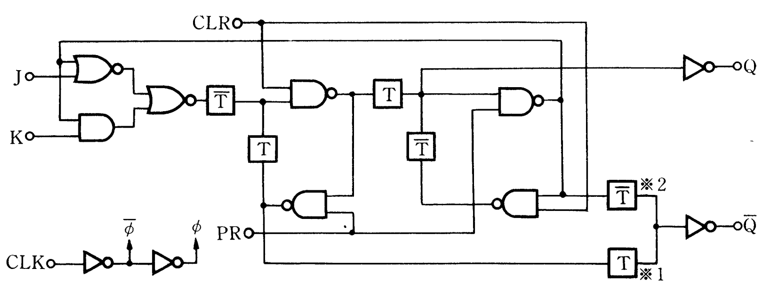
Input					Output	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	×	×	Q_0	$\overline{Q}_0$

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ↓: Rise of negative direction
3. Q_0: Q level prior to determination of input condition shown in table
4. $\overline{Q}_0$: $\overline{Q}$ level prior to determination of input condition shown in table
5. Toggle: With ↓ change, output becomes a complement of the previous condition
5. H*: When preset and clear are low, Q and $\overline{Q}$ are HIGH; however, when preset and clear simultaneously change to HIGH, requirements of Q and $\overline{Q}$ cannot be predicted.

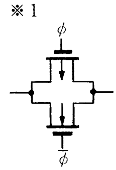
Pin configuration (top view)



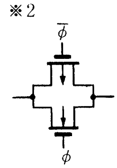
■ Logic Diagram



※1



※2



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65 \sim +150$	℃
Power dissipation	MN74HC112	Ta=$-40 \sim +60$℃	P_D	400	mW
		Ta=$+60 \sim +85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC112S	Ta=$-40 \sim +60$℃	P_D	275	mW
		Ta=$+60 \sim +85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4 \sim 6.0$	V
Input/output voltage	V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature range	T_A		$-40 \sim +85$	℃
Input rise and fall time	t_r, t_f	2.0	$0 \sim 1000$	ns
		4.5	$0 \sim 500$	ns
		6.0	$0 \sim 400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=$-40 \sim +85$℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					4.0		40.0	μA

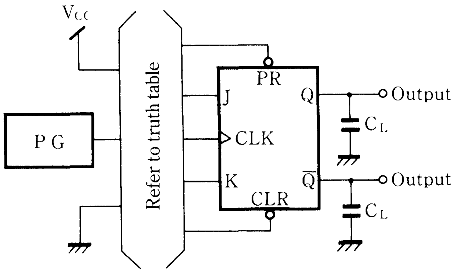
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time CLK→Q, $\overline{Q}$ (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			16	25		31	
		6.0				21		26	
Propagation time CLK→Q, $\overline{Q}$ (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			16	25		31	
		6.0				21		26	
Propagation time PR, CLR→Q, $\overline{Q}$ (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			17	25		31	
		6.0				21		26	
Propagation time PR, CLR→Q, $\overline{Q}$ (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			19	25		31	
		6.0				21		26	
Minimum pulse width PR, CLR	t_W	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			7	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5			1	15		19	
		6.0				13		16	
Maximum clock frequency	$f_{max.}$	2.0		6			4		MHz
		4.5		30	59		24		
		6.0		35			28		

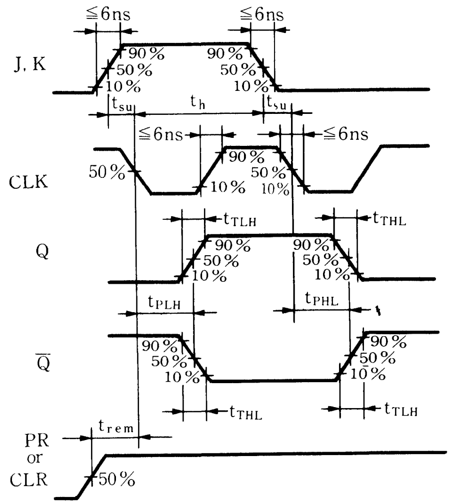
- Switching Time Measuring Circuit and Waveforms

[1] t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL} (CLK→Q, $\overline{Q}$), t_{rem}, t_h

1. Measuring Circuit (t_{PLH}, t_{PHL})

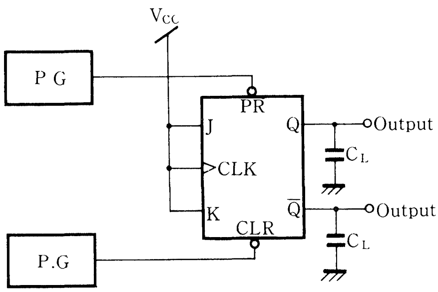


2. Waveforms

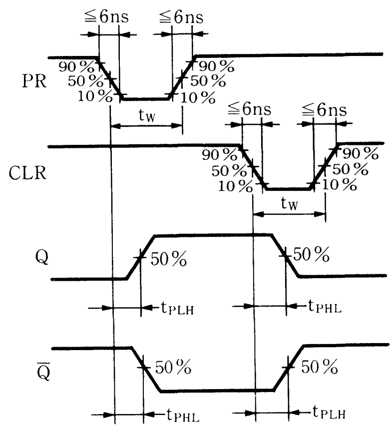


[2] t_{PLH}/t_{PHL} (CLR→Q, $\overline{Q}$), t_W

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



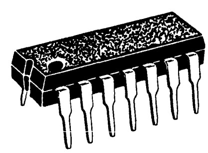
MN74HC125/MN74HC125S

Quad TRI-STATE Buffers

■ Description

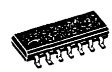
MN74HC125/MN74HC125S are high-speed non-inverted buffers consisting of quad tri-state outputs. High-speed operation is possible for driving a large capacitance bus line owing to large current output. The gate can be controlled by tri-state input (C), when output becomes enabled at LOW. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P- 1



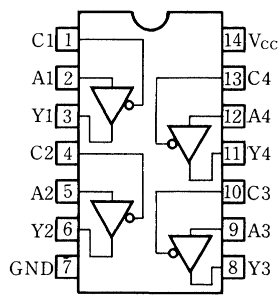
14-pin plastic DIL package

P- 2



14-pin Panaflat package (SO-14D)

Pin Configuration (top view)

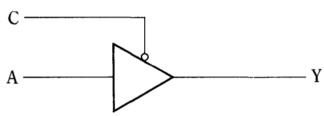


■ Truth Table

Input		Output
C	A	Y
H	×	Hi-Z
L	L	L
L	H	H

Note:
1. H: HIGH level
2. L: LOW level
3. ×: Either HIGH or LOW; doesn't matter.
4. Hi-Z: Hi-Impeadance

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input/output voltage			V_I, V_O	−0.5~V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65~+150	°C
Power dissipation	MN74HC125	Ta=−40~+60°C	P_D	400	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC125S	Ta=−40~+60°C	P_D	275	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating temperature range	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	°C
Input rise and fall time	t_r, t_f	V_{CC}=2.0V	0~1000	ns
		V_{CC}=4.5V	0~500	ns
		V_{CC}=6.0V	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	I_O Unit	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		V
		6.0				4.2			4.2		V
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	V
		6.0						1.2		1.2	V
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		V
		6.0		−20.0	μA	5.9	6.0		5.9		V
		4.5		−6.0	mA	3.86			3.76		V
		6.0		−7.8	mA	5.36			5.26		V
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	V
		6.0		20.0	μA		0.0	0.1		0.1	V
		4.5		6.0	mA			0.32		0.37	V
		6.0		7.8	mA			0.32		0.37	V
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

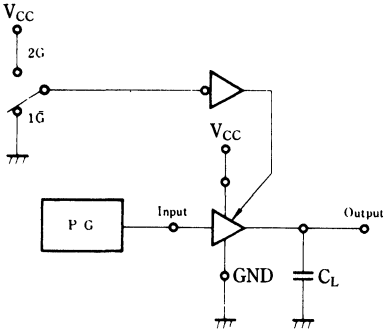
■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25°C			Ta=−40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0			19	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Output fall time	t_{THL}	2.0			15	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
Propagation time (L→H)	t_{PLH}	2.0			15	75		95	ns
		4.5			9	15		19	
		6.0			8	13		16	
Propagation time (H→L)	t_{PHL}	2.0			15	75		95	ns
		4.5			8	15		19	
		6.0			6	13		16	
Propagation time (H→Z)	t_{PHZ}	2.0	R_L=1kΩ		20	125		155	ns
		4.5			15	25		31	
		6.0			14	21		26	
Propagation time (L→Z)	t_{PLZ}	2.0	R_L=1kΩ		18	100		125	ns
		4.5			12	20		25	
		6.0			11	17		21	
Propagation time (Z→H)	t_{PZH}	2.0	R_L=1kΩ		18	100		125	ns
		4.5			10	20		25	
		6.0			8	17		21	
Propagation time (Z→L)	t_{PZL}	2.0	R_L=1kΩ		28	100		125	ns
		4.5			8	20		25	
		6.0			7	17		21	

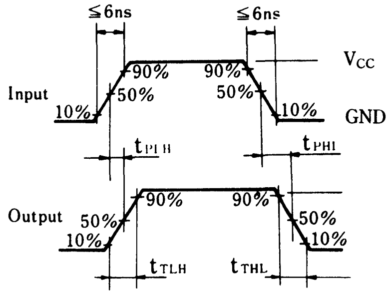
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

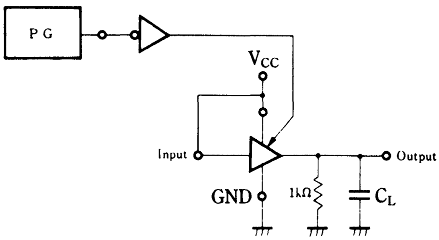


2. Waveforms

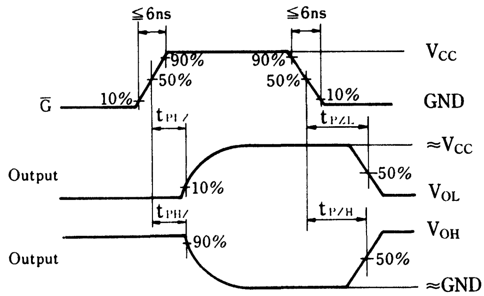


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

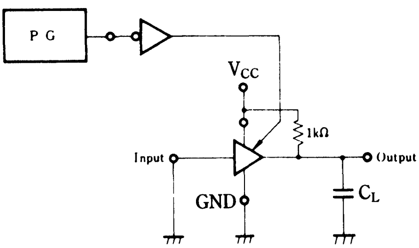


2. Waveforms (t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



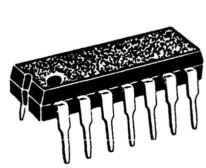
MN74HC126/MN74HC126S

Quad TRI-STATE Buffers

MN74HC126/MN74HC126S are high-speed non-inverted buffers consisting of quad tri-state outputs. High-speed operation is possible for driving a large capacitance bus line owing to large current output. The gate can be controlled by tri-state input (C), when output becomes enabled at HIGH. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven.

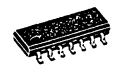
Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P- 1



14-pin plastic DIL package

P- 2



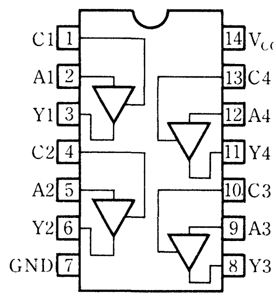
14-pin Panaflat package (SO-14D)

■ Truth Table

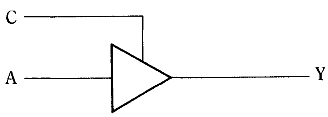
Input		Output
C	A	Y
L	×	Hi-Z
H	L	L
H	H	H

Note:
1. H: HIGH level
2. L: LOW level
3. ×: Either HIGH or LOW; doesn't matter.
4. Hi-Z: Hi-Impeadance

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	°C
Power dissipation	MN74HC126	Ta=$-40\sim+60$°C	P_D	400	mW
		Ta=$+60\sim+85$°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC126S	Ta=$-40\sim+60$°C	P_D	275	mW
		Ta=$+60\sim+85$°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating usppply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	°C
Input rise and fall time	t_r, t_f	V_{CC}=2.0V	0~1000	ns
		V_{CC}=4.5V	0~500	ns
		V_{CC}=6.0V	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O	Unit	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		V
		6.0				4.2			4.2		V
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	V
		6.0						1.2		1.2	V
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		V
		6.0	or	−20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	−6.0	mA	3.86			3.76		V
		6.0		−7.8	mA	5.36			5.26		V
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	6.0	mA			0.32		0.37	V
		6.0		7.8	mA			0.32		0.37	V
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

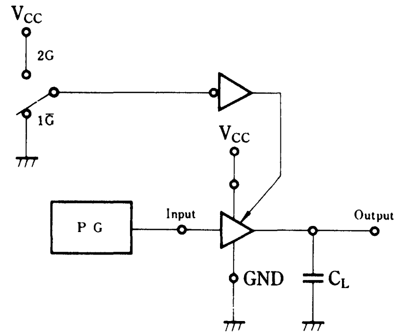
■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25°C			Ta=−40∼+85°C		
				min.	typ.	max.	min.	max.	
Output irse time	t_{TLH}	2.0			18	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Output fall time	t_{THL}	2.0			13	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
Propagation time (L→H)	t_{PLH}	2.0			19	75		95	ns
		4.5			9	15		19	
		6.0			8	13		16	
Propagation time (H→L)	t_{PHL}	2.0			19	75		95	ns
		4.5			8	15		19	
		6.0			6	13		16	
Propagation time (H→Z)	t_{PHZ}	2.0	R_L=1kΩ		20	125		155	ns
		4.5			15	25		31	
		6.0			14	21		26	
Propagation time (L→Z)	t_{PLZ}	2.0	R_L=1kΩ		18	100		125	ns
		4.5			12	20		25	
		6.0			11	17		21	
Propagation time (Z→H)	t_{PZH}	2.0	R_L=1kΩ		19	100		125	ns
		4.5			10	20		25	
		6.0			8	17		21	
Propagation time (Z→L)	t_{PZL}	2.0	R_L=1kΩ		20	100		125	ns
		4.5			8	20		25	
		6.0			7	17		21	

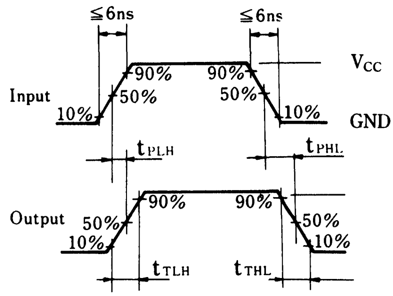
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

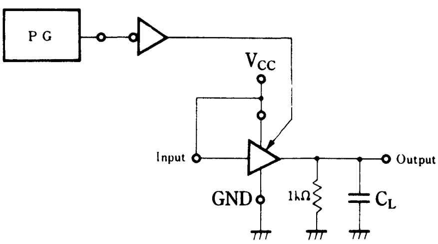


2. Waveforms

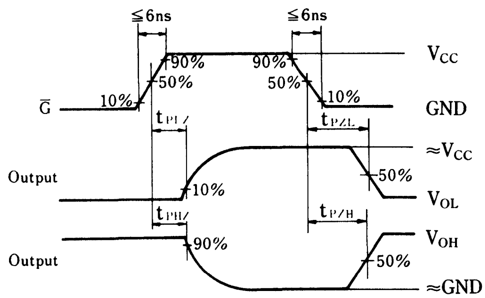


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

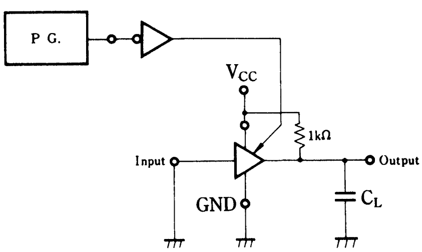


2. Waveforms (t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



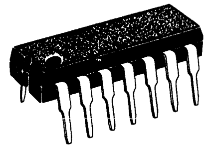
MN74HC132/MN74HC132S

Quad 2-Input NAND Schmitt Triggers

■ Description

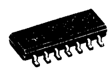
MN74HC132/MN74HC132S contain quad 2-input NAND with Schmitt triggers at all input terminals.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Because the circuit threshold voltage differs (V_{IH}, V_{IL}) when the input waveform rises and falls, wider applications are possible for the line reciever, waveform shaping and multi-vibrator in addition to the normal inverter.
Resistors and diode are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

P-1



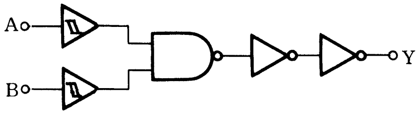
14-pin plastic DIL package

P-2

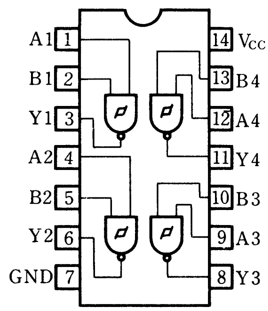


14-pin Panaflat package (SO-14D)

■ Logic Diagram



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC132	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC132S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O	Unit	Ta=25℃			Ta=−40~+85℃		
						min.	typ.	max.	min.	max.	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9	0.1	V
		4.5		−20.0	μA	4.4	4.5		4.4	0.1	
		6.0		−20.0	μA	5.9	6.0		5.9	0.1	
		4.5		−4.0	mA	3.86			3.76	0.37	
		6.0		−5.2	mA	5.36			5.26	0.37	
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA
Input threshold voltage	V_{T^+}	2.0				0.7	1.35	1.5	0.7	1.5	V
		4.5				1.55	2.69	3.15	1.55	3.15	
		6.0				2.1	3.55	4.2	2.1	4.2	
	V_{T^-}	2.0				0.3	0.75	1.0	0.3	1.0	V
		4.5				0.9	1.85	2.45	0.9	2.45	
		6.0				1.2	2.45	3.2	1.2	3.2	
Hysteresis voltage	V_H	2.0				0.2	0.60	1.2	0.2	1.2	V
		4.5				0.4	0.84	2.1	0.4	2.1	
		6.0				0.5	1.10	2.5	0.5	2.5	

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40~+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
Propagation time (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	

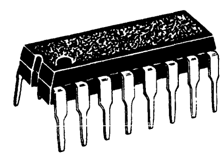
MN74HC133/MN74HC133S

13-Input NAND Gate

■ Description

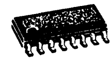
MN74HC133/MN74HC133S contain 13-input positive isolation NAND gate.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



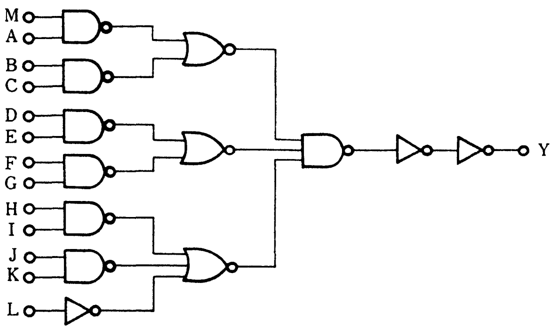
16-pin plastic DIL package

P-4

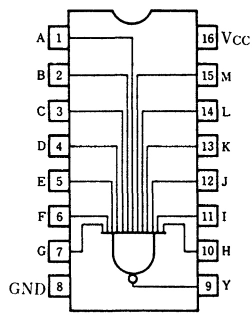


16-pin Panaflat package (SO-16D)

■ Logic Diagram



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	± 20	mA
Output parasitic diode current			I_{OK}	± 20	mA
Output current			I_O	± 25	mA
Supply current			I_{CC}, I_{GND}	± 50	mA
Storage temperature range			Tstg	$-65 \sim +150$	℃
Power dissipation	MN74HC133	Ta=$-40 \sim +60$℃	P_D	400	mW
		Ta=$+60 \sim +85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC133S	Ta=$-40 \sim +60$℃	P_D	275	mW
		Ta=$+60 \sim +85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
Propagation time (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	

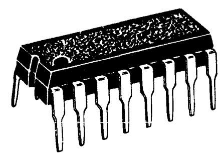
MN74HC137/MN74HC137S

3-to-8 Line Decoder with Address Latches (Inverted Output)

■ Description

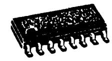
MN74HC137/MN74HC137S are high-speed 3-to-8 line decoders with three address latches. Addresses are stored, when $\overline{GL}$ input is "H". When enable input G1 is "H" and G2 is "L", the output depending on A, B and C inputs become "L", and all other outputs become "H". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P- 3



16-pin plastic DIL package

P- 4



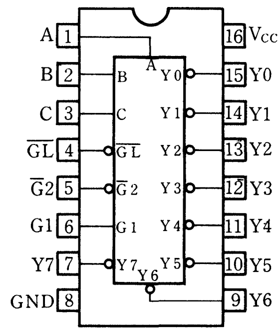
16-pin Panaflat package (SO-16D)

■ Truth Table

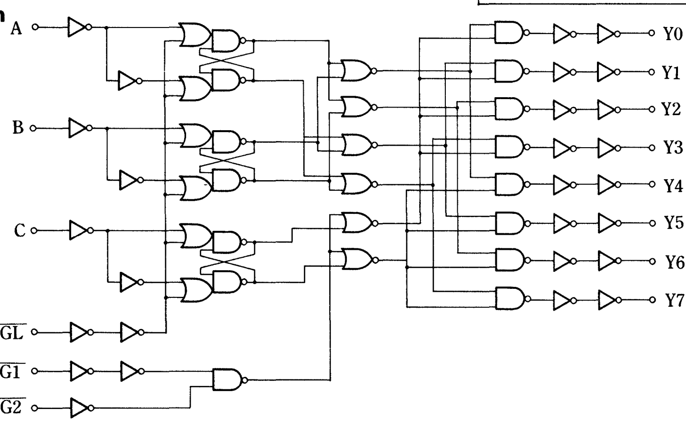
Input						Output							
Enable			Select										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
×	×	H	×	×	×	H	H	H	H	H	H	H	H
×	L	×	×	×	×	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	×	×	×	Output corresponding to stored address L all others, H							

Note:
1. H: HIGH level
2. L: LOW level
3. ×: Either HIGH or LOW; doesn't matter

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	°C
Power dissipateion	MN74HC137	Ta=−40∼+60°C	PD	400	mW
		Ta=+60∼+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC137S	Ta=−40∼+60°C	PD	275	mW
		Ta=+60∼+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	°C
Input rise and fall time	t_r, t_f	V_{CC}=2.0V	$0\sim1000$	ns
		V_{CC}=4.5V	$0\sim500$	ns
		V_{CC}=6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

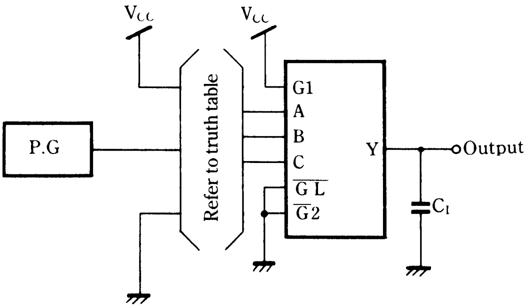
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40∼+85°C min.	Ta=−40∼+85°C max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		V
		6.0				4.2			4.2		V
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	V
		6.0						1.2		1.2	V
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		V
		6.0	or	−20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	−4.0	mA	3.86			3.76		V
		6.0		→5.2	mA	5.36			5.26		V
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

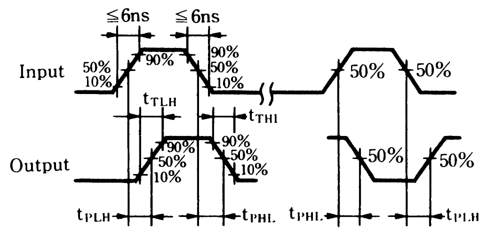
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40∼+85°C min.	Ta=−40∼+85°C max.	Unit
Output rise time	t_{TLH}	2.0			23	75		95	ns
		4.5			9	15		19	
		6.0			8	13		16	
Output fall time	t_{THL}	2.0			19	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time A, B, C→Y (L→H)	t_{PLH}	2.0			49	150		190	ns
		4.5			24	30		38	
		6.0			21	26		33	
Propagation time A, B, C→Y (H→L)	t_{PHL}	2.0			41	150		190	ns
		4.5			22	30		38	
		6.0			21	26		33	
Propagation time $\overline{GL}$→Y (L→H)	t_{PLH}	2.0			49	150		190	ns
		4.5			23	30		38	
		6.0			20	26		33	
Propagation time $\overline{GL}$→Y (H→H)	t_{PHL}	2.0			52	150		190	ns
		4.5			22	30		38	
		6.0			20	26		33	
Propagation time G1→Y (L→H)	t_{PLH}	2.0			35	150		190	ns
		4.5			19	30		38	
		6.0			15	26		33	
Propagation time G1→Y (H→Y)	t_{PHL}	2.0			35	150		190	ns
		4.5			19	30		38	
		6.0			15	26		33	
Propagation time $\overline{G2}$→Y (L→H)	t_{PLH}	2.0			35	150		190	ns
		4.5			18	30		38	
		6.0			17	26		33	
Propagation time $\overline{G}$2→Y (H→L)	t_{PHL}	2.0			35	150		190	ns
		4.5			19	30		38	
		6.0			18	26		33	
Minimum pulse width $\overline{GL}$→Y	t_w	2.0			≦6	100		125	ns
		4.5			≦6	20		25	
		6.0			≦6	17		21	
Minimum Set-up time A, B, C	t_{su}	2.0			17	100		125	ns
		4.5			4	20		25	
		6.0			2	17		21	
Minimum Hold time	t_h	2.0			—	75		95	ns
		4.5			—	15		19	
		6.0			—	13		16	

● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



2. Waveforms

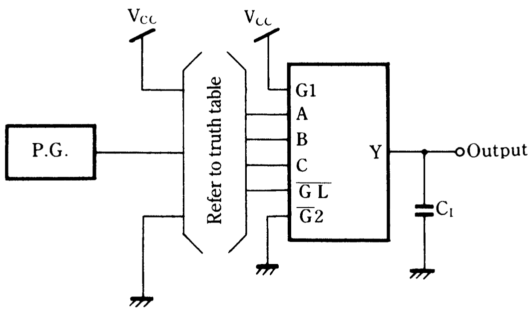


(Positive) (Negative)

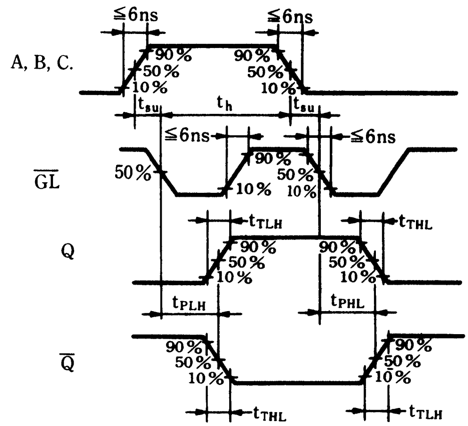
● Switching Time Measuring Circuit and Waveforms

[1] t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL} (CLK→Q, $\overline{Q}$), t_{rem}, t_h

1. Measuring Circuit (t_{PLH},t_{PHL})



2. Waveforms



MN74HC138/MN74HC138S

3-to-8 Line Decoder

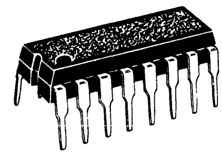
■ Description

MN74HC138/MN74HC138S are high-speed 3-to-8 line decoders decoding one of eight ouput lines depending on the condition of three select inputs (A, B and C) and three enable inputs (G1, G2A and G2B)

The enable input consists of an active LOW of 2-inputs and an active HIGH of 1-input, with makes the subsidiary connection easy. Low power dissipation and high noise margin equivalent to standard CMOS; operation speed of LS TTL. LS TTL 10 inputs can be directly driven.

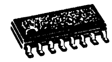
Resistors and diode are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



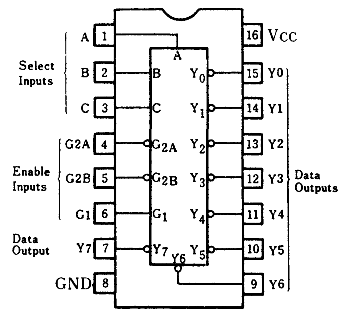
16-pin Panaflat package (SO-16D)

■ Truth Table

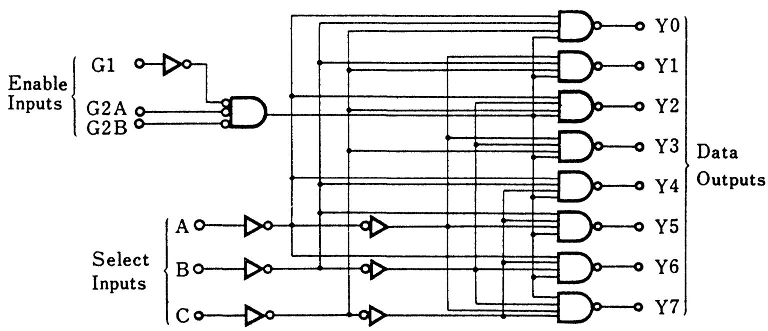
Input					Output							
Enable		Select										
G1	G2	C	B	A	Y0	Y1	Y3	Y2	Y4	Y5	Y6	Y7
×	H	×	×	×	H	H	H	H	H	H	H	H
L	×	×	×	×	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note:
1. G_2=G2A+G2B
2. ×: Either HIGH or LOW; it doesn't matter.

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC138	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC138S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

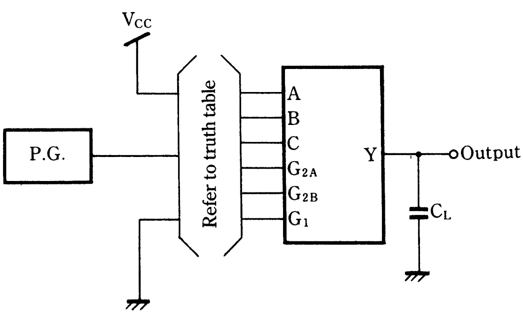
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

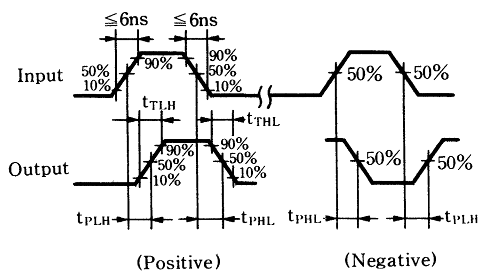
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time A, B, C→Y (L→H)	t_{PLH}	2.0				200		250	ns
		4.5			22	40		50	
		6.0				34		43	
Propagation time A, B, C→Y (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			19	35		44	
		6.0				30		37	
Propagation time Enable G1→Y (L→H)	t_{PLH}	2.0				200		250	ns
		4.5			25	40		50	
		6.0				34		43	
Propagation time Enable G1→Y (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			20	35		44	
		6.0				30		37	
Propagation time Enable G2A, G2B→Y (L→H)	t_{PLH}	2.0				200		250	ns
		4.5			22	40		50	
		6.0				34		43	
Propagation time Enable G2A, G2B→Y (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			19	35		44	
		6.0				30		37	

● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



2. Waveforms



MN74HC139/MN74HC139S

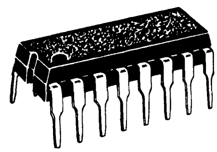
Dual 2-to-4 Line Decoders

■ Description

MN74HC139/MN74HC139S are high-speed silicon gate CMOS, 2-to-4 line decoders decoding one of 4 output lines depending on the condition of two select inputs (A and B) and one enable input (G). Two independent 2-to-4 line decoder/demultiplexers are used on one clip.

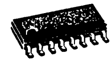
Low power dissipation and high noise margin equivalent to standard CMOS;operation speed of LS TTL. LS TTL 10 inputs can be directly driven. Aresistor and diode are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS.

P-3



16-pin plastic DIL package

P-4



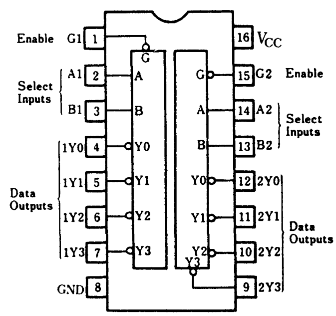
16-pin Panaflat package (SO-16D)

■ Truth table

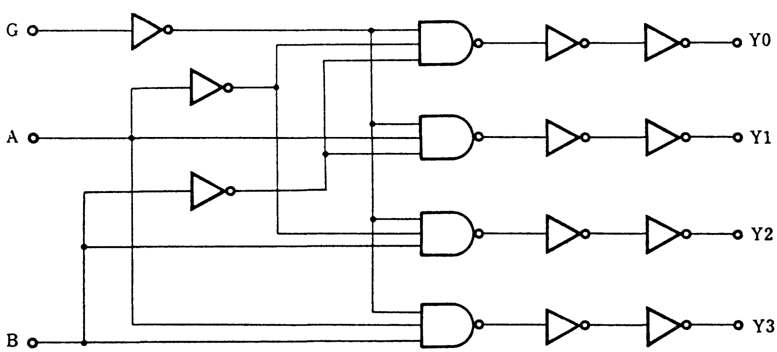
Input			Output			
Enable	Select					
G	B	A	Y_0	Y_1	Y_2	Y_3
H	×	×	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Note:
1. ×: Either HIGH or LOW; it doesn't matter

Pin configuration (top view)



■ Logic Diagram



Panasonic

■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC139	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/℃	
	MN74HC139S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/℃	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

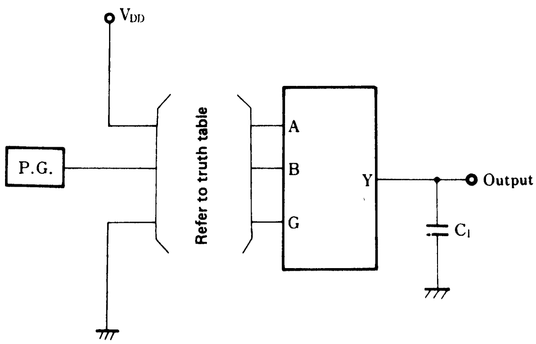
Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=$-40\sim+85$℃ min.	Ta=$-40\sim+85$℃ max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	-20.0	μA	1.9	2.0		1.9		V
		4.5		-20.0	μA	4.4	4.5		4.4		
		6.0		-20.0	μA	5.9	6.0		5.9		
		4.5		-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

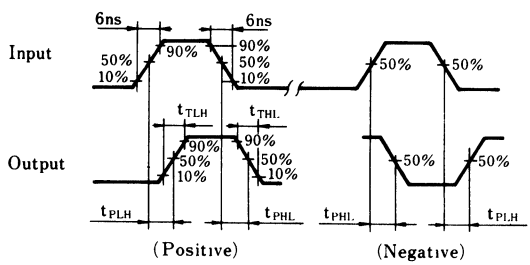
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time A, B→Y (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	
Propagation time A, B→Y (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
Propagation time Enable G→Y (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	
Propagation time Enable G→Y (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	

• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



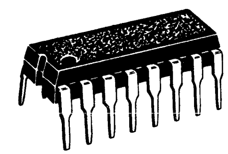
MN74HC147/MN74HC147S

10-to-4 Line Priority Encoder

■ Description

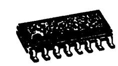
MN74HC147/MN74HC147S are 10-to-4 line priority encoders which prioritize the highest input and encode ten data lines to four data lines, when two or more input data are applied simultaneously. The binary signal 0 is encoded when all nine data inputs are "H". When all inputs and outputs are "L", the encoder is active. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



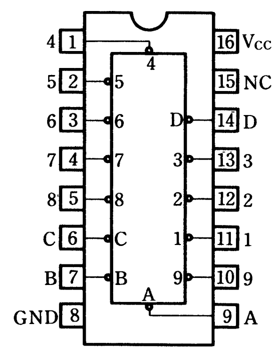
16-pin Panaflat package (SO-16D)

■ Truth table

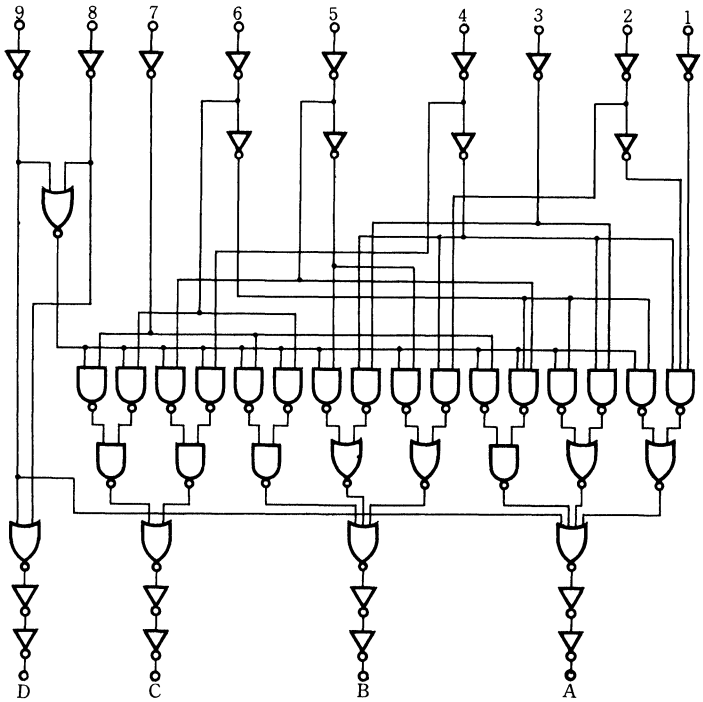
Input									Output			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
×	×	×	×	×	×	×	×	L	L	H	H	L
×	×	×	×	×	×	×	L	H	L	H	H	H
×	×	×	×	×	×	L	H	H	H	L	L	L
×	×	×	×	×	L	H	H	H	H	L	L	H
×	×	×	×	L	H	H	H	H	H	L	H	L
×	×	×	L	H	H	H	H	H	H	L	H	H
×	×	L	H	H	H	H	H	H	H	H	L	L
×	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

Note:
1. X: Either HIGH or LOW; it doesn't matter

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC147	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC147S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

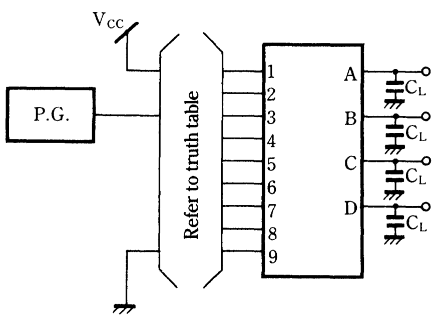
Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25℃			Ta=−40～+85℃		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

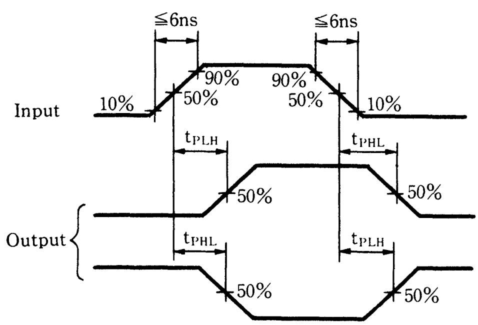
Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Propagation time 1 ~9 →A, B, C (L→H)	t_{PLH}	2.0				175		220	ns
		4.5				35		44	
		6.0				30		37	
Propagation time 1 ~9 →A, B, C (H→L)	t_{PHL}	2.0				175		220	ns
		4.5				35		44	
		6.0				30		37	
Propagation time 1 ~9 →D (L→H)	t_{PLH}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	
Propagation time 1 ~9 →D (H→L)	t_{PHL}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	

● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



MN74HC148/MN74HC148S

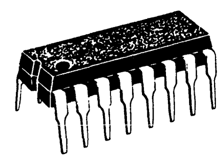
8-to-3 Line Priority Encoder

■ Description

MN74HC148/MN74HC148S are 8-to-3 line priority encoders which detect the most LOW out of eight input signals and output a binary code signal. Input consists of eight input signals (0 - 7) and an EI input. When EI input is "H", encoding stops and all outputs become "H".

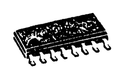
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



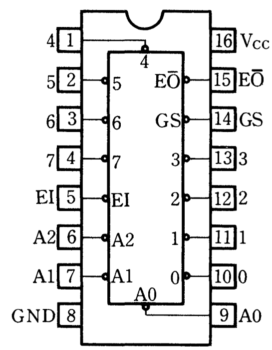
16-pin Panaflat package (SO-16D)

■ Truth Table

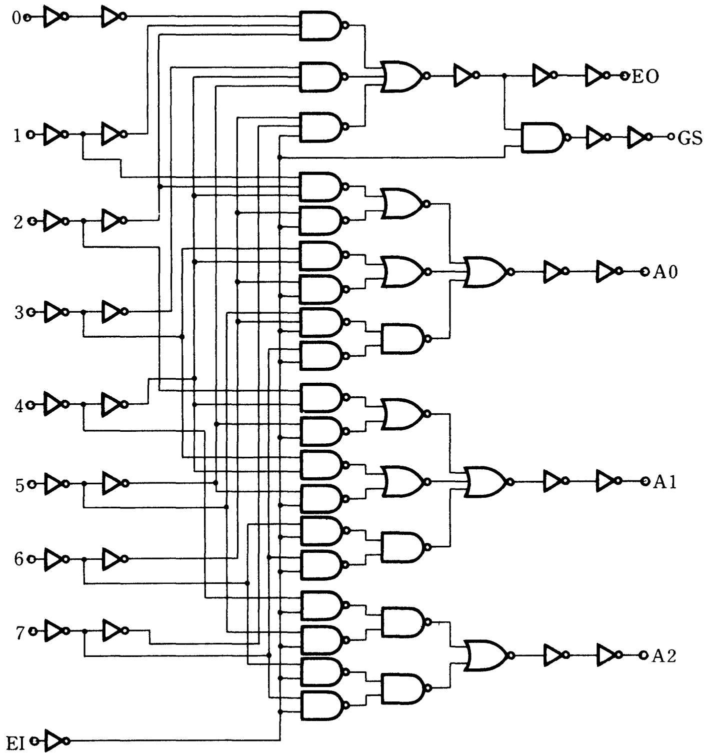
Input									Output				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	×	×	×	×	×	×	×	×	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	×	×	×	×	×	×	×	L	L	L	L	L	H
L	×	×	×	×	×	×	L	H	L	L	H	L	H
L	×	×	×	×	×	L	H	H	L	H	L	L	H
L	×	×	×	×	L	H	H	H	L	H	H	L	H
L	×	×	×	L	H	H	H	H	H	L	L	L	H
L	×	×	L	H	H	H	H	H	H	L	H	L	H
L	×	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

Note:
H: HIGH level
L: LOW level
×: Either HIGH or LOW; it doesn't matter

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC148	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC148S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

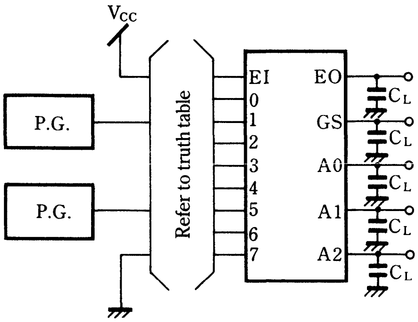
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

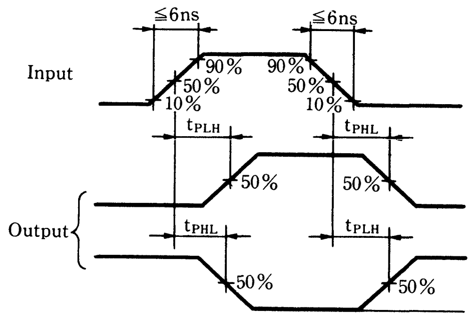
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time 0~7→A0, A1, A2 (L→H)	t_{PLH}	2.0				175		220	ns
		4.5				35		44	
		6.0				30		37	
Propagation time 0~7→A0, A1, A2 (H→L)	t_{PHL}	2.0				175		220	ns
		4.5				35		44	
		6.0				30		37	
Propagation time 0~7→EO (L→H)	t_{PLH}	2.0				175		220	ns
		4.5				35		44	
		6.0				30		37	
Propagation time 0~7→EO (H→L)	t_{PHL}	2.0				175		220	ns
		4.5				35		44	
		6.0				30		37	
Propagation time 0~7→GS (L→H)	t_{PLH}	2.0				200		250	ns
		4.5				40		50	
		6.0				34		43	
Propagation time 0~7→GS (H→L)	t_{PHL}	2.0				200		250	ns
		4.5				40		50	
		6.0				34		43	
Propagation time EI→A0, A1, A2 (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Propagation time EI→A0, A1, A2 (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Propagation time EI→GS (L→H)	t_{PLH}	2.0				175		220	ns
		4.5				35		44	
		6.0				30		37	
Propagation time EI→GS (H→L)	t_{PHL}	2.0				175		220	ns
		4.5				35		44	
		6.0				30		37	
Propagation time EI→EO (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Propagation time EI→EO (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	

● Switching Time Measurmg Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



MN74HC151/MN74HC151S

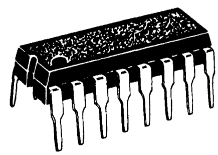
8-Channel Digital Multiplexer

■ Description

MN74HC151/MN74HC151S are digital multiplexer, which selects one input from 8-channel data input according to select input (A, B C), transfer data to the reverse phase outputs W and Y mutually. When strobe input is "L", the output is selected by the select input combination. When strobe input is "H", output W is "H" and output Y is "L".

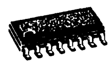
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



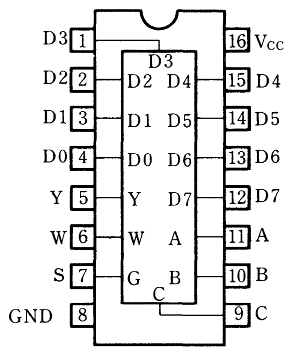
16-pin Panaflat package (SO-16D)

■ Truth Table

Input				Output	
Select			Strobe	Y	W
C	B	A	S		
×	×	×	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

Note:
1. X: Either HIGH or LOW; it doesn't matter
   D0, D1, ······· D7: respective data input level

Pin Configuration (top view)



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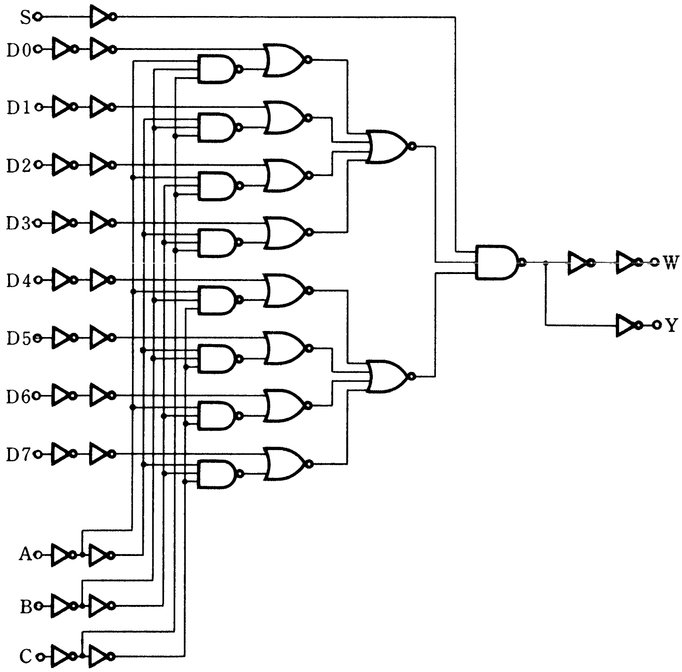
■ Logic diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC151	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC151S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

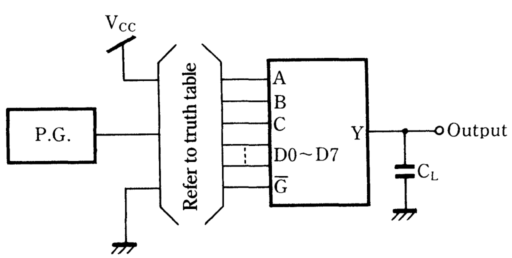
Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time A, B, C→Y (L→H)	t_{PLH}	2.0				200		250	ns
		4.5			23	40		50	
		6.0				34		43	
Propagation time A, B, C→Y (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			21	35		44	
		6.0				30		37	
Propagation time A, B, C→W (L→H)	t_{PLH}	2.0				200		250	ns
		4.5			22	40		50	
		6.0				34		43	
Propagation time A, B, C→W (H→L)	t_{PHL}	2.0				200		250	ns
		4.5			22	40		50	
		6.0				34		43	

■ AC/Characteristics (Cont'd)

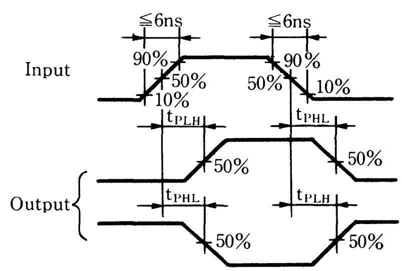
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Propagation time S→Y (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			10	20		25	
		6.0				17		21	
Propagation time S→Y (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			9	15		19	
		6.0				13		16	
Propagation time S→W (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
Propagation time S→W (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			10	20		25	
		6.0				17		21	
Propagation time D→Y (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	
Propagation time D→Y (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
Propagation time D→W (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
Propagation time D→W (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	

- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



MN74HC153/MN74HC153S

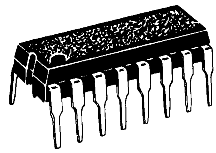
Dual 4-Input Multiplexer

■ Description

MN74HC153/MN74HC153S are dual 4-input multiplexer which transfer one of four data to output Y according to the common select input (A, B). Each multiplexer has respective enable input multiplexer functions at LOW level. At HIGH level, output is fixed LOW.

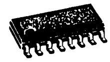
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



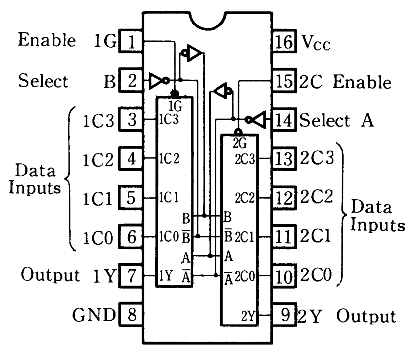
16-pin Panaflat package (SO-16D)

■ Truth table

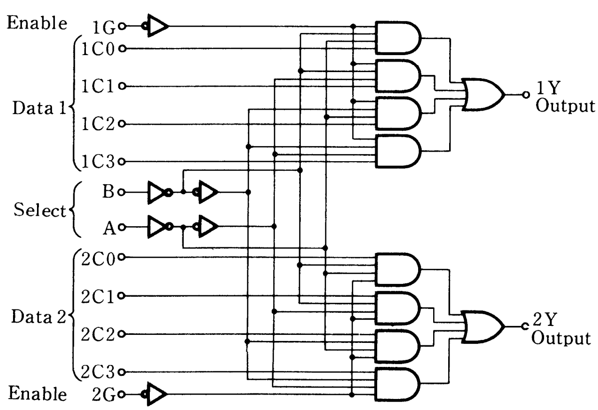
Select Inputs		Data Inputs				Enable	Output
B	A	C0	C1	C2	C3	G	Y
×	×	×	×	×	×	H	L
L	L	L	×	×	×	L	L
L	L	H	×	×	×	L	H
L	H	×	L	×	×	L	L
L	H	×	H	×	×	L	H
H	L	×	×	L	×	L	L
H	L	×	×	H	×	L	H
H	H	×	×	×	L	L	L
H	H	×	×	×	H	L	H

Note:
1. X: Either HIGH or LOW; it doesn't matter

Pin configuration (top view)



■ Logic Diagram



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■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	± 20	mA
Output parasitic diode current			I_{OK}	± 20	mA
Output current			I_O	± 25	mA
Supply current			I_{CC}, I_{GND}	± 50	mA
Storage temperature range			Tstg	$-65 \sim +150$	℃
Power dissipation	MN74HC153	Ta=$-40 \sim +60$℃	P_D	400	mW
		Ta=$+60 \sim +85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC153S	Ta=$-40 \sim +60$℃	P_D	275	mW
		Ta=$+60 \sim +85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4 \sim 6.0$	V
Input/output voltage	V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature range	T_A		$-40 \sim +85$	℃
Input rise and fall time	t_r, t_f	2.0	$0 \sim 1000$	ns
		4.5	$0 \sim 500$	ns
		6.0	$0 \sim 400$	ns

■ DC Characteristics (GND=0V)

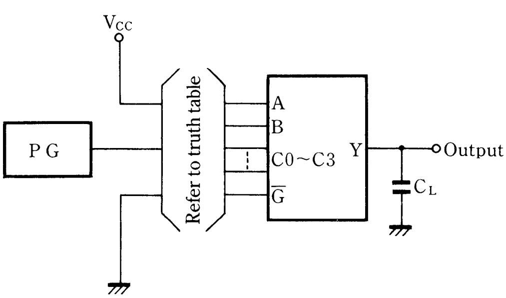
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=$-40 \sim +85$℃ min.	Ta=$-40 \sim +85$℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	-20.0	μA	1.9	2.0		1.9		V
		4.5		-20.0	μA	4.4	4.5		4.4		
		6.0		-20.0	μA	5.9	6.0		5.9		
		4.5		-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					± 0.1		± 1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

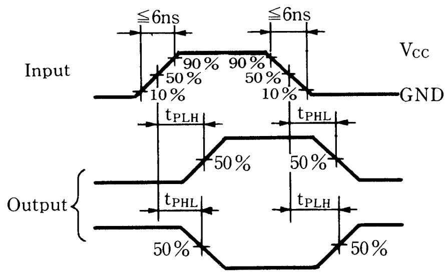
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time A, B→Y (L→H)	t_{PLH}	2.0			47	175		220	ns
		4.5			20	35		44	
		6.0			17	30		37	
Propagation time A, B→Y (H→L)	t_{PHL}	2.0			45	150		155	ns
		4.5			18	30		38	
		6.0			14	26		26	
Propagation time $\overline{G}$→Y (L→H)	t_{PLH}	2.0			38	125		155	ns
		4.5			14	25		31	
		6.0			12	21		26	
Propagation time $\overline{G}$→Y (H→L)	t_{PHL}	2.0			40	150		190	ns
		4.5			17	30		38	
		6.0			14	26		33	
Propagation time C→Y (L→H)	t_{PLH}	2.0			45	150		190	ns
		4.5			18	30		38	
		6.0			15	26		33	
Propagation time C→Y (H→L)	t_{PHL}	2.0			44	150		190	ns
		4.5			17	30		38	
		6.0			14	26		33	

- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



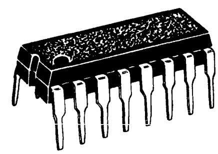
MN74HC155/MN74HC155S

Dual 2-to-4 Line Decoders/Demultiplexers

■ Description

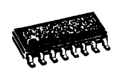
MN74HC155/MN74HC155S contain dual 2-bit 2-to-4 line decoders/demultiplexers.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS.

P-3



16-pin plastic DIL package

P-4



16-pin Panaflat package (SO-16D)

■ Truth table

2-line to 4-line Decoder/1-line to 4-line Demultiplexer

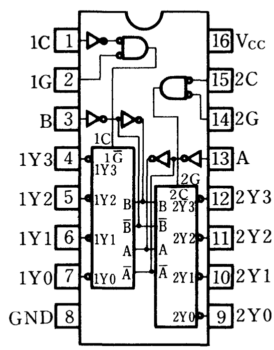
Input				Output			
Select		Enable	Data	1Y0	1Y2	1Y2	1Y3
B	A	1G	1C				
×	×	H	×	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
×	×	×	L	H	H	H	H

Input				Output			
Select		Enable	Data	2Y0	2Y1	2Y2	2Y3
B	A	2G	2C				
×	×	H	×	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
×	×	×	H	H	H	H	H

3-line to 8-line Decoder/1-line to 8-line Demultiplexer

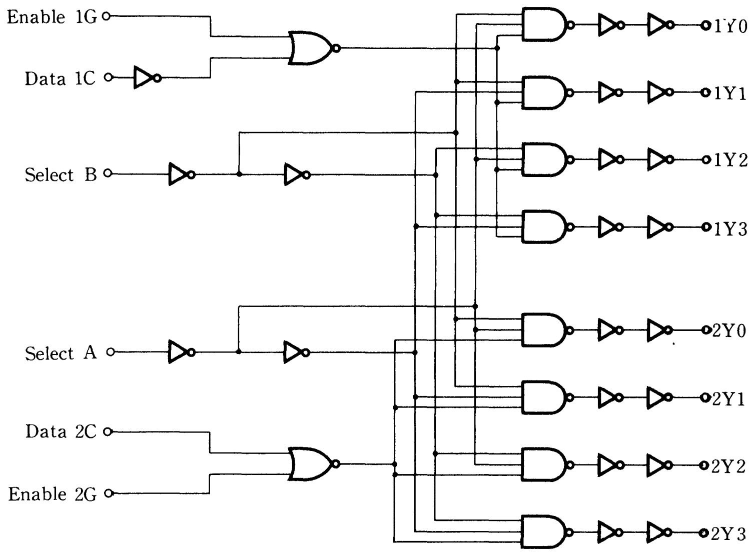
Input				Output							
Select			Enable Data	0	1	2	3	4	5	6	7
C	B	A	G	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
×	×	×	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Pin configuration (top view)



Note:
1. H: High level
2. L: Low level
3. X: Either H or L; it doesn't matter
4. C: 1C/2C inputs connected between them
5. G: 1G/2G inputs connected between them

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC155	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC155S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics

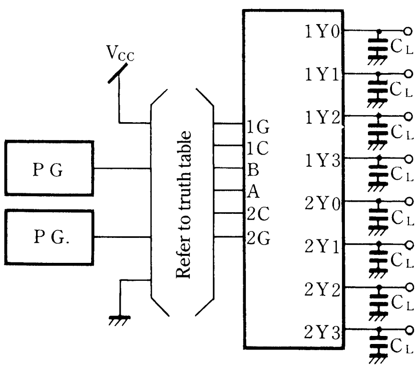
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

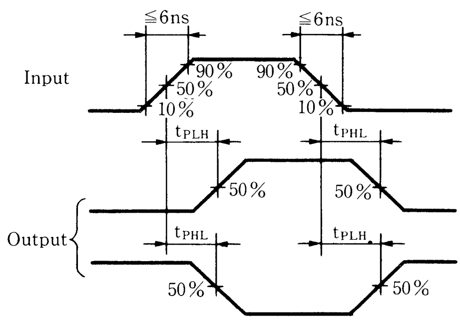
Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Propagation time A, B→Y (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time A, B→Y (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	
Propagation time 1G, 2C, 2G→Y (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time 1G, 2C, 2G→Y (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			10	25		31	
		6.0				21		26	
Propagation time 1C→Y (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
Propagation time 1C→Y (H→Y)	t_{PHL}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	

● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



MN74HC157/MN74HC157S

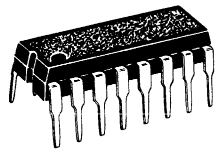
Quad 2-Input Multiplexers

■ Description

MN74HC157/MN74HC157S contain quad 2-input multiplexer circuits which select one of two data. Strobe and select inputs are common to each output of the quad circuits, all outputs become "L", 1-input data is selected from each of 2-input signals depending on the state of the select input, and is transferred to quad outputs. The selected input data is transferred to output by in-phase. Adoption of a silicon date CMOS process makes possible low power consumption, a high noise allowance, and an operation speed equivalent to LS TTL; and LS TTL 10-inputs can be directly driven.

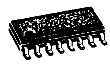
Resistors and diodes are used in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



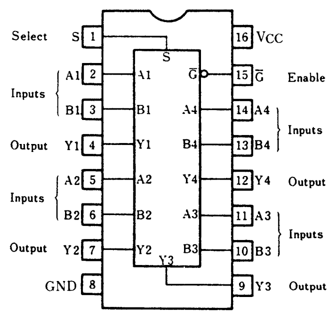
16-pin Panaflat package (SO-16D)

■ Truth Table

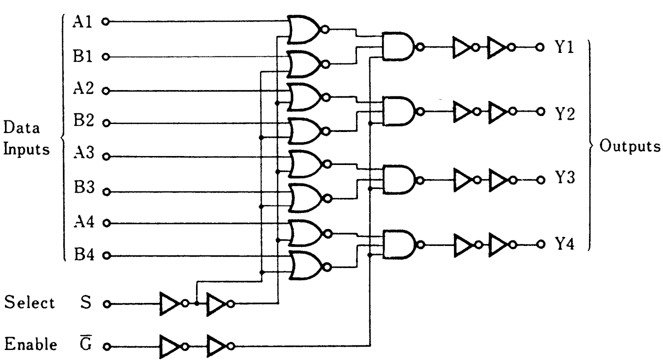
Input				Output
Strobe $\overline{G}$	Select S	A	B	Y
H	×	×	×	L
L	L	L	×	L
L	L	H	×	H
L	H	×	L	L
L	H	×	H	H

Note:
1. ×: Either HIGH or LOW; it doesn't matter

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC157	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC157S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

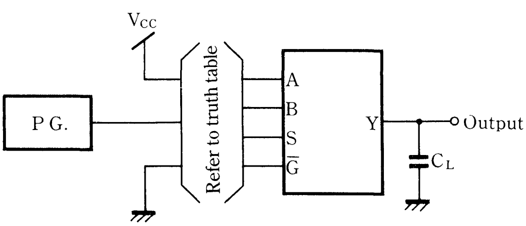
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=$-40\sim+85$℃ min.	Ta=$-40\sim+85$℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	-20.0	μA	1.9	2.0		1.9		V
		4.5		-20.0	μA	4.4	4.5		4.4		
		6.0		-20.0	μA	5.9	6.0		5.9		
		4.5		-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

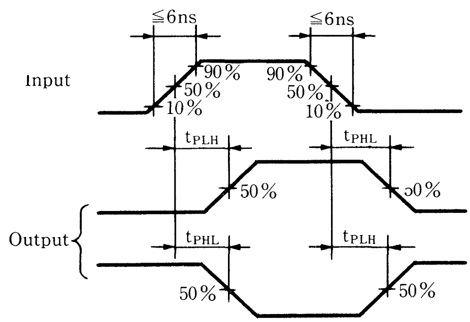
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40〜+85℃ min.	Ta=−40〜+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time A, B→Y (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
Propagation time A, B→Y (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			11	20		25	
		6.0				17		21	
Propagation time S→Y (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
Propagation time S→Y (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time $\overline{G}$→Y (L→H)	t_{PLH}	2.0				125		125	ns
		4.5			13	25		25	
		6.0				17		21	
Propagation time $\overline{G}$→Y (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			13	20		25	
		6.0				17		21	

● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



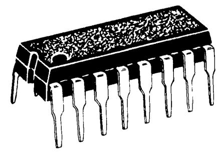
MN74HC158/MN74HC158S

Quad 2-Input Multiplexers (Inverted Output)

■ Description

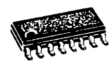
MN74HC158/MN74HC158S contain quad 2-input multiplexer circuits which select one of two data. Strobe and select input is common, and, when it is "H", all output become "H". When strobe input is "L", 1-input data is selected from each of 2-input signals depending on the state of the select input, and is transferred to each of the quad outputs. Then, the selected input data is transferred to output inverted. Adoption of a silicon date CMOS process makes possible low power consumption, a high noise allowance, and an operation speed equivalent to LS TTL; LS TTL 10-inputs can be directly driven. Resistors and diodes are used in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



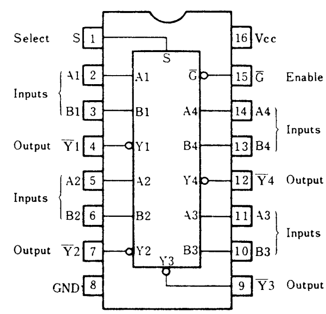
16-pin Panaflat package (SO-16D)

■ Truth Table

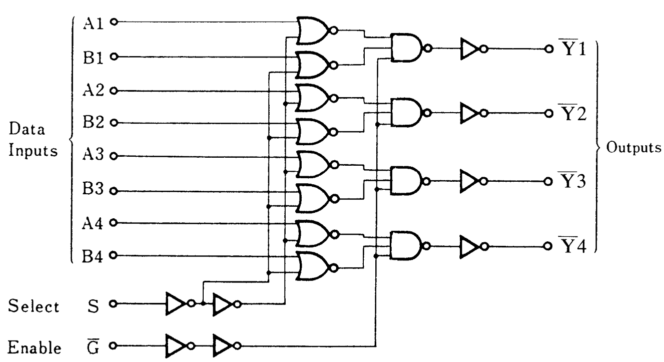
Input				Output
Strobe $\overline{G}$	Select S	A	B	$\overline{Y}$
H	×	×	×	H
L	L	L	×	H
L	L	H	×	L
L	H	×	L	H
L	H	×	H	L

Note
1 × Either HIGH or LOW, it doesn't matter

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC158	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC158S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

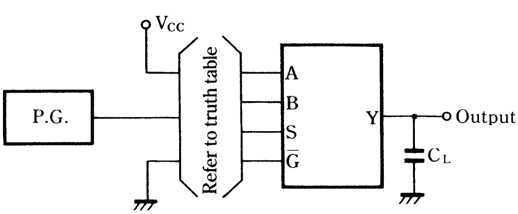
Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25℃			Ta=$-40\sim+85$℃		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	-20.0	μA	1.9	2.0		1.9		V
		4.5		-20.0	μA	4.4	4.5		4.4		
		6.0		-20.0	μA	5.9	6.0		5.9		
		4.5		-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

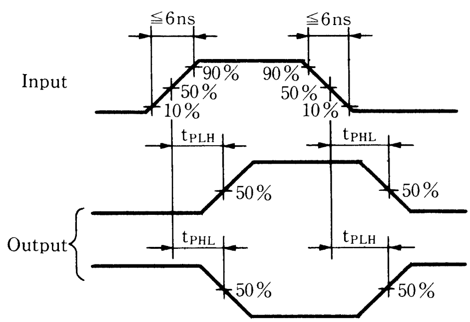
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time A, B→$\overline{Y}$ (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			11	20		25	
		6.0				17		21	
Propagation time A, B→$\overline{Y}$ (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			11	20		25	
		6.0				17		21	
Propagation time S→$\overline{Y}$ (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	
Propagation time S→$\overline{Y}$ (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			11	20		25	
		6.0				17		21	
Propagation time $\overline{G}$→$\overline{Y}$ (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time $\overline{G}$→$\overline{Y}$ (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	

- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



2. Waveforms



Panasonic

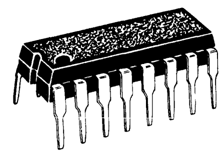
MN74HC160/MN74HC160S

Synchronous Decade Counter with Asynchronous Clear

■ Description

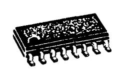
MN74HC160/MN74HC160S are pre-settable synchronous decade counters with an internal carry-look-ahead system which makes possible high-speed counter applications. Outputs of all flip-flop change at the rising edge of clock input. Since this counter is perfectly programmable, the output can be preset to both "H" and "L" by using load input. Four flip-flops are preset synchronously with the rising edge of clock input. When load input is "L", the counter stops its function, and the data corresponding with input data to be set at next clock pulse, regardless of the enable input level, appears in the output. Even if the load input becomes "H" before the rising edge of clock input, the counter doesn't operate. Clear operates asynchronously, and, when clear input is "L", it operates regardless of load or enable input level.
The carry-look-ahead circuit is used for cascade connection of an n bit synchronous counter without additional components. These junctions are performed by the enable input (ENP·ENT) of two active "HIGH" and ripple-carry (RC) outputs. When both enable inputs P and T are "H", the count can be enabled.
Ripple-carry output becomes almost the same width as output $\overline{Q}_A$ "H".
This "H" overflow ripple-carry pulse is used to enable each connected stage to cascade. Adoption of a silicon gate CMOS process makes possible low power consumption, a high noise allowance, and an operation speed equivalent to LS TTL. Resistors and diodes are used in the V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

P-3



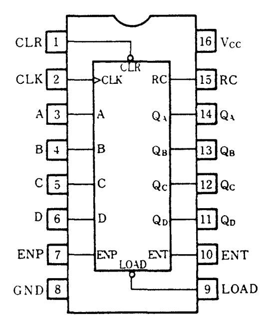
16-pin plastic DIL package

P-4



16-pin Panaflat package (SO-16D)

Pin configuration (top view)

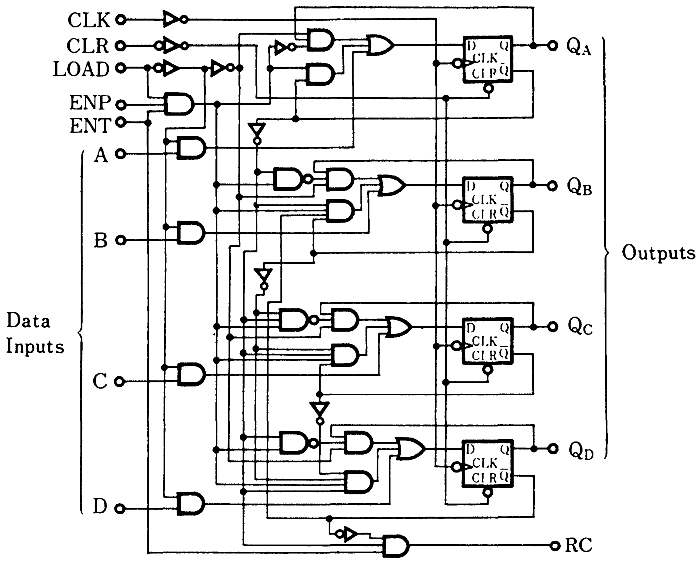


■ Truth Table

CLK	CLR	ENP	ENT	LOAD	Output
×	L	×	×	×	Clear
×	H	H	L	H	Count & RC disabled
×	H	L	H	H	Count disabled
×	H	L	L	H	Count & RC disabled
↑	H	×	×	L	Load
↑	H	H	H	H	Increment Counter

Note:
1. ↑ : When clock rises from LOW to HIGH, output increments and counts. When the load is LOW, input data is loaded.
2. ×: Either HIGH or LOW; it doesn't matter.

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC160	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC160S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	Test Conditions I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

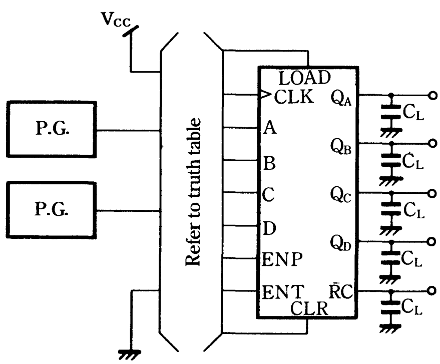
Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time CLK→Q_A~Q_D (L→H)	t_{PLH}	2.0				175		220	ns
		4.5			18	35		44	
		6.0				30		37	
Propagation time CLK→Q_A~Q_D (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			18	35		44	
		6.0				30		37	
Propagation time CLK→RC (L→H)	t_{PLH}	2.0				175		220	ns
		4.5			18	35		44	
		6.0				30		37	
Propagation time CLK→RC (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			17	35		44	
		6.0				30		37	

■ AC Characteristics (Cont'd)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Propagation time ENT→RC (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			11	25		31	
		6.0				21		26	
Propagation time ENT→RC (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	
Propagation time CLR→Q_A~Q_D (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			17	35		44	
		6.0				30		37	
Propagation time CLR→RC (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			20	35		44	
		6.0				30		37	
Minimum Set-up time LOAD	t_{su}	2.0				100		125	ns
		4.5			9	20		25	
		6.0				17		21	
Minimum Set-up time A, B, C, D	t_{su}	2.0				100		125	ns
		4.5			5	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum pulse width CLR	t_W	2.0				100		125	ns
		4.5			7	20		25	
		6.0				17		21	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5			2	15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30	71		24		
		6.0		35			28		

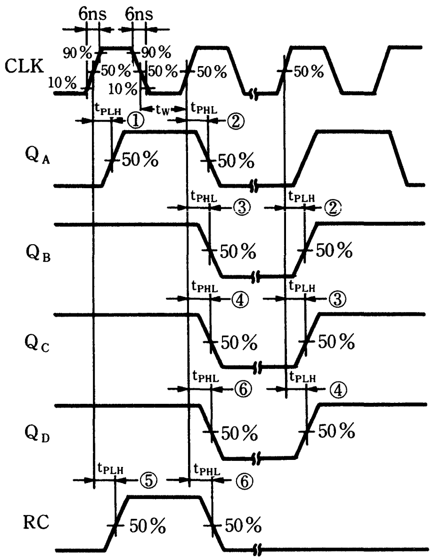
• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



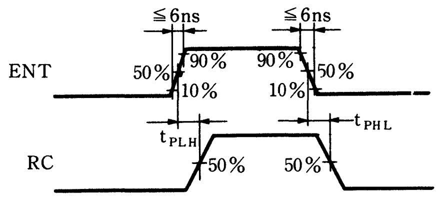
2. Waveforms

Waveforms-1 t_{PLH}, t_{PHL} (CLK→Q_A ~ Q_D, RC)

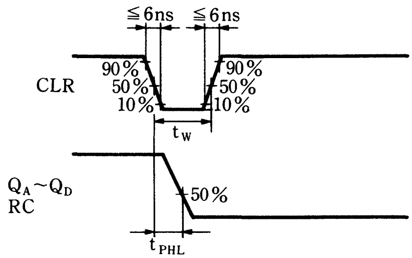


① measured when t_n+1
② measured when t_n+2
③ measured when t_n+4
④ measured when t_n+8
⑤ measured when t_n+9
⑥ measured when t_n+10

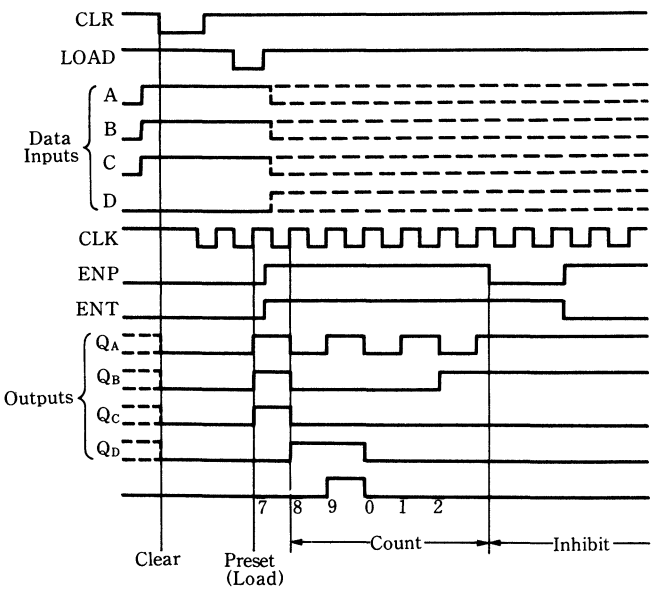
Waveforms-2 t_{PLH}, t_{PHL} (ENT→RC)



Waveforms-3 t_{PHL} (CLR→Q_A ~ Q_D, RC)



■ Timing chart



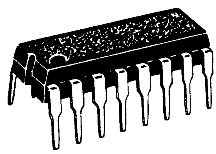
MN74HC161/MN74HC161S

Synchronous Binary Counter

■ Description

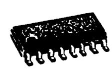
MN74HC161/MN74HC161S are presettable synchronous binary counters with an internal carry-look-ahead system which makes possible high-speed counter applications. Outputs of all flip-flops change at the rising edge of the clock input. Since this counter is perfectly programmable, the output can be preset to both "H" and "L" by utilizing the load input. Four flip-flops are preset synchronously with the rising edge of the clock input. When the load input is "L", the counter stops its function, and the data corresponding with input data to be set at the next clock pulse, regardless of the enable input level, appears in the output. Even if the load input becomes "H" before the rising edge of clock input, the counter doesn't operate. The clear function operates asynchronously, and, when clear input is "L", it operates regardless of load or enable input level. The carry-look-ahead circuit is used for cascade connection of an n bit synchronous counter without any additional components. These functions are performed by the enable input (ENP·ENT) of two active "HIGH" and ripple-carry (RC) outputs. When both enable inputs P and T are "H", the counter can be enabled. Ripple-carry-out becomes almost the same width as output $\overline{Q}_A$ "H".
This "H" overflow ripple-carry pulse is used to enable each stage connected to cascade. Adoption of a silicon gate CMOS process makes possible low power consumption, a high noise allowance and an operation speed equivalent to LS TTL. Resistors and diodes are used in the V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

P-3



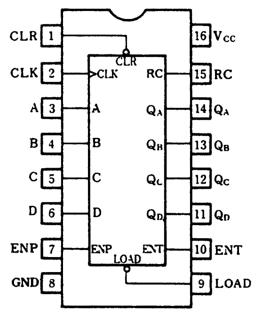
16-pin plastic DIL package

P-4



16-pin Panaflat package (SO-16D)

Pin configuration (top view)

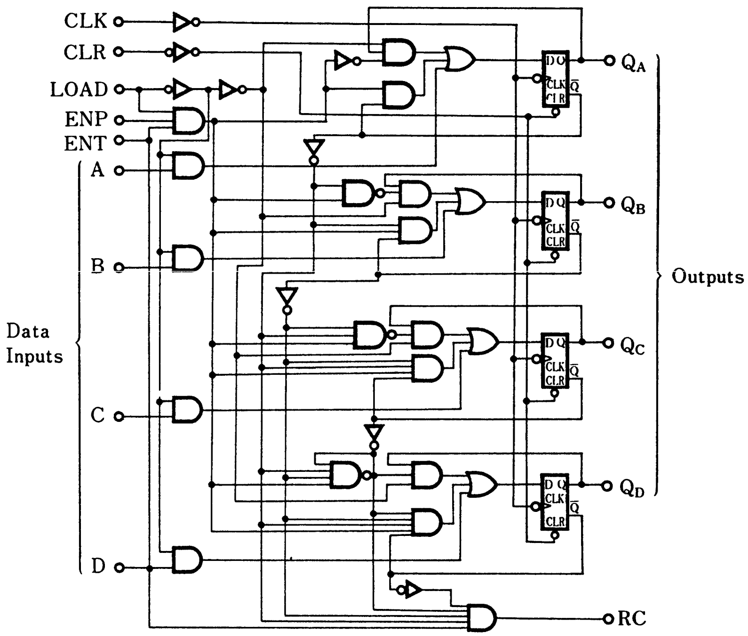


■ Truth Table

CLK	CLR	ENP	ENT	LOAD	Output
×	L	×	×	×	Clear
×	H	H	L	H	Count & RC disabled
×	H	L	H	H	Count disabled
×	H	L	L	H	Count & RC disabled
↑	H	×	×	L	Load
↑	H	H	H	H	Increment Counter

Note:
1. ↑: When clock rises from LOW to HIGH, output increments and counts. When the load is LOW, input data is loaded.
2. ×: Either HIGH or LOW; it doesn't matter.

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC161	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC161S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

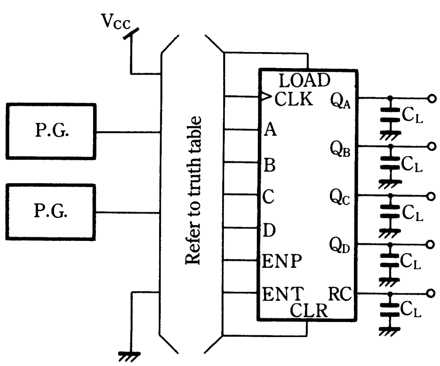
Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ts=−40~+85℃ min.	Ts=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time CLK→Q_A~Q_D (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			18	30		38	
		6.0				26		33	
Propagation time CLK→Q_A~Q_D (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			18	30		38	
		6.0				26		33	
Propagation time CLK→RC (L→H)	t_{PLH}	2.0				175		220	ns
		4.5			17	35		44	
		6.0				30		37	
Propagation time CLK→RC (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			16	35		44	
		6.0				30		37	

■ AC Characteristics (Cont'd)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Propagation time ENT→RC (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
Propagation time ENT→RC (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time CLR→Q_A~Q_D (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			16	30		38	
		6.0				26		33	
Propagation time CLR→RC (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			20	35		44	
		6.0				30		37	
Minimum Set-up time LOAD	t_{su}	2.0				100		125	ns
		4.5			10	20		25	
		6.0				17		21	
Minimum Set-up time A, B, C, D	t_{su}	2.0				100		125	ns
		4.5			5	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum pulse width $\overline{CLR}$	t_W	2.0				100		125	ns
		4.5			7	20		25	
		6.0				17		21	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5			3	15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		28	45		22		
		6.0		33			26		

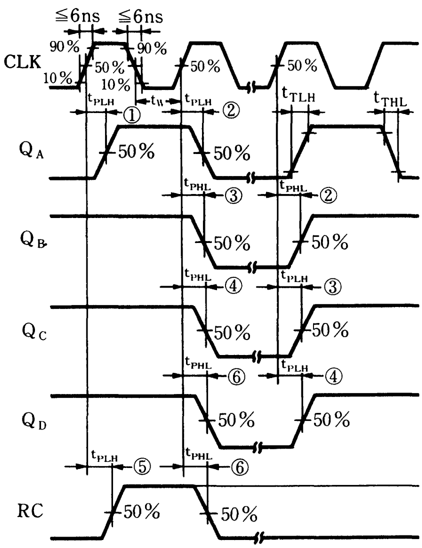
● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



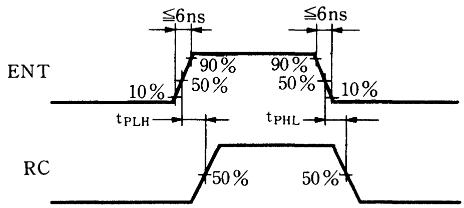
2. Waveforms

Waveforms-1 t_{PLH}, t_{PHL} (CLK→Q_A~Q_D, RC)

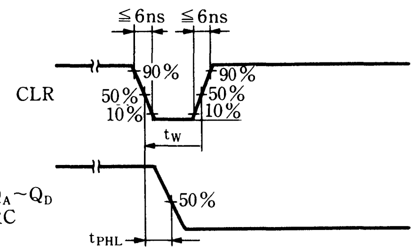


① measured when t_n+1
② measured when t_n+2
③ measured when t_n+4
④ measured when t_n+8
⑤ measured when t_n+15
⑥ measured when t_n+16

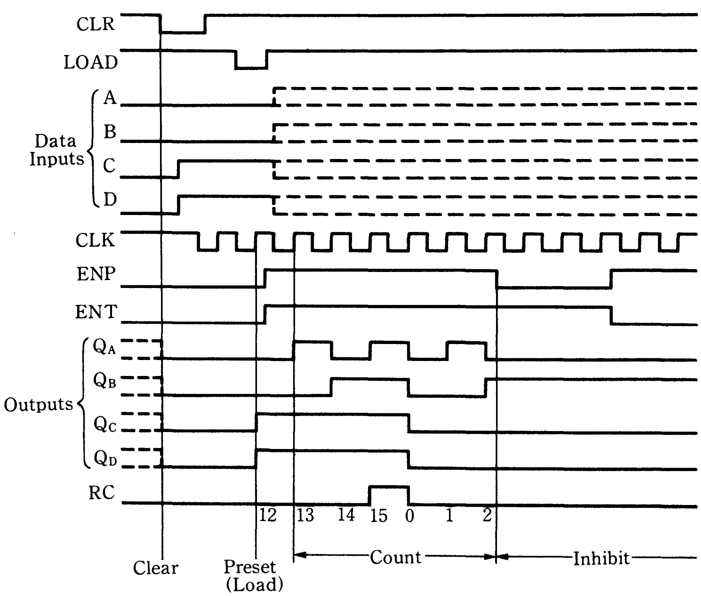
Waveforms-2 t_{PLH}, t_{PHL} (ENT→RC)



Waveforms-3 t_{PHL} (CLR→Q_A~Q_D, RC)



■ Timing chart



Panasonic

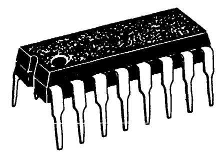
MN74HC162/MN74HC162S

Synchronous Decade Counter with Synchronous Clear

■ Description

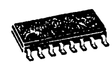
MN74HC162/MN74HC162S are presettable synchronous decade counters with an internal carry-look-ahead system which makes possible high-speed counter applications. Outputs of all flip-flops change at the rising edge of the clock input. Since this counter is perfectly programmable, the output can be preset to both "H" and "L" by utilizing the load input. Four flip-flops are preset synchronously with the rising edge of the clock input. When the load input is "L", the counter stops its function, and the data corresponding with input data to be set at the next clock pulse, regardless of the enable input level, appears in the output. Even if the load input becomes "H" before the rising edge of clock input, the counter doesn't operate. The clear function operates with clock synchronously, and, when clear input is "L", it operates on the rising edge of clock input. The carry-look-ahead circuit is used for cascade connection of an n bit synchronous counter without any additional components. These functions are performed by the enable input (ENP·ENT) of two active "HIGH" and ripple-carry (RC) outputs. When both enable inputs P and T are "H", the counter can be enabled. Ripple-carry-out becomes almost the same width as output $\overline{Q}_A$ "H".
This "H" overflow ripple-carry pulse is used to enable each stage connected to cascade. Adoption of a silicon gate CMOS process makes possible low power consumption, a high noise allowance and an operation speed equivalent to LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are used in the V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

P-3



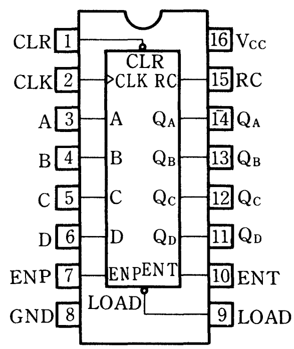
16-pin plastic DIL package

P-4



16-pin Panaflat package (SO-16D)

Pin Configuration (top view)

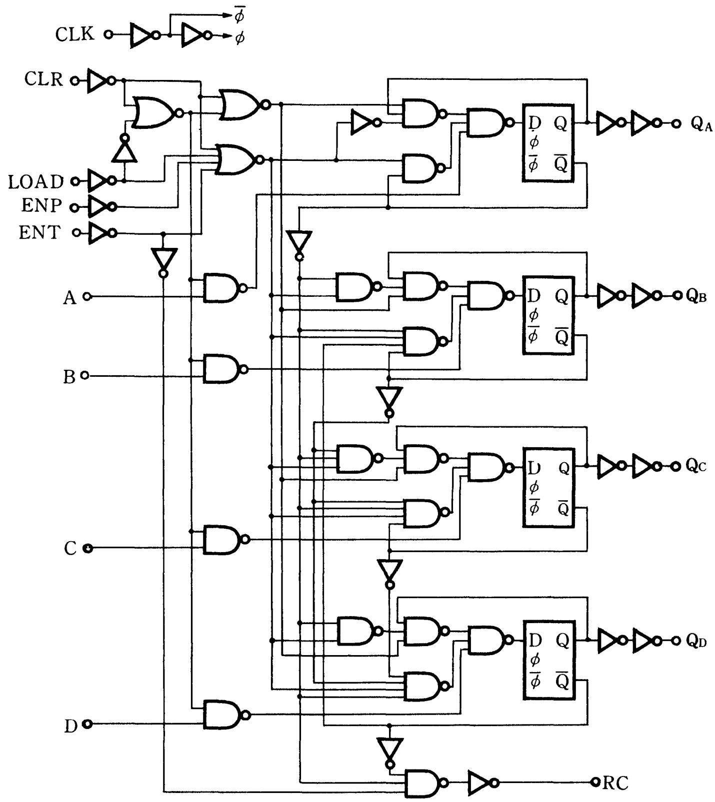


■ Truth Table

CLK	CLR	ENP	ENT	LOAD	Output
_/¯	L	×	×	×	Clear
×	H	H	L	H	Count & RC disabled
×	H	L	H	H	Count disabled
×	H	L	L	H	Count & RC disabled
_/¯	H	×	×	L	Load
_/¯	H	H	H	H	Increment Counter

Note:
1. _/¯ : When clock rises from LOW to HIGH, output increments and counts. When the load is LOW, input data is loaded.
2. × : Either HIGH or LOW; it doesn't matter

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			T_{stg}	−65～+150	℃
Power dissipation	MN74HC162	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC162S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

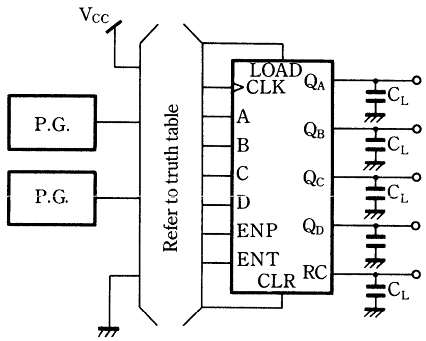
Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
E Propagation time CLK→Q_A~Q_D (L→H)	t_{PLH}	2.0	LOAD="H"			175		220	ns
		4.5			19	35		44	
		6.0				30		37	
E Propagation time CLK→Q_A~Q_D (H→L)	t_{PHL}	2.0	LOAD="H"			175		220	ns
		4.5			18	35		44	
		6.0				30		37	
E Propagation time CLK→Q_A~Q_D (L→H)	t_{PLH}	2.0	LOAD="L"			175		220	ns
		4.5			19	35		44	
		6.0				30		37	
E Propagation time CLK→Q_A~Q_D (H→L)	t_{PHL}	2.0	LOAD="L"			175		220	ns
		4.5			18	35		44	
		6.0				30		37	

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Condition Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
E Propagation time CLK→RC (L→H)	t_{PLH}	2.0				200		250	ns
		4.5			25	40		50	
		6.0				34		43	
E Propagation time CLK→RC (H→L)	t_{PHL}	2.0				200		250	ns
		4.5			23	40		50	
		6.0				34		43	
E Propagation time ENT→RC (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			15	30		38	
		6.0				26		33	
E Propagation time ENT→RC (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			17	35		44	
		6.0				30		37	
Minimum Set-up time LOAD	t_{su}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	
Minimum Set-up time A, B, C, D	t_{su}	2.0				100		125	ns
		4.5			6	20		25	
		6.0				17		21	
Minimum Set-up time CLR	t_{su}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum pulse width CLK	t_w	2.0				100		125	ns
		4.5			11	20		25	
		6.0				17		21	
Minimum recovery time	t_{rem}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
Maximum clock frequency	f_{max}	2.0		6			5		MHz
		4.5		30	56		24		
		6.0		35			28		

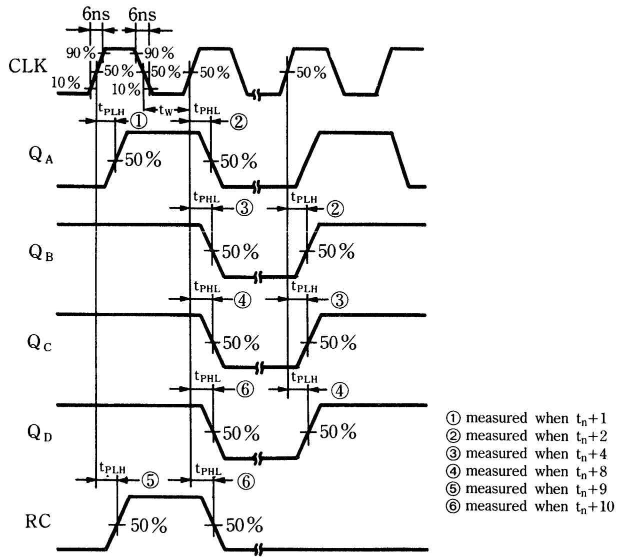
● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit

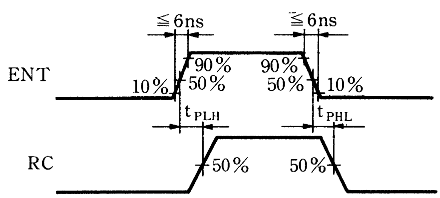


2. Waveforms

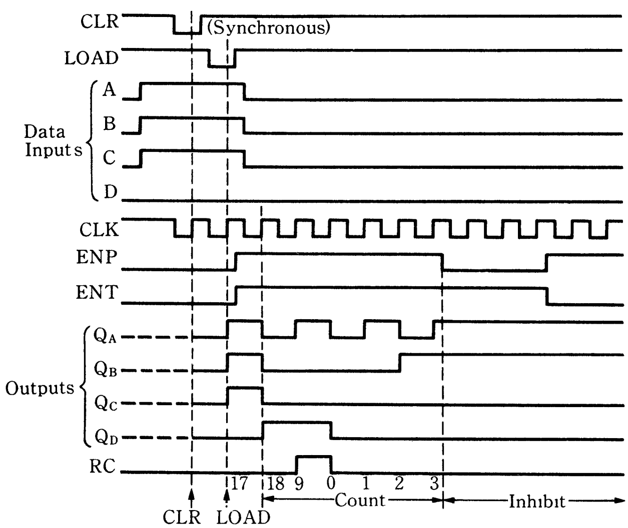
Waveforms-1 t_{PLH}, t_{PHL} (CLK→Q_A ~Q_D , RC)



Waveforms-2 t_{PLH}, t_{PHL} (ENT→RC)



■ Typical Operating Conditions



MN74HC163/MN74HC163S

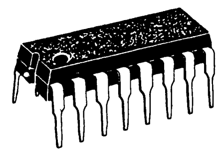
Synchronous Binary Counter with Synchronous Clear

■ Description

MN74HC163/MN74HC163S are presettable synchronous binary counters with an internal carry-look-ahead system which makes possible high-speed counter applications. Outputs of all flip-flops change at the rising edge of the clock input. Since this counter is perfectly programmable, the output can be preset to both "H" and "L" by utilizing the load input. Four flip-flops are preset synchronously with the rising edge of the clock input. When the load input is "L", the counter stops its function, and the data corresponding with input data to be set at the next clock pulse, regardless of the enable input level, appears in the output. Even if the load input becomes "H" before the rising edge of clock input, the counter doesn't operate. The clear function operates with clock synchronously, and, when clear input is "L", it operates on the rising edge of clock input. The carry-look-ahead circuit is used for cascade connection of an n bit syschronous counter without any additional components. These functions are performed by the enable input (ENP·ENT) of two active "HIGH" and ripple-carry (RC) outputs. When both enable inputs P and T are "H", the counter can be enabled. Ripple-carry-out becomes almost the same width as output $\overline{Q}_A$ "H".

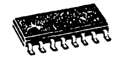
This "H" overflow ripple-carry pulse is used to enable each stage connected to cascade. Adoption of a silicon gate CMOS process makes possible low power consumption, a high noise allowance and an operation speed equivalent to LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are used in the V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

P-3



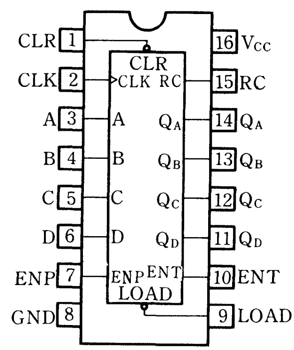
16-pin plastic DIL package

P-4



16-pin Panaflat package (SO-16D)

Pin Configuration (top view)

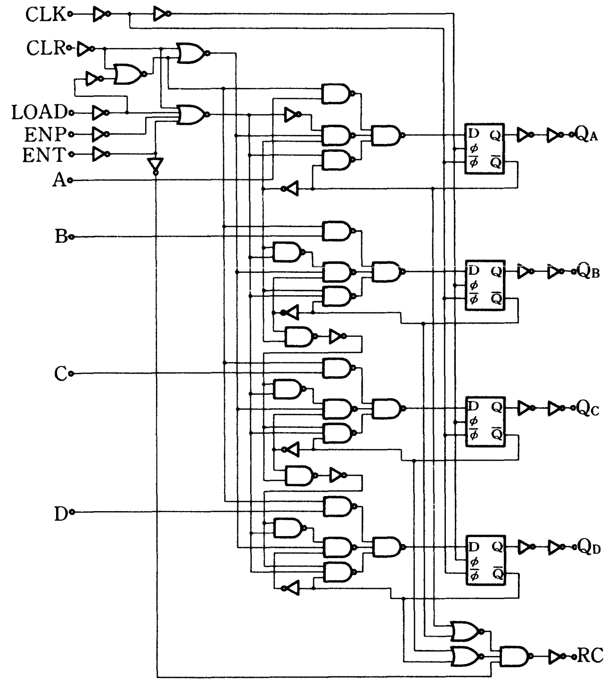


■ Truth Table

CLK	CLR	ENP	ENT	LOAD	Output
↑	L	×	×	×	Clear
×	H	H	L	H	Count & RC disabled
×	H	L	H	H	Count disabled
×	H	L	L	H	Count & RC disabled
↑	H	×	×	L	Load
↑	H	H	H	H	Increment Counter

Note:
1. : When clock rises from LOW to HIGH, output increments and counts. When the load is LOW, input data is loaded.
2. ×: Either HIGH or LOW, it doesn't matter

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	± 20	mA
Output parasitic diode current			I_{OK}	± 20	mA
Output current			I_O	± 25	mA
Supply current			I_{CC}, I_{GND}	± 50	mA
Storage temperature range			Tstg	$-65 \sim +150$	℃
Power dissipation	MN74HC163	Ta$=-40 \sim +60$℃	P_D	400	mW
		Ta$=+60 \sim +85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC163S	Ta$=-40 \sim +60$℃	P_D	275	mW
		Ta$=+60 \sim +85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4 \sim 6.0$	V
Input/output voltage	V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature range	T_A		$-40 \sim +85$	℃
Input rise and fall time	t_r, t_f	2.0	$0 \sim 1000$	ns
		4.5	$0 \sim 500$	ns
		6.0	$0 \sim 400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

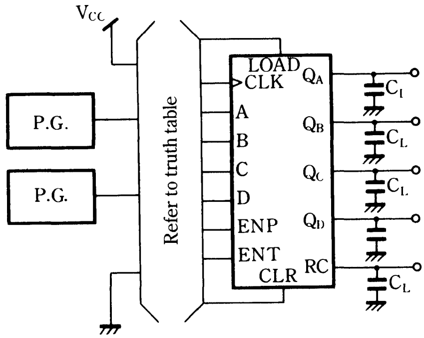
Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
E Propagation time CLK→Q_A~Q_D (L→H)	t_{PLH}	2.0	LOAD= "H"		16	150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time CLK→Q_A~Q_D (H→L)	t_{PHL}	2.0	LOAD= "H"		15	125		155	ns
		4.5				25		31	
		6.0				21		26	
E Propagation time CLK→Q_A~Q_D (L→H)	t_{PLH}	2.0	LOAD= "L"		16	150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time CLK→Q_A~Q_D (H→L)	t_{PHL}	2.0	LOAD= "L"		15	125		155	ns
		4.5				25		31	
		6.0				21		26	

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
E Propagation time CLK→RC (L→H)	t_{PLH}	2.0				200		250	ns
		4.5			24	40		50	
		6.0				34		43	
E Propagation time CLK→RC (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			20	35		44	
		6.0				30		37	
E Propagation time ENT→RC (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
E Propagation time ENT→RC (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			16	30		38	
		6.0				26		33	
Minimum Set-up time LOAD	t_{su}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
Minimum Set-up time A, B, C, D	t_{su}	2.0				100		125	ns
		4.5			6	20		25	
		6.0				17		21	
Minimum Set-up time CLR	t_{su}	2.0				100		125	ns
		4.5			11	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum CLR pulse width	t_W	2.0				150		190	ns
		4.5			16	30		38	
		6.0				26		33	
Minimum recovery time	t_{rem}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
Maximum clock frequency	f_{max}	2.0		6			5		MHz
		4.5		30	56		24		
		6.0		35			28		

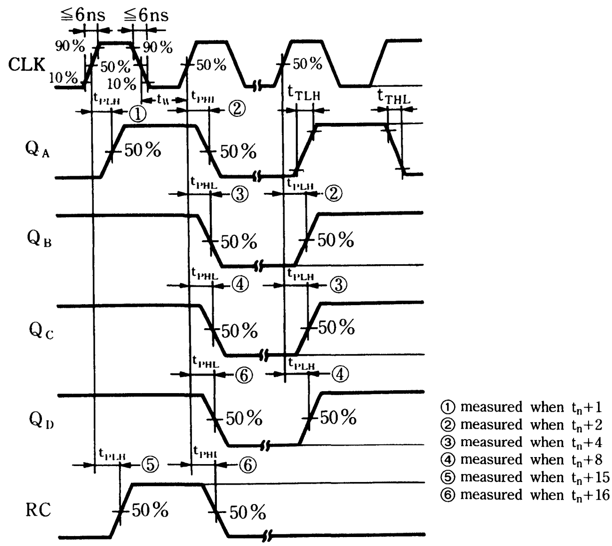
- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit

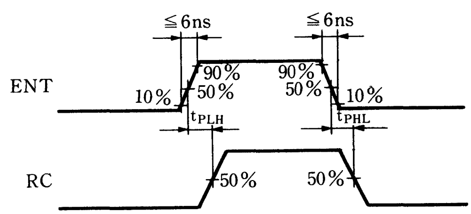


2. Waveforms

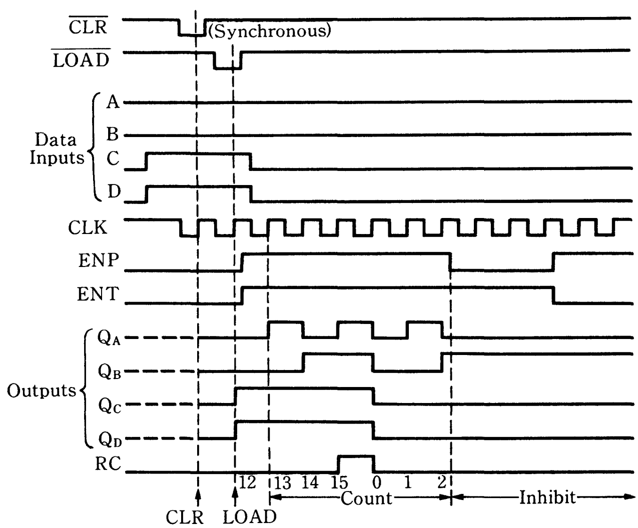
Waveforms-1 t_{PLH}, t_{PHL} (CLK→Q_A~Q_D, RC)



Waveforms-2 t_{PLH}, t_{PHL} (ENL→RC)



■ Typical Operating Conditions



MN74HC164/MN74HC164S

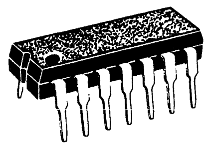
8-Bit Serial-Input Parallel-Output Shift Register

■ Description

MN74HC164/MN74HC164S is 8-bit shift registor with gated serial input and asynchronous clear input. Gated serial input (A, B) control data input. When a LOW is applied to either or both, data input stops and the initial flip-flop is reset to "L" by the next clock pulse. When one input is "H", other inputs become enabled, and data is input to the initial flip-flop by the next clock pulse. Serial input data is not input, when clock is "H" or "L". But, data satisfying the set-up conditions clock rise at all times. Clear functions, when clear input is "L" regardless of clock.

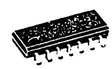
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



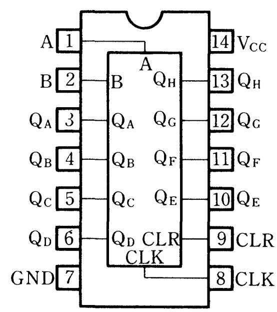
14-pin plastic DIL package

P-2



14-pin Panaflat package (SO-14D)

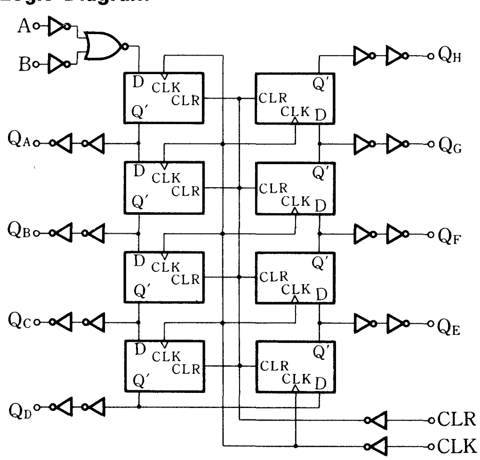
Pin Configuration (top view)



■ Truth table

Input				Output			
CLR	CLK	A	B	Q_A	Q_B	…	Q_H
L	×	×	×	L	L		L
H	L	×	×	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	×	L	Q_{An}		Q_{Gn}
H	↑	×	L	L	Q_{An}		Q_{Gn}

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC164	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC164S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

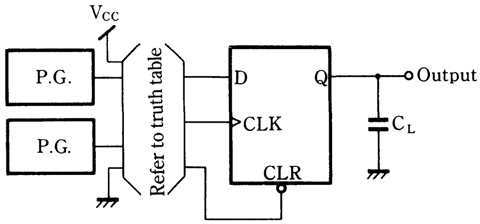
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85°C min.	Ta=−40～+85°C max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40~+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
E Propagation time CLK→Q(L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time CLK→Q(H→K)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time CLR→Q(L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time CLR→Q(H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Minimum pulse width CLR	t_W	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Hold time minimum	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30			24		
		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms

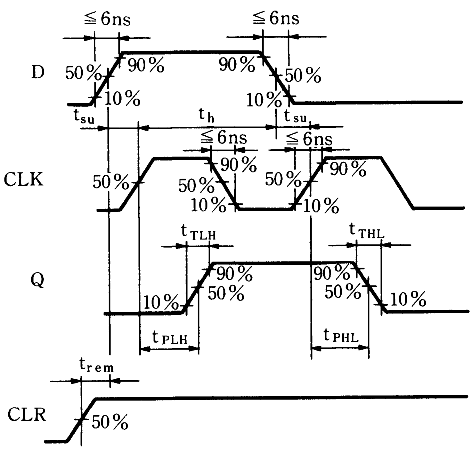
1. Measuring Circuit

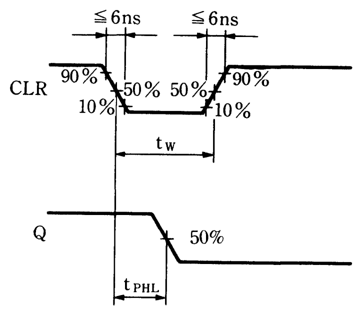


2. Waveforms

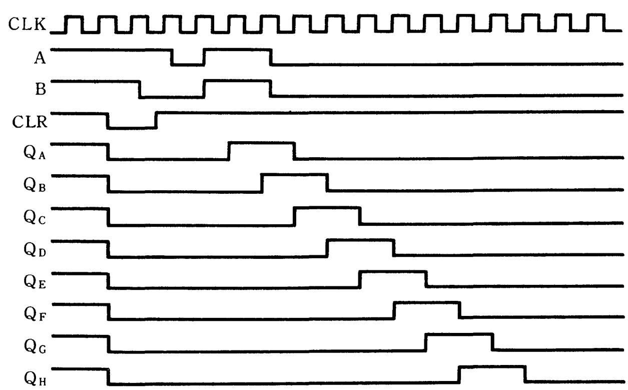
Waveforms-1 (t_{TLH}, t_{THL}, t_{PLH}/t_{PHL} (CLK→Q) t_{su}, fmax, trem, th)

Waveforms-2 (t_{PLH}/t_{PHL} (CLR→Q), t_w)





■ Typical Operating Conditions



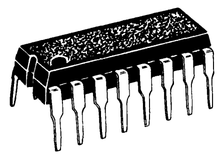
MN74HC165/MN74HC165S

8-Bit Parallel-Input Serial-Output Shift Register

■ Description

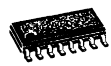
MN74HC165/MH74HC165S are high-speed 8-bit parallel-input/serial output shift registor. The data is shifted from Q_A to Q_H by the clock. Parallel input at each stages works, when shift/load input is "L". These has gated clock input and complementary output from the 8th bit. When clock inhibit input is "L", the clock generates through 2 inputs NOR gate. When one of two clock inputs is "H", the internal clock stops. When shift/load input is "H", the other clock input works, if one of two clock input is maintained at LOW. The data is transferred by the rising edge of clock pulse. Parallel loading stops as long as shift/load input is "H". When shift/load input is "L", parrallel input data is directly loaded to the registor regardless of clock.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



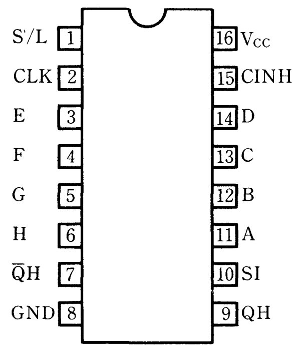
16-pin plastic DIL package

P-4

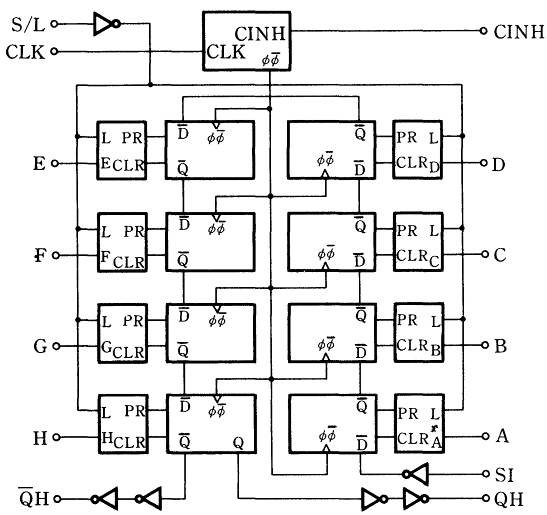


16-pin Panaflat package (SO-16D)

Pin Configuration (top view)



■ Logic Diagram



■ Truth Table

Input					Internal Stages		Output
S/L	CINH	CLK	SI	A···H	Q_A	Q_B	Q_H
L	×	×	×	a···h	a	b	h
H	L	L	×	×	Q_{AO}	Q_{BO}	Q_{HO}
H	L	↑	H	×	H	Q_{An}	Q_{Gn}
H	L	↑	L	×	L	Q_{An}	Q_{Gn}
H	H	×	×	×	Q_{AO}	Q_{BO}	Q_{HO}

■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC} +0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC165	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC165S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

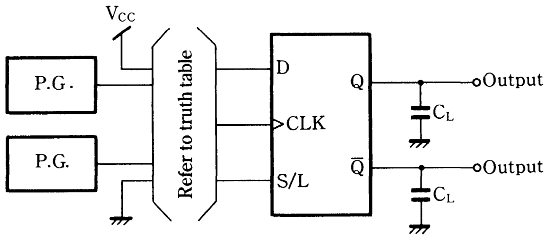
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

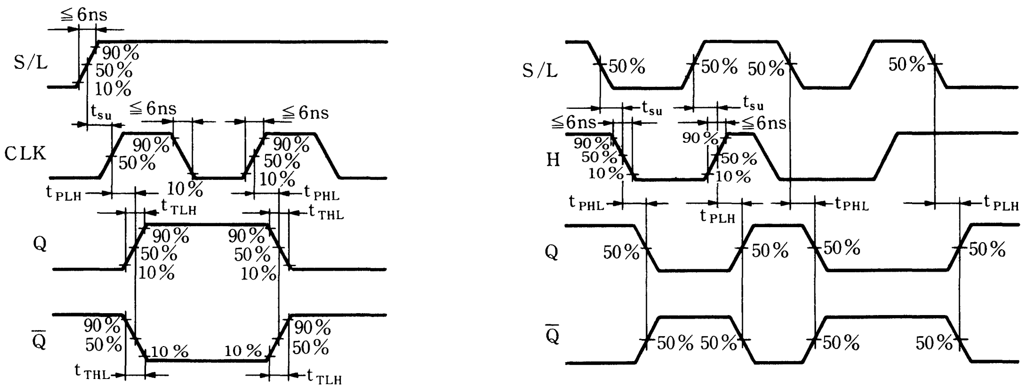
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40～+85℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
E Propagation time CLK→Q, $\overline{Q}$ (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time CLK→Q, $\overline{Q}$ (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time S/L→Q, $\overline{Q}$ (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time S/L→Q, $\overline{Q}$ (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time H→Q (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time H→Q (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time H→$\overline{Q}$ (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time H→$\overline{Q}$ (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30			24		
		6.0		35			28		

● Switching Time Measuring Circuit and Waveforms

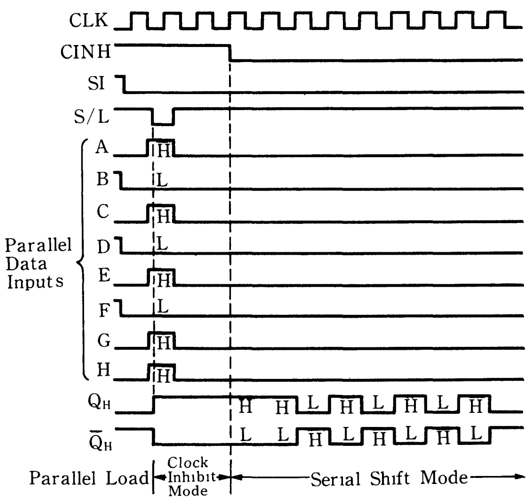
1. Measuring Circuit



2. Waveforms



■ Typical Operating Conditions



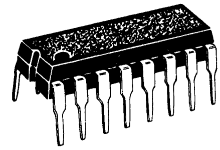
MN74HC166/MN74HC166S

Parallel-load 8-bit shift Registers

■ Description

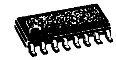
MN74HC166/MN74HC166S are high-speed, parallel-load 8-bit shift registers. The parallel-input or serial-input mode can be selected by the serial/load input.
When this input is HIGH, the serial-data input functions, and data are shifted from Q_A to Q_H by clock pulse.
When this input is LOW, however, the parallel-data input functions, and data are loaded by clock pulse.
When the input used as the clock pulse inhibit function is LOW, the internal clock pulses are generated through the two-input NOR gate.
Internal clock pulses are inhibited when either one of the clock inputs is held at HIGH. Data transmission is made at the positive going edge of the clock pulse.
A buffer has been added to the gate output, thus improving the input/output transmission characteristics; fluctuations of the transmission time resulting from increasing the load capacity are suppressed to the minimum and, Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



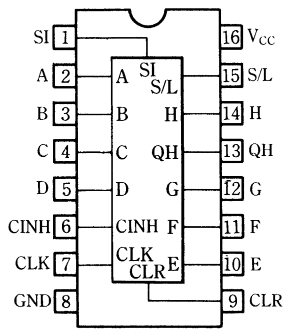
16-pin plastic DIL package

P-4



16-pin Panaflat package (SO-16D)

Pin Configuration (top view)

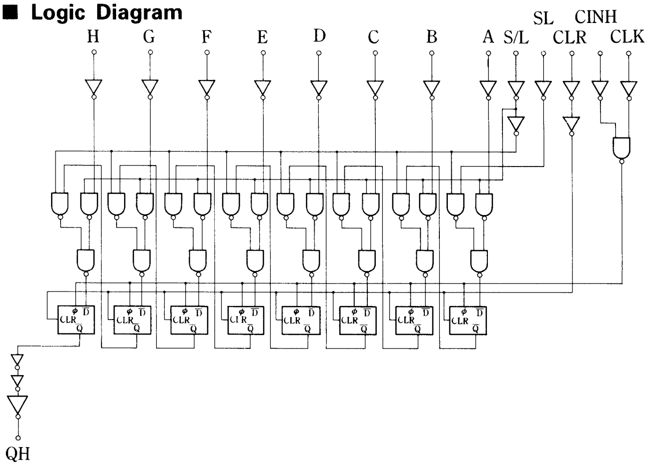


■ Truth Table

Input								Output
CLR	S/L	CINH	CLK	SI	Parallel A ...H	QA	QB	QH
L	×	×	×	×	×	L	L	L
H	×	L	L	×	×	QA0	QB0	QH0
H	L	L		×	a . h	a	b	h
H	H	L		H	×	H	QAn	QGn
H	H	L		L	×	L	QAn	QGn
H	×	H		×	×	QA0	QB0	QH0

Note: 1. ×: Either HIGH or Low; it doesn't matter

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	°C
Power dissipation	MN74HC166	Ta=−40～+60°C	PD	400	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC166S	Ta=−40～+60°C	PD	275	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	°C
Input rise and fall time	t_r, t_f	V_{CC}=2.0V	$0\sim1000$	ns
		V_{CC}=4.5V	$0\sim500$	ns
		V_{CC}=6.0V	$0\sim400$	ns

■ DC Characteristics (GND=0V)

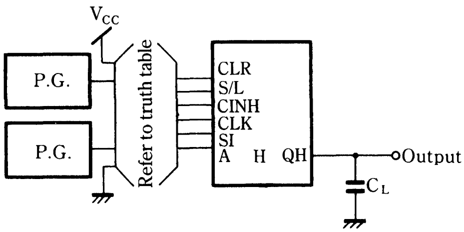
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25°C min.	typ.	max.	Ta=−40～+85°C min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		V
		6.0				4.2			4.2		V
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	V
		6.0						1.2		1.2	V
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		V
		6.0	or	−20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	−4.0	mA	3.86			3.76		V
		6.0		−5.2	mA	5.36			5.26		V
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		+1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25°C min.	typ.	max.	Ta=−40~+85°C min.	max.	Unit
Output rise time	t_{TLH}	2.0			21	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			18	65		80	ns
		4.5			7	13		16	
		6.0			6	11		14	
Propagation time CLK→QH (L→H)	t_{PLH}	2.0			53	180		225	ns
		4.5			20	36		45	
		6.0			17	31		38	
Propagation time CLK→QH (H→L)	t_{PHL}	2.0			49	175		220	ns
		4.5			19	35		44	
		6.0			16	30		37	
Propagation time CLR→QH (H→L)	t_{PHL}	2.0			49	190		240	ns
		4.5			21	38		48	
		6.0			18	32		41	
Minimum pulse width CLR	t_w	2.0			16	70		90	ns
		4.5			8	14		18	
		6.0			7	12		15	
Minimum Set-up time	t_{su}	2.0			13	100		125	ns
		4.5			3	20		25	
		6.0			2	17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	T_{rem}	2.0			5	75		95	ns
		4.5			3	15		19	
		6.0			1	13		16	
Maximum clock frequency	f_{max}	2.0		6	30		4		MHz
		4.5		30	70		24		
		6.0		35	80		28		

• Switching Time Measuring Circuit and Waveforms

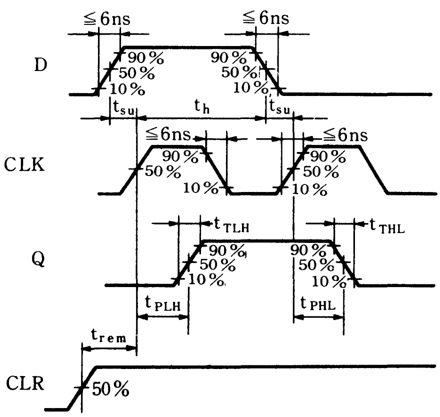
1. Measuring Circuit

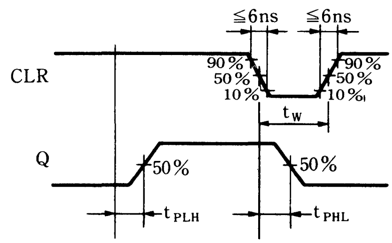


2. Waveforms

Waveforms-1 (t_{TLH}, t_{THL}, t_{su}, f_{max}, $t_{PLH}/t_{PHL}(CLK \rightarrow Q, \overline{Q})$, t_{rem}, t_h)

Waveforms-2 ($t_{PLH}/t_{PHL}(CLR \rightarrow Q, \overline{Q})$, t_W)





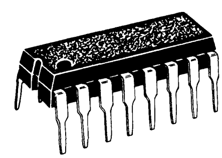
MN74HC173/MN74HC173S

Quad TRI-STATE D-Type Flip-Flops

■ Description

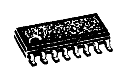
MN74HC173/MN74HC173S are TRI-STATE quad D-type flip-flops. Quad D-type flip-flops is sysnchronously operated by common clock.
When one or either of output control (M, N) become "H", output turns to be tri-state mode and become ineffective. But, it doesn't effect the continuous operation of flip-flops. When one of data enable input (G1, G2) becomes "H", output Q is trasferred to input and remain flip-flops at the same condition. Clear operates, when clear input is "H". Date output operates on the rising edge of clock.Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



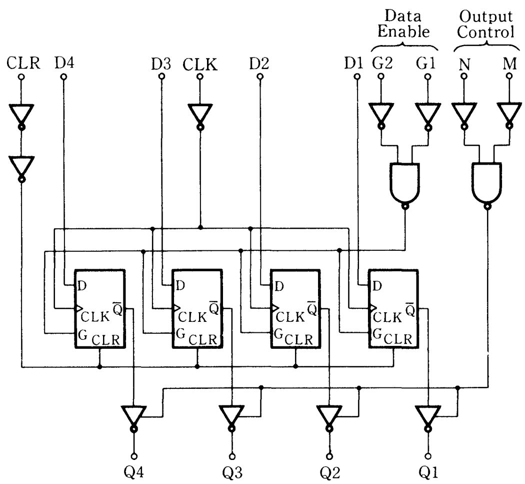
16-pin plastic DIL package

P-4

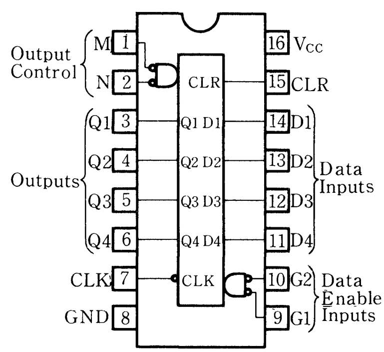


16-pin Panaflat package (SO-16D)

■ Logic Diagram



Pin configuration (top view)



■ Truth Table

Input					Output
CLR	CLK	Data Enable G1	Data Enable G2	Data D	Q
H	X	×	×	×	L
L	L	×	×	×	Q_0
L	↑	H	×	×	Q_0
L	↑	×	H	×	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ↑ : Rise of positive direction
3. Q_0: Q level prion to determination of input condition shown in table
4. When one or either of M, N is "H", output turns to high impedence and becomes ineffective. But, it doesn't effect the continous operation of flip-flops.

■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5∼+7.0	V
Input/output voltage			V_I, V_O	−0.5∼V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			T_{stg}	−65∼+150	℃
Power dissipation	MN74HC173	Ta=−40∼+60℃	P_D	400	mW
		Ta=+60∼+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC173S	Ta=−40∼+60℃	P_D	275	mW
		Ta=+60∼+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4∼6.0	V
Input/output voltage	V_I, V_O		0∼V_{CC}	V
Operating temperature range	T_A		−40∼+85	℃
Input rise and fall time	t_r, t_f	2.0	0∼1000	ns
		4.5	0∼500	ns
		6.0	0∼400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40∼+85℃ min.	Ta=−40∼+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					4.0		40.0	μA

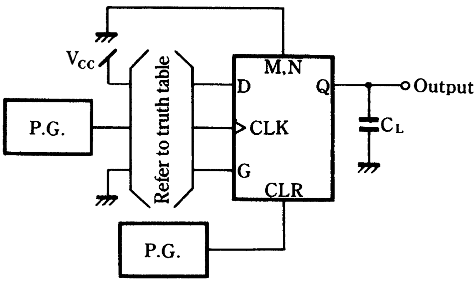
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40~+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time CLK→Q (L→H)	t_{PLH}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Propagation time CLK→Q (H→L)	t_{PHL}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Propagation time CLR→Q (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Minimum pulse width CLR	t_W	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
3-state propagation time (H→Z)	t_{PHZ}	2.0				100		125	ns
		4.5	R_L=1kΩ			20		25	
		6.0				17		21	
3-state propagation time (L→Z)	t_{PLZ}	2.0				125		155	ns
		4.5	R_L=1kΩ			25		31	
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L=1kΩ			20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				125		155	ns
		4.5	R_L=1kΩ			25		31	
		6.0				21		26	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	t_{rem}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30			24		
		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms

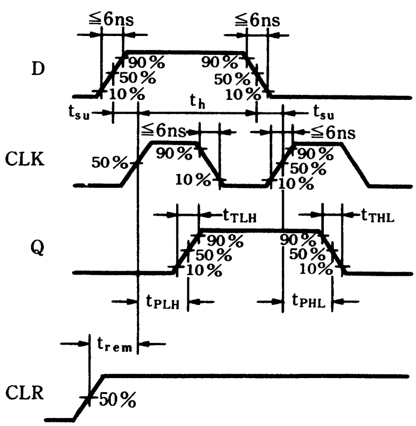
〔1〕 t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL}(CLK→Q) t_{PHL}(CLR→Q), t_W, t_{rem}, t_h

1. Measuring Circuit

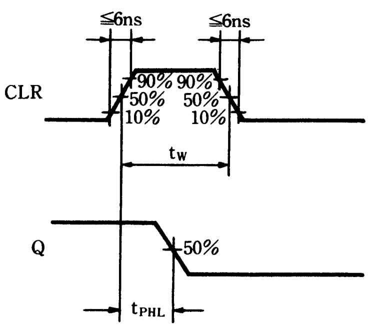


2. Switching Waveforms

Waveforms-1

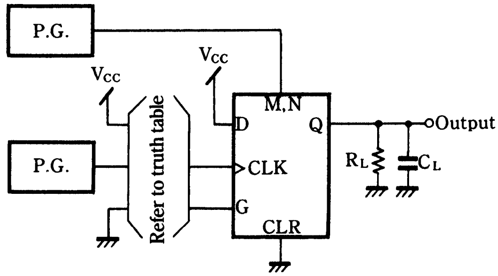


Waveforms-2

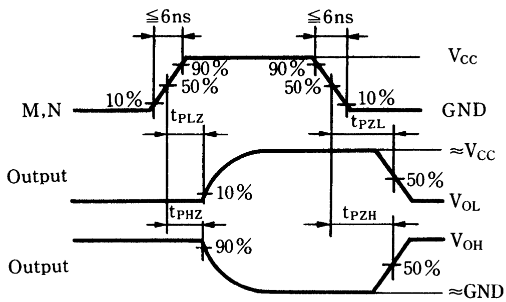


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

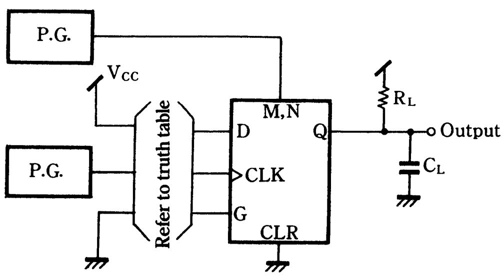


2. Switching Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Switching Waveforms

See above [2] 2. for waveforms.

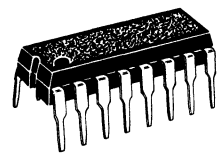
MN74HC174/MN74HC174S

Hex D-Type Flip-Flops with Clear

■ Description

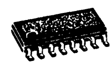
MN74HC174/MN74HC174S contain six D-type flip-flop circuits with clear in one chip, and this master/slave flip-flop has common clock and clear. D-input data to be met to set-up time is transferred to output Q at the positive going edge of the clock pulse. When the clear input is "L", all outputs are set to "L". Adoption of a silicon gate CMOS process makes possible low power consumption, a high noise allowance, and an operation speed equivalent to LS TTL; LS TTL 10-inputs can be directly driven. Resistors and diodes are used in the V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

P-3



16-pin plastic DIL package

P-4



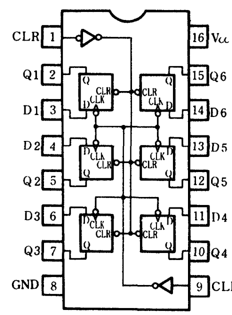
16-pin Panaflat package (SO-16D)

■ Truth Table

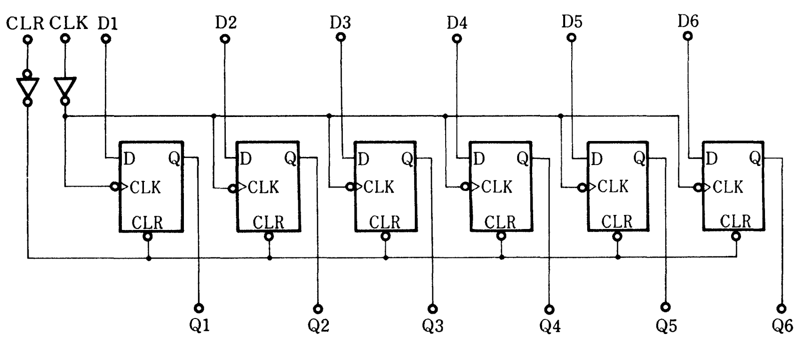
Input			Output
CLR	CLK	D	Q
L	×	×	L
H	↑	H	H
H	↑	L	L
H	L	×	Q_0

Note:
1. ↑: Data input is transferred to output on the positive going edge from LOW to HIGH of the clock
2. ×: Either HIGH or LOW; it doesn't matter
3. Q_O: Q level prior to determination of input condition shown in table

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC174	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC174S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

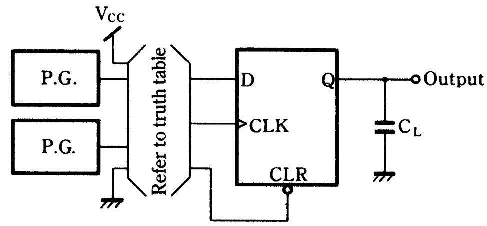
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions I_O Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40～+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time CLK→Q (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time CLK→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time CLR→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			17	25		31	
		6.0				21		26	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			2	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum pulse width CLR	t_w	2.0				100		125	ns
		4.5			8	20		25	
		6.0				17		21	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5			1	15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6	20		4		MHz
		4.5		30	68		24		
		6.0		35	70		28		

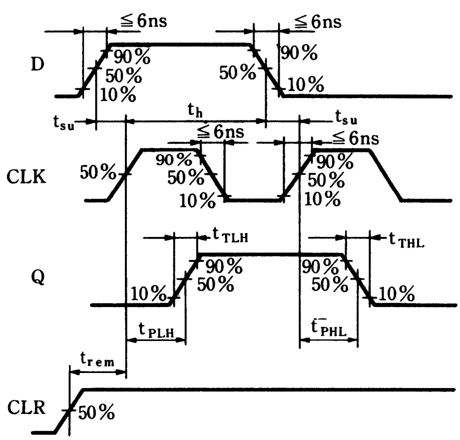
- Switching Time Measuring Circuit and Waveforms

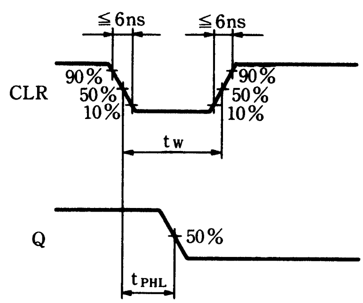
1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms

Waveforms—1 (t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL}(CLK→Q), t_{rem}, t_h) Waveforms—2 (t_{PHL}(CLR→Q), t_w)





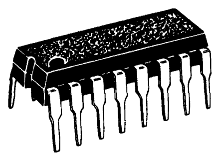
MN74HC175/MN74HC175S

Quad D-Type Flip-Flops with Clear

■ Description

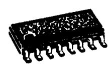
MN74HC175/MN74HC175S contain four quad D-type flip-flop circuits with clear, and this circuit has common clock and clear, and complementary outputs Q and $\overline{Q}$. D-input data is transferred to outputs Q and $\overline{Q}$ at the rising edge of the clock pulse. The output from each flip-flop circuit is a reversed phase output of the other. All flip-flops are controlled by a common clock and clear; the clear function operates when the clear input is "L", and all Q and $\overline{Q}$ outputs become "L" and "H" respectively. Adoption of the silicon gate CMOS process makes possible low power consumption and a high noise allowance; LS TTL 10-inputs can be directly driven. Resistors and diodes are used in the V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

P-3



16-pin plastic DIL package

P-4



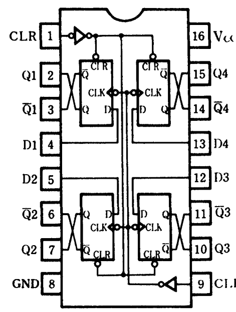
16-pin Panaflat package (SO-16D)

■ Truth Table

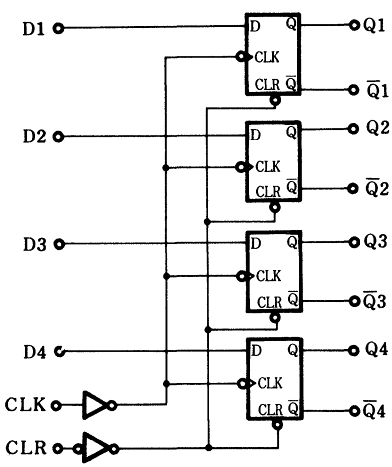
Input			Output	
CLR	CLK	D	Q	$\overline{Q}$
L	×	×	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	×	Q_0	$\overline{Q}_0$

Note:
1. ×: Data input is transferred to output on the negative-going edge from HIGH to LOW of the clock
2. ×: Either HIGH or LOW; it doesn't matter
3. Q_O: ($\overline{Q}_O$): Q ($\overline{Q}$) level prior to determination of input condition shown in table

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input/output voltage			V_I, V_O	−0.5~V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65~+150	℃
Power dissipation	MN74HC175	Ta=−40~+60℃	P_D	400	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC175S	Ta=−40~+60℃	P_D	275	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

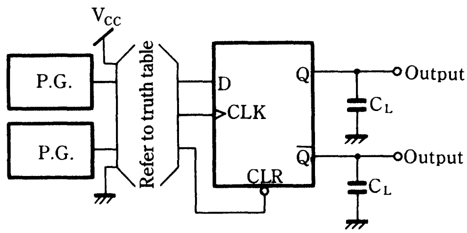
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time CLK→Q, $\overline{Q}$ (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
Propagation time CLK→Q, $\overline{Q}$ (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
Propagation time CLR→$\overline{Q}$ (L→H)	t_{PLH}	2.0				175		220	ns
		4.5			22	35		44	
		6.0				30		37	
Propagation time CLR→Q (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			3	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum pulse width CLR	t_w	2.0				100		125	ns
		4.5			8	20		25	
		6.0				17		21	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5			1	15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30	66		24		
		6.0		35			28		

● Switching Time Measuring Circuit and Waveforms

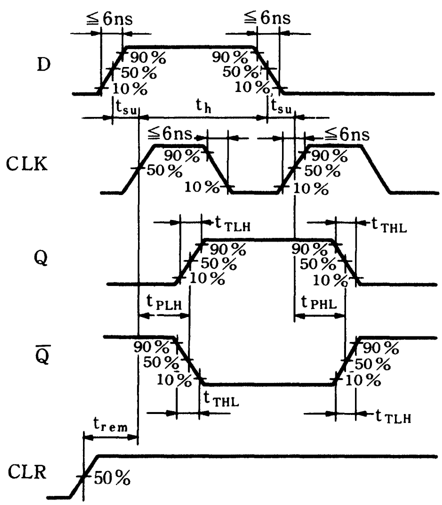
1. Measuring Circuit

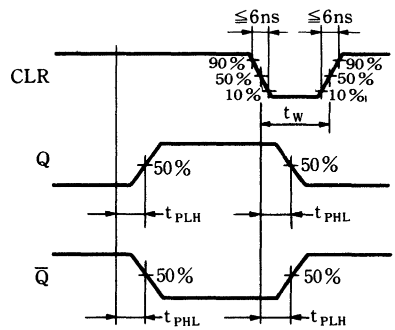


2. Waveforms

Waveforms-1 (t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL}(CLK→Q, Q̄), t_{rem}, t_h)

Waveforms-2 (t_{PLH}/t_{PHL}(CLR→Q, Q̄), t_W)





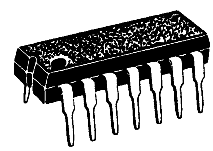
MN74HC183/MN74HC183S

Dual Carry-Save Full Adders

■ Description

MN74HC183/MN74HC183S are dual carry-save full adders. Σ output is obtained by the sum of each bit, and the digit-carry signal from the 2nd bit's output is obtained in Cn+1 output.
Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P- 1



14-pin plastic DIL package

P- 2

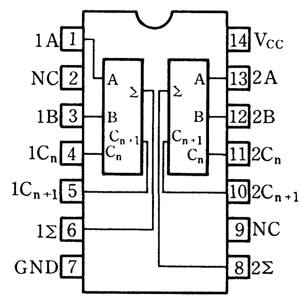
14-pin Panaflat package (SO-14D)

■ Truth Table

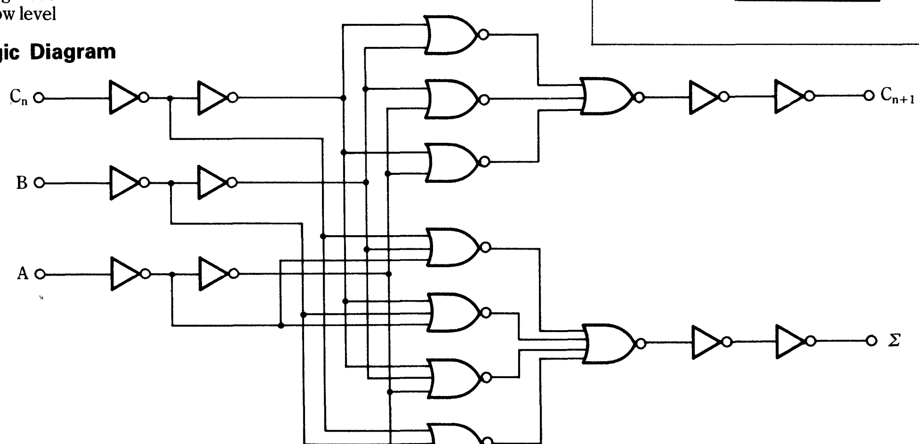
Input			Output	
C_n	B	A	Σ	C_{n+1}
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Note:
1. H: High level
2. L: Low level

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input/output voltage			V_I, V_O	−0.5~V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65~+150	°C
Power dissipation	MN74HC183	Ta=−40~+60°C	PD	400	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC183S	Ta=−40~+60°C	PD	275	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	°C
Input rise and fall time	t_4, t_f	V_{CC}=2.0V	0~1000	ns
		V_{CC}=4.5V	0~500	ns
		V_{CC}=6.0V	0~400	ns

■ DC Characteristics (GND=0V)

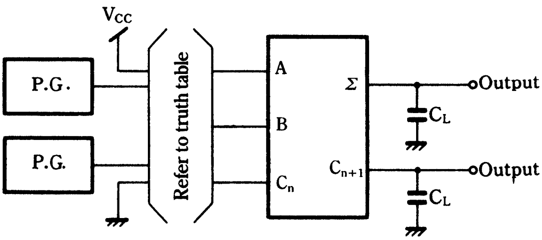
Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25°C			Ta=−40~+85°C		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		V
		6.0				4.2			4.2		V
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	V
		6.0						1.2		1.2	V
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		V
		6.0	or	−20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	−4.0	mA	3.86			3.76		V
		6.0		−5.2	mA	5.36			5.26		V
Output LOW votlage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, IO=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

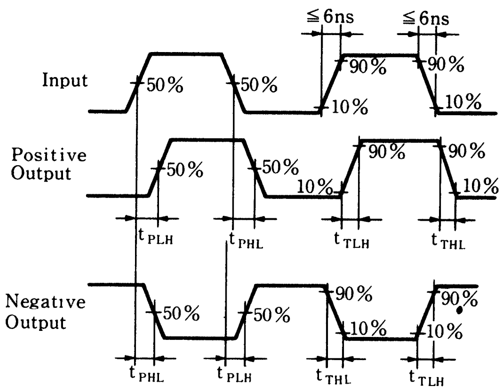
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25°C			Ta=−40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Propagation time A, B, Cn→Σ, Cn+1 (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Propagation time A, B, Cn→Σ, Cn+1 (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	

● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



2. Waveforms



MN74HC194/MN74HC194S

4-Bit Bidirectional Universal Shift Register

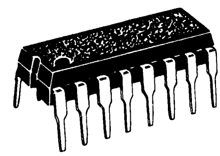
■ Description

MN74HC194/MH74HC194S is bidirectional shift register composed of parallel input, parallel output, right shift/left shift serial input, operating mode control, and direct clear input.

This register has four operating mode: parallel load, right shift (from Q_A to Q_D), left shift (from Q_D to Q_A), and clock stop. Synchronized parallel load is executed by applying four-bit data to the parallel input, when both mode control inputs S0 and S1 is "H". Data is loaded to the respective flip-flops, and transferred to the output on the rising edge of the clock. The serial shift stops during parallel loading. Right shift synchronizes with the clock pulse rise, when mode control input S0 is "H" and S1 is "L". When S0 is "L" and S1 is "H", left shift is executed by applying new data to the left shift serial input. The flip-flop clock stops when both mode control inputs are "L". Mode control input changes only when clock input is "H".

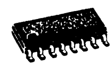
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



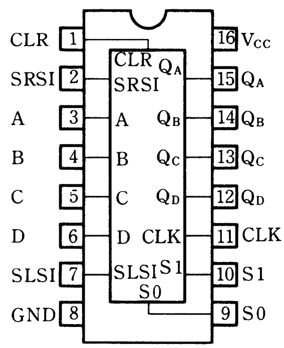
16-pin plastic DIL package

P-4



16-pin Panaflat package (SO-16D)

Pin Configuration (top view)

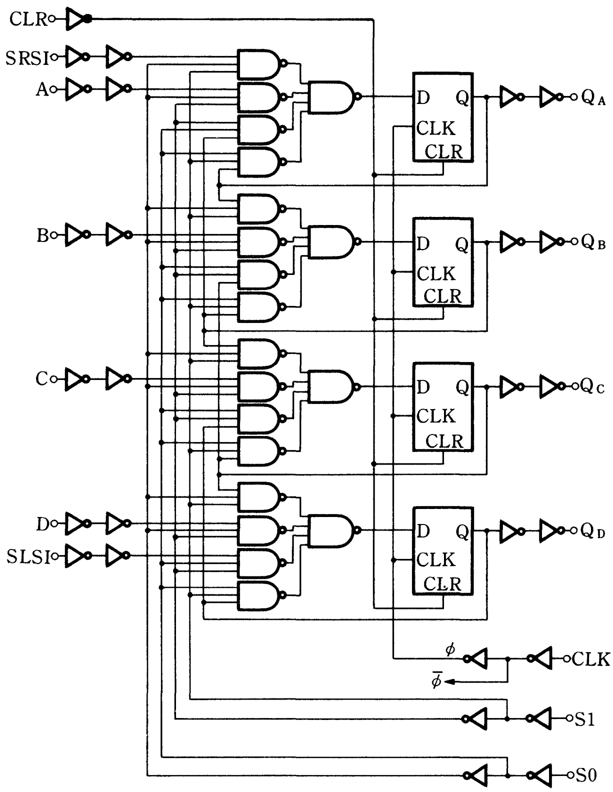


■ Truth Table

Input										Output			
CLR	Mode		CLK	SLSI	SRSI	Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0				A	B	C	D				
L	×	×	×	×	×	×	×	×	×	L	L	L	L
H	×	×	L	×	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	×	×	a	b	c	d	a	b	c	d
H	L	H	↑	×	H	×	×	×	×	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	×	L	×	×	×	×	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	×	×	×	×	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	×	×	×	×	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	×	×	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

Note: 1. H: HIGH 2. L: LOW 3. ×: Either H or L, it doesn't matter
4. ↑ : Rise from "L" to "H" 5. a, b, c, d: Input level of A, B, C, D on the normal condition
6. Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}: Q_A, Q_B, Q_C, Q_D level prion to the determination of input conditions shown in table.
7. Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}: Q_A, Q_B, Q_C, Q_D level before trasmition

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	± 20	mA
Output parasitic diode current			I_{OK}	± 20	mA
Output current			I_O	± 25	mA
Supply current			I_{CC}, I_{GND}	± 50	mA
Storage temperature range			Tstg	$-65 \sim +150$	℃
Power dissipation	MN74HC194	Ta=$-40 \sim +60$℃	P_D	400	mW
		Ta=$+60 \sim +85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC194S	Ta=$-40 \sim +60$℃	P_D	275	mW
		Ta=$+60 \sim +85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4 \sim 6.0$	V
Input/output voltage	V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature range	T_A		$-40 \sim +85$	℃
Input rise and fall time	t_r, t_f	2.0	$0 \sim 1000$	ns
		4.5	$0 \sim 500$	ns
		6.0	$0 \sim 400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

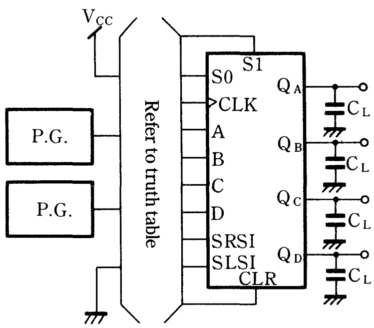
Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time CLK→Q (L→H)	t_{PLH}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	
Propagation time CLK→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	
Propagation time CLR→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	
Minimum pulse width CLK, CLR	t_W	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	

■ AC Characteristics (Cont'd)

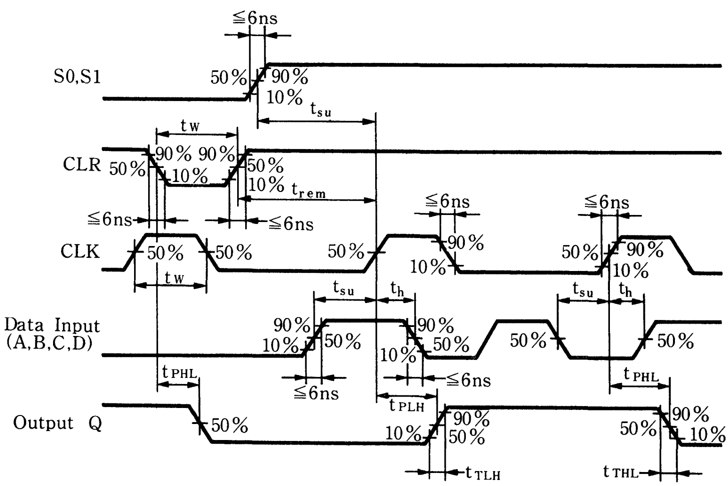
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40∼+85℃ min.	max.	Unit
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	t_{rem}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30			24		
		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms

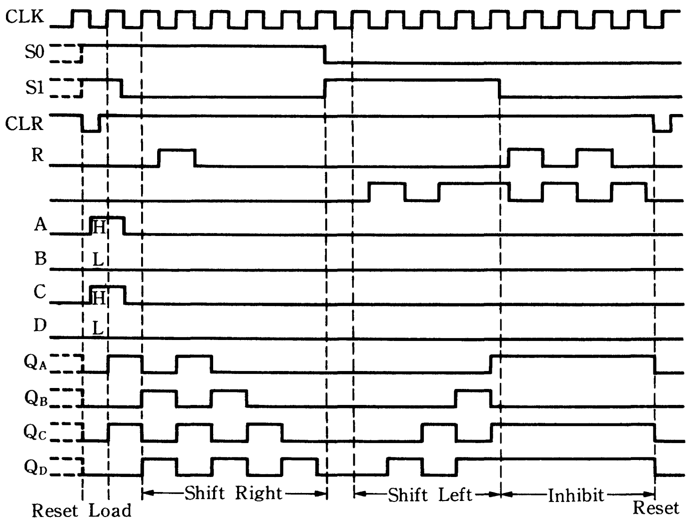
1. Measuring Circuit



2. Switching Waveforms



■ Typical Operating Conditions



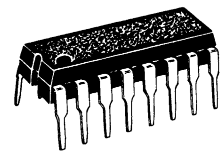
MN74HC195/MN74HC195S

4-Bit Parallel Shift Register

■ Description

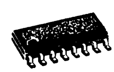
MN74HC195/MH74HC195S are four-bit parallel shift registers composed of parallel input, parallel output, J-$\overline{K}$ serial input, shift/load control input, and direct clear input. This shift register operates in two modes, parallel load and Q_A to Q_D. Parallel loading is executedy putting in four-bit data to a parallel input, and setting "L" to the shift/load control input. Data is loaded to the respective flip-flop; output appears on the rising edge of clock pulse. The serial shift function stops between parallel loads. Serial shift is executed by the rising edge of clock pulse, when shift/load control input is "H" and data is input to the J-$\overline{K}$.
As shown in the truth table, the first stage represents to function as a J-$\overline{K}$, D, or toggle flip-flop.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



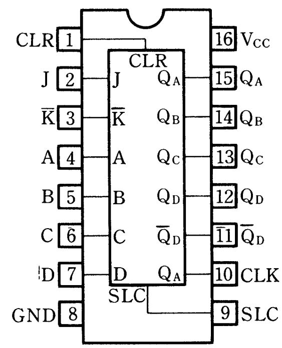
16-pin plastic DIL package

P-4



16-pin Panaflat package (SO-16D)

Pin Configuration (top view)

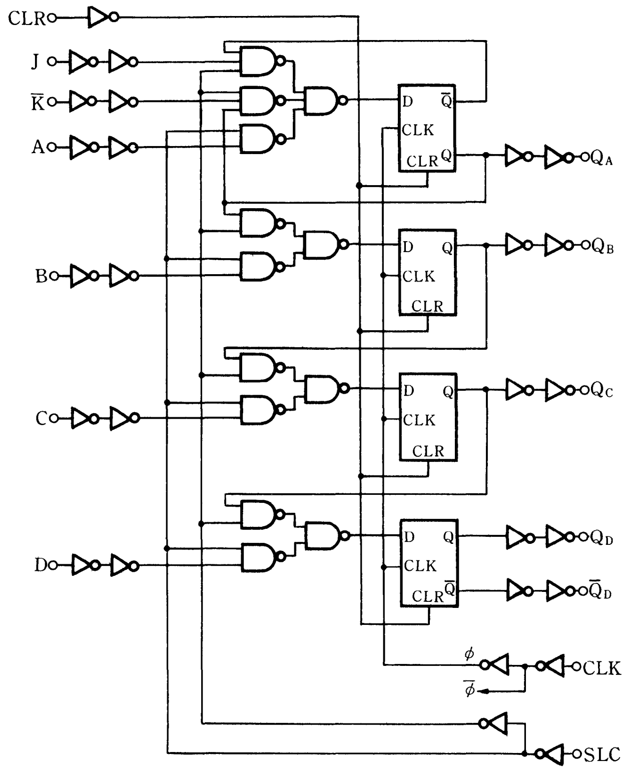


■ Truth Table

Input									Output				
CLR	SLC	CLK	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	×	×	×	×	×	×	×	×	L	L	L	L	H
H	L	↑	×	×	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	×	×	×	×	×	×	Q_{Ao}	Q_{Bo}	Q_{Co}	Q_{Do}	$\overline{Q}_{Do}$
H	H	↑	L	H	×	×	×	×	Q_{Ao}	Q_{Ao}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	×	×	×	×	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	×	×	×	×	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	×	×	×	×	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Note: 1. H: HIGH 2. L: LOW 3. ×: Either H or L, it doesn't matter
4. ↑ : Rise from "L" to "H" 5. a, b, c, d: Input level of A, B, C, D on the normal condition
6. Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}: Q_A, Q_B, Q_C, Q_D level prion to the determination of input conditions shown in table.
7. Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}: Q_A, Q_B, Q_C, Q_D level before trasmition

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC195	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC195S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		2.0	0.1		0.1	V
		4.5		20.0	μA		4.5	0.1		0.1	
		6.0		20.0	μA		6.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

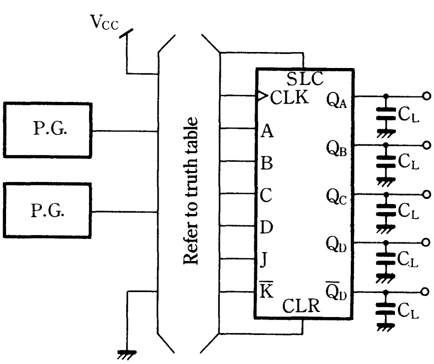
Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
E Propagation time CLK→Q (L→H)	t_{PLH}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	
E Propagation time CLK→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	
E Propagation time CLK→$\overline{Q}$ (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time CLK→$\overline{Q}$ (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
E Propagation time CLR→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	

■ AC/Characteristics (Cont'd)

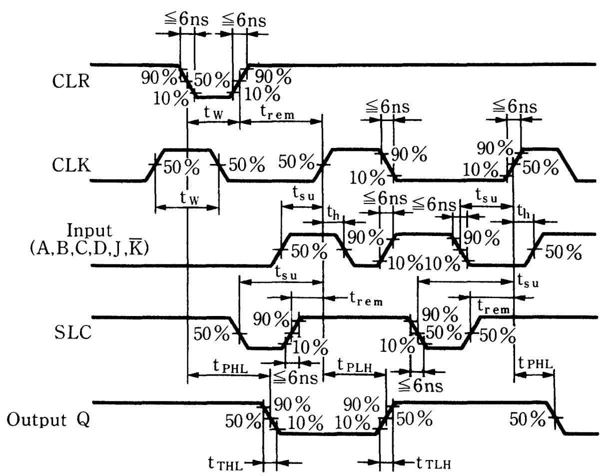
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40〜+85℃ min.	Ta=−40〜+85℃ max.	Unit
Minimum pulse width CLK, CLR	t_W	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30			24		
		6.0		35			28		

• Switching Time Measuring Circuit and Waveforms

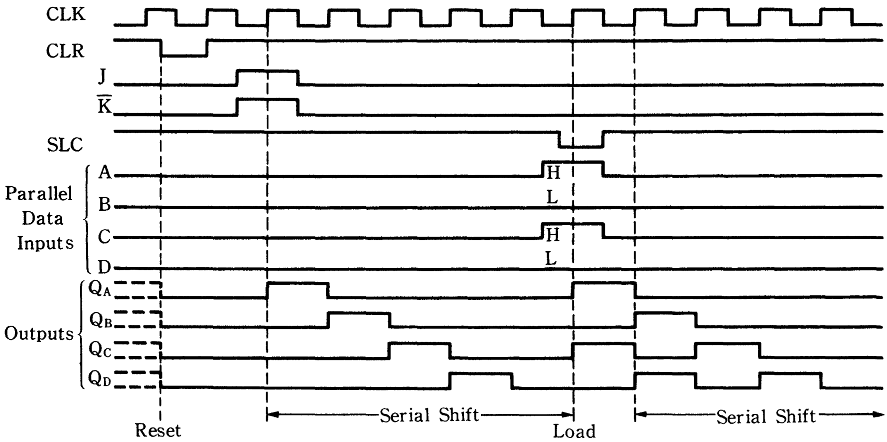
1. Measuring Circuit



2. Waveforms



■ Typical Operating Conditions



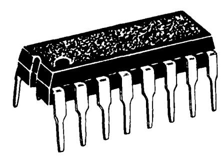
MN74HC221/MN74HC221S

Dual Monostable Multivibrators with Clear

■ Description

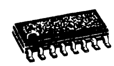
MN74HC221/MN74HC221S are dual monostable multivibrator. Trigger input is triggered on falling edge of A input and rising edge of B input/CLR input. Once input is triggered, the monostable mode is sustained by a resitor and capacitor mounted externally, unless CLR input is "L".
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



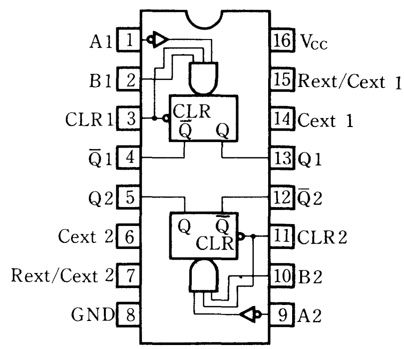
16-pin Panaflat package (SO-16D)

■ Truth Table

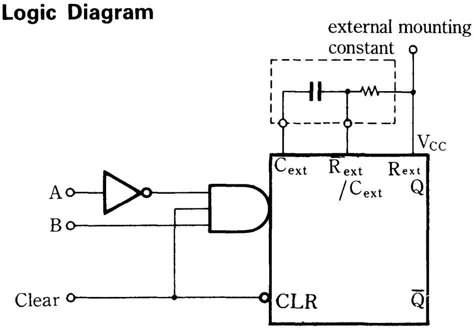
Input			Output	
CLEAR	A	B	Q	$\overline{Q}$
L	×	×	L	H
×	H	×	L	H
×	×	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

Note:
H : High level
L : Low level
X : Either H or L, it doesn't matter
↓ : fall from H to L
↑ : use from L to H
⊓ : one High level pulse
⊔ : one Low level pulse

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC221	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC221S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		2.0～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time A, CLR	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns
external timing resistance	Rext		5～1000	kΩ
external timing capacitance	Cext		no limit	pF
wiring capacitance	Rext/Cext		0～50	pF

■ DC Characteristics (GND=0V)

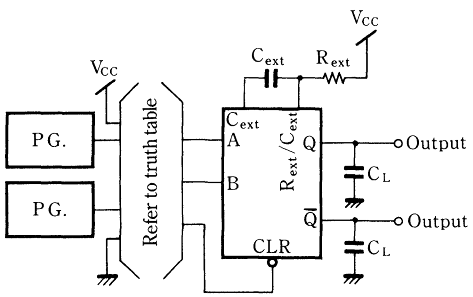
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		− 4.0	mA	3.86			3.76		
		6.0		− 5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Rext/Cext pin leak current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

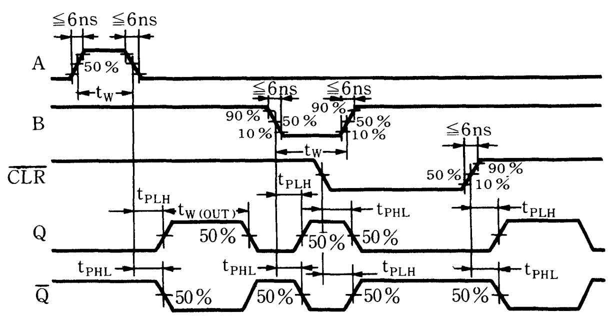
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40~+80℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0			27	75		95	ns
		4.5			10	15		19	
		6.0			8	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			8	15		19	
		6.0			6	13		16	
Propagation time A,B,CLR→Q,(L→H)	t_{PLH}	2.0			76	250		315	ns
		4.5			28	50		63	
		6.0			20	43		54	
Propagation time A,B,CLR→$\overline{Q}$,(H→L)	t_{PHL}	2.0			83	250		315	ns
		4.5			29	50		63	
		6.0			22	43		54	
Propagation time CLR→Q, $\overline{Q}$ (L→H)	t_{PLH}	2.0			47	150		190	ns
		4.5			16	30		38	
		6.0			15	26		33	
Propagation time CLR→Q, $\overline{Q}$ (H→L)	t_{PHL}	2.0			44	150		190	ns
		4.5			16	30		38	
		6.0			15	26		33	
Propagation time	$t_{W(OUT)}$	2.0	Cext=0 Rext=5kΩ		—				ns
		4.5			78				
		6.0			—				
Propagation time	$t_{W(OUT)}$	2.0	Cext=1000pF Rext=10kΩ		—				μs
		4.5			4.8				
		6.0			—				
Minimum pulse width A, B	$t_{W(IN)}$	2.0				100		125	ns
		4.5			9	20		25	
		6.0				34		21	
Minimum pulse width CLR	$t_{W(IN)}$	2.0				200		250	ns
		4.5			21	40		50	
		6.0				34		43	

● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



2. Waveforms



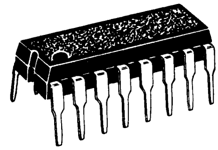
MN74HC237/MN74HC237S

3-to-8 Line Decoder with Address Latches

■ Description

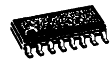
MN74HC237/MN74HC237S are high-speed 3-to-8 line decoders with three address latches. Address are stored, when $\overline{GL}$ input is "H". When enable input G1 is "H" and G2 is "L", the output depending on A, B and C inputs become "H", and all other outputs become "L". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P- 3



16-pin plastic DIL package

P- 4



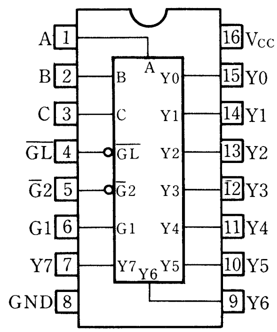
16-pin Panaflat package (SO-16D)

■ Truth Table

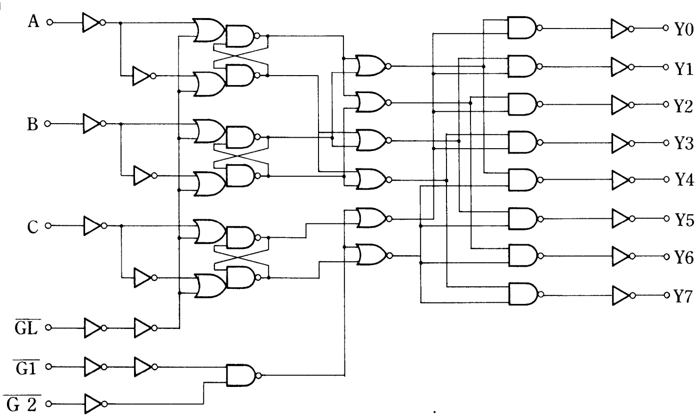
Input						Output							
Enable			Select										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
×	×	H	×	×	×	L	L	L	L	L	L	L	L
×	L	×	×	×	×	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	×	×	×	Output corresponding to stored address, L: all others, H							

Note:
1. H: HIGH level
2. L: LOW level
3. ×: Either HIGH or LOW; doesn't matter

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	°C
Power dissipation	MN74HC237	Ta=$-40\sim+60$°C	PD	400	mW
		Ta=$+60\sim+85$°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC237S	Ta=$-40\sim+60$°C	PD	275	mW
		Ta=$+60\sim+85$°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	°C
Input rise and fall time	t_r, t_f	V_{CC}=2.0V	$0\sim1000$	ns
		V_{CC}=4.5V	$0\sim500$	ns
		V_{CC}=6.0V	$0\sim400$	ns

■ DC Characteristics (GND=0V)

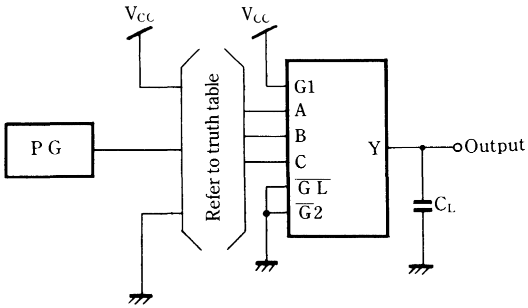
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25°C min.	typ.	max.	Ta=$-40\sim+85$°C min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		V
		6.0				4.2			4.2		V
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	V
		6.0						1.2		1.2	V
Ouptut HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		V
		6.0		−20.0	μA	5.9	6.0		5.9		V
		4.5		−4.0	mA	3.86			3.76		V
		6.0		−5.2	mA	5.36			5.26		V
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	V
		6.0		20.0	μA		0.0	0.1		0.1	V
		4.5		4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

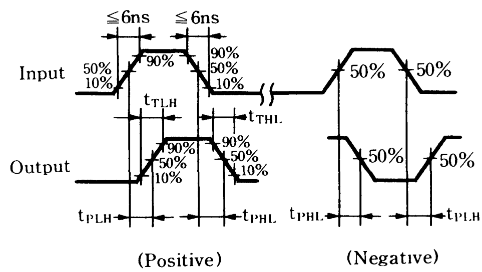
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25°C min.	typ.	max.	Ta=−40~+85°C min.	max.	Unit
Output rise time	t_{TLH}	2.0			22	75		95	ns
		4.5			9	15		19	
		6.0			8	13		16	
Output fall time	t_{THL}	2.0			19	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time A, B, C→Y (L→H)	t_{PLH}	2.0			48	150		190	ns
		4.5			22	30		38	
		6.0			20	26		33	
Propagation time A, B, C→Y (H→L)	t_{PHL}	2.0			40	150		190	ns
		4.5			23	30		38	
		6.0			20	26		33	
Propagation time GL→Y (L→H)	t_{PLH}	2.0			47	150		190	ns
		4.5			22	30		38	
		6.0			19	26		33	
Propagation time GL→Y (H→L)	t_{PHL}	2.0			50	150		190	ns
		4.5			20	30		38	
		6.0			18	26		33	
Propagation time G1→Y (L→H)	p_{LH}	2.0			34	150		190	ns
		4.5			17	30		38	
		6.0			15	26		33	
Propagation time G1→Y (H→Y)	t_{PHL}	2.0			33	150		190	ns
		4.5			17	30		38	
		6.0			15	26		33	
Propagation time $\overline{G}$2→Y (L→H)	t_{PLH}	2.0			33	125		155	ns
		4.5			17	25		31	
		6.0			16	21		26	
Propagation time $\overline{G}$2→Y (H→L)	t_{PHL}	2.0			32	125		155	ns
		4.5			17	25		31	
		6.0			16	21		26	
Minimum pulse width GL	t_w	2.0			≦6	100		125	ns
		4.5			≦6	20		25	
		6.0			≦6	17		21	
Minimum Set-up time A, B, C	t_{su}	2.0			17	100		125	ns
		4.5			3	20		25	
		6.0			2	17		21	
Minimum Hold time	t_h	2.0			—	75		95	ns
		4.5			—	15		19	
		6.0			—	13		16	

- Switching Time Measuring Circuit and Waveforms

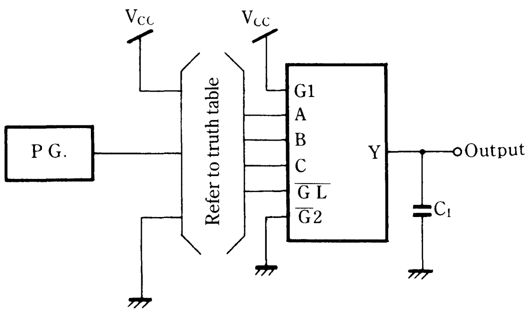
1. Measuring Circuit



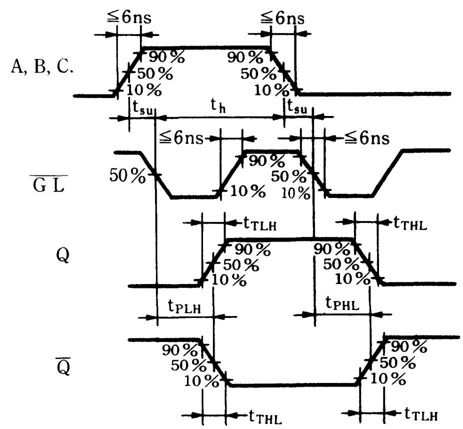
2. Waveforms



1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



MN74HC238/MN74HC238S

3-to-8 Line Decoder/Demultiplexer

■ Description

MN74HC238/MN74HC238S are high-speed 3-to-8 decoder/ demultiplexer decoding one of eight output lines depending on the condition of three select inputs (A0, A1 and A2) and threes enable inputs ($\overline{E1}$, $\overline{E2}$ and E3). The enable input consists of an active LOW of 2 inputs and active HIGH of 1-input which makes the subsidiary connection easy. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

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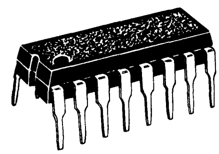
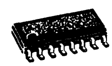


16-pin plastic DIL package

P- 4



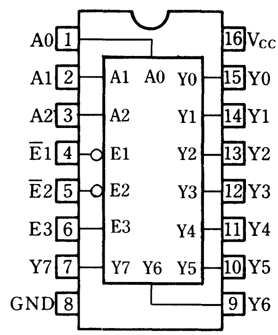
16-pin Panaflat package (SO-16D)

■ Truth Table

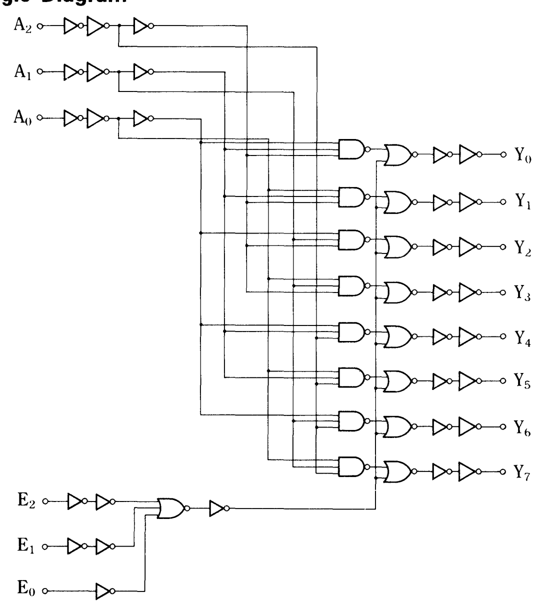
Input						Output							
$\overline{E1}$	$\overline{E2}$	E3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	×	×	×	×	×	L	L	L	L	L	L	L	L
×	H	×	×	×	×	L	L	L	L	L	L	L	L
×	×	L	×	×	×	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	H	H	L	L	L	H	L	L	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

Note: 1. H: HIGH level 2. L: LOW level

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	°C
Power dissipation	MN74HC238	Ta=−40～+60°C	PD	400	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC238S	Ta=−40～+60°C	PD	275	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	°C
		V_{CC}=2.0V	0～1000	ns
Inupt rise and fall time	t_r, t_f	V_{CC}=4.5V	0～500	ns
		V_{CC}=6.0V	0～400	ns

■ DC Characteristics (GND=0V)

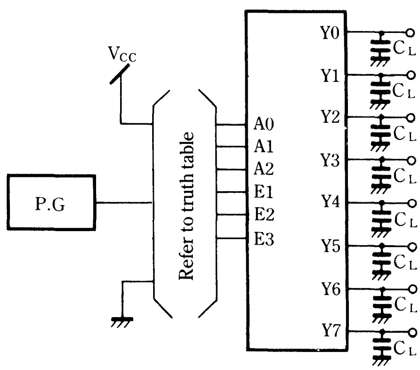
Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25°C			Ta=−40～+85°C		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		V
		6.0				4.2			4.2		V
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	V
		6.0						1.2		1.2	V
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		V
		6.0	or	−20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	−4.0	mA	3.86			3.76		V
		6.0		−5.2	mA	5.36			5.26		V
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

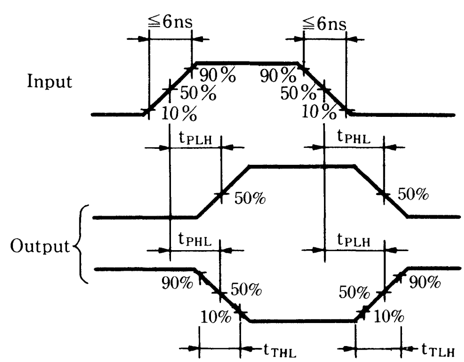
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25°C			Ta=−40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0			21	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
Output fall time	t_{THL}	2.0			13	75		95	ns
		4.5			5	15		19	
		6.0			4	13		16	
Propagation time A→Y (L→H)	t_{PLH}	2.0			36	150		190	ns
		4.5			13	30		38	
		6.0			11	26		33	
Propagation time A→Y (H→L)	t_{PHL}	2.0			33	150		190	ns
		4.5			13	30		38	
		6.0			11	26		33	
Propagation time $\overline{E}1$, $\overline{E}2$→Y (L→H)	t_{PLH}	2.0			49	150		190	ns
		4.5			16	30		38	
		6.0			13	26		33	
Propagation time $\overline{E}1$, $\overline{E}2$→Y (H→L)	t_{PHL}	2.0			41	150		190	ns
		4.5			16	30		38	
		6.0			13	26		33	
Propagation time E3→Y (L→H)	t_{PLH}	2.0			41	150		190	ns
		4.5			15	30		38	
		6.0			12	26		33	
Propagation time E3→Y (H→L)	t_{PHL}	2.0			40	150		190	ns
		4.5			15	30		38	
		6.0			13	26		33	

- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



MN74HCT238/MN74HCT238S

3-to-8 Decoder/Demultiplexer (TTL Input)

■ Description

MN74HCT238/MN74HCT238S are high-speed 3-to-8 decoder/demultiplexer (TTL input) decoding one of eight output lines depending on the condition of three select inputs (A0, A1 and A2) and threes enable inputs ($\overline{E1}$, $\overline{E2}$ and E3). The input consists of an active LOW of 2 inputs and active HIGH of 1-input which makes the subsidiary connection easy. All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2V or more is logic "1". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

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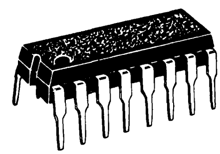
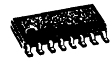


16-pin plastic DIL package

P- 4



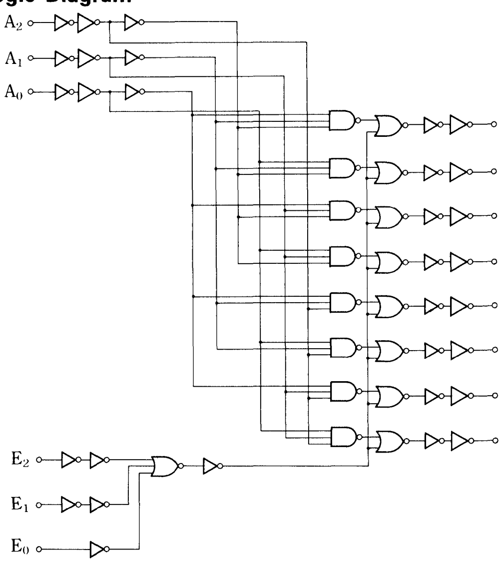
16-pin Panaflat package (SO-16D)

■ Truth Table

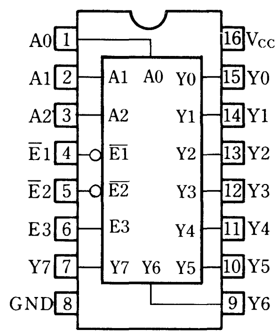
Input						Output							
$\overline{E1}$	$\overline{E2}$	E3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	×	×	×	×	×	L	L	L	L	L	L	L	L
×	H	×	×	×	×	L	L	L	L	L	L	L	L
×	×	L	×	×	×	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	H	H	L	L	L	H	L	L	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

Note: 1. H: HIGH level 2. L: LOW level

■ Logic Diagram



Pin Configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	°C
Power dissipation	MN74HC238	Ta=−40～+60°C	PD	400	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC238S	Ta=−40～+60°C	PD	275	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		4.5～5.5	V
Input/output	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	°C
Inupt rise and fall time	t_r, t_f	4.5V	0～500	ns

■ DC Characteristics (GND=0V)

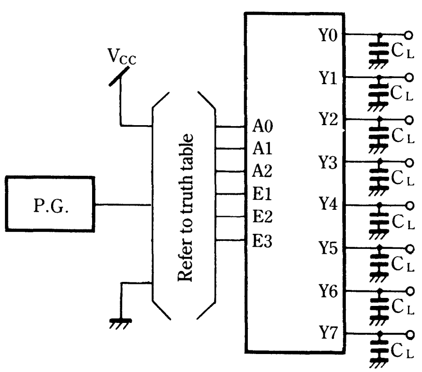
Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25°C			Ta=−40～+85°C		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	4.5 ～ 5.5				2.0			2.0		V
Input LOW voltage	V_{IL}	4.5 ～ 5.5						0.8		0.8	V
Output HIGH voltage	V_{OH}	4.5	V_{IH} or V_{IL}	−20.0	μA	4.4	4.5		4.4		V
		4.5		−4.0	mA	3.86			3.76		V
Output LOW voltage	V_{OL}	4.5	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		4.0	mA			0.32		0.37	V
Input current	I_I	5.5	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	5.5	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

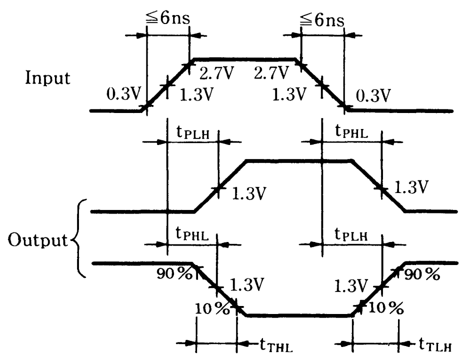
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25°C			Ta=−40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	4.5			5	15		19	ns
Output fall time	t_{THL}	4.5			4	15		19	ns
Propagation time A→Y (L→H)	t_{PLH}	4.5			18	35		44	ns
Propagation time A→Y (H→L)	t_{PHL}	4.5			13	30		38	ns
Propagation time $\overline{E}1$, $\overline{E}2$→Y (L→H)	t_{PLH}	4.5			20	40		50	ns
Propagation time $\overline{E}1$, $\overline{E}2$→Y (H→L)	t_{PHL}	4.5			16	30		38	ns
Propagation time E3→Y (L→H)	t_{PLH}	4.5			15	30		38	ns
Propagation time E3→Y (H→L)	t_{PHL}	4.5			21	40		50	ns

● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



MN74HC240/MN74HC240S

Inverting Octal TRI-STATE Buffers

■ Description

MN74HC240/MN74HC240S are high-speed inverting buffers constructed with octal tri-state outputs. High-speed operation can be obtained for driving a large capacity bus line, because these ICs have large current output. When the output is "L", inputs $1\overline{G}$ and $2\overline{G}$ are available, where output becomes enable and each of the four buffers is independently controlled. Adoption of the silicon gate CMOS process makes possible low power consumption and a high noise allowance; LS TTL 15-inputs can be directly driven. Resistors and diodes are used in the V_{CC} and GND in order to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

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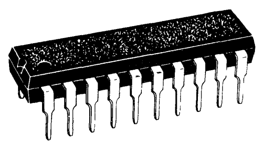
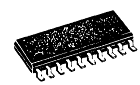


20-pin plastic DIL package

P-6



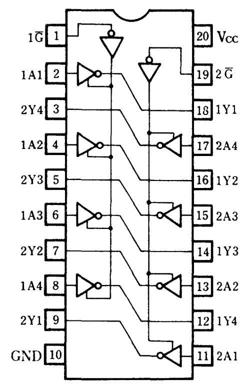
20-pin Panaflat package (SO-20D)

■ Truth Table

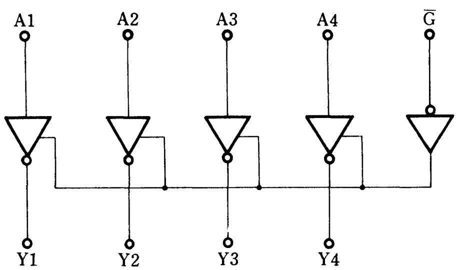
Input		Output	Input		Output
$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Hi-Z	H	L	Hi-Z
H	H	Hi-Z	H	H	Hi-Z

Note:
Hi-Z: High impedance

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC240	Ta$=-40\sim+60$℃	P_D	400	mW
		Ta$=+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC240S	Ta$=-40\sim+60$℃	P_D	275	mW
		Ta$=+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=$-40\sim+85$℃ min.	Ta=$-40\sim+85$℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
		6.0	or	-20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	$V_I=V_{IH}$ or V_{IL} $V_O=V_{CC}$ or GND					±0.5		±5.0	μA
Quescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

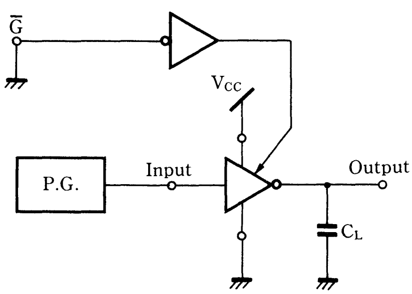
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time (L→H)	t_{PLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Propagation time (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
3-state propagation time (H→Z)	t_{PHZ}	2.0				125		155	ns
		4.5	R_L = 1 kΩ		14	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0				150		190	ns
		4.5	R_L = 1 kΩ		17	30		38	
		6.0				26		33	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L = 1 kΩ		12	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	ns
		4.5	R_L = 1 kΩ		13	20		25	
		6.0				17		21	

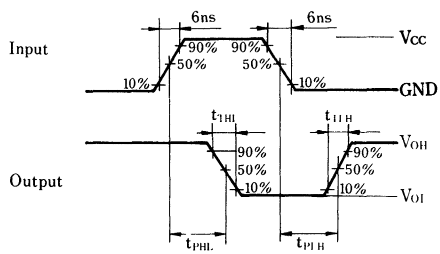
• Switching Time Measuring Circuit and Waveforms

[1] t_{TLH}, t_{THL}, t_{PLH}/t_{PHL}

1. Measuring Circuit (t_{PLH}, t_{PHL})

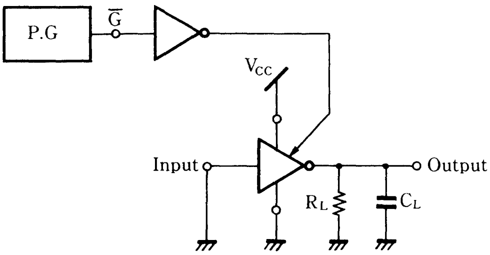


2. Waveforms

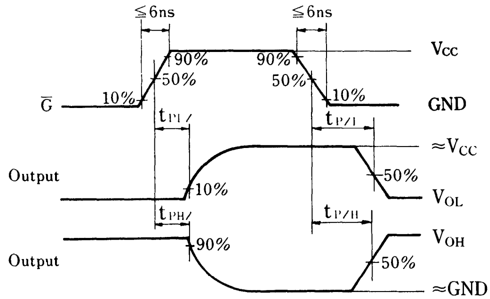


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

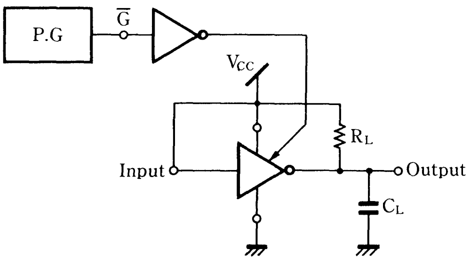


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

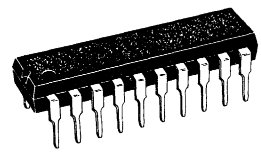
MN74HC241/MN74HC241S

Octal TRI-STATE Buffer

■ Description

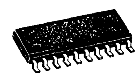
MN74HC241/MN74HC241S are high-speed non-inverted buffers constructed with octal tri-state outputs. High-speed operation can be obtained for driving a large capacity bus line, because these ICs have large current outputs. Also, these ICs have input $1\overline{G}$ where output becomes enable at "L" output, and input 2G where output becomes enable at "H" output, and each of the four buffers is independently controlled. Adoption of the silicon gate CMOS process makes possible low power consumption, a high noise allowance, and an operation speed equivalent to LS TTL; LS TTL 15-inputs can be directly drive. Resistors and diodes ar used in the V_{CC} and GND in order to protect the input/output from damage by static electricity. Same pin configuration and function as standard 45LS/74LS Logic Family.

P-5



20-pin plastic DIL package

P-6



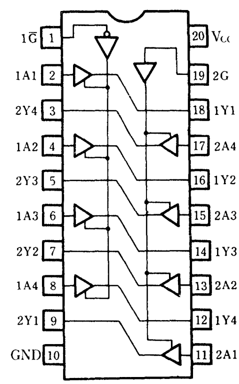
20-pin Panaflat package (SO-20D)

■ Truth Table

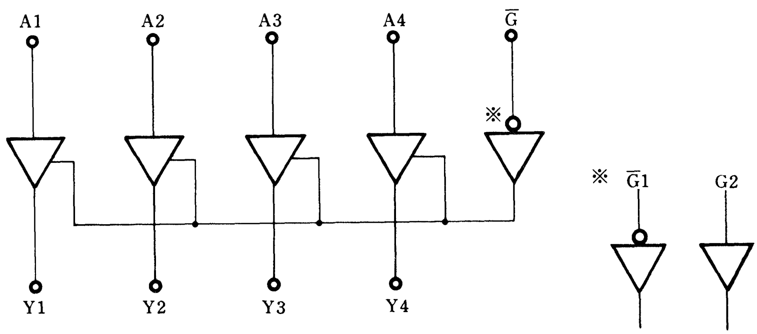
Input		Output	Input		Output
$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	L	L	Hi-Z
L	H	H	L	H	Hi-Z
H	L	Hi-Z	H	L	L
H	H	Hi-Z	H	H	H

Note:
1. Hi-Z: High impedance

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC241	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC241S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

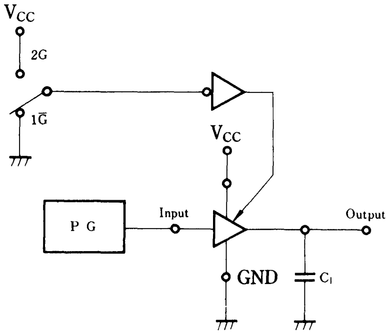
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Propagation time (L→H)	t_{PLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Propagation time (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
3-state propagation time (H→Z)	t_{PHZ}	2.0				125		155	ns
		4.5	R_L=1kΩ		14	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0				100		125	ns
		4.5	R_L=1kΩ		11	20		25	
		6.0				17		21	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L=1kΩ		11	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	ns
		4.5	R_L=1kΩ		11	20		25	
		6.0				17		21	

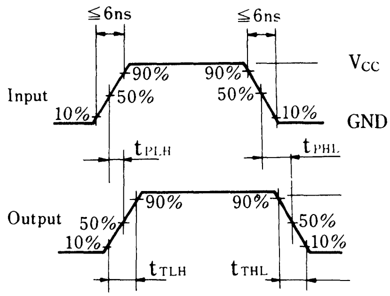
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

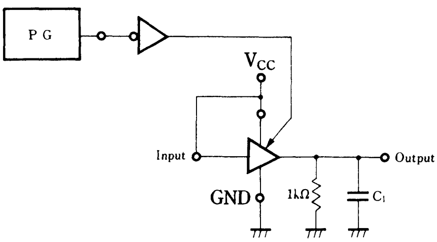


2. Waveforms

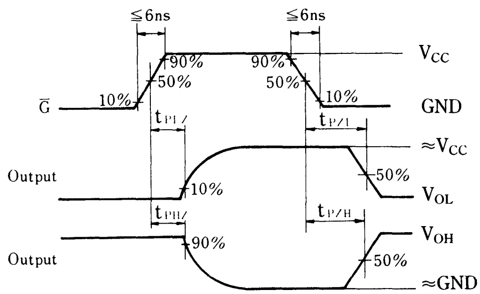


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

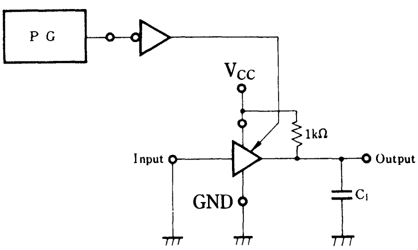


2. Waveforms (t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



MN74HC242/MN74HC242S

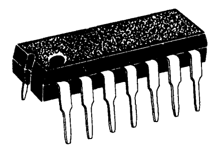
Inverting Quad TRI-STATE Transceivers

■ Description

MN74HC242/MN74HC242S are high-speed tri-state output, inverting buffers which asynchronously transfer the input bidirectionally through the data bus line. Large current output makes possible high-speed operation for driving a large capacity bus line. These ICs have input GBA where output A becomes enable at "H" level, and input $\overline{G}$AB where output B becomes enabled at "L" level. Adoption of the silicon gate CMOS process makes possible low power consumption, a high noise allowance, and an operation speed equivalent to LS TTL; LS TTL 15-pints can be directly driven.

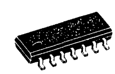
Resistors and diodes are used in the V_{CC} and GND in order to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

P-1



14-pin plastic DIL package

P-2



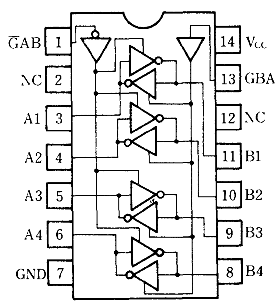
14-pin Panaflat package (SO-14D)

■ Truth Table

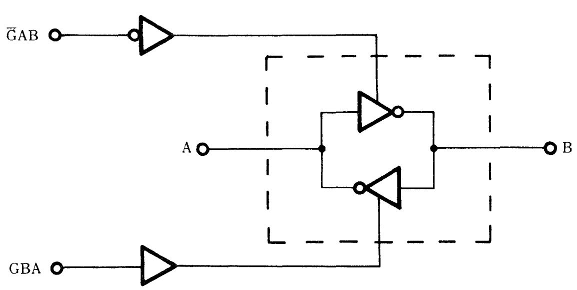
Control Input		Data Port Status	
$\overline{G}$AB	GBA	A	B
H	H	$\overline{\text{OUTPUT}}$	INPUT
L	H	*	*
H	L	Hi-Z	Hi-Z
L	L	INPUT	$\overline{\text{OUTPUT}}$

Note:
1. *: When the transceiver operates bi-directionally at the same time, destructive oscillation might occur.
2. Hi-Z: High impedance

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC242	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC242S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	$V_I=V_{IH}$ or V_{IL}, $V_O=V_{CC}$ or GND					±0.5		±5.0	μA
Quescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

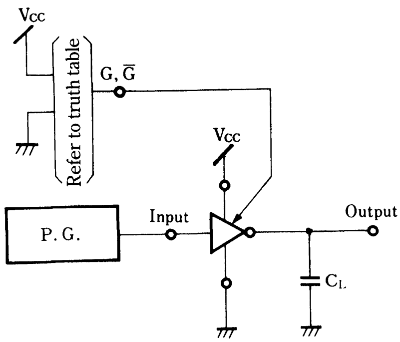
■ **AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)**

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40〜+85℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				50		65	ns
		4.5			6	10		13	
		6.0				9		11	
Propagation time A→B (L→H)	t_{PLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Propagation time A→B (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Propagation time B→A (L→H)	t_{PLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Propagation time B→A (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
3-state propagation time (H→Z)	t_{PHZ}	2.0				150		190	ns
		4.5	R_L= 1 kΩ		17	30		38	
		6.0				26		33	
3-state propagation time (L→Z)	t_{PLZ}	2.0				125		155	ns
		4.5	R_L= 1 kΩ		15	25		31	
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L= 1 kΩ		13	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				125		155	ns
		4.5	R_L= 1 kΩ		15	25		31	
		6.0				21		26	

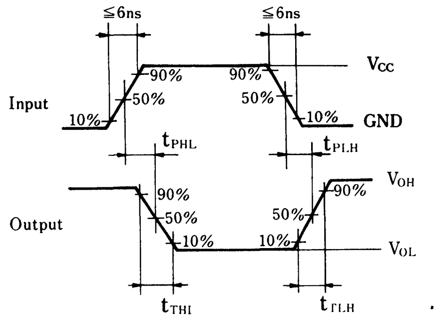
• Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, PLH t_{PHL}(A→B or B→A)

1. Measuring Circuit

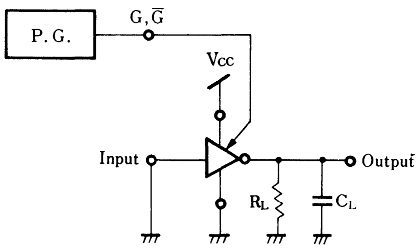


2. Waveforms

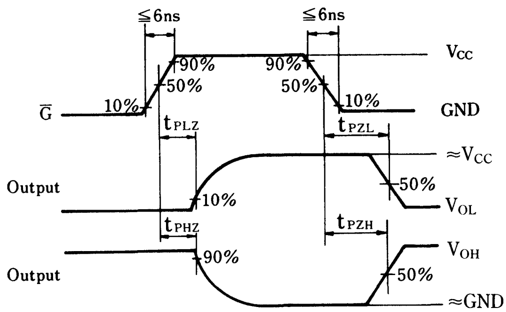


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

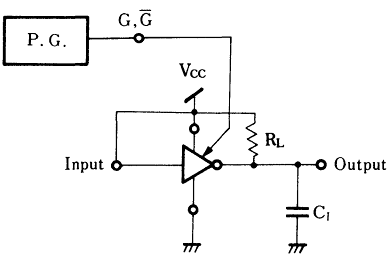


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

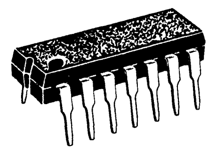
MN74HC243/MN74HC243S

Quad TRI-STATE Transceivers

■ Description

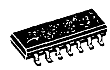
MN74HC243/MN74HC243S are high-speed tri-state output and non-inverted buffer transferring input bi-directionally and asynchronously through a data bus line. High-speed operation can be obtained for driving a large-capacity bus line due to large current output. It has input GBA where output A becomes enabled at HIGH, and input $\overline{G}$AB where output B becomes enable at LOW. Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

P-1



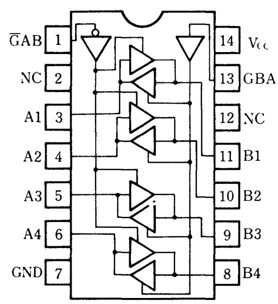
14-pin plastic DIL package

P-2



14-pin Panaflat package (SO-14D)

Pin configuration (top view)

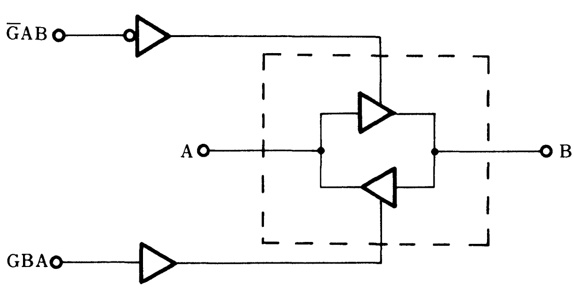


■ Truth Table

Control Inputs		Data Port Status	
$\overline{G}$AB	GBA	A	B
H	H	Output	Input
L	H	*	*
H	L	Hi-Z	Hi-Z
L	L	Input	Output

Note:
1. *: If transceiver is bi-directionally at the same time, destructive oscillation may be generated.
2. Hi-Z: High impedance

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC243	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC243S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=$-40\sim+85$℃ min.	Ta=$-40\sim+85$℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
		6.0	or	-20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	$V_I=V_{IH}$ or V_{IL}, $V_O=V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

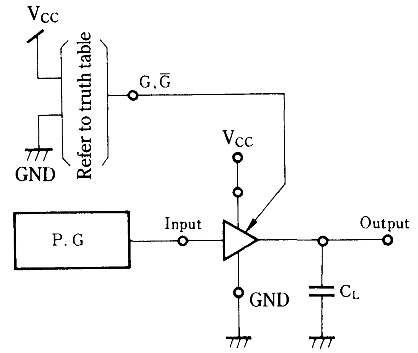
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time A→B (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			8	20		25	
		6.0				17		21	
Propagation time A→B (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			6	20		25	
		6.0				17		21	
Propagation time B→A (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			8	20		25	
		6.0				17		21	
Propagation time B→A (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			7	20		25	
		6.0				17		21	
3-state propagation time (H→Z)	t_{PHZ}	2.0				125		155	ns
		4.5	R_L= 1 kΩ		15	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0				100		125	ns
		4.5	R_L= 1 kΩ		12	20		25	
		6.0				17		21	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L= 1 kΩ		9	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	ns
		4.5	R_L= 1 kΩ		10	20		25	
		6.0				17		21	

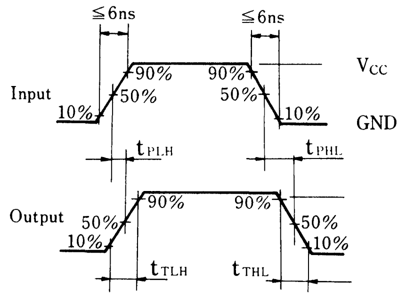
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}/t_{PHL} (A→B or B→A)

1. Measuring Circuit

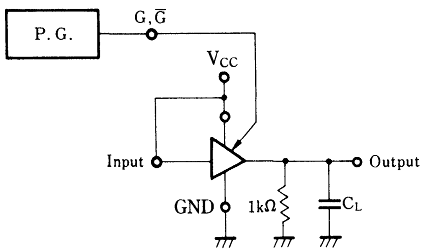


2. Waveforms

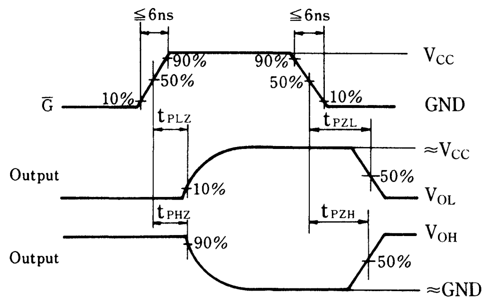


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

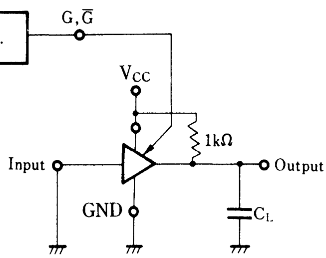


2. Waveforms (t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



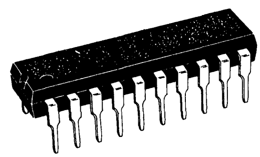
MN74HC244/MN74HC244S

Octal TRI-STATE Buffers

■ Description

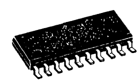
MN74HC244/MN74HC244S are high-speed non-inverted buffers consisting of octal tri-state outputs. High-speed operation is possible for driving a large capacitance bus line owing to large current output. Inputs $1\overline{G}$ and $2\overline{G}$ are available where output becomes enabled at LOW, and each input controls 4 buffers. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-5



20-pin plastic DIL package

P-6



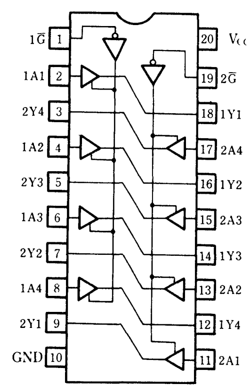
20-pin Panaflat package (SO-20D)

■ Truth Table

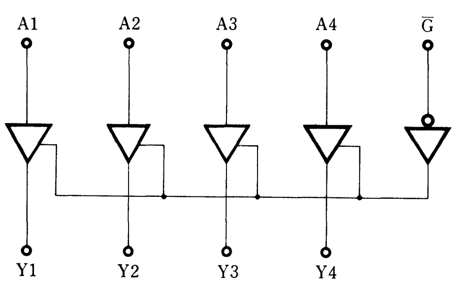
Input		Output	Input		Output
$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Hi-Z	H	L	Hi-Z
H	H	Hi-Z	H	H	Hi-Z

Note:
1. Hi-z: High impedance

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC244	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC244S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=−40～+85℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL} V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

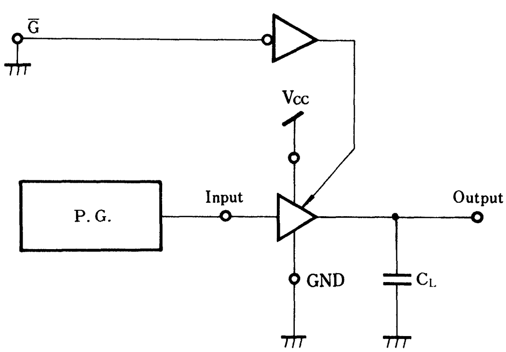
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40～+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0			18	75		95	ns
		4.5			9	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0			17	75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Propagation time (L→H)	t_{PLH}	2.0			16	75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Propagation time (H→L)	t_{PHL}	2.0			18	75		95	ns
		4.5			8	15		19	
		6.0				13		16	
3-state propagation time (H→Z)	t_{PHZ}	2.0	R_L= 1 kΩ		21	125		155	ns
		4.5			13	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0	R_L= 1 kΩ		28	125		155	ns
		4.5			16	25		31	
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0	R_L= 1 kΩ		25	100		125	ns
		4.5			12	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0	R_L= 1 kΩ		33	125		155	ns
		4.5			14	25		31	
		6.0				21		26	

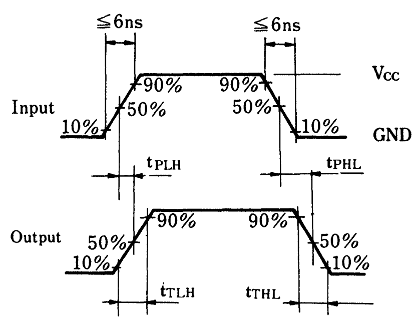
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

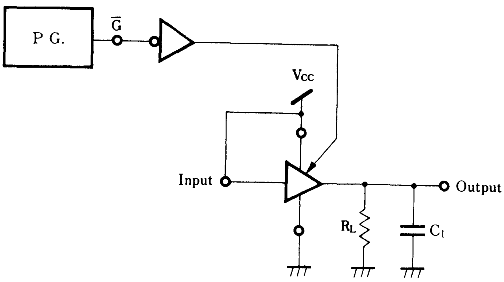


2. Waveforms

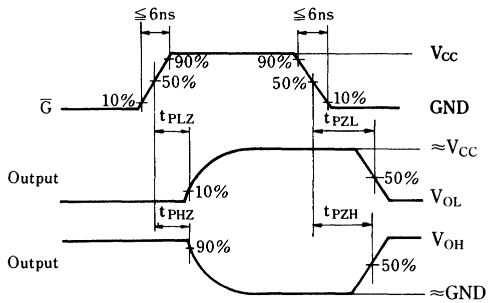


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

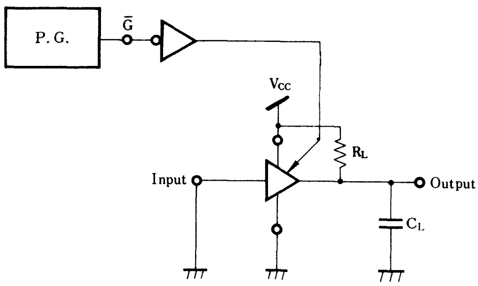


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

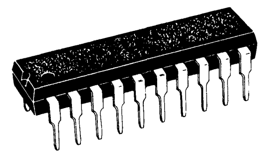
MN74HC245/MN74HC245S

Octal TRI-STATE Transceivers

■ Description

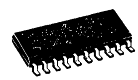
MN74HC245/MN74HC245S are high-speed non-inverted bi-directional buffers consisting of octal tri-state output. Input is transferred bi-directionally asynchronously through a data bus line. Large current output enables high-speed operation for driving a large capacitance bus line. It has input G where output becomes enabled at LOW, and direction control input DIR. When DIR input is HIGH, data is transferred from input A to B, and, when DIR input is LOW, data is transferred from input B to output A. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs are directly driven.
Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-5



20-pin plastic DIL package

P-6



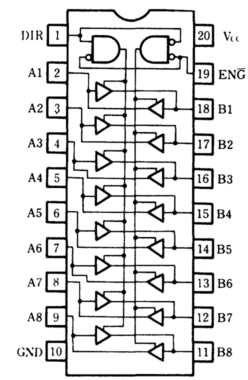
20-pin Panaflat package (SO-20D)

■ Truth Table

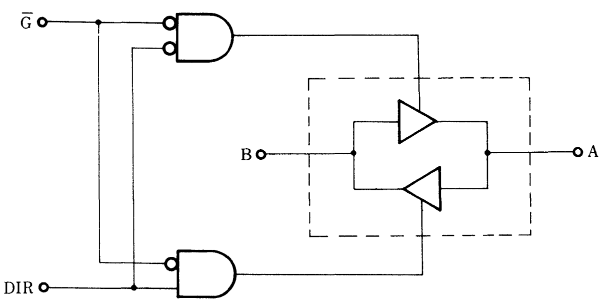
Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	×	Hi-Z

Note:
1. Hi-Z: High impedance
2. ×: Either HIGH OR LOW; it doesn't matter

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC245	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC245S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

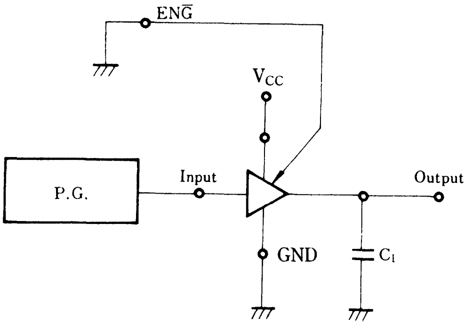
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40～+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time (L→H)	t_{PLH}	2.0				75		95	ns
		4.5			5	15		19	
		6.0				13		16	
Propagation time (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			5	15		19	
		6.0				13		16	
3-state propagation time (H→Z)	t_{PHZ}	2.0				150		190	ns
		4.5	R_L = 1 kΩ		16	30		38	
		6.0				26		33	
3-state propagation time (L→Z)	t_{PLZ}	2.0				150		190	ns
		4.5	R_L = 1 kΩ		18	30		38	
		6.0				26		33	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L = 1 kΩ		12	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				125		155	ns
		4.5	R_L = 1 kΩ		14	25		31	
		6.0				21		26	

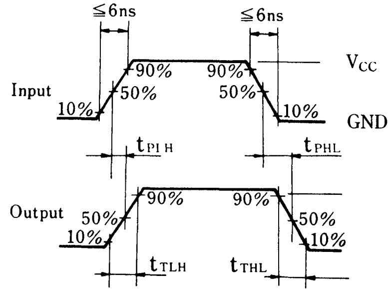
• Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

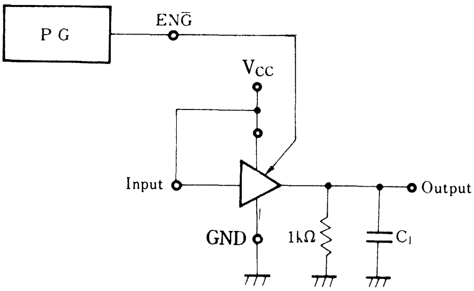


2. Waveforms

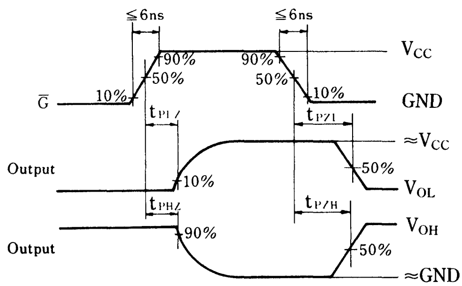


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

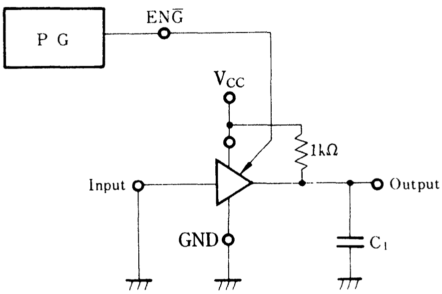


2. Waveforms (t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



MN74HC251/MN74HC251S

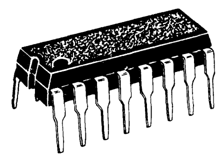
8-Channel TRI-STATE Multiplexer

■ Description

MN74HC251/MH74HC251S are 8-channel tri-state multiplexer selecting one input from eight channel data input; each multiplexer has a reverse phase output Y, W, and strobe input. When strobe input is "L", the circuit becomes enabled; when strobe input is "H", status. Accordingly, when strobe input is "L", one input is selected according to the select input A, B, C combination, and data is transferred to outputs Y, W.

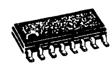
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



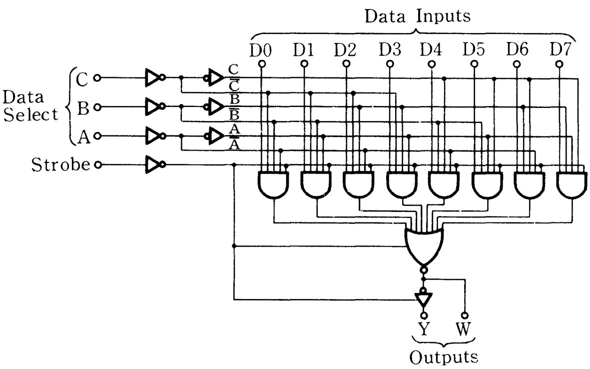
16-pin plastic DIL package

P-4

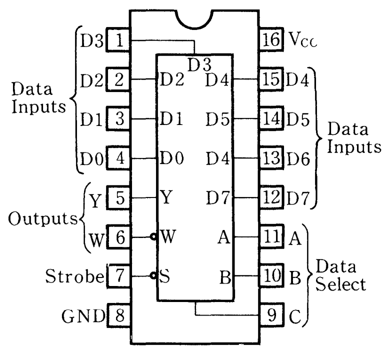


16-pin Panaflat package (SO-16D)

■ Logic Diagram



Pin configuration (top view)



■ Truth Table

Input				Output	
Select			Strobe S	Y	W
C	B	A			
×	×	×	H	Hi-Z	Hi-Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance
3. D0, D1, ... D7: Related D input level

■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC} +0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC251	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC251S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL} V_O=V_{CC} or GND					±0.5		±5.0	μA
Quescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

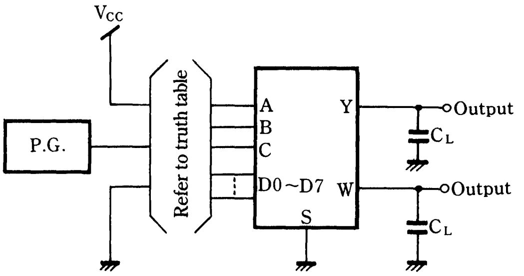
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time D→Y, W(L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Propagation time D→Y, W(H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Propagation time A,B,C→Y,W(L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Propagation time A,B,C→Y,W(H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
3-state propagation time (H→Z)	t_{PHZ}	2.0				100		125	ns
		4.5	R_L=1kΩ			20		25	
		6.0				17		21	
3-state propagation time (L→Z)	t_{PLZ}	2.0				100		125	ns
		4.5	R_L=1kΩ			20		25	
		6.0				17		21	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L=1kΩ			20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	ns
		4.5	R_L=1kΩ			20		25	
		6.0				17		21	

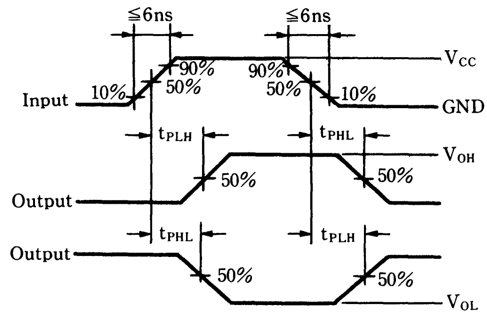
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

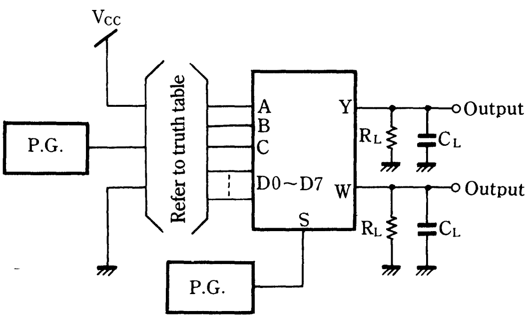


2. Waveforms

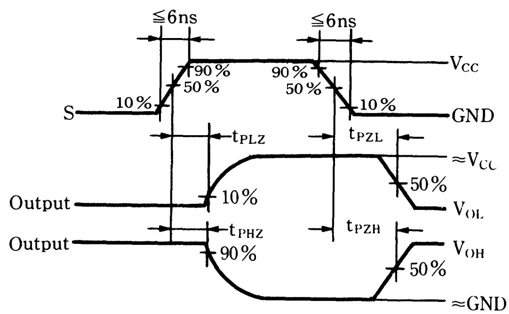


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

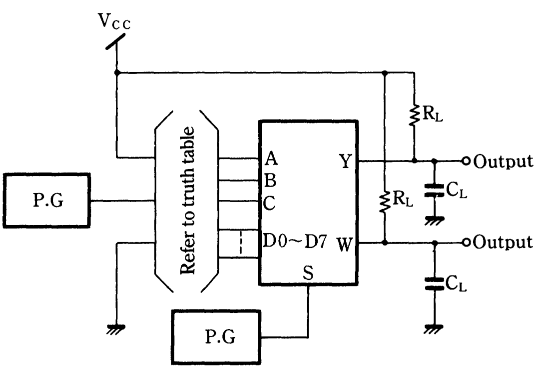


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

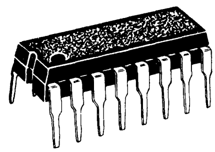
MN74HC253/MN74HC253S

Dual 4-Channel TRI-STATE Multiplexers

■ Description

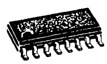
MN74HC253/MH74HC253S contain two tri-state multiplexers selecting one input from 4-channel data inputs in one chip. Output control input controls dual 4 lines respectively. When output control input is "H", output becomes high impedance regardless of bus line. When output control input is "L", data is transferred to the output by selecting output channel suited for data input signal from select input A and B.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



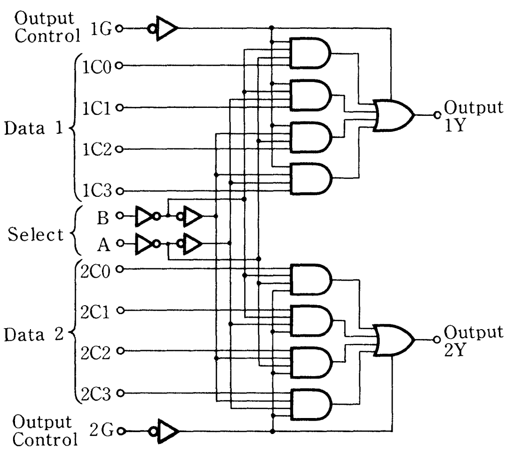
16-pin plastic DIL package

P-4

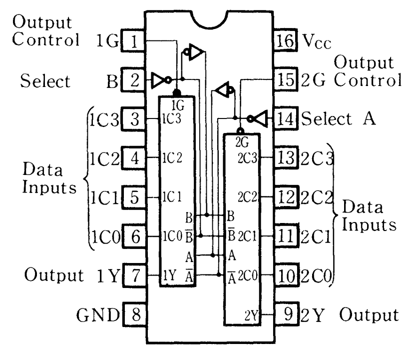


16-pin Panaflat package (SO-16D)

■ Logic Diagram



Pin configuration (top view)



■ Truth Table

Input							Output
Select		Data				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
×	×	×	×	×	×	H	Hi-Z
L	L	L	×	×	×	L	L
L	L	H	×	×	×	L	H
L	H	×	L	×	×	L	L
L	H	×	H	×	×	L	H
H	L	×	×	L	×	L	L
H	L	×	×	H	×	L	H
H	H	×	×	×	L	L	L
H	H	×	×	×	H	L	H

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance

■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC253	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC253S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=−40～+85℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	− 6.0	mA	3.86			3.76		
		6.0		− 7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

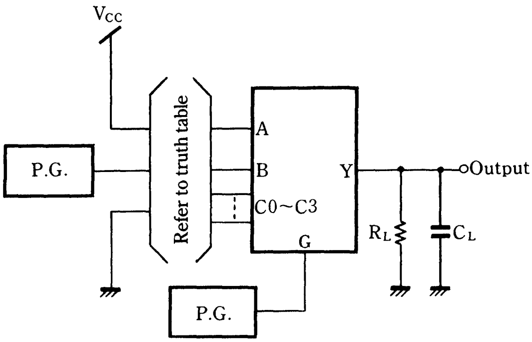
■ **AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)**

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time A,B→Y(L→H)	t_{PLH}	2.0				150		190	ns
		4.5			18	30		38	
		6.0				26		33	
Propagation time A,B→Y(H→L)	t_{PHL}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
Propagation time C→Y(L→H)	t_{PLH}	2.0				150		190	ns
		4.5			18	30		38	
		6.0				26		33	
Propagation time C→Y(H→L)	t_{PHL}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
3-state propagation time (H→Z)	t_{PHZ}	2.0				125		155	ns
		4.5	R_L=1kΩ		12	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0				125		155	ns
		4.5	R_L=1kΩ		13	25		31	
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0				150		190	ns
		4.5	R_L=1kΩ		17	30		38	
		6.0				26		33	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	ns
		4.5	R_L=1kΩ		10	20		25	
		6.0				17		21	

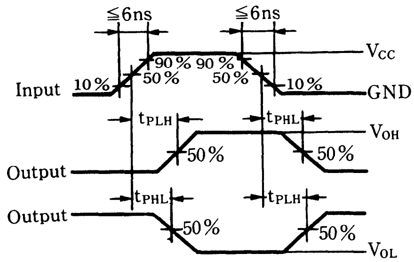
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

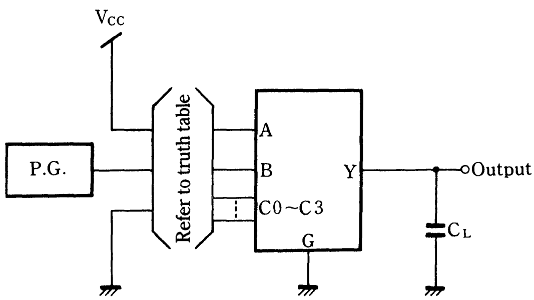


2. Waveforms

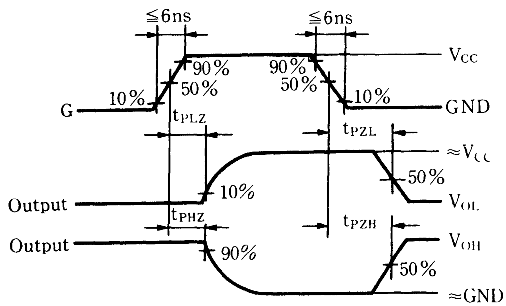


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

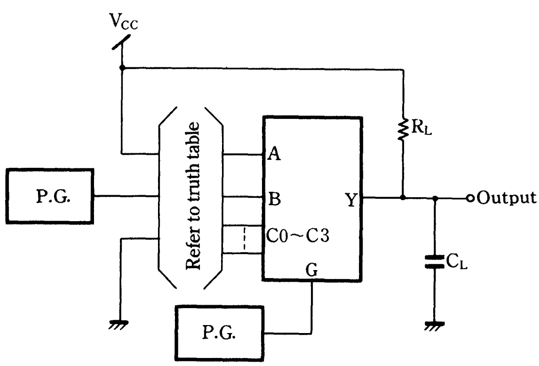


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

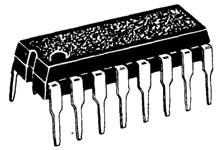
MN74HC257/MN74HC257S

Quad 2-Channel TRI-STATE Multiplexers

■ Description

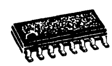
MN74HC257/MH74HC257S contain four tri-state multiplexers selecting one input from two data inputs in one chip. Input is composed of two data inputs A, B each determining the output, output control, and select input common to four output groups. When output control is "H", quad multiplexer outputs become high impedance. If select input is "H" at LOW level, data B status is output; if select input is "L", data A status is output.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



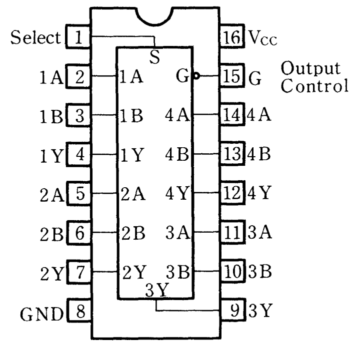
16-pin Panaflat package (SO-16D)

■ Truth Table

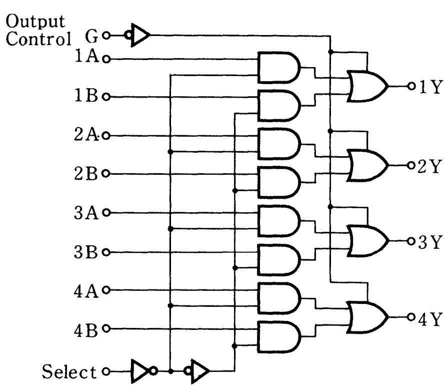
Input				Output
G	Select	A	B	Y
H	×	×	×	Hi-Z
L	L	L	×	L
L	L	H	×	H
L	H	×	L	L
L	H	×	H	H

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC257	Ta$=-40\sim+60$℃	P_D	400	mW
		Ta$=+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC257S	Ta$=-40\sim+60$℃	P_D	275	mW
		Ta$=+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta$=-40\sim+85$℃ min.	Ta$=-40\sim+85$℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	-20.0	μA	1.9	2.0		1.9		V
		4.5		-20.0	μA	4.4	4.5		4.4		
		6.0		-20.0	μA	5.9	6.0		5.9		
		4.5		-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	$V_I=V_{IH}$ or V_{IL}, $V_O=V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

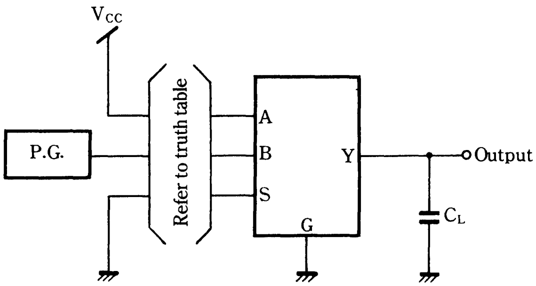
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40~+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time A,B→Y (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			13	30		38	
		6.0				26		33	
Propagation time A,B→Y (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			12	30		38	
		6.0				26		33	
Propagation time S→Y (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			13	30		38	
		6.0				26		33	
Propagation time S→Y (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			13	30		38	
		6.0				26		33	
3-state propagation time (H→Z)	t_{PHZ}	2.0				125		155	ns
		4.5	R_L=1kΩ		12	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0				125		155	ns
		4.5	R_L=1kΩ		13	25		31	
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L=1kΩ		10	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	ns
		4.5	R_L=1kΩ		10	20		25	
		6.0				17		21	

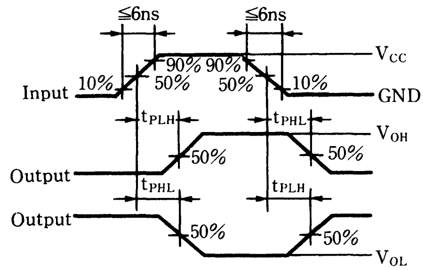
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

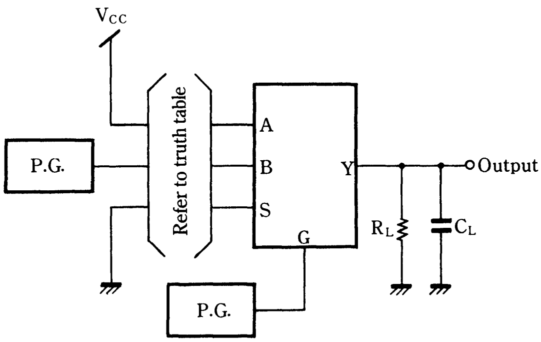


2. Waveforms

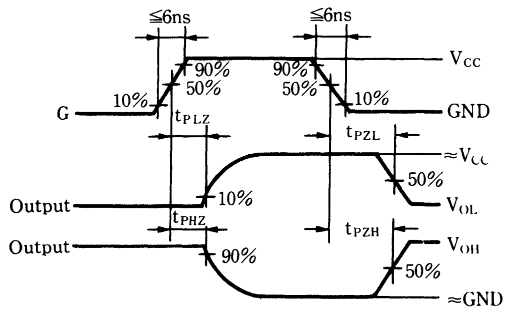


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

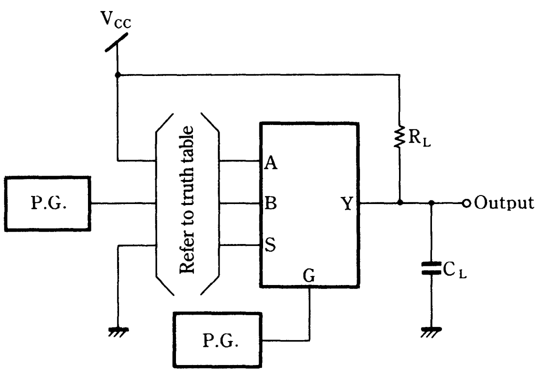


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

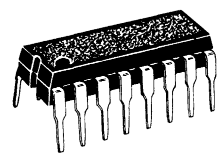
MN74HC258/MN74HC258S

Quad 2-Channel TRI-STATE Multiplexers (Inverted Output)

■ Description

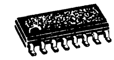
MN74HC258/MH74HC258S contain four tri-state multiplexers selecting one input from two data inputs in one chip. Input is composed of two data inputs A, B each determining the output, output control, and select input common to four output groups. When output control is "H", quad multiplexer outputs become high impedance. If select input is "H" inverted data B is output; if select inputs is "L", inverted data A is output.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



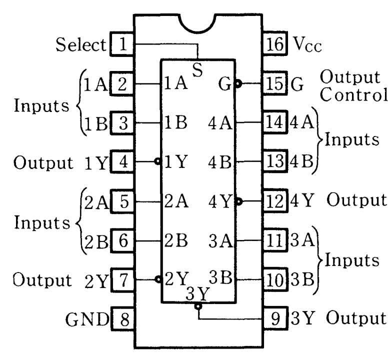
16-pin Panaflat package (SO-16D)

■ Truth Table

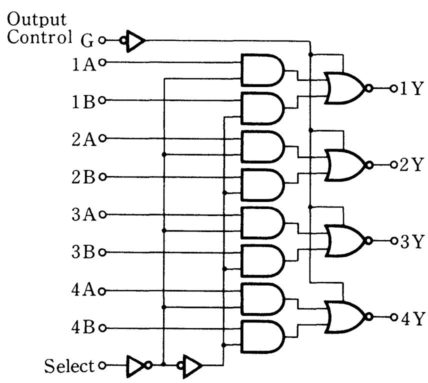
Input				Output
G	Select	A	B	Y
H	×	×	×	Hi-Z
L	L	L	×	H
L	L	H	×	L
L	H	×	L	H
L	H	×	H	L

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC258	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC258S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

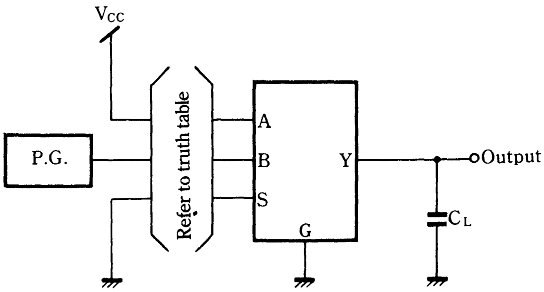
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time A,B→Y (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			12	30		38	
		6.0				26		33	
Propagation time A,B→Y (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			11	30		38	
		6.0				26		33	
Propagation time S→Y (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			14	30		38	
		6.0				26		33	
Propagation time S→Y (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			13	30		38	
		6.0				26		33	
3-state propagation time (H→Z)	t_{PHZ}	2.0				125		155	ns
		4.5	R_L=1kΩ		12	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0				125		155	ns
		4.5	R_L=1kΩ		14	25		31	
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L=1kΩ		10	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	ns
		4.5	R_L=1kΩ		11	20		25	
		6.0				17		21	

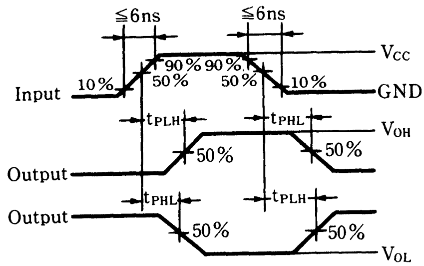
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

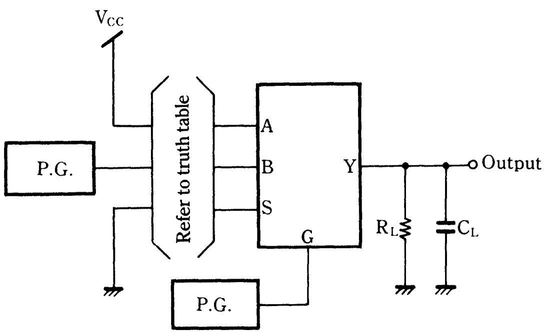


2. Waveforms

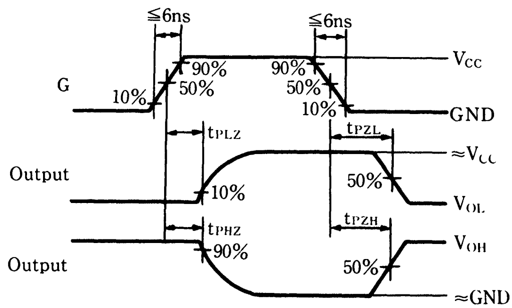


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

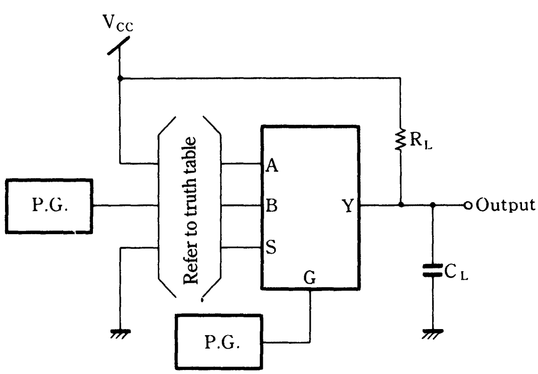


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

MN74HC266/MN74HC266S

Quad 2-Input Exclusive NOR (XNOR) Gates

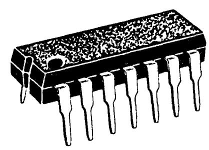
■ Description

MN74HC266/MN74HC266S contain quad 2-input exclusive NOR gates.

Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

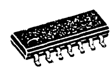
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



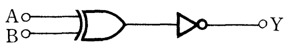
14-pin plastic DIL package

P-2

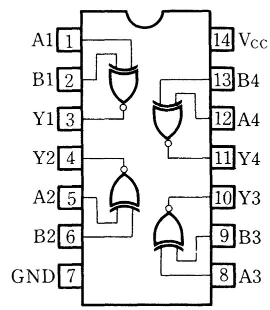


14-pin Panaflat package (SO-14D)

■ Logic Diagram (1 gate)



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC266	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC266S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25℃			Ta=−40~+85℃		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40~+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

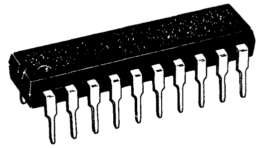
MN74HC273/MN74HC273S

Quad D-Type Flip-Flops with Clear

■ Description

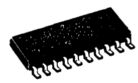
MN74HC273/MN74HC273S contain eight D-type flip-flops with clear. This is a master/slave flip-flop with common clock and clear. D input data satisfying set-up time is transferred to output Q on the positive-going edge of the clock pulse. When the clear input is low, all outputs are set to low. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs are directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-5



20-pin plastic DIL package

P-6



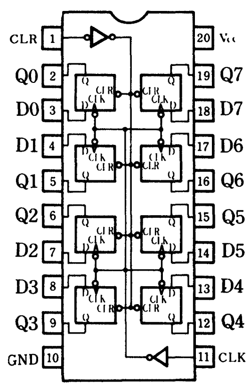
20-pin Panaflat package (SO-20D)

■ Truth Table

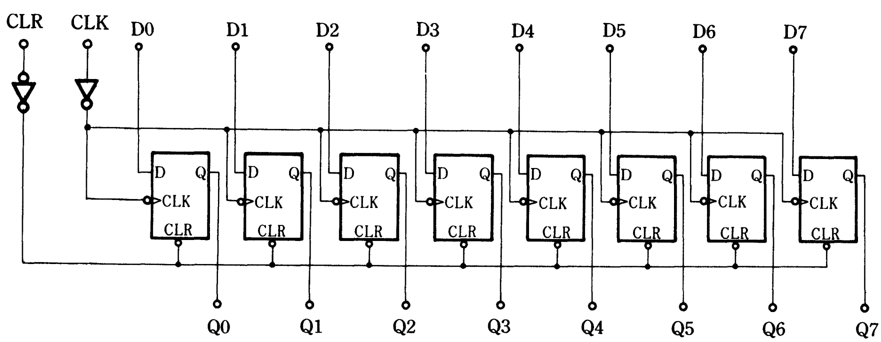
Input			Output
CLR	CLK	D	Q
L	×	×	L
H	_/‾	H	H
H	_/‾	L	L
H	L	×	Q_0

Note:
1. _/‾ : Data Input is transmitted to output during the rise of clock from "L" to "H".
2. X_0: Either of "H" and "L" will do.
3. Q_0: Q level before establishment of input conditions shown in the table.

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC273	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC273S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	tr, tf	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

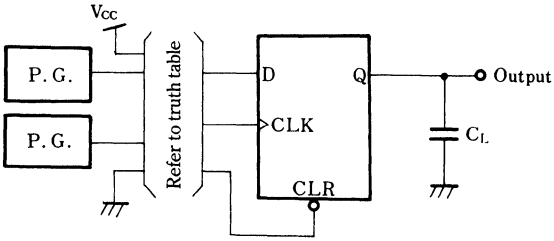
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time CLK→Q (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			12	25		31	
		6.0				21		26	
Propagation time CLK→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	
Propagation time CLR→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Minimum Set-up time	t_{su}	2.0				100		95	ns
		4.5			1	20		19	
		6.0				17		16	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum CLR pulse width	t_w	2.0				100		125	ns
		4.5			6	20		25	
		6.0				17		21	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5			2	15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30	45		24		
		6.0		35			28		

● Switchıng Time Measurıng Circuit and Waveforms

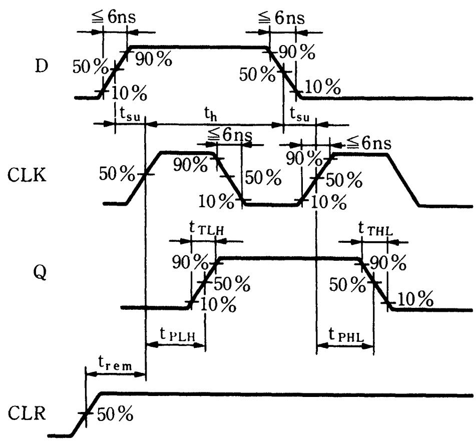
1. Measurıng Circuit

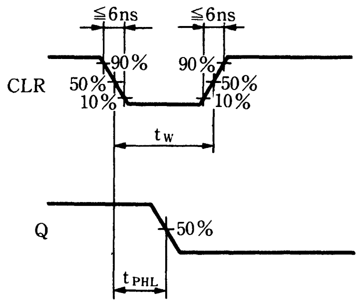


2. Waveforms

Waveforms-1 (t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH}/t_{PHL}(CLK→Q), t_{rem}, t_h)

Waveforms-2 (t_{PHL}(CLR→Q), t_W)





MN74HC280/MN74HC280S

9-Bit Odd/Even Parity Generator/Checker

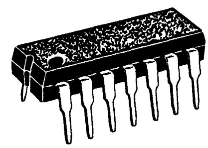
■ Description

MN74HC280/280S are 9-bit odd/even parity generator/checker, which have odd/even outputs to follow odd/even parity. Word length can be easily expanded by cascade connection.

All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2V or more is logic "1". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

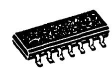
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P- 1



14-pin plastic DIL package

P- 2



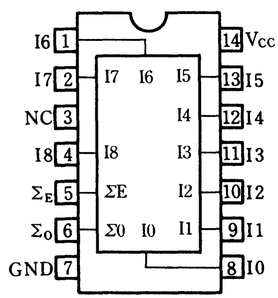
14-pin Panaflat package (SO-14D)

■ Truth Table

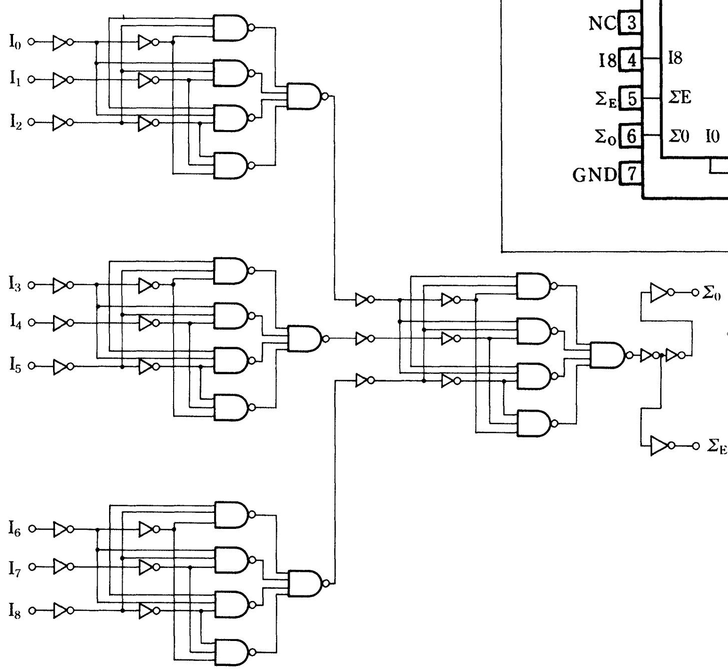
Input signal at HIGH level from data input (I_0~I_8)	Output	
	ΣE	ΣO
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Note:
1. H: HIGH level
2. L: LOW level

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	°C
Power dissipation	MN74HC280	Ta=−40～+60°C	P_D	400	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC280S	Ta=−40～+60°C	P_D	275	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	°C
Input rise and fall time	t_r, t_f	V_{CC}=2.0V	0～1000	ns
		V_{CC}4.5V	0～500	ns
		V_{CC}=6.0V	0～400	ns

■ DC Characteristics (GND=0V)

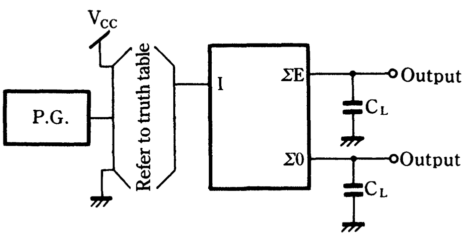
Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
						Ta=25°C			Ta=−40～+85°C		
			V_I	I_O	Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		V
		6.0				4.2			4.2		V
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	V
		6.0						1.2		1.2	V
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		V
		6.0	or	−20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	−4.0	mA	3.86			3.76		V
		6.0		−5.2	mA	5.36			5.26		V
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

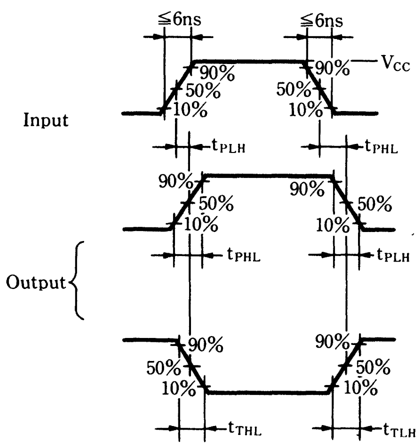
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25°C			Ta=−40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Propagation time I→ΣE (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				30		38	
Propagation time I→ΣE (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		83	
		6.0				26		33	
Propagation time I→ΣO (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Propagation time I→ΣO (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	

- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



MN74HCT280/MN74HCT280S

9-Bit Odd/Even Parity Generator/Checker (TTL Input)

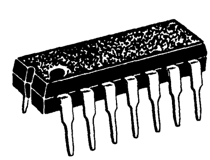
■ Description

MN74HCT280/MN74HCT280S are 9-bit odd/even parity generator/checker, which have odd/even outputs to follow odd/even parity. Word length can be easily expanded by cascade connection.

All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2V or more is logic "1". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

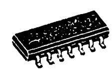
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P- 1



14-pin plastic DIL package

P- 2



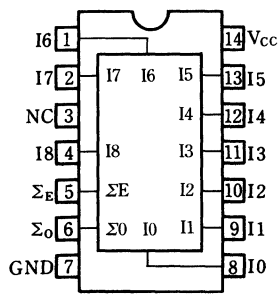
14-pin Panaflat package (SO-14D)

■ Truth Table

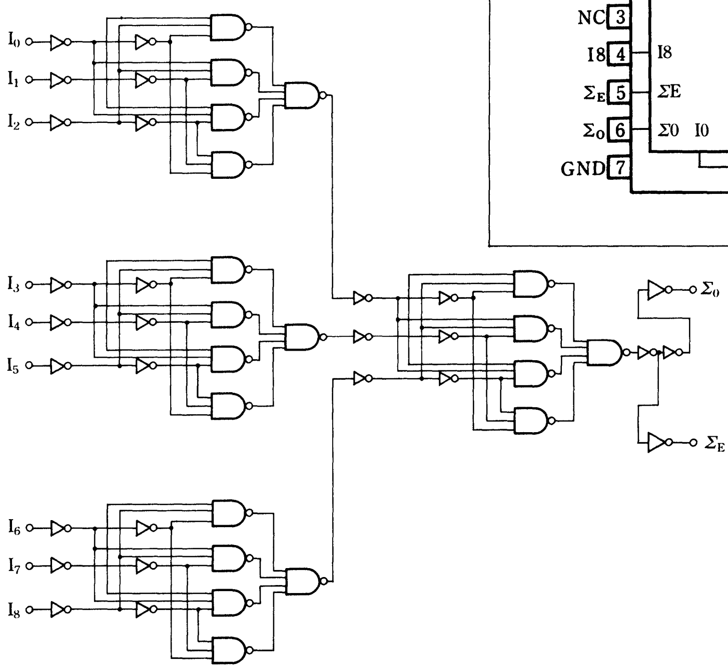
Input signal at HIGH level from data input (I_0~I_8)	Output	
	ΣE	ΣO
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Note:
1. H: HIGH level
2. L: LOW level

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input/output voltage			V_I, V_O	−0.5~V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65~+150	°C
Power dissipation	MN74HCT280	Ta=−40~+60°C	P_D	400	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HCT280S	Ta=−40~+60°C	P_D	275	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		4.5~5.5	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	°C
Input rise and fall time	t_r, t_f	V_{CC}=4.5V	0~500	ns

■ DC Characteristics (GND=0V)

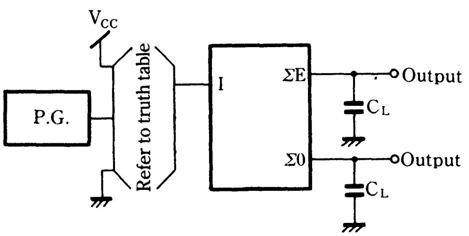
Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25°C			Ta=−40~+85°C		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	4.5~5.5				2.0			2.0		V
Input LOW voltage	V_{IL}	4.5~5.5						0.8		0.8	V
Output HIGH voltage	V_{OH}	4.5	V_{IH} or V_{IL}	−20.0	μA	4.4	4.5		4.4		V
		4.5		−4.0	mA	3.86			3.76		V
Output LOW voltage	V_{OL}	4.5	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		4.0	mA			0.32		0.37	V
Input current	I_I	5.5	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	5.5	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

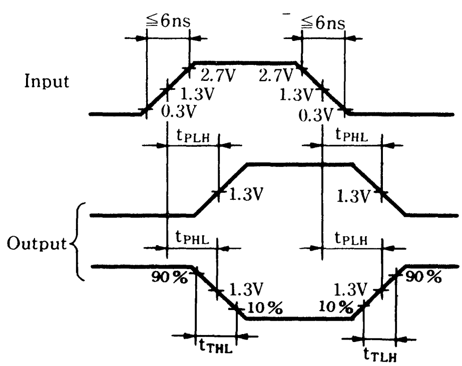
Parameter	Symbol	V_{CC} (V)	Test Condıtions	Temperature Ta=25°C min.	typ.	max.	Ta=−40∼+85°C min.	max.	Unit
Output rise time	t_{TLH}	4.5				15		19	ns
Output fall time	t_{THL}	4.5				15		19	ns
Propagatıon time I→ΣE (L→H)	t_{PLH}	4.5				30		38	ns
Propagation time I→ΣE (H→L)	t_{PHL}	4.5				30		38	ns
Propagation time I→ΣO (L→H)	t_{PLH}	4.5				30		38	ns
Propagation time I→ΣO (H→L)	t_{PHL}	4.5				30		38	ns

● Switchıng Tıme Measurıng Circuıt and Waveforms

1. Measurıng Cırcuıt (t_{PLH}, t_{PHL})



2. Waveforms



MN74HC352/MN74HC352S

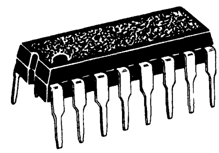
Dual 4-Input Multiplexers (Inverted Output)

■ Description

MN74H352/352S are dual 4-input multiplexers which transfer one of four inverted data to output Y according to the common select input (A, B). Each multiplexer has a respective strobe input. Multiplexer functions at LOW level. At HIGH level, output is fixed LOW.

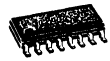
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directry driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



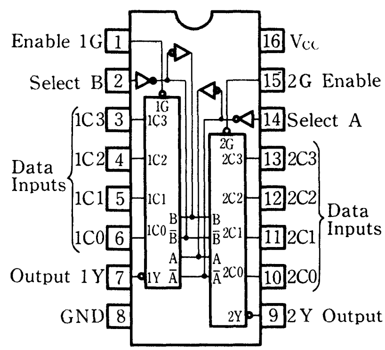
16-pin Panaflat package (SO-16D)

■ Truth Table

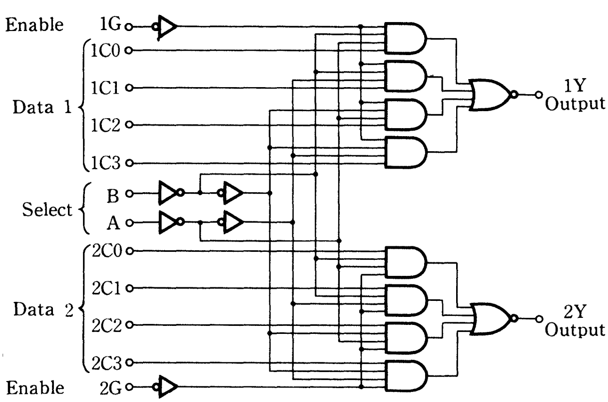
Select Inputs		Data Inputs				Enable	Output
B	A	C0	C1	C2	C3	G	Y
×	×	×	×	×	×	H	H
L	L	L	×	×	×	L	H
L	L	H	×	×	×	L	L
L	H	×	L	×	×	L	H
L	H	×	H	×	×	L	L
H	L	×	×	L	×	L	H
H	L	×	×	H	×	L	L
H	H	×	×	×	L	L	H
H	H	×	×	×	H	L	L

Note:
1. ×: Either HIGH or LOW; it doesn't matter

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input/output voltage			V_I, V_O	−0.5~V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65~+150	℃
Power dissipation	MN74HC352	Ta=−40~+60℃	P_D	400	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC352S	Ta=−40~+60℃	P_D	275	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

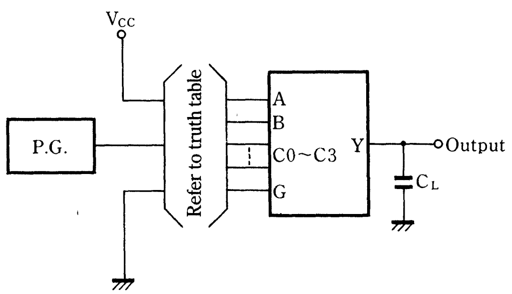
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

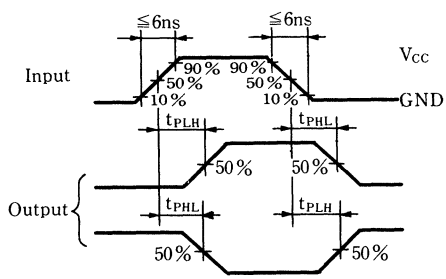
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time A, B→Y (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			18	30		38	
		6.0				26		33	
Propagation time A, B→Y (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
Propagation time G→Y (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
Propagation time G→Y (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
Propagation time C→Y (L→H)	t_{PLH}	2.0				175		220	ns
		4.5			19	35		44	
		6.0				30		37	
Propagation time C→Y (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			20	35		44	
		6.0				30		37	

- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



2. Switching Waveforms



MN74HC353/MN74HC353S

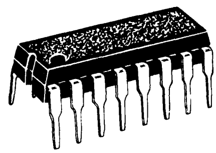
Dual 4-Channel TRI-STATE Multiplexers (Inverted Output)

■ Description

MN74HC353/MH74HC353S contain dual 4-channel tri-state multiplexers (Inverted Output) in one chip, selecting one input from four channel data input. The output control input controls two sets of four lines respectively. When output control is "H", output becomes high impedance regardless of bus line. When output control input is "L", the output channel suited to the data input signal from select input A or B is selected, the data is inverted and transferred to the output.

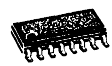
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



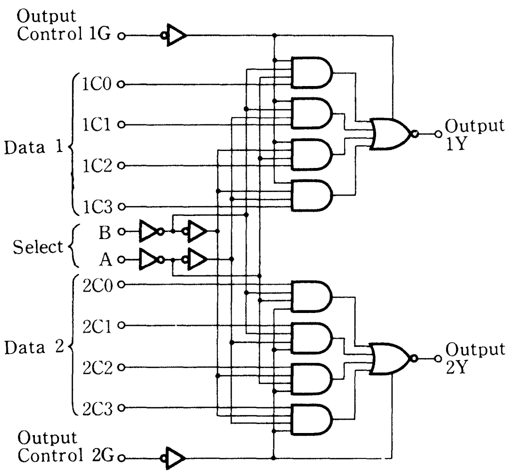
16-pin plastic DIL package

P-4

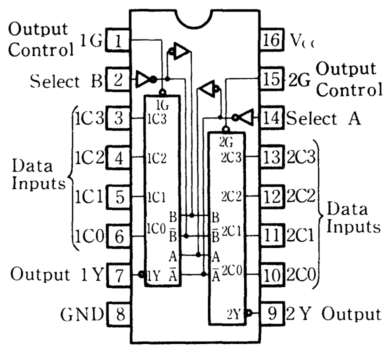


16-pin Panaflat package (SO-16D)

■ Logic Diagram



Pin configuration (top view)



■ Truth Table

Input							Output
Select		Data				Output Control	
B	A	C0	C1	C2	C3	G	Y
×	×	×	×	×	×	H	Hi-Z
L	L	L	×	×	×	L	H
L	L	H	×	×	×	L	L
L	H	×	L	×	×	L	H
L	H	×	H	×	×	L	L
H	L	×	×	L	×	L	H
H	L	×	×	H	×	L	L
H	H	×	×	×	L	L	H
H	H	×	×	×	H	L	L

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance

■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC353	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC353S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
						Ta=25℃			Ta=$-40\sim+85$℃		
			V_I	I_O	Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
		6.0	or	-20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	$V_I=V_{IH}$ or V_{IL}, $V_O=V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

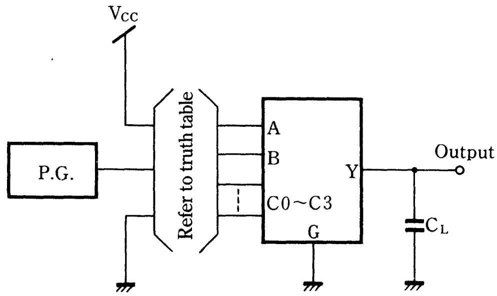
■ **AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)**

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time A,B→Y (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			18	30		38	
		6.0				26		33	
Propagation time A,B→Y (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
Propagation time C→Y (L→H)	t_{PLH}	2.0				175		220	ns
		4.5			19	35		44	
		6.0				30		37	
Propagation time C→Y (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			18	30		38	
		6.0				26		33	
3-state propagation time (H→Z)	t_{PHZ}	2.0				125		155	ns
		4.5	R_L=1kΩ		15	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0				125		155	ns
		4.5	R_L=1kΩ		15	25		31	
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L=1kΩ		11	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				175		220	ns
		4.5	R_L=1kΩ		19	35		44	
		6.0				30		37	

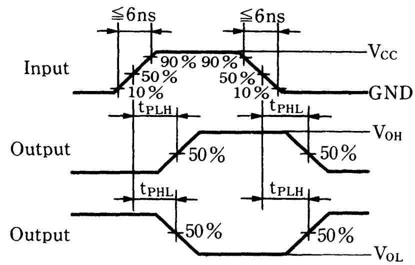
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1 Measuring Circuit

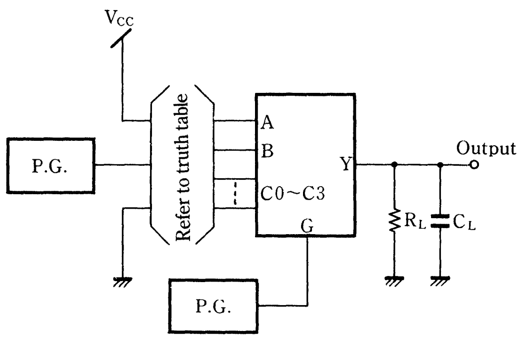


2. Waveforms

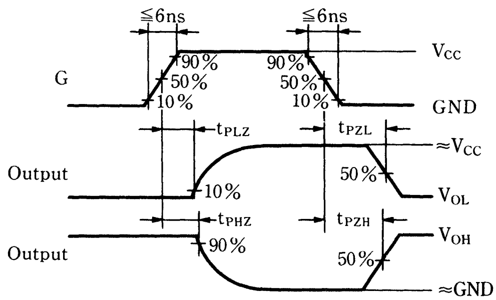


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

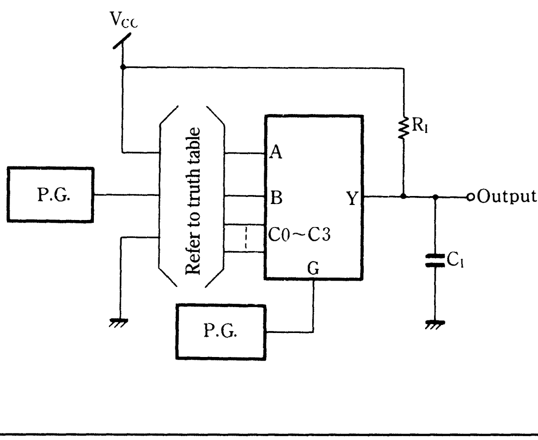


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

MN74HC365/MN74HC365S

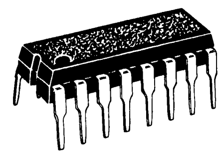
Hex TRI-STATE Buffers

■ Description

MN74HC365/MN74HC365S are high-speed non-inverted buffers consisting of six tri-state outputs. Large current output makes possible high-speed operation for driving a large capacity bus line. The hex gate can be simultaneously controlled by two tri-state control inputs ($\overline{G}_1$ and $\overline{G}_2$) when output becomes enabled at LOW level.

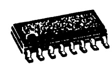
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



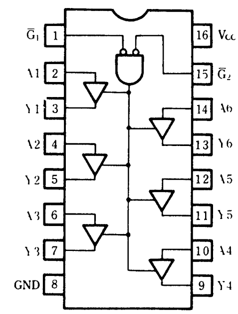
16-pin Panaflat package (SO-16D)

■ Truth Table

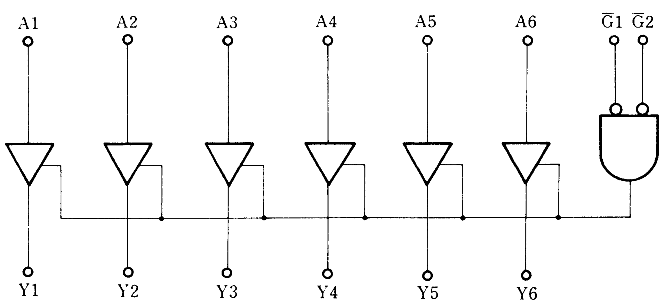
Input			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	×	×	Hi-Z
×	H	×	Hi-Z
L	L	H	H
L	L	L	L

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC365	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC365S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=$-40\sim+85$℃ min.	Ta=$-40\sim+85$℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	$V_I=V_{IH}$ or V_{IL}, $V_O=V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

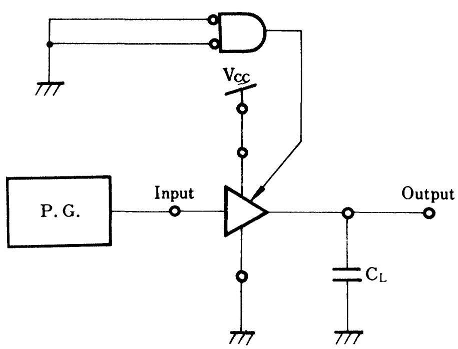
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Temperature Ta=25℃ typ.	Temperature Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	
		4.5			7	15		19	ns
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	
		4.5			6	15		19	ns
		6.0				13		16	
Propagation time (L→H)	t_{PLH}	2.0				75		95	
		4.5			8	15		19	ns
		6.0				13		16	
Propagation time (H→L)	t_{PHL}	2.0				75		95	
		4.5			7	15		19	ns
		6.0				13		16	
3-state propagation time (H→Z)	t_{PHZ}	2.0				100		125	
		4.5	R_L = 1 kΩ		12	20		25	ns
		6.0				17		21	
3-state propagation time (L→Z)	t_{PLZ}	2.0				125		155	
		4.5	R_L = 1 kΩ		16	25		31	ns
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	
		4.5	R_L = 1 kΩ		11	20		25	ns
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	
		4.5	R_L = 1 kΩ		13	20		25	ns
		6.0				17		21	

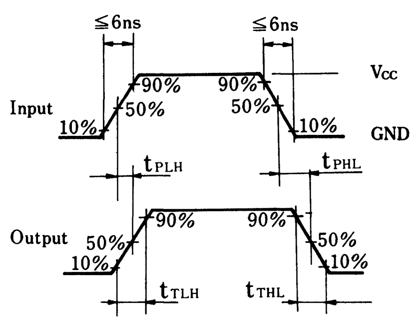
● Switching Time Measuring Circuit and Waveforms

[1] t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit (t_{PLH}, t_{PHL})

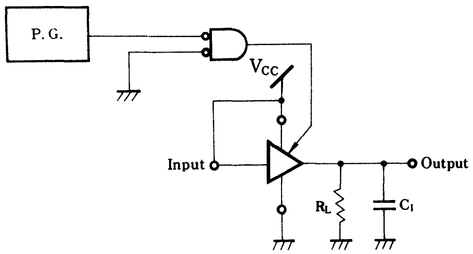


2. Waveforms

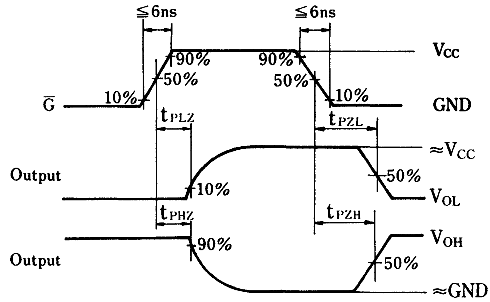


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

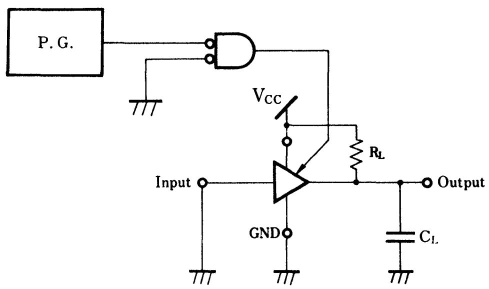


2. Waveforms



〔3〕 t_{PLZ}/t_{PZL}

1 1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

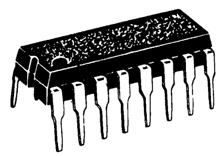
MN74HC366/MN74HC366S

Inverting Hex TRI-STATE Buffers

■ Description

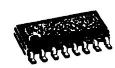
MN74HC366/MN74HC366S are high-speed inverting buffers consisting of six tri-state outputs. Large current output makes possible high-speed operation for driving a large capacity bus line.
Six gates can be simultaneously controlled by two tri-state control inputs ($\overline{G}_1$ and $\overline{G}_2$) where output becomes enable at LOW.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and family as standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



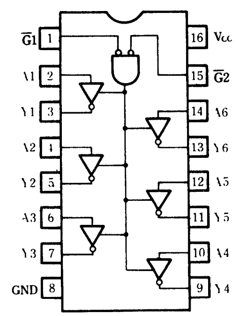
16-pin Panaflat package (SO-16D)

■ Truth Table

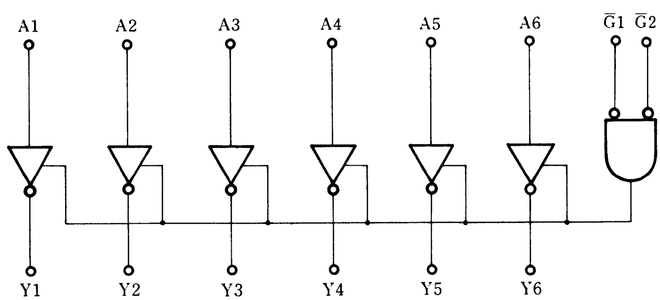
Input			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	×	×	Hi-Z
×	H	×	Hi-Z
L	L	H	L
L	L	L	H

Note:
1. X: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC366	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC366S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=$-40\sim+85$℃ min.	Ta=$-40\sim+85$℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
		6.0	or	-20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	$V_I=V_{IH}$ or V_{IL} $V_O=V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

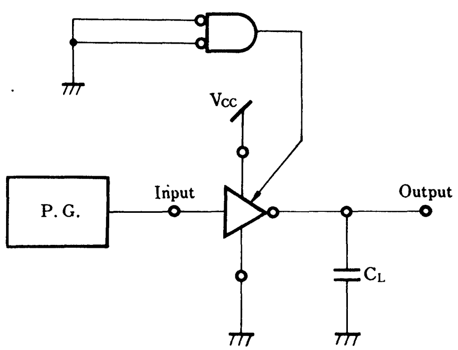
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40∼+85℃ min.	Ta=−40∼+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time (L→H)	t_{PLH}	2.0				75		95	ns
		4.5			9	15		19	
		6.0				13		16	
Propagation time (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Propagation time (H→Z)	t_{PHZ}	2.0				100		125	ns
		4.5	R_L = 1 kΩ		13	20		25	
		6.0				17		21	
3-state propagation time (L→Z)	t_{PLZ}	2.0				150		190	ns
		4.5	R_L = 1 kΩ		18	30		38	
		6.0				26		33	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L = 1 kΩ		11	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	ns
		4.5	R_L = 1 kΩ		13	20		25	
		6.0				17		21	

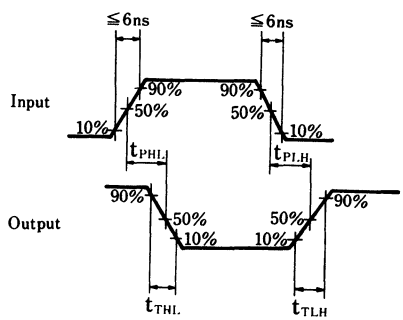
• Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit (t_{PLH}, t_{PHL})

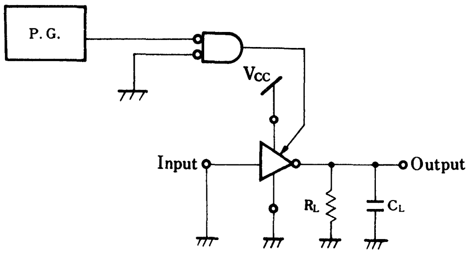


2. Waveforms

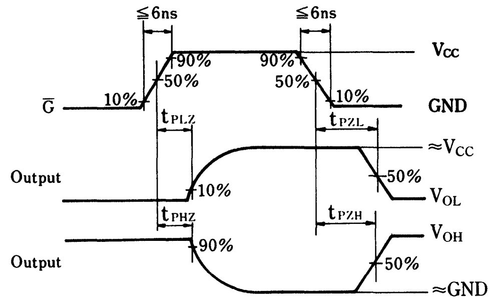


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

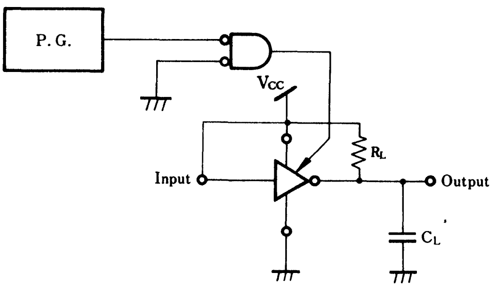


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

MN74HC367/MN74HC367S

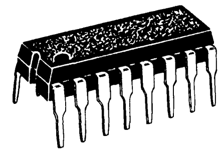
Hex TRI-STATE Buffers

■ Description

MN74HC367/MN74HC367S are high-speed non-inverted buffers consisting of six tri-state outputs. Large current output makes possible high-speed operation for driving a large bus line. Two inputs ($\overline{G}_1$ and $\overline{G}_2$) are available where output becomes enable at LOW, and $\overline{G}_1$ controls four gates and $\overline{G}_2$ controls two gates respectively.

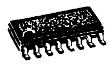
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



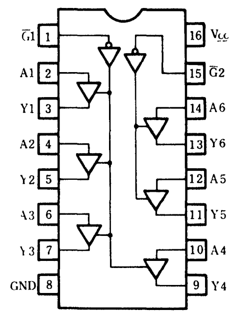
16-pin Panaflat package (SO-16D)

■ Truth Table

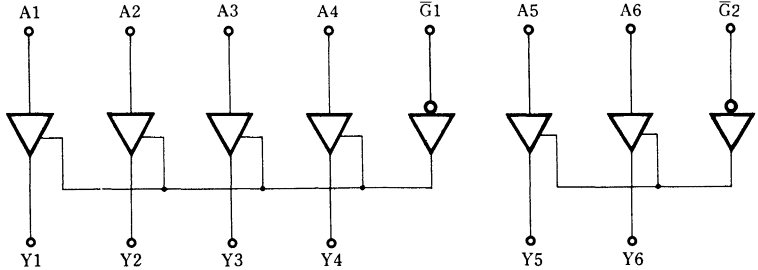
Input		Output
$\overline{G}$	A	Y
H	×	Hi-Z
L	H	H
L	L	L

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65 \sim +150$	℃
Power dissipation	MN74HC367	Ta $= -40 \sim +60$℃	P_D	400	mW
		Ta $= +60 \sim +85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC367S	Ta $= -40 \sim +60$℃	P_D	275	mW
		Ta $= +60 \sim +85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4 \sim 6.0$	V
Input/output voltage	V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature range	T_A		$-40 \sim +85$	℃
Input rise and fall time	t_r, t_f	2.0	$0 \sim 1000$	ns
		4.5	$0 \sim 500$	ns
		6.0	$0 \sim 400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	$V_I = V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	$V_I = V_{IH}$ or V_{IL}, $V_O = V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CC}$ or GND, $I_O = 0$					8.0		80.0	μA

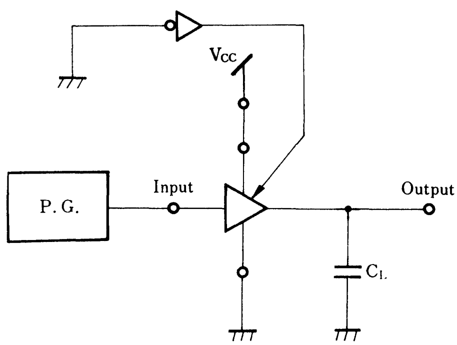
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time (L→H)	t_{PLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Propagation time (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
3-state propagation time	t_{PHZ}	2.0				100		125	ns
		4.5	R_L = 1 kΩ		12	20		25	
		6.0				17		17	
3-state propagation time	t_{PLZ}	2.0				100		125	ns
		4.5	R_L = 1 kΩ		13	20		25	
		6.0				17		17	
3-state propagation time	t_{PZH}	2.0				75		95	ns
		4.5	R_L = 1 kΩ		9	15		19	
		6.0				13		16	
3-state propagation time	t_{PZL}	2.0				75		95	ns
		4.5	R_L = 1 kΩ		10	15		19	
		6.0				13		16	

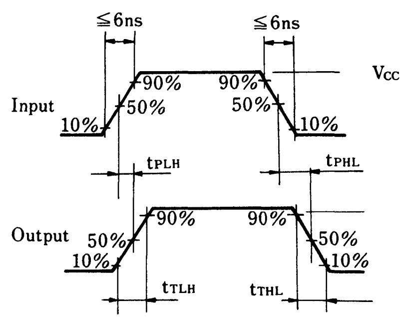
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

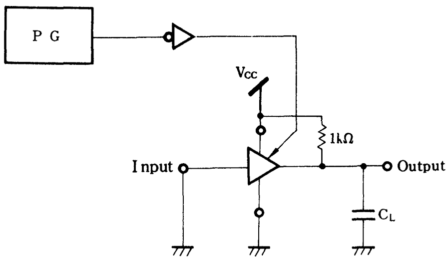


2. Waveforms

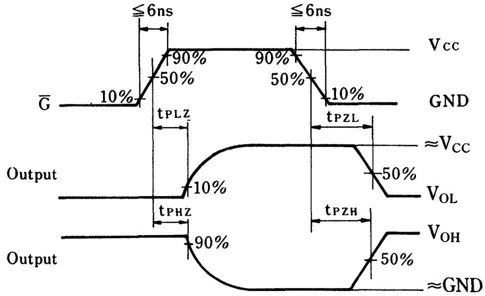


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

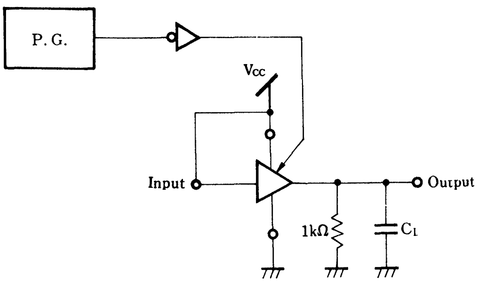


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

MN74HC368/MN74HC368S

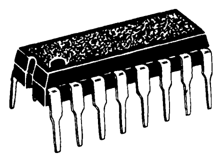
Inverting Hex TRI-STATE Buffers

■ Description

MN74HC368/MN74HC368S are high-speed inverting buffers consisting of six tri-state outputs. Large current output makes possible high-speed operating for driving a large capacitance bus line. Two inputs ($\overline{G}_1$ and $\overline{G}_2$) are available where output becomes enable at LOW, and $\overline{G}_1$ controls four gates and $\overline{G}_2$ controls two gates respectively.

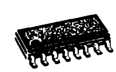
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



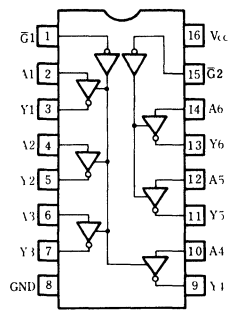
16-pin Panaflat package (SO-16D)

■ Truth Table

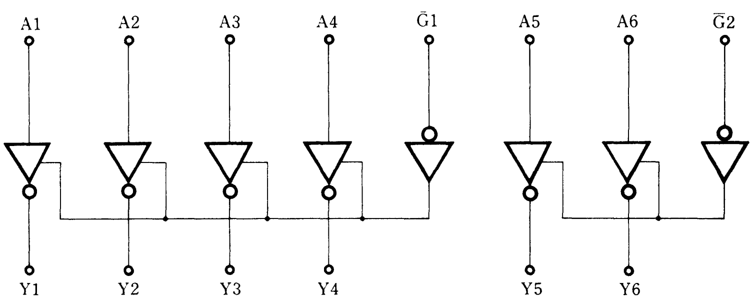
Input		Output
$\overline{G}$	A	Y
H	×	Hi-Z
L	H	L
L	L	H

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC368	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC368S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=$-40\sim+85$℃ min.	Ta=$-40\sim+85$℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	-20.0	μA	1.9	2.0		1.9		V
		4.5		-20.0	μA	4.4	4.5		4.4		
		6.0		-20.0	μA	5.9	6.0		5.9		
		4.5		-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	$V_I=V_{IH}$ or V_{IL}, $V_O=V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

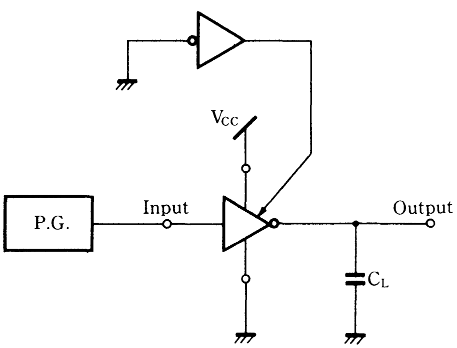
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40〜+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time (L→H)	t_{PLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Propagation time (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
3-state propagation time	t_{PHZ}	2.0				125		155	ns
		4.5	R_L= 1 kΩ		13	25		31	
		6.0				21		26	
3-state propagation time	t_{PLZ}	2.0				125		155	ns
		4.5	R_L= 1 kΩ		12	25		31	
		6.0				21		26	
3-state propagation time	t_{PZH}	2.0				100		125	ns
		4.5	R_L= 1 kΩ		9	20		25	
		6.0				17		21	
3-state propagation time	t_{PZL}	2.0				100		125	ns
		4.5	R_L= 1 kΩ		10	20		25	
		6.0				17		21	

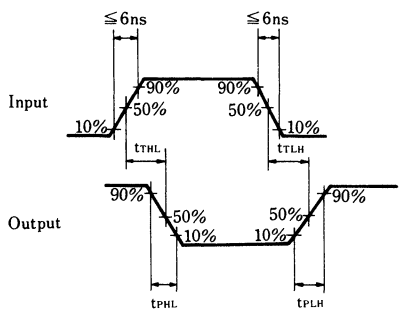
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

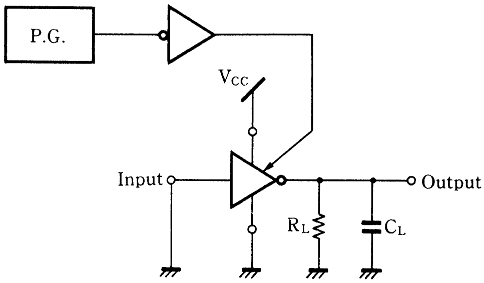


2. Waveforms

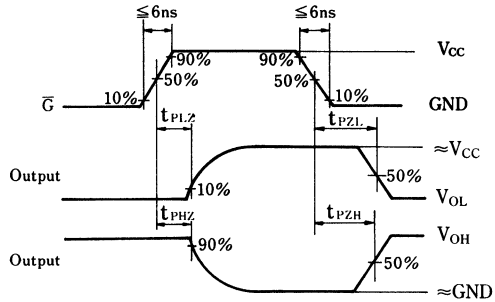


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

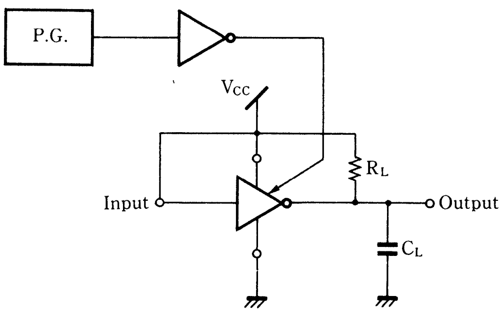


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

MN74HC373/MN74HC373S

Octal TRI-STATE D-Type Latches

■ Description

MN74HC373/MN74HC373S contain octal tri-state D-type latches. High output driving capacity and tri-state outputs are suited for the use of a common bus line in the bus utilized system. When output disable input is "L" and latch enable input is "H", the output outputs the data input. When latch enable is "L", data input is maintained as is until when latch enable input becomes "H" again. Output disable input is "H", all inputs become high impedance state, regardless of other inputs and data-hold circuit.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

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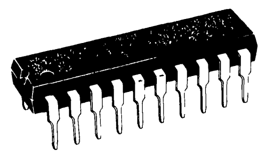
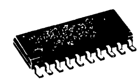


20-pin plastic DIL package

P-6



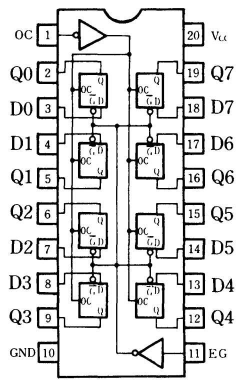
20-pin Panaflat package (SO-20D)

■ Truth Table

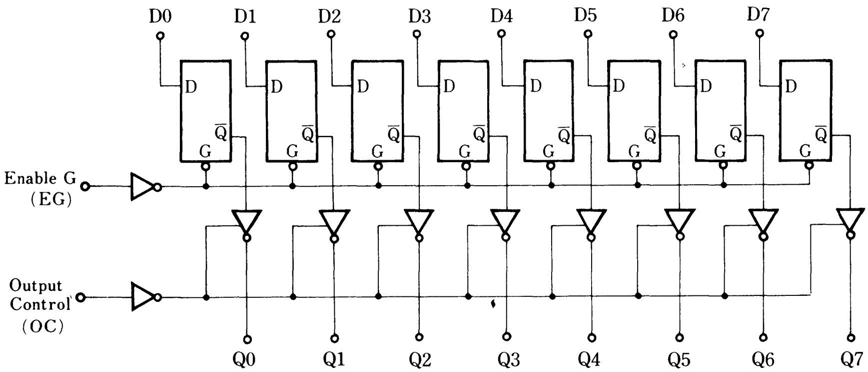
Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	×	Q_0
H	×	×	Hi-Z

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance
3. Q_O: Q level prior to determination of input condition shown in table

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC373	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC373S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=−40～+85℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

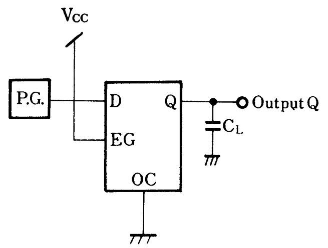
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time D→Q (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
Propagation time D→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time Enable G→Q(L→H)	t_{PLH}	2.0				175		220	ns
		4.5			19	35		44	
		6.0				30		37	
Propagation time Enable G→Q(H→L)	t_{PHL}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
3-state propagation time (H→Z)	t_{PHZ}	2.0				150		190	ns
		4.5	R_L = 1 kΩ		17	30		38	
		6.0				26		33	
3-state propagation time (L→Z)	t_{PLZ}	2.0				150		190	ns
		4.5	R_L = 1 kΩ		18	30		38	
		6.0				26		33	
3-state propagation time (Z→H)	t_{PZH}	2.0				125		155	ns
		4.5	R_L = 1 kΩ		14	25		31	
		6.0				21		26	
3-state propagation time (Z→L)	t_{PZL}	2.0				125		155	ns
		4.5	R_L = 1 kΩ		15	25		31	
		6.0				21		26	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			2	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	

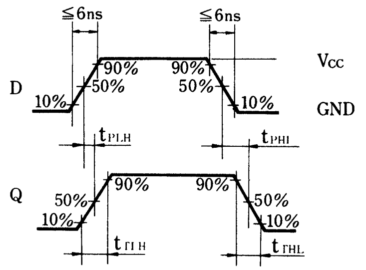
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}/t_{PHL}(D→Q)

1. Measuring Circuit

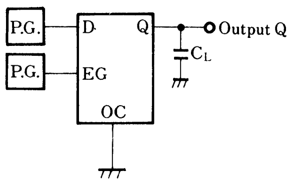


2. Waveforms

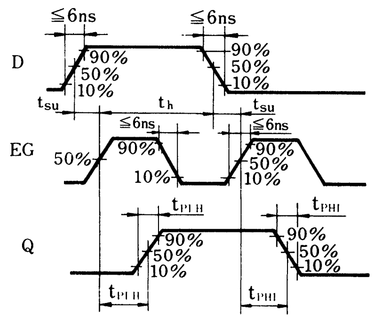


〔2〕 t_{PLH}/t_{PHL}(ENG→Q), t_{su}, t_h

1. Measuring Circuit

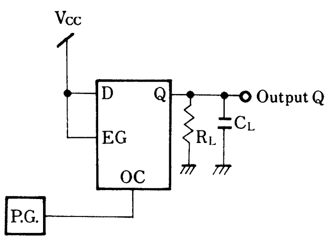


2. Waveforms

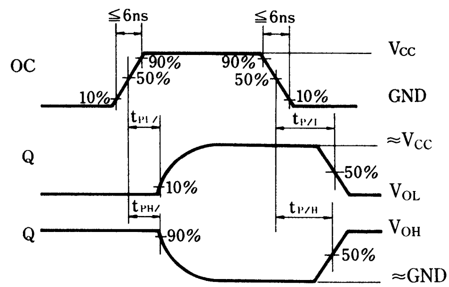


〔3〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

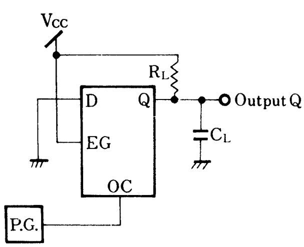


2. Waveforms



〔4〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [3] 2. for waveforms.

MN74HC374/MN74HC374S

Octal TRI-STATE D-Type Flip-Flops

■ Description

MN74HC374/MN74HC374S contain eight high speed D-type flip-flops with tri-state outputs.
High output driving capability and tri-state outputs are suited for the use of a common bus line in the bus utilized system.
D input data satisfying set-up time is transferred to the output on the positive-going edge of clock input. When output disable input is HIGH, all outputs become high impedance state regardless of other input data and the data-hold circuit.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity.
Same pin configuration and function as standard 54LS/74LS logic family.

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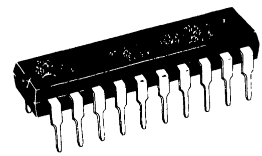
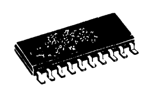


20-pin plastic DIL package

P-6



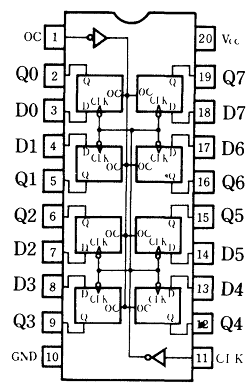
20-pin Panaflat package (SO-20D)

■ Truth Table

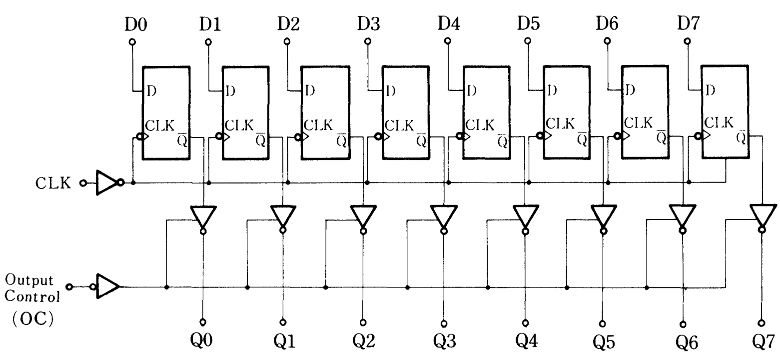
Input			Output
Output Control	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	×	Q_0
H	×	×	Hi-Z

Note:
1. ↑ : Data input is transferred to output on the positive-going edge from LOW to HIGH
2. ×: Either HIGH or LOW; it doesn't matter
3. Q_0: Q level prior to determination of input condition shown in table
4. Hi-Z High impedance

Pin Configuration (top view)



■ Logic Diagram (1 gate)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	± 20	mA
Output parasitic diode current			I_{OK}	± 20	mA
Output current			I_O	± 35	mA
Supply current			I_{CC}, I_{GND}	± 70	mA
Storage temperature range			Tstg	$-65 \sim +150$	℃
Power dissipation	MN74HC374	Ta $= -40 \sim +60$ ℃	P_D	400	mW
		Ta $= +60 \sim +85$ ℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC374S	Ta $= -40 \sim +60$ ℃	P_D	275	mW
		Ta $= +60 \sim +85$ ℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Item	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4 \sim 6.0$	V
Input/output voltage	V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature range	T_A		$-40 \sim +85$	℃
Input rise and fall time	t_r, t_f	2.0	$0 \sim 1000$	ns
		4.5	$0 \sim 500$	ns
		6.0	$0 \sim 400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25℃			Ta=−40~+85℃		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	$V_I = V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	$V_I = V_{IH}$ or V_{IL}, $V_O = V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CC}$ or GND, $I_O = 0$					8.0		80.0	μA

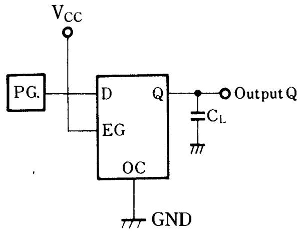
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time CLK→Q (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			18	30		38	
		6.0				26		33	
Propagation time CLK→Q (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			19	30		38	
		6.0				26		33	
3-state propagation time (H→Z)	t_{PHZ}	2.0				150		190	ns
		4.5	R_L = 1 kΩ		18	30		38	
		6.0				26		33	
3-state propagation time (L→Z)	t_{PLZ}	2.0				150		190	ns
		4.5	R_L = 1 kΩ		18	30		38	
		6.0				26		33	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L = 1 kΩ		13	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				125		155	ns
		4.5	R_L = 1 kΩ		15	25		31	
		6.0				21		26	
Minimum pulse width	t_{su}	2.0				75		95	ns
		4.5			2	15		19	
		6.0				13		16	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30	64		24		
		6.0		35			28		

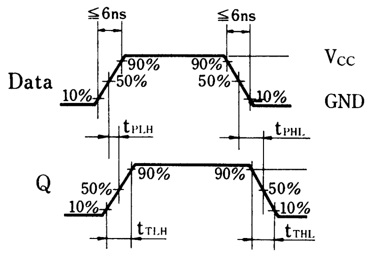
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}/t_{PHL}(D→Q)

1. Measuring Circuit

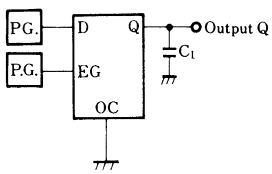


2. Waveforms

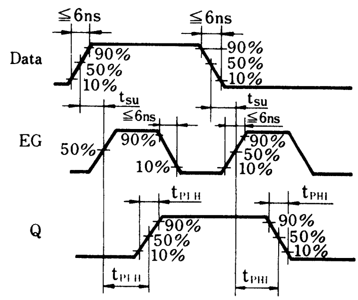


〔2〕 t_{PLH}/t_{PHL}(ENG→Q)

1. Measuring Circuit

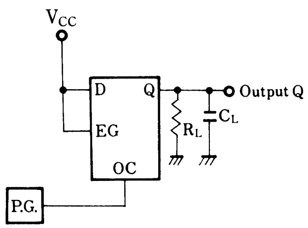


2. Waveforms

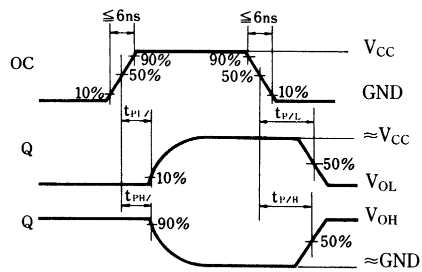


〔3〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

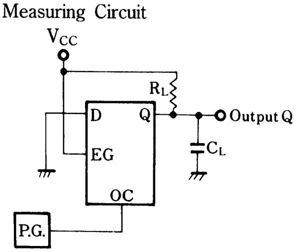


2. Waveforms (t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})



〔4〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



MN74HC375/MN74HC375S

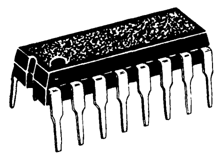
4-Bit Bistable Latches

■ Description

MN74HC375/MH74HC375S are bistable latches with four bit Q, $\overline{Q}$ output. These are suited for temporary binary data memory circuits between the data processing unit and the I/O, or between display units. Data at data input (D) are transferred to output Q when enable pin (G) is "H"; output Q follows the data input state so long as the enable is "H". When enable becomes "L", output Q is maintained as is until when the enable becomes "H". Output Q indicates the data input state when the enable changes from "H" to "L".

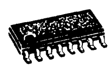
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



16-pin plastic DIL package

P-4



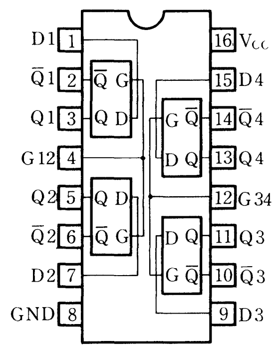
16-pin Panaflat package (SO-16D)

■ Truth Table

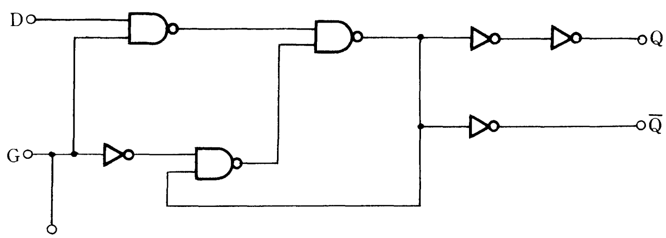
Input		Output	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
×	L	Q_O	$\overline{Q}_O$

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Q_O: Q level prior to determination of input condition shown in table
3. $\overline{Q}_O$ Q level prior to determination of input condition shown in table

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC375	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC375S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=$-40\sim+85$℃ min.	Ta=$-40\sim+85$℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	-20.0	μA	1.9	2.0		1.9		V
		4.5		-20.0	μA	4.4	4.5		4.4		
		6.0		-20.0	μA	5.9	6.0		5.9		
		4.5		-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

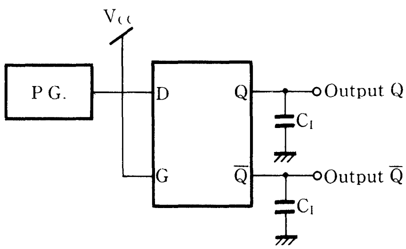
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40〜+85℃ min.	Ta=−40〜+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time D→Q (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			10	20		25	
		6.0				17		21	
Propagation time D→Q (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			11	20		25	
		6.0				17		21	
Propagation time D→$\overline{Q}$ (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			11	20		25	
		6.0				17		21	
Propagation time D→$\overline{Q}$ (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			9	20		25	
		6.0				17		21	
Propagation time G→Q (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			12	25		31	
		6.0				21		26	
Propagation time G→Q (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time G→$\overline{Q}$ (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time G→$\overline{Q}$ (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			10	25		31	
		6.0				21		26	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			2	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum pulse width	t_W	2.0				125		155	ns
		4.5			1	25		31	
		6.0				21		26	

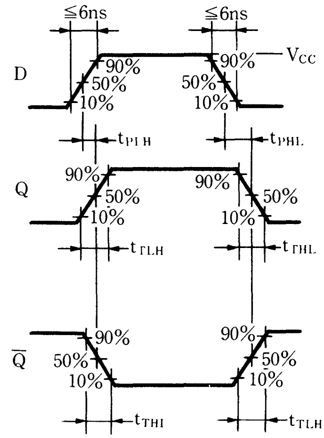
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}/t_{PHL} ($D \rightarrow Q, \bar{Q}$)

1. Measuring Circuit

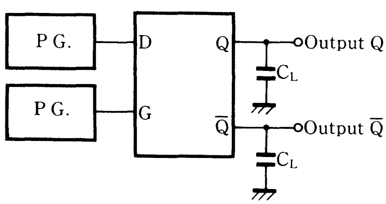


2. Waveforms

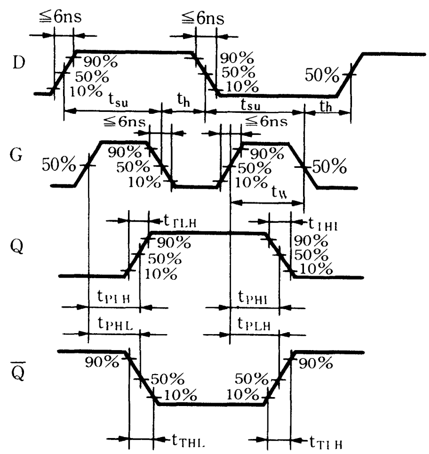


〔2〕 t_{PLH}/t_{PHL} ($G \rightarrow Q, \bar{Q}$), t_w, t_{su}, t_h

1. Measuring Circuit



2. Waveforms



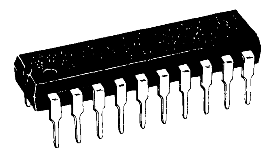
MN74HC377/MN74HC377S

Octal D-Type Flip-Flop with Enable Data

■ Description

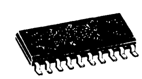
MN74HC377/377S contain eight high-speed D-type flip-flops with enable data.
D input data satisfying set-up time is transferred to the output Q on the rising edge of clock input, when enable data input $\overline{CE}$ is "L". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-5



20-pin plastic DIL package

P-6



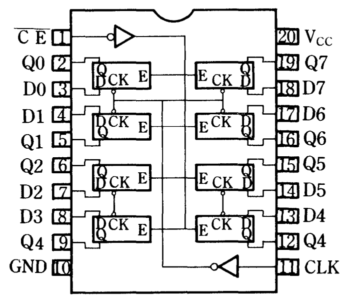
20-pin Panaflat package (SO-20D)

■ Truth Table

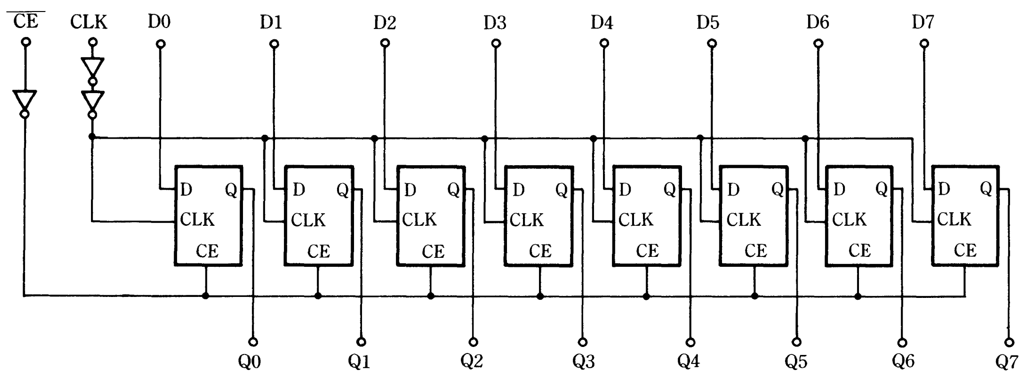
Operating Mode	Input			Output
	CLK	CE	Dn	Qn
Load "1"	↑	L	H	H
Load "0"	↑	L	L	L
Hold (Do nothing)	↑	H	×	No Change
	H	H	×	No Change

Note:
1. ↑: Data input is transferred to output on the positive-going edge from LOW to HIGH.
2. × : Either HIGH or LOW; it doesn't matter.

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	°C
Power dissipation	MN74HC377	Ta=−40～+60°C	P_D	400	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC377S	Ta=−40～+60°C	P_D	275	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	°C
Input rise and fall time	t_r, t_f	V_{CC}=2.0V	0～1000	ns
		V_{CC}=4.5V	0～500	ns
		V_{CC}=6.0V	0～400	ns

■ DC Characteristics (GND=0V)

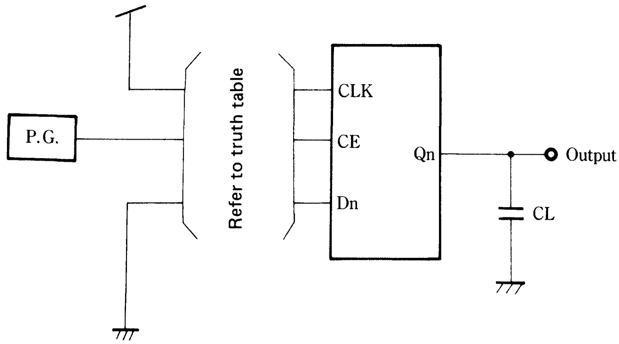
Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O	Unit	Ta=25°C			Ta=−40～+85°C		
						min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		V
		6.0				4.2			4.2		V
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	V
		6.0						1.2		1.2	V
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.5		V
		6.0		−20.0	μA	5.9	6.0		5.9		V
		4.5		−4.0	mA	3.86			3.76		V
		6.0		−5.2	mA	5.36			5.26		V
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	V
		6.0		20.0	μA		0.0	0.1		0.1	V
		4.5		4.0	mA			0.32		0.37	V
		6.0		5.2	mA			0.32		0.37	V
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±0.1	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

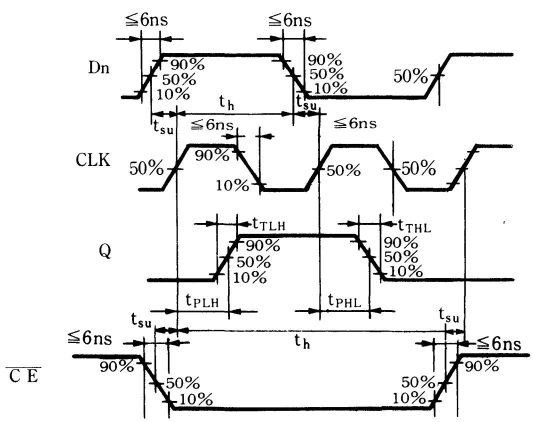
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25°C			Ta=−40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Propagation time CLK→D (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Propagation time CLK→D (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Minimum Set-up time D	t_{su}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum Set-up time CE	t_{su}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum Hold time D	t_h	2.0				0		0	ns
		4.5				0		0	
		6.0				0		0	
Minimum Hold time CE	t_h	2.0				0		0	ns
		4.5				0		0	
		6.0				0		0	
Minimum pulse width CLK	t_w	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30			24		
		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



MN74HCT377/MN74HCT377S

Octal D-Type Flip-Flop with Enable Data (TTL Input)

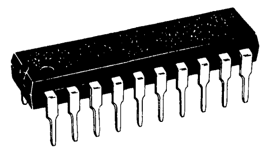
■ Description

MN74HCT377/MN74HCT377S contain eight high-speed D-type flip-flops with enable data. D input data satisfying set-up time is transferred to the output Q on the positive-going edge of clock input, when enable data input $\overline{CE}$ is "L".

All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2V or more is logic "1". Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven.

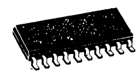
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-5



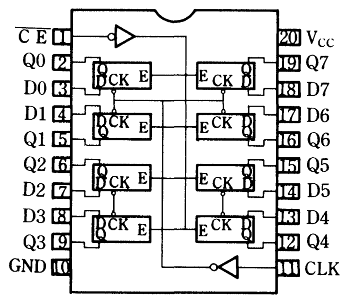
20-pin plastic DIL package

P-6



20-pin Panaflat package (SO-20D)

Pin Configuration (top view)

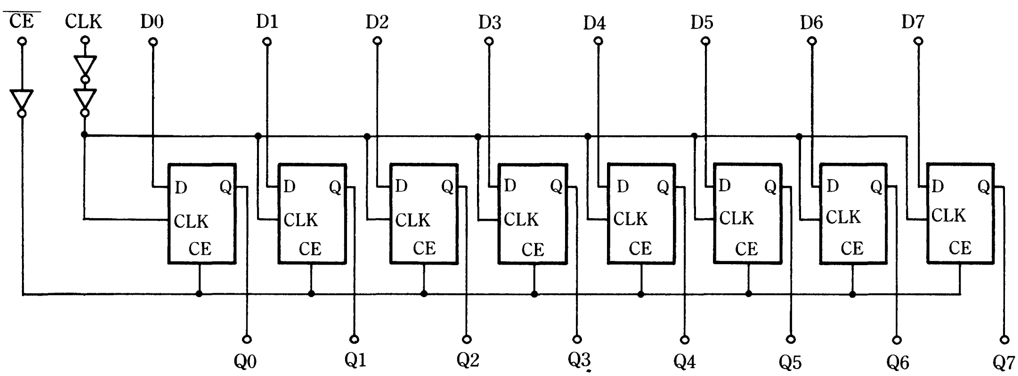


■ Truth Table

Operating Mode	Input			Output
	CLK	CE	Dn	Qn
Load "1"	↑	L	H	H
Load "0"	↑	L	L	L
Hold (Do nothing)	↑	H	×	No Change
	H	H	×	No Change

Note:
1. ↑: Data input is transferred to output on the positive-going edge from LOW to HIGH.
2. × : Either HIGH or LOW; it doesn't matter.

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	°C
Power dissipation	MN74HCT377	Ta=$-40\sim+60$°C	P_D	400	mW
		Ta=$+60\sim+85$°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HCT377S	Ta=$-40\sim+60$°C	P_D	275	mW
		Ta=$+60\sim+85$°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		$4.5\sim5.5$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	°C
Input rise and fall time	t_r, t_f	V_{CC}=4.5V	$0\sim500$	ns

■ DC Characteristics (GND=0V)

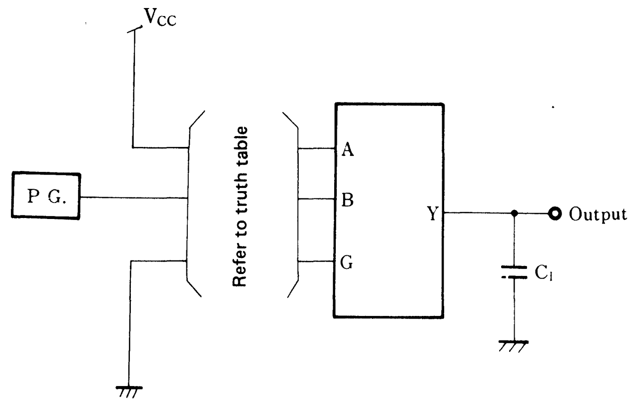
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Unit	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=$-40\sim+85$°C min.	Ta=$-40\sim+85$°C max.	Unit
Input HIGH voltage	V_{IH}	4.5 ~ 5.5				2.0			2.0		V
Input LOW voltage	V_{IL}	4.5 ~ 5.5						0.8		0.8	V
Output HIGH voltage	V_{OH}	4.5	V_{IH} or V_{IL}	−20.0	μA	4.4	4.5		4.4		V
		4.5		−4.0	mA	3.86			3.76		V
Output LOW voltage	V_{OL}	4.5	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		4.0	mA			0.32		0.37	V
Input current	I_I	5.5	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	5.5	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

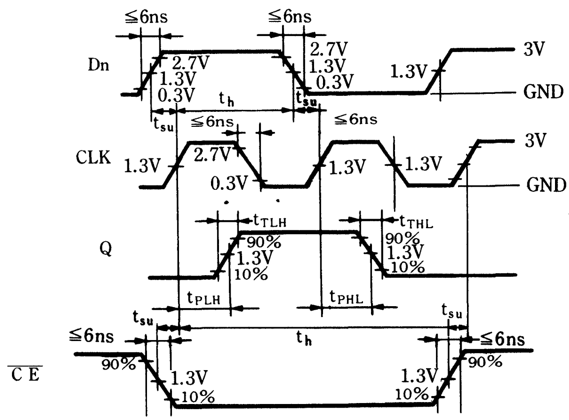
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25°C min.	Temperature Ta=25°C typ.	Temperature Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Output rise time	t_{TLH}	4.5				15		19	ns
Output fall time	t_{THL}	4.5				15		19	ns
Propagation time CLK→D (L→H)	t_{PLH}	4.5				30		38	ns
Propagation time CLK→D (H→L)	t_{PHL}	4.5				30		38	ns
Minimum Set-up time D	t_{su}	4.5				20		25	ns
Minimum Set-up time CE	t_{su}	4.5				20		25	ns
Minimum Hold time D	t_h	4.5				0		0	ns
Minimum Hold time CE	t_h	4.5				0		0	ns
Minimum pulse width CLK	t_w	4.5				20		25	ns
Maximum clock frequency	f_{max}	4.5		30			24		MHz

- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



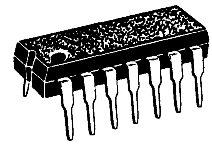
MN74HC386/MN74HC386S

Quad 2-Input Exclusive OR Gates

■ Description

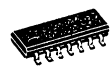
MN74HC386/MN74HC386S contain quad 2-input exclusive OR gates.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directry driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-1



14-pin plastic DIL package

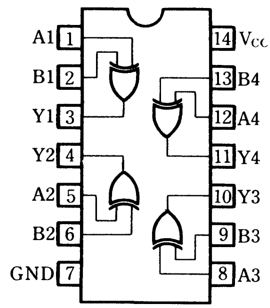
P-2



14-pin Panaflat package (SO-14D)

■ Logic Diagram (1 gate)

Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC386	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC386S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

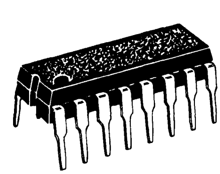
MN74HC390/MN74HC390S

Dual 4-Bit Decade Counters

■ Description

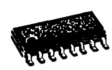
MN74HC390/MN74HC390S are independent ripple-carry counters consisting of two decade counters.
The decade counter consists of divide-by-two and divide-by-five counters. Divide-by-two and divide-by-five counters can have a maximum of divide-by-100 counters by using two decade counters or combinations.
This counter provides increments on the negative-going edge of clock input, and each has independent clear input. When the clear input is HIGH, all of the four outputs of each counter become LOW. The clear input decreases the count number and functions to make this counter a Modulo-N counter.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-3



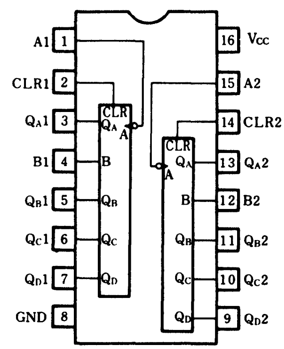
16-pin plastic DIL package

P-4

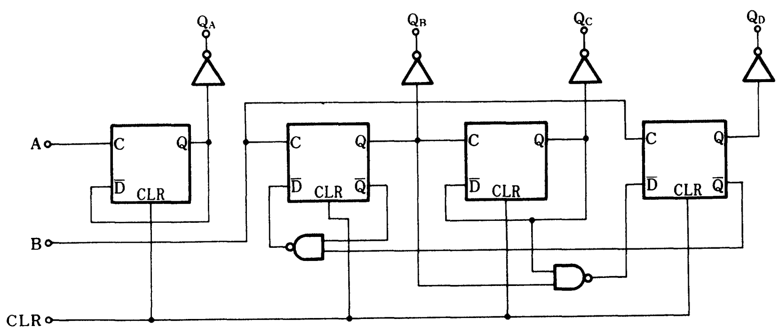


16-pin Panaflat package (SO-16D)

Pin Configuration (top view)



■ Logic Diagram



■ Truth Table

A or B	CLR	Output
×	H	L
↓	L	Count

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ↓: A(B) from "H" to "L"

※ Output Q_A to be connected to input B

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

※ Output Q_D to be connected to input A

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC390	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC390S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions: V_I	Test Conditions: I_O	Test Conditions: Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

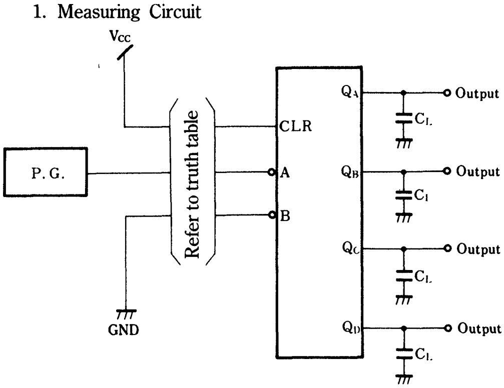
Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time A→Q_A (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
Propagation time A→Q_A (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
Propagation time A→Q_C (L→H)	t_{PLH}	2.0				325		406	ns
		4.5			38	65		81	
		6.0				55		69	
Propagation time A→Q_C (H→L)	t_{PHL}	2.0				325		406	ns
		4.5			38	65		81	
		6.0				55		69	

■ AC Characteristics (Cont'd)

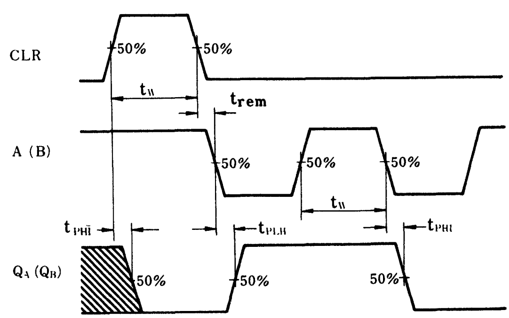
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40～+85℃ min.	max.	Unit
Propagation time B→Q_B (L→H)	t_{PLH}	2.0				175		220	ns
		4.5			22	35		44	
		6.0				30		37	
Propagation time B→Q_B (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			18	30		38	
		6.0				26		33	
Propagation time B→Q_C (L→H)	t_{PLH}	2.0				200		250	ns
		4.5			24	40		50	
		6.0				34		43	
Propagation time B→Q_C (H→L)	t_{PHL}	2.0				200		250	ns
		4.5			24	40		50	
		6.0				34		43	
Propagation time B→Q_D (L→H)	t_{PLH}	2.0				175		220	ns
		4.5			20	35		44	
		6.0				30		37	
Propagation time B→Q_D (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
Propagation time CLR→Q (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			20	35		44	
		6.0				30		37	
Minimum pulse width CLK(A),CLK(B),CLR	t_W	2.0				125		155	ns
		4.5			5	25		31	
		6.0				21		26	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5			3	15		19	
		6.0				13		16	
Maximum clock frequency A, B	f_{max}	2.0		6			4		MHz
		4.5		30	81		24		
		6.0		35			28		

● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



2. Waveforms



MN74HC393/MN74HC393S

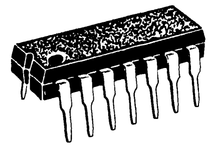
Dual 4-Bit Binary Counters

■ Description

MN74HC393/MN74HC393S are independent ripple-carry counters consisting of two independent 4-bit ripple-carry binary counters which can be subsidiarily connected to one divide-by-256 counter.

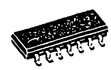
This counter provides increments on the negative-going edge of clock input, and each has independent clear input. When the clear input is HIGH, all of the four outputs of each counter become LOW. The clear input decrease the count number and functions to make this counter a Modulo-N counter. Adoption of a silicon gate CMOS process has realized a low power dissipation, high noise margin equivalent to a standard CMOS and operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family. family.

P-1



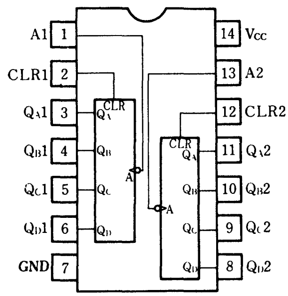
14-pin plastic DIL package

P-2

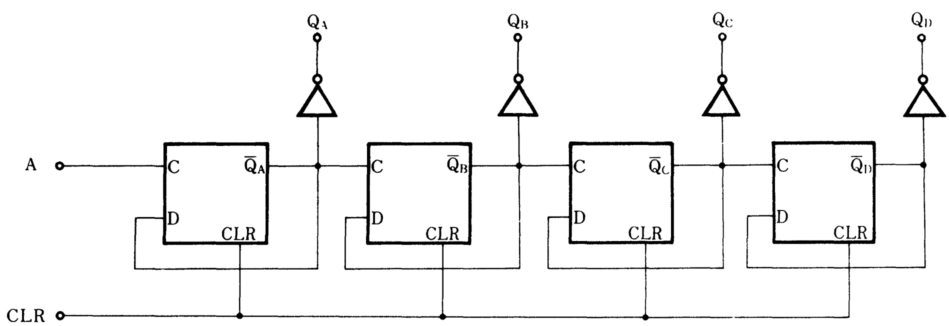


14-pin Panaflat package (SO-14D)

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC393	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC393S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

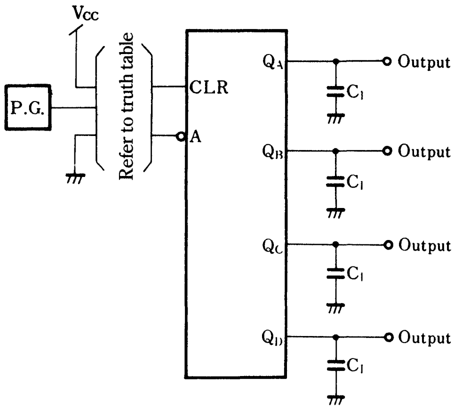
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

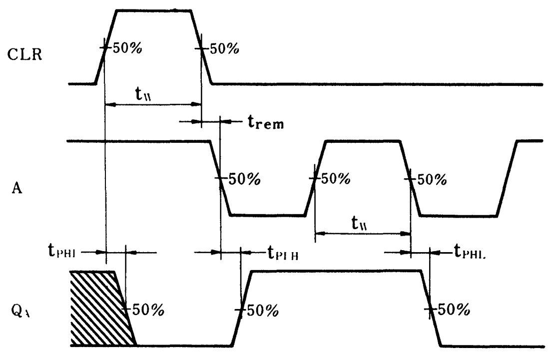
Parameter	Symbol	V_{CC} (V)	Test Condition	Temperature					Unit
				Ta=25℃			Ta=−40〜+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0			20	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			15	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time A→Q_A (L→H)	t_{PLH}	2.0			27	100		120	ns
		4.5			12	20		24	
		6.0			9	17		20	
Propagation time A→Q_A (H→L)	t_{PHL}	2.0			24	100		120	ns
		4.5			10	20		24	
		6.0			9	17		20	
Propagation time A→Q_D (L→H)	t_{PLH}	2.0			53	175		220	ns
		4.5			22	35		44	
		6.0			15	30		37	
Propagation time A→Q_D (H→L)	t_{PHL}	2.0			53	175		220	ns
		4.5			22	35		44	
		6.0			15	30		37	
Propagation time CLR→Q (H→L)	t_{PHL}	2.0			33	150		190	ns
		4.5			17	30		38	
		6.0			14	26		33	
Minimum pulse width CLK, CLR	t_W	2.0			16	75		95	ns
		4.5			18	15		19	
		6.0			7	13		16	
Minimum Set-up time	t_{rem}	2.0			10	75		95	ns
		4.5			4	15		19	
		6.0			3	13		16	
Maximum clock frequency	f_{max}	2.0		6	38		5		MHz
		4.5		30	68		24		
		6.0		35	98		28		

• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



■ Truth Table

A	CLR	Output
×	H	L
⌝_	L	Count

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ⌝_ : count on the negative-going edge from HIGH to LOW of A

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

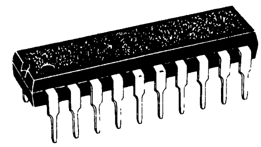
MN74HC533/MN74HC533S

Octal TRI-STATE D-Type Latches with Inverting Outputs

■ Description

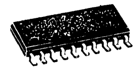
MN74HC533/MN74HC533S contain eight high-speed D-type latches with inverting tri-state outputs. High output driving capability and tri-state outputs are suitable for the use of a common bus line in a bus utilized system.
When output disable input is LOW and latch enable input is HIGH, the output outputs the inverting data input state.
When latch enable is LOW, the data input data is held in the output until when latch enable input becomes HIGH.
When output disable input is HIGH, all outputs become high impedance state regardless of the state of other inputs and data hold circuits.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

P-5



20-pin plastic DIL package

P-6



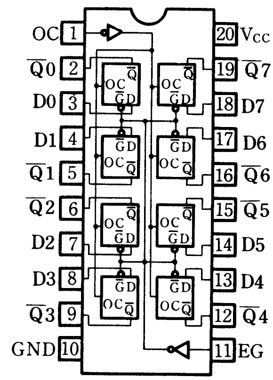
20-pin Panaflat package (SO-20D)

■ Truth Table

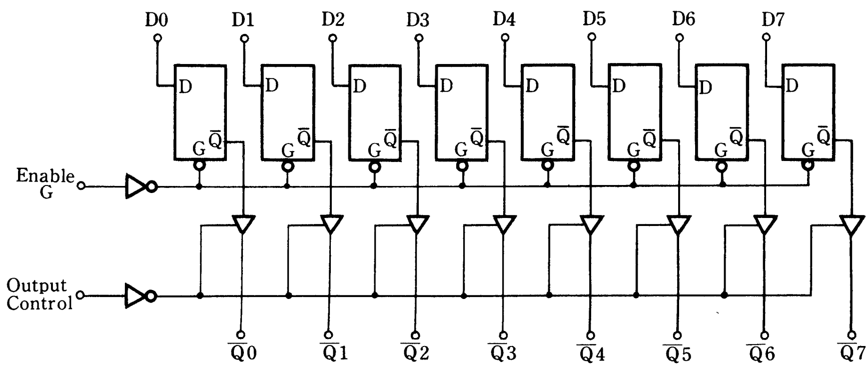
Output Control	Enable G	D	Output
L	H	H	L
L	H	L	H
L	L	×	Q_0
H	×	×	Hi-Z

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance
3. Q_O: Q level prior to determination of input condition shown in tabel

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC533	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC533S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

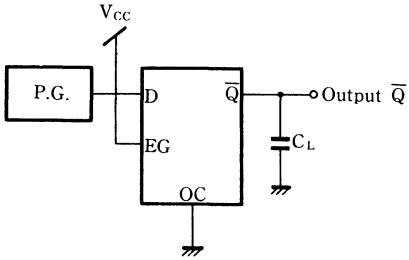
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time D→$\overline{Q}$ (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			13	20		25	
		6.0				17		21	
Propagation time D→$\overline{Q}$ (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
Propagation time Enable G→$\overline{Q}$(L→H)	t_{PLH}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
Propagation time Enable G→$\overline{Q}$(H→L)	t_{PHL}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
3-state propagation time (H→Z)	t_{PHZ}	2.0				125		155	ns
		4.5	R_L = 1 kΩ		14	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0				125		155	ns
		4.5	R_L = 1 kΩ		10	25		31	
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L = 1 kΩ		10	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	ns
		4.5	R_L = 1 kΩ		12	20		25	
		6.0				17		21	
Minimum Set-up time	t_{su}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	

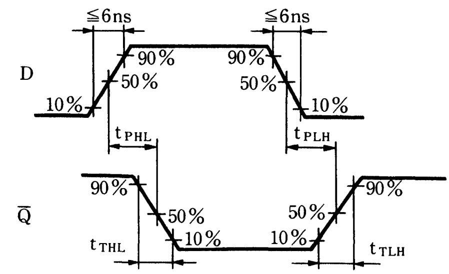
• Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}/t_{PHL}(D→$\overline{Q}$)

1. Measuring Circuit

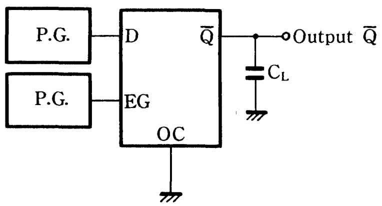


2. Waveforms

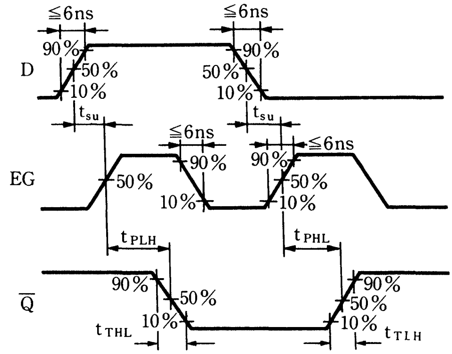


〔2〕 t_{PLH}/t_{PHL}(EG→$\overline{Q}$), t_{su}

1. Measuring Circuit

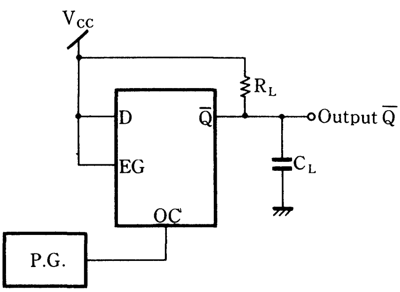


2. Waveforms

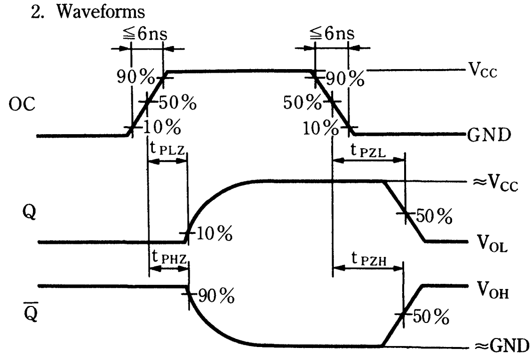


〔3〕t_{PHZ}, t_{PZH}

1. Measuring Circuit

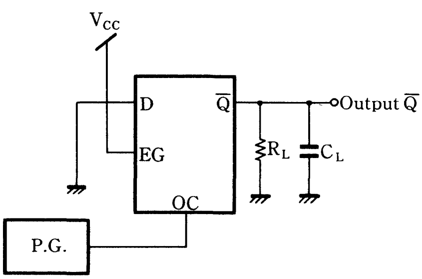


2. Waveforms



〔4〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [3] 2. for waveforms.

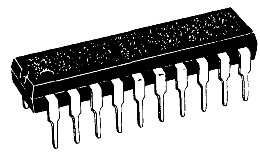
MN74HC534/MN74HC534S

Octal TRI-STATE D-Type Flip-Flops with Inverting Outputs

■ Description

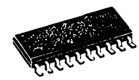
MN74HC534/MN74HC534S contain eight high-speed D-type flip-flops with inverting tri-state outputs. High output driving capability and tri-state outputs are suitable for the use of a common bus line in a bus utilized system. D input data satisfying set-up time is inverted and transferred to the output on the positive going edge of clock input.
When output disable input is HIGH, all outputs become high impedance state regardless of the state of other inputs and data hold circuits.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

P-5



20-pin plastic DIL package

P-6



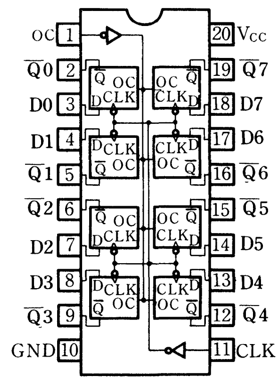
20-pin Panaflat package (SO-20D)

■ Truth Table

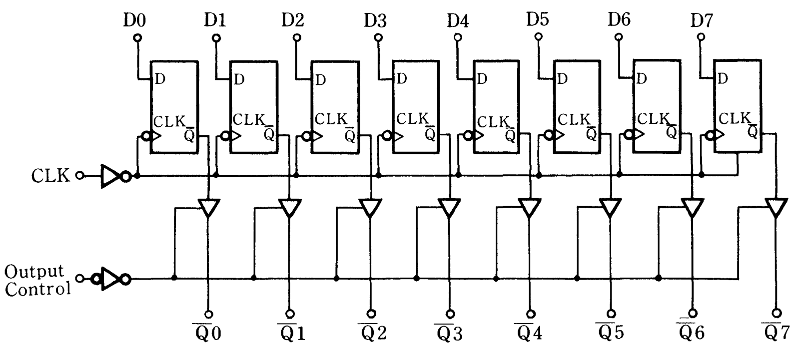
Input			Output
Output Control	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	×	$\overline{Q}_0$
H	×	×	Hi-Z

Note:
1. ↑: Data input is transferred to output on the negative-going edge from LOW to HIGH of the clock
2. ×: Either HIGH or LOW; it doesn't matter
3. Q_O: Q level prior to determination of input condition shown in table
4. Hi-Z: High impedance

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC534	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC534S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=$-40\sim+85$℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	-20.0	μA	1.9	2.0		1.9		V
		4.5		-20.0	μA	4.4	4.5		4.4		
		6.0		-20.0	μA	5.9	6.0		5.9		
		4.5		-6.0	mA	3.86			3.76		
		6.0		-7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	$V_I=V_{IH}$ or V_{IL}, $V_O=V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

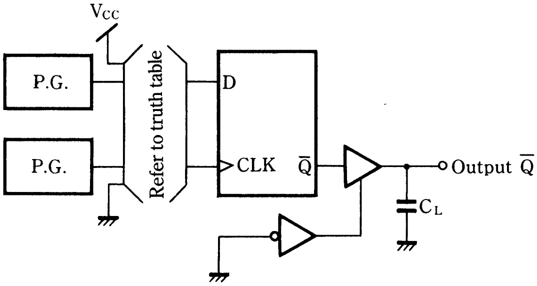
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40〜+85℃ min.	Ta=−40〜+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time CLK→$\overline{Q}$ (L→H)	t_{PLH}	2.0							ns
		4.5			17	30			
		6.0							
Propagation time CLK→$\overline{Q}$ (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
3-state propagation time (H→Z)	t_{PHZ}	2.0				150		190	MHz
		4.5	R_L=1kΩ		17	30		38	
		6.0				26		33	
3-state propagation time (L→Z)	t_{PLZ}	2.0				150		190	ns
		4.5	R_L=1kΩ		17	30		38	
		6.0				26		33	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L=1kΩ		12	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	ns
		4.5	R_L=1kΩ		13	20		25	
		6.0				17		21	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			2	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Maximum clock frequency	f_{max}	2.0		6			4		ns
		4.5		30	49		24		
		6.0		35			28		

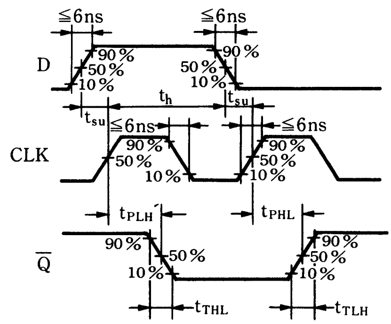
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}/t_{PHL}(CLK→$\overline{Q}$), t_{su}, f_{max}, t_h

1. Measuring Circuit

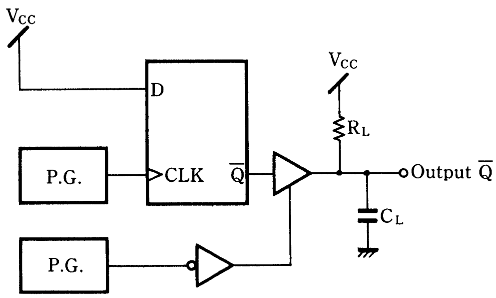


2. Waveforms

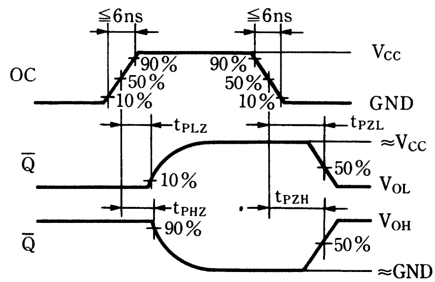


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

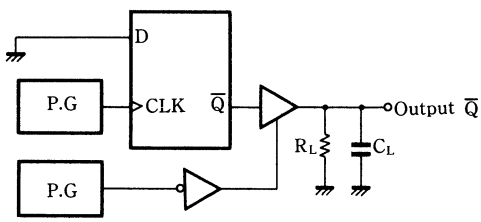


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

MN74HC540/MN74HC540S

Inverting Octal TRI-STATE Buffers Line Drivers

■ Description

MN74HC540/MN74HC540S are inverting octal tri-state buffers line drivers. Large current output make possible high-speed operation for driving a large capacity bus line. When one of 3-state control input ($\overline{G1}$, $\overline{G2}$) operated as 2 inputs NOR is "H", 8 outputs become high impedance.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

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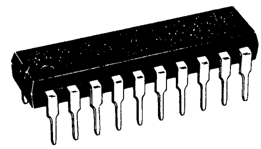
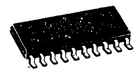


20-pin plastic DIL package

P-6



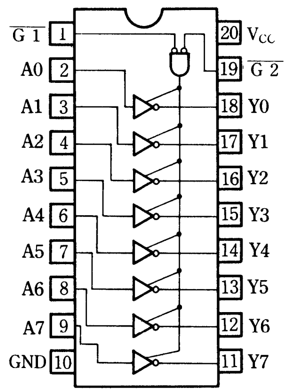
20-pin Panaflat package (SO-20D)

■ Truth Table

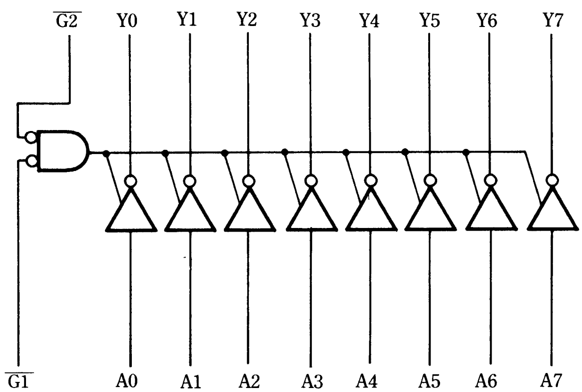
Input			Output
$\overline{G1}$	$\overline{G2}$	An	Yn
L	L	L	H
L	L	H	L
×	H	×	Z
H	×	×	Z

Note:
1. ×: Either HIGH or LOW; doesn't matter
2. Hi-Z: Hi-Impedance

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	°C
Power dissipation	MN74HC540	Ta=−40∼+60°C	P_D	400	mW
		Ta=+60∼+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC540S	Ta=−40∼+60°C	P_D	275	mW
		Ta=+60∼+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	°C
Input rise and fall time	t_r, t_f	V_{CC}=2.0V	$0\sim1000$	ns
		V_{CC}=4.5V	$0\sim500$	ns
		V_{CC}=6.0V	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25°C			Ta=−40∼+85°C		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		V
		6.0				4.2			4.2		V
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	V
		6.0						1.2		1.2	V
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		V
		6.0	or	−20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	−6.0	mA	3.86			3.76		V
		6.0		−7.8	mA	5.36			5.26		V
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	6.0	mA			0.32		0.37	V
		6.0		7.8	mA			0.32		0.37	V
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	0.6	$V_I=V_{IH}$ or VIL $V_O=V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

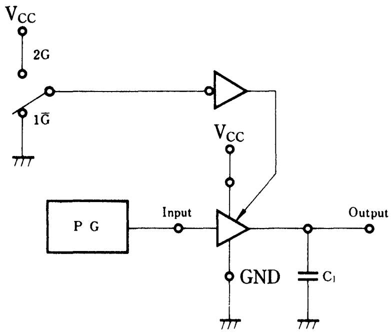
■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Output rise time	t_{TLH}	2.0			28	75		95	ns
		4.5			12	15		19	
		6.0			10	13		16	
Output fall time	t_{THL}	2.0			22	75		95	ns
		4.5			9	15		19	
		6.0			7	13		16	
Propagation time (L→H)	t_{PLH}	2.0			39	90		115	ns
		4.5			14	18		23	
		6.0			12	15		20	
Propagation time (H→L)	t_{PHL}	2.0			40	90		115	ns
		4.5			14	18		23	
		6.0			11	15		20	
3-stage output off leakage current (H→Z)	t_{PHZ}	2.0	R_L=1kΩ		46	140		175	ns
		4.5			22	28		35	
		6.0			19	24		30	
3-stage output off leakage current (L→Z)	t_{PLZ}	2.0	R_L=1kΩ		44	140		175	ns
		4.5			17	28		35	
		6.0			19	24		30	
3-stage output off leakage current (Z→H)	t_{PZH}	2.0	R_L=1kΩ		62	140		175	ns
		4.5			23	28		35	
		6.0			18	24		30	
3-stage output off leakage current (Z→L)	t_{PZL}	2.0	R_L=1kΩ		62	140		175	ns
		4.5			23	28		35	
		6.0			18	24		30	

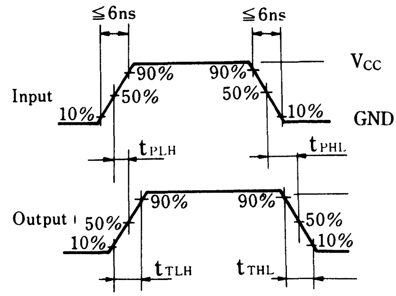
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

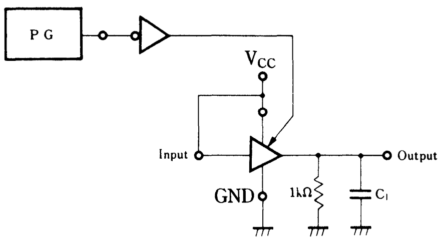


2. Waveforms

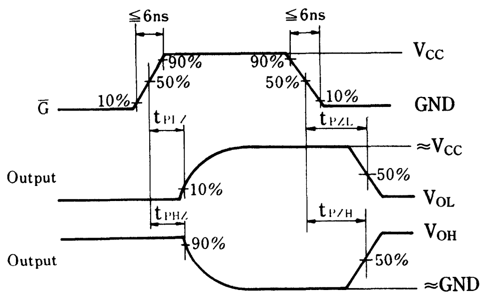


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

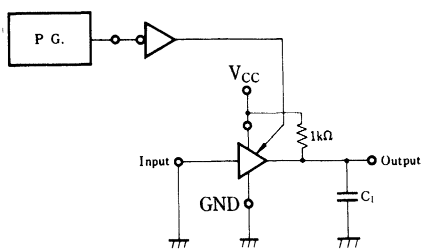


2. Waveforms (t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



MN74HC541/MN74HC541S

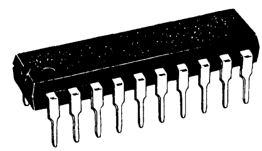
Octal TRI-STATE Buffers Line Drivers

■ Description

MN74HC541/MN74HC541S are octal tri-state buffers line drivers. Large current output make possible high-speed operation for driving a large capacity bus line. When one of 3-state control input ($\overline{G}1$, $\overline{G}2$) operated as inputs NOR is "H". 8 outpurs become high impedance

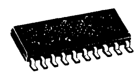
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-5



20-pin plastic DIL package

P-6



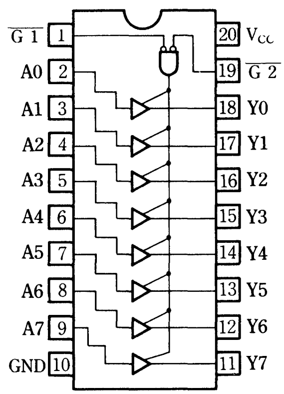
20-pin Panaflat package (SO-20D)

■ Truth Table

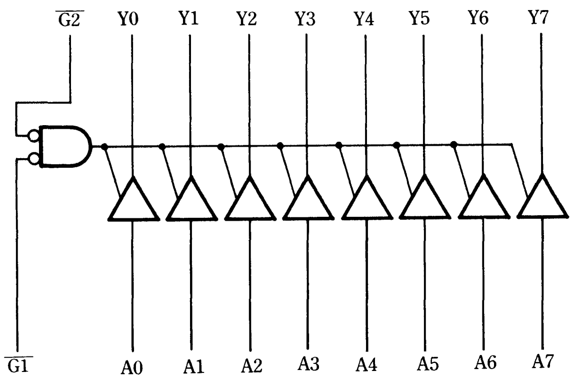
Input			Output
$\overline{G}1$	$\overline{G}2$	An	Yn
L	L	L	H
L	L	H	L
×	H	×	Z
H	×	×	Z

Note:
1. ×: Either HIGH or LOW; doesn't matter
2. Hi-Z: Hi-Impedance

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	°C
Power dissipation	MN74HC541	Ta=$-40\sim+60$°C	P_D	400	mW
		Ta=$+60\sim+85$°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC541S	Ta=$-40\sim+60$°C	P_D	275	mW
		Ta=$+60\sim+85$°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	°C
Input rise and fall time	t_r, t_f	V_{CC}=2.0V	$0\sim1000$	ns
		V_{CC}=4.5V	$0\sim500$	ns
		V_{CC}=6.0V	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25°C			Ta=$-40\sim+85$°C		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		V
		6.0				4.2			4.2		V
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	V
		6.0						1.2		1.2	V
Output HIGH voltage	V_{OH}	2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		V
		6.0	or	-20.0	μA	5.9	6.0		5.9		V
		4.5	V_{IL}	±6.0	mA	3.86			3.76		V
		6.0		-7.8	mA	5.36			5.26		V
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		6.0	or	20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IL}	6.0	mA			0.32		0.37	V
		6.0		7.8	mA			0.32		0.37	V
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	0.6	$V_I=V_{IH}$ or V_{IL} $V_O=V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

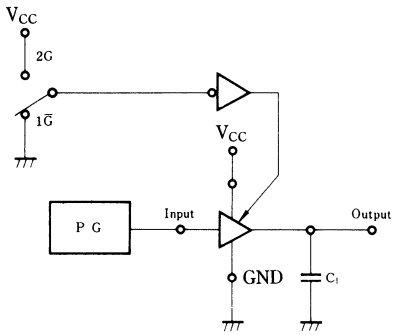
■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25°C			Ta=−40∼+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0			27	75		95	ns
		4.5			12	15		19	
		6.0			10	13		16	
Output fall time	t_{THL}	2.0			26	75		95	ns
		4.5			10	15		19	
		6.0			7	13		16	
Propagation time (L→H)	t_{PLH}	2.0			33	90		115	ns
		4.5			13	18		23	
		6.0			11	15		20	
Propagation time (H→L)	t_{PHL}	2.0			36	90		115	ns
		4.5			13	18		23	
		6.0			10	15		20	
3-stage output off leakage current (H→Z)	t_{PHZ}	2.0	R_L=1kΩ		42	140		175	ns
		4.5			23	28		35	
		6.0			20	24		30	
3-stage output off leakage current (L→Z)	t_{PLZ}	2.0	R_L=1kΩ		40	140		175	ns
		4.5			16	28		35	
		6.0			13	24		30	
3-stage output off leakage current (Z→H)	t_{PZH}	2.0	R_L=1kΩ		59	140		175	ns
		4.5			21	28		35	
		6.0			17	24		30	
3-stage output off leak current (Z→L)	t_{PZL}	2.0	R_L=1kΩ		63	140		175	ns
		4.5			22	28		35	
		6.0			17	24		30	

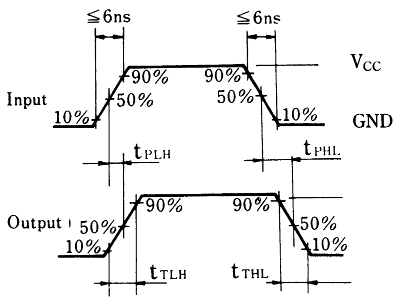
● Switching Time Measurng Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

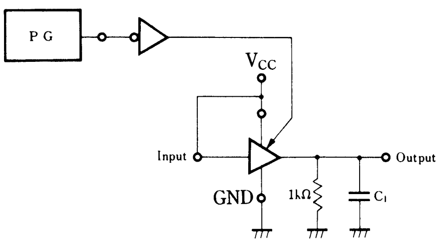


2. Waveforms

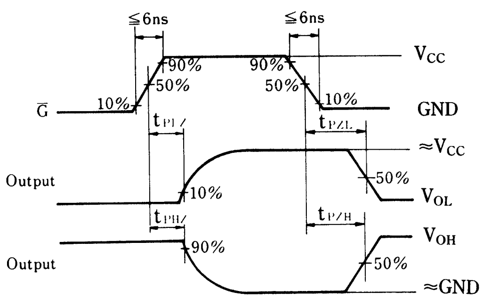


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

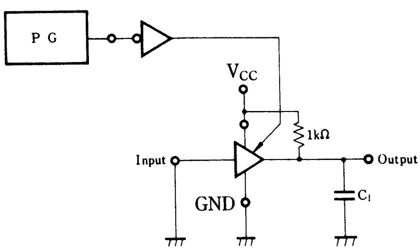


2. Waveforms (t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



MN74HC563/MN74HC563S

Octal TRI-STATE D-Type Latches with Inverting Outputs

■ Description

MN74HC563/MN74HC563S contain eight high-speed D-type latches with inverting tri-state outputs. High output driving capability and tri-state outputs are suitable for the use of a common bus line in a bus utilized system.
When output disable input is LOW and latch enable input is HIGH, the output outputs the inverting data input state.
When latch enable is LOW, the data input is held in the output until when latch enable input becomes HIGH.
When output disable input is HIGH, all outputs become high impedance state regardless of the state of other inputs and data hold circuits.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

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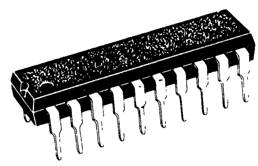
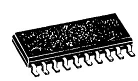


20-pin plastic DIL package

P-6



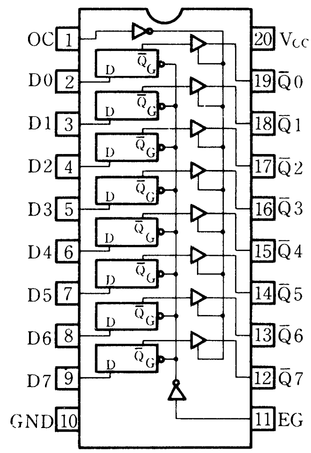
20-pin Panaflat package (SO-20D)

■ Truth Table

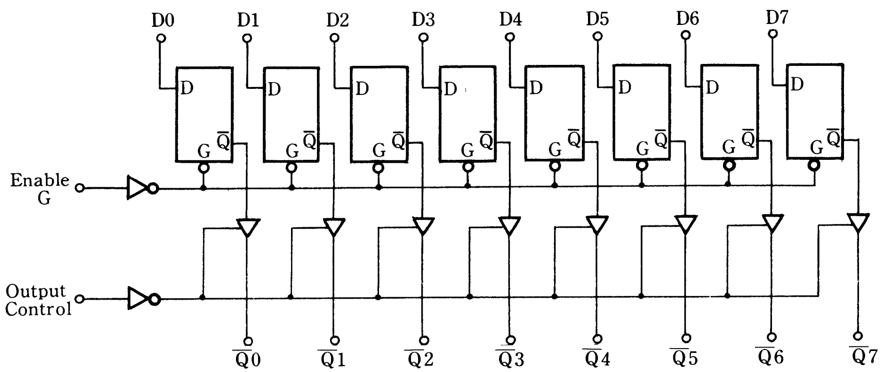
Input			Output
Output Control	Enable G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	×	$\overline{Q}_0$
H	×	×	Hi-Z

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance
3. $\overline{Q}_0$: Q level prior to determination of input condition shown in table

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC536	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC536S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Ratıng	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25℃			Ta=−40～+85℃		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL} V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

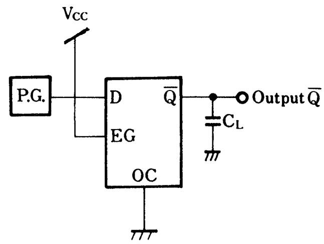
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time D→$\overline{Q}$ (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
Propagation time D→$\overline{Q}$ (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
E Propagation time Enable G→$\overline{Q}$(L→H)	t_{PLH}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
E Propagation time Enable G→$\overline{Q}$(H→L)	t_{PHL}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	
3-state propagation time (H→Z)	t_{PHZ}	2.0				125		155	ns
		4.5	R_L = 1 kΩ		14	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0				125		155	ns
		4.5	R_L = 1 kΩ		10	25		31	
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L = 1 kΩ		9	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				125		155	ns
		4.5	R_L = 1 kΩ		13	25		31	
		6.0				21		36	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			1	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	

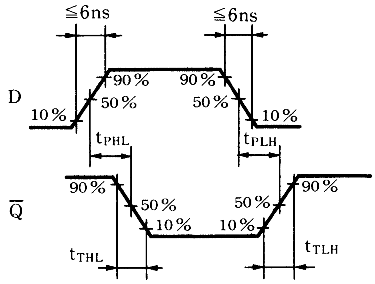
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}/t_{PHL}(D→$\overline{Q}$)

1. Measuring Circuit (t_{PLH}, t_{PHL})

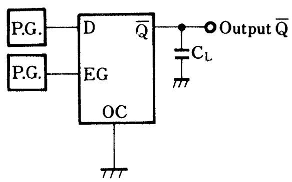


2. Waveforms

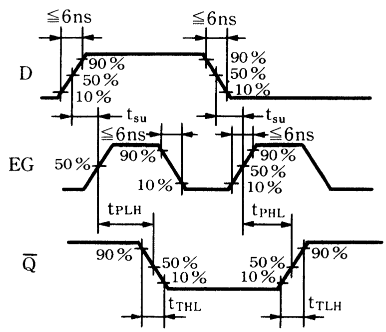


〔2〕 t_{PLH}/t_{PHL}(EG→$\overline{Q}$)

1. Measuring Circuit (t_{PLH}, t_{PHL})

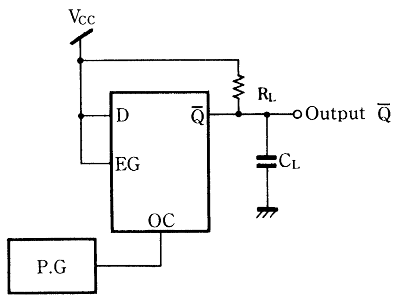


2. Waveforms

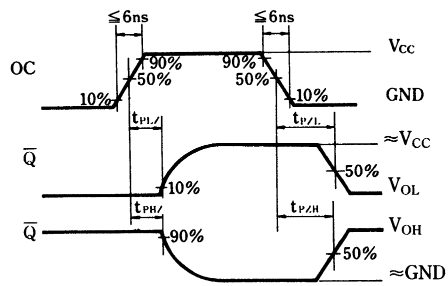


〔3〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit (t_{PLH}, t_{PHL})

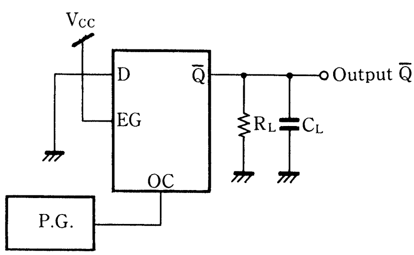


2. Waveforms



〔4〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms

See above [3] 2. for waveforms.

MN74HC564/MN74HC564S

Octal TRI-STATE D-Type Flip-Flops with Inverting Outputs

■ Description

MN74HC564/MN74HC564S contain eight high-speed D-type latches with inverting tri-state outputs. High output driving capability and tri-state outputs are suitable for the use of a common bus line in a bus utilized system. D input data satisfying set-up time is inverted and transferred to the output on the positive going edge of clock input.

When output disable input is HIGH, all outputs become high impedance state regardless of the state of other inputs and data hold circuits.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

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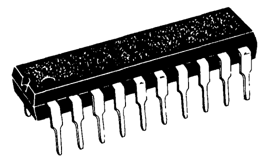
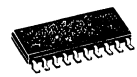


20-pin plastic DIL package

P-6



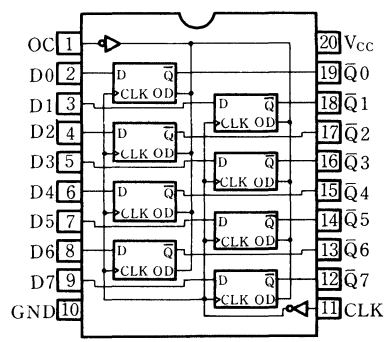
20-pin Panaflat package (SO-20D)

■ Truth Table

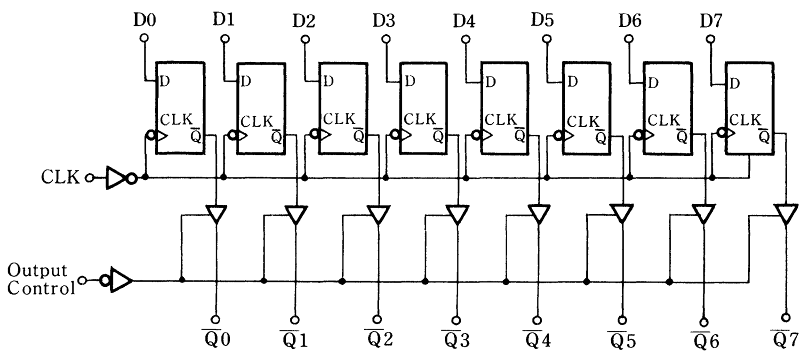
Input			Output
Output Control	CLK	D	$\overline{Q}$
L	↑	L	L
L	↑	H	H
L	L	×	$\overline{Q}_0$
H	×	×	Hi-Z

Note:
1. ↑: Data input is transferred to output on the positive-going edge from LOW to HIGH of the clock
2. ×: Either HIGH or LOW; it doesn't matter
3. Q_O: Q level prior to determination of input condition shown in table
4. HI-Z: High impedance

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC564	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC564S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25℃			Ta=−40～+85℃		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

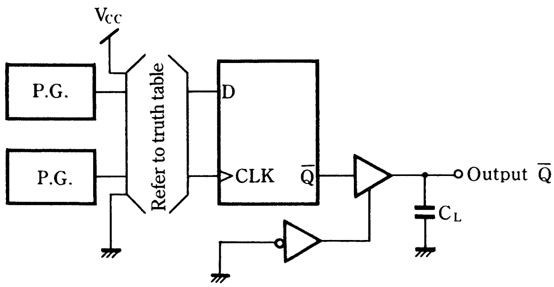
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	(V) Vcc	Test Conditions	Ta≒25℃ min.	Ta≒25℃ typ.	Ta≒25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time CLK→$\overline{Q}$ (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			16	25		31	
		6.0				21		26	
Propagation time CLK→$\overline{Q}$ (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			14	25		31	
		6.0				21		26	
3-state propagation time (H→Z)	t_{PHZ}	2.0				150		190	ns
		4.5	R_L = 1 kΩ		15	30		38	
		6.0				26		33	
3-state propagation time (L→Z)	t_{PLZ}	2.0				150		190	ns
		4.5	R_L = 1 kΩ		18	30		38	
		6.0				26		33	
3-state propagation time (Z→H)	t_{PZH}	2.0				125		155	ns
		4.5	R_L = 1 kΩ		13	25		31	
		6.0				21		26	
3-state propagation time (Z→L)	t_{PZL}	2.0				125		155	ns
		4.5	R_L = 1 kΩ		15	25		31	
		6.0				21		26	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			1	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30	42		24		
		6.0		35			28		

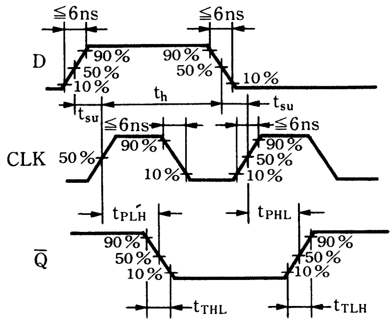
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}/t_{PHL}(CLK→$\overline{Q}$), t_{su}, t_h, f_{max}

1. Measuring Circuit (t_{PLH}, t_{PHL})

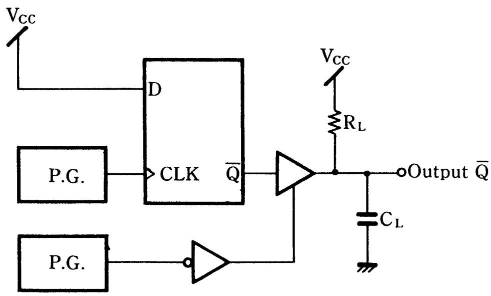


2. Waveforms

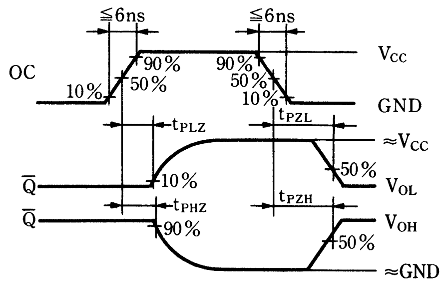


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit (t_{PLH}, t_{PHL})

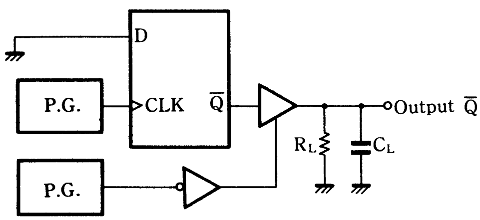


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms

See above [2] 2. for waveforms.

MN74HC573/MN74HC573S

Octal TRI-STATE D-Type Latches

■ Description

MN74HC537/MN74HC573S contain eight high-speed D-type latches with tri-state outputs. High output driving capability and tri-state outputs are suitable for the use of a common bus line in a bus utilized system.
When output disable input is LOW and latch enable input is HIGH, the output outputs the data input state.
When latch enable is LOW, the data input data is held in the output until when latch enable input becomes HIGH.
When output disable input is HIGH, all outputs become high impedance state regardless of the state of other inputs and data hold circuits.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS logic family.

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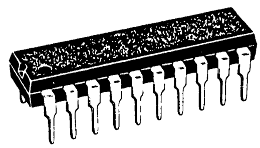
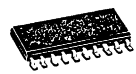


20-pin plastic DIL package

P-6



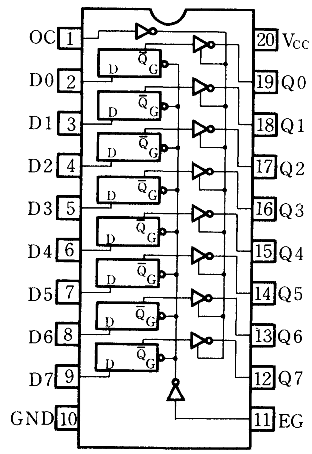
20-pin Panaflat package (SO-20D)

■ Truth Table

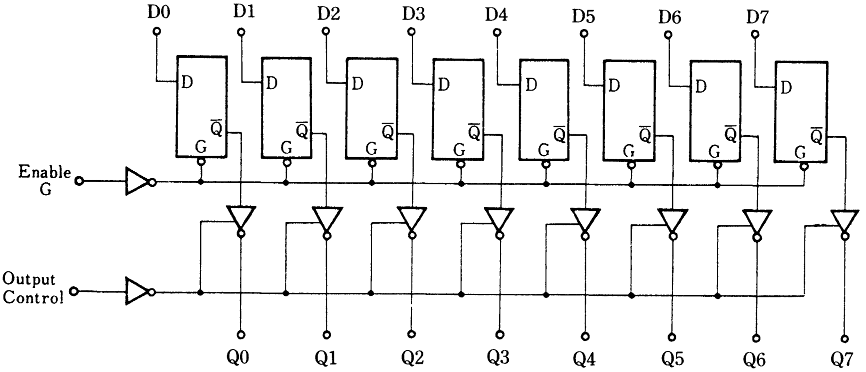
Input			Output
Output Control	G	D	Q
L	H	H	H
L	H	L	L
L	L	×	Qo
H	×	×	Hi-Z

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance
3. Q_O: Q level prior to determination of input condition shown in table

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC573	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC573S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I = V_{IH} or V_{IL}, V_O = V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

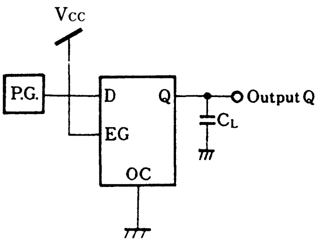
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time D→Q (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			11	20		25	
		6.0				17		21	
Propagation time D→Q (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			12	20		25	
		6.0				17		21	
Propagation time Enable G→Q (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
Propagation time Enable G→Q (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			16	30		38	
		6.0				26		33	
3-state propagation time (H→Z)	t_{PHZ}	2.0				125		155	ns
		4.5	R_L=1kΩ		10	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0				125		155	ns
		4.5	R_L=1kΩ		9	25		31	
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L=1kΩ		9	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	ns
		4.5	R_L=1kΩ		11	20		25	
		6.0				17		21	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			2	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	

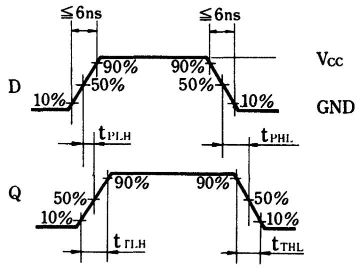
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}/t_{PHL} (D→Q) , t_{su} ,t_h

1. Measuring Circuit (t_{PLH},t_{PHL})

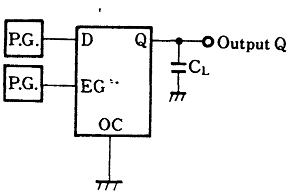


2. Waveforms

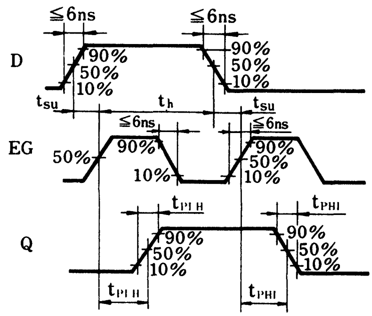


〔2〕 t_{PLH}/t_{PHL} (EG→Q)

1. Measuring Circuit (t_{PLH},t_{PHL})

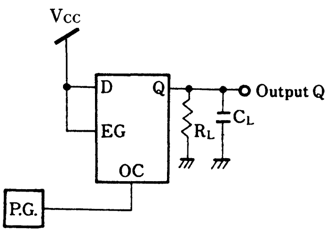


2. Waveforms

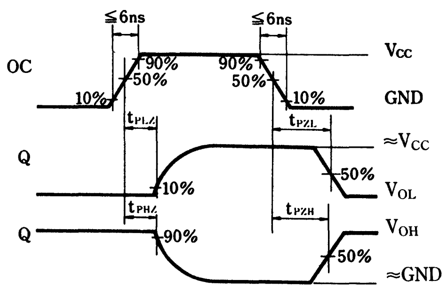


〔3〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit (t_{PLH},t_{PHL})

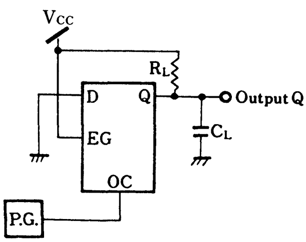


2. Waveforms



〔4〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit (t_{PLH},t_{PHL})



2. Waveforms

See above [3] 2. for waveforms.

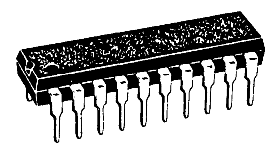
MN74HC574/MN74HC574S

Octal TRI-STATE D-Type Flip-Flops

■ Description

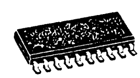
MN74HC574/MN74HC574S contain eight high-speed D-type flip-flops with trip-state outputs. High output driving capability and tri-state outputs are suitable for the use of a common bus line in a bus utilized system.
D input data satisfying set-up time is inverted and transferred to the output on the rising edge of clock input.
When output disable input is HIGH, all outputs become high impedance state regardless of the state of other inputs and data hold circuits.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly drive. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity.
Same pin configuration and function as standard 54LS/74LS logic family.

P-5



20-pin plastic DIL package

P-6



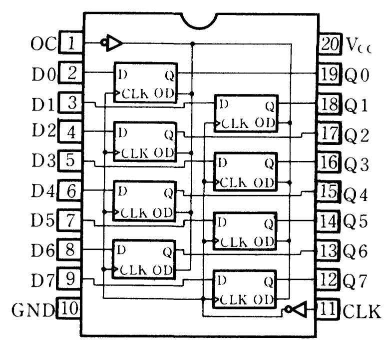
20-pin Panaflat package (SO-20D)

■ Truth Table

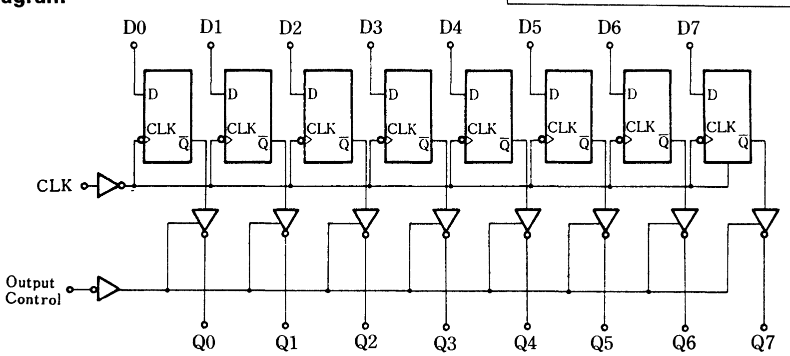
Input			Output
Output Control	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	×	Qo
H	×	×	Hi-Z

Note:
1. ↑: Data input is transferred to output on the negative-going edge from LOW to HIGH of the clock
2. ×: Either HIGH or LOW; it doesn't matter
3. Q_O: Q level prior to determination of input condition shown in table
4. Hi-Z: High impedance

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC574	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC574S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=−40～+85℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL} V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

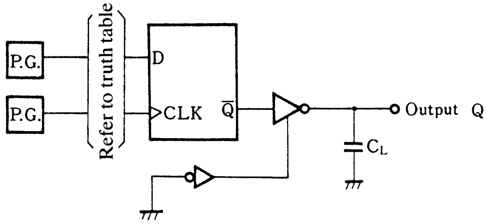
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40~+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time CLK→Q (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			14	30		38	
		6.0				26		33	
Propagation time CLK→Q (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			14	30		38	
		6.0				26		33	
3-state propagation time (H→Z)	t_{PHZ}	2.0				100		125	ns
		4.5	R_L=1 kΩ		11	20		25	
		6.0				17		21	
3-state propagation time (L→Z)	t_{PLZ}	2.0				125		155	ns
		4.5	R_L=1 kΩ		14	25		31	
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0				100		125	ns
		4.5	R_L=1 kΩ		9	20		25	
		6.0				17		21	
3-state propagation time (Z→L)	t_{PZL}	2.0				100		125	ns
		4.5	R_L=1 kΩ		11	20		25	
		6.0				17		21	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			2	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30	59		24		
		6.0		35			28		

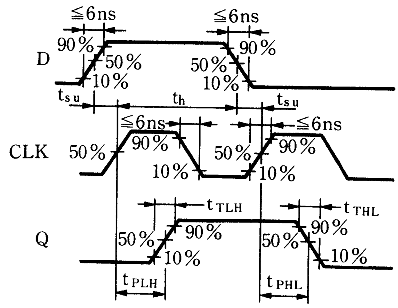
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH} / t_{PHL} (CLK→Q), t_{su}, f_{max}, t_h

1. Measuring Circuit (t_{PLH}, t_{PHL})

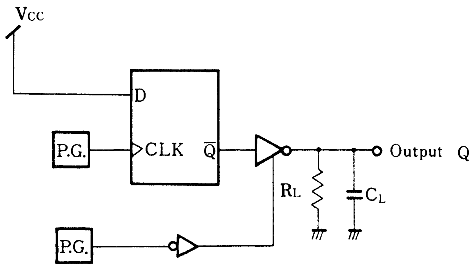


2. Waveforms

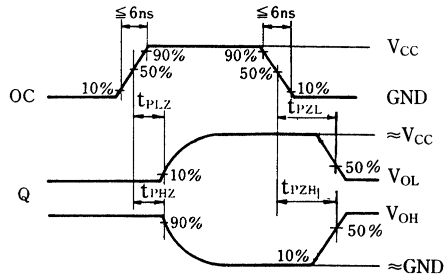


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit (t_{PLH}, t_{PHL})

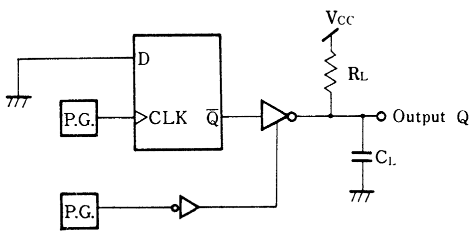


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms

See above [2] 2. for waveforms.

MN74HC640/MN74HC640S

Inverting Octal TRI-STATE Transceivers

■ Description

MN74HC640/MN74HC640S are high speed, inverting bidirectional buffers composed of eight 3-state outputs. Input is transferred bidirectionally, asynchronously through the data bus line. Large current output makes possible high-speed operation for driving a large capacity bus line. It has input G where output becomes enabled at LOW and directional control input DIR.
When DIR input is "H", data is transferred from input A to output B. When DIR input is "L", data is transferred from input B to output A. The transferred data is inverted.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 45LS/74LS logic family.

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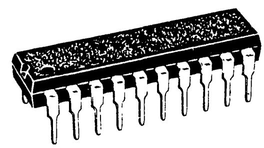
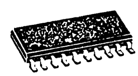


20-pin plastic DIL package

P-6



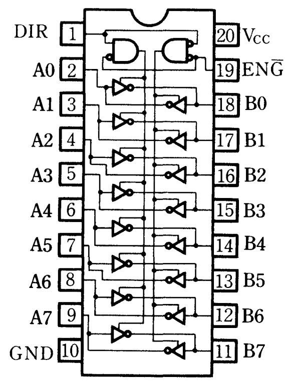
20-pin Panaflat package (SO-20D)

■ Truth Table

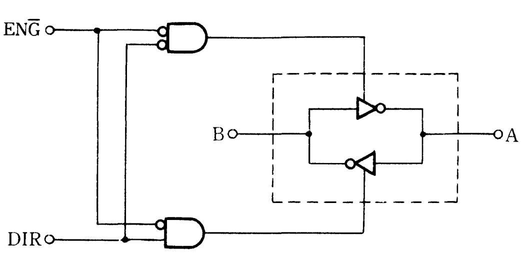
Enable $\overline{G}$	Direction Control DIR	Operation
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	×	Hi-Z

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Input/output voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC640	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC640S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=−40～+85℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

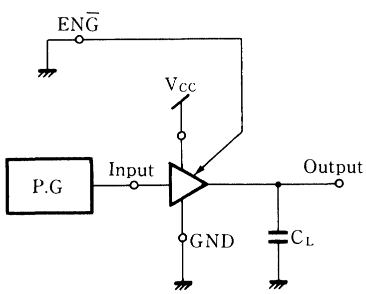
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40〜+85℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			10	20		25	
		6.0				17		21	
Propagation time (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			9	15		19	
		6.0				13		16	
3-state propagation time (H→Z)	t_{PHZ}	2.0				125		155	ns
		4.5	R_L=1kΩ		14	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0				150		190	ns
		4.5	R_L=1kΩ		18	30		38	
		6.0				26		33	
3-state propagation time (Z→H)	t_{PZH}	2.0				125		155	ns
		4.5	R_L=1kΩ		14	25		31	
		6.0				21		26	
3-state propagation time (Z→L)	t_{PZL}	2.0				125		155	ns
		4.5	R_L=1kΩ		15	25		31	
		6.0				21		26	

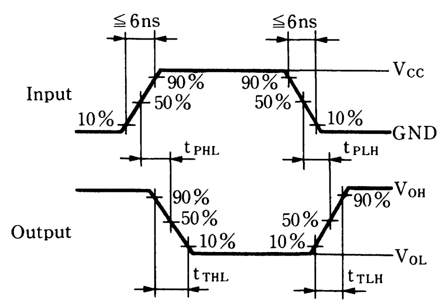
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit (t_{PLH}, t_{PHL})

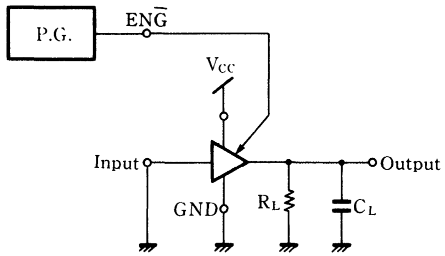


2. Waveforms

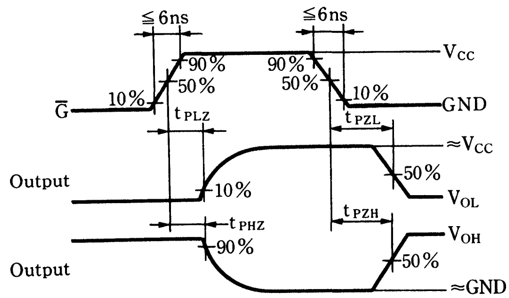


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit (t_{PLH}, t_{PHL})

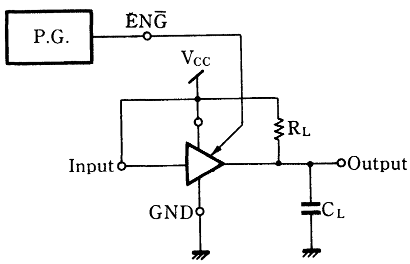


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

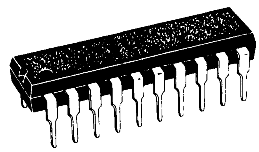
MN74HC643/MN74HC643S

True-Inverting Octal TRI-STATE Transceiver

■ Description

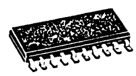
MN74HC643/MN74HC643S are high-speed, true-inverting bidirectional buffers composed of eight 3-state outputs. Input is transferred bidirectionally, asynchronously through the data bus line. Large current output makes possible high-speed operation for driving a large capacity bus line. It has input G where output becomes enabled at LOW and directional control input DIR. When DIR input is "H", data is inverted and transferred from input A to output B. When DIR input is "L", data is transferred from input B to output A.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-5



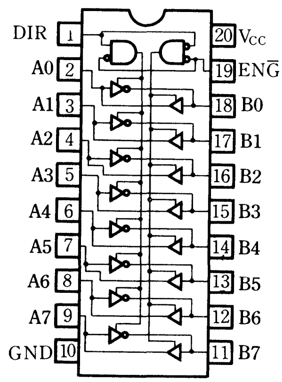
20-pin plastic DIL package

P-6



20-pin Panaflat package (SO-20D)

Pin configuration (top view)

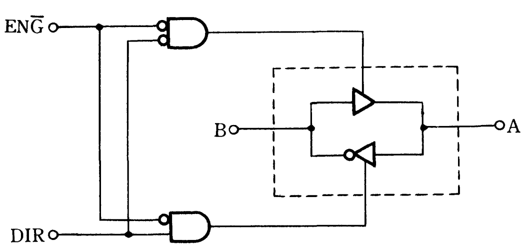


■ Truth Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	$\overline{A}$ data to B bus
H	×	Hi-Z

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance

■ Logic Diagram



Panasonic

■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC643	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC643S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=−40～+85℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−6.0	mA	3.86			3.76		
		6.0		−7.8	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		6.0	mA			0.32		0.37	
		6.0		7.8	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	6.0	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

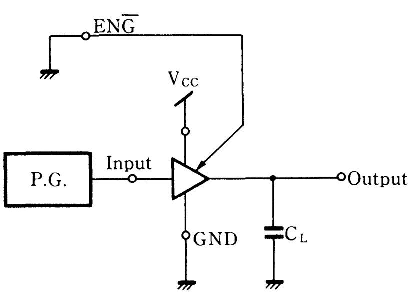
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40~+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time (L→H)	t_{PLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Propagation time (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
3-state propagation time (H→Z)	t_{PHZ}	2.0	R_L=1kΩ			125		155	ns
		4.5			14	25		31	
		6.0				21		26	
3-state propagation time (L→Z)	t_{PLZ}	2.0	R_L=1KΩ			125		155	ns
		4.5			13	25		31	
		6.0				21		26	
3-state propagation time (Z→H)	t_{PZH}	2.0	R_L=1kΩ			125		155	ns
		4.5			14	25		31	
		6.0				21		26	
3-state propagation time (Z→L)	t_{PZL}	2.0	R_L=1kΩ			100		125	ns
		4.5			10	20		25	
		6.0				17		21	

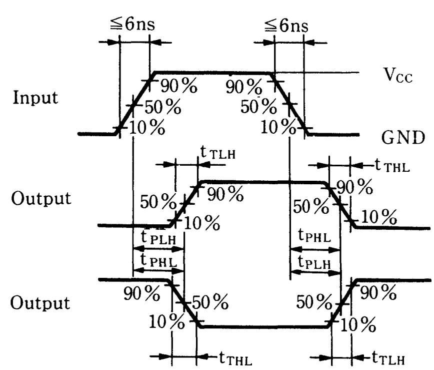
• Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

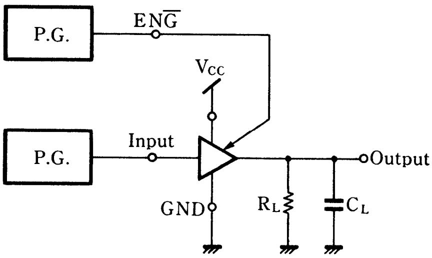


2. Waveforms

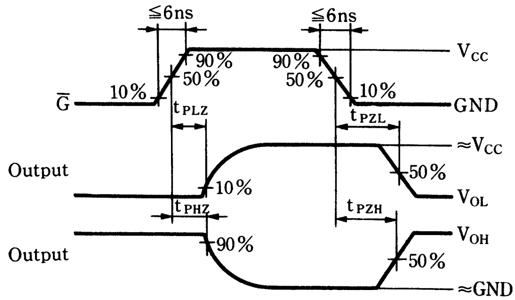


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

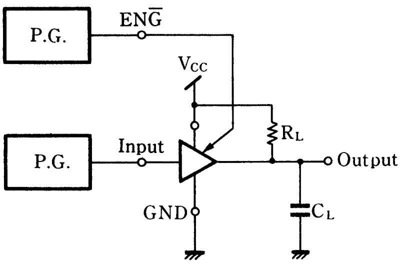


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

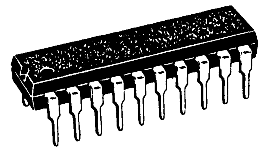
MN74HC688/MN74HC688S

8-Bit Magnitude Comparator (Equality Detector)

■ Description

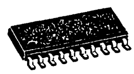
MN74HC688/MH74HC688S are high speed magnitude comparator which compare two eight-bit words and indicate equality, when $\overline{P=Q}$ output is "L", it indicates equality. A single input enabling output at Low level compares words greater than 8 bits, and can be used for easy dependent connection of multiple stages. This circuit can be used for decoding of memory blocks enable signal generated by computer address data.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-5



20-pin plastic DIL package

P-6

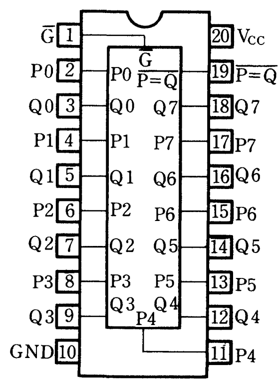


20-pin Panaflat package (SO-20D)

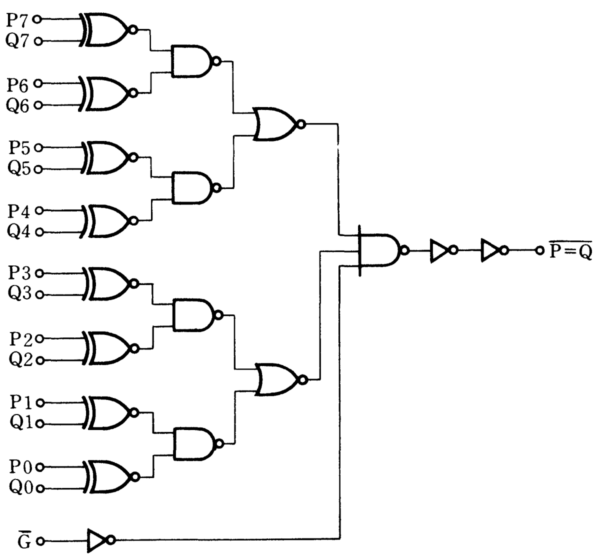
■ Truth Table

Input		Output
Data P, Q	Enable $\overline{G}$	$\overline{P=Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
×	H	H

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC688	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC688S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

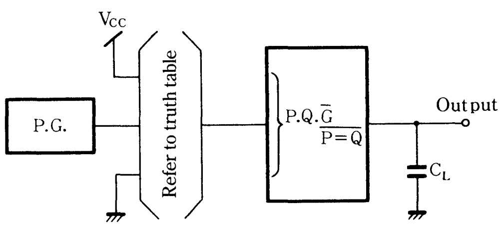
Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25℃			Ta=−40～+85℃		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

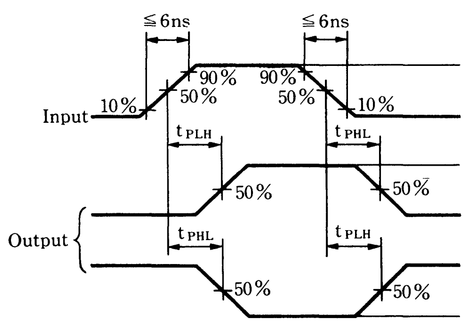
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time P, Q→P=Q (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
Propagation time P, Q→P=Q (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			14	30		38	
		6.0				26		33	
Propagation time G→P=Q (L→H)	t_{PLH}	2.0				100		125	ns
		4.5			11	20		25	
		6.0				17		21	
Propagation time G→P=Q (H→L)	t_{PHL}	2.0				100		125	ns
		4.5			9	20		25	
		6.0				17		21	

- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



2. Waveforms



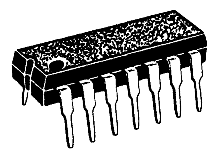
MN74HC4002/MN74HC4002S

Dual 4-Input NOR Gates

■ Description

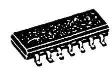
MN74HC4002/MN74HC4002S contain two 4-input positive isolation NOR gate circuits.
Adoption of a silicon gate CMOS process has made possible a low power dissipation, a high noise margin equivalent to a standard CMOS and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum.
LS TTL 10-inputs can be directly driven.
Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as standard CMOS logic 4000 family.

P-1



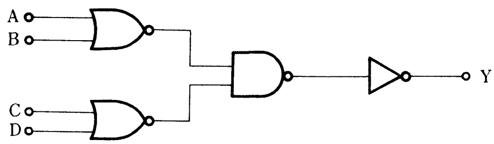
14-pin plastic DIL package

P-2

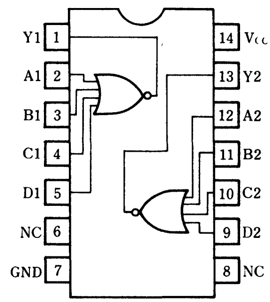


14-pin Panaflat package (SO-14D)

■ Logic Diagram



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC4002	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4002S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

MN74HC4015/MN74HC4015S

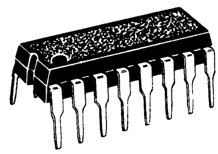
Dual 4-Stage Shift Registers with Serial-Input/Parallel-Output

■ Description

MN74HC4015/MH74HC4015S contain dual four-stage static shift registers in one chip. Flip-flop at each stage has common clear input, enabling asynchronous clearing with an external input at any time. Flip-flop at each stage is triggered by the rise of the clock pulse.

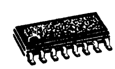
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 family.

P-3



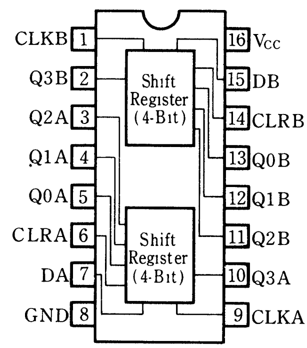
16-pin plastic DIL package

P-4



16-pin Panaflat package (SO-16D)

Pin Configuration (top view)

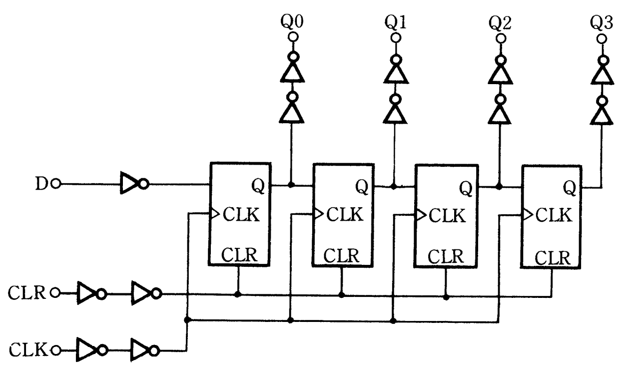


■ Truth Table

Input				Output			
n	CLK	D	CLR	Q_0	Q_1	Q_2	Q_3
1	↑	D1	L	D1	×	×	×
2	↑	D2	L	D2	D1	×	×
3	↑	D3	L	D3	D2	D1	×
4	↑	D4	L	D4	D3	D2	D1
	↓	×	L	no change			
	×	×	H	L	L	L	L

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. D_n: "H" or "L"
3. n: Number of clock pulse
4. ↑: The rise of clock from "L" to "H"
5. ↓: The fall of clock from "H" to "L"

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Input/output voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65 \sim +150$	℃
Power dissipation	MN74HC4015	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4015S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0.	V
Input/output voltage	V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

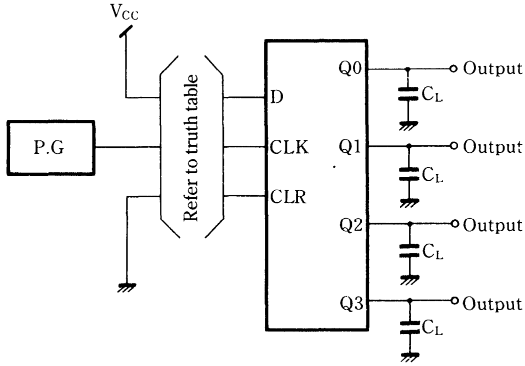
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OI}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

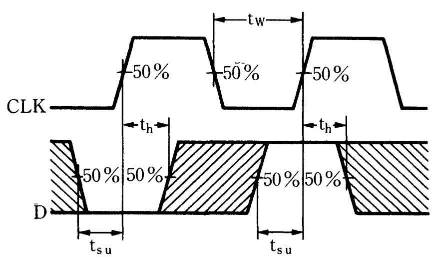
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			10	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Propagation time CLK→Qn (L→H)	t_{PLH}	2.0				175		220	ns
		4.5			20	35		44	
		6.0				30		37	
Propagation time CLK→Qn (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			19	35		44	
		6.0				30		37	
Propagation time CLR→Qn (H→L)	t_{PHL}	2.0				175		220	ns
		4.5			19	35		44	
		6.0				30		37	
Minimum pulse width CLR, CLK	t_W	2.0				125		155	ns
		4.5			10	25		31	
		6.0				21		26	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5			2	20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30	71		24		
		6.0		35			28		

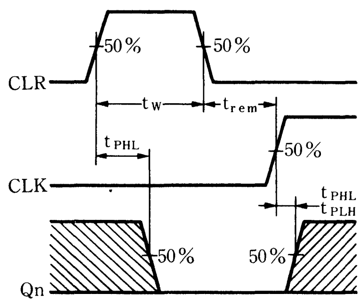
● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



2. Waveforms





MN74HC4020/MN74HC4020S

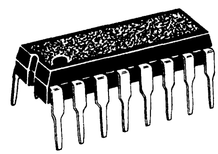
14-Stage Binary Counter

■ Description

MN74HC4020/4020S high-speed 14-Stage binary counter. This counter provides increments on the falling edge of clock input. The clear input operates in the counter, and all outputs (Q1~Q14) become "L" regardless of the clock input, when the clear input is "H".

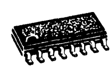
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 family.

P-3



16-pin plastic DIL package

P-4



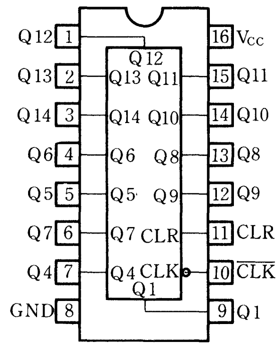
16-pin Panaflat package (SO-16D)

■ Truth Table

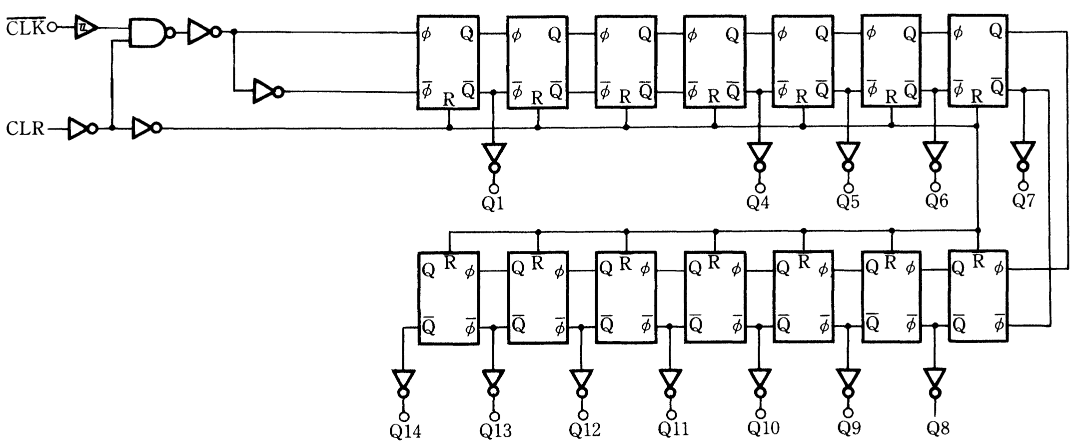
$\overline{CLK}$	CLR	Mode
×	H	All Outputs are low
↑	L	No Change
↓	L	Counter Advances

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ↓: The fall of clock from "H" to "L"
3. ↑: The rise of clock from "L" to "H"

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC4020	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4020S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

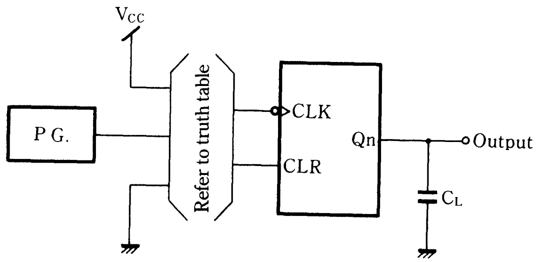
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

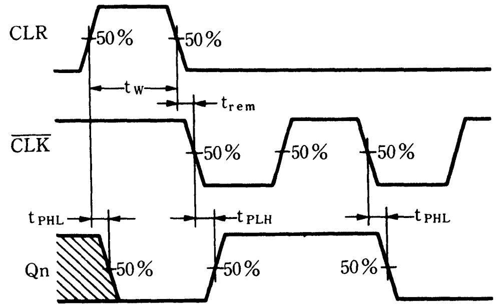
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time $\overline{CLK}$→Q1 (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			16	30		38	
		6.0				26		33	
Propagation time $\overline{CLK}$→Q1 (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			16	30		38	
		6.0				26		33	
Propagation time Qn→Qn+1 (L→H)	t_{PLH}	2.0				75		95	ns
		4.5			5	15		19	
		6.0				13		16	
Propagation time Qn→Qn+1 (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			5	15		19	
		6.0				13		16	
Propagation time CLR→Qn (H→L)	t_{PLH}	2.0				150		190	ns
		4.5			16	30		38	
		6.0				26		33	
Minimum pulse width CLR	t_W	2.0				125		155	ns
		4.5			12	25		31	
		6.0				21		26	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5			2	15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30	75		24		
		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms

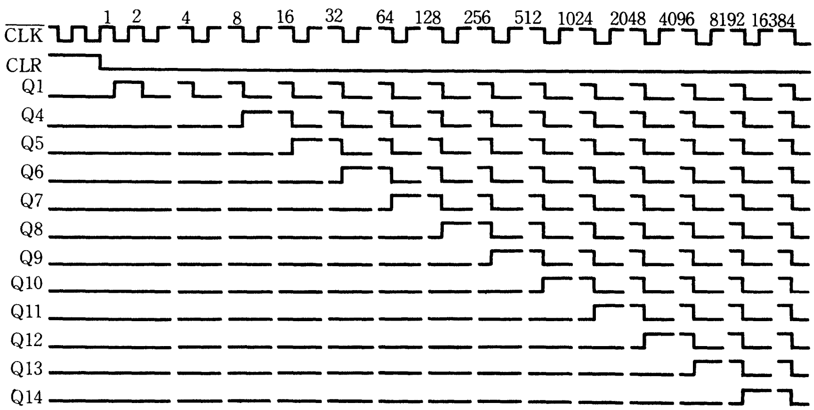
1. Measuring Circuit



2. Waveforms



■ Typical Operating Conditions



MN74HC4024/MN74HC4024S

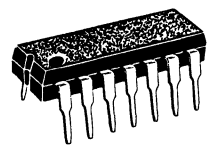
7-Stage Binary Counter

■ Description

MN74HC4024/4024S high speed 7-stage ripple-carry counter. This counter provides increments on the falling edge of clock input. The clear input operates in the counter, and all outputs (Q1~Q7) become "L" regardless of the clock, when the clear input is "H".

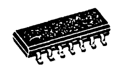
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 family.

P-1



14-pin plastic DIL package

P-2



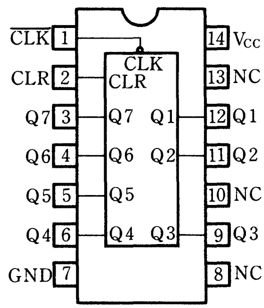
14-pin Panaflat package (SO-14D)

■ Truth Table

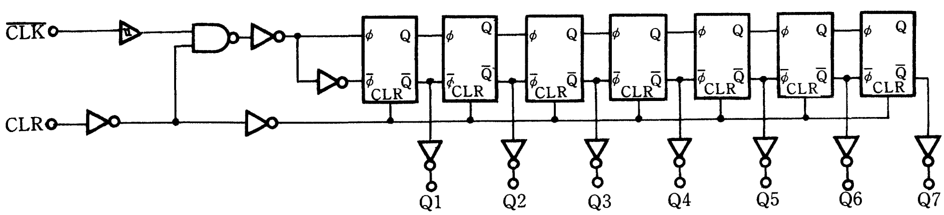
$\overline{CLK}$	CLR	Mode
×	H	All Outputs are low
↑	L	No Change
↓	L	Counter Advances

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ↓: The fall of clock from "H" to "L"
3. ↑: The rise of clock from "L" to "H"

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC4024	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4024S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

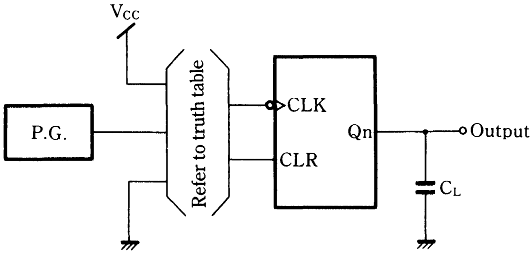
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=$-40\sim+85$℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
		6.0	or	-20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	-4.0	mA	3.86			3.76		
		6.0		-5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ **AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)**

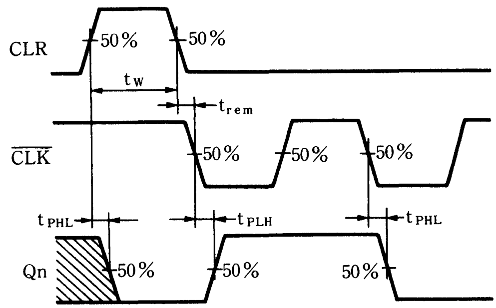
Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time $\overline{CLK}$→Q1 (L→H)	t_{PLH}	2.0				150		190	ns
		4.5			16	30		38	
		6.0				26		33	
Propagation time $\overline{CLK}$→Q1 (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			15	30		38	
		6.0				26		33	
Propagation time Qn→Qn+1 (L→H)	t_{PLH}	2.0				75		95	ns
		4.5			5	15		19	
		6.0				13		16	
Propagation time Qn→Qn+1 (H→L)	t_{PHL}	2.0				75		95	ns
		4.5			7	15		19	
		6.0				13		16	
Propagation time CLR→Qn (H→L)	t_{PHL}	2.0				150		190	ns
		4.5			17	30		38	
		6.0				26		33	
Minimum CLR pulse width	t_w	2.0				125		155	ns
		4.5			7	25		31	
		6.0				21		26	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5			4	15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30	98		24		
		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms

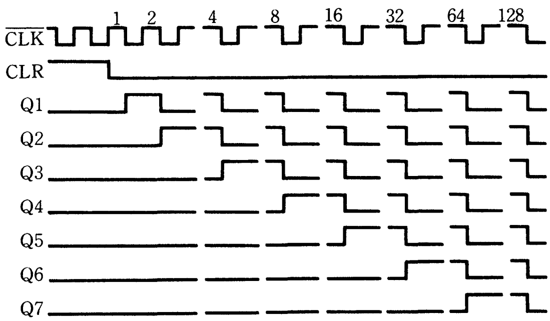
1. Measuring Circuit



2. Waveforms



■ Typical Operating Conditions



MN74HC4040/MN74HC4040S

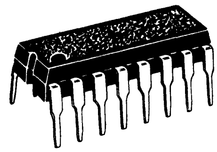
14-Stage Binary Counter

■ Description

MN74HC4040/4040S high speed12-stage ripple-carry counter. This counter provides increments on the falling edge of clock input. The clear input operates in the counter, and all outputs (Q1~Q12) become "L" regardless of the clock, when the clear input is "H".

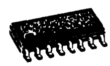
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 family.

P-3



16-pin plastic DIL package

P-4



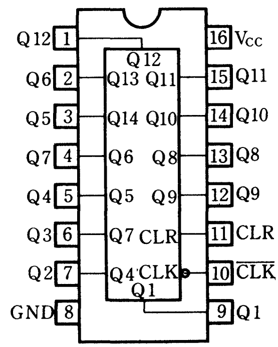
16-pin Panaflat package (SO-16D)

■ Truth Table

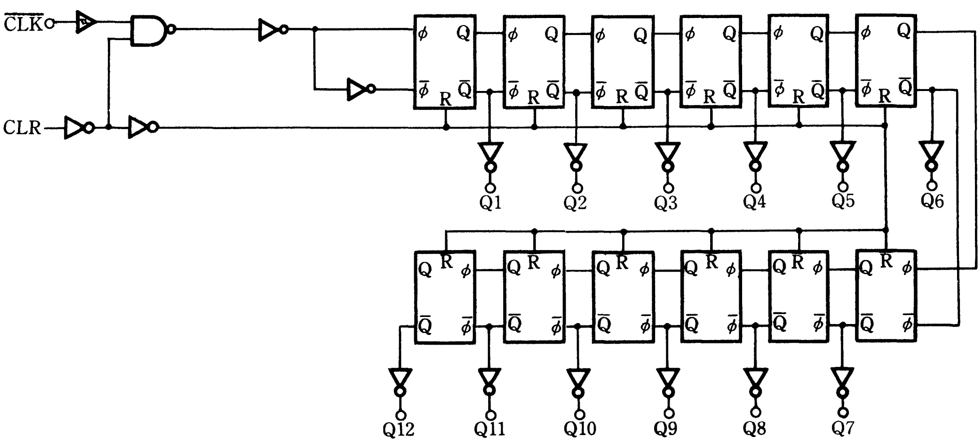
$\overline{CLK}$	CLR	Mode
×	H	All Outputs are low
↑	L	No Change
↓	L	Counter Advances

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ↓: The fall of clock from "H" to "L"
3. ↑: The rise of clock from "L" to "H"

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	± 20	mA
Output parasitic diode current			I_{OK}	± 20	mA
Output current			I_O	± 25	mA
Supply current			I_{CC}, I_{GND}	± 50	mA
Storage temperature range			Tstg	$-65 \sim +150$	℃
Power dissipation	MN74HC4040	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4040S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4 \sim 6.0$	V
Input/output voltage	V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature range	T_A		$-40 \sim +85$	℃
Input rise and fall time	t_r, t_f	2.0	$0 \sim 1000$	ns
		4.5	$0 \sim 500$	ns
		6.0	$0 \sim 400$	ns

■ DC Characteristics (GND=0V)

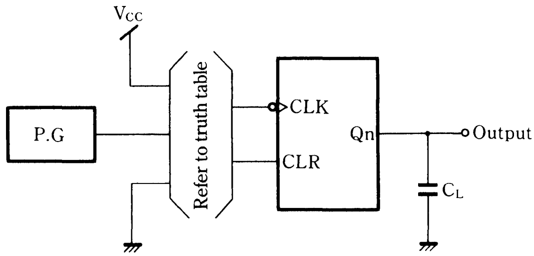
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=−40～+85℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

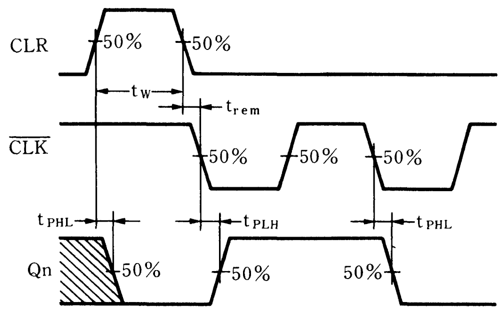
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40∼+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			12	15		19	
		6.0			10	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			9	15		19	
		6.0			8	13		16	
Propagation time $\overline{CLK}$→Q1 (L→H)	t_{PLH}	2.0			55	200		250	ns
		4.5			20	40		50	
		6.0			15	34		43	
Propagation time $\overline{CLK}$→Q1 (H→L)	t_{PHL}	2.0			50	175		220	ns
		4.5			18	35		44	
		6.0			15	30		37	
Propagation time Qn→Qn+1 (L→H)	t_{PLH}	2.0			18	75		95	ns
		4.5			7	15		19	
		6.0			5	13		16	
Propagation time Qn→Qn+1 (H→L)	t_{PHL}	2.0			17	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
Propagation time CLR→Qn (H→L)	t_{PHL}	2.0			55	150		190	ns
		4.5			17	30		38	
		6.0			14	26		33	
Minimum CLR pulse width	t_w	2.0			20	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
Minimum recovery time	t_{rem}	2.0			5	75		95	ns
		4.5			3	15		19	
		6.0			2	13		16	
Maximum clock frequency	f_{max}	2.0		6	25		4		MHz
		4.5		30	70		24		
		6.0		35	80		28		

• Switching Time Measuring Circuit and Waveforms

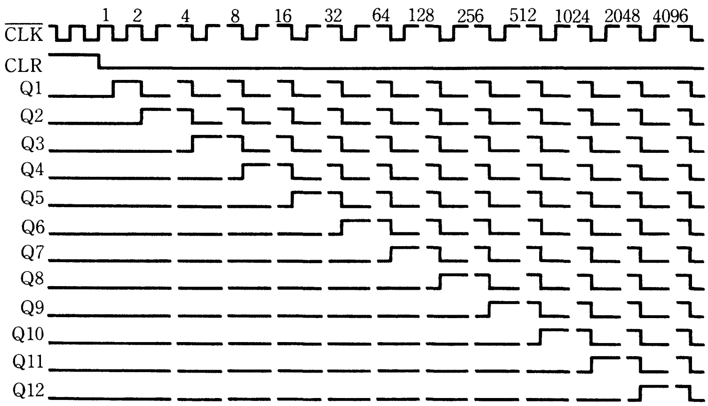
1. Measuring Circuit (t_{PLH}, t_{PHL})



2 . Switching Waveforms



■ Typical Operating Condition



MN74HC4049/MN74HC4049S

Hex Inverting Logic Level Down Converters

■ Description

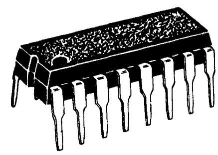
MN74HC4049/MN74HC4049S are inverting logic level down converters which function to correct input protection construction. This construction is used for the logic level converter, changing HIGH to LOW logic while it is not operated by LOW logic voltage.

For example, 0-15V CMOS logic can be converted to 0-5V logic when a 5V power supply voltage is used.

As for corrected input protection, input voltage can exceed the power supply voltage because the diode is not connected to V_{CC}. The zener diode connected to GND protects the input against plus-minus quiescent voltage, and can be used as a inverter without level conversion.

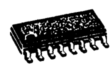
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Same pin configuration and function as the standard CMOS logic 4000 family.

P-3



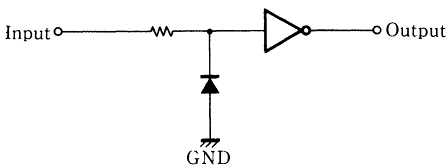
16-pin plastic DIL package

P-4

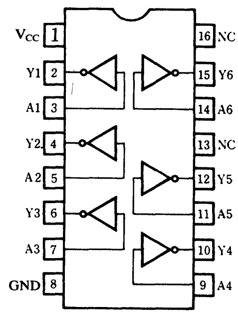


16-pin Panaflat package (SO-16D)

■ Sckematic Diagram



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Output voltage			V_O	$-0.5\sim V_{CC}+0.5$	V
Input voltage			V_I	−0.5~16	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65~+150	°C
Power dissipation	MN74HC4049	Ta=−40~+60°C	PD	400	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4049S	Ta=−40~+60°C	PD	275	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Output voltage	V_O		0~V_{CC}	V
Input voltage	V_I		0~15	V
Operating temperature range	T_A		−40~+85	°C
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.76			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					4.0		40.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0			19	75		95	ns
		4.5			10	15		19	
		6.0			9	13		16	
Output fall time	t_{THL}	2.0			18	75		95	ns
		4.5			10	15		19	
		6.0			8	13		16	
Propagation time (L→H)	t_{PLH}	2.0			15	100		125	ns
		4.5			11	20		25	
		6.0			10	17		21	
Propagation time (H→L)	t_{PHL}	2.0			18	100		125	ns
		4.5			11	20		25	
		6.0			9	17		21	

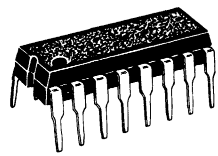
MN74HC4050/MN74HC4050S

Hex Logic Level Down Converter

■ Description

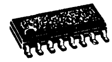
MN74HC4050/MN74HC4050S are non-inverted logic level down converts which function to correct input protection construction. This construction is used for the logic level converter, changing HIGH to LOW logic while it is not operated by LOW logic voltage.
For example, 0–15V CMOS logic can be converted to 0–5V logic when a 5V power supply voltage is used.
As for corrected input protection, input voltage can exceed the power supply voltage because the diode is not connected to V_{CC}.
The zener diode connected to GND protects the input against plus-minus quiescent voltage, and can be used as a buffer without level conversion.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Same pin configuration and function as the standard CMOS logic 4000 family.

P-3



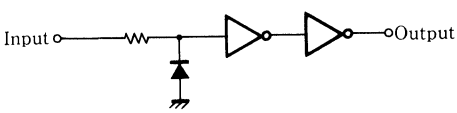
16-pin plastic DIL package

P-4

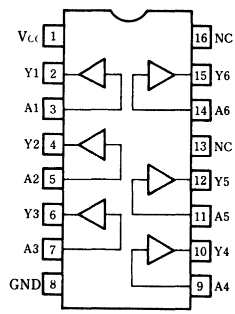


16-pin Panaflat package (SO-16D)

■ Sckematic Diagram



Pin configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~−7.0	V
Output voltage			V_O	−0.5~V_{CC}+0.5	V
Input voltage			V_I	−0.5~16	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65~+150	°C
Power dissipation	MN74HC4050	Ta=−40~+60°C	PD	400	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4050S	Ta=−40~+60°C	PD	275	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Output voltage	V_O		0~V_{CC}	V
Input voltage	V_I		0~15	V
Operating temperature range	T_A		−40~+85	°C
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	I_O Unit	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					4.0		40.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Output rise time	t_{TLH}	2.0			21	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			13	75		95	ns
		4.5			7	15		19	
		6.0			5	13		16	
Propagation time (L→H)	t_{PLH}	2.0			39	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			10	75		95	ns
		4.5			8	15		19	
		6.0			6	13		16	

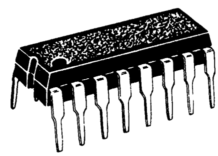
MN74HC4051/MN74HC4051S

Single 8-Channel Multiplexer/Demultiplexer

■ Description

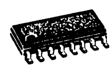
MN74HC4051/MN74HC4051S are an analog multiplexer which controls 8-channel analog switch with three input digital signal. Since each switch ON resitance is low, this chip can be connected to low impedance circuits. Pin configuration is same as the standard CMOS logic 4000 family.

P-3



16-pin plastic DIL package

P-4



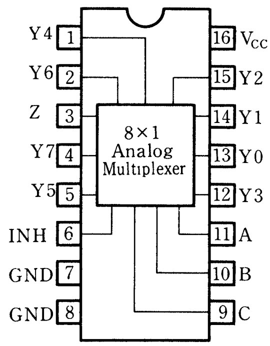
16-pin Panaflat package (SO-16D)

■ Truth Table

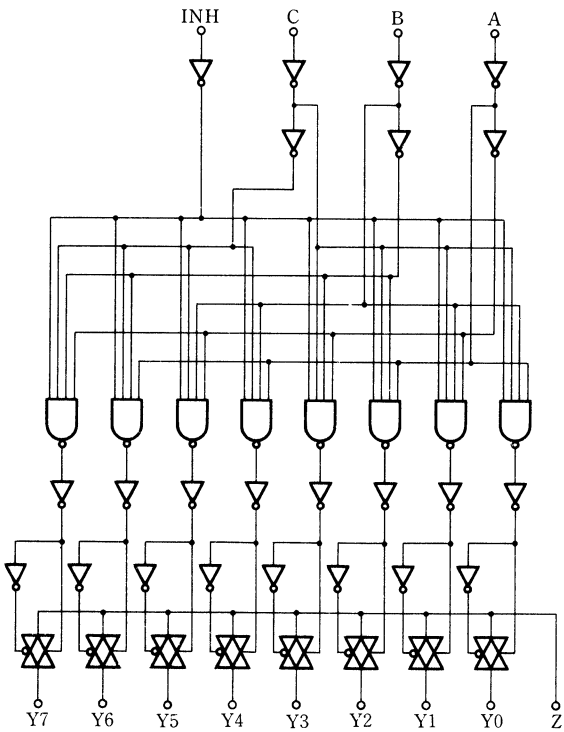
Input				Channel ON
INH	C	B	A	
L	L	L	L	Y0 − Z
L	L	L	H	Y1 − Z
L	L	H	L	Y2 − Z
L	L	H	H	Y3 − Z
L	H	L	L	Y4 − Z
L	H	L	H	Y5 − Z
L	H	H	L	Y6 − Z
L	H	H	H	Y7 − Z
H	×	×	×	All OFF

Note: ×: don't care

Pin configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC4051	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4051S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		$2.0\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=$-40\sim+85$℃ min.	Ta=$-40\sim+85$℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0		1.5			1.5		V
		4.5		3.15			3.15		V
		6.0		4.2			4.2		V
Input LOW voltage	V_{IL}	2.0				0.3		0.3	V
		4.5				0.9		0.9	V
		6.0				1.2		1.2	V
Input current	I_I	6.0	$V_I=V_{CC}$ or GND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND $I_O=0$			8.0		80.0	μA
Input/output off reak current	$I_{S(off)}$	6.0	$V_I=V_{IH}$ or V_{IL} $\|V_S\|=V_{CC}$ or GND			±0.1		±1.0	μA
On resistance	R_{ON}	2.0	$V_{is}=V_{CC}\sim GND$		1000	2000		3000	Ω
		3.0			200	400		600	Ω
		4.5			80	160		240	Ω
		6.0			60	120		130	Ω
Variation of On resistance	ΔR_{ON}	2.0			150				Ω
		3.0			25				Ω
		4.5			10				Ω
		6.0			7				Ω

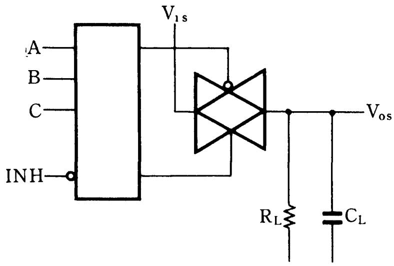
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Propagation time Vis→Vos (H→L)	t_{PHL}	2.0	R_L=1kΩ, C_L=50pF, INH=GND, Input transition time =15ns			50		65	ns
		4.5				10		13	
		6.0				9		11	
Propagation time Vis→Vos (L→H)	t_{PLH}	2.0				50		65	ns
		4.5				10		13	
		6.0				9		11	
Propagation time A, B, C→Vos (H→L)	t_{PHL}	2.0	R_L=1kΩ, C_L=50pF, INH=GND			150		190	ns
		4.5				30		38	
		6.0				26		33	
Propagation time A, B, C→Vos (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Output Disable Time INH→V_{OS} (H)	t_{PHZ}	2.0	R_L=1kΩ, C_L=50pF, INH=Vcc			150		190	ns
		4.5				330		38	
		6.0				26		33	
Output Disable Time INH→V_{OS} (L)	t_{PLZ}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Output Enable Time INH→V_{OS} (H)	t_{PZH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Output Enable Time INH→V_{OS} (L)	t_{PZL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Sine Wave Distortion		2.0	R_L=10kΩ, C_L=50pF, fi =1kHz, Y = $\frac{1}{2}$Vcc(P−P)		0.1				%
		4.5							
		6.0							
Crosstalk 2 channel		2.0	R_L=1kΩ, Y=$\frac{1}{2}$Vcc(P−P)		t.b.f				MHz
		4.5							
		6.0							
Crosstalk (Address Input→Output)		2.0	R_L=10kΩ, C_L=50pF, INH or A, B, C=Vcc		t.b.f				mV
		4.5							
		6.0							
Feedthrough (OFF)		2.0	R_L=10kΩ, Y=$\frac{1}{2}$Vcc (P-P), C_L=50pF, INH=GND		t.b.f				MHz
		4.5							
		6.0							
Frequency Response		2.0	R_L=1kΩ, INH=$\frac{1}{2}$Vcc (P-P)		t.b.f				MHz
		4.5							
		6.0							

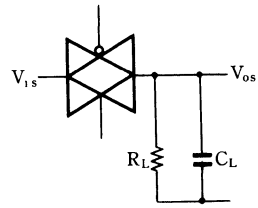
- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit

(Fig. 1) Progation Delay Time, Output Disable/ Enable Time, Crosstalk Measuring Circuit



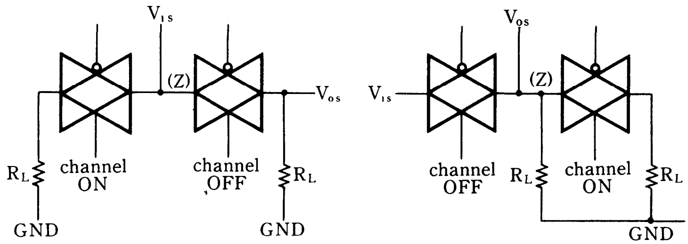
(Fig. 2) Sine Wave Distortion, Feedthrough, Frequency Response Measuring Circuit



$$20 \log \frac{V_{OS}}{V_{IS}} = -50\text{dB}$$

$$20 \log \frac{V_{OS}}{V_{IS}} = -3\text{dB}$$

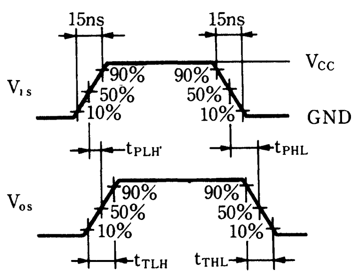
(Fig. 3) Crosstalk Measurnng Cirucit

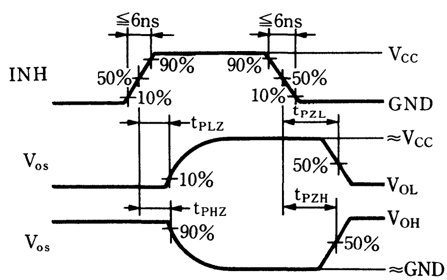


(a) (b)

$$20 \log \frac{V_{OS}}{V_{IS}} = -50\text{dB}$$

2. Waveforms





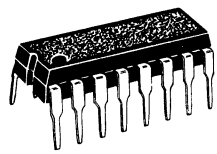
MN74HC4052/MN74HC4052S

Dual 4-Channel Analog Multiplexer/Demultiplexer

■ Description

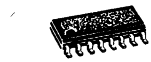
MN74HC4052/MN74HC4052S are dual 4-channel multiplexer/demultiplexer for analog or digital signals. The switch to each channel become ON with the control signal. Since each switch ON resitance is low, it can be connected to low impedance circuits. Pin configuration is same as standard CMOS logic 4000 family.

P-3



16-pin plastic DIL package

P-4



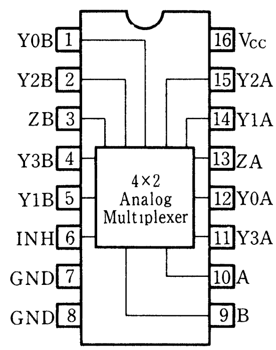
16-pin Panaflat package (SO-16D)

■ Truth Table

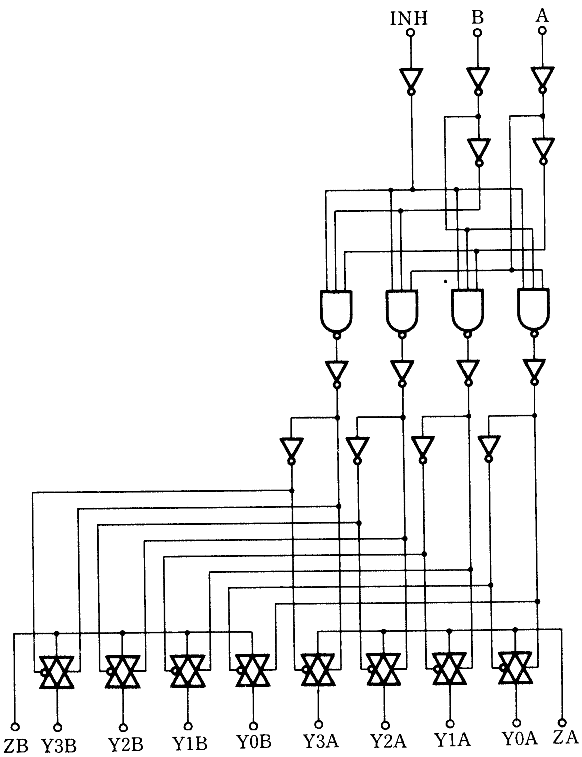
Input			Channel ON
INH	B	A	
L	L	L	Y0A–ZA; Y0B–ZB
L	L	H	Y1A–ZA; Y1B–ZB
L	H	L	Y2A–ZA; Y2B–ZB
L	H	H	Y3A–ZA; Y3B–ZB
H	×	×	All OFF

Note:
1. ×: don't care

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65~+150	℃
Power dissipation	MN74HC4052	Ta=−40~+60℃	P_D	400	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4052S	Ta=−40~+60℃	P_D	275	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		2.0~6.0	V
Input/output voltage	V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0		1.5			1.5		V
		4.5		3.15			3.15		V
		6.0		4.2			4.2		V
Input LOW voltage	V_{IL}	2.0				0.3		0.3	V
		4.5				0.9		0.9	V
		6.0				1.2		1.2	V
Input current	I_I	6.0	$V_I = V_{CC}$ or GND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I = V_{CC}$ or GND, $I_O=0$			8.0		80.0	μA
Input/output off reak current	t_{THL}	6.0	$V_I = V_{IH}$ or V_{IL}, $\|V_S\| = V_{CC}$ or GND			±0.1		±1.0	μA
On resistance	R_{ON}	2.0	V_{IS}: V_{CC}~GND		1000	2000		3000	Ω
		3.0			200	400		600	Ω
		4.5			80	160		240	Ω
		6.0			60	120		180	Ω
Variation of On resistance	ΔR_{ON}	2.0			150				Ω
		3.0			25				Ω
		4.5			10				Ω
		6.0			7				Ω

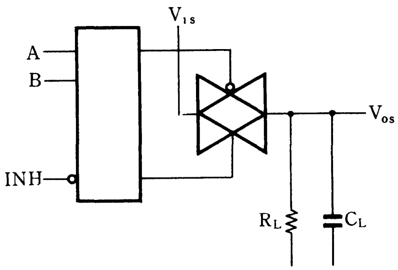
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Propagation time $V_{is} \rightarrow V_{os}$ (H→L)	t_{PHL}	2.0	R_L=1kΩ			50		65	ns
		4.5	C_L=50pF			10		13	
		6.0	INH=GND			9		11	
Propagation time $V_{is} \rightarrow V_{os}$ (L→H)	t_{PLH}	2.0	Input transition			50		65	ns
		4.5	time=15ns			10		13	
		6.0				9		11	
Propagation time A, B, →V_{os} (H→L)	t_{PHL}	2.0	R_L=1kΩ			150		190	ns
		4.5	C_L=50pF			30		38	
		6.0	INH=GND			26		33	
Propagation time A, B, →V_{os} (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Output Disable Time INH→V_{OS} (H)	t_{PHZ}	2.0	R_L=1kΩ			150		190	ns
		4.5	C_L=50pF			30		38	
		6.0	INH=Vcc			26		33	
Output Disable Time INH→V_{OS} (L)	t_{PLZ}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Output Enable Time INH→V_{OS} (H)	t_{PZH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Output Enable Time INH→V_{OS} (L)	t_{PZL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Sine Wave Distortion		2.0	R_L=10kΩ		0.1				ns
		4.5	C_L=50pF						
		6.0	f_i=1 H, Y=½Vcc(P-P)						
Crosstalk 2 channel		2.0	R_L=1kΩ		t.b.f				%
		4.5	Y=½Vcc (P-P)						
		6.0							
Crosstalk (Address Input→Output)		2.0	R_L=10kΩ		t.b.f				mV
		4.5	C_L=50pF						
		6.0	INH or A, B, C=Vcc						
Feedthough (OFF)		2.0	R_L=10kΩ		t.b.f				MHz
		4.5	C_L=50pF						
		6.0	INH=GND, Y=½Vcc(P-P)						
Frequency Response		2.0	R_L=1kΩ		t.b.f				MHz
		4.5	INH=½Vcc (P-P)						
		6.0							

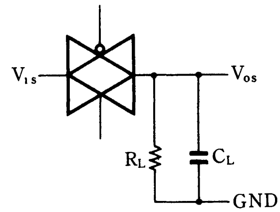
- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit

(Fig. 1) Propagation Delay Time, Output Disable/ Enable Time, Crosstalk Measuring Circuit



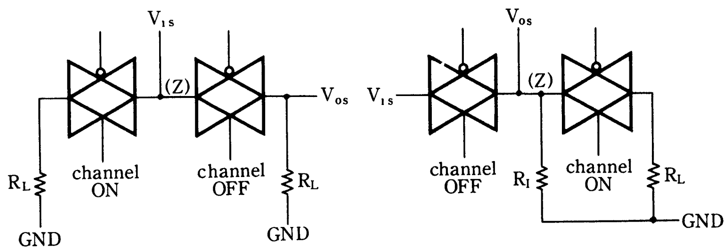
(Fig. 2) Sine Wave Distortion, Feedthrough, Frequency Response Measuring Circuit



$$20\log\frac{V_{OS}}{V_{IS}} = -50\text{dB}$$

$$20\log\frac{V_{OS}}{V_{IS}} = -3\text{dB}$$

(Fig. 3) Crosstalk Measuring Cirucit

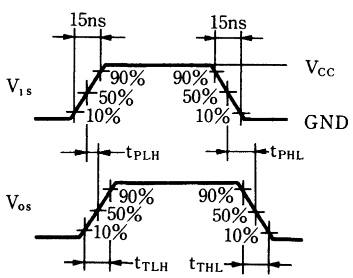


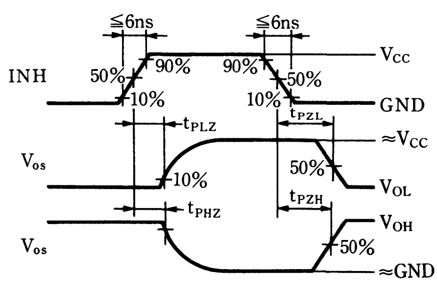
(a)

(b)

$$20\log\frac{V_{OS}}{V_{IS}} = -50\text{dB}$$

2. Waveforms





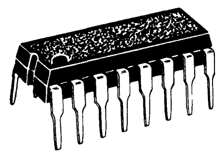
MN74HC4053/MN74HC4053S

Triple 2-Channel Analog Multiplexer/Demultiplexer

■ Description

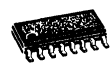
MN74HC4053/MN74HC4053S are triple 2-channel multiplexers/demultiplexers for analog or digital signals. The switch to each channel becomes ON with the control signal. Since each switch ON resitance is low, it can be connected to low impedance circuits. Pin configuration is same as standard CMOS logic 4000 family.

P-3



16-pin plastic DIL package

P-4



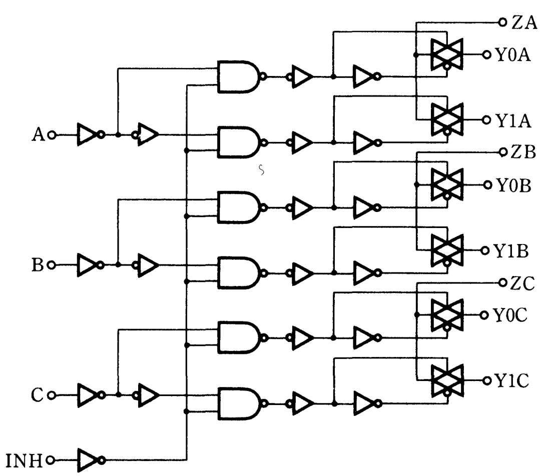
16-pin Panaflat package (SO-16D)

■ Truth Table

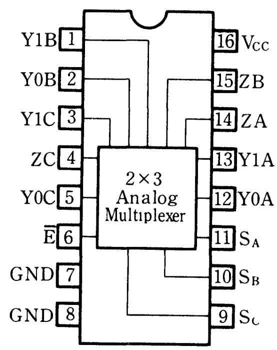
Input		Channel ON
INH	S_A	
L	L	Y0A–ZA
L	H	Y1A–ZA
H	×	All OFF

Note:
1. ×: don't care

■ Logic Diagram



Pin Configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC4053	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4053S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC} (V)	Rating	Unit
Operating supply voltage	V_{CC}		2.0～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0		1.5			1.5		V
		4.5		3.15			3.15		V
		6.0		4.2			4.2		V
Input LOW voltage	V_{IL}	2.0				0.3		0.3	V
		4.5				0.9		0.9	V
		6.0				1.2		1.2	V
Input current	I_I	6.0	V_I=V_{CC} or GND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0			8.0		80.0	μA
Input/output off reak current	$I_{S(off)}$	6.0	V_I=V_{IH} or V_{IL}, $\|V_S\|$=V_{CC} or GND			±0.1		±1.0	μA
On resistance	R_{ON}	2.0	V_{IS}: V_{CC}～GND		1000	2000		3000	Ω
		3.0			200	400		600	Ω
		4.5			80	160		240	Ω
		6.0			60	120		180	Ω
Variation of On resistance	ΔR_{ON}	2.0			150				Ω
		3.0			25				Ω
		4.5			10				Ω
		6.0			7				Ω

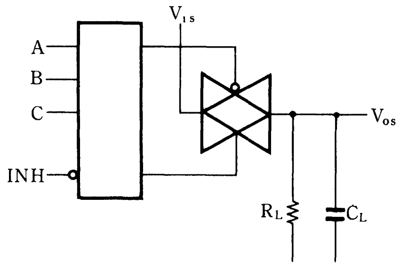
■ **AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)**

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Propagation time $V_{is} \to V_{OS}$ (H→L)	t_{PHL}	2.0 4.5 6.0	R_L=1kΩ C_L=50pF INH=GND Input transition time=15ns		5	50 10 9		65 13 11	ns
Propagation time $V_{is} \to V_{OS}$ (L→H)	t_{PLH}	2.0 4.5 6.0			4	50 10 9		65 13 11	ns
Propagation time A, B, →V_{OS} (H→L)	t_{PHL}	2.0 4.5 6.0	R_L=1kΩ C_L=50pF INH=GND		17	150 30 26		190 38 33	ns
Propagation time A, B, →V_{OS} (L→H)	t_{PLH}	2.0 4.5 6.0			14	150 30 26		190 38 33	ns
Output Disable Time INH→V_{OS} (H)	t_{PHZ}	2.0 4.5 6.0	R_L=1kΩ C_L=50pF INH=Vcc		18	150 30 26		190 38 33	ns
Output Enable Time INH→V_{OS} (L)	t_{PLZ}	2.0 4.5 6.0			15	150 30 26		190 38 33	ns
Output Enable Time INH→V_{OS} (H)	t_{PZH}	2.0 4.5 6.0			14	150 30 26		190 38 33	ns
Output Disable Time INH→V_{OS} (L)	t_{PZL}	2.0 4.5 6.0			15	150 30 26		190 38 33	ns
Sine Wave Distortion		2.0 4.5 6.0	R_L=10kΩ C_L=50pF f_i=1kHz, Y= $\frac{1}{2}$Vcc(P-P)		0.1				%
Crosstalk 2 channel		2.0 4.5 6.0	R_L=1kΩ Y= $\frac{1}{2}$Vcc (P-P)		t.b.f				MHz
Crosstalk (Address Input→Output)		2.0 4.5 6.0	R_L=10kΩ C_L=50pF INH or A, B, C=Vcc		t.b.f				mV
Feedthrough (OFF)		2.0 4.5 6.0	R_l=10kΩ C_L=50pF INH=GND, Y= $\frac{1}{2}$Vcc(P-P)		t.b.f				MHz
Frequency Response		2.0 4.5 6.0	R_L=1kΩ INH= $\frac{1}{2}$Vcc (P-P)		t.b.f				MHz

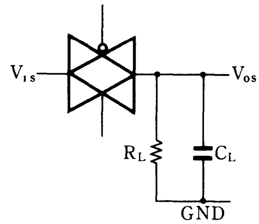
- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit

(Fig. 1) Propagation Delay Time, Output Disadle /Enable Time, Crosstalk Measuring Circuit



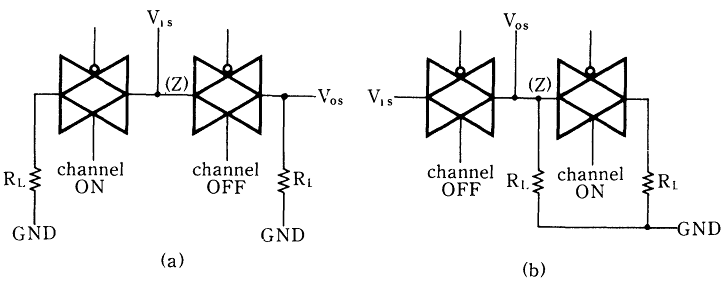
(Fig. 2) Sine Wave Distortion, Feedthrough, Frequency Response Measuring Circuit



$$20 \log \frac{V_{OS}}{V_{IS}} = -50\text{dB}$$

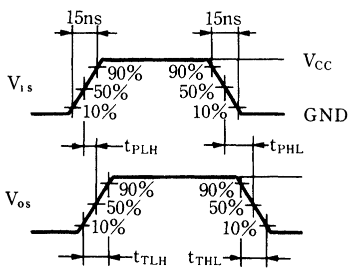
$$20 \log \frac{V_{OS}}{V_{IS}} = -3\text{dB}$$

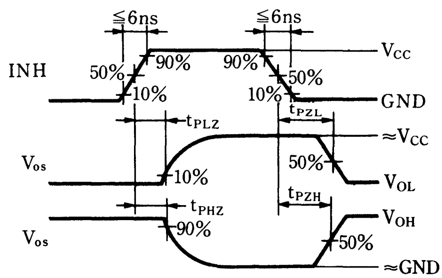
(Fig. 3) Crosstalk Measuring Crucit



$$20 \log \frac{V_{OS}}{V_{IS}} = -50\text{dB}$$

2. Waveforms





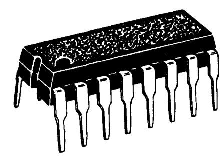
MN74HC4060/MN74HC4060S

14-Stage Ripple-Carry Binary Counter

■ Description

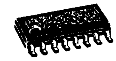
MN74HC4060/4060S are high-speed 14-stage ripple-carry counter. This counter provides increments on the falling edge of clock input. The clear input operates in the counter, and all outputs become "L" regardless of the clock, when the clear input is "H". The clock line is provided with 2-input terminal, which makes the connection with RC or crystal oscillation easy.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 familiy.

P- 3



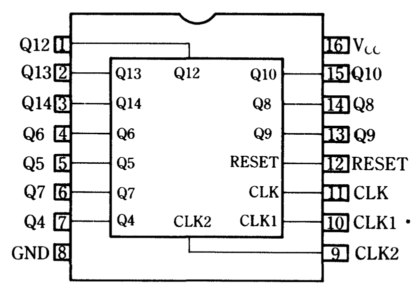
16-pin plastic DIL package

P- 4



16-pin Panaflat package (SO-16D)

Pin Configuration (top view)

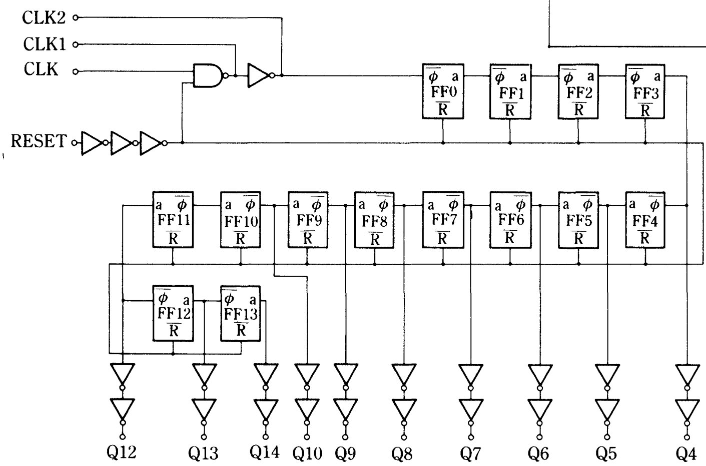


■ Truth Table

Clock	Reset	Output State
$\uparrow$	L	No Change
$\downarrow$	L	Advance to next state
×	H	All outputs are Low

Note:
1. $\uparrow$: The rise of clock from "L" to "H"
2. $\downarrow$: The fall of clock from "H" to "L"
3. × : Don't care.

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	°C
Power dissipation	MN74HC4060	Ta=−40～+60°C	P_D	.400	mW
		Ta=+60～+85°C		Decrease to 200m Watt the rate of 8mW/°C	
	MN74HC4060S	Ta+−40～+60°C	P_D	275	mW
		Ta=+60～+85°C		Decrease to 200m Watt the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operation supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	°C
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	
		6.0	0～400	

■ DC Characteristics (GND=0V)

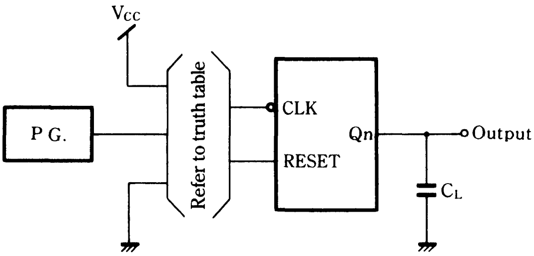
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40～+85°C min.	Ta=−40～+85°C max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	VI=V_{CC} or GND, I_O=0					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

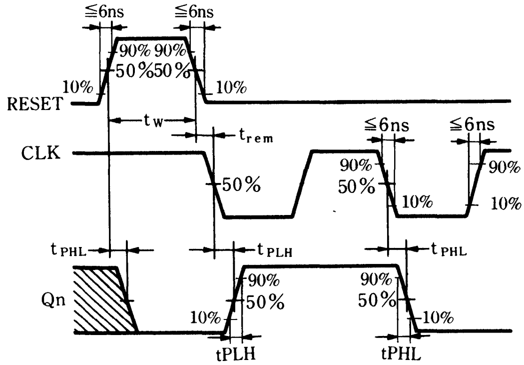
Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time CLK→Q4 (L→H)	t_{PLH}	2.0				330		415	ns
		4.5				66		83	
		6.0				56		70	
Propagation time CLK→Q4 (H→L)	t_{PHL}	2.0				330		415	ns
		4.5				66		83	
		6.0				56		70	
Propagation time Qn→Qn+1 (L→H)	t_{PLH}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Propagation time Qn→Qn+1 (H→L)	t_{PHL}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Propagation time RESET→Qn (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Propagation time CLK, RESET	t_W	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30			24		
		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Switching Waveforms



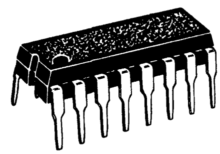
MN74HCT4060/MN74HCT4060S

14-Stage Ripple-Carry Binary Counter (TTL Input)

■ Description

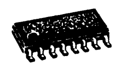
MN74HCT4060/MN74HCT4060S are high-speed 14-stage ripple-carry counter. This counter provides increments on the negative going edge of clock input. The clear input operates in the counter, and all outputs become "L" regardless of the clock, when the clear input is "H".
The clock line is provided with 2-input terminal, which makes the connection with RC or crystal oscillation easy.
All inputs are compatible with TTL logic level:0.8V or less is logic "0" input and 2.0V or more is logic "1".
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 familiy.

P- 3



16-pin plastic DIL package

P- 4



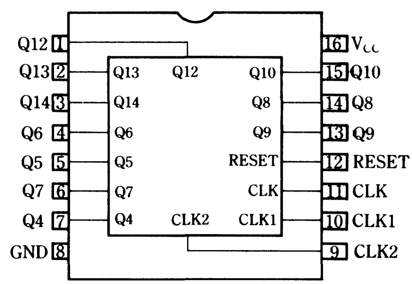
16-pin Panaflat package (SO-16D)

■ Truth Table

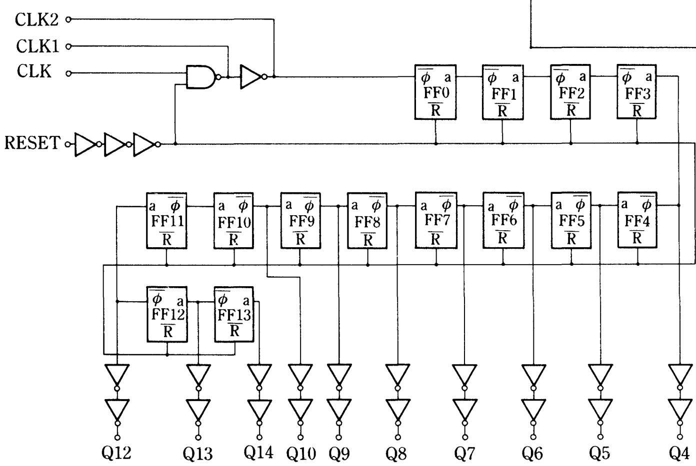
Clock	Reset	Output State
_/‾	L	No Change
‾_	L	Advance to next state
×	H	All outputs are Low

Note:
1. _/‾ : The rise of clock from "L" to "H"
2. ‾_ : The fall of clock from "H" to "L"
3. × : Don't care.

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	°C
Power dissipation	MN74HCT4060	Ta=−40∼±60°C	P_D	400	mW
		Ta=+60∼+85°C		Decrease to 200m Watt the rate of 8mW/°C	
	MN74HCT4060S	Ta+−40∼+60°C	P_D	275	mW
		Ta=+60∼+85°C		Decrease to 200m Watt the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operation supply voltage	V_{CC}		4.5∼5.5	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	°C
Input rise and fall time	t_r, t_f	4.5	0∼500	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
			V_I	I_O		Ta=25°C			Ta=−40∼+85°C		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	4.5 ≀ 5.5				2.0			2.0		V
Input LOW voltage	V_{IL}	4.5 5.5						0.8		0.8	V
Output HIGH voltage	V_{OH}	4.5	V_{IH} or V_{IL}	−20.0	μA	4.4	4.5		4.4		V
		4.5		−4.0	mA	3.86			3.76		
Output LOW voltage	V_{OL}	4.5	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		4.0	mA			0.32		0.37	
Input current	I_I	5.5	$V_I=V_{CC}$ or GND					±0.1		+1.0	μA
Quiescent supply current	I_{CC}	5.5	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ **AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)**

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Output rise time	t_{TLH}	4.5			8	15		19	ns
Output fall time	t_{THL}	4.5			6	15		19	ns
Propagation time CLK→Q4 (L→H)	t_{PLH}	4.5				66		83	ns
Propagation time CLK→Q4 (H→L)	t_{PHL}	4.5				66		83	ns
Propagation time Qn→Qn+1 (L→H)	t_{PLH}	4.5				20		25	ns
Propagation time Qn→Qn+1 (H→L)	t_{PHL}	4.5				20		25	ns
Propagation time RESET→Qn (H→L)	t_{PHL}	4.5				30		38	ns
Minimum pulse width	t_W	4.5				20		25	ns
Minimum recovery time	t_{rem}	4.5				15		19	ns
Maximum clock frequency	f_{max}	4.5		30			24		MHz

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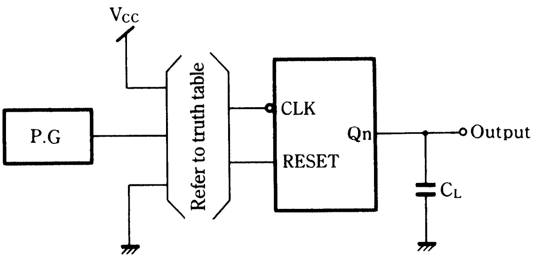
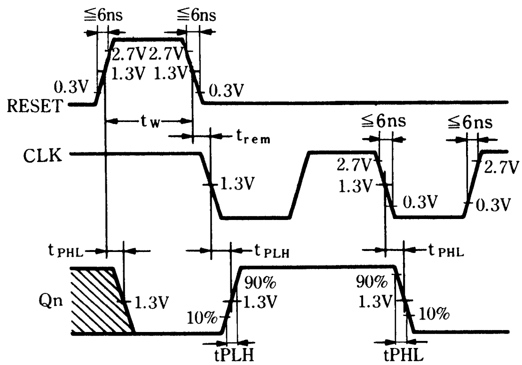
- Switching Time Measuring Circuit and Waveforms
  1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Switching Waveforms



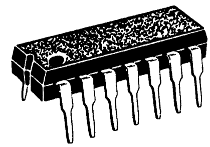
MN74HC4066/MN74HC4066S

Quad Analog Switch

■ Description

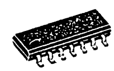
MN74HC4006/MN74HC4066S are quad independant bidirectional analog switch. When inhibit input (INH) is "H", the state between switch input and output becomes LOW impedance (ON). When inhibit input is "L", it becomes HIGH impedance (OFF). Pin configuration is same as standard CMOS logic 4000 family.

P-1



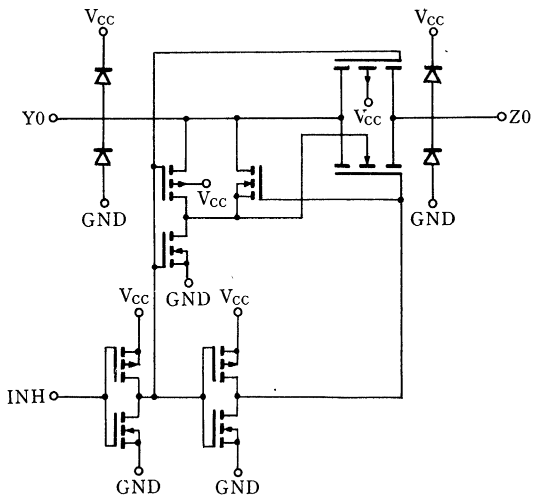
14-pin plastic DIL package

P-2

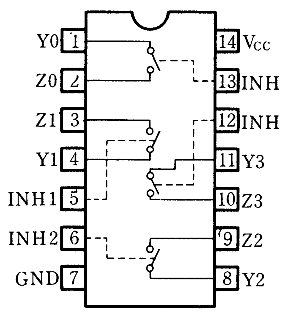


14-pin Panaflat package (SO-14D)

■ Schematic Diagram



Pin Configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input/output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	± 20	mA
Output parasitic diode current			I_{OK}	± 20	mA
Output current			I_O	± 35	mA
Supply current			I_{CC}, I_{GND}	± 70	mA
Storage temperature range			Tstg	$-65 \sim +150$	°C
Power dissipation	MN74HC4066	$Ta=-40 \sim +60$°C	P_D	400	mW
		$Ta=+60 \sim +85$°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4066S	$Ta=-40 \sim +60$°C	P_D	275	mW
		$Ta=+60 \sim +85$°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	V_{CC}		2.0～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0		1.5			1.5		V
		4.5		3.15			3.15		V
		6.0		4.2			4.2		V
Input LOW voltage	V_{IL}	2.0				0.3		0.3	V
		4.5				0.9		0.9	V
		6.0				1.2		1.2	V
Input current	I_I	6.0	V_I= Vcc or GND			±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I= V_{CC} or GND I_O=0			2.0		20.0	μA
Input/output off reak current	$I_{S(off)}$	6.0	V_I = V_{IH} or V_{IL} $\|V_S\|$ = V_{CC} or GND			±1.0		±0.1	μA
On resistance	R_{ON}	2.0	Vis : V_{CC}～GND		1000	2000		3000	Ω
		3.0			200	400		600	Ω
		4.5			80	160		240	Ω
		6.0			60	120		180	Ω
Variation of On resistance	ΔR_{ON}	2.0			150				Ω
		3.0			25				Ω
		4.5			10				Ω
		6.0			7				Ω

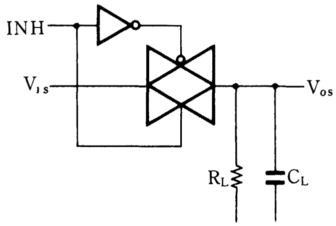
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Propagation time (H→L)	t_{PHL}	2.0	R_L=1kΩ, C_L=50pF, INH=Vcc, Input transition time=15ns			50		65	ns
		4.5				10		13	
		6.0				9		11	
Propagation time (L→H)	t_{PLH}	2.0				50		65	ns
		4.5				10		13	
		6.0				9		11	
3-state propagation time (H→Z)	t_{PHZ}	2.0	R_L=1kΩ, C_L=50pF, Y=Vcc, R_L→GND			150		190	ns
		4.5				30		38	
		6.0				26		33	
3-state propagation time (Z→H)	t_{PZH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
3-state propagation time (L→Z)	t_{PLZ}	2.0	R_L=10kΩ, C_L=50pF, Y=GND, R_L→Vcc			150		190	ns
		4.5				30		38	
		6.0				26		33	
3-state propagation time (Z→L)	t_{PZL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Sine Wave Distortion		2.0 / 4.5 / 6.0	R_L=10kΩ, C_L=50pF, fi=1kHz, Y=$\frac{1}{2}$Vcc(P-P)		0.1				%
Crosstalk 2 channel		2.0 / 4.5 / 6.0	P_L=1kΩ, Y=$\frac{1}{2}$Vcc(P-P)		t.b.f				MHz
Grosstalk INH→V_{SS}		2.0 / 4.5 / 6.0	R_L=10kΩ, C_L=50pF, INH=Vcc		t.b.f				mV
Feedthrough		2.0 / 4.5 / 6.0	R_L=1kΩ, C_L=50pF, INH=GND, Y=$\frac{1}{2}$Vcc(P-P)		t.b.f				MHz
Frequency Response		2.0 / 4.5 / 6.0	R_L=1kΩ, INH=Vcc		t.b.f				MHz

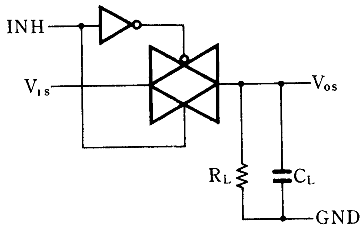
- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit (t_{PLH}, t_{PHL})

(Fig. 1) Propagation Delay Time, Crosstalk Measuring circuit

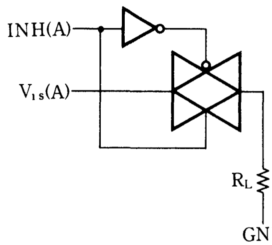


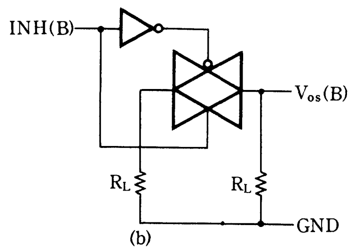
(Fig. 2) Sine Wave Distortion, Feedthrough Measuring Circuit



$$20 \log \frac{V_{OS}}{V_{IS}} = -50\text{dB}$$

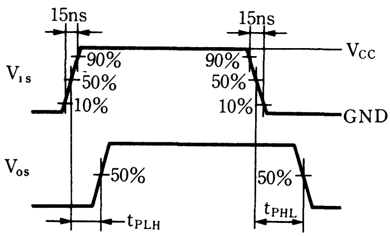
(Fig. 3) Crosstalk Measuring Circuit



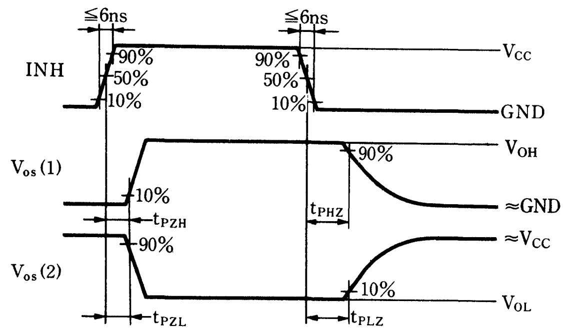


(b)

2. Switching Time Waveforms



($V_{IS} \rightarrow V_{OS}$)



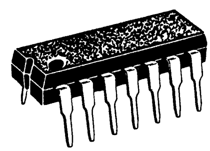
MN74HC4075/MN74HC4075S

Triple 3-Input OR Gates

■ Description

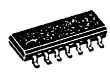
MN74HC4075/MN74HC4075S contain three 3-input positive isolation OR gate circuits.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to minimum. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard CMOS 4000 logic family.

P-1



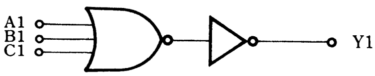
14-pin plastic DIL package

P-2

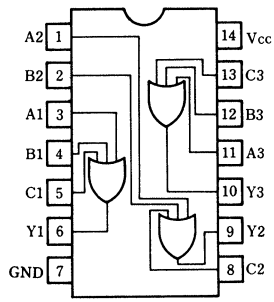


14-pin Panaflat package (SO-14D)

■ Logic Diagram (1 gate)



Pin Configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	−65～+150	°C
Power dissipation	MN74HC4075	Ta=−40～+60°C	P_D	400	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4075S	Ta=−40～+60°C	P_D	275	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Temperature Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t_{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

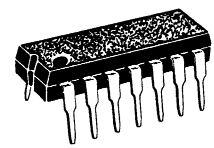
MN74HC4078/MN74HC4078S

8-Input NOR Gate

■ Description

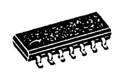
MN74HC4078/MN74HC4078S contain 8-input positive isolation NOR gate circuits.
Adoption of a silicon gate CMOS process has resulted in low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. Input/output transfer characteristics have been improved by applying a buffer to the gate output, and fluctuation of transfer time due to increased load capacitance is limited to the minimum. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{DD} and V_{SS} for protection of the input/output against damage by static electricity. Same pin configuration and function as the standard CMOS 4000 logic family.

P-1



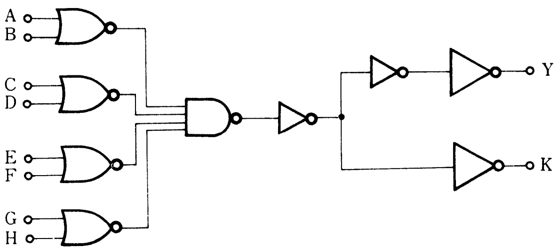
14-pin plastic DIL package

P-2

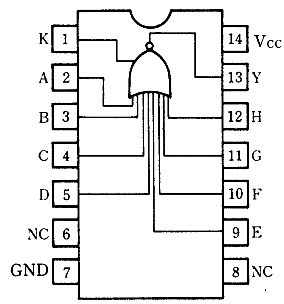


14-pin Panaflat package (SO-14D)

■ Logic Diagram



Pin Configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5∼+7.0	V
Input/output voltage			V_I, V_O	−0.5∼V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			T_{stg}	−65∼+150	℃
Power dissipation	MN74HC4078	Ta=−40∼+60°C	P_D	400	mW
		Ta=+60∼+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4078S	Ta=−40∼+60°C	P_D	275	mW
		Ta=+60∼+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	V_{CC}		1.4~6.0	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	Vcc (V)	Test Conditions V_I	I_O	Unit	Ta=25°C min.	typ.	max.	Ta=−40°C~+85°C min.	max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0. 3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0	0.1	1.9	0.1	V
		4.5	V_{IH}	−20.0	μA	4.4	4.5	0.1	4.4	0.1	
		6.0	or	−20.0	μA	5.9	6.0	0.1	5.9	0.1	
		4.5	V_{IL}	−4.0	mA	3.86		0.32	3.76	0.37	
		6.0		−5.2	mA	5.36		0.32	5.26	0.37	
Output LOW voltage	V_{OI}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	V_I=V_{CC} or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	V_I=V_{CC} or GND, I_O=0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Ta=25°C min.	typ.	max.	Ta=−40~+85°C min.	max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t_{PLH}	2.0				125		155	ns
		4.5			15	25		31	
		6.0				21		26	
Propagation time (H→L)	t_{PHL}	2.0				125		155	ns
		4.5			13	25		31	
		6.0				21		26	

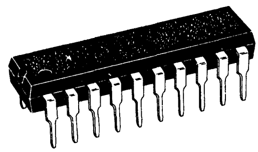
MN74HC4301/MN74HC4301S

TTL Input Octal TRI-STATE Latch with Inverting Outputs

■ Description

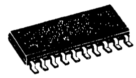
MN74HC4301/MN74HC4301S contain TTL input octal tri-state latches with inverting outputs. All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2.0V or more logic "1". High output driving capacity and tri-state output driving capacity and tri-state output are suited for the use of common bus line in the bus utilized system. When output disable input is "L", and latch enable input is "H", data input is inverted and transferred to output.
When latch enable is "L", data input is maintained as is until when latch enable input becomes "H" again.
When output disable input is "H", all outputs become high impedance state regardless of other inputs or data hold circuits.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directry driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-5



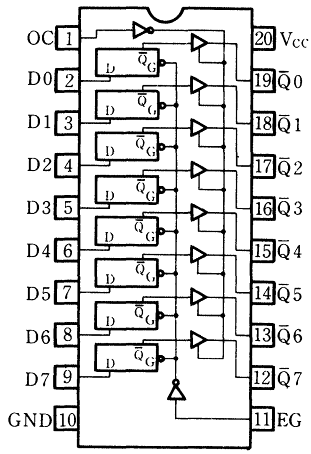
20-pin plastic DIL package

P-6



20-pin Panaflat package (SO-20D)

Pin Configuration (top view)

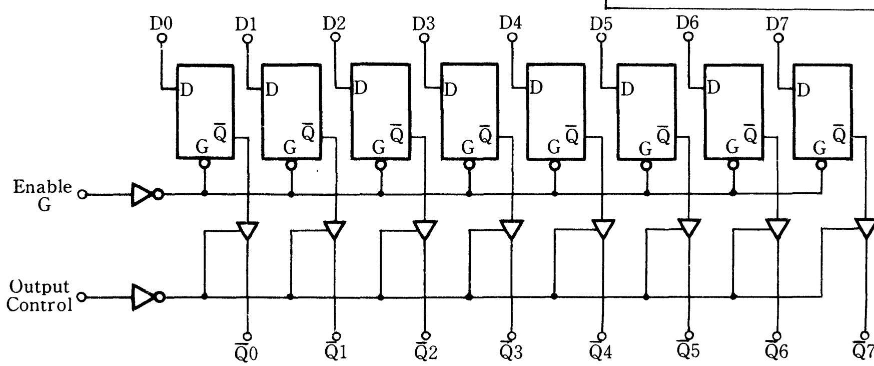


■ Truth Table

Output Control	Enable	D	Output
L	H	H	L
L	H	L	H
L	L	×	Q_0
H	×	×	Hi-Z

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance
3. Q_O: Q level prior to determination of input condition shown in table

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	± 70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74 HC4301	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74 HC4301 S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		4.5～5.5	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	TA		−40～+85	℃
Input rise and fall time	tr, tf	4.5	0～500	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	4.5 ～ 5.5				2.0			2.0		V
Input LOW voltage	V_{IL}	4.5 ～ 5.5						0.8		0.8	V
Output HIGH voltage	V_{OH}	4.5	V_{IH} or V_{IL}	−20.0	μA	4.4	4.5		4.4		V
		4.5		− 6.0	mA	3.86			3.76		V
Output LOW voltage	V_{OL}	4.5	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		6.0	mA			0.32		0.37	V
Input current	I_I	5.5	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	5.5	V_I = V_{IH} or V_{IL} V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	5.5	V_I = V_{CC} or GND, I_O=0					8.0		80.0	μA

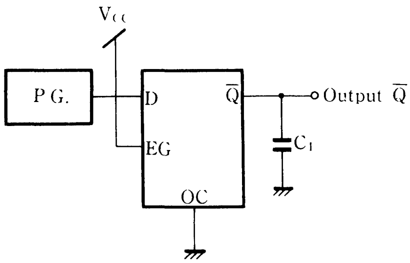
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Condition Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Output rise time	t_{TLH}	4.5			8	15		19	ns
Output fall time	t_{THL}	4.5			7	15		19	ns
Propagation time D→$\overline{Q}$ (L→H)	t_{PLH}	4.5			10	20		25	ns
Propagation time D→$\overline{Q}$ (H→L)	t_{PHL}	4.5			14	25		31	ns
Propagation time enable G→$\overline{Q}$(L→H)	t_{PLH}	4.5			12	25		31	ns
Propagation time enable G→$\overline{Q}$(H→L)	t_{PHL}	4.5			17	30		38	ns
3-state propagation time (H→Z)	t_{PHZ}	4.5	R_L = 1kΩ		15	25		31	ns
3-state propagation time (L→Z)	t_{PLZ}	4.5	R_L = 1kΩ		15	25		31	ns
3-state propagation time (Z→H)	t_{PZH}	4.5	R_L = 1kΩ		10	20		25	ns
3-state propagation time (Z→L)	t_{PZL}	4.5	R_L = 1kΩ		18	30		38	ns

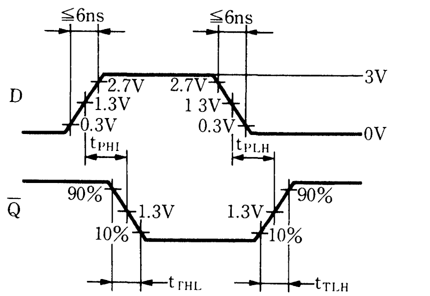
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}/t_{PHL} (D→$\overline{Q}$)

1. Measuring Circuit

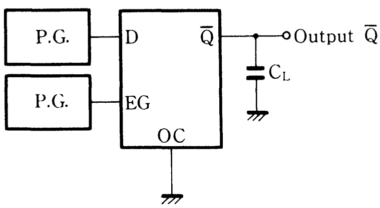


2. Waveforms

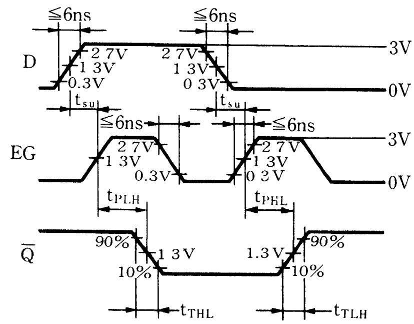


〔2〕 t_{PLH}/t_{PHL} (EG→$\overline{Q}$)

1. Measuring Circuit

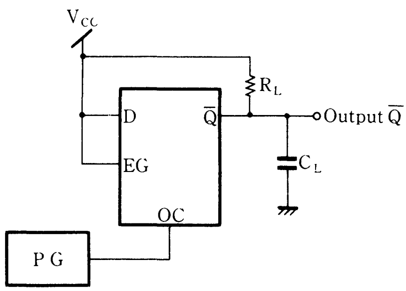


2. Waveforms

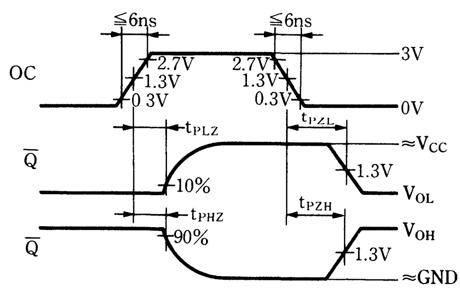


〔3〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

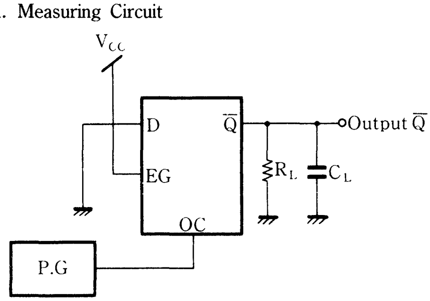


2. Waveforms



〔4〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [3] 2. for waveforms.

MN74HC4302/MN74HC4302S

TTL Input Octal TRI-STATE Latches

■ Description

MN74HC4302/MN74HC4302S contain TTL input octal tri-state latches with outputs. All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2.0V or more logic "1". High output driving capacity and tri-state output driving capacity and tri-state output are suited for the use of common bus line in the bus utilized system. When output disable input is "L", and latch enable input is "H", data input is inverted and transferred to output. When latch enable is "L", data input is maintained as is until when latch enable input becomes "H" again.
When output disable input is "H", all outputs become high impedance state regardless of other inputs or data hold circuits. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directry driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

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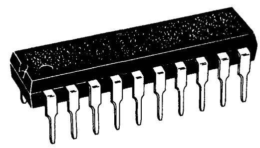
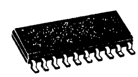


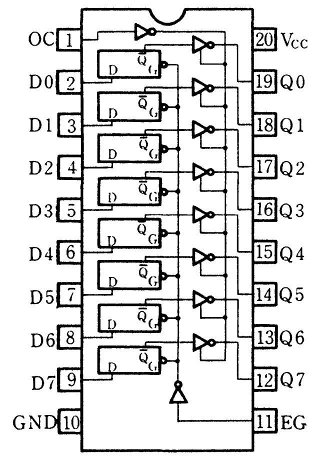
20-pin plastic DIL package

P-6



20-pin Panaflat package (SO-20D)

Pin Configuration (top view)

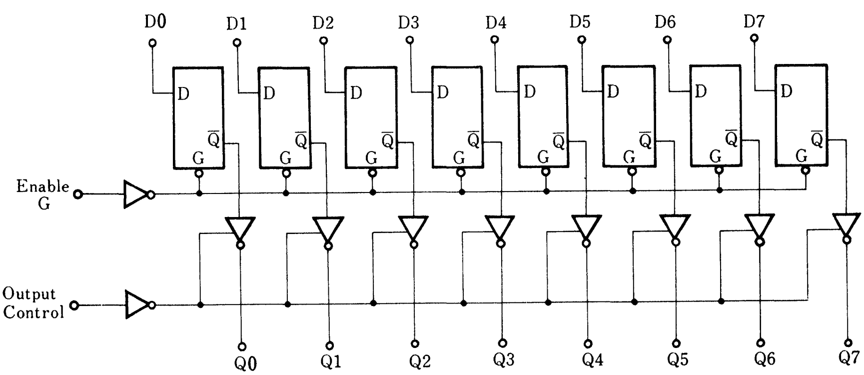


■ Truth Table

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	×	Q_0
H	×	×	Hi-Z

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. Hi-Z: High impedance
3. Q_O: Q level prior to determination of input condition shown in table

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input/output voltage			V_I, V_O	−0.5~V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65~+150	℃
Power dissipation	MN74HC4302	Ta=−40~+60℃	P_D	400	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4302S	Ta=−40~+60℃	P_D	275	mW
		Ta=+60~+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}	Rating	Unit
Operating supply voltage	V_{CC}		4.5~5.5	V
Input/output voltage	V_I, V_O		0~V_{CC}	V
Operating temperature range	T_A		−40~+85	℃
Input rise and fall time	t_r, t_f	4.5V	0~500	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40~+85℃ min.	Ta=−40~+85℃ max.	Unit
Input HIGH voltage	V_{IH}	4.5 ~ 5.5				2.0			2.0		V
Input LOW voltage	V_{IL}	4.5 ~ 5.5						0.8		0.8	V
Output HIGH voltage	V_{OH}	4.5	V_{IH} or V_{IL}	−20.0	μA	4.4	4.5		4.4		V
		4.5		−6.0	mA	3.86			3.76		V
Output LOW voltage	V_{OL}	4.5	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		6.0	mA			0.32		0.37	V
Input current	I_I	5.5	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	5.5	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	5.5	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

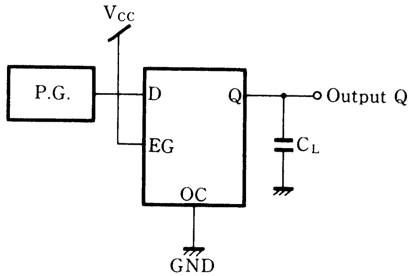
■ **AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)**

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40~+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	4.5			7	15		19	ns
Output fall time	t_{THL}	4.5			6	15		19	ns
Propagation time D→Q (L→H)	t_{PLH}	4.5			11	20		25	ns
Propagation time D→Q (H→L)	t_{PHL}	4.5			16	30		38	ns
Propagation time enable G→Q(L→H)	t_{PLH}	4.5			15	25		31	ns
Propagation time enable G→Q(H→L)	t_{PHL}	4.5			15	25		31	ns
3-state propagation time (H→Z)	t_{PHZ}	4.5	R_L= 1kΩ		10	25		31	ns
3-state propagation time (L→Z)	t_{PLZ}	4.5	R_L= 1kΩ		16	30		38	ns
3-state propagation time (Z→H)	t_{PZH}	4.5	R_L= 1kΩ		9	20		25	ns
3-state propagation time (Z→L)	t_{PZL}	4.5	R_L= 1kΩ		18	30		38	ns

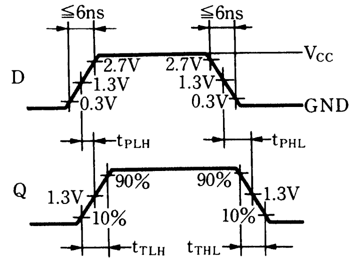
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}/t_{PHL}(D→Q)

1. Measuring Circuit

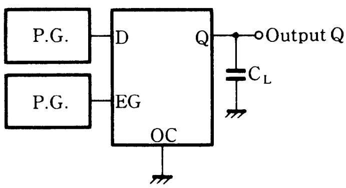


2. Waveforms

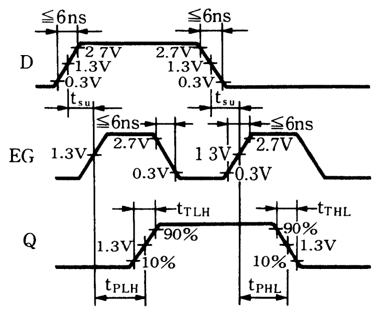


〔2〕 t_{PLH}/t_{PHL}(ENG→Q)

1. Measuring Circuit

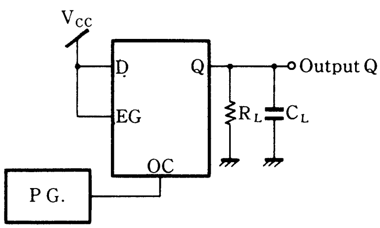


2. Waveforms

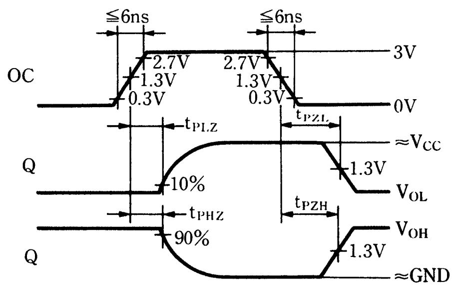


〔3〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

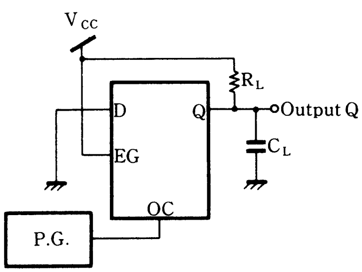


2. Waveforms



〔4〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [3] 2. for waveforms.

MN74HC4303/MN74HC4303S

TTL Input Octal TRI-STATE D-Type Flip-Flops with Inverting Outputs

■ Description

MN74HC4303/MN74HC3403S are TTL input octal tri-state D-type flip-flop with inverting outputs. All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2.0V or more logic "1". High output driving capacity and tri-state output are suited for the use of common bus line in the bus utilized system D input data satisfying set-up time is inverted by the rising edge of clock input and trasferred to output. When output disable input is "H", all outputs become high impedance regardless of other inputs or data hold circuits.

Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

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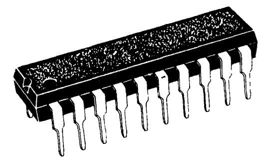
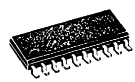


20-pin plastic DIL package

P-6



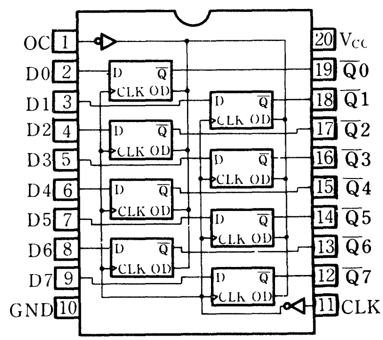
20-pin Panaflat package (SO-20D)

■ Truth Table

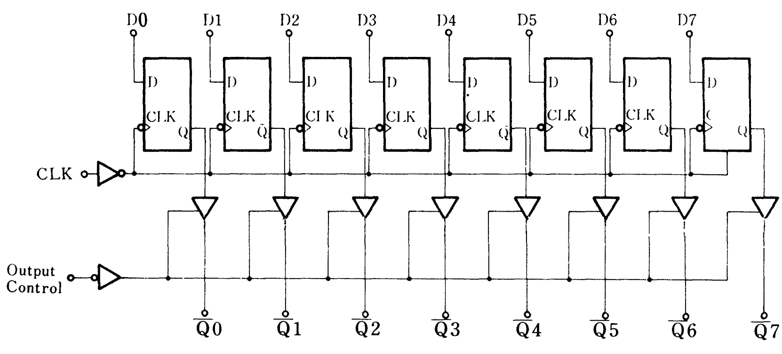
Input			Output
Output Control	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	×	Q_0
H	×	×	Hi-Z

Note:
1. ↑: Data input is transferred to output on the positive-going edge from LOW to HIGH of the clock
2. ×: Either HIGH or LOW; it doesn't matter
3. Q_0: Q level prior to determination of input condition shown in table
4. Hi-Z: High impedance

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC4303	Ta=$-40\sim+60$℃	P_D	400	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4303S	Ta=$-40\sim+60$℃	P_D	275	mW
		Ta=$+60\sim+85$℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		$4.5\sim5.5$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	4.5	$0\sim500$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=$-40\sim+85$℃ min.	Ta=$-40\sim+85$℃ max.	Unit
Input HIGH voltage	V_{IH}	4.5 ∼ 5.5				2.0			2.0		V
Input LOW voltage	V_{IL}	4.5 ∼ 5.5						0.8		0.8	V
Output HIGH voltage	V_{OH}	4.5	V_{IH} or V_{IL}	-20.0	µA	4.4	4.5		4.4		V
		4.5		-6.0	mA	3.86			3.76		V
Output LOW voltage	V_{OL}	4.5	V_{IH} or V_{IL}	20.0	µA		0.0	0.1		0.01	V
		4.5		6.0	mA			0.32		0.37	V
Input current	I_I	5.5	$V_I=V_{CC}$ or GND					±0.1		1.0	µA
3-state output off state current	I_{OZ}	5.5	$V_I=V_{IH}$ or V_{IL}, $V_O=V_{CC}$ or GND					±0.5		±5.0	µA
Quiescent supply current	I_{CC}	5.5	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	µA

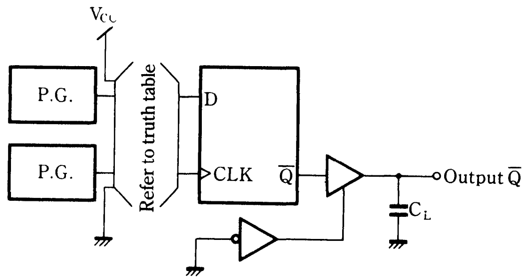
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40~+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	4.5			8	15		19	ns
Output fall time	t_{THL}	4.5			6	15		19	ns
Propagation time CLK→$\overline{Q}$ (L→H)	t_{PLH}	4.5			13	30		38	ns
Propagation time CLK→$\overline{Q}$ (H→L)	t_{PHL}	4.5			18	30		38	ns
3-state propagation time (H→Z)	t_{PHZ}	4.5	R_L= 1 kΩ		18	30		38	
3-state propagation time (L→Z)	t_{PLZ}	4.5	R_L= 1 kΩ		15	25		31	ns
3-state propagation time (Z→H)	t_{PZH}	4.5	R_L= 1 kΩ		14	25		31	ns
3-state propagation time (Z→L)	t_{PZL}	4.5	R_L= 1 kΩ		14	25		31	ns
Minimum Set-up time	t_{su}	4.5			2	20		25	ns
Minimum Hold time	t_h	4.5			—	0			ns
Maximum clock frequency	f_{max}	4.5		30	79		24		MHz

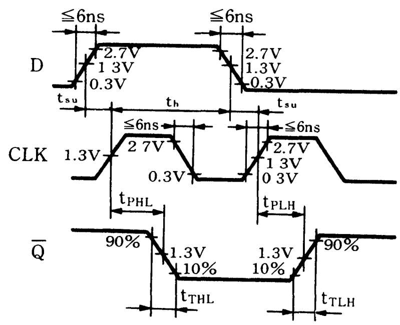
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{su}, f_{max}, t_{PLH} / t_{PHL} (CLK→$\overline{Q}$)

1. Measuring Circuit

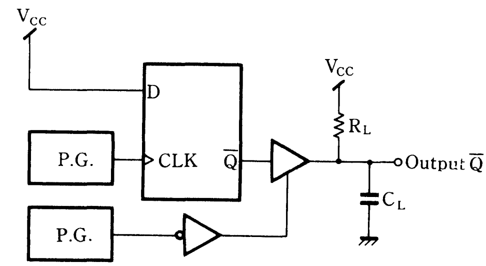


2. Waveforms

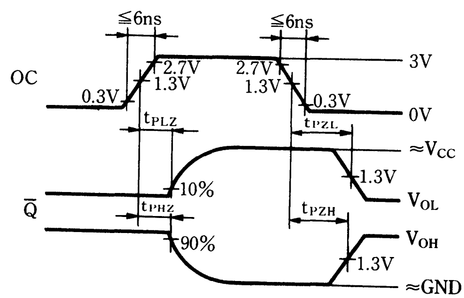


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

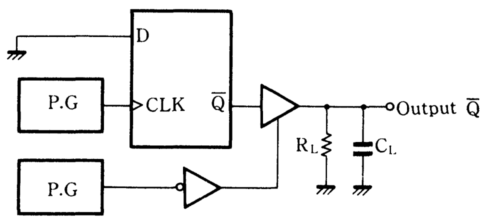


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [3] 2. for waveforms.

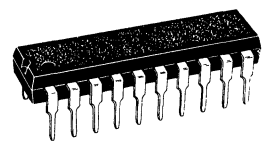
MN74HC4304/MN74HC4304S

TTL Input Octal TRI-STATE Flip-Flops

■ Description

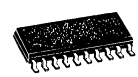
MN74HC4304/MN74HC4304S are TTL input octal tri-state D type flip-flop. All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2.0V or more logic "1".
High output driving capacity and tri-state output are suited for the use of common bus line in the bus utilized system. D input data satisfying set-up time is transferred to output by the rising edge of clock input. When output disable input is "H", all outputs become high impedance regardless of other inputs or data hold circuits. Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard 54LS/74LS logic family.

P-5



20-pin plastic DIL package

P-6



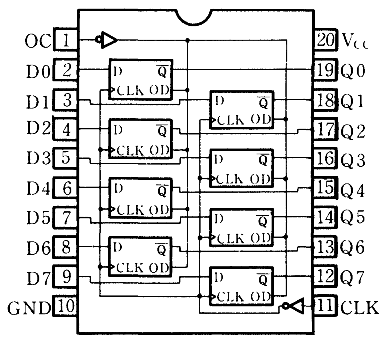
20-pin Panaflat package (SO-20D)

■ Truth Table

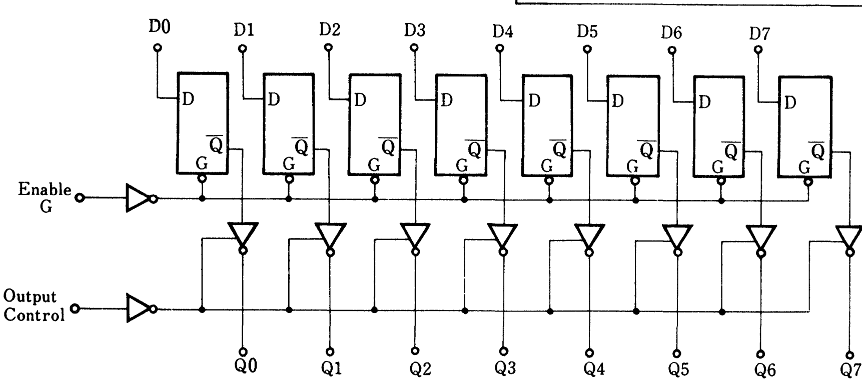
Input			Output
Output Control	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	×	Q_0
H	×	×	Hi-Z

Note:
1. ↑: Data input is transferred to output on the positive-going edge from LOW to HIGH of the clock
2. ×: Either HIGH or LOW; it doesn't matter
3. Q_O: Q level prior to determination of input condition shown in table
4. Hi-Z: High impedance

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HN4304	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4304S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	Vcc(V)	Rating	Unit
Operating supply voltage	V_{CC}		4.5～5.5	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	4.5V	0～500	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions			Temperature					Unit
				I_O		Ta=25℃			T_a=−40～+85℃		
					Unit	min.	typ.	max.	min.	max.	
Input HIGH voltage	V_{IH}	4.5～5.5				2.0			2.0		V
Input LOW voltage	V_{IL}	4.5～5.5						0.8		0.8	V
Output HIGH voltage	V_{OH}	4.5	V_{IH} or V_{IL}	−20.0	μA	4.4	4.5		4.4		V
		4.5		− 6.0	mA	3.86			3.76		V
Output LOW voltage	V_{OL}	4.5	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		6.0	mA			0.32		0.37	V
Input current	I_I	5.5	V_I=V_{CC} or GND					±0.1		±0.1	μA
3-state output off state current	I_{OZ}	5.5	V_I=V_{IH} or V_{IL} V_O=V_{CC} or GND					±0.5		±0.5	μA
Quiescent supply current	I_{CC}	5.5	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

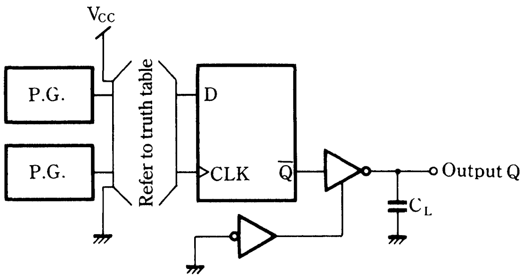
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40~+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	4.5			8	15		19	ns
Output fall time	t_{THL}	4.5			6	15		19	ns
Propagation time CLK→Q (L→H)	t_{PLH}	4.5			15	30		38	ns
Propagation time CLK→Q (H→L)	t_{PHL}	4.5			16	30		38	ns
3-state propagation time (H→Z)	t_{PHZ}	4.5	R_L=1kΩ		16	20		25	ns
3-state propagation time (L→Z)	t_{PLZ}	4.5	R_L=1kΩ		15	20		25	ns
3-state propagation time (Z→H)	t_{PZH}	4.5	R_L=1kΩ		14	20		25	ns
3-state propagation time (Z→L)	t_{PZL}	4.5	R_L=1kΩ		14	20		25	ns
Minimum Set-up time	t_{su}	4.5			2	20		25	ns
Minimum Hold time	t_h	4.5			—	0			ns
Maximum clock frequency	f_{max}	4.5		30	87		24		MHz

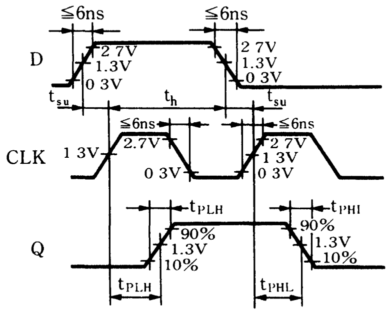
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, tsu, fmax, t_{PLH}, t_{PHL} (CLK→Q)

1. Measurıng Circuit

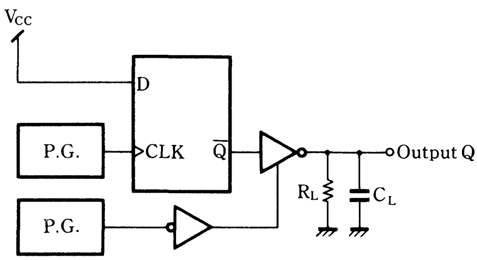


2. Waveforms

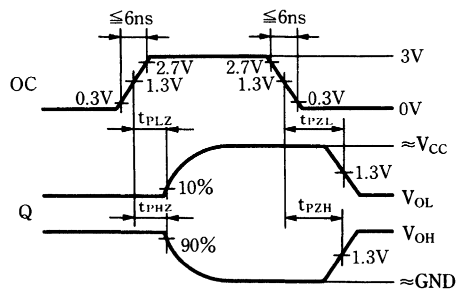


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

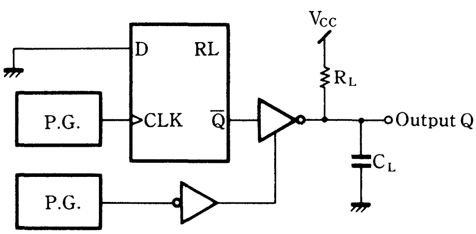


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

MN74HC4305/MN74HC4305S

TTL Input Octal TRI-STATE Inverting Buffers

■ Description

MN74HC4305/MN74HC4305S are TTL input octal tri-state inverting buffer.
All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2.0V or more is logic "1". Large current output makes possible high-speed operation for driving a large capacity busline. It has input $\overline{1G}$ and $\overline{2G}$ where output becomes enabled at LOW, and each can control 4 buffers.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity.

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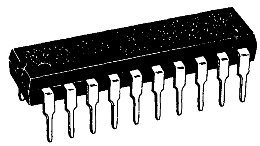
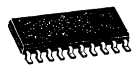


20-pin plastic DIL package

P-6



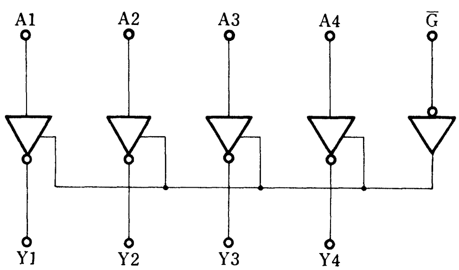
20-pin Panaflat package (SO-20D)

■ Truth Table

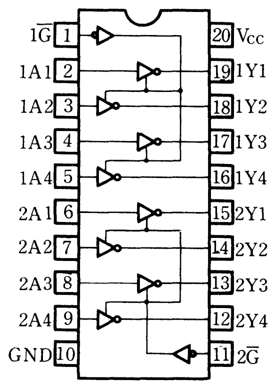
Input		Output	Input		Output
$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Hi-Z	H	L	Hi-Z
H	H	Hi-Z	H	H	Hi-Z

Note:
Hi-Z: High impedance

■ Logic Diagram



Pin Configuration (top view)



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC4305	Ta=−40～+60°C	P_D	400	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4305S	Ta=−40～+60°C	P_D	275	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		4.5～5.5	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	°C
Input rise and fall time	t_r, t_f	4.5	0～500	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40～+85°C min.	Ta=−40～+85°C max.	Unit
Input HIGH voltage	V_{IH}	4.5～5.5				2.0			2.0		V
Input LOW voltage	V_{IL}	4.5～5.5						0.8		0.8	V
Output HIGH voltage	V_{OH}	4.5	V_{IH} or V_{IL}	−20.0	μA	4.4	4.5		4.4		V
		4.5		−6.0	mA	3.86			3.76		V
Output LOW voltage	V_{OL}	4.5	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		6.0	mA			0.32		0.37	V
Input current	I_I	5.5	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	5.5	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	5.5	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

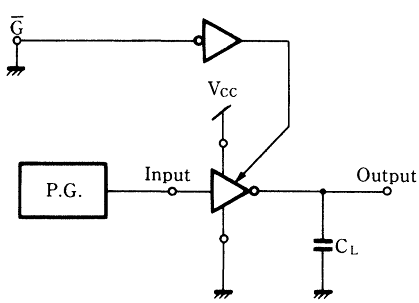
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40～+85℃ min.	max.	Unit
Minimum Set-up time	t_{TLH}	4.5			8	15		19	ns
Output fall time	t_{THL}	4.5			6	15		19	ns
Propagation time (L→H)	t_{PLH}	4.5			8	20		25	ns
Propagation time (H→L)	t_{PHL}	4.5			8	20		25	ns
3-state propagation time (H→Z)	t_{PHZ}	4.5	R_L= 1 kΩ		12	25		31	ns
3-state propagation time (L→Z)	t_{PLZ}	4.5	R_L= 1 kΩ		10	25		31	ns
3-state propagation time (Z→H)	t_{PZH}	4.5	R_L= 1 kΩ		12	20		25	ns
3-state propagation time (Z→L)	t_{PZL}	4.5	R_L= 1 kΩ		17	30		38	ns

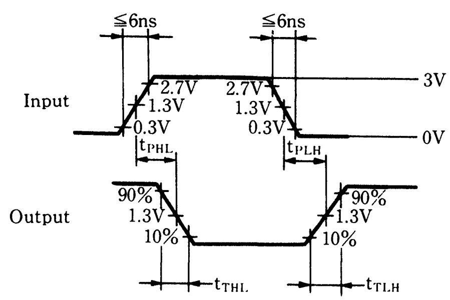
● Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

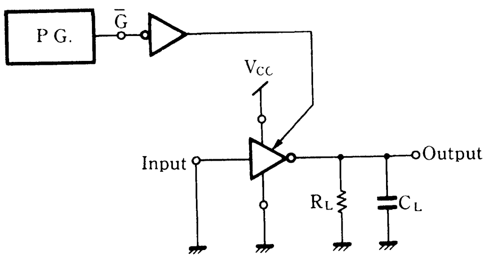


2. Waveforms

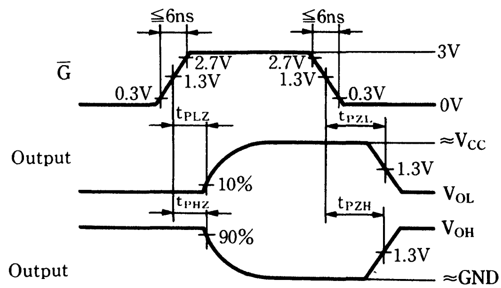


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

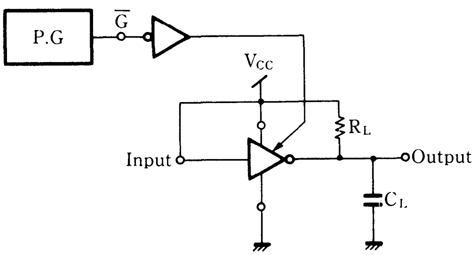


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

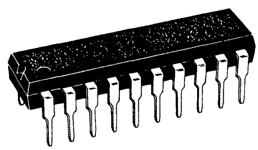
MN74HC4306/MN74HC4306S

TTL Input Octal TRI-STATE Buffer

■ Description

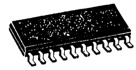
MN74HC4305/MN74HC4305S are TTL input octal tri-state buffer.
All inputs are compatible with TTL logic level: 0.8V or less is logic "0" and 2.0V or more is logic "1". Large current output makes possible high-speed operation for driving a large capacity busline. It has input $1\overline{G}$ and $2\overline{G}$ where output becomes enabled at LOW, and each can control 4 buffers.
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity.

P-5



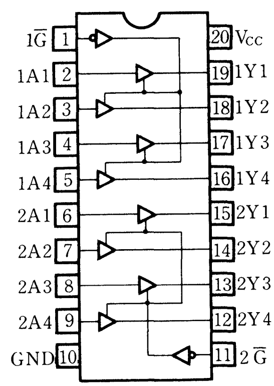
20-pin plastic DIL package

P-6



20-pin Panaflat package (SO-20D)

Pin Configuration (top view)

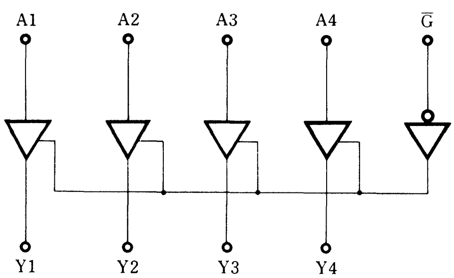


■ Truth Table

Input		Output	Input		Output
$1\overline{G}$	1 A	1 Y	$2\overline{G}$	2 A	2 Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Hi-Z	H	L	Hi-Z
H	H	Hi-Z	H	H	Hi-Z

Note:
Hi-Z: High impedance

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	−65～+150	℃
Power dissipation	MN74HC4306	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4306S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		4.5～5.5	V
Input/output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature range	T_A		−40～+85	℃
Input rise and fall time	t_r, t_f	4.5	0～500	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	Test Conditions Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	4.5 ～ 5.5				2.0			2.0		V
Input LOW voltage	V_{IL}	4.5 ～ 5.5						0.8		0.8	V
Output HIGH voltage	V_{OH}	4.5	V_{IH} or V_{IL}	−20.0	μA	4.4	4.5		4.4		V
		4.5		−6.0	mA	3.86			3.76		V
Output LOW voltage	V_{OL}	4.5	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		6.0	mA			0.32		0.37	V
Input current	I_I	5.5	V_I=V_{CC} or GND					±0.1		±1.0	μA
3-state output off state current	I_{OZ}	5.5	V_I=V_{IH} or V_{IL}, V_O=V_{CC} or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	5.5	V_I=V_{CC} or GND, I_O=0					8.0		80.0	μA

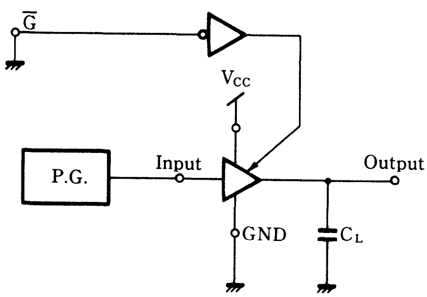
■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

Parameter	Symbol	Vcc (V)	Test Conditions	Temperature					Unit
				Ta=25℃			Ta=−40~+85℃		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	4.5			8	15		19	ns
Output fall time	t_{THL}	4.5			6	15		19	ns
Propagation time (L→H)	t_{PLH}	4.5			8	20		25	ns
Propagation time (H→L)	t_{PHL}	4.5			12	20		25	ns
3-state propagation time (H→Z)	t_{PHZ}	4.5	R_L= 1 kΩ		14	25		31	ns
3-state propagation time (L→Z)	t_{PLZ}	4.5	R_L= 1 kΩ		14	25		31	ns
3-state propagation time (Z→H)	t_{PZH}	4.5	R_L= 1 kΩ		10	20		25	ns
3-state propagation time (Z→L)	t_{PZL}	4.5	R_L= 1 kΩ		14	25		31	ns

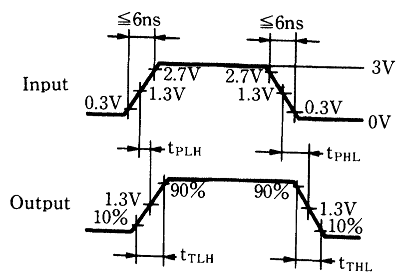
- Switching Time Measuring Circuit and Waveforms

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measuring Circuit

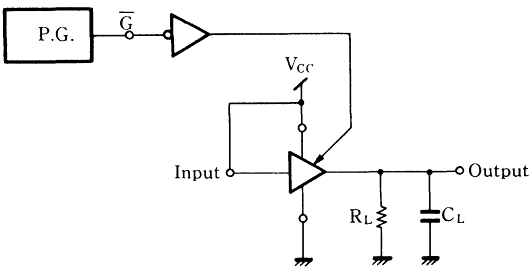


2. Waveforms

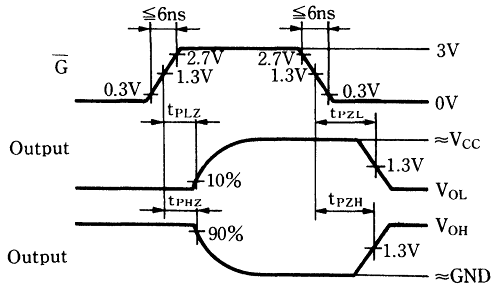


〔2〕 t_{PHZ}, t_{PZH}

1. Measuring Circuit

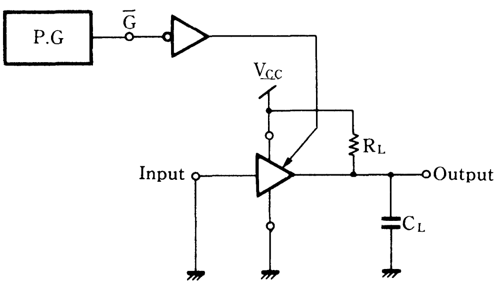


2. Waveforms



〔3〕 t_{PLZ}, t_{PZL}

1. Measuring Circuit



2. Waveforms

See above [2] 2. for waveforms.

MN74HC4520/MN74HC4520S

Dual Binary Up Counter

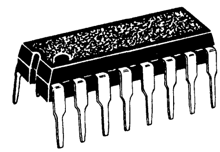
■ Description

MN74HC4520/MN74HC4520S contain independent dual 4-bit binary up counters.

It is counted by the rise of CLK, when $\overline{CLK}$ is "H" and counted by the fall of CLK, when $\overline{CLK}$ is "L". When clear input is "H", it clears the counter regardless of clock and all outputs (Q0~Q3) is "L".

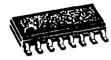
Adoption of a silicon gate CMOS process has made possible low power dissipation, a high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 10-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity. Same pin configuration and function as the standard CMOS logic 4000 family.

P-3



16-pin plastic DIL package

P-4



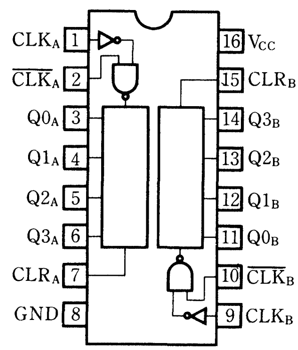
16-pin Panaflat package (SO-16D)

■ Truth Table

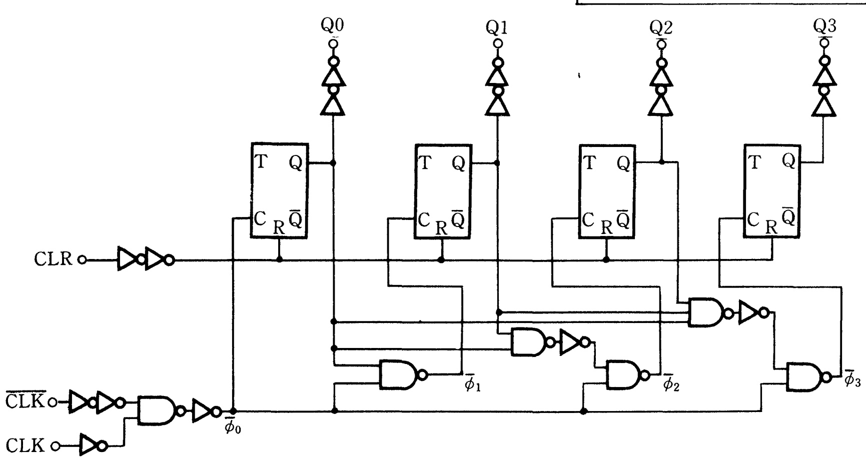
CLK	$\overline{CLK}$	CLR	Mode
×	×	H	All outputs are low
↑	H	L	Counter Advances
L	↓	L	Counter Advances
↓	×	L	No Change
×	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change

Note:
1. ×: Either HIGH or LOW; it doesn't matter
2. ↓: The fall of clock from "H" to "L"
3. ↑: The rise of clock from "L" to "H"

Pin Configuration (top view)



■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature range			Tstg	$-65\sim+150$	℃
Power dissipation	MN74HC4520	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC4520S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operating supply voltage	V_{CC}		$1.4\sim6.0$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	℃
Input rise and fall time	t_r, t_f	2.0	$0\sim1000$	ns
		4.5	$0\sim500$	ns
		6.0	$0\sim400$	ns

■ DC Characteristics (GND=0V)

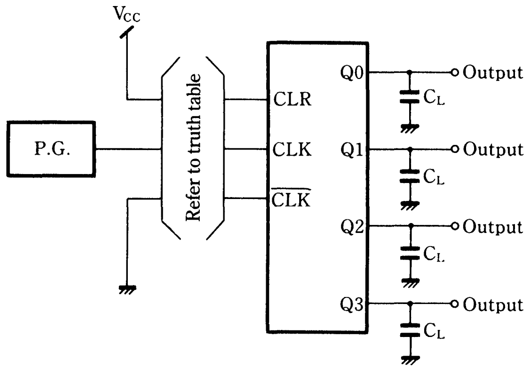
Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25℃ min.	Ta=25℃ typ.	Ta=25℃ max.	Ta=−40～+85℃ min.	Ta=−40～+85℃ max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0	V_{IH} or V_{IH}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Quiescent supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time ≦6ns, C_L=50pF)

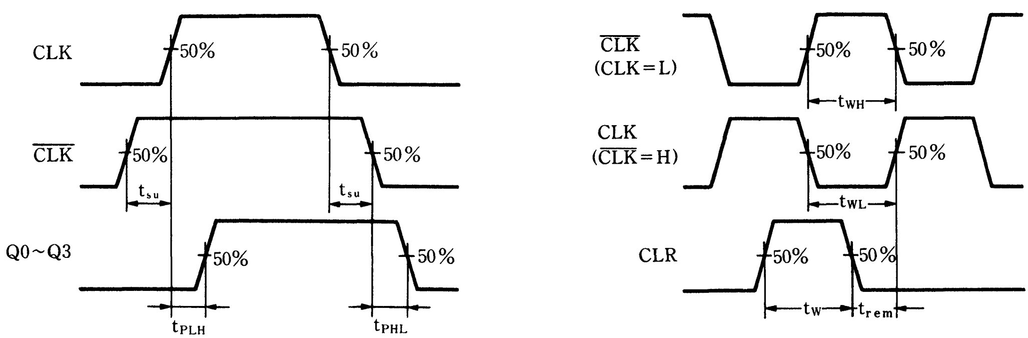
Parameter	Symbol	Vcc (V)	Test Conditions	Temperature Ta=25℃ min.	typ.	max.	Ta=−40~+85℃ min.	max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time CLK, $\overline{CLK}$→Q_0 (L→H)	t_{PLH}	2.0				175		220	ns
		4.5				35		44	
		6.0				30		37	
Propagation time CLK→$\overline{CLK}$→Q_0 (H→L)	t_{PHL}	2.0				175		220	ns
		4.5				35		44	
		6.0				30		37	
Propagation time CLK, $\overline{CLK}$→Q_3 (L→H)	t_{PLH}	2.0				250		315	ns
		4.5				50		63	
		6.0				43		54	
Propagation time CLK, $\overline{CLK}$→Q_3 (H→L)	t_{PHL}	2.0				250		315	ns
		4.5				50		63	
		6.0				43		54	
Propagation time CLR→Q_3 (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Low level Minimum pulse width CLK	t_{WL}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
High level Minimum pulse width $\overline{CLK}$	t_{WH}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum pulse width CLR	t_{WCD}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Minimum Set-up time CLK→$\overline{CLK}$	t_{su}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Minimum Set-up time $\overline{CLK}$→CLK	t_{su}	2.0				50		65	ns
		4.5				10		13	
		6.0				9		11	
Minimum recovery time	t_{rem}	2.0				75		95	ns
		4.5				15		19	
		6.0				13		16	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30			24		
		6.0		35			28		

- Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit



2. Waveforms



MN74HC40104/MN74HC40104S

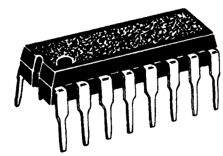
4-Bit TRI-STATE Bidirectional Universal Shift Register

■ Description

MN74HC40104/MN74HC40104S are 4-bit 3-state bidirectional shift registers with parallel inputs, parallel outputs, right-shift and left-shift serial inputs, and operational mode control inputs.
Large current output makes possible high-speed operation for driving a large capacity busline.
For sysnchronized-parallel loads, 4-bit data are added to the parallel input, when both mode control inputs (S0 and S1) are HIGH.
Data are loaded to the respective flip-flops, and are transferred to the outut on the positive going edge of the clock pulse.
The serial-shift function can be stopped between parallel loads.
The right shift functions (when mode-control input S0 is HIGH and S1 is LOW) when there is synchronization to the rise of the clock pulse.
When S0 is LOW and S1 is HIGH, the left shift functions as a result of insertion of new data to the left-shift serial input.

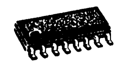
When S0 is LOW and S1 is LOW, all outputs become LOW regardless of the clock pulse.
When enable input is LOW, all outputs become high impedance.
Adoption of a silicon gate CMOS process has made possible low power dissipation, high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity.
Same pin configuration and function as the standard CMOS logic 4000 family.

P- 3



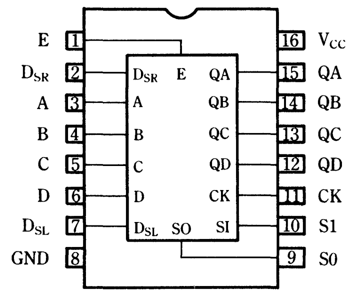
16-pin plastic DIL package

P- 4



16-pin Panaflat package (SO-16D)

Pin Configuration (top view)

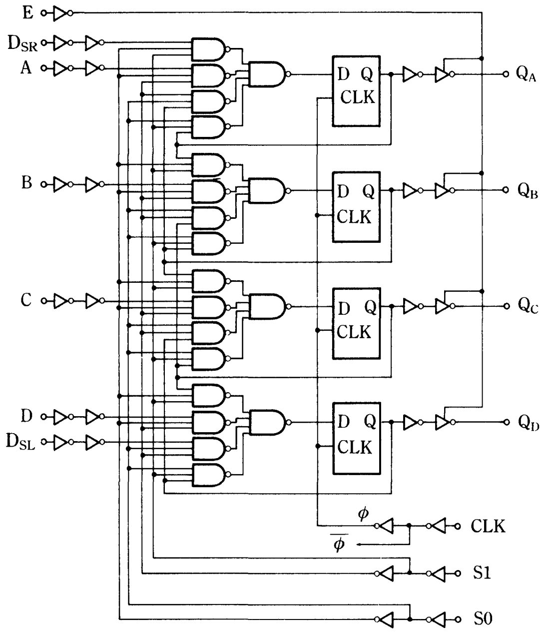


■ Truth Table

Input										Output			
Enable E	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0		D_{SL}	D_{SR}	A	B	C	D				
L	×	×	×	×	×	×	×	×	×	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	×	×	L	×	×	×	×	×	×	Q_{Ao}	Q_{Bo}	Q_{Co}	Q_{Do}
H	H	H	↑	×	×	a	b	c	d	a	b	c	d
H	L	H	↑	×	H	×	×	×	×	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	×	L	×	×	×	×	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	×	×	×	×	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	×	×	×	×	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	×	×	×	×	×	×	×	L	L	L	L

Note:
1. ↑: Data input is transferred to output on the positive-going edge from LOW to HIGH of the clock
2. X: Either HIGH or LOW; it doesn't matter
3. Hi-Z: High impedance

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	°C
Power dissipation	MN74HC40104	Ta=−40～+60°C	P_D	400	mW
		Ta=+60～85°C		Decrease to 200m Watt the rate of 8mW/°C	
	MN74HC40104S	Ta+−40～+60°C	P_D	275	mW
		Ta=+60～+85°C		Decrease to 200m Watt the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operation supply voltage	V_{CC}		1.4～6.0	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		−40～+85	°C
Input rise and fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	
		6.0	0～400	

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	Test Conditions I_O	I_O Unit	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Input HIGH voltage	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input LOW voltage	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output HIGH voltage	V_{OH}	2.0		−20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	−20.0	μA	4.4	4.5		4.4		
		6.0	or	−20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	−4.0	mA	3.86			3.76		
		6.0		−5.2	mA	5.36			5.26		
Output LOW voltage	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	4.0	mA			0.32		0.37	
		6.0		5.2	mA			0.32		0.37	
Input current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{oz}	6.0	$V_I=V_{IH}$ or V_{IL} $V_o=V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	6.0	$VI=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

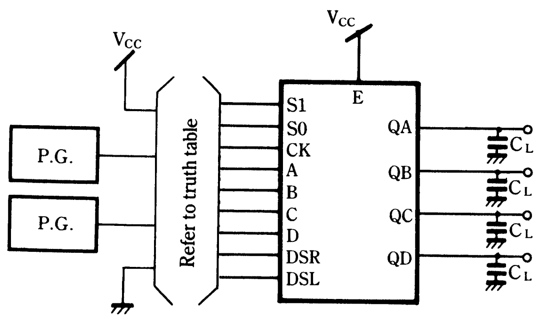
■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Output rise time	t_{TLH}	2.0				75		95	ns
		4.5			8	15		19	
		6.0				13		16	
Output fall time	t_{THL}	2.0				75		95	ns
		4.5			6	15		19	
		6.0				13		16	
Propagation time CLK→Q4 (L→H)	t_{PLH}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
Propagation time CLK→Q4 (H→L)	t_{PHL}	2.0				150		190	ns
		4.5				30		38	
		6.0				26		33	
3-stage propagation time (H→Z)	t_{HZ}	2.0	RL=1KΩ			175		220	ns
		4.5				35		44	
		6.0				30		37	
3-stage propagation time (L→Z)	t_{LZ}	2.0	RL=1KΩ			175		220	ns
		4.5				35		44	
		6.0				30		37	
3-stage propagation time (Z→H)	t_{ZH}	2.0	RL=1KΩ			150		190	ns
		4.5				30		38	
		6.0				26		33	

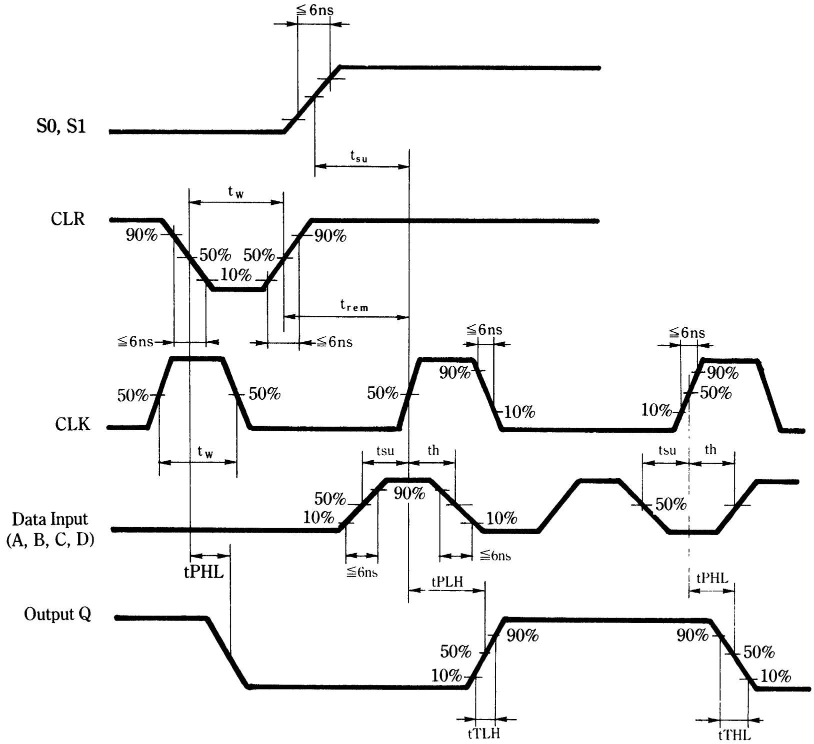
■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25°C			Ta=−40~+85°C		
				min.	typ.	max.	min.	max.	
3-stage propagation time (Z→L)	t_{ZL}	2.0	RL=1KΩ			150		190	ns
		4.5				30		38	
		6.0				26		33	
Minimum pulse width CLK	t_W	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum Set-up time	t_{su}	2.0				100		125	ns
		4.5				20		25	
		6.0				17		21	
Minimum Hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	t_{rem}	2.0				125		155	ns
		4.5				25		31	
		6.0				21		26	
Maximum clock frequency	f_{max}	2.0		6			4		MHz
		4.5		30			24		
		6.0		35			28		

1. Measuring Circuit (t_{PLH}, t_{PHL})

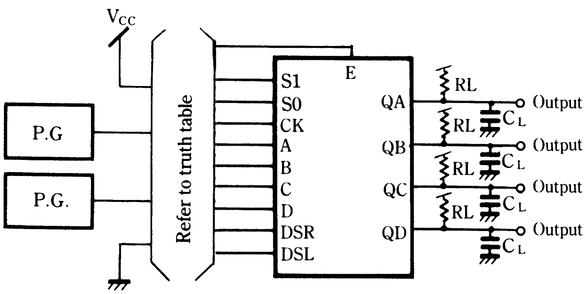


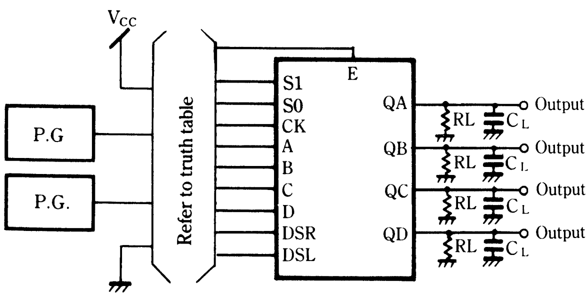
2. Waveforms



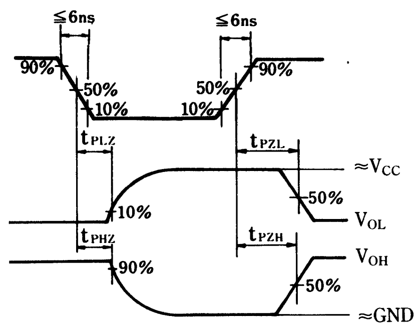
• Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit





2. Waveforms



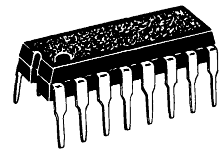
MN74HCT40104/MN74HCT40104S

4-Bit TRI-STATE Bidirectional Universal Shift Register (TTL Input)

■ Description

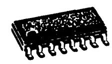
MN74HCT40104/MN74HCT40104S are TTL input level 4-bit 3-state bidirectional shift registers with parallel inputs, parallel outputs, right-shift and left-shift serial inputs, and operational mode-control inputs.
Large current output makes possible for driving a large capacity bus line.
For synchronized-parallel loads, 4-bit data are added to the parallel input, when both mode control inputs (S0 and S1) are HIGH.
Data are loaded to the respective flip-flops, and are transferred to the output at the positive going edge of the clock pulse.
The serial-shift function can be stopped between parallel loads.
The right shift functions (when mode-control input S0 is HIGH and S1 is LOW) when there is synchronization to the rise of the clock pulse.
Whe S0 is LOW and S1 is HIGH, the left shift functions as result of insertion of new data to the left-shift serial input.
When S0 is LOW and S1 is LOW, all outputs become LOW regardless of the clock pulse.
When the enable input is LOW, all outputs become high impedance.
Adoption of a silicon gate CMOS process has made possible low power dissipation, high noise margin equivalent to a standard CMOS, and an operation speed of LS TTL. LS TTL 15-inputs can be directly driven. Resistors and diodes are provided in V_{CC} and GND to protect the input/output from damage by static electricity.
Same pin configuration and function as the standard CMOS logic 4000 family.

P-3



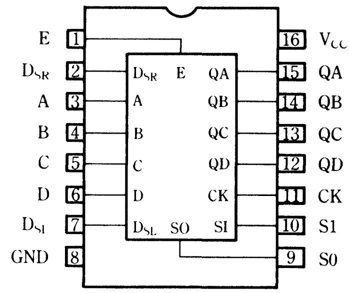
16-pin plastic DIL package

P-4



16-pin Panaflat package (SO-16D)

Pin Configuration (top view)

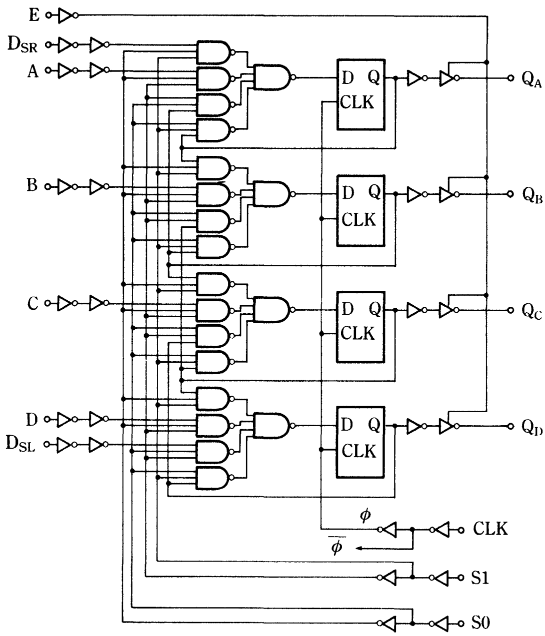


■ Truth Table

Input										Output			
Enable E	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0		D_{SL}	D_{SR}	A	B	C	D				
L	×	×	×	×	×	×	×	×	×	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	×	×	L	×	×	×	×	×	×	Q_{Ao}	Q_{Bo}	Q_{Co}	Q_{Do}
H	H	H	↑	×	×	a	b	c	d	a	b	c	d
H	L	H	↑	×	H	×	×	×	×	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	×	L	×	×	×	×	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	×	×	×	×	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	×	×	×	×	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	×	×	×	×	×	×	×	L	L	L	L

Note:
1. ↑: Data input is transferred to output on the positive-going edge from LOW to HIGH of the clock
2. X: Either HIGH or LOW; it doesn't matter.
3. Hi-Z: High impedance

■ Logic Diagram



■ Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5\sim+7.0$	V
Input/output voltage			V_I, V_O	$-0.5\sim V_{CC}+0.5$	V
Input protection diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±35	mA
Supply current			I_{CC}, I_{GND}	±70	mA
Storage temperature range			Tstg	$-65\sim+150$	°C
Power dissipation	MN74HCT40104	Ta=−40∼+60°C	P_D	400	mW
		Ta=+60∼85°C		Decrease to 200m Watt the rate of 8mW/°C	
	MN74HCT40104S	Ta+−40∼+60°C	P_D	275	mW
		Ta=+60∼+85°C		Decrease to 200m Watt the rate of 3.8mW/°C	

■ Operating Conditions

Parameter	Symbol	V_{CC}(V)	Rating	Unit
Operation supply voltage	V_{CC}		$4.5\sim5.5$	V
Input/output voltage	V_I, V_O		$0\sim V_{CC}$	V
Operating temperature range	T_A		$-40\sim+85$	°C
Input rise and fall time	t_r, t_f	4.5	$0\sim500$	ns

■ DC Characteristics (GND=0V)

Parameter	Symbol	V_{CC} (V)	Test Conditions V_I	I_O	Unit	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Input HIGH voltage	V_{IH}	4.5 ~ 5.5				2.0			2.0		V
Input LOW voltage	V_{IL}	4.5 ~ 5.5						0.8		0.8	V
Output HIGH voltage	V_{OH}	4.5	V_{IH} or V_{IL}	−20.0	μA	4.4	4.5		4.4		V
		4.5		−4.0	mA	3.86			3.76		
Output HIGH voltage	V_{OL}	4.5	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		4.0	mA			0.32		0.37	
Input current	I_I	5.5	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
3-state output off state current	I_{oz}	5.5	$V_I=V_{IH}$ or V_{IL}, $V_o=V_{CC}$ or GND					±0.5		±5.0	μA
Quiescent supply current	I_{CC}	5.5	VI=V_{CC} or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

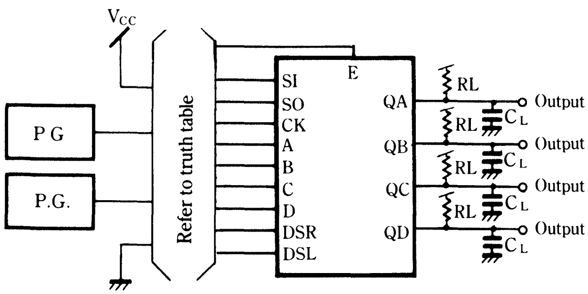
Parameter	Symbol	V_{CC} (V)	Test Conditions	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Output rise time	t_{TLH}	4.5			8	15		19	ns
Output fall time	t_{THL}	4.5			6	15		19	ns
Propagation time CLK→Q (L→H)	t_{PLH}	4.5				30		38	ns
Propagation time CLK→Q (H→L)	t_{PHL}	4.5				30		38	ns
3-stage propagation time (H→Z)	t_{HZ}	4.5	RL=1KΩ			35		44	ns
3-stage propagation time (L→Z)	t_{LZ}	4.5	RL=1KΩ			35		44	ns
3-stage propagation time (Z→H)	t_{ZH}	4.5	RL=1KΩ			30		38	ns
3-stage propagation time (Z→L)	t_{ZL}	4.5	RL=1KΩ			30		38	ns

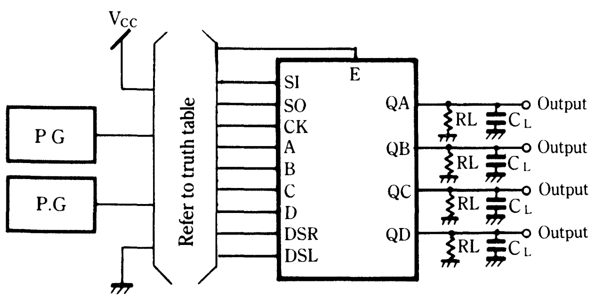
■ AC Characteristics (GND=0V, Input transistion tiem ≦6ns, C_L=50pF)

Parameter	Symbol	V_{CC} (V)	Test Conditions	Temperature					Unit
				Ta=25°C			Ta=−40~+85°C		
				min.	typ.	max.	min.	max.	
Minimum pulse width CLK	t_W	4.5				20		25	ns
Minimum Set-up time	t_{su}	4.5				20		25	ns
Minimum Hold time	t_h	4.5			—	0		0	ns
Minimum recovery time	t_{rem}	4.5				25		31	ns
Maximum clock frequency	f_{max}	4.5		30			24		MHz

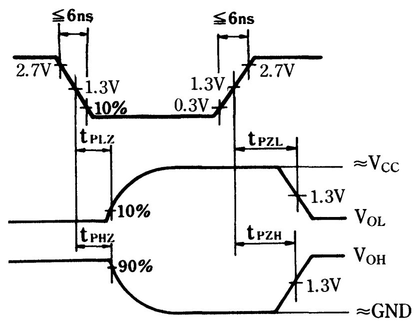
● Switching Time Measuring Circuit and Waveforms

1. Measuring Circuit

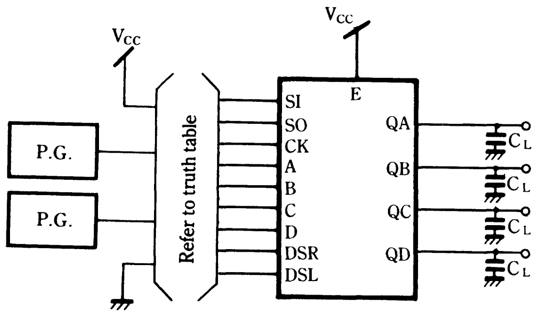




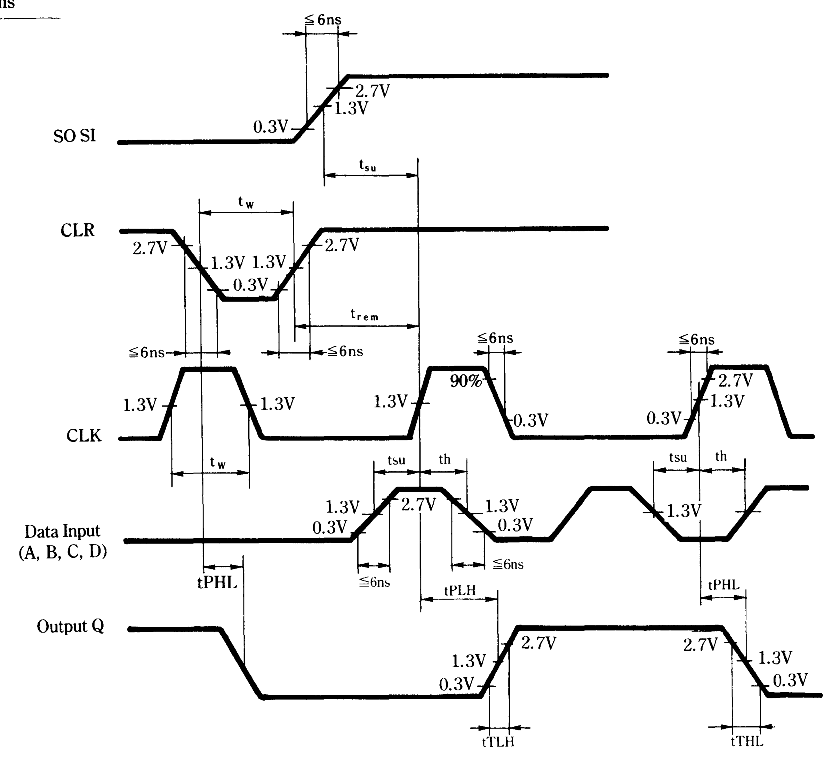
2. Waveforms



1. Measuring Circuit (t_{PLH}, t_{PHL})



2. Waveforms



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