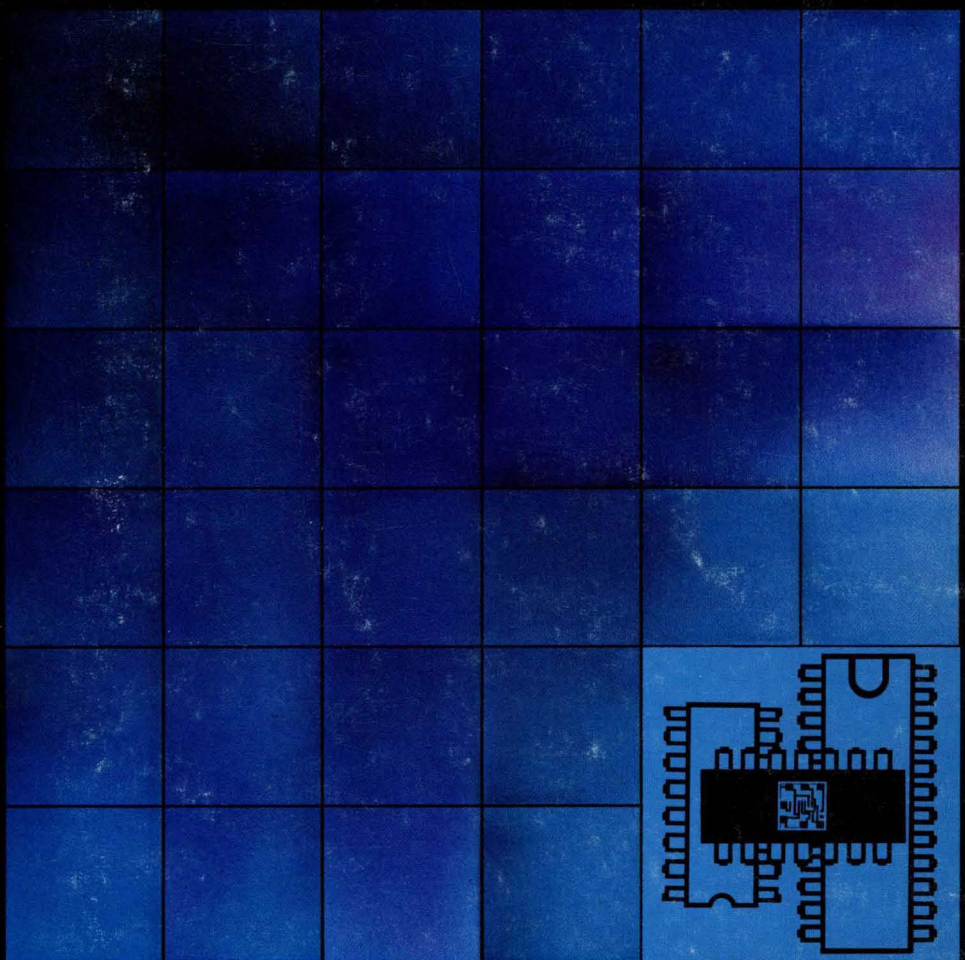
PHILIPS

Electronic components and materials

PHILIPS

INTEGRATED CIRCUITS 1978



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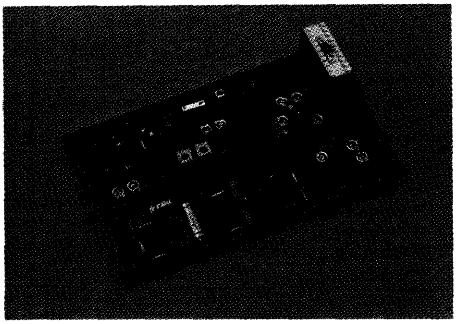

High-frequency section of hi-fi f.m. receiver

		hi-fi equipment	portables radios and radio/recorders	car radios	mains radios
a.m. channel receivers		**TDA5700** **TBA570A**	**TBA570A** **TBA700**	**TBA570A**	**TBA570A**
f.m. channel receivers		**TCA420A**	**TBA570A**	**TBA570A** **TCA420A**	**TBA570A**
a.m./f.m. receiver circuits			**TBA570A** **TBA700**	**TBA570A**	**TBA570A**
stereo decoders		**TDA1005** **TCA290A**		**TDA1005**	
stabilizer for electronic tuning		**TCA530** **TCA750**			
d.c. controlled audio circuits	volume and balance	**TCA730**			**TCA730**
	tone	**TCA740**			**TCA740**
	quadruple signal-sources switch	**TDA1028**			
	stereo signal-sources switch	**TDA1029**			

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a.f. power amplifiers	2 W audio amplifier	**TCA760B**
	5 W audio power amplifier for audio and tv sound	**TDA2611A**
	6 W audio power amplifier for audio and tv sound	**TDA2610; TDA2610A**
	6 W audio power amplifier for car radios and general audio	**TDA1004A**
	6 W audio power amplifier for car radios and general audio	**TDA1010**
	stereo audio power amplifier up to 2 x 10 W	**TDA1009**
miscellaneous	hearing aid amplifier	**OM200/S2**
	low level amplifier	**TAA263**
	integrated MOST amplifier	**TAA320**
	integrated MOST level sensor	**TAA320A**
	recording preamplifier circuit	**TDA1002A**
	motor regulator and bias/erase oscillator circuit	**TDA1003A**
	motor regulator with automatic tape-end indicator for car cassettes	**TDA1006**
	motor-speed regulator	**TDA1059B**
	bipolar frequency divider	**SAJ110**
	magnetic field detector using Hall effect	**TCA450A**
	gating-frequency divider for electronic organs	**TDA1008**
Signetics circuits	Dolby "B" processor	**NE545**
	Dolby "B" processor	**NE645**
	a.m. radio	**NE546**
	f.m. detector/limiter	**ULN2111**
	f.m. gain block	**ULN2208**
	f.m. gain block	**ULN2209**
	f.m. channel receiver	**CA3089**
	f.m. channel receiver	**TBA120SR**
	stereo decoder	**μA758**
	dual low noise preamplifier	**LM381; LM381A**
	dual low noise preamplifier	**LM382**
	dual low noise preamplifier	**LM387**
	dual low noise preamplifier	**NE542**
	power driver	**NE541**
	a.m. channel receiver	**TCA440**

consumer
television

For detailed information
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vision i.f. demodulators	**TCA270S**	signal processing circuit
	TCA540	synchronous demodulator
	TDA2540	i.f. amplifier (n-p-n tuner) and signal processor
	TDA2541	as TDA2540, but for p-n-p tuner
	TDA2670	i.f. amplifier/demodulator
signal processors	**TBA550, TBA890, TBA900, TDA2680A, TDA2690A**	video preamplifier, automatic horizontal sync and vertical sync separator, etc.
sound circuits	**TBA750A**	limiter-amplifier/demodulator
	TDA2610(A)	output circuit
	TDA2790	limiter-amplifier/demodulator
sync processors; horizontal, vertical	**TBA920**	horizontal combination
	TBA720A	horizontal oscillator circuit
	TDA2571	horizontal oscillator with vertical divider
	TDA2581	horizontal deflection stabilizer
	TDA2590 to 92	horizontal combination
vertical deflection circuit	**TDA2600**	switched mode
colour decoding	**TBA560C, TDA2560**	luminance and chrominance control combination
	TCA660B	contrast, saturation and brightness control for colour difference and luminance signals
	TBA510, TDA2510	chrominance combination
	TCA640	chrominance amplifier for SECAM or PAL/SECAM decoders
	TCA650	chrominance demodulator for SECAM or PAL/SECAM decoders
	TBA540	reference combination
	TAA630S	synchronous demodulator for colour difference drive
	TBA520, TBA990, TCA800	colour demodulator
	TDA2520, TDA2522/23	colour demodulator combination
	TBA530, TDA2530	RGB matrix preamplifier
miscellaneous	**TDA2640**	switched-mode power supply drive circuit
	TAA550	voltage stabilizer (electronic tuning)

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SE5534	High performance op amp	B41
SE5535	Dual high slew rate op amp	B38
SE5538	Dual high slew rate op amp	B39
SE5551 to 55	Dual polarity regulators	B57
SE5596	Double balanced mixer/modulator	B94
SU536	FET input op amp	B37
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TAA970	Microphone amp	B96
TBA673	Ring modulator	B97
TBA915	Low-power audio amp	B97
TCA210	Low-power audio amp	B97
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TCA520	General purpose op amp	B39
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7523	Dual core sense amp	B85
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75232	Dual core sense amp	B86
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professional analogue replacement

type to be replaced	replacement	type to be replaced	replacement	type to be replaced	replacement
AD101AD	LM101AF	AMLM207H	LM207T	CA555F	SE555F
AD101AH	LM101AT	AMLM208AH	LM208AT	CA555T	SE555T
AD108AH	LM108AT	AMLM208D	LM208F	CA723CE	μA723CN
AD108H	LM108T	AMLM211D	LM211F	CA723CT	μA723CT
AD201AH	LM201AT	AMLM211H	LM211T	CA723E	μA723N
AD201AN	LM201AN	AMLM301AD	LM301AF	CA723T	μA723T
AD208AH	LM208AT	AMLM301AH	LM301AT	CA741CE	μA741CN
AD208H	LM208T	AMLM307D	LM307F	CA741CF	μA741CF
AD301AH	LM301AT	AMLM307H	LM307T	CA741CT	μA741CT
AD301AN	LM301AN	AMLM308AH	LM308AT	CA741F	μA741F
AD308H	LM308T	AMLM308H	LM308T	CA741T	μA741T
AD741H	μA741T	AMLM311D	LM311F	CA747CF	μA747CF
AD741N	μA741N	AMLM311H	LM311T	CA747CT	μA747CT
AD741CH	μA741CT	CA101AF	LM101AF	CA747F	μA747F
AD741CN	μA741CN	CA101AT	LM101AT	CA747T	μA747T
AD559JD	MC1408-8F	CA101F	LM101F	CA748CE	μA748CN
AD559K	MC1408-8F	CA101T	LM101T	CA748CF	μA748CF
AD559KD	MC1408-8F	CA107F	LM107F	CA748CT	μA748CT
AD559S	MC1508-8F	CA107T	LM107T	CA748F	μA748F
AD559SD	MC1508-8F	CA108AT	LM108AT	CA748T	μA748T
AM555DC	NE555F	CA108T	LM108T	CA1458E	MC1458N
AM555DM	SE555F	CA111F	LM111F	CA1458F	MC1458F
AM555HC	NE555T	CA111T	LM111T	CA1458T	MC1458T
AM555HM	SE555T	CA124F	LM124F	CA1558T	MC1558T
AM555TC	NE555N	CA139AF	LM139AF	CA3045F	CA3045F
AM723DC	μA723CF	CA139F	LM139F	CA3046E	CA3046N
AM723DM	μA723F	CA201AF	LM201AF	CA3081E	CA3081N
AM723HC	μA723CT	CA201AT	LM201AT	CA3082E	CA3082N
AM723HM	μA723T	CA201F	LM201F	CA3083E	CA3083N
AM741DC	μA741CF	CA201T	LM201T	CA3086E	CA3086N
AM741DM	μA741F	CA207F	LM207F	CA3183E	CA3183N
AM741HC	μA741CT	CA207T	LM207T	DM7820AJ	DS7820AF
AM741HM	μA741T	CA208T	LM208T	DM7820J	DS7820F
AM747DC	μA747CF	CA211F	LM211F	DM7830J	DS7830F
AM747DM	μA747F	CA211T	LM211T	DM7880J	DS7880F
AM747HC	μA747CT	CA224F	LM224F	DM8820AJ	DS8820AF
AM747HM	μA747T	CA239AF	LM239AF	DM8820AN	DS8820AN
AM748DC	μA748CF	CA239F	LM239F	DM8820J	DS8820F
AM748DM	μA748F	CA301AF	LM301AF	DM8820N	DS8820N
AM748HC	μA748CT	CA301AT	LM301AT	DM8830J	DS8830F
AM748HM	μA748T	CA307F	LM307F	DM8830N	DS8830N
AMLM101AD	LM101AF	CA307T	LM307T	DM8880J	DS8880F
AMLM101AH	LM101AT	CA308AT	LM308AT	DM8880N	DS8880N
AMLM101H	LM101T	CA308T	LM308T	DS1488J	MC1488F
AMLM107D	LM107F	CA311F	LM311F	DS1489AJ	MC1489AF
AMLM107H	LM107T	CA311T	LM311T	DS1489J	MC1489F
AMLM108AH	LM108AH	CA324E	LM324N	DS3611H	DS3611T
AMLM108H	LM108T	CA324F	LM324F	DS3611N	DS3611N
AMLM111D	LM111F	CA339E	LM339N	DS3612H	DS3612T
AMLM111H	LM111T	CA339F	LM339F	DS3612N	DS3612N
AMLM201AD	LM201AF	CA339AE	LM339AN	DS3613H	DS3613T
AMLM201AH	LM201AT	CA339AF	LM339AF	DS3613N	DS3613N
AMLM201D	LM201F	CA555CE	NE555N	DS3614H	DS3614T
AMLM201H	LM201T	CA555CF	NE555F	DS3614N	DS3614N
AMLM207D	LM207F	CA555CT	NE555T	DS7520J	7520F

type to be replaced	replacement	type to be replaced	replacement	type to be replaced	replacement
DS7520N	7520N	LF155AL	LF155AT	LH2308AD	LH2308AF
DS7521J	7521F	LF155H	LF155T	LH2308D	LH2308F
DS7521N	7521N	LF155J-8	LF155FE	LH2311D	LH2311F
DS7522J	7522F	LF155L	LF155T	LM78L05ACH	78L05ACDB
DS7522N	7522N	LF156AH	LF156AT	LM78L05ACZ	78L05ACS
DS7523J	7523F	LF156AJ-8	LF156AFE	LM78L05CH	78L05CDB
DS7523N	7523N	LF156AL	LF156AT	LM78L05CZ	78L05CS
DS7524J	7524F	LF156H	LF156AT	LM78L06ACH	78L06ACDB
DS7524N	7524N	LF156J-8	LF156FE	LM78L06ACZ	78L06ACS
DS7525J	7525F	LF156L	LF156T	LM78L06CH	78L06CDB
DS7525N	7525N	LF157AH	LF157AT	LM78L06CZ	78L06CS
DS7528J	7528F	LF157AJ-8	LF157AFE	LM78L08ACH	78L08ACDB
DS7528N	7528N	LF157AL	LF157AT	LM78L08ACZ	78L08ACS
DS7820AJ	DS7820AF	LF157H	LF157T	LM78L08CH	78L08CDB
DS7820J	DS7820F	LF157J-8	LF157FE	LM78L08CZ	78L08CS
DS7830J	DS7830F	LF157L	LF157T	LM78L12ACH	78L12ACDB
DS7880J	DS7880F	LF255AL	LF255AT	LM78L12ACZ	78L12ACS
DS8820J	DS8820F	LF255L	LF255T	LM78L12CH	78L12CDB
DS8820AJ	DS8820AF	LF256AL	LF256AT	LM78L12CZ	78L12CS
DS8820AN	DS8820AN	LF256L	LF256T	LM78L15ACH	78L15ACDB
DS8820N	DS8820N	LF257AL	LF257AT	LM78L15ACZ	78L15ACS
DS8830J	DS8830F	LF257L	LF257T	LM78L15CH	78L15CDB
DS8830N	DS8830N	LF355AH	LF355AT	LM78L15CZ	78L15CS
DS8880J	DS8880F	LF355AJ-8	LF355AFE	LM78L24ACH	78L24ACDB
DS8880N	DS8880N	LF355AL	LF355AT	LM78L24ACZ	78L24ACS
DS55450J	55450BF	LF355AN	LF355AN	LM78L24CH	78L24CDB
DS55450T	55450BT	LF355H	LF355T	LM78L24CZ	78L24CS
DS55451H	55451BT	LF355J-8	LF355FE	LM101AD	LM101AF
DS55452H	55452BT	LF355L	LF355T	LM101AH	LM101AT
DS55453H	55453BT	LF355N	LF355N	LM101AJ	LM101AF
DS55454H	55454BT	LF356AH	LF356AT	LM101AJ-14	LM101AF
DS75107J	75S107F	LF356AJ-8	LF356AFE	LM101AJG	LM101AFE
DS75107N	75S107N	LF356AL	LF356AT	LM101AL	LM101AT
DS75108J	75S108F	LF356AN	LF356AN	LM101H	LM101T
DS75108N	75S108N	LF356H	LF356T	LM101J-14	LM101F
DS75207J	75S207F	LF356J-8	LF356FE	LM107D	LM107F
DS75207N	75S207N	LF356L	LF356T	LM107H	LM107T
DS75208J	75S208F	LF356N	LF356N	LM107J	LM107F or FE
DS75208N	75S208N	LF357AH	LF357AT	LM107J-14	LM107F
DS75324J	75324F	LF357AJ-8	LF357AFE	LM107JG	LM107FE
DS75324N	75324N	LF357AL	LF357AT	LM107L	LM107T
DS75325J	75325F	LF357AN	LF357AN	LM108AD	LM108AF
DS75325N	75325N	LF357H	LF357T	LM108AH	LM108AT
DS75450J	75450BF	LF357J-8	LF357FE	LM108AJ	LM108AF
DS75450N	75450BN	LF357L	LF357T	LM108D	LM108F
DS75451H	75451BT	LF357N	LF357N	LM108H	LM108T
DS75451N	75451BN	LH2101AD	LH2101AF	LM108J	LM108F
DS75452H	75452BT	LH2108AD	LH2108AF	LM109H	LM109DB
DS75452N	75452BN	LH2108D	LH2108F	LM109K	LM109DA
DS75453H	75453BT	LH2111D	LH2111F	LM109LA	LM109DB
DS75453N	75453BN	LH2201AD	LH2201AF	LM111D	LM111F
DS75454H	75454BT	LH2208AD	LH2208AF	LM111H	LM111T
DS75454N	75454BN	LH2208D	LH2208F	LM111J	LM111F
LF155AH	LF155AT	LH2211D	LH2211F	LM111JG	LM111FE
LF155AJ-8	LF155AFE	LH2301AD	LH2301AF	LM111L	LM111T

professional analogue replacement

type to be replaced	replacement
LM119D	LM119F
LM119H	LM119T
LM119J	LM119F
LM124AD	LM124AF
LM124AJ	LM124AF
LM124D	LM124F
LM124J	LM124F
LM139AD	LM139AF
LM139AJ	LM139AF
LM139D	LM139F
LM139J	LM139F
LM158AH	LM158AT
LM158H	LM158T
LM158JG	LM158FE
LM158L	LM158T
LM161D	SE529F
LM161H	SE529K
LM161J	SE529F
LM193AH	LM193AT
LM193H	LM193T
LM193JG	LM193FE
LM193L	LM193T
LM201AD	LM201AF
LM201AH	LM201AT
LM201AJ	LM201AF
LM201AJ-14	LM201AF
LM201AJG	LM201AFE
LM201AL	LM201AT
LM201AN	LM201AN-14
LM201AP	LM201AN
LM201H	LM201T
LM201J	LM201FE
LM201J-14	LM201F
LM207D	LM207F
LM207H	LM207T
LM207J	LM207F or FE
LM207J-14	LM207F
LM207JG	LM207FE
LM207L	LM207T
LM207N	LM207N-14
LM207P	LM207N
LM208AD	LM208AF
LM208AH	LM208AT
LM208AJ	LM208AF
LM208D	LM208F
LM208H	LM208T
LM208J	LM208F
LM209H	LM209DB
LM209K	LM209DA
LM209LA	LM209DB
lLM211D	LM211F
LM211H	LM211T
LM211J	LM211F
LM219D	LM219F
LM219H	LM219T
LM219J	LM219F
LM224AD	LM224AF
LM224AJ	LM224AF
LM224D	LM224F
LM224J	LM224F
LM224N	LM224N
LM239AD	LM239AF
LM239AJ	LM239AF
LM239D	LM239F
LM239J	LM239F
LM239N	LM239N
LM258AH	LM258AT
LM258H	LM258T
LM258JG	LM258FE
LM258L	LM258T
LM258P	LM258N
LM293AH	LM293AT
LM293H	LM293T
LM293JG	LM293FE
LM293L	LM293T
LM293P	LM293N
LM301AH	LM301AT
LM301AJ	LM301AF or AFE
LM301AJ-14	LM301AF
LM301AJG	LM301AFE
LM301AL	LM301AT
LM301AN	LM301AN or AN-14
LM301AP	LM301AN
LM307D	LM307F
LM307H	LM307T
LM307J	LM307F or FE
LM307J-14	LM307F
LM307JG	LM307FE
LM307L	LM307T
LM307N	LM307N or N-14
LM307P	LM307N
LM308AD	LM308AF
LM308AH	LM308AT
LM308AJ	LM308AF
LM308D	LM308F
LM308H	LM308T
LM308J	LM308F
LM308N	LM308N
LM309H	LM309DB
LM309K	LM309DA
LM309LA	LM309DB
LM311D	LM311F
LM311H	LM311T
LM311J	LM311F or FE
LM311J-14	LM311F
LM311JG	LM311FE
LM311L	LM311T
LM311N	LM311N or N-14
LM311N-14	LM311N-14
LM311P	LM311N
LM319D	LM319F
LM319H	LM319T
LM319J	LM319F
LM319N	LM319N
LM324AJ	LM324AF
LM324AN	LM324AN
LM324J	LM324F
LM324N	LM324N
LM339AJ	LM339AF
LM339AN	LM339AN
LM339J	LM339F
LM339N	LM339N
LM340K-5.0	LM340-5DA
LM340K-6.0	LM340-6DA
LM340K-8.0	LM340-8DA
LM340K-12	LM340-12DA
LM340K-15	LM340-15DA
LM340K-18	LM340-18DA
LM340K-24	LM340-24DA
LM340T-5.0	LM340-5U
LM340T-6.0	LM340-6U
LM340T-8.0	LM340-8U
LM340T-12	LM340-12U
LM340T-15	LM340-15U
LM340T-18	LM340-18U
LM340T-24	LM340-24U
LM341P-5.0	78M05CU
LM341P-6.0	78M06CU
LM341P-8.0	78M08CU
LM341P-12	78M12CU
LM341P-15	78M15CU
LM341P-20	78M20CU
LM341P-24	78M24CU
LM358AH	LM358AT
LM358AN	LM358AN
LM358H	LM358T
LM358JG	LM358FE
LM358L	LM358T
LM358N	LM358N
LM358P	LM358N
LM361D	LM361F
LM361H	LM361T
LM361J	LM361F
LM361N	LM361N
LM381N	LM381N
LM382N	LM382N
LM387N	LM387N
LM393AH	LM393AT
LM393AN	LM393AN
LM393H	LM393T
LM393JG	LM393FE
LM393L	LM393T
LM393N	LM393N
LM393P	LM393N
LM555CH	NE555T

type to be replaced	replacement	type to be replaced	replacement	type to be replaced	replacement
LM555CN	NE555N	LM747H	μA747T	LM7918T	7918CU
LM555H	SE555T	LM747J	μA747F	LM7924T	7924CU
LM556CD	NE556F	LM748CH	μA748CT	MC78L02ACG	78L02ACDB
LM556CJ	NE556F	LM748CJ	μA748CF	MC78L02ACP	78L02ACS
LM556CN	NE556N	LM748CN	μA748CN	MC78L05ACG	78L05ACDB
LM556D	SE556F	LM748H	μA748T	MC78L05ACP	78L05ACS
LM556J	SE556F	LM748J	μA748F	MC78L05CG	78L05CDB
LM565CH	NE565T	LM1458H	MC1458T	MC78L05CP	78L05CS
LM565CN	NE565N	LM1458J	MC1458FE	MC78L08ACG	78L08ACDB
LM565H	SE565T	LM1458N	MC1458N	MC78L08ACP	78L08ACS
LM566CH	NE566T	LM1458N-14	MC1458N-14	MC78L08CG	78L08CDB
LM566CN	NE566N	LM1496H	MC1496T	MC78L08CP	78L08CS
LM566H	SE566T	LM1496J	MC1496F	MC78L12ACG	78L12ACDB
LM567CH	NE567T	LM1496N	MC1496N	MC78L12ACP	78L12ACS
LM567CN	NE567N	LM1558H	MC1558T	MC78L12CG	78L12CDB
LM567H	SE567T	LM1558J	MC1558FE	MC78L12CP	78L12CS
LM709AJ	μA709AF	LM1596H	MC1596T	MC78L15ACG	78L15ACDB
LM709CH	μA709CT	LM1596J	MC1596F	MC78L15ACP	78L15ACS
LM709CJ	μA709CF	LM2901J	LM2901F	MC78L15CG	78L15CDB
LM709CN	μA709CN	LM2901N	LM2901N	MC78L15CP	78L15CS
LM709CN-14	μA709CN-14	LM2902J	LM2902F	MC78L18ACG	78L18ACDB
LM709H	μA709T	LM2902N	LM2902N	MC78L18ACP	78L18ACS
LM709J	μA709F	LM2903JG	LM2903FE	MC78L18CG	78L18CDB
LM710H	μA710T	LM2903L	LM2903T	MC78L18CP	78L18CS
LM710CH	μA710CT	LM2903N	LM2903N	MC78L24ACG	78L24ACDB
LM711CH	μA711CT	LM2903P	LM2903N	MC78L24ACP	78L24ACS
LM711CN	μA711CN	LM2904JG	LM2904FE	MC78L24CG	78L24CDB
LM711H	μA711T	LM2904L	LM2904T	MC78L24CP	78L24CS
LM723CD	μA723CF	LM2904N	LM2904N	MC78M05CG	78M05CDB
LM723CH	μA723CT	LM2904P	LM2904N	MC78M05CT	78M05CU
LM723CJ	μA723CF	LM3045D	CA3045F	MC78M06CG	78M06CDB
LM723CN	μA723CN	LM3045J	CA3045F	MC78M06CT	78M06CU
LM723D	μA732F	LM3046N	CA3046N	MC78M08CG	78M08CDB
LM723H	μA723T	LM3086N	CA3086N	MC78M08CT	78M08CU
LM723J	μA723F	LM3302N	MC3302N	MC78M12CG	78M12CDB
LM723N	μA723N	LM7805KC	7805CDA	MC78M12CT	78M12CU
LM733CD	μA733CF	LM7805T	7805CU	MC78M15CG	78M15CDB
LM733CH	μA733CT	LM7806KC	7806CDA	MC78M15CT	78M15CU
LM733CJ	μA733CF	LM7806T	7806CU	MC78M18CG	78M18CDB
LM733CN	μA733CN	LM7808KC	7808CDA	MC78M18CT	78M18CU
LM733D	μA733F	LM7808T	7808CU	MC78M20CG	78M20CDB
LM733H	μA733T	LM7812KC	7812CDA	MC78M20CT	78M20CU
LM733T	μA733F	LM7812T	7812CU	MC78M24CG	78M24CDB
LM741CH	μA741CT	LM7815KC	7815CDA	MC78M24CT	78M24CU
LM741CJ	μA741CFE	LM7815T	7815CU	MC1408L6	MC1408-6F
LM741CJ-14	μA741CF	LM7818KC	7818CDA	MC1408L7	MC1408-7F
LM741CN	μA741CN	LM7818T	7818CU	MC1408L8	MC1408-8F
LM741CN-14	μA741CN-14	LM7824KC	7824CDA	MC1408P6	MC1408-6N
LM741D	μA741F	LM7824T	7824CU	MC1408P7	MC1408-7N
LM741H	μA741T	LM7905T	7905CU	MC1408P8	MC1408-8N
LM741J-14	μA741F	LM7905.2T	7905.2CU	MC1411P	ULN2001N
LM747CD	μA747CF	LM7906T	7906CU	MC1412P	ULN2002N
LM747CH	μA747CT	LM7908T	7908CU	MC1413P	ULN2003N
LM747CJ	μA747CF	LM7912T	7912CU	MC1416P	ULN2004N
LM747D	μA747F	LM7915T	7915CU	MC1455G	NE555T

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type to be replaced	replacement	type to be replaced	replacement	type to be replaced	replacement
MC1455P1	NE555N	MC1709CL	μA709CF	MC3456P	NE556N
MC1455U	NE555FE	MC1709CP1	μA709CN	MC3556L	SE556F
MC1456CG	MC1456T	MC1709CP2	μA709CN14	MC7524L	7524F
MC1456CL	MC1456F	MC1709CU	μA709CFE	MC7524P	7524N
MC1456CP1	MC1456N	MC1709G	μA709T	MC7525L	7525F
MC1456CU	MC1456FE	MC1709L	μA709F	MC7525P	7525N
MC1456G	MC1456T	MC1709U	μA709FE	MC7528L	7528F
MC1456L	MC1456F	MC1710CG	μA710CT	MC7528P	7528N
MC1456P1	MC1456N	MC1710CL	μA710CF	MC7529L	7529F
MC1456U	MC1456FE	MC1710CP	μA710CN	MC7529P	7529N
MC1458CG	MC1458T	MC1710G	μA710T	MC7805CK	7805CDA
MC1458CL	MC1458F	MC1710L	μA710F	MC7805CT	7805CU
MC1458CP1	MC1458N	MC1711CG	μA711CT	MC7806CK	7806CDA
MC1458CP2	MC1458N-14	MC1711CL	μA711CF	MC7806CT	7806CU
MC1458CU	MC1458FE	MC1711CP	μA711CN	MC7808CK	7808CDA
MC1458G	MC1458T	MC1711G	μA711T	MC7808CT	7808CU
MC1458JG	MC1458FE	MC1711L	μA711F	MC7812CK	7812CDA
MC1458L	MC1458F or T	MC1723CG	μA723CT	MC7812CT	7812CU
MC1458P	MC1458N	MC1723CL	μA723CF	MC7815CK	7815CDA
MC1458P1	MC1458N	MC1723CP	μA723CN	MC7815CT	7815CU
MC1458P2	MC1458N-14	MC1723G	μA723T	MC7818CK	7818CDA
MC1458SG	NE5535T	MC1723L	μA723F	MC7818CT	7818CU
MC1458SL	NE5535F	MC1733CG	μA733CT	MC7824CK	7824CDA
MC1458SP1	NE5535N	MC1733CL	μA733CF	MC7824CT	7824CU
MC1458SP2	NE5535N-14	MC1733CP	μA733CN	MC7902CK	79M02CDA
MC1458SU	NE5535FE	MC1733G	μA733T	MC7902CT	79M02CU
MC1458U	MC1458FE	MC1733L	μA733F	MC7905CK	79M05CDA
MC1471P1	UDN5711N	MC1741CG	μA741CT	MC7905CT	79M05CU
MC1472P1	UDN5712N	MC1741CL	μA741CF	MC7905.2CK	7905.2CDA
MC1473P1	UDN5713N	MC1741CP1	μA741CN	MC7905.2CT	7905.2CU
MC1474P1	UDN5714N	MC1741CP2	μA741CN-14	MC7906CK	7906CDA
MC1488L	MC1488F	MC1741CU	μA741CFE	MC7906CT	7906CU
MC1489AL	MC1489AF	MC1741G	μA741T	MC7908CK	7908CDA
MC1489L	MC1489F	MC1741L	μA741F	MC7908CT	7908CU
MC1496G	MC1496T	MC1741SCG	NE535T	MC7912CK	7912CDA
MC1496L	MC1496F	MC1741SCP1	NE535N	MC7912CT	7912CU
MC1496P	MC1496N	MC1741SCU	NE535FE	MC7915CK	7915CDA
MC1508L8	MC1508-8F	MC1741SG	SE535T	MC7915CT	7915CU
MC1555G	SE555T	MC1741SU	SE535FE	MC7918CK	7918CDA
MC1555U	SE555FE	MC1741U	SE535FE	MC7918CT	7918CU
MC1556G	MC1556T	MC1747CG	μA747CT	MC7924CK	7924CDA
MC1556L	MC1556F	MC1747CL	μA747CF	MC7924CT	7924CU
MC1556U	MC1556FE	MC1747CP2	μA747CN	MC55325L	55325F
MC1558G	MC1558T	MC1747G	μA747T	MC75107L	75S107F
MC1558JG	MC1558FE	MC1747L	μA747F	MC75107P	75S107N
MC1558L	MC1558F or T	MC1748CG	μA748CT	MC75108L	75S108F
MC1558SG	SE5535T	MC1748CP1	μA748CN	MC75108P	75S108N
MC1558SL	SE5535F	MC1748CU	μA748CFE	MC75324L	75324F
MC1558SU	SE5535FE	MC1748G	μA748T	MC75324P	75324N
MC1558U	MC1558FE	MC1748U	μA748FE	MC75450L	75450F
MC1596G	MC1596T	MC3302L	MC3302F	MC75450P	75450N
MC1596L	MC1596F	MC3302P	MC3302N	MC75451P	75451N
MC1709AG	μA709AT	MC3346P	CA3046N	MC75451U	75451FE
MC1709AL	μA709AF	MC3386P	CA3086N	MC75452P	75452N
MC1709CG	μA709CT	MC3456L	NE556F	MC75452U	75452FE

type to be replaced	replacement	type to be replaced	replacement	type to be replaced	replacement
MC75453P	75453N	MLM308P1	LM308N	µA78M08CKC	78M08CU
MC75453U	75453FE	MLM309G	LM309DB	µA78M08CLA	78M08CDB
MC75454P	75454N	MLM309K	LM309DA	µA78M08HC	78M08CDB
MC75454U	75454FE	MLM311G	LM311T	µA78M08HM	78M08DB
MLM101AG	LM101AT	MLM311L	LM311F	µA78M08MLA	78M08DB
MLM101AU	LM101AFE	MLM311P1	LM311N	µA78M08UC	78M08CU
MLM107G	LM107T	MLM311U	LM311FE	µA78M12CKC	78M12CU
MLM107U	LM107FE	MLM324L	LM324F	µA78M12CLA	78M12CDB
MLM108G	LM108T	MLM324P	LM324N	µA78M12HC	78M12CDB
MLM108L	LM108F	MLM339AL	LM339AF	µA78M12HM	78M12DB
MLM108AG	LM108AT	MLM339AP	LM339AN	µA78M12MLA	78M12DB
MLM108AL	LM108AF	MLM339L	LM339F	µA78M12UC	78M12CU
MLM109G	LM109DB	MLM339P	LM339N	µA78M15CKC	78M15CU
MLM109K	LM109DA	MLM358G	LM358T	µA78M15CLA	78M15CDB
MLM111G	LM111T	MLM358P1	LM358N	µA78M15HC	78M15CDB
MLM111L	LM111F	MLM358U	LM358FE	µA78M15HM	78M15DB
MLM111U	LM111FE	MLM565CP	NE565CN	µA78M15MLA	78M15DB
MLM124L	LM124F	MLM2901P	LM2901N	µA78M15UC	78M15CU
MLM139AL	LM139AF	MLM2902P	LM2902N	µA78M20CKC	78M20CU
MLM139L	LM139F	µA78GU1C	78GCU1	µA78M20CLA	78M20CDB
MLM158G	LM158T	µA78L02ACLP	78L02ACS	µA7820HC	78M20CDB
MLM158U	LM158FE	µA78L02CLP	78L02CS	µA78M20HM	78M20DB
MLM201AG	LM201AT	µA78L05ACLP	78L05ACS	µA78M20MLA	78M20DB
MLM201AP1	LM201AN	µA78L05AHC	78L05ACDB	µA78M20UC	78M20CU
MLM201AU	LM201AFE	µA78L05AWC	78L05ACS	µA78M24CKC	78M24CU
MLM207G	LM207T	µA78L05CLP	78L05CS	µA78M24CLA	78M24CDB
MLM207U	LM207FE	µA78L06ACLP	78L06ACS	µA78M24HC	78M24CDB
MLM208AG	LM208AT	µA78L06AHC	78L06ACDB	µA78M24HM	78M24DB
MLM208AL	LM208AF	µA78L06AWC	78L06ACS	µA78M24MLA	78M24DB
MLM208G	LM208T	µA78L06CLP	78L06CS	µA78M24UC	78M24CU
MLM208L	LM208F	µA78L08ACLP	78L08ACS	µA78MGU1C	78MGCU1
MLM209G	LM209DB	µA78L08CLP	78L08CS	µA79GU1C	79GCU1
MLM209K	LM209DA	µA78L12ACLP	78L12ACS	µA79M05	79M05DB
MLM211G	LM211T	µA78L12AHC	78L12ACDB	µA79M05AHC	79M05CDB
MLM211L	LM211F	µA78L12AWC	78L12ACS	µA79M05AUC	79M05CU
MLM211U	LM211FE	µA78L12CLP	78L12CS	µA79M05CKC	79M05CU
MLM224L	LM224F	µA78L15ACLP	78L15ACS	µA79M05CLA	79M05CDB
MLM224P	LM224N	µA78L15AHC	78L15ACDB	µA79M05HM	79M05DB
MLM239AL	LM239AF	µA78L15AWC	78L15ACS	µA79M06AHC	79M06CDB
MLM239AP	LM239AN	µA78L15CLP	78L15CS	µA79M06AUC	79M06CU
MLM239L	LM239F	µA78L26AWC	78L02ACS	µA79M06CKC	79M06CU
MLM239P	LM239N	µA78L82AHC	78L08ACDB	µA79M06CLA	79M06CDB
MLM258G	LM258T	µA78L82AWC	78L08ACS	µA79M06HM	79M06DB
MLM258P1	LM258N	µA78M05CKC	78M05CU	µA79M06LA	79M06DB
MLM258U	LM258FE	µA78M05CLA	78M05CDB	µA79M08AHC	79M08CDB
MLM301AG	LM301AT	µA78M05HC	78M05CDB	µA79M08AUC	79M08CU
MLM301AP1	LM301AN	µA78M05HM	78M05DB	µA79M08CKC	79M08CU
MLM301AU	LM301AFE	µA78M05MLA	78M05DB	µA79M08CLA	79M08CDB
MLM307G	LM307T	µA78M05UC	78M05CU	µA79M08HM	79M08DB
MLM307P1	LM307N	µA78M06CKC	78M06CU	µA79M08LA	79M08DB
MLM307U	LM307FE	µA78M06CLA	78M06CDB	µA79M12AHC	79M12CDB
MLM308AG	LM308AT	µA78M06HC	78M06CDB	µA79M12AUC	79M12CU
MLM308AL	LM308AF	µA78M06HM	78M06DB	µA79M12CKC	79M12CU
MLM308G	LM308T	µA78M06MLA	78M06DB	µA79M12CLA	79M12CDB
MLM308L	LM308F	µA78M06UC	78M06CU	µA79M12HM	79M12DB

professional analogue replacement

type to be replaced	replacement	type to be replaced	replacement	type to be replaced	replacement
µA79M12LA	79M12DB	µA311HC	LM311T	µA711CL	µA711CT
µA79M15AHC	79M15CDB	µA311TC	LM311N	µA711CN	µA711CN
µA79M15AUC	79M15CU	µA324DC	LM324F	µA711DC	µA711CF
µA79M15CKC	79M15CU	µA324PC	LM324N	µA711DM	µA711F
µA79M15CLA	79M15CDB	µA339ADC	LM339AF	µA711MJ	µA711F
µA79M15HM	79M15DB	µA339DC	LM339F	µA711ML	µA711T
µA79M15LA	79M15DB	µA339PC	LM339N	µA711PC	µA711CN
µA79M18AHC	79M18CDB	µA555HC	NE555T	µA723CJ	µA723CF
µA79M18AUC	79M18CU	µA555HM	SE555T	µA723CL	µA723CT
µA79M18HM	79M18DB	µA555TC	NE555N	µA723CN	µA723CN
µA79M20CKC	79M20CU	µA556DC	NE556F	µA723DC	µA723CF
µA79M20CLA	79M20CDB	µA556DM	SE556F	µA723DM	µA723F
µA79M20LA	79M20DB	µA556PC	NE556N	µA723HC	µA723CT
µA79M24AHC	79M24CDB	µA709	µA709T	µA723HM	µA723T
µA79M24AUC	79M24CU	µA709ADM	µA709AF	µA723MJ	µA723F
µA79M24CKC	79M24CU	µA709AHM	µA709AT	µA723ML	µA723T
µA79M24CLA	79M24CDB	µA709AJ	µA709AF	µA723PC	µA723CN
µA79M24HM	79M24DB	µA709AJG	µA709AFE	µA733CJ	µA733CF
µA79M24LA	79M24DB	µA709AL	µA709AT	µA733CL	µA733CT
µA79MGU1C	79MGCU1	µA709C1	µA709CT	µA733CN	µA733CN
µA101ADM	LM101AF	µA709C2	µA709CN	µA733DC	µA733CF
µA101AHM	LM101AT	µA709CJ	µA709CF	µA733DM	µA733F
µA101DM	LM101F	µA709CJG	µA709CFE	µA733HC	µA733CT
µA101HM	LM101T	µA709CL	µA709CT	µA733HM	µA733T
µA107HM	LM107T	µA709CN	µA709CN-14	µA733MJ	µA733F
µA108ADM	LM108AF	µA709CP	µA709CN	µA733ML	µA733T
µA108AHM	LM108AT	µA709DC	µA709CF	µA740HC	µA740CT
µA108DM	LM108F	µA709DM	µA709F	µA741CJ	µA741CF
µA108HM	LM108T	µA709HC	µA709CT	µA741CJG	µA741CFE
µA109KM	LM109DA	µA709HM	µA709T	µA741CL	µA741CT
µA111HM	LM111T	µA709MJ	µA709F	µA741CN	µA741CN-14
µA124DM	LM124F	µA709MJG	µA709FE	µA741CP	µA741CN
µA139ADM	LM124AF	µA709ML	µA709T	µA741DC	µA741CF
µA139DM	LM124F	µA709PC	µA709CN-14	µA741DM	µA741F
µA201AHD	LM201AF	µA709TC	µA709CN	µA741HC	µA741ÇT
µA201AHM	LM201AT	µA710	µA710T	µA741HM	µA741T
µA201DM	LM201F	µA710C1	µA710CT	µA741MJ	µA741F
µA201HM	LM201T	µA710C2	µA710CN	µA741MJG	µA741FE
µA207HM	LM207T	µA710CJ	µA710CF	µA741ML	µA741T
µA208ADM	LM208AF	µA710CJG	µA710CFE	µA741PC	µA741CN-14
µA208AHM	LM208AT	µA710CL	µA710CT	µA741TC	µA741CN
µA208DM	LM208F	µA710CN	µA710CN-14	µA747CJ	µA747CF
µA208HM	LM208T	µA710CP	µA710CN	µA747CL	µA747CT
µA209KM	LM209DA	µA710DC	µA710CF	µA747CN	µA747CN
µA224DM	LM224F	µA710DM	µA710F	µA747DC	µA747CF
µA301ADC	LM301AF	µA710HC	µA710CT	µA747DM	µA747F
µA301AHC	LM301AT	µA710HM	µA710T	µA747HC	µA747CT
µA301ANC	LM301AN	µA710MJ	µA710F	µA747HM	µA747T
µA307HC	LM307T	µA710MJG	µA710FE	µA747MJ	µA747F
µA307TC	LM307N	µA710ML	µA710T	µA747ML	µA747T
µA308ADC	LM308AF	µA710PC	µA710CN-14	µA747PC	µA747CN
µA308AHC	LM308AT	µA711	µA711K	µA748CJ	µA748CF
µA308DC	LM308F	µA711C1	µA711CK	µA748CJG	µA748CFE
µA308HC	LM308T	µA711C2	µA711CN	µA748CL	µA748CT
µA308TC	LM308N	µA711CJ	µA711CF	µA748CN	µA748CN-14

type to be replaced	replacement	type to be replaced	replacement	type to be replaced	replacement
µA748CP	µA748CN	µA7818CKA	7818CDA	µAF155HM	LF155T
µA748DC	µA748CF	µA7818CKC	7818CU	µAF156AHM	LF156AT
µA748DM	µA748F	µA7818KC	7818CDA	µAF156HM	LF156T
µA748HC	µA748CT	µA7818KM	7818DA	µAF157AHM	LF157AT
µA748HM	µA748T	µA7818MKA	7818DA	µAF157HM	LF157T
µA748MJ	µA748F	µA7818UC	7818CU	µAF355AHC	LF355AT
µA748MJG	µA748FE	µA7824CKA	7824CDA	µAF355HC	LF355T
µA748ML	µA748T	µA7824CKC	7824CU	µAF356AHC	LF356AT
µA748TC	µA748CN	µA7824KC	7824CDA	µAF356HC	LF356T
µA796HC	MC1496T	µA7824KM	7824DA	µAF357AHC	LF357AT
µA0802DC-1	MC1408-8F	µA7824MKA	7824DA	µAF357HC	LF357T
µA0802DC-2	MC1408-7F	µA7824UC	7824CU	NE555JG	NE555FE
µA0802DC-3	MC1408-6F	µA7905CKA	7905CDA	NE555L	NE555T
µA0802DM-1	MC1508-8F	µA7905CKC	7905CU	NE555P	NE555N
µA0802PC-1	MC1408-8N	µA7905KA	7905DA	NE592G	NE592T
µA0802PC-2	MC1408-7N	µA7905KC	7905CDA	NE592L	NE592F
µA0802PC-3	MC1408-6N	µA7905KM	7905DA	RC709D	µA709CF
µA1458HC	MC1458T	µA7905UC	7905CU	RC709DN	µA709CN
µA1458TC	MC1458N	µA7906CKA	7906CDA	RC709DP	µA709CN-14
µA1558HM	MC1558T	µA7906CKC	7906CU	RC709T	µA709CT
µA2901PC	LM2901N	µA7906KA	7906DA	RC710DC	µA710CF
µA2902PC	LM2902N	µA7906KC	7905CDA	RC710DP	µA710CN
µA3045DM	CA3045F	µA7906KM	7905DA	RC710T	µA710CT
µA3046TC	CA3046N	µA7906UC	7905CU	RC711DC	µA711CF
µA3086TC	CA3086N	µA7908CKA	7908CDA	RC711DP	µA711CN
µA7805CKA	7805CDA	µA7908CKC	7908CU	RC711T	µA711CT
µA7805CKC	7805CU	µA7908KA	7908DA	RC723D	µA723CF
µA7805KC	7805CDA	µA7908KC	7908CDA	RC723T	µA723CT
µA7805KM	7805DA	µA7908KM	7908DA	RC733D	µA733CF
µA7805MKA	7805DA	µA7908UC	7908CU	RC733T	µA733CT
µA7805UC	7805CU	µA7912CKA	7912CDA	RC741D	µA741CF
µA7806CKA	7806CDA	µA7912CKC	7912CU	RC741DN	µA741CN
µA7806CKC	7806CU	µA7912KA	7912DA	RC741DP	µA741CN-14
µA7806KC	7806CDA	µA7912KC	7912CDA	RC741T	µA741CT
µA7806KM	7806DA	µA7912KM	7912DA	RC747D	µA747CF
µA7806MKA	7806DA	µA7912UC	7912CU	RC747T	µA747CT
µA7806UC	7806CU	µA7915CKA	7915CDA	RC748T	µA748CT
µA7808CKA	7808CDA	µA7915CKC	7915CU	RC1458DN	MC1458N
µA7808CKC	7808CU	µA7915KA	7915DA	RC1458T	MC1458T
µA7808KC	7808CDA	µA7915KC	7915CDA	RC1488DC	MC1488F
µA7808KM	7808DA	µA7915KM	7915DA	RC1489ADC	MC1489AF
µA7808MKA	7808DA	µA7915UC	7915CU	RC1489DC	MC1489F
µA7808UC	7808CU	µA7918CKA	7918CDA	RC1556T	MC1456T
µA7812CKA	7812CDA	µA7918CKC	7918CU	SE555JG	SE555FE
µA7812CKC	7812CU	µA7918KA	7918DA	SE555L	SE555T
µA7812KC	7812CDA	µA7918KC	7918CDA	SE592G	SE592T
µA7812KM	7812DA	µA7918KM	7918DA	SE592L	SE592F
µA7812MKA	7812DA	µA7918UC	7918CU	SFC2101A	LM101AT
µA7812UC	7812CU	µA7924CKA	7924CDA	SFC2107M	LM107T
µA7815CKA	7815CDA	µA7924CKC	7924CU	SFC2111M	LM111T
µA7815CKC	7815CU	µA7924KA	7924DA	SFC2201A	LM201AT
µA7815KC	7815CDA	µA7924KC	7924CDA	SFC2207	LM207T
µA7815KM	7815DA	µA7924KM	7924DA	SFC2208	LM208T
µA7815MKA	7815DA	µA7924UC	7924CU	SFC2211	LM211T
µA7815UC	7815CU	µAF155AHM	LF155AT	SFC2301A	LM301AT

professional analogue replacement

type to be replaced	replacement
SFC2301ADC	LM301AN
SFC2307	LM307T
SFC2308	LM308T
SFC2309	LM309DA
SFC2311	LM311T
SFC2709C	µA709CT
SFC2709EC	µA709CN
SFC2709EM	µA709N
SFC2709M	µA709T
SFC2710C	µA710CT
SFC2710EC	µA710CN
SFC2710EM	µA710N
SFC2710M	µA710T
SFC2711C	µA711CK
SFC2711EC	µA711CN
SFC2711EM	µA711N
SFC2711M	µA711K
SFC2741C	µA741CT
SFC2741DC	µA741CV
SFC2741EC	µA741CN
SFC2741EM	µA741N
SFC2741M	µA741T
SFC2748C	µA748CT
SFC2748DC	µA748CV
SN7520J	7520F
SN7520N	7520N
SN7521J	7521F
SN7521N	7521N
SN7522J	7522F
SN7522N	7522N
SN7523J	7523F
SN7523N	7523N
SN7524J	7524F
SN7524N	7524N
SN7525J	7525F
SN7525N	7525N
SN7528J	7528F
SN7528N	7528N
SN52101AJ	LM101AF
SN52101AL	LM101AT
SN52107J	LM107F
SN52107L	LM107T
SN52108AJ	LM108AF
SN52108AL	LM108AT
SN52108J	LM108F
SN52108L	LM108T
SN52109LA	LM109DB
SN52111J	LM111F
SN52111T	LM111T
SN52555L	SE555T
SN52558L	MC1558T
SN52709AJ	µA709AF
SN52709AL	µA709AT
SN52709J	µA709F
SN52709L	µA709T
SN52710J	µA710F
SN52710L	µA710T
SN52711J	µA711F
SN52711L	µA711T
SN52723J	µA723F
SN52723L	µA723T
SN52733J	µA733F
SN52733L	µA733T
SN52741J	µA741F
SN52741L	µA741T
SN52747J	µA747F
SN52747L	µA747T
SN52748J	µA748F
SN52748L	µA748T
SN52771J	MC1556F
SN52771L	MC1556T
SN55182J	DS7820F
SN55182N	DS7820N
SN55183J	DS7830F
SN55183N	DS7830N
SN55325J	55325F
SN55450BJ	55450BF
SN55450BN	55450BN
SN55451BJG	55451BFE
SN55451BL	55451BT
SN55452BJG	55452BFE
SN55452BL	55452BT
SN55453BJG	55453BFE
SN55453BL	55453BT
SN55454BJG	55454BFE
SN55454BL	55454BT
SN72301AJ	LM301AF
SN72301AL	LM301AT
SN72301AN	LM301AN-14
SN72301AP	LM301AN
SN72307J	LM307F
SN72307L	LM307T
SN72307N	LM307N-14
SN72307P	LM307N
SN72308AJ	LM308AF
SN72308AL	LM308AT
SN72308AP	LM308AN
SN72308J	LM308F
SN72308L	LM308T
SN72308P	LM308N
SN72309LA	LM309DB
SN72311J	LM311F
SN72311L	LM311T
SN72311N	LM311N-14
SN72311P	LM311N
SN72555L	NE555T
SN72555P	NE555N
SN72558L	MC1458T
SN72558P	MC1458N
SN72709J	µA709CF
SN72709L	µA709CT
SN72709N	µA709CN-14
SN72709P	µA709CN
SN72710J	µA710CF
SN72710L	µA710CT
SN72710N	µA710CN-14
SN72710P	µA710CN
SN72711J	µA711CF
SN72711L	µA711CT
SN72711N	µA711CN
SN72723J	µA723CF
SN72723L	µA723CT
SN72723N	µA723CN
SN72733J	µA733CF
SN72733L	µA733CT
SN72733N	µA733CN
SN72741J	µA741CF
SN72741L	µA741CT
SN72741N	µA741CN-14
SN72741P	µA741CN
SN72747J	µA747CF
SN72747L	µA747CT
SN72747N	µA747CN
SN72748J	µA748CF
SN72748L	µA748CT
SN72748N	µA748CN-14
SN72748P	µA748CN
SN72771J	MC1456F
SN72771N	MC1456N
SN72771T	MC1456T
SN75107AT	75S107F
SN75107AN	75S107N
SN75108AT	75S108F
SN75108AN	75S108N
SN75182J	DS8820F
SN75182N	DS8820N
SN75183J	DS8830F
SN75183N	DS8830N
SN75188J	MC1488F
SN75188N	MC1488N
SN75189AT	MC1489AF
SN75189AN	MC1489AN
SN75189J	MC1489F
SN75189N	MC1489N
SN75207J	75S207F
SN75207N	75S207N
SN75208J	75S208F
SN75208N	75S208N
SN75324J	75324F
SN75324N	75324N
SN75450BJ	75450BF
SN75451BJG	75452BFE
SN75451BL	75451BT
SN75450BN	75450BN
SN75451BP	75451BN

type to be replaced	replacement	type to be replaced	replacement	type to be replaced	replacement
SN75452BJG	75452BFE	556CJ	NE556CN	9667DC	ULN2003F
SN75452BL	75452BT	709AE	µA709AT	9667PC	ULN2003N
SN75452BP	75452BN	709AL	µA709AF	55325DM	55325F
SN75453BJG	75453BFE	709BE	µA709T	55450BDM	55450BF
SN75453BL	75453BT	709BL	µA709F	55451BHM	55451BT
SN75453BP	75453BN	709CE	µA709CT	55451BRM	55451BFE
SN75454JG	75454FE	709CJ	µA709CN-14	55452BHM	55452BT
SN75454L	75454T	709CL	µA709CF	55452BRM	55452BFE
SN75454P	75454N	710BE	µA710T	55453BHM	55453BT
SN75466J	NE5501F	710BL	µA710F	55453BRM	55453BFE
SN75466N	NE5501N	710CE	µA710CT	55454BHM	55454BT
SN75467J	NE5502F	710CL	µA710CF	55454BRM	55454BFE
SN75467N	NE5502N	711BE	µA711T	75107ADC	75S107F
SN75468J	NE5503F	711BL	µA711F	75107APC	75S107N
SN75468N	NE5503N	711CE	µA711CT	75108ADC	75S108F
SN75469J	NE5504F	711CJ	µA711CN	75108APC	75S108N
SN75469N	NE5504N	711CL	µA711CF	75207DM	75S207F
TBB0747	µA747CK	723BE	µA723T	75207PC	75S207N
TBB0748	µA748CT	723CE	µA723CT	75208DM	75S208F
TBB0748B	µA748CN	723CT	µA723CN	75208PC	75S208N
TBB1458	MC1458T	723CL	µA723CF	75325DC	75325F
TBB1458B	MC1458N	733BE	µA733T	75325PC	75325N
TBC0747	µA747K	733CE	µA733CT	75450BDC	75450BF
TBC1458	MC1558T	733CJ	µA733CN	75450BPC	75450BN
TDB0555	NE555T	741BE	µA741T	75451BDC	75451BF
TDB0555B	NE555N	741BL	µA741F	75451BHC	75451BT
TDB0556A	NE556N	741CE	µA741CT	75451BRC	75451BFE
TDB0723	µA723CK	741CJ	µA741CN-14	75451BTC	75451BN
TDB0723A	µA723CN	741CP	µA741CN	75452BHC	75452BT
TDB7805	7805CDN	747BE	µA747T	75452BRC	75452BFE
TDB7805T	7805CU	747BL	µA747F	75452BTC	75452BN
TDB7806	7806CDA	747CE	µA747CT	75453BHC	75453BT
TDB7806T	7806CU	747CJ	µA747CN	75453BRC	75453BFE
TDB7808	7808CDA	747CL	µA747CF	75453BTC	75453BN
TDB7808T	7808CU	748BE	µA748T	75454BHC	75454BT
TDB7812	7812CDA	748BL	µA748F	75454BRC	75454BFE
TDB7812T	7812CU	748CE	µA748CT	75454BTC	75454BN
TDB7815	7815CDA	748CL	µA748CF		
TDB7815T	7815CU	748CP	µA748CN-14		
TDB7818	7818CDA	1458CE	MC1458T		
TDB7818T	7818CU	1458CP	MC1458N		
TDB7824	7824CDA	1458E	MC1458T		
TDB7824T	7824CU	1458P	MC1458N		
TDC0555	SE555T	1558E	MC1558T		
TDC0723	µA723K	2740CE	µA740CT		
TL430JG	TL430FE	7524DC	7524F		
TL430LP	TL430S	7524PC	7524N		
UDN5711M	UDN5711N	7525DC	7525F		
UDN5712M	UDN5712N	7525PC	7525N		
UDN5713M	UDN5713N	7528DC	7528F		
UDN5714M	UDN5714N	7528PC	7528N		
ULN2001A	ULN2001N	9665DC	ULN2001F		
ULN2002A	ULN2002N	9665PC	ULN2001N		
ULN2003A	ULN2003N	9666DC	ULN2002F		
ULN2004A	ULN2004N	9666PC	ULN2002N		

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device no.	temp. range	max input voltage offset mV	max input voltage drift µV/°C	max input current offset nA	max input current bias nA	min A_{VOL} V/mV	typ BW $A_V = 1$ MHz	typ slew rate V/µs	typical common mode rej. ratio dB	typical common mode volt. range V
LF155	military	7,00	5,0 ●	20	50	25	2,5	5,0	100	± 12
LF255	industrial	6,50	5,0 ●	1,0	5,0	25	2,5	5,0	100	± 12
LF355	commercial	13,0	5,0 ●	2,0	8,0	15	2,5	5,0	100	± 12
LF156	military	7,00	5,0 ●	20	50	25	5,0	12,0	100	± 12
LF256	industrial	6,50	5,0 ●	1,0	5,0	25	5,0	12,0	100	± 12
LF356	commercial	13,0	5,0 ●	2,0	8,0	15	5,0	12,0	100	± 12
LF157	military	7,00	5,0 ●	20	50	25	20	50,0	100	± 12
LF257	industrial	6,50	5,0 ●	1,0	5,0	25	20	50,0	100	± 12
LF357	commercial	13,0	5,0 ●	2,0	8,0	15	20	50,0	100	± 12
LF155A	military	2,50	5,0	10	25	25	2,5	5,0	100	± 12
LF355A	commercial	2,30	5,0	1,0	5,0	15	2,5	5,0	100	± 12
LF156A	military	2,50	5,0	10	25	25	5,0	12,0	100	± 12
LF356A	commercial	2,30	5,0	1,0	5,0	15	5,0	12,0	100	± 12
LF157A	military	2,50	5,0	10,0	25	25	20	50,0	100	± 12
LF357A	commercial	2,30	5,0	1,0	5,0	15	20	50,0	100	± 12
LM101	military	6,00	3,0 ■	500	1500	25	1,0	0,5	90	± 12
LM201	industrial	10,0	6,0 ■	750	2000	15	1,0	0,5	90	± 12
LM101A	military	3,00	15	20	100	25	1,0	0,5	96	± 15
LM201A	industrial	3,00	15	20	100	25	1,0	0,5	96	± 15
LM301A	commercial	10,0	30	70	300	15	1,0	0,5	90	± 12
LM107	military	3,00	15	20	100	25	1,0	0,5	96	± 15
LM207	industrial	3,00	15	20	100	25	1,0	0,5	96	± 15
LM307	commercial	10,0	30	70	300	15	1,0	0,5	90	± 12
LM108	military	3,00	15	0,4	3,0	25	1,0	0,3	100	± 13,5
LM208	industrial	3,00	15	0,4	3,0	25	1,0	0,3	100	± 13,5
LM308	commercial	10,0	30	1,5	10,0	15	1,0	0,3	100	± 14
LM108A	military	1,00	5,0	0,4	3,0	40	1,0	0,3	110	± 13,5
LM208A	industrial	1,00	5,0	0,4	3,0	40	1,0	0,3	110	± 13,5
LM308A	commercial	0,75	5,0	1,5	10,0	60	1,0	0,3	110	± 14
MC1456	commercial	14,0	–	14,0	40	40	1,0	2,5	110	± 12
MC1556	military	6,00	–	5,0	30	40	1,0	2,5	110	± 13
NE530	commercial	6,00	6,0 ●	80	200	15	3,0	35	90	± 13
SE530	military	3,00	15	20	100	25	3,0	35	90	± 13
NE531	commercial	7,50	–	300	2000	15	1,0	35	90	± 11
SE531	military	6,00	–	500	1500	25	1,0	35	90	± 11
NE535	commercial	6,00	6,0 ●	80	200	15	1,0	15	90	± 13
SE535	military	3,00	15	20	100	25	1,0	15	90	± 13

Specifications guaranteed over full temperature range unless otherwise indicated by following marks:

- ● typical over full temperature range
- ▲ guaranteed at 25 °C
- ■ typical at 25 °C

diff. input voltage V	typ PSRR dB	supply voltage typ min V	supply voltage max V	output current mA	max supply current mA	min output volt. swing V	internal compen-sation	packages	page no.
± 40	100	± 3	± 22	–	4,0	± 12	yes	T	
± 40	100	± 3	± 22	–	4,0	± 12	yes	T	B26
± 30	100	± 3	± 18	–	4,0	± 12	yes	T	
± 40	100	± 3	± 22	–	7,0	± 12	yes	T	
± 40	100	± 3	± 22	–	7,0	± 12	yes	T	B26
± 30	100	± 3	± 18	–	10,0	± 12	yes	T	
± 40	100	± 3	± 22	–	7,0	± 12	yes	T	
± 40	100	± 3	± 22	–	7,0	± 12	yes	T	B26
± 30	100	± 3	± 18	–	10,0	± 12	yes	T	
± 40	100	± 3	± 22	–	4,0	± 12	yes	T	B26
± 30	100	± 3	± 18	–	4,0	± 12	yes	T	
± 40	100	± 3	± 22	–	7,0	± 12	yes	T	B27
± 30	100	± 3	± 18	–	10,0	± 12	yes	T	
± 40	100	± 3	± 22	–	7,0	± 12	yes	T	B27
± 30	100	± 3	± 18	–	10,0	± 12	yes	T	
± 30	90	± 3	± 22	5,0	2,5	± 12	no	F,FE,N,N-14,T	B28
± 30	90	± 3	± 22	5,0	3,0 ▲	± 12	no	F,FE,N,N-14,T	
± 30	96	± 3	± 22	7,5	2,5	± 12	no	F,FE,N,N-14,T	
± 30	96	± 3	± 22	5,0	2,5	± 12	no	F,FE,N,N-14,T	B29
± 30	96	± 3	± 18	5,0	3,0 ▲	± 12	no	F,FE,N,N-14,T	
± 30	96	± 3	± 22	7,5	2,5	± 12	yes	F,FE,N,T	
± 30	96	± 3	± 22	5,0	2,5	± 12	yes	F,FE,N,T	B29
± 30	96	± 3	± 18	5,0	3.0 ▲	± 12	yes	F,FE,N,T	
–	96	± 2	± 20	1,0	0,4	± 13	no	F,FE,N,T	
–	96	± 2	± 20	1,0	0,4	± 13	no	F,FE,N,T	B30
–	96	± 2	± 18	1,0	0,8 ▲	± 13	no	F,FE,N,T	
–	110	± 2	± 20	1,0	0,4	± 13	no	F,FE,T	
–	110	± 2	± 20	1,0	0,4	± 13	no	F,FE,T	B30
–	110	± 2	± 18	1,0	0,8 ▲	± 13	no	F,FE,N,T	
± 18	86	± 3	± 18	20	3,0 ▲	± 11	yes	F,N,T	B34
± 22	86	± 3	± 22	20	1,5 ▲	± 12	yes	F,N,T	
± 30	110	± 3	± 18	5,0	3,0	± 12	yes	FE,N,T	B35
± 30	110	± 3	± 22	5,0	3,0	± 12	yes	FE,N,T	
± 15	100	± 5	± 22	5,0	10 ▲	± 10	no	N,T	B36
± 15	100	± 5	± 22	5,0	7,0 ▲	± 10	no	T	
± 30	110	± 3	± 18	5,0	3,0	± 12	yes	FE,N,T	B37
± 30	110	± 3	± 22	5,0	3,0	± 12	yes	FE,N,T	

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For low noise specifications of very low noise op amps
NE/SE5534 and **TDA1034** see page **B41**.

Single op amps

device no.	temp. range	max input voltage offset mV	max input voltage drift µV/°C	max input current offset nA	max input current bias nA	min A_{VOL} V/mV	typ BW A_V = 1 MHz	typ slew rate V/µs	typical common mode rej. ratio dB	typical common mode volt. range V
NE536	commercial	30 ●	30 ●	5 pA ■	0,1 ▲	25	1,0	6,0	80	± 11
SU536	military	30	20 ●	5 pA ■	3,0	50	1,0	6,0	80	± 11
NE538	commercial	6,0	6,0 ●	80	200	25	6,0	60	90	± 13
SE538	military	3,0	15	20	100	25	6,0	60	90	± 13
NE5534	commercial	5,0	—	400	2000	15	10	13	100	± 13
SE5534	military	3,0	—	500	1500	25	10	13	100	± 13
TDA1034	industrial	5,0	—	500	2000	15	10	13	100	± 13
µA709	military	6,0	6,0 ●	500	1500	25	1,0	0,3	90	± 10
µA709A	military	3,0	25	250	600	25	1,0	0,3	110	± 10
µA709C	commercial	10,0	12,0 ●	750	1500	12	1,0	0,3	90	± 10
SA709C	ext. ind.	10,0	12,0 ●	750	1500	12	1,0	0,3	90	± 10
µA740C	commercial	30 ●	—	0,06 ●	10,0	500 ●	1,0	6,0	80	± 12
µA741	military	6,0	—	500	1500	25	1,0	0,5	90	± 13
µA741C	commercial	7,5	—	300	800	15	1,0	0,5	90	± 13
SA741C	ext. ind.	6,0	—	500	1500	15	1,0	0,5	90	± 13
µA748	military	6,0	—	500	1500	25	1,0	0,5	90	± 13
µA748C	commercial	7,5	—	300	800	25	1,0	0,5	90	± 13
SA748C	ext. ind.	7,5	—	500	1500	25	1,0	0,5	90	± 13
TCA520	commercial	6,0 ▲	5,0 ●	30 ▲	100 ▲	—	1,0 ▲	0,3 ▲	100 ▲	± 11 ▲
TDA0301	commercial	—	—	—	—	—	—	—	—	—
TDA0741	commercial	7,5	—	300	800	15	1,0	0,5	90	± 13
TDA0748	commercial	6 ▲	—	200 ▲	500 ▲	15	1,0	0,5	90	± 13
TDA1078 NE5539	commercial	5,0 ▲	—	—	—	—	2,0	800 ■	85 ■	—

Specifications guaranteed over full temperature range unless otherwise indicated by following marks:

- ● typical over full temperature range
- ▲ guaranteed at 25 °C
- ■ typical at 25 °C

diff. input voltage V	typ PSRR dB	supply voltage typ min V	supply voltage max V	output current mA	max supply current mA	min output volt. swing V	internal compen-sation	packages	page no.
± 30	80	± 6	± 20	5,0	8,0 ▲	± 12	yes	T	B37
± 30	86	± 6	± 18	5,0	5,5 ▲	± 12	yes	T	
± 30	110	± 3	± 18	5,0	3,0	± 12	yes	FE,N,T	B37
± 30	110	± 3	± 22	5,0	3,0	± 12	yes	FE,N,T	
± 30	100	± 3	± 20	10	8,0	± 12	yes	FE,N,T	B41
± 30	100	± 3	± 20	10	6,5	± 12	yes	FE,N,T	
± 30	100	± 3	± 20	10	8,0	± 12	yes	FE,N,T	B41
± 5	92	± 9	± 18	5,0	5,5 ▲	± 12	no	F,N,N-14,T	
± 5	92	± 9	± 18	5,0	5,5 ▲	± 12	no	F,N,N-14,T	B32
± 5	92	± 9	± 18	5,0	6,6 ▲	± 12	no	F,N,N-14,T	
± 5	92	± 9	± 18	5,0	6,6 ▲	± 12	no	F,FE,N,N-14	B32
± 30	80	± 5	± 22	5,0	8,0 ▲	± 12	yes	T	B32
± 30	100	± 3	± 22	5,0	2,5	± 12	yes	F,FE,N,N-14,T	B33
± 30	100	± 3	± 18	5,0	2,8 ▲	± 12	yes	F,FE,N,N-14,T	
± 30	100	± 3	± 18	5,0	2,8 ▲	± 12	yes	F,FE,N,N-14,T	B33
± 30	90	± 3	± 22	5,0	2,8	± 12	no	F,FE,N,N-14,T	B34
± 30	90	± 3	± 18	5,0	2,8	± 12	no	F,FE,N,N-14,T	
± 30	90	± 3	± 18	5,0	2,8	± 12	no	F,FE,N,N-14,T	B34
± 6 ▲	–	2	22	12,0 ▲	1,5 ■	–	no	FE, N, SO-8	B39
–	–	–	–	–	–	–	–	SO-8	B40
± 30	100	± 3	± 18	5,0	2,8 ▲	± 12	yes	SO-8	B40
± 30	100	± 3	± 18	5,0	2,8 ▲	± 12	yes	SO-8	B41
–	–	± 8	± 12	40 ■	15 ■	–	no	N-14	B42

operational amplifiers

selection guide

For low noise specifications of very low noise op amps
NE/SE5533 see page B38.

Dual op amps

device no.	temp. range	max input voltage offset mV	max input voltage drift µV/°C	max input current offset nA	max input current bias nA	min A_{VOL} V/mV	typ BW A_V = 1 MHz	typ slew rate V/µs	typical common mode rej. ratio dB	typical common mode volt. range V
LH2101A	military	3,0	15	20	100	25	1,0	0,5	96	± 15
LH2201A	industrial	3,0	15	20	100	25	1,0	0,5	96	± 15
LH2301A	commercial	10,0	30	70	300	15	1,0	0,5	90	± 12
LH2108	military	3,0	15	0,4	3,0	25	1,0	0,3	100	± 13,5
LH2208	industrial	3,0	15	0,4	3,0	25	1,0	0,3	100	± 13,5
LH2308	commercial	10,0	30	1,5	10,0	15	1,0	0,3	100	± 14
LH2108A	military	1,0	5,0	0,4	3,0	40	1,0	0,3	110	± 13,5
LH2208A	industrial	1,0	5,0	0,4	3,0	40	1,0	0,3	110	± 13,5
LH2308A	commercial	0,75	5,0	1,5	10,0	60	1,0	0,3	110	± 14
LM158	military	7,0	7,0 ●	100	300	25	1,0	–	85	V_S–1,5
LM258	industrial	9,0	7,0 ●	150	500	25	1,0	–	85	V_S–1,5
LM358	commercial	9,0	7,0 ●	150	500	15	1,0	–	85	V_S–1,5
LM158A	military	4,0	15,0	30	100	25	1,0	–	85	V_S–1,5
LM258A	industrial	4,0	15,0	30	100	25	1,0	–	85	V_S–1,5
LM358A	commercial	5,0	20,0	75	200	15	1,0	–	85	V_S–1,5
MC1458	commercial	7,5	–	300	800	15	1,0	0,8	90	± 13
MC1558	military	6,0	–	500	1500	25	1,0	0,5	90	± 13
SA1458	ext. ind.	7,5	–	500	1500	15	1,0	0,5	90	± 13
NE532	commercial	7,5	7,0 ●	150	500	15	1,0	–	85	V_S–1,5
SA532	ext. ind.	7,5	7,5 ●	150	500	15	1,0	–	85	V_S–1,5
SE532	military	7,0	7,0 ●	100	300	25	1,0	–	85	V_S–1,5
NE532A	commercial	5,0	20	75	200	15	1,0	–	85	V_S–1,5
SE532A	military	4,0	15	30	100	25	1,0	–	85	V_S–1,5
NE5530	commercial	6,0	6,0 ●	80	200	15	3,0	35	90	± 13
SE5530	military	3,0	15	20	100	25	3,0	35	90	± 13
NE5533	commercial	5,0	–	400	2000	15	10	13	100	± 13
SE5533	military	3,0	–	500	1500	25	10	13	100	± 13
NE5535	commercial	6,0	6,0 ●	80	200	15	1,0	15	90	± 13
SE5535	military	3,0	15	20	100	25	1,0	15	90	± 13
NE5538	commercial	6,0	6,0 ●	80	200	25	6,0	60	90	± 13
SE5538	military	3,0	15	20	100	25	6,0	60	90	± 13
µA747	military	6,0	–	500	1500	25	1,0	0,5	90	± 13
µA747C	commercial	7,5	–	300	800	15	1,0	0,5	90	± 13
SA747C	ext. ind.	7,5	–	500	1500	15	1,0	0,5	90	± 13
TDA0358	commercial	5,0	20	75	200	15	1,0	–	85	V_S–1,5
TDA1458	commercial	7,5	–	300	800	15	1,0	0,5	90	± 13

Specifications guaranteed over full temperature range unless otherwise indicated by following marks:

- ● typical over full temperature range
- ▲ guaranteed at 25 °C
- ■ typical at 25 °C

diff. input voltage V	typ PSRR dB	supply voltage typ min V	max V	output current mA	max supply current mA	min output volt. swing V	internal compen-sation	packages	page no.
± 30	96	± 3	± 22	7,5	2,5	± 12	no	F	
± 30	96	± 3	± 22	5,0	2,5	± 12	no	F	B27
± 30	96	± 3	± 18	5,0	3,0▲	± 12	no	F	
–	96	± 2	± 20	1,0	0,4	± 13	no	F	
–	96	± 2	± 20	1,0	0,4	± 13	no	F	B28
–	96	± 2	± 18	1,0	0,8▲	± 13	no	F	
–	110	± 2	± 20	1,0	0,4	± 13	no	F	
–	110	± 2	± 20	1,0	0,4	± 13	no	F	B28
–	110	± 2	± 18	1,0	0,8▲	± 13	no	F	
32	100	3	30	40	2,0	V_S–2	yes	FE,N,T	
32	100	3	30	40	2,0	V_S–2	yes	FE,N,T	B31
32	100	3	30	40	2,0	V_S–2	yes	FE,N,T	
32	100	3	30	40	2,0	V_S–2	yes	FE,N,T	
32	100	3	30	40	2,0	V_S–2	yes	FE,N,T	B31
32	100	3	30	40	2,0	V_S–2	yes	FE,N,T	
± 30	90	± 3	± 18	5,0	5,6▲	± 12	yes	F,FE,N,N-14,T	
± 30	90	± 3	± 22	5,0	5,0▲	± 12	yes	F,FE,N,N-14,T	B35
± 30	90	± 3	± 22	5,0	5,6▲	± 12	yes	F,FE,N,N-14,T	
32	100	3	30	40	1,2	V_S–2	yes	FE,N,T	
32	100	3	30	40	1,2	V_S–2	yes	FE,N,T	B36
32	100	3	30	40	1,2	V_S–2	yes	FE,N,T	
32	100	3	30	40	1,2	V_S–2	yes	FE,N,T	B36
32	100	3	30	40	1,2	V_S–2	yes	FE,N,T	
± 30	110	± 3	± 18	5,0	3,0	± 12	yes	FE,N,T	B38
± 30	110	± 3	± 22	5,0	3,0	± 12	yes	FE,N,T	
± 30	100	± 3	± 20	10	8,0	± 12	yes	F,FE,N,N-14,T	B38
± 30	100	± 3	± 20	10	6,5	± 12	yes	F,FE,N,N-14,T	
± 30	110	± 3	± 18	5,0	3,0	± 12	yes	F,FE,N,N-14,T	B38
± 30	110	± 3	± 22	5,0	3,0	± 12	yes	F,FE,N,N-14,T	
± 30	110	± 3	± 18	5,0	–	± 12	yes	F,FE,N,N-14,T	B39
± 30	110	± 3	± 22	5,0	–	± 12	yes	F,FE,N,N-14,T	
± 30	90	± 3	± 22	5,0	3,3	± 12	yes	F,K,N-14	B33
± 30	90	± 3	± 18	5,0	3,3	± 12	yes	F,K,N-14	
± 30	90	± 3	± 18	5,0	3,3	± 12	yes	F,K,N-14	B33
32	100	3	30	40	2,0	V_S–2	yes	SO-8	B40
± 30	100	± 3	± 18	5,0	2,8▲	± 12	yes	SO-8	B42

operational amplifiers

selection guide

Triple op amps

device no.	temp. range	max input voltage offset mV	max input voltage drift μV/°C	max input current offset nA	max input current bias nA	min A_{VOL} V/mV	typ BW A_V = 1 MHz	typ slew rate V/μs	typical common mode rej. ratio dB	typical common mode volt. range V
TCA220	commercial	10,0 ▲	–	200 ▲	2000 ▲	4,0 ■	5,0	0,4	90	18

Quadruple op amps

LM124	military	7,0	7,0 ●	100	300	25	1,0	–	85	V_S–1,5
LM224	industrial	9,0	7,0 ●	150	500	15	1,0	–	85	V_S–1,5
LM324	commercial	9,0	7,0 ●	150	500	15	1,0	–	85	V_S–1,5
SA534	ext. ind.	9,0	7,0 ●	150	500	15	1,0	–	85	V_S–1,5
LM2902	ext. ind.	15,0	7,0 ●	200	1000	15	1,0	–	85	V_S–1,5
LM124A	military	4,0	20	30	100	25	1,0	–	85	V_S–1,5
LM224A	industrial	4,0	20	30	100	25	1,0	–	85	V_S–1,5
LM324A	commercial	5,0	30	75	200	15	1,0	–	85	V_S–1,5
TDA0324	commercial	9,0	7,0 ●	150	500	15	1,0	–	85	V_S–1,5

Specifications guaranteed over full temperature range unless otherwise indicated by following marks:

- ● typical over full temperature range
- ▲ guaranteed at 25 °C
- ■ typical at 25 °C

diff. input voltage V	typ PSRR dB	supply voltage typ min V	max V	output current mA	max supply current mA	min output volt. swing V	internal compen-sation	packages	page no.
5,0	66	–	18	100	1,0 ■	5	no	N-16	B39
32	100	3	30	40	2,0	V_S-2	yes	F,N-14	
32	100	3	30	40	2,0	V_S-2	yes	F,N-14	B30
32	100	3	30	40	2,0	V_S-2	yes	F,N-14	
32	100	3	30	40	2,0	V_S-2	yes	F,N-14	B30
26	100	3	26	40	2,0	V_S-2	yes	N-14	B30
32	100	3	30	40	2,0	V_S-2	yes	F,N-14	
32	100	3	30	40	2,0	V_S-2	yes	F,N-14	B31
32	100	3	30	40	2,0	V_S-2	yes	F,N-14	
32	100	3	30	40	2,0	V_S-2	yes	SO-14	B40

operational amplifiers

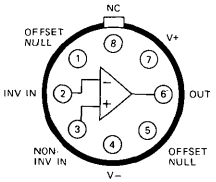
abridged data

J-FET input op amp — LF155/255/355

Temperature range:

Military	−55 °C to 125 °C	LF155T
Industrial	−25 °C to 85 °C	LF255T
Commercial	0 °C to 70 °C	LF355T

- Low supply current 4 mA(max)
- Input offset voltage 3 mV(typ)
- Input offset current 3 pA(typ)
- Input offset voltage drift 5 μV/ °C(typ)



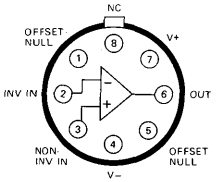
Package T

J-FET input op amp — LF155A/355A

Temperature range:

Military	−55 °C to 125 °C	LF155AT
Commercial	0 °C to 70 °C	LF355AT

- Low supply current 4 mA(max)
- Input offset voltage 1 mV(typ)
- Input offset current 3 pA(typ)
- Input offset voltage drift 5 μV/ °C(max)



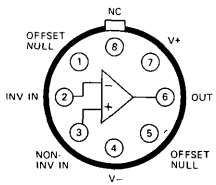
Package T

J-FET input op amp — LF156/256/356

Temperature range:

Military	−55 °C to 125 °C	LF156T
Industrial	−25 °C to 85 °C	LF256T
Commercial	0 °C to 70 °C	LF356T

- Fast slew rate 7,5 V/μs(min)
- Input noise voltage 12 nV/√Hz(typ)
- Input offset voltage 3 mV(typ)
- Input offset current 3 pA(typ)
- Input offset voltage drift 5 μV/ °C(typ)



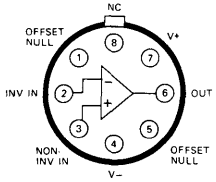
Package T

J-FET input op amp — LF157/257/357

Temperature range:

Military	−55 °C to 125 °C	LF157T
Industrial	−25 °C to 85 °C	LF257T
Commercial	0 °C to 70 °C	LF357T

- Extra fast slew rate 30 V/μs (min)
- Gain bandwidth product 20 MHz
- Input noise voltage 12 nV/√Hz (typ)
- Input offset voltage 3 mV (typ)
- Input offset current 3 pA (typ)
- Input offset voltage drift 5 μV/ °C (typ)



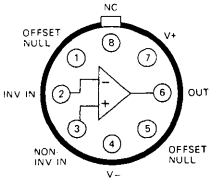
Package T

J-FET input op amp — LF156A/356A

Temperature range:

Military	−55 °C to 125 °C	LF156AT
Commercial	0 °C to 70 °C	LF356AT

- Fast slew rate 7,5 V/μs(min)
- Input noise voltage 12 nV/√Hz(typ)
- Input offset voltage 1 mV(typ)
- Input offset current 3 pA(typ)
- Input offset voltage drift 5 μV/ °C(max)



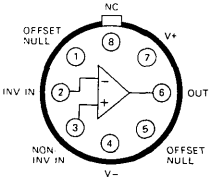
Package T

J-FET input op amp — LF157A/357A

Temperature range:

Military	−55 °C to 125 °C	LF157AT
Commercial	0 °C to 70 °C	LF357AT

- Extra fast slew rate 30 V/μs(min)
- Gain bandwidth product 20 MHz
- Input noise voltage 12 nV/√Hz(typ)
- Input offset voltage 1 mV(typ)
- Input offset current 3 pA(typ)
- Input offset voltage drift 5 μV/ °C(max)



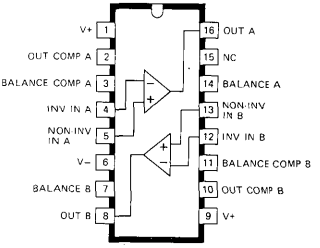
Package T

Dual high performance op amp — LH2101A/2201A/2301A

Temperature range:

Military	−55 °C to 125 °C	LH2101AF
Industrial	−25 °C to 85 °C	LH2201AF
Commercial	0 °C to 70 °C	LH2301AF

- Typical gain 160 000
- Input offset current 3,0 nA(typ)
- Input offset voltage 2 mV(typ)



Package F

operational amplifiers

abridged data

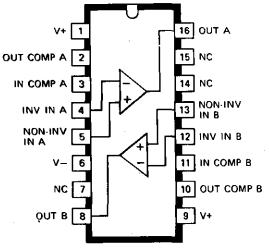
Dual precision op amp

LH2108/2208/2308

Temperature range:

Military	−55 °C to 125 °C	LH2108F
Industrial	−25 °C to 85 °C	LH2208F
Commercial	0 °C to 70 °C	LH2308F

- Super β input transistors
- Typical offset current 0,2 nA
- Typical offset voltage 2 mV
- Typical gain 300000



Package F

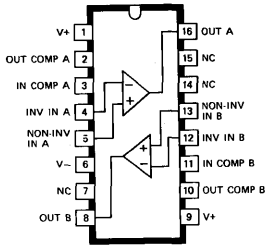
Dual precision op amp

LH2108A/2208A/2308A

Temperature range:

Military	−55 °C to 125 °C	LH2108AF
Industrial	−25 °C to 85 °C	LH2208AF
Commercial	0 °C to 70 °C	LH2308AF

- Super β input transistors
- Typical offset current 0,2 nA
- Typical offset voltage 0,3 mV
- Typical gain 300000



Package F

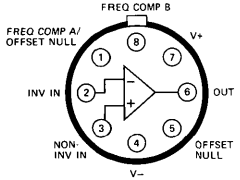
High performance op amp

LM101/201

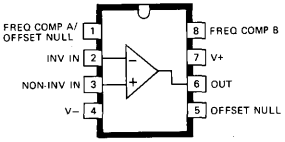
Temperature range:

Military	−55 °C to 125 °C	LM101F, FE, N, T
Commercial	0 °C to 70 °C	LM201F, FE, N, T

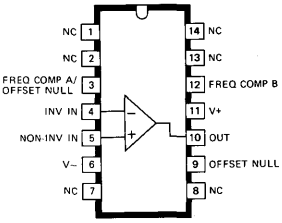
- Typical gain 150 000
- Input offset voltage 2 mV(typ)
- Output short-circuit protection



Package T



Package FE, N



Package F, N-14

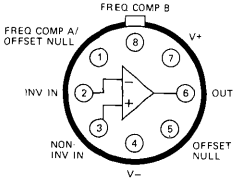
High performance op amp

LM101A/201A/301A

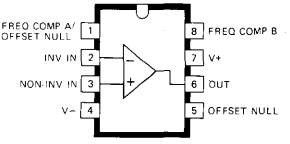
Temperature range:

Military	−55 °C to 125 °C	LM101AF, FE, N, T
Industrial	−25 °C to 85 °C	LM201AF, FE, N, T
Commercial	0 °C to 70 °C	LM301AF, FE, N, T

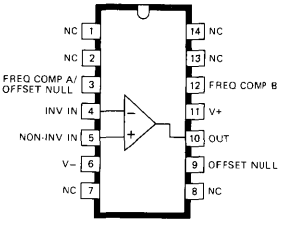
- Typical gain 160 000
- Input offset current, 3,0 nA(typ)
- Input offset voltage, 2 mV(typ)



Package T



Package FE, N



Package F, N-14

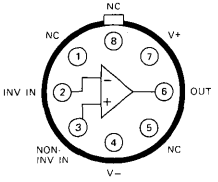
High performance op amp

LM107/207/307

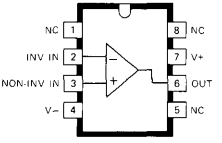
Temperature range:

Military	−55 °C to 125 °C	LM107F, FE, N, T
Industrial	−25 °C to 85 °C	LM207F, FE, N, T
Commercial	0 °C to 70 °C	LM307F, FE, N, T

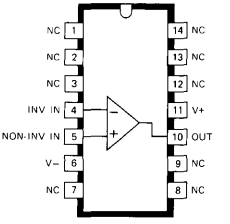
- Internally compensated
- Typical voltage gain 160 000
- Short-circuit protected input and output



Package T



Package FE, N



Package F

operational amplifiers

abridged data

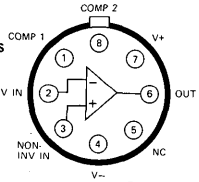
Precision op amp

LM108/208/308

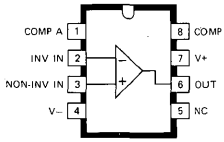
Temperature range:

Military	−55 °C to 125 °C	LM108F, FE, N, T
Industrial	−25 °C to 85 °C	LM208F, FE, N, T
Commercial	0 °C to 70 °C	LM308F, FE, N, T

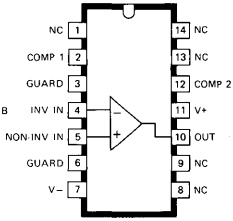
- Super β input transistors
- Low input offset and bias currents typically 0,2 and 1,5 nA
- Offset voltage typically 2 mV
- Typical gain 300 000



Package T



Package FE, N



Package F

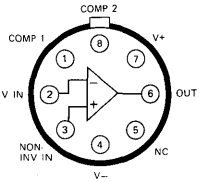
Precision op amp

LM108A/208A/308A

Temperature range:

Military	−55 °C to 125 °C	LM108AF, FE, T
Industrial	−25 °C to 85 °C	LM208AF, FE, T
Commercial	0 °C to 70 °C	LM308AF, FE, N, T

- Super β input transistors
- Typical offset current 0,2 nA
- Typical offset voltage 0,3 mV
- Typical gain 300 000



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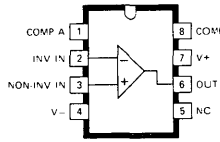
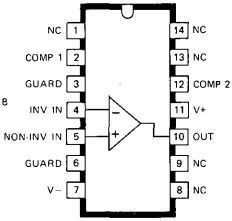


Package FE, N



Package F

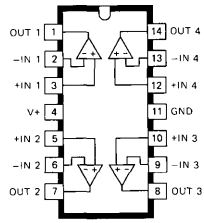
Quad op amp

LM124/224/324/2902
SA534

Temperature range:

Military	−55 °C to 125 °C	LM124F, N
Ext. Ind.	−40 °C to 85 °C	LM2902N/SA534F, N
Industrial	−25 °C to 85 °C	LM224F, N
Commercial	0 °C to 70 °C	LM324F, N

- Internally compensated
- Operation down to 3 volt supply
- Low power supply current 200 μA per amplifier
- Offset voltage 9 mV(max)



Package F, N-14

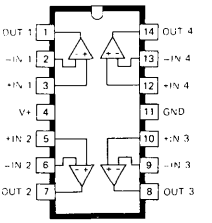
Quad op amp

LM124A/224A/324A

Temperature range:

Military	−55 °C to 125 °C	LM124AF, N
Industrial	−25 °C to 85 °C	LM224AF, N
Commercial	0 °C to 70 °C	LM324AF, N

- Internally compensated
- Operation down to 3 volt supply
- Low power supply current 200 μA per amplifier
- Offset voltage 3 mV(max)



Package F, N-14

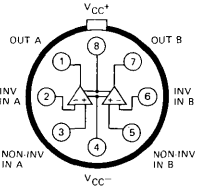
Dual low power op amp

LM158/258/358

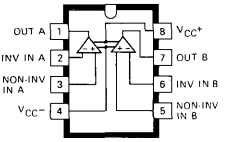
Temperature range:

Military	−55 °C to 125 °C	LM158FE, N, T
Industrial	−25 °C to 85 °C	LM258FE, N, T
Commercial	0 °C to 70 °C	LM358FE, N, T

- Internally compensated
- Operation down to 3 volt supply
- Supply current typically 200 μA per amplifier
- Offset voltage 9 mV(max)



Package T



Package FE, N

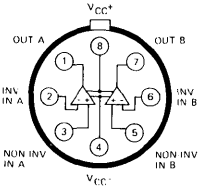
Dual low power op amp

LM158A/258A/358A

Temperature range:

Military	−55 °C to 125 °C	LM158AFE, N, T
Industrial	−25 °C to 85 °C	LM258AFE, N, T
Commercial	0 °C to 70 °C	LM358AFE, N, T

- Internally compensated
- Operation down to 3 volt supply
- Supply current typically 200 μA per amplifier
- Offset voltage 3 mV(max)



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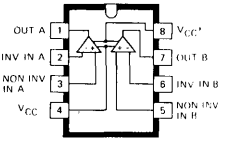


Package FE, N

operational amplifiers

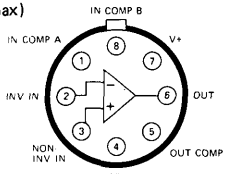
abridged data

Op amp

μA709A

Temperature range:
Military –55 °C to 125 °C μA709AF, N, T

- Open loop gain 45 000 typical
- Input voltage range typ ± 10 V
- Offset voltage 3 mV(max)



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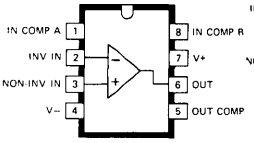
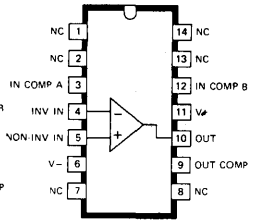


Package N



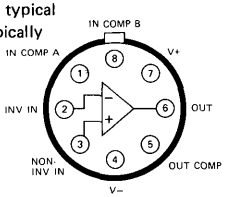
Package F, N-14

Op amp

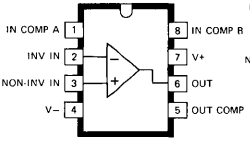
μA709/709C
SA709C

Temperature range:
Military –55 °C to 125 °C μA709F, N, T
Ext. Ind. –40 °C to 85 °C SA709CF, FE, N
Commercial 0 °C to 70 °C μA709CF, N, T

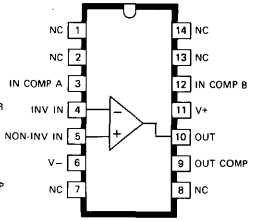
- Open loop gain 45 000 typical
- Input voltage range typically ± 10 Volts



Package T



Package FE, N



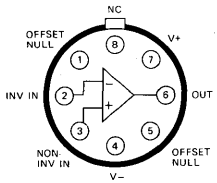
Package F, N-14

FET input op amp

μA740C

Temperature range:
Commercial 0 °C to 70 °C μA740CT

- Input bias current typically 100 pA
- Slew rate 6 V/μs
- Input impedance 10^{12} Ω
- Internally compensated



Package T

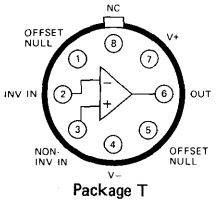
General purpose op amp

μA741/741C
SA741C

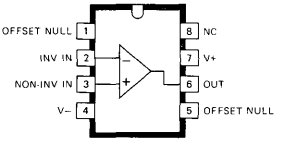
Temperature range:

Military	−55 °C to 125 °C	μA741F, FE, N, T
Ext. Ind.	−40 °C to 85 °C	SA741CF, FE, N, T
Commercial	0 °C to 70 °C	μA741CF, FE, N, T

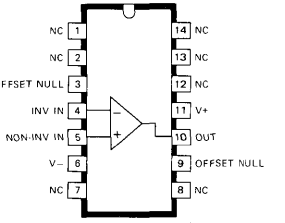
- Typical open loop gain 200 000
- Internal compensation
- Offset null capability
- Output impedance 75 Ω typical



Package T



Package FE, N



Package F, N-14

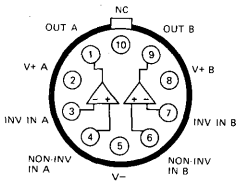
Dual general purpose op amp

μA747/747C
SA747C

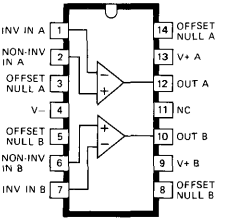
Temperature range:

Military	−55 °C to 125 °C	μA747F, K, N
Ext. Ind.	−40 °C to 85 °C	SA747CF, K, N
Commercial	0 °C to 70 °C	μA747CF, K, N

- Typical open loop gain 200 000
- Internally compensated
- Offset null capability
- Output impedance 75 Ω



Package K



Package F, N-14

operational amplifiers

abridged data

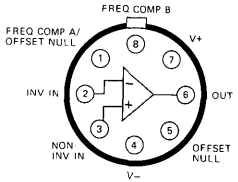
General purpose op amp

μA748/748C
SA748C

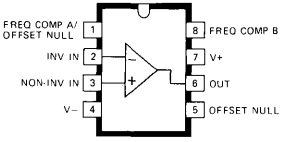
Temperature range:

Military	–55 °C to 125 °C	μA748F, FE, N, T
Ext. Ind.	–40 °C to 85 °C	SA748CF, FE, N, T
Commercial	0 °C to 70 °C	μA748CF, FE, N, T

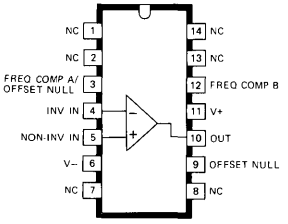
- Typical open loop gain 200 000
- Uncompensated
- Offset null capability
- Output impedance 75 Ω



Package T



Package FE, N



Package F, N-14

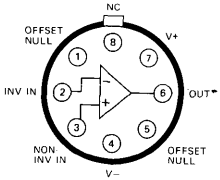
Precision op amp

MC1456/1556

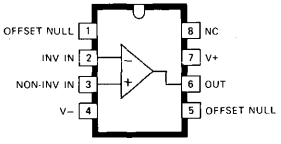
Temperature range:

Military	–55 °C to 125 °C	MC1556F, N, T
Commercial	0 °C to 70 °C	MC1456F, N, T

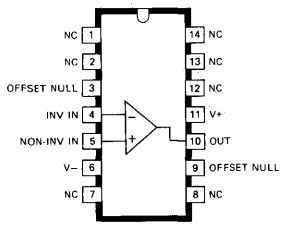
- Super β input transistor
- Low input offset and bias currents, typically 2,0 and 15,0 nA
- 2,5 V/μs slew rate
- Internally compensated



Package T



Package N



Package F

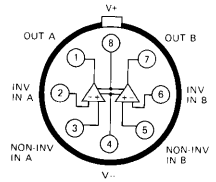
Dual general purpose op amp

MC1458/1558
SA1458

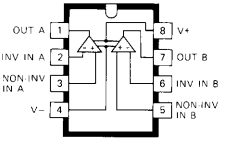
Temperature range:

Military	–55 °C to 125 °C	MC1558F, FE, N, T
Ext. Ind.	–40 °C to 85 °C	SA1458F, FE, N, T
Commercial	0 °C to 70 °C	MC1458F, FE, N, T

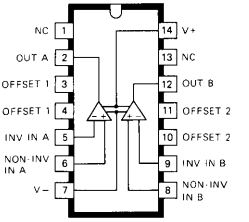
- Typical gain 100 000
- Internally compensated
- Unity gain slew rate 0,8 V/μs



Package T



Package FE, N



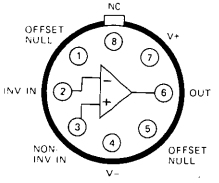
Package F, N-14

High slew rate op amp

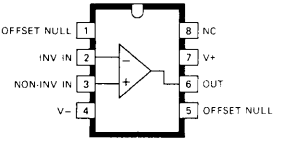
NE/SE530

Temperature range:

Military	–55 °C to 125 °C	SE530FE, N, T
Commercial	0 °C to 70 °C	NE530FE, N, T



Package T



Package FE, N

operational amplifiers

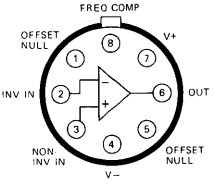
abridged data

High slew rate op amp

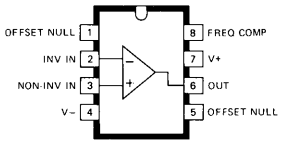
NE/SE531

Temperature range:
Military −55 °C to 125 °C SE531T
Commercial 0 °C to 70 °C NE531N, T

- 35 V/μs slew rate at unity gain
- 1 MHz small signal bandwidth
- 500 kHz large signal bandwidth
- Typical open loop gain 100 000
- Pin compatible with μA708, μA748 or LM101
- Compensated with a single capacitor
- Offset null capability



Package T



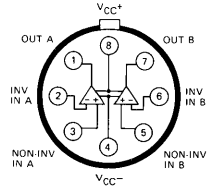
Package N

Dual low power op amp

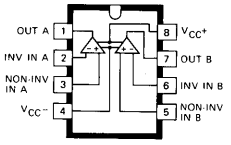
NE/SE532
SA532

Temperature range:
Military −55 °C to 125 °C SE532FE, N, T
Industrial −25 °C to 85 °C SA532FE, N, T
Commercial 0 °C to 70 °C NE532FE, N, T

- Internally compensated
- Operation down to 3 volt supply
- Supply current typically 200 μA per amplifier



Package T



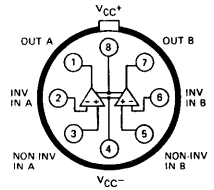
Package FE, N

Dual low power op amp

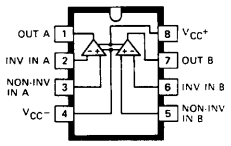
NE/SE532A

Temperature range:
Military −55 °C to 125 °C SE532AFE, N, T
Commercial 0 °C to 70 °C NE532AFE, N, T

Similar to NE/SE532, however
- better offset voltage
- better offset current
- lower input current



Package T



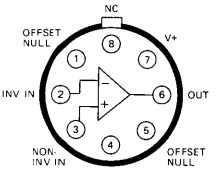
Package FE, N

High slew rate op amp

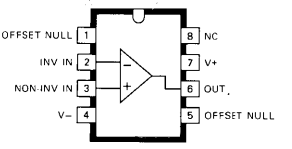
NE/SE535

Temperature range:
Military −55 °C to 125 °C SE535FE, N, T
Commercial 0 °C to 70 °C NE535FE, N, T

- 15 V/μs slew rate at unity gain
- Input offset voltage 2 mV (typ)
- Large common mode and differential voltage ranges
- Short-circuit protected



Package T



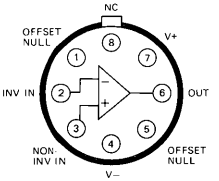
Package FE, N

FET input op amp

NE/SU536

Temperature range:
Military −55 °C to 85 °C SU536T
Commercial 0 °C to 70 °C NE536T

- Input bias current 5 pA at 20 °C
- Slew rate 6 V/μs
- Input impedance $10^{14}\ \Omega$
- Internally compensated



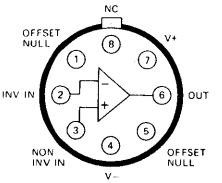
Package T

High slew rate op amp

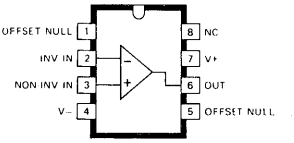
NE/SE538

Temperature range:
Military −55 °C to 125 °C SE530FE, N, T
Commercial 0 °C to 70 °C NE538FE, N,T

- 2 mV max input offset voltage
- 60 nA max input offset current
- Short-circuit protected
- 60 V/μs slew rate
- 6 MHz gain bandwidth



Package T



Package FE, N

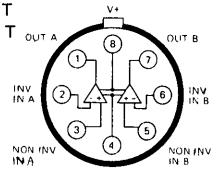
operational amplifiers

abridged data

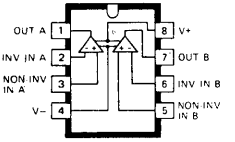
Dual high slew rate op amp

NE/SE5530

Temperature range:
Military −55 °C to 125 °C SE5530FE, N, T
Commercial 0 °C to 70 °C NE5530FE, N, T



Package FE, N



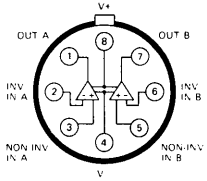
Package N

Dual low noise op amp

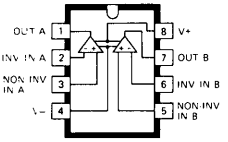
NE/SE5533

Temperature range:
Military −55 °C to 125 °C SE5533F, FE, N, T
Commercial 0 °C to 70 °C NE5533F, FE, N, T

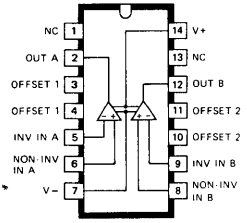
- Small signal bandwidth 10 MHz
- Output drive 10 V(r.m.s.) into 600 Ω
- Input noise 4 nV/√Hz
- Slew rate 13 V/μs



Package T



Package FE, N



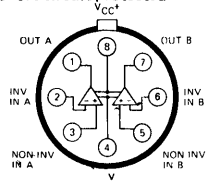
Package F, N-14

Dual high slew rate op amp

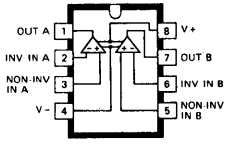
NE/SE5535

Temperature range:
Military −55 °C to 125 °C SE5535F, FE, N, T
Commercial 0 °C to 70 °C NE5535F, FE, N, T

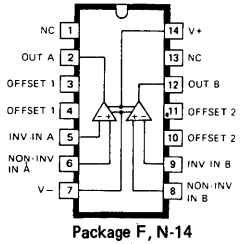
- 15 V/μs slew rate at unity gain
- Input offset voltage 2 mV (typ)
- Large common mode and differential voltage ranges
- Short-circuit protected



Package T



Package FE, N



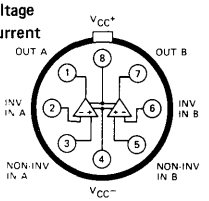
Package F, N-14

Dual high slew rate op amp

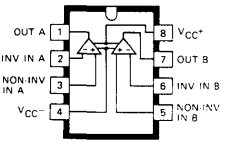
NE/SE5538

Temperature range:
Military −55 °C to 125 °C SE5538F, FE, N, T
Commercial 0 °C to 70 °C NE5538F, FE, N, T

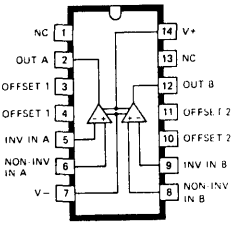
- 2 mV max input offset voltage
- 60 nA max input offset current
- Short-circuit protected
- 60 V/μs slew rate
- 6 MHz gain bandwidth



Package T



Package FE, N



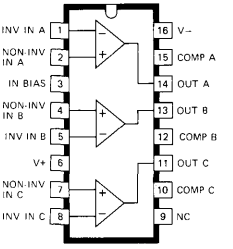
Package F, N-14

Triple op amp

TCA220

Temperature range:
Commercial 0 °C to 70 °C TCA220

- Input offset voltage 2 mV(typ)
- Input offset current 200 nA(typ)
- Channel separation 100 dB(typ)
- CMRR 90 dB(typ)



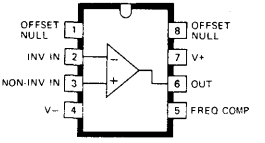
Package N-16

General purpose op amp

TCA520

Temperature range:
Commercial −25 °C to 70 °C TCA520B

- Supply voltage range 2 to 20 V
- Output TTL compatible
- Slew rate 50 V/μs
- Input offset voltage 2 nV(typ)
- Input offset current 30 nA(typ)



Package FE, N

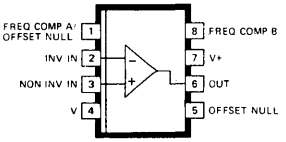
operational amplifiers

abridged data

High performance op amp — TDA0301

Temperature range:
Commercial 0 °C to 70 °C TDA0301D

- Typical gain 160 000
- Input offset current, typically 3,0 nA
- Input offset voltage, typically 2 mV

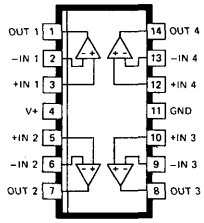


Package SO-8

Quad op amp — TDA0324

Temperature range:
Commercial 0 °C to 70 °C TDA0324D

- Internally compensated
- Operation down to 3 V supply
- Low power supply current 200 μA per amplifier

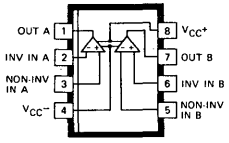


Package SO-14

Dual low power op amp — TDA0358

Temperature range:
Commercial 0 °C to 70 °C TDA0358D

- Internally compensated
- Operation down to 3 V supply
- Supply current typically 200 μA per amplifier

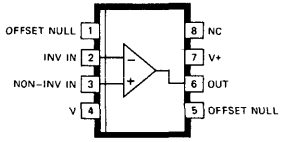


Package SO-8

General purpose op amp — TDA0741

Temperature range:
Commercial 0 °C to 70 °C TDA0741D

- Typical open loop gain 200 000
- Offset null capability
- Output impedance 75 Ω typical



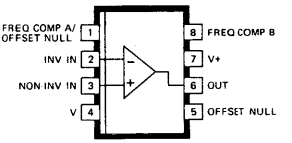
Package SO-8

General purpose op amp

TDA0748

Temperature range:
Commercial 0 °C to 70 °C TDA0748D

- Typical open loop gain 200 000
- Uncompensated
- Offset null capability
- Output impedance 75 Ω



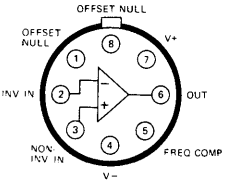
Package SO-8

High performance op amp

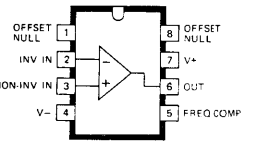
TDA1034
NE/SE5534

Temperature range:
Military −55 °C to 125 °C SE5534FE, N, T
Industrial −25 °C to 85 °C TDA1034FE, N, T
Commercial 0 °C to 70 °C SE5534FE, N, T

- Input noise voltage 3,5 nV/$\sqrt{\text{Hz}}$(typ)
- Input noise current 0,4 pA/$\sqrt{\text{Hz}}$(typ)
- Input offset voltage 0,5 mV(typ)
- Input offset current 20 nA(typ)
- Slew rate 13 V/ns
- Small signal bandwidth 10 MHz



Package T



Package FE, N

Power bandwidth	
at $V_{OUT(p-p)}$ = 20 V	typ 200 kHz
Noise voltage at 1 kHz	3,5 nV/$\sqrt{\text{Hz}}$
at 30 Hz	5,5 nV/$\sqrt{\text{Hz}}$

operational amplifiers

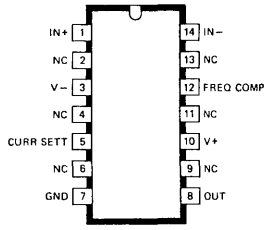
abridged data

High slew rate op amp

TDA1078
NE5539

Temperature range:
Commercial 0 °C to 70 °C TDA1078, NE5539N

- High open loop gain
- High slew rate
- High bandwidth
- High output current
- Not compensated
- Power response 64 MHz



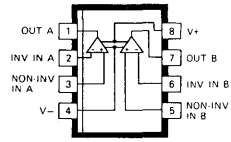
Package N-14

Dual general purpose op amp

TDA1458

Temperature range:
Commercial 0 °C to 70 °C TDA1458D

- Typical gain 100 000
- Internally compensated
- Unity gain slew rate 0,8 V/μs



Package SO-8

differential amplifiers

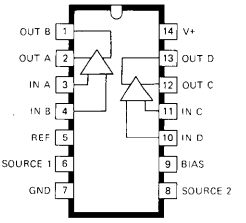
abridged data

Dual differential amplifier

NE/SE510

Temperature range:
Military −55 °C to 125 °C SE510F, N
Commercial 0 °C to 70 °C NE510N

- Low input offset voltage −0,5 mV typical
- Bandwidth greater than 100 MHz
- AGC capability



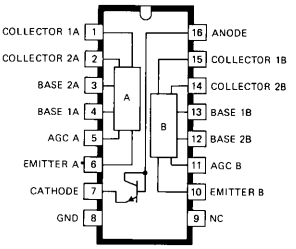
Package F, N-14

Dual differential transistor pair

NE/SE511

Temperature range:
Military −55 °C to 125 °C SE511F, N
Commercial 0 °C to 70 °C NE511F, N

- Low input offset voltage −0,5 mV typical
- Operation up to 100 MHz
- AGC capability



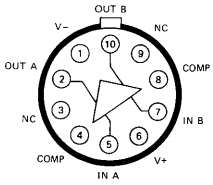
Package F, N-14

Differential amplifier

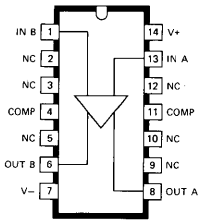
NE/SE515

Temperature range:
Military −55 °C to 125 °C SE515K, N
Commercial 0 °C to 70 °C NE515K, N

- Differential inputs and outputs
- Open loop gain 4,500 (typ)
- Bandwidth (open loop) 1 MHz
- Input offset voltage typical 0,5 mV



Package K



Package N-14

comparators

selection guide

device no.	complexity	temp. range	max inp. offset volt. mV	max inp. current bias μA	max inp. current offset μA	supply voltage V	response time (typ) ns	common mode voltage range V
μA710	single	military	3,00	45,0	7,00	+12, −6	40	± 5
μA710C	single	commercial	6,50	40,0	7,50	+12, −6	40	± 5
LM111	single	military	4,00	0,15	0,02	± 15	200	± 14
LM211	single	industrial	4,00	0,15	0,02	to	200	± 14
LM311	single	commercial	10,0	0,30	0,07	+5 and GND	200	± 14
NE526	single	commercial	5,00	35,0	5,00	+5, −5	40	−3,2, +4,2
SE526	single	military	5,00	35,0	5,00	+5, −5	40	−3,2, +4,2
NE527	single	commercial	10,0	4,00	1,00	± 5 to ± 15	16	± 6
SE527	single	military	6,00	4,00	1,00	and GND	16	± 6
NE529	single	commercial	10,0	50,0	15,0	± 5 to ± 15	12	± 6
SE529	single	military	6,00	36,0	9,00	and GND	12	± 6
LM119	dual	military	7,00	1,00	0,10	± 15	80	± 13
LM219	dual	industrial	7,00	1,00	0,10	to	80	± 13
LM319	dual	commercial	10,0	1,20	0,30	+5 and GND	80	± 13
LM193	dual	military	9,00	0,30	0,10	± 1 to ± 18	1300	± 18
LM293	dual	industrial	9,00	0,40	0,15	or	1300	± 18
LM393	dual	commercial	9,00	0,40	0,15	+2 to +36 GND	1300	± 18
LM2903	dual	ext. ind.	15,0	0,50	0,20		1300	± 18
NE521	dual	commercial	10,0	40,0	12,0	+5, −5, GND	4,5	± 3
NE522	dual	commercial	10,0	40,0	12,0	+5, −5, GND	6	± 3
μA711	dual	military	6,00	150	20,0	+12, −6	40	± 5
μA711C	dual	commercial	10,0	150	25,0	+12, −6	40	± 5
TDA0319	dual	commercial	10,0	1,20	0,30	+5 and GND	80	± 13
LM139	quad	military	9,00	0,30	0,10		1300	V_S-2
LM239	quad	industrial	9,00	0,40	0,15	± 1 to ± 18 or	1300	V_S-2
LM339	quad	commercial	9,00	0,40	0,15	+2 to +36	1300	V_S-2
LM2901	quad	ext. ind.	15,0	0,50	0,20		1300	V_S-2
LM139A	quad	military	4,00	0,30	0,10	+2 to +36	1300	V_S-2
LM239A	quad	industrial	4,00	0,40	0,15	and GND	1300	V_S-2
LM339A	quad	commercial	4,00	0,40	0,15		1300	V_S-2
MC3302	quad	ext. ind.	40,0	1,00	0,20	+2 to +28 GND	2000	V_S-2

output voltage		output	voltage	TTL	max diff.	packages	comments	page
V_{OLmax} V	V_{OHmin} V	structure	gain (typ) V/mV	fan out	inp. voltage V			
0	2,5	TTL	1,7	1	± 5	F, T	differential input	B47
0	2,5	TTL	1,5	1	± 5	F, FE, N N-14, T	single ended output	
0,4	V_S	open coll.	200	5	± 30	F,T	with strobe; will operate from	
0,4	V_S	open coll.	200	5	± 30	F, FE, N	single supply	B46
0,4	V_S	open coll.	200	5	± 30	N-14, T		
0,4	2,8	TTL		10	5	F, K, N-14	plus TTL output gate	B49
0,4	2,8	TTL		10	5	F, K, N-14		
0,5	2,7	TTL	5	5	± 5	K, N-14	complementary output	B49
0,5	2,5	TTL	5	5	± 5	K	gates with individual strobes	
0,5	2,7	TTL	5	5	± 5	K, N-14	complementary output	B50
0,5	2,5	TTL	5	5	± 5	K	gates with individual strobes	
0,6	V_S	open coll.	40	2	± 5	F, K	will operate from single	
0,6	V_S	open coll.	40	2	± 5	F, K	or dual supplies	B46
0,6	V_S	open coll.	40	2	± 5	F, K, N-14		
0,7	V_S	open coll.	200	2	36	T	will operate from single	
0,7	V_S	open coll.	200	2	36	FE, N, T	or dual supplies	
0,7	V_S	open coll.	200	2	36	FE, N, T		B47
0,7	V_S	open coll.	100	2	36	FE, N		
0,5	2,7	TTL	5	12	± 6	F, N-14	ultra-high speed	B48
0,5	V_S	open coll.	5	12	± 6	F, N-14		B49
0	2,5	TTL	1,5	2	± 5	F, K, N-14	differential in, common out,	B48
0	2,5	TTL	1,5	2	± 5	F, K, N-14	individual strobes	
0,6	V_S	open coll.	40	2	± 5	SO-10		B50
0,7	V_S	open coll.	200	2	36	F		
0,7	V_S	open coll.	200	2	36	F, N-14	will operate from single	B46
0,7	V_S	open coll.	200	2	36	F, N-14	or dual supplies	
0,7	V_S	open coll.	100	2	36	F, N-14		
0,7	V_S	open coll.	200	2	36	F	will operate from single	
0,7	V_S	open coll.	200	2	36	F, N-14	or dual supplies	B47
0,7	V_S	open coll.	200	2	36	F, N-14		
0,4	V_S	open coll.	30	2	28	N-14	will operate from single or dual supplies	B48

comparators

abridged data

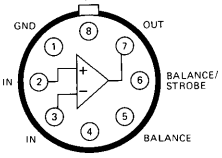
Precision voltage comparator

LM111/211/311

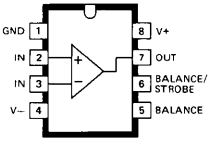
Temperature range:

Military	−55 °C to 125 °C	LM111F, T
Industrial	−25 °C to 85 °C	LM211F, FE, N, T
Commercial	0 °C to 70 °C	LM311F, FE, N, T

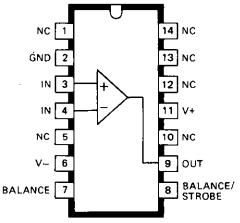
- Operates from single 5 V supply
- Voltage gain 200 000 typical
- Input bias current
  Military 60 nA
  Industrial 100 nA
  typical



Package T



Package FE, N



Package F, N-14

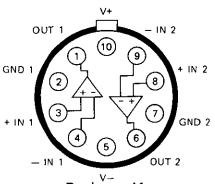
Dual voltage comparator

LM119/219/319

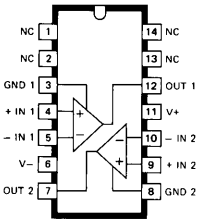
Temperature range:

Military	−55 °C to 125 °C	LM119F, K
Industrial	−25 °C to 85 °C	LM219F, K
Commercial	0 °C to 70 °C	LM319F, K, N

- Operates from single supply
- Output can be level shifted
- Input bias current typically 250 nA
- Minimum fan-out 2 each side
- High common mode slew rate
- 8 ns response time (± 15 V)



Package K



Package F, N-14

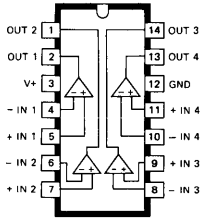
Quad comparator

LM139/239/339/2901

Temperature range:

Military	−55 °C to 125 °C	LM139F
Ext. Ind.	−40 °C to 85 °C	LM2901F, N
Industrial	−25 °C to 85 °C	LM239F, N
Commercial	0 °C to 70 °C	LM339F, N

- Single voltage supply
- Operation down to 2 V
- Offset current 3 nA(typ)
- Offset voltage 5 mV(max)
- Input bias current 35 nA(typ)
- Output TTL compatible



Package F, N-14

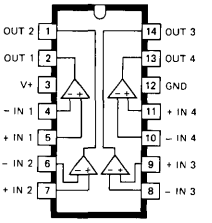
Quad comparator

LM139A/239A/339A

Temperature range:

Military	−55 °C to 125 °C	LM139AF
Industrial	−25 °C to 85 °C	LM239AF, N
Commercial	0 °C to 70 °C	LM339AF, N

- Single voltage supply
- Operation down to 2 V
- Offset current 3 nA(typ)
- Offset voltage 2 mV(max)
- Input bias current 35 nA(typ)
- Output TTL compatible



Package F, N-14

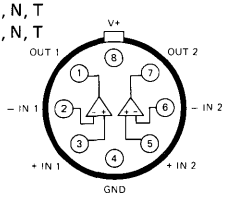
Dual comparator

LM193/293/393/2903

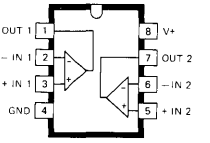
Temperature range:

Military	−55 °C to 125 °C	LM193T
Ext. Ind.	− 40 °C to 85 °C	LM2903FE, N
Industrial	−25 °C to 85 °C	LM293FE, N, T
Commercial	0 °C to 70 °C	LM393FE, N, T

- Single supply voltage
- Operation down to 2 V
- Offset current 3 nA(typ)
- Offset voltage 2 mV(max)
- Input bias current 35 nA(typ)
- Output TTL compatible



Package T



Package FE, N

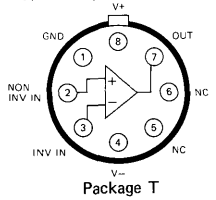
Comparator

μA710/710C

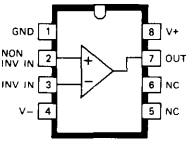
Temperature range:

Military	−55 °C to 125 °C	μA710F, T
Commercial	0 °C to 70 °C	μA710CF, FE, N, T

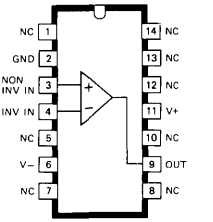
- Typical gain 1700
- Offset voltage temperature coefficient, 3,5 μV/ °C
- Typical response time 40 ns



Package T



Package FE, N



Package F, N-14

comparators

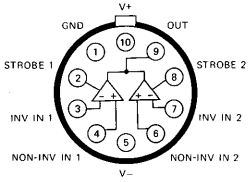
abridged data

Dual comparator

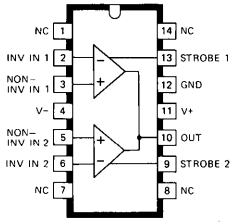
μA711/711C

Temperature range:
Military −55 °C to 125 °C μA711F, K, N
Commercial 0 °C to 70 °C μA711CF, K, N

- Typical gain 1700
- Input strobes
- Typical response time, 40 ns



Package K



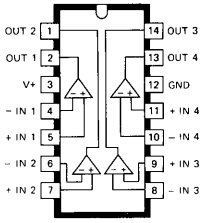
Package F, N-14

Quad voltage comparator

MC3302

Temperature range:
Ext. Ind. −40 °C to 85 °C MC3302N

- TTL compatible
- Differential input voltage ± V_{CC}
- Single supply +2 V to +28 V
- Input common mode voltage to GND
- Low current drain



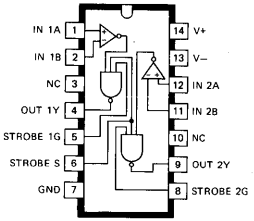
Package N-14

Dual high-speed comparator

NE521

Temperature range:
Commercial 0 °C to 70 °C NE521F, N

- Schottky linear process
- 8 ns typical propagation delay
- Typical offset voltage 6 mV
- Totem-pole outputs



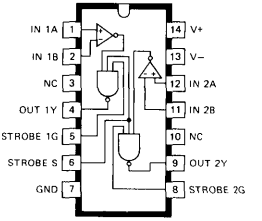
Package F, N-14

Dual high-speed comparator

NE522

Temperature range:
Commercial 0 °C to 70 °C NE522F, N

- Schottky linear process
- 10 ns typical propagation delay
- Typical offset voltage 6 mV
- Open collector outputs



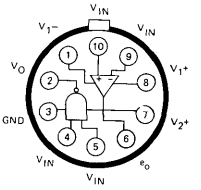
Package F, N-14

Precision voltage comparator

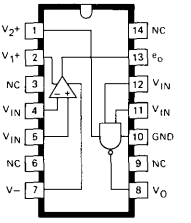
NE/SE526

Temperature range:
Military −55 °C to 125 °C SE526F, K, N
Commercial 0 °C to 75 °C NE526F, K, N

- Typical offset current 0,5 μA
- Typical offset voltage 2 mV
- TTL fan-out of 10



Package K



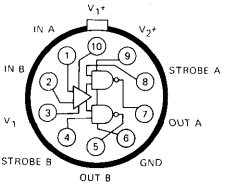
Package F, N-14

High-speed comparator

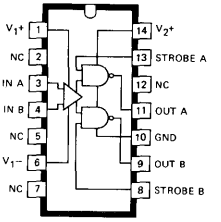
NE/SE527

Temperature range:
Military −55 °C to 125 °C SE527K
Commercial 0 °C to 70 °C NE527K, N

- Low offset current 0,3 μA (typ)
- Low offset voltage, 2 mV (typ)
- Complementary outputs
- Typical propagation delay, 15 ns



Package K



Package N-14

comparators

abridged data

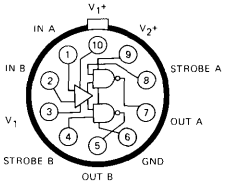
High-speed comparator

NE/SE529

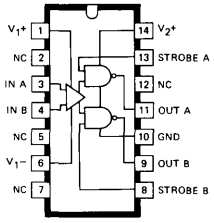
Temperature range:

Military	−55 °C to 125 °C	SE529K
Commercial	0 °C to 70 °C	NE529K, N

- Offset current 2 μA (typ)
- Low offset voltage 2 mV (typ)
- Complementary outputs
- Typical propagation delay 11 ns



Package K



Package N-14

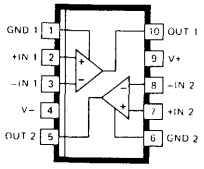
Dual voltage comparator

TDA0319

Temperature range:

Commercial	0 °C to 70 °C	TDA0319D

- Operates from single 5 V supply
- Output can be level shifted
- Input bias current typically 250 nA



Package SO-10

voltage regulators

selection guide

device no.	polarity and function	input voltage range V	output voltage range V	max outp. current A	peak outp. current A	typ line regulation %	typ load regulation %
LM109/309	5 V pos.; fixed	7,0 to 35	4,8 to 5,2	1,0	2,2	1,0	2,0
LM340-5	5 V pos.; fixed	7,0 to 35	4,8 to 5,2				
LM340-6	6 V pos.; fixed	8,0 to 35	5,75 to 6,25				
LM340-8	8 V pos.; fixed	10 to 35	7,7 to 8,3				
LM340-12	12 V pos.; fixed	14 to 35	11,5 to 12,5	1,0	2,2	1,0	1,0
LM340-15	15 V pos.; fixed	17 to 35	14,4 to 15,6				
LM340-18	18 V pos.; fixed	20 to 35	17,3 to 18,7				
LM340-24	24 V pos.; fixed	26 to 40	23 to 25				
NE/SE550	precision adjustable	8,5 to 40	2,0 to 37	0,125	0,150	0,1	0,4
NE/SE5551			± 5				
NE/SE5552			± 6				
NE/SE5553	dual polarity regulators	± 3,2	± 12	–	0,4	–	–
NE/SE5554			± 15				
NE/SE5555			+ 5; –12				
μA723/723C	precision adjustable	9,5 to 40	2,0 to 37	0,125	0,150	0,1	0,6
7805	5 V pos.; fixed	7,0 to 35	4,8 to 5,2		2,2		
7806	6 V pos.; fixed	8,0 to 35	5,75 to 6,25		2,2		
7808	8 V pos.; fixed	10 to 35	7,7 to 8,3		2,2		
7812	12 V pos.; fixed	14 to 35	11,5 to 12,5	1,0	2,2	1,0	1,0
7815	15 V pos.; fixed	17 to 35	14,4 to 15,6		2,1		
7818	18 V pos.; fixed	20 to 35	17,3 to 18,7		2,1		
7824	24 V pos.; fixed	26 to 40	23 to 25		2,1		
78G *	pos.; adjustable	7,5 to 40	5,0 to 30	1,0	2,1	0,75	1,0
78L02AC	2,6 V pos.; fixed	4,3 to 30	2,5 to 2,7				
78L05AC	5 V pos.; fixed	6,7 to 30	4,8 to 5,2	0,15		2,0	1,0
78L06AC	6,2 V pos.; fixed	7,9 to 30	5,95 to 6,45				
78L08AC *	8,2 V pos.; fixed	9,9 to 30	7,9 to 8,5				

* Type in development.

For special voltage requirements contact us – see back cover for address

typ quiesc. current mA	min ripple rejection dB	min dropout voltage V	av temp. coefficient mV/°C	packages with corresponding max θ	$\theta_{j\text{-}c}$ °C/W	$\theta_{j\text{-}a}$		$\theta_{j\text{-}c}$ °C/W	$\theta_{j\text{-}a}$	page
5,0		2,0	–0,8	TO-220	5,0	65	TO-3	5,5	45	B56
4,2	62		–1,1							
4,3	59		–0,8							
4,3	56		–0,8							
4,3	61	2,0	–1,0	TO-220	5,0	65	TO-3	5,5	45	B56
4,4	60		–1,0							
4,5	59		–1,0							
4,6	56		–1,5							
1,6	75	3,0	–0,015	TO-100	25	150	TO-116	65	150	B56
+1,7; –5,6	–	–	1	N	25	150	T	35	95	B57
2,3	74	3,0	–0,015	TO-100	25	150	TO-116	65	150	B56
4,2	62		–1,1							
4,3	59		–0,8							
4,3	56		–0,8							
4,3	61	2,0	–1,0	TO-220	5,0	65	TO-3	5,5	45	B59
4,4	60		–1,0							
4,5	59		–1,0							
4,6	56		–1,5							
3,2	62	2,5	–1,1	U1	11	80	TO-3	6,0	47	B57
3,6	43									
3,8	41	1,7		TO-39	40	190	TO-92	70	200	B57
3,9	39									
4,0	38									

voltage regulators

selection guide

device no.	polarity and function	input voltage range V	output voltage range V	max outp. current A	peak outp. current A	typ line regulation %	typ load regulation %
78L12AC	12 V pos.; fixed	13,7 to 35	11,5 to 12,5				
78L15AC	15 V pos.; fixed	16,7 to 35	14,4 to 15,6	0,15		2,0	1,0
78L18AC *	18 V pos.; fixed	19,7 to 35	17,3 to 18,9				
78L24AC	24 V pos.; fixed	25,7 to 35	23,1 to 14,9				
78M05	5 V pos.; fixed	7,0 to 30	4,8 to 5,2				
78M06	6 V pos.; fixed	8,0 to 30	5,75 to 6,25				
78M08	8 V pos.; fixed	10 to 30	7,7 to 8,3				
78M12	12 V pos.; fixed	14 to 35	11,5 to 12,5	0,5	0,7	1,0	1,0
78M15	15 V pos.; fixed	17 to 35	14,4 to 15,6				
78M20	20 V pos.; fixed	22 to 40	19 to 21				
78M24	24 V pos.; fixed	26 to 40	23 to 25				
78MG	pos.; adjustable	7,5 to 40	5,0 to 30	0,5	0,8	0,75	1,0
7905	5 V neg.; fixed	−7,2 to −35	−4,8 to −5,2				
7906	6 V neg.; fixed	−8,3 to −35	−5,75 to −6,25				
7908	8 V neg.; fixed	−10,3 to −35	−7,7 to −8,3				
7912	12 V neg.; fixed	−14,5 to −35	−11,5 to −12,5	1,0	2,1	1,0	1,0
7915	15 V neg.; fixed	−17,6 to −35	−14,4 to −15,6				
7918	18 V neg.; fixed	−20,7 to −35	−17,3 to −18,7				
7924	24 V neg.; fixed	−27 to −40	−23 to −25				
79G	neg.; adjustable	−7,0 to −40	−2,23 to −30	1,0	2,2	1,0	1,0
79M05	5 V neg.; fixed	−7,5 to −35	−5,2 to −4,8				
79M06	6 V neg.; fixed	−7,35 to −35	−6,25 to −5,75				
79M08	8 V neg.; fixed	−9,4 to −35	−8,3 to −7,7				
79M12	12 V neg.; fixed	−13,6 to −35	−12,5 to −11,5	0,5	0,65	1,0	1,0
79M15	15 V neg.; fixed	−16,7 to −35	−15,6 to −14,4				
79M20	20 V neg.; fixed	−22,1 to −40	−20 to −19				
79M24	24 V neg.; fixed	−26,1 to −40	−25 to −23				
79MG	neg.; adjustable	−7,0 to −40	−2,2 to −30	0,5	0,65	0,75	1,0
TDA0723	precision adjustable	9,5 to 40	2,0 to 37	0,125	0,150	0,1	0,6

* Type in development.

For special voltage requirements contact us – see back cover for address

typ quiesc. current mA	min ripple rejection dB	min dropout voltage V	av temp. coefficient mV/°C	packages with corresponding max θ	$\theta_{j\text{-}c}$ °C/W	$\theta_{j\text{-}a}$ °C/W		$\theta_{j\text{-}c}$ °C/W	$\theta_{j\text{-}a}$ °C/W	page
4,2 4,4 4,6 4,8	36 33	1,7		TO-39	40	190	TO-92	70	200	B57
4,2	62		−1,0							
4,3	59		−0,5							
4,3	56		−0,5							
4,3	55	2,0	−1,0	TO-220	5,0	70	TO-39	25	185	B57
4,4	54		−1,0							
4,5	53		−1,1							
4,6	50		−1,2							
2,8	78	2,5	−0,5	TO-39	25	185	U1	11	80	B58
			−0,4							
			−0,4							
			−0,6							
1,0	54	2,0	−0,8	TO-3	5,5	45	TO-220	5,0	65	B59
			−1,0							
			−1,0							
			−1,0							
0,5	50	2,3	−0,4	U1	11	80	TO-3	6,0	47	B58
	60		−0,4							
	60		−0,4							
	60		−0,6							
1,0	60	1,0	−0,8	TO-220	5,0	70	TO-39	25	185	B58
	60		−1,0							
	59		−1,0							
	58		−1,0							
0,5	60	2,3	−0,4	TO-39	25	185	U1	11	80	B59
2,3	74	3,0	−0,015	SO-10						B59

voltage regulators

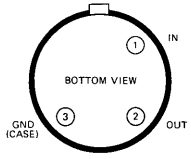
abridged data

Fixed 5 volt regulator — LM109/209/309

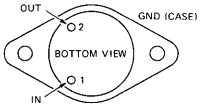
Temperature range:

Military	−55 °C to 125 °C	LM109DA, DB
Industrial	−25 °C to 85 °C	LM209DA, DB
Commercial	0 °C to 70 °C	LM309DA, DB

- Fixed 5 V output
- Short-circuit and thermal overload protection
- 1 A capability in TO-3



Package DB



Package DA

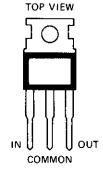
Fixed positive voltage regulators — LM340 series

Temperature range (junction):

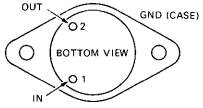
Military	−55 °C to 125 °C	LM340DA
Commercial	0 °C to 125 °C	LM340DA, U

- 1 A output
- Short-circuit and overload protection

LM340-5	5 V
LM340-6	6 V
LM340-8	8 V
LM340-12	12 V
LM340-15	15 V
LM340-18	18 V
LM340-24	24 V



Package U



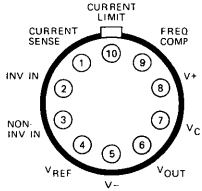
Package DA

Variable voltage regulator — μA723/723C

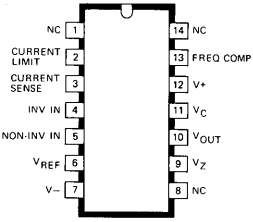
Temperature range:

Military	−55 °C to 125 °C	μA723F, K, N
Commercial	0 °C to 70 °C	μA723CK, N

- Output voltage range, 2 to 37 V
- 150 mA output current capability
- 7,15 V reference



Package K



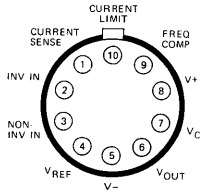
Package F, N-14

Variable voltage regulator — NE/SE550

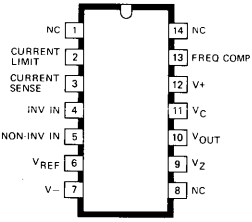
Temperature range:

Military	−55 °C to 125 °C	SE550F, K
Commercial	0 °C to 70 °C	NE550F, K, N

- Output voltage range, 2 to 37 V
- 150 mA output current capability
- 1,63 V reference



Package K



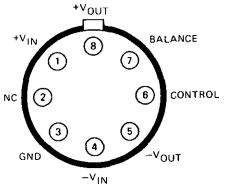
Package F, N-14

Dual polarity regulators — NE/SE5551 to 55

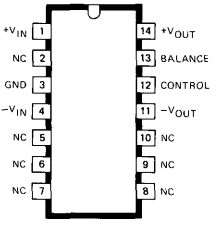
Temperature range:

Military	−55 °C to 155 °C	SE5551 to 55F, N, T
Commercial	0 °C to 150 °C	NE5551 to 55F, N, T

- Internally current-limited
- Thermal overload protection
- Continuously adjustable from 5 to 20 V, balanced or unbalanced
- No external components required



Package T



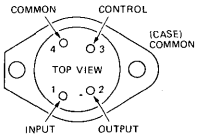
Package F, N-14

Adjustable positive voltage regulator — 78G

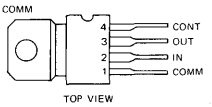
Temperature range (junction):

Military	−55 °C to 150 °C	78G, DA
Commercial	0 °C to 150 °C	78GC, DA, U1

- Output current in excess of 1,0 A
- 78G positive output voltage 5 to 30 V
- Internal thermal overload protection
- Internal short-circuit current protection
- Output transistor safe area protection
- Military and commercial versions available
- Available in 4-pin TO-202 type and 4-pin TO-3



Package DA



Package U1

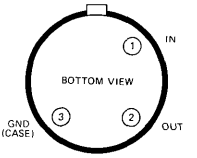
Fixed positive voltage regulators — 78L00 series

Temperature range (junction):

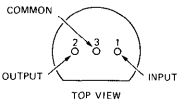
Military	−55 °C to 150 °C	78L00DB
Commercial	0 °C to 150 °C	78L00CS, DB

- 0,1 A output
- Short-circuit and overload protection

78L02	2,6 V	78L12	12 V
78L05	5 V	78L15	15 V
78L06	6,2 V	78L18	18 V
78L08	8,2 V	78L24	24 V



Package DB



Package S

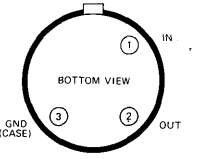
Fixed positive voltage regulators — 78M00 series

Temperature range (junction):

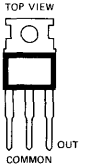
Military	−55 °C to 150 °C	78M00DB
Commercial	0 °C to 150 °C	78M00C, DB, U

- 0,5 A output
- Short-circuit and overload protection

78M05 5 V
78M06 6 V
78M08 8 V
78M12 12 V
78M15 15 V
78M20 20 V
78M24 24 V



Package DB



Package U

voltage regulators

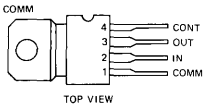
abridged data

Adjustable positive voltage regulator — 78MG

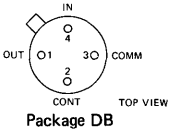
Temperature range (junction):

Military	−55 °C to	150 °C	78MGDB
Commercial	0 °C to	150 °C	78GCDB, U1

- Output current in excess of 0,5 A
- μA78MG positive output voltage 5 to 30 V
- Internal thermal overload protection
- Internal short-circuit current protection
- Output transistor safe area protection
- Power miniature dual in-line package



Package U1



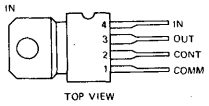
Package DB

Adjustable negative voltage regulator — 79G

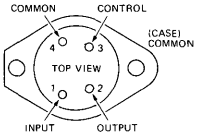
Temperature range (junction):

Military	−55 °C to	150 °C	79GDA
Commercial	0 °C to	150 °C	79GCDA, U1

- Output current in excess of 1,0 A
- 79G negative output voltage −30 to −5 V
- Internal thermal overload protection
- Internal short-circuit current protection
- Output transistor safe area protection
- Military and commercial versions available
- Available in 4-pin TO-202 type and 4-pin TO-3



Package U1



Package DA

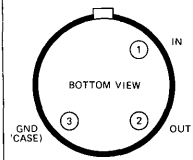
Fixed negative voltage regulators — 79M00 series

Temperature range (junction):

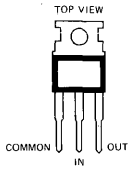
Military	−55 °C to	150 °C	79M00DB
Commercial	0 °C to	150 °C	79M00CDB, U

- 0,5 A output
- Short-circuit and overload protection

79M05	5 V
79M06	6 V
79M08	8 V
79M12	12 V
79M15	15 V
79M20	20 V
79M24	24 V



Package DB



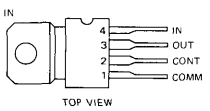
Package U

Adjustable negative voltage regulator — 79MG

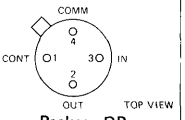
Temperature range (junction):

Military	−55 °C to 150 °C	79MGDB
Commercial	0 °C to 150 °C	79MGCDB, U1

- Output current in excess of 0,5 A
- 79MG negative output voltage −30 V to −2,2 V
- Internal thermal overload protection
- Internal short-circuit current protection
- Output transistor safe area protection
- Power miniature dual in-line package



Package U1



Package DB

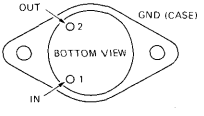
Fixed positive voltage regulators — 7800 series

Temperature range (junction):

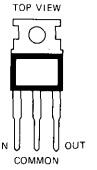
Military	−55 °C to 150 °C	7800DA
Commercial	0 °C to 150 °C	7800CDA, U

- 1 A output
- Short-circuit and overload protection

7805	5 V
7806	6 V
7808	8 V
7812	12 V
7815	15 V
7818	18 V
7824	24 V



Package DA



Package U

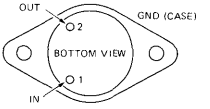
Fixed negative voltage regulators — 7900 series

Temperature range (junction):

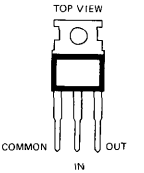
Military	−55 °C to 150 °C	7900DA
Commercial	0 °C to 150 °C	7900CDA, U

- 1 A output
- Short-circuit and overload protection

7905	5 V
7906	6 V
7908	8 V
7912	12 V
7915	15 V
7918	18 V
7924	24 V



Package DA



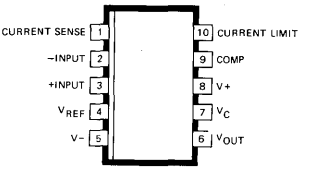
Package U

Variable voltage regulator — TDA0723

Temperature range:

Military	−55 °C to 125 °C	TDA0723D
Commercial	0 °C to 70 °C	TDA0723D

- Output voltage range, 2 to 37 V
- 150 mA output current capability
- 7,15 V reference



Package SO-10

general industrial

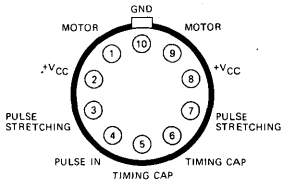
abridged data

Servo amplifier — NE543

Temperature range:
Commercial 0 °C to 70 °C NE543K

- Directly drives 11 Ω servo motor
- Few external components
- Operates from 4,5 V supply

NO LONGER RECOMMENDED
FOR NEW DESIGN

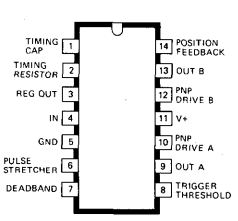


Package K

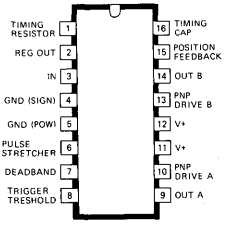
Servo amplifier — NE544

Temperature range:
Industrial −20 °C to 75 °C NE544N

- 500 mA load current capability
- Low stand-by power drain
- Bidirectional bridge output (single supply)
- Adjustable deadband/trigger thresholds
- High linearity 0,5% max error
- Output for external PNPs optional
- Wide supply range



Package N-14

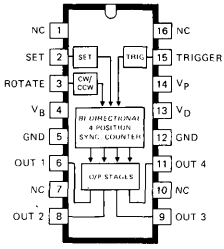


Package N-16

Stepper motor driver — SAA1027

Temperature range:
Industrial −20 °C to 70 °C SAA1027

- Supply range 9,5 to 18 V
- Load current (each output) 350 mA(max)
- Logic on chip for clockwise/counterclockwise rotation

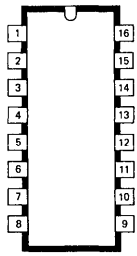


Package N-16

Industrial logic circuit — SAA1029

Temperature range:
Industrial −30 °C to 85 °C SAA1029N

- High noise immunity
- High max input voltage
- High voltage process
- Short-circuit protected

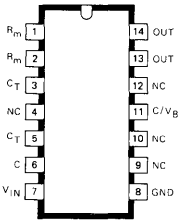


Package N-16

Revolution counter — SAA1049

Temperature range:
Ext. Ind. −40 °C to 85 °C SAA1049N

- Temperature compensation
- Supply voltage compensation
- Positive triggering
- Adjustable output pulse duration

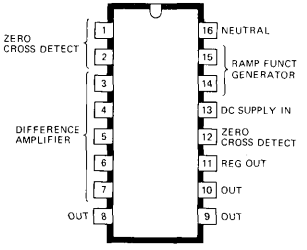


Package N-14

Universal triac control — TCA280A

Temperature range:
Industrial −20 °C to 80 °C TCA280A

- Universal triac control
- Zero crossing
- Trigger current 200 mA(max)
- Supply current 30 mA(max)

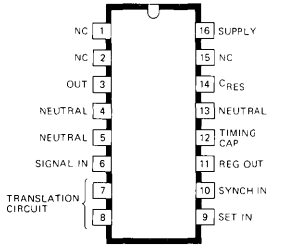


Package N-16

Time proportional triac control — TDA1023

Temperature range:
Industrial −20 °C to 80 °C TDA1023

- Adjustable hysteresis
- Fail safe
- Linear temperature scale
- Trigger current 200 mA(max)
- Supply current less than 30 mA
- Zero crossing

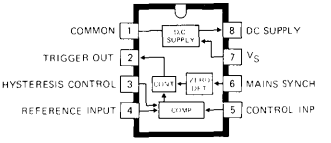


Package N-16

On/off triac control — TDA1024

Temperature range:
Industrial −20 °C to 80 °C TDA1024

- Adjustable hysteresis
- Trigger current capability 100 mA(max)
- Supply current 10 mA(typ)
- Zero crossing



Package N

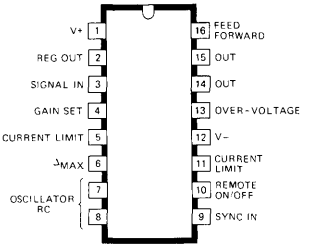
general industrial

abridged data

Switched mode power supply control — TDA1060

Temperature range:
Military −55 °C to 125 °C TDA1060B
Industrial −25 °C to 85 °C TDA1060

- Complete SMPS control
- δ_{max} control
- Slow start
- Current limit control
- Over-current protection
- Over-voltage protection

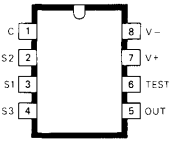


Package F, N-16

Voltage indication circuit — TDA1092

Temperature range:
Industrial −40 °C to 85 °C TDA1092N

- High voltage indication
- Low voltage indication
- Adjustable tresholds
- Temperature compensation
- Spike-protection
- 2 W output capability

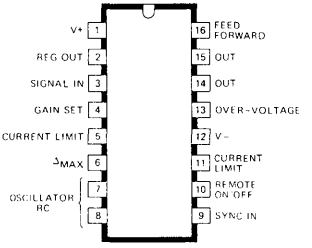


Package N

Switched mode power supply control — TDA3060

Temperature range:
Commercial 0 °C to 70 °C *TDA3060*

- Complete SMPS control
- δ_{max} control
- Slow start
- Current limit control
- Over-current protection
- Over-voltage protection



Package F, N-16

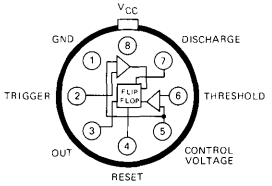
timers
abridged data

Timer

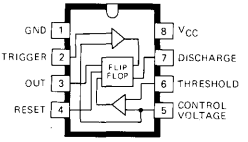
NE555
SE555/555C

Temperature range:
Military −55 °C to 125 °C SE555F, N, T/SE555CF, N, T
Commercial 0 °C to 70 °C NE555T, N

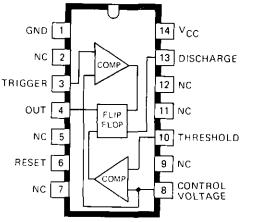
- Timing over 9 decades
- Operates in monostable and astable modes
- 200 mA output current capability
- SE555C is industrial spec maintained over military temperature range



Package T



Package N



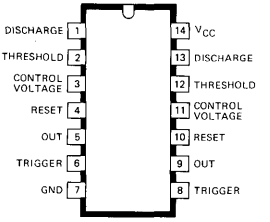
Package F

Dual timer

NE556
SE556/556C

Temperature range:
Military −55 °C to 125 °C SE556F, N/SE556CF, N
Commercial 0 °C to 70 °C NE556N

- Timing over 9 decades
- Operates in monostable and astable modes
- Replaces two 555 timers
- SE556C is industrial spec maintained over military temperature range



Package F, N-14

timers

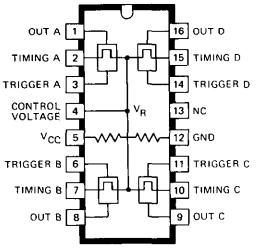
abridged data

Quad timer

NE558

Temperature range:
Commercial 0 °C to 70 °C NE558N

- TTL compatible inputs and outputs
- All four monostables independently adjustable
- 100 mA output sink capability



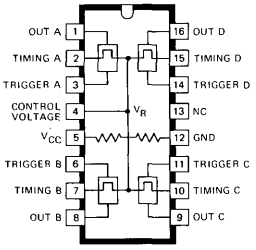
Package N-16

Quad timer

NE559

Temperature range:
Commercial 0 °C to 70 °C NE559N

- TTL compatible inputs
- 100 mA output source capability
- All four monostables independently adjustable



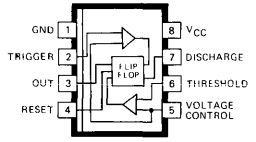
Package N-16

Timer

TDA0555

Temperature range:
Commercial 0 °C to 70 °C TDA0555D

- Timing over 9 decades
- Operates in monostable and astable modes
- 200 mA output current capability



Package SO-8

interface

selection guide

Peripheral interface

Peripheral drivers (TTL compatible)

device no.	function	switching speed ns	output voltage V	comments	packages	page
75450B	NAND	30	30	separate output transistor	F, N-14	B75
75451B	NAND	25	30	output transistor is internally connected	F, N, T	B76-B77
75452B	AND	35				
75453B	NOR	25				
75454B	OR	35				
DS3611	AND	130	80	inputs compatible with TTL and MOS	N	B69-B70
DS3612	NAND	110				
DS3613	OR	125				
DS3614	NOR	220				
UDN5711	AND	750	80	all devices have suppression diodes on output	N	B74
UDN5712	NAND					
UDN5713	OR					
UDN5714	NOR					
NE590		100		sink current	F, N-16	B72
NE591		70		source current	F, N-18	

Line receivers (TTL compatible)

device no.	complexity	supply voltage V	common mode voltage V	propag. delay ns	diff. input	output enable	packages	page
MC1489 **MC1489A**	quad	+ 10		85	no	no	F, N-14	B71
75S107 **75S108**	dual	± 5	± 3	17	yes	yes	F, N-14	B75
DS7820	dual	± 5	± 15	40	yes	yes	F	B69
DS8820							F, N-14	
DS7820A							F	
DS8820A							F, N-14	

interface

selection guide

Peripheral interface

Data conversion products

device	function	temperature range	number of bits	settling time typ	accuracy	packages	page
MC1408-8 **MC1508-8**	DAC	commercial military	8	300 ns	± 0,19%	F, N-16	B71
NE5007 **NE5008** **SE5008**	DAC	commercial commercial military	8	100 ns	0,39% 0,19% 0,19%	F, N-16	B73
NE5009 **SE5009**	DAC	commercial military	8	60 ns	± 0,1%	F, N-16 F	B73
NE5018 **SE5018**	ADC	commercial military	8	2 µs	± 0,19%	F, N-22 F	B73

Video amplifiers

	function	bandwidth	packages	page
NE/SE501	broadband video amplifier	14	K, N-14	B72
NE/SE592	differential input video amplifier	120	F, K, N-14	B72
µA733/733C	differential input video amplifier	120	F, K, N-14	B70

Line drivers (TTL compatible)

device no.	complexity	supply voltage V	V_{OH} V	V_{OL} V	I_{OH} mA	I_{OL} mA	propag. delay ns	packages	page
MC1488	quad	± 9	−7,0	6,8	−12	12	300	F, N-14	B71
DS7830 **DS8830**	dual	+ 5	−3,3	0,5	−40	40	12	F F, N-14	B69

Display drivers

device no.	display	function	input compat.	BCD decoder	ripple blanking	output current mA	output voltage V	comments	packages	page
DS8880 **DS8880-1**	gas disch.	7-segment decoder drivers	TTL	yes	yes	0,2 to 1,5	80 100	constant current output	F, N-16	B80
NE580	bar-graph	driver	—	no	no	1	3,5		F, N-22	B80
NE582	LED	hex universal driver	MOS/TTL	no	no	400	10		F, N-16	B81
NE584-9 **NE584-8**	gas disch.	cath. driver	MOS/TTL	no	no	—	100		**F, N-24** **F, N-22**	B81
NE585-9 **NE585-6**	gas disch.	anode driver	MOS/TTL	no	no	—	100	displays	F, N-22 F, N-16	B82
NE586 **NE588**	LED	fixed current driver	micro-processor	yes	yes	25	0,7 to 3		F, N-16, N-18	B82
NE587 **NE589**	LED	current pro-grammable driver	micro-processor	yes	yes	0 to 15	−0,7 to −3		F, N-16, N-18	B82

Transistor arrays

device no.	function	V_{CBO} V	V_{CEO} V	V_{CEsat} V	I_C mA	current gain	comments	packages	page
CA3045	transistor array	—	—	—	—	—	—	—	B78
CA3046/86	5 transistor array	50	35	0,4	100	350	n-p-n transistors	N-14	B78
CA3081	7 transistor array						common emitter		B78
CA3082	7 transistor array	50	35	0,8	100	300	common collector	N-16	B79
CA3083	5 transistor array						separate transistor		B79
CA3183	transistor array	—	—	—	—	—	—	—	B79
NE5501 **NE5502** **NE5503** **NE5504**	7 n-p-n Darlington pairs	6	100	1,6	350	1000	general purpose use with PMOS with TTL/CMOS PMOS/CMOS	N-16	B83

interface

selection guide

Memory interface

Memory drivers (TTL compatible)

device no.	function	supply voltage	output current mA	t_d max ns	packages	page
55325/75325	memory driver	+14	400	90	F, N-16	B88
75324		+7, +25	600	25	N-14	

Dual memory sense amplifiers (TTL compatible)

device no.	V_{TH} mV	V_{CM} V	output configuration	typ t_{pd} ns	features	packages	page
7520	19	± 3	common collector	20	perform as flip-flops	F, N-16	B84
7521	22						
7522	19	± 3	open collector	20	single ended output	F, N-16	B85
7523	22						
7524	19	± 2,5	common collector	25	separate outputs	F, N-16	B85
7525	22						
7528	19	± 2,5	common collector	25	output available as test points	F, N-16	B86
7529	22						
75232	19	± 2,5	open collector	25	inverted outputs	F, N-16	B86
75233	22						
75234	19	± 2,5	common collector	25	inverted outputs	F, N-16	B87
75235	22						
75S207		± 3	active pull-up	17		F, N-14	B87
75S208			open collector				

peripheral interface

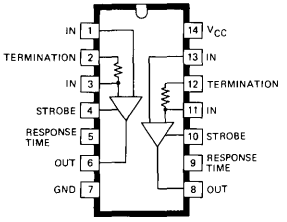
abridged data

Dual line receiver — DS7820/8820

Temperature range:

Military	–55 °C to 125 °C	DS7820F
Commercial	0 °C to 70 °C	DS8820F, N

- Operates from single 5 V supply
- Response time typically 50 ns
- Input voltage range, ± 15 V
- Fan-out of 2 with DTL or TTL



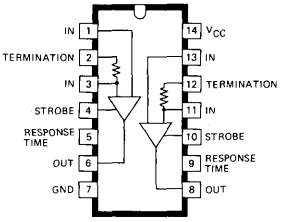
Package F, N-14

Dual line receiver — DS7820A/8820A

Temperature range:

Military	–55 °C to 125 °C	DS7820AF
Commercial	0 °C to 70 °C	DS8820AF, N

- Operates from single 5 V supply
- Response time typically 50 ns
- Input voltage range, ± 15 V
- Fan-out of 10 with DTL or TTL



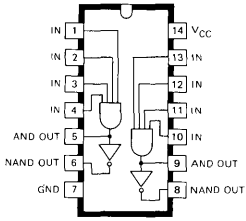
Package F, N-14

Dual differential line driver — DS7830/8830

Temperature range:

Military	–55 °C to 125 °C	DS7830F
Commercial	0 °C to 70 °C	DS8830F, N

- Operates from single 5 V supply
- Short-circuit protected outputs
- Differential propagation delay typically 12 ns



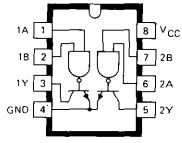
Package F, N-14

Dual AND peripheral driver — DS3611

Temperature range:

Commercial	0 °C to 70 °C	DS3611N

- 300 mA capability per driver
- High voltage output (80 V)
- TTL/DTL compatible
- Input clamping diodes
- Typical delay 125 ns



Package N

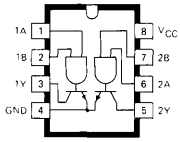
peripheral interface

abridged data

Dual NAND peripheral driver — DS3612

Temperature range:
Commercial 0 °C to 70 °C DS3612N

- 300 mA capability per driver
- High voltage output (80 V)
- TTL/DTL compatible
- Input clamping diodes
- Typical delay 110 ns

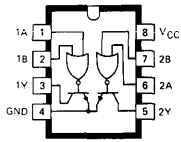


Package N

Dual OR peripheral driver — DS3613

Temperature range:
Commercial 0 °C to 70 °C DS3613N

- 300 mA capability per driver
- High voltage output (80 V)
- TTL/DTL compatible
- Input clamping diodes
- Typical delay 125 ns

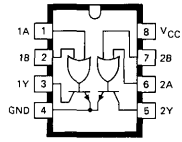


Package N

Dual NOR peripheral driver — DS3614

Temperature range:
Commercial 0 °C to 70 °C DS3614N

- 300 mA capability per driver
- High voltage output (80 V)
- TTL/DTL compatible
- Input clamping diodes
- Typical delay 150 ns

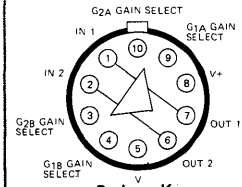


Package N

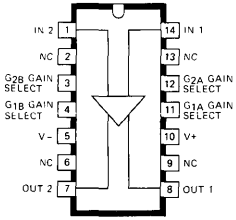
Video amplifier — μA733/733C

Temperature range:
Military −55 °C to 125 °C μA733F, K, N
Commercial 0 °C to 70 °C μA733CF, K, N

- 120 MHz bandwidth
- Gain adjustable from 10 to 400
- No frequency compensation required



Package K

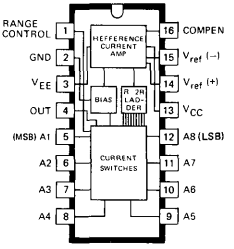


Package F, N-14

8-bit D to A converter — MC1408-8 / MC1508-8

Temperature range:
Military −55 °C to 125 °C MC1508-8F, N
Commercial 0 °C to 70 °C MC1408-8F, N

- Relative accuracy ± 0,19% error(max)
- Settling time 300 ns(typ)
- Non-invert I/P TTL/CMOS compatible
- Output swing +0,5 to −5,0 V
- Multiplying input slew rate 4,0 mA/μs
- Standard supply voltages +5,0 V and −5,0 V to −15 V

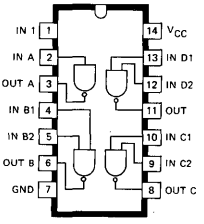


Package F, N-16

Quad line driver — MC1488

Temperature range:
Commercial 0 °C to 70 °C MC1488F, N

- Complies with CCITT recommendation V24
- Current limited output at ± 10 mA typical
- Simple slew rate control
- Typical power dissipation, 440 mW at ± 12 V

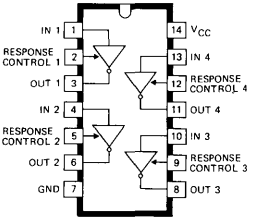


Package F, N-14

Quad line receiver — MC1489

Temperature range:
Commercial 0 °C to 75 °C MC1489F, N

- Complies with CCITT recommendation V24
- 250 mV of input hysteresis
- Typical power dissipation 100 mW

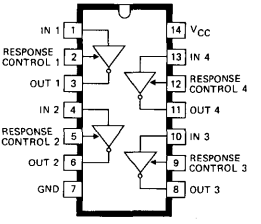


Package F, N-14

Quad line receiver — MC1489A

Temperature range:
Commercial 0 °C to 75 °C MC1489AF, N

- Complies with CCITT recommendation V24
- 1 V of input hysteresis
- Typical power dissipation 100 mW



Package F, N-14

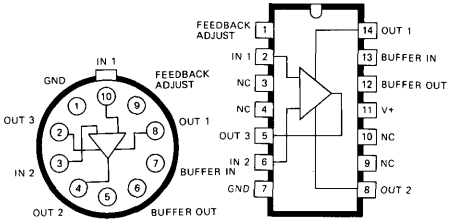
peripheral interface

abridged data

Video amplifier — NE/SE501

Temperature range:
Military −55 °C to 125 °C SE501K, N
Commercial 0 °C to 70 °C NE501K, N

- Adjustable gain and impedance characteristics
- Unity gain frequency 150 MHz
- Typical gain 24 dB
- Bandwidth 14 MHz (−3 dB)

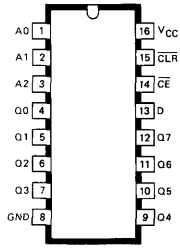


Package K Package N-14

Peripheral driver — NE590

Temperature range:
Commercial 0 °C to 70 °C NE590F, N

- TTL compatible

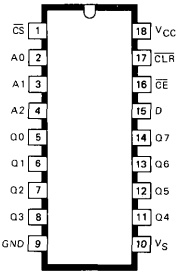


Package F, N-16

Peripheral driver — NE591

Temperature range:
Commercial 0 °C to 70 °C NE591F, N

- TTL compatible

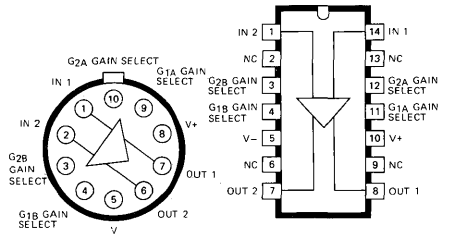


Package F, N-18

Video amplifier — NE/SE592

Temperature range:
Military −55 °C to 125 °C SE592F, K, N
Commercial 0 °C to 70 °C NE592F, K, N

- 120 MHz bandwidth
- Gain adjustable from 0 to 400
- Suitable for high, low or bandpass filters



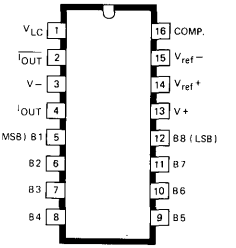
Package K Package F, N-14

8-bit D to A converter

NE5007
NE/SE5008

Temperature range:
Military −55 °C to 125 °C SE5008F, N
Commercial 0 °C to 70 °C NE5007/8F, N

- Fast settling output current 85 ns
- Full scale current pre-matched to ± 1 LSB
- Direct interface to TTL, CMOS, ECL, HTL, PMOS
- Wide power supply range ± 4,5 V to ± 18 V
- Relative accuracy to 0,1% maximum over full temp. range



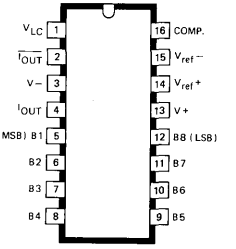
Package F, N-16

8-bit D to A converter

NE/SE5009

Temperature range:
Military −55 °C to 125 °C SE5009F
Commercial 0 °C to 70 °C NE5009F, N

- Fast settling output current −60 ns typ; 135 ns max
- Relative accuracy ± 0,1% max
- Differential non-linearity ± 0,19% max
- Low scale current drift, ± 10 ppm/ °C typ



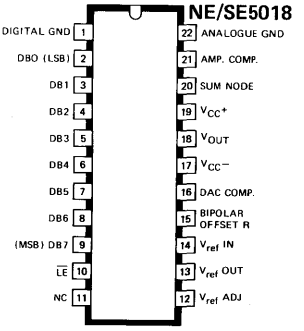
Package F, N-16

8-bit A to D converter

NE/SE5018

Temperature range:
Military −55 °C to 125 °C SE5018F
Commercial 0 °C to 70 °C NE5018F, N

- 8-bit resolution
- Input latches
- Accurate to ± ½ LSB
- Amplifier and reference both short-circuit protected
- Microprocessor compatible



Package F, N-22

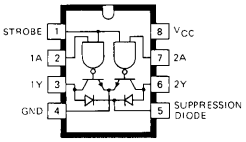
peripheral interface

abridged data

Dual AND peripheral driver — UDN5711

Temperature range:
Commercial 0 °C to 70 °C — UDN5711N

- 300 mA capability per driver
- High voltage output (80 V)
- High voltage PNP inputs
- Output suppression diodes
- Input clamping diodes
- DTL/TTL compatible
- Typical delay 300 ns

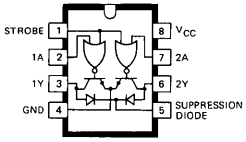


Package N

Dual OR peripheral driver — UDN5713

Temperature range:
Commercial 0 °C to 70 °C — UDN5713N

- 300 mA capability per driver
- High voltage output (80 V)
- High voltage PNP inputs
- Output suppression diodes
- Input clamping diodes
- DTL/TTL compatible
- Typical delay 300 ns

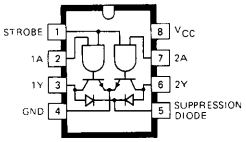


Package N

Dual NAND peripheral driver — UDN5712

Temperature range:
Commercial 0 °C to 70 °C — UDN5712N

- 300 mA capability per driver
- High voltage output (80 V)
- High voltage PNP inputs
- Output suppression diodes
- Input clamping diodes
- DTL/TTL compatible
- Typical delay 300 ns

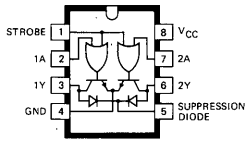


Package N

Dual NOR peripheral driver — UDN5714

Temperature range:
Commercial 0 °C to 70 °C — UDN5714N

- 300 mA capability per driver
- High voltage output (80 V)
- High voltage PNP inputs
- Output suppression diodes
- Input clamping diodes
- DTL/TTL compatible
- Typical delay 300 ns



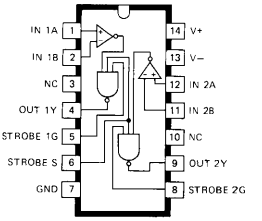
Package N

High-speed line receiver

75S107

Temperature range:
Commercial 0 °C to 70 °C 75S107F, N

- Typical offset voltage 6 mV
- 8 ns typical propagation delay
- Totem-pole outputs



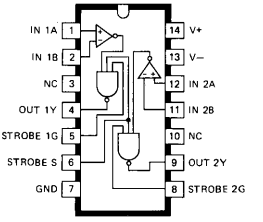
Package F, N-14

High-speed line receiver

75S108

Temperature range:
Commercial 0 °C to 70 °C 75S108F, N

- Typical offset voltage 6 mV
- 10 ns typical propagation delay
- Open-collector outputs



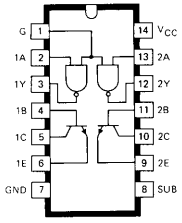
Package F, N-14

Dual peripheral driver

75450B

Temperature range:
Commercial 0 °C to 70 °C 75450BF, N

- Dual NAND function plus uncommitted transistors
- 30 V and 300 mA output rating
- Typical delay 20 ns



Package F, N-14

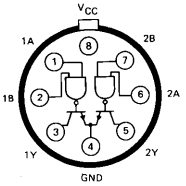
peripheral interface

abridged data

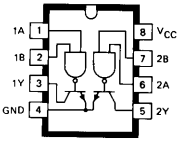
Dual peripheral driver — 75451B

Temperature range:
Commercial 0 °C to 70 °C 75451BF, N, T

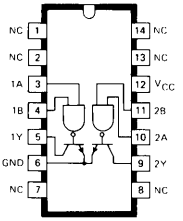
- Dual AND function
- 30 V and 300 mA output rating
- Typical delay 20 ns



Package T



Package N

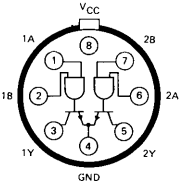


Package F

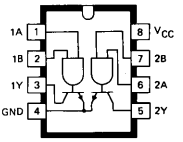
Dual peripheral driver — 75452B

Temperature range:
Commercial 0 °C to 70 °C 75452BF, N, T

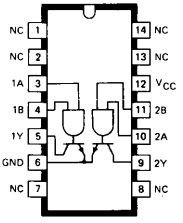
- Dual NAND function
- 30 V and 300 mA output rating
- Typical delay 20 ns



Package T



Package N



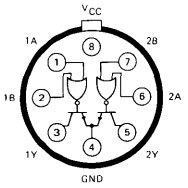
Package F

Dual peripheral driver

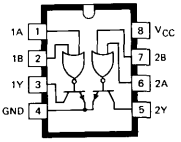
75453B

Temperature range:
Commercial 0 °C to 70 °C 75453BF, N, T

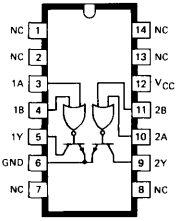
- Dual OR function
- 30 V and 300 mA output rating
- Typical delay 20 ns



Package T



Package N



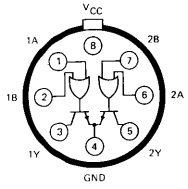
Package F

Dual peripheral driver

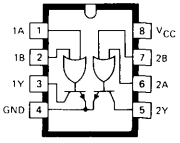
75454B

Temperature range:
Commercial 0 °C to 70 °C 75454BF, N, T

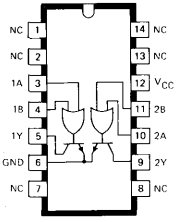
- Dual NOR function
- 30 V and 300 mA output rating
- Typical delay 20 ns



Package T



Package N



Package F

display interface

abridged data

For other transistor array requirements contact us — see back cover for address.

General purpose NPN transistor array

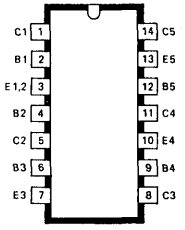
CA3045

General purpose NPN transistor array

CA3046
CA3086

Temperature range:
Military −40 °C to 125 °C CA3046N, CA3086N

- 3 single transistors
- 2 common emitter transistors
- V_{CEO} 35 V
- V_{CBO} 50 V
- V_{EBO} 6 V
- V_{CEsat} 0,4 V



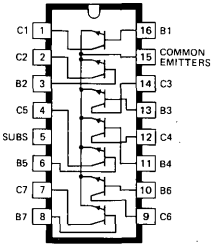
Package N-14

General purpose NPN transistor array

CA3081

Temperature range:
Military −55 °C to 125 °C CA3081N

- Current 100 mA(max)
- V_{CEsat} 0,4 V at 50 mA(typ)
- V_{CEO} 16 V(max)
- V_{CBO} 20 V(max)
- V_{EBO} 5 V(max)
- Common emitter



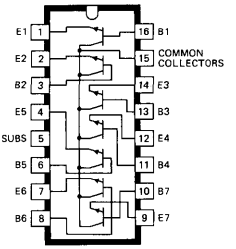
Package N-16

General purpose NPN transistor array

CA3082

Temperature range:
Military −55 °C to 125 °C **CA3082N**

- Current 100 mA(max)
- V_{CEsat} 0,4 V at 50 mA(typ)
- V_{CEO} 16 V(max)
- V_{CBO} 20 V(max)
- V_{EBO} 5 V(max)
- Common collector



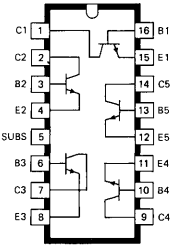
Package N-16

General purpose NPN transistor array

CA3083

Temperature range:
Military −55 °C to 125 °C **CA3083N**

- Current 100 mA(max)
- V_{CEsat} 0,4 V at 50 mA(typ)
- V_{CEO} 16 V(max)
- V_{CBO} 20 V(max)
- V_{EBO} 5 V(max)



Package N-16

General purpose NPN transistor array

CA3183

display interface

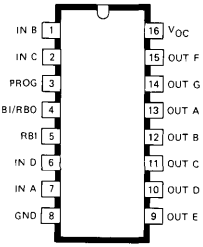
abridged data

7-segment decoder/driver

DS8880

Temperature range:
Commercial 0 °C to 70 °C DS8880N

- Directly drives high voltage gas discharge displays
- Ripple blanking facility
- TTL compatible inputs
- 135 mW typical power dissipation



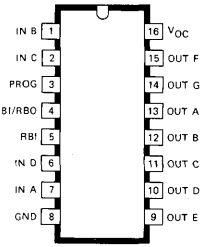
Package F, N-16

7-segment decoder/driver

DS8880-1

Temperature range:
Commercial 0 °C to 70 °C DS8880-1F, N

- Directly drives high voltage gas discharge displays
- Ripple blanking facility
- TTL compatible inputs
- 135 mW typical power dissipation
- 100 V interface



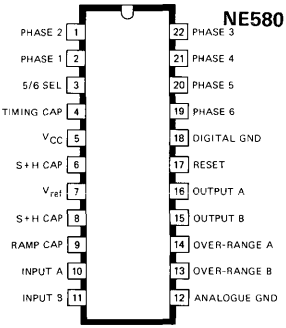
Package F, N-16

Bar-graph driver

NE580

Temperature range:
Commercial 0 °C to 70 °C NE580F, N

- Dual channel device
- Easily expandable to handle more channels
- Single 5 V supply
- 3, 5 or 6-phase operation
- Can be custom masked for different cathode segment counts (max 240)
- Overrange indication outputs



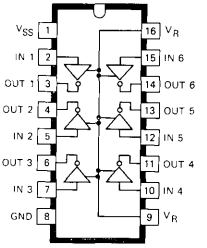
Package F, N-22

Hex universal driver

NE582

Temperature range:
Commercial 0 °C to 70 °C NE582F, N

- Low saturation voltage 0,5 V(typ)
- Output sink capability
  - each output 400 mA
  - all outputs 1200 mA
- Low input current loading
- Suitable for 3 V battery operation



Package F, N-16

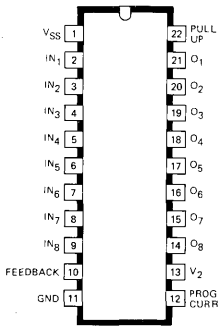
Gas discharge cathode driver

NE584

Temperature range:
Commercial 0 °C to 70 °C NE584F, N

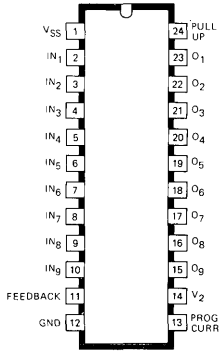
- Segment current programmability up to 5 mA
- Integral current limiting
- Minimum component count for system cost effectiveness
- Internal feedback network
- High output breakdown 90 V
- Internal output pull-up
- 8 or 9 segment versions

NE584-8



Package F, N-22

NE584-9



Package F, N-24

display interface

abridged data

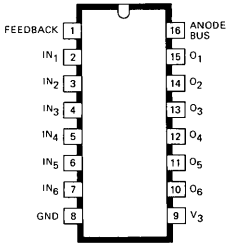
Gas discharge anode driver

NE585

Temperature range:
Commercial 0 °C to 70 °C NE585F, N

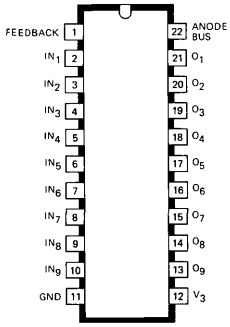
- Segment current programmability
- Internal current limiting
- Minimum component count for system cost effectiveness
- Internal feedback network
- Automatic loop control of firing voltage
- 6 or 9 digit versions
- High output breakdown 90 V
- Internal output pull-down

NE585-6



Package F, N-16

NE585-9



Package F, N-22

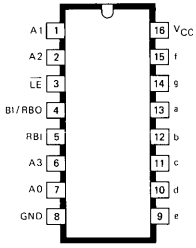
LED drivers

NE586 to 589

Temperature range:
Commercial 0 °C to 70 °C NE586 to 589F, N

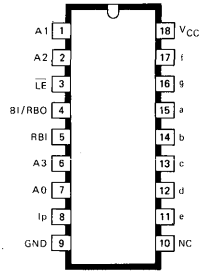
- Input microprocessor compatible
- NE586, NE588 fixed current
- NE587, NE589 current programmable
- NE586, NE587 current sinking outputs
- NE588, NE589 current sourcing outputs

NE586; NE588



Package F, N-16

NE587; NE589

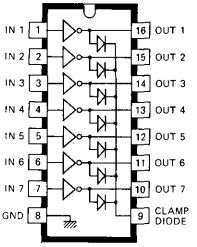


Package F, N-18

Darlington transistor array — NE5501

Temperature range:
Commercial 0 °C to 85 °C NE5501N

- High current 350 mA(max)
- V_{CEsat} 1,6 V at 350 mA(max)
- Output breakdown voltage 100 V(min)
- Input voltage V_{IN} 30 V(max)

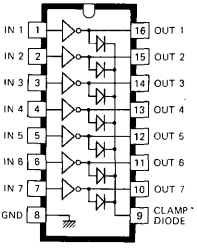


Package N-16

Darlington transistor array — NE5502

Temperature range:
Commercial 0 °C to 85 °C NE5502N

- High current 350 mA(max)
- V_{CEsat} 1,6 V at 350 mA(max)
- Output breakdown voltage 100 V(min)
- Input voltage V_{IN} 30 V(max)
- Each input has zener diode and resistor current limiting

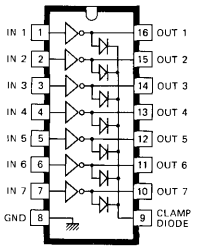


Package N-16

Darlington transistor array — NE5503

Temperature range:
Commercial 0 °C to 85 °C NE5503N

- High current 350 mA(max)
- V_{CEsat} 1,6 V at 350 mA(max)
- Output breakdown voltage 100 V(min)
- Input voltage V_{IN} 30 V(max)
- Each input has series resistor

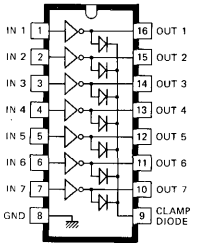


Package N-16

Darlington transistor array — NE5504

Temperature range:
Commercial 0 °C to 85 °C NE5504N

- High current 350 mA(max)
- V_{CEsat} 1,6 V at 350 mA(max)
- Output breakdown voltage 100 V(min)
- Input voltage V_{IN} 30 V(max)
- Each input has series resistor



Package N-16

memory interface

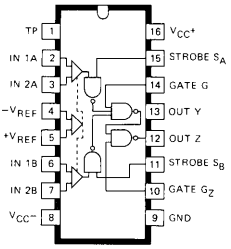
abridged data

Dual core sense amp

7520

Temperature range:
Commercial 0 °C to 70 °C 7520F, N

- Typical propagation delay 25 ns
- Complementary outputs with strobes
- No external stabilizing capacitor necessary
- ± 4 mV threshold uncertainty



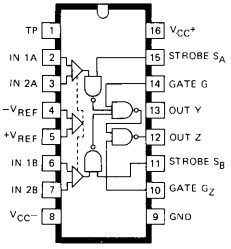
Package F, N-16

Dual core sense amp

7521

Temperature range:
Commercial 0 °C to 70 °C 7521F, N

- Typical propagation delay 25 ns
- Complementary outputs with strobes
- No external stabilizing capacitor necessary
- ± 7 mV thresehold uncertainty

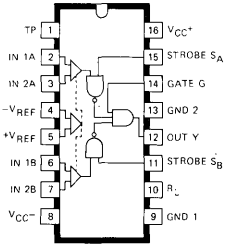


Package F, N-16

Dual core sense amp 7522

Temperature range:
Commercial 0 °C to 70 °C 7522F, N

- Typical propagation delay 25 ns
- Open collector output
- No external stabilizing capacitor necessary
- ± 4 mV threshold uncertainty

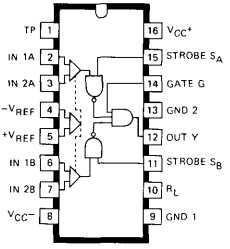


Package F, N-16

Dual core sense amp 7523

Temperature range:
Commercial 0 °C to 70 °C 7523F, N

- Typical propagation delay 25 ns
- Open collector output
- No external stabilizing capacitor necessary
- ± 7 mV threshold uncertainty

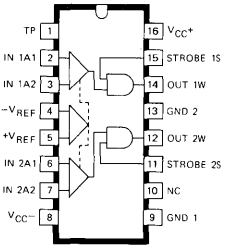


Package F, N-16

Dual core sense amp 7524

Temperature range:
Commercial 0 °C to 70 °C 7524F, N

- Typical propagation delay 25 ns
- Independent outputs with gating
- No external stabilizing capacitor necessary
- ± 4 mV threshold uncertainty

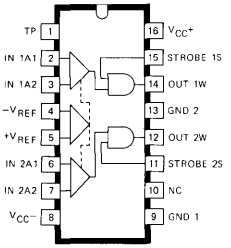


Package F, N-16

Dual core sense amp 7525

Temperature range:
Commercial 0 °C to 70 °C 7525F, N

- Typical propagation delay 25 ns
- Independent outputs with gating
- No external stabilizing capacitor necessary
- ± 7 mV threshold uncertainty



Package F, N-16

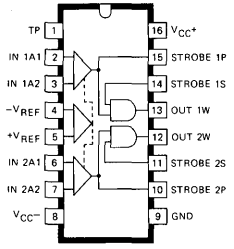
memory interface

abridged data

Dual core sense amp — 7528

Temperature range;
Commercial 0 °C to 70 °C 7528F, N

- Typical propagation delay 25 ns
- Independent outputs with gating
- No external stabilizing capacitor necessary
- Amplifier output available as a test point
- ± 4 mV threshold uncertainty

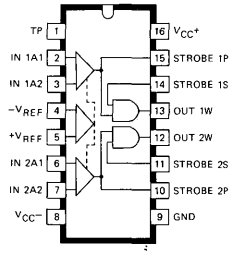


Package F, N-16

Dual core sense amp — 7529

Temperature range:
Commercial 0 °C to 70 °C 7529F, N

- Typical propagation delay 25 ns
- Independent outputs with gating
- No external stabilizing capacitor necessary
- Amplifier output available as a test point
- ± 7 mV threshold uncertainty

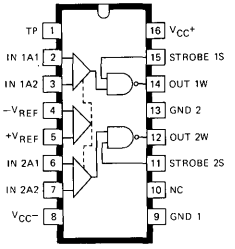


Package F, N-16

Dual core sense amp — 75232

Temperature range:
Commercial 0 °C to 70 °C 75232F, N

- Typical propagation delay 25 ns
- Independent outputs with gating
- No external stabilizing capacitor necessary
- Open collector output
- ± 4 mV threshold uncertainty

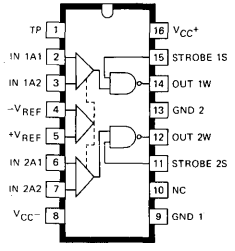


Package F, N-16

Dual core sense amp — 75233

Temperature range:
Commercial 0 °C to 70 °C 75233F, N

- Typical propagation delay 25 ns
- Independent outputs with gating
- No external stabilizing capacitor necessary
- Open collector output
- ± 7 mV threshold uncertainty

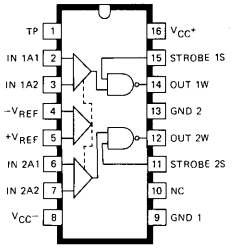


Package F, N-16

Dual core sense amp — 75234

Temperature range:
Commercial 0 °C to 70 °C — 75234F, N

- Typical propagation delay 25 ns
- Independent outputs with gating
- No external stabilizing capacitor necessary
- ± 4 mV threshold uncertainty

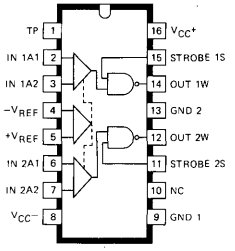


Package F, N-16

Dual core sense amp — 75235

Temperature range:
Commercial 0 °C to 70 °C — 75235F, N

- Typical propagation delay 25 ns
- Independent outputs with gating
- No external stabilizing capacitor necessary
- ± 7 mV threshold uncertainty

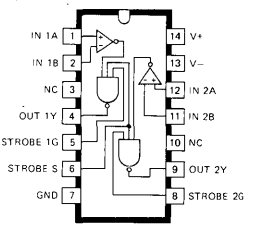


Package F, N-16

High-speed dual sense amp — 75S207

Temperature range:
Commercial 0 °C to 70 °C — 75S207F, N

- 17 ns guaranteed propagation delay
- 20 μA(max) input bias current
- STTL compatible strobes and outputs
- Large common mode input voltage range
- Standard supply voltages
- Function and pin compatible with SN75207

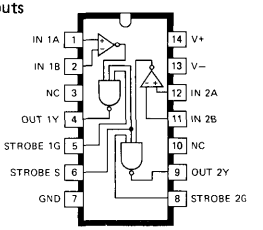


Package F, N-14

High-speed dual sense amp — 75S208

Temperature range:
Commercial 0 °C to 70 °C — 75S208F, N

- 17 ns guaranteed propagation delay
- 20 μA(max) input bias current
- STTL compatible strobes and outputs
- Large common mode input voltage range
- Standard supply voltages
- Function and pin compatible with SN75208
- Open collector outputs



Package F, N-14

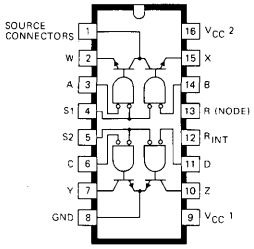
memory interface

abridged data

Memory driver — 55325/75325

Temperature range:
Military −55 °C to 125 °C 55325F
Commercial 0 °C to 70 °C 75325F, N

- 600 mA output capability
- Propagation delays 25 ns(typ)
- Output short-circuit protected
- Dual sink and source outputs
- Minimum time skew between address and output current rise
- 24 V output capability

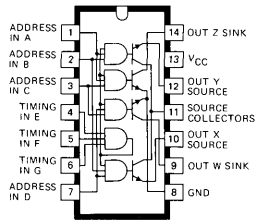


Package F, N-16

Memory driver — 75324

Temperature range:
Commercial 0 °C to 70 °C 75324N

- 400 mA output capability
- Internal decoding and timing
- Output short-circuit protection
- Dual sink/source outputs



Package N-14

telecommunications

survey

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telecommunications

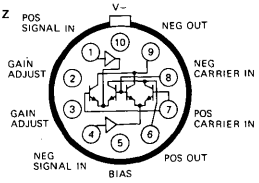
abridged data

Double balanced mixer/modulator

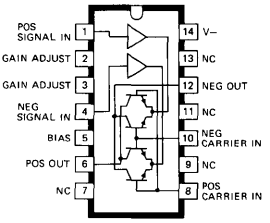
MC1496/1596

Temperature range:
Military −55 °C to 125 °C MC1596F, K, N
Commercial 0 °C to 70 °C MC1496F, K, N

- Carrier suppression 65 dB typical at 0,5 MHz
- Common mode rejection 85 dB



Package K



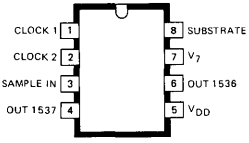
Package F, N-14

Bucket brigade delay line

NE503

Temperature range:
Industrial −20 °C to 85 °C NE503N

- Clock frequency 5-100 kHz
- 1536 buckets
- Signal delay 153,6 μs – 7,68 ms
- Attenuation 0 dB



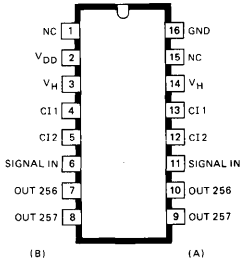
Package N

Bucket brigade delay line

NE504

Temperature range:
Industrial −20 °C to 85 °C NE504N

- Clock frequency 5-500 kHz
- 2 x 256 buckets
- Signal delay 256 μs – 25,6 ms
- Attenuation 3,5 dB



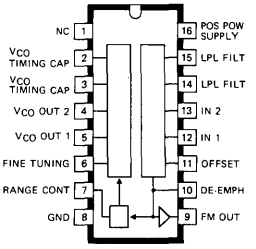
Package N-16

Phase locked loop — NE/SE560

Temperature range:

Military	−55 °C to 125 °C	SE560F
Commercial	0 °C to 70 °C	NE560F, N

- FM demodulation without tuned circuits
- Bandpass adjustable down to ± 1%
- Operating frequency up to 30 MHz typical



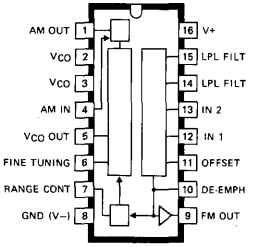
Package F, N-16

Phase locked loop — NE/SE561

Temperature range:

Military	−55 °C to 125 °C	SE561F
Commercial	0 °C to 70 °C	NE561F, N

- FM demodulation without tuned circuits
- Synchronous AM detection
- Operating frequency up to 30 MHz typical



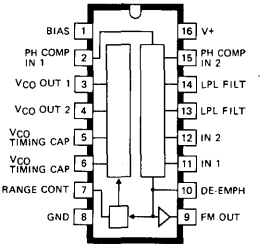
Package F, N-16

Phase locked loop — NE/SE562

Temperature range:

Military	−55 °C to 125 °C	SE562F
Commercial	0 °C to 70 °C	NE562F, N

- FM demodulation without tuned circuits
- Frequency multiplication and division
- Operating frequency up to 30 MHz typical



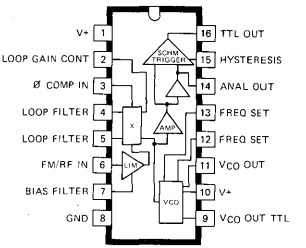
Package F, N-16

Phase locked loop — NE/SE564

Temperature range:

Military	−55 °C to 125 °C	SE564F
Commercial	0 °C to 70 °C	NE564F, N

- Operation with 5 V supply
- TTL compatible inputs/outputs
- Reduced carrier feed-through
- External loop gain control
- Operation to 50 MHz



Package F, N-16

telecommunications

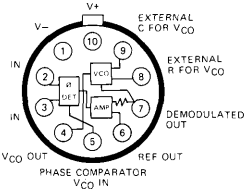
abridged data

Phase locked loop

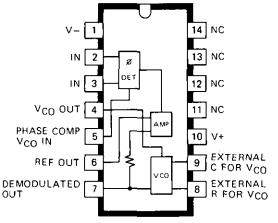
NE/SE565

Temperature range:
Military −55 °C to 125 °C SE565K
Commercial 0 °C to 70 °C NE565K, N

- Frequency range 0,001 Hz to 500 kHz
- High linearity of demodulated output, 0,2% typical
- Bandpass adjustable from ± 1% to ± 60%



Package K



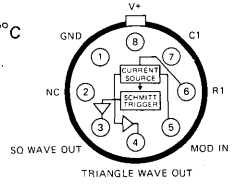
Package N-14

Function generator

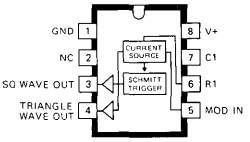
NE/SE566

Temperature range:
Military −55 °C to 125 °C SE566T
Commercial 0 °C to 70 °C NE566N, T

- High linear triangle wave output
- Temperature stability typically 200 ppm/°C
- Frequency range from 0,01 Hz to 1 MHz



Package T



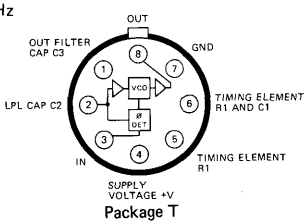
Package N

Tone decoder

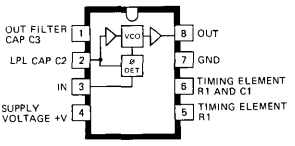
NE/SE567

Temperature range:
Military −55 °C to 125 °C SE567T
Commercial 0 °C to 70 °C NE567N, T

- Wide frequency range 0,01 Hz to 500 KHz
- Independently controlled bandwidth, up to 14%
- Logic compatible open collector output



Package T



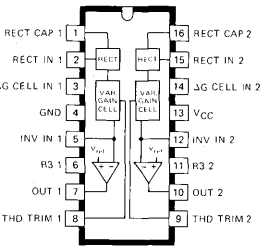
Package N

Analogue compandor

NE570

Temperature range:
Industrial −40 °C to 70 °C NE570F, N

- Complete IC compressor expandor
- 110 dB dynamic range
- Operates down to 6 V
- Typical noise 15 μV
- Full audio bandwidth



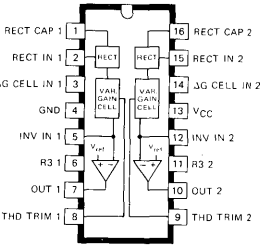
Package F, N-16

Analogue compandor

NE571

Temperature range:
Industrial −40 °C to 70 °C NE571F, N

- Complete IC compressor expandor
- 110 dB dynamic range
- Operates down to 6 V
- Typical noise 10 μV
- Full audio bandwidth



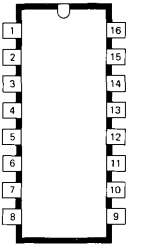
Package F, N-16

Phase locked loop

NE575

Temperature range:
Commercial 0 °C to 70 °C NE575N

- Single crystal
- Binary input
- ROM-programmed
- Supply 8 to 16 V



Package N-16

telecommunications

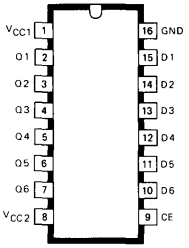
abridged data

Sextuple latch

NE593

Temperature range:
Industrial −25 °C to 85 °C NE593N

- Driving loads from 30 V supply
- 100 mA output
- TTL inputs
- Chip enable



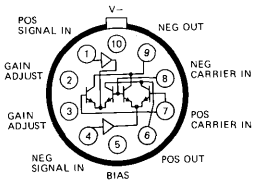
Package N-16

Double balanced mixer/modulator

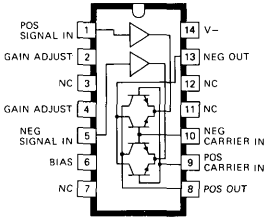
NE/SE5596

Temperature range:
Military −55 °C to 125 °C SE5596F, K, N
Commercial 0 °C to 70 °C NE5596F, K, N

- Carrier suppression 65 dB typical at 0,5 MHz
- Common mode rejection 85 dB



Package K



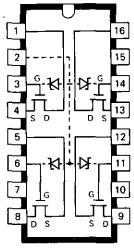
Package F, N-14

Quad analogue S.P.S.T. switch

SD5000

Temperature range:
Commercial 0 °C to 85 °C SD5000F, N

- Analogue signal range ± 10 V
- Ultra-fast t_d(ON) 1 ns(max)
- Isolation (at 3 kHz) 105 dB (typ)
- ON resistance 30 Ω (typ)
- Low feed-through and feedback transients
- Zener diode protected

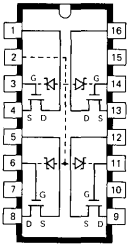


Package F, N-16

Quad analogue S.P.S.T. switch — SD5001

Temperature range:
Commercial 0 °C to 85 °C SD5001F, N

- Analogue signal range ± 5 V
- Ultra-fast t_d(ON) 1 ns (max)
- Isolation (at 3 kHz) – 105 dB (typ)
- ON resistance 30 Ω (typ)
- Low feed-through and feedback transients
- Zener diode protected

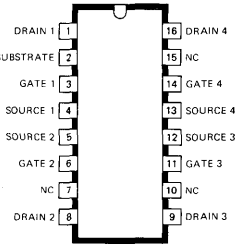


Package F, N-16

30 V driver circuit — SD5002

Temperature range:
Commercial 0 °C to 85 °C SD5002F, N

- Analogue signal range ± 7,5 V
- Ultra-fast t_d(ON) 1 ns (max)
- Isolation (at 3 kHz) – 105 dB (typ)
- ON resistance 30 Ω (typ)
- Low feed-through and feedback transients
- Zener diode protected

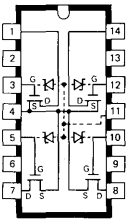


Package F, N-16

Four channel multiplexer — SD5100

Temperature range:
Commercial 0 °C to 85 °C SD5100F, N

- Analogue signal range ± 10 V
- Ultra-fast t_d(ON) 1 ns(max)
- Isolation (at 3 kHz) – 105 dB (typ)
- ON resistance 30 Ω (typ)
- Low feed-through and feedback transients
- Zener diode protected

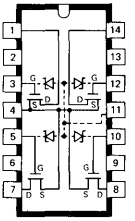


Package F, N-14

Four channel multiplexer — SD5101

Temperature range:
Commercial 0 °C to 85 °C SD5101F, N

- Analogue signal range ± 5 V
- Ultra-fast t_d(ON) 1 ns(max)
- Isolation (at 3 kHz) –105 dB (typ)
- ON resistance 30 Ω (typ)
- Low feed-through and feedback transients
- Zener diode protected



Package F, N-14

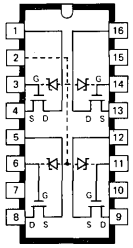
telecommunications

abridged data

Quad analogue S.P.S.T. driver — SD5200

Temperature range:
Commercial 0 °C to 85 °C SD5200F, N

- Drive capability ± 15 V
- Ultra-fast t_d(ON) 1 ns(max)
- Isolation (at 3 kHz) – 105 dB (typ)
- ON resistance 30 Ω (typ)
- Low feed-through and feedback transients
- Zener diode protected

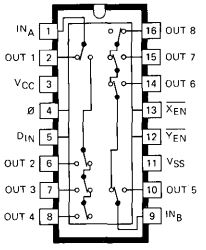


Package F, N-16

Cross point switch — SD5301

Temperature range:
Commercial 0 °C to 70 °C SD5301F, N

- Insertion loss 0,1 dB (typ)
- Crosstalk –120 dB (typ)
- Isolation –120 dB (typ)
- Supply current 4 mA (typ)
- V_{DD} 10-15 V
- TTL/C-MOS compatible controls

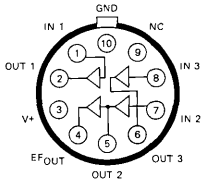


Package F, N-16

Triple amp — TAA960

Temperature range:
Ext. Ind. –55 °C to 65 °C TAA960

- Input resistance 25 kΩ (min)
- Supply current 2 mA (typ)
- Voltage gain 39 dB (typ)
- Emitter follower output stage

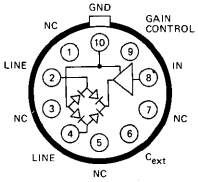


Package K

Microphone amp — TAA970

Temperature range:
Industrial –35 °C to 75 °C TAA970

- Reversible polarity
- Line current 10 to 100 mA
- Voltage drop 4,8 V (typ)

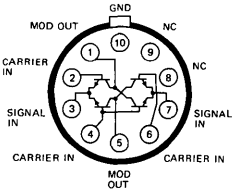


Package K

Ring modulator — TBA673

Temperature range:
Industrial −25 °C to 75 °C TBA673

- Closely matched transistors
- I_{CBO} less than 100 nA
- f_T 160 MHz (typ)

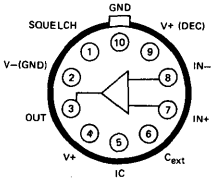


Package K

Low power audio amp — TBA915

Temperature range:
Military −55 °C to 125 °C TBA915

- Quiescent current 2 mA (typ)
- Output power 500 mW
- Total harmonic distortion less than 5%
- Supply voltage 12 V

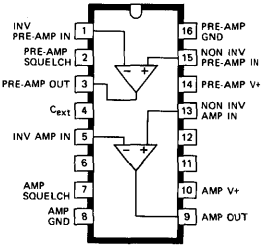


Package K

Low power audio amp — TCA210

Temperature range:
Military −55 °C to 125 °C TCA210

- Separate pre-amp
- Power output 500 mW
- Total harmonic distortion less than 5%
- Quiescent current 8 mA (typ)
- Pre-amp voltage gain 10 000
  noise figure typ. 4 dB
- Supply 12 V

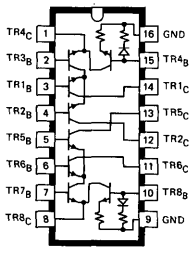


Package N-16

Double balanced mixer/modulator — TCA240

Temperature range:
Industrial −20 °C to 70 °C TCA240

- V_{BE} match less than 2,5 mV
- h_{FE} 23 to 190



Package N-16

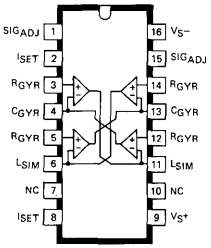
telecommunications

abridged data

Gyrator — TCA580

Temperature range:
Industrial −20 °C to 70 °C TCA580

- Frequency range DC to 10 kHz
- Q factor over 500
- Very high simulated inductance

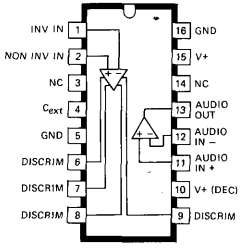


Package N-16

IF limiter amp — TCA770A

Temperature range:
Industrial −30 °C to 70 °C TCA770A

- Total current consumption 450 μA
- Supply voltage 7,5 V
- Frequency range 100-500 kHz
- AM rejection 50 dB (typ)

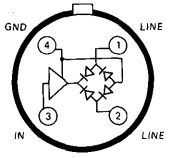


Package N-16

Microphone amp — TCA980

Temperature range:
Military −55 °C to 125 °C TDA980

- Reversible polarity
- Line current 10 to 100 nA
- Voltage drop 4,5 V (typ)

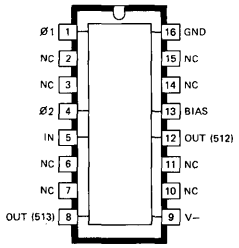


Package DE

Bucket brigade delay line — TDA1022 NE502

Temperature range:
Industrial −20 °C to 85 °C TDA1022 ,NE502N

- Clock frequency 5 to 500 kHz
- 512 buckets
- Signal delay 0,5 to 50 ms
- Frequency range 0 to 45 kHz
- Attenuation 4 dB (typ)



Package N-16

LOCMOS

HE4000B family

For detailed information
Handbook SC6

The LOCMOS HE4000B range is a fully buffered digital integrated circuit family which meets the Jedec-B specification. The members of this family are plug-in replacements for the well-known C-MOS 4000 and 14500 ranges. The HE family has the same advantages as conventional C-MOS circuits, plus the additional LOCMOS advantages. Recommended supply voltage range 3 to 15 V.

LOCMOS means Local Oxidation Complementary MOS.

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

Advantages of the C-MOS:

- low power dissipation – typically 10 nW per gate (static)
- wide operating supply voltage range
- wide operating temperature range from –40 to +85 °C
- high d.c. fan-out
- inputs and outputs are protected against electrostatic voltages

In addition to these, the LOCMOS HE4000B range has:

- buffered outputs on **all** circuits
- higher speed
- higher packing density – essential for MSI/LSI
- excellent noise immunity

The HE family is designed with standardized output drive characteristics which, combined with relative intensitivity to output capacitance loading, simplify system design.

Family ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

supply voltage	V_{DD}		–0,5 to +18	V
voltage on any input	V_I		–0,5 to (V_{DD} + 0,5)	V *
current into any input	$\pm I_I$	max.	10	mA
power dissipation per package				
for T_{amb} = –40 to +60 °C	P_{tot}	max.	400	mW
for T_{amb} = +60 to +85 °C	derate linearly with 8 mW/°C to 200 mW			
operating ambient temperature	T_{amb}		–40 to +85	°C
storage temperature	T_{stg}		–65 to +150	°C

* V_{DD} + 0,5 V should not exceed 18 V.

Type numbers have a suffix which signifies the type of package: P = plastic DIL; D = ceramic DIL

Family characteristics (d.c.) at V_{SS} = 0

parameter	symbol	T_{amb} = −40 °C min	T_{amb} = −40 °C max	T_{amb} = +25 °C min	T_{amb} = +25 °C max	T_{amb} = +85 °C min	T_{amb} = +85 °C max	V_{DD} V	conditions
Quiescent device current for gates	I_{DD}(μA)	–	1,0	–	1,0	–	7,5	5	
		–	2,0	–	2,0	–	15,0	10	
		–	4,0	–	4,0	–	30,0	15	
Quiescent device current for buffers, and flip-flops	I_{DD}(μA)	–	4,0	–	4,0	–	30	5	all valid input combinations; $V_I = V_{SS}$ or V_{DD}
		–	8,0	–	8,0	–	60	10	
		–	16,0	–	16,0	–	120	15	
Quiescent device current for MSI	I_{DD}(μA)	–	20	–	20	–	150	5	
		–	40	–	40	–	300	10	
		–	80	–	80	–	600	15	
Quiescent device current for LSI	I_{DD}(μA)	–	50	–	50	–	375	5	
		–	100	–	100	–	750	10	
		–	200	–	200	–	1500	15	
Output voltage LOW $\lvert I_O \rvert < 1$ μA	V_{OL}(V)	–	0,05	–	0,05	–	0,05	5	
		–	0,05	–	0,05	–	0,05	10	$V_I = V_{SS}$ or V_{DD}
		–	0,05	–	0,05	–	0,05	15	
Output voltage HIGH $\lvert I_O \rvert < 1$ μA	V_{OH}(V)	4,95	–	4,95	–	4,95	–	5	
		9,95	–	9,95	–	9,95	–	10	$V_I = V_{SS}$ or V_{DD}
		14,95	–	14,95	–	14,95	–	15	
Input voltage LOW $\lvert I_O \rvert < 1$ μA	V_{IL}(V)	–	1,5	–	1,5	–	1,5	5	V_O = 0,5 or 4,5 V
		–	3,0	–	3,0	–	3,0	10	V_O = 1,0 or 9,0 V
		–	4,0	–	4,0	–	4,0	15	V_O = 1,5 or 13,5 V
Input voltage HIGH $\lvert I_O \rvert < 1$ μA	V_{IH}(V)	3,5	–	3,5	–	3,5	–	5	V_O = 0,5 or 4,5 V
		7,0	–	7,0	–	7,0	–	10	V_O = 1,0 or 9,0 V
		11,0	–	11,0	–	11,0	–	15	V_O = 1,5 or 13,5 V
Output (sink) current LOW	I_{OL}(mA)	0,52	–	0,44	–	0,36	–	5	V_O = 0,4; V_I = 0 or 5 V
		1,3	–	1,1	–	0,9	–	10	V_O = 0,5; V_I = 0 or 10 V
		3,6	–	3,0	–	2,4	–	15	V_O = 1,5; V_I = 0 or 15 V
Output (source) current HIGH	$-I_{OH}$(mA)	0,52	–	0,44	–	0,36	–	5	V_O = 4,6; V_I = 0 or 5 V
		1,3	–	1,1	–	0,9	–	10	V_O = 9,5; V_I = 0 or 10 V
		3,6	–	3,0	–	2,4	–	15	V_O = 13,5; V_I = 0 or 15 V
Input leakage current	$\pm I_{IN}$(μA)	–	0,3	–	0,3	–	1,0	15	V_I = 0 or 15 V
Three-state output leakage current; HIGH	I_{OZH}(μA)	–	1,6	–	1,6	–	12,0	15	output returned to V_{DD}
Three-state output leakage current; LOW	$-I_{OZL}$(μA)	–	1,6	–	1,6	–	12,0	15	output returned to V_{DD}
Input capacitance per unit load	C_{IN}(pF)	–	–	–	7,5	–	–	–	any input

*CP= clock input to output
I = input to output
one figure means equal delays

conditions for t_{PLH}; t_{PHL}; f_{max}; dissipation: V_{DD} = 10 V; C_L = 50 pF			propagation delay * t_{PLH}; t_{PHL} ns		maximum clock pulse frequency MHz	dynamic dissipation at 1 MHz mW
NAND gates	**HEF4011B**	quadruple 2-input NAND gate	(I)	25	–	26
	HEF4012B	dual 4-input NAND gate	(I)	30; 25	–	14
	HEF4023B	triple 3-input NAND gate	(I)	30; 25	–	20
	HEF4068B	8-input NAND gate	(I)	35; 40	–	8
AND gates	**HEF4073B**	triple 3-input AND gate	(I)	20; 25	–	18
	HEF4081B	quadruple 2-input AND gate	(I)	20; 25	–	24
	HEF4082B	dual 4-input AND gate	(I)	30	–	17
NOR gates	**HEF4000B**	dual 3-input NOR gate and inverter	(I)	35	–	23
	HEF4001B	quadruple 2-input NOR gate	(I)	25	–	25
	HEF4002B	dual 4-input NOR gate	(I)	25	–	14
	HEF4025B	triple 3-input NOR gate	(I)	25	–	19
	HEF4078B	8-input NOR gate	(I)	35	–	8
OR gates	**HEF4071B**	quadruple 2-input OR gate	(I)	20; 25	–	25
	HEF4072B	dual 4-input OR gate	(I)	35	–	15
	HEF4075B	triple 3-input OR gate	(I)	30	–	19
Inverters and buffers	**HEF4007UB**	dual complementary pair and inverter	(I)	20	–	35
	HEF4041B	quadruple true/complement buffer	(I)	20	–	53
	HEF4049B	hex inverting buffers	(I)	30; 20	–	46
	HEF4050B	hex non-inverting buffers	(I)	25; 20	–	42
	HEF4069UB	hex inverter	(I)	20	–	34
	HEF4502B	strobed hex inverter/buffer	(I)	45	–	55
	HEF40097B	3-state hex non-inverting buffer	(I)	25; 30	–	55
	HEF40098B	3-state hex inverting buffer	(I)	30; 35	–	53
Complex gates	**HEF4030B**	quadruple EXCLUSIVE-OR gate	(I)	30; 35	–	25
	HEF4070B	quadruple EXCLUSIVE-OR gate	(I)	30; 35	–	25
	HEF4077B	quadruple EXCLUSIVE-NOR gate	(I)	30; 35	–	25
	HEF4085B	dual 2-wide 2-input AND-OR-invert gate	(I)	30	–	13
	HEF4086B	4-wide 2-input AND-OR-invert gate	(I)	40	–	8
Flip-flops	**HEF4013B**	dual D-type flip-flop	(CP)	40	25	15
	HEF4027B	dual JK flip-flop	(CP)	50	15	14
	HEF4076B	quadruple D-type flip-flop with 3-state outputs	(CP)	65; 60	22	19
	HEF40174B	hex D-type flip-flop	(CP)	30	30	31
	HEF40175B	quadruple D-type flip-flop	(CP)	30; 35	30	28
Specials	**HEF4046B**	phase-locked loop				
	HEF4738V	IEC/IEEE bus interface				
	HEF4739V	digital voltmeter circuit				

LOCMOS

HE4000B family

*CP= clock input to output
I = input to output
one figure means equal delays

		conditions for t_{PLH}; t_{PHL}; f_{max}; dissipation: V_{DD} = 10 V; C_L = 50 pF	propagation delay * t_{PLH}; t_{PHL} ns		maximum clock pulse frequency MHz	dynamic dissipation at 1 MHz mW
Counters	**HEF4017B**	5-stage Johnson counter	(CP)	95; 75	16	7
	HEF4018B	presettable divide-by-n counter	(CP)	55; 65	11	8
	HEF4020B	14-stage binary counter	(CP)	50; 45	25	8
	HEF4022B	4-stage divide-by-8 Johnson counter	(CP)	95; 75	16	7
	HEF4024B	7-stage binary counter	(CP)	45:40	25	8
	HEF4029B	synchronous up/down counter, binary/decade counter	(CP)	60; 55	25	10
	HEF4040B	12-stage binary counter	(CP)	50; 45	25	9
	HEF4510B	BCD up/down counter	(CP)	65; 60	24	10
	HEF4516B	binary up/down counter	(CP)	65; 60	24	10
	HEF4518B	dual BCD up counter	(CP)	65; 75	15	13
	HEF4520B	dual binary counter	(CP)	65; 75	15	13
	HEF4521B	24-stage frequency divider	(I)	400	25	10
	HEF4522B	programmable 4-bit BCD down counter		–	–	–
	HEF4526B	programmable 4-bit binary down counter		–	–	–
	HEF4534B	real time 5-decade counter	(CP)	750	6	–
	HEF4737B; V	quadruple static decade counters	(CP)	450	10	–
	HEF40160B	4-bit synchronous decade counter with asynchronous reset	(CP)	45	25	11
	HEF40161B	4-bit synchronous binary counter with asynchronous reset	(CP)	45	25	11
	HEF40162B	4-bit synchronous decade counter with synchronous reset	(CP)	45	25	11
	HEF40163B	4-bit synchronous binary counter with synchronous reset	(CP)	45	25	11
	HEF40192B	4-bit up/down decade counter	(CP)	70; 85	18	7
	HEF40193B	4-bit up/down binary counter	(CP)	70; 85	18	8
Registers	**HEF4006B**	18-stage static shift register	(CP)	40	30	18
	HEF4014B	8-bit shift register	(CP)	50; 60	22	13
	HEF4015B	dual 4-bit static shift register	(CP)	55; 60	23	28
	HEF4021B	8-bit static shift register	(CP)	55; 65	25	13
	HEF4031B	64-stage static shift register	(CP)	80; 85	14	19
	HEF4035B	4-bit universal shift register	(CP)	65; 70	25	15
	HEF4076B	quadruple D-type register with 3-state outputs	(CP)	65; 60	22	19
	HEF4094B	8-stage shift-and-store bus register	(CP)	120	8	–
	HEF4517B	dual 64-bit static shift register	(CP)	80; 85	14	45
	HEF4557B	1-to-64-bit variable length shift register	(CP)	80; 85	14	17
	HEF4731B; V	quadruple 64-bit static shift registers	(CP)	80; 85	14	60
	HEF40194B	4-bit bidirectional universal shift register	(CP)	35; 40	30	17
	HEF40195B	4-bit universal shift register	(CP)	45; 50	28	21
Digital multiplexers	**HEF4019B**	quadruple 2-input multiplexer	(I)	25; 30	–	25
	HEF4512B	8-input multiplexer with 3-state output	(I)	40; 35	–	7
	HEF4519B	quadruple 2-input multiplexer	(I)	40; 45	–	26
	HEF4539B	dual 4-input multiplexer	(I)	50; 45	–	13

*A = address to output
D = data to output
I = input to output
R/S = reset/set input to output
t_{ACC} = read access time
ST = strobe input to output
one figure means equal delays

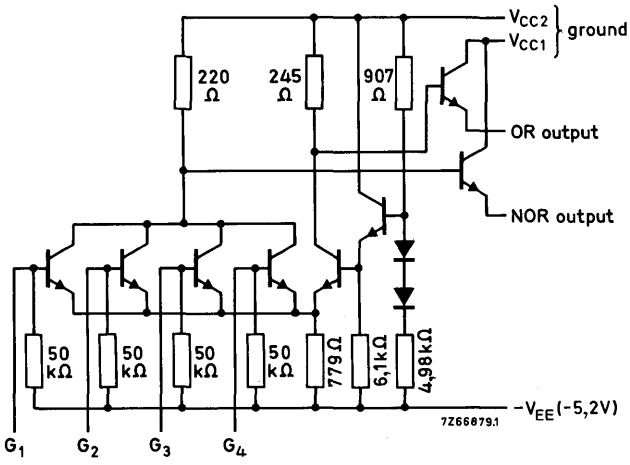
conditions for t_{PLH}; t_{PHL}; f_{max}; dissipation: V_{DD} = 10 V; C_L = 50 pF			propagation delay * t_{PLH}; t_{PHL} ns		ON-state frequency response MHz	dynamic dissipation at 1 MHz mW
Decoders	**HEF4028B**	1-of-10 decoder	(A)	45; 50	–	13
	HEF4511B	BCD to 7-segment latch/decoder/driver	(A)	55; 60	–	44
	HEF4514B	1-of-16 decoder/demultiplexer with input latches	(A)	95	–	11
	HEF4515B	1-of-16 decoder/demultiplexer with input latches	(A)	95	–	11
	HEF4543B	BCD to 7-segment latch/decoder driver for liquid crystal and LED displays	(A)	60; 70	–	46
	HEF4555B	dual 1-of-4 decoder/demultiplexer	(A)	55; 45	–	29
	HEF4556B	dual 1-of-4 decoder/demultiplexer	(A)	40; 50	–	28
Analogue switches and multiplexers/ demultiplexers	**HEF4016B**	quadruple bilateral switches	(I)	10	90	21
	HEF4051B	8-channel analogue multiplexer/demultiplexer	(I)	5	40	11
	HEF4052B	dual 4-channel analogue multiplexer/demultiplexer	(I)	5	40	16
	HEF4053B	triple 2-channel analogue multiplexer/demultiplexer	(I)	5	40	27
	HEF4066B	quadruple bilateral switches	(I)	5	90	24
	HEF4067B	16-channel analogue multiplexer/demultiplexer	(I)	10; 15	40	10
Latches	**HEF4042B**	quadruple D-latch	(D)	40	–	36
	HEF4043B	quadruple R/S latch with 3-state outputs	(R/S)	25; 35	–	14
	HEF4044B	quadruple R/S latch with 3-state outputs	(R/S)	40	–	15
	HEF4508B	dual 4-bit latch	(ST)	50	–	19
	HEF4724B	8-bit addressable latch	(D)	35	–	24
Translator	**HEF4104B**	quadruple low to high voltage translator with 3-state outputs	(I)	80	–	52
Memories	**HEF4505B**	64-bit, 1-bit per word read/write RAM	(t_{ACC})	100	–	–
	HEF4720B; V	256-bit, 1-bit per word RAM	(t_{ACC})	130	–	–
Multivibrators	**HEF4047B**	monostable/astable multivibrator	(I)	60	–	–
	HEF4528B	dual retriggerable-resettable monostable multivibrator	(I)	60; 50	–	30
Arithmetic circuits	**HEF4008B**	4-bit binary full adder	(D)	50; 55	–	35
	HEF4531B	13-input parity checker/generator	(I)	80	–	–
	HEF4532B	8-input priority encoder	(I)	70	–	–
	HEF4585B	4-bit magnitude comparator	(I)	55; 60	–	12
Schmitt triggers	**HEF4093B**	quadruple 2-input NAND Schmitt trigger	(I)	40	–	26
	HEF4583B	dual Schmitt trigger		–	–	–
	HEF40106B	hex Schmitt trigger	(I)	40	–	40

ECL

ECL 10 000 (GX family)

The GX family of ECL silicon monolithic integrated circuits is designed for high speed central processors and digital communication systems.
With 2,0 ns typical propagation delay and only 25 mW power dissipation per gate, this family offers an excellent speed-power product and so is recommended for high speed large system design.

Basic gate circuit



GX family ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

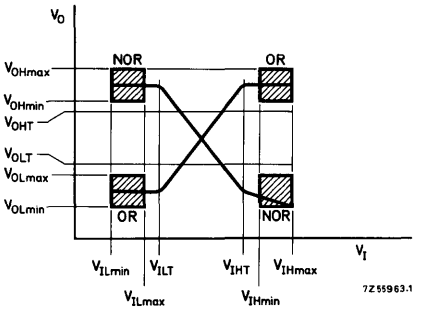
supply voltage (d.c.)	V_{EE}	max	−8,0	V
input voltage	V_I	0 to V_{EE}		
output current	I_O	max	50	mA
storage temperature	T_{stg}	−55 to +125		°C
junction temperature	T_j	max	125	°C

GX family characteristics (d.c.) at V_{CC} = ground; V_{EE} = −5,2 V

Each GX circuit has been designed to meet the d.c. specifications shown in the test table below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board and transverse air flow > 2,5 m/s is maintained. Outputs are terminated via a 50 Ω resistor to −2,0 V. Test values for applied conditions are given in the table and defined in the figure.

Test table

T_{amb}	0 °C	25 °C	75 °C	
V_{IHmax}	−0,840	−0,810	−0,720	V
V_{IHT}	−1,145	−1,105	−1,045	V
V_{ILT}	−1,490	−1,475	−1,450	V
V_{ILmin}	−1,870	−1,850	−1,830	V



	symbol		T_{amb} 0 °C	25 °C	75 °C		conditions
output voltage HIGH	V_{OH}	min	−1000	−960	−900	mV	inputs at V_{IHmax}
		typ		−880		mV	
		max	−840	−810	−720	mV	
output voltage LOW	V_{OL}	min	−1,870	−1,850	−1,830	V	inputs at V_{ILmin}
		typ		−1,720		V	
		max	−1,665	−1,650	−1,625	V	
output threshold voltage HIGH	V_{OHT}	min	−1020	−980	−920	mV	inputs at V_{IHT}
output threshold voltage LOW	V_{OLT}	max	−1,645	−1,630	−1,605	V	inputs at V_{ILT}
input current HIGH	I_{IH}	max		265		μA	V_{IHmax} for input under test
input current LOW	I_{IL}	min		10		μA	V_{ILmin} for input under test

ECL

ECL 10 000 (GX family)

Gates	**GXB10100**	quadruple 3-input NOR gate (1 input common)
	GXB10101	quadruple 2-input OR/NOR gate (1 input common)
	GXB10102	quadruple 2-input, 3 NOR and 1 OR/NOR gate
	GXB10103	quadruple 2-input, 3 OR and 1 OR/NOR gate
	GXB10104	quadruple 2-input, 3 AND and 1 AND/NAND gate
	GXB10105	triple 2-3-2 input OR/NOR gate
	GXB10106	triple 4-3-3 input NOR gate
	GXB10107	triple 2-input EXCLUSIVE-OR/EXCLUSIVE-NOR gate
	GXB10108	dual 3-input AND/NAND gate
	GXB10109	dual 4-5 input OR/NOR gate
	GXB10110	dual 3-input/3-output OR gate (line driver)
	GXB10111	dual 3-input/3-output NOR gate (line driver)
	GXB10113	quadruple EXCLUSIVE-OR gate (with enable)
	GXB10117	dual 2-wide 2-3 input OR-AND/OR-AND-invert gate
	GXB10118	dual 2-wide 3-input OR-AND gate
	GXB10119	4-wide 4-3-3-3 input OR-AND gate
	GXB10121	4-wide OR-AND/OR-AND-invert gate
	GXB10210	high speed dual 3-input/3-output OR gate
	GXB10211	high speed dual 3-input/3-output NOR gate
Interfaces	**GXB10112**	dual 3-input/3-output (1 OR and 2 NOR) line driver
	GXB10114	triple line receiver
	GXB10115	quadruple line receiver
	GXB10116	triple line receiver
	GXB10124	quadruple TTL to ECL translator
	GXB10125	quadruple ECL to TTL translator
	GXB10129	quadruple TTL/IBM bus receiver/latch
	GXB10188	hex buffer (non-inverting)
	GXB10189	hex inverter
	GXB10212	high speed dual 3-input/3-output (1 OR and 2 NOR) line driver
	GXB10216	high speed triple line receiver
Flip-flops	**GXB10130**	dual D-type latch
	GXB10131	dual D-type master-slave flip-flop
	GXB10133	quadruple latch with D-type inputs and enable outputs
	GXB10135	dual JK master-slave flip-flop
	GXB10175	quint D-latch with common reset and two wired-OR common clock inputs
	GXB10176	hex D-type master-slave flip-flop
	GXB10231	high speed dual D-type master-slave flip-flop
Counters and registers	**GXB10136**	universal hexadecimal counter
	GXB10137	universal decade counter
	GXB10141	4-bit universal shift register

Type numbers have a suffix which signifies the type of package: P = plastic DIL; D = ceramic DIL; E = metal-ceramic (for memories only)

Complex	**GXB10132**	dual 2-input multiplexer with clocked D-type latches and common reset
	GXB10134	dual 2-input multiplexer with clocked D-type latches
	GXB10158	quadruple 2-to-1 multiplexer (non-inverting)
	GXB10159	quadruple 2-to-1 multiplexer (inverting)
	GXB10160	12-bit parity checker/generator
	GXB10161	3-bit decoder with two enable inputs (1 of 8 lines LOW)
	GXB10162	3-bit decoder with two enable inputs (1 of 8 lines HIGH)
	GXB10164	8-input multiplexer with enable input
	GXB10165	8-input priority encoder
	GXB10170	9-bit parity checker/generator
	GXB10171	dual 2-bit decoder (one of four lines LOW)
	GXB10172	dual 2-bit decoder (one of four lines HIGH)
	GXB10173	quadruple 2-input multiplexer with latched outputs
	GXB10174	dual 4-to-1 multiplexer (with enable)
	GXB10179	look-ahead carry block
	GXB10180	dual 2-bit adder/subtractor
	GXB10181	4-bit arithmetic logic unit
	GXB10190	quadruple differential receiver/MST-ECL translator
	GXB10191	hex ECL-MST translator
Memories	**GXB10139**	256-bit, 8-bits per word PROM
	GXB10140	64-bit, 1-bit per word RAM (90 Ω output)
	GXB10142	fast 64-bit, 1-bit per word RAM
	GXB10144	256-bit, 1-bit per word RAM
	GXB10145	64-bit, 4-bits per word RAM
	GXB10146	1024-bit, 1-bit per word RAM
	GXB10148	64-bit, 1-bit per word RAM (50 Ω output)
	GXB10149	1024-bit, 4-bits per word PROM
	GXB10155	16-bit, 2-bits per word CAM (content addressable memory)
	GXB10405	128-bit, 1-bit per word RAM
	GXB10410	256-bit, 1-bit per word RAM
	GXB10415	1024-bit, 1-bit per word RAM

ECL

u.h.f. dividers

Type numbers have a suffix which signifies the type of package: P = plastic DIL, E = metal-ceramic

Temperature range: –40 to 85 °C

SAF1034E 4-to-1 divider 1,05 GHz
SAF1534E 4-to-1 divider 1,5 GHz

Temperature range: 0 to 75 °C

SAB1034P 4-to-1 divider 1,05 GHz
SAB1534P 4-to-1 divider 1,5 GHz

- dividers by four
- supply voltage: –5,2 V ± 5%
- power consumption: 250 mW (typ)
- output levels: ECL 10 000
- differential inputs
- packages: plastic and metal-ceramic DIL 14 pins

Applications

- high speed instrumentation (counters and frequency meters, synthesizers, oscilloscopes, nuclear instrumentation)
- telecommunications

TTL
survey

Military types	Commercial types		page
S54 . . series	**N74 . . series**	standard-range gold doped TTL	B110-B112
S54H . . series	**N74H . . series**	high-speed gold doped TTL	B113
S54S . . series	**N74S . . series**	high-speed Schottky TTL	B114-B115
S54LS . . series	**N74LS . . series**	low-power Schottky TTL	B116-B118
S82 . . series	**N82 . . series**	proprietary Schottky TTL	B119-B120
	N82S . . series	proprietary Schottky TTL	B121
S8T . . series	**N8T . . series**	TTL interface	B122

For military products see also pages B231-B237

Ratings

		Commercial types N74, N74H, N74S, N74LS	**Commercial types N82, N82S**	**Military types**	
supply voltage V_{CC}	min	4,75	4,75	4,5	V
	nom	5,0	5,0	5,0	V
	max	5,25	5,25	5,5	V
ambient temperature	min	0	0	−55	°C
	max	70	75	125	°C
storage temperature	min	−65	−65	−65	°C
	max	150	175	150	°C
				S82 and S8T max 200	°C

Characteristics

	S54/N74	**S54H/N74H**	**S54S/N74S**	**S54LS/N74LS**	**S82/N82**	**N82S**	
typ power dissipation per gate	10	23	20	2	10	20	mW
typ gate propagation delay	10	6	3	10	10	3	ns

Packages

Military types are generally available in both hermetic dual in-line (CERDIP) and hermetic flat package (CERPAC). Commercial types are predominantly supplied in plastic dual in-line package.

TTL

S54/N74 . .series

Gates	**S54/N7400**	quadruple 2-input positive NAND gate
	S54/N7401	quadruple 2-input positive NAND gate with open collector output
	S54/N7402	quadruple 2-input positive NOR gate
	S54/N7403	quadruple 2-input positive NAND gate with open collector output
	S54/N7408	quadruple 2-input positive AND gate
	S54/N7409	quadruple 2-input AND gate with open collector output
	S54/N7410	triple 3-input positive NAND gate
	S54/N7411	triple 3-input positive AND gate
	S54/N7412	triple 3-input NAND gate with open collector output
	S54/N7420	dual 4-input positive NAND gate
	S54/N7421	dual 4-input positive AND gate
	N7425	dual 4-input positive NOR gate (with strobe)
	S54/N7426	quadruple 2-input NAND gate with open collector output
	S54/N7427	triple 3-input NOR gate
	S54/N7430	8-input positive NAND gate
	S54/N7432	quadruple 2-input positive OR gate
	S54/N7450	expandable dual 2-wide 2-input AND-OR-invert gate
	S54/N7451	dual 2-wide 2-input AND-OR-invert gate
	S54/N7453	4-wide 2-input AND-OR-invert gate (expandable)
	S54/N7454	4-wide 2-input AND-OR-invert gate
	S54/N7460	dual 4-input expander
	S54/N7486	quadruple 2-input EXCLUSIVE-OR gate
Buffers, inverters	**S54/N7404**	hex inverter
	S54/N7405	hex inverter with open collector output
	S54/N7406	hex inverter buffer/driver with open collector output
	S54/N7407	hex buffer/driver with open collector output
	S54/N7416	hex inverter buffer/driver with open collector output
	S54/N7417	hex buffer/driver with open collector output
	S54/N7428	quadruple 2-input positive NOR buffer
	S54/N7433	quadruple 2-input positive NOR buffer
	S54/N7437	quadruple 2-input positive NAND buffer
	S54/N7438	quadruple 2-input positive NAND buffer with open collector output
	S54/N7440	dual 4-input positive NAND buffer
Bus drivers transceivers	**S54/N74125**	quadruple bus buffer gate with three-state outputs
	S54/N74126	quadruple bus buffer gate with three-state outputs
	S54/N74128	quadruple 2-input positive NOR buffer
	S54/N74365A	hex three-state buffer
	S54/N74366A	hex three-state inverter
	S54/N74367A	hex three-state buffer
	S54/N74368A	hex three-state inverter

Flip-flops	**S54/N7413**	dual NAND Schmitt trigger
	S54/N7414	hex Schmitt trigger
	S54/N7470	JK flip-flop
	S54/N7472	JK master-slave flip-flop
	S54/N7473	dual JK master-slave flip-flop
	S54/N7474	dual D-type edge-triggered flip-flop
	S54/N7476	dual JK master-slave flip-flop
	S54/N74107	dual JK master-slave flip-flop
	S54/N74109	dual JK positive edge-triggered flip-flop
	S54/N74121	monostable multivibrator
	N74122	retriggerable monostable multivibrator
	S54/N74123	retriggerable monostable multivibrator
	S54/N74132	quadruple Schmitt trigger
	S54/N74173	quadruple D-type flip-flop (three-state) (8T10)
	S54/N74174	hex D-type flip-flop with clear
	S54/N74175	quadruple D-type edge-triggered flip-flop
	N74221	dual monostable multivibrator
Shift registers	**S54/N7491**	8-bit shift register
	S54/N7494	4-bit shift register parallel-in/serial-out
	S54/N7495	4-bit left-right shift register
	S54/N7495A	4-bit left-right shift register
	S54/N7496	5-bit shift register
	S54/N74164	8-bit parallel-out serial shift register
	S54/N74165	parallel-load 8-bit shift register
	S54/N74166	8-bit shift register
	S54/N74170	4 x 4 register file
	N74178	4-bit parallel access shift register
	N74179	4-bit parallel access shift register
	S54/N74194	4-bit bidirectional universal shift register
	S54/N74195	4-bit parallel-access shift register
	S54/N74198	8-bit shift register
	S54/N74199	8-bit shift register
Counters	**S54/N7490**	decade counter
	S54/N7492	divide-by-twelve counter
	S54/N7493	4-bit binary counter
	S54/N74160	synchronous 4-bit decade counter
	S54/N74161	synchronous 4-bit binary counter
	S54/N74162	synchronous 4-bit decade counter
	S54/N74163	synchronous 4-bit binary counter
	N74176	presettable decade counter/latch
	N74177	presettable binary counter/latch
	N74190	synchronous up/down counter (BCD)
	N74191	synchronous up/down counter (binary)
	S54/N74192	synchronous decade up/down counter
	S54/N74193	synchronous 4-bit binary up/down counter
	N74196	presettable decade counter/latch
	N74197	presettable binary counter/latch

Latches	**S54/N7475**	quadruple bistable latch
	S5477	quadruple bistable latch
	S54/N74100	4-bit bistable latch (dual)
	S54/N74116	dual 4-bit latch with clear
	S54/N74279	quadruple S-R latch
Decoders-drivers	**S54/N7445**	BCD-to-decimal decoder/driver with open collector output
	S54/N7446A	BCD-to-7 segment decoder/driver
	S54/N7447A	BCD-to-7 segment decoder/driver
	S54/N7448	BCD-to-7 segment decoder/driver
	S54/N74145	BCD-to-decimal decoder/driver with open collector output
Decoder-multiplexers	**S54/N7442**	BCD-to-decimal decoder
	S54/N7443	excess 3-to-decimal decoder
	S54/N7444	excess 3-gray-to-decimal decoder
	S54/N74147	10-line to 4-line priority encoder
	S54/N74148	8-line to 3-line priority encoder
	S54/N74150	16-line to 1-line multiplexer
	S54/N74151	8-line to 1-line multiplexer
	S54/N74152	8-line to 1-line multiplexer
	S54/N74153	dual 4-line to 1-line multiplexer
	S54/N74154	4-line to 16-line decoder/demultiplexer
	S54/N74155	dual 2-line to 4-line decoder/demultiplexer
	S54/N74156	2-line to 4-line decoder demultiplexer
	S54/N74157	quadruple 2-input data selector (non-inverting)
	S54/N74158	quadruple 2-input data selector (inverting)
	S54/N74298	quadruple 2-input multiplexer with storage
Arithmetic units	**S54/N7480**	gated full adder
	S54/N7483	4-bit binary full adder
	N7483A	4-bit binary full adder
	S54/N7485	4-bit magnitude comparator
	S54/N74180	8-bit odd/even parity checker
	S54/N74181	4-bit arithmetic logic unit
	S54/N74182	look-ahead carry generator
	N74280	9-bit odd/even parity generator/checker
	N74283	4-bit adder

S54H/N74H . .series

Gates	**S54H/N74H00**	quadruple 2-input positive NAND gate
	S54H/N74H01	quadruple 2-input positive NAND gate with open collector output
	S54H/N74H08	quadruple 2-input positive AND gate
	S54H/N74H10	triple 3-input positive NAND gate
	S54H/N74H11	triple 3-input positive AND gate
	S54H/N74H20	dual 4-input positive NAND gate
	S54H/N74H21	dual 4-input positive AND gate
	S54H/N74H22	dual 4-input positive NAND gate with open collector output
	S54H/N74H30	8-input positive NAND gate
	S54H/N74H50	expandable dual 2-wide 2-input AND-OR-invert gate
	S54H/N74H51	dual 2-wide 2-input AND-OR-invert gate
	S54H/N74H52	expandable 4-wide 2-2-2-3 input AND-OR
	S54H/N74H53	4-wide 2-input AND-OR-invert gate (expandable)
	S54H/N74H54	4-wide 2-input AND-OR-invert gate
	S54H/N74H55	2-wide 2-input AND-OR-invert gate
	S54H/N74H60	dual 4-input expander
	S54H/N74H61	triple 3-input expander
	S54H/N74H62	3-2-2-3-input AND-OR expander
Buffers, inverters	**S54H/N74H04**	hex inverter
	S54H/N74H05	hex inverter with open collector output
	S54H/N74H40	dual 4-input positive NAND buffer
Flip-flops	**S54H/N74H71**	JK master-slave flip-flop with AND-OR
	S54H/N74H72	JK master-slave flip-flop
	S54H/N74H73	dual JK master-slave flip-flop
	S54H/N74H74	dual D-type edge-triggered flip-flop
	S54H/N74H76	dual JK master-slave flip-flop
	S54H/N74H101	JK negative edge-triggered flip-flop
	S54H/N74H102	JK negative edge-triggered flip-flop
	S54H/N74H103	dual JK negative edge-triggered flip-flop
	S54H/N74H106	dual JK negative edge-triggered flip-flop
	S54H/N74H108	dual JK negative edge-triggered flip-flop

TTL

S54S/N74S . .series

Gates	**S54S/N74S00**	quadruple 2-input positive NAND gate
	S54S/N74S02	quadruple 2-input positive NOR gate
	S54S/N74S03	quadruple 2-input positive NAND gate with open collector output
	S54S/N74S08	quadruple 2-input positive AND gate
	S54S/N74S09	quadruple 2-input AND gate with open collector output
	S54S/N74S10	triple 3-input positive NAND gate
	S54S/N74S11	triple 3-input positive AND gate
	S54S/N74S15	triple 3-input AND gate with open collector output
	S54S/N74S20	dual 4-input positive NAND gate
	S54S/N74S22	dual 4-input positive NAND gate with open collector output
	S54S/N74S32	quadruple 2-input positive OR gate
	S54S/N74S51	dual 2-wide 2-input AND-OR-invert gate
	S54S/N74S64	4-2-3-2-input AND-OR-invert gate
	S54S/N74S65	4-2-3-2-input AND-OR-invert gate
	S54S/N74S86	quadruple 2-input EXCLUSIVE-OR gate
	S54S/N74S133	13-input NAND gate
	S54S/N74S134	12-input NAND gate with three-state outputs
	N74S135	quadruple EXCLUSIVE-OR/NOR gate
	S54S/N74S260	dual 5-input NOR gate
Buffers, inverters	**S54S/N74S04**	hex inverter
	S54S/N74S05	hex inverter with open collector output
	N74S37	quadruple 2-input positive NAND buffer
	N74S38	quadruple 2-input positive NAND buffer with open collector output
	S54S/N74S40	dual 4-input positive NAND buffer
Flip-flops	**S54S/N74S74**	dual D-type edge-triggered flip-flop
	S54S/N74S112	dual JK negative edge-triggered flip-flop
	S54S/N74S113	dual JK positive edge-triggered flip-flop
	S54S/N74S114	dual JK negative edge-triggered flip-flop
	S54S/N74S174	hex D-type flip-flop with clear
	N74S175	quadruple D-type edge-triggered flip-flop
Shift registers	**N74S172**	16-bit multiple port register file
	N74S178	4-bit parallel access shift register
	N74S179	4-bit parallel access shift register
	N74S194	4-bit bidirectional universal shift register
	N74S195	4-bit parallel-access shift register
Counters	**N74S196**	presettable decade counter/latch
	N74S197	presettable binary counter/latch

Decoders-multiplexers	**N74S138**	3 to 1 of 8 line decoder/demultiplexer
	S54S/N74S139	dual 2 to 10 of 4 line decoder/demultiplexer
	S54S/N74S151	8-line to 1-line multiplexer
	S54S/N74S153	dual 4-line to 1-line multiplexer
	S54S/N74S157	quadruple 2-input data selector (non-inverting)
	S54S/N74S158	quadruple 2-input data selector (inverting)
	N74S251	data selector/multiplexer with three-state outputs
	S54S/N74S253	dual 4-line to 1-line data selector/multiplexer
	N74S257	quadruple 2-line to 1-line data selector/multiplexer
	N74S258	quadruple 2-line to 1-line data selector/multiplexer
Decoders-drivers	**S54S/N74S140**	dual 4-input NAND line driver
Arithmetic units	**S54S/N74S85**	4-bit magnitude comparator
	S54S/N74S181	4-bit arithmetic logic unit
	N74S182	look-ahead carry generator
	N74S280	9-bit odd/even parity generator/checker
	S54S/N74S350	4-bit shifter with three-state outputs

Gates	**S54LS/N74LS00**	quadruple 2-input positive NAND gate	
	S54LS/N74LS01	quadruple 2-input positive NAND gate with open collector output	
	S54LS/N74LS02	quadruple 2-input positive NOR gate	
	S54LS/N74LS03	quadruple 2-input positive NAND gate with open collector output	
	S54LS/N74LS08	quadruple 2-input positive AND gate	
	S54LS/N74LS09	quadruple 2-input AND gate with open collector output	
	S54LS/N74LS10	triple 3-input positive NAND gate	
	S54LS/N74LS11	triple 3-input positive AND gate	
	S54LS/N74LS12	triple 3-input NAND gate with open collector output	
	S54LS/N74LS15	triple 3-input AND gate with open collector output	
	S54LS/N74LS20	dual 4-input positive NAND gate	
	S54LS/N74LS21	dual 4-input positive AND gate	
	S54LS/N74LS22	dual 4-input positive NAND gate with open collector output	
	S54LS/N74LS26	quadruple 2-input NAND gate with open collector output	
	S54LS/N74LS27	triple 3-input NOR gate	
	S54LS/N74LS30	8-input positive NAND gate	
	S54LS/N74LS32	quadruple 2-input positive OR gate	
	S54LS/N74LS51	dual 2-wide 2-input AND-OR-invert gate	
	S54LS/N74LS54	4-wide 2-input AND-OR-invert gate	
	S54LS/N74LS55	2-wide 4-input AND-OR-invert gate	
	S54LS/N74LS86	quadruple 2-input EXCLUSIVE-OR gate	
	S54LS/N74LS136	quadruple EXCLUSIVE-OR with open collector output	
	S54LS/N74LS260	dual 5-input NOR gate	
	S54LS/N74LS266	quadruple EXCLUSIVE-NOR	
	S54LS/N74LS386	EXCLUSIVE-OR gate	
Buffers, inverters	**S54LS/N74LS04**	hex inverter	
	S54LS/N74LS05	hex inverter with open collector output	
	S54LS/N74LS28	quadruple 2-input positive NOR buffer	
	S54LS/N74LS33	quadruple 2-input positive NOR buffer with open collector output	
	S54LS/N74LS37	quadruple 2-input positive NAND buffer	
	S54LS/N74LS38	quadruple 2-input positive NAND buffer with open collector output	
	S54LS/N74LS40	dual 4-input positive NAND buffer	
Bus drivers, transceivers	**S54LS/N74LS125**	quadruple bus buffer gate	with three-state output
	S54LS/N74LS126	quadruple bus buffer gate	
	N74LS240	octal line driver receiver	
	N74LS241	octal line driver receiver	
	S54LS/N74LS242	quadruple bus transceiver	
	S54LS/N74LS243	quadruple bus transceiver	
	S54LS/N74LS365	hex 3-state buffer	
	S54LS/N74LS366	hex 3-state inverter	
	S54LS/N74LS367	hex 3-state buffer	
	S54LS/N74LS368	hex 3-state inverter	

Flip-flops	**S54LS/N74LS13**	dual NAND Schmitt trigger
	S54LS/N74LS14	hex Schmitt trigger
	S54LS/N74LS73	dual JK master-slave flip-flop
	S54LS/N74LS74	dual D-type edge triggered flip-flop
	S54LS/N74LS76	dual JK master-slave flip-flop
	S54LS/N74LS78	dual JK negative edge-triggered flip-flop
	S54LS/N74LS107	dual JK master-slave flip-flop
	S54LS/N74LS109	dual JK positive edge-triggered flip-flop
	S54LS/N74LS112	dual JK negative edge-triggered flip-flop
	S54LS/N74LS113	dual JK positive edge-triggered flip-flop
	S54LS/N74LS114	dual JK negative edge-triggered flip-flop
	N74LS123	dual retriggerable monostable multivibrator
	S54LS/N74LS132	quadruple Schmitt trigger
	S54LS/N74LS173	quadruple D-type flip-flop
	S54LS/N74LS174	hex D-type flip-flop with clear
	S54LS/N74LS175	quadruple D-type edge-triggered flip-flop
	S54LS/N74LS221	dual monostable multivibrator
	N74LS273	octal D-type flip-flop with clear
	N74LS377	octal D-type flip-flop with clear
Arithmetic units	**S54LS/N74LS83A**	4-bit binary full adder
	S54LS/N74LS85	4-bit magnitude comparator
	S54LS/N74LS181	4-bit arithmetic logic unit
	S54LS/N74LS261	2 x 4 parallel binary multiplier
	S54LS/N74LS283	4-bit adder
	S54LS/N74LS670	4 x 4 register file (three-state)
Shift registers	**S54LS/N74LS95B**	4-bit right-shift left-shift register
	S54LS/N74LS96	5-bit shift register
	S54LS/N74LS164	8-bit parallel-out serial shift register
	S54LS/N74LS170	4 x 4 register file
	S54LS/N74LS194A	4-bit bidirectional universal shift register
	S54LS/N74LS195A	4-bit parallel-access shift register
	S54LS/N74LS295A	4-bit right-shift left-shift register
	S54LS/N74LS395	4-bit cascadable shift register

Counters	**S54LS/N74LS90**	decade counter
	S54LS/N74LS92	divide-by-twelve counter
	S54LS/N74LS93	4-bit binary counter
	S54LS/N74LS161	synchronous 4-bit binary counter
	S54LS/N74LS163	synchronous 4-bit binary counter
	S54LS/N74LS190	synchronous up/down counter (BCD)
	S54LS/N74LS191	synchronous up/down counter (binary)
	S54LS/N74LS192	synchronous decade up/down counter
	S54LS/N74LS193	synchronous 4-bit binary up/down counter
	S54LS/N74LS196	presettable decade counter/latch
	S54LS/N74LS197	presettable binary counter/latch
	S54LS/N74LS290	decade counter
	S54LS/N74LS293	4-bit binary counter
Latches	**S54LS/N74LS75**	quadruple latch
	N74LS273	octal latch
	S54LS/N74LS279	quadruple S-R latch
	S54LS/N74LS375	quadruple latch
Decoders-multiplexers	**S54LS/N74LS42**	BCD-to-decimal decoder
	S54LS/N74LS138	3 to 1 of 8 line decoder/demultiplexer
	S54LS/N74LS139	dual 2-line to 4-line decoder/demultiplexer
	S54LS/N74LS151	8-line to 1-line multiplexer
	S54LS/N74LS153	dual 4-line to 1-line multiplexer
	S54LS/N74LS154	4-line to 16-line decoder/demultiplexer
	S54LS/N74LS155	dual 2-line to 4-line decoder/demultiplexer
	S54LS/N74LS156	dual 2-line to 4-line decoder/demultiplexer
	S54LS/N74LS157	quadruple 2-input data selector (non-inverting)
	S54LS/N74LS158	quadruple 2-input data selector (inverting)
	S54LS/N74LS251	data selector/multiplexer with three-state outputs
	S54LS/N74LS253	dual 4-line to 1-line data selector/multiplexer
	N74LS254	4 to 16 decoder/demultiplexer with three-state output
	S54LS/N74LS257	quadruple 2-line to 1-line data selector/multiplexer
	S54LS/N74LS258	quadruple 2-line to 1-line data selector/multiplexer
	S54LS/N74LS298	quadruple 2-input multiplexer with storage
Decoders-drivers	**S54LS/N74LS145**	high-voltage BCD-to-decimal decoder/driver with open collector output

MSI – S82/N82 and other series

Arithmetic units	**S82/N8260**	arithmetic logic unit
	S82/N8261	fast carry extender
	S82/N8268	gated full adder
Buffers/inverters	**S80/N8095**	hex 3-state buffer
	S80/N8096	hex 3-state inverter
	S80/N8097	hex 3-state buffer
	S80/N8098	hex 3-state inverter
Counters	**S82/N8280**	presettable decade counter
	S82/N8281	presettable binary counter
	S82/N8284	binary up/down counter
	S82/N8285	decade up/down counter
	S82/N8288	divide-by-12 counter
	S82/N8290	high-speed presettable decade counter
	S82/N8291	high-speed presettable binary counter
	S82/N8292	presettable low power decade counter
	S82/N8293	presettable low power binary counter
	S93/N9310	4-bit decade counter
	S93/N9316	4-bit binary counter
Decoders/display drivers	**S82/N8250**	binary-to-octal decoder
	S82/N8251	BCD-to-decimal decoder
	S82/N8252	BCD-to-decimal decoder
Flip-flops	**S96/N9601**	retriggerable monostable multivibrator
	S96/N9602	dual monostable multivibrator
Multiplexers	**S82/N8230**	8-input digital multiplexer
	S82/N8231	8-input digital multiplexer
	S82/N8232	8-input digital multiplexer
	S82/N8233	2-input, 4-bit digital multiplexer
	S82/N8234	2-input, 4-bit digital multiplexer
	S82/N8235	2-input, 4-bit digital multiplexer
	S82/N8263	3-input, 4-bit digital multiplexer
	S82/N8264	3-input, 4-bit digital multiplexer
	S82/N8266	2-input, 4-bit digital multiplexer
	S82/N8267	2-input, 4-bit digital multiplexer
	S93/N9309	dual 4-input multiplexer
	S93/N9312	8-input digital multiplexer
	S93/N9322	data selector multiplexer

Parity functions	**S82/N8241**	quadruple EXCLUSIVE-OR
	S82/N8242	quadruple EXCLUSIVE-NOR
	S82/N8262	9-bit parity generator and checker
	S82/N8269	4-bit comparator
	S93/N9324	5-bit comparator
Registers/latches	**S82/N8200**	dual 5-bit buffer register
	S82/N8201	dual 5-bit buffer register with D complement
	S82/N8202	10-bit buffer register
	S82/N8203	10-bit buffer register with D complement
	S82/N8270	4-bit shift register
	S82/N8271	4-bit shift register
	S82/N8273	10-bit serial-in, parallel-out shift register
	S82/N8274	10-bit parallel-in, serial-out shift register
	S82/N8275	quadruple bistable latch
	S82/N8276	8-bit serial shift register
	S82/N8277	dual 8-bit shift register
	S93/N9300	4-bit shift register
	S93/N9308	dual 4-bit latch with clear
	S93/N9314	quadruple latch
	S93/N9334	8-bit addressable latch
Scaler (Asynchronous shift register)	**S82/N8243**	8-bit position scaler

Decoders/drivers	**N82S50**	binary-to-octal decoder
	N82S52	BCD-to-decimal decoder
	N82S90	high-speed presettable decimal/binary decoder
	N82S91	high-speed presettable decimal/binary decoder
Multiplexers	**N82S30**	8-input digital multiplexer
	N82S31	8-input digital multiplexer
	N82S32	8-input digital multiplexer
	N82S33	2-input, 4-bit digital multiplexer
	N82S34	2-input, 4-bit digital multiplexer
	N82S66	2-input, 4-bit digital multiplexer
	N82S67	2-input, 4-bit digital multiplexer
Parity functions	**N82S41**	quadruple EXCLUSIVE-OR element
	N82S42	4-bit quadruple EXCLUSIVE-NOR
	N82S62	9-bit parity generator/checker
Shift registers	**N82S70**	high-speed 4-bit shift register
	N82S71	high-speed 4-bit shift register
Arithmetic units	**N82S82**	4-bit BCD arithmetic unit
	N82S83	4-bit BCD adder

TTL

interface — S8T/N8T . .series

Translators/buffers	**S8T/N8T18**	high voltage to TTL translator
	S8T/N8T80	quadruple 2-input NAND gate (high voltage)
	S8T/N8T90	hex inverter (high voltage)
Timing circuits	**S8T/N8T20**	bidirectional one shot
	S8T/N8T22/9601	retriggerable monostable multivibrator
	N8T363	dual zero crossing detector
	S96/N9602	dual retriggerable monostable multivibrator
Line drivers receivers transceivers	**S8T/N8T09**	quadruple three-state bus driver
	S8T/N8T10	quadruple three-state D-type bus flip-flop
	S8T/N8T13	dual low impedance line driver
	S8T/N8T14	triple line receiver/Schmitt trigger
	S8T/N8T15	dual communications line driver
	S8T/N8T16	dual communications line receiver
	N8T23	dual IBM 360/370 line driver
	N8T24	triple IBM 360/370 line receiver
	N8T25	dual MOS to TTL interface
	S8T/N8T26A	quadruple three-state bus transceiver (inverting)
	S8T/N8T28	quadruple three-state bus transceiver (non-inverting)
	N8T30	dual DTL/TTL to MOS transceiver/port controller
	S8T/N8T31	8-bit bidirectional input/output port
	N8T34	quadruple bus transceiver (three-state outputs)
	S8T/N8T37	hex bus receiver/Schmitt trigger
	N8T38	quadruple bus transceiver (open collector)
	N8T93	high-speed hex inverter
	S8T/N8T94	high-speed hex inverter (open collector)
	S8T/N8T95/97	high-speed hex three-state buffer
	S8T/N8T96/98	high-speed hex three-state inverter
	N8T380	quadruple bus receiver with hysteresis/Schmitt trigger
Decoder drivers	**S8T/N8T04**	7-segment decoder display driver
	S8T/N8T05	7-segment decoder display driver
	S8T/N8T06	7-segment decoder display driver

memories

type index

Bipolar

For military products see also pp B231 to B237

technology	RAM capacity	type	page	PROM capacity	type	page
TTL	16 x 4	**N3101A**	B132-B133	32 x 8	**N82S23**	B134-B135
	16 x 4	**N74S89**		32 x 8	**N82S123**	
	16 x 4	**N74S189**		256 x 4	**N82S27**	
	16 x 4	**N82S25**		256 x 4	**N82S126**	
	256 x 1	**N74S200**		256 x 4	**N82S129**	
	256 x 1	**N74S201**		256 x 8	**N82S114**	
	256 x 1	**N74S301**		512 x 4	**N82S130**	
	256 x 1	**N82S16**		512 x 4	**N82S131**	
	256 x 1	**N82S116**		512 x 8	**N82S115**	
	256 x 1	**N82S17**		512 x 8	**N82S140**	
	256 x 1	**N82S117**		512 x 8	**N82S141**	
	64 x 9	**N82S09**		512 x 8	**N82S146**	
	1k x 1	**N82S10**		512 x 8	**N82S147**	
	1k x 1	**N93415A**		1k x 4	**N82S136**	
	1k x 1	**N82S110**		1k x 4	**N82S137**	
	1k x 1	**N82LS10**		1k x 8	**N82S180**	
	1k x 1	**N82S11**		1k x 8	**N82S181**	
	1k x 1	**N93425A**		1k x 8	**N82S2708**	
	1k x 1	**N82S111**		2k x 4	**N82S184**	
	1k x 1	**N82LS11**		2k x 4	**N82S185**	
	256 x 8	**N82S208**		2k x 8	**N82S190**	
	256 x 9	**N82S210**		2k x 8	**N82S191**	
	4k x 1	**N82S400**				
	4k x 1	**N82S401**				
ECL	16 x 4	**GXB10145**	B136-B137	32 x 8	**GXB10139**	B136-B137
	64 x 1	**GXB10140**		256 x 4	**GXB10149**	
	64 x 1	**GXB10142**				
	64 x 1	**GXB10148**				
	128 x 1	**GXB10405**				
	256 x 1	**GXB10144**				
	256 x 1	**GXB10410**				
	1k x 1	**GXB10415**				

When ordering please quote the ordering code to specify device, temperature range if applicable (prefix N or S), and package (suffix D, E, F, I, K, N, P, T or TA).

Examples:
N82S25N commercial temperature range, plastic DIL package
S82S16F military temperature range, cerdip DIL package
N74S89N commercial temperature range, plastic DIL package
S54S89F military temperature range, cerdip DIL package

technology	ROM capacity	type	page	specials capacity		type	page
TTL	256 x 4	**N82S226**	B136-B137	8 x 4	SAM	**N82S12**	B136-B137
	256 x 4	**N82S229**		8 x 4	SAM	**N82S112**	
	256 x 8	**N82S214**		32 x 2	WWRM	**N82S21**	
	512 x 4	**N82S230**		16 x 48 x 8	FPLA	**N82S100**	
	512 x 4	**N82S231**		16 x 48 x 8	FPLA	**N82S101**	
	512 x 8	**N82S215**		16 x 9	FPGA	**N82S102**	
	512 x 8	**N82S240**		16 x 9	FPGA	**N82S103**	
	512 x 8	**N82S241**		16 x 48 x 8	FPLA	**N82S106**	
	1k x 4	**N8228**		16 x 48 x 8	FPLA	**N82S107**	
	1k x 8	**N82S280**		16 x 48 x 8	PLA	**N82S200**	
	1k x 8	**N82S281**		16 x 48 x 8	PLA	**N82S201**	
	2k x 8	**N82S290**					
	2k x 8	**N82S291**					
ECL				8 x 2	CAM	**GXB10155**	B136-B137

memories

type index

MOS

	RAM			EPROM		
technology	capacity	type	page	capacity	type	page
MOS	**static**					
	256 x 1	**2501**	B138-B139	4k	**2704**	B138-B139
	256 x 1	**25L01**		8k	**2708**	
	256 x 1	**HEF4720B(V)**				
	256 x 4	**2101**				
	256 x 4	**2111**				
	256 x 4	**2112**				
	256 x 4	**2606**				
	256 x 4	**2606-1**				
	1k x 1	**2102**				
	1k x 1	**21F02**				
	1k x 1	**21L02**				
	1k x 1	**2102A/AL**				
	1k x 1	**2115**				
	1k x 1	**2125**				
	1k x 4	**2614**				
	1k x 4	**2624**				
	4k x 1	**2613**				
	4k x 1	**2623**				
	dynamic					
	4k x 1	**2627**	B138-B139			
	4k x 1	**2660**				
	4k x 1	**2680**				
	16k x 1	**2690**				

When ordering please quote the ordering code to specify device, temperature range if applicable (prefix N or S), and package (suffix D, E, F, I, K, N, P, T or TA).

Examples:
N82S25N commercial temperature range, plastic DIL package
S82S16F military temperature range, cerdip DIL package
N74S89N commercial temperature range, plastic DIL package
S54S89F military temperature range, cerdip DIL package

technology	capacity	type	page	capacity	type	page
MOS	**ROM**			**static**		
	512 x 8	**2530**	B138-B139	2 x 50	**2509**	B140
	1k x 8	**2607**		6 x 32	**2518**	
	1k x 8	**2608**		2 x 100	**2510**	
	2k x 4	**2580**		6 x 40	**2519**	
	2k x 8	**2600**		2 x 128	**2521**	
	2k x 8	**2616**		2 x 132	**2522**	
	2k x 8	**2617**		4 x 80	**2532**	
				2 x 200	**2511**	
				2 x 240	**2529**	
				2 x 250	**2528**	
				2 x 256	**2527**	
				1 x 1k	**2533**	
	character generators			**dynamic**		
	64 x 8 x 5	**2513**	B138-B139	2 x 100	**2506**	B140
	64 x 6 x 8	**2516**		2 x 100	**2507**	
	64 x 9 x 9	**2526**		2 x 100	**2517**	
	128 x 7 x 9	**2609**		1 x 512	**2505**	
				1 x 512	**2524**	
				4 x 256	**2502**	
				2 x 512	**2503**	
				1 x 1k	**2504**	
				1 x 1k	**2512**	
				1 x 1k	**2525**	

memories

cross reference

Bipolar

AMD	Signetics
2700/27LS00	82S16
2701/27LS01	82S17
27S08/27LS08	82S23
27S09/27LS09	82S123
27S10	82S126
27S11	82S129
2952	82S10/93415A
2953	82S11/93425A
2980	82S101
2981	82S100
3101	82S25
3101A/27S02	3101A

Fairchild	Signetics
10405	GXB10405
10410	GXB10410/10144
10415	GXB10415
10145A	GXB10145
10149	GXB10149
93403	82S25
93406	82S226
93410	74S301
93411	82S17
93411A	82S117
93415	82S10
93415A	93415A
93415B	82S110
93L415	82LS10
93417	82S126
93419	82S09
93421	82S16
93421A	82S116
93425	82S11
93425A	93425A
93425B	82S111
93L425	82LS11
93427	82S129
93431	82S230
93436	82S130
93438	82S140
93441	82S231
93442	82S241
93446	82S131
93448	82S141
93452	82S136
93453	82S137
93454	82S280
93457	82S226
93464	82S281
93467	82S229

Harris	Signetics
0064	82S25
1024/HM7610	82S129
1024A/HM7611	82S126
2048	82S131
2048A	82S130
HM7602/8256	82S23
HM7603	82S123
HM7615	GXB10149
HM7620	82S130
HM7621	82S131
HM7640	82S140
HM7641	82S141
HM7642	82S136
HM7643	82S137
HM7644	82S115 **
HM7699	82S115 **

Intel	Signetics
2708	82S2708
3101	82S25
3101A	3101A
3106/3106A	82S16
3107/3107A	82S17
3301A	82S226
3302	82S230
3304	82S215 **
3322	82S231
3601	82S126
3602	82S130
3604	82S140
3605	82S136
3621	82S129
3622	82S131
3624	82S141
3625	82S137

** Not pin-for-pin compatible.

Intersil	Signetics
5501	82S25
5503	74S301
55S08(A)	82S10
55S18(A)	82S11
5523A	82S16
5533A	82S17
5600	82S23
5603	82S126
5604A	82S130
5605	82S140
56S06	82S136
5610	82S123
5623A	82S129
5624	82S131
5625	82S141
56S26	82S137

Motorola	Signetics
10139	GXB10139
10140	GXB10140
10142	GXB10142
10144	GXB10144/10410
10145	GXB10145
10146/10415	GXB10415
10147	GXB10405
10148	GXB10148
10149	GXB10149
4004A	82S226
4064	82S25
4256	82S16
5005	82S126
68708	82S2708

MMI	Signetics
10149	GXB10149
6200	82S226
6201	82S229
6205	82S230
6206	82S231
6275	82S290
6276	82S291
6280	82S280
6281	82S281
6300-1	82S126
6301-1	82S129
6305-1	82S130
6306-1	82S131
6330	82S23
6331	82S123
6335	82S114 **
6340	82S140
6341	82S141
6348	82S146
6349	82S147
6352	82S136
6353	82S137
6380	82S180
6381	82S181
6385	82S2708
6530	82S17
6531	82S16
6555	82S09
6560	82S25/3101A
6561	74S189
82S100	82S100
82S101	82S101

National Semiconductor	Signetics
74187	82S226
8573	82S126
8574	82S129
8582	82S17
8588	82S23
86L99	82S25

TI	Signetics
2708	82S2708
	82S400
	82S401
10142	GXB10142
10144	GXB10144/10410
10147	GXB10405
74187	82S226
74S188	82S23
74S189	74S189
74S89	74S89
74S200	74S200
74S201	74S201
74S209	82S11/93425A
74S270	82S230
74S287	82S129
74S288	82S123
74S289	3101A
74S301	74S301
74S309	82S10/93415A
74S370	82S231
74S387	82S126
74S472	82S146
74S473	82S147

** Not pin-for-pin compatible.

memories

cross reference

MOS

AMD	Signetics
2102	2102
	21F02
	21L02
9216	2617
AM1402APC	2502
AM1403A	2503
AM1404A	2504
AM1507	2517
AM1507T	2506
AM2505K	2505
AM2806HC	2512
AM2807PC	2524
AM2808PC	2525
AM2809	2521
AM2833PC	2533
AM9060	2680
P1101	2501

Electronic Arrays	Signetics
4600	2600
4900	2600

Fairchild	Signetics
2102	2102
	21F02
	21L02
3343	2521
3344	2522
3347	2532
3349	2518
3533	2533
F4720	HEF4720B

General Instruments	Signetics
2509	2509
2510	2510
2511	2511
2513	2513
2516	2516
2530	2530
2533	2533
2580	2580

Intel	Signetics
2101	2101
2102A	2102
	21F02
	21L02
	2102A
2102AL	2102AL
2107B	2680
2111	2111
2112	2112
2114	2614
2115	2115
2116A	2690
2125	2125
2308	2607
2316E	2616
2704	2704
2708	2607
	2708
C1402A	2502
C1403A	2503
M1404A	2504
M1405A	2505
P1101	2501

Intersil	Signetics
IM7501	2501
IM7552	2102
	21F02
	21L02
IM7712C	2512
IM7722C	2525
IM7780C	2532

Mostek	Signetics
29000	2600
MK1007P	2532
MK4007	2501
	25L01
MK4027	2627
MK4096	2660
MK4102	2102
	21F02
	21L02
MK4116	2690

Motorola	Signetics
6570	2609
6830	2608

National Semiconductor	Signetics
MM1101	2501
MM1402A	2502
MM1403A	2503
MM1404A	2504
MM1506H	2506
MM1507H	2517
MM2102	2102
	21F02
	21L02
MM2521	2521
MM2522	2522
MM5058	2533
MM5280	2680

Synertex	Signetics
2316B	2616
4600	2600

Texas Instruments	Signetics
TMS3112NC	2518
TMS3120NC	2532
TMS3128NC	2521
TMS3129NC	2522
TMS3133NC	2533
TMS4035	2102
	21F02
	21L02
TMS4030	2680
TMS4060	2680

Bipolar

Output structure: OC open collector
TS three-state

	capacity	type	output structure	no. of pins	t_{AA} max ns	input current µA	supply voltage V	max supply current mA	packages
TTL-RAM	16 x 4	**N3101A** *	OC	16	35	100	5	105	N, F
	16 x 4	**N74S89**	OC	16	50	100	5	105	N, F
	16 x 4	**N74S189**	TS	16	35	250	5	110	N, F
	16 x 4	**N82S25**	OC	16	50	100	5	105	N, F
	256 x 1	**N74S200**	TS	16	50	100	5	130	N, F
	256 x 1	**N74S201**	TS	16	50	100	5	130	N, F
	256 x 1	**N74S301**	OC	16	50	100	5	130	N, F
	256 x 1	**N82S16**	TS	16	50	100	5	115	N, F
	256 x 1	**N82S17**	OC	16	50	100	5	115	N, F
	256 x 1	**N82S116**	TS	16	40	100	5	115	N, F
	256 x 1	**N82S117**	OC	16	40	100	5	115	N, F
	64 x 9	**N82S09**	OC	28	45	100	5	190	N, I
	1024 x 1	**N82S10**	OC	16	45	100	5	170	N, F
	1024 x 1	**N82S11**	TS	16	45	100	5	170	N, F
	1024 x 1	**N82S110**	OC	16	35	100	5	170	N, F
	1024 x 1	**N82S111**	TS	16	35	100	5	170	N, F
	1024 x 1	**N93415A**	OC	16	45	100	5	170	N, F
	1024 x 1	**N93425A**	TS	16	45	100	5	170	N, F
	1024 x 1	**N82LS10** *	OC	16	60	100	5	60	N, F
	1024 x 1	**N82LS11** *	TS	16	60	100	5	60	N, F
	256 x 8	**N82S208**	TS	22	60	100	5	185	N, F
	256 x 9	**N82S210**	TS	24	60	100	5	185	N, F
	4096 x 1	**N82S400** *	OC	18	70	150	5	155	I
	4096 x 1	**N82S401** *	TS	18	70	150	5	155	I

* In development.

Military versions of industrial ICs with prefix N have S as a prefix.
Example: industrial version N82S25, military version S82S25.
The specifications shown below apply to industrial versions. There is generally some derating in specification for military versions due to the extended temperature range.
Temperature ranges

C 0 to 75 °C
M −55 to +125 °C

chip enable lines	temp. range	pin compatible types ▲ = fully compatible	second sourced by	pin diagram on page
1	M, C	82S25, 74S89	AMD, Intel, MMI, TI	
1	M, C	N3101A, 82S25	TI	B148
1	M, C	–	MMI, TI	
1	M, C	N3101A, 74S89	AMD, Fch, Harris, Intel, Intersil, MMI, Mot, National	
3	M, C	82S16, 82S116, 74S201 ▲	TI	
3	M, C	82S16, 82S116, 74S200 ▲	TI	
3	M, C	82S17, 82S117	Fch, Intersil, TI	B146
3	M, C	82S116, 74S200, 74S201	AMD, Fch, Intel, Intersil, MMI, Mot	
3	M, C	82S117, 82S301	AMD, Fch, Intel, Intersil, MMI	
3	C	82S16, 74S200, 74S201	Fch	B146
3	C	82S17, 74S301	Fch	B146
1	M, C	–	Fch, MMI	B149
1	M, C	82S110, 93415A ▲, 82LS10	AMD, Fch, Intersil, TI	B147
1	M, C	82S111, 93425A, 82LS11	AMD, Fch, Intersil, TI	B147
1	C	82S10, 93415A, 82LS10	Fch	
1	C	82S11, 93425A, 82LS11	Fch	
1	C	82S10 ▲, 82S110, 82LS10	AMD, Fch, TI	B147
1	C	82S11 ▲, 82S111, 82LS11	AMD, Fch, TI	
1	C	82S10, 93415A, 82S110	Fch	
1	C	82S11, 93425A, 82S111	Fch	B147
1	C	–	–	B149
1	C	–	–	B149
1	C	–	TI	B147
1	C	–	TI	B147

Bipolar

Output structure: OC open collector
TS three-state

	capacity	type	output structure	no. of pins	t_{AA} max ns	input current µA	supply voltage V	max supply current mA	packages
TTL-PROM	32 x 8	**N82S23**	OC	16	50	100	5	77	N, F
	32 x 8	**N82S123**	TS	16	50	100	5	77	N, F
	256 x 4	**N82S27**	OC	16	40	1600	5	140	F
	256 x 4	**N82S126**	OC	16	50	100	5	120	N, F
	256 x 4	**N82S129**	TS	16	50	100	5	120	N, F
	256 x 8	**N82S114**	TS	24	60	100	5	180	N, F
	512 x 4	**N82S130**	OC	16	50	100	5	140	N, F
	512 x 4	**N82S131**	TS	16	50	100	5	140	N, F
	512 x 8	**N82S115**	TS	24	60	100	5	180	N, F
	512 x 8	**N82S140**	OC	24	60	100	5	175	N, F
	512 x 8	**N82S141**	TS	24	60	100	5	175	N, F
	512 x 8	**N82S146** *	OC	20	45	–	5	–	N
	512 x 8	**N82S147** *	TS	20	45	–	5	–	N
	1024 x 4	**N82S136**	OC	18	60	100	5	140	F
	1024 x 4	**N82S137**	TS	18	60	100	5	140	F
	1024 x 8	**N82S180**	OC	24	70	100	5	150	F
	1024 x 8	**N82S181**	TS	24	70	100	5	150	F
	1024 x 8	**N82S2708**	TS	24	70	100	5	150	F
	2048 x 4	**N82S184**	OC	18	100	100	5	120	I
	2048 x 4	**N82S185**	TS	18	100	100	5	120	I
	2048 x 8	**N82S190**	OC	24	80	100	5	175	N, F
	2048 x 8	**N82S191**	TS	24	80	100	5	175	N, F

* In development.

Military versions of industrial ICs with prefix N have S as a prefix.
Example: industrial version N82S25, military version S82S25.
The specifications shown below apply to industrial versions. There is generally some derating in specification for military versions due to the extended temperature range.
Temperature ranges

C 0 to 75 °C
M −55 to +125 °C

chip enable lines	temp. range	pin compatible types ▲ = fully compatible	second sourced by	pin diagram on page
1	M, C	–	AMD, Harris, Intersil, MMI, National, TI	B143
1	M, C	–	AMD, Harris, Intersil, MMI, TI	B143
2	C	82S126, 82S226	–	B141
2	M, C	82S226 ▲, 82S27	AMD, Fch, Harris, Intel, Intersil, MMI, Mot, National, TI	B141
2	M, C	82S229 ▲	AMD, Fch, Harris, Intel, Intersil, MMI, National, TI	B141
2	M, C	82S214 ▲	MMI **	B143
1	M, C	82S230 ▲	Fch, Harris, Intel, Intersil, MMI	B141
1	M, C	82S231 ▲	Fch, Harris, Intel, Intersil, MMI	B141
2	M, C	82S215 ▲	Harris **	
4	M, C	82S240 ▲	Fch, Harris, Intel, Intersil, MMI	
4	M, C	82S241 ▲	Fch, Harris, Intel, Intersil, MMI	B144
1	C	–	MMI, TI **	
1	C	–	MMI, TI **	
2	M, C	–	Fch, Harris, Intel, Intersil, MMI	B142
2	M, C	–	Fch, Harris, Intel, Intersil, MMI	B142
4	M, C	82S280 ▲	MMI	B145
4	M, C	82S281 ▲	MMI	B145
1	M, C	–	MMI, (EPROM – Intel, Mot, TI)	B145
1	M, C	–	–	B142
1	M, C	–	–	B142
3	C	82S290 ▲	–	B145
3	C	82S291 ▲	–	B145

** Not pin-for-pin compatible.

memories

technical data

Bipolar

Output structure: OC open collector OE open emitter
TP totem pole TS three-state

	capacity	type	output structure	no. of pins	t_{AA} max	input current	supply voltage	max supply current	packages
					ns	µA	V	mA	
TTL-ROM	256 x 4	**N82S226**	OC	16	50	100	5	120	N, F
	256 x 4	**N82S229**	TS	16	50	100	5	120	N, F
	256 x 8	**N82S214**	TS	24	60	100	5	175	F
	512 x 4	**N82S230**	OC	16	50	100	5	135	F
	512 x 4	**N82S231**	TS	16	50	100	5	135	F
	512 x 8	**N82S215**	TS	24	60	100	5	175	F
	512 x 8	**N82S240**	OC	24	60	100	5	175	F
	512 x 8	**N82S241**	TS	24	60	100	5	175	F
	1024 x 4	**N8228**	TP	16	70	400	5	170	F, I
	1024 x 8	**N82S280**	OC	24	70	100	5	150	I
	1024 x 8	**N82S281**	TS	24	70	100	5	150	I
	2048 x 8	**N82S290**	OC	24	70	100	5	170	F
	2048 x 8	**N82S291**	TS	24	70	100	5	170	F
TTL-SAM	8 x 4	**N82S12**	OC	24	35	250	5	160	N, F
	8 x 4	**N82S112**	TS	24	35	250	5	160	N, F
TTL-WWRM	32 x 2	**N82S21**	OC	16	50	1600	5	130	N, F
TTL-FPLA	16 x 48 x 8	**N82S100**	TS	28	50	100	5	170	N, I
	16 x 48 x 8	**N82S101**	OC	28	50	100	5	170	N, I
	16 x 48 x 8	**N82S106**	OC	28	50	100	5	170	N, I
	16 x 48 x 8	**N82S107**	TS	28	50	100	5	170	N, I
TTL-FPGA	16 x 9	**N82S102**	OC	28	30	100	5	170	N, I
	16 x 9	**N82S103**	TS	28	30	100	5	170	N, I
TTL-PLA	16 x 48 x 8	**N82S200**	TS	28	50	100	5	170	N, I
	16 x 48 x 8	**N82S201**	OC	28	50	100	5	170	N, I
ECL-RAM	64 x 1	**GXB10140**	OE	16	15	265	5,2	80 (typ)	D, P
	64 x 1	**GXB10142**	OE	16	10	265	5,2	100	D, P
	64 x 1	**GXB10148**	OE	16	15	265	5,2	80 (typ)	D, P
	16 x 4	**GXB10145**	OE	16	–	220	5,2	145	D, P
	128 x 1	**GXB10405**	OE	16	15	200	5,2	110	E
	256 x 1	**GXB10144**	OE	16	30	200	5,2	112	D, E
	256 x 1	**GXB10410**	OE	16	35	220	5,2	125	E
	1024 x 1	**GXB10415** *	OE	16	25	–	5,2	–	E
ECL-PROM	32 x 8	**GXB10139**	OE	16	20	265	5,2	145	D
	256 x 4	**GXB10149**	OE	16	20	265	5,2	150	D, E
ECL-CAM	8 x 2	**GXB10155**	OE	18	13	220	5,2	140	E

* In development.

Military versions of industrial ICs with prefix N have S as a prefix.
Example: industrial version N82S25, military version S82S25.
The specifications shown below apply to industrial versions. There is generally some derating in specification for military versions due to the extended temperature range.

Temperature ranges

TTL – C – 0 to 75 °C
TTL – M – –55 to +125 °C
ECL – C – –30 to + 85 °C

chip enable lines	temp. range	pin compatible types ▲ = fully compatible	second sourced by	pin diagram on page
2	M, C	N82S126 ▲, N82S27	Fch, Intel, MMI, Mot, National, TI	B141
2	M, C	N82S129 ▲	Fch, MMI	B141
2	M, C	N82S114	–	B143
1	M, C	N82S130 ▲	Fch, Intel, MMI, TI	B141
1	M, C	N82S131 ▲	Fch, Intel, MMI, TI	B141
2	M, C	N82S115 ▲	–	B144
4	C	N82S140 ▲	–	B144
4	C	N82S141 ▲	Fch	B144
–	C	–	–	B142
4	M, C	N82S180 ▲	Fch, MMI	B145
4	M, C	N82S181 ▲	Fch, MMI	
3	C	N82S190 ▲	MMI	
3	C	N82S191 ▲	MMI	
2 wr. en.	C	–	–	B150
2 wr. en.	C	–	–	
–	C	–	–	B150
1	M, C	N82S200 ▲	AMD, MMI	B151
1	M, C	N82S201 ▲	AMD, MMI	
–	C	–	–	
–	C	–	–	
1	M, C	–	–	B151
1	M, C	–	–	
1	M, C	N82S100	–	B151
1	M, C	N82S101	–	
2	C	GXB10142, GXB10148	Mot	B146
2	C	GXB10140, GXB10148	Mot, TI	B146
2	C	GXB10140, GXB10142	Mot	B146
1	C	–	Fch, Mot	B148
–	C	–	Mot, TI	B146
3	C	GXB10410	Fch, Mot, TI	B146
3	C	GXB10144	Fch, Mot, TI	B146
–	C	–	Fch, Mot	B147
1	C	–	Mot	B143
1	C	–	Fch, Harris, MMI, Mot	B141
–	C	–	–	B150

memories

technical data

MOS

	capacity	type	no. of pins	t_{AA} typ ns	supply voltage V
Static RAM	256 x 1	**2501**	16	1000	+5, −9
	256 x 1	**25L01**	16	1000	+5, −12
	256 x 4	**2101**	22	450 – 1000	+5
	256 x 4	**2111**	18	450 – 1000	+5
	256 x 4	**2112**	16	450 – 1000	+5
	256 x 4	**2606**	16	750	+5
	256 x 4	**2606-1**	16	500	+5
	1024 x 1	**2102**	16	500 – 1000	+5
	1024 x 1	**21F02**	16	250 – 450	+5
	1024 x 1	**21L02**	16	400 – 1000	+5
	1024 x 1	**2102A/AL**	16	150 – 650	+5
	1024 x 1	**2115**	16	35 – 75	+5
	1024 x 1	**2125**	16	35 – 75	+5
	1024 x 4	**2614** *	18		+5
	1024 x 4	**2624** *	18		+5
	4096 x 1	**2613** *	18		+5
	4096 x 1	**2623** *	18		+5
LOCMOS static RAM	256 x 1	**HEF4720B(V)**	16	150 – 450	+3 to +15
Dynamic RAM	4096 x 1	**2660**	16	200 – 350	+12, +5, −5
	4096 x 1	**2680**	22	200 – 350	+12, +5, −5
	4096 x 1	**2627**	16	150 – 250	+12, +5, −5
	16384 x 1	**2690** *	16	150 – 250	+12, +5, −5
ROMs and character generators p-channel	512 x 8	**2530**	24	700	+5, −12
	2048 x 4	**2580**	24	950	+5, −12
	64 x 8 x 5	**2513**	24	600	+5, −12
	64 x 6 x 8	**2516**	24	600	+5, −12
	64 x 9 x 9	**2526**	24	700	+5, −12
n-channel	1024 x 8	**2607**	24	450	+5
	1024 x 8	**2608**	24	550	+5
	2048 x 8	**2600**	24	300	+5
	2048 x 8	**2616**	24	300	+5
	2048 x 8	**2617**	24	450	+5
	4096 x 8	**2632** *	24		+5
	4096 x 8	**2633** *	24		+5
	128 x 7 x 9	**2609**	24	500	+5
EPROM	4096	**2704**	24	450	+12, +5, −5
	8192	**2708**	24	450	+12, +5, −5

* In development.

Temperature range
C = 0 to +70 °C
XC = –40 to +85 °C

chip enable lines	temp. range	pin compatible types	second sourced by	pin diagram on page
–	C	25L01	AMD, Intel, Intersil, Mostek, National	B152
1	C	2501	Mostek	B152
2	C	–	Intel	B154
2	C	–	Intel	B154
1	C	–	Intel	B155
1	C	2606-1	–	B155
1	C	2606	–	B155
1	C	21F02, 21L02, 2102A/AL	AMD, Fch, Intel, Intersil, Mostek, National, TI	B152
1	C	2102, 21L02, 2102A/AL		B152
1	C	2102, 21F02, 2102A/AL		B152
1	C	2102, 21F02, 21L02	Intel	B152
1	C	2125	Intel	B153
1	C	2115	Intel	B153
–	C	2624	Intel	B155
–	C	2614	Intel	B155
–	C	2623	Intel	B153
–	C	2613	Intel	
1	XC	–	Fch	B152
1	C	–	Mostek	B156
1	C	–	AMD, Intel, National, TI	
1	C	–	Mostek	
1	C	–	Intel, Mostek	
1	C	–	GI	B157
4	C	–	GI	B158
1	C	–	GI	B160
1	C	–	GI	B160
1	C	–	–	B160
2	C	–	Intel	B157
4	C	–	Motorola	B157
2	C	–	Electronic Arrays, Mostek, Synertex	B158
3	C	–	Intel, Synertex	B159
3	C	–	AMD	B159
–	C	–	–	B159
–	C	–	will be industry standard	–
4	C	–	Motorola	B161
1	C	–	Intel	B161
1	C	–	Intel	

memories

technical data

MOS

Several types can be made available in Cerdip (F package) and metal ceramic (I package).

Static shift registers – one clock (TTL compatible)
– power supplies +5 and –12 V; 2509/10/11 also –5 V

capacity	type	output structure	on-chip recirculate	package leads	typ speed MHz	second sourced by	pin diagram on page
hex 32 bits	2518	bare drain	yes	N-16	3,0	Fch, TI	B162
hex 40 bits	2519	bare drain	yes	N-16	3,0	–	B162
dual 50 bits	2509	three-state	yes	N-14, K	3,0	GI	B162
quad 80 bits	2532	push-pull	yes	N-16	3,0	Fch, Intersil, Mostek, TI	B163
dual 100 bits	2510	three-state	yes	N-14, K	3,0	GI	B162
dual 128 bits	2521	push-pull	yes	N-8	3,0	AMD, Fch, National, TI	B163
dual 132 bits	2522	push-pull	yes	N-8	3,0	Fch, National, TI	B163
dual 200 bits	2511	three-state	yes	N-14, K	3,0	GI	B162
dual 240 bits	2529	push-pull	yes	N-8	3,0	–	B163
dual 250 bits	2528	push-pull	yes	N-8	3,0	–	B163
dual 256 bits	2527	push-pull	yes	N-8	3,0	–	B163
1024 bits	2533	push-pull	jumper	N-8	2,0	AMD, Fch, GI, National, TI	B163

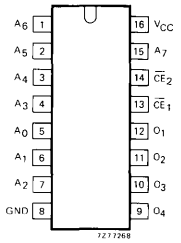
Dynamic shift registers – two clocks (not TTL compatible)
– power supplies +5 and –5 V

dual 100 bits	2517	20 kΩ PD	no	T, N-8	4,0	AMD, National	
dual 100 bits	2507	7,5 kΩ PD	no	T, N-8	4,0		B164
dual 100 bits	2506	bare drain	no	T, N-8	4,0	AMD, National	
quad 256 bits	2502	bare drain	no	N-16	10,0	AMD, Intel, National	B164
512 bits	2524	bare drain	yes	N-8	5,0	AMD	B164
512 bits	2505	bare drain	yes	K	3,0	AMD, Intel	B165
dual 512 bits	2503	bare drain	no	TA, N-8	10,0	AMD, Intel, National	B165
1024 bits	2525	bare drain	yes	N-8	5,0	AMD, Intersil	B164
1024 bits	2512	bare drain	yes	K	3,0	AMD, Intersil	B165
1024 bits	2504	bare drain	no	TA, N-8	10,0	AMD, Intel, National	B165

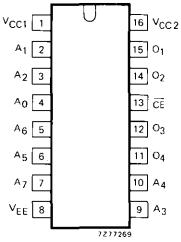
pin diagrams — second sources

Bipolar

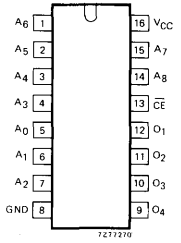
ROMs and PROMs 4 bits wide



type	capacity/output structure	second source
82S27	256 x 4 PROM/OC	–
82S126	256 x 4 PROM/OC	AMD 27S10, Fch 93417, Harris 1024A/7611, Intel 3601, Intersil 5603, MMI 6300-1, Mot 5005, National 8573, TI 74S387
82S129	256 x 4 PROM/TS	AMD 27S11, Fch 93427, Harris 1024/HM7610, Intel 3621, Intersil 5623A, MMI 6301-1, National 8574, TI 74S287
82S226	256 x 4 ROM/OC	Fch 93406, Intel 3301A, MMI 6200, Mot 4004A, National 74187,
82S229	256 x 4 ROM/TS	TI 74187 Fch 93467, MMI 6201



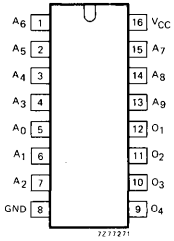
GXB10149	256 x 4 PROM/OE	Fch 10149, Harris HM7615, MMI 10149, Mot 10149



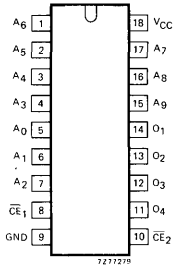
82S130	512 x 4 PROM/OC	Fch 93436, Harris HM7620, Intel 3602, Intersil 5604A, MMI 6305-1
82S131	512 x 4 PROM/TS	Fch 93446, Harris HM7621, Intel 3622, Intersil 5624, MMI 6306-1
82S230	512 x 4 ROM/OC	Fch 93431, Intel 3302, MMI 6205, TI 74S270
82S231	512 x 4 ROM/TS	Fch 93441, Intel 3322, MMI 6206, TI 74S370

Bipolar

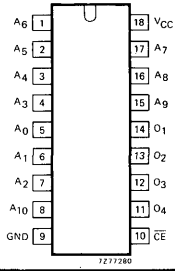
ROMs and PROMs 4 bits wide



type	capacity/output structure	second source
8228	1024 x 4 ROM/TP	–

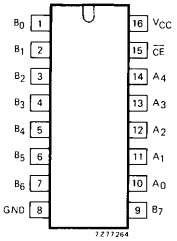


82S136	1024 x 4 PROM/OC	Fch 93452, Harris HM7642, Intel 3605, Intersil 56S06, MMI 6352
82S137	1024 x 4 PROM/TS	Fch 93453, Harris HM7643, Intel 3625, Intersil 56S26, MMI 6353

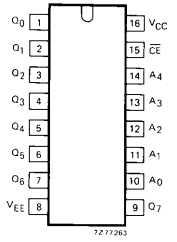


82S184	2048 x 4 PROM/OC	–
82S185	2048 x 4 PROM/TS	–

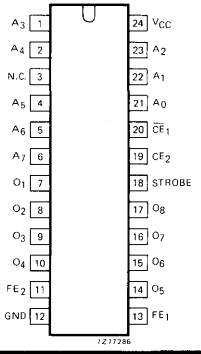
ROMs and PROMs 8 bits wide



type	capacity/output structure	second source
82S23	32 x 8 PROM/OC	AMD 27S08/27LS08, Harris HM7602/8256, Intersil 5600, MMI 6330, National 8588, TI 74S188
82S123	32 x 8 PROM/TS	AMD 27S09/27LS09, Harris HM7603, Intersil 5610, MMI 6331, TI 74S288



GXB10139	32 x 8 PROM/OE	Mot 10139

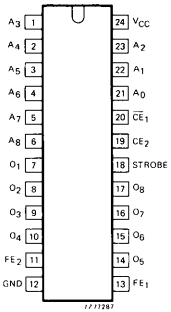


82S114	256 x 8 PROM/TS	MMI 6335**
82S214	256 x 8 ROM/TS	

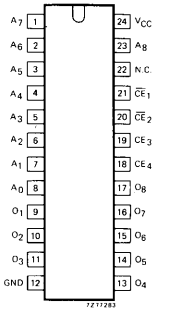
** Not pin-for-pin compatible.

Bipolar

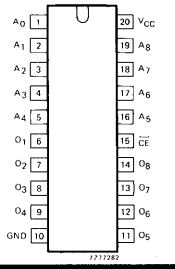
ROMs and PROMs 8 bits wide



type	capacity/output structure	second source
82S115	512 x 8 PROM/TS	Harris HM7644**/HM7699**
82S215	512 x 8 ROM/TS	—

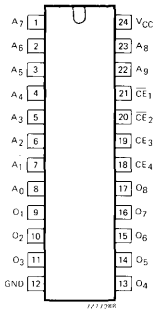


82S140	512 x 8 PROM/OC	Fch 93438, Harris HM7640, Intel 3604, Intersil 5605, MMI 6340
82S141	512 x 8 PROM/TS	Fch 93448, Harris HM7641, Intel 3624, Intersil 5625, MMI 6341
82S240	512 x 8 ROM/OC	—
82S241	512 x 8 ROM/TS	Fch 93442

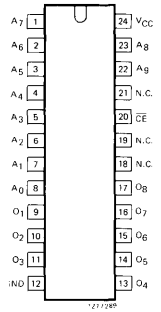


82S146	512 x 8 PROM/OC	MMI 6348, TI 74S472**
82S147	512 x 8 PROM/TS	MMI 6349, TI 74S473**

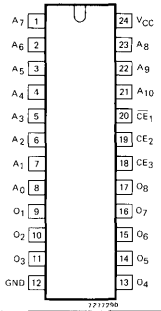
** Not pin-for-pin compatible.



type	capacity/output structure	second source
82S180	1024 x 8 PROM/OC	MMI 6380
82S181	1024 x 8 PROM/TS	MMI 6381
82S280	1024 x 8 ROM/OC	Fch 93454, MMI 6280
82S281	1024 x 8 ROM/TS	Fch 93464, MMI 6281



82S2708	1024 x 8 PROM/TS	MMI6385, EPROM – Intel 2708, Mot 68708, TI 2708



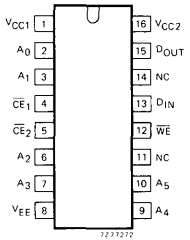
82S190	2048 x 8 PROM/OC	–
82S191	2048 x 8 PROM/TS	–
82S290	2048 x 8 ROM/OC	MMI 6275
82S291	2048 x 8 ROM/TS	MMI 6276

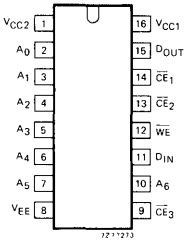
memories

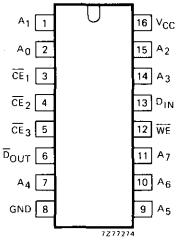
pin diagrams — second sources

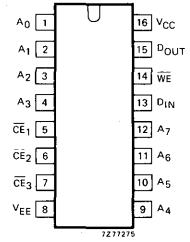
Bipolar

RAMs 1 bit wide



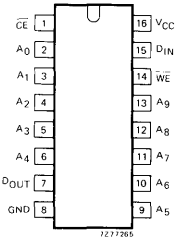




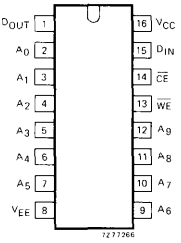


type	capacity/output structure	second source
GXB10140	64 x 1/OE	Mot 10140
GXB10142	64 x 1/OE	Mot 10142, TI 10142
GXB10148	64 x 1/OE	Mot 10148
GXB10405	128 x 1/OE	Mot 10147, TI 10147
74S200	256 x 1/TS	TI 74S200
74S201	256 x 1/TS	TI 74S201
74S301	256 x 1/OC	Fch 93410, Intersil 5503, TI 74S301
82S16	256 x 1/TS	AMD 2700/27LS00, Fch 93421, Intel 3106/3106A, Intersil 5523A, MMI 6531, Mot 4256
82S116	256 x 1/TS	Fch 93421A
82S17	256 x 1/OC	AMD 2701/27LS01, Fch 93411, Intel 3107/3107A, Intersil 5533A, MMI 6530
82S117	256 x 1/OC	Fch 93411A
GXB10144	256 x 1/OE	Fch 10410, Mot 10144, TI 10144
GXB10410	256 x 1/OE	Fch 10410, Mot 10144, TI 10144

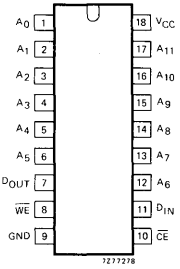
RAMs 1 bit wide



type	capacity/output structure	second source
82S10	1024 x 1/OC	AMD 2952, Fch 93415, Intersil 55S08(A), TI 74S309
82S110	1024 x 1/OC	Fch 93415B
82S11	1024 x 1/TS	AMD 2953, Fch 93425, Intersil 55S18(A), TI 74S209
82S111	1024 x 1/TS	Fch 93425B
82LS10	1024 x 1/OC	Fch 93L415
82LS11	1024 x 1/TS	Fch 93L425
93415A	1024 x 1/OC	AMD 2952, Fch 93415A, TI 74S309
93425A	1024 x 1/TS	AMD 2953, Fch 93425A, TI 74S209



GXB10415	1024 x 1/OE	Fch 10415, Mot 10146/10415



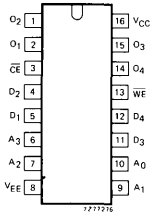
82S400	4096 x 1/OC	TI 2708
82S401	4096 x 1/TS	TI 2708

memories

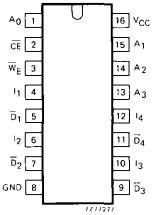
pin diagrams — second sources

Bipolar

RAMs 4 bits wide

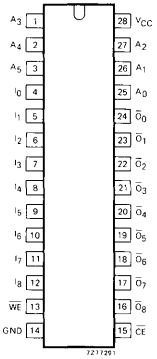


type	capacity/output structure	second source
GXB10145	16 x 4/OE	Fch 10145A, Mot 10145,

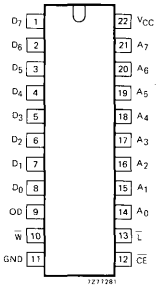


82S25	16 x 4/OC	AMD 3101, Fch 93403, Harris 0064, Intel 3101, Intersil 5501, MMI 6560, Mot 4064, National 86L99
74S89	16 x 4/OC	TI 74S89
74S189	16 x 4/TS	MMI 6561, TI 74S189
3101A	16 x 4/OC	AMD 3101A/27S02, Intel 3101A, MMI 6560, TI 74S289

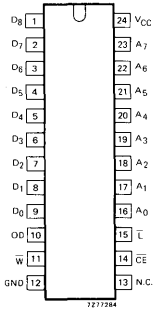
RAMs 1 byte (8 or 9 bits) wide



type	capacity/output structure	second source
82S09	64 x 9/OC	Fch 93419, MMI 6555



82S208	256 x 8/TS	–



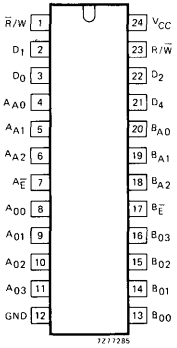
82S210	256 x 9/TS	–

memories

pin diagrams — second sources

Bipolar

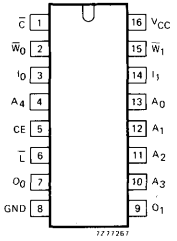
Specials (SAM, WWRM, CAM)



type	capacity/output structure	second source
82S12	8 x 4 SAM/OC	–
82S112	8 x 4 SAM/TS	–

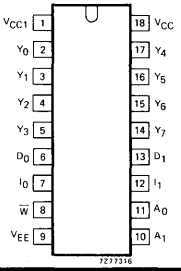
A Simultaneous Addressable Memory or multiport memory is one in which different locations can be selected at the same time.

The 82S12/112 SAM-element has two independent sets of address-decoders and outputs.



82S21 32 x 2 WWRM/OC –

A Write While Read Memory element is a RAM provided with output latches, in such a way that (read out) data may be retained in the latches either when the chip is disabled or when new information has to be written in the memory.

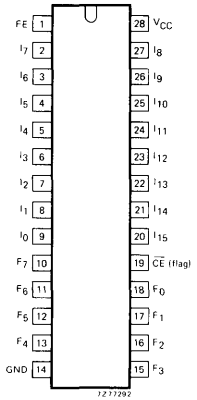


GXB10155 8 x 2 CAM/OE –

In a Content Addressable Memory or association memory the address information is associated with the memory content to search whether and/or in which location this information is stored; data is searched in parallel.

The normal functions of read-out and write-in can also be performed.

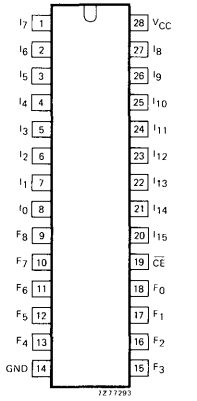
Specials (PLA, FPLA, FPGA)



type	capacity/output structure	second source
82S100	16 x 48 x 8 FPLA/TS	AMD 2981, MMI 82S100
82S101	16 x 48 x 8 FPLA/OC	AMD 2980, MMI 82S101
82S200	16 x 48 x 8 PLA/TS	–
82S201	16 x 48 x 8 PLA/OC	–
82S106	16 x 48 x 8 FPLA/OC	–
82S107	16 x 48 x 8 FPLA/TS	–

In the 82S106/107, the chip enable input is replaced by a "flag" output indicating whether a programmed product term is activated.

The Programmable Logic Array is a two level AND-OR/AND-NOR combinational logic element, consisting of a system of logic gates with programmable inputs and outputs in order to generate series of product-terms according to customer requirements. Programming can either be done during production (PLA) or by the customer in the field (FPLA).



82S102	16 x 9 FPGA/OC	–
82S103	16 x 9 FPGA/TS	–

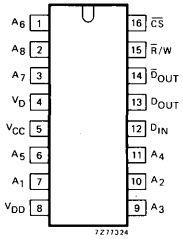
The Field Programmable Gate Array is a one-level AND/NAND logic element with programmable inputs and outputs to generate several AND/NAND functions according to customer requirements.

memories

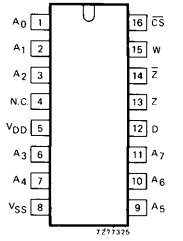
pin diagrams — second sources

MOS

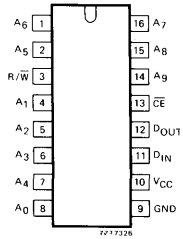
Static RAMs 1-bit wide



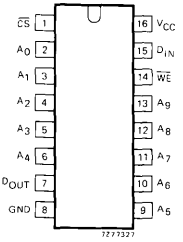
type	capacity	second source
2501	256 x 1	AMD P1101, Intel P1101, Intersil IM7501, Mostek MK4007, National MM1101
25L01	256 x 1	Mostek MK4007



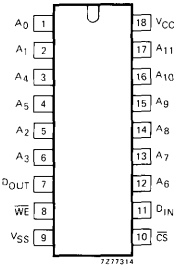
HEF4720B(V)	256 x 1	Fch F4720



2102	1024 x 1	AMD 2102, Fch 2102, Intel 2102A, Intersil IM7552, Mostek MK4102, National MM2102, TI TMS4035
21F02	1024 x 1	
21L02	1024 x 1	
2102A	1024 x 1	Intel 2102A
2102AL	1024 x 1	Intel 2102AL



type	capacity	second source
2115	1024 x 1	Intel 2115
2125	1024 x 1	Intel 2125



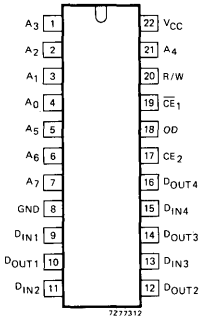
2613	4096 x 1	Intel
2623	4096 x 1	Intel

memories

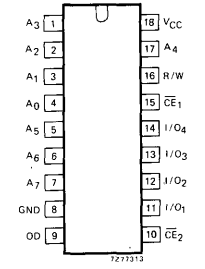
pin diagrams — second sources

MOS

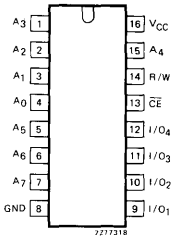
Static RAMs 4-bits wide



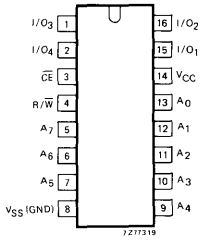
type	capacity	second source
2101	256 x 4	Intel 2101



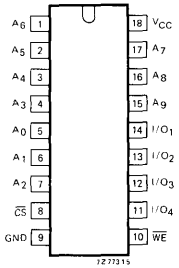
type	capacity	second source
2111	256 x 4	Intel 2111



type	capacity	second source
2112	256 x 4	Intel 2112



2606	256 x 4	–
2606-1	256 x 4	–



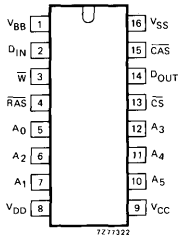
2614	1024 x 4	Intel 2114
2624	1024 x 4	Intel

memories

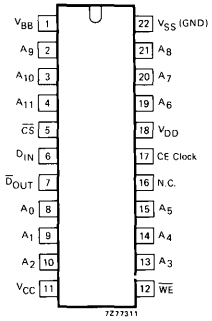
pin diagrams — second sources

MOS

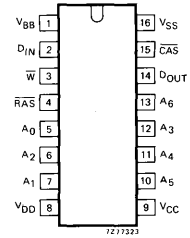
Dynamic RAMs 1-bit wide



type	capacity	second source
2627	4096 x 1	Mostek MK4027
2660	4096 x 1	Mostek MK4096

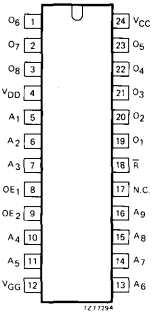


2680	4096 x 1	AMD 9060, Intel 2107B, National MM5280, TI TMS4060, TMS4030

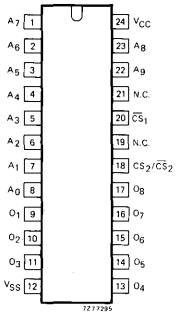


2690	16384 x 1	Intel 2116A, Mostek MK4116

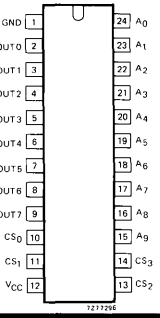
ROMs 8-bits wide



type	capacity	second source
2530	512 x 8	General 2530



2607	1024 x 8	Intel 2308, EPROM – Intel 2708



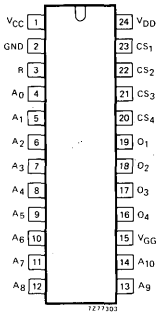
2608	1024 x 8	Motorola 6830

memories

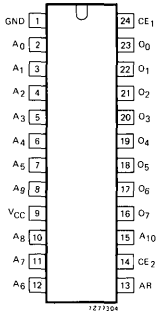
pin diagrams — second sources

MOS

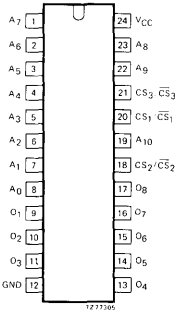
ROMs 4 and 8-bits wide



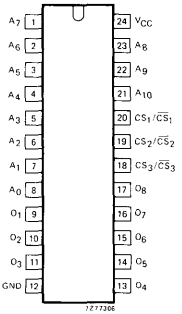
type	capacity	second source
2580	2048 x 4	General 2580



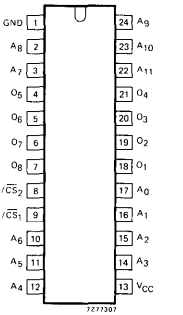
2600	2048 x 8	Electronic Arrays 4600 and 4900, Mostek 29000, Synertex 4600



type	capacity	second source
2616	2048 x 8	Intel 2316E, Synertex 2316B



2617	2048 x 8	AMD 9216



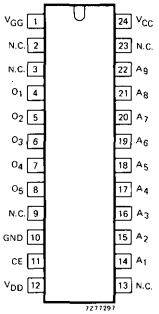
2632	4096 x 8	–

memories

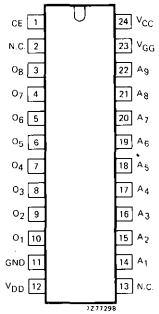
pin diagrams — second sources

MOS

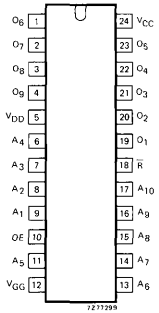
Character generators



type	capacity	second source
2513	64 x 8 x 5	General 2513

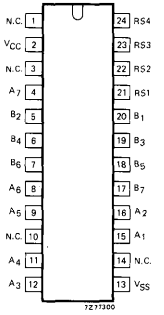


2516	64 x 6 x 8	General 2516

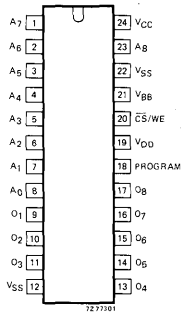


2526	64 x 9 x 9	–

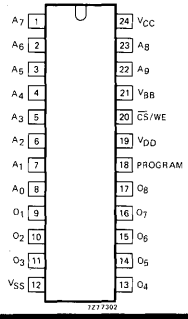
EPROMs



type	capacity	second source
2609	128 x 7 x 9	Motorola 6570



2704	4096	Intel 2704



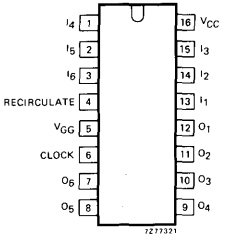
2708	8192	Intel 2708

memories

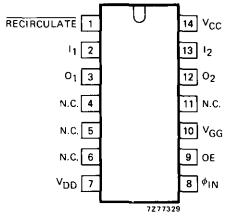
pin diagrams — second sources

MOS

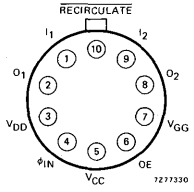
Static shift registers

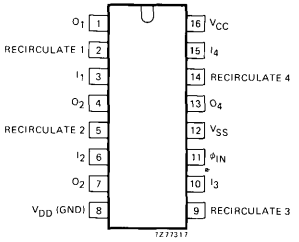


type	capacity	second source
2518	6 x 32	Fch 3349, TI TMS3112NC
2519	6 x 40	–

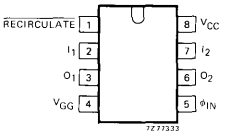


2509	2 x 50	General 2509
2510	2 x 100	General 2510
2511	2 x 200	General 2511

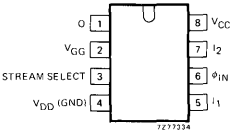




type	capacity	second source
2532	4 x 80	Fch 3347, Intersil IM7780C Mostek MK1007P, TI TMS3120NC



2521	2 x 128	AMD AM2809, Fch 3343, National MM2521, TI TMS3128NC
2522	2 x 132	Fch 3344, National MM2522, TI TMS3129NC
2529	2 x 240	–
2528	2 x 250	–
2527	2 x 256	–



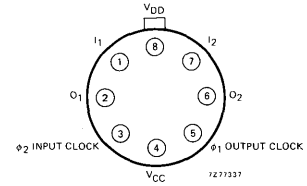
2533	1024	AMD AM2833PC, Fch 3533, General 2533, National MM5058, TI TMS3133NC

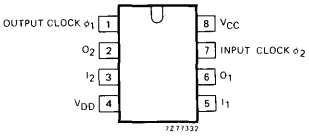
memories

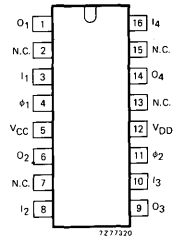
pin diagrams — second sources

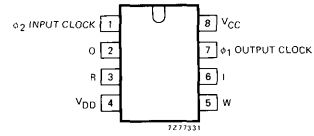
MOS

Dynamic shift registers

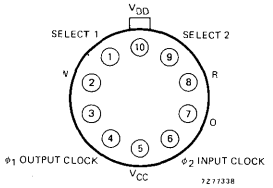




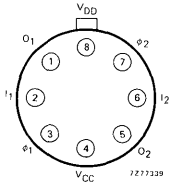


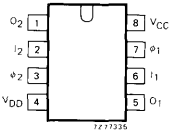


type	capacity	second source
2506	2 x 100	AMD AM1507T, National MM1506H
2507	2 x 100	–
2517	2 x 100	AMD AM1507, National MM1507H
2502	4 x 256	AMD AM1402APC, Intel C1402A, National MM1402A
2524	512	AMD AM2807PC
2525	1024	AMD AM2808PC, Intersil IM7722C

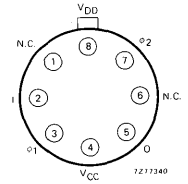


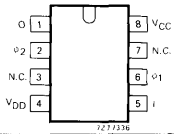
type	capacity	second source
2505	512	AMD AM2505K, Intel M1405A
2512	1024	AMD AM2806HC, Intersil IM7712C





2503	2 x 512	AMD AM1403A, Intel C1403A, National MM1403A





2504	1024	AMD AM1404A, Intel M1404A, National MM1404A

microprocessors

type index

cross reference

Type index

Bipolar		MOS	
AMD	**Signetics**	**National**	**Signetics**
2901A	N2901-1	2650	2650
Intel	**Signetics**		
3001	N3001		
3002	N3002		

technology	description	type	page
Bipolar	Cyclic Redundancy Check generator/checker	**8X01**	B170
	Control Store Sequencer	**8X02**	B171
	Microprocessor	**8X300**	B167
	Designers evaluation kit	**8X300KT100SK**	B168-B169
	Synchronous Input/Output Port – three-state	**N8T32**	B172
	Synchronous I/O Port – open collector	**N8T33**	B172
	Asynchronous I/O Port – open collector	**N8T35**	B172
	Asynchronous I/O Port – three-state	**N8T36**	B172
	Interface Vector Byte address programming kit	**8T32KT1000SK**	B173
	Bus Expander	**N8T39**	B174
	Microprocessor Central Processing Element	**N2901-1**	B175
	Microprogram Control Unit	**N3001**	B176
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	Prototyping kit	**3000KT1000**	B177
	Emulator kit	**3000KT8080SK**	B178-B179
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	8-bit Microprocessor	**2650A**	B180-B185
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	Microprocessor Prototyping Card	**2650PC1001**	B203-B205
	Adaptable Board Computer (ABC) assembled	**2650PC1500**	B206-B210
	Adaptable Board Computer (ABC) kit	**2650KT9500**	B206-B210
	Resident Assembler Board	**2650PC1600**	B211
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	Microprocessor Demonstration System	**2650DS2000**	B214-B216
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	2650 Assembler version 3.2	**2650AS1000/1100**	B223-B224
	2650 Simulator version 1.2	**2650SM1000/1100**	B225-B226
	Signetics Higher Level Language (PLμS)	**2650PL1000**	B227
	Microcomputer Prototype Development System	**TWIN**	B228-B230

8X300 fixed instruction set bipolar microprocessor

The Signetics 8X300 is a monolithic, high-speed microprocessor implemented with bipolar Schottky technology. As the central processing unit, CPU, it allows 16-bit instructions to be fetched, decoded and executed in 250 ns. A 250 ns instruction cycle requires maximum memory access of 65 ns, and maximum I/O device access of 35 ns.

Instructions operate on an 8-bit byte. Input data can be rotated and masked before being subjected to an arithmetic or logic operation. Output data can be shifted and merged with the input data before being applied to external logic. This allows 1 to 8-bit I/O and data memory fields to be accessed and the resulting data to be processed in a single instruction cycle.

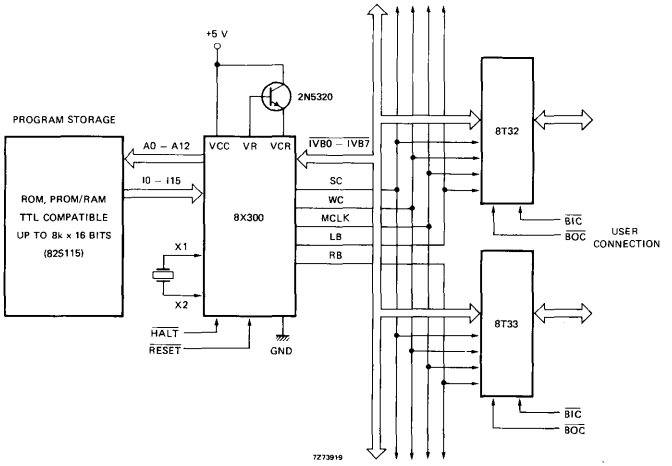
Features

- 185 ns instruction decode and execute delay (with Signetics 8T32/33 I/O port)
- Eight 8-bit working registers
- Single instruction access to 1-bit, 2-bit, 3-bit ... or 8-bit field on I/O bus
- Separate instruction address, instruction, and I/O data busses
- On-chip oscillator
- Bipolar Schottky technology
- TTL inputs and outputs
- Three-state output on I/O data bus
- +5 V operation from 0 to 70 °C

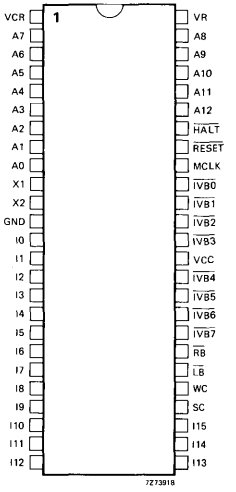
8X300 Instruction Set

- General purpose instruction set with substantial capabilities in arithmetic, byte and bit manipulation and I/O processing
- 16-bit instruction word
- 13 bits allow 8k program words
- Eight instruction classes: MOVE, ADD, AND, XOR, XEC, NZT, XMIT and JMP

Typical system configuration



Pin configuration – I package



8X300KT100SK designer's evaluation kit for fixed instruction bipolar microprocessor

The Signetics 8X300 Fixed Instruction Bipolar Microprocessor provides new levels of high performance to microprocessor applications not previously possible with MOS technology.

In the majority of cases, the choice of a bipolar microprocessor slice, as opposed to a MOS device, is based on speed. The 8X300 processor, combined with high-speed memory and I/O devices, is capable of executing all instructions in 250 ns.

The 8X300 is optimized for control and data movement applications. It has a 13-bit address bus for selecting instructions from program storage and a separate input bus for entering 16-bit instruction words. Data handling and I/O device addressing are accomplished via the 8-bit Interface Vector (IV) bus. The IV bus is supported by four additional control lines and a clock.

The unique features of the 8X300 IV bus and instruction set permit 8-bit parallel data to be rotated or masked before undergoing arithmetic or logic operations. Then, the data may be shifted and merged into any set of from 1 to 8 contiguous bits at the destination. The entire process of input, shifting, processing and output is done in 1 instruction cycle time. The 250 ns cycle time makes the 8X300 ideally suited for high-speed applications.

The evaluation board contains all the elements which a designer needs to judge the suitability of the 8X300 for his systems applications. Included with the 8X300 are 4 I/O ports for external device interface, 256 bytes of temporary (working) data storage, and 512 words of program storage, all properly connected to the 8X300 to allow immediate exercising of the board. For this purpose, the PROMs are preprogrammed with the I/O control, RAM control, and RAM integrity diagnostic programs. With the remaining PROM space, the designer may enter his own benchmark, test, or development routines.

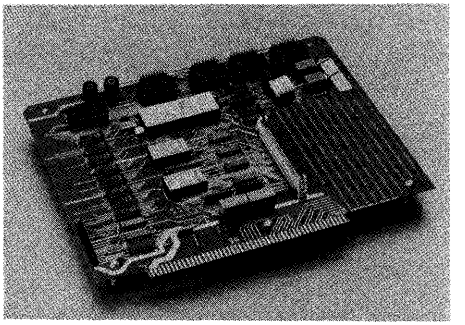
The board design allows complete flexibility in access to the address, instruction and IV busses as well as all controls and signals of the 8X300. The IV bus, I/O port user connection, clock signals control lines, address bus and instruction bus are wired to output pins, the board edge connector and flat cable connectors.

The board layout permits variations and/or expansions of the basic design. In addition to the access to all signals for transfer off the board, a wire wrap area is provided so that the designer may add to the board circuitry as he desires. The addition may include memory, additional interfaces, or special circuits which meet specific user requirements.

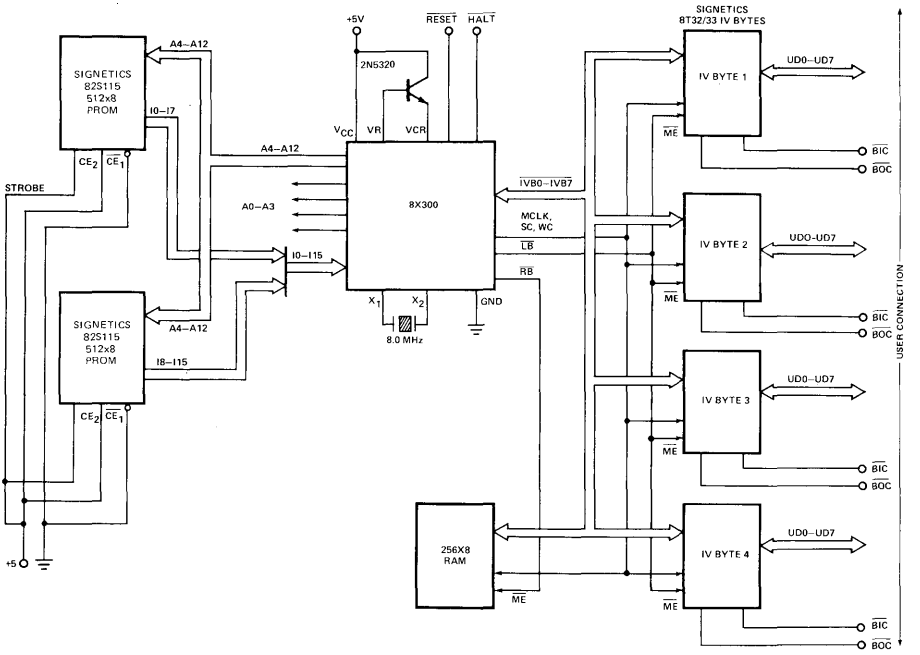
Controls are also provided for diagnostic and instructional purposes by allowing various operating modes. In the WAIT mode, the program may be single-stepped for ease of checkout. The one-shot instruction jamming allows control of the program start location, changes of program flow, changing or examining the internal registers, or testing of simple sequences. The repeated instruction jamming provides a means of repetitive execution of an instruction so that the I/O bus and the control lines may be examined without software changes. In both of these jam cases, the jammed instruction is selected by board-mounted switches.

Features

- 250 ns CPU with crystal
- 4 I/O ports (32 lines)
- 256 bytes data storage
- 512 words program storage
- run/wait control
- single step
- instruction jamming, one-shot instruction jam repeated jam
- all busses to output pins
- firmware diagnostics
- wire wrap area
- edge connector
- flat cable connectors
- wire wrap posts for bus lines



Assembled kit 8X300KT100SK



8X300 KIT CONFIGURATION

Contents

1 each 8X300
8 each 82S116 (256 x 1 RAM)
2 each 82S115 (512 x 8 PROM)
4 each 8T32 (addressable bidirectional I/O port)
1 each 8T31 (bidirectional I/O port)
2 each 8T26A (quad bus transceiver)
4 each 74157 (quad 2-input data selector)
2 each 7474 (dual D flip-flop)
2 each 7400 (quad NAND gate)
1 each 7427 (3-input NOR gate)
1 each p.c. board
miscellaneous parts
1 each introductory manual, assembly instructions, code listings and schematics

8X01 CRC generator/checker

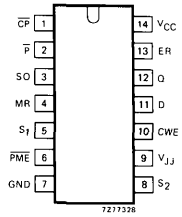
Objective specification

The CRC Generator/Checker circuit is used to provide an error detection capability for serial digital data handling system. The serial data stream is divided by a selected polynomial and the division remainder is transmitted at the end of the data stream as a Cyclic Redundancy Check Character (CRCC). When the data is received, the same calculation is performed. If the received message is error-free, the calculated remainder should satisfy a predetermined pattern. In most cases, the remainder is zero except in the case where Synchronous Data Link Control type protocols are used whereby the correct remainder is checked for 1111000010111000 ($X^0 - X^{15}$).

8 polynomials are provided and can be selected via a 3-bit control bus. Popular polynomials such as CRC-16 and CCITT are implemented. Polynomials can be programmed to start with either all zeros or all ones.

Automatic right justification for polynomials of degree less than 16 is provided.

Pin configuration – F, N packages



Features

- I^2L technology
- TTL inputs/outputs
- 5 MHz (max) data rate
- total power dissipation = 175 mW (max)
- V_{CC} = 5,0 V
- V_{JJ} = 1,0 V
- separate preset and reset controls
- SDLC specified pattern match
- automatic right justification

Typical applications

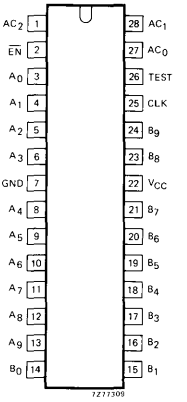
- floppy and other disc systems
- digital cassette and cartridge systems
- data communication systems

8X02 control store sequencer

Objective specification

The Signetics 8X02 is a Low-Power Schottky LSI device intended for use in high performance microprogrammed systems to control the fetch sequence of microinstructions. When combined with standard ROM or PROM, the 8X02 forms a powerful microprogrammed control section for computers, controllers, or sequenced logic.

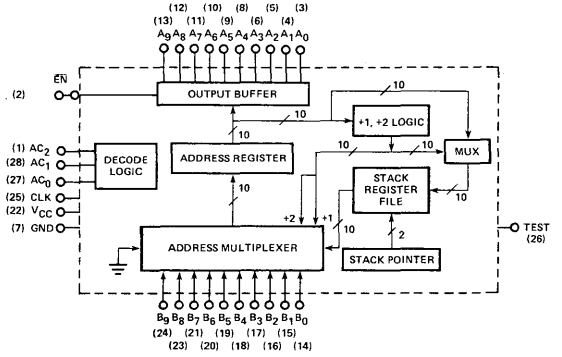
Pin configuration – N, I packages



Features

- low-power Schottky process
- 50 ns cycle time (typ)
- 1024 microinstruction addressability
- N-way branch
- 4-level stack register file (LIFO type)
- automatic push/pop stack operation
- "test & skip" operation on test input line
- 3-bit command code
- three-state buffered outputs
- auto-reset to address 0 during power up
- conditional branching, pop stack and push stack
- positive edge trigger (low-to-high transition)

Block diagram



8-bit latched addressable bidirectional I/O ports

8T32 Three-state, synchronous user port
8T33 Open collector, synchronous user port
8T35 Open collector, asynchronous user port
8T36 Three-state, asynchronous user port

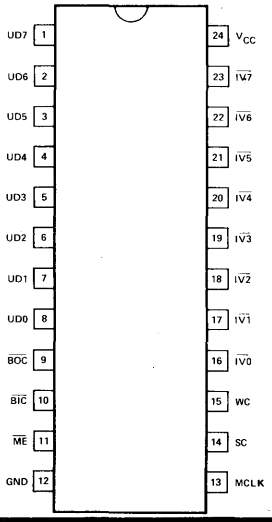
The interface vector (IV) byte is an 8-bit bidirectional data register designed to function as an I/O interface element in microprocessor systems. It contains 8 data latches accessible from either a microprocessor (IV) port or a user port. Separate I/O control is provided for each port. The 2 ports operate independently, except when both are attempting to input data into the IV byte. In this case, the user port has priority.

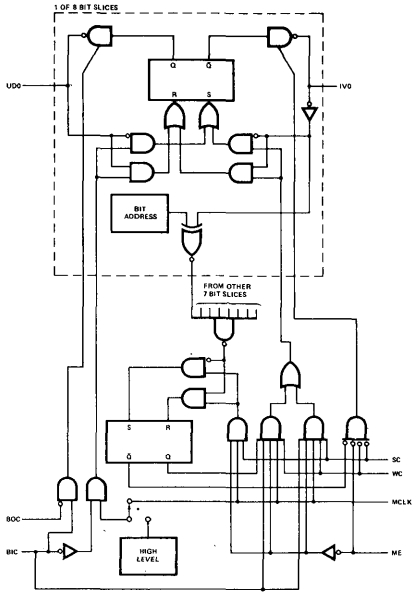
A unique feature of the 8T32/33/35/36 IV byte is the way in which it is addressed. Each IV byte has an 8-bit, field programmable address, which is used to enable the microprocessor port. When the SC control signal is HIGH, data at the microprocessor port is treated as an address. If the address matches the IV byte's internally programmed address, the microprocessor port is enabled, allowing data transfer through it.

Features

- A field-programmable address allows 1 of 512 IV bytes on a bus to be selected, without decoder
- Each byte has 2 ports, one to the user, the other to a microprocessor. IV bytes are completely bidirectional
- Ports are independent, with the user port having priority for data entry
- A selected IV byte de-selects itself when another IV byte address is sensed
- User data input available as synchronous (8T32, 8T33) or as asynchronous (8T35, 8T36) function
- The user data bus is available with three-state (8T32, 8T36) or open collector (8T33, 8T35) outputs
- At power up, the IV byte is not selected and the user port outputs are HIGH
- Three-state TTL outputs for high drive capability
- Directly compatible with the 8X300 interpreter
- Operates from a single 5 V power supply over a temperature range of 0 to 70 °C

F, N packages





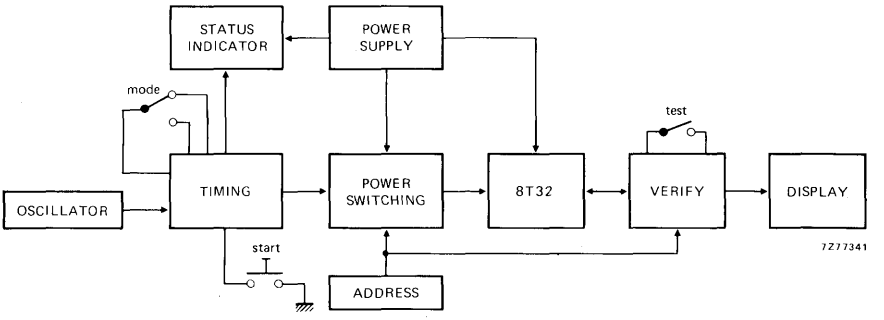
8T32KT1000SK programming kit for 8T32 addressable I/O port

This kit provides signals and levels required for programming the select addresses of the 8T32, 8T33, 8T35 and 8T36 I/O ports. Controls are provided for programming, testing and isolating the nichrome fuses which determine the device address.

Contents

1 x NE556A timer
2 x 74LS74 latch
1 x 74 LS93 counter
1 x 74LS154 decoder
4 x 8T26AB transceiver
2 x 74LS08 AND gate
1 x 8T80A NAND gate
1 x 74LS04 inverter
6 x 75450BA driver
2 x LM309DA regulator
printed circuit board and associated components

Block diagram



8T39 bus expander

The Bus Expander is specifically designed to increase the I/O capability of 8X300 systems previously limited by fan-out considerations. The bus expander serves as a buffer between the 8X300 and blocks of I/O devices. Each bus expander can buffer a block of 16 I/O ports while only adding a single load to the 8X300.

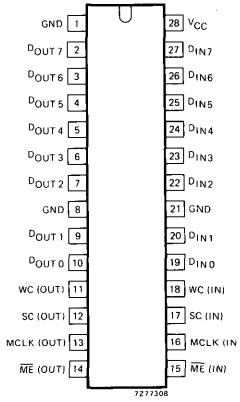
Features

- 15 ns propagation delay
- bidirectional
- three-state outputs on both ports
- pre programmed address range

Applications

The bus expander is not limited to use with the 8X300, but may be applied in any system which uses a combined address/data bus.

Pin configuration – I, N packages



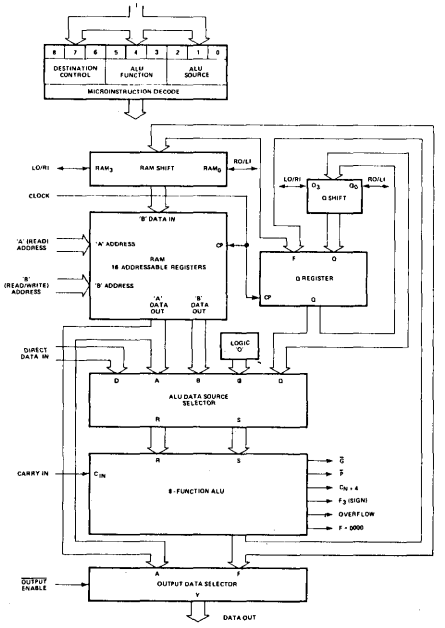
N2901-1 bipolar microprocessor processing element

Objective specification

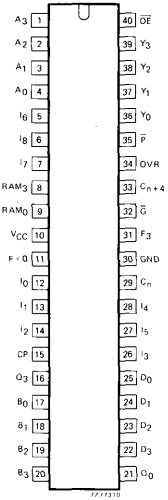
The 4-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPUs, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the 2901-1 will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The 9-bit microinstruction word is organized into 3 groups of 3 bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

Block diagram



Pin configuration – I, N packages



Features

- 80 ns cycle time
- 2-address architecture
  independent simultaneous access to 2 working registers saves machine cycles
- 8-function ALU
  performs addition, 2 subtraction operations, and 5 logic functions on 2 source operands
- flexible data source selection
  ALU data is selected from 5 source ports for a total of 203 source operand pairs for every ALU function
- left/right shift independent of ALU
  add and shift operations take only 1 cycle
- 4 status flags
  carry, overflow, zero, and negative
- expandable
  connect any number of 2901-1s together for longer word lengths
- microprogrammable
  3 groups of 3 bits each for source operand, ALU function, and destination control

Microprogram control unit N3001

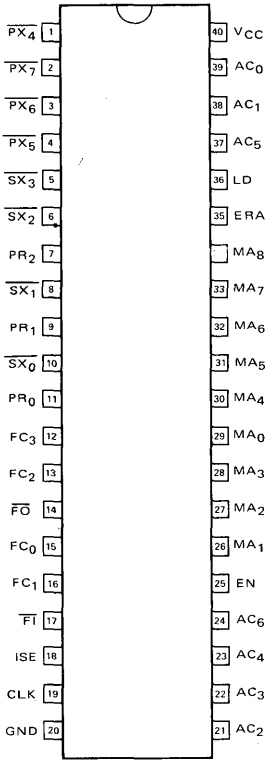
The N3001 MCU is one element of a bipolar microcomputer set. When used with the 3002, 74S182, ROM or PROM, a powerful microprogrammed computer can be implemented. The 3001 MCU controls the fetch sequence of microinstructions from the microprogram memory. Functions performed by the 3001 include:

- maintenance of microprogram address register
- selection of next microinstruction address
- decoding and testing of data supplied via several input busses
- saving and testing of carry output data from the central processing (CP) array
- control of carry/shift input data to the CP array
- control of microprogram interrupts

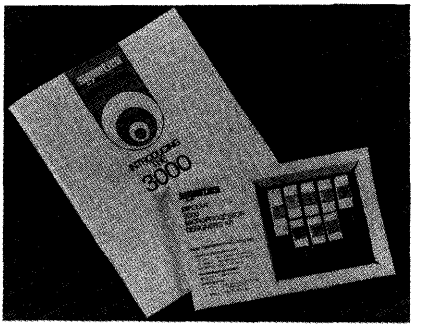
Features

- Schottky TTL process
- 45 ns cycle time (typ)
- direct addressing of standard bipolar PROM or ROM
- 512 microinstruction addressability
- advanced organization:
  9-bit microprogram address register and bus organized to address memory by row and column
  4-bit program latch
  2 flag registers
- 11 address control functions
- flight flag control functions:
  4 flag input functions
  4 flag output functions

Pin configuration – I, N packages



Central processing element N3002



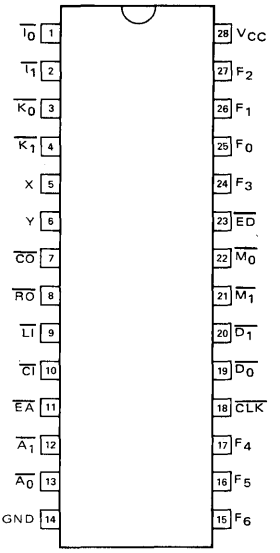
3000KT1000 prototyping kit.

The N3002 central processing element (CPE) is one part of a bipolar microcomputer set. The N3002 is organized as a 2-bit slice and performs the logical and arithmetic functions required by microinstructions. A system with any number of bits in a data word can be implemented by using multiple N3002s, the N3001 microcomputer control unit, the N74S182 carry look-ahead unit and ROM or PROM.

Features

- 45 ns cycle time (typ)
- easy expansion to multiple of 2 bits
- 11 general purpose registers
- full function accumulator
- useful functions include:
  - 2's complement arithmetic
  - logical AND, OR, NOT, EXCLUSIVE-NOR
  - increment, decrement
  - shift left/shift right
  - bit testing and zero detection
  - carry look-ahead generation
  - masking via K-bus
  - conditioned clocking allowing non-destructive testing of data in accumulator and scratchpad
- 3 input busses
- 2 output busses
- control bus

Pin configuration — I, N packages



3000KT1000 — 12 package prototyping kit

Central processing unit		
• microprogram control unit	N3001I	(1 x)
• central processing element	N3002I	(4 x)
• carry look-ahead	N74S182B	(1 x)
Microprogram memory		
• 256 x 8 PROM	N82S114I	(3 x)
Input/output		
• 8-bit bidirectional I/O port with latches	N8T31N	(1 x)
• 4-bit bus transceiver	N8T26AB	(2 x)

3000KT8080SK bipolar emulation kit for the 3000 series
8080A system emulator

The 8080 Emulation Kit is a microprogrammable microprocessor utilizing Schottky LSI components to implement an emulation of an Intel 8080A microcomputer system. The emulation is functionally equivalent to a microprocessor system incorporating the following Intel devices: 8080A, 8228, 8224 and 8212. The kit provides the standard address, data, status and control busses as defined in the Intel 8080 Microcomputer System Manual. Since the kit uses bipolar LSI elements, the emulator lacks the two-phase non-overlapping clock. Furthermore, those signals emanating from the 8080 during SYNC time are not provided, but rather the useful status signals provided by the 8228 system controller are implemented. The emulation also provides an extension of the 8228 operation during multi-byte interrupts. This is realized by allowing any 8080 program branch instruction to be inserted during interrupts rather than restricting multi-byte instructions to CALL during interrupts. Finally, a non-standard status signal, RTRAP, is provided which indicates that the present instruction is a reserved or undefined instruction. After this indication, the processor will enter the normal HALT routine and await an interrupt. (Intel 8080A operation during undefined instructions is undefined.) Thus all 12 of the unused instructions in the 8080 instruction set are reserved for future instruction set expansion. These unused codes may be used at any time to extend the usual instruction set without requiring any reprogramming of the bipolar PROMs used for microprogram memory. Finally, the emulator is fully static so that the clock may be adjusted from a typical cycle time of 150 ns to d.c.

The kit contains all the parts necessary to construct the emulator and includes preprogrammed PROMs. The kit is designed to be assembled by a skilled technician in about 8 hours.

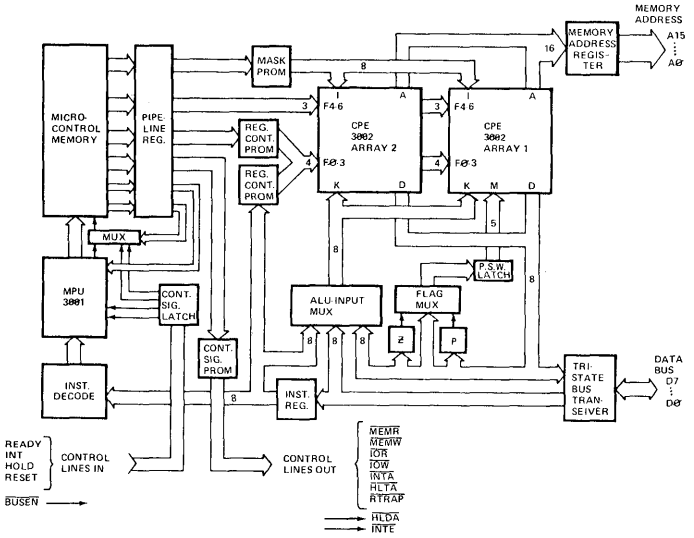
Features

- full emulation of 8080A system
- speed increase by factor of 2 to 9,2 over 8080A system
- static operation; microcycle time d.c. to 150 ns
- operation from single +5 V supply
- executes all 8080 instructions
- hardware multiply and divide
- microprogram expandable
- includes single-phase clock
- full vectored interrupt to any location within 64k memory

Kit contents

1 each	N74123
1 each	N3001
8 each	N3002
7 each	N82S115
1 each	N82S23
2 each	N82S123
2 each	N82S126
3 each	N8263
3 each	N74S182
1 each	N74S280
2 each	N7475
1 each	DM8613
11 each	N74S174
2 each	N8T28
3 each	N8T97
1 each	N74S153
2 each	N74S157
1 each	N7400
1 each	N74S02
3 each	N74S04
1 each	N74S08
1 each	N74S10
1 each	N74S133
2 each	resistor networks 1 kΩ, 16 pin
1 each	P.C. board
1 each	manual
1 each	schematic
1 each	set of microprogram listings
plus:	over 25 miscellaneous resistors, capacitors and other parts

Block diagram



8-bit MOS microprocessors 2650, 2650A

The 2650 processor is a general purpose, single chip, fixed instruction set, parallel 8-bit binary processor. It can perform any data manipulations through execution of a stored sequence of machine instructions. The processor has been designed to closely resemble conventional binary computers, but executes variable length instructions of one to three bytes in length. BCD arithmetic is made possible through use of a special "DAR" machine instruction.

The 2650 is manufactured using Signetics' n-channel silicon gate MOS technology. N-channel provides high carrier mobility for increased speed and also allows the use of a single 5 V power supply. Silicon gate provides for better density and speed. Standard 40-pin dual in-line packages are used for the processor.

The 2650 contains a total of seven general purpose registers, each eight bits long. They may be used as a source or destination for arithmetic operations, as index registers and for I/O transfers.

The processor can address up to 32 768 bytes of memory in four pages of 8 192 bytes each. Processor instructions are one, two or three bytes long, depending on the instruction. Variable length instructions tend to conserve memory space since a one or two-byte instruction may often be used rather then a three-byte instruction. The first byte of each instruction always specifies the operation to be performed and the addressing mode to be used. Most instructions use six of the first eight bits for this purpose, with the remaining two bits forming the register field. Some instructions use the full eight bits as an operation code.

The most complex direct instruction is three bytes long and takes 9,6 μs to execute assuming that the processor is running at its maximum clock rate and has an associated memory with cycle and access times of 620 ns or less. The minimum instruction execution time is 4,8 μs.

The clock input to the processor is a single phase pulse train and uses only one interface pin. It requires a normal TTL voltage swing, so no special clock driver is required.

The Data Bus and Address signals are three-state to provide convenience in system design. Memory and I/O interface signals are synchronous so that Direct Memory Access (DMA) and multiprocessor operations are easy to implement.

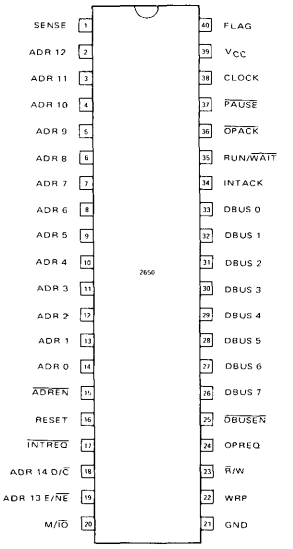
The interrupt mechanism is implemented as a single level, address vectoring type. Address vectoring means that an interrupting device can force the processor to execute code at a device-determined location in memory.

The 2650A is a functional equivalent of the 2650 with a new mask design which provides improved device-operating margins. Both versions are pin-for-pin compatible.

Features

- general purpose processor
- single chip
- fixed instruction set
- parallel 8-bit binary operations
- 40-pin dual in-line package
- n-channel silicon gate MOS technology
- TTL compatible inputs and outputs
- single power supply of +5 V
- seven general purpose registers
- return address stack, 8 deep, on chip
- 32k byte addressing range
- separate address and data lines
- variable length instructions of 1, 2 or 3 bytes
- 75 instructions
- machine cycle time of 2,4 μs at clock frequency of 1,25 MHz
- direct instructions take 2, 3, or 4 cycles
- single phase TTL level clock input
- static logic
- three-state output buses
- register, immediate, relative, absolute, indirect, and indexed addressing modes
- vector interrupt format

Pin configuration — I package



Addressing modes

The 2650 processor can develop addresses in eight ways:

- register addressing
- immediate addressing
- relative addressing
- relative, indirect addressing
- absolute addressing
- absolute, indirect addressing
- absolute, indexed addressing
- absolute, indirect, indexed addressing

Interface signal definition

ADR0-ADR12 – The low order 13 bits of address for memory access are on these pins. ADR0-ADR7 are also used in two-byte I/O instructions. These outputs are three-state buffers controlled by ADREN.

ADR13-E/$\overline{NE}$ – This multiplexed output signal delivers the ADR13 address bit when M/IO is in the M phase or discriminates between Extended and Non-Extended I/O instructions when M/IO is in the I/O phase.

ADR14-D/$\overline{C}$ – Address 14 or Data/Control is a multiplexed output signal. This pin delivers the ADR14 address bit when M/IO is in the M phase or discriminates between Data and Control I/O instructions when M/IO is in the I/O phase.

$\overline{ADREN}$ – Address Bus Enable is an input providing the external control for the ADR0-ADR12 three-state buffer drivers.

DBUS0-DBUS7 – This is the 8-bit, bidirectional three-state bus over which data is communicated into or out of the processor.

$\overline{DBUSEN}$ – Data Bus Enable is an input that controls the three-state buffer drivers for DBUS0 to DBUS7.

OPREQ – Operation Request is an output signal that informs external devices that the information on other output pins is valid.

$\overline{OPACK}$ – Operation Acknowledge is an input which is used by external devices to end an I/O or memory signalling sequence.

M/$\overline{IO}$ – Memory/Input-Output. This output informs external devices whether Memory or Input/Output functions are being performed.

$\overline{R}$/W – This output signal describes an I/O or memory operation as Read or Write, and defines whether the bidirectional DBUS is transmitting or receiving.

WRP – This Write Pulse is generated during write sequences and may be used to strobe memory or I/O devices.

SENSE – Is an input, independent of the other I/O signals, that provides a direct input to the processor.

FLAG – This pin provides a direct output signal that is completely independent of the other I/O signals.

$\overline{INTREQ}$ – Interrupt Request. This input is used by external devices to force the processor into the interrupt sequence.

INTACK – Interrupt Acknowledge is the signal used by the processor to inform external devices that it has entered an interrupt sequence.

$\overline{PAUSE}$ – Pause is used to temporarily stop the processor at the end of the current instruction. It may stop processing for an indefinite length of time and is available to use for DMA (Direct Memory Access).

RUN/$\overline{WAIT}$ – Informs external circuits as to the Run/Wait status of the 2650 processor.

RESET – Is an input that resets the program counter to zero and clears the interrupt inhibit bit.

CLOCK – This is the only clock input to the processor. It accepts standard TTL levels.

V_{CC} – +5 V power.

GND – The logic and power supply ground for the processor.

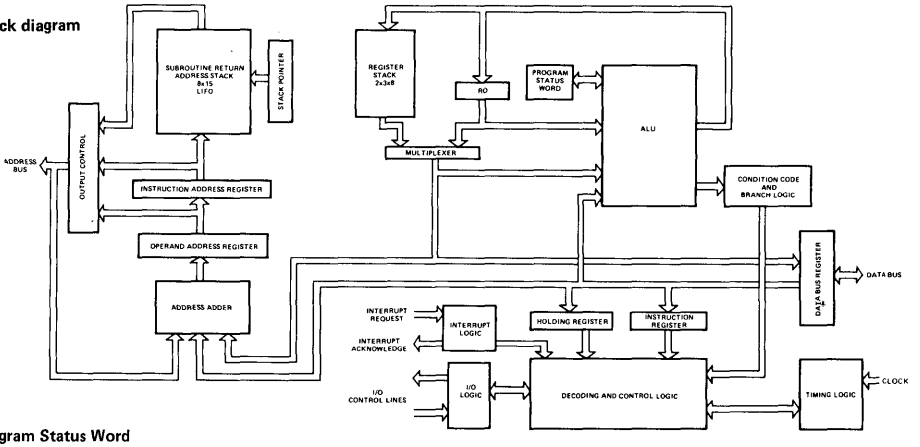
Processor hardware architecture

A block diagram of the processor is shown below. The first, second, and third bytes of instructions are read into the processor on the data bus and loaded into the Instruction Register, Holding Register, and Data Bus Register, respectively. The instructions are decoded through a combination of ROM and random logic.

The ALU performs arithmetic, Boolean, and combinatorial shifting functions. It operates on eight bits in parallel and utilizes carry-look-ahead logic. A second adder is used to increment the instruction address register and to calculate operand addresses for the indexed and relative addressing modes. This separate address adder allows complex addressing modes to be implemented with no increase in instruction execution time.

The General Purpose Register Stack and the Subroutine Return Address Stack are implemented with static RAM cells. The Register Stack consists of seven 8-bit registers. The Subroutine Stack can contain eight 15-bit addresses, thereby allowing eight levels of subroutine nesting. Placing the Subroutine Stack on the chip allows efficient ROM-only systems to be implemented in some applications. Separate 15-bit Instruction Address and Operand Address Registers are provided. The 2650 is an 8-bit binary processor with BCD capability.

Block diagram



Program Status Word

The Program Status Word (PSW) increases the flexibility and processing power of the 2650. The PSW is a special purpose register within the processor that contains status and control bits.

It is divided into two registers called the Program Status Upper (PSU) and Program Status Lower (PSL). The PSW bits may be tested, loaded, stored, preset, or cleared using the instructions which affect the PSW. The bits are utilized as follows:

PSU

7	6	5	4	3	2	1	0
S	F	II	Not Used	Not Used	SP2	SP1	SP0

S Sense
F Flag
II Interrupt Inhibit
SP2 Stack Pointer Two
SP1 Stack Pointer One
SP0 Stack Pointer Zero

PSL

7	6	5	4	3	2	1	0
CC1	CC0	IDC	RS	WC	OVF	COM	C

CC1 Condition Code One
CC0 Condition Code Zero
IDC Interdigit Carry
RS Register Bank Select
WC With/Without Carry
OVF Overflow
COM Logical/Arith. Compare
C Carry/Borrow

Instruction set

	mnemonic		op code	format*	description of operation	affects	cycles
Load/Store	LOD	Z	000 000	1Z	Load Register Zero	CC (Note 1)	2
		I	000 001	2I	Load Immediate	CC (Note 1)	2
		R	000 010	2R	Load Relative	CC (Note 1)	3
		A	000 011	3A	Load Absolute	CC (Note 1)	4
	STR	Z	110 000	1Z	Store Register Zero ($r \neq 0$)	CC (Note 1)	2
		R	110 010	2R	Store Relative	–	3
		A	110 011	3A	Store Absolute	–	4
Arithmetic	ADD	Z	100 000	1Z	Add to Register Zero w/wo Carry	C, CC (Note 1), IDC, OVF	2
		I	100 001	2I	Add Immediate w/wo Carry	C, CC (Note 1), IDC, OVF	2
		R	100 010	2R	Add Relative w/wo Carry	C, CC (Note 1), IDC, OVF	3
		A	100 011	3A	Add Absolute w/wo Carry	C, CC (Note 1), IDC, OVF	4
	SUB	Z	101 000	1Z	Subtract from Register Zero w/wo Borrow	C, CC (Note 1), IDC, OVF	2
		I	101 001	2I	Subtract Immediate w/wo Borrow	C, CC (Note 1), IDC, OVF	2
		R	101 010	2R	Subtract Relative w/wo Borrow	C, CC (Note 1), IDC, OVF	3
		A	101 011	3A	Subtract Absolute w/wo Borrow	C, CC (Note 1), IDC, OVF	4
	DAR		100 101	1Z	Decimal Adjust Register	CC (Note 2)	3
Logical	AND	Z	010 000	1Z	AND to Register Zero ($r \neq 0$)	CC (Note 1)	2
		I	010 001	2I	AND Immediate	CC (Note 1)	2
		R	010 010	2R	AND Relative	CC (Note 1)	3
		A	010 011	3A	AND Absolute	CC (Note1)	4
	IOR	Z	011 000	1Z	Inclusive OR to Register Zero	CC (Note 1)	2
		I	011 001	2I	Inclusive OR Immediate	CC (Note 1)	2
		R	011 010	2R	Inclusive OR Relative	CC (Note 1)	3
		A	011 011	3A	Inclusive OR Absolute	CC (Note 1)	4
	EOR	Z	001 000	1Z	Exclusive OR to Register Zero	CC (Note 1)	2
		I	001 001	2I	Exclusive OR Immediate	CC (Note 1)	2
		R	001 010	2R	Exclusive OR Relative	CC (Note 1)	3
		A	001 011	3A	Exclusive OR Absolute	CC (Note 1)	4
Compare	COM	Z	111 000	1Z	Compare to Register Zero Arithmetic/Logical	CC (Note 3)	2
		I	111 001	2I	Compare Immediate Arithmetic/Logical	CC (Note 4)	2
		R	111 010	2R	Compare Relative Arithmetic/Logical	CC (Note 4)	3
		A	111 011	3A	Compare Absolute Arithmetic/Logical	CC (Note 4)	4
Rotate	RRR		010 100	1Z	Rotate Register Right w/wo Carry	C, CC, IDC, OVF	2
	RRL		110 100	1Z	Rotate Register Left w/wo Carry	C, CC, IDC, OVF	2
Branch	BCT	R	000 110	2R	Branch On Condition True Relative	–	3
		A	000 111	3B	Branch On Condition True Absolute	–	3
	BCF	R	100 110	2R	Branch On Condition False Relative	–	3
		A	100 111	3B	Branch On Condition False Absolute	–	3
	BRN	R	010 110	2R	Branch On Register Non-Zero Relative	–	3
		A	010 111	3B	Branch On Register Non-Zero Absolute	–	3
	BIR	R	110 110	2R	Branch On Incrementing Register Relative	–	3
		A	110 111	3B	Branch On Incrementing Register Absolute	–	3

	mnemonic		op code	format*	description of operation	affects	cycles
Branch	BDR	R	111 110	2R	Branch On Decrementing Register Relative	—	3
		A	111 111	3B	Branch On Decrementing Register Absolute	—	3
	ZBRR		100 110 11	2ER	Zero Branch Relative, Unconditional	—	3
	BXA		100 111 11	3EB	Branch Indexed Absolute, Unconditional (Note 5)	—	3
Subroutine branch/return	BST	R	001 110	2R	Branch To Subroutine On Condition True, Relative	SP	3
		A	001 111	3B	Branch To Subroutine On Condition True, Absolute	SP	3
	BSF	R	101 110	2R	Branch To Subroutine On Condition False, Relative	SP	3
		A	101 111	3B	Branch To Subroutine On Condition False, Absolute	SP	3
	BSN	R	011 110	2R	Branch To Subroutine On Non-Zero Register, Relative	SP	3
		A	011 111	3B	Branch To Subroutine On Non-Zero Register, Absolute	SP	3
	ZBSR		101 110 11	2ER	Zero Branch To Subroutine Relative, Unconditional	SP	3
	BSXA		101 111 11	3EB	Branch To Subroutine, Indexed, Absolute Unconditional (Note 5)	SP	3
	RET	C	000 101	1Z	Return From Subroutine, Conditional	SP	3
		E	001 101	1Z	Return From Subroutine and Enable Interrupt, Conditional	SP, II	3
Input/Output	WRTD		111 100	1Z	Write Data	—	2
	REDD		011 100	1Z	Read Data	CC (Note 1)	2
	WRTC		101 100	1Z	Write Control	—	2
	REDC		001 100	1Z	Read Control	CC (Note 1)	2
	WRTE		110 101	2I	Write Extended	—	3
	REDE		010 101	2I	Read Extended	CC (Note 1)	3
Misc.	HALT		010 000 00	1E	Halt, Enter Wait State	—	2
	NOP		110 000 00	1E	No Operation	—	2
	TMI		111 101	2I	Test Under Mask Immediate	CC (Note 6)	3
Program status	LPS	U	100 100 10	1E	Load Program Status, Upper	F, II, SP	2
		L	100 100 11	1E	Load Program Status, Lower	CC, IDC, RS, WC, OVF, COM, C	2
	SPS	U	000 100 10	1E	Store Program Status, Upper	CC (Note 1)	2
		L	000 100 11	1E	Store Program Status, Lower	CC (Note 1)	2
	CPS	U	011 101 00	2EI	Clear Program Status, Upper, Masked	F, II, SP	3
		L	011 101 01	2EI	Clear Program Status, Lower, Masked	CC, IDC, RS, WC, OVF, COM, C	3
	PPS	U	011 101 10	2EI	Preset Program Status, Upper, Masked	F, II, SP	3
		L	011 101 11	2EI	Preset Program Status, Lower, Masked	CC, IDC, RS, WC, OVF, COM, C	3
	TPS	U	101 101 00	2EI	Test Program Status, Upper, Masked	CC (Note 6)	3
		L	101 101 01	2EI	Test Program Status, Lower, Masked	CC (Note 6)	3

* Format code: The number indicates the number of bytes. The letter(s) indicate the format type(s).

Notes:

1. Condition code (CC1, CC0): 01 if positive, 00 if zero, 10 if negative.
2. Condition code is set to a meaningless value.
3. Condition code (CC1, CC0): 01 if R0 > r, 00 if R0 = r, 10 if R0 < r.
4. Condition code (CC1, CC0): 01 if r > V, 00 if r = V, 10 if r < V.
5. Index register must be register 3 or 3'.
6. Condition code (CC1, CC0): 00 if all selected bits are 1s, 10 if not all selected bits are 1s.

Programmable Communications Interface (PCI) 2651

Applications

- intelligent terminals
- network processors
- front end processors
- remote data concentrators
- computer to computer links
- serial peripherals

The Signetics 2651 PCI is a universal synchronous/asynchronous data communications controller chip designed for microcomputer systems. It interfaces directly to the Signetics 2650 microprocessor and may be used in a polled or interrupt driven system environment. The 2651 accepts programmed instructions from the microprocessor and supports many serial data communication disciplines, synchronous and asynchronous, in the full or half-duplex mode.

The PCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The 2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

The PCI is constructed using Signetics' n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.

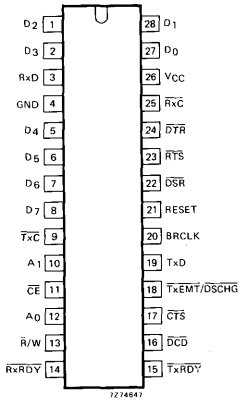
Features

- Synchronous operation
  5 to 8-bit characters
  single or double SYN operation
  internal character synchronization
  transparent or non-transparent mode
  automatic SYN or DLE-SYN insertion
  SYN or DLE stripping
  odd, even, or no parity
  local or remote maintenance loop back mode
  baud rate: d.c. to 0,8M baud (1x clock)
- Asynchronous operation
  5 to 8-bit characters
  1, 1½ or 2 stop bits
  odd, even, or no parity
  parity, overrun and framing error detection
  line break detection and generation
  false start bit detection
  automatic serial echo mode
  local or remote maintenance loop back mode
  baud rate: d.c. to 0,8M baud (1x clock)
  d.c. to 50k baud (16x clock)
  d.c. to 12,5k baud (64x clock)

Pin designation

pin no.	symbol	name and function	type
27, 28, 1, 2, 5-8	D_0-D_7	8-bit data bus	I/O
21	RESET	Reset	I
12, 10	A_0-A_1	Internal register select lines	I
13	$\overline{R}/W$	Read or write command	I
11	$\overline{CE}$	Chip enable input	I
22	$\overline{DSR}$	Data set ready	I
24	$\overline{DTR}$	Data terminal ready	O
23	$\overline{RTS}$	Request to send	O
17	$\overline{CTS}$	Clear to send	I
16	$\overline{DCD}$	Data carrier detected	I
18	$\overline{TxEMT}/\overline{DSCHG}$	Transmitter empty or data set change	O
9	$\overline{TxC}$	Transmitter clock	I/O
25	$\overline{RxC}$	Receiver clock	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	$\overline{TxRDY}$	Transmitter ready	O
14	$\overline{RxRDY}$	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5 V supply	I
4	GND	Ground	I

Pin configuration – I package

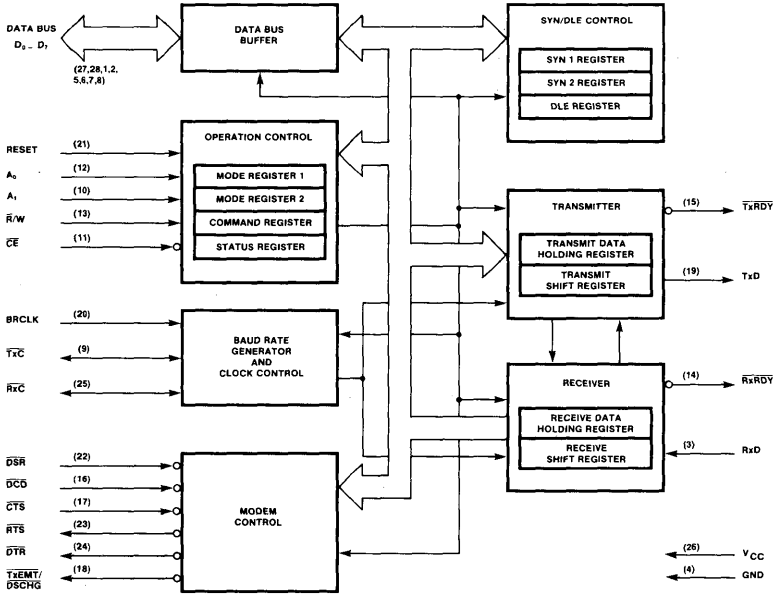


Block diagram

The PCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Other features

- internal or external baud rate clock
- 16 internal rates – 50 to 19 200 baud
- double buffered transmitter and receiver
- full or half-duplex operation
- fully compatible with 2650 CPU
- TTL compatible inputs and outputs
- single 5 V power supply
- no system clock required
- 28-pin dual in-line package



Programmable Communications Interface (continued)

Table 1 Baud rate generator characteristics – crystal frequency = 5,0688 MHz

baud rate	theoretical frequency 16x clock	actual frequency 16x clock	percentage error	duty cycle %	divisor
50	0,8 kHz	0,8 kHz	–	50/50	6336
75	1,2	1,2	–	50/50	4224
110	1,76	1,76	–	50/50	2880
134,5	2,152	2,1523	0,016	50/50	2355
150	2,4	2,4	–	50/50	2112
300	4,8	4,8	–	50/50	1056
600	9,6	9,6	–	50/50	528
1 200	19,2	19,2	–	50/50	264
1 800	28,8	28,8	–	50/50	176
2 000	32,0	32,081	0,253	50/50	158
2 400	38,4	38,4	–	50/50	132
3 600	57,6	57,6	–	50/50	88
4 800	76,8	76,8	–	50/50	66
7 200	115,2	115,2	–	50/50	44
9 600	153,6	153,6	–	48/52	33
19 200	307,2	316,8	3,125	50/50	16

Note
16x clock is used in asynchronous mode. In synchronous mode clock multiplier is 1x and duty cycle is 50% for any baud rate.

Table 2 CPU-related signals

pin name	pin no.	input/output	function
V_{CC}	26	I	+5 V supply input.
GND	4	I	Ground.
RESET	21	I	A high on this input performs a master reset on the 2651. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
A_1-A_0	10, 12	I	Address lines used to select internal PCI registers.
$\overline{R}/W$	13	I	Read command when low, write command when high.
$\overline{CE}$	11	I	Chip enable command. When low, indicates that control and data lines to the PCI are valid and that the operation specified by the $\overline{R}/W$, A_1 and A_0 inputs should be performed. When high, places the D_0-D_7 lines in the three-state condition.
D_7-D_0	8, 7, 6, 5 2, 1, 28, 27	I/O	8-bit, three-state data bus used to transfer commands, data and status between PCI and the CPU. D_0 is the least significant bit; D_7 the most significant bit.
$\overline{TxRDY}$	15	O	This output is the complement of Status Register bit SR0. When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$	14	O	This output is the complement of Status Register bit SR1. When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT}/\overline{DSCHG}$	18	O	This output is the complement of Status Register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the Status Register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU.

Multi-Protocol Communications Controller (MPCC) 2652

The 2652 Multi-Protocol Communications Controller (MPCC) is a monolithic n-channel MOS LSI circuit that formats, transmits and receives synchronous serial data while supporting bit-oriented or byte control protocols. The chip is TTL compatible, operates from a single +5 V supply, and can interface to a processor with an 8 or 16-bit bidirectional data bus.

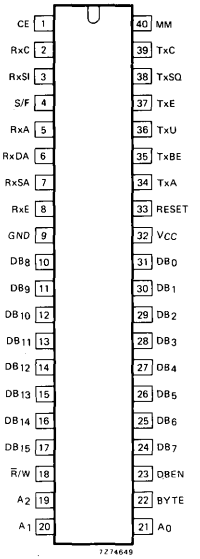
Features

- d.c. to 500k bps data rate
- protocol management
  bit-oriented protocols (BOP): SDLC, ADCCP, HDLC
  byte-control protocols (BCP): BI-SYNC, DDCMP
- programmable operation
  8 or 16-bit three-state data bus
  protocol selection – BOP or BCP
  error control –CRC or VRC or no error check
  character length – 1 to 8-bits for BOP or 5 to 8 bits for BCP
  SYNC or secondary station address comparison for BCP-BOP
  idle transmission of SYNC/FLAG or MARK for BCP-BOP
- automatic detection and generation of special BOP control sequences, i.e., FLAG, ABORT, GA
- zero insertion and deletion for BOP
- short character detection for last BOP data character
- SYNC generation, detection, and stripping for BCP
- maintenance mode for self-testing
- common parameter control registers
- independent status and data registers for receive and transmit
- status indicator signals can be used as CPU interrupts
- TTL compatible
- 40-pin package
- single +5 V supply

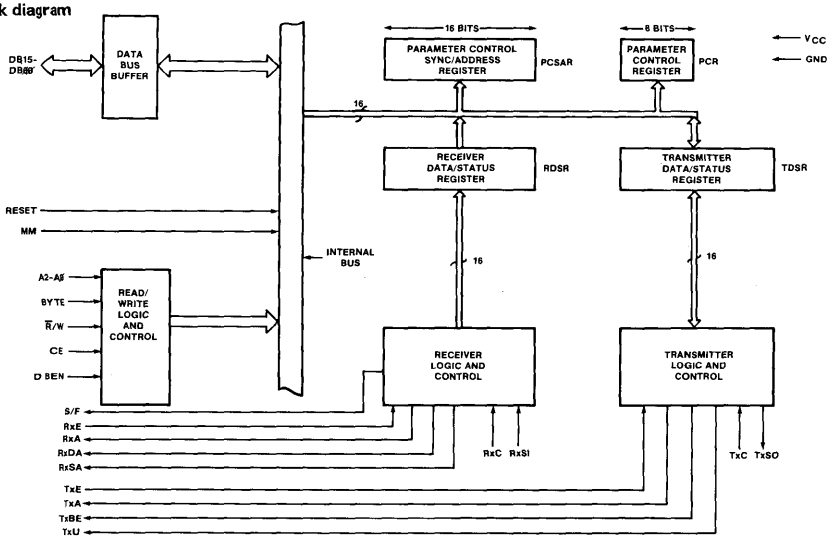
Applications

- intelligent terminals
- network processors
- front end communications
- remote data concentrators
- communication test equipment
- computer to computer links

Pin configuration — I package



MPCC block diagram



Pin designation

mnemonic	pin no.	type	name and function
DB15-DB00	17-10 24-31	I/O	**Data Bus.** DB07-DB00 contain bidirectional data while DB15-DB08 contain control and status information to or from the processor. Corresponding bits of the high and low order bytes can be WIRE OR'ed into an 8-bit data bus.
A2-A0	19-21	I	**Address Bus.** A2-A0 select internal registers. The four 16-bit registers can be addressed on a word or byte basis. See Register Address section.
BYTE	22	I	**Byte.** Single byte (8-bit) data bus transfers are specified when this input is high. A low level specifies 16-bit data bus transfers.
CE	1	I	**Chip Enable.** A high input permits a data bus operation when DBEN is activated.
R/W	18	I	**Read/Write.** $\bar{R}$/W controls the direction of data bus transfer. When high, the data is to be loaded into the addressed register. A low input causes the contents of the addressed register to be presented on the data bus.
DBEN	23	I	**Data Bus Enable.** After A2-A0, CE, BYTE and $\bar{R}$/W are set up, DBEN may be strobed. During a read, the three-state data bus (DB) is enabled with information for the processor. During a write, the stable data is loaded into the addressed register and TxBE will be reset if TDSR was addressed.
RESET	33	I	**Reset.** A high level initializes all internal registers and timing.
MM	40	I	**Maintenance Mode.** MM internally gates TxSO back to RxSI and TxC to RxC for off-line diagnostic purposes. The RxC input is disabled when MM is asserted.

Multi-Protocol Communications Controller (continued)

Pin designation

mnemonic	pin no.	type	name and function
RxE	8	I	**Receiver Enable.** A high level input permits the processing of RxSI data. A low level disables the receiver logic and initializes all receiver registers and timing.
RxA	5	O	**Receiver Active.** RxA is asserted when the first data character of a message is ready for the processor. In the BOP mode this character is the address. The received address must match the secondary station address if the MPCC is a secondary station. In BCP mode, if Strip-SYNC ($PCSAR_{13}$) is set, the first non-SYNC character is the first data character; if Strip-SYNC is zero, the character following the second SYNC is the first data character. In the BOP mode, the closing FLAG resets RxA. In the BCP mode, RxA is reset by a low level at RxE.
RxDA*	6	O	**Receiver Data Available.** RxDA is asserted when an assembled character is in $RDSR_L$ and is ready to be presented to the processor. This output is reset when $RDSR_L$ is read.
RxC	2	I	**Receiver Clock.** RxC (1x) provides timing for the receiver logic. The positive-going edge shifts serial data into the RxSR from RxSI.
S/F	4	O	**SYNC/FLAG.** S/F is asserted for one RxC clock time when a SYNC or FLAG character is detected.
RxSA*	7	O	**Receiver Status Available.** RxSA is asserted when there is a zero to one transition of any bit in $RDSR_H$ except for RSOM. It is cleared when $RDSR_H$ is read.
RxSI	3	I	**Receiver Serial Input.** RxSI is the received serial data. Mark = '1', space = '0'.
TxE	37	I	**Transmitter Enable.** A high level input enables the transmitter data path between $TDSR_L$ and TxSO. At the end of a message, a low level input causes TxSO = 1 (mark) and TxA = 0 after the closing FLAG (BOP) or last character (BCP) is output onTxSO.
TxA	34	O	**Transmitter Active.** TxA is asserted when TxE is high and TSOM ($TDSR_8$) is set. This output will reset when TxE is low and the closing FLAG (BOP) or last character (BCP) has been output on TxSO.
TxBE*	35	O	**Transmitter Buffer Empty.** TxBE is asserted when the TDSR is ready to be loaded with new control information or data. The processor should respond by loading the TDSR which resets TxBE.
TxU*	36	O	**Transmitter Underrun.** TxU is asserted during a transmit sequence when the service of TxBE has been delayed for more than one character time. This indicates the processor is not keeping up with the transmitter (TxSO depends on $PCSAR_{11}$). TxU is reset by RESET or setting of TSOM ($TDSR_8$).
TxC	39	I	**Transmitter Clock.** TxC (1x) provides timing for the transmitter logic. The positive-going edge shifts data out of the TxSR to TxSO.
TxSO	38	O	**Transmitter Serial Output.** TxSO is the transmitted serial data.
V_{CC}	32	PS	+5 V power supply.
GND	9	GND	0 V reference ground.

* Indicates possible interrupt signal.

Programmable Peripheral Interface (PPI)
2655

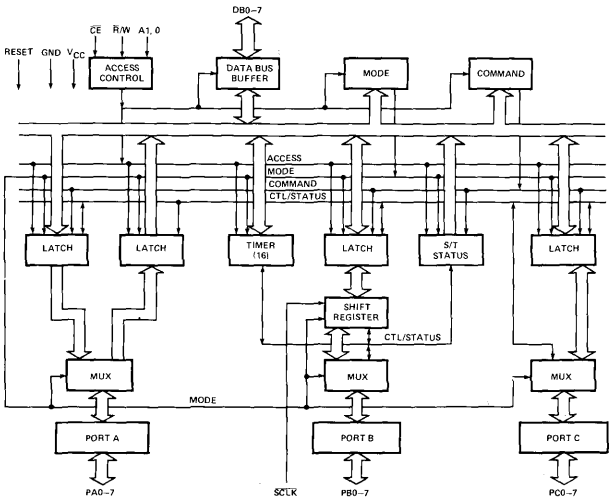
The 2655 PPI is designed for 2650 microcomputer systems. It consists of three ports (24 I/O pins), which can be individually programmed to function as input, output or bidirectional ports. Interface with the 2650 is via an eight-bit bidirectional data bus.

The PPI may be programmed for five major modes of operation: static I/O, strobed I/O, bidirectional I/O, serial I/O, or serial/timer I/O. In the serial/timer mode, parallel-to-serial or serial-to-parallel conversion of data operates simultaneously with the timer on one of the three ports.

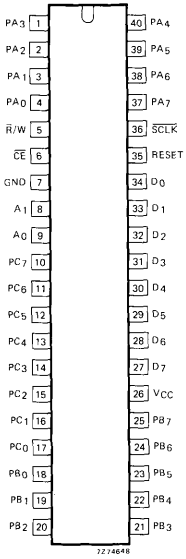
Features

- five selectable major operating modes:
  static I/O
  strobed I/O
  bidirectional I/O
  serial I/O
  serial/timer I/O
- three ports (A, B and C) with 24 programmable I/O pins
- completely TTL compatible
- 3 MHz programmable timer or event counter
- fully compatible with the 2650 microprocessor
- direct bit set/reset capability of each bit for all three ports
- ability to source 1 mA at 1,5 V
- 300 ns port read/write access time
- operates in a polled or interrupt driven system environment
- 40-pin dual in-line package
- single +5 V supply

Block diagram



Pin configuration — I package



Programmable Peripheral Interface (continued)

Operation

The following is a functional description of the five operating modes of the PPI. Each mode is selected via a mode control word. Interrupt generation and interrupt enable/disable functions are available with each mode except the static mode which operates entirely under program control.

Static mode

All three ports can operate in the static I/O mode. This mode allows each pin of each port to be either an input pin or an output pin. A logic '1' written to a pin of a selected port from the 2650 will condition that pin to be an input or output pin. Writing a logic '0' to the pin conditions that pin to be an output pin only. Outputs are latched while inputs are not. Each pin may be set or reset on an individual basis by a "set/reset" command.

Strobed I/O mode

In this mode, data may be transferred to or from a specified port in conjunction with strobe or "handshaking" signals. Ports A and B can operate in the strobed I/O mode and port C bits are used as control and status bits. In this mode both inputs and outputs are latched, and each port can be either an input or output.

Bidirectional I/O mode

This mode provides a means for communicating with a peripheral device over a single eight-bit bus with both transmitting and receiving capability. Port A operates in this mode with Port C pins providing "handshaking" signals for status and control. Both inputs and outputs are latched and port direction is determined by a control signal from the peripheral.

Serial I/O mode

This mode provides a means for communicating with a peripheral device on a bit serial basis through Port B. Parallel data from the CPU will be shifted out to the peripheral over the least significant bit of Port B (PB0). Eight clocks will be required for a complete character transfer. The eight-bit character will be repeatedly shifted out until the CPU presents another character to Port B.

For the serial in mode, data is input from the peripheral at the most significant bit of Port B (PB7). Eight clocks will be required to assemble the eight-bit character. An interrupt request will signal the CPU for character transfer.

Timer mode

This mode enables the PPI to perform time interval measurements, pulse width measurements, and event counting. This timing function is performed during the serial/timer mode, and is restricted to Port B only. The mode is initiated by selecting the desired operation and loading a 16-bit down counter with an initial value. The counter does not start counting until the upper eight bits have been loaded. An interrupt can be generated to signal the CPU when the timer reaches a zero count.

Pin definitions

pin no.	pin name	type	function
27-34	D7-D0	I/O	Eight-bit three-state bidirectional data bus. All data and command transfers are made using this bus. D0 is the least-significant bit; D7 is the most-significant bit.
35	Reset	I	Resets all internal storage elements, including the data latches and command registers. Resets ports A, B and C to accept input data, and operating mode to static mode. A functionally equivalent on-chip power-on reset is also provided.
8, 9	A1, A0	I	Address lines used to select internal PPI modes or registers. Indicates control or data words to be placed on the data bus. Used in conjunction with the $\overline{R}$/W line.
5	$\overline{R}$/W	I	When low, gates the selected register to the data bus. When high, gates the contents of the data bus into the selected register.
6	$\overline{CE}$	I	When low, identifies that control and data lines to the PPI are valid.
36	$\overline{SCLK}$	I	Provides a serial clock for the parallel-to-serial or serial-to-parallel conversion.
37-40 1-4	PA7-PA0	I/O	An eight-bit three-state quasi-bidirectional port.* PA0 is the least-significant bit; PA7 is the most-significant bit.
25-18	PB7-PB0	I/O	An eight-bit quasi-bidirectional port.* PB0 is the least-significant bit; PB7 is the most-significant bit. Port B also has parallel-to-serial or serial-to-parallel conversion capability with PB0, 7 being either the serial output or input respectively. Data is double buffered. Port B can also operate as a 16-bit binary timer, as an event counter, or as a pulse width indicator. An output is generated whenever the counter is decremented to the all-zero state.
10-17	PC7-PC0	I/O	A eight-bit quasi-bidirectional port.* PC0 is the least-significant bit; PC7 is the most-significant bit. Port C bits are also used as control and status signals in conjunction with ports A and B. When the pin bit is used as a strobe input, the line receives an external strobe input which clocks information from port A or port B into the port A or port B data latches. When the pin is used as a status line, the line indicates port A or port B status condition which may be used as an interrupt input to the 2650.
26	V_{CC}	I	+5 V supply.
7	GND	I	Ground.

* A quasi-bidirectional port allows each bit to be designated as input or output under program control. If any bit of the port is set to a '1', that bit becomes an input or output depending on the usage of the port pin. If the peripheral is driving the port bit (i.e. overriding the logic '1' condition produced by the internal port pull-up resistor), then the bit is an input. If the peripheral is receiving from the port bit, then a '0' or '1' written to the port will be transmitted to the peripheral.

System Memory Interface (SMI)
2656

The 2656 System Memory Interface (SMI) is a mask programmable circuit with on-chip memory, I/O, and timing (clock) functions. It is usable either in 2-chip or multi-chip microcomputer systems. Used with the 2650 microprocessor, it provides a 2-chip microcomputer. This 2-chip microcomputer offers the user 2kx8 bits of ROM, 128x8 bits of RAM, and an 8-bit multi-function I/O port.

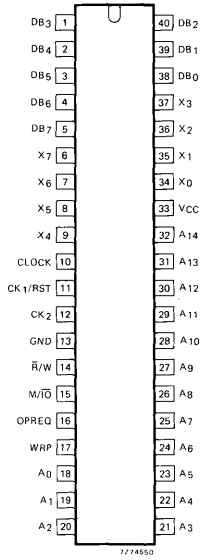
Used as a system interface in a multi-chip microcomputer, with large memory and/or additional peripheral requirements, the programmable versatility of the SMI provides decoded chip enable outputs. These outputs connect directly to other memory or I/O functional blocks with few, if any, requirements for additional interfacing chips. This reduces both chip count and cost in complex microcomputer systems.

The 2656 is processed using Signetics' n-channel silicon gate technology. Only a single power supply of +5 V is needed.

Features

- 2kx8 mask programmable ROM
- 128x8 static RAM
- 8 multi-purpose pins for either chip enables or I/O bits
- 8-bit latch for either I/O or MPU storage
- internal clock generator with crystal, RC, or external timing source
- system power-on reset
- 40-pin dual in-line package
- single +5 V supply
- 2-chip microcomputer
- system control for multi-chip microcomputers – eliminates or reduces TTL support circuitry for memory and I/O device selection
- from small (2k-2 chip) to 32k microprocessor-based systems.

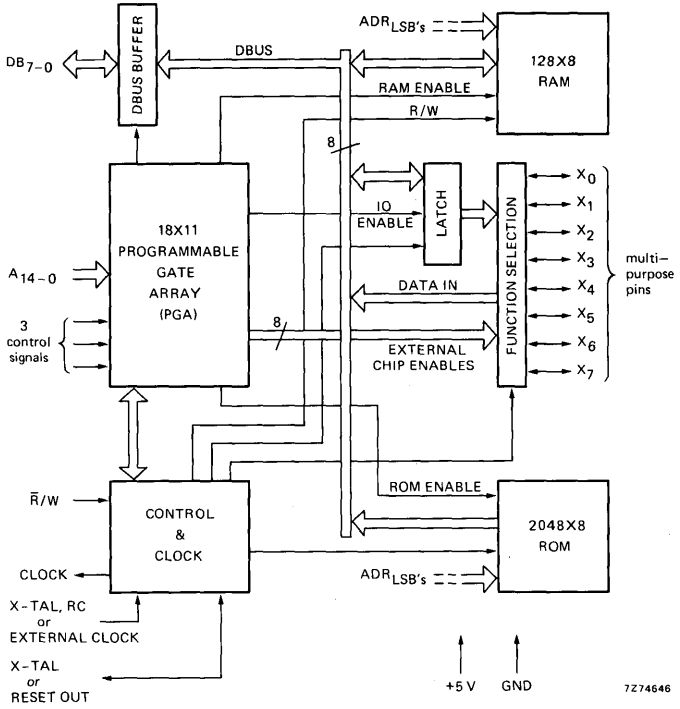
Pin configuration – I package



Pin definitions

pin no.	pin name	function
38-40, 1-5	DB_0-DB_7	8-bit bidirectional data bus. All data transfers between the MPU and ROM, RAM, Latch and X pins are made using this bus.
15-32	PGA inputs	18 PGA inputs that are used to determine SMI operation during the current MPU cycle. These inputs should include:
18-32	A_0-A_{14}	• MPU address bus. Address bus inputs occupy contiguous bit positions with A_0 as the least-significant address bit.
16	OPREQ	• A control signal that specifies the valid state of address and control bus.
15, 17	M/$\overline{IO}$, WRP	• Optional signals. Possibilities include Memory or I/O (M/$\overline{IO}$), Write Pulse (WRP), external control signals, or additional high order address bits.
14	$\overline{R}$/W	A control signal from the MPU that indicates whether the requested operation is to be a Read or Write (0 or 1 respectively). This signal must not change while OPREQ is true.
10	CLOCK	Output clock to the MPU. The frequency is determined by the timing element and the mask programmable divisor (divided by 1, 2, 3, 4).
11, 12	CK_1/RST, CK_2	Connections for the timing element. Only CK_2 is necessary for an RC or external timing source. The CK_1/RST pin then becomes a power-on RESET output. Two pins are necessary for direct connection of a crystal.
33, 13	V_{CC}, GND	Power supply connection and ground.
34-37, 9-6	X_0-X_7	Multi-purpose I/O pins. These pins can be mask programmed as external memory or I/O Chip Enables, or bidirectional I/O Port data bits, or any combination of the two.

System Memory Interface (continued)



Functional block descriptions

Data Bus Buffer
A three-state bidirectional 8-bit bus transceiver for data transfer between the SMI and MPU.

Programmable Gate Array (PGA)
Provides select signal outputs for the internal ROM, RAM, Latch, and up to 8 multi-purpose I/O pins that are mask-programmed as Chip Enables. A PGA output is active when the input variables match any one of 11 corresponding mask-programmed product terms. The 18 input variables are normally address and control bus signals from the MPU and may be programmed as '1', '0', and 'don't care'. Each product term is a specified combination of the input variables.

Control and Clock
Generates the CLOCK output signal to the MPU and control signals for the ROM, RAM, and LATCH. A mask programmable frequency divider provides input frequency division by 1, 2, 3 or 4. The timing source is mask programmable and may be a crystal, RC, or external oscillator. If either of the latter two are designated as a timing source, the second timing pin becomes a RESET output to the MPU.

ROM
2 048 bytes of mask-programmable Read Only Memory for storage of instructions and constants. The ROM base address is PGA mask programmable over the entire MPU address range. The ROM can be disabled by a mask option.

RAM
128 bytes of Read/Write Memory for MPU data storage and retrieval. The RAM base address is PGA mask programmable over the entire MPU address range. RAM dominates over ROM if address overlap is intentionally mask programmed. The RAM can be disabled by a mask option.

Function Select (FS)
A 1 x 8 Function Select array of mask-programmable contacts determine the function of each of the multi-purpose I/O pins (X_0-X_7). Two modes exist:

1. CE – The X pin is an active low Chip Enable ($\overline{CE}$) for either external memory or an I/O port. PGA inputs receive the external address and MPU control signals required to generate the $\overline{CE}$ output.
2. P – The X pin is a bidirectional I/O Port Data bit. A portion of the PGA provides the control signal to select the Port.

Latch
Holds output data for the multi-purpose I/O pins mask programmed as a mode P. The latch continues to function as a read/write element even if all multi-purpose I/O pins are programmed as chip enables. Thus, any X pin that is programmed as an external chip enable can have corresponding latch bits available for temporary data storage or software flags. To read an input pin, the corresponding latch bit must first be written to a '1' by the MPU program. This is done to disable all active outputs, changing them to passive pull-up outputs. This permits inputs to be sensed on the same pin. Subsequent reads of the same pin do not have to be preceded by a write if the state of the latch pin remains a '1'.

2650PC4000 Emulator board for 2656

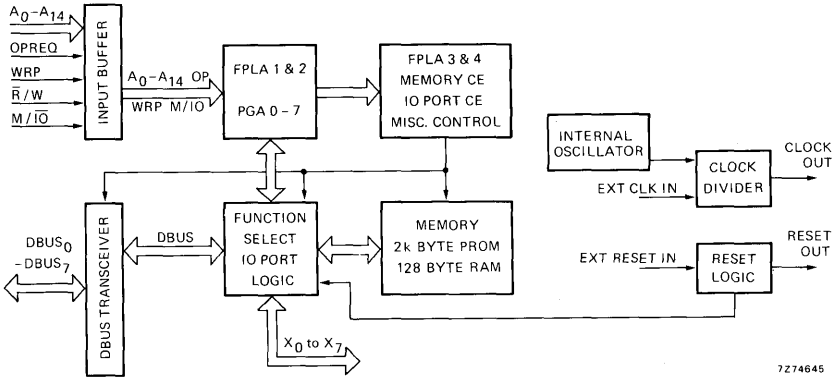
The PC4000 is a circuit emulation of the 2656, a 40-pin NMOS-LSI system memory interface chip. The PC4000, in circuit board form, offers the engineer a system design aid. By designing with the PC-board emulator, specific ROM and PGA (programmable gate array) patterns can be determined for the user's application.

In utilizing the PC4000, the engineer-designer is able to implement the same functions as the 2656. Through a cable and 40-pin plug with a pin configuration identical to the 2656, the user connects the PC4000 directly into his prototype system. He can access the 128x8 RAM, the preprogrammed ROM, and the gate array. The user can simulate the eight multi-function ports either as I/O ports or chip enables, the power-on reset, and the clock generator and divider.

The PC4000 emulator contains the same circuits that are available to the user on the 2656 Systems Memory Interface chip. Functionally the PC4000 replaces the 2656 in the user's prototyping system through a pin-for-pin compatible plug and its 40-wire ribbon cable attached to the PC4000. Identical circuit functionality of the 2656 chip is provided to the user by the functions of the PC Board.

In emulating the 2656, the speed of the board circuitry is equivalent to or faster than the on-chip circuitry. ROM is implemented with bipolar PROMs and on-chip RAM is implemented with the bipolar RAM packages. The programmable gate array (PGA) for the selection of the ROM and RAM enables and the I/O function selects are implemented with field programmable logic arrays (FPLAs).

The oscillator provided on the PC4000 has the same frequency dividers available as on the 2656. The oscillator divide ratio is implemented by the toggle switch settings.



Functional block descriptions

Input Buffer
This circuitry buffers the incoming signals from the MPU (specifically for the 2650 MPU, the addresses, A0-A14, and the 4 control signals, OPREQ, WRP, $\overline{R}$/W and M/$\overline{IO}$).

Data Bus Transceiver
This circuitry buffers the incoming 8-bit data bus from the MPU, and provides output drivers to the data bus.

FPLAs 1 and 2
FPLAs 1 and 2 represent a portion of the programmable gate array of the 2656 SMI chip. These 2 FPLAs decode the chip enable signals.

FPLAs 3 and 4
These FPLAs represent the remainder of the gate array. FPLA 3 and a portion of FPLA 4 generate the on-board ROM, RAM and port enable signals. The remainder of FPLA 4 is used to generate the data bus control signals.

Function Select and I/O Port Logic (via FPLAs 1-4)
The function select and I/O port logic allow the multi-purpose pins of the 2656 to be individually selected as either an I/O port or a chip enable via eight switches, FS0-FS7. When assigned as chip enables, they must be programmed in FPLAs 1 and 2. When a multi-purpose pin is assigned as I/O or as an input port, the port address is programmed in FPLAs 1 and 2. When the FS switch is ON, the corresponding pin of the 2656 is selected as an I/O port. When the FS switch is OFF, the corresponding pin is selected as a chip enable.

Memory
Both ROM and RAM memory functions are implemented in bipolar PROM and RAM respectively. The memory chip enables are programmed in FPLAs 3 and 4. (See the PROGRAMMING section.)

Clock Divider, Reset Logic, and Internal Oscillator
This circuitry provides an internal oscillator with switches for frequency divide by 1, 2, 3 or 4. Reset logic is provided on the PC4000 to allow the user to reset the system during debug via an external switch closure, without the need for powering down. The reset logic is used when the RC or external oscillator modes are selected.

If the RC or crystal internal oscillator mode is desired, the frequency determining components must be installed on the emulator PCB. The pins on the header that correspond to the RC and Crystal pins are not used in this mode, and only the external Reset function is provided.

Part list

part number	quantity	description
7403	2	Open Collector Quad Nand
7404	3	Hex Inverter
7405	2	Open Collector Hex Inverter
74LS14	1	Hex Schmitt Trigger Inverter
7432	1	Quad 2-Input OR gate
74LS86	1	Quad 2-Input XOR
74109	1	Dual JK Flip-Flop
74116	1	Dual Quad D Latch with Clear
74126	4	Quad Three-state Buffer
74163	1	4-bit Binary Counter
8T28B	2	Bidirectional Data Bus Driver Receiver
8T97B	5	Three-state Hex Buffer
8T98B	2	Three-state Hex Inverter Buffer
82S101	4	Open Collector FPLA
82S115	4	512x8 PROM
82S09	2	64x9 BIPOLAR RAM
NE555	1	Timer
761-1-51,0 kΩ	4	Resistor Dip Pak
	1	10 kΩ Resistor
	1	100 kΩ Resistor
	1	220 Ω Resistor
		Note: All Resistors ¼ watt
	1	150 pF Capacitor
	2	0,01 μF Capacitor
	5	4,7 μF Capacitor
	14	0,1 μF Capacitor
	1	Edge Connector AMP 225-21021-401-117
	2	8-Position Dip Switch
	1	PC Board 2650/PC4000
	4	24-pin Dip Socket
	4	28-pin Dip Socket
	1	40-pin Dip Socket
	1	Cable Assembly

Required but not supplied:
Timing element for oscillator.

Emulator board for 2656 (continued)

40-core cable pin configuration

The interface from the PC4000 to the user's system is a 40-core cable with 40-pin DIP plugs at both ends.

function	pin no.	pin no.	function
DBUS3	1	40	DBUS2
DBUS4	2	39	DBUS1
DBUS5	3	38	DBUS0
DBUS6	4	37	X3
DBUS7	5	36	X2
X7	6	35	X1
X6	7	34	X0
X5	8	33	NC*
X4	9	32	ADDR14
CLK OUT	10	31	ADDR13
CLK 1	11	30	ADDR12
CLK2	12	29	ADDR11
VSS GND	13	28	ADDR10
R/W	14	27	ADDR9
M/I/O	15	26	ADDR8
OPREQ	16	25	ADDR7
WRP	17	24	ADDR6
ADDR0	18	23	ADDR5
ADDR1	19	22	ADDR4
ADDR2	20	21	ADDR3

* VDD for chip, no connection for board.

Note: Timing Element pins have alternative functions determined by connections W on the printed circuit board.
CLK 1 is external reset out. To use, connect W (4) to W (5).
CLK 2 is external clock in. To use, connect W (2) to W (3).
CLK 2 not used: To use internal RC oscillator connect W (1) to W (2).
To use internal XTAL oscillator connect W (2) to W (8).

Edge connector

The edge connector for the 2650PC4000 is an AMP 225-21021-4-01-117 edge connector. This edge connector has 20 pins on 0,156 inch centres with the following pin configuration:

GND	1	A	GND
GND	2	B	GND
	3	C	C2X
	4	D	
	5	E	RESET OUT**
	6	F	CLK OUT**
	7	H	RESET IN**
CK	8	J	OSC**
VCC	9	K	VCC
VCC	10	L	VCC

** Factory test only – do not use.

Microprocessor prototyping card 2650PC1001

The 2650PC1001 is a complete microcomputer on a single printed circuit board. The heart of this computer is Signetics' 2650 Microprocessor; a single chip, n-channel MOS Integrated Circuit which contains the CPU and control sections of the classical general purpose computer architecture.

In addition to the Microprocessor, the 2650PC1001 contains both control and read/write memory, I/O ports, clock, and all the necessary buffering and interface circuits to permit data transfer both on and off the p.c.b.

Features

- 2650 Microprocessor
- 1k bytes of ROM with PIPBUG*
- 1k bytes of RAM (off-board expandable)
- 1 MHz crystal oscillator
- serial I/O (either TTY 20 mA current loop or RS232 – selectable by jumper wire)
- 2 eight-bit output ports
- 2 eight-bit input ports
- DMA capability
- LED display indicators
- data bus and address bus test points
- buffered data and address outputs
- single power supply (+5 V)**

* Signetics' Loader and Debugging Program. (See appl. note SS50)

** Assumes RS232 I/O port is not used.

Memory

The memory of the 2650PC1001 is divided into two segments:

a. ROM with PIPBUG

b. RAM (Read/Write Memory)

The Read-Only Memory supplied with the card is the 82S129 Field Programmable type (PROM). Eight of these 256x4 devices are arranged to provide a 1kx8 memory array. The 2650PC1001 is supplied with the PIPBUG loader and debugger already programmed into the ROM. Since the devices are loaded into sockets, however, they can be easily replaced with other ROMs or PROMs programmed by the user.

The 1kx8 array is constructed with 2606 NMOS RAM devices. Since the 2606 is a 256x4 device, again 8 devices are used in the array.

Serial I/O

The serial I/O capability of the 2650PC1001 utilizes a unique serial I/O feature of the basic 2650 microprocessor. This feature allows serial data to be transferred directly into the 2650 under program control by using the sense and flag pins on the microprocessor.

Two types of serial I/O ports are available. The first is a teletype interface which can be directly connected to a teletype 20 mA current loop. The second is an RS232 interface which provides a connection for voltage-driven peripheral equipment. The selection of the particular interface to be used is made by connecting a jumper wire directly from the microprocessor flag and sense lines to the appropriate output port. If the RS232 interface is used, +12 and −12 V supplies are required in addition to the +5 V supply which operates the rest of the board.

Parallel I/O

Parallel I/O channels using the 2650's unique Non-Extended I/O mode are also provided. This mode allows a single byte instruction to select one of two distinct I/O devices. On the 2650PC1001, these two devices are represented by four separate data channels; two for reading and two for writing. The output (or write) channels are fully latched and buffered. The input (or read) channels are fully buffered. One read and one write channel represent a single I/O device. In addition to the Non-Extended I/O ports, the data and address buses, plus the appropriate control signals, are also available to provide the full extended I/O capability.

Microprocessor prototyping card (continued)

Other I/O

A complete listing of the I/O pins, plus a brief description of any I/O signal not detailed above, is as follows:

1,2	Ground
4-11	Processor Data Bus*
12	Strobe to Enable Input Data Port
13	D/C Output*
14	DMA Control Input
15	Extended/Non-Extended Output*
16	Interrupt Acknowledge Output*
17	R/W Output*
18	Write Pulse Output*
19	Run/Wait Output*
20	Operation Request Output*
21	Memory/IO Output*
22	Operation Acknowledge Input*
23	Clock Output (or Input if on-board clock not used)
24	Operation Request Input for DMA
25	Reset Input*
26	Interrupt Request Input*
27	Pause Input*
28-32	Unused
33-47	Address Bus*
48	+12 V for RS232
49	−12 V for RS232
50	+5 V
A, B	Ground
C	Not used
D-M	Non Extended Output Port "D"
N	Clock to load data into Output Port "D"
P	TTY serial data input (+)
R	TTY serial data input (−)
S	TTY serial data Output pull-up resistor (current loop +)
T	TTY serial data Output; TTL Level, open collector (current loop return)
U	RS232 ground
V	RS232 Output
W	TTY tape reader Output; TTL Level, open collector (+)
X	TTY tape reader Output pull-up resistor (−)
Y	RS232 Input
Z	Clock to load data into Output Port "C"
a-h	Non-Extended Output Port "C"
j	Strobe to enable Input Port Control
k-u	Non-Extended Input Port "D"
v-c	Non-Extended Input Port "C"
d	+12 V for RS232
e	−12 V for RS232
f	+5 V

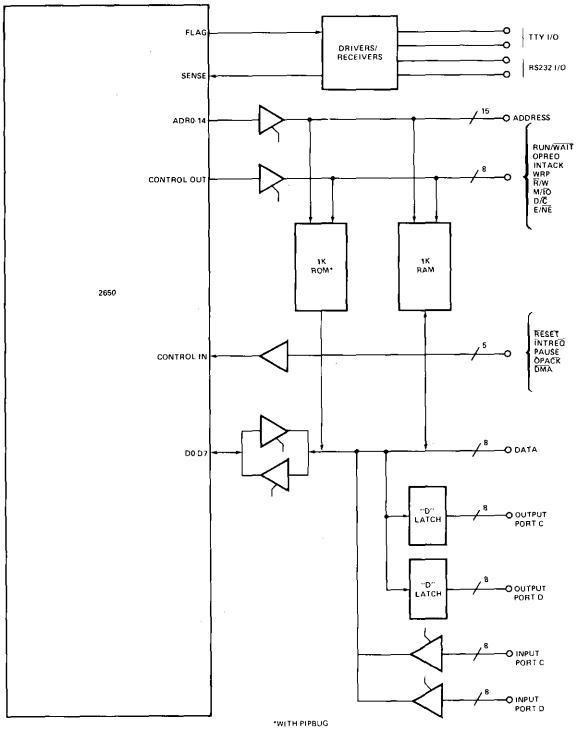
Summary

The above is intended to provide a brief description of Signetics' 2650PC1001 Prototyping Board. More detailed information can be obtained from the following:

SS50	PIPBUG Application Note
SP50	2650PC1001 Manual (Detailed Description)
AS50	Serial I/O using Sense and Flag Application Note
2650BM 1000	Basic 2650 Microprocessor Manual

* Buffered 2650 microprocessor outputs.

PC1001 Block diagram



Adaptable Board Computer (ABC) prototyping system
2650PC1500
2650KT9500

The Adaptable Board Computer, ABC 1500, is a modular microcomputer containing a CPU, memory, I/O ports and support circuitry. It is designed to cover a broad range of applications from software development to system hardware prototyping. Cost performance trade-offs have been carefully considered to achieve maximum flexibility and allow the card to be tailored to a variety of individual requirements.

The basic configuration consists of the 2650 8-bit microprocessor, 512 bytes of read/write memory (four 2112 static RAMs), 1k bytes of 2608 ROM with PIPBUG*, two 8T31 I/O ports and buffering on data, address and control lines. A single +5 V supply will be required to power the card and communicate with a serial 20 mA current loop terminal.

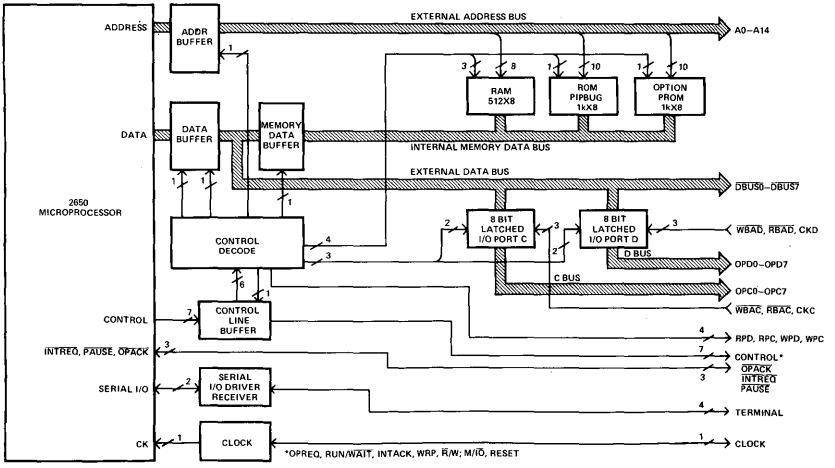
Modifications to the basic system can be easily made to allow for various memory configurations and operating modes. Unused plated-through holes are provided for the PROM memory chips (82S115s). Other options are jumper selectable. The area on the card associated with each jumper is identified with a "Wx" mnemonic.

The ABC 1500 is sold either as a completely assembled and tested card (2650PC1500) or in kit form (2650KT9500).

Features

- expandable printed circuit card:
  unused area on card filled with plated-through holes on 7,5 mm centres for wire-wrap sockets
- 1k bytes of PIPBUG* ROM (in socket)
- 512 bytes of RAM
- two latched I/O ports
  – four non-extended I/O read/write user strobes
- three-state buffers on data, address and control lines
- serial input/output port
- single +5 V supply requirement (1,7 A max) for card and 20 mA current loop interface (±12 V supply for RS232 interface)
- simple memory and I/O port decoding with two 16-pin DIPs
- interrupt and single step capability
- simple clock configured from dual monostable multivibrator
- 24k memory expansion capability
- directly compatible with 4k RAM card (2650PC2000) and power supply demonstration base (2650DS2000)
- card dimensions: 20 cm by 17,5 cm with a 100-pin connector along the 20 cm dimension

* PIPBUG is a loader, editor, and debug program. See Table 1.



Options

- 1k bytes of PROM in place of ROM
- 512 bytes of PROM or ROM in place of RAM
- asynchronous operation capability
- external clock input
- interrupt vector from port C

Interface

- terminal interface jumper selectable
  a. W4 to W5 and W6 to W7 jumpers select the 20 mA current loop mode
  b. W3 to W4 and W7 to W8 jumpers select the RS232 mode
- normally high input lines (10 kΩ pull-up resistor on each): $\overline{\text{INTREQ}}$, $\overline{\text{PAUSE}}$, $\overline{\text{RESET}}$, $\overline{\text{WBAC}}$, $\overline{\text{WBAD}}$, CKC, CKD
- plated-through holes are available at each connector pin to allow for insertion of wire-wrap pins
- edge connector supplied with card
- to allow for external clock input, remove jumper W9-W10
- asynchronous operation by removing jumper W1 to W2 and driving $\overline{\text{OPACK}}$
- during vectored interrupts, it is possible to allow port C to place the interrupt address on the data bus by removing jumper W21-W22 and jumpering W22-W23

Table 1 PIPBUG commands

alpha character input	command
A	alter memory
B	set breakpoint
C	clear breakpoint
D	dump memory to papertape
G	go to address
L	load memory from papertape
S	see and alter registers

Note: The program is entered by resetting the card. The terminal will then respond with an asterisk (*).

Memory configuration

All of page 0 is reserved for on-card memory (0 to 8191_{10}). Address lines A9, A11 and A12 are not decoded (Don't care signals) allowing two ICs to perform not only memory decoding but also I/O port decoding. As an added benefit, usable memory space exists at the top of page 0 (see memory map) due to the interleaving effect between the ROM and RAM memories. This memory space can be used as interrupt vector address locations in a negative direction from address location "0" (a negative relative instruction from address location "0" wraps around the first 8k page).

There is a total of two blocks in the RAM structure, each of which contains 256 bytes of RAM. Since PIPBUG uses the first 63 RAM locations for temporary storage, the first actual user location is 1087_{10} ($43F_{16}$) (there are seven other address locations corresponding to the first user location – see memory map). Starting at $43F_{16}$, the range for on card RAM extends to address 1535_{10} ($5FF_{16}$), giving a total usable on-card space of 449 bytes.

The first external memory location for add-on memory is 8192_{10} (2000_{16}). All of page 1, 2, and 3 are available, giving a total memory expansion capability of 24k.

Memory options

Modifications to the basic configuration can be made to provide a mix of RAM/PROM/ROM memories. PROM memories can be used in place of the PIPBUG ROM by removing the ROM from its socket and adding one or two 82S115 PROMs (512x8). Area and plated-through holes are provided on the card for insertion of sockets for the PROMs or the PROMs themselves. Decoding for the PROMs has been provided by ABC 1500 logic.

Data and address lines for 2112 RAMs and 82S129 PROMs or 82S229 ROMs are identical. It is, therefore, possible to use PROMs and/or ROMs in place of RAM. This option will require removal of the RAMs (two per block), and changing the jumper for each 256 byte block of PROM or ROM added. The jumper needed for each block of memory is as follows:

memory section	RAM jumper	PROM/ROM jumper
first block	W12-W13	W11-W13
second block	W15-W16	W14-W16

Adaptable Board Computer (ABC) prototyping system (continued)

I/O Port configuration

Two ports (C and D) are implemented with 8T31 bidirectional ports and can be used for general purpose I/O. Each consists of 8 clocked latches with two sets of bidirectional inputs/outputs. Data written into one side of the port will appear inverted at the other side.

One side of each port (Bus B of the 8T31) is tied to the external data bus ($\overline{DBUSX}$). The 2650 communicates with each port over this bus with one byte, non-extended I/O instructions. During 2650 activity with the ports, the ABC 1500 will provide four output strobes indicating the nature of the operation.

Table 2 Page 0 memory map

ADDRESS LINES						DECIMAL ADDRESS	ORGANIZATION	HEX ADDRESS
A14	A13	* A12	* A11	A10	** A9			
						8k	SECOND BLOCK RAM	1FFF
0	0	X	X	1	X		FIRST BLOCK RAM	
							SECOND BLOCK RAM	
						7k	FIRST BLOCK RAM	1BFF
0	0	X	X	0	X		PIPBUG ROM	
						6k		17FF
							SECOND BLOCK RAM	
0	0	X	X	1	X		FIRST BLOCK RAM	
							SECOND BLOCK RAM	
						5k	FIRST BLOCK RAM	13FF
0	0	X	X	0	X		PIPBUG ROM	
						4k		0FFF
							SECOND BLOCK RAM	
0	0	X	X	1	X		FIRST BLOCK RAM	
							SECOND BLOCK RAM	
						3k	FIRST BLOCK RAM	0BFF
0	0	X	X	0	X		PIPBUG ROM	
						2k		07FF
							SECOND BLOCK RAM	06FF
0	0	X	X	1	X		FIRST BLOCK RAM	05FF
							SECOND BLOCK RAM	04FF
						1k	FIRST BLOCK RAM	03FF
0	0	X	X	0	X		PIPBUG ROM	
						0		0000

Notes

1. * = Don't care for ROM and RAM; ** = Don't care for RAM.
2. Each block of RAM = 256 bytes.

strobe	function	strobe pulse width
WPC	write to Port C	duration of WRP
WPD	write to Port D	duration of WRP
RPC	read Port C	duration of OPREQ
RPD	read Port D	duration of OPREQ

The other side of each port (Bus A of the 8T31) is controlled by the user. Four control lines are used to read, write or three-state the buses.

control line				function
$\overline{WBAD}$	(1)	$\overline{RBAD}$	(0)	Read Port D
$\overline{WBAD}$	(0)	$\overline{RBAD}$	(0)	Write to Port D
$\overline{WBAD}$	(1)	$\overline{RBAD}$	(1)	Three-state D Bus
$\overline{WBAC}$	(1)	$\overline{RBAC}$	(0)	Read Port C
$\overline{WBAC}$	(0)	$\overline{RBAC}$	(0)	Write to Port C
$\overline{WBAC}$	(1)	$\overline{RBAC}$	(1)	Three-state C Bus

If no external logic is connected each port will be in the "read" mode ($\overline{WBAX}$ lines pulled high). The $\overline{RBAX}$ lines are tied to ground to allow read/write control of the buses with just the $\overline{WBAX}$ lines. To allow control for three-stating the buses, the following jumpers must be removed:

Line	Jumper
$\overline{RBAC}$	W19-W20
$\overline{RBAD}$	W17-W18

The clock for each port (CKC-Port C clock, CKD-Port D clock) is available at a connector pin for external control. These normally "high" lines can be pulled low to disable writing to the ports from either the 2650 or the external device.

ABC 1500 edge connector signal list

pin no.	function	pin no.	function	pin no.	function	pin no.	function
1	GND	26	$\overline{INTREQ}$	A	GND	d	OPC 3
2	GND	27	$\overline{PAUSE}$	B	GND	e	OPC 4
3	NC*	28	NC*	C	NC*	f	OPC 5
4	$\overline{DBUS0}$	29	$\overline{RBAD}$	D	OPD 0	g	OPC 6
5	$\overline{DBUS1}$	30	NC*	E	OPD 1	h	OPC 7
6	$\overline{DBUS2}$	31	$\overline{RBAC}$	F	OPD 2	j	NC*
7	$\overline{DBUS3}$	32	NC*	H	OPD 3	k	RPD
8	$\overline{DBUS4}$	33	A11	J	OPD 4	m	$\overline{WBAD}$
9	$\overline{DBUS5}$	34	A13-E/$\overline{NE}$	K	OPD 5	n	WPD
10	$\overline{DBUS6}$	35	A12	L	OPD 6	p	CKD
11	$\overline{DBUS7}$	36	A14-D/$\overline{C}$	M	OPD 7	r	NC*
12	NC*	37	A9	N	NC*	s	NC*
13	A14-D/$\overline{C}$	38	A10	P	TTY serial in +	t	NC*
14	NC*	39	A8	R	TTY serial in −	u	NC*
15	A13-E/$\overline{NE}$	40	A7	S	TTY serial out +	v	RPC
16	INTACK	41	A6	T	TTY serial out −	w	$\overline{WBAC}$
17	$\overline{R}$/W	42	A5	U	RS232 ground	x	WPC
18	WRP	43	A3	V	RS232 output	y	CKC
19	RUN/$\overline{WAIT}$	44	A0	W	NC*	z	NC*
20	OPREQ	45	A1	X	NC*	$\overline{a}$	NC*
21	M/$\overline{IO}$	46	A4	Y	RS232 input	$\overline{b}$	NC*
22	$\overline{OPACK}$	47	A2	Z	NC*	$\overline{c}$	NC*
23	CLOCK	48	+12 V	a	OPC 0	$\overline{d}$	+12 V
24	$\overline{TS}$	49	−12 V	b	OPC 1	$\overline{e}$	−12 V
25	$\overline{RESET}$	50	+5 V	c	OPC 2	$\overline{f}$	+5 V

Adaptable Board Computer (ABC) prototyping system (continued)

ABC 1500 parts list

quantity	description
1	PC1500 printed circuit board
1	edge connector – AMP 225-804-50
1	2650 8-bit static microprocessor
1	N7402 quad 2-input NOR gate – I/O strobe logic
1	N7416 hex inverter buffer – current loop interface
1	N74123 monostable multivibrator – clock for 2650
1	N74S138 3 line to 8 line decoder – control decode
1	8T15 – EIA line driver – R232 driver
4	8T26 quad three-state driver/receiver – data and memory data buffer
2	8T31 – bit latched bidirectional I/O port
4	8T97 hex three-state driver – address and control line buffer
1	2608 static ROM (1024x8) – PIPBUG ROM – CN0035
4	2112 static RAM (256x4) – organized as 512 byte RAM
1	82S123 PROM (32x8) coded PROM CD 1500 – control decode
4	1N914 diode
1	2N2222 transistor
1	50 pF capacitor
1	300 pF capacitor
13	0,1 μF capacitor
3	4,7 μF capacitor
2	220 Ω resistor
6	1 kΩ resistor
2	2 kΩ resistor
1	3,3 kΩ resistor
8	10 kΩ resistor
1	20 kΩ resistor
1	24-pin 2608 ROM socket – Robinson-Nugent ICN 246-54

Resident Assembler Board 2650PC1600

Features

- 3-pass Resident Assembler
- 5,5k bytes assembler program
- socket for 512 bytes user defined PROM
- 2k bytes RAM
- 365 user-definable symbols
- 20 pre-defined symbols
- generation of error messages
- LIBR directive to create subroutine libraries
- compatible with PC1001, ABC1500 and DS2000
- paper tape editor facility
- single +5 V supply requirement (4 A max)
- card dimensions 20 cm by 17,5 cm with a 100-pin connector along the 20 cm dimension

The 2650PC1600 is a resident assembler to be used with the PC1001 or ABC1500 prototyping boards. It also fits into the DS2000 power supply base.

The system consists of a printed-wiring board on which 11 PROMs containing the assembler program are mounted, together with 16 RAM ICs for use as storage during program assembly. The assembler has been designed for use with paper tape and so input and output are transmitted via a teletype. Alternatively, a fast paper tape reader may be used to advantage. An extra socket has been included on the PC1600 board for PROM containing a tape-reader control program.

The PC1600 resident assembler accepts a program written in 2650 Assembly Language as input and produces a tape containing a hexadecimal translation of the program. This hexadecimal tape has a format suitable for input to the PC1001 or ABC1500 prototyping boards via the PIPBUG control program which is included on both these boards. The assembler is a three-pass type, that is the entire assembly language program is scanned three times by the assembler. On the first pass all the symbols defined by the user (up to a maximum of 365) are assigned values and stored in the RAMs on the PC1600 board and simple errors such as invalid symbols detected. During the second pass the internal logic of the program is checked and any further errors detected, the line-by-line assembly is performed and a full listing of the program, including any error messages, is printed out. On the third pass the hexadecimal tape is punched and a corresponding hexadecimal listing produced for reference.

The assembler program introduces several additional features over the cross assembler, the most important being four new error messages, 20 pre-defined symbols and a new assembler directive LIBR. This directive enables the user to assemble several tapes into one hexadecimal tape as part of the same program, this facilitates the creation of subroutine "libraries". The assembler also makes patching of a program in RAM easier by assembling the correct number of bytes for a line containing an error, so that these bytes may be altered without changing the memory locations of the rest of the bytes of the program.

PC1600 edge connector signal list

pin no.	function
1	GND
2	GND
4	DBUS0
5	DBUS1
6	DBUS2
7	DBUS3
8	DBUS4
9	DBUS5
10	DBUS6
11	DBUS7
17	R/W
18	WRP
20	OPREQ
21	M/IO
33	ABUS11
34	ABUS13
35	ABUS12
36	ABUS14
37	ABUS9
38	ABUS10
39	ABUS8
40	ABUS1
41	ABUS6
42	ABUS5
43	ABUS3
44	ABUS0
45	ABUS1
46	ABUS4
47	ABUS2
50	+5 V
A	GND
B	GND

4k Memory Card
2650PC2000

The 2650PC2000 is a 4k Memory Card designed to be compatible with the 2650 microprocessor. It is composed of 32 NMOS, 1k by 1 bit static RAMs, 21L02, and organized in four groups of one kilobyte each. Decoding is provided to select one of the four groups and also distinguish the card in multi-card configurations. In a system application utilizing up to 8 cards (32k), each card is uniquely identified by hardwired jumpers. No external decoding is required.

The decoding logic is sectioned into two blocks. The first block determines if the address identifies that card as being part of the 8k page address. (The 2650 memory scheme is organized into 4 pages of 8k each.) The second block uniquely locates 1k bytes of memory on the board in the 8k bytes of memory of the selected page. Each 1k bank is individually selected by hardwired jumpers to the decoder.

Features

- requires only single +5 V supply
- industry standard 21L02 memories
- fully decoded for 32k memory organization
- data bus buffered with three-state drivers/receivers
- accessable from microprocessor or DMA controller
- TTL compatible
- dimensions are 20 x 17,5 cm with a 50-pin edge connector along 20 cm dimension
- typical power consumption of 4,5 W

Signal definition

Memory control signals and address lines between the 2650 microprocessor and the 2650PC2000 are indicated in the block diagram. The $\overline{\text{OPEX}}$ control line is reserved for use with DMA controllers. Its function is similar to that of the OPREQ line from the 2650. When either of these lines are true and a memory operation is specified (M/$\overline{\text{IO}}$ = High) the memory card is enabled to decode address lines A0-A14. When a bank is selected, the selected card control logic block allows the read-write line ($\overline{\text{R}}$/W) and write pulse (WRP) to pass to the memory array and also enable the external data bus drivers. When the operation is complete the memory card responds with a true condition on $\overline{\text{OPACK}}$.

Jumper address decoding

Jumpers are applied to designated plated-through holes identified by a "Wn" mnemonic. To identify the card to be part of a particular page, jumper point W5 to one of the following:

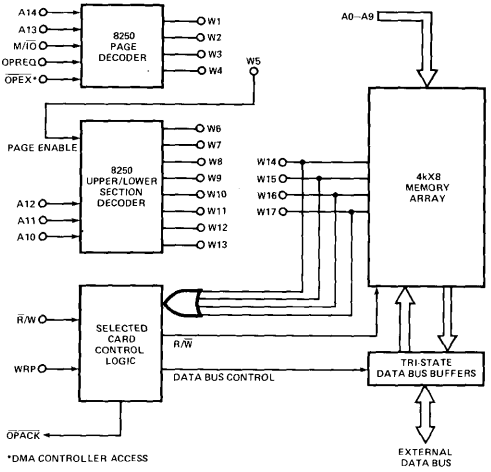
W1 for page 0
W2 for page 1
W3 for page 2
W4 for page 3

To locate each of the 1k bytes of the memory card in the selected memory page, four bank jumpers are required. The outputs of the decoder used to select one of eight 1k byte memory segments (W6-W13) must be connected to the selected 1k bytes of memory on the 2650PC2000 (W14-W17).

Factory installed jumpers allow for immediate connection to a Demo System (DS1000/2000) which has 2k of memory. These jumpers have been connected as follows:

W1 to W5 (page 0)
W8 to W14
W9 to W15
W10 to W16
W11 to W17

2650PC2000 block diagram



2650PC2000 edge connector

pin no.	function	pin no.	function
1,2, A, B	GROUND	34	ABUS13
4	$\overline{DBUS0}$	35	ABUS12
5	$\overline{DBUS1}$	36	ABUS14
6	$\overline{DBUS2}$	37	ABUS9
7	$\overline{DBUS3}$	38	ABUS10
8	$\overline{DBUS4}$	39	ABUS8
9	$\overline{DBUS5}$	40	ABUS7
10	$\overline{DBUS6}$	41	ABUS6
11	$\overline{DBUS7}$	42	ABUS5
17	$\overline{R}/W$	43	ABUS3
18	WRP	44	ABUS0
20	OPREQ	45	ABUS1
21	$M/\overline{IO}$	46	ABUS4
22	$\overline{OPACK}$	47	ABUS2
24	$\overline{OPEX}$	50, f	VCC +5 V
33	ABUS11		

Microprocessor Demonstration System 2650DS2000

The Demo System 2000 (2650DS2000) is a hardware base for use with the 2650 CPU printed circuit board (PC1001) and allows the exercising of this card with user defined options. When the DS2000 is combined with a CPU board (PC1001) and a teletype (TTY), the user is equipped with everything he needs to exercise any of the software or hardware features of the 2650. The DS2000 has a built-in power supply.

Features

- user-defined expansion capability from connector supplying address, data and control lines
- RS232 and TTY interface
- two extended and two non-extended I/O ports
- single step capability for program debugging
- display of address bus, data bus and the two non-extended I/O ports

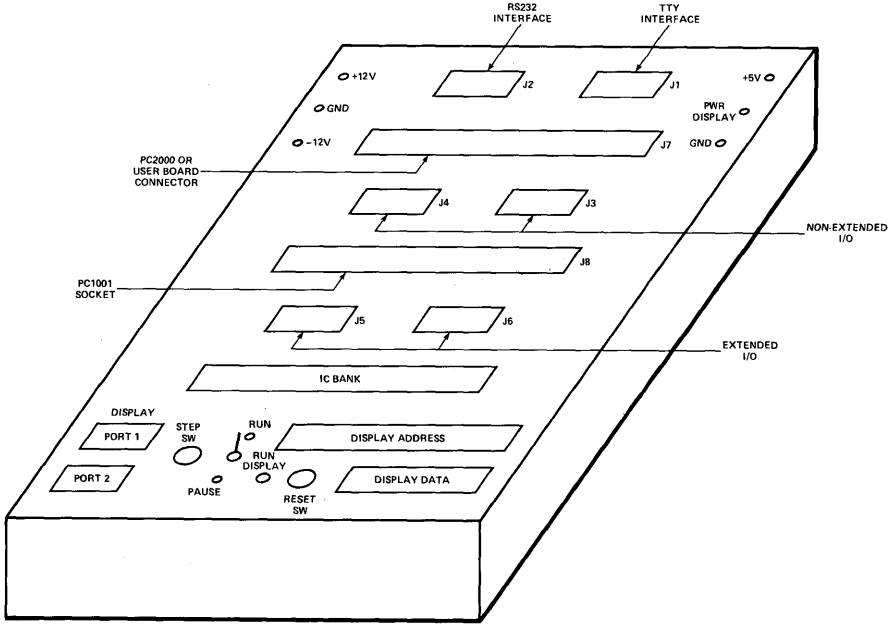
Connectors

The 2650 CPU Board (PC1001) is inserted into the J8 connector to complete the demo system. The user printed circuit board is inserted into the J7 connector. Both connectors are the same type (100 Pin Amphenol, series 225) and the numbered pins J7 and J8 have the same signals (except pin 12). The lettered pins of J7 (pins A to g) are not used.

Displays

The address and data bus led displays reflect the information on these buses during each OPREQ (beginning of an external operation). Latches store the information until another OPREQ is received. The two non-extended port displays represent data on channel C (port 2) and channel D (port 1) during the OPREQ for each I/O operation. A logic one on these displays will turn "on" the leds and a logic zero will turn them "off".

DS2000 hardware base



Controls

The pause and step logic allows one instruction to be executed at a time by pushing the 'step' button when the Run/Pause switch is in the pause position. In this mode the Run/$\overline{\text{Wait}}$ display led will go off. The reset switch will reset the display latches and place all zeros in the 2650 instruction address register.

Connections to sockets J7 and J8

pin no.	function (J7 and J8)	pin no.	function (J7 and J8)	pin no.	function (J8 only)*	pin no.	function (J8 only)*
1	GND	26	$\overline{\text{INTREQ}}$	A	GND	d	OPC 3
2	GND	27	$\overline{\text{PAUSE}}$	B	GND	e	OPC 4
3	NC**	28	NC	C	NC	f	OPC 5
4	$\overline{\text{DBUS0}}$	29	NC	D	OPD 0	g	OPC 6
5	$\overline{\text{DBUS1}}$	30	NC	E	OPD 1	h	OPC 7
6	$\overline{\text{DBUS2}}$	31	NC	F	OPD 2	j	EIPC
7	$\overline{\text{DBUS3}}$	32	NC	H	OPD 3	k	IPD 0
8	$\overline{\text{DBUS4}}$	33	ABUS 11	J	OPD 4	m	IPD 1
9	$\overline{\text{DBUS5}}$	34	ABUS 13	K	OPD 5	n	IPD 2
10	$\overline{\text{DBUS6}}$	35	ABUS 12	L	OPD 6	p	IPD 3
11	$\overline{\text{DBUS7}}$	36	ABUS 14	M	OPD 7	r	IPD 4
12*	EIPD	37	ABUS 9	N	COPD	s	IPD 5
13	D/$\overline{\text{C}}$	38	ABUS 10	P	TTY serial in +	t	IPD 6
14	$\overline{\text{DMA}}$	39	ABUS 8	R	TTY serial in −	u	IPD 7
15	E/$\overline{\text{NE}}$	40	ABUS 7	S	TTY serial out +	v	IPC 0
16	INTACK	41	ABUS 6	T	TTY serial out −	w	IPC 1
17	R/$\overline{\text{W}}$	42	ABUS 5	U	RS232 ground	x	IPC 2
18	WRP	43	ABUS 3	V	RS232 output	y	IPC 3
19	RUN/$\overline{\text{WAIT}}$	44	ABUS 0	W	TTY tape reader out +	z	IPC 4
20	OPREQ	45	ABUS 1	X	TTY tape reader out −	$\overline{\text{a}}$	IPC 5
21	M/$\overline{\text{IO}}$	46	ABUS 4	Y	RS232 input	$\overline{\text{b}}$	IPC 6
22	$\overline{\text{OPACK}}$	47	ABUS 2	Z	COPC	$\overline{\text{c}}$	IPC 7
23	CLOCK	48	+12 V	a	OPC 0	$\overline{\text{d}}$	+12 V
24	$\overline{\text{OPEX}}$	49	−12 V	b	OPC 1	$\overline{\text{e}}$	−12 V
25	$\overline{\text{RESET}}$	50	+5 V	c	OPC 2	$\overline{\text{g}}$	+5 V

* J7 has no connections to these pins.

** NC = No Connection.

Microprocessor Demonstration System (continued)

Extended I/O DIL sockets			Non-extended I/O DIL sockets		
pin no.	function J5	function J6	pin no	function J3	function J4
1	$\overline{DBUS0}$	ABUS 0	1	(Output Port C) 0	(Output Port D) 0
2	$\overline{DBUS1}$	ABUS 1	2	OPC 1	OPD 1
3	$\overline{DBUS2}$	ABUS 2	3	OPC 2	OPD 2
4	$\overline{DBUS3}$	ABUS 3	4	OPC 3	OPD 3
5	$\overline{DBUS4}$	ABUS 4	5	OPC 4	OPD 4
6	$\overline{DBUS5}$	ABUS 5	6	OPC 5	OPD 5
7	$\overline{DBUS6}$	ABUS 6	7	OPC 6	OPD 6
8	$\overline{DBUS7}$	ABUS 7	8	OPC 7	OPD 7
9	$\overline{OPACK}$	ABUS 8	9	Clock Output Port C	Clock Output Port D
10	M/$\overline{IO}$	ABUS 9	10	Enable Input Port C	Enable Input Port D
11	OPREQ	ABUS 10	11	(Input Port C) 7	(Input Port D) 7
12	RUN/$\overline{WAIT}$	ABUS 11	12	IPC 6	IPD 6
13	WRP	ABUS 12	13	IPC 5	IPD 5
14	R/$\overline{W}$	ABUS 13	14	IPC 4	IPD 4
15	INTACK	ABUS 14	15	IPC 3	IPD 3
16	E/$\overline{NE}$	$\overline{PAUSE}$	16	IPC 2	IPD 2
17	$\overline{DMA}$	$\overline{INTREQ}$	17	IPC 1	IPD 1
18	D/$\overline{C}$	CLOCK	18	IPC 0	IPD 0

TTY interface DIL socket		RS232 interface connector	
pin no.	function J1	pin no.	function J2
1	TTY serial in +	1	RS232 ground
2	TTY serial in –	2	RS232 input
8	TTY tape reader out –	3	RS232 output
9	TTY tape reader out +	5	jumper
13	TTL serial out –	6	jumper
14	TTL serial out +	7	RS232 ground
		8	jumper
		20	jumper

Intelligent Typewriter Controller
2650PC3000

The 2650PC3000 is a basic text generating system requiring only six integrated circuits including one 2650 microprocessor. The serial communication link between the 2650 and the users terminal is accomplished with the flag and sense lines on the microprocessor. The 2650PC3000 is used to control the storage of characters entered from a terminal with either a current loop or voltage swing capability (±7,5 V min).

Control Characters allow the text to be printed out on the terminal with the capability for inserting unique characters at locations identified during text generation. When the text is printed out the entire text will be output unless a control character is detected. The microprocessor then stops the print-out and the operator enters the desired unique information. Another control character is then given to continue printing the text until all characters stored in memory are printed or until another stop character is detected. The stop character is recorded in memory just like any other character; however, it is not printed during text print-out.

Additional control characters allow for the erasure of the previous character typed or the erasure of the entire memory.

Features

- total of six IC packages
- operates at +5 V at a max of 500 mA
- interface to either current loop or device capable of sending and receiving a minimum voltage swing of ±7,5 V referenced to signal ground
- 250 character storage capability
- card size less than 7,5 x 10 cm with four screwed-on stand-offs at corners
- 1 MHz clock implemented with 74123 one-shot
- variable baud rate between 110 and 300 baud by trimmer pot adjustment of clock
- PROM mounted in 24-pin socket
- card edge connector supplied with each card
- inputs provided for an external system reset

Parts descriptions

2650	8-bit TTL compatible N-Channel Microprocessor incorporating a serial I/O Port. (See 2650 Hardware Specification Manual for complete description – 2650BM1000.)
2606	1024-bit static MOS, TTL compatible RAM memory organized as 256 words by 4 bits/word
82S115	4096-bit Bipolar TTL compatible PROM organized as 512 words by 8 bits/word
N7426	Quad 2-input high voltage NAND gate with open collector capable of driving voltage and current loop interfaces (20 mA max)
74123	Dual retriggerable monostable multivibrator with clear configured as a clock for 2650
Potentiometer	Helipot series 91C 50 kΩ, 9,5 mm cermet trimming potentiometer
PC edge connector	Amphenol – 225-21021-401-117 Cinch – 251-10-30-160

Miscellaneous components consist of eleven ¼ W and two ½ W resistors, and two mica, one ceramic and one tantalum capacitor.

The following are required to make the board functional but are not supplied with the card:
RS232 type connector for voltage swing interface: DB25P or DB25S
Reset switch – (normally open, connected to +5 V)
Power supplies: +5 V
±15 V

Intelligent Typewriter Controller (continued)

Terminal interface
voltage mode terminal connection

The voltage mode interface is very similar to the standard RS232 interface except that the "signal" ground cannot be connected to "protective" ground. When a Cinch type 25-pin connector (DB25P or DB25S) is used on an RS232 compatible terminal, the PC3000 should be connected as follows:

DB25P (DB25S) pin no.	PC3000 edge connector pin no.	PC3000 signal name
1	no connection	–
3	6	VS out +
2	J	VS in +
7	K	VS out – (signal GND)
5, 6, 8, 20	connect together	–

on card – jumper point A to C
and point D to E.

current loop terminal connection

When a terminal is used that employs current loop transmission techniques the four wires from the terminal should be connected to the corresponding four pins on the PC3000 card: TTY out +, TTY out –, TTY in +, and TTY in–.
on card – jumper point A to B
and point D to F.

PC3000 command summary

key	function
Rubout (delete)	Erase last character in memory and echo the erased character. Additional preceding characters can be erased by continuing to depress the delete key.
Control and E	Erase entire memory.
Control and B	Used to indicate beginning of inserted message. Is not printed but stored in memory. Stops print-out when read from memory. Required once from each unique information entry.
Control and C	Continues print-out of memory after entry of unique information.
Control and P	Prints out contents of terminal memory.
Control and R	Software reset.

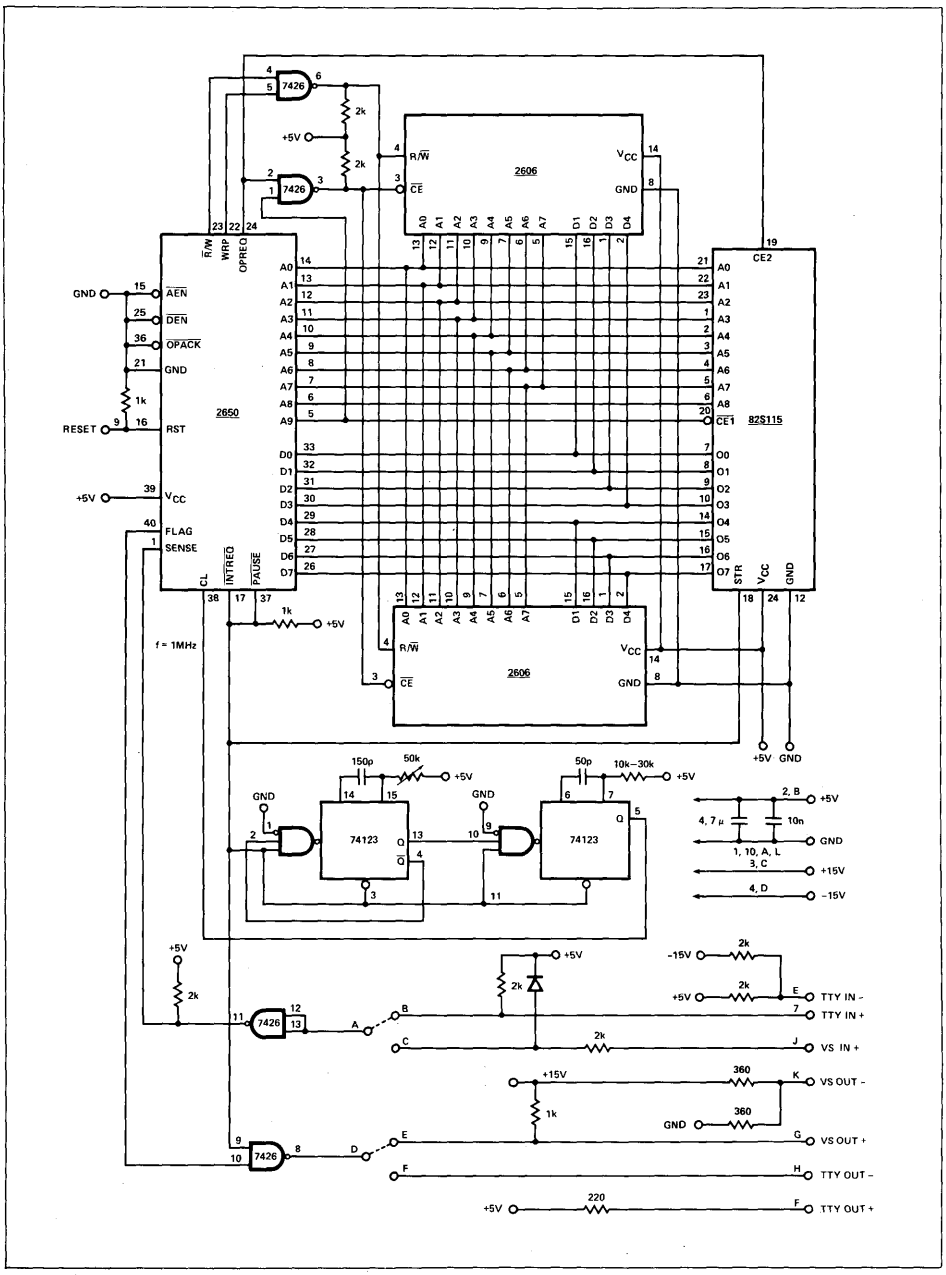
Note:
Bell will ring if any of the following are true
1. Entering more than 250 characters in memory.
2. Requesting print-out of an empty buffer.
3. Attempting to delete more characters than there are in memory.

PC3000 connector pin assignment

pin no.	function	pin no.	function
1	GND	A	GND
2	+5	B	+5
3	+15	C	+15 V
4	–15	D	–15
5	–	E	TTY in –
6	VS out +	F	TTY out +
7	TTY in +	H	TTY out –
8	–	J	VS in +
9	RESET	K	VS out – (Signal Ground)
10	GND	L	GND

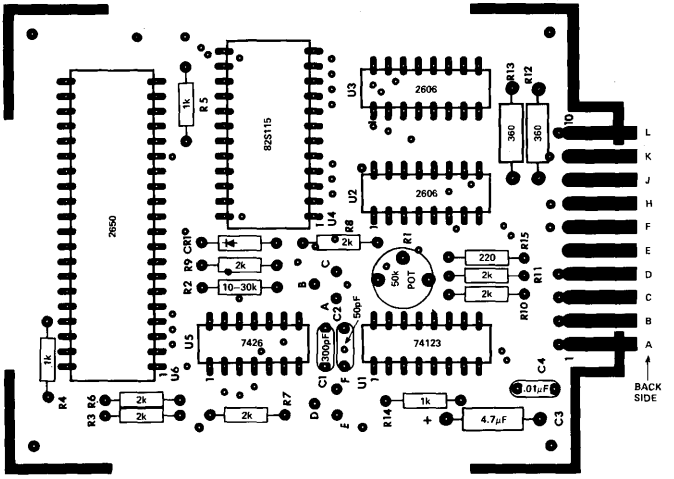
VS – Voltage Swing

Intelligent typewriter controller

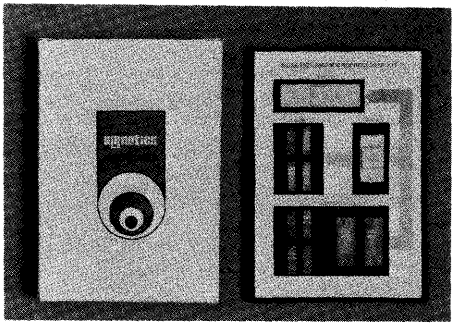


Intelligent Typewriter Controller (continued)

Intelligent typewriter controller board layout



Microprocessor Prototyping Kit
2650KT9100



The KT9100 kit contains a 2650 microprocessor and enough chips to implement a small development system. Since the interface requirements of the 2650 are completely TTL compatible, no attempt has been made to limit the user's flexibility by dictating a fixed logic configuration. There is complete freedom in using standard SSI or MSI logic to adapt the microprocessor to the memory, I/O devices, or clock.

Several simple system examples are presented to enable quick set up and evaluation. Other configurations to adapt to individual requirements should become evident from these examples.

Parts descriptions

2112: The 2112 is a static 1024-bit RAM organized as 256 words by 4 Bits/Word. It is manufactured with n-channel, silicon gate, MOS technology and achieves an access time of less than 800 ns. No clocks are required, and the chip is powered from a single 5 V source.

82S115I: The 82S115I is a 4096-bit Schottky-Clamped, bipolar PROM incorporating on-chip data output registers. It is field-programmable and fully TTL compatible with on-chip decoding and two chip enable inputs for easy memory expansion. Inputs to the device are pnp transistors with a maximum current requirement of 100 μA.

8T31: The 8T31 is an 8-bit Bidirectional I/O Port designed to function as a general purpose I/O interface element. It consists of 8 clocked latches with two sets of bidirectional Inputs/Outputs allowing master control from either the microprocessor or from the I/O device.

8T26B: The 8T26B consists of four pairs of inverting three-state logic elements configured as Quad Bus Drivers/ Receivers with separate buffered receiver enable and driver enable lines. Both the driver and receiver gates have three-state outputs and low-current pnp inputs.

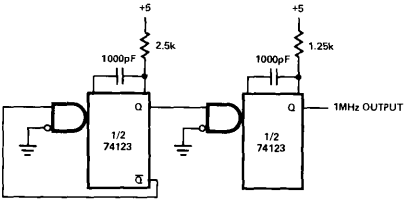
Circuit examples

Two circuit configurations are presented to indicate a possible program checkout approach. The first allows the use of RAM for program debugging. The second figure represents a possible final system configuration with the program fixed in PROM. Both circuits use the 8T26s as bus buffers.

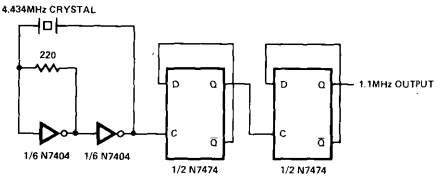
Parts list

part no.	qty	description
2650	1	CPU
2112	4	256 x 4 RAM
82S115I	1	4k PROM (Unprogrammed) 512 x 8
8T31I	2	8-bit Bidirectional I/O Port
8T26B	4	Quad Bus DR/REC

One-shot clock oscillator circuit

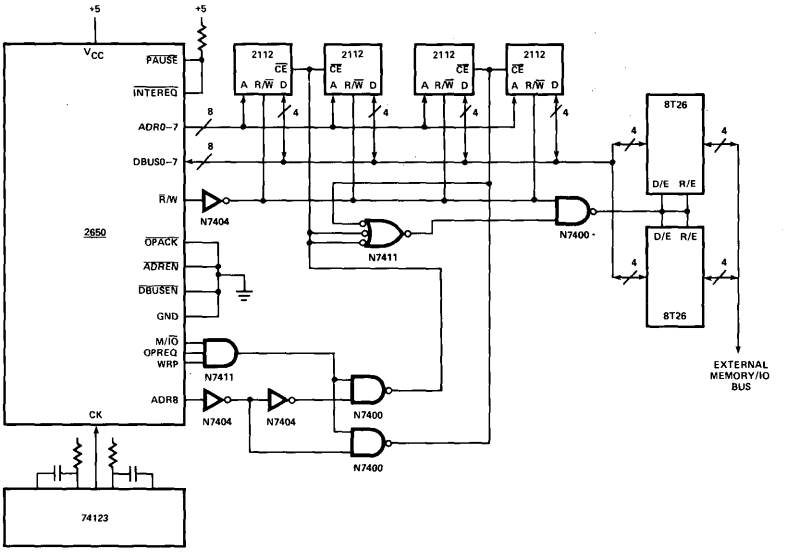


Crystal oscillator circuit

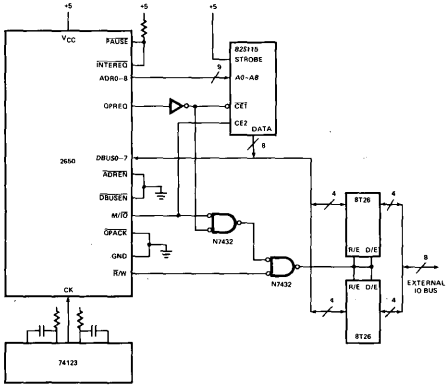


Microprocessor Prototyping Kit (continued)

Example of initial program checkout configuration



Finalized configuration with program fixed in PROM



2650 Assembler Version 3.2
2650AS1000/1100

The 2650 assembly language (PIPHASM) is a symbolic language designed specifically to facilitate the writing of programs for the 2650 microprocessor.

The AS1000 is for 32-bit or larger machines and the AS1100 is for 16-bit machines.

The 2650 assembler is a program which accepts symbolic source code as input and produces a listing and/or an object module "Hexadecimal" format compatible to the two tape punching programs PIPHTAP (for acceptance by PIPBUG), PIPSTAP (for PROMs) and also to the simulator, PIPSIM.

The assembler is written in standard Fortran IV and is approximately 1 250 Fortran card images in length. It is modular and may be executed in an overlay mode should memory restrictions make that necessary. It operates in a two-pass mode to build a symbol table, to issue helpful error messages, produce an easily readable program listing and output a computer-readable object module. This version of the assembler compiles into a 12k word load module on the PDP-11/40 (16-bit words) and executes under DOS (8k) within a 28k memory.

Availability

The 2650 assembler is available on both NCSS and GE timeshare. It is also available from Signetics on 9-track magnetic tape written in EBCDIC in 80-character unblocked records at a density of 800 bpi.

Features

- forward references
- pseudo-ops to aid programming
- self-defining constants
- symbolic machine operation codes
- free format source code
- syntax error checking
- symbolic address assignment and references
- data creation statements
- storage reservation statements
- assembly listing control statements
- addresses can be generated as constants
- character codes may be specified as ASCII or EBCDIC
- comments and remarks may be encoded for documentation

Language requirements

I. Input requirements

Input to the assembler consists of a sequence of characters combined to form assembly language elements. These language elements include symbols, instruction mnemonics, constants and expressions which make up the individual program statements that comprise a source program.

A. Characters

alphabetic:	A-Z
numeric	0-9
special characters	blank
	(left parenthesis
	) right parenthesis
	+ add or positive value
	– subtract or negative value
	* asterisk
	' single quote
	, comma
	/ slash
	$ dollar sign
	< less than sign
	> greater than sign

B. Symbols

Symbols are formed from combination of characters. Symbols provide a convenient means of identifying program elements so they can be referenced by other elements.

C. Constants

A constant is a self-defining language element. Unlike a symbol, the value of a constant is its own "face" value and is invariant. Internal numbers are represented in 2s complement notation. There are two forms in which constants may be written: the Self-Defining Constant and the General Constant.

Self-Defining Constant

The self-defining constant is a form of constant which is written directly in an instruction and defines a decimal value.

General Constant

The general constant is also written directly in an instruction, but the interpretation of its value is dictated by a code character and delimited by quotation marks. Its form can be binary, octal, decimal, hexadecimal, EBCDIC or ASCII.

D. Expressions

An expression is an assembly language element that represents a value. It consists of a single term or combination of terms separated by arithmetic operators. A term may be a valid symbolic reference, a self-defining constant or a general constant.

2650 Assembler Version 3.2 (continued)

II. Fields

A statement prepared for processing by the assembler is logically divided into four fields, as indicated below. They are free form and are separated by at least one blank character. The name must begin in logical column 1.

Label	Operation	Operand	Comments
name	opcode	operand(s)	

Where:

Label field	contains an optional label which the assembler will assign as the symbolic address of the first byte of the instruction.
Operation field	contains any of the 2650 processor mnemonic operation codes or any assembler Directive. This field may include an expression which specifies a register or value as required by the instruction. All symbols used in this field must have been previously defined, i.e. no symbolic forward references are allowed.
Operand field	contains one or more operand elements such as indirect address indicator, operand expression, index register specification, auto-increment/ auto-decrement indicator, constant specification, etc. depending on the requirements of the particular instruction.
Comments field	any characters following the operand field will be reproduced in the assembly listing without processing. The Comments Field must be separated from the argument field by at least one blank.

III. Directives

There are eleven directives which the assembler will recognize. These assembler directives, although written much like processor instructions, are simply commands to the assembler instead of to the processor. They direct the assembler to perform specific tasks during the assembly process, but have no meaning to the 2650 processor. These assembler directives are:

ORG	Set location counter
EQU	Specify a symbol equivalence
ACON	Define address constant
DATA	Defines memory data
RES	Reserve memory storage
END	End of assembly
EJE	Eject the listing page
PRT	Printer control
SPC	Space control
TITL	Title
PCM	Punch control

2650 Simulator Version 1.2
2650SM1000/1100

The 2650 Simulator (PIPSIM) is a Fortran IV program which allows a user to simulate the execution of his program without utilizing the 2650 processor. The simulator executes the 2650 program via host computer software by maintaining its own internal Fortran storage registers to describe the 2650 program, the microprocessor registers, the ROM/RAM memory configuration, and the input data to be read dynamically from I/O devices. Inputs to the simulator are the object module (or the 2650 program in object format) produced by the 2650 assembler and a deck of user commands. The simulator can accommodate an object module of up to 8192 Bytes.

The output consists of a listing of the user's commands and a print out of both static and dynamic information as requested by the commands. The user may request traces of the processor status, dumps of the contents of memory, and recording of program timing statistics. Multiple simulations of the same program with different parameters may be executed during one simulation run.

The SM1000 is configured to operate on 32-bit or larger machines and executes under DOS (8k) within a 28k memory. The SM1100 is configured for 16-bit machines and compiles into a 16k word load module on a PDP-11/40.

Availability
The 2650 Simulator is available on both NCSS and GE timeshare. It is also available from Signetics on a 9-track magnetic tape written in EBCDIC in 80-character unblocked records at a density of 800 bpi.

Features
- cycle counter for timing estimates
- instruction fetch break points
- operand fetch break points
- trace facilities
- snapshot dumps
- patching facility
- statistical information generated
- easy-to-use command language
- optionally selected start and end addresses
- simulated registers may be displayed while the simulation program is executed
- simulated registers may be altered while the program is executing
- maintains a 2k cell (easily modified to 8k) to simulate a read/write RAM
- capability exists for configuring parts of simulator memory to look like ROM
- incorporates a 200-byte first in, first out (FIFO) buffer to store the data read from a simulated input device
- establishes initial program conditions
- monitors execution sequences

User commands
Commands specify how the program is to run and what data is to be recorded. The simulator accepts information in card image form. The entire card is read in Fortran "A" format, and one command must be complete on one card. Comments may appear in any order within a command set.

The basic manual set (2650BM1000) contains a complete description of the user commands and the general operation of the simulator.

2650 Simulator Version 1.2 (continued)

command name	parameters	description
DUMP	LOC, FWA-LWA(;....;LOC, FWA-LWA)	Display the area of memory, FWA-LWA, whenever the instruction at LOC executes.
REND	NONE	Execute the last simulation and terminate the entire run.
INPUT	VALUE (;....;VALUE)	Define the data to be read by simulated I/O instructions.
INSTR.	LOC(;....;LOC)	Display the processor state whenever the instruction at LOC executes.
LIMIT	NO	Specify the total number of instructions executed.
PATCH	LOC, VALUE(;....;LOC,VALUE)	Initialize each memory location, LOC, to VALUE
REFER.	LOC(;....;LOC)	Display the processor state whenever the instruction at LOC is referenced by another instruction.
SETP.	LOC(,PSL=VALUE), (,PSU=VALUE)	Set the program status byte (lower and/or upper) to VALUE whenever the instruction at LOC executes.
SETR.	LOC (9, R0=VALUE)...(R6=VALUE)	Set the general purpose registers to VALUE whenever the instruction at LOC executes.
SROM	FWA-LWA	Specify the boundaries of Read-Only Memory.
START	LOC	Start the simulated program execution at LOC.
STAT	None	Display instruction statistics at end of program execution.
STOP.	LOC(;....;LOC)	Terminate the program execution when the instruction at LOC executes.
TEND	None	Execute the last simulation and prepare to read the User Commands for the next simulation.
TRACE.	FWA-LWA(;....;FWA-LWA)	Display the processor state whenever an instruction executes, which lies within the area of memory, FWA-LWA.

Higher Level Language (PLμS)
2650PL1000

The higher level language is designed for use with the 2650 microprocessor. This language allows the programmer to reduce programming effort while retaining the control and efficiency of assembly language. It is written in ANSI standard Fortran IV and will execute on most machines without alteration. Programs written in this language tend to be self-documenting and are easily altered.

The higher level language is a sequence of "Declarations" and "Executable Statements".

The declarations allow the programmer to control allocation of storage, define simple textual substitutions (Macros), and define procedures. The language is "Block Structured": procedures may contain further declarations which control storage allocation and define other procedures.

The procedure definition facility of the language allows modular programming: a program can be divided into sections (e.g. teletype input, conversion from binary to decimal forms, and printing output messages). Each of these sections is written as a language procedure. Such procedures are conceptually simple, easy to formulate and debug and easily incorporated into a large program. They may form a basis for a procedure library, if a family of similar programs is being developed. Procedures may be individually compiled.

The language handles two kinds of data, its two basic "Data Types": byte and address. A byte variable or constant is one that can be represented as an 8-bit quantity; an address variable or constant is a 16-bit or double-byte quantity. The programmer can declare variable names to represent byte or address values. One can also declare vectors (or arrays) or type byte or address.

In general, executable statements specify the computational processes that are to take place. To achieve this, arithmetic, logical (Boolean), and comparison (relational) operators are defined for variables and constants of both types (BYTE and ADDRESS). These operators and operands are combined to form EXPRESSIONS, which resemble those of elementary algebra. Expressions are a major component of language statements.

A simple statement form is the assignment statement, which computes a result and stores it in a memory location defined by a variable name. Other statements in the language perform conditional tests and branching, loop control, and procedure invocation with parameter passing. The flow of program execution is specified by means of powerful control structures that take advantage of the block-structured nature of the language. Input and output statements read and write 8-bit values from and to input and output ports. Procedures can be defined which use these basic input and output statements to perform more complicated I/O operations.

A method of automatic text-substitution (more specifically, a "compile-time macro facility") is also provided. A programmer can declare a symbolic name to be completely equivalent to an arbitrary sequence of characters. As each occurrence of the name is encountered by the compiler, the declared character sequence is substituted, so the compiler actually processes the substituted character string instead of the symbolic name.

The compiler supports compile time expression evaluation and conditional compilation which allows selective compilation of code depending on an input parameter at compile time.

The language generates absolute and/or relocatable code. The relocatable modules may be linked by a powerful linkage editor at load time.

Additionally the language contains all machine independent features of the PL/M language as a subset, thereby enhancing portability of programs.

Availability

The higher level language is available on NCSS timeshare. It is also available from Signetics on magnetic tape for 16 and 32-bit machines.

Features

- written in free-form
- adaptable to both 16 and 32-bit machines
- block structured
- employs procedure calls
- byte and address data elements
- based variables
- in-line assembly language
- Macro capability
- generates relocatable code supported by a relocating loader
- includes PL/M as a subset
- allows separate compilation of program modules
- has improved control structure over PL/M
- conditional compilation
- compile time expression evaluation

Microcomputer Prototype Development System TWIN

The Microprocessor Prototype Development System is a modular system designed to support development and implementation of 2650 microcomputer systems.

A typical system consists of three hardware elements: a Prototype Development Computer (PDC), a floppy disk storage subsystem, and a system console (typically an ASR33 teletype). The PDC includes an integral MOS and bipolar PROM programmer and an in-circuit emulation/hardware debug facility. A wide range of PDC cards and system peripherals are available.

System software includes an Operating System, File Management, Debug Software, Text Editor, and 2650 Resident Assembler. These programs provide the user with the tools to perform his software development easily and quickly. These software capabilities, together with the capacity and performance of the floppy disk subsystem, and the in-circuit emulation/hardware debug capability significantly reduce the time and cost of a microcomputer system development project.

The Microprocessor Prototype Development System introduces a unique new Multiprocessor architecture for prototyping systems. This architecture provides users with the benefits of maximum availability of common (user) memory space and a Master processor/Operating System that is isolated and independent from the user system in the in-circuit emulation/hardware debug mode.

The Microprocessor Prototype Development System will have a long life cycle, since it is designed with the capability of supporting future microprocessors, additional peripherals and expanded software support and hardware debug capabilities.

Hardware features

Modular microprocessor prototype development system to support development, implementation and check out of 2650 microcomputer systems.

Powerful new Multiprocessor architecture provides maximum memory space to user and a protected environment for the Master processor/Operating System at all times.

The 2650 microprocessor –5 V only, fully TTL compatible, 2,4 μs cycle time, easy-to-learn instruction set – is used for the Master and Slave microprocessors.

Hardware interfaces and software drivers provided for floppy disk storage subsystem, TTY, CRT terminal, paper tape reader, line printer and EIA RS232 terminals.

In-circuit emulation/hardware debug and powerful debug software provides extensive emulation and diagnostic facilities for the user system.

Integral MOS and bipolar PROM programmers.

User/Common memory of 16k bytes, expandable to 64k bytes.

Two universal bus structures with multiprocessor and DMA capabilities.

Eight-level maskable priority interrupt system available to the user.

Software features

System software provided with the Prototype Development System includes the Signetics Disk Operating System (SDOS), text editor, debug package, 2650 assembler and linkage editor.

The Signetics Disk Operating System (SDOS) provides complete control over operation of all portions of the Prototype Development System. All functions relating to file handling, loading and execution are included, as well as provision for invoking the debug system and PROM programming functions.

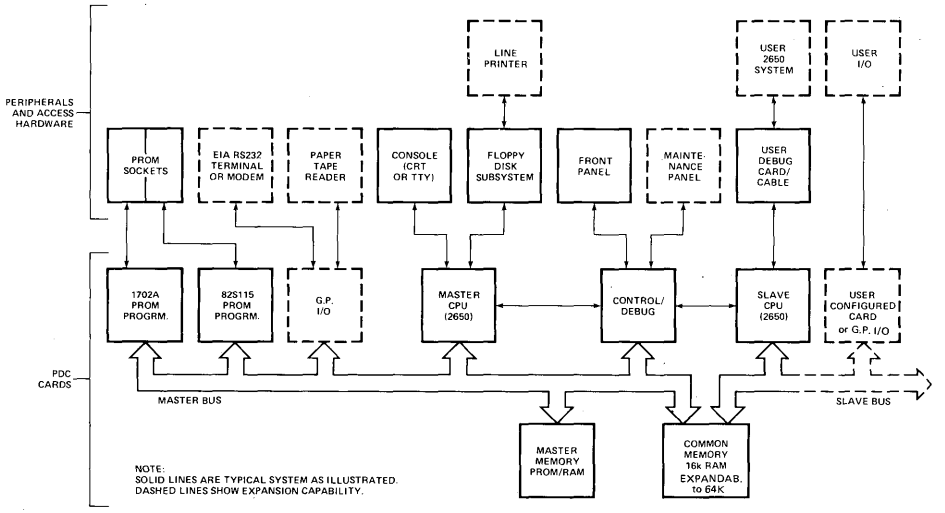
The SDOS software has been designed to allow the user to create, edit, and assemble files; obtain object and listing outputs; load and execute programs; and through the debug system, check out programs in a most efficient manner.

SDOS provides a powerful procedure capability which gives the user the capability of creating powerful and customized operating system commands dynamically.

Programs may be read and written in either hexadecimal or SMS (Signetics Memory Services) format for (P)ROM programming.

The SDOS software provides a flexible input/output system which is organized through logical channels allowing the user to dynamically assign any logical channel to any physical device or file within the system. Thus, system I/O devices may be dynamically assigned using SDOS commands either from the console or from within a user's program.

Typical system



SDOS assumes a dual CPU environment with one CPU designated as a master and the other as a slave. SDOS resides in a dedicated memory consisting of ¼k PROM and 16k of RAM running under the master CPU.

SDOS will control a multidrive floppy disk subsystem (up to 8 drives), a line printer, a high speed paper tape reader and an ASR-33TTY compatible console. Drivers are provided within SDOS for these I/O devices. In addition, the user may write his own driver for other peripheral devices and easily link them into the SDOS system.

The Prototype Development System Resident Assembler translates symbolic 2650 assembly language instructions into appropriate machine language code.

Microcomputer Prototype Development System (continued)

The Assembler produces absolute object code. The absolute object code produced is in hexadecimal format which may be converted by an SDOS command to SMS format for PROM or ROM programming.

The Text Editor is a comprehensive software package which allows the user to enter and modify text files. The Text Editor is line oriented and accepts inputs from an input file, performs modifications in a work space and outputs the revised text to an output file.

The Debug System is a software program which will provide the user with run-time program debug capabilities within a hardware environment. It utilizes special hardware features built into the program development system to control the execution of the user's program. User programs operating under the debug system will have dynamic program trace, breakpoint capabilities, memory modification capabilities, and status reporting on the memory, program, and internal processor status.

All of the above-described software will be supplied in object format on diskette and is provided with each Prototype Development System.

PDC cards

Master CPU
System Crystal Clock
Master 2650
UART/TTY Interface
Real Time Clock
Disk/Paper tape Port

Control/debug
Debug Logic
Master/Slave Interaction
Interrupt Logic
Front Panel Interface

Slave CPU
Slave 2650
User Cable Interface

Master memory
4k-Byte Static NMOS RAM
2k-Byte 1702A Erasable PROM

Common memory – 4k RAM
4k-Byte Static NMOS RAM

Common memory – 16k RAM
16k-Byte Dynamic NMOS RAM

General purpose I/O
EIA Interface
Four Output Ports
Four Input Ports
8 Interrupt Lines

1702 PROM programmer

82S115 PROM programmer

User configurable card
For interfacing directly with users own I/O devices.

Extender card

Peripherals

Floppy disk subsystem
Expandable to 8 drives

Line printer (optional)

High speed paper tape reader (optional)

Teletype (optional)

CRT terminal (optional)

A.C. power requirements
50 Hz or 60 Hz, 115/230 VAC

military products

process levels

The Signetics Mil 38510/883 program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customers to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to tables.

JAN qualified (JB)

JAN qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC qualified products list (QPL-38510).

Group B testing, per Mil-Std-883 method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN qualified products also possess a requirement for a standard marking used throughout the IC industry.

/883B(RB)

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 method 5004, and is 100% electrically tested to industry data sheets.

Group B, C and D testing is performed per Mil-Std-883 method 5005, in accordance with the Signetics military generic data program. Offshore assembly is allowed.

MIL temp/883C (S/RC)

If you need a Military temperature range device, but do not require all the high reliability screening performed in the other processing options, our Mil-Temp. product is ideal. Mil-Temp. parts are the standard full Mil-Temperature range product guaranteed to a 1% AQL to the Signetics data sheet parameters.

military products

military generic data

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity of running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all military generic data is controlled and audited by both government inspection in the case of JAN data and Signetics quality assurance.

Signetics military generic data is compiled by the Military Products Division based on data from:

1. JAN quality conformance lots.
2. Data generated by quality conformance lots run for other reliability programs. Refer to table.

A military generic family is defined as consisting of die function and package type families.

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

Definition and qualifying manufacturing periods for generic data

qualified sub-groups	qualifies	option 1	option 2
A	Electrical Test	Group A is performed on each lot or sublot of Signetics devices.	Group A is performed on each lot or sublot of Signetics devices.
B	Package Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied.	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

Summary
Package availability
Products processing matrix

X = applicable

Military summary

	JB JAN qualified	RB /883	S Mil temp.
54/54H	X	X	X
54LS	X	X	X
54S	X	X	X
82/8T	X	X	X
93xx	X	X	X
96xx	–	X	X
Linear	X	X	X
Bipolar Memory	planned	X	X
Microprocessor	–	X	X

Military package availability

JAN case outline and lead finish	Signetics military package types				
	metal can		dual-in-line		
	8-pin	10-pin	14-pin	16-pin	24-pin
CB	–	–	F	–	–
EB	–	–	–	F	–
JB	–	–	–	–	I/F
DB	–	–	W	–	–
FB	–	–	–	W	–
ZC	–	–	–	–	Q
GC	T	–	–	–	–
IC	–	K	–	–	–

Military products processing matrix

process level and marking	pre-cap visual	burn-in	functional test	d.c./a.c. at 25 °C	d.c./a.c. at temp.	QPL	offshore assembly
JB JM38510/xxxxx	883B	yes	100%	100%	100%	yes	no
RB Sxxxx/883B	883B	yes	100%	100%	100%	no	yes
RC/S Sxxxx/883C	883B	no	100%	100% d.c. sample a.c.	sample d.c. only	no	yes

military products

requirements and screening flows

description of requirements and screens	MIL-M-38510 and MIL-STD-883 requirements, methods and test conditions	requirement	processing levels class A	JAN qualified (JB)	/883B (RB)	/883C (RC)
General Mil-M-38510						
1 Pre-certification a Prod. assurance program plan b Manufacturer's certification	The manufacturer shall establish and implement a products assurance program plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	n.a.	n.a.
2 Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	n.a.	n.a.
3 Device qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C and D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	n.a.	n.a.
4 Traceability	Traceability maintained back to a production lot, Para. 3.4.6	—	X	X	X	X
5 Country of origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	n.a.	n.a.
Screening per method 5004 of Mil-Std-883						
6 Internal visual (pre-cap)	2010. cond. A or B	100%	XA	XB	XB	XB
7 Stabilization bake	1008. cond. C min; (24 h at 150 °C)	100%	X	X	X	X
8 Temperature cycling For class B and C devices thermal shock may be substituted, 1011, cond. A; (15 cycles, 0 to +100 °C)	1010. cond. C (10 cycles, –65 to +150 °C)	100%	X	X	X	X
9 Constant acceleration	2001, cond. E; (30 000g in Y1 plane)	100%	X	X	X	X
10 Visual inspection	There is no test method for this screen; it is intended only for the removal of 'Catastrophic Failures' defined as 'Missing Leads, Broken Packages or Lids Off'.	100%	X	X	X	X
11 Seal (hermeticity)	1014					
a Fine	cond. A or B (5,0 x 10^{-8} cm^3/s)	100%	X	X	X	X
b Gross	cond. C2 min.	100%	X	X	X	X
12 Interim electricals (pre-burn-in)	Per applicable device specification	100% optional	100% read & record	slash sheet	data sheet	n.a.
13 Burn-in	1015. cond. as specified (min 160 h at 125 °C)	100%	100% 240 h	X	X	n.a.

X = applicable
n.a. = not applicable

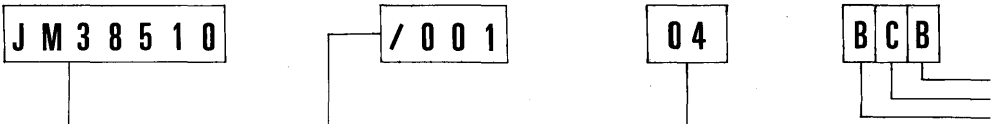
description of requirements and screens	MIL-M-38510 and MIL-STD-883 requirements methods and test conditions	requirement	processing levels class A	JAN qualified (JB)	/883B (RB)	/883C (RC)
Screening per method 5004 of Mil-Std-883 (cont.)						
14 Final electricals	Per applicable device specification	100%	100% read & record	slash sheet	data sheet	data sheet
a Static tests, at 25 °C	Sub-group 1		X	X	X	X
b Static tests, at +125 °C	Sub-group 2		X	X	X	n.a.
c Static tests, at −55 °C	Sub-group 3		X	X	X	n.a.
d Dynamic test, at 25 °C	Sub-group 4 (for linear product mainly)		X	X	X	X
e Functional test, at 25 °C	Sub-group 7		X	X	X	X
f Switching test, at 25 °C	Sub-group 9		X	X	X	n.a.
15 Percent Defective Allowable (PDA)	A PDA of 10% is a normal requirement applied against the static test at 25 °C (A-1). This is controlled by the slash sheets for JB & JBX products. For RBX & RB 10% is standard.	10%	5%	X	X	n.a.
16 Marking (between brackets meaning of xxxx)	Fungus inhibiting paint	100%	as req'd	JM38510 /xxx (slash sheet no)	Sxxxx /883B (Sig. basic no)	Sxxxx /883C (Sig. basic no)
17 X-ray	2012		100%	n.a.	n.a.	n.a.
18 External visual	2009	100%	X	X	X	X
Quality conformance inspection per method 5005 of Mil-Std-883						
19 Group A	Electrical tests — final electricals (no 14 above) repeated on a sample basis. (Sub-groups 1 to 12 as specified).	each lot	X	X	X	X
20 Group B	Package functional and constructional related test i.e. package dimensions, resistance to solvents, internal visual and mechanical, bond strength and solderability.	every 6 weeks per package type	X	X	generic data available	
21 Group C	Die related tests i.e. 1000 h operating life, temperature cycling and constant acceleration.	every 3 months per microcircuit group	n.a.*	X	generic data available	
22 Group D	Package related tests i.e. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration and salt atmosphere.	every 6 months per package type	X	X	generic data available	

* For class A devices these tests are included in Group B.

military products

JAN 38510 type numbers – what they mean

The following chart is offered for your reference to help take some of the mystery out of JAN part number marking. For an example, we will take the marking for a 5400F processed to JAN and explain its meaning as well as other options.



MILITARY DESIGNATOR

calls out

MIL-M-38510

JAN IC

The "J" in the marking is very important.

If it's not there it's not a JAN device.

DO NOT be confused by JAN equivalents marked M38510.

DETAIL SPECIFICATION

refers to detail slash sheet spec 001, 002, 003 ----

A slash sheet detail spec will usually represent a family of devices with similar functions.

i.e. the /001

detail spec represents many positive NAND gates such as the 5400, 5401, 5403, 5410, 5420 and 5430 etc.

The /002 detail spec on the other hand represents many flip-flop functions such as the 5472, 5473, 54107, 5476, 5474, 5470 and so on for the rest of the slash sheets.

DEVICE TYPE

refers to a specific part type under the detail spec.

This, plus the detail spec no. will denote a part type.

i.e.:

detail spec	+	dev. type	=	generic type
001		01	=	5430
001		02	=	5420
001		03	=	5410
001		04	=	5400

detail spec	+	dev. type	=	generic type
002		01	=	5472
002		02	=	5473
002		03	=	54107

and so on for the rest of the slash sheets.

Actual marking for our 5400F as it appears on the device.

date code

Signetics manufacturer's code (per Mil-M-38510)

DEVICE CLASS

calls out processing to either class A or C of MIL-STD-883

CASE OUTLINE

This code denotes the package i.e.:

A = ¼" x ¼" flat pack 14 pin

B = ¼" x ⅛" flat pack 14 pin

C = ¼" x ¾" 14 pin dual in-line

D = ¼" x ⅜" flat pack 14 pin

E = ¼" x ¾" 16 pin dual in-line

F = ¼" x ⅜" flat pack 16 pin

G = 8 lead metal can

H = ¼" x ¼" 10 pin flat pack

I = 10 lead metal can

J = ½" x 1¼" 24 pin dual in-line

K = ⅜" x ½" 24 pin flat pack

L = ⅜" x ½" 24 pin flat pack

Z = ¼" x ⅜" 24 pin flat pack

LEAD FINISH

A = Kovar or alloy 42 with hot solder dip

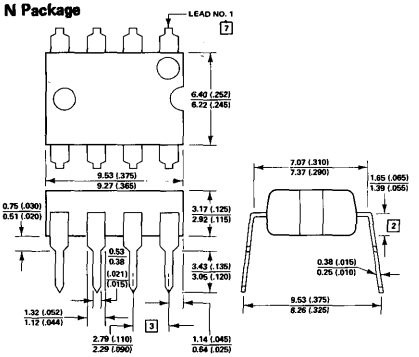
B = Kovar or alloy 42 with tin plate

C = Kovar or alloy with gold plate

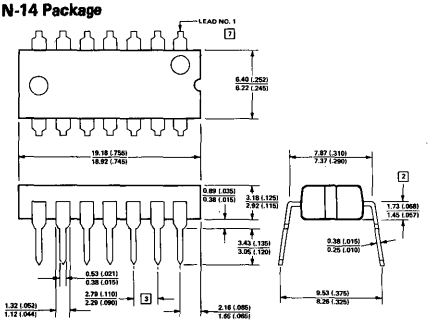
packages

PLASTIC: Standard Dual-In-Line Number of pins N Package: 8, 14, 16, 20, 22, 24, 28, 40
P Package: 16

N Package

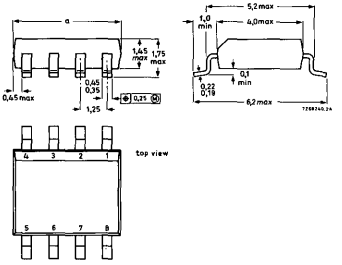


N-14 Package



PLASTIC: Miniature Dual-In-Line Number of pins SO Package: 6, 8, 10, 14, 16

SO Package (SO-8 as example)

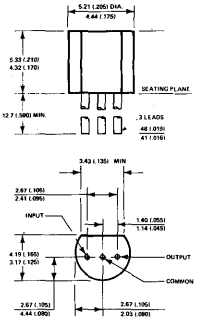


dimensions a

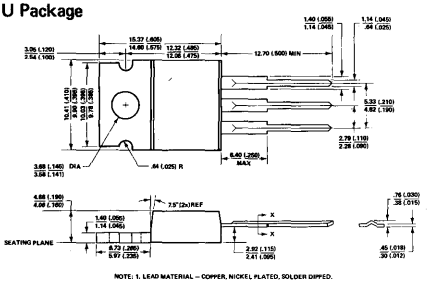
	SO-6	SO-8	SO-10	SO-14	SO-16
min.	3,55	4,8	6,05	8,55	9,8
max.	3,75	5,0	6,25	8,75	10,0

PLASTIC: Power

S Package

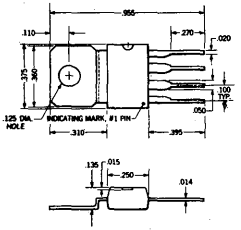


U Package



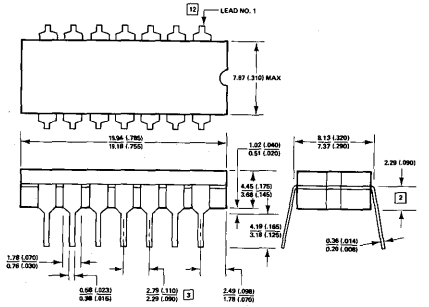
NOTE: 1. LEAD MATERIAL – COPPER, NICKEL PLATED, SOLDER DIPPED.

U1 Package

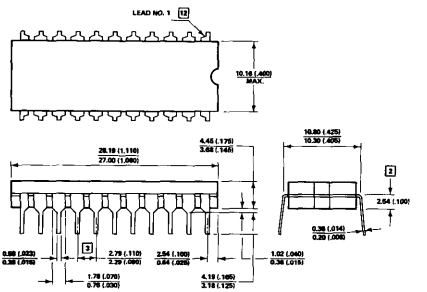


HERMETIC: Cerdip Number of pins **F Package: 14, 16, 18, 22, 24**

F Package 14 pin

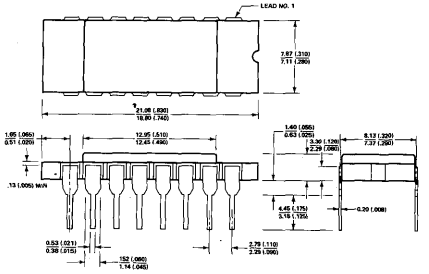


F Package 22-pin



HERMETIC: Metal ceramic Dual-in-Line Number of pins **E Package: 16, 18**
I Package: 16, 18, 24, 28, 40, 50

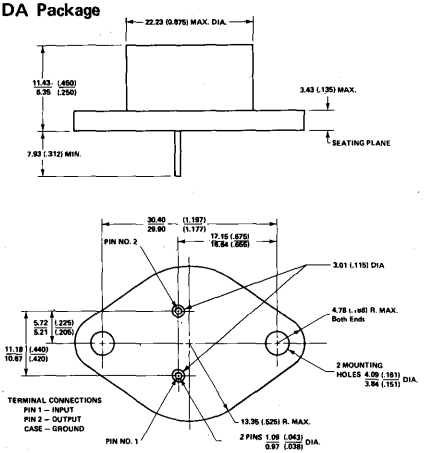
E or I package 16 pin



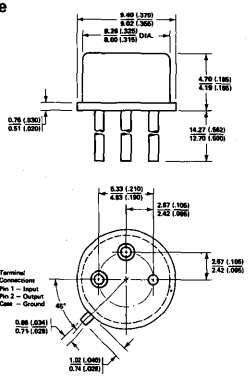
packages

HERMETIC: Metal Headers

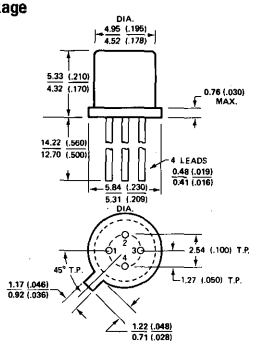
DA Package



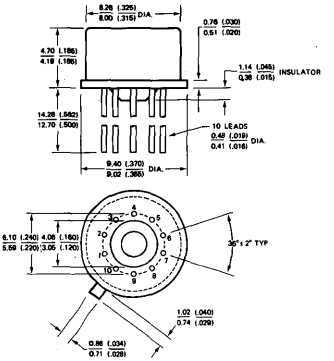
DB Package



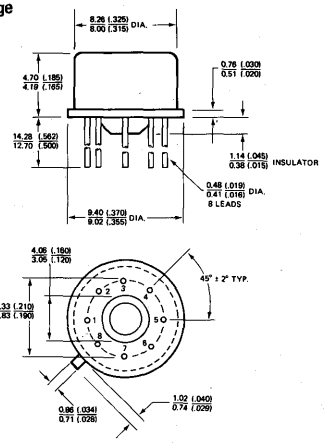
DE Package



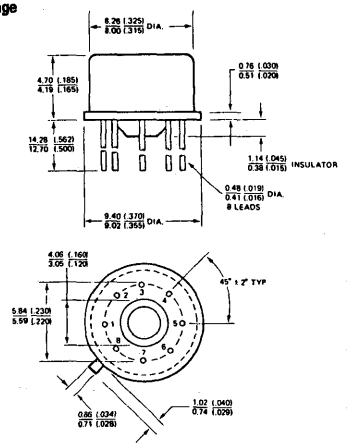
K Package



T Package



TA package



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