PHILIPS

Data handbook

PHILIPS

Electronic
components
and materials

Integrated circuits

Part 2 January 1984

Bipolar ICs for video equipment

PHILIPS

Bipolar ICs for video equipment

IC2

01-84

Electronic components and materials for professional, industrial and consumer uses from the world-wide Philips Group of Companies

Argentina: PHILIPS ARGENTINA S.A., Div. Elcoma, Vedia 3892, 1430 BUENOS AIRES, Tel. 541-7141/7242/7343/7444/7545.
Australia: PHILIPS INDUSTRIES HOLDINGS LTD., Elcoma Division, 67 Mars Road, LANE COVE, 2066, N.S.W., Tel. 427 08 88.
Austria: ÖSTERREICHISCHE PHILIPS BAUELEMENTE Industrie G.m.b.H., Triester Str. 64, A-1101 WIEN, Tel. 62 91 11.
Belgium: N.V. PHILIPS & MBLE ASSOCIATED, 9, rue du Pavillon, B-1030 BRUXELLES, Tel. (02) 242 74 00.
Brazil: IBRAPE, Caixa Postal 7383, Av. Brigadeiro Faria Lima, 1735 SAO PAULO, SP, Tel. (011) 211-2600.
Canada: PHILIPS ELECTRONICS LTD., Electron Devices Div., 601 Milner Ave., SCARBOROUGH, Ontario, M1B 1M8, Tel. 292-5161.
Chile: PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. 39-4001.
Colombia: SADAPE S.A., P.O. Box 9805, Calle 13, No. 51 + 39, BOGOTA D.E. 1., Tel. 600 600.
Denmark: MINIWATT A/S, Strandlodsvej 2, P.O. Box 1919, DK 2300 COPENHAGEN S, Tel. (01) 54 11 33.
Finland: OY PHILIPS AB, Elcoma Division, Kaivokatu 8, SF-00100 HELSINKI 10, Tel. 1 72 71.
France: R.T.C. LA RADIOTECHNIQUE-COMPELEC, 130 Avenue Ledru Rollin, F-75540 PARIS 11, Tel. 355-44-99.
Germany: VALVO, UB Bauelemente der Philips G.m.b.H., Valvo Haus, Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040) 3296-0.
Greece: PHILIPS S.A. HELLENIQUE, Elcoma Division, 52, Av. Syngrou, ATHENS, Tel. 9215111.
Hong Kong: PHILIPS HONG KONG LTD., Elcoma Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)-24 51 21.
India: PEICO ELECTRONICS & ELECTRICALS LTD., Elcoma Div., Ramon House, 169 Backbay Reclamation, BOMBAY 400020, Tel. 295144.
Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Elcoma Div., Panim Bank Building, 2nd Fl., Jl. Jend. Sudirman, P.O. Box 223, JAKARTA, Tel. 716 131.
Ireland: PHILIPS ELECTRICAL (IRELAND) LTD., Newstead, Clonskeagh, DUBLIN 14, Tel. 69 33 55.
Italy: PHILIPS S.p.A., Sezione Elcoma, Piazza IV Novembre 3, I-20124 MILANO, Tel. 2-6752.1.
Japan: NIHON PHILIPS CORP., Shuwa Shinagawa Bldg., 26-33 Takanawa 3-chome, Minato-ku, TOKYO (108), Tel. 448-5611.
(IC Products) SIGNETICS JAPAN LTD., 8-7 Sanbancho Chiyoda-ku, TOKYO 102, Tel. (03)230-1521.
Korea: PHILIPS ELECTRONICS (KOREA) LTD., Elcoma Div., Philips House, 260-199 Itaewon-dong, Yongsan-ku, C.P.O. Box 3680, SEOUL, Tel. 794-4202.
Malaysia: PHILIPS MALAYSIA SDN. BERHAD, No. 4 Persiaran Barat, Petaling Jaya, P.O.B. 2163, KUALA LUMPUR, Selangor, Tel. 77 44 11.
Mexico: ELECTRONICA, S.A. de C.V., Carr. Mexico-Toluca km. 62.5, TOLUCA, Edo. de Mexico 50140, Tel. Toluca 91(721)613-00.
Netherlands: PHILIPS NEDERLAND, Marktgroep Elonco, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 79 33 33.
New Zealand: PHILIPS ELECTRICAL IND. LTD., Elcoma Division, 110 Mt. Eden Road, C.P.O. Box 1041, AUCKLAND, Tel. 605-914.
Norway: NORSK A/S PHILIPS, Electronica Dept., Sandstuveien 70, OSLO 6, Tel. 68 02 00.
Peru: CADESA, Av. Alfonso Ugarte 1268 , LIMA 5, Tel. 326070.
Philippines: PHILIPS INDUSTRIAL DEV. INC., 2246 Pasong Tamo, P.O. Box 911, Makati Comm. Centre, MAKATI-RIZAL 3116, Tel. 86-89-51 to 59.
Portugal: PHILIPS PORTUEGESA S.A.R.L., Av. Eng. Duarte Pacheco 6, LISBOA 1, Tel. 68 31 21.
Singapore: PHILIPS PROJECT DEV. (Singapore) PTE LTD., Elcoma Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 25 38 811.
South Africa: EDAC (Pty.) Ltd., 3rd Floor Rainer House, Upper Railway Rd. & Ove St., New Doornfontein, JOHANNESBURG 2001, Tel. 614-2362/9.
Spain: MINIWATT S.A., Balmes 22, BARCELONA 7, Tel. 301 63 12.
Sweden: PHILIPS KOMPONENTER A.B., Lidingövägen 50, S-11584 STOCKHOLM 27, Tel. 08/7821000.
Switzerland: PHILIPS A.G., Elcoma Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. 01-488 22 11.
Taiwan: PHILIPS TAIWAN LTD., 3rd Fl., San Min Building, 57-1, Chung Shan N. Rd, Section 2, P.O. Box 22978, TAIPEI, Tel. (02)-5631717.
Thailand: PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.O. Box 961, BANGKOK, Tel. 233-6330-9.
Turkey: TÜRK PHILIPS TICARET A.S., EMET Department, Inonu Cad. No. 78-80. ISTANBUL, Tel. 43 59 10.
United Kingdom: MULLARD LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. 01-580 6633.
United States: (Active Devices & Materials) AMPEREX SALES CORP., Providence Pike, SLATERSVILLE, R.I. 02876, Tel. (401) 762-9000.
(Passive Devices) MEPCO/ELECTRA INC., Columbia Rd., MORRISTOWN, N.J. 07960, Tel. (201)539-2000.
(Passive Devices & Electromechanical Devices) CENTRALAB INC., 5855 N. Glen Park Rd., MILWAUKEE, WI 53201, Tel. (414)228-7380.
(IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, California 94086, Tel. (408) 739-7700.
Uruguay: LUZILECTRON S.A., Avda Uruguay 1287, P.O. Box 907, MONTEVIDEO, Tel. 91 43 21.
Venezuela: IND. VENEZOLANAS PHILIPS S.A., Elcoma Dept., A. Ppal de los Ruices, Edif. Centro Colgate, CARACAS, Tel. 36 05 11.

For all other countries apply to: Philips Electronic Components and Materials Division, International Business Relations, Building BAE-3, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Tel. +31 40 72 33 04, Telex 35000 phtc nl/nl be vec.

A35

Printed in The Netherlands

9398 121 30011

INTEGRATED CIRCUITS

PART 2 – JANUARY 1984

BIPOLAR ICs FOR VIDEO EQUIPMENT

DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, subassemblies and materials; it is made up of four series of handbooks each comprising several parts.

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks is comprised of the following parts:

T1	**Tubes for r.f. heating**
T2a	**Transmitting tubes for communications, glass types**
T2b	**Transmitting tubes for communications, ceramic types**
T3	**Klystrons, travelling-wave tubes, microwave diodes**
ET3	**Special Quality tubes, miscellaneous devices** (will not be reprinted)
T4	**Magnetrons**
T5	**Cathode-ray tubes** Instrument tubes, monitor and display tubes, C.R. tubes for special applications
T6	**Geiger-Müller tubes**
T7	**Gas-filled tubes** Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories
T8	**Picture tubes and components** Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display
T9	**Photo and electron multipliers** Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates
T10	**Camera tubes and accessories, image intensifiers**
T11	**Microwave semiconductors and components**

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks is comprised of the following parts:

S1 **Diodes**
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes(< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2 **Power diodes, thyristors, triacs**
Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Microminiature semiconductors for hybrid circuits**

S8 **Devices for optoelectronics**
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks is comprised of the following parts:

IC1	**Bipolar ICs for radio and audio equipment**
IC2	**Bipolar ICs for video equipment**
IC3	**ICs for digital systems in radio, audio and video equipment**
IC4	**Digital integrated circuits** CMOS HE4000B family
IC5	**Digital integrated circuits – ECL** ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs
IC6	**Professional analogue integrated circuits**
IC7	**Signetics bipolar memories**
IC8	**Signetics analogue circuits**
IC9	**Signetics TTL logic**
IC10	**Signetics Integrated Fuse Logic (IFL)**
IC11	**Microprocessors, microcomputers and peripheral circuitry**

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks is comprised of the following parts:

C1	**Assemblies for industrial use** PLC modules, PC20 modules, HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs
C2	**Television tuners, video modulators, surface acoustic wave filters**
C3	**Loudspeakers**
C4	**Ferroxcube potcores, square cores and cross cores**
C5	**Ferroxcube for power, audio/video and accelerators**
C6	**Electric motors and accessories** Permanent magnet synchronous motors, stepping motors, direct current motors
C7	**Variable capacitors**
C8	**Variable mains transformers**
C9	**Piezoelectric quartz devices** Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements
C10	**Connectors**
C11	**Non-linear resistors** Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
C12	**Variable resistors and test switches**
C13	**Fixed resistors**
C14	**Electrolytic and solid capacitors**
C15	**Film capacitors, ceramic capacitors**
C16	**Piezoelectric ceramics, permanent magnet materials**

FUNCTIONAL AND NUMERICAL INDEX
MAINTENANCE TYPE LIST

SELECTION GUIDE BY FUNCTION

type number	description	package code	pins
Vision i.f. circuits			
Economical circuits			
TDA2540	i.f. amplifier and demodulator; n-p-n tuners	SOT-38	16
TDA2540Q	i.f. amplifier and demodulator; n-p-n tuners	SOT-58	16
TDA2541	i.f. amplifier and demodulator; p-n-p tuners	SOT-38	16
TDA2541Q	i.f. amplifier and demodulator; p-n-p tuners	SOT-58	16
TDA2542	i.f. amplifier and demodulator; for E and L standards; p-n-p tuners	SOT-38	16
TDA2542Q	i.f. amplifier and demodulator; for E and L standards; p-n-p tuners	SOT-58	16
TDA2544	i.f. amplifier and demodulator; MOS tuners	SOT-38	16
TDA2544Q	i.f. amplifier and demodulator; MOS tuners	SOT-58	16
TDA2548	i.f. amplifier and demodulator; p-n-p tuners	SOT-38	16
TDA2548Q	i.f. amplifier and demodulator; p-n-p tuners	SOT-58	16
TDA2549	i.f. amplifier and demodulator; for multistandard TV receivers	SOT-101A	24
High-performance circuits			
TDA3540	i.f. amplifier and demodulator; n-p-n tuners	SOT-38	16
TDA3540Q	i.f. amplifier and demodulator; n-p-n tuners	SOT-58	16
TDA3541	i.f. amplifier and demodulator; p-n-p tuners	SOT-38	16
TDA3541Q	i.f. amplifier and demodulator; p-n-p tuners	SOT-58	16
Colour decoding circuits			
TBA540	reference combination	SOT-38	16
TBA540Q	reference combination	SOT-58	16
TCA640	chrominance amplifier for SECAM or PAL/SECAM decoders	SOT-38	16
TCA650	chrominance demodulator for SECAM or PAL/SECAM decoders	SOT-38	16
TCA660B	contrast, saturation and brightness control circuit for colour difference and luminance signals	SOT-38	16
TDA3500	video control combination	SOT-117	28
TDA3501	video control combination	SOT-117	28
TDA3505	video control combination with automatic cut-off control	SOT-117	28
TDA3510	PAL decoder	SOT-101A	24
TDA3560	PAL decoder	SOT-117	28

SELECTION GUIDE BY FUNCTION (continued)

type number	description	package code	pins
Colour decoding circuits (continued)			
TDA3561A	PAL decoder	SOT-117	28
TDA3562A	PAL/NTSC decoder	SOT-117	28
TDA3563	NTSC decoder	SOT-117	28
TDA3564	NTSC decoder	SOT-101A, B	24
TDA3570	NTSC decoder	–	28
TDA3590	SECAM processor circuit	SOT-101B	24
TDA3590A	SECAM processor circuit (improved TDA3590)	SOT-101B	24
TDA3591	SECAM processor circuit	SOT-101B	24
TDA4510	PAL decoder	SOT-38	16
TDA4530	SECAM decoder	SOT-102A	18
TDA4550	multistandard decoder	SOT-117	28
TDA4560	colour transient improvement circuit	SOT-102CS	18
Vertical deflection circuits			
TDA2653A	vertical deflection circuit; PIL-S4; 30AX	SOT-141B	13
TDA2654	vertical deflection circuit; monochrome, 110°; tiny-vision colour, 90°	SOT-110B	9
TDA2655B	vertical deflection circuit; colour and monochrome, 90°	SOT-150	12
TDA3650	vertical deflection circuit	SOT-141B	13
TDA3651	vertical delfection circuit	SOT-110B	9
TDA3651A	vertical deflection circuit	SOT-131B	9
TDA3651AQ	vertical deflection circuit	SOT-157B	9
TDA3652	vertical deflection circuit	SOT-131B	9
TDA3652Q	vertical deflection circuit	SOT-157B	9
TDA3653	vertical deflection circuit	SOT-110B	9
TDA3653A	vertical deflection circuit	SOT-131B	9

type number	description	package code	pins
Sync processors; horizontal; vertical			
TBA720A	horizontal oscillator circuit	SOT-38	16
TBA720AQ	horizontal oscillator circuit	SOT-58	16
TBA890	signal processing circuit	SOT-38	16
TBA890Q	signal processing circuit	SOT-58	16
TDA2571A	horizontal synchronization and vertical 625 divider system	SOT-38	16
TDA2571AQ	horizontal synchronization and vertical 625 divider system	SOT-58	16
TDA2575A	horizontal synchronization and vertical 625 divider system	SOT-38	16
TDA2575AQ	horizontal synchronization and vertical 625 divider system	SOT-58	16
TDA2576A	horizontal oscillator combination with vertical 625 divider system	SOT-38	16
TDA2577A	synchronization circuit with vertical oscillator and driver stages	SOT-102HE	18
TDA2578A	synchronization circuit with vertical oscillator and driver stages	SOT-102HE	18
TDA2593	horizontal combination	SOT-38	16
TDA2594	horizontal combination with transmitter identification	SOT-102DS	18
TDA2595	horizontal combination with transmitter identification and protection circuits	SOT-102CS	18
TDA3571B	sync combination with transmitter identification and vertical 625 divider system	SOT-102A	18
TDA3576B	sync combination with transmitter identification and vertical 625 divider system	SOT-102HE	18
Sound circuits			
TBA120U	sound i.f. amplifier/demodulator for TV	SOT-27K,M,T	14
TBA750C	limiter/amplifier	SOT-38	16
TBA750CQ	limiter/amplifier	SOT-58	16
TDA1029	signal sources switch (4 x two channels)	SOT-38	16
TDA1512	12 to 20 W hi-fi audio power amplifier	SOT-131B	9
TDA1512Q	12 to 20 W hi-fi audio power amplifier	SOT-157B	9
TDA1520	20 W hi-fi audio power amplifier	SOT-131A	9
TDA1520Q	20 W hi-fi audio power amplifier	SOT-157A	9
TDA1520A	20 W hi-fi audio power amplifier	SOT-131A	9
TDA1520AQ	20 W hi-fi audio power amplifier	SOT-157A	9
TDA1524	stereo-tone/volume control circuit	SOT-102CS	18
TDA2543	AM sound i.f. circuit for French standard	SOT-102CS	18
TDA2545A	quasi-split-sound circuit	SOT-38	16
TDA2546A	quasi-split-sound circuit with 5,5 MHz demodulation	SOT-102CS	18
TDA2611A	5 W audio power amplifier	SOT-110B	9

SELECTION GUIDE BY FUNCTION (continued)

type number	description	package code	pins
Sound circuits (continued)			
TDA2791	TV sound combination; volume, treble, bass	SOT-38	16
TDA2795	TV stereo/dual sound identification decoder	SOT-102DS	18
TDA3800S	stereo/dual TV sound processing circuit	SOT-117	28
TDA3800AS	stereo/dual TV sound processing circuit	SOT-117	28
TDA3800G	stereo/dual TV sound processing circuit	SOT-117	28
TDA3800GS	stereo/dual TV sound processing circuit	SOT-117	28
TDA3810	spatial, stereo and pseudo-stereo sound circuit	SOT-102CS	18
Video recorder circuits			
TDA2501	PAL-NTSC encoder	SOT-38WE-2	16
TDA2502	tacho motor speed controller	SOT-102HE	18
TDA2503	track sensing amplifier for video recorders	SOT-38WE-2	16
TDA2730	FM limiter/demodulator (video recorders)	SOT-38	16
TDA2740	amplifier and drop-out identification circuit (video recorders)	SOT-38	16
TDA3701	PAL synchronization processor for video recorders	SOT-117	28
TDA3710	chrominance signal/mixer (video recorders)	SOT-117	28
TDA3720	SECAM processor for video recorders	SOT-102HE	18
TDA3730	frequency demodulator and drop out compensator for video recorders	SOT-117	28
TDA3771	video processor (video recorders)	SOT-102CS	18
TDA3780	frequency modulator (video recorders)	SOT-102CS	18
TDA3791	band selector and window detector	SOT-38WE-2	16
TDA5010	VCR tape end detector	SOT-38	16
Miscellaneous			
SAA5030	videotex/video processor	SOT-101A	24
TDA0820T	double balanced modulator/demodulator	SOT-108A (SO-14)	14
TDA1082	east-west correction driver circuit	SOT-38	16
TDA2579	synchronization circuit with synchronized vertical divider system and output stages	SOT-102HE	18
TDA2581	control circuit for SMPS	SOT-38	16
TDA2581Q	control circuit for SMPS	SOT-58	16
TDA2582	control circuit for PPS	SOT-38	16
TDA2582Q	control circuit for PPS	SOT-58	16
TDA3047	infrared receiver	SOT-38	16
TDA3048	infrared receiver	SOT-38	16
TDA4500	small signal combination IC for monochrome TV	SOT-117	28
TDA5030	VHF mixer/oscillator circuit	SOT-102HE	18
TEA1002	PAL colour encoder and video summer	SOT-102CS	18

NUMERICAL INDEX

type number	description	package code	pins
SAA5030	videotex/video processor	SOT-101A	24
TBA120U	sound i.f. amplifier/demodulator for TV	SOT-27K,M,T	14
TBA540	reference combination	SOT-38	16
TBA540Q	referenec combination	SOT-58	16
TBA720A	horizontal oscillator circuit	SOT-38	16
TBA720AQ	horizontal oscillator circuit	SOT-58	16
TBA750C	limiter/amplifier	SOT-38	16
TBA750CQ	limiter/amplifier	SOT-58	16
TBA890	signal processing circuit	SOT-38	16
TBA890Q	signal processing circuit	SOT-58	16
TCA640	chrominance amplifier for SECAM or PAL/SECAM decoders	SOT-38	16
TCA650	chrominance demodulator for SECAM or PAL/SECAM decoders	SOT-38	16
TCA660B	contrast, saturation and brightness control circuit for colour difference and luminance signals	SOT-38	16
TDA0820T	double balanced modulator/demodulator	SOT-108A (SO-14)	14
TDA1029	signal sources switch (4 x two channels)	SOT-38	16
TDA1082	east-west correction driver circuit	SOT-38	16
TDA1512	12 to 20 W hi-fi audio power amplifier	SOT-131B	9
TDA1512Q	12 to 20 W hi-fi audio power amplifier	SOT-157B	9
TDA1520	20 W hi-fi audio power amplifier	SOT-131A	9
TDA1520Q	20 W hi-fi audio power amplifier	SOT-157A	9
TDA1520A	20 W hi-fi audio power amplifier	SOT-131A	9
TDA1520AQ	20 W hi-fi audio power amplifier	SOT-157A	9
TDA1524	stereo-tone volume control circuit	SOT-102CS	18
TDA2501	PAL/NTSC encoder	SOT-38WE-2	16
TDA2502	tacho motor speed controller	SOT-102HE	18
TDA2503	track sensing amplifier for video recorders	SOT-38WE-2	16
TDA2540	i.f. amplifier and demodulator; n-p-n tuners	SOT-38	16
TDA2540Q	i.f. amplifier and demodulator; n-p-n tuners	SOT-58	16
TDA2541	i.f. amplifier and demodulator; p-n-p tuners	SOT-38	16
TDA2541Q	i.f. amplifier and demodulator; p-n-p tuners	SOT-58	16
TDA2542	i.f. amplifier and demodulator; for E and L standards; p-n-p tuners	SOT-38	16
TDA2542Q	i.f. amplifier and demodulator; for E and L standards; p-n-p tuners	SOT-58	16
TDA2543	AM sound i.f. circuit for French standard	SOT-102CS	18
TDA2544	i.f. amplifier and demodulator; MOS tuners	SOT-38	16
TDA2544Q	i.f. amplifier and demodulator; MOS tuners	SOT-58	16

NUMERICAL INDEX (continued)

type number	description	package code	pins
TDA2545A	quasi-split-sound circuit	SOT-38	16
TDA2546A	quasi-split-sound circuit with 5,5 MHz demodulation	SOT-102CS	18
TDA2548	i.f. amplifier and demodulator; p-n-p tuners	SOT-38	16
TDA2548Q	i.f. amplifier and demodulator; p-n-p tuners	SOT-58	16
TDA2549	i.f. amplifier and demodulator; for multistandard TV receivers	SOT-101A	24
TDA2571A	horizontal synchronization and vertical 625 divider system	SOT-38	16
TDA2571AQ	horizontal synchronization and vertical 625 divider system	SOT-58	16
TDA2575A	horizontal synchronization and vertical 625 divider system	SOT-38	16
TDA2575AQ	horizontal synchronization and vertical 625 divider system	SOT-58	16
TDA2576A	horizontal oscillator combination with vertical 625 divider system	SOT-38	16
TDA2577A	synchronization circuit with vertical oscillator and driver stages	SOT-102HE	18
TDA2578A	synchronization circuit with vertical oscillator and driver stages	SOT-102HE	18
TDA2579	synchronization circuit with synchronized vertical divider system and output stages	SOT-102HE	18
TDA2581	control circuit for SMPS	SOT-38	16
TDA2581Q	control circuit for SMPS	SOT-58	16
TDA2582	control circuit for PPS	SOT-38	16
TDA2582Q	control circuit for PPS	SOT-58	16
TDA2593	horizontal combination	SOT-38	16
TDA2594	horizontal combination with transmitter identification	SOT-102DS	18
TDA2595	horizontal combination with transmitter identification and protection circuits	SOT-102CS	18
TDA2611A	5 W audio power amplifier	SOT-110B	9
TDA2653A	vertical deflection circuit; PIL-S4; 30 AX	SOT-141B	13
TDA2654	vertical deflection circuit; monochrome, 110°; tiny-vision colour, 90°	SOT-110B	9
TDA2655B	vertical deflection circuit; colour and monochrome, 90°	SOT-150	12
TDA2730	FM limiter/demodulator (video recorders)	SOT-38	16
TDA2740	amplifier and drop-out identification circuit (video recorders)	SOT-38	16
TDA2791	TV sound combination; volume, treble, bass	SOT-38	16
TDA2795	TV stereo/dual sound identification decoder	SOT-102DS	18
TDA3047	infrared receiver	SOT-38	16
TDA3048	infrared receiver	SOT-38	16

type number	description	package code	pins
TDA3500	video control combination	SOT-117	28
TDA3501	video control combination	SOT-117	28
TDA3505	video control combination with automatic cut-off control	SOT-117	28
TDA3510	PAL decoder	SOT-101A	24
TDA3540	i.f. amplifier and demodulator; n-p-n tuners	SOT-38	16
TDA3540Q	i.f. amplifier and demodulator; n-p-n tuners	SOT-58	16
TDA3541	i.f. amplifier and demodulator; p-n-p tuners	SOT-38	16
TDA3541Q	i.f. amplifier and demodulator; p-n-p tuners	SOT-58	16
TDA3560	PAL decoder	SOT-117	28
TDA3561A	PAL decoder	SOT-117	28
TDA3562A	PAL/NTSC decoder	SOT-117	28
TDA3563	NTSCdecoder	SOT-117	28
TDA3564	NTSC decoder	SOT-101A,B	24
TDA3570	NTSC decoder	—	28
TDA3571B	sync combination with transmitter identification and vertical 625 divider system	SOT-102A	18
TDA3576B	sync combination with transmitter identification and vertical 625 divider system	SOT-102HE	18
TDA3590	SECAM processor circuit	SOT-101B	24
TDA3590A	SECAM processor circuit (improved TDA3590)	SOT-101B	24
TDA3591	SECAM processor circuit	SOT-101B	24
TDA3650	vertical deflection circuit	SOT-141B	13
TDA3651	vertical deflection circuit	SOT-110B	9
TDA3651A	vertical deflection circuit	SOT-131B	9
TDA3651AQ	vertical deflection circuit	SOT-157B	9
TDA3652	vertical deflection circuit	SOT-131B	9
TDA3652Q	vertical deflection circuit	SOT-157B	9
TDA3653	vertical deflection circuit	SOT-110B	9
TDA3653A	vertical deflection circuit	SOT-131B	9
TDA3701	PAL synchronization processor for video recorders	SOT-117	28
TDA3710	chrominance signal/mixer (video recorders)	SOT-117	28
TDA3720	SECAM processor for video recorders	SOT-102HE	18

NUMERICAL INDEX (continued)

type number	description	package code	pins
TDA3730	frequency demodulator and drop out compensator for video recorders	SOT-117	28
TDA3771	video processor (video recorders)	SOT-102CS	18
TDA3780	frequency modulator (video recorders)	SOT-102CS	18
TDA3791	band selector and window detector	SOT-38WE-2	16
TDA3800G	stereo/dual TV sound processing circuit	SOT-117	28
TDA3800GS	stereo/dual TV sound processing circuit	SOT-117	28
TDA3800S	stereo/dual TV sound processing circuit	SOT-117	28
TDA3800AS	stereo/dual TV sound processing circuit	SOT-117	28
TDA3810	spatial, stereo and pseudo-stereo sound circuit	SOT-102CS	18
TDA4500	small signal combination IC for monochrome TV	SOT-117	28
TDA4510	PAL decoder	SOT-38	16
TDA4530	SECAM decoder	SOT-102A	18
TDA4550	multistandard decoder	SOT-117	28
TDA4560	colour transient improvement circuit	SOT-102CS	18
TDA5010	VCR tape end detector	SOT-38	16
TDA5030	VHF mixer/oscillator circuit	SOT-102HE	18
TEA1002	PAL colour encoder and video summer	SOT-102CS	18

MAINTENANCE TYPE LIST

TBA920	horizontal combination
TBA920Q	horizontal combination
TBA920S	horizontal combination
TDA1028	signal sources switch (2 x four channels)
TDA2510	chrominance combination
TDA2510Q	chrominance combination
TDA2520	colour demodulator combination
TDA2520Q	colour demodulator combination
TDA2522	colour demodulator combination
TDA2522Q	colour demodulator combination
TDA2523	colour demodulator combination
TDA2523Q	colour demodulator combination
TDA2524	colour demodulator combination
TDA2525	colour demodulator combination
TDA2530	RGB matrix preamplifier
TDA2530Q	RGB matrix preamplifier
TDA2532	RGB matrix preamplifier
TDA2532Q	RGB matrix preamplifier
TDA2545	quasi-split-sound circuit (successor type: TDA2545A)
TDA2546	quasi-split-sound circuit with 5,5 MHz demodulation (successor type TDA2546A)
TDA2560	luminance and chrominance control combination
TDA2560Q	luminance and chrominance control combination
TDA2640	SMPS drive circuit
TDA2640Q	SMPS drive circuit
TDA2652	vertical deflection circuit: 20AX; 30AX
TDA2653	vertical deflection circuit; PIL-S4; 30AX
TDA2655A	vertical deflection circuit; colour, 90°
TDA2721	colour sub-carrier oscillator and mixer (video recorders)
TDA3520	SECAM decoder
TDA3700A	PAL synchronization processor (video recorders)
TDA3800	stereo/dual TV sound processing circuit (successor type: TDA3800G)

GENERAL

Type designation
Rating systems

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : $\left\{\begin{array}{l}\text{Microcomputer}\\\text{Central processing unit}\end{array}\right.$
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : –55 to + 125 °C
D : –25 to + 70 °C
E : –25 to + 85 °C
F : –40 to + 85 °C
G : –55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

PACKAGE OUTLINES

PACKAGE OUTLINES

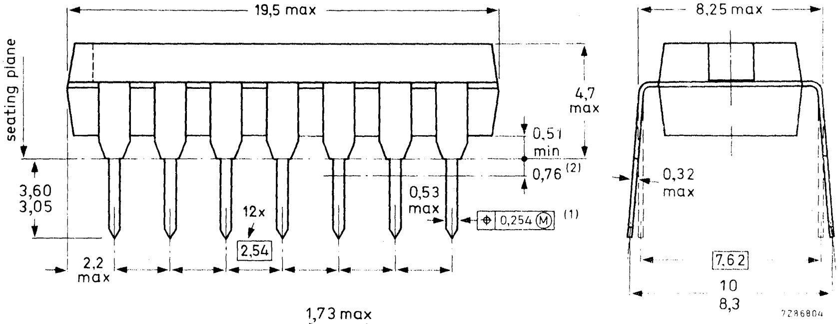
In this chapter the package outlines are given for the following types, except for those marked with an asterisk which are included in the device data sheet.

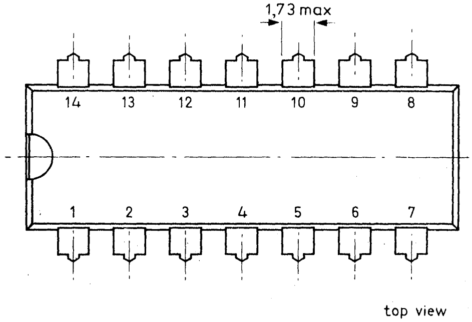
type number	package code	description
SAA5030	SOT-101A	24-lead dual in-line; plastic with internal heat spreader (SOT-101A, B)
TBA120U	SOT-27K,M,T	14-lead dual in-line; plastic (SOT-27K,M,T)
TBA540	SOT-38	16-lead dual in-line; plastic (SOT-38)
TBA540Q	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TBA720A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TBA720AQ	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TBA750C	SOT-38	16-lead dual in-line; plastic (SOT-38)
TBA720CQ	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TBA890	SOT-38	16-lead dual in-line; plastic (SOT-38)
TBA890Q	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TCA640	SOT-38	16-lead dual in-line; plastic (SOT-38)
TCA650	SOT-38	16-lead dual in-line; plastic (SOT-38)
TCA660B	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA0820T	SOT-108A	14-lead mini-pack; plastic (SO-14; SOT-108A)
TDA1029	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1082	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1512	SOT-131B	9-lead single in-line; plastic power (SOT-131A, B)
TDA1512Q	SOT-157B	9-lead SIL-bent-to-DIL; plastic power (SOT-157A, B)
TDA1520	SOT-131A	9-lead single in-line; plastic power (SOT-131A, B)
TDA1520Q	SOT-157A	9-lead single in-line; plastic power (SOT-157A, B)
TDA1520A	SOT-131A	9-lead single in-line; plastic power (SOT-131A, B)
TDA1520AQ	SOT-157A	9-lead single in-line; plastic power (SOT-157A, B)
TDA1524	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)
TDA2501	SOT-38WE-2	16-lead dual in-line; plastic with internal heat spreader (SOT-38WE-2)
TDA2502	SOT-102HE	18-lead dual in-line; plastic (SOT-102HE)
TDA2503	SOT-38WE-2	16-lead dual in-line; plastic with internal heat spreader (SOT-38WE-2)
TDA2540	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2540Q	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TDA2541	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2541Q	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TDA2542	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2542Q	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TDA2543	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)
TDA2544	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2544Q	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TDA2545A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2546A	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)
TDA2548	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2548Q	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TDA2549	SOT-101A	24-lead dual in-line; plastic (SOT-101A)

type number	package code	description
TDA2571A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2571AQ	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TDA2575A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2575AQ	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TDA2576A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2577A	SOT-102HE	18-lead dual in-line; plastic (SOT-102HE)
TDA2578A	SOT-102HE	18-lead dual in-line; plastic (SOT-102HE)
TDA2579	SOT-102HE	18-lead dual in-line; plastic (SOT-102HE)
TDA2581	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2581Q	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TDA2582	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2582Q	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TDA2593	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2594	SOT-102DS	18-lead dual in-line; plastic (SOT-102DS)
TDA2595	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)
TDA2611A	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TDA2653A	SOT-141B	13-lead SIL-bent-to-DIL; plastic power (SOT-141B)
TDA2654	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TDA2655B	SOT-150	12-lead dual in-line; plastic with metal cooling fin (SOT-150)
TDA2730	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2740	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2791	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA2795	SOT-102DS	18-lead dual in-line; plastic (SOT-102DS)
TDA3047	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA3048	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA3500	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3501	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3505	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3510	SOT-101A	24-lead dual in-line; plastic (SOT-101A)
TDA3540	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA3540Q	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TDA3541	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA3541Q	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TDA3560	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3561A	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3562A	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3563	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3564	SOT-101A, B	24-lead dual in-line; plastic with internal heat spreader (SOT-102A, B)
TDA3570*	—	28-lead dual in-line; plastic (SOT-117)
TDA3571B	SOT-102A	18-lead dual in-line; plastic (SOT-102A

type number	package code	description
TDA3576B	SOT-102HE	18-lead dual in-line; plastic (SOT-102HE)
TDA3590	SOT-101B	24-lead dual in-line; plastic with internal heat spreader (SOT-101A, B)
TDA3590A	SOT-101B	24-lead dual in-line; plastic with internal heat spreader (SOT-101A, B)
TDA3591	SOT-101B	24-lead dual in-line; plastic with internal heat spreader (SOT-101A, B)
TDA3650	SOT-141B	13-lead SIL-bent-to-DIL; plastic power (SOT-141B)
TDA3651	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TDA3651A	SOT-131B	9-lead single in-line; plastic power (SOT-131A, B)
TDA3651AQ	SOT-157B	9-lead SIL-bent-to-DIL; plastic power (SOT-157B)
TDA3652	SOT-131B	9-lead single in-line; plastic power (SOT-131A, B)
TDA3652Q	SOT-157B	9-lead SIL-bent-to-DIL; plastic power (SOT-157B)
TDA3653	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TDA3653A	SOT-131B	9-lead single in-line; plastic power (SOT-131A, B)
TDA3701	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3710	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3720	SOT-102HE	18-lead dual in-line; plastic (SOT-102HE)
TDA3730	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3771	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)
TDA3780	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)
TDA3791	SOT-38WE-2	16-lead dual in-line; plastic with internal heat spreader (SOT-38WE-2)
TDA3800G	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3800GS	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3800S	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3800AS	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA3810	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)
TDA4500	SOT-117	28-lead dual in-line; plastic with internal heat spreader (SOT-117)
TDA4510	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA4530	SOT-102A	18-lead dual in-line; plastic (SOT-102A)
TDA4550	SOT-117	28-lead dual in-line; plastic (SOT-117)
TDA4560	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)
TDA5010	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA5030	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)
TEA1002	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27K,M,T)





⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

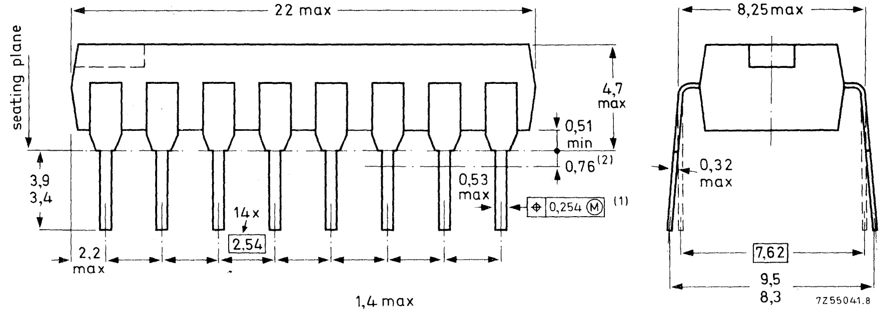
2. By dip or wave

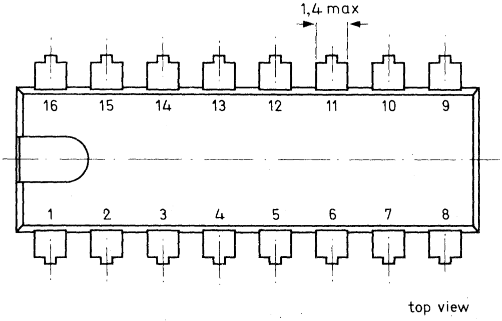
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)





⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

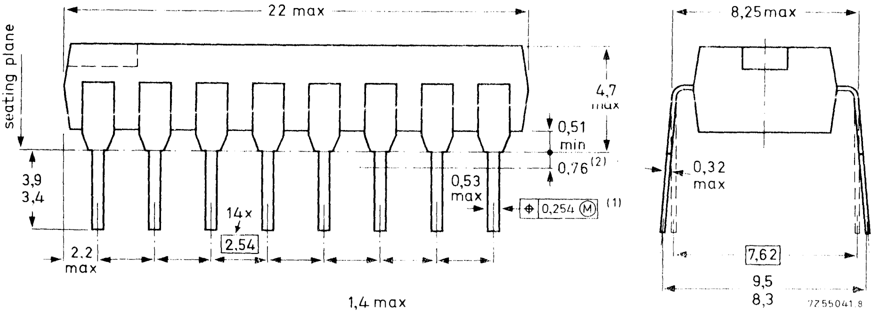
2. By dip or wave

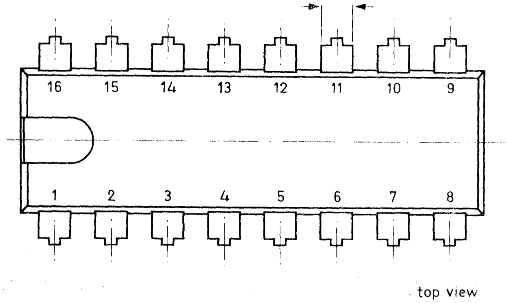
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT-38WE-2)





⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

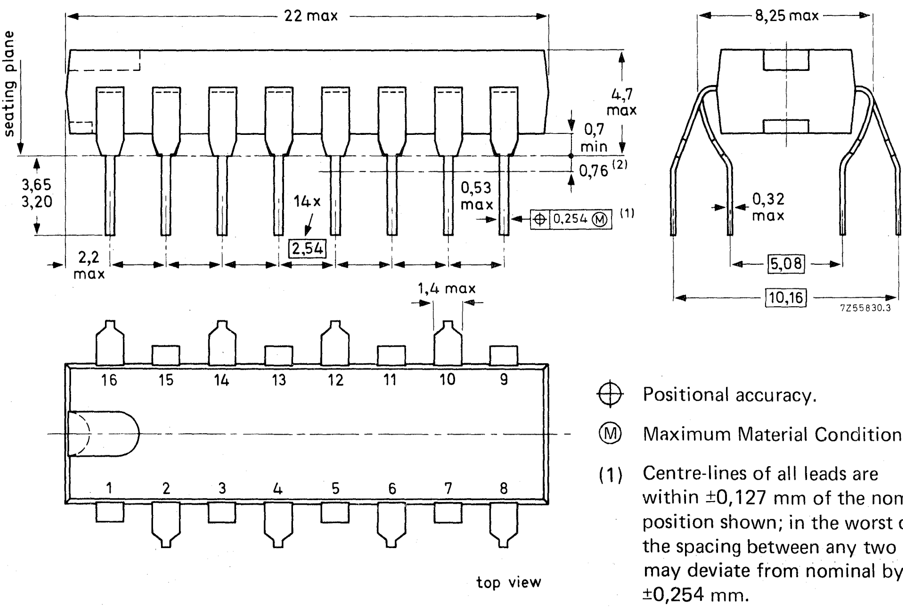
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD QUADRUPLE IN-LINE; PLASTIC (SOT-58)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

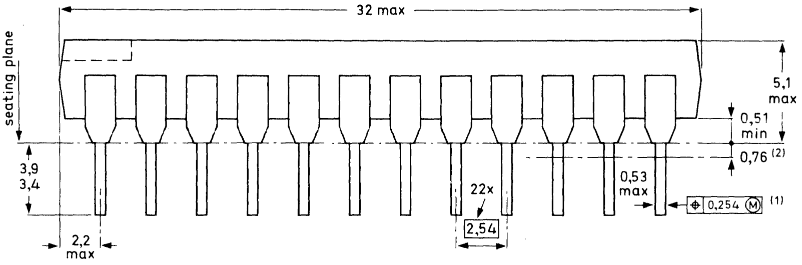
2. By dip or wave

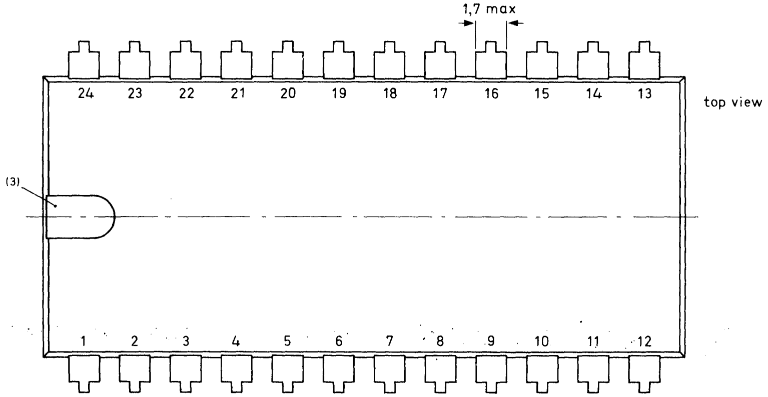
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

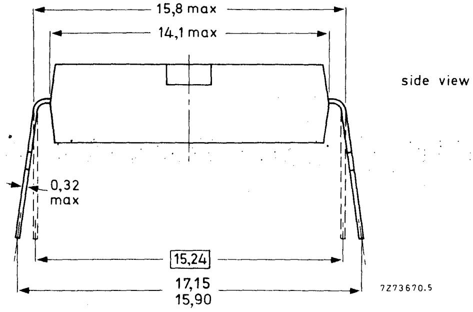
3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)







⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

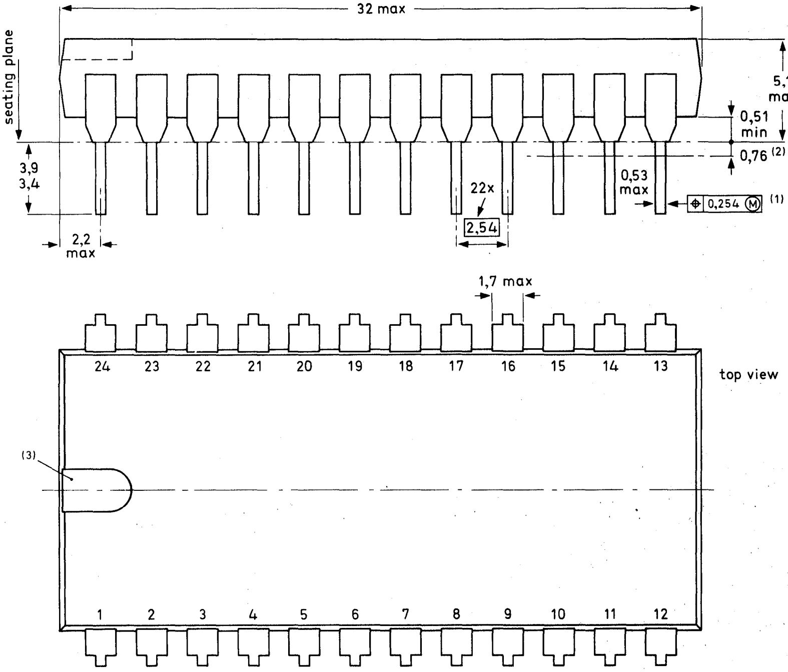
(3) Index may be horizontal as shown, or vertical.

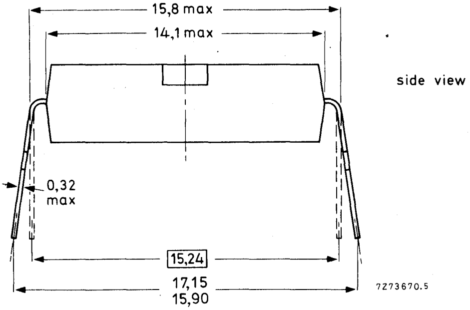
Dimensions in mm

SOLDERING

See page 23 of this chapter (SOT-27K,M,T).

24-LEAD DUAL IN-LINE; PLASTIC (WITH INTERNAL HEAT SPREADER) (SOT-101A, B)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

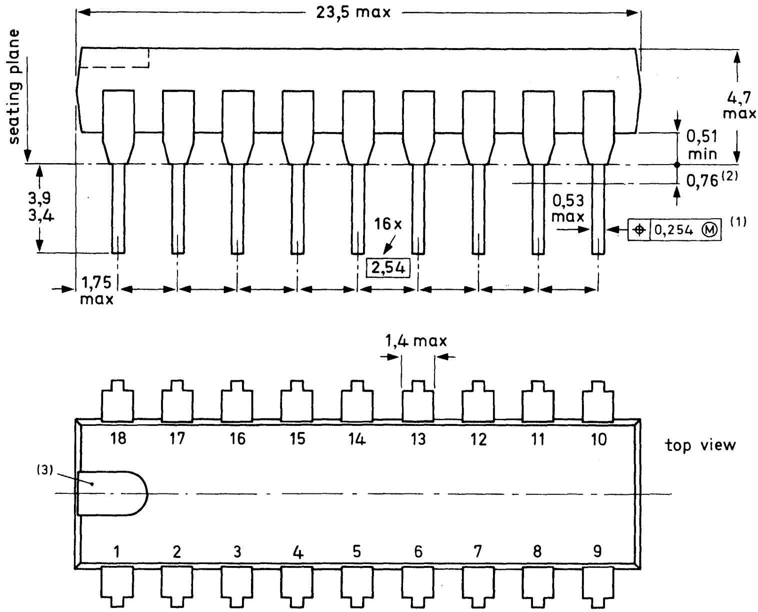
(3) Index may be horizontal as shown, or vertical.

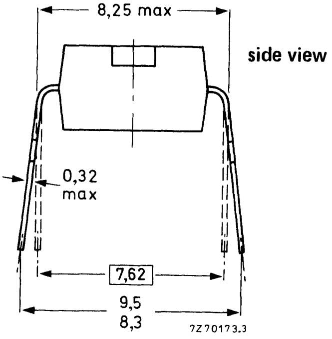
Dimensions in mm

SOLDERING

See page 23 of this chapter (SOT-27K,M,T).

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

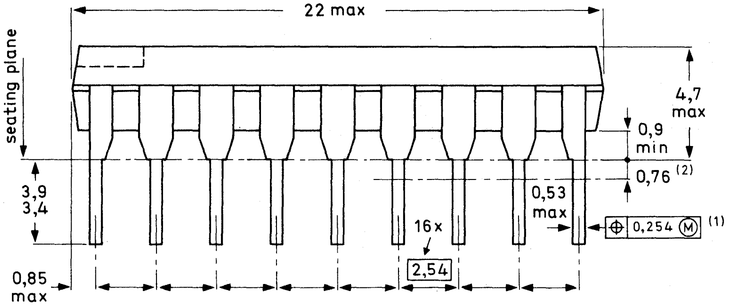
(3) Index may be horizontal as shown, or vertical.

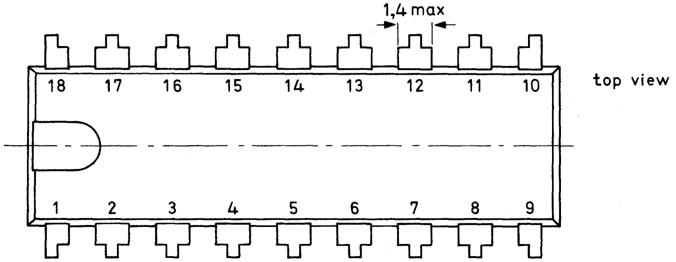
Dimensions in mm

SOLDERING

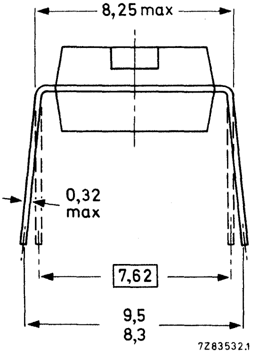
See page 23 of this chapter (SOT-27K,M,T).

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102CS)





top view



side view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

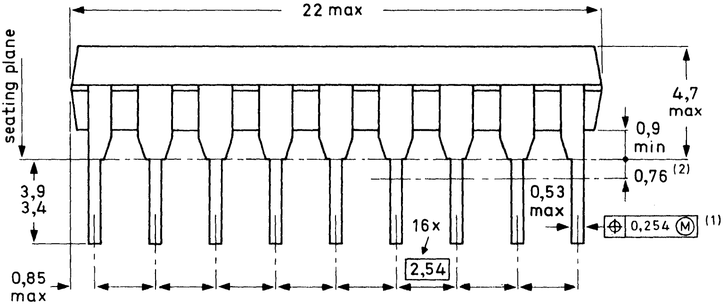
(2) Lead spacing tolerances apply from seating plane to the line indicated.

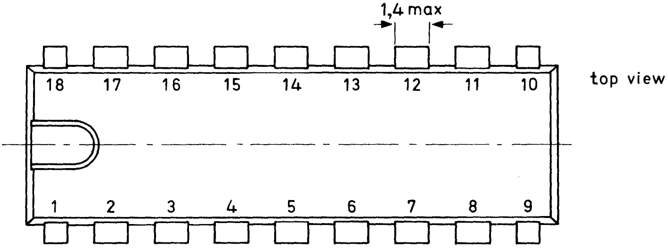
Dimensions in mm

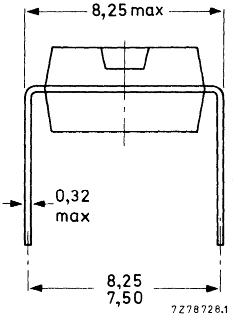
SOLDERING

See page 23 of this chapter (SOT-27K,M,T).

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102DS)







side view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

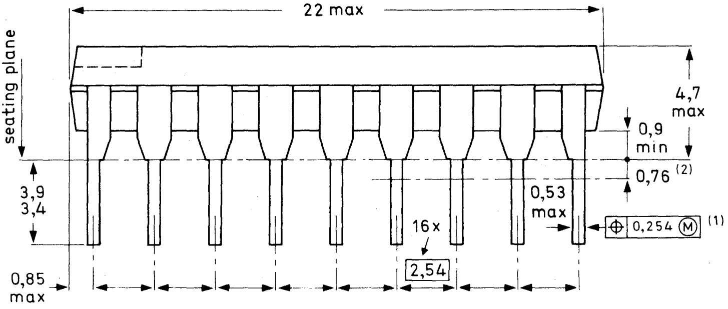
(2) Lead spacing tolerances apply from seating plane to the line indicated.

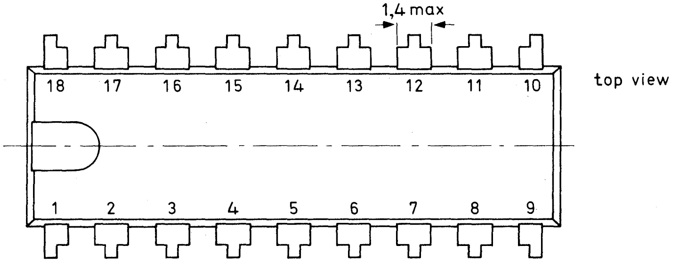
Dimensions in mm

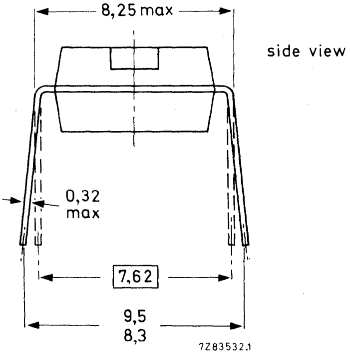
SOLDERING

See page 23 of this chapter (SOT-27K,M,T).

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102HE)







⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

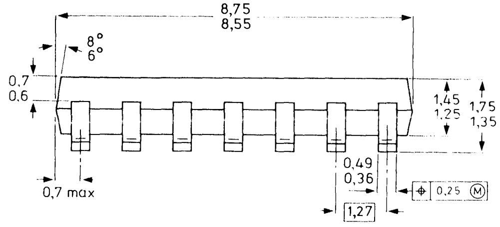
(2) Lead spacing tolerances apply from seating plane to the line indicated.

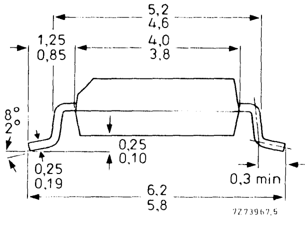
Dimensions in mm

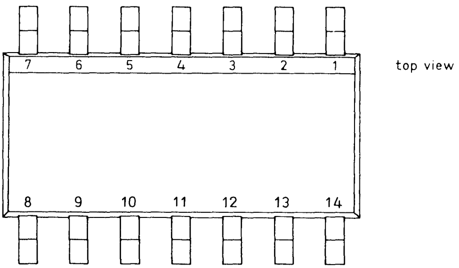
SOLDERING

See page 23 of this chapter (SOT-27K,M,T).

14-LEAD MINI-PACK; PLASTIC (SO-14; SOT-108A)







Dimensions in mm

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

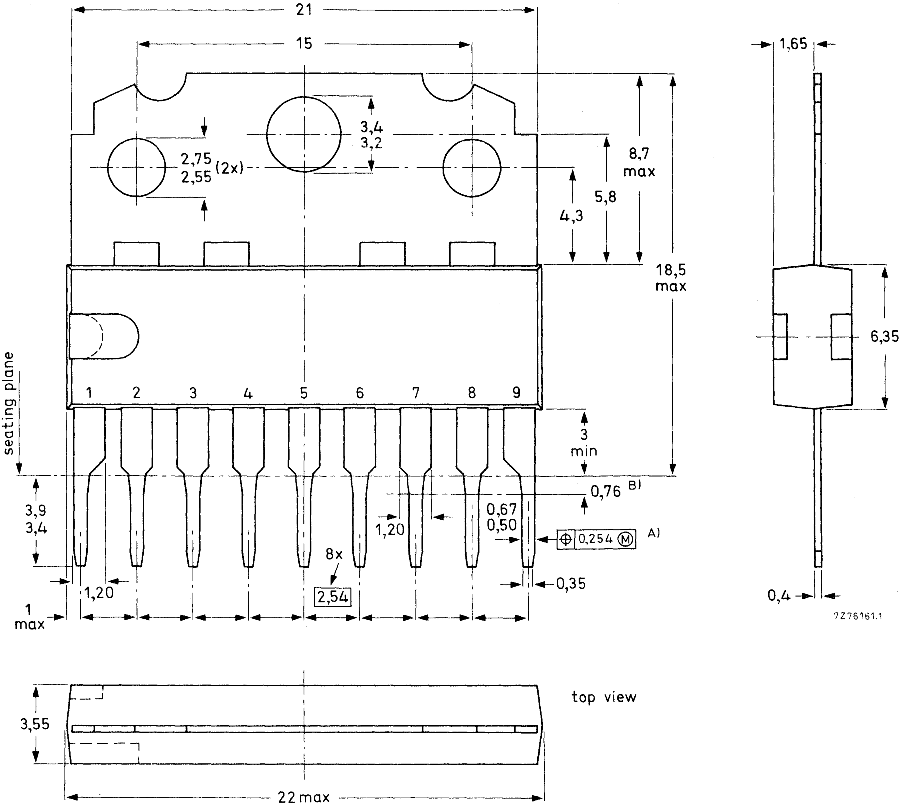
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110B)



Dimensions in mm

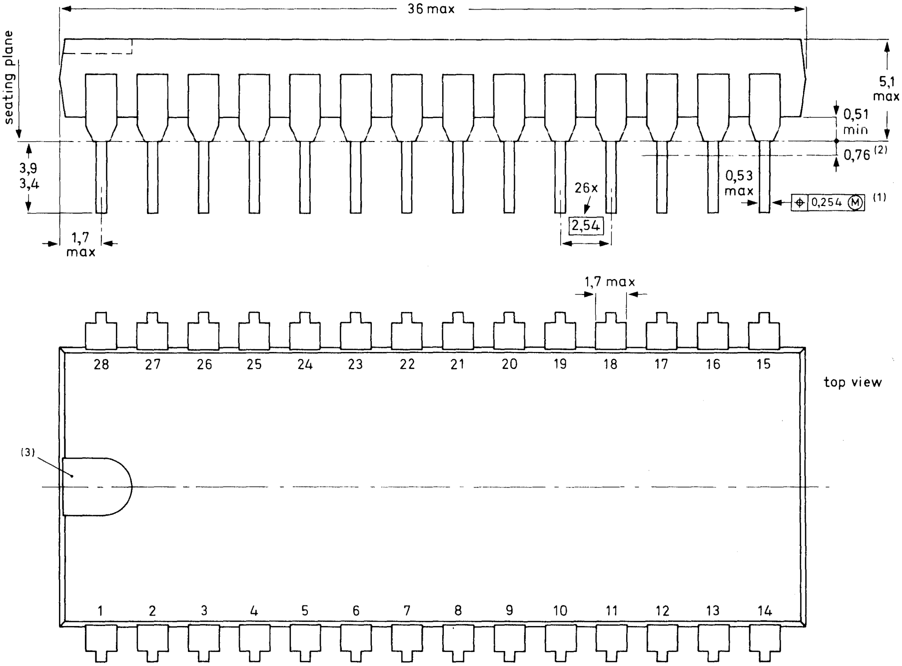
⊕ Positional accuracy.

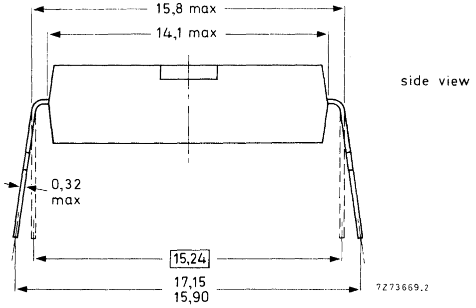
Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

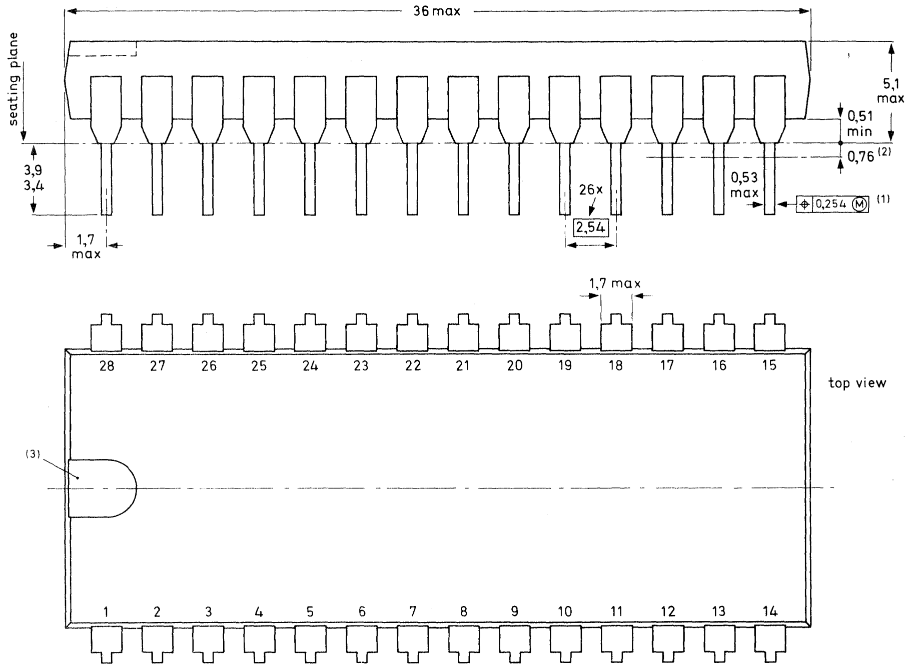
(3) Index may be horizontal as shown, or vertical.

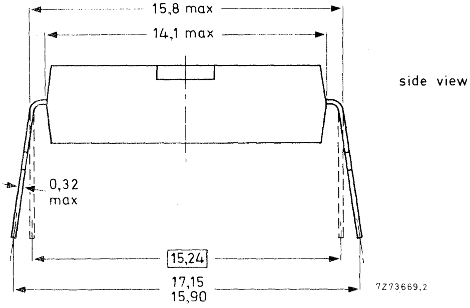
Dimensions in mm

SOLDERING

See page 23 of this chapter (SOT-27K,M,T).

28-LEAD DUAL IN-LINE; PLASTIC (WITH INTERNAL HEAT SPREADER) (SOT-117)





⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

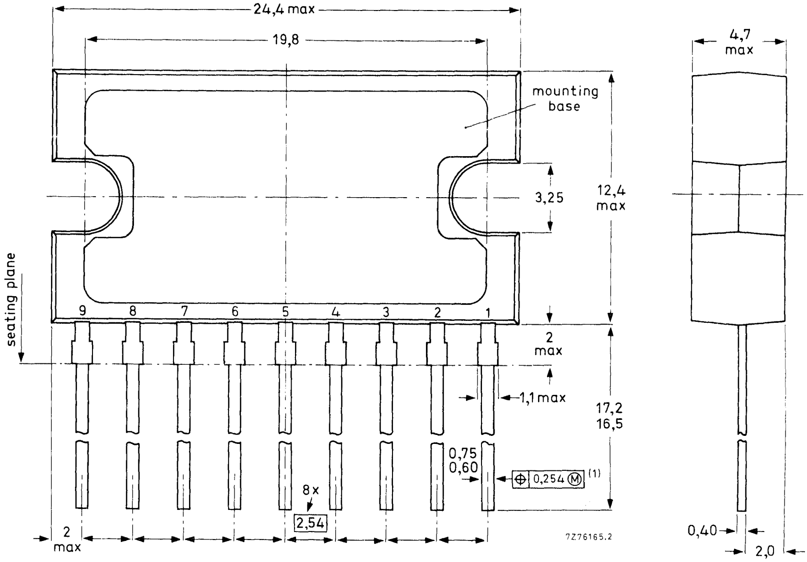
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See page 23 of this chapter (SOT-27K, M, T).

9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT-131A, B)



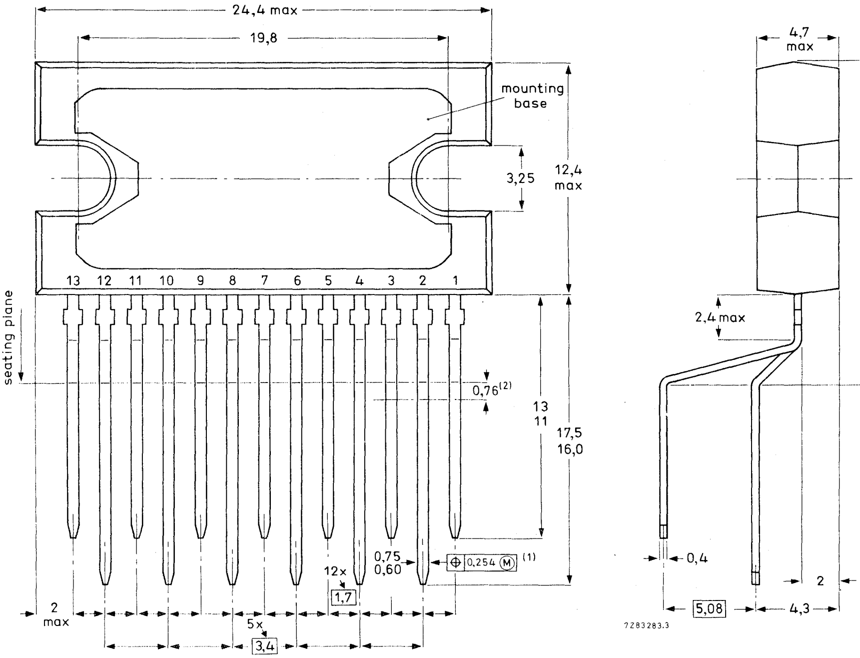
Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

13-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-141B)



Dimensions in mm

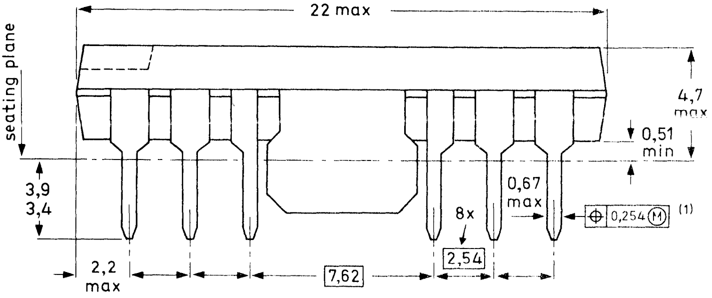
⌖ Positional accuracy.

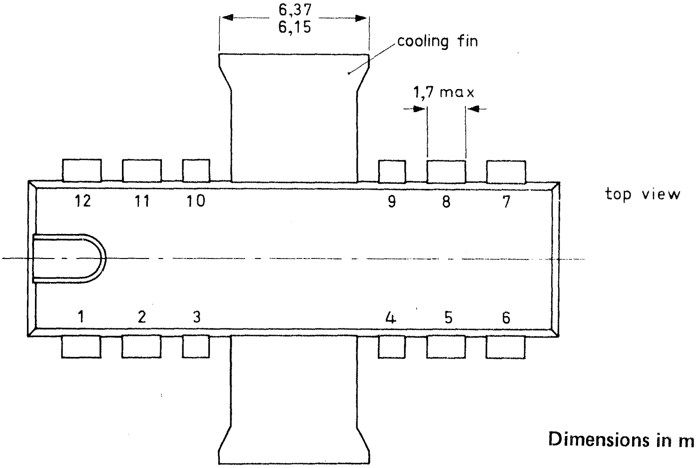
Ⓜ Maximum Material Condition.

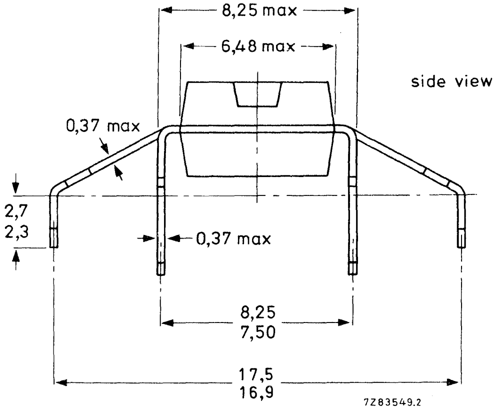
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

12-LEAD DUAL IN-LINE; PLASTIC WITH METAL COOLING FIN (SOT-150)







Dimensions in mm

⊕ Positional accuracy.

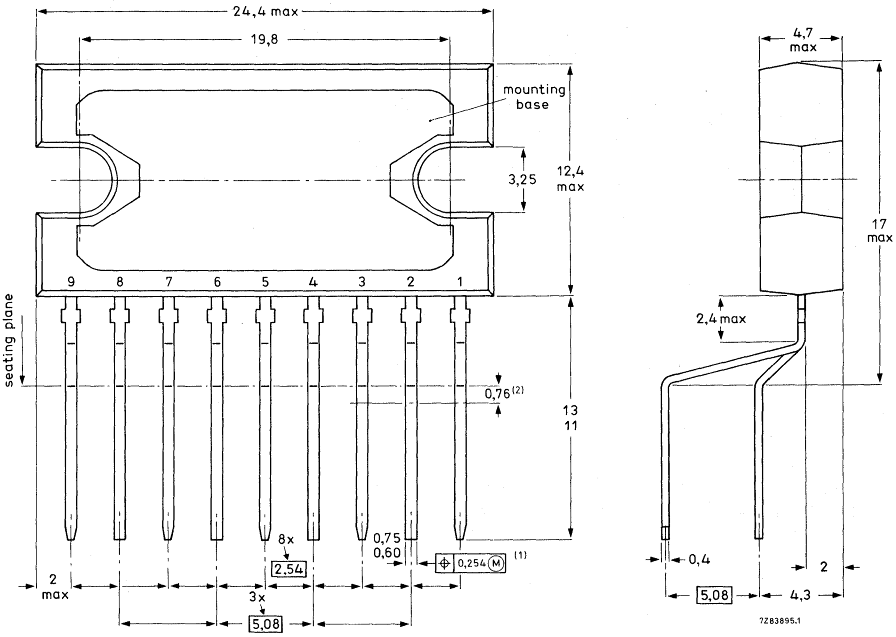
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

SOLDERING

See page 23 of this chapter (SOT-27K,M,T).

9-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-157A,B)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

DEVICE DATA

TELETEXT VIDEO PROCESSOR

The SAA5030 is a monolithic bipolar integrated circuit used for teletext video processing. It is one of a package of four circuits to be used in teletext tv data systems. The SAA5030 extracts data and data clock information from the television composite video signal and feeds this to the Acquisition and Control circuit SAA5040. A 6 MHz crystal controlled phase locked oscillator is incorporated which drives the Timing Chain circuit SAA5020. An adaptive sync separator is also provided which derives line and field sync pulses from the input video in order to synchronise the timing chain.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	12	V
Supply current (V_{CC} = 12 V)	I_{CC}	typ.	110	mA
Video input amplitude (sync-white)	$V_{16video(p-p)}$	nom.	2.4	V
Teletext data input amplitude	$V_{16teletext(p-p)}$	nom.	1.1	V
Sync amplitude	$V_{16sync(p-p)}$	nom.	0.7	V
Operating ambient temperature range	T_{amb}		−20 to +70	°C

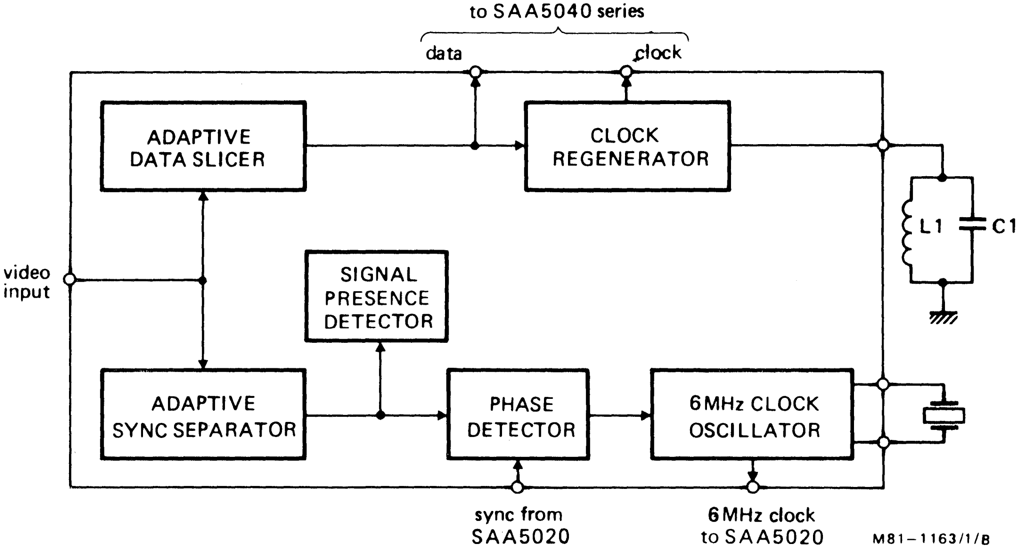


Fig.1 Block diagram

PACKAGE OUTLINE

24-lead DIL; plastic (SOT–101A with internal heat spreader).

PINNING

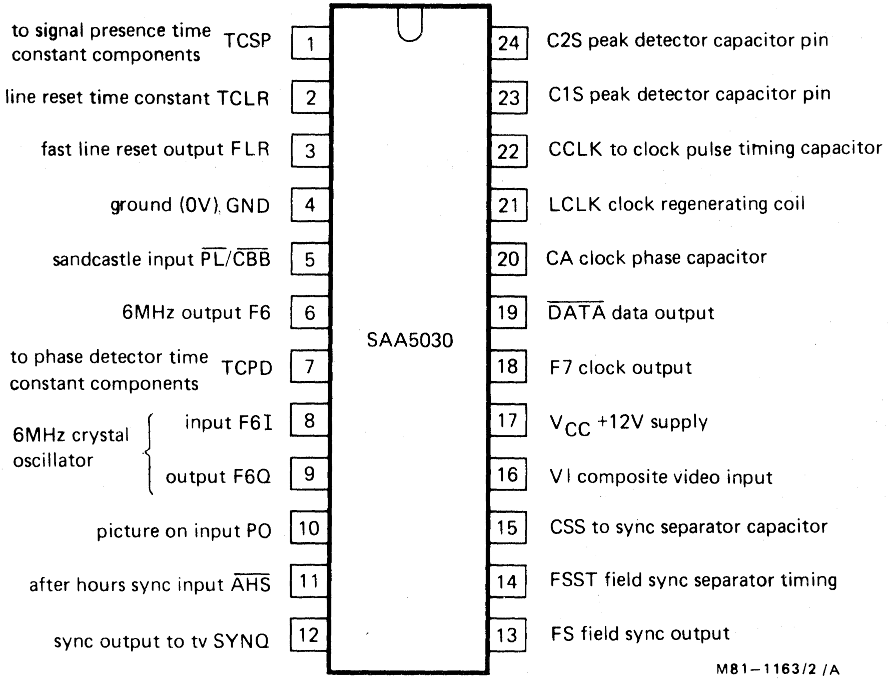


Fig.2 Pinning diagram

RATINGS Limiting values in accordance with the Absolute Maximum System. (IEC134)

Voltages

Supply voltage	$V_{17\text{-}4}$	V_{CC}	max.	13.2	V
Input voltages	$V_{5\text{-}4}$	V_I	max.	9.0	V
	$V_{10\text{-}4}$	V_I	max.	V_{CC}	V
	$V_{11\text{-}4}$	V_I	max.	7.5	V

Temperatures

Storage temperature range	T_{stg}	−20 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

CHARACTERISTICS (At T_{amb} = 25 °C, V_{CC} = 12 V and with external components as shown in Fig.3 unless otherwise stated).

		min.	typ.	max.	
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current (V_{CC} = 12.0 V)	I_{CC}	–	110	–	mA
Video input and sync separator					
Video input amplitude (sync to white) Fig.4	$V_{16video(p\text{-}p)}$	2.0	1.4	3.0	V
Source impedance, f = 100 kHz	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude	$V_{16sync(p\text{-}p)}$	0.07	0.7	1.0	V
Delay through sync separator	t_d	–	0.5	–	μs
Delay between field sync datum at pin 12 and the leading edge of separated field sync at pin 13 (Note 1, Fig.4)	t_d	32	48	62	μs
Field sync output					
V_O (LOW) (I_{13} = 20 μA)	V_{OL}	–	–	0.5	V
V_O (HIGH) ($-I_{13}$ = 100 μA)	V_{OH}	2.4	–	–	V

Crystal controlled phase-locked oscillator

Measured using a crystal with the following specification e.g. catalogue number 4322 143 03241

C_1 = 27.5 fF (typ.)
C_0 = 6.8 pF (typ.)
C_L = 20 pF

Trimability (C_L increased to 30 pF) > 750 Hz
Fundamental ESR < 50 Ω

		min.	typ.	max.	
Frequency	f_{F6}	–	6.0	–	MHz
Holding range		1.5	3.0	–	kHz
Catching range		1.5	3.0	–	kHz
Control sensitivity of phase detector measured as voltage at pin 7 with respect to phase difference between separated syncs and phase lock pulse $\overline{PL}$		–	0.3	–	mV/ns
Control sensitivity of oscillator measured as change in 6 MHz phase shift from pin 8 to pin 9 with respect to voltage at pin 7		–	2	–	deg/mV
Gain of sustaining amplifier, $V_{9\text{-}8}$ measured with input voltage of 100 $mV_{p\text{-}p}$ and phase detector immobilised		2.5	–	–	V/V
Output voltage of 6 MHz signal at pin 6, measured into 20 pF load capacitance; peak-to-peak value		–	5.5	–	V
Output rise and fall times at pin 6 into 20 pF load	t_r; t_f	–	–	30	ns

Data slicer and clock regenerator

		min.	typ.	max.	
Teletext data input amplitude, pin 16 (Note 2, Fig.4); peak-to-peak value		–	1.1	–	V
Data input amplitude at pin 16 required to enable amplitude gate flip-flop; peak-to-peak value		–	0.46	–	V
Attack rate, measured at pins 23 and 24 with a step to pin 16 (positive)		–	15	–	V/µs
(negative)		–	9	–	V/µs

		min.	typ.	max.	
Data slicer and clock regenerator (continued)					
Decay rate, measured at pins 23 and 24 with a step input to pin 16		48	100	144	mV/μs
Width of clock coil drive pulses from pin 21 when clock amplitude is not being controlled (Note 3)		–	40	–	ns
Clock hangover measured at pin 18 as the time the clock coil continues ringing after the end of data (Note 4)		20	–	–	Clock Periods
Clock and data output voltages at pins 18 and 19 measured with 20 pF load capacitance; peak-to-peak value		–	5.5	–	V
Output rise and fall times at pins 18 and 19 into 20 pF loads	t_r; t_f	–	–	30	ns
Sandcastle input					
Sandcastle detector thresholds, pin 5					
Phase lock pulse (PL) on		2	–	–	V
Phase lock pulse off		–	–	3	V
Blanking pulse ($\overline{\text{CBB}}$) on		4.5	–	–	V
Blanking pulse off		–	–	5.5	V
Dual polarity sync buffer					
After hours sync ($\overline{\text{AHS}}$) pulse input pin 11					
Threshold for $\overline{\text{AHS}}$ active		1.0	–	–	V
Threshold for $\overline{\text{AHS}}$ off		–	–	2.0	V
Picture On (PO) input, pin 10					
Threshold for PO active		–	–	2.0	V
Threshold for PO off		1.0	–	–	V
Sync output, pin 12					
$\overline{\text{AHS}}$ output with pin 10 < 1 V (Note 5) peak-to-peak value		–	0.7	–	V
Composite sync output with pin 10 > 2 V (Notes 5 and 6); peak-to-peak value		–	0.7	1.0	V
Output current		–	–	3	mA
Line reset and signal presence detectors					
Schmitt trigger threshold on pin 2 to inhibit line reset output at pin 3 (syncs coincident)		–	6.2	–	V
Schmitt trigger threshold on pin 2 to permit line reset output at pin 3 (syncs non-coincident)		–	7.8	–	V
Line reset output V_{OL} ($I_3 = 20\ \mu A$)		–	–	0.5	V
Line reset output V_{OH} ($-I_3 = 100\ \mu A$)		2.4	–	–	V
Signal presence Schmitt trigger threshold on pin 2 below which the circuit accepts the input signal		–	6.0	–	V
Signal presence Schmitt trigger threshold on pin 2 above which the input signal is rejected.		–	6.3	–	V

Notes

1. This is measured with the dual polarity buffer external resistor connected to give negative-going syncs. The measurement is made after adjustment of the potential divider at pin 14 for optimum delay.
2. The teletext data input contains binary elements as a two level NRZ signal shaped by a raised cosine filter. The bit rate is 6.9375 M bit/s. The use of odd parity for the 8-bit bytes ensures that there are never more than 14-bit periods between each data transition.
3. This is measured by replacing the clock coil with a small value resistor.
4. This must be measured with the clock coil tuned and using a clock-cracker signal into pin 16. The clock-cracker is a teletext waveform consisting of only one data transition in each byte.
5. With the external resistor connected to the ground rail, syncs are positive-going centred on +2.3 V. With the resistor connected to the supply rail, syncs are negative-going centred on +9.7 V.
6. When the composite sync is being delivered, the level is substantially the same as that at the video input.

APPLICATION DATA

The function is quoted against the corresponding pin number

Pin No.

1. **Signal presence time constant**

   A capacitor and a resistor connected in parallel between this pin and supply determine the delay in operation of the signal presence detector.

2. **Line reset time constant**

   A capacitor between this pin and supply integrates current pulses from the coincidence detector; the resultant level is used to determine whether to allow FLR pulses (see pin 3).

3. **Fast line reset output (FLR)**

   Positive-going sync pulses are produced at this output if the coincidence detector shows no coincidence between the syncs separated from the incoming video and the $\overline{\mathrm{CBB}}$ waveform from the timing chain circuit SAA5020. These pulses are sent to the timing chain circuit and are used to reset its counters, so as to effect rapid lock-up of the phase locked loop.

4. **Ground** (0 V)

5. **Sandcastle input ($\overline{\mathrm{PL}}$ and $\overline{\mathrm{CBB}}$)**

   This input accepts a sandcastle waveform which is formed from $\overline{\mathrm{PL}}$ and $\overline{\mathrm{CBB}}$ from the timing chain SAA5020. PL is obtained by slicing the waveform at 2.5 V, and this, together with separated sync, are inputs to the phase detector which forms part of the phase locked loop. When the loop has locked up, the edges of $\overline{\mathrm{PL}}$ are nominally 2 μs before and 2 μs after the leading edge of separated line syncs.
   CBB is obtained by slicing the waveform at 5 V, and is used to prevent the data slicer being offset by the colour burst.

6. **6 MHz output (F6)**

   This is the output of the crystal oscillator (see pins 8 and 9), and is taken to the timing chain circuit SAA5020 via a series capacitor.

7. **Phase detector time constant**

   The integrating components for the phase detector of the phase locked loop are connected between this pin and supply.

APPLICATION DATA (continued)

8, 9. **6 MHz crystal**

A 6 MHz crystal in series with a trimmer capacitor is connected between these pins. It forms part of an oscillator whose frequency is controlled by the voltage on pin 7, which forms part of the phase locked loop.

10\. **Picture On input (PO)**

The PO signal from the acquisition and control circuits SAA5040 Series is fed to this input and is used to determine whether the input video (pin 16) or the $\overline{\text{AHS}}$ waveform (pin 11) appears at pin 12.

11\. **After hours sync ($\overline{\text{AHS}}$)**

A composite sync waveform $\overline{\text{AHS}}$ is generated in the timing chain circuit SAA5020 and is used to synchronise the tv (see pin 10).

12\. **Sync output to tv**

Either the input video of $\overline{\text{AHS}}$ is available at this output dependent on whether the PO signal is HIGH or LOW. In addition either signal may be positive-going or negative-going, dependent on whether the load resistor at this output is connected to ground or supply.

13\. **Field sync output (FS)**

A pulse, derived from the input video by the field sync separator, which is used to reset the line counter in the timing chain circuit SAA5020.

14\. **Field sync separator timing**

A capacitor and adjusting network is connected to this pin and forms the integrator of the field sync separator.

15\. **Sync separator capacitor**

A capacitor connected to this pin forms part of the adaptive sync separator.

16\. **Composite video input (VI)**

The composite video is fed to this input via a coupling capacitor.

17\. **Supply voltage (+12 V)**

18\. **Clock output**

The regenerated clock, after extraction from the teletext data, is fed out to the acquisition and control circuits SAA5040 Series via a series capacitor.

19\. **Data output**

The teletext data is sliced off the video waveform, squared up and latched within the SAA5030. The latched output is fed to the acquisition and control circuits SAA5040 Series via a series capacitor.

20\. **Clock decoupling**

A 1 nF capacitor between pin 20 and ground is required for clock decoupling.

21\. **Clock regenerator coil**

A high-Q parallel tuned circuit is connected between this pin and an external potential divider. The coil is part of the clock regeneration circuit (see pin 22).

APPLICATION DATA (continued)

22. **Clock pulse timing capacitor**

Short pulses are derived from both edges of data with the aid of a capacitor connected to this pin. The resulting pulses are fed, as a current, into the clock coil connected to pin 21. Resulting oscillations are limited and taken to the acquisition and control circuits SAA5040 Series via pin 18.

23, 24 **Peak detector capacitors**

The teletext data is sliced with an automatic data slicer whose slicing level is the mid-point of two peak detectors working on the video signal. Storage capacitors are connected to these pins for the negative and positive peak detectors.

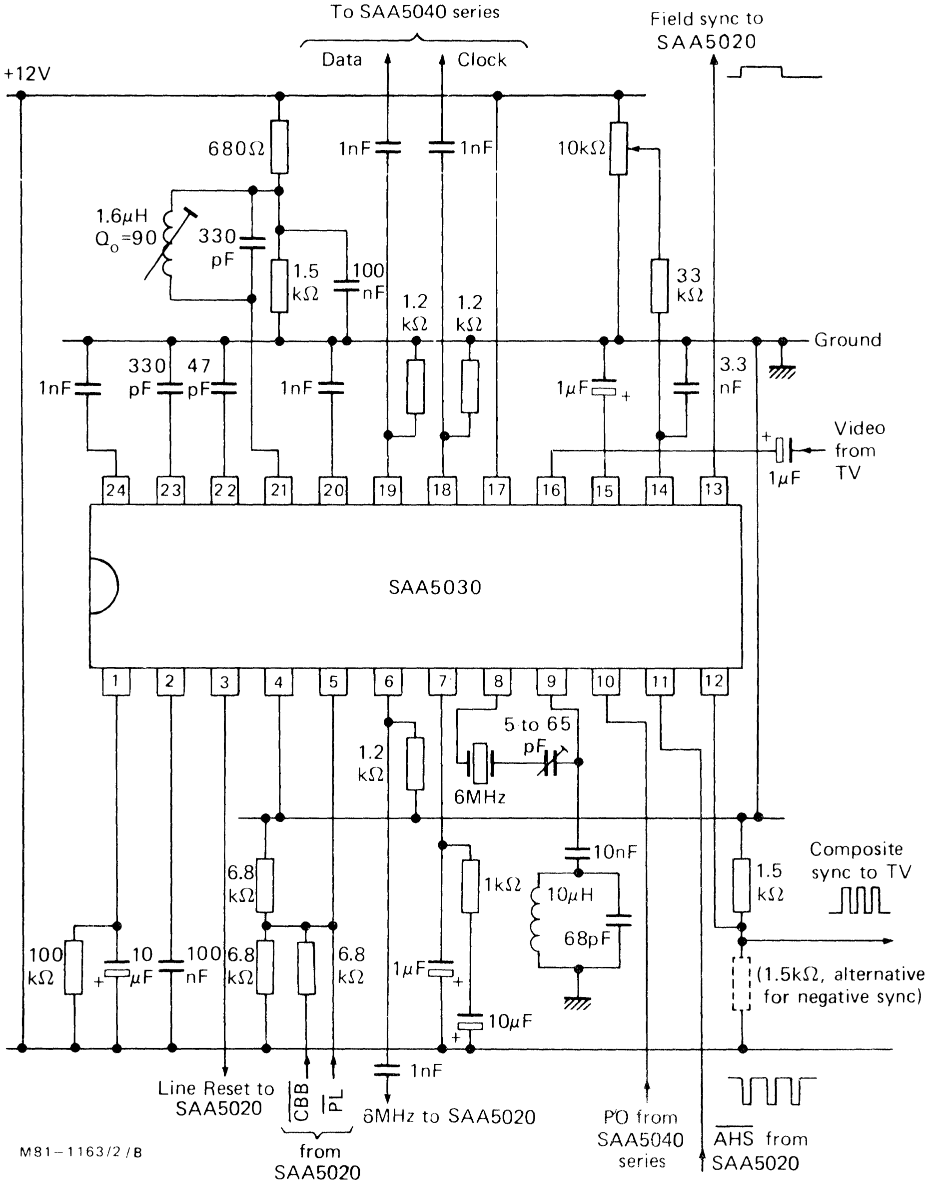


Fig.3 Peripheral circuit

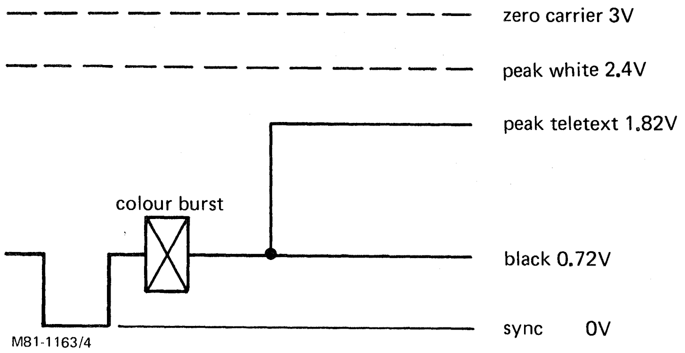


Fig.4 Part of teletext line, with burst showing nominal levels.

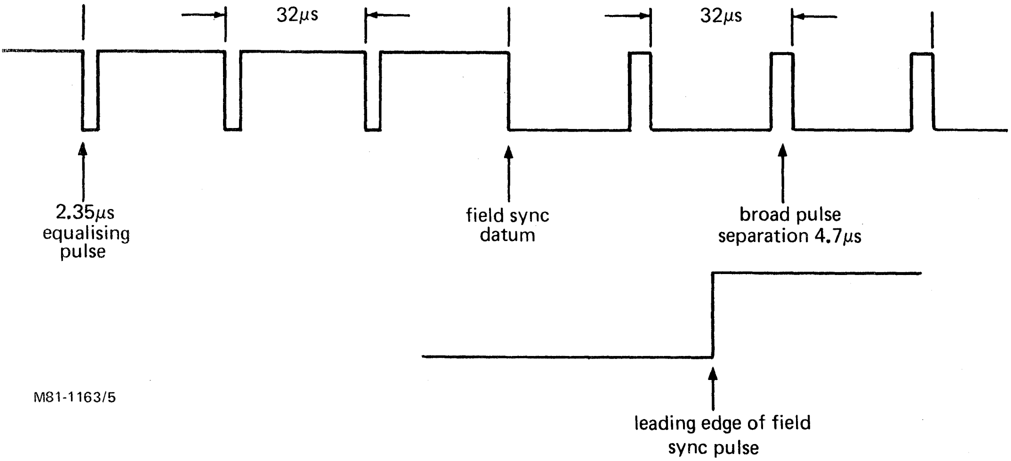


Fig.5 Detail of idealised composite sync waveform.

SOUND I.F. AMPLIFIER/DEMODULATOR FOR TV

The TBA120U is an i.f. amplifier with a symmetrical FM demodulator and an a.f. amplifier with adjustable output voltage. The a.f. amplifier is also provided with an output for volume control and an input for VCR operation.

The input and output of the TBA120U are especially designed for LC-circuits, but the input can also be used with a ceramic filter.

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	12	V
Supply current	I_P	typ.	13,5	mA
I.F. voltage gain at f = 5,5 MHz	$G_{v\ if}$	typ.	68	dB
Input voltage starting limiting	V_i	typ.	30	μV
AM suppression at $\Delta f = \pm 50$ kHz	α	typ.	60	dB
A.F. output voltage adjustment range (pin 8)	$\Delta V_{o\ af}$	typ.	85	dB
A.F. output voltage at $\Delta f = \pm 50$ kHz (r.m.s. value)				
at pin 8	$V_{o\ af(rms)}$	typ.	1,2	V
at pin 12	$V_{o\ af(rms)}$	typ.	1,0	V

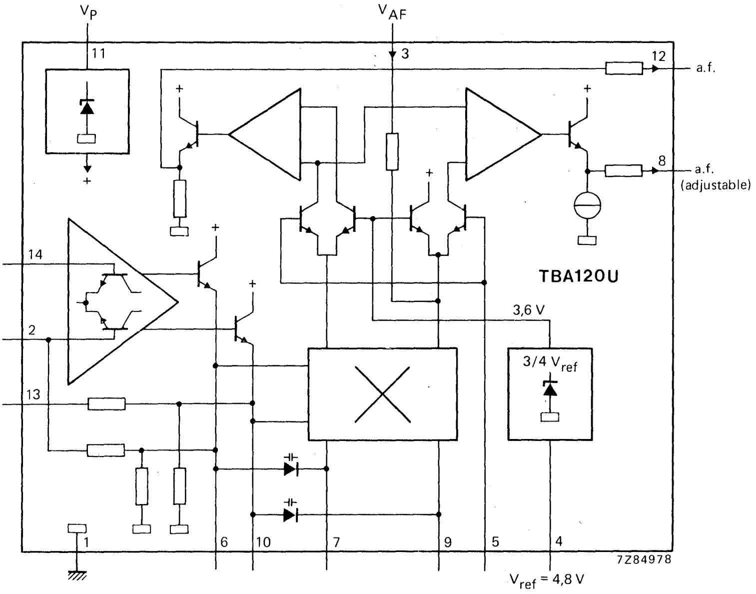


Fig. 1 Block diagram.

PACKAGE OUTLINE

14-lead DIL; plastic (SOT-27K, M, T).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11\text{-}1}$	max.	18	V*
Adjustment voltage (pin 5)	$V_{5\text{-}1}$	max.	6	V
Total power dissipation	P_{tot}	max.	400	mW
By-pass resistance	$R_{13\text{-}14}$	max.	1	kΩ
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−15 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; f = 5,5 MHz

I.F. voltage gain	$G_{v\ if\ 6\text{-}14}$	typ.	68	dB
Input voltage starting limiting at Δf = ± 50 kHz; f_m = 1 kHz	V_i	typ.	30	µV
		<	60	µV
I.F. output voltage at limiting (peak-to-peak value)	$V_{o\ if\ (p\text{-}p)}$	typ.	250	mV
AM suppression at Δf = ± 50 kHz; V_i = 500 µV; f_m = 1 kHz; m = 30%	α	>	50	dB
		typ.	60	dB
I.F. residual voltage without de-emphasis at pin 12	$V_{if\ 12}$	typ.	30	mV
at pin 8	$V_{if\ 8}$	typ.	20	mV
A.F. voltage gain	$G_{v\ af\ 8\text{-}3}$	typ.	7,5	
A.F. adjustment at $R_{4\text{-}5}$ = 5 kΩ; $R_{5\text{-}1}$ = 13 kΩ	$\Delta V_{o\ af}$		20 to 36	dB
		typ.	28	dB
A.F. output voltage control range	$\Delta V_{o\ af}$	>	70	dB
		typ.	85	dB
Adjustment resistor**	$R_{4\text{-}5}$		1 to 10	kΩ
D.C. voltage portion at the a.f. outputs pin 12	$V_{12\text{-}1}$	typ.	5,6	V
pin 8	$V_{8\text{-}1}$	typ.	4,0	V
Output resistance of the a.f. outputs pin 12	$R_{o\ 12\text{-}1}$	typ.	1,1	kΩ
pin 8	$R_{o\ 8\text{-}1}$	typ.	1,1	kΩ
Input resistance of the a.f. input	$R_{i\ 3\text{-}1}$	typ.	2	kΩ
Stabilized reference voltage	$V_{4\text{-}1} = V_{ref}$		4,2 to 5,3	V
		typ.	4,8	V
Source resistance of reference voltage source	$R_{4\text{-}1}$	typ.	12	Ω

---

* Supply voltage operating range is 10 to 18 V.

** Pin 5 must be connected to pin 4, when volume control adjustment is not applicable.

Hum suppression				
at pin 12	V_{12}/V_{11}	typ.	30	dB
at pin 8	V_8/V_{11}	typ.	35	dB
Supply current (pin 11)	$I_P = I_{11}$		9,5 to 17,5	mA
		typ.	13,5	mA
I.F. input impedance	$\lvert Z_i \rvert$	typ.	40 kΩ/4,5	pF
		>	15 kΩ/< 6	pF
A.F. output voltage at Δf = ± 50 kHz; f_m = 1 kHz; V_i = 10 mV; Q_o = 45; r.m.s. value				
at pin 12	$V_{o\,af\,(rms)}$	typ.	1,0	V
at pin 8	$V_{o\,af\,(rms)}$	typ.	1,2	V
Distortion at Δf = ± 50 kHz; f_m = 1 kHz; V_i = 10 mV; Q_o = 20	d_{tot}	typ.	1	%

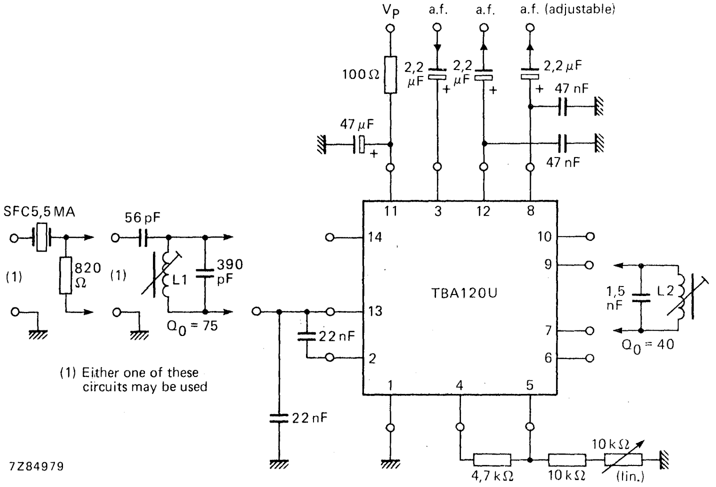


Fig. 2 Application example using TBA120U.

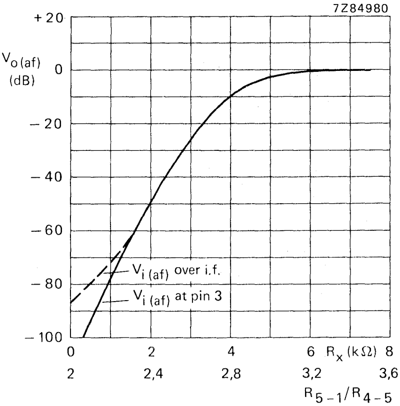


Fig. 3 The a.f. output voltage at pin 8 as a function of the resistance values as shown in Fig. 4.

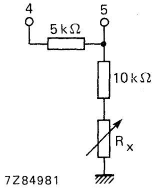
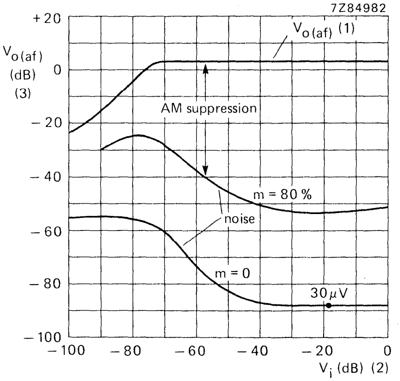


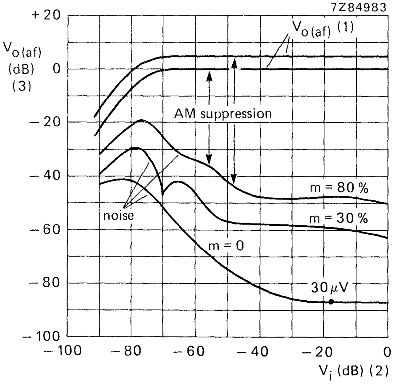
Fig. 4 Resistor conditions for curves in Fig. 3.



(1) $V_{o\,af}$ with de-emphasis at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $d_{tot} = 1{,}5\%$; 0 dB ≙ 770 mV.

(2) V_i: 0 dB ≙ 200 mV at 60 Ω.

Fig. 5 The a.f. output voltage at pin 8 as a function of the input voltage with SFC 5,5 MA at the input (see Fig. 2).



(1) $V_{o\,af}$ with de-emphasis at $f_m = 1$ kHz; 0 dB ≙ 770 mV;
curve a: $\Delta f = \pm 50$ kHz; $d_{tot} = 3\%$;
curve b: $\Delta f = \pm 25$ kHz; $d_{tot} = 1\%$.

(2) V_i: 0 dB ≙ 200 mV at pin 14.

Fig. 6 The a.f. output voltage at pin 8 as a function of the input voltage with broadband input (60 Ω).

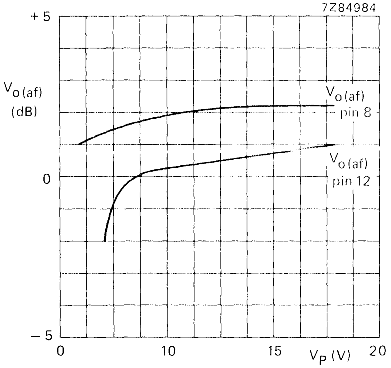


Fig. 7 The a.f. output voltages at pins 8 and 1 as a function of the supply voltage; 0 dB ≙ 770 mV.

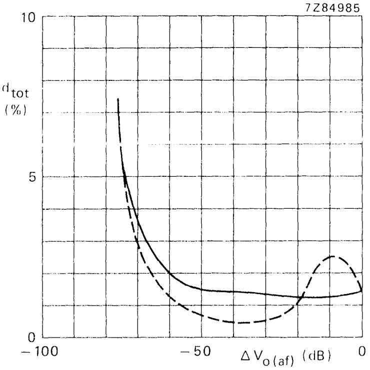


Fig. 8 Total distortion as a function of the a.f. output voltage change.
——— 0 dB ≙ 900 mV over i.f. (pin 8)
– – – – 0 dB ≙ 1,15 V (pin 8)

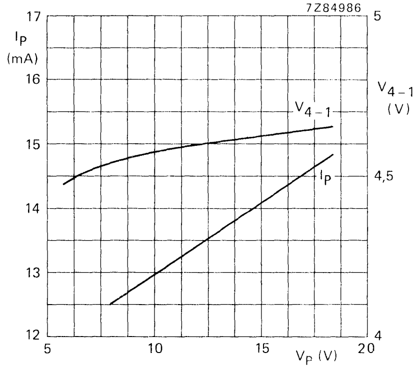


Fig. 9 Supply current and the reference voltage at pin 4 as a function of supply voltage.

REFERENCE COMBINATION

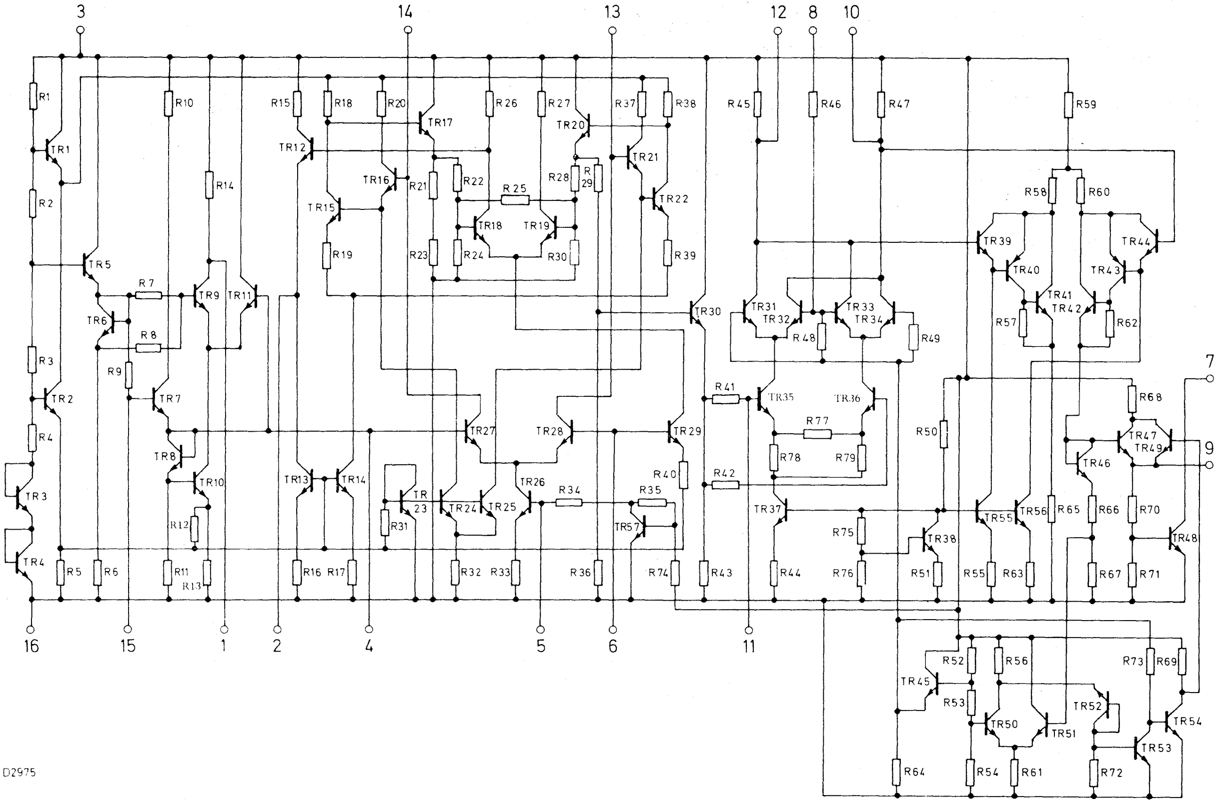
The TBA540 is an integrated reference oscillator circuit for colour television receivers incorporating an automatic phase and amplitude controlled oscillator employing a quartz crystal, together with a half-line frequency synchronous demodulator circuit. The latter compares the phases and amplitude of the swinging burst ripple and the PAL flip-flop waveform, and generates appropriate a.c.c., colour killer and identification signals. The use of synchronous demodulation for these functions permits a high standard of noise immunity.

QUICK REFERENCE DATA				
Supply voltage	V_{3-16}	nom.	12	V
Total current drain	I_3	typ.	33	mA
R-Y reference signal output peak-to-peak value	$V_{4-16(p-p)}$	typ.	1,5	V
Colour killer output: colour on	V_{7-16}	typ.	12	V
colour off	V_{7-16}	$<$	250	mV
A.C.C. output voltage range at correct phase of PAL switch	V_{9-16}		+4 to +0,2	V
at incorrect phase of PAL switch	V_{9-16}		+4 to +11	V

PACKAGE OUTLINES

TBA540 : 16-lead DIL; plastic (SOT-38).
TBA540Q: 16-lead QIL; plastic (SOT-58).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{3-16}	max.	13.2	V
Power dissipation				
Total power dissipation at T_{amb} = 50 °C	P_{tot}	max.	680	mW
Temperatures				
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		−20 to +60	°C

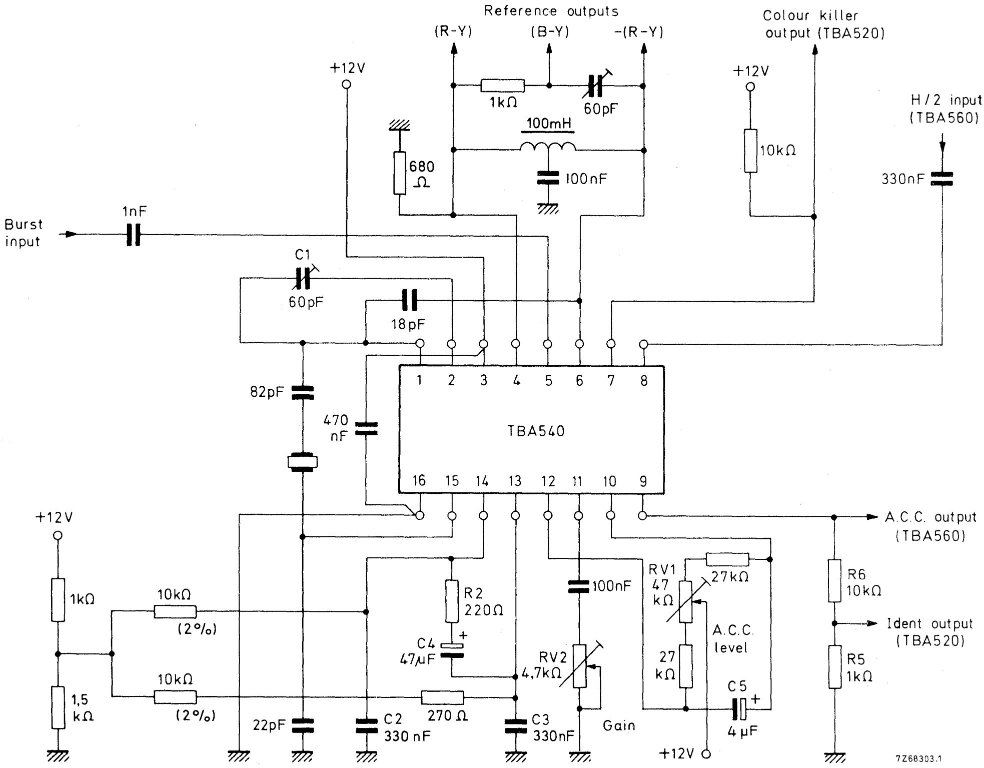
CHARACTERISTICS at V_{3-16} = 12 V; T_{amb} = 25 °C; $V_{5-16\,M}$ = 0.7 V (burst signal input); $V_{8-16(p-p)}$ = 2.5 V (P.A.L. square wave input) Measured in circuit shown on page 4.

Output signals				
R-Y reference signal output peak-to-peak value	$V_{4-16(p-p)}$	typ.	1.5	V
Colour killer output: colour on	V_{7-16}	typ.	12	V
colour off	V_{7-16}	<	250	mV
A.C.C. output signal range				
at correct phase of P.A.L. switch	V_{9-16}		+4 to +0.2	V
at incorrect phase of P.A.L. switch	V_{9-16}		+4 to +11	V
Oscillator section (amplifier)				
Input resistance	R_{15-16}	typ.	3.5	kΩ
Input capacitance	C_{15-16}	typ.	5	pF
Voltage gain	G_{15-1}	typ.	4.7	
Reactance control section				
Voltage gain with pins 13 and 14 interconnected	G_{15-2}	typ.	1.3	
Rate of change of gain G_{15-2} with phase difference between burst and reference signal	$\frac{\Delta G_{15-2}}{\Delta \varphi_{5-4}}$	typ.	5	$\frac{1}{\text{rad}}$
Supply current consumption	I_3	typ.	33	mA

PINNING

1. Oscillator feedback output
2. Reactance control stage feedback
3. Supply voltage (12 V)
4. Reference waveform output
5. Burst waveform input
6. Reference waveform input
7. Colour killer output
8. P.A.L. flip-flop square wave input
9. A.C.C. output
10. A.C.C. level setting (see also pin 12)
11. A.C.C. gain setting
12. A.C.C. level setting (see also pin 10)
13. } D.C. control points for
14. } oscillator phase control loop
15. Oscillator feedback input
16. Earth (negative supply)

APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Oscillator feedback output
   The crystal receives its energy from this pin. The input impedance is approximately 2 kΩ in parallel with 5 pF.

2. Reactance control stage feedback
   This pin is fed internally with a sinewave derived from the reference input (pin 6) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from pin 2 to the crystal via C1 is such that the value of C1 is effectively increased. Pin 2 is held internally at a very low impedance therefore the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.

3. Positive 12 V supply
   The maximum voltage must not exceed 13.2 V.

4. Reference waveform output
   This pin is driven internally by the regenerated subcarrier waveform in R-Y phase. An output amplitude of nominally 1.5 V peak-to-peak is produced at low impedance. No d.c. load to earth is required. A d.c. connection between pins 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase (-(R-Y)) to that on pin 4. A centre tap on the inductor, connected to earth via a d.c. blocking capacitor, is therefore necessary.

5. Burst waveform input
   A burst waveform amplitude of 1 V peak-to-peak is required to be a.c.-coupled to this pin. The amplitude of the burst will normally be controlled by the adjustment and operation of the a.c.c. circuit. The input impedance at this pin is approximately 1 kΩ and a threshold level of 0.7 V must be exceeded before the burst signal becomes effective. A d.c. bias of 400 mV is internally derived for pin 5 The absolute level of the tip of the burst at pin 5 will normally reach 1.25 V (1.5 V peak-to-peak burst amplitude). Under abnormal conditions the burst amplitude should not be allowed to exceed 3 V peak-to-peak and a limiting condition will be reached in the i.c. which inhibits the performance of the phase lock loop.

APPLICATION INFORMATION (continued)

6. Reference waveform input
   This pin requires a reference waveform in the -(R-Y) phase, derived from pin 4 via a bifilar transformer (see pin 4), to drive the internal balanced reactance control stage. A d.c. connection between pins 4 and 6 must be made via the transformer.

7. Colour killer output
   This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typical 10 kΩ) connected to +12 V. The unkilled and killed voltages on this pin are then +12 V and < 250 mV respectively. (The voltage on pin 9 at which switching of the colour killer output on pin 7 occurs is nominally +2.5 V

8. P.A.L. flip-flop square wave input
   A 2.5 V peak-to-peak square wave derived from the P.A.L. flip-flop (in the TBA520 demodulator i.c.) is required at this pin, a.c.-coupled via a capacitor. The input impedance is about 3.3 kΩ.

9. A.C.C. output
   An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero input signal the d.c. potential produced at pin 9 is set to be +4 V (RV1). The appearance of a burst signal on pin 5 will cause the potential on pin 9 to go in a negative direction in the event that the P.A.L. flip-flop is identified to be in the correct phase. The range of potential over which full a.c.c. control is excercised at pin 9 is determined by the control characteristics of the a.c.c. amplifier i.e. for the TBA560 from 1 V to 0.2 V. The potential at pin 9 will fall to a value within this range as the burst input signal is stabilised at 1.5 V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the P.A.L. flip-flop phase is wrong the potential on pin 9 will move positively. The potential divider R5, R6 will then operate a P.A.L. switch cut-off function in the TBA520 demodulator i.c. The switching of the colour killer output at pin 7 is designed to occur as the potential on pin 9 moves past +2.5 V.

10. A.C.C. level setting
    The network connected between pins 10 and 12 balances the a.c.c. circuit and RV1 is adjusted to give +4 V on pin 9 with no burst input signal to pin 5. C5 provides filtering.

11. A.C.C. gain control
    RV2 is adjusted to give the correct amplitude of burst signal on pin 5 (1.5 V peak-to-peak) under a.c.c. control;

12. See pin 10.

13. See pin 14.

APPLICATION INFORMATION (continued)

14. D.C. control points in reference control loop
Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purposes d.c. balancing of the reactance stage and the connection of the bandwidth-determining filter network. The conventional double time constant filter networks are R2, C2, R3, C3 and R_4, C_4. The d.c. potentials on these pins are nominally +7,2 V.

15. Oscillator feedback input
The input impedance at this pin is nominally 3.5 kΩ in parallel with 5 pF. No d.c. connection is required on this pin. The voltage in the i.c. between pin 15 and pin 1 is nominally 4.7 times.

16. Negative supply (earth)

PERFORMANCE AND COMMENTS

Initial adjustment

(a) Remove burst signal.

(b) Short-circuit pins 13-14. Adjust oscillator to correct frequency by C1. Remove short circuit.

(c) Set the a.c.c. level adjustment RV1, to give +4 V on pin 9.

(d) Apply burst signal.

(e) Adjust a.c.c. gain, RV 2, to give a burst amplitude of 1.5 V peak-to-peak on pin 5.

Phase lock loop performance (with crystal type 4322 152 0110)

(a) Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency, $\pm 10^{o}$.

(b) Typical holding range, ± 600 Hz.

(c) Typical pull-in range, ± 300 Hz.

(d) Temperature coefficient of oscillator frequency, i.c. only, 2 Hz/^{o}C.

LINE OSCILLATOR CIRCUIT

This circuit has been designed for use as line-oscillator and reactance stage in colour and monochrome t.v. receivers.
The circuit consists of a Miller-integrator-oscillator followed by a pulse shaping circuit, which delivers a positive pulse of 8 V and adjustable width. The available output current is in excess of 60 mA. Finally a supply voltage take-over switch for starting purposes is built in. The TBA720A can co-operate with the TBA890.

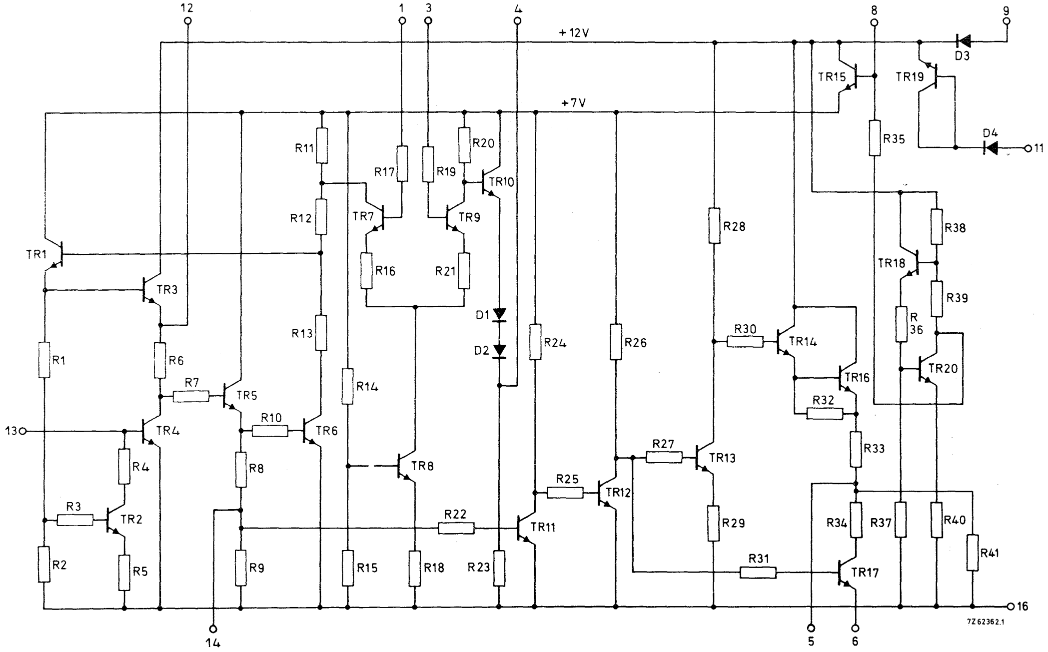
QUICK REFERENCE DATA

Supply voltage	V_{11-16}	typ.	12	V
Starting voltage	V_{9-16}		8 to 12	V
Required input signals				
D.C. control voltage at pin 1	V_{1-16}		2,4 to 5,3	V
at pin 3	V_{3-16}		2,4 to 5,3	V
Delivered output signals				
Output voltage at pin 5 no load; peak-to-peak value	$V_{5-16(p-p)}$	typ.	8	V
Output current at pin 5	I_5	<	60	mA

PACKAGE OUTLINES

TBA720A : 16-lead DIL; plastic (SOT-38).
TBA720AQ: 16-lead QIL; plastic (SOT-58).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltages

Supply voltage	V_{11-16}	max.	16 V
Starting voltage	V_{9-16}	max.	15 V

Currents

Output current	I_5	max.	60 mA

Power dissipation

Total power dissipation when mounted on a printed-wiring board	P_{tot}	max.	280 mW

Temperatures

Storage temperature	T_{stg}		-55 to +125 °C
Operating ambient temperature	T_{amb}		0 to +60 °C

CHARACTERISTICS Measured in the test set-up on page 4

Supply voltage	V_{11-16}	typ.	12 V 10 to 13 V
Starting voltage	V_{9-16}	>	8 V [1]

CHARACTERISTICS at $T_{amb} = 25\ ^{\circ}C$; $V_{11-16} = 12$ V

Supply current [2]	I_{11}	typ.	10,5 mA 7,5 to 13,5 mA

Required input signals

D.C. control voltage for nominal frequency at pin No. 1 and pin No. 3	$V_{1-16} = V_{3-16}$		2,4 to 5,3 V
Sensitivity of reactance stage	V_{1-3}	typ.	2 kHz/V
Duty cycle regulation at pin No. 14	I_{14}	typ.	0 µA +400 to -400 µA

Delivered output signals

Output voltage at pin No. 5 no load; peak-to-peak value	$V_{5-16(p-p)}$	typ.	8 V
Output current	I_5	<	60 mA
Duty cycle; without regulation	δ	typ.	40 % 35 to 45 %
with regulation	δ		20 to 60 %
Rise time at pin No. 5 leading edge of output pulse	t_r	typ.	200 ns

---

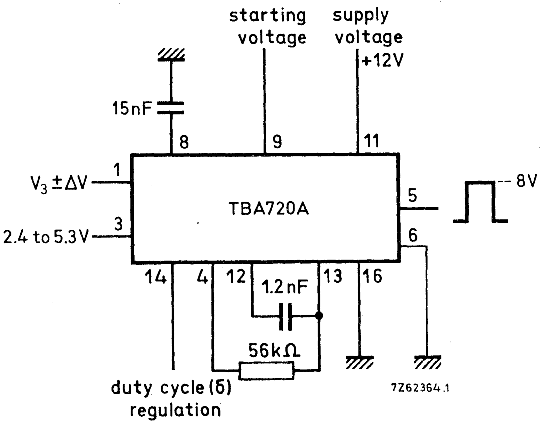
[1] Maximum starting voltage should not exceed the value of the supply voltage minus 1 volt.

[2] No load connected to the output. When the output is loaded, the extra current is: $\delta \times I$, in which δ = duty cycle of output pulse and I = current flowing during output pulse.

CHARACTERISTICS (continued)

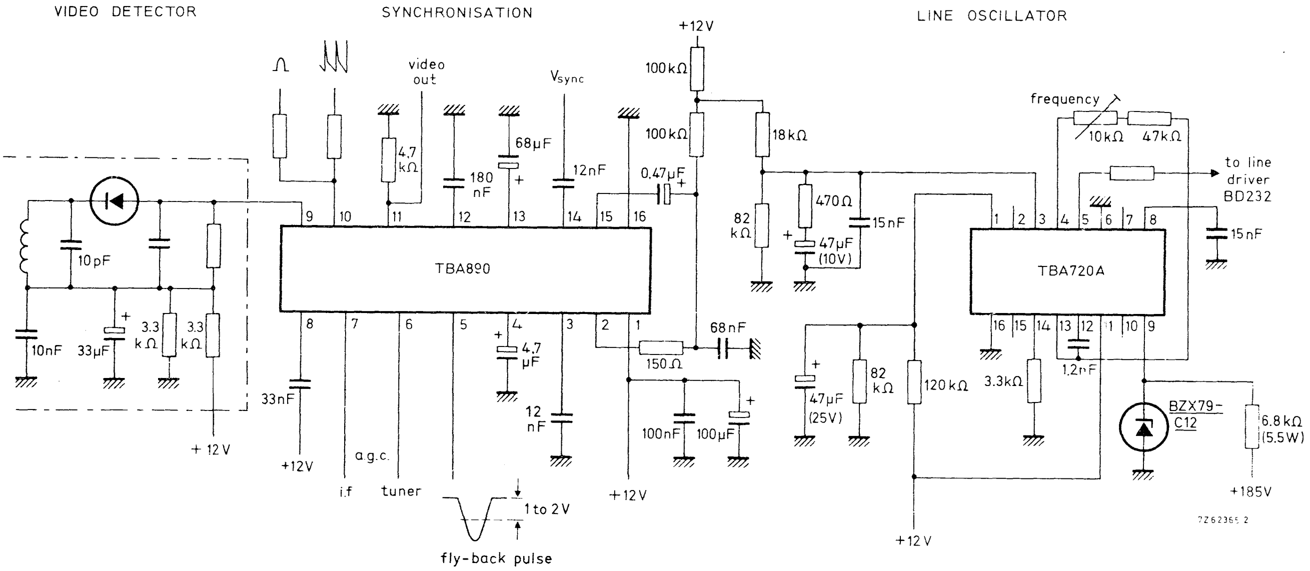
Relative frequency deviation for $\Delta V_{11} = 1$ V			2 ‰
Relative frequency deviation for change of ambient temperature 25 to 55 °C			3 ‰
Allowable hum-ripple on supply line (peak-to-peak value)	$\Delta V_{11\text{-}16(p\text{-}p)}$	typ.	100 mV

Test set-up



APPLICATION INFORMATION

The TBA720A with the TBA890 or TBA900 in a receiver with transistorized line deflection.



APPLICATION INFORMATION (continued)

Notes

1. The TBA720A is intended to drive a line deflection circuit equipped with transistors.
2. The duty cycle δ can be adjusted by connecting a resistor between pin 14 and ground or the supply.
3. The oscillation frequency can be set between 10 kHz and 25 kHz by connecting a resistor between pins 4 and 13, and a capacitor between pins 12 and 13.
4. At a nominal oscillation frequency of 15,625 kHz, the frequency deviation is limited to ±1,3 kHz to safeguard the line timebase output circuits.
5. Besides the oscillator, the TBA720A incorporates a reactance stage and a supply voltage take-over switch for starting purposes (pin 9). The latter can be used to advantage if the 12 V supply is derived from the line flyback pulse.
6. Pins 2, 7, 10 and 15 should not be connected.

LIMITER/AMPLIFIER

The TBA750C is a limiter/amplifier with f.m. detector, d.c. volume control and a.f. preamplifier. It is intended for 4,5 MHz, 5,5 MHz or 10,7 MHz. The limiter/amplifier is a four-stage differential amplifier that gives very good noise and interference suppression. The detector is of the balanced type. The d.c. volume control stage has excellent control characteristics with a control range of more than 80 dB. The a.f. preamplifier can drive a triode-pentode output stage or a class-A push-pull transistor output stage.

QUICK REFERENCE DATA

Supply voltage	V_{2-5}	typ	12	V
Total current drain	I_{tot}	typ	34	mA
Frequency	f_o		5,5	MHz
Input voltage at start of limiting	$V_{i\,lim}$	typ	130	μV
A.M. rejection at V_i = 1 mV	α	typ	45	dB
A.F. output voltage at $\Delta f = \pm$ 15 kHz at pin 16	$V_{o(rms)}$	typ	2,7	V
D.C. volume control range		>	80	dB

PACKAGES OUTLINES

TBA750C: 16-lead DIL; plastic (SOT-38).
TBA750CQ: 16-lead QIL; plastic (SOT-58).

CIRCUIT DIAGRAM

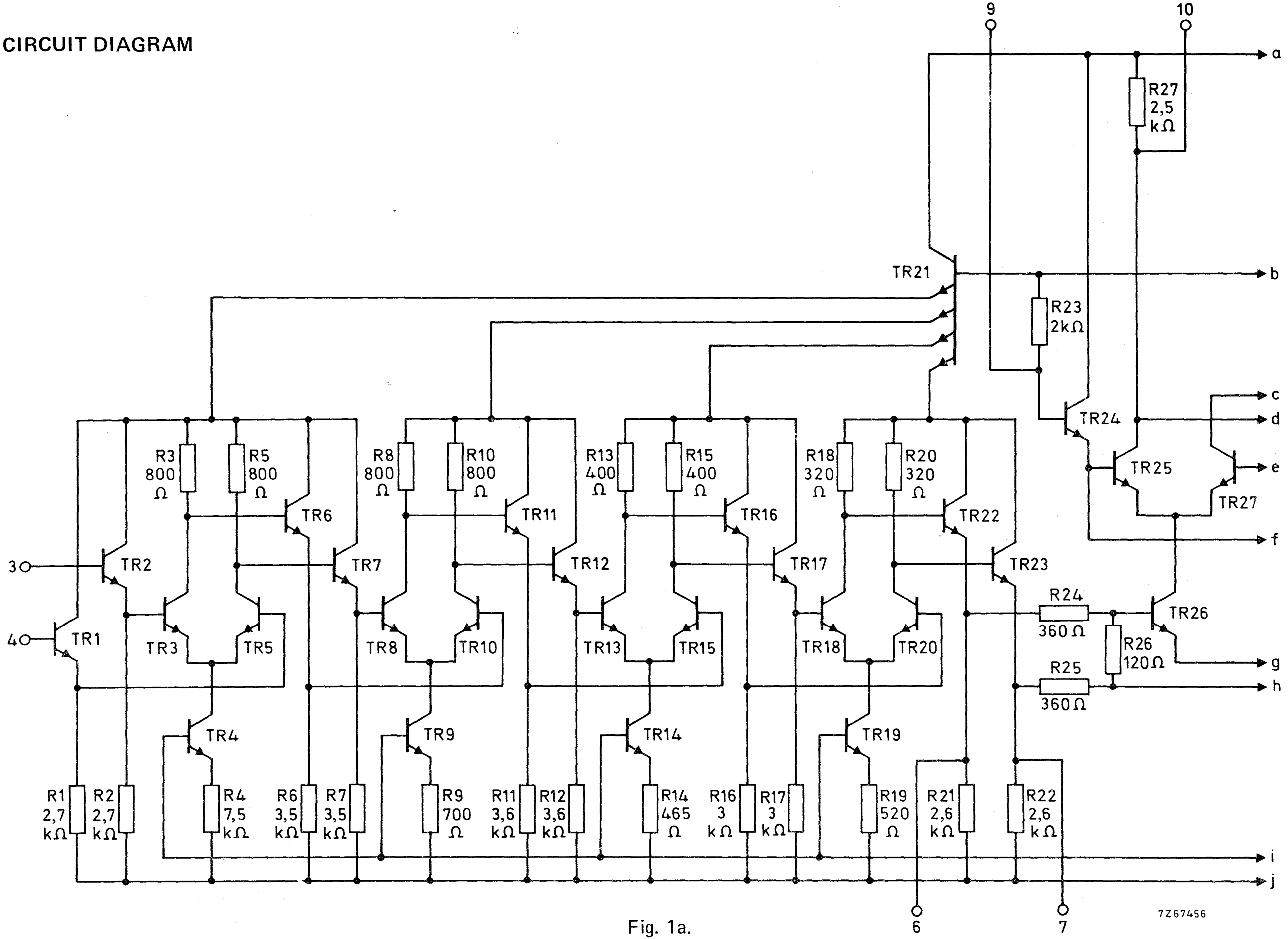


Fig. 1a.

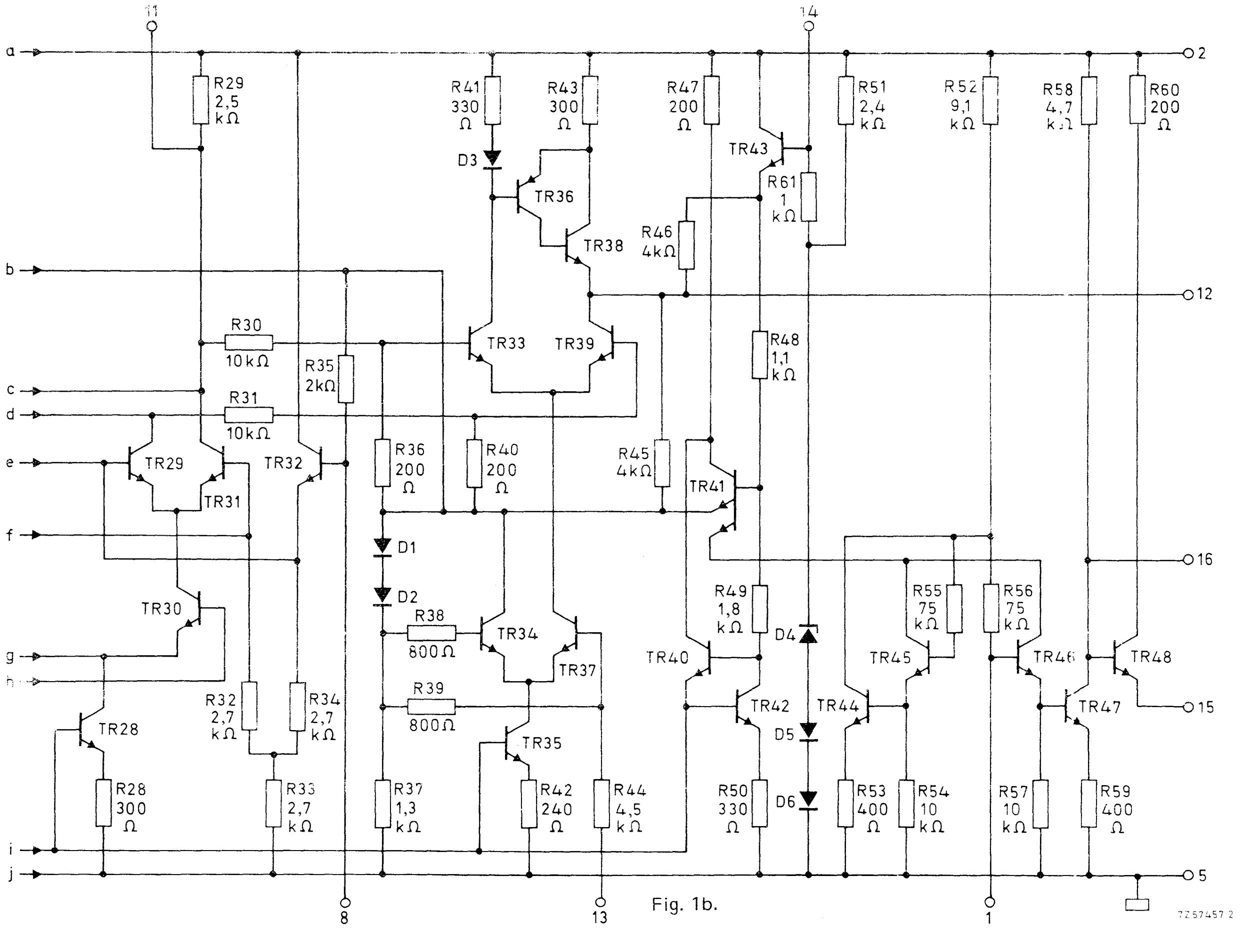

11
14
a
b
c
d
e
f
g
h
i
j
2
12
16
15
5
8
13
1
R29 2,5 kΩ
R41 330 Ω
R43 300 Ω
R47 200 Ω
R51 2,4 kΩ
R52 9,1 kΩ
R58 4,7 kΩ
R60 200 Ω
D3
TR36
TR38
TR43
R61 1 kΩ
R46 4kΩ
R30 10kΩ
R31 10kΩ
R35 2kΩ
TR33
TR39
R48 1,1 kΩ
R36 200 Ω
R40 200 Ω
R45 4kΩ
TR41
TR29
TR31
TR32
TR30
D1
D2
R38 800Ω
TR34
TR37
R39 800Ω
TR35
R49 1,8 kΩ
D4
TR40
TR42
D5
D6
R55 75 kΩ
R56 75 kΩ
TR45
TR46
TR48
TR44
TR47
TR28
R28 300 Ω
R32 2,7 kΩ
R34 2,7 kΩ
R33 2,7 kΩ
R37 1,3 kΩ
R42 240 Ω
R44 4,5 kΩ
R50 330 Ω
R53 400 Ω
R54 10 kΩ
R57 10 kΩ
R59 400 Ω
7Z57457.2

Fig. 1b.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{2-5}	max	16	V *
Storage temperature	T_{stg}		−55 to + 125	°C
Operating ambient temperature	T_{amb}		−25 to + 55	°C
Power dissipation				

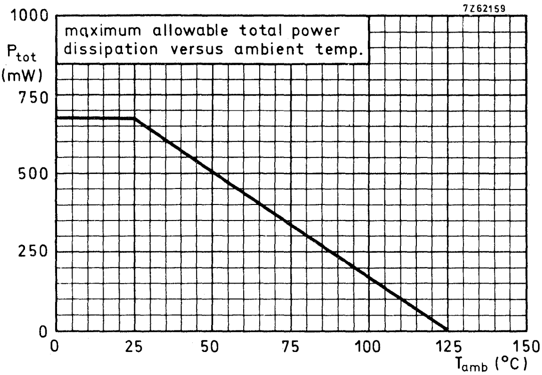


Fig. 2.

CHARACTERISTICS

Measured in test circuit Fig. 3.

Supply voltage range see also Fig. 4	V_{2-5}		10 to 25	V
Total current drain; pin 15 not connected	I_2		25 to 45	mA
Input limiting voltage at V_o = −3 dB (r.m.s. value)	$V_{i\,lim(rms)}$	typ	130	µV
I.F. output voltage at pins 6 and 7 (peak-to-peak value)	$V_{6-5(p\text{-}p)}$ $V_{7-5(p\text{-}p)}$	typ	380	mV
A.M. rejection				
V_i = 1 mV	α	typ	45	dB
V_i = 10 mV	α	typ	50	dB
V_i = 100 mV	α	typ	55	dB
D.C. volume control range; see also Fig. 5		>	80	dB
A.F. preamplifier voltage gain pin 1 to pin 16	G_v	typ	10	
Input resistance at pin 1	R_i	⩾	35	kΩ

---

* Allowable only if the dissipation in the IC is limited by means of a series resistor in the supply (see also Fig. 4).

CHARACTERISTICS (continued)

A.F. output voltages (r.m.s. values)				
$\Delta f = \pm$ 15 kHz; f_m = 1 kHz	$V_{10-5(rms)}$ $V_{11-5(rms)}$	typ	65	mV
	$V_{12-5(rms)}$	typ	250	mV
	$V_{16-5(rms)}$	typ	2,7	V
Total harmonic distortion				
at pin 12; Δf = 15 kHz	d_{tot}	typ	3	%
at pin 1 with respect to pin 16; $V_{o(rms)}$ = 3 V	d_{tot}	typ	2,6	%

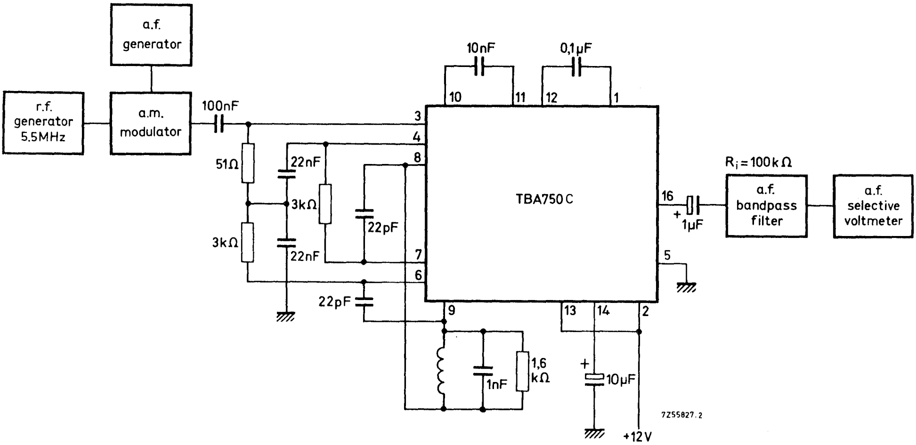


Fig.3 Test circuit; for f.m.: f_o = 5,5 MHz; $\Delta f = \pm$ 15 kHz; f_m = 70 Hz. For a.m.: m = 0,3; f_m = 1 kHz.

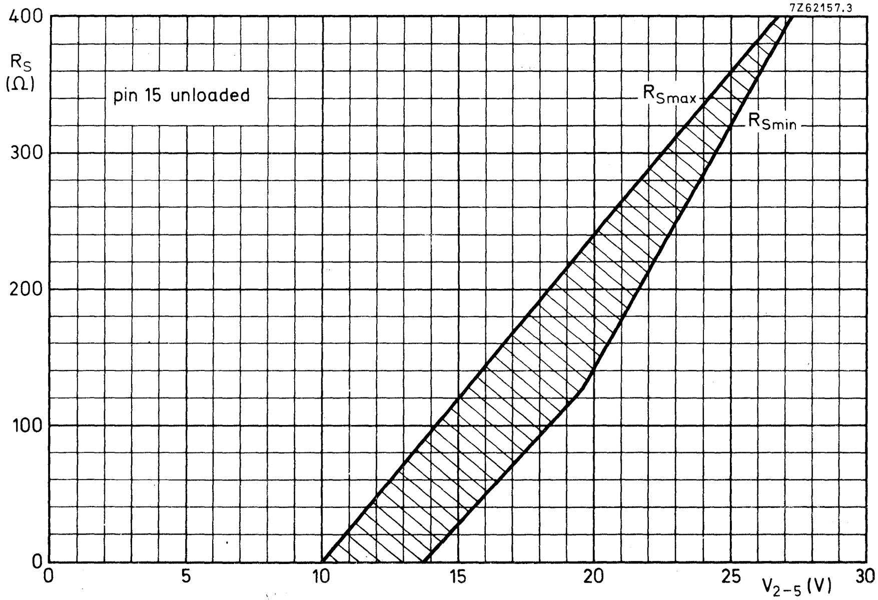


Fig. 4 Maximum and minimum values for the power supply series resistance (R_S).

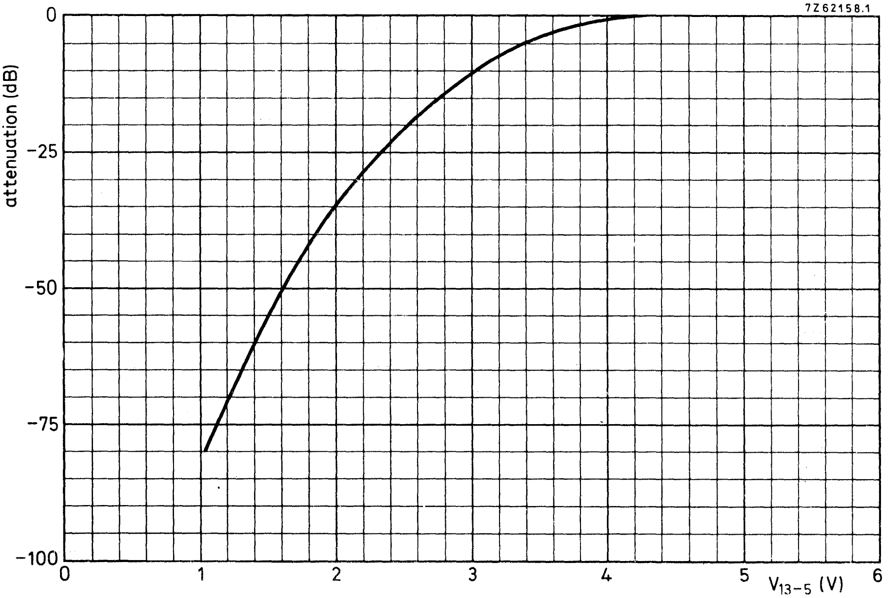


Fig. 5 Remote control characteristic.

APPLICATION INFORMATION at f = 5,5 MHz

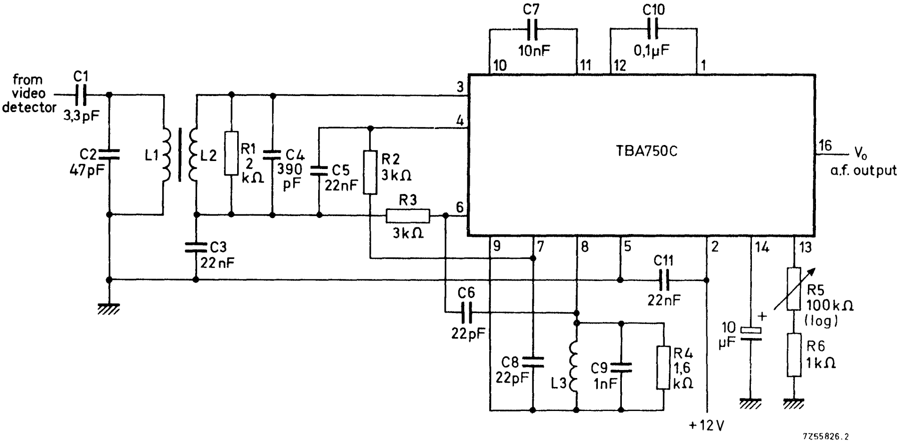


Fig. 6.

L1 = 18 µH; Q_{L1} = 36
L2 = 2,2 µH; Q_{L2} = 21
L3 = 0,84 µH; Q_{L3} = 22

Note

Q_{L1}, Q_{L2} and Q_{L3} are the loaded Q-factors.

The transfer ratio of the input bandpass filter: $\frac{V_2}{V_1} = 0{,}54$.

The peak-to-peak bandwidth of the detector S-curve is 300 kHz.

TELEVISION SIGNAL PROCESSING CIRCUIT

The TBA890 is a silicon monolithic integrated signal processing circuit for monochrome and colour television receivers.
It combines the following functions:

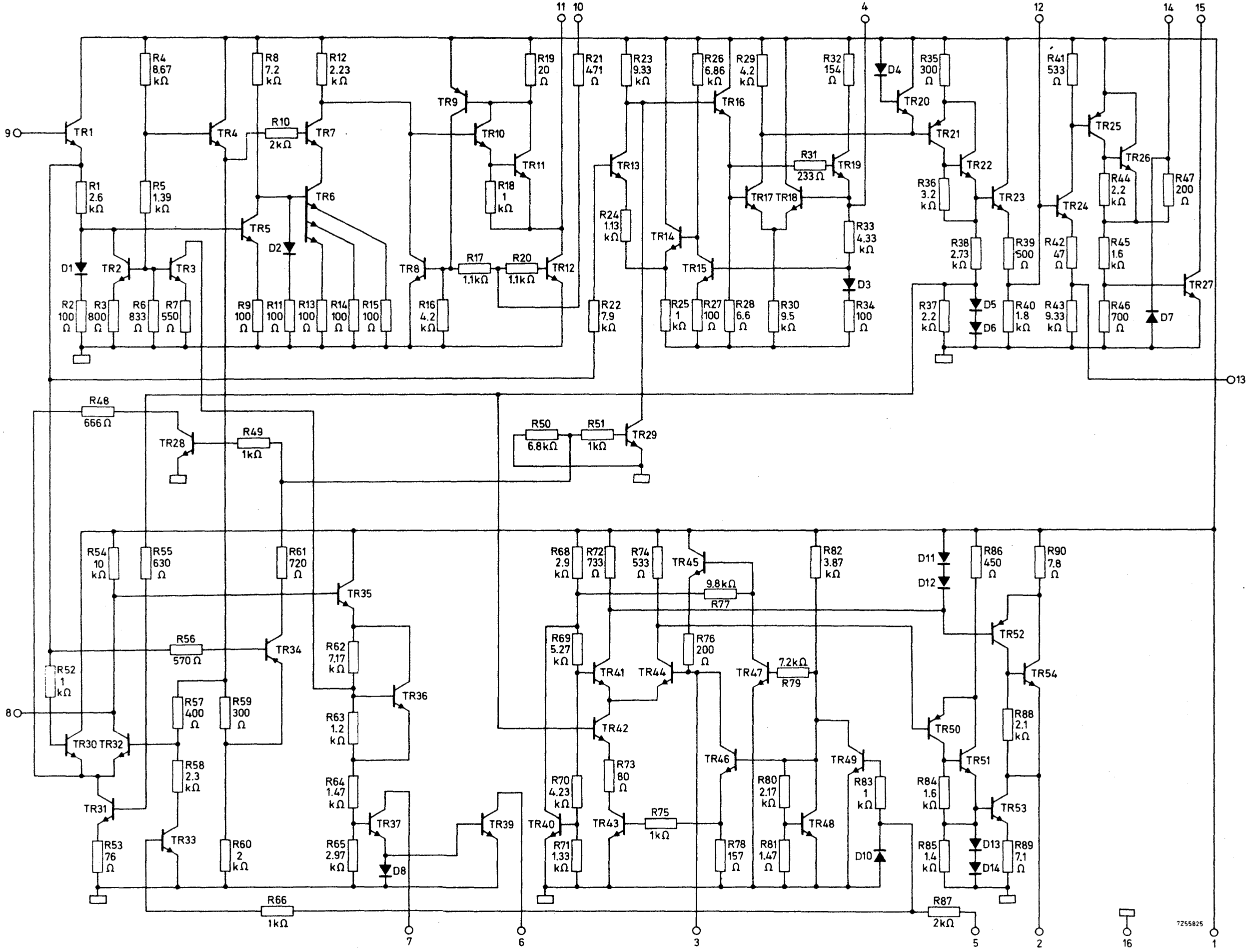
- video pre-amplifier with emitter-follower output and short circuit protection.
- blanking facility for the video amplifier.
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner.
- noise cancelling circuit in the a.g.c. and sync separator circuits.
- sync separator.
- automatic horizontal phase detector
- vertical sync pulse separator.

The circuit is designed for receivers equipped with tubes or transistors in the deflection and video output stages.
The control stages in the i.f. amplifier and the tuner have to be equipped with n-p-n transistors. The circuit is developed for signals with negative modulation.

QUICK REFERENCE DATA					
Supply voltage	V_P	typ.		12	V
Ambient temperature	T_{amb}	typ.		25	°C
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.		2,7	V
Voltage gain of the video amplifier	G_V	typ.		7	dB
A.G.C. voltage for i.f. part	V_{7-16}	1,0	to	12	V
A.G.C. voltage for tuner	V_{6-16}	0,3	to	12	V
Output voltage range horizontal phase detector	V_{2-16}	2	to	10	V
Vertical sync output voltage (positive going pulse; peak-to-peak value)	$V_{14-16(p-p)}$	typ.		11	V

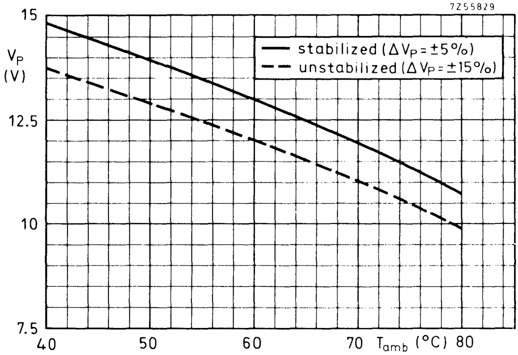
PACKAGE OUTLINES

TBA890 : 16-lead DIL; plastic (SOT-38).
TBA890Q: 16-lead QIL; plastic (SOT-58).


11
10
4
12
14
15
9
TR1
R1 2.6 kΩ
D1
R2 100 Ω
TR2
R3 800 Ω
R4 8.67 kΩ
R5 1.39 kΩ
R6 833 Ω
TR3
R7 550 Ω
TR4
R8 7.2 kΩ
R10 2kΩ
TR5
D2
R9 100 Ω
R11 100 Ω
R12 2.23 kΩ
TR7
TR6
R13 100 Ω
R14 100 Ω
R15 100 Ω
TR8
R16 4.2 kΩ
TR9
TR10
TR11
R17 1.1kΩ
R18 1 kΩ
R19 20 Ω
R20 1.1kΩ
TR12
R21 471 Ω
R22 7.9 kΩ
R23 9.33 kΩ
TR13
R24 1.13 kΩ
TR14
TR15
R25 1 kΩ
TR16
R26 6.86 kΩ
R27 100 Ω
R28 6.6 Ω
R29 4.2 kΩ
TR17 TR18
R30 9.5 kΩ
R31 233 Ω
TR19
R32 154 Ω
R33 4.33 kΩ
D3
R34 100 Ω
D4
TR20
R35 300 Ω
TR21
TR22
R36 3.2 kΩ
TR23
R37 2.2 kΩ
R38 2.73 kΩ
D5
D6
R39 500 Ω
R40 1.8 kΩ
R41 533 Ω
TR24
R42 47 Ω
R43 9.33 kΩ
TR25
TR26
R44 2.2 kΩ
R45 1.6 kΩ
R46 700 Ω
R47 200 Ω
D7
TR27
13
R48 666 Ω
TR28
R49 1kΩ
R50 6.8kΩ
R51 1kΩ
TR29
R52 1 kΩ
8
TR30 TR32
TR31
R53 76 Ω
R54 10 kΩ
R55 630 Ω
R56 570 Ω
R57 400 Ω
R58 2.3 kΩ
TR33
R59 300 Ω
R60 2 kΩ
R61 720 Ω
TR34
TR35
R62 7.17 kΩ
TR36
R63 1.2 kΩ
R64 1.47 kΩ
R65 2.97 kΩ
TR37
D8
TR39
R66 1kΩ
7
6
R68 2.9 kΩ
R69 5.27 kΩ
R70 4.23 kΩ
TR40
R71 1.33 kΩ
R72 733 Ω
TR41
TR42
R73 80 Ω
TR43
R74 533 Ω
TR44
TR45
R75 1kΩ
R76 200 Ω
R77 9.8kΩ
3
TR46
TR47
R79 7.2kΩ
R78 157 Ω
R80 2.17 kΩ
R81 1.47 Ω
TR48
R82 3.87 kΩ
TR49
R83 1 kΩ
D10
D11
D12
TR50
TR51
R84 1.6 kΩ
R85 1.4 kΩ
D13
D14
R86 450 Ω
TR52
TR53
TR54
R87 2kΩ
5
R88 2.1 kΩ
R89 7.1 Ω
R90 7.8 Ω
2
16
1
7Z55825

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.		20	V[1]
Power dissipation	P_{tot}	max.		700	mW
Temperatures					
Storage temperature	T_{stg}	−55	to	+125	°C
Operating ambient temperature	T_{amb}	-25	to	+80	°C



Maximum allowable nominal supply voltage as a function of the maximum ambient temperature.

---

[1] Allowed only while receiver is warming up.

CHARACTERISTICS

Supply voltage range V_P See curves on page 83

The following characteristics are measured in the circuit on p. 87 at $T_{amb} = 25\ ^{\circ}C$; $V_P = 12$ V.

Video amplifier

Input resistance	R_{9-16}	>	30	kΩ
Input capacitance	C_{9-16}	<	3	pF
Bandwidth (3 dB)	B	>	5	MHz
Linearity (m)		>	0.9	
Rise time and fall time at the output	$t_r; t_f$	<	50	ns
Voltage gain	G_v	typ.	7	dB
Video input voltage (peak-to-peak value)	$V_{9-16(p-p)}$	typ.	2.7	V[1]
D.C. bias video detector voltage	V_{bias}	typ.	6	V[2]
Video output voltage (peak-to-peak value)	$V_{11-16(p-p)}$	typ.	6	V[1]
Black level at the output	V_{11-16}	typ.	5	V[3]
Available video output current (peak value)	I_{11M}	≤	30	mA[4]

Tolerances on the video output voltages

I.C. processing spreads	$\pm\Delta V_{11-16}$	<	420	mV[5]
Temperature drift	$-\Delta V_{11-16}$	typ.	1.8	mV/°C
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{11-16}$	<	100	mV[6]
Supply voltage	$\frac{\Delta V_{11-16}}{\Delta V_P}$	typ.	0.5	

---

1) Signal with negative going sync.; this value is obtained only when the input signal meets the C.C.I.R. standard.

2) A voltage divider with 5% tolerance resistors is required between pin 9 and supply terminal.

3) Only valid if the video signal is in accordance with the C.C.I.R. standard.

4) The total load on pin 11 must be such that the d.c. output current $I_{11} \leq 15$ mA.

5) The spreads of the voltage divider for the bias of the video detector of ± 5% is included in this figure.

6) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

CHARACTERISTICS (continued)

Tolerances on the black level at the output				
I.C. processing spreads	$\pm\Delta V_{11\text{-}16}$	<	420	mV[1]
Temperature drift	$-\Delta V_{11\text{-}16}$	typ.	1.7	mV/^{o}C
Spreads over a.g.c. expansion (entire range)	$\pm\Delta V_{11\text{-}16}$	<	130	mV[2]
Supply voltage	$\frac{\Delta V_{11\text{-}16}}{\Delta V_P}$	typ.	0.4	
Video blanking				
Input voltage (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		1 to 5	V
Input resistance	$R_{10\text{-}16}$	typ.	1	kΩ
Output voltage during blanking	$V_{11\text{-}16}$	<	500	mV
A.G.C. circuit				
Range of control voltage i.f. amplifier	$V_{7\text{-}16}$		1 to 12	V[3]
Range of control voltage tuner	$V_{6\text{-}16}$		0.3 to 12	V[3]
Signal expansion for full control of i.f. amplifier and tuner		typ.	0.5	dB
Current i.f. control point	I_7	<	20	mA
Current tuner control point	I_6	<	20	mA
Current i.f. control point for tuner take-over	I_7	see note 4		
Keying input pulse (peak-to-peak value)	$V_{5\text{-}16(p\text{-}p)}$	see note 5		
Input resistance	$R_{5\text{-}16}$	typ.	2	kΩ

---

1) The spreads of the voltage divider for the bias of the video detector of ± 5% is included in this figure (pin 9).

2) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

3) Positive going at increasing input signal.

4) This value depends on the ratio between the external impedances on pins 6 and 7. With equal impedances the current of the i.f. control point at tuner take-over will be about 16% from its maximum value (minimum control voltage).

5) Negative going pulse is required. The voltage during scan should be between 1 V and 2 V.

CHARACTERISTICS (continued)

Horizontal synchronization circuit				
Sync. separator			see note 1	
Output voltage range of phase detector	V_{2-16}		2 to 10	V[2)]
Control steepness	S_{φ}	typ.	2.5	V/µs[3)]
Phase deviation between front edge sync. pulse and front edge flyback pulse	φ_0	typ.	1.5	µs
Variation φ_0 caused by internal spreads	$\pm\Delta_{\varphi 0}$	typ.	0.3	µs[4)]
Output voltage range as a frequency detector	V_{2-16}		4 to 8	V[5)]
Vertical synchronization circuit				
Output voltage vertical sync. pulse generator	V_{14-16}	typ.	11	V
Output impedance	R_{14-16}	typ.	2	kΩ

---

1) The sync. pulse is sliced about 25% below top sync. level. A sliding bias circuit makes the slicing level independent of the signal strength.

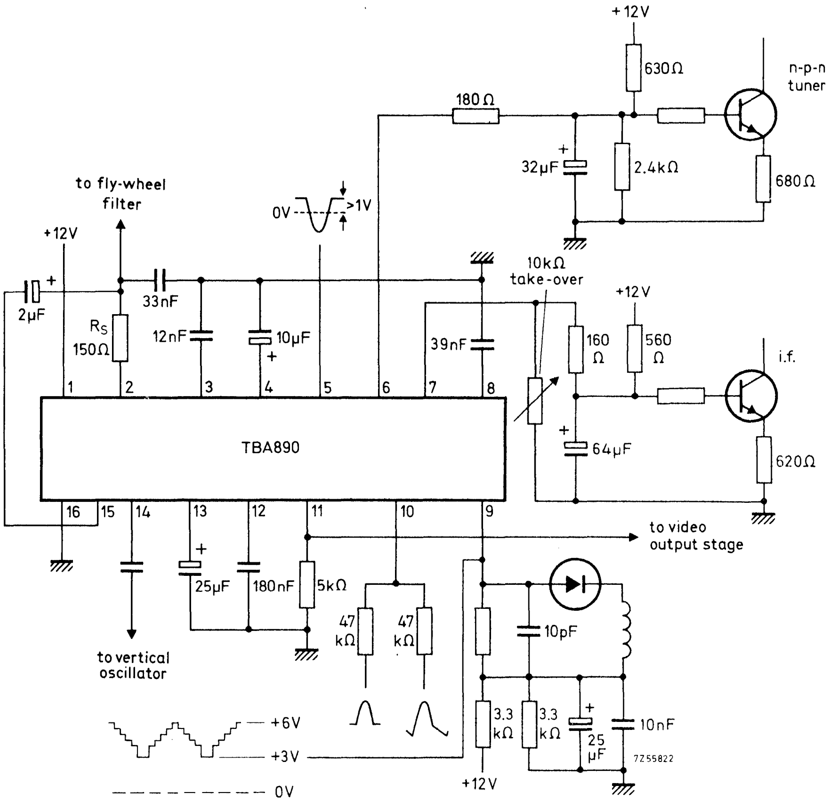
2) Nominal voltage 6 V.

3) Higher values of this control steepness can be obtained by changing R_S (see circuit on page 7). For example R_S = 56 Ω, S_{φ} = 5 V/µs and R_S = 0, S_{φ} = ≥25 V/µs.

4) In addition to this figure ± 7% of the retrace time of the sawtooth generated on pin 3 has to be added to find the total spreads of φ_0.
This value of ± 7% is obtained only when the tolerance of the capacitor connected to pin 3 does not exceed ± 10%.

5) Nominal voltage 6 V.
The load impedance on pin 2 of the circuit on page 7 is about 50 kΩ.
When a higher impedance is used (tube equipped reactance stage) values from 2 V to 10 V can be reached.

APPLICATION INFORMATION



CHROMINANCE AMPLIFIER FOR SECAM OR PAL/SECAM DECODERS

The TCA640 is an integrated chrominance amplifier for either a SECAM decoder or a double standard PAL/SECAM decoder.
Switching of the standard is performed internally, controlled by an external applied d.c. signal.
In addition to the chrominance amplifier the circuit also incorporates a 7,8 kHz flip-flop and an identification circuit for SECAM.
For PAL identification the circuit included in the TBA540 should be used.
Furthermore, the TCA640 incorporates a blanking circuit, a burst gating circuit and a colour killer detector.

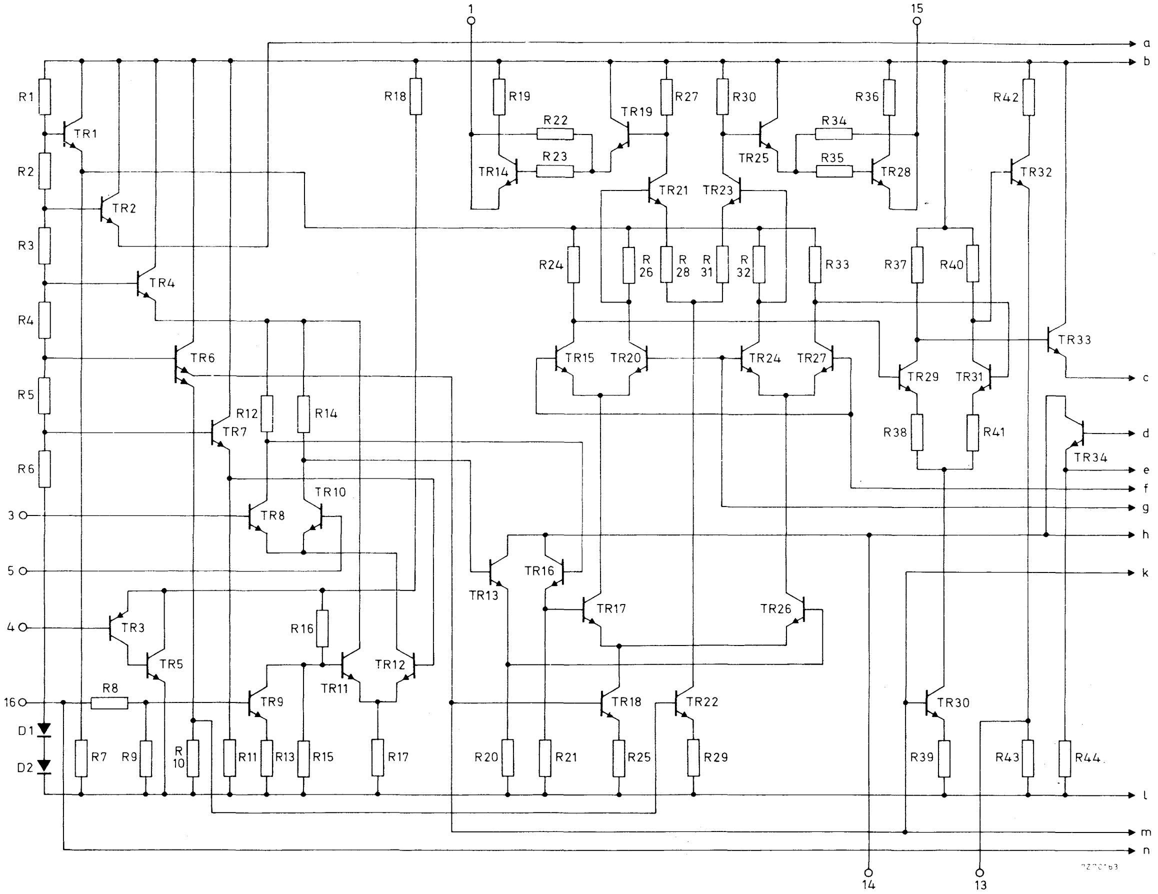
QUICK REFERENCE DATA

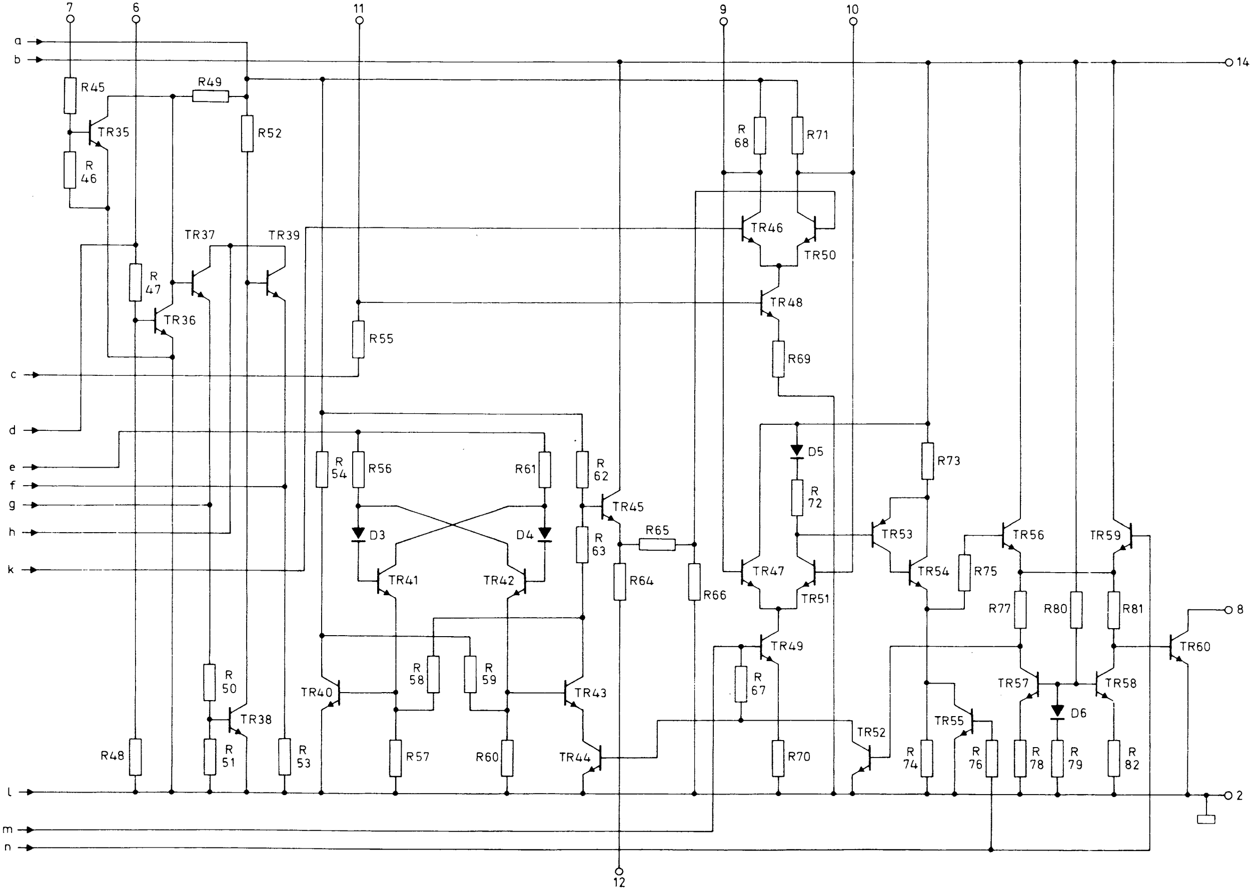
Supply voltage	V_{14-2}	nom.	12	V
Supply current	I_{14}	nom.	37	mA

			PAL	SECAM	
Chrominance input signals (peak-to-peak value)	$V_{3-5(p-p)}$	>	4	7	mV
		<	80	400	mV
Chrominance output signals (peak-to-peak value)	$V_{15-2\,(p-p)}$ $V_{1-2\,(p-p)}$	typ.	500	2000	mV
Burst output (closed a.c.c. loop) (peak-to-peak value)	$V_{13-2(p-p)}$	typ.	1	–	V
System switching signal	V_{4-2}	typ.	12	0	V
Burst blanking of chrominance signal		>	40	–	dB
Chrominance blanking at field identification		>	–	40	dB
Square-wave output (7, 8 kHz) (peak-to-peak value)	$V_{12-2(p-p)}$	typ.	3	3	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).


1
15
a
b
R1
TR1
R2
TR2
R3
TR4
R4
TR6
R5
TR7
R6
3
5
4
16
D1
D2
R7
R8
R9
R
10
TR3
TR5
TR9
R11
R13
R15
R16
TR11
TR12
R17
R12
R14
TR8
TR10
R18
R19
R22
R23
TR14
TR19
R27
TR21
R30
TR23
TR25
R34
R35
TR28
R36
R42
TR32
R24
R
26
R
28
R
31
R
32
R33
R37
R40
TR15
TR20
TR24
TR27
TR29
TR31
TR33
c
R38
R41
TR34
d
e
f
g
h
k
TR13
TR16
TR17
TR26
TR18
TR22
TR30
R20
R21
R25
R29
R39
R43
R44
l
m
n
14
13
7Z70163


7
6
11
9
10
a
b
14
R45
R49
R52
TR35
R
46
R
68
R71
TR37
TR39
TR46
TR50
R
47
TR36
TR48
R55
R69
c
d
e
f
g
h
k
D5
R73
R
54
R56
R61
R
62
R
72
TR45
R65
TR53
D3
D4
R
63
TR56
TR59
TR41
TR42
R64
R66
TR47
TR54
R75
TR51
R77
R80
R81
8
TR49
TR60
R
58
R
59
R
67
R
50
TR40
TR43
TR57
TR58
D6
TR38
TR55
TR52
R48
R
51
R
53
R57
R60
TR44
R70
R
74
R
76
R
78
R
79
R
82
l
2
m
n
12

TCA640

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage			
Supply voltage	V_{14-2}	max.	13,2 V
Power dissipation			
Total power dissipation	P_{tot}	max.	625 mW
Temperatures			
Storage temperature	T_{stg}		−25 to +125 °C
Operating ambient temperature	T_{amb}		−25 to +65 °C 1)

CHARACTERISTICS measured in the circuit on page 6

Supply voltage	V_{14-2}		typ.	12 V 10,2 to 13,2 V

Required input signals at V_{14-2} = 12 V and T_{amb} = 25 °C

Chrominance input signal				
peak-to-peak value	$V_{3-5(p-p)}$	PAL SECAM		4 to 80 mV 7 2) to 400 mV
Automatic chrominance control starting	V_{16-2}	PAL	typ.	1,2 V 3)
Flyback pulses for blanking and burst/identification lines-keying			See note 4	
Line flyback pulses (positive)				
peak-to-peak value	$V_{6-2(p-p)}$			4,5 to 12 V
Field idenfication pulses (positive)				
peak-to-peak value	$V_{7-2(p-p)}$			4 to 12 V
System switch signal	V_{4-2}	PAL SECAM		7 to V_{14-2} V 0 to 1 V
Colour killer threshold	V_{16-2}	PAL	typ.	2,5 V 5)

---

1) When a stabilized power supply of ≤ 12 V is applied, T_{amb} is max. 75 °C.

2) Start of limiting.

3) A negative-going potential provides a 26 dB a.c.c. range.

4) The line flyback pulses also provide the clock pulses for the flip-flop.

5) The colour killer is operative above the quoted input voltage.

CHARACTERISTICS (continued)

Obtainable output signals

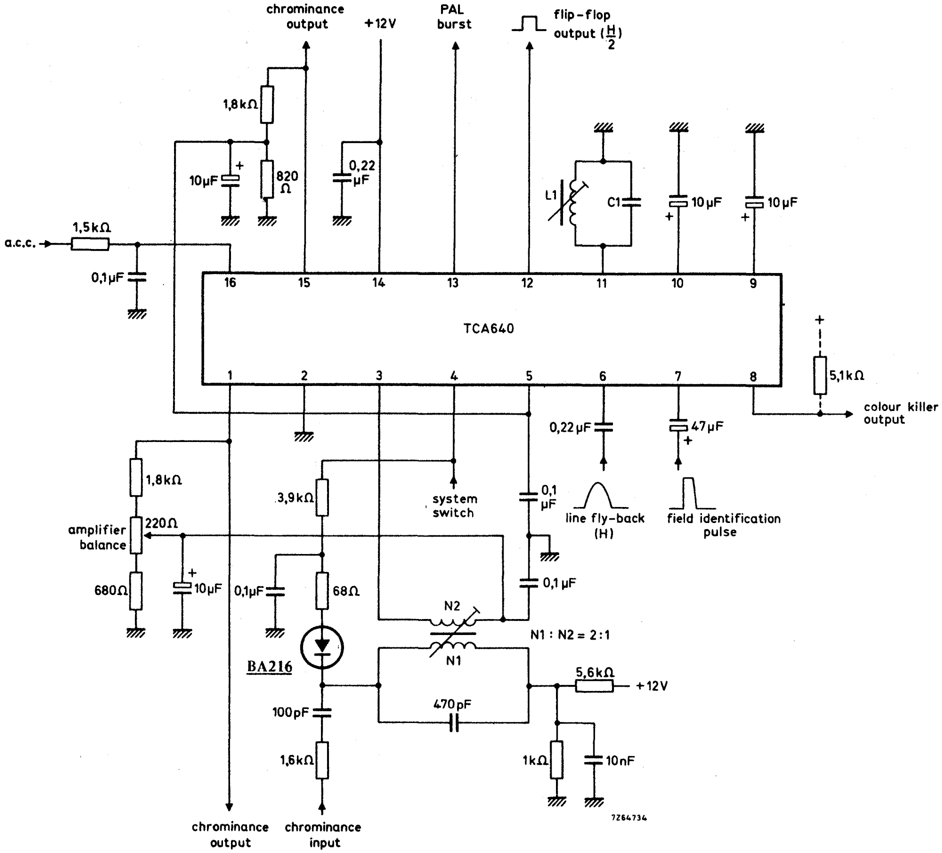
Chrominance output signals						
peak-to-peak value		$V_{15\text{-}2(p\text{-}p)}$	PAL		425 to 575	mV
		$V_{1\text{-}2(p\text{-}p)}$	SECAM		1, 8 to 2, 3	V
Phase difference between output pins		$\Delta\varphi_{15\text{-}1}$	PAL		170° to 190°	[1]
Burst signal (peak-to-peak value)		$V_{13\text{-}2(p\text{-}p)}$	PAL	typ.	1	[2]
Identification signal						
peak-to-peak value		$I_{11(p\text{-}p)}$	SECAM		1, 4 to 2, 4	mA
Output resistance		$R_{11\text{-}2}$			2 to 2, 9	kΩ
Flip-flop signal						
peak-to-peak value		$V_{12\text{-}2(p\text{-}p)}$			2, 5 to 3, 5	V
Colour killer	killed	$V_{8\text{-}2}$		<	0, 5	V
		I_8		<	10	mA
	unkilled	$V_{8\text{-}2}$			$V_{14\text{-}2}$	V
		I_8		<	10	µA
Bandwidth of chrominance amplifier (−1 dB)						
at a carrier frequency of 4, 2 MHz				>	± 1	MHz
Blanking						
burst rejection			PAL	>	40	dB
rejection identification lines with field identification			SECAM	>	40	dB

---

[1] Over the a.c.c. control range the phase difference varies less than 2, 5°.

[2] The burst is kept constant at 1 V peak-to-peak by automatic gain control.

APPLICATION INFORMATION



Pinning

1. Chrominance output	9. } Identification integrating
2. Earth (negative supply)	10. } capacitor (SECAM)
3. Chrominance input	11. Identification tank circuit (SECAM)
4. System switch input	12. Flip-flop output
5. Chrominance input	13. Burst output (PAL)
6. Line fly-back pulse input	14. Supply voltage (12 V)
7. Field identification pulse input	15. Chrominance output
8. Colour killer output	16. A.C.C. input

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Chrominance output (in conjunction with pin 15)

   A balanced output is available at pins 1 and 15.
   At SECAM reception a limited signal of 2 V peak-to-peak is available, starting from an input voltage of 15 mV peak-to-peak.
   At PAL reception the output signal is 500 mV peak-to-peak for a burst signal of 1 V peak-to-peak.
   An external d.c. network is required which provides negative feedback to pin 3. The same holds for the feedback from pin 15 to pin 5.
   The figures for input and output signals are based on a 100% saturated colour bar signal.

2. Negative supply (earth)

3. Chrominance input (in conjunction with pin 5)

   The input signal is derived from a bandpass filter which provides the required "bell" shape bandpass for the SECAM signal and a flat bandpass for the PAL signal.
   The input signal can be supplied either in a balanced mode or single ended. Both inputs (pins 3 and 5) require a d.c. potential of about 2,5 V obtained from a resistive divider connected to output pins 1 and 15. The figures for the input signals are based on a 100% saturated colour bar signal and a burst-to-chrominance ratio of 1:3 of the input signal (PAL).

4. System switch input

   Between 7 V and the supply voltage, the gain of the chrominance amplifier is controlled by the a.c.c. voltage at pin 16.
   The chrominance amplifier then provides linear amplification required for the PAL signal.
   Between 0 V and 1 V the chrominance amplifier operates as a limiter for the SECAM signal.

5. Chrominance input (see pin 3)

6. Line fly-back pulse input (in conjunction with pin 11)

   Positive going pulses provide

   - blanking of the chrominance signal at the outputs (pins 1 and 15).
   - burst gating for both PAL and SECAM.
     The carrier signal present during the second half of the back porch of the SECAM signal is gated. It provides line identification when the circuit L_1C_1 (see circuit on page 6) is tuned to 4,25 MHz (at C_1 = 470 pF).
   - trigger signal for the flip-flop.

7. Field identification pulse input (in conjunction with pin 11)

   Like the line fly-back pulses, positive going identification pulses provide blanking and burst gating.
   To operate the TCA640 on the identification lines (SECAM) in the field blanking period the circuit L_1C_1 (see circuit on page 6) should be tuned to 3,9 MHz and the capacitor C_1 should be increased to 1 nF. The field fly-back pulse should be shaped so that its amplitude exceeds 4 V during the identification lines.

APPLICATION INFORMATION (continued)

8. Colour killer output

   This pin is driven from the collector of an internal switching transistor and requires an external load resistor connected to the supply voltage. The killer is operative when the a.c.c. voltage exceeds the threshold, when the SECAM chrominance signal at the input is below the limiting level or when the flip-flop operates in the wrong phase.

9. Identification integrating capacitor (SECAM)

10. Identification integrating capacitor (SECAM)

11. Identification detector tank circuit (see pins 6 and 7)

12. Flip-flop output

    A square wave of 7,8 kHz with an amplitude of 3 V is available at this pin.
    An external load resistor is not required.

13. Burst output (PAL)

    A 1 V peak-to-peak burst (kept constant by the a.c.c. system) is produced here.

14. Supply voltage (12 V)

    Correct operation occurs within the range 10,2 to 13,2 V.
    The power dissipation must not exceed 625 mW at 65 °C ambient temperature.

15. Chrominance output (see pin 1)

16. A.C.C. input

    With the system switch input (pin 4) connected for PAL operation, a negative going potential gives a 26 dB range of a.c.c. starting at + 1,2 V
    During SECAM operation, the voltage at the input should not exceed +0,5 V, otherwise the SECAM identification circuit and the colour killer become inoperative.

CHROMINANCE DEMODULATOR FOR SECAM OR PAL/SECAM DECODERS

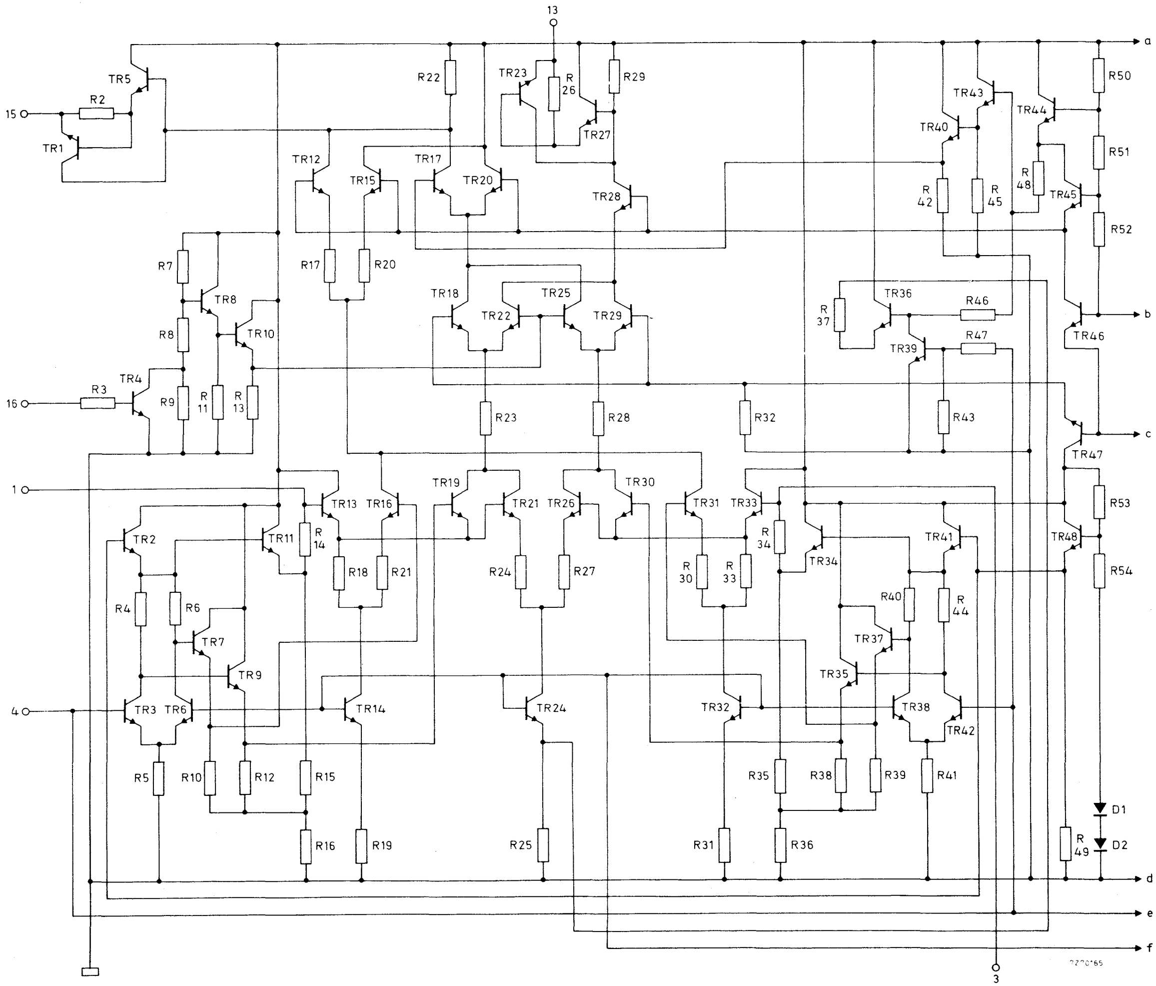
The TCA650 is an integrated synchronous demodulator for both the SECAM and PAL chrominance signals.
Switching of the standard is performed internally, controlled by an external applied d. c. signal.
In addition to the synchronous demodulator, which delivers colour difference signals, the circuit also incorporates:

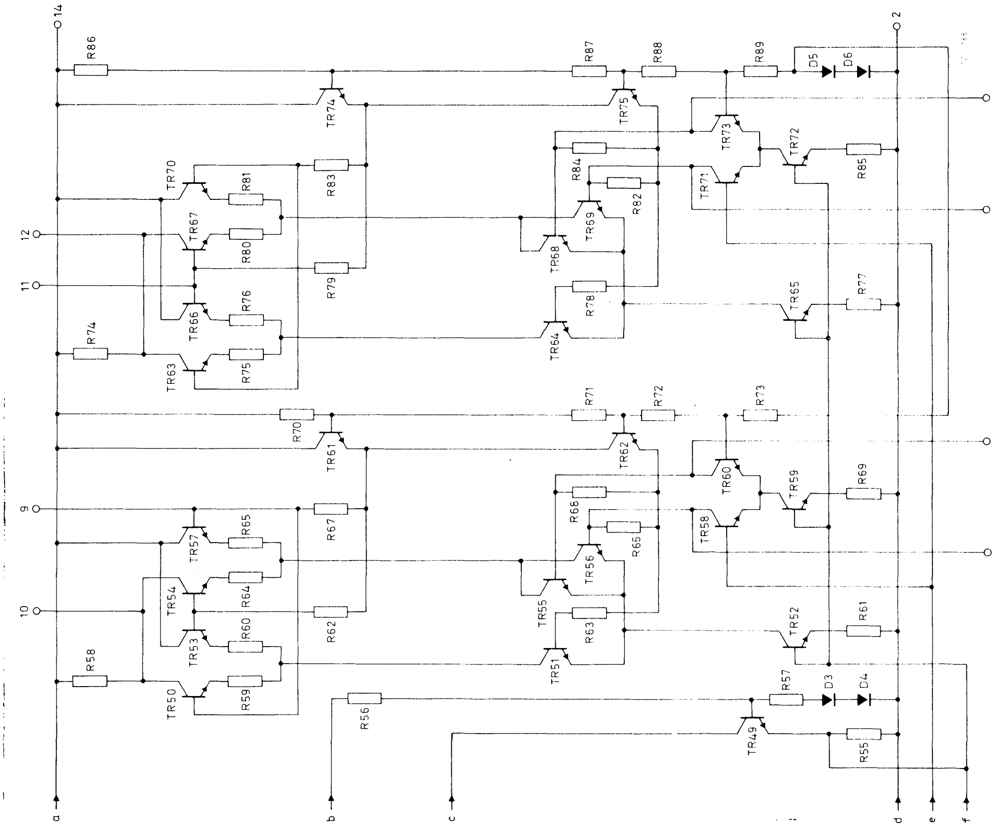
- a PAL matrix, used for adding the delayed and non-delayed signals to obtain separately the (R-Y) and (B-Y) components of the chrominance signal.
- a PAL switch, which reverses the phase of the (R-Y) component of the chrominance signal on alternating lines.
- a SECAM switch, which performs the separation of the D_R and D_B components of the chrominance signal by switching the delayed and non-delayed signals.
- a SECAM limiter.

QUICK REFERENCE DATA					
Supply voltage	V_{14-2}	nom.		12	V
Supply current	I_{14}	nom.		36	mA
			PAL	SECAM	
Chrominance input signals (peak-to-peak value)	$V_{1-2(p-p)}$ $V_{3-2(p-p)}$	typ.	50	200	mV
System switch input	V_{4-2}	typ.	12	0	V
Colour difference output signals (peak-to-peak value)	(R-Y): $V_{12-2(p-p)}$	typ.		1, 1	V
	(B-Y): $V_{10-2(p-p)}$	typ.		1, 47	V
Reference input signals (PAL) (peak-to-peak value)	$V_{6-2(p-p)}$ $V_{7-2(p-p)}$	typ.		1	V
Square-wave input (peak-to-peak value)	$V_{16-2(p-p)}$	typ.		3	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).


13
a
b
c
d
e
f
15
16
1
4
3
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
TR13
TR14
TR15
TR16
TR17
TR18
TR19
TR20
TR21
TR22
TR23
TR24
TR25
TR26
TR27
TR28
TR29
TR30
TR31
TR32
TR33
TR34
TR35
TR36
TR37
TR38
TR39
TR40
TR41
TR42
TR43
TR44
TR45
TR46
TR47
TR48
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
R46
R47
R48
R49
R50
R51
R52
R53
R54
D1
D2
7Z70165


14
2
12
11
9
10
a
b
c
d
e
f
6
5
R86
R87
R88
R89
D5
D6
TR74
TR75
TR73
TR72
TR71
R85
R84
R82
R83
TR70
R81
TR67
R80
TR69
TR68
R79
R78
TR66
R76
TR65
R77
TR64
R74
TR63
R75
R70
R71
R72
R73
TR61
TR62
TR60
TR59
R69
TR58
R68
R66
R67
TR57
R65
TR56
TR55
TR54
R64
R62
R63
TR53
R60
TR52
R61
TR51
R58
TR50
R59
R56
R57
D3
D4
TR49
R55

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{14-2}	max.	13,2	V
Power dissipation				
Total power dissipation	P_{tot}	max.	510	mW
Temperatures				
Storage temperature	T_{stg}		-25 to +125	°C
Operating ambient temperature	T_{amb}		-25 to +65	°C[1]

CHARACTERISTICS measured in the circuit on page 6

Supply voltage	V_{14-2}		typ. 12 10,2 to 13,2	V V

Required input signals at $V_{14-2} = 12$ V and $T_{amb} = 25$ °C

Chrominance input signal				
peak-to-peak value	$V_{1-2(p-p)}$	PAL	35 to 75	mV
	$V_{3-2(p-p)}$	SECAM	150 to 400	mV
Input impedance	$\lvert Z_{1-2}\rvert$ $\lvert Z_{3-2}\rvert$		1,2 to 2,6	kΩ
PAL matrix				
Gain from both inputs to pin 13			2,3 to 3,3	
Gain from both inputs to pin 15			2,6 to 3,6	
Gain difference from line-to-line			< 5	%
Phase errors from line-to-line in the (R-Y) output for zero error in the (B-Y) output			< 2,5°	
Output impedance	$\lvert Z_{13-2}\rvert$ $\lvert Z_{15-2}\rvert$		< 100	Ω
SECAM permutator				
Diaphotie			< -46	dB
Output signal (peak-to-peak value)	$V_{13-2(p-p)}$ $V_{15-2(p-p)}$		1,6[2] to 2,2	V
Output impedance	$\lvert Z_{13-2}\rvert$ $\lvert Z_{15-2}\rvert$		< 100	Ω

---

[1] When a stabilized power supply of ≤ 12 V is applied, T_{amb} is max. 75 °C.

[2] At an input voltage of 0, 15 V; at an input voltage > 0, 2 V the figure is 1, 7 V.

CHARACTERISTICS (continued)

Demodulator				
Chrominance input signal amplitude				
PAL: (B-Y); peak-to-peak value	$V_{9-2(p-p)}$	typ.	0, 22	V
(R-Y); peak-to-peak value	$V_{11-2(p-p)}$	typ.	0, 28	V
SECAM: peak-to-peak value	$V_{9-2(p-p)}$ $V_{11-2(p-p)}$		1, 5 to 3	V
Input impedance	$\lvert Z_{9-2}\rvert$ $\lvert Z_{11-2}\rvert$	>	1	kΩ
Reference input signal amplitude				
PAL: peak-to-peak value	$V_{6-2(p-p)}$ $V_{7-2(p-p)}$		0, 5 to 1, 5	V
SECAM: peak-to-peak value	$V_{5-2(p-p)}$ $V_{8-2(p-p)}$		0, 18 ¹) to 1, 5	V
Input impedance	$\lvert Z_{5-2}\rvert ; \lvert Z_{7-2}\rvert$ $\lvert Z_{6-2}\rvert ; \lvert Z_{8-2}\rvert$		0, 75 to 1, 25	kΩ
Colour difference output signal				
(R-Y); peak-to-peak value	$V_{12-2(p-p)}$		0, 99 to 1, 21	V ²)
(B-Y); peak-to-peak value	$V_{10-2(p-p)}$		1, 32 to 1, 62	V ²)
Output impedance	$\lvert Z_{10-2}\rvert$ $\lvert Z_{12-2}\rvert$		2, 4 to 4, 2	kΩ
Diaphotie at SECAM operation				
Diaphotie of the total circuit at frequencies corresponding to saturated green D_R = 4, 72 MHz and D_B = 4, 04 MHz		<	−40	dB
Square wave input				
peak-to-peak value	$V_{16-2(p-p)}$		2, 5 to 3, 5	V
Input impedance	$\lvert Z_{16-2}\rvert$	>	3, 8	kΩ
System switch input ³)				
PAL:			7 to V_{14-2}	V
SECAM:			0 to 1	V

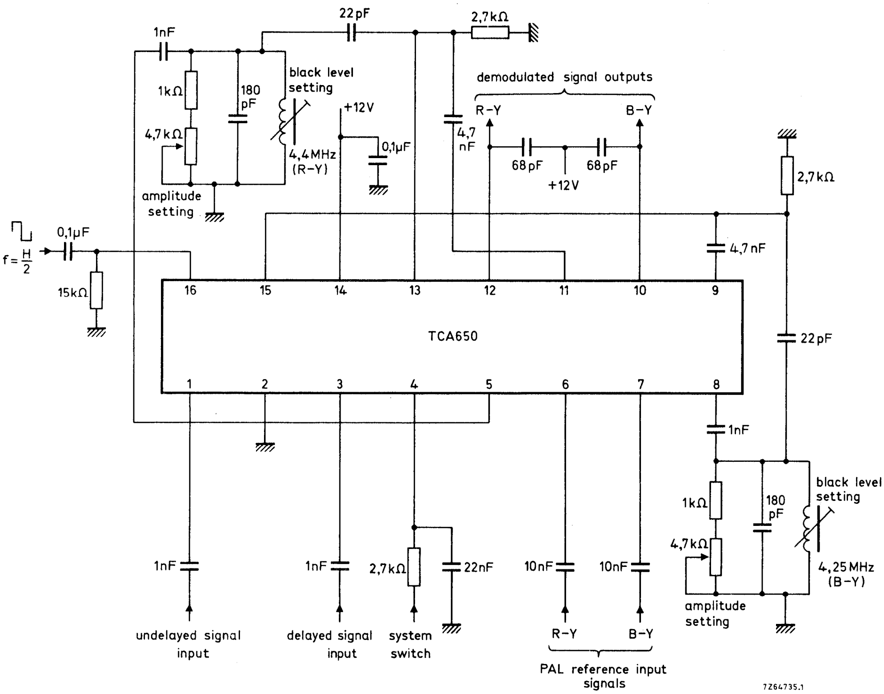
---

¹) Limiting starts at the quoted value.

²) The peak-to-peak clipping level for PAL is about 4, 7 V for (B-Y) and 3 V for (R-Y). The discriminator characteristic allows a maximum peak-to-peak output signal of 3, 6 V for (B-Y) and 2, 4 V for (R-Y) (SECAM).

³) The switching signal is applied to pin 4 via a resistor of 2, 7 kΩ (±10%).

APPLICATION INFORMATION



Pinning

1. Chrominance input
2. Earth (negative supply)
3. Chrominance input
4. System switch input
5. Reference (R-Y) input SECAM
6. Reference (R-Y) input PAL
7. Reference (B-Y) input PAL
8. Reference (B-Y) input SECAM
9. Chrominance (B-Y), D_B input
10. Colour difference (B-Y) output
11. Chrominance (R-Y), D_R input
12. Colour difference (R-Y) output
13. Chrominance (R-Y), D_R output
14. Supply voltage (12 V)
15. Chrominance (B-Y), D_B output
16. Square wave input

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Chrominance input

   The blanked composite chrominance signal from pin 1 of the TCA640 is applied to this input via a resistive divider.

2. Negative supply (earth)

3. Chrominance input

   The blanked composite chrominance signal from pin 15 of the TCA640 is applied to this input via a delay-line, which has a delay time of 64 µs.

4. System switch input

   The control voltage for switching the standard is applied to this input via a resistor of 2,7 kΩ (± 10%). A decoupling capacitor of at least 10 nF is recommended. Between 7 V and the supply voltage the circuit operates in the PAL mode, whereas between 0 V and 1 V the mode SECAM is selected.

5. Reference input for the (R-Y) demodulator

   The SECAM reference signal is applied to this pin. The reference signal is obtained from pin 11 via a tank circuit. The tank circuit is tuned such that the level at the (R-Y) output (pin 12) during black (f_0 = 4, 4 MHz) equals the level during blanking (no signal). The output voltage amplitude at pin 12 can be adjusted by damping the tank circuit.

6. Reference input for the (R-Y) demodulator

   A PAL reference signal having (R-Y) phase is applied to this pin.

7. Reference input for the (B-Y) demodulator

   A PAL reference signal having (B-Y) phase is applied to this pin.

8. Reference input for the (B-Y) demodulator

   The SECAM reference signal is applied to this pin. The reference signal is obtained from pin 15 via a tank circuit. The tank circuit is tuned such that the level at the (B-Y) output (pin 10) during black (f_0 = 4, 25 MHz) equals the level during blanking (no signal). The output voltage amplitude at pin 10 can be adjusted by damping the tank circuit.

9. Chrominance input to the (B-Y), D_B demodulator

   The output signal of pin 15 is applied via a coupling capacitor of 4, 7 nF.

10. Output of the (B-Y) demodulator

    The output signal of the balance demodulator contains an r.f. ripple of twice the chrominance frequency to be filtered by a π filter. At SECAM the required de-emphasis circuit should be applied.

11. Chrominance input to the (R-Y), D_R demodulator

    The output signal of pin 13 is applied via a coupling capacitor of 4, 7 nF.

APPLICATION INFORMATION (continued)

12. Output of the (R-Y) demodulator

    See pin 10.

13. Chrominance (R-Y), D_R output

    The (R-Y) component of the chrominance signal (D_R component at SECAM) is present at this pin.
    The signal is applied to the input of the (R-Y) demodulator (pin 11) and to the tank circuit for the SECAM reference signal.
    The emitter follower output should be loaded with a 2, 7 kΩ resistor to obtain an output impedance of $<100\ \Omega$.

14. Supply voltage (12 V)

    Correct operation occurs within the range 10, 2 to 13, 2 V.
    The power dissipation must not exceed 510 mW at 65 °C ambient temperature.

15. Chrominance (B-Y), D_B output

    The (B-Y) component of the chrominance signal (D_B component at SECAM) is present at this pin.
    The signal is applied to the input of the (B-Y) demodulator (pin 9) and to the tank circuit for the SECAM reference signal.
    The emitter follower output should be loaded with a 2, 7 kΩ resistor to obtain an output impedance of $<100\ \Omega$.

16. Square wave input

    A square wave with an amplitude of 3 V drives the PAL switch or the SECAM permutator.
    The square wave is available at pin 12 of the TCA640.

CONTRAST, SATURATION AND BRIGHTNESS CONTROL CIRCUIT FOR COLOUR DIFFERENCE AND LUMINANCE SIGNALS

The TCA660B is an integrated circuit performing the control functions of contrast, saturation and brightness in colour television receivers.
Contrast is controlled by three tracking electronic potentiometers; one for the luminance signal and the other two for the (R-Y) and (B-Y) colour difference signals.
In addition two tracking electronic potentiometers provide the saturation control of the colour difference signals.
Brightness is controlled by varying the black level of the luminance signal at the output.
An inverting amplifier is also included for matrixing the (G-Y) signal from the (R-Y) and (B-Y) colour difference signals.

QUICK REFERENCE DATA

Supply voltage	V_{13-4}	nom.	12	V	
Supply current	I_{13}	nom.	35	mA	
Luminance input current (black-to-white positive video signal)	I_{16}	typ.	0,7	mA	
Luminance output voltage (black-to-white positive video signal; peak-to-peak value)	$V_{1-4(p-p)}$	typ.	3	V	1)
Black level (nominal value)	V_{1-4}	typ.	4,2	V	
Brightness control (around nominal black level)	V_{1-4}		+1 to −2	V	
Gain of the (R-Y) and (B-Y) amplifier		typ.	5	dB	1) 2)
Gain of the (G-Y) amplifier		typ.	1		
Contrast control range			+3 to −20	dB	3)
Saturation control range			+6 to −20	dB	3)

---

1) At nominal contrast setting (max. contrast −3 dB)

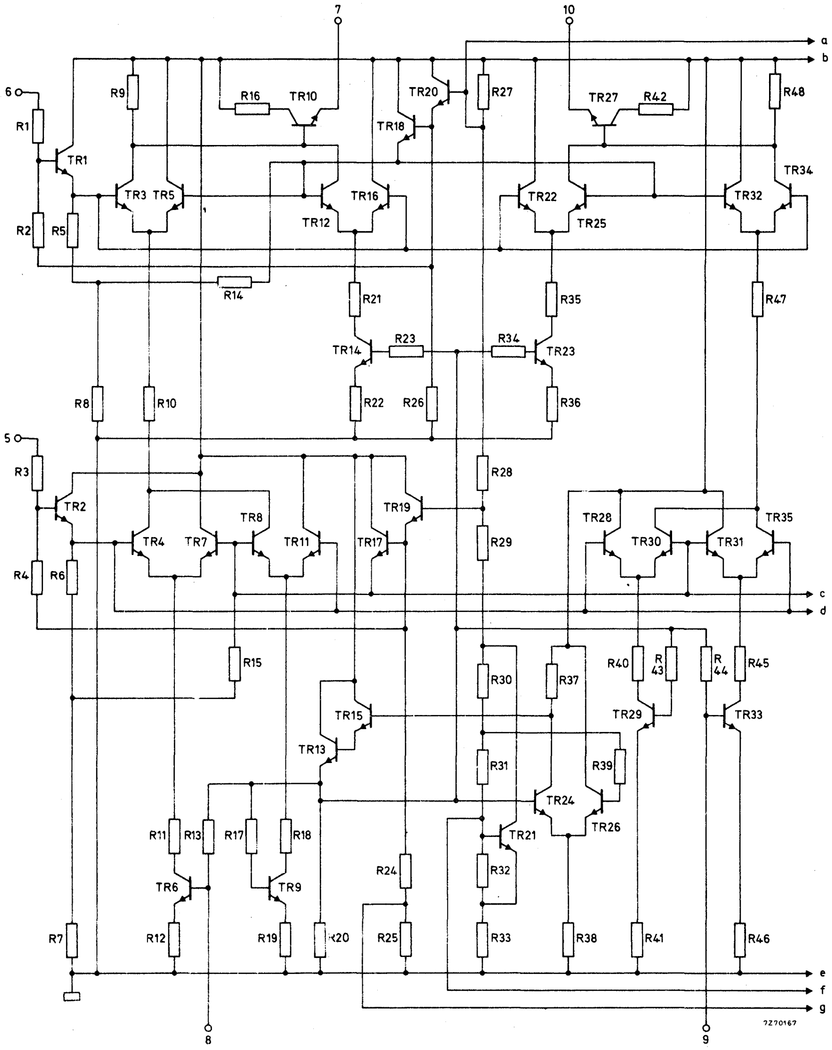
2) At nominal saturation control setting (max. saturation −6 dB)

3) Nominal contrast and nominal saturation are specified as 0 dB.

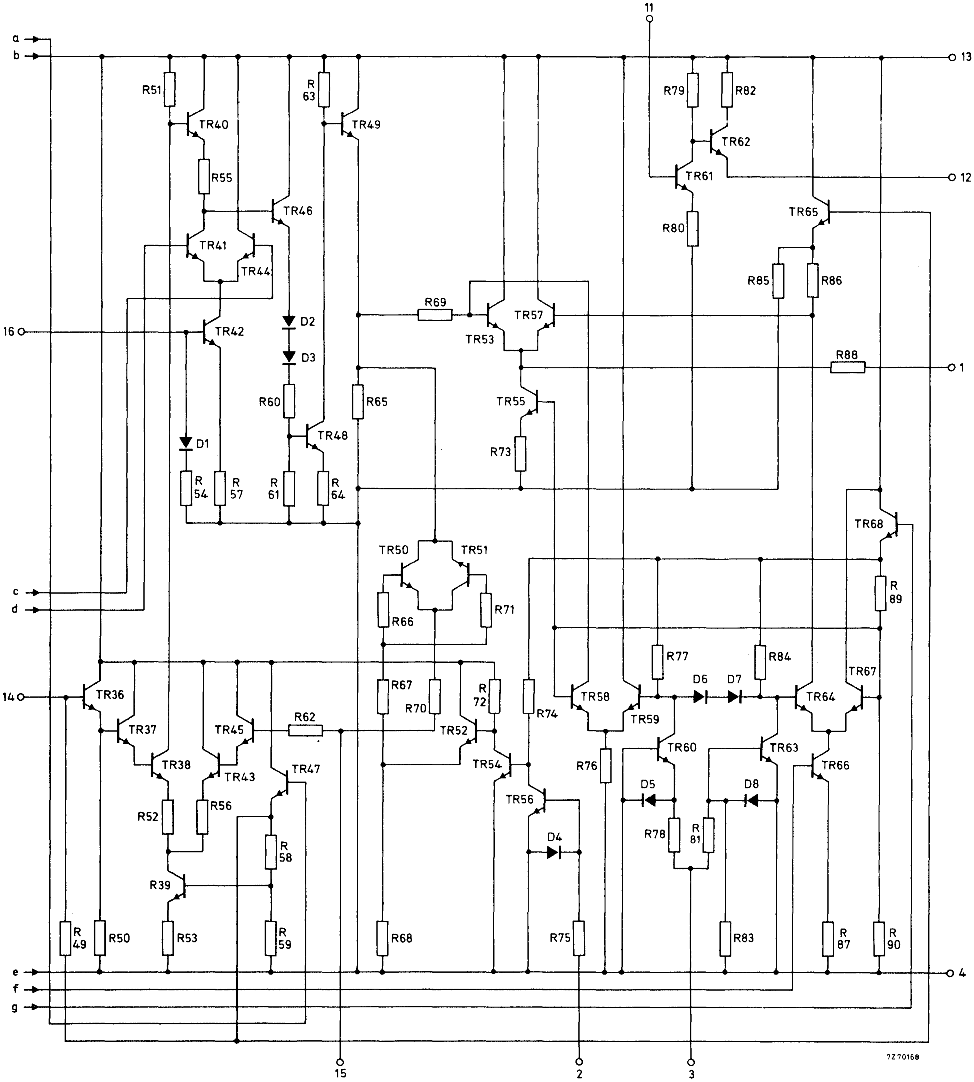
PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltage			
Supply voltage	V_{13-4}	max.	13,2 V
Power dissipation			
Total power dissipation	P_{tot}	max.	600 mW
Temperatures			
Storage temperature	T_{stg}		−25 to +125 °C
Operating ambient temperature	T_{amb}		−25 to +65 °C 1)

CHARACTERISTICS measured in the circuit on page 7

Supply voltage	V_{13-4}	typ.	12 V 10,2 to 13,2 V
Required input signals at V_{13-4} = 12 V and T_{amb} = 25 °C			
Luminance input current			
black-to-white positive video signal	I_{16}	typ.	0,7 mA 0 to 2,5 mA
Input impedance at I_{16} = 1 mA	$\|Z_{16-4}\|$		60 to 90 Ω
Input impedance variation for an input current variation $\Delta I_{16} = \pm 0,5$ mA	$\|\Delta Z_{16-4}\|$		∓25 Ω
Colour difference input voltage			
(R-Y); peak-to-peak value	$V_{9-4(p-p)}$	<	0,7 V
(B-Y); peak-to-peak value	$V_{8-4(p-p)}$	<	0,9 V
Input voltage variation before clipping of the output voltage occurs	ΔV_{8-4} ΔV_{9-4}	typ.	0,8 V
Input impedance	$\|Z_{8-4}\|$ $\|Z_{9-4}\|$		3,5 to 6,5 kΩ
Blanking pulse (peak value)	V_{3-4M}		−1,5 to −10 V
Black level reinsertion pulse (peak value)	V_{3-4M}		+2 to +12 V 2)
Black level clamp pulse (peak value)	V_{2-4M}		+1 to +12 V
Luminance output voltage at nominal contrast			
black-to-white positive video signal; peak-to-peak value	$V_{1-4(p-p)}$		2 to 4 V 3)

---

1) When a stabilized power supply of ≤ 12 V is applied, T_{amb} is max. 75 °C.

2) During scan V_{3-4} must be kept lower than 0,7 V (positive and negative) to avoid blanking of the luminance signal.

3) Nominal contrast is specified as maximum contrast −3 dB.

CHARACTERISTICS (continued)

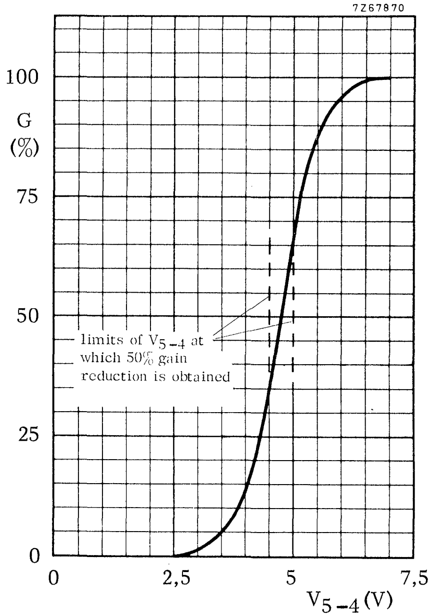
Black level at nominal brightness setting	V_{1-4}	typ.	4,2	V	1)
Black level variation with brightness setting	ΔV_{1-4}		+1 to −2	V	
Contrast control voltage range	V_{5-4}	See graph on page 6			
Black level variation with contrast control	ΔV_{1-4}	<	40	mV	2)
Black level variation with video contents	ΔV_{1-4}	<	20	mV	3)
Variation between video black level and reinserted black level at $\Delta T_{amb} = 25\ ^{\circ}C$ and $\Delta V_{13-4} \pm 10\%$	V_{1-4}	<	±20	mV	
Blanking level with respect to nominal brightness	V_{1-4}		−0,8 to −1,2	V	
Bandwidth (−3 dB) of luminance signal	B	>	6	MHz	
Colour difference output signal for nominal contrast and saturation 4) 5)					
(R-Y); peak-to-peak value	$V_{10-4(p-p)}$	typ.	1,25	V	6)
(B-Y); peak-to-peak value	$V_{7-4(p-p)}$	typ.	1,6	V	6)
D.C. output level	V_{7-4} V_{10-4}	typ.	6,1	V	
Output level variation with contrast and saturation control	ΔV_{7-4} ΔV_{10-4}	<	500	mV	
Permissible d.c. load impedance	$\lvert Z_{7-4} \rvert$ $\lvert Z_{10-4} \rvert$	>	4	kΩ	
Saturation control voltage range	V_{6-4}	See graph on page 6			
Saturation control at $V_{6-4} < 0,5$ V		<	−50	dB	
Bandwidth (−3 dB) of colour difference signal	B	>	2,5	MHz	

---

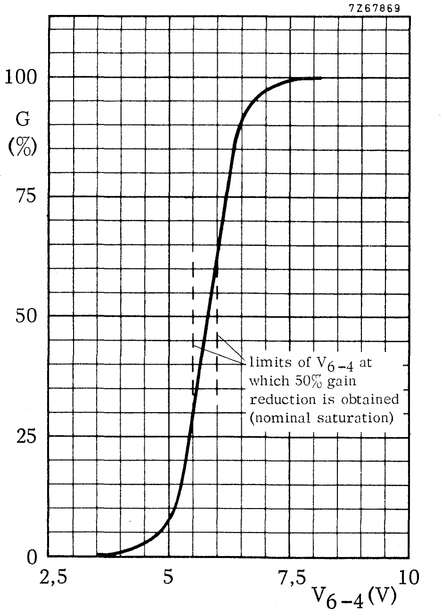
1) Nominal brightness setting $V_{14-4} = 5,7$ V.
2) Only valid if the input current does not exceed 0,5 mA during black.
3) For a.c. coupling only.
4) Nominal contrast is specified as maximum contrast −3 dB.
5) Nominal saturation is specified as maximum saturation −6 dB.
6) This value is obtained at the specified maximum input voltage.

CHARACTERISTICS (continued)

(G-Y) amplifier				
input voltage (peak-to-peak value)	$V_{11\text{-}4(p\text{-}p)}$	<	1	V
output voltage (peak-to-peak value)	$V_{12\text{-}2(p\text{-}p)}$	<	1	V
voltage gain	$G_{11\text{-}12}$		-1 to +0,5	dB
Tracking during contrast and saturation control				
at a contrast decrease of 20 dB				
change of the ratio $\frac{(R-Y)}{(B-Y)}$		<	±1	dB
change of the ratio $\frac{Y}{(B-Y)}$			0 to 4	dB
at a saturation decrease of 20 dB				
change of the ratio $\frac{(R-Y)}{(B-Y)}$		<	±1	dB
Cross coupling				
luminance signal to colour difference signal		<	-40	dB
(B-Y) signal to (R-Y) signal		<	-30	dB
colour difference signal to luminance signal		<	-40	dB

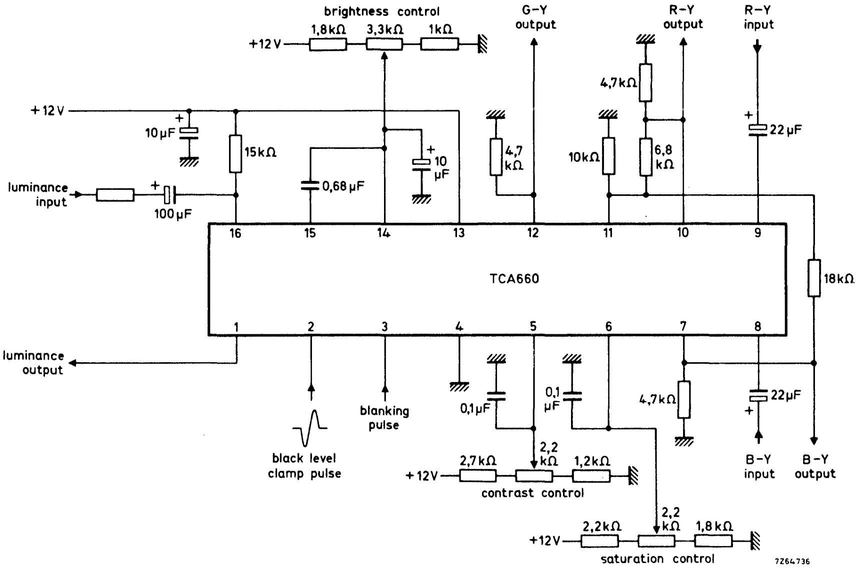


Contrast control of luminance amplifier



Saturation control of chrominance amplifier

APPLICATION INFORMATION



Pinning

1. Luminance signal output
2. Black level clamp pulse input
3. Blanking pulse input
4. Earth (negative supply)
5. Contrast control input
6. Saturation control input
7. (B-Y) signal output
8. (B-Y) signal input
9. (R-Y) signal input
10. (R-Y) signal output
11. (G-Y) signal input
12. (G-Y) signal output
13. Supply voltage (12 V)
14. Brightness control input
15. Black level clamp capacitor
16. Luminance signal input

APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Luminance signal output

   A positive video signal of 3 V peak-to-peak is available at nominal contrast setting. The black level is clamped internally on the back porch.
   By means of the brightness control the black level can be varied between 2,2 V and 5,2 V. The blanking level of the output signal will assume a value of 3,0 to 3,4 V.

2. Black level clamp pulse input

   A positive pulse with a peak value between +1 V and +12 V will clamp the black level of the video signal to a nominal level of 4,2 V. The pulse may only be present during the back porch and should have a duration of about 3 μs.

3. Blanking pulse input

   Two modes operation can be selected by the choice of the amplitude of the pulse applied:

   - blanking
   - black level reinsertion

   Blanking of the luminance output signal is obtained when the peak value of the pulse ranges from −1,5 to −10 V. An artificial black level of nominally + 4,2 V is inserted in the luminance output signal during the blanking period when the peak value of the pulse ranges from +2 to + 12 V.
   During scan the amplitude at pin 3 should remain between +0,7 V and −0,7 V to avoid blanking.

4. Negative supply (earth)

5. Contrast control input

   The contrast curve is given on page 4. To avoid damaging of the circuit by flash-over pulses, picked-up by the leads, it is recommended that a capacitor of 100 nF be connected between this pin and earth.

6. Saturation control input

   The control curve is given on page 4. To avoid damaging of the circuit by flash-over pulses, picked-up by the leads, it is recommended that a capacitor of 100 nF be connected between this pin and earth.

7. (B-Y) signal output

   The amplitude of this signal is controlled by the contrast setting and the saturation setting simultaneously. At nominal contrast and nominal saturation setting an amplitude of 1,6 V peak-to-peak is obtained at an input amplitude of 0,9 V peak-to-peak. The average level is typically 6,1 V.

8. (B-Y) signal input

   The signal has to be a.c. coupled to the input.
   To cope with the variation of picture contents an input voltage margin of ± 0,8 V is provided, whereas the input signal has a typical value of ± 0,45 V for a saturated colour bar signal.

APPLICATION INFORMATION (continued)

9. (R-Y) signal input

The signal has to be a.c. coupled to the input.
To cope with the variation of picture contents an input voltage margin of ± 0,8 V is provided, whereas the input signal has a typical value of ± 0,35 V for a saturated colour bar input.

10. (R-Y) signal output

The amplitude of this signal is controlled by the contrast setting and saturation setting simultaneously. At nominal contrast and nominal saturation setting an amplitude of 1,25 V peak-to-peak is obtained at an input amplitude of 0,7 V peak to peak.
The average level is typically 6,1 V.

11. (G-Y) signal input

The (G-Y) signal is obtained by matrixing a part of the (R-Y) and (B-Y) signals in a resistor network. The input may range from 1 to 6,5 V.
An average level of typical 5,9 V is required to produce an average output level of 6,1 V.
The gain of the inverter stage is typically 1.

12. (G-Y) signal output

An inverted signal with an amplitude of maximum 1 V peak-to-peak is available at this pin.

13. Supply voltage (12 V)

Correct operation occurs within the range 10,2 to 13,2 V.
The power dissipation must not exceed 600 mW at 65 °C ambient temperature.

14. Brightness control input

The black level of the luminance output signal tracks the potential applied to this pin.
A typical value for setting the brightness control is 5,7 V, for which a black level of 4,2 V is obtained.
It is recommended that a capacitor of at least 10 μF be connected between this pin and earth.

15. Black level clamp capacitor

The level of the back porch of the luminance output signal is stored in an external capacitor of about 0,68 μF; the latter to be connected between pins 14 and 15.

16. Luminance signal input

A positive luminance signal of 0,7 mA peak-to-peak between black and white level drives the luminance amplifier.
A black level of about 0,3 mA is recommended. For a.c. coupling a bias resistor to the supply line is required to bias the amplifier properly.
The resistance depends on the signal amplitude e.g.: 15 kΩ is recommended for a input signal of 0,7 mA peak-to-peak.

DOUBLE BALANCED MODULATOR/DEMODULATOR

The TDA0820T is a monolithic integrated circuit for use at frequencies up to 650 MHz.
Typical applications are:

- modulator
- mixer
- switch/chopper
- a.m. synchronous demodulator
- f.m. quadrature demodulator
- phase comparator
- differential amplifier

The circuit is arranged to offer very flexible circuit design possibilities. The excellent matching and temperature tracking of the transistors in the circuit allow the use of circuit techniques which are not available when using discrete devices.

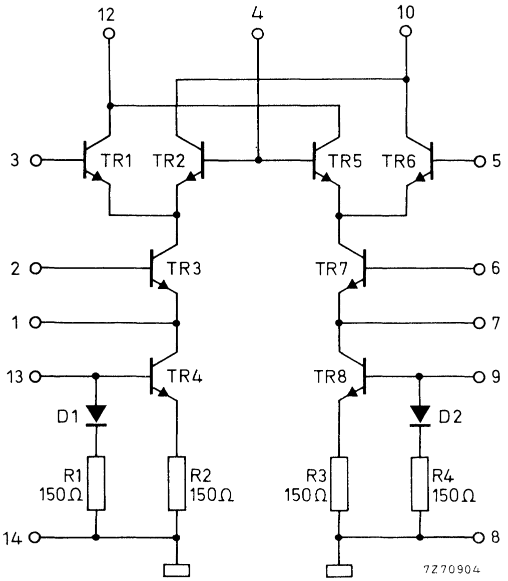


Fig. 1 Circuit diagram.

PACKAGE OUTLINE

14-lead mini-pack; plastic (SO-14; SOT-108A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_{10\text{-}8}$; $V_{10\text{-}14}$; $V_{12\text{-}8}$; $V_{12\text{-}14}$		0 to 13,2	V
Voltages (each transistor)				
Collector-substrate voltage (open base and emitter)	V_{CSO}	max.	15	V
Collector-base voltage (open emitter)	V_{CBO}	max.	12	V
Collector-emitter voltage (open base)	V_{CEO}	max.	10	V
Emitter-base voltage (open collector)	V_{EBO}	max.	5	V
Currents (each transistor)				
Emitter current	I_E	max.	10	mA
Base current	I_B	max.	10	mA
Total power dissipation when mounted on a printed-circuit board	P_{tot}	max.	250	mW
Storage temperature	T_{stg}		−55 to + 125	°C
Operating ambient temperature	T_{amb}		0 to + 70	°C

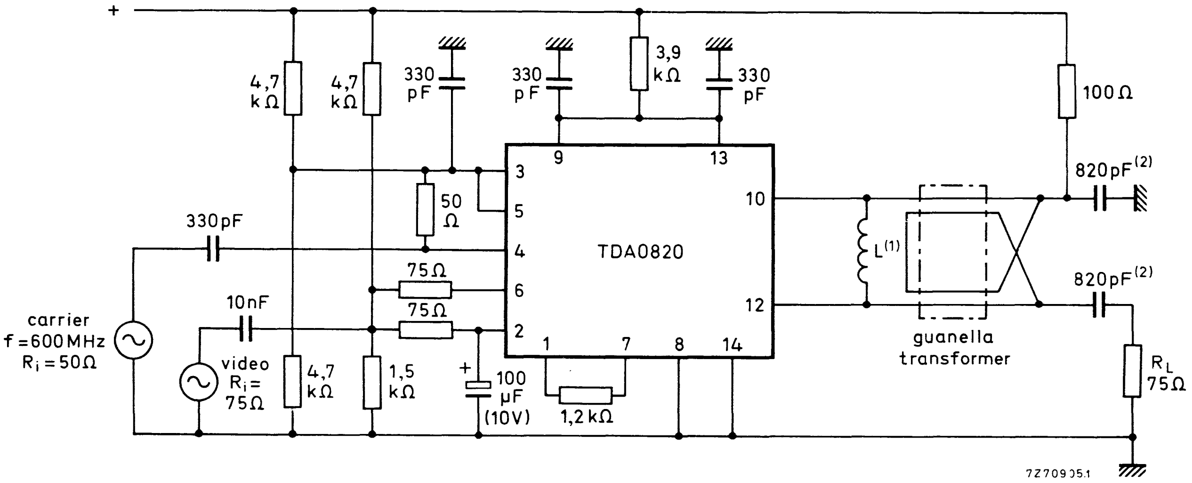
THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	220	K/W

CHARACTERISTICS

$V_{10\text{-}8} = V_{10\text{-}14} = V_{12\text{-}8} = V_{12\text{-}14} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 2

Supply current	$I_{10} + I_{12}$	typ. $<$	2,5 3	mA mA
Input signals				
carrier signal (r.m.s. value)	$V_{3\text{-}4(rms)}$; $V_{5\text{-}4(rms)}$	$<$	100	mV
video signal; negative modulated (peak-to-peak value)	$V_{6\text{-}2(p\text{-}p)}$	$<$	1,4	V
Output signal at top sync over 75 Ω (peak-to-peak value)	$V_{10\text{-}12(p\text{-}p)}$	$>$	22	mV
Carrier suppression in balanced condition	$V_{10\text{-}12}$	$>$	38	dB
Differential phase		$<$	6°	
Differential gain		$<$	15	%
Distortion of video signal		$<$	−38	dB



(1) L = air coil; 3 turns; ϕ 3 mm.

(2) U.H.F. decoupling capacitor 2212 669 98003.

Fig. 2 Test circuit.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 14)	V_P	typ.	20	V
Current consumption	I_{14}	typ.	3,5	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

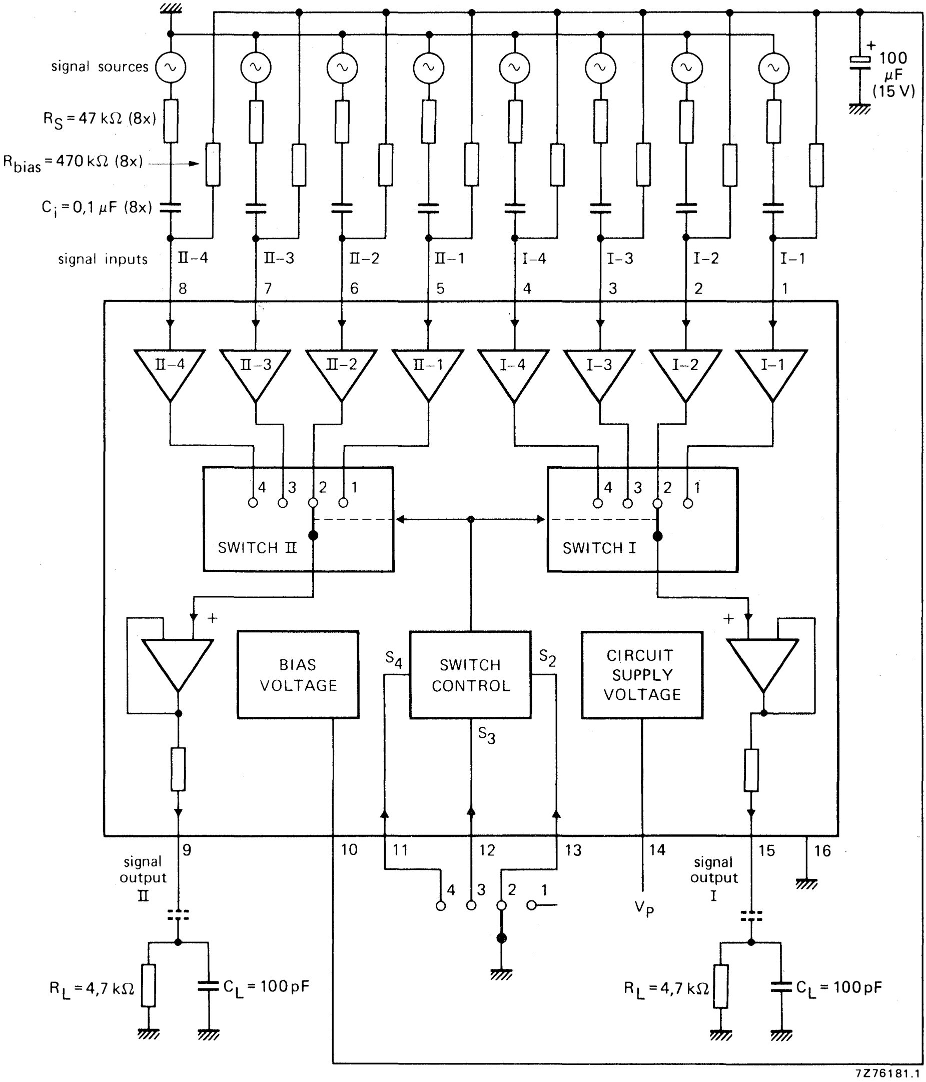


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I $-V_I$	max. max.	V_P 0,5	 V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

$V_P = 20$ V; $T_{amb} = 25$ °C; unless otherwise specified

Current consumption without load; $I_9 = I_{15} = 0$	I_{14}	typ.	3,5 2 to 5	mA mA
Supply voltage range (pin 14)	V_P		6 to 23	V

Signal inputs

Input offset voltage of switched-on inputs $R_S \leqslant 1$ kΩ	V_{io}	typ. <	2 10	mV mV
Input offset current of switched-on inputs	I_{io}	typ. <	20 200	nA nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ. <	20 200	nA nA
Input bias current independent of switch position	I_i	typ. <	250 950	nA nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100	µV/V
Equivalent input noise voltage $R_S = 0$; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	µV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $R_S = 1$ kΩ; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at V_P = 6 to 23 V	$\pm I_9; \pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p-p)} = 1$ V; $R_S = 1$ kΩ; $R_L = 10$ MΩ; $C_L = 10$ pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{9-16}/\Delta t$; $\Delta V_{15-16}/\Delta t$ $R_L = 10$ MΩ; $C_L = 10$ pF	S	typ.	2 V/µs

Bias voltage

D.C. output voltage	V_{10-16}	typ.	11 V *
			10,2 to 11,8 V
Output resistance	R_{10-16}	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		V_{11-16}	V_{12-16}	V_{13-16}
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1{,}5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 µA
LOW (control current)	$-I_{SL}$	<	250 µA

---

* V_{10-16} is typically $0{,}5 \cdot V_{14-16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5	dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ. <	10 100	mV mV
Total harmonic distortion				
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01	%
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02	%
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03	%
Output signal handling d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 5,3	V V
Noise output voltage (unweighted) f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5	μV
Noise output voltage (weighted) f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12	μV
Amplitude response V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1	dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75	dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90	dB **

---

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

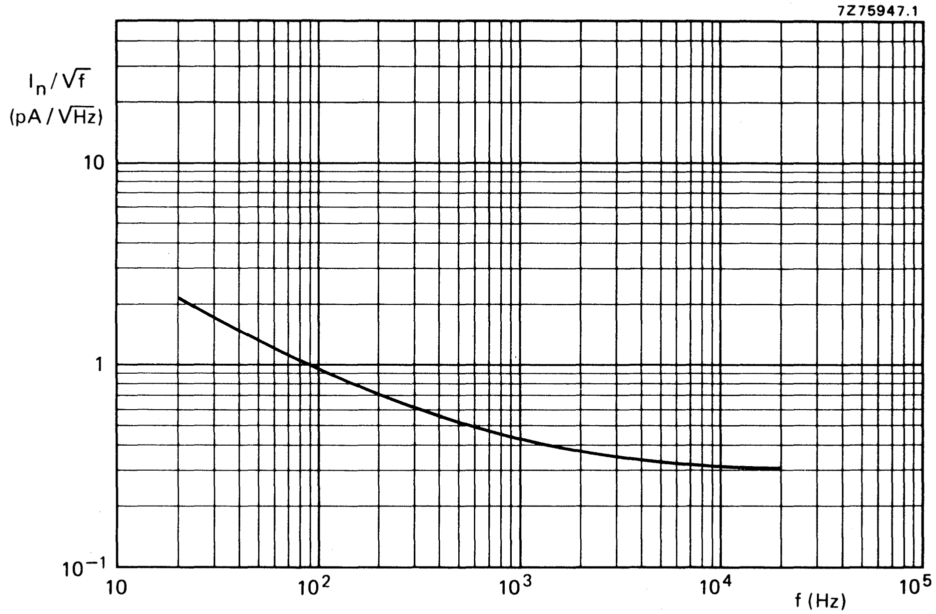


Fig. 2 Equivalent input noise current.

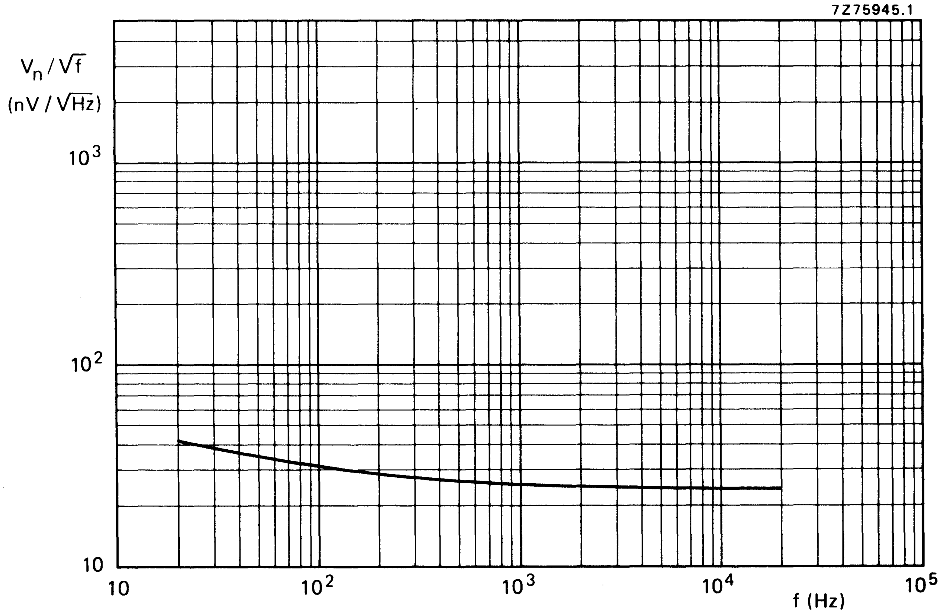


Fig. 3 Equivalent input noise voltage.

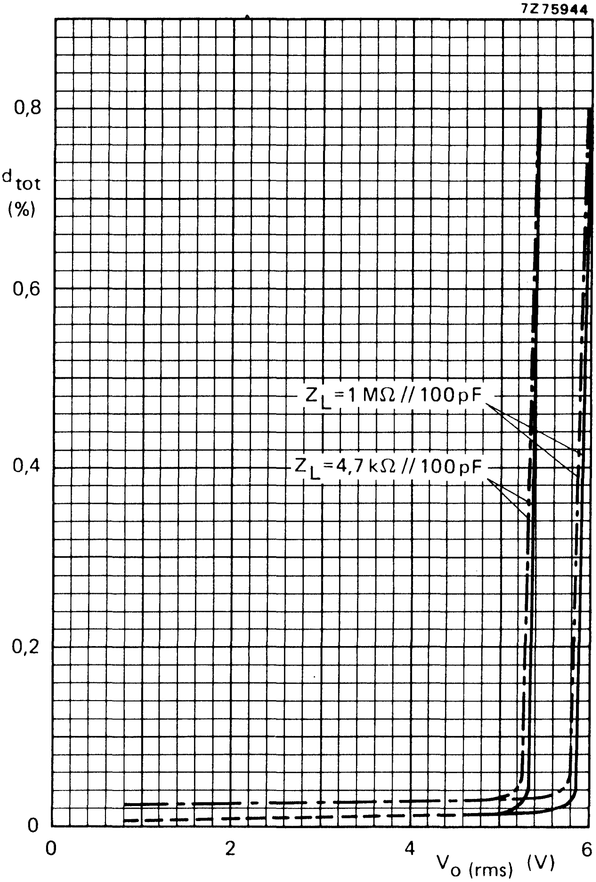


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — - — - f = 20 kHz.

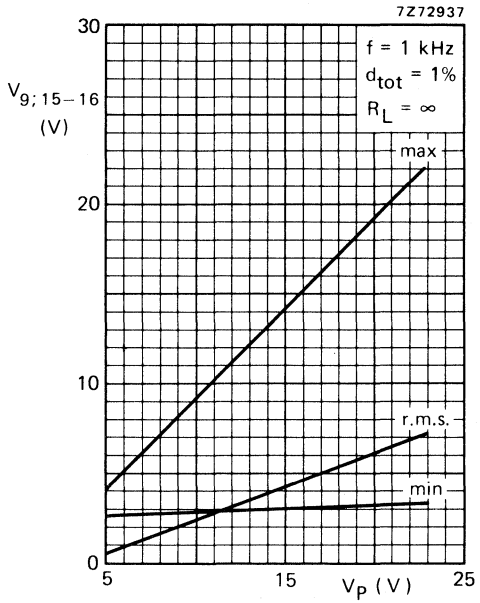


Fig. 5 Output voltage as a function of supply voltage.

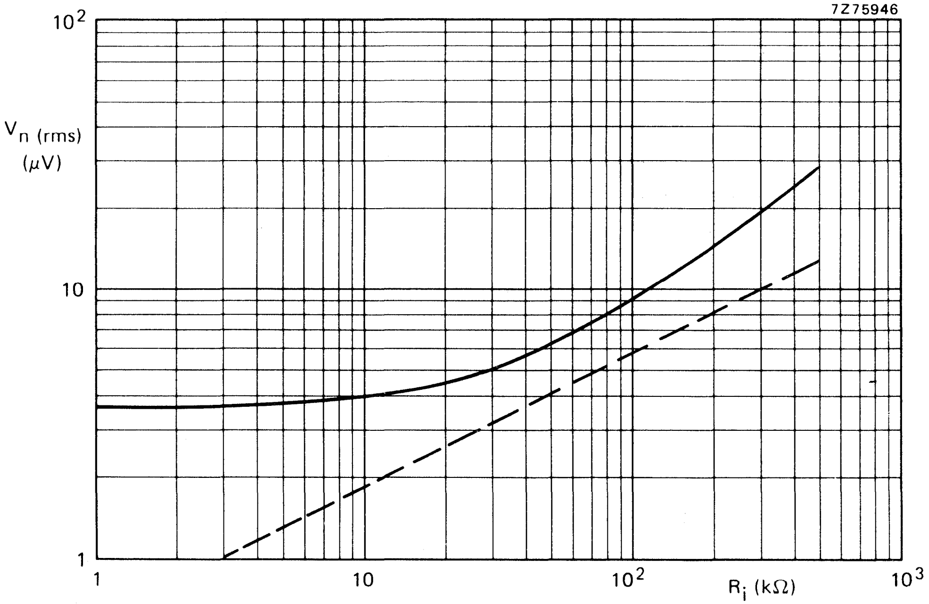


Fig. 6 Noise output voltage as a function of input resistance; $G_V = 1$; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

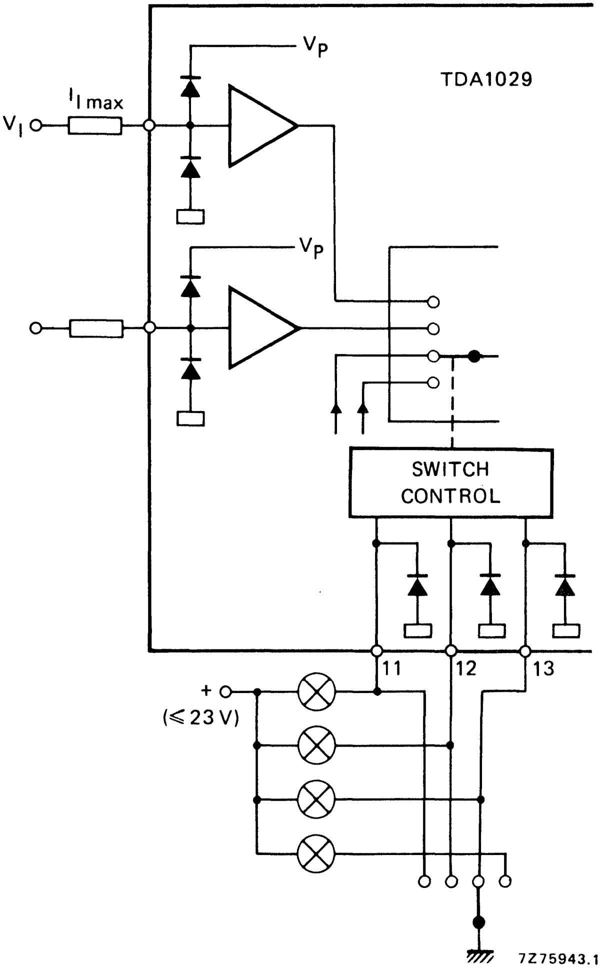


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leq 20$ V ($I_{SH} \leq 1$ μA), as well as, when the supply voltage (pin 14) is switched off.

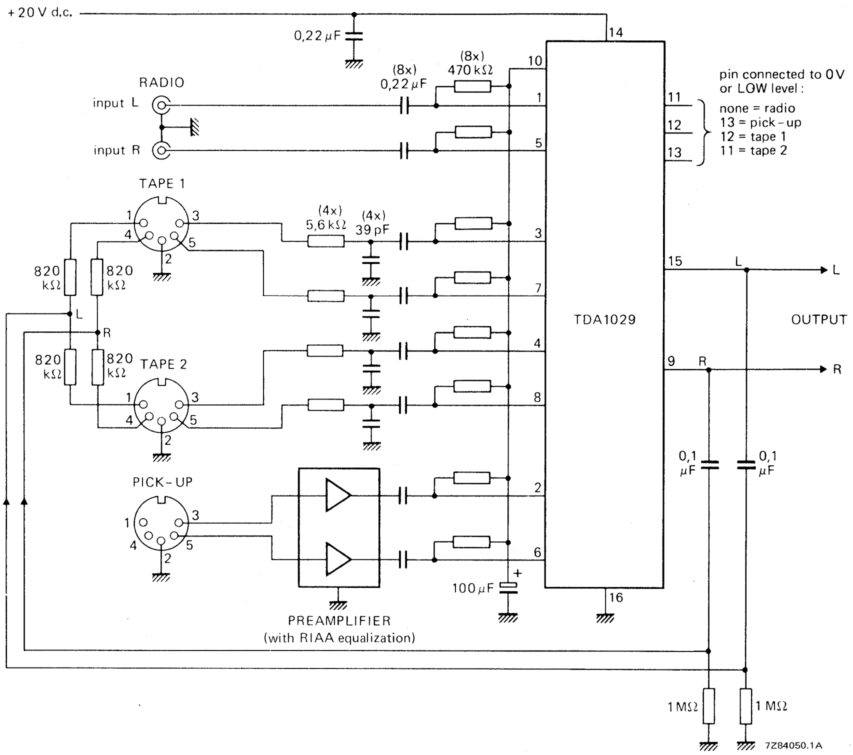


Fig. 8 TDA1029 connected as a four input stereo source selector.

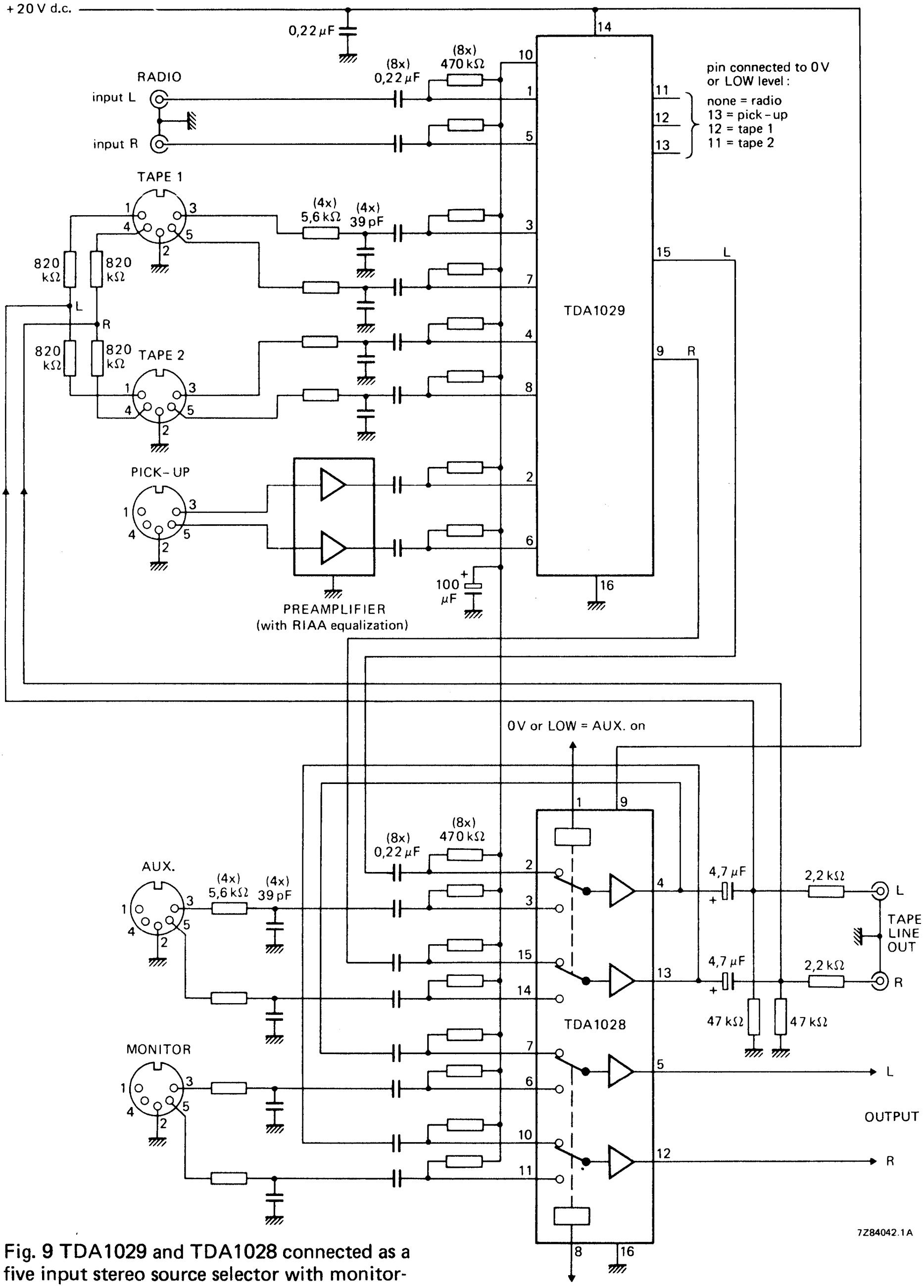


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

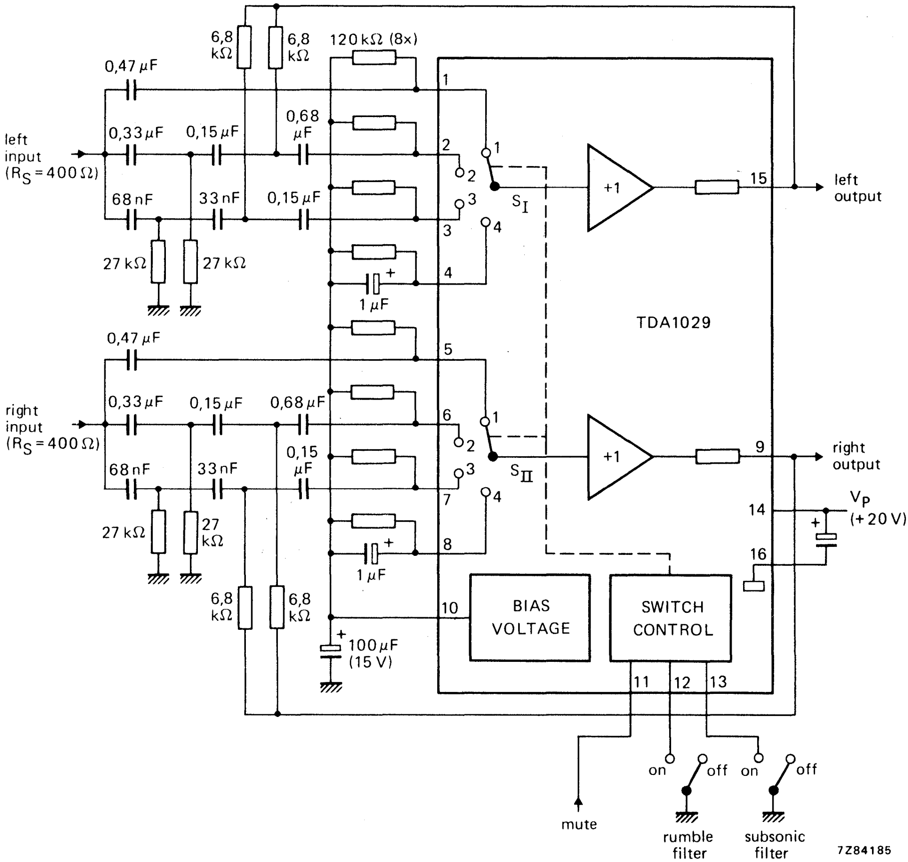


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

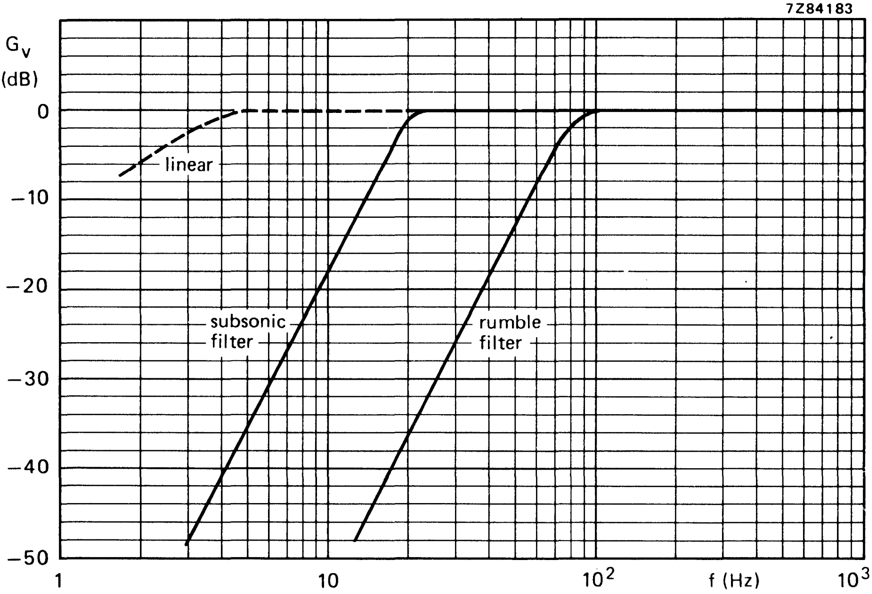


Fig. 11 Frequency response curves for the circuit of Fig. 10.

EAST-WEST CORRECTION DRIVER CIRCUIT

The TDA1082 is a monolithic integrated circuit driving east-west correction of colour tubes in television receivers. The circuit can be used for class-A and class-D operation and incorporates the following functions:

- differential input amplifier
- squaring stage
- differential output amplifier with driver stage
- protection stage with threshold
- switching off the correction during flyback
- voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 1)	V_P	typ.	12	V
Current consumption	I_P	typ.	17	mA
Total power dissipation	P_{tot}	max.	600	mW
Operating ambient temperature range	T_{amb}	−20 to	+70	°C
Collector voltage drift external transistor	ΔV_C	typ.	0,7	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

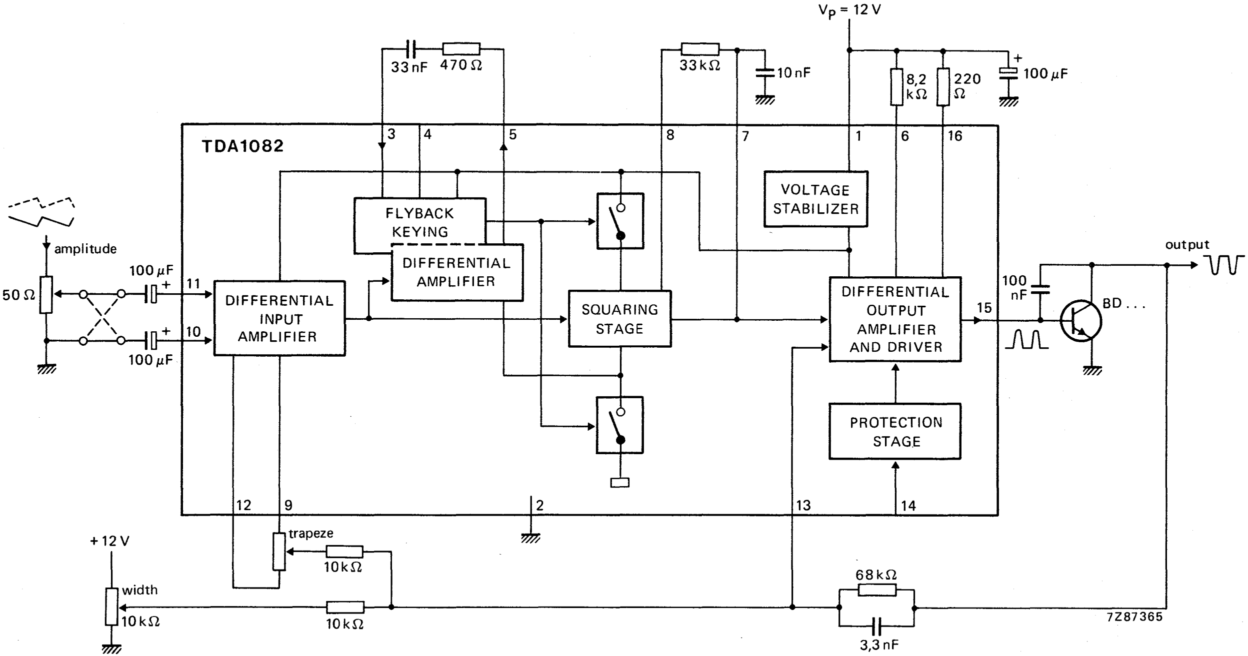


Fig. 1 Block diagram with external components (class-A operation). Also used as test circuit.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	V_P	max.	16 V
Output current (pin 15)	$-I_O$	max.	50 mA
Total power dissipation	P_{tot}	max.	600 mW
Storage temperature range	T_{stg}	−25 to +150	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

Voltages

with respect to ground (pin 2)	min.	max.
Pins 1, 5, 7, 8, 9, 12, 13 and 16	0	16 V
Pins 3 and 4	0	– V
Pins 10, 11 and 15	0	5 V

Currents

Pins 3, 4 and 6	–	5 mA
Pin 14	0	1,5 mA
Pins 15 and 16 ($-I_{15}$ and $+I_{16}$)	0	50 mA

CHARACTERISTICS

V_P = 12 V (range 10,5 to 14 V); T_{amb} = 25; measured in circuit Fig. 1 with colour tube A66-500X; unless otherwise specified

Supply

Voltage range	V_P	10,5 to	14 V
Voltage peak value	V_{PM}	max.	15 V
Current range	I_P	11 to	30 mA
Current typical value	I_P	typ.	17 mA

Sawtooth signal (pin 10 or 11)

Input voltage d.c. value	V_i	typ.	2,5 V
Input resistance	R_i	typ. <	5,6 kΩ 7,0 kΩ

Correcting signals (pin 13)

Input voltage d.c. value	V_{13}	typ.	0,6 V
Input current	I_{13}	typ.	0,5 mA

Flyback keying (pin 3)

Input current range	I_3	0,05 to	5 mA
Peak value, d = 5%	I_3	typ.	20 mA

Threshold (pin 14)

Input voltage at I_{14} = 200 μA for switching off the driver stage	V_i	typ. 7,2 to	8 V 8,8 V

Output stage (pin 6)			
Generator current	I_6	typ.	1 mA
Flyback differential amplifier (pin 5)			
D.C. value output voltage	V_5	typ.	6 V
Output resistance	R_5	typ.	5,6 kΩ
Squaring stage (pin 7)			
D.C. value output voltage	V_7	typ.	6 V
Peak to peak value output voltage	$V_{7(p\text{-}p)}$	typ.	1,5 V
Output resistance	R_7	5,6 to typ.	9,4 kΩ 7,5 kΩ
Correction trapezoidal deformation (pins 9 and 12)			
D.C. voltage	$V_{9,12}$	typ.	5 V
Output resistance	$R_{9,12}$	typ.	7,5 kΩ
Driver output (pin 15)			
Output current	$-I_{15}$	$<$	50 mA
Drift of d.c. collector voltage			
Of external transistor in closed loop T_{amb} = 15 to 70 °C; V_{CO} = 8 V	ΔV_C	typ.	0,7 V

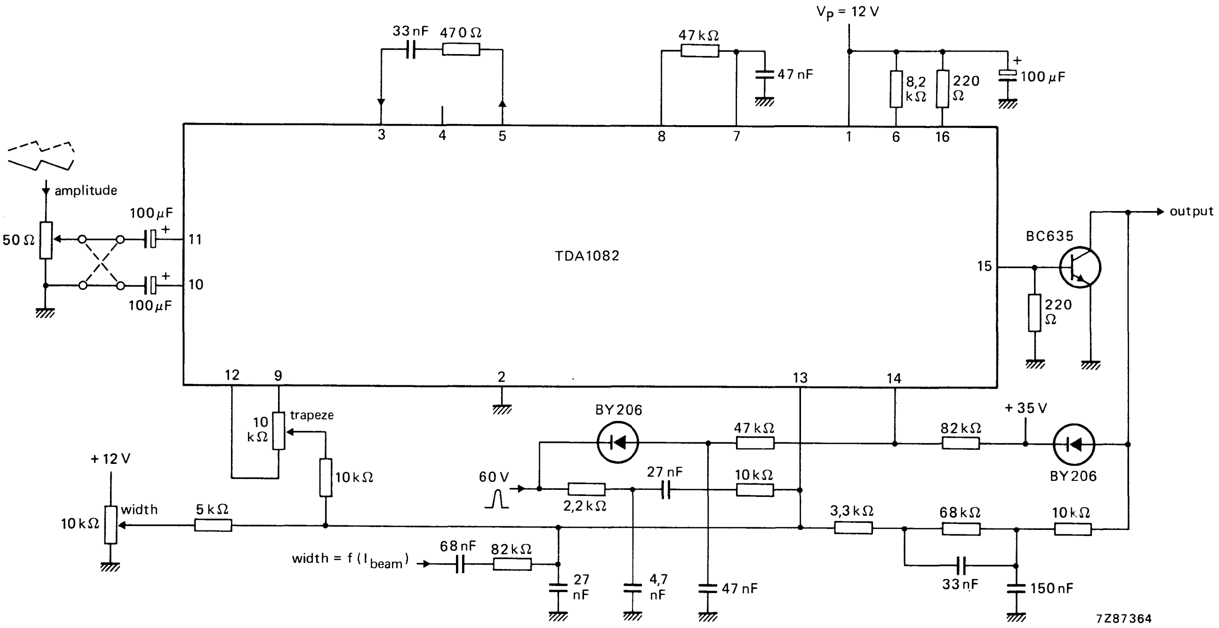


Fig. 2 Application circuit E-W-correction (class-D operation).

12 TO 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35	V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65	mA
Output power at d_{tot} = 0,7%				
sine-wave power				
V_P = 25 V; R_L = 4 Ω	P_o	typ.	13	W
V_P = 25 V; R_L = 8 Ω	P_o	typ.	7	W
music power				
V_P = 32 V; R_L = 4 Ω	P_o	typ.	21	W
V_P = 32 V; R_L = 8 Ω	P_o	typ.	12	W
Closed-loop voltage gain (externally determined)	G_c	typ.	30	dB
Input resistance (externally determined)	R_i	typ.	20	kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	72	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	50	dB

PACKAGE OUTLINES

TDA1512: 9-lead SIL; plastic power (SOT-131B).
TDA1512Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157B).

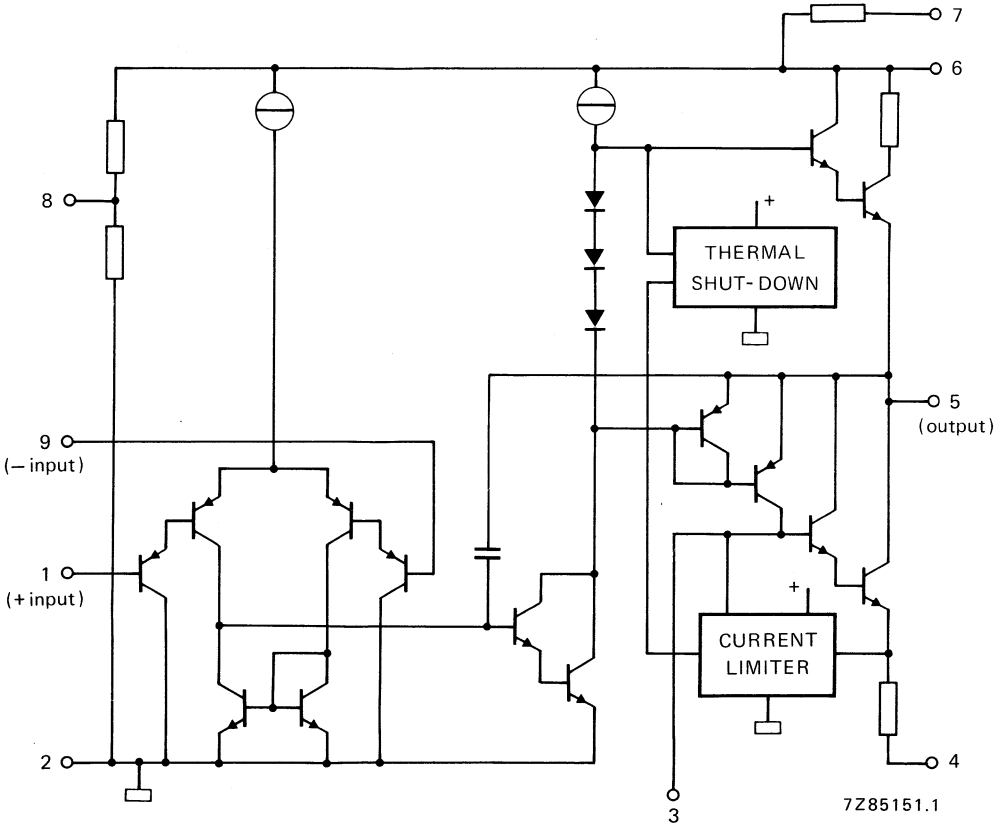


Fig. 1 Simplified internal circuit diagram.

PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Ground potential
5. Output
6. Positive supply (V_P)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35	V
Repetitive peak output current	I_{ORM}	max.	3,2	A
Non-repetitive peak output current	I_{OSM}	max.	5	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−25 to + 150	°C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100	hours

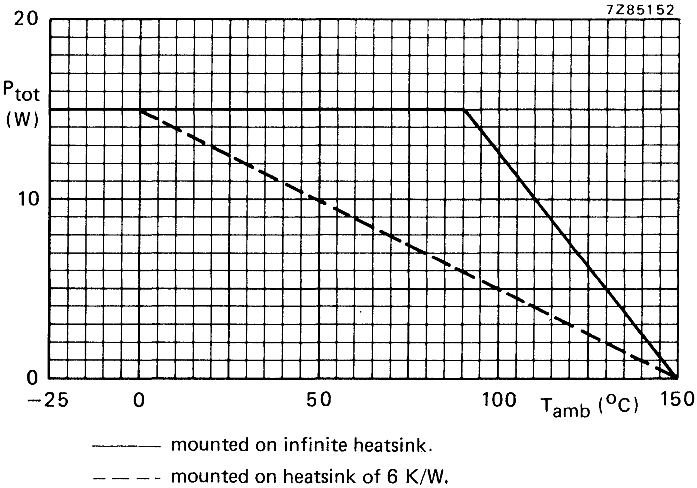


Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	typ.	3	K/W
		≤	4	K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 35	V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65	mA

A.C. CHARACTERISTICS

V_P = 25 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power				
sine-wave power at d_{tot} = 0,7 %				
R_L = 4 Ω	P_o	typ.	13	W
R_L = 8 Ω	P_o	typ.	7	W
music power at V_P = 32 V				
R_L = 4 Ω; d_{tot} = 0,7 %	P_o	typ.	21	W
R_L = 4 Ω; d_{tot} = 10 %	P_o	typ.	25	W
R_L = 8 Ω; d_{tot} = 0,7 %	P_o	typ.	12	W
R_L = 8 Ω; d_{tot} = 10 %	P_o	typ.	15	W
Power bandwidth; −1,5 dB; d_{tot} = 0,7%	B		40 Hz to 16	kHz
Voltage gain				
open-loop	G_o	typ.	74	dB
closed-loop	G_c	typ.	30	dB
Input resistance (pin 1)	R_i	>	100	kΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20	kΩ
Input sensitivity				
for P_o = 50 mW	V_i	typ.	16	mV
for P_o = 10 W	V_i	typ.	210	mV
Signal-to-noise ratio				
at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	>	68	dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	76	dB
Ripple rejection at f = 100 Hz	RR	typ.	50	dB
Total harmonic distortion at P_o = 10 W	d_{tot}	typ. <	0,1 0,3	% %
Output resistance (pin 5)	R_o	typ.	0,1	Ω

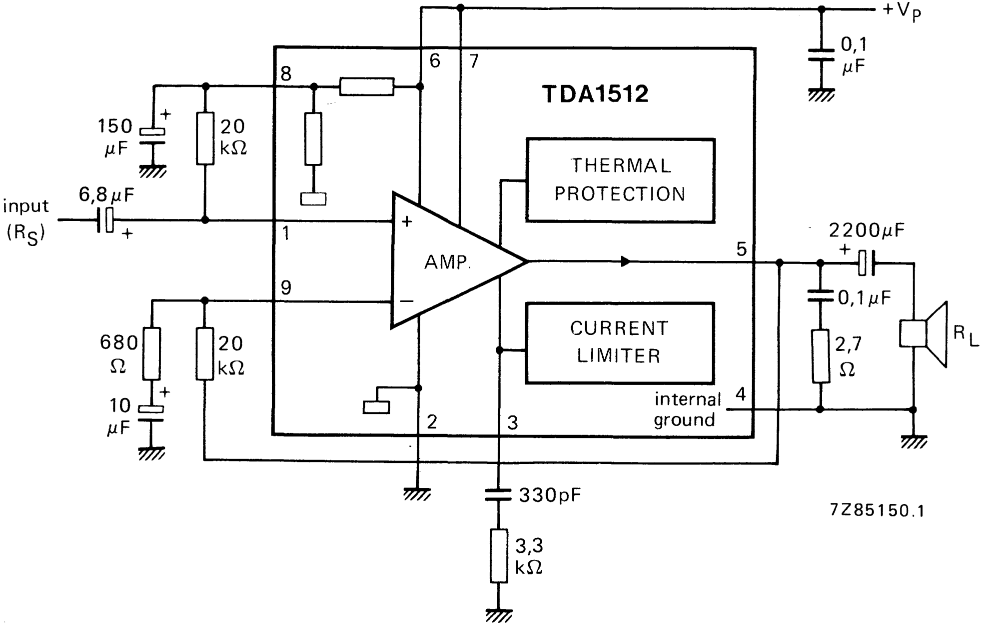


Fig. 3 Test circuit.

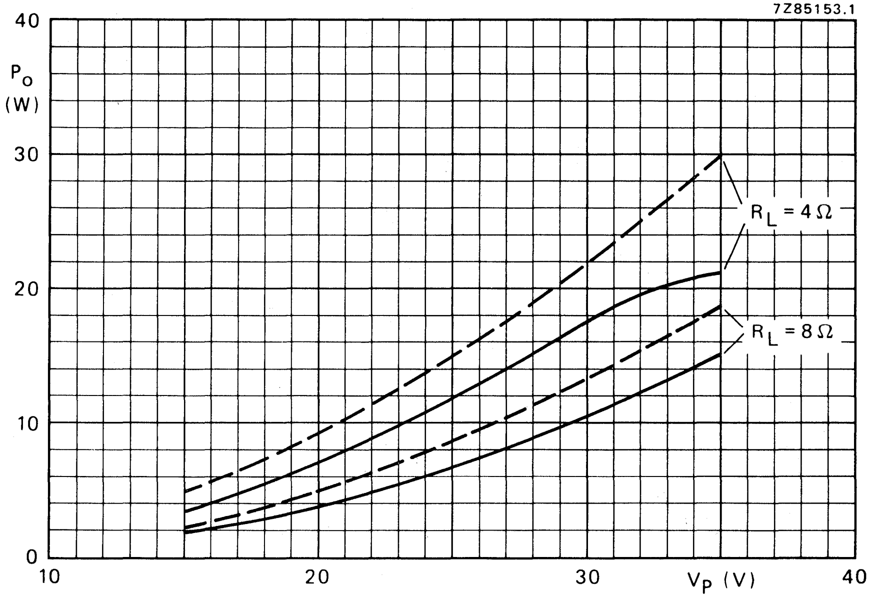


Fig. 4 Output power as a function of the supply voltage; f = 1 kHz; ——— d_{tot} = 0,7 %; – – – d_{tot} = 10 %.

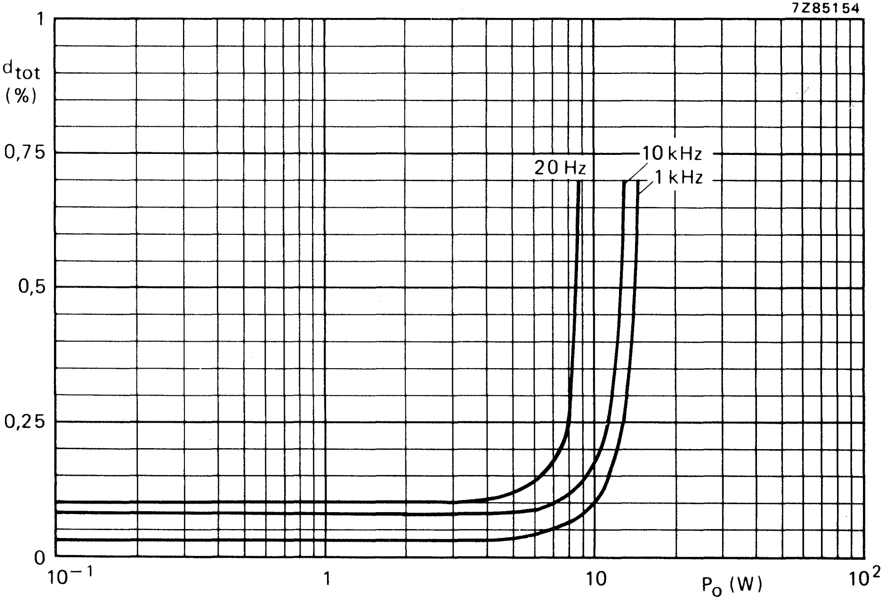


Fig. 5 Total harmonic distortion as a function of the output power.

20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1520 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 40	V
Total quiescent current at $V_P = 33$ V	I_{tot}	typ.	54	mA
Output power at $d_{tot} = 0,5\%$				
sine-wave power				
$V_P = 33$ V; $R_L = 4\ \Omega$	P_o	typ.	22	W
$V_P = 33$ V; $R_L = 4\ \Omega$	P_o	>	16	W
$V_P = 33$ V; $R_L = 8\ \Omega$	P_o	typ.	11	W
Closed-loop voltage gain (externally determined)	G_c	typ.	30	dB
Input resistance (externally determined by R_{8-1})	R_i	typ.	20	kΩ
Signal-to-noise ratio at $P_o = 50$ mW	S/N	typ.	75	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	60	dB

PACKAGE OUTLINE

TDA1520 : 9-lead SIL; plastic power (SOT-131A).
TDA1520Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157A).

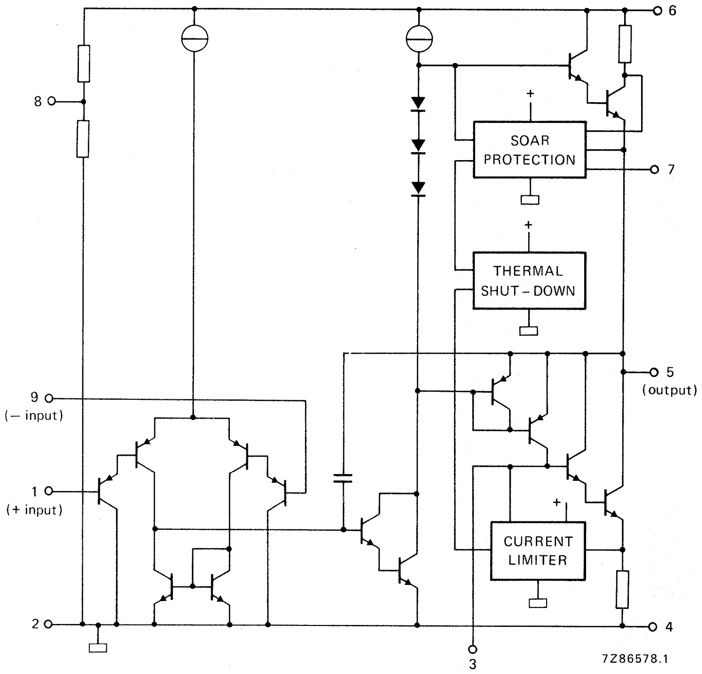


Fig. 1 Simplified internal circuit diagram.

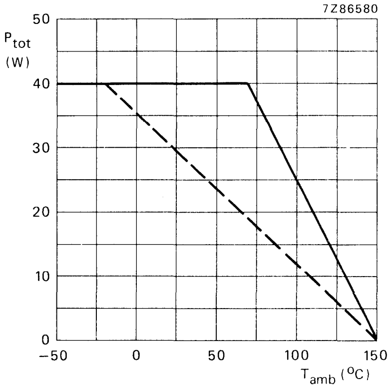
PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply (V_P)
7. Internally connected
8. Ripple rejection
9. Inverting input (feedback)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	44	V
Repetitive peak output current	I_{ORM}	max.	4	A
Non-repetitive peak output current	I_{OSM}	max.	5	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature	T_{amb}	−25 to + 150		°C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 28$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100	hours



——— mounted on infinite heatsink.
– – – mounted on heatsink of 2,3 K/W.

Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base $R_{th\ j\text{-}mb}$ ≤ 2 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 40 V
Total quiescent current at V_P = 33 V	I_{tot}		22 to 105 mA
		typ.	54 mA

A.C. CHARACTERISTICS

V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at d_{tot} = 0,5%			
R_L = 4 Ω	P_o	typ.	22 W
R_L = 4 Ω	P_o	>	16 W
R_L = 8 Ω	P_o	typ.	11 W
Power bandwidth; –3 dB; d_{tot} = 0,5%	B	20 Hz to	20 kHz
Voltage gain			
open-loop	G_o	typ.	74 dB
closed-loop	G_c	typ.	30 dB
Input resistance (pin 1)	R_i	>	1 MΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20 kΩ
Input sensitivity			
for P_o = 50 mW	V_i	typ.	16 mV
for P_o = 16 W	V_i	typ.	260 mV
Signal-to-noise ratio at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	typ.	76 dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	80 dB
Ripple rejection at f = 100 Hz	RR	typ.	70 dB
Total harmonic distortion at P_o = 16 W	d_{tot}	typ.	0,01 %
Output resistance (pin 5)	R_o	typ.	0,01 Ω
	R_o	<	0,1 Ω

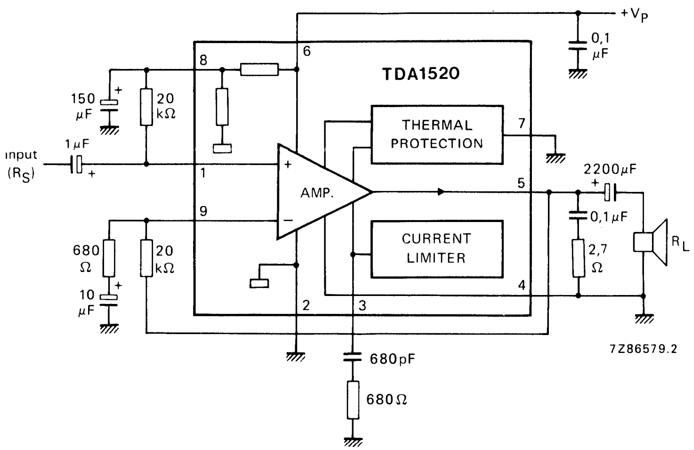


Fig. 3 Test circuit.

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

20 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1520A is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.

Features

- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected
- Very low internal thermal resistance
- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Complete SOAR protection

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 50	V
Total quiescent current at V_P = 33 V	I_{tot}	typ.	70	mA
Output power at d_{tot} = 0,5% sine-wave power				
V_P = 33 V; R_L = 4 Ω	P_o	typ.	22	W
V_P = 33 V; R_L = 4 Ω	P_o	>	20	W
V_P = 42 V; R_L = 8 Ω	P_o	typ.	20	W
Closed-loop voltage gain (externally determined)	G_c	typ.	30	dB
Input resistance (externally determined by R_{8-1})	R_i	typ.	20	kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	76	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	60	dB

PACKAGE OUTLINE

TDA1520A : 9-lead SIL; plastic power (SOT-131A).
TDA1520AQ: 9-lead SIL-bent-to-DIL; plastic power (SOT-157A).

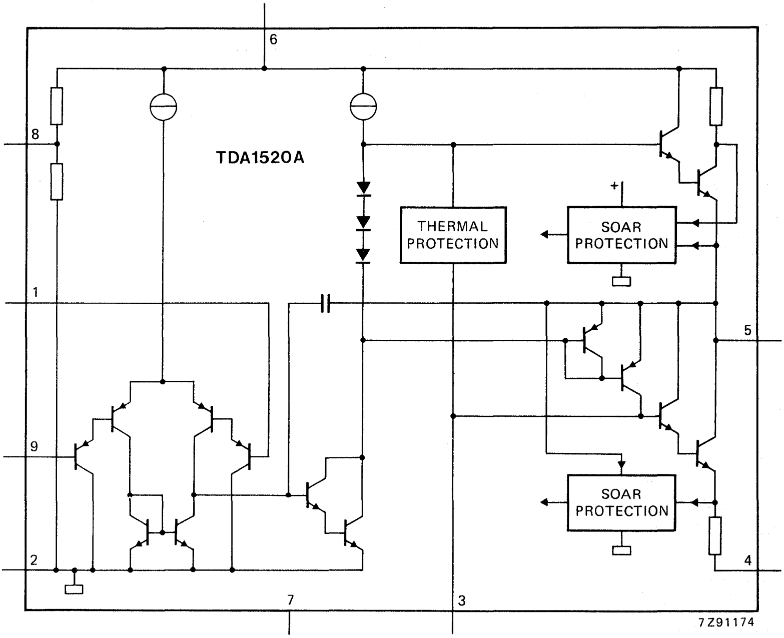


Fig. 1 Simplified internal circuit diagram.

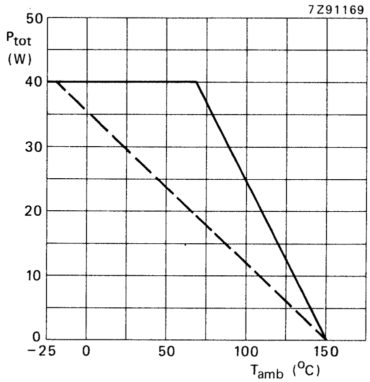
PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply (V_P)
7. Not connected
8. Ripple rejection
9. Inverting input (feedback)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	50	V
Repetitive peak output current	I_{ORM}	max.	4	A
Non-repetitive peak output current	I_{OSM}	max.	5	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to +	150	°C
Operating ambient temperature	T_{amb}	−25 to +	150	°C
Duration of a.c. short-circuit of load ($R_L = 0\ \Omega$) during full-load sine-wave drive at: $V_S = \pm 20$ V (symmetrical) and $R_{supply} = 0\ \Omega$; or $V_S = 35$ V (asymmetrical) and $R_{supply} \geqslant 4\ \Omega$	t_{sc}	max.	100	hours



——mounted on infinite heatsink.
— — —mounted on heatsink of 2,3 K/W.

Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb} \leqslant$	2	K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 50	V
Total quiescent current at V_P = 33 V	I_{tot}	typ.	70	mA
		≤	105	mA
Minimum guaranteed output current (peak value)	I_{ORM}	≥	3,2	A

A.C. CHARACTERISTICS

V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power				
sine-wave power at d_{tot} = 0,5%				
R_L = 4 Ω (Fig. 4)	P_o	typ.	22	W
R_L = 4 Ω	P_o	>	20	W
R_L = 8 Ω; V_P = 42 V	P_o	typ.	20	W
Power bandwidth at d_{tot} = 0,5% from P_o = 50 mW to 10 W	B		20 Hz to 20	kHz
Voltage gain				
open-loop	G_o	typ.	74	dB
closed-loop	G_c	typ.	30	dB
Internal resistance of pin 1 (at $R_{1\text{-}8} = \infty$)	R_i	>	1	MΩ
Input resistance of test circuit at pin 1 (Fig. 3)	R_i	typ.	20	kΩ
Input sensitivity for P_o = 16 W	V_i	typ.	260	mV
Signal-to-noise ratio at P_o = 50 mW; R_{source} = 2 kΩ				
f = 20 Hz to 20 kHz; unweighted	S/N	typ.	76	dB
weighted; measured according to IEC 179 (A-curve)	S/N	typ.	80	dB
Ripple rejection at f = 100 Hz; R_S = 0 Ω	RR	typ.	60	dB
Total harmonic distortion at P_o = 16 W	d_{tot}	typ.	0,01	%
Output resistance (pin 5)	R_o	typ.	0,01	Ω
Input offset voltage	$V_{5\text{-}8}$	typ.	1	mV
		<	100	mV
Transient intermodulation distortion at P_o = 10 W	d_{TIM}	typ.	0,01	%
Intermodulation distortion at P_o = 10 W	d_{IM}	typ.	0,01	%
Slew rate	SR	typ.	9	V/µs

APPLICATION INFORMATION

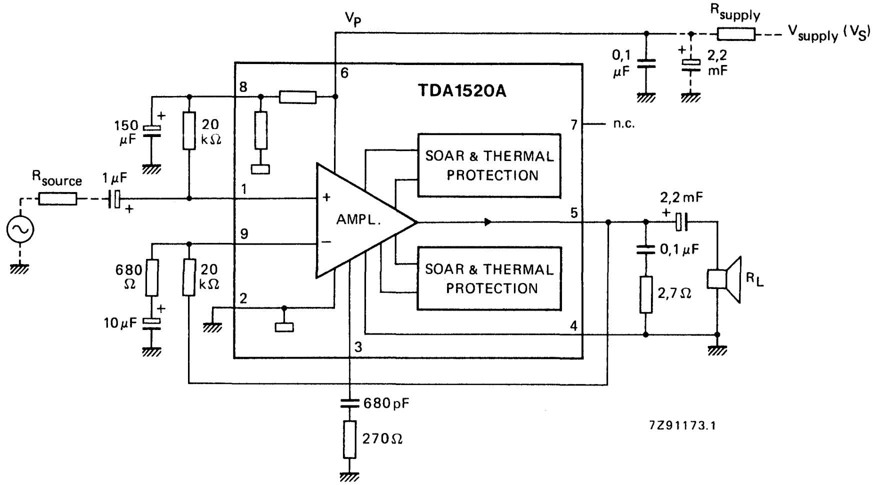


Fig. 3 Test and application circuit.

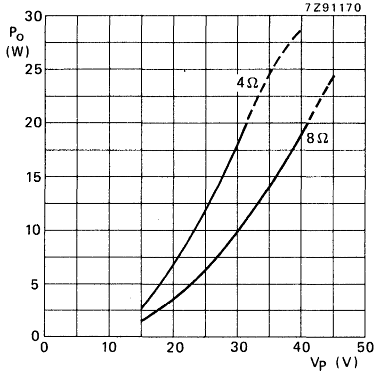


Fig. 4 Output power (P_o) versus supply voltage (V_p) at f = 1 kHz, d_{tot} = 0,5%, G_v = 30 dB.

APPLICATION INFORMATION (continued)

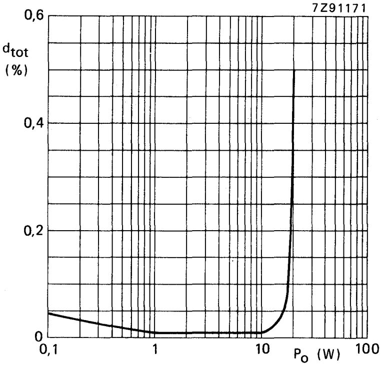


Fig. 5 Total harmonic distortion (d_{tot}) versus output power (P_o) at $V_p = 33$ V, $R_L = 4\ \Omega$, f = 1 kHz.

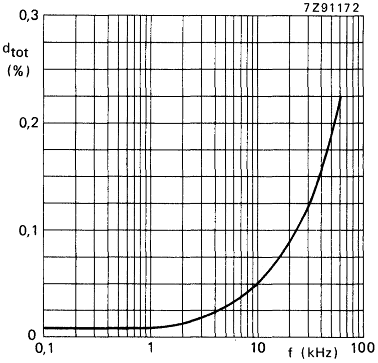


Fig. 6 Total harmonic distortion (d_{tot}) versus operating frequency (f) at $V_p = 33$ V, $R_L = 4\ \Omega$, $P_o = 10$ W (constant).

Successor type is TDA1524A

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The TDA1524 is a monolithic integrated circuit designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

Features

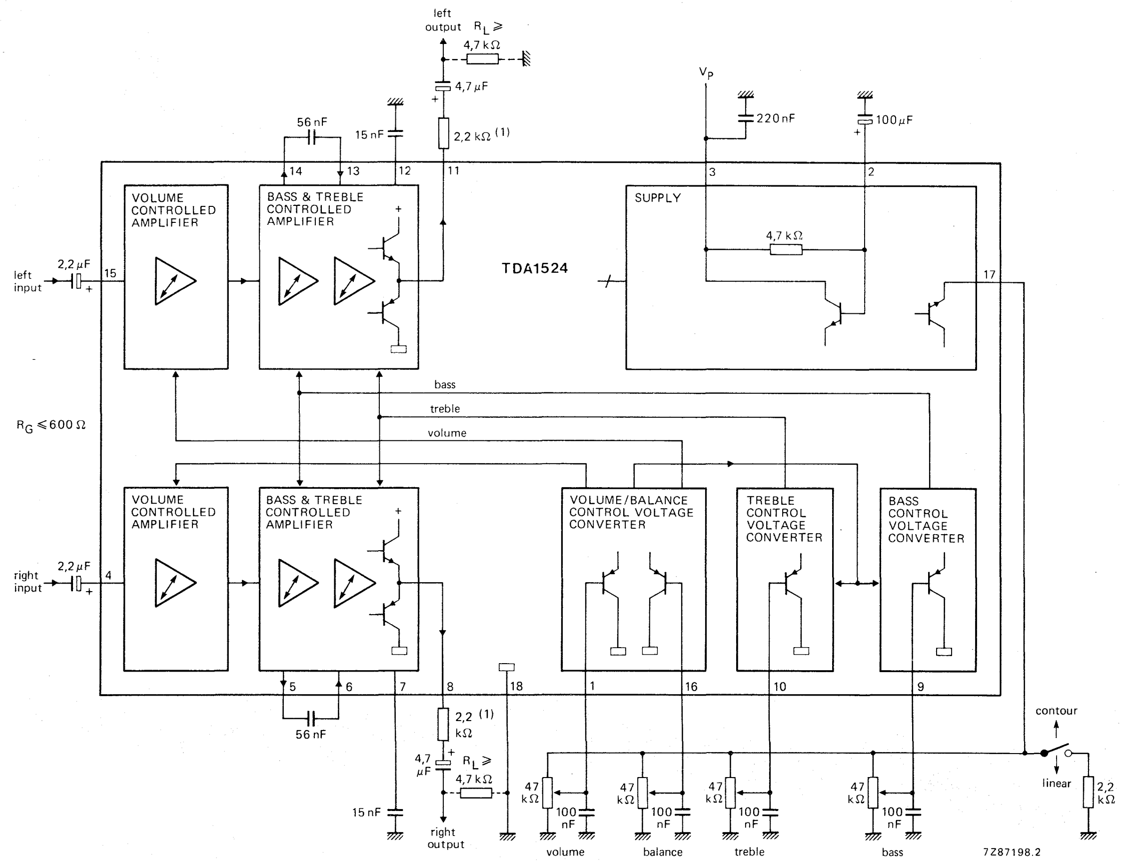
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	typ.	12	V
Supply current (pin 3)	$I_P = I_3$	typ.	35	mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2,5	V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3	V
Volume control range	G_v		−80 to + 21,5	dB
Bass control range at 40 Hz	ΔG_v	typ.	± 15	dB
Treble control range at 16 kHz	ΔG_v	typ.	± 15	dB
Total harmonic distortion	THD	typ.	0,3	%
Output noise voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz; $V_P = 12$ V;				
for max. voltage gain	$V_{no(rms)}$	typ.	310	μV
for voltage gain $G_v = -40$ dB	$V_{no(rms)}$	typ.	100	μV
Channel separation at $G_v = -20$ to $+ 21,5$ dB	α_{cs}	typ.	60	dB
Tracking between channels at $G_v = -20$ to $+ 26$ dB	ΔG_v	max.	2,5	dB
Ripple rejection at 100 Hz	RR	typ.	50	dB
Supply voltage range (pin 3)	$V_P = V_{3\text{-}18}$		7,5 to 16,5	V
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 33 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

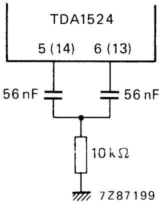


Fig. 2 Double-pole low-pass filter for improved bass-boost.

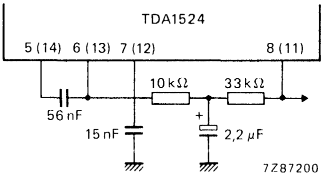


Fig. 3 D.C. feedback with filter network for improved signal handling.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	max.	20	V
Total power dissipation	P_{tot}	max.	1200	mW
Storage temperature range	T_{stg}	−55 to + 150		°C
Operating ambient temperature range	T_{amb}	−30 to + 80		°C

D.C. CHARACTERISTICS

$V_P = V_{3\text{-}18} = 12$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 30$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3\text{-}18}$	7,5	–	16,5	V
Supply current					
at $V_P = 8{,}5$ V	$I_P = I_3$	19	27	35	mA
at $V_P = 12$ V	$I_P = I_3$	25	35	45	mA
at $V_P = 15$ V	$I_P = I_3$	30	43	56	mA
D.C. input levels (pins 4 and 15)					
at $V_P = 8{,}5$ V	$V_{4,15\text{-}18}$	3,8	4,25	4,7	V
at $V_P = 12$ V	$V_{4,15\text{-}18}$	5,3	5,9	6,6	V
at $V_P = 15$ V	$V_{4,15\text{-}18}$	6,5	7,3	8,2	V
D.C. output levels (pins 8 and 11) under all control voltage conditions with d.c. feedback (Fig. 3)					
at $V_P = 8{,}5$ V	$V_{8,11\text{-}18}$	3,3	4,25	5,2	V
at $V_P = 12$ V	$V_{8,11\text{-}18}$	4,6	6,0	7,4	V
at $V_P = 15$ V	$V_{8,11\text{-}18}$	5,7	7,5	9,3	V
Pin 17					
Internal potentiometer supply voltage at $V_P = 8{,}5$ V	$V_{17\text{-}18}$	3,5	3,75	4,0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0,5	mA
linear (switch closed)	$-I_{17}$	1,5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10{,}8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	$V_{17\text{-}18}$	4,5	–	$V_P/2 - V_{BE}$	V
D.C. control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at $V_{17\text{-}18} = 5$ V	$V_{1,9,10,16}$	1,0	–	4,25	V
using internal supply	$V_{1,9,10,16}$	0,25	–	3,8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

A.C. CHARACTERISTICS

$V_P = V_{3\text{-}18} = 8,5$ V; $T_{amb} = 25$ °C; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4,7$ kΩ; $C_L \leqslant 30$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Max. gain of volume (Fig. 5)	$G_{v\ max}$	20,5	21,5	23	dB
Volume control range; $G_{v\ max}/G_{v\ min}$	ΔG_v	90	100	–	dB
Balance control range; $G_v = 0$ dB (Fig. 6)	ΔG_v	–	–40	–	dB
Bass control range at 40 Hz (Fig. 7)	ΔG_v	± 12	± 15	–	dB
Treble control range at 16 kHz (Fig. 8)	ΔG_v	± 12	± 15	–	dB
Contour characteristics		see Figs 9 and 10			
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1) at gain of volume control: $G_v = 20$ dB	$R_{i4,15}$	10	–	–	kΩ
$G_v = -40$ dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; $G_v = 0$ dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz) at $G_v = -20$ to + 21,5 dB	α_{cs}	46	60	–	dB
Spread of volume control with constant control voltage $V_{1\text{-}18} = 0,5\ V_{17\text{-}18}$	ΔG_v	–	–	± 3	dB
Gain tolerance between left and right channel $V_{16\text{-}18} = V_{1\text{-}18} = 0,5\ V_{17\text{-}18}$	$\Delta G_{v,L\text{-}R}$	–	–	1,5	dB
Tracking between channels for $G_v = 21,5$ to -26 dB f = 250 Hz to 6,3 kHz; balance adjusted at $G_v = 10$ dB	ΔG_v	–	–	2,5	dB

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with d.c. feedback (Fig. 3)					
Input signal handling (note 2)					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 8,5 V; THD = 0,7%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,8	2,4	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 12 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 15 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
Output signal handling (note 2 and note 3)					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	1,8	2,0	–	V
at V_P = 8,5 V; THD = 10%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	–	2,2	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	2,5	3,0	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	–	3,5	–	V
Noise performance (V_P = 8,5 V)					
Output noise voltage (unweighted; Fig. 15) at f = 20 Hz to 20 kHz (r.m.s. value)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	260	–	μV
for G_V = –3 dB (note 4)	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	890	–	μV
for maximum emphasis of bass and treble (contour off; G_V = –40 dB)	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 15) at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	310	–	μV
for G_V = –16 dB (note 4)	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	940	–	μV
for maximum emphasis of bass and treble (contour off; G_V = –40 dB)	$V_{no(m)}$	–	400	–	μV

parameter	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)					
Output noise voltage (unweighted; Fig. 15) at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	350	–	μV
for G_v = 16 dB (note 4)	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	980	–	μV
for maximum emphasis of bass and treble (contour off; G_v = –40 dB)	$V_{no(m)}$	–	420	–	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160\ k\Omega}{1 + G_v};\ G_{v\ max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4,5 dB to r.m.s. values.

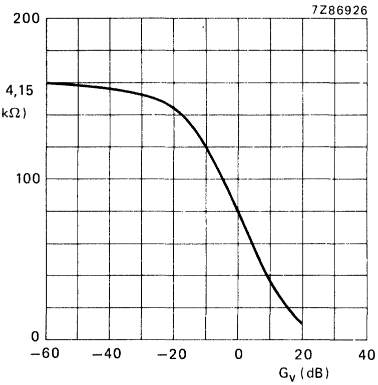


Fig. 4 Input resistance (R_i) as a function of gain of volume control (G_v). Measured in Fig. 1.

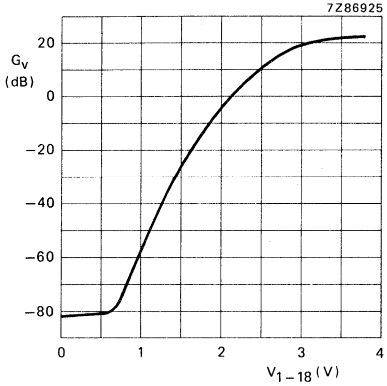


Fig. 5 Volume control curve; voltage gain (G_v) as a function of control voltage ($V_{1\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 1 kHz.

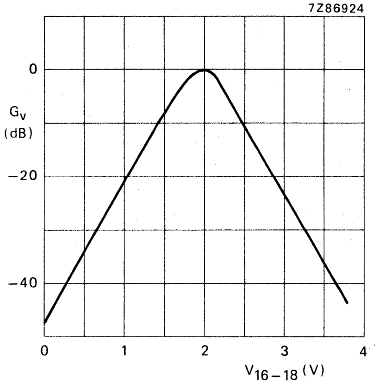


Fig. 6 Balance control curve; voltage gain (G_v) as a function of control voltage ($V_{16\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V.

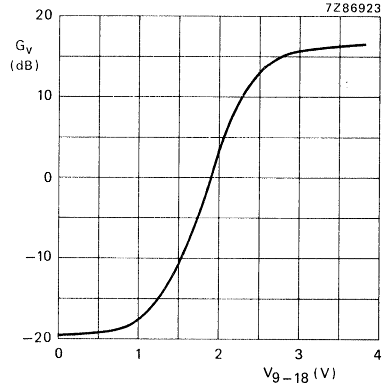


Fig. 7 Bass control curve; voltage gain (G_v) as a function of control voltage ($V_{9\text{-}18}$). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 40 Hz.

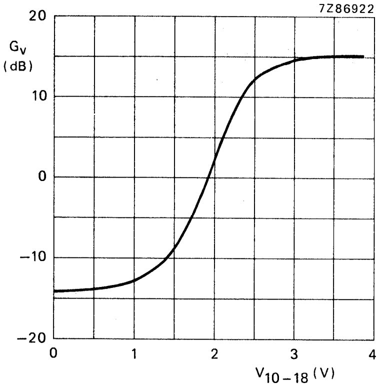


Fig. 8 Treble control curve; voltage gain (G_v) as a function of control voltage ($V_{10\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 16 kHz.

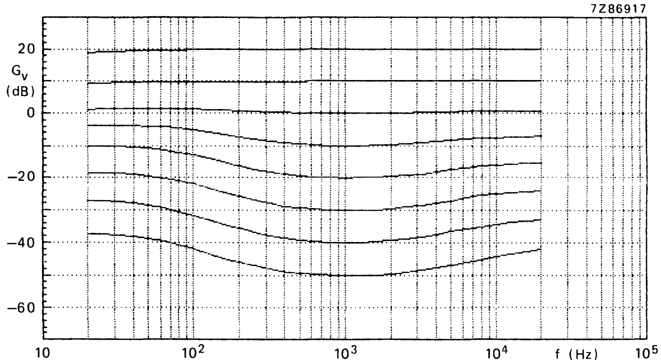


Fig. 9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

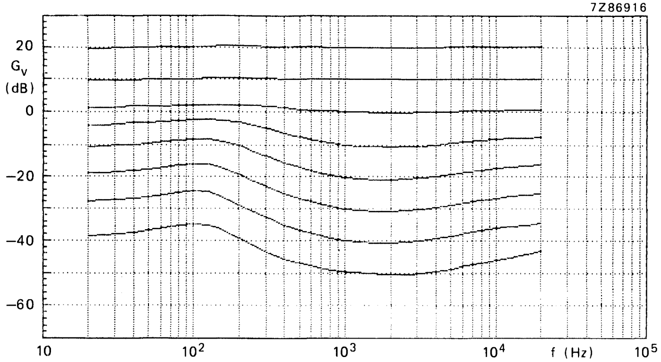


Fig. 10 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

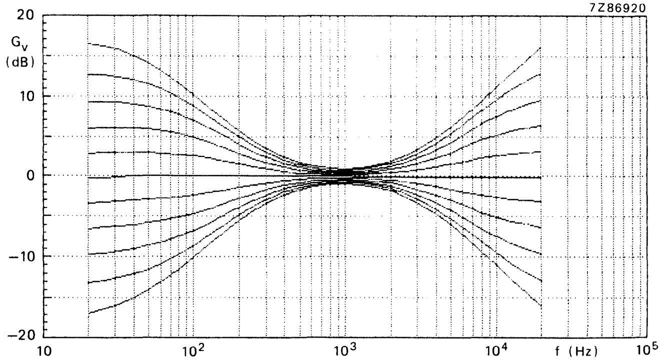


Fig. 11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

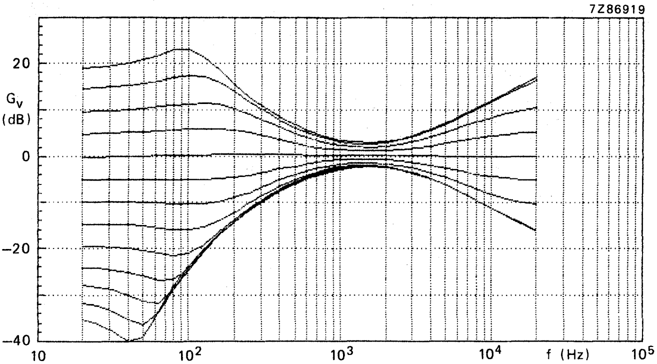


Fig. 12 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

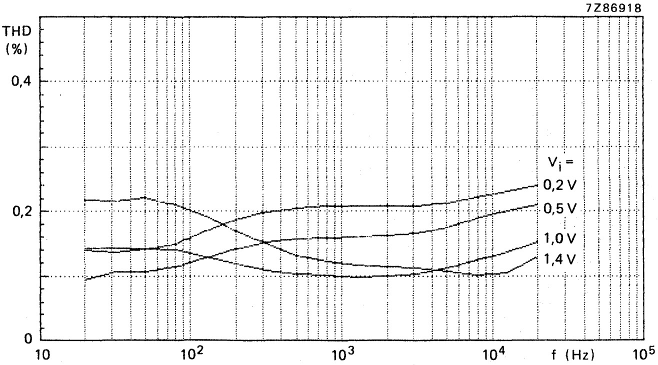


Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1; V_P = 8,5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB.}$$

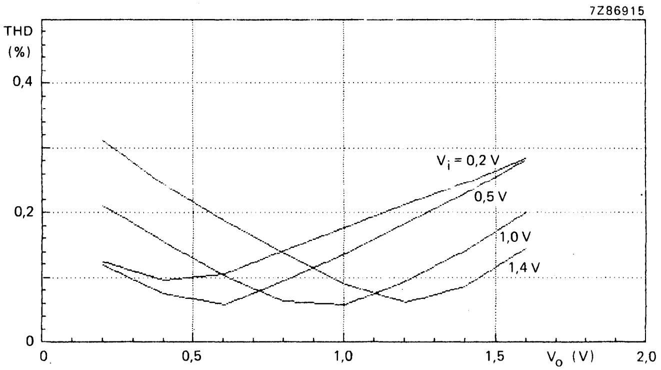
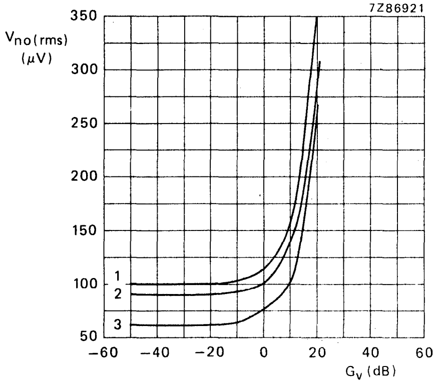


Fig. 14 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig. 1; V_P = 8,5 V; f_i = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8,5 V.

Fig. 15 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig. 1; f = 20 Hz to 20 kHz.

PAL – NTSC ENCODER

The TDA2501 encodes two colour-difference signals R-Y and B-Y onto one subcarrier. Quadrature modulation allows the coding to be in accordance with either the PAL or NTSC system.

Functions:

- Generates two sinusoidal subcarriers with a relative phase of 90° (also accepts external subcarriers)
- Modulates the two subcarriers with the colour difference signals
- Inverts the output from one modulator on command of an external signal (as in case of PAL)
- Sums the output from the modulators to obtain a quadrature modulated output signal
- Clamps the output d.c. level to a reference voltage
- Divides the frequency of horizontal sync pulses by three so that the output level can be clamped and the balance of the two modulators sequentially controlled during the line-blanking minus burst-key period

QUICK REFERENCE DATA

Supply voltage (pin 6)	V_P	typ.	6	V
Supply current	I_P	typ.	40	mA
Output chrominance voltage (pin 9)	$V_{9(p-p)}$	max.	1,4	V
Storage temperature	T_{stg}	–65 to	+150	°C
Operating ambient temperature	T_{amb}	–25 to	+70	°C

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT-38WE-2).

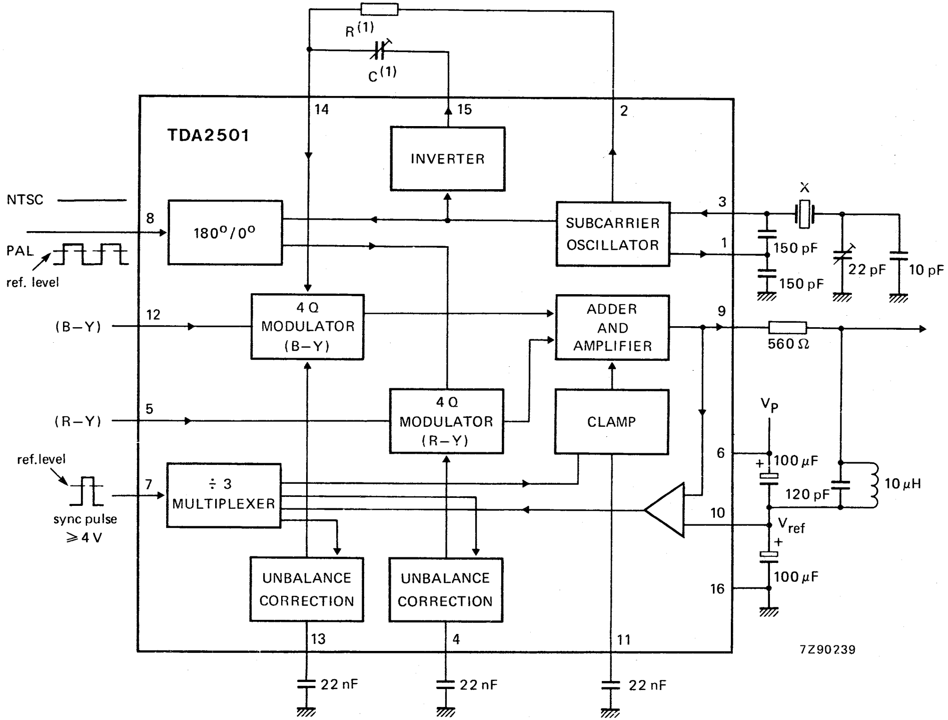


Fig. 1 Block diagram. Also test and application diagram.

(1) R = 0,885 (2 π fC); for PAL f = 4,433 619 MHz, R = 963 Ω and C = 33 pF.

DESCRIPTION

The colour difference signals B-Y and R-Y with a maximum amplitude of 1,4 volt are to be applied at pin 12 and pin 5. D.C.-coupling of the input signals is allowed if their d.c. levels are within specified limits from the d.c. level at pin 10 (V_{ref}). The following table shows these limits as a function of supply voltage. The table also shows the limits of the reference voltage range as a function of the supply voltage.

supply voltage $V_{6\text{-}16}$ (V)	input d.c. (R-Y) (B-Y) min. (V)*	$V_{5\text{-}16}$ $V_{12\text{-}16}$ (V) max. (V)*	reference voltage• $V_{10\text{-}16}$ (V)		
			min	typ.	max.
5,5	2,4	3,3	2,3	3,0	3,5
6,0	$> V_{ref} - 1,4$ V	3,8	2,4	3,3	3,9
7,0	$> V_{ref} - 1,4$ V	4,8	2,6	4,0	4,7
8,0	$> V_{ref} - 1,4$ V	5,8	2,8	4,8	5,5
9,0	$> V_{ref} - 1,4$ V	6,8	3,0	5,5	6,3
10,0	$> V_{ref} - 1,4$ V	7,8	3,2	6,3	7,1

* Minimum 2,4 V.

** At $V_S - 2,2$ V.

• Minimum values at $0,2\,V_S + 1,2$ V.
Typical values without pull-up or pull-down resistor.
Maximum values at $0,8\,V_S - 0,9$ V.

The inputs (B-Y) and (R-Y) should be zero, independent of their (limited) d.c.-levels, during the line-blanking minus burst-key period (LB – BK). Clamping the output and correcting the out-of-balance of the modulators, is done by applying a HIGH level to pin 7 within the (LB – BK) period (e.g. line sync pulse).

Modulation at output:
V_8 = LOW; output = sc x (B-Y) + sc′ x (R-Y)
V_8 = HIGH; output = sc x (B-Y) – sc′ x (R-Y)
in which sc′ = subcarrier
sc = 90° phase-shifted subcarrier to sc′ (sc lags).

The bandpass filter at the output suppresses the d.c. components of the (R-Y) + (B-Y) signal. Luminance (Y) is not processed by this circuit.

Internal subcarrier

The internal subcarrier oscillator is crystal controlled. The oscillator generates a sinewave with low harmonic distortion and an amplitude of about 500 mV peak-to-peak. The amplitude can be changed if necessary with a current input at pin 1. The adjustment range is 0 to 800 mV, with a corresponding current range of +250 to −150 μA.

Phase shift

To obtain a 90° phase-shifted carrier, two low impedance subcarrier outputs are provided, pins 2 and 15, the last being the inverse of the first. Between pins 2 and 15 an external RC combination must be used to obtain the desired 90° shift. The capacitor value must be limited to 33 pF to minimize subcarrier distortion.

The resistor required between pins 2 and 14 is 0,885 ($2\pi fC$).

External subcarrier

The (B-Y) and (R-Y) signals can also be multiplied with an external subcarrier. In this case the external subcarrier is connected to pin 1. For maximum input impedance at pin 1 $V_3 = V_{16}$ ($Z_{mi} > 1400\ \Omega$). The same RC network generate the 90° phase-shifted subcarrier. For the use of an externally generated subcarrier, applied at pin 14, the d.c. level must be the same as in the case of an RC-network generated one.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage $V_{6\text{-}16}$	V_P	max.	13,2 V
Total power dissipation	see derating curve (Fig. 2)		
Storage temperature range	T_{stg}	−65 to +150	°C
Operating ambient temperature	T_{amb}	−25 to +70	°C

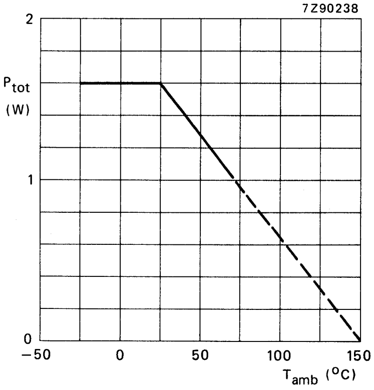


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

$V_{6\text{-}10} = -V_{16\text{-}10} = 3$ V; $T_{amb} = 25$ °C; see Fig. 1

		min.	typ.	max.	
Single power supply	$V_{6\text{-}16}$	5,5	6	10	V
Dual power supply					
positive	$V_{6\text{-}10}$	2	3	5	V
negative	$-V_{16\text{-}10}$	2,3	3	5	V
Supply current					
at pin 10	I_{10}	−1	0	3,5	mA
positive (pin 6)	I_6	28	40	64	mA
negative (pin 6)	$-I_{16}$	28	40	64	mA
Limitation d.c. level					
oscillator feedback	V_1	−30	0	+30	mV
Nominal amplitude input signal					
a.c. peak-to-peak	$V_{5(p\text{-}p)}$ $V_{12(p\text{-}p)}$	—	1	1,4	V
Input voltages (R-Y) and (B-Y)					
zero d.c. level	V_5, V_{12}	2,4	3,3	3,9	V
Required level sync input					
HIGH	V_7	4	—	V_P	V
LOW	V_7	—	—	V_{10}	V
Required level PAL pulse (H/2)					
HIGH	V_8	$V_{10} + 0{,}8$	—	V_P	V
LOW	V_8	$-V_P$	—	0	V
Input current sync input					
$V_7 = V_P + 1$ V	I_7	—	4	15	μA
Input current PAL input (H/2)					
$V_8 = V_{10} + 0{,}8$ V	I_8	—	1,5	5	μA
Output chroma voltage swing					
(R-Y) = (B-Y) = 1,4 V					
subcarrier pulse = 0,5 V	$V_{9(p\text{-}p)}$	—	—	1,4	V
Amplitude of suppressed					
subcarrier	V_9	0	7	16	mV
Input currents					
$V_4 = V_{10}$	I_4	0	1,5	5	μA
$V_{11} = V_{10}$	I_{11}	0	1,5	5	μA
$V_{13} = V_{10}$	I_{13}	0	1,5	5	μA
$V_5 = V_{10}$	I_5	0	9	30	μA
$V_{12} = V_{10}$	I_{12}	0	9	30	μA
$V_{14} = V_{16} + 2{,}3$ V	I_{14}	—	6	—	μA
Input impedance (R-Y)	Z_5	—	160	—	kΩ
Input impedance (B-Y)	Z_{12}	—	160	—	kΩ

TACHO MOTOR SPEED CONTROLLER

GENERAL DESCRIPTION

The TDA2502 is a tacho motor speed controller for the head drive in video recorders. The device provides motor speed control plus service signals for internal and external controls as two separate functions.

QUICK REFERENCE DATA

Supply voltage range (pin 12)	$V_{CC1} = V_{12\text{-}14}$		9 to 12,5	V
Supply voltage range (pin 6)	$V_{CC2} = V_{6\text{-}14}$		V_{CC1} to 12,5	V
Supply current (pin 12)	$I_{CC1} = I_{12}$	typ.	11	mA
Supply current (pin 6)	$I_{CC2} = I_6$	typ.	5	mA
Tacho input current (pin 17)	I_{17}	typ.	30	nA
Phase lock input (pin 1)				
LOW	V_{iL}	max.	4,8	V
HIGH	V_{iH}	min.	5,3	V
Phase reference input (pin 18)				
LOW	V_{iL}	max.	4,8	V
HIGH	V_{iH}	min.	5,3	V
Motor stop input (pin 4)	$V_{4\text{-}14}$	max.	0,5	V
Current limiting input (pin 8)	$V_{8\text{-}14}$	min.	0,42	V
Motor drive output (pin 5)				
at $-I_o = 10$ mA	V_{oH}	min.	9,15	V
at $I_o = 10$ mA	V_{oL}	max.	0,8	V
Operating ambient temperature range	T_{amb}		0 to 75	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

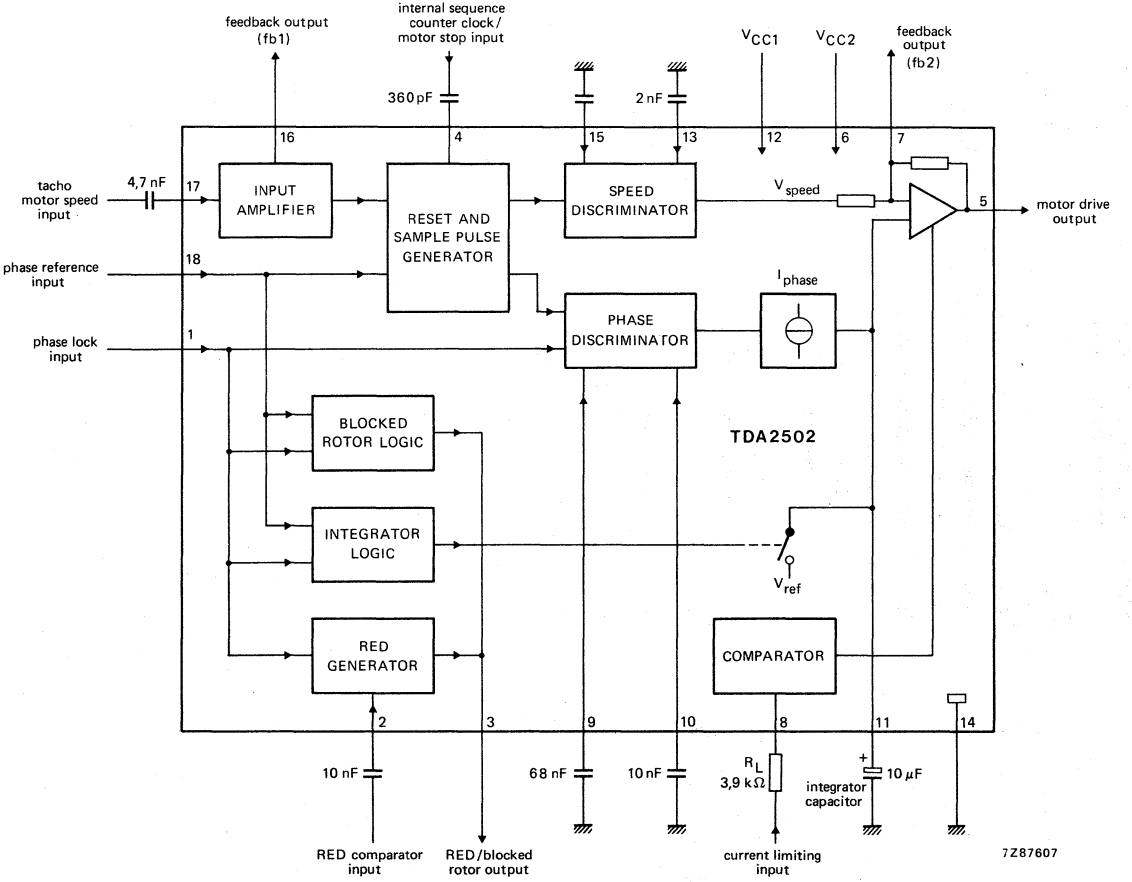


Fig. 1 Block diagram.

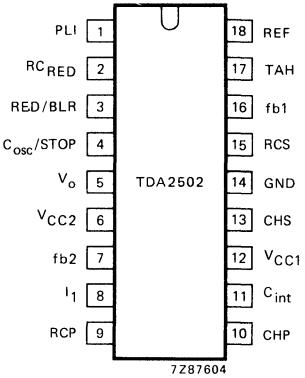


Fig. 2 Pinning diagram.

PINNING

1	PL1	phase lock input
2	RC_{RED}	RED comparator input
3	RED/BLR	RED/Blocked Rotor output
4	C_{osc}/STOP	internal sequence counter clock/motor stop input
5	V_o	motor drive output
6	V_{CC2}	positive supply 2 (output amplifier)
7	fb2	output amplifier feedback input
8	I_1	current limiting input
9	RCP	phase discriminator reset input
10	CHP	phase discriminator hold capacitor input
11	C_{int}	integrator capacitor
12	C_{CC1}	positive supply 1
13	CHS	speed discriminator hold capacitor input
14	GND	ground
15	RCS	speed discriminator reset input
16	fb1	input amplifier feedback output
17	TAH	input amplifier feedback input
18	REF	phase reference input

DEVELOPMENT SAMPLE DATA

FUNCTIONAL DESCRIPTION

Motor speed control

The d.c. motor drive output voltage (pin 5) is dependent upon both the motor speed and phase information.

The motor speed information is proportional to the tacho motor speed input frequency (pin 17) which is processed by a speed discriminator. The speed discriminator is an analogue circuit based on the sampled sawtooth principle. It is driven by reset and sample pulses at a frequency equal to the tachogenerator output frequency. Since the tachogenerator and motor are mechanically connected the circuit provides motor speed control.

The motor phase information is obtained by a comparison of the phase reference input (pin 18) and the phase lock input (pin 1).

The phase lock information is provided by a 1 pulse per revolution detector, connected to the head motor unit.

The phase information is generated by a phase discriminator. The system will reach a lock-in situation. The phase discriminator output current is integrated in an external capacitor (pin 11) after detection of the lock-in situation.

Service signals

The digital part of the circuit is responsible for:

- Aiding the RESET AND SAMPLE PULSE GENERATOR (Fig. 5)
- Reset of the integrated phase information during not-in-lock (start-up) via the INTEGRATOR LOGIC (Fig. 6)
- Generating a blocked rotor signal (BLR) which occurs after detection of 12 missing phase lock pulses by the BLOCKED ROTOR LOGIC (Fig. 1). The motor output is forced HIGH and the BLR/RED output (pin 3) is forced LOW
- RED pulse generation (Fig. 7)

Combined function

The blocked rotor signal of the head drive controller is coded in the RED output signal without affecting the C-MOS compatibility of the $\underline{\text{RED}}$ output. The blocked rotor information can be decoded by one external transistor (motor stop $\overline{\text{MS}}$, Fig. 8).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 12)	$V_{CC1} = V_{12\text{-}14}$	max.	13,2	V
Supply voltage (pin 6)	$V_{CC1} = V_{6\text{-}14}$	max.	13,2	V
Continuous output current	I_5		(see Fig. 4)	mA
Current from power supply to pins 4 and 11*	$I_{4,11}$		10	mA
Total power dissipation	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		0 to + 75	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	typ.	70	K/W

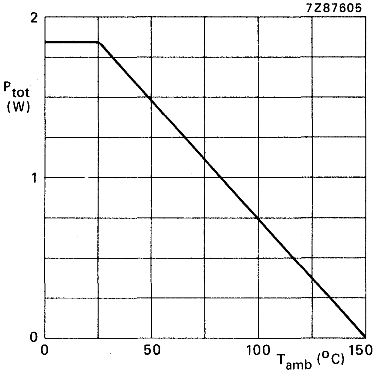
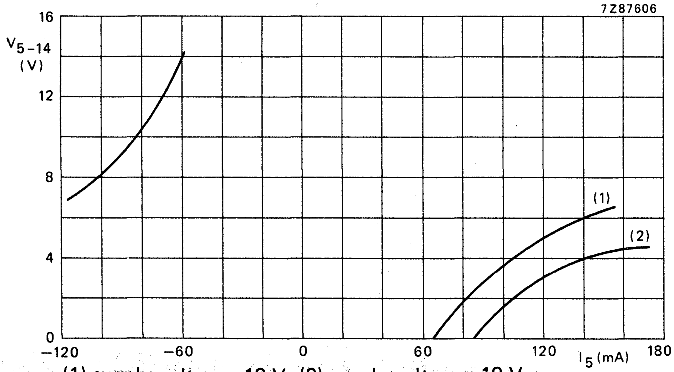


Fig. 3 Power derating curve.



(1) supply voltage = 12 V; (2) supply voltage = 10 V

Fig. 4 Maximum output current I_5 as a function of the output voltage $V_{5\text{-}14}$.

* All pins can be connected to ground or to the power supply during operation except pins 4 and 11.

CHARACTERISTICS

$V_{CC1} = V_{CC2} = 10$ V; $T_{amb} = 25$ °C; measured in Fig. 8; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 12)	$V_{CC1} = V_{12\text{-}14}$	9	10	12,5	V
Supply current (pin 12)	$I_{CC1} = I_{12}$	–	11	15	mA
Supply voltage (pin 6)	$V_{CC2} = V_{6\text{-}14}$	V_{CC1}	–	12,5	V
Supply current (pin 6) at I_o pin 5 = 0	$I_{CC2} = I_6$	–	5	–	mA
Power dissipation	P_{tot}	–	140	–	mW
Inputs					
Tacho motor speed input (pin 17)					
Input current	I_{17}	–	30	100	nA
Open loop gain (pin 17 to pin 16)	G_o	1000	–	–	V/V
Phase lock input (pin 1)					
Input voltage LOW	V_{iL}	–	–	4,8	V
Input voltage HIGH	V_{iH}	5,3	–	–	V
Input current LOW at $V_{1\text{-}14} = 0{,}5$ V	$\lvert I_{iL}\rvert$	–	–	20	µA
Input current HIGH at $V_{1\text{-}14} = 10$ V	$\lvert I_{iH}\rvert$	–	–	0,5	µA
Phase reference input (pin 18)					
Input voltage LOW	V_{iL}	–	–	4,8	V
Input voltage HIGH	V_{iH}	5,3	–	–	V
Input current LOW at $V_{18\text{-}14} = 0$ V	$\lvert I_{iL}\rvert$	–	–	5	µA
Input current HIGH at $V_{18\text{-}14} = 10$ V	$\lvert I_{iH}\rvert$	–	–	0,1	µA
Slope at $V_{18\text{-}14} = 4$ to 6 V	dV_i/dt	5	–	–	V/ms
Current limiting input (pin 8)					
Input voltage with no current limit	$V_{8\text{-}14}$	–300	–	340	mV
Input voltage with current limit	$V_{8\text{-}14}$	0,42	–	1,5	V
External load resistor to ground at $V_{8\text{-}14} = 0$ V	R_L	2	–	–	kΩ
input current LOW	$\lvert I_{iL}\rvert$	–	–	1	µA
Motor stop input (via pin 4)					
Input voltage	$V_{4\text{-}14}$	0	–	0,5	V
Input current LOW at $V_{4\text{-}14} = 0{,}5$ V	$\lvert I_{iL}\rvert$	–	–	0,5	mA

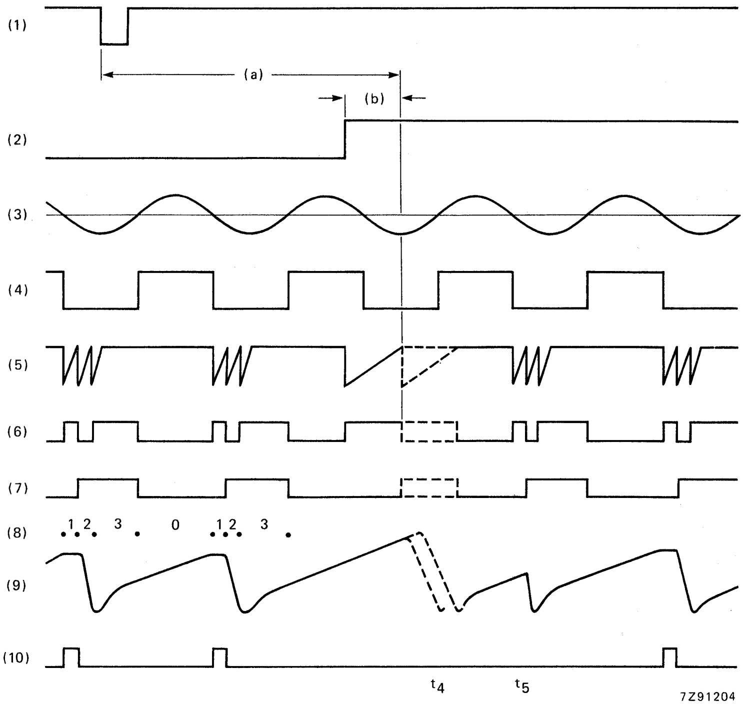
DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Outputs					
Input amplifier output (pin 16)					
Minimum voltage swing (peak-to-peak value)	$V_{16\text{-}14(p\text{-}p)}$	–	0,5	–	V
Maximum voltage swing at f = 3,5 kHz (peak-to-peak value)	$V_{16\text{-}14(p\text{-}p)}$	–	8,4	–	V
Output current at $V_{16\text{-}14}$ = 1 to 8,5 V	I_{16}	–0,5	–	0,5	mA
Output impedance	$\lvert Z_{16\text{-}14}\rvert$	–	400	–	Ω
RED/BLR output (pin 3)					
Output voltage HIGH at BLR and RED HIGH; $-I_o$ = 25 μA	V_{oH}	9	–	–	V
Output current HIGH at V_{oH} = 1,5 V	$-I_{oH}$	30	–	–	μA
Output voltage LOW at BLR HIGH; RED LOW; $-I_o$ = 5 μA	V_{oL}	1,2	–	1,6	V
Output current LOW at V_{oL} = 1,5 V	$-I_{oL}$	40	–	–	μA
Output voltage LOW at BLR LOW; I_o = 0,5 mA	$-V_{oL}$	–	–	0,5	V
Motor drive output (pin 5)					
Output voltage HIGH at $-I_o$ = 10 mA	V_{oH}	9,15	–	–	V
Output voltage LOW at I_o = 10 mA	V_{oL}	–	–	0,8	V
Output current HIGH at V_o = 0 V*	$-I_{oH}$	30	–	400	mA
Output current LOW at V_o = 10 V*	I_{oL}	10	–	300	mA
Functional connections					
Sawtooth speed discriminator (pin 15)					
Capacitor connected to pin 4 = 360 pF					
Load current	I_{15}	50	65	75	μA
Reset current at $V_{15\text{-}14}$ = 0,8 V	I_{15}	2,5	–	–	mA
Reset time	t_r	–	15	–	μs
Input current during sampling at $V_{15\text{-}14}$ = 5,5 V	$\lvert I_{15}\rvert$	–	–	300	nA
Hold capacitor (pin 13)					
Capacitor connected to pin 4 = 360 pF					
External capacitor	$G_{13\text{-}14}$	–	–	2,5	nF
Input current at $V_{13\text{-}14}$ = 6 V	I_{13}	–10	–	10	nA
Sample time	t_s	–	15	–	μs
Current during sampling	$\lvert I_{13}\rvert$	300	–	–	μA

* Pin 5 short-circuit to ground; time t_{sc} must not exceed 10 seconds.

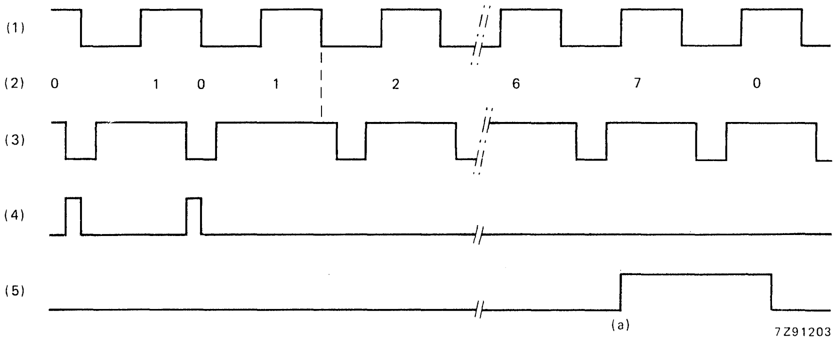
parameter	symbol	min.	typ.	max.	unit
Integrator capacitor (pin 11)					
Input impedance at pin 7 floating; in-lock	$dV_{7\text{-}14}/dI_{11}$	4	–	–	V/μA
Reference voltage; not-in-lock	V_{ref}	–	5,5	–	V
Output current not-in-lock	$\|I_o\|$	0,3	–	–	mA
$V_{10\text{-}14}$ = 1/2 supply voltage; in-lock	$\|I_o\|$	–	–	10	μA
Sawtooth phase discriminator (pin 9)					
Capacitor connected to pin 4 = 360 pF					
Reset current	I_9	0,4	–	–	mA
Reset time	t_r	–	100	150	μs
Input current	$\|I_9\|$	–	–	1	μA
Gain to pin 11; in-lock	$G_{9\text{-}11}$	17	–	23	μA/V
Hold capacitor (pin 10)					
Capacitor connected to pin 4 = 360 pF					
Input current	I_{10}	−10	–	10	nA
Sample time	t_s	–	100	150	μs
Current during sampling	$\|I_{10}\|$	300	–	–	μA
RED comparator input (pin 2)					
Reset current at $V_{1\text{-}14}$ = 0,5 V	I_2	0,6	–	–	mA
Comparator voltage level	$V_{2\text{-}14}$	4,8	–	5,4	V
Output amplifier feedback (pin 7)					
Open loop gain pin 7 to pin 5	G_o	400	1000	–	V/V
pin 15 to pin 7; pin 7 floating	G_o	19	–	23	V/V
pin 9 to pin 7; not-in-lock	G_o	1,2	–	1,5	V/V
Internal feedback resistor at pin 7	R_7	21	26	32	kΩ



Key to waveforms

(1) Phase lock input (pin 1)
(2) Phase reference input (pin 18)
  (a) sawtooth runtime for phase measurement (pin 9)
  (b) phase sample (pin 9 to pin 10)
(3) Tacho motor speed input (pin 17)
(4) Internal signal used for reset of the internal sequence counter
(5) Oscillator input (pin 4). Clocks the internal sequence counter
(6) Internal sequence counter; Q_0
(7) Internal sequence counter; Q_1
(8) Decoded functions:
  0; reset counter
  1; sample for speed discriminator
  2; reset for speed discriminator
  3; oscillator stop
(9) Result at pin 15
(10) Internal sample pulse for pin 13.
At time t_4 and t_5 the sample is suppressed by a control circuit to avoid sampling of the wrong sawtooth at pin 15 caused by the interrupt of pin 18.

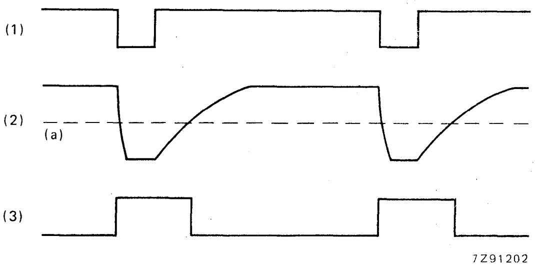
Fig. 5 Sample and reset pulse generation for speed and phase discriminators.



Key to waveforms

(1) Phase reference input (pin 18)
(2) INTEGRATOR counter
(3) Phase lock input (pin 1)
(4) Detection of "not-in-lock" if pin 1 is LOW and pin 18 is HIGH.
This condition resets the INTEGRATOR flip-flop and counter
(5) Counter condition 7 sets the INTEGRATOR flip-flop (= integration)
(a) start of integrating phase information into capacitor at pin 11.

Fig. 6 INTEGRATOR switch logic control.

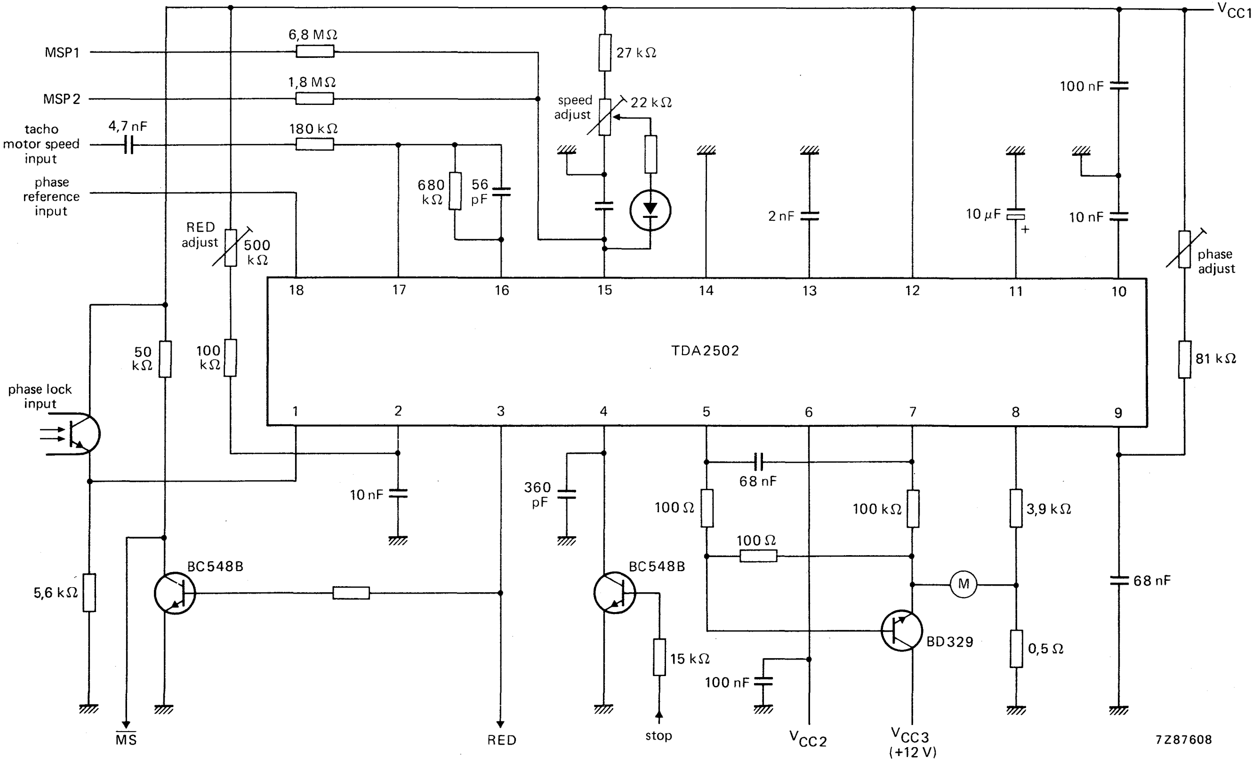


Key to waveforms

(1) Phase lock input (pin 1)
(2) RED comparator input (pin 2)
(a) 1/2 V_P
(3) RED/BLR output, if no BLR (pin 3)

Fig. 7 RED pulse generation.

APPLICATION INFORMATION



Microprocessor signals

MS: motorstop indication
RED: headswitch indication
MSP1: 1% motorspeed adjust
MSP2: 4% motorspeed adjust
stop: motorstop input

Fig. 8 Application diagram; also used as test circuit.

TRACK SENSING AMPLIFIER FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA2503 is a monolithic integrated circuit used in the servo system of video recorders. On selection of "play" (pin 10) the input signal f_1-f_4 (pin 2) is amplified then mixed with a signal f_{mix} (pin 13) from the SAA1085. The resultant mixed signal is filtered to provide mixer outputs pins 15 and 14 at a frequency of 45 kHz and 15 kHz respectively.

These two signals $V_i(f45)$ and $V_i(f_{15})$ are amplified and rectified via pins 4 and 7. A differential amplifier provides an output signal that is proportional to the difference between the two signals. This output signal is available at pin 12 via an electronic switch.

On selection of "record" a 220 kHz input signal $V_i(f_5)$ at pin 8 is amplified and rectified then sampled by an RC network connected to pin 11. The signal is fed via the electronic switch to the common output at pin 12.

Amplification of the "record-rectifier" is controlled by the d.c. level of the READ pulse input at pin 9. When "record" is selected only the applicable part of the circuit is activated.

QUICK REFERENCE DATA

Supply voltage (pin 16)	$V_P = V_{16-1}$	typ.	10	V
		max.	13,2	V
Supply current (pin 16)				
mode PLAY (V_9 and V_{10} high level)	$I_P = I_{16}$	typ.	11,5	mA
mode RECORD (V_9 and V_{10} low level)	$I_P = I_{16}$	typ.	8,5	mA
Play				
Output current mixer	$I_{14,15}$		190 to 360	µA
Amplification "mixer" part	$\Delta\lvert I_{15}-I_{14}\rvert$	typ.	120	µA
Amplification "rectifier" part				
D.C. voltage shift	ΔV_{12-1}	typ.	660	mV
Output voltage (pin 12) without input signal at V_{ref} (pin 3) = 4,2 V	V_{12-1}	typ.	3,5	V
Input voltage range (pin 13)	V_{13-1}		50 to 100	mV
Maximum input voltage (pin 2)	V_{2-1}		20	mV
Record				
Amplification "record-rectifier"				
Output voltage (pin 12) $V_{8(p-p)}$ = 200 mV; f = 220 kHz				
at V_{9-1} low level	V_{12-1}	typ.	4	V
at V_{9-1} high level	V_{12-1}	typ.	2,1	V

PACKAGE OUTLINE

16-lead DIL; plastic, with internal heat spreader (SOT-38WE-2).

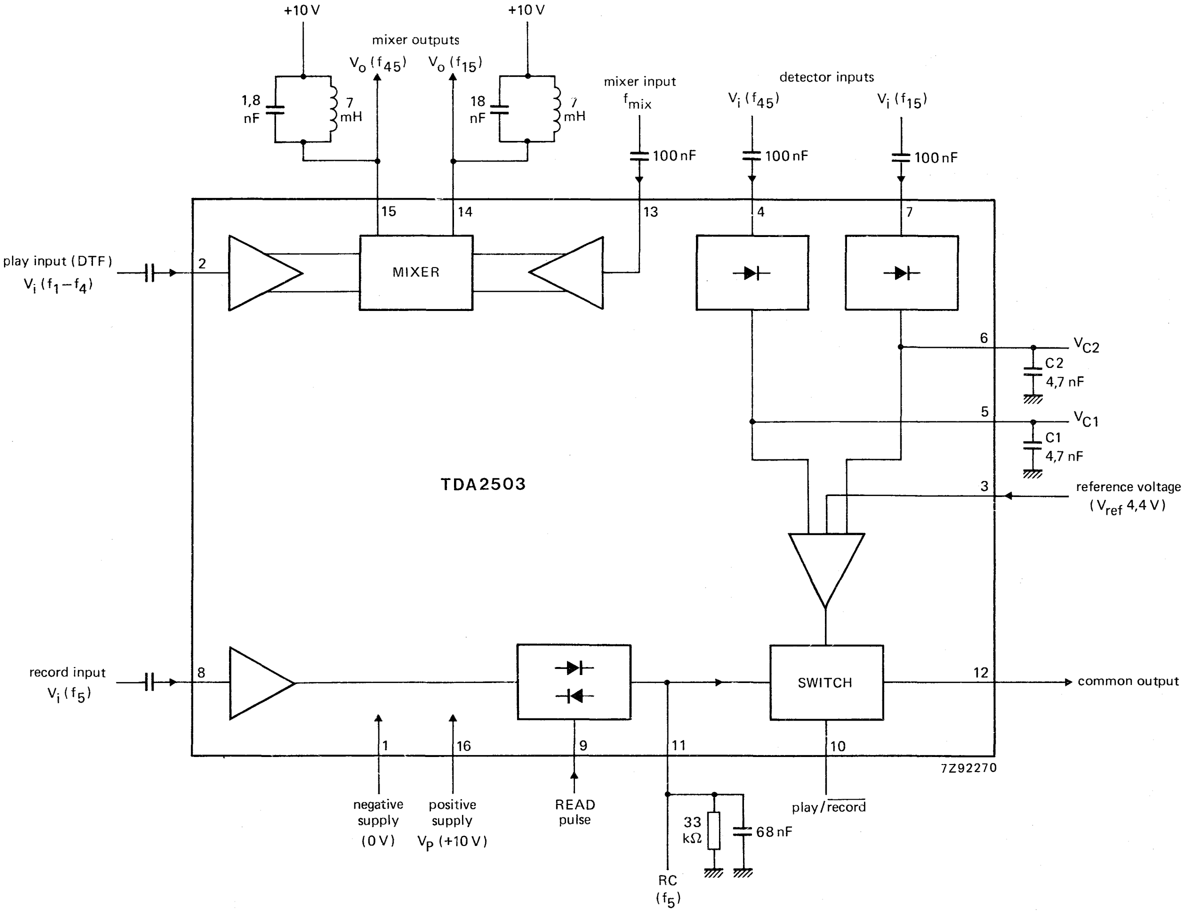


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 16)	$V_P = V_{16\text{-}1}$	max.	13,2	V
Voltages with respect to pin 1				
Input voltage all pins	$V_{n\text{-}1}$	max.	9	V
Output voltage				
pin 12	$V_{12\text{-}1}$	max.	8	V
pin 14	$V_{14\text{-}1}$	max.	13,2	V
pin 15	$V_{15\text{-}1}$	max.	13,2	V
Voltage at pin 11	$V_{11\text{-}1}$	max.	9	V
Current at pin 12	I_{12}	max.	10	mA
Total power dissipation	P_{tot}	max.	500	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	typ.	75	K/W

DEVELOPMENT SAMPLE DATA

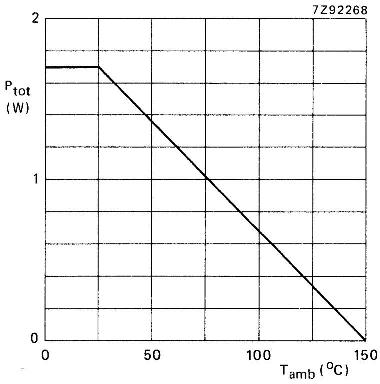


Fig. 2 Power derating curve.

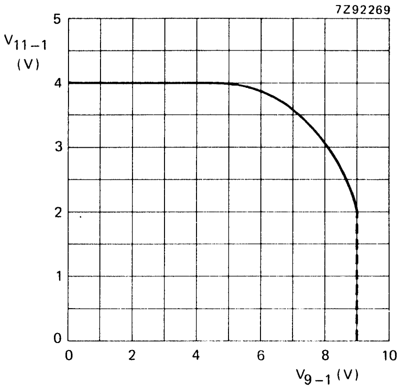


Fig. 3 Amplification of the "record-amplifier" $V_{11\text{-}1}$ as a function of input voltage $V_{9\text{-}1}$; $V_P = 10$ V; $V_{8(p\text{-}p)} = 200$ mV.

D.C. CHARACTERISTICS

$V_P = V_{16\text{-}1} = 10$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 16)	$V_P = V_{16\text{-}1}$	9	10	12,6	V
Reference voltage (pin 3)	$V_{ref} = V_{3\text{-}1}$	—	4,2	—	V
Supply current (pin 16)					
"play"; V_9 and V_{10} high level	$I_P = I_{16}$	7,5	11,3	14,8	mA
"record"; V_9 and V_{10} low level	$I_P = I_{16}$	5,6	8,5	11,2	mA
Input current					
high level; $V_{10\text{-}1} = 10$ V	I_{10}	—	—	1	μA
low level; $V_{10\text{-}1} = 0$ V	$-I_{10}$	—	—	1	μA
Input voltage (pin 10 at position "play")					
V_i (f_1-f_4)	$V_{2\text{-}1}$	3,0	3,2	3,4	V
V_i (f_5)	$V_{8\text{-}1}$	3,0	3,2	3,4	V
V_i (f_{45})	$V_{4\text{-}1}$	2,7	2,9	3,1	V
V_i (f_{15})	$V_{7\text{-}1}$	2,7	2,9	3,1	V
Input voltage (pin 10)					
position "play" = high level	$V_{10\text{-}1}$	2	—	—	V
position "record" = low level	$V_{10\text{-}1}$	—	—	0,8	V
V_{C1} (pin 10 at position "play")	$V_{5\text{-}1}$	2,7	2,9	3,1	V
V_{C2} (pin 10 at position "play")	$V_{6\text{-}1}$	2,7	2,9	3,1	V
READ pulse current (pin 9)					
$V_{9\text{-}1} = 10$ V	I_9	—	—	1	μA
$V_{9\text{-}1} = 0$ V	$-I_9$	—	—	10	μA
Mixer output current (pins 14 and 15) from + 10 V; pin 10 at position "play"					
I_o (f_{15}) pin 14)	I_{14}	190	275	360	μA
I_o (f_{45}) pin 15)	I_{15}	190	275	360	μA
Input voltage (pin 13)					
V_{fmix} (pin 10 at position "play")	$V_{13\text{-}1}$	3,0	3,2	3,4	V
V_{RC} (f_5) with $V_{9\text{-}1}$ at low level	$V_{11\text{-}1}$	—	2,1	—	V
Output voltage (pin 12)					
at V_i (f_{45}) = V_i (f_{15})	$V_{12\text{-}1}$	—	V_{ref}—0,7	—	V
at V_i (f_{45}) $\ll$ V_i (f_{15})	$V_{12\text{-}1}$	—	60	150	mV
at V_i (f_{45}) $\gg$ V_i (f_{15})	$V_{12\text{-}1}$	6,5	7,0	7,75	V
Input voltage (pin 9)					
$\overline{\text{READ}}$ = high level	$V_{9\text{-}1}$	9	—	—	V
READ = low level	$V_{9\text{-}1}$	—	—	2	V

A.C. CHARACTERISTICS

$V_P = V_{16-1} = 10$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Position "play"					
Amplification "mixer" part					
V_i (f_{1-4}) = 1 mV, 100 kHz sine					
V_{fmix} = 100 mV$_{(p-p)}$, 100 kHz square wave provides output current					
(a) square wave in phase with sine	$I_{15}-I_{14}$	–	120	–	μA
(b) square wave 180° with respect to sine	$I_{14}-I_{15}$	–	120	–	μA
(c) square wave 90° with respect to sine	$\|I_{15}-I_{14}\|$	–	0	–	μA
D.C. voltage shift*					
$\|V_{4(rms)} - V_{7(rms)}\|$ = 10 mV; f = 100 kHz	ΔV_{12-1}	560	660	760	mV
Position "record" (see also Fig. 3)					
Output voltage					
$V_{8(p-p)}$ = 200 mV; f = 220 kHz					
at V_{9-1} = high; $V_{11-1} = V_{12-1}$	V_{12-1}	–	2,1	–	V
at V_{9-1} = low; $V_{11-1} = V_{12-1}$; when $-I_{11max.}$ = 2 mA	V_{12-1}	–	4	–	V
Common mode rejection ratio (pin 12)					
at $V_{4(rms)} = V_{7(rms)}$ = 0 to 1500 mV	CMRR	20	–	–	dB
Input impedances					
dynamic track following (pin 2)	$\|Z_{2-1}\|$	6,4	8,2	11,0	kΩ
record (pin 8)	$\|Z_{8-1}\|$	6,4	8,2	11,0	kΩ
mixer (pin 13)	$\|Z_{13-1}\|$	6,4	8,2	11,0	kΩ
reference voltage (pin 3)	$\|Z_{3-1}\|$	0,1	1,0	–	MΩ
detector inputs (pins 4 and 7)	$\|Z_{4,7-1}\|$	6,4	8,2	11,0	kΩ
Input voltages					
mixer (pin 13)	V_{13-1}	50	–	100	mV
dynamic track following (pin 2) for undisturbed output signal pins 14, 15	V_{2-1}	–	–	20	mV
detector inputs (pins 4 and 7) (peak-to-peak value)	$V_{4,7-1(p-p)}$	–	–	1,5	V
record (pin 8) (peak-to-peak value)	$V_{8-1(p-p)}$	–	–	2,0	V

---

* Voltage with respect to $V_{12} = V_{ref} - 0,7$ V.

TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2540 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using n-p-n tuners.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit which can be switched on/off by a d.c. level, e.g. during tuning
- a.g.c. circuit with noise gating
- tuner a.g.c. output (n-p-n tuners)
- VCR switch, which switches off the video output; e.g. for insertion of a VCR playback signal

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}13}$	typ.	12	V
Supply current	I_{11}	typ.	50	mA
I.F. input voltage at f = 38,9 MHz (r.m.s. value)	$V_{1\text{-}16\,(rms)}$	typ.	100	μV
Video output voltage (white at 10% of top sync)	$V_{12(p\text{-}p)}$	typ.	2,7	V
I.F. voltage gain control range	G_v	typ.	64	dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58	dB
A.F.C. output voltage swing for Δf = 100 kHz	$\Delta V_{5\text{-}13}$	typ.	10	V

PACKAGE OUTLINES

TDA2540 : 16-lead DIL; plastic (SOT-38).
TDA2540Q: 16-lead QIL; plastic (SOT-58).

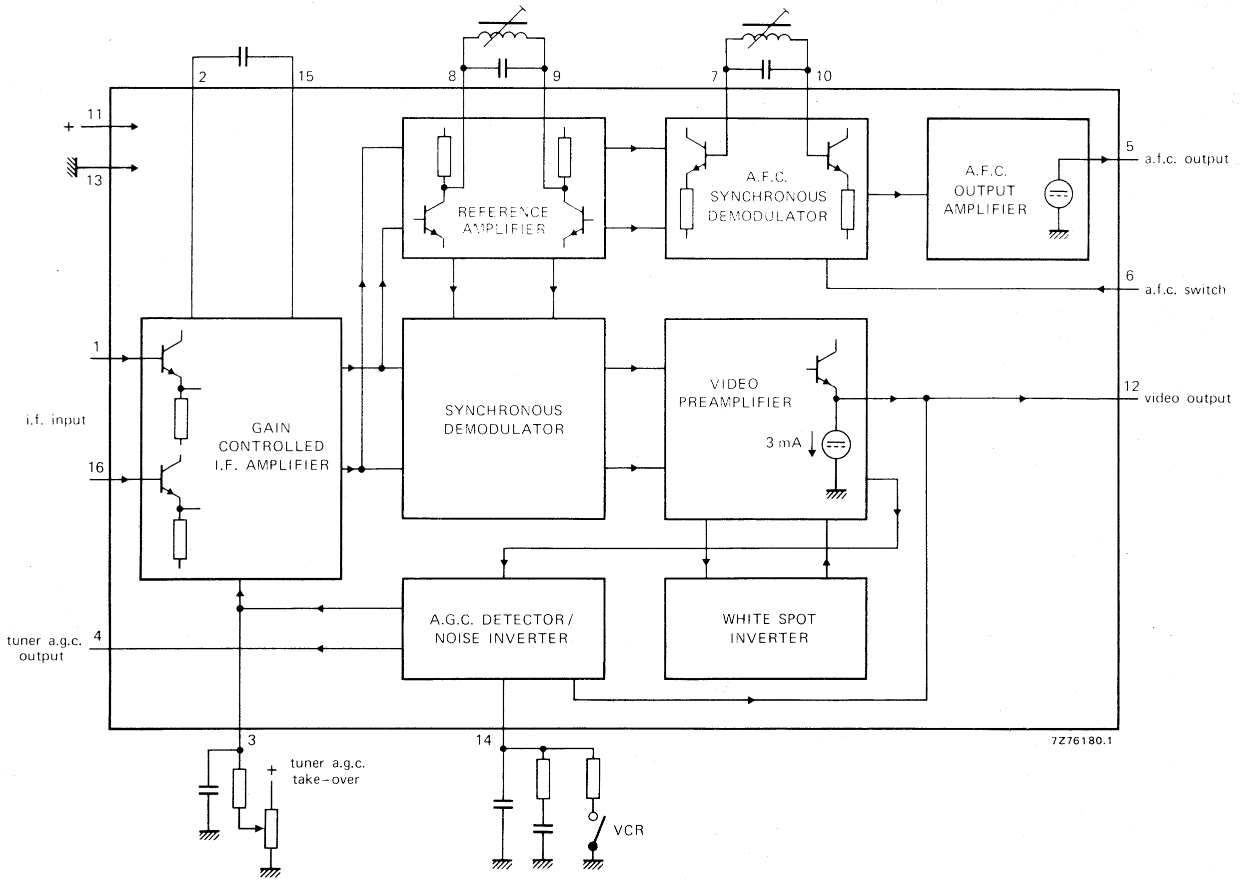


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{11\text{-}13}$	max.	13,2 V
Tuner a.g.c. voltage	$V_{4\text{-}13}$	max.	12 V
Total power dissipation	P_{tot}	max.	900 mW
Storage temperature	T_{stg}		−55 to + 125 °C
Operating ambient temperature	T_{amb}		−25 to + 60 °C

CHARACTERISTICS (measured in Fig. 5)

Supply voltage range	$V_{11\text{-}13}$	typ.	12 V
			10,2 to 13,2 V

The following characteristics are measured at $T_{amb} = 25\ ^{o}C$; $V_{11\text{-}13} = 12$ V; f = 38,9 MHz

I.F. input voltage for onset of a.g.c. (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	100 μV
		<	150 μV
Differential input impedance	$\lvert Z_{1\text{-}16} \rvert$	typ.	2 kΩ in parallel with 2 pF
Zero-signal output level	$V_{12\text{-}13}$	typ.	6 ± 0,3 V*
Top sync output level	$V_{12\text{-}13}$	typ.	3,07 V
			2,9 to 3,2 V
I.F. voltage gain control range	G_v	typ.	64 dB
Bandwidth of video amplifier (3 dB)	B	typ.	6 MHz
Signal-to-noise ratio at $V_i = 10$ mV	S/N	typ.	58 dB**
Differential gain	dG	typ.	4 %
		<	10 %
Differential phase	$d\varphi$	typ.	2°
		<	10°

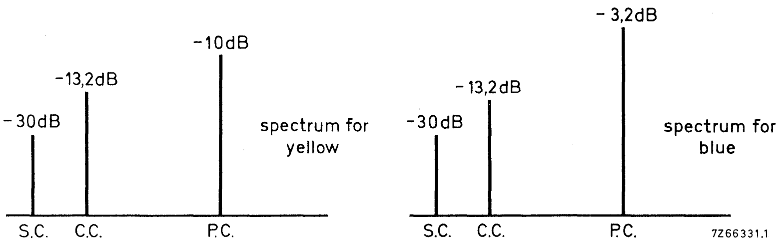
---

* So-called 'projected zero point', e.g. with switched demodulator.

$$** \ S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}} .$$

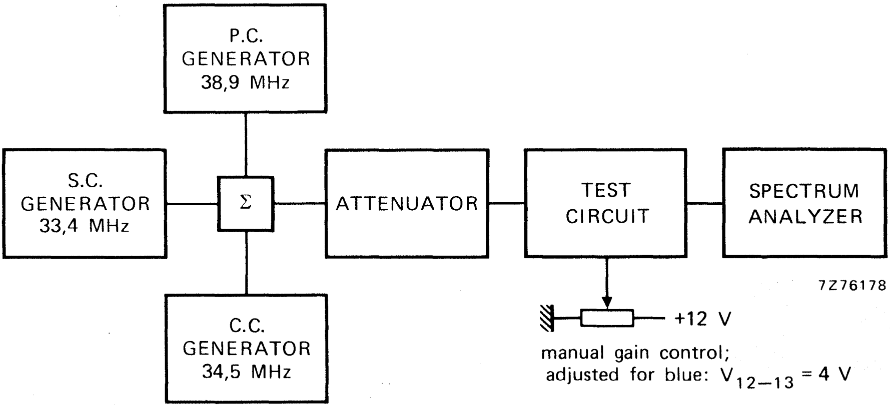
CHARACTERISTICS (continued)

Intermodulation at 1,1 MHz: blue*	>	46	dB
	typ.	60	dB
yellow*	>	46	dB
	typ.	50	dB
at 3,3 MHz**	>	46	dB
	typ.	54	dB



S.C.: sound carrier level
C.C.: chrominance carrier level
P.C.: picture carrier level
} with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.



manual gain control;
adjusted for blue: $V_{12-13} = 4$ V

Fig. 3 Test set-up for intermodulation.

* $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 1{,}1 \text{ MHz}} + 3{,}6$ dB.   ** $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 3{,}3 \text{ MHz}}$.

Carrier signal at video output		typ.	4	mV
		<	30	mV
2nd harmonic of carrier at video output		typ.	20	mV
		<	30	mV
White spot inverter threshold level (Fig. 4)		typ.	6,6	V
White spot insertion level (Fig. 4)		typ.	4,7	V
Noise inverter threshold level (Fig. 4)		typ.	1,8	V
Noise insertion level (Fig. 4)		typ.	3,8	V
External video switch (VCR) switches off the output at:	$V_{14\text{-}13}$	<	1,1	V

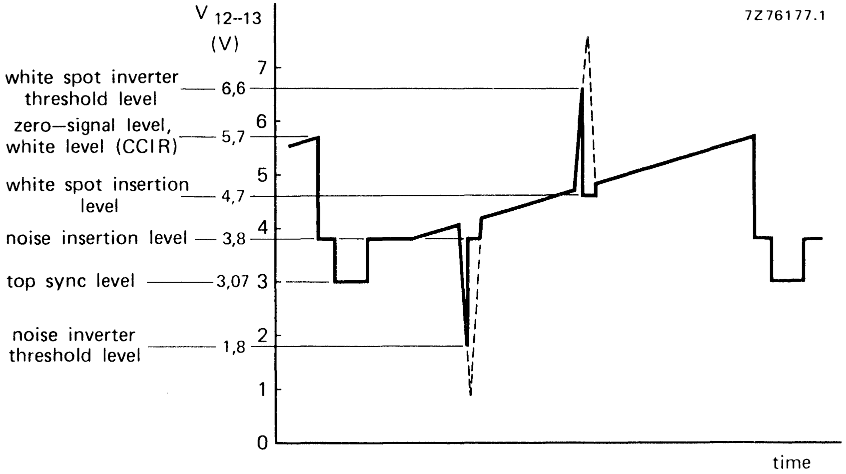


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

Tuner a.g.c. output current range	I_4		10 to 0	mA
Tuner a.g.c. output voltage at I_4 = 10 mA	$V_{4\text{-}13}$	<	0,3	V
Tuner a.g.c. output leakage current $V_{14\text{-}13}$ = 5 V; $V_{4\text{-}13}$ = 12 V	I_4	<	15	μA
Maximum a.f.c. output voltage swing	$\Delta V_{5\text{-}13}$	>	10	V
		typ.	11	V
Detuning for a.f.c. output voltage swing of 10 V	Δf	typ.	100	kHz
		<	200	kHz
A.F.C. zero-signal output voltage (minimum gain)	$V_{5\text{-}13}$	typ.	6	V
			4 to 8	V
A.F.C. switches on at:	$V_{6\text{-}13}$	>	3,2	V
A.F.C. switches off at:	$V_{6\text{-}13}$	<	1,5	V

APPLICATION INFORMATION

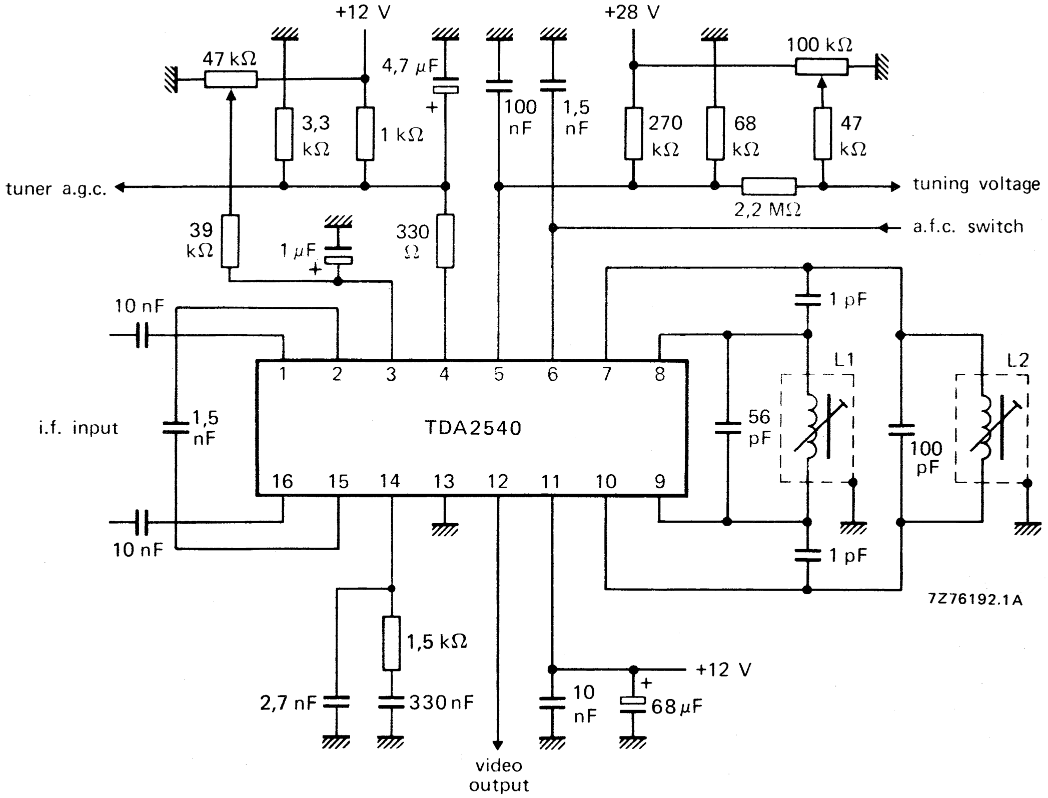


Fig. 5 Typical application circuit diagram; Q of L1 and L2 ≈ 80; f = 38,9 MHz.

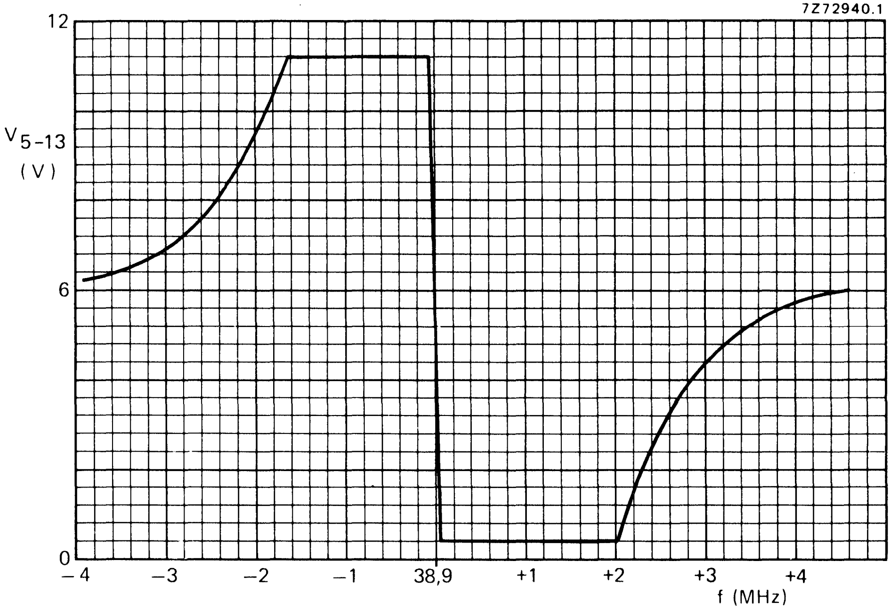


Fig. 6 A.F.C. output voltage (V_{5-13}) as a function of the frequency.

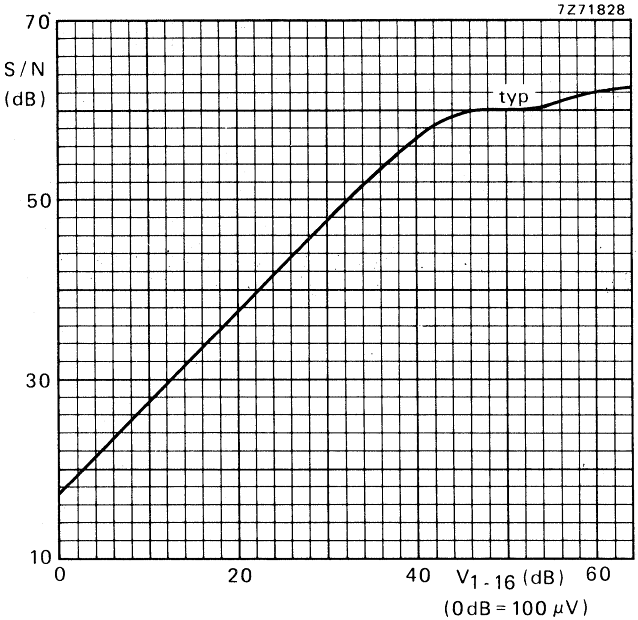


Fig. 7 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2541 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using p-n-p tuners.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit which can be switched on/off by a d.c. level, e.g. during tuning
- a.g.c. circuit with noise gating
- tuner a.g.c. output (p-n-p tuners)
- VCR switch, which switches off the video output; e.g. for insertion of a VCR playback signal.

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}13}$	typ.	12	V
Supply current	I_{11}	typ.	50	mA
I.F. input voltage at f = 38,9 MHz (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	100	μV
Video output voltage (white at 10% of top sync)	$V_{12(p\text{-}p)}$	typ.	2,7	V
I.F. voltage gain control range	G_v	typ.	64	dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58	dB
A.F.C. output voltage swing for Δf = 100 kHz	$\Delta V_{5\text{-}13}$	typ.	10	V

PACKAGE OUTLINES

TDA2541 : 16-lead DIL; plastic (SOT-38).
TDA2541Q: 16-lead QIL; plastic (SOT-58).

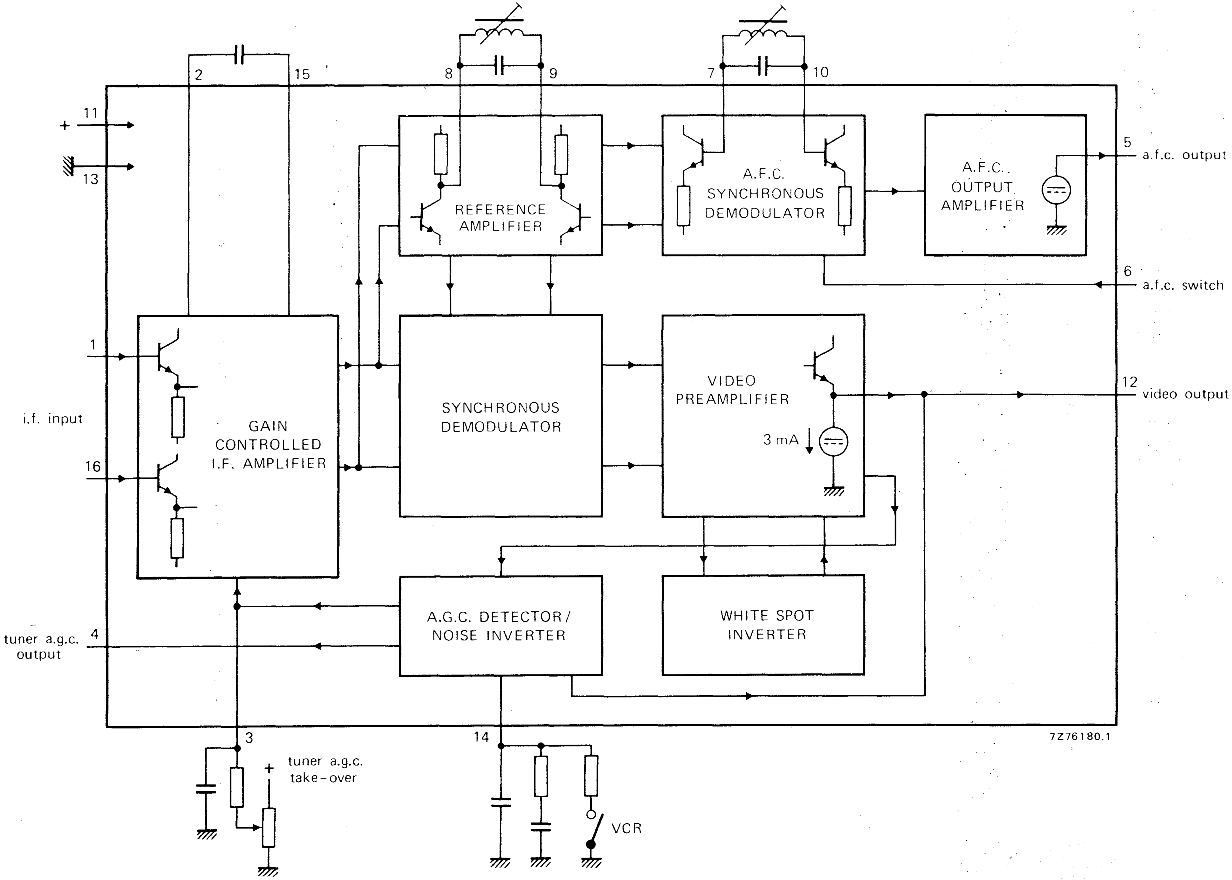


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{11\text{-}13}$	max.	13,2	V
Tuner a.g.c. voltage	$V_{4\text{-}13}$	max.	12	V
Total power dissipation	P_{tot}	max.	900	mW
Storage temperature	T_{stg}		−55 to + 125	°C
Operating ambient temperature	T_{amb}		−25 to + 60	°C

CHARACTERISTICS (measured in Fig. 5)

Supply voltage range	$V_{11\text{-}13}$	typ.	12	V
			10,2 to 13,2	V

The following characteristics are measured at T_{amb} = 25 °C; $V_{11\text{-}13}$ = 12 V; f = 38,9 MHz

I.F. input voltage for onset of a.g.c. (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	100	μV
		<	150	μV
Differential input impedance	$\lvert Z_{1\text{-}16} \rvert$	typ.	2 kΩ in parallel with 2 pF	
Zero-signal output level	$V_{12\text{-}13}$	typ.	6 ± 0,3	V*
Top sync output level	$V_{12\text{-}13}$	typ.	3,07	V
			2,9 to 3,2	V
I.F. voltage gain control range	G_v	typ.	64	dB
Bandwidth of video amplifier (3 dB)	B	typ.	6	MHz
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58	dB**
Differential gain	dG	typ.	4	%
		<	10	%
Differential phase	dφ	typ.	2°	
		<	10°	

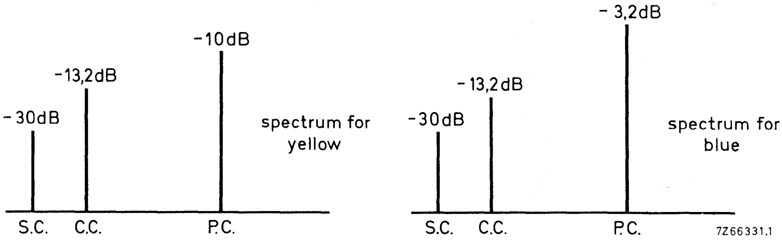
---

* So-called 'projected zero point', e.g. with switched demodulator.

** $$S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at B = 5 MHz}}.$$

CHARACTERISTICS (continued)

Intermodulation at 1,1 MHz: blue*		>	46 dB
		typ.	60 dB
	yellow*	>	46 dB
		typ.	50 dB
at 3,3 MHz**		>	46 dB
		typ.	54 dB



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level
with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

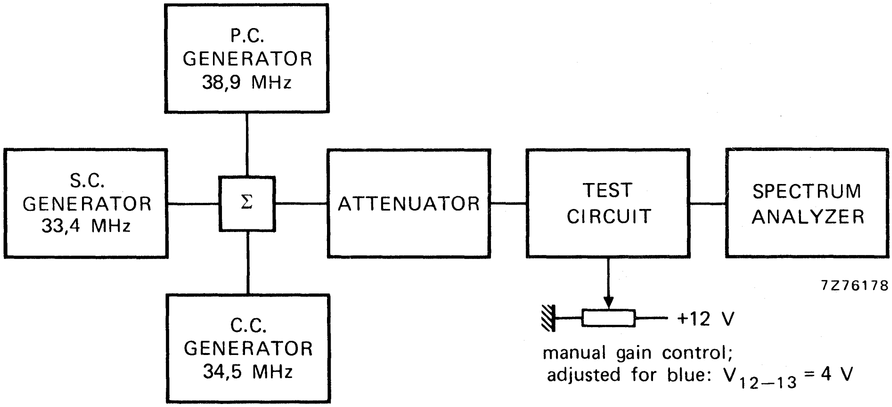


Fig. 3 Test set-up for intermodulation.

* $20 \log \frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 1,1 \text{ MHz}} + 3,6$ dB.

** $20 \log \frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 3,3 \text{ MHz}}$

Carrier signal at video output		typ. <	4 30	mV mV
2nd harmonic of carrier at video output		typ. <	20 30	mV mV
White spot inverter threshold level (Fig. 4)		typ.	6,6	V
White spot insertion level (Fig. 4)		typ.	4,7	V
Noise inverter threshold level (Fig. 4)		typ.	1,8	V
Noise insertion level (Fig. 4)		typ.	3,8	V
External video switch (VCR) switches off the output at:	V_{14-13}	<	1,1	V

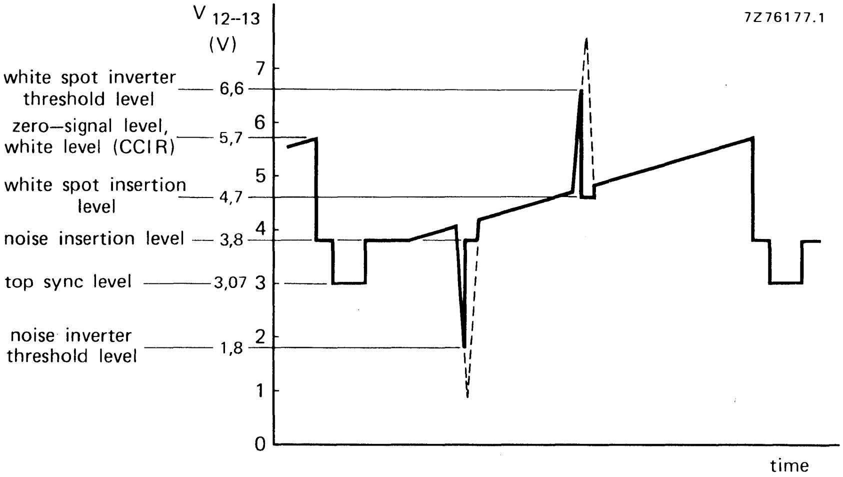


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

Tuner a.g.c. output current range	I_4		0 to 10	mA
Tuner a.g.c. output voltage at I_4 = 10 mA	V_{4-13}	<	0,3	V
Tuner a.g.c. output leakage current V_{14-13} = 11 V; V_{4-13} = 12 V	I_4	<	15	μA
Maximum a.f.c. output voltage swing	ΔV_{5-13}	> typ.	10 11	V V
Detuning for a.f.c. output voltage swing of 10 V	Δf	typ. <	100 200	kHz kHz
A.F.C. zero-signal output voltage (minimum gain)	V_{5-13}	typ.	6 4 to 8	V V
A.F.C. switches on at:	V_{6-13}	>	3,2	V
A.F.C. switches off at:	V_{6-13}	<	1,5	V

APPLICATION INFORMATION

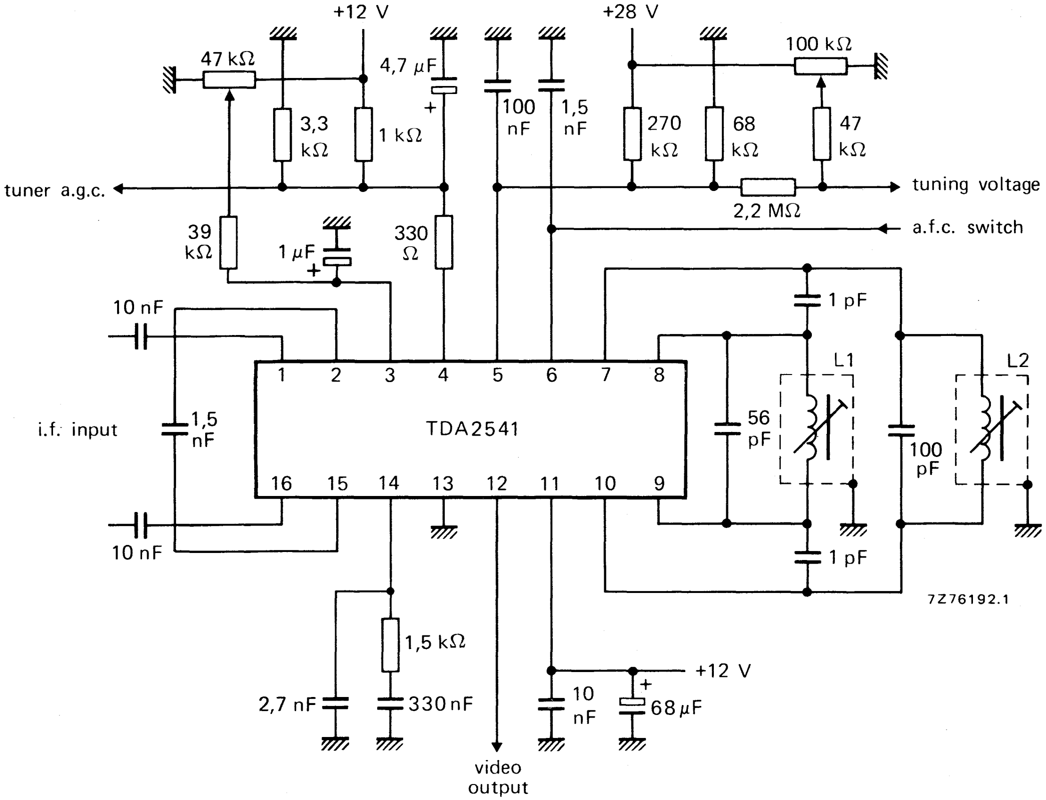


Fig. 5 Typical application circuit diagram; Q of L1 and L2 ≈ 80; f_o = 38,9 MHz.

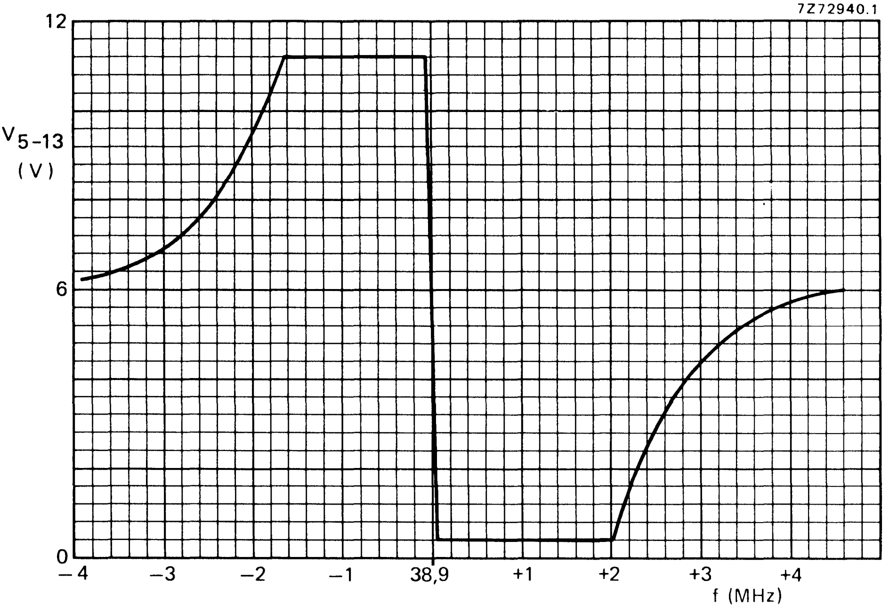


Fig. 6 A.F.C. output voltage ($V_{5\text{-}13}$) as a function of the frequency.

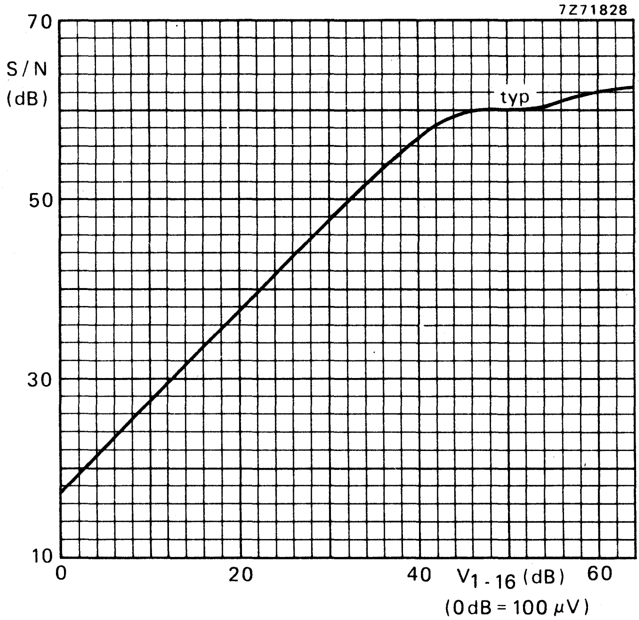


Fig. 7 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2542 is an i.f. amplifier and **demodulator** circuit for E and L standards in colour and black and white television receivers using p-n-p tuners.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- video preamplifier
- a.f.c. circuit which can be switched on/off by a d.c. level, e.g. during tuning
- a.g.c. circuit
- tuner a.g.c. output (p-n-p tuners)

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}13}$	typ.	12	V
Supply current	I_{11}	typ.	50	mA
I.F. input voltage at f = 32,7 MHz (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	100	μV
Video output voltage (peak-to-peak value)	$V_{12(p\text{-}p)}$	typ.	3	V
I.F. voltage gain control range	G_v	typ.	64	dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58	dB
A.F.C. output voltage swing for Δf = 100 kHz	$\Delta V_{5\text{-}13}$	typ.	10	V

PACKAGE OUTLINES

TDA2542 : 16-lead DIL; plastic (SOT-38).
TDA2542Q: 16-lead QIL; plastic (SOT-58).

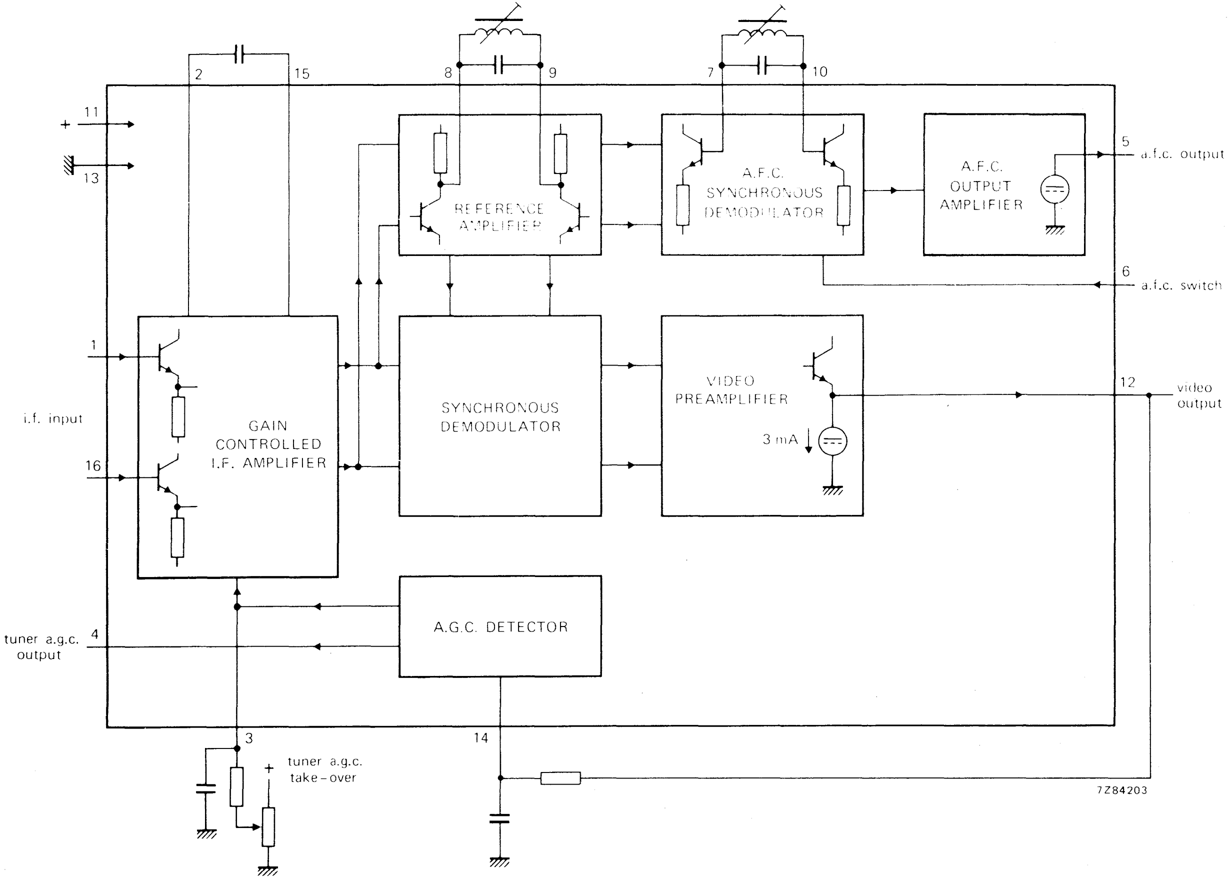


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{11\text{-}13}$	max.	13,8 V
Tuner a.g.c. voltage	$V_{4\text{-}13}$	max.	12 V
Total power dissipation	P_{tot}	max.	900 mW
Storage temperature	T_{stg}		−55 to + 125 °C
Operating ambient temperature	T_{amb}		−25 to + 60 °C

CHARACTERISTICS (measured in Fig. 2)

Supply voltage range	$V_{11\text{-}13}$	typ.	12 V
			10,2 to 13,8 V

The following characteristics are measured at T_{amb} = 25 °C; $V_{11\text{-}13}$ = 12 V; f = 32,7 MHz

I.F. input voltage for onset of a.g.c. (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	100 μV
		$<$	150 μV
Differential input impedance	$\|Z_{1\text{-}16}\|$	typ.	2 kΩ in parallel with 2 pF
Zero-signal output level	$V_{12\text{-}13}$	typ.	2,9 V
Maximum video output voltage (peak-to-peak value)	$V_{12(p\text{-}p)}$	$>$	4 V
Video output voltage variation at 50 dB input voltage variation	$\Delta V_{12\text{-}13}$	$<$	0,5 dB
I.F. voltage gain control range	G_v	typ.	64 dB
Bandwidth of video amplifier (3 dB)	B	typ.	6 MHz
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58 dB*
Differential gain	dG	typ.	4 %
		$<$	10 %
Differential phase	dφ	typ.	2°
		$<$	10°

DEVELOPMENT SAMPLE DATA

$$* \; S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$

CHARACTERISTICS (continued)

Carrier signal at video output		typ. <	4 30	mV mV
2nd harmonic of carrier at video output		typ. <	20 30	mV mV
Tuner a.g.c. output current range	I_4		0 to 10	mA
Tuner a.g.c. output voltage at I_4 = 10 mA	$V_{4\text{-}13}$	<	0,3	V
Tuner a.g.c. output leakage current $V_{14\text{-}13}$ = 3 V; $V_{4\text{-}13}$ = 12 V	I_4	<	15	μA
Maximum a.f.c. output voltage swing	$\Delta V_{5\text{-}13}$	> typ.	10 11	V V
Detuning for a.f.c. output voltage swing of 10 V	Δf	typ. <	100 200	kHz kHz
A.F.C. switches on at:	$V_{6\text{-}13}$	>	3,2	V
A.F.C. switches off at:	$V_{6\text{-}13}$	<	1,5	V
A.G.C. detector reference voltage	$V_{14\text{-}13}$	typ.	3,9	V

APPLICATION INFORMATION

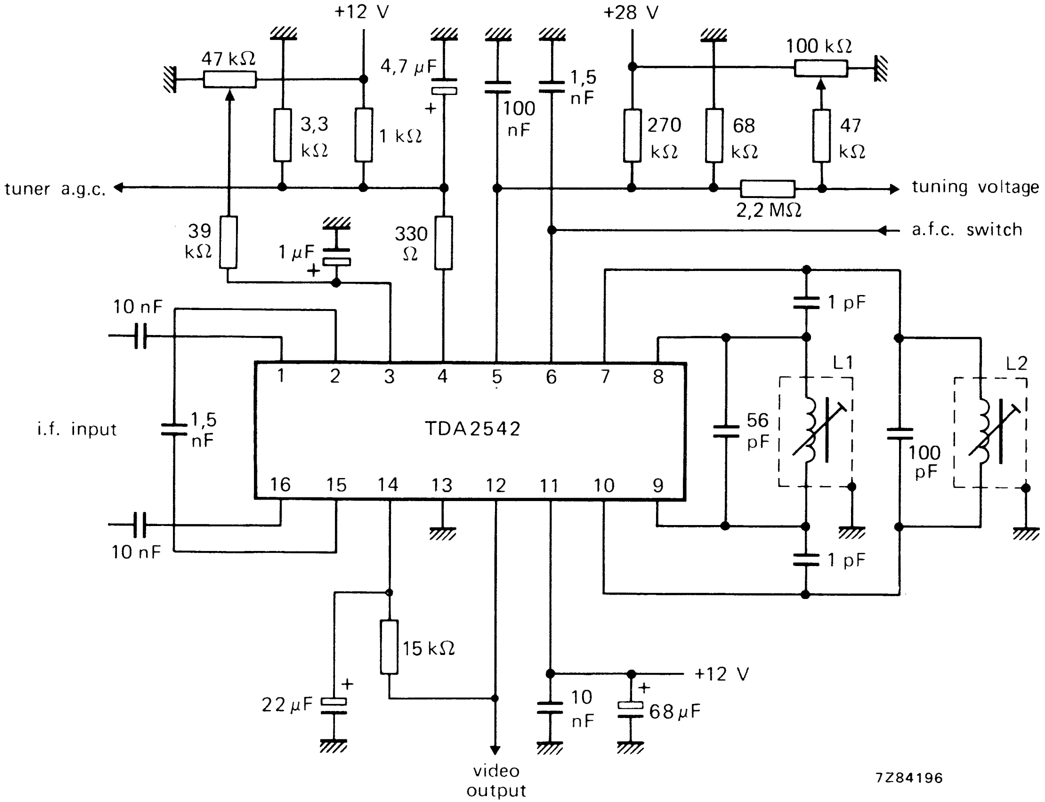
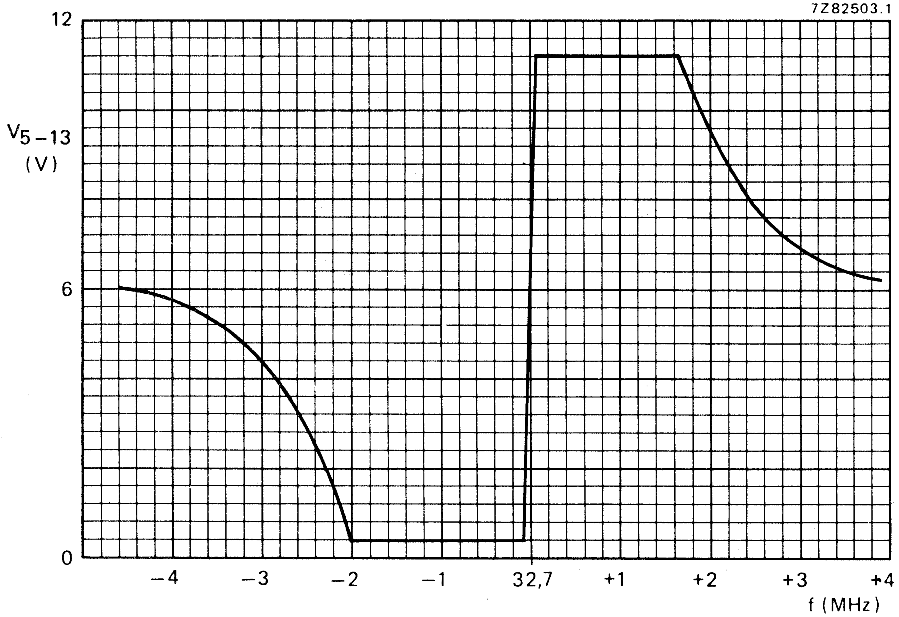


Fig. 2 Typical application circuit diagram; Q of L1 and L2 ≈ 80; f = 32,7 MHz.



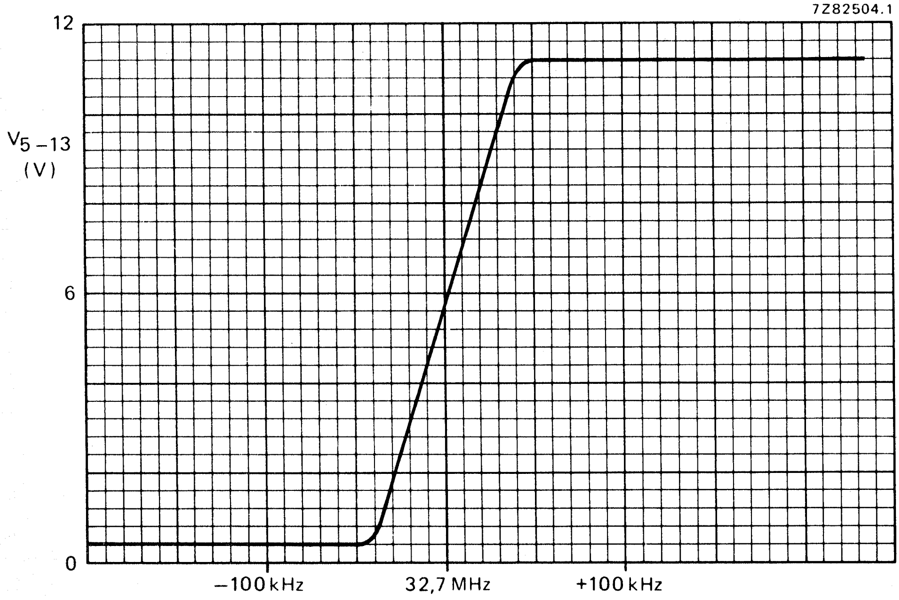


Fig. 3 A.F.C. output voltage (V_{5-13}) as a function of the frequency.

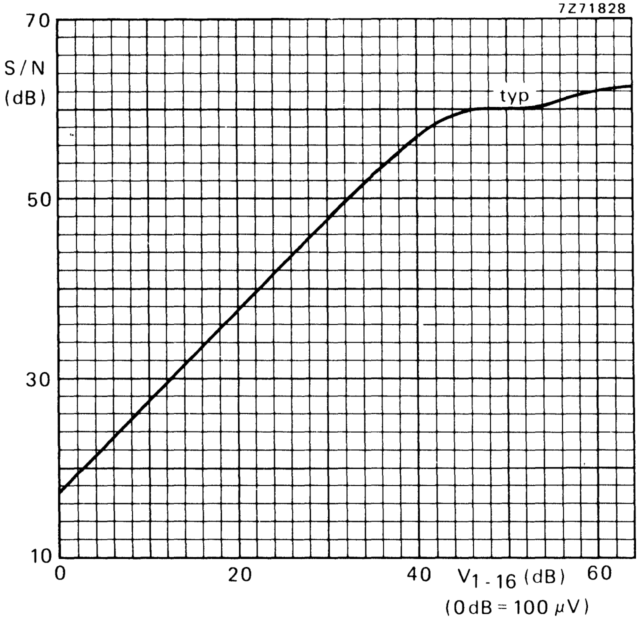


Fig. 4 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

AM SOUND I.F. CIRCUIT FOR FRENCH STANDARD

GENERAL DESCRIPTION

The TDA2543 is a monolithic integrated AM sound i.f. circuit in television receivers for the French standards L and L′.

The circuit incorporates the following functions:

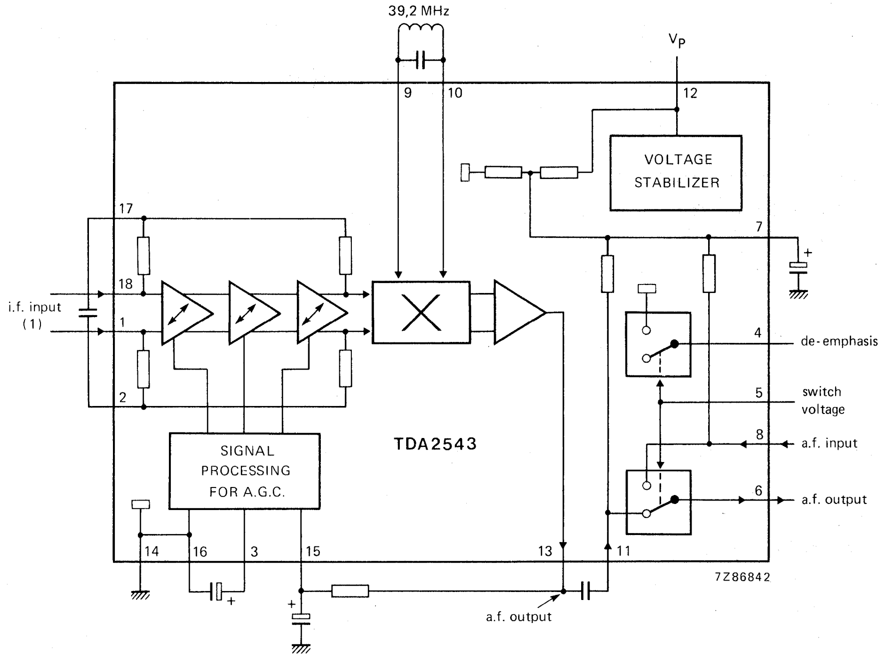
- 3-stage gain controlled i.f. amplifier, providing complete i.f. gain
- Synchronous AM demodulator
- A.G.C. circuit
- Audio input circuit with two external audio inputs and switching facilities to provide for either the demodulated i.f. or an external signal output
- Demodulated i.f. output is available from the input of the switching circuit

QUICK REFERENCE DATA

Supply voltage (pin 12)	$V_{12\text{-}14} = V_P$	typ.	12	V
Minimum i.f. vision carrier input voltage (r.m.s. value) for an output signal $V_{13\text{-}14(rms)} = 480$ mV	$V_{VC1\text{-}18(rms)}$	max.	30	μV
I.F. control range	ΔG_v	min.	60	dB
A.F. output voltage (r.m.s. value)	$V_{13\text{-}14(rms)}$	typ.	680	mV
Distortion at $V_{VC1\text{-}18(rms)} = 5$ mV	d_{tot}	max.	1	%
Signal-to-weighted-noise ratio according to CCIR 468	S + N/N	min.	50	dB
Maximum signal amplitude for the a.f. switch (r.m.s. value)	$V_{8;11\text{-}14(rms)}$	min.	2	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 12)	$V_{12\text{-}14} = V_P$	max.	13,2	V
Switch voltage (pin 5)	$V_{5\text{-}14}$	max.	V_P	V
Current at pin 4	I_4	max.	5	mA
	$-I_4$	short-circuit proof		
Storage temperature range	T_{stg}	−25 to	+150	°C
Operating ambient temperature range	T_{amb}	−20 to	+70	°C

CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C; input signal (vision carrier V.C.) with $f_{VC} = 39{,}2$ MHz; sound carrier (S.C.) modulated with $f_m = 1$ kHz and $m = 0{,}8$; measured in Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage range (pin 12)	V_P	10,8	–	13,2	V
Supply current (pin 12)	I_P	–	50	–	mA
I.F. input (pins 1 and 18)					
Minimum i.f. vision carrier input voltage (r.m.s. value) for an output signal $V_{13\text{-}14(rms)} = 480$ mV	$V_{VC1\text{-}18(rms)}$	–	–	30	μV
Maximum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1\text{-}18(rms)}$	–	50	–	mV
Input resistance	$R_{1\text{-}18}$	–	2	–	kΩ
Input capacitance	$C_{1\text{-}18}$	–	2	–	pF
I.F. control range (–3 dB)	ΔG_v	60	–	–	dB
A.F. output (pin 13)					
A.F. output voltage (r.m.s. value) at $V_{VC1\text{-}18(rms)} = 5$ mV	$V_{13\text{-}14(rms)}$	–	680	–	mV
Output resistance	$R_{13\text{-}14}$	–	100	–	Ω
Distortion at $V_{VC1\text{-}18(rms)} = 5$ mV	d_{tot}	–	–	1	%
Signal-to-weighted-noise ratio at a.f. output (pin 13) according to CCIR 468 at $V_{VC1\text{-}18(rms)} = 5$ mV	S + N/N	50	–	–	dB
A.F. switch (pins 8, 11 and 6)					
Maximum input voltage (r.m.s. value)	$V_{8\text{-}14(rms)}$ $V_{11\text{-}14(rms)}$	2 2	– –	– –	V V
Voltage gain	G_v	–	0 ± 1	–	dB
Amplitude frequency response (–3 dB)	f	20	–	20 000	Hz
Crosstalk between the non-switched input and the output	α	60	–	–	dB
Input resistance	$R_{8;\,11\text{-}14}$	10	–	–	kΩ
Output resistance	$R_{6\text{-}14}$	–	400	–	Ω
De-emphasis switch (pin 4)					
Input resistance for:					
ON ($V_{5\text{-}14} > 3$ V)	$R_{4\text{-}14}$	–	–	200	Ω
OFF ($V_{5\text{-}14} < 1$ V)	$R_{4\text{-}14}$	100	–	–	kΩ
Switch voltage (pin 5)					
A.F. switch ON (pin 8 switched)	$V_{5\text{-}14}$	3	–	V_P	V
A.F. switch OFF (pin 11 switched)	$V_{5\text{-}14}$	0	–	1	V

DEVELOPMENT SAMPLE DATA

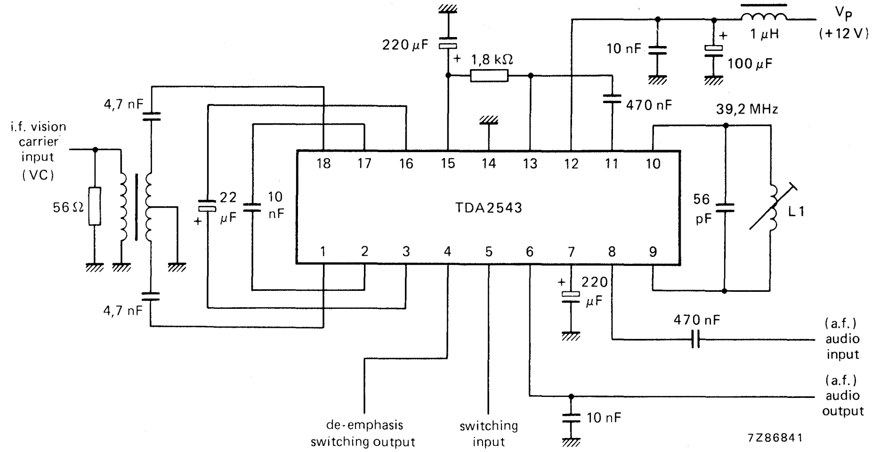


Fig. 2 Measuring circuit; L1 adjusted to minimum distortion at the a.f. output.

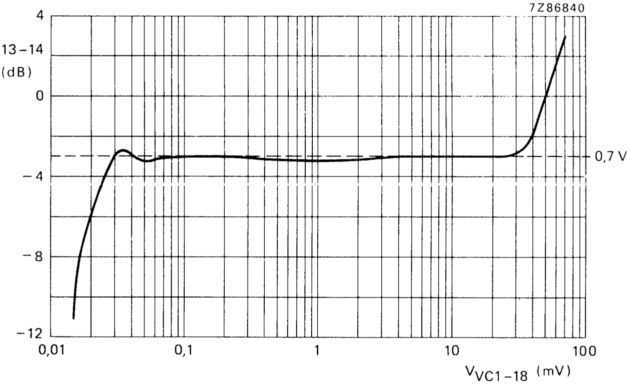


Fig. 3 Control curve of the i.f. amplifier; the r.m.s. a.f. output voltage at pin 13 ($V_{13\text{-}14(rms)}$) as a function of the r.m.s. i.f. vision carrier input voltage ($V_{VC1\text{-}18(rms)}$) at f_m = 1 kHz and m = 0,8.

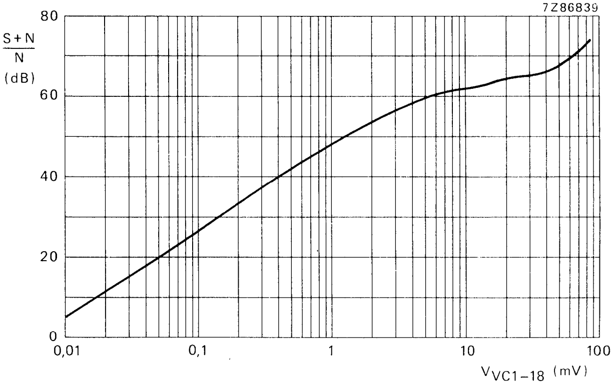


Fig. 4 Signal-to-weighted-noise ratio (S + N/N) at the output (pin 13) as a function of the r.m.s. i.f. vision carrier input voltage ($V_{VC1\text{-}18(rms)}$).

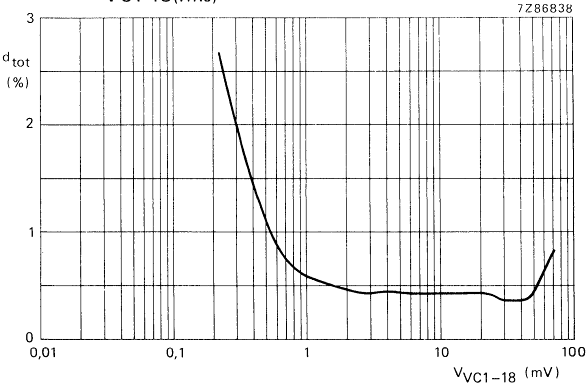


Fig. 5 Distortion (d_{tot}) at the output (pin 13) as a function of the r.m.s. i.f. vision carrier input voltage ($V_{VC1\text{-}18(rms)}$) at f_m = 1 kHz and m = 0,8.

TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2544 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- low-level synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit with balanced output
- a.g.c. circuit with noise gating
- tuner a.g.c. output for control of MOS tuners
- external video switch

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}13}$	typ.	12	V
Supply current	I_{11}	typ.	50	mA
I.F. input sensitivity at f = 45,75 MHz (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	150	μV
Video output voltage (white at 12,5% of top sync)	$V_{12(p\text{-}p)}$	typ.	2,6	V
I.F. voltage gain control range	G_v	typ.	63	dB
Signal-to-noise ratio V_i = 10 mV	S/N	typ.	58	dB
A.F.C. sensitivity		typ.	80	mV/kHz

PACKAGE OUTLINES

TDA2544 16-lead DIL; plastic (SOT-38).
TDA2544Q: 16-lead QIL; plastic (SOT-58).

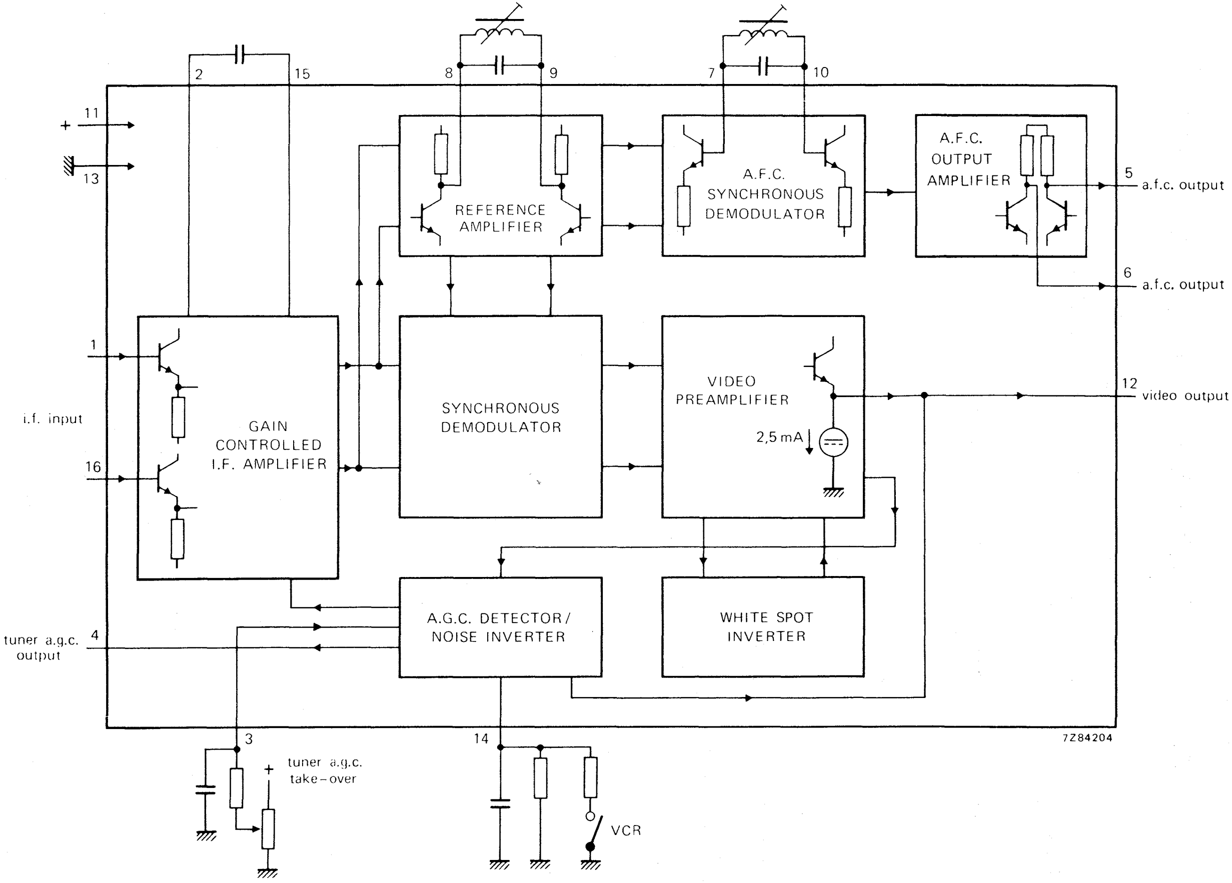


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{11\text{-}13}$	max.	13,8	V
Tuner a.g.c. voltage	$V_{4\text{-}13}$	max.	12	V
Total power dissipation	P_{tot}	max.	1,2	W
Storage temperature	T_{stg}		−55 to + 125	°C
Operating ambient temperature	T_{amb}		−25 to + 65	°C

CHARACTERISTICS (measured in Fig. 5)

Supply voltage range	$V_{11\text{-}13}$	typ. 	12 10,2 to 13,8	V V

The following characteristics are measured at T_{amb} = 25 °C; $V_{11\text{-}13}$ = 12 V

I.F. input voltage for onset of a.g.c. (r.m.s. value) at f = 45,75 MHz	$V_{1\text{-}16(rms)}$	typ.	150	μV
Differential input impedance	$\|Z_{1\text{-}16}\|$	typ.	3 kΩ in parallel with 2 pF	
Zero-signal output level	$V_{12\text{-}13}$	typ.	5,5	V*
Top sync output level	$V_{12\text{-}13}$	typ.	2,5	V
I.F. voltage gain control range	G_v	typ.	63	dB
Bandwidth of video amplifier (3 dB)	B	typ.	6	MHz
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58	dB**
Differential gain	dG	typ. <	4 10	% %
Differential phase	$d\varphi$	typ. <	2° 10°	

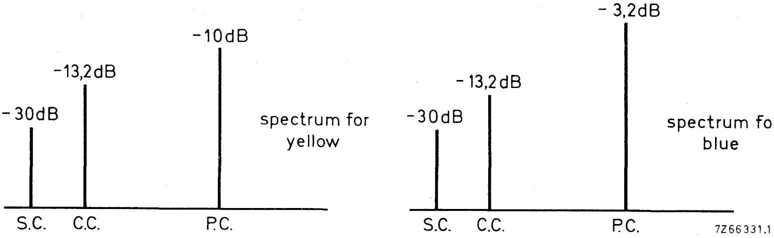
---

* So-called 'projected zero point', e.g. with switched demodulator.

$$** \; S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$

CHARACTERISTICS (continued)

Intermodulation at 0,9 MHz: blue*	typ.	50 dB
yellow*	typ.	46 dB
at 2,6 MHz**	typ.	49 dB



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level
with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

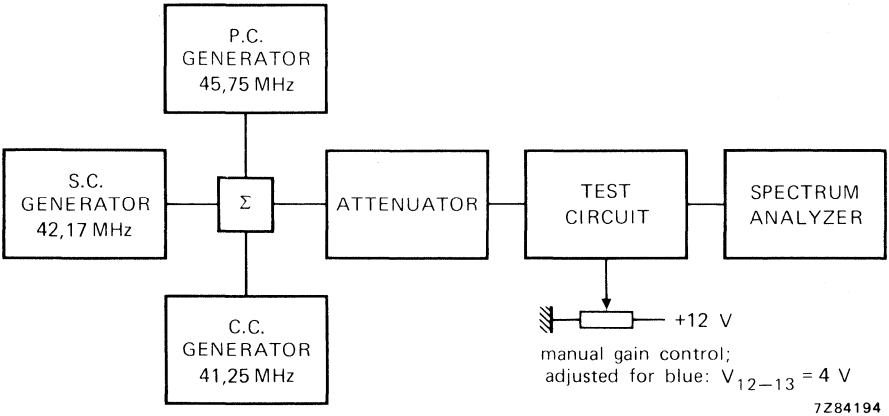


Fig. 3 Test set-up for intermodulation.

---

* $20 \log \frac{V_o \text{ at } 3,6 \text{ MHz}}{V_o \text{ at } 0,9 \text{ MHz}} + 3,6$ dB.

** $20 \log \frac{V_o \text{ at } 3,6 \text{ MHz}}{V_o \text{ at } 2,6 \text{ MHz}}$.

Carrier signal at video output		<	30	mV
2nd harmonic of carrier at video output		<	30	mV
White spot inverter threshold level (Fig. 4)		typ.	6,4	V
White spot insertion level (Fig. 4)		typ.	4,1	V
Noise inverter threshold level (Fig. 4)		typ.	1,6	V
Noise insertion level (Fig. 4)		typ.	3,3	V
External video switch (VCR) switches off the output at	$V_{14\text{-}13}$	<	1,0	V

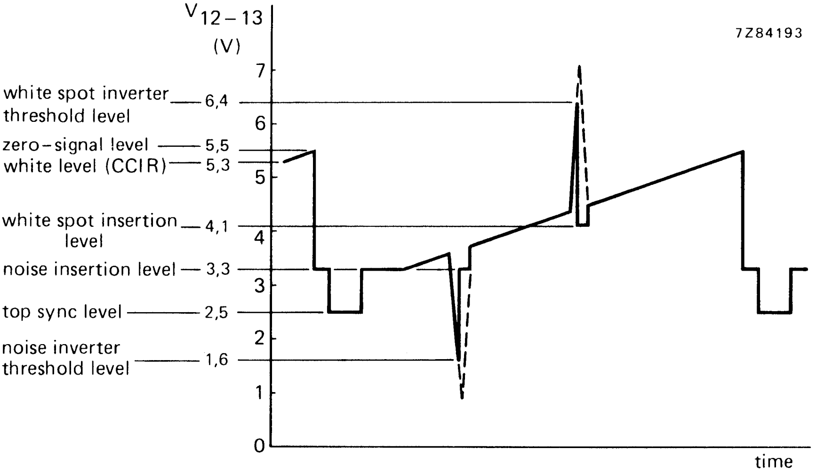


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

Tuner a.g.c. output current range	I_4		0 to 0,3	mA
Tuner a.g.c. output voltage at $I_4 = 0,3$ mA	$V_{4\text{-}13}$	<	0,3	V
Tuner a.g.c. output leakage current $V_{14\text{-}13} = 3$ V; $V_{4\text{-}13} = 12$ V	I_4	<	10	µA
A.F.C. output voltage (d.c. value)	$V_{5;6\text{-}13}$	typ.	6,8	V
A.F.C. output offset voltage	$\lvert V_{5\text{-}6} \rvert$	<	1,5	V
Maximum a.f.c. output voltage	$V_{5;6\text{-}13}$	>	11,6	V
Minimum a.f.c. output voltage	$V_{5;6\text{-}13}$	<	2,8	V
A.F.C. sensitivity		typ.	80	mV/kHz

APPLICATION INFORMATION

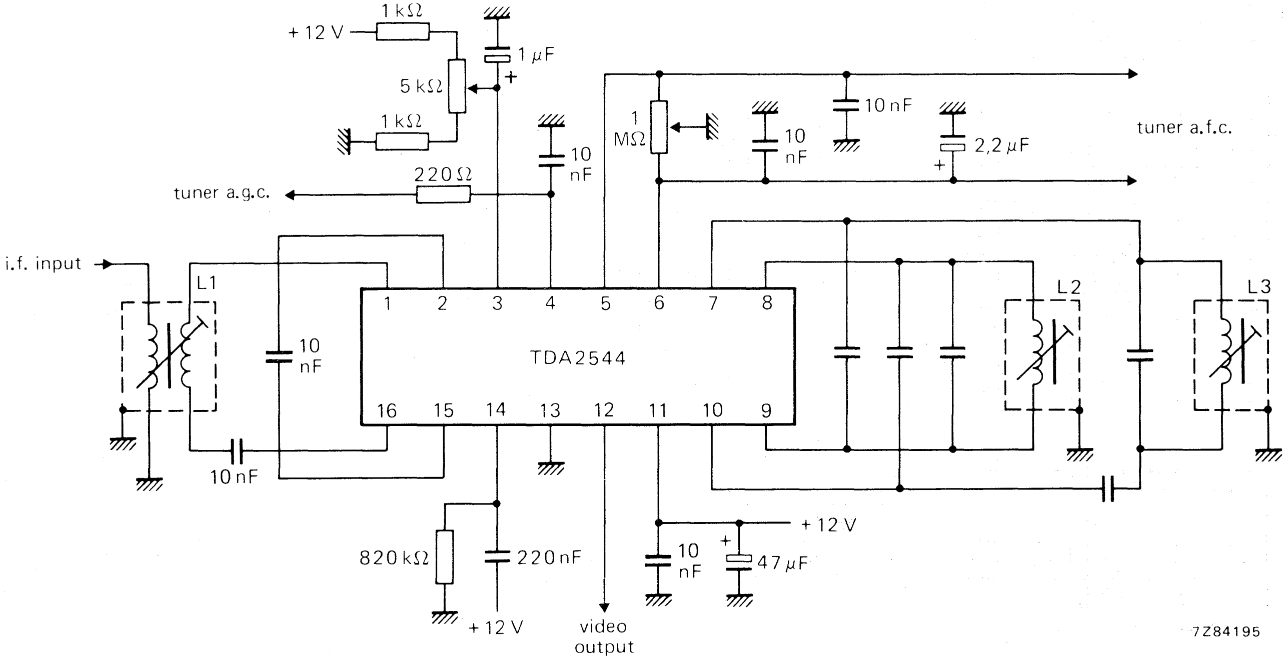


Fig. 5 Typical application diagram.

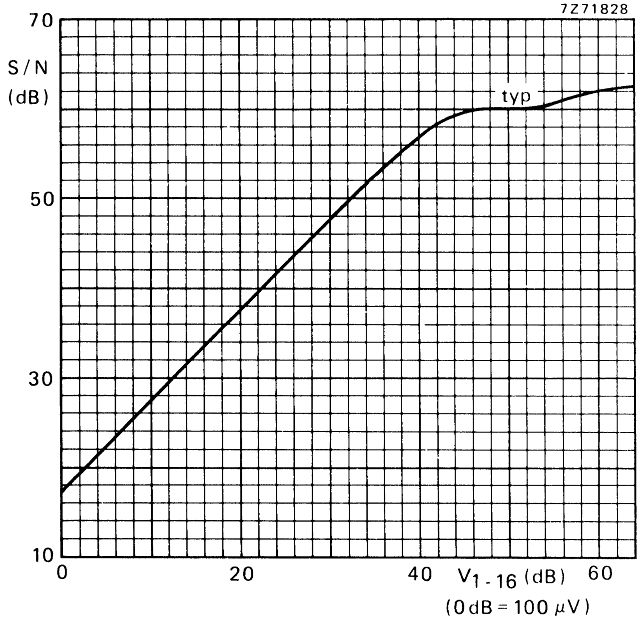


Fig. 6 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

QUASI-SPLIT-SOUND CIRCUIT

GENERAL DESCRIPTION

The TDA2545A is a monolithic integrated circuit for quasi-split-sound processing in television receivers.

Features

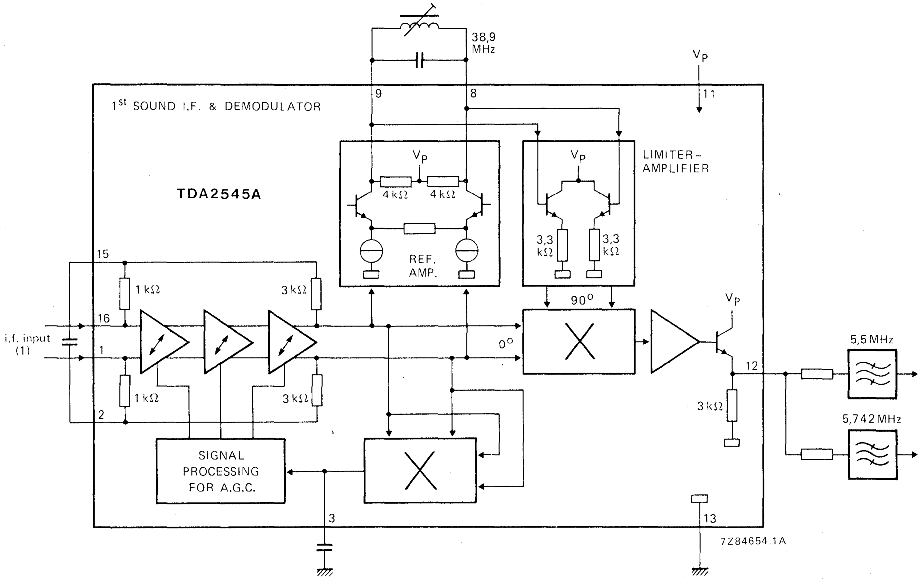
- 3-stage gain controlled i.f. amplifier
- A.G.C. circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

QUICK REFERENCE DATA

Supply voltage (pin 11)	$V_P = V_{11\text{-}13}$	typ.	12	V
Supply current (pin 11)	$I_P = I_{11}$	typ.	42	mA
Minimum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1\text{-}16(rms)}$	typ.	50	μV
Output voltage; 5,5 MHz (r.m.s. value)	$V_{12\text{-}13(rms)}$	typ.	100	mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{12\text{-}13(rms)}$	typ.	45	mV
I.F. control range	ΔG_v	min.	66	dB
Signal-to-weighted-noise ratio				
at 5,5 MHz	S + W/W	min.	53	dB
at 5,742 MHz	S + W/W	min.	51	dB

PACKAGE OUTLINES

16-lead DIL; plastic (SOT-38).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11\text{-}13}$	max.	13,2 V
Storage temperature range	T_{stg}	−25 to +150 °C	
Operating ambient temperature range	T_{amb}	0 to +70 °C	

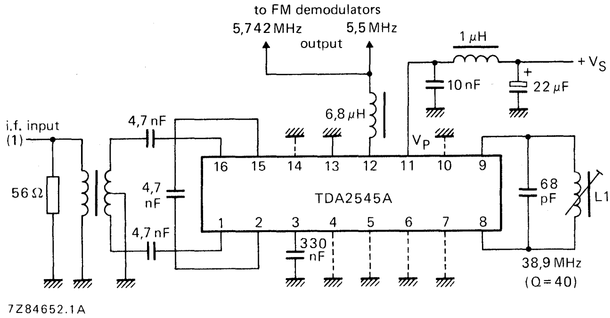
CHARACTERISTICS

$V_P = V_{11\text{-}13} = 12$ V; $T_{amb} = 25\ ^oC$; measured at $f_{VC} = 38{,}9$ MHz, $f_{SC1} = 33{,}4$ MHz, $f_{SC2} = 33{,}158$ MHz:

Vision carrier (V.C.) modulated with 2 T/20 T pulses, line-for-line alternating with white bars; modulation depth 100% (proportional to 10% residual carrier).

Sound carriers (S.C.1, S.C.2) modulated with f = 1 kHz and $\Delta f = \pm 30$ kHz.
Vision-to-sound carrier ratios are V.C./S.C.1 = 13 dB and V.C./S.C.2 = 20 dB.
Vision carrier amplitude (r.m.s. value) is $V_{VC} = 10$ mV.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 11)					
Supply voltage	$V_P = V_{11\text{-}13}$	10,8	12	13,2	V
Supply current	$I_P = I_{11}$	–	42	–	mA
I.F. amplifier					
Minimum input voltage (r.m.s. value) (intercarrier signals –3 dB)	$V_{VC1\text{-}16(rms)}$	–	50	–	μV
Maximum input voltage (r.m.s. value) (intercarrier signals + 1 dB)	$V_{VC1\text{-}16(rms)}$	–	100	–	mV
I.F. control range	ΔG_v	66	–	–	dB
Control voltage range	$V_{3\text{-}13}$	4	–	9	V
Input resistance	$R_{1\text{-}16}$	–	2	–	kΩ
Input capacitance	$C_{1\text{-}16}$	–	2	–	pF
Intercarrier generation					
Output voltage; 5,5 MHz (r.m.s. value)	$V_{12\text{-}13(rms)}$	–	100	–	mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{12\text{-}13(rms)}$	–	45	–	mV
D.C. output voltage	$V_{12\text{-}13}$	–	5,9	–	V
Allowable load resistance at the output	$R_{12\text{-}13}$	7	–	–	kΩ
Allowable output current	$-I_{12}$	–	–	1	mA
Intercarrier signal-to-noise (measured behind the FM demodulators)					
Signal-to-weighted-noise ratio according to CCIR 468-2, quasi-peak at 5,5 MHz	S + W/W	53	–	–	dB
at 5,742 MHz	S + W/W	51	–	–	dB
with black level (vision carrier modulated with sync pulses only) at 5,5 MHz	S + W/W	60	–	–	dB
at 5,742 MHz	S + W/W	58	–	–	dB



Pins 4, 5, 6, 7, 10 and 14 not connected.

(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 2 Measuring circuit for TDA2545A.

QUASI-SPLIT-SOUND CIRCUIT WITH 5,5 MHz DEMODULATION

GENERAL DESCRIPTION

The TDA2546A is a monolithic integrated circuit for quasi-split-sound processing, including 5,5 MHz demodulation, in television receivers.

Features

1st i.f. (V.C.: vision carrier plus S.C.: sound carrier)

- 3-stage gain controlled i.f. amplifier
- A.G.C. circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

2nd i.f. (5,5 MHz signal)

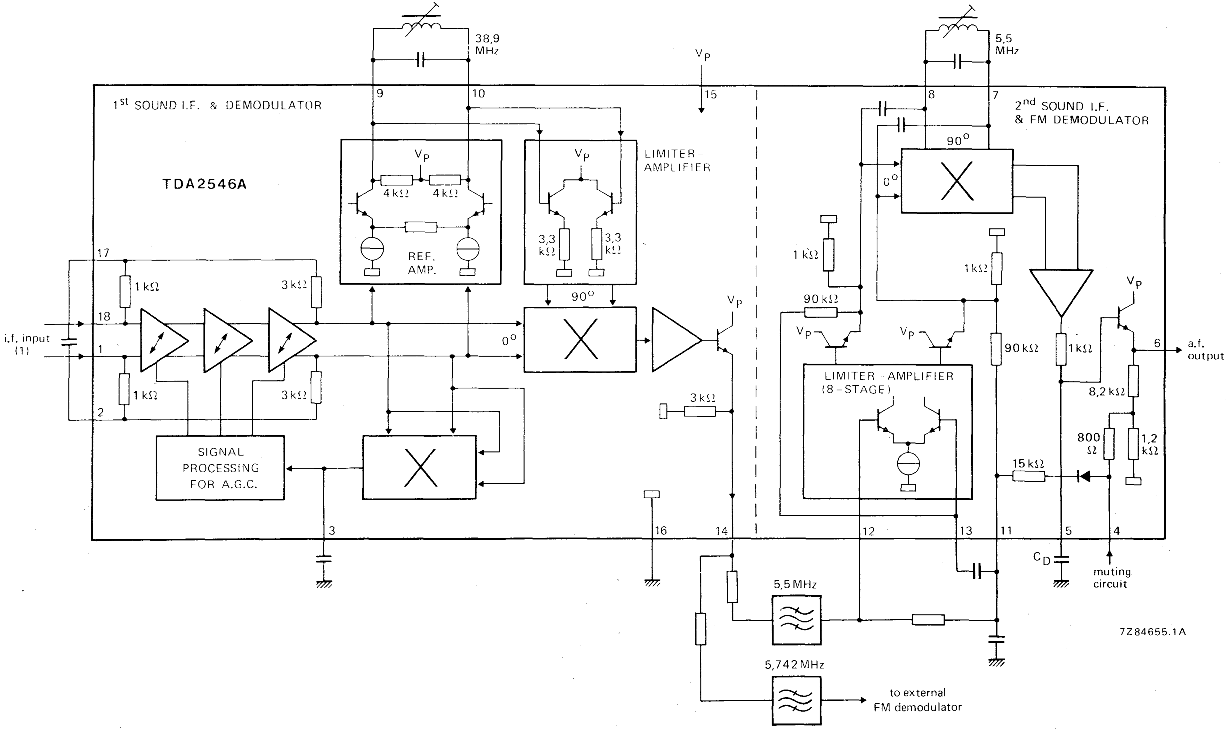
- 8-stage limiter amplifier
- Quadrature demodulator
- A.F. amplifier with de-emphasis
- AV switch

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_P = V_{15\text{-}16}$	typ.	12	V
Supply current (pin 15)	$I_P = I_{15}$	typ.	54	mA
Minimum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1\text{-}18(rms)}$	typ.	50	μV
Output voltage; 5,5 MHz (r.m.s. value)	$V_{14\text{-}16(rms)}$	typ.	100	mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{14\text{-}16(rms)}$	typ.	45	mV
I.F. control range	ΔG_v	min.	66	dB
Signal-to-weighted-noise ratio				
at 5,5 MHz	S + W/W	min.	53	dB
at 5,742 MHz	S + W/W	min.	51	dB
A.F. output voltage (r.m.s. value)	$V_{o6\text{-}16(rms)}$	typ.	0,6	V

PACKAGE OUTLINES

18-lead DIL; plastic (SOT-102CS).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.)

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15\text{-}16}$	max.	13,2	V
Input current (pin 4)	I_4	max.	5	mA
Storage temperature range	T_{stg}	−25 to	+150	°C
Operating ambient temperature range	T_{amb}	0 to	+70	°C

CHARACTERISTICS

$V_P = V_{15\text{-}16} = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38{,}9$ MHz, $f_{SC1} = 33{,}4$ MHz, $f_{SC2} = 33{,}158$ MHz:

Vision carrier (V.C.) modulated with 2 T/20 T pulses, line-for-line alternating with white bars; modulation depth 100% (proportional to 10% residual carrier).

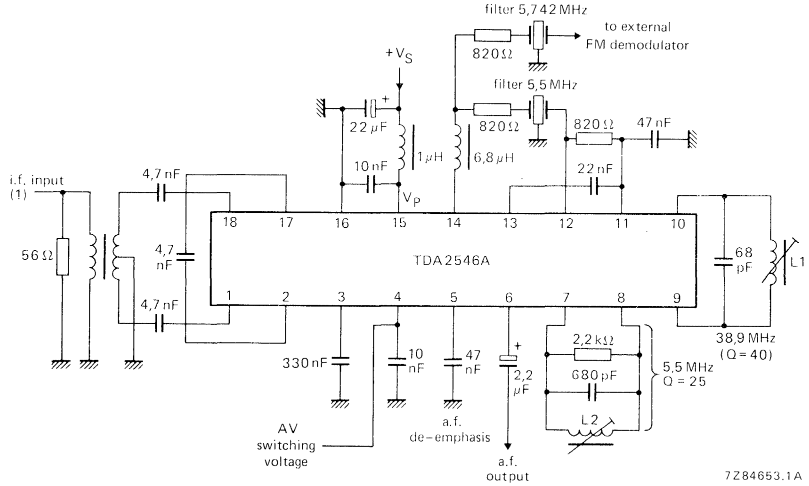
Sound carriers (S.C.1, S.C.2) modulated with f = 1 kHz and Δf = ± 30 kHz.

Vision-to-sound carrier ratios are V.C./S.C.1 = 13 dB and V.C./S.C.2 = 20 dB.
Vision carrier amplitude (r.m.s. value) is $V_{VC} = 10$ mV.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15\text{-}16}$	10,8	12	13,2	V
Supply current	$I_P = I_{15}$	–	54	–	mA
I.F. amplifier					
Minimum input voltage (r.m.s. value) (intercarrier signals –3 dB)	$V_{VC1\text{-}18(rms)}$	–	50	–	μV
Maximum input voltage (r.m.s. value) (intercarrier signals + 1 dB)	$V_{VC1\text{-}18(rms)}$	–	100	–	mV
I.F. control range	ΔG_v	66	–	–	dB
Control voltage range	$V_{3\text{-}16}$	4	–	9	V
Input resistance	$R_{1\text{-}18}$	–	2	–	kΩ
Input capacitance	$C_{1\text{-}18}$	–	2	–	pF
Intercarrier generation					
Output voltage; 5,5 MHz (r.m.s. value)	$V_{14\text{-}16(rms)}$	–	100	–	mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{14\text{-}16(rms)}$	–	45	–	mV
D.C. output voltage	$V_{14\text{-}16}$	–	5,9	–	V
Allowable load resistance at the output	$R_{14\text{-}16}$	7	–	–	kΩ
Allowable output current	$-I_{14}$	–	–	1	mA
Frequency demodulator (measured at f = 5,5 MHz)					
Input voltage for start of limiting (r.m.s. value)	$V_{12\text{-}16(rms)}$	–	–	100	μV
Maximum input voltage (r.m.s. value)	$V_{12\text{-}16(rms)}$	–	200	–	mV
D.C. output voltage	$V_{11,12,13\text{-}16}$	–	2,2	–	V

DEVELOPMENT SAMPLE DATA

parameter	symbol	min.	typ.	max.	unit
A.F. output voltage (r.m.s. value)	$V_{6\text{-}16(rms)}$	–	600	–	mV
D.C. output voltage	$V_{6\text{-}16}$	–	4	–	V
Allowable load resistance at the output	$R_{6\text{-}16}$	27	–	–	kΩ
Total harmonic distortion	THD	–	–	1	%
Internal de-emphasis resistance	$R_{i5\text{-}16}$	–	1	–	kΩ
Switching voltage (pin 4)					
for mute	$V_{4\text{-}16}$	9	–	–	V
for a.f. on	$V_{4\text{-}16}$	–	–	2,5	V
Intercarrier signal-to-noise (measured behind the FM demodulators)					
Signal-to-weighted-noise ratio according to CCIR 468-2, quasi-peak					
at 5,5 MHz	S + W/W	53	–	–	dB
at 5,742 MHz	S + W/W	51	–	–	dB
with black level (vision carrier modulated with sync pulses only)					
at 5,5 MHz	S + W/W	60	–	–	dB
at 5,742 MHz	S + W/W	58	–	–	dB



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 2 Measuring circuit for TDA2546A.

TELEVISION I.F. AMPLIFIER AND DEMODULATOR

GENERAL DESCRIPTION

The TDA2548 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using p-n-p tuners.
It incorporates the following functions:

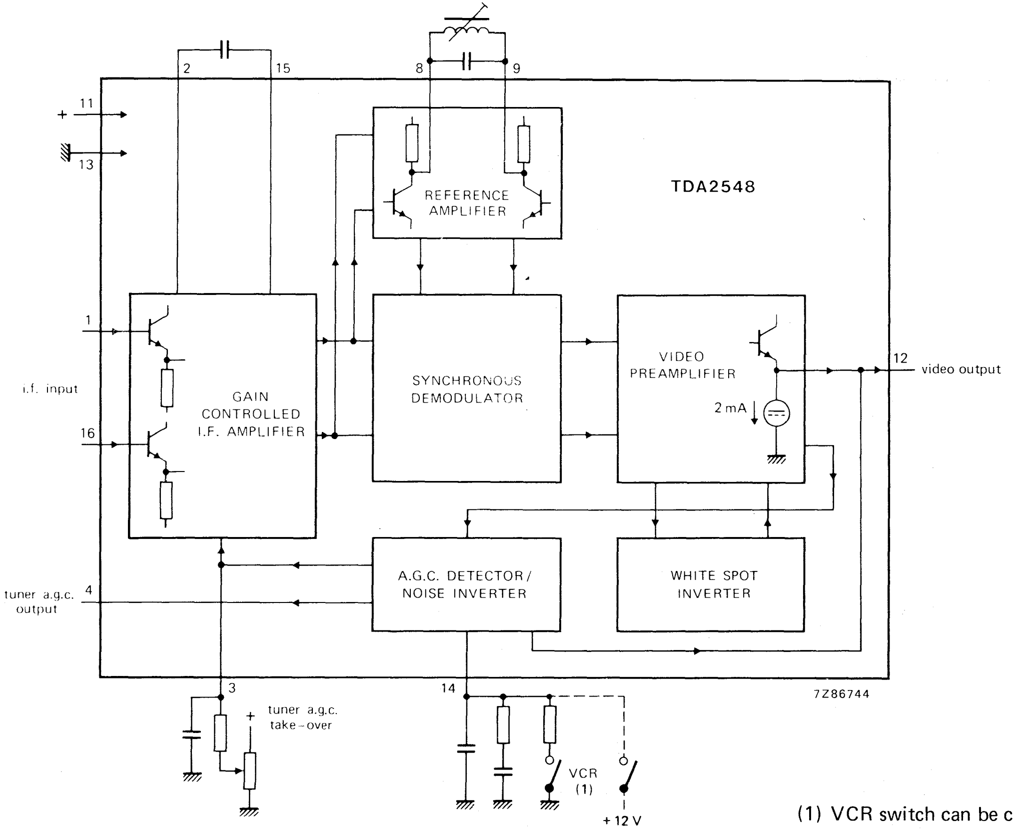
- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.g.c. circuit with noise gating
- tuner a.g.c. output (p-n-p tuners)
- VCR switch, which switches off the video output; e.g. for insertion of a VCR playback signal.

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}13}$	typ.	12	V
Supply current	I_{11}	typ.	50	mA
I.F. input voltage at f = 38,9 MHz (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	100	μV
Video output voltage (white at 10% of top sync)	$V_{12(p\text{-}p)}$	typ.	2,7	V
I.F. voltage gain control range	G_v	typ.	64	dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58	dB

PACKAGE OUTLINES

TDA2548 : 16-lead DIL; plastic (SOT-38).
TDA2548Q: 16-lead QIL; plastic (SOT-58).



(1) VCR switch can be connected either to ground or to + 12 V.

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{11\text{-}13}$	max.	13,2	V
Tuner a.g.c. voltage	$V_{4\text{-}13}$	max.	12	V
Total power dissipation	P_{tot}	max.	900	mW
Storage temperature	T_{stg}	−55 to + 125		°C
Operating ambient temperature	T_{amb}	−25 to + 60		°C

CHARACTERISTICS (measured in Fig. 5)

Supply voltage range	$V_{11\text{-}13}$	typ. 	12 10,2 to 13,2	V V

The following characteristics are measured at T_{amb} = 25 °C; $V_{11\text{-}13}$ = 12 V; f = 38,9 MHz

I.F. input voltage for onset of a.g.c. (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ. <	100 150	μV μV
Differential input impedance	$\|Z_{1\text{-}16}\|$	typ.	2 kΩ in parallel with 2 pF	
Zero-signal output level	$V_{12\text{-}13}$	typ.	6 ± 0,3	V*
Top sync output level	$V_{12\text{-}13}$	typ. 	3,07 2,9 to 3,2	V V
I.F. voltage gain control range	G_v	typ.	64	dB
Bandwidth of video amplifier (3 dB)	B	typ.	6	MHz
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58	dB**
Differential gain	dG	typ. <	4 10	% %
Differential phase	dφ	typ. <	2° 10°	

---

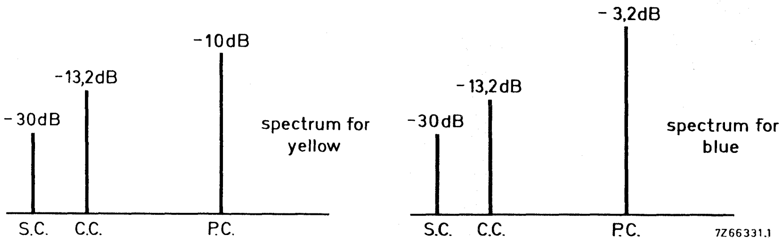
* So-called 'projected zero point', e.g. with switched demodulator.

**

$$S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$

CHARACTERISTICS (continued)

Intermodulation at 1,1 MHz:	blue*	>	46 dB
		typ.	60 dB
	yellow*	>	46 dB
		typ.	50 dB
at 3,3 MHz**		>	46 dB
		typ.	54 dB



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level

} with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

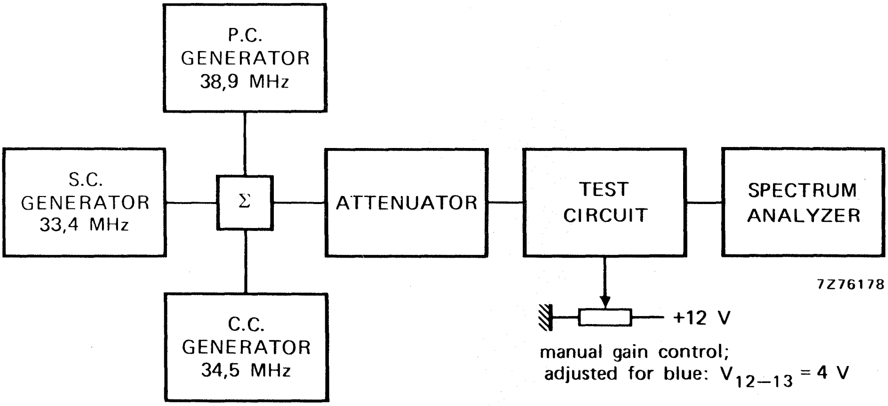


Fig. 3 Test set-up for intermodulation.

$$* \; 20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 1{,}1 \text{ MHz}} + 3{,}6 \text{ dB}. \qquad ** \; 20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 3{,}3 \text{ MHz}}$$

Carrier signal at video output		typ.	4	mV
		<	30	mV
2nd harmonic of carrier at video output		typ.	20	mV
		<	30	mV
White spot inverter threshold level (Fig. 4)		typ.	6,6	V
White spot insertion level (Fig. 4)		typ.	4,7	V
Noise inverter threshold level (Fig. 4)		typ.	1,8	V
Noise insertion level (Fig. 4)		typ.	3,8	V
External video switch (VCR) switches off the output at:	$V_{14\text{-}13}$	<	1,1	V

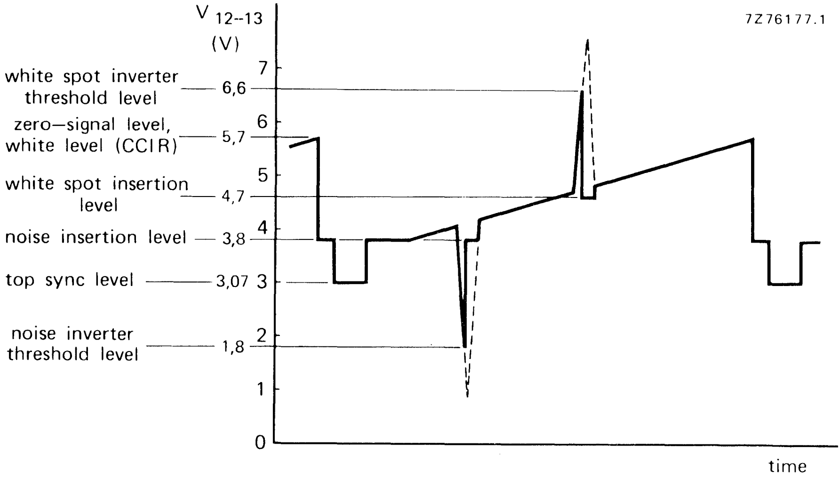


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

Tuner a.g.c. output current range	I_4		0 to 10	mA
Tuner a.g.c. output voltage at I_4 = 10 mA	$V_{4\text{-}13}$	<	0,3	V
Tuner a.g.c. output leakage current $V_{14\text{-}13}$ = 11 V; $V_{4\text{-}13}$ = 12 V	I_4	<	15	μA

APPLICATION INFORMATION

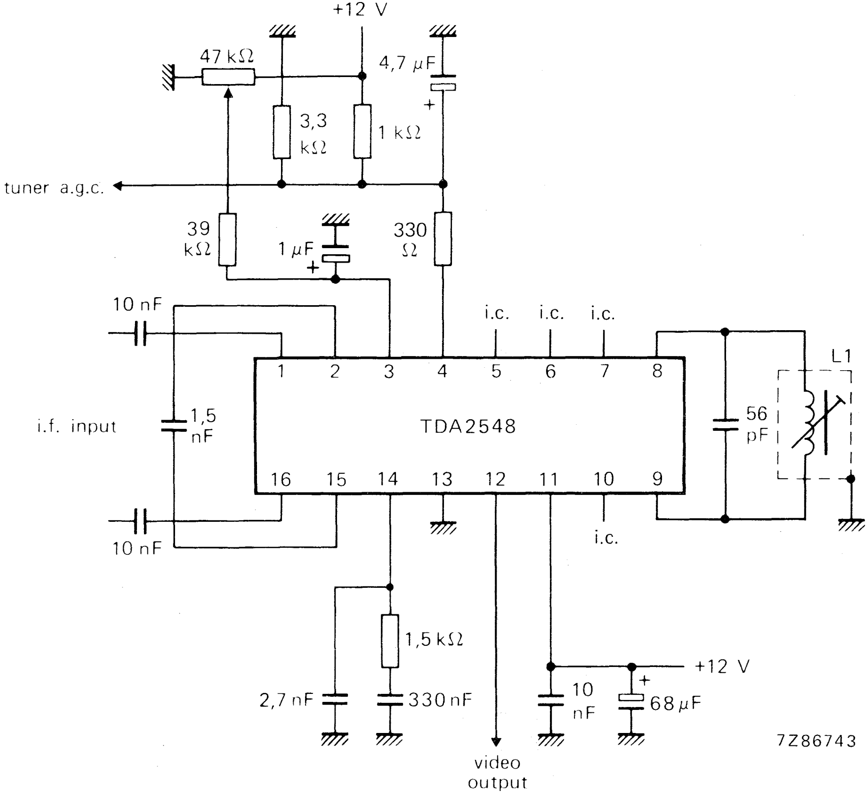


Fig. 5 Typical application circuit diagram; Q of L1 ≈ 80; f_o 38,9 MHz.

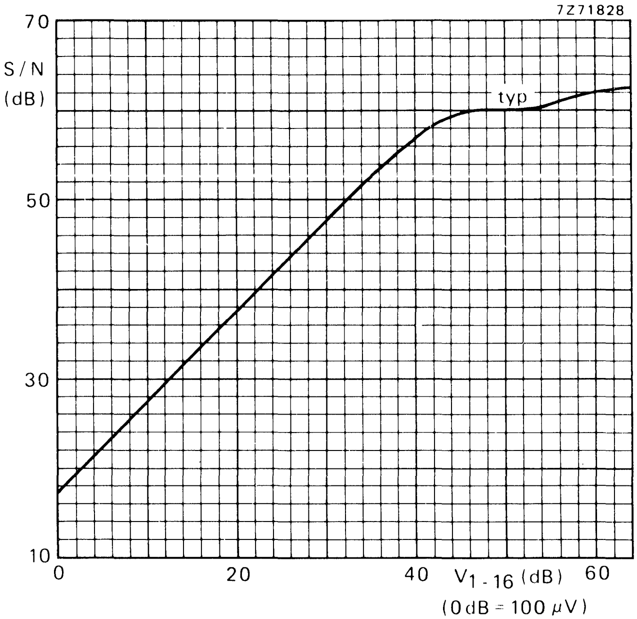


Fig. 6 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

I.F. AMPLIFIER AND DEMODULATOR FOR MULTISTANDARD TV RECEIVERS

GENERAL DESCRIPTION

The TDA2549 is a complete i.f. circuit with a.f.c., a.g.c., demodulation and video preamplification facilities for multistandard television receivers. It is capable of handling positively and negatively modulated video signals in both colour and black/white receivers.

Features

- Gain-controlled wide-band amplifier providing complete i.f. gain
- Synchronous demodulator for positive and negative modulation
- Video preamplifier with noise protection for negative modulation
- Auxiliary video input and output (75 Ω)
- Video switch to select between auxiliary video input signal and demodulated video signal
- A.F.C. circuit with on/off switch and inverter switch
- A.G.C. circuit for positive modulation (mean level) and negative modulation (noise gate)
- A.G.C. output for controlling MOSFET tuners

QUICK REFERENCE DATA

Supply voltage (pins 13 and 21)	$V_P = V_{13;21\text{-}3}$	typ.	12 V
Supply current (pins 13 and 21)	$I_P = I_{13;21\text{-}3}$	typ.	92 mA
I.F. input signal at $V_o = 2$ V (between pins 6 and 7)	$V_i = V_{6\text{-}7}$	typ.	100 μV
Video output voltage at $V_i = 0$ V (between pins 22 and 3)			
positive modulation	$V_o = V_{22\text{-}3}$	typ.	2 V
negative modulation	$V_o = V_{22\text{-}3}$	typ.	4 V
Gain control range	G_v	typ.	64 dB
Signal-to-noise ratio at $V_i = 10$ mV	S/N	typ.	56 dB
A.F.C. output voltage swing (pin 15)	$V_{15\text{-}3}$	min.	10 V
Max. tuner a.g.c. output current (pin 10)	I_{10}	min.	0,3 mA
Video bandwidth (3 dB)	B	typ.	5 MHz
Auxiliary video input voltage (pin 12) at $V_o = 2$ V (peak-to-peak value)	$V_{12\text{-}3(p\text{-}p)}$	typ.	1 V
Auxiliary video output impedance (pin 14)	$\lvert Z_{14\text{-}3}\rvert$	typ.	7 Ω
Auxiliary video output voltage (pin 14)	$V_{14\text{-}3}$	typ.	2 V

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

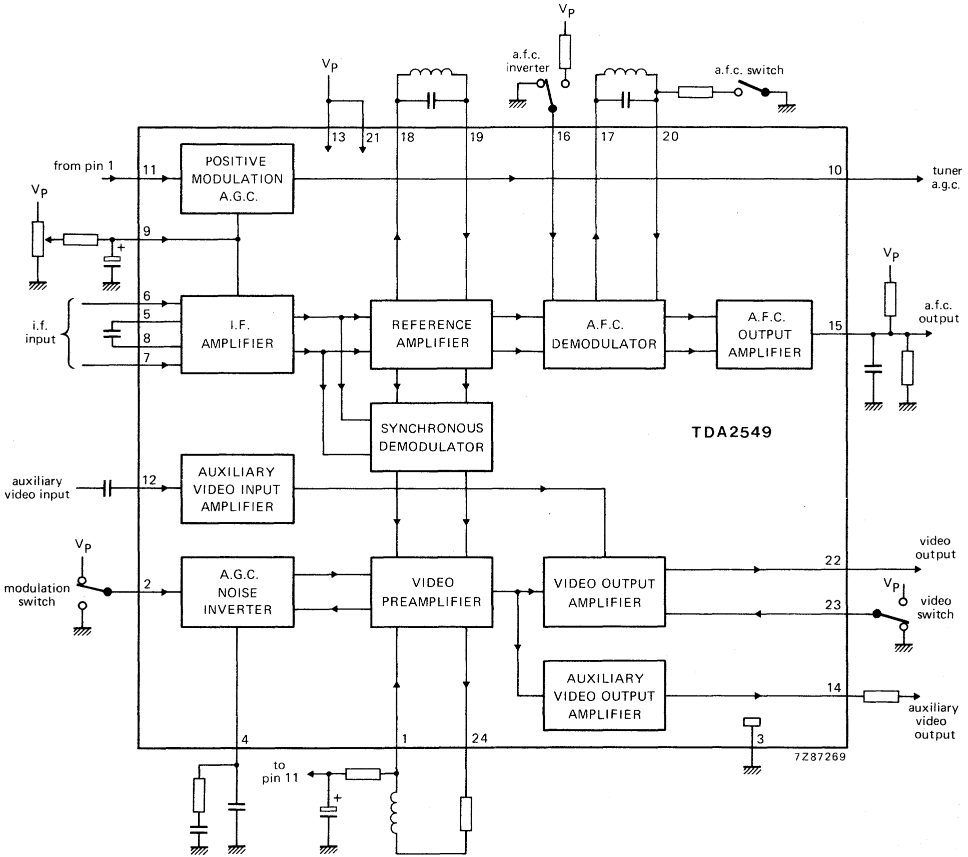


Fig. 1 Block diagram.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pins 13 and 21)	$V_P = V_{13;21\text{-}3}$	10,2 to 13,2 V
Storage temperature range	T_{stg}	−25 to +120 °C
Operating ambient temperature range	T_{amb}	−25 to +60 °C

CHARACTERISTICS (measured in Fig. 5)

$V_P = 12$ V; $T_{amb} = 25$ °C

parameter	symbol	min.	typ.	max.	unit
Supply current (pins 13 and 21)	I_P	–	92	–	mA
I.F. input signal for $V_o = 2$ V (between pins 6 and 7)	$V_i = V_{6\text{-}7}$	–	100	–	μV
Input impedance (differential)	$\lvert Z_{6\text{-}7}\rvert$	–	2	–	kΩ
Input capacitance (differential)	$C_{6\text{-}7}$	–	2	–	pF
Zero signal output level					
positive modulation	$V_{22\text{-}3}$	1,7	2	2,3	V
negative modulation	$V_{22\text{-}3}$	3,7	4	4,3	V
Top sync output level	$V_{22\text{-}3}$	1,7	2	2,3	V
Gain control range	G_v	50	64	–	dB
Signal-to-noise ratio at $V_i = 10$ mV (note 1)	S/N	50	56	–	dB
Maximum video output amplitude for positive modulation (peak-to-peak value)	$V_{22\text{-}3(p\text{-}p)}$	5	–	–	V
Bandwidth of video amplifier (3 dB)	B	–	5	–	MHz
Differential gain at $V_o = 2$ V	dG	–	4	10	%
Differential phase at $V_o = 2$ V	$d\varphi$	–	2	10	%
Residual carrier signal (r.m.s. value)	$V_{24\text{-}3(rms)}$	–	10	20	mV
Residual second harmonic of carrier signal (r.m.s. value)	$V_{24\text{-}3(rms)}$	–	20	50	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
A.F.C. output voltage swing	$V_{15\text{-}3}$	10	–	–	V
Change of frequency required for a.f.c. output voltage swing of 10 V	Δf	–	100	200	kHz
A.F.C. switch off for a voltage lower than:	$V_{17\text{-}3}$	2	2,5	–	V
A.F.C. inverter switch					
positive a.f.c. (Fig. 2)	$V_{16\text{-}3}$	0	–	1,5	V
negative a.f.c. (Fig. 3)	$V_{16\text{-}3}$	3	–	12	V
Signal expansion at G_V = 50 dB	$\Delta V_{22\text{-}3}$	–	–	0,5	dB
Negative modulation (Fig. 4)					
white spot inverter threshold level	$V_{22\text{-}3}$	–	4,6	–	V
white spot insertion level	$V_{22\text{-}3}$	–	3,1	–	V
noise inverter threshold level	$V_{22\text{-}3}$	–	0,9	–	V
noise insertion level	$V_{22\text{-}3}$	–	2,5	–	V
Positive modulation a.g.c. detector reference level	$V_{11\text{-}3}$	–	3,1	–	V
Auxiliary video input signal for $V_{o(p\text{-}p)}$ = 2 V	$V_{12\text{-}3}$	0,7	1	1,4	V
Auxiliary video output					
output signal (note 2)	$V_{14\text{-}3}$	–	1	–	V
top sync level	$V_{14\text{-}3}$	1	2	3	V
output impedance	$\lvert Z_{14\text{-}3}\rvert$	–	7	–	Ω
Levels for video switches					
positive video	$V_{2\text{-}3}$	–	–	1	V
negative video	$V_{2\text{-}3}$	3	–	–	V
internally demodulated signal	$V_{23\text{-}3}$	–	–	1	V
auxiliary video signal	$V_{23\text{-}3}$	3	–	–	V

Notes to the characteristics

1. Signal-to-noise ratio $S/N = \dfrac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.
2. Measured in application of Fig. 5.

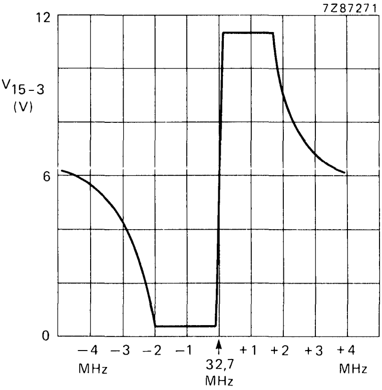


Fig. 2 A.F.C. output voltage V_{15-3} for positive a.f.c.

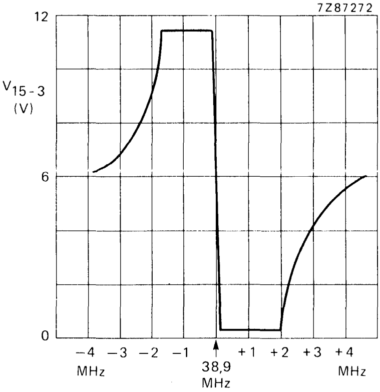


Fig. 3 A.F.C. output voltage V_{15-3} for negative a.f.c.

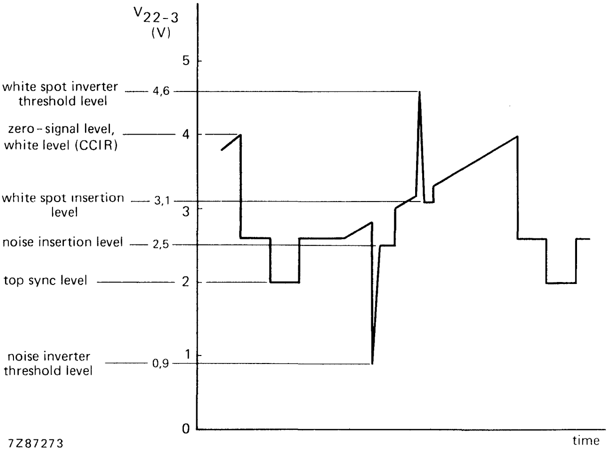


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

APPLICATION INFORMATION

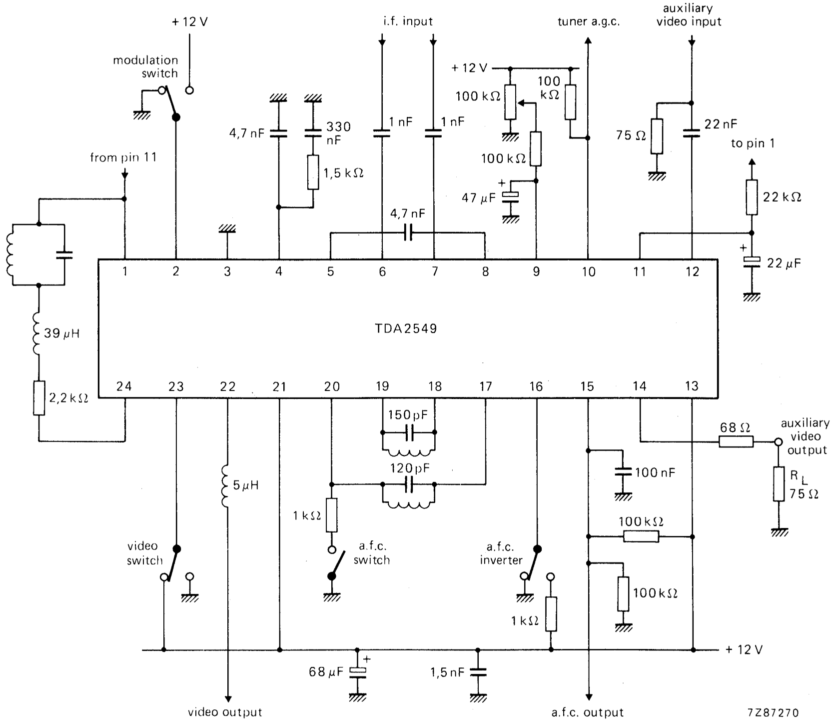


Fig. 5 Application diagram.

HORIZONTAL SYNCHRONIZATION AND VERTICAL 625 DIVIDER SYSTEM

The TDA2571A is designed in combination with the TDA2581 as a matched pair for switched-mode driven horizontal deflection stages. When supplied with a composite video signal the TDA2571A delivers drive pulses for the TDA2581 and sync pulses for the vertical deflection. The circuit is optimized for a horizontal and vertical frequency ratio of 625.

The circuit incorporates the following functions:

- Horizontal sync separator with sliding bias in such a way that the sync pulse is always sliced between top-sync level and blanking level.
- Noise gate.
- Horizontal phase detector switching to a small time constant during catching. The phase detector is gated when the oscillator is synchronized.
- Horizontal oscillator (31,25 kHz).
- Burst-key pulse generator. This pulse can also be applied as black level clamp pulse.
- Vertical sync pulse separator.
- Automatic vertical synchronization (625 divider system), without delay after channel change.

QUICK REFERENCE DATA

Supply voltage				
horizontal	$V_{12\text{-}11}$	typ.	12	V
vertical	$V_{16\text{-}11}$	typ.	12	V
Sync input voltage (peak-to-peak value)	$V_{2\text{-}11(p\text{-}p)}$		0,07 to 1	V
Slicing level		typ.	50	%
Control sensitivity of horizontal PLL		typ.	2000	Hz/μs
Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Horizontal output pulse (peak-to-peak value)	$V_{8\text{-}11(p\text{-}p)}$	typ.	11	V
Vertical sync output pulse (peak-to-peak value)	$V_{1\text{-}11(p\text{-}p)}$	typ.	11	V
Burst-key output pulse(peak-to-peak value)	$V_{13\text{-}11(p\text{-}p)}$	typ.	11	V

PACKAGE OUTLINES

TDA2571A: 16 lead DIL; plastic (SOT-38).
TDA2571AQ: 16-lead QIL; plastic (SOT-58).

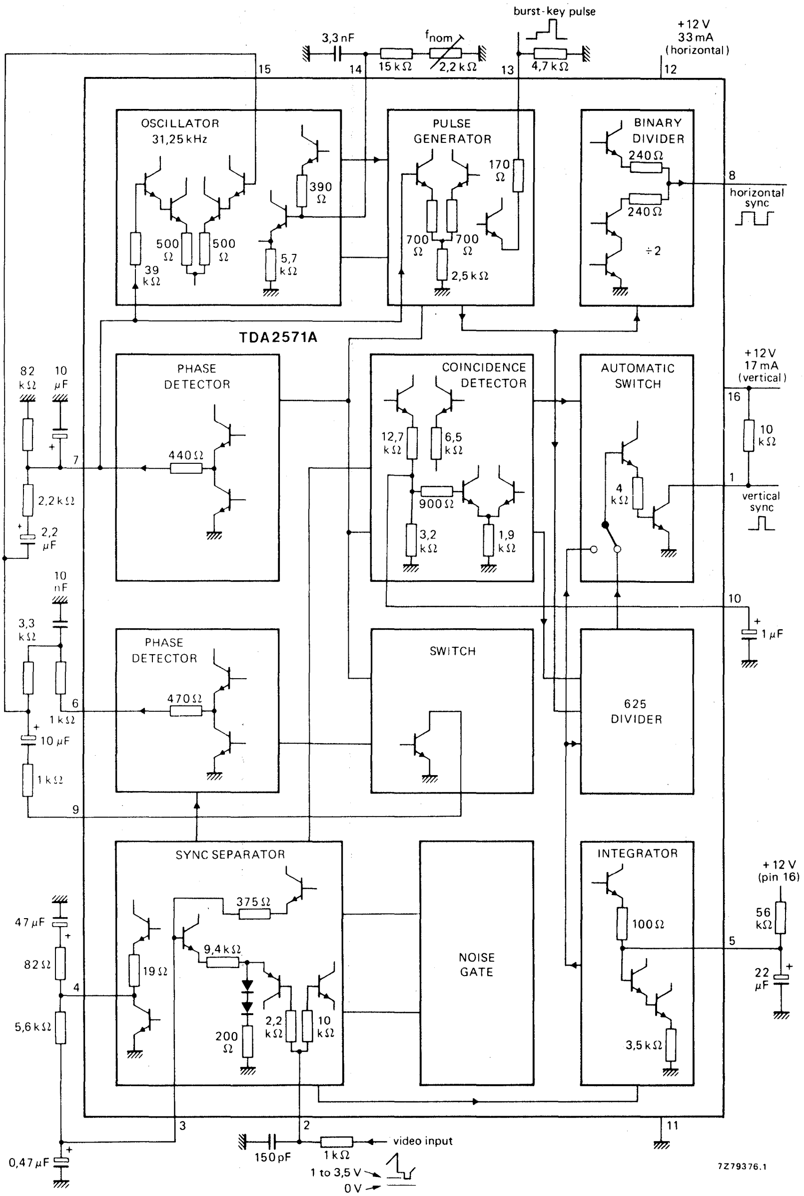


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Sypply voltage				
horizontal	$V_{12\text{-}11}$	max.	13,2	V
vertical	$V_{16\text{-}11}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1	W
Storage temperature	T_{stg}		−25 to + 130	°C
Operating ambient temperature	T_{amb}		−25 to + 65	°C

CHARACTERISTICS

At $V_{12\text{-}11}$ = 12 V; $V_{16\text{-}11}$ = 12 V; T_{amb} = 25 °C; measured in Fig. 1

Supply voltage range (pins 12 and 16)	$V_{12\text{-}11}$; $V_{16\text{-}11}$	typ.	12 10 to 13,2	V V
Current consumption	$I_{12} + I_{16}$	typ. <	50 75	mA mA

Sync separator and noise gate

Sync pulse amplitude (negative going)				
peak-to-peak value	$V_{2\text{-}11(p\text{-}p)}$		0,07 to 1	V*
Top-sync level	$V_{2\text{-}11}$		1,0 to 3,5	V
Slicing level		typ.	50	%**
Slicing level noise gating	$V_{2\text{-}11}$	typ.	0,7	V

Phase locked loop

Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Control sensitivity of horizontal PLL		typ.	2000	Hz/µs
Control sensitivity of phase detector		typ.	1,2	V/µs
Delay between sync input and detector output (pin 6)	t_d	typ.	0,4	µs
Phase modulation due to hum on the supply line		typ.	2,0	µs/V▲

---

* Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

** The slicing level is defined as the ratio of the amplitude of the slicing level to black level to the amplitude of the sync pulse.

▲ The voltage is a peak-to-peak value; the figure given can be reduced to 0,6 µs/V(p-p) by means of an extra capacitor of 330 nF between pins 12 and 7.

CHARACTERISTICS (continued)

Horizontal oscillator

Frequency; free running	f_o	typ.	31,250	kHz
Frequency at output pin 8	f_8	typ.	15,625	kHz
Spread of frequency without spread of external components	Δf_o	$<$	4	%
Temperature coefficient	T	typ.	$2,5 \times 10^{-4}$	K^{-1}
Change of frequency when $V_{12\text{-}11}$ drops to 6 V	Δf_o	$<$	10	%
Change of frequency when $V_{12\text{-}11}$ increases from 10 to 13,2 V	Δf_o	$<$	0,5	%
Output voltage; no load (peak-to-peak value)	$V_{8\text{-}11(p\text{-}p)}$	$>$	10	V
Output resistance	$R_{8\text{-}11}$	typ.	300	Ω
Output current range (peak-to-peak value)	$I_{8(p\text{-}p)}$		0 to 40	mA
Duty factor of output pulse	δ	typ.	46	%*
Delay between falling edge of output pulse and end of sync pulse at pin 2	t_d	typ.	0,9	μs**

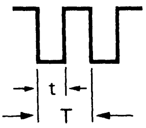
Burst-key pulse

Output voltage (peak-to-peak value)	$V_{13\text{-}11(p\text{-}p)}$	$>$	10	V
Duration of upper part of output pulse	t_p	typ.	3,6	μs**
Duration of lower part of output pulse	t_p	typ.	9,1	μs**
Amplitude of lower part of output pulse	$V_{13\text{-}11(p\text{-}p)}$	typ.	3	V**
Output resistance	$R_{13\text{-}11}$	typ.	200	Ω
Delay between the end of the sync pulse at pin 2 and the rising edge of the burst key pulse	t_d	typ.	0,9	μs**

Coincidence detector

Voltage level of time constant switch	$V_{10\text{-}11}$	typ.	2,0	V
Voltage when the oscillator is in sync	$V_{10\text{-}11}$	typ.	0,4	V
Voltage when the oscillator is out-of-sync	$V_{10\text{-}11}$	typ.	2,5	V
Voltage during noise	$V_{10\text{-}11}$	typ.	1,0	V

* The duty factor is specified as follows:



$$\delta = \frac{t}{T} \times 100\%.$$

** See waveforms Fig. 2.

Vertical sync pulse

Output voltage (peak-to-peak value)	$V_{1\text{-}11(p\text{-}p)}$	>	10	V
Duration of output pulse during indirect synchronization	t_p	typ.	170	μs
Duration of output pulse during direct synchronization (coincidence detector high)	t_p	typ.	160	μs
Load resistor to pin 2	R_L	>	2	kΩ
Output voltage low with $R_L = 2\ \text{k}\Omega$	$V_{1\text{-}11}$	<	500	mV
Ratio between basic horizontal oscillator frequency and vertical pulse			625	*

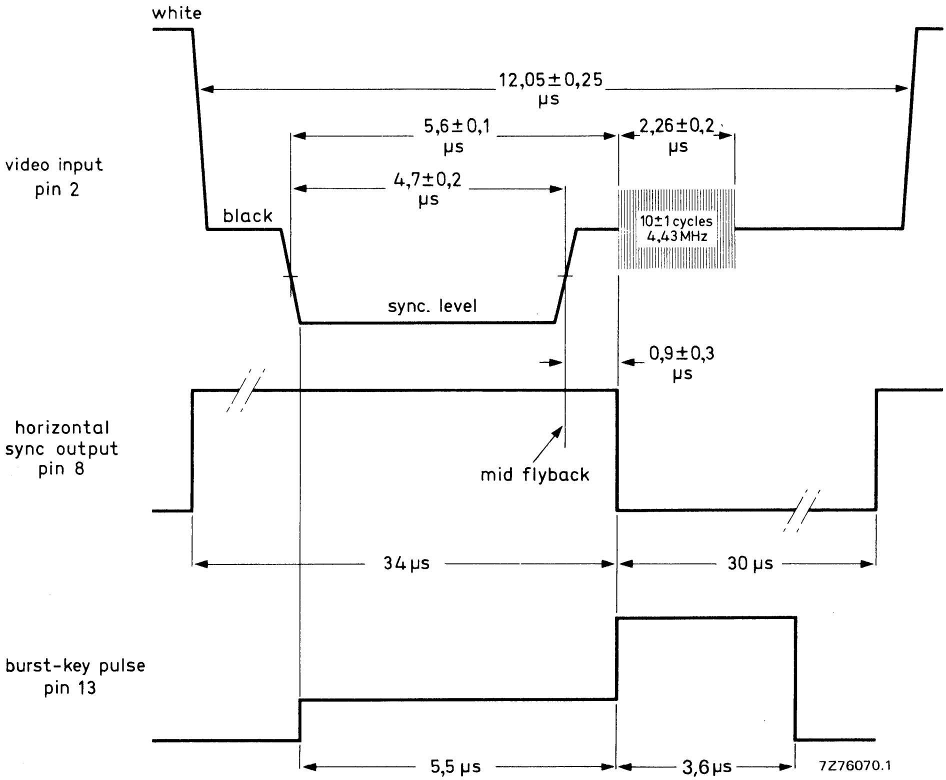


Fig. 2 Relationship between the video input signal to the TDA2571A and the horizontal sync and burst-key pulse output.

---

* When a non-standard sync signal is applied the separated vertical sync pulse of the incoming signal is connected to pin 1; the pulse of the divider circuit is switched off.

PINNING

1. Vertical sync pulse output
2. Video input
3. Sync separator slicing level output
4. Black level detector output
5. Vertical integrator bias network
6. Horizontal phase detector output
7. Reference voltage horizontal frequency control stage
8. Horizontal sync pulse output
9. Time constant switch
10. Coincidence detector output
11. Negative supply (ground)
12. Positive supply (horizontal)
13. Burst-key pulse output
14. RC-network horizontal oscillator
15. Control horizontal oscillator
16. Positive supply (vertical)

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1. Vertical sync pulse output

   A resistor of about 10 kΩ must be connected between pin 1 and the positive supply line (pin 16; vertical supply).

   The output pulse will come from the 625 divider stage (standard signal) or from the vertical sync pulse separator (non-standard signal), depending on the input signal on pin 2. The standard and non-standard signals are detected automatically.

2. Video input

   The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation.

   The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,07 to 1 V. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 70 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

   The noise gate is activated at an input level < 0,7 V, thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V. When i.f. circuits with a noise gate are used (e.g. TDA2540; TDA2541) the noise gate of the TDA2571A is not required.

3. Sync separator slicing level output

   The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 4. The capacitor connected to pin 3 must be about 0,47 μF.

4. Black level detector output

   The black level of the input signal is detected on this pin, which is required to obtain good sync separator operation. A capacitor of 47 μF in series with a resistor of 82 Ω has to be connected to this pin. A 5,6 kΩ resistor must be connected between pins 3 and 4.

5. Vertical sync pulse integrator bias network

   The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external RC-network is required for the correct biasing of this circuit for various input conditions. Typical values are: R = 56 kΩ; C = 22 μF.

6. Horizontal phase detector output

   The control voltage for the horizontal oscillator is obtained on this pin. The output current is about 2 mA.

7. Reference voltage horizontal frequency control stage

   This pin has two functions. It is used to decouple the reference voltage for the frequency control of the horizontal oscillator (so a good suppression of interference is obtained which may be present on the supply line). This pin is also used to control the reference waveform for the phase detector to the middle of the gating, giving a good noise immunity of the synchronization.

8. Horizontal sync pulse output

   This pulse is obtained from the horizontal oscillator via a divider circuit. The duty factor is 46%. The falling edge of this pulse has a delay of 0,9 μs with respect to the end of the sync pulse. Because of this phase relationship this pulse can directly drive the TDA2581.

9. Time constant switch
   This pin is used to switch the time constant of the flywheel filter. The pin condition is determined by the coincidence detector (pin 10). During in-sync or when only noise is received pin 9 assumes ground level, which results in a long time constant and good noise immunity.

   During out-of-sync or VCR playback, pin 9 has a high impedance and consequently only the short time constant is available. In this condition a large catching range is obtained.

10. Coincidence detector output

    A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.
    The following output voltages can occur:
    – when in-sync: 0,4 V
    – when out-of-sync: 2,0 V
    – during noise at input: 1,0 V

    When the output voltage < 1,85 V, the flywheel filter is switched to a long time constant, and the gating of the phase detector is switched-on.

    For a voltage > 1,85 V, the flywheel filter has a short time constant, and the gating of the phase detector is switched-off. The result is that during noise the flywheel time constant remains long thus preventing large shifts in the frequency of the horizontal oscillator (and screening of the horizontal output transformer).

    The information of the line coincidence detector is fed to the divider circuit so that there is no delay in vertical synchronization after a channel change, or an unsynchronized camera change in the studio. Thus, the divider circuit is reset to direct sync, when line synchronization is lost.

    The time constant value can be switched manually by a resistor (10 kΩ) to + 12 V.

11. Negative supply (ground)

12. Positive supply horizontal oscillator

    Interference and hum on this supply line can affect the oscillator frequency. It is therefore necessary to have a separate decoupling of this pin with respect to pin 16. The current-draw of this pin is typically 33 mA.

13. Burst-key pulse output

    This pulse is composed of two parts. The lower part has an amplitude of 3 V peak-to-peak and a width of 9,1 μs (for phase relation see Fig. 2). The upper part has a total amplitude in excess of 10 V peak-to-peak and a width of 3,6 μs.The leading edge of this pulse has a delay of 0,9 μs with respect to the falling edge of the sync pulse at the input (pin 2).

    This pulse can directly drive the burst gate/black level clamp input of the TDA2560.

APPLICATION INFORMATION (continued)

14. RC-network horizontal oscillator

    Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part should be as small as possible, because of poor stability of variable carbon resistors.

    The oscillator can be adjusted when pins 7 and 15 are short-circuited.

15. Horizontal oscillator control pin

16. Positive supply sync separator and divider circuit (vertical)

    For this supply only a simple decoupling is required. The current-draw of this pin is typically 17 mA.

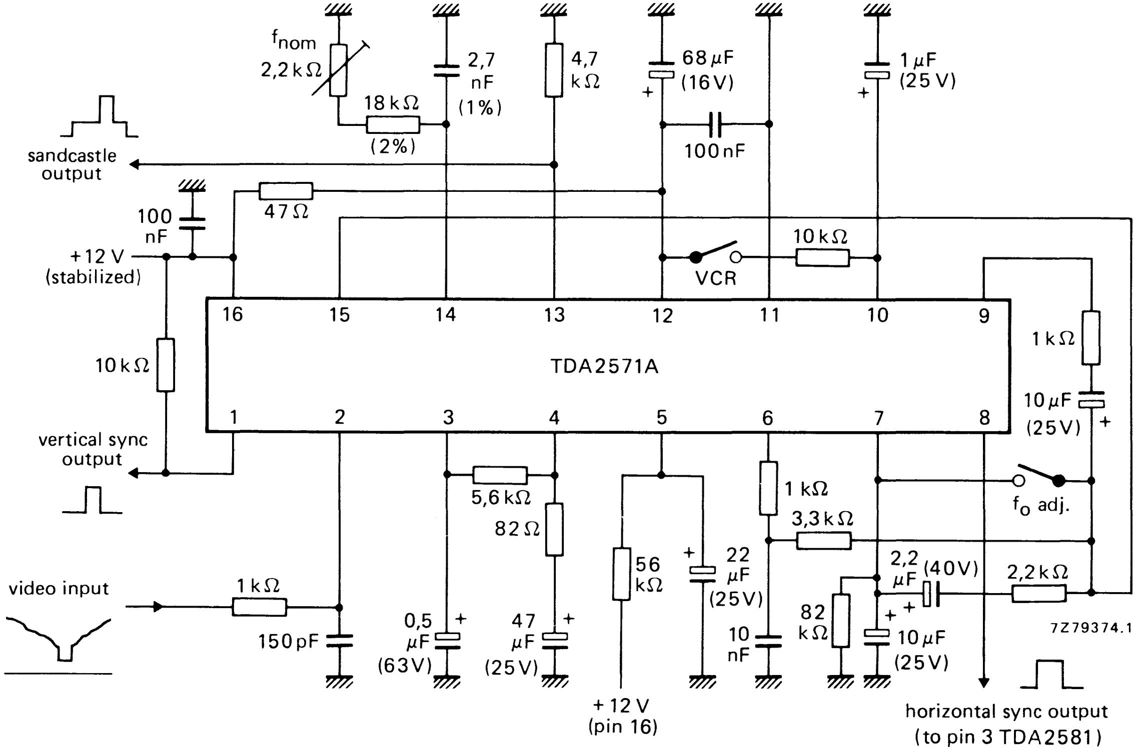


Fig. 3 Typical application circuit diagram; for combination of the TDA2571A with the TDA2581 see Fig. 4.

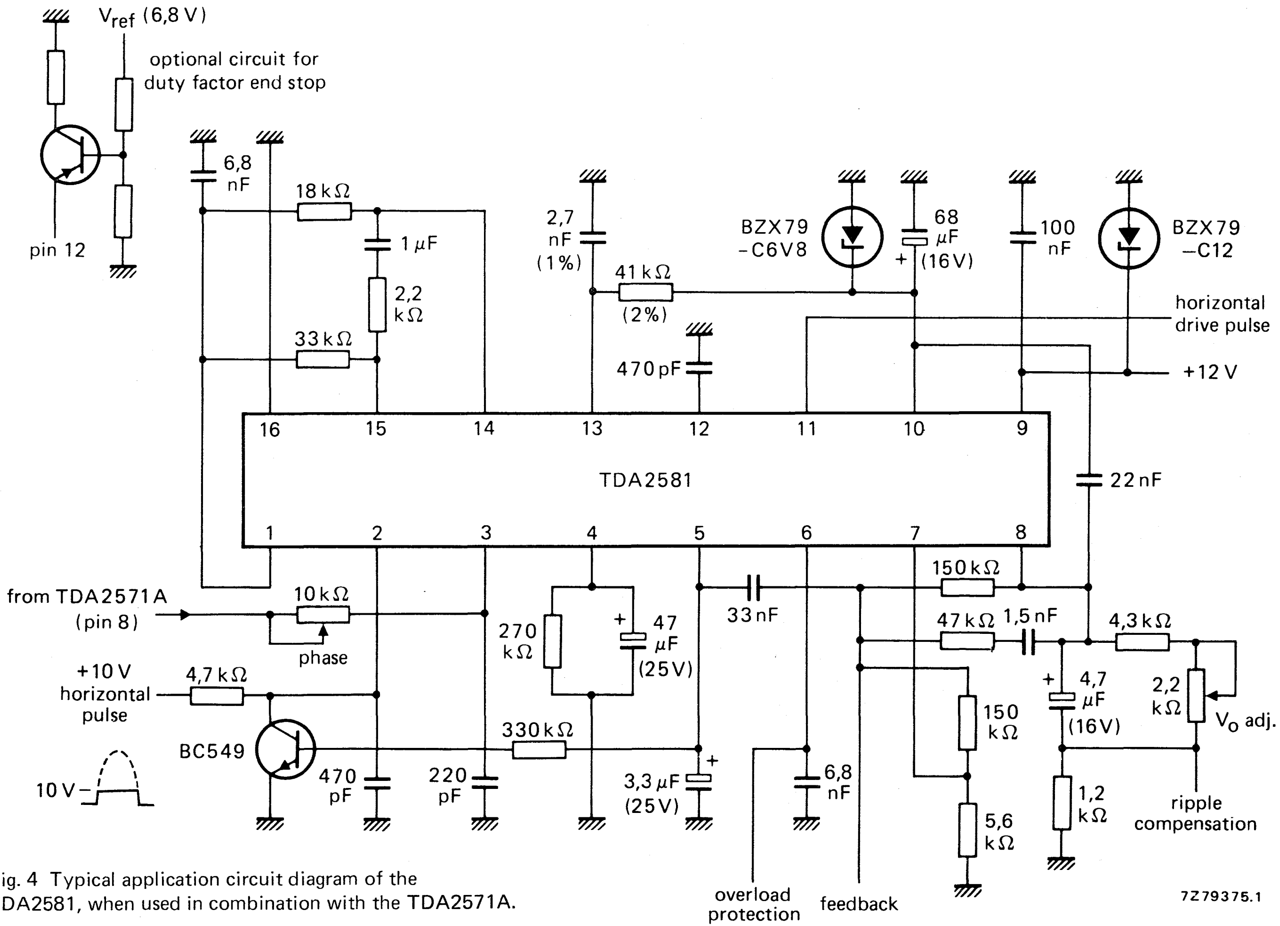


Fig. 4 Typical application circuit diagram of the TDA2581, when used in combination with the TDA2571A.

HORIZONTAL SYNCHRONIZATION AND VERTICAL 525 DIVIDER SYSTEM

The TDA2575A is designed in combination with the TDA2581 as a matched pair for switched-mode driven horizontal deflection stages. When supplied with a composite video signal the TDA2575A delivers drive pulses for the TDA2581 and sync pulses for the vertical deflection. The circuit is optimized for a horizontal and vertical frequency ratio of 525.

The circuit incorporates the following functions:
- Horizontal sync separator with sliding bias in such a way that the sync pulse is always sliced between top-sync level and blanking level.
- Noise gate.
- Horizontal phase detector switching to a small time constant during catching. The phase detector is gated when the oscillator is synchronized.
- Horizontal oscillator (31,5 kHz).
- Burst-key pulse generator. This pulse can also be applied as black level clamp pulse.
- Vertical sync pulse separator.
- Automatic vertical synchronization (525 divider system), without delay after channel change.

QUICK REFERENCE DATA

Supply voltage				
horizontal	V_{12-11}	typ.	12	V
vertical	V_{16-11}	typ.	12	V
Sync input voltage (peak-to-peak value)	$V_{2-11(p-p)}$		0,07 to 1	V
Slicing level		typ.	50	%
Control sensitivity of horizontal PLL		typ.	2000	Hz/μs
Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Horizontal output pulse (peak-to-peak value)	$V_{8-11(p-p)}$	typ.	11	V
Vertical sync output pulse (peak-to-peak value)	$V_{1-11(p-p)}$	typ.	11	V
Burst-key output pulse (peak-to-peak value)	$V_{13-11(p-p)}$	typ.	11	V

PACKAGE OUTLINES

TDA2575A : 16-lead DIL; plastic (SOT-38).
TDA2575AQ: 16-lead QIL; plastic (SOT-58).

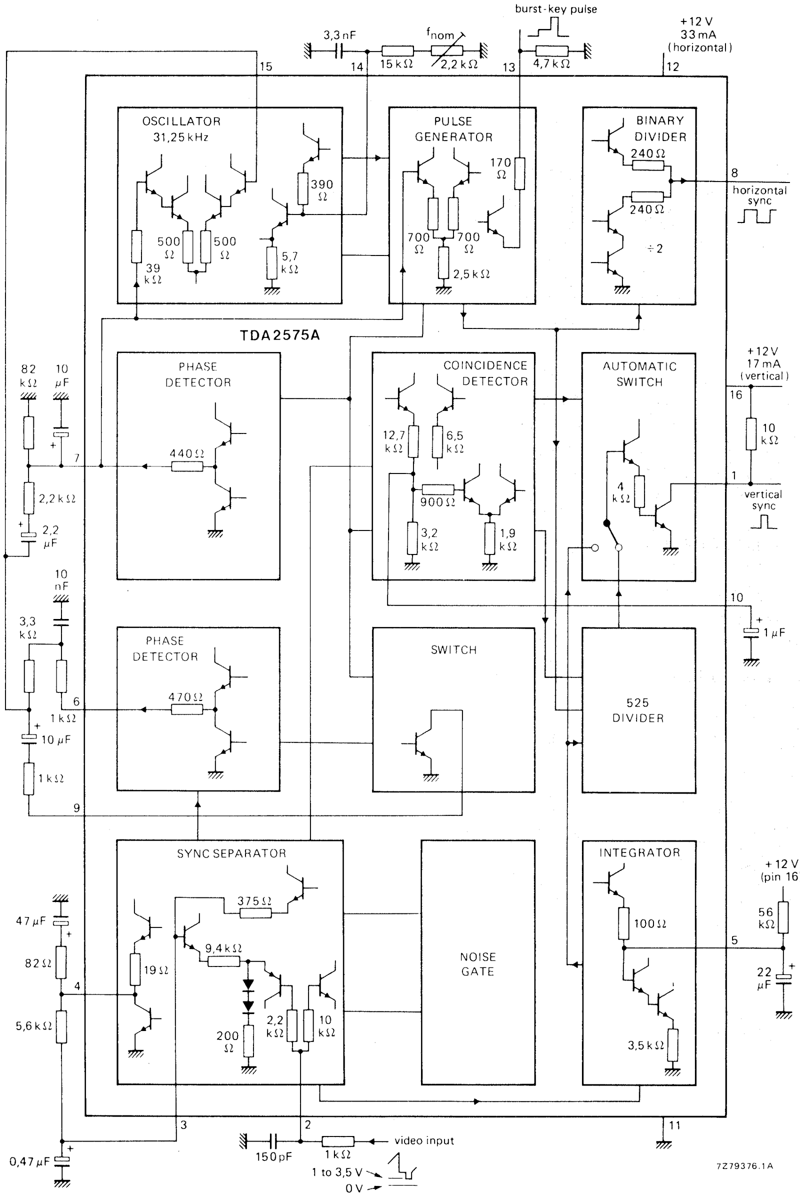


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage				
horizontal	$V_{12\text{-}11}$	max.	13,2	V
vertical	$V_{16\text{-}11}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1	W
Storage temperature	T_{stg}		−25 to + 130	°C
Operating ambient temperature	T_{amb}		−25 to + 65	°C

CHARACTERISTICS

At $V_{12\text{-}11} = 12$ V; $V_{16\text{-}11} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

Supply voltage range (pins 12 and 16)	$V_{12\text{-}11}$; $V_{16\text{-}11}$	typ.	12	V
			10 to 13,2	V
Current consumption	$I_{12} + I_{16}$	typ.	50	mA
		$<$	75	mA

Sync separator and noise gate

Sync pulse amplitude (negative going)				
peak-to-peak value	$V_{2\text{-}11(p\text{-}p)}$		0,07 to 1	V *
Top-sync level	$V_{2\text{-}11}$		1,0 to 3,5	V
Slicing level		typ.	50	% **
Slicing level noise gating	$V_{2\text{-}11}$	typ.	0,7	V

Phase locked loop

Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Control sensitivity of horizontal PLL		typ.	2000	Hz/µs
Control sensitivity of phase detector		typ.	1,2	V/µs
Delay between sync input and detector output (pin 6)	t_d	typ.	0,4	µs
Phase modulation due to hum on the supply line		typ.	2,0	µs/V ▲

---

* Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

** The slicing level is defined as the ratio of the amplitude of the slicing level to black level to the amplitude of the sync pulse.

▲ The voltage is a peak-to-peak value; the figure given can be reduced to 0,6 µs/V (p-p) by means of an extra capacitor of 330 nF between pins 12 and 7.

CHARACTERISTICS (continued)

Horizontal oscillator

Frequency; free running	f_o	typ.	31,500	kHz
Frequency at output pin 8	f_8	typ.	15,750	kHz
Spread of frequency without spread of external components	Δf_o	$<$	4	%
Temperature coefficient	T	typ.	$2,5 \times 10^{-4}$	K^{-1}
Change of frequency when $V_{12\text{-}11}$ drops to 6 V	Δf_o	$<$	10	%
Change of frequency when $V_{12\text{-}11}$ increases from 10 to 13,2 V	Δf_o	$<$	0,5	%
Output voltage; no load (peak-to-peak value)	$V_{8\text{-}11(p\text{-}p)}$	$>$	10	V
Output resistance	$R_{8\text{-}11}$	typ.	300	Ω
Output current range (peak-to-peak value)	$I_{8(p\text{-}p)}$		0 to 40	mA
Duty factor of output pulse	δ	typ.	46	% *
Delay between falling edge of output pulse and end of sync pulse at pin 2	t_d	typ.	0,9	µs **

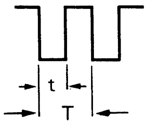
Burst-key pulse

Output voltage (peak-to-peak value)	$V_{13\text{-}11(p\text{-}p)}$	$>$	10	V
Duration of upper part of output pulse	t_p	typ.	3,6	µs **
Duration of lower part of output pulse	t_p	typ.	9,1	µs **
Amplitude of lower part of output pulse	$V_{13\text{-}11(p\text{-}p)}$	typ.	3	V **
Output resistance	$R_{13\text{-}11}$	typ.	200	Ω
Delay between the end of the sync pulse at pin 2 and the rising edge of the burst key pulse	t_d	typ.	0,9	µs **

Coincidence detector

Voltage level of time constant switch	$V_{10\text{-}11}$	typ.	2,0	V
Voltage when the oscillator is in sync	$V_{10\text{-}11}$	typ.	0,4	V
Voltage when the oscillator is out-of-sync	$V_{10\text{-}11}$	typ.	2,5	V
Voltage during noise	$V_{10\text{-}11}$	typ.	1,0	V

* The duty factor is specified as follows:



$$\delta = \frac{t}{T} \times 100\%.$$

** See waveforms Fig. 2.

Vertical sync pulse

Output voltage (peak-to-peak value)	$V_{1\text{-}11(p\text{-}p)}$	>	10	V
Duration of output pulse during indirect synchronization	t_p	typ.	170	μs
Duration of output pulse during direct synchronization (coincidence detector high)	t_p	typ.	190	μs
Load resistor to pin 2	R_L	>	2	kΩ
Output voltage low with R_L = 2 kΩ	$V_{1\text{-}11}$	<	500	mV
Ratio between basic horizontal oscillator frequency and vertical pulse			525	*

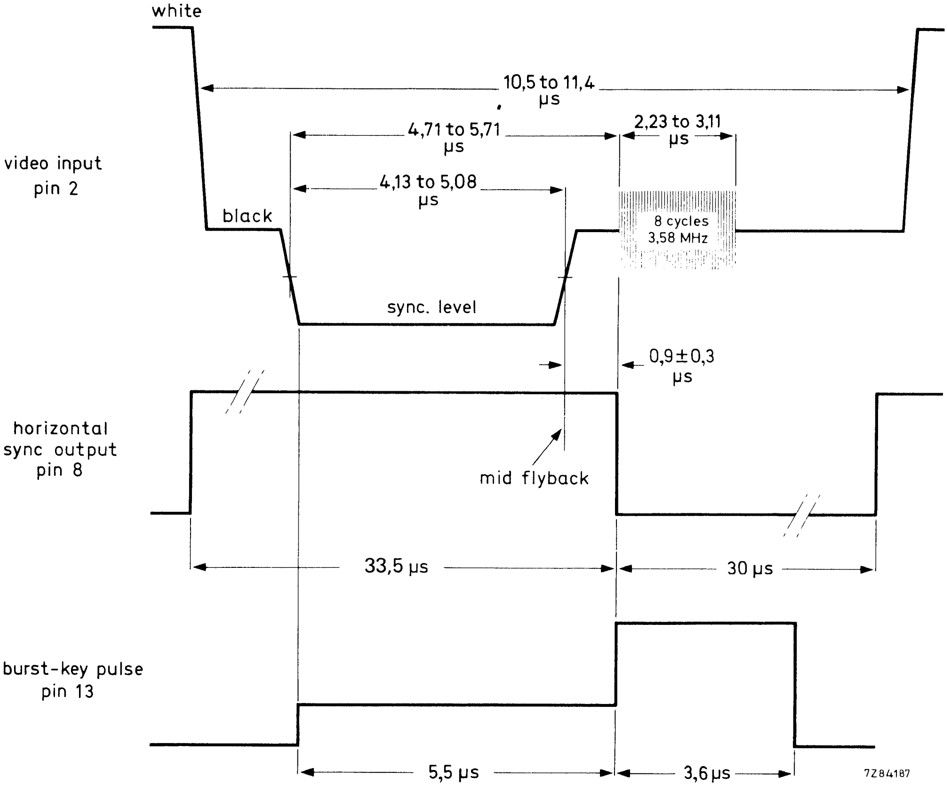


Fig. 2 Relationship between the video input signal to the TDA2575A and the horizontal sync and burst-key pulse output.

* When a non-standard sync signal is applied the separated vertical sync pulse of the incoming signal is connected to pin 1; the pulse of the divider circuit is switched off.

PINNING

1. Vertical sync pulse output
2. Video input
3. Sync separator slicing level output
4. Black level detector output
5. Vertical integrator bias network
6. Horizontal phase detector output
7. Reference voltage horizontal frequency control stage
8. Horizontal sync pulse output
9. Time constant switch
10. Coincidence detector output
11. Negative supply (ground)
12. Positive supply (horizontal)
13. Burst-key pulse output
14. RC-network horizontal oscillator
15. Control horizontal oscillator
16. Positive supply (vertical)

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1. Vertical sync pulse output

   A resistor of about 10 kΩ must be connected between pin 1 and the positive supply line (pin 16; vertical supply).

   The output pulse will come from the 525 divider stage (standard signal) or from the vertical sync pulse separator (non-standard signal), depending on the input signal on pin 2. The standard and non-standard signals are detected automatically.

2. Video input

   The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation.

   The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,07 to 1 V. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 70 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

   The noise gate is activated at an input level $< 0,7$ V, thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V. When i.f. circuits with a noise gate are used (e.g. TDA2540; TDA2541) the noise gate of the TDA2575A is not required.

3. Sync separator slicing level output

   The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 4. The capacitor connected to pin 3 must be about 0,47 μF.

4. Black level detector output

   The black level of the input signal is detected on this pin, which is required to obtain good sync separator operation. A capacitor of 47 μF in series with a resistor of 82 Ω has to be connected to this pin. A 5,6 kΩ resistor must be connected between pins 3 and 4.

5. Vertical sync pulse integrator bias network

   The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external RC-network is required for the correct biasing of this circuit for various input conditions. Typical values are: R = 56 kΩ; c = 22 μF.

6. Horizontal phase detector output

   The control voltage for the horizontal oscillator is obtained on this pin. The output current is about 2 mA.

7. Reference voltage horizontal frequency control stage

   This pin has two functions. It is used to decouple the reference voltage for the frequency control of the horizontal oscillator (so a good suppression of interference is obtained which may be present on the supply line). This pin is also used to control the reference waveform for the phase detector to the middle of the gating, giving a good noise immunity of the synchronization.

8. Horizontal sync pulse output

   This pulse is obtained from the horizontal oscillator via a divider circuit. The duty factor is 46%. The falling edge of this pulse has a delay of 0,9 μs with respect to the end of the sync pulse. Because of this phase relationship this pulse can directly drive the TDA2581.

9. Time constant switch

   This pin is used to switch the time constant of the flywheel filter. The pin condition is determined by the coincidence detector (pin 10). During in-sync or when only noise is received pin 9 assumes ground level, which results in a long time constant and good noise immunity.

   During out-of-sync or VCR playback, pin 9 has a high impedance and consequently only the short time constant is available. In this condition a large catching range is obtained.

10. Coincidence detector output

    A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.
    The following output voltages can occur:
    – when in-sync: 0,4 V
    – when out-of-sync: 2,0 V
    – during noise at input: 1,0 V

    When the output voltage $< 1,85$ V, the flywheel filter is switched to a long time constant, and the gating of the phase detector is switched-on.

    For a voltage $> 1,85$ V, the flywheel filter has a short time constant, and the gating of the phase detector is switched-off. The result is that during noise the flywheel time constant remains long thus preventing large shifts in the frequency of the horizontal oscillator (and screening of the horizontal output transformer).

    The information of the line coincidence detector is fed to the divider circuit so that there is no delay in vertical synchronization after a channel change, or an unsynchronized camera change in the studio. Thus, the divider circuit is reset to direct sync, when line synchronization is lost.

    The time constant value can be switched manually by a resistor (10 kΩ) to + 12 V.

11. Negative supply (ground)

12. Positive supply horizontal oscillator

    Interference and hum on this supply line can affect the oscillator frequency. It is therefore necessary to have a separate decoupling of this pin with respect to pin 16. The current-draw of this pin is typically 33 mA.

13. Burst-key pulse output

    This pulse is composed of two parts. The lower part has an amplitude of 3 V peak-to-peak and a width of 9,1 μs (for phase relation see Fig. 2). The upper part has a total amplitude in excess of 10 V peak-to-peak and a width of 3,6 μs. The leading edge of this pulse has a delay of 0,9 μs with respect to the falling edge of the sync pulse at the input (pin 2).

    This pulse can directly drive the burst gate/black level clamp input of the TDA2560.

APPLICATION INFORMATION (continued)

14. RC-network horizontal oscillator

    Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part should be as small as possible, because of poor stability of variable carbon resistors.

    The oscillator can be adjusted when pins 7 and 15 are short-circuited.

15. Horizontal oscillator control pin

16. Positive supply sync separator and divider circuit (vertical)

    For this supply only a simple decoupling is required. The current-draw of this pin is typically 17 mA.

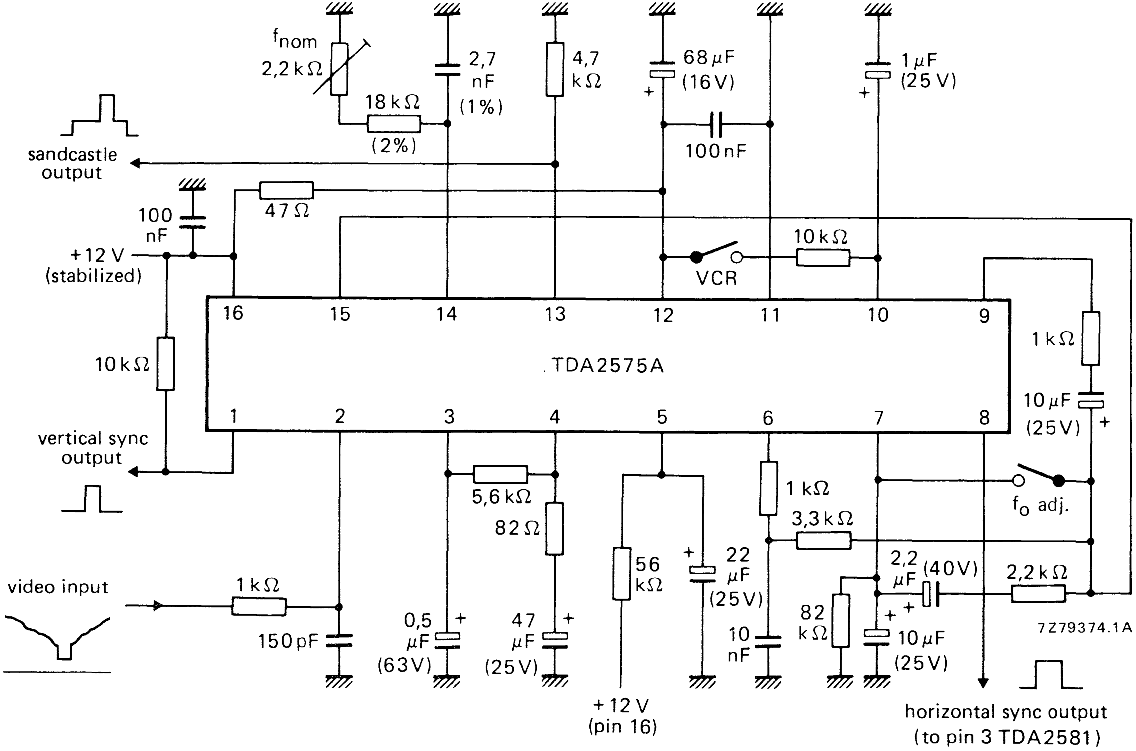


Fig. 3 Typical application circuit diagram; for combination of the TDA2575A with the TDA2581 see Fig. 4.

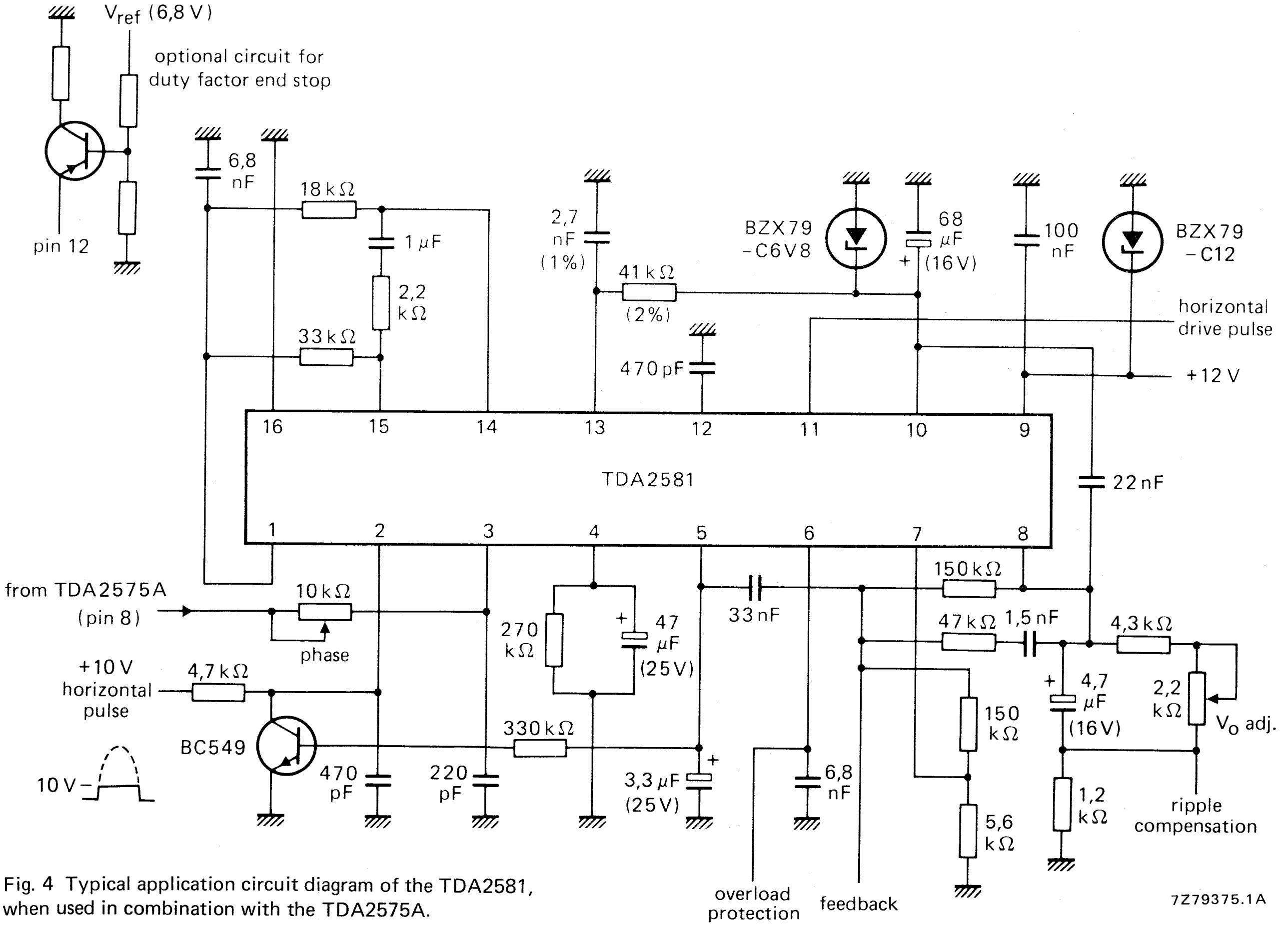


Fig. 4 Typical application circuit diagram of the TDA2581, when used in combination with the TDA2575A.

HORIZONTAL OSCILLATOR COMBINATION WITH VERTICAL 625 DIVIDER SYSTEM

The TDA2576A is a horizontal oscillator combination intended to be used in various types of transistorized horizontal deflection circuits, e.g. switched-mode driven and power-pack system circuits.

The circuit is optimized for a horizontal and vertical frequency ratio of 625.

The circuit incorporates the following functions:

- Horizontal sync separator with sliding bias in such way that the sync pulse is always sliced between top-sync level and blanking level.
- Noise gate.
- Phase detector which compares the sync pulse with the oscillator voltage; this phase detector is gated.
- Phase detector which compares the line flyback pulse with the oscillator voltage.
- Horizontal oscillator (31,25 kHz).
- Time constant switching of the first control loop (short time constant during catching and reception of VCR signals).
- Burst key pulse generator (sandcastle pulse with three levels).
- Vertical sync pulse separator.
- Very stable vertical synchronization due to the 625 divider system, without delay after channel change.

QUICK REFERENCE DATA

Supply voltage	$V_{16\text{-}9}$	typ.	12	V
Supply current consumption	I_{16}	typ.	53	mA
Sync input voltage (peak-to-peak value)	$V_{4\text{-}9(p\text{-}p)}$		0,1 to 1	V
Slicing level		typ.	50	%
Control sensitivity sync to flyback		typ.	10	kHz/μs
Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Horizontal output pulse (peak-to-peak value)	$V_{10\text{-}9(p\text{-}p)}$	typ.	11	V
Vertical output pulse; pin 2 (peak-to-peak value)	$V_{2\text{-}9(p\text{-}p)}$	typ.	11	V
Sandcastle output pulse (peak-to-peak value)	$V_{14\text{-}9(p\text{-}p)}$	typ.	11	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

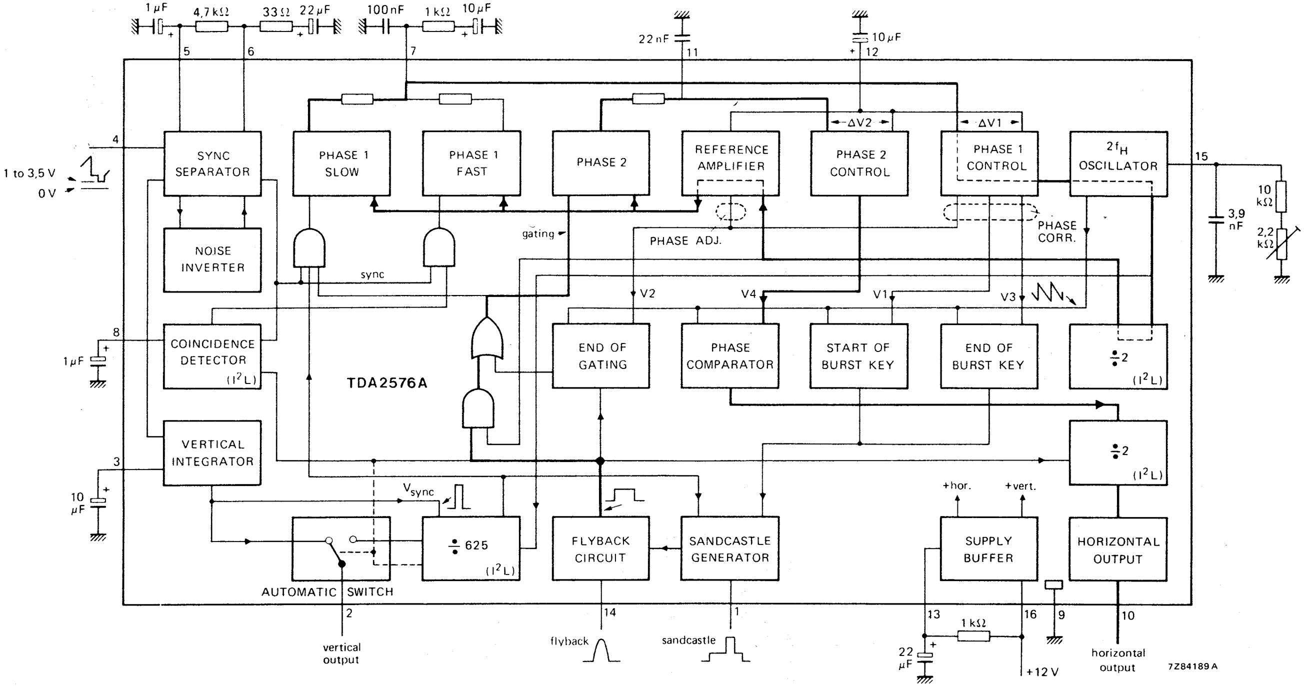


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{16\text{-}9}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1	W
Storage temperature	T_{stg}		−55 to + 125	°C
Operating ambient temperature	T_{amb}		−25 to + 65	°C

CHARACTERISTICS

$V_{16\text{-}9}$ = 12 V; T_{amb} = 25 °C; measured in Fig. 2.

Supply voltage	$V_{16\text{-}9}$	typ.	12	V
			10 to 13,2	V
Supply current consumption	I_{16}	typ.	53	mA
		<	70	mA

Sync separator and noise gate

Sync pulse amplitude (negative going) peak-to-peak value	$V_{4\text{-}9(p\text{-}p)}$		0,1 to 1	V*
Top-sync level	$V_{4\text{-}9}$		1,0 to 3,5	V
Slicing level noise gate	$V_{4\text{-}9}$	<	1	V
Delay between sync input and detector output (pin 7)		typ.	0,35	μs

First control loop (sync-to-oscillator)

Holding range	Δf	typ.	± 1000	Hz
Catching range	Δf	typ.	± 900	Hz
Control sensitivity video				
with respect to oscillator		typ.	2,0	kHz/μs
with respect to sandcastle		typ.	10,0	kHz/μs
with respect to flyback pulse		typ.	10,0	kHz/μs
Phase modulation due to hum on the supply line (pin 16)		<	1,0	μs/V**

Second control loop (oscillator-to-flyback)

Control sensitivity	$\Delta t_d/\Delta t_o$	typ.	250	▲
Control range	t_d	<	26	μs

---

* Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

** This voltage is a peak-to-peak value.

▲ t_d = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.

t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (I_7).

CHARACTERISTICS (continued)

Horizontal oscillator

Frequency; free running	f_o	typ.	31,250	kHz
Frequency at output pin 10	f_{10}	typ.	15,625	kHz
Spread of frequency without spread of external components	Δf_o	<	4	%
Temperature coefficient	T	typ.	$2,5 \times 10^{-4}$	
Change of frequency when $V_{16\text{-}9}$ increases from 10 to 13,2 V	Δf_o	<	0,5	%
Minimum supply voltage (+ hor. see Fig. 1)		typ.	7	V
Frequency deviation at min. supply voltage		<	10	%

Horizontal output (pin 10)

Maximum supply voltage		<	13,2	V
Minimum output voltage at a current of 60 mA	$V_{10\text{-}9}$	<	700	mV
Maximum output current	I_{10}	<	60	mA
Duration of the output pulse	t_p		12 to 38	μs

Sandcastle pulse (pin 1)

Output voltage during burst key pulse	$V_{1\text{-}9}$	>	10	V
Pulse duration	t_p	typ.	4,0	μs
Amplitude of second level of output pulse	$V_{1\text{-}9}$	typ.	4,5	V
Pulse duration	flyback pulse			
Amplitude of third level of output pulse	$V_{1\text{-}9}$	typ.	2,5	V
Pulse duration	t_p	typ.	1,34	μs*
Delay between the start of the sync pulse at the video input (pin 4) and the rising edge of the burst key pulse	t_d	typ.	4,9	μs

Phase adjustment (pin 12)

Voltage at pin 12	$V_{12\text{-}9}$	typ.	2,8	V
Control sensitivity		typ.	0,6	V/μs
Control range		typ.	± 1	μs

Coincidence detector (pin 8)

Voltage level of time constant switch	$V_{8\text{-}9}$	typ.	2,1	V
Voltage when the oscillator is in sync	$V_{8\text{-}9}$	typ.	1,2	V
Voltage when the oscillator is out-of-sync	$V_{8\text{-}9}$	typ.	2,6	V
Voltage during noise	$V_{8\text{-}9}$	typ.	1,7	V

* During standard video signals.

Flyback input pulse (pin 14)

Switching level	$V_{14\text{-}9}$	typ.	0,7 V
Input pulse	$V_{14\text{-}9}$	<	12 V
Input resistance		typ.	2,5 kΩ
Delay between the start of the sync pulse at the video input (pin 4) and the rising edge of the flyback pulse	t_p	typ.	1,5 μs

Vertical outputs

Output voltage (peak-to-peak value)	$V_{2\text{-}9(p\text{-}p)}$	>	10 V
Output current	I_2	<	5 mA
Output voltage low at $I_2 = 5$ mA	$V_{2\text{-}9}$	<	500 mV
Duration of output pulse during indirect synchronization	t_p	typ.	190 μs
Duration of output pulse during direct synchronization	t_p	typ.	160 μs
Ratio between basic horizontal oscillator frequency and vertical pulse			625 *

---

* When a non-standard sync signal is applied the separated vertical sync pulse of the incoming signal is connected to pin 2; the pulse of the divider circuit is switched off.

APPLICATION INFORMATION (see also Fig. 2)

The function is described against the corresponding pin number

1. Sandcastle output pulse

   This output pulse has three levels. The first and highest level (10 V) is the burst key pulse with a typical duration of 4,0 μs. The second level for the line blanking is typ. 4,5 V with a pulse duration equal to the line flyback pulse. The third level (typ. 2,5 V) is used for frame blanking and has a duration of typ. 1,34 ms (21 lines). This last pulse is only available with a standard video input signal. Under all other conditions, an external vertical flyback pulse must be applied to this pin. This pulse will be clamped to 2,5 V by means of an internal clamping circuit. The input current is typ. 2 mA.

2. Vertical output pulse

   This pulse is obtained from the divider circuit, the amplitude is in excess of 10 V peak-to-peak. This pulse has a duration of 190 μs when standard signals are received. The pulse is obtained from the vertical sync pulse integrator during non-standard signals and has a duration of about 160 μs. It has good stability and accuracy, so it is intended to be used for triggering the vertical oscillator.

3. Vertical sync pulse integrator bias network

   The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external capacitor with an internal resistor are required for the correct biasing of this circuit for various input conditions. A typical value for the capacitor is 10 μF.

4. Video input

   The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation.

   The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,1 to 1 V peak-to-peak. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 100 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

   The noise gate is activated at an input level < 1 V (typ. 0,7 V), thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V.

5. Sync separator slicing level output

   The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 6. The capacitor connected to pin 5 must be about 1 μF.

6. Black level detector output

   The black level of the input signal is detected on this pin. A capacitor of 22 μF in series with a resistor of 33 Ω has to be connected to this pin. A 4,7 kΩ resistor must be connected between pins 5 and 6.

7. Horizontal phase detector output and control oscillator input

   The flywheel filter must be connected to this pin. Typical values for the components are a capacitor of 100 nF in parallel with an RC-network of 1 kΩ and 10 μF. Furthermore, a resistor of 270 kΩ should be connected between pins 7 and 12.
   The output current of the phase detector depends on the condition of the coincidence detector. The output current is high when the oscillator is out of sync. The result is a large catching range, and the phase detector is not gated in that condition. The output current is low when the oscillator is synchronized and the phase detector is gated. A good noise immunity is obtained in this case.

8 Coincidence detector output

A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.
The following output voltages can occur:

– when in-sync	1,2 V
– when out-of-sync	2,6 V
– during noise at the input	1,7 V

When the output voltage < 2,1 V, the phase detector output current is low and the phase detector is gated. A good noise immunity is obtained in this case. For a voltage > 2,1 V, the output current of the phase detector is high and the phase detector is not gated. This results in a large catching range and a high dynamical steepness of the PLL. This latter condition is required during VCR-playback. It can be obtained by connecting pin 8 to the positive supply line via a resistor of 10 kΩ. The information of the line coincidence detector is fed to the divider circuit so that there is no delay in vertical synchronization after a channel change, or an unsynchronized camera change in the studio. Thus, the divider circuit is reset to direct sync, when line synchronization is lost.

9. Negative supply (ground)

10. Horizontal output

This is an open collector output. The collector resistor must be chosen such that sufficient current is supplied to the driver stage. The maximum current is 60 mA. The output stage is designed such that the line output transistor cannot be switched-on during flyback. Switching-on occurs directly after the flyback pulse to avoid linearity errors. The duty factor of the output pulse depends on the delay in the output stage (correction via the second control loop).

11. Control voltage second loop

This voltage controls the start of the output pulse at pin 10 (positive-going edge). The capacitor connected to this pin must have a value of about 22 nF.

12. Reference voltage control loops

The reference voltage must be decoupled by means of a capacitor of about 10 μF.
It is possible to obtain a phase shift between video and flyback pulse by changing this reference voltage externally. The possible phase shift is ± 1 μs.
The required voltage change is ± 0,6 V.

13. Decoupling internal power supply

The IC has two power supply terminals. The main terminal (pin 16) supplies the output stages, the sync separator and the divider circuit. The specially decoupled supply terminal (pin 13) supplies the horizontal oscillator. This is to avoid coupling of the video signal into the oscillator part. The capacitor connected to pin 13 should have a value of about 22 μF. The resistor connected between pins 13 and 16 should have a value of about 1 kΩ.

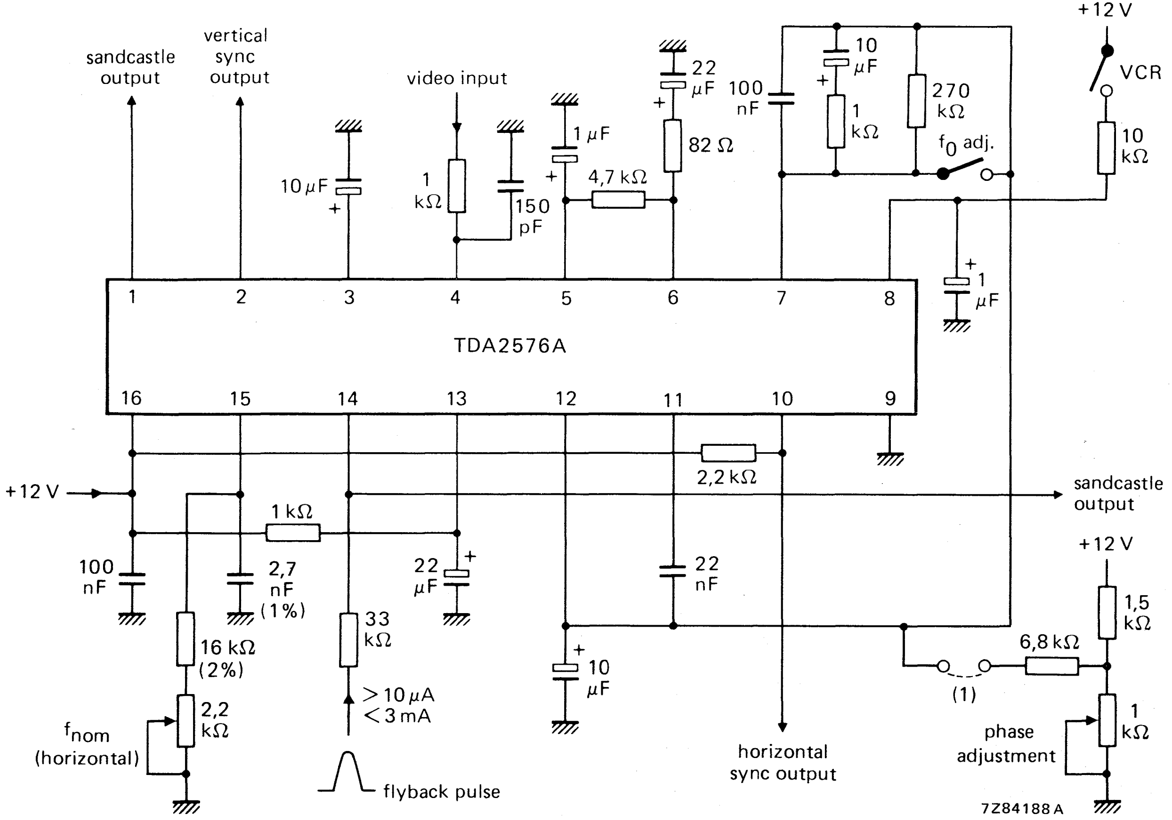
14. Flyback input pulse

The flyback input pulse is required for the second phase control loop and for generating the line blanking pulse in the sandcastle output. The input current should be at least 10 μA and not exceed 3 mA.

15. RC-network horizontal oscillator

Stable components should be chosen for a good frequency stability. A part of the total resistance must be variable for adjusting the frequency. This part should be as small as possible, because of poor stability of variable carbon resistors.
The oscillator can be adjusted when pins 7 and 12 are short-circuited (see Fig. 2).

16. Positive supply: The supply voltage may vary between 10 V and 13,2 V. The current-draw is 53 mA (typical) and a range of 35 to 70 mA at 12 V.



(1) Optional circuit for phase adjustment.

Fig. 2 Application circuit diagram.

SYNCHRONIZATION CIRCUIT WITH VERTICAL OSCILLATOR AND DRIVER STAGES

GENERAL DESCRIPTION

The TDA2577A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector ($\varphi 2$) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6,5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 3% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical comparator with internal 3% pre-correction circuit for vertical oscillator/sawtooth generator
- Vertical driver stage
- Vertical blanking pulse generator with external adjustment of pulse duration (50 Hz: 21 lines; 60Hz: 17 lines)
- Vertical guard circuit

QUICK REFERENCE DATA

Supply				
Minimum current required to start horizontal oscillator and output stage (pin 16)	I_{16}	>	4	mA
Main supply voltage (pin 10)	$V_P = V_{10\text{-}9}$	typ.	12	V
Supply current	$I_P = I_{10}$	typ.	55	mA
Input signals				
Sync pulse input voltage (peak-to-peak value; negative-going)	$V_{5\text{-}9(p\text{-}p)}$		0,15 to 1	V
Output signals				
Horizontal output pulse (open collector) at I_{11} = 40 mA	$V_{11\text{-}9}$	<	0,5	V
Vertical output pulse (emitter-follower) at I_1 = 10 mA	$V_{1\text{-}9}$	>	4	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

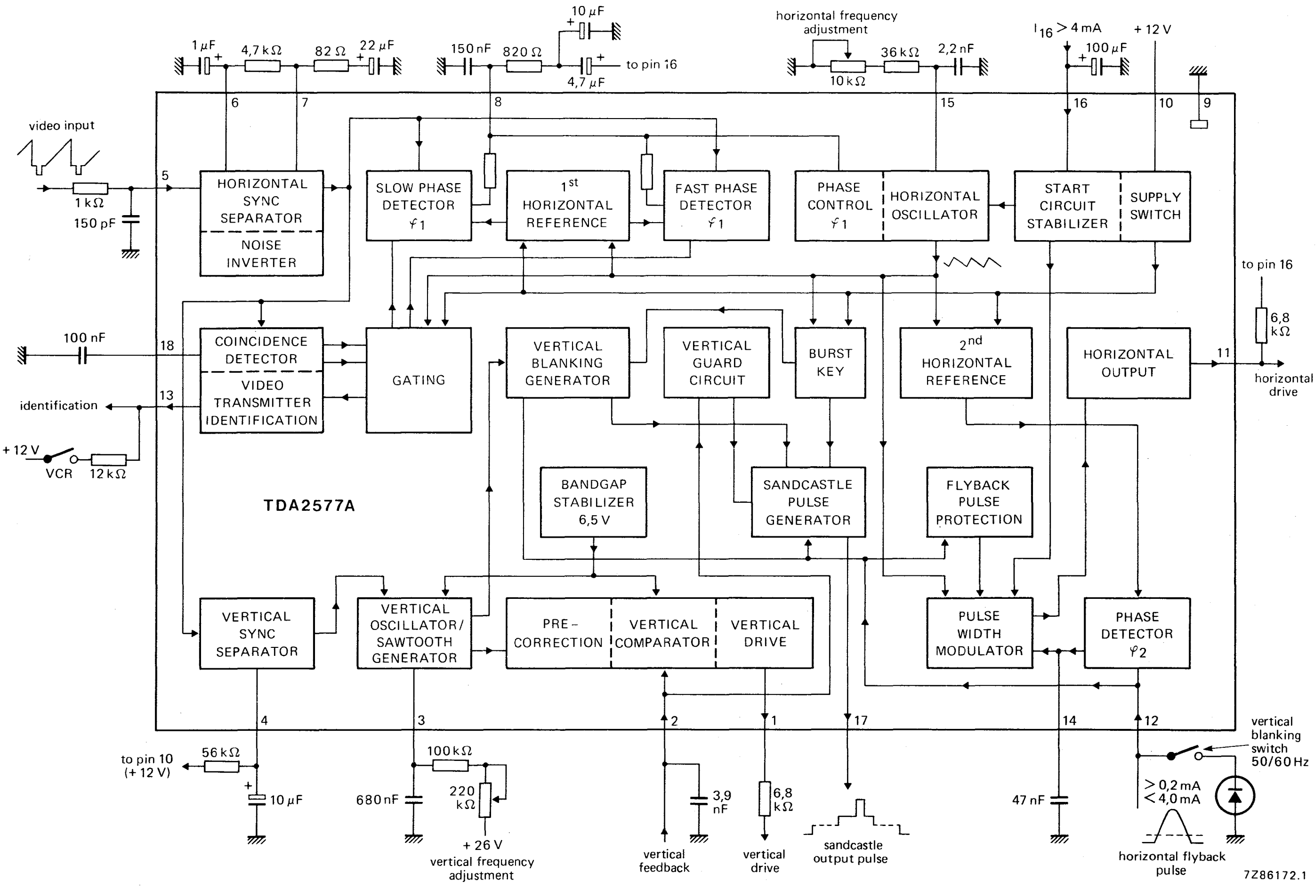


Fig. 1 Block diagram.

DEVELOPMENT SAMPLE DATA

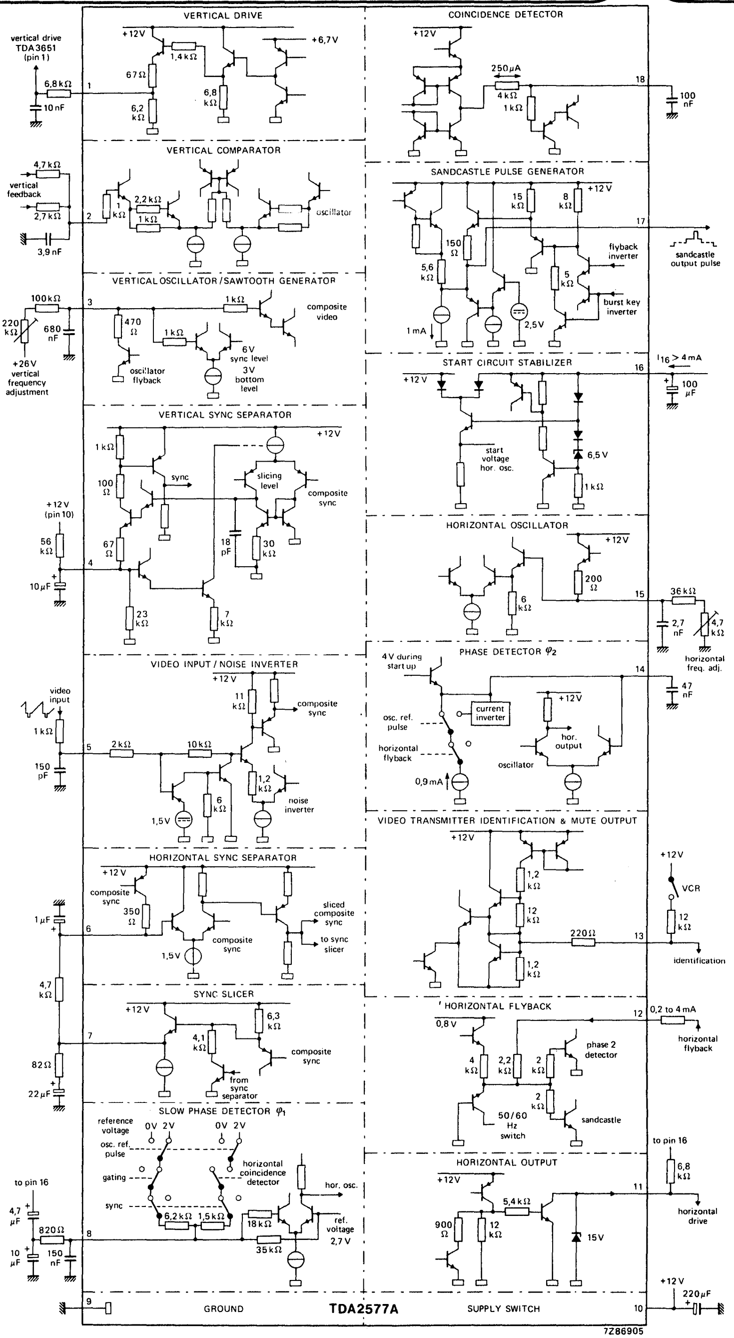


Fig. 2 TDA2577A circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Start current (pin 16)	I_{16}	max.	8	mA
Supply voltage (pin 10)	$V_P = V_{10\text{-}9}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	typ.	50	K/W

CHARACTERISTICS

$I_{16} = 5$ mA; $V_P = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

Supply

Supply current at pin 16	I_{16}		4 to 8	mA
Stabilized supply voltage (pin 16)	$V_{16\text{-}9}$	typ.	8,7	V
			8,0 to 9,5	V
Supply current (pin 10)	I_{10}	typ.	55	mA
		<	70	mA
Supply voltage (pin 10)	$V_P = V_{10\text{-}9}$	typ.	12	V
			10 to 13,2	V

Video input (pin 5)

Top-sync level	$V_{5\text{-}9}$	typ.	3,1	V
			1,5 to 3,75	V
Sync pulse amplitude (peak-to-peak value) (note 1)	$V_{5\text{-}9(p\text{-}p)}$	typ.	0,6	V
			0,15 to 1	V
Slicing level		typ.	50	%
			35 to 65	%
Delay between video input and detector output	t_1	typ.	0,35	µs

Noise gate (pin 5)

Switching level	$V_{5\text{-}9}$	typ.	0,7	V
		<	1	V

First control loop (sync to oscillator; pin 8)

Holding range	Δf	typ.	± 800	Hz
Catching range	Δf	typ.	± 800	Hz
			± 600 to 1100	Hz
Control sensitivity video with respect to oscillator, burst key and flyback pulse				
for slow time constant		typ.	1	kHz/µs
for fast time constant		typ.	2,75	kHz/µs

DEVELOPMENT SAMPLE DATA

Second control loop (horizontal output to flyback; pin 14)				
Control sensitivity; static (see note 2)	$\Delta t_d/\Delta t_o$	typ.	400	µs/µs
Control range	t_d		1 to 50	µs
Controlled edge	negative			
Phase adjustment (via 2nd control loop; pin 14)				
Control sensitivity		typ.	25	µA/µs
Maximum permissible control current	$\pm I_{14}$	<	50	µA
Horizontal oscillator (pin 15)				
Frequency (no sync)	f_{osc}	typ.	15 625	Hz
Frequency spread (C_{osc} = 2,2 nF; R_{osc} = 40 kΩ)	Δf_{osc}	<	4	%
Frequency deviation between starting point of output signal and stabilized condition	Δf_{osc}	typ.	6	%
		<	8	%
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$	K^{-1}
Horizontal output (pin 11)				
Output voltage; high level	$V_{11\text{-}9}$	<	13,2	V
Voltage at which protection starts	$V_{11\text{-}9}$		13 to 15,8	V
Output voltage; low level				
start condition at I_{11} = 10 mA	$V_{11\text{-}9}$	typ.	0,3	V
		<	0,5	V
normal condition at I_{11} = 40 mA	$V_{11\text{-}9}$	typ.	0,3	V
		<	0,5	V
Duty factor of output signal during starting (no phase shift; voltage at pin 11 low)	δ	typ.	65	%
Duty factor of output signal without flyback pulse	δ	typ.	50	%
			45 to 55	%
Controlled edge	negative			
Duration of output pulse (see Fig. 3)			$t_d + t_o + 2{,}5$	µs
Sandcastle output pulse (pin 17)				
Output voltage during:				
burst key	$V_{17\text{-}9}$	>	10	V
horizontal blanking	$V_{17\text{-}9}$	typ.	4,6	V
			4,2 to 5	V
vertical blanking	$V_{17\text{-}9}$	typ.	2,5	V
			2 to 3	V
Pulse duration				
burst key	t_p	typ.	4	µs
			3,6 to 4,4	µs
horizontal blanking	flyback pulse (see note 3)			
vertical blanking				
for 50 Hz application ($-I_{12}$: 0 to 0,1 mA)			21	lines
for 60 Hz application ($-I_{12}$: typ. 0,2 mA)			17	lines

CHARACTERISTICS (continued)

Delay between the start of the sync at the video input and the rising edge of the burst key pulse	t_2	typ. 4,9 µs 4,5 to 5,3 µs

Coincidence detector; video transmitter identification circuit; time constant switches (pin 18); see also Fig. 2

Detector output current	$\pm I_{18}$	typ. 300 µA
Voltage during noise (note 4)	$V_{18\text{-}9}$	typ. 0,3 V
Voltage level for in-sync condition	$V_{18\text{-}9}$	typ. 7,5 V
Switching level slow to fast	$V_{18\text{-}9}$	typ. 3,5 V 3,2 to 3,8 V
Switching level mute function active; φ_1 fast to slow	$V_{18\text{-}9}$	typ. 1,2 V 1,0 to 1,4 V
vertical period counter 3 periods fast	$V_{18\text{-}9}$	typ. 0,12 V 0,08 to 0,16 V
Switching level slow to fast (locking) mute function inactive	$V_{18\text{-}9}$	typ. 1,7 V 1,5 to 1,9 V
Switching level fast to slow (locking)	$V_{18\text{-}9}$	typ. 5,0 V 4,7 to 5,3 V
Switching level for VCR (fast time constant) without mute function	$V_{18\text{-}9}$	typ. 8,6 V 8,2 to 9,0 V

Video transmitter identification output (pin 13)

Output voltage active (no sync) at $I_{13} = 1$ mA	$V_{13\text{-}9}$	> 10 V typ. 11 V
Output voltage active (no sync) at $I_{13} = 5$ mA	$V_{13\text{-}9}$	> 7 V typ. 10 V
Output voltage inactive	$V_{13\text{-}9}$	< 0,5 V typ. 0,1 V

VCR switching (pin 13)

Input current for fast time constant phase detector φ_1, with mute function active	I_{13}	typ. 0,6 mA 0,4 to 0,8 mA

Flyback input pulse (pin 12)

Switching level	$V_{12\text{-}9}$	typ. 1 V
Input current	I_{12}	0,2 to 4 mA
Input pulse amplitude (peak-to-peak value)	$V_{12\text{-}9(p\text{-}p)}$	< 12 V
Input resistance	$R_{12\text{-}9}$	typ. 2,7 kΩ
Delay time of sync pulse (measured in φ_1) to flyback at switching level; $t_{fl} = 12$ µs (see also note 2 and Fig. 4)	t_o	typ. 1,3 µs

DEVELOPMENT SAMPLE DATA

Duration of vertical blanking pulse (pin 12)

Required input current (negative)				
for 50 Hz application; 21 lines blanking	$-I_{12}$	typ.	0,2	mA
			$>0,15$ to $<0,3$	mA
for 60 Hz application; 17 lines blanking	$-I_{12}$	<	0,1	mA
Maximum allowed input current	$-I_{12}$	<	0,4	mA

Vertical sawtooth generator (pin 3)

Vertical frequency (no sync)	f_s	typ.	46	Hz
Frequency spread (C_{osc} = 680 nF; R_{osc} = 180 kΩ; at + 26 V)	Δf_s	<	4	%
Synchronization range		typ.	22	%
Input current at V_{3-9} = 6 V	I_3	<	2	μA
Frequency shift for V_P = 10 to 13 V	Δf_s	<	0,2	%
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$	K^{-1}

Comparator (pin 2)

Input voltage; d.c. level	V_{2-9}	typ.	4,4	V
			4,0 to 4,8	V
a.c. level (peak-to-peak value)	$V_{2-9(p-p)}$	typ.	1,6	V
Input current at V_{2-9} = 6 V	I_2	<	2	μA
Sawtooth internal pre-correction (parabolic convex)		typ.	3	%

Vertical output stage; emitter follower (pin 1)

Output voltage at I_1 = 10 mA	V_{1-9}	typ.	3,6	V
			3,2 to 5	V
Output current	I_1	<	20	mA

Vertical guard circuit

Activating voltage levels (vertical blanking level is 2,5 V)				
switching level low	V_{2-9}	typ.	3	V
			2,7 to 3,3	V
switching level high	V_{2-9}	typ.	5,7	V
			5,3 to 6,1	V

Notes to characteristics

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. t_d = delay between negative transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V (t_{fl}).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5-9} \approx 5$ V.

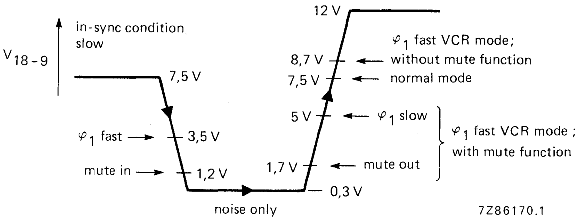


Fig. 3 Voltage levels at pin 18 (V_{18-9}).

APPLICATION INFORMATION

The TDA2577A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector (φ_2) is activated to control the timing of the negative-going edge of the horizontal output signal.

A bandgap reference voltage (6,5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4,7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3,1 V. The amplitude selective noise inverter is activated at a level of 0,7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking interval of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

APPLICATION INFORMATION (continued)

Table 1 Switching levels at pin 18.

voltage at pin 18	first phase detector φ_1				mute output at pin 13		receiving conditions
	time constant		gating				
	slow	fast	on	off	on	off	
7,5 V	X		X			X	video signal detected
7,5 to 3,5 V	X		X			X	video signal detected
3,5 to 1,2 V		X		X		X	video signal detected
1,2 to 0,1 V	X		X		X		noise only
0,1 to 1,7 V	X	*	X	*	X		new video signal detected
1,7 to 5,0 V		X		X		X	horizontal oscillator locked VCR playback with mute function
5,0 to 7,5 V	X		X			X	horizontal oscillator locked
8,7 V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5,5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0,1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1,2 V is reached within 5 ms (C_{18} = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground. Also a current of 0,6 mA into pin 13 sets the first phase detector to fast without affecting the mute output function (active HIGH with no video signal detected). For VCR playback without mute function, the first phase detector can be set to fast by connecting a resistor of 1 kΩ to the supply (pin 10).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 3,5 mA, which will result in a supply voltage of about 5,5 V (for guaranteed operation of all devices $I_{16} > 4$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5,5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8,8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8,7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally precorrected by 3% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6,5 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4,6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2,5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration is set by the negative voltage value of the horizontal flyback pulse at pin 12.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3 V or higher than 5,8 V, the guard circuit will insert a continuous level of 2,5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

APPLICATION INFORMATION (continued)

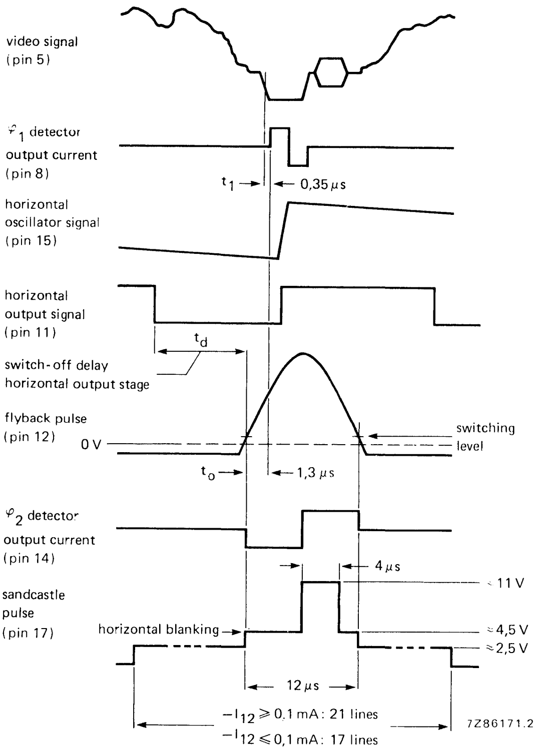


Fig. 4 Timing diagram of the TDA2577A.

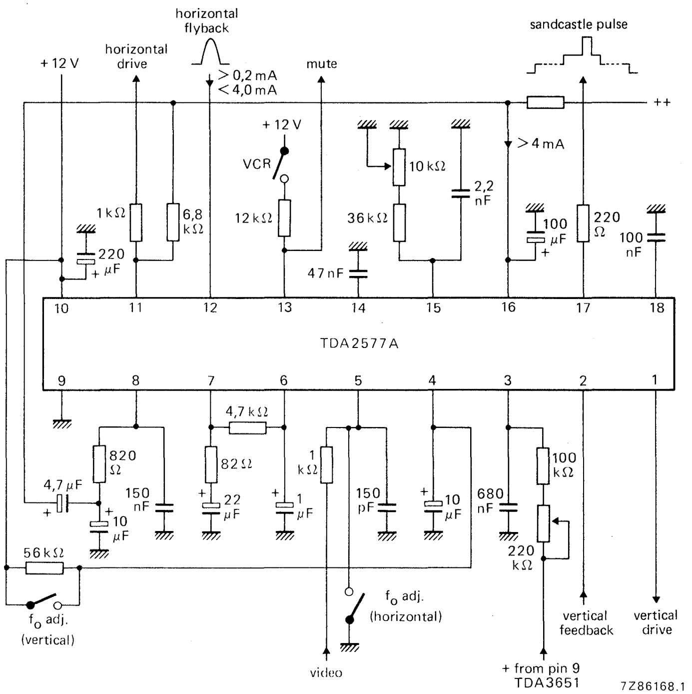


Fig. 5 Typical application circuit diagram; for combination of the TDA2577A with the TDA3651 see Fig. 7.

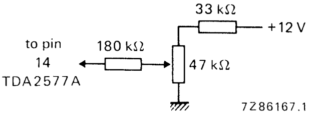


Fig. 6 Circuit configuration at pin 14 for phase adjustment.

APPLICATION INFORMATION (continued)

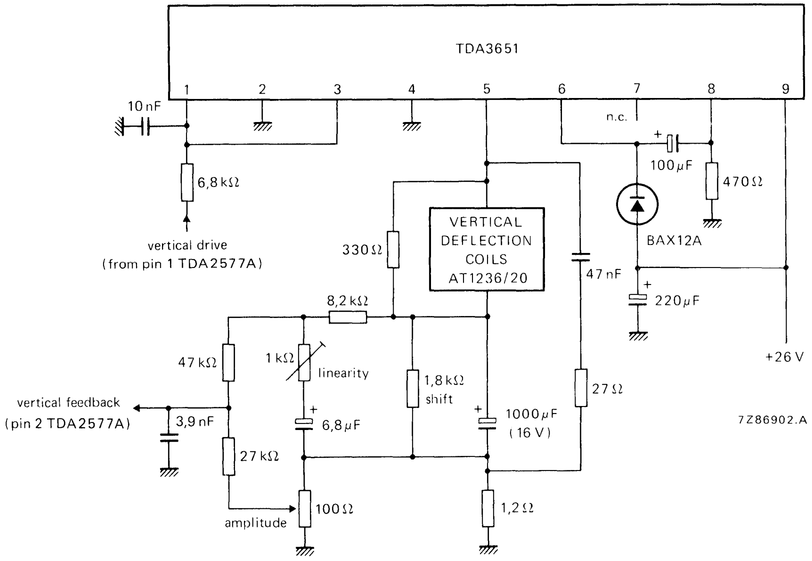


Fig. 7 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2577A (90° application).

DEVELOPMENT SAMPLE DATA

DEVELOPMENT SAMPLE DATA

SYNCHRONIZATION CIRCUIT WITH VERTICAL OSCILLATOR AND DRIVER STAGES

GENERAL DESCRIPTION

The TDA2578A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector (φ_2) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6,5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 6% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical driver stage
- Vertical blanking pulse generator
- 50/60 Hz detector
- 50/60 Hz identification output
- Automatic amplitude adjustment for 60 Hz
- Automatic adjustment of blanking pulse duration (50 Hz: 21 lines; 60 Hz: 17 lines)
- Vertical guard curcuit

QUICK REFERENCE DATA

Supply				
Minimum current required to start horizontal oscillator and output stage (pin 16)	I_{16}	>	4	mA
Main supply voltage (pin 10)	$V_P = V_{10\text{-}9}$	typ.	12	V
Supply current	$I_P = I_{10}$	typ.	55	mA
Input signals				
Sync pulse input voltage (peak-to-peak value; negative-going)	$V_{5\text{-}9(p\text{-}p)}$		0,15 to 1	V
Output signals				
Horizontal output pulse (open collector) at I_{11} = 40 mA	$V_{11\text{-}9}$	<	0,5	V
Vertical output pulse (emitter-follower) at I_1 = 10 mA	$V_{1\text{-}9}$	>	4	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

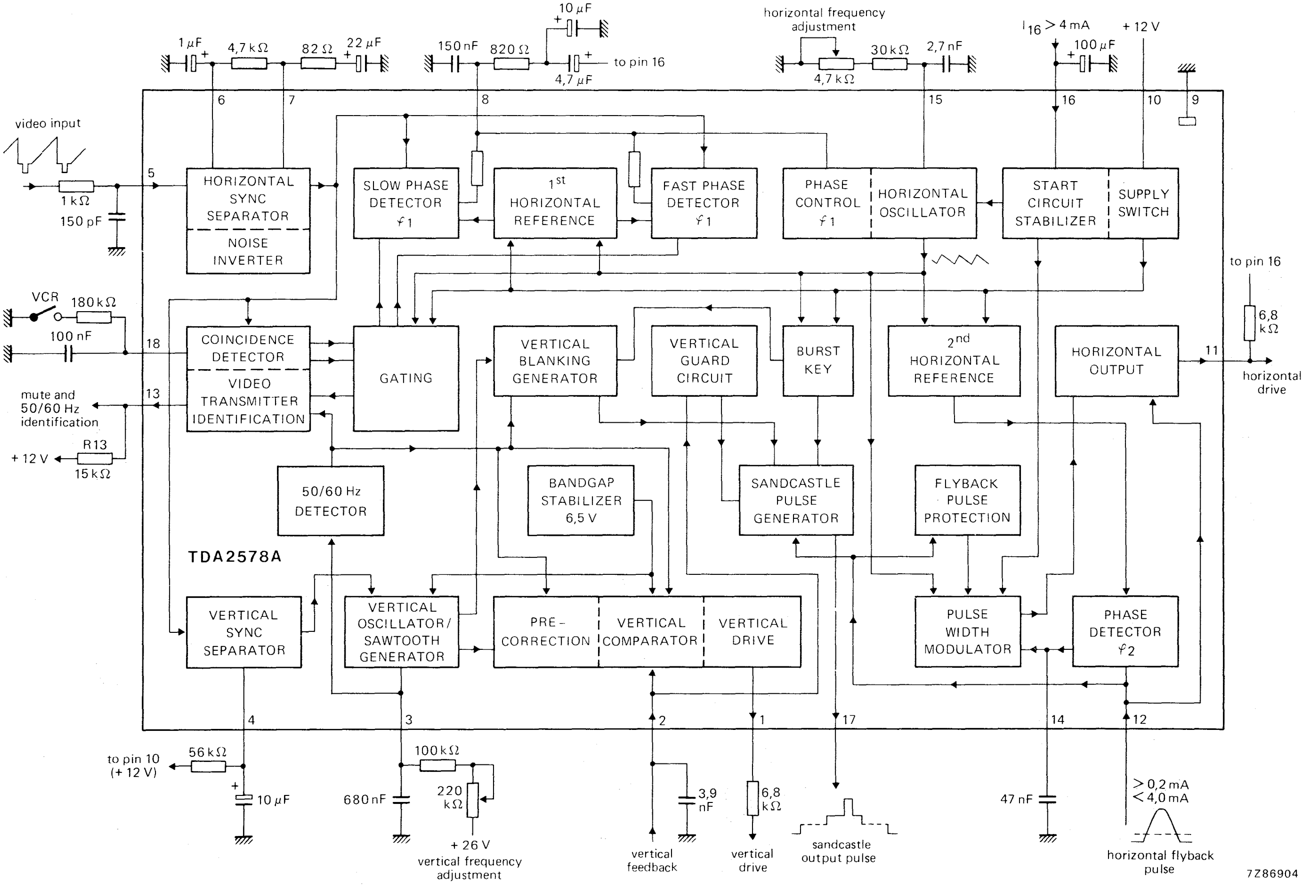


Fig. 1 Block diagram.

DEVELOPMENT SAMPLE DATA

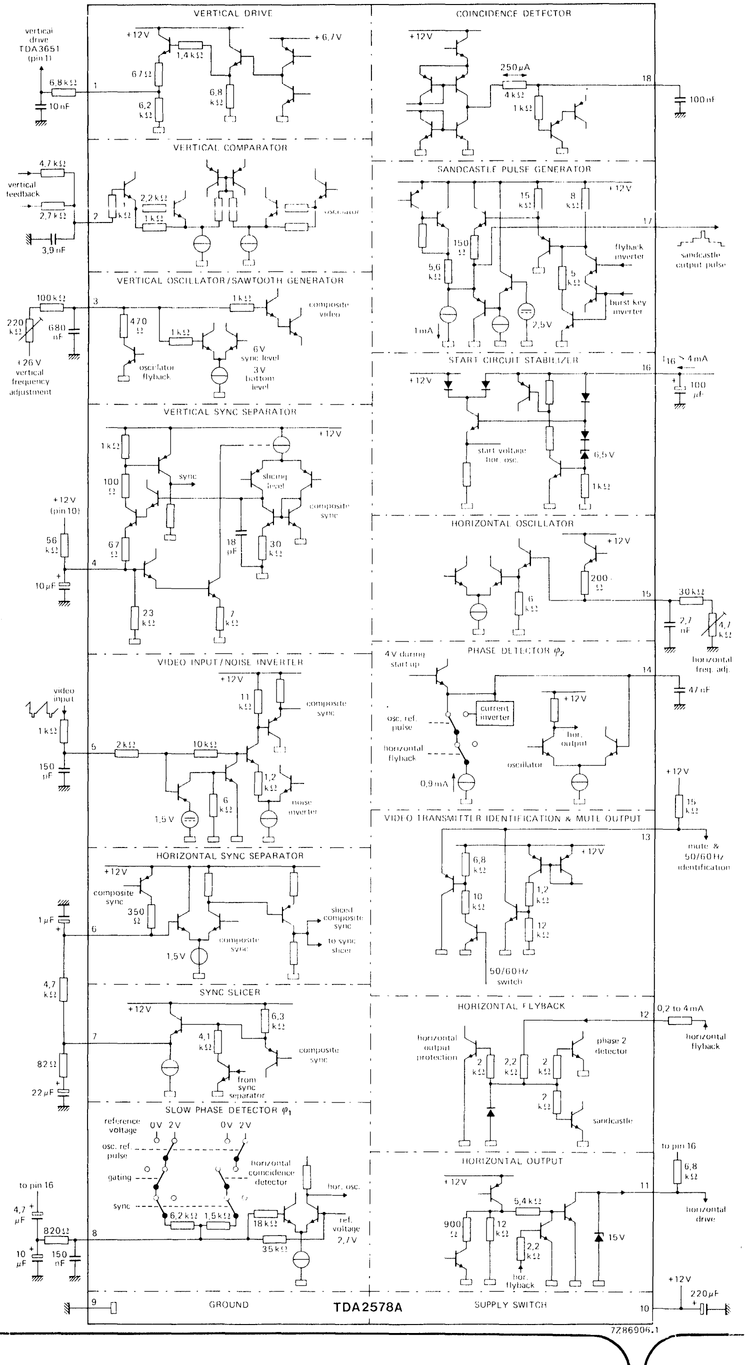


Fig. 2 TDA2578A circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Start current (pin 16)	I_{16}	max.	8	mA
Supply voltage (pin 10)	$V_P = V_{10\text{-}9}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	typ.	50	K/W

CHARACTERISTICS

$I_{16} = 5$ mA; $V_P = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

Supply				
Supply current at pin 16	I_{16}		4 to 8	mA
Stabilized supply voltage (pin 16)	$V_{16\text{-}9}$	typ.	8,7	V
			8,0 to 9,5	V
Supply current (pin 10)	I_{10}	typ.	55	mA
		<	70	mA
Supply voltage (pin 10)	$V_P = V_{10\text{-}9}$	typ.	12	V
			10 to 13,2	V
Video input (pin 5)				
Top-sync level	$V_{5\text{-}9}$	typ.	3,1	V
			1,5 to 3,75	V
Sync pulse amplitude (peak-to-peak value) (note 1)	$V_{5\text{-}9(p\text{-}p)}$	typ.	0,6	V
			0,15 to 1	V
Slicing level		typ.	50	%
			35 to 65	%
Delay between video input and detector output	t_1	typ.	0,35	μs
Noise gate (pin 5)				
Switching level	$V_{5\text{-}9}$	typ.	0,7	V
		<	1	V
First control loop (sync to oscillator; pin 8)				
Holding range	Δf	typ.	± 800	Hz
Catching range	Δf	typ.	± 800	Hz
			± 600 to 1100	Hz
Control sensitivity video with respect to oscillator, burst key and flyback pulse				
for slow time constant		typ.	1	kHz/μs
for fast time constant		typ.	2,75	kHz/μs

Second control loop (horizontal output to flyback; pin 14)				
Control sensitivity; static (see note 2)	$\Delta t_d/\Delta t_o$	typ.	400	μs/μs
Control range	t_d		1 to 45	μs
Controlled edge	positive			
Phase adjustment (via 2nd control loop; pin 14)				
Control sensitivity		typ.	25	μA/μs
Maximum permissible control current	$\pm I_{14}$	$<$	50	μA
Horizontal oscillator (pin 15)				
Frequency (no sync)	f_{osc}	typ.	15 625	Hz
Frequency spread (C_{osc} = 2,7 nF; R_{osc} = 33 kΩ; no sync)	Δf_{osc}	$<$	4	%
Frequency deviation between starting point of output signal and stabilized condition	Δf_{osc}	typ. $<$	6 8	% %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$	K^{-1}
Horizontal output (pin 11)				
Output voltage; high level	$V_{11\text{-}9}$	$<$	13,2	V
Voltage at which protection starts	$V_{11\text{-}9}$		13 to 15,8	V
Output voltage; low level start condition at I_{11} = 10 mA	$V_{11\text{-}9}$	typ. $<$	0,3 0,5	V V
normal condition at I_{11} = 40 mA	$V_{11\text{-}9}$	typ. $<$	0,3 0,5	V V
Duty factor of output signal during starting (no phase shift) I_{16} = 4 mA (voltage at pin 11 low)	δ	typ.	65	%
Duty factor of output signal without flyback pulse	δ	typ.	50 45 to 55	% %
Controlled edge	positive			
Duration of output pulse (see Fig. 4)	t_d + horizontal flyback pulse			
Sandcastle output pulse (pin 17)				
Output voltage during: burst key	$V_{17\text{-}9}$	$>$	10	V
horizontal blanking	$V_{17\text{-}9}$	typ.	4,6 4,2 to 5	V V
vertical blanking	$V_{17\text{-}9}$	typ.	2,5 2 to 3	V V
Pulse duration burst key	t_p	typ.	4 3,6 to 4,4	μs μs
horizontal blanking	flyback pulse (see note 3)			
vertical blanking at 50 Hz	21 lines			
at 60 Hz	17 lines			

CHARACTERISTICS (continued)

Delay between the start of the sync at the video input and the rising edge of the burst key pulse	t_2	typ.	4,9 μs 4,5 to 5,3 μs

Coincidence detector; video transmitter identification circuit; time constant switches (pin 18); see also Fig. 3

Detector output current	$\pm I_{18}$	typ.	300 μA
Voltage during noise (note 4)	$V_{18\text{-}9}$	typ.	0,3 V
Voltage level for in-sync condition	$V_{18\text{-}9}$	typ.	7,5 V
Switching level slow to fast	$V_{18\text{-}9}$	typ.	3,5 V 3,2 to 3,8 V
Switching level mute function active; φ_1 fast to slow	$V_{18\text{-}9}$	typ.	1,2 V 1,0 to 1,4 V
vertical period counter 3 periods fast	$V_{18\text{-}9}$	typ.	0,12 V 0,08 to 0,16 V
Switching level slow to fast (locking) mute function inactive	$V_{18\text{-}9}$	typ.	1,7 V 1,5 to 1,9 V
Switching level fast to slow (locking)	$V_{18\text{-}9}$	typ.	5,0 V 4,7 to 5,3 V
Switching level for VCR (fast time constant) without mute function	$V_{18\text{-}9}$	typ.	8,6 V 8,2 to 9,0 V

Video transmitter identification output (pin 13)

Output voltage active (no sync) at $I_{13} = 1$ mA	$V_{13\text{-}9}$	< typ.	0,5 V 0,3 V
Sink current active (no sync)	I_{13}	⩽	5 mA
Output current inactive (sync: 50 Hz)	I_{13}	<	1 μA

50/60 Hz identification (pin 13)

R13 = 15 kΩ to + 12 V (note 5)

at f = 50 Hz (in sync condition)	$V_{13\text{-}9}$	typ.	$V_{10\text{-}9}$ V
at f = 60 Hz (in sync condition)	$V_{13\text{-}9}$	typ.	7,6 V 7,2 to 8 V

Flyback input pulse (pin 12)

Switching level	$V_{12\text{-}9}$	typ.	1 V
Input current	I_{12}		0,2 to 4 mA
Input pulse amplitude (peak-to-peak value)	$V_{12\text{-}9(p\text{-}p)}$	<	12 V
Input resistance	$R_{12\text{-}9}$	typ.	2,7 kΩ
Delay time of sync pulse (measured in φ_1) to flyback at switching level; $t_{fl} = 12$ μs (see also note 2 and Fig. 4)	t_o	typ.	1,3 μs

Vertical sawtooth generator (pin 3)

Vertical frequency (no sync)	f_s	typ.	46	Hz
Frequency spread (C_{osc} = 680 nF; R_{osc} = 180 kΩ; at + 26 V)	Δf_s	<	4	%
Synchronization range (note 6)		typ.	33	%
Input current at $V_{3\text{-}9}$ = 6 V	I_3	<	3	μA
Frequency shift for V_P = 10 to 13 V	Δf_s	<	0,2	%
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$	K^{-1}

Comparator (pin 2)

Input voltage; d.c. level	$V_{2\text{-}9}$	typ.	4,4	V
			4,0 to 4,8	V
a.c. level (peak-to-peak value)	$V_{2\text{-}9(p\text{-}p)}$	typ.	0,8	V
Input current at $V_{2\text{-}9}$ = 6 V	I_2	<	2	μA
Sawtooth internal pre-correction (parabolic convex)		typ.	6	%

Vertical output stage; emitter follower (pin 1)

Output voltage at I_1 = 10 mA	$V_{1\text{-}9}$	typ.		V
			3,2 to 5	V
Output current	I_1	<	20	mA

Vertical guard circuit

Activating voltage levels (vertical blanking level is 2,5 V) switching level low	$V_{2\text{-}9}$	typ.	3,35	V
			3,0 to 3,7	V
switching level high	$V_{2\text{-}9}$	typ.	5,15	V
			4,75 to 5,55	V

Notes to characteristics

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. t_d = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V (t_{fl}).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5\text{-}9} \approx 5$ V.
5. For 60 Hz a p-n-p emitter clamp is activated.
6. When f_o = 46 Hz the 50/60 Hz detector switches over to 60 Hz; video input signal at pin 5 ≈ 55 Hz.

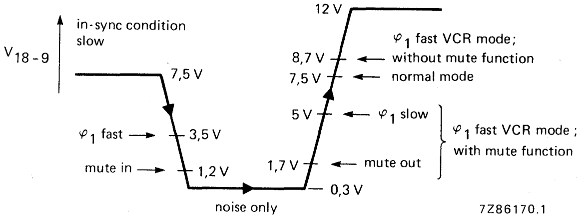


Fig. 3 Voltage levels at pin 18 ($V_{18\text{-}9}$).

APPLICATION INFORMATION

The TDA2578A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector (φ_2) is activated to control the timing of the positive-going edge of the horizontal output signal.

A bandgap reference voltage (6,5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4,7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3,1 V. The amplitude selective noise inverter is activated at a level of 0,7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking internal of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

Table 1 Switching levels at pin 18.

voltage at pin 18	first phase detector φ_1				mute output at pin 13		receiving conditions
	time constant		gating				
	slow	fast	on	off	on	off	
7,5 V	X		X			X	video signal detected
7,5 to 3,5 V	X		X			X	video signal detected
3,5 to 1,2 V		X		X		X	video signal detected
1,2 to 0,1 V	X		X		X		noise only
0,1 to 1,7 V	X	*	X	*	X		new video signal detected
1,7 to 5,0 V		X		X		X	horizontal oscillator locked VCR playback with mute function
5,0 to 7,5 V	X		X			X	horizontal oscillator locked
8,7 V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

APPLICATION INFORMATION (continued)

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5,5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0,1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1,2 V is reached within 5 ms (C_{18} = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground (see Fig. 7).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 3,6 mA, which will result in a supply voltage of about 5,5 V (for guaranteed operation of all devices $I_{16} > 4$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5,5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8,8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8,7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally pre-corrected by 6% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6,7 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4,6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2,5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration and sawtooth amplitude is automatically adjusted via the 50/60 Hz detector.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3,35 V or higher than 5,15 V, the guard circuit will insert a continuous level of 2,5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

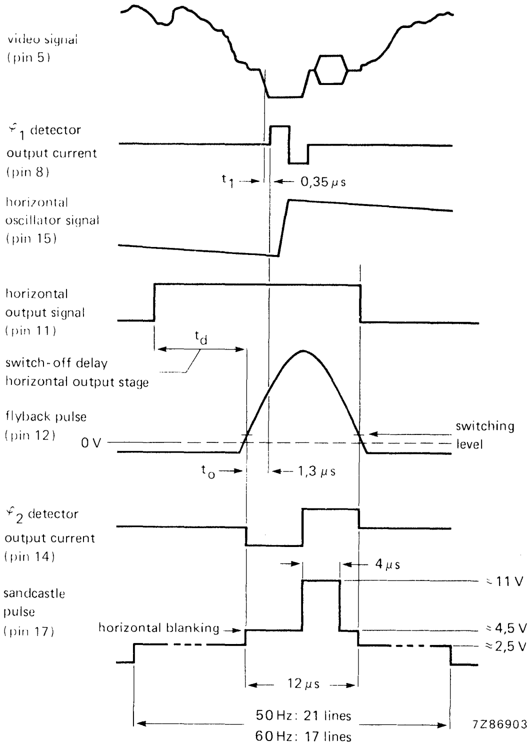
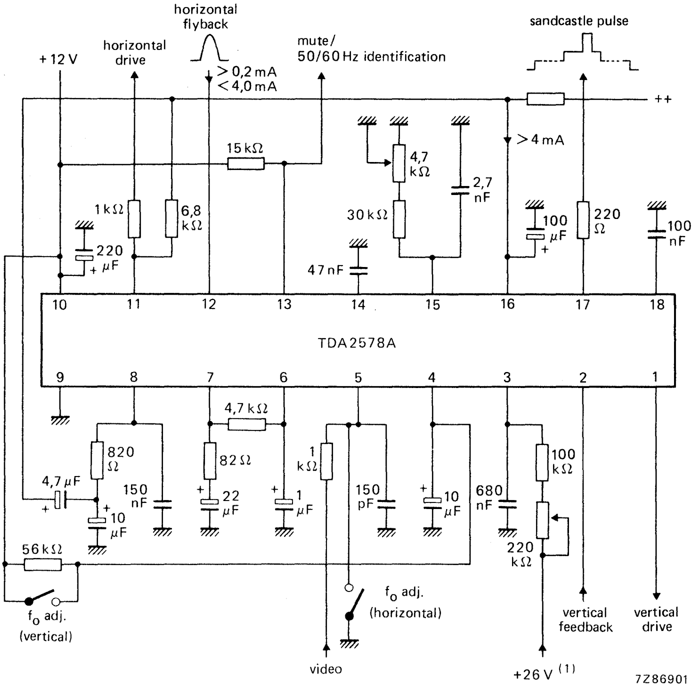


Fig. 4 Timing diagram of the TDA2578A.

APPLICATION INFORMATION (continued)



(1) ⩾ 26 V for linear scan.

Fig. 5 Typical application circuit diagram; for application of the TDA2578A with the TDA3651 see Fig. 8.

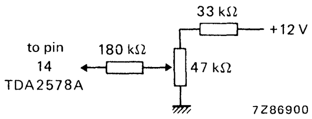


Fig. 6 Circuit configuration at pin 14 for phase adjustment.

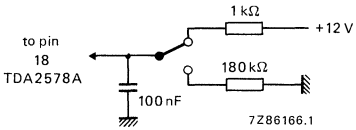


Fig. 7 Circuit configuration at pin 18 for VCR mode.
1 kΩ resistor between pin 18 and + 12 V: without mute function.
180 kΩ between pin 18 and ground: with mute function.

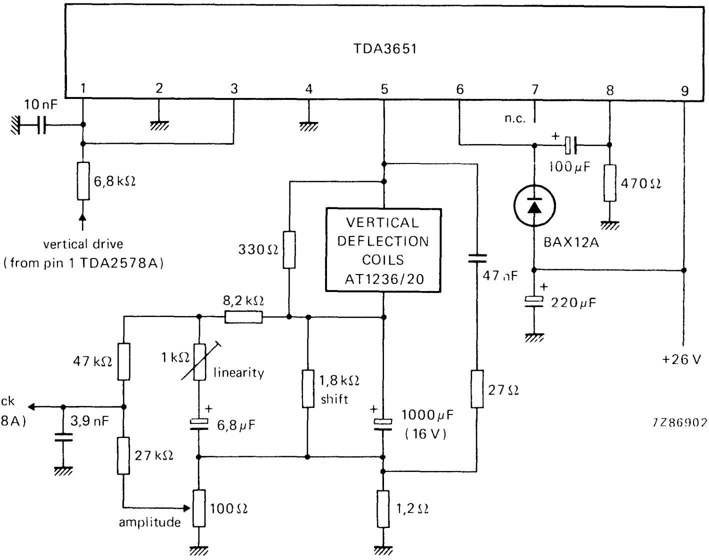


Fig. 8 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2578A, (90° application).

DEVELOPMENT SAMPLE DATA

SYNCHRONIZATION CIRCUIT WITH SYNCHRONIZED VERTICAL DIVIDER SYSTEM AND OUTPUT STAGES

GENERAL DESCRIPTION

The TDA2579 separates the vertical and horizontal sync pulses from the composite television video signal and uses them to synchronize the horizontal oscillator and the vertical divider system.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Triple current source in the phase detector with automatic selection dependent upon input signal conditions (automatic fast for VCR)
- Time constant externally switchable
- Inhibit of horizontal phase detector and video transmitter identification circuit during equalizing pulses and vertical sync pulses
- Second phase detector ($\varphi 2$) for storage compensation of the horizontal output stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Horizontal output pulse with constant duty cycle value of 28 μs
- Duty factor of the horizontal output pulse is 50% when horizontal flyback pulse is absent and during starting
- Vertical sync separator without external components and two integration times with automatic selection
- Zener diode reference source for the vertical sawtooth generator and vertical comparator
- Divider system with three different reset enable windows
- Synchronization is set to 628 divider ratio when no vertical sync pulses and no video transmitter is identified
- Linear negative going sawtooth generated via the divider system (no frequency adjustment)
- Comparator with a low d.c. feedback signal
- Vertical driver stage
- 50/60 Hz detector circuit
- 50/60 Hz identification output combined with the mute function
- Automatic amplitude adjustment for 50 and 60 Hz
- Automatic adjustment of blanking pulse duration (50 Hz; 21 lines; 60 Hz: 17 lines)
- Vertical guard circuit

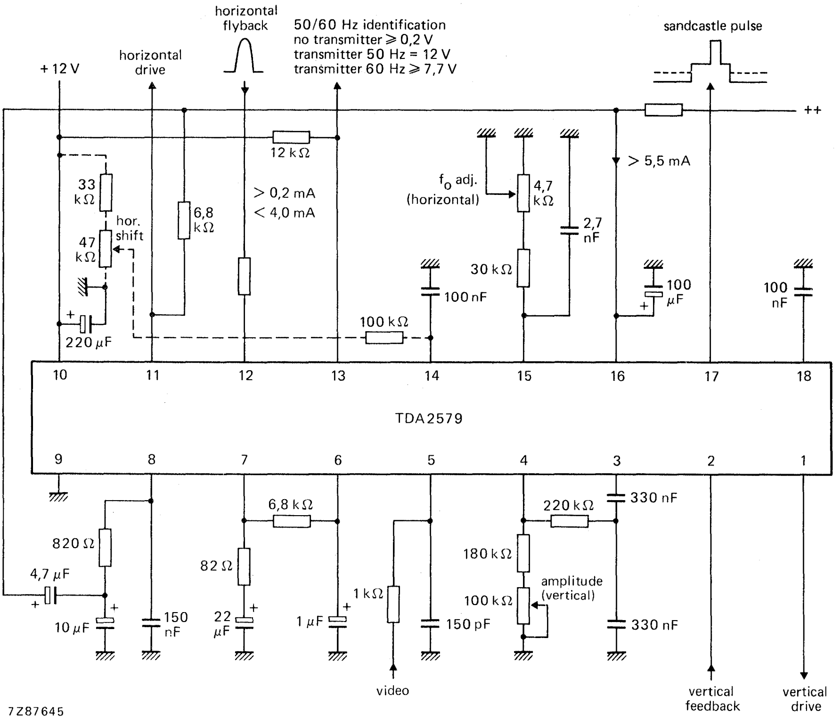


Fig. 1 Typical application circuit diagram; for combination of the TDA2579 with the TDA3653 see Fig. 2.

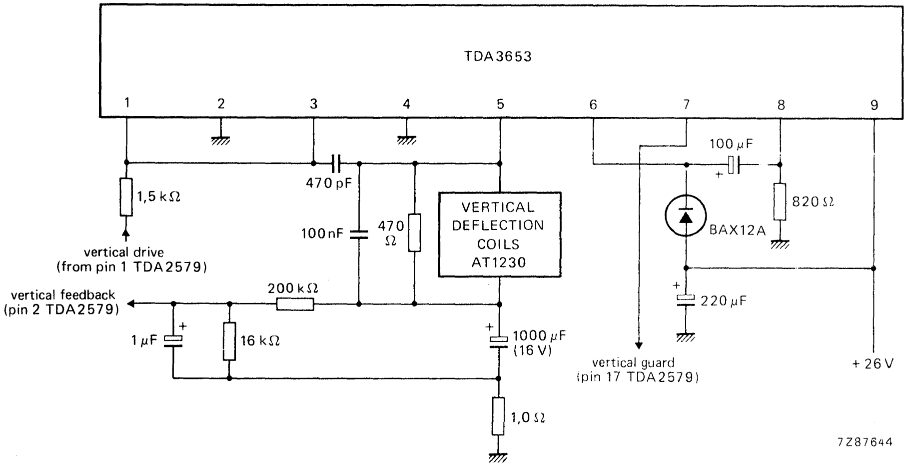


Fig. 2 Typical application of the TDA3653 (vertical output), when used in combination with the TDA2579.

DEVELOPMENT SAMPLE DATA

CONTROL CIRCUIT FOR SMPS

The TDA2581 is a monolithic integrated circuit for controlling switched-mode power supplies (SMPS) which are provided with the drive for the horizontal deflection stage.

The circuit features the following:

- Voltage controlled horizontal oscillator.
- Phase detector.
- Duty factor control for the positive-going transient of the output signal.
- Duty factor increases from zero to its normal operation value.
- Adjustable maximum duty factor.
- Over-voltage and over-current protection with automatic re-start after switch-off.
- Counting circuit for permanent switch-off when n-times over-current or over-voltage is sensed.
- Protection for open-reference voltage.
- Protection for too low supply voltage.
- Protection against loop faults.
- Positive tracking of duty factor and feedback voltage when the feedback voltage is smaller than the reference voltage minus 1,5 V.

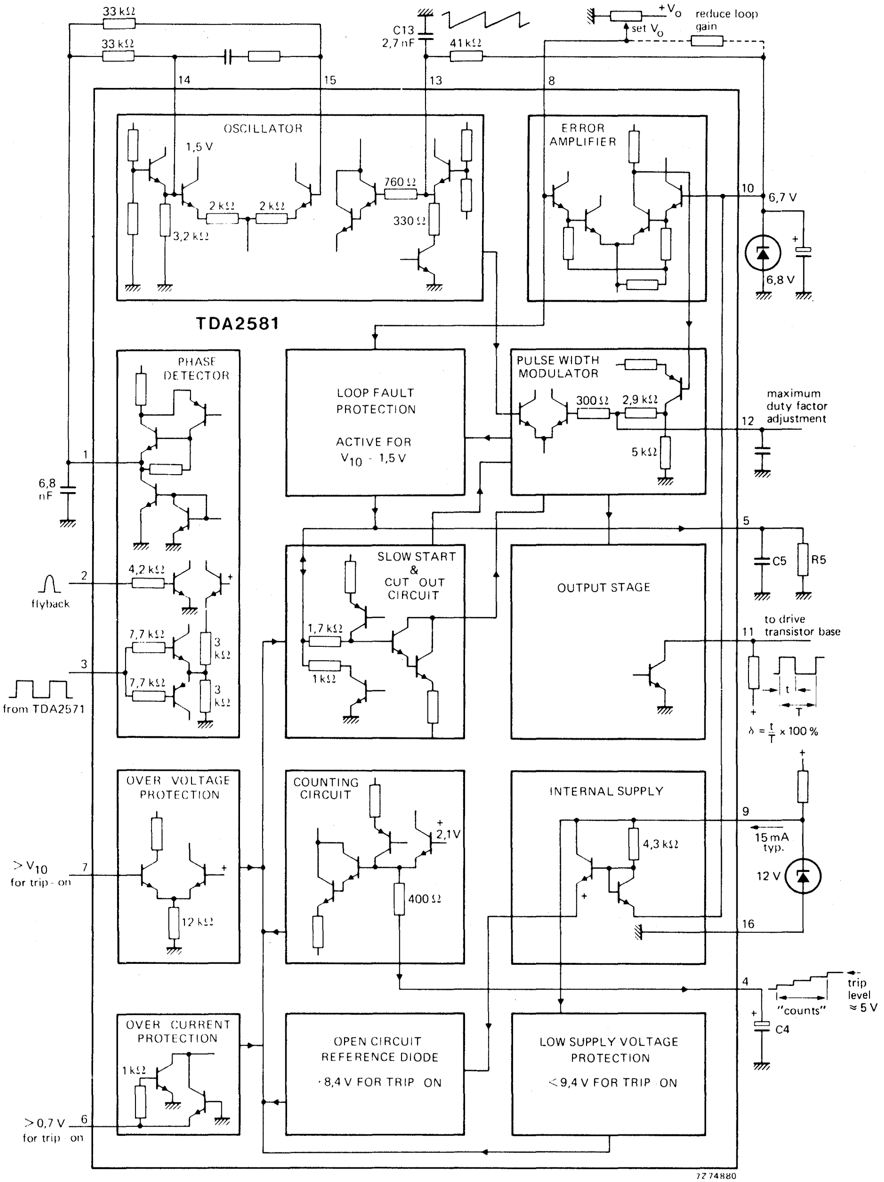
QUICK REFERENCE DATA

Supply voltage	$V_{9\text{-}16}$	typ.	12	V
Supply current	I_9	typ.	15	mA
Input signals				
Horizontal drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	11	V
Flyback pulse (differentiated deflection current); peak-to-peak value	$V_{2\text{-}16(p\text{-}p)}$	typ.	5	V
External reference voltage	$V_{10\text{-}16}$	typ.	6,7	V
Output signals				
Duty factor of output pulse	δ	> <	0 98 ± 0,6	% %
Output voltage at $I_O < 20$ mA (peak value)	$V_{11\text{-}16M}$	typ.	11,8	V
Output current (peak value)	I_{11M}	<	40	mA

PACKAGE OUTLINES

TDA2581: 16-lead DIL; plastic (SOT-38).
TDA2581Q: 16-lead QIL; plastic (SOT-58).

BLOCK DIAGRAM



Note: trip levels are nominal values.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{9\text{-}16}$	max.	14	V
Voltage at pin 11	$V_{11\text{-}16}$		0 to 14	V
Output current	I_{11}	max.	40	mA
Total power dissipation	P_{tot}	max.	340	mW
Storage temperature	T_{stg}		−25 to +125	°C
Operating ambient temperature	T_{amb}		−25 to +80	°C

CHARACTERISTICS

$V_{9\text{-}16}$ = 12 V; $V_{10\text{-}16}$ = 6,7 V; T_{amb} = 25 °C; measured in the circuit on page 314

Supply voltage range	$V_{9\text{-}16}$	typ.	12	V
			10 to 14	V
Protection voltage too low supply voltage	$V_{9\text{-}16}$	typ.	9,4	V
			8,6 to 9,9	V
Supply current at δ = 50%	I_9	typ.	15	mA
Supply current during protection	I_9	typ.	15	mA
Minimum required supply current	I_9	<	18,5	mA*
Power consumption	P	typ.	180	mW
Required input signals				
Reference voltage	$V_{10\text{-}16}$	typ.	6,7	V
			5,6 to 7,5	V**
High reference voltage protection: threshold voltage	$V_{10\text{-}16}$	typ.	8,4	V
			7,9 to 8,9	V
Feedback input impedance at pin 8	$\lvert Z_{8\text{-}16} \rvert$	typ.	200	kΩ
Horizontal drive pulse (square-wave or differentiated; negative transient is reference) peak-to-peak value	$V_{3\text{-}16(p\text{-}p)}$	typ.	11	V
			5 to 12	V
Flyback pulse or differential deflection current	$V_{2\text{-}16}$		1 to 5	V
Over-current protection: threshold voltage	$-V_{6\text{-}16}$	typ.	640	mV
			690 to 695	mV▲
	$+V_{6\text{-}16}$	typ.	680	mV
			640 to 735	mV▲
Over-voltage protection: threshold voltage	$V_{7\text{-}16}$	typ.	$V_{10\text{-}16}$ −60	mV
			$V_{10\text{-}16}$ −130 to $V_{10\text{-}16}$ −0	mV

---

* This value refers to the minimum required supply current that will start all devices under the following conditions: $V_{9\text{-}16}$ = 10 V; $V_{10\text{-}16}$ = 6,8 V; δ = 50%.

** Voltage obtained via an external reference diode. Specified voltages do not refer to the nominal voltages of reference diodes.

▲ This spread is inclusive temperature rise of the IC due to warming up. For other ambient temperatures the values must be corrected by using a temperature coefficient of typical −1,85 mV/°C.

CHARACTERISTICS (continued)

Remote control voltage; switch off	V_{4-16}	>	5,8	V*
switch on	V_{4-16}	<	4,5	V*

Delivered output signals

Horizontal drive pulse (loaded with a resistor of 560 Ω to +12 V) peak-to-peak value	$V_{11-16(p-p)}$	>	11,6	V
Output current; peak value	I_{11M}	<	40	mA
Saturation voltage of output transistor at I_{11} = 20 mA	V_{CEsat}	typ.	200	mV
		<	400	mV
at I_{11} = 40 mA	V_{CEsat}	<	525	mV
Duty factor of output pulse**	δ	>	0	%
		<	98 ± 0,6	%
Charge current for capacitor on pin 4	I_4	typ.	120	μA
Charge current for capacitor on pin 5	I_5	typ.	130	μA
Supply current for reference	I_{10}	typ.	1	mA
			0,6 to 1,45	mA

Oscillator

Temperature coefficient		typ.	−300	ppm/°C
		<	−400	ppm/°C
Relative frequency deviation for V_{10-16} changing from 6 to 7 V		typ.	−1,5	%
		⩽	−2	%
Oscillator frequency spread (with fixed external components)		⩽	±3	%
Frequency control sensitivity at pin 15		typ.	4,5	kHz/V▲

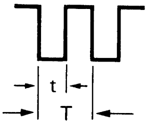
Phase control loop

Loop gain of APC-system (automatic phase control)		typ.	5	kHz/μs
Catching range	Δf	typ.	±1,5	kHz
Phase relation between negative transient of sync pulse and middle of flyback	t	typ.	1	μs
Tolerance of phase relation	Δt	⩽	±0,4	μs

---

* See pin 4 on pages 319 and 320.

** The duty factor is specified as follows:



$\delta = \frac{t}{T} \times 100\%$.

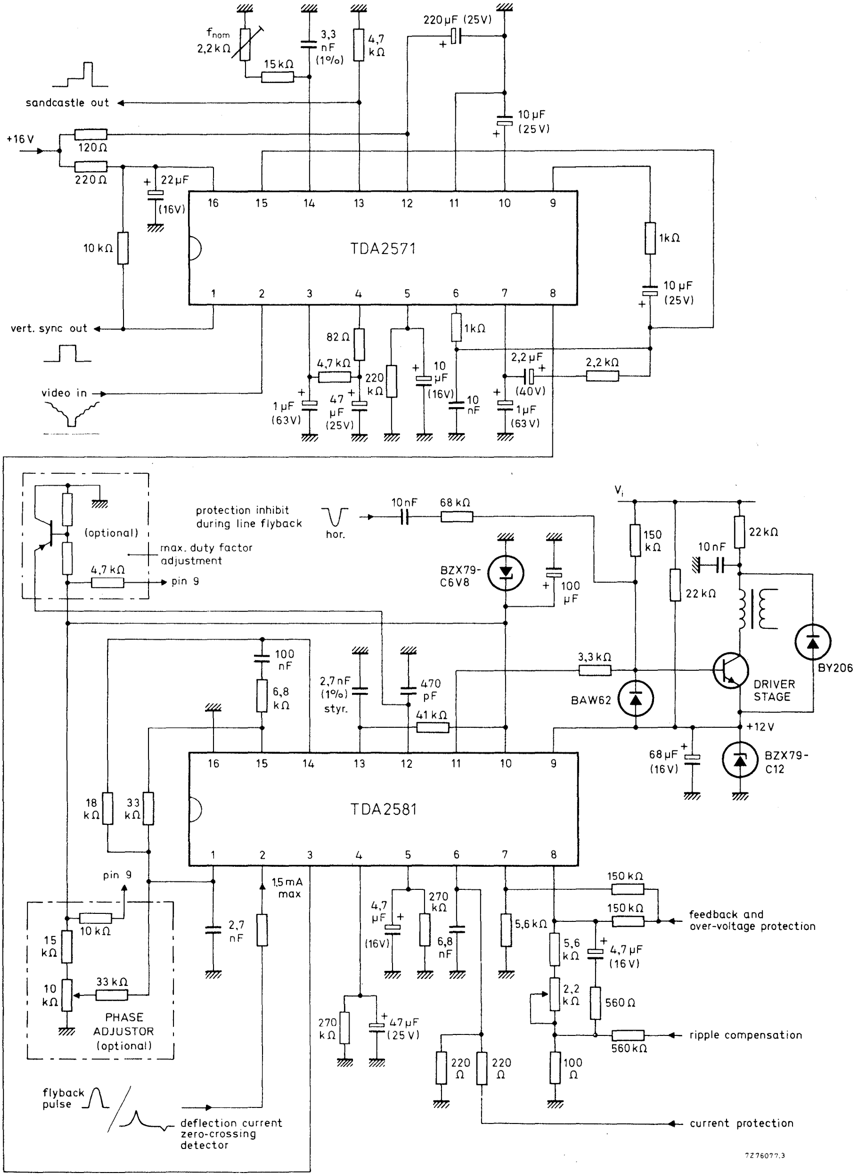
The maximum duty factor value can be set to a desired value (see application information pin 12 on page 321).

▲ For component values see circuit diagram on page 314.

PINNING

1. Phase detector output
2. Flyback pulse position input
3. Reference frequency input
4. Re-start count capacitor/remote control input
5. Slow start and transfer characteristic for low feedback voltages
6. Over-current protection input
7. Over-voltage protection input
8. Feedback voltage input
9. Positive supply
10. Reference input
11. Output
12. Maximum duty factor adjustment/smoothing
13. Oscillator timing network
14. Reactance stage reference voltage
15. Reactance stage input
16. Negative supply (ground)

APPLICATION INFORMATION



The TDA2571 and TDA2581 controlling an SMPS driver stage.

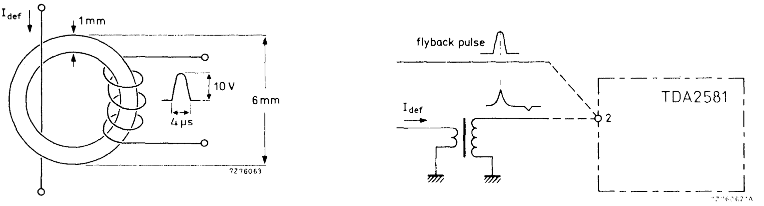
The function is quoted against the corresponding pin number

1. Phase detector output

   The output circuit consists of a bidirectional current source which is active for the time that the signal on pin 2 exceeds 1 V.
   The current values are chosen such that the correct phase relation is obtained when the reference signal on pin 3 is delivered by the TDA2571.
   With a resistor of 18 kΩ and a capacitor of 2,7 nF the control steepness is 0,55 V/µs.

2. Flyback pulse input

   The signal applied to pin 2 is normally a flyback pulse with a duration of about 12 µs. However, the phase detector system also accepts a signal derived by differentiating the deflection current by means of a small toroidal core (pulse duration > 3 µs).



(a) (b)

The toroidal transformer in (a) is for obtaining a pulse representing the mid-flyback from the deflection current. The connection of the picture phase information is shown in (b).

3. Reference frequency input

   The input circuit can be driven directly by the square-wave output voltage from pin 8 of the TDA2571.
   The negative-going transient switches the current source connected to pin 1 from positive to negative.
   The input circuit is made such that a differentiated signal of the square-wave from the TDA2571 is also accepted (this enables mains isolation). The input circuit switching level is about 3 V and the input impedance is about 10 kΩ.

4. Re-start count capacitor/remote control input

   Counting

   An external capacitor (C4 = 47 µF) is connected between pins 4 and 16. This capacitor controls the characteristics of the protection circuits as follows.
   If the protection circuits are required to operate, e.g. over-current at pin 6, the duty factor will be set to zero thus turning off the power supply.
   After a short interval (determined by the time constant on pin 5) the power supply will be restarted via the slow start circuit.
   If the fault condition has cleared, then normal operation will be resumed. If the fault condition is persistent, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated.

   The number of times this action is repeated (n) for a persisting fault condition is now determined by: n = C4/C5.

APPLICATION INFORMATION (continued)

Remote control input

For this application the capacitor on pin 4 has to be replaced by a resistor with a value between 4,7 and 18 kΩ. When the externally applied voltage $V_{4\text{-}16} > 5{,}8$ V, the circuit switches off; switching on occurs when $V_{4\text{-}16} < 4{,}5$ V and the normal starting-up procedure is followed. Pin 4 is internally connected to an emitter-follower, with an emitter voltage of 1,5 V.

5. Slow start and transfer characteristics for low feedback voltages

Slow start

An external shunt capacitor (C5 = 4,7 μF) and resistor (R5 = 270 kΩ) are connected between pins 5 and 16. The network controls the rate at which the duty factor increases from zero to its steady-state value after switch-on. It provides protection against surges in the power transistor.

Transfer characteristic for low feedback voltages

The duty factor transfer characteristic for low feedback voltages can be influenced by R5.
The transfer for three different resistor values is given in the graph on page 322.

6. Over-current protection input

A voltage proportional to the current in the power switching device is applied to the integrated circuit between pins 6 and 16. The circuit trips on both positive and negative polarity.

7. Over-voltage protection input

When the voltage applied to this pin exceeds the threshold level, the protection circuit will operate. When this function is not used, pin 7 should be connected to pin 16.

8. Feedback voltage input

The control loop input is applied to pin 8. This pin is internally connected to one input of a differential amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 10.
Under normal operating conditions, the voltage on pin 8 will be about equal to the reference voltage on pin 10. For further information refer to the graphs on pages 322 and 323.

9. 12 V positive supply

The maximum voltage that may be applied is 14 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 9 and 16 to ensure that the maximum voltage does not exceed 14 V. When the voltage on this pin falls below a minimum of 8,6 V (typically 9,4 V), the protection circuit will switch-off the power supply.

10. Reference input

An external reference diode must be connected between this pin and pin 16.
The reference voltage must be between 5,6 and 7,5 V. The IC delivers about 1 mA into the external regulator diode. When the external load on the regulator diode approaches this current, replenishment of the current can be obtained by connecting a suitable resistor between pins 9 and 10.

11. Output

    An external resistor determines the output current fed into the base of the driver transistor. The output circuit uses an n-p-n transistor with 3 series-connected clamping diodes to the internal 12 V supply rail. This provides a low impedance in the "ON" state, that is with the drive transistor turned-off.

12. Maximum duty factor adjustment/smoothing

    Maximum duty factor adjustment

    Pin 12 is connected to the output voltage of the amplitude comparator ($V_{10\text{-}8}$). This voltage is internally connected to one input of a differential amplifier, the other input of which is connected to the sawtooth voltage of the horizontal oscillator. A low voltage on pin 12 results in a low duty factor. This enables the maximum duty factor to be adjusted by limiting the voltage by connecting pin 12 to the emitter of a p-n-p transistor used as a voltage source.
    The graph on page 10 plots the maximum duty factor as a function of the voltage applied to pin 12.
    If some spread is acceptable the maximum duty factor can also be limited by connecting a resistor from pin 12 to pin 16. A resistor of 12 kΩ limits the maximum duty factor to about 50%.
    This application also reduces the total IC gain.

    Smoothing

    Any double pulsing of the IC due to circuit layout can be suppressed by connecting a capacitor of about 470 pF between pins 12 and 16.

13. Oscillator timing network

    The timing network comprises a capacitor between pins 13 and 16, and a resistor between pin 13 and the reference voltage on pin 10.
    The charging current for the capacitor (C13) is derived from the voltage reference diode connected to pin 10 and discharged via an internal resistor of about 330 Ω.

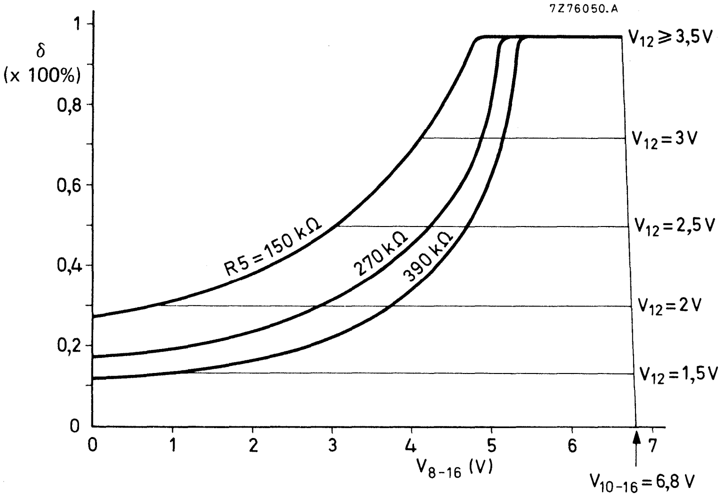
14. Reactance stage reference voltage

    This pin is connected to an emitter follower which determines the nominal reference voltage for the reactance stage (1,5 V for reference voltage $V_{10\text{-}16} = 6{,}7$ V). Free-running frequency is obtained when pins 14 and 15 are short-circuited.

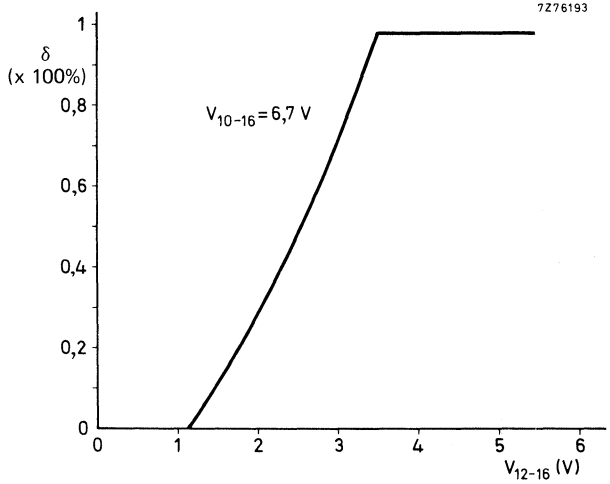
15. Reactance stage input

    The output voltage of the phase detector (pin 1) is connected to pin 15 via a resistor. The voltage applied to pin 15 shifts the upper level of the voltage sensor of the oscillator thus changing the oscillator frequency and phase. The time constant network is connected between 14 and 15.
    Control sensitivity is typically 4,5 kHz/V.

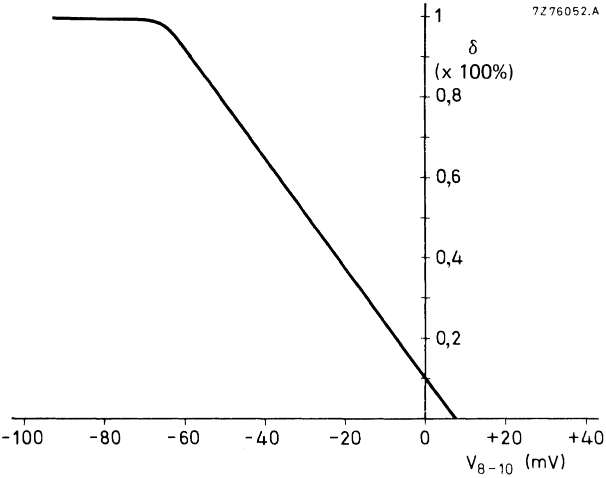
16. Negative supply (ground)



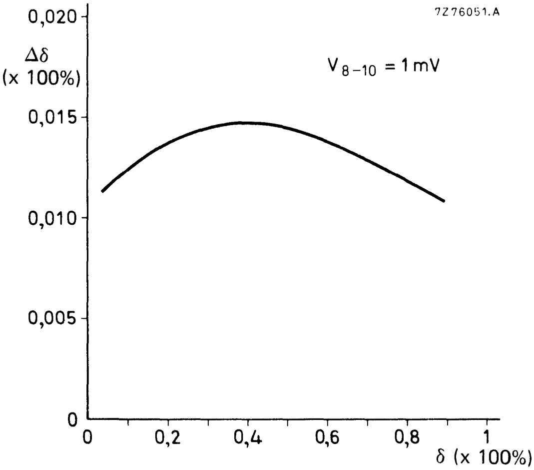
Duty factor of output pulses as a function of $V_{8\text{-}16}$ with R5 as a parameter, and with V_{12} as a limiting value; $V_{10\text{-}16} = 6,8$ V.



Maximum duty factor limitation as a function of $V_{12\text{-}16}$.



Duty factor of output pulses as a function of error amplifier input (V_{8-10}).



Change in duty factor of output pulses for a 1 mV error amplifier input change (V_{8-10}) as a function of initial duty factor.

CONTROL CIRCUIT FOR POWER SUPPLIES

The TDA2582 is a monolithic integrated circuit for controlling power supplies which are provided with the drive for the horizontal deflection stage.
The circuit features the following:

- Voltage controlled horizontal oscillator.
- Phase detector.
- Duty factor control for the negative-going transient of the output signal.
- Duty factor increases from zero to its normal operation value.
- Adjustable maximum duty factor.
- Over-voltage and over-current protection with automatic re-start after switch-off.
- Counting circuit for permanent switch-off when n-times over-current or over-voltage is sensed.
- Protection for open-reference voltage.
- Protection for too low supply voltage.
- Protection against loop faults.
- Positive tracking of duty factor and feedback voltage when the feedback voltage is smaller than the reference voltage minus 1,5 V.
- Normal and 'smooth' remote ON/OFF possibility.

QUICK REFERENCE DATA

Supply voltage	$V_{9\text{-}16}$	typ.	12	V
Supply current	I_9	typ.	14	mA
Input signals				
Horizontal drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$		5 to 11	V
Flyback pulse (differentiated deflection current); peak-to-peak value	$V_{2\text{-}16(p\text{-}p)}$		1 to 5	V
External reference voltage	$V_{10\text{-}16}$	typ.	6,1	V
Output signals				
Duty factor of output pulse	δ	> <	0 98 ± 0,8	% %
Output voltage at $I_O < 20$ mA (peak value)	$V_{11\text{-}16M}$	typ.	11,8	V
Output current (peak value)	I_{11M}	<	40	mA

PACKAGE OUTLINES

TDA2582 : 16-lead DIL; plastic (SOT-38).
TDA2582Q: 16-lead QIL; plastic (SOT-58).

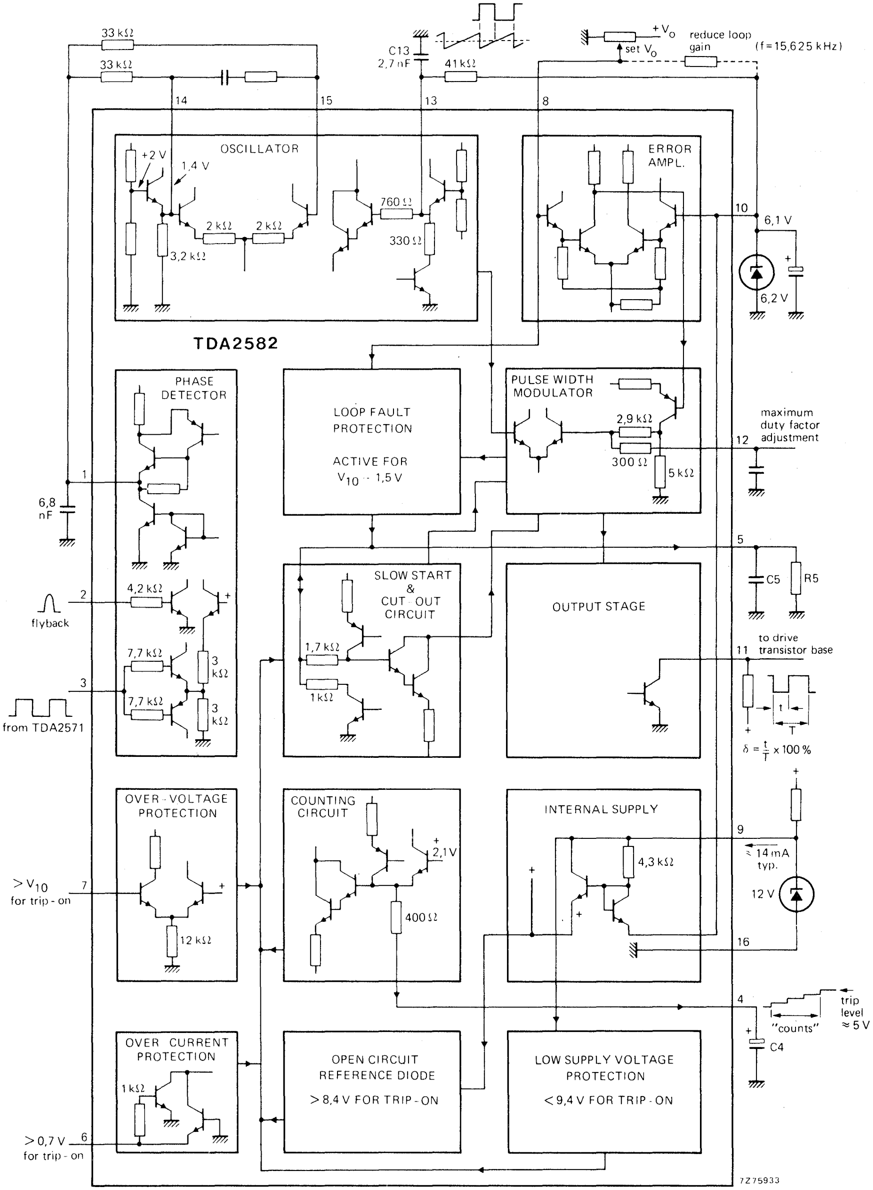


Fig. 1 Block diagram.

Note: trip levels are nominal values.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage at pin 9	$V_{9\text{-}16}$	max.	14	V
Voltage at pin 11	$V_{11\text{-}16}$		0 to 14	V
Output current (peak value)	I_{11M}	max.	40	mA
Total power dissipation	P_{tot}	max.	280	mW
Storage temperature	T_{stg}		−25 to + 125	°C
Operating ambient temperature	T_{amb}		−25 to + 80	°C

CHARACTERISTICS

$V_{9\text{-}16} = 12$ V; $V_{10\text{-}16} = 6{,}1$ V; $T_{amb} = 25$ °C; measured in Fig. 4

Supply voltage range	$V_{9\text{-}16}$	typ.	12	V
			10 to 14	V
Protection voltage too low supply voltage	$V_{9\text{-}16}$	typ.	9,4	V
			8,6 to 9,9	V
Supply current at $\delta = 50\%$	I_9	typ.	14	mA
Supply current during protection	I_9	typ.	14	mA
Minimum required supply current (note 1)	I_9	<	17	mA
Power consumption	P	typ.	170	mW
Required input signals				
Reference voltage (note 2)	$V_{10\text{-}16}$	typ.	6,1	V
			5,6 to 6,6	V
Feedback input impedance	$\lvert Z_{8\text{-}16}\rvert$	typ.	200	kΩ
High reference voltage protection: threshold voltage	$V_{10\text{-}16}$	typ.	8,4	V
			7,9 to 8,9	V
Horizontal reference signal (square-wave or differentiated; negative transient is reference)				
Voltage driven (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$		5 to 12	V
Current driven (peak value)	I_{3M}		−1 to + 1,5	mA
Switching level current	$\pm I_3$	<	100	μA
Flyback pulse or differential deflection current	$V_{2\text{-}16}$		1 to 5	V
Flyback pulse current (peak value)	I_{2M}	<	1,5	mA
Over-current protection: (note 3) threshold voltage	$-V_{6\text{-}16}$	typ.	640	mV
			600 to 695	mV
	$+V_{6\text{-}16}$	typ.	680	mV
			640 to 735	mV

Notes

1. This value refers to the minimum required supply current that will start all devices under the following conditions: $V_{9\text{-}16} = 10$ V; $V_{10\text{-}16} = 6{,}2$ V; $\delta = 50\%$.
2. Voltage obtained via an external reference diode. Specified voltages do not refer to the nominal voltages of reference diodes.
3. This spread is inclusive temperature rise of the IC due to warming up. For other ambient temperatures the values must be corrected by using a temperature coefficient of typical −1,85 mV/°C.

CHARACTERISTICS (continued)

Over-voltage protection: ($V_{ref} = V_{10-16}$) threshold voltage	V_{7-16}	typ.	$V_{ref}-60$	mV
			$V_{ref}-130$ to $V_{ref}-0$	mV
Remote control voltage; switch-off (note 1)	V_{4-16}	>	5,6	V
Remote control voltage; switch-on	V_{4-16}	<	4,5	V
'Smooth' remote control; switch-off (note 2)	V_{5-16}	>	4,5	V
'Smooth' remote control; switch-on	V_{5-16}	<	3	V
Remote control switch-off current	I_4	<	1	mA

Delivered output signals

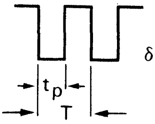
Horizontal drive pulse (loaded with a resistor of 560 Ω to + 12 V peak-to-peak value	$V_{11-16(p-p)}$	>	11,6	V
Output current; peak value	I_{11M}	<	40	mA
Saturation voltage of output transistor at I_{11} = 20 mA	V_{CEsat}	typ.	200	mV
		<	400	mV
at I_{11} = 40 mA	V_{CEsat}	<	525	mV
Duty factor of output pulse (note 3)	δ	>	0	%
		<	98 ± 0,8	%
Charge current for capacitor on pin 4	I_4	typ.	110	μA
Charge current for capacitor on pin 5	I_5	typ.	120	μA
Supply current for reference	I_{10}	typ.	1	mA
			0,6 to 1,45	mA

Oscillator

Temperature coefficient		typ.	0,0003	$^{o}C^{-1}$
		<	0,0004	$^{o}C^{-1}$
Relative frequency deviation for V_{10-16} changing from 5,6 to 6,6 V		typ.	−1,4	%
		<	−2	%
Oscillator frequency spread (with fixed external components)		<	3	%
Frequency control sensitivity at pin 15 f_{nom} = 15,625 kHz		typ.	5	kHz/V

Notes

1. See function description pin 4 (pages 333 and 334).
2. See function description pin 5 (page 334).
3. The duty factor is specified as follows: $\delta = \frac{t_p}{T} \times 100\%$ (see Fig. 2). After switch-on the duty factor rises gradually from 0% to the steady value. The relationship between V_{8-16} and the duty factor is given in Fig. 7 and the relationship between V_{12-16} and the duty factor is shown in Fig. 9.



$\delta = \frac{t_p}{T} \times 100\%.$

Fig. 2.

Phase control loop

Loop gain of APC-system (automatic phase control) *		typ.	5	kHz/μs
Catching range (f_{nom} = 15,625 kHz)	Δf	> <	1300 2100	Hz Hz
Phase relation between negative transient of sync pulse and middle of flyback	t	typ.	1	μs
Tolerance of phase relation	Δt	⩽	± 0,4	μs

PINNING

1. Phase detector output	9. Positive supply
2. Flyback pulse position input	10. Reference input
3. Reference frequency input	11. Output
4. Re-start count capacitor/remote control input	12. Maximum duty factor adjustment/smoothing
5. Slow start and transfer characteristic for low feedback voltages	13. Oscillator timing network
6. Over-current protection input	14. Reactance stage reference voltage
7. Over-voltage protection input	15. Reactance stage input
8. Feedback voltage input	16. Negative supply (ground)

---

* For component values see Fig. 1.

APPLICATION INFORMATION

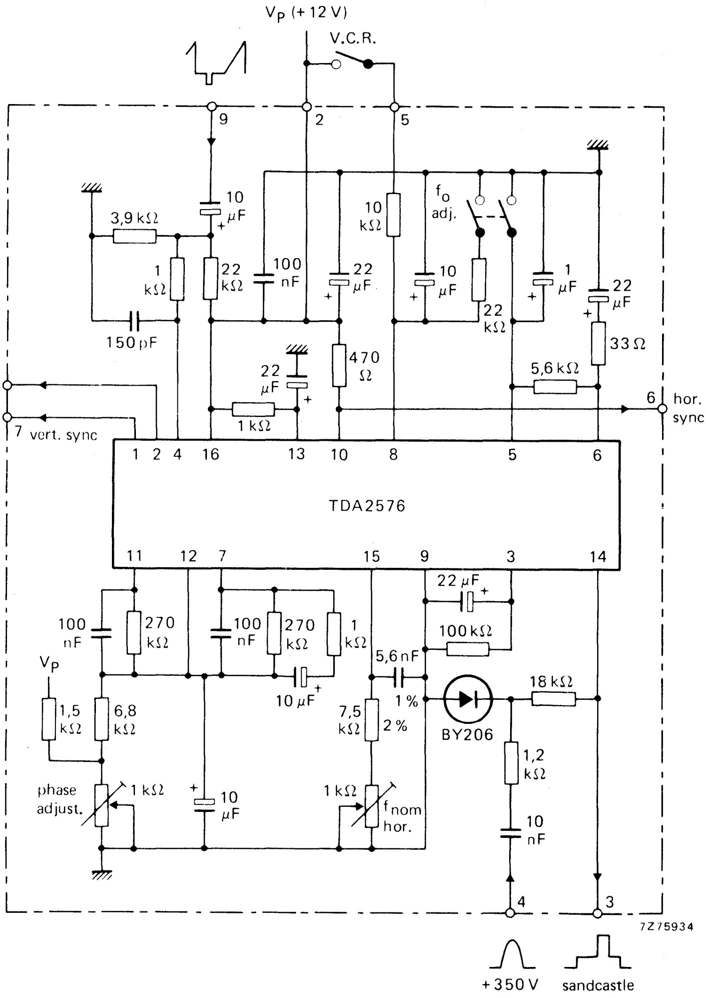


Fig. 3a.

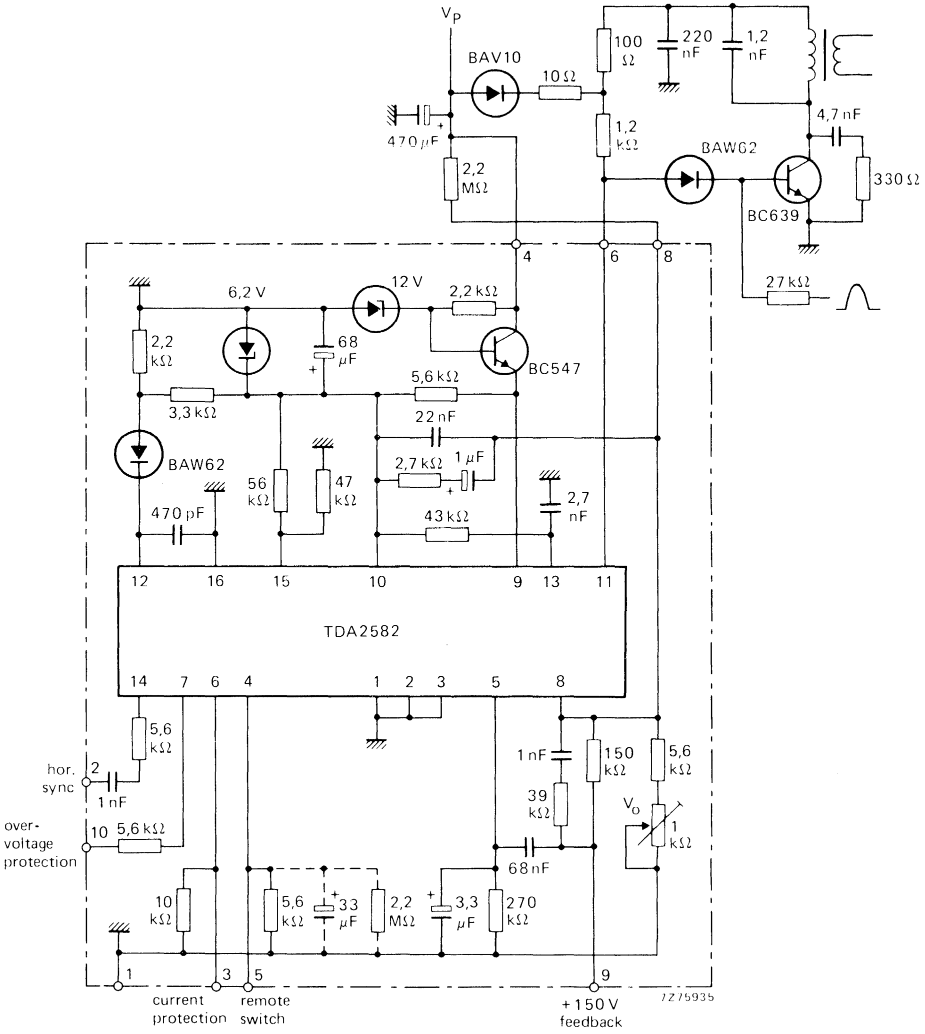


Fig. 3b.

Lead 6 (pin 10) of circuit TDA2576 connected to lead 2 (pin 14) of circuit TDA2582.

APPLICATION INFORMATION

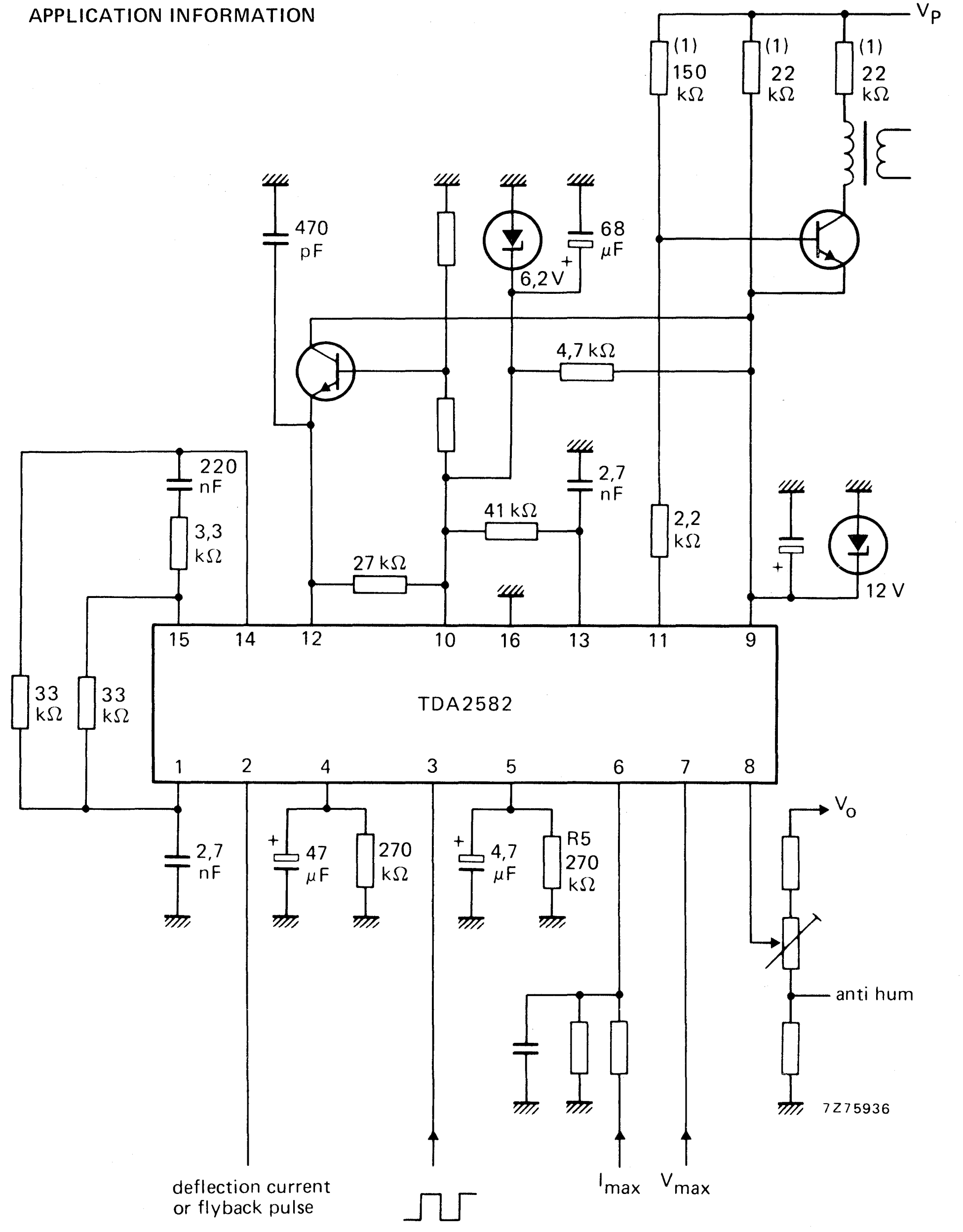


Fig. 4 Circuit diagram.

The function is described against the corresponding pin number

1. Phase detector output

The output circuit consists of a bidirectional current source which is active for the time that the signal on pin 2 exceeds 1 V.
The current values are chosen such that the correct phase relation is obtained when the output signal of the TDA2571 is applied to pin 3.
With a resistor of 2 x 33 kΩ and a capacitor of 2,7 nF the control steepness is 0,55 V/μs (Fig. 4).

2. Flyback pulse input

The signal applied to pin 2 is normally a flyback pulse with a duration of about 12 μs. However, the phase detector system also accepts a signal derived by differentiating the deflection current by means of a small toroidal core (pulse duration > 3 μs).

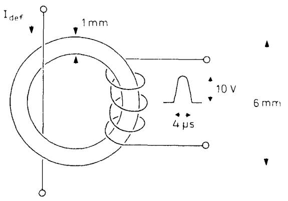


Fig. 5a.

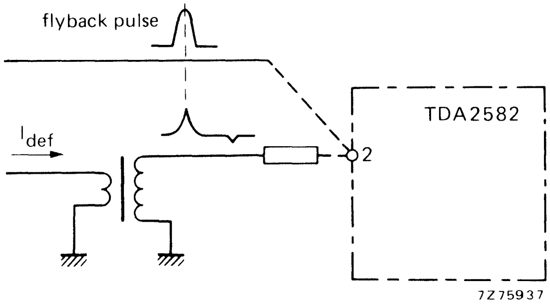


Fig. 5b.

The toroidal transformer in Fig. 5a is for obtaining a pulse representing the mid-flyback from the deflection current. The connection of the picture phase information is shown in Fig. 5b.

3. Reference frequency input

The input circuit can be driven directly by the square-wave output voltage from pin 8 of the TDA2571.
The negative-going transient switches the current source connected to pin 1 from positive to negative. The input circuit is made such that a differentiated signal of the square-wave from the TDA2571 is also accepted (this enables mains isolation). The input circuit switching level is about 3 V and the input impedance is about 8 kΩ.

4. Re-start count capacitor/remote control input

Counting

An external capacitor (C4 = 47 μF) is connected between pins 4 and 16. This capacitor controls the characteristics of the protection circuits as follows.
If the protection circuits are required to operate, e.g. over-current at pin 6, the duty factor will be set to zero thus turning off the power supply.
After a short interval (determined by the time constant on pin 5) the power supply will be restarted via the slow start circuit.
If the fault condition has cleared, then normal operation will be resumed. If the fault condition is persistent, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated.

The number of times this action is repeated (n) for a persisting fault condition is now determined by: n = C4/C5.

APPLICATION INFORMATION (continued)

Remote control input

For this application the capacitor on pin 4 has to be replaced by a resistor with a value between 4,7 and 18 kΩ. When the externally applied voltage $V_{4\text{-}16} > 5{,}6$ V, the circuit switches off; switching on occurs when $V_{4\text{-}16} < 4{,}5$ V and the normal starting-up procedure is followed. Pin 4 is internally connected to an emitter-follower, with an emitter voltage of 1,5 V.

5. Slow start and transfer characteristics for low feedback voltages

Slow start

An external shunt capacitor (C5 = 4,7 μF) and resistor (R5 = 270 kΩ) are connected between pins 5 and 16. The network controls the rate at which the duty factor increases from zero to its steady-state value after switch-on. It provides protection against surges in the power transistor.

Transfer characteristic for low feedback voltages

The duty factor transfer characteristic for low feedback voltages can be influenced by R5.
The transfer for three different resistor values is given in Fig. 7.

'Smooth' remote ON/OFF

The ON/OFF information should be applied to pin 5 via a high ohmic resistor, a high OFF-level gives a slow rising voltage at pin 5, which results in a slowly decreasing duty factor.

6. Over-current protection input

A voltage proportional to the current in the power switching device is applied to the integrated circuit between pins 6 and 16. The circuit trips on both positive and negative polarity. When the tripping level is reached, the output pulse is immediately blocked and the starting circuit is activated again.

7. Over-voltage protection input

When the voltage applied to this pin exceeds the threshold level the protection circuit will operate. The tripping level is about the same as the reference voltage on pin 10.

8. Feedback voltage input

The control loop input is applied to pin 8. This pin is internally connected to one input of a differential amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 10.
Under normal operating conditions, the voltage on pin 8 will be about equal to the reference voltage on pin 10. For further information refer to the Figs 7 and 8.

9. 12 V positive supply

The maximum voltage that may be applied is 14 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 9 and 16 to ensure that the maximum voltage does not exceed 14 V. When the voltage on this pin falls below a minimum of 8,6 V (typically 9,4 V), the protection circuit will switch-off the power supply.

10. Reference input

An external reference diode must be connected between this pin and pin 16.
The reference voltage must be between 5,6 and 6,6 V. The IC delivers about 1 mA into the external regulator diode. When the external load on the regulator diode approaches this current, replenishment of the current can be obtained by connecting a suitable resistor between pins 9 and 10. A higher reference voltage value up to 7,5 V is allowed when use is made of a duty factor limiting resistor < 27 kΩ between pins 12 and 16.

11. Output

An external resistor determines the output current fed into the base of the driver transistor. The output circuit uses an n-p-n transistor with 3 series-connected clamping diodes to the internal 12 V supply rail. This provides a low impedance in the "ON" state, that is with the drive transistor turned-off.

12. Maximum duty factor adjustment/smoothing

Maximum duty factor adjustment

Pin 12 is connected to the output voltage of the amplitude comparator ($V_{10\text{-}8}$). This voltage is internally connected to one input of a differential amplifier, the other input of which is connected to the sawtooth voltage of the horizontal oscillator. A high voltage on pin 12 results in a low duty factor. This enables the maximum duty factor to be adjusted by limiting the voltage by connecting pin 12 to the emitter of an n-p-n transistor used as a voltage source.
Fig. 9 plots the maximum duty factor as a function of the voltage applied to pin 12. If some spread is acceptable the maximum duty factor can also be limited by connecting a resistor from pin 12 to pin 16. A resistor of 12 kΩ limits the maximum duty factor to about 50%. This application also reduces the total IC gain.

Smoothing

Any double pulsing of the IC due to circuit layout can be suppressed by connecting a capacitor of about 470 pF between pins 12 and 16.

13. Oscillator timing network

The timing network comprises a capacitor between pins 13 and 16, and a resistor between pin 13 and the reference voltage on pin 10.
The charging current for the capacitor (C13) is derived from the voltage reference diode connected to pin 10 and discharged via an internal resistor of about 330 Ω.

14. Reactance stage reference voltage

This pin is connected to an emitter follower which determines the nominal reference voltage for the reactance stage (1,4 V for reference voltage $V_{10\text{-}16} = 6,1$ V). Free-running frequency is obtained when pins 14 and 15 are short-circuited.

15. Reactance stage input

The output voltage of the phase detector (pin 1) is connected to pin 15 via a resistor. The voltage applied to pin 15 shifts the upper level of the voltage sensor of the oscillator thus changing the oscillator frequency and phase. The time constant network is connected between 14 and 15. Control sensitivity is typically 5 kHz/V.

16. Negative supply (ground)

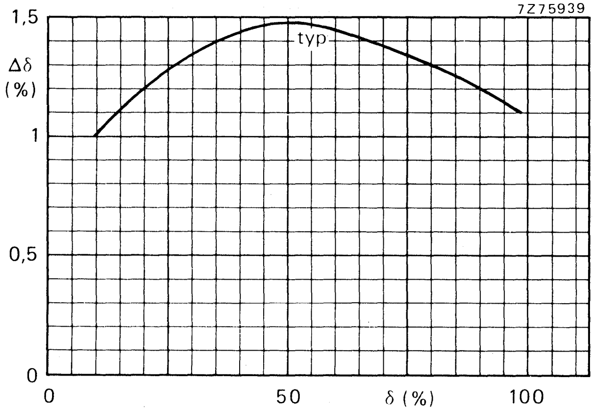


Fig. 6 Duty factor change as a function of initial duty factor; at 1 mV error amplifier input change; $\Delta V_{8\text{-}10(p\text{-}p)} = 1$ mV.

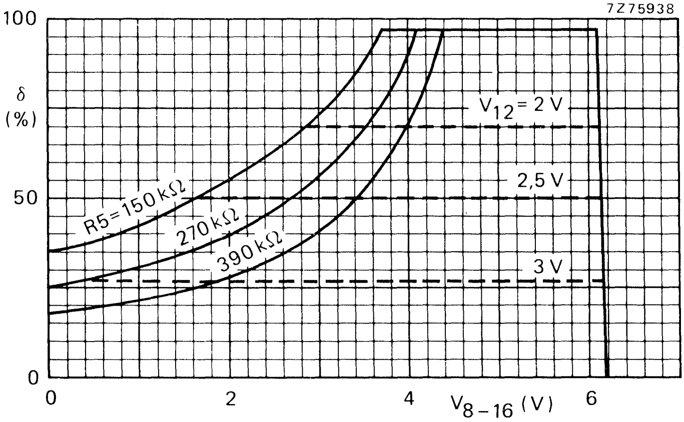


Fig. 7 Duty factor of output pulses as a function of feedback input voltage ($V_{8\text{-}16}$) with R5 as a parameter and $V_{12\text{-}16}$ as a limiting value; $V_{10\text{-}16} = 6{,}1$ V.

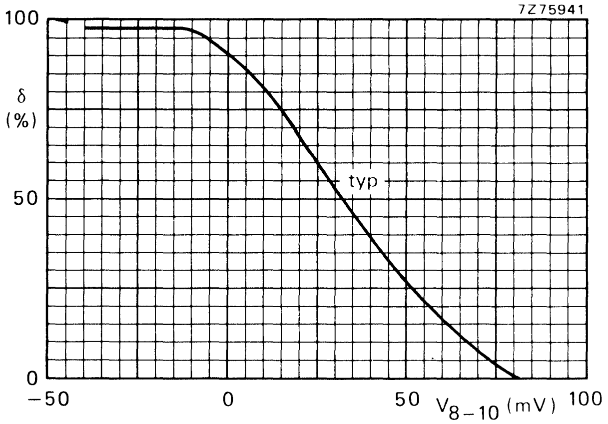


Fig. 8 Duty factor of output pulses as a function of error amplifier input ($V_{8\text{-}10}$); $V_{10\text{-}16}$ = 6,1 V.

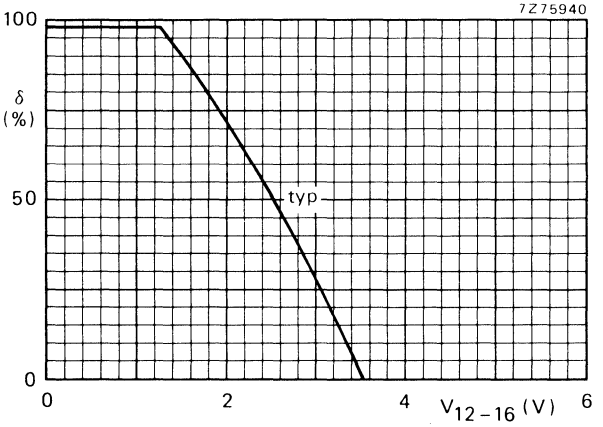


Fig. 9 Maximum duty factor limitation as a function of the voltage applied to pin 12; $V_{10\text{-}16}$ = 6,1 V.

HORIZONTAL COMBINATION

The TDA2593 is a monolithic integrated circuit intended for use in colour television receivers in combination with TDA2510, TDA2520, TDA2560 as well as with TDA3500, TDA3510 and TDA3520. The circuit incorporates the following functions:

- horizontal oscillator based on the threshold switching principle
- phase comparison between sync pulse and oscillator voltage (φ_1)
- internal key pulse for phase detector (φ_1) (additional noise limiting)
- phase comparison between line flyback pulse and oscillator voltage (φ_2)
- larger catching range obtained by coincidence detector (φ_3; between sync and key pulse)
- switch for changing the filter characteristic and the gate circuit (VCR-operation)
- sync separator
- noise separator
- vertical sync separator and output stage
- colour burst keying and line flyback blanking pulse generator
- phase shifter for the output pulse
- output pulse duration switching
- output stage with separate supply voltage for direct drive of thyristor deflection circuits
- low supply voltage protection

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}16}$	typ.	12	V
Supply current	I_1	typ.	30	mA
Input signals				
Sync separator input voltage (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$		3 to 4	V
Noise separator input voltage (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		3 to 4	V
Pulse duration switch input voltage				
at t = 7 μs (thyristor driving)	$V_{4\text{-}16}$		9,4 to $V_{1\text{-}16}$	V
at t = 14 μs + t_d (transistor driving)	$V_{4\text{-}16}$		0 to 3,5	V
at t = 0 (input 4 open or $V_{3\text{-}16}$ = 0)	$V_{4\text{-}16}$		5,4 to 6,6	V
Output signals				
Vertical sync output pulse (peak-to peak value)	$V_{8\text{-}16(p\text{-}p)}$	typ.	11	V
Burst gating output pulse (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	typ.	11	V
Line drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10,5	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

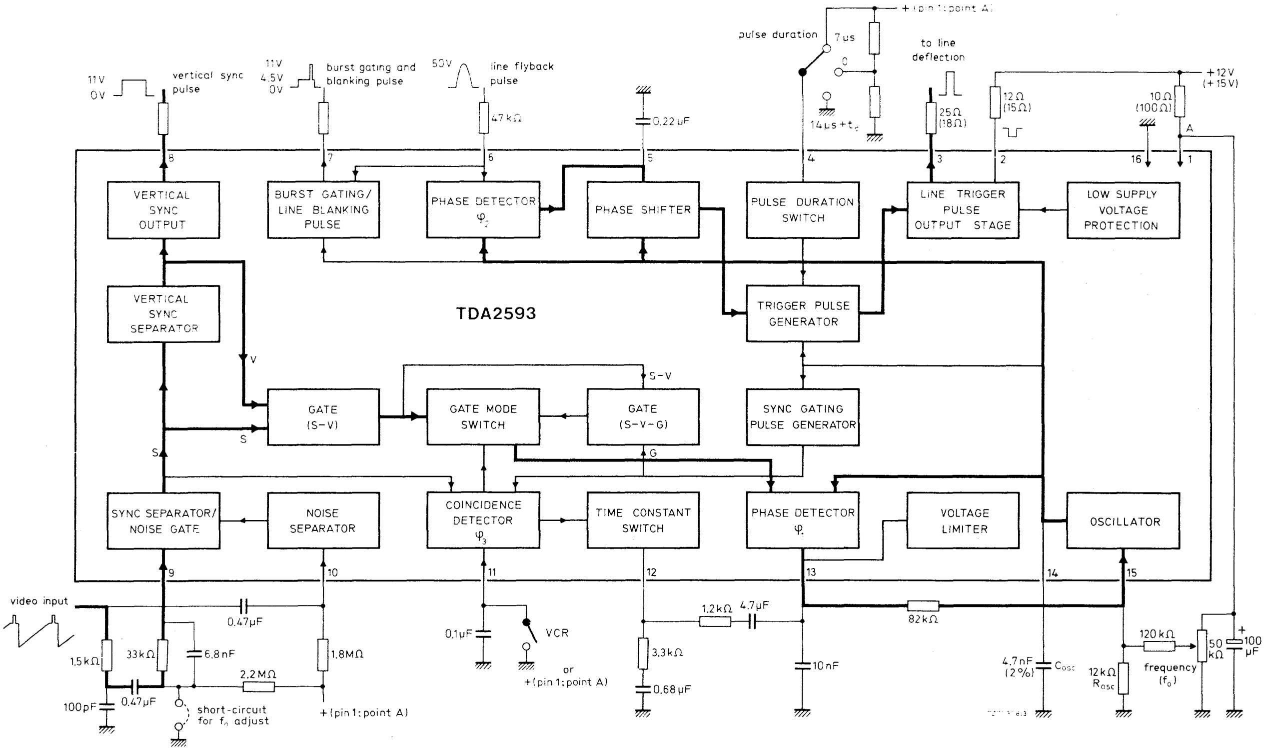


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage				
at pin 1 (voltage source)	$V_{1\text{-}16}$	max.	13,2	V
at pin 2	$V_{2\text{-}16}$	max.	18	V
Voltages				
Pin 4	$V_{4\text{-}16}$	max.	13,2	V
Pin 9	$\pm V_{9\text{-}16}$	max.	6	V
Pin 10	$\pm V_{10\text{-}16}$	max.	6	V
Pin 11	$V_{11\text{-}16}$	max.	13,2	V
Currents				
Pins 2 and 3 (thyristor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	650	mA
Pins 2 and 3 (transistor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	400	mA
Pin 4	I_4	max.	1	mA
Pin 6	$\pm I_6$	max.	10	mA
Pin 7	$-I_7$	max.	10	mA
Pin 11	I_{11}	max.	2	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−25 to + 125	°C
Operating ambient temperature	T_{amb}		−20 to + 70	°C

CHARACTERISTICS at $V_{1\text{-}16} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

Sync separator

Input switching voltage	$V_{9\text{-}16}$	typ.	0,8	V
Input keying current	I_9		5 to 100	µA
Input leakage current at $V_{9\text{-}16} = -5$ V	I_9	$<$	1	µA
Input switching current	I_9	$\leq$	5	µA
Switch off current	I_9	$>$ typ.	100 150	µA µA
Input signal (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$		3 to 4	V*

---

* Permissible range 1 to 7 V.

Noise separator

Input switching voltage	V_{10-16}	typ.	1,4	V
Input keying current	I_{10}		5 to 100	μA
Input switching current	I_{10}	> typ.	100 150	μA μA
Input leakage current at $V_{10-16} = -5$ V	I_{10}	<	1	μA
Input signal (peak-to-peak value)	$V_{10-16(p-p)}$		3 to 4	V *
Permissible superimposed noise signal (peak-to-peak value)	$V_{10-16(p-p)}$	<	7	V

Line flyback pulse

Input current	I_6	typ.	1 0,02 to 2	mA mA
Input switching voltage	V_{6-16}	typ.	1,4	V
Input limiting voltage	V_{6-16}		−0,7 to + 1,4	V

Switching on VCR

Input voltage	V_{11-16} V_{11-16}		0 to 2,5 9 to V_{1-16}	V V
Input current	$-I_{11}$ I_{11}	< <	200 2	μA mA

Pulse duration switch

For t = 7 μs (thyristor driving)				
Input voltage	V_{4-16}		9,4 to V_{1-16}	V
Input current	I_4	>	200	μA
For t = 14 μs + t_d (transistor driving)				
Input voltage	V_{4-16}		0 to 3,5	V
Input current	$-I_4$	>	200	μA
For t = 0; $V_{3-16} = 0$ or input pin 4 open				
Input voltage	V_{4-16}		5,4 to 6,6	V
Input current	I_4	typ.	0	μA

---

* Permissible range 1 to 7 V.

Vertical sync pulse (positive-going)

Output voltage (peak-to-peak value)	$V_{8\text{-}16(p\text{-}p)}$	> typ.	10 11	V V
Output resistance	R_8	typ.	2	kΩ
Delay between leading edge of input and output signal	t_{on}	typ.	15	μs
Delay between trailing edge of input and output signal	t_{off}	typ.	t_{on}	μs

Burst gating pulse (positive-going)

Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	> typ.	10 11	V V
Output resistance	R_7	typ.	70	Ω
Pulse duration; $V_{7\text{-}16} = 7$ V	t_p	typ.	4 3,7 to 4,3	μs μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse; $V_{7\text{-}16} = 7$ V	t	typ.	2,65 2,15 to 3,15	μs μs
Output trailing edge current	I_7	typ.	2	mA

Line flyback-blanking pulse (positive-going)

Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$		4 to 5	V
Output resistance	R_7	typ.	70	Ω
Output trailing edge current	I_7	typ.	2	mA

Line drive pulse (positive-going)

Output voltage (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10,5	V
Output resistance				
for leading edge of line pulse	R_3	typ.	2,5	Ω
for trailing edge of line pulse	R_3	typ.	20	Ω
Pulse duration (thyristor driving) $V_{4\text{-}16} = 9{,}4$ to $V_{1\text{-}16}$ V	t_p	typ.	7 5,5 to 8,5	μs μs
Pulse duration (transistor driving) $V_{4\text{-}16} = 0$ to 4 V; $t_{fp} = 12$ μs	t_p		14 + t_d	μs*
Supply voltage for switching off the output pulse	$V_{1\text{-}16}$	typ.	4	V

Overall phase relation

Phase relation between middle of sync pulse and the middle of the flyback pulse	t	typ.	2,6	μs**
Tolerance of phase relation	$\lvert \Delta t \rvert$	<	0,7	μs

---

* t_d = switch-off delay of line output stage.

** Line flyback pulse duration t_{fp} = 12 μs.

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2.

If additional adjustment is applied it can be arranged by current supply at pin 5 such that	$\Delta I_5/\Delta t$	typ.	30	μA/μs

Oscillator

Threshold voltage low level	$V_{14\text{-}16}$	typ.	4,4	V
Threshold voltage high level	$V_{14\text{-}16}$	typ.	7,6	V
Discharge current	$\pm I_{14}$	typ.	0,47	mA
Frequency; free running (C_{osc} = 4,7 nF; R_{osc} = 12 kΩ)	f_o	typ.	15,625	kHz
Spread of frequency	$\Delta f_o/f_o$	$<$	± 5	%*
Frequency control sensitivity	$\Delta f_o/\Delta I_{15}$	typ.	31	Hz/μA
Adjustment range of network in circuit (Fig. 1)	$\Delta f_o/f_o$	typ.	± 10	%
Influence of supply voltage on frequency	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	$<$	± 0,05	%*
Change of frequency when $V_{1\text{-}16}$ drops to 5 V	Δf_o	$<$	± 10	%*
Temperature coefficient of oscillator frequency		$<$	$\pm 10^{-4}$	Hz/K*

Phase comparison φ_1

Control voltage range	$V_{13\text{-}16}$		3,8 to 8,2	V
Control current (peak value)	$\pm I_{13M}$		1,9 to 2,3	mA
Output leakage current at $V_{13\text{-}16}$ = 4 to 8 V	I_{13}	$<$	1	μA
Output resistance at $V_{13\text{-}16}$ = 4 to 8 V	R_{13}	high ohmic		**
at $V_{13\text{-}16} < 3{,}8$ V or $> 8{,}2$ V	R_{13}	low ohmic		▲
Control sensitivity		typ.	2	kHz/μs
Catching and holding range (82 kΩ beteeen pins 13 and 15)	Δf	typ.	± 780	Hz
Spread of catching and holding range	$\Delta(\Delta f)$	typ.	± 10	%*

---

* Excluding external component tolerances.

** Current source.

▲ Emitter follower.

Phase comparison φ_2 and phase shifter				
Control voltage range	$V_{5\text{-}16}$		5,4 to 7,6	V
Control current (peak value)	$\pm I_{5M}$	typ.	1	mA
Output resistance				
at $V_{5\text{-}16} = 5{,}4$ to $7{,}6$ V		high ohmic		*
at $V_{5\text{-}16} < 5{,}4$ V or $> 7{,}6$ V	R_5	typ.	8	kΩ
Input leakage current				
$V_{5\text{-}16} = 5{,}4$ to $7{,}6$ V	I_5	<	5	μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse ($t_{fp} = 12$ μs)	t_d	<	15	μs
Static control error	$\Delta t/\Delta t_d$	<	0,2	%
Coincidence detector φ_3				
Output voltage	$V_{11\text{-}16}$		0,5 to 6	V
Output current (peak value)				
without coincidence	I_{11M}	typ.	0,1	mA
with coincidence	$-I_{11M}$	typ.	0,5	mA
Time constant switch				
Output voltage	$V_{12\text{-}16}$	typ.	6	V
Output current (limited)	$\pm I_{12}$	<	1	mA
Output resistance				
at $V_{11\text{-}16} = 2{,}5$ to 7 V	R_{12}	typ.	0,1	kΩ
at $V_{11\text{-}16} < 1{,}5$ V or > 9 V	R_{12}	typ.	60	kΩ
Internal gating pulse				
Pulse duration	t_p	typ.	7,5	μs

---

* Current source.

HORIZONTAL COMBINATION

The TDA2594 is a monolithic integrated circuit intended for use in colour television receivers. The circuit incorporates the following functions:

- Horizontal oscillator based on the threshold switching principle.
- Phase comparison between sync pulse and oscillator voltage (φ_1).
- Internal key pulse for phase detector (φ_1) (additional noise limiting).
- Phase comparison between line flyback pulse and oscillator voltage (φ_2).
- Larger catching range obtained by coincidence detector (φ_3; between sync and key pulse).
- Switch for changing the filter characteristic and the gate circuit (VCR-operation).
- Sync separator.
- Noise separator.
- Vertical sync separator and output stage.
- Colour burst keying and line flyback blanking pulse generator and clamp circuit for vertical blanking.
- Phase shifter for the output pulse.
- Output pulse duration for transistor deflection systems.
- External switching off of the line trigger pulse.
- Output stage with separate supply voltage.
- Low supply voltage protection.
- Transmitter identification and muting circuit, and vertical sync switch-off.

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}18} = V_S$	typ.	12	V
Supply current	I_1	typ.	30	mA
Input signals				
Sync separator input voltage (peak-to-peak value)	$V_{11\text{-}18(p\text{-}p)}$	typ.	3	V*
Noise separator input voltage (peak-to-peak value)	$V_{12\text{-}18(p\text{-}p)}$	typ.	3	V*
Pulse duration switch input voltage				
at t = 14 μs + t_d (transistor driving)	$V_{4\text{-}18}$		0 to 3,5	V
at t = 0 ($V_{3\text{-}18}$ = 0); input 4 open (I_4 = 0)	$V_{4\text{-}18}$		5,4 to 6,6	V
Output signals				
Vertical sync output pulse (peak-to-peak value)	$V_{8\text{-}18(p\text{-}p)}$	typ.	11	V
Burst key output pulse (peak-to-peak value)	$V_{7\text{-}18(p\text{-}p)}$	typ.	11	V
Line drive-pulse (peak-to-peak value)	$V_{3\text{-}18(p\text{-}p)}$	typ.	10	V

* Permissible range: 1 to 7 V.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102DS).

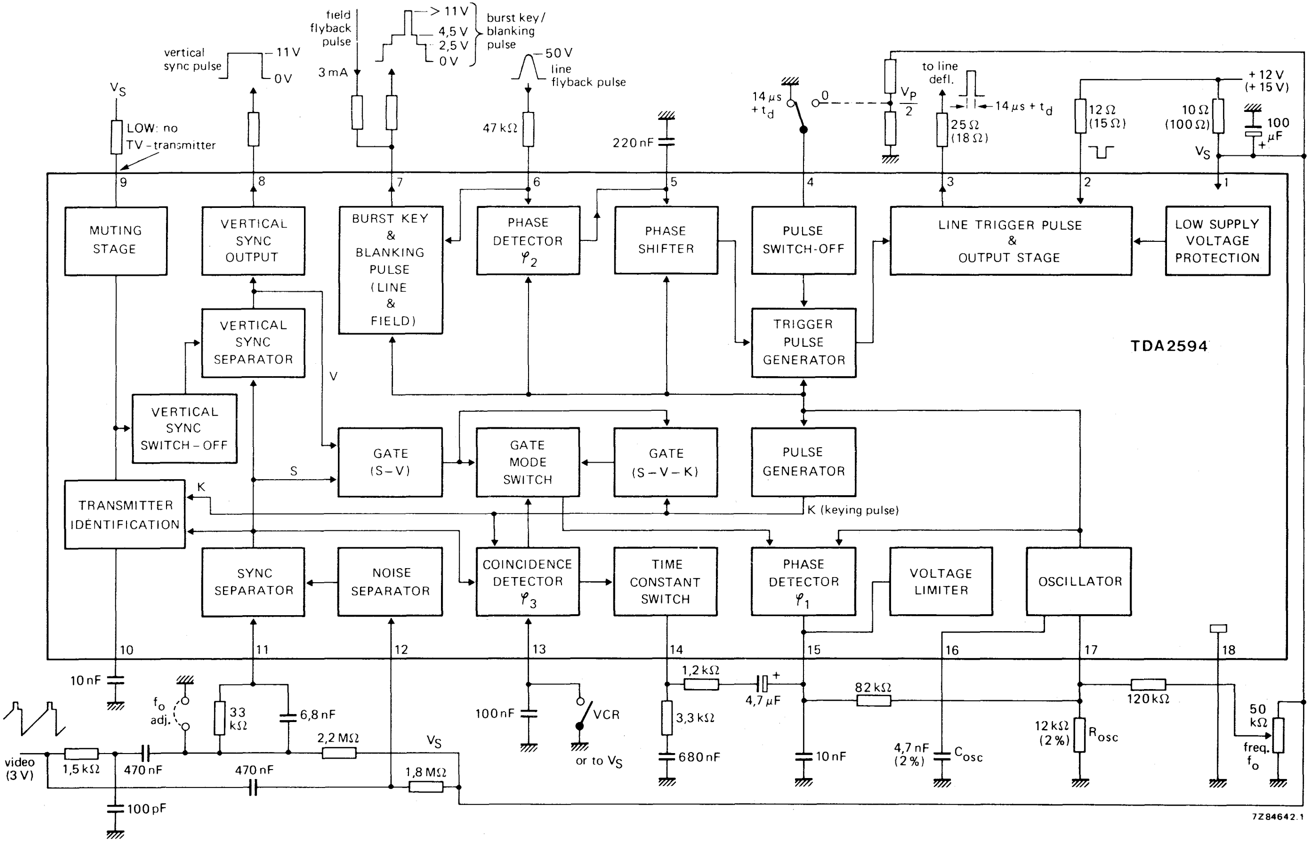


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage				
at pin 1 (voltage source)	$V_{1\text{-}18} = V_S$	max.	13,2	V
at pin 2	$V_{2\text{-}18}$	max.	18	V
Voltages				
Pin 4	$V_{4\text{-}18}$	max.	13,2	V
Pin 9	$V_{9\text{-}18}$ $-V_{9\text{-}18}$	max. max.	18 0,5	V V
Pin 11	$\pm V_{11\text{-}18}$	max.	6	V
Pin 12	$\pm V_{12\text{-}18}$	max.	6	V
Pin 13	$V_{13\text{-}18}$	max.	13,2	V
Currents				
Pins 2 and 3 (transistor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	400	mA
Pin 4	I_4	max.	1	mA
Pin 6	$\pm I_6$	max.	10	mA
Pin 7	$-I_7$	max.	5	mA
Pin 9	I_9	max.	10	mA
Pin 13	I_{13}	max.	2	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−25 to	+125	°C
Operating ambient temperature range	T_{amb}	−20 to	+70	°C

CHARACTERISTICS at $V_{1\text{-}18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

Sync separator (pin 11)

Input switching voltage	$V_{11\text{-}18}$	typ.	0,8	V
Input keying current	I_{11}		5 to 100	μA
Input leakage current at $V_{11\text{-}18} = -5$ V	I_{11}	⩽	1	μA
Input switching current	I_{11}	⩽	5	μA
Switch off current	I_{11}	⩾ typ.	100 150	μA μA
Input signal (peak-to-peak value)	$V_{11\text{-}18(p\text{-}p)}$		3 to 4	V*

---

* Permissible range 1 to 7 V.

Noise separator (pin 12)

Input switching voltage	$V_{12\text{-}18}$	typ.	1,4	V
Input keying current	I_{12}		5 to 100	μA
Input switching current	I_{12}	⩾ typ.	100 150	μA μA
Input leakage current at $V_{12\text{-}18} = -5$ V	I_{12}	⩽	1	μA
Input signal (peak-to-peak value)	$V_{12\text{-}18(p\text{-}p)}$		3 to 4	V*
Permissible superimposed noise signal (peak-to-peak value)	$V_{12\text{-}18(p\text{-}p)}$	⩽	7	V

Line flyback pulse (pin 6)

Input current	I_6	⩾ typ.	0,02 1	mA mA
Input switching voltage	$V_{6\text{-}18}$	typ.	1,4	V
Input limiting voltage	$V_{6\text{-}18}$		−0,7 to +1,4	V

Switching on VCR (pin 13)

Input voltage	$V_{13\text{-}18}$ or: $V_{13\text{-}18}$		0 to 2,5 9 to V_S	V V
Input current	$-I_{13}$ or: I_{13}	⩽ ⩽	200 2	μA mA

Pulse switching off (pin 4)

For t = 0; input pin 4 open or $V_{3\text{-}18} = 0$

Input voltage	$V_{4\text{-}18}$		5,4 to 6,6	V
Input current	I_4	typ.	0	μA

Vertical sync pulse (positive-going) (pin 8)

Output voltage (peak-to-peak value)	$V_{8\text{-}18(p\text{-}p)}$	⩾ typ.	10 11	V V
Output resistance	R_8	typ.	2	kΩ
Delay between leading edge of input and output signal	t_{on}	typ.	15	μs
Delay between trailing edge of input and output signal	t_{off}	⩾	t_{on}	μs
Switching off the vertical sync pulse	$V_{10\text{-}18}$	⩽	3	V

Burst key pulse (positive-going) (pin 7)

Output voltage	$V_{7\text{-}18}$	⩾ typ.	10 11	V V
Output resistance	R_7	typ.	70	Ω
Pulse duration; $V_{7\text{-}18} = 7$ V	t_p	typ.	4 3,7 to 4,3	μs μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst key pulse; $V_{7\text{-}18} = 7$ V	t	typ.	2,65 2,15 to 3,15	μs μs
Output trailing edge current	I_7	typ.	2	mA
Saturation voltage during line scan	$V_{7\text{-}18}$	⩽	1	V

* Permissible range 1 to 7 V.

Line flyback-blanking pulse (positive-going) (pin 7)

Output voltage	$V_{7\text{-}18}$		4,1 to 4,9	V
Output resistance	R_7	typ.	70	Ω
Output trailing edge current	I_7	typ.	2	mA

Field flyback/blanking pulse (pin 7)

Output voltage with externally forced in current I_7 = 2,4 to 3,6 mA	$V_{7\text{-}18}$		2 to 3	V
Output resistance at I_7 = 3 mA	R_7	typ.	70	Ω

TV-transmitter identification output (pin 9; open collector)

Output voltage at I_9 = 3 mA; no TV-transmitter	$V_{9\text{-}18}$	$\leqslant$	0,5	V
Output resistance at I_9 = 3 mA; no TV-transmitter	R_9	$\leqslant$	100	Ω
Output current at $V_{10\text{-}18} \geqslant 3$ V; TV-transmitter identified	I_9	$\leqslant$	5	μA

TV-transmitter identification (pin 10)

When receiving a TV signal the voltage $V_{10\text{-}18}$ will change from $\leqslant 1$ V to $\geqslant 7$ V.

Line drive pulse (positive-going)

Output voltage (peak-to-peak value)	$V_{3\text{-}18(p\text{-}p)}$	typ.	10	V
Output resistance				
for leading edge of line pulse	R_3	typ.	2,5	Ω
for trailing edge of line pulse	R_3	typ.	20	Ω
Pulse duration (transistor driving) $V_{4\text{-}18}$ = 0 to 3,5 V; $-I_4 \geqslant 200$ μA; t_{fp} = 12 μs	t_p		14 + t_d	μs*
Supply voltage for switching off the output pulse	$V_{1\text{-}18}$	typ.	4	V

Overall phase relation

Phase relation between middle of sync pulse and the middle of the flyback pulse	Δt	typ.	2,6 ± 0,7	μs**

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2.

If additional adjustment is applied it can be arranged by current supply at pin 5, such that:

Supplying current	$\Delta I/\Delta t$	typ.	30	μA/μs

---

* t_d = switch-off delay of line output stage.

** Line flyback pulse duration t_{fp} = 12 μs.

Oscillator (pins 16 and 17)

Threshold voltage low level	$V_{16\text{-}18}$	typ.	4,4	V
Threshold voltage high level	$V_{16\text{-}18}$	typ.	7,6	V
Charging current	$\pm I_{16}$	typ.	0,47	mA
Frequency; free running (C_{osc} = 4,7 nF; R_{osc} = 12 kΩ)	f_o	typ.	15,625	kHz
Spread of frequency	Δf_o	⩽	± 5	%▲
Frequency control sensitivity	$\Delta f_o/\Delta_{17}$	typ.	31	Hz/μA
Adjustment range of network in circuit (Fig. 1)	Δf_o	typ.	± 10	%
Influence of supply voltage on frequency; reference at V_S = 12 V	$\dfrac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	⩽	± 0,05	%▲
Change of frequency when V_S drops to 5 V; reference at V_S = 12 V	Δf_o	⩽	± 10	%▲
Temperature coefficient of oscillator frequency	TC	⩽	$\pm 10^{-4}$	K^{-1}▲

Phase comparison φ_1 (pin 15)

Control voltage range	$V_{15\text{-}18}$		4,1 to 7,9	V
Control current (peak value)	$\pm I_{15M}$		1,8 to 2,2	mA
Output leakage current at $V_{15\text{-}18}$ = 4,3 to 7,7 V	I_{15}	⩽	1	μA
Output resistance				
at $V_{15\text{-}18}$ = 4,3 to 7,7 V	R_{13}	high ohmic		*
at $V_{15\text{-}18}$ ⩽ 4,1 V or ⩾ 7,9 V	R_{13}	low ohmic		**
Control sensitivity		typ.	2	kHz/μs
Catching and holding range (82 kΩ between pins 15 and 17)	Δf	typ.	± 680	Hz
Spread of catching and holding range	Δ(Δf)	typ.	± 12	%▲

Phase comparison φ_2 **and phase shifter** (pin 5)

Control voltage range	$V_{5\text{-}18}$		5,4 to 7,6	V
Control current (peak value)	$\pm I_{5M}$	typ.	1	mA
Output resistance at $V_{5\text{-}18}$ = 5,4 to 7,6 V	R_5	high ohmic		*
Input leakage current at $V_{5\text{-}18}$ = 5,4 to 7,6 V	I_5	⩽	5	μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t_{fp} = 12 μs)	t_d	⩽	15,5	μs
Static control error	$\Delta t/\Delta t_d$	⩽	0,2	%

Coincidence detector φ_3 (pin 13)

Output voltage	$V_{13\text{-}18}$		0,5 to 6	V
Output current (peak value)				
without coincidence	I_{13M}	typ.	0,1	mA
with coincidence	$-I_{13M}$	typ.	0,5	mA

* Current source.

** Emitter follower.

▲ Excluding external component tolerances.

Time constant switch (pin 14)

Output voltage	$V_{14\text{-}18}$	typ.	6 V
Output current (limited)	$\pm I_{14}$	typ.	1 mA
Output resistance			
at $V_{13\text{-}18} = 3{,}5$ to 7 V	R_{14}	typ.	0,1 kΩ
at $V_{13\text{-}18} \leqslant 2{,}5$ V or $\geqslant 9$ V	R_{14}	typ.	60 kΩ

Internal keying pulse

Pulse duration	t_p	typ.	7,5 μs

HORIZONTAL COMBINATION

GENERAL DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in colour television receivers. The circuit incorporates the following functions:

- Positive video input; capacitively coupled (source impedance $< 200\ \Omega$)
- Adaptive sync separator; slicing level at 50% of sync amplitude
- Internal vertical pulse separator with double slope integrator
- Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting
- φ_1 phase control between horizontal sync and oscillator
- Coincidence detector φ_3 for automatic time-constant switching; overruled by the VCR switch
- Time-constant switch between two external time-constants or loop-gain; both controlled by the coincidence detector φ_3
- φ_1 gating pulse controlled by coincidence detector φ_3
- Mute circuit depending on TV transmitter identification
- φ_2 phase control between line flyback and oscillator; the slicing levels for φ_2 control and horizontal blanking can be set separately
- Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)
- Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor
- Detector for too low supply voltage
- Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4 V or higher than 8 V
- Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse
- Spot-suppressor controlled by the line flyback control

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_{15\text{-}5} = V_P$	typ.	12	V
Sync pulse amplitude (positive video)	$V_{i(p\text{-}p)}$	min.	50	mV
Horizontal output current	I_4	max.	30	mA

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

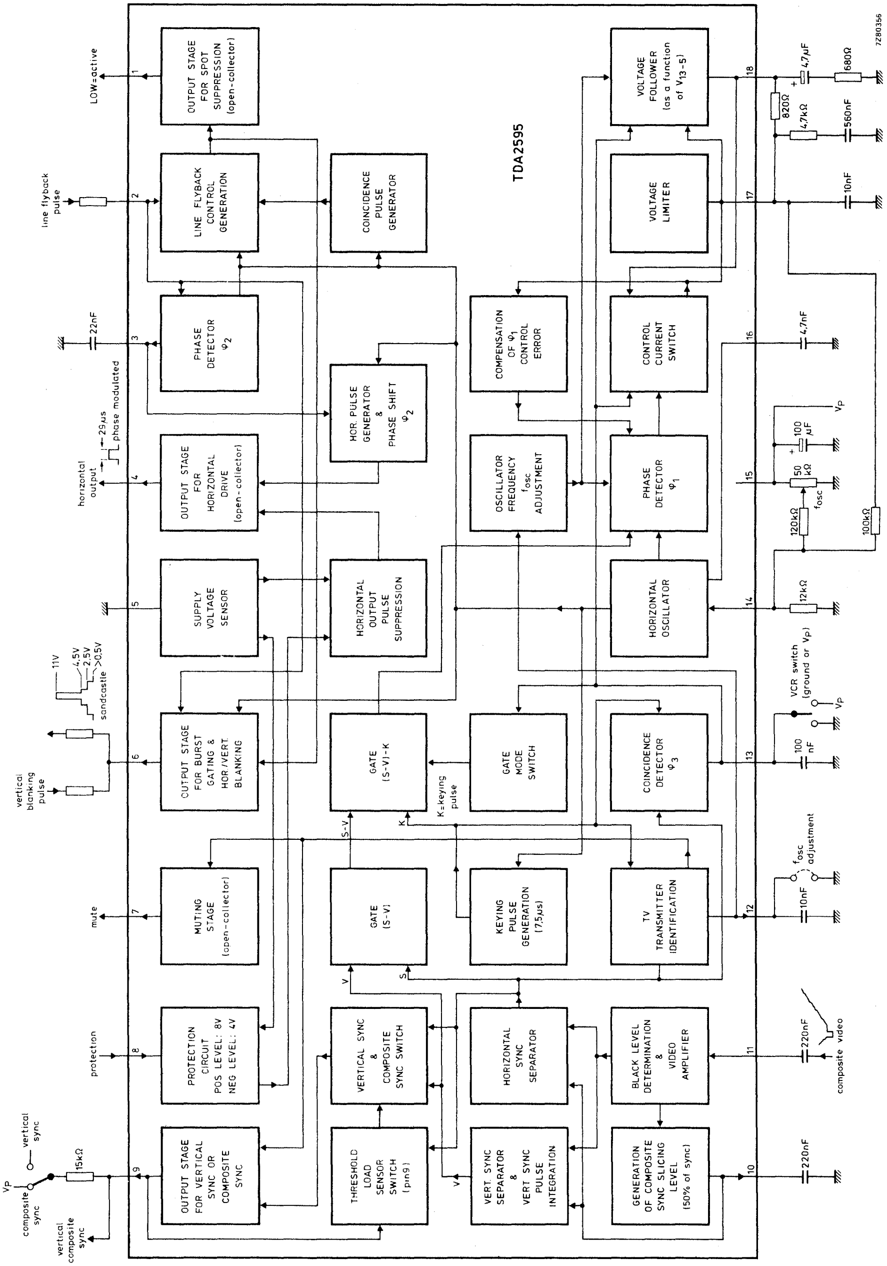


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_{15\text{-}5} = V_P$	max.	13,2	V
Voltages at:				
pins 1, 4 and 7	$V_{1;4;7\text{-}5}$	max.	18	V
pins 8, 13 and 18	$V_{8;13;18\text{-}5}$	max.	V_P	V
pin 11 (range)	$V_{11\text{-}5}$		−0,5 to + 6	V
Currents at:				
pin 1	I_1	max.	10	mA
pin 2 (peak value)	$\pm I_{2M}$	max.	10	mA
pin 4	I_4	max.	100	mA
pin 6 (peak value)	$\pm I_{6M}$	max.	6	mA
pin 7	I_7	max.	10	mA
pin 8 (range)	I_8		−5 to + 1	mA
pin 9 (range)	I_9		−10 to + 3	mA
pin 18	$\pm I_{18}$	max.	10	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−25 to + 125	°C
Operating ambient temperature range	T_{amb}		−20 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Composite video input and sync separator (pin 11) (internal black level determination)					
Input signal (positive video; standard signal; peak-to-peak value)	$V_{11\text{-}5(p\text{-}p)}$	0,2	1	3	V
Sync pulse amplitude (independent of video content)	$V_{11\text{-}5(p\text{-}p)}$	50	–	–	mV
Generator resistance	R_G	–	–	200	Ω
Input current during:					
video	I_{11}	–	5	–	μA
sync pulse	$-I_{11}$	–	40	–	μA
black level	$-I_{11}$	–	30	–	μA
Composite sync generation (pin 10) horizontal slicing level at 50% of the sync pulse amplitude					
Capacitor current during:					
video	I_{10}	–	12	–	μA
sync pulse	$-I_{10}$	–	170	–	μA
Vertical sync pulse generation slicing level at 25% (50% between black level and horizontal slicing level); pin 9					
Output voltage	$V_{9\text{-}5}$	10	–	–	V
Pulse duration	t_p	–	190	–	μs
Delay with respect to the vertical sync pulse (leading edge)	t_d	–	45	–	μs
Pulse-mode control					
output current for vertical sync pulse (dual integrated)		no current applied at pin 9			
output current for horizontal and vertical sync pulse (non-integrated separated signal)		current applied via a resistor of 15 kΩ from V_P to pin 9			

parameter	symbol	min.	typ.	max.	unit
Horizontal oscillator (pins 14 and 16)					
Frequency; free running	f_{osc}	–	15 625	–	Hz
Reference voltage for f_{osc}	$V_{14\text{-}5}$	–	6	–	V
Frequency control sensitivity	$\Delta f_{osc}/\Delta I_{14}$	–	31	–	Hz/μA
Adjustment range of circuit Fig. 1	Δf_{osc}	–	± 10	–	%
Spread of frequency	Δf_{osc}	–	–	5	%
Frequency dependency (excluding tolerance of external components)					
with supply voltage (V_P = 12 V)	$\frac{\Delta f_{osc}/f_{osc}}{\Delta V_{15\text{-}5}/V_{15\text{-}5}}$	–	± 0,05	–	
with supply voltage drop of 5 V	Δf_{osc}	–	–	10	%
with temperature	TC	–	–	$\pm 10^{-4}$	K^{-1}
Capacitor current during:					
charging	$-I_{16}$	–	1024	–	μA
discharging	I_{16}	–	313	–	μA
Sawtooth voltage timing (pin 14)					
rise time	t_r	–	49	–	μs
fall time	t_f	–	15	–	μs
Horizontal output pulse (pin 4)					
Output voltage LOW at I_4 = 30 mA	$V_{4\text{-}5}$	–	–	0,5	V
Pulse duration (HIGH)	t_p	–	29 ± 1,5	–	μs
Supply voltage for switching off the output pulse (pin 15)	V_P	–	4	–	V

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_1 (pin 17)					
Control voltage range	$V_{17\text{-}5}$	3,55	–	8,3	V
Leakage current at $V_{17\text{-}5}$ = 3,55 to 8,3 V	I_{17}	–	–	1	μA
Control current for external time-constant switch	$\pm I_{17}$	1,8	2	2,2	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5} < 2$ V or $V_{13\text{-}5} > 9{,}5$ V	$\pm I_{17}$	–	8	–	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5}$ = 2 to 9,5 V	$\pm I_{17}$	1,8	2	2,2	mA
Horizontal oscillator control					
control sensitivity	S_φ	6	–	–	kHz/μs
catching and holding range	Δf_{osc}	–	± 680	–	Hz
spread of catching and holding range	Δf_{osc}	–	± 10	–	%
Internal keying pulse at $V_{13\text{-}5}$ = 2,9 to 9,5 V	t_p	–	7,5	–	μs
Time-constant switch					
slow time-constant at	$V_{13\text{-}5}$	9,5	–	2	V
fast time-constant at	$V_{13\text{-}5}$	2	–	9,5	V
Impedance converter offset voltage (slow time-constant)	$\pm V_{17\text{-}18}$	–	–	3	mV
Output resistance					
slow time-constant	$R_{18\text{-}5}$	–	–	10	Ω
fast time-constant	$R_{18\text{-}5}$	high impedance			
Leakage current	I_{18}	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Coincidence detector φ_3 (pin 13)					
Output voltage					
without coincidence with composite video signal	$V_{13\text{-}5}$	–	–	1	V
without coincidence without composite video signal (noise)	$V_{13\text{-}5}$	–	–	2	V
with coincidence with composite video signal	$V_{13\text{-}5}$	–	6	–	V
Output current					
without coincidence with composite video signal	I_{13}	–	50	–	μA
with coincidence with composite video signal	$-I_{13}$	–	300	–	μA
Switching current					
at $V_{13\text{-}5} = V_P - 0{,}5$ V	I_{13}	–	–	100	μA
at $V_{13\text{-}5} = 0{,}5$ V (average value)	$I_{13(av)}$	–	–	100	μA
Phase comparison φ_2 (pins 2 and 3) (see note 1)					
Input for line flyback pulse (pin 2)					
Switching level for φ_2 comparison	$V_{2\text{-}5}$	–	3	–	V
Switching level for horizontal blanking and flyback control	$V_{2\text{-}5}$	–	3	–	V
Input voltage limiting	$V_{2\text{-}5}$	–	–0,7	–	V
	or:	–	+4,5	–	V
Switching current					
at horizontal flyback	I_2	0,01	1	–	mA
at horizontal scan	I_2	–	–	2	μA
Phase detector output (pin 3)					
Control current for φ_2	$\pm I_3$	–	1	–	mA
Control range	$\Delta t_{\varphi 2}$	–	19	–	μs
Static control error	$\Delta t/\Delta t_d$	–	–	0,2	%
Leakage current	I_3	–	–	5	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_2 (pins 2 and 3) (continued)					
Phase relation between middle of the horizontal sync pulse and the middle of the line flyback pulse at t_{fp} = 12 µs (note 2)	Δt	–	2,6 ± 0,7	–	µs
If additional adjustment is required, it can be arranged by applying a current at pin 3, such that for applied current:	$\Delta I/\Delta t$	–	30	–	µA/µs
Burst gating pulse (pin 6; note 3)					
Output voltage	$V_{6\text{-}5}$	10	11	–	V
Pulse duration	t_p	3,7	4	4,3	µs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse at $V_{6\text{-}5}$ = 7 V	$t_{\varphi 6}$	2,15	2,65	3,15	µs
Output trailing edge current	I_6	–	2	–	mA
Horizontal blanking pulse (pin 6) (note 3)					
Output voltage	$V_{6\text{-}5}$	4,2	4,5	4,9	V
Output trailing edge current	I_6	–	2	–	mA
Saturation voltage at horizontal scan	$V_{6\text{-}5sat}$	–	–	0,5	V
Clamping circuit for vertical blanking pulse (pin 6; note 3)					
Output voltage at I_6 = 2,8 mA	$V_{6\text{-}5}$	2,15	2,5	3	V
Minimum output current at $V_{6\text{-}5} > 2{,}15$ V	I_{6min}	–	2,3	–	mA
Maximum output current at $V_{6\text{-}5} < 3$ V	I_{6max}	–	3,3	–	mA
TV-transmitter identification (pin 12)					
Output voltage					
no TV transmitter	$V_{12\text{-}5}$	–	–	1	V
TV transmitter identified	$V_{12\text{-}5}$	7	–	–	V

parameter	symbol	min.	typ.	max.	unit
Mute output (pin 7)					
Output voltage at I_7 = 3 mA no TV transmitter	$V_{7\text{-}5}$	–	–	0,5	V
Output resistance at I_7 = 3 mA no TV transmitter	$R_{7\text{-}5}$	–	–	100	Ω
Output leakage current at $V_{12\text{-}5} > 3$ V TV transmitter identified	I_7	–	–	5	μA
Protection circuit (beam-current/ EHT voltage protection) (pin 8)					
No-load voltage for $I_8 = 0$ (operative condition)	$V_{8\text{-}5}$	–	6	–	V
Threshold at positive-going voltage	$V_{8\text{-}5}$	–	8 ± 0,8	–	V
Threshold at negative-going voltage	$V_{8\text{-}5}$	–	4 ± 0,4	–	V
Current limiting for $V_{8\text{-}5}$ = 1 to 8,5 V	$\pm I_8$	–	60	–	μA
Input resistance for $V_{8\text{-}5} > 8{,}5$ V	$R_{8\text{-}5}$	–	3	–	kΩ
Response delay of threshold switch	t_d	–	10	–	μs
Control output of line flyback pulse control (pin 1)					
Saturation voltage at standard operation; I_1 = 3 mA	$V_{1\text{-}5sat}$	–	–	0,5	V
Output leakage current in case of break in transmission	I_1	–	–	5	μA

Notes to the characteristics

1. Phase comparison between horizontal oscillator and the line flyback pulse. Generation of a phase modulated (φ_2) horizontal output pulse with constant duration.
2. t_{fp} is the line flyback pulse duration.
3. Three-level sandcastle pulse.

DEVELOPMENT SAMPLE DATA

5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 35	V
Repetitive peak output current	I_{ORM}	<	1,5	A
Output power at d_{tot} = 10%				
V_P = 18 V; R_L = 8 Ω	P_o	typ.	4,5	W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5	W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ.	0,3	%
Input impedance	$\|Z_i\|$	typ.	45	kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25	mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ.	55	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

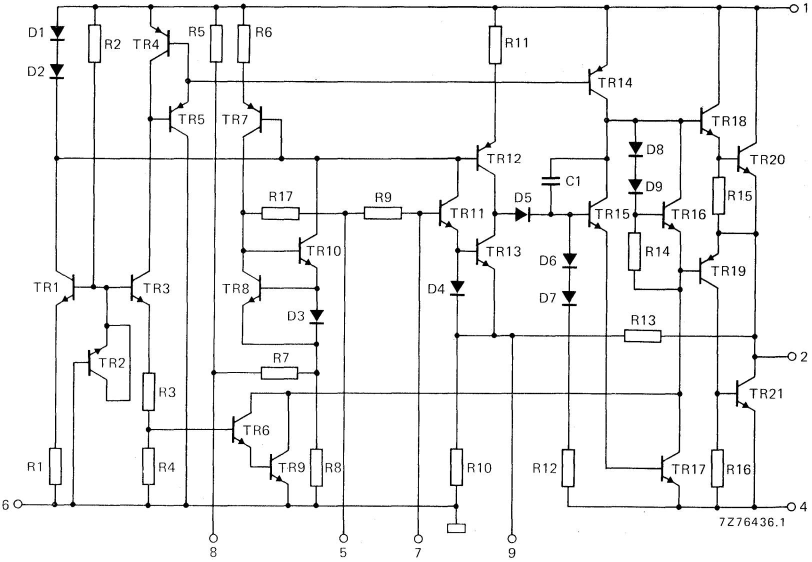


Fig. 1 Circuit diagram; pin 3 not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C

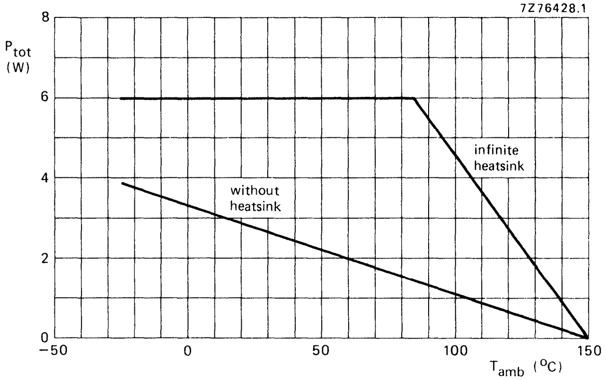


Fig. 2 Power derating curves.

HEATSINK EXAMPLE

Assume $V_P = 18$ V; $R_L = 8\ \Omega$; $T_{amb} = 60$ °C maximum; $T_j = 150$ °C (max. for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,2 W).

The thermal resistance from junction to ambient can be expressed as:

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150 - 60}{2,2} = 41 \text{ K/W}.$$

Since $R_{th\,j\text{-}tab} = 11$ K/W and $R_{th\,tab\text{-}h} = 1$ K/W, $R_{th\,h\text{-}a} = 41 - (11 + 1) = 29$ K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 35	V
Repetitive peak output current	I_{ORM}	<	1,5	A
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 18 V; R_L = 8 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3

A.F. output power at d_{tot} = 10%				
V_P = 18 V; R_L = 8 Ω	P_o	>	4	W
		typ.	4,5	W
V_P = 12 V; R_L = 8 Ω	P_o	typ.	1,7	W
V_P = 8,3 V; R_L = 8 Ω	P_o	typ.	0,65	W
V_P = 20 V; R_L = 8 Ω	P_o	typ.	6	W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5	W
Total harmonic distortion at P_o = 2 W	d_{tot}	typ.	0,3	%
		<	1	%
Frequency response		>	15	kHz
Input impedance	$\lvert Z_i \rvert$	typ.	45	kΩ *
Noise output voltage at R_S = 5 kΩ; B = 60 Hz to 15 kHz	V_n	typ.	0,2	mV
		<	0,5	mV
Sensitivity for P_o = 2,5 W	V_i	typ.	55	mV
			44 to 66	mV

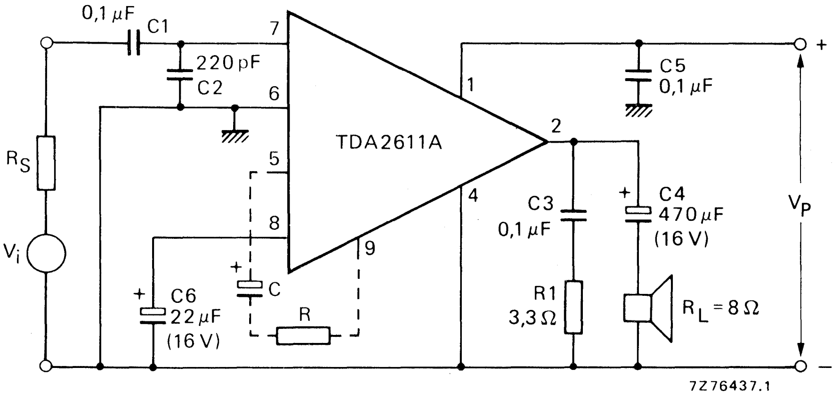


Fig. 3 Test circuit; pin 3 not connected.

---

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

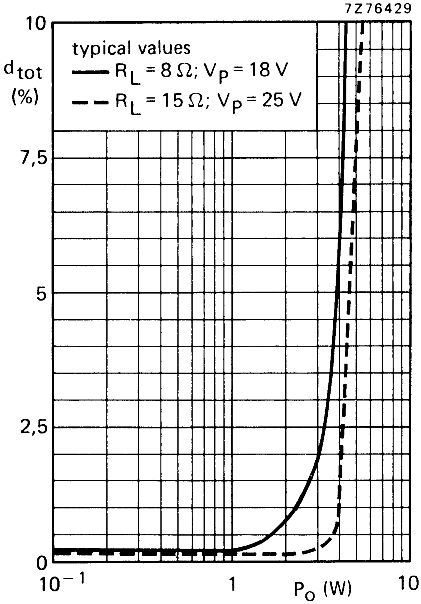


Fig. 4 Total harmonic distortion as a function of output power.

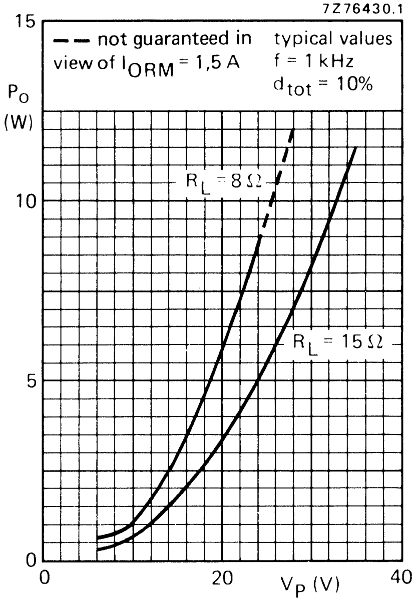


Fig. 5 Output power as a function of supply voltage.

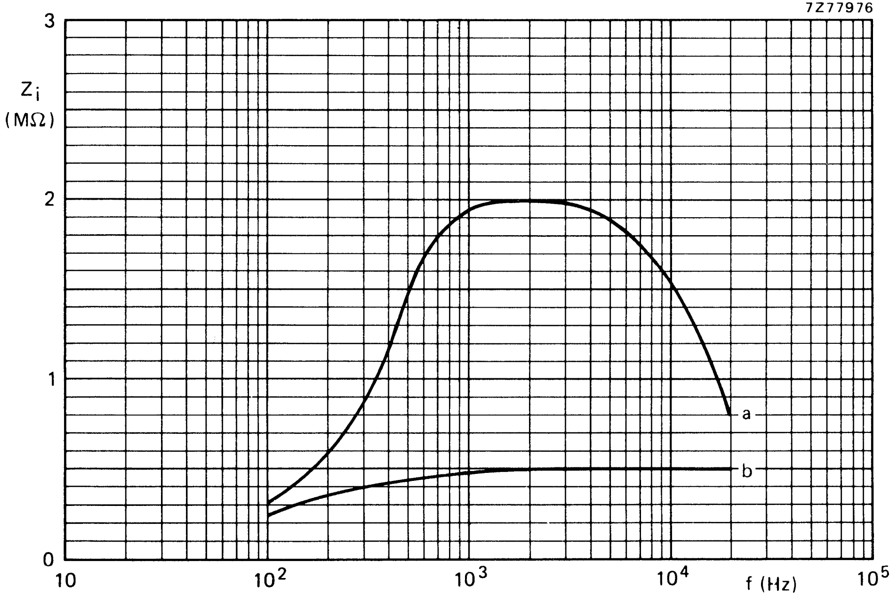


Fig. 6 Input impedance as a function of frequency; curve a for C = 1 μF, R = 0 Ω; curve b for C = 1 μF, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

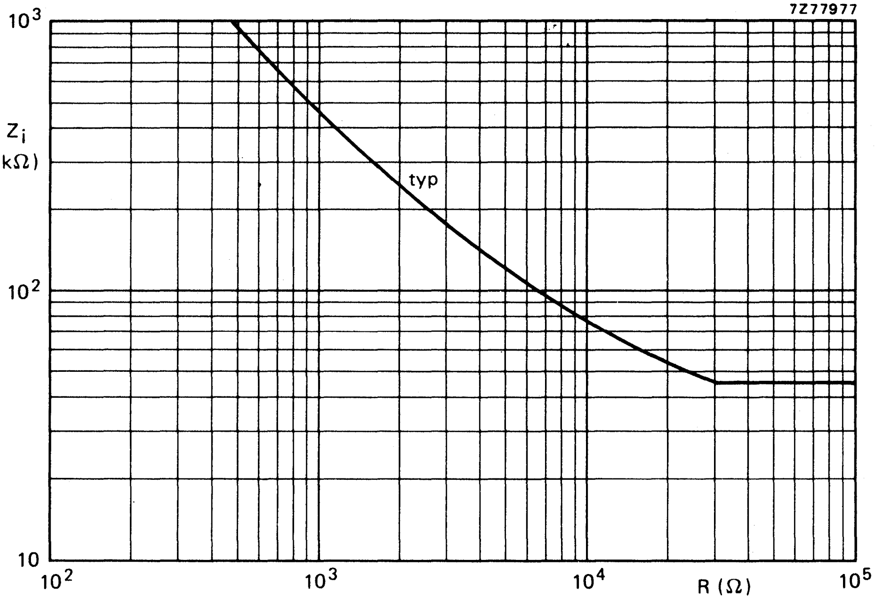


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

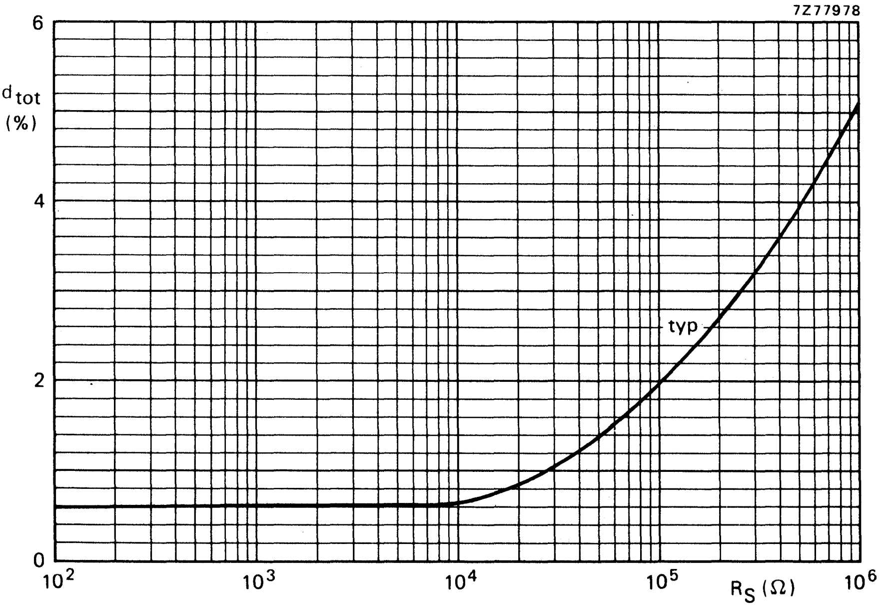


Fig. 8 Total harmonic distortion as a function of R_S in the circuit of Fig. 3; P_o = 3,5 W; f = 1 kHz.

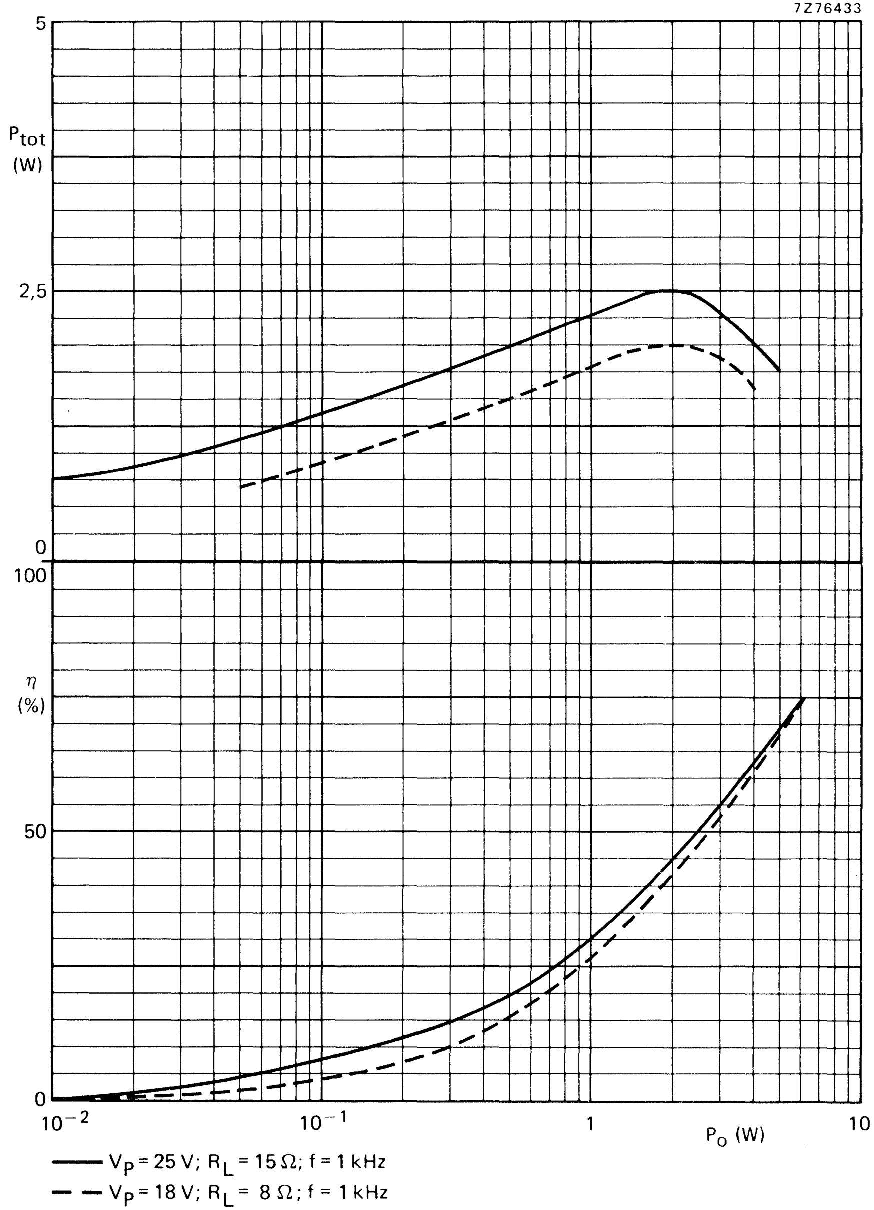


Fig. 9 Total power dissipation and efficiency as a function of output power.

APPLICATION INFORMATION

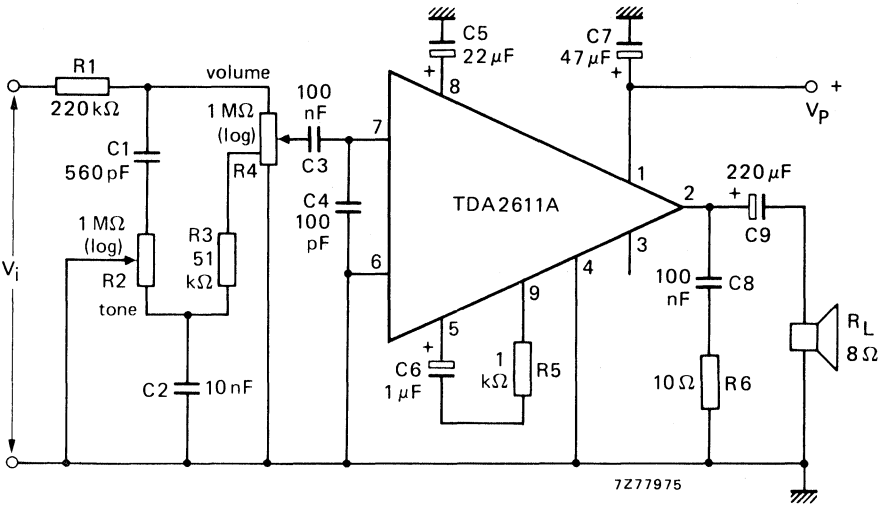


Fig. 10 Ceramic pickup amplifier circuit.

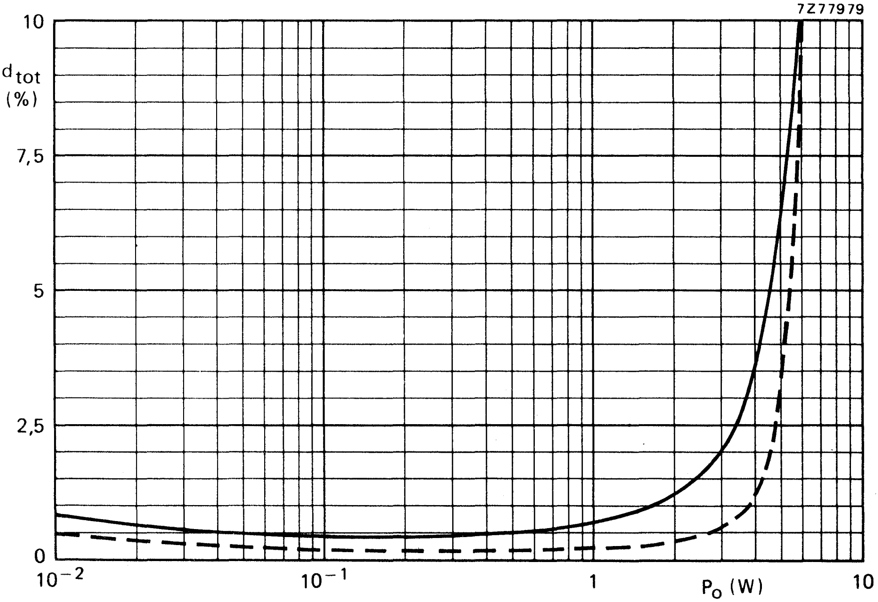


Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

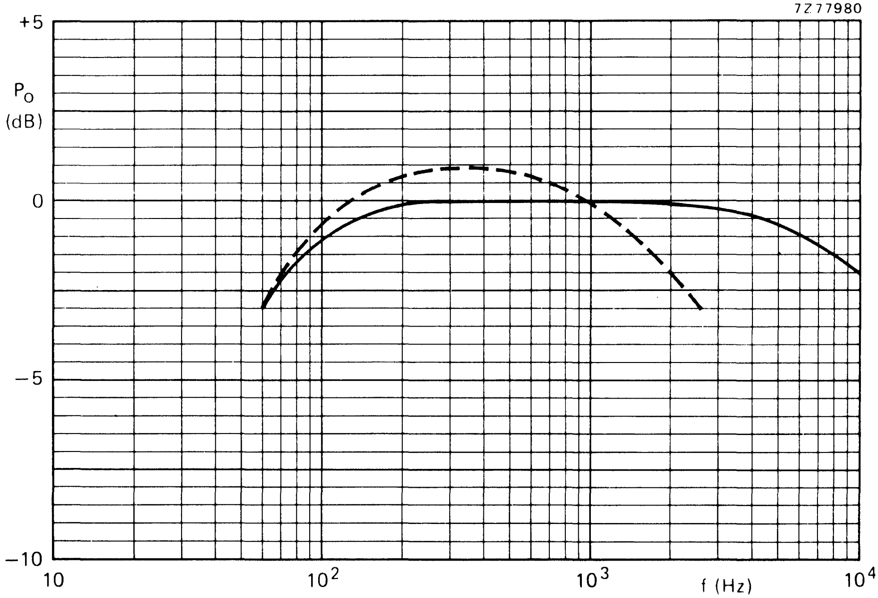


Fig. 12 Frequency characteristics of the circuit of Fig. 10; —— tone control max. high; – – – tone control min. high; P_o relative to 0 dB = 3 W; typical values.

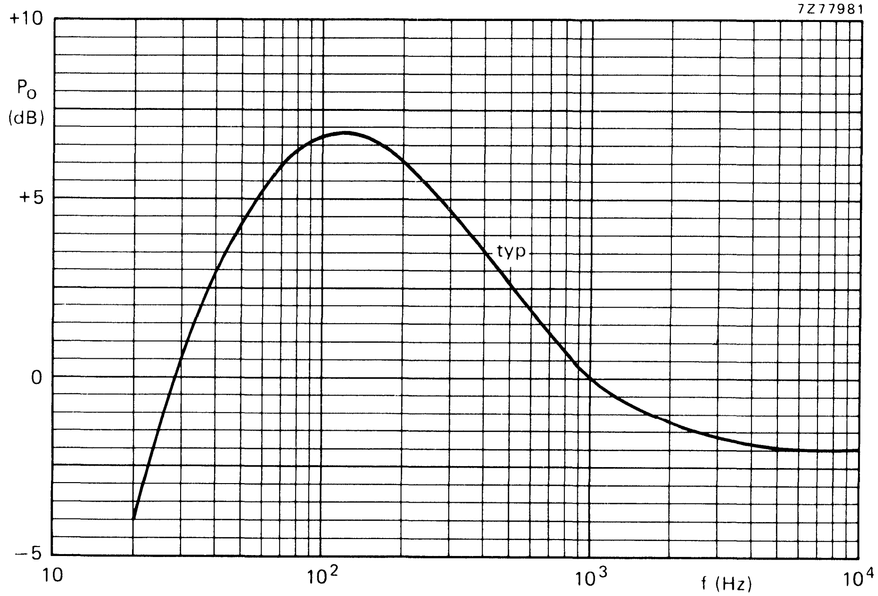


Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.

VERTICAL DEFLECTION CIRCUIT

The TDA2653A is a monolithic integrated circuit for vertical deflection in large screen colour television receivers, e.g. 30AX and PIL-S4 systems.

The circuit incorporates the following functions:

- Oscillator; switch capability for 50 Hz/60 Hz operation.
- Synchronization circuit.
- Blanking pulse generator with guard circuit.
- Sawtooth generator with buffer stage.
- Preamplifier with fed-out inputs.
- Output stage with thermal and short-circuit protection.
- Flyback generator.
- Voltage stabilizer.

QUICK REFERENCE DATA

For 30AX system				
Supply voltage (pin 9)	$V_{9\text{-}8} = V_S$	typ.	26	V
Supply current (pin 5 + pin 9)	$I_5 + I_9 = I_S$	typ.	325	mA
Output current (peak-to-peak value)	$I_{6(p\text{-}p)}$	typ.	2,2	A
Picture frequency	f		50 Hz/60	Hz
Sync input pulse (peak-to-peak value)	$V_{2\text{-}8(p\text{-}p)}$	$\geqslant$	1	V
Thermal resistance from junction to mounting base	$R_{th\ j\text{-}mb}$	$\leqslant$	5	K/W

PACKAGE OUTLINE

13-lead DIL; plastic power (SOT-141B).

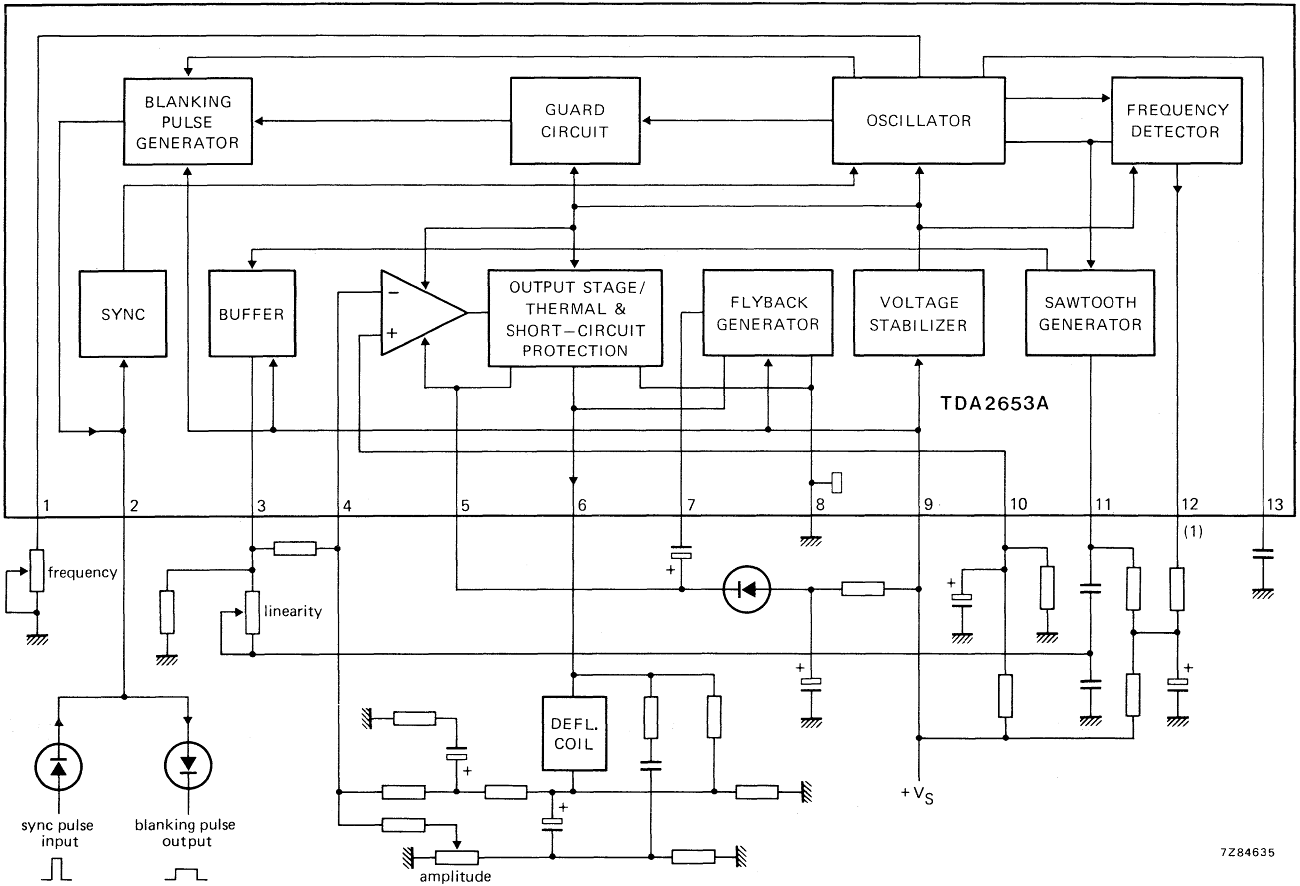


Fig. 1 Block diagram.

(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_{9-8} = V_S$	max.	40 V
Supply voltage output stage (pin 5)	V_{5-8}	max.	58 V
Voltages			
Pin 3	V_{3-11}	max.	7 V
Pin 13	V_{13-8}	max.	7 V
Pins 4 and 10	$V_{4;\,10-8}$	max.	24 V
Pin 6	V_{6-8}	max.	58 V
	$-V_{6-8}$	max.	0 V
Pins 7 and 11	$V_{7;\,11-8}$	max.	40 V
Currents			
Pin 1	I_1	max.	0 mA
	$-I_1$	max.	1 mA
Pin 2	$\pm I_2$	max.	10 mA
Pin 3	I_3	max.	0 mA
	$-I_3$	max.	5 mA
Pin 7	I_7	max.	1,2 A
	$-I_7$	max.	1,5 A
Pin 11	I_{11}	max.	50 mA
	$-I_{11}$	max.	1 mA
Pin 12	I_{12}	max.	3 mA
	$-I_{12}$	max.	0 mA

Pins 5, 6 and 8: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit.

Storage temperature range	T_{stg}	−25 to + 150 °C
Operating ambient temperature range	T_{amb}	−20 °C to limiting value

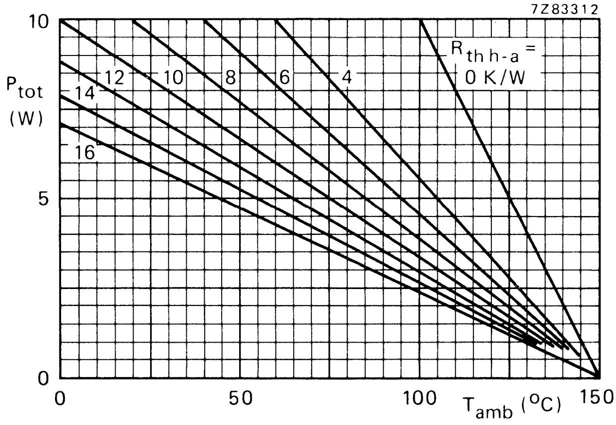


Fig. 2 Total power dissipation. $R_{th\,h-a}$ includes $R_{th\,mb-h}$ which is expected when heat-sink compound is used. $R_{th\,j-mb} \leqslant 5$ K/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

Supply voltage/output stage				
Supply voltage	$V_{9\text{-}8} = V_S$		9 to 30	V
Output voltage at $-I_6$ = 1,1 A	$V_{6\text{-}8}$	⩾ typ.	$V_{5\text{-}8} - 2{,}2$ $V_{5\text{-}8} - 1{,}9$	V V
at I_6 = 1,1 A	$V_{6\text{-}8}$	typ. ⩽	1,3 1,6	V V
Flyback generator output voltage at $-I_6$ = 1,1 A	$V_{7\text{-}8}$	typ.	$V_S - 2{,}2$	V
Peak output current	$\pm I_6$	⩽	1,2	A
Flyback generator peak current	$\pm I_7$	⩽	1,2	A
Feedback				
Input quiescent current	$-I_{4;\,10}$	typ.	0,1	μA
Synchronization				
Sync input pulse	$V_{2\text{-}8}$		1 to 12	V
Tracking range		typ.	28	%
Oscillator/sawtooth generator				
Oscillator frequency control input voltage	$V_{1\text{-}8}$		6 to 9	V
Sawtooth generator output voltage	$V_{3\text{-}8}$ $V_{11\text{-}8}$		0 to $V_S - 1$ 0 to $V_S - 2$	V V
Sawtooth generator output current	$-I_3$		0 to 4	mA
	I_{11}	⩾ ⩽	−2 +30	μA mA
Oscillator temperature dependency T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	typ.	10^{-4}	K^{-1}
Oscillator voltage dependency V_S = 10 to 30 V	$(\Delta f/f)/\Delta V_S$	typ.	4×10^{-4}	V^{-1}
Blanking pulse generator				
Output voltage at V_S = 24 V; I_2 = 1 mA	$V_{2\text{-}8}$	typ.	18,5	V
Output current	$-I_2$	⩽	3	mA
Output resistance	$R_{2\text{-}8}$	typ.	410	Ω
Blanking pulse duration at 50 Hz sync	t_b	typ.	1,4 ± 0,07	ms
50 Hz/60 Hz switch capability				
Saturation voltage; LOW voltage level	$V_{12\text{-}8}$	typ.	1	V
Output leakage current	I_{12}	typ.	1	μA

Thermal resistance/junction temperature

From junction to mounting base	$R_{th\ j\text{-}mb}$	$\leqslant$	5 K/W
Junction temperature; switching point thermal protection	T_j	typ.	150 ± 8 °C

PINNING

1. Oscillator adjustment
2. Synchronization input/blanking output
3. Sawtooth generator output
4. Preamplifier input
5. Positive supply of output stage
6. Output
7. Flyback generator output
8. Ground
9. Positive supply (V_S)
10. Reference voltage
11. Sawtooth capacitor
12. 50 Hz/ 60 Hz switching voltage
13. Oscillator capacitor

APPLICATION INFORMATION

The function is described against the corresponding pin number

1, 13. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 13.

2. Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector delivers a switching level at pin 12.
The blanking pulse amplitude is 20 V with a load of 1 mA.

3. Sawtooth generator output

The sawtooth signal is fed via a buffer stage to pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 11 (linearity) and via a resistor to pin 4 (preamplifier).

4. Preamplifier input

The d.c. voltage is proportional to the output voltage (d.c. feedback). The a.c. voltage is proportional to the sum of the buffered sawtooth voltage at pin 3 and the voltage, with opposite polarity, at the feedback resistor (a.c. feedback).

5. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 7 and 5, and a diode between pins 5 and 9 have to be connected for proper operation of the flyback generator.

6. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 5 to complete the flyback generator.

8. Negative supply (ground)

Negative supply of output stage and small signal part.

9. Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

APPLICATION INFORMATION (continued)

10. Reference voltage of preamplifier

    External adjustment and decoupling of reference voltage of the preamplifier.

11. Sawtooth capacitor

    This sawtooth capacitor has been split to realize linearity control.

12. 50 Hz/60 Hz switching level

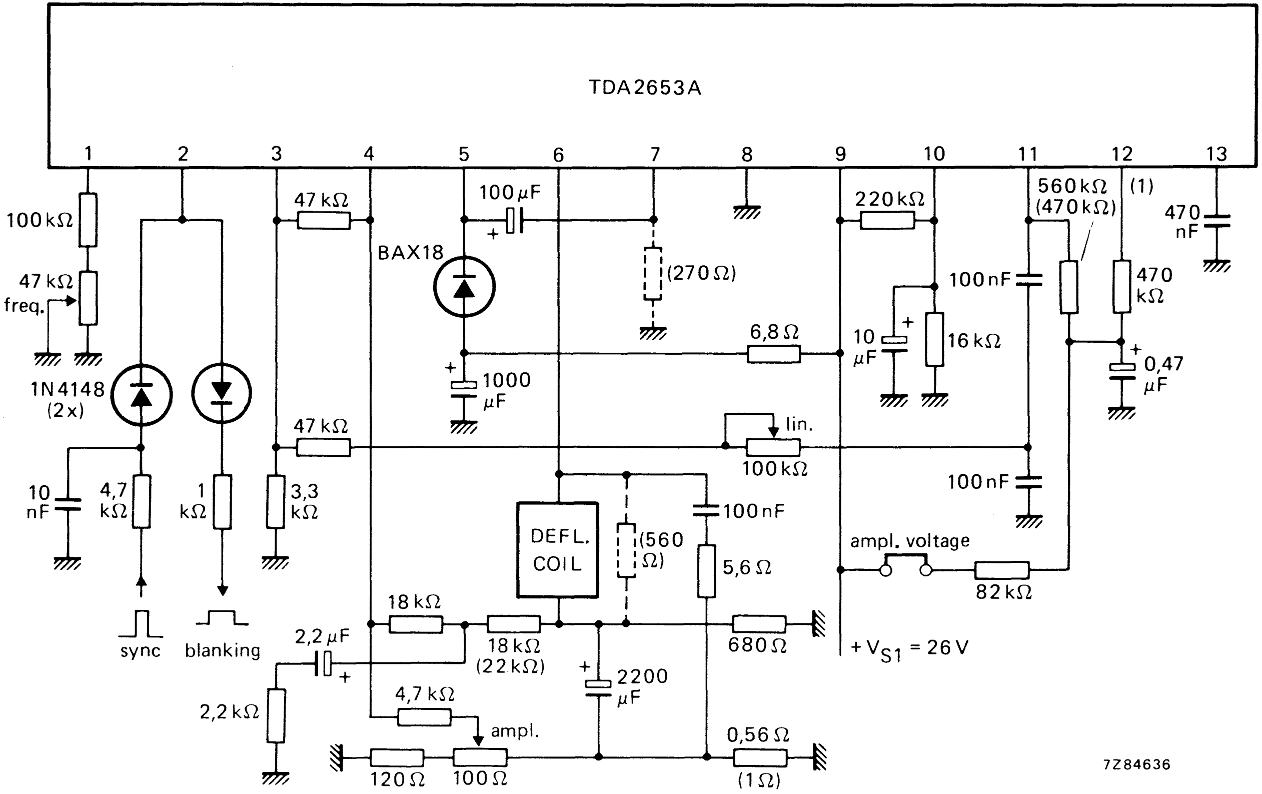
    This pin delivers a LOW voltage level for 50 Hz and a HIGH voltage level for 60 Hz. The amplitudes of the sawtooth signals can be made equal for 50 Hz and 60 Hz with these levels.

The following application data are measured in Figs 3 and 4.

			30AX system (26 V) Fig. 3	30AX system (26 V/12 V) Fig. 4	PIL-S4 system Fig. 3	
System supply voltages	V_{S1}	typ.	26	26	26	V
	V_{S2}	typ.	–	12	–	V
System supply currents	I_{S1}	typ.	315	330	195	mA
	I_{S2}	typ.	–	–35	–	mA
Output voltage	$V_{6\text{-}8}$	typ.	14	14,6	13,5	V
Output voltage (peak value)	$V_{6\text{-}8}$	typ.	42	42	49	V
Deflection current (peak-to-peak value)	$I_{6(p\text{-}p)}$	typ.	2,2	2,2	1,32	A
Flyback time	t_{fl}	typ.	1	0,9	1,1	ms
Total power dissipation per package	P_{tot}	typ.	4,1	4	3	W
		max.	4,8	4,8	3,4	W*
Oscillator frequency unsynchronized	f	typ.	46,5	46,5	46,5	Hz

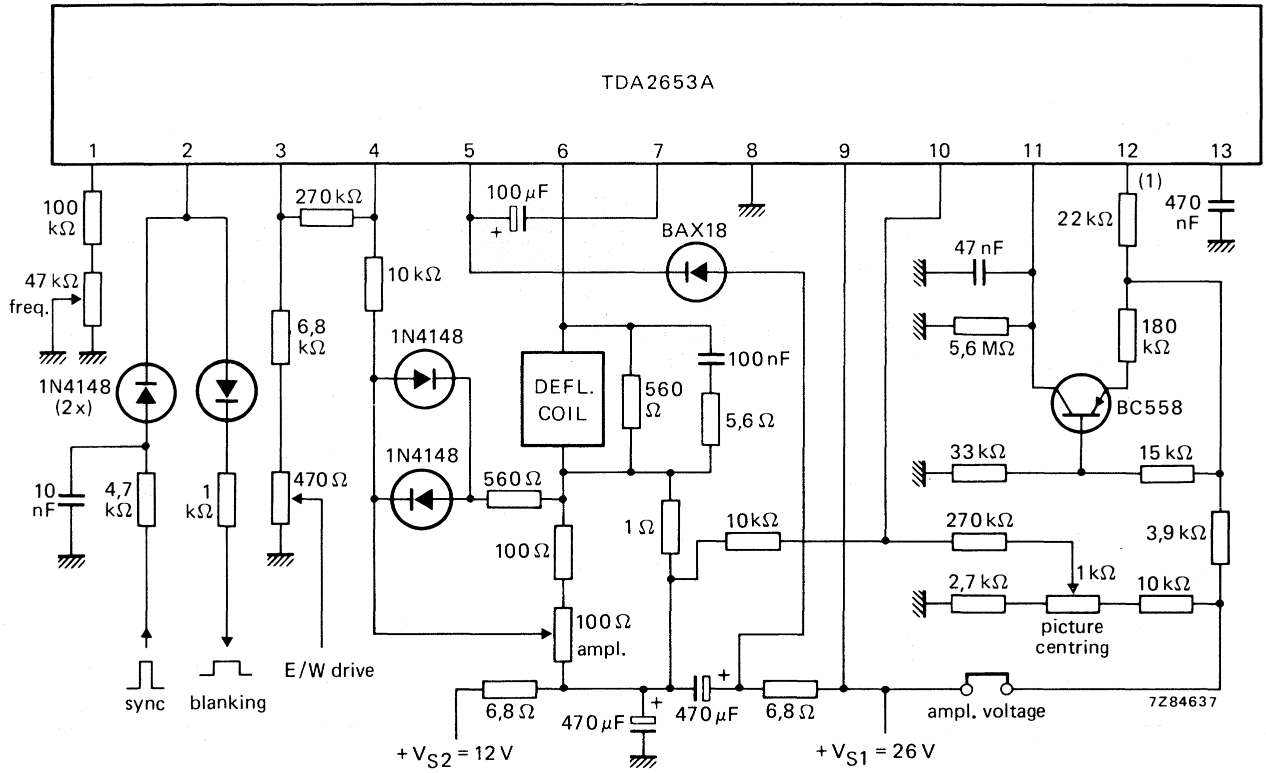
---

* Calculated with $\Delta V_S = +5\%$ and $\Delta R_{yoke} = -7\%$.



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 3 Typical vertical deflection circuit for 30AX system (26 V). The values given in parentheses and the dotted components are valid for the PIL-S4 system.



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 4 Typical vertical deflection circuit for 30AX system (V_{S1} = 26 V, V_{S2} = 12 V) in quasi-bridge connection.

VERTICAL DEFLECTION CIRCUIT

The TDA2654 is a monolithic integrated circuit for vertical deflection in monochrome and tiny-vision colour television receivers.

The circuit incorporates the following functions:

- Oscillator
- Synchronization circuit
- Blanking pulse generator
- Sawtooth generator
- S-correction and linearity circuit
- Comparator and drive circuit
- Output stage
- Flyback dissipation limiting circuit
- Supply for pre-stages via internal voltage divider
- Thermal protection circuit
- Controlled switch-on

QUICK REFERENCE DATA

Supply voltage range (ref. to tab = ground)	V_P		10 to 35	V
Output current (peak-to-peak value)	$I_{9(p-p)}$	max.	2	A
Total power dissipation	P_{tot}	max.	5	W
Operating junction temperature	T_j	max.	150	°C
Thermal resistance from junction to tab	$R_{th\ j\text{-}tab}$	=	12	°C/W

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

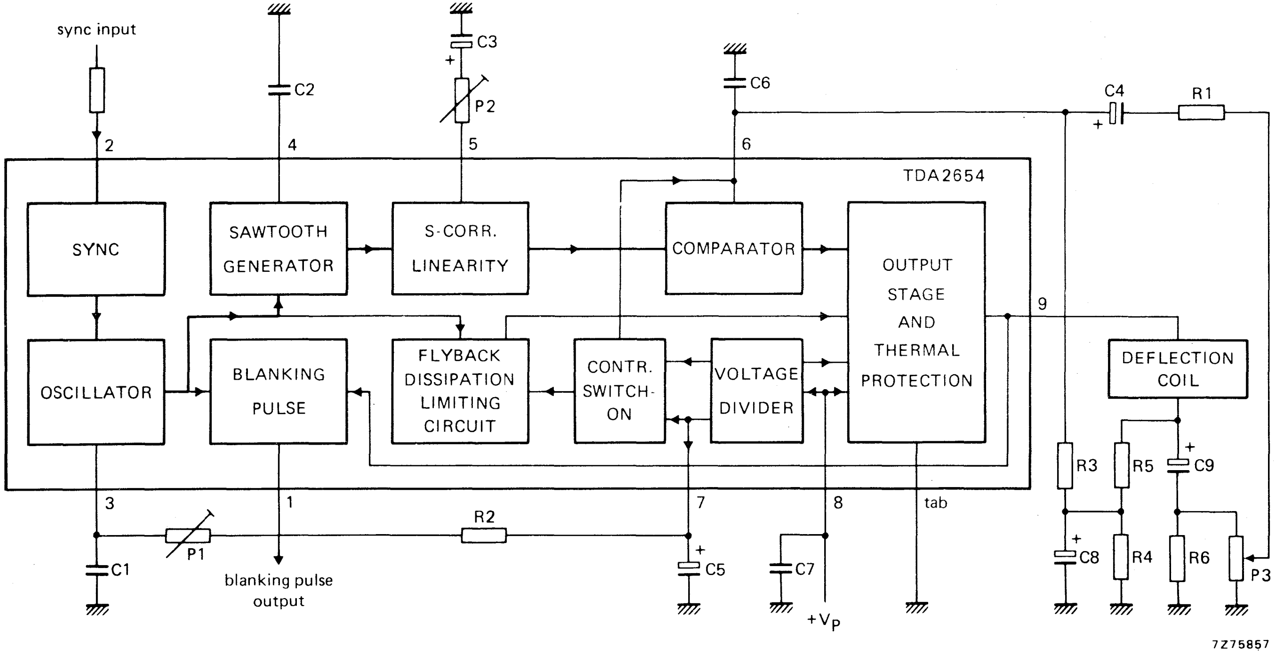


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

All voltages and currents refer to the tab (ground) connection.

Voltages				
Pin 2	V_2	max.	5	V
Pin 3	V_3	max.	17	V
Pin 4	V_4	max.	17	V
Pin 5	V_5	max.	6	V
Pin 6	V_6	max.	13	V
Pin 7	V_7	max.	18	V
Pin 8	V_8 (V_P)	max.	35	V
Currents				
Pin 1	$+I_1$	max.	1	mA
	$-I_1$	max.	5	mA
Pin 2	I_2	max.	2,5	mA
Pin 3	I_3	max.	30	mA
Pin 4	I_4	max.	30	mA
Pin 5	$\pm I_5$	max.	1	mA
Pin 6	$\pm I_6$	max.	3	mA
Pin 9 (repetitive)	$\pm I_9$	max.	1	A
Pin 9 (non-repetitive)	$\pm I_9$	max.	1,5	A
Total power dissipation (see also Fig. 2)	P_{tot}	max.	5	W
Storage temperature	T_{stg}		−25 to + 150	°C
Operating junction temperature	T_j	max.	150	°C

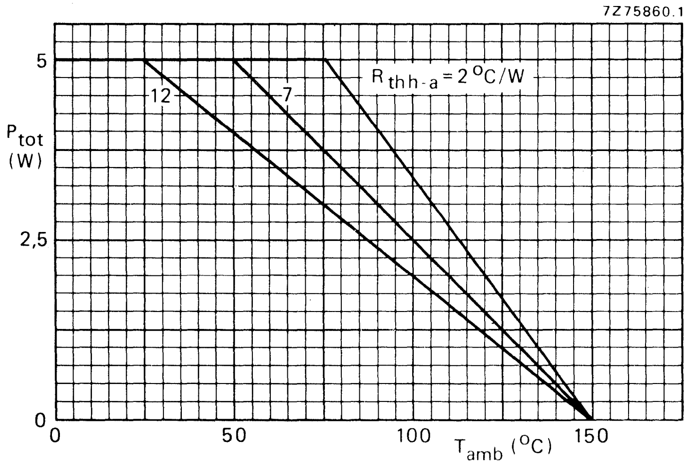


Fig. 2 Total power dissipation. The graph takes into account an $R_{th\ tab\text{-}h} = 1$ °C/W which is to be expected when the tab is connected to a heatsink with one 3 mm bolt, without using heatsink compound. $R_{th\ j\text{-}tab} = 12$ °C/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified; voltages and currents ref. to tab (ground)

			monochrome (Fig. 3)	tiny-vision colour (Fig. 4)	
Supply voltage (pin 8)	V_P	typ.	25	31	V
Supply current (pin 8)	I_P	typ.	165	150	mA
Total power dissipation	P_{tot}	typ.	3,1	3,5	W
Output voltage (peak-to-peak value)	$V_{9(p\text{-}p)}$	typ.	22	28	V
Blanking pulse; I_1 = 1 mA	V_1	typ.	11,5	14,5	V
Blanking pulse duration	t_p	typ.	1,3	1,4	ms
D.C. input voltage (pin 6)	V_6	typ.	3,4	4,4	V
Deflection current (peak-to-peak value)	$I_{9(p\text{-}p)}$	typ.	1,1	0,92	A
Flyback time	t	typ.	1,3	1,32	ms
Free running oscillator frequency	f_{osc}	typ.	46	46	Hz
Oscillator thermal drift		typ.	−0,01	−0,01	Hz/°C
Oscillator voltage shift		typ.	−0,13	−0,12	Hz/V
Tracking range oscillator		typ.	18	18	%
Synchronization input voltage	V_2	>	1	1	V
Voltage divider ratio	V_7/V_8	typ.	0,52	0,52	
Input resistance pin 7	R_7	typ.	2,8	2,8	kΩ
Recommended thermal resistance of heatsink for T_{amb} up to 70 °C	$R_{th\ h\text{-}a}$	<	13	10	°C/W

PINNING

1. Blanking pulse output
2. Synchronization input
3. Oscillator timing network
4. Sawtooth generator
5. S-correction and linearity control
6. Feedback input
7. Voltage divider
8. Positive supply
9. Output

Tab. Negative supply (ground)

APPLICATION INFORMATION (see also Fig. 1)

The function is described against the corresponding pin number

1. Blanking pulse output

When the IC is adjusted on a free running frequency of 46 Hz the internal blanking pulse generator delivers a blanking pulse with a duration between 1,2 ms and 1,5 ms. The circuit is, however, made such that when the flyback time of the deflection current is longer, the blanking pulse corresponds to the flyback time. The output voltage is also high when the voltage at pin 9 is lower than nominal 5 V. An external blanking circuit is recommended when tiny-vision receivers are operated from a car-battery.

2. Synchronization input

The oscillator has to be synchronized by a positive-going pulse. The circuit is made such that synchronization is inhibited during the flyback time.

APPLICATION INFORMATION (continued)

3. Oscillator

   The oscillator frequency is set by the potentiometer P1 and resistor R2 between pins 3 and 7 and capacitor C1 between pin 3 and ground. For 50 Hz systems the free running frequency is preferably adjusted to 46 Hz.

4. Sawtooth generator

   This pin supplies the charging and discharging currents of the capacitor between pin 4 and ground (C2).

5. S-correction and linearity control

   The amount of S-correction can be set by the value of C3. For 110° deflection coils, e.g. AT1040/15, a capacitor of 15 μF will give the right value for S-correction. For 90° deflection systems (e.g. AT1235/00) a nearly linear deflection current is required, this can be achieved by increasing C3 to 100 μF. The linearity can be adjusted by potentiometer P2.

6. Output current feedback

   To this pin is applied a part of the output current measured across R6 and superimposed on a d.c. voltage derived from the voltage across the output coupling capacitor. This signal is compared with the internal reference sawtooth. The internal reference sawtooth has an amplitude of about 0,6 V peak to peak and a d.c. level of about 3,4 V, for a supply voltage of 25 V at pin 8.

7. Internal voltage divider decoupling

   The voltage on this pin is about half the supply voltage at pin 8 and is applied to the bases of emitter followers supplying the pre-stages of the IC. This voltage controls the amplitude of the internal reference sawtooth. In this way tracking with the line deflection system is achieved when the supply voltage at pin 8 is derived from the line output transformer.

8. Positive supply

   The value depends on the deflection coil.

9. Output

   The deflection coil is connected to ground via coupling capacitor C9 and current sensing resistor R6. The line frequency superimposed on the output voltage may be too high due to the current feedback system. The line frequency ripple can be decreased by connecting a resistor across the deflection coil. The flyback time can be influenced by the resistor divider (R4, R5) for the d.c. feedback to pin 6. It should be noted that the output voltage shows a negative swing of about 1 V during the first (positive current) part of the flyback.

Tab

The tab is used as negative supply (ground) connection. Therefore, the tab should be well connected to the negative side of the power supply.

Controlled switch-on

This feature is achieved by charging the a.c. coupling capacitor (C4; connected to pin 6) from an internal current source of about 2 mA (voltage limited to maximum 15 V) for a short period after switch-on. The charging time can be influenced by the value of C5 (connected to pin 7). Discharging of C4 results in a slowly increasing deflection current after a delay of about 1 second. The blanking voltage at pin 1 is high during this delay.

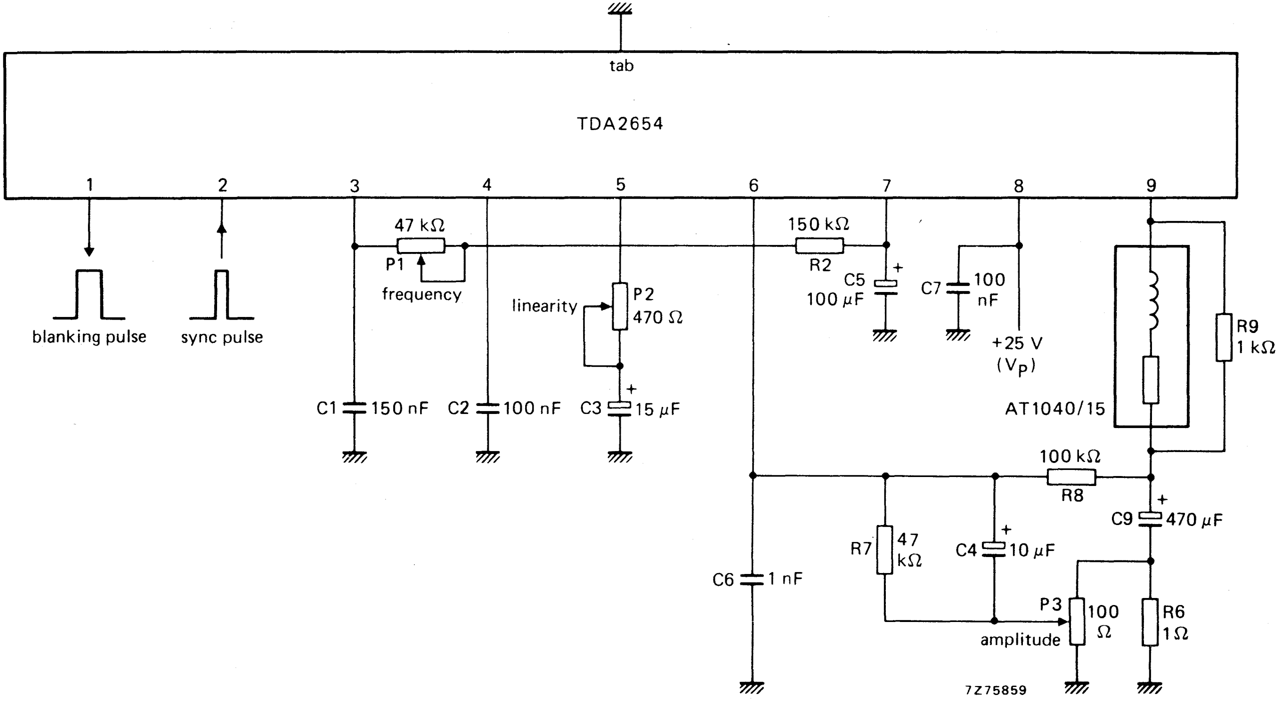
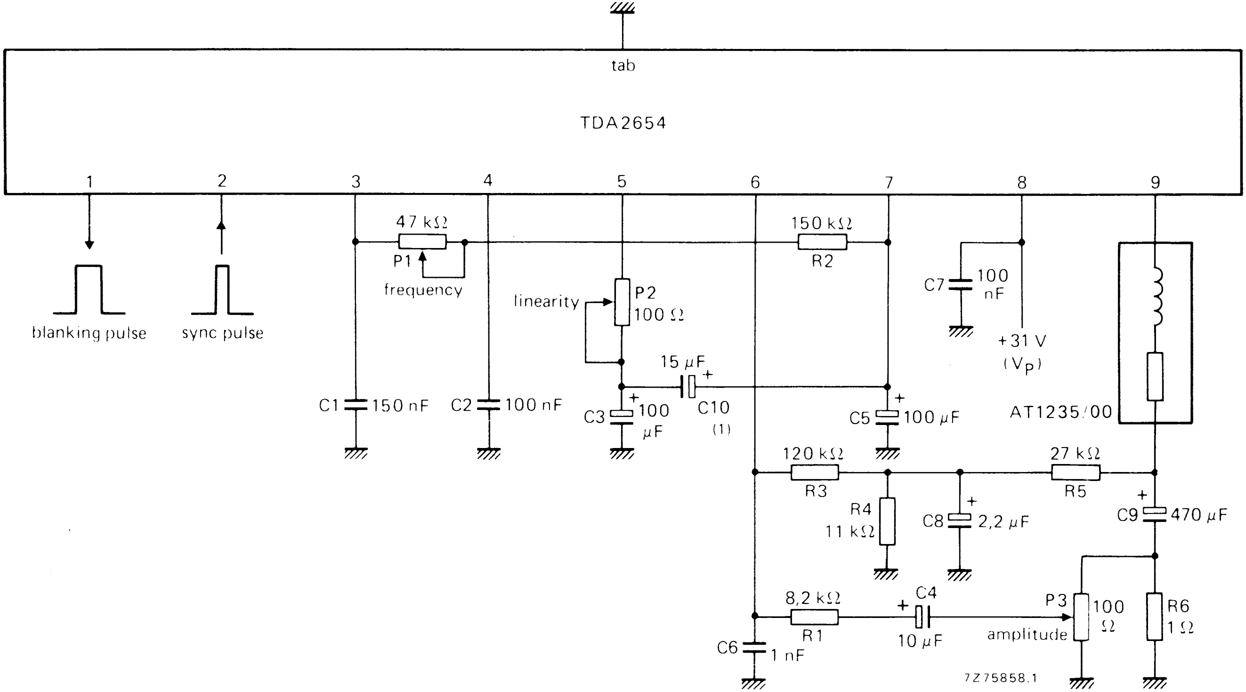


Fig. 3 Monochrome 110° vertical deflection system.

APPLICATION INFORMATION (continued)



(1) Only required when rapid variations in the supply voltage are expected.

Fig. 4 Colour 90° vertical deflection system.

VERTICAL DEFLECTION CIRCUIT

GENERAL DESCRIPTION

The TDA2655B is a monolithic integrated circuit for vertical deflection in colour television receivers with 90° picture tubes.

Features

- Synchronization circuit
- Vertical oscillator; 50/60 Hz switch
- Sawtooth generator with buffer stage
- Preamplifier with fed-out inputs
- Output stage with termal and short-circuit protection
- Flyback generator
- Blanking pulse generator with guard circuit
- Voltage stabilizer
- Frequency detector with memory and storage

QUICK REFERENCE DATA

For 90° deflection; measured with respect to cooling fin (ground)

			concept 1*	concept 2*	
System supply voltages	V_{P1}	typ.	22	22	V
	V_{P2}	typ.	12	–	V
System supply currents	I_{P1}	typ.	135	140	mA
	$-I_{P2}$	typ.	8	–	mA
Deflection current (peak-to-peak value)	$I_{9(p\text{-}p)}$	typ.	450	450	mA
Synchronization input voltage (peak-to-peak value)	$V_{5(p\text{-}p)}$	min.	1	1	V

*Concept 1: with two supply voltages ; concept 2: with one supply voltage. (See also Figs 2 and 3).

PACKAGE OUTLINE

12-lead DIL; plastic with metal cooling fin (SOT-150).

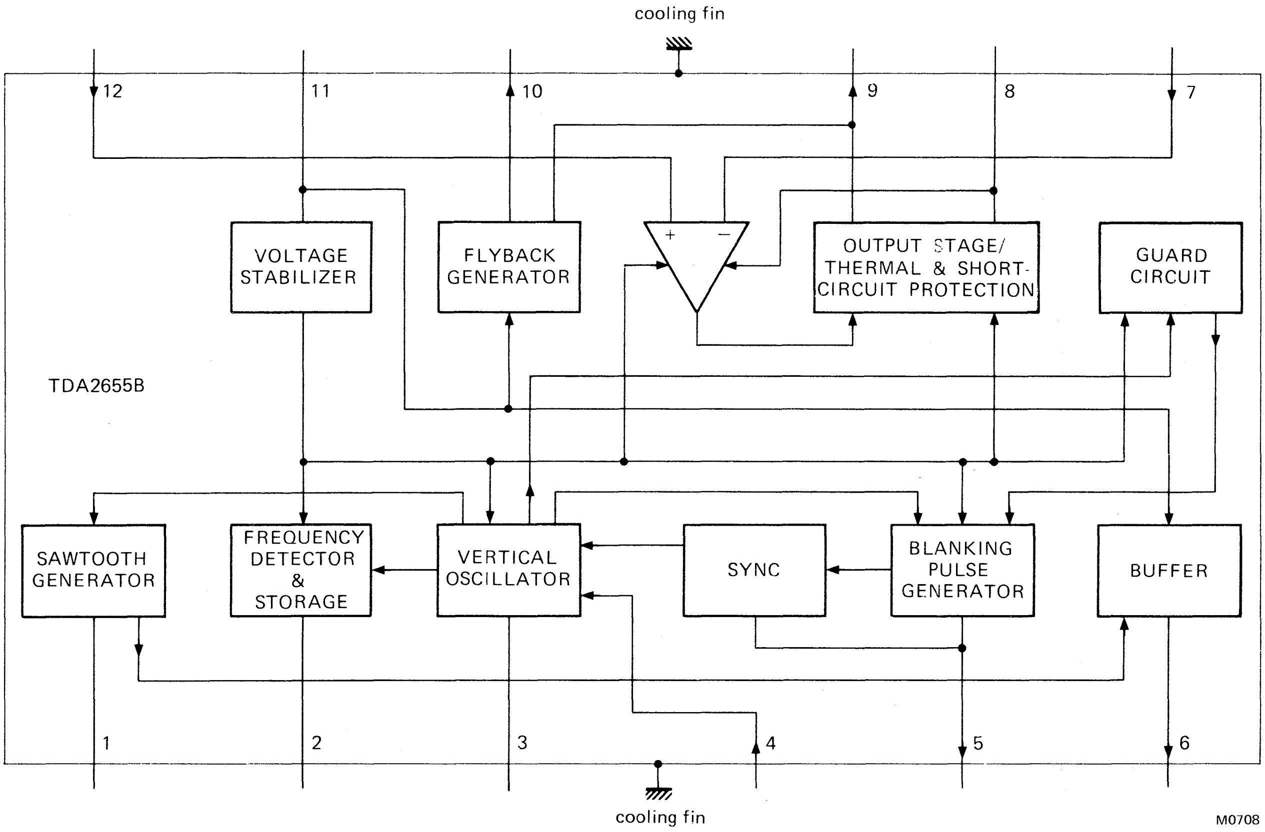


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

with respect to cooling fin (ground)

Supply voltage (pin 11)	$V_{11} = V_P$	max.	40	V
Supply voltage output stage (pin 8)	V_8	max.	60	V
Pin 9	V_9	max.	60	V
	$-V_9$	max.	0	V
Pin 10	V_{10}	max.	40	V
Pin 3	V_3	max.	7	V
Pin 1	V_1	max.	40	V
Pin 6	V_6	max.	7	V
Pins 7 and 12	$V_7; V_{12}$	max.	24	V

Currents

Pin 10	I_{10}	max.	1,2	A
	$-I_{10}$	max.	1,5	A
Pin 5	$\pm I_5$	max.	10	mA
Pin 2	I_2	max.	3	mA
Pin 1	I_1	max.	50	mA
	$-I_1$	max.	0,1	mA
Pin 6	$-I_6$	max.	5	mA
Pin 4	$-I_4$	max.	1	mA
Pin 8, pin 9 and cooling fin	internally limited by the short-circuit protection circuit			

Temperatures

Total power dissipation	internally limited by the short-circuit protection circuit	
Storage temperature range	T_{stg}	−55 to +150 °C
Operating ambient temperature range	T_{amb}	−25 °C to limiting value

PINNING

pin number	function	pin number	function
1.	sawtooth capacitor	7.	feedback input
2.	frequency storage information	8.	positive supply of output stage
3.	oscillator capacitor	9.	output
4.	oscillator resistor (adjustment)	10.	flyback generator output
5.	synchronization input/blanking output	11.	positive supply (V_P)
6.	sawtooth buffer stage output	12.	preamplifier input

CHARACTERISTICS

V_P = 22 V; T_{amb} = 25 °C; these characteristics are measured with respect to cooling fin (ground), unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage/output stage					
Supply voltage	$V_{11} = V_P$	9	–	30	V
Output voltage					
at I_9 = 0,75 A	V_9	–	1,2	1,4	V
at $-I_9$ = 0,75 A	V_9	$(V_P - 1{,}9)$	$(V_P - 1{,}7)$	–	V
Flyback generator output voltage at I_{10} = 0,75 A	V_{10}	–	$(V_P - 2{,}0)$	–	V
Supply currents (without load)					
pin 11	I_{11}	–	10	–	mA
pin 8	I_8	–	3	–	mA
Output current	$\pm I_9$	–	–	1,2	A
Flyback generator peak current	$\pm I_{10}$	–	–	1,2	A
Feedback					
Preamplifier quiescent input currents	$-I_7 = -I_{12}$	–	0,1	–	μA
Synchronization					
Sync input voltage range	V_5	1,0	–	–	V
Synchronizing range		–	28	–	%
Oscillator/sawtooth generator					
Frequency setting input voltage	V_4	6	–	9	V
Sawtooth generator output voltage (peak value)	$V_{1(m)}$	0	$(V_P - 2)$	–	V
Sawtooth generator output current	I_1	–	–	30	mA
Sawtooth generator leakage current	$-I_1$	2	–	–	μA
Oscillator temperature dependency T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	–	10^{-4}	–	K^{-1}
Oscillator voltage dependency V_P = 10 to 30 V	$(\Delta f/f)/\Delta V_P$	–	10^{-3}	–	V^{-1}
Blanking pulse generator					
Output voltage (at I_5 = 1 mA)	V_5	–	20	–	V
Output resistance	R_5	–	410	–	Ω
Output current (at V_P = 21 V)	$-I_5$	–	–	5	mA
Blanking pulse duration at 50 Hz sync	t_b	1,33	1,4	1,47	ms
50/60 Hz frequency detector					
Output saturation voltage (LOW level for 50 Hz)	V_2	–	1	–	V
Leakage current	I_2	–	1	–	μA

parameter	symbol	min.	typ.	max.	unit
Buffer stage					
Output voltage	$V_{6(m)}$	0	$(V_P - 1)$	–	V
Output current	$-I_6$	–	–	4	mA
Thermal resistance					
From junction to case (cooling fin)	$R_{th\ j\text{-}c}$	–	–	15	K/W
Junction temperature					
Switching point thermal protection	T_j	142	150	158	°C

APPLICATION INFORMATION

The following application data is obtained from measurements made on the circuits shown in Figs 2 and 3, application circuits for 90° deflection systems. Measurements are made with respect to the cooling fin (ground).

			Fig. 2 concept 1*	Fig. 3 concept 2*	
System supply voltages	V_{P1}	typ.	22	22	V
	V_{P2}	typ.	12	–	V
Supply currents	I_{P1}	typ.	135	140	mA
	$-I_{P2}$	typ.	8	–	mA
Output voltage (d.c. value)	V_9	typ.	12,2	13,8	V
Output voltage (peak-to-peak value)	$V_{9(p\text{-}p)}$	typ.	42	43	V
Output current (peak value)	$-I_{9(m)}$	typ.	450	450	mA
Deflection current (peak-to-peak value)	$I_{defl\ (p\text{-}p)}$	typ.	850	850	mA
Flyback time	t_{fl}	typ.	0,9	1,0	ms
Oscillator frequency adjustment without sync	f_o	typ.	46,5	46,5	Hz
Total power dissipation per package (see note)	P_{tot}	max.	1,8	1,8	W
Ambient temperature	T_{amb}	max.	70	70	°C
Thermal resistance (junction to ambient)	$R_{th\ j\text{-}a}$	max.	40	40	K/W

*Concept 1 : with two supply voltages; concept 2 : with one supply voltage.

Note

Calculated with ΔV_{P1} of +5% and ΔR_{defl} of –7%.

DEVELOPMENT SAMPLE DATA

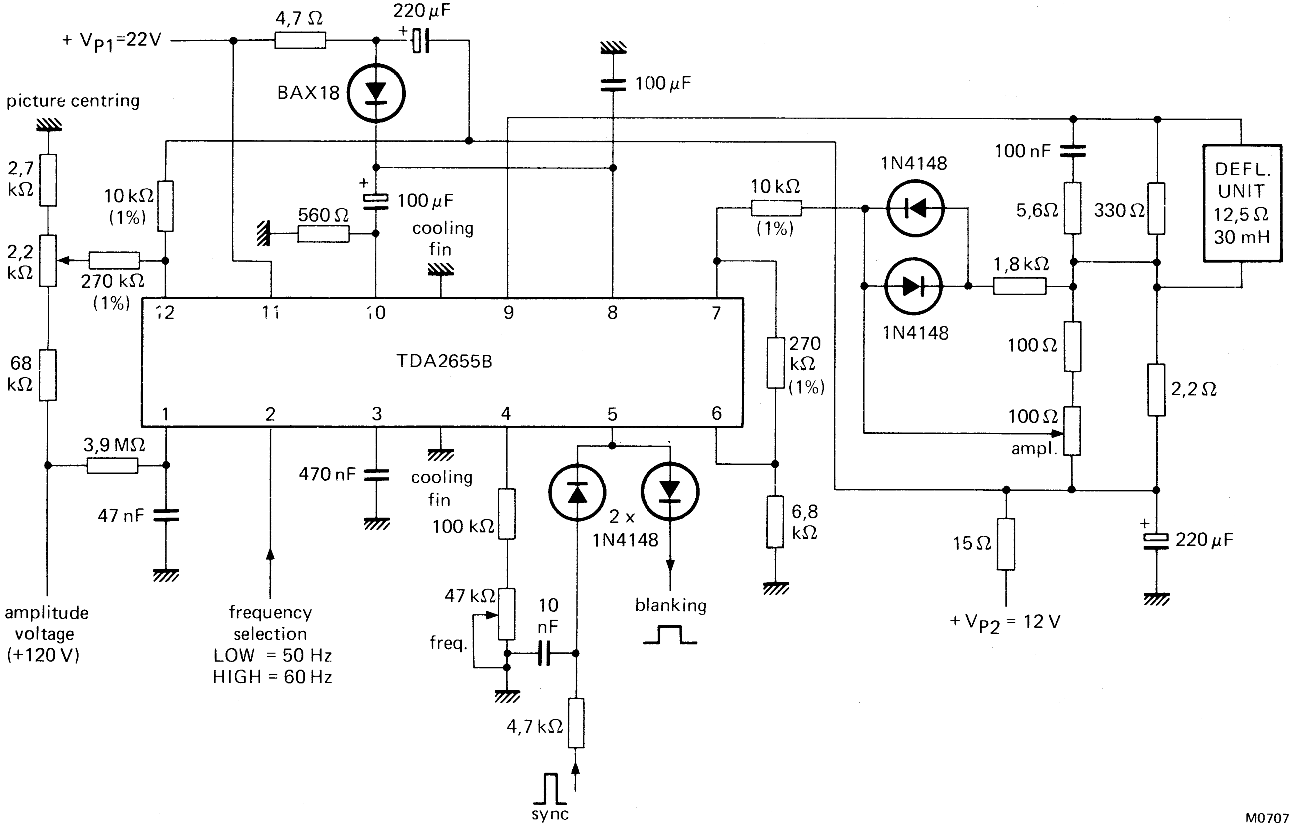


Fig. 2 Typical application circuit with two supply voltages; for use with 90° picture tubes.

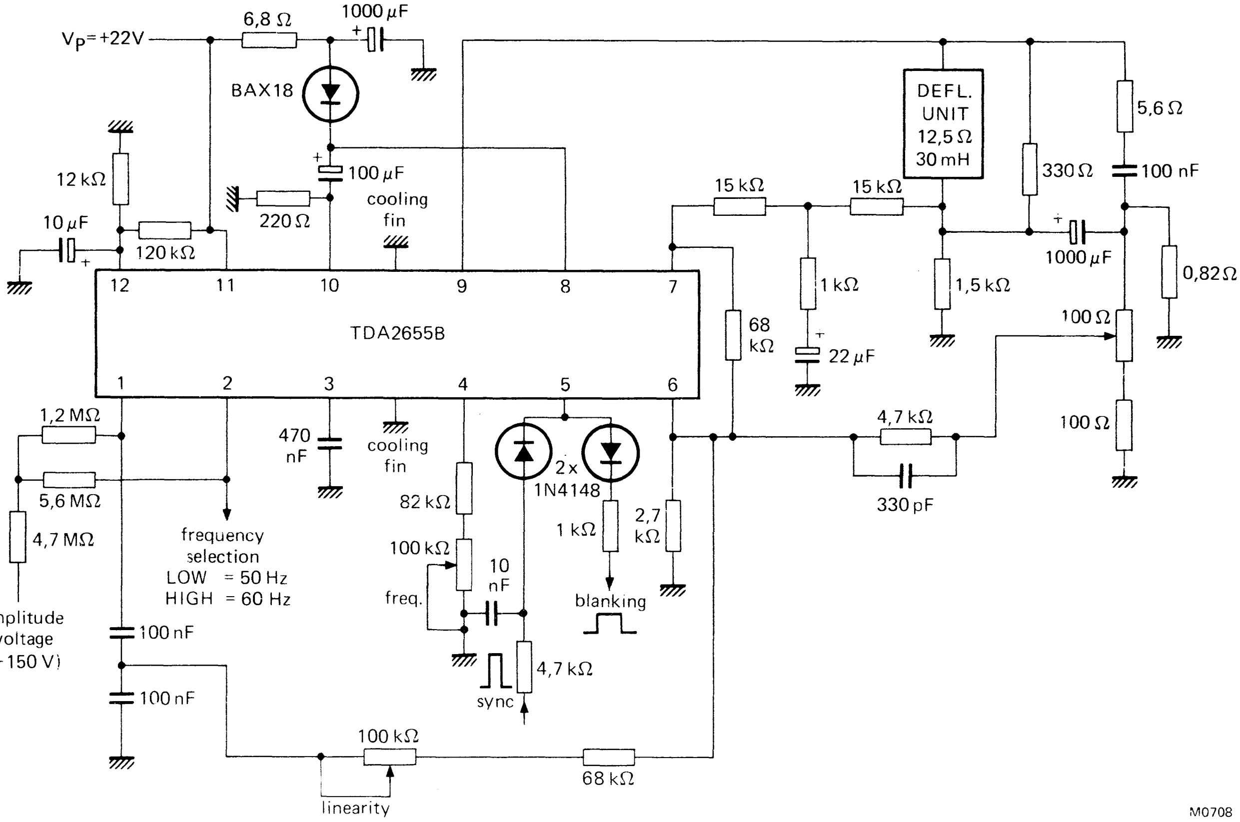


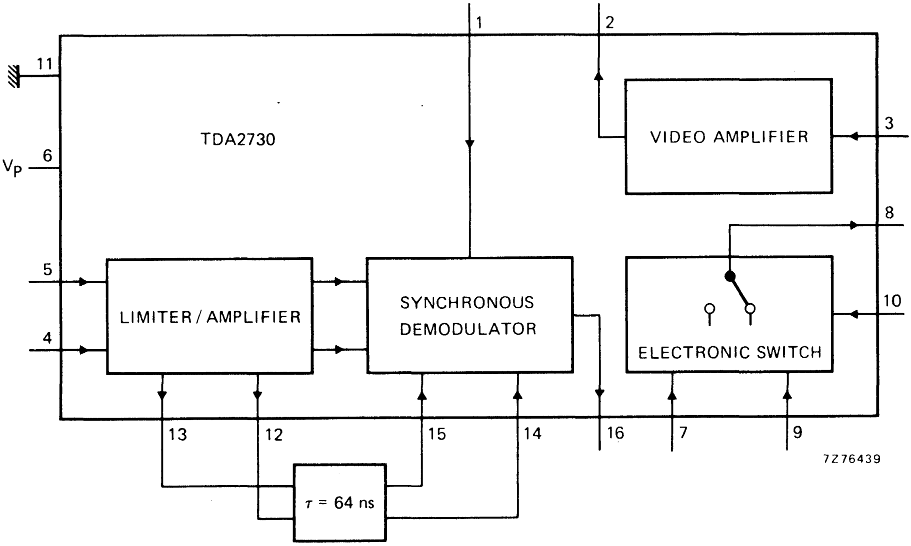
Fig. 3 Typical application circuit for a single supply voltage; for use with 90° picture tubes.

FM LIMITER/DEMODULATOR

The TDA2730 is a monolithic integrated circuit for use in audio-visual equipment, e.g.; video recorders and video disc players.
The circuit comprises an f.m. limiter/demodulator for the playback signal, a video amplifier and an electronic switch, which can be used for drop-out elimination.

QUICK REFERENCE DATA				
Supply voltage	V_{6-11}	typ.	12	V
Supply current	I_6	typ.	42	mA
Input signal range (peak-to-peak value)	$V_{4-5(p-p)}$		30 to 2000	mV
Video output signal (peak-to-peak value)	$V_{2-11(p-p)}$	typ.	4	V

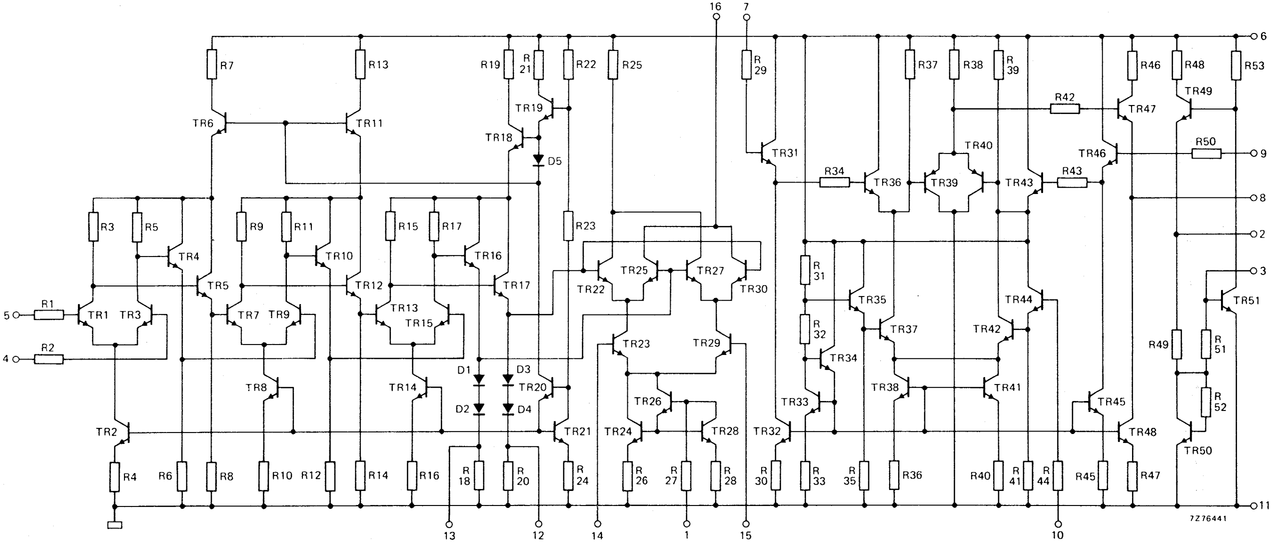
BLOCK DIAGRAM



PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

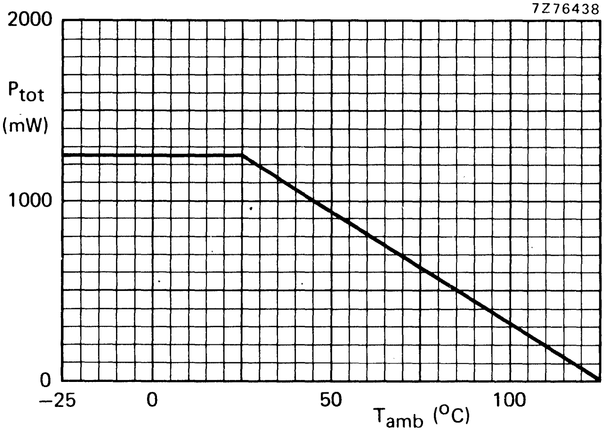
Supply voltage	V_{6-11}	max.	13	V

Power dissipation

Total power dissipation (see also derating curve below)	P_{tot}	max.	1,25	W

Temperatures

Storage temperature	T_{stg}	−65 to +125	°C
Operating ambient temperature	see derating curve below		



CHARACTERISTICS measured in the circuit on in Fig. 1

Supply voltage range	V_{6-11}	typ.	12	V
			11 to 13	V

The following characteristics are measured at V_{6-11} = 12 V; T_{amb} = 25 °C

Supply current	I_6	typ.	42	mA
			25 to 54	mA

Limiter

Start of limiting (−3 dB) f_o = 4 MHz; peak-to-peak value	$V_{4-5(p-p)}$	typ.	0,8	V
Input signal range for constant luminance output (peak-to-peak value)	$V_{4-5(p-p)}$		30 to 2000	mV
Output voltage (peak-to-peak value)	$V_{12-13(p-p)}$	typ.	750	mV
Available output voltage at an external load of 1 kΩ; peak-to-peak value	$V_{12-13(p-p)}$	>	5	V

Demodulator

Measured at I_1 = 4 mA; $|Z_{16-11}|$ = 1,5 kΩ; delay time τ = 64 ns; Δf = 1,4 MHz (f_L = 3,0 MHz, f_H = 4,4 MHz)

Current ratio	I_1/I_{16}	typ.	1	
Output voltage (peak-to-peak value)	V_{16-11}	typ.	540	mV

Drop-out switch

Input drive voltage range	$V_{7;9-11}$		6,5 to 12	V
Voltage drop between input and output				
for signal flow from pin 7 to pin 8	V_{7-8}	typ.	1,5	V
for signal flow from pin 9 to pin 8	V_{9-8}	typ.	1,5	V
Input offset voltage	$\lvert V_{7-8}-V_{9-8}\rvert$	<	20	mV
Switch actuating input voltage				
for signal flow from pin 7 to pin 8	V_{10-11}		0 to 2,7	V
for signal flow from pin 9 to pin 8	V_{10-11}		3,7 to 6,0	V
Output impedance at 1,5 mA by internal load	Z_{8-11}		emitter follower	

CHARACTERISTICS (continued)

Video amplifier

Input voltage level	V_{3-11}	typ.	730	mV
Output voltage level	V_{2-11}	typ.	5,5	V
Open loop gain	G	typ.	43	dB
Bandwidth (3 dB)	B	typ.	8,8	MHz
Output voltage (peak-to-peak value; see note)	$V_{2-11(p-p)}$	typ.	4	V

Note

The gain of the amplifier is determined by the feedback network comprising the impedances between pins 2 and 3, and pins 8 and 3. The values quoted apply to the circuit in Fig. 1.

PINNING

1. Current setting demodulator	9. Switch input
2. Video amplifier output	10. Switch actuating input
3. Video amplifier input	11. Negative supply (ground)
4. F.M. signal input	12. Limiter output
5. F.M. signal input	13. Limiter output
6. Positive supply	14. Demodulator input
7. Switch input	15. Demodulator input
8. Switch output	16. Demodulator output

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1. Current setting of demodulator

   The current into this pin directly determines the amplitude and the d.c. level of the demodulator output. At I_1 = 4 mA, optimum temperature compensation is obtained.

2. Video amplifier output

   A signal up to 4 V peak-to-peak is available from this output (Fig. 1).
   This can be the video signal (Fig. 1) or the f.m. signal to the delay line (drop-out elimination; Fig. 2).

3. Video amplifier input

   The demodulator output signal is the input signal to this pin (Fig. 1) or the f.m. modulated signal (Fig. 2).

4. F.M. signal input (in conjunction with pin 5)

   A frequency modulated signal of 1 V peak-to-peak is applied between pins 4 and 5. D.C. feedback from the limiter output is applied to stabilize the operation.

5. F.M. signal input

   See pin 4.

APPLICATION INFORMATION (continued)

6. Positive supply

   Correct operation can be obtained in the range 11 to 13 V.

7. Switch input

   The signal applied to pin 7 or to pin 9 is transferred to pin 8, depending on the switch position. For an input level between 0 and 2,7 V at pin 10, the signal at pin 7 is transferred to pin 8, and when between 3,7 and 6 V the input signal at pin 9 is transferred to pin 8.
   The signal at pin 7 or pin 9 may vary from 6,5 to 12 V.
   The signal at pin 8 is 1,5 V below the value at pin 7 or 9.
   The difference in input level at pins 7 and 9, to obtain equal output at pin 8, will be less than 20 mV.

8. Switch output

   See pin 7.

9. Switch input

   See pin 7.

10. Switch actuating input

    See pin 7.

11. Negative supply (ground)

12. Limiter output

    A balanced signal is available between pins 12 and 13. The signal amplitude is limited to 750 mV at both outputs.

13. Limiter output

    See pin 12.

14. Demodulator input

    A phase shifted signal (with respect to the internally applied signal) is applied between pins 14 and 15.

15. Demodulator input

    See pin 14.

16. Demodulator output

    The output signal is proportional to :
    - current into pin 1
    - slope of the phase characteristic of the network between pins 12 and 13, and pins 14 and 15
    - impedance level at the output
    - the sweep (Δf) of the f. m. signal.

    A signal of typically 540 mV is available at this pin when using the component values in Fig. 1 and $\Delta f = 1,4$ MHz.

APPLICATION INFORMATION (continued)

Test circuit

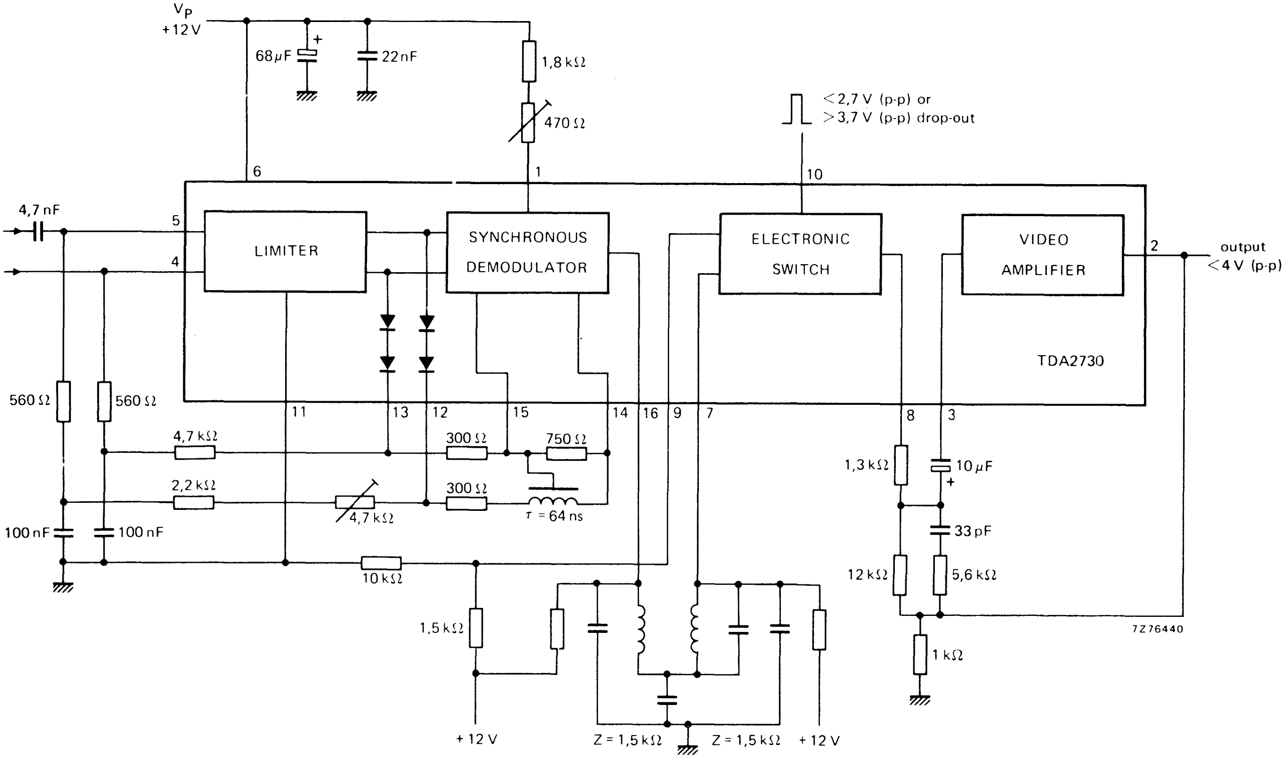


Fig. 1

APPLICATION INFORMATION (continued)

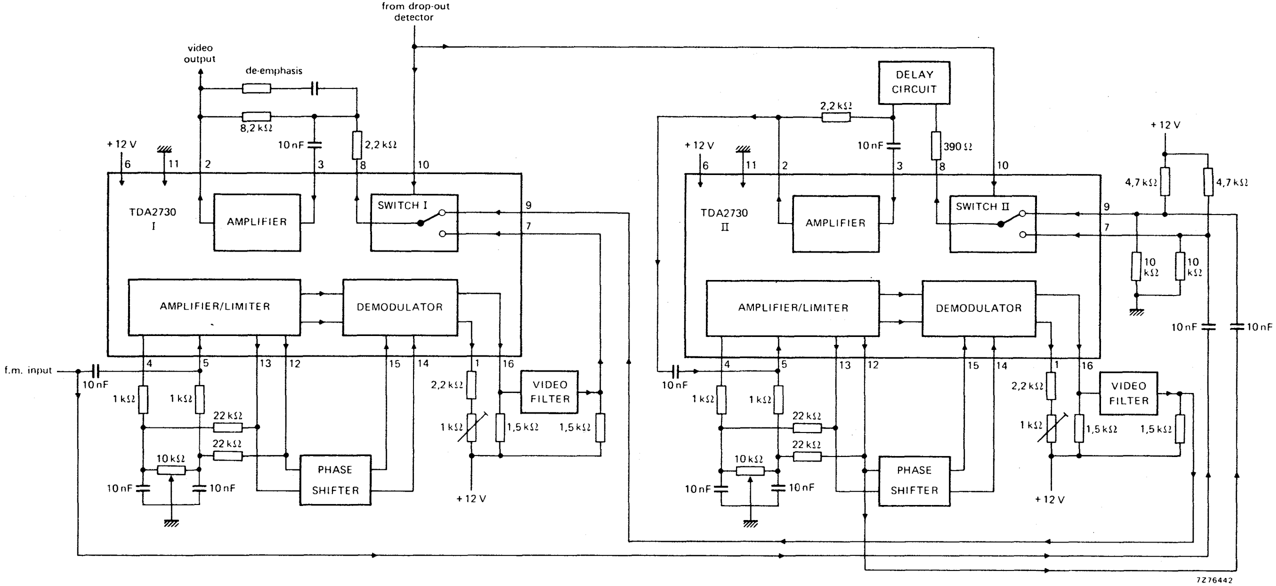


Fig. 2. Drop-out eliminator.

AMPLIFIER AND DROP-OUT IDENTIFICATION CIRCUIT

GENERAL DESCRIPTION

The TDA2740 is a monolithic integrated circuit intended for use in colour television receivers. It also can be used, in conjunction with the TDA2730, in the reproduction part of video recorder sets. The circuit incorporates the following functions:

- Electronic switch
- A.G.C. FM amplifier with display drive capability
- Drop-out detector
- Schmitt-trigger for generating a drop-out pulse

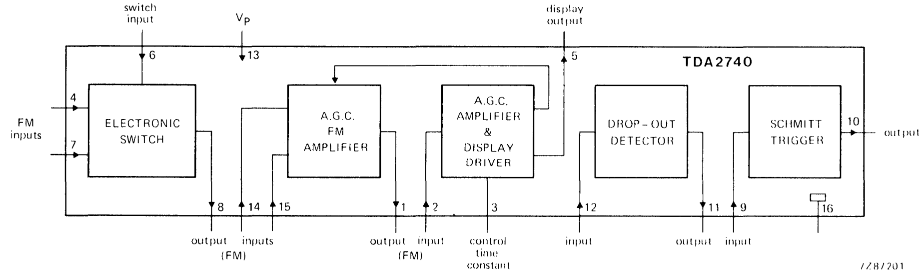


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

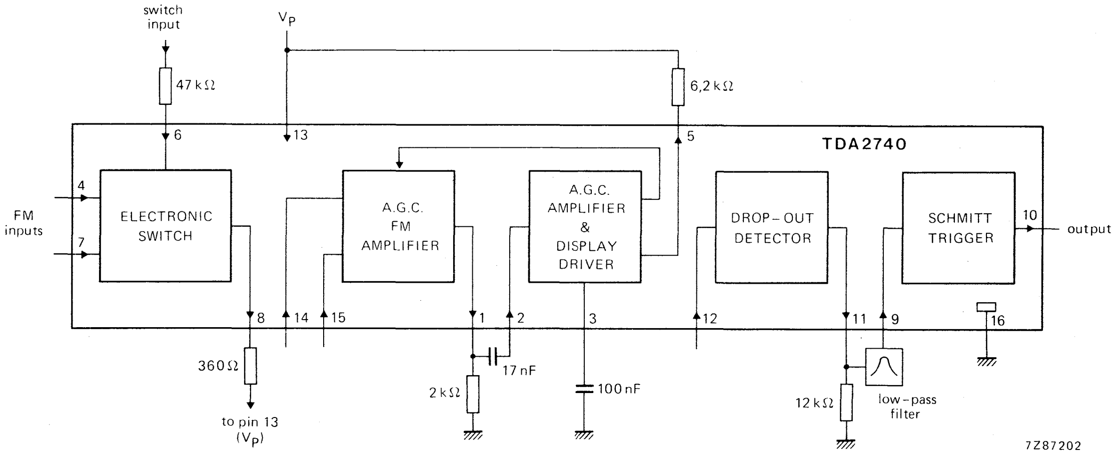


Fig. 2 Test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_{13\text{-}16} = V_P$	max.	13 V
Total power dissipation	P_{tot}	max.	780 mW
Storage temperature range	T_{stg}	–25 to +150 °C	
Operating ambient temperature range	T_{amb}	–20 to +90 °C	

CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage range (pin 13)	V_P	11,5	12	13	V
Supply current (pin 13)	I_P	30	40	60	mA
Electronic switch					
Input voltages (d.c.)	$V_{4;7\text{-}16}$	6,5	7,1	7,5	V
Input impedances	$\|Z_{4;7\text{-}16}\|$	–	1	–	kΩ
Input voltages (pin 6)					
for signal from pin 7 to pin 8	V_6	0	–	1,7	V
for signal from pin 4 to pin 8	V_6	2,7	–	V_P	V
Input current (pin 6)	I_6	–	–	60	μA
Output pin 8			open collector		
Output current (d.c.)	I_8	1,3	1,8	2,5	mA
Output voltage	$V_{8\text{-}16}$	6,7	–	V_P	V
Forward transfer admittance	$\|Y_f\|$	2,45	3,3	4,45	mS
2nd harmonic suppression referred to a sinusoidal signal at pin 4 or 7 of $V_{4;7(p\text{-}p)} = 500$ mV; f = 4 MHz	α	–	–43	–	dB
A.G.C. amplifier and display driver					
Input voltages (d.c.)	$V_{14;15\text{-}16}$	2,3	2,6	2,9	V
Input impedance	$\|Z_{14\text{-}15}\|$	–	1,2	–	kΩ
Input voltage range (peak-to-peak value)	$V_{14\text{-}15(p\text{-}p)}$	6	–	60	mV
Output voltage (peak-to-peak value)	$V_{1(p\text{-}p)}$	0,7	1	1,4	V
Open-loop voltage gain at f = 4 MHz	G_{ov}	43	46	49	dB
Bandwidth (–3 dB) within control range	B	7	–	–	MHz
Output voltage (d.c.)	$V_{1\text{-}16}$	5,0	6,7	8,5	V
Output impedance	$Z_{1\text{-}16}$		emitter follower		
Input voltage (d.c.)	$V_{2\text{-}16}$	2,2	2,5	2,8	V
Input impedance	$\|Z_{2\text{-}16}\|$	–	2,3	–	kΩ
Output pin 5			open collector		

CHARACTERISTICS (continued)

paramter	symbol	min.	typ.	max.	unit
A.G.C. amplifier and display driver (continued)					
Display current (pin 5)					
without input signal	I_5	–	–	400	μA
with input signal of 60 mV (peak to peak)	I_5	–	1,3	–	mA
D.C. voltage at pin 3					
without input signal	$V_{3\text{-}16}$	1,1	1,5	1,9	V
with input signal	$V_{3\text{-}16}$	2,4	2,7	3,2	V
Drop-out detector					
Input voltage (d.c.)	$V_{12\text{-}16}$	2,6	2,8	3,0	V
Input impedance	$\lvert Z_{12\text{-}16}\rvert$	–	1	–	kΩ
Input voltage (a.c.) (peak-to-peak value)					
for negative-going threshold (t_{PLH})	$V_{12(p\text{-}p)}$	9	18	36	mV
for positive-going threshold (t_{PHL})	$V_{12(p\text{-}p)}$	11	26	60	mV
Output pin 11		open collector			
Maximum output current	I_{11}	–	2,3	–	mA
Output current (d.c.) without input signal	I_{11}	–	1,3	–	mA
Schmitt-trigger (see Fig. 3)					
Threshold voltage: ON	$V_{9\text{-}16}$	10,05	10,15	10,30	V
Threshold voltage: OFF	$V_{9\text{-}16}$	9,65	9,80	9,95	V
Input impedance	$\lvert Z_{9\text{-}13}\rvert$	–	1,2	–	kΩ
Output voltage HIGH	$V_{10\text{-}16H}$	3,7	3,9	4,2	V
Output voltage LOW	$V_{10\text{-}16L}$	2,1	2,4	2,7	V
Output impedance	$Z_{10\text{-}16}$	emitter follower			

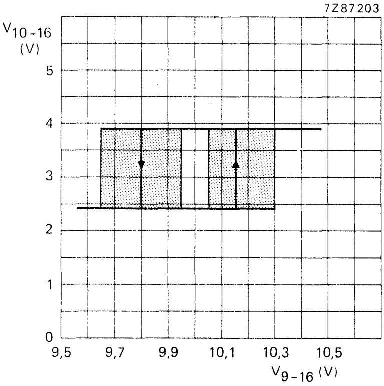


Fig. 3 Schmitt-trigger output voltage as a function of the input voltage.

TELEVISION SOUND COMBINATION

The TDA2791 contains the following functions:

- Limiter/amplifier
- F.M. detector.
- Physiological d.c. volume control.
- D.C. tone control.

The limiter/amplifier is designed as a four-stage differential amplifier, to obtain good noise and interference suppression. The detector is a balanced quadrature demodulator.

During VTR operation audio signals can be inserted before the tone and volume control circuits. The limiter amplifier and demodulator must be switched off by grounding pin 2. This switching action occurs without a d.c. shift, so that no transients will be noticed in the speaker. The circuit is very flexible in its application because the characteristics of the various controls can be adapted by changing external component values.

QUICK REFERENCE DATA

Supply voltage	$V_{13\text{-}3}$	typ.	12	V
Total current drain	I_{13}	typ.	61	mA
Frequency	f_o		5,5	MHz
Input voltage at start of limiting (r.m.s. value)	$V_{i(rms)}$	typ.	100	μV
A.M. rejection at $V_i = 5$ mV	α	typ.	60	dB
A.F. output voltage at $\Delta f = \pm 27$ kHz (r.m.s. value) (at pin 7 after de-emphasis)	$V_{o(rms)}$	typ.	700	mV
D.C. bass control range		<	+16 −19	dB
D.C. treble control range		<	+12 −15	dB
D.C. volume control range		>	−75	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

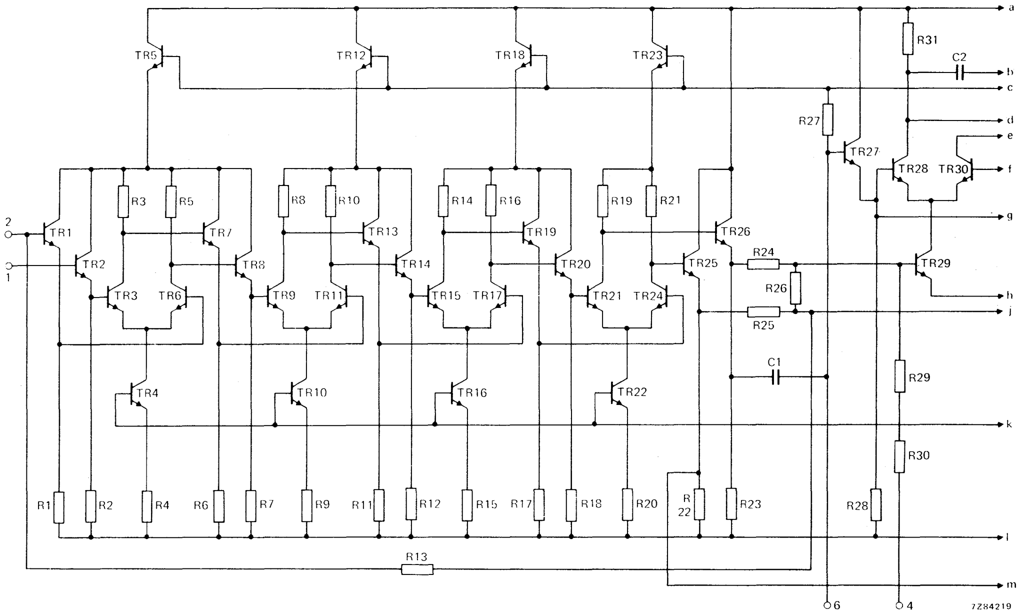


Fig. 1a Circuit diagram; continued in Fig. 1b.

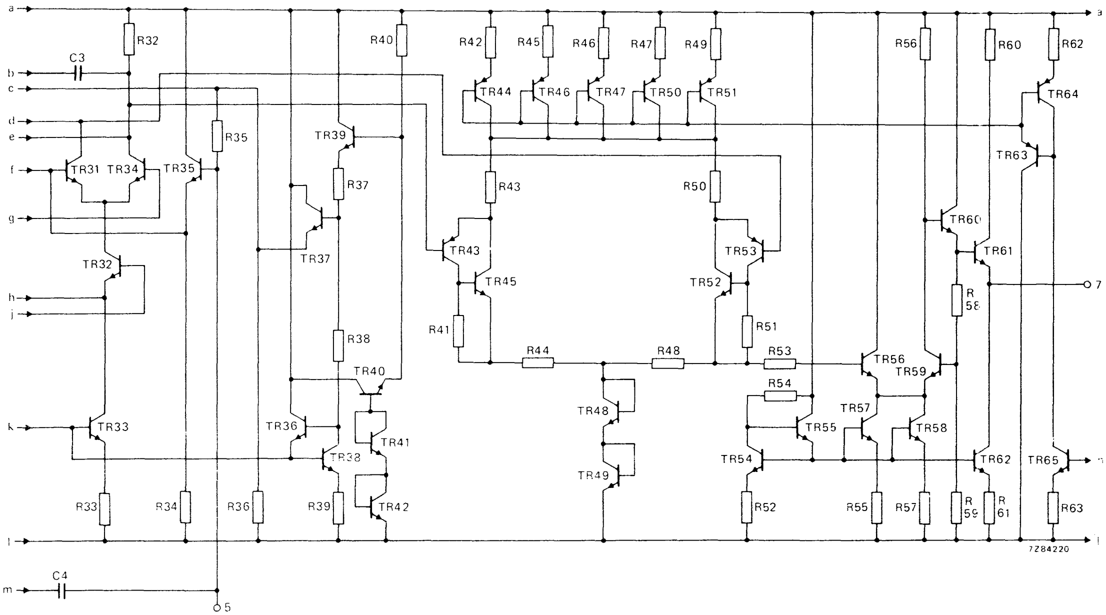


Fig. 1b Circuit diagram; continued from Fig. 1a; continued in Fig. 1c, for line 'n' see Fig. 1d.

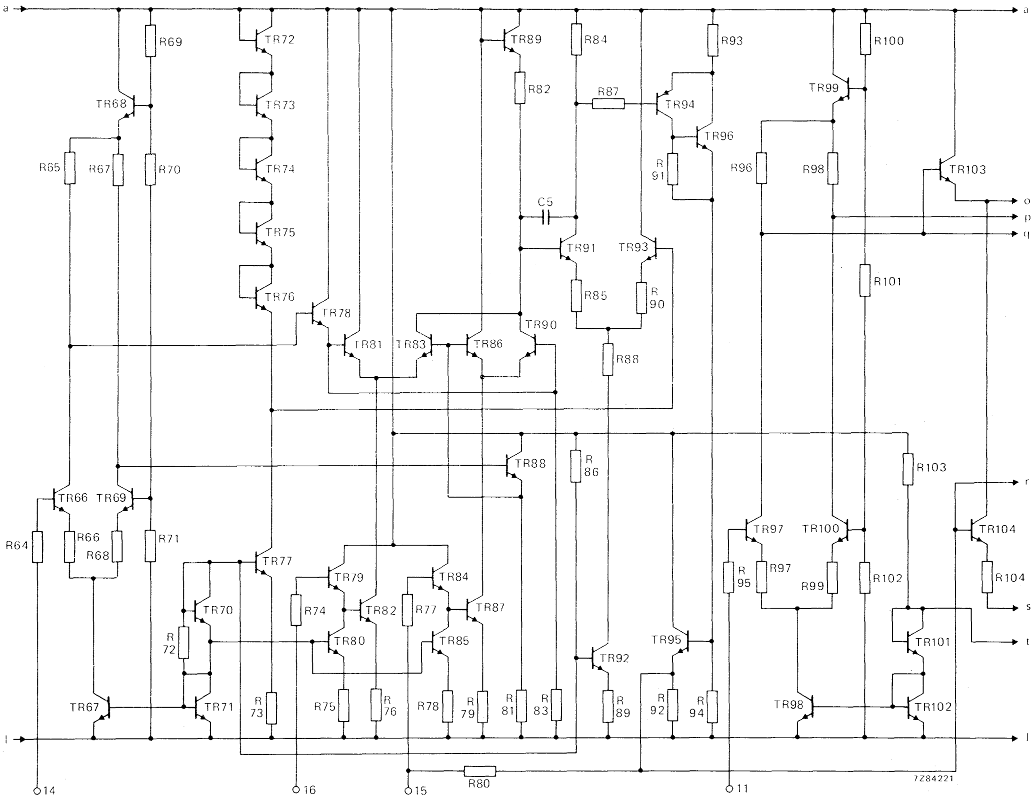


Fig. 1c Circuit diagram; continued from Fig. 1b; continued in Fig. 1d.

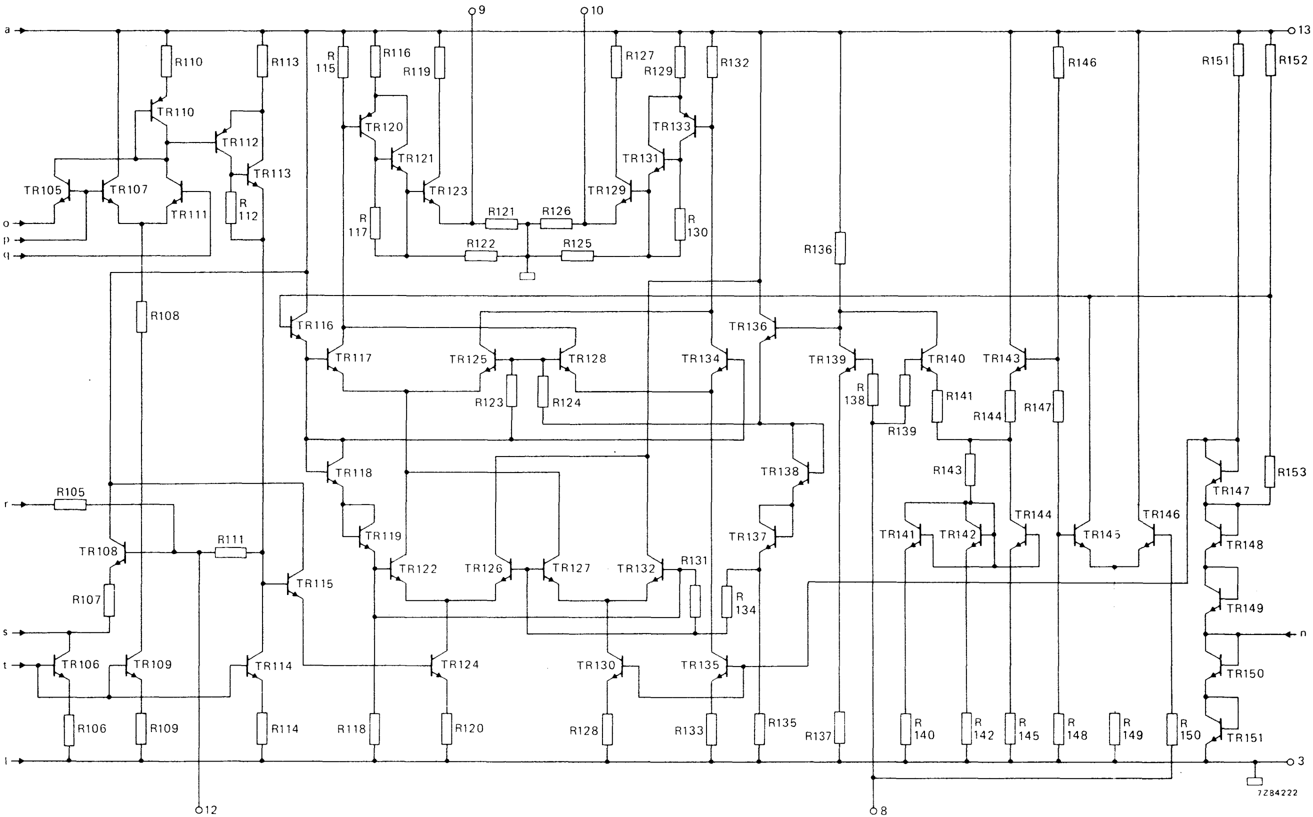


Fig. 1d Circuit diagram; continued from Fig. 1c and Fig. 1b.

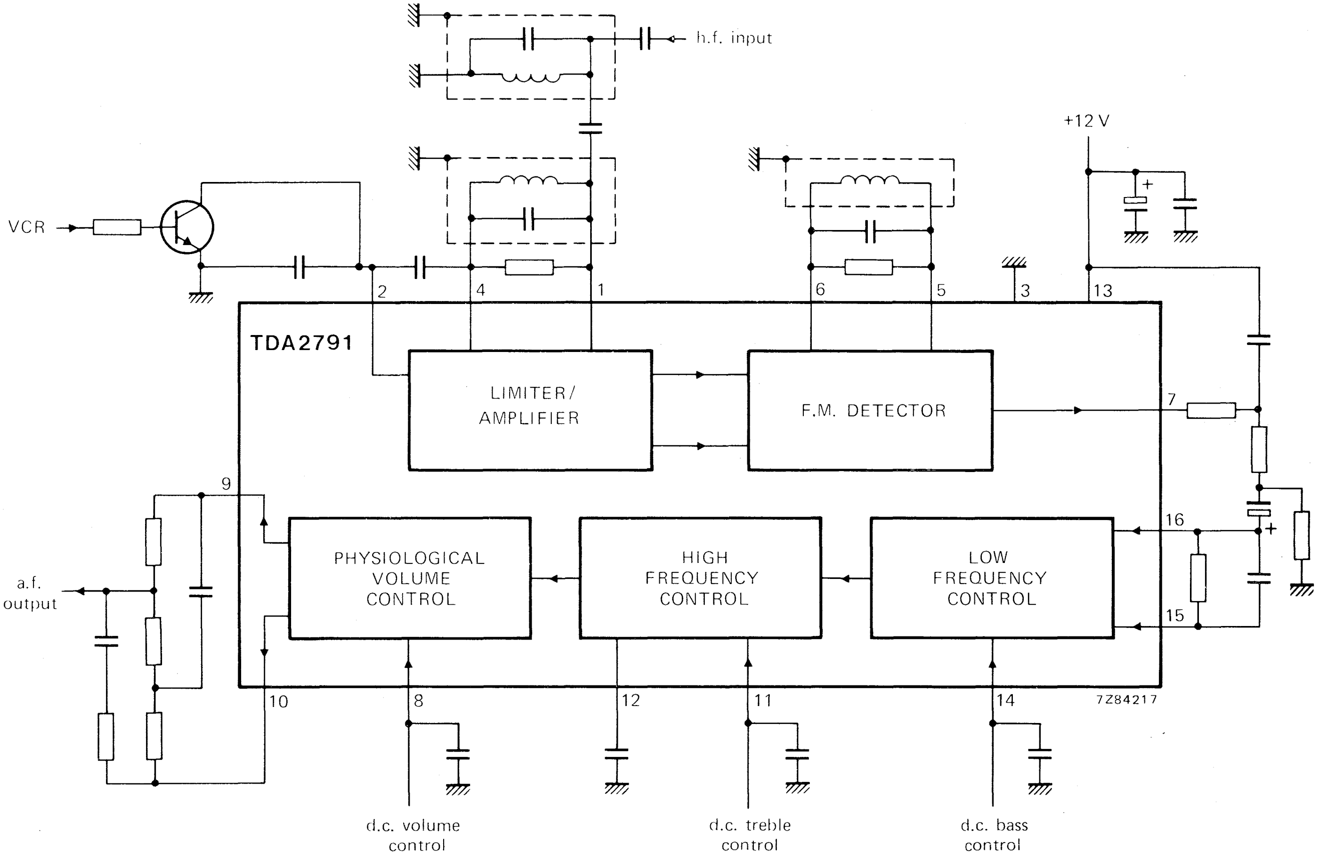


Fig. 2 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{13\text{-}3}$	max.	13,2 V

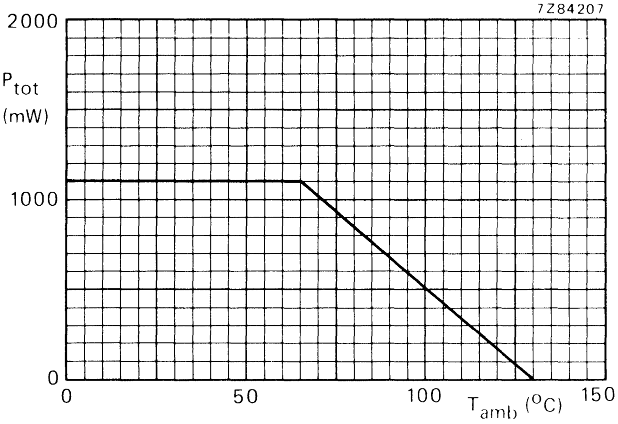


Fig. 3 Power derating curve.

Storage temperature	T_{stg}	−25 to + 130 °C
Operating ambient temperature	T_{amb}	−25 to + 65 °C

CHARACTERISTICS

Measured in Fig. 9 at T_{amb} = 25 °C; $V_{13\text{-}3}$ = 12 V; f = 5,5 MHz (unless otherwise specified)

Supply voltage range	$V_{13\text{-}3}$	10,8 to 13,2 V
Total current drain	I_{13}	43 to 79 mA

Limiter/amplifier/demodulator (note 1)

Input limiting voltage at $V_{7\text{-}3}$ = −3 dB (r.m.s. value)	$V_{i(rms)}$	typ.	100 µV
Input impedance	$\lvert Z_{1\text{-}3} \rvert$	typ.	200 kΩ
A.M. rejection			
V_i = 0,5 mV (note 2)	α	typ.	50 dB
V_i = 1 mV (note 2)	α	typ.	50 dB
V_i = 5 mV (note 2)	α	typ.	60 dB
V_i = 50 mV (note 2)	α	typ.	55 dB
A.F. output voltage at pin 7 (r.m.s. value) f_m = 1 kHz; Δf = ± 27 kHz; V_i = 5 mV; Q_{L3} = 12,5	$V_{o(rms)}$	typ.	700 mV

Notes
1. The quadrature reference circuit must be tuned in such a way that there is no difference in the demodulator d.c. output voltage when the limiter input is switched from signal to no signal.
2. See test set-up Fig. 4.

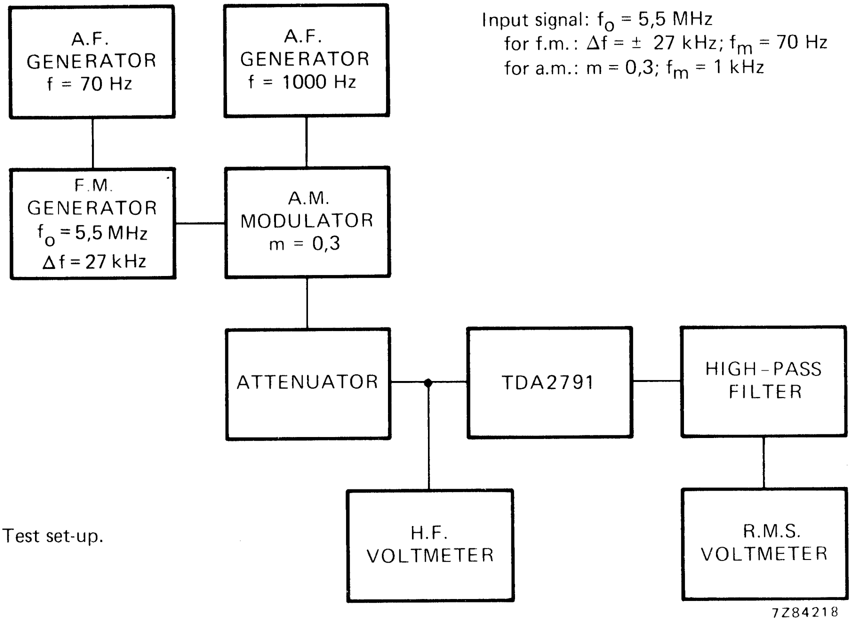
CHARACTERISTICS (continued)

Total harmonic distortion at pin 7				
f_m = 1 kHz; Δf = ± 27 kHz; V_i = 5 mV	d_{tot}	typ.	0,35	%
Zero-point stability at 30 μV to 10 mV; pin 7		typ.	2	kHz
Hum suppression; pin 7		typ.	20	dB
Signal-to-noise ratio at pin 7				
f_m = 1 kHz; Δf = ± 27 kHz; V_i = 5 mV (note 1)	S/N	typ.	63	dB
Demodulator output impedance	$\lvert Z_{7-3} \rvert$	typ.	25	Ω

A.F. amplifier

Input voltage bass control circuit at pin 16 (r.m.s. value)				
at Δf = ± 27 kHz	$V_{i(rms)}$	typ.	215	mV
Bass control	see graph, Fig. 5			
Input impedance	$\lvert Z_{14-3} \rvert$	typ.	500	kΩ
Treble control	see graph, Fig. 6			
Input impedance	$\lvert Z_{11-3} \rvert$	typ.	500	kΩ
Control voltages for flat frequency characteristic	V_{11-3}	typ.	3,2	V
	V_{14-3}	typ.	3,2	V
Volume control	see graph, Fig. 7			
Input current at V_{8-3} = 4 V	I_8	typ.	40	μA
Physiological volume control (bass and treble compensation)	see graph, Fig. 8			
Voltage gain of audio part				
f = 1 kHz; V_{11-3} = 3,2 V; V_{14-3} = 3,2 V; V_{8-3} = 4 V	G_v	typ.	4	dB
D.C. volume control range		>	−75	dB
Weighted signal-to-noise ratio				
$V_{i(rms)}$ = 215 mV; −24 dB volume control (notes 1 and 2)		typ.	56	dB
Total harmonic distortion at output				
f = 1 kHz; $V_{i(rms)}$ = 215 mV				
(related to max. output; note 2) at:				
0 dB	d_{tot}	typ.	0,2	%
−20 dB	d_{tot}	typ.	0,4	%

Notes
1. Specified according to DIN 45405; weighted noise (peak value).
2. Measured at flat-tone control characteristics.



Input signal: f_o = 5,5 MHz
for f.m.: Δf = ± 27 kHz; f_m = 70 Hz
for a.m.: m = 0,3; f_m = 1 kHz

Fig. 4 Test set-up.

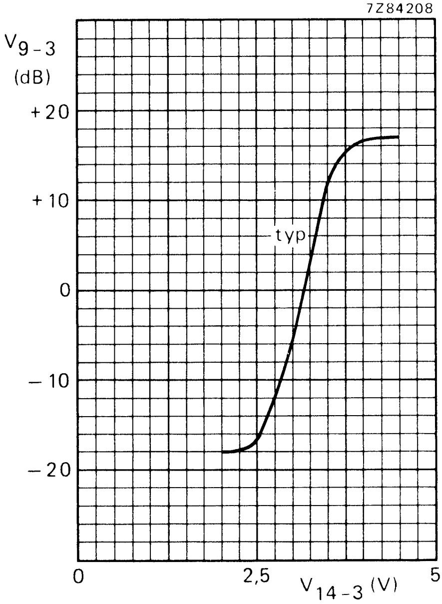


Fig. 5 Bass control curve; f = 40 Hz; $V_{11\text{-}3}$ = 3,2 V; $V_{8\text{-}3}$ = 4 V.

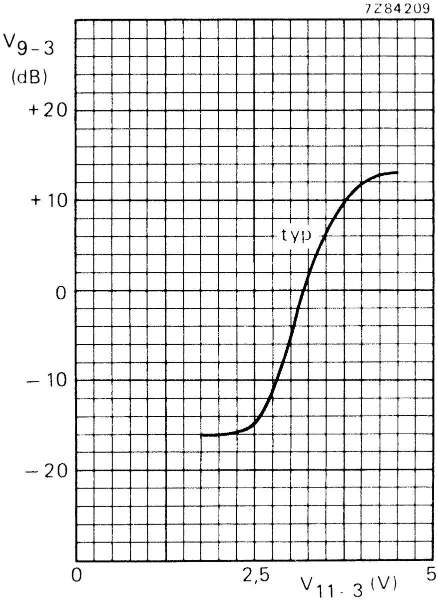
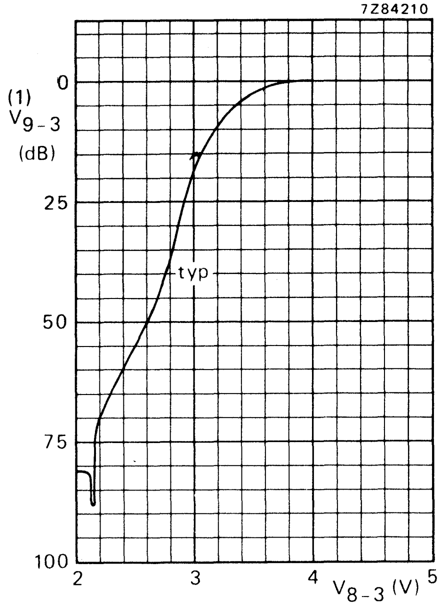
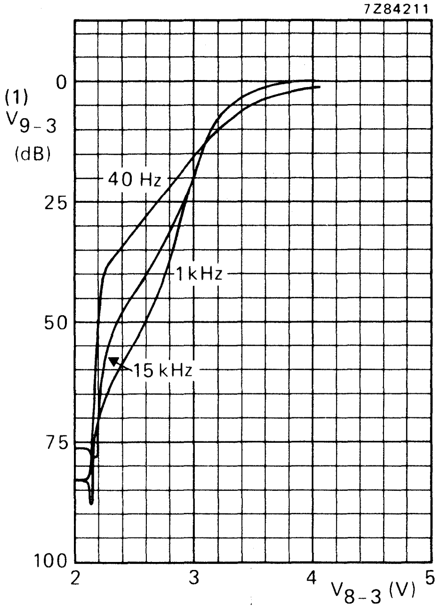


Fig. 6 Treble control curve; f = 15 kHz; $V_{14\text{-}3}$ = 3,2 V; $V_{8\text{-}3}$ = 4 V.





(1) This is actually the a.f. output voltage as shown in Fig. 9.

Fig. 7 Volume control curve; f = 1 kHz. $V_{14\text{-}3}$ = 3,2 V; $V_{11\text{-}3}$ = 3,2 V.

Fig. 8 Physiological volume control curves (typical values); $V_{14\text{-}3}$ = 3,2 V; $V_{11\text{-}3}$ = 3,2 V.

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1.	Limiter input.
2.	The decoupling capacitor for the internal limiter feedback is connected to this pin.
3.	Negative supply (ground).
4.	Limiter output for external feedback to pin 1.
5 and 6.	External tank circuit (demodulator reference signal).
7.	Demodulator output.
8.	D.C. volume control.
9 and 10.	External circuit for physiological volume control.
11.	D.C. treble control.
12.	External capacitor for treble control.
13.	Positive supply.
14.	D.C. bass control.
15 and 16.	External circuit for bass control.

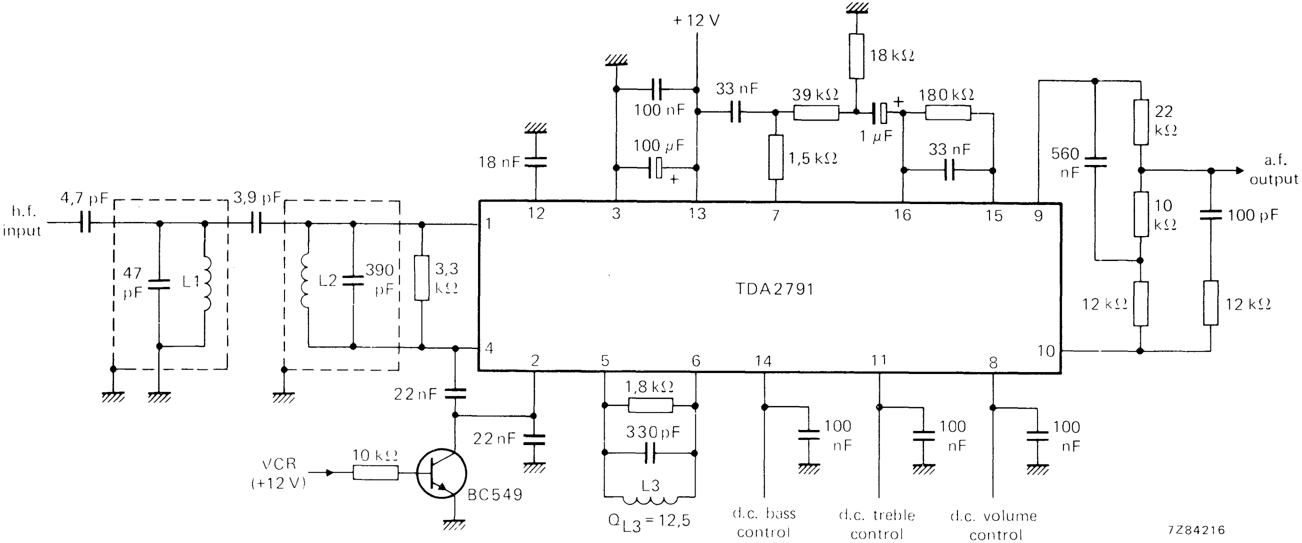


Fig. 9 Application circuit diagram.

TV STEREO/DUAL SOUND IDENTIFICATION DECODER

The TDA2795 is a monolithic integrated circuit for stereo/dual sound in television receivers.

The circuit incorporates the following functions:

- Controlled pilot signal amplifier.
- Envelope demodulator.
- Two separate signal paths for processing the identification frequencies: operational amplifier for active filter, integral evaluation circuit with TTL compatible 'open collector' outputs.
- Stereo indicator driver.

QUICK REFERENCE DATA

Supply voltage	V_S	typ.	12	V
Supply current	I_S	typ.	8	mA
Nominal input voltage at f = 54,6875 kHz	V_i	typ.	10	mV
Input impedance	$\|Z_i\|$	$\geqslant$	500	kΩ
Operational amplifier				
open loop voltage gain at 200 Hz	G_o	$\geqslant$	78	dB
input resistance	R_i	$\geqslant$	1	MΩ
output resistance	R_o	$\leqslant$	3,5	kΩ
Supply voltage range	V_S		10,8 to 13,2	V
Operating ambient temperature range	T_{amb}		−20 to +70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102DS).

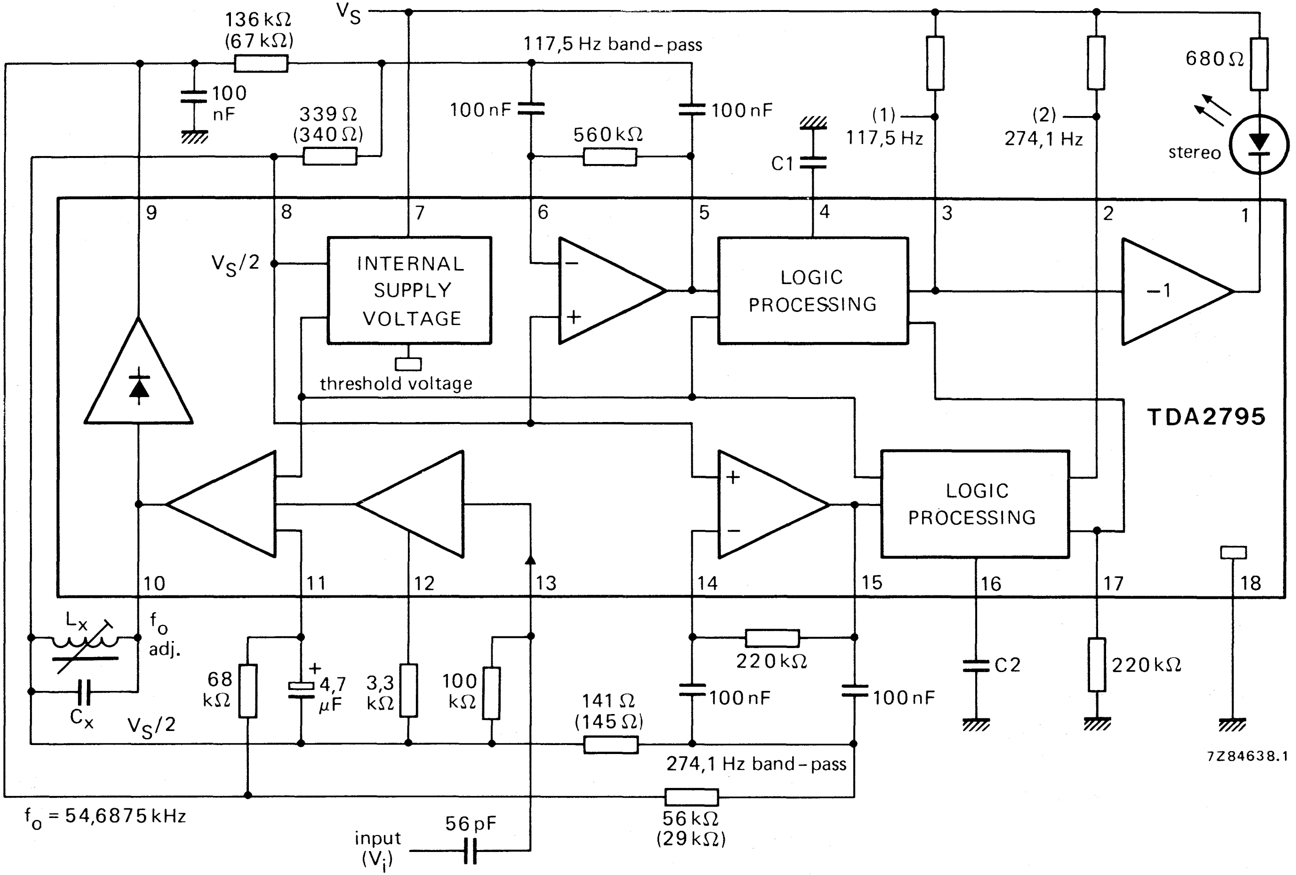


Fig. 1 Block diagram; C1 and C2 values 22 to 150 nF (dependent on switching time); values given in parenthesis are for G = 4 at 117,5/274,1 Hz; C_x = 3,3 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_{7\text{-}18} = V_S$	max.	15	V
Signal input (pin 13)	$V_{13\text{-}18}$	max.	V_S	V
	$-V_{13\text{-}18}$	max.	0,5	V
Switch outputs (pins 1, 2 and 3)	$V_{1\text{-}18}$	max.	18	V
	I_1	max.	50	mA
	$V_{2;\,3\text{-}18}$	max.	15	V
	$I_{2;3}$	max.	5	mA
	$-V_{1;\,2;\,3\text{-}18}$	max.	0,5	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−25 to	+ 125	°C
Operating ambient temperature range	T_{amb}	−20 to	+ 70	°C

CHARACTERISTICS

V_S = 12 V; T_{amb} = 25 °C, unless otherwise specified; measured in Fig. 1, at V_i = 10 mV; f = 54,6875 kHz amplitude modulated with f_{m1} = 117,5 Hz or f_{m2} = 274,1 Hz; $m_1 = m_2$ = 50%.

Supply voltage range	V_S	10,8 to	13,2	V
Supply current	I_S	typ. $\leqslant$	8 12	mA mA

Pilot signal amplifier and envelope demodulator

Maximum input voltage (peak-to-peak value)	$V_{i(p\text{-}p)}$	typ.	2	V
Input impedance	$\|Z_{13\text{-}18}\|$	$\geqslant$	500	kΩ
Voltage gain ($V_{9\text{-}18}/V_{13\text{-}18}$) at V_i = 1 mV	$G_{v9\text{-}13}$	typ.	42	dB
Start of control at V_i	see Fig. 3			
Control range	ΔG_v	$\geqslant$	40	dB
Controlled output voltage (r.m.s. value) (pin 9)	$V_{o(rms)}$	typ.	550	mV

Operational amplifiers

Input bias current (pins 6 and 14)	$\pm I_6;\ \pm I_{14}$	$\leqslant$	70	nA
Open loop voltage gain at f = 200 Hz	G_o	$\geqslant$	78	dB
Available output current (pins 5 and 15)	$\pm I_5;\ \pm I_{15}$	$\geqslant$	1,5	mA
Output resistance (pins 5 and 15)	R_o	typ. $\leqslant$	2 3,5	kΩ kΩ
Allowable load capacitance	C_L	$\leqslant$	30	pF
Output offset voltage at $R_{5\text{-}6}$ = 560 kΩ	$\pm V_{o5\text{-}8}$	$\leqslant$	70	mV

CHARACTERISTICS (continued)

Evaluation circuitry

Switch-on threshold voltage (pins 5 and 15)	$V_5; V_{15}$	typ.	1,0 V
Switch hysteresis	$\frac{V_{5on}}{V_{5off}} = \frac{V_{15on}}{V_{15off}}$	typ.	3,8 ± 0,5 dB
Switch outputs (pins 2 and 3)			
allowable output current	$I_3; I_2$	⩽	2 mA
saturation voltage at $I_3 = I_2 = 1,5$ mA	$V_{3;2\text{-}18sat}$	⩽	0,35 V
leakage voltage at $I_3 = I_2 \leqslant 5\ \mu$A	$V_{3;2\text{-}18}$	⩽	15 V
Indicator driver (pin 1)			
allowable output current	I_1	⩽	40 mA
saturation voltage at $I_1 = 20$ mA	$V_{1\text{-}18sat}$	⩽	0,8 V
leakage voltage at $I_1 < 10\ \mu$A	$V_{1\text{-}18}$	⩽	18 V

Internal reference voltage

Reference voltage (pin 8)	$V_{8\text{-}18}$	typ.	6 V
Available output current (pin 8)	$-I_8$	⩾	2 mA
	$+I_8$	⩾	0,6 mA

Reference current source

Reference voltage (pin 17)	$V_{17\text{-}18}$	typ.	5,3 V
Internal bias resistor	R_{i17}	typ.	5 kΩ
Allowable load resistor (pin 17)	R_L		180 to 270 kΩ

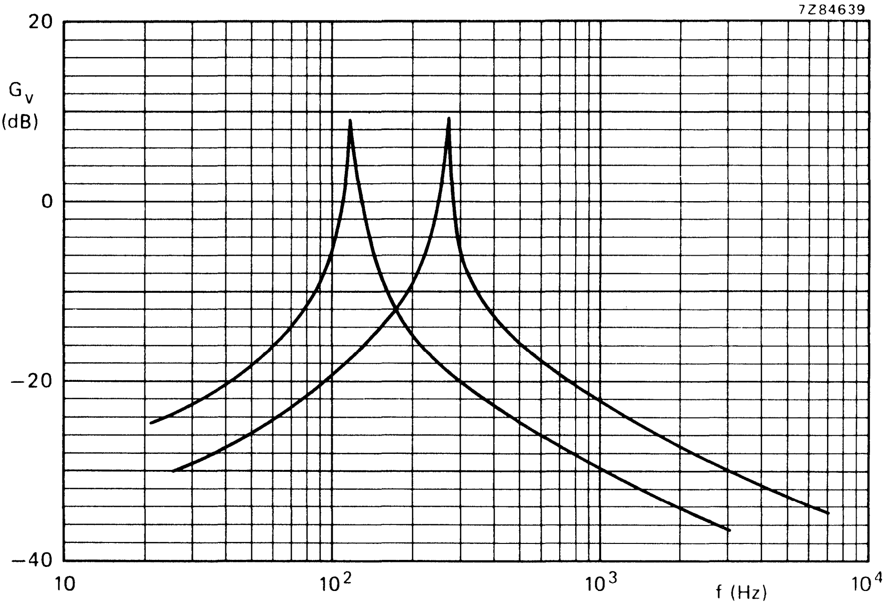


Fig. 2 Band-pass curves for 117,5 Hz and 274,1 Hz.

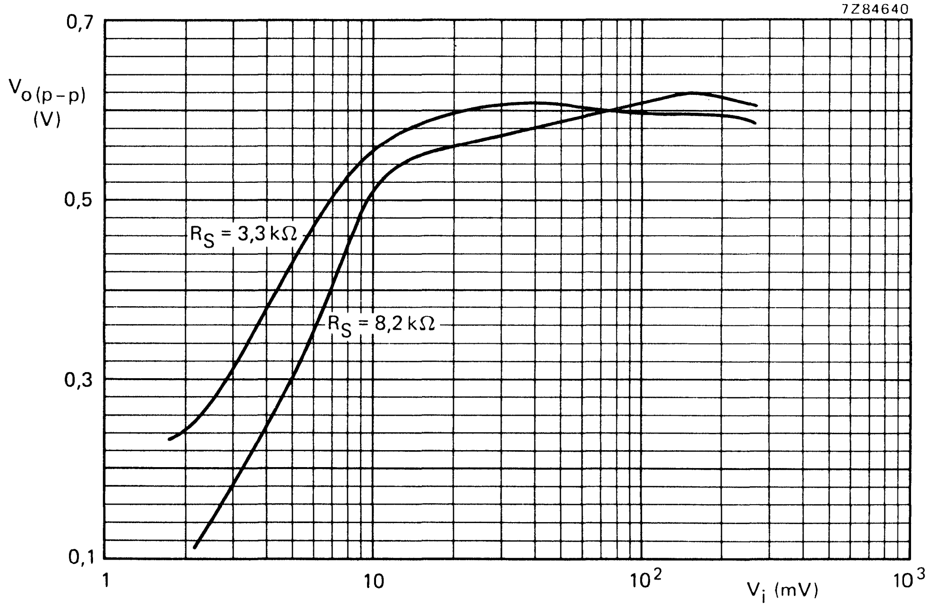


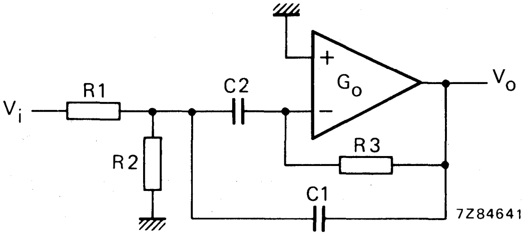
Fig. 3 Controlled output voltage as a function of the input signal (Q_o = 80); pilot frequency f_o = 54,6875 kHz; R_S is source resistance.

GENERAL FILTER CALCULATIONS

1. Gain

Amplifier conditions: $G_o >> G_V$ and $G_o >> 2 \cdot Q^2$

$$G_V = -\frac{\dfrac{p}{R1 \cdot C1}}{p^2 + p\dfrac{C1 + C2}{R3 \cdot C1 \cdot C2} + \dfrac{R1 + R2}{R1 \cdot R2 \cdot R3 \cdot C1 \cdot C2}}, \text{ in which: } p = j\omega;\ G_V = \frac{V_o}{V_i}$$



2. Resonance frequency

$$\omega_r = \frac{1}{\sqrt{\dfrac{R1 \cdot R2}{R1 + R2} \cdot R3 \cdot C1 \cdot C2}}$$

3. Gain at $\omega = \omega_r$

$$-G_{Vr} = \frac{C2}{C1 + C2} \cdot \frac{R3}{R1}$$

4. Quality

$$Q = \frac{\sqrt{C1 \cdot C2}}{C1 + C2} \cdot \sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$$

5. Recommended components

C1 and C2: 5% MKC (metallized polycarbonate film capacitor)
R1, R2 and R3: 2% MR (metal film resistor)

or:

C1 and C2: 5% MKT (metallized polyester film capacitor)
R1, R2 and R3: 2% CR (carbon film resistor)

INFRARED RECEIVER

The TDA3047 is for infrared reception with low power consumption.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	5	V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1	mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2\text{-}15(p\text{-}p)}$	0,02 to 200		mV
Output signal (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$	typ.	4,5	V

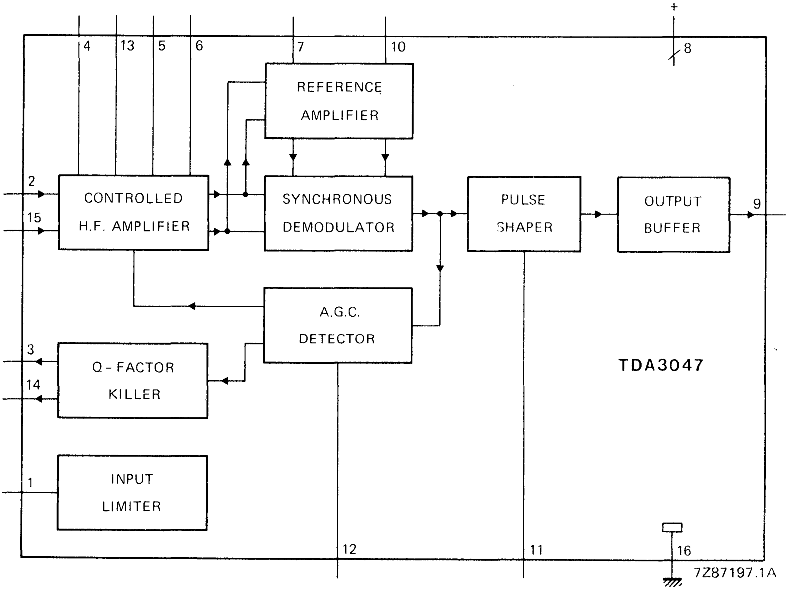


Fig. 1 Block diagram of TDA3047.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of $> 75\ \mu A$ with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *high.*

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	max.	13,2	V
Output current pulse shaper (pin 11)	I_{11}	max.	10	mA
Voltages between pins*				
pins 2 and 15	$V_{2\text{-}15}$	max.	4,5	V
pins 4 and 13	$V_{4\text{-}13}$	max.	4,5	V
pins 5 and 6	$V_{5\text{-}6}$	max.	4,5	V
pins 7 and 10	$V_{7\text{-}10}$	max.	4,5	V
pins 9 and 11	$V_{9\text{-}11}$	max.	4,5	V
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 125	°C

---

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8\text{-}16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8\text{-}16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2\text{-}15(p\text{-}p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2\text{-}15(p\text{-}p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2\text{-}15(p\text{-}p)}$	0,02	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0{,}5$ μA) (peak-to-peak value)	$V_{2\text{-}15(p\text{-}p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3 =$ max.) (peak-to-peak value)	$V_{2\text{-}15(p\text{-}p)}$	28	–	–	mV
Q-killing range		see Fig. 2			
Inputs					
Input voltage (pin 2)	$V_{2\text{-}16}$	2,25	2,45	2,65	V
Input voltage (pin 15)	$V_{15\text{-}16}$	2,25	2,45	2,65	V
Input resistance (pin 2)	$R_{2\text{-}15}$	10	15	20	kΩ
Input capacitance (pin 2)	$C_{2\text{-}15}$	–	3	–	pF
Input limiting (pin 1) at $I_1 =$ 3 mA	$V_{1\text{-}16}$	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9\text{-}8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	$V_{9\text{-}16}$	–	0,1	0,5	V
Output current; output voltage *high*					
at $V_{9\text{-}16} = 4{,}5$ V	$-I_9$	75	120	–	μA
at $V_{9\text{-}16} = 3{,}0$ V	$-I_9$	75	130	–	μA
at $V_{9\text{-}16} = 1{,}0$ V	$-I_9$	75	140	–	μA
Output current; output voltage *low* at $V_{9\text{-}16} = 0{,}5$ V	I_9	75	120	–	μA
Output resistance between pins 7 and 10	$R_{7\text{-}10}$	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *high*; $-I_9 = 75$ μA.
2. Voltage pin 9 remains *low*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*)	$V_{11\text{-}16}$	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*)	$V_{11\text{-}16}$	3,4	3,55	3,7	V
Hysteresis of trigger levels	$\Delta V_{11\text{-}16}$	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,3	4,7	6,1	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at $V_{12\text{-}16} = 2$ V	$-I_3$	2,5	7,5	15	μA
Output current (pin 14) at $V_{12\text{-}16} = 2$ V	$-I_{14}$	2,5	7,5	15	μA

DEVELOPMENT SAMPLE DATA

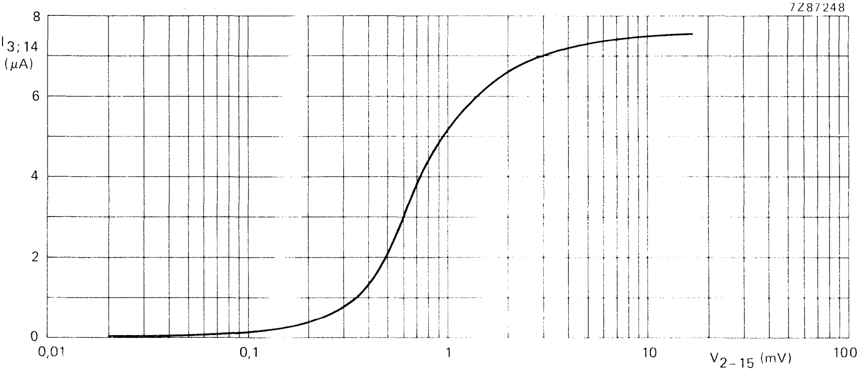
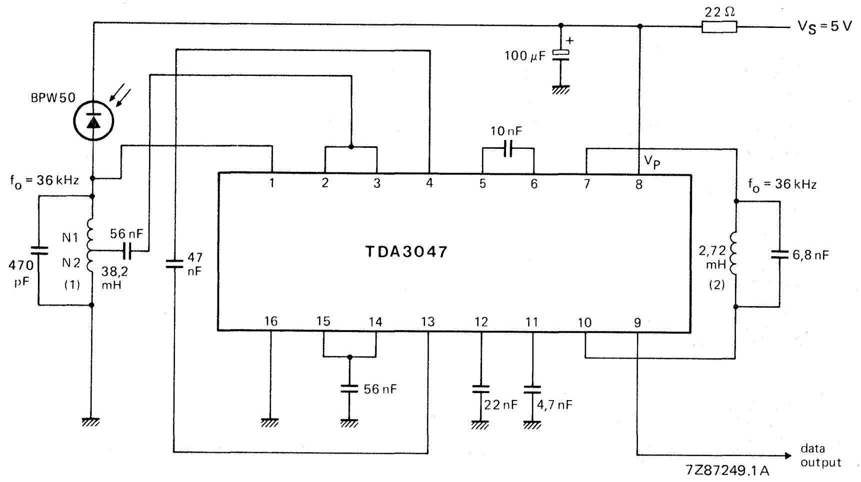


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage ($V_{2\text{-}15}$); $I_{3,\,14}$ is measured to ground, $V_{2\text{-}15(p\text{-}p)}$ is a symmetrical square wave. Measured in Fig. 4; $V_P = 5$ V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3047.

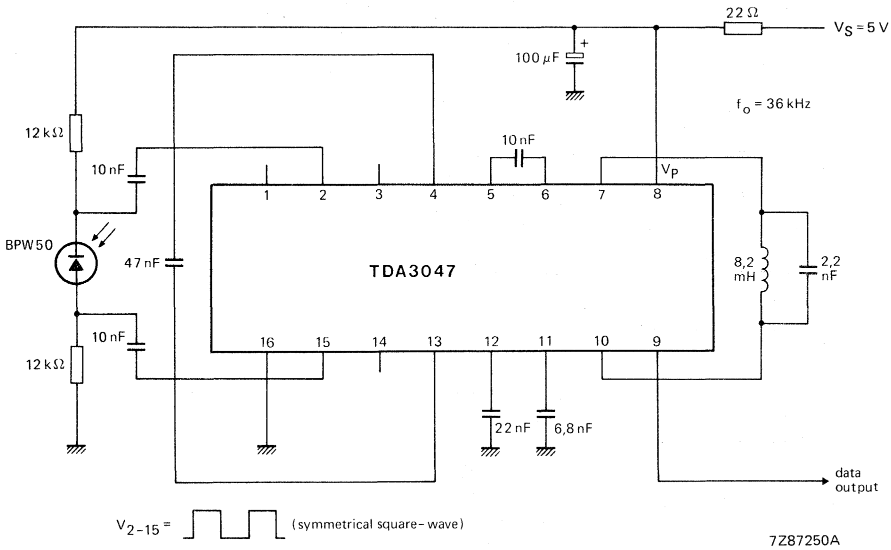


Fig. 4 Wide-band receiver with TDA3047.
For better sensitivity both 12 kΩ resistors may have a higher value.

INFRARED RECEIVER

The TDA3048 is for infrared reception with low power consumption.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	5	V
Supply current (pin 8)	$I_P = I_8$	typ.	2,1	mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2\text{-}15(p\text{-}p)}$	0,02 to	200	mV
Output signal (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$	typ.	4,5	V

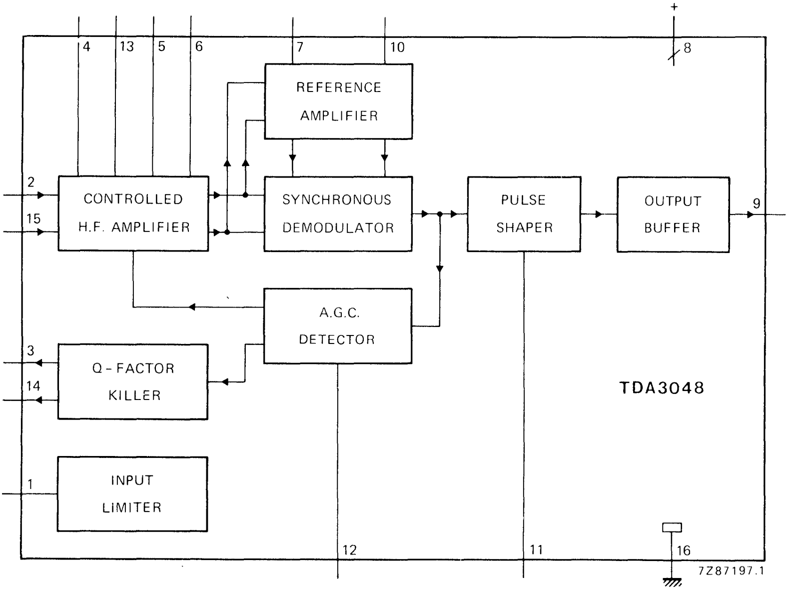


Fig. 1 Block diagram of TDA3048.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of > 75 μA with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *low.*

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0,7 V. Limiting is 0,9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	max.	13,2	V
Output current pulse shaper (pin 11)	I_{11}	max.	10	mA
Voltages between pins*				
pins 2 and 15	$V_{2\text{-}15}$	max.	4,5	V
pins 4 and 13	$V_{4\text{-}13}$	max.	4,5	V
pins 5 and 6	$V_{5\text{-}6}$	max.	4,5	V
pins 7 and 10	$V_{7\text{-}10}$	max.	4,5	V
pins 9 and 11	$V_{9\text{-}11}$	max.	4,5	V
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 125	°C

DEVELOPMENT SAMPLE DATA

---

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8\text{-}16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8\text{-}16}$	4,65	5,0	5,35	V
Supply current	$I_P = I_8$	1,2	2,1	3,0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2\text{-}15(p\text{-}p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2\text{-}15(p\text{-}p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2\text{-}15(p\text{-}p)}$	0,02	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0,5$ μA) (peak-to-peak value)	$V_{2\text{-}15(p\text{-}p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3 =$ max.) (peak-to-peak value)	$V_{2\text{-}15(p\text{-}p)}$	28	–	–	mV
Q-killing range			see Fig. 2		
Inputs					
Input voltage (pin 2)	$V_{2\text{-}16}$	2,25	2,45	2,65	V
Input voltage (pin 15)	$V_{15\text{-}16}$	2,25	2,45	2,65	V
Input resistance (pin 2)	$R_{2\text{-}15}$	10	15	20	kΩ
Input capacitance (pin 2)	$C_{2\text{-}15}$	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	$V_{1\text{-}16}$	–	0,8	0,9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9\text{-}8}$	–	0,1	0,5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	$V_{9\text{-}16}$	–	0,1	0,5	V
Output current; output voltage *low*					
$-V_{9\text{-}8} = 4,5$ V	I_9	75	120	–	μA
$-V_{9\text{-}8} = 3,0$ V	I_9	75	130	–	μA
$-V_{9\text{-}8} = 1,0$ V	I_9	75	140	–	μA
Output current; output voltage *high* $-V_{9\text{-}8} = 0,5$ V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	$R_{7\text{-}10}$	3,1	4,7	6,2	kΩ

Notes

1. Voltage pin 9 is *low*; $I_9 = 75$ μA.
2. Voltage pin 9 remains *high*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*	$V_{11\text{-}16}$	3,75	3,9	4,05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*	$V_{11\text{-}16}$	3,4	3,55	3,7	V
Hysteresis of trigger levels	$\Delta V_{11\text{-}16}$	0,25	0,35	0,45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3,3	4,7	6,1	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at $V_{12\text{-}16} = 2$ V	$-I_3$	2,5	7,5	15	μA
Output current (pin 14) at $V_{12\text{-}16} = 2$ V	$-I_{14}$	2,5	7,5	15	μA

DEVELOPMENT SAMPLE DATA

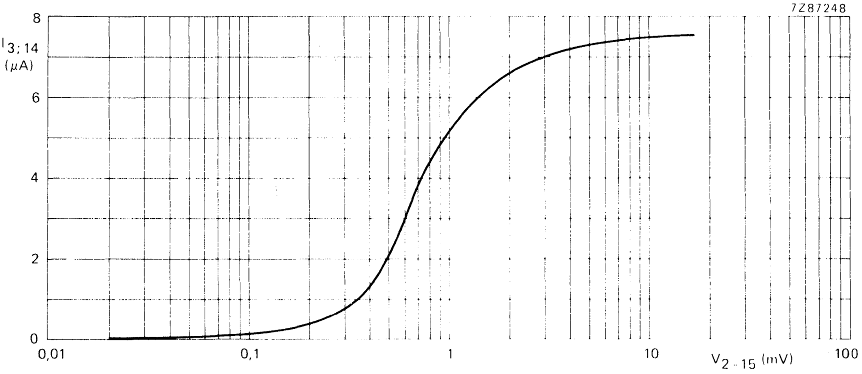
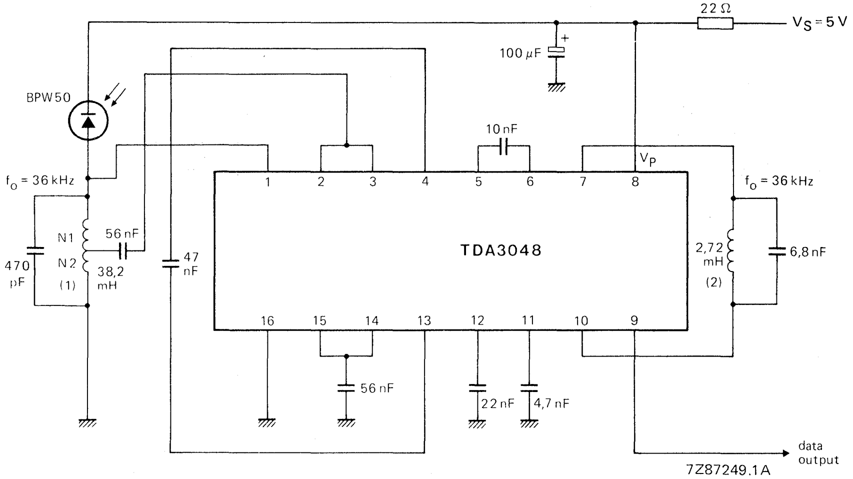


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage ($V_{2\text{-}15}$); $I_{3,14}$ is measured to ground, $V_{2\text{-}15(p\text{-}p)}$ is a symmetrical square wave. Measured in Fig. 4; $V_P = 5$ V.

APPLICATION INFORMATION



(1) N1 = 3,21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3048.

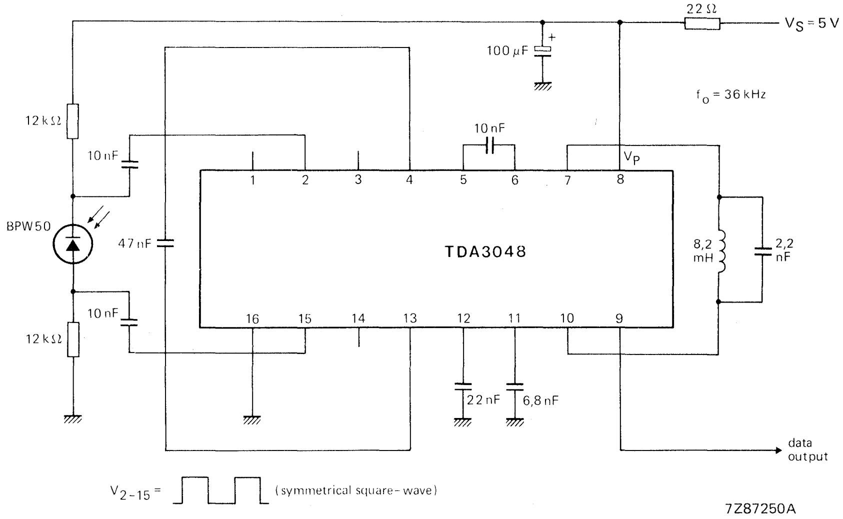


Fig. 4 Wide-band receiver with TDA3048.
For better sensitivity both 12 kΩ resistors may have a higher value.

VIDEO CONTROL COMBINATION

The TDA3500 is a monolithic integrated circuit performing the control functions in a PAL/SECAM decoder which additionally comprises the integrated circuits TDA3510 (PAL decoder) and/or TDA3520 (SECAM decoder).

The required input signals are: luminance and colour difference –(R-Y) and –(B-Y), while linear RGB signals can be inserted from an external source.

RGB signals are provided at the output to drive the video output stages.

The TDA3500 has the following features:

- capacitive coupling of the input signals
- linear saturation control
- (G-Y) and RGB matrix
- insertion possibility of linear RGB signals, e.g. video text, video games, picture-in-picture, camera or slide-scanner
- equal black level for inserted and matrixed signals by clamping
- 3 identical channels for the RGB signals
- linear contrast and brightness control, operating on both the inserted and matrixed RGB signals
- horizontal and vertical blanking (black and ultra-black respectively) and black-level clamping obtained via a 3-level sandcastle pulse
- differential amplifiers with feedback-inputs for stabilization of the RGB output stages
- 3 d.c. gain controls for the RGB output signals (white point adjustment)

QUICK REFERENCE DATA

Supply voltage	$V_{6\text{-}24}$	typ.	12	V
Supply current	I_6	typ.	100	mA
Luminance input signal (peak-to-peak value)	$V_{15\text{-}24(p\text{-}p)}$	typ.	0,45	V
Luminance input resistance	$R_{15\text{-}24}$	typ.	12	kΩ
Colour difference input signals (peak-to-peak values)				
–(B-Y)	$V_{18\text{-}24(p\text{-}p)}$	typ.	1,33	V
–(R-Y)	$V_{17\text{-}24(p\text{-}p)}$	typ.	1,05	V
Inserted RGB signals (peak-to-peak values)	$V_{12,13,14\text{-}24(p\text{-}p)}$	typ.	1	V
Three-level sandcastle pulse detector	$V_{10\text{-}24}$	typ.	2,5/4,5/8,0	V
Control voltage ranges				
brightness	$V_{20\text{-}24}$		1 to 3	V
contrast	$V_{19\text{-}24}$		2 to 4	V
saturation	$V_{16\text{-}24}$		2,1 to 4	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

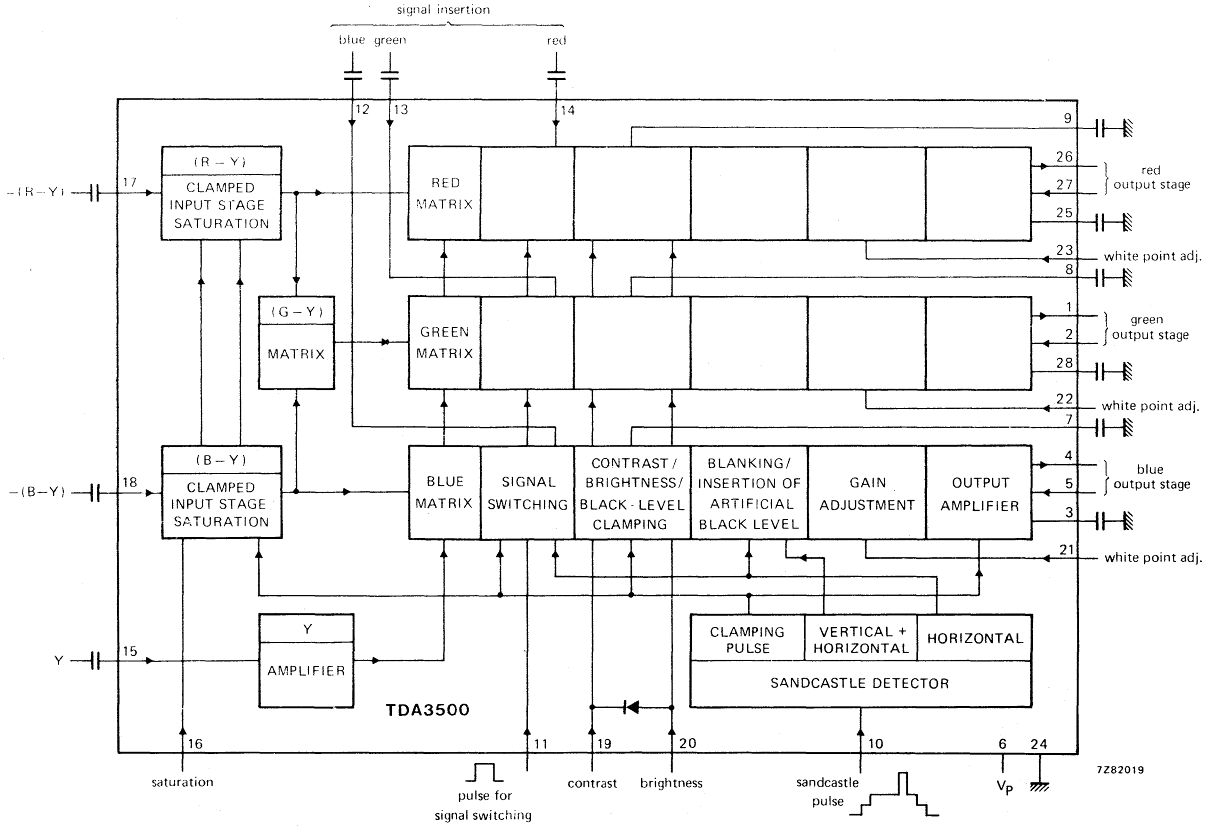


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			min.	max.	
Supply voltage	$V_P = V_{6-24}$		–	13,2	V
Voltages with respect to pin 24					
pins 1,4,26	$V_{1,4,26-24}$		½V_P	$V_P + 1$	V
pins 2,5,27	$V_{2,5,27-24}$		0	V_P	V
pin 10	V_{10-24}		0	V_P	V
pin 11	V_{11-24}		–0,5	3	V
pins 16,19,20	$V_{16,19,20-24}$		0	½V_P	V
pins 21,22,23	$V_{21,22,23-24}$		0	V_P	V
pins 3,25,28; 7,8,9; 12,13,14; 15,17,18	no external d.c. voltage				
Current at pin 20	I_{20}	max.		5	mA
Total power dissipation	P_{tot}	max.		1,7	W
Storage temperature	T_{stg}			–25 to + 125	°C
Operating ambient temperature	T_{amb}			–20 to + 70	°C

CHARACTERISTICS

Supply voltage range	V_P		10,8 to 13,2	V

The following characteristics are measured in Fig. 2; $V_P = 12$ V; $T_{amb} = 25$ °C; $V_{18-24(p-p)} = 1{,}33$ V; $V_{17-24(p-p)} = 1{,}05$ V; $V_{15-24(p-p)} = 0{,}45$ V; $V_{12,13,14-24(p-p)} = 1$ V; unless otherwise specified

Current consumption	I_6	typ.	100	mA
Colour difference inputs				
–(B-Y) input signal (peak-to-peak value)*	$V_{18-24(p-p)}$		1,33	V
–(R-Y) input signal (peak-to-peak value)*	$V_{17-24(p-p)}$		1,05	V
Internal resistance of colour difference sources		<	200	Ω
Input resistance	$R_{17,18-24}$	>	100	kΩ
Internal d.c. voltage due to clamping	$V_{17,18-24}$	typ.	4,2	V
Saturation control				
control voltage range for a change of saturation from –20 dB to + 6 dB	V_{16-24}		2,1 to 4	V
control voltage for attenuation > 40 dB	V_{16-24}	<	1,8	V
nominal saturation (6 dB below max.)	V_{16-24}	typ.	3	V
input current	I_{16}	<	20	µA

---

* For saturated colour bar with 75% of maximum amplitude.

CHARACTERISTICS (continued)

(G-Y) matrix

Matrixed according the equation $V_{(G-Y)} = -0,51\ V_{(R-Y)} - 0,19\ V_{(B-Y)}$

Luminance amplifier

Input signal (peak-to-peak)	$V_{15\text{-}24(p\text{-}p)}$		0,45	V
Input resistance	$R_{15\text{-}24}$	typ.	12	kΩ
Internal d.c. voltage	$V_{15\text{-}24}$	typ.	2,7	V

RGB channels

Signal switching input voltage for insertion				
on level	$V_{11\text{-}24}$		0,9 to 1,5	V
off level	$V_{11\text{-}24}$		−0,5 to 0,3	V
Input current	I_{11}		−100 to + 200	μA
Signal insertion				
external RGB input signal (peak-to-peak value)*	$V_{12,13,14\text{-}24(p\text{-}p)}$		1	V
internal d.c. voltage due to clamping	$V_{12,13,14\text{-}24}$	typ.	3,5	V
input current	$I_{12,13,14}$	<	5	μA
Contrast control				
control voltage range for a change of contrast from −17 dB to + 3 dB	$V_{19\text{-}24}$		2 to 4	V
nominal contrast (3 dB below max.)	$V_{19\text{-}24}$	typ.	3,4	V
control voltage for −6 dB	$V_{19\text{-}24}$	typ.	2,7	V
input current	I_{19}	<	10	μA
Brightness control				
control voltage range	$V_{20\text{-}24}$		1 to 3	V
nominal brightness voltage	$V_{20\text{-}24}$		2	V
input current	I_{20}	<	10	μA
control voltage for nominal black level which equals the inserted artificial black level	$V_{20\text{-}24}$	typ.	2	V
change of black level in the control range related to the nominal luminance signal (black-white)		typ.	± 50	%
Internal signal limiting **				
signal limiting for nominal luminance (black to white = 100%)				
black		typ.	−25	%
white		typ.	125	%

---

* During the clamping time (see sandcastle detector Fig. 1), the inserted RGB signals are clamped to the same black level as the internal RGB signals. For proper clamping, the internal resistance of the external signal sources should be < 200 Ω.

** Brightness, contrast and saturation control in nominal position.

White point adjustment

A.C. voltage gain*				
at $V_{21,22,23\text{-}24} = 6$ V			100	%
at $V_{21,22,23\text{-}24} = 0$ V		$<$	60	%
at $V_{21,22,23\text{-}24} = 12$ V		$>$	140	%
Input resistance	$R_{21,22,23\text{-}24}$	typ.	20	kΩ

Differential output amplifier

Feedback inputs (pins 2, 5, 27)				
d.c. voltage during clamping	$V_{2,5,27\text{-}24}$	typ.	6	V
voltage difference between the feedback inputs	ΔV	$<$	80	mV
input resistance	$R_{2,5,27\text{-}24}$	$>$	100	kΩ
Output amplifiers (pins 1, 4, 26)				
transconductance	$\frac{\Delta I_1}{\Delta V_{2\text{-}24}} = \frac{\Delta I_4}{\Delta V_{5\text{-}24}} = \frac{\Delta I_{26}}{\Delta V_{27\text{-}24}}$	typ.	20	mA/V
integrated load resistance	$R_{1,4,26\text{-}24}$	typ.	610	Ω
output current (peak value) at $V_{1,4,26\text{-}24} = 8{,}2$ V	$\pm I_{1,4,26\,m}$	typ.	5	mA

Gain data

At nominal contrast, saturation and white point adjustment

Voltage gain between Y-input (pin 15) and feedback inputs (pins 2, 5, 27)	$G_{2,5,27\text{-}15}$	typ.	10	dB
Frequency response (0 to 5 MHz)	$d_{2,5,27\text{-}15}$	$<$	3	dB
Voltage gain between colour difference inputs (pins 17 and 18) and feedback inputs (pins 5 and 27)	$G_{5\text{-}18} = G_{27\text{-}17}$	typ.	0	dB
Frequency response (0 to 2 MHz)	$d_{5\text{-}18} = d_{27\text{-}17}$	$<$	3	dB
Voltage gain between signal display inputs (pins 12, 13, 14) and feedback inputs (pins 2, 5, 27)	$G_{2\text{-}13} = G_{5\text{-}12} = G_{27\text{-}14}$	$<$	0	dB
Frequency response (0 to 5 MHz)	$d_{2\text{-}13} = d_{5\text{-}12} = d_{27\text{-}14}$	$<$	3	dB

---

* With input pins 21, 22 and 23 not connected an internal bias voltage of 6 V is supplied.

CHARACTERISTICS (continued)

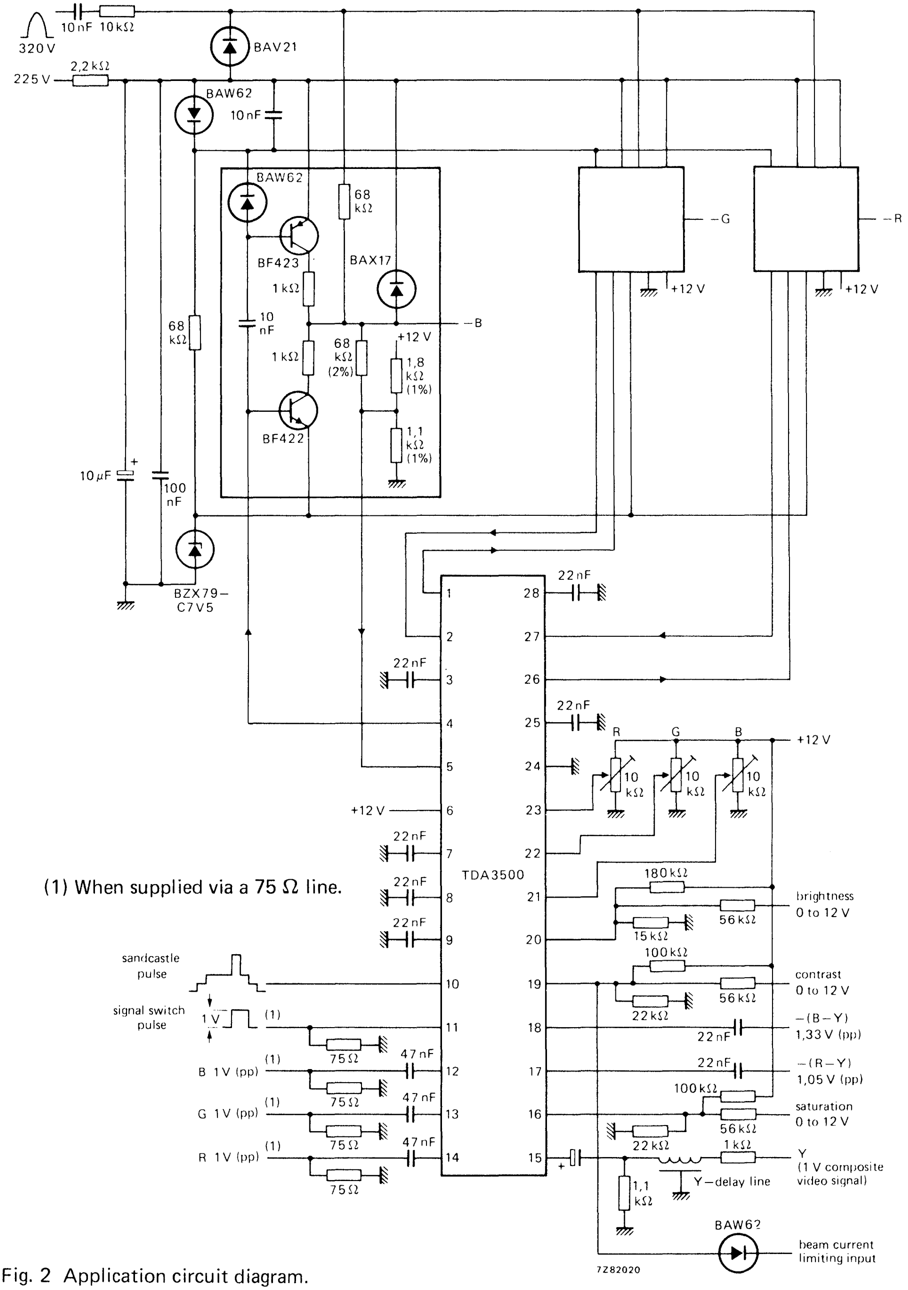
Sandcastle detector

There are 3 internal thresholds (proportional to V_P) the following amplitudes are required for separating the various pulses:

horizontal and vertical blanking pulses (note 1)	$V_{10\text{-}24}$	$>$ $<$	2 V 3 V
horizontal pulse (note 2)	$V_{10\text{-}24}$	$>$ $<$	4 V 5 V
clamping pulse (note 3)	$V_{10\text{-}24}$	$>$	7,5 V
d.c. voltage for artificial black level (note 4) (scan and flyback)	$V_{10\text{-}24}$	$>$	7,5 V
no keying	$V_{10\text{-}24}$	$<$	1 V

Notes

1. Blanking to ultra-black (−20%).
2. Insertion of artificial black level.
3. Pulse duration $> 3{,}5\ \mu s$.
4. This function will also be obtained by leaving pin 10 open.



(1) When supplied via a 75 Ω line.

Fig. 2 Application circuit diagram.

VIDEO CONTROL COMBINATION

The TDA3501 is a monolithic integrated circuit performing the control functions in a PAL/SECAM decoder which additionally comprises the integrated circuits TDA3510 (PAL decoder) and/or TDA3520 (SECAM decoder).

The required input signals are: luminance and colour difference −(R-Y) and −(B-Y), while linear RGB signals can be inserted from an external source.

RGB signals are provided at the output to drive the video output stages.

The TDA3501 has the following features:

- capacitive coupling of the input signals
- linear saturation control
- (G-Y) and RGB matrix
- insertion possibility of linear RGB signals, e.g. video text, video games, picture-in-picture, camera or slide-scanner
- equal black level for inserted and matrixed signals by clamping
- 3 identical channels for the RGB signals
- linear contrast and brightness control, operating on both the inserted and matrixed RGB signals
- horizontal and vertical blanking (black and ultra-black respectively) and black-level clamping obtained via a 3-level sandcastle pulse
- differential amplifiers with feedback-inputs for stabilization of the RGB output stages
- 2 d.c. gain controls for the green and blue output signals (white point adjustment)
- beam current limiting possibility

QUICK REFERENCE DATA

Supply voltage	$V_{6\text{-}24}$	typ.	12	V
Supply current	I_6	typ.	100	mA
Luminance input signal (peak-to-peak value)	$V_{15\text{-}24(p\text{-}p)}$	typ.	0,45	V
Luminance input resistance	$R_{15\text{-}24}$	typ.	12	kΩ
Colour difference input signals (peak-to-peak values)				
−(B-Y)	$V_{18\text{-}24(p\text{-}p)}$	typ.	1,33	V
−(R-Y)	$V_{17\text{-}24(p\text{-}p)}$	typ.	1,05	V
Inserted RGB signals (peak-to-peak values)	$V_{12,13,14\text{-}24(p\text{-}p)}$	typ.	1	V
Three-level sandcastle pulse detector	$V_{10\text{-}24}$	typ.	2,5/4,5/8,0	V
Control voltage ranges				
brightness	$V_{20\text{-}24}$		1 to 3	V
contrast	$V_{19\text{-}24}$		2 to 4	V
saturation	$V_{16\text{-}24}$		2,1 to 4	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

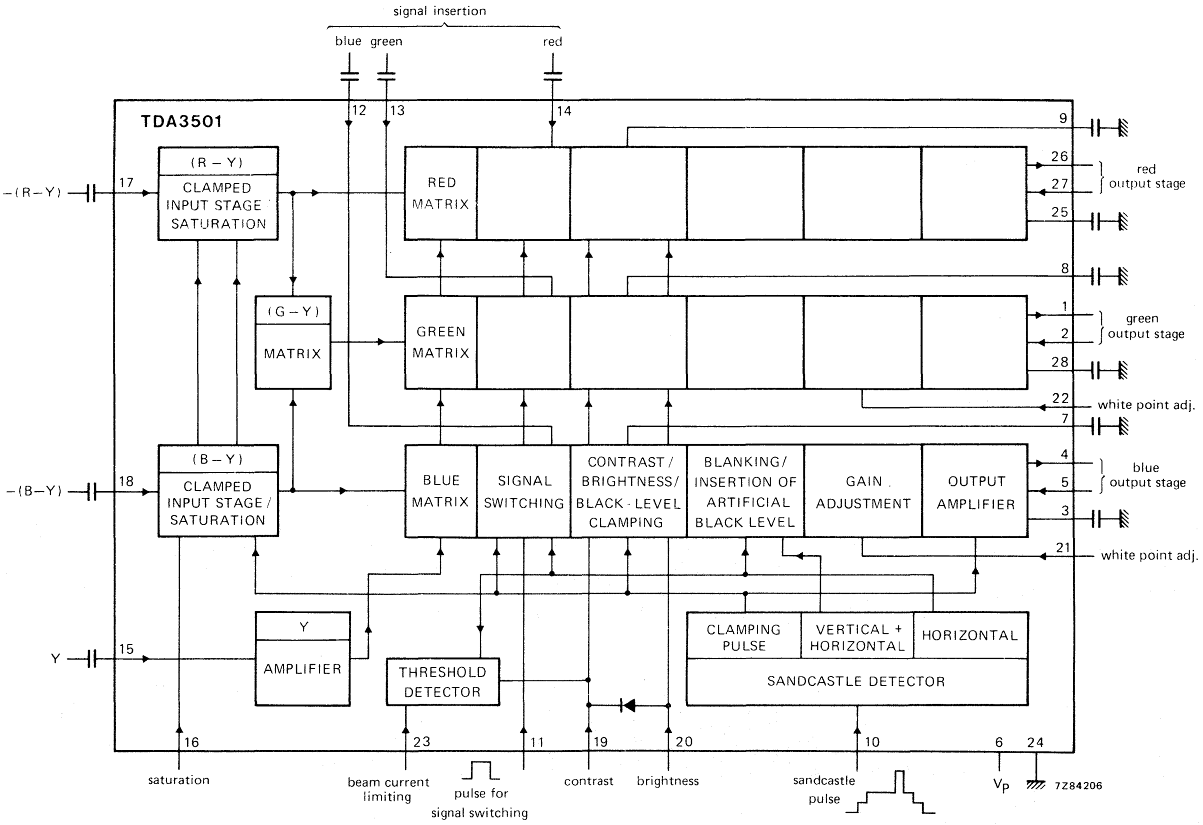


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			min.	max.	
Supply voltage	$V_P = V_{6\text{-}24}$		–	13,2	V
Voltages with respect to pin 24					
pins 1,4,26	$V_{1,4,26\text{-}24}$		½V_P	$V_P + 1$	V
pins 2,5,27	$V_{2,5,27\text{-}24}$		0	V_P	V
pin 10	$V_{10\text{-}24}$		0	V_P	V
pin 11	$V_{11\text{-}24}$		−0,5	3	V
pins 16,19,20	$V_{16,19,20\text{-}24}$		0	½V_P	V
pins 21,22	$V_{21,22\text{-}24}$		0	V_P	V
pin 23	$V_{23\text{-}24}$		0	V_P	V
pins 3,25,28; 7,8,9; 12,13,14; 15,17,18	no external d.c. voltage				
Current at pin 20	I_{20}	max.		5	mA
Total power dissipation	P_{tot}	max.		1,7	W
Storage temperature	T_{stg}			−25 to + 125	°C
Operating ambient temperature	T_{amb}			−20 to + 70	°C

CHARACTERISTICS

Supply voltage range	V_P		10,8 to 13,2	V

The following characteristics are measured in Fig. 2; $V_P = 12$ V; $T_{amb} = 25$ °C; $V_{18\text{-}24(p\text{-}p)} = 1,33$ V; $V_{17\text{-}24(p\text{-}p)} = 1,05$ V; $V_{15\text{-}24(p\text{-}p)} = 0,45$ V; $V_{12,13,14\text{-}24(p\text{-}p)} = 1$ V; unless otherwise specified

Current consumption	I_6	typ.	100	mA
Colour difference inputs				
−(B-Y) input signal (peak-to-peak value)*	$V_{18\text{-}24(p\text{-}p)}$		1,33	V
−(R-Y) input signal (peak-to-peak value)*	$V_{17\text{-}24(p\text{-}p)}$		1,05	V
Internal resistance of colour difference sources		<	200	Ω
Input resistance	$R_{17,18\text{-}24}$	>	100	kΩ
Internal d.c. voltage due to clamping	$V_{17,18\text{-}24}$	typ.	4,2	V
Saturation control				
control voltage range for a change of saturation from −20 dB to + 6 dB	$V_{16\text{-}24}$		2,1 to 4	V
control voltage for attenuation > 40 dB	$V_{16\text{-}24}$	<	1,8	V
nominal saturation (6 dB below max.)	$V_{16\text{-}24}$	typ.	3	V
input current	I_{16}	<	20	μA

---

* For saturated colour bar with 75% of maximum amplitude.

CHARACTERISTICS (continued)

(G-Y) matrix

Matrixed according the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$

Luminance amplifier

Input signal (peak-to-peak)	$V_{15-24(p-p)}$		0,45	V
Input resistance	R_{15-24}	typ.	12	kΩ
Internal d.c. voltage	V_{15-24}	typ.	2,7	V

RGB channels

Signal switching input voltage for insertion				
on level	V_{11-24}		0,9 to 1,5	V
off level	V_{11-24}		−0,5 to + 0,3	V
Input current	I_{11}		−100 to + 200	μA
Signal insertion				
external RGB input signal (peak-to-peak value)*	$V_{12,13,14-24(p-p)}$		1	V
internal d.c. voltage due to clamping	$V_{12,13,14-24}$	typ.	3,5	V
input current	$I_{12,13,14}$	<	5	μA
Contrast control				
control voltage range for a change of contrast from −17 dB to + 3 dB	V_{19-24}		2 to 4	V
nominal contrast (3 dB below max.)	V_{19-24}	typ.	3,4	V
control voltage for −6 dB	V_{19-24}	typ.	2,7	V
input current at $V_{23-24} \geqslant 6$ V	I_{19}	<	2,5	μA
Beam current limiting				
internal d.c. voltage	V_{23-24}	typ.	6	V
input resistance	R_{23-24}	typ.	10	kΩ
input current contrast control				
$V_{23-24} = 5{,}8$ V	I_{19}	typ.	0,7	mA
$V_{23-24} = 5{,}7$ V	I_{19}	typ.	10	mA
$V_{23-24} = 5{,}6$ V	I_{19}	typ.	16	mA
Brightness control				
control voltage range	V_{20-24}		1 to 3	V
nominal brightness voltage	V_{20-24}		2	V
input current	I_{20}	<	10	μA
control voltage for nominal black level which equals the inserted artificial black level	V_{20-24}	typ.	2	V
change of black level in the control range related to the nominal luminance signal (black-white)		typ.	± 50	%

---

* During the clamping time (see sandcastle detector Fig. 1), the inserted RGB signals are clamped to the same black level as the internal RGB signals. For proper clamping, the internal resistance of the external signal sources should be < 200 Ω.

Internal signal limiting*				
signal limiting for nominal luminance (black to white = 100%)				
black		typ.	−25	%
white		typ.	125	%

White point adjustment

A.C. voltage gain **				
at $V_{21,22-24} = 6$ V			100	%
at $V_{21,22-24} = 0$ V		$<$	60	%
at $V_{21,22-24} = 12$ V		$>$	140	%
Input resistance	$R_{21,22-24}$	typ.	20	kΩ

Differential output amplifier

Feedback inputs (pins 2,5,27)				
d.c. voltage during clamping	$V_{2,5,27-24}$		5,79 to 5,95	V
voltage difference between the feedback inputs	ΔV	$<$	80	mV
input resistance	$R_{2,5,27-24}$	$>$	100	kΩ
Output amplifiers (pins 1,4,26)				
transconductance	$\frac{\Delta I_1}{\Delta V_{2-24}} = \frac{\Delta I_4}{\Delta V_{5-24}} = \frac{\Delta I_{26}}{\Delta V_{27-24}}$	typ.	20	mA/V
integrated load resistance	$R_{1,4,26-24}$	typ.	610	Ω
output current (peak value) at $V_{1,4,26-24} = 8{,}2$ V	$\pm I_{1,4,26\,m}$	typ.	5	mA

Gain data

At nominal contrast, saturation and white point adjustment				
Voltage gain between Y-input (pin 15) and feedback inputs (pins 2,5,27)	$G_{2,5,27-15}$	typ.	10	dB
Frequency response (0 to 5 MHz)	$d_{2,5,27-15}$	$<$	3	dB
Voltage gain between colour difference inputs (pins 17 and 18) and feedback inputs (pin 5 and 27)	$G_{5-18} = G_{27-17}$	typ.	0	dB
Frequency response (0 to 2 MHz)	$d_{5-18} = d_{27-17}$	$<$	3	dB
Voltage gain between signal display inputs (pins 12,13,14) and feedback inputs (pins 2,5,27)	$G_{2-13} = G_{5-12} = G_{27-14}$	typ.	0	dB
Frequency response (0 to 5 MHz)	$d_{2-13} = d_{5-12} = d_{27-14}$	$<$	3	dB

---

* Brightness, contrast and saturation control in nominal position.

** With input pins 21 and 22 not connected an internal bias voltage of 6 V is supplied.

CHARACTERISTICS (continued)

Sandcastle detector

There are 3 internal thresholds (proportional to V_P) the following amplitudes are required for separating the various pulses:

horizontal and vertical blanking pulses (note 1)	$V_{10\text{-}24}$	$>$ $<$	2 V 3 V
horizontal pulse (note 2)	$V_{10\text{-}24}$	$>$ $<$	4 V 5 V
clamping pulse (note 3)	$V_{10\text{-}24}$	$>$	7,5 V
d.c. voltage for artificial black level (note 4) (scan and flyback)	$V_{10\text{-}24}$	$>$	7,5 V
no keying	$V_{10\text{-}24}$	$<$	1 V
Input current	$-I_{10}$	$<$	100 μA

Notes

1. Blanking to ultra-black (−20%).
2. Insertion of artificial black level.
3. Pulse duration $> 3{,}5$ μs.
4. This function will also be obtained by leaving pin 10 open.

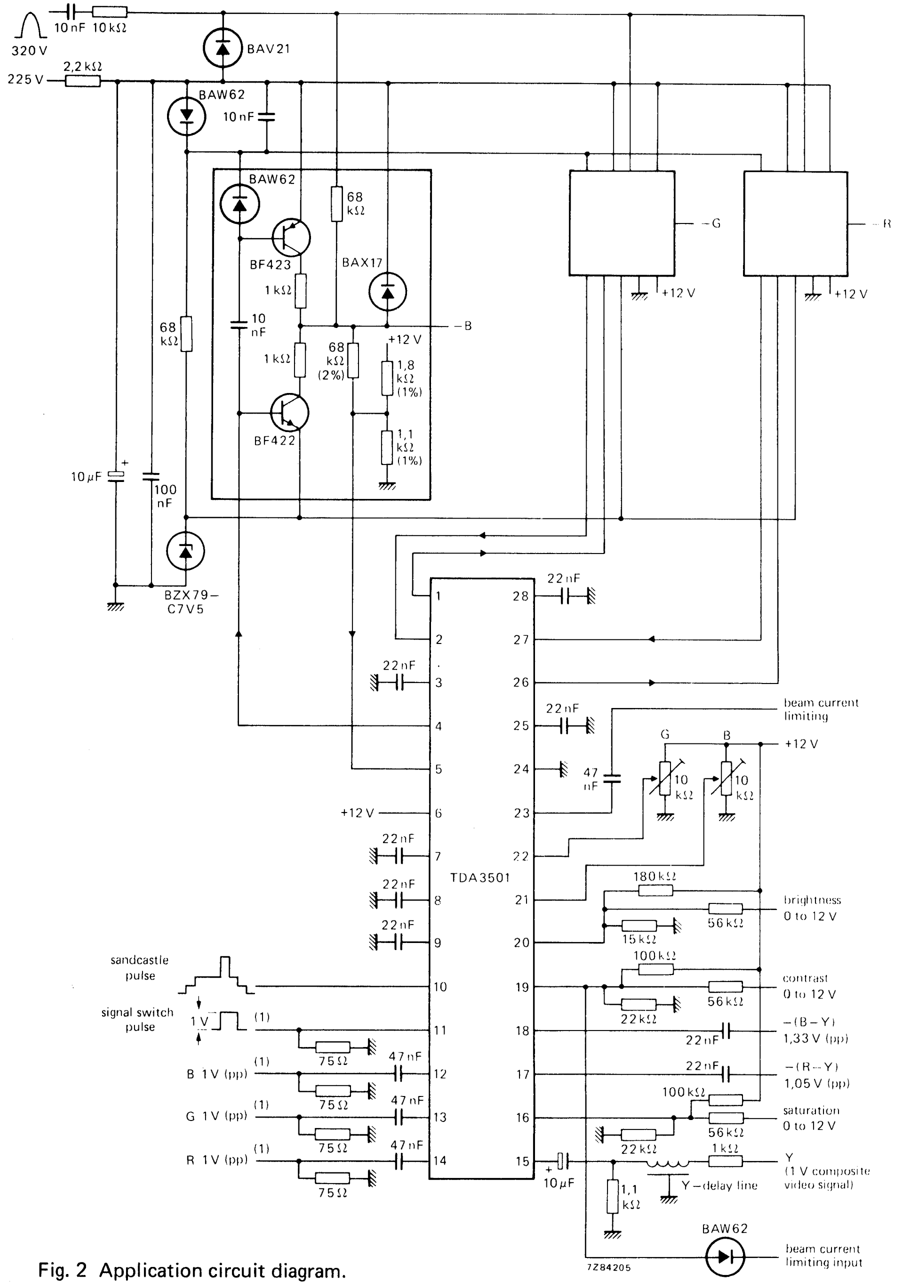


Fig. 2 Application circuit diagram.

VIDEO CONTROL COMBINATION CIRCUIT

with automatic cut-off control

The TDA3505 performs the control functions in a PAL/SECAM decoder, which also comprises the TDA3510 (PAL decoder) and/or TDA3530 (SECAM decoder).

The required input signals are: luminance and colour difference –(R-Y) and –(B-Y), while linear RGB signals can be inserted from external sources. RGB output signals are delivered for driving the video output stages. This circuit provides automatic cut-off control of the picture tube. The TDA3505 has the following features:

- capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- linear saturation control in the colour difference stages
- (G-Y) and RGB matrix
- linear transmission of inserted signals
- equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- linear contrast and brightness control, operating on both the inserted and matrixed RGB signals
- peak beam current limiting input
- horizontal and vertical blanking and clamping of the three input signals obtained via a 3-level sandcastle pulse
- d.c. gain controls for each of the RGB output signals (white point adjustment)
- emitter-follower outputs for driving the RGB output stages
- input for automatic cut-off control of the picture tube
- compensation for leakage current of the picture tube

QUICK REFERENCE DATA

Supply voltage	$V_{6\text{-}24} = V_P$	typ.	12	V
Supply current	$I_6 = I_P$	typ.	85	mA
Composite video input signal (peak-to-peak value)	$V_{15\text{-}24(p\text{-}p)}$	typ.	0,45	V
Input resistance	$R_{15\text{-}24}$	>	100	kΩ
Colour difference input signals (peak-to-peak values)				
–(B-Y)	$V_{18\text{-}24(p\text{-}p)}$	typ.	1,33	V
–(R-Y)	$V_{17\text{-}24(p\text{-}p)}$	typ.	1,05	V
Inserted RGB signals (black-to-white values)	$V_{12,13,14\text{-}24(p\text{-}p)}$	typ.	1	V
Three-level sandcastle pulse (required input voltage)	$V_{10\text{-}24}$	typ.	2,5/4,5/8,0	V
Control voltage ranges				
brightness	$V_{20\text{-}24}$		1,0 to 3,0	V
contrast	$V_{19\text{-}24}$		2,0 to 4,3	V
saturation	$V_{16\text{-}24}$		2,0 to 4,3	V

PACKAGE OUTLINE 28-lead DIL; plastic (SOT-117).

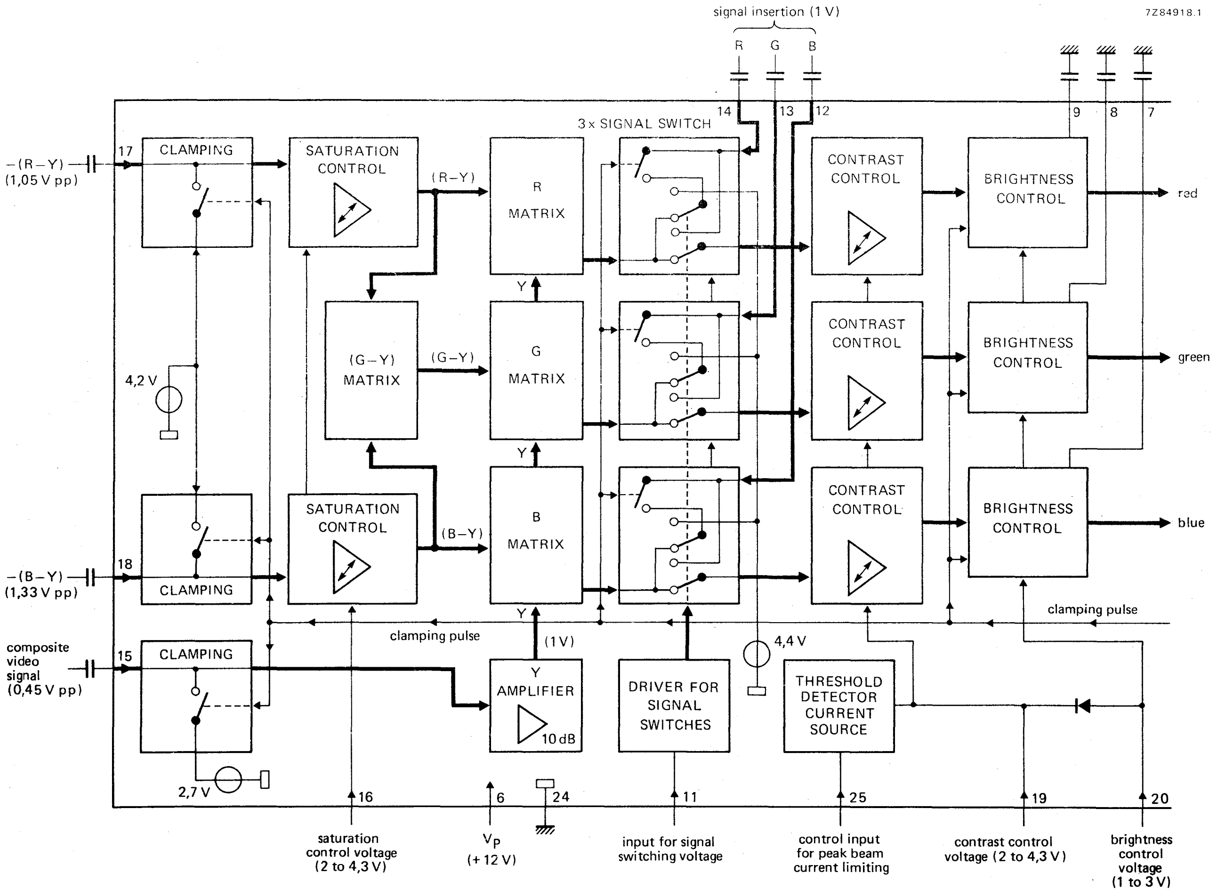


Fig. 1a Part of block diagram; continued in Fig. 1b.

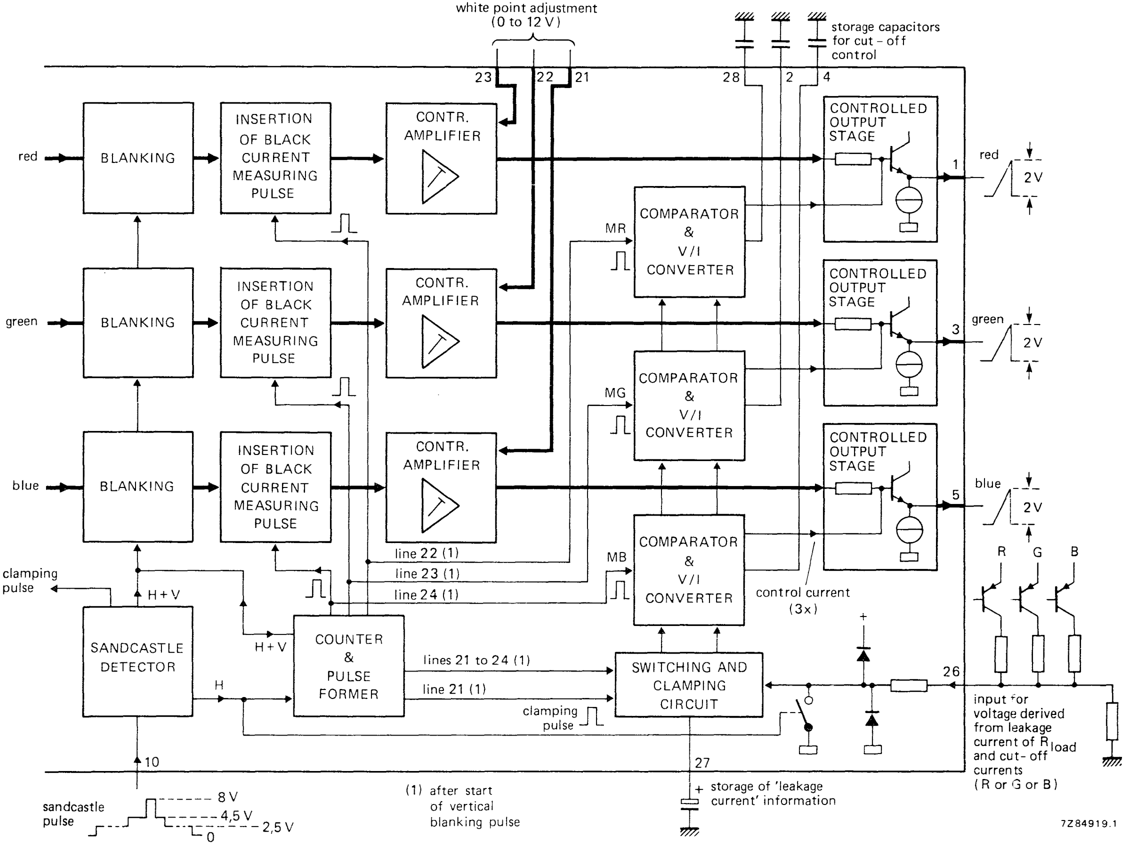


Fig. 1b Part of block diagram; continued from Fig. 1a.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		min.	max.	
Supply voltage	$V_P = V_{6-24}$	—	13,2	V
Voltages with respect to pin 24				
pin 26	V_{26-24}	0	V_P	V
pin 25	V_{25-24}	0	V_P	V
pin 10	V_{10-24}	0	V_P	V
pin 11	V_{11-24}	−0,5	3	V
pins 16, 19, 20	$V_{16,19,20-24}$	0	0,5 V_P	V
pins 21, 22, 23	$V_{21,22,23-24}$	0	V_P	V
pins 1, 3, 5; 2, 4, 28; 7, 8, 9; 12, 13, 14; 15, 17, 18; 27	no external d.c. voltage			
Currents				
pins 1, 3, 5	$-I_{1, 3, 5}$	max.	3	mA
pin 19	I_{19}	max.	10	mA
pin 20	I_{20}	max.	5	mA
pin 25	$-I_{25}$	max.	5	mA
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to +125	°C
Operating ambient temperature range	T_{amb}		−20 to +70	°C

CHARACTERISTICS

Supply voltage range	$V_P = V_{6-24}$		10,8 to 13,2	V

The following characteristics are measured in a circuit similar to Fig. 2; $V_P = 12$ V; $T_{amb} = 25$ °C; $V_{18-24(p-p)} = 1,33$ V; $V_{17-24(p-p)} = 1,05$ V; $V_{15-24(p-p)} = 0,45$ V; $V_{12,13,14-24(p-p)} = 1$ V; unless otherwise specified

Supply current	$I_6 = I_P$	typ.	85	mA
Colour difference inputs				
−(B-Y) input signal at pin 18 (peak-to-peak value)*	$V_{18-24(p-p)}$	typ.	1,33	V
−(R-Y) input signal at pin 17 (peak-to-peak value)*	$V_{17-24(p-p)}$	typ.	1,05	V
Input current during scanning	$I_{17, 18}$	<	1	µA
Input resistance	$R_{17,18-24}$	>	100	kΩ
Internal d.c. voltage due to clamping	$V_{17,18-24}$	typ.	4,2	V
Saturation control at pin 16				
control voltage range for a change of saturation from −20 dB to +6 dB	V_{16-24}		2,1 to 4,3	V
control voltage for attenuation > 40 dB	V_{16-24}	<	1,8	V
nominal saturation (6 dB below max.)	V_{16-24}	typ.	3,1	V
input current	I_{16}	<	20	µA

* For saturated colour bar with 75% of maximum amplitude.

(G-Y) matrix

Matrixed according to the equation $V_{(G\text{-}Y)} = -0{,}51\,V_{(R\text{-}Y)} - 0{,}19\,V_{(B\text{-}Y)}$

Luminance amplifier (pin 15)

Composite video input signal (peak-to-peak value)	$V_{15\text{-}24(p\text{-}p)}$	typ.	0,45	V
Input resistance	$R_{15\text{-}24}$	$>$	100	kΩ
Internal d.c. voltage	$V_{15\text{-}24}$	typ.	2,7	V
Input current during scanning	I_{15}	$<$	1	μA

RGB channels

Signal switching input voltage for insertion (pin 11)				
on level	$V_{11\text{-}24}$		0,9 to 3	V
off level	$V_{11\text{-}24}$	$<$	0,4	V
Input current	I_{11}		−100 to + 200	μA
Signal insertion (pin 12: blue; pin 13: green; pin 14: red)				
external RGB input signal (black-to-white values)	$V_{12,13,14\text{-}24(p\text{-}p)}$	=	1	V
internal d.c. voltage due to clamping*	$V_{12,13,14\text{-}24}$	typ.	4,4	V
input current during scanning	$I_{12,13,14}$	$<$	1	μA
Contrast control (pin 19)				
control voltage range for a change of contrast from −18 dB to + 3 dB	$V_{19\text{-}24}$		2 to 4,3	V
nominal contrast (3 dB below max.)	$V_{19\text{-}24}$	typ.	3,6	V
control voltage for −6 dB	$V_{19\text{-}24}$	typ.	2,8	V
input current at $V_{25\text{-}24} \geq 6$ V	I_{19}	$<$	2	μA
Peak beam current limiting (pin 25)				
internal d.c. bias voltage	$V_{25\text{-}24}$	typ.	5,5	V
input resistance	$R_{25\text{-}24}$	typ.	10	kΩ
input current at contrast control input at $V_{25\text{-}24} = 5{,}1$ V	I_{19}	typ.	17	mA
Brightness control (pin 20)				
control voltage range	$V_{20\text{-}24}$		1 to 3	V
input current	$-I_{20}$	$\leq$	10	μA
control voltage for nominal black level which equals the inserted artificial black level	$V_{20\text{-}24}$	typ.	2	V
change of black level in the control range related to the nominal luminance signal (black-white) for $\Delta V_{20\text{-}24} = 1$ V		typ.	50	%

* $V_{11\text{-}24} < 0{,}4$ V during clamping time: the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
$V_{11\text{-}24} > 0{,}9$ V during clamping time: the black levels of the inserted signals are clamped on an internal d.c. voltage.
Correct clamping of the external RGB signals is only possible when they are synchronous with the sandcastle pulse.

CHARACTERISTICS (continued)

Internal signal limiting				
signal limiting for nominal luminance (black to white = 100%)				
black		typ.	−25	%
white		typ.	120	%

White point adjustment (pin 21: blue; pin 22: green; pin 23: red)

A.C. voltage gain (note 1)				
at $V_{21,22,23\text{-}24}$ = 5,5 V		typ.	100	%
at $V_{21,22,23\text{-}24}$ = 0 V		=	60	%
at $V_{21,22,23\text{-}24}$ = 12 V		=	140	%
Input resistance	$R_{21,22,23\text{-}24}$	typ.	20	kΩ

Emitter-follower outputs (pin 1: red; pin 3: green; pin 5: blue)

At nominal contrast, saturation and white point adjustment

Output voltage (black-to-white signal, positive)	$V_{1,3,5\text{-}24(p\text{-}p)}$	typ.	2	V
Black level without automatic cut-off control ($V_{28,2,4\text{-}24}$ = 10 V)	$V_{1,3,5\text{-}24}$	typ.	6,7	V
Internal current source	I_{source}	typ.	3	mA
Cut-off current control range	$-\Delta V_{1,3,5\text{-}24}$	typ.	4,6	V

Automatic cut-off control (pin 26)

The measurement occurs in the following lines after start of the vertical blanking pulse:
line 21: measurement of leakage current
line 22: measurement of red cut-off current
line 23: measurement of green cut-off current
line 24: measurement of blue cut-off current

Input voltage range	$V_{26\text{-}24}$		0 to + 6,5	V
Voltage difference between cut-off current measurement (note 2) and leakage current measurement (note 3)	$\Delta V_{26\text{-}24}$	typ.	0,7	V

Input 26 switches to ground during horizontal flyback

Notes

1. With input pins 21, 22 and 23 not connected an internal bias voltage of 5,5 V is supplied.
2. Black level of measured channel is nominal; the other two channels are blanked to ultra-black.
3. All three channels blanked to ultra-black.
   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.
   The internal signal blanking continues until the end of the last measurement line.
   The vertical blanking pulse is not allowed to contain more than 34 line pulses otherwise another control cycle begins.

Gain data

At nominal contrast, saturation and white point adjustment

Voltage gain with respect to Y-input (pin 15)	$G_{1,3,5\text{-}15}$	typ.	16 dB
Frequency response (0 to 5 MHz)	$d_{1,3,5\text{-}15}$	$\leqslant$	3 dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)	$G_{5\text{-}18} = G_{1\text{-}17}$	typ.	6 dB
Frequency response (0 to 2 MHz)	$d_{5\text{-}18} = d_{1\text{-}17}$	$\leqslant$	3 dB
Voltage gain of inserted signals	$G_{1\text{-}14} = G_{3\text{-}13} = G_{5\text{-}12}$	typ.	6 dB
Frequency response (0 to 6 MHz)	$d_{1\text{-}14} = d_{3\text{-}13} = d_{5\text{-}12}$	$\leqslant$	3 dB

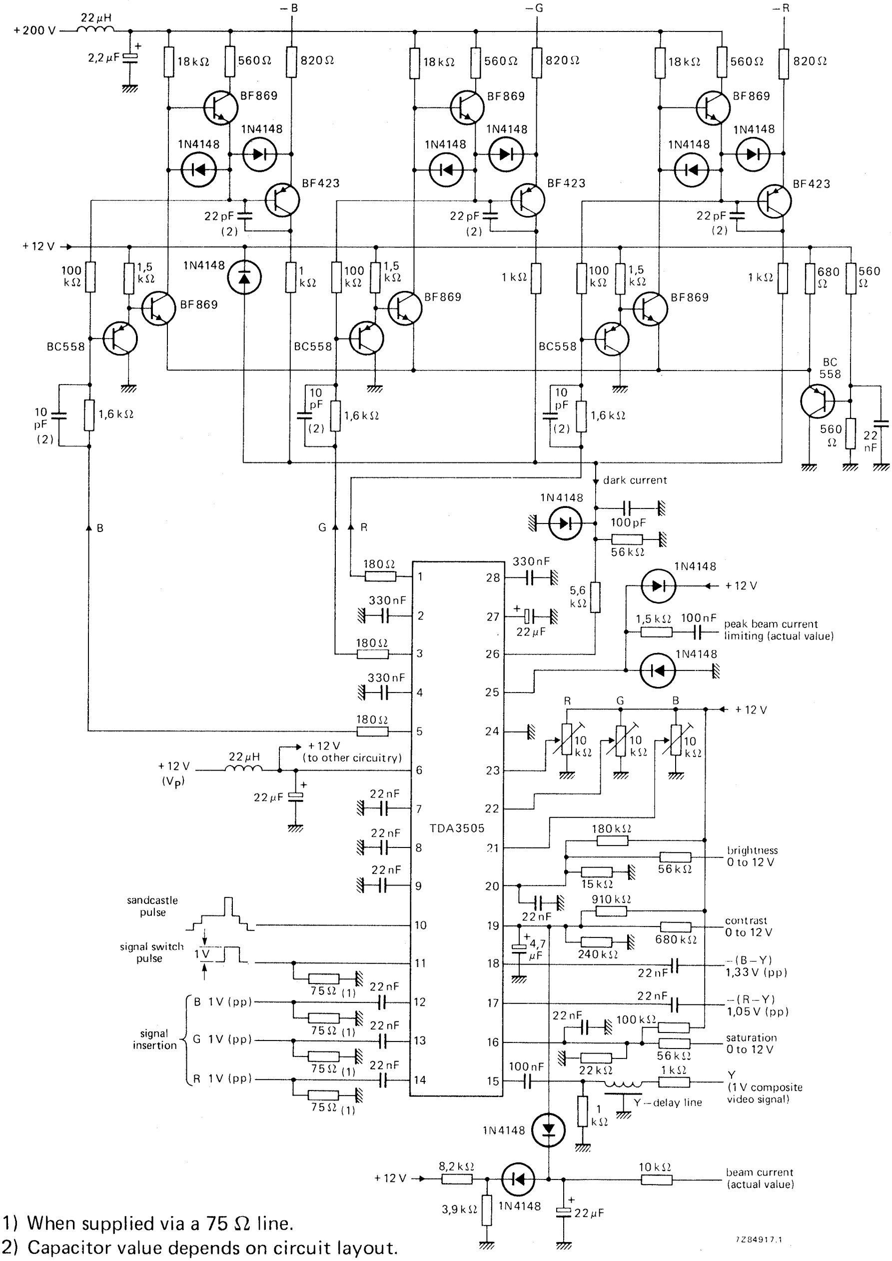
Sandcastle detector (pin 10)

There are 3 internal thresholds (proportional to V_P); note 1. The following amplitudes are required for separating the various pulses:

horizontal and vertical blanking pulses (note 2)	$V_{10\text{-}24}$	> <	2 V 3 V
horizontal pulse	$V_{10\text{-}24}$	> <	4 V 5 V
clamping pulse (note 3)	$V_{10\text{-}24}$	>	7,5 V
d.c. voltage for artificial black level (scan and flyback)	$V_{10\text{-}24}$	>	7,5 V
no keying	$V_{10\text{-}24}$	<	1 V
input current	$-I_{10}$	<	110 μA

Notes

1. The thresholds are for
   horizontal and vertical blanking: $V_{10\text{-}24} = 1{,}5$ V
   horizontal pulse: $V_{10\text{-}24} = 3{,}5$ V
   clamping pulse: $V_{10\text{-}24} = 7{,}0$ V
2. Blanking to ultra-black (−25%).
3. Pulse duration $\geqslant$ 3,5 μs.



(1) When supplied via a 75 Ω line.

(2) Capacitor value depends on circuit layout.

Fig. 2 Typical application circuit diagram using the TDA3505.

PAL DECODER

The TDA3510 is a monolithic integrated colour decoder for the PAL standard.
The circuit incorporates the following functions:

Chrominance part

- Controlled chrominance amplifier
- Chrominance output stage with automatic standard switch for driving the 64 µs delay line
- Blanking circuit for the colour burst signal

Reference voltage and control voltage part

- 8,8 MHz reference oscillator with divider stage to obtain both the 4,4 MHz reference signals
- Gated phase comparison for an optimum noise ratio
- Circuit for obtaining the chrominance control voltage and a reference voltage
- Circuit for generating the colour killer signal and the identification signal

Demodulator part

- Two synchronous demodulators for the (B-Y) and (R-Y) signals
- PAL flip-flop and PAL switch
- Flyback blanking incorporated in the synchronous demodulators
- (R-Y) and (B-Y) signal output stages, which are controlled by the colour killer with switchable d.c. voltage levels

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{9\text{-}24}$	typ.	12	V
Supply current	I_9	typ.	58	mA
Chrominance input signal (peak-to-peak value)	$V_{1\text{-}24(p\text{-}p)}$		10 to 200	mV
Sandcastle pulse				
burst gating level	$V_{20\text{-}24}$	>	7,5	V
blanking level	$V_{20\text{-}24}$	>	1,8	V
Colour difference output signals				
peak-to-peak values				
−(R-Y) signal	$V_{11\text{-}24(p\text{-}p)}$	typ.	1,05 V ± 3	dB
−(B-Y) signal	$V_{10\text{-}24(p\text{-}p)}$	typ.	1,33 V ± 3	dB

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

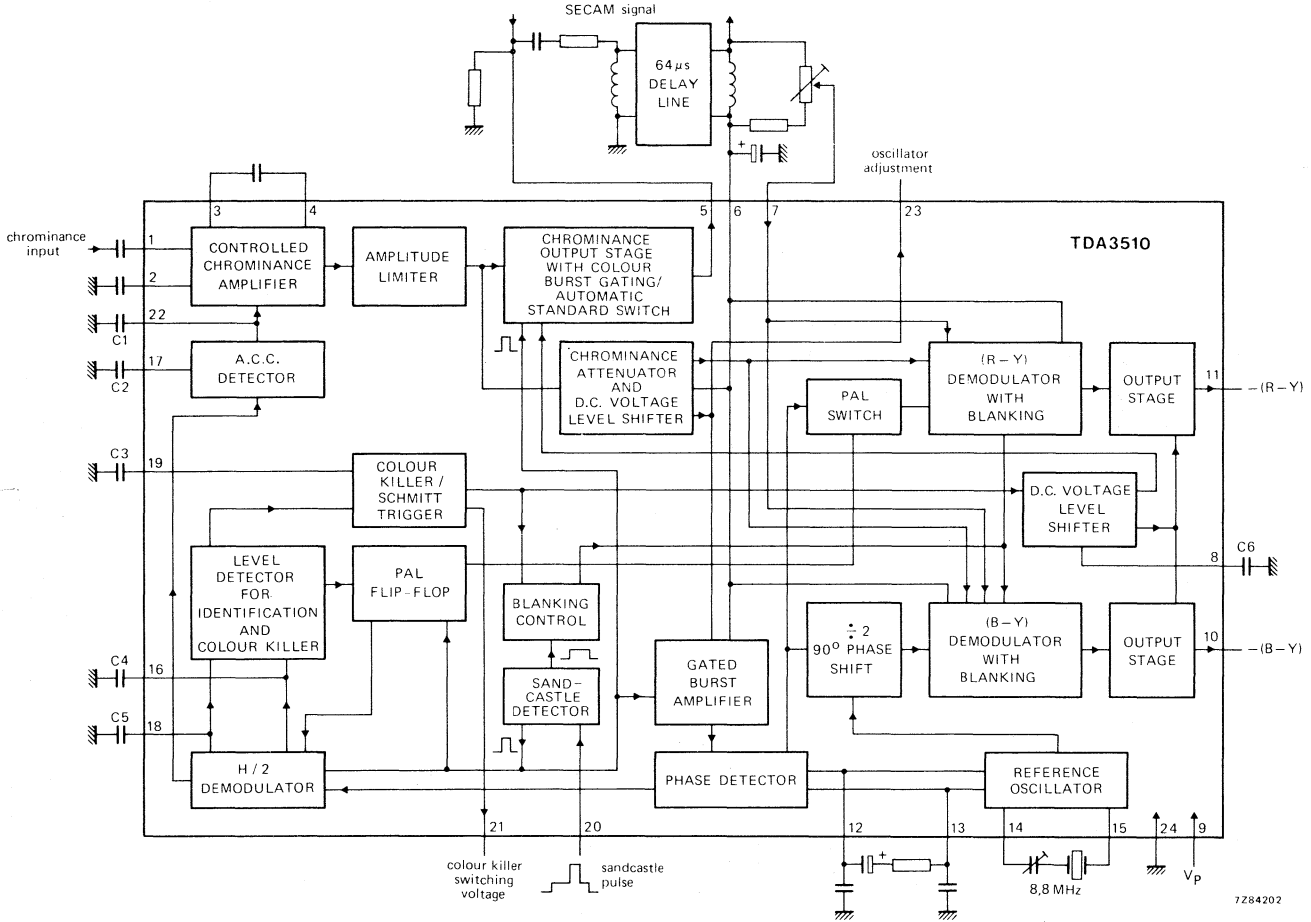


Fig. 1 Block diagram; for external capacitors see next page.

External capacitors in Fig. 1

capacitor	pins	
C1	22 – 24	filter capacitor for control voltage
C2	17 – 24	time constant for control voltage
C3	19 – 24	time constant for colour ON
C4	16 – 24	identification signal and colour OFF time constant
C5	18 – 24	load capacitor for the reference voltage
C6	8 – 24	time constant for the rise or fall time of the d.c. voltage level of the colour difference signal

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{9\text{-}24}$		10,8 to 13,2	V
Currents				
at pin 5	$-I_5$	max.	10	mA
at pins 10 and 11	$-I_{10}, -I_{11}$	max.	1	mA
at pin 21	I_{21}	max.	10	mA
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature	T_{stg}		−20 to + 125	°C
Operating ambient temperature	T_{amb}		−20 to + 65	°C

CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C

Supply current	I_9	typ.	58	mA

Chrominance part

Chrominance signal is asymmetric (pins 1, 2)

Input voltage range (peak-to-peak value)	$V_{1\text{-}24(p\text{-}p)}$		10 to 200	mV
Nominal input voltage (peak-to-peak value) with 75% colour bar signal	$V_{1\text{-}24(p\text{-}p)}$	typ.	100	mV
Input impedance	$\lvert Z_i \rvert$	typ.	3,3	kΩ
Colour ON				
chrominance output voltage (peak-to-peak value) with 75% colour bar signal	$V_{5\text{-}24(p\text{-}p)}$	typ.	2	V
d.c. voltage at chrominance output	$V_{5\text{-}24}$	typ.	8	V
Colour OFF				
chrominance suppression		>	56	dB
d.c. voltage at chrominance output	$V_{5\text{-}24}$	typ.	4	V

CHARACTERISTICS (continued)

Reference voltage and control voltage part

Oscillator (8,8 MHz)			
Gain	$G_{14\text{-}15}$	>	8 dB
Input resistance	$R_{15\text{-}24}$	typ.	270 Ω
Output resistance	$R_{14\text{-}24}$	<	200 Ω
Catching range	Δf	typ.	500 Hz
Sandcastle pulse (pin 20)			
Burst gating level	$V_{20\text{-}24}$	>	7,5 V
Blanking level	$V_{20\text{-}24}$	>	1,8 V
Colour switching voltage (open collector)			
Maximum output current	I_{21max}	typ.	10 mA
Colour ON	$V_{21\text{-}24}$	typ.	V_P
Colour OFF	$V_{21\text{-}24}$	<	0,5 V
Reference output voltage	$V_{18\text{-}24}$	typ.	5,5 V
Colour killer voltages			
colour OFF at	$V_{18\text{-}16}$	typ.	0 V
or at	$V_{19\text{-}24}$	>	6 V
colour ON at	$V_{18\text{-}16}$	typ.	1,5 V
or at	$V_{19\text{-}24}$	<	4 V
Colour unkill delay; depends on C3	t_d	typ.	20 ms/μF
Identification ON	$V_{16\text{-}18}$	<	200 mV

Demodulator part

Delayed chrominance input signal (peak-to-peak value) with 75% colour bar signal	$V_{7\text{-}24(p\text{-}p)}$	typ.	250 mV
Colour difference output signals (peak-to-peak values)			
−(R-Y) signal	$V_{11\text{-}24(p\text{-}p)}$	typ.	1,05 V ± 3 dB
−(B-Y) signal	$V_{10\text{-}24(p\text{-}p)}$	typ.	1,33 V ± 3 dB
Ratio of colour difference output signals (R-Y)/(B-Y)	$\frac{V_{11\text{-}24}}{V_{10\text{-}24}}$	typ.	0,79 ± 10 %
D.C. voltage at colour difference outputs			
at colour ON	$V_{10;\,11\text{-}24}$	typ.	8 V
at colour OFF	$V_{10;\,11\text{-}24}$	typ.	4 V
Signal attenuation at colour OFF		>	60 dB
Residual 4,4 MHz signal	$V_{10;\,11\text{-}24}$	<	20 mV
H/2 ripple at (R-Y) output (peak-to-peak value) without input signal	$V_{11\text{-}24(p\text{-}p)}$	<	10 mV

TELEVISION I.F. AMPLIFIERS AND DEMODULATORS

The TDA3540 and TDA3541 are i.f. amplifier and demodulator circuits for colour and black and white television receivers, using n-p-n tuners for the TDA3540 and p-n-p tuners for the TDA3541.

They incorporate the following functions:

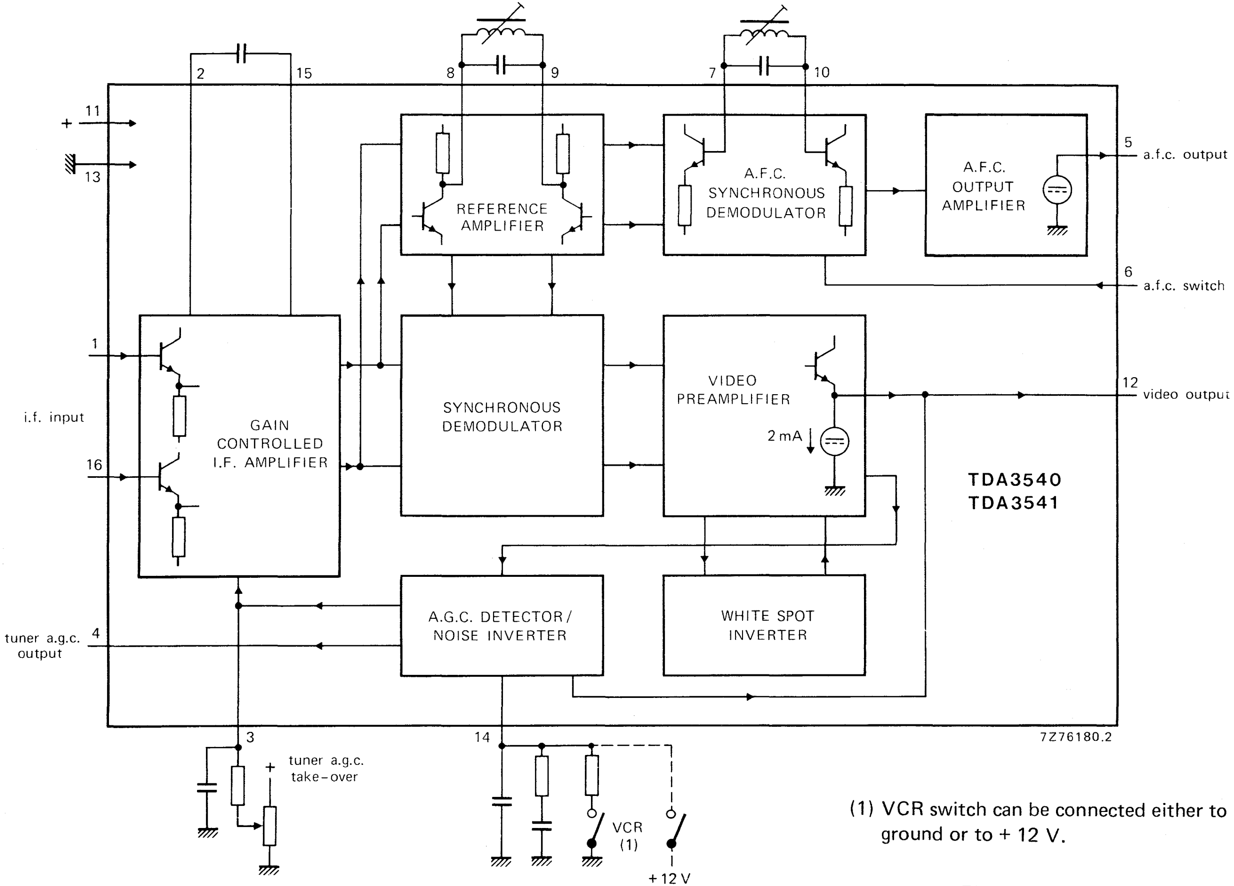
- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator with excellent intermodulation
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit with a.f.c. on/off switch
- a.g.c. circuit with noise gating
- tuner a.g.c. output (n-p-n tuners: **TDA3540**; p-n-p tuners: **TDA3541**)
- external video switch which switches off the video output; e.g. for insertion of a VCR playback signal, by either a high or a low level.

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}13}$	typ.	12	V
Supply current	I_{11}	typ.	50	mA
I.F. input sensitivity at 38,9 MHz (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	60	μV
Video output voltage (white at 10% of top sync)	$V_{12\text{-}13(p\text{-}p)}$	typ.	2,7	V
I.F. voltage gain control range	G_v	typ.	64	dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58	dB
A.F.C. output voltage swing (peak-to-peak value)	$V_{5\text{-}13(p\text{-}p)}$	typ.	10,7	V

PACKAGE OUTLINES

TDA3540; TDA3541: 16-lead DIL; plastic (SOT-38).
TDA3540Q; TDA3541Q: 16-lead QIL; plastic (SOT-58).



(1) VCR switch can be connected either to ground or to + 12 V.

Fig. 1 Block diagram.

PINNING

1 - 16	Balanced i.f. input.
2 - 15	Decoupling capacitor for the d.c. feedback loop of the i.f. amplifier.
3	Adjusting pin for starting point of tuner a.g.c.
4	Tuner a.g.c. output.
5	A.F.C. output.
6	A.F.C. on/off switch.
7 - 10	A.F.C. circuitry to obtain $\pi/2$ phase shift of the reference carrier.
8 - 9	Circuitry for passive regeneration of the i.f. picture carrier.
11	Positive power supply.
12	Video output.
13	Ground.
14	I.F. a.g.c.; VCR switch.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{11\text{-}13}$	max.	13,2	V
I.F. a.g.c. voltage/VCR switch	$V_{14\text{-}13}$	max.	13,2	V
Tuner a.g.c. voltage	$V_{4\text{-}13}$	max.	12	V
A.F.C. switch voltage	$V_{6\text{-}13}$	max.	13,2	V
Maximum voltage level at pin 12 with VCR switch active	$V_{12\text{-}13}$	max.	5,0	V
D.C. output current at video output	I_{12}	max.	10	mA
Total power dissipation	P_{tot}	max.	1,2	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (measured in Fig. 8)

Supply voltage range	$V_{11\text{-}13}$	typ.	12	V
			10,2 to 13,2	V

The following characteristics are measured at T_{amb} = 25 °C; $V_{11\text{-}13}$ = 12 V

Current consumption (no input signal)	I_{11}	typ.	50	mA
			35 to 70	mA

I.F. amplifier (note 1)

I.F. sensitivity (onset of a.g.c.)	$V_{1\text{-}16}$	typ.	60	μV
		$<$	100	μV
Input resistance (differential)	$R_{1\text{-}16}$	typ.	2	kΩ
			1,5 to 3	kΩ
Input capacitance (differential)	$C_{1\text{-}16}$	typ.	2	pF
		$<$	5	pF
Gain control range	G_v	typ.	64	dB
Output signal expansion for 50 dB input signal variation (note 2)	$\Delta V_{12\text{-}13}$	$<$	0,5	dB
Maximum input signal	$V_{1\text{-}16}$	$>$	70	mV

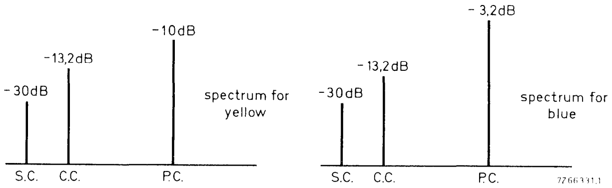
Tuner a.g.c. (note 1)

Starting point tuner a.g.c.; adjustable (note 3)				
pin 3 connected with 39 kΩ to pin 11				
TDA3540	$V_{1\text{-}16}$	$<$	3	mV
TDA3541	$V_{1\text{-}16}$	$<$	3	mV
pin 3 connected with 39 kΩ to ground	$V_{1\text{-}16}$	$>$	70	mV
Maximum tuner a.g.c. output current swing	I_4	$>$	10	mA
Input signal variation (note 4) for a tuner a.g.c. current variation of:				
9 mA to 1 mA **(TDA3540)**	$\Delta V_{1\text{-}16}$	typ.	5	dB
1 mA to 9 mA **(TDA3541)**	$\Delta V_{1\text{-}16}$	typ.	5	dB
Output saturation voltage at I_4 = 7 mA	$V_{4\text{-}13sat}$	typ.	200	mV
		$<$	300	mV
Leakage current at $V_{4\text{-}13}$ = 12 V	I_4	$<$	1	μA
Tuner a.g.c. characteristic	see Fig. 5			

Video output (note 5)

Zero-signal output level (note 6)	$V_{12\text{-}13}$	typ.	6	V
			5,7 to 6,3	V
Top sync output level	$V_{12\text{-}13}$	typ.	2,95	V
			2,80 to 3,10	V
Video output signal (peak-to-peak value) white at 10% of top sync	$V_{12\text{-}13(p\text{-}p)}$	typ.	2,7	V

Internal bias current of n-p-n emitter-follower output transistor		typ.	2 1 to 3	mA mA
Bandwidth of demodulated output signal	B	> typ.	5,5 6,5	MHz MHz
Differential gain (note 7)	dG	typ. <	3 10	% %
Differential phase (note 8)	$d\varphi$	typ. <	2° 10°	
Residual carrier signal (r.m.s. value)	$V_{12\text{-}13(rms)}$	typ. <	3,5 30,0	mV mV
Residual 2nd harmonic of carrier signal (r.m.s. value)	$V_{12\text{-}13(rms)}$	typ. <	15 30	mV mV
Intermodulation (see Figs 2 and 3) at 1,1 MHz: blue (note 9)		> typ.	56 62	dB dB
yellow (note 9)		> typ.	53 57	dB dB
at 3,3 MHz (note 10)		>	66	dB



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level

with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

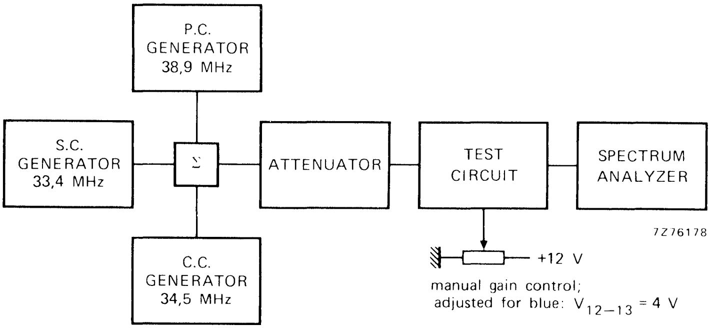


Fig. 3 Test set-up for intermodulation.

CHARACTERISTICS (continued)

Signal-to-noise ratio (note 11)		
at 10 mV input signal	S/N	> 50 dB typ. 58 dB
at end of gain control range	S/N	> 54 dB typ. 61 dB
as a function of the input signal	see Fig. 6	

White spot and noise inverter (see Fig. 4)

White spot inverter threshold level	$V_{12\text{-}13}$	typ. 6,8 V 6,3 to 7,3 V
White spot insertion level	$V_{12\text{-}13}$	typ. 4,5 V 4,2 to 4,8 V
Noise inverter threshold level	$V_{12\text{-}13}$	typ. 1,8 V 1,6 to 2,0 V
Noise insertion level	$V_{12\text{-}13}$	typ. 3,8 V 3,4 to 4,1 V

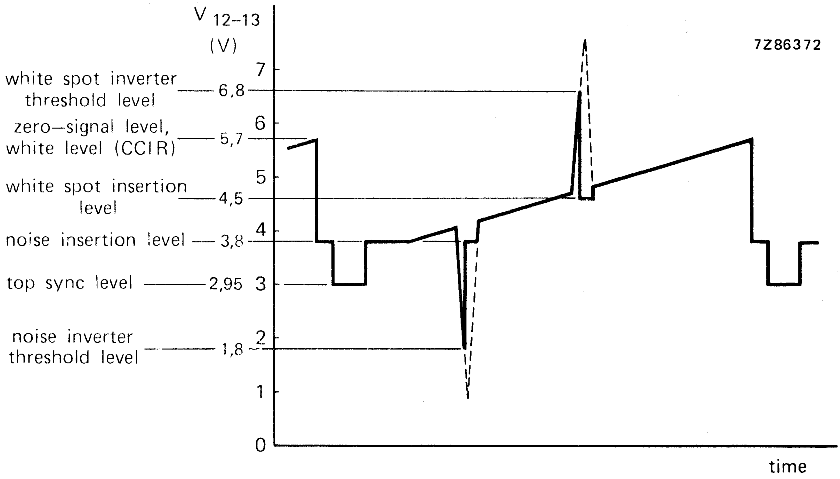


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

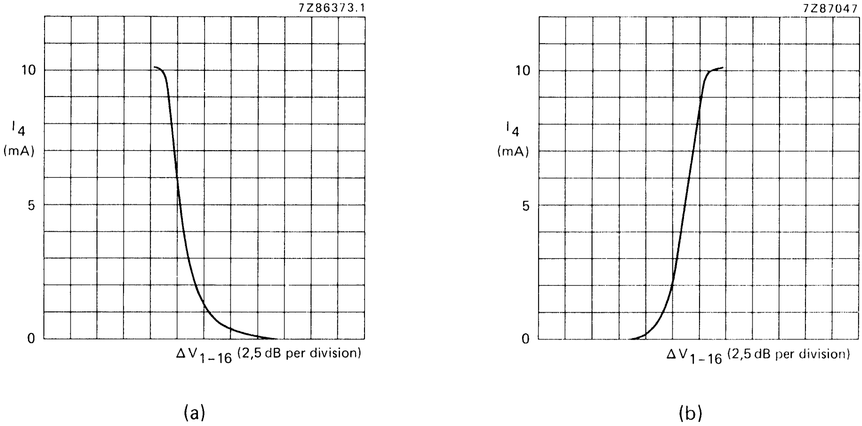
VCR switch

Switches the output off:		
below	$V_{14\text{-}13}$	typ. 1,9 V 1,4 to 2,4 V
above	$V_{14\text{-}13}$	typ. 10,7 V 10 to 11,3 V

A.F.C. (note 12)

A.F.C. output voltage swing (peak-to-peak value)	$V_{5\text{-}13(p\text{-}p)}$	> typ.	10 10,7	V V
Change of frequency for an a.f.c. output voltage swing of 10 V at 100% picture carrier	Δf	typ. <	70 150	kHz kHz
at 10% picture carrier	Δf	typ. <	100 200	kHz kHz
A.F.C. output voltage when tuned at 38,9 MHz	$V_{5\text{-}13}$	typ.	6	V
A.F.C. output voltage (no input signal)	$V_{5\text{-}13}$	typ.	6 4 to 8	V V
A.F.C. switch switches off below	$V_{6\text{-}13}$	typ.	2,9 1,6 to 3,5	V V
Recommended a.f.c. active voltage	$V_{6\text{-}13}$ or: pin 6 floating		3,5 to 6	V
A.F.C. switch leakage current at $V_{6\text{-}13} = 6$ V	I_6	<	1	μA
A.F.C. output current during a.f.c. off measured with $f_o \pm 300$ kHz and $V_{6\text{-}13} = 1{,}5$ V	I_5		−2,5 to + 2,5	μA
A.F.C. output current during a.f.c. on	I_5	> typ.	1 2	mA mA

DEVELOPMENT SAMPLE DATA



(a)

(b)

Fig. 5 Typical tuner a.g.c. characteristics;
pin 3 connected to the supply voltage (pin 11) with 39 kΩ.

a: TDA3540
b: TDA3541

CHARACTERISTICS (continued)

Notes to characteristics

1. All input signals are measured r.m.s. at top sync and 38,9 MHz.
2. Measured with 0 dB = 200 μV.
3. Starting point of the tuner a.g.c. is defined as the input signal level where the tuner a.g.c. current is 9 mA for the **TDA3540** and 1 mA for the **TDA3541**.
4. Measured with pin 3 connected with 39 kΩ to the supply voltage (pin 11).
5. Measured at 10 mV r.m.s. top sync input signal.
6. So-called 'projected zero point', e.g. with switched demodulator.
7. Measured according to EBU test, line 330.
   The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest section relative to the sub-carrier amplitude at blanking level.
8. Measured according to EBU test, line 330.
   The differential phase is defined as the difference in degrees between the largest and smallest phase angle of the six sections.
9. $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 1{,}1 \text{ MHz}} + 3{,}6 \text{ dB}$.
10. $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 3{,}3 \text{ MHz}}$.
11. Measured with a 75 Ω source; $S/N = 20 \log \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.
12. Measured with an input signal $V_{1\text{-}16}$ = 10 mV and a.f.c. output pin 5 symmetrically loaded with 100 kΩ to the supply voltage ($V_{11\text{-}13}$) and 100 kΩ to ground.

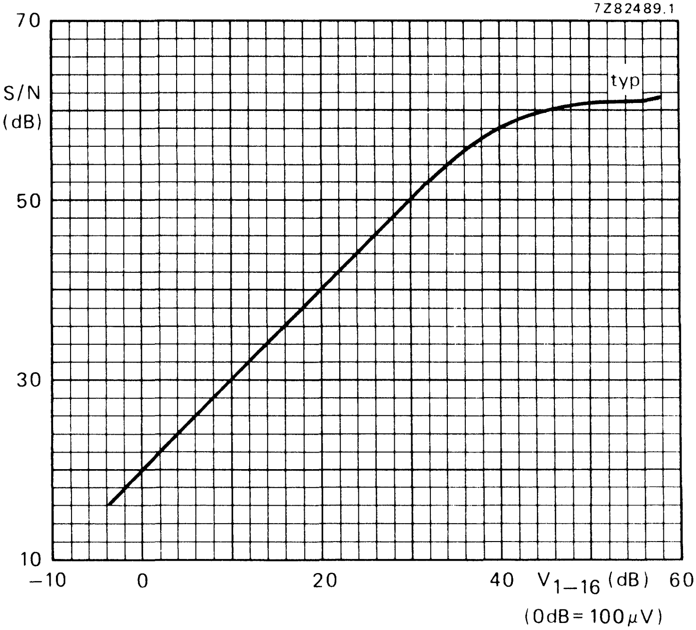


Fig. 6 Signal-to-noise ratio as a function of the input voltage ($V_{1\text{-}16}$).

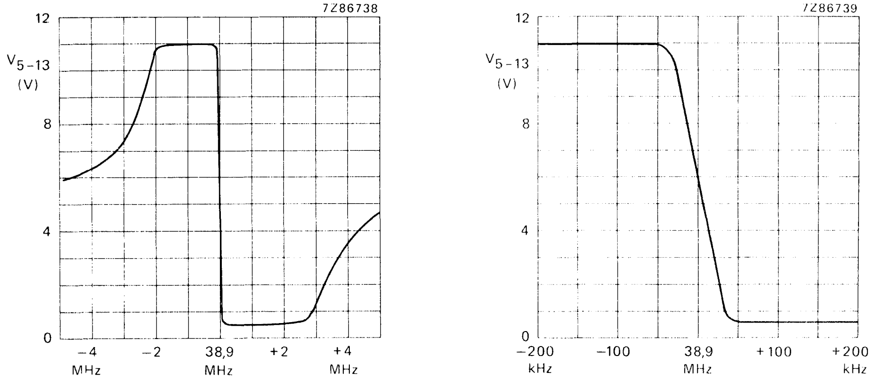


Fig. 7 A.F.C. output voltage ($V_{5\text{-}13}$) as a function of deviation of the i.f. vision carrier from its nominal frequency.

APPLICATION INFORMATION

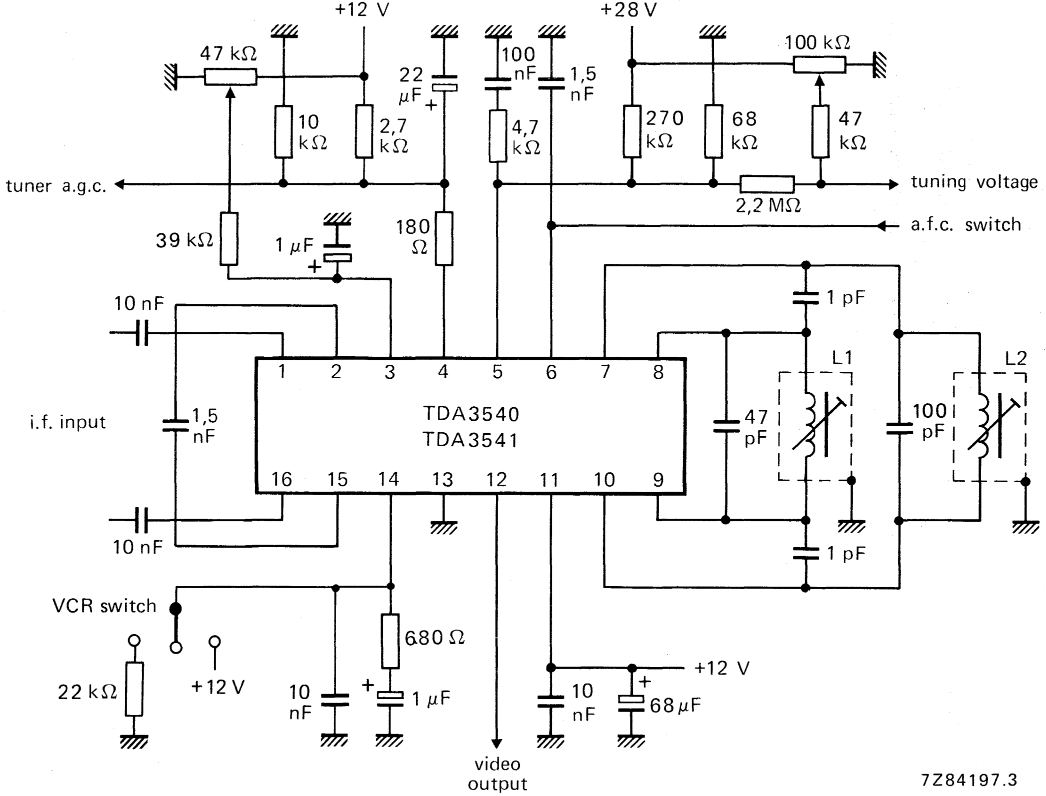


Fig. 8 Typical application circuit diagram; Q of L1 and L2 = 80; f_o = 38,9 MHz.

PAL DECODER

The TDA3560 is a monolithic integrated colour decoder for the PAL standard. It combines all functions required for the identification and demodulation of PAL signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for Teletext information, channel number display, etc.

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}27}$	typ.	12	V
Supply current	I_1	typ.	85	mA
Luminance input signal (peak-to-peak value)	$V_{10\text{-}27(p\text{-}p)}$	typ.	0,45	V
Chrominance input signal (peak-to-peak value)	$V_{3\text{-}27(p\text{-}p)}$	55 to	1100	mV
Data input signals (peak-to-peak value)	$V_{13,15,17\text{-}27(p\text{-}p)}$	typ.	1	V
RGB output signals at nominal contrast and saturation (peak-to-peak value)	$V_{12,14,16\text{-}27(p\text{-}p)}$	typ.	5	V
Contrast control range		typ.	20	dB
Saturation control range		typ.	50	dB
Input for fast video-data signal switching	$V_{9\text{-}27}$	typ.	1	V
Blanking input voltage	$V_{8\text{-}27}$	typ.	1,5	V
Burst gating and black-level gating input voltage	$V_{8\text{-}27}$	typ.	7	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

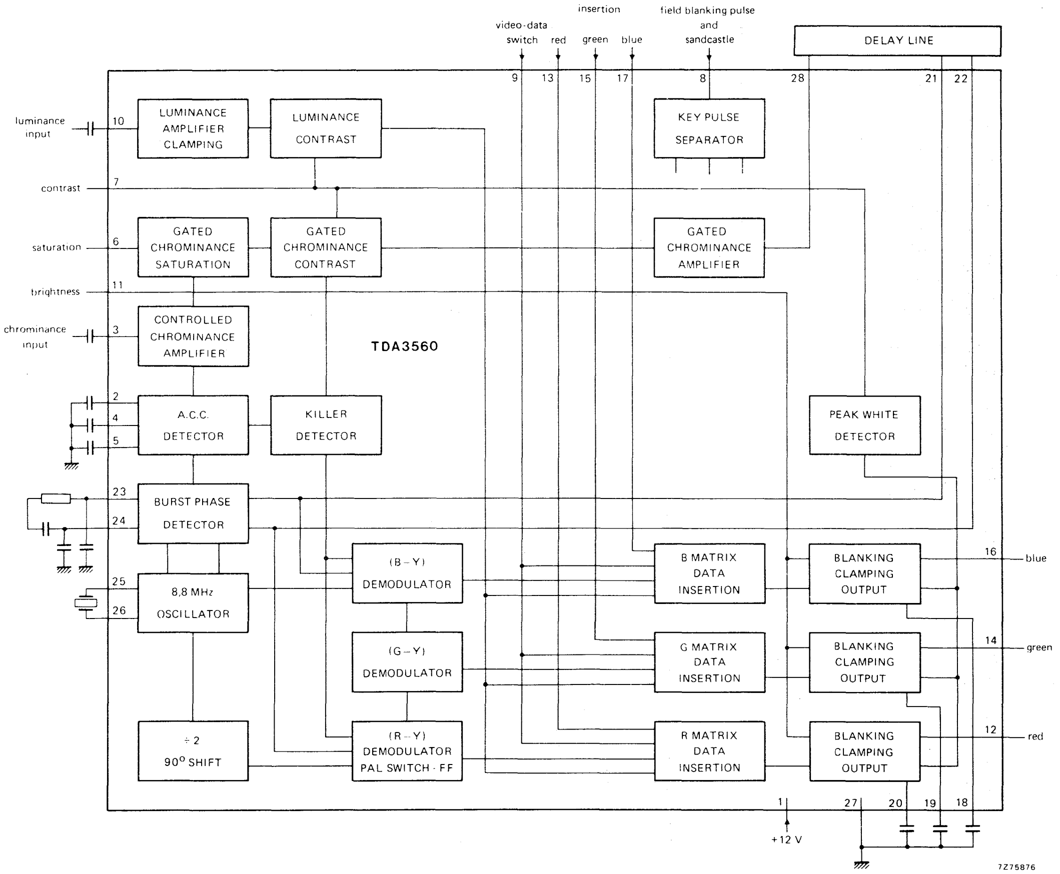


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		min.	max.	
Supply voltage	$V_P = V_{1\text{-}27}$	–	13,2	V
Input saturation voltage	$V_{6\text{-}27}$	0	V_P	V
Input contrast voltage	$V_{7\text{-}27}$	0	V_P	V
Input blanking pulse and sandcastle	$V_{8\text{-}27}$	0	V_P	V
Input video-data switch voltage	$V_{9\text{-}27}$	0	V_P	V
Input brightness voltage	$V_{11\text{-}27}$	0	V_P	V
Power dissipation	see Fig. 2			
Storage temperature	T_{stg}	−25 to	+ 150	°C
Operating ambient temperature	T_{amb}	−25 to	+ 65	°C

CHARACTERISTICS

$V_{1\text{-}27} = 12$ V; $V_{10\text{-}27(p\text{-}p)} = 0{,}45$ V; $V_{3\text{-}27(p\text{-}p)} = 500$ mV; $T_{amb} = 25$ °C; measured in Fig. 6; unless otherwise specified

Supply voltage range	V_P	typ.	12	V
			8 to 13,2	V
Supply current	I_1	typ.	85	mA
Luminance amplifier				
Input voltage (peak-to-peak value)	$V_{10\text{-}27(p\text{-}p)}$	typ.	0,45	V
Input current	I_{10}	<	1	μA
Contrast control range			−17 to + 3	dB
Contrast control voltage range	see Fig. 3			
Chrominance amplifier				
Input voltage (peak-to-peak value)	$V_{3\text{-}27(p\text{-}p)}$		55 to 1100	mV
A.C.C. control range		>	30	dB
Output signal (peak-to-peak value) * burst signal (peak-to-peak value) = 0,5 V	$V_{28\text{-}27(p\text{-}p)}$	typ.	1,7	V
Saturation control range		>	50	dB
Saturation control voltage range	see Fig. 4			
Phase shift between burst and chrominance *		<	5°	
Tracking between luminance and chrominance with contrast control over a range of 10 dB, starting at maximum contrast		typ.	1	dB

---

* At nominal contrast and saturation setting. Nominal setting = maximum contrast −3 dB; maximum saturation −6 dB.

CHARACTERISTICS (continued)

Reference oscillator

Phase locked loop:				
– catching range (note 1)		>	500	Hz
– phase shift (note 2)		<	5°	
Oscillator:				
– input resistance	R_{26-27}	typ.	300	Ω
– input capacitance	C_{26-27}	<	10	pF
– output resistance	R_{25-27}	typ.	200	Ω
A.C.C. generation:				
– reference voltage	V_{4-27}	typ.	4,6	V
– control voltage at nominal input signal	V_{2-27}	typ.	4,7	V
– control voltage without burst	V_{2-27}	typ.	2,4	V

Demodulator circuit

Input burst signal amplitude (peak-to-peak value)	$V_{21,22-27(p-p)}$	typ.	60	mV
Ratio of demodulated signals without luminance input signal				
(B-Y)/(R-Y)	$\frac{V_{16-27}}{V_{12-27}}$	typ.	1,78	
(G-Y)/(R-Y)	$\frac{V_{14-27}}{V_{12-27}}$	typ.	–0,51	
(G-Y)/(B-Y)	$\frac{V_{14-27}}{V_{16-27}}$	typ.	–0,19	

RGB matrix and amplifiers

Output voltage (peak-to-peak value) (note 3)	$V_{12,14,16-27(p-p)}$	typ.	5	V
Maximum white level		typ.	9,3	V
Birghtness control voltage range	see Fig. 5			
Relative spread between R, G and B output signals		<	10	%
Variation of black level with contrast control	ΔV	<	200	mV
Relative black-level variation between the three stages during variation of contrast saturation, brightness and supply voltage		<	20	mV
Differential black-level drift over a temperature range of 40 °C		<	20	mV
Blanking level at RGB outputs		typ.	2,1	V
Signal-to-noise ratio of output signals (note 4)	S/N	>	62	dB

Notes

1. Frequency referred to 4,4 MHz carrier frequency.
2. For ± 400 Hz deviation of the oscillator frequency.
3. For nominal setting of the controls.
4. The signal-to-noise ratio is specified as the nominal peak-to-peak output signal with respect to r.m.s. noise.

Residual 8,8 MHz and higher harmonics on RGB-outputs (peak-to-peak value)		<	150 mV
Output impedance RGB outputs	$\|Z_o\|$	typ.	50 Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		<	−3 dB
Signal insertion			
Input signals for an RGB output voltage of 5 V (peak-to-peak value)	$V_{13,15,17\text{-}27(p\text{-}p)}$	typ.	1 V
Difference between the black levels of the RGB signals and the inserted signals at the output	ΔV	<	260 mV
Output rise time	t_r	typ.	50 ns
Differential delay time for the three channels	t_d	<	40 ns
Video-data switching			
Input voltage for switching from video to inserted signals	$V_{9\text{-}27}$		0,9 to 2 V
Input voltage for no data insertion	$V_{9\text{-}27}$	<	0,3 V
Delay between signal switching at the output and the signal switching input pulse at pin 9	t_d	<	20 ns
Sandcastle and field blanking input (pin 8)			
Burst gate and clamping pulse	$V_{8\text{-}27}$	>	7,5 V
RGB blanking level			
on	$V_{8\text{-}27}$		2 to 6,5 V
off	$V_{8\text{-}27}$	<	0,8 V

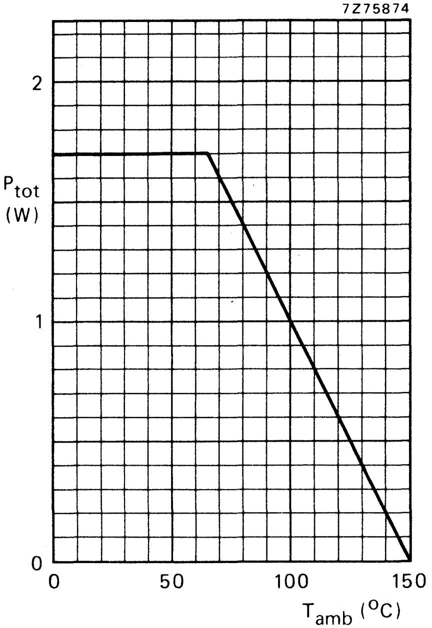


Fig. 2 Power derating curve.

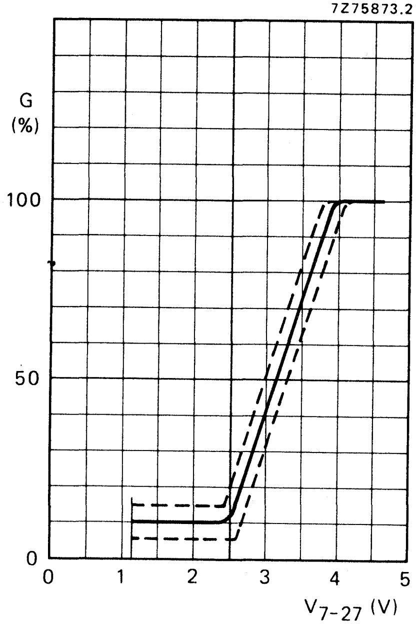


Fig. 3 Contrast control voltage range.

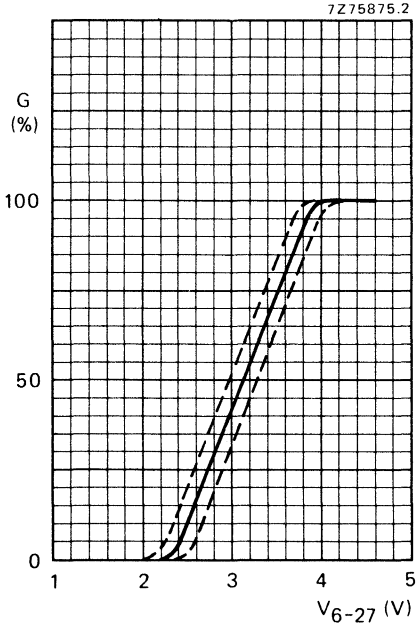


Fig. 4 Saturation control voltage range.

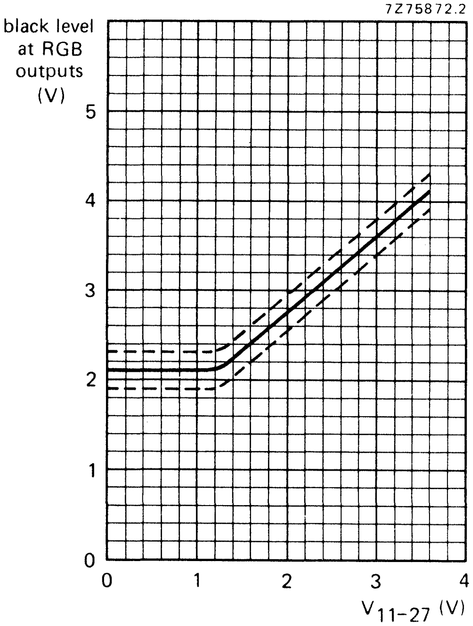


Fig. 5 Brightness control voltage range.

APPLICATION INFORMATION

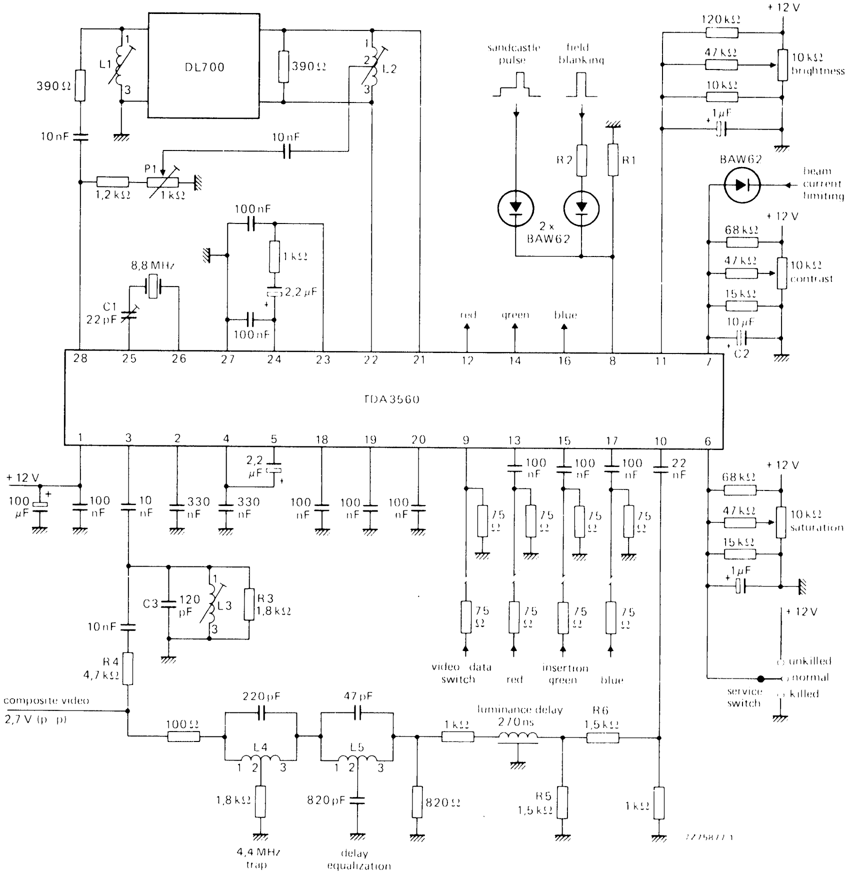


Fig. 6 Application circuit.
For adjustments see page 488.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. + 12 V power supply

The circuit gives good operation in a supply voltage range between 8 and 13,2 V provided that the supply voltage for the controls is equal to the supply voltage for the TDA3560. All signal and control levels have a linear dependency on the supply voltage. The current taken by the device at 12 V is typically 85 mA. It is linearly dependent on the supply voltage.

2. Control voltage for identification

This pin requires a detection capacitor of about 330 nF for correct operation. The voltages available under various signal conditions are given in the specification.

3. Chrominance input

The chroma signal must be a.c.-coupled to the input. Its amplitude must be between 55 mV and 1100 mV peak-to-peak (25 mV to 500 mV peak-to-peak burst signal). All figures for the chroma signals are based on a colour bar signal with 75% saturation, that is the burst-to-chroma ratio of the input signal is 1 : 2,25.

4. Reference voltage A.C.C. detector

This pin must be decoupled by a capacitor of about 330 nF. The voltage at this pin is 4,6 V.

5. Control voltage A.C.C.

The A.C.C. is obtained by synchronous detection of the burst signal followed by a peak detector. A good noise immunity is obtained in this way and an increase of the colour for weak input signals is prevented. The recommended capacitor value at this pin is 2,2 μF.

6. Saturation control

The saturation control range is in excess of 50 dB. The control voltage range is 2 to 4 V. Saturation control is a linear function of the control voltage.

When the colour killer is active, the saturation control voltage is reduced to a low level if the resistance of the external saturation control network is sufficiently high. Then the chroma amplifier supplies no signal to the demodulator. Colour switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply the colour killer circuit is overruled so that the colour signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also pins 25 and 26).

7. Contrast control

The contrast control range is 20 dB for a control voltage change from + 2 to + 4 V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1 V or less. If one or more output signals surpasses the level of 9 V the peak white limiter circuit becomes active and reduces the output signals via the contrast control by discharging C2 via an internal current sink.

8. Sandcastle and field blanking input

The output signals are blanked if the amplitude of the input pulse is between 2 and 6,5 V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7,5 V.
The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of video signal on the sync pulse. The width should be about 4 μs for proper A.C.C. operation.

9. Video-data switching

The insertion circuit is activated by means of this input by an input pulse between 1 V and 2 V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted this pin should be connected to the negative supply. The switching times are very short (< 20 ns) to avoid coloured edges of the inserted signals on the screen.

10. Luminance signal input

The input signal should have a peak-to-peak amplitude of 0,45 V (peak white to sync) to obtain a black-white output signal of 5 V at nominal contrast. It must be a.c.-coupled to the input by a capacitor of about 22 nF. The signal is clamped at the input to an internal reference voltage.
A 1 kΩ luminance delay line can be applied because the luminance input impedance is made very high. Consequently the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally the coupling capacitor value may be small.

11. Brightness control

The black level of the RGB outputs can be set by the voltage on this pin (see Fig. 5). The minimum black level is identical to the blanking level. The black level can be set higher than 4 V however the available output signal amplitude is reduced (see pin 7). Brightness control also operates on the black level of the inserted signals.

12, 14, 16. RGB outputs

The output circuits for red, green and blue are identical. Output signals are 5 V (black-white) for nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2 V. The peak white level is limited to 9 V. When this level is exceeded the output signal amplitude is reduced via the contrast control (see pin 7).

13, 15, 17. Inputs for external RGB signals

The external signals must be a.c.-coupled to the inputs via a coupling capacitor of about 100 nF. Source impedance should not exceed 150 Ω. The input signal required for a 5 V peak-to-peak output signal is 1 V peak -to-peak. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used the coupling capacitors have to be connected to the negative supply.

18, 19, 20. Black level clamp capacitors

The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100 nF.

21, 22. Inputs (B-Y) and (R-Y) demodulators

The input signal is automatically fixed to the required level by means of the burst phase detector and A.C.C. generator which are connected to this pin and pin 22. As the burst (applied differentially to those pins) is kept constant by the A.C.C., the colour difference signals automatically have the correct value.

APPLICATION INFORMATION (continued)

23, 24. Burst phase detector outputs

At these pins the output of the burst phase detector is filtered and controls the reference oscillator. An adequate catching range is obtained with the time constants given in the application circuit (see Fig. 6).

25, 26. Reference oscillator

The frequency of the oscillator is adjusted by the variable capacitor C1. For frequency adjustment interconnect pin 23 and pin 24. The frequency can be measured by connecting a suitable frequency counter to pin 25.

28. Output of the chroma amplifier

Both burst and chroma signals are available at the output. The burst-to-chroma ratio at the output is identical to that at the input for nominal control settings. The burst signal is not affected by the controls. The amplitude of the input signal to the demodulator is kept constant by the A.C.C. Therefore the output signal at pin 28 will depend on the signal loss in the delay line.

Adjustments (see Fig. 6)

C1	8,8 MHz osciliator	
L1	phase delay line	= 10,7 μH
L2	nominal value	= 10,7 μH
L3	4,4 MHz chrominance input filter	= 10,7 μH = L1
L4	4,4 MHz trap in luminance signal line	= 5,6 μH
L5	delay equalization	= 66,1 μH
P1	amplitude of direct chroma signal	
R1 R2	field blanking $\frac{R1}{R1 + R2}$ x field blanking amplitude 2,0 V to 6,5 V.	

For a video input voltage of 1 V peak-to-peak: R4 = 1 kΩ; R3, R5 and R6 can be omitted.

PAL DECODER

The TDA3561A is a decoder for the PAL colour television standard. It combines all functions required for the identification and demodulation of PAL signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. (Teletext/ broadcast antiope), channel number display, etc. Additional to the TDA3560, the circuit includes the following features:

- The peak white limiter is only active during the time that the 9,3 V level at the output is exceeded. The start of the limiting function is delayed by one line period. This avoids peak white limiting by test patterns which have abrupt transitions from colour to white signals.
- The brightness control is obtained by inserting a variable pulse in the luminance channel. Therefore the ratio of brightness variation and signal amplitude at the three outputs will be identical and independent of the difference in gain of the three channels. Thus discolouring due to adjustment of contrast and brightness is avoided.
- Improved suppression of the internal RGB signals when the device is switched to external signals, and vice versa.
- Non-synchronized external RGB signals do not disturb the black level of the internal signals.
- Improved suppression of the residual 4,4 MHz signal in the RGB output stages.
- Cascoded stages in the demodulators and burst phase detector minimize the radiation of the colour demodulator inputs.
- High current capability of the RGB outputs and the chrominance output.

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}27}$	type.	12	V
Supply current	I_1	typ.	85	mA
Luminance input signal (peak-to-peak value)	$V_{10\text{-}27(p\text{-}p)}$	typ.	0,45	V
Chrominance input signal (peak-to-peak value)	$V_{3\text{-}27(p\text{-}p)}$		55 to 1100	mV
Data input signals (peak-to-peak value)	$V_{13,15,17\text{-}27(p\text{-}p)}$	typ.	1	V
RGB output signals at nominal contrast and saturation (peak-to-peak value)	$V_{12,14,16\text{-}27(p\text{-}p)}$	typ.	5,25	V
Contrast control range		typ.	20	dB
Saturation control range		min.	50	dB
Input voltage for data insertion	$V_{9\text{-}27}$	min.	0,9	V
Blanking input voltage	$V_{8\text{-}27}$	typ.	1,5	V
Burst gating and black-level gating input voltage	$V_{8\text{-}27}$	typ.	7	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

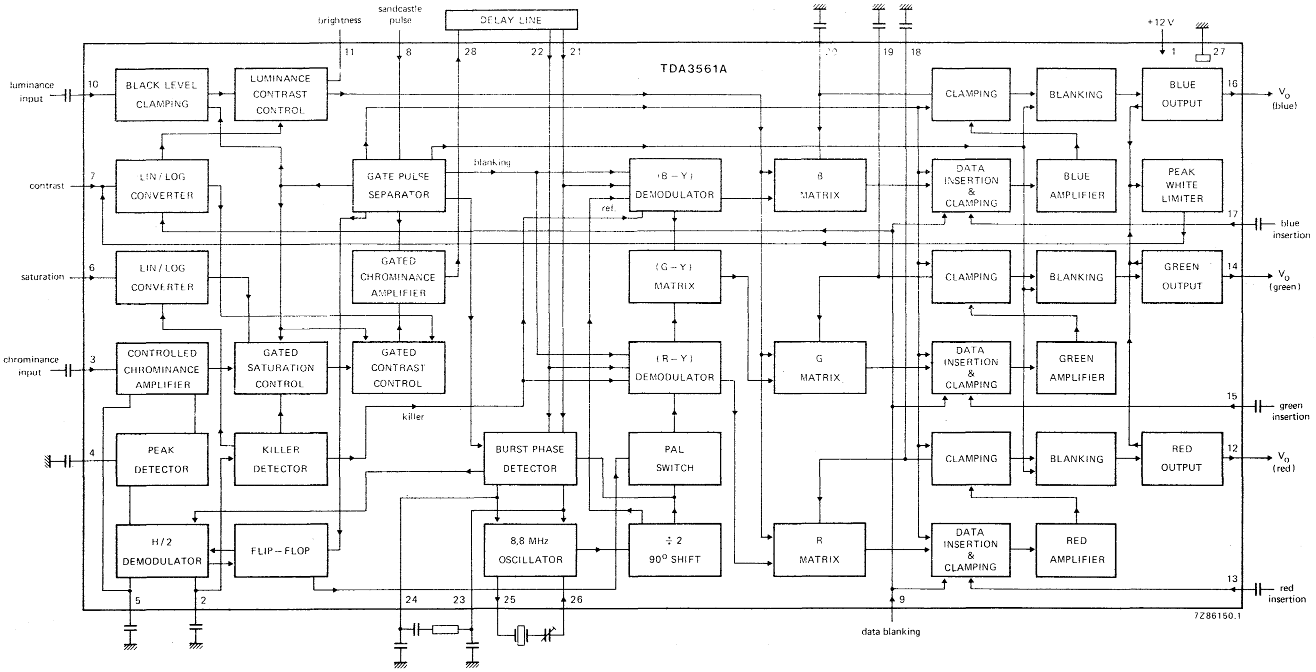


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{1\text{-}27}$	max.	13,2	V
Total power dissipation; see also Fig. 2	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	50	K/W

CHARACTERISTICS

$V_P = V_{1\text{-}27} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

Supply voltage	$V_P = V_{1\text{-}27}$	typ.	12	V
			8 to 13,2	V
Supply current		typ.	85	mA
		<	115	mA
Total power dissipation	P_{tot}	typ.	1,0	W
		<	1,4	W
Luminance input (pin 10)				
Input voltage (peak-to-peak value); note 1	$V_{10\text{-}27(p\text{-}p)}$	typ.	0,45	V
Input level before clipping	$V_{10\text{-}27}$	<	2	V
Input current; input level 2 V, clamp not active	I_{10}	typ.	0,15	μA
		<	1	μA
Contrast control range (see Fig. 3)			−17 to + 3	dB
Control voltage for 40 dB attenuation	$V_{7\text{-}27}$	typ.	1,2	V
Input current contrast control at $V_{7\text{-}27} = 3$ V	I_7	<	10	μA
Chrominance amplifier				
Input voltage (peak-to-peak value); note 2	$V_{3\text{-}27(p\text{-}p)}$	typ.	550	mV
			55 to 1100	mV
Input impedance	$\|Z_{3\text{-}27}\|$	typ.	9	kΩ
			6 to 12	kΩ
Input capacitance	$C_{3\text{-}27}$	typ.	4	pF
		<	6	pF
A.C.C. control range		>	30	dB
Change of the burst signal at the output over the whole control range		<	1,5	dB
Gain at nominal contrast/saturation pin 3 to pin 28; note 3		>	32	dB
Output signal (peak-to-peak value) at nominal contrast/saturation; burst signal: 0,5 V peak to peak	$V_{28\text{-}27(p\text{-}p)}$	typ.	1,7	V
Maximum output voltage (peak-to-peak value) $R_L = 2$ kΩ	$V_{28\text{-}27(p\text{-}p)}$	typ.	4,0	V

CHARACTERISTICS (continued)

Chrominance amplifier (continued)

Distortion of chrominance amplifier at $V_{28\text{-}27(p\text{-}p)} = 2$ V up to $V_{3\text{-}27(p\text{-}p)} = 1$ V	d	typ. <	1,5 5	% %
Frequency response between 0 and 5 MHz			−2	dB
Saturation control range (see Fig. 4)		>	50	dB
Input current saturation control at $V_{6\text{-}27} = 3$ V	I_6	<	15	μA
Tracking between luminance and chrominance with contrast control over a range of 10 dB		<	2	dB
Cross-coupling between luminance and chrominance amplifier; note 10		<	−46	dB
Signal-to-noise ratio at nominal input signal; note 11	S/N	>	56	dB
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\varphi$	<	± 5°	
Output impedance of chrominance amplifier	$\lvert Z_{28\text{-}27} \rvert$	typ.	25	Ω
Maximum output current	I_{28}	<	15	mA

Reference part

Phase locked loop:				
– catching range; note 4		> typ.	500 700	Hz Hz
– phase shift; note 5		<	5°	
Oscillator:				
– temperature coefficient of oscillator frequency; note 4		typ.	−1,5	Hz/K
– frequency deviation for V_P changing from 10 to 13,2 V; note 4		typ.	40	Hz
– input resistance (pin 26)	$R_{26\text{-}27}$	typ. 	340 260 to 420	Ω Ω
– input capacitance (pin 26)	$C_{26\text{-}27}$	<	10	pF
– output resistance (pin 25)	$R_{25\text{-}27}$	typ. 	150 100 to 200	Ω Ω
– output voltage (peak-to-peak value; pin 25)	$V_{25\text{-}27(p\text{-}p)}$	typ.	700	mV
A.C.C. generation:				
– reference voltage (pin 4)	$V_{4\text{-}27}$	typ.	4,9	V
– control voltage at nominal input signal (pin 2)	$V_{2\text{-}27}$	typ.	5,1	V
– control voltage without chrominance input (pin 2)	$V_{2\text{-}27}$	typ.	2,65	V
– colour-off voltage (pin 2)	$V_{2\text{-}27}$	typ.	3,15	V
– colour-on voltage (pin 2)	$V_{2\text{-}27}$	typ.	3,4	V
– identification-on voltage (pin 2)	$V_{2\text{-}27}$	typ.	1,9	V
– change in burst amplitude with supply voltage (± 10%)		proportional		
– change in burst amplitude with temperature		typ. <	0,1 0,25	%/K %/K
– voltage at pin 5 at nominal input signal	$V_{5\text{-}27}$	typ.	5	V

Demodulator part

Input burst signal amplitude (peak-to-peak value) between pins 21 and 22; note 6	$V_{21\text{-}22(p\text{-}p)}$	typ.	100	mV
Input impedance between pins 21 and 22	$\lvert Z_{21\text{-}22}\rvert$	typ.	2	kΩ
Ratio of demodulated signals for equal input signals at pins 21 and 22 (B–Y)/(R–Y)	$\frac{V_{16\text{-}27}}{V_{12\text{-}27}}$	typ.	1,78 ± 10%	
(G–Y)/(R–Y); no (B–Y) signal	$\frac{V_{14\text{-}27}}{V_{12\text{-}27}}$	typ.	–0,51 ± 10%	
(G–Y)/(B–Y); no (R–Y) signal	$\frac{V_{14\text{-}27}}{V_{16\text{-}27}}$	typ.	–0,19 ± 25%	
Frequency response between 0 and 1 MHz			–3	dB
Cross talk between colour demodulated signals		>	40	dB
Phase difference between (R–Y) signal and (R–Y) reference signal		<	5°	
Phase difference between (R–Y) and (B–Y) reference signals		typ.	90° 85 to 95°	

R.G.B. matrix and amplifiers

Output voltage (peak-to-peak value) at nominal luminance/contrast (black to white); note 3	$V_{12,14,16\text{-}27(p\text{-}p)}$	typ.	5,4 4,5 to 6,3	V V
Output voltage (peak-to-peak value) of the RED channel at nominal contrast/saturation and no luminance signal at the input, (R–Y) signal	$V_{12\text{-}27(p\text{-}p)}$	typ.	5,25 3,7 to 6,7	V V
Maximum peak white level; note 7		typ.	9,3 9,0 to 9,6	V V
Maximum output current	$I_{12,14,16}$	<	15	mA
Black level at the output for a brightness control voltage of 2 V	$V_{12,14,16\text{-}27}$	typ.	2,6	V
Difference in black level between the three channels at an output level of 3 V; note 8	ΔV	<	200	mV
Black level shift with vision contents		<	40	mV
Brightness control voltage range	see Fig. 5			
Input current brightness control	I_{11}	<	50	μA
Variation of black level with temperature	ΔV	typ. <	0,35 1,0	mV/K mV/K
Variation of black level with contrast control	ΔV	typ. <	10 200	mV mV
Relative spread between the R, G and B output signals		<	10	%
Relative black-level variation between the three channels during variation of contrast and supply voltage		typ. <	0 20	mV mV

CHARACTERISTICS (continued)

RGB matrix and amplifier (continued)

Differential black-level drift over a temperature range of 40 °C		typ. <	0 20	mV mV
Blanking level at the RGB outputs		typ.	2,1 1,9 to 2,3	V V
Difference in blanking level of the three channels		typ.	0	mV
Differential blanking level drift over a temperature range of 40 °C		typ.	0	mV
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	typ.	1,1	
Signal-to-noise ratio of output signals; note 11	S/N	>	62	dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)		typ. <	40 150	mV mV
Residual 8,8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		typ. <	75 150	mV mV
Output impedance of RGB outputs	$\lvert Z_{12,14,16\text{-}27} \rvert$	typ.	50	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		<	−3	dB

Signal insertion (pins 13,15 and 17)

Input signals (peak-to-peak value) for an RGB output voltage of 5 V peak-to-peak	$V_{13,15,17\text{-}27(p\text{-}p)}$	typ.	1 0,85 to 1,1	V V
Difference between the black levels of the RGB signals and the inserted signals at the output; note 9	ΔV	<	260	mV
Output rise time	t_r	typ. <	40 80	ns ns
Differential delay time for the three channels	t_d	typ. <	0 40	ns ns
Input current	$I_{13,15,17}$	<	10	μA

Data blanking (pin 9)

Input voltage for no data insertion	$V_{9\text{-}27}$	<	0,4	V
Input voltage for data insertion	$V_{9\text{-}27}$	>	0,9	V
Maximum input voltage	$V_{9\text{-}27}$	<	3	V
Delay of data blanking	t_d	<	20	ns
Input current	I_9	<	35	μA
Input impedance	$\lvert Z_{9\text{-}27} \rvert$	typ.	10	kΩ
Suppression of the internal RGB signals when $V_{9\text{-}27} > 0,9$ V		>	46	dB

Sandcastle input (pin 8)

Level at which the RGB blanking is activated	$V_{8\text{-}27}$	typ. 1,5 V 1 to 2 V
Level at which burst gating and clamping pulse are separated	$V_{8\text{-}27}$	typ. 7,0 V 6,5 to 7,5 V
Delay between black level clamping and burst gating pulse	t_d	typ. 0,4 μs
Input current for:		
$V_{8\text{-}27} = 0$ to 1 V	$-I_8$	< 1 mA
$V_{8\text{-}27} = 1$ to 8,5 V	I_8	typ. 20 μA
$V_{8\text{-}27} = 8{,}5$ to 12 V	I_8	< 2 mA

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal for a colour bar with 75% saturation, so chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast −3 dB and nominal saturation as the maximum saturation −6 dB.
4. All frequency variations are referred to the 4,4 MHz carrier frequency.
5. For ± 400 Hz deviation of the oscillator frequency.
6. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
7. When this level is exceeded, the amplitude of the output signal is reduced via a discharge of the capacitor at pin 7 (contrast control). The start of the peak white limiting action has a delay of one line period.
8. The variation of the black level depends directly on the gain of each channel during brightness control in the three channels. As a consequence, the black levels at the outputs (for output levels above or below 3 V) can have a difference which exceeds 200 mV. Because the amplitude and the black level change with brightness control have a direct relationship, no discolouring can occur, caused by adjustment of contrast and brightness.
9. This difference occurs when the source impedance of the data signal inputs is 150 Ω and the black level clamp pulse duration is 4 μs (sandcastle pulse). A lower difference is obtained when the impedance is lower.
10. Cross-coupling is measured under the following condition. Input signals nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
11. The signal-to-noise ratio is specified as peak-to-peak signal with respect to r.m.s. noise.

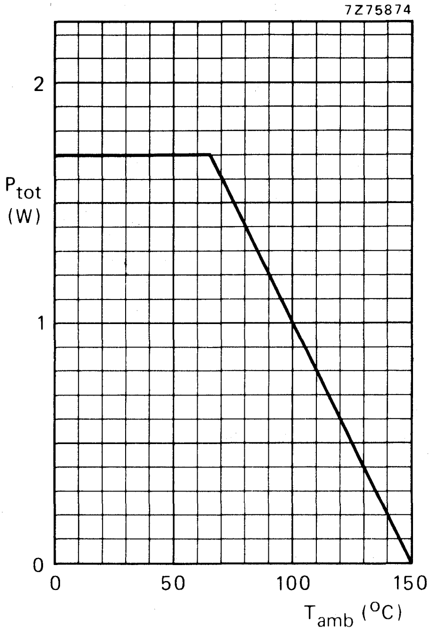


Fig. 2 Power derating curve.

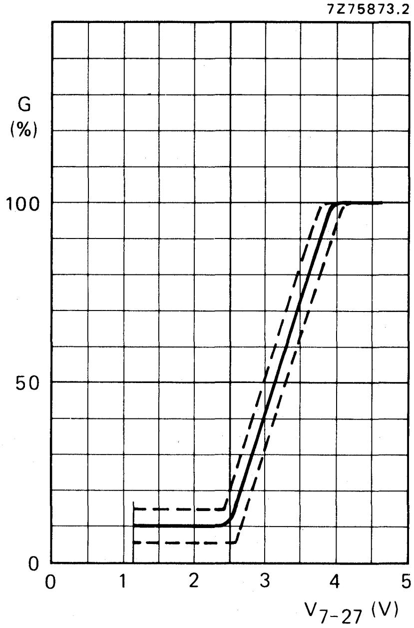


Fig. 3 Contrast control voltage range.

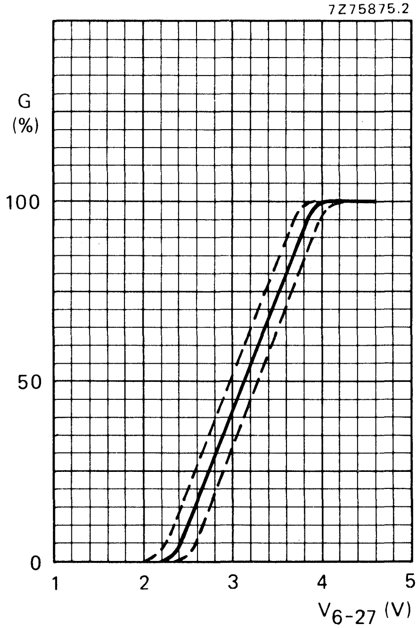


Fig. 4 Saturation control voltage range.

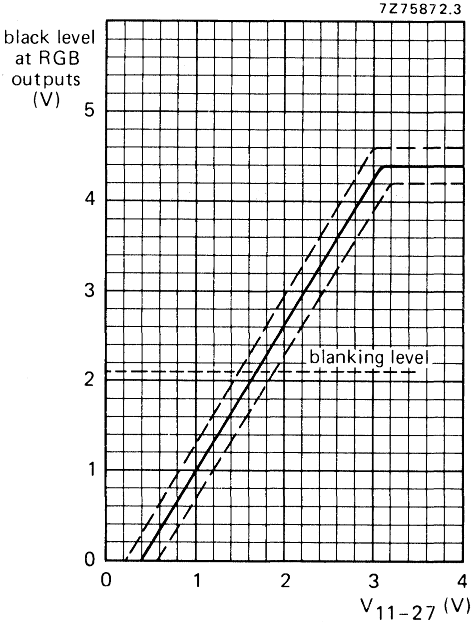


Fig. 5 Brightness control voltage range.

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION

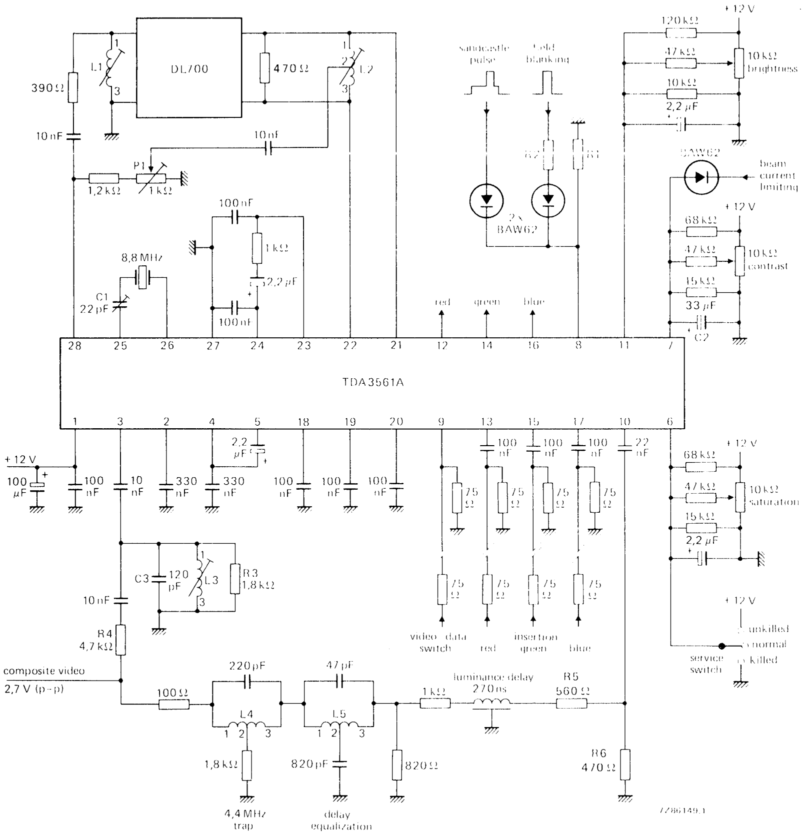


Fig. 6 Application circuit.

Adjustments (see Fig. 6)

C1	8,8 MHz oscillator	
L1	phase delay line	= 10,7 µH
L2	nominal value	= 10,7 µH
L3	4,4 MHz chrominance input filter	= 10,7 µH = L1
L4	4,4 MHz trap in luminance signal line	= 5,6 µH
L5	delay equalization	= 66,1 µH
P1	amplitude of direct chroma singal	

R1, R2: field blanking $\frac{R1}{R1 + R2}$ x field blanking amplitude 2,0 V to 6,5 V.

For a video input voltage of 1 V peak-to-peak: R3 can be omitted; R4 = 1 kΩ; R5 must be short-circuited; R6 = 1 kΩ.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. + 12 V power supply

The circuit gives good operation in a supply voltage range between 8 and 13,2 V provided that the supply voltage for the controls is equal to the supply voltage for the TDA3561A. All signal and control levels have a linear dependency on the supply voltage. The current taken by the device at 12 V is typically 85 mA. It is linearly dependent on the supply voltage.

2. Control voltage for identification

This pin requires a detection capacitor of about 330 nF for correct operation. The voltages available under various signal conditions are given in the specification.

3. Chrominance input

The chroma signal must be a.c.-coupled to the input. Its amplitude must be between 55 mV and 1100 mV peak-to-peak (25 mV to 500 mV peak-to-peak burst signal). All figures for the chroma signals are based on a colour bar signal with 75% saturation, that is the burst-to-chroma ratio of the input signal is 1 : 2,25.

4. Reference voltage A.C.C. detector

This pin must be decoupled by a capacitor of about 330 nF. The voltage at this pin is 4,9 V.

5. Control voltage A.C.C.

The A.C.C. is obtained by synchronous detection of the burst signal followed by a peak detector. A good noise immunity is obtained in this way and an increase of the colour for weak input signals is prevented. The recommended capacitor value at this pin is 2,2 μF.

6. Saturation control

The saturation control range is in excess of 50 dB. The control voltage range is 2 to 4 V. Saturation control is a linear function of the control voltage.

When the colour killer is active, the saturation control voltage is reduced to a low level if the resistance of the external saturation control network is sufficiently high. Then the chroma amplifier supplies no signal to the demodulator. Colour switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply the colour killer circuit is overruled so that the colour signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also pins 25 and 26).

7. Contrast control

The contrast control range is 20 dB for a control voltage change from + 2 to + 4 V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1 V or less. If one or more output signals surpasses the level of 9 V the peak white limiter circuit becomes active and reduces the output signals via the contrast control by discharging C2 via an internal current sink.

8. Sandcastle and field blanking input

The output signals are blanked if the amplitude of the input pulse is between 2 and 6,5 V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7,5 V.
The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of video signal on the sync pulse. The width should be about 4 μs for proper A.C.C. operation.

9. Video-data switching

The insertion circuit is activated by means of this input by an input pulse between 1 V and 2 V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted this pin should be connected to the negative supply. The switching times are very short (< 20 ns) to avoid coloured edges of the inserted signals on the screen.

10. Luminance signal input

The input signal should have a peak-to-peak amplitude of 0,45 V (peak white to sync) to obtain a black-white output signal of 5 V at nominal contrast. It must be a.c.-coupled to the input by a capacitor of about 22 nF. The signal is clamped at the input to an internal reference voltage.
A 1 kΩ luminance delay line can be applied because the luminance input impedance is made very high. Consequently the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally the coupling capacitor value may be small.

11. Brightness control

The black level of the RGB outputs can be set by the voltage on this pin (see Fig. 5). The black level can be set higher than 4 V however the available output signal amplitude is reduced (see pin 7). Brightness control also operates on the black level of the inserted signals.

12, 14, 16. RGB outputs

The output circuits for red, green and blue are identical. Output signals are 5,25 V (R, G and B) at nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2,1 V. The peak white level is limited to 9,3 V. When this level exceeded the output signal amplitude is reduced via the contrast control (see pin 7).

13, 15, 17. Inputs for external RGB signals

The external signals must be a.c.-coupled to the inputs via a coupling capacitor of about 100 nF. Source impedance should not exceed 150 Ω. The input signal required for a 5 V peak-to-peak output signal is 1 V peak -to-peak. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used the coupling capacitors have to be connected to the negative supply.

18, 19, 20. Black level clamp capacitors

The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100 nF.

21, 22. Inputs (B-Y) and (R-Y) demodulators

The input signal is automatically fixed to the required level by means of the burst phase detector and A.C.C. generator which are connected to pin 21 and pin 22. As the burst (applied differentially to those pins) is kept constant by the A.C.C., the colour difference signals automatically have the correct value.

APPLICATION INFORMATION (continued)

23, 24. Burst phase detector outputs

At these pins the output of the burst phase detector is filtered and controls the reference oscillator. An adequate catching range is obtained with the time constants given in the application circuit (see Fig. 6).

25, 26. Reference oscillator

The frequency of the oscillator is adjusted by the variable capacitor C1. For frequency adjustment interconnect pin 21 and pin 22. The frequency can be measured by connecting a suitable frequency counter to pin 25.

28. Output of the chroma amplifier

Both burst and chroma signals are available at the output. The burst-to-chroma ratio at the output is identical to that at the input for nominal control settings. The burst signal is not affected by the controls. The amplitude of the input signal to the demodulator is kept constant by the A.C.C. Therefore the output signal at pin 28 will depend on the signal loss in the delay line.

PAL/NTSC DECODER

GENERAL DESCRIPTION

The TDA3562A is a monolithic integrated decoder for the PAL and/or NTSC colour television standards. It combines all functions required for the identification and demodulation of PAL/NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 4 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. Teletext/broadcast Antiope), channel number display, etc.

Features

- A black-current stabilizer which controls the black-currents of the three electron-guns to a level low enough to omit the black-level adjustment
- Contrast control of inserted RGB signals
- No black-level disturbance when non-synchronized external RGB signals are available on the inputs
- NTSC capability with hue control

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_P = V_{1\text{-}27}$	typ.	12	V
Supply current (pin 1)	$I_P = I_l$	typ.	80	mA
Luminance amplifier (pin 8)				
Input voltage (peak-to-peak value)	$V_{8\text{-}27(p\text{-}p)}$	typ.	450	mV
Contrast control range		typ.	20	dB
Chrominance amplifier (pin 4)				
Input voltage range (peak-to-peak value)	$V_{4\text{-}27(p\text{-}p)}$		40 to 1100	mV
Saturation control range		min.	50	dB
RGB matrix and amplifiers				
Output voltage at nominal luminance and contrast (peak-to-peak value)	$V_{13,15,17\text{-}27(p\text{-}p)}$	typ.	4	V
Data insertion				
Input signals (peak-to-peak value)	$V_{12,14,16\text{-}27(p\text{-}p)}$	typ.	1	V
Data blanking (pin 9)				
Input voltage for data insertion	$V_{9\text{-}27}$	min.	0,9	V
Sandcastle input (pin 7)				
Blanking input voltage	$V_{7\text{-}27}$	typ.	1,5	V
Burst gating and clamping input voltage	$V_{7\text{-}27}$	typ.	7	V

PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT-117).

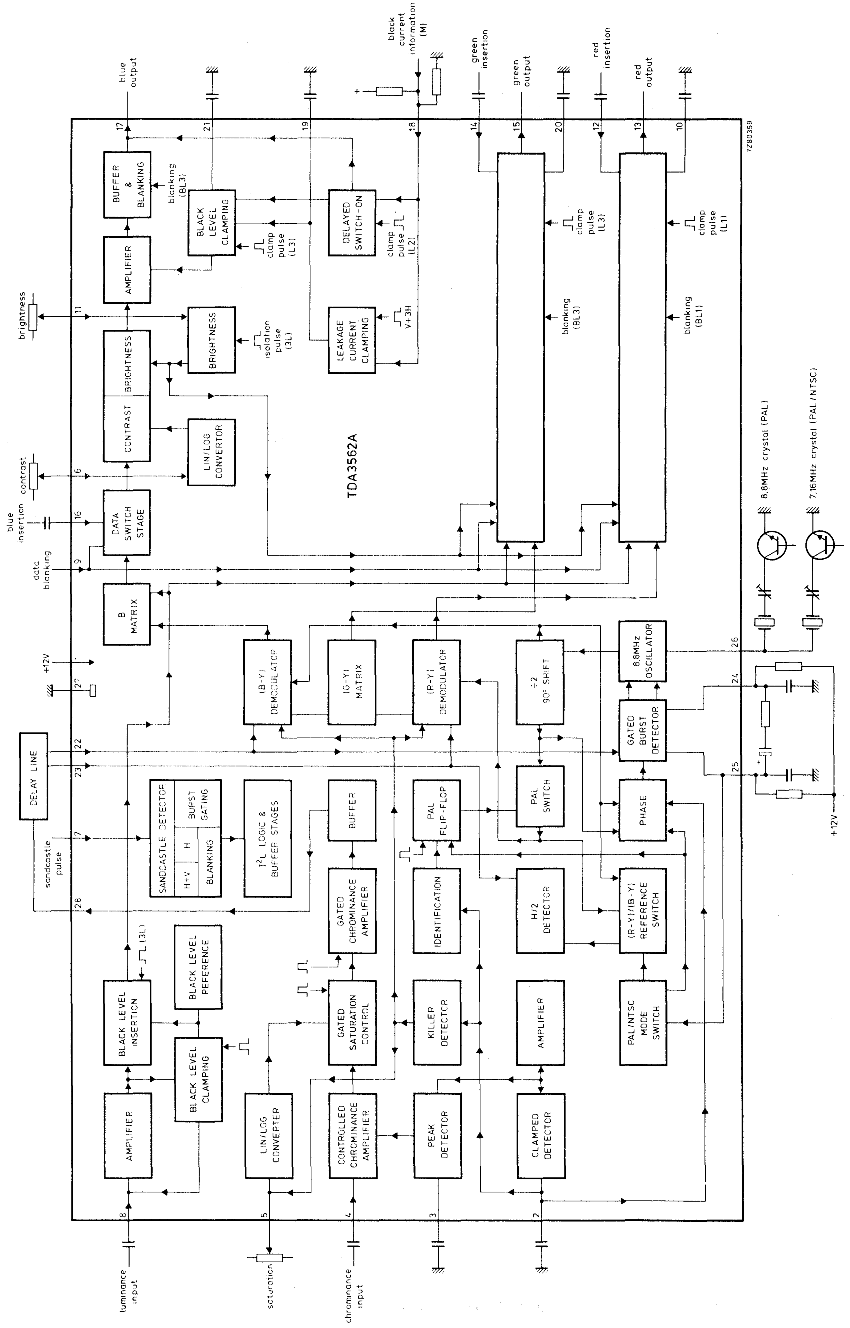


Fig. 1 Block diagram; for explanation of pulse mnemonics see Fig. 6.

FUNCTIONAL DESCRIPTION

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal is a.c. coupled to the input (pin 8). After amplification, the black level at the output of the preamplifier is clamped to a fixed d.c. level by the black level clamping circuit.

During three line periods after vertical blanking, the luminance signal is blanked out and the black level reference voltage is inserted by a switching circuit. This black level reference voltage is controlled via pin 11 (brightness). At the same time the RGB signals are clamped. Noise and residual signals have no influence during clamping thus simple internal clamping circuitry is used.

Chrominance amplifiers

The chrominance amplifier has an asymmetrical input. The input signal must be a.c. coupled (pin 4) and have a minimum amplitude of 40 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal must not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the saturation control stage. Saturation is linear controlled via pin 5. The control voltage range is 2 to 4 V, the input impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by saturation control. The signal is then fed to a gated amplifier which has a 12 dB higher gain during the chrominance signal. As a result the signal at the output (pin 28) has a burst to chrominance ratio which is 6 dB lower than that of the input signal when the saturation control is set at −6 dB. The chrominance output signal is fed to the delay line and, after matrixing, is applied to the demodulator input pins (pins 22 and 23). These signals are fed to the burst phase detector.

Oscillator and identification circuit

The burst phase detector is gated with the narrow part of the sandcastle pulse (pin 7). In the detector the (R-Y) and (B-Y) signals are added to provide the composite burst signal again. This composite signal is compared with the oscillator signal divided-by-2 (R-Y) reference signal. The control voltage is available at pins 24 and 25, and is also applied to the 8,8 MHz oscillator. The 4,4 MHz signal is obtained via the divide-by-2 circuit, which generates both the (B-Y) and (R-Y) reference signals and provides a 90° phase shift between them.

The flip-flop is driven by pulses obtained from the sandcastle detector. For the identification of the phase at PAL mode, the (R-Y) reference signal coming from the PAL switch, is compared to the vertical signal (R-Y) of the PAL delay line. This is carried out in the H/2 detector, which is gated during burst. When the phase is incorrect, the flip-flop gets a reset from the identification circuit. When the phase is correct, the output voltage of the H/2 detector is directly related to the burst amplitude so that this voltage can be used for the a.c.c. To avoid 'blooming-up' of the picture under weak input signal conditions the a.c.c. voltage is generated by peak detection of the H/2 detector output signal.

The killer and identification circuits get their information from a gated output signal of the H/2 detector. Killing is obtained via the saturation control stage and the demodulators to obtain good suppression. The time constant of the saturation control (pin 5) provides a delayed switch-on after killing.

Adjustment of the oscillator is achieved by variation of the burst phase detector load resistance between pins 24 and 25 (see Fig. 7). With this application the trimmer capacitor in series with the 8,8 MHz crystal (pin 26) can be replaced by a fixed value capacitor to compensate for unbalance of the phase detector.

FUNCTIONAL DESCRIPTION (continued)

Demodulator

The (R-Y) and (B-Y) demodulators are driven by the colour difference signals from the delay-line matrix circuit and the reference signals from the 8,8 MHz divider circuit. The (R-Y) reference signal is fed via the PAL-switch. The output signals are fed to the R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G-matrix. The demodulation circuits are killed and blanked by by-passing the input signals.

NTSC mode

The NTSC mode is switched on when the voltage at the burst phase detector outputs (pins 24 and 25) is adjusted below 9 V. To ensure reliable application the phase detector load resistors are external. When the TDA3562A is used only for PAL these two 33 kΩ resistors must be connected to + 12 V (see Fig. 7). For PAL/NTSC application the value of each resistor must be reduced to 10 kΩ and connected to the slider of a potentiometer (see Fig. 8). The switching transistor brings the voltage at pins 24 and 25 below 9 V which switches the circuit to the NTSC mode. The position of the PAL flip-flop ensures that the correct phase of the (R-Y) reference signal is supplied to the (R-Y) demodulator. The drive to the H/2 detector is now provided by the (B-Y) reference signal. In the PAL mode it is driven by the (R-Y) reference signal.

Hue control is realized by changing the phase of the reference drive to the burst phase detector. This is achieved by varying the voltage at pins 24 and 25 between 7,5 and 8,5 V, nominal position 8,0 V. The hue control characteristic is shown in Fig. 5.

RGB matrix and amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described.

The luminance and the colour difference signals are added in the matrix circuit to obtain the colour signal, which is then fed to the contrast control stage. The contrast control voltage is supplied to pin 6 (high-input impedance). The control range is +5 dB to −15 dB nominal. The relationship between the control voltage and the gain is linear (see Fig. 2).

During the 3-line period after blanking a pulse is inserted at the output of the contrast control stage. The amplitude of this pulse is varied by a control voltage at pin 11. This applies a variable offset to the normal black level, thus providing brightness control. The brightness control range is 1 V to 3 V.

While this offset level is present, the 'black-current' input impedance (pin 18) is high and the internal clamp circuit is activated. The clamp circuit then compares the reference voltage at pin 19 with the voltage developed across the external resistor network R_A and R_B (pin 18) which is provided by picture tube beam current. The output of the comparator is stored in capacitors connected from pins 10, 20 and 21 to ground which controls the black level at the output. The reference voltage is composed by the resistor divider network and the leakage current of the picture tube into this bleeder. During vertical blanking, this voltage is stored in the capacitor connected to pin 19, which ensures that the leakage current of the CRT does not influence the black current measurement.

The RGB output signals can never exceed a level of 10 V. When the signal tends to exceed this level the output signal is clipped. The black level at the outputs (pins 13, 15 and 17) will be about 3 V. This level depends on the spread of the guns of the picture tube. If a beam current stabilizer is not used it is possible to stabilize the black levels at the outputs, which in this application must be connected to the black current measuring input (pin 18) via a resistor network.

Data insertion

Each colour amplifier has a separate input for data insertion. A 1 V peak-to-peak input signal provides a 4 V peak-to-peak output signal. To avoid the 'black-level' of the inserted signal differing from the black level of the normal video signal, the data is clamped to the black level of the luminance signal. Therefore a.c. coupling is required for the data inputs. To avoid a disturbance of the blanking level due to the clamping circuit, the source impedance of the driver circuit must not exceed 150 Ω.

The data insertion circuit is activated by the data blanking input (pin 9). When the voltage at this pin exceeds a level of 0,9 V, the RGB matrix circuits are switched off and the data amplifiers are switched on. To avoid coloured edges, the data blanking switching time is short.

The amplitude of the data output signals is controlled by the contrast control at pin 6. The black level is equal to the video black level and can be varied between 2 and 4 V (nominal condition) by the brightness control voltage at pin 11.

Non-synchronized data signals do not disturb the black level of the internal signals.

Blanking of RGB and data signals

Both the RGB and data signals can be blanked via the sandcastle input (pin 7). A slicing level of 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking a level of + 1 V is available at the output.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1\text{-}27}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	=	40	K/W

CHARACTERISTICS

$V_P = V_{1\text{-}27} = 12$ V; $T_{amb} = 25$ V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	$V_P = V_{1\text{-}27}$	10,8	12	13,2	V
Supply current	$I_P = I_1$	–	80	110	mA
Total power dissipation	P_{tot}	–	0,95	1,3	W
Luminance amplifier (pin 8)					
Input voltage (note 1) (peak-to-peak value)	$V_{8\text{-}27(p\text{-}p)}$	–	0,45	–	V
Input level before clipping	$V_{8\text{-}27}$	–	–	1	V
Input current	I_8	–	0,1	1	μA
Contrast control range (see Fig. 2)		–15	–	+5	dB
Input current contrast control	I_7	–	–	15	μA
Chrominance amplifier (pin 4)					
Input voltage (note 2) (peak-to-peak value)	$V_{4\text{-}27(p\text{-}p)}$	40	390	1100	mV
Input impedance	$\lvert Z_{4\text{-}27}\rvert$	–	10	–	kΩ
Input capacitance	$C_{4\text{-}27}$	–	–	6,5	pF
A.C.C. control range		30	–	–	dB
Change of the burst signal at the output over the whole control range		–	–	1	dB
Gain at nominal contrast/saturation pin 4 to pin 28 (note 3)		34	–	–	dB
Chrominance to burst ratio at nominal saturation (notes 2 and 3) at pin 28		–	12	–	dB
Maximum output voltage (peak-to-peak value); $R_L = 2$ kΩ	$V_{28\text{-}27(p\text{-}p)}$	4	5	–	V
Distortion of chrominance amplifier at $V_{28\text{-}27(p\text{-}p)} = 2$ V (output) up to $V_{4\text{-}27(p\text{-}p)} = 1$ V (input)	d	–	–	5	%
Frequency response between 0 and 5 MHz	$\alpha_{28\text{-}4}$	–	–	–2	dB
Saturation control range (see Fig. 3)		50	–	–	dB
Input current saturation control (pin 5)	I_5	–	–	20	μA
Cross-coupling between luminance and chrominance amplifier (note 4)		–	–	–46	dB
Signal-to-noise ratio at nominal input signal (note 5)	S/N	56	–	–	dB
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\varphi$	–	–	± 5	deg
Output impedance of chrominance amplifier	$\lvert Z_{28\text{-}27}\rvert$	–	10	–	Ω
Output current	I_{28}	–	–	15	mA

parameter	symbol	min.	typ.	max.	unit
Reference part					
Phase-locked-loop catching range (note 6)	Δf	500	700	–	Hz
phase shift for ± 400 Hz deviation of f_{osc} (note 6)	Δφ	–	–	5	deg
Oscillator temperature coefficient of oscillator frequency (note 6)	TC_{osc}	–	−2	–	Hz/K
frequency variation when supply voltage increases from 10 V to 13,2 V (note 6)	Δf_{osc}	–	40	–	Hz
input resistance (pin 26)	$R_{26\text{-}27}$	–	400	–	Ω
input capacitance (pin 26)	$C_{26\text{-}27}$	–	–	10	pF
A.C.C. generation (pin 2) control voltage at nominal input signal	$V_{2\text{-}27}$	–	4,5	–	V
control voltage without chrominance input	$V_{2\text{-}27}$	–	2,0	–	V
colour-off voltage	$V_{2\text{-}27}$	–	2,8	–	V
colour-on voltage	$V_{2\text{-}27}$	–	3,0	–	V
identification-on voltage	$V_{2\text{-}27}$	–	1,7	–	V
change in burst amplitude with temperature		–	0,1	0,25	%/K
voltage at pin 3 at nominal input signal	$V_{3\text{-}27}$	–	5,1	–	V
Demodulator part					
Input burst signal amplitude (peak-to-peak value) between pins 23 and 27 (note 7)	$V_{23\text{-}27(p\text{-}p)}$	–	80	–	mV
Input impedance between pins 22 or 23 and 27	$\lvert Z_{22\text{-}27/23\text{-}27}\rvert$	–	1	–	kΩ
Ratio of demodulated signals (note 8) (B-Y)/(R-Y)	$\frac{V_{17\text{-}27}}{V_{13\text{-}27}}$	–	1,78 ± 10%	–	
(G-Y)/(R-Y); no (B-Y) signal	$\frac{V_{15\text{-}27}}{V_{13\text{-}27}}$	–	−0,51 ± 10%	–	
(G-Y)/(B-Y); no (R-Y) signal	$\frac{V_{15\text{-}27}}{V_{17\text{-}27}}$	–	−0,19 ± 25%	–	
Frequency response between 0 and 1 MHz		–	–	−3	dB
Cross-talk between colour difference signals		40	–	–	dB
Phase difference between (R-Y) signal and (R-Y) reference signal	Δφ	–	–	5	deg
Phase difference between (R-Y) and (B-Y) reference signals	Δφ	85	90	95	deg

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB matrix and amplifiers					
Output voltage (peak-to-peak value) at nominal luminance/contrast (black-to-white) (note 3)	$V_{13,15,17\text{-}27(p\text{-}p)}$	3,5	4	4,5	V
Output voltage at pin 13 (peak-to-peak value) at nominal contrast/saturation and no luminance signal to (R-Y)	$V_{13\text{-}27(p\text{-}p)}$	–	4,2	–	V
Maximum peak-white level	$V_{13,15,17(m)}$	9,7	10	10,3	V
Available output current (pins 13,15,17)	$I_{13,15,17}$	10	–	–	mA
Difference between black level and measuring level at the output for a brightness control voltage at pin 11 of 2 V (note 9)	$\Delta V_{13,15,17\text{-}27}$	–	0	–	V
Difference in black level between the three channels without black current stabilization (note 10)		–	–	100	mV
Control range of black-current stabilization at V_{b1} = 3 V; $V_{11\text{-}27}$ = 2 V		–	–	± 2	V
Black level shift with vision contents		–	–	40	mV
Brightness control voltage range		see Fig. 4			
Brightness control input current	I_{11}	–	–	5	μA
Variation of black level with temperature	$\Delta V/\Delta T$	–	0	–	mV/K
Variation of black level with contrast*	ΔV	–	–	100	mV
Relative spread between the R, G and B output signals		–	–	10	%
Relative black-level variation between the three channels during variation of contrast, brightness and supply voltage (± 10%)		–	0	20	mV
Differential black-level drift over a temperature range of 40 °C*		–	0	20	mV
Blanking level at the RGB outputs		–	0,95	1,1	V
Difference in blanking level of the three channels		–	0	–	mV
Differential drift of the blanking levels over a temperature range of 40 °C		–	0	–	mV
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	–	1	–	
Tracking of contrast control between the three channels over a control range at 10 dB		–	–	0,5	dB

* With respect to the measuring pulses.

parameter	symbol	min.	typ.	max.	unit
Output signal during the clamp pulse (3L) after switch-on		7,5	–	–	V
Signal-to-noise ratio of output signals (note 5)	S/N	62	–	–	dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)		–	–	50	mV
Residual 8,8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		–	–	150	mV
Output impedance of RGB outputs	$\lvert Z_{13,15,17\text{-}27} \rvert$	–	50	–	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		–	–1	–3	dB
Current source of output stage		2	3	–	mA
Difference of black level at the three outputs at nominal brightness*		–	–	10	mV
Tracking of brightness control		–	–	2	%
Data insertion (pins 12, 14 and 16)					
Input signals (peak-to-peak value) for an RGB output voltage of 4 V (peak-to-peak) at nominal contrast	$V_{12,14,16\text{-}27(p\text{-}p)}$	0,9	1	1,1	V
Difference between the black levels of the RGB signals and the inserted signals at the output (note 11)	ΔV	–	–	100	mV
Output rise time	t_r	–	–	80	ns
Differential delay time for the three channels	t_d	–	0	40	ns
Input current	$I_{12,14,16}$	–	–	10	μA
Data blanking (pin 9)					
Input voltage for no data insertion	$V_{9\text{-}27}$	–	–	0,4	V
Input voltage for data insertion	$V_{9\text{-}27}$	0,9	–	–	V
Maximum input voltage	$V_{9\text{-}27(m)}$	–	–	3	V
Delay of data blanking	t_d	–	–	20	ns
Input resistance	$R_{9\text{-}27}$	7	10	13	kΩ
Suppression of the internal RGB signals when $V_{9\text{-}27} > 0{,}9$ V		46	–	–	dB

DEVELOPMENT SAMPLE DATA

---

* With respect to the measuring pulses.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Sandcastle input (pin 7)					
Level at which the RGB blanking is activated	$V_{7\text{-}27}$	1	1,5	2	V
Level at which the horizontal pulses are separated	$V_{7\text{-}27}$	3	3,5	4	V
Level at which burst gating and clamping pulse are separated	$V_{7\text{-}27}$	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse	t_d	–	0,6	–	μs
Input current					
at $V_{7\text{-}27}$ = 0 to 1 V	$-I_7$	–	–	1	mA
at $V_{7\text{-}27}$ = 1 to 8,5 V	I_7	–	50	–	μA
at $V_{7\text{-}27}$ = 8,5 to 12 V	I_7	–	–	2	mA
Black current stabilization (pin 18)					
D.C. bias voltage	$V_{18\text{-}27}$	3,5	5	7,0	V
Difference between input voltage for 'black' current and leakage current	ΔV	–	0,5	–	V
Input current during 'black' current	I_{18}	–	–	1	μA
Input current during scan	I_{18}	–	–	10	mA
Internal limiting at pin 10	$V_{10\text{-}27}$	–	9	–	V
Switching threshold for 'black' current control ON	$V_{1\text{-}27}$	–	8	–	V
Input resistance during scan	$R_{1\text{-}27}$	–	1,5	–	kΩ
D.C. input current during scan at pins 10, 20 and 21	$I_{10,20,21}$	–	–	50	nA
Maximum charge/discharge current during measuring time at pins 10,19,20 and 21	$I_{c/d}$	–	10	–	mA
NTSC					
Level at which the PAL/NTSC switch is activated (pins 24 and 25)	$V_{24\text{-}25}$	–	9	–	V
Average output current (note 12)	I_{24+25}	75	90	105	μA
Hue control			see Fig. 5		

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75% saturation; chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast –5 dB and nominal saturation as the maximum saturation –6 dB.
4. Cross coupling is measured under the following condition: input signal nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to r.m.s. noise.
6. All frequency variations are referred to 4,4 MHz carrier frequency.
7. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
8. The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal. This also applies to the (B-Y) signals.
9. This value depends on the gain setting of the RGB output amplifiers and the drift of the picture tube guns. Higher black level values are possible (up to 5 V) but in that application the amplitude of the output signal is reduced.
10. The variation of the black-level during brightness control in the three different channels is directly dependent on the gain of each channel. Discolouration during adjustments of contrast and brightness does not occur because amplitude and the black-level change with brightness control are directly related.
11. This difference occurs when the source impedance of the data signals is 150 Ω and the black level clamp pulse width is 4 μs (sandcastle pulse). For a lower impedance the difference will be lower.
12. The voltage at pins 24 and 25 can be changed by connecting the load resistors (10 kΩ in this application) to the slider bar of the hue control potentiometer (see Fig. 8). When the transistor is switched on, the voltage at pins 24 and 25 is reduced below 9 V, and the circuit is switched to NTSC mode.

DEVELOPMENT SAMPLE DATA

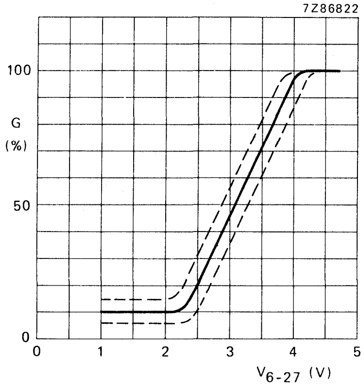


Fig. 2 Contrast control voltage range.

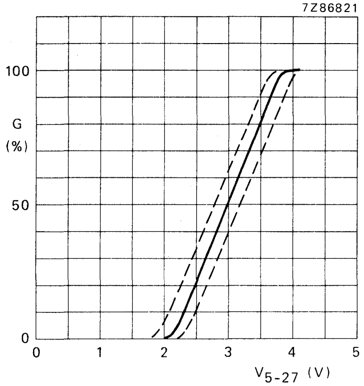


Fig. 3 Saturation control voltage range.

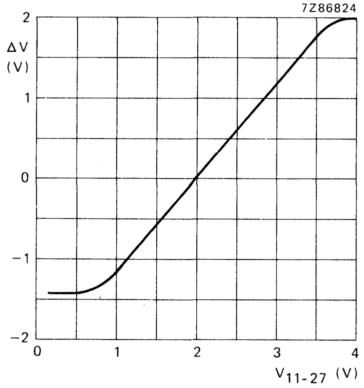


Fig. 4 Difference between black level and measuring level at the RGB outputs (ΔV) as a function of the brightness control input voltage (V_{11-27}).

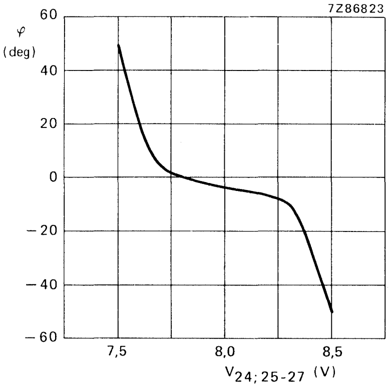


Fig. 5 Hue control voltage range.

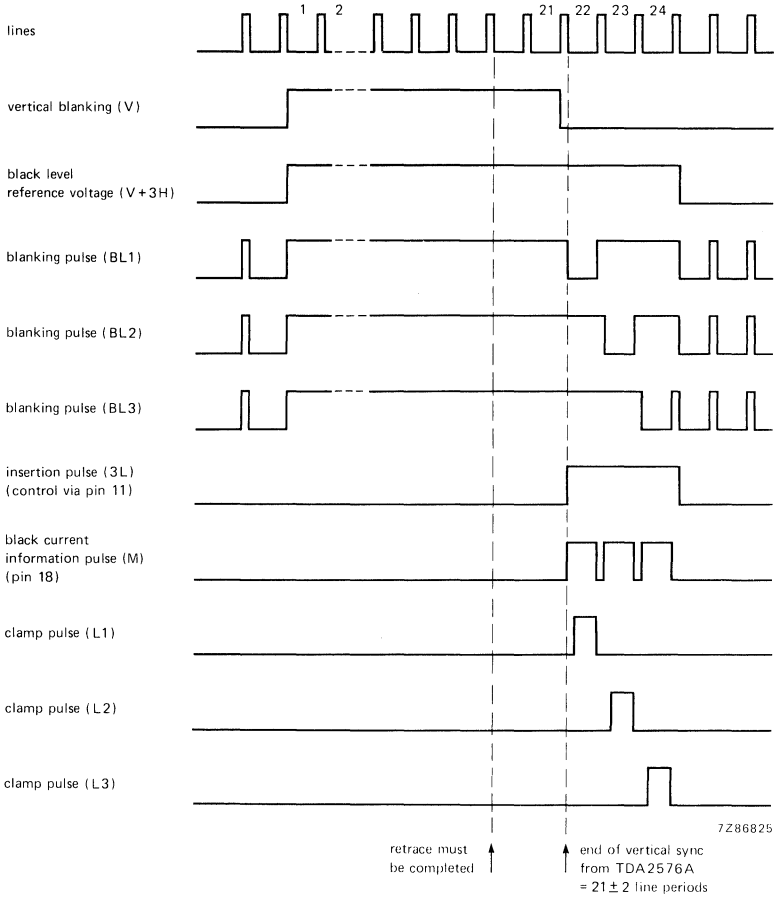


Fig. 6 Timing diagram for black-current stabilizing.

APPLICATION INFORMATION

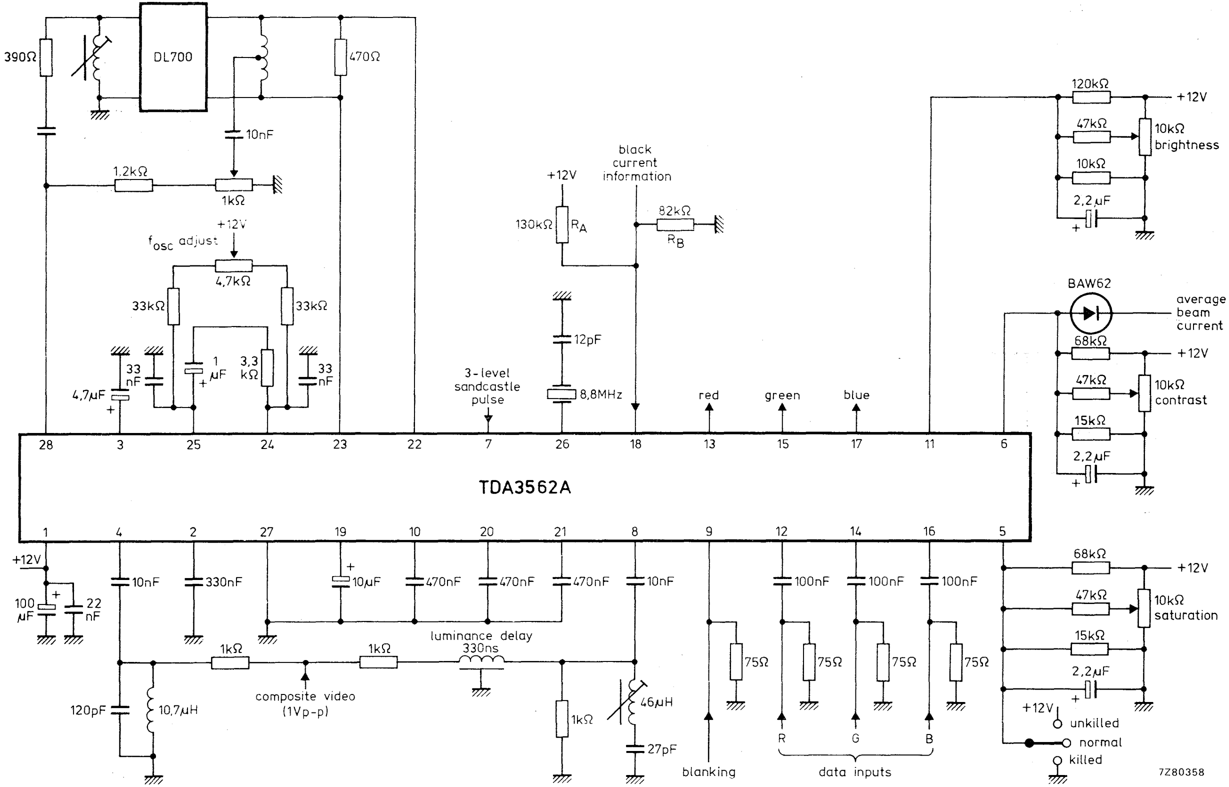


Fig. 7 Application diagram showing the TDA3562A for a PAL decoder.

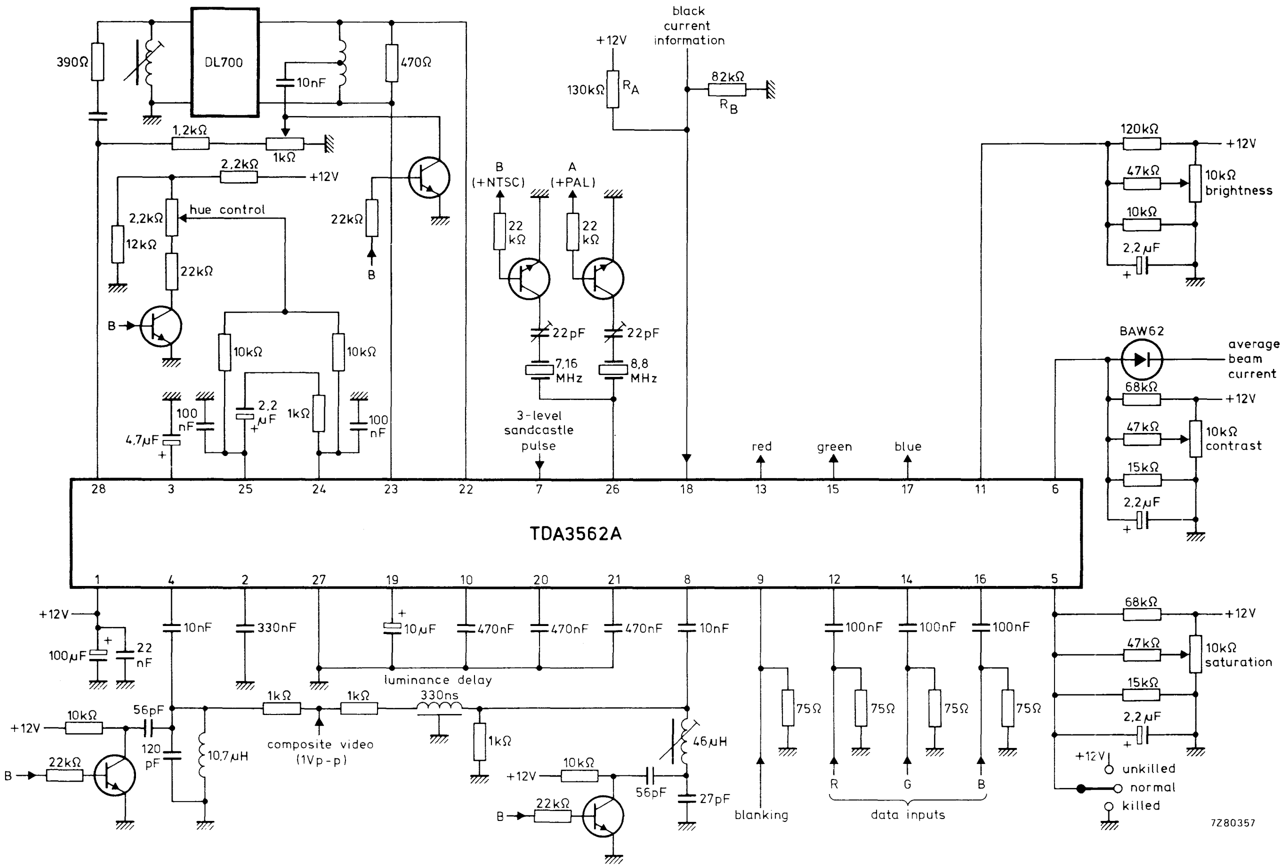


Fig. 8 Application diagram showing the TDA3562A for a PAL/NTSC decoder.

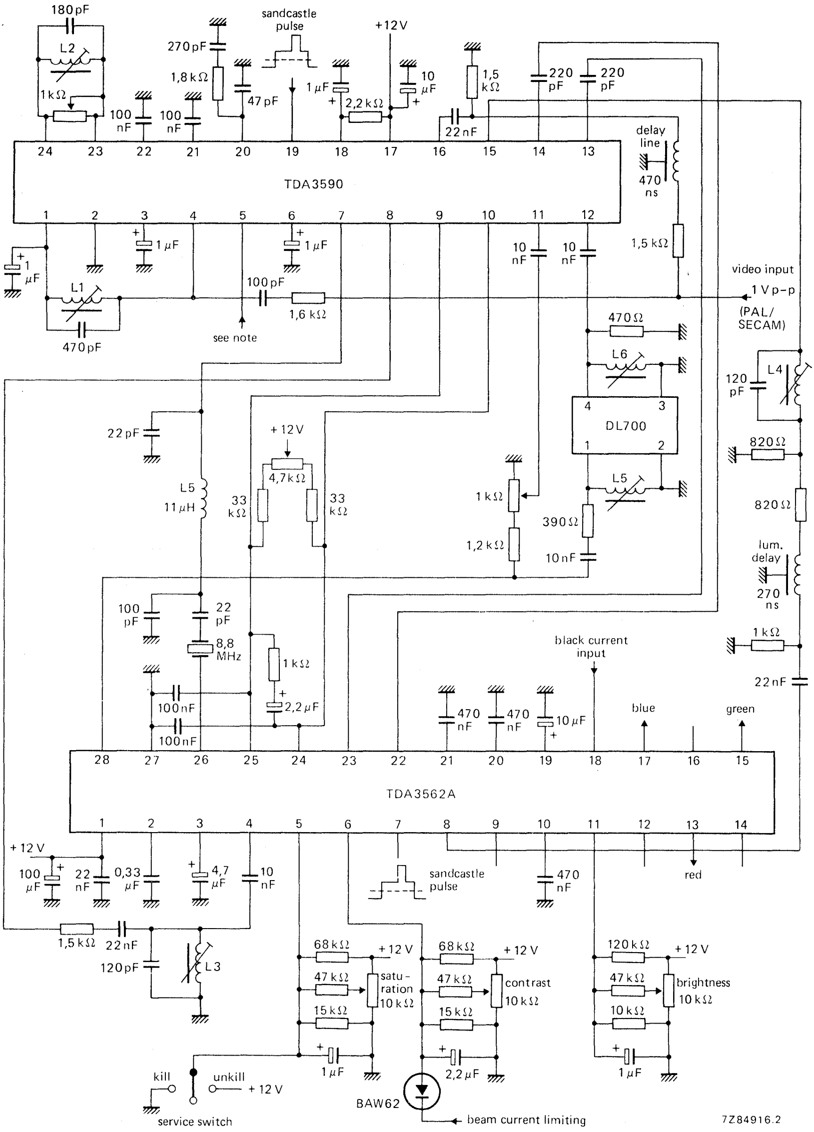


Fig. 9 PAL/SECAM application circuit diagram using the TDA3590 and TDA3562A.

Note to pin 5 TDA3590:

$V_{5\text{-}2} < 1$ V; horizontal identification and black level clamping.

$V_{5\text{-}2} > 11$ V; vertical identification and artificial black level.

$V_{5\text{-}2} =$ 5 to 7 V; horizontal identification and artificial black level.

NTSC DECODER

GENERAL DESCRIPTION

The TDA3563 is a monolithic integrated colour decoder for the NTSC standard. It combines all functions required for the identification and demodulation of NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply signals up to 5,3 V peak-to-peak (picture information) enabling direct drive of the output stages. The circuit also contains inputs for data insertion, analogue as well as digital, which can be used for Teletext information, channel number display, etc.

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_P = V_{1\text{-}27}$	typ.	12	V
Supply current (pin 1)	$I_P = I_1$	typ.	85	mA
Luminance input signal (peak-to-peak value)	$V_{10\text{-}27(p\text{-}p)}$	typ.	0,45	V
Chrominance input signal (peak-to-peak value)	$V_{3\text{-}27(p\text{-}p)}$		55 to 1100	mV
Data input signals (peak-to-peak value)	$V_{13;15;17\text{-}27(p\text{-}p)}$	typ.	1	V
RGB output signals at nominal contrast and saturation (peak-to-peak value)	$V_{12;14;16\text{-}27(p\text{-}p)}$	typ.	5,3	V
Contrast control range		typ.	20	dB
Saturation control range		min.	50	dB
Input voltage for fast video-data signal switching	$V_{9\text{-}27}$	min.	0,9	V
Blanking input voltage	$V_{8\text{-}27}$	typ.	1,5	V
Burst gating and black-level gating input voltage	$V_{8\text{-}27}$	typ.	7	V

PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT-117).

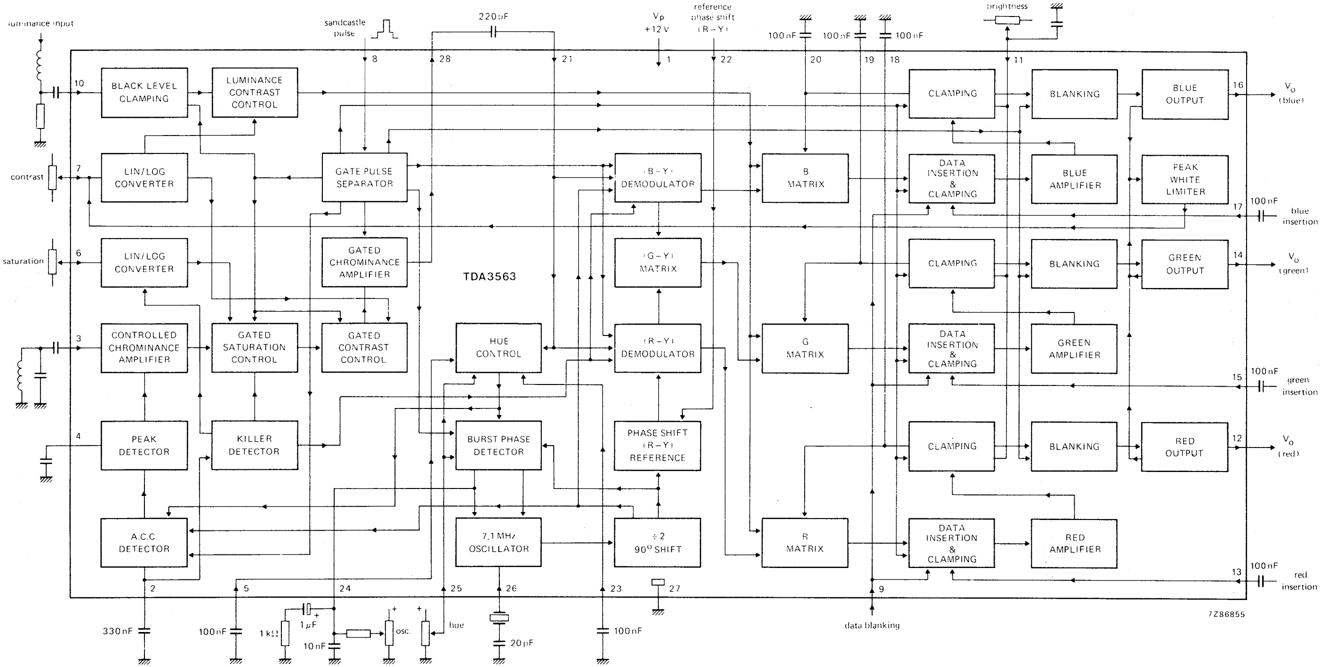


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1\text{-}27}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to +65	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	=	50	K/W

CHARACTERISTICS

$V_P = V_{1\text{-}27} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	$V_P = V_{1\text{-}27}$	10	12	13,2	V
Supply current	$I_P = I_1$	–	85	115	mA
Total power dissipation	P_{tot}	–	1	1,4	W
Luminance amplifier					
Input voltage (note 1) (peak-to-peak value)	$V_{10\text{-}27(p\text{-}p)}$	–	0,45	–	V
Contrast control range (see Fig. 2)		–17	–	+3	dB
Control voltage for an attenuation of 40 dB		–	1,2	–	V
Contrast control input current	I_7	–	–	15	μA
Chrominance amplifier					
Input voltage (note 2) (peak-to-peak value)	$V_{3\text{-}27(p\text{-}p)}$	55	550	1100	mV
A.C.C. control range		30	–	–	dB
Change of the burst signal at the output over the whole control range		–	–	1	dB
Output voltage (note 3) (peak-to-peak value) at a burst signal of 0,3 V peak to peak	$V_{28\text{-}27}$	–	0,15	–	V
Maximum output voltage range (peak-to-peak value); $R_L = 2$ kΩ	$V_{28\text{-}27}$	–	4	–	V
Frequency response between 0 and 5 MHz	$\alpha_{28\text{-}3}$	–	–	–2	dB
Saturation control range (see Fig. 3)		50	–	–	dB
Saturation control input current	I_6	–	–	20	μA
Output impedance of chrominance amplifier	$\lvert Z_{28\text{-}27}\rvert$	–	25	–	Ω
Output current	I_{28}	–	–	10	mA
Reference part					
Phase-locked loop					
Catching range (note 4)	Δf	500	700	–	Hz
Phase shift (notes 4 and 5)	$\Delta\varphi$	–	–	5	deg
Oscillator					
Temperature coefficient of oscillator frequency (note 4)	TC_{osc}	–	–1,5	–	Hz/K
Frequency variation when supply voltage increases from 10 V to 13,2 V (note 4)	Δf_{osc}	–	40	–	Hz

DEVELOPMENT SAMPLE DATA

parameter	symbol	min.	typ.	max.	unit
Reference part (continued)					
Oscillator (continued)					
Input resistance (pin 26)	$R_{26\text{-}27}$	–	400	–	Ω
Input capacitance (pin 26)	$C_{26\text{-}27}$	–	–	10	pF
A.C.C. generation (pin 2)					
Control voltage at nominal input signal	$V_{2\text{-}27}$	–	5,0	–	V
Control voltage without chrominance input	$V_{2\text{-}27}$	–	2,7	–	V
Colour-off voltage	$V_{2\text{-}27}$	–	3,0	–	V
Colour-on voltage	$V_{2\text{-}27}$	–	3,3	–	V
Hue control					
Control range		± 50	–	–	deg
Demodulator part					
Input burst signal amplitude (peak-to-peak value)	$V_{21\text{-}27(p\text{-}p)}$	–	300	–	mV
Ratio for demodulated signals for equal input signal amplitudes					
(B-Y)/(R-Y)	$\frac{V_{16\text{-}27}}{V_{12\text{-}27}}$	–	1,06 ± 10%	–	
(G-Y)/(R-Y); no (B-Y) signal	$\frac{V_{14\text{-}27}}{V_{12\text{-}27}}$	–	–0,27 ± 20%	–	
(G-Y)/(B-Y); no (R-Y) signal	$\frac{V_{14\text{-}27}}{V_{16\text{-}27}}$	–	–0,2 ± 20%	–	
Frequency response between 0 and 1 MHz		–	–	–3	dB
RGB matrix and amplifiers					
Output voltage (note 3) (peak-to-peak value) at nominal luminance/contrast (black-to-white)	$V_{12;14;16\text{-}27}$	4,5	5,3	6,3	V
Maximum peak-white level (note 6)	$V_{12;14;16\text{-}27}$	9,0	9,3	9,6	V
Maximum output current	$I_{12;14;16}$	–	–	10	mA
Output black level voltage for brightness control of 2 V		–	2,7	–	V
Brightness control voltage range			see Fig. 4		
Brightness control input current	I_{11}	–	–	50	μA
Relative spread between R, G and B output signals		–	–	10	%
Blanking level at RGB outputs		1,9	2,1	2,3	V
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	–	1,1	–	

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB matrix and amplifiers (continued)					
Output impedance of RGB outputs	$\lvert Z_{12;14;16\text{-}27}\rvert$	–	50	–	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		–	–	–3	dB
Data insertion					
Input signals (peak-to-peak value) for an RGB output voltage of 5 V (peak-to-peak)	$V_{13;15;17\text{-}27(p\text{-}p)}$	0,9	1	1,1	V
Data blanking (pin 9)					
Input voltage for no data insertion	$V_{9\text{-}27}$	–	–	0,3	V
Input voltage for data insertion	$V_{9\text{-}27}$	0,9	–	–	V
Maximum input voltage	$V_{9\text{-}27(m)}$	–	–	2	V
Delay of data blanking	t_d	–	–	20	ns
Input current	I_9	–	–	35	μA
Sandcastle input (pin 8)					
Level at which RGB blanking is activated	$V_{8\text{-}27}$	1	1,5	2	V
Level at which burst gating and clamping pulse are separated	$V_{8\text{-}27}$	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse	t_d	–	0,4	–	μs
Input current					
at $V_{8\text{-}27}$ = 0 to 1 V	$-I_8$	–	–	1	mA
at $V_{8\text{-}27}$ = 1 to 8,5 V	I_8	–	20	–	μA
at $V_{8\text{-}27}$ = 8,5 to 12 V	I_8	–	–	2	mA

Notes to the characteristics

1. Signal with negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75% saturation; chrominance to burst ratio is 2,2 : 1.
3. At nominal contrast and saturation. Nominal contrast is specified as the maximum contrast –3 dB and nominal saturation as the maximum saturation –6 dB.
4. All frequency variations are referred to 3,58 MHz carrier frequency.
5. For ± 400 Hz deviation of the oscillator frequency.
6. If the typical voltage for this white level is exceeded, the output voltage is reduced by discharging the capacitor at pin 7 (contrast control); discharge current is 1,5 mA.

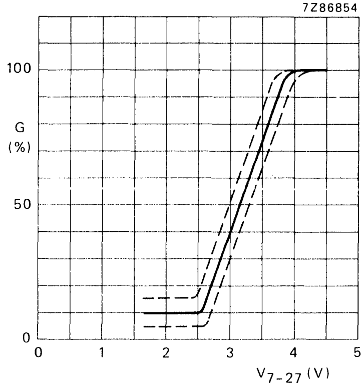


Fig. 2 Contrast control voltage range.

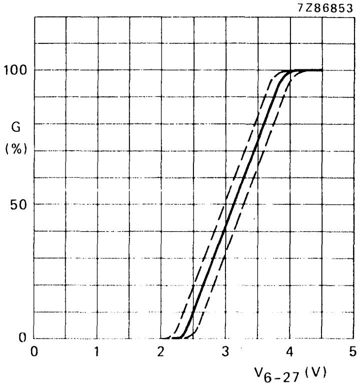


Fig. 3 Saturation control voltage range.

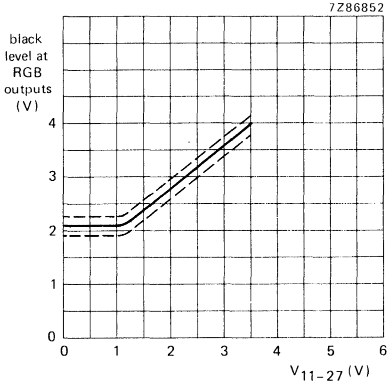


Fig. 4 Brightness control voltage range.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. + 12 V power supply

The circuit gives good operation in a supply voltage range between 8 and 13,2 V provided that the supply voltage for the controls is equal to the supply voltage of the TDA3563. All signal and control levels have a linear dependency on the supply voltage. The current consumed by the IC at + 12 V is typically 85 mA. It is linearly dependent on the supply voltage.

2. Control voltage for identification

The output pulses of the a.c.c. detector are detected with a sample-and-hold circuit to obtain information for the colour killer. The output is available at pin 2.

3. Chrominance input

The chrominance signal must be a.c.-coupled to the input. Its amplitude must be between 55 and 1100 mV peak-to-peak (25 to 500 mV peak-to-peak burst signal). All figures for the chrominance signals are based on a colour bar signal with 75% saturation, that is if the burst-to-chrominance ratio of the input is 1 : 2,2.

4. Control voltage a.c.c. detector

The shifted burst signal is synchronously demodulated in a separate a.c.c. detector to generate the a.c.c. voltage. The output pulses of this detector are peak detected to control the gain of the chrominance amplifier, thus preventing blooming-up of the colour during weak signal reception.

5. Decoupling of the 90° phase shift circuit

A control circuit is required in the 90° phase shift circuit to make the chrominance voltage independent of the hue setting. The control circuit is decoupled by a capacitor at this pin.

6. Saturation control

The saturation control range is in excess of 50 dB. The control voltage range is 2 to 4 V. Saturation control is a linear function of the control voltage.

When the colour killer is active, the saturation control voltage is reduced to a low level if the resistance of the external control network is sufficiently high. Then the chrominance amplifier supplies no signal to the demodulator. Colour switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply the colour killer circuit is overruled so that the colour signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also pins 24 and 26).

7. Contrast control

The contrast control range is 20 dB for a control voltage change from + 2 V to + 4 V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1 V or less. If one or more output signals surpasses the level of 9 V the peak-white limiter circuit becomes active and reduces the output signals via the contrast control by discharging a 10 μF capacitor via an internal current sink.

8. Sandcastle and vertical blanking input

The output signals are blanked if the amplitude of the pulse is between 2 V and 6,5 V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7,5 V. The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of the video signal on the sync pulse. The duration should be about 4 μs for proper a.c.c. operation.

9. Video-data switching

The insertion circuit is activated by means of this input by an input pulse between 1 and 2 V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted this pin should be connected to ground (pin 27).

The switching times are very short (< 20 ns) to avoid coloured edges of the inserted signals on the screen.

10. Luminance signal input

The input signal should have a peak-to-peak amplitude of 0,45 V (peak-white to sync) to obtain a black-white output signal of 5,3 V at nominal contrast. It must be a.c.-coupled to the input by a capacitor of about 22 nF. The signal is clamped at the input to an internal reference voltage. The 1 kΩ luminance delay line can be applied because the luminance impedance is very high. Consequently the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally the coupling capacitor value may be small.

11. Brightness control

The black level of the RGB outputs can be set by the voltage on this pin (see Fig. 4). The minimum black level is identical to the blanking level. The black level can be set higher than 4 V, however, the available output signal amplitude is reduced (see also pin 7). Brightness control also operates on the black level of the inserted signals.

12, 14, 16. RGB outputs

The output circuits for red, green and blue are identical. Output signals are 5,3 V (black-white) for nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2,1 V. The peak-white level is limited to 9 V. When this level is exceeded the output signal amplitude is reduced via the contrast control (see also pin 7).

13, 15, 17. Inputs for external RGB signals

The external signals must be a.c.-coupled to the inputs via a coupling capacitor of about 100 nF. Source impedance should not exceed 150 Ω. The input signal required for a 5 V peak-to-peak output signal is 1 V peak to peak. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used the coupling capacitors have to be connected to ground (pin 27).

18, 19, 20. Black level clamp capacitors

The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100 nF.

21, 22. Demodulator input and reference signal phase adjustment

The (R-Y) and (B-Y) demodulator inputs are internally connected (pin 21). The phase angle between the two reference carriers is 115°. At the nominal hue adjustment the (B-Y) signal is demodulated with a difference of 0°. The phase shift of 115° can be changing the voltage at pin 22. The gain at the two demodulators is identical. The (G-Y) is composed of −0,27(R-Y) −0,22(B-Y).

23, 25. Hue control

The hue control is obtained by changing the phase of the input signal of the burst phase detector with respect to the demodulator input signal. This phase shift is obtained by generating a 90° shifted sine-wave via a Miller integrator (biased via pin 23) which is mixed with the original burst signal.

APPLICATION INFORMATION (continued)

24, 26. Reference oscillator

As the burst phase detector has an asymmetrical output the oscillator can be adjusted by changing the voltage of the output (pin 24) via a high-ohmic resistor. The capacitor in series with the oscillator crystal must then have a fixed value. When pin 6 (saturation control) is connected to the positive supply line the burst phase detector is based in its nominal position and the colour killer is overruled. This position can therefore be used for the adjustment of the oscillator.

27. Ground

28. Output of the chrominance amplifier

The (R-Y) and (B-Y) demodulator input (pin 21) is a.c.-coupled to this output.

NTSC DECODER

GENERAL DESCRIPTION

The TDA3564 is a monolithic integrated decoder for the NTSC colour television standards. It combines all functions required for the demodulation of NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages.

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_P = V_{1-23}$	typ.	12	V
Supply current (pin 1)	$I_P = I_1$	typ.	85	mA
Luminance input signal (pin 9)				
Input voltage (peak-to-peak value)	$V_{9-23(p-p)}$	typ.	450	mV
Contrast control range		typ.	−17 to + 3	dB
Chrominance amplifier (pin 3)				
Input voltage range (peak-to-peak value)	$V_{3-23(p-p)}$		55 to 1100	mV
Saturation control range		min.	50	dB
RGB matrix and amplifiers				
Output voltage at nominal luminance input signal and nominal contrast (peak-to-peak value)	$V_{13,\ 14,\ 15-23(p-p)}$	typ.	5	V
Sandcastle input (pin 8)				
Blanking input voltage	V_{8-23}	typ.	1,5	V
Burst gating and clamping input voltage	V_{8-23}	typ.	7	V

PACKAGE OUTLINE

24-lead DIL; plastic, with internal heat spreader (SOT-101A, B).

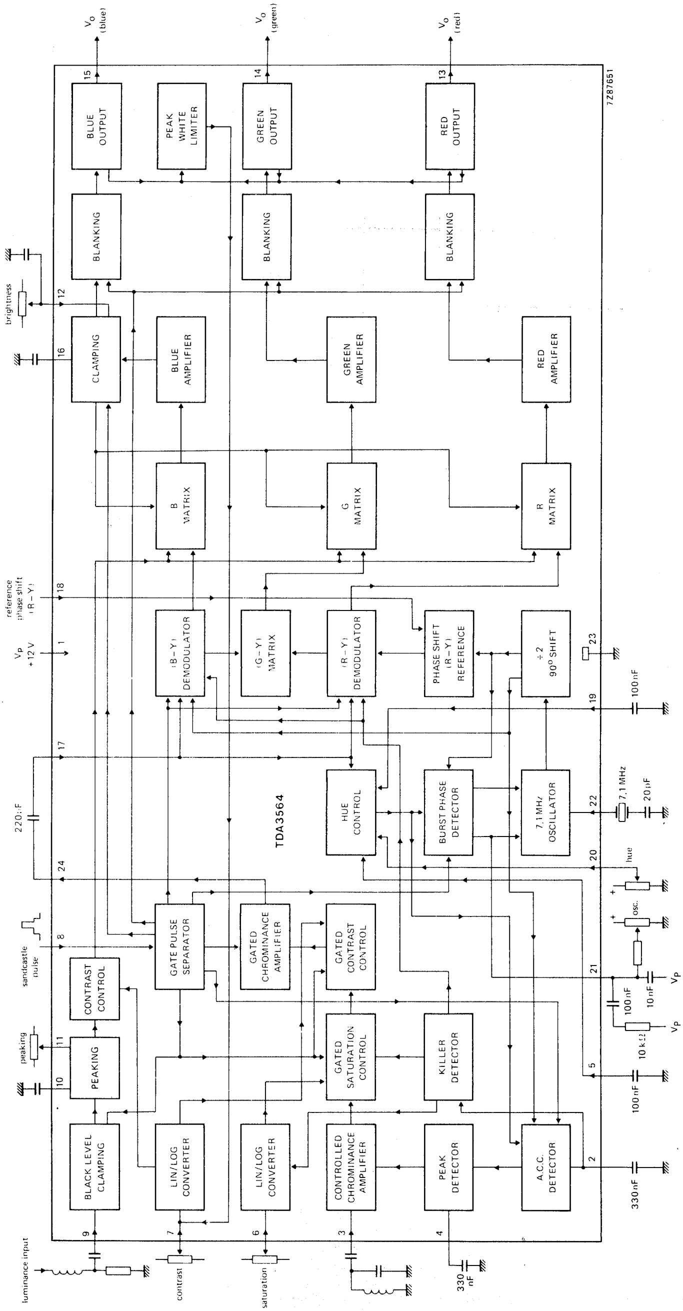


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal is a.c. coupled to the input (pin 9).

The black level at the output of the preamplifier is clamped to a fixed d.c. level by the black level clamping circuit. The high input impedance of the luminance amplifier minimizes disturbance of the input signal black level by the source impedance (delay line matching resistors).

During clamping the low input impedance reduces noise and residual signals. After clamping the signal is fed to a peaking stage. The overshoot is defined by the capacitor connected to pin 10 and the peaking is adjusted by the control voltage at pin 11.

The peaking stage is followed by a contrast control stage. The contrast control voltage range (pin 7) is nominally −17 to + 3 dB. The linear relationship between the contrast control voltage and the gain is shown in Fig. 2.

Chrominance amplifier

The chrominance amplifier has an asymmetrical input. The input signal must be a.c. coupled (pin 3) and have a minimum amplitude of 55 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal must not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the saturation and contrast control stages. Chrominance and luminance contrast control stages are directly coupled to obtain good tracking. Saturation is linearly controlled via pin 6 (see Fig. 3). The control voltage range is 2 V to 4 V, the input impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by saturation control. The output signal at pin 24 is a.c. coupled to the demodulators via pin 17.

Oscillator and a.c.c. detector

The 7,16 MHz reference oscillator operates at twice the subcarrier frequency. The reference signals for the (R-Y) and (B-Y) demodulators, burst phase detector and a.c.c. detector are obtained via the divide-by-2 circuit, which provides a 90° phase shift. The oscillator is controlled by the burst phase detector, which is gated with the narrow part of the sandcastle pulse (pin 8). As the burst phase detector has an asymmetrical output the oscillator can be adjusted by changing the voltage of the output (pin 21) via a high-ohmic resistor. The capacitor in series with the oscillator crystal must then have a fixed value. When pin 6 (saturation control) is connected to the positive supply line the burst signal is suppressed and the colour killer is overruled. This position can therefore be used for adjustment of the oscillator. The adjustment is visible on the screen.

The hue control is obtained by changing the phase of the input signal of the burst phase detector with respect to the chrominance signal applied to the demodulators. This phase shift is obtained by generating a 90° shifted sine-wave via a Miller integrator (biased via pin 19) which is mixed with the original burst signal. A control circuit is required in the 90° phase shift circuit to make the chrominance voltage independent of the hue setting. This control circuit is decoupled by a capacitor connected to pin 5.

Oscillator and a.c.c. detector

As the shifted burst signal is synchronously demodulated in a separate a.c.c. detector to generate the a.c.c. voltage, it is not affected by the hue control. The output pulses of this detector are peak detected (pin 4) to control the gain of the chrominance amplifier, thus preventing blooming-up of the colour during weak signal reception. This ensures reliable operation of the colour killer. During colour killing the colour channel is blocked by switching-off saturation control and the demodulators.

FUNCTIONAL DESCRIPTION (continued)

Demodulators

The (R-Y) and (B-Y) demodulators are driven by the chrominance signal (pin 24) and the reference signals from the 7,16 MHz divider circuit. The phase angle between the two reference carriers is 115°. This is achieved by the (R-Y) demodulator receiving an additional phase shift by mixing the two signals from the divider circuit. The phase shift of 115° can be varied between 90° and 140° by changing the bias voltage at pin 18. The demodulator output signals are fed to R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G matrix. The demodulator circuits are killed and blanked by by-passing the input signals.

RGB matrix and amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described.
The luminance and the colour difference signals are added in the matrix circuit to obtain the colour signal. Output signals are 5 $V_{(p-p)}$ (black-white) for the following nominal input signals and control settings.

- Luminance 450 $mV_{(p-p)}$
- Chrominance 550 $mV_{(p-p)}$ (burst-to-chrominance ratio of the input 1: 2,2)
- Contrast −3 dB max.
- Saturation −6 dB max.

The maximum output voltage is approximately 7 $V_{(p-p)}$.
The black level of the blue channel is compared with a variable external reference level (pin 12) which provides brightness control. The brightness control range is 1 V to 3,2 V (see Fig. 4). The control voltage is stored in a capacitor (connected to pin 16) and controls the black level at the output (pin 15) between 2 V and 4 V, via a change of the level of the luminance signal before matrixing.

Note

Black levels of up to approximately 6 V are possible, but amplitude of the output signal is reduced to 3 $V_{(p-p)}$.
If the output signal surpasses the level of 9 V the peak-white limiter circuit becomes active and reduces the output signal via the contrast control.

Blanking of RGB signals

The RGB signals can be blanked via the sandcastle input (pin 8). A slicing level of 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking a level of + 2 V is available at the output.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-23}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Storage temperature range	T_{stg}		−25 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 65 °C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	=	50 K/W

CHARACTERISTICS

$V_P = V_{1\text{-}23} = 12$ V; $T_{amb} = 25\ ^{o}C$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	$V_P = V_{1\text{-}23}$	8	12	13,2	V
Supply current	$I_P = I_1$	–	85	–	mA
Total power dissipation	P_{tot}	–	1,0	–	W
Luminance amplifier (pin 9)					
Input voltage (note 1) (peak-to-peak value)	$V_{9\text{-}23(p\text{-}p)}$	–	450	–	mV
Input level before clipping	$V_{9\text{-}23}$	–	–	2	V
Input current	I_9	–	0,15	1	μA
Contrast control range (see Fig. 2)		–17	–	+ 3	dB
Control voltage for an attenuation of 40 dB		–	1,2	–	V
Input current contrast control	I_7	–	–	15	μA
Peaking of luminance signal					
Output impedance (pin 10)	$\|Z_{10\text{-}23}\|$	–	200	–	Ω
Ratio of internal/external current when pin 10 is short-circuited		–	3	–	
Control voltage for peaking adjustment (pin 11)	$V_{11\text{-}23}$	–	2-4	–	V
Input impedance (pin 11)	$\|Z_{11\text{-}23}$	–	10	–	kΩ
Chrominance amplifier (pin 3)					
Input voltage (note 2) (peak-to-peak value)	$V_{3\text{-}23(p\text{-}p)}$	55	550	1100	mV
Input impedance	$\|Z_{3\text{-}23}\|$	–	8	–	kΩ
Input capacitance	$C_{3\text{-}23}$	–	4	6	pF
A.C.C. control range		30	–	–	dB
Change of the burst signal at the output over the whole control range		–	–	1	dB
Gain at nominal contrast/saturation pin 3 to pin 24 (note 3)		13	–	–	dB
Output voltage (note 3) (peak-to-peak value) at a burst signal of 300 $mV_{(p\text{-}p)}$	$V_{24\text{-}23(p\text{-}p)}$	–	240	–	mV
Maximum output voltage range (pin 24) (peak-to-peak value)	$V_{24\text{-}23(p\text{-}p)}$	–	1-7	–	V
Distortion of chrominance amplifier at $V_{24\text{-}23(p\text{-}p)} = 0{,}5$ V (output) up to $V_{3\text{-}23(p\text{-}p)} = 1$ V (input)	d	–	3,0	5	%

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance amplifier (continued)					
Frequency response between 0 and 5 MHz	$\alpha_{24\text{-}3}$	–	–	–2	dB
Saturation control range (see Fig. 3)		50	–	–	dB
Input current saturation control (pin 6)	I_6	–	–	20	μA
Tracking between luminance and chrominance contrast control		–	–	2	dB
Cross-coupling between luminance and chrominance amplifier (note 4)		–	–	–46	dB
Signal-to-noise ratio at nominal input signal (note 5)	S/N	56	–	–	dB
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\phi$	–	–	± 5	deg
Output impedance of chrominance amplifier	$\lvert Z_{24\text{-}23}\rvert$	–	25	–	Ω
Output current	I_{24}	–	–	10	mA
Reference part					
Phase-locked loop					
Catching range (note 6)	Δf	500	700	–	Hz
Phase shift for ± 400 Hz deviation of f_{osc} (note 6)	$\Delta\phi$	–	–	5	deg
Oscillator					
Temperature coefficient of oscillator frequency (note 6)	TC_{osc}	–	–1,5	–	Hz/K
Frequency variation when supply voltage increases from 10 to 13,2 V (note 6)	Δf_{osc}	–	40	–	Hz
Input resistance (pin 22)	$R_{22\text{-}23}$	–	300	–	Ω
Input capacitance (pin 22)	$C_{22\text{-}23}$	–	–	10	pF
A.C.C. generation (pin 2)					
Control voltage at nominal input signal	$V_{2\text{-}23}$	–	5,3	–	V
Control voltage without chrominance input	$V_{2\text{-}23}$	–	2,8	–	V
Colour-off voltage	$V_{2\text{-}23}$	–	3,4	–	V
Colour-on voltage	$V_{2\text{-}23}$	–	3,6	–	V
Change in burst amplitude with supply voltage			independent		
Voltage at pin 4 at nominal input signal	$V_{4\text{-}23}$	–	5,2	–	V
Hue control					
Control range		± 50	–	–	deg
Control voltage range			see Fig. 5		V

DEVELOPMENT SAMPLE DATA

parameter	symbol	min.	typ.	max.	unit
Demodulator part					
Input burst signal amplitude (pin 17) (peak-to-peak value)	$V_{17\text{-}23(p\text{-}p)}$	–	320	–	mV
Input impedance (pin 17; note 7)	$\lvert Z_{17\text{-}23} \rvert$	–	2	–	kΩ
Ratio of demodulated signals (B-Y)/(R-Y)	$\frac{V_{15\text{-}23}}{V_{13\text{-}23}}$	–	1,1	–	
(G-Y)/(R-Y); no (B-Y) signal	$\frac{V_{14\text{-}23}}{V_{13\text{-}23}}$	–	0,26	–	
(G-Y)/(B-Y); no (R-Y) signal	$\frac{V_{14\text{-}23}}{V_{15\text{-}23}}$	–	0,22	–	
Frequency response between 0 and 1 MHz		–	–	–3	dB
Cross-talk between colour difference signals		40	–	–	dB
Control range reference signal (R-Y) demodulator (pin 18; note 8)	ϕ		see Fig. 6		deg
RGB matrix and amplifiers					
Output voltage (peak-to-peak value) at nominal input signal (black-to-white) (note 3)	$V_{13,14,15\text{-}23(p\text{-}p)}$	–	5	–	V
Output voltage at pin 13 (peak-to-peak value) at nominal contrast/saturation and no luminance signal to (R-Y)	$V_{13\text{-}23(p\text{-}p)}$	–	5,25	–	V
Maximum peak-white level (note 9)	$V_{13,14,15\text{-}23}$	9,0	9,3	9,6	V
Maximum output current (pins 13, 14, 15)	$I_{13,14,15}$	–	–	10	mA
Output black level voltage for a brightness control voltage at pin 12 of 2 V	$V_{13,14,15\text{-}23}$	–	2,7	–	V
Black level shift with vision contents		–	–	40	mV
Brightness control voltage range			see Fig. 4		V
Brightness control input current	I_{12}	–	–	5	μA
Variation of black level					
with temperature	$\Delta V/\Delta T$	–	0,35	1,0	mV/K
with contrast	ΔV	–	10	100	mV
Relative spread between the R, G and B output signals		–	–	10	%
Relative black-level variation between the three channels during variation of contrast, brightness and supply voltage		–	0	20	mV
Differential black-level drift over a temperature range of 40 °C		–	0	20	mV
Blanking level at the RGB outputs		1,9	2,1	2,3	V
Difference in blanking level of the three channels		–	0	–	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB matrix and amplifiers (continued)					
Differential drift of the blanking levels over a temperature range of 40 °C		–	0	–	mA
Tracking of output black level with supply voltage	$\frac{\Delta V_{b1}}{V_{b1}} \times \frac{V_P}{\Delta V_P}$	–	1,1	–	
Signal-to-noise ratio of output signals (note 5)	S/N	62	–	–	dB
Residual 7,1 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		–	75	150	mV
Output impedance of RGB outputs	$\lvert Z_{13,14,15\text{-}23} \rvert$	–	50	–	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		–	–	–3	dB
Sandcastle input (pin 8)					
Level at which the RGB blanking is activated	$V_{8\text{-}23}$	1	1,5	2	V
Level at which burst gating and clamping pulse are separated	$V_{8\text{-}23}$	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse	t_d	–	0,4	–	μs
Input current					
at $V_{8\text{-}23}$ = 0 to 1 V	$-I_8$	–	–	1	mA
at $V_{8\text{-}23}$ = 1 to 8,5 V	I_8	–	20	–	μA
at $V_{8\text{-}23}$ = 8,5 to 12 V	I_8	–	–	2	mA

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75% saturation; chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast –3 dB and nominal saturation as the maximum saturation –6 dB.
4. Cross coupling is measured under the following conditions:
   - Input signals nominal
   - Contrast and saturation such that nominal output signals are obtained
   - The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to r.m.s. noise.
6. All frequency variations are referred to 3,58 MHz carrier frequency.
7. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
8. When pin 18 is open circuit the phase shift between the (R-Y) and (B-Y) reference carrier is 115°. This phase shift can be varied by changing the voltage applied to pin 18.
9. If the typical voltage for this white level is exceeded, the output voltage is reduced by discharging the capacitor at pin 7 (contrast control); discharge current is 1,5 mA.

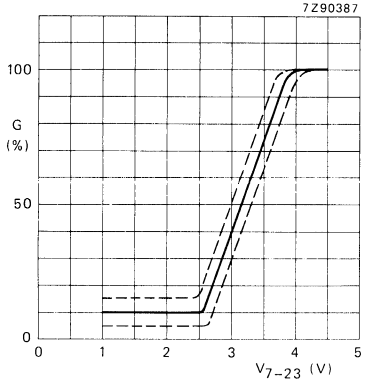


Fig. 2 Contrast control voltage range.

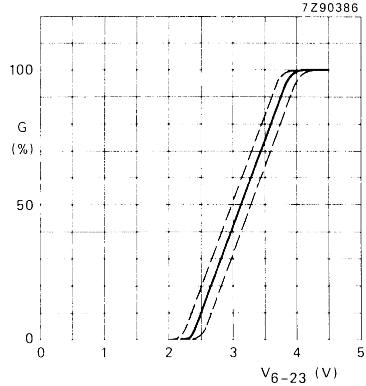


Fig. 3 Saturation control voltage range.

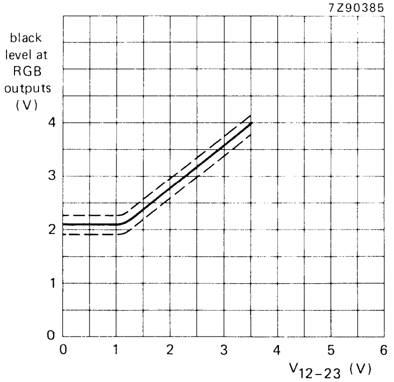


Fig. 4 Brightness control voltage range.

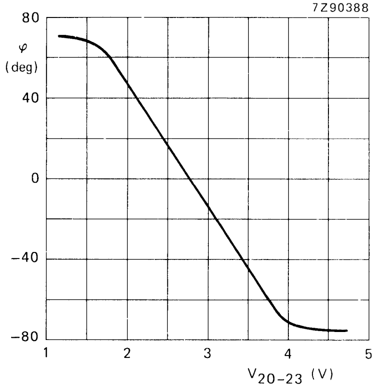


Fig. 5 Hue control voltage range.

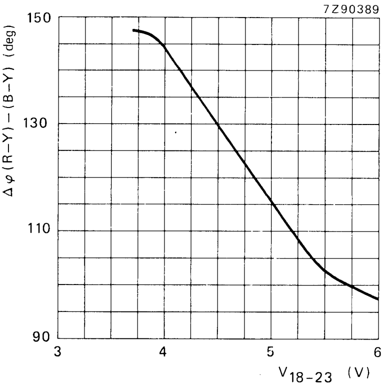


Fig. 6 Phase shift between (R-Y) and (B-Y) as a function of $V_{18\text{-}23}$.

NTSC DECODER

The TDA3570 is a monolithic integrated colour decoder for the NTSC standard. It combines all functions required for the identification and demodulation of NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. The amplifier supplies output signals up to 3,5 V peak-to-peak (picture information) enabling direct drive of the output stages. The circuit also contains an automatic picture setting switch to preset positions of both saturation and tint controls.

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}14}$	typ.	12	V
Supply current	I_1	typ.	43	mA
Luminance input signal (peak-to-peak value)	$V_{5\text{-}14(p\text{-}p)}$	typ.	1	V
RGB output signals (peak-to-peak value)	$V_{26,27,28\text{-}14(p\text{-}p)}$	typ.	3,5	V
Contrast control range		typ.	13	dB
Blanking pulse and black level gating input voltage	$V_{24,20\text{-}14}$	⩾	2	V
Chrominance input voltage (peak-to-peak value)	$V_{13\text{-}14(p\text{-}p)}$		10 to 300	mV
Saturation control range		⩾	40	dB
Tint control range		typ.	± 45°	

PACKAGE OUTLINE

28-lead DIL; plastic

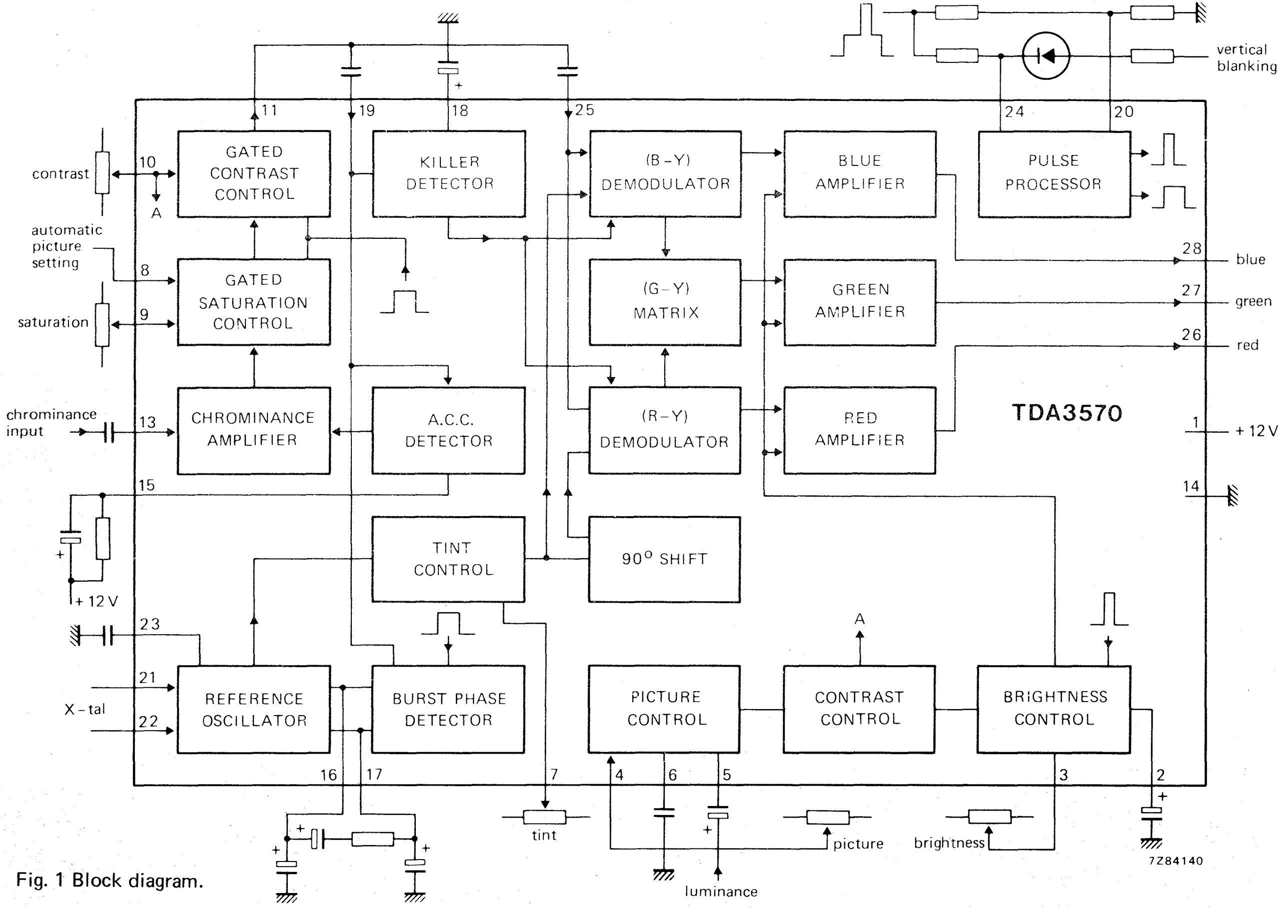


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		min.	max.	
Supply voltage	$V_P = V_{1\text{-}14}$	0	14,4	V
Input saturation voltage	$V_{9\text{-}14}$	0	V_P	V
Input contrast voltage	$V_{10\text{-}14}$	0	V_P	V
Input tint voltage	$V_{7\text{-}14}$	0	V_P	V
Input picture voltage	$V_{4\text{-}14}$	0	V_P	V
Input brightness voltage	$V_{3\text{-}14}$	0	V_P	V
Input sandcastle current	I_{20}	−30	−	mA
Input blanking pulse voltage	$V_{24\text{-}14}$	−6	V_P	V
Power dissipation at T_{amb} = 70 °C			750	mW
Storage temperature	T_{stg}	−40 to + 125		°C
Operating ambient temperature	T_{amb}	−20 to + 70		°C

CHARACTERISTICS

$V_{1\text{-}14}$ = 12 V; $V_{5\text{-}14(p\text{-}p)}$ = 1 V; $V_{13\text{-}14(p\text{-}p)}$ = 150 mV;
T_{amb} = 25 °C; measured in Fig. 2

Supply voltage	$V_{1\text{-}14}$	typ.	12	V
Supply current	I_1	typ.	43	mA

Luminance

Input voltage (positive-going sync pulse; peak-to-peak value)	$V_{5\text{-}14(p\text{-}p)}$	typ.	1	V
Video gain	G_v	typ.	5	
Contrast control voltage range	$V_{10\text{-}14}$		0 to 12	V
Contrast control range		typ.	13	dB
Brightness control voltage range	$V_{3\text{-}14}$		8 to 10	V
Black level range	$V_{26,27,28\text{-}14}$		0 to 7	V*
Max. output voltage	$V_{26,27,28\text{-}14}$	typ.	7	V
Blanking and gating pulse	$V_{24\text{-}14}$	typ.	$\geqslant 2$	V
Input impedance (pin 24)	$\lvert Z_{24\text{-}14}\rvert$	typ.	1,5	kΩ
Black level clamp and burst gating pulse	$V_{20\text{-}14}$	typ.	$\geqslant 2$	V
Input impedance (pin 20)	$\lvert Z_{20\text{-}14}\rvert$	typ.	3	kΩ

Input circuit: 3 pF in parallel with 9 kΩ

Output circuit: emitter followers with internal R_E = 2,2 kΩ

Picture control voltage	$V_{4\text{-}14}$		0 to 12	V

---

* Usable range depends on the output signal amplitude.

Chrominance

Input voltage (peak-to-peak value)	$V_{13\text{-}14(p\text{-}p)}$	typ.	150	mV
A.C.C. control range		typ.	30	dB
Colour kill level (peak-to-peak value)	$V_{13\text{-}14(p\text{-}p)}$	typ.	5	mV
Saturation control voltage range	$V_{9\text{-}14}$		1 to 6	V
Saturation control range		typ.	40	dB
Saturation control range in position AUTO*		typ.	6	dB
Tint control voltage range	$V_{7\text{-}14}$		1 to 6	V
Tint control range		typ.	± 45°	
Tint control range in position AUTO*		typ.	± 17°	
Pull in range of oscillator		typ.	± 600	Hz
Phase difference for 100 Hz change of burst		typ.	± 1,5°	

Input circuit: 6 pF in parallel with 3 kΩ

---

* Depends on the ratio of R1/R2 in Fig. 2; position AUTO: switch closed.

APPLICATION INFORMATION

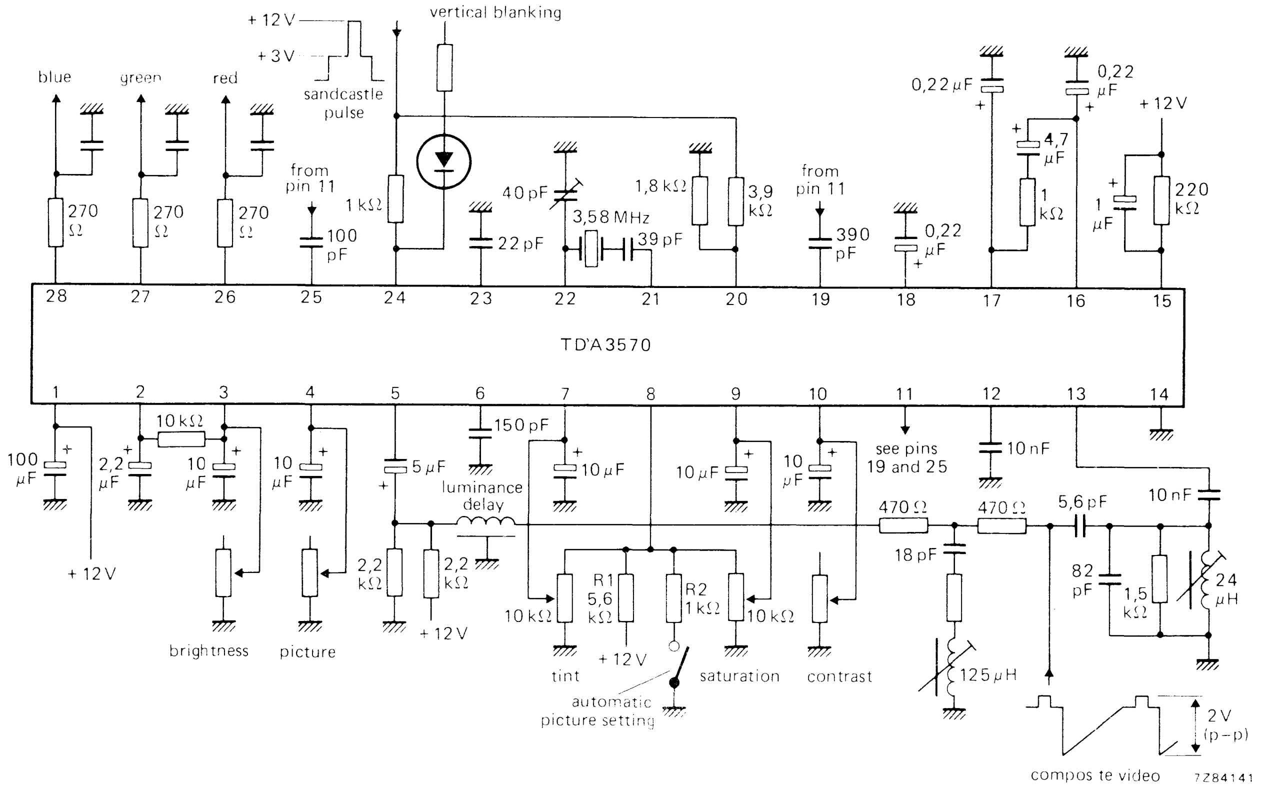
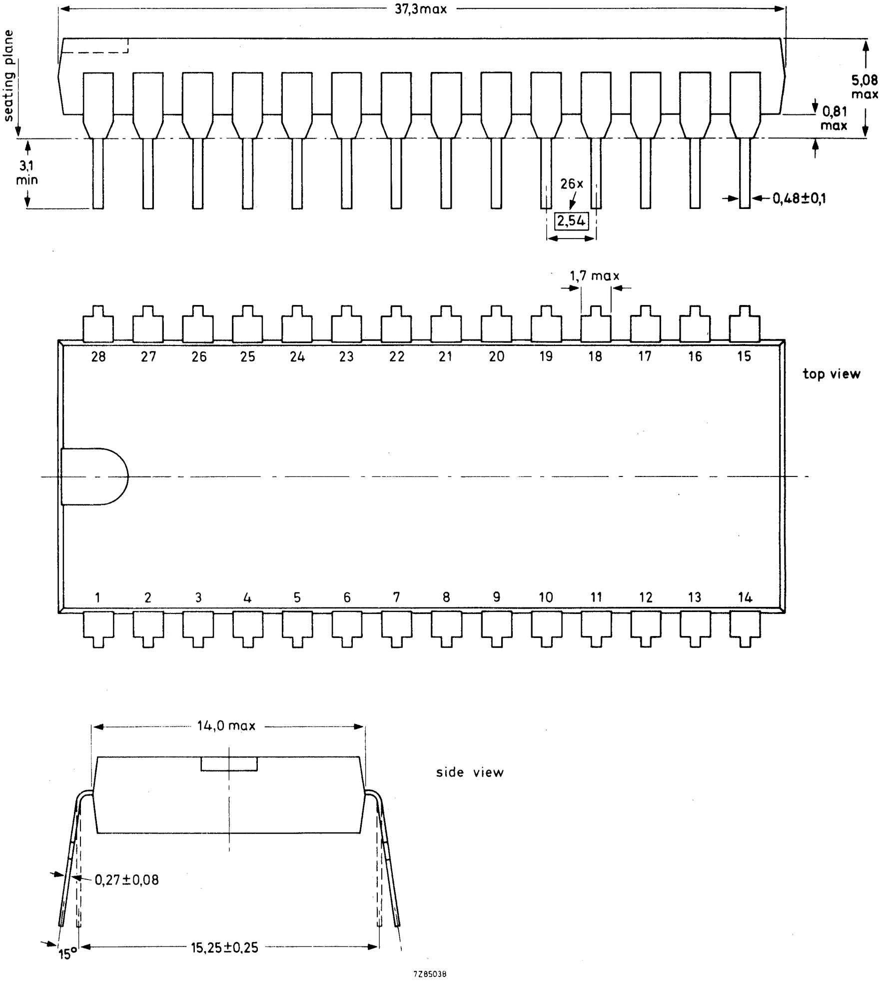


Fig. 2 Application circuit.

28-LEAD DUAL IN-LINE; PLASTIC



DEVELOPMENT SAMPLE DATA

SYNC COMBINATION WITH TRANSMITTER IDENTIFICATION AND VERTICAL 625 DIVIDER SYSTEM

GENERAL DESCRIPTION

The TDA3571B is a monolithic integrated circuit for use in colour television receivers with switched mode driven or self-regulating horizontal time-base circuits. It is designed in combination with the TDA2581 to operate as a matched pair. When supplied with a composite video signal the TDA3571B delivers drive pulses for the TDA2581 and sync pulses for the vertical deflection. The circuit is optimized for a horizontal and vertical frequency ratio of 625. It incorporates the following features:

Features

- Horizontal sync separator (including noise inverter)
- Horizontal phase detector
- Horizontal oscillator (31,25 kHz)
- Sandcastle pulse generator
- Vertical sync pulse separator
- Very stable automatic vertical synchronization due to the 625 divider system, without delay after channel change
- Three voltage level sensor on coincidence detector circuit output
- Video transmitter identification circuit for sound muting and search tuning systems
- Inhibit of vertical sync pulse when no video transmitter is detected

QUICK REFERENCE DATA

Supply voltage				
horizontal (pin 14)	$V_{14\text{-}13}$	typ.	12	V
vertical (pin 18)	$V_{18\text{-}13}$	typ.	12	V
Supply current (pin 14 + pin 18)	V_{14+18}	typ.	52	mA
Sync separator				
input voltage level (peak-to-peak value)	$V_{2\text{-}13(p\text{-}p)}$	0,07 to	1	V
slicing level		typ.	50	%
Output pulse				
horizontal (peak-to-peak value)	$V_{8\text{-}13(p\text{-}p)}$	min.	10	V
vertical sync (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	min.	10	V
burst key (peak-to-peak value)	$V_{15\text{-}13(p\text{-}p)}$	min.	10	V
Video transmitter identification circuit				
Output voltage (pin 10)				
sync pulse present	$V_{10\text{-}13}$	typ.	8	V
no sync pulse	$V_{10\text{-}13}$	max.	1	V
Phase locked loop				
control sensitivity		typ.	2000	Hz/μs
holding range	Δf	typ.	± 1000	Hz
catching range	Δf	typ.	± 900	Hz
Operating ambient temperature range	T_{amb}	−25 to +	65	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102A).

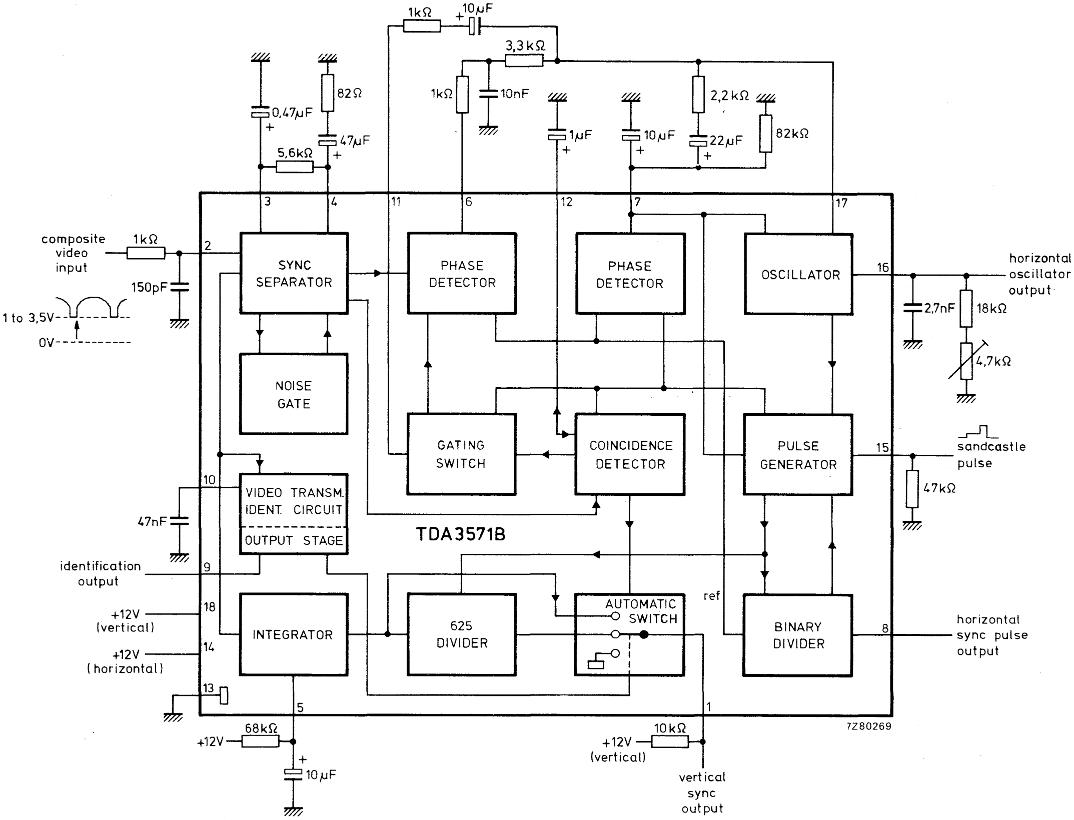


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The video input voltage to drive the sync separator must have negative-going sync, which can be obtained from synchronous demodulators such as TDA2540, TDA2541 and TDA2670.

The slicing level of the sync separator is determined by the value of the resistor between pins 3 and 4. A 5,6 kΩ resistor provides a slicing level midway between the top sync level and the blanking level. Thus the slicing level is independent of the amplitude of the sync pulse input at pin 2.

The nominal top sync level at pin 2 is 1,5 V, and the amplitude selective noise inverter is activated at 0,7 V. The horizontal phase detector has a steepness of 1,2 V/μs and together with the 1800 Hz/V of the horizontal oscillator provides a total control steepness of 2000 Hz/μs.

A second horizontal phase detector provides a 5,5 μs pulse which ensures symmetrical gating of the horizontal synchronization. During catching the gating is automatically switched off. At the same time the flywheel filter is switched to a short time constant. The value of this time constant can be determined externally via pin 11.

When the indirect vertical sync output is generated by the 625 divider system an anti-top flutter pulse switches off the equalizing and vertical sync pulse operation of the phase detector. Thus top flutter distortion of the control voltage due to vertical pulses can be anticipated. When the 625 divider system is in the direct mode the anti-top flutter pulse is inhibited.

DEVELOPMENT SAMPLE DATA

The free running output frequency of the horizontal oscillator is 31,25 kHz. The vertical frequency output is obtained by dividing this double horizontal frequency by 625. The double horizontal frequency is fed via a binary divider to provide the normal 15,625 kHz horizontal output at pin 8. The trailing edge of this pulse is positioned 0,9 μs after the end of the video sync pulse input at pin 2 (see Fig. 2).

The automatic vertical sync block contains the following:

- 625 divider
- In/out-sync detector
- Direct/indirect sync switch
- Identification circuit

It is fed by a signal obtained by integration of the composite sync signal and an internally generated, clipped video signal. The vertical sync pulse is sliced out of this integrated signal by an automatically biased clipper. The videopart of the signal helps to build up a vertical sync pulse when heavy negative-going reflections (mountains) distort the video signal. The in/out sync-detector considers a signal out-of-sync when fifteen or more successive incoming vertical sync pulses are not in phase with a reference signal from the 625 divider. Therefore a distorted vertical sync signal needs only one out-of-fifteen pulses to be in phase to keep the system in sync. When the sixteenth successive out-of-sync pulse is detected, the direct/indirect sync switch is activated to feed the vertical sync signal directly out of the block at pin 2 (direct sync vertical output).
At the same time the 625 divider is reset by one of the sync pulses. After the reset pulse, if the 7th sliced vertical sync pulse coincides with a 625 divider window, the sync output pulse is presented again by the divider system and switch-over to indirect mode occurs.
In the direct mode, every 7th non-coinciding sliced vertical sync pulse will reset the counter. Thus a non-standard video signal will result in continuous reset pulses and the direct/indirect switch will remain in the direct position.

To avoid delay in vertical synchronization, caused by waiting time of the divider circuit after channel change or an unsynchronized camera change in the studio, information is fed from the horizontal coincidence detector to the automatic switch for the vertical sync pulse. The loss of horizontal synchronization sets the automatic switch to direct vertical sync. When horizontal coincidence is detected again the setting of the automatic switch depends on whether a standard video signal is received or not. When an external voltage between 2,5 V and 7,25 V is applied via pin 12 to the coincidence detector, the horizontal phase detector is switched to a short time constant and the automatic switch to direct vertical

FUNCTIONAL DESCRIPTION (continued)

sync. A voltage level on pin 12 $>$ 8,25 V switches the horizontal phase detector to a short time constant, without affecting the indirect/direct vertical sync system which remains operational.

The video transmitter identification circuit detects when a sync pulse occurs during the internal gating pulse. This indicates the presence of a video transmitter and results in the capacitor connected to pin 10 being charged to 8 V. When no sync pulse is present the capacitor discharges to $<$ 1 V. The voltage at pin 10 is compared with an internal d.c. voltage. The identification output at pin 9 is active when pin 10 is $<$ 1,6 V (no video transmitter) and inactive (high impedance) when pin 10 is $>$ 3,5 V. The vertical sync output pulse at pin 1 is inhibited when no video transmitter is identified, which prevents interference or noise affecting the frequency of the vertical output stage. This results in a vertical stable picture, plus vertical stable position information of tuning systems.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage				
horizontal (pin 14)	$V_{14\text{-}13}$	max.	13,2	V
vertical (pin 18)	$V_{18\text{-}13}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1020	mW
Storage temperature range	T_{stg}	−25 to	+130	°C
Operating ambient temperature range	T_{amb}	−25 to	+65	°C

CHARACTERISTICS

$V_{14\text{-}13}$ = 12 V; $V_{18\text{-}13}$ = 12 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pins 14 and 18)					
Supply voltage range	$V_{14;18\text{-}13}$	10	12	13,2	V
Supply current (pin 14 + pin 18)	$I_{14} + I_{18}$	–	52	77	mA
Sync separator and noise gate (pin 2)					
Top sync level (note 1)	$V_{2\text{-}13}$	1	1,5	3,5	V
Sync pulse amplitude (peak-to-peak value) (note 2)	$V_{2\text{-}13(p\text{-}p)}$	0,07	–	1	V
Noise level	$V_{2\text{-}13}$	0,5	0,7	1,1	V
Slicing level (note 3)		35	50	65	%
Delay between sync input at pin 2 and phase detector output at pin 6*	t_d	–	0,40	–	μs
Phase detector (pin 6)					
Control voltage	$V_{6\text{-}13}$	0,5	2,8	5	V
Control sensitivity		–	1,2	–	V/μs
Phase locked loop					
Holding range (note 4)	Δf	–	± 1000	–	Hz
Catching range (note 4)	Δf	± 600	± 900	–	Hz
Control sensitivity		–	2000	–	Hz/μs
Phase modulation due to hum on the supply line (note 5)		–	2	–	μs/V

DEVELOPMENT SAMPLE DATA

---

* See waveforms Fig. 2.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Horizontal oscillator					
Output frequency					
free running	f_o	–	31,250	–	kHz
at pin 8	f_8	–	15,625	–	kHz
Temperature coefficient	T	–	$2,5 \times 10^{-4}$	–	K^{-1}
Frequency variation					
without tolerance of external components	Δf_o	–	–	4	%
when voltage at pin 14 drops to 6 V	Δf_o	–	–	10	%
when voltage at pin 14 increases from 10 to 13,2 V	Δf_o	–	–	0,5	%
Output pin 8					
voltage (no load; peak-to-peak value)	$V_{8\text{-}13(p\text{-}p)}$	10	–	–	V
current (peak-to-peak value)	$I_{8(p\text{-}p)}$	–	10	25	mA
Output resistance	$R_{8\text{-}13}$	–	433	–	Ω
Output pulse duty factor	δ	–	54	–	%
Delay between trailing edge of output pulse and end of sync pulse at pin 2	t_d	–	0,9	–	μs
Sandcastle pulse (pin 15)					
Output voltage (peak-to-peak value)	$V_{15\text{-}13(p\text{-}p)}$	9	–	–	V
Duration of upper part of output pulse*	t_p	3	3,6	4,4	μs
Duration of lower part of output pulse*	t_p	8,4	8,8	9,2	μs
Amplitude of lower part of output pulse (peak-to-peak value)*	$V_{15\text{-}13(p\text{-}p)}$	4	4,5	5	V
Output impedance	$\lvert Z_o \rvert$	–	200	–	Ω
Delay between trailing edge of sync pulse at pin 2 and leading edge of sandcastle pulse at pin 15*	t_d	–	0,9	–	μs

---

* See waveforms Fig. 2.

parameter	symbol	min.	typ.	max.	unit
Vertical sync pulse (pin 1)					
Output voltage (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	10	–	–	V
Load resistor to pin 18	R_L	4	–	–	kΩ
Duration of output pulse during indirect synchronization	t_p	–	170	–	μs
Video transmitter identification circuit Pin 10					
Sync pulse present					
charge current	I_{10}	–	+ 100	–	μA
output voltage	$V_{10\text{-}13}$	–	8	–	V
No sync pulse					
discharge current	I_{10}	–	–100	–	μA
output voltage	$V_{10\text{-}13}$	–	–	1	V
Switching level output stage					
pin 9 active when:	$V_{10\text{-}13}$	1,6	1,9	2,5	V
pin 9 inactive when:	$V_{10\text{-}13}$	3,0	3,5	4,0	V
Pin 9 (note 6)					
Sync pulse present					
output current inactive	I_9	–	–	1	μA
No sync pulse					
output current active	I_9	2,5	4,0	5,0	mA
output voltage active (load ⩽ 0,1 mA)	$V_{9\text{-}13}$	10,5	11,0	–	V
Coincidence detector (pin 12)					
First switching level (note 7)					
voltage	$V_{12\text{-}13}$	1,7	2,0	2,2	V
required input current	I_{12}	0,8	–	–	mA
maximum allowed input current	I_{12}	–	–	1,5	mA
Second switching level* (note 8)					
voltage	$V_{12\text{-}13}$	7,25	7,75	8,25	V
required input current	I_{12}	–	2,2	3,0	mA
Voltage					
normal conditions	$V_{12\text{-}13}$	–	0,4	–	V
out-of-sync	$V_{12\text{-}13}$	–	2,5	–	V
during noise	$V_{12\text{-}13}$	–	1,0	–	V

* VDR conditions.

Notes to characteristics

1. The video signal at pin 2 must have negative-going sync.
2. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
3. The slicing level is determined by the value of the resistor between pin 3 and pin 4. The 50% figure is obtained with a 5,6 kΩ resistor.
4. Values of external circuitry as shown in Fig. 1.
5. The voltage is a peak-to-peak value; the figure can be reduced to 0,6 μs/V (p-p) by connecting a 330 nF capacitor between pins 7 and 14.
6. The video transmitter identification output stage at pin 9 consists of a p-n-p current source with an n-p-n emitter-follower.
7. A voltage level between 2,5 V and 7,25 V switches the horizontal phase detector to a short time constant and the automatic switch to direct vertical sync.
8. A voltage level > 8,25 V switches the horizontal phase detector to a short time constant without affecting the operation of the automatic switch.

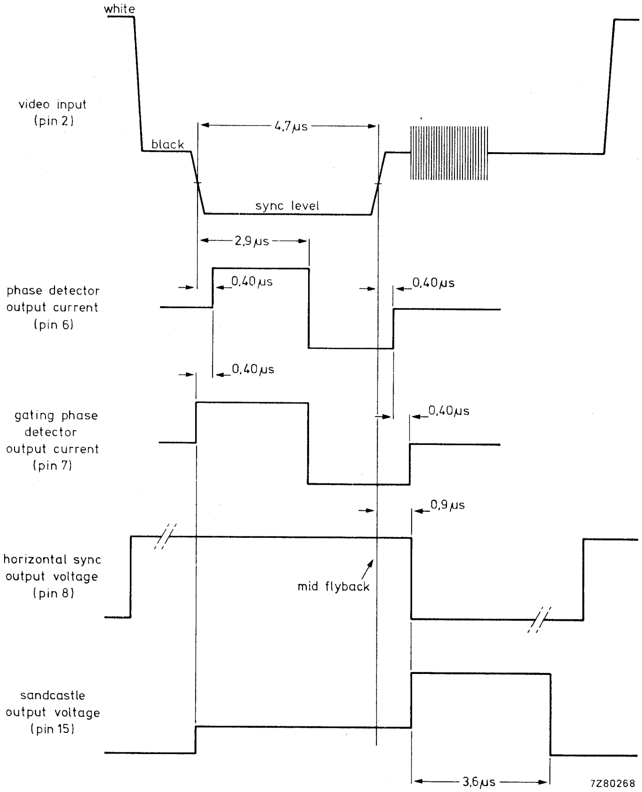


Fig. 2 Phase relationship between the input and output signals of the TDA3571B.

APPLICATION INFORMATION (see also Fig. 3)

The function is described against the corresponding pin number.

1. Vertical output pulse

A 10 kΩ resistor must be connected between pin 1 and the positive vertical supply line at pin 18. The pulse is obtained from the 625 divider circuit when standard input signals a received or from the sync separator when the signals are non-standard. The pulse is inhibited when no video transmitter is detected.

2. Video input

The video input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation. The slicing level is fixed at 50% for the sync pulse amplitude range 0,07 to 1 V which provides good sync separation down to pulses with an amplitude of 70 mV peak-to-peak. The slicing level is increased for sync pulses in excess of 1 V peak-to-peak. The noise gate is activated at an input level < 1 V, thus when noise gating is required the top sync level should be close to the minimum level of 1 V. When i.f. circuits with a noise gate are used (TDA2540; TDA2541) the noise gate of the TDA3571B is not required.

3. Sync separator slicing level output

The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 4. The slicing level P is determined by the following formula.

$$P = \frac{R_S}{R_S + T_{hor}/T_{sync} \times 0{,}35\ \text{k}\Omega} \times 100\% = \frac{R_S}{R_S + 5{,}6\ \text{k}\Omega} \times 100\%$$

where R_S is the resistor (in kΩ) between pins 3 and 4. The capacitor that is connected to pin 3 must be between 0,47 μF and 4,7 μF.

4. Black level detector output

The black level of the input signal is detected on this pin. This is required to obtain good sync separator operation. A 47 μF capacitor in series with a resistor of 82 Ω must be connected to this pin. A 5,6 kΩ resistor connected between pin 3 and pin 4 results in a slicing level of 50%.

5. Vertical sync pulse integrator biasing network

The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external RC-network is required for the correct biasing of this circuit for various input conditions. Typical values are: R = 68 kΩ; C = 10 μF. The resistor influences the delay of the **direct** vertical sync pulse.

6. Horizontal phase detector output

The control voltage for the horizontal oscillator is obtained on this pin. The output current is about 2 mA.

7. Reference voltage horizontal frequency control stage

This pin has two functions. It is used to decouple the reference voltage for the frequency control of the horizontal (so a good suppression of interference is obtained which may be present on the supply line). It also controls the reference waveform for symmetrical gating of the horizontal synchronization, thus providing good noise immunity.

APPLICATION INFORMATION (continued)

8. Horizontal sync pulse output

This pulse is obtained from the horizontal oscillator via a divider circuit. The duty factor is 54%. The trailing edge of this pulse occurs 0,9 μs after the end of the video sync pulse input at pin 2. Because of this phase relationship the horizontal sync pulse can drive directly the TDA2581.

9. Video transmitter identification output

This is an emitter-follower output which will be inactive (high-impedance) when the level at pin 10 is >3,5 V (video transmitter detected). The output will be active high when the level at pin 10 is < 1,6 V (no video transmitter detected). This feature can be used for search-tuning and sound-muting.

10. Video transmitter identification

A 47 nF capacitor must be connected to this pin. It charges to a level of 8 V when a sync pulse is detected, and discharges to a level of < 1 V when no sync pulse is detected.

11. Gating switch

This pin is used to switch the time constant of the flywheel filter. The pin condition is determined by the coincidence detector (pin 12). During in-sync or when only noise is being received pin 11 assumes ground level, which results in a long time constant and good noise immunity.

12. Coincidence detector output

A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal. There are two switching levels at pin 12. At the first switching level when the output voltage is < 1,85 V, the flywheel filter is switched to a long time constant and the gating of the phase detector is switched on. When the output voltage is > 1,85 V, the flywheel filter has a short time constant, and the gating of the phase detector is switched off. The result is that during noise the flywheel filter time constant remains long thus preventing large shifts in the frequency of the horizontal oscillator (and screening of the horizontal output transformer). At the second switching level when the output voltage is > 8,25 V the sync system is switched to a short time constant while the indirect/direct vertical sync system remains fully operational. This condition is suitable for VCR application.

13. Negative supply (ground)

14. Positive supply horizontal oscillator

Interference and hum on this supply line can affect the oscillator frequency. It is therefore necessary to have separate decoupling of this pin with respect to pin 18.

15. Sandcastle pulse output

This pulse is composed of two parts. The lower part has an amplitude of typ. 4,5 V peak-to-peak and a width of max. 9,2 μs (for phase relationship see Fig. 2). The upper part has a total amplitude in excess of 9 V peak-to-peak and a width of max. 4,4 μs. The leading edge of this pulse has a delay of 0,9 μs with respect to the trailing edge of the sync pulse at the input (pin 2). This pulse can directly drive the burst gate/black level clamp input of the TDA2560.

16. RC-network horizontal oscillator

Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part must be as small as possible, because of poor stability of variable carbon resistors.

The oscillator can be adjusted when pins 7 and 17 are short circuited (see Fig. 3).

17. Horizontal oscillator control pin

18. Positive supply sync separator and divider circuit (vertical)

This supply requires only simple decoupling. The typical combined current draw of pins 14 and 18 is 52 mA.

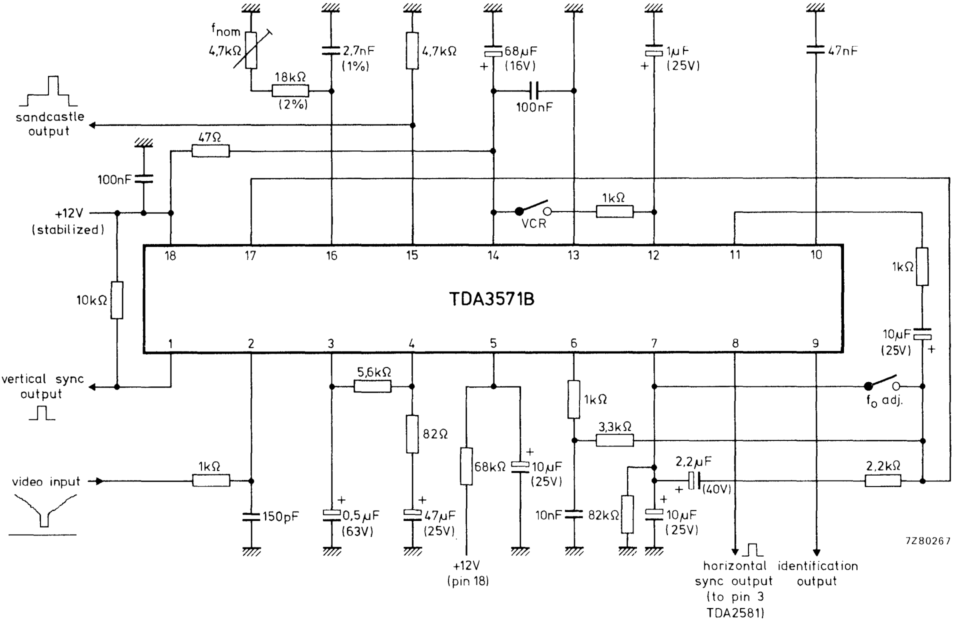


Fig. 3 Typical application circuit diagram; for combination of the TDA3571B with the TDA2581.

DEVELOPMENT SAMPLE DATA

SYNC COMBINATION WITH TRANSMITTER IDENTIFICATION AND VERTICAL 625 DIVIDER SYSTEM

GENERAL DESCRIPTION

The TDA3576B is a monolithic integrated circuit for use in colour television receivers. The circuit is optimized for a horizontal and vertical frequency ratio of 625.

Features

- Horizontal sync separator (including noise inverter) with sliding bias such that the sync pulse is always sliced between top sync level and blanking level
- Phase detector which compares the horizontal sync pulse with the oscillator voltage; this phase detector is gated
- Phase detector which compares the horizontal flyback pulse with the oscillator voltage
- Horizontal oscillator (31,25 kHz)
- Time constant switching of the first control loop (short time constant during catching and reception of VCR signals)
- Burst key pulse generator (sandcastle pulse with three levels)
- Very stable automatic vertical synchronization due to the 625 divider system, without delay after channel change
- Vertical sync pulse separator
- Three voltage level sensor on coincidence detector circuit output
- Video transmitter identification circuit for sound muting and search tuning systems
- Inhibit of vertical sync pulse when no video transmitter is detected

QUICK REFERENCE DATA

Supply voltage (pin 17)	$V_P = V_{17\text{-}10}$	typ.	12	V
Supply current (pin 17)	I_{17}	typ.	70	mA
Sync separator				
input voltage level (peak-to-peak value)	$V_{5\text{-}10(p\text{-}p)}$		0,1 to 1	V
slicing level		typ.	50	%
Phase-locked-loop				
control sensitivity sync to flyback pulse		typ.	4	kHz/μs
holding range	Δf	typ.	± 1000	Hz
catching range	Δf	typ.	± 900	Hz
Horizontal output pulse (peak-to-peak value)	$V_{11\text{-}10(p\text{-}p)}$	min.	11,3	V
Vertical output pulse (peak-to-peak value)	$V_{3\text{-}10(p\text{-}p)}$	min.	10	V
Burst key output pulse (peak-to-peak value)	$V_{2\text{-}10(p\text{-}p)}$	min.	9	V
Video transmitter identification circuit output voltage (pin 1)				
sync pulse present	$V_{1\text{-}10}$	typ.	8,4	V
no sync pulse	$V_{1\text{-}10}$	max.	1	V
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE4).

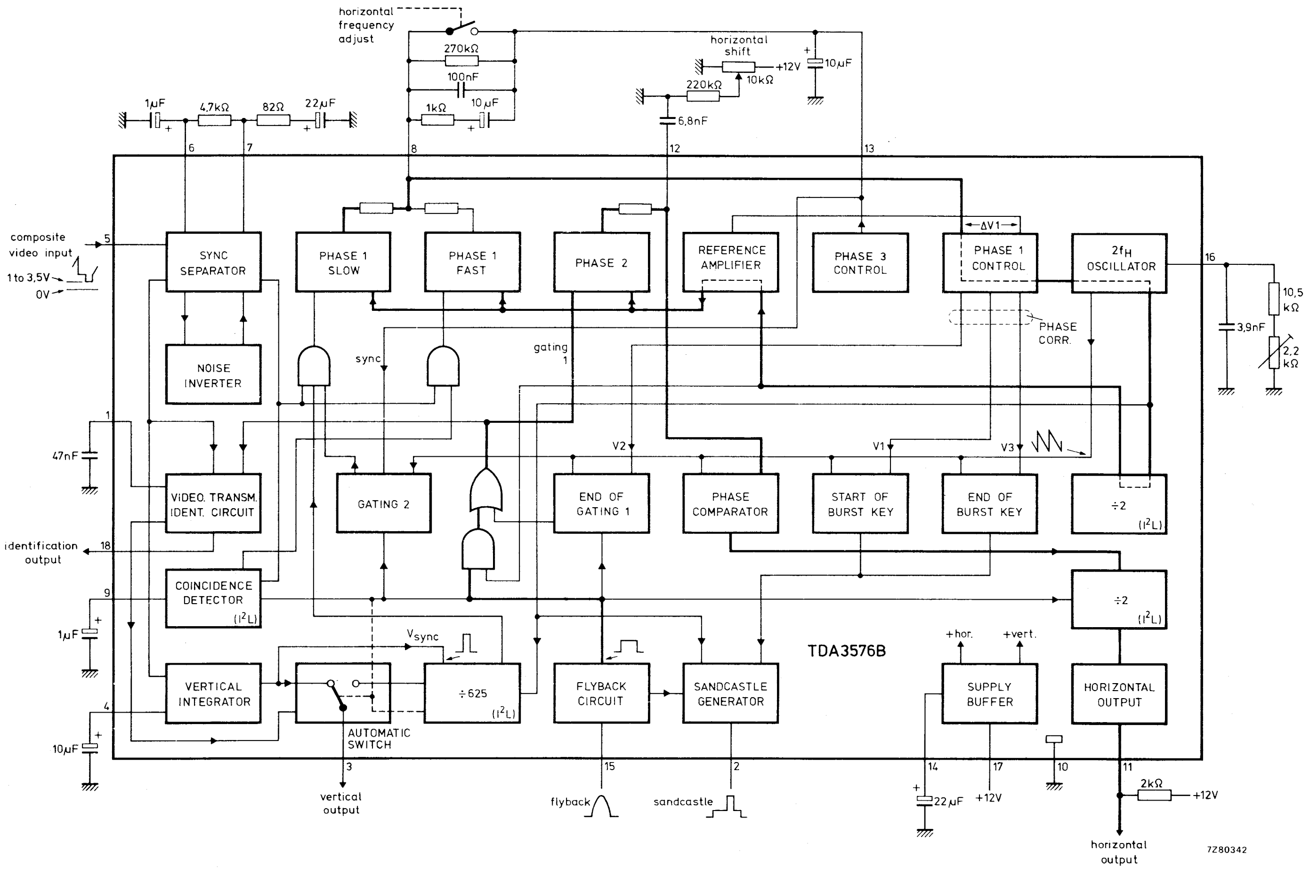


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The video input voltage to drive the sync separator must have negative-going sync, which can be obtained from synchronous demodulators such as TDA2540 and TDA2541.

The slicing level of the sync separator is determined by the value of the resistor between pins 6 and 7. A 4,7 kΩ resistor provides a slicing level midway between the top sync level and the blanking level. Thus the slicing level is independent of the amplitude of the sync pulse input at pin 5.

The nominal top sync level at pin 5 is 3 V, and the amplitude selective noise inverter is activated at 0,7 V.

To obtain good stability the circuit contains three control loops. In the first loop the phase of the horizontal sync pulse is compared with a reference output pulse from the horizontal oscillator. In the second loop the phase of the flyback pulse is compared with the same reference output pulse. The first loop is designed for good noise immunity and the second loop has a fast time constant to compensate quickly for storage variations of the output stage. The second loop also generates a gating signal of about 5,5 μs for use in the transmitter identification circuit. The third control loop generates a second gating signal which is used in the first phase detector. The pulse width is typically 14 μs.

For a short catching time the output current of the first phase detector is not gated but is increased by 5 times during catching. This is caused by the voltage of the coincidence detector at pin 9. For VCR playback conditions the first control loop must be forced to a fast time constant, this is achieved by applying an external voltage of ≥ 2,7 V to pin 9.

The free running output frequency of the horizontal oscillator is 31,25 kHz. The vertical frequency output is obtained by dividing this double horizontal frequency by 625. The double horizontal frequency is fed via a binary divider to provide the normal 15,625 kHz horizontal output to pin 11.

The sandcastle pulse is generated at pin 2 and has three levels. The burst key pulse is of short duration, typically 4 μs, with an amplitude of 10 V and is the highest level. The second level has a pulse duration equal to the horizontal flyback pulse with an amplitude of 4,5 V and is used for horizontal blanking. The third level, amplitude 2,5 V, is used for vertical blanking and has a pulse duration of 1,34 ms. The last pulse is internally generated by the divider circuit and is only available when a standard video input signal is received. An external vertical blanking pulse can be added to this pin via a suitable series resistor. This pulse will be automatically clamped to 2,5 V.

DEVELOPMENT SAMPLE DATA

The automatic vertical sync block contains the following:

- 625 divider
- In/out-sync detector
- Direct/indirect sync switch
- Identification circuit

It is fed by a signal obtained by integration of the composite video signal and an internally generated, clipped video signal. The vertical sync pulse is sliced out of this integrated signal by an automatically biased clipper. The video part of the signal helps to build up a vertical sync when heavy negative-going reflections (mountains) distort the video signal. The in/out sync-detector considers a signal out-of-sync when fourteen or more successive incoming vertical sync pulses are not in phase with a reference signal from the 625 divider. Therefore a distorted vertical sync signal needs only one out-of-fourteen pulses to be in phase to keep the system in sync. When the fifteenth successive out-of-sync pulse is detected, the direct/indirect sync switch is activated to feed the vertical sync signal directly out of the block at pin 3 (direct sync vertical output).

At the same time the 625 divider is reset by one of the sync pulses. After the reset pulse, if the 7th sliced vertical sync pulse coincides with a 625 divider window, the sync output pulse is presented again by the divider system and switch-over to indirect mode occurs.

In the direct mode, every 7th non-coinciding sliced vertical sync pulse will reset the counter. A non-standard video signal will result in continuous reset pulses and the direct/indirect switch will remain in the direct position.

FUNCTIONAL DESCRIPTION (continued)

To avoid delay in vertical synchronization, caused by waiting time of the divider circuit after channel change or an unsynchronized camera change in the studio, information is fed from the horizontal coincidence detector to the automatic switch for the vertical sync pulse. The loss of horizontal synchronization sets the automatic switch to direct vertical sync.

When an external voltage between 2,7 V and 8,2 V is applied via pin 9 to the coincidence detector, the horizontal phase detector is switched to a short time constant and the automatic switch to direct vertical sync. A voltage level on pin 9 between 9,2 V and 12 V switches the horizontal phase detector to a short time constant, without affecting the indirect/direct vertical sync system which remains operational. Thus when standard signals are received vertical sync pulses are generated by the divider system.

To avoid disturbance of the horizontal phase detector by the vertical sync pulse the 625 divider system generates an anti-top-flutter pulse. This pulse is applied to the phase 1 detector when a standard video signal is received. The anti-top-flutter pulse is also active for standard VCR signal conditions, voltage at pin 9 $\geqslant$ 9,2 V.

The video transmitter identification circuit detects when a sync pulse occurs during the internal 5,5 μs gating pulse. This indicates the presence of a video transmitter and results in the capacitor connected to pin 1 being charged to 8,4 V. When no sync pulse is present the capacitor discharges to $<$ 1 V. The voltage at pin 1 is compared with an internal d.c. voltage. The identification output at pin 18 is active when pin 1 is $\leqslant$ 1,5 V (no video transmitter) and inactive (high impedance) when pin 1 is $>$ 3,5 V, this information can be used for search tuning.

The vertical sync output pulse at pin 3 is inhibited when no video transmitter is identified, which prevents interference or noise affecting the frequency of the vertical output stage. This results in a vertical stable picture, plus vertical stable position information for tuning systems.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 17)	$V_P = V_{17\text{-}10}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1200	mW
Storage temperature range	T_{stg}	−55 to	+125	°C
Operating ambient temperature range	T_{amb}	−25 to	+65	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	=	50	K/W

CHARACTERISTICS

$V_P = V_{17\text{-}10} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 17)					
Supply voltage range	$V_P = V_{17\text{-}10}$	10,5	12	13,2	V
Supply current ($V_{17\text{-}10} = 12$ V)	I_{17}	50	70	85	mA
Buffer voltage ($V_{17\text{-}10} = 12$ V)	$V_{14\text{-}10}$	10,5	11	11,5	V
Sync separator and noise gate (pin 5)					
Top sync level (note 1)	$V_{5\text{-}10}$	1,0	3,0	3,5	V
Sync pulse amplitude (note 2) (peak-to-peak value)	$V_{5\text{-}10(p\text{-}p)}$	0,1	0,6	–	V
Slicing level (note 3)		35	50	65	%
Delay between sync input at pin 5 and phase detector output at pin 8*	t_d	–	0,35	–	μs
Noise gate switching level	$V_{5\text{-}10}$	–	0,7	1,0	V
Phase detector (pin 8)					
Control voltage	$V_{8\text{-}10}$	0,4	2,7	5,2	V
Control sensitivity (note 7)					
with slow time constant		–	1,0	–	V/μs
with fast time constant		–	1,0	–	V/μs
with slow time constant▲		–	0,7	–	V/μs
Phase-locked-loop (pins 8 and 13)					
Holding range (note 4)	Δf	–	± 1000	–	Hz
Catching range (note 4)	Δf	–	± 900	–	Hz
Control sensitivity video					
with respect to oscillator**		–	2,0	–	kHz/μs
with respect to oscillator▲		–	1,5	–	kHz/μs
with respect to burst key pulse		–	7,5	–	kHz/μs
with respect to flyback pulse		–	4	–	kHz/μs
Phase modulation due to hum on the supply line; pin 17 (note 4)		–	–	1,0	μs/V

DEVELOPMENT SAMPLE DATA

* See waveforms Fig. 2.

** Without resistor between pins 8 and 13.

▲ 270 kΩ between pins 8 and 13.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase detector (pin 12)					
Control voltage (t_d = 10 μs)	$V_{12\text{-}10}$	–	4,0	–	V
Control sensitivity		–	30	–	V/μs
Loop gain phase control *	$\Delta t_d/\Delta t_o$	–	250	–	μs/μs
Control range					
C = 6,8 nF (pin 12)*	t_d	6,5	–	24	μs
C = 100 nF (pin 12)*	t_d	2,2	–	24	μs
Phase adjustment					
control sensitivity		–	12	–	μA/μs
control range		−1,5	–	+3	μs
Horizontal oscillator (pin 16)					
Output frequency; C_{osc} = 3,9 nF; R_{osc} = 11,5 kΩ					
free running	f_o	–	31,250	–	kHz
at pin 11	f_{11}	–	15,625	–	kHz
Temperature coefficient	TC	–	$+3\times10^{4}$	–	K^{-1}
Frequency variation					
without tolerance of external components	Δf_o	–	–	±4	%
when supply voltage (pin 17) increases from 10 V to 13,2 V	Δf_o	–	0,2	–	%
at minimum supply voltage	Δf_o	–	1,5	5,0	%
Horizontal output (pin 11; note 5)					
Maximum supply voltage	$V_{17\text{-}10}$	–	–	13,2	V
Voltage at which output is started	$V_{17\text{-}10}$	6,2	6,7	7,2	V
Output voltage high level	$V_{11\text{-}10}$	–	–	13,2	V
Output voltage low level					
I_{11} = 10 mA	$V_{11\text{-}10}$	–	200	400	mV
I_{11} = 50 mA	$V_{11\text{-}10}$	–	500	700	mV
Output current at voltage low level	I_{11}	–	–	50	mA
Duration of the output pulse	t_p		see note 6		μs
Rise time of the output pulse	t_r	0,05	–	0,3	μs
Protection voltage (pin 11)		13	14,5	15,5	V

* See waveforms Fig. 2.

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse (pin 2)*					
Output voltage during burst key pulse (peak-to-peak value)	$V_{2\text{-}10(p\text{-}p)}$	9	10	—	V
Duration of upper level of output pulse	t_p	3,6	4,0	4,4	µs
Amplitude of second level of output pulse (peak-to-peak value)	$V_{2\text{-}10(p\text{-}p)}$	4,0	4,5	5,0	V
Duration of second level of output pulse	t_p		flyback pulse		µs
Amplitude of lower level of output pulse (peak-to-peak value)	$V_{2\text{-}10(p\text{-}p)}$	2,0	2,5	3,0	V
Duration of lower level of output pulse during standard signals (note 8)	t_p	—	1,34**	—	ms
Amplitude at zero level of output pulse	$V_{2\text{-}10}$	—	—	1	V
Delay between start of the sync pulse at pin 5 and the rising edge of the burst key pulse at pin 2	t_b	4,6	4,9	5,2	µs
Phase detector (pin 13)					
Output voltage	$V_{13\text{-}10}$	—	2,8	—	V
Charge current	I_{13}	—	0,9	—	mA
Discharge current	I_{13}	—	0,9	—	mA
Vertical sync pulse (pin 3)					
Output voltage (peak-to-peak value)	$V_{3\text{-}10(p\text{-}p)}$	10	—	—	V
Output current	I_3	—	—	5	mA
Duration of output pulse during indirect synchronization	t_p	—	190	—	µs
Phase variation between first vertical sync pulse and start of output pulse in divider mode		—	—	± 2,5	lines
Coincidence detector (pin 9)					
Switching level (note 7)	$V_{9\text{-}10}$	2,1	2,4	2,7	V
Voltage					
normal conditions (in-sync)	$V_{9\text{-}10}$	—	1,3	—	V
out-of-sync	$V_{9\text{-}10}$	—	2,7	—	V
during noise	$V_{9\text{-}10}$	—	2,1	—	V

---

* See waveforms Fig. 2.
** 21 lines.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Switching levels for VCR (pin 9)					
Fast time constant for phase 1					
switching level	V_{9-10}	2,1	2,4	2,7	V
input current	I_9	1,0	–	2,0	mA
Vertical sync output indirect/direct with divider system active					
switching level*	V_{9-10}	8,2	8,7	9,2	V
input current	I_9	3,0	–	4,0	mA
Flyback input pulse (pin 15)					
Switching level	V_{15-10}	–	0,85	1,0	V
Input pulse (peak-to-peak value)	$V_{15-10(p-p)}$	–	–	12	V
Input resistance	R_{15-10}	–	3,5	–	kΩ
Input current	I_{15}	0,2	–	3,0	mA
Delay between the start of the sync pulse at the video input and the leading edge of the flyback pulse	t_d	–	0,5	–	μs
Video transmitter identification circuit					
Pin 1					
Sync pulse present					
charge current	I_1	–	+100	–	μA
output voltage	V_{1-10}	–	8,4	–	V
No sync pulse					
discharge current	I_1	–	–100	–	μA
output voltage	V_{1-10}	–	–	1	V
Switching level output stage					
pin 18 active when:	V_{1-10}	1,7	2,0	2,2	V
pin 18 inactive when:	V_{1-10}	3,0	3,5	4,0	V
Pin 18 (note 9)					
Sync pulse present					
output current inactive	I_{18}	–	–	1	μA
No sync pulse					
minimum available output current active (V_{18-10} = 7 V)	I_{18}	4,0	–	–	mA
maximum allowed output current	I_{18}	–	–	10	mA
output voltage active (I_9 = 1 mA)	V_{9-13}	10,5	11,0	V_{17-10}	V

* The maximum allowed voltage at pin 9 is V_P (pin 17).

Notes to characteristics

1. The video signal at pin 5 must have negative-going sync.
2. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
3. The slicing level is determined by the value of the resistor between pin 6 and pin 7. The 50% figure is obtained with a 4,7 kΩ resistor. The slicing level P is determined by the formula:

   $$P = \frac{R_S}{4880 + R_S} \times 100\%;$$ where R_S is the resistor between pins 6 and 7.
4. Values of external circuitry as shown in Fig. 1; the voltage in this ratio has a peak-to-peak value.
5. The horizontal output configuration is an open collector with internal high voltage protection during the off-state of the output transistor.
6. The horizontal output pulse width is determined by the horizontal flyback pulse. The circuit is designed such that the horizontal output transistor cannot be switched on during flyback, but is switched on directly after flyback. Thus t_p = switch-off delay of horizontal output stage plus flyback time.
7. When the voltage level at pin 9 is $< 2,1$ V, phase detector 1 (pin 8) is gated. When the level is $> 2,7$ V, the dynamical control sensitivity of the phase detector is raised such that the output current is increased by five times the original amount and the phase detector is not gated.
8. An external vertical blanking pulse can be applied to pin 2 via a series resistor. The required input current is 2 mA. This external pulse is clamped to 2,5 V by internal circuitry.
9. The video transmitter identification output stage at pin 18 consists of a p-n-p current source with an n-p-n emitter-follower.

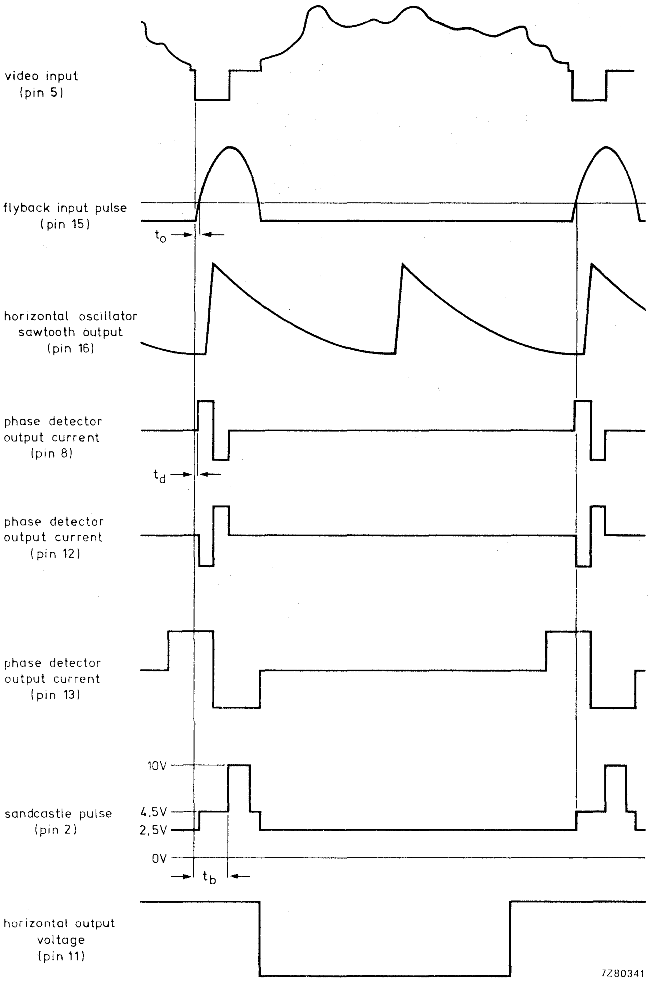


Fig. 2 Phase relationship between the input and output signals of the TDA3576B.

APPLICATION INFORMATION (see also Fig. 3)

The function is described against the corresponding pin number.

1. Video transmitter identification

A 47 nF capacitor must be connected to this pin. It charges to a level of 8 V when a sync pulse is detected, and discharges to a level of < 1 V when no sync pulse is detected.

2. Sandcastle output pulse

This output has three levels. The first and highest level (10 V) is the burst key pulse with a typical duration of 4,0 μs. The second level, for the horizontal blanking, is typically 4,5 V with a pulse duration equal to the horizontal flyback pulse. For the third level an external vertical flyback pulse must be applied to this pin. This pulse will be clamped to 2,5 V by an internal clamping circuit. The input current is typically 2 mA.

3. Vertical output pulse

This pulse is obtained from the 625 divider circuit when standard input signals are received or from the sync separator when the signals are non-standard. The pulse is inhibited when no video transmitter is detected. Both pulses have good stability and accuracy and are used to trigger the vertical oscillator.

4. Vertical sync pulse integrator biasing network

The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external capacitor of 10 μF is required for biasing the vertical sync separator, this provides the vertical sync output pulse with a delay of 37 μs. This value can be changed by an external resistor. A resistor of 470 kΩ between pin 3 and +12 V gives a delay of 45 μs.

5. Video input

The video input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation. The slicing level is fixed at 50% for the sync pulse amplitude range 0,1 to 1 V which provides good sync separation down to pulses with an amplitude of 100 mV peak-to-peak. The slicing level is increased for sync pulses in excess of 1 V peak-to-peak. The noise gate is activated at an input level < 1 V, thus when noise gating is required the top sync level should be close to the minimum level of 1 V.

6. Sync separator slicing level output

The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 7.

7. Black level detector output

The black level of the input signal is detected on this pin. This is required to obtain good sync separator operation. A 22 μF capacitor in series with a resistor of 82 Ω must be connected to this pin. A 4,7 kΩ resistor connected between pins 6 and 7 results in a slicing level of 50%.

8. Horizontal phase detector output and control oscillator input

The flywheel filter must be connected to this pin. Typical values for the components are a capacitor of 100 nF in parallel with an RC-network of 1 kΩ and 10 μF. Furthermore, a resistor of 270 kΩ should be connected between pins 8 and 13 to limit the free running frequency drift.

The output current of the phase detector depends on the condition of the coincidence detector. The output current is high when the oscillator is out-of-sync. The result is a large catching range, and the phase detector not gated. The output current is low when the oscillator is synchronized and the phase detector is gated; this provides good noise immunity.

APPLICATION INFORMATION (continued)

9. Coincidence detector output

A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal. The following output voltages can occur:

• when in-sync	1,3 V
• when out-of-sync	2,7 V
• during noise at the input	2,1 V

There are two switching levels at pin 9. At the first switching level when the output voltage is < 2,1 V, the phase detector output is low and the gating of the phase detector is switched on. When the output voltage is > 2,7 V, the output current of the phase detector is high and the gating of the phase detector is switched off. The result is a large catching range and a high dynamic steepness of the PLL. At the second switching level when the output voltage is > 9,2 V the sync system is switched to a short time constant while the indirect/direct vertical sync system remains fully operational. This condition is suitable for VCR application.

10. Negative supply (ground)

11. Horizontal sync pulse output

This is an open collector output. The collector resistor mus be chosen such that sufficient current is supplied to the driver stage. The maximum current is 60 mA. The circuit is designed such that the horizontal output transistor cannot be switched on during flyback, but is switched on directly after flyback.

12. Control voltage second loop

This voltage controls the output pulse at pin 11 (positive-going edge). The capacitor connected to this pin must have a minimum value of 6,8 nF. A higher value decreases the dynamic-loop gain in the second control loop. When a high dynamic-loop gain is not required a capacitor value of 100 nF is recommended. Horizontal shift is possible by applying an external current to pin 12.

13. Reference voltage control loops

The reference voltage must be decoupled by a capacitor of 10 μF.

14. Decoupling internal power supply

The IC has two power terminals. The main terminal (pin 17) supplies the output stages, the sync separator and the divider circuit. The specially decoupled terminal (pin 14) supplies the horizontal oscillator. The decoupling capacitor should be 22 μF.

15. Flyback input pulse

This pulse is required for the second phase control loop and for generating the horizontal blanking pulse in the sandcastle output. The input current must be at least 0,2 mA and not exceed 3 mA.

16. RC-network horizontal oscillator

Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part must be as small as possible, because of poor stability of variable carbon resistors. The oscillator can be adjusted when pins 8 and 13 are short circuited (see Fig. 3).

17. Positive supply

The supply voltage may vary between 10,5 and 13,2 V. The current-draw is typ. 70 mA and the range is 50 to 85 mA.

18. Video transmitter identification output

This is an emitter-follower output which will be inactive (high-impedance) when the level at pin 1 is > 4 V (video transmitter detected). The output will be active high when the level at pin 1 is < 1,7 V (no video transmitter detected). This feature can be used for search-tuning and sound-muting.

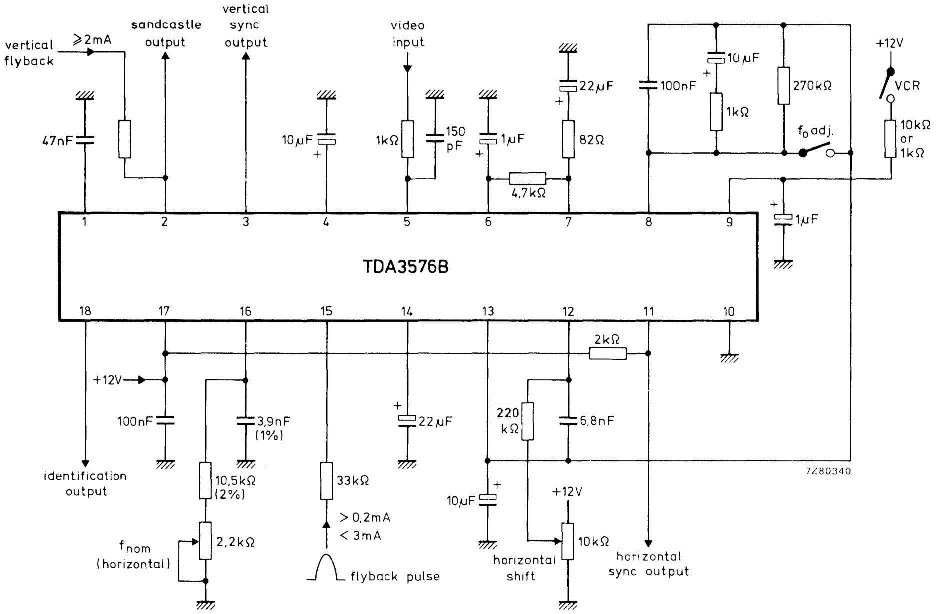


Fig. 3 Application circuit diagram.

DEVELOPMENT SAMPLE DATA

SECAM PROCESSOR CIRCUIT

The TDA3590 is a processor circuit that converts SECAM signals into sequential phase modulated signals. This circuit is intended to be used in combination with the TDA3560, TDA3561 or TDA3562 of which the 8,8 MHz oscillator signal is used as the carrier for the modulator. The TDA3590 incorporates the following functions:

- Limiter/amplifier for the chrominance signal
- SECAM demodulator
- Clamp circuit and de-emphasis for the colour difference signals
- Modulator to convert the colour difference signals in sequential phase modulated signals
- Identification circuit which can be used as:
  - horizontal identification
  - vertical identification
  - combination of hor./vert. identification
- Divider circuit which generates the 4,4 MHz carrier signal from the 8,8 MHz signal of the PAL-modulator oscillator
- Sandcastle pulse detector
- SECAM switch and PAL matrix
- Video amplifier

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{17\text{-}2}$	typ.	12	V
Supply current	$I_P = I_{17}$	typ.	90	mA
Chrominance amplifier and demodulator				
Input signal PAL (peak-to-peak value)	$V_{4\text{-}2(p\text{-}p)}$	typ.	550	mV
Input signal SECAM (peak-to-peak value)	$V_{4\text{-}2(p\text{-}p)}$	typ.	100	mV
Output signal PAL (peak-to-peak value)	$V_{8\text{-}2(p\text{-}p)}$	typ.	400	mV
Output signal SECAM (peak-to-peak value)	$V_{8\text{-}2(p\text{-}p)}$	typ.	1100	mV
Identification				
Input voltage for horizontal identification	$V_{5\text{-}2}$		0 to 8	V
Input voltage for vertical identification	$V_{5\text{-}2}$		10,5 to 12	V
Voltage at pin 6 for PAL	$V_{6\text{-}2}$	typ.	10,3	V
Voltage at pin 6 for SECAM	$V_{6\text{-}2}$	typ.	7	V
Sandcastle pulse detector				
Vertical blanking level	$V_{19\text{-}2}$	typ.	1,5	V
Horizontal blanking level	$V_{19\text{-}2}$	typ.	3,5	V
Burst gating level	$V_{19\text{-}2}$	typ.	7,0	V
Luminance amplifier				
Luminance input signal (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	typ.	0,5	V
Luminance output signal (peak-to-peak value)	$V_{15\text{-}2(p\text{-}p)}$	typ.	1	V
PAL-matrix and SECAM-switch				
Burst signal amplitude (peak-to-peak value)	$V_{11;12\text{-}2(p\text{-}p)}$	typ.	60	mV
Amplification for PAL		typ.	0	dB
Amplification for SECAM		typ.	6	dB

PACKAGE OUTLINE 24-lead DIL; plastic with heat spreader (SOT-101B).

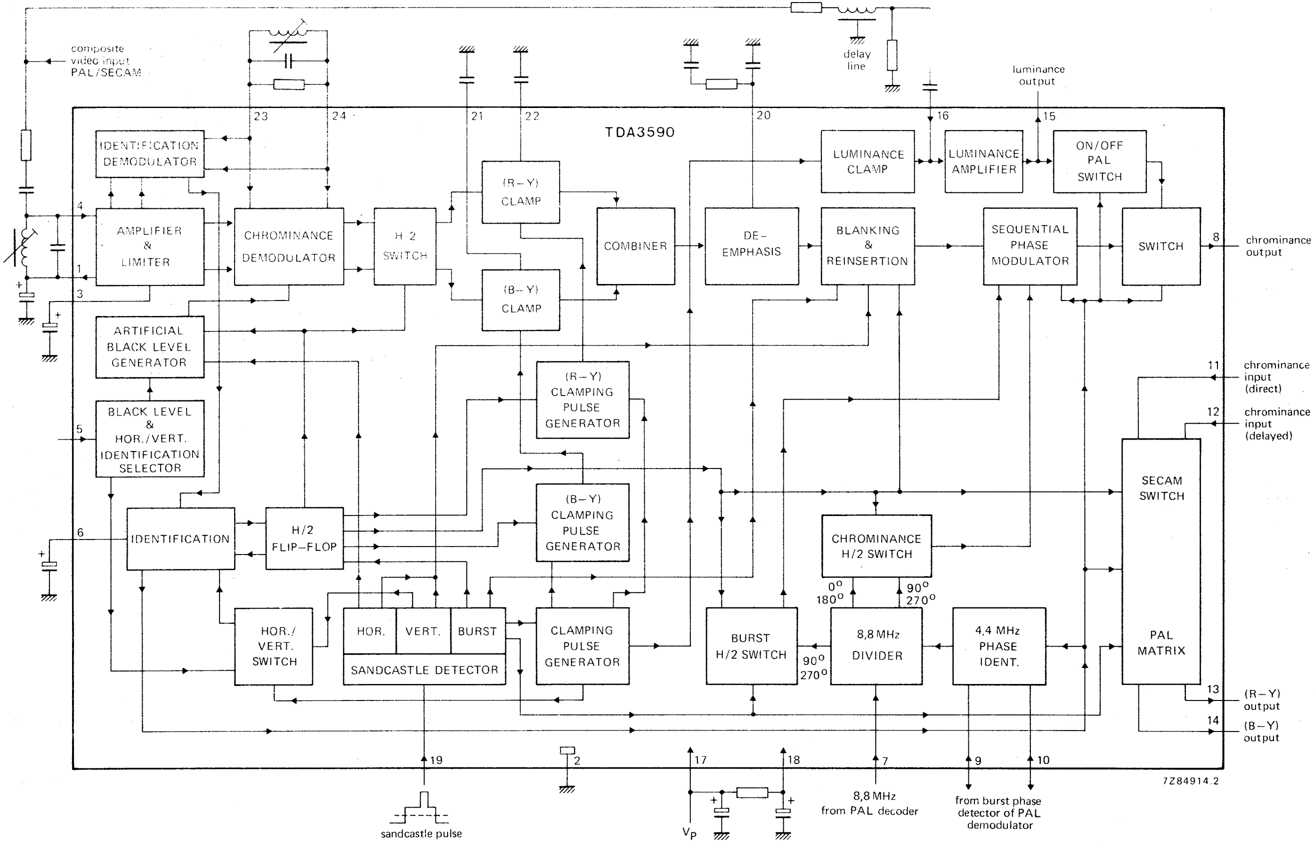


Fig. 1 Block diagram.

GENERAL DESCRIPTION

Demodulation

The TDA3590 comprises a chrominance and an identification demodulator, both using the same reference tuned circuit. The identification circuit automatically detects whether the incoming signal at pin 4 is SECAM or not (NTSC, PAL or black-and-white). When PAL signals are received, they are diverted via pin 16 to the chrominance output (pin 8).

The delay line connected to pin 16 delays the PAL luminance signal. The SECAM signal has the same delay in the processor circuitry. When SECAM signals are received, the PAL signal path is switched off. Then, the SECAM signal is applied to a limiter/amplifier (via a bandpass filter with a bell-shaped response, after which it is demodulated). The (R—Y) and (B—Y) signals are available sequentially, so only one demodulator is necessary. After demodulation the signals are applied to an H/2 switch, which separates the two colour difference signals. Now the signals are applied to the (R—Y) and (B—Y) clamp circuits, where the black levels are clamped to the same d.c. level. The optimum black level can be obtained at the end of the horizontal burst, so the timing of the (R—Y) and (B—Y) clamp is determined by an internally generated pulse of 800 ns, which starts just after the sandcastle burst gate pulse. The two signals are added again after clamping. The signal is applied to the modulator via a de-emphasis, blanking and reinsertion circuit.

If $V_{5-2} > 2$ V, artificial black levels are inserted during the horizontal blanking period. The clamp circuits then react upon these levels instead of the demodulated burst signals (necessary in case there are no horizontal burst signals available). The inserted signals may not be identical to the detected signals, because of circuitry spread. This can be corrected by detuning the demodulator tuned circuit.

Modulation

The (R—Y)/(B—Y) ratio is 1,78 at the de-emphasis output (pin 20). The demodulated (R—Y) and (B—Y) signals have a positive phase position for a magenta colour.

A burst signal is added to the demodulated SECAM signal at the input of the modulator. A sequential modulated chrominance signal is present at the modulator output. The modulation carriers of the (R—Y) and (B—Y) signals are 90° out of phase. The burst is modulated in the + (R—Y) direction and is only present during an (R—Y) line. The modulated (R—Y) component has the same phase position as the (R—Y) burst for a magenta colour.

Identification

The identification circuit compares the voltage difference, which is obtained after demodulation, with the phase of the flip-flop. For horizontal identification this comparison occurs during the internally generated 800 ns pulse. Only SECAM signals have a voltage difference from line to line during comparison. If the phase relationship between both the signals is wrong, the flip-flop will get a reset with an extra input pulse.

The identification detector information is also used for colour killing and for switching to PAL, if required.

The identification (as above) occurs when the horizontal identification system is active. When the vertical identification system is switched on (pin 5), the system only compares the demodulator output voltage during line scanning of the vertical blanking. The further operation is identical to the horizontal identification.

Sandcastle pulse detector

The sandcastle pulse detector is able to handle a 3-level sandcastle pulse. It detects the various blanking and gating pulses and it generates the correct drive pulses for the clamping circuits.

GENERAL DESCRIPTION (continued)

Carrier generation

The carrier signal for the PAL modulator is obtained from the 8,8 MHz oscillator signal of the TDA3560. The frequency of this signal is divided-by-two to obtain 90° shift. These two signals are applied to the modulator. There is a possibility that the two dividers in the TDA3560 (pins 23 and 24) and the TDA3590 are out-of-phase. This can be corrected by connecting pins 9 and 10 of the TDA3590 to pins 24 and 23 of the TDA3560 respectively. At incorrect phase, the TDA3590 divider is reset and correct phase is obtained.

PAL-matrix and SECAM-switch

The colour difference signals are transmitted sequentially in the SECAM-system, so the modulated PAL-signal from the TDA3590 is also sequential. The consequences are:

- The two colour difference signals are mixed again in the delay line matrix circuit, so that both demodulators get a combination of an (R—Y) and (B—Y) signal. The phase position of the reference carrier must be very accurate for obtaining a proper demodulated signal, otherwise colour errors will occur (e.g. in the NTSC-system).
- Two different signals are added or subtracted in the matrix circuit, which results in an amplitude that has half the amplitude when compared with a normal PAL signal.

  Increase of the chrominance signal in the TDA3590 results in an overdrive of the chrominance amplifier of the TDA3560.

These effects can be avoided by the matrix and switching circuit which is included in the TDA3590. The direct and delayed (from the PAL delay line) signals are applied to the processor where they are matrixed (for PAL) or switched (for SECAM). In the latter condition, the gain of the circuit is twice as high as for the normal PAL reception. The phase accuracy is not critical in this situation, because the two colour difference signals are not mixed.

For SECAM, the (B—Y) output of the SECAM-switch will be a signal without burst. The (R—Y) output of the SECAM-switch only has a burst during the +(R—Y) line. This burst is modulated in the +(R—Y) direction.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{17\text{-}2}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

Supply voltage	$V_P = V_{17\text{-}2}$	typ. 	12 10,8 to 13,2	V V
Supply current	$I_P = I_{17}$	typ.	90	mA
Total power dissipation	P_{tot}	typ.	1,1	W

Chrominance amplifier and demodulator

Input signal PAL (peak-to-peak value)	$V_{4\text{-}2(p\text{-}p)}$	typ. 	550 55 to 1100	mV mV
Input signal SECAM (peak-to-peak value)	$V_{4\text{-}2(p\text{-}p)}$	typ. 	100 15 to 300	mV mV
Input current	I_4	typ.	5	μA
Input capacitance	$C_{4\text{-}2}$	<	5	pF
(R−Y)/(B−Y) ratio before modulation (pin 20)		typ.	1,78	
Relative deviation of the black level of the colour difference signals before modulation	see note 1			
Output signal PAL (peak-to-peak value)	$V_{8\text{-}2(p\text{-}p)}$	typ.	400	mV
Output signal SECAM (peak-to-peak value)	$V_{8\text{-}2(p\text{-}p)}$	typ.	1100	mV
Output impedance	$\lvert Z_{8\text{-}2}\rvert$	typ.	50	Ω
Input voltage for clamping on the back-porch of the colour difference signals	$V_{5\text{-}2}$	<	0,5	V
Input voltage for insertion of the artificial black level after demodulation	$V_{5\text{-}2}$	>	2	V
Input resistance between pins 23 and 24	$R_{23\text{-}24}$	typ.	4	kΩ
Input capacitance between pins 23 and 24	$C_{23\text{-}24}$	typ.	17	pF
Input current at pin 5 $V_{5\text{-}2} = 12$ V	I_5	<	25	μA
Output current at pin 5 $V_{5\text{-}2} = 0$ V	$-I_5$	<	25	μA

CHARACTERISTICS (continued)

Identification

Input voltage for horizontal identification	V_{5-2}		0 to 8	V
Input voltage for vertical identification	V_{5-2}		10,5 to 12	V
Voltage at pin 6 for PAL	V_{6-2}	typ.	10,3	V
Voltage at pin 6 for SECAM	V_{6-2}	typ.	7	V
Identification 'on' for SECAM	V_{6-2}	typ.	10,7	V
Colour 'off' at SECAM	V_{6-2}	typ.	9,20	V
Colour 'on' at SECAM	V_{6-2}	typ.	9,05	V
Voltage at pins 9 and 10 for SECAM	$V_{9-2}; V_{10-2}$	typ.	10,5	V
Voltage between pins 9 and 10 for SECAM	V_{9-10}	<	3	mV
Permissible voltage at pins 9 and 10 for PAL	$V_{9-2}; V_{10-2}$		8,2 to 10,3	V

Sandcastle pulse detector and clamping pulse generator

Voltage level at which the vertical blanking pulse is separated	V_{19-2}	typ.	1,5	V
			1 to 2	V
required pulse amplitude	V_{19-2}		2 to 3	V
Voltage level at which the horizontal blanking pulse is separated	V_{19-2}	typ.	3,5	V
			3 to 4	V
required pulse amplitude	V_{9-12}		4 to 6,5	V
Voltage level at which the burst gating pulse is separated	V_{19-2}	typ.	7	V
			6,5 to 7,5	V
required pulse amplitude	V_{19-2}	>	7,5	V
Internal clamping pulse duration (see note 2)	t_p	typ.	0,8	μs
Input current at $V_{19-2} = 7$ V	I_2	typ.	10	μA

Carrier generator (see note 3)

Input signal from TDA3560 (peak-to-peak value)	$V_{7-2(p-p)}$	>	150	mV
Input resistance	R_{7-2}	typ.	4,4	kΩ

Luminance amplifier

Input signal (peak-to-peak value)	$V_{16-2(p-p)}$	typ.	0,5	V
Output signal (peak-to-peak value) at $V_{16-2(p-p)} = 0,5$ V	$V_{15-2(p-p)}$	typ.	1	V
Input current	I_{16}	typ.	0,15	μA
Output impedance (load: $R_{15-2} = 2$ kΩ)	$\|Z_{15-2}\|$	typ.	20	Ω
Frequency response (−3 dB)	f	>	8	MHz

PAL-matrix and SECAM-switch

Burst signal amplitude (peak-to-peak value)	$V_{11;12(p-p)}$	typ.	60	mV
Input impedance	$\|Z_{11;12-2}\|$	typ.	2	kΩ
Amplification for PAL		typ.	0	dB
Amplification for SECAM		typ.	6	dB
Difference in amplification from the inputs to one output for PAL		<	5	%
Phase error from line-to-line in the (R—Y) output for zero-error in the (B—Y) output for PAL		<	2,5°	
Output impedance	$\|Z_{13;14-2}\|$	typ.	40	Ω

Notes to the characteristics

1. When an artificial black level is inserted after demodulation, the resulting black level deviation depends on the adjustment of the demodulator tuned circuit. It is therefore possible to obtain a value of zero per cent.
2. This pulse starts directly after the burst clamping pulse.
3. The phase delay between the oscillator output of the TDA3560 and the input of the TDA3590 (pin 7) must be adjusted such, that the burst amplitude at pin 28 of the TDA3560 is minimum.

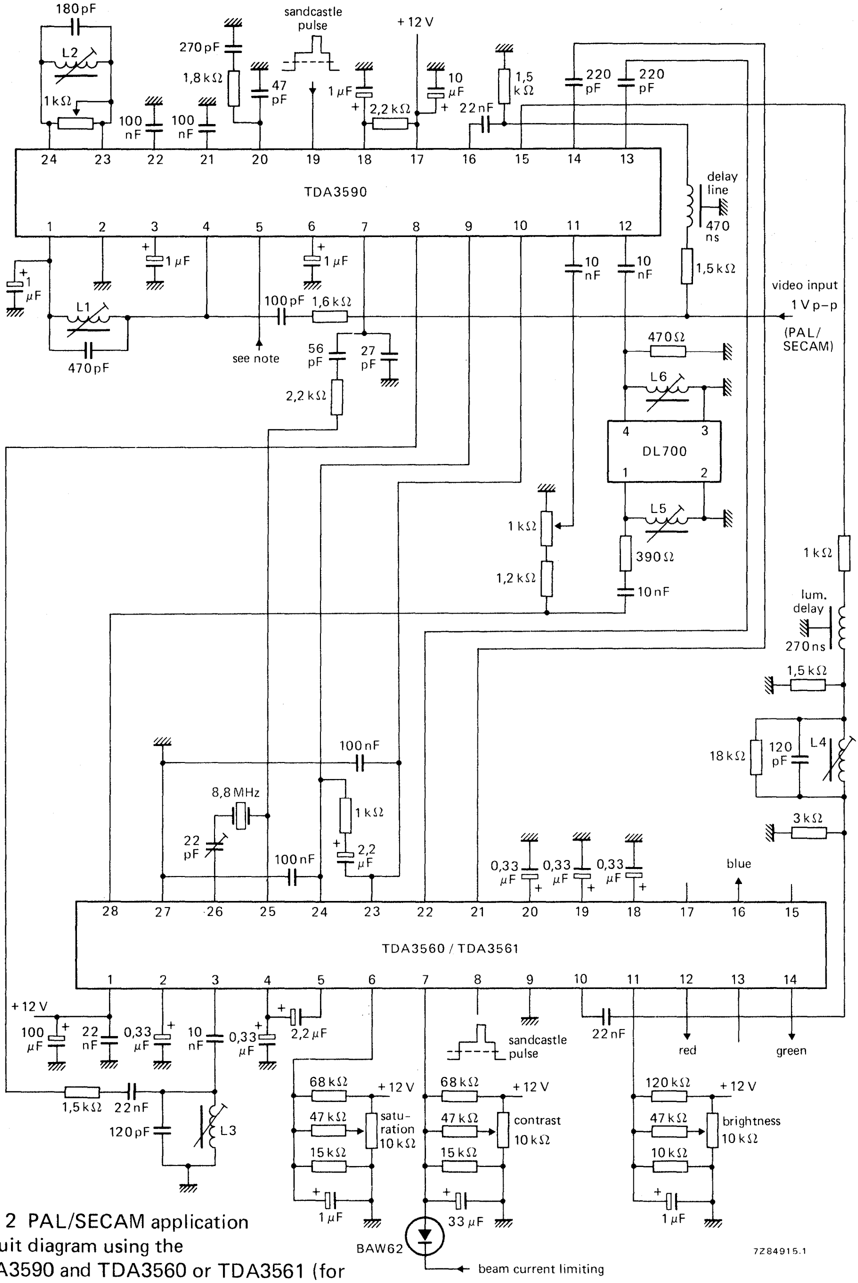


Fig. 2 PAL/SECAM application circuit diagram using the TDA3590 and TDA3560 or TDA3561 (for a combination with the TDA3562 see Fig. 3). For note to pin 5 of the TDA3590 see next page.

Note to Fig. 2

$V_{5\text{-}2} < 0,5$ V : horizontal identification and black level clamping.
$V_{5\text{-}2} > 10,5$ V : vertical identification and artificial black level.
$V_{5\text{-}2} = 5$ to 7 V: horizontal identification and artificial black level.

PINNING

1. Limiter feedback to pin 4.
2. Ground.
3. Limiter feedback.
4. Input limiter; PAL identification input; SECAM chrominance/identification input.
5. Via a d.c. voltage to this pin, the SECAM identification system can be chosen.
   At $V_{5\text{-}2} < 8$ V the processor is preset for horizontal identification.
   At $V_{5\text{-}2} > 10,5$ V the processor is preset for vertical identification.
   At $V_{5\text{-}2} < 0,5$ V the demodulated black level of the SECAM horizontal burst will be used as black level reference.
   At $V_{5\text{-}2} > 2$ V the demodulated chroma signal will have an artificial black level during the SECAM horizontal burst.
6. Store capacitor of PAL/SECAM identification circuit;
   horizontal identification: 100 nF
   vertical identification: 1 μF
7. Input of 8,8 MHz oscillator signal.
8. PAL/processed SECAM signal output (chrominance output).
9. Identification input of 8,8 MHz divider (to pin 24 of TDA3560).
10. Identification input of 8,8 MHz divider (to pin 23 of TDA3560).
11. Direct chrominance input of PAL matrix/processed SECAM switch.
12. Delayed chrominance input of PAL matrix/processed SECAM switch.
13. PAL/processed SECAM (R–Y) h.f. output.
14. PAL/processed SECAM (B–Y) h.f. output.
15. Luminance output.
16. Luminance/PAL input.
17. Positive supply voltage (+ 12 V).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input. It detects the various blanking and gating pulses and it generates the correct drive pulses for the clamping circuits.
20. De-emphasis is performed at this pin with a 1,8 kΩ resistor and a 270 pF capacitor. To avoid moiré patterns on the screen, additional filtering of the demodulator double-frequency products is obtained by a 47 pF decoupling capacitor.
21. Store capacitor (B–Y) clamp.
22. Store capacitor (R–Y) clamp.
23. Demodulator reference tuned circuit.
24. Demodulator reference tuned circuit. The demodulator reference circuit has to be tuned to a nominal frequency of about 4,33 MHz. The quality factor of the tuned circuit must be nominal 2,45.

APPLICATION INFORMATION (see Fig. 2)

The function is described against the corresponding pin number

Pin 4. Chrominance input

The SECAM input signal is typically 100 mV peak to peak, while the PAL input signal is about 550 mV peak to peak. This corresponds to a PAL/SECAM ratio of 5,5 (based on 75% saturated colour bar signals). The input signal, which should be free from any sound modulation, is applied single-ended to pin 4 via a filter which provides the required bell-shaped bandpass for SECAM signals. D.C. biasing takes place via coil L1, which has an unloaded quality factor between 80 and 100.

Pin 8. Chrominance output

During PAL reception, this output is internally connected to the luminance stage, therefore a composite video signal of 0,9 V peak to peak (typical) is present at the output. During SECAM reception, the chrominance output stage is connected to the modulator. The sequentially modulated (R—Y) and (B—Y) signals are then available at the output (amplitudes of typically 1100 mV peak to peak). These signals are applied via a chrominance bandpass filter to the chrominance a.c.c. amplifier in the TDA3560.

Pin 6. System identification

A 1 μF capacitor is connected to this pin. During PAL reception, the typical voltage at pin 6 is 10,3 V. The chrominance output stage is then internally connected to the luminance stage and the PAL matrix circuit is activated for normal matrixing of the PAL signals. During SECAM reception, the voltage at pin 6 is about 7 V (typical). The chrominance output stage is connected to the modulator and the SECAM switch is enabled. During noisy SECAM signals, the voltage at pin 6 increases and colour killing/unkilling occurs around 9,20 V and 9,05 V respectively.

Pin 5. Horizontal/vertical identification

Horizontal or vertical identification can be selected depending on the externally applied voltage at pin 5. When the d.c. level on pin 5 changes with time (pulse information), a combination of horizontal and vertical identification is possible.

Horizontal identification

If the voltage at pin 5 is < 2 V, horizontal identification occurs with black level clamping. This clamping occurs on the back-porch of the demodulated colour difference signals. If artificial black level insertion is required, the voltage at pin 5 should be < 8 V.

Vertical identification

If the voltage at pin 5 is $> 10{,}5$ V, vertical identification occurs, i.e. identification on 9 lines in the vertical blanking period. In this mode, the black level is artificially inserted after demodulation.

Pin 19. Sandcastle pulse

A 3-level sandcastle pulse is required and this can be directly coupled to the sandcastle pulse detector. Horizontal blanking, vertical blanking and burst clamping pulses are separated by the IC. A clamping pulse of 800 ns is generated internally just after the burst gating pulse. The input current is typically 10 μA at an input signal of 7 V.

Pins 16 and 15. Luminance input/output

The input signal at pin 16 should be typically 0,5 V peak to peak. The input impedance is relatively high, so a 22 nF coupling capacitor can be applied. This luminance signal is internally clamped and after a 2 times amplification available at pin 15.

During SECAM reception, the luminance signal is delayed by about 470 ns in a luminance delay line. The chrominance and luminance signals are then correctly timed at the output of the TDA3590.

During PAL reception, the composite video signal passes through this delay line and, after amplification, is available at pins 8 and 15. The nominal amplitude of the signals is 900 mV peak to peak in both cases.

Pins 11, 12, 13 and 14. SECAM switch and PAL matrix

During PAL reception, the system identification 'enables' the PAL matrix circuitry. An a.c.c. composite chroma signal (from pin 28 TDA3560) is coupled via the glass delay line to pin 12 of the TDA3590. A direct signal is applied to pin 11 of the TDA3590 via a resistor network. Active matrixing takes place in the IC and consequently (R—Y) and (B—Y) signals are available at pins 13 and 14 respectively. These signals are applied to the TDA3560 demodulators (pins 22 and 21 respectively).

During SECAM reception, the PAL matrix circuitry is 'disabled' and the SECAM switch is 'enabled'. A sequentially modulated (R—Y) and (B—Y) signal is available at pin 28 of the TDA3560. Direct and delayed signals are applied to pins 11 and 12 of the TDA3590, and via the SECAM switch the (R—Y) and (B—Y) signals are applied to their respective demodulator in the TDA3560.

Pins 17 and 18. Supply voltage (+ 12 V)

Correct operation is ensured within the supply range of 10,8 V to 13,2 V, and the typical power dissipation of the IC is 1,1 W at 12 V.

Pins 17 and 18 are separated by an external RC filter. Pin 18 is the supply for biasing several current-sinks in the IC and for all the output stages.

This supply voltage separation minimizes crosstalk via the supply lines between various parts of the circuitry. The capacitor at pin 18 must be small ($\approx 1\ \mu F$) so that, if pin 17 is short-circuited to ground, the collector-base junction of a transistor in the IC, through which the discharge current flows, is not damaged.

Pin 20. De-emphasis

De-emphasis is performed at this pin with a 1,8 kΩ and a 270 pF capacitor. To avoid moiré patterns on the screen, additional filtering of the 8,8 MHz signal is obtained by a 47 pF decoupling capacitor.

Pins 21 and 22. Clamping of (R—Y) and (B—Y) signals

After demodulation, the sequential (R—Y) and (B—Y) signals are separated by means of an H/2 switch and passed-on to their respective clamping circuits, where they are clamped to the same d.c. level. The value of each clamping capacitor should be 100 nF and they may, if desired, be increased to 470 nF.

Pins 23 and 24. Demodulator reference tuned circuit

The SECAM signal is applied to the demodulator via the 'bell-filter' and limiter/amplifier. Only one demodulator is used because of the sequential nature of the signal. The reference signal, obtained from the tank circuit, is applied to pins 23 and 24. At $V_{5\text{-}2} > 2$ V, the tuning and damping of the tank circuit should be done in such a way that a minimum modulator output voltage at pin 8 of the TDA3590 is obtained (the (R—Y) and (B—Y) information in the SECAM video signal is switched off). Therefore, any deviations between the black levels (when clamping on the back-porch and when an artificial black level is filled in) can be made minimum.

APPLICATION INFORMATION (continued)

Pin 7. Carrier generation

An 8,8 MHz signal from pin 25 of the TDA3560 is applied via pin 7 to the divider circuit in the TDA3590. Two 4,4 MHz signals are obtained with a phase shift of 90° with respect to each other. These signals are applied to the modulator via an H/2 switch. The phase delay of the 8,8 MHz input signal must be adjusted such that the burst amplitude of the chrominance signal at pin 28 (TDA3560) has its minimum amplitude. Under this condition, the burst generated by the TDA3590 is in phase with the (R−Y) reference signal for the demodulator in the TDA3560. Since the a.c.c. of the TDA3560 operates in the + (R−Y) direction, the burst signal at pin 28 of the TDA3560 will have its minimum amplitude.

Pins 9 and 10. Divider resetting

The output of the burst phase detector of the TDA3560 is connected to pins 9 and 10. At SECAM reception, the differential a.c. current information, obtained from the burst detector (TDA3560), is applied to pins 9 and 10 (TDA3590). This gives information about the phase relationship between the two 4,4 MHz dividers in both ICs. The TDA3590 now generates a minimum relative voltage between pins 9 and 10 at an absolute voltage level of 10,6 V. The result is that the oscillator control function of the TDA3560 is overruled, and the oscillator is set to 2 x 4,43 MHz.

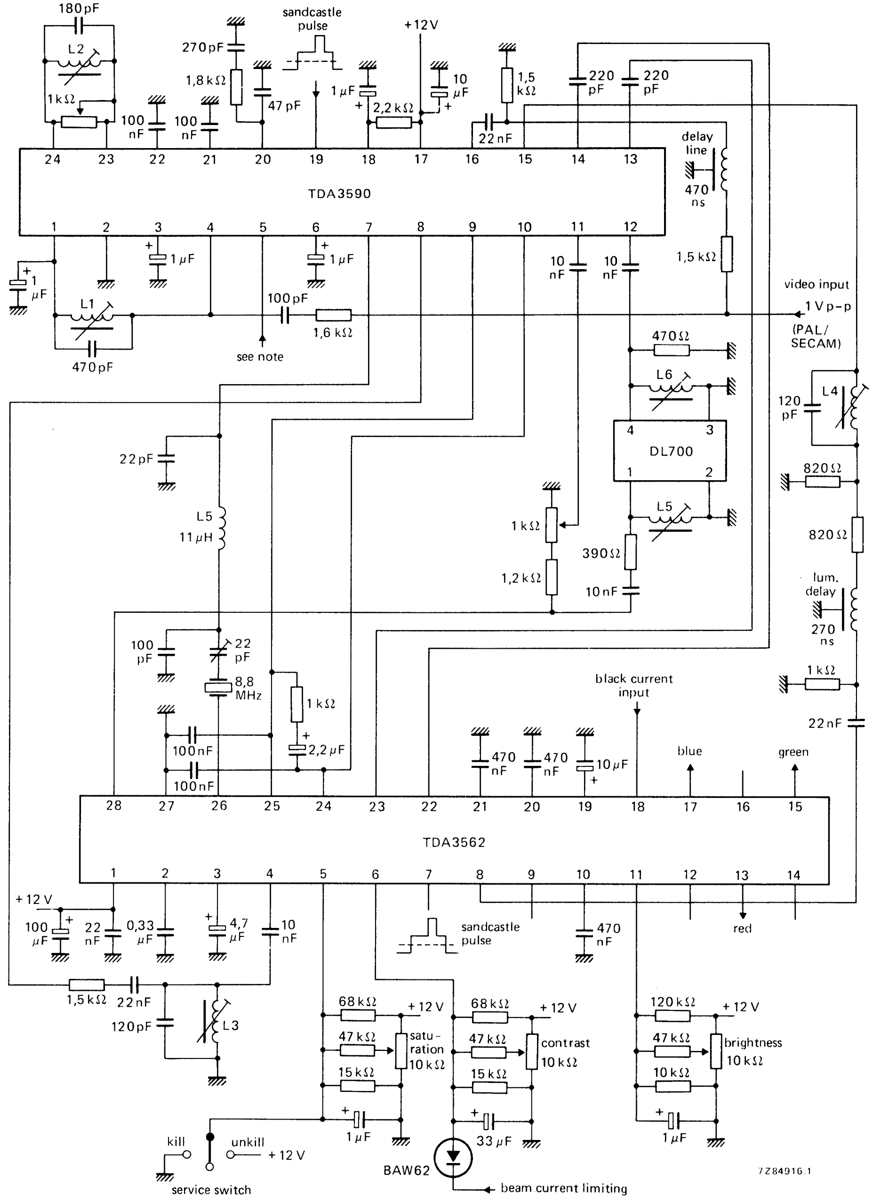


Fig. 3 PAL/SECAM application circuit diagram using the TDA3590 and TDA3562.
Note to pin 5 TDA3590: $V_{5\text{-}2} < 2$ V; horizontal identification and black level clamping.
$V_{5\text{-}2} > 10{,}5$ V; vertical identification and artificial black level.
$V_{5\text{-}2} = 5$ to 7 V; horizontal identification and artificial black level.

SECAM PROCESSOR CIRCUIT

GENERAL DESCRIPTION

The TDA3590A processor circuit converts SECAM signals into sequential phase-modulated (quasi-PAL) signals. It combines all the functions of the TDA3590, TDA3591 and TDA3591A to provide a complete SECAM processor system. The circuit is intended for use in conjunction with TDA3560, TDA3561, TDA3561A, TDA3562A or TDA3566 to provide SECAM/PAL/NTSC/black-and-white processor combinations.

Features

- Limiter/amplifier for chrominance signal
- SECAM demodulator
- Clamp circuits and de-emphasis for colour difference signals
- Modulator to convert colour difference signals into sequential, phase-modulated signals
- Identification circuit for horizontal, vertical or combined horizontal and vertical SECAM identification
- Divider circuit to provide 4,4 MHz carrier from 8,8 MHz signals generated in TDA3560/61/61A/62A/66
- Sandcastle pulse detector
- SECAM switch and PAL matrix
- Video amplifier
- Pin compatibility with TDA3590, TDA3591 and TDA3591A when application requires SECAM ident priority (does not apply with PAL ident priority)

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{17\text{-}2}$	typ.	12	V
Supply current	$I_P = I_{17}$	typ.	100	mA
Chrominance amplifier and demodulator				
Input signal PAL (peak-to-peak value)	$V_{4\text{-}2(p\text{-}p)}$	typ.	550	mV
Input signal SECAM (peak-to-peak value)	$V_{4\text{-}2(p\text{-}p)}$	typ.	100	mV
Output signal PAL (peak-to-peak value) at $V_{16(p\text{-}p)} = 1{,}2$ V	$V_{8\text{-}2(p\text{-}p)}$	typ.	900	mV
Output signal SECAM (peak-to-peak value)	$V_{8\text{-}2(p\text{-}p)}$	typ.	500	mV
Identification				
Input voltage range for horizontal identification (pin 5)	$V_{5\text{-}2}$		0 to 8	V
Input voltage range for vertical identification (pin 5)	$V_{5\text{-}2}$		10,5 to 12,0	V
Voltage at pin 6 for PAL	$V_{6\text{-}2}$	typ.	10,2	V
Voltage at pin 6 for SECAM	$V_{6\text{-}2}$	typ.	7,0	V
Sandcastle pulse detector				
Vertical blanking level	$V_{19\text{-}2}$	typ.	1,5	V
Horizontal blanking level	$V_{19\text{-}2}$	typ.	3,5	V
Burst gating level	$V_{19\text{-}2}$	typ.	7,2	V
Luminance amplifier				
Luminance input signal (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	typ.	1,2	V
Luminance output signal (peak-to-peak value)	$V_{15\text{-}2(p\text{-}p)}$	typ.	3,0	V
PAL matrix and SECAM switch				
Burst signal amplitude (peak-to-peak value)	$V_{11;\,12\text{-}2(p\text{-}p)}$	typ.	60	mV
Amplification for PAL		typ.	0	dB
Amplification for SECAM		typ.	6	dB

PACKAGE OUTLINE

24-lead DIL; plastic (with internal heat spreader) (SOT-101B).

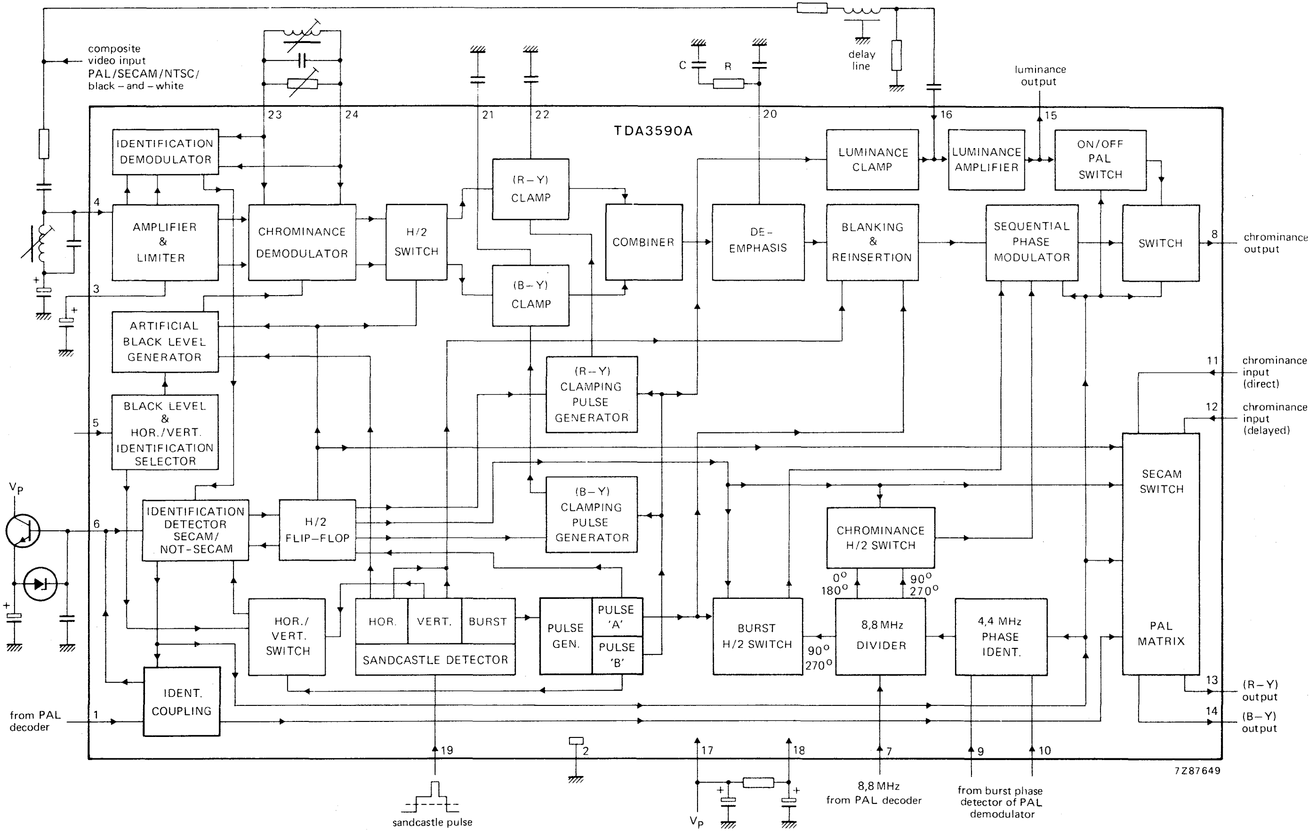


Fig. 1 Block diagram.

PINNING

1. Identification coupling input for PAL/not-PAL identification using half the saturation voltage of the PAL decoder.
2. Ground.
3. Limiter feedback.
4. SECAM video input.
5. Identification selection input using a d.c. level to preset the identification mode of horizontal/vertical detection + black level clamping/insertion.
6. Storage circuit input to SECAM/not-SECAM identification detector.
7. Divider circuit input of 8,8 MHz from the PAL decoder.
8. Chrominance signal output comprising PAL or processed SECAM (quasi-PAL).
9. Carrier signal phase identification input from the burst phase detector of the PAL decoder.
10. As for pin 9.
11. Direct chrominance input to SECAM switch/PAL matrix.
12. Delayed chrominance input to SECAM switch/PAL matrix.
13. Colour difference output (R-Y).
14. Colour difference output (B-Y).
15. Luminance output.
16. Luminance/PAL input.
17. Positive supply voltage (V_P).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input.
20. De-emphasis circuit connection.
21. Storage capacitor connection for (B-Y) clamp.
22. Storage capacitor connection for (R-Y) clamp.
23. Connection for reference tuned circuit for SECAM chrominance and identification demodulators.
24. As for pin 23.

FUNCTIONAL DESCRIPTION

Demodulation

The chrominance and identification demodulators of the TDA3590A both share the same reference tuned circuit (pins 23 and 24). The identification circuit automatically detects whether the incoming signal is SECAM or not-SECAM.

When the incoming signals are not-SECAM (PAL/NTSC/black-and-white) they are diverted via pin 16 to the chrominance output at pin 8 and no signal demodulation takes place. The delay line connected to pin 16 delays the signals to equalize the delay of the SECAM processor circuitry. When SECAM signals are received the PAL signal path is switched off.

Incoming SECAM signals are applied to pin 4 via an external bell filter. The signals are amplified, limited and then demodulated. The limiters give optimum i.f. interference suppression. Only one demodulator is necessary as the colour difference signals are available sequentially. After demodulation the colour difference signals are separated by an H/2 switch and then applied to (R-Y) and (B-Y) clamp circuits where the black levels are clamped to the same d.c. level. The optimum black level can be obtained at the end of the horizontal burst, so the timing of the (R-Y) and (B-Y) clamp is determined by the last 1,5 μs of the burst gate pulse.

The two colour difference signals are combined again after clamping and then applied to the modulator via de-emphasis, blanking and reinsertion circuits.

The ratio of (R-Y) to (B-Y) at the de-emphasis output (pin 20) is 1,78. The external de-emphasis components of R = 1 kΩ and C = 470 pF give a spread at the internal de-emphasis network < 20%.

FUNCTIONAL DESCRIPTION (continued)

If artificial black level reinsertion is required the burst gating pulse (Fig. 2) is used to time black level clamping. Artificial black levels are inserted during the horizontal blanking period when $V_{5\text{-}2} > 2$ V. The clamp circuits then react to the artificial levels instead of the demodulated burst signals (this is necessary when no horizontal burst signals are available). The inserted signals may not be identical to the demodulated signals because of circuitry spread but this can be corrected by detuning the demodulator reference tuned circuit.

Modulation

A burst signal is reinserted into the combined SECAM signal at the input to the sequential phase modulator. The nominal duration of this burst is 2,6 μs which approximates to the duration of the PAL burst and, in combination with the horizontal blanking pulse (used as keying pulse in the SECAM switch), minimizes interference in the a.c.c. loop of the TDA3560/61/62.

At the input to the modulator the (R-Y) and (B-Y) signals have a positive phase position for magenta colour. The modulation carriers for the (R-Y) and (B-Y) signals are 90° out of phase; the burst is modulated in the + (R-Y) direction and is only present during an (R-Y) line, the modulated (R-Y) component has the same phase position as the (R-Y) burst for magenta colour.

The chrominance output from pin 8, in the SECAM mode, is a quasi-PAL signal with alternate line, sequential modulation. Odd and even harmonics of the 4,4 MHz carrier introduced by the modulator are suppressed by internal filters. A correction is made to the burst-chrominance ratio of the quasi-PAL signals for equal saturation of PAL and SECAM signals.

Identification

Identification of the SECAM signal is performed using the fact that only SECAM has a line-to-line difference in demodulated voltage level. This is detected during the last 1,5 μs of the burst gate pulse. A flip-flop, which is switched by the burst gate pulse, provides the reference input to the identification detector. Here the phase of the flip-flop is compared with that of the changing voltage levels from the demodulator. The SECAM identification circuits operate when selected by the voltage on pin 5; this may be horizontal, vertical or combined horizontal and vertical identification, depending on the switching arrangements of pin 5. An internal voltage divider presets pin 5 to 6 V to give automatic selection of horizontal identification plus black level re-insertion. Vertical identification is selected by taking the voltage on pin 5 above 10,5 V, then the system compares the demodulator output voltage only during line scanning of the vertical blanking.

Information obtained from the identification detector is also used for colour killing and, if required, for switching to PAL.

Luminance amplification

The luminance amplifier input at pin 16 can be up to 1,2 V (peak-to-peak value) which equates to a peak-to-peak voltage of 2,7 V −7 dB. The amplifier gain is typically 8 dB. The luminance clamping circuit is activated during the SECAM identification timing (see Fig. 2).

Sandcastle pulse detection

The sandcastle pulse detector requires a three-level sandcastle pulse to provide horizontal blanking, vertical blanking and burst gate pulses. The detected burst gate pulse triggers a pulse generator which produces two timing pulses, pulse 'A' and pulse 'B' (see Fig. 2). Pulse 'A' is used to time the PAL burst modulator and to trigger the H/2 flip-flop. Pulse 'B' provides the timing of the (R-Y) clamp (present only during a red line); the (B-Y) clamp (present only during a blue line); the luminance clamp (present every line); and the SECAM horizontal identification circuit.

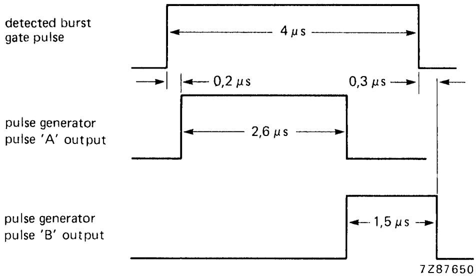


Fig. 2 Burst gate timing pulse generation.

PAL matrix and SECAM switch

The PAL matrix and SECAM switch is included in the TDA3590A to facilitate handling of the two chrominance signal types, PAL and SECAM. For PAL, the direct chrominance signal and the chrominance signal delayed by the PAL delay line are used by the PAL matrix to separate the two colour difference signals. Phase accuracy is not critical for this operation as the colour difference signals are not mixed. For SECAM, the quasi-PAL sequential colour difference signals are separated by switching. The gain of the switching circuit is two times that for normal PAL reception to maintain signal balance between the two systems. The (B-Y) output from the SECAM switch is a signal with no burst; the (R-Y) output has a burst modulated in the + (R-Y) direction during the + (R-Y) line. There is minimal crosstalk between the colour difference signals in the SECAM switch.

Carrier generation

The carrier for the sequential phase modulator is obtained using the 8,8 MHz input from the PAL decoder. This input is divided by two to provide two 4,4 MHz signals with a phase relationship of 90°. Correct phasing between the 4,4 MHz and the PAL decoder is ensured by the 4,4 MHz phase identifier circuit which resets the divider if the phasing is wrong (see Figs 3 and 4 for inter-connections). The inputs/outputs to the phase identifier have internal current sources in the case of SECAM.

Coupling of identification systems

Coupling of system identification between TDA3590A and a PAL decoder is performed using the functions of pins 1 and 6. The voltage level at pin 1 is controlled by the PAL/not-PAL detection of the PAL decoder; the voltage level at pin 6 is a function of SECAM/not-SECAM detection of the TDA3590A modified by the action of pin 6 external circuit.

The circuit action is as follows and is summarized in Table 1.

Channel switching	During channel switching pin 6 is taken rapidly to a high voltage (± 10,2 V) by the external circuit. This corresponds to the not-SECAM mode of the TDA3590A.
PAL	The high voltage level at pin 6 caused by channel switching is maintained by the TDA3590A when it recognizes the signal as not-SECAM. An internal current source keeps pin 6 voltage high, locking the TDA3590A in the not-SECAM mode. This condition is maintained even if reflected PAL signals are present. The PAL decoder recognizes the signal as PAL and takes pin 1 of TDA3590A to a voltage of between 0,5 and 2,6 V, depending on the setting of the saturation voltage. The system is thus locked in the PAL mode.

FUNCTIONAL DESCRIPTION (continued)

SECAM

The initial high voltage level (± 10,2 V) at pin 6 caused by channel switching sets the TDA3590A in the not-SECAM mode and during this time the PAL decoder detects a not-PAL signal. This causes a voltage at pin 1 of < 0,4 V which prevents the internal current source of TDA3590A maintaining the high voltage level of pin 6 which, in turn, allows the TDA3590A to detect SECAM. The initiation of SECAM detection is delayed by the action of pin 6 external circuit and commences when pin 6 approaches 9,1 V. The SECAM signals are converted by TDA3590A to quasi-PAL signals at pin 8 which are detected by the PAL decoder as PAL signals. The resulting modes of operation are SECAM for the TDA3590A and PAL for the PAL decoder, together giving a system operation in the SECAM mode.

Black-and-white

The TDA3590A is initially set in the not-SECAM mode as previously described. The PAL decoder detects not-PAL and the TDA3590A detects not-SECAM which results in a system operation in the colour-killing mode.

Table 1 System operating modes

TDA3590A mode	PAL decoder mode	system operating mode
SECAM	PAL	SECAM
SECAM	not-PAL	condition not used
not-SECAM	PAL	PAL
not-SECAM	not-PAL	black-and-white

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 17)	$V_P = V_{17\text{-}2}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,88 W
Operating ambient temperature range	T_{amb}		−25 to + 65 °C
Storage temperature range	T_{stg}		−25 to + 150 °C

CHARACTERISTICS

$V_P = V_{17\text{-}2} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified. The parameter values are valid only when the reference tuned circuit has been aligned as detailed in note 1.

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range (pin 17)	$V_{17\text{-}2}$	10,8	12,0	13,2	V
Supply current (pin 17)	I_{17}	–	100	–	mA
Input current (pin 18)	I_{18}	–	–	170	μA
Total power dissipation	P_{tot}	–	1,2	–	W
Chrominance amplifier and demodulator					
Input signal PAL (peak-to-peak value)	$V_{4\text{-}2(p\text{-}p)}$	–	–	1,1	V
Input signal SECAM (peak-to-peak value)	$V_{4\text{-}2(p\text{-}p)}$	15	100	300	mV
Input resistance (pin 4)	$R_{4\text{-}2}$	–	10	–	kΩ
Input capacitance (pin 4)	$C_{4\text{-}2}$	–	–	5	pF
(R-Y)/(B-Y) ratio before modulation (pin 20)		–	1,78	–	
Relative black level deviation of colour difference signals before modulation (note 2)					
Output signal PAL (peak-to-peak value) at $V_{16(p\text{-}p)} = 1{,}2$ V	$V_{8\text{-}2(p\text{-}p)}$	–	900	–	mV
Output signal SECAM (peak-to-peak value)	$V_{8\text{-}2(p\text{-}p)}$	–	500	–	mV
Output impedance	$\lvert Z_{8\text{-}2}\rvert$	–	65	–	Ω
Input voltage for clamping on back porch of colour difference signals	$V_{5\text{-}2}$	–	–	0,5	V
Input voltage for artificial black level insertion after demodulation	$V_{5\text{-}2}$	2	–	–	V
Input resistance between pins 23 and 24	$R_{23\text{-}24}$	–	4	–	kΩ
Input capacitance between pins 23 and 24	$C_{23\text{-}24}$	–	12	–	pF
Linearity of (B-Y) signal (pin 8) (note 3)		85	92	–	%
Linearity of (R-Y) signal (pin 8) (note 4)		88	95	–	%
Input resistance (pin 5)	$R_{5\text{-}2}$	–	10	–	kΩ
Chrominance demodulator zero point stability (pin 20) (note 5)	f_0	–	5	–	kHz
Offset (B-Y) black level (pin 8) at f_0 clamping; $f_{offset} = 4{,}4$ MHz		–	−15	–	kHz
Offset (R-Y) black level (pin 8) at f_0 clamping; $f_{offset} = 4{,}4$ MHz		–	−25	–	kHz

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification SECAM/not-SECAM					
Input voltage range for horizontal identification (pin 5)	$V_{5\text{-}2}$	0	–	8	V
Input voltage range for vertical identification (pin 5)	$V_{5\text{-}2}$	10,5	–	12,0	V
Voltage at pin 6 for PAL	$V_{6\text{-}2}$	–	10,2	–	V
Voltage at pin 6 for SECAM	$V_{6\text{-}2}$	–	7,0	–	V
Identification ON for SECAM	$V_{6\text{-}2}$	–	10,7	–	V
Colour OFF for SECAM	$V_{6\text{-}2}$	–	9,8	–	V
Colour ON for SECAM	$V_{6\text{-}2}$	–	9,1	–	V
Voltage at pins 9 and 10 for SECAM	$V_{9\text{-}2;\,10\text{-}12}$	–	10,5	–	V
Voltage between pins 9 and 10 for SECAM	$V_{9\text{-}10}$	–	–	3	mV
Permissible voltage range at pins 9 and 10 for PAL	$V_{9\text{-}2;\,10\text{-}2}$	6,8	–	10,2	V
Sandcastle pulse detector and clamping pulse generator					
Voltage level at which the vertical blanking pulse is separated	$V_{19\text{-}2}$	1,0	1,5	2,0	V
required pulse ampiitude (peak-to-peak value)	$V_{19\text{-}2(p\text{-}p)}$	2,1	–	2,9	V
Voltage level at which the horizontal blanking pulse is separated	$V_{19\text{-}2}$	3,0	3,5	4,0	V
required pulse amplitude (peak-to-peak value)	$V_{19\text{-}2(p\text{-}p)}$	4,1	–	6,6	V
Voltage level at which the burst gating pulse is separated	$V_{19\text{-}2}$	6,7	7,2	7,7	V
required pulse amplitude (peak-to-peak value)	$V_{19\text{-}2(p\text{-}p)}$	7,8	–	–	V
Input current at $V_{19\text{-}2}$ = 7 V	I_{19}	–	–	40	μA
Carrier generator (note 6)					
Input signal from TDA3560/61/61A/62A/66 (peak-to-peak value)	$V_{7\text{-}2(p\text{-}p)}$	150	–	–	mV
Input resistance	$R_{7\text{-}2}$	–	4	–	kΩ
Input capacitance	$C_{7\text{-}2}$	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
Luminance amplifier					
Input signal (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	–	1,2	1,7	V
Chrominance input signal when no luminance information is present (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	–	–	1	V
Gain (pin 16 to 15) at f_{16} = 4,4 MHz	$G_{16\text{-}15}$	–	8	–	dB
Input current (pin 16)	I_{16}	–	–	1	μA
Input resistance during clamping (pin 16)	$R_{16\text{-}2}$	–	4	–	kΩ
Output impedance (pin 15) at I_{15} = 2 mA	$\lvert Z_{15\text{-}2}\rvert$	–	20	–	Ω
Frequency response at –3 dB (pin 16 to 15)	f	6	–	–	MHz
Gain (pin 16 to 8) at f_{16} = 4,4 MHz; not-SECAM condition	$G_{16\text{-}8}$	–	7	–	dB
Frequency response at –3 dB (pin 16 to 8) not-SECAM condition	f	–	5	–	MHz
PAL matrix and SECAM switch					
Burst signal amplitude (peak-to-peak value)	$V_{11;\,12(p\text{-}p)}$	–	60	–	mV
Input resistance	$R_{11;\,12\text{-}2}$	–	900	–	Ω
Input capacitance	$C_{11;\,12\text{-}2}$	–	3	–	pF
Amplification for PAL	A	–	0	–	dB
Amplification for SECAM	A	–	6	–	dB
Difference in amplification from inputs to one output for PAL	ΔA	–	–	0,5	dB
Line-to-line phase error in (R-Y) output for zero error in (B-Y) output for PAL		–	–	3,5	deg
Output impedance	$\lvert Z_{13;\,14\text{-}2}\rvert$	–	50	–	Ω
Identification PAL/not-PAL					
Input condition for PAL (pin 1)	$V_{1\text{-}2}$	0,5	–	2,5	V
Input conditions for not-PAL (pin 1): lower voltage level	$V_{1\text{-}2}$	–	–	$<0,4$	V
upper voltage level	$V_{1\text{-}2}$	$>2,6$	–	–	V

DEVELOPMENT SAMPLE DATA

Notes to the characteristics

1. The parameter values given in the characteristics are valid only when the following alignment procedure is performed:
   a. Supply a SECAM signal input to pin 4 at 100 mV (peak-to-peak value) without deviation during a red and blue line (SECAM black colour information).
   b. Align the reference tuned circuit so that the output signal from pin 8 to the PAL decoder is minimum during scan (PAL black colour information).
2. When an artificial black level is inserted after demodulation the resulting black level deviation depends on the adjustment of the demodulator tuned circuit. It is therefore possible to obtain a value of 0%.
3. (B-Y) linearity is defined by $V_{out(yellow)}/V_{out(blue)}$ where f_{yellow} = (typ.) 4,02 MHz; f_{blue} = (typ.) 4,48 MHz; $V_{5\text{-}2} = 2{,}0$ V.
4. (R-Y) linearity is defined by $V_{out(cyan)}/V_{out(red)}$ where f_{cyan} = (typ.) 4,68 MHz; f_{red} = (typ.) 4,12 MHz; $V_{5\text{-}2} = 2{,}0$ V.
5. When the input signal to the limiter (pin 4) changes from 300 to 15 mV (peak-to-peak value) the zero point of the chrominance demodulator shifts by a typical value of 5 kHz.
6. The phase delay between the oscillator output of TDA3560/61/61A/62A/66 and the input to TDA3590A pin 7 must be adjusted for minimum burst amplitude at pin 28 of the PAL decoder.

APPLICATION INFORMATION

The pin-to-pin functions of the application shown in Fig. 3 are described against the corresponding pin numbers.

Pin 4. Chrominance input

Typical input signal values (peak-to-peak) are: SECAM 100 mV; PAL 0,55 V. The input signal, which should be free from any sound modulation, is applied single-ended to pin 4 via a filter which has the bell-shaped bandpass required for SECAM signals.

Pin 5. Horizontal/vertical identification

Selection of horizontal or vertical identification depends on the external voltage applied to pin 5. When the d.c. level on pin 5 changes with time (pulse information) a combination of horizontal and vertical identification is possible.

Horizontal identification

When the voltage at pin 5 is $< 0{,}5$ V horizontal identification and black level clamping occur. The clamping is during the back porch of the colour difference signals. If artificial black level insertion is required the voltage at pin 5 should be between 2 and 8 V.

Vertical identification

When the voltage on pin 5 is $> 10{,}5$ V vertical identification occurs (identification on 9 lines in the vertical blanking period). In this mode the black level is artificially inserted after demodulation.

Pin 6. System identification

During PAL reception the typical voltage at pin 6 is 10,2 V. This causes the luminance stage to be connected internally to the chrominance output at pin 8 and also activates the PAL matrix for normal PAL signals. During SECAM reception the typical voltage at pin 6 is 7 V. This changes the internal connection of the output from the luminance stage to the sequential phase modulator and enables the SECAM switch. Noisy SECAM signals cause the voltage at pin 6 to increase, colour killing occurs at 9,8 V and colour is reinstated at 9,1 V.

Pin 7. Carrier generation

An 8,8 MHz signal from the PAL decoder is applied via pin 7 to the divider circuit in the TDA3590A. From this two 4,4 MHz signals are obtained with a phase shift of 90° with respect to each other. These signals are applied to the modulator via an H/2 switch. The delay of the 8,8 MHz input must be adjusted for minimum burst amplitude of the chrominance signal at pin 28 of the PAL decoder. With this condition the burst generated by the TDA3590A is in phase with the (R-Y) reference signal for the PAL decoder demodulator (the a.c.c. of the PAL decoder operates in the + (R-Y) direction).

Pin 8. Chrominance output

During PAL reception this output is connected internally to the luminance stage and a composite PAL video signal is present at pin 8. During SECAM reception the sequential phase modulator is connected to this output to give a quasi-PAL signal from pin 8. Typical peak-to-peak amplitudes of the signal from pin 8 are 900 mV for PAL (with peak-to-peak input at pin 16 of 1,2 V) and 500 mV for SECAM. The output signals are applied via a chrominance bandpass filter to the chrominance a.c.c. amplifier input of the PAL decoder.

Pins 9 and 10. Divider resetting

The output of the PAL decoder burst phase detector is connected to pins 9 and 10 of TDA3590A. During SECAM reception this signal carries differential a.c. current information about the phase relationship of the 4,4 MHz dividers of both ICs. The TDA3590A generates a minimum relative voltage between pins 9 and 10 at an absolute voltage level of 10,5 V. This overrules the PAL decoder oscillator control function causing the oscillator to run at 2 x 4,43 MHz.

Pins 11, 12, 13 and 14. SECAM switch and PAL matrix

The PAL matrix circuit is enabled by system identification of PAL reception. The signal inputs to the matrix are the (direct) a.c.c. composite video output from the PAL decoder via an attenuator to pin 11 and a delayed version of the same signal via a glass delay line to pin 12. Active matrixing takes place in the IC and the separated (R-Y) and (B-Y) signals are available at pins 13 and 14 respectively.

The SECAM switch circuit is selected by system identification of SECAM reception. The inputs to the SECAM switch are the sequentially modulated quasi-PAL signals, direct and delayed, to pins 11 and 12 respectively. The SECAM switch separates the (R-Y) and (B-Y) signals which are then available at pins 13 and 14 respectively.

Pins 15 and 16. Luminance signals

The maximum peak-to-peak amplitude of the input to pin 16 should be 1,7 V. The relatively high input impedance of the luminance amplifier allows a 22 nF coupling capacitor to be used. The luminance amplifier has internal input clamping and a gain of 8 dB. The output is available at pin 15.

During SECAM reception the luminance signal is delayed approximately 470 ns by an external delay line to equalize the SECAM processing delay. The luminance and chrominance outputs are then correctly timed.

During PAL reception the PAL composite video signal passes through the external delay line and, after amplification, is available at pins 15 and 8.

APPLICATION INFORMATION (continued)

Pins 17 and 18. Supply voltage (+ 12 V)

Correct operation is ensured within the supply voltage range of 10,8 to 13,2 V. The typical power dissipation of the IC at 12 V is 1,2 W.

Pins 17 and 18 are separated by an external RC filter. Pin 18 supplies all the output stages and the biasing for several current sinks in the IC. Separation of the supply voltages minimizes crosstalk between the various parts of the IC. The capacitor at pin 18 must be small (≈ 1 μF) to avoid the possibility of internal damage to the IC by discharge current should pin 17 be short-circuited to ground.

Pin 19. Sandcastle pulse

The required three-level sandcastle pulse may be coupled directly to the sandcastle pulse detector input at pin 19. The horizontal blanking, vertical blanking and burst gate pulses are separated by the IC.

Pin 20. De-emphasis

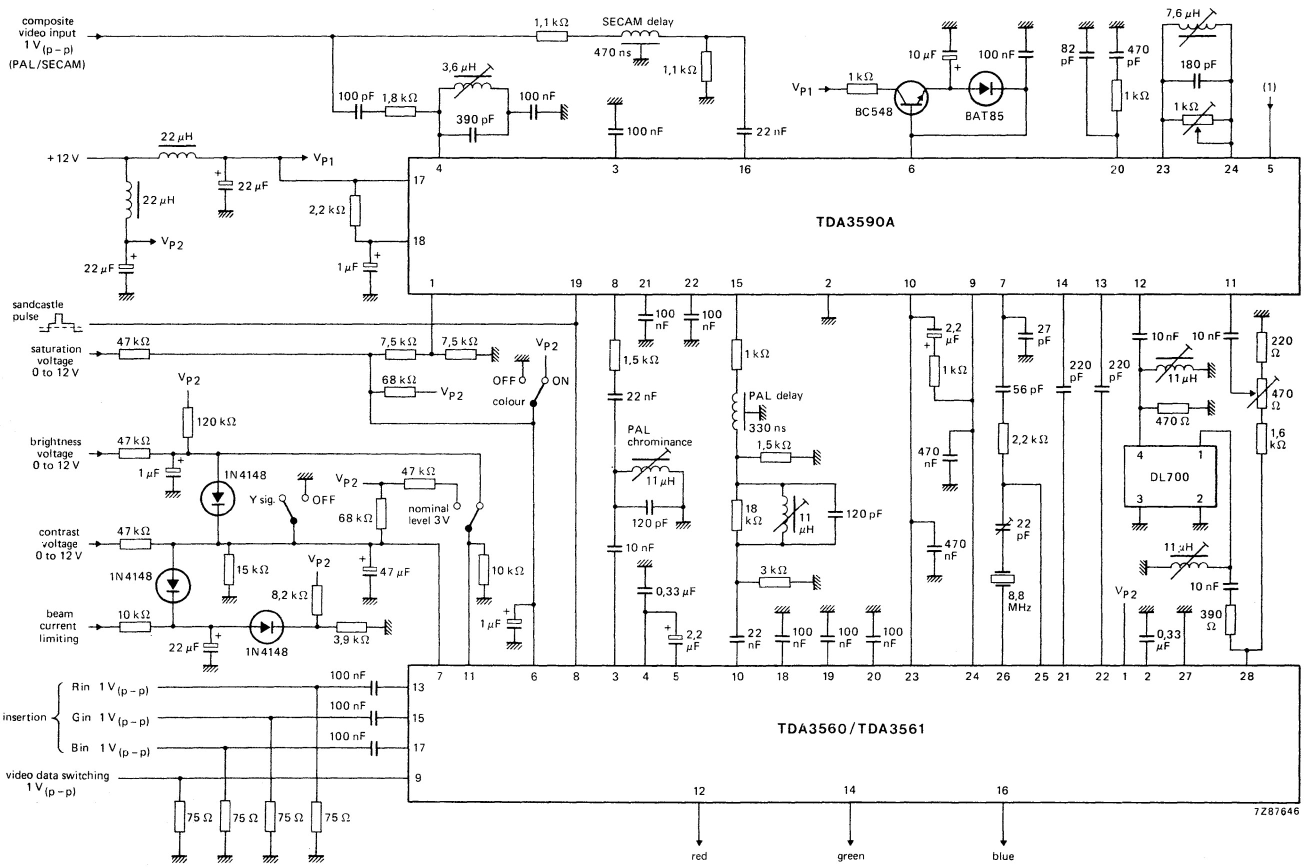
De-emphasis is performed at this pin with a 1 kΩ resistor and a 470 pF capacitor. Additional filtering of the 8,8 MHz signal using an 82 pF coupling capacitor prevents moiré patterns appearing on the screen.

Pins 21 and 22. Clamping of (R-Y) and (B-Y) signals

Clamping of the colour difference signals is performed after they have been separated. The normal value for the clamping storage capacitors is 100 nF but this may be increased to 470 nF if required.

Pins 23 and 24. Demodulator reference tuned circuit

The SECAM signal is applied to the demodulator via a bell filter and a limiter amplifier. Only one chrominance demodulator is used because of the sequential nature of the signal. The reference signal from the tuned circuit is applied to pins 23 and 24. Tuning and damping adjustments of the reference tuned circuit should be performed at $V_{5\text{-}2} > 2$ V (SECAM video (R-Y) (B-Y) information switched off). Adjustments should be such that minimum modulator voltage appears at pin 8, then any deviations between the black levels (when clamping on the back porch and when an artificial black level is filled in) can be made minimum.



(1) See Application Information for pin 5 – horizontal/vertical identification.

Fig. 3 PAL/SECAM decoder application.

APPLICATION INFORMATION (continued)

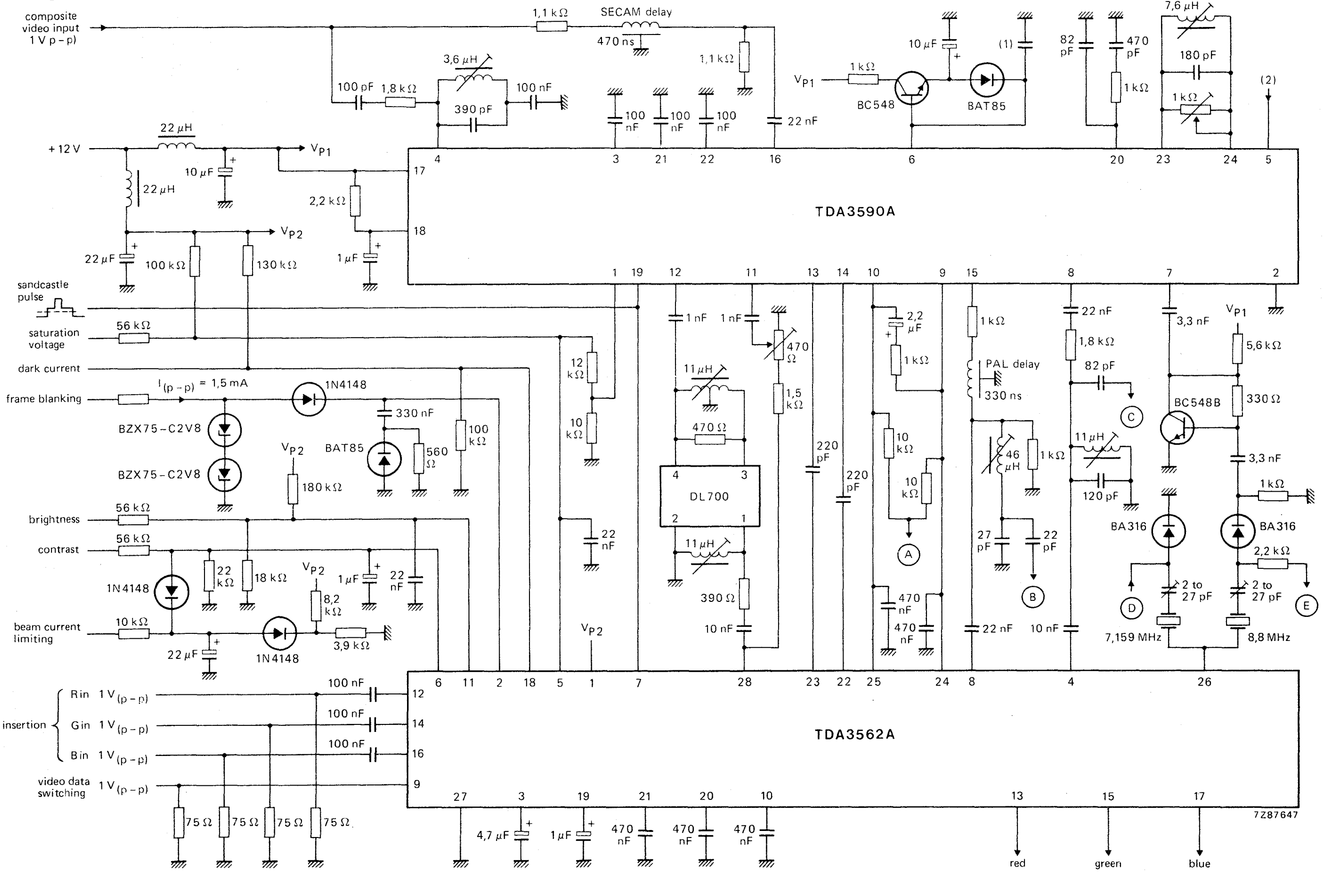
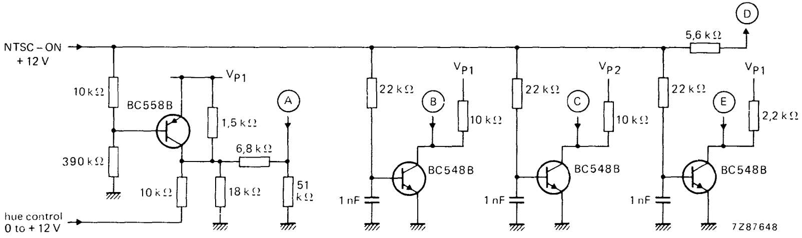


Fig. 4a PAL/SECAM/NTSC decoder application (continued in Fig. 4b).



(1) Capacitor value = 100 nF for horizontal identification or 1 μF for vertical identification.
(2) See Application Information for pin 5 – horizontal/vertical identification.

Fig. 4b PAL/SECAM/NTSC decoder application (continued from Fig. 4a).

SECAM PROCESSOR CIRCUIT

GENERAL DESCRIPTION

The TDA3591 is a processor circuit that converts SECAM signals into sequential phase-modulated signals. This circuit is intended to be used in combination with the TDA3560, TDA3561A or TDA3562A of which the 8,8 MHz oscillator signal is used as the carrier for the modulator.

Features

- Limiter/amplifier for the chrominance signal
- SECAM demodulator
- Clamp circuit and de-emphasis for the colour difference signals
- Modulator to convert the colour difference signals in sequential phase-modulated signals
- Identification circuit which can be used as:
  — horizontal identification — vertical identification — combination of hor./vert. identification
- Divider circuit which generates the 4,4 MHz carrier signal from the 8,8 MHz signal of the PAL-modulator oscillator
- Sandcastle pulse detector
- SECAM switch and PAL matrix
- Video amplifier

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{17\text{-}2}$	typ.	12	V
Supply current	$I_P = I_{17}$	typ.	90	mA
Chrominance amplifier and demodulator				
Input signal PAL (peak-to-peak value)	$V_{4\text{-}2(p\text{-}p)}$	typ.	550	mV
Input signal SECAM (peak-to-peak value)	$V_{4\text{-}2(p\text{-}p)}$		15 to 300	mV
Output signal PAL (peak-to-peak value)	$V_{8\text{-}2(p\text{-}p)}$	typ.	265	mV
Output signal SECAM (peak-to-peak value)	$V_{8\text{-}2(p\text{-}p)}$	typ.	1300	mV
Identification				
Input voltage for horizontal identification	$V_{5\text{-}2}$		0 to 8	V
Input voltage for vertical identification	$V_{5\text{-}2}$		10,5 to 12	V
Voltage at pin 6 for PAL	$V_{6\text{-}2}$	typ.	10,1	V
Voltage at pin 6 for SECAM	$V_{6\text{-}2}$	typ.	7	V
Sandcastle pulse detector				
Vertical blanking level	$V_{19\text{-}2}$	typ.	1,5	V
Horizontal blanking level	$V_{19\text{-}2}$	typ.	3,5	V
Burst gating level	$V_{19\text{-}2}$	typ.	7,2	V
Luminance amplifier				
Luminance input signal (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	typ.	0,45	V
Luminance amplifier gain at 4,4 MHz		typ.	5	dB
PAL-matrix and SECAM-switch				
Burst signal amplitude (peak-to-peak value)	$V_{11;12\text{-}2(p\text{-}p)}$	typ.	60	mV
Amplification for PAL (pin 13)		typ.	−0,3	dB
Amplification for PAL (pin 14)		typ.	−0,5	dB
Amplification for SECAM		typ.	5,5	dB

PACKAGE OUTLINE 24-lead DIL; plastic with heat spreader (SOT-101B).

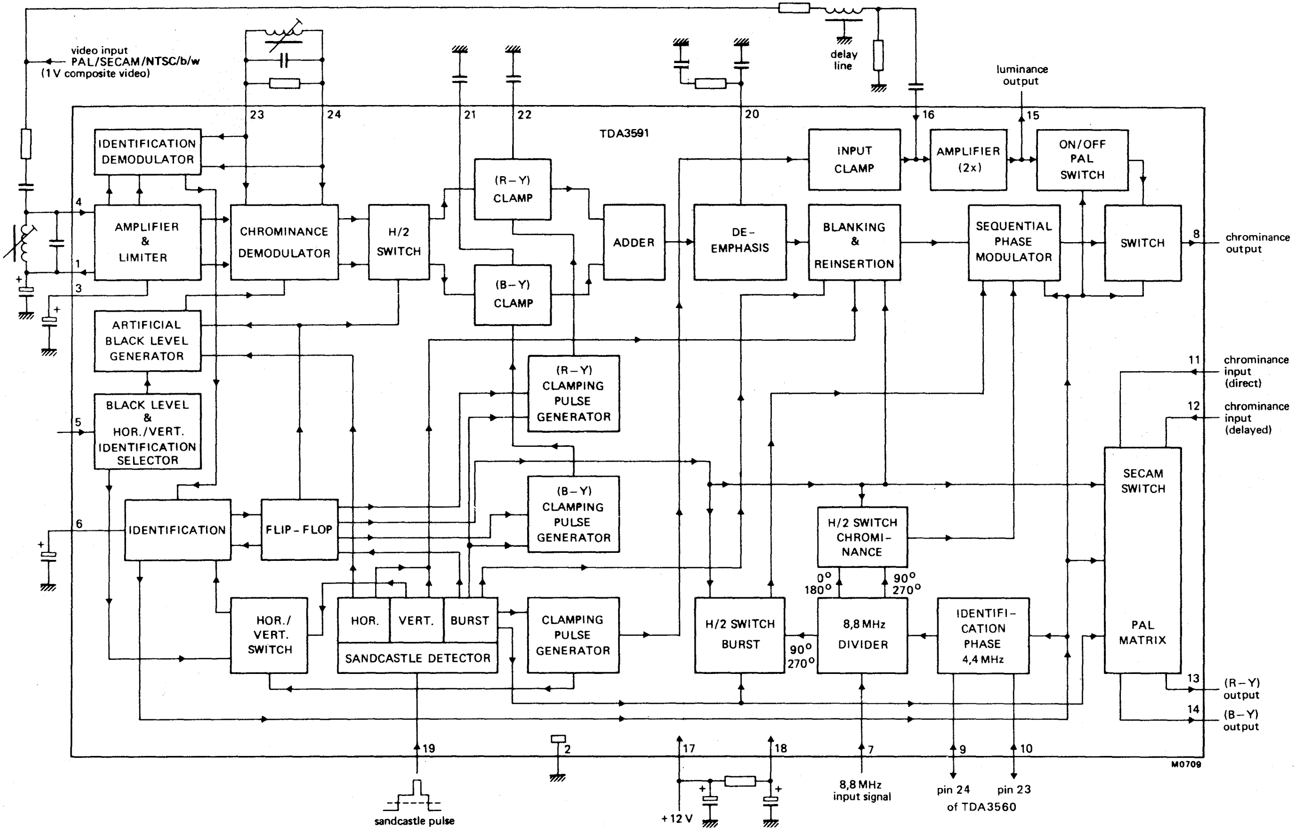


Fig.1 Block diagram

FUNCTIONAL DESCRIPTION

Demodulation

The TDA3591 comprises a chrominance and an identification demodulator, both using the same reference tuned circuit. The identification circuit automatically detects whether the incoming signal at pin 4 is SECAM or not (NTSC, PAL or black-and-white). When PAL signals are received, they are diverted via pin 16 to the chrominance output (pin 8).

The delay line connected to pin 16 delays the PAL luminance signal by 450 ns. The SECAM signal has the same delay in the processor circuitry. When the SECAM signals are received, the PAL signal path is switched off. Then, the SECAM signal is applied to a limiter/amplifier (via a bandpass filter with a bell-shaped response) after which it is demodulated. The (R—Y) and (B—Y) signals are applied sequentially, so only one demodulator is necessary. After demodulation the signals are applied to an H/2 switch, which separates the two colour difference signals. Now the signals are applied to the (R—Y) and (B—Y) clamp circuits, where the black levels are clamped to the same d.c. level. The (R—Y) and (B—Y) clamps are only active during the burst gate period.

If $V_{5\text{-}2} > 2$ V, artificial black levels are inserted during the horizontal blanking period. The clamp circuits then react upon these levels instead of the demodulated burst signals (necessary in case there are no horizontal burst signals available). The inserted signals may not be identical to the detected signals, because of circuitry spread. This can be corrected by detuning the demodulator tuned circuit.

Modulation

The (R—Y)/(B—Y) ratio is nominally 1,78 at the de-emphasis output (pin 20). The demodulated (R—Y) and (B—Y) signals have a positive phase position for a magenta colour.

A burst signal is added to the demodulated SECAM signal at the input of the modulator. A sequential modulated chrominance signal is present at the modulator output. The modulation carriers of the (R—Y) and (B—Y) signals are 90° out of phase. The burst is modulated in the + (R—Y) direction and is only present during an (R—Y) line. The modulated (R—Y) component for a magenta colour has the same phase position as the (R—Y) burst.

Identification

The identification circuit compares the voltage difference, which is obtained after demodulation, with the state of the flip-flop. For horizontal identification this comparison occurs during the internally generated 800 ns pulse. Only SECAM signals have a voltage difference from line to line during comparison. If the phase relationship between both the signals is wrong, the flip-flop will be reset by an extra input pulse.

The identification detector information is also used for colour killing and for switching to PAL, if required.

The identification (as above) occurs when the horizontal identification system is active. When the vertical identification system is switched on (pin 5), the system only compares the demodulator output voltage during line scanning of the vertical blanking. The further operation is identical to the horizontal identification.

Sandcastle pulse detector

The sandcastle pulse detector is able to handle a 3-level sandcastle pulse. It detects the various blanking and gating pulses and it generates the correct drive pulses for the clamping circuits.

FUNCTIONAL DESCRIPTION (continued)

Carrier generation

The carrier signal for the PAL modulator is obtained from the 8,8 MHz oscillator signal of the TDA3560. The frequency of this signal is divided-by-two to obtain 90° shift. These two signals are applied to the modulator. There is a possibility that the two dividers in the TDA3560 (pins 23 and 24) and the TDA3591 are out-of-phase. This can be corrected by connecting pins 9 and 10 of the TDA3591 to pins 24 and 23 of the TDA3560 respectively. At incorrect phase, the TDA3591 divider is reset and correct phase is obtained.

PAL-matrix and SECAM-switch

The colour difference signals are transmitted sequentially in the SECAM-system, so the modulated PAL-signal from the TDA3591 is also sequential. The consequences are:

- The two colour difference signals are mixed again in the delay line matrix circuit, so that both demodulators get a combination of an (R—Y) and (B—Y) signal. The phase position of the reference carrier must be very accurate for obtaining a proper demodulated signal, otherwise colour errors will occur (e.g. in the NTSC-system).
- Two different signals are added or subtracted in the matrix circuit, which results in an amplitude that has half the amplitude when compared with a normal PAL signal.

  Increase of the chrominance signal in the TDA3591 results in an overdrive of the chrominance amplifier of the TDA3560.

These effects are avoided by the matrix and switching circuit which is included in the TDA3591. The direct and delayed signals (from the PAL delay line) are applied to the processor where they are matrixed (for PAL) or switched (for SECAM). In the latter condition, the gain of the circuit is twice as high as for the normal PAL reception. The phase accuracy is not critical in this situation, because the two colour difference signals are not mixed.

For SECAM, the (B—Y) output of the SECAM-switch will be a signal without burst. The (R—Y) output of the SECAM-switch only has a burst during the +(R—Y) line. This burst is modulated in the +(R—Y) direction.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{17\text{-}2}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		−25 to +65	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 17)	V_P	10,8	12	13,2	V
Supply current (pin 17)	I_P	50	90	120	mA
Total power dissipation	P_{tot}	–	1,1	–	W
Thermal resistance from junction to ambient	$R_{th\ j\text{-}a}$	–	40	–	K/W
Chrominance amplifier and demodulator					
Input signal PAL (peak-to-peak value)	$V_{4\text{-}2(p\text{-}p)}$	55	550	1100	mV
Input signal SECAM (peak-to-peak value)	$V_{4\text{-}2(p\text{-}p)}$	15	–	300	mV
Input current	I_4	0,5	5	20	μA
Input capacitance	$C_{4\text{-}2}$	–	–	5	pF
(R–Y)/(B–Y) ratio before modulation (pin 20)		1,70	1,78	1,86	
Relative deviation of the black level of the colour difference signals before modulation (pin 20) (note 1)		–	5	–	%
Relative deviation of the black level of the colour difference signals before modulation without the application of a bell-shaped bandpass filter (note 2)		–	–	4	%
Output signal PAL (peak-to-peak value) (note 3)	$V_{8\text{-}2(p\text{-}p)}$	–	265	–	mV
Output signal SECAM (peak-to-peak value)	$V_{8\text{-}2(p\text{-}p)}$	–	1,3	–	V
Output impedance	$\lvert Z_{8\text{-}2}\rvert$	–	50	–	Ω
Input voltage for insertion of the artificial black level after demodulation	$V_{5\text{-}2}$	2	–	12	V
Input resistance between pins 23 and 24	$R_{23\text{-}24}$	3,0	4,0	5,0	kΩ
Input capacitance between pins 23 and 24	$C_{23\text{-}24}$	–	17	–	pF
Identification					
Input voltage for horizontal identification	$V_{5\text{-}2}$	0	–	8	V
Input voltage for vertical identification	$V_{5\text{-}2}$	10,5	–	12	V
Input current at pin 5 $V_{5\text{-}2}$ = 12 V	I_5	–	3	10	μA
Output current at pin 5 $V_{5\text{-}2}$ = 0 V (during horizontal blanking)	$-I_5$	–	0,1	5	μA

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Identification (continued)					
Voltage pin 6 for PAL	$V_{6\text{-}2}$	–	10,1	–	V
Voltage at pin 6 for SECAM	$V_{6\text{-}2}$	–	7,0	–	V
Identification 'on' for SECAM	$V_{6\text{-}2}$	–	10,6	–	V
Colour 'off' for SECAM	$V_{6\text{-}2}$	–	9,25	–	V
Colour 'on' for SECAM	$V_{6\text{-}2}$	–	9,1	–	V
Voltage at pin 9 for SECAM	$V_{9\text{-}2}$	10,3	10,5	–	V
Voltage between pins 9 and 10 for SECAM	$\pm V_{9\text{-}10}$	–	–	3	mV
Permissible voltage at pins 9 and 10 for PAL	$V_{9\text{-}2}; V_{10\text{-}2}$	8,2	–	10,2	V
Sandcastle pulse detector and clamping pulse generator					
Voltage level at which the vertical blanking pulse is separated	$V_{19\text{-}2}$	1	1,5	2	V
required pulse amplitude	$V_{19\text{-}2(p\text{-}p)}$	2	–	3	V
Voltage level at which the horizontal blanking pulse is separated	$V_{19\text{-}2}$	3	3,5	4	V
required pulse amplitude	$V_{19\text{-}2(p\text{-}p)}$	4	–	6,7	V
Voltage level at which the burst gating pulse is separated	$V_{19\text{-}2}$	6,7	7,2	7,7	V
required pulse amplitude	$V_{19\text{-}2(p\text{-}p)}$	7,7	–	12	V
Internal clamping pulse duration (note 4)	t_p	–	0,8	–	μs
Input current at $V_{19\text{-}2}$ = 7 V	I_2	–	10	40	μA
Carrier generator (note 5)					
Input signal from TDA3560 (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	150	–	–	mV
Input impedance	$\lvert Z_{7\text{-}2}\rvert$	–	1	–	kΩ
Input resistance	$R_{7\text{-}2}$	3,5	–	5,5	kΩ
Luminance amplifier					
Input signal (peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$	–	0,45	0,7	V
Luminance amplifier gain at 4,4 MHz		4	5	6	dB
Input current	I_{16}	–	0,15	1	μA
Output impedance (2 mA load current)	$\lvert Z_{15\text{-}2}\rvert$	–	20	–	Ω
Frequency response (–3 dB)	f	6	–	–	MHz

parameter	symbol	min.	typ.	max.	unit
PAL-matrix and SECAM-switch					
Burst signal amplitude at pins 11 and 12 (peak-to-peak value)	$V_{11,12(p\text{-}p)}$	–	60	–	mV
Input resistance at pins 11 and 12	$R_{11;12\text{-}12}$	1,5	2	2,5	kΩ
Amplification for PAL					
pin 13		−1,3	−0,3	+0,7	dB
pin 14		−1,5	−0,5	+0,5	dB
Amplification for SECAM (pins 13 and 14)		4,5	5,5	6,5	dB
Difference in amplification from the inputs to one output for PAL (note 6)	ΔG	–	–	0,5	dB
Phase error from line to line in the (R−Y) output for zero error in the (B−Y) output for PAL		–	2	3,5	deg
Output impedance at pins 13 and 14	$\|Z_{13;14-2}\|$	–	50	–	Ω

Notes to characteristics

1. A nominal value of 5% is obtained for clamping on the back porch of the colour difference signals. This value is related to the demodulated (B—Y) signal at Δf = 230 kHz. When an artificial black level is inserted after demodulation, the resulting black level deviation depends on the adjustment of the demodulator tuned circuit. It is therefore possible to obtain a value of zero percent.
2. This value is related to the demodulated (B—Y) signal at Δf = 230 kHz.
3. The luminance amplifier input voltage (peak-to-peak value) must be typically 0,45 V based on 75% saturated colour bar signals.
4. This pulse starts directly after the burst clamping pulse.
5. The phase delay between the oscillator output of the TDA3560 and the 8,8 MHz input of the TDA3591 (pin 7) must be adjusted so as to minimize the burst amplitude at pin 28 of the TDA3560.
6. $\Delta G = G_{11\text{-}13}/G_{12\text{-}13}$ and/or $G_{11\text{-}14}/G_{12\text{-}14}$.

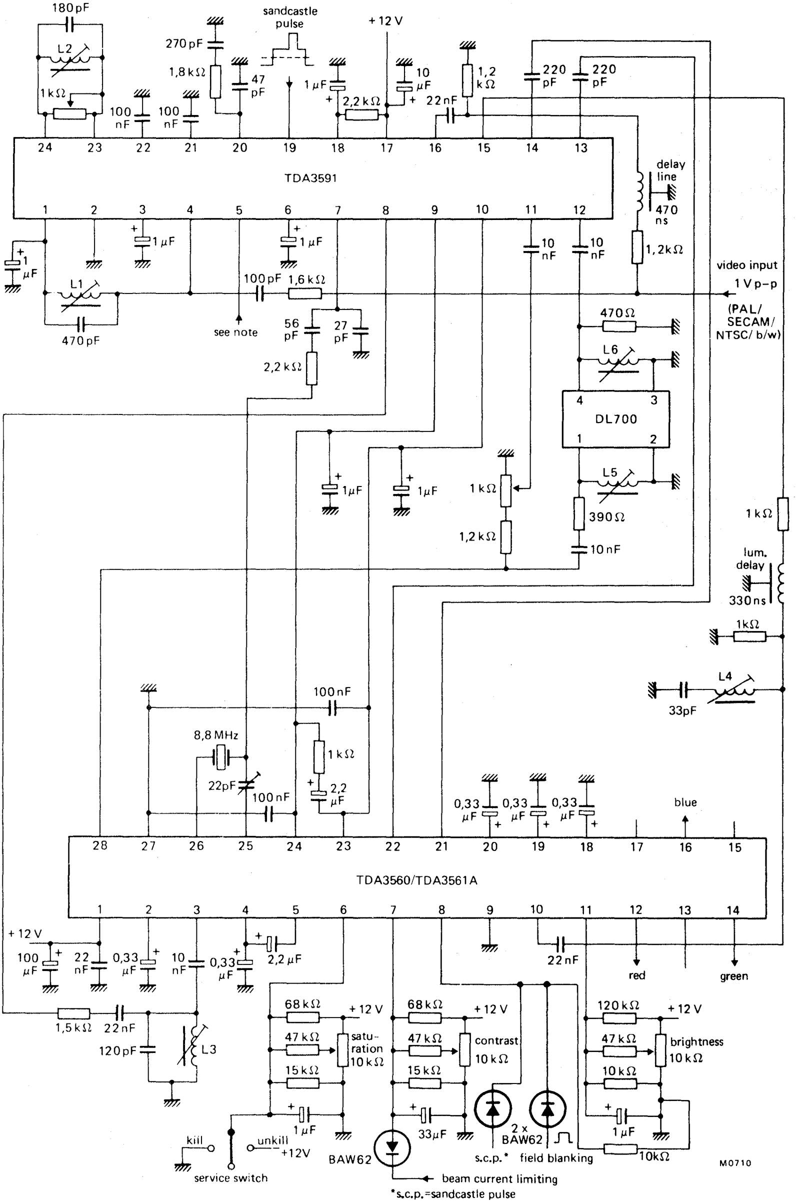


Fig.2 PAL/SECAM application circuit diagram using the TDA3591 and TDA3560; (for a combination with the TDA3562A see Fig.3). For note to pin 5 of the TDA3591 see next page.

Note to Fig. 2

$V_{5-2} < 0{,}5$ V : horizontal identification and black level clamping.
$V_{5-2} > 10{,}5$ V : vertical identification and artificial black level.
$V_{5-2} = 5$ to 7 V: horizontal identification and artificial black level.

PINNING

1. Limiter feedback to pin 4.
2. Ground.
3. Limiter feedback.
4. Input limiter; PAL identification input; SECAM chrominance/identification input.
5. Via a d.c. voltage to this pin, the SECAM identification system can be chosen.
   At $V_{5-2} < 8$ V the processor is preset for horizontal identification.
   At $V_{5-2} > 10{,}5$ V the processor is preset for vertical identification.
   At $V_{5-2} < 0{,}5$ V the demodulated black level of the SECAM horizontal burst will be used as black level reference.
   At $V_{5-2} > 2$ V the demodulated chroma signal will have an artificial black level during the SECAM horizontal burst.
6. Store capacitor of PAL/SECAM identification circuit;
   horizontal identification: 100 nF
   vertical identification: 1 μF
7. Input of 8,8 MHz oscillator signal.
8. PAL/processed SECAM signal output (chrominance output).
9. Identification input of 8,8 MHz divider (to pin 24 of TDA3560).
10. Identification input of 8,8 MHz divider (to pin 23 of TDA3560).
11. Direct chrominance input of PAL matrix/processed SECAM switch.
12. Delayed chrominance input of PAL matrix/processed SECAM switch.
13. PAL/processed SECAM (R–Y) h.f. output.
14. PAL/processed SECAM (B–Y) h.f. output.
15. Luminance output.
16. Luminance/PAL input.
17. Positive supply voltage (+ 12 V).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input. It detects the various blanking and gating pulses and it generates the correct drive pulses for the clamping circuits.
20. De-emphasis is performed at this pin with a 1,8 kΩ resistor and a 270 pF capacitor. To avoid moiré patterns on the screen, additional filtering of the demodulator double-frequency products is obtained by a 47 pF decoupling capacitor.
21. Store capacitor (B–Y) clamp.
22. Store capacitor (R–Y) clamp.
23. Demodulator reference tuned circuit.
24. Demodulator reference tuned circuit. The demodulator reference circuit has to be tuned to a nominal frequency of about 4,33 MHz. The quality factor of the tuned circuit must be nominal 2,45.

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION (see Fig. 2)

The function is described against the corresponding pin number

Pin 4. Chrominance input

The SECAM input signal is typically 100 mV peak to peak, while the PAL input signal is about 550 mV peak to peak. This corresponds to a PAL/SECAM ratio of 5,5 (based on 75% saturated colour bar signals). The input signal, which should be free from any sound modulation, is applied single-ended to pin 4 via a filter which provides the required bell-shaped bandpass for SECAM signals. D.C. biasing takes place via coil L1, which has an unloaded quality factor between 80 and 100.

Pin 8. Chrominance output

During PAL reception, this output is internally connected to the luminance stage, therefore a composite video signal of 0,9 V peak to peak (typical) is present at the output. During SECAM reception, the chrominance output stage is connected to the modulator. The sequentially modulated (R—Y) and (B—Y) signals are then available at the output (amplitudes of typically 1300 mV peak to peak). These signals are applied via a chrominance bandpass filter to the chrominance a.c.c. amplifier in the TDA3560.

Pin 6. System identification

A 1 μF capacitor is connected to this pin. During PAL reception, the typical voltage at pin 6 is 10,1 V. The chrominance output stage is then internally connected to the luminance stage and the PAL matrix circuit is activated for normal matrixing of the PAL signals. During SECAM reception, the voltage at pin 6 is about 7 V (typical). The chrominance output stage is connected to the modulator and the SECAM switch is enabled. During noisy SECAM signals, the voltage at pin 6 increases and colour killing/unkilling occurs around 9,25 V and 9,1 V respectively.

Pin 5. Horizontal/vertical identification

Horizontal or vertical identification can be selected depending on the externally applied voltage at pin 5. When the d.c. level on pin 5 changes with time (pulse information), a combination of horizontal and vertical identification is possible.

Horizontal identification

If the voltage at pin 5 is < 2 V, horizontal identification occurs with black level clamping. This clamping occurs on the back-porch of the demodulated colour difference signals. If artificial black level insertion is required, the voltage at pin 5 should be < 8 V.

Vertical identification

If the voltage at pin 5 is > 10,5 V, vertical identification occurs, i.e. identification on 9 lines in the vertical blanking period. In this mode, the black level is artificially inserted after demodulation.

Pin 19. Sandcastle pulse

A 3-level sandcastle pulse is required and this can be directly coupled to the sandcastle pulse detector. Horizontal blanking, vertical blanking and burst clamping pulses are separated by the IC. A clamping pulse of 800 ns is generated internally just after the burst gating pulse. The input current is typically 10 μA at an input signal of 7,2 V.

Pins 16 and 15. Luminance input/output

The input signal at pin 16 should be typically 0,5 V peak to peak. The input impedance is relatively high, so a 22 nF coupling capacitor can be applied. This luminance signal is internally clamped and after a 2 times amplification available at pin 15.

During SECAM reception, the luminance signal is delayed by about 470 ns in a luminance delay line. The chrominance and luminance signals are then correctly timed at the output of the TDA3591.

During PAL reception, the composite video signal passes through this delay line and, after amplification, is available at pins 8 and 15. The nominal amplitude of the signals is 900 mV peak to peak in both cases.

Pins 11, 12, 13 and 14. SECAM switch and PAL matrix

During PAL reception, the system identification 'enables' the PAL matrix circuitry. An a.c.c. composite chroma signal (from pin 28 TDA3560) is coupled via the glass delay line to pin 12 of the TDA3591. A direct signal is applied to pin 11 of the TDA3591 via a resistor network. Active matrixing takes place in the IC and consequently (R—Y) and (B—Y) signals are available at pins 13 and 14 respectively. These signals are applied to the TDA3560 demodulators (pins 22 and 21 respectively).

During SECAM reception, the PAL matrix circuitry is 'disabled' and the SECAM switch is 'enabled'. A sequentially modulated (R—Y) and (B—Y) signal is available at pin 28 of the TDA3560. Direct and delayed signals are applied to pins 11 and 12 of the TDA3591, and via the SECAM switch the (R—Y) and (B—Y) signals are applied to their respective demodulator in the TDA3560.

Pins 17 and 18. Supply voltage (+ 12 V)

Correct operation is ensured within the supply range of 10,8 V to 13,2 V, and the typical power dissipation of the IC is 1,1 W at 12 V.

Pins 17 and 18 are separated by an external RC filter. Pin 18 is the supply for biasing several current-sinks in the IC and for all the output stages.

This supply voltage separation minimizes crosstalk via the supply lines between various parts of the circuitry. The capacitor at pin 18 must be small ($\approx$ 1 μF) so that, if pin 17 is short-circuited to ground, the collector-base junction of a transistor in the IC, through which the discharge current flows, is not damaged.

Pin 20. De-emphasis

De-emphasis is performed at this pin with a 1,8 kΩ and a 270 pF capacitor. To avoid moiré patterns on the screen, additional filtering of the 8,8 MHz signal is obtained by a 47 pF decoupling capacitor.

Pins 21 and 22. Clamping of (R—Y) and (B—Y) signals

After demodulation, the sequential (R—Y) and (B—Y) signals are separated by means of an H/2 switch and passed-on to their respective clamping circuits, where they are clamped to the same d.c. level. The value of each clamping capacitor should be 100 nF and they may, if desired, be increased to 470 nF.

Pins 23 and 24. Demodulator reference tuned circuit

The SECAM signal is applied to the demodulator via the 'bell-filter' and limiter/amplifier. Only one demodulator is used because of the sequential nature of the signal. The reference signal, obtained from the tank circuit, is applied to pins 23 and 24. At $V_{5\text{-}2} > 2$ V, the tuning and damping of the tank circuit should be done in such a way that a minimum modulator output voltage at pin 8 of the TDA3591 is obtained (the (R—Y) and (B—Y) information in the SECAM video signal is switched off). Therefore, any deviations between the black levels (when clamping on the back-porch and when an artificial black level is filled in) can be made minimum.

APPLICATION INFORMATION (continued)

Pin 7. Carrier generation

An 8,8 MHz signal from pin 25 of the TDA3560 is applied via pin 7 to the divider circuit in the TDA3591. Two 4,4 MHz signals are obtained with a phase shift of 90° with respect to each other. These signals are applied to the modulator via an H/2 switch. The phase delay of the 8,8 MHz input signal must be adjusted such that the burst amplitude of the chrominance signal at pin 28 (TDA3560) has its minimum amplitude. Under this condition, the burst generated by the TDA3591 is in phase with the (R–Y) reference signal for the demodulator in the TDA3560. Since the a.c.c. of the TDA3560 operates in the + (R–Y) direction, the burst signal at pin 28 of the TDA3560 will have its minimum amplitude.

Pins 9 and 10. Divider resetting

The output of the burst phase detector of the TDA3560 is connected to pins 9 and 10. At SECAM reception, the differential a.c. current information, obtained from the burst detector (TDA3560), is applied to pins 9 and 10 (TDA3591). This gives information about the phase relationship between the two 4,4 MHz dividers in both ICs. The TDA3591 now generates a minimum relative voltage between pins 9 and 10 at an absolute voltage level of 10,6 V. The result is that the oscillator control function of the TDA3560 is overruled, and the oscillator is set to 2 x 4,43 MHz.

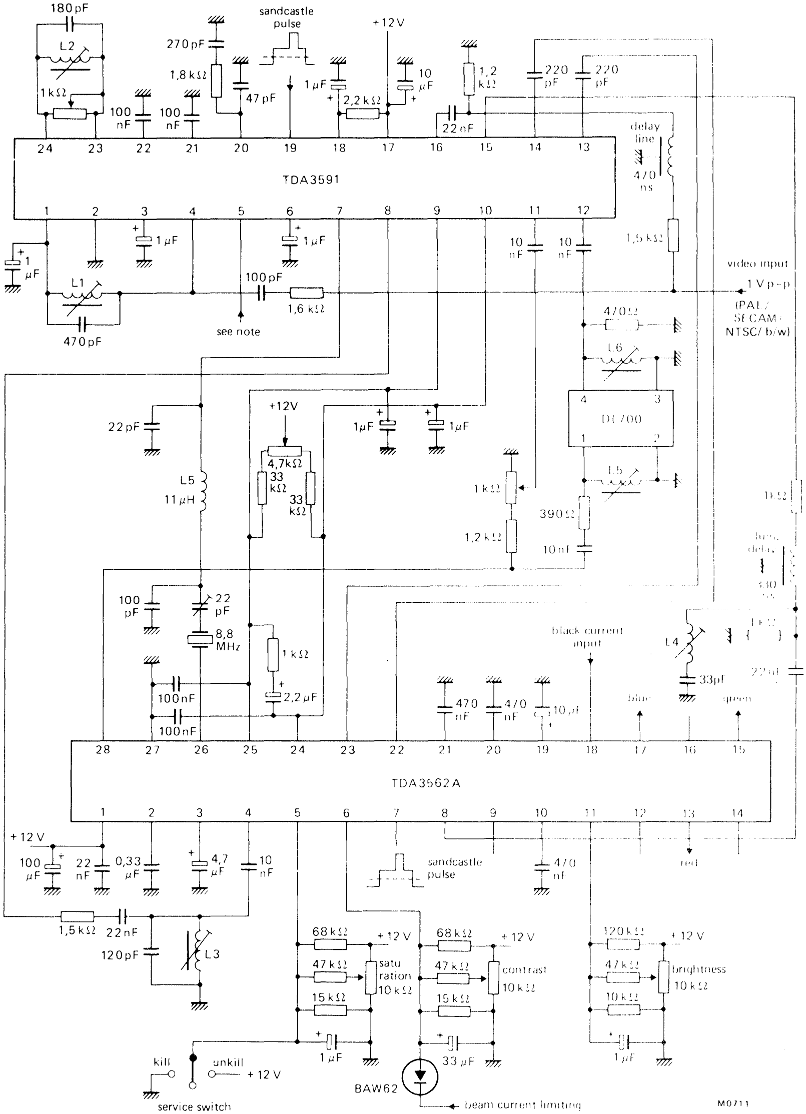


Fig.4 PAL/SECAM application circuit diagram using the TDA3591 and the TDA3562A.
Note to pin 5 TDA3591: $V_{5-2} < 2$ V; horizontal identification and black level clamping.
$V_{5-2} > 10,5$ V; vertical identification and artificial black level.
$2\ \mathrm{V} < V_{5-2} < 10,5$ horizontal identification and artificial black level.

VERTICAL DEFLECTION CIRCUIT

GENERAL DESCRIPTION

TDA3650 is a monolithic integrated circuit for vertical deflection in large screen colour television receivers.

The circuit incorporates the following functions:

- Oscillator
- Synchronization circuit
- Blanking pulse generator
- Sawtooth generator
- S-correction and linearity control
- Comparator and drive circuit
- Output stage
- Flyback generator
- Voltage stabilizer
- Thermal protection circuit
- Guard circuit
- Output stage protection

QUICK REFERENCE DATA

Supply voltage range (pin 13)	$V_{P1} = V_{13\text{-}12}$		0 to 30	V
Output current (peak-to-peak value)	$I_{3(p\text{-}p)}$	typ.	2,2	A
Operating junction temperature	T_j	max.	150	°C
Thermal resistance from junction to copper heat spreader (mounting base)	$R_{th\ j\text{-}mb}$	max.	4	K/W

PACKAGE OUTLINE

TDA3650: 13-lead SIL bent to DIL; plastic power (SOT-141B).

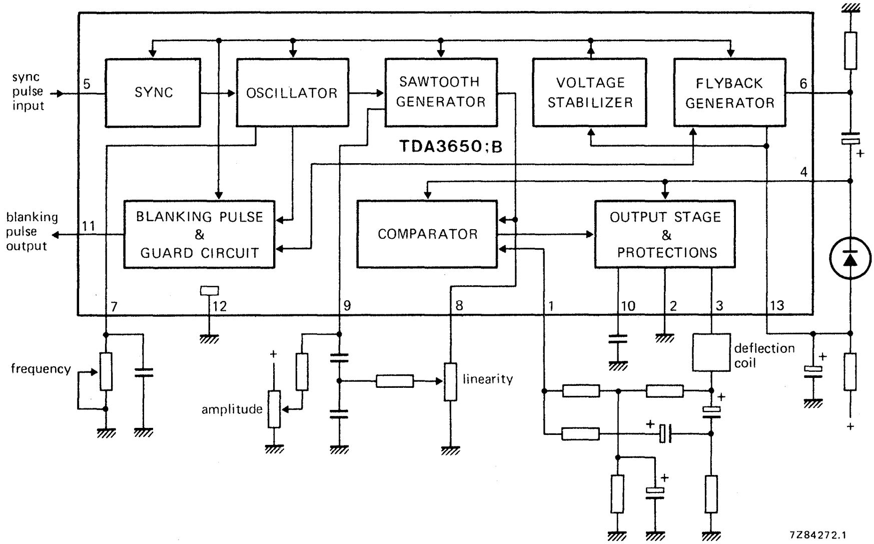


Fig. 1 Block diagram.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

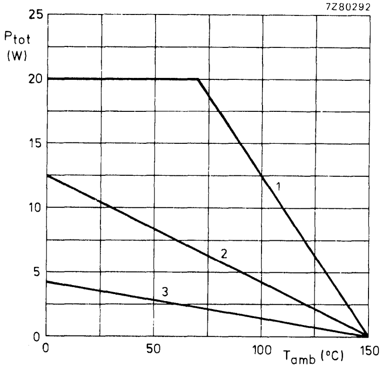
Pin 1; feedback voltage	$V_{1\text{-}12}$	max.	6	V
Pin 3; output voltage	$V_{3\text{-}12}$	max.	50	V
Pin 4; supply voltage output stage	$V_{4\text{-}12}$ (V_{P2})	max.	47	V
Pin 5; sync voltage	$V_{5\text{-}12}$	max.	6	V
Pin 11; blanking pulse	$V_{11\text{-}12}$	max.	6	V
Pin 13; supply voltage	$V_{13\text{-}12}$ (V_{P1})	max.	30	V

Currents

Pin 3; repetitive peak output current	$\pm I_{3RM}$	max.	2,8	A
Pin 3; non-repetitive peak output current	$\pm I_{3SM}$	max.	6	A
Pin 6; flyback generator	I_6	max.	2,8	A
Pin 11; blanking pulse	I_{11}	max.	10	mA

Total power dissipation internally limited by the thermal protection circuit (see also Fig. 2)

Storage temperature range	T_{stg}		−65 to + 150	°C
Operating junction temperature	T_j	max.	150	°C



(1) Mounted on infinite heatsink.
(2) Mounted on heatsink of 8 K/W.
(3) Without heatsink.

Fig. 2 Total power dissipation derating curves.

THERMAL RESISTANCE

From junction to mounting base $R_{th\,j\text{-}mb}$ = 4 K/W

CHARACTERISTICS

V_S = 26 V; pins 2 and 12 connected; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage range (note 1); V_{P1}	V_{13-2}	10	–	30	V
Supply voltage range output stage; V_{P2}	V_{4-2}	10	–	47	V
Supply current (without load)	I_{13}	–	55	–	mA
Output (pin 3)					
Output voltage (note 2)					
minimum	V_{3-2}	–	2,5	3,0	V
maximum	V_{3-2}	$V_{P2}-3$	$V_{P2}-2,5$	50	V
Output current (peak-to-peak value)	$I_{3(p-p)}$	–	2,2	2,8	A
Output current temperature dependency	$\Delta I_3/\Delta T$	–	–0,03	–	%/K
Sync (pin 5)					
Input voltage	V_{5-12}	1,0	–	6,0	V
Sync pulse width (note 4)	t_p	–	–	200	μs
Input impedance during oscillator scan	$\lvert Z_{5-12}\rvert$	1,8	2,2	2,6	kΩ
Oscillator (pin 7)					
Input current during scan	I_7	–	1,0	3,0	μA
Tracking range (note 5)		18	20	24	%
Frequency dependency					
with temperature	$\Delta f/\Delta T$	–	–	–0,02	Hz/K
with supply voltage	$\Delta f/\Delta V_{P1}$	–	–	–0,03	Hz/V
Tolerance of frequency adjustment range	$\Delta f_o/f_o$	–	–	± 3,5	%
Sawtooth generator (pin 9)					
Sawtooth voltage					
range	V_{9-12}	1,6	–	3,8	V
tolerance of minimum voltage level	V_{9-12}	1,45	1,6	1,7	V
Input resistance of pin 9					
during scan	R_{9-12}	0,5	–	–	MΩ
during oscillator flyback	R_{9-12}	500	650	800	Ω
Voltage offset between pins 8 and 9	V_{8-9}	–	40	100	mV
Blanking pulse generator (pin 11)					
Output voltage; I_{11} = 0	V_{11-12}	5,5	6,0	6,5	V
Blanking pulse width (note 3)	t_p	1,3	1,4	1,5	ms
Blanking pulse dependence with oscillator frequency (note 3)	$\Delta t_p/\Delta f$	–	–0,024	–	ms/Hz
Output impedance during blanking	$\lvert Z_{11-12}\rvert$	–	400	550	Ω
Blanking pulse output current	I_{11}	–	–	10	mA

parameter	symbol	min.	typ.	max.	unit
Comparator (pin 1)					
Input voltage	$V_{1\text{-}12}$	2,3	–	3,8	V
Input voltage temperature dependency	$\Delta V_{1\text{-}12}/\Delta T$	–	1,0	–	mV/K
Tolerance of d.c. level	$\Delta V_{1\text{-}12}$	–	–	± 150	mV
Open loop voltage gain (note 6) $V_{3\text{-}12}/V_{1\text{-}12}$ at 1000 Hz	G_o	–	64	–	dB
Frequency response (note 6) at –3 dB	f	–	10	–	kHz
Input current	I_1	–	–	5	μA
External load impedance of pin 8	$\lvert Z_{8\text{-}12}\rvert$	12	–	–	kΩ
Flyback generator (pin 6)					
Maximum output voltage (note 2)	$V_{6\text{-}2}$	$V_{P1}-5$	$V_{P1}-3$	–	V
Output current (peak-to-peak value)	$I_{6(p\text{-}p)}$	–	2,2	2,8	A
Thermal data					
Junction temperature thermal protection switching level	T_j	158	175	198	°C
Thermal resistance from junction to copper heat spreader (mounting base)	$R_{th\,j\text{-}mb}$	–	–	4	K/W

DEVELOPMENT SAMPLE DATA

Notes to characteristics

1. When the flyback generator is used, the maximum supply voltage must be chosen such that during flyback the voltage at pin 3 and pin 4 (supply voltage output stage) does not exceed 50 V.
2. These values (pin 3) are obtained at an output current of 2,8 A peak-to-peak (knee voltages of the output transistors). For an output current of 1 A peak-to-peak the maximum knee voltage is 2,5 V.

   The output voltage of the flyback generator is given at an output current of 2,8 A peak-to-peak (I_6). For an output current of 1 A peak-to-peak the output voltage at pin 3 will be V_{P1} – 2,5 V.
3. These values are obtained with the free running oscillator frequency adjusted to 45,5 kHz (22 ms) and an external 150 Ω resistor connected to pin 7 in series with the 150 nF capacitor. Without the 150 Ω resistor the width of the blanking pulse is 1,6 ± 0,1 ms.
4. The width of the synchronization pulse must be smaller than the oscillator flyback.
5. These values are obtained with the free running oscillator frequency adjusted to 45,5 kHz (22 ms).
6. These values are obtained with a load resistance of 1 kΩ between pin 3 and ground, and a 4,7 nF decoupling capacitor connected between pin 10 and ground.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. Comparator and drive circuit

The current flowing through the deflection coils is measured across an external series resistor. The signal across this resistor is fed to the comparator via pin 1, where it is compared with the internally generated sawtooth signal. The output of the comparator drives the output stage. Pin 1 is also used for d.c. feedback of the output stage (mid-point setting).

2. Negative supply (ground) for the output stage

3. Output stage

The output stage provides the current to the deflection coils. The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor to ground. The output stage is protected against over-voltages and over-currents by a SOAR-protection circuit. When one of the transistors exceeds its operational threshold the drive current is reduced to a safe level. Temperature protection reduces the drive of the output stage when the junction temperature exceeds 170 °C.

4. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 4 and 6, a diode between pins 4 and 13, and a resistor between pins 6 and ground must be connected for correct operation of the flyback generator.

5. Synchronization input

When the voltage applied to pin 5 reaches a level of 0,7 V the lower switching level is increased thus initiating the charge cycle of the oscillator capacitor. The synchronization circuit is inhibited during oscillator flyback time.

6. Flyback generator

The flyback generator reduces power dissipation in the vertical stage. As a result a lower power supply can be chosen (26 V for 30AX application). Whereas the voltage during flyback is increased to 45 V (depending on the design of external components), the maximum increase of the voltage during flyback is nearly factor 2.

The capacitor between pins 6 and 4 is charged via the external diode during the scan period. Then, when the flyback generator is activated by the oscillator flyback pulse, the voltage across the capacitor is connected in series with the supply voltage to provide the required flyback voltage. At the end of the oscillator pulse the drive of the flyback generator is maintained by the flyback voltage of the deflection circuit.

7. Oscillator

The oscillator frequency is determined by the values of the external resistor and capacitor connected in parallel to pin 7. The capacitor is discharged via the resistor which is connected to ground. The voltage on the capacitor is compared with an internal voltage from the voltage stabilizer (lower switching level). When this lower switching level is reached the capacitor is charged via an internal 500 Ω resistor. At the same time the comparator voltage is increased (higher switching level). When the voltage on the capacitor reaches the higher switching level the charge current is switched off and the capacitor is discharged again.

DEVELOPMENT SAMPLE DATA

8. S-correction and linearity circuit

From pin 8 an adjustable parabolic current is fed back to the mid-point of the sawtooth generator capacitors at pin 9 to provide linearity control. The external components connected between pins 8 and 9 together with the d.c. feedback circuitry at pin 1 define the S-shape of the deflection current.

9. Sawtooth generator

The sawtooth signal is obtained by charging the capacitors connected to pin 9 via an external resistor. Variation of the charge current will vary the amplitude of the signal. During oscillator flyback time the capacitors are discharged to an internally fixed voltage level.

10. Output stage decoupling

A low value capacitor must be connected to pin 10 for decoupling of the output driver stage.

11. Blanking pulse generator

The blanking pulse duration is determined by the oscillator sawtooth signal. The guard circuit provides continuous blanking when the vertical deflection current is absent.

12. Negative supply (ground) of small-signal part

13. Positive supply

The supply voltage at this pin is used to supply the flyback generator, the voltage stabilizer and the protection circuits.

The following application data are measured in a typical 30AX system (Fig. 3).

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage*	$V_{13\text{-}12}$	22	26	30	V
Supply current*	I_{13}	260	320	380	mA
Output (pin 3)					
Output voltage (peak value)	$V_{3\text{-}2}$	–	–	50	V
Output voltage (mid-point)	$V_{3\text{-}2}$	–	13	–	V
Output current (peak-to-peak value)**	$I_{3(p\text{-}p)}$	1,6	2,1	2,4	A
Flyback time▲	t_{f1}	–	0,7	0,9	ms
Total power dissipation in IC▲	P_{tot}	–	4,6	5,0	W
Total power consumption	P	5,2	8,5	11,5	W
Blanking time	t_p	–	1,45	–	ms
Non-linearity		–	–	3	%
Thermal resistance of heatsink	$R_{th\ h\text{-}a}$	–	8	–	K/W
Ambient temperature	T_{amb}	–	–	65	°C

* These values are obtained with a supply voltage (V_S) of 26 V and an output current of 2,1 A peak-to-peak. When the supply voltage is decreased to 22 V the output current changes to 1,6 A peak-to-peak and the supply current to 260 mA. When the supply voltage is increased to 30 V the output current increases to 2,4 A peak-to-peak and the supply current to 380 mA. But when the circuit is adjusted for an output current of 2,1 A peak-to-peak at a supply voltage of 30 V, the supply current remains at 320 mA (see note 1 to characteristics).

** Including 6% overscan.

▲ With the supply voltage V_S = 26 V.

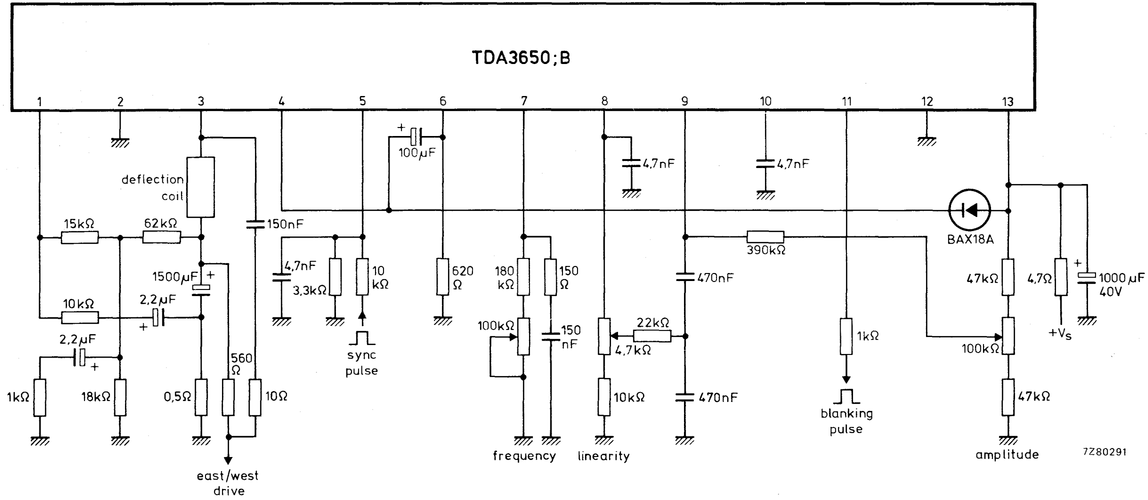


Fig. 3 Complete vertical deflection circuit for 30AX.

VERTICAL DEFLECTION CIRCUIT

The TDA3651 is a vertical deflection output circuit for drive of various deflection systems with deflection currents up to 2 A peak-to-peak.

The circuit incorporation the following functions:

- Driver
- Output stage
- Thermal protection and output stage protection
- Flyback generator
- Voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_{9\text{-}4} = V_P$		0 to 50	V
Peak output voltage during flyback (pin 5)	$V_{5\text{-}4M}$	$<$	55	V
Output current (peak-to-peak value)	$I_{5(p\text{-}p)}$	$<$	1,5	A
Operating junction temperature	T_j	max.	150	°C
Thermal resistance from junction to tab	$R_{th\ j\text{-}tab}$	typ.	10	K/W

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

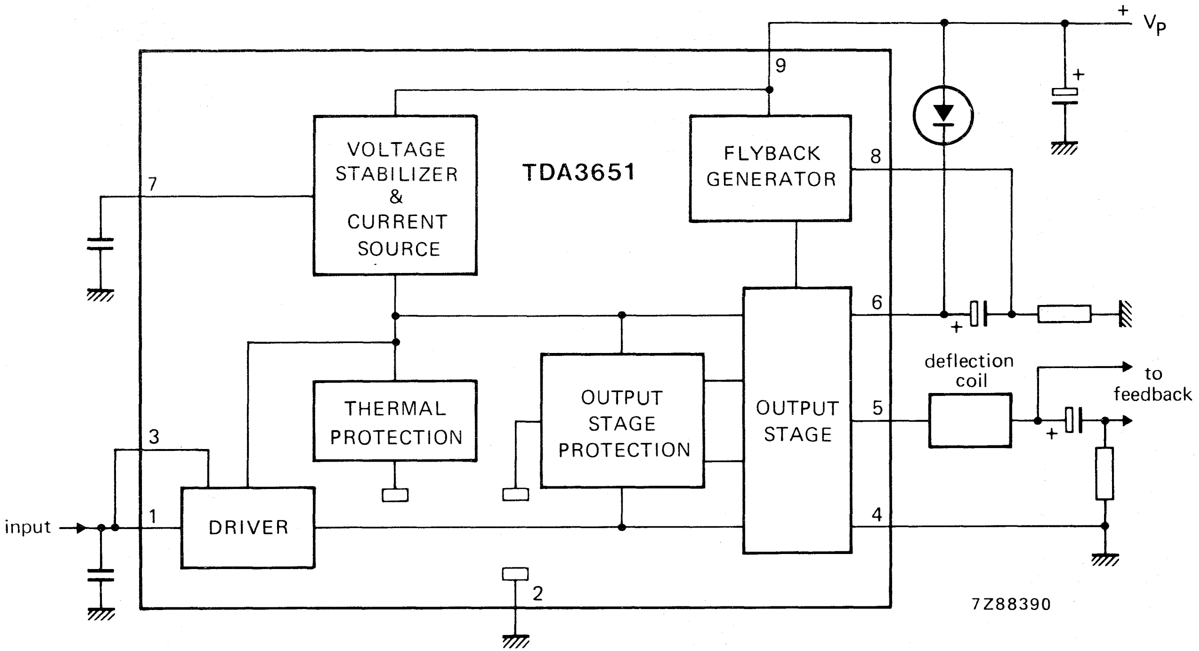


Fig. 1 Block diagram.

GENERAL DESCRIPTION

Output stage and protection circuit

Pin 5 is the output pin. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4. The output transistors of the class-B output stage can each deliver 1 A maximum. The 'upper' power transistor is protected against short-circuit currents to ground, whereas, during flyback, the 'lower' power transistor is protected against too high voltages which may occur during adjustments.
Moreover, the output transistors have been given extra solidity by means of special measures in the internal circuit layout.
A thermal protection circuit is incorporated to protect the IC against too high dissipation. This circuit is 'active' at 175 °C and then reduces the deflection current to such a value that the dissipation cannot increase.

Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied to pin 3 which is the input of a switching circuit. When the flyback starts, this switching circuit rapidly turns off the lower output stage and so limits the turn-off dissipation. It also allows a quick start of the flyback generator.
Pin 3 is connected externally to pin 1, in order to allow for different applications in which pin 3 is driven separately from pin 1.

Flyback generator

The capacitor at pin 6 is charged to a maximum voltage, which is equal to the supply voltage V_P (pin 9), during scan.
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage (pin 9), the flyback generator is activated. Then V_P is connected in series (via pin 8) with the voltage across the capacitor.
The voltage at the supply pin (pin 6) of the output stage will then be maximum twice V_P. Lower voltages can be chosen by changing the value of the external resistor at pin 8.

Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V for drive of the output stage, so the drive current of the output stage is not affected by supply voltage variations. The stabilized voltage is available at pin 7.
A decoupling capacitor of 2,2 μF can be connected to this pin.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages (pins 4 and 2 externally connected to ground)

Output voltage (pin 5)	$V_{5\text{-}4}$	max.	55 V
Supply voltage (pin 9)	$V_{9\text{-}4} = V_P$	max.	50 V
Supply voltage output stage (pin 6)	$V_{6\text{-}4}$	max.	55 V
Input voltage (pins 1 and 3)	$V_{1\text{-}2}; V_{3\text{-}2}$	max.	V_P

Currents

Repetitive peak output current (pin 5)	$\pm I_{5RM}$	max.	0,75 A
Non-repetitive peak output current (pin 5)	$\pm I_{5SM}$	max.	1,5 A*
Repetitive peak flyback generator output current (pin 8)	I_{8RM}	max.	−0,75 A +0,85 A
Non-repetitive peak flyback generator output current (pin 8)	I_{8SM}	max.	−1,5 A +1,6 A*

Temperatures

Storage temperature range	T_{stg}	−65 to + 150 °C
Operating ambient temperature range	T_{amb}	−25 to + 65 °C
Operating junction temperature range	T_j	−25 to + 150 °C

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 26 V; pins 4 and 2 externally connected to ground; unless otherwise specified.

Output current (peak-to-peak value)	$I_{5(p\text{-}p)}$	typ. <	1,2 A 1,5 A
Flyback generator output current	$-I_8$	typ. <	0,7 A 0,85 A
Flyback generator output current	I_8	typ. <	0,6 A 0,75 A

Output voltages

Peak voltage during flyback	$V_{5\text{-}4M}$	<	55 V
Saturation voltage to supply at $-I_5 = 1$ A	$-V_{5\text{-}6sat}$	typ. <	2,5 V 3,0 V
Saturation voltage to ground at $I_5 = 1$ A	$V_{5\text{-}4sat}$	typ. <	2,5 V 3,0 V
Saturation voltage to supply at $-I_5 = 0,75$ A	$-V_{5\text{-}6sat}$	typ. <	2,2 V 2,7 V
Saturation voltage to ground at $I_5 = 0,75$ A	$V_{5\text{-}4sat}$	typ. <	2,2 V 2,7 V

---

* Non-repetitive duty factor maximum 3,3%.

Supply				
Supply voltage	$V_{9\text{-}2;\,4}$		10 to 50	V*
Supply voltage output stage	$V_{6\text{-}4}$	<	55	V*
Supply current (no load and no quiescent current)	I_9	typ.	9	mA
		<	12	mA
Quiescent current (see Fig. 2)	I_4	typ.	38	mA
			25 to 52	mA
Variation of quiescent current with temperature		typ.	−0,04	mA/K
Flyback generator				
Saturation voltage at $-I_8 = 1{,}1$ A	$V_{9\text{-}8sat}$	typ.	1,6	V
		<	2,1	V
Saturation voltage at $I_8 = 1$ A	$V_{8\text{-}9sat}$	typ.	2,5	V
		<	3,0	V
Saturation voltage at $I_8 = 0{,}85$ A	$V_{9\text{-}8sat}$	typ.	1,4	V
		<	1,9	V
Saturation voltage at $I_8 = 0{,}75$ A	$V_{8\text{-}9sat}$	typ.	2,3	V
		<	2,8	V
Flyback generator active if:	$V_{5\text{-}9}$	>	4	V
Leakage current	$-I_8$	typ.	5	µA
		<	100	µA
Input current for $\pm I_5 = 1$ A	I_1	typ.	230	µA
			175 to 380	µA
Input voltage during scan	$V_{1\text{-}2}$	typ.	1,9	V
			0,9 to 2,7	V
Input current during scan	I_3		0,01 to 2,5	mA
Input voltage during scan	$V_{3\text{-}2}$		0,9 to V_P	V
Input voltage during flyback	$V_{3\text{-}2}$		0 to 0,2	V
Voltage at pin 7	$V_{7\text{-}2}$	typ.	6,1	V
			5,6 to 6,6	V
Load current of pin 7	I_7	<	2	mA
Unloaded voltage at pin 7 during flyback	$V_{7\text{-}2}$	typ.	15	V
Junction temperature of switching on the thermal protection	T_j	typ.	175	°C
			158 to 192	°C
Thermal resistance from junction to tab	$R_{th\,j\text{-}tab}$	typ.	10	K/W
		<	12	K/W
Power dissipation	see Fig. 3			
Open loop gain at 1 kHz; $R_{load} = 1$ kΩ	G_o	typ.	36	dB
Frequency response (−3 dB); $R_{load} = 1$ kΩ	f	typ.	60	kHz

---

* The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 55 V.

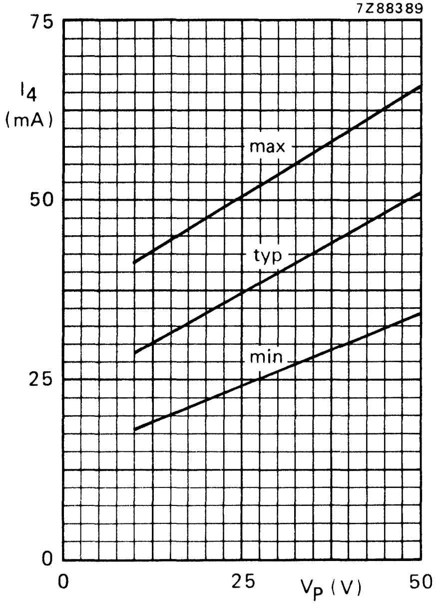


Fig. 2 Quiescent current I_4 as a function of supply voltage V_P.

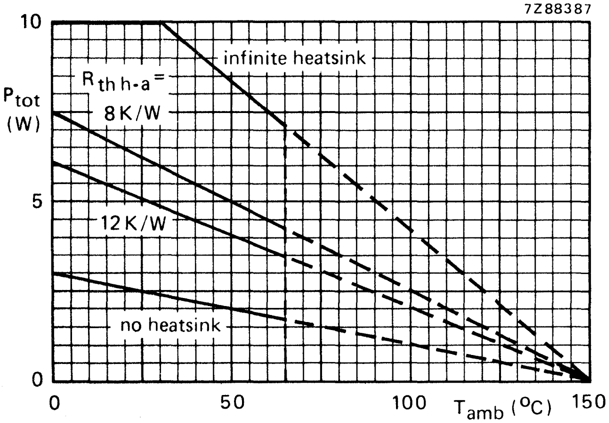


Fig. 3 Power derating curves.

APPLICATION INFORMATION

The following application data are measured in a typical application as shown in Figs 4 and 5.

Deflection current (including 6% overscan) peak-to-peak value	$I_{5(p-p)}$	typ.	0,87	A
Supply voltage	V_{9-4}	typ.	26	V
Total supply current	I_{tot}	typ.	148	mA
Peak output voltage during flyback	V_{5-4M}	<	50	V
Saturation voltage to supply	V_{5-6sat}	typ.	2,0	V
		<	2,5	V
Saturation voltage to ground	V_{5-4sat}	typ.	2,0	V
		<	2,5	V
Flyback time	t_{fl}	typ.	0,95	ms
		<	1,2	ms
Total power dissipation in IC	P_{tot}	typ.	2,5	W
Operating ambient temperature	T_{amb}	<	65	°C

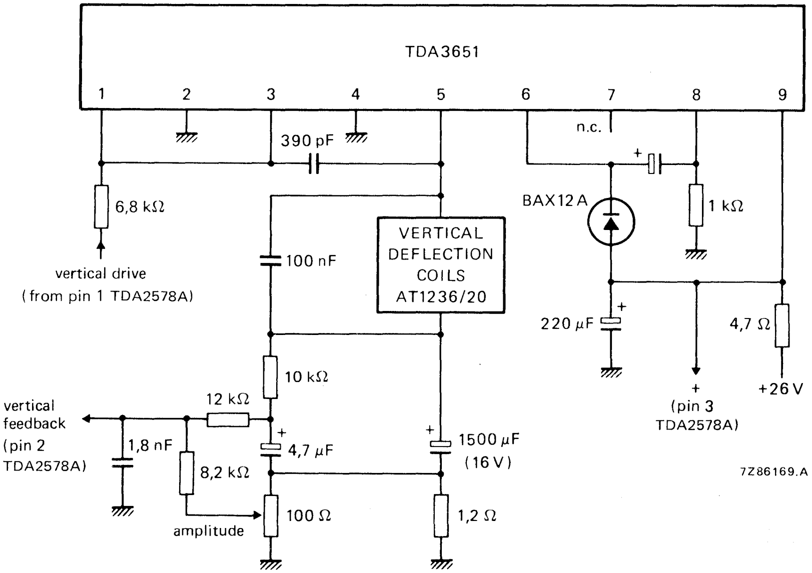


Fig. 4 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2578A (see Fig. 5).

Note to deflection coils AT1236/20: L = 29 mH, R = 13,6 Ω; deflection current without overscan is 0,82 A peak-to-peak and EHT voltage is 25 kV.

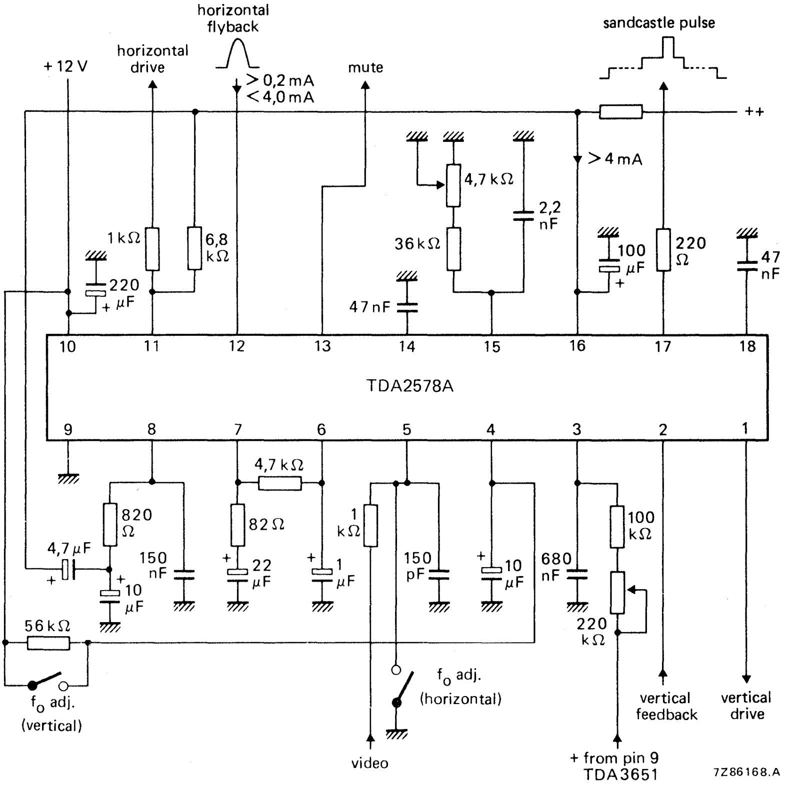


Fig. 5 Typical application circuit diagram; for combination of the TDA2578A with the TDA3651 see Fig. 4.

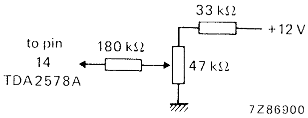


Fig. 6 Circuit configuration at pin 14 for phase adjustment.

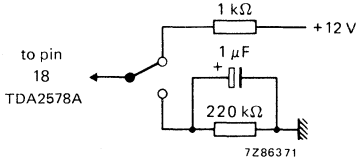


Fig. 7 Circuit configuration at pin 18 for VCR mode.
1 kΩ resistor between pin 18 and + 12 V: without mute function.
220 kΩ between pin 18 and ground: with mute function.

VERTICAL DEFLECTION CIRCUIT

The TDA3651A;AQ is a vertical deflection output circuit for drive of various deflection systems with deflection currents up to 2 A peak-to-peak.

The circuit incorporates the following functions:

- Driver
- Output stage
- Thermal protection and output stage protection
- Flyback generator
- Voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_{9-4} = V_P$		0 to 50	V
Peak output voltage during flyback (pin 5)	V_{5-4M}	<	55	V
Output current (peak-to-peak value)	$I_{5(p-p)}$	<	1,5	A
Operating junction temperature	T_j	max.	150	°C
Thermal resistance from junction to mounting base	$R_{th\ j-mb}$	typ.	3	K/W

PACKAGE OUTLINES

TDA3651A: 9-lead SIL; plastic power (SOT-131B).

TDA3651AQ: 9-lead SIL bent to DIL; plastic power (SOT-157B).

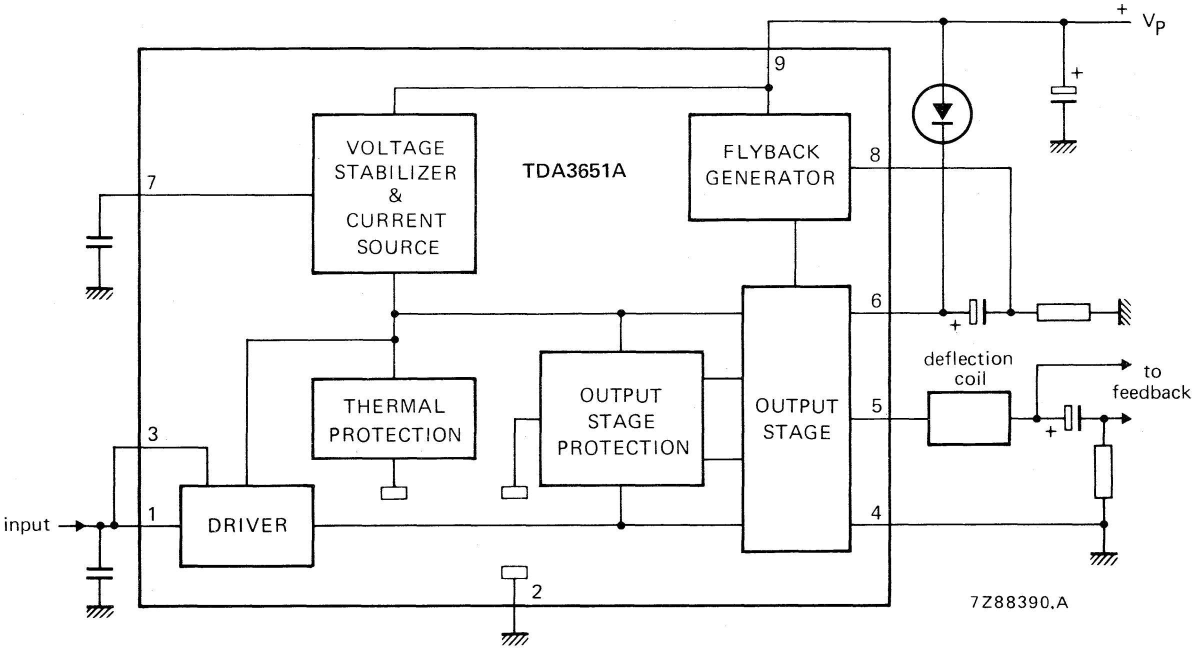


Fig. 1 Block diagram.

GENERAL DESCRIPTION

Output stage and protection circuit

Pin 5 is the output pin. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4. The output transistors of the class-B output stage can each deliver 1 A maximum. The 'upper' power transistor is protected against short-circuit currents to ground, whereas, during flyback, the 'lower' power transistor is protected against too high voltages which may occur during adjustments.
Moreover, the output transistors have been given extra solidity by means of special measures in the internal circuit layout.
A thermal protection circuit is incorporated to protect the IC against too high dissipation. This circuit is 'active' at 175 °C and then reduces the deflection current to such a value that the dissipation cannot increase.

Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied to pin 3 which is the input of a switching circuit. When the flyback starts, this switching circuit rapidly turns off the lower output stage and so limits the turn-off dissipation. It also allows a quick start of the flyback generator. Pin 3 is connected externally to pin 1, in order to allow for different applications in which pin 3 is driven separate from pin 1.

Flyback generator

The capacitor at pin 6 is charged to a maximum voltage, which is equal to the supply voltage V_P (pin 9), during scan.
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage (pin 9), the flyback generator is activated. The V_P is connected in series (via pin 8) with the voltage across the capacitor.
The voltage at the supply pin (pin 6) of the output stage will then be maximum twice V_P. Lower voltages can be chosen by changing the value of the external resistor at pin 8.

Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V for drive of the output stage, so the drive current of the output stage is not affected by supply voltage variations. The stabilized voltage is available at pin 7.
A decoupling capacitor of 2,2 μF can be connected to this pin.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages (pins 4 and 2 externally connected to ground)

Output voltage (pin 5)	$V_{5\text{-}4}$	max.	55	V
Supply voltage (pin 9)	$V_{9\text{-}4} = V_P$	max.	50	V
Supply voltage output stage (pin 6)	$V_{6\text{-}4}$	max.	55	V
Input voltage (pins 1 and 3)	$V_{1\text{-}2}; V_{3\text{-}2}$	max.	V_P	

Currents

Repetitive peak output current (pin 5)	$\pm I_{5RM}$	max.	0,75	A
Non-repetitive peak output current (pin 5)	$\pm I_{5SM}$	max.	1,5	A*
Repetitive peak flyback generator output current (pin 8)	I_{8RM}	max.	−0,75 +0,85	A A
Non-repetitive peak flyback generator output current (pin 8)	I_{8SM}	max.	−1,5 +1,6	A A*

Temperatures

Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	−25 to + 65	°C
Operating junction temperature range	T_j	−25 to + 150	°C

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 26 V; pins 4 and 2 externally connected to ground; unless otherwise specified.

Output current (peak-to-peak value)	$I_{5(p\text{-}p)}$	typ. <	1,2 1,5	A A
Flyback generator output current	$-I_8$	typ. <	0,7 0,85	A A
Flyback generator output current	I_8	typ. <	0,6 0,75	A A

Output voltages

Peak voltage during flyback	$V_{5\text{-}4M}$	<	55	V
Saturation voltage to supply at $-I_5$ = 1 A	$-V_{5\text{-}6sat}$	typ. <	2,5 3,0	V V
Saturation voltage to ground at I_5 = 1 A	$V_{5\text{-}4sat}$	typ. <	2,5 3,0	V V
Saturation voltage to supply at $-I_5$ = 0,75 A	$-V_{5\text{-}6sat}$	typ. <	2,2 2,7	V V
Saturation voltage to ground at I_5 = 0,75 A	$V_{5\text{-}4sat}$	typ. <	2,2 2,7	V V

---

* Non-repetitive duty factor maximum 3,3%.

Supply				
Supply voltage	$V_{9\text{-}2;\,4}$		10 to 50	V*
Supply voltage output stage	$V_{6\text{-}4}$	<	55	V*
Supply current (no load and no quiescent current)	I_9	typ. <	9 12	mA mA
Quiescent current (see Fig. 2)	I_4	typ.	38 25 to 52	mA mA
Variation of quiescent current with temperature		typ.	–0,04	mA/K
Flyback generator				
Saturation voltage at $-I_8 = 1{,}1$ A	$V_{9\text{-}8sat}$	typ. <	1,6 2,1	V V
Saturation voltage at $I_8 = 1$ A	$V_{8\text{-}9sat}$	typ. <	2,5 3,0	V V
Saturation voltage at $I_8 = 0{,}85$ A	$V_{9\text{-}8sat}$	typ. <	1,4 1,9	V V
Saturation voltage at $I_8 = 0{,}75$ A	$V_{8\text{-}9sat}$	typ. <	2,3 2,8	V V
Flyback generator active if:	$V_{5\text{-}9}$	>	4	V
Leakage current	$-I_8$	typ. <	5 100	μA μA
Input current for $\pm I_5 = 1$ A	I_1	typ.	230 175 to 380	μA μA
Input voltage during scan	$V_{1\text{-}2}$	typ.	1,9 0,9 to 2,7	V V
Input current during scan	I_3		0,01 to 2,5	mA
Input voltage during scan	$V_{3\text{-}2}$		0,9 to V_P	V
Input voltage during flyback	$V_{3\text{-}2}$		0 to 0,2	V
Voltage at pin 7	$V_{7\text{-}2}$	typ.	6,1 5,6 to 6,6	V V
Load current of pin 7	I_7	<	2	mA
Unloaded voltage at pin 7 during flyback	$V_{7\text{-}2}$	typ.	15	V
Junction temperature of switching on the thermal protection	T_j	typ.	175 158 to 192	^oC ^oC
Thermal resistance from junction to mounting base	$R_{th\ j\text{-}mb}$	typ. <	3 4	K/W K/W
Power dissipation	see Fig. 3			
Open loop gain at 1 kHz; $R_{load} = 1$ kΩ	G_o	typ.	36	dB
Frequency response (–3 dB); $R_{load} = 1$ kΩ	f	typ.	60	kHz

---

* The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 55 V.

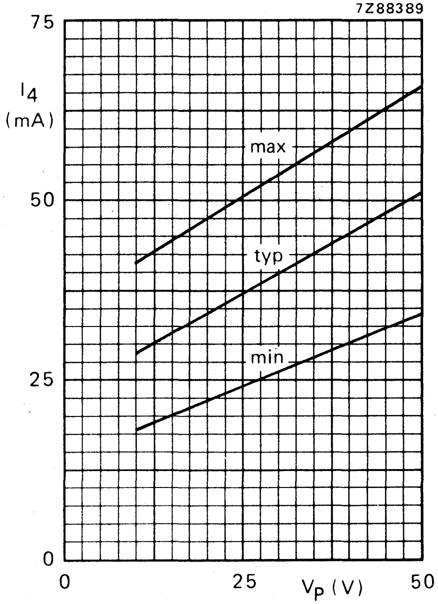


Fig. 2 Quiescent current I_4 as a function of supply voltage V_P.

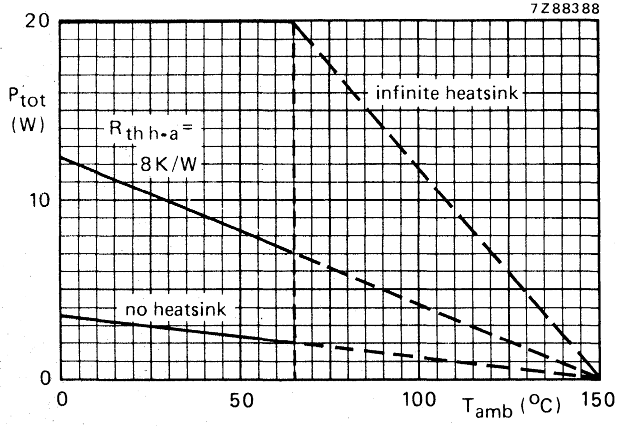


Fig. 3 Power derating curves.

APPLICATION INFORMATION

The following application data are measured in a typical application as shown in Figs 4 and 5.

Deflection current (including 6% overscan) peak-to-peak value	$I_{5(p-p)}$	typ.	0,87	A
Supply voltage	V_{9-4}	typ.	26	V
Total supply current	I_{tot}	typ.	148	mA
Peak output voltage during flyback	V_{5-4M}	<	50	V
Saturation voltage to supply	V_{5-6sat}	typ.	2,0	V
		<	2,5	V
Saturation voltage to ground	V_{5-4sat}	typ.	2,0	V
		<	2,5	V
Flyback time	t_{fl}	typ.	0,95	ms
		<	1,2	ms
Total power dissipation in IC	P_{tot}	typ.	2,5	W
Operating ambient temperature	T_{amb}	<	65	°C

DEVELOPMENT SAMPLE DATA

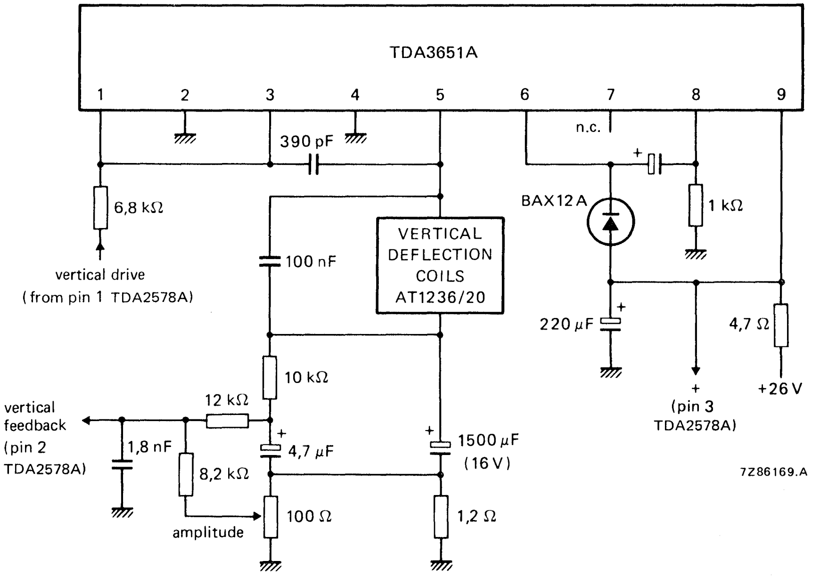


Fig. 4 Typical application circuit diagram of the TDA3651A (vertical output), when used in combination with the TDA2578A (see Fig. 5).

Note to deflection coils AT1236/20: L = 29 mH, R = 13,6 Ω; deflection current without overscan is 0,82 A peak-to-peak and EHT voltage is 25 kV.

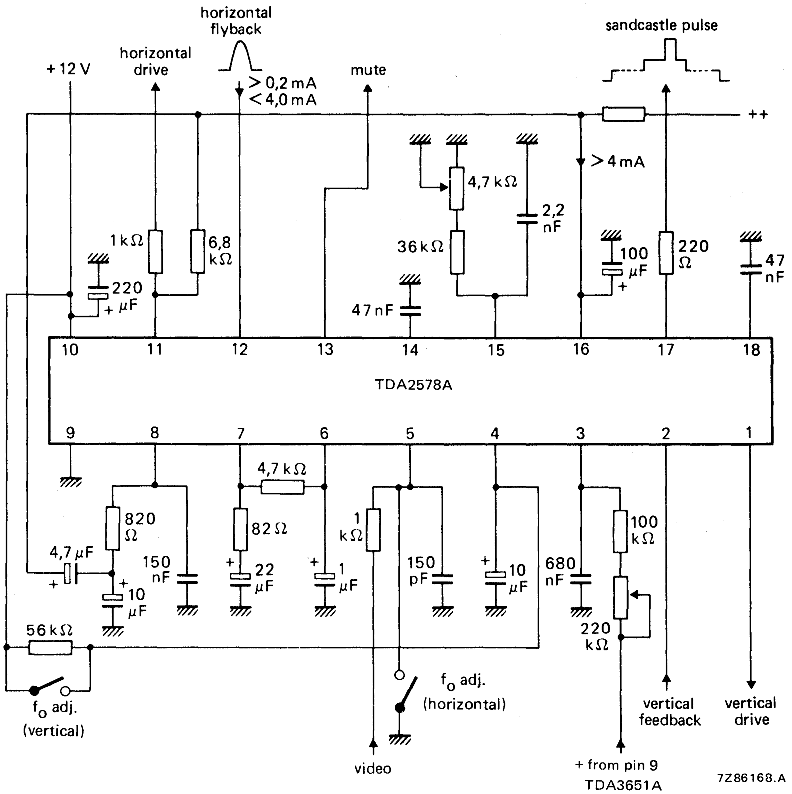


Fig. 5 Typical application circuit diagram; for combination of the TDA2578A with the TDA3651A see Fig. 4.

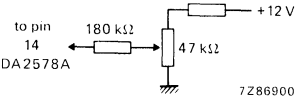


Fig. 6 Circuit configuration at pin 14 for phase adjustment.

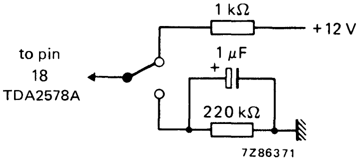


Fig. 7 Circuit configuration at pin 18 for VCR mode.
1 kΩ resistor between pin 18 and + 12 V: without mute function.
220 kΩ between pin 18 and ground: with mute function.

DEVELOPMENT SAMPLE DATA

TDA3652
TDA3652Q

VERTICAL DEFLECTION CIRCUIT

GENERAL DESCRIPTION

The TDA3652 is an integrated power output circuit for vertical deflection in systems with deflection currents up to 3 A peak to peak.

Features

- Driver
- Output stage and protection circuits
- Flyback generator
- Voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_{9\text{-}4} = V_P$		0 to 40	V
Peak output voltage during flyback (pin 5)	$V_{5\text{-}4M}$	<	55	V
Output current (peak-to-peak value)	$I_{5(p\text{-}p)}$	max.	3	A
Operating junction temperature	T_j	max.	150	°C
Thermal resistance from junction to mounting base	$R_{th\ j\text{-}mb}$	max.	4	K/W

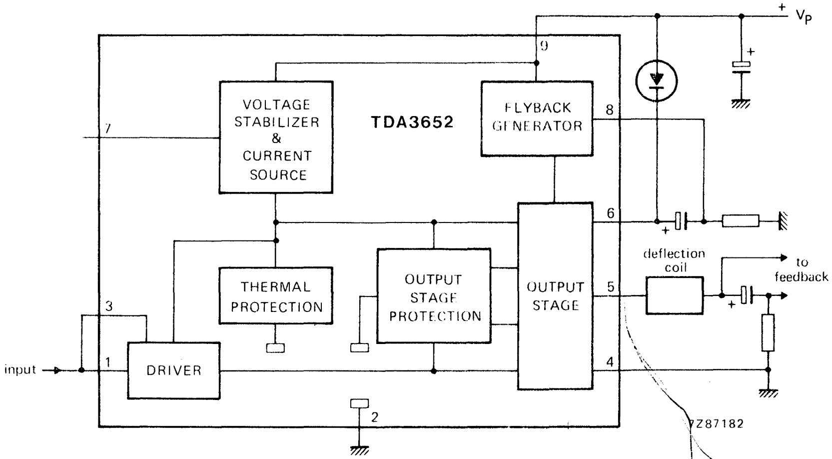


Fig. 1 Block diagram.

PACKAGE OUTLINES

TDA3652: 9-lead SIL; plastic (SOT-131B).
TDA3652Q: 9-lead SIL bent to DIL; plastic (SOT-157B).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages (pins 4 and 2 externally connected to ground)

Output voltage (pin 5)	$V_{5\text{-}4}$		0 to 55 V
Supply voltage (pin 9)	$V_{9\text{-}4} = V_P$		0 to 40 V
Supply voltage output stage (pin 6)	$V_{6\text{-}4}$		0 to 55 V
Driver input voltage (pin 1)	$V_{1\text{-}2}$		0 to V_P V*
Switching circuit input voltage (pin 3)	$V_{3\text{-}2}$		0 to 5,6 V

Currents

Repetitive peak output current (pin 5)	$\pm I_{5RM}$	max.	1,5 A
Non-repetitive peak output current (pin 5)	$\pm I_{5SM}$	max.	3 A**
Repetitive peak flyback generator output current (pin 8)	I_{8RM}	max.	−1,5 A +1,6 A
Non-repetitive peak flyback generator output current (pin 8)	$\pm I_{8SM}$	max.	3 A**

Temperatures

Storage temperature range	T_{stg}	−65 to +150 °C
Operating ambient temperature range	T_{amb}	−25 to +65 °C
Operating junction temperature range	T_j	−25 to +150 °C

---

* The maximum input voltage should not exceed the supply voltage (V_P at pin 9). In most applications pin 1 is connected to pin 3; the maximum input voltage should then not exceed 5,6 V.

** Non-repetitive duty factor maximum 3,3%.

CHARACTERISTICS

V_P = 26 V; T_{amb} = 25 °C; pins 4 and 2 externally connected to ground; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage; pin 9	V_P	10	–	40	V*
Supply voltage output stage; pin 6	V_{6-4}	–	–	55	V*
Supply current (no load and no quiescent current); pin 9	I_P	–	9	12	mA
Quiescent current (see Fig. 2)	I_4	25	40	65	mA
Variation of quiescent current with temperature	ΔI_4	–	–0,04	–	mA/K
Output current					
Output current (pin 5) (peak-to-peak value)	$I_{5(p-p)}$	–	2,5	3,0	A
Output current flyback generator (pin 8)	$-I_8$	–	1,35	1,6	A
Output current flyback generator (pin 8)	I_8	–	1,25	1,5	A
Output voltage					
Peak voltage during flyback	V_{5-4M}	–	–	55	V
Saturation voltage to supply at $-I_5$ = 1,5 A	$-V_{5-6sat}$	–	2,5	3,0	V
Saturation voltage to ground at I_5 = 1,5 A	V_{5-4sat}	–	2,5	3,0	V
Saturation voltage to supply at $-I_5$ = 1 A	$-V_{5-6sat}$	–	2,2	2,7	V
Saturation voltage to ground at I_5 = 1 A	V_{5-4sat}	–	2,2	2,7	V
Flyback generator					
Saturation voltage at $-I_8$ = 1,6 A	V_{9-8sat}	–	1,6	2,1	V
Saturation voltage at I_8 = 1,5 A	V_{8-9sat}	–	2,5	3,0	V
Saturation voltage at $-I_8$ = 1,1 A	V_{9-8sat}	–	1,4	1,9	V
Saturation voltage at I_8 = 1 A	V_{8-9sat}	–	2,3	2,8	V
Flyback generator active if:	V_{5-9}	4	–	–	V
Leakage current at pin 8	$-I_8$	–	5	100	μA
Input current for I_5 = 4 A at pin 1 (peak-to-peak value)	$I_{1(p-p)}$	190	240	400	μA
Input voltage during scan (pin 1)	V_{1-2}	1,3	2,0	3,5	V
Input current during scan (pin 3)	I_3	0,01	–	2,5	mA

* The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 55 V.

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Flyback generator (continued)					
Input voltage during scan (pin 3)	$V_{3\text{-}2}$	0,9	–	5,6	V
Input voltage during flyback (pin 3)	$V_{3\text{-}2}$	0	–	0,2	V
General data					
Junction temperature of switching on the thermal protection	T_j	158	175	192	°C
Thermal resistance from junction to mounting base	$R_{th\ j\text{-}mb}$	–	–	4	K/W
Total power dissipation	P_{tot}		see Fig. 3		
Open-loop gain at 1 kHz	G_o	–	36	–	dB
Frequency response (–3 dB) at R_L = 1 kΩ	f	–	50	–	kHz

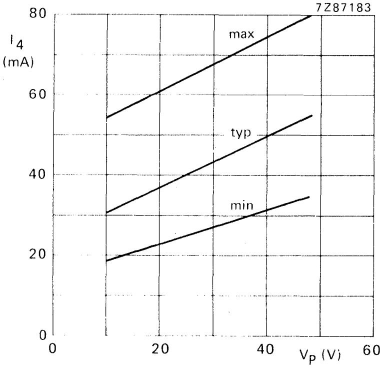


Fig. 2 Quiescent current (I_4) as a function of supply voltage (V_P).

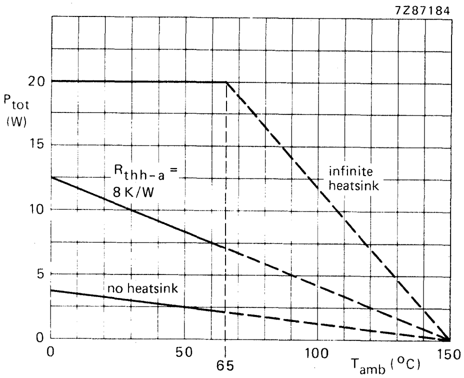


Fig. 3 Power derating curve.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. Driver

This is the input for the driver of the output stage.

2. Negative supply (ground)

3. Switching circuit

This pin is normally connected externally to pin 1. It is also possible to use this pin to drive the switching circuit for different applications. This switching circuit rapidly turns off the lower output stage at the end of scan and also allows for a quick start of the flyback generator.

4. Output stage ground

5 and 6. Output stage and protection circuits

Pin 5 is the output pin and pin 6 is the output stage supply pin. The output stage is a class-B type with each transistor capable of delivering 1,5 A maximum. The "upper" output transistor is protected against short-circuit currents to ground. The base of the "lower" power transistor is connected to ground during flyback and so it is protected against too high flyback pulses which may occur during adjustments. In addition the output transistors are protected by a special layout of the internal circuit. The circuit is protected thermally against excessive dissipation by a circuit which operates at temperatures of 175 °C upwards causing the output current to drop to a value such that the dissipation cannot increase.

DEVELOPMENT SAMPLE DATA

7. Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply voltage of 6 V for drive of the output stage, so the drive current is not influenced by the various voltages of different applications.

8 and 9. Flyback generator

Pin 8 is the output pin of the flyback generator. Depending on the value of the external resistor at pin 8, the capacitor at pin 6 will be charged to a fixed level during the scan period. The maximum height of this level is equal to the supply voltage at pin 9 (V_P). When the flyback starts and the flyback pulse at pin 5 exceeds the supply voltage, the flyback generator is activated and then the supply voltage is connected in series (via pin 8) with the voltage across the capacitor. The voltage at the supply pin (pin 6) of the output stage will then be not more than twice the supply voltage.

VERTICAL DEFLECTION CIRCUIT

GENERAL DESCRIPTION

The TDA3653 is a vertical deflection output circuit for drive of various deflection systems with currents up to 1,5 A peak-to-peak.

Features

- Driver
- Output stage
- Thermal protection and output stage protection
- Flyback generator
- Voltage stabilizer
- Guard circuit

QUICK REFERENCE DATA

Supply voltage range (pin 9)	$V_P = V_{9\text{-}4}$		0 to 40	V
Peak output voltage during flyback (pin 5)	$V_{5\text{-}4M}$	max.	60	V
Output current (peak-to-peak value)	$I_{5(p\text{-}p)}$	max.	1,5	A
Operating junction temperature	T_j	max.	150	^oC
Thermal resistance from junction to mounting base				
(SOT-110B)	$R_{th\ j\text{-}mb}$	typ.	10	K/W
(SOT-131B)	$R_{th\ j\text{-}mb}$	typ.	3,5	K/W

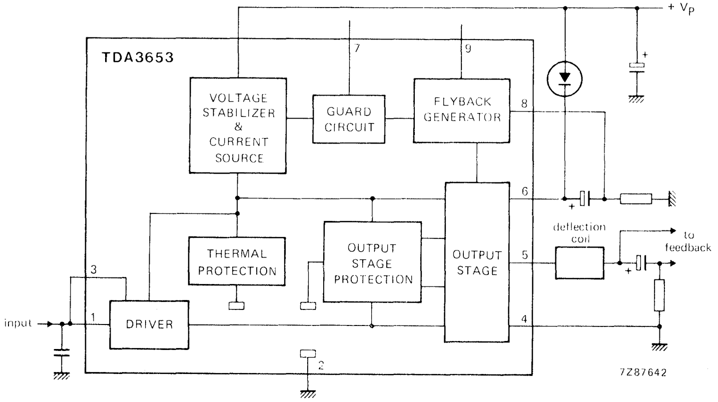


Fig. 1 Block diagram.

PACKAGE OUTLINES

TDA3653: 9-lead SIL; plastic (SOT-110B).
TDA3653A: 9-lead SIL; plastic power (SOT-131B).

FUNCTIONAL DESCRIPTION

Output stage and protection circuit

Pin 5 is the output pin. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4. The output transistors of the class-B output stage can each deliver 0,75 A maximum. The maximum voltage for pin 5 and 6 is 60 V.

The output power transistors are protected such that their operation remains within the SOAR area. This achieved by the co-operation of the thermal protection circuit, the current-voltage detector, the short-circuit protection and the special measures in the internal circuit layout.

Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied to pin 3 which is the input of a switching circuit. When the flyback starts, this switching circuit rapidly turns off the lower output stage and so limits the turn-off dissipation. It also allows a quick start of the flyback generator.

External connection of pin 1 to pin 3 allows for applications in which the pins are driven separately.

Flyback generator

During scan the capacitor at pin 6 is charged to a maximum voltage, which is dependent on the value of the resistor at pin 8. During normal operation the voltage at pin 8 may not be lower than 2,2 V.

When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage (pin 9), the flyback generator is activated. Then $V_P = 2$ V is connected in series (via pin 8) with the voltage across the capacitor.

The voltage at the supply pin (pin 6) of the output stage will then be maximum $2V_P - 2$ V. Lower voltages can be obtained, determined by the value of the resistor at pin 8.

Guard circuit

When there is no deflection current and the flyback generator is not activated, the voltage at pin 8 reduces to less than 2 V. The guard circuit will then produce a d.c. voltage at pin 7, which can be used to blank the picture tube and thus prevent screen damage.

Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V to drive the output stage, which prevents the drive current of the output stage being affected by supply voltage variations.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134); pins 4 and 2 externally connected to ground.

Supply voltage (pin 9)	$V_P = V_{9\text{-}4}$	max.	40	V
Supply voltage output stage (pin 6)	$V_{6\text{-}4}$	max.	60	V
Output voltage (pin 5)	$V_{5\text{-}4}$	max.	60	V
Input voltage (pins 1 and 3)	$V_{1;\,3\text{-}2}$	max.	V_P	V
External voltage at pin 7	$V_{7\text{-}2}$	max.	5,6	V
Peak output current (pin 5)				
repetitive	$\pm I_{5RM}$	max.	0,75	A
non-repetitive	$\pm I_{5SM}$	max.	1,5	A*
Peak output current (pin 8)				
repetitive	I_{8RM}	−0,85 to	+ 0,75	A
non-repetitive	$\pm I_{8SM}$	max.	1,5	A*
Total power dissipation	P_{tot}	see Fig. 2		
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}	see Fig. 2		
Operating junction temperature range	T_j		−25 to + 150	°C

DEVELOPMENT SAMPLE DATA

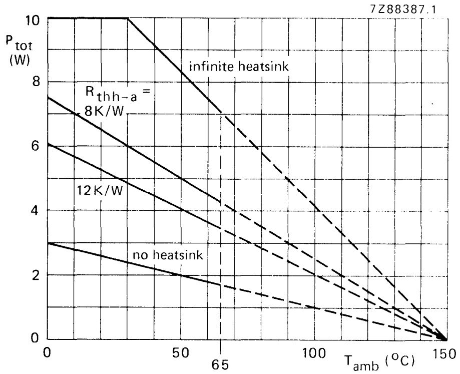


Fig. 2 Power derating curves (for SOT-110B).

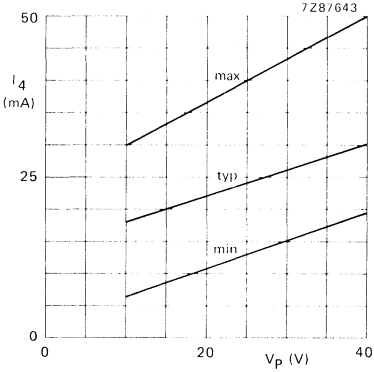


Fig. 3 Quiescent current I_4 as a function of supply voltage V_P.

---

* Non-repetitive duty factor maximum 3,3%.

CHARACTERISTICS

$V_P = V_{9\text{-}4} = 26$ V; $T_{amb} = 25$ °C; pins 2 and 4 externally connected to ground; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage; pin 9 (note 1)	$V_P = V_{9\text{-}4}$	10	–	40	V
Supply voltage; pin 6 (note 1)	$V_{6\text{-}4}$	–	–	60	V
Supply current; pin 9 (note 2)	$I_P = I_9$	–	10	20	mA
Quiescent current; pin 4 (see Fig. 3)	I_4	6	25	40	mA
Variation of quiescent current with temperature	ΔI_4	–	–0,04	–	mA/K
Output current					
Output current (pin 5) (peak-to-peak value)	$I_{5(p\text{-}p)}$	–	1,2	1,5	A
Output current flyback generator (pin 8)	$-I_8$	–	0,7	0,85	A
Output current flyback generator (pin 8)	I_8	–	0,6	0,75	A
Output voltage					
Peak voltage during flyback	$V_{5\text{-}4M}$	–	–	60	V
Saturation voltage to supply					
at $-I_5 = 0,75$ A	$V_{6\text{-}5sat}$	–	2,5	3,0	V
at $I_5 = 0,75$ A (note 3)	$V_{5\text{-}6sat}$	–	2,5	3,0	V
at $-I_5 = 0,6$ A	$V_{6\text{-}5sat}$	–	2,2	2,7	V
at $I_5 = 0,6$ A (note 3)	$V_{5\text{-}6sat}$	–	2,3	2,8	V
Saturation voltage to ground					
at $I_5 = 0,75$ A	$V_{5\text{-}4sat}$	–	2,0	2,5	V
at $I_5 = 0,6$ A	$V_{5\text{-}4sat}$	–	1,7	2,2	V
Flyback generator					
Satuartion voltage					
at $-I_8 = 0,85$ A	$V_{9\text{-}8sat}$	–	1,6	2,1	V
at $I_8 = 0,75$ A (note 3)	$V_{8\text{-}9sat}$	–	2,3	2,8	V
at $-I_8 = 0,7$ A	$V_{9\text{-}8sat}$	–	1,4	1,9	V
at $I_8 = 0,6$ A (note 3)	$V_{8\text{-}9sat}$	–	2,2	2,7	V
Flyback generator active if:	$V_{5\text{-}9}$	4	–	–	V
Leakage current at pin 8	$-I_8$	–	5	100	µA
Input current (pin 1) at $I_{5(p\text{-}p)} = 1,5$ A	I_1	–	–	1,3	mA
Input voltage during scan (pin 1)	$V_{1\text{-}2}$	–	–	3,2	V
Input voltage during scan (pin 3) pins 1 and 3 not connected	$V_{3\text{-}2}$	0,9	–	V_P	V

parameter	symbol	min.	typ.	max.	unit
Input current during scan (pin 3) pins 1 and 3 not connected	I_3	0,01	–	–	mA
Input current during scan (pin 3) pins 1 and 3 connected	I_3	–	–	0,52	mA
Input resistance (pin 3)	R_3	3,75	5,0	6,25	kΩ
Input voltage during flyback (pin 1)	$V_{1\text{-}2}$	–	–	250	mV
Input voltage during flyback (pin 3)	$V_{3\text{-}2}$	–	–	250	mV
Guard circuit					
Output voltage; pin 7 (note 4)					
loaded with 100 kΩ	$V_{7\text{-}2}$	4,4	5,0	5,6	V
loaded with 0,5 mA	$V_{7\text{-}2}$	3,5	4,4	5,1	V
Internal series resistance of pin 7	R_{i7}	0,9	1,2	1,5	kΩ
Guard circuit active if $V_{8\text{-}2}$ is lower than (note 6)	$V_{8\text{-}2}$	–	–	2,0	V
General data					
Thermal protection becomes active if junction temperature exceeds	T_j	158	175	192	°C
Thermal resistance junction to mounting base	$R_{th\ j\text{-}mb}$	–	10	12	K/W
Open loop gain at 1 kHz (note 5)	G_o	–	42	–	dB
Frequency response (–3 dB) (note 7)	f	–	40	–	kHz

DEVELOPMENT SAMPLE DATA

Notes to the characteristics

1. The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 60 V.
2. These values are obtained (pin 9) at no load and no quiescent current.
3. Duty factor maximum 3,3%.
4. Guard circuit is active.
5. $R_{load} = 8\ \Omega$; $I_{load(rms)} = 125$ mA.
6. During normal operation the voltage $V_{8\text{-}2}$ may not be lower than 2,2 V.
7. With 220 pF between pins 1 and 5.

APPLICATION INFORMATION

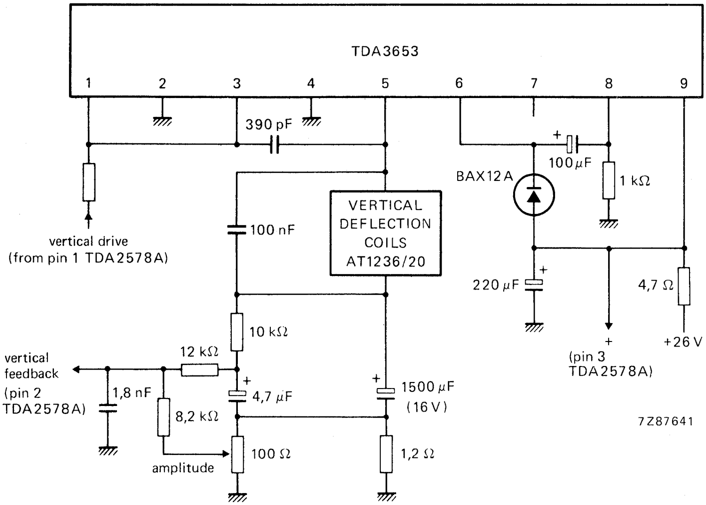


Fig. 4 Typical application circuit diagram of the TDA3653 (vertical output), when used in combination with the TDA2578A (see Fig. 5).

Note to deflection coils AT1236/20: L = 29 mH, R = 13,6 Ω; deflection current without overscan is 0,82 A peak-to-peak and e.h.t. voltage is 25 kV.

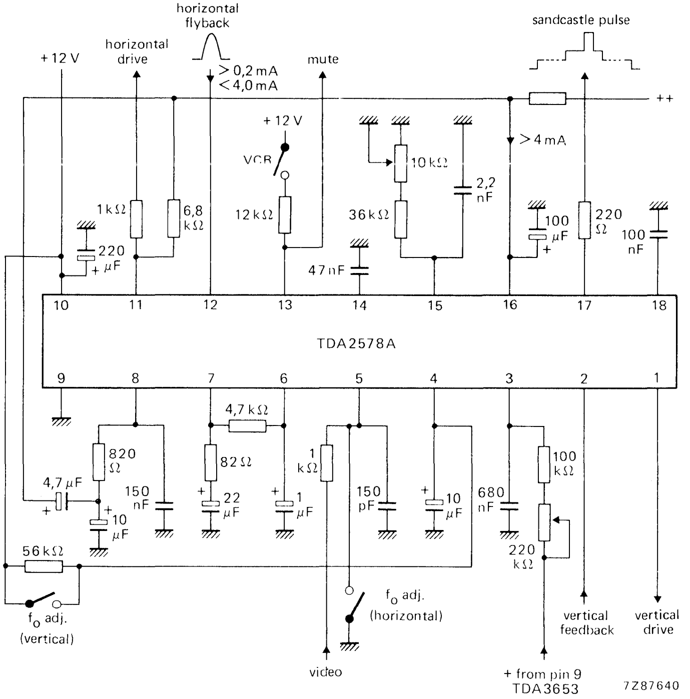


Fig. 5 Typical application circuit diagram; for combination of the TDA2578A with the TDA3653 (see Fig. 4).

DEVELOPMENT SAMPLE DATA

PAL SYNCHRONIZATION PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3701 is a monolithic integrated circuit for PAL synchronization processing in video recorders.

Features

- Sync separator with noise inverter
- Phase detector with 2 time constants for oscillator synchronization
- Automatic identification of norm-signals (625 lines referred to CCIR)
- Colour subcarrier oscillator with separate output (625 kHz sinewave) and 1: 40 divider
- Separate horizontal and vertical coincidence detectors
- Internal generation of a complete standard synchronization pulse
- Vertical synchronization pulse output
- Field identification output
- Burst gate pulse output (externally adjustable phase relationship)
- H/8 signal output with correction/inversion inputs
- Record (REC/TV; REC/VCR)/playback (PB) selector

QUICK REFERENCE DATA

Supply voltage (pin 22)	$V_P = V_{22\text{-}23}$	typ.	12	V
Supply current (pin 22)	$I_P = I_{22}$	typ.	85	mA
Sync separator				
Sync pulse amplitude (peak-to-peak value)	$V_{4\text{-}23(p\text{-}p)}$	typ.	0,3	V
Phase detector				
Catching range	Δf	typ.	± 5	%
Oscillator				
Output frequency	f_o	typ.	625	kHz
Output sinewave (peak-to-peak value)	$V_{7\text{-}23(p\text{-}p)}$	typ.	3,2	V
Field identification				
Output voltage				
1st field	$V_{26\text{-}23}$	min.	10	V
2nd field	$V_{26\text{-}23}$	max.	1	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

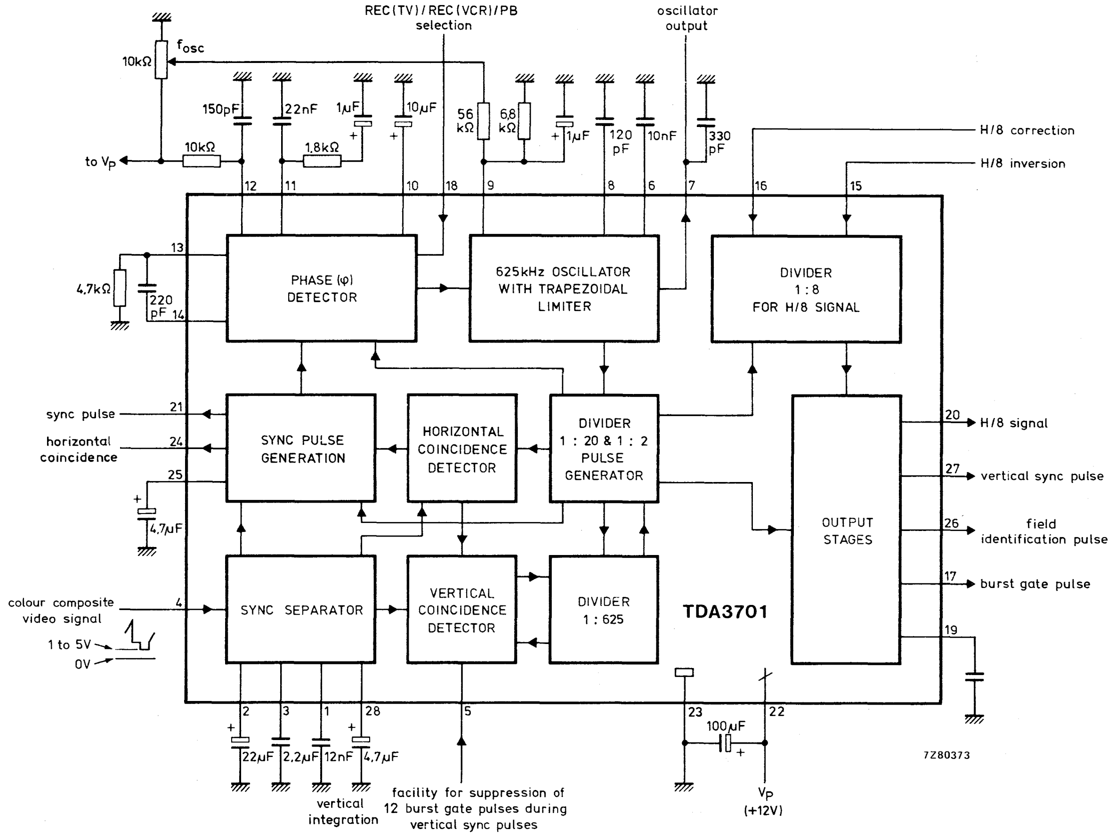


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 22)	$V_P = V_{22\text{-}23}$	max.	13,2	V
Voltage range at pins 4, 12, 15, 16, 18, 24 to pin 23 (ground)	$V_{n\text{-}23}$		0 to V_P	V
Voltage range at pin 9	$V_{9\text{-}23}$		0,3 V_P to 0,7 V_P	V
Voltage at pin 5	$V_{5\text{-}23}$	min.	0	V
Currents				
at pins 17, 20, 21, 24, 26, 27	I_n	max.	20	mA
at pin 5	I_5	max.	50	μA
at pin 7	$\pm I_7$	max.	1	mA
Total power dissipation	P_{tot}	max.	1,5	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS

$V_P = V_{22\text{-}23} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 22)					
Supply voltage range	$V_P = V_{22\text{-}23}$	9,6	–	13,2	V
Supply current	$I_P = I_{22}$	–	85	–	mA
Sync separator (pin 4)					
Colour composite video input voltage (note 1) (peak-to-peak value)	$V_{4\text{-}23(p\text{-}p)}$	–	1	–	V
Sync pulse amplitude (peak-to-peak value)	$V_{4\text{-}23(p\text{-}p)}$	0,1	0,3	0,6	V
Slicing level, relative to sync pulse amplitude		–	50	–	%
Output voltage (peak-to-peak value)	$V_{21\text{-}23(p\text{-}p)}$	10	–	–	V
Output current (peak-to-peak value)	$I_{21(p\text{-}p)}$	–	–	5	mA
Delay between signal at input pin 4 and sync pulse at output pin 21 (note 2)	t_d	–	0,4	–	μs
Adjustment of phase relationship (pin 12)		–	± 1	–	μs
Phase detector					
D.C. control voltages					
pin 10	$V_{10\text{-}23}$	–	3	–	V
pin 11	$V_{11\text{-}23}$	–	$V_{10\text{-}23}$	–	V
Catching range	Δf	–	± 5	–	%
Control sensitivity (note 3)		–	5,7	–	kHz/μs
625 kHz oscillator					
Output frequency with $C_{osc} = 120$ pF (pin 8); $R_{osc} = 6{,}8$ kΩ (pin 9) at pin 7 (note 4)	f_o	575	625	675	kHz
Output sinewave ($C_{7\text{-}23} = 330$ pF) (peak-to-peak value)	$V_{7\text{-}23(p\text{-}p)}$	–	3,2	–	V
D.C. output voltage	$V_{7\text{-}23}$	–	6,0	–	V
2nd harmonic suppression	α_{2nd}	35	–	–	dB
3rd harmonic suppression	α_{3rd}	30	–	–	dB
Horizontal coincidence detector					
D.C. output voltage					
no coincidence; $I_{24} = 5$ mA	$V_{24\text{-}23}$	–	–	2	V
coincidence	$V_{24\text{-}23}$	–	12	–	V

parameter	symbol	min.	typ.	max.	unit
Vertical sync pulse (note 5)					
Output voltage (peak-to-peak value)	$V_{27\text{-}23(p\text{-}p)}$	10	–	–	V
Output current (peak-to-peak value)	$I_{27(p\text{-}p)}$	–	–	4,5	mA
Duration of internally generated output pulse	t_p	–	160	–	μs
Delay between input signal at pin 4 and start of output pulse at pin 27	t_d	–	11	–	μs
Duration of the separated vertical sync pulse	t_p	–	260	–	μs
Delay between input signal at pin 4 and start of output pulse at pin 27	t_d	–	12	–	μs
Field identification pulse (pin 26)					
Output voltage					
1st field	$V_{26\text{-}23}$	10	–	–	V
2nd field	$V_{26\text{-}23}$	–	–	1	V
Output current (peak-to-peak value)	$I_{26(p\text{-}p)}$	–	–	4,5	mA
Duration of output pulse	t_p	–	20	–	ms
Burst gate pulse (pin 17)					
Amplitude of output pulse (peak-to-peak value)	$V_{17\text{-}23(p\text{-}p)}$	10	–	–	V
Output current (peak-to-peak value)	$I_{17(p\text{-}p)}$	–	–	5	mA
Duration of output pulse	t_p	–	4	–	μs
Delay between rising edge of horizontal sync pulse at pin 4 and rising edge of gate pulse at pin 17					
without external capacitor (pin 19)	t_d	–	5,1	–	μs
with external capacitor (pin 19)	$\Delta t_d/\Delta C$	–	3	–	ns/pF
H/8 signal output (pin 20)					
Amplitude of output pulse (peak-to-peak value)	$V_{20\text{-}23(p\text{-}p)}$	10	–	–	V
Output current (peak-to-peak value)	$I_{20(p\text{-}p)}$	–	–	5	mA
Duration of output pulse at $V_{15\text{-}23} = V_{16\text{-}23} > 5$ V	t_p	–	256	–	μs
Delay between rising edge of horizontal sync pulse at pin 4 and rising edge of H/8 at pin 20	t_d	–	–	2,5	μs
H/8 signal correction (note 6)					
input voltage for ‘correction’	$V_{16\text{-}23}$	–	–	2	V
input voltage for ‘no correction’	$V_{16\text{-}23}$	5	–	–	V
H/8 signal inversion					
input voltage for ‘inversion’	$V_{15\text{-}23}$	–	–	2	V
input voltage for ‘no inversion’	$V_{15\text{-}23}$	5	–	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
REC (TV)/REC (VCR)/PB selection					
REC (TV)					
input voltage	$V_{18\text{-}23}$	–	–	2	V
input current ($V_{18\text{-}23} = 2$ V)	I_{18}	–	–	200	μA
REC (VCR)					
input voltage	$V_{18\text{-}23}$	4	–	8	V
input current ($V_{18\text{-}23} = 8$ V)	I_{18}	–	–	1	mA
PB					
input voltage	$V_{18\text{-}23}$	10	–	–	V
input current ($V_{18\text{-}23} = 12$ V)	I_{18}	–	–	2	mA

Notes to characteristics

1. The sync separator input signal is shown in Fig. 2.

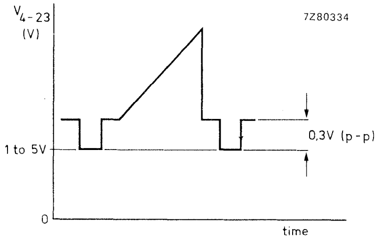


Fig. 2 Colour composite video input signal at pin 4.

2. The internally generated standard sync pulse is available at pin 21 if: horizontal and vertical coincidence is detected, that is, a standard input signal is applied to pin 4 and the record/playback selector is in the record mode.
3. The control sensitivity of the phase detector is related to the horizontal frequency.
4. Balance of the oscillator output frequency is achieved if pins 10 and 11 are short-circuited.
5. The vertical sync pulse is also available without application of the colour composite video signal provided the record/playback selector is in the record mode.
6. During active correction of the H/8 signal one of 8 input pulses of the 1 : 8 divider circuit will be rejected in a time interval of 4 fields.

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION

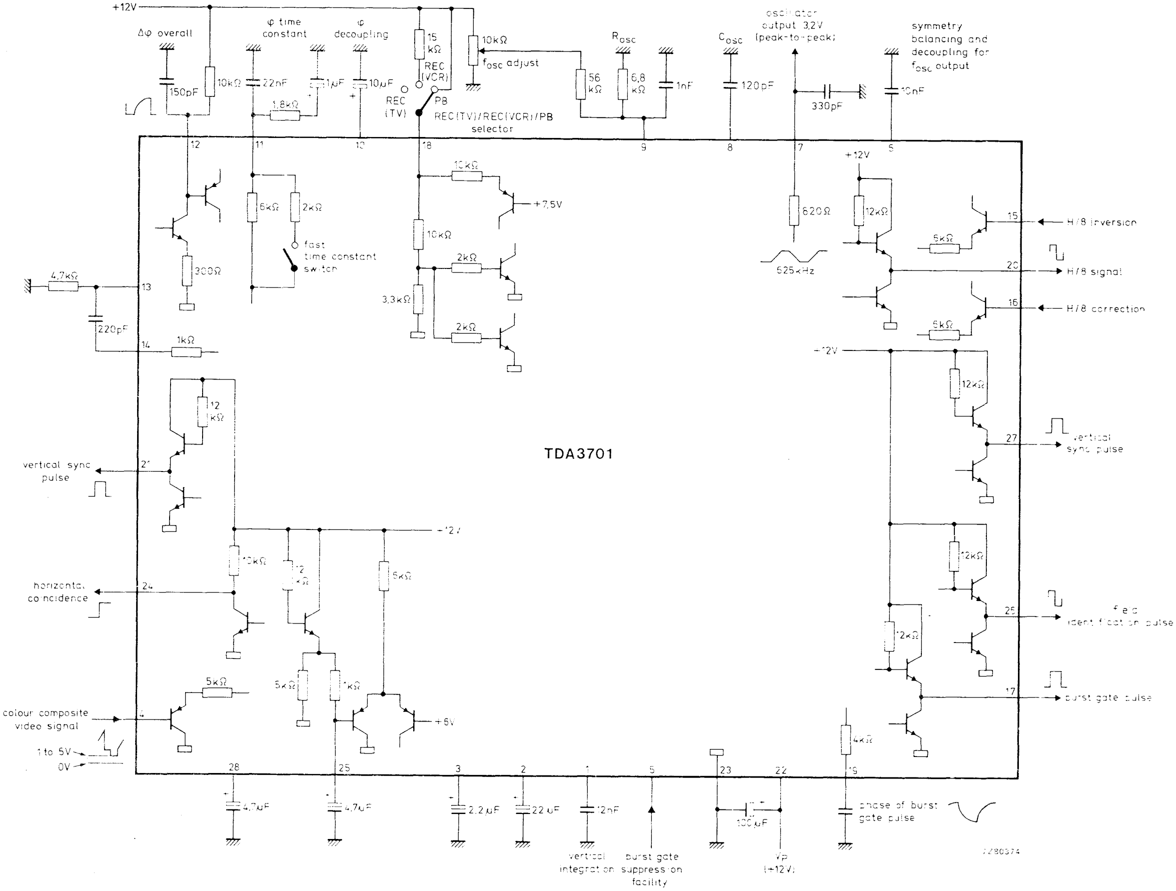


Fig. 3 Application circuit diagram.

CHROMINANCE SIGNAL/MIXER FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3710 is a monolithic integrated circuit for chrominance signal processing in video recorders.

Features

- Automatic gain controlled preamplifier with record/playback selection
- Signal mixer with balancing stage for phase inversion of chrominance signal
- H/8-control for subcarrier phase inversion
- Amplifier with record/playback selected burst pre- and de-emphasis
- Output stage for the 625 kHz chrominance signal, with facility for being disabled by colour killer, record/playback mode switch and external track sensing circuit
- Amplitude detector with automatic gain control for the preamplifier
- 4,43 MHz voltage controlled oscillator (VCO) for recording and 4,43 MHz local oscillator for playback
- Phase discriminator controlled synchronization of the voltage controlled oscillator
- Subcarrier mixer, disabled for SECAM operation
- H/2 demodulator for the production of PAL identification and colour killing signals
- Flip-flop for PAL identification
- Burst pulse stage for the production of non-delayed (BK1) and delayed (BK2) keying pulses
- Colour killing stage with hysteresis and heterodyned H/2 signal
- Threshold voltage detector for SECAM operation or forced colour on/off
- Voltage stabilization with external reference voltage (5,6 V)
- Internal record/playback and PAL/SECAM selection.

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10\text{-}16}$	typ.	10	V
Supply current (pin 10)	$I_P = I_{10}$	typ.	61	mA
Inputs				
Chrominance signal				
4,43 MHz for record (peak-to-peak value)	$V_{2\text{-}16(p\text{-}p)}$	typ.	200	mV
625 kHz for playback (peak-to-peak value)	$V_{1\text{-}16(p\text{-}p)}$	typ.	200	mV
Outputs				
Chrominance signal				
4,43 MHz (peak-to-peak value)	$V_{23\text{-}16(p\text{-}p)}$	typ.	470	mV
625 kHz (peak-to-peak value)	$V_{26\text{-}16(p\text{-}p)}$	typ.	2	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

P = PAL
S = SECAM
BK1 = burst key pulse 1
BK2 = burst key pulse 2
REC = record
PB = playback
CK = colour killer

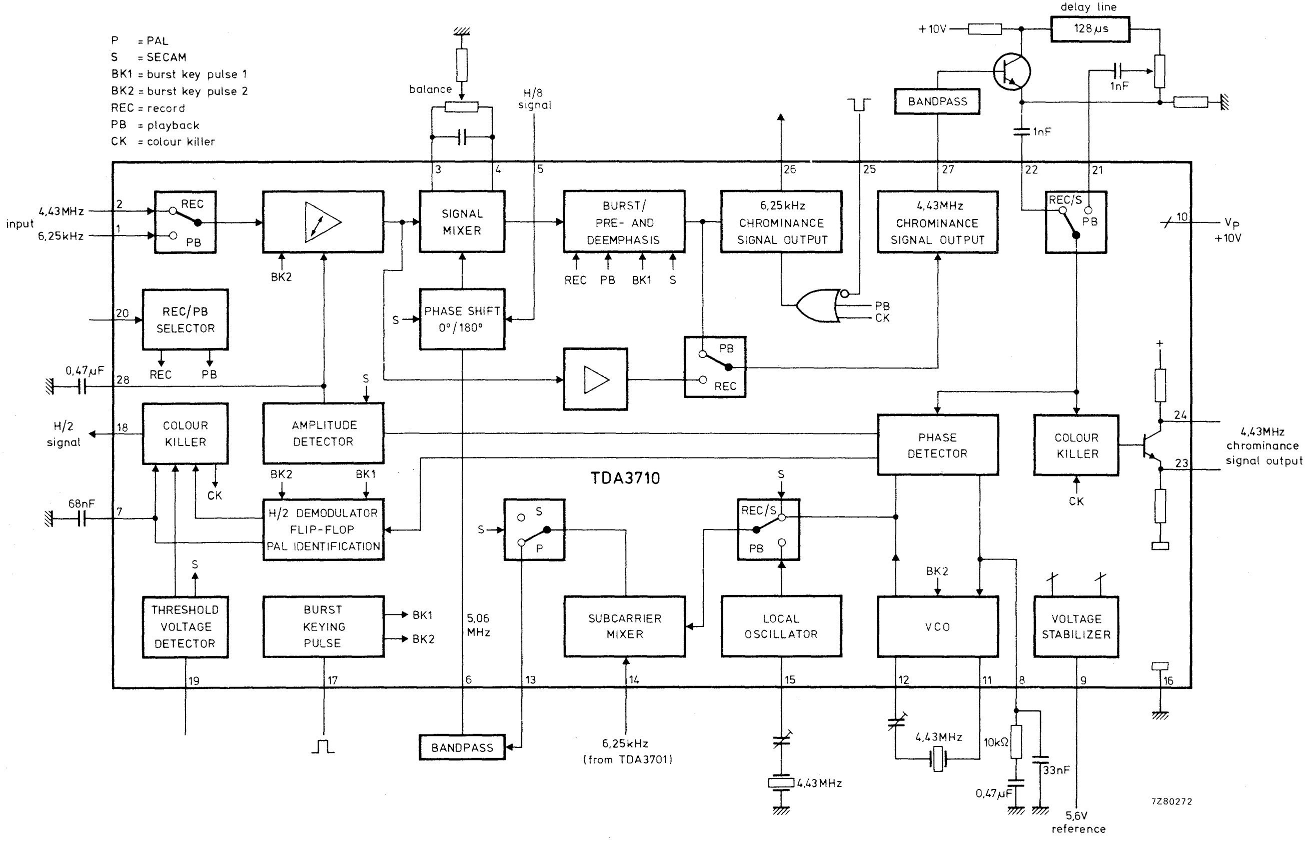


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 10)	$V_P = V_{10-16}$	max.	13,2	V
Voltage range at pins 1, 2, 5, 7, 8, 9, 17, 19, 20, 21, 22, 25 to pin 16 (ground)	V_{n-16}		0 to V_P	V
Voltage ranges				
at pins 3, 4*	$V_{3, 4-16}$		3 to 6	V
at pin 6*	V_{6-16}		0 to 5	V
at pin 11*	V_{11-16}		1,5 to 4	V
at pin 14*	V_{14-16}		0 to 3	V
at pin 15*	V_{15-16}		0 to 8	V
at pin 24	V_{24-16}		5 to V_P	V
Voltages				
at pin 13	V_{13-16}	max.	9	V
at pin 23	V_{23-16}	max.	7	V
Currents				
at pins 12, 18	$-I_{12,18}$	max.	2	mA
at pins 13, 26, 27	$-I_{13, 26, 27}$	max.	5	mA
at pin 23	$-I_{23}$	max.	3	mA
Total power dissipation	P_{tot}	max.	2	W
Storage temperature range	T_{stg}		−55 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

---

* Measured with $V_{9-16} = 5{,}6$ V and applied supply voltage.

CHARACTERISTICS

$V_P = V_{10-16} = 10$ V; $V_{9-16} = 5{,}6$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 10)					
Supply voltage	$V_P = V_{10-16}$	9,6	–	13,2	V
Supply current for playback and burst keying					
at $-I_{13, 18, 23, 26, 27} = 0$	$I_P = I_{10}$	–	61	–	mA
at $-I_{13, 18, 23, 26, 27} = 0$; $V_P = 12$ V	$I_P = I_{10}$	–	62	–	mA
A.G.C. preamplifier (pins 1 and 2)					
Input voltage (f = 4,43 MHz) during record (peak-to-peak value)	$V_{2-16(p-p)}$	20	–	400	mV
Input voltage (f = 6,25 kHz) during playback (peak-to-peak value)	$V_{1-16(p-p)}$	30	–	400	mV
Input resistance	$R_{1, 2-16}$	6	–	–	kΩ
Input capacitance	$C_{1, 2-16}$	–	–	5	pF
625 kHz chrominance signal (pin 26)* (transposed on to 625 kHz signal)					
Output voltage (peak-to-peak value)	$V_{26-16(p-p)}$	–	2	–	V
Burst pre-emphasis (gain)	G_{26}	–	6	–	dB
Signal suppression at output					
for f = 1,25 MHz	α_{26}	–	35	–	dB
for f = 5,06 MHz (externally balanced via pins 3 and 4)	α_{26}	–	40	–	dB
during colour killing (pin 25)	α_{26}	40	–	–	dB
D.C. output voltage	V_{26-16}	–	6,7	–	V
Colour killing voltage	V_{25-16}	–	–	2	V
4,43 MHz chrominance signal (pin 27)*					
Output voltage					
during record (peak-to-peak value)	$V_{27-16(p-p)}$	–	1,15	–	V
during playback after signal mixing subcarrier (peak-to-peak value)	$V_{27-16(p-p)}$	–	–	3,1	V
Burst de-emphasis (gain)	G_{27}	–	−5	–	dB
Signal suppression at output					
for f = 5,06 MHz (externally balanced)	α_{27}	–	40	–	dB
for f = 8,86 MHz	α_{27}	–	30	–	dB
for f = 3,81 MHz	α_{27}	–	38	–	dB
for f = 3,18 MHz	α_{27}	–	30	–	dB
D.C. output voltage	V_{27-16}	–	7	–	V

* The chrominance signal values hold for a 75% saturated colour bar signal.

parameter	symbol	min.	typ.	max.	unit
4,43 MHz chrominance signal amplifier*					
Burst input signal					
at pin 21 (peak-to-peak value)	$V_{21-16(p-p)}$	–	190	–	mV
at pin 22 (peak-to-peak value)	$V_{22-16(p-p)}$	–	190	–	mV
Input resistance					
at pin 21	R_{21-16}	3,3	–	–	kΩ
at pin 22	R_{22-16}	3,3	–	–	kΩ
Output voltage of the chrominance signal					
at pin 23 (peak-to-peak value)	$V_{23-16(p-p)}$	–	470	–	mV
at pin 24 (peak-to-peak value)**	$V_{24-16(p-p)}$	–	–	2	V
Signal suppression at output (pin 23) during colour killing	α_{23}	35	–	–	dB
D.C. output voltage					
during colour-on	V_{23-16}	–	2,4	–	V
during colour-off (killed)	V_{23-16}	–	0,7	–	V
Subcarrier-mixer					
625 kHz input voltage; sinewave (peak-to-peak value)	$V_{14-16(p-p)}$	220	–	–	mV
Input resistance	R_{14-16}	1	–	–	kΩ
D.C. output voltage	V_{13-16}	–	6,25	–	V
5,06 MHz output voltage▲ selective (peak-to-peak value)	$V_{13-16(p-p)}$	–	800	–	V
Signal suppression at output▲					
for f = 4,43 MHz	α_{13}	20	–	–	dB
for f = 5,68 MHz	α_{13}	30	–	–	dB
Subcarrier amplifier and H/8 selector					
5,06 MHz input voltage (peak-to-peak value)	$V_{6-16(p-p)}$	250	–	–	mV
Input resistance	R_{6-16}	1,9	–	–	kΩ
Input capacitance	C_{6-16}	–	–	5	pF
Input voltage (pin 5)					
for H/8 selector ON	V_{5-16}	1,6	–	–	V
for H/8 selector OFF	V_{5-16}	–	–	0,8	V
Input resistance with $V_{5-16} > 1,6$ V	R_{5-16}	3	–	–	kΩ

---

* Chrominance signal values hold for a 75% saturated colour bar signal.

** Output voltage externally adjusted.

▲ Measured with a 0,3 V (peak-to-peak), 625 kHz input signal on pin 14 ($-I_{13}$ = 1 mA).

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
4,43 MHz voltage controlled oscillator (VCO)					
Input resistance	$R_{11\text{-}16}$	–	430	–	Ω
Input capacitance	$C_{11\text{-}16}$	–	–	10	pF
Output resistance	$R_{12\text{-}16}$	–	–	220	Ω
PLL-controlled oscillator catching range	Δf	± 500	–	–	Hz
Phase difference between oscillator and burst signals for ± 400 Hz deviation of crystal frequency	φ	± 7	–	–	deg
4,43 MHz local oscillator					
Oscillator temperature coefficient*	TC	–	–	3	Hz/K
Record/playback selector (pin 20)					
Input voltage for record**	$V_{20\text{-}16}$	–	–	4	V
Input current with $V_{20\text{-}16} = 4$ V	I_{20}	–	–	130	μA
Input voltage for playback	$V_{20\text{-}16}$	8	–	–	V
Input current with $V_{20\text{-}16} = 8$ V	I_{20}	–	–	430	μA
Input resistance	$R_{20\text{-}16}$	7	–	–	kΩ
Colour on/off and SECAM selector					
Input voltage (pin 19)					
for forced colour ON	$V_{19\text{-}16}$	–	$V_{9\text{-}16}$	–	V
for forced colour OFF	$V_{19\text{-}16}$	–	–	0,5	V
for SECAM operation	$V_{19\text{-}16}$	8,8	–	–	V
for PAL operation (normal)	$V_{19\text{-}16}$		pin open		
Output voltage (pin 18)▲					
with colour ON	$V_{18\text{-}16}$	5,9	–	–	V
with colour OFF	$V_{18\text{-}16}$	–	–	1	V

* Not considering the effects of external components.

** Pin open: record.

▲ D.C. average heterodyned by 1,6 V (peak-to-peak) H/2 signal.

parameter	symbol	min.	typ.	max.	unit
Voltage stabilizer (pin 9)					
External reference voltage range	$V_{9\text{-}16}$	5,4	–	5,8	V
Input current	$-I_9$	–	–	0,12	mA
Burst keying pulse (pin 17)					
Threshold voltage for burst keying	$V_{17\text{-}16}$	7,5	–	–	V
Input current	I_{17}	–	–	5	μA
Delay time of BK2	t_d	–	1,0	–	μs
SECAM operation (with $V_{19\text{-}16} > 8{,}8$ V)					
5,0 MHz subcarrier input signal (pin 6) with phase inversion internally switched OFF (peak-to-peak value)	$V_{6\text{-}16(p\text{-}p)}$	250	–	–	mV
Chrominance signal output voltage* (peak-to-peak value)	$V_{23\text{-}1(p\text{-}p)}$	–	370	–	mV
D.C. output voltage with subcarrier-mixer switched OFF	$V_{13\text{-}16}$	–	3,5	–	V

DEVELOPMENT SAMPLE DATA

---

* Chrominance signal values hold for a 75% saturated colour bar signal.

SECAM PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3720 is a monolithic integrated circuit for SECAM signal processing in PAL/SECAM video recorders.

Features

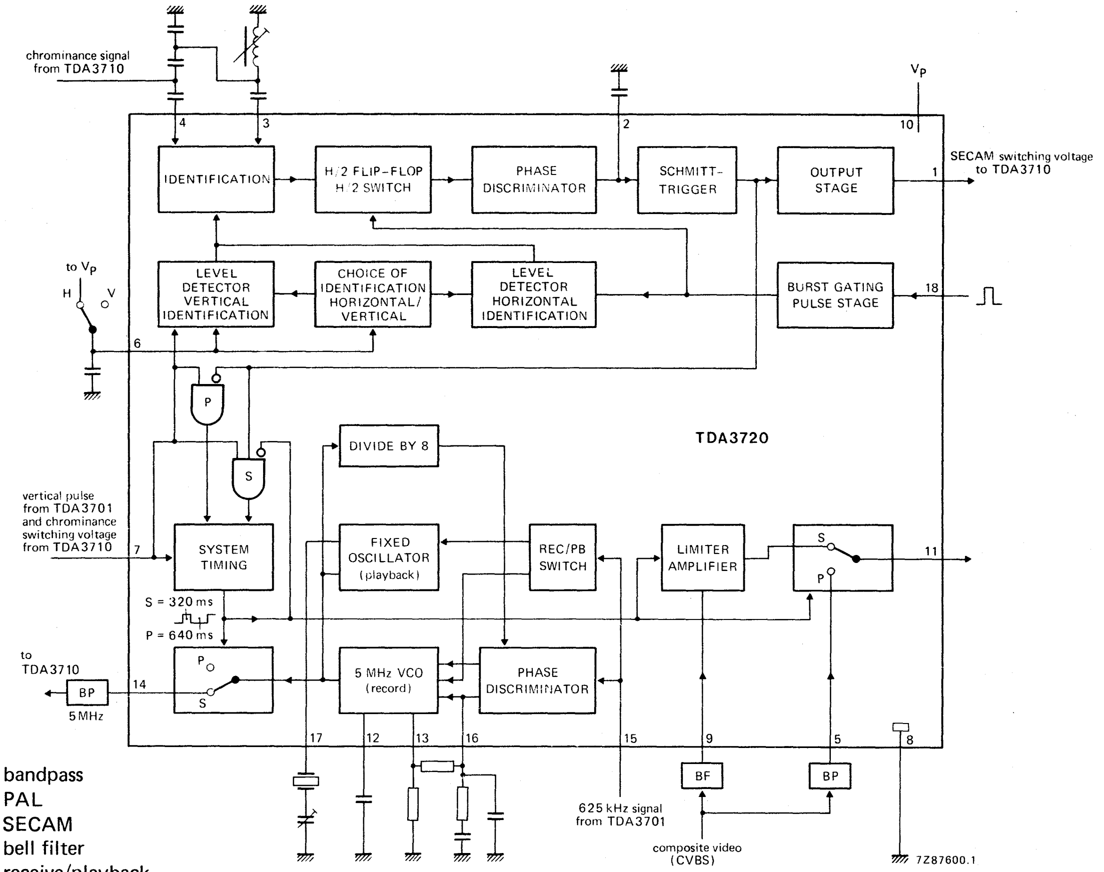
- Limiter amplifier
- Switch for choice of identification (horizontal or vertical)
- H/2 flip-flop and H/2 switch
- PAL/SECAM system timing
- PAL/SECAM switch
- 5 MHz voltage controlled oscillator (VCO) for record
- 5 MHz fixed oscillator for playback
- 1 : 8 divider stage to obtain 625 kHz signal
- Record/playback switch (REC/PB)

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10\text{-}8}$	typ.	10	V
Supply current (pin 10)	$I_P = I_{10}$	typ.	35	mA
Chrominance input signal (peak-to-peak value)				
PAL (pin 5)	$V_{5\text{-}8(p\text{-}p)}$	max.	200	mV
SECAM (pin 9)	$V_{9\text{-}8(p\text{-}p)}$	max.	500	mV
Chrominance input signal for identification (peak-to-peak value)	$V_{4\text{-}8(p\text{-}p)}$	max.	1,8	V
Burst gating pulse	$V_{18\text{-}8}$	min.	5	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).



BP = bandpass
P = PAL
S = SECAM
BF = bell filter
REC/PB = receive/playback
VCO = voltage controlled oscillator

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 10)	$V_P = V_{10\text{-}8}$	max.	13,2	V
Voltage range at pins 2, 3, 4, 5, 6, 7, 9, 12, 13, 15, 16, 18 to pin 8 (ground)	$V_{n\text{-}8}$		0 to V_P	V
Currents				
at pins 1, 11, 14	$-I_{1, 11, 14}$	max.	5	mA
at pin 17	$\pm I_{17}$	max.	10	mA
Total power dissipation	P_{tot}	max.	570	mW
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

CHARACTERISTICS

$V_P = V_{10\text{-}8} = 10$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 10)					
Supply voltage range	$V_P = V_{10\text{-}8}$	9,6	–	13,2	V
Supply current	$I_P = I_{10}$	–	35	–	mA
Limiter amplifier					
Chrominance input signal PAL (pin 5)					
input voltage (peak-to-peak value)	$V_{5\text{-}8(p\text{-}p)}$	–	–	200	mV
input resistance	$R_{5\text{-}8}$	8	–	–	kΩ
input capacitance	$C_{5\text{-}8}$	–	–	5	pF
Chrominance input signal SECAM (pin 9)					
input voltage (peak-to-peak value)	$V_{9\text{-}8(p\text{-}p)}$	–	–	500	mV
input resistance	$R_{9\text{-}8}$	1,5	–	–	kΩ
input capacitance	$C_{9\text{-}8}$	–	–	5	pF
level for start of limiting (peak-to-peak value)	$V_{9\text{-}8(p\text{-}p)}$	–	–	30	mV
Limited output signal (pin 11) (peak-to-peak value)	$V_{11\text{-}8(p\text{-}p)}$	–	200	–	mV
Gain (SECAM)	$G_{11\text{-}9}$	–	20	–	dB
Gain (PAL)	$G_{11\text{-}5}$	–	0	–	dB
D.C. output voltage emitter follower with a current source of 0,3 mA	$V_{11\text{-}8}$	–	3,2	–	V
Voltage controlled oscillator					
Output frequency (pin 14) with C_{osc} = 56 pF (pin 12); R_{osc} = 13 kΩ (pin 13)	f_o	–	5	–	MHz
Output sine-wave (peak-to-peak value)	$V_{14\text{-}8(p\text{-}p)}$	–	0,7	–	V
D.C. output voltage					
PAL	$V_{14\text{-}8}$	–	3,5	–	V
SECAM	$V_{14\text{-}8}$	–	8	–	V
625 kHz input voltage (peak-to-peak value)	$V_{15\text{-}8(p\text{-}p)}$	–	300	–	mV
D.C. input voltage (pin 15)	$V_{15\text{-}8}$	–	5	–	V
Input resistance (pin 15)	$R_{15\text{-}8}$	10	–	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Fixed oscillator					
Output resistance (pin 17)	$R_{17\text{-}8}$	–	–	30	Ω
Identification					
D.C. output voltage (SECAM)	$V_{1\text{-}8}$	9,3	–	–	V
Capacitor charge for reaction time of 300 ms at $V_{9\text{-}8}$ = 10 mV	$C_{2\text{-}8}$	0,1	–	2,0	μF
Chrominance input signal (pin 3)					
input voltage (peak-to-peak value)	$V_{3\text{-}8(p\text{-}p)}$	–	–	1,8	V
input resistance	$R_{3\text{-}8}$	12	–	–	kΩ
Chrominance input signal (pin 4)					
input voltage (peak-to-peak value)	$V_{4\text{-}8(p\text{-}p)}$	–	–	1,8	V
input resistance	$R_{4\text{-}8}$	12	–	–	kΩ
Horizontal identification at	$V_{6\text{-}8}$	8	–	–	V
Vertical identification with capacitor $C_{6\text{-}8}$ and a delay of	t_d	–	0,15	–	ms/nF
Burst gating pulse (pin 18)					
Voltage threshold level					
to activate stage	$V_{18\text{-}8}$	5	–	–	V
to de-activate stage	$V_{18\text{-}8}$	–	–	2,5	V
System timing (pin 7)					
Activate slope of the divider, negative going (derived at vertical pulse from pin 27 of TDA3701)					
Voltage of vertical pulse	$V_{7\text{-}8}$	5	–	8	V
Voltage threshold level					
to activate stage	$V_{7\text{-}8}$	–	–	2	V
to de-activate stage	$V_{7\text{-}8}$	2,5	–	3,5	V
Input resistance	$R_{7\text{-}8}$	30	–	–	kΩ

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION

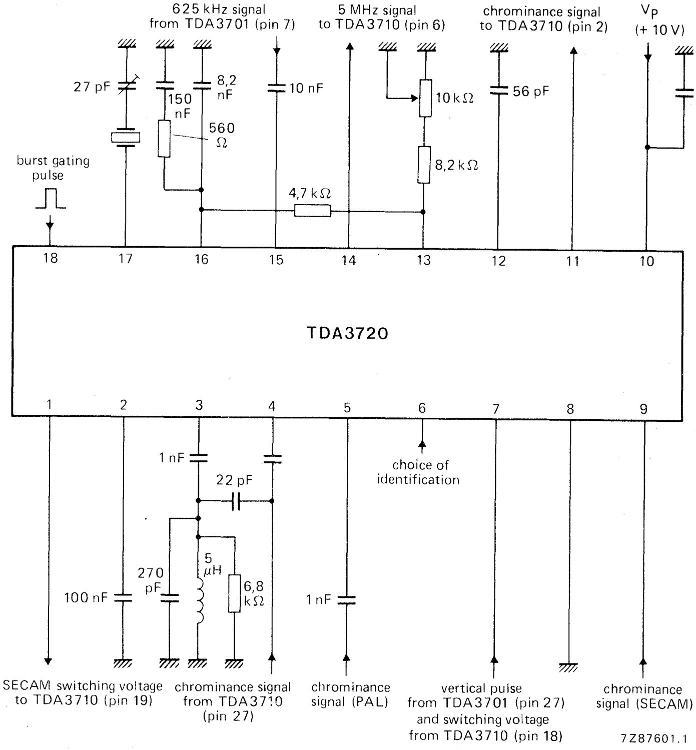


Fig. 2 Application diagram.

FREQUENCY DEMODULATOR AND DROP OUT COMPENSATOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3730 is a monolithic integrated circuit for luminance processing in the playback path of video recorders. The device incorporates two signal channels, one for the main signal and one for the drop out signal.

Features

- FM preamplifier
- Limiter in main and drop out channel
- Demodulator in main and drop out channel
- Drop out detector with Schmitt-trigger
- Electronic switches for FM and video signal controlled by drop out detector
- Linear and dynamic video de-emphasis
- D.C. reference stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 7 and pin 23)	$V_P = V_{7,\,23\text{-}5,\,25}$	typ.	10	V
Supply current (pin 7 + pin 23)	$I_P = I_7 + I_{23}$	typ.	35	mA
FM input signal (pin 17) (peak-to-peak value)	$V_{17\text{-}25(p\text{-}p)}$	typ.	100	mV
Video output signal (pin 26) (peak-to-peak value)	$V_{26\text{-}5(p\text{-}p)}$	typ.	2	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

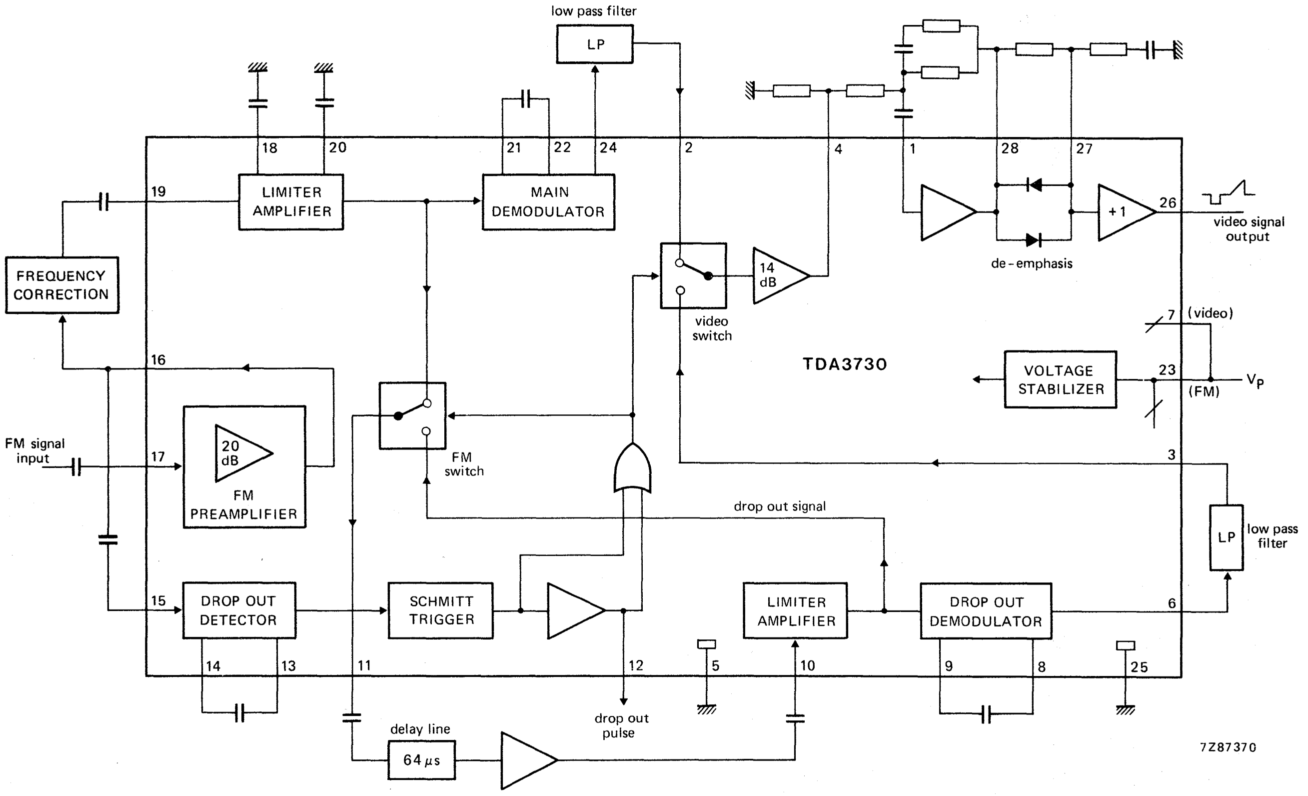


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7 and pin 23)	$V_P = V_{7, 23\text{-}5, 25}$	typ.	13,2	V
Voltage range at pins 1, 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 24, 26, 27, 28 to pin 5 and 25 (ground)	$V_{n\text{-}5, 25}$	0 to	V_P	V
Currents				
at pins 8, 9, 13, 14, 21, 22	$-I_n$	max.	3	mA
at pins 27 and 28	I_n	max.	1	mA
Total power dissipation	P_{tot}	max.	1,33	W
Storage temperature range	T_{stg}	−25 to	+150	°C
Operating ambient temperature range	T_{amb}	0 to	+70	°C

DEVELOPMENT SAMPLE DATA

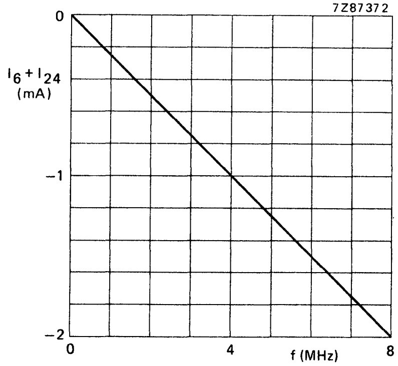


Fig. 2 Steepness of the main and drop out demodulator.

CHARACTERISTICS

$V_P = V_{7,\ 23\text{-}5,\ 25} = 10$ V; $T_{amb} = 25\ ^{\circ}C$; measured in test circuit Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7 and pin 23)					
Supply voltage	$V_P = V_{7,\ 23\text{-}5,\ 25}$	9,6	10	13,2	V
Supply current	$I_{P1} = I_7$	–	23	–	mA
	$I_{P2} = I_{23}$	–	12	–	mA
FM amplifier					
Input voltage (pin 17) (peak-to-peak value)	$V_{17\text{-}25(p\text{-}p)}$	–	100	–	mV
Input resistance	$R_{17\text{-}25}$	10	–	–	kΩ
Gain	G_v	–	20	–	dB
Bandwidth ($R_G \leqslant 50\ \Omega$)	b	–	12	–	MHz
Output signal amplitude (pin 16) (peak-to-peak value)	$V_{16\text{-}25(p\text{-}p)}$	–	–	1,3	V
Main limiter amplifier (pin 19)					
FM input signal (peak-to-peak value)	$V_{19\text{-}25(p\text{-}p)}$	–	0,5	1	V
Input resistance	$R_{19\text{-}25}$	–	600	–	Ω
Start of limiting (referred to pin 11) (peak-to-peak value)	$V_{19\text{-}25(p\text{-}p)}$	–	4	–	mV
Drop out limiter amplifier (pin 10)					
FM input signal (peak-to-peak value)	$V_{10\text{-}5(p\text{-}p)}$	–	–	0,8	V
Input resistance	$R_{10\text{-}5}$	–	1	–	kΩ
Start of limiting (referred to pin 11) (peak-to-peak value)	$V_{10\text{-}5(p\text{-}p)}$	–	25	–	mV
Main and drop out demodulators					
Range of output voltages (pin 6 and pin 24) (peak-to-peak value)	$V_{6,\ 24\text{-}5,\ 25(p\text{-}p)}$	–	–	3,5	V
Linearity (bandwidth = 1 to 6 MHz)		–	± 5	–	%
Steepness (see Fig. 2)	S	–	0,25	–	mA/MHz
FM switch (pin 11)					
Output amplitude (peak-to-peak value)	$V_{11\text{-}5(p\text{-}p)}$	–	0,5	–	V
D.C. output voltage	$V_{11\text{-}5}$	–	8,4	–	V

parameter	symbol	min.	typ.	max.	unit
Video switch (pin 4)					
Input voltage (pin 2 and pin 3) (peak-to-peak value)	$V_{2,\,3\text{-}5(p\text{-}p)}$	–	–	0,5	V
Input resistance (open base)	$R_{2,\,3\text{-}5}$	20	–	–	kΩ
Voltage gain	G_V	–	14	–	dB
D.C. output voltage at $V_{2,\,3\text{-}5} = 9{,}5$ V	$V_{4\text{-}5}$	–	5,4	–	V
De-emphasis amplifier (linear)					
Video output signal (pin 28) (peak-to-peak value)	$V_{28\text{-}5(p\text{-}p)}$	–	–	3	V
Gain-bandwidth product	G.b	30	–	–	MHz
D.C. output voltage	$V_{28\text{-}5}$	–	5	–	V
Dynamic de-emphasis					
Output signal (pin 26) (peak-to-peak value) at $V_{28\text{-}5(p\text{-}p)} = 1$ V; f = 1 MHz sine	$V_{26\text{-}5(p\text{-}p)}$	–	632	–	mV
D.C. output voltage	$V_{26\text{-}5}$	–	3,2	–	V
Output current (emitter follower)	$-I_{26}$	–	–	3	mA
Drop out detector and Schmitt-trigger					
Input voltage for lower drop out threshold (pin 15) (peak-to-peak value)	$V_{15\text{-}5(p\text{-}p)}$	–	110	–	mV
Hysteresis of the Schmitt-trigger	V/V	–	1,5	–	dB
Input resistance	$R_{15\text{-}5}$	1,4	–	–	kΩ
Output voltage without drop out	$V_{12\text{-}5}$	–	–	2	V
Output voltage with drop out	$V_{12\text{-}5}$	5	–	–	V
OR-gate (internal)					
Switching voltage threshold (pin 12) for signal flow from pin 2 to pin 4	$V_{12\text{-}5}$	–	–	1,5	V
for signal flow from pin 3 to pin 4	$V_{12\text{-}5}$	3	–	–	V

APPLICATION INFORMATION

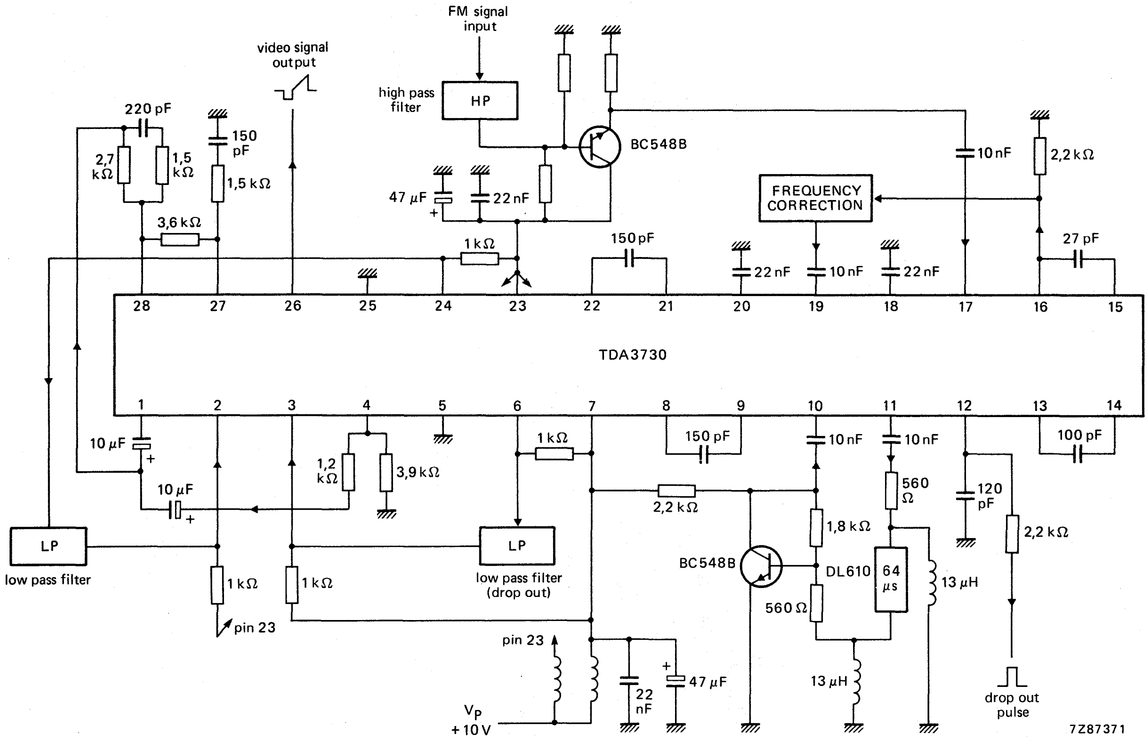


Fig. 3 Application diagram; also used as test circuit.

VIDEO PROCESSOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3771 is a monolithic integrated circuit for video signal processing in video recorders. It incorporates the following features:

Features

- 3 channel input selector
- 4 dB preamplifier
- A.G.C. amplifier:
  during record: controlled to sync pulse level and peak white level
  during playback: controlled to sync pulse level
- Gated clamping control stage
- Regeneration of the sync pulse
- Adder stage for the luminance signal (with reinserted sync pulse) and chrominance signal
- Emitter follower output stage for the luminance signal (composite video)
- Two emitter follower output stages for the composite colour video signal.

QUICK REFERENCE DATA

Supply voltage (pin 14)	$V_P = V_{14-11}$	typ.	12	V
Supply current (pin 14)	$I_P = I_{14}$	typ.	60	mA
Preamplifier				
Composite colour video input signals (peak-to-peak value)	$V_{2,3,4-11(p-p)}$	typ.	1	V
Gain	$G_{18-2,3,4}$	typ.	4	dB
A.G.C. amplifier				
Composite video signal (peak-to-peak value)	$V_{12-11(p-p)}$	typ.	0,4 V ± 6	dB
Composite video output signal (controlled) (peak-to-peak value)	$V_{6-11(p-p)}$	typ.	4	V
Adder stage				
Chrominance input voltage (peak-to-peak value)	$V_{16-11(p-p)}$	typ.	0,3	V
Gain	$G_{15,17-16}$	typ.	12	dB
Composite colour video output signals (peak-to-peak value)				
negative going	$V_{15-11(p-p)}$	typ.	2	V
positive going	$V_{17-11(p-p)}$	typ.	2	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

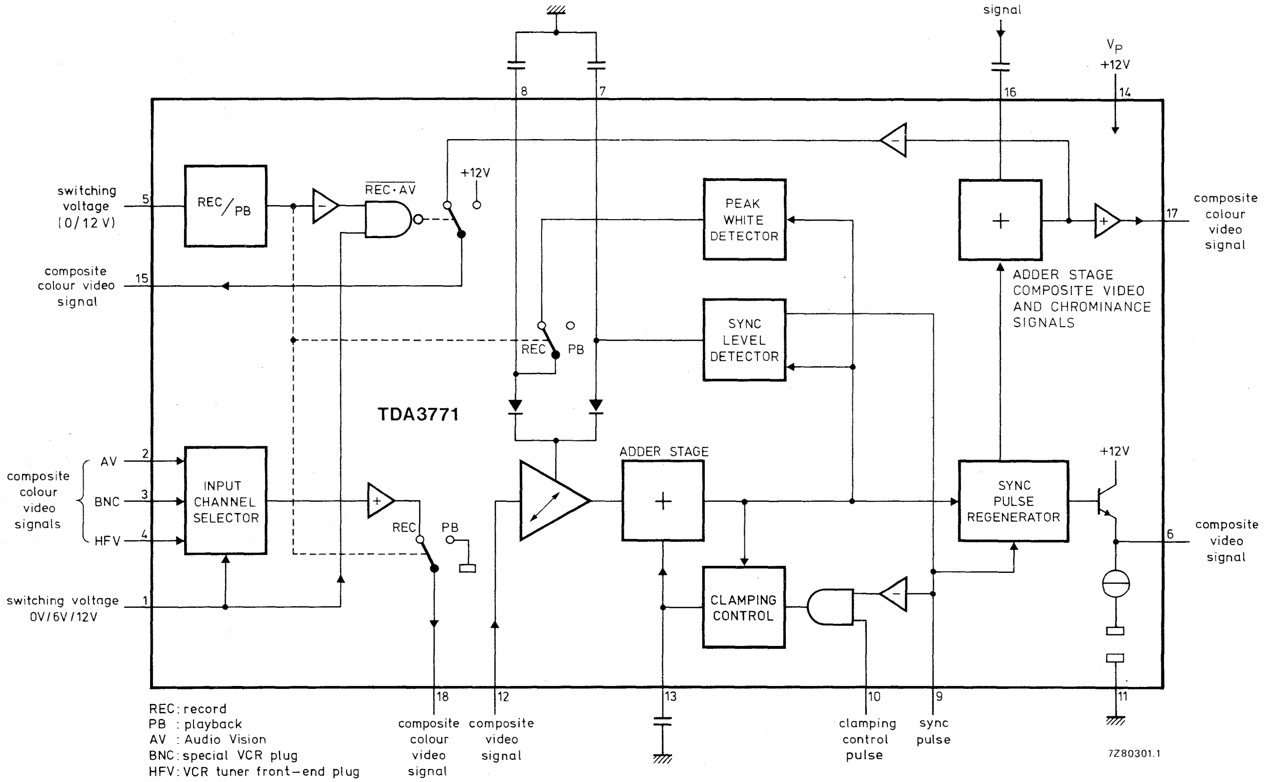


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 14)	$V_P = V_{14\text{-}11}$		0 to 13,2	V
Voltage range at pins 1, 5, 9, 10, 12, 16 to pin 11 (ground)	$V_{n\text{-}11}$		0 to V_P	V
Voltage ranges				
at pins 2, 3, 4	$V_{2,3,4\text{-}11}$		0 to 0,8V_P	V
at pins 7, 8	$V_{7,8\text{-}11}$		0,7V_P to V_P	V
at pin 13	$V_{13\text{-}11}$		0,25V_P to V_P	V
Currents				
at pins 6, 15, 17	$I_{6,15,17}$	max.	10	mA
at pin 18	I_{18}	max.	20	mA
Total power dissipation	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS

$V_P = V_{14\text{-}11} = 12$ V; trigger pulse on pin 10 with a width of 4 μs; $T_{amb} = 25$ °C; measured in test circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 14)					
Supply voltage	$V_P = V_{14\text{-}11}$	9,6	–	13,2	V
Supply current	$I_P = I_{14}$	–	60	–	mA
Input channel selector					
Input resistance	$R_{1\text{-}11}$	–	7,5	–	kΩ
Internal bias voltage	$V_{1\text{-}11}$	–	6	–	V
Selector switching voltages on pin 1-11					
to select input pin 4	$V_{1\text{-}11}$	–	–	2	V
to select input pin 3	$V_{1\text{-}11}$	4	–	8	V
to select input pin 2	$V_{1\text{-}11}$	10	–	–	V
Preamplifier					
Composite colour video input signals (peak-to-peak value)	$V_{2,3,4\text{-}11(p\text{-}p)}$	–	2	–	V
Input resistance	$R_{2,3,4\text{-}11}$	–	10	–	kΩ
Input capacitance	$C_{2,3,4\text{-}11}$	–	10	–	pF
Gain	$G_{18\text{-}2,3,4}$	–	4	–	dB
D.C. output voltage					
during record	$V_{18\text{-}11}$	–	–	5,8	V
during playback	$V_{18\text{-}11}$	–	1	–	V
Frequency response (0 to 3 MHz)	$\alpha_{18\text{-}2,3,4}$	–	–	1	dB
Signal suppression at output (pin 18)					
with no input selected	α_{18}	43	–	–	dB
during playback	α_{18}	50	–	–	dB
A.G.C. amplifier					
Input voltage (composite video signal) (peak-to-peak value)	$V_{12\text{-}11(p\text{-}p)}$	–	0,4 ± 6 dB	–	V
Input resistance	$R_{12\text{-}11}$	–	10	–	kΩ
Input capacitance	$C_{12\text{-}11}$	–	10	–	pF
Frequency response (0 to 3 MHz)	$\alpha_{15,17\text{-}12}$	–	1	–	dB
Peak-white and sync-pulse level detectors					
Capacitor currents					
charging current on pin 8	$-I_8$	–	15	–	mA
discharging current on pin 8	I_8	–	0,8	–	μA
charging current on pin 7	$-I_7$	–	0,3	–	mA
discharging current on pin 7	I_7	–	0,3	–	mA

parameter	symbol	min.	typ.	max.	unit
Gated clamping control and sync pulse regeneration					
Threshold voltage for clamping control ON $V_{9\text{-}11} = 0$ V	$V_{10\text{-}11}$	7	–	–	V
Input current	$-I_{10}$	–	–	50	μA
Threshold voltage for active sync pulse generation and clamping control OFF	$V_{9\text{-}11}$	6	–	–	V
Input current	$-I_9$	–	–	50	μA
Charging current	$-I_{13}$	–	0,3	–	mA
Discharging current	I_{13}	–	0,3	–	mA
Black level voltage	$V_{6\text{-}11}$	–	5,5	–	V
Sync pulse cut-off level	$V_{6\text{-}11}$	–	5,2	–	V
Controlled output signal (peak-to-peak value)	$V_{6\text{-}11(p\text{-}p)}$	–	4,0	–	V
Record/playback selector					
Input voltage					
for playback	$V_{5\text{-}11}$	7	–	–	V
for record	$V_{5\text{-}11}$	–	–	5	V
Input current	$-I_5$	–	–	50	μA
Chrominance signal adder and output stage					
Input voltage (peak-to-peak value)	$V_{16\text{-}11(p\text{-}p)}$	–	0,3	–	V
Gain	$G_{15,17\text{-}16}$	–	12	–	dB
Input resistance	$R_{16\text{-}11}$	–	10	–	kΩ
Input capacitance	$C_{16\text{-}11}$	–	10	–	pF
Output signal (peak-to-peak values)					
composite colour video signal: negative	$V_{15\text{-}11(p\text{-}p)}$	–	2	–	V
composite colour video signal: positive	$V_{17\text{-}11(p\text{-}p)}$	–	2	–	V
2nd harmonic suppression	α_{17}	40	–	–	dB
Black level					
composite colour video signal: negative	$V_{15\text{-}11}$	–	9,3	–	V
composite colour video signal: positive	$V_{17\text{-}11}$	–	3,7	–	V
Signal suppression during record and with input pin 2 selected	α_{15}	40	–	–	dB
D.C. voltage during record and with input pin 2 selected	$V_{15\text{-}11}$	–	12	–	V
Output resistance during record and with input pin 2 selected	$R_{15\text{-}11}$	–	30	–	kΩ

APPLICATION INFORMATION

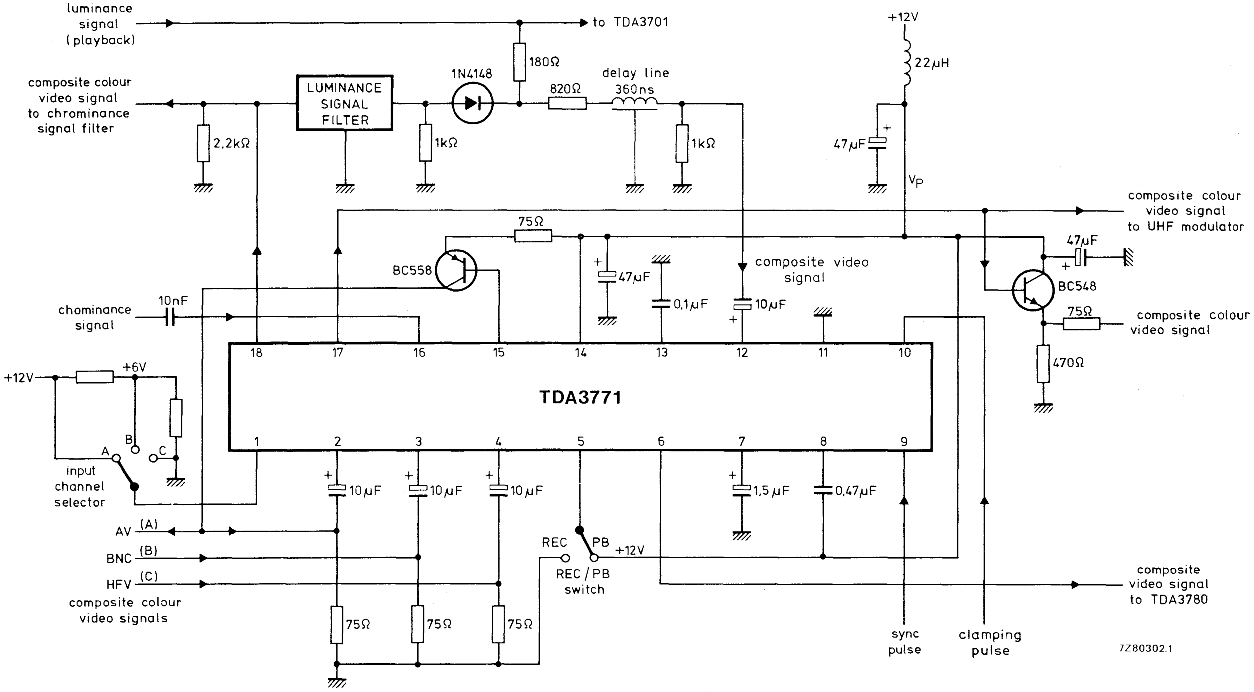


Fig. 2 Application diagram; also used as test circuit.

FREQUENCY MODULATOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3780 is a monolithic integrated circuit for frequency modulation in video recorders.

Features

- Voltage clamping control stage
- Two-stage amplification of the luminance signal with dynamic (adjustable) and linear pre-emphasis
- Adjustable white limiter
- Voltage controlled oscillator (VCO)
- Limiting stage with facility to disconnect from output stage
- Blanking pulse for VCO and output stage

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_P = V_{1\text{-}18}$	typ.	12	V
Supply current (pin 1)	$I_P = I_1$	typ.	52	mA
Clamping stage and pre-emphasis (dynamic) **amplifier**				
Luminance input signal (pin 2) (peak-to-peak value)	$V_{2\text{-}18(p\text{-}p)}$	typ.	2,0	V
Output voltage (pin 4)	$V_{4\text{-}18}$		2,5 to 8,0	V
Pre-emphasis (linear) **amplifier stage**				
Output voltage (pin 7)	$V_{7\text{-}18}$		2,5 to 8,0	V
Oscillator				
Output frequency	f_{osc}	typ.	3,3	MHz
Output stage				
D.C. output voltage	$V_{17\text{-}18}$	typ.	6,0	V
FM signal output voltage (peak-to-peak value)	$V_{17\text{-}18(p\text{-}p)}$	typ.	4,2	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

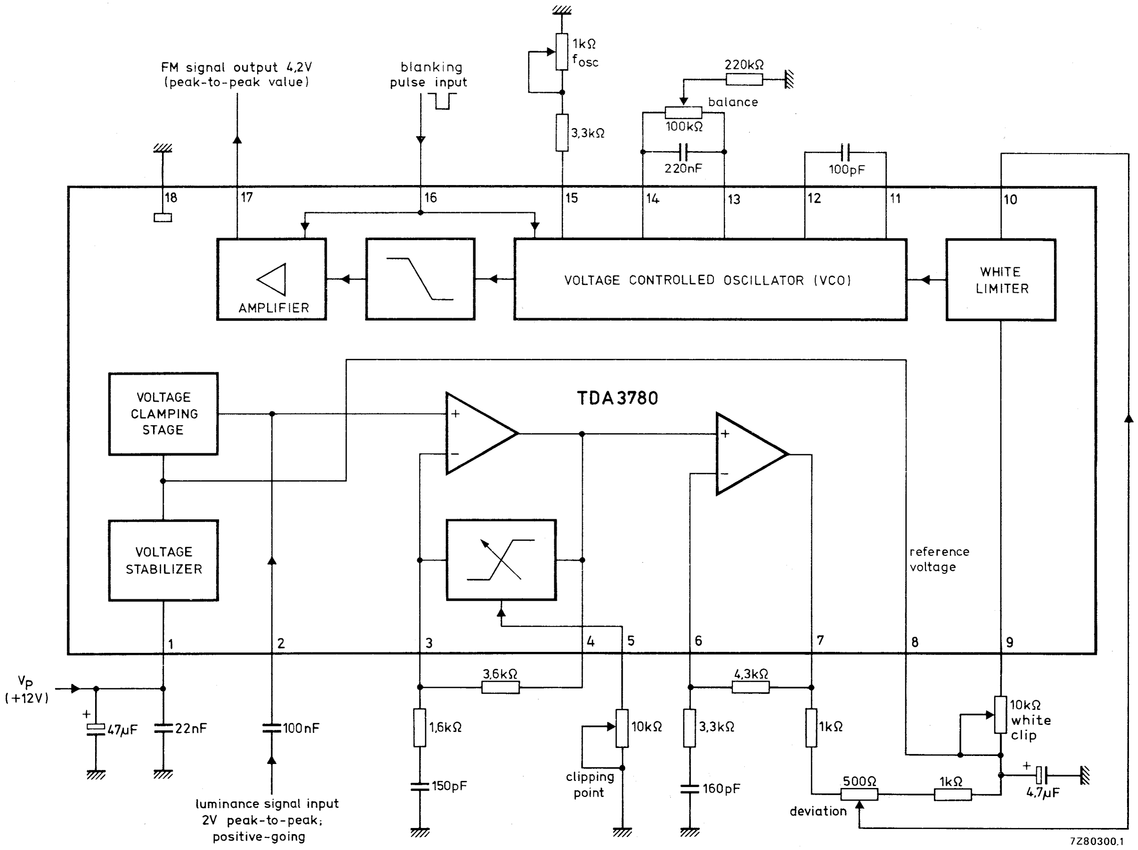


Fig. 1 Block diagram.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1\text{-}18}$	max.	13,2	V
Voltage range at pins 2, 3, 4, 5, 6, 7, 9, 10, 13, 14, 15, 16, 17 to pin 18 (ground)	$V_{n\text{-}18}$		0 to V_P	V
Voltage at pin 8	$V_{8\text{-}18}$	max.	10	V
Currents at pins 11 and 12	$\pm I_{11,12}$	max.	5	mA
Total power dissipation	P_{tot}	max.	920	mW
Storage temperature range	T_{stg}		–25 to + 150	$^{\circ}$C
Operating ambient temperature range	T_{amb}		0 to + 70	$^{\circ}$C

CHARACTERISTICS

$V_P = V_{1\text{-}18} = 12$ V; balancing the 2nd harmonic to the minimum level; $T_{amb} = 25\ ^{\circ}$C; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	$V_P = V_{1\text{-}18}$	9,6	12	13,2	V
Supply current	$I_P = I_1$	–	52	–	mA
Reference voltage	$V_{8\text{-}18}$	–	4	–	V
Clamping stage and pre-emphasis (dynamic) **amplifier**					
Luminance input signal (pin 2) (peak-to-peak value)	$V_{2\text{-}18(p\text{-}p)}$	–	2	–	V
Input impedance at $V_{2\text{-}18} < V_{8\text{-}18}$; $-I_2 = 1$ mA	$\lvert Z_{2\text{-}18}\rvert$	–	25	–	Ω
Input current at $V_{2\text{-}18} > V_{8\text{-}18}$	I_2	–	2	–	µA
Input bias current	I_3	–	1	–	µA
Clamping voltage for the input signal clamped at top sync	$V_{2\text{-}18}$	–	4	–	V
Gain-bandwidth product		30	–	–	MHz
Output voltage (pin 4)	$V_{4\text{-}18}$	2,5	–	8	V
Start of gain reduction (adjustable at pin 5)	$V_{4\text{-}3}$	100	–	–	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Pre-emphasis (linear) **amplifier**					
Input bias current	I_6	–	–	1	μA
Gain-bandwidth product		30	–	–	MHz
Output voltage (pin 7)	$V_{7\text{-}18}$	2,5	–	8	V
White limiter (pin 10)					
Limitation					
at $I_9 = 0$	$V_{10\text{-}18}$	7,5	–	–	V
at $I_9 = 0{,}5$ mA	$V_{10\text{-}18}$	–	4	–	V
Voltage controlled oscillator (VCO)					
Output frequency with $C_{osc} = 100$ pF (pin 11-12); $R_{osc} = 3{,}8$ kΩ (pin 15)	f_{osc}	3,04	3,30	3,56	MHz
Oscillator steepness	$f_{osc}/\Delta V_{10\text{-}18}$	–	1,5	–	MHz/V
FM output signal switching stage					
Input voltage to switch FM off	$V_{16\text{-}18}$	–	–	4	V
Input voltage to switch FM on	$V_{16\text{-}18}$	6	–	–	V
Output voltage suppression with FM switched off	α_o	50	–	–	dB
Output stage (pin 17)					
D.C. output voltage	$V_{17\text{-}18}$	–	6	–	V
FM signal output voltage (peak-to-peak value)	$V_{17\text{-}18(p\text{-}p)}$	–	4,2	–	V
Suppression of the 2nd harmonic $\frac{\text{V (1st harmonic)}}{\text{V (2nd harmonic)}}$	α_{harm}	40	–	–	dB
AM suppression	α_{AM}	40	–	–	dB
Crosstalk between output and input	$\frac{V_{17\text{-}18}}{V_{2\text{-}18}}$	40	–	–	dB

BAND SELECTOR AND WINDOW DETECTOR

GENERAL DESCRIPTION

The TDA3791 is a monolithic integrated circuit intended for application in search-tuning systems for video recorders. It is designed to select one out of four tuners, each representing a particular band. Band selection tuning is indicated by a variable voltage V_{AFC}.

Features

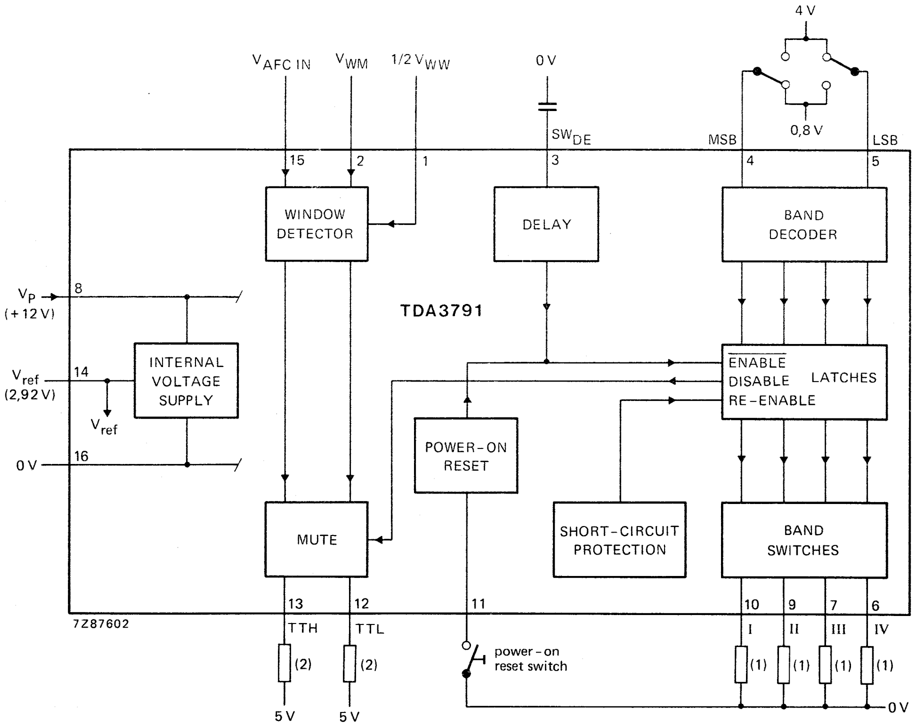
- Voltage window detector
- Band switch selector
- 4 short-circuit protected band switches
- Muting circuit
- Delay circuit
- Short-circuit protection circuit
- Power-on reset

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	12	V
Supply current (pin 8)	$I_P = I_8$			
unloaded band switches ON		typ.	25	mA
all band switches OFF		typ.	12	mA
Power dissipation	P_{tot}	max.	1,8	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Operating ambient temperature range	T_{amb}	0 to	70	°C

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT-38WE-2).



(1) $R = \frac{10\ \text{V}}{30\ \text{mA}}$. (2) $R = \frac{5\ \text{V}}{2\ \text{mA}}$.

Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Voltage window detector (see Table 1)

The voltage window is dependent upon two inputs; V_{WM} (pin 2) and $1/2V_{WW}$ (pin 1), which represent the centre of the window and the (window width)/2 respectively.

The voltage window range is from $V_{WM} - 1/2V_{WW}$ to $V_{WM} + 1/2V_{WW}$. A variable input voltage $V_{AFC\ IN}$ (pin 15) is compared with these window edges.

Table 1 Truth table; window detector

inputs	outputs	
$V_{AFC\ IN} = V_{15\text{-}16}$; $V_{WM} = V_{2\text{-}16}$; $V_{WW} = V_{1\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
$V_{AFC\ IN} < V_{WM} - 1/2V_{WW}$	HIGH	LOW
$V_{WM} - 1/2V_{WW} < V_{AFC\ IN} < V_{WM} + 1/2V_{WW}$	HIGH	HIGH
$V_{AFC\ IN} > V_{WM} + 1/2V_{WW}$	LOW	HIGH

Where: $V_{12\text{-}16}$ = tuning too low (TTL); $V_{13\text{-}16}$ = tuning too high (TTH).

During transitions of the outputs ($V_{12\text{-}16}$ and $V_{13\text{-}16}$), a hysteresis value of approximately 20 mV is applied at the window edges.

Band-switch selector (see Table 2)

Selection of the band switches is determined by the input voltage levels of MSB (pin 4) and LSB (pin 5).

- If MSB or LSB > 4 V, the input is HIGH
- If MSB or LSB < 0,8 V, the input is LOW.

The band switches are selected as confirmed by Table 2.

Table 2 Truth table; band switch selector

MSB ($V_{4\text{-}16}$)	LSB ($V_{5\text{-}16}$)	switch	HIGH output
HIGH	HIGH	I	$V_{10\text{-}16}$
HIGH	LOW	II	$V_{9\text{-}16}$
LOW	HIGH	III	$V_{7\text{-}16}$
LOW	LOW	IV	$V_{6\text{-}16}$

Short-circuit protected band switches

A selected band switch has a minimum output voltage of $V_P - 0{,}3$ V provided the current is not more than 30 mA (I_{10}, I_9, I_7, I_6). If the output voltage at pins 10, 9, 7 or 6 is less than 9 V a short-circuit condition exists, and the output current will not be more than 70 mA. In this event the band switch is switched off, after an externally determined delay.

Muting

The muting circuit is active when a selected band switch is switched off. Both outputs TTL (pin 12) and TTH (pin 13) will then be LOW.

DEVELOPMENT SAMPLE DATA

FUNCTIONAL DESCRIPTION (continued)

Delay circuit

After selection of a band switch, it will be in a conducting state. If after selection and a delay, the output voltage has not reached 9 V, the band is switched off. This delay is determined by an external capacitor on output SW_{DE} (pin 3).

Short-circuit protection

The short-circuit protection of each switch is provided by a flip-flop. If the condition of a band switch $V_o < 9$ V is detected, its flip-flop will be set and the band switch is switched off.

In the event of an incidental short-circuit to a band switch output, the band switch can be reset by applying 0 V to the power-on reset input (pin 11) or 0 V to the switch delay output SW_{DE} (pin 3).

Power-on reset

Before the voltage supply reaches 9,6 V, the short-circuit protection flip-flops are reset to enable the selection of a band switch.

The power-on reset circuit also supplies the voltage level for short-circuit detection.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13,2 V
Total power dissipation	P_{tot}	see Fig. 2	
Storage temperature range	T_{stg}	−65 to +150 °C	
Operating ambient temperature range	T_{amb}	0 to +70 °C	

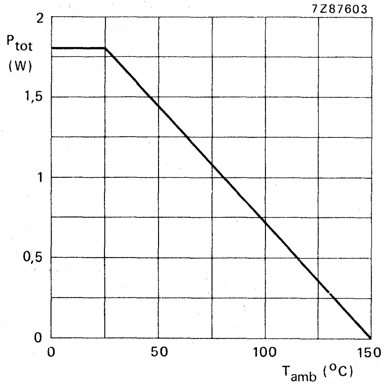


Fig. 2 Power derating curve.

CHARACTERISTICS

$V_P = V_{8\text{-}16} = 12$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	10	12	13,2	V
Supply current (pin 8)					
unloaded band switches ON	$I_P = I_8$	18	25	33	mA
all band switches OFF	$I_P = I_8$	9	12	16	mA
Voltage range					
$1/2V_{WW}$ (pin 1)	$V_{1\text{-}16}$	0,1	–	4,5	V
V_{WM} (pin 2)	$V_{2\text{-}16}$	1,8	–	10,5	V
$V_{WM} + 1/2V_{WW}$ at $V_{8\text{-}16} - 1,4$ V	$V_{2\text{-}16} \pm V_{1\text{-}16}$	1,7	–	10,6	V
$V_{AFC\ IN}$ (pin 15)	$V_{15\text{-}16}$	0,5	–	11,5	V
Input current					
$1/2V_{WW}$ (pin 1)	$-I_1$	–	–	2	μA
V_{WM} (pin 2)	I_2	–	–	0,2	μA
$V_{AFC\ IN}$ (pin 15)	I_{15}	–	0,2	0,4	μA
Hysteresis voltage V_{AFC}*	$\Delta V_{15\text{-}16}$	–	20	50	mV
Delta current at $V_{AFC\ IN}$*	ΔI_{15}	–	–	25	nA
Temperature coefficient $I_{AFC\ IN}$	$TC(I_{15})$	–	–0,42	–	nA/°C
Temperature coefficient I_{WM}	$TC(I_2)$	–	–0,27	–	nA/°C
Deviation of applied voltage (pin 1)					
at $V_{1\text{-}16} = 100$ mV	$\Delta V_{1\text{-}16}$	–35	–	+35	mV
at $V_{1\text{-}16} = 4,6$ V	$\Delta V_{1\text{-}16}$	–180	–	+180	mV
Input current (pin 4)					
at MSB < 0,8 V	I_4	–	–	0,1	μA
at MSB > 4 V	I_4	–	–	1,0	μA
Input current (pin 5)					
at LSB > 4 V	I_5	–	–	1,0	μA
at LSB < 0,8 V	I_5	–	–	0,1	μA
Voltage level (pin 4)					
at MSB HIGH	$V_{4\text{-}16}$	4	–	–	V
at MSB LOW	$V_{4\text{-}16}$	–	–	0,8	V
Voltage level (pin 5)					
at LSB HIGH	$V_{5\text{-}16}$	4	–	–	V
at LSB LOW	$V_{5\text{-}16}$	–	–	0,8	V
Short-circuit current of band switches I, II, III, IV (pins 10, 9, 7, 6)	$-I_{10, 9, 7, 6}$	33	50	75	mA
Voltage drop of band switches I, II, III, IV (pins 10, 9, 7, 6) at $I_{o(max)} = 30$ mA; $V_P = 10$ V	$V_{10, 9, 7, 6\text{-}16}$	–	–	0,3	V

* During switching of outputs $V_{12\text{-}16}$ and/or $V_{13\text{-}16}$.

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Voltage level short-circuit detection at $0{,}75V_P$	$V_{10, 9, 7, 6\text{-}16}$	8,5	9,0	9,5	V
Output voltage (pin 13) TTH at $I_{13} = 2$ mA (LOW)	$V_{13\text{-}16}$	–	–	0,3	V
Output voltage (pin 12) TTL at $I_{12} = 2$ mA (LOW)	$V_{12\text{-}16}$	–	–	0,3	V
Leakage current (pin 13) TTH at $V_{13\text{-}16} = 13{,}2$ V	I_{13}	–	–	10	μA
Leakage current (pin 12) TTH at $V_{12\text{-}16} = 13{,}2$ V	I_{12}	–	–	10	μA
Output current (pin 3) SW_{DE} at $V_{3\text{-}16} = 6$ V	$-I_3$	5	12	20	μA
Maximum value of delay capacitor	C_3	–	–	40	nF
Maximum delay time at $\pm\ C_3\ (nF)/(I_3/10)$ ms	t_d	–	–	50	ms
Power-on-reset voltage	$V_{8\text{-}16}$	6	–	9,6	V
Leakage current unswitched band switches at $V_{10, 9, 7, 6\text{-}16} = -12$ V	$I_{10, 9, 7, 6}$	–	–	2	μA

STEREO/DUAL TV SOUND PROCESSING CIRCUITS

GENERAL DESCRIPTION

The TDA3800G; GS are stereo/dual TV sound decoder circuits for processing an a.f. and a sound i.f. signal in TV and VCR equipment, using active filters in selective frequency processing.

In deviation of our standard terms and conditions of sale the supply of the TDA3800 (ABS) does not imply any patent indemnity whatsoever with respect to the stereo-tone patent rights of I.G.R. Germany.

Features

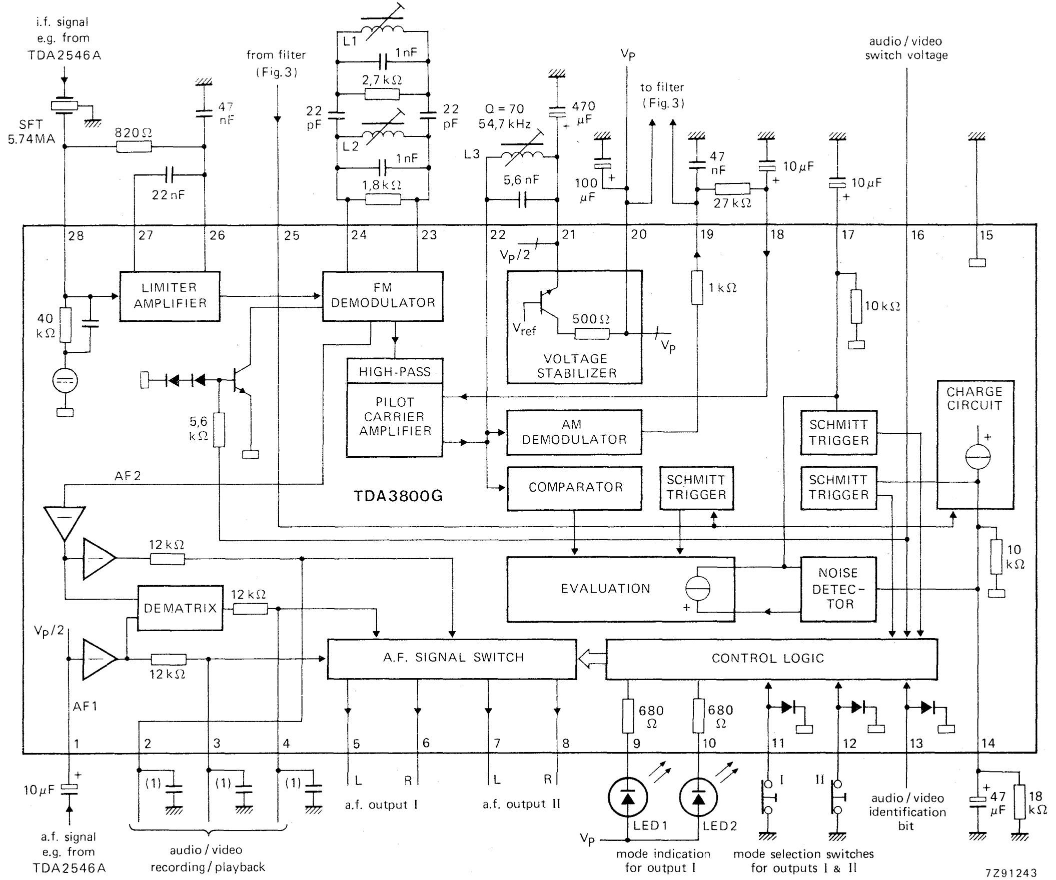
- Signal processing of one a.f. signal and one i.f. signal
- 2nd i.f. limiter/amplifier and FM demodulator (5,742 MHz) for the second sound channel
- Pilot carrier processing with digital identification, hysteresis and short switching times
- De-matrixing of the signals for the two audio channels
- De-emphasis
- Two dual channel, independently controllable a.f. outputs
- Low-resistance a.f. outputs (short-circuit protected); can be used for headphone
- Standardized switched output for controlling external audio/video equipment
- Signal path control by an identification bit (also in audio/video mode)
- LED indication of selected mode (also in audio/video mode)
- Possibility to apply a.f. signals from external equipment via the de-emphasis inputs (audio/video mode)
- Mode selection of stereo/mono or sound I/sound II
  TDA3800G dynamic selection with internal storage
  TDA3800GS static selection

QUICK REFERENCE DATA

Supply voltage (pin 20)	$V_P = V_{20\text{-}15}$	typ.	12	V
2nd sound i.f. input voltage for start of limiting (r.m.s. value)	$V_{i(rms)}$	typ.	50	μV
Pilot carrier amplifier control range	ΔG_v	min.	20	dB
A.F. input voltage (r.m.s. value)	$V_{i(rms)}$	typ.	1	V
A.F. demodulator output voltage (r.m.s. value)	$V_{o(rms)}$	typ.	0,6	V
LED output current	I_{LED}	typ.	15	mA
Signal-to-noise ratio of the a.f. signal switches	S/N	typ.	80	dB
Crosstalk in stereo mode	α_S	min.	40	dB
Crosstalk in dual sound mode	α_{DS}	min.	60	dB

PACKAGE OUTLINES

28-lead DIL; plastic (SOT-117).



(1) De-emphasis 3,9 nF.

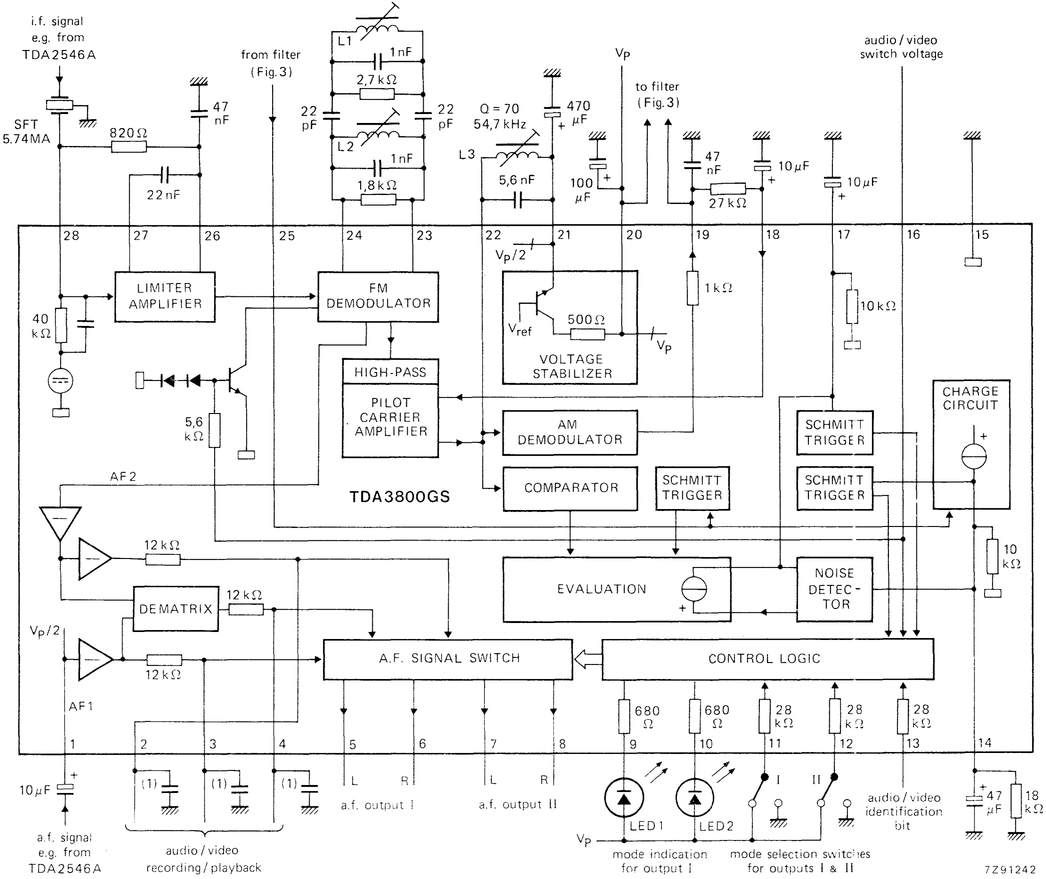
(2) TDA3800G application using active filters.

Coil data

L1 and L2: TOKO 7 k;
Q = 25, f_o = 5,74 MHz.

Fig. 1 TDA3800G block diagram and test circuit in accordance with Fig. 3.

DEVELOPMENT SAMPLE DATA



(1) De-emphasis 3,9 nF.
(2) TDA3800GS application
using active filters.

Coil data

L1 and L2: TOKO 7 k;
Q = 25, f_0 = 5,74 MHz.

Fig. 2 TDA3800GS block diagram and test circuit in accordance with Fig. 3.

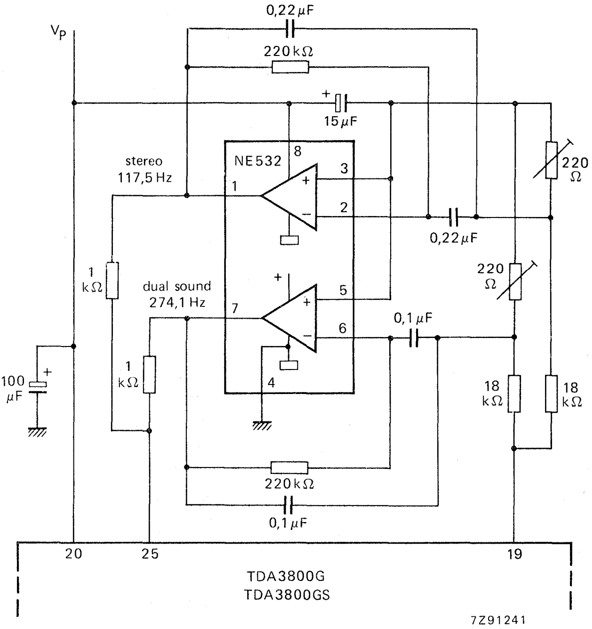


Fig. 3 External filter circuit for the identification frequencies 117,5 Hz and 247,1 Hz.

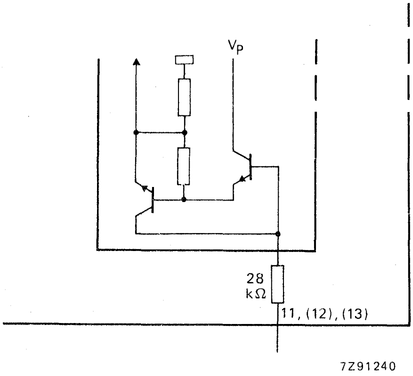


Fig. 4 TDA3800GS internal circuit for the control input leads 11, 12 and 13.

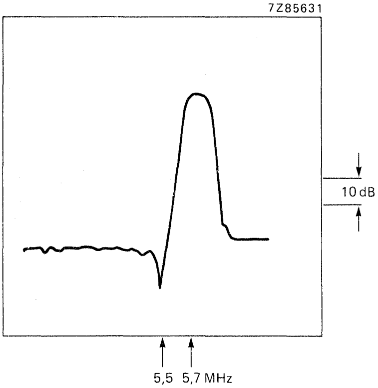


Fig. 5 IF2 filter selection.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 20)	$V_P = V_{20\text{-}15}$	max.	14	V
Voltage				
at pins 1; 9; 10; 16 and 25	$V_{n\text{-}15}$	max.	V_P	
at pins 11; 12 and 13*	$V_{11;12;13\text{-}15}$	max.	V_P	
Current				
at pins 11; 12 and 13**	$I_{11;12;13}$	max.	1	mA
at pin 21	short-circuit protected			
Total power dissipation	P_{tot}	max.	1,5	W
Storage temperature range	T_{stg}	−25 to +150		°C
Operating ambient temperature range	T_{amb}	0 to +70		°C

* TDA3800GS only.
** TDA3800G only.

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 1/Fig. 2 with a 1 kHz signal. $V_{1\text{-}15(rms)}$ = 0,5 V, an i.f. signal $V_{28\text{-}15(rms)}$ = 5 mV (VC/2SC = 20 dB, Δf = ± 50 kHz, f_m = 400 Hz) and with adjusted de-matrix circuit; i.f. filter selection at input pin 28 as in Fig. 5; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 20)					
Supply voltage range	$V_P = V_{20\text{-}15}$	10,8	12	13,2	V
Supply current (without LED current; mono)	$I_P = I_{20}$	40	–	87	mA
FM limiter/amplifier and demodulator					
Start of limiting	$V_{28\text{-}15(rms)}$	–	–	60	μV
Input resistance	$R_{28\text{-}15}$	–	40	–	kΩ
Input capacitance (Fig. 5)	$C_{28\text{-}15}$	–	4,5	–	pF
AM suppression at V_i = 0,5 mV; Δf = ± 30 kHz	α_{AMS}	50	–	–	dB
Pilot carrier processing					
D.C. input voltage	$V_{18\text{-}15}$	–	7,2	–	V
D.C. voltage (reference via tuning coil)	$V_{22\text{-}15}$	–	6,0	–	V
AM demodulator output voltage	$V_{19\text{-}15}$	–	7,3	–	V
Controlled pilot carrier output voltage (peak-to-peak value)	$V_{22\text{-}21(p\text{-}p)}$	–	250	–	mV
Output resistance	$R_{22\text{-}15}$	50	–	–	kΩ
Identification frequency evaluation					
No identification signal (lower threshold)	$V_{14\text{-}15}$	–	–	2	V
Identification signal (upper threshold)	$V_{14\text{-}15}$	4	–	–	V
Stereo transmission	$V_{17\text{-}15}$	–	–	2	V
Dual sound transmission	$V_{17\text{-}15}$	4	–	–	V
De-matrixing					
Output voltages	$V_{2;3;4\text{-}15}$	–	5,3	–	V
De-emphasis output resistances	$R_{2;3;4\text{-}15}$	–	12	–	kΩ
A.F. output signal of 2nd i.f. (r.m.s. value)	$V_{2\text{-}15(rms)}$	–	0,6	–	V
Attenuation of the demodulator output signal AF2 at audio/video mode	α_{AF2}	75	–	–	dB
Distortion of the AF2 signal $V_{o2\text{-}15}$	d_{tot}	–	0,4	–	%

parameter	symbol	min.	typ.	max.	unit
AF1 input					
D.C. input voltage	$V_{1\text{-}15}$	–	6	–	V
Input resistance	$R_{1\text{-}15}$	–	14	–	kΩ
Maximum input signal (r.m.s. value)	$V_{1\text{-}15(rms)}$	–	2	–	V
A.F. signal switches					
D.C. output voltages	$V_{5;6;7;8\text{-}15}$	–	5,3	–	V
Output resistances	$R_{5;6;7;8\text{-}15}$	–	200	–	Ω*
Maximum a.f. output signals (r.m.s. value)					
for $V_{AFI(rms)}$	$V_{5;6\text{-}15(rms)}$	–	2	–	V
for $V_{AFII(rms)}$	$V_{7;8\text{-}15(rms)}$	–	2	–	V
Total distortion when applying a signal at $V_{2;3;4\text{-}15(rms)} = 0{,}5$ V	d_{tot}	–	–	0,1	%
Signal plus noise-to-noise ratio	S + S/N	–	80	–	dB
Crosstalk attenuation					
in stereo mode (f = 1 kHz at pin 2)	α_S	40	–	–	dB
in dual sound mode (f = 20 Hz to 20 kHz)	α_{DS}	60	–	–	dB
Audio/video switch					
Audio/video switch voltage					
for playback (HIGH)	$V_{16\text{-}15}$	7	–	V_P	V
for recording (LOW)	$V_{16\text{-}15}$	0	–	2,5	V
Audio/video identification bit (TDA3800G)					
for stereo mode (LOW)	$V_{13\text{-}15}$	0	–	0,2	V
for dual sound mode (HIGH) at $V_{13\text{-}15} \approx 0{,}7$ V	I_{13}	–	0	–	mA
Audio/video switch voltage (TDA3800GS) (stereo/dual sound)					
for stereo mode (LOW)	$V_{13\text{-}15}$	–	–	0,8	V
for dual sound mode (HIGH)	$V_{13\text{-}15}$	2,4	–	–	V
Mode selection switches for outputs I and II					
Active LOW (TDA3800G)					
input voltage LOW	$V_{11;12\text{-}15}$	0	–	0,2	V
switch open condition at $V_{11;12\text{-}15} \approx 0{,}7$ V	$I_{11;12}$	–	0	–	mA
Pulse duration	t_p	1	–	–	μs

---

* Connection of high-impedance headphones is possible.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Switching voltage (TDA3800GS)					
Mono transmission both equals I and II mono					
Dual sound transmission switching voltage to pin 11 (pin 12 not affected)					
a.f. output II sound I and a.f. output I sound II	$V_{11\text{-}15}$	–	–	0,8	V
a.f. output I sound I and a.f. output II and II	$V_{11\text{-}15}$	2,4	–	–	V
Stereo transmission switching voltage to pin 12 (pin 11 not affected)					
a.f. outputs I and II mono	$V_{12\text{-}15}$	–	–	0,8	V
a.f. outputs I and II stereo	$V_{12\text{-}15}$	2,4	–	–	V
Mode indication (pins 9 and 10; see also Table 1)					
Only the mode for output I is indicated					
Maximum output current	$I_{9;10}$	–	15	–	mA
Voltage stabilizer (pin 21)					
Output voltage	$V_{21\text{-}15}$	–	6	–	V
Maximum d.c. output current short-circuit protected	$\pm I_{21}$	–	0,5	–	mA

Notes to the characteristics (TDA3800G only)

1. Serial commands for stereo/mono or sound I/sound II selection are determined by the identification bit of the transmission.
2. The pushbuttons at pins 11 and 12 are assigned to the a.f. outputs I and II respectively.
3. When a transmitter changes its identification from dual sound to stereo and then back to dual sound again, the last selected dual sound signal is available automatically because of the internal storage of the choice. This is also applicable for mono/stereo selection.
4. Power-on reset: when applying the supply voltage, the stereo or the AF1 signal appears at both outputs I and II depending on the type of transmission.

Table 1 Mode indication possibilities

LED 1	LED 2	selected reception mode
OFF	OFF	mono at mono or stereo transmission
ON	ON	stereo at stereo transmission
OFF	ON	AF1 signal at dual sound transmission
ON	OFF	AF2 signal at dual sound transmission

STEREO/DUAL TV SOUND PROCESSING CIRCUITS

GENERAL DESCRIPTION

The TDA3800S is a stereo/dual TV sound decoder circuit with static switching for processing two a.f. signals in TV and VCR equipment.

The TDA3800AS is applicable for active filters in selective frequency processing.

In deviation of our standard terms and conditions of sale the supply of the TDA3800 (ABS) does not imply any patent indemnity whatsoever with respect to the stero-tone patent rights of I.G.R. Germany.

Features

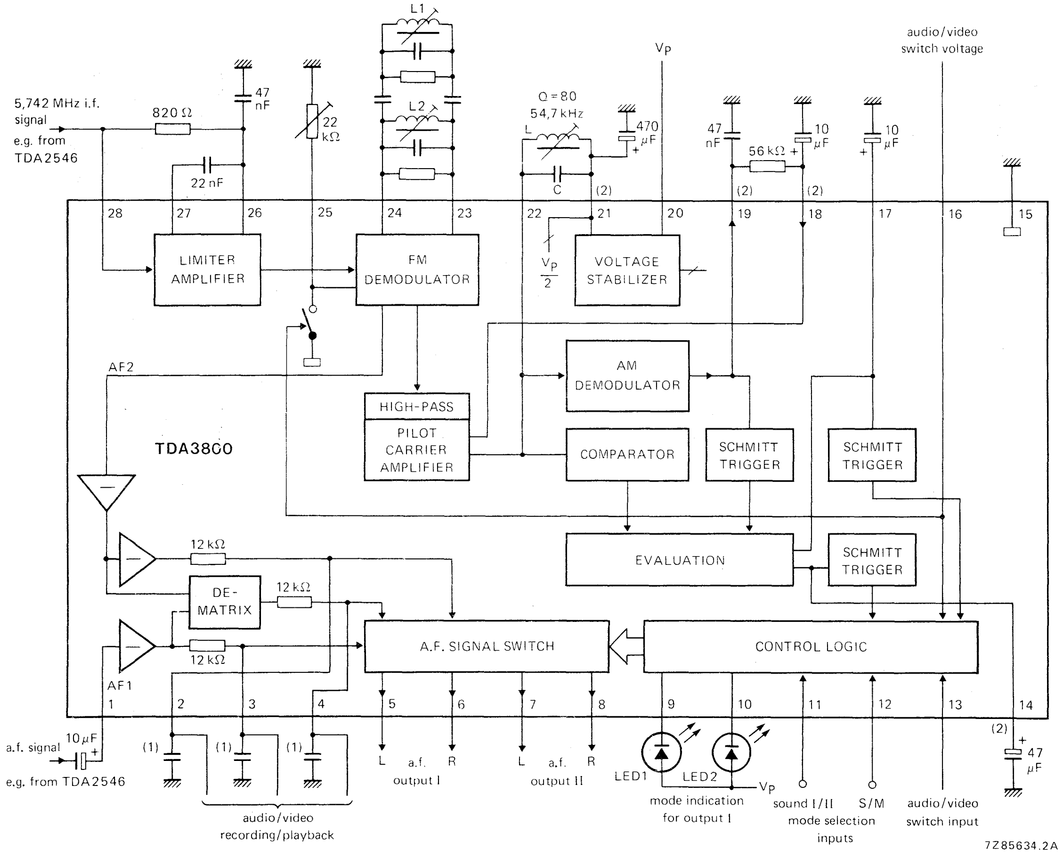
- 2nd i.f. limiter/amplifier and FM demodulator (5,742 MHz) for the second sound channel
- Level adjustment of the demodulated a.f. signal for channel matching
- Pilot carrier processing with digital identification, hysteresis and short switching times
- De-matrixing of the signals for the two audio channels
- De-emphasis
- Mode selection of stereo/mono or sound I (pin 12) and sound II (pin 11)
- Two dual channel a.f. outputs
- Low-resistance a.f. outputs (short-circuit protected); can be used for headphone
- Switched output for controlling external audio/video equipment
- Signal path control by an identification bit (also in audio/video mode)
- LED indication of selected mode (also in audio/video mode)
- Possibility to apply a.f. signals from external equipment via the de-emphasis inputs (audio/video mode)

QUICK REFERENCE DATA

Supply voltage (pin 20)	$V_P = V_{20\text{-}15}$	typ.	12 V
Supply current (pin 20)	$I_P = I_{20}$	typ.	53 mA
2nd sound i.f. input voltage for start of limiting (r.m.s. value)	$V_{i(rms)}$	typ.	50 μV
Pilot carrier amplifier control range	ΔG_v	>	20 dB
A.F. input signals; AF1 and AF2 (r.m.s. value)	$V_{i(rms)}$	typ.	1 V
LED output current	I_{LED}	typ.	15 mA
Signal-to-noise ratio of the a.f. signal switches	S/N	typ.	80 dB
Crosstalk in stereo mode	α_S	>	40 dB
Crosstalk in dual sound mode	α_{DS}	>	60 dB

PACKAGE OUTLINES

28-lead DIL; plastic (SOT-117).



(1) De-emphasis 4,7 nF.

(2) TDA3800AS application using active filters; see Fig. 2.

Fig. 1 TDA3800S block diagram and test circuit.

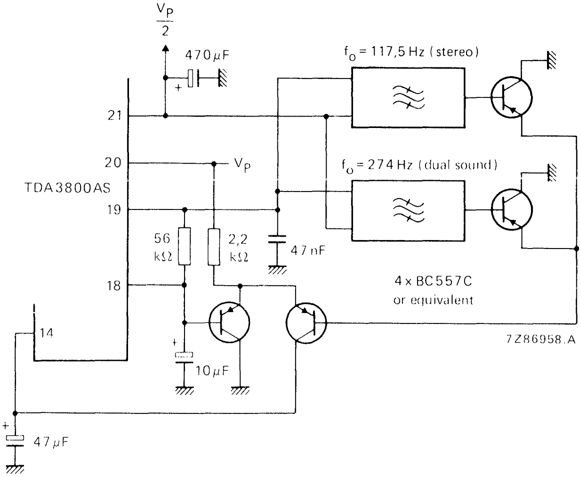


Fig. 2 Application using active filters in selective frequency processing with TDA3800AS.

FUNCTIONAL DESCRIPTION

The ICs provide two independent double/audio outputs with mode selection of stereo/mono or sound I/ sound II. Selection of output I is indicated by two LEDs.

The limiting amplifier and FM demodulator detects the 5,742 MHz i.f. for stereo/dual TV processing. The a.f. output of the demodulator is adjusted via pin 25.

A 54,687 kHz pilot carrier amplifier, AM demodulator and Schmitt-trigger identifies the 117,5 Hz stereo signal and the 274,1 Hz dual sound signal. AM modulation of the pilot-signal is eliminated by the comparator which produces a rectangular wave to drive the I^2 L frequency divider.

The I^2 L frequency divider comprises 8 flip-flops and in combination with an evaluation flip-flop provides a d.c. output for indication of the selected mode. An integrator and Schmitt-trigger with built-in hysteresis eliminates noise and interference on the stereo/dual sound switching signal.
An integrator and modified comparator followed by a Schmitt-trigger with built-in hysteresis eliminates noise and interference on the stereo/dual sound respective mono identification signal. The circuit automatically switches to mono when noise or interference dominates.

The I^2 L control logic circuit is driven by the stereo/dual sound switching signal, the identification/mono signal and the externally applied audio/video switching voltage at pin 16. Inputs at pins 11 and 12 provide mode selection for sound output I (pins 5 and 6) and sound output II (pins 7 and 8) respectively. Output control signals operate the audio switches and the LED-driver circuit.

A decoder circuit is fed with the AF2 audio signal from the FM demodulator and the AF1 audio signal externally applied via pin 1. The decoder output provides the stereo or dual sound signal for the audio switches and the de-emphasis at pins 2, 3 and 4 for audio/video recording/playback.

The audio switches provide two independent double stereo/dual sound outputs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 20)	$V_P = V_{20\text{-}15}$	max.	14 V
Voltage			
at pin 1	$V_{1\text{-}15}$	max.	V_P
at pins 9 and 10	$V_{9;\,10\text{-}15}$	max.	V_P
at pins 11, 12 and 13	$V_{11,12,13\text{-}15}$	max.	V_P
at pin 16	$V_{16\text{-}15}$	max.	V_P
Current			
at pin 21	short-circuit protected		
Total power dissipation	P_{tot}	max.	1,5 W
Storage temperature range	T_{stg}	−25 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 1 with a 1 kHz signal. $V_{1\text{-}15(rms)}$ = 0,5 V, an i.f. signal $V_{28\text{-}15(rms)}$ = 5 mV (VC/2SC = 20 dB, Δf = ± 50 kHz, f_m = 400 Hz) and with adjusted de-matrix circuit; i.f. filter selection at input pin 28 as in Fig. 3

Supply voltage range	$V_P = V_{20\text{-}15}$	10,8 to	13,2	V
Supply current	$I_P = I_{20}$	typ.	53	mA
FM limiter/amplifier and demodulator				
Start of limiting at:	$V_{28\text{-}15(rms)}$	typ.	50	μV
Input resistance	$R_{28\text{-}15}$	typ.	40	kΩ
Input capacitance	$C_{28\text{-}15}$	typ.	4,5	pF
AM suppression	α_{AMS}	typ.	60	dB
Pilot carrier processing				
Input voltage	$V_{18\text{-}15}$	typ.	6,9	V
D.C. voltage (reference via tuning coil)	$V_{22\text{-}15}$	typ.	6,0	V
AM demodulator output voltage	$V_{19\text{-}15}$	typ.	7,0	V
Controlled pilot carrier output voltage (peak-to-peak value)	$V_{22\text{-}21(p\text{-}p)}$	typ.	200	mV
Output resistance	$R_{22\text{-}15}$	>	50	kΩ
Identification frequency evaluation				
No identification signal (lower threshold)	$V_{14\text{-}15}$	typ.	2	V
Identification signal available (upper threshold)	$V_{14\text{-}15}$	typ.	4	V
Stereo transmission	$V_{17\text{-}15}$	<	2	V
Dual sound transmission	$V_{17\text{-}15}$	>	7	V
De-matrixing				
Output voltages	$V_{2;\,3;\,4\text{-}15}$	typ.	5,3	V
De-emphasis output resistances	$R_{2;\,3;\,4\text{-}15}$	typ.	12	kΩ
A.F. output signal of 2nd i.f. (r.m.s. value; see Fig. 4)	$V_{2\text{-}15(rms)}$	<	1	V
Attenuation of the demodulator output signal AF2 at audio/video mode	α_{AF2}	>	75	dB
AF1 input				
Input voltage	$V_{1\text{-}15}$	typ.	6	V
Input resistance	$R_{1\text{-}15}$	typ.	14	kΩ
Maximum input signal (r.m.s. value)	$V_{1\text{-}15(rms)}$	typ.	2	V

CHARACTERISTICS (continued)

A.F. signal switches

Output voltages	$V_{5;\,6;\,7;\,8\text{-}15}$	typ.		5,3	V
Output resistances	$R_{5;\,6;\,7;\,8\text{-}15}$	typ.		200	Ω*
Maximum a.f. output signals (r.m.s. value)					
for $V_{AF\,I(rms)}$	$V_{5;\,6\text{-}15(rms)}$	typ.		2	V
for $V_{AF\,II(rms)}$	$V_{7;\,8\text{-}15(rms)}$	typ.		2	V
Total distortion during applying a signal:					
$V_{2;\,3;\,4\text{-}15(rms)} = 0{,}5$ V	d_{tot}	typ.		0,1	%
Signal plus noise-to-noise ratio	S + N/N	typ.		80	dB
Crosstalk attenuation					
in stereo mode	α_S	>		40	dB
in dual sound mode (f = 20 Hz to 20 kHz)	α_{DS}	>		60	dB

Audio/video switch

Audio/video switch voltage (pin 16)					
for playback (HIGH)	$V_{16\text{-}15}$	7	to	V_P	V
for recording (LOW)	$V_{16\text{-}15}$	0	to	2,5	V
Audio/video switch voltage (pin 13)					
for stereo mode (LOW)	$V_{13\text{-}15}$	<		0,8	V
for dual sound mode (HIGH)	$V_{13\text{-}15}$	>		2,4	V

Switching stereo/mono and sound I/sound II

Stereo transmission					
switching voltage to pin 12 (pin 11 not affected)					
a.f. outputs I and II mono	$V_{12\text{-}15}$	<		0,8	V
a.f. outputs I and II stereo	$V_{12\text{-}15}$	>		2,4	V
Mono transmission both outputs I and II mono					
Dual sound transmission					
switching voltage to pin 11 (pin 12 not affected)					
a.f. output II sound I and output I sound II	$V_{11\text{-}15}$	<		0,8	V
a.f. output I sound I and output II sound II	$V_{11\text{-}15}$	>		2,4	V

---

* Connection of high-impedance headphones is possible.

Mode indication (pins 9 and 10)

Only the audio/video mode for a.f. output I is indicated

Maximum output current	$I_{9;\,10}$	typ.	15 mA

Indication possibilities

LED 1	LED 2	selected reception mode
OFF	OFF	mono at mono or stereo transmission
ON	ON	stereo at stereo transmission
ON	OFF	AF1 signal at dual sound transmission
OFF	ON	AF2 signal at dual sound transmission

Voltage stabilizer (pin 21)

Output voltage	$V_{21\text{-}15}$	typ.	6 V
Maximum d.c. output current short-circuit protected	$\pm I_{21}$	typ.	0,5 mA

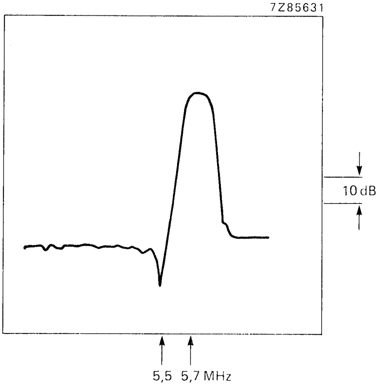


Fig. 3 IF2 filter selection.

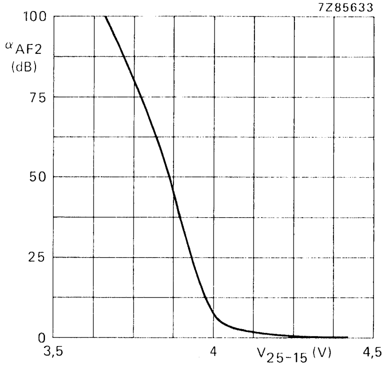


Fig. 4 Level adjustment in the demodulator part for matching of the AF2 signal to the AF1 signal; attenuation α_{AF2} as a function of $V_{25\text{-}15}$.

SPATIAL, STEREO AND PSEUDO-STEREO SOUND CIRCUIT

The TDA3810 is for radio and television equipment. Its main features are:

- Three switched functions
  - spatial (widened stereo image)
  - stereo
  - pseudo-stereo (artificial stereo from mono source material)

  mono listening only possible if a mono signal is applied directly to the output pins
- Offset compensated operational amplifiers preventing switch noise
- Muting circuit prevents LED flickering
- LED driving outputs (pins 7 and 8) indicating selected mode of operation
- TTL compatible inputs for selecting operating mode

QUICK REFERENCE DATA

Supply voltage (pin 8)	V_P	typ.	12	V
Supply current (LEDs off)	I_P	typ.	6	mA
Operating ambient temperature range	T_{amb}		0 to 70	°C
Input signal (r.m.s. value)	$V_{i(rms)}$	$<$	2	V
Total harmonic distortion (stereo)	THD	typ.	0,1	%
Channel separation (stereo)	a	typ.	70	dB
Gain (stereo)	G_v	typ.	0	dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

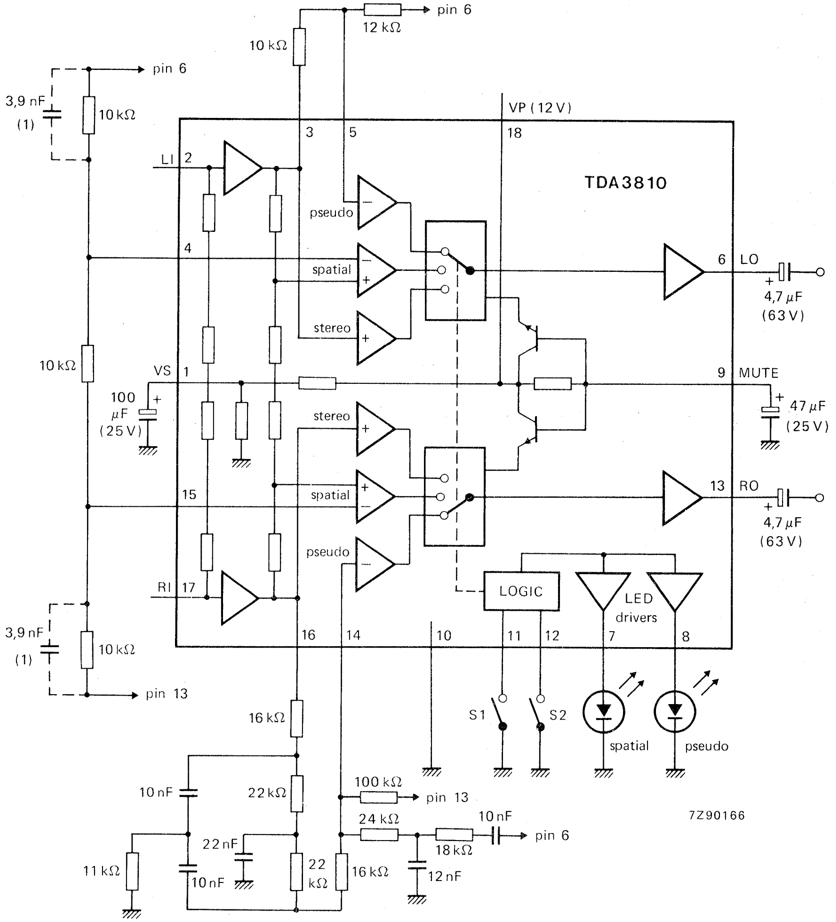


Fig. 1 Block diagram with external components. Also used as test circuit. For switch positions S1 and S2 see truth table.

1) In spatial mode for correction of high frequency only (optimal performance).

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_P	max.	17 V
Supply current (pin 18)	I_P	max.	12 mA
Storage temperature range	T_{stg}		−25 to + 150 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; test circuit Fig. 1 stereo mode (pin 11 to ground) unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 18)	V_P	4,5	–	16,5	V
Supply current	I_P	–	6	12	mA
Reference voltage	V_S	5,3	6	6,7	V
Input voltage (pin 2 or 17) THD = 0,2%	$V_{i(rms)}$	2	–	–	V
Input resistance (pin 2 or 17)	R_i	50	75	–	kΩ
Voltage gain V_o/V_i	G_v	–	0	–	dB
Channel separation (R/L)	α	60	70	–	dB
Total harmonic distortion f = 40 to 16 000 Hz; $V_{o(rms)}$ = 1 V	THD	–	0,1	–	%
Power supply ripple rejection	RR	–	50	–	dB
Noise output voltage (unweighted) left and right output	$V_{n(rms)}$	–	10	–	μV
SPATIAL MODE (pins 11 and 12 HIGH)					
Antiphase crosstalk	α	–	50	–	%
Voltage gain	G_v	1,4	2,4	3,4	dB

PSEUDO-STEREO MODE

The quality and strength of the pseudo-stereo effect is determined by external filter components.

parameter	symbol	min.	typ.	max.	unit
CONTROL INPUTS (pins 11 and 12)					
Input resistance	R_i	70	120	–	kΩ
Switching current	$-I_i$	–	35	100	μA
LED DRIVERS (pins 7 and 8)					
Output current for LED	I_o	10	12	15	mA
Forward voltage	V_F	–	–	6	V

Truth table

mode	control input state		LED spatial pin 7	LED pseudo pin 8
	pin 11	pin 12		
Mono pseudo-stereo	HIGH	LOW	off	on
Spatial stereo	HIGH	HIGH	on	off
Stereo	LOW	X	off	off

LOW = 0 to 0,8 V (the less positive voltage)
HIGH = 2 V to V_P (the more positive voltage)
X = state is immaterial

SMALL SIGNAL COMBINATION IC FOR MONOCHROME TV

GENERAL DESCRIPTION

The TDA4500 combines all small signal functions (except the tuner) which are required for a monochrome television receiver.

For a complete monochrome television receiver only output stages are required to be added for horizontal and vertical deflection, video and sound. The TDA4500 can also be used in simple colour television receivers. In this application an external sandcastle pulse generator is required.

It incorporates the following functions:

- vertical sync separator/oscillator
- vertical output
- coincidence detector (sound mute)
- phase detector/frequency control
- a.g.c. detector
- sync separator
- horizontal oscillator
- synchronous demodulator
- vision i.f. amplifier
- tuner a.g.c.
- d.c. volume control
- a.f.c. detector
- video output
- sound demodulator
- audio output
- gate pulse generator
- sound limiter/feedback
- 90° phase shift
- overload detector
- horizontal output

QUICK REFERENCE DATA

Supply voltage	V_{7-10}, V_{22-10}	typ.	10,5	V
Supply current	I_7	typ.	75	mA
Supply current	I_{22}	typ.	4,5	mA
Operating ambient temperature range	T_{amb}		−25 to +65	°C
Storage temperature range	T_{stg}		−25 to +150	°C
Power dissipation	P_{tot}	max.	1,7	W

PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT-117).

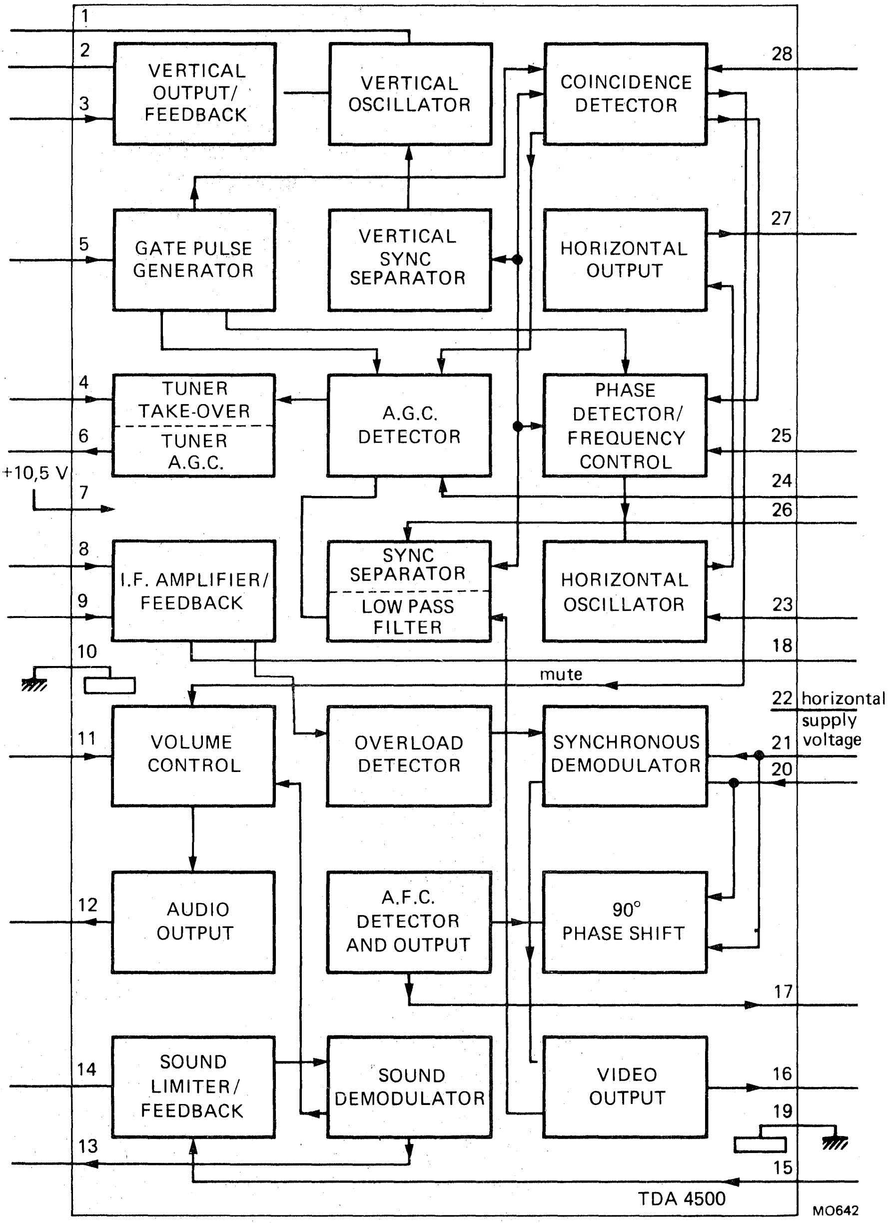


Fig. 1 Block diagram.

PINNING

Pin number	function	Pin number	function
1.	vertical oscillator	15.	sound i.f.
2.	vertical output	16.	video output
3.	vertical feedback	17.	a.f.c. output
4.	top linearity	18.	decoupling capacitor
5.	flyback pulse	19.	ground
6.	tuner a.g.c.	20.	38,5 MHz reference
7.	+10,5 V supply	21.	(38,9 MHz reference)
8.	i.f. input	22.	horizontal supply voltage
9.		23.	horizontal oscillator
10.	ground	24.	top sync detector
11.	volume control	25.	phase detector
12.	sound output	26.	sync separator
13.	6 MHz tuning (5,5 MHz tuning)	27.	horizontal output
14.	decoupling	28.	mute/coincidence detector

DEVELOPMENT SAMPLE DATA

FUNCTIONAL DESCRIPTION (Fig. 1)

A complete black-and-white receiver can be built around this circuit by adding only the output stages for horizontal and vertical deflection with the video and sound output stages. The TDA4500 can also be used in simple colour television receivers using an external circuit to generate the sandcastle.

The block diagram (Fig. 1) depicts the various functions which are described briefly below.

The sensitivity of the i.f. amplifier is 70 μV for a peak-to-peak output voltage of 3 V (compare the TDA3541). This amplifier has a symmetrical input (pins 8 and 9) and is followed by a synchronous demodulator. The external tuned circuit is connected to pins 20 and 21. This circuit provides the information for the a.f.c. circuit, the 90^o phase shift being supplied by internal RC-networks. An a.f.c. output with a voltage swing of about 9 V is obtained from pin 17 (V_{7-10} = 10,5 V).

The a.g.c. detector is gated to reduce sensitivity to external electrical noise and the a.g.c. time constant network is connected to pin 24. Gain control range of the i.f. amplifier is greater than 60 dB. Adjustments of the tuner take-over point is made at pin 4. When the voltage at pin 4 is approximately 3,5 V the direction of the tuner control voltage is positive-going. When the voltage at pin 4 is approximately 8 V the direction of the tuner control voltage is negative-going.

An output signal of 3 V (p-p) is obtained from the video amplifier (top sync level 1,5 V) with negative-going sync. Since the sound signal is derived from pin 16 (see Fig. 4) the video output is not blanked during the flyback period. As shown in the application circuit (Fig. 4) the band-pass filter for the sound must be connected between video output (pin 16) and sound i.f. input (pin 15). Sound information passes through a sound limiter network and a sound demodulator circuit with an external tuned circuit for this stage connected to pin 13. The demodulator is followed by a volume control stage with a control range of 80 dB and an output amplifier with an audio output signal of 170 mV (r.m.s.) for a Δf of 7,5 kHz and at maximum volume setting.

The slicing level of the sync separator is referred to the top sync and is determined by the values of external resistors, the recommended slicing level being 30%. Noise protection is provided for the sync separator stage. Separated sync pulses are supplied to the gated phase detector which compare the sync pulses with the sawtooth voltage obtained from the horizontal flyback pulse (pin 5). During catching the gating of the phase detector is switched off and the phase detector output current is increased.

The in-sync or out-of-sync condition is detected with the coincidence detector which is also used for transmitter identification. Sound output is suppressed when no input signal is available. Clamping the voltage on pin 28 to a level of 3,5 V sets the phase detector to a high output current, short time constant mode. This is appropriate for the reception of VCR signals.

Phase detector output voltage levels maintain the horizontal oscillator at its correct operating frequency. The push-pull output (pin 27) has a typical duty cycle of 40%.

Vertical sync pulses are obtained from an internal integrating network with the vertical sawtooth being generated in the vertical oscillator. This sawtooth voltage is compared with the feedback voltage from the deflection coil via pin 3. The comparator generates the drive voltage for the vertical deflection output stage.

The TDA4500 has four supply pins. Pin 7 and pin 10 are for the main positive supply and circuit ground respectively.

Critical circuits are grounded by pin 19. Pin 22 is the supply for the horizontal oscillator. A low current supply (5 mA minimum) can be used to start the oscillator from an external high voltage supply rail.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_{7-10}, V_{22-10}	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		–25 to +150	°C
Operating ambient temperature range	T_{amb}		–25 to +65	°C

CHARACTERISTICS

V_{7-10} = 10,5 V, V_{22-10} = 10,5 V and T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{7-10}	9,5	10,5	13,2	V
Supply current	I_7	–	75	–	mA
Supply voltage (horizontal oscillator)	V_{22-10}	9,5	10,5	13,2	V
Supply current (horizontal oscillator, note 1)	I_{22}	–	4,5	–	mA
Power dissipation	P_{tot}	–	850	–	mW
Vision i.f. amplifier (pin 8)					
Input sensitivity (onset of a.g.c.) at 39,5 MHz (note 2)	$V_{i(rms)}$	–	70	–	μV
Differential input resistance (note 3)	R_i	–	800	–	Ω
Differential input capacitance (note 3)	C_i	–	6	–	pF
Gain control range	ΔG	–	56	–	dB
Output signal expansion for 50 dB input signal variation (note 4)	ΔV_o	–	1	–	dB
Maximum input signal	$V_{i\,max}$	–	50	–	mV
Video amplifier (note 5)					
Zero signal output level (note 6)	V_{16-10}	–	5	–	V
Top sync output level (note 7)	V_{16-10}	1,2	1,4	1,6	V
Video output signal amplitude (peak-to-peak value)	$V_{16-10(p-p)}$	2,75	3,0	3,25	V
Internal bias current of n-p-n emitter follower output transistor	I_B	1,4	2,0	–	mA
Bandwidth of demodulated output signal	B	5	6	–	MHz
Video non-linearity (note 8)		–	–	10	%

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuner a.g.c.					
Take-over voltage (pin 4) for positive-going tuner a.g.c. (n-p-n tuner)	V_{4-10}	–	3,5	–	V
Take-over voltage (pin 4) for negative-going tuner a.g.c. (p-n-p tuner)	V_{4-10}	–	8	–	V
Maximum tuner a.g.c. output swing	$I_{6\ max}$	2	3	–	mA
Output saturation voltage at $I_6 = 2$ mA	$V_{6-10(sat)}$	–	–	300	mV
Leakage current	I_6	–	–	1	μA
A.F.C. circuit (note 9)					
A.F.C. output voltage swing	V_{17-19}	9	–	10	V
Available output current	$\pm I_{17}$	–	1	–	mA
Output voltage at nominal tuning of the reference tuned circuit	V_{17-19}	–	5,25	–	V
Sound circuit					
Input limiting voltage when $V_O = V_{Omax} - 3$ dB (note 10)	$V_{14\ lim}$	–	400	–	μV
Input resistance at pin 15 (note 11)	R_i	–	3	–	kΩ
A.F. output signal at pin 12 (note 12) (r.m.s. value)	$V_{12-10(rms)}$	170	–	240	mV
Volume control (pin 11) (Fig. 3)					
Voltage with pin 11 disconnected	V_{11-10}	–	6,5	–	V
Current pin 11 short-circuited to ground	I_{11}	–	1	–	mA
Volume control characteristic (note 13)			See Fig. 3		
Value of external control resistor	R_{11-10}	–	5	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Horizontal synchronization circuit					
Slicing level sync separator (note 14)		–	30	–	%
Holding range PLL		–	±1000	–	Hz
Catching range PLL		–	±600	–	Hz
Control sensitivity video to flyback (note 15)		–	2	–	kHz/μs
Horizontal oscillator					
Free running frequency	f_{osc}	–	15625	–	Hz
Spread with fixed external components	Δf_{osc}	–	–	4	%
Frequency variations due to supply voltage changes (note 16)	$\Delta f_{osc}/\Delta V$	–	0	–	%
Frequency variation with temperature	$\Delta f_{osc}/\Delta T$	–	–	1×10^{-4}	K^{-1}
Maximum frequency shift	Δf_{osc}	–	–	10	%
Maximum frequency deviation between starting point output and nominal condition	Δf_{osc}	–	–	10	%
Horizontal (push-pull) output					
Output current	I_{27}	10	–	–	mA
Output impedance	R_{27-10}	–	200	–	Ω
Voltage when I_{27} = 10 mA	V_{27-10}	–	2	–	V
	V_{27-22}	–	3	–	V
Duty cycle of output pulse (note 17)	δ	0,35	0,40	0,45	
Flyback input (note 18)					
Minimum required input amplitude (peak-to-peak value)	$V_{5-10(p-p)}$	–	4	–	V
Phase detector switching voltage		–	0	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Coincidence detector (mute) (note 19)					
Voltage in synchronized condition	V_{28-19}	–	9,5	–	V
Voltage in non-synchronized condition (no-signal)	V_{28-19}	–	1,0	1,5	V
Switching level to switch phase detector from slow to fast	V_{28-19}	4,5	5,0	5,5	V
Switching level to activate the 'mute' function (transmitter identification)	V_{28-19}	2,25	2,5	2,75	V
Output current; in-sync (peak-to-peak value)	$I_{28(p-p)}$	–	1	–	mA
Vertical oscillator					
Free running frequency	f_{osc}	–	47,5	–	Hz
Spread with fixed external components	Δf_{osc}	–	–	4	%
Holding range at nominal frequency		52,5	–	–	Hz
Temperature coefficient	TC	–	1×10^{-4}	–	K^{-1}
Frequency shift due to a supply voltage change from 9,5 to 12 V	$\Delta f_{osc}/\Delta V$	–	5	–	%
Vertical output (pin 2)					
Output current	I_2	1	1,3	–	mA
Output resistance	R_{2-10}	–	2	–	kΩ
Feedback input (pin 3)					
D.C. input voltage	V_{3-10}	4,75	5	5,25	V
A.C. input voltage (peak-to-peak value)	$V_{3-10(p-p)}$	–	1,2	–	V
Input current	I_3	–	–	10	μA
Non-linearity of deflection current at V_P = 10,5 V		–	–	2,5	%

Notes to characteristics

1. It is possible to start the horizontal oscillator by supplying a current of 5 mA which can be taken from the mains rectifier, to pin 22. The main supply (pin 7) can then be derived from the horizontal output stage.
2. I.F. input voltage (r.m.s.) – value at top sync level at which the video amplitude has dropped 0,5 dB compared with the amplitude at an input signal of 10 mV.
3. The input impedance has been chosen such that a SAW-filter can be applied. 800 Ω is an acceptable compromise between the requirements for triple transient suppression and power loss.
4. Measured with 0 dB = 150 μV.
5. Measured at 10 mV(r.m.s.) top sync input signal.
6. With switched demodulator.
7. Signal with negative-going sync with top white being 10% of the top sync amplitude (Fig. 2).
8. This figure is valid for the complete video signal amplitude (peak-white to top sync).
9. Measured with an input signal (V_{8-9}) of 10 mV(r.m.s.); the a.f.c. output (pin 7) loaded with 2 x 100 kΩ between the supply and ground. The Q factor of the reference tuned circuit is 50.
10. Voltage at pin 15 is the r.m.s. value. Q_L of the demodulator tuned circuit is 20. Audio frequency is 1 kHz and the carrier frequency is 5,5 MHz.
11. Measured with an input signal of 1 mV(r.m.s.)
12. The tuned demodulator circuit must give an output level equal to that given in the "mute" condition.
13. Volume can be controlled using a variable resistor connected to ground (nominal 5 kΩ) or by means of a variable d.c. voltage. In this latter case the rather low impedance at pin 11 must be taken into account.

DEVELOPMENT SAMPLE DATA

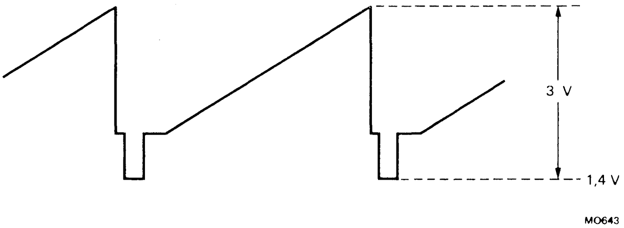


Fig. 2 Video output signal.

Notes to characteristics (continued)

14. The sync separator is noise gated. The slicing level is referred to top sync level and is independent of the video information. The value given is a percentage of the sync pulse amplitude. The slicing depends on the values of external resistors connected to pin 26.
15. Phase detector current increases by a factor of 7 during "catching" and when phase detector operates in the 'FAST' mode (pin 28). This ensures a high catching range and a higher dynamic loop gain.
16. Supply voltage variation in the range 8 to 12 V.
17. The negative-going edge of this pulse initiates the switch-off of the horizontal output transistor (simultaneous driver).
18. The circuit requires an integrated flyback pulse. The gate pulses for a.g.c. and the coincidence detector are obtained from the sawtooth.
19. The functions of in-sync/out-of-sync and transmitter identification have been combined on pin 28. For reception of VCR-signals the voltage on this pin must be fixed between 3 V and 4,5 V so that the time constant is fast and the sound is still available.

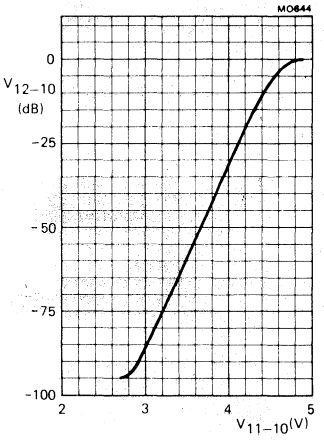


Fig. 3 Volume control characteristic at f = 1 kHz.

APPLICATION INFORMATION

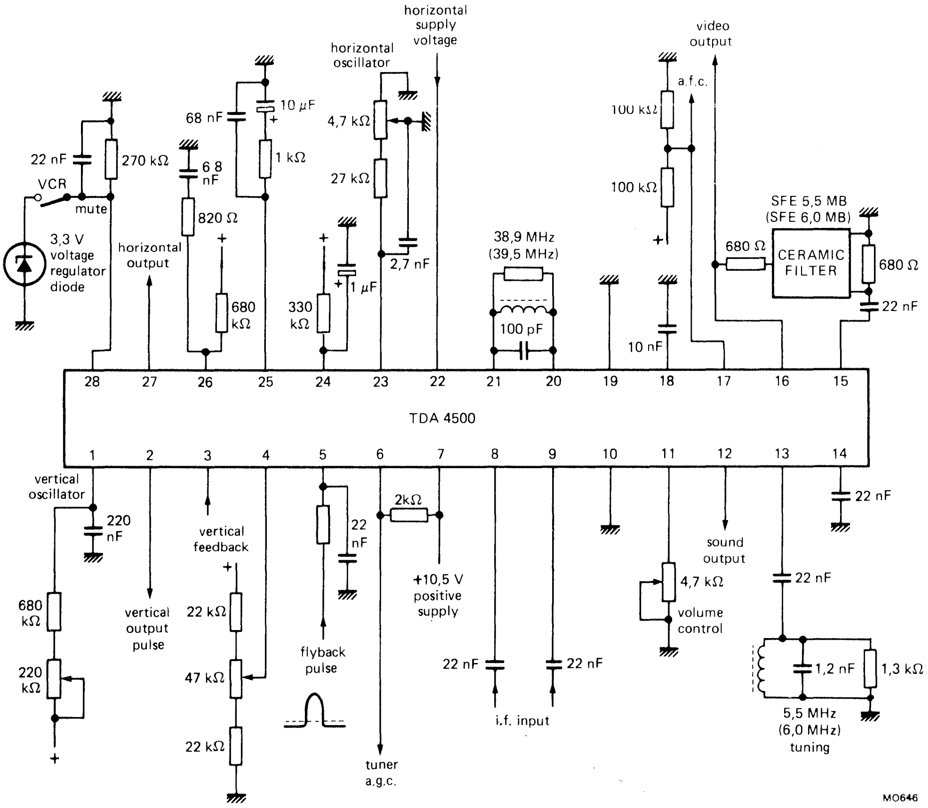


Fig. 4 Typical application circuit.

DEVELOPMENT SAMPLE DATA

PAL DECODER

The TDA4510 is a colour decoder for the PAL standard, which is pin-sequence compatible with multi-standard decoder TDA4550. It incorporates the following functions.

Chrominance part

- Gain controlled chrominance amplifier
- Chrominance output stage with automatic standard switch for driving the 64 μs delay line
- Blanking circuit for the colour burst signal

Oscillator and control voltage part

- 8,8 MHz reference oscillator with divider stage to obtain both the 4,4 MHz reference signals
- Gated phase comparison with sample and hold circuit for optimum noise characteristics
- Independent time constants for phase control and identification
- Quasi peak detector for obtaining the chrominance control voltage
- Circuit for generating the colour killer and the identification signal
- Sandcastle pulse detector.

Demodulator part

- Two synchronous demodulators for the (B-Y) and (R-Y) signals
- PAL flip-flop and PAL switch
- Flyback blanking incorporated in the synchronous demodulators
- (B-Y) and (R-Y) signal output stages with switchable d.c. voltage levels, which are controlled by the colour killer
- Internal filtering of residual carrier

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{7\text{-}3}$	typ.	12	V
Supply current	$I_P = I_7$	typ.	37	mA
Chrominance input signal (peak-to-peak)	$V_{9\text{-}3(p\text{-}p)}$		10 to 200	mV
Chrominance output signal (peak-to-peak)	$V_{6\text{-}3(p\text{-}p)}$	typ.	2	V
Colour difference output signals (peak-to-peak values)				
−(R-Y) signal	$V_{1\text{-}3(p\text{-}p)}$	typ.	1,05 V ±2	dB
−(B-Y) signal	$V_{2\text{-}3(p\text{-}p)}$	typ.	1,33 V ±2	dB
Sandcastle pulse				
burst gating level	$V_{15\text{-}3}$	typ.	7,1	V
blanking level	$V_{15\text{-}3}$	typ.	1,6	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

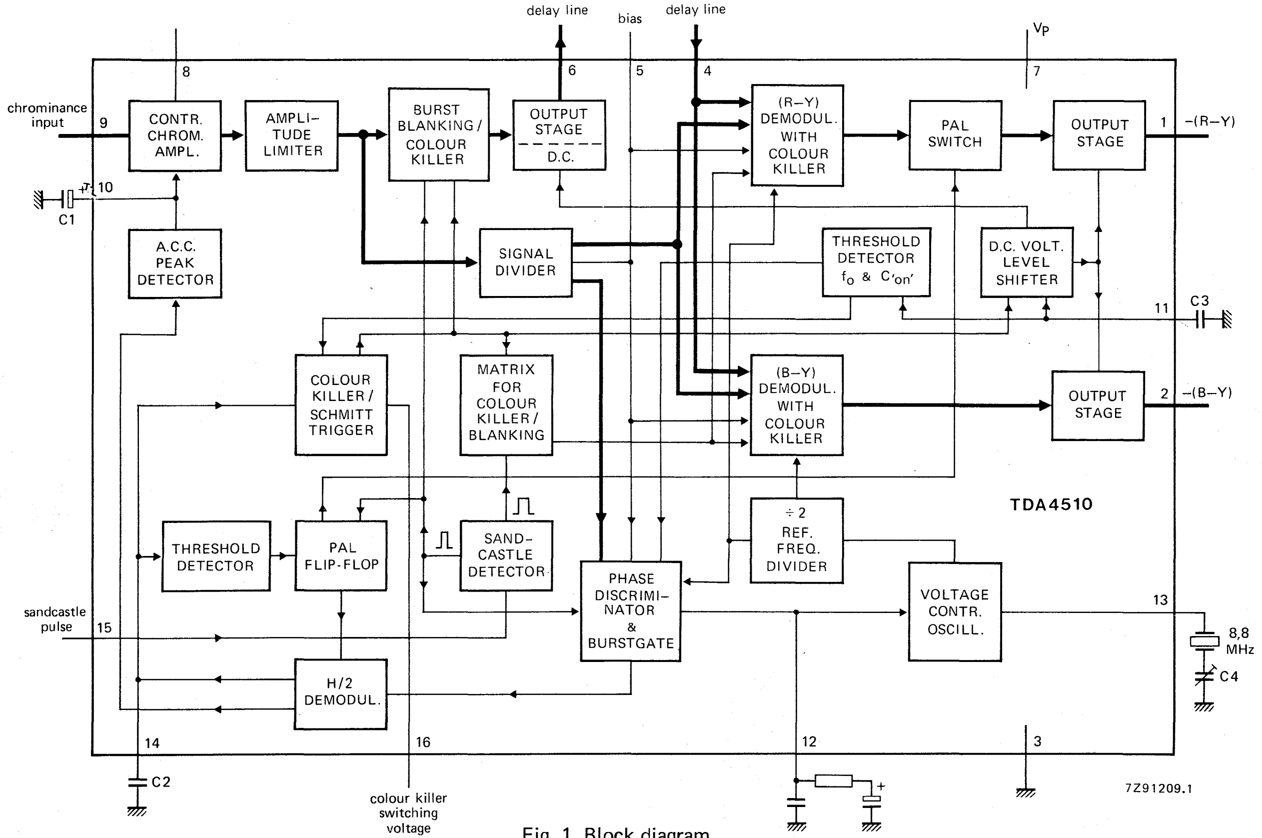


Fig. 1 Block diagram.

External capacitors

C1 pins 10-3 filter capacitor for control voltage
C2 pins 14-3 identification signal time constant.

C3 pins 11-3 time constant for the rise or fall time of the d.c. voltage level of the colour difference signals and colour OFF/ON time constant.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{7\text{-}3}$		10,8 to 13,2	V
Voltage at pins 11 and 14	$V_{11\text{-}3}$ $V_{14\text{-}3}$	max.	V_P	V
Currents				
at pins 1 and 2	$-I_{1,2}$	max.	2	mA
at pin 6	$-I_6$	max.	12	mA
at pin 16	$-I_{16}$	max.	10	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−25 to + 150	°C
Operating ambient temperature	T_{amb}		0 to + 70	°C

CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 2 unless otherwise specified

Supply current	I_7	typ.	37	mA
Chrominance part				
Input voltage range (peak-to-peak value)	$V_{9\text{-}3(p\text{-}p)}$		10 to 200	mV
Nominal input voltage (peak-to-peak value) with 75% colour bar signal	$V_{9\text{-}3(p\text{-}p)}$	typ.	100	mV
Input impedance	$Z_{9\text{-}3}$	typ.	10	kΩ
Input capacitance	$C_{9\text{-}3}$	$<$	5	pF
Colour ON				
chrominance output voltage (peak-to-peak) with 75% colour bar signal	$V_{6\text{-}3(p\text{-}p)}$	typ.	2	V
d.c. voltage at chrominance output	$V_{6\text{-}3}$	typ.	9	V
Colour OFF				
chrominance suppression	α	$>$	56	dB
d.c. voltage at chrominance output	$V_{6\text{-}3}$	typ.	3	V
Oscillator and control voltage part				
Oscillator frequency	f_o	typ.	8,8	MHz
Input resistance	$R_{13\text{-}3}$	typ.	270	Ω
Catching range (depending on RC-network between pins 12 and 3) at R = 4,7 kΩ and C = 470 nF	Δf	$>$	500	Hz
Control voltage				
at nominal input signal	$V_{14\text{-}3}$	typ.	5,2	V
without chrominance input signal	$V_{14\text{-}3}$	typ.	6,0	V
colour OFF voltage	$V_{14\text{-}3}$	typ.	5,7	V
colour ON voltage	$V_{14\text{-}3}$	typ.	5,5	V
identification ON voltage	$V_{14\text{-}3}$	typ.	6,2	V
forced colour OFF	$V_{14\text{-}3}$	typ.	7,0	V
forced colour ON	$V_{14\text{-}3}$	typ.	5,3	V

CHARACTERISTICS (continued)

Oscillator and control voltage part (continued)

Colour ON delay via ramp generator C3 = 0,47 μF	t_d	<	40	ms
forced colour ON voltage (for oscillator adjustment)	$V_{11\text{-}3}$	>	$V_P - 0{,}2$	V
Colour switching output (open npn emitter)				
output current	$-I_{16}$	<	5	mA
colour ON voltage	$V_{16\text{-}3}$	>	10	V
colour OFF voltage	$V_{16\text{-}3}$	<	0,5	V

Demodulator part

Delayed chrominance input signal (peak-to-peak value) with 75% colour bar signal	$V_{4\text{-}3(p\text{-}p)}$	typ.	220	mV
Colour difference output signals (peak-to-peak value)				
−(R-Y) signal	$V_{1\text{-}3(p\text{-}p)}$	typ.	1,05 V ± 2	dB
−(B-Y) signal	$V_{2\text{-}3(p\text{-}p)}$	typ.	1,33 V ± 2	dB
Ratio of colour difference output signals (R-Y)/(B-Y)	$\frac{V_{1\text{-}3}}{V_{2\text{-}3}}$	typ.	0,79	V
Tolerance of ratio			± 10	%
D.C. voltage at colour difference outputs				
at colour ON	$V_{1;2\text{-}3}$	typ.	9	V
at colour OFF	$V_{1;2\text{-}3}$	typ.	3	V
Signal attenuation at colour OFF	$\alpha_1; \alpha_2$	>	60	dB
Residual 4,4 MHz (peak-to-peak value)	$V_{1,2\text{-}3(p\text{-}p)}$	<	20	mV
H/2 ripple at (R-Y) output (peak-to-peak) without input signal	$V_{1\text{-}3(p\text{-}p)}$	<	10	mV

Sandcastle pulse detector

Voltage level at which the vertical and line blanking pulse is separated	$V_{15\text{-}3}$	typ.	1,6 V ± 0,3	V
Required pulse amplitude	$V_{15\text{-}3(p\text{-}p)}$	typ.	2,5 V ± 0,5	V
Voltage level at which the burst gating pulse is separated	$V_{15\text{-}3}$	typ.	7,1 V ± 0,5	V
Required pulse amplitude	$V_{15\text{-}3(p\text{-}p)}$	>	7,6	V
Input voltage during horizontal scanning	$V_{15\text{-}3}$	<	1,1	V
Input current	$-I_{15}$	<	100	μA

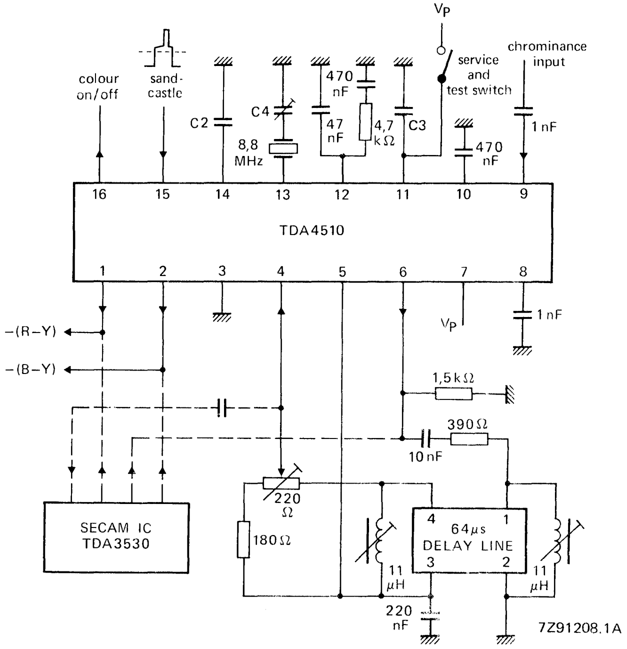


Fig. 2 Application information and test circuit.

C1 = 470 nF; C2 = 100 nF; C3 = 470 nF; C4 = 5 to 27 pF, X = 8,8 MHz.

Nominal crystal frequency 8,867 238 MHz; resonance resistance 60 Ω;
load capacitance 20 pF; dynamic capacitance 22 fF and static capacitance 5,5 pF.

SECAM DECODER

GENERAL DESCRIPTION

The TDA4530 is a colour decoder for the SECAM standard. It is compatible for direct use with the TDA4550 multistandard decoder and may also be used with the TDA4510 PAL decoder to form a flexible PAM/SECAM decoding system with automatic standard switching.

Features

- Vertical or combined horizontal and vertical identification
- Uses external phase shifting networks
- Simple application and alignment

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}6}$	typ.	12	V
Supply current (pin 8)	$I_P = I_8$	typ.	50	mA
Input voltage range (peak-to-peak value)	$V_{11\text{-}6(p\text{-}p)}$		15 to 300	mV
A.G.C. control range		>	26	dB
Ratio of colour difference outputs −(B−Y)/−(R−Y)	$V_{18/16\text{-}6}$		0,79	
Colour difference output −(B−Y) with 75% colour bar signal (peak-to-peak value)	$V_{18\text{-}6(p\text{-}p)}$		1,33	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102A).

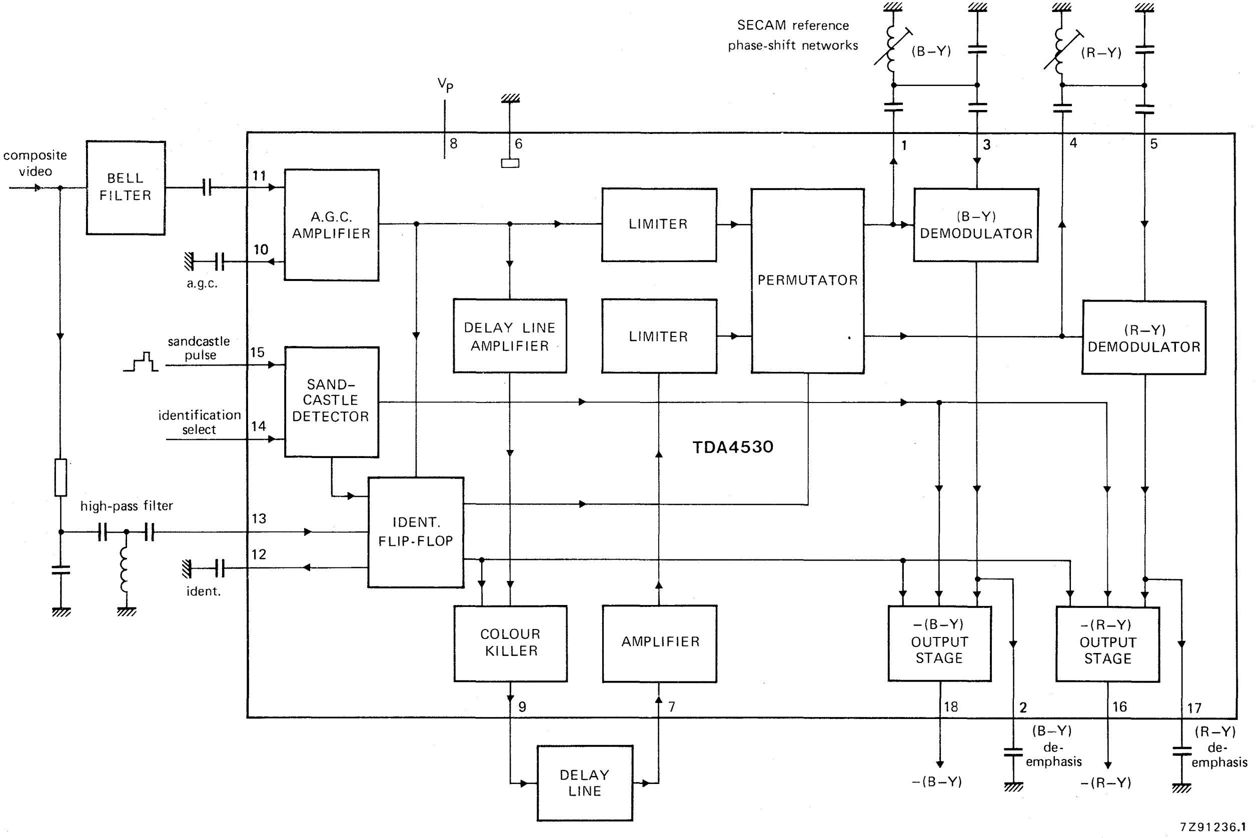


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8\text{-}6}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,6 W
Operating ambient temperature range	T_{amb}		−20 to + 70 °C
Storage temperature range	T_{stg}		−55 to + 150 °C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\,cr\text{-}a}$	50 K/W

CHARACTERISTICS

$V_P = V_{8\text{-}6} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies (pin 8)					
Supply voltage	$V_{8\text{-}6}$	10,8	12,0	13,2	V
Supply current	I_8	–	50	–	mA
A.G.C. amplifier input (pin 10)					
Input signal (peak-to-peak value) (note 1)	$V_{11\text{-}6(p\text{-}p)}$	15	–	300	mV
Input resistance	$R_{11\text{-}6}$	7,5	10,0	–	kΩ
A.G.C. control range		26	–	–	dB
Colour killer output (pin 9)					
Output voltage (peak-to-peak value) at SECAM ON; $V_{11\text{-}6(p\text{-}p)} = 100$ mV	$V_{9\text{-}6(p\text{-}p)}$	1,0	1,2	1,4	V
Variation of output signal for input signal full range variation of 26 dB at pin 11		–	–	3	dB
D.C. voltage level at SECAM ON (note 2)	$V_{9\text{-}6}$	5,5	6,0	6,5	V
D.C. voltage level at SECAM OFF (note 2)	$V_{9\text{-}6}$	3,5	4,0	4,5	V
Output impedance at SECAM ON	$Z_{9\text{-}6}$	–	20	25	Ω
Maximum output current (peak value)	I_9	8	–	–	mA
Attenuation of output signal at SECAM OFF (PAL/SECAM application only)	$V_{9\text{-}6}$	56	60	–	dB
Delayed chrominance input (pin 7)					
Input voltage (peak-to-peak value)	$V_{7\text{-}6(p\text{-}p)}$	–	150	175	mV
Input resistance	$R_{7\text{-}6}$	–	4	–	kΩ

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Permutator outputs (pins 1 and 4)					
Output voltage (peak-to-peak value)	$V_{1,4\text{-}6(p\text{-}p)}$	–	2	–	V
Output impedance	$Z_{1,4\text{-}6}$	–	–	100	Ω
Identification input (pin 13)					
Input voltage (peak-to-peak value)	$V_{13\text{-}6}$	–	tbf	–	mV
Input impedance	$Z_{13\text{-}6}$	–	4	–	kΩ
Horizontal identification timing		–	4	–	μs
Sandcastle detector (pin 15)					
Input current at $V_{15\text{-}6} = 0$ V	$-I_{15\text{-}6}$	–	–	100	μA
Input capacitance	C_{15}	–	–	10	pF
Decoding threshold levels (notes 2 and 3)					
horizontal identification	$V_{15\text{-}6}$	5,5	6,5	7,0	V
flip-flop triggering	$V_{15\text{-}6}$	3,1	3,5	3,9	V
half picture identification	$V_{15\text{-}6}$	1,0	1,5	1,8	V
vertical/horizontal pulse separation:					
pulse ON	$V_{15\text{-}6}$	1,3	1,6	1,9	V
pulse OFF	$V_{15\text{-}6}$	1,1	1,4	1,7	V
horizontal pulse separation: pulse ON	$V_{15\text{-}6}$	3,3	3,6	3,9	V
pulse OFF	$V_{15\text{-}6}$	3,1	3,4	3,7	V
burst pulse separation: pulse ON	$V_{15\text{-}6}$	6,6	7,1	7,6	V
pulse OFF	$V_{15\text{-}6}$	6,4	6,9	7,4	V
Demodulators (pins 3 and 5)					
Input voltage (peak-to-peak value)	$V_{3,5\text{-}6(p\text{-}p)}$	300	–	–	mV
Input resistance	$R_{3,5\text{-}6}$	–	4,7	–	kΩ
Demodulator linearity		95	–	–	%
Colour difference outputs (pins 16 and 18)					
Spread of –(B–Y) colour difference output with 75% colour bar signal (peak-to-peak value)	$V_{18\text{-}6(p\text{-}p)}$	–1 dB	1,33	+ 1 dB	V
Ratio of colour difference outputs –(B–Y)/–(R–Y)	$V_{18/16\text{-}6}$	0,71	0,79	0,87	
D.C. voltage level of colour difference outputs (note 2)	$V_{16,18\text{-}6}$	5,5	6,0	6,5	V
Output impedance	$Z_{16,18\text{-}6}$	–	–	200	Ω
Signal attenuation at colour OFF	$\alpha_{16,18\text{-}6}$	54	60	–	dB

parameter	symbol	min.	typ.	max.	unit
Cross-coupling in chrominance frequency range: at frequencies corresponding to saturated green; f_R = 4,72 MHz and f_B = 4,04 MHz (note 4)		40	–	–	dB
H/2 ripple at outputs when input signal is zero	$V_{16,18\text{-}6}$	34	40	–	dB
Output voltage for chrominance frequencies $(4 \leqslant f \leqslant 5)$ MHz (peak-to-peak value)	$V_{16,18\text{-}6}$	–	–	20	mV
Output voltage for chrominance harmonics $(8 < f < 10)$ MHz (peak-to-peak value)	$V_{16,18\text{-}6}$	–	–	50	mV

Notes to the characteristics

1. Harmonics increase at maximum input signal.
2. Levels are proportional to supply voltage V_P.
3. For horizontal + half picture identification pin 14 should be connected to ground and the sandcastle pulse should contain the half picture blanking.
4. With ideal delay line.

MULTISTANDARD DECODER

GENERAL DESCRIPTION

The TDA4550 is a monolithic integrated multistandard colour decoder for the PAL, SECAM, NTSC 3,58 MHz and NTSC 4,43 MHz standards.

Features

Chrominance part

- Gain controlled chrominance amplifier for PAL, SECAM and NTSC
- ACC rectifier circuits (PAL/NTSC, SECAM)
- Burst blanking (PAL) in front of 64 µs glass delay line
- Chrominance output stage for driving the 64 µs glass delay line (PAL, SECAM)
- Limiter stages for direct and delayed SECAM signal
- SECAM permutator

Demodulator part

- Flyback blanking incorporated in the two synchronous demodulators (PAL, NTSC)
- PAL switch
- Internal PAL matrix
- Two quadrature demodulators with external reference tuned circuits (SECAM)
- Internal filtering of residual carrier
- De-emphasis (SECAM)
- Insertion of reference voltages as achromatic value (SECAM) in the (B-Y) and (R-Y) colour difference output stages (blanking)

Identification part

- Automatic standard recognition by sequential inquiry
- Delay for colour-on and scanning-on
- Reliable SECAM identification by PAL priority circuit
- Forced switch-on of a standard
- Four switching voltages for chrominance filters, traps and crystals
- Two identification circuits for PAL/SECAM (H/2) and NTSC
- PAL/SECAM flip-flop
- SECAM identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Crystal oscillator with divider stages and PLL circuitry (PAL, NTSC) for double colour subcarrier frequency
- HUE control (NTSC)
- Service switch

QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13\text{-}9}$	typ.	12	V
Supply current (pin 13)	$I_P = I_{13}$	typ.	60	mA
Chrominance input signal (peak-to-peak)	$V_{15\text{-}9(p\text{-}p)}$		10 to 200	mV
Chrominance output signal (peak-to-peak)	$V_{12\text{-}9(p\text{-}p)}$	typ.	1,6	V
Colour difference output signals (peak-to-peak values)				
– (R-Y) signal	$V_{1\text{-}9(p\text{-}p)}$	typ.	1,05	V ± 2 dB
– (B-Y) signal	$V_{3\text{-}9(p\text{-}p)}$	typ.	1,33	V ± 2 dB
Sandcastle pulse; required amplitude for				
vertical and horizontal pulse separation	$V_{24\text{-}9}$	typ.	2,5	V
horizontal pulse separation	$V_{24\text{-}9}$	typ.	4,5	V
burst gating	$V_{24\text{-}9}$	typ.	7,7	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

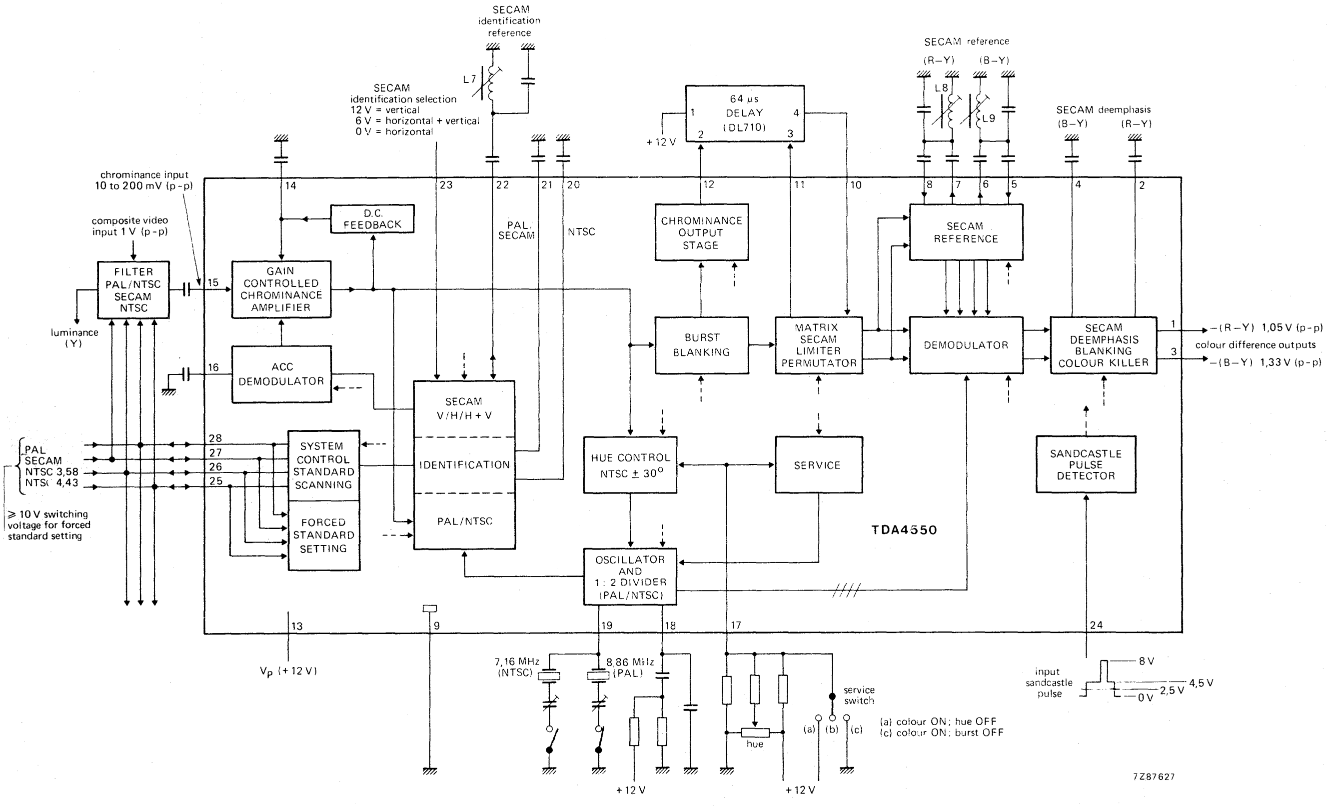


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13\text{-}9}$	max.	13,2	V
Voltage range at pins 10, 11, 17, 23, 24, 25, 26, 27, 28 to pin 9 (ground)	$V_{n\text{-}9}$		0 to V_P	V
Current at pin 12	$-I_{12}$	max.	10	mA
Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

CHARACTERISTICS

$V_P = V_{13\text{-}9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13\text{-}9}$	10,8	–	13,2	V
Supply current	$I_P = I_{13}$	–	60	–	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage with 75% colour bar signal (peak-to-peak value)	$V_{15\text{-}9(p\text{-}p)}$	10	100	200	mV
input impedance	$\lvert Z_{15\text{-}9}\rvert$	–	3,3	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12\text{-}9(p\text{-}p)}$	–	1,6	–	V
output impedance (n-p-n emitter follower)	$\lvert Z_{12\text{-}9}\rvert$	–	–	20	Ω
d.c. output voltage	$V_{12\text{-}9}$	–	8	–	V
Input for delayed signal (pin 10)					
d.c. input current	I_{10}	–	–	10	μA
input resistance	$R_{10\text{-}9}$	10	–	–	kΩ
Demodulator part (PAL/NTSC)					
Colour difference output signals					
output voltage (peak-to-peak value)					
– (R-Y) signal (pin 1)	$V_{1\text{-}9(p\text{-}p)}$	–	1,05 V ± 2 dB	–	V
– (B-Y) signal (pin 3)	$V_{3\text{-}9(p\text{-}p)}$	–	1,33 V ± 2 dB	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3\text{-}9}$	–	0,79 ± 10%	–	
Residual carrier (subcarrier frequency) (peak-to-peak value)	$V_{1,3\text{-}9(p\text{-}p)}$	–	–	30	mV
H/2 ripple at (R-Y) output (pin 1) (peak-to-peak value) without input signal	$V_{1\text{-}9(p\text{-}p)}$	–	–	10	mV
D.C. output voltage n-p-n emitter follower with internal current source of 0,3 mA	$V_{1,3\text{-}9}$	–	7,8	–	V
output impedance	$\lvert Z_{1,3\text{-}9}\rvert$	–	–	150	Ω

parameter	symbol	min.	typ.	max.	unit
Demodulator part (SECAM)					
Colour difference signals (see note 1) output voltage (peak-to-peak value)					
– (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05	–	V
– (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33	–	V
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	–	30	mV
H/2 ripple at (R-Y) (B-Y) outputs (pins 1 and 3) (peak-to-peak value) with f_o signals	$V_{1,3-9(p-p)}$	–	–	20	mV
D.C. output voltage	$V_{1,3-9}$	–	7,8	–	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only)	$\Delta V/\Delta T$	–	–	0,5	mV/K
HUE control (NTSC)/service switch					
Phase shift of reference carrier at $V_{17-9} = 2$ V	$-\phi$	–	30	–	deg
at $V_{17-9} = 3$ V	ϕ	–	0	–	deg
at $V_{17-9} = 4$ V	$+\phi$	–	30	–	deg
Input resistance	R_{17-9}	–	5	–	kΩ
Service position					
Switching voltage (pin 17) burst OFF; colour ON (for oscillator adjustment)	V_{17-9}	–	–	0,5	V
HUE control OFF; colour ON (for forced colour ON)	V_{17-9}	6	–	–	V
Crystal oscillator (pin 19)					
For double colour subcarrier frequency input resistance	R_{19-9}	–	270	–	Ω
lock-in-range referred to subcarrier frequency	Δf	± 500	–	–	Hz

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Identification part					
Switching voltages for chrominance filters and crystals					
at pin 28 (PAL)					
at pin 27 (SECAM)					
at pin 26 (NTSC 3,58 MHz)					
at pin 25 (NTSC 4,43 MHz)					
Control voltage OFF state	$V_{25,26,27,28\text{-}9}$	–	–	0,5	V
Control voltage ON state					
during scanning; colour OFF	$V_{25,26,27,28\text{-}9}$	–	2,5	–	V
colour ON	$V_{25,26,27,28\text{-}9}$	–	6	–	V
Output current	$-I_{25,26,27,28\text{-}9}$	–	–	3	mA
Voltage for forced switching ON					
PAL	$V_{28\text{-}9}$	9	–	–	V
SECAM	$V_{27\text{-}9}$	9	–	–	V
NTSC 3,58 MHz	$V_{26\text{-}9}$	9	–	–	V
NTSC 4,43 MHz	$V_{25\text{-}9}$	9	–	–	V
Delay time for					
restart of scanning	t_{dS}	2 to 3 vertical periods			
colour ON	t_{dC1}	2 to 3 vertical periods			
colour OFF	t_{dC2}	0 to 1 vertical periods			
SECAM identification (pin 23)					
Input voltage for					
horizontal identification (H)	$V_{23\text{-}9}$	–	–	2	V
vertical identification (V)	$V_{23\text{-}9}$	10	–	–	V
combined (H) and (V) identification	$V_{23\text{-}9}$	–	6*	–	V
Sequence of standard inquiry PAL-SECAM-NTSC 3,58 MHz-NTSC 4,43 MHz					
Reliable SECAM identification by PAL priority circuit					
Scanning time for each standard	t_S	4 vertical periods			

---

* Or not connected.

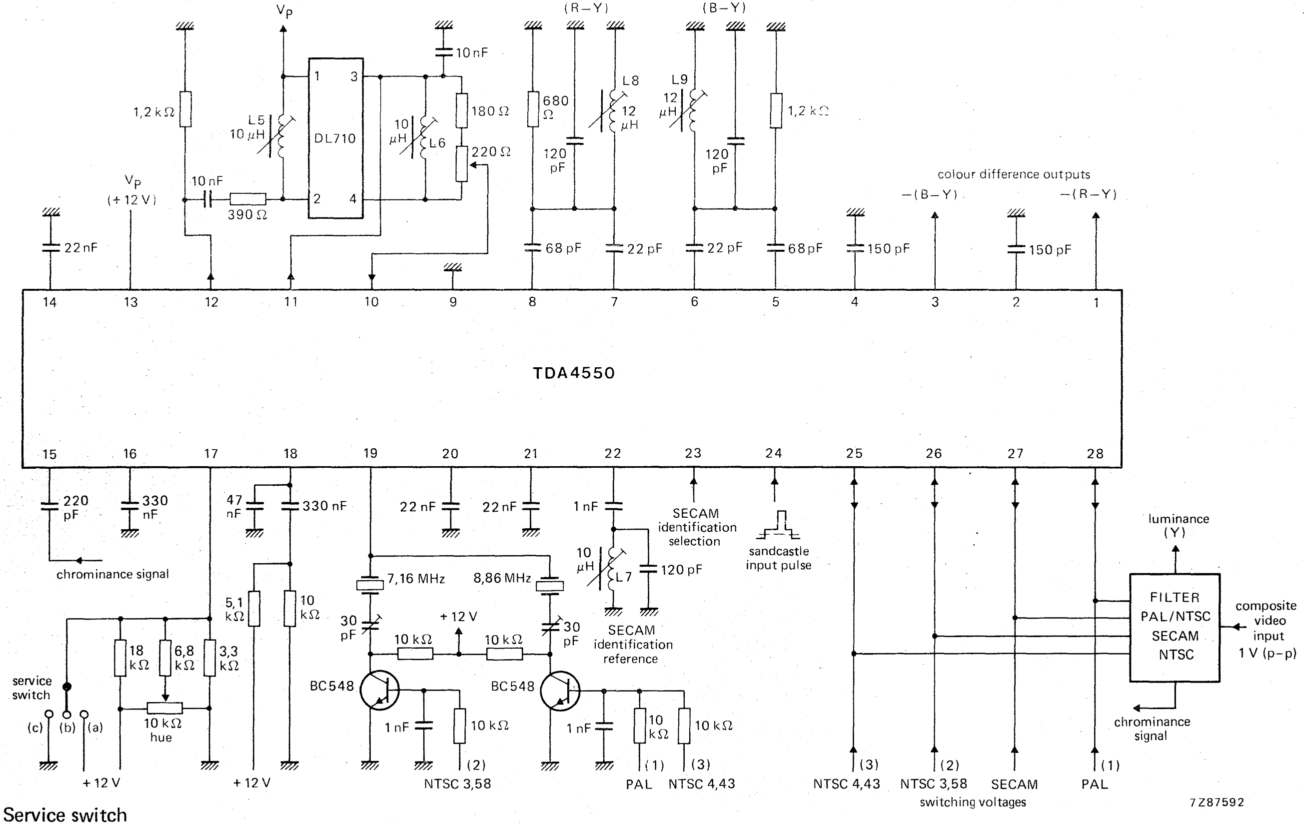
parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (see note 2)					
Input voltage pulse levels (pin 24)					
to separate vertical and horizontal blanking pulses	$V_{24\text{-}9}$	1,2	–	2,0	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	2,0	–	3,0	V
to separate horizontal blanking pulse	$V_{24\text{-}9}$	3,2	–	4,0	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	4,0	–	5,0	V
to separate burst gating pulse	$V_{24\text{-}9}$	6,5	–	7,7	V
required pulse amplitude	$V_{24\text{-}9(p\text{-}p)}$	7,7	–	V_P	V
Input voltage during horizontal scanning	$V_{24\text{-}9}$	–	–	1,0	V
Input current	$-I_{24}$	–	–	100	μA

Notes to the characteristics

1. The signal amplitude of the colour difference signals (R-Y) and B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 6, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_0) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION



Service switch

(a) colour ON; hue OFF

(c) colour ON; burst OFF

Fig. 2 Application diagram.

COLOUR TRANSIENT IMPROVEMENT CIRCUIT

GENERAL DESCRIPTION

The TDA4560 is a monolithic integrated circuit for colour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 720 ns to 1035 ns in steps of 45 ns
- Output for the option of velocity modulation

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10\text{-}18}$	typ.	12	V
Supply current (pin 10)	$I_P = I_{10}$	typ.	35	mA
(R-Y) and (B-Y) attenuation	α_{cd}	typ.	0	dB
(R-Y) and (B-Y) output transient time	t_{tr}	typ.	150	ns
Adjustable Y-delay time	t_d		720 to 1035	ns
Y-attenuation	α_y	typ.	7	dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

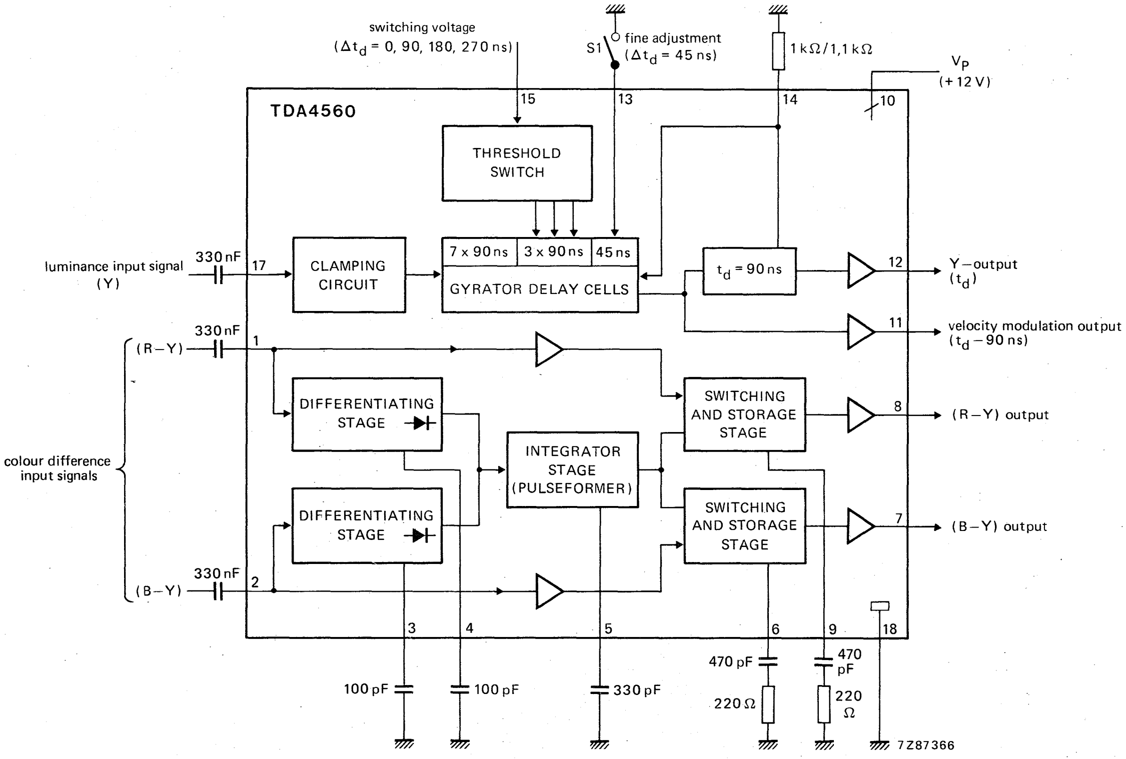


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The IC consists of two colour difference channels (B-Y) and (R-Y) and a luminance signal path (Y) as shown in Fig. 1.

Colour difference channels

The (B-Y) and (R-Y) colour difference channels consist of a buffer amplifier at the input, a switching stage and an output amplifier. The switching stages, which are controlled by transient detecting stages (differentiators), switch to a value that has been stored at the beginning of the transients. The differentiating stages get their signal direct from the colour difference detecting signal (pins 1 and 2). Two parallel storage stages are incorporated in which the colour difference signals are stored during the transient time of the signal. After a time of about 600 ns they are switched immediately (transient time of 150 ns) to the outputs. The colour difference channels are not attenuated.

Y-signal path

The Y-signal input (pin 17) is capacitively coupled to an input clamping circuit. Gyrator delay cells provide a maximum delay of 1035 ns including an additional delay of 45 ns via the fine adjustment switch (S1) at pin 13. Three delay cells are switched with two interstage switches dependent on the voltage at pin 15. Thus three switchable delay times of 90 ns, 180 ns or 270 ns less than the maximum delay time are available. A tuning compensation circuit ensures accuracy of delay time despite process tolerances. The Y-signal path has a 7 dB attenuation as a normal Y-delay coil and can replace this completely. The output is fed to pin 12 via a buffer amplifier. An additional output stage provides a signal of 90 ns less delay at pin 11 for the option of velocity modulation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 10)	$V_P = V_{10\text{-}18}$	max.	13,2	V
Voltage ranges to pin 18 (ground)				
at pins 1, 2, 12, 15	$V_{n\text{-}18}$		0 to V_P	V
at pin 11	$V_{11\text{-}18}$		0 to $V_P - 3$	V
at pin 17	$V_{17\text{-}18}$		0 to 7	V
Voltages ranges				
at pin 7 to pin 6	$V_{7\text{-}6}$		0 to 5	V
at pin 8 to pin 9	$V_{8\text{-}9}$		0 to 5	V
Currents				
at pins 6, 9	$\pm I_{6,9}$	max.	15	mA
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

Note

Pins 3, 4, 5, 6, 9, 13 and 14 d.c. potential not published.

CHARACTERISTICS

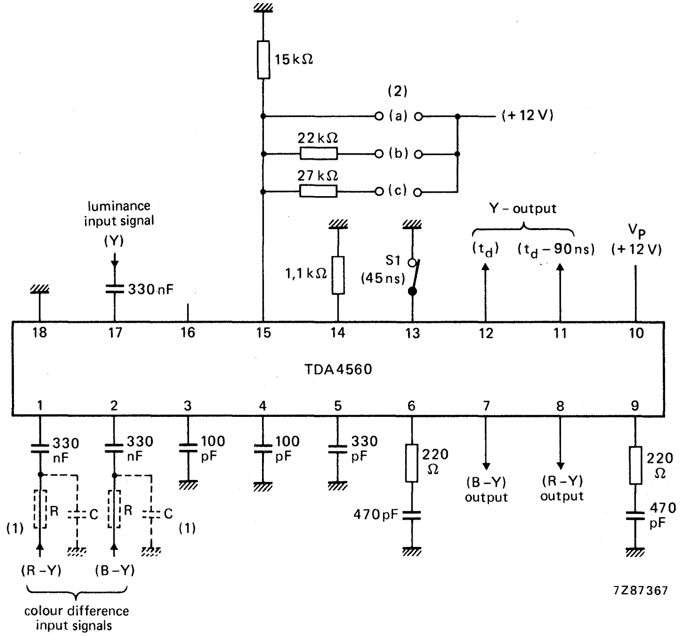
$V_P = V_{10\text{-}18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 10)					
Supply voltage	$V_P = V_{10\text{-}18}$	–	12	13,2	V
Supply current	$I_P = I_{10}$	–	35	–	mA
Colour difference channels (pins 1 and 2)					
(R-Y) input voltage (peak-to-peak value) 75% colour bar signal	$V_{1\text{-}18}$	–	1,05	–	V
(B-Y) input voltage (peak-to-peak value) 75% colour bar signal	$V_{2\text{-}18}$	–	1,33	–	V
Input resistance	$R_{1,\,2\text{-}18}$	–	12	–	kΩ
(B-Y), (R-Y) signal attenuation $\frac{V_8}{V_1}, \frac{V_7}{V_2}$	α_{cd}	–	0	–	dB
Output current (emitter follower with constant current source 0,5 mA)	$-I_{7,\,8}$	–	1,2	–	mA
(R-Y) and (B-Y) output signal transient time	t_{tr}	–	150	–	ns
Y-signal path (pin 17)					
Y-input voltage (composite signal) (peak-to-peak value)	$V_{17\text{-}18(p\text{-}p)}$	–	1	–	V
Input resistance	$R_{17\text{-}18}$	–	20	–	kΩ
Internal bias voltage	$V_{17\text{-}18}$	–	2,3	–	V
Input current					
during picture content	I_{17}	–	8	–	μA
during synchronizing pulse	$-I_{17}$	–	100	–	μA
Y-signal attenuation $\frac{V_{11}}{V_{17}}, \frac{V_{12}}{V_{17}}$	α_y	–	7	–	dB
Output current (emitter follower with constant current source 0,4 mA)	$-I_{11,\,12}$	–	1,2	–	mA
Frequency response ($V_{15\text{-}18} = 0$ V)					
at $R_{14\text{-}18} = 1$ kΩ	$f_{12\text{-}17}$	–	6	–	MHz
at $R_{14\text{-}18} = 1,1$ kΩ	$f_{12\text{-}17}$	–	4,5	–	MHz

parameter	symbol	min.	typ.	max.	unit
Y-signal path (pin 17) (continued)					
Adjustable delay (switch S1 open)					
at $V_{15\text{-}18}$ = 0 to 2,5 V; $R_{14\text{-}18}$ = 1 kΩ	t_d	–	640	–	ns
at $V_{15\text{-}18}$ = 0 to 2,5 V; $R_{14\text{-}18}$ = 1,1 kΩ	t_d	–	720	–	ns
at $V_{15\text{-}18}$ = 3,5 to 5,5 V; $R_{14\text{-}18}$ = 1 kΩ	t_d	–	720	–	ns
at $V_{15\text{-}18}$ = 3,5 to 5,5 V; $R_{14\text{-}18}$ = 1,1 kΩ	t_d	–	810	–	ns
at $V_{15\text{-}18}$ = 6,5 to 8,5 V; $R_{14\text{-}18}$ = 1 kΩ	t_d	–	800	–	ns
at $V_{15\text{-}18}$ = 6,5 to 8,5 V; $R_{14\text{-}18}$ = 1,1 kΩ	t_d	–	900	–	ns
at $V_{15\text{-}18}$ = 9,5 to 12 V; $R_{14\text{-}18}$ = 1 kΩ	t_d	–	880	–	ns
at $V_{15\text{-}18}$ = 9,5 to 12 V; $R_{14\text{-}18}$ = 1,1 kΩ	t_d	–	990	–	ns
Fine adjustment delay (switch S1 closed)					
at $V_{13\text{-}18}$ = 0 V	Δt_d	–	45	–	ns
Signal delay for velocity modulation (pin 11)					
with $R_{14\text{-}18}$ = 1 kΩ	t		t_d – 80 ns		
with $R_{14\text{-}18}$ = 1,1 kΩ	t		t_d – 90 ns		
Thermal resistance					
From junction to ambient (in free air)	$R_{th\ j\text{-}a}$	–	–	70	K/W

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.

Fig. 2 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
X	X	X	0 to 2,5 V	720
X	X	O	3,5 to 5,5 V	810
X	O	O	6,5 to 8,5 V	900
O	O	O	9,5 to 12 V	990

Where: X = connection closed; O = connection open.

---

* When switch (S1) is closed the delay time is increased by 45 ns.

TAPE END DETECTOR FOR VCR

GENERAL DESCRIPTION

The TDA5010 is designed to make digital switch pulses out of information coming from a pair of reflection light barriers and it also contains a logic switch array with an enable input. Specially intended for tape end detection and logic switching in VCR applications.

Features

- Two inputs for two light barriers
- Output signal proportional to the ratio of the two currents
- Balance adjustment for the inputs
- Logic expander with enable input

QUICK REFERENCE DATA

Supply voltage	V_{CC}		4,75 to 9	V
Supply current	I_{CC}	typ.	1	mA
Voltage control inputs				
LOW	V_{IL}		0 to 0,8	V
HIGH	V_{IH}		2 to 13	V
Input current pins 1 and 2	$I_{1,2}$	typ.	130	μA
Power dissipation	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		−25 to + 150	°C
Operating ambient temperature	T_{amb}		+ 5 to + 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

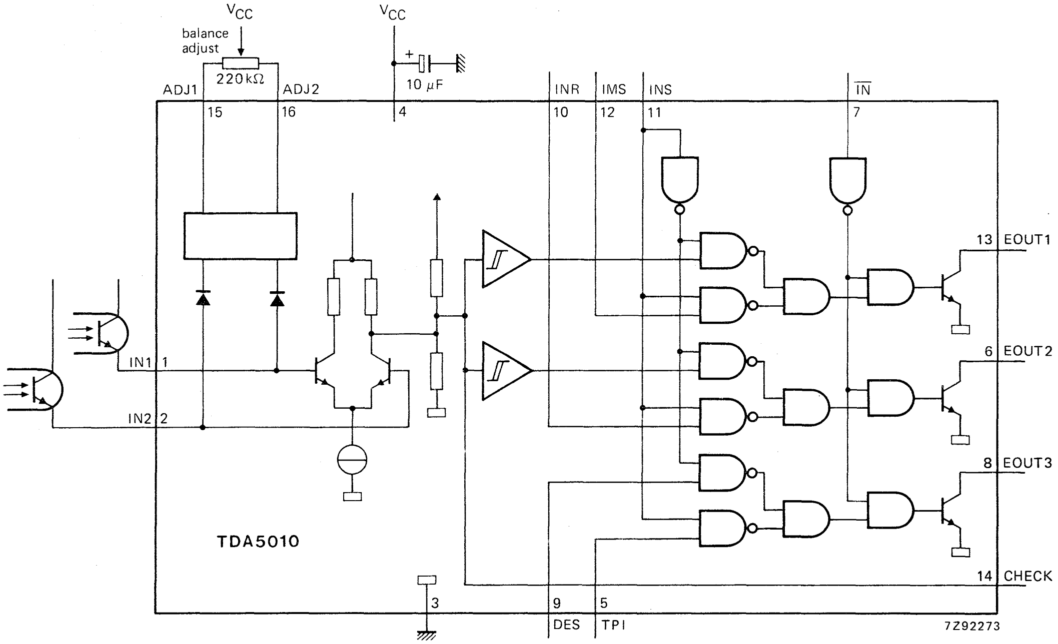
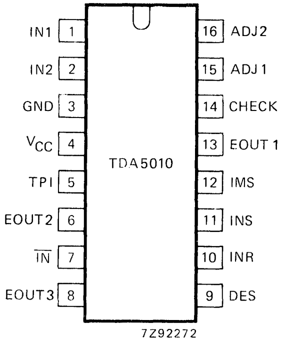


Fig. 1 Functional diagram.

PINNING



1	IN1	current input 1
2	IN2	current input 2
3	GND	ground
4	V_{CC}	positive supply
5	TPI	logic input
6	EOUT2	expander output 2
7	IN	enable input
8	EOUT3	expander output 3
9	DES	logic input
10	INR	logic input
11	SWIT	switch input
12	IMS	logic input
13	EOUT1	expander output 1
14	CHECK	check output
15	ADJ1	balance adjustment 1
16	ADJ2	balance adjustment 2

DEVELOPMENT SAMPLE DATA

FUNCTIONAL DESCRIPTION

The logarithm of the two input currents coming out of the two light barriers is obtained by use of two diodes and is fed to a differential antilog amplifier. Because the amplifier shows on its output the difference of the log of the input currents the output is proportional to the ratio of the two input currents.

To suppress the sensitivity difference of the light barriers a balance adjusment at the input of the differential amplifier is used. The signal is then admitted to two Schmitt-trigger circuits which detect the "ON" and "OFF" case and add a small hysteresis to increase switching safety. The signal is then fed to a logic expander with an enable input, which can also be used for other switching functions in combination with an external microprocessor control.

TRUTH TABLE

inputs							outputs		
7	11	5	9	11	12	1 – 2	6	8	13
H	X	X	X	X	X	X	H	H	H
L	L	X	X	X	X	$I_1 = I_2$	H	X	L
L	L	X	X	X	X	$I_1 > I_2$	L	X	L
L	L	X	X	X	X	$I_1 < I_2$	H	X	H
L	H	X	X	H	X	X	H	X	X
L	H	X	X	L	X	X	L	X	X
L	H	X	X	X	H	X	X	X	H
L	H	X	X	X	L	X	X	X	L
L	H	H	X	X	X	X	X	H	X
L	H	L	X	X	X	X	X	L	X
L	L	X	H	X	X	X	X	H	X
L	L	X	L	X	X	X	X	L	X

Positive logic:
H = HIGH state = 1
(the more positive voltage)
L = LOW state = 0
(the less positive voltage)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	13,2	V
Power dissipation	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	−25 to + 150		°C
Operating ambient temperature	T_{amb}	+ 5 to + 70		°C

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C		min.	typ.	max.	
Supply voltage	V_{CC}	4,75	5	9	V
Supply current	I_{CC}	–	1	2	mA
Input amplifier					
Input current	$I_{1,2}$	–	–	10	mA
Input current for proper current divide function	$I_{1,2}$	16	–	1200	μA
Balance adjustment*					
I_i = 16 to 1200 μA		2	–	–	
after offset adjustment; pins 7 and 11 LOW; no change at pins 6 and 13					
with I_1 = 50 μA	I_2/I_1	–	–	2	
with I_2 = 50 μA	I_1/I_2	–	–	2	
pins 6 and 13 react according truth table					
with I_1 = 100 μA	I_2/I_1	4	–	–	
with I_2 = 100 μA	I_1/I_2	4	–	–	
Schmitt trigger					
Threshold voltage HIGH (pins 14 and 6)	V_{14}	3,4	3,75	4,1	V
Threshold voltage LOW (pins 14 and 13)	V_{14}	1,9	2,1	2,3	V
Hysteresis (pin 14) upper and lower trigger	V_{14}	0,08	0,12	0,16	V
Logic inputs (Pins 5, 7, 9, 10, 11 and 12)					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2	–	13	V
Input current					
V_i = 0 V	$I_{5,7,10,11}$	–	0,5	1,2	μA
V_i = 0 V	$I_{9,12}$	–	1	2,4	μA
Logic outputs (Pins 6, 8 and 13)					
Output voltage LOW					
I = 2 mA	V_{OL}	–	–	0,45	V
Output voltage HIGH					
I = 50 μA	V_{OH}	2,4	V_{CC}	–	V
Output leakage current					
$V_+ > V_i > +0,45$ V	I_o	–	–	−10	μA
Delay time at V_{CC} = 4,75 V; T_{amb} = 5 °C					
pins 5, 9, 10, 11, 12 to outputs 6, 8 and 13	t_d	–	–	5	μs
pin 7 to outputs 6, 8 and 13	t_d	–	–	3	μs

* Range expressed in input current quotient.

V.H.F. MIXER/OSCILLATOR CIRCUIT

GENERAL DESCRIPTION

The TDA5030 performs the v.h.f. mixer, v.h.f. oscillator; SAW filter i.f. amplifier and u.h.f. i.f. amplifier functions in television tuners.

Functions:

- A balanced v.h.f. mixer
- An amplitude-controlled v.h.f. local oscillator
- A surface accoustic wave filter i.f. amplifier
- A u.h.f. i.f. preamplifier
- A buffer stage for driving an external prescaler with the local oscillator signal
- A voltage stabilizer
- A u.h.f./v.h.f. switching circuit

QUICK REFERENCE DATA

Supply voltage (pin 15)	V_F	10	to	13,2	V
Supply current	I_P			42	mA
Frequency range v.h.f. mixer	f	50	to	470	MHz
Storage temperature	T_{stg}	−55	to	+125	°C
Operating ambient temperature	T_{amb}	−25	to	+85	°C

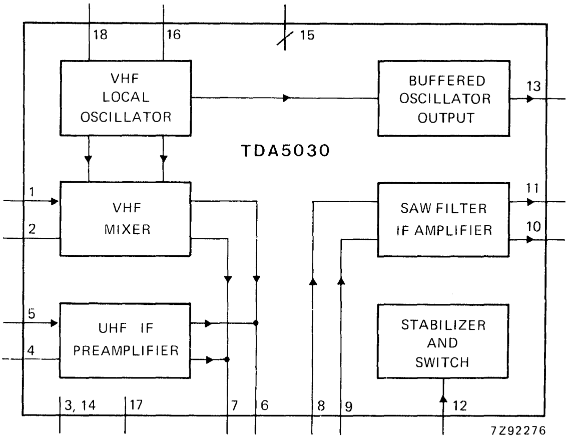


Fig. 1 Block diagram.

PACKAGE OUTLINE

18-lead DIL, plastic (SOT-102HE4).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	V_P	max.	14 V
Input voltage (pins 1, 2, 4 and 5)	V_i	0 to	5 V
Switching voltage (pin 12)	V_{12}	0 to	14 V
Output currents	$-I_{10,11,13}$	max.	10 mA
Short-circuit time on outputs (pins 10 and 11)	t_{ss}	max.	10 s
Storage temperature	T_{stg}	−55 to	+125 °C
Operating ambient temperature	T_{amb}	−25 to	+85 °C
Junction temperature	T_j	max.	+125 °C

CHARACTERISTICS

Measured in circuit of Fig. 2; $V_P = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	$V_{15\text{-}3}$	10	–	13,2	V
Supply current	I_{15}	–	42	55	mA
Switching voltage v.h.f.	V_{12}	0	–	2,5	V
Switching voltage u.h.f.	V_{12}	9,5	–	13,2	V
Switching current u.h.f.	I_{12}	–	–	0,7	mA
V.H.F. mixer (including i.f. amplifier)					
Frequency range	f	50	–	470	MHz
Input conductance 50 MHz	G_1	–	0,5	–	mS
Input capacitance 50 MHz	C_i	–	3	–	pF
Noise figure					
50 MHz	F	–	–	9	dB
200 MHz	F	–	–	9	dB
300 MHz	F	–	–	10	dB
470 MHz	F	–	–	11	dB
Input voltage for 1% cross-modulation (in channel); $R_p > 1$ kΩ; tuned circuit with $C_P = 22$ pF; $f_{res} = 36$ MHz	$V_{1\text{-}14}$	100	–	–	dBμV
Input voltage for 10 kHz pulling (in channel) at < 300 MHz	$V_{1\text{-}14}$	100	–	–	dBμV
Voltage gain	A_V	23	25	27	dB

parameter	symbol	min.	typ.	max.	unit
U.H.F. preamplifier (including i.f. amplifier)					
Input conductance	G_5	–	0,5	–	mS
Input capacitance	C_5	–	3	–	pF
Noise figure	F	–	–	6	dB
Input voltage for 1% cross-modulation (in channel)	$V_{5\text{-}14}$	91	–	–	dBμV
Voltage gain	A_v	32	34	36	dB
Optimum source admittance	G_5	–	3,3	–	mS
V.H.F. mixer					
Conversion transadmittance	$S_{c1\text{-}6,7}$	–	5,7	–	mS
Output impedance	Z_o	–	1,6	–	kΩ
V.H.F. oscillator					
Frequency range	f	70	–	520	MHz
Frequency shift ΔV_b = 10%; 70 to 330 MHz	Δf	–	–	200	kHz
Frequency drift ΔT = 15 K; 70 to 330 MHz	Δf	–	–	250	kHz
Frequency drift from 5 s to 15 min after switching on	Δf	–	–	200	kHz
V.H.F. local oscillator buffer stage					
Output voltage R_L = 75 Ω	V_{13}	10	20	–	mV
Output impedance f = 100 MHz	Z_{13}	–	130	–	Ω
SAW filter i.f. amplifier					
Input impedance $Z_{10,11}$ = 2 kΩ, f = 36 MHz	$Z_{8,9}$	–	220+j40	–	Ω
Transimpedance	$Z_{8,9\text{-}10,11}$	–	3,3	–	kΩ
Output impedance $Z_{8,9}$ = 1,6 kΩ; f = 36 MHz	$Z_{10,11}$	–	25+j20	–	Ω

DEVELOPMENT SAMPLE DATA

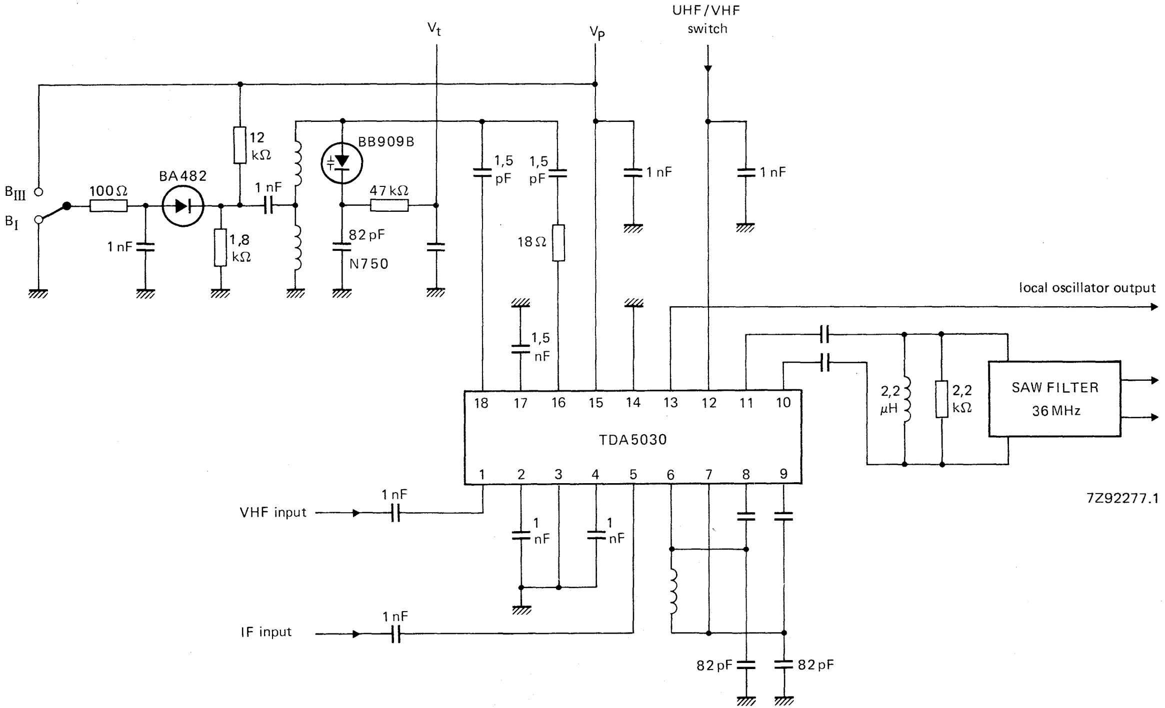


Fig. 2 Test circuit.

PAL COLOUR ENCODER AND VIDEO SUMMER

The TEA1002 is mainly intended for video games, add-on teletext applications and colour bar generators for video test equipment. It is a bipolar integrated circuit which converts binary colour information into a PAL composite video output suitable for driving a v.h.f./u.h.f. modulator.

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10\text{-}16}$	nom.	12 V
Supply current at V_P = 12 V	$I_P = I_{10}$	typ.	70 mA
Input voltages (pins, 1, 2, 3, 4, 5, 12, 15, 18)			
LOW	V_{IL}	$\leqslant$	0,8 V
HIGH	V_{IH}	$\geqslant$	2,0 V
Composite video output voltage (pin 8)			
peak-to-peak value	$V_{8\text{-}16(p\text{-}p)}$	typ.	3 V
Operating ambient temperature range	T_{amb}		−20 to +65 °C

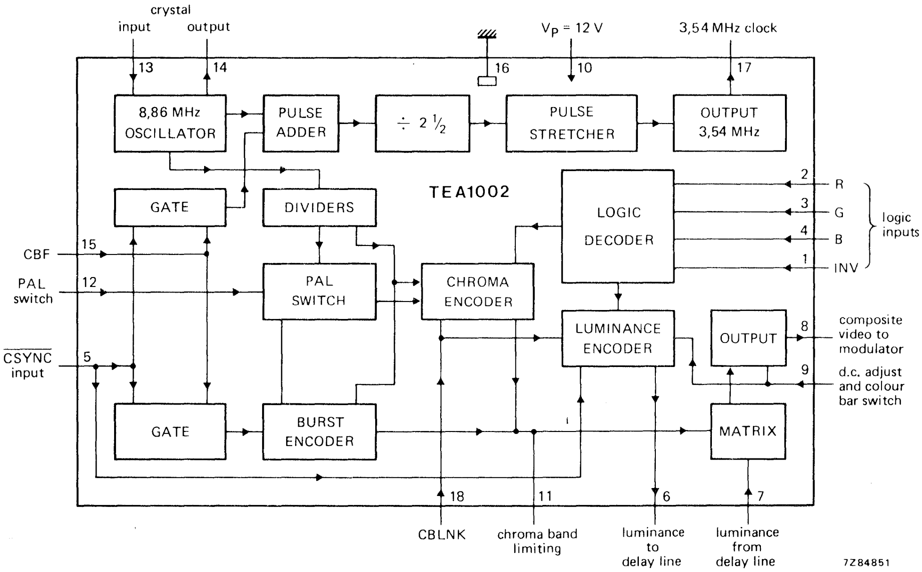


Fig. 1 Block diagram.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

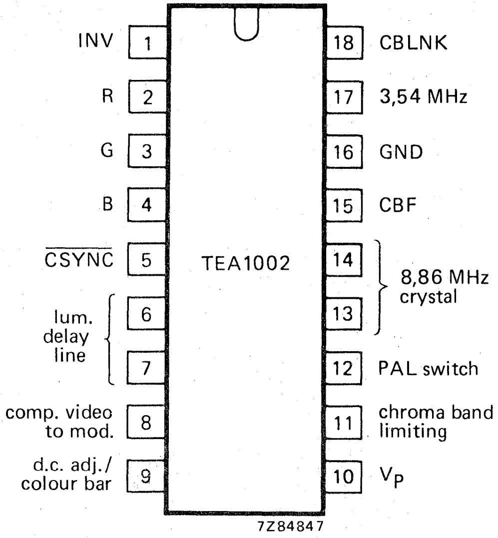


Fig. 2 Pinning diagram.

PINNING

1	INV	inverting logic input	
2	R	red logic input	
3	G	green logic input	
4	B	blue logic input	
5	$\overline{\text{CSYNC}}$	composite sync input	
6	luminance output to delay line		
7	luminance input from delay line		
8	composite video output to modulator		
9	d.c. adjust and colour bar switch		
10	V_P	supply voltage (+ 12 V)	
11	chroma band limiting		
12	PAL switch input		
13	crystal input		8,86 MHz
14	crystal output		
15	CBF	colour burst flag input	
16	GND	ground	
17	3,54 MHz	clock output	
18	CBLNK	composite blanking input	

GENERAL DESCRIPTION

The TEA1002 PAL colour encoder and video summer IC has an internal 8,86 MHz oscillator from which the 4,43 MHz (R-Y) and B-Y) waveforms are generated. For use in TV games systems, a 3,54 MHz clock output is provided which is buffered via the 2621 sync generator IC. The TEA1002 accepts timing signals (composite sync burst gate, PAL switch and composite blanking) from the 2621 and 4-bit binary coded logic inputs giving colour information from the 2636 programmable video interface IC. The resulting output, which has an adjustable d.c. level, is a 16 colour (including black and white) composite video signal, based on 75% colour bars. Alternatively, with one of the colour inputs connected to ground and the d.c. adjustment disabled, the TEA1002 can be used as a general purpose video encoder providing standard 95% colour bars from RGB logic inputs, suitable for applications such as add-on teletext.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 10)	$V_P = V_{10\text{-}16}$	max.	13,2	V
Input voltage (pins 1, 2, 3, 4, 5, 12, 15, 18) HIGH	V_{IH}	max.	V_P	V
Storage temperature range	T_{stg}		−25 to + 125	^oC
Operating ambient temperature range	T_{amb}		−20 to +65	^oC

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; measured in Fig. 8; unless otherwise specified

		min.	typ.	max.	
Supply voltage	$V_P = V_{10\text{-}16}$	10,8	12	13,2	V
Supply current	$I_P = I_{10}$	–	70	–	mA
Clock output (pin 17) (notes 1 and 2, Fig. 6)					
Clock cycle time	T	–	282	–	ns
Output voltage (peak-to-peak value) measured into 30 pF load capacitance	$V_{17\text{-}16(p\text{-}p)}$	4	–	6	V
Output rise time into 30 pF load	t_r	–	4	30	ns
Output fall time into 30 pF load	t_f	–	10	30	ns
Clock pulse width LOW measured at + 0,8 V after restoration	t_L	100	140	–	ns
Clock pulse width HIGH measured at + 2,4 V after restoration	t_H	100	130	–	ns
Oscillator stability (pins 13, 14) (notes 3 and 4)					
Variation in internal 4,43 MHz reference clock frequency					
temperature range: –20 to + 25 °C	$\Delta f_{osc}/\Delta T$	–	–0,8	–	Hz/K
+ 25 to + 70 °C	$\Delta f_{osc}/\Delta T$	–	–2,6	–	Hz/K
supply voltage range: 10,8 to 13,2 V	$\Delta f_{osc}/\Delta V_P$	–	–25	–	Hz/V
Timing inputs (pins 5, 12, 15, 18) (Fig. 3)					
Input voltage LOW	V_{IL}	–	–	0,8	V
Input voltage HIGH	V_{IH}	2	–	V_P	V
Input current LOW (d.c.); V_I = 0 V	I_{IL}	–	–	100	µA
Input current HIGH (d.c.); V_I = 12 V	I_{IH}	–	–	100	µA
Input capacitance	C_I	–	–	10	pF
Input rise and fall times	t_r, t_f	–	–	200	ns
Colour code inputs (pins 1, 2, 3, 4) (note 6)					
Input voltage LOW	V_{IL}	–	–	0,8	V
Input voltage HIGH	V_{IH}	2	–	V_P	V
Input current LOW (d.c.); V_I = 0 V	I_{IL}	–	–	100	µA
Input current HIGH (d.c.); V_I = 12 V	I_{IH}	–	–	100	µA
Input capacitance	C_I	–	–	10	pF

CHARACTERISTICS (continued)

Composite video output (pin 8) (note 5, Table 1)		min.	typ.	max.	
Output voltage (peak-to-peak value) sync tip to white	$V_{8\text{-}16(p\text{-}p)}$	–	3	–	V
Residual chroma voltage on white (r.m.s. value) (4,43 MHz)	$V_{8\text{-}16(rms)}$	–	30	–	mV
Sync tip d.c. levels for $V_{9\text{-}16} = 12$ V	$V_{8\text{-}16}$	–	5,1	–	V
for $V_{9\text{-}16} < 9$ V	$V_{8\text{-}16}$	–	2,6	–	V
D.C. output adjustment (pin 9)					
D.C. adjustment voltage range where $\Delta V_{8\text{-}16} = \Delta V_{9\text{-}16}$	$V_{9\text{-}16}$	9,5	–	12	V
Applied voltages to guarantee 75% colour bars	$V_{9\text{-}16}$	4	–	–	V
95% colour bars	$V_{9\text{-}16}$	–	–	3	V
Chroma band limiting (pin 11)					
Internal impedance at pin 11	$\lvert Z_i \rvert$	–	1,5	–	kΩ

Notes

1. This circuit assumes capacitive coupling to the N-MOS games IC (see Fig. 5).
2. The integrated circuit gates the CBF and CSYNC signals to provide a 'frame offset' which lengthens two clock periods by 56 ns every field. This provides a subcarrier/line frequency relationship of $f_{sc} = 283\tfrac{3}{4} f_l + 25$ Hz which gives an optimum picture response.
3. These figures hold for a typical quartz crystal as specified below:
   Crystal catalogue no. 4322 143 04051, used in series with 20 pF trimmer capacitance (C_L).
   motional resistance (R1): typ. 15 Ω; max. 60 Ω
   static capacitance (C0): typ. 5 pF; max. 6 pF.
4. These figures exclude the temperature dependence of the crystal and load capacitance (C_L).
5. The chroma/luminance phase inequality can be compensated by an external delay line connected between pins 6 and 7 (see Fig. 8).
   For measurements on the composite video output use the circuit as shown in Fig. 7.
6. To generate standard colour bar signals, pin 1 must be grounded externally.

APPLICATION INFORMATION

The function is described against the corresponding pin number

1. **Inverting logic input**

   When this pin is connected to ground, the logic inputs on pins 2, 3 and 4 are decoded as R, G and B respectively and the chrominance signal at the output is at its full amplitude. If this pin is taken HIGH (> 2 V) the logic inputs are decoded as $\overline{R}$, $\overline{G}$ and $\overline{B}$ and the chrominance signal is reduced to half its full amplitude (see Table 1).

2, 3, 4. **Red, green and blue logic inputs**

5. **Composite sync input**

   This pin requires a negative logic composite sync signal (CSYNC). The signal is also gated with CBF to control a frame offset phase adjustment for the 3,54 MHz clock (see pins 13 and 14).

6, 7. **Luminance delay line**

The combined luminance and sync signal appearing at pin 6 must be d.c. coupled to pin 7 via an appropriate luminance delay line or resistor network. The resistors must have a tolerance of ± 5% (see Fig. 7).

8. **Composite video output**

The output is internally buffered by an emitter follower stage giving a nominal output voltage of 3 V sync-white. The d.c. level is temperature compensated and can be continuously adjusted over a nominally 2,5 V range via an input on pin 9.

9. **D.C. adjustment and colour bar switch**

This pin provides the dual function of d.c. level adjustment for the composite video output stage and colour bar standard selection. An adjustment of $V_{9\text{-}16}$ from 9,5 V to 12 V will cause a corresponding change of output sync tip level from 3 V to 5,5 V (nominal values).

With $V_{9\text{-}16} \geqslant 4$ V the luminance levels are set to give 75% (E.B.U.) colour signals when using the RGB inputs with pin 1 grounded. With $V_{9\text{-}16} \leqslant 3$ V the output levels will be changed to give 95% (B.B.C.) colour signals (see Table 1). Thus d.c. adjustment can only be obtained with 75% colours.

10. **Supply voltage** (+ 12 V)

11. **Chroma band limiting**

This pin is connected internally to the chrominance summing junction and may be used to limit the bandwidth of the chroma signal by connecting it to a 4,43 MHz tuned filter via a blocking capacitor. The internal impedance is nominally 1,5 kΩ. If a filter is used at this point, then the delay of the chroma signals must be compensated by an appropriate luminance delay line between pins 6 and 7.

12. **PAL switch**

This pin requires a logic signal at half line frequency to control the phase of the (R-Y) modulator and the burst signal.

13, 14. **8,86 MHz crystal**

An 8,867238 MHz crystal in series with a trimmer capacitor is connected between these pins to form part of an oscillator. The output of the oscillator is divided to provide the four subcarrier phases required in the encoder.

The 8,86 MHz signal is also divided by 2½ to give a 3,54 MHz clock input to the 2621 sync generator IC. A phase correction is made after every field to ensure the correct subcarrier to line frequency relationship.

15. **Colour burst flag**

This pin requires a positive logic signal to enable the colour burst encoder.

16. **Ground** (0 V)

17. **Clock output**

The 3,54 MHz clock signal from this pin must be a.c. coupled to the 2621 sync generator IC.

18. **Composite blanking**

This pin requires a positive logic composite blanking signal. The colour logic inputs at pins 1 to 4 are gated to logic '0' when this input is HIGH.

APPLICATION INFORMATION (continued)

Table 1. Logic inputs and composite video output

	inputs				colour	nominal outputs			
	pin 2 R	pin 3 G	pin 4 B	pin 1 INV		luminance $V_{9-16} \geqslant 4$ V (%)	luminance $V_{9-16} \leqslant 3$ V (%)	chroma phase (degrees)	chroma amplitude (% black-white)
1	0	0	0	0	black	0 75% (E.B.U.) colour bars	0 95% (B.B.C.) colour bars	–	–
2	1	0	0	0	red	22,5	47,5	103	± 48
3	0	1	0	0	green	44	69	241	± 44
4	1	1	0	0	yellow	66,5	91,5	167	± 33
5	0	0	1	0	blue	8,5	33,5	347	± 33
6	1	0	1	0	magenta	31	56	61	± 44
7	0	1	1	0	cyan	52,5	77,5	283	± 48
8	1	1	1	0	white	100	100	–	–
9	0	0	0	1	grey	75	100	–	–
10	1	0	0	1	cyan	52,5	77,5	283	± 24
11	0	1	0	1	magenta	31	56	61	± 22
12	1	1	0	1	blue	8,5	33,5	347	± 17
13	0	0	1	1	yellow	66,5	91,5	167	± 17
14	1	0	1	1	green	44	69	241	± 22
15	0	1	1	1	red	22,5	47,5	103	± 24
16	1	1	1	1	black	0	0	–	–

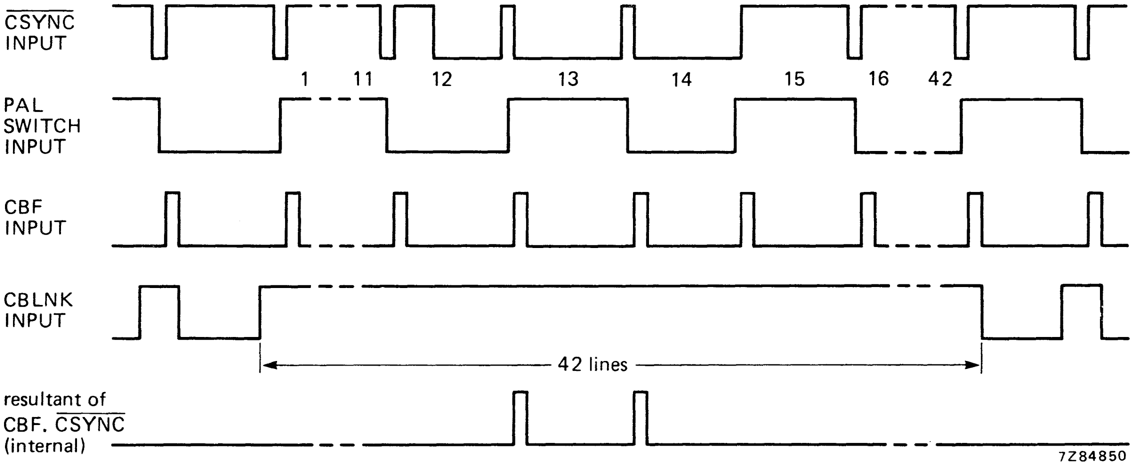


Fig. 3 Timing diagram (signals supplied from sync generator IC).

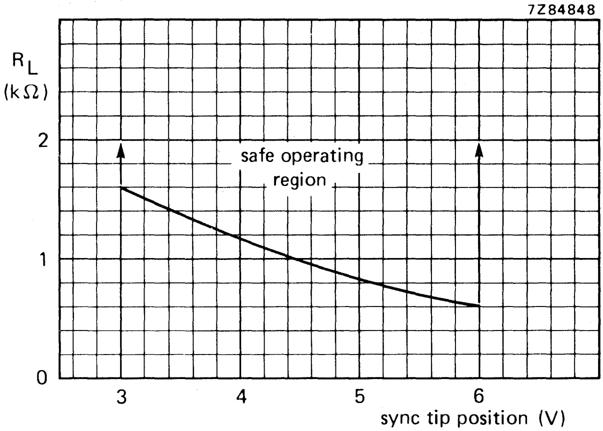


Fig. 4 Safe operating area for load resistor (R_L) at pin 8 as a function of sync tip d.c. position.

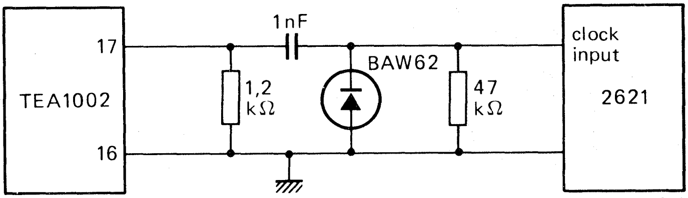


Fig. 5 Clock coupling circuit.

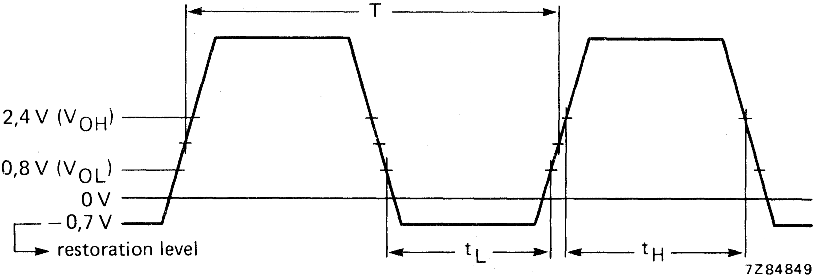


Fig. 6 Clock output waveform at pin 17 to the input of the 2621.

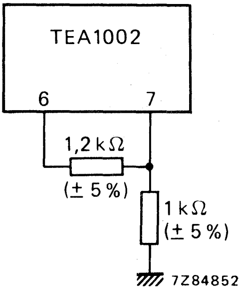
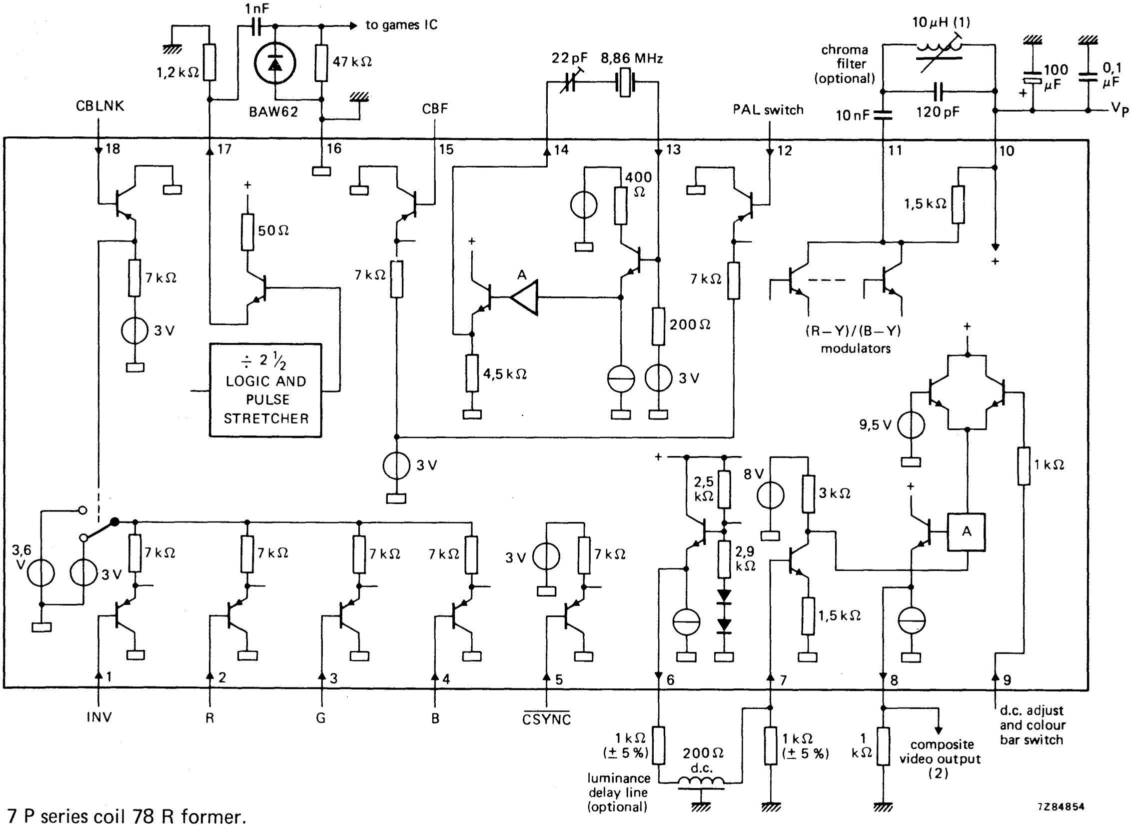


Fig. 7 Connections for pins 6 and 7 when no luminance delay line is used.



(1) TOKO 7 P series coil 78 R former.

(2) See derating curve Fig. 4.

Fig. 8 Internal circuit details and typical external connections.

NOTES

NOTES

NOTES

BIPOLAR ICs FOR VIDEO EQUIPMENT