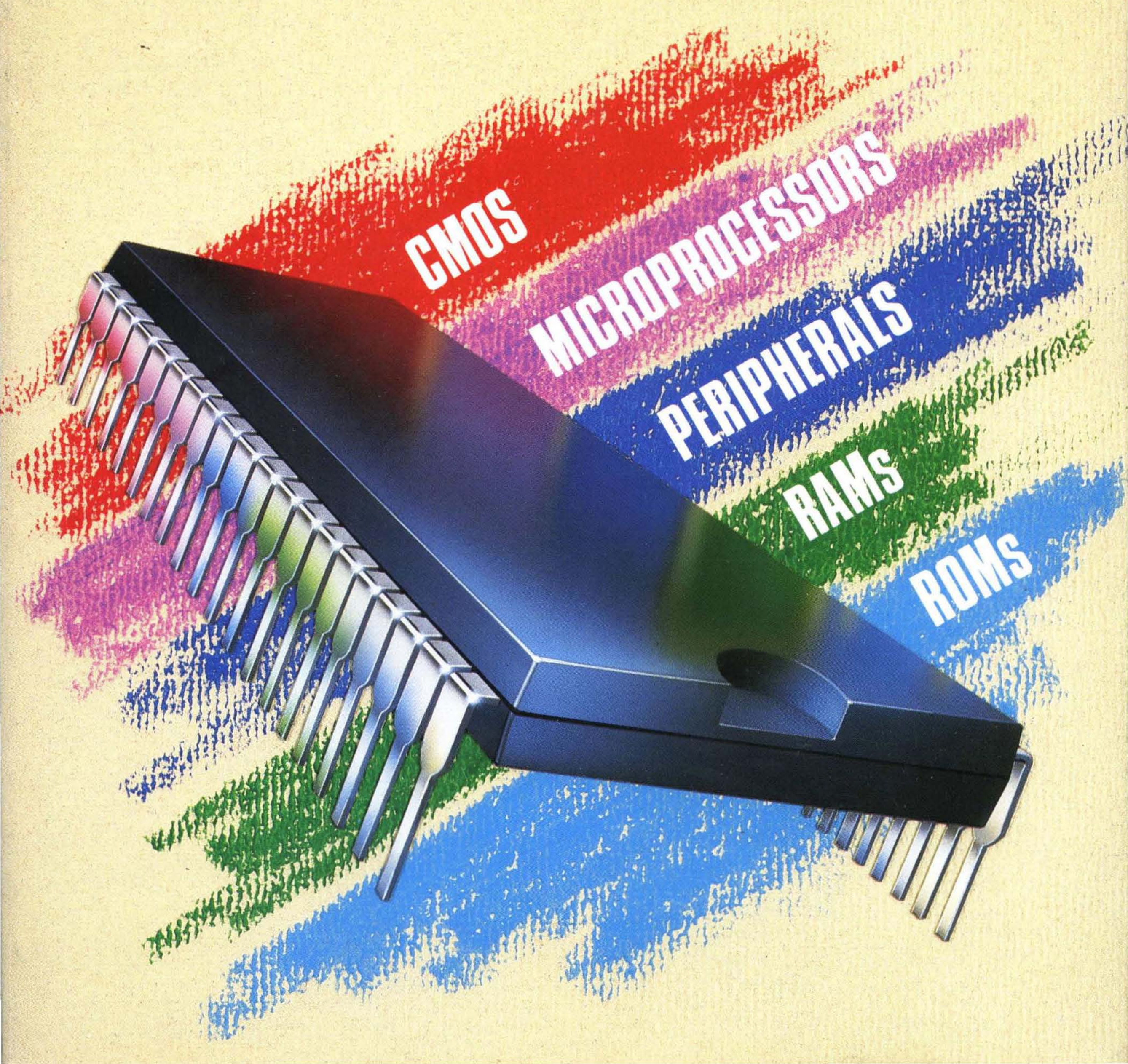
GE

WYLE LABORATORIES ELECTRONICS MARKETING GROUP

GE Solid State Data Book



RCA CMOS
Microprocessors, Memories, and Peripherals

This DATABOOK contains detailed information on CMOS microprocessors, microcomputers, memories, and peripherals currently available from GE Solid State, a division of GE Corporation. GE Solid State is a consolidation of the strengths of three broad-based semiconductor suppliers—GE Semiconductor, RCA Solid State and Intersil—that formerly operated as separate, independent organizations.

An Index to Products provides a complete listing of types. Following the Index to Products are several pages of general product information that include a Product Classification Chart that groups integrated circuits and systems according to product type and intended function; photographs showing available package options; a Product Overview that summarizes the basic features of each category of products; and a description of the Enhanced Product. The DATABOOK then includes a general discussion of Operating and Handling Considerations for CMOS Integrated Circuits.

Five separate data sections provide definitive ratings, electrical characteristics, and user information for the (1) 1800-Series Microprocessors and Microcomputers, (2) 6805-Series Microprocessors and Microcomputers, (3) CMOS Peripherals, (4) CMOS Random-Access Memories (RAMs), and (5) CMOS Read-Only Memories (ROMs). Within each data section, data pages for individual integrated circuits and systems are grouped in alphanumerical sequence by type numbers.

A section on CMOS LSI High-Reliability Devices provides a description of non-radiation-hardened CMOS LSI devices and radiation-hardened CMOS/SOS LSI RAMs with a list of devices available.

The DATABOOK also contains Dimensional Outlines of all packages in which memory/microprocessor products are supplied and a list of Application Notes on memory/microprocessor products.

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GE Solid State

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GE/RCA/Intersil Semiconductors

The device data shown for some types are indicated as product preview or advance information. **Product preview** data are intended for engineering evaluation of product under development. The type designations and data are subject to change or withdrawal, unless otherwise arranged. **Advance information data** are intended for guidance purposes in evaluating new product for equipment design. Such data are shown for types currently being designed for inclusion in our standard line of commercially available products. No obligations are assumed for notice of change of these devices. For current information on the status of product preview or advance information data programs, please contact your local GE sales office.

Printed in USA/12-87

Guide to Products

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CDP68EM05C4	8-Bit Microcomputer Piggyback Emulator	351	1961
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CDP6818A	Real-Time Clock Plus RAM	579	2041
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Product Classification Chart

Microprocessors

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CDP1823,C	128 x 8	660
CDP1824,C	32 x 8	666
CDP1826C	64 x 8	671
CDM6116A	2K x 8	636
CDM6264	8K x 8	642
CDM62256	32 x 8	722
MWS5101	256 x 4	686
MWS5101A	256 x 4	692
MWS5114	1K x 4	698
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Part Number	Description	Page No.
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CDM5333	4K x 8	705
CDM5364,A	8K x 8	709
CDM5365	8K x 8	714
CDM53128	16K x 8	718
CDM53256	32K x 8	722
CDP1831,C	512 x 8	726
CDP1832,C	512 x 8	730
CDP1833,C,BC	1K x 8	734
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CDP1883,C	7-Bit Latch & Decoder	474
CDP1854A,AC	Programmable UART	387
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CDP65C51	Asynchronous Communications Interface Adapter	487
CDP65C51A	Asynchronous Communications Interface Adapter	503
CDP6853	Asynchronous Communications Interface Adapter, (ACIA), MOTEL Bus	612
CDP1855,C	8-Bit Programmable Multiply/ Divide Unit (MDU)	404
CDP1871A,AC	Keyboard Encoder, ASCII Hex	417
CDP1878,C	Dual Counter/Timer	439
CDP1879,C-1	Real-Time Clock	452
CDP6818	Real-Time Clock with RAM, MOTEL Bus	560
CDP6818A	Real-Time Clock Plus RAM	579
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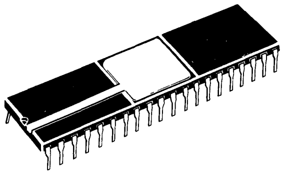
Package and Ordering Information

Packages

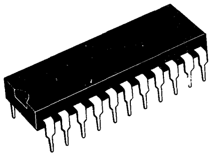
RCA CMOS microprocessor and memory integrated circuits are available in one or more of the following package styles and are identified by the Suffix Letters indicated: dual-in-line side-brazed ceramic, dual-in-line plastic, small-outline plastic, plastic chip-carrier, and in chip form. The available package styles for any specific type are given in the technical data for that type.

D Suffix
Dual-In-Line Side-Brazed Ceramic Packages



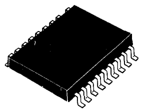
16-, 18-, 22-, 24-, 28-, and 40-lead versions

E Suffix
Plastic Dual-In-Line Packages



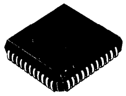
8-, 16-, 18-, 20-, 22-, 24-, 28-, and 40-lead versions

M Suffix
Small-Outline Plastic Package (SO)



16-, 20-, and 28-lead versions

Q Suffix
Plastic Chip-Carrier



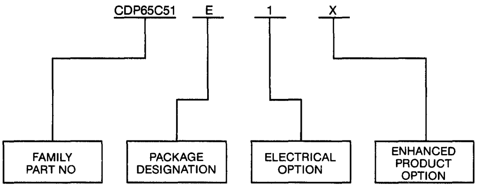
28- and 44-lead version

Ordering Information

The RCA family packages and electrical options are identified by suffix letters indicated in the following chart. When ordering a Memory/Microprocessor device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package/Option	Suffix Letter
Dual-In-Line Side-Brazed Ceramic	D
Dual-In-Line Plastic	E
Small-Outline Plastic (SOP)	M
Plastic Chip-Carrier	Q
Chip (when applicable)	H
Enhanced Product Screening i.e., Burn-In - optional for D, E package types	X
Electrical Option	1, 2, 4

For example, a CDP65C51-1 in a dual-in-line plastic package will be identified as the CDP65C51E1. A CDP65C51E1 with enhanced product screening option will be identified as the CDP65C51E1X.



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Package and Ordering Information

Instructions for Submitting Data for ROM Patterns

Data Format Options

Data for RCA ROMs or microcomputers should be submitted in one of the following forms.

1. Any industry-standard EPROM or ROM that is pin and polarity compatible with industry-standard 27XXX-series EPROMs.
2. IBM PC 5¼-inch floppy diskette (data must be in Motorola "S" format)
3. GE worldwide electronic data transfer system

Regardless of the media on which the data is submitted, the entire address range of the ROM being requested must be covered, even if a portion of it is not being used. This restriction also applies to microcomputers. For example, a CDP5332 requires 4k bytes of EPROM, a CDP68HC05C4, 8K bytes.

Procedure for Submitting Data

A. By EPROM, ROM or floppy diskette:
   1. Complete the application ROM and microcomputer information sheet. (Contact the nearest GE Solid State Sales Office for appropriate forms).
   2. Submit the data as described above.
   3. Include a set of blank EPROMs that will cover the memory space of your ROM or microcomputer. These EPROMs will be returned to you.
   4 When the EPROMs have been returned, confirm that the code is correct, and respond to GE Solid State by completing the ROM verification form. (Included with return of EPROM.)
   5. NOTE—GE Solid State will add the latest self-check code in the memory areas of the Address map shown on the applicable data sheet on the CDP6805-series and CDP68HC05-series microcomputers. On all devices except the CDP6805F2, GE Solid State will assign a three-character variant code to the device and will add the ASCII equivalent of it to the ROM area. On the G2, this code is entered in locations 1FF2, 1FF3 and 1FF4; on the C4 in locations 1FF0, 1FF1, and 1FF2; and on the D2 in locations 1FE6, 1FF0, and 1FF1. GE Solid State also calculates a checksum byte of the entire ROM area, that is, the user ROM, self-check area, and the vector area. The checksum is the EXCLUIVE-OR of all the ROM bytes with hex FF. This byte is put in location 07F5 on the F2, 1FF5 on the G2, 1FF3 on the C4, and 1FE7 on the D2.

B. By electronic data transfer:
   Contact the nearest GE Solid State Sales Office for procedure.

Product Overview

An all CMOS line of microprocessor, microcomputer, memory, and peripheral integrated circuits for use in a broad range of diverse industrial, consumer, and military applications is available from GE Solid State. These devices offer the user all the advantages unique to CMOS technology, including:

- **Low power drain** — makes CMOS integrated circuits a natural choice for battery-operated systems, battery backed-up systems, and systems in which heat dissipation is a prime consideration.
- **High noise immunity and wide operating temperature range (up to -55°C to +125°C)*** — allows CMOS integrated circuits to be used in the most demanding industrial environments.
- **Wide operating voltage range** — reduces the need for expensive regulated power supplies and there-by allows the design engineer greater freedom to concentrate on other aspects of system design.

CDP1800 Series

The RCA CDP1800 series offers a complete line of CMOS microprocessor, microcomputer and associated memory and peripheral devices. The heart of the series is the CDP1802A central processing unti (CPU). This unit, which features CMOS register-based architecture, offers 16 internal registers to facilitate data manipulation and to reduce the need for additional devices The need for external devices is even further reduced by use of on-chip clock, DMA, and single phase operation.

The CDP1804A microcomputer incorporates all the features of the CDP1802A augmented by additional hardware and increased performance capabilities. The additional on-chip hardware enhancements include 2-kilobytes of ROM, a 64-byte RAM array, and an 8-bit presettable down-counter. Thirty-two additional software instructions add subroutine call and return capability, enhance data transfer manipulation, control counter modes and interrupt arbitration and provide BCD arithmetic capability.

Also available, are two other 8-bit microprocessors that are functional and performance enhancements of the CDP1802A. The CDP1805A features an on-board RAM and Counter/Timer. The CDP1806A has all the features of the CDP1805A, but contains no on-board RAM.

The microprocessor and microcomputer devices use CMOS technology, designed on a single chip to maintain low power drain. They are intended for multi-system applications requiring general-purpose CPUs, large memory address space, and extensive external I/O for use with optimized peripherals.

The RCA CDP1800-series memory/microprocessor product line offers the system designer exceptional flexibility in hardware/software tradeoffs In addition to microprocessor and microcomputers, this product line includes a hardware multiply/divide unit (MDU), a programmable I/O, keyboard interface circuits, latches and decoders, universal asynchronous receiver-transmitters (UARTs), and a broad complement of directly interfaceable random-access memories (RAMs) and read-only memories (ROMs).

CDP6805 Series

The RCA CDP6805 family of CMOS microprocessors, microcomputers, and peripherals are primarily intended for single-chip system applications requiring limited space, minimum memory, on-board I/O, and minimum external I/O. The series offers pin-for-pin replacements for Motorola's MC146805, and MC68HC05 series of microprocessors, microcomputers, and peripherals. This family of parts includes the CDP6805E2 and CDP6805E3 8-bit microprocessors; the CDP6805F2 8-bit microcomputer (1K ROM); the CDP6805G2 8-bit microcomputer (2K ROM); the CDP68HC05C4, CDP68HC05C8, and CDP68HC05D2 8-bit microcomputers featuring on-chip ROM, RAM, 16-bit timer, asynchronous serial communications interface (CDP68HC05C4, and CDP68HC05C8), synchronous serial peripheral interface, and 24 or 28 bidirectional I/O lines; the CDP68HC68T1 Serial Real-Time Clock/ RAM; the CDP68HC68R1 and CDP68HC68R2 Serial Peripheral Interface (SPI) RAMs; the CDP68HC68A2 10-bit A/D Converter; the CDP68HC68P1 Serial I/O Port; the CDP6818 Real-Time Clock plus RAM; and the CDP6823 Parallel Interface I/O. Also available is the CDP6853 Asynchronous Communications Interface Adapter which is a multiplexed-bus version of our CDP65C51 UART.

Additional types will be added as they become available.

General-Purpose Memories

In addition to the memories designed to interface directly with CDP1800-series microprocessors and microcomputers, a line of general-purpose memories is also available. These memories include industry-standard ROMs that can be mask-programmed to meet customer application requirements. These ROMs feature: low-power CMOS technology with high-noise immunity and full-temperature-range characteristics; space-efficient NAND stack memory cells providing small chip size for cost effectiveness; and JEDEC standard pin outs for interchangeability with industry-standard NMO ROMs and EPROMs.

The list of memories also includes fully static CMOS RAMs with densities up to 32K-bytes, low operating power, low standby current, and memory retention for 2-volt minimum standby battery voltage.

Memory/Microprocessor Surface-Mounted Packages

The RCA CMOS memory/microprocessor product line now includes standard CDP- and CDM-series chips in a new generation of IC miniaturized packages.

Microprocessors, microcomputers, memories, and peripherals are now offered in two versions of the surface-mounted-package configuration as follows:

- **Small-outline package (SOP)**
- **Plastic chip-carrier (PCC)**

The small-outline package (SOP) will be offered in 16-, 20-, 24- and 28-lead versions with 50-mil lead centers; the plastic chip-carrier (PCC) will be offered as 28- or 44-lead packages with 50-mil lead centers.

Enhanced Product

Most RCA memory/microprocessor parts are available with burn-in to enhance commercial reliability. This cost-effective approach is provided by the RCA Enhanced Product. Enhanced product is identified with the suffix "X", e.g., CDP1802ACEX.

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*Maximum Rating

Enhanced Product

LSI Circuits

Burn-in Time*	160 Hours
Temperature*	125°C
Bias Voltage:	
CDP1800 "C" Product	7 V
All Other	6 V
CDP1800 "Non-C" Product	11 V

PRODUCT IDENTIFICATION

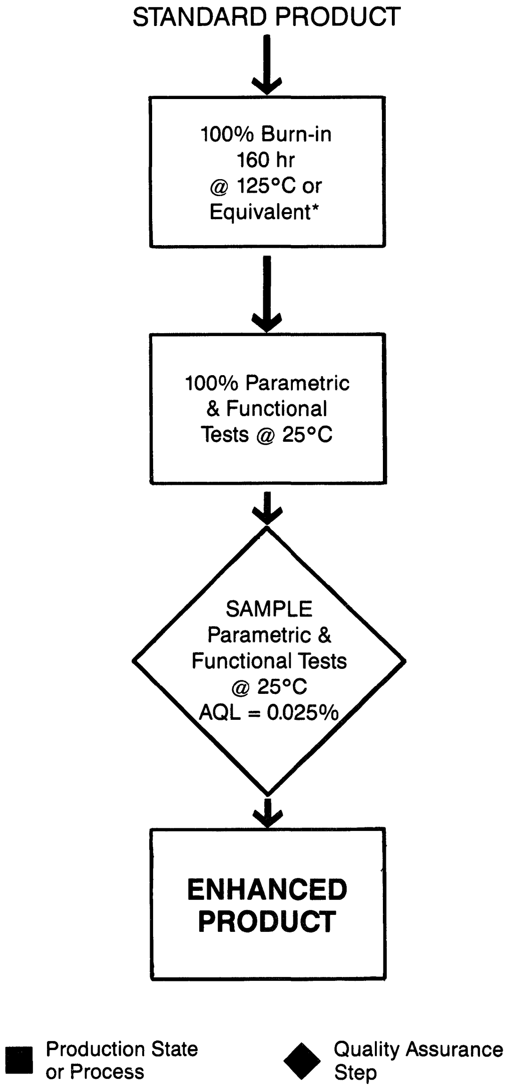
All enhanced product is identified by a suffix "x".

Examples:

Standard	Enhanced
CDP1854ACE	CDP1854ACEX
CDP6805G2E	CDP6805G2EX

*Or equivalent means equivalent time-temperature/voltage resulting in the same activation energy.

Product Flow


STANDARD PRODUCT
100% Burn-in 160 hr @ 125°C or Equivalent*
100% Parametric & Functional Tests @ 25°C
SAMPLE Parametric & Functional Tests @ 25°C AQL = 0.025%
ENHANCED PRODUCT
Production State or Process
Quality Assurance Step

Enhanced Product Application

The need to achieve the enhanced reliability resulting from burn-in screening must be determined by careful analysis of system design and application.

How many IC's are incorporated into the total system?

How many devices on each board?

Is the proper device being used for the application?

What are the reliability goals?

What failure rates are being experienced without screening?

Cost-effectiveness of using enhanced CMOS can be determined by mutual analysis of the economic trade-offs made possible by the following features of the program:

- Available in both plastic and frit-seal ceramic packages.
- Offered on the industry's broadest line of circuit functions.
- 0.025% AQL cumulative.
- Reduction in PC board reworking through fewer line rejects.
- Lower warranty requirements through the elimination of infant mortality failures.
- Reduced incoming inspection cost by reduction or complete elimination of test procedures.
- Reduction of system failures and related service expenses and customer complaints.

Enhanced Product Reliability Data

FAILURE RATES IN PLASTIC DUAL-IN-LINE PACKAGES

Product Category	Device Family	Temp (°C)	V_{DD} (V)	Equivalent Device Hrs.†	Failure Rate (FITs)* Standard No Burn-In	Failure Rate (FITs)* Burn-In (160 Hrs., 125°C)#
Memory/μP						
C^2L	CDP1800	85	7	2.4×10^7	160	67
	(RAM/ROM, I/O, μP)	55	7	4.6×10^8	8.3	3.5
CMOS I	CDP1800, CDP6805	85	6	9.2×10^7	170	71
	(RAM/ROM, μCOMP/μP)	55	6	1.8×10^9	8.8	3.7
CMOS II	ROMs Only	85	6	5.6×10^7	70	29
	(64K, 128K, 256K)	55	6	1.1×10^9	3.6	1.5

NOTES: * FITs are the number of failures in 10^9 device hours. The failure rate is estimated at 60% upper confidence level. To convert the above data from FITs to %/1000 hours, multiply by 10^{-4}.

† Equivalent device hours are extrapolated from accelerated test temperatures to the maximum 85°C rating and nominal use condition of 55°C, using a 1.0eV activation energy. Actual test temperatures ranged between 125°C-175°C.

# The difference in failure rate between standard and burned-in product is estimated from several sample studies.

Operating and Handling Considerations RCA CMOS Integrated Circuits

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid-state devices.

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

Absolute Maximum Ratings

The published ratings of GE, RCA, and Intersil Solid-State Devices are based on the Absolute-Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

> Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult GE Solid State whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

In general, with any application where devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

The metal shells of some solid-state devices such as the TO-5-style package often used for integrated circuits usually has the substrate or most negative supply voltage connected to the case. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device and result in destruction and/or possible shattering of the enclosure.

The small size of most solid-state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the device package. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces.

Thermal Considerations

The maximum allowable power dissipation in a solid-state device is limited by the junction temperature. An important factor in assuring that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid-state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data for the device. Thermal considerations require that a free flow of air around the device is always present and that the power dissipation be maintained below the level which would cause the junction temperature to rise above the maximum rating at the worst-case ambient temperature.

Electrostatic Voltage Discharge Considerations

Electrostatic voltage discharge of sufficient energy can damage any solid-state device. These electrical potentials can be significantly reduced during handling or testing by following industry-accepted practices such as those used by GE Solid State. These include:

- properly grounded equipment, workstations, operators and handlers
- the use of air ionizers
- control of ambient humidity
- device storage and transportation in a charge-dissipative medium such as "Eccosorb● LD26" or equivalent.

Mounting

Integrated circuits are normally supplied with tin-lead dipped leads to facilitate soldering into circuit boards.

When integrated circuits are welded onto printed-circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. When solder-dipped leads are formed, they must be reflowed or redipped within 40 mils of the package body. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

Many GE/RCA/Intersil semiconductor products are available in surface-mounted packages which enable the user to mount these devices directly on the surface of a circuit board. Unlike conventional dual-in-line (DIP) leaded packages which require through-holes for insertion, surface-mounted packages are soldered to a series of pads on a

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●Trade Name: Emerson and Cumming, Inc.

Operating and Handling Considerations

circuit board using a variety of acceptable techniques such as vapor phase or infrared reflow. This series of pads, commonly called a footprint, matches the lead or contact outline of the package(s) being used.

Recommended Lead-Forming Practices

DIC Packages

The leads on dual-in-line CERDIP or dual-in-line side-brazed packages are not intended to be bent or formed No further lead-forming is recommended.

Flat Packages

Flat packages including quad flat-packages are provided to users with the leads in a horizontal plane.

Since users form leads into many configurations, these relatively thin-leaded devices require a certain amount of care to avoid any handling which would affect the suitability of these leads.

Taking guidance from MIL-STD 4544, the following is recommended when bending leads:

a) the bend radius must exceed twice the lead thickness.
b) Always start the bending 0.015 inches or more away from the device body to protect body-to-lead adherence, and body hermeticity.
c) bend leads 85-degrees maximum to provide a strong fixed position condition.
d) use roller-type die when forming gold-plated leads to minimize surface scouring.
e) provide a minimum surface contact length of 2 times the lead width.
f) leads should be cleaned of any bending tool lubricants to enhance solderability.

Cleaning After Mounting

A wide variety of chemicals and solvents is available for fluxing, degreasing, and flux removal. Care must be exercised in the selection of materials, such that from a reliability standpoint, there is no adverse effect on component life. A major contributor affecting device reliaiblity, is the chemical reaction of chloride with the aluminum metallization of the die. Eventually this etching process will result in electrical open circuits. The mechanism is defined as Electrolytic Metal Attack (EMA) and is accelerated in a mositure environment. Cleaning and fluxing compounds free of chloride will therefore maximize device life. Chloride is defined as the dissociated ion, which is soluble in water, as contrasted to the water insoluble organic chlorine of compounds such as perchloroethylene and trichloroethane. It is, of course, impractical to evaluate the long-term effect on semiconductor life of all chemicals which are marketed under a variety of brand names.

The choice of fluxes for electronic applications should be restricted to rosin types, R, RMA and RA and water soluble organic acid, OA, formulations. Inorganic acid fluxes should not be used as they can attack the internal metallization of the semiconductor. As stated above, it is further recommended, where applicable, that non-halide type fluxes be used for improved device reliability. Some examples of acceptable fluxes are:

A. Rosin Types (RA)
   Alpha 711
   Alpha 809 foam flux
   Alpha 811 foam flux
   Alpha 815 foam flux
   Alpha TL33M halide free
B. Water soluble organic acid (OA) types, halide free
   Blackstone 1452
   Kenco 183
   Alpha 260HF and 265HF

Since circuit boards can fall into several categories, such as single sided, double sided with plated-through holes and densely populated multilayer types, it must be stressed that the manufacturer's recommendation be considered when choosing the proper flux for the process being used.

Flux cleaning and/or degreasing is necessary to assure that the final soldered assembly is free of contaminating soils. The choice of the cleaning system is relative to the soil being removed. Water-based cleaners are generally used to remove polar soils, such as rosin activators, organic acid residues, and finger salts. Solvent cleaners are chosen for removal of organic (non-polar) contaminants, which include rosins, oils, and greases. Cleaning methods can incorporate immersion (with or without ultrasonics), brushing, and spraying. The choice of cleaner should be based on affinity for the contaminant, ability to thoroughly wet the parts, and compatibility with components. It should also be safe to use.

Solvent cleaners are generally divided into two classes: chlorinated and fluorinated. These can be used for cleaning rosin-activated (RA) fluxes. The chlorinated solvents are more aggressive and care must be taken to assure there is no damage to components or substrate. This type solvent should not be used with silicone-encapsulated transistors as the solvent will tend to dissolve the plastic. The use of chlorinated solvents must be closely monitored because a breakdown to form acid components in the presence of moisture. The solvent should be checked regularly and discarded when acid levels exceed manufacturer's guidelines. Fluorinated solvents are normally blends of trifluorotrichloroethane with other solvents, such as: methanol, ethanol, isopropanol, acetone, methylene chloride, or chloroform. These solvents can be purchased under trade names as Freon TE, TE35, TP35, Frigen 113 TR-M, Haltron 113 MOM, and Flugene 113 MA. Fluorinated systems are milder acting and are used in vapor degreasing systems at the boiling point of the solvent mixture.

The solvents may be used for a maximum of 4 hours at 25° C or for a maximum of 1 hour at 50° C.

Rosin fluxes can be removed by either solvent or aqueous cleaners. The water systems contain an additive that reacts with the rosin acids to convert the acids to a water-soluble biodegradable soap. Water-soluble organic-acid fluxes may require the use of a neutralizer to accelerate the solubility of the acid residues and neutralize any residues that may remain. Alcohols are acceptable solvents for rosin-based flux removal; but because of flammability concerns, the fluorinated alcohol blends are preferred. Examples of suitable alcohols are methanol, isopropanol, and special denatured ethyl alcohols, such as SDA1, SDA30, SDA34, and SDA44.

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and physical standpoint.

Handling

All CMOS gate inputs have a diode or resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n

Operating and Handling Considerations

junction diodes. These diode networks at input and output interface protect CMOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. It is recommended that ionizers be used in the handling and assembly areas to minimize damage from electrostatic discharge (ESD). See ICAN-6525, "Handling and Operating Considerations for MOS Integrated Circuits", for proper handling procedures.

Operating

Unused Inputs

All unused input leads must be connected to either the low rail (V_{SS}, V_{EE}, or GND) or the high rail (V_{CC} or V_{DD}), whichever is appropriate for the logic circuit involved. A floating input not only can result in faulty logic operation, but can cause the maximum-rated power dissipation to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a resistor to the high or low voltage supply rails A useful range of values for such resistors is from 10 kilohms to 1 megohm. Pins that are I/O must have a terminating resistor.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady-state value of less than the absolute-maximum rating. Input currents of less than the maximum rating prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

Output Short Circuits

Shorting of outputs to the high or low supply rail can damage many of the higher-output-current CMOS types, such as the CD4007, CD4041, CD4049, and CD4050. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For the CMOS HC/HCT/HCU types, outputs may be shorted to V_{CC} (5 V ± 10%) for 1 second maximum and only one output at a time. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below the device maximum-rated output power.

For detailed CMOS IC operating and handling considerations, refer to Application Note ICAN-6525 "Handling and Operating Considerations for MOS Integrated Circuits."

CMOS Power-Supply Distribution and Decoupling

Power distribution should be a prime consideration in all CMOS designs. Although DC power dissipation is very low, dynamic power (due to switching transients) can be high. High-voltage and/or low-temperature operation increase dynamic current transients.

A low-impedance power source and supply-to-ground capacitance bypass will significantly reduce noise generation on signal and power line to greatly enhance system reliability.

Decoupling

Higher speeds, faster edges and higher output-drive currents cause higher-frequency current transients to be imposed on ground and V_{CC} rails of an IC. For LSI and high-speed families, consideration of power-supply distribution and decoupling become important. Before decoupling can be utilized for noise reduction, there must first be a good power-supply distribution network. A good ground connection system and capacitive decoupling must be employed. For details refer to Application Note ICAN-7329, "Power-Supply Distribution and Decoupling for CMOS High-Speed-Logic ICs."

SOLID-STATE CHIPS

When supplied in individual die form, solid-state chips, unlike packaged devices, are normally fragile and small in physical size, and therefore, require special-handling as follows:

1. Chips must be stored under proper conditions to ensure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40° C
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. The procedures used to reduce the possibility of electrostatic discharge in packaged devices also apply for solid-state chips.
4. During mounting and lead bonding of chips, the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
5. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to ensure that these non-hermetic chips are not subjected to moist or contaminated atmospheres which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

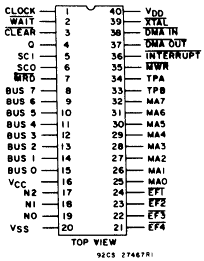
1800-Series Microprocessors and Microcomputers

Technical Data

Comparison of RCA CMOS CDP1800-Series Microprocessors and Microcomputers

Features	CDP1802A CDP1802AC	CDP1802BC	CDP1804AC	CDP1805AC	CDP1806AC
Memory Addressing (Bytes)	64k	64k	64k	64k	64k
On-Chip RAM (Bytes)	—	—	64k	64k	—
On-chip ROM (Bytes)	—	—	2k	—	—
Max. Clock Frequency (MHz)	3.2	5	5	5	5
Instruction Time Min./Max. (μs)	5/7.5	3.2/4.8	3.2/16	3.2/16	3.2/16
Timer/Counter Bits	—	—	8	8	8
Prescalers	—	—	÷ 32	÷ 32	÷ 32
Bus Structure		Non-multiplexed Address Lines			
Interrupts	√	√	√	√	√
Latched I/O Lines		Off-Chip			
Max. Operating Temp. Temp. Range (°C)		-55 to +125°C			
Package No. of Pins	40 D, E 44 Q	40 D, E 44 Q	40 D, E —	40 D, E 44 Q	40 D, E 44 Q
Serial Interface		Q-Line			

CDP1802A, CDP1802AC



TERMINAL ASSIGNMENT

CMOS 8-Bit Microprocessor

Features:

- *Minimum instruction fetch-execute time of 5 µs or 7.5 µs at V_{DD} = 5 V; 2.5 µs or 3.75 µs at V_{DD} = 10 V*
- *Any combination of standard RAM and ROM up to 65,536 bytes*
- *Operates with slow memories, up to 1 µs access time at f_{CL} = 4 MHz*
- *8-bit parallel organization with bidirectional data bus and multiplexed address bus*
- *16 x 16 matrix of registers for use as multiple program counters, data pointers, or data registers*
- *On-chip DMA, interrupt, and flag inputs*
- *Programmable single-bit output port*
- *91 easy-to-use instructions*

The RCA-CDP1802A LSI CMOS 8-bit register-oriented central-processing unit (CPU) is designed for use as a general-purpose computing or control element in a wide range of stored-program systems or products.

The CDP1802A includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

The 1800 series architecture is designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The 1800 series CPU also provides a synchronous interface to memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Further, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct memory-access modes.

The CDP1802A and CDP1802AC are functionally identical. They differ in that the CDP1802A has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1802AC a recommended operating voltage range of 4 to 6.5 volts.

These types are supplied in 40-lead dual-in-line side-brazed ceramic packages (D suffix), 40-lead dual-in-line plastic packages (E suffix) and 44-lead plastic chip-carrier (PCC) package (Q suffix). The CDP1802AC is also available in chip form (H suffix).

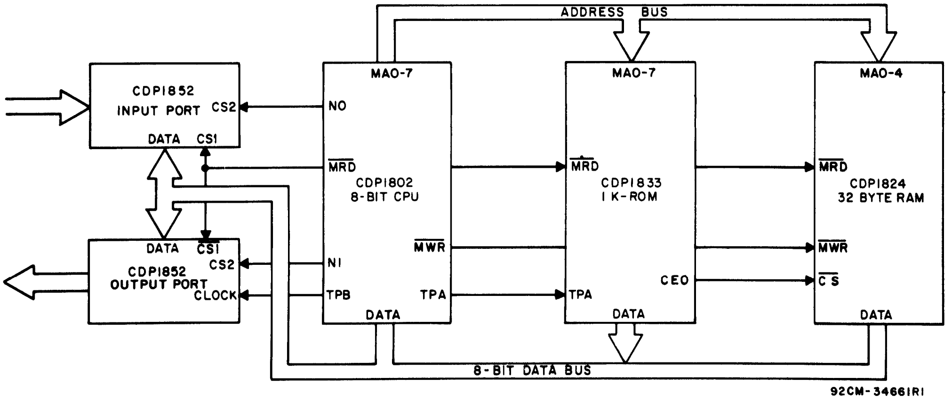


Fig. 1 - Typical CDP1802A small microprocessor system.

File Number **1305**

CDP1802A, CDP1802AC

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}).
(All voltages referenced to V_{SS} terminal)
CDP1802A .... −0.5 to +11 V
CDP1802AC .... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A=−40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A=−55 to +100°C (PACKAGE TYPE D) .... 500 mW
For T_A=+100 to +125°C (PACKAGE TYPE D) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -40°C to +85°C (PACKAGE TYPE Q) * .... 500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)·
PACKAGE TYPE D .... −55 to +125°C
PACKAGE TYPE E and Q .... −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16±1/32 in (1.59±0 79 mm) from case for 10 s max .... +265°C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

OPERATING CONDITIONS at T_A=-40°C to +85°C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS		LIMITS				UNITS
	V_{CC}[1] (V)	V_{DD} (V)	CDP1802A		CDP1802AC		
			Min.	Max.	Min.	Max.	
DC Operating Voltage Range	—	—	4	10.5	4	6.5	V
Input Voltage Range	—	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	
Maximum Clock Input Rise or Fall Time, t_r,t_f	4 to 10.5	4 to 10.5	—	1	—	1	µs
Minimum Instruction Time[2]	5	5	5	—	5	—	
	5	10	4	—	—	—	
	10	10	2.5	—	—	—	
Maximum DMA Transfer Rate	5	5	—	400	—	400	KBytes per second
	5	10	—	500	—	—	
	10	10	—	800	—	—	
Maximum Clock Input Frequency, f_{CL}, Load Capacitance (C_L)=50 pF	5	5	DC	3.2	DC	3.2	MHz
	5	10	DC	4	—	—	
	10	10	DC	6.4	—	—	

[1] V_{CC} must never exceed V_{DD}.

[2] Equals 2 machine cycles—one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles—one Fetch and two Execute operations

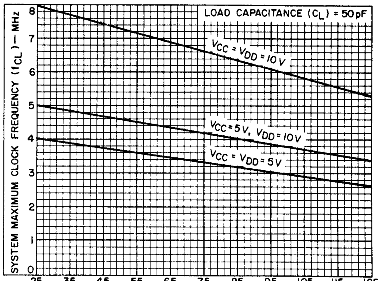


Fig. 2 - *Typical maximum clock frequency as a function of temperature.*

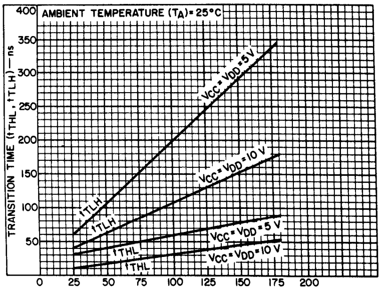
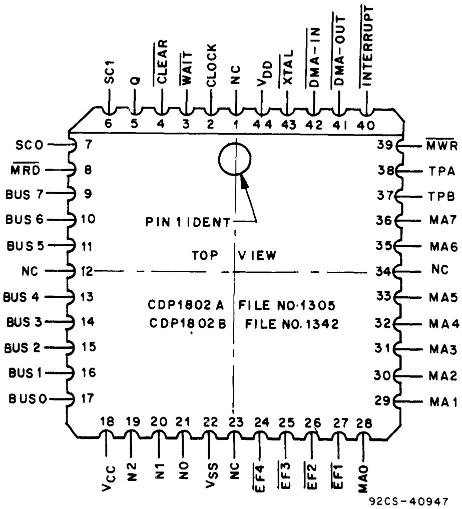


Fig. 3 - *Typical transition time vs. load capacitance.*

CDP1802A, CDP1802AC

TERMINAL ASSIGNMENT



Plastic Chip-Carrier (PCC) Package

2

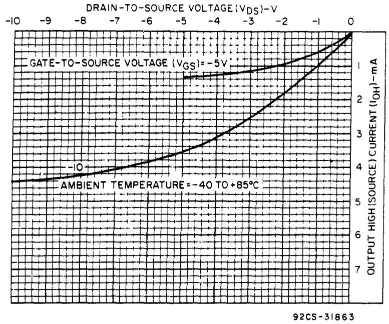


Fig. 4 - Minimum output high (source) current characteristics.

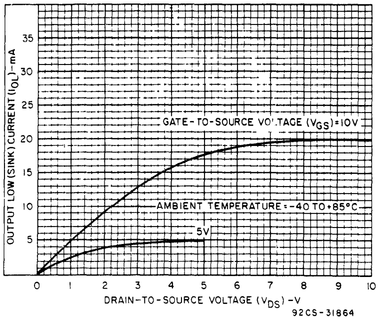


Fig. 5 - Minimum output low (sink) current characteristics.

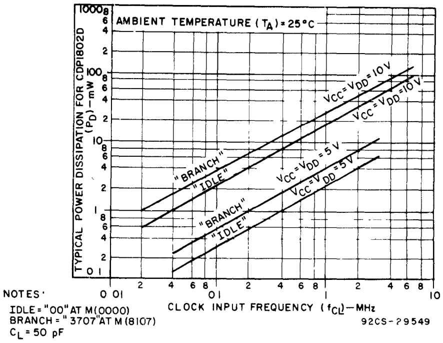


Fig. 6 - Typical power dissipation as a function of clock frequency for BRANCH instruction and IDLE instruction

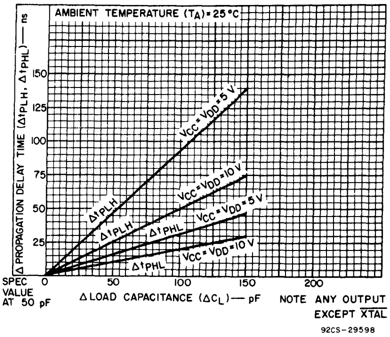


Fig 7 - Typical change in propagation delay as a function of a change in load capacitance.

CDP1802A, CDP1802AC

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, except as noted.

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_{OUT} (V)	V_{IN} (V)	V_{CC}, V_{DD} (V)	CDP1802A			CDP1802AC			
				Min.	Typ.•	Max.	Min.	Typ.•	Max.	
Quiescent Device Current I_{DD}	—	—	5	—	0.1	50	—	1	200	µA
	—	—	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current (Except $\overline{XTAL}$) I_{OL}	0.4	0,5	5	1.1	2.2	—	1.1	2.2	—	mA
	0.5	0,10	10	2.2	4.4	—	—	—	—	
$\overline{XTAL}$ I_{OL}	0.4	5	5	170	350	—	170	350	—	µA
Output High Drive (Source) Current (Except $\overline{XTAL}$) I_{OH}	4.6	0,5	5	−0.27	−0.55	—	−0.27	−0.55	—	mA
	9.5	0,10	10	−0.55	−1.1	—	—	—	—	
XTAL I_{OH}	4.6	0	5	−125	−250	—	−125	−250	—	µA
Output Voltage Low-Level V_{OL}	—	0,5	5	—	0	0.1	—	0	0.1	V
	—	0,10	10	—	0	0.1	—	—	—	
Output Voltage High Level V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
	0.5, 4.5	—	5,10	—	—	1	—	—	—	
	1,9	—	10	—	—	3	—	—	—	
Input High Voltage V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,4.5	—	5,10	4	—	—	—	—	—	
	1,9	—	10	7	—	—	—	—	—	
$\overline{CLEAR}$ Input Voltage Schmitt Hysteresis V_H	—	—	5	0.4	0.5	—	0.4	0.5	—	
	—	—	5,10	0.3	0.4	—	—	—	—	
	—	—	10	1.5	2	—	—	—	—	
Input Leakage Current I_{IN}	Any Input	0,5	5	—	$\pm 10^{-4}$	±1	—	$\pm 10^{-4}$	±1	µA
		0,10	10	—	$\pm 10^{-4}$	±1	—	—	—	
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	—	$\pm 10^{-4}$	±1	—	$\pm 10^{-4}$	±1	
	0,10	0,10	10	—	$\pm 10^{-4}$	±1	—	—	—	
Operating Current, I_{DD1}^{Δ} f=3.2 MHz	—	—	5	—	2	4	—	2	4	mA
Minimum Data Retention Voltage V_{DR}	$V_{DD}=V_{DR}$			—	2	2.4	—	2	2.4	V
Data Retention Current I_{DR}	V_{DD}=2.4 V			—	0.05	—	—	0.5	—	µA
Input Capacitance C_{IN}				—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}				—	10	15	—	10	15	

•Typical values are for T_A=25°C and nominal V_{DD}

$^{\Delta}$Idle "00" at M(0000), C_L=50 pF.

CDP1802A, CDP1802AC

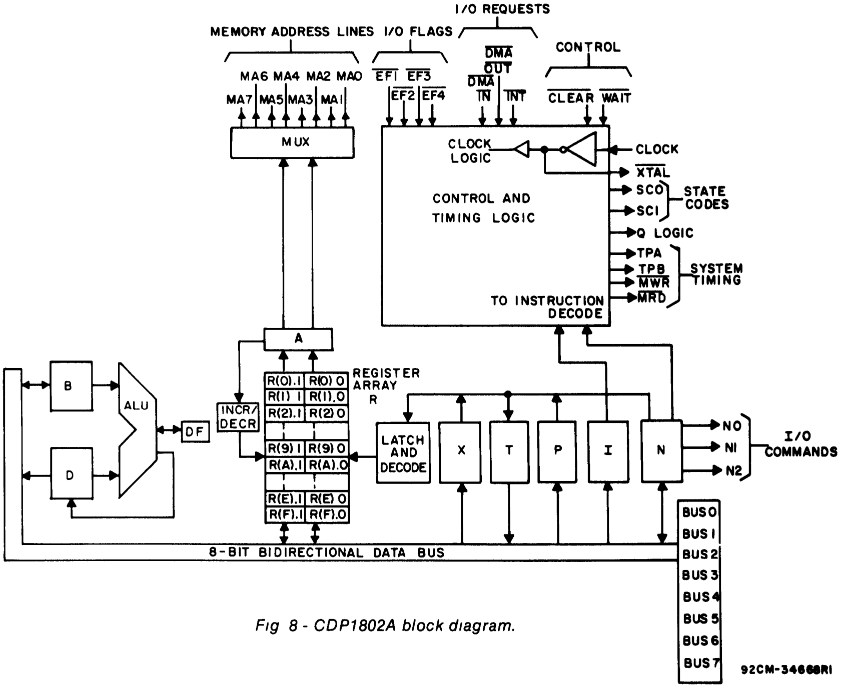


Fig 8 - CDP1802A block diagram.

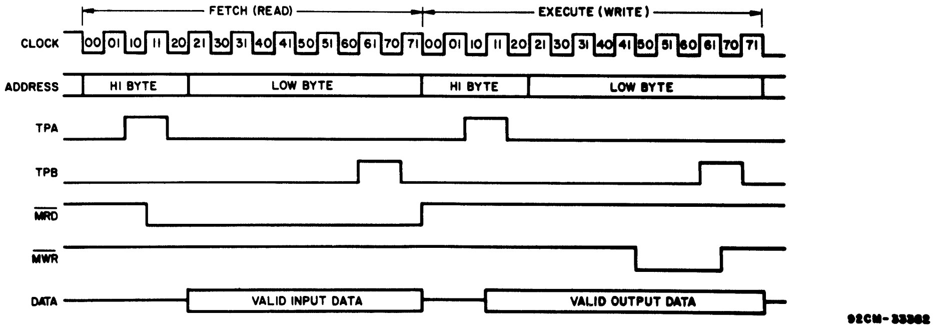


Fig. 9 - Basic dc timing waveforms, one instruction cycle.

CDP1802A, CDP1802AC

SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus):

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O) Lines):

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal.

$\overline{\text{MRD}}=V_{CC}$: Data from I/O to CPU and Memory
$\overline{\text{MRD}}=V_{SS}$: Data from Memory to I/O

$\overline{\text{EF1}}$ to $\overline{\text{EF4}}$ (4 Flags):

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

$\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, $\overline{\text{DMA-OUT}}$ (3 I/O Requests)

These inputs are sampled by the CDP1802A during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and Interrupt requests, DMA-IN has priority followed by DMA-OUT and then Interrupt.

SC0, SC1, (2 State Code Lines):

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA. $H=V_{CC}$, $L=V_{SS}$.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB (2 Timing Pulses):

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

MA0 to MA7 (8 Memory Address Lines):

In each cycle, the higher-order byte of a 16-bit CPU memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64K bytes.

$\overline{\text{MWR}}$ (Write Pulse):

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{\text{MRD}}$ (Read Level):

A low level on $\overline{\text{MRD}}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, $\overline{\text{MRD}}$ is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction. For additional information see Table I.

Q:

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK:

Input for externally generated single-phase clock. A typical clock frequency is 6.4 MHz at $V_{CC}= V_{DD}=10$ volts. The clock is counted down internally to 8 clock pulses per machine cycle.

$\overline{\text{XTAL}}$:

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{\text{XTAL}}$) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be required at terminals 1 and 39. For additional information, see ICAN-6565.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$ (2 Control Lines):

Provide four control modes as listed in the following truth table:

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

V_{DD}, V_{SS}, V_{CC} (Power Levels):

The internal voltage supply V_{DD} is isolated from the Input/Output voltage supply V_{CC} so that the processor may operate at maximum speed while interfacing with peripheral devices operating at lower voltage. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}. The recommended input voltage swing is V_{SS} to V_{CC}.

ARCHITECTURE

The CPU block diagram is shown in Fig. 8. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. the D register (either of the two bytes can be gated to D);
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

With two exceptions, CPU instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and third if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. indicate to the I/O devices a command code or device-selection code for peripherals;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions (70-73 and 78-7B);
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations F1-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions — 70-73, 78, 60, F0.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the 1800-series architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, four instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

The Q Flip Flop

An internal flip flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a microprocessor output.

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request occurs and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Interrupt Enable is automatically de-activated to inhibit further interruptions. The user's interrupt routine is now in control; the contents of T may be saved by means of a single instruction (78) in the memory location pointed to by R(X). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with a single instruction (70 or 71). The Interrupt-Enable flip flop can be activated to permit further interrupts or can be disabled to prevent them.

CDP1802A, CDP1802AC

CPU Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer

N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nibble)
IE	1 Bit	Interrupt Enable
Q	1 Bit	Output Flip Flop

CDP1802 Control Modes

The $\overline{\text{WAIT}}$ and $\overline{\text{CLEAR}}$ lines provide four control modes as listed in the following truth table:

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

The function of the modes are defined as follows:

Load

Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

Reset

Registers I, N, Q are reset, IE is set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Powerup reset can be realized by connecting an RC network directly to the $\overline{\text{CLEAR}}$ pin, since it has a Schmitt-triggered input, see Fig. 10.

Pause

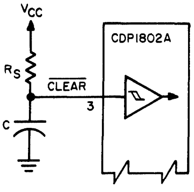
Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

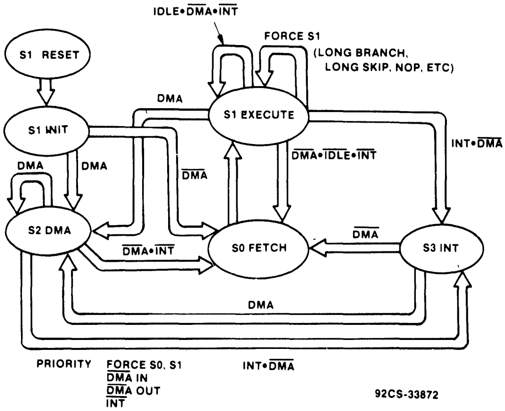
RUN-MODE STATE TRANSITIONS

The CDP1802A CPU state transitions when in the RUN and RESET modes are shown in Fig. 11. Each machine cycle requires the same period of time, 8 clock pulses, except the initialization cycle, which requires 9 clock pulses. The execution of an instruction requires either two or three machine cycles, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response. Table II shows the conditions on Data Bus and Memory-Address lines during all machine states.



The RC time constant should be greater than the oscillator start-up time (typically 20 ms).

Fig. 10 - Reset diagram.



IDLE•$\overline{\text{DMA}}$•$\overline{\text{INT}}$
FORCE S1
(LONG BRANCH, LONG SKIP, NOP, ETC)
S1 RESET
S1 INIT
S1 EXECUTE
DMA
INT•$\overline{\text{DMA}}$
$\overline{\text{DMA}}$•$\overline{\text{IDLE}}$•$\overline{\text{INT}}$
DMA
DMA
$\overline{\text{DMA}}$
S2 DMA
$\overline{\text{DMA}}$•$\overline{\text{INT}}$
S0 FETCH
$\overline{\text{DMA}}$
S3 INT
DMA
PRIORITY
FORCE S0, S1
$\overline{\text{DMA}}$ IN
$\overline{\text{DMA}}$ OUT
$\overline{\text{INT}}$
INT•$\overline{\text{DMA}}$
92CS-33872

Fig. 11 - State transition diagram.

INSTRUCTION SET

The CPU instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where
W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)

Operation Notation
M(R(N)) → D; R(N) + 1 → R(N)

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I — INSTRUCTION SUMMARY (See Notes following table, pp. 11 and 12)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N))→D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N))→D; (RN)+1 →R(N)
LOAD VIA X	LDX	F0	M(R(X))→D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X))→D; R(X)+1→R(X)
LOAD IMMEDIATE	LDI	F8	M(R(P))→D; R(P)+1→R(P)
STORE VIA N	STR	5N	D→M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D→M(R(X)); R(X)−1→R(X)
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N)+1→R(N)
DECREMENT REG N	DEC	2N	R(N)−1→R(N)
INCREMENT REG X	IRX	60	R(X)+1→R(X)
GET LOW REG N	GLO	8N	R(N).0→D
PUT LOW REG N	PLO	AN	D→R(N).0
GET HIGH REG N	GHI	9N	R(N).1→D
PUT HIGH REG N	PHI	BN	D→R(N).1
LOGIC OPERATIONS§			
OR	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D→D; R(P)+1→R(P)
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D→D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D→D; R(P)+1→R(P)
AND	AND	F2	M(R(X)) AND D→D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D→D; R(P)+1→R(P)
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)→DF, 0→MSB(D)
SHIFT RIGHT WITH CARRY RING SHIFT RIGHT	SHRC RSHR	76§	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)
SHIFT LEFT WITH CARRY RING SHIFT LEFT	SHLC RSHL	7E§	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS §			
ADD	ADD	F4	M(R(X))+D→DF, D
ADD IMMEDIATE	ADI	FC	M(R(P))+D→DF,D; R(P)+1→R(P)
ADD WITH CARRY	ADC	74	M(R(X))+D+DF→DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P))+D+DF→DF, D R(P)+1→R(P)
SUBTRACT D	SD	F5	M(R(X))−D→DF, D

SUBTRACT D IMMEDIATE	SDI	FD	M(R(P))−D→DF, D;
			R(P)+1→R(P)

SUBTRACT D WITH BORROW	SDB	75	M(R(X))−D−(NOT DF)→DF, D

SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P))−D−(NOT DF)→DF, D;
			R(P)+1→R(P)

SUBTRACT MEMORY	SM	F7	D−M(R(X))→DF, D

SUBTRACT MEMORY IMMEDIATE	SMI	FF	D−M(R(P))→DF, D;
			R(P)+1→R(P)

SUBTRACT MEMORY WITH BORROW	SMB	77	D−M(R(X))−(NOT DF)→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D−M(R(P))−(NOT DF)→DF, D R(P)+1→R(P)
BRANCH INSTRUCTIONS—SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38§	R(P)+1→R(P)

SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF DF=1	BDF	33§	IF DF=1, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		

SHORT BRANCH IF DF=0	BNF	3B§	IF DF=0, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		

SHORT BRANCH IF Q=1	BQ	31	IF Q=1, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF EF1=1
($\overline{EF1}=V_{SS}$)
	B1	34	IF EF1=1, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF EF1=0
($\overline{EF1}=V_{CC}$)
	BN1	3C	IF EF1=0, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF EF2=1
($\overline{EF2}=V_{SS}$)
	B2	35	IF EF2=1, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF EF2=0
($\overline{EF2}=V_{CC}$)
	BN2	3D	IF EF2=0, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF EF3=1
($\overline{EF3}=V_{SS}$)
	B3	36	IF EF3=1, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF EF3=0
($\overline{EF3}=V_{CC}$)
	BN3	3E	IF EF3=0, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS—SHORT BRANCH			

SHORT BRANCH IF EF4=1
($\overline{EF4}=V_{SS}$)
	B4	37	IF EF4=1, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF EF4=0
($\overline{EF4}=V_{CC}$)
	BN4	3F	IF EF4=0, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

BRANCH INSTRUCTIONS—LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P)+1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8§	R(P)+2→R(P)

LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1
			M(R(P)+1)→R(P).0
			ELSE R(P)+2→R(P)

LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1
			M(R(P)+1)→R(P).0
			ELSE R(P)+2→R(P)

LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1
			M(R(P)+1)→R(P).0
			ELSE R(P)+2→R(P)

LONG BRANCH IF DF=0	LBNF	CB	IF DF=0, M(R(P))→R(P).1
			M(R(P)+1)→R(P).0
			ELSE R(P)+2→R(P)

LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1
			M(R(P)+1)→R(P).0
			ELSE R(P)+2→R(P)

LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1
			M(R(P)+1)→R(P).0
			ELSE R(P)+2→R(P)

SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38§	R(P)+1→R(P)
LONG SKIP (SEE NLBR)	LSKP	C8§	R(P)+2→R(P)

LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P)+2→R(P)
			ELSE CONTINUE

LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P)+2→R(P)
			ELSE CONTINUE

LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P)+2→R(P)
			ELSE CONTINUE

LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P)+2→R(P)
			ELSE CONTINUE

LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P)+2→R(P)
			ELSE CONTINUE

LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P)+2→R(P)
			ELSE CONTINUE

LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P)+2→R(P)
			ELSE CONTINUE

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)−1→R(2)
RETURN	RET	70	M(R(X))→(X,P); R(X)+1→R(X) 1→IE
DISABLE	DIS	71	M(R(X))→(X,P); R(X)+1→R(X) 0→IE
INPUT-OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS;R(X)+1→R(X); N LINES=1
OUTPUT 2	OUT 2	62	M(R(X))→BUS;R(X)+1→R(X); N LINES=2
OUTPUT 3	OUT 3	63	M(R(X))→BUS;R(X)+1→R(X); N LINES=3
OUTPUT 4	OUT 4	64	M(R(X))→BUS;R(X)+1→R(X); N LINES=4
OUTPUT 5	OUT 5	65	M(R(X))→BUS;R(X)+1→R(X); N LINES=5
OUTPUT 6	OUT 6	66	M(R(X))→BUS;R(X)+1→R(X); N LINES=6
OUTPUT 7	OUT 7	67	M(R(X))→BUS;R(X)+1→R(X); N LINES=7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES=1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES=2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES=3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES=4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES=5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES=6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES=7

Notes

∮THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF AFTER AN ADD INSTRUCTION:
DF=1 DENOTES A CARRY HAS OCCURRED
DF=0 DENOTES A CARRY HAS NOT OCCURRED
AFTER A SUBTRACT INSTRUCTION
DF=1 DENOTES NO BORROW D IS A TRUE POSITIVE NUMBER
DF=0 DENOTES A BORROW D IS TWO'S COMPLEMENT
THE SYNTAX "−(NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

§THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC EACH MNEMONIC IS INDIVIDUALLY LISTED

#AN IDLE INSTRUCTION INITIATES A REPEATING S1 CYCLE THE PROCESSOR WILL CONTINUE TO IDLE UNTIL AN I/O REQUEST ($\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, OR $\overline{\text{DMA-OUT}}$) IS ACTIVATED WHEN THE REQUEST IS ACKNOWLEDGED, THE IDLE CYCLE IS TERMINATED AND THE I/O REQUEST IS SERVICED, AND THEN NORMAL OPERATION IS RESUMED

Notes for TABLE I

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch +2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high- and low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

   The short-branch instruction can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test the status (1 or 0) of the four EF flags
   f) Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program

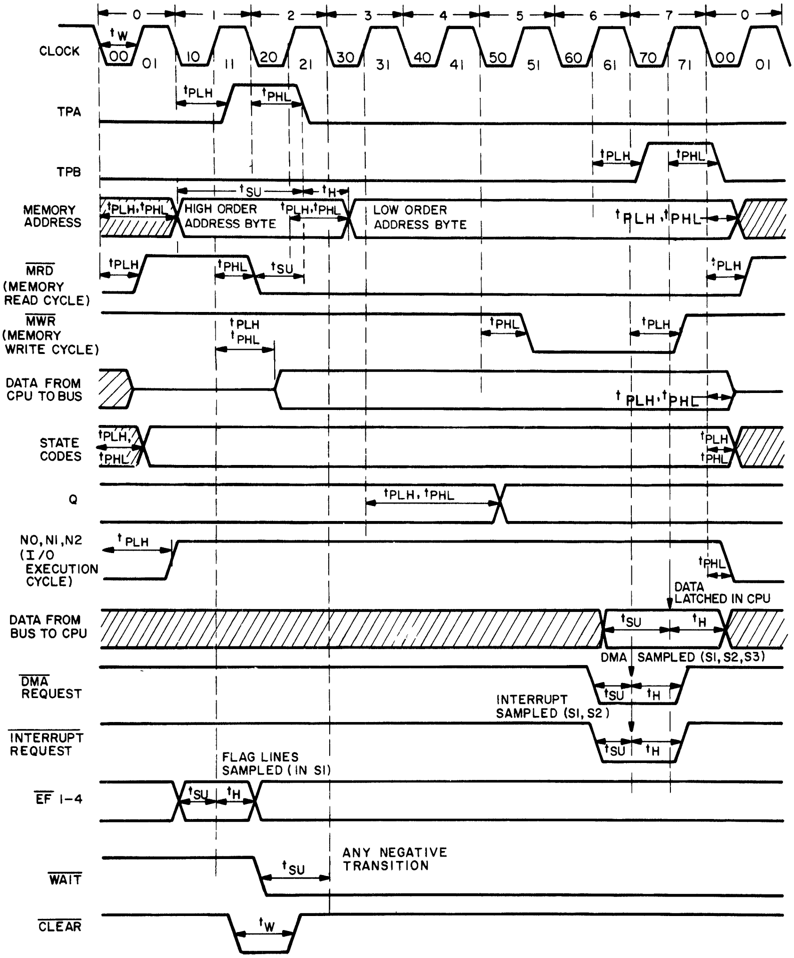
   The Long-Skip instructions take three cycles to complete (1 fetch +2 execute).

   They can:
   a) Skip unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test for IE=1

   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken.

   Execution is continued by fetching the next instruction in sequence.

CDP1802A, CDP1802AC



NOTES

1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE
2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS
3. SHADED AREAS INDICATE "DON'T CARE" OR UNDEFINED STATE; MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD

92CL-33869R2

Fig. 12 - Timing waveforms

CDP1802A, CDP1802AC

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85°C, C_L=50 pF, V_{DD}±5%, except as noted.

CHARACTERISTIC		V_{CC} (V)	V_{DD} (V)	LIMITS		UNITS
				Typ.●	Max.	
Propagation Delay Times:						
Clock to TPA, TPB	t_{PLH}, t_{PHL}	5	5	200	300	ns
		5	10	150	250	
		10	10	100	150	
Clock-to-Memory High-Address Byte	t_{PLH}, t_{PHL}	5	5	600	850	
		5	10	400	600	
		10	10	300	400	
Clock-to-Memory Low-Address Byte Valid	t_{PLH}, t_{PHL}	5	5	250	350	
		5	10	150	250	
		10	10	100	150	
Clock to $\overline{MRD}$	t_{PHL}	5	5	200	300	
		5	10	150	250	
		10	10	100	150	
Clock to $\overline{MRD}$	t_{PLH}	5	5	200	350	
		5	10	150	290	
		10	10	100	175	
Clock to $\overline{MWR}$	t_{PLH}, t_{PHL}	5	5	200	300	
		5	10	150	250	
		10	10	100	150	
Clock to (CPU DATA to BUS) Valid	t_{PLH}, t_{PHL}	5	5	300	450	
		5	10	250	350	
		10	10	100	200	
Clock to State Code	t_{PLH}, t_{PHL}	5	5	300	450	
		5	10	250	350	
		10	10	150	250	
Clock to Q	t_{PLH}, t_{PHL}	5	5	250	400	
		5	10	150	250	
		10	10	100	150	
Clock to N (0-2)	t_{PLH}, t_{PHL}	5	5	300	550	
		5	10	200	350	
		10	10	150	250	
Minimum Setup and Hold Times:						
Data Bus Input Setup	t_{SU}	5	5	−20	25	
		5	10	0	50	
		10	10	−10	40	
Data Bus Input Hold	t_H■	5	5	150	200	
		5	10	100	125	
		10	10	75	100	
$\overline{DMA}$ Setup	t_{SU}	5	5	0	30	
		5	10	0	20	
		10	10	0	10	
$\overline{DMA}$ Hold	t_H■	5	5	150	250	
		5	10	100	200	
		10	10	75	125	
Interrupt Setup	t_{SU}	5	5	−75	0	
		5	10	−50	0	
		10	10	−25	0	

●Typical values are for T_A=25°C and nominal V_{DD}

■Maximum limits of minimum characteristics are the values above which all devices function

CDP1802A, CDP1802AC

DYNAMIC ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC		V_{CC} (V)	V_{DD} (V)	LIMITS		UNITS
				Typ.•	Max.	
Minimum Setup and Hold Times:						
Interrupt Hold	t_H■	5	5	100	150	ns
		5	10	75	100	
		10	10	50	75	
$\overline{\text{WAIT}}$ Setup	t_{SU}	5	5	10	50	
		5	10	−10	15	
		10	10	0	25	
$\overline{\text{EF1-4}}$ Setup	t_{SU}	5	5	−30	20	
		5	10	−20	30	
		10	10	−10	40	
$\overline{\text{EF1-4}}$ Hold	t_H■	5	5	150	200	
		5	10	100	150	
		10	10	75	100	
Minimum Pulse Width Times:						
$\overline{\text{CLEAR}}$ Pulse Width	t_{WL}■	5	5	150	300	
		5	10	100	200	
		10	10	75	150	
$\overline{\text{CLOCK}}$ Pulse Width	t_{WL}	5	5	125	150	
		5	10	100	125	
		10	10	60	75	

•Typical values are for T_A=25°C and nominal V_{DD}.

■Maximum limits of minimum characteristics are the values above which all devices function.

TIMING SPECIFICATIONS as a function of T(T=1/f_{CLOCK}) at T_A=-40 to +85°C

CHARACTERISTIC		V_{CC} (V)	V_{DD} (V)	LIMITS		UNITS
				Min.	Typ.•	
High-Order Memory-Address Byte Set Up to TPA ↘ Time	t_{SU}	5	5	2T-550	2T-400	ns
		5	10	2T-350	2T-250	
		10	10	2T-250	2T-200	
High-Order Memory-Address Byte Hold after TPA Time	t_H	5	5	T/2-25	T/2-15	
		5	10	T/2-35	T/2-25	
		10	10	T/2-10	T/2+0	
Low-Order Memory-Address Byte Hold after WR Time	t_H	5	5	T-30	T+0	
		5	10	T-20	T+0	
		10	10	T-10	T+0	
CPU Data to Bus Hold after WR Time	t_H	5	5	T-200	T-150	
		5	10	T-150	T-100	
		10	10	T-100	T-50	
Required Memory Access Time Address to Data	t_{ACC}	5	5	5T-375	5T-250	
		5	10	5T-250	5T-150	
		10	10	5T-190	5T-100	
$\overline{\text{MRD}}$ to TPA (↘)	t_{SU}	5	5	T/2-25	T/2-18	
		5	10	T/2-20	T/2-15	
		10	10	T/2-15	T/2-10	

•Typical values are for T_A=25°C and nominal V_{DD}

CDP1802A, CDP1802AC

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES[G]
S1	RESET			0→I,N,Q,X,P; 1→IE	00	XXXX	1	1	0	A
S1	INITIALIZE NOT PROGRAMMER ACCESSIBLE			0000→R	00	XXXX	1	1	0	B
S0	FETCH			MRP→I, N; RP+1→RP	MRP	RP	0	1	0	C
S1	0	0	IDL	IDLE	MR0	R0	0	1	0	D,3
	0	1-F	LDN	MRN→D	MRN	RN	0	1	0	3
	1	0-F	INC	RN+1→RN	FLOAT	RN	1	1	0	1
	2	0-F	DEC	RN−1→RN	FLOAT	RN	1	1	0	1

	3	0-F	SHORT BRANCH	TAKEN;
				MRP→RP.0
				NOT TAKEN;
				RP+1→RP
					MRP	RP	0	1	0	3

	4	0-F	LDA	MRN→D; RN+1→RN	MRN	RN	0	1	0	3
	5	0-F	STR	D→MRN	D	RN	1	0	0	2
	6	0	IRX	RX+1→RX	MRX	RX	0	1	0	2
	6	1	OUT 1	MRX→BUS; RX+1→RX	MRX	RX	0	1	1	6
		2	OUT 2						2	
		3	OUT 3						3	
		4	OUT 4						4	
		5	OUT 5						5	
		6	OUT 6						6	
		7	OUT 7						7	
		9	INP 1	BUS→MRX,D	DATA FROM I/O DEVICE	RX	1	0	1	5
		A	INP 2						2	
		B	INP 3						3	
		C	INP 4						4	
		D	INP 5						5	
		E	INP 6						6	
		F	INP 7						7	
	7	0	RET	MRX→(X,P), RX+1→RX; 1→IE	MRX	RX	0	1	0	3
		1	DIS	MRX→(X,P), RX+1→RX, 0→IE	MRX	RX	0	1	0	3
		2	LDXA	MRX→D; RX+1→RX	MRX	RX	0	1	0	3
		3	STXD	D→MRX; RX−1→RX	D	RX	1	0	0	2
		4	ADC	MRX+D+ DF→DF,D	MRX	RX	0	1	0	3

CDP1802A, CDP1802AC

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (CONT'D)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	N LINES	NOTES^G
S1	7	5	SDB	MRX−D−DFN→DF,D	MRX	RX	0	1	0	3
		6	SHRC	LSB(D)→DF, DF→MSB(D)	FLOAT	RX	1	1	0	1
		7	SMB	D−MRX−DFN→DF,D	MRX	RX	0	1	0	3
		8	SAV	T→MRX	T	RX	1	0	0	2
		9	MARK	(X,P)→T, MR2, P→X, R2−1→R2	T	R2	1	0	0	2
		A	REQ	0→Q	FLOAT	RP	1	1	0	1
		B	SEQ	1→Q	FLOAT	RP	1	1	0	1
		C	ADCI	MRP+D+DF→DF,D, RP+1	MRP	RP	0	1	0	3
		D	SDBI	MRP−D−DFN→DF,D, RP+1	MRP	RP	0	1	0	3
		E	SHLC	MSB(D)→DF, DF→LSB(D)	FLOAT	RP	1	1	0	1
		F	SMBI	D−MRP−DFN→DF,D, RP+1	MRP	RP	0	1	0	3
	8	0-F	GLO	RN 0→D	RN.0	RN	1	1	0	1
	9	0-F	GHI	RN 1→D	RN 1	RN	1	1	0	1
	A	0-F	PLO	D→RN 0	D	RN	1	1	0	1
	B	0-F	PHI	D→RN 1	D	RN	1	1	0	1
S1#1	C	0-3, 8-B	LONG BRANCH	TAKEN MRP→B, RP+1→RP	MRP	RP	0	1	0	4
#2				TAKEN B→RP.1, MRP→RP 0	M(RP+1)	RP+1	0	1	0	4
S1#1				NOT TAKEN RP+1→RP	MRP	RP	0	1	0	4
#2				NOT TAKEN RP+1→RP	M(RP+1)	RP+1	0	1	0	4
S1#1		5 6 7 C D E F	LONG SKIP	TAKEN RP+1→RP	MRP	RP	0	1	0	4
#2				TAKEN RP+1→RP	M(RP+1)	RP+1	0	1	0	4
S1#1				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0	4
#2				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0	4
S1#1		4	NOP	NO OPERATION	MRP	RP	0	1	0	4
#2				NO OPERATION	MRP	RP	0	1	0	4

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (CONT'D)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES[G]
S1	D	0-F	SEP	N→P	NN	RN	1	1	0	1
	E	0-F	SEX	N→X	NN	RN	1	1	0	1
	F	0	LDX	MRX→D	MRX	RX	0	1	0	3
		1	OR	MRX OR D→D	MRX	RX	0	1	0	3
		2	AND	MRX AND D→D						
		3	XOR	MRX XOR D→D						
		4	ADD	MRX+D→DF,D						
		5	SD	MRX−D→DF,D						
		7	SM	D−MRX→DF,D						
		6	SHR	LSB(D)→DF; 0→MSB(D)	FLOAT	RX	1	1	0	1
		8	LDI	MRP→D, RP+1→RP	MRP	RP	0	1	0	3
		9	ORI	MRP OR D→D; RP+1→RP						
		A	ANI	MRP AND D→D; RP+1→RP						
		B	XRI	MRP XOR D→D, RP+1→RP						
		C	ADI	MRP+D→DF,D, RP+1→RP						
		D	SDI	MRP−D→DF,D; RP+1→RP						
		F	SMI	D−MRP→DF,D, RP+1→RP						
		E	SHL	MSB(D)→DF; 0→LSB(D)	FLOAT	RP	1	1	0	1
S2	DMA IN			BUS→MR0; R0+1→R0	DATA FROM I/O DEVICE	R0	1	0	0	F, 7
	DMA OUT			MR0→BUS, R0+1→R0	MR0	R0	0	1	0	F, 8
S3	INTERRUPT			X,P→T, 0→IE 1→P, 2→X	FLOAT	RN	1	1	0	9
S1	LOAD			IDLE ($\overline{\text{CLEAR}}$, $\overline{\text{WAIT}}$=0)	M(R0−1)	R0−1	0	1	0	E,3

NOTES:

A. IE=1, TPA, TPB suppressed, state=S1.

B BUS=0 for entire cycle.

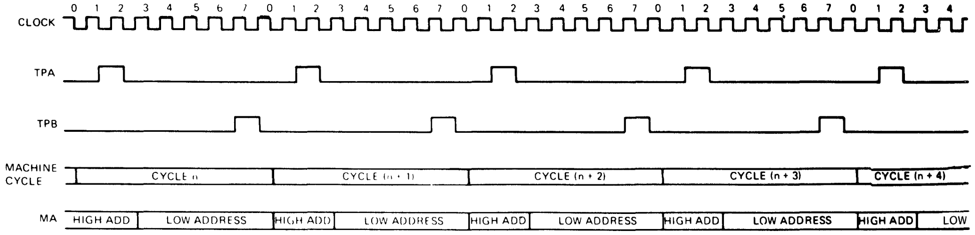
C. Next state always S1.

D. Wait for DMA or INTERRUPT.

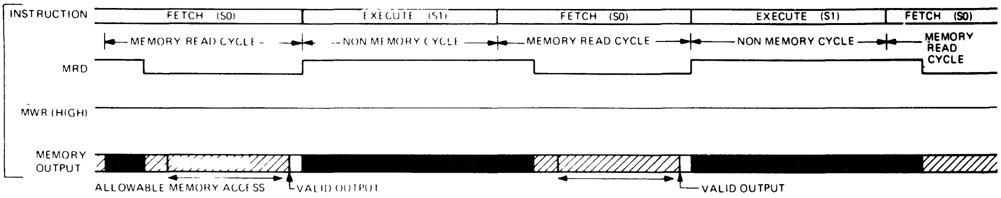
E. Suppress TPA, wait for DMA

F. IN REQUEST has priority over OUT REQUEST.

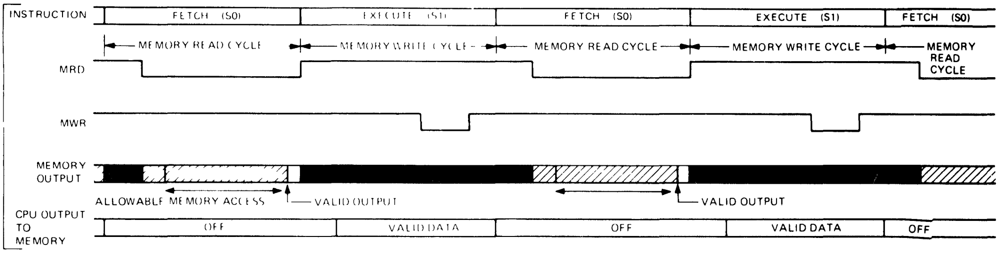
G. Number refers to machine cycle. See Fig 13 timing waveforms for machine cycles 1 through 9.



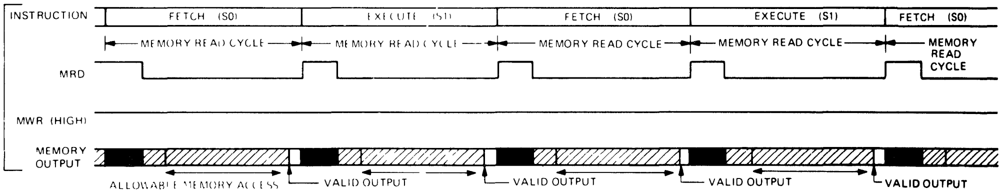
General timing waveforms.



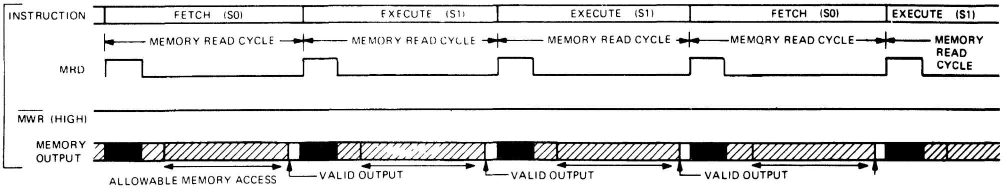
No. 1 Non-memory-cycle timing waveforms



No. 2 Memory write-cycle timing waveforms



No. 3 Memory read-cycle timing waveforms.

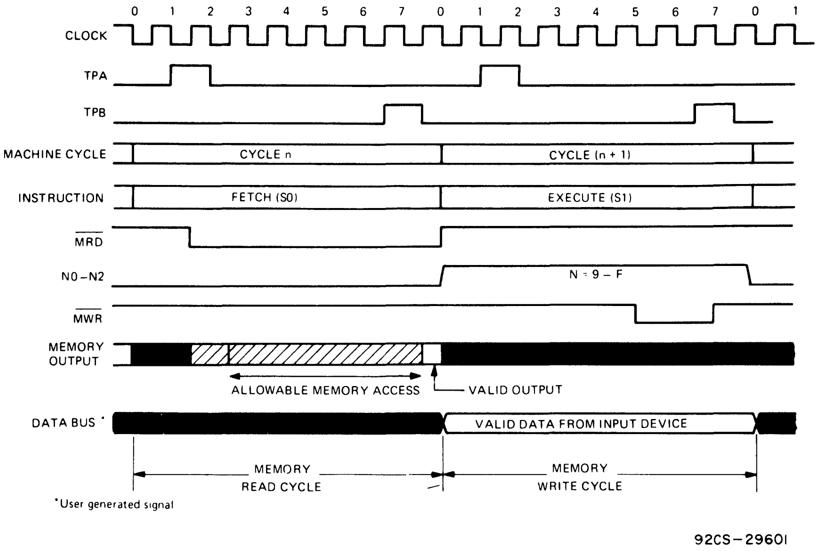


No. 4 Long-branch or long-skip-cycle timing waveforms.

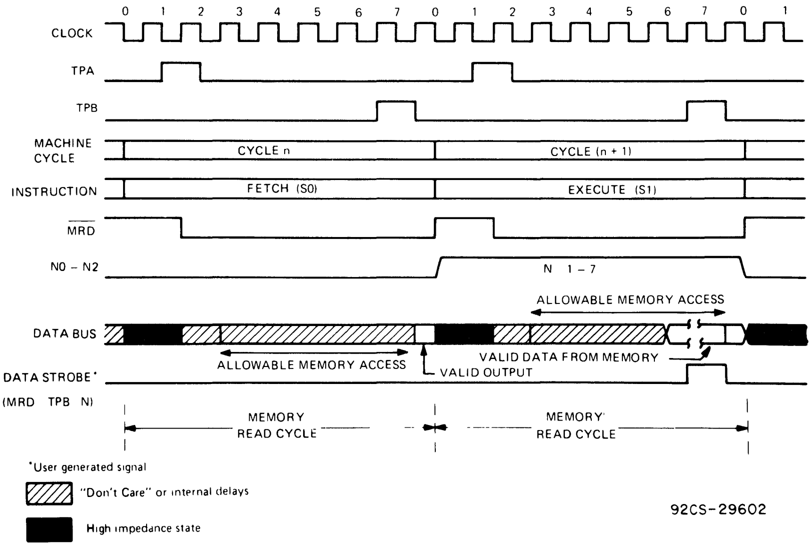
▨ Don't Care or internal delays ■ High impedance state

92CL-29600

Fig. 13 - Machine-cycle timing waveforms (propagation delays not shown).

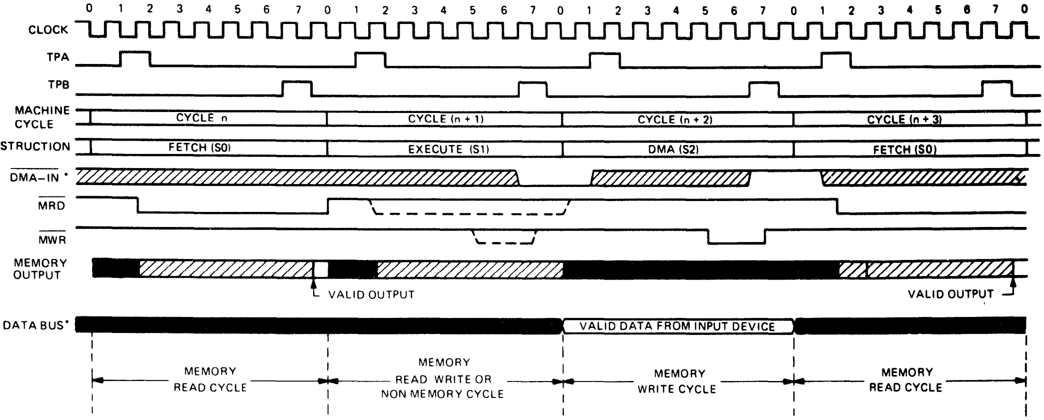


No. 5 Input-cycle timing waveforms.



No. 6 Output-cycle timing waveforms.

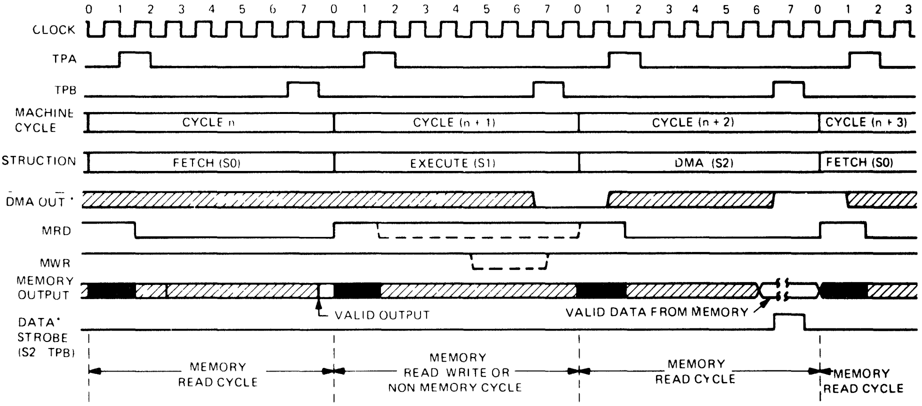
Fig. 13 - Machine-cycle timing waveforms (propagation delays not shown). Continued.



*User generated signal

92CS-29603

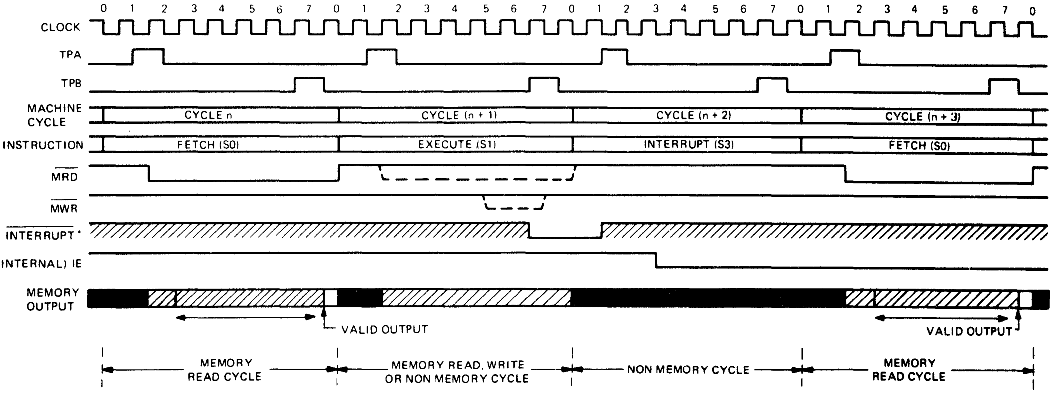
No. 7 DMA-IN-cycle timing waveforms.



*User generated signal

92CM-29604RI

No. 8 DMA-OUT-cycle timing waveforms.



*User generated signal

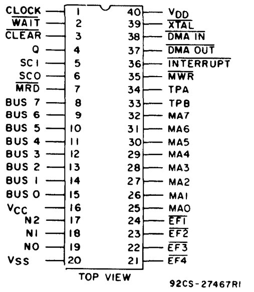
▨ "Don't Care" or internal delays ■ High impedance state

No. 9 INTERRUPT-cycle timing waveforms.

92CM-29605

*Fig. 13 - Machine-cycle timing waveforms (propagation delays not shown). **Continued.***

CDP1802BC



TERMINAL ASSIGNMENT

CMOS 8-Bit Microprocessor

Features:

- *Minimum instruction fetch-execute time of 3.2 μs (maximum clock frequency = 5 MHz) at V_{DD} = 5 V*
- *Any combination of standard RAM and ROM up to 65,536 bytes*
- *Operates with slow memories, up to 775 ns access time at f_{CL} = 5 MHz*
- *8-bit parallel organization with bidirectional data bus and multiplexed address bus*
- *16 x 16 matrix of registers for use as multiple program counters, data pointers, or data registers*
- *On-chip DMA, interrupt, and flag inputs*
- *Programmable single-bit output port*
- *91 easy-to-use instructions*

The RCA-CDP1802BC LSI CMOS 8-bit register-oriented central-processing unit (CPU) is designed for use as a general-purpose computing or control element in a wide range of stored-program systems or products.

The CDP1802BC includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

The 1800 series architecture is designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The 1800 series CPU also provides a synchronous interface to memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Further, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct memory-access modes.

The CDP1802BC has a recommended operating voltage range of 4 to 6.5 volts. These types are supplied in 40-lead dual-in-line side-brazed ceramic packages (D suffix), 40-lead dual-in-line plastic packages (E suffix), and 44-lead plastic chip-carrier (PCC) packages (Q suffix).

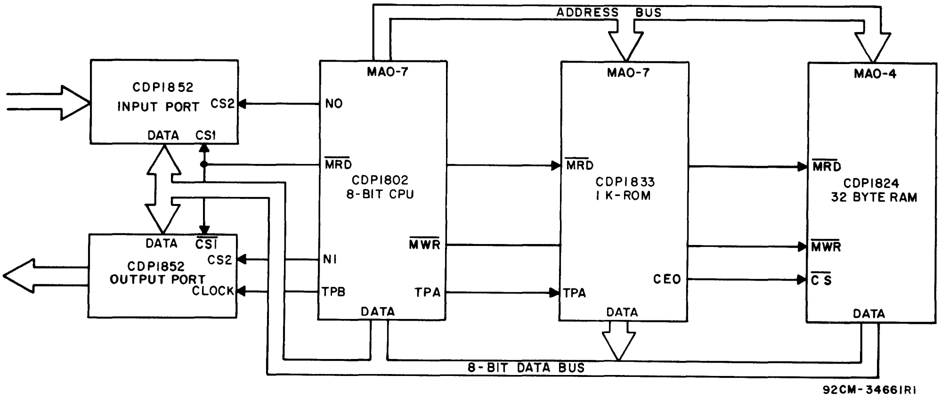


Fig 1 - Typical CDP1802BC small microprocessor system.

CDP1802BC

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}): (All voltages referenced to V_{SS} terminal)	
CDP1802BC	−0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A=−40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A=−55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A=+100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -40°C to +85°C (PACKAGE TYPE Q) *	500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A=FULL PACKAGE-TEMPERATURE RANGE	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	−55 to +125°C
PACKAGE TYPE E and Q	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16±1/32 in. (1.59±0 79 mm) from case for 10 s max.	+265°C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

OPERATING CONDITIONS at T_A=-40°C to +85°C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS		LIMITS		UNITS
	V_{CC}[1] (V)	V_{DD} (V)	CDP1802BC Min.	CDP1802BC Max.	
DC Operating Voltage Range	—	—	4.0	6.5	V
Input Voltage Range	—	—	V_{SS}	V_{DD}	
Maximum Clock Input Rise or Fall Time, t_r,t_f	4 to 6.5	4 to 6.5	—	1	µs
Minimum Instruction Time[2]	5	5	3.2	—	
Maximum DMA Transfer Rate	5	5	—	667	KBytes/s
Maximum Clock Input Frequency, f_{CL} Load Capacitance (C_L)=50 pF	5	5	DC	5	MHz

[1] V_{CC} must never exceed V_{DD}.

[2] Equals 2 machine cycles—one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles—one Fetch and two Execute operations.

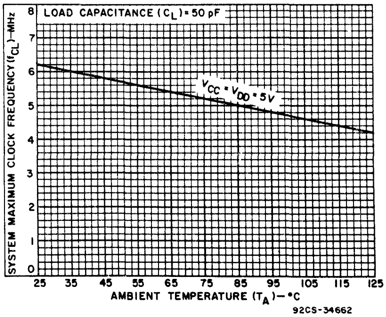


Fig. 2 - Typical maximum clock frequency as a function of temperature.

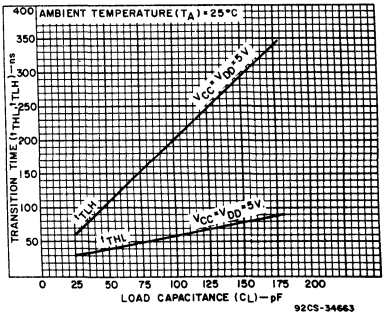
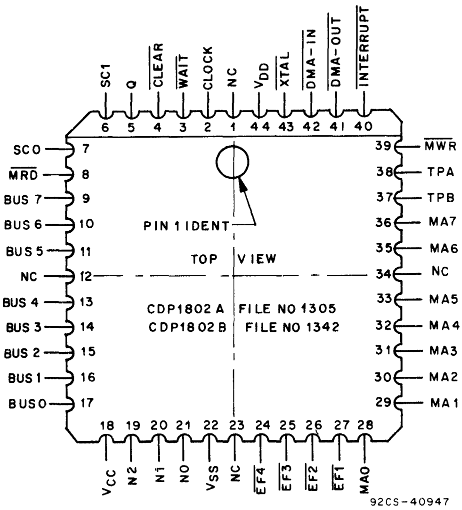


Fig. 3 - Typical transition time vs. load capacitance.

TERMINAL ASSIGNMENT



Plastic Chip-Carrier (PCC) Package

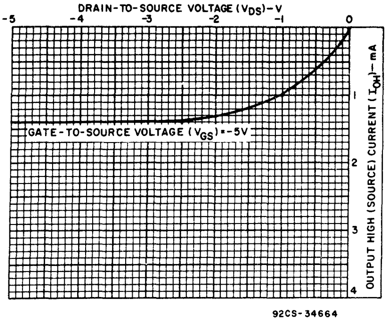


Fig. 4 - Minimum output high (source) current characteristics.

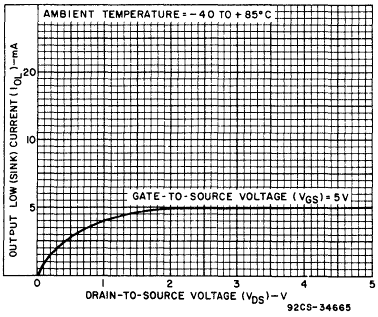


Fig. 5 - Minimum output low (sink) current characteristics.

CDP1802BC

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, except as noted.

CHARACTERISTIC		CONDITIONS			LIMITS			UNITS
		V_{OUT} (V)	V_{IN} (V)	V_{CC}, V_{DD} (V)	CDP1802BC			
					Min.	Typ.*	Max.	
Quiescent Device Current	I_{DD}	—	—	5	—	1	200	μA
Output Low Drive (Sink) Current (Except $\overline{XTAL}$)	I_{OL}	0.4	0,5	5	1.1	2.2	—	mA
$\overline{XTAL}$		0.4	5	5	170	350	—	μA
Output High Drive (Source) Current (Except $\overline{XTAL}$)	I_{OH}	4.6	0,5	5	−0.27	−0.55	—	mA
$\overline{XTAL}$		4.6	0	5	−125	−250	—	μA
Output Voltage Low-Level	V_{OL}	—	0,5	5	—	0	0.1	V
Output Voltage High Level	V_{OH}	—	0,5	5	4.9	5	—	
Input Low Voltage	V_{IL}	0.5,4.5	—	5	—	—	1.5	
Input High Voltage	V_{IH}	0.5,4.5	—	5	3.5	—	—	
$\overline{CLEAR}$ Input Voltage Schmitt Hysteresis	V_H	—	—	5	0.4	0.5	—	
Input Leakage Current	I_{IN}	Any Input	0,5	5	—	$\pm10^{-4}$	±1	μA
3-State Output Leakage Current	I_{OUT}	0,5	0,5	5	—	$\pm10^{-4}$	±1	
Total Power Dissipation, f=5 MHz$^{\Delta}$		—	—	5	—	15	30	mW
Minimum Data Retention Voltage	V_{DR}	$V_{DD}=V_{DR}$			—	2	2.4	V
Data Retention Current	I_{DR}	V_{DD}=2.4 V			—	0.5	—	μA
Input Capacitance	C_{IN}				—	5	7.5	pF
Output Capacitance	C_{OUT}				—	10	15	

*Typical values are for T_A=25° C and nominal V_{DD}.

$^{\Delta}$Idle "00" at M(0000), C_L=50 pF

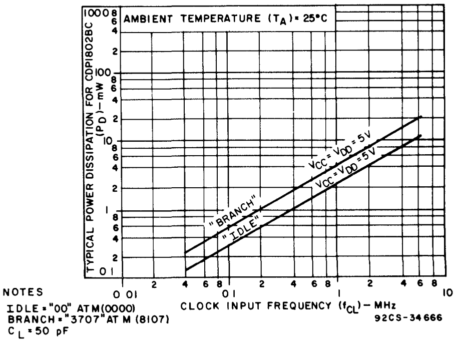


Fig. 6 - Typical power dissipation as a function of clock frequency for BRANCH instruction and IDLE instruction.

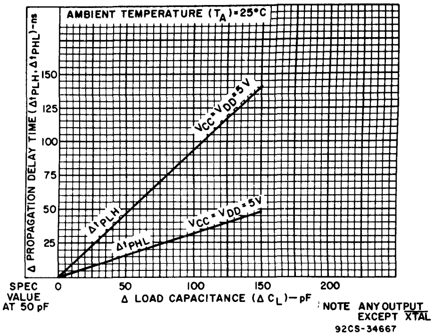


Fig. 7 - Typical change in propagation delay as a function of a change in load capacitance.

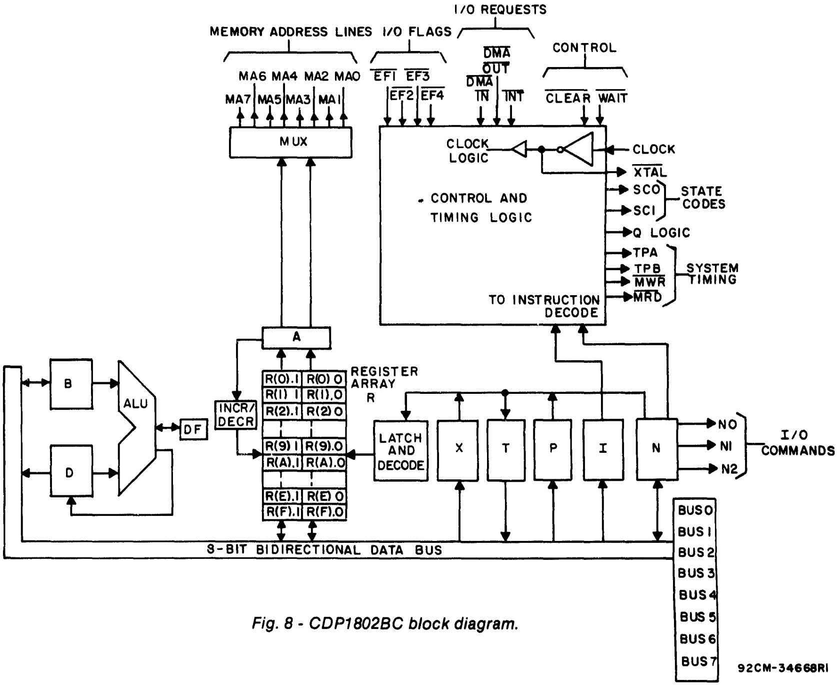


Fig. 8 - CDP1802BC block diagram.

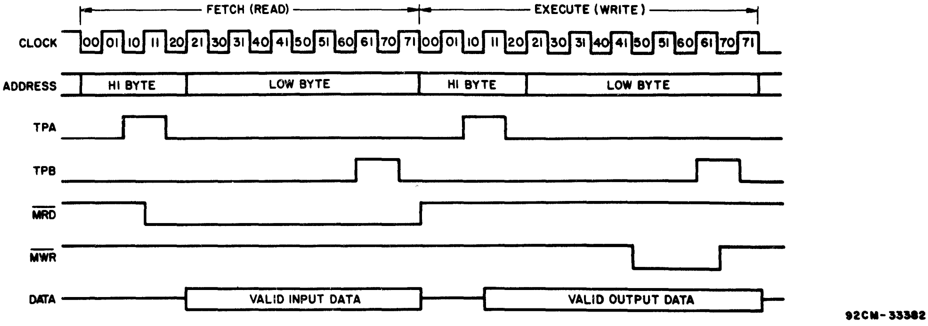


Fig. 9 - Basic dc timing waveforms, one instruction cycle.

SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus):

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O) Lines):

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal.

$\overline{\text{MRD}}=V_{CC}$: Data from I/O to CPU and Memory
$\overline{\text{MRD}}=V_{SS}$: Data from Memory to I/O

$\overline{\text{EF1}}$ to $\overline{\text{EF4}}$ (4 Flags):

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

$\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, $\overline{\text{DMA-OUT}}$ (3 I/O Requests)

These inputs are sampled by the CDP1802BC during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and Interrupt requests, DMA-IN has priority followed by DMA-OUT and then Interrupt.

SC0, SC1, (2 State Code Lines):

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA. H=V_{CC}, L=V_{SS}.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB (2 Timing Pulses):

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

MA0 to MA7 (8 Memory Address Lines):

In each cycle, the higher-order byte of a 16-bit CPU memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64K bytes.

$\overline{\text{MWR}}$ (Write Pulse):

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{\text{MRD}}$ (Read Level):

A low level on $\overline{\text{MRD}}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, $\overline{\text{MRD}}$ is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction. For additional information see Table I.

Q:

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK:

Input for externally generated single-phase clock. A typical clock frequency is 5 MHz at $V_{CC}= V_{DD}= 5$ volts. The clock is counted down internally to 8 clock pulses per machine cycle.

$\overline{\text{XTAL}}$:

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{\text{XTAL}}$) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be required at terminals 1 and 39. For additional information, see ICAN-6565.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$ (2 Control Lines):

Provide four control modes as listed in the following truth table:

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

V_{DD}, V_{SS}, V_{CC} (Power Levels):

The internal voltage supply V_{DD} is isolated from the Input/Output voltage supply V_{CC} so that the processor may operate at maximum speed while interfacing with peripheral devices operating at lower voltage. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}. The recommended input voltage swing is V_{SS} to V_{CC}.

ARCHITECTURE

The CPU block diagram is shown in Fig. 8. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. the D register (either of the two bytes can be gated to D);
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

With two exceptions, CPU instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and third if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. indicate to the I/O devices a command code or device-selection code for peripherals;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions (70-73 and 78-7B);
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations F1-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions — 70-73, 78, 60, F0.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the 1800-series architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, four instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

The Q Flip Flop

An internal flip flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a microprocessor output.

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request occurs and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Interrupt Enable is automatically de-activated to inhibit further interruptions. The user's interrupt routine is now in control; the contents of T may be saved by means of a single instruction (78) in the memory location pointed to by R(X). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with a single instruction (70 or 71). The Interrupt-Enable flip flop can be activated to permit further interrupts or can be disabled to prevent them.

CDP1802BC

CPU Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer

N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nibble)
IE	1 Bit	Interrupt Enable
Q	1 Bit	Output Flip Flop

CDP1802 Control Modes

The $\overline{\text{WAIT}}$ and $\overline{\text{CLEAR}}$ lines provide four control modes as listed in the following truth table:

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	LOAD
L	H	RESET
H	L	PAUSE
H	H	RUN

The function of the modes are defined as follows:

Load

Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

Reset

Registers I, N, Q are reset, IE is set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Powerup reset can be realized by connecting an RC network directly to the CLEAR pin, since it has a Schmitt-triggered input, see Fig. 10.

Pause

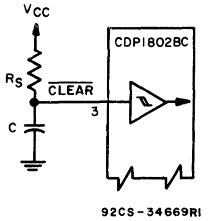
Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RUN-MODE STATE TRANSITIONS

The CDP1802BC CPU state transitions when in the RUN and RESET modes are shown in Fig. 11. Each machine cycle requires the same period of time, 8 clock pulses, except the initialization cycle, which requires 9 clock pulses. The execution of an instruction requires either two or three machine cycles, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response. Table II shows the conditions on Data Bus and Memory-Address lines during all machine states.



The RC time constant should be greater than the oscillator start-up time (typically 20 ms).

Fig. 10 - Reset diagram.

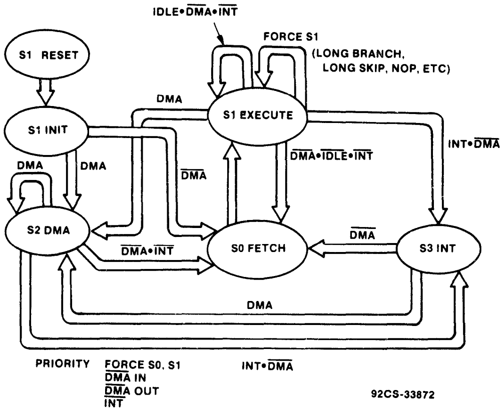

IDLE•$\overline{\text{DMA}}$•$\overline{\text{INT}}$
FORCE S1
(LONG BRANCH, LONG SKIP, NOP, ETC)
S1 RESET
S1 INIT
DMA
S1 EXECUTE
INT•$\overline{\text{DMA}}$
$\overline{\text{DMA}}$•$\overline{\text{IDLE}}$•$\overline{\text{INT}}$
DMA
DMA
$\overline{\text{DMA}}$
S2 DMA
$\overline{\text{DMA}}$•$\overline{\text{INT}}$
S0 FETCH
$\overline{\text{DMA}}$
S3 INT
DMA
PRIORITY
FORCE S0, S1
$\overline{\text{DMA}}$ IN
$\overline{\text{DMA}}$ OUT
$\overline{\text{INT}}$
INT•$\overline{\text{DMA}}$
92CS-33872

Fig. 11 - State transition diagram.

INSTRUCTION SET

The CPU instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where
W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)

Operation Notation
M(R(N)) → D; R(N) + 1 → R(N)

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I — INSTRUCTION SUMMARY (See Notes following table, pp. 11 and 12)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N))→D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N))→D; (RN)+1 →R(N)
LOAD VIA X	LDX	F0	M(R(X))→D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X))→D; R(X)+1→R(X)
LOAD IMMEDIATE	LDI	F8	M(R(P))→D; R(P)+1→R(P)
STORE VIA N	STR	5N	D→M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D→M(R(X)); R(X)−1→R(X)
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N)+1→R(N)
DECREMENT REG N	DEC	2N	R(N)−1→R(N)
INCREMENT REG X	IRX	60	R(X)+1→R(X)
GET LOW REG N	GLO	8N	R(N).0→D
PUT LOW REG N	PLO	AN	D→R(N).0
GET HIGH REG N	GHI	9N	R(N).1→D
PUT HIGH REG N	PHI	BN	D→R(N).1
LOGIC OPERATIONS∮			
OR	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D→D; R(P)+1→R(P)
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D→D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D→D; R(P)+1→R(P)
AND	AND	F2	M(R(X)) AND D→D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D→D; R(P)+1→R(P)
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)→DF, O→MSB(D)
SHIFT RIGHT WITH CARRY	SHRC }	76§	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
RING SHIFT RIGHT	RSHR }		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)
SHIFT LEFT WITH CARRY	SHLC }	7E§	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	RSHL }		

CDP1802BC

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS ¶			
ADD	ADD	F4	M(R(X))+D→DF, D
ADD IMMEDIATE	ADI	FC	M(R(P))+D→DF,D; R(P)+1→R(P)
ADD WITH CARRY	ADC	74	M(R(X))+D+DF→DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P))+D+DF→DF, D R(P)+1→R(P)
SUBTRACT D	SD	F5	M(R(X))−D→DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P))−D→DF, D; R(P)+1→R(P)
SUBTRACT D WITH BORROW	SDB	75	M(R(X))−D−(NOT DF)→DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P))−D−(NOT DF)→DF, D; R(P)+1→R(P)
SUBTRACT MEMORY	SM	F7	D−M(R(X))→DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D−M(R(P))→DF, D; R(P)+1→R(P)
SUBTRACT MEMORY WITH BORROW	SMB	77	D−M(R(X))−(NOT DF)→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D−M(R(P))−(NOT DF)→DF, D R(P)+1→R(P)
BRANCH INSTRUCTIONS—SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38§	R(P)+1→R(P)
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF DF=1	BDF	33§	IF DF=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B§	IF DF=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	BQ	31	IF Q=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF1=1 ($\overline{EF1}=V_{SS}$)	B1	34	IF EF1=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF1=0 ($\overline{EF1}=V_{CC}$)	BN1	3C	IF EF1=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF2=1 ($\overline{EF2}=V_{SS}$)	B2	35	IF EF2=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF2=0 ($\overline{EF2}=V_{CC}$)	BN2	3D	IF EF2=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF3=1 ($\overline{EF3}=V_{SS}$)	B3	36	IF EF3=1, M(R(P))→R(P).0 ELSE R(P)+1→R(P)
SHORT BRANCH IF EF3=0 ($\overline{EF3}=V_{CC}$)	BN3	3E	IF EF3=0, M(R(P))→R(P).0 ELSE R(P)+1→R(P)

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS—SHORT BRANCH			

SHORT BRANCH IF EF4=1 ($\overline{EF4}=V_{SS}$)	B4	37	IF EF4=1, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

SHORT BRANCH IF EF4=0 ($\overline{EF4}=V_{CC}$)	BN4	3F	IF EF4=0, M(R(P))→R(P).0
			ELSE R(P)+1→R(P)

BRANCH INSTRUCTIONS—LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P)+1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8§	R(P)+2→R(P)

LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1
			M(R(P)+1)→R(P).0
			ELSE R(P)+2→R(P)

LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1
			M(R(P)+1)→R(P).0
			ELSE R(P)+2→R(P)

LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1
			M(R(P)+1)→R(P).0
			ELSE R(P)+2→R(P)

LONG BRANCH IF DF=0	LBNF	CB	IF DF=0, M(R(P))→R(P).1
			M(R(P)+1)→R(P).0
			ELSE R(P)+2→R(P)

LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1
			M(R(P)+1)→R(P).0
			ELSE R(P)+2→R(P)

LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1
			M(R(P)+1)→R(P).0
			ELSE R(P)+2→R(P)

SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38§	R(P)+1→R(P)
LONG SKIP (SEE NLBR)	LSKP	C8§	R(P)+2→R(P)

LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P)+2→R(P)
			ELSE CONTINUE

LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P)+2→R(P)
			ELSE CONTINUE

LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P)+2→R(P)
			ELSE CONTINUE

LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P)+2→R(P)
			ELSE CONTINUE

LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P)+2→R(P)
			ELSE CONTINUE

LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P)+2→R(P)
			ELSE CONTINUE

LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P)+2→R(P)
			ELSE CONTINUE

CDP1802BC

TABLE I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)−1→R(2)
RETURN	RET	70	M(R(X))→(X,P); R(X)+1→R(X) 1→IE
DISABLE	DIS	71	M(R(X))→(X,P); R(X)+1→R(X) 0→IE
INPUT-OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS;R(X)+1→R(X); N LINES=1
OUTPUT 2	OUT 2	62	M(R(X))→BUS;R(X)+1→R(X); N LINES=2
OUTPUT 3	OUT 3	63	M(R(X))→BUS;R(X)+1→R(X); N LINES=3
OUTPUT 4	OUT 4	64	M(R(X))→BUS;R(X)+1→R(X); N LINES=4
OUTPUT 5	OUT 5	65	M(R(X))→BUS;R(X)+1→R(X); N LINES=5
OUTPUT 6	OUT 6	66	M(R(X))→BUS;R(X)+1→R(X); N LINES=6
OUTPUT 7	OUT 7	67	M(R(X))→BUS;R(X)+1→R(X); N LINES=7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES=1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES=2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES=3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES=4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES=5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES=6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES=7

∮THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF. AFTER AN ADD INSTRUCTION:
DF=1 DENOTES A CARRY HAS OCCURRED
DF=0 DENOTES A CARRY HAS NOT OCCURRED
AFTER A SUBTRACT INSTRUCTION
DF=1 DENOTES NO BORROW D IS A TRUE POSITIVE NUMBER
DF=0 DENOTES A BORROW. D IS TWO'S COMPLEMENT
THE SYNTAX "−(NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

§THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC EACH MNEMONIC IS INDIVIDUALLY LISTED

#AN IDLE INSTRUCTION INITIATES A REPEATING S1 CYCLE. THE PROCESSOR WILL CONTINUE TO IDLE UNTIL AN I/O REQUEST ($\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, OR $\overline{\text{DMA-OUT}}$) IS ACTIVATED. WHEN THE REQUEST IS ACKNOWLEDGED, THE IDLE CYCLE IS TERMINATED AND THE I/O REQUEST IS SERVICED, AND THEN NORMAL OPERATION IS RESUMED.

Notes for TABLE I

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch +2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high- and low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, C_L=50 pF, V_{DD}±5%, except as noted.

CHARACTERISTIC		V_{CC} (V)	V_{DD} (V)	LIMITS Typ.●	LIMITS Max.	UNITS
Propagation Delay Times.						ns
Clock to TPA, TPB	t_{PLH}, t_{PHL}	5	5	200	300	
Clock-to-Memory High-Address Byte	t_{PLH}, t_{PHL}	5	5	475	525	
Clock-to-Memory Low-Address Byte Valid	t_{PLH}, t_{PHL}	5	5	175	250	
Clock to $\overline{MRD}$	t_{PLH}, t_{PHL}	5	5	175	275	
Clock to $\overline{MWR}$	t_{PLH}, t_{PHL}	5	5	175	225	
Clock to (CPU DATA to BUS) Valid	t_{PLH}, t_{PHL}	5	5	250	375	
Clock to State Code	t_{PLH}, t_{PHL}	5	5	250	400	
Clock to Q	t_{PLH}, t_{PHL}	5	5	200	300	
Clock to N (0-2)	t_{PLH}, t_{PHL}	5	5	275	350	
Minimum Setup and Hold Times·						
Data Bus Input Setup	t_{SU}	5	5	−20	0	
Data Bus Input Hold	t_H■	5	5	125	150	
$\overline{DMA}$ Setup	t_{SU}	5	5	0	30	
$\overline{DMA}$ Hold	t_H■	5	5	100	150	
Interrupt Setup	t_{SU}	5	5	−75	0	
Interrupt Hold	t_H■	5	5	75	125	
$\overline{WAIT}$ Setup	t_{SU}	5	5	20	40	
$\overline{EF1\text{-}4}$ Setup	t_{SU}	5	5	−30	0	
$\overline{EF1\text{-}4}$ Hold	t_H■	5	5	100	150	
Minimum Pulse Width Times.						
$\overline{CLEAR}$ Pulse Width	t_{WL}■	5	5	100	150	
$\overline{CLOCK}$ Pulse Width	t_{WL}	5	5	90	100	

●Typical values are for T_A=25°C and nominal V_{DD}

■Maximum limits of minimum characteristics are the values above which all devices function

Notes for TABLE I (Continued)

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

   The short-branch instruction can
   - a) Branch unconditionally
   - b) Test for D=0 or D≠0
   - c) Test for DF=0 or DF=1
   - d) Test for Q=0 or Q=1
   - e) Test the status (1 or 0) of the four EF flags
   - f) Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

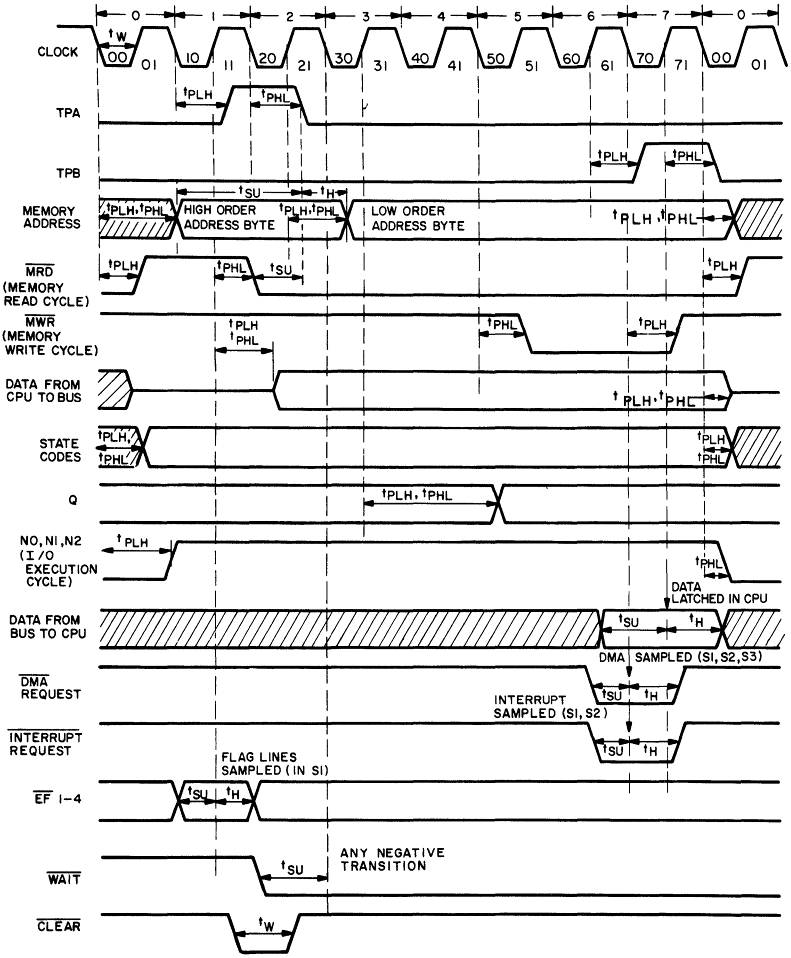
   The Long-Skip instructions take three cycles to complete (1 fetch +2 execute).

   They can:
   - a) Skip unconditionally
   - b) Test for D=0 or D≠0
   - c) Test for DF=0 or DF=1
   - d) Test for Q=0 or Q=1
   - e) Test for IE=1

   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken.

   Execution is continued by fetching the next instruction in sequence.

CDP1802BC



NOTES·

1 THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE

2 ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS

3 SHADED AREAS INDICATE "DON'T CARE" OR UNDEFINED STATE; MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD

92CL-33869R2

Fig. 12 - Timing waveforms.

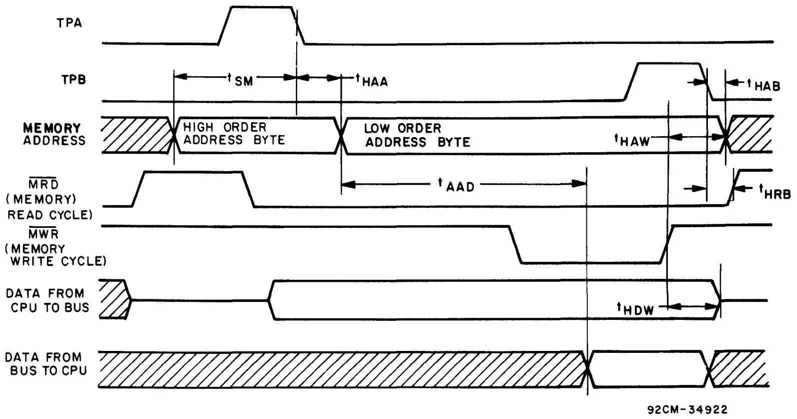


Fig. 13 - Clock frequency dependent relative timing waveforms.

TIMING SPECIFICATIONS as a function of T(T=1/f_{CLOCK}) at T_A=-40 to +85°C

CHARACTERISTIC		V_{CC} (V)	V_{DD} (V)	LIMITS		UNITS
				Min.	Typ.•	
High-Order Memory-Address Byte Set Up to TPA ↘ Time	t_{SM}	5	5	2T-325	2T-275	ns
High-Order Memory-Address Byte Hold after TPA Time	t_{HAA}	5	5	T/2-25	T/2-15	
Low-Order Memory-Address Byte Hold after WR Time	t_{HAW}	5	5	T-30	T+0	
CPU Data to Bus Hold after WR Time	t_{HDW}	5	5	T-175	T-125	
Low-Order Memory-Address Byte Hold after TPB Time	t_{HAB}	5	5	T/2+0	T/2+100	
$\overline{MRD}$ Hold to TPB Time	t_{HRB}	5	5	T/2-25	T/2+0	
Required Memory Access Time Address to Data	t_{AAD}	5	5	5T-225	5T-175	
$\overline{MRD}$ to TPA (↘)	t_{SU}	5	5	T/2-20	T/2-15	

•Typical values are for T_A=25° C and nominal V_{DD}

CDP1802BC

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES
S1	RESET			0→I,N,Q,X,P; 1→IE	00	XXXX	1	1	0	A
S1	INITIALIZE NOT PROGRAMMER ACCESSIBLE			0000→R	00	XXXX	1	1	0	B
S0	FETCH			MRP→I, N; RP+1→RP	MRP	RP	0	1	0	C
S1	0	0	IDL	IDLE	MR0	R0	0	1	0	D,3
	0	1-F	LDN	MRN→D	MRN	RN	0	1	0	3
	1	0-F	INC	RN+1→RN	FLOAT	RN	1	1	0	1
	2	0-F	DEC	RN−1→RN	FLOAT	RN	1	1	0	1

	3	0-F	SHORT BRANCH	TAKEN;
				MRP→RP.0
				NOT TAKEN;
				RP+1→RP
					MRP	RP	0	1	0	3

	4	0-F	LDA	MRN→D; RN+1→RN	MRN	RN	0	1	0	3
	5	0-F	STR	D→MRN	D	RN	1	0	0	2
	6	0	IRX	RX+1→RX	MRX	RX	0	1	0	2
	6	1	OUT 1	MRX→BUS; RX+1→RX	MRX	RX	0	1	1	6
		2	OUT 2						2	
		3	OUT 3						3	
		4	OUT 4						4	
		5	OUT 5						5	
		6	OUT 6						6	
		7	OUT 7						7	
		9	INP 1	BUS→MRX,D	DATA FROM I/O DEVICE	RX	1	0	1	5
		A	INP 2						2	
		B	INP 3						3	
		C	INP 4						4	
		D	INP 5						5	
		E	INP 6						6	
		F	INP 7						7	
	7	0	RET	MRX→(X,P); RX+1→RX; 1→IE	MRX	RX	0	1	0	3
		1	DIS	MRX→(X,P); RX+1→RX; 0→IE	MRX	RX	0	1	0	3
		2	LDXA	MRX→D; RX+1→RX	MRX	RX	0	1	0	3
		3	STXD	D→MRX; RX−1→RX	D	RX	1	0	0	2
		4	ADC	MRX+D+ DF→DF,D	MRX	RX	0	1	0	3

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (CONT'D)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES	NOTES[G]
S1	7	5	SDB	MRX–D–DFN→DF,D	MRX	RX	0	1	0	3
		6	SHRC	LSB(D)→DF; DF→MSB(D)	FLOAT	RX	1	1	0	1
		7	SMB	D–MRX–DFN→DF,D	MRX	RX	0	1	0	3
		8	SAV	T→MRX	T	RX	1	0	0	2
		9	MARK	(X,P)→T, MR2; P→X; R2–1→R2	T	R2	1	0	0	2
		A	REQ	0→Q	FLOAT	RP	1	1	0	1
		B	SEQ	1→Q	FLOAT	RP	1	1	0	1
		C	ADCI	MRP+D+DF→DF,D; RP+1	MRP	RP	0	1	0	3
		D	SDBI	MRP–D–DFN→DF,D; RP+1	MRP	RP	0	1	0	3
		E	SHLC	MSB(D)→DF, DF→LSB(D)	FLOAT	RP	1	1	0	1
		F	SMBI	D–MRP–DFN→DF,D; RP+1	MRP	RP	0	1	0	3
	8	0-F	GLO	RN.0→D	RN.0	RN	1	1	0	1
	9	0-F	GHI	RN 1→D	RN 1	RN	1	1	0	1
	A	0-F	PLO	D→RN.0	D	RN	1	1	0	1
	B	0-F	PHI	D→RN.1	D	RN	1	1	0	1
S1#1	C	0-3, 8-B	LONG BRANCH	TAKEN MRP→B; RP+1→RP	MRP	RP	0	1	0	4
#2				TAKEN: B→RP 1; MRP→RP.0	M(RP+1)	RP+1	0	1	0	4
S1#1				NOT TAKEN: RP+1→RP	MRP	RP	0	1	0	4
#2				NOT TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0	4
S1#1		5 6 7 C D E F	LONG SKIP	TAKEN RP+1→RP	MRP	RP	0	1	0	4
#2				TAKEN RP+1→RP	M(RP+1)	RP+1	0	1	0	4
S1#1				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0	4
#2				NOT TAKEN· NO OPERATION	MRP	RP	0	1	0	4
S1#1		4	NOP	NO OPERATION	MRP	RP	0	1	0	4
#2				NO OPERATION	MRP	RP	0	1	0	4

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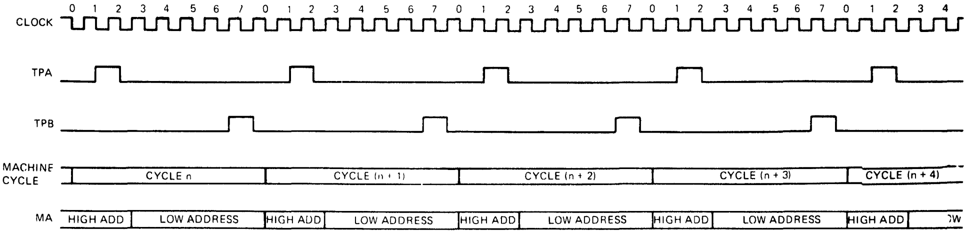
TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (CONT'D)

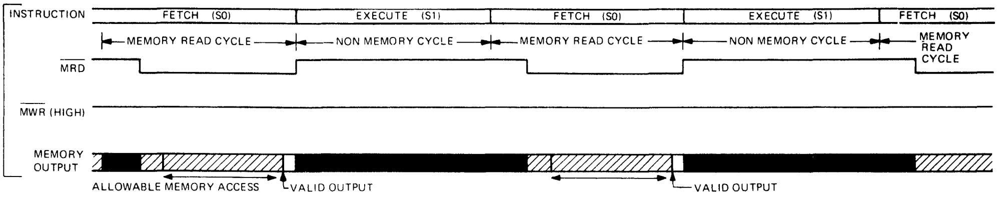
STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	N LINES	NOTES[G]
S1	D	0-F	SEP	N→P	NN	RN	1	1	0	1
	E	0-F	SEX	N→X	NN	RN	1	1	0	1
	F	0	LDX	MRX→D	MRX	RX	0	1	0	3
		1	OR	MRX OR D→D	MRX	RX	0	1	0	3
		2	AND	MRX AND D→D						
		3	XOR	MRX XOR D→D						
		4	ADD	MRX+D→DF,D						
		5	SD	MRX–D→DF,D						
		7	SM	D–MRX→DF,D						
		6	SHR	LSB(D)→DF; 0→MSB(D)	FLOAT	RX	1	1	0	1
		8	LDI	MRP→D; RP+1→RP	MRP	RP	0	1	0	3
		9	ORI	MRP OR D→D; RP+1→RP						
		A	ANI	MRP AND D→D; RP+1→RP						
		B	XRI	MRP XOR D→D; RP+1→RP						
		C	ADI	MRP+D→DF,D; RP+1→RP						
		D	SDI	MRP–D→DF,D; RP+1→RP						
		F	SMI	D–MRP→DF,D; RP+1→RP						
		E	SHL	MSB(D)→DF; 0→LSB(D)	FLOAT	RP	1	1	0	1
S2	DMA IN			BUS→MR0; R0+1→R0	DATA FROM I/O DEVICE	R0	1	0	0	F, 7
	DMA OUT			MR0→BUS; R0+1→R0	MR0	R0	0	1	0	F, 8
S3	INTERRUPT			X,P→T, 0→IE 1→P; 2→X	FLOAT	RN	1	1	0	9
S1	LOAD			IDLE ($\overline{\text{CLEAR}}$, $\overline{\text{WAIT}}$=0)	M(R0–1)	R0–1	0	1	0	E,3

NOTES:

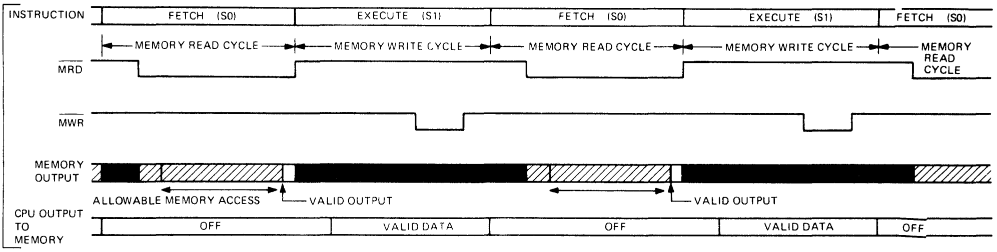
A. IE=1, TPA, TPB suppressed, state=S1.
B. BUS=0 for entire cycle.
C. Next state always S1.
D. Wait for DMA or INTERRUPT.
E. Suppress TPA, wait for DMA.
F. IN REQUEST has priority over OUT REQUEST.
G. Number refers to machine cycle. See Fig. 14 timing waveforms for machine cycles 1 through 9.



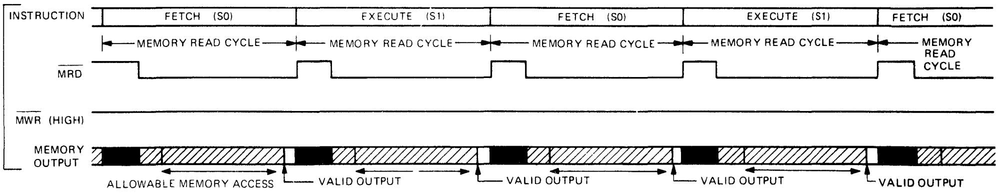
General timing waveforms.



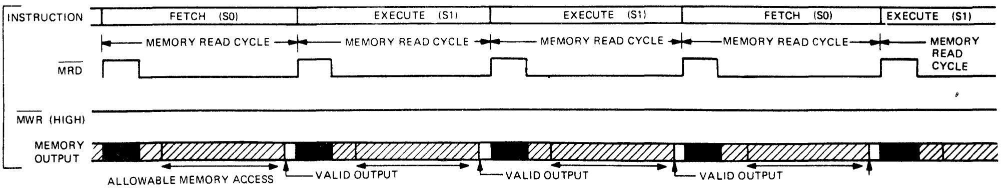
No. 1 Non-memory-cycle timing waveforms.



No. 2 Memory write-cycle timing waveforms.



No. 3 Memory read-cycle timing waveforms.

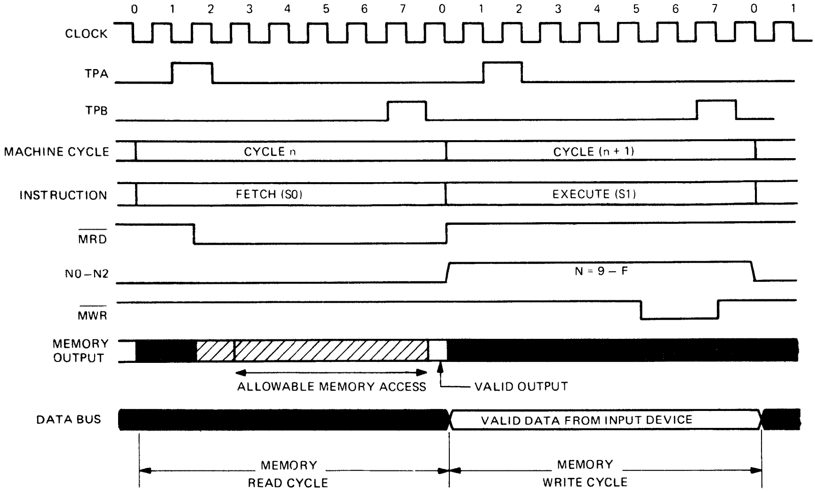


No. 4 Long-branch or long-skip-cycle timing waveforms.

▨ "Don't Care" or internal delays ■ High impedance state

92CL-29600

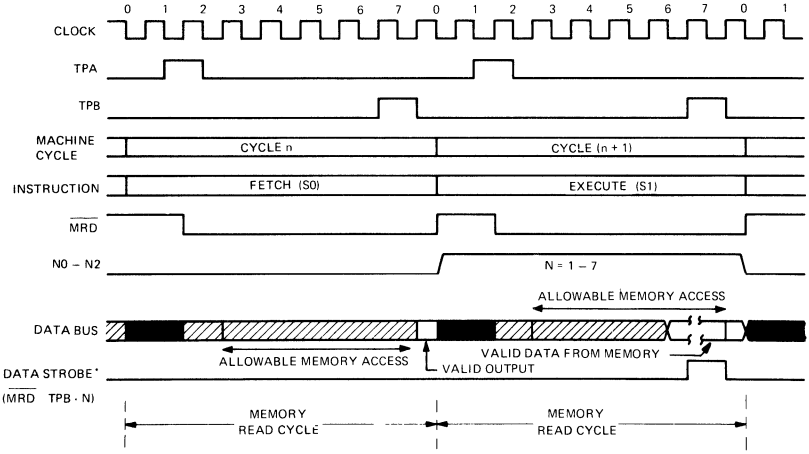
Fig. 14 - Machine-cycle timing waveforms (propagation delays not shown).



*User generated signal

92CS-29601

No. 5 Input-cycle timing waveforms.



*User generated signal

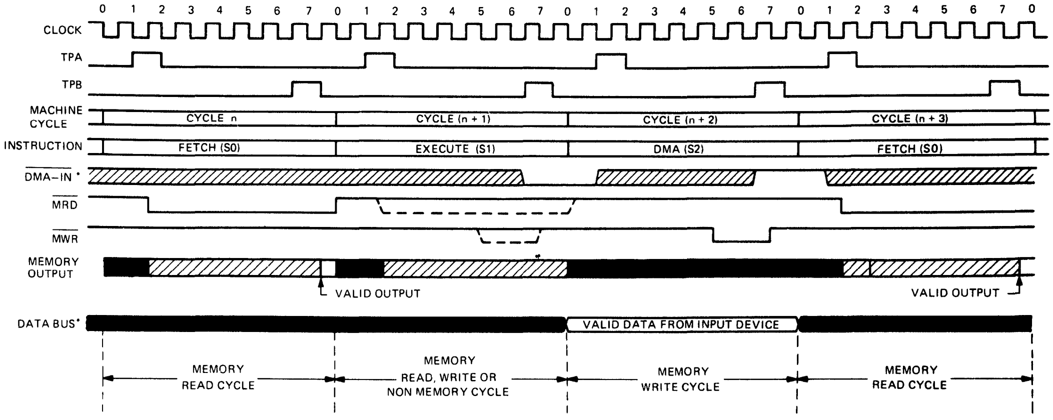
▨ "Don't Care" or internal delays

■ High impedance state

92CS-29602

No. 6 Output-cycle timing waveforms.

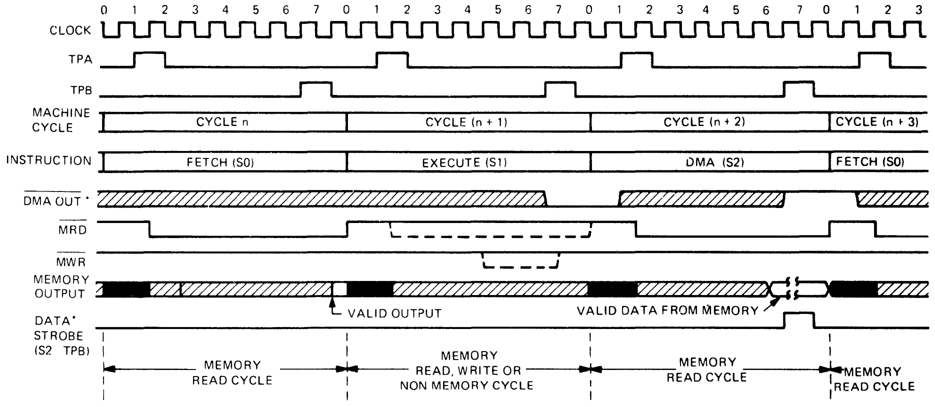
Fig. 14 - Machine-cycle timing waveforms (propagation delays not shown). Continued.



*User generated signal

92CS-29603

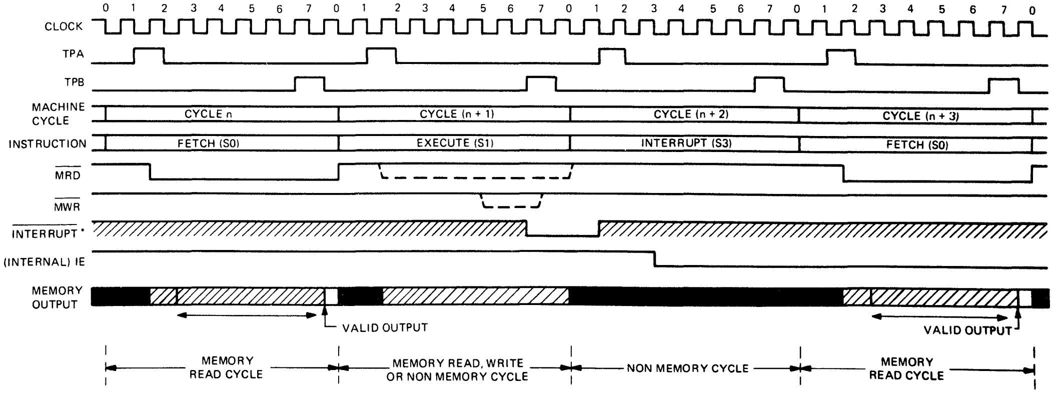
No. 7 DMA-IN-cycle timing waveforms.



*User generated signal

92CM-29604RI

No. 8 DMA-OUT-cycle timing waveforms.



*User generated signal

▨ "Don't Care" or internal delays ■ High impedance state

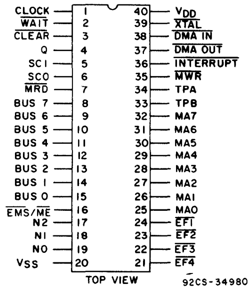
92CM-29605

No. 9 INTERRUPT-cycle timing waveforms.

Fig. 14 - Machine-cycle timing waveforms (propagation delays not shown). Continued.

CDP1804AC

TERMINAL ASSIGNMENT



CMOS 8-Bit Microcomputer With On-Chip RAM, ROM, and Counter/Timer

Performance Features:

- *Instruction time of 3.2 µs, -40 to +85° C*
- *123 instructions-upwards sofware compatible with CDP1802, CDP1805A, and CDP1806A*
- *BCD arithmetic instructions*
- *Low-power IDLE mode*
- *Pin compatible with CDP1802, CDP1805A, and CDP1806A except for terminal 16 (terminal 18 for chip-carrier package)*
- *64K-byte memory address capability*
- *2 K bytes of on-chip ROM*
- *64 bytes of on-chip RAM*
- *16 x 16 matrix of on-board registers*
- *On-chip crystal or RC controlled oscillator*
- *8-bit Counter/Timer*

The RCA-CDP1804AC is a functional and performance enhancement of the CDP1802, CDP1805A, and CDP1806A CMOS 8-bit register-oriented microprocessor series and is designed for use in a wide variety of general-purpose applications.

The CDP1804AC hardware enhancements include a 2K-byte ROM, a 64-byte RAM, and a 8-bit presettable down counter. The Counter/Timer, which generates an internal interrupt request, can be programmed for use in time-base, event-counting, and pulse-duration measurement applications. The Counter/Timer underflow output can also be directed to the Q output terminal.

The CDP1805AC and CDP1806AC which are identical to the CDP1804AC, except for the on-chip memory, should be used for CDP1804AC development purposes.

The CDP1804AC software enhancements include 32 more instructions than the CDP1802. The 32 additional software instructions include subroutine call and return capability, enhanced data transfer manipulation, counter/timer control, improved interrupt handling, single-instruction loop counting, and BCD arithmetic.

Upwards software and hardware compatibility are maintained when substituting a CDP1804AC for other CDP1800-series microprocessors. Pinout is identical except for the replacement of V_{CC} with $\overline{EMS}/\overline{ME}$.

The CDP1804AC has an operating voltage range of 4 V to 6.5 V and is supplied in a 40-lead hermetic dual-in-line ceramic package (D suffix), in a 40-lead dual-in-line plastic package (E suffix), and in a 44-lead plastic chip-carrier package (Q suffix).

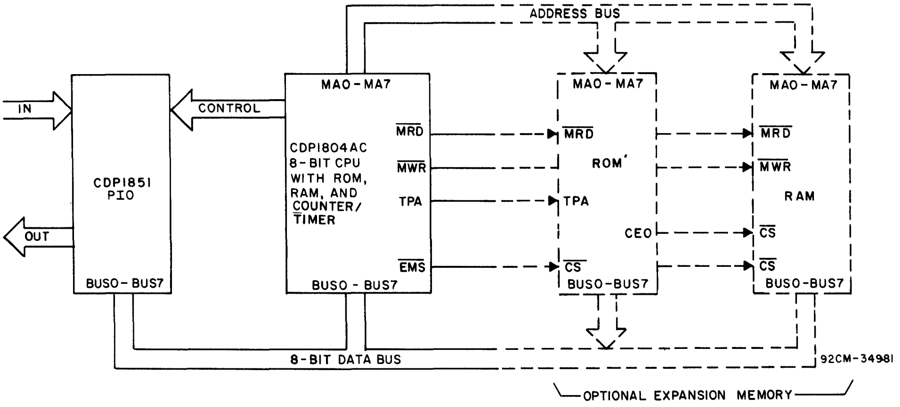


Fig. 1 - Typical CDP1804AC microprocessor system.

File Number **1371**

CDP1804AC

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):	
(Voltage referenced to V_{SS} Terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D).	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 +85° C (PACKAGE TYPE E)	Derate Linearly at 12 mW/° C to 200 mW
For T_A = -55 to +100° C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D)	Derate Linearly at 12 mW/° C to 200 mW
For T_A = -40° C to +85° C (PACKAGE TYPE Q)*	500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125° C
PACKAGE TYPE E AND Q	-40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in (1 59 ± 0 79 mm) from case for 10 s max	+265° C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

RECOMMENDED OPERATING CONDITIONS at T_A = -40 to +85° C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITION	LIMITS		UNITS
		CDP1804ACD CDP1804ACE		
	V_{DD} (V)	MIN.	MAX.	
DC Operating Voltage Range	—	4	6.5	V
Input Voltage Range	—	V_{SS}	V_{DD}	
Minimum Instruction Time* (f_{CL}=5 MHz)	5	3.2	—	μs
Maximum DMA Transfer Rate	5	—	0.625	Mbytes/s
Maximum Clock Input Frequency, Load Capacitance (CL) = 50 pF	5	DC	5	MHz
Maximum External Counter/Timer Clock Input Frequency to $\overline{EF1}$, $\overline{EF2}$ t_{CLX}	5	DC	2	

* Equals 2 machine cycles - one Fetch and one Execute operation for all instructions except Long Branch, Long Skip, NOP, and "68" family instructions, which are more than two cycles

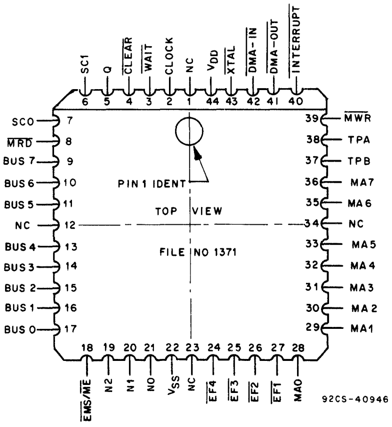
CDP1804AC

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS			UNITS
					CDP1804ACD, CDP1804ACE			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	50	200	µA
Output Low Drive (Sink) Current (Except $\overline{\text{XTAL}}$)	I_{OL}	0.4	0, 5	5	1.6	4	—	mA
$\overline{\text{XTAL}}$ Output	I_{OL}	0.4	5	5	0.2	0.4	—	
Output High Drive (Source) Current (Except $\overline{\text{XTAL}}$)	I_{OH}	4.6	0, 5	5	-1.6	-4	—	
$\overline{\text{XTAL}}$	I_{OH}	4.6	0	5	-0.1	-0.2	—	
Output Voltage Low-Level	V_{OL}	—	0, 5	5	—	0	0.1	V
Output Voltage High Level	V_{OH}	—	0, 5	5	4.9	5	—	
Input Low Voltage (BUS 0 — BUS 7, $\overline{\text{EMS}}/\overline{\text{ME}}$)	V_{IL}	0.5, 4.5	—	5	—	—	1.5	
Input High Voltage (BUS 0 — BUS 7, $\overline{\text{EMS}}/\overline{\text{ME}}$)	V_{IH}	0.5, 4.5	—	5	3.5	—	—	
Schmitt Trigger Input Voltage (Except BUS 0 — BUS 7, $\overline{\text{EMS}}/\overline{\text{ME}}$)								
Positive Trigger Threshold	V_P	0.5, 4.5	—	5	2.2	2.9	3.6	
Negative Trigger Threshold	V_N				0.9	1.9	2.8	
Hysteresis	V_H				0.3	0.9	1.6	
Input Leakage Current	I_{IN}	—	0, 5	5	—	±0.1	±5	µA
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	—	±0.2	±5	
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	
Total Power Dissipation$^\Delta$ Run		—	—	5	—	35	50	mW
Idle "00" at M(0000)		—	—	5	—	12	18	
Minimum Data Retention Voltage	V_{DR}	$V_{DD} = V_{DR}$			—	2	2.4	V
Data Retention Current	I_{DR}	V_{DD} = 2.4			—	25	100	µA

*Typical values are for T_A = 25° C and nominal V_{DD}. $^\Delta$External Clock: f=5 MHz, t_r,t_f=10 ns C_L=50 pF

TERMINAL ASSIGNMENT



44-Lead
Plastic Chip-Carrier
Package (Q Suffix)

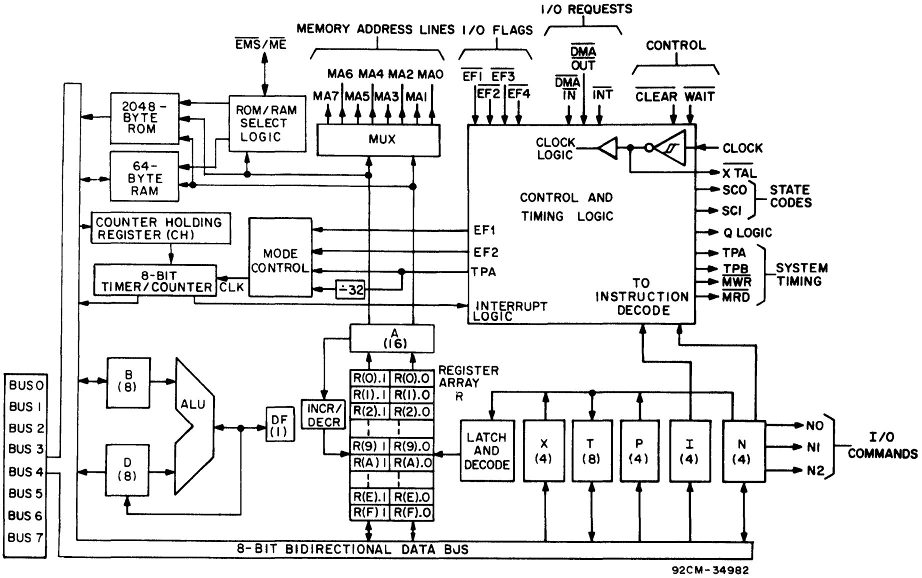


Fig. 2 - Block diagram for CDP1804AC.

Enhanced 1804AC Operation

ROM/RAM

The 2K-byte ROM is mask-programmable and mask-selectable in any 2K block of the available 64K address space in the RUN (ROM/RAM) mode. (The procedure is detailed in the Mask-Programming section at the end of the data sheet.)

The 64-byte RAM is mask-selectable in any 64-byte block of memory in the RUN (ROM/RAM) mode. It may also be externally selected via the $\overline{\text{ME}}$ input in the RUN (RAM only) mode.

The $\overline{\text{EMS}}/\overline{\text{ME}}$ pin serves a dual function. In the RUN (ROM/RAM) mode, $\overline{\text{EMS}}$ acts as an active low output to indicate when the internal ROM or RAM is not selected. This provides a convenient chip-select signal for any optional expansion memory devices and a stable-address latch signal for synchronous RAMs. In the RUN (RAM only) mode, $\overline{\text{ME}}$ acts as an active low input and is used to select the internal RAM, which is not mask-selected in this mode. Decoding is performed externally and the RAM may reside in any 64-byte block.

Timing

Timing for the CDP1804AC is the same as the CDP1802 microprocessor series, with the following exceptions:

- 4.5 clock cycles are provided for memory access instead of 5.
- Q changes 1/2 clock cycle earlier during the SEQ and REQ instructions.
- Flag lines ($\overline{\text{EF1}}$-$\overline{\text{EF4}}$) are sampled at the end of the S0 cycle instead of at the beginning of the S1 cycle.
- Pause can only occur on the low-to-high transition of either TPA or TPB, instead of any negative clock transition.

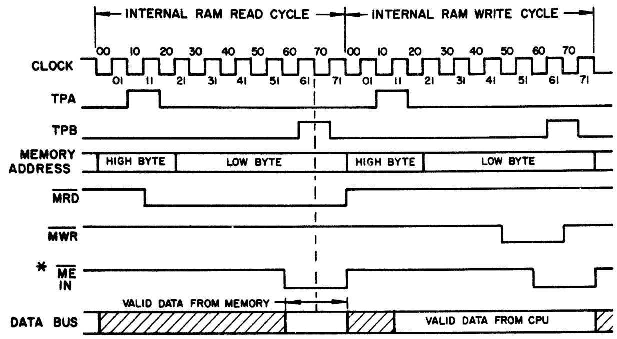
Special Features

Schmitt triggers are provided on all inputs, except $\overline{\text{EMS}}/\overline{\text{ME}}$, and BUS 0 - BUS 7, for maximum immunity from noise and slow signal transitions. A Schmitt trigger in the oscillator section allows operation with an RC or crystal.

The CDP1802 series LOAD mode is not retained. This mode ($\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$=0) is the RUN (ROM/RAM) mode on the CDP1804AC.

A low power mode is provided, which is initiated via the IDLE instruction. In this mode all external signals, except the oscillator, are stopped on the low-to-high transition of TPB. All outputs remain in their previous states, $\overline{\text{MRD}}$ is set to a logic "1", and the data bus floats. The IDLE mode is exited by a DMA or INT condition. The INT includes both external interrupts and interrupts generated by the Counter/Timer. The only restrictions are that the Timer mode, which uses the TPA ÷ 32 clock source, and the underflow condition of the Pulse Width Measurement modes are not available to exit the IDLE mode.

TIMING WAVEFORMS FOR POSSIBLE OPERATING MODES



*NOTE FOR RUN (RAM ONLY) MODE:
$\overline{\text{ME}}$ HAS A MINIMUM SETUP AND HOLD TIME WITH RESPECT TO THE BEGINNING OF CLOCK 70. FOR A MEMORY READ OPERATION, RAM DATA WILL APPEAR ON THE DATA BUS DURING THE TIME $\overline{\text{ME}}$ IS ACTIVE AFTER CLOCK 31. THE TIME SHOWN CAN BE LONGER, IF FOR INSTANCE, A DMA OUT OPERATION IS PERFORMED ON INTERNAL RAM DATA, TO ALLOW DATA ENOUGH TIME TO BE LATCHED INTO AN EXTERNAL DEVICE. THE INTERNAL RAM IS AUTOMATICALLY DESELECTED AT THE END OF CLOCK 71, INDEPENDENT OF $\overline{\text{ME}}$.
NOTE FOR RUN (ROM/RAM) MODE:
INTERNAL MEMORY DATA WILL APPEAR ON THE DATA BUS AFTER CLOCK PULSE 31.

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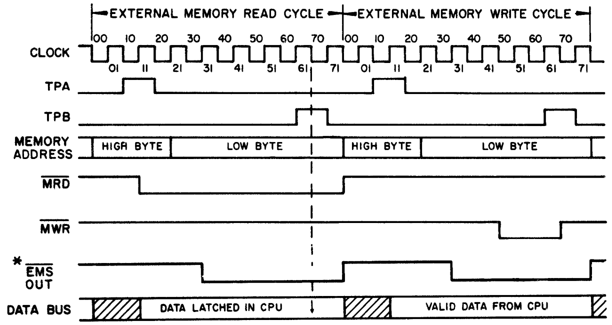
Fig. 3 - Internal memory operation timing waveforms for CDP1804AC.



*FOR RUN (ROM/RAM) MODE ONLY.
NOTE: FOR THE RUN (RAM ONLY) MODE $\overline{\text{ME}}$ MUST BE HIGH DURING EXTERNAL MEMORY ACCESSES.

92CS-34984

Fig. 4 - External memory operation timing waveforms for CDP1804AC.

SIGNAL DESCRIPTIONS

Bus 0 to BUS 7 (Data Bus):

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O) Lines):

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices. The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register. The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the $\overline{\text{MRD}}$ signal:

$\overline{\text{MRD}}$ = V_{DD}: Input data from I/O to CPU and Memory
MRD = V_{SS}: Output data from Memory to I/O

EF1 to EF4 (4 Flags):

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. The flag(s) are sampled at the end of every S0 cycle. EF1 and EF2 are also used for event counting and pulse-width measurement in conjunction with the Counter/Timer.

INTERRUPT, DMA-IN, DMA-OUT (3 I/O Requests)

DMA-IN and DMA-OUT are sampled during TPB every S1, S2, and S3 cycle. INTERRUPT is sampled during TPB every S1 and S2 cycle.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable (MIE) is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and R(0) is incremented.

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority followed by DMA-OUT and then Interrupt. (The Interrupt request is not internally latched and must be held true after DMA).

SC0, SC1, (2 State Code Lines):

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

H = V_{DD}, L = V_{SS}.

TPA, TPB (2 Timing Pulses):

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the multiplexed 16-bit memory address.

MA0 to MA7 (8 Memory Address Lines):

In each cycle, the higher-order byte of a 16-bit memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines 1/2 clock after the termination of TPA.

MWR (Write Pulse):

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

MRD (Read Level):

A low level on MRD indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory and to indicate the direction of data transfer during and I/O instruction.

Q:

Single bit output from the CPU which can be set or reset, under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB. The Q-line can also be controlled by the Counter/Timer underflow via the Enable Toggle Q instruction. The Enable Toggle Q command connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q line changes state. This command is cleared by a LOAD COUNTER (LDC) instruction with the Counter/Timer stopped, a CPU reset, or a BRANCH COUNTER INTERRUPT (BCI) instruction with the counter interrupt flip-flop set.

CLOCK:

Input for externally generated single-phase clock. The maximum clock frequency is 5 MHZ at V_{DD} = 5 V. The clock is counted down internally to 8 clock pulses per machine cycle.

XTAL:

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized.

WAIT, CLEAR (2 Control Lines):

Provide four control modes as listed in the following truth table:

CLEAR	WAIT	MODE
L	L	RUN (ROM/RAM)
L	H	RESET
H	L	PAUSE
H	H	RUN (RAM ONLY)

ME (Memory Enable) RUN (RAM ONLY) Mode

This active low input is used to select or deselect the internal RAM. It must be active prior to clock 70 for an internal RAM access to take place. Internal RAM data will appear on the data bus during the time that ME is active (after clock 31). Thus, if this data is to be latched into an external device (i.e., during an OUTPUT instruction or DMA-OUT cycle), ME should be wide enough to provide enough time for valid data to be latched. The internal RAM is automatically deselected after clock 71. ME is ineffective when MRD • MWR = 1.

In the RUN (RAM ONLY) mode the internal RAM is not internally mask-decoded. Decoding of the starting address is performed externally, and may reside in any 64-byte block of memory.

CDP1804AC

$\overline{\text{EMS}}$ (External Memory Select) RUN (ROM/RAM) Mode

This active low output is used for external memory expansion. It is low when external memory is being addressed and high at all other times. It is initiated 1.5 clock periods after TPA (at which time all addresses are stable) and terminates at the end of the cycle. Use of $\overline{\text{EMS}}$ for memory selection allows 3.5 clock cycles for data access.

Note that in the RUN (ROM/RAM) mode data from the internal ROM or RAM, when selected, will appear on the data bus after clock 31.

V_{DD}, V_{SS}, (Power Levels):

V_{SS} is the most negative supply voltage terminal and is normally connected to ground. V_{DD} is the positive supply voltage terminal. All outputs swing from V_{SS} to V_{DD}. The recommended input voltage swing is from V_{SS} to V_{DD}.

ARCHITECTURE

Fig. 2 shows a block diagram of the CDP1804AC. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following paths:

1. the external memory (multiplexed, higher-order byte first, on to 8 memory address lines)
2. the D register (either of the two bytes can be gated to D)
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register
4. to any other 16-bit scratch-pad register in the array.

The four paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

Most instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and more if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations
2. indicate to the I/O devices a command code or device-selection code for peripherals
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P)
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations
2. output instructions
3. input instructions
4. register to memory transfer
5. memory to register transfer
6. interrupt and subroutine handling.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F, and the RLDI instruction 68CN. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the CDP1804AC architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters. The new RLDI, RLXA, RSXD, and RNX instructions also allow loading, storing, and exchanging the full 16-bit contents of the R registers without affecting the D register. The new DBNZ instruction allows decrementing and branching-on-not-zero of any 16-bit R register also without affecting the D register.

The Q Flip Flop

An internal flip flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. It can also be driven by the underflow output of the Counter/Timer. The output of Q is also available as a microprocessor output.

Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which Register is Program Counter
X	4 Bits	Designates which Register is Data Pointer
N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nibble)
Q	1 Bit	Output Flip-Flop
CNTR	8-Bits	Counter/Timer
CH	8 Bits	Holds Counter Jam Value
MIE	1 Bit	Master Interrupt Enable
CIE	1 Bit	Counter Interrupt Enable
XIE	1 Bit	External Interrupt Enable
CIL	1 Bit	Counter Interrupt Latch

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request occurs and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Master Interrupt Enable is automatically deactivated to inhibit further interrupts. The user's interrupt routine is now in control; the contents of T may be saved by means of a single SAV instruction (78) in the memory location pointed to by R(X) or the contents of T, D, and DF may be saved using a single DSAV instruction (6876). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with either a RET instruction (70) which permits further interrupts, or a DIS instruction (71), which disables further interrupts.

Interrupt Generation and Arbitration (See Fig. 5)

Interrupt requests can be generated from the following sources:

1. Externally through the interrupt input (Request not latched)
2. Internally due to Counter/Timer response (Request is latched)
    a. On the transition from count $(01)_{16}$ to its next value (counter underflow)
    b. On the $\nearrow$ transition of $\overline{EF1}$ in pulse measurement mode 1
    c. On the $\nearrow$ transition of $\overline{EF2}$ in pulse measurement mode 2

For an interrupt to be serviced by the CPU, the appropriate Interrupt Enable flip-flops must be set. Thus, the External Interrupt Enable flip-flop must be set to service an external interrupt request, and the Counter Interrupt Enable flip-flop must be set to service an internal Counter/Timer interrupt request. In addition, the Master Interrupt Enable flip-flop (as used in the CDP1802A) must be set to service either type of request. All 3 flip-flops are initially enabled with the application of a hardware reset, and, can be selectively enabled or disabled with software: CIE, CID instructions for the CIE flip-flop; XIE, XID instructions for the XIE flip-flop; RET, DIS instructions for the MIE flip-flop.

Short branch instructions on Counter Interrupt (BCI) and External Interrupt (BXI) can be placed in the user's interrupt service routine to provide a means of identifying and prioritizing the interrupt source. Note, however, that since the External Interrupt request is not latched, it must remain active until the short branch is executed if this priority arbitration scheme is used.

Interrupt requests can also be polled if automatic interrupt service is not desired (MIE=0). With the Counter Interrupt and External Interrupt short branch instructions, the branch will be taken if an interrupt request is pending, regardless of the state of any of the 3 Interrupt Enable flip-flops. The latched counter interrupt request signal will be reset when the branch is taken, when the CPU is reset, or with a LDC instruction with the Counter stopped. Note that exiting a counter-initiated interrupt routine without resetting the counter interrupt latch will result in immediately re-entering the interrupt routine.

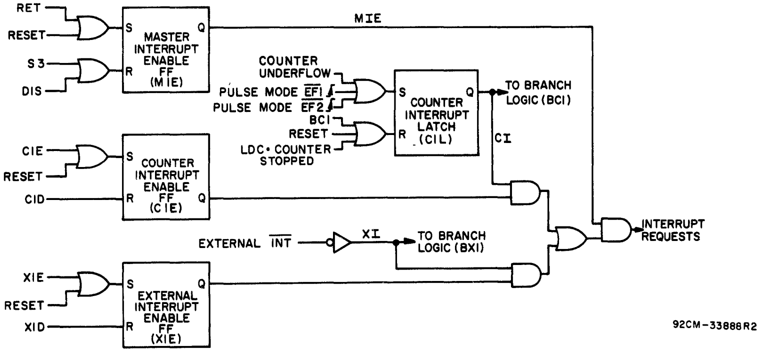


Fig. 5 - Interrupt logic-control diagram for CDP1804AC.

Counter/Timer and Controls (See Fig. 6)

This logic consists of a presettable 8-bit down-counter (Modulo N type), and a conditional divide-by-32 prescaler. After counting down to $(01)_{16}$ the counter returns to its initial value at the next count and sets the Counter Interrupt Latch. It will continue decrementing on subsequent counts. If the counter is preset to $(00)_{16}$ a full 256 counts will occur.

During a Load Counter instruction (LDC) if the counter was stopped with a STPC instruction, the counter and its holding register (CH) are loaded with the value in the D register and any previous counter interrupt is cleared. If the LDC is executed when the counter is running, the contents of the D register are loaded into the holding register (CH) only and any previous counter interrupt is not cleared. (LDC resets the Counter Interrupt Latch only when the counter is stopped). After counting down to $(01)_{16}$ the next count will load the new initial value into the counter, set the Counter Interrupt Latch, and operation will continue.

The Counter/Timer has the following five programmable modes:

1. Event Counter 1: Input to counter is connected to the $\overline{\text{EF1}}$ terminal. The high-to-low transition decrements the counter.
2. Event Counter 2: Input to counter is connected to the $\overline{\text{EF2}}$ terminal. The high-to-low transition decrements the counter.
3. Timer: Input to counter is from the divide-by-32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA. The divide-by-32 prescaler is reset when the counter is in a mode other than the Timer mode, system reset, or stopped by a STPC.
4. Pulse Duration Measurement 1: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{\text{EF1}}$ terminal (gate input) is low. On the transition of $\overline{\text{EF1}}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but counting will continue.
5. Pulse Duration Measurement 2: Operation is identical to Pulse Duration Measurement 1, except $\overline{\text{EF2}}$ is used as the gate input.

The modes can be changed without affecting the stored count.

Those modes which use $\overline{\text{EF1}}$ and $\overline{\text{EF2}}$ terminals as inputs do not exclude testing these flags for branch instructions.

The Stop Counter (STPC) instruction clears the counter mode and stops counting. The STPC instruction should be executed prior to a GEC instruction, if the counter is in the Event Counter Mode 1 or 2.

In addition to the five programmable modes, the Decrement Counter instruction (DTC) enables the user to count in software. In order to avoid conflict with counting done in other modes, the instruction should be used only after the mode has been cleared by a Stop Counter instruction.

The Enable Toggle Q instruction (ETQ) connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q output changes state. This action is independent of the counter mode and the Interrupt Enable flip-flops. The Enable Toggle Q condition is cleared by an LDC with the Counter/Timer stopped; system Reset, or a BCI with CI=1. Note that SEQ and REQ instructions are independent of ETQ.—they can Set or Reset Q while the counter is running.

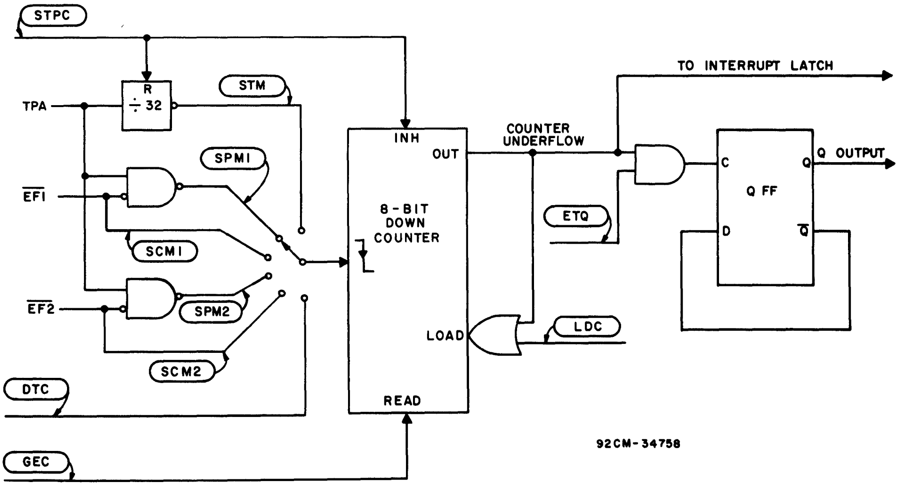


Fig. 6 - Counter/Timer diagram for CDP1804AC.

CDP1804AC

On-Chip Clock (See Figs. 7, 8 and 9)

Clock circuits may use either an external crystal or an RC network.

A typical crystal oscillator circuit is shown in Fig. 7. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{\text{XTAL}}$) in parallel with a resistance. RF (1 megohm typ.). Frequency trimming capacitors, C_{IN} and C_{OUT}, may be required at terminals 1 and 39. For additional information on crystal oscillators, see ICAN-6565.

Because of the Schmitt Trigger input, an RC oscillator can be used as shown in Fig. 8. The frequency is approximately 1/RC (See Fig. 9).

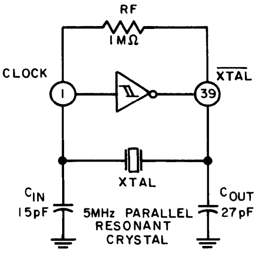


Fig. 7 - Typical 5-MHz crystal oscillator.

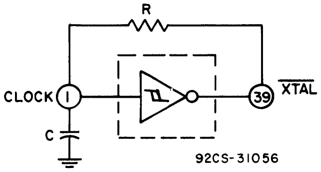


Fig. 8 - RC network for oscillator.

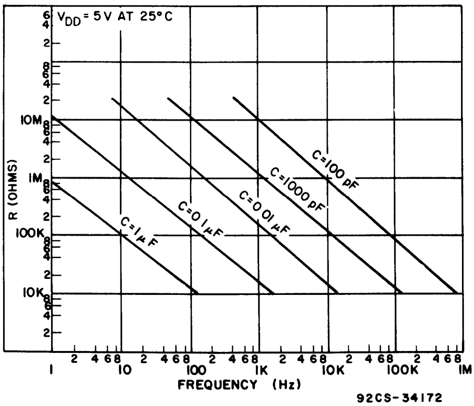


Fig. 9 - Nominal component values as a function of frequency for the RC oscillator.

CONTROL MODES

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	RUN (ROM/RAM)
L	H	RESET
H	L	PAUSE
H	H	RUN (RAM ONLY)

The function of the modes are defined as follows:

RESET

The levels of the CDP1804A external signal lines will asynchronously be forced by RESET to the following states:

Q=0 SC1,SC0=0, 1 BUS 0-7=0
$\overline{\text{EMS}}$/$\overline{\text{ME}}$=INPUT (EXECUTE) MA0-7=RO.1
$\overline{\text{MRD}}$=1 N0, N1, N2=0, 0, 0 TPA=0
TPB=0 $\overline{\text{MWR}}$=1

Internal changes caused by RESET are:
I, N instruction register is cleared to 00. XIE and CIE are set to allow interrupts following initialize. CIL is cleared (any pending counter interrupt is cleared), counter is stopped, the counter mode is cleared, and ETQ is disabled.

Initialization Cycle

The first machine cycle following termination of RESET is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and the following additional changes occur:

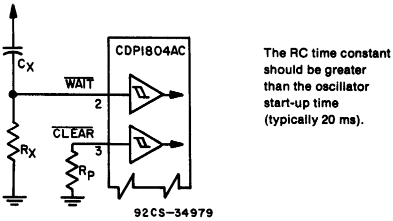
1 → MIE
X, P → T (The old value of X, P will be put into T. This only has meaning following an orderly Reset with power applied).
X, P, RO ← 0 (X, P and RO are cleared).

Interrupt and DMA servicing is suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. The use of a 71 instruction followed by 00 at memory locations 0000 and 0001, may be used to reset MIE so as to preclude interrupts until ready for them.

Reset and Initialize do not affect:
D (Accumulator)
DF
R1, R2, R3, R4, R5, R6, R7, R8, R9, RA, RB, RC, RD, RE, RF
CH (Counter Holding Register)
Counter (the counter is stopped but the value is unaffected)

Power-up Reset/Run Circuits

Power-up Reset/Run (ROM/RAM) and Reset/Run (RAM only) can be realized with the circuits shown in Fig. 10 and 11.



The RC time constant should be greater than the oscillator start-up time (typically 20 ms).

Fig. 10 - Reset/Run (ROM/RAM) diagram.

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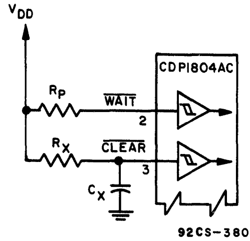


The RC time constant should be greater than the oscillator start-up time (typically 20 ms)

Fig. 11 - Reset/Run (RAM only) diagram.

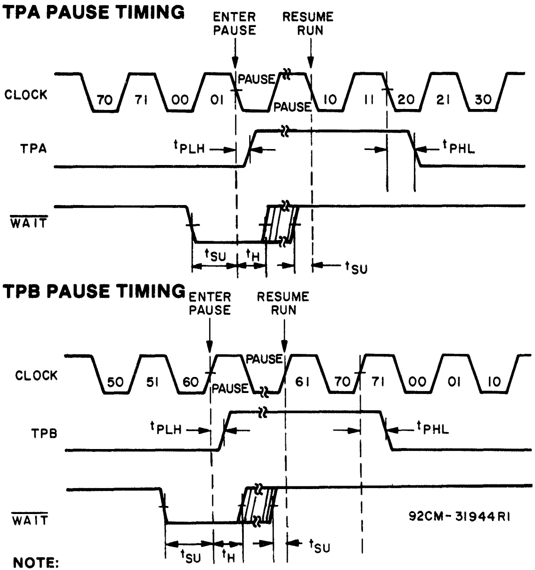
PAUSE

Pause is a low power mode which stops the internal CPU timing generator and freezes the state of the processor. The CPU may be held in the Pause mode indefinitely. Hardware pause can occur at two points in a machine cycle, on the low to high transition of either TPA or TPB. A TPB pause can also be initiated by software with the execution of an IDLE instruction. In the pause mode, the oscillator continues to run but subsequent clock transitions are ignored. TPA and TPB remain at their previous state (see Fig. 12).

Pause is entered from RUN (RAM only) by dropping $\overline{\text{WAIT}}$ low, and from RUN (ROM/RAM) by raising $\overline{\text{CLEAR}}$ high. Appropriate setup and hold times must be met.

If Pause is entered while in the event counter mode, the appropriate Flag transition will continue to decrement the counter.

Hardware-initiated pause is exited to RUN (RAM only) by raising the $\overline{\text{Wait}}$ line, and the RUN (ROM/RAM) by lowering $\overline{\text{CLEAR}}$. Pause entered with an IDLE instruction requires $\overline{\text{DMA}}$, $\overline{\text{INTERRUPT}}$ or RESET to resume execution.



NOTE:
PAUSE (IN CLOCK WAVEFORM) WHILE REPRESENTED HERE AS ONE CLOCK CYCLE IN DURATION, COULD BE INFINITELY LONG.

Fig. 12 - Pause mode timing waveforms.

RUN

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the next high-to-low clock transition, while if paused at TPB, it will resume on the next low-to-high clock transition. (See Fig. 12). When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

SCHMITT TRIGGER INPUTS

All inputs except BUS 0 — BUS 7 and $\overline{\text{ME}}$ contain a Schmitt Trigger circuit, which is especially useful on the $\overline{\text{CLEAR}}$ input as a power-up RESET (See Fig. 10 and 11) and the CLOCK input (See Fig. 7 and 8).

STATE TRANSITIONS

The CDP1804AC state transitions are shown in Fig. 13. Each machine cycle requires the same period of time, 8 clock pulses, except the initialization cycle (INT) which requires 9 clock pulses. Reset is asynchronous and can be forced at any time.

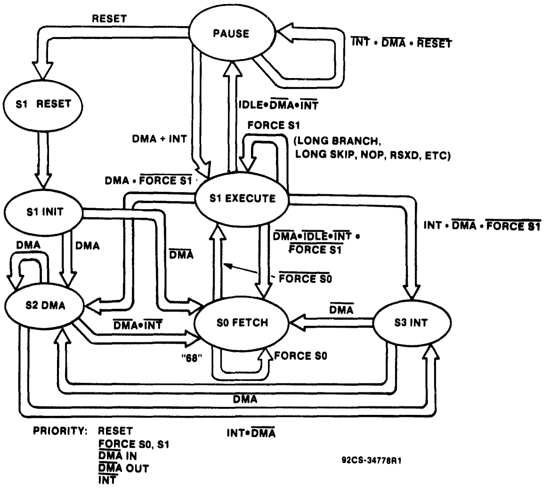

RESET
PAUSE
$\overline{\text{INT}}$ • $\overline{\text{DMA}}$ • $\overline{\text{RESET}}$
S1 RESET
IDLE•$\overline{\text{DMA}}$•$\overline{\text{INT}}$
FORCE S1
(LONG BRANCH, LONG SKIP, NOP, RSXD, ETC)
DMA + INT
DMA • $\overline{\text{FORCE S1}}$
S1 EXECUTE
S1 INIT
INT • $\overline{\text{DMA}}$ • $\overline{\text{FORCE S1}}$
$\overline{\text{DMA}}$•$\overline{\text{IDLE}}$•$\overline{\text{INT}}$ • $\overline{\text{FORCE S1}}$
DMA
DMA
$\overline{\text{DMA}}$
$\overline{\text{FORCE S0}}$
S2 DMA
$\overline{\text{DMA}}$•$\overline{\text{INT}}$
S0 FETCH
$\overline{\text{DMA}}$
S3 INT
"68"
FORCE S0
DMA
PRIORITY: RESET
FORCE S0, S1
DMA IN
DMA OUT
INT
INT•$\overline{\text{DMA}}$
92CS-34778R1

Fig. 13 - State transition diagram.

INSTRUCTION SET

The CDP1804AC instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where
W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)

Operation Notation
M (R(N))→D; R(N) + 1→R(N)

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I — INSTRUCTION SUMMARY

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE				
LOAD IMMEDIATE	2	LDI	F8	M(R(P))→D; R(P)+1→R(P)
REGISTER LOAD IMMEDIATE	5	RLDI	68CN■	M(R(P))→R(N).1; M(R(P))+1→ R(N).0; R(P)+2→R(P)
LOAD VIA N	2	LDN	0N	M(R(N))→D; FOR N NOT 0
LOAD ADVANCE	2	LDA	4N	M(R(N))→D; R(N)+1→R(N)
LOAD VIA X	2	LDX	F0	M(R(X))→D
LOAD VIA X AND ADVANCE	2	LDXA	72	M(R(X))→D; R(X)+1→R(X)
REGISTER LOAD VIA X AND ADVANCE	5	RLXA	686N■	M(R(X))→R(N).1; M(R(X)+1)→ R(N).0; R(X))+2→R(X)
STORE VIA N	2	STR	5N	D→M(RN))
STORE VIA X AND DECREMENT	2	STXD	73	D→M(R(X)); R(X)-1→R(X)
REGISTER STORE VIA X AND DECREMENT	5	RSXD	68AN■	R(N).0→M(R(X)); R(N).1→ M(R(X)-1); R(X)-2→R(X)
REGISTER OPERATIONS				
INCREMENT REG N	2	INC	1N	R(N)+1→R(N)
DECREMENT REG N	2	DEC	2N	R(N)-1→R(N)
DECREMENT REG N AND LONG BRANCH IF NOT EQUAL 0	5	DBNZ	682N	R(N)-1→R(N); IF R(N) NOT 0, M(R(P))→R(P).1, M(R(P)+1)→ R(P).0, ELSE R(P)+2→R(P)
INCREMENT REG X	2	IRX	60	R(X)+1→R(X)
GET LOW REG N	2	GLO	8N	R(N).0→D
PUT LOW REG N	2	PLO	AN	D→R(N).0
GET HIGH REG N	2	GHI	9N	R(N).1→D
PUT HIGH REG N	2	PHI	BN	D→R(N).1
REGISTER N TO REGISTER X COPY	4	RNX	68BN■	R(N)→R(X)
LOGIC OPERATIONS (Note 5)				
OR	2	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	2	ORI	F9	M(R(P)) OR D→D; R(P)+1→R(P)
EXCLUSIVE OR	2	XOR	F3	M(R(X)) XOR D→D
EXCLUSIVE OR IMMEDIATE	2	XRI	FB	M(R(P)) XOR D→D; R(P)+1→R(P)
AND	2	AND	F2	M(R(X)) AND D→D
AND IMMEDIATE	2	ANI	FA	M(R(P)) AND D→D; R(P)+1→R(P)
SHIFT RIGHT	2	SHR	F6	SHIFT D RIGHT, LSB(D)→DF, 0→MSB(D)
SHIFT RIGHT WITH CARRY	2	SHRC	76▲	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
RING SHIFT RIGHT	2	RSHR		
SHIFT LEFT	2	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)

■Previous contents of T register are destroyed during instruction execution.

▲This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

Table I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
LOGIC OPERATIONS (Note 5) (Cont'd)				
SHIFT LEFT WITH CARRY	2	SHLC	7E▲	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	2	RSHL		
ARITHMETIC OPERATIONS (Note 5)				
ADD	2	ADD	F4	M(R(X))+D→DF, D
DECIMAL ADD	4	DADD	68F4	M(R(X))+D→DF, D DECIMAL ADJUST→DF, D
ADD IMMEDIATE	2	ADI	FC	M(R(P))+D→DF, D; R(P)+1→R(P)
DECIMAL ADD IMMEDIATE	4	DADI	68FC	M(R(P))+D→DF,D R(P)+1→R(P) DECIMAL ADJUST→DF, D
ADD WITH CARRY	2	ADC	74	M(R(X))+D+DF→DF, D
DECIMAL ADD WITH CARRY	4	DADC	6874	M(R(X))+D+DF→DF, D DECIMAL ADJUST→DF, D
ADD WITH CARRY, IMMEDIATE	2	ADCI	7C	M(R(P))+D+DF→DF, D R(P)+1→R(P)
DECIMAL ADD WITH CARRY, IMMEDIATE	4	DACI	687C	M(R(P))+D+DF→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
SUBTRACT D	2	SD	F5	M(R(X))-D→DF, D

SUBTRACT D IMMEDIATE	2	SDI	FD	M(R(P))-D→DF, D;
				R(P)+1→R(P)

SUBTRACT D WITH BORROW	2	SDB	75	M(R(X))-D-(NOT DF)→DF, D

SUBTRACT D WITH BORROW, IMMEDIATE	2	SDBI	7D	M(R(P))-D-(NOT DF)→DF, D;
				R(P)+1→R(P)

SUBTRACT MEMORY	2	SM	F7	D-M(R(X))→DF, D
DECIMAL SUBTRACT MEMORY	4	DSM	68F7	D-M(R(X))→DF, D DECIMAL ADJUST→DF, D

SUBTRACT MEMORY IMMEDIATE	2	SMI	FF	D-M(R(P))→DF, D;
				R(P)+1→R(P)

DECIMAL SUBTRACT MEMORY, IMMEDIATE	4	DSMI	68FF	D-M(R(P))→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
SUBTRACT MEMORY WITH BORROW	2	SMB	77	D-M(R(X))-(NOT DF)→DF, D
DECIMAL SUBTRACT MEMORY WITH BORROW	4	DSMB	6877	D-M(R(X))-(NOT DF)→DF, D DECIMAL ADJUST→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	2	SMBI	7F	D-M(R(P))-(NOT DF)→DF, D R(P)+1→R(P)
DECIMAL SUBTRACT MEMORY WITH BORROW, IMMEDIATE	4	DSBI	687F	D-M(R(P))-(NOT DF)→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
BRANCH INSTRUCTIONS — SHORT BRANCH				
SHORT BRANCH	2	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	2	NBR	38▲	R(P)+1→R(P)

SHORT BRANCH IF D = 0	2	BZ	32	IF D = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF D NOT 0	2	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

▲This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

Table I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS — SHORT BRANCH (Cont'd)				

SHORT BRANCH IF DF = 1	2	BDF	33▲	IF DF = 1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF POS OR ZERO	2	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	2	BGE		

SHORT BRANCH IF DF = 0	2	BNF	3B▲	IF D = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF MINUS	2	BM		
SHORT BRANCH IF LESS	2	BL		

SHORT BRANCH IF Q = 1	2	BQ	31	IF Q = 1. M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF Q = 0	2	BNQ	39	IF Q = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF1 = 1
($\overline{EF1} = V_{SS}$)
	2	B1	34	IF EF1 = 1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF1 = 0
($\overline{EF1} = V_{DD}$)
	2	BN1	3C	IF EF1 = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF2 = 1
($\overline{EF2} = V_{SS}$)
	2	B2	35	IF EF2 = 1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF2 = 0
($\overline{EF2} = V_{DD}$)
	2	BN2	3D	IF EF2 = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF3 = 1
($\overline{EF3} = V_{SS}$)
	2	B3	36	IF EF3 = 1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF3 = 0
($\overline{EF3} = V_{DD}$)
	2	BN3	3E	IF EF3 = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF4 = 1
($\overline{EF4} = V_{SS}$)
	2	B4	37	IF EF4 =1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF4 = 0
($\overline{EF4} = V_{DD}$)
	2	BN4	3F	IF EF4 = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH ON COUNTER INTERRUPT	3	BCI	683E•	IF CI=1, M(R(P))→R(P).0; 0→CI
				ELSE R(P)+1→R(P)

SHORT BRANCH ON EXTERNAL INTERRUPT	3	BXI	683F	IF XI=1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

BRANCH INSTRUCTIONS — LONG BRANCH				
LONG BRANCH	3	LBR	C0	M(R(P))→R(P).1, M(R(P)+1)→R(P).0
NO LONG BRANCH (SEE LSKP)	3	NLBR	C8▲	R(P)+2→R(P)

LONG BRANCH IF D = 0	3	LBZ	C2	IF D = 0, M(R(P))→R(P).1
				M(R(P)+1)→R(P).0
				ELSE R(P)+2→R(P)

LONG BRANCH IF D NOT 0	3	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1
				M(R(P)+1)→R(P).0
				ELSE R(P)+2→R(P)

LONG BRANCH IF DF = 1	3	LBDF	C3	IF DF = 1, M(R(P))→R(P).1
				M(R(P)+1)→R(P).0
				ELSE R(P)+2→R(P)

LONG BRANCH IF DF = 0	3	LBNF	CB	IF DF = 0, M(R(P))→R(P).1
				M(R(P)+1)→R(P).0
				ELSE R(P)+2→R(P)

LONG BRANCH IF Q = 1	3	LBQ	C1	IF Q = 1, M(R(P))→R(P).1
				M(R(P)+1)→R(P).0
				ELSE R(P)+2→R(P)

LONG BRANCH IF Q = 0	3	LBNQ	C9	IF Q = 0, M(R(P))→R(P).1
				M(R(P)+1)→R(P).0
				ELSE R(P)+2→R(P)

▲This instruction is associated with more than one mnemonic Each mnemonic is individually listed.

•IETQ cleared by LDC with the Counter/Timer stopped, reset of CPU, or BCI • (CI=1).
CI = Counter Interrupt, XI = External Interrupt.

CDP1804AC

Table I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
SKIP INSTRUCTIONS				
SHORT SKIP (SEE NBR)	2	SKP	38▲	R(P)+1→R(P)
LONG SKIP (SEE NLBR)	3	LSKP	C8▲	R(P)+→R(P)

LONG SKIP IF D = 0	3	LSZ	CE	IF D = 0, R(P)+2→R(P)
				ELSE CONTINUE

LONG SKIP IF D NOT 0	3	LSNZ	C6	IF D NOT 0, R(P)+2→R(P)
				ELSE CONTINUE

LONG SKIP IF DF = 1	3	LSDF	CF	IF DF = 1, R(P)+2→R(P)
				ELSE CONTINUE

LONG SKIP IF DF = 0	3	LSNF	C7	IF DF = 0, R(P)+2→R(P)
				ELSE CONTINUE

LONG SKIP IF Q = 1	3	LSQ	CD	IF Q = 1, R(P)+2→R(P)
				ELSE CONTINUE

LONG SKIP IF Q = 0	3	LSNQ	C5	IF Q = 0, R(P)+2→R(P)
				ELSE CONTINUE

LONG SKIP IF MIE = 1	3	LSIE	CC	IF MIE = 1, R(P)+2→R(P)
				ELSE CONTINUE

CONTROL INSTRUCTIONS				
IDLE	2	IDL	00#	STOP ON TPB; WAIT FOR DMA OR INTERRUPT; BUS FLOATS
NO OPERATION	3	NOP	C4	CONTINUE
SET P	2	SEP	DN	N→P
SET X	2	SEX	EN	N→X
SET Q	2	SEQ	7B	1→Q
RESET Q	2	REQ	7A	0→Q
PUSH X, P TO STACK	2	MARK	79	(X, P)→T; (X, P)→M(R(2)) THEN P→X; R(2)→1→R(2)
TIMER/COUNTER INSTRUCTIONS				
LOAD COUNTER	3	LDC	6806•	CNTR STOPPED: D→CH, CNTR; 0=CI.CNTR RUNNING; D→CH
GET COUNTER	3	GEC	6808	CNTR→D
STOP COUNTER	3	STPC	6800	STOP CNTR CLOCK; 0→÷32 PRESCALER
DECREMENT TIMER/COUNTER	3	DTC	6801	CNTR-1→CNTR
SET TIMER MODE AND START	3	STM	6807	TPA÷32→ CNTR
SET COUNTER MODE 1 AND START	3	SCM1	6805	$\overline{EF1}$→ CNTR CLOCK
SET COUNTER MODE 2 AND START	3	SCM2	6803	EF2→ CNTR CLOCK
SET PULSE WIDTH MODE 1 AND START	3	SPM1	6804	TPA.$\overline{EF1}$→ CNTR CLOCK; $\overline{EF1}$ ↗ STOPS COUNT
SET PULSE WIDTH MODE 2 AND START	3	SPM2	6802	TPA.EF2→ CNTR CLOCK; $\overline{EF2}$ ↗ STOPS COUNT
ENABLE TOGGLE Q	3	ETQ	6809•	IF CNTR = 01 • NEXT CNTR CLOCK ↗ : $\overline{Q}$→Q

▲This instruction is associated with more than one mnemonic Each mnemonic is individually listed

#An IDLE instruction initiates an S1 cycle All external signals, except the oscillator, are stopped on the low-to-high transition of TPB. All outputs remain in their previous states, $\overline{MRD}$, $\overline{MWR}$, $\overline{EMS}$ are set to a logic '1' and the data bus floats. The processor will continue to IDLE until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and the normal operation is resumed. (To respond to an INTERRUPT during an IDLE, MIE and either CIE or XIE must be enabled).

• ETQ cleared by LDC with the Counter/Timer stopped, reset of CPU or BCI · (CI = 1)

CI = Counter Interrupt, XI = External Interrupt.

Table I — INSTRUCTION SUMMARY (Cont'd)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
INTERRUPT CONTROL				
EXTERNAL INTERRUPT ENABLE	3	XIE	680A	1→XIE
EXTERNAL INTERRUPT DISABLE	3	XID	680B	0→XIE
COUNTER INTERRUPT ENABLE	3	CIE	680C	1→CIE
COUNTER INTERRUPT DISABLE	3	CID	680D	0→CIE
RETURN	2	RET	70	M(R(X))→X, P; R(X)+1→R(X); 1→MIE
DISABLE	2	DIS	71	M(R(X)→X, P; R(X)+1→R(X); 0→MIE
SAVE	2	SAV	78	T→M(R(X))
SAVE T, D, DF	6	DSAV	6876■	R(X)-1→R(X), T→M(R(X)), R(X)-1→R(X), D→M (R(X)), R(X)-1→R(X), SHIFT D RIGHT WITH CARRY, D→M(R(X))
INPUT-OUTPUT BYTE TRANSFER				
OUTPUT 1	2	OUT 1	61	M(R(X))→BUS; R(X)+1→R(X); N LINES = 1
OUTPUT 2	2	OUT 2	62	M(R(X))→BUS; R(X)+1→R(X); N LINES = 2
OUTPUT 3	2	OUT 3	63	M(R(X))→BUS; R(X)+1→R(X); N LINES = 3
OUTPUT 4	2	OUT 4	64	M(R(X))→BUS; R(X)+1→R(X); N LINES = 4
OUTPUT 5	2	OUT 5	65	M(R(X))→BUS; R(X)+1→R(X); N LINES = 5
OUTPUT 6	2	OUT 6	66	M(R(X))→BUS; R(X)+1→R(X); N LINES = 6
OUTPUT 7	2	OUT 7	67	M(R(X))→BUS; R(X)+1→R(X); N LINES = 7
INPUT 1	2	INP 1	69	BUS→M(R(X)); BUS→D; N LINES = 1
INPUT 2	2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES = 2
INPUT 3	2	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES = 3
INPUT 4	2	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES = 4
INPUT 5	2	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES = 5
INPUT 6	2	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES = 6
INPUT 7	2	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES = 7
CALL AND RETURN				

STANDARD CALL	10	SCAL	688N■	R(N).0→M(R(X));
				R(N).1→M(R(X)-1);
				R(X)-2→R(X); R(P)→R(N);
				THEN M(R(N))→R(P).1;
				M(R(N)+1)→R(P).0;
				R(N)+2→R(N)

STANDARD RETURN	8	SRET	689N■	R(N)→R(P); M(R(X)+1)→R(N).1;
				M(R(X)+2)→R(N).0;
				R(X)+2→R(X)

■Previous contents of T register are destroyed during instruction execution

NOTES FOR TABLE I

1. Long-Branch, Long-Skip and No Op instructions require three cycles to complete (1 fetch + 2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:
   a. Branch unconditionally
   b. Test for D=0 or D≠0
   c. Test for DF=0 or DF=1
   d. Test for Q=0 or Q=1
   e. Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

2. The short-branch instructions are two or three bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address, except for the branches on interrupt. For those, the first two bytes specify the condition to be tested and the third byte specifies the branching address.

   The short branch instruction can:
   a. Branch unconditionally
   b. Test for D=0 or D≠0
   c. Test for DF=0 or DF=1
   d. Test for Q=0 or Q=1
   e. Test the status (1 or 0) of the four EF flags
   f Effect an unconditional no branch
   g. Test for counter or external interrupts (BCI, BXI)

   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

   The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

   They can:
   a. Skip unconditionally
   b. Test for D=0 or D≠0
   c. Test for DF=0 or DF=1
   d. Test for Q=0 or Q=1
   e. Test for MIE=1

   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

4. Instruction 6800 through 68FF take a minimum of 3 machine cycles and up to a maximum of 10 machine cycles. In all cases, the first two cycles are fetches and subsequent cycles are executes. The first byte (68) of these two-byte op codes is used to generate the second fetch, the second byte is then interpreted differently than the same code without the 68 prefix. DMA and INT requests are not serviced until the end of the last execute cycle.

5. Arithmetic Operations:
   The arithmetic and shift operations are the only instructions that can alter the content of DF. The syntax '(NOT DF)' denotes the subtraction of the borrow.
   Binary Operations:
   After an ADD instruction —
   DF=1 denotes a carry has occurred. Result is greater than FF_{16}.
   DF=0 denotes a carry has not occurred.
   After a SUBTRACT instruction —
   DF=1 denotes no borrow. D is a true positive number.
   DF=0 denotes a borrow. D is in two's complement form.

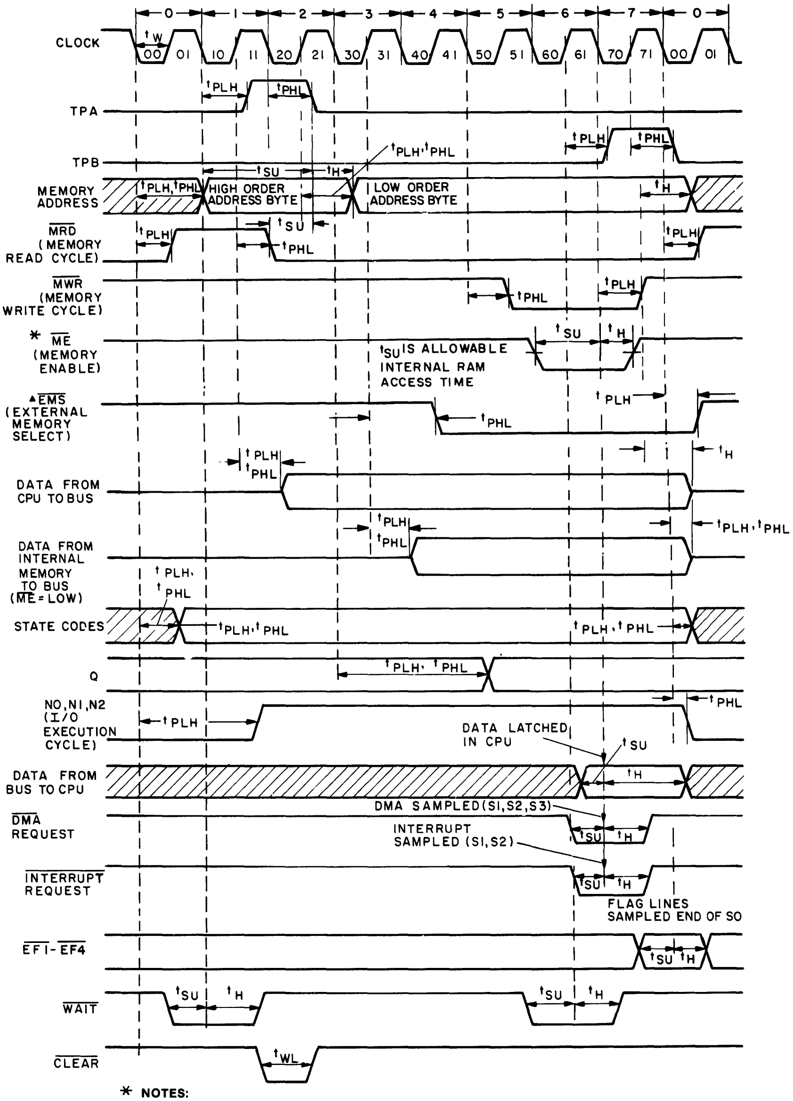
   Binary Coded Decimal Operations:
   After a BCD ADD instruction —
   DF=1 denotes a carry has occurred. Result is greater than 99_{10}.
   DF=0 denotes a carry has not occurred.
   After a BCD SUBTRACT instruction —
   DF=1 denotes no borrow. D is a true positive decimal number.

$$\begin{array}{llll} \text{(Example)} & 99 & D & \\ & -88 & M(R(X)) & \\ \cline{2-2} & 11 & D & DF=1 \end{array}$$

   DF=0 denotes a borrow. D is in ten's complement form.

$$\begin{array}{llll} \text{(Example)} & 88 & D & \\ & -99 & M(R(X)) & \\ \cline{2-2} & 89 & D & DF=0 \end{array}$$

   89 is the ten's complement of 11, which is the correct answer (with a minus value denoted by DF=0).



✱ NOTES:
1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE.
2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS.
3. SHADED ARE AS INDICATED "DON'T CARE" OR UNDEFINED STATE. MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD.

*FOR THE RUN (RAM ONLY) MODE ONLY.

▲ FOR THE RUN (RAM/ROM) MODE ONLY

92CL-34986R1

Fig. 14 - Dynamic timing waveforms for CDP1804AC.

CDP1804AC

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C; C_L = 50 pF; Input t_r, t_f = 10ns; Input Pulse Levels = 0.1 V to V_{DD} -0.1 V; V_{DD} = 5 V, ±5%.

CHARACTERISTIC		LIMITS		UNITS
		CDP1804AC		
		Typ.•	Max.	
Propagation Delay Times:				
Clock to TPA, TPB	t_{PLH}, t_{PHL}	150	275	ns
Clock-to-Memory High-Address Byte	t_{PLH}, t_{PHL}	325	550	
Clock-to-Memory Low-Address Byte	t_{PLH}, t_{PHL}	275	450	
Clock to $\overline{\text{MRD}}$	t_{PLH}, t_{PHL}	200	325	
Clock to $\overline{\text{MWR}}$	t_{PLH}, t_{PHL}	150	275	
Clock to (CPU DATA to BUS)	t_{PLH}, t_{PHL}	375	625	
Clock to State Code	t_{PLH}, t_{PHL}	225	400	
Clock to Q	t_{PLH}, t_{PHL}	250	425	
Clock to N	t_{PLH}, t_{PHL}	250	425	
Clock to Internal RAM Data to BUS	t_{PLH}, t_{PHL}	420	650	
Clock to $\overline{\text{EMS}}$	t_{PLH}, t_{PHL}	275	450	
Minimum Set Up and Hold Times:■				
Data Bus Input Set-Up	t_{SU}	-100	0	ns
Data Bus Input Hold	t_H	125	225	
$\overline{\text{DMA}}$ Set-Up	t_{SU}	-75	0	
$\overline{\text{DMA}}$ Hold	t_H	100	175	
$\overline{\text{ME}}$ Set-Up	t_{SU}	125	320	
$\overline{\text{ME}}$ Hold	t_H	0	50	
Interrupt Set-Up	t_{SU}	-100	0	
Interrupt Hold	t_H	100	175	
$\overline{\text{WAIT}}$ Set-Up	t_{SU}	20	50	
$\overline{\text{EF1-4}}$ Set-Up	t_{SU}	-125	0	
$\overline{\text{EF1-4}}$ Hold	t_H	175	300	
Minimum Pulse Width Times:■				
$\overline{\text{CLEAR}}$ Pulse Width	t_{WL}	100	175	ns
$\overline{\text{CLOCK}}$ Pulse Width	t_{WL}	75	100	

•Typical values are for T_A = 25° C and nominal V_{DD}.

■Maximum limits of minimum characteristics are the values above which all devices function.

TIMING SPECIFICATIONS as a function of T (T = 1/f_{CLOCK}) at T_A = -40 to +85° C, V_{DD} = 5 V, ±5%.

CHARACTERISTIC		LIMITS		UNITS
		CDP1804AC		
		Min.	Typ.•	
High-Order Memory-Address Byte Set-Up to TPA ↘ Time	t_{SU}	2T-275	2T-175	ns
$\overline{\text{MRD}}$ to TPA ↘ Time	t_{SU}	T/2-100	T/2-75	
High-Order Memory-Address Byte Hold After TPA Time	t_H	T/2+75	T/2+100	
Low-Order Memory-Address Byte Hold After WR Time	t_H	T+180	T+240	
CPU Data to Bus Hold After WR Time	t_H	T+110	T+150	
Required Memory Access Time Address to Data	t_{ACC}	4.5T-440	4.5T-330	

•Typical values are for T_A = 25° C and nominal V_{DD}.

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES
S1	RESET			0→Q,I,N, COUNTER PRESCALER, CIL; 1→CIE, XIE	00	UNDEFINED	1	1	0
	INITIALIZE NOT PROGRAMMER ACCESSIBLE			X, P→T THEN 0→X, P; 1→MIE, 0000→R0	00▲	UNDEFINED	1	1	0
S0		FETCH		MRP→I, N; RP+1→RP	MRP	RP	0	1	0
S1	0	0	IDL	STOP AT TPB WAIT FOR DMA OR INT	HIGH Z	RO	1	1	0
	0	1-F	LDN	MRN→D	MRN	RN	0	1	0
	1	0-F	INC	RN+1→RN	HIGH Z	RN	1	1	0
	2	0-F	DEC	RN-1→RN	HIGH Z	RN	1	1	0
	3	0-F	SHORT BRANCH	TAKEN: MRP→RP.0 NOT TAKEN: RP+1→RP	MRP	RP	0	1	0
	4	0-F	LDA	MRN→D; RN+1→RN	MRN	RN	0	1	0
	5	0-F	STR	D→MRN	D	RN	1	0	0
	6	0	IRX	RX+1→RX	MRX	RX	1	1	0
	6	1	OUT 1	MRX→BUS; RX+1→RX	MRX	RX	0	1	1
		2	OUT 2						2
		3	OUT 3						3
		4	OUT 4						4
		5	OUT 5						5
		6	OUT 6						6
		7	OUT 7						7
		9	INP 1	BUS→MRX, D	DATA FROM I/O DEVICE	RX	1	0	1
		A	INP 2						2
		B	INP 3						3
		C	INP 4						4
		D	INP 5						5
		E	INP 6						6
		F	INP 7						7
	7	0	RET	MRX→X,P; RX+1→RX 1→MIE	MRX	RX	0	1	0
		1	DIS	MRX→X,P; RX+1→RX 0→MIE	MRX	RX	0	1	0
		2	LDXA	MRX→D; RX+1→RX	MRX	RX	0	1	0
		3	STXD	D→MRX; RX-1→RX	D	RX	1	0	0
		4	ADC	MRX+D+DF→DF, D	MRX	RX	0	1	0
		5	SDB	MRX- D-DFN→DF, D	MRX	RX	0	1	0
		6	SHRC	LSB(D)→DF; DF→MSB(D)	HIGH Z	RX	1	1	0
		7	SMB	D- MRX- DFN→DF, D	MRX	RX	0	1	0
		8	SAV	T→MRX	T	RX	1	0	0
		9	MARK	X,P→T, MR2; P→X R2-1→R2	T	R2	1	0	0
		A	REQ	0→Q	HIGH Z	RP	1	1	0
		B	SEQ	1→Q	HIGH Z	RP	1	1	0
		C	ADCI	MRP+D+DF→DF, D; RP+1	MRP	RP	0	1	0
		D	SDBI	MRP-D-DFN→DF, D; RP+1	MRP	RP	0	1	0
		E	SHLC	MSB(D)→DF; DF→LSB(D)	HIGH Z	RP	1	1	0
		F	SMBI	D-MRP-DFN→DF, D; RP+1	MRP	RP	0	1	0
	8	0-F	GLO	RN.0→D	RN.0	RN	1	1	0
	9	0-F	GHI	RN.1→D	RN.1	RN	1	1	0
	A	0-F	PLO	D→RN.0	D	RN	1	1	0
	B	0-F	PHI	D→RN.1	D	RN	1	1	0

▲ = Data bus floats for first 2-1/2 clocks of the 9 clock initialization cycle; all zeros for remainder of cycle.

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TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES
S1#1	C	0-3, 8-B	LONG BRANCH	TAKEN: MRP→B; RP+1→RP	MRP	RP	0	1	0
#2				TAKEN:B→RP.1;MRP→RP.0	M(RP+1)	RP+1	0	1	0
S1#1				NOT TAKEN RP+1→RP	MRP	RP	0	1	0
#2				NOT TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0
S1#1		5 6 7 C D E F	LONG SKIP	TAKEN: RP+1→RP	MRP	RP	0	1	0
#2				TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0
S1#1				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0
#2				NOT TAKEN: NO OPERATION	M(RP+1)	RP+1	0	1	0
S1#1		4	NOP	NO OPERATION	MRP	RP	0	1	0
#2				NO OPERATION	M(RP+1)	RP+1	0	1	0
S1	D	0-F	SEP	N→P	NN	RN	1	1	0
	E	0-F	SEX	N→X	NN	RN	1	1	0
	F	0	LDX	MRX→D	MRX	RX	0	1	0
		1 2 3 4 5 7	OR AND XOR ADD SD SM	MRX OR D→D MRX AND D→D MRX XOR D→D MRX+D→DF, D MRX-D→DF, D D-MRX→DF; D	MRX	RX	0	1	0
		6	SHR	LSB(D)→DF; 0→MSB(D)	HIGH Z	RX	1	1	0
		8 9 A B C D F	LDI ORI ANI XRI ADI SDI SMI	MRP→D; RP+1→RP MRP OR D→D; RP+1→RP MRP AND D→D; RP+1→RP MRP XOR D→D; RP+1→RP MRP+D→DF, D; RP+1→RP MRP-D→DF, D; RP+1→RP D-MRP→DF, D; RP+1→RP	MRP	RP	0	1	0
		E	SHL	MSB(D)→DF; 0→LSB(D)	HIGH Z	RP	1	1	0
S2	DMA IN			BUS→MR0; R0+1→R0	DATA FROM I/O DEVICE	R0	1	0	0
	DMA OUT			MR0→BUS; R0+1→R0	MR0	R0	0	1	0
S3	INTERRUPT			X,P→T; 0→MIE 1→P; 2→X	HIGH Z	RN	1	1	0

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TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	N LINES
THE FOLLOWING ARE ALL LINKED INSTRUCTIONS "68" PRECEDES ALL THE OP CODES, SO THERE IS A DOUBLE FETCH									
S1	0	0	STPC	STOP COUNTER CLOCK; 0→÷32 PRESCALER	HIGH Z	R0	1	1	0
		1	DTC	CNTR→1→CNTR	HIGH Z	R1	1	1	0
		2	SPM2	CNTR-1 ON EF2 AND TPA	HIGH Z	R2	1	1	0
		3	SCM2	CNTR-1 ON EF2 0 TO 1	HIGH Z	R3	1	1	0
		4	SPM1	CNTR-1 ON EF1 AND TPA	HIGH Z	R4	1	1	0
		5	SCM1	CNTR-1 ON EF1 0 TO 1	HIGH Z	R5	1	1	0
		6	LDC	CNTR STOPPED: D→CH, CNTR, 0→CI CNTR RUNNING· D→CH	D	R6	1	1	0
		7	STM	CNTR-1 ON TPA÷32	HIGH Z	R7	1	1	0
		8	GEC	CNTR→D	CNTR	R8	1	1	0
		9	ETQ	IF CNTR THRU 0: $\overline{\text{Q}}$→Q	HIGH Z	R9	1	1	0
		A	XIE	1→XIE	HIGH Z	RA	1	1	0
		B	XID	0→XIE	HIGH Z	RB	1	1	0
		C	CIE	1→CIE	HIGH Z	RC	1	1	0
		D	CID	0→CIE	HIGH Z	RD	1	1	0
S1#1	2	0-F	DBNZ	RN-1→RN	HIGH Z	RN	1	1	0
#2				MRP→B; RP+1→RP	MRP	RP	0	1	0
#3				TAKEN: B→RP.1, MRP→RP.0 NOT TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0
S1	3	E	BCI	TAKEN: MRP→RP.0; 0→CI NOT TAKEN: RP+1→RP	MRP	RP	0	1	0
		F	BXI	TAKEN: MRP→RP.0 NOT TAKEN: RP+1→RP	MRP	RP	0	1	0
S1#1	6	0-F	RLXA	MRX→B, RX+1→RX	MRX	RX	0	1	0
#2				B→T; MRX→B; RX+1→RX	M(RX+1)	RX+1	0	1	0
#3				B, T→RN.0, RN.1	HIGH Z	RN	1	1	0
S1#1	7	4	DADC	MRX+D+DF→DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP	1	1	1
S1#1	7	6	DSAV	RX-1→RX	HIGH Z	RX	1	1	0
#2				T→MRX; RX-1→RX	T	RX-1	1	0	0
#3				D→MRX; RX-1→RX SHIFT D RIGHT WITH CARRY	D	RX-2	1	0	0
#4				D→MRX	D	RX-3	1	0	0
S1#1	7	7	DSMB	D-MRX-(NOT DF)→DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP	1	1	0
S1#1	7	C	DACI	MRP+D+DF→DF, D; RP+1→RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP+1	1	1	0
S1#1	7	F	DSBI	D-MRP-(NOT DF)→DF, D; RP+1→RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP+1	1	1	0
S1#1	8	0-F	SCAL	RN.0, RN.1→T, B	HIGH Z	RN	1	1	0
#2				T→MRX; RX-1→RX	RN.0	RX	1	0	0
#3				B→MRX, RX-1→RX	RN.1	RX-1	1	0	0
#4				RP.0, RP.1→T, B	HIGH Z	RP	1	1	0
#5				B, T→RN.1, RN.0	HIGH Z	RN	1	1	0
#6				MRN→B; RN+1→RN	MRP	RP	0	1	0
#7				B→T; MRN→B; RN+1→RN	M(RP+1)	RP+1	0	1	0
#8				B, T→RP.0, RP.1	HIGH Z	RP	1	1	0

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	N LINES
THE FOLLOWING ARE ALL LINKED INSTRUCTIONS "68" PRECEDES ALL THE OP CODES, SO THERE IS A DOUBLE FETCH									
S1#1	9	0-F	SRET	RN.0, RN.1→T, B	HIGH Z	RN	1	1	0
#2				RX+1→RX	HIGH Z	RX	1	1	0
#3				B, T→RP.1, RP.0	HIGH Z	RP	1	1	0
#4				MRX→B; RX+1→RX	M(RX+1)	RX+1	0	1	0
#5				B→T; MRX→B	M(RX+1)	RX+2	0	1	0
#6				B, T→RN.0, RN.1	HIGH Z	RN	1	1	0
S1#1	A	0-F	RSXD	RN.0, RN.1→T, B	HIGH Z	RN	1	1	0
#2				T→MRX; RX-1→RX	RN.0	RX	1	0	0
#3				B→MRX; RX-1→RX	RN.1	RX-1	1	0	0
S1#1	B	0-F	RNX	RN.0, RN.1→T, B	HIGH Z	RN	1	1	0
#2				B, T→RX.1, RX.0	HIGH Z	RX	1	1	0
S1#1	C	0-F	RLDI	MRP→B; RP+1→RP	MRP	RP	0	1	0
#2				B→T; MRP→B; RP+1→RP	M(RP+1)	RP+1	0	1	0
#3				B, T→RN.0, RN.1; RP+1→RP	HIGH Z	RN	1	1	0
S1#1	F	4	DADD	MRX+D→DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP	1	1	0
S1#1	F	7	DSM	D-MRX→DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP	1	1	0
S1#1	F	C	DADI	MRP+D→DF, D; RP+1→RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP+1	1	1	0
S1#1	F	F	DSMI	D-MRP→DF, D RP+1→RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP+1	1	1	0

Instruction Summary

N

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	IDL	LDN														
1	INC															
2	DEC															
3	BR	BQ	BZ	BDF	B1	B2	B3	B4	SKP	BNQ	BNZ	BNF	BN1	BN2	BN3	BN4
4	LDA															
5	STR															
6	IRX	OUT							*	INP						
7	RET	DIS	LDXA	STXD	ADC	SDB	SHRC	SMB	SAV	MARK	REQ	SEQ	ADCI	SDBI	SHLC	SMBI
8	GLO															
9	GHI															
A	PLO															
B	PHI															
C	LBR	LBQ	LBZ	LBDF	NOP	LSNQ	LSNZ	LSNF	LSKP	LBNQ	LBNZ	LBNF	LSIE	LSQ	LSZ	LSDF
D	SEP															
E	SEX															
F	LDX	OR	AND	XOR	ADD	SD	SHR	SM	LDI	ORI	ANI	XRI	ADI	SDI	SHL	SMI
	'68' LINKED OPCODES (DOUBLE FETCH)															
0	STPC	DTC	SPM2	SCM2	SPM1	SCM1	LDC	STM	GEC	ETQ	XIE	XID	CIE	CID	—	—
2	DBNZ															
3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BCI	BXI
6	RLXA															
7	—	—	—	—	DADC	—	DSAV	DSMB	—	—	—	—	DACI	—	—	DSBI
8	SCAL															
9	SRET															
A	RSXD															
B	RNX															
C	RLDI															
F	—	—	—	—	DADD	—	—	DSM	—	—	—	—	DADI	—	—	DSMI

* '68' IS USED AS A LINKING OPCODE FOR THE DOUBLE FETCH INSTRUCTIONS.

CDP1804AC Mask-Programming

The ROM pattern for the CDP1804AC may be submitted on a suitable media, such as floppy diskette, ROM or EPROM.

In addition to specifying the 2K-byte ROM pattern, the address space for the ROM and RAM must also be defined. The locations of ROM and RAM in the CDP1804AC are determined by AND-gate decoders which decode the upper memory addresses and are programmable at the time of ROM pattern masking during device fabrication. The logical values of the decoder inputs are selectable as 1 or P (positive), 0 or N (negative), or X (don't care). A 5-bit decoder is used for the ROM selection, so the ROM can be placed at one or more of the 32 available 2K-byte blocks within the 65,536 locations of memory. Similarly, the RAM has a 10-bit decoder and can be selected at one or more of the available 64-byte blocks. If the RAM is located within the ROM space, only the RAM will be enabled at the locations where both are mapped. The RAM may also be selectively disabled.

Programming Options

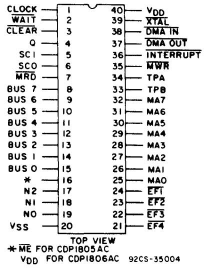
Address Options

The logic levels of high-order address bits are mask programmable in the CDP1804AC. The high (1), low (0), or "don't care" (X) logic status of the high-order address bits is dependent upon the desired starting address of the 2K-byte ROM block and the 64-byte RAM block. The desired logic levels for the high-order address bits (A15 through A6) can be selected by use of the ROM order sheet.

Multiple mapping can be achieved by choosing X (don't care) for one or more of the high-order address lines; this choice will cause the ROM or RAM block to appear in more than one location in the 64K memory space. The RAM may also be disabled completely in the RUN (ROM/RAM) mode by programming the RAM enable bit to an N.

CDP1805AC, CDP1806AC

TERMINAL ASSIGNMENT



*ME FOR CDP1805AC
VDD FOR CDP1806AC 92CS-35004

CMOS 8-Bit Microprocessor With On-Chip RAM▲ and Counter/Timer

Performance Features:

- *Instruction time of 3.2 μs, −40 to +85° C*
- *123 instructions - upwards software compatible with CDP1802*
- *BCD arithmetic instructions*
- *Low-power IDLE mode*
- *Pin compatible with CDP1802 except for terminal 16*
- *64K-byte memory address capability*
- *64 bytes of on-chip RAM▲*
- *16 x 16 matrix of on-board registers*
- *On-chip crystal or RC controlled oscillator*
- *8-bit Counter/Timer*

▲CDP1805AC only

The RCA-CDP1805AC and CDP1806AC are functional and performance enhancements of the CDP1802 CMOS 8-bit register-oriented microprocessor series and are designed for use in general-purpose applications

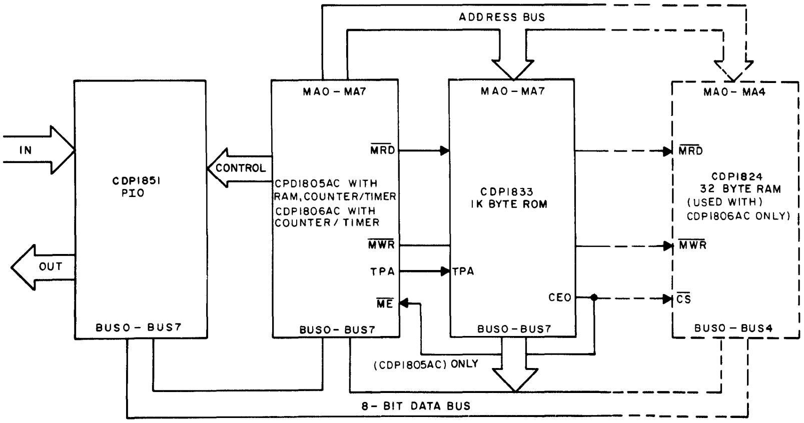
The CDP1805AC hardware enhancements include a 64-byte RAM and an 8-bit presettable down counter. The Counter/Timer which generates an internal interrupt request, can be programmed for use in time-base, event-counting, and pulse-duration measurement applications. The Counter/Timer underflow output can also be directed to the Q output terminal. The CDP1806AC hardware enhancements are identical to the CDP1805AC, except the CDP1806AC contains no on-chip RAM.

The CDP1805AC and CDP1806AC are identical to the CDP1804AC, except for the on-chip memory, and may be used for CDP1804AC development purposes.

The CDP1805AC and CDP1806AC software enhancements include 32 more instructions that the CDP1802. The 32 new software instructions add subroutine call and return capability, enhanced data transfer manipulation, Counter/Timer control, improved interrupt handling, single-instruction loop counting, and BCD arithmetic.

Upwards software and hardware compatibility is maintained when substituting a CDP1805AC or CDP1806AC for other CDP1800-series microprocessors. Pinout is identical except for the replacement of V_{CC} with $\overline{ME}$ on the CDP1805AC and the replacement of V_{CC} with V_{DD} on the CDP1806AC.

The CDP1805AC and CDP1806AC have an operating voltage range of 4 V to 6.5 V and are supplied in a 40-lead hermetic dual-in-line ceramic package (D suffix), 40-lead dual-in-line plastic package (E suffix) and 44-lead plastic chip-carrier (PCC) package (Q suffix).



92CM-34987R1

Fig. 1 - Typical CDP1805AC, CDP1806AC small microprocessor system.

File Number **1370**

CDP1805AC, CDP1806AC

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal) .... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPE D) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -40 to +85°C (PACKAGE TYPE Q)* .... 500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D .... -55 to +125°C
PACKAGE TYPE E and Q .... -40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum .... +265°C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

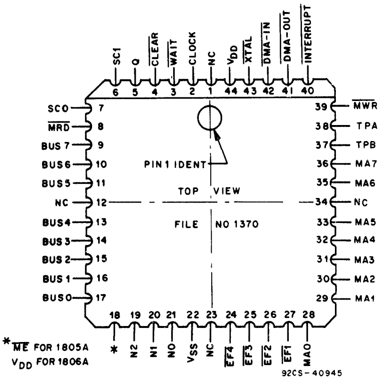
RECOMMENDED OPERATING CONDITIONS at T_A = -40 to +85°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITION	LIMITS		UNITS
		CDP1805ACD, CDP1805ACE CDP1806ACD, CDP1806ACE		
	V_{DD} (V)	MIN.	MAX.	
DC Operating Voltage Range	—	4	6.5	V
Input Voltage Range	—	V_{SS}	V_{DD}	
Minimum Instruction Time* (f_{CL}=5 MHz)	5	3.2	—	μs
Maximum DMA Transfer Rate	5	—	0.625	Mbytes/s
Maximum Clock Input Frequency, Load Capacitance (CL) = 50 pF	5	DC	5	MHz
Maximum External Counter/Timer Clock Input Frequency to $\overline{EF1}$, $\overline{EF2}$ t_{CLX}	5	DC	2	

*Equals 2 machine cycles - one Fetch and one Execute operation for all instructions except Long Branch, Long Skip, NOP, and "68" family instructions, which are more than two cycles.

TERMINAL ASSIGNMENT



44-Lead Plastic Chip-Carrier (PCC) Package (Q Suffix)

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ± 5%, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1805ACD, CDP1805ACE CDP1806ACD, CDP1806ACE			
					Min.	Typ.*	Max.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	50	200	µA
Output Low Drive (Sink) Current (Except $\overline{\text{XTAL}}$)	I_{OL}	0.4	0, 5	5	1.6	4	—	mA
$\overline{\text{XTAL}}$ Output	I_{OL}	0.4	5	5	0.2	0.4	—	
Output High Drive (Source) Current (Except $\overline{\text{XTAL}}$)	I_{OH}	4.6	0, 5	5	-1.6	-4	—	
$\overline{\text{XTAL}}$	I_{OH}	4.6	0	5	-0.1	-0.2	—	
Output Voltage Low-Level	V_{OL}	—	0, 5	5	—	0	0.1	V
Output Voltage High Level	V_{OH}	—	0, 5	5	4.9	5	—	
Input Low Voltage (BUS 0 — BUS 7, $\overline{\text{ME}}$)	V_{IL}	0.5, 4.5	—	5	—	—	1.5	
Input High Voltage (BUS 0 — BUS 7, $\overline{\text{ME}}$)	V_{IH}	0.5, 4.5	—	5	3.5	—	—	
Schmitt Trigger Input Voltage (Except BUS 0 — BUS 7, $\overline{\text{ME}}$)		0.5, 4.5	—	5				
Positive Trigger Threshold	V_P				2.2	2.9	3.6	
Negative Trigger Threshold	V_N				0.9	1.9	2.8	
Hysteresis	V_H				0.3	0.9	1.6	
Input Leakage Current	I_{IN}	—	0, 5	5	—	±0.1	±5	µA
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	—	±0.2	±5	
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	
Total Power Dissipation Δ Run		—	—	5	—	35	50	mW
Idle "00" at M(0000)		—	—	5	—	12	18	
Minimum Data Retention Voltage	V_{DR}	$V_{DD} = V_{DR}$			—	2	2.4	V
Data Retention Current	I_{DR}	V_{DD} = 2.4			—	25	100	µA

•Typical values are for T_A = 25°C and nominal V_{DD}.

Δ External clock: f = 5 MHz, t_r, t_f = 10 ns. C_L = 50 pF.

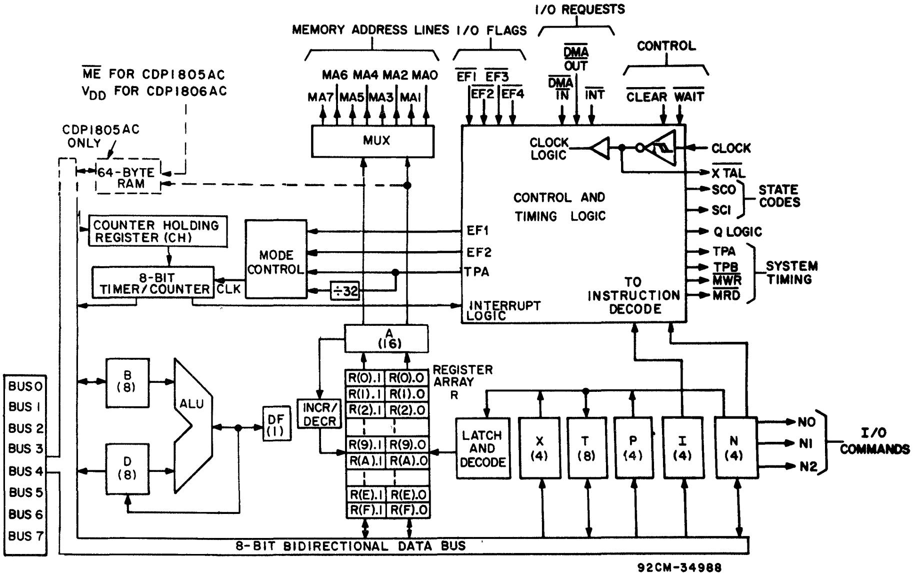
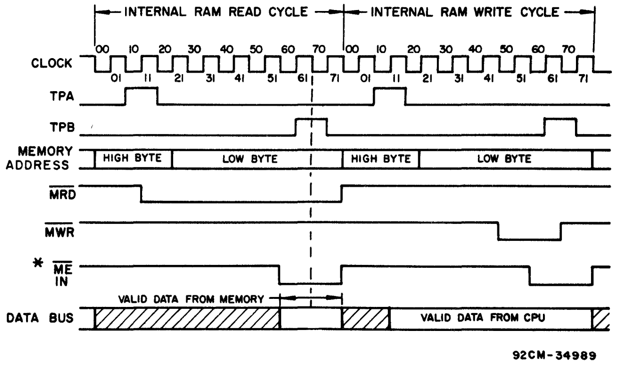


Fig. 2 - Block diagram for CDP1805AC and CDP1806AC.

TIMING WAVEFORMS FOR POSSIBLE OPERATING MODES



***NOTE**

ME HAS A MINIMUM SETUP AND HOLD TIME WITH RESPECT TO THE BEGINNING OF CLOCK 70. FOR A MEMORY READ OPERATION, RAM DATA WILL APPEAR ON THE DATA BUS DURING THE TIME ME IS ACTIVE AFTER CLOCK 31. THE TIME SHOWN CAN BE LONGER, IF FOR INSTANCE, A DMA OUT OPERATION IS PERFORMED ON INTERNAL RAM DATA, TO ALLOW DATA ENOUGH TIME TO BE LATCHED INTO AN EXTERNAL DEVICE. THE INTERNAL RAM IS AUTOMATICALLY DESELECTED AT THE END OF CLOCK 71, INDEPENDENT OF ME.

* FOR CDP1805AC ONLY

Fig. 3 - Internal memory operation timing waveforms for CDP1805AC and CDP1806AC.

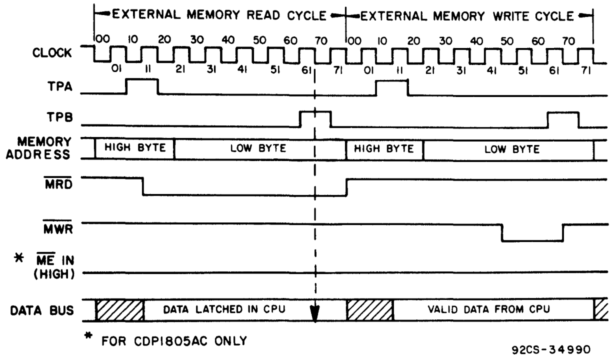


Fig. 4 - External memory operation timing waveforms for CDP1805AC and CDP1806AC.

ENHANCED CDP1805AC and CDP1806AC OPERATION

TIMING

Timing for the CDP1805AC and CDP1806AC is the same as the CDP1802 microprocessor series, with the following exceptions:

- 4.5 clock cycles are provided for memory access instead of 5.
- Q changes 1/2 clock cycle earlier during the SEQ and REQ instructions.
- Flag lines ($\overline{\text{EF1}}$-$\overline{\text{EF4}}$) are sampled at the end of the S0 cycle instead of at the beginning of the S1 cycle.
- Pause can only occur on the low-to-hgh transition of either TPA or TPB, instead of any negative clock transition.

SPECIAL FEATURES

Schmitt triggers are provided on all inputs, except $\overline{\text{ME}}$ and BUS 0-BUS 7, for maximum immunity from noise and slow signal transitions. A Schmitt trigger in the oscillator section allows operation with an RC or crystal.

The CDP1802-series LOAD mode is not retained. This mode ($\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$=0) is not allowed on the CDP1805AC and CDP1806AC.

A low power mode is provided, which is initiated via the IDLE instruction. In this mode all external signals, except the oscillator, are stopped on the low-to-high transition of TPB. All outputs remain in their previous states, $\overline{\text{MRD}}$ is set to a logic "1", and the data bus floats. The IDLE mode is exited by a DMA or INT condition. The INT includes both external interrupts and interrupts generated by the Counter/Timer. The only restrictions are that the Timer mode, which uses the TPA ÷ 32 clock source, and the underflow condition of the Pulse Width Measurement modes are not available to exit the IDLE mode.

SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus):

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O) Lines:

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices. The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register. The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the $\overline{\text{MRD}}$ signal:

$\overline{\text{MRD}}$ = V_{DD}: Input data from I/O to CPU and Memory
$\overline{\text{MRD}}$ = V_{SS}: Output data from Memory to I/O

$\overline{\text{EF1}}$ to $\overline{\text{EF4}}$ (4 Flags):

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. The flag(s) are sampled at the end of every S0 cycle. $\overline{\text{EF1}}$ and $\overline{\text{EF2}}$ are also used for event counting and pulse-width measurement in conjunction with the Counter/Timer.

$\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, $\overline{\text{DMA-OUT}}$ (3 I/O Requests)

$\overline{\text{DMA-IN}}$ and $\overline{\text{DMA-OUT}}$ are sampled during TPB every S1, S2, and S3 cycle. $\overline{\text{INTERRUPT}}$ is sampled during TPB every S1 and S2 cycle.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable (MIE) is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and R(0) is incremented.

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority followed by DMA-OUT and then INTERRUPT. (The interrupt request is not internally latched and must be held true after DMA.)

SC0, SC1, (2 State Code Lines):

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

H = V_{DD}, L = V_{SS}.

TPA, TPB (2 Timing Pulses):

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the high-order byte of the multiplexed 16-bit memory address.

MA0 to MA7 (8 Memory Address Lines):

In each cycle, the higher-order byte of a 16-bit memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines 1/2 clock after the termination of TPA.

$\overline{\text{MWR}}$ (Write Pulse):

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{\text{MRD}}$ (Read Level):

A low level on $\overline{\text{MRD}}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory and to indicate the direction of data transfer during an I/O instruction.

Q:

Single bit output from the CPU which can be set or reset, under program control. During SEQ and REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB. The Q line can also be controlled by the Counter/Timer underflow via the Enable Toggle Q instruction.

The Enable Toggle Q command connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q line changes state. This command is cleared by a LOAD COUNTER (LDC) instruction with the Counter/Timer stopped, a CPU reset, or a BRANCH COUNTER INTERRUPT (BCI) instruction with the counter interrupt flip-flop set.

CLOCK:

Input for externally generated single-phase clock. The maximum clock frequency is 5 MHz at V_{DD} = 5 V. The clock is counted down internally to 8 clock pulses per machine cycle.

$\overline{\text{XTAL}}$:

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$ (2 Control Lines):

Provide four control modes as listed in the following truth table:

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	NOT ALLOWED
L	H	RESET
H	L	PAUSE
H	H	RUN

$\overline{\text{ME}}$ (Memory Enable CDP1805AC Only):

This active low input is used to select or deselect the internal RAM. It must be active prior to clock 70 for an internal RAM access to take place. Internal RAM data will appear on the data bus during the time that $\overline{\text{ME}}$ is active (after clock 31). Thus, if this data is to be latched into an external device (i.e., during an OUTPUT instruction or DMA OUT cycle), $\overline{\text{ME}}$ should be wide enough to provide enough time for valid data to be latched. The internal RAM is automatically deselected after clock 71. $\overline{\text{ME}}$ is ineffective when $\overline{\text{MRD}} \bullet \overline{\text{MWR}}$ =1.

The internal RAM is not internally mask-decoded. Decoding of the starting address is performed externally, and may reside in any 64-byte block of memory.

V_{DD} (CDP1806AC Only):

This input replaces the $\overline{\text{ME}}$ signal of the CDP1805AC and must be connected to the positive power supply.

V_{DD}, V_{SS}, (Power Levels):

V_{SS} is the most negative supply voltage terminal and is normally connected to ground. V_{DD} is the positive supply voltage terminal. All outputs swing from V_{SS} to V_{DD}. The recommended input voltage swing is from V_{SS} to V_{DD}.

ARCHITECTURE

Fig. 2 shows a block diagram of the CDP1805AC and CDP1806AC. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following paths:

1. the external memory (multiplexed, higher-order byte first on to 8 memory address lines)
2. the D register (either of the two bytes can be gated to D)
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.
4. to any other 16-bit scratch pad register in the array.

The four paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

Most instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second —and more if necessary — are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations
2. indicate to the I/O devices a command code or device-selection code for peripherals
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P)
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to subroutine . When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R(0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations
2. output instructions
3. input instructions
4. register to memory transfer
5. memory to register transfer
6. interrupt and subroutine handling.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F, and the RLDI instruction 68CN. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the CDP1805AC and CDP1806AC architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters. The new RLDI, RLXA, RSXD, and RNX instructions also allow loading, storing, and exchanging the full 16-bit contents of the R registers without affecting the D register. The new DBNZ instruction allows decrementing and branching-on-not-zero of any 16-bit R register also without affecting the D register.

The Q Flip-Flop

An internal flip-flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. It can also be driven by the underflow output of the counter/timer. The output of Q is also available as a microprocessor output.

Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
B	8 Bits	Auxiliary Holding Register
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which Register is Program Counter
X	4 Bits	Designates which Register is Data Pointer
N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nibble)
Q	1 Bit	Output Flip-Flop
CNTR	8-Bits	Counter/Timer
CH	8 Bits	Holds Counter Jam Value
MIE	1 Bit	Master Interrupt Enable
CIE	1 Bit	Counter Interrupt Enable
XIE	1 Bit	External Interrupt Enable
CIL	1 Bit	Counter Interrupt Latch

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initialized. When an interrupt request occurs and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Master Interrupt Enable is automatically deactivated to inhibit further interrupts. The user's interrupt routine is now in control; the contents of T may be saved by means of a single SAV instruction (78) in the memory location pointed to by R(X) or the contents of T, D, and DF may be saved using a single DSAV instruction (6876). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with either a RET instruction (70) which permits further interrupts, or a DIS instruction (71), which disables further interrupts.

Interrupt Generation and Arbitration (See Fig. 5)

Interrupt requests can be generated from the following sources:

1. Externally through the interrupt input (Request not latched)
2. Internally due to Counter/Timer response (Request is latched)
   a. On the transition from count $(01)_{16}$ to its next value (counter underflow)
   b. On the ↗ transition of $\overline{EF1}$ in pulse measurement mode 1
   c. On the ↗ transition of $\overline{EF2}$ in pulse measurement mode 2

For an interrupt to be serviced by the CPU, the appropriate Interrupt Enable flip-flops must be set. Thus, the External Interrupt Enable flip-flop must be set to service an external interrupt request, and the Counter Interrupt Enable flip-flop must be set to service an internal Counter/Timer interrupt request. In addition, the Master Interrupt Enable flip-flop (as used in the CDP1802) must be set to service either type of request. All 3 flip-flops are initially enabled with the application of a hardware reset, and, can be selectively enabled or disabled with software: CIE, CID instructions for the CIE flip-flop; XIE, XID instructions for the XIE flip-flop; RET, DIS instructions for the MIE flip-flop.

Short branch instructions on Counter Interrupt (BCI) and External Interrupt (BXI) can be placed in the user's interrupt service routine to provide a means of identifying and prioritizing the interrupt source. Note, however, that since the External Interrupt request is not latched, it must remain active until the short branch is executed if this priority arbitration scheme is used.

Interrupt requests can also be polled if automatic interrupt service is not desired (MIE=0). With the Counter Interrupt and External Interrupt short branch instructions, the branch will be taken if an interrupt request is pending, regardless of the state of any of the 3 Interrupt Enable flip-flops. The latched counter interrupt request signal will be reset when the branch is taken, when the CPU is reset, or with a LDC instruction with the Counter stopped. Note, that exiting a counter-initiated interrupt routine without resetting the counter-interrupt latch will result in immediately re-entering the interrupt routine.

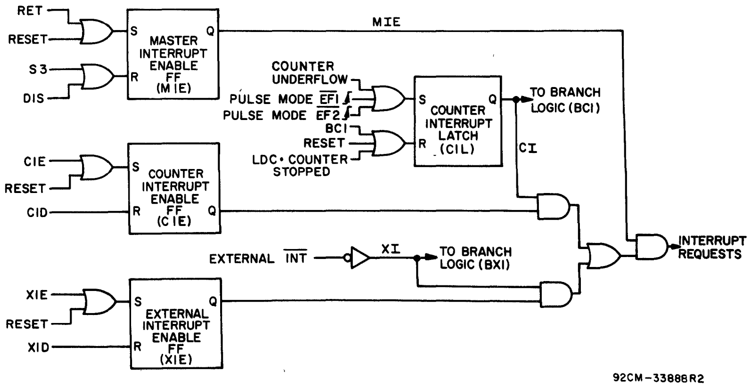

RET
RESET
S3
DIS
S
R
Q
MASTER INTERRUPT ENABLE FF (MIE)
MIE
COUNTER UNDERFLOW
PULSE MODE $\overline{EF1}$
PULSE MODE $\overline{EF2}$
BCI
RESET
LDC • COUNTER STOPPED
COUNTER INTERRUPT LATCH (CIL)
TO BRANCH LOGIC (BCI)
CI
CIE
RESET
CID
COUNTER INTERRUPT ENABLE FF (CIE)
EXTERNAL $\overline{INT}$
XI
TO BRANCH LOGIC (BXI)
INTERRUPT REQUESTS
XIE
RESET
XID
EXTERNAL INTERRUPT ENABLE FF (XIE)
92CM-33886R2

Fig. 5 - Interrupt logic-control diagram for CDP1805AC and CDP1806AC.

Counter/Timer and Controls (see Fig. 6)

This logic consists of a presettable 8-bit down-counter (Modulo N type), and a conditional divide-by-32 prescaler. After counting down to $(01)_{16}$ the counter returns to its initial value at the next count and sets the Counter Interrupt Latch. It will continue decrementing on subsequent counts. If the counter is preset to $(00)_{16}$ a full 256 counts will occur.

During a Load Counter instruction (LDC) if the counter was stopped with a STPC instruction, the counter and its holding register (CH) are loaded with the value in the D register and any previous counter interrupt is cleared. If the LDC is executed when the counter is running, the contents of the D register are loaded into the holding register (CH) only and any previous counter interrupt is not cleared. (LDC RESETS the Counter Interrupt Latch only when the Counter is stopped). After counting down to $(01)_{16}$ the next count will load the new initial value into the counter, set the Counter Interrupt Latch, and operation will continue.

The Counter/Timer has the following five programmable modes:

1. Event Counter 1: Input to counter is connected to the $\overline{\text{EF1}}$ terminal. The high-to-low transition decrements the counter.
2. Event Counter 2: Input to counter is connected to the $\overline{\text{EF2}}$ terminal. The high-to-low transition decrements the counter.
3. Timer: Input to counter is from the divide-by-32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA. The divide-by-32 prescaler is reset when the counter is in a mode other than the Timer mode, system RESET, or stopped by a STPC.
4. Pulse Duration Measurement 1: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{\text{EF1}}$ terminal (gate input) is low. On the transition of $\overline{\text{EF1}}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but counting will continue.
5. Pulse Duration Measurement 2: Operation is identical to Pulse Duration Measurement 1, except $\overline{\text{EF2}}$ is used as the gate input.

The modes can be changed without affecting the stored count.

Those modes which use $\overline{\text{EF1}}$ and $\overline{\text{EF2}}$ terminals as inputs do not exclude testing these flags for branch instructions.

The Stop Counter (STPC) instruction clears the counter mode and stops counting. The STPC instruction should be executed prior to a GEC instruction, if the counter is in the Event Counter Mode 1 or 2.

In addition to the five programmable modes, the Decrement Counter instruction (DTC) enables the user to count in software In order to avoid conflict with counting done in the other modes, the instruction should be used only after the mode has been cleared by a Stop Counter instruction.

The Enable Toggle Q instruction (ETQ) connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q output changes state. This action is independent of the counter mode and the Interrupt Enable flip-flops. The Enable Toggle Q condition is cleared by an LDC with the Counter/Timer stopped, system Reset, or a BCI with CI = 1.

Note: SEQ and REQ instructions are independent of ETQ—they can SET or RESET Q while the Counter is running.

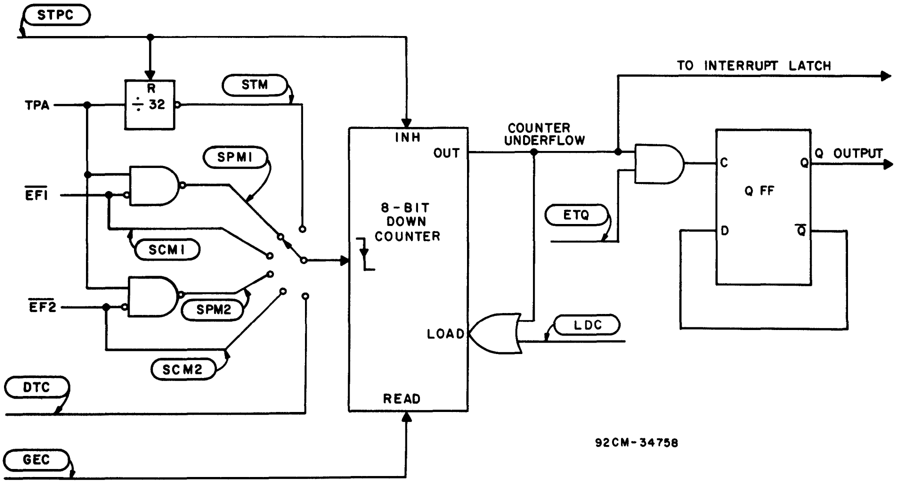


Fig. 6 - Timer/Counter diagram for CDP1805AC and CDP1806AC.

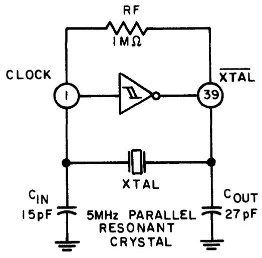
CDP1805AC, CDP1806AC

On-Board Clock (see Figs. 7, 8 and 9)

Clock circuits may use either an external crystal or an RC network.

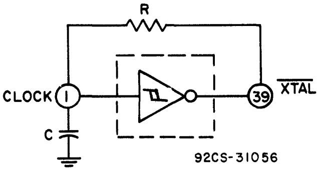
A typical crystal oscillator circuit is shown in Fig. 7. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{\text{XTAL}}$) in parallel with a resistance, RF (1 megohm typ.). Frequency trimming capacitors, C_{IN} and C_{OUT}, may be required at terminals 1 and 39. For additional information on crystal oscillators, see ICAN-6565.

Because of the Schmitt Trigger input, an RC oscillator can be used as shown in Fig. 8. The frequency is approximately 1/RC (see Fig. 9).



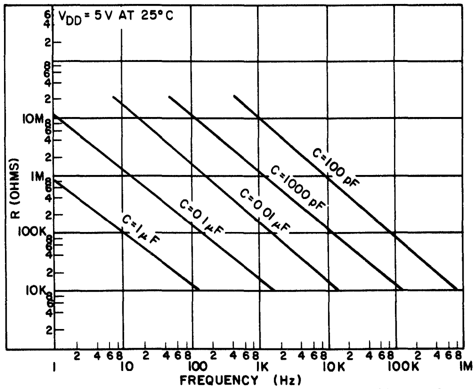
92CS-38099

Fig. 7 - Typical 5 MHz crystal oscillator.



92CS-31056

Fig. 8 - RC network for oscillator.



92CS-34172

Fig. 9 - Nominal component values as a function of frequency for the RC oscillator.

CONTROL MODES

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	NOT ALLOWED
L	H	RESET
H	L	PAUSE
H	H	RUN

The function of the modes are defined as follows:

RESET

The levels on the CDP1805A and CDP1806A external signal lines will asynchronously be forced by RESET to the following states:

Q=0	SC1, SC0=0, 1	BUS 0-7=0
MRD=1	(EXECUTE)	MA0-7=RO.1
TPB=0	N0, N1, N2=0, 0, 0	TPA=0
	$\overline{\text{MWR}}$=1	

Internal changes caused by RESET are:

I, N instruction register is cleared to 00. XIE and CIE are set to allow interrupts following initialize. CIL is cleared (any pending counter interrupt is cleared), counter is stopped, the counter mode is cleared, and ETQ is disabled.

Initialization Cycle

The first machine cycle followiing termination of RESET is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and the following additional changes occur:

I → MIE

X, P → T (The old value of X, P will be put into T. This only has meaning following an orderly Reset with power applied).

X, P, RO ← 0 (X, P, and RO are cleared).

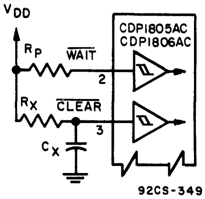
Interrupt and DMA servicing is suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. The use of a 71 instruction followed by 00 at memory locations 0000 and 0001, may be used to reset MIE so as to preclude interrupts until ready for them.

Reset and Initialize do not affect:

D (Accumulator)
DF
R1, R2, R3, R4, R5, R6, R7, R8, R9, FA, RB, RC, RD, RE, RF
CH (Counter Holding Register)
Counter (the counter is stopped but the value is unaffected)

Power-up Reset/Run Circuit

Power-up Reset/Run can be realized with the circuit shown in Fig. 10.



The RC time constant should be greater than the oscillator start-up time (typically 20 ms).

92CS-34991

Fig. 10 - Reset/run diagram.

PAUSE

Pause is a low power mode which stops the internal CPU timing generator and freezes the state of the processor. The CPU may be held in the Pause mode indefinitely. Hardware pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB. A TPB pause can also be initiated by software with the execution of an IDLE instruction. In the pause mode. the oscillator continues to run but subsequent clock transitions are ignored. TPA and TPB remain at their previous state (see Fig. 11).

Pause is entered from RUN by dropping WAIT low. Appropriate Setup and Hold times must be met.

If Pause is entered while in the event counter mode, the appropriate Flag transition will continue to decrement the counter.

Hardware-initiated pause is exited to RUN by raising the Wait line high. Pause entered with an IDLE instruction requires DMA, INTERRUPT or RESET to resume execution.

RUN

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the next high-to-low clock transition, while if paused at TPB, it will resume on the next low-to-high clock transition (see Fig. 11). When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

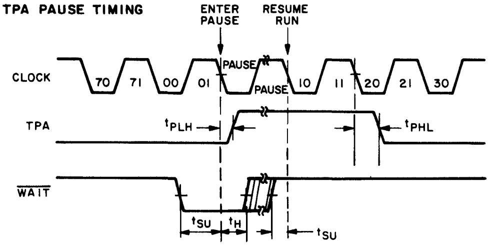
SCHMITT TRIGGER INPUTS

All inputs except BUS 0—BUS 7 and ME contain a Schmitt Trigger circuit, which is especially useful on the CLEAR input as a power-up RESET (see Fig. 10) and the CLOCK input (see Figs. 7 and 8).

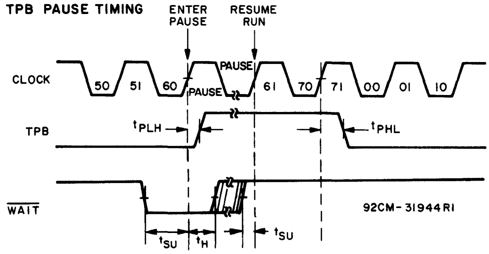
STATE TRANSITIONS

The CDP1805A and CDP1806A state transitions are shown in Fig. 12. Each machine cycle requires the same period of time, 8 clock pulses, except the initialization cycle (INIT) which requires 9 clock pulses. Reset is asynchronous and can be forced at any time.

TPA PAUSE TIMING



TPB PAUSE TIMING



NOTE:
PAUSE (IN CLOCK WAVEFORM) WHILE REPRESENTED HERE AS ONE CLOCK CYCLE IN DURATION, COULD BE INFINITELY LONG.

Fig. 11 - Pause mode timing waveforms.

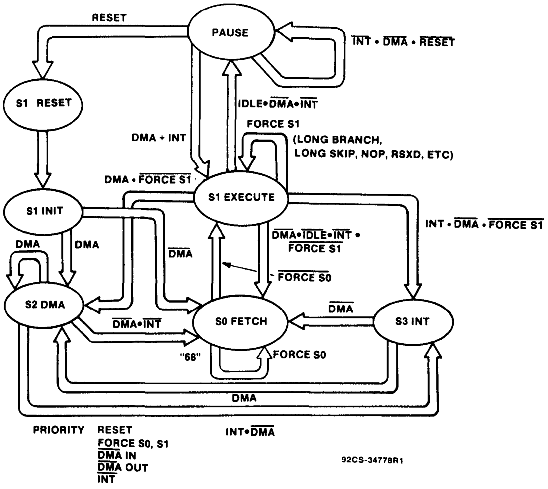

RESET
PAUSE
$\overline{INT}$ • $\overline{DMA}$ • $\overline{RESET}$
S1 RESET
IDLE•$\overline{DMA}$•$\overline{INT}$
FORCE S1
(LONG BRANCH, LONG SKIP, NOP, RSXD, ETC)
DMA + INT
DMA • $\overline{FORCE\ S1}$
S1 EXECUTE
S1 INIT
INT • $\overline{DMA}$ • $\overline{FORCE\ S1}$
DMA
DMA
$\overline{DMA}$
$\overline{DMA}$•$\overline{IDLE}$•$\overline{INT}$ • $\overline{FORCE\ S1}$
$\overline{FORCE\ S0}$
S2 DMA
$\overline{DMA}$
$\overline{DMA}$•$\overline{INT}$
S0 FETCH
S3 INT
"68"
FORCE S0
DMA
PRIORITY
RESET
FORCE S0, S1
DMA IN
DMA OUT
INT
INT•$\overline{DMA}$
92CS-34778R1

Fig. 12 - State transition diagram.

INSTRUCTION SET

The CDP1805AC and CDP1806AC instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)

R(W).1: Higher-order byte of R(W)

Operation Notation

M (R(N))→D; R(N) + 1→R(N)

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I — INSTRUCTION SUMMARY (For Notes, see also page 17)

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE				
LOAD IMMEDIATE	2	LDI	F8	M(R(P))→D; R(P)+1→R(P)
REGISTER LOAD IMMEDIATE	5	RLDI	68CN■	M(R(P))→R(N).1; M(R(P))+1→ R(N).0; R(P)+2→R(P)
LOAD VIA N	2	LDN	0N	M(R(N))→D; FOR N NOT 0
LOAD ADVANCE	2	LDA	4N	M(R(N))→D; R(N)+1→R(N)
LOAD VIA X	2	LDX	F0	M(R(X))→D
LOAD VIA X AND ADVANCE	2	LDXA	72	M(R(X))→D; R(X)+1→R(X)
REGISTER LOAD VIA X AND ADVANCE	5	RLXA	686N■	M(R(X))→R(N).1; M(R(X)+1)→ R(N).0; R(X))+2→R(X)
STORE VIA N	2	STR	5N	D→M(RN))
STORE VIA X AND DECREMENT	2	STXD	73	D→M(R(X)); R(X)-1→R(X)
REGISTER STORE VIA X AND DECREMENT	5	RSXD	68AN■	R(N).0→M(R(X)); R(N).1→ M(R(X)-1); R(X)-2→R(X)
REGISTER OPERATIONS				
INCREMENT REG N	2	INC	1N	R(N)+1→R(N)
DECREMENT REG N	2	DEC	2N	R(N)-1→R(N)
DECREMENT REG N AND LONG BRANCH IF NOT EQUAL 0	5	DBNZ	682N	R(N)-1→R(N); IF R(N) NOT 0, M(R(P))→R(P).1, M(R(P)+1)→ R(P).0, ELSE R(P)+2→R(P)
INCREMENT REG X	2	IRX	60	R(X)+1→R(X)
GET LOW REG N	2	GLO	8N	R(N).0→D
PUT LOW REG N	2	PLO	AN	D→R(N).0
GET HIGH REG N	2	GHI	9N	R(N).1→D
PUT HIGH REG N	2	PHI	BN	D→R(N).1
REGISTER N TO REGISTER X COPY	4	RNX	68BN■	R(N)→R(X)
LOGIC OPERATIONS (Note 5)				
OR	2	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	2	ORI	F9	M(R(P)) OR D→D; R(P)+1→R(P)
EXCLUSIVE OR	2	XOR	F3	M(R(X)) XOR D→D
EXCLUSIVE OR IMMEDIATE	2	XRI	FB	M(R(P)) XOR D→D; R(P)+1→R(P)
AND	2	AND	F2	M(R(X)) AND D→D
AND IMMEDIATE	2	ANI	FA	M(R(P)) AND D→D; R(P)+1→R(P)
SHIFT RIGHT	2	.SHR	F6	SHIFT D RIGHT, LSB(D)→DF, 0→MSB(D)
SHIFT RIGHT WITH CARRY	2	SHRC	76▲	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
RING SHIFT RIGHT	2	RSHR		
SHIFT LEFT	2	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)

■Previous contents of T register are destroyed during instruction execution

▲This instruction is associated with more than one mnemonic Each mnemonic is individually listed.

Table I — INSTRUCTION SUMMARY

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
LOGIC OPERATIONS (Note 5) (Cont'd)				
SHIFT LEFT WITH CARRY	2	SHLC	7E▲	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	2	RSHL		
ARITHMETIC OPERATIONS (Note 5)				
ADD	2	ADD	F4	M(R(X))+D→DF, D
DECIMAL ADD	4	DADD	68F4	M(R(X))+D→DF, D DECIMAL ADJUST→DF, D
ADD IMMEDIATE	2	ADI	FC	M(R(P))+D→DF, D; R(P)+1→R(P)
DECIMAL ADD IMMEDIATE	4	DADI	68FC	M(R(P))+D→DF,D R(P)+1→R(P) DECIMAL ADJUST→DF, D
ADD WITH CARRY	2	ADC	74	M(R(X))+D+DF→DF, D
DECIMAL ADD WITH CARRY	4	DADC	6874	M(R(X))+D+DF→DF, D DECIMAL ADJUST→DF, D
ADD WITH CARRY, IMMEDIATE	2	ADCI	7C	M(R(P))+D+DF→DF, D R(P)+1→R(P)
DECIMAL ADD WITH CARRY, IMMEDIATE	4	DACI	687C	M(R(P))+D+DF→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
SUBTRACT D	2	SD	F5	M(R(X))-D→DF, D

SUBTRACT D IMMEDIATE	2	SDI	FD	M(R(P))-D→DF, D;
				R(P)+1→R(P)

SUBTRACT D WITH BORROW	2	SDB	75	M(R(X))-D-(NOT DF)→DF, D

SUBTRACT D WITH BORROW, IMMEDIATE	2	SDBI	7D	M(R(P))-D-(NOT DF)→DF, D;
				R(P)+1→R(P)

SUBTRACT MEMORY	2	SM	F7	D-M(R(X))→DF, D
DECIMAL SUBTRACT MEMORY	4	DSM	68F7	D-M(R(X))→DF, D DECIMAL ADJUST→DF, D

SUBTRACT MEMORY IMMEDIATE	2	SMI	FF	D-M(R(P))→DF, D;
				R(P)+1→R(P)

DECIMAL SUBTRACT MEMORY, IMMEDIATE	4	DSMI	68FF	D-M(R(P))→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
SUBTRACT MEMORY WITH BORROW	2	SMB	77	D-M(R(X))-(NOT DF)→DF, D
DECIMAL SUBTRACT MEMORY WITH BORROW	4	DSMB	6877	D-M(R(X))-(NOT DF)→DF, D DECIMAL ADJUST→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	2	SMBI	7F	D-M(R(P))-(NOT DF)→DF, D R(P)+1→R(P)
DECIMAL SUBTRACT MEMORY WITH BORROW, IMMEDIATE	4	DSBI	687F	D-M(R(P))-(NOT DF)→DF, D R(P)+1→R(P) DECIMAL ADJUST→DF, D
BRANCH INSTRUCTIONS — SHORT BRANCH				
SHORT BRANCH	2	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	2	NBR	38▲	R(P)+1→R(P)

SHORT BRANCH IF D = 0	2	BZ	32	IF D = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF D NOT 0	2	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

▲This instruction is associated with more than one mnemonic Each mnemonic is individually listed.

Table I — INSTRUCTION SUMMARY

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS — SHORT BRANCH (Cont'd)				

SHORT BRANCH IF DF = 1	2	BDF	33▲	IF DF = 1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF POS OR ZERO	2	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	2	BGE		

SHORT BRANCH IF DF = 0	2	BNF	3B▲	IF D = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF MINUS	2	BM		
SHORT BRANCH IF LESS	2	BL		

SHORT BRANCH IF Q = 1	2	BQ	31	IF Q = 1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF Q = 0	2	BNQ	39	IF Q = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF1 = 1
($\overline{EF1}$ = V_{SS})
	2	B1	34	IF EF1 = 1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF1 = 0
($\overline{EF1}$ = V_{DD})
	2	BN1	3C	IF EF1 = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF2 = 1
($\overline{EF2}$ = V_{SS})
	2	B2	35	IF EF2 = 1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF2 = 0
($\overline{EF2}$ = V_{DD})
	2	BN2	3D	IF EF2 = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF3 = 1
($\overline{EF3}$ = V_{SS})
	2	B3	36	IF EF3 = 1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF3 = 0
($\overline{EF3}$ = V_{DD})
	2	BN3	3E	IF EF3 = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF4 = 1
($\overline{EF4}$ = V_{SS})
	2	B4	37	IF EF4 =1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH IF EF4 = 0
($\overline{EF4}$ = V_{DD})
	2	BN4	3F	IF EF4 = 0, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

SHORT BRANCH ON COUNTER INTERRUPT	3	BCI	683E•	IF CI=1, M(R(P))→R(P).0; 0→CI
				ELSE R(P)+1→R(P)

SHORT BRANCH ON EXTERNAL INTERRUPT	3	BXI	683F	IF XI=1, M(R(P))→R(P).0
				ELSE R(P)+1→R(P)

BRANCH INSTRUCTIONS — LONG BRANCH				
LONG BRANCH	3	LBR	C0	M(R(P))→R(P) 1, M(R(P)+1)→R(P).0
NO LONG BRANCH (SEE LSKP)	3	NLBR	C8▲	R(P)+2→R(P)

LONG BRANCH IF D = 0	3	LBZ	C2	IF D = 0, M(R(P))→R(P).1
				M(R(P)+1)→R(P) 0
				ELSE R(P)+2→R(P)

LONG BRANCH IF D NOT 0	3	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1
				M(R(P)+1)→R(P).0
				ELSE R(P)+2→R(P)

LONG BRANCH IF DF = 1	3	LBDF	C3	IF DF = 1, M(R(P))→R(P).1
				M(R(P)+1)→R(P).0
				ELSE R(P)+2→R(P)

LONG BRANCH IF DF = 0	3	LBNF	CB	IF DF = 0, M(R(P))→R(P).1
				M(R(P)+1)→R(P).0
				ELSE R(P)+2→R(P)

LONG BRANCH IF Q = 1	3	LBQ	C1	IF Q = 1, M(R(P))→R(P).1
				M(R(P)+1)→R(P).0
				ELSE R(P)+2→R(P)

LONG BRANCH IF Q = 0	3	LBNQ	C9	IF Q = 0, M(R(P))→R(P).1
				M(R(P)+1)→R(P).0
				ELSE R(P)+2→R(P)

▲This instruction is associated with more than one mnemonic Each mnemonic is individually listed

• ETQ cleared by LDC with the Counter/Timer stopped, reset of CPU, or BCI • (CI=1).

CI = Counter Interrupt, XI = External Interrupt

Table I — INSTRUCTION SUMMARY

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
SKIP INSTRUCTIONS				
SHORT SKIP (SEE NBR)	2	SKP	38[▲]	R(P)+1→R(P)
LONG SKIP (SEE NLBR)	3	LSKP	C8[▲]	R(P)+→R(P)

LONG SKIP IF D = 0	3	LSZ	CE	IF D = 0, R(P)+2→R(P)
				ELSE CONTINUE

LONG SKIP IF D NOT 0	3	LSNZ	C6	IF D NOT 0, R(P)+2→R(P)
				ELSE CONTINUE

LONG SKIP IF DF = 1	3	LSDF	CF	IF DF = 1, R(P)+2→R(P)
				ELSE CONTINUE

LONG SKIP IF DF = 0	3	LSNF	C7	IF DF = 0, R(P)+2→R(P)
				ELSE CONTINUE

LONG SKIP IF Q = 1	3	LSQ	CD	IF Q = 1, R(P)+2→R(P)
				ELSE CONTINUE

LONG SKIP IF Q = 0	3	LSNQ	C5	IF Q = 0, R(P)+2→R(P)
				ELSE CONTINUE

LONG SKIP IF MIE = 1	3	LSIE	CC	IF MIE = 1, R(P)+2→R(P)
				ELSE CONTINUE

CONTROL INSTRUCTIONS				
IDLE	2	IDL	00[#]	STOP ON TPB; WAIT FOR DMA OR INTERRUPT; BUS FLOATS
NO OPERATION	3	NOP	C4	CONTINUE
SET P	2	SEP	DN	N→P
SET X	2	SEX	EN	N→X
SET Q	2	SEQ	7B	1→Q
RESET Q	2	REQ	7A	0→Q
PUSH X, P TO STACK	2	MARK	79	(X, P)→T; (X, P)→M(R(2)) THEN P→X; R(2)−1→R(2)
TIMER/COUNTER INSTRUCTIONS				
LOAD COUNTER	3	LDC	6806[•]	CNTR STOPPED: D→CH, CNTR; 0→CI. CNTR RUNNING; D→CH
GET COUNTER	3	GEC	6808	CNTR→D
STOP COUNTER	3	STPC	6800	STOP CNTR CLOCK; 0→÷32 PRESCALER
DECREMENT TIMER/COUNTER	3	DTC	6801	CNTR-1→CNTR
SET TIMER MODE AND START	3	STM	6807	TPA÷32→ CNTR
SET COUNTER MODE 1 AND START	3	SCM1	6805	$\overline{\text{EF1}}$→ CNTR CLOCK
SET COUNTER MODE 2 AND START	3	SCM2	6803	$\overline{\text{EF2}}$→ CNTR CLOCK
SET PULSE WIDTH MODE 1 AND START	3	SPM1	6804	TPA.$\overline{\text{EF1}}$→ CNTR CLOCK; $\overline{\text{EF1}}$ ↗ STOPS COUNT
SET PULSE WIDTH MODE 2 AND START	3	SPM2	6802	TPA.EF2→ CNTR CLOCK; $\overline{\text{EF2}}$ ↗ STOPS COUNT
ENABLE TOGGLE Q	3	ETQ	6809[•]	IF CNTR = 01 • NEXT CNTR CLOCK ↗ : $\overline{\text{Q}}$→Q

[▲] This instruction is associated with more than one mnemonic Each mnemonic is individually listed.

[#] An IDLE instruction initiates an S1 cycle All external signals, except the oscillator, are stopped on the low-to-high transition of TPB. All outputs remain in their previous states, $\overline{\text{MRD}}$, $\overline{\text{MWR}}$, are set to a logic '1' and the data bus floats. The processor will continue to IDLE until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and the normal operation is resumed. (To respond to an INTERRUPT during an IDLE, MIE and either CIE or XIE must be enabled).

[•] ETQ cleared by LDC with the Counter/Timer stopped, reset of CPU or BCI • (CI = 1).

CI = Counter Interrupt, XI = External Interrupt.

CDP1804AC CDP1804AC

Table I — INSTRUCTION SUMMARY

INSTRUCTION	NO. OF MACHINE CYCLES	MNEMONIC	OP CODE	OPERATION
INTERRUPT CONTROL				
EXTERNAL INTERRUPT ENABLE	3	XIE	680A	1→XIE
EXTERNAL INTERRUPT DISABLE	3	XID	680B	0→XIE
COUNTER INTERRUPT ENABLE	3	CIE	680C	1→CIE
COUNTER INTERRUPT DISABLE	3	CID	680D	0→CIE
RETURN	2	RET	70	M(R(X))→X, P, R(X)+1→R(X), 1→MIE
DISABLE	2	DIS	71	M(R(X)→X, P, R(X)+1→R(X); 0→MIE
SAVE	2	SAV	78	T→M(R(X))
SAVE T, D, DF	6	DSAV	6876■	R(X)-1→R(X), T→M(R(X)), R(X)-1→R(X), D→M (R(X)), R(X)-1→R(X), SHIFT D RIGHT WITH CARRY, D→M(R(X))
INPUT-OUTPUT BYTE TRANSFER				
OUTPUT 1	2	OUT 1	61	M(R(X))→BUS, R(X)+1→R(X); N LINES = 1
OUTPUT 2	2	OUT 2	62	M(R(X))→BUS, R(X)+1→R(X); N LINES = 2
OUTPUT 3	2	OUT 3	63	M(R(X))→BUS, R(X)+1→R(X); N LINES = 3
OUTPUT 4	2	OUT 4	64	M(R(X))→BUS; R(X)+1→R(X); N LINES = 4
OUTPUT 5	2	OUT 5	65	M(R(X))→BUS, R(X)+1→R(X); N LINES = 5
OUTPUT 6	2	OUT 6	66	M(R(X))→BUS; R(X)+1→R(X), N LINES = 6
OUTPUT 7	2	OUT 7	67	M(R(X))→BUS, R(X)+1→R(X), N LINES = 7
INPUT 1	2	INP 1	69	BUS→M(R(X)), BUS→D, N LINES = 1
INPUT 2	2	INP 2	6A	BUS→M(R(X)); BUS→D, N LINES = 2
INPUT 3	2	INP 3	6B	BUS→M(R(X)), BUS→D; N LINES = 3
INPUT 4	2	INP 4	6C	BUS→M(R(X)), BUS→D, N LINES = 4
INPUT 5	2	INP 5	6D	BUS→M(R(X)), BUS→D, N LINES = 5
INPUT 6	2	INP 6	6E	BUS→M(R(X)), BUS→D, N LINES = 6
INPUT 7	2	INP 7	6F	BUS→M(R(X)), BUS→D, N LINES = 7
CALL AND RETURN				
STANDARD CALL	10	SCAL	688N■	R(N).0→M(R(X)), R(N) 1→M(R(X)-1), R(X)-2→R(X), R(P)→R(N), THEN M(R(N))→R(P) 1, M(R(N)+1)→R(P) 0, R(N)+2→R(N)
STANDARD RETURN	8	SRET	689N■	R(N)→R(P); M(R(X)+1)→R(N) 1; M(R(X)+2)→R(N).0; R(X)+2→R(X)

■Previous contents of T register are destroyed during instruction execution

NOTES FOR TABLE I

1. Long-Branch, Long-Skip and No Op instructions require three cycles to complete (1 fetch + 2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:
   a. Branch unconditionally
   b. Test for D=0 or D≠0
   c. Test for DF=0 or DF=1
   d. Test for Q=0 or Q=1
   e. Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

2. The short-branch instructions are two or three bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address, except for the branches on interrupt. For those, the first two bytes specify the condition to be tested and the third byte specifies the branching address.

   The short branch instruction can:
   a. Branch unconditionally
   b. Test for D=0 or D≠0
   c. Test for DF=0 or DF=1
   d. Test for Q=0 or Q=1
   e. Test the status (1 or 0) of the four EF flags
   f. Effect an unconditional no branch
   g. Test for counter or external interrupts (BCI, BXI)

   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

   The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

   They can:
   a. Skip unconditionally
   b. Test for D=0 or D≠0
   c. Test for DF=0 or DF=1
   d. Test for Q=0 or Q=1
   e. Test for MIE=1

   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

4. Instruction 6800 through 68FF take a minimum of 3 machine cycles and up to a maximum of 10 machine cycles. In all cases, the first two cycles are fetches and subsequent cycles are executes. The first byte (68) of these two-byte op codes is used to generate the second fetch, the second byte is then interpreted differently than the same code without the 68 prefix. DMA and INT requests are not serviced until the end of the last execute cycle.

5. Arithmetic Operations:
   The arithmetic and shift operations are the only instructions that can alter the content of DF. The syntax '(NOT DF)' denotes the subtraction of the borrow.
   Binary Operations:
   After an ADD instruction —
   DF=1 denotes a carry has occurred. Result is greater than FF_{16}.
   DF=0 denotes a carry has not occurred.
   After a SUBTRACT instruction —
   DF=1 denotes no borrow. D is a true positive number
   DF=0 denotes a borrow. D is in two's complement form.

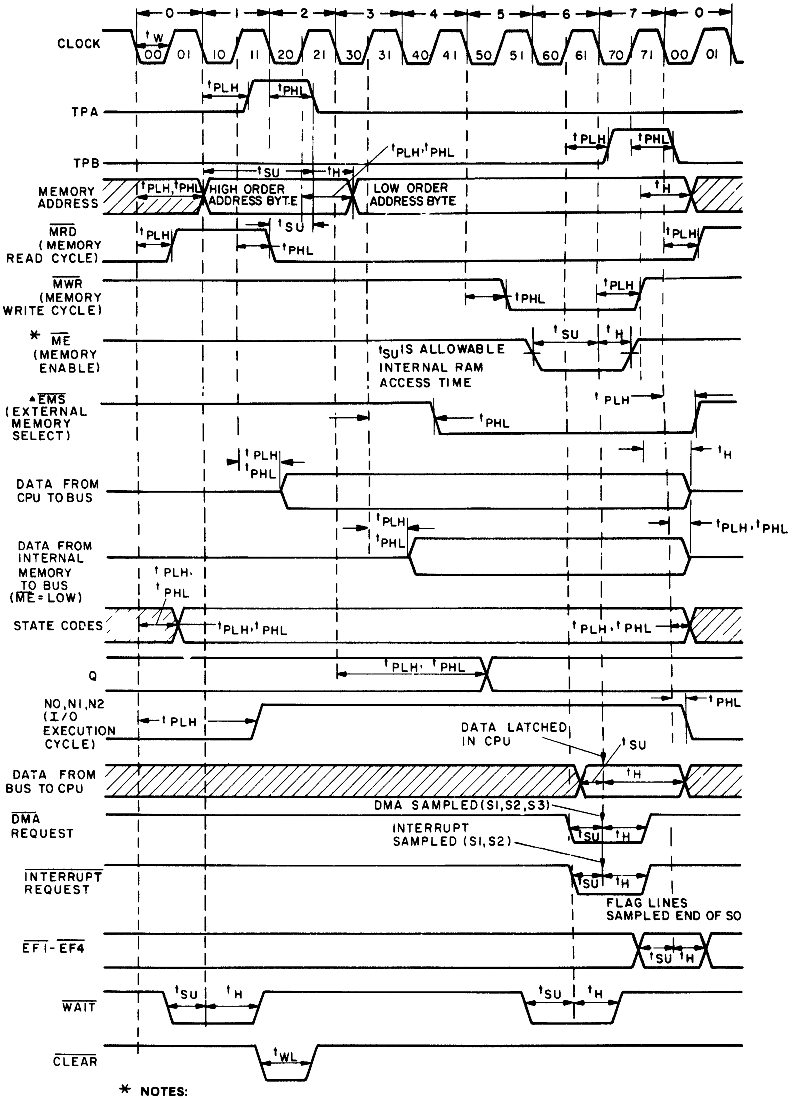
   Binary Coded Decimal Operations:
   After a BCD ADD instruction —
   DF=1 denotes a carry has occurred. Result is greater than 99_{10}.
   DF=0 denotes a carry has not occurred.
   After a BCD SUBTRACT instruction —
   DF=1 denotes no borrow. D is a true positive decimal number.

   (Example) 99 D
   -88 M(R(X))
   11 D DF=1

   DF=0 denotes a borrow. D is in ten's complement form.

   (Example) 88 D
   -99 M(R(X))
   89 D DF=0

   89 is the ten's complement of 11, which is the correct answer (with a minus value denoted by DF=0).



* NOTES:
1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE.
2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS
3. SHADED ARE AS INDICATED "DON'T CARE" OR UNDEFINED STATE. MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD.

•FOR THE RUN (RAM ONLY) MODE ONLY
▲ FOR THE RUN (RAM/ROM) MODE ONLY.

92CL-34986RI

Fig. 13 - Timing waveforms for CDP1805AC and CDP1806AC.

CDP1805AC, CDP1806AC

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C; C_L = 50 pF; Input t_r,t_f = 10 ns; Input Pulse Levels = 0.1 V to V_{DD}-0.1 V; V_{DD} = 5 V, ±5%.

CHARACTERISTIC		LIMITS		UNITS
		CDP1805AC, CDP1806AC		
		Typ.•	Max.	
Propagation Delay Times:				ns
Clock to TPA, TPB	t_{PLH}, t_{PHL}	150	275	
Clock-to-Memory High-Address Byte	t_{PLH}, t_{PHL}	325	550	
Clock-to-Memory Low-Address Byte	t_{PLH}, t_{PHL}	275	450	
Clock to $\overline{\text{MRD}}$	t_{PLH}, t_{PHL}	200	325	
Clock to $\overline{\text{MWR}}$	t_{PLH}, t_{PHL}	150	275	
Clock to (CPU DATA to BUS)	t_{PLH}, t_{PHL}	375	625	
Clock to State Code	t_{PLH}, t_{PHL}	225	400	
Clock to Q	t_{PLH}, t_{PHL}	250	425	
Clock to N	t_{PLH}, t_{PHL}	250	425	
Clock to Internal RAM Data to BUS	t_{PLH}, t_{PHL}	420	650	
Minimum Set Up and Hold Times:■				ns
Data Bus Input Set-Up	t_{SU}	-100	0	
Data Bus Input Hold	t_H	125	225	
$\overline{\text{DMA}}$ Set-Up	t_{SU}	-75	0	
$\overline{\text{DMA}}$ Hold	t_H	100	175	
$\overline{\text{ME}}$ Set-Up	t_{SU}	125	320	
$\overline{\text{ME}}$ Hold	t_H	0	50	
Interrupt Set-Up	t_{SU}	-100	0	
Interrupt Hold	t_H	100	175	
$\overline{\text{WAIT}}$ Set-Up	t_{SU}	20	50	
$\overline{\text{EF1-4}}$ Set-Up	t_{SU}	-125	0	
$\overline{\text{EF1-4}}$ Hold	t_H	175	300	
Minimum Pulse Width Times:■				ns
$\overline{\text{CLEAR}}$ Pulse Width	t_{WL}	100	175	
$\overline{\text{CLOCK}}$ Pulse Width	t_W	75	100	

•Typical values are for T_A = 25° C and nominal V_{DD}

■Maximum limits of minimum characteristics are the values above which all devices function

TIMING SPECIFICATIONS as a function of T (T = 1/f_{CLOCK}) at T_A = -40 to +85° C, V_{DD} = 5 V, ±5%.

CHARACTERISTIC		LIMITS		UNITS
		CDP1805AC, CDP1806AC		
		Min.	Typ.•	
High-Order Memory-Address Byte Set-Up to TPA ↘ Time	t_{SU}	2T-275	2T-175	ns
$\overline{\text{MRD}}$ to TPA ↘ Time	t_{SU}	T/2-100	T/2-75	
High-Order Memory-Address Byte Hold after TPA Time	t_H	T/2+75	T/2+100	
Low-Order Memory-Address Byte Hold after WR Time	t_H	T+180	T+240	
CPU Data to Bus Hold after WR Time	t_H	T+110	T+150	
Required Memory Access Time Address to Data	t_{ACC}	4.5T-440	4.5T-330	

•Typical values are for T_A = 25° C and nominal V_{DD}

CDP1805AC, CDP1806AC

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES
S1	RESET			0→Q,I,N, COUNTER PRESCALER, CIL; 1→CIE, XIE	00	UNDEFINED	1	1	0
	INITIALIZE NOT PROGRAMMER ACCESSIBLE			X, P→T THEN 0→X, P; 1→MIE, 0000→R0	00▲	UNDEFINED	1	1	0
S0		FETCH		MRP→I, N; RP+1→RP	MRP	RP	0	1	0
S1	0	0	IDL	STOP AT TPB WAIT FOR DMA OR INT	HIGH Z	RO	1	1	0
	0	1-F	LDN	MRN→D	MRN	RN	0	1	0
	1	0-F	INC	RN+1→RN	HIGH Z	RN	1	1	0
	2	0-F	DEC	RN-1→RN	HIGH Z	RN	1	1	0
	3	0-F	SHORT BRANCH	TAKEN: MRP→RP.0 NOT TAKEN: RP+1→RP	MRP	RP	0	1	0
	4	0-F	LDA	MRN→D; RN+1→RN	MRN	RN	0	1	0
	5	0-F	STR	D→MRN	D	RN	1	0	0
	6	0	IRX	RX+1→RX	MRX	RX	1	1	0
	6	1	OUT 1	MRX→BUS; RX+1→RX	MRX	RX	0	1	1
		2	OUT 2						2
		3	OUT 3						3
		4	OUT 4						4
		5	OUT 5						5
		6	OUT 6						6
		7	OUT 7						7
		9	INP 1	BUS→MRX, D	DATA FROM I/O DEVICE	RX	1	0	1
		A	INP 2						2
		B	INP 3						3
		C	INP 4						4
		D	INP 5						5
		E	INP 6						6
		F	INP 7						7
	7	0	RET	MRX→X,P; RX+1→RX 1→MIE	MRX	RX	0	1	0
		1	DIS	MRX→X,P; RX+1→RX 0→MIE	MRX	RX	0	1	0
		2	LDXA	MRX→D; RX+1→RX	MRX	RX	0	1	0
		3	STXD	D→MRX; RX-1→RX	D	RX	1	0	0
		4	ADC	MRX+D+DF→DF, D	MRX	RX	0	1	0
		5	SDB	MRX-D-DFN→DF, D	MRX	RX	0	1	0
		6	SHRC	LSB(D)→DF; DF→MSB(D)	HIGH Z	RX	1	1	0
		7	SMB	D-MRX-DFN→DF, D	MRX	RX	0	1	0
		8	SAV	T→MRX	T	RX	1	0	0
		9	MARK	X,P→T, MR2; P→X R2-1→R2	T	R2	1	0	0
		A	REQ	0→Q	HIGH Z	RP	1	1	0
		B	SEQ	1→Q	HIGH Z	RP	1	1	0
		C	ADCI	MRP+D+DF→DF, D; RP+1	MRP	RP	0	1	0
		D	SDBI	MRP-D-DFN→DF, D; RP+1	MRP	RP	0	1	0
		E	SHLC	MSB(D)→DF; DF→LSB(D)	HIGH Z	RP	1	1	0
		F	SMBI	D-MRP-DFN→DF, D; RP+1	MRP	RP	0	1	0
	8	0-F	GLO	RN.0→D	RN.0	RN	1	1	0
	9	0-F	GHI	RN.1→D	RN.1	RN	1	1	0
	A	0-F	PLO	D→RN.0	D	RN	1	1	0
	B	0-F	PHI	D→RN.1	D	RN	1	1	0

▲ = Data bus floats for first 2-1/2 clocks of the 9 clock initialization cycle; all zeros for remainder of cycle

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES
S1#1	C	0-3, 8-B	LONG BRANCH	TAKEN: MRP→B; RP+1→RP	MRP	RP	0	1	0
#2				TAKEN:B→RP.1;MRP→RP.0	M(RP+1)	RP+1	0	1	0
S1#1				NOT TAKEN RP+1→RP	MRP	RP	0	1	0
#2				NOT TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0
S1#1		5 6 7 C D E F	LONG SKIP	TAKEN: RP+1→RP	MRP	RP	0	1	0
#2				TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0
S1#1				NOT TAKEN: NO OPERATION	MRP	RP	0	1	0
#2				NOT TAKEN: NO OPERATION	M(RP+1)	RP+1	0	1	0
S1#1		4	NOP	NO OPERATION	MRP	RP	0	1	0
#2				NO OPERATION	M(RP+1)	RP+1	0	1	0
S1	D	0-F	SEP	N→P	NN	RN	1	1	0
	E	0-F	SEX	N→X	NN	RN	1	1	0
	F	0	LDX	MRX→D	MRX	RX	0	1	0
		1	OR	MRX OR D→D	MRX	RX	0	1	0
		2	AND	MRX AND D→D					
		3	XOR	MRX XOR D→D					
		4	ADD	MRX+D→DF, D					
		5	SD	MRX-D→DF, D					
		7	SM	D-MRX→DF; D					
		6	SHR	LSB(D)→DF; 0→MSB(D)	HIGH Z	RX	1	1	0
		8	LDI	MRP→D; RP+1→RP	MRP	RP	0	1	0
		9	ORI	MRP OR D→D; RP+1→RP					
		A	ANI	MRP AND D→D; RP+1→RP					
		B	XRI	MRP XOR D→D; RP+1→RP					
		C	ADI	MRP+D→DF, D; RP+1→RP					
		D	SDI	MRP-D→DF, D; RP+1→RP					
		F	SMI	D-MRP→DF, D; RP+1→RP					
		E	SHL	MSB(D)→DF; 0→LSB(D)	HIGH Z	RP	1	1	0
S2	DMA IN			BUS→MR0; R0+1→R0	DATA FROM I/O DEVICE	R0	1	0	0
	DMA OUT			MR0→BUS; R0+1→R0	MR0	R0	0	1	0
S3	INTERRUPT			X,P→T; 0→MIE 1→P; 2→X	HIGH Z	RN	1	1	0

CDP1805AC, CDP1806AC

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES (Cont'd)

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	N LINES
THE FOLLOWING ARE ALL LINKED INSTRUCTIONS “68” PRECEDES ALL THE OP CODES, SO THERE IS A DOUBLE FETCH									
S1	0	0	STPC	STOP COUNTER CLOCK; 0→÷32 PRESCALER	HIGH Z	R0	1	1	0
		1	DTC	CNTR-1→CNTR	HIGH Z	R1	1	1	0
		2	SPM2	CNTR-1 ON EF2 AND TPA	HIGH Z	R2	1	1	0
		3	SCM2	CNTR-1 ON EF2 0 TO 1	HIGH Z	R3	1	1	0
		4	SPM1	CNTR-1 ON EF1 AND TPA	HIGH Z	R4	1	1	0
		5	SCM1	CNTR-1 ON EF1 0 TO 1	HIGH Z	R5	1	1	0
		6	LDC	CNTR STOPPED D→CH, CNTR; 0→CI CNTR RUNNING D→CH	D	R6	1	1	0
		7	STM	CNTR-1 ON TPA÷32	HIGH Z	R7	1	1	0
		8	GEC	CNTR→D	CNTR	R8	1	1	0
		9	ETQ	IF CNTR THRU 0: $\overline{Q}$→Q	HIGH Z	R9	1	1	0
		A	XIE	1→XIE	HIGH Z	RA	1	1	0
		B	XID	0→XIE	HIGH Z	RB	1	1	0
		C	CIE	1→CIE	HIGH Z	RC	1	1	0
		D	CID	0→CIE	HIGH Z	RD	1	1	0
S1#1	2	0-F	DBNZ	RN-1→RN	HIGH Z	RN	1	1	0
#2				MRP→B; RP+1→RP	MRP	RP	0	1	0
#3				TAKEN: B→RP.1, MRP→RP.0 NOT TAKEN: RP+1→RP	M(RP+1)	RP+1	0	1	0
S1	3	E	BCI	TAKEN: MRP→RP 0, 0→CI NOT TAKEN: RP+1→RP	MRP	RP	0	1	0
		F	BXI	TAKEN: MRP→RP.0 NOT TAKEN· RP+1→RP	MRP	RP	0	1	0
S1#1	6	0-F	RLXA	MRX→B, RX+1→RX	MRX	RX	0	1	0
#2				B→T; MRX→B; RX+1→RX	M(RX+1)	RX+1	0	1	0
#3				B, T→RN 0, RN.1	HIGH Z	RN	1	1	0
S1#1	7	4	DADC	MRX+D+DF→DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP	1	1	1
S1#1	7	6	DSAV	RX-1→RX	HIGH Z	RX	1	1	0
#2				T→MRX; RX-1→RX	T	RX-1	1	0	0
#3				D→MRX, RX-1→RX SHIFT D RIGHT WITH CARRY	D	RX-2	1	0	0
#4				D→MRX	D	RX-3	1	0	0
S1#1	7	7	DSMB	D-MRX-(NOT DF)→DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP	1	1	0
S1#1	7	C	DACI	MRP+D+DF→DF, D; RP+1→RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP+1	1	1	0
S1#1	7	F	DSBI	D-MRP-(NOT DF)→DF, D, RP+1→RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP+1	1	1	0
S1#1	8	0-F	SCAL	RN.0, RN.1→T, B	HIGH Z	RN	1	1	0
#2				T→MRX; RX-1→RX	RN.0	RX	1	0	0
#3				B→MRX, RX-1→RX	RN.1	RX-1	1	0	0
#4				RP.0, RP.1→T, B	HIGH Z	RP	1	1	0
#5				B, T→RN.1, RN.0	HIGH Z	RN	1	1	0
#6				MRN→B; RN+1→RN	MRP	RP	0	1	0
#7				B→T; MRN→B; RN+1→RN	M(RP+1)	RP+1	0	1	0
#8				B, T→RP.0, RP 1	HIGH Z	RP	1	1	0

CDP1805AC, CDP1806AC

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	$\overline{MWR}$	N LINES
THE FOLLOWING ARE ALL LINKED INSTRUCTIONS "68" PRECEDES ALL THE OP CODES, SO THERE IS A DOUBLE FETCH									
S1#1	9	0-F	SRET	RN.0, RN.1→T, B	HIGH Z	RN	1	1	0
#2				RX+1→RX	HIGH Z	RX	1	1	0
#3				B, T→RP.1, RP.0	HIGH Z	RP	1	1	0
#4				MRX→B; RX+1→RX	M(RX+1)	RX+1	0	1	0
#5				B→T; MRX→B	M(RX+1)	RX+2	0	1	0
#6				B, T→RN.0, RN.1	HIGH Z	RN	1	1	0
S1#1	A	0-F	RSXD	RN.0, RN.1→T, B	HIGH Z	RN	1	1	0
#2				T→MRX; RX-1→RX	RN.0	RX	1	0	0
#3				B→MRX; RX-1→RX	RN.1	RX-1	1	0	0
S1#1	B	0-F	RNX	RN 0, RN 1→T, B	HIGH Z	RN	1	1	0
#2				B, T→RX.1, RX.0	HIGH Z	RX	1	1	0
S1#1	C	0-F	RLDI	MRP→B; RP+1→RP	MRP	RP	0	1	0
#2				B→T; MRP→B; RP+1→RP	M(RP+1)	RP+1	0	1	0
#3				B, T→RN.0, RN.1; RP+1→RP	HIGH Z	RN	1	1	0
S1#1	F	4	DADD	MRX+D→DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP	1	1	0
S1#1	F	7	DSM	D-MRX→DF, D	MRX	RX	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP	1	1	0
S1#1	F	C	DADI	MRP+D→DF, D; RP+1→RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP+1	1	1	0
S1#1	F	F	DSM!	D-MRP→DF, D RP+1→RP	MRP	RP	0	1	0
#2				DECIMAL ADJUST→DF, D	HIGH Z	RP+1	1	1	0

CDP1805AC, CDP1806AC

Instruction Summary

N

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	IDL	LDN														
1	INC															
2	DEC															
3	BR	BQ	BZ	BDF	B1	B2	B3	B4	SKP	BNQ	BNZ	BNF	BN1	BN2	BN3	BN4
4	LDA															
5	STR															
6	IRX	OUT							*	INP						
7	RET	DIS	LDXA	STXD	ADC	SDB	SHRC	SMB	SAV	MARK	REQ	SEQ	ADCI	SDBI	SHLC	SMBI
8	GLO															
9	GHI															
A	PLO															
B	PHI															
C	LBR	LBQ	LBZ	LBDF	NOP	LSNQ	LSNZ	LSNF	LSKP	LBNQ	LBNZ	LBNF	LSIE	LSQ	LSZ	LSDF
D	SEP															
E	SEX															
F	LDX	OR	AND	XOR	ADD	SD	SHR	SM	LDI	ORI	ANI	XRI	ADI	SDI	SHL	SMI
	'68' LINKED OPCODES (DOUBLE FETCH)															
0	STPC	DTC	SPM2	SCM2	SPM1	SCM1	LDC	STM	GEC	ETQ	XIE	XID	CIE	CID	—	—
2	DBNZ															
3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BCI	BXI
6	RLXA															
7	—	—	—	—	DADC	—	DSAV	DSMB	—	—	—	—	DACI	—	—	DSBI
8	SCAL															
9	SRET															
A	RSXD															
B	RNX															
C	RLDI															
F	—	—	—	—	DADD	—	—	DSM	—	—	—	—	DADI	—	—	DSMI

* '68' IS USED AS A LINKING OPCODE FOR THE DOUBLE FETCH INSTRUCTIONS.

6805-Series Microprocessors and Microcomputers

Technical Data

Comparison of RCA CMOS CDP6805 Family Microprocessors and Microcomputers

Features	CDP6805E2 CDP6805E2C#	CDP6805E3 CDP6805E3C#	CDP6805F2 CDP6805F2C#	CDP6805G2 CDP6805G2C#	CDP68HC05D2°	CDP68HC05D2A°	CDP68HC05C4°	CDP68HC05C8°
Memory Addressing (Bytes)	8k	64k	—	—	—	—	—	—
On-Chip RAM (Bytes)	112	112	64	112	96	96	176	176
On-Chip ROM (Bytes)	—	—	1089	2106	2176	2176	4160	7744
Max. Clock Frequency (MHz)	5.0	5.0	4.0	4.0	4.2	4.2	4.2	4.2
Instruction Time Min./Max.(μs)	2.0/10.0	2.0/10.00	2.0/10.00	2.0/10.00	0.95/5.23	0.95/5.23	0.95/5.23	0.95/5.23
Timer/Counter Bits	8	8	8	8	16	16	16	16
Prescalers	Program	Program	Program	Program	÷ 4	÷ 4	÷ 4	÷ 4
Bus Structure	Multiplexed Address/Data		—	—	—	—	—	—
Interrupts	V	V	V	V	V	V	V	V
Latched I/O Lines	16	13	16	32	28	16	24	24
Max. Operating Temp. Range (°C)	0 to + 70	0 to + 70	0 to + 70	0 to + 70	-40 to + 125	-40 to + 125	-40 to + 125	-40 to + 125
Package No. of Pins	40 D, E 44 Q	40 D, E 44 Q	28 D, E 28 Q	40 D, E —	40 D, E 44 Q	28 E 28 Q	40 D, E 44 Q	40 D, E 44 Q
Serial Interface	—	—	—	—	SPI	—	SPI/SCI	SPI/SCI

V = Vectored address °Multiply instruction in the CDP68HC05C4, CDP68HC05C8, and CDP68HC05D2

# "C" Version has -40 to +85°C operating temperature range.

CDP68HC05C4, CDP68HC05C8

HCMOS Microcomputers

SECTION 1
INTRODUCTION

1.1 GENERAL

The CDP68HC05C4 HCMOS Microcomputer is a member of the CDP68HC05 Family of low-cost single-chip microcomputers. This 8-bit microcomputer contains an on-chip oscillator, CPU, RAM, ROM, I/O, two serial interface systems, and timer. The fully static design allows operation at frequencies down to dc, further reducing its already low-power consumption.

The CDP68HC05C8 Microcomputer (MCU) device is similar to the CDP68HC05C4 MCU with one exception. This exception incorporates 3584 additional bytes of user ROM for a total of 7744 bytes of on-chip user ROM. All information on the CDP68HC05C4 MCU applies to the CDP68HC05C8 MCU with the exception of the memory description.

1.2 FEATURES

The following are some of the hardware and software highlights of these HCMOS Microcomputers.

HARDWARE FEATURES

- HCMOS Technology
- 8-Bit Architecture
- Power-Saving Stop and Wait Modes
- Fully Static Operation
- 176 Bytes of On-Chip RAM
- 4160 Bytes of On-Chip ROM (CDP68HC05C4)
  7744 Bytes of On-Chip ROM (CDP68HC05C8)
- 24 Bidirectional I/O Lines
- 2.1-MHz Internal Operating Frequency at 5 Volts; 1 MHz at 3 Volts
- Internal 16-Bit Timer Similar to MC6801 Timer
- Serial Communications Interface System
- Serial Peripheral Interface System
- Self-Check Mode
- External, Timer, Serial Communications Interface, and Serial Peripheral Interface Interrupts
- Master Reset and Power-On Reset
- Single 3- to 6-Volt Supply (2-V Data Retention Mode)
- On-Chip Oscillator with RC or Crystal Mask Options
- 40-Pin Dual-In-Line Package
- 44-Lead Plastic Chip Carrier Also Available

TSM-203A

CDP68HC05C4, CDP68HC05C8

SOFTWARE FEATURES

- Similar to MC6800
- 8 x 8 Unsigned Multiply Instruction
- Efficient Use of Program Space
- Versatile Interrupt Handling
- True Bit Manipulation
- Addressing Modes with Indexed Addressing for Tables
- Efficient Instruction Set
- Memory Mapped I/O
- Two Power-Saving Standby Modes
- Upward Software Compatible with the CDP6805 CMOS Family

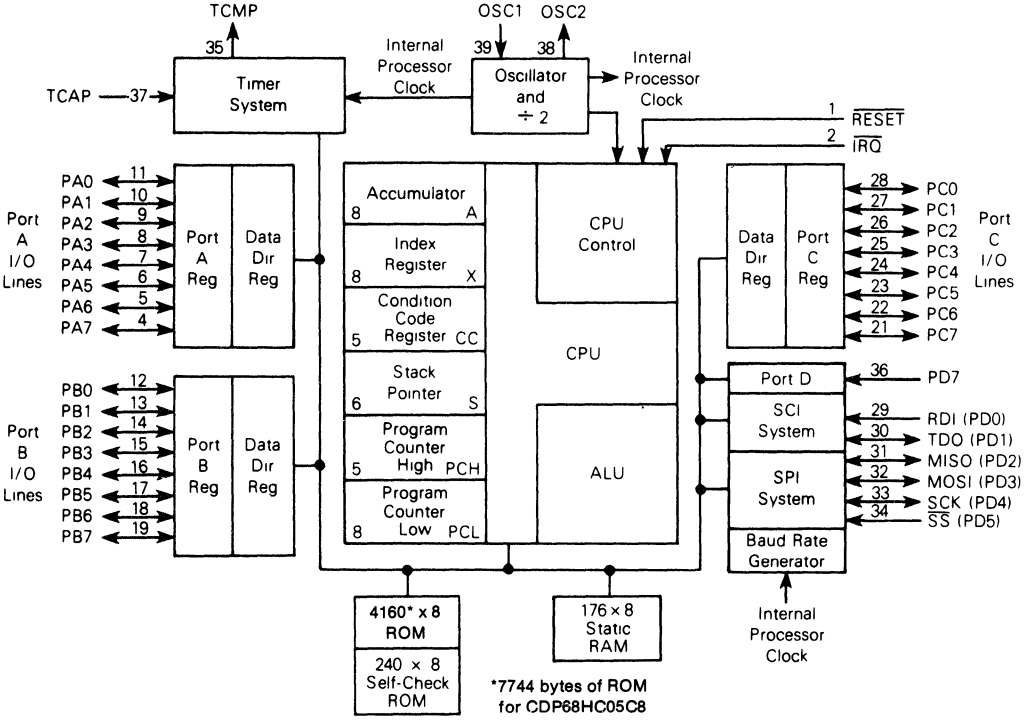


Figure 1-1. Microcomputer Block Diagram

SECTION 2
FUNCTIONAL PIN DESCRIPTION, INPUT/OUTPUT PROGRAMMING, MEMORY, CPU REGISTERS, AND SELF-CHECK

This section provides a description of the functional pins, input/output programming, memory, CPU registers, and self-check.

2.1 FUNCTIONAL PIN DESCRIPTION

2.1.1 V_{DD} and V_{SS}

Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is ground.

2.1.2 $\overline{\text{IRQ}}$ (Maskable Interrupt Request)

$\overline{\text{IRQ}}$ is a programmable option which provides two different choices of interrupt triggering sensitivity. These options are: 1) negative edge-sensitive triggering only, or 2) both negative edge-sensitive and level-sensitive triggering. In the latter case, either type of input to the $\overline{\text{IRQ}}$ pin will produce the interrupt. The MCU completes the current instruction before it responds to the interrupt request. When the $\overline{\text{IRQ}}$ pin goes low for at least on t_{ILIH}, a logic one is latched internally to signify an interrupt has been requested. When the MCU completes its current instruction, the interrupt latch is tested. If the interrupt latch contains a logic one, and the interrupt mask bit (I bit) in the condition code register is clear, the MCU then begins the interrupt sequence.

If the option is selected to include level-sensitive triggering, then the $\overline{\text{IRQ}}$ input requires an external resistor to V_{DD} for "wire-OR" operation. See **INTERRUPTS** in Section 3 for more detail concerning interrupts.

2.1.3 $\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ input is not required for startup but can be used to reset the MCU internal state and provide an orderly software startup procedure. Refer to **RESETS** in Section 3 for a detailed description.

2.1.4 TCAP

The TCAP input controls the input capture feature for the on-chip programmable timer system. Refer to **INPUT CAPTURE REGISTER** in Section 4 for additional information.

2.1.5 TCMP

The TCMP pin (35) provides an output for the output compare feature of the on-chip timer system. Refer to **OUTPUT COMPARE REGISTER** in Section 4 for additional information.

CDP68HC05C4, CDP68HC05C8

2.1.6 OSC1, OSC2

The CDP68HC05C4 and CDP68HC05C8 can be configured to accept either a crystal input or an RC network to control the internal oscillator. The internal clocks are derived by a divide-by-two of the internal oscillator frequency (f_{OSC}).

2.1.6.1. CRYSTAL. The circuit shown in Figure 2-1(b) is recommended when using a crystal. The internal oscillator is designed to interface with an AT-cut parallel resonant quartz-crystal resonator in the frequency range specified for f_{OSC} in 9.7 or 9.8 Control Timing. Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and startup stabilization time. Refer to 9.5 or 9.6 for V_{DD} specifications.

2.1.6.2 CERAMIC RESONATOR. A ceramic resonator may be used in place of the crystal in cost-sensitive applications. The circuit in Figure 2-1(b) is recommended when using a ceramic resonator. Figure 2-1(a) lists the recommended capacitance and feedback resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

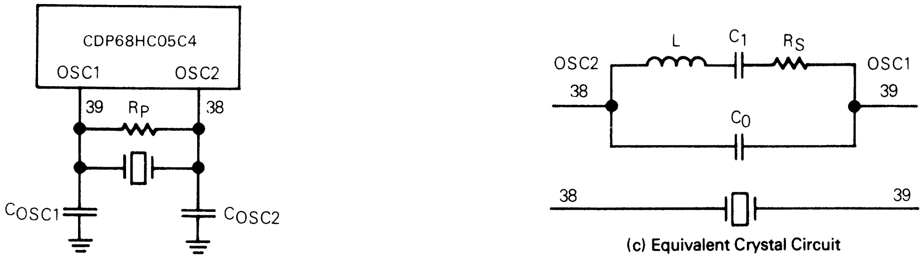
Crystal

	2 MHz	4 MHz	Units
R_{SMAX}	400	75	Ω
C_0	5	7	pF
C_1	0.008	0 012	µF
C_{OSC1}	15-40	15-30	pF
C_{OSC2}	15-30	15-25	pF
R_P	10	10	MΩ
Q	30	40	K

Ceramic Resonator

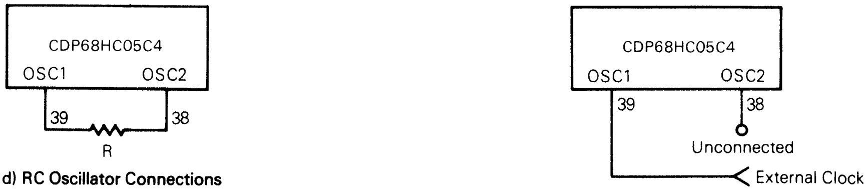
	2-4 MHz	Units
RS (typical)	10	Ω
C_0	40	pF
C_1	4.3	pF
C_{OSC1}	30	pF
C_{OSC2}	30	pF
R_P	1-10	MΩ
Q	1250	—

(a) Crystal/Ceramic Resonator Parameters



(b) Crystal Oscillator Connections

(c) Equivalent Crystal Circuit



(d) RC Oscillator Connections

(e) External Clock Source Connections

Figure 2-1. Oscillator Connections

2.1.6.3 RC. If the RC oscillator option is selected, then a resistor is connected to the oscillator pins as shown in Figure 2-1(d).

2.1.6.4 EXTERNAL CLOCK. An external clock should be applied to the OSC1 input with the OSC2 input not connected, as shown in Figure 2-1(e). An external clock may be used with either the RC or crystal oscillator option. The t_{OXOV} or t_{ILCH} specifications do not apply when using an external clock input. The equivalent specification of the external clock source should be used in lieu of t_{OXOV} or t_{ILCH}.

2.1.7 PA0-PA7

These eight I/O lines comprise port A. The state of any pin is software programmable and all port A lines are configured as input during power-on or reset. Refer to **INPUT/OUTPUT PROGRAMMING** paragraph below for a detailed description of I/O programming.

2.1.8 PB0-PB7

These eight lines comprise port B. The state of any pin is software programmable and all port B lines are configured as input during power-on or reset. Refer to **INPUT/OUTPUT PROGRAMMING** paragraph below for a detailed description of I/O programming.

2.1.9 PC0-PC7

These eight lines comprise port C. The state of any pin is software programmable and all port C lines are configured as input during power-on or reset. Refer to **INPUT/OUTPUT PROGRAMMING** paragraph below for a detailed description of I/O programming.

2.1.10 PD0-PD5, PD7

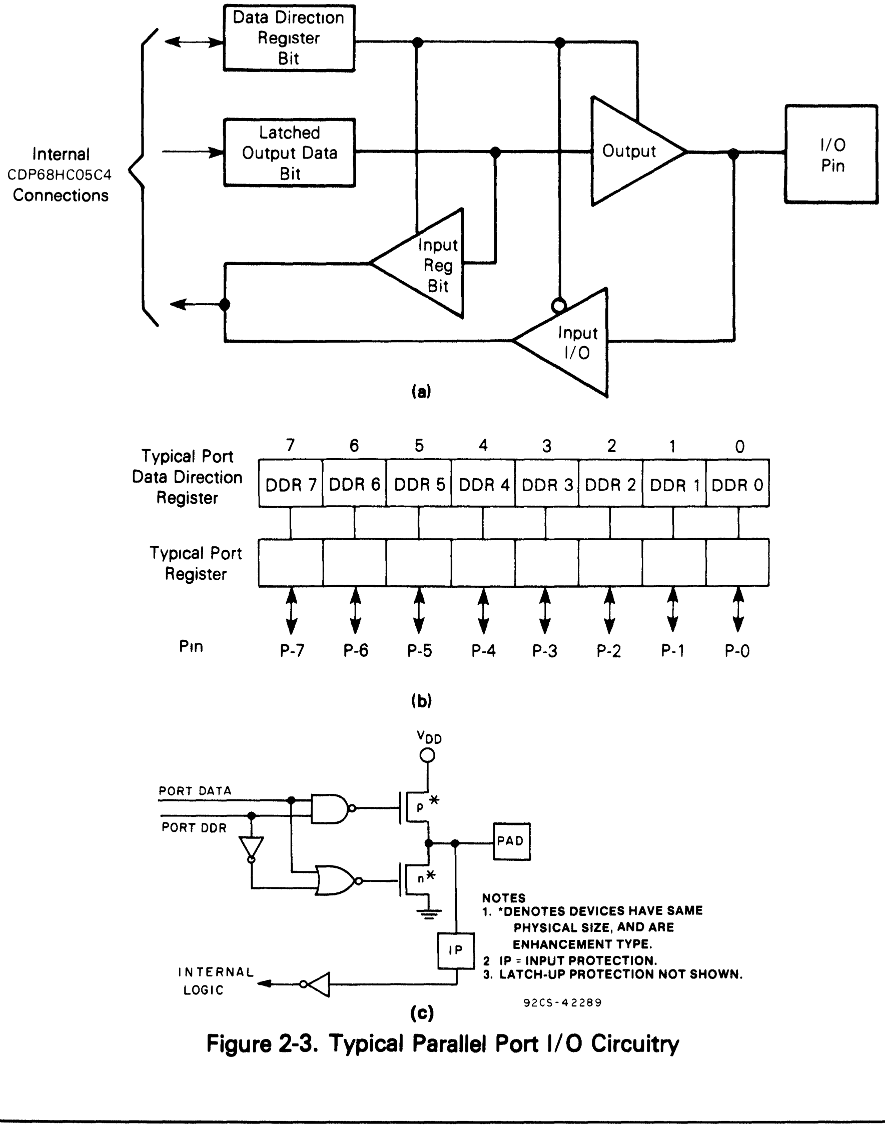
These seven lines comprise port D, a fixed input port that is enabled during power-on. All enabled special functions (SPI and SCI) affect the pins on this port. Four of these lines, PD2/MISO, PD3/MOSI, PD4/SCK, and PD5/$\overline{SS}$, are used in the serial peripheral interface (SPI) discussed in Section 6. Two of these lines, PD0/RDI and PD1/TDO, are used in the serial communications interface (SCI) discussed in Section 5. Refer to **2.2 INPUT/OUTPUT PROGRAMMING** for a detailed description of I/O programming.

CDP68HC05C4, CDP68HC05C8

2.2 INPUT/OUTPUT PROGRAMMING

2.2.1 Parallel Ports

Ports A, B, and C may be programmed as an input or an output under software control. The direction of the pins is determined by the state of the corresponding bit in the port data direction register (DDR). Each 8-bit port has an associated 8-bit data direction register. Any port A, port B, or port C pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared to a logic zero. At power-on or reset, all DDRs are cleared, which configure all port A, B, and C pins as inputs. The data direction registers are capable of being written to or read by the processor. Refer to Figure 2-3 and Table 2-1. During the programmed output state, a read of the data register actually reads the value of the output data latch and not the I/O pin.


Data Direction Register Bit
Latched Output Data Bit
Internal CDP68HC05C4 Connections
Output
I/O Pin
Input Reg Bit
Input I/O
Typical Port Data Direction Register
7 6 5 4 3 2 1 0
DDR 7 DDR 6 DDR 5 DDR 4 DDR 3 DDR 2 DDR 1 DDR 0
Typical Port Register
Pin
P-7 P-6 P-5 P-4 P-3 P-2 P-1 P-0
VDD
PORT DATA
PORT DDR
p*
n*
PAD
IP
INTERNAL LOGIC
92CS-42289

(a)

(b)

(c)

NOTES
1. *DENOTES DEVICES HAVE SAME PHYSICAL SIZE, AND ARE ENHANCEMENT TYPE.
2 IP = INPUT PROTECTION.
3. LATCH-UP PROTECTION NOT SHOWN.

Figure 2-3. Typical Parallel Port I/O Circuitry

Table 2-1. I/O Pin Functions

R/$\overline{W}$*	DDR	I/O Pin Function
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read

*R/$\overline{W}$ is an internal signal

2.2.2 Fixed Port

Port D is a 7-bit fixed input port (PD0-PD5, PD7) that continually monitors the external pins whenever the SPI or SCI systems are disabled. During power-on reset or external reset all seven bits become valid input ports because all special function output drivers are disabled. For example, with the serial communications interface (SCI) system enabled, (RE=TE=1) PD0 and PD1 inputs will read zero. With the serial peripheral interface (SPI) system disabled (SPE=0) PD2 through PD5 will read the state of the pin at the time of the read operation. No data register is associated with the port when it is used as an input.

NOTE

It is recommended that all unused inputs, except OSC2, and I/O ports (configured as inputs) be tied to an appropriate logic level (e.g. either V_{DD} or V_{SS}).

2.2.3 Serial Port (SCI and SPI)

The serial communications interface (SCI) and serial peripheral interface (SPI) use the port D pins for their functions. The SCI function requires two of the pins (PD0-PD1) for its receive data input (RDI) and transmit data output (TDO) respectively, whereas the SPI function requires four of the pins (PD2-PD5) for its serial data input/output (MISO), serial data output/input (MOSI), system clock (SCK), and slave select ($\overline{SS}$) respectively. Refer to **SECTION 5 SERIAL COMMUNICATIONS INTERFACE** and **SECTION 6 SERIAL PERIPHERAL INTERFACE** for a more detailed discussion.

2.3 MEMORY

As shown in Figure 2-4, the MCU is capable of addressing 8192 bytes of memory and I/O registers with its program counter. The CDP68HC05C4 MCU has implemented 4601 bytes of these locations. The first 256 bytes of memory (page zero) include: 25 bytes of I/O features such as data ports, the port DDRs, timer, serial peripheral interface (SPI), and serial communication interface (SCI); 48 bytes of user ROM, and 176 bytes of RAM. The next 4096 bytes complete the user ROM. The self-check ROM (224 bytes) and self-check vectors (16 bytes) are contained in memory locations $1F00 through $1FEF. The 16 highest address bytes contain the user defined reset and the interrupt vectors. Seven bytes of the lowest 32 memory locations are unused and the 176 bytes of user RAM include up to 64 bytes for the stack. Since most programs use only a small part of the allocated stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are usable for program data storage. Figure 2-5 illustrates the CDP68HC05C8 memory map.

CDP68HC05C4, CDP68HC05C8

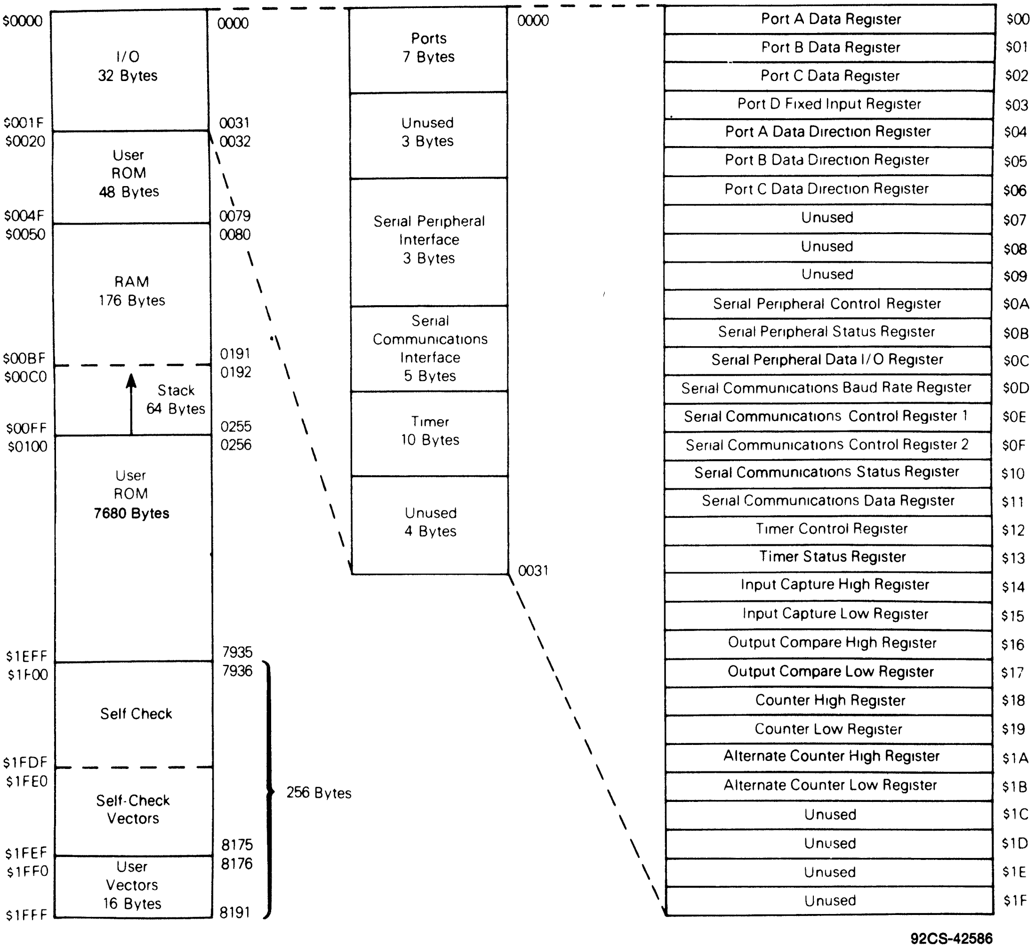


Figure 2-5. CDP68HC05C8 Address Map.

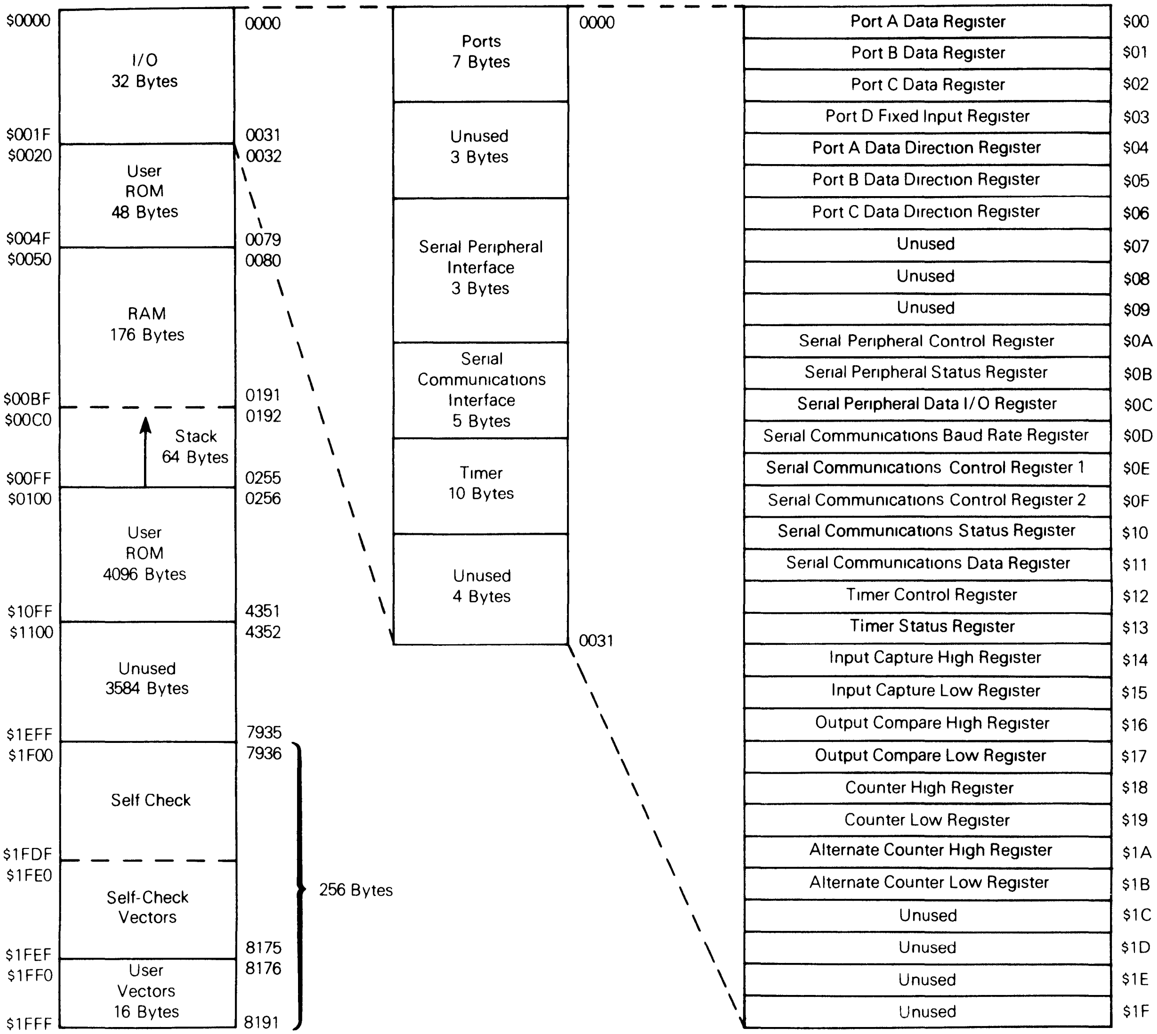


Figure 2-4. CDP68HC05C4 Address Map.

CDP68HC05C4, CDP68HC05C8

2.4 CPU REGISTERS

The CPU contains five registers, as shown in the programming model of Figure 2-5. The interrupt stacking order is shown in Figure 2-6.

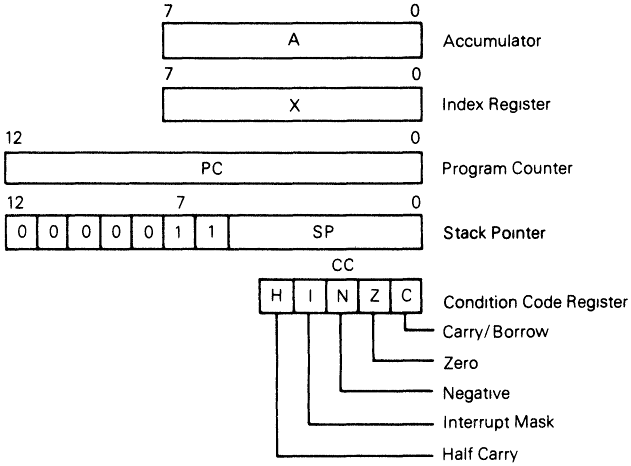
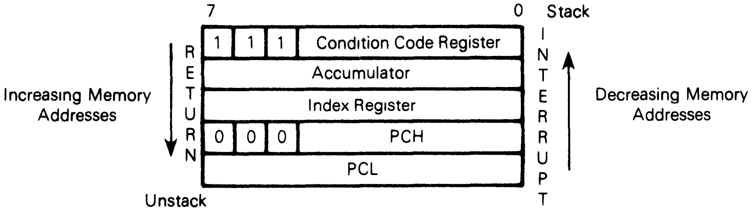


Figure 2-5. Programming Model


7
0
Stack
1 1 1 Condition Code Register
Accumulator
Index Register
0 0 0 PCH
PCL
Increasing Memory Addresses
RETURN
Unstack
INTERRUPT
Decreasing Memory Addresses

NOTE. Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc Pulling from the stack is in the reverse order.

Figure 2-6. Stacking Order

2.4.1 Accumulator (A)

The accumulator is an 8-bit general purpose register used to hold operands, results of the arithmetic calculations, and data manipulations.

2.4.2 Index Register (X)

The X register is an 8-bit register which is used during the indexed modes of addressing. It provides an 8-bit value which is used to create an effective address. The index register is also used for data manipulations with the read-modify-write type of instructions and as a temporary storage register when not performing addressing operations.

2.4.3 Program Counter (PC)

The program counter is a 13-bit register that contains the address of the next instruction to be executed by the processor.

2.4.4 Stack Pointer (SP)

The stack pointer is a 13-bit register containing the address of the next free locations on the push-down/pop-up stack. When accessing memory, the seven most significant bits are permanently configured to 0000011. These seven bits are appended to the six least significant register bits to produce an address within the range of $00FF to $00C0. The stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts. During external or power-on reset, and during a reset stack pointer (RSP) instruction, the stack pointer is set to its upper limit ($00FF). Nested interrupt and/or subroutines may use up to 64 (decimal) locations. When the 64 locations are exceeded, the stack pointer wraps around and points to its upper limit ($00FF), thus, losing the previously stored information. A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five RAM bytes.

2.4.5 Condition Code Register (CC)

The condition code register is a 5-bit register which indicates the results of the instruction just executed as well as the state of the processor. These bits can be individually tested by a program and specified action taken as a result of their state. Each bit is explained in the following paragraphs.

2.4.5.1 HALF CARRY BIT (H). The H bit is set to a one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H bit is useful in binary coded decimal subroutines.

2.4.5.2 INTERRUPT MASK BIT (I). When the I bit is set, all interrupts are disabled. Clearing this bit enables the interrupts. If an external interrupt occurs while the I bit is set, the interrupt is latched and is processed after the I bit is next cleared; therefore, no interrupts are lost because of the I bit being set. An internal interrupt can be lost if it is cleared while the I bit is set (refer to **SECTION 4 PROGRAMMABLE TIMER, SECTION 5 SERIAL COMMUNICATIONS INTERFACE,** and **SECTION 6 SERIAL PERIPHERAL INTERFACE** for more information).

2.4.5.3 NEGATIVE (N). When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation is negative (bit 7 in the result is a logic one).

2.4.5.4 ZERO (Z). When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation is zero.

2.4.5.5 CARRY/BORROW (C). Indicates that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts, and rotates.

2.5 SELF-CHECK

The self-check capability of the CDP68HC05C4 MCU provides an internal check to determine if the device is functional. Self-check is performed using the circuit shown in the schematic diagram of Figure 2-7. As shown in the diagram, port C pins PC0-PC3 are monitored (light emitting diodes are shown but other devices could be used) for the self-check results. The self-check mode is entered by applying a 9 Vdc input (through a 4.7 kilohm resistor) to the $\overline{\text{IRQ}}$ pin (2) and 5 Vdc input (through a 4.7 kilohm resistor) to the TCAP pin (37) and then depressing the reset switch to execute a reset. After reset, the following seven tests are performed automatically:

I/O — Functionally exercises ports A, B, and C
RAM — Counter test for each RAM byte
Timer — Tracks counter register and checks OCF flag
SCI — Transmission Test; checks for RDRF, TDRE, TC, and FE flags
ROM — Exclusive OR with odd ones parity result
SPI — Transmission test with check for SPIF, WCOL, and MODF flags
INTERRUPTS — Tests external, timer, SCI, and SPI interrupts.

Self-check results (using the LEDs as monitors) are shown in Table 2-2. The following subroutines are available to user programs and do not require any external hardware.

2.6 TIMER TEST SUBROUTINE

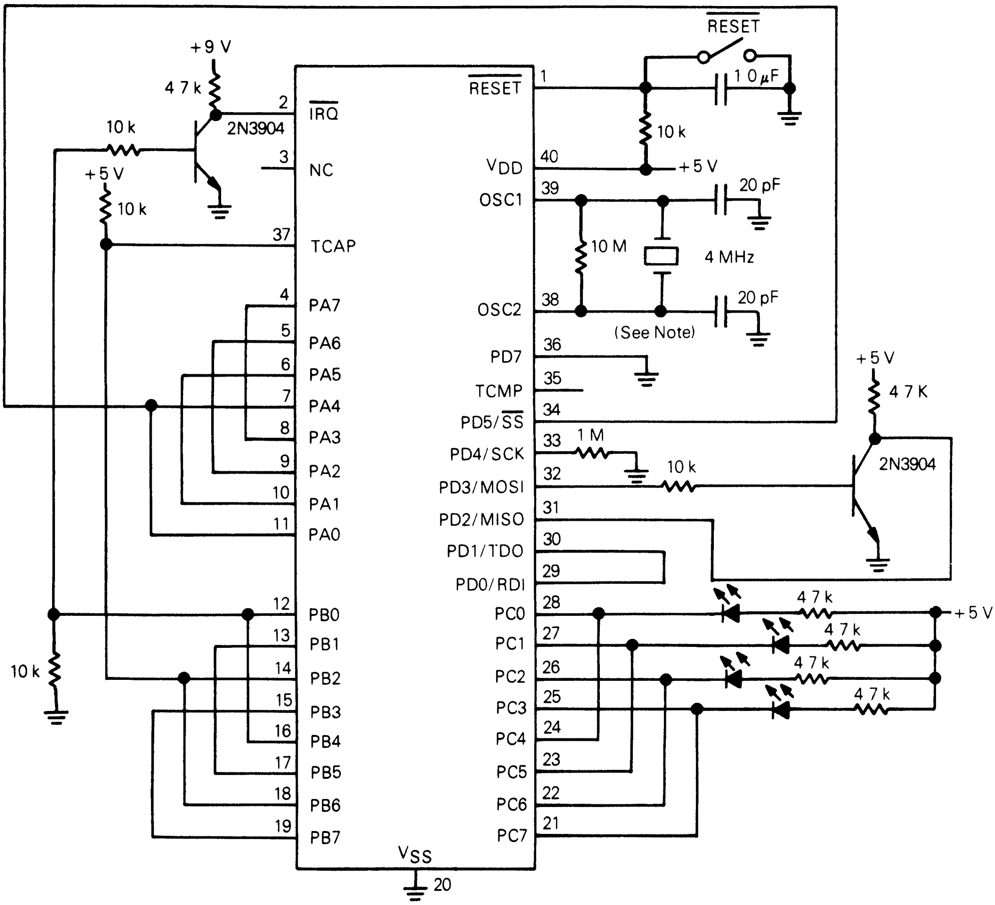
This subroutine returns with the Z bit cleared if any error is detected; otherwise, the Z bit is set.

This subroutine is called at location $1F0E. The output compare register is first set to the current timer state. Because the timer is free running and has only a divide-by-four prescaler, each timer count cannot be tested. The test reads the timer once every 10 counts (40 cycles) and checks for correct counting. The test tracks the counter until the timer wraps around, triggering the output compare flag in the timer status register. RAM locations $0050 and $0051 are overwritten. Upon return to the user's program, X=40. If the test passed, A=0.

2.7 ROM CHECKSUM SUBROUTINE

This subroutine returns with the Z bit cleared if any error is detected; otherwise, the Z bit is set.

This subroutine is called at location $1F93 with RAM location $0053 equal to $01 and A=0. A short routine is set up and executed in RAM to compute a checksum of the entire ROM pattern. Upon return to the user's program, X=0. If the test passed, A=0. RAM locations $0050 through $0053 are overwritten.



NOTE The RC Oscillator Option may also be used in this circuit

Figure 2-7. Self-Check Circuit Schematic Diagram

Table 2-2. Self-Check Results

PC3	PC2	PC1	PC0	Remarks
1	0	0	1	Bad I/O
1	0	1	0	Bad RAM
1	0	1	1	Bad Timer
1	1	0	0	Bad SCI
1	1	0	1	Bad ROM
1	1	1	0	Bad SPI
1	1	1	1	Bad Interrupts or IRQ Request
Flashing				Good Device
All Others				Bad Device, Bad Port C, etc

0 Indicates LED on; 1 Indicates LED is off.

SECTION 3
RESETS, INTERRUPTS, AND LOW POWER MODES

3.1 RESETS

The MCU has two reset modes: an active low external reset pin ($\overline{\text{RESET}}$) and a power-on reset function; refer to Figure 3-1.

3.1.1 $\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ input pin is used to reset the MCU to provide an orderly software startup procedure. When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one and one half t_{CYC}. The $\overline{\text{RESET}}$ pin contains an internal Schmitt Trigger as part of its input to improve noise immunity.

3.1.2 Power-On Reset

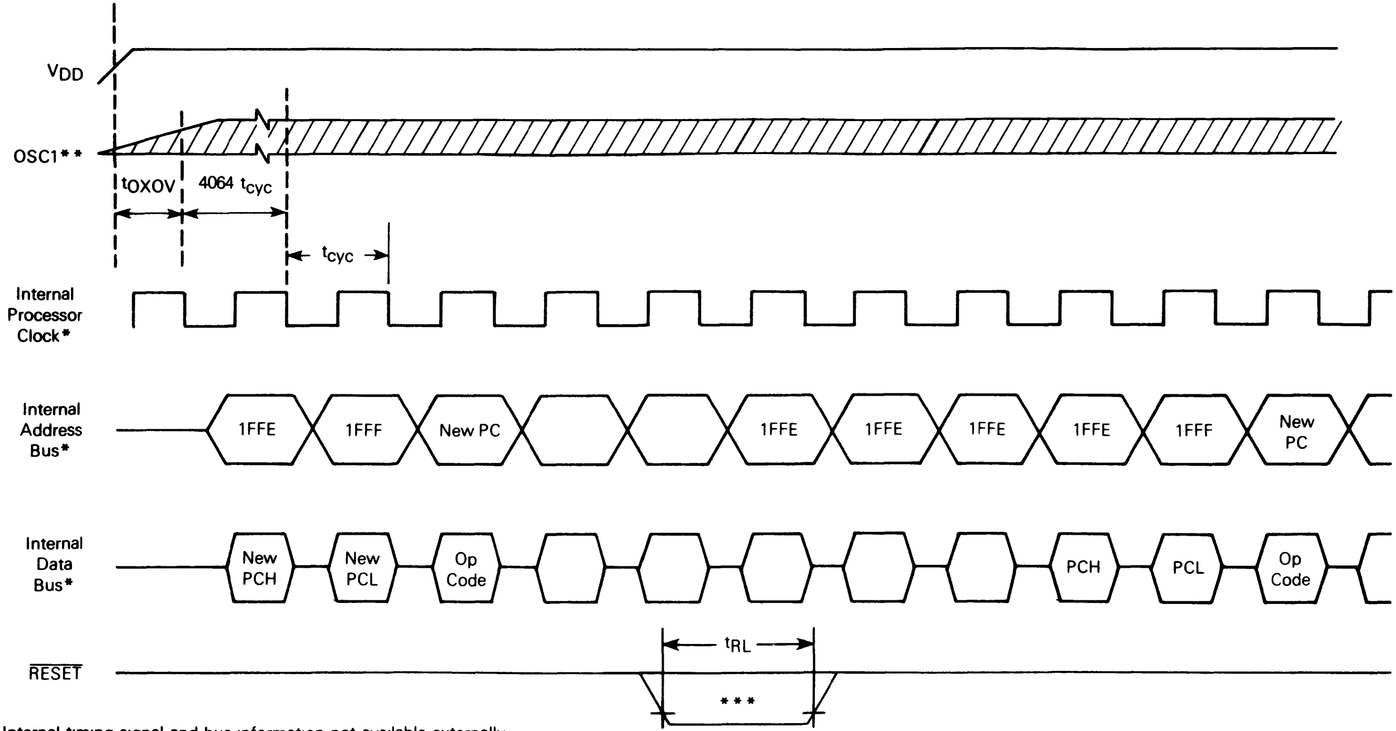
The power-on reset occurs when a positive transition is detected on V_{DD}. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. There is no provision for a power-down reset. The power-on circuitry provides for a 4064 t_{CYC} delay from the time that the oscillator becomes active. If the external $\overline{\text{RESET}}$ pin is low at the end of the 4064 t_{CYC} time out, the processor remains in the reset condition until $\overline{\text{RESET}}$ goes high.

Table 3-1 shows the actions of the two resets on internal circuits, but not necessarily in order of occurrence (X indicates that the condition occurs for the particular reset).

3.2 INTERRUPTS

Systems often require that normal processing be interrupted so that some external event may be serviced The CDP68HC05C4 may be interrupted by one of five different methods. either one of four maskable hardware interrupts ($\overline{\text{IRQ}}$, SPI, SCI, or Timer) and one non-maskable software interrupt (SWI). Interrupts such as Timer, SPI, and SCI have several flags which will cause the interrupt. Generally, interrupt flags are located in read-only status registers, whereas their equivalent enable bits are located in associated control registers. The interrupt flags and enable bits are never contained in the same register. If the enable bit is a logic zero it blocks the interrupt from occurring but does not inhibit the flag from being set. Reset clears all enable bits to preclude interrupts during the reset procedure.

The general sequence for clearing an interrupt is a software sequence of first accessing the status register while the interrupt flag is set, followed by a read or write of an associated register. When any of these interrupts occur, and if the enable bit is a logic one, normal processing is suspended at the end of the current instruction execution. Interrupts cause the processor registers to be saved on



*Internal timing signal and bus information not available externally

**OSC1 line is not meant to represent frequency It is only used to represent time

***The next rising edge of the internal processor clock following the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence

Figure 3-1. Power-On Reset and $\overline{\text{RESET}}$

Table 3-1. Reset Action on Internal Circuit

Condition	$\overline{\text{RESET}}$ Pin	Power-On Reset
Timer Prescaler reset to zero state	X	X
Timer counter configured to $FFFC	X	X
Timer output compare (TCMP) bit reset to zero	X	X
All timer interrupt enable bits cleared (ICIE, OCIE, and TOIE) to disable timer interrupts The OLVL timer bit is also cleared by reset	X	X
All data direction registers cleared to zero (input)	X	X
Configure stack pointer to $00FF	X	X
Force internal address bus to restart vector ($1FFE-$1FFF)	X	X
Set I bit in condition code register to a logic one	X	X
Clear STOP latch	X*	X
Clear external interrupt latch	X	X
Clear WAIT latch	X	X
Disable SCI (serial control bits TE=0 and RE=0) Other SCI bits cleared by reset include TIE, TCIE, RIE, ILIE, RWU, SBK, RDRF, IDLE, OR, NF, and FE	X	X
Disable SPI (serial output enable control bit SPE=0) Other SPI bits cleared by reset include SPIE, MSTR, SPIF, WCOL, and MODF	X	X
Set serial status bits TDRE and TC	X	X
Clear all serial interrupt enable bits (SPIE, TIE, and TCIE)	X	X
Place SPI system in slave mode (MSTR=0)	X	X
Clear SCI prescaler rate control bits SCP0-SCP1	X	X

*Indicates that timeout still occurs

the stack (see Figure 2-6) and the interrupt mask (I bit) set to prevent additional interrupts. The appropriate interrupt vector then points to the starting address of the interrupt service routine (refer to Figure 2-4 for vector location). Upon completion of the interrupt service routine, the RTI instruction (which is normally a part of the service routine) causes the register contents to be recovered from the stack followed by a return to normal processing. The stack order is shown in Figure 2-6.

NOTE

The interrupt mask bit (I bit) will be cleared if and only if the corresponding bit stored in the stack is zero.

A discussion of interrupts, plus a table listing vector addresses for all interrupts including reset, in the MCU is provided in Table 3-2.

Table 3.2. Vector Address for Interrupts and Reset*

Register	Flag Name	Interrupts	CPU Interrupt	Vector Address
N/A	N/A	Reset	$\overline{\text{RESET}}$	$1FFE-$1FFF
N/A	N/A	Software	SWI	$1FFC-$1FFD
N/A	N/A	External Interrupt	$\overline{\text{IRQ}}$	$1FFA-$1FFB
Timer Status	ICF	Input Capture	TIMER	$1FF8-$1FF9
	OCF	Output Compare		
	TOF	Timer Overflow		
SCI Status	TDRE	Transmit Buffer Empty	SCI	$1FF6-$1FF7
	TC	Transmit Complete		
	RDRF	Receiver Buffer Full		
	IDLE	Idle Line Detect		
	OR	Overrun		
SPI Status	SPIF	Transfer Complete	SPI	$1FF4-$1FF5
	MODF	Mode Fault		

*For explanation of ROM addresses $1FF0-1FF3, see "Ordering Information-Procedure for Submitting Data, Note #5" section of this document on page

3.2.1 Hardware Controlled Interrupt Sequence

The following three functions ($\overline{\text{RESET}}$, STOP, and WAIT) are not in the strictest sense an interrupt; however, they are acted upon in a similar manner. Flowcharts for hardware interrupts are shown in Figure 3-2, and for STOP and WAIT are provided in Figure 3-3. A discussion is provided below.

(a) – A low input on the $\overline{\text{RESET}}$ input pin causes the program to vector to its starting address which is specified by the contents of memory locations $1FFE and $1FFF. The I bit in the condition code register is also set. Much of the MCU is configured to a known state during this type of reset as previously described in **RESETS** paragraph 3.1.

(b) STOP – The STOP instruction causes the oscillator to be turned off and the processor to "sleep" until an external interrupt ($\overline{\text{IRQ}}$) or reset occurs.

(c) WAIT – The WAIT instruction causes all processor clocks to stop, but leaves the Timer, SCI, and SPI clocks running. This "rest" state of the processor can be cleared by reset, an external interrupt ($\overline{\text{IRQ}}$), Timer interrupt, SPI interrupt, or SCI interrupt There are no special wait vectors for these individual interrupts.

3.2.2 Software Interrupt (SWI)

The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask (I bit) in the condition code register. The interrupt service routine address is specified by the contents of memory location $1FFC and $1FFD.

3.2.3 External Interrupt

If the interrupt mask (I bit) of the condition code register has been cleared and the external interrupt pin ($\overline{\text{IRQ}}$) has gone low, then the external interrupt is recognized When the interrupt is recognized, the current state of the CPU is pushed onto the stack and the I bit is set. This masks further interrupts until the present one is serviced. The interrupt service routine address is specified by the contents of memory location $1FFA and $1FFB. Either a level-sensitive and negative edge-sensitive trigger, or a negative edge-sensitive only trigger are available as a mask option. Figure 3-4 shows both a functional and mode timing diagram for the interrupt line. The timing diagram shows two different treatments of the interrupt line ($\overline{\text{IRQ}}$) to the processor. The first method shows single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the number of cycles required to execute the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an RTI occurs). The second configuration shows several interrupt lines "wire-ORed" to form the interrupts at the processor. Thus, if after servicing one interrupt the interrupt line remains low, then the next interrupt is recognized.

NOTE

The internal interrupt latch is cleared in the first part of the service routine; therefore, one (and only one) external interrupt pulse could be latched during t_{ILIL} and serviced as soon as the I bit is cleared.

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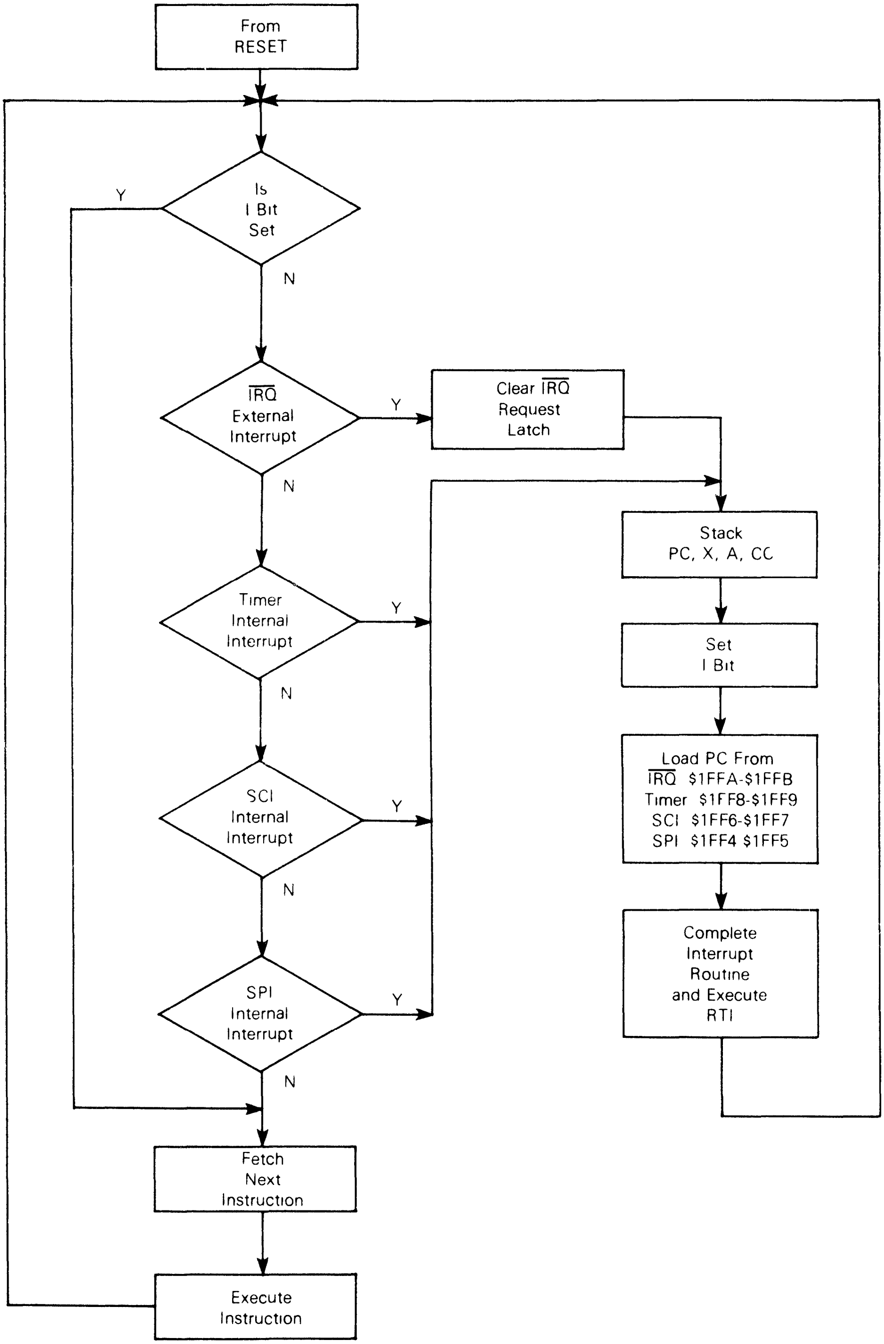


Figure 3-2. Hardware Interrupt Flowchart

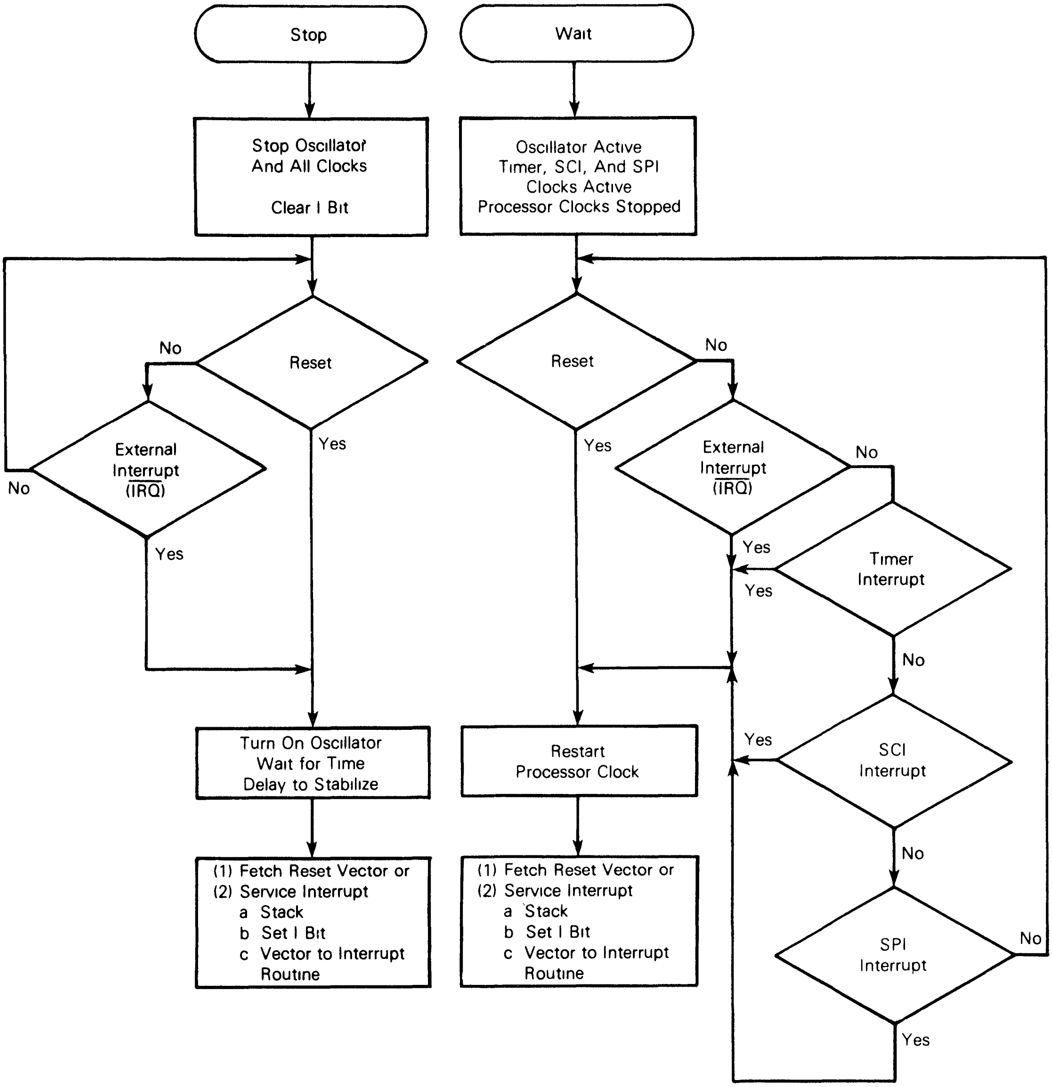
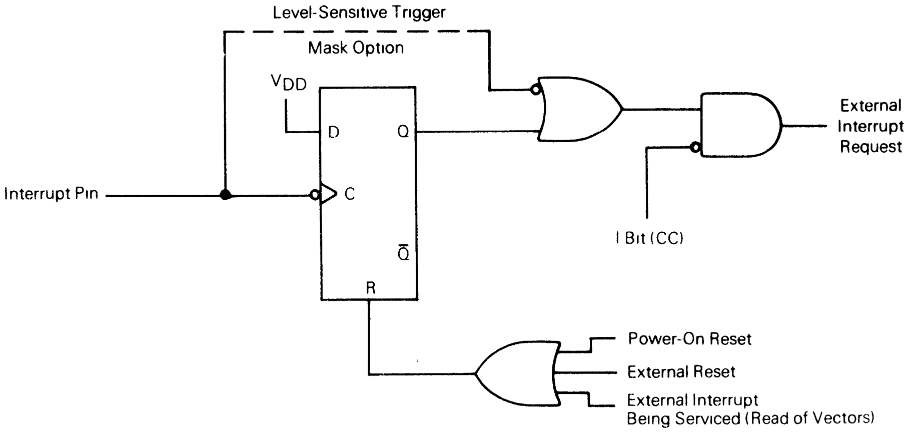
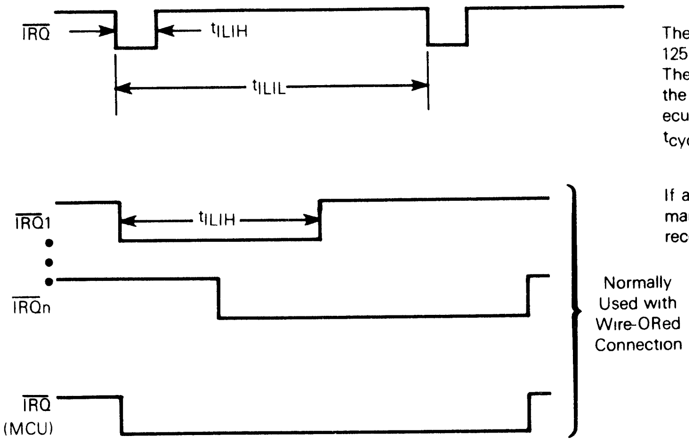


Figure 3-3. STOP/WAIT Flowcharts



(a) Interrupt Function Diagram



Edge-Sensitive Trigger Condition

The minimum pulse width (t_{ILIH}) is either 125 ns ($V_{DD}=5$ V) or 250 ns ($V_{DD}=3$ V) The period t_{ILIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routine plus 21 t_{cyc} cycles

Level-Sensitive Trigger Condition

If after servicing an interrupt the $\overline{IRQ}$ remains low, then the next interrupt is recognized

(b) Interrupt Mode Diagram

Figure 3-4. External Interrupt

3.2.4 Timer Interrupt

There are three different timer interrupt flags that will cause a timer interrupt whenever they are set and enabled. These three interrupt flags are found in the three most significant bits of the timer status register (TSR, location $13) and all three will vector to the same interrupt service routine ($1FF8-$1FF9).

All interrupt flags have corresponding enable bits (ICIE, OCIE, and TOIE) in the timer control register (TCR, location $12). Reset clears all enable bits, thus preventing an interrupt from occurring during the reset time period. The actual processor interrupt is generated only if the I bit in the condition code register is also cleared. When the interrupt is recognized, the current machine state is pushed onto the stack and I bit is set. This masks further interrupts until the present one is serviced. The interrupt service routine address is specified by the contents of memory location $1FF8 and $1FF9. The general sequence for clearing an interrupt is a software sequence of accessing the status register while the flag is set, followed by a read or write of an associated register. Refer to **SECTION 4 PROGRAMMABLE TIMER** for additional information about the timer circuitry.

3.2.5 Serial Communications Interface (SCI) Interrupts

An interrupt in the serial communications interface (SCI) occurs when one of the interrupt flag bits in the serial communications status register is set, provided the I bit in the condition code register is clear and the enable bit in the serial communications control register 2 (location $0F) is enabled. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the I bit in the condition code register is set. This masks further interrupts until the present one is serviced. The SCI interrupt causes the program counter to vector to memory location $1FF6 and $1FF7 which contains the starting address of the interrupt service routine. Software in the serial interrupt service routine must determine the priority and cause of the SCI interrupt by examining the interrupt flags and the status bits located in the serial communications status register (location $10). The general sequence for clearing an interrupt is a software sequence of accessing the serial communications status register while the flag is set followed by a read or write of an associated register. Refer to **SECTION 5 SERIAL COMMUNICATIONS INTERFACE** for a description of the SCI system and its interrupts.

3.2.6 Serial Peripheral Interface (SPI) Interrupts

An interrupt in the serial peripheral interface (SPI) occurs when one of the interrupt flag bits in the serial peripheral status register (location $0B) is set, provided the I bit in the condition code register is clear and the enable bit in the serial peripheral control register (location $0A) is enabled. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the I bit in the condition code register is set. This masks further interrupts until the present one is serviced. The SPI interrupt causes the program counter to vector to memory location $1FF4 and $1FF5 which contains the starting address of the interrupt service routine. Software in the serial peripheral interrupt service routine must determine the priority and cause of the SPI interrupt by examining the interrupt flag bits located in the SPI status register. The general sequence for clearing an interrupt is a software sequence of accessing the status register while the flag is set, followed by a read or write of an associated register. Refer to **SECTION 6 SERIAL PERIPHERAL INTERFACE** for a description of the SPI system and its interrupts.

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3.3 LOW POWER MODES

3.3.1 STOP Instruction

The STOP instruction places the MCU in its lowest power consumption mode. In the STOP mode the internal oscillator is turned off, causing all internal processing to be halted; refer to Figure 3-3. During the STOP mode, the I bit in the condition code register is cleared to enable external interrupts. All other registers and memory remain unaltered and all input/output lines remain unchanged. This continues until an external interrupt ($\overline{\text{IRQ}}$) or reset is sensed at which time the internal oscillator is turned on. The external interrupt or reset causes the program counter to vector to memory location $1FFA and $1FFE and $1FFF which contains the starting address of the interrupt or reset service routine respectively.

3.3.2 WAIT Instruction

The WAIT instruction places the MCU in a low power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode. In the WAIT mode, the internal clock remains active, and all CPU processing is stopped; however, the programmable timer, serial peripheral interface, and serial communications interface systems remain active. Refer to Figure 3-3. During the WAIT mode, the I bit in the condition code register is cleared to enable all interrupts. All other registers and memory remain unaltered and all parallel input/output lines remain unchanged. This continues until any interrupt or reset is sensed. At this time the program counter vectors to the memory location ($1FF4 through $1FFF) which contains the starting address of the interrupt or reset service routine.

3.4 DATA RETENTION MODE

The contents of RAM and CPU registers are retained at supply voltages as low as 2 V dc. This is referred to as the DATA RETENTION mode, where the data is held, but the device is not guaranteed to operate.

SECTION 4
PROGRAMMABLE TIMER

4.1 INTRODUCTION

The programmable timer, which is preceded by a fixed divide-by-four prescaler, can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from several microseconds to many seconds. A block diagram of the timer is shown in Figure 4-1 and timing diagrams are shown in Figures 4-2 through 4-5

Because the timer has a 16-bit architecture, each specific functional segment (capability) is represented by two registers. These registers contain the high and low byte of that functional segment. Generally, accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

NOTE

> The I bit in the condition code register should be set while manipulating both the high and low byte register of a specific timer function to ensure that an interrupt does not occur. This prevents interrupts from occurring between the time that the high and low bytes are accessed

The programmable timer capabilities are provided by using the following ten addressable 8-bit registers (note the high and low represent the significance of the byte). A description of each register is provided below.

Timer Control Register (TCR) location $12,
Timer Status Register (TSR) location $13,
Input Capture High Register location $14,
Input Capture Low Register location $15,
Output Compare High Register location $16,
Output Compare Low Register location $17,
Counter High Register location $18,
Counter Low Register location $19,
Alternate Counter High Register location $1A, and
Alternate Counter Low Register location $1B.

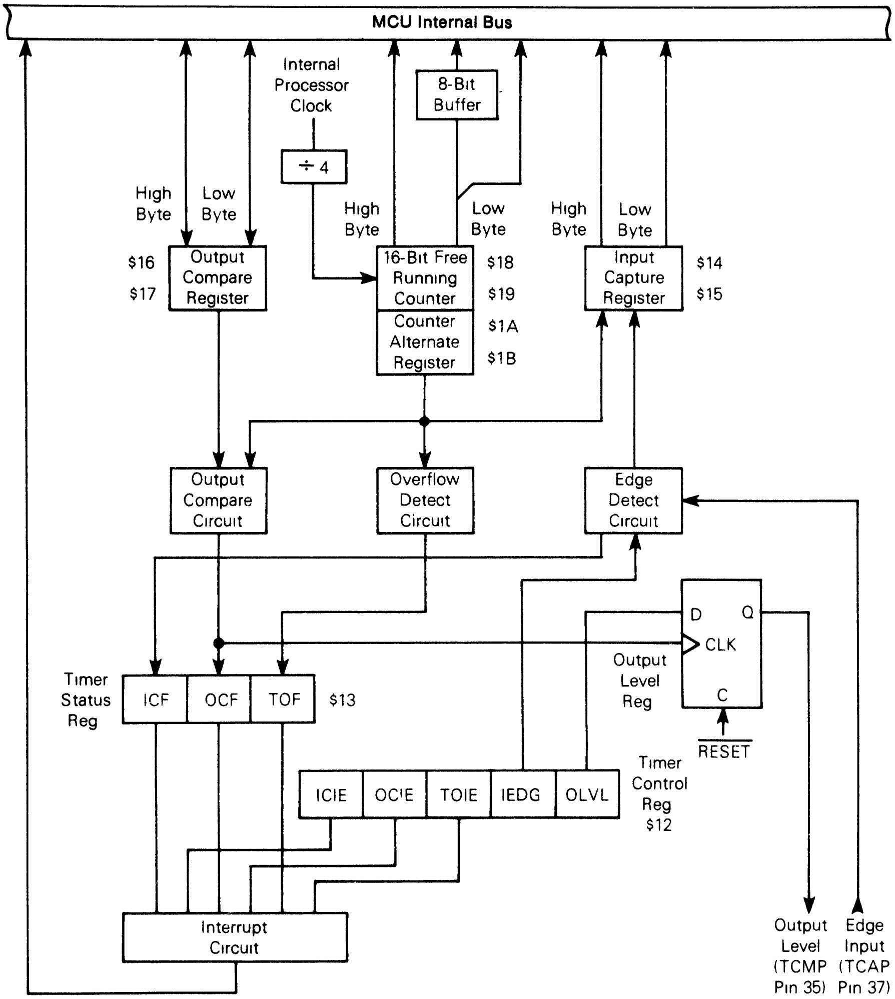
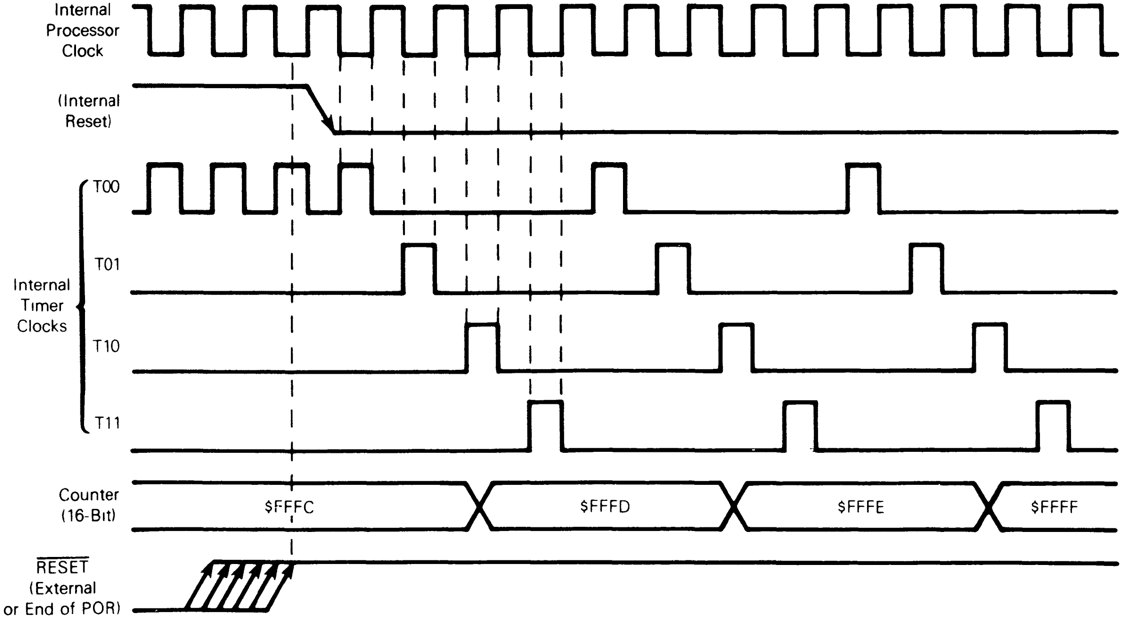
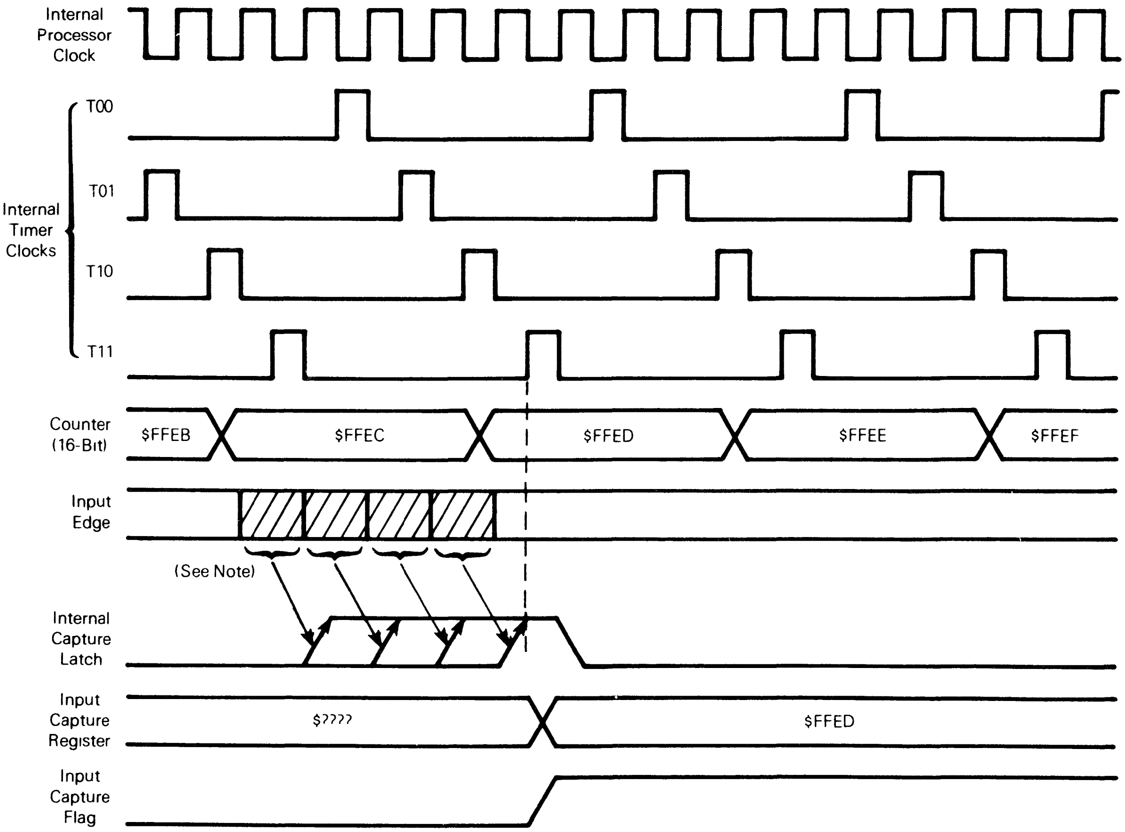


Figure 4-1. Programmable Timer Block Diagram



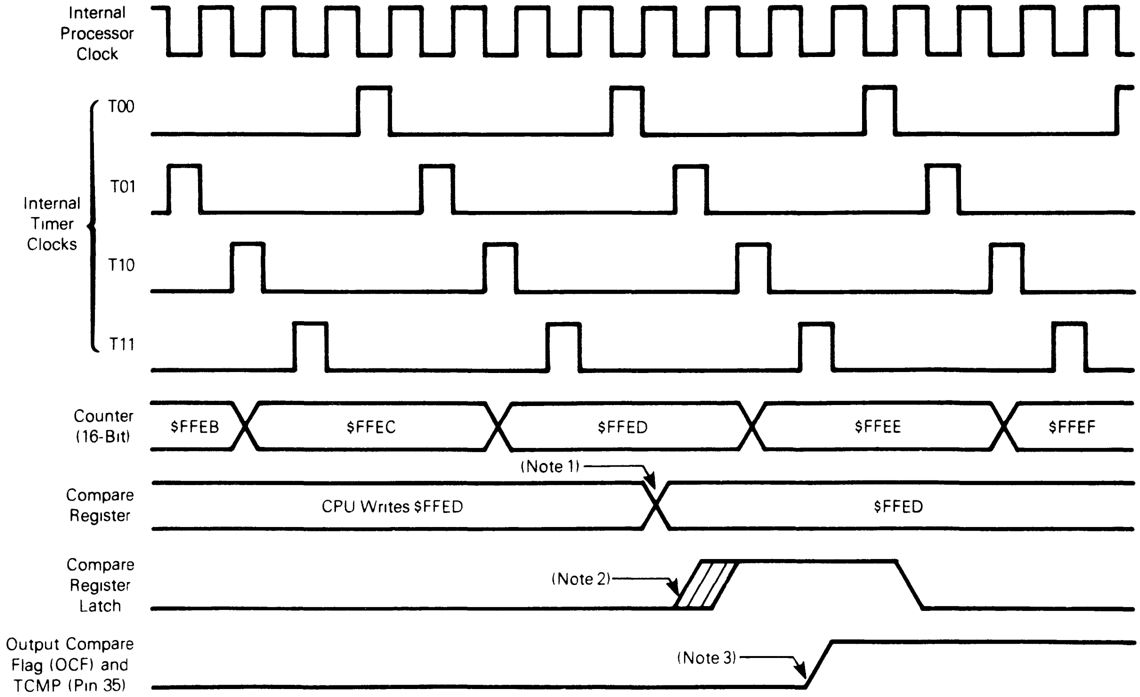
NOTE The Counter Register and Timer Control Register are the only ones affected by $\overline{\text{RESET}}$

Figure 4-2. Timer State Timing Diagram For Reset



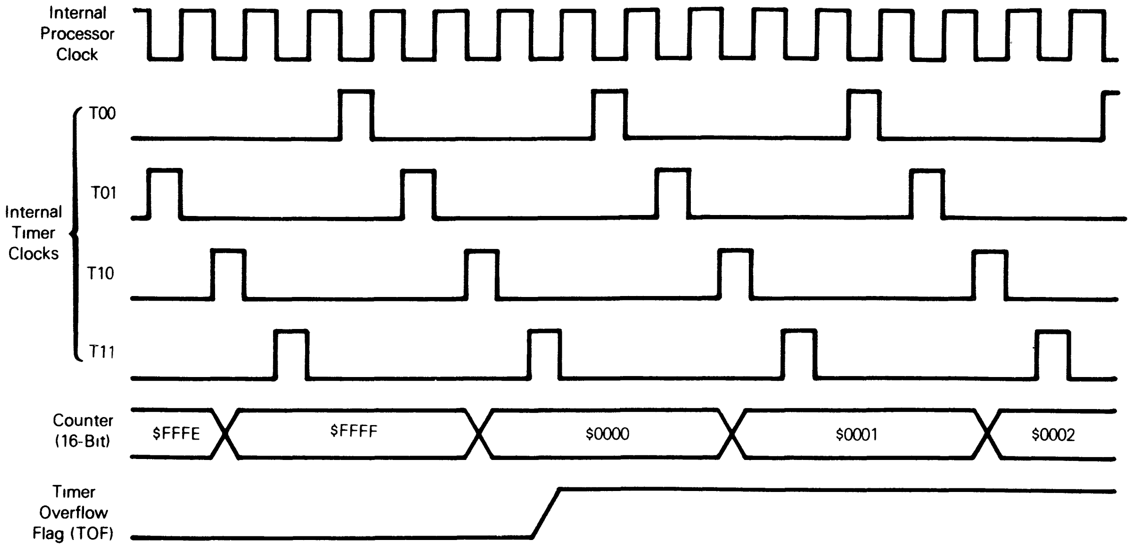
NOTE If the input edge occurs in the shaded area from one timer state T10 to the other timer state T10 the input capture flag is set during the next state T11

Figure 4-3. Timer State Timing Diagram For Input Capture



NOTES
1 The CPU write to the compare register may take place at any time, but a compare only occurs at timer state T01 Thus, a 4-cycle difference may exist between the write to the compare register and the actual compare
2 Internal compare takes place during timer state T01
3 OCF is set at the timer state T11 which follows the comparison match ($FFED in this example)

Figure 4-4. Timer State Timing Diagram For Output Compare



NOTE The TOF bit is set at timer state T11 (transition of counter from $FFFF to $0000) It is cleared by a read of the timer status register during the internal processor clock high time followed by a read of the counter low register

Figure 4-5. Timer State Diagram For Timer Overflow

4.2 COUNTER

The key element in the programmable timer is a 16-bit free running counter, or counter register, preceded by a prescaler which divides the internal processor clock by four. The prescaler gives the timer a resolution of 2.0 microseconds if the internal processor clock is 2.0 MHz. The counter is clocked to increasing values during the low portion of the internal processor clock. Software can read the counter at any time without affecting its value.

The double byte free running counter can be read from either of two locations \$18-\$19 (called counter register at this location), or \$1A-\$1B (counter alternate register at this location). A read sequence containing only a read of the least significant byte of the free running counter (\$19,\$1B) will receive the count value at the time of the read. If a read of the free running counter or counter alternate register first addresses the most significant byte (\$18,\$1A) it causes the least significant byte (\$19,\$1B) to be transferred to a buffer. This buffer value remains fixed after the first most significant byte "read" even if the user reads the most significant byte several times This buffer is accessed when reading the free running counter or counter alternate register least significant byte (\$19 or \$1B), and thus completes a read sequence of the total counter value. Note that in reading either the free running counter or counter alternate register, if the most significant byte is read, the least significant byte must also be read in order to complete the sequence.

The free running counter is configured to \$FFFC during reset and is always a read-only register. During a power-on-reset (POR), the counter is also configured to \$FFFC and begins running after the oscillator startup delay. Because the free running counter is 16 bits preceded by a fixed divide-by-four prescaler, the value in the free running counter repeats every 262,144 MPU internal processor clock cycles. When the counter rolls over from \$FFFF to \$0000, the timer overflow flag (TOF) bit is set. An interrupt can also be enabled when counter rollover occurs by setting its interrupt enable bit (TOIE).

4.3 OUTPUT COMPARE REGISTER

The output compare register is a 16-bit register, which is made up of two 8-bit registers at locations \$16 (most significant byte) and \$17 (least significant byte) The output compare register can be used for several purposes such as, controlling an output waveform or indicating when a period of time has elapsed. The output compare register is unique in that all bits are readable and writable and are not altered by the timer hardware. Reset does not affect the contents of this register and if the compare function is not utilized, the two bytes of the output compare register can be used as storage locations.

The contents of the output compare register are compared with the contents of the free running counter once during every four internal processor clocks If a match is found, the corresponding output compare flag (OCF) bit is set and the corresponding output level (OLVL) bit is clocked (by the output compare circuit pulse) to an output level register. The values in the output compare register and the output level bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit, OCIE, is set

After a processor write cycle to the output compare register containing the most significant byte (\$16), the output compare function is inhibited until the least significant byte (\$17) is also written. The user must write both bytes (locations) if the most significant byte is written first. A write made only to the least significant byte ($17) will not inhibit the compare function. The free running counter is updated every four internal processor clock cycles due to the internal prescaler. The minimum time required to update the output compare register is a function of the software program rather than the internal hardware.

A processor write may be made to either byte of the output compare register without affecting the other byte. The output level (OLVL) bit is clocked to the output level register regardless of whether the output compare flag (OCF) is set or clear.

Because neither the output compare flag (OCF bit) or output compare register is affected by reset, care must be exercised when initializing the output compare function with software. The following procedure is recommended:

(1) Write the high byte of the output compare register to inhibit further compares until the low byte is written.
(2) Read the timer status register to arm the OCF if it is already set.
(3) Write the output compare register low byte to enable the output compare function with the flag clear.

The advantage of this procedure is to prevent the OCF bit from being set between the time it is read and the write to the output compare register. A software example is shown below.

```
B7   16   STA   OCMPHI   INHIBIT OUTPUT COMPARE
B6   13   LDA   TSTAT    ARM OCF BIT IF SET
BF   17   STX   OCMPLD   READY FOR NEXT COMPARE
```

4.4 INPUT CAPTURE REGISTER

The two 8-bit registers which make up the 16-bit input capture register are read-only and are used to latch the value of the free running counter after a defined transition is sensed by the corresponding input capture edge detector. The level transition which triggers the counter transfer is defined by the corresponding input edge bit (IEDG). Reset does not affect the contents of the input capture register.

The result obtained by an input capture will be one more than the value of the free running counter on the rising edge of the internal processor clock preceding the external transition (refer to timing diagram shown in Figure 4-3). This delay is required for internal synchronization. Resolution is affected by the prescaler allowing the timer to only increment every four internal processor clock cycles.

The free running counter contents are transferred to the input capture register on each proper signal transition regardless of whether the input capture flag (ICF) is set or clear. The input capture register always contains the free running counter value which corresponds to the most recent input capture.

After a read of the most significant byte of the input capture register ($14), counter transfer is inhibited until the least significant byte ($15) of the input capture register is also read. This characteristic forces the minimum pulse period attainable to be determined by the time used in the capture software routine and its interaction with the main program. The free running counter increments every four internal processor clock cycles due to the prescaler.

A read of the least significant byte ($15) of the input capture register does not inhibit the free running counter transfer. Again, minimum pulse periods are ones which allow software to read the least significant byte ($15) and perform needed operations. There is no conflict between the read of the input capture register and the free running counter transfer since they occur on opposite edges of the internal processor clock.

4.5 TIMER CONTROL REGISTER (TCR)

The timer control register (TCR, location $12) is an 8-bit read/write register which contains five control bits. Three of these bits control interrupts associated with each of the three flag bits found in the timer status register (discussed below). The other two bits control: 1) which edge is significant to the input capture edge detector (i.e., negative or positive), and 2) the next value to be clocked to the output level register in response to a successful output compare. The timer control register and the free running counter are the only sections of the timer affected by reset. The TCMP pin is forced low during external reset and stays low until a valid compare changes it to a high. The timer control register is illustrated below followed by a definition of each bit.

7	6	5	4	3	2	1	0	
ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL	$12

B7, ICIE	If the input capture interrupt enable (ICIE) bit is set, a timer interrupt is enabled when the ICF status flag (in the timer status register) is set. If the ICIE bit is clear, the interrupt is inhibited. The ICIE bit is cleared by reset.
B6, OCIE	If the output compare interrupt enable (OCIE) bit is set, a timer interrupt is enabled whenever the OCF status flag is set. If the OCIE bit is clear, the interrupt is inhibited. The OCIE bit is cleared by reset.
B5, TOIE	If the timer overflow interrupt enable (TOIE) bit is set, a timer interrupt is enabled whenever the TOF status flag (in the timer status register) is set. If the TOIE bit is clear, the interrupt is inhibited. The TOIE bit is cleared by reset.
B1, IEDG	The value of the input edge (IEDG) bit determines which level transition on pin 37 will trigger a free running counter transfer to the input capture register. Reset does not affect the IEDG bit. 0 = negative edge 1 = positive edge
B0, OLVL	The value of the output level (OLVL) bit is clocked into the output level register by the next successful output compare and will appear at pin 35. This bit and the output level register are cleared by reset. 0 = low output 1 = high output

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4.6 TIMER STATUS REGISTER (TSR)

The timer status register (TSR) is an 8-bit register of which the three most significant bits contain read-only status information. These three bits indicate the following:

1. A proper transition has taken place at pin 37 with an accompanying transfer of the free running counter contents to the input capture register,
2. A match has been found between the free running·counter and the output compare register, and
3. A free running counter transition from $FFFF to $0000 has been sensed (timer overflow).

The timer status.register is illustrated below followed by a definition of each bit. Refer to timing diagrams shown in Figures 4-2, 4-3, and 4-4 for timing relationship to the timer status register bits.

7	6	5	4	3	2	1	0	
ICF	OCF	TOF	0	0	0	0	0	$13

B7, ICF — The input capture flag (ICF) is set when a proper edge has been sensed by the input capture edge detector. It is cleared by a processor access of the timer status register (with ICF set) followed by accessing the low byte ($15) of the input capture register. Reset does not affect the input compare flag.

B6, OCF — The output compare flag (OCF) is set when the output compare register contents matches the contents of the free running counter. The OCF is cleared by accessing the timer status register (with OCF set) and then accessing the low byte ($17) of the output compare register. Reset does not affect the output compare flag.

B5, TOF — The timer overflow flag (TOF) bit is set by a transition of the free running counter from $FFFF to $0000. It is cleared by accessing the timer status register (with TOF set) followed by an access of the free running counter least significant byte ($19). Reset does not affect the TOF bit.

Accessing the timer status register satisfies the first condition required to clear any status bits which happen to be set during the access. The only remaining step is to provide an access of the register which is associated with the status bit. Typically, this presents no problem for the input capture and output compare functions.

A problem can occur when using the timer overflow function and reading the free running counter at random times to measure an elapsed time. Without incorporating the proper precautions into software, the timer overflow flag could unintentionally be cleared if: 1) the timer status register is read or written when TOF is set, and 2) the least significant byte of the free running counter is read but not for the purpose of servicing the flag. The counter alternate register at address $1A and $1B contains the same value as the free running counter (at address $18 and $19); therefore, this alternate register can be read at any time without affecting the timer overflow flag in the timer status register.

During STOP and WAIT instructions, the programmable timer functions as follows: during the wait mode, the timer continues to operate normally and may generate an interrupt to trigger the CPU out of the wait state; during the stop mode, the timer holds at its current state, retaining all data, and resumes operation from this point when an external interrupt is received.

SECTION 5
SERIAL COMMUNICATIONS INTERFACE (SCI)

5.1 INTRODUCTION

A full-duplex asynchronous serial communications interface (SCI) is provided with a standard NRZ format and a variety of baud rates. The SCI transmitter and receiver are functionally independent, but use the same data format and bit rate. The serial data format is standard mark/space (NRZ) which provide one start bit, eight or nine data bits, and one stop bit. "Baud" and "bit rate" are used synonymously in the following description.

5.1.1 SCI Two Wire System Features

- Standard NRZ (mark/space) format.
- Advanced error detection method includes noise detection for noise duration of up to 1/16 bit time.
- Full-duplex operation (simultaneous transmit and receive).
- Software programmable for one of 32 different baud rates.
- Software selectable world length (eight or nine bit words)
- Separate transmitter and receiver enable bits.
- SCI may be interrupt driven.
- Four separate enable bits available for interrupt control

5.1.2 SCI Receiver Features

- Receiver wake-up function (idle or address bit).
- Idle line detect.
- Framing error detect.
- Noise detect.
- Overrun detect.
- Receiver data register full flag.

5.1.3 SCI Transmitter Features

- Transmit data register empty flag.
- Transmit complete flag.
- Break send.

Any SCI two-wire system requires receive data in (RDI) and transmit data out (TDO).

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5.2 DATA FORMAT

Receive data in (RDI) or transmit data out (TDO) is the serial data which is presented between the internal data bus and the output pin (TDO), and between the input pin (RDI) and the internal data bus. Data format is as shown for the NRZ in Figure 5-1 and must meet the following criteria:

1. A high level indicates a logic one and a low level indicates a logic zero.
2. The idle line is in a high (logic one) state prior to transmission/reception of a message.
3. A start bit (logic zero) is transmitted/received indicating the start of a message.
4. The data is transmitted and received least-significant-bit first.
5. A stop bit (high in the tenth or eleventh bit position) indicates the byte is complete.
6. A break is defined as the transmission or reception of a low (logic zero) for some multiple of the data format.

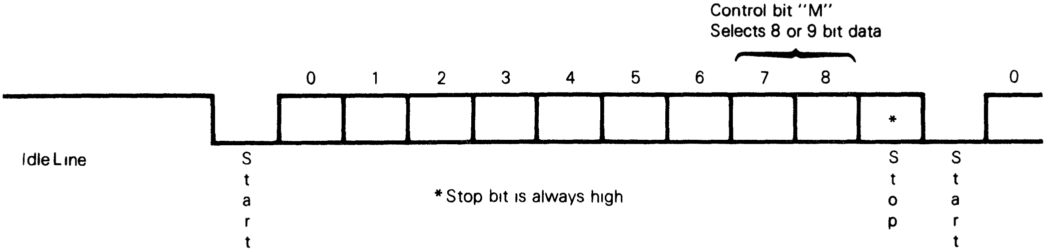

Figure 5-1. Data Format

5.3 WAKE-UP FEATURE

In a typical multiprocessor configuration, the software protocol will usually identify the addressée(s) at the beginning of the message. In order to permit uninterested MPUs to ignore the remainder of the message, a wake-up feature is included whereby all further SCI receiver flag (and interrupt) processing can be inhibited until its data line returns to the idle state. An SCI receiver is re-enabled by an idle string of at least ten (or eleven) consecutive ones. Software for the transmitter must provide for the required idle string between consecutive messages and prevent it from occurring within messages.

The user is allowed a second method of providing the wake-up feature in lieu of the idle string discussed above. This method allows the user to insert a logic one in the most significant bit of the transmit data word which needs to be received by all "sleeping" processors.

5.4 RECEIVE DATA IN

Receive data in is the serial data which is presented from the input pin via the SCI to the internal data bus. While waiting for a start bit, the receiver samples the input at a rate which is 16 times higher than the set baud rate. This 16 times higher-than-baud rate is referred to as the RT rate in Figures 5-2 and 5-3, and as the receiver clock in Figure 5-7. When the input (idle) line is detected low, it is tested for three more sample times (referred to as the start edge verification samples in Figure 5-2). If at least two of these three verification samples detect a logic low, a valid start bit is assumed to have been detected (by a logic low following the three start qualifiers) as shown in Figure 5-2; however, if in two or more of the verification samples a logic high is detected, the line is

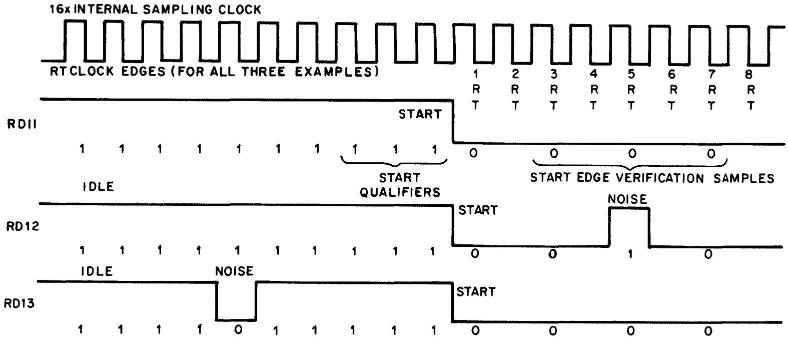

Figure 5-2. Examples of Start Bit Sampling Technique

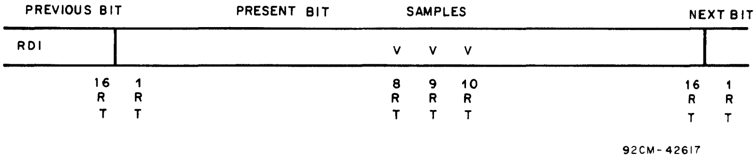

Figure 5-3. Sampling Technique Used on All Bits

assumed to be idle. (A noise flag is set if one of the three verification samples detects a logic high, thus a valid start bit could be assumed and a noise flag still set) The receiver clock generator is controlled by the baud rate register (see Figures 5-6 and 5-7); however, the serial communications interface is synchronized by the start bit (independent of the transmitter).

Once a valid start bit is detected, the start bit, each data bit, and the stop bit are sampled three times at RT intervals of 8RT, 9RT, and 10RT (1RT is the position where the bit is expected to start) as shown in Figure 5-3. The value of the bit is determined by voting logic which takes the value of the majority of samples (two or three out of three). A noise flag is set when all three samples on a valid start bit or a data bit or the stop bit do not agree. (As discussed above, a noise flag is also set when the start bit verification samples do not agree.)

5.5 START BIT DETECTION FOLLOWING A FRAMING ERROR

If there has been a framing error without detection of a break (10 zeros for 8-bit format or 11 zeros for 9-bit format), the circuit continues to operate as if there actually were a stop bit and the start

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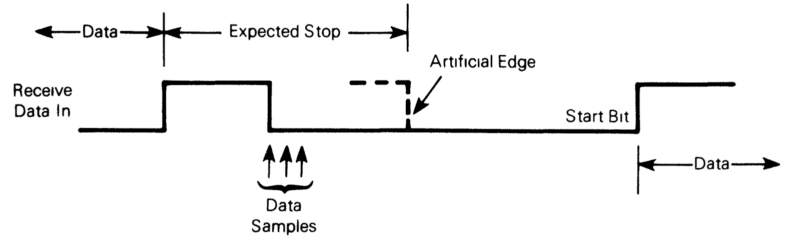
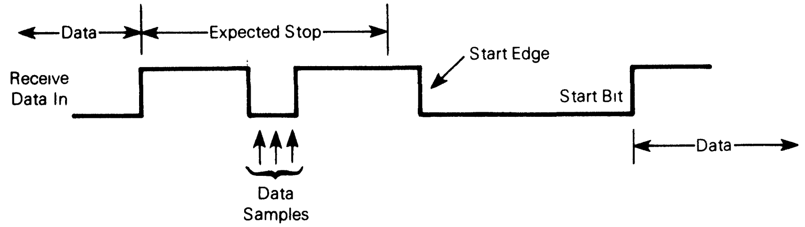
edge will be placed artificially. The last bit received in the data shift register is inverted to a logic one, and the three logic one start qualifiers (shown in Figure 5-2) are forced into the sample shift register during the interval when detection of a start bit is anticipated (see Figure 5-4); therefore the start bit will be accepted no sooner than it is anticipated.

If the receiver detects that a break (RDRF = 1, FE = 1, receiver data register = $00) produced the framing error, the start bit will not be artificially induced and the receiver must actually receive a logic one bit before start. See Figure 5-5.



(a) Case 1, Receive Line Low During Artificial Edge



(b) Case 2, Receive Line High During Expected Start Edge

Figure 5-4. SCI Artificial Start Following A Framing Error

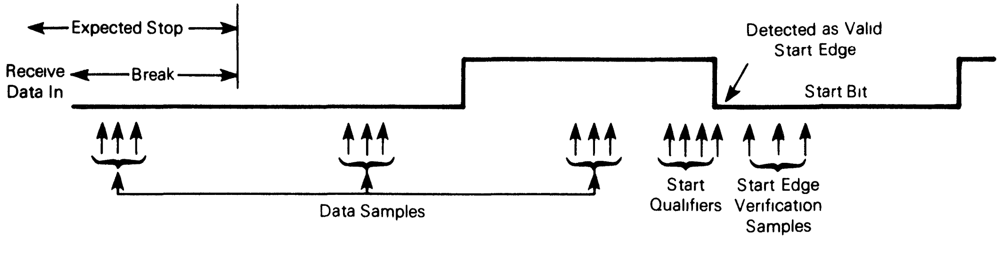


Figure 5-5. SCI Start Bit Following A Break

5.6 TRANSMIT DATA OUT (TDO)

Transmit data out is the serial data which is presented from the internal data bus via the SCI and then to the output pin. Data format is as discussed above and shown in Figure 5-1. The transmitter generates a bit time by using a derivative of the RT clock, thus producing a transmission rate equal to 1/16 that of the receiver sample clock.

5.7 REGISTERS

There are five different registers used in the serial communications interface (SCI) and the internal configuration of these registers is discussed in the following paragraphs. A block diagram of the SCI system is shown in Figure 5-6.

5.7.1 Serial Communications Data Register (SCDAT)

7	6	5	4	3	2	1	0	
Serial Communications Data Register								$11

The serial communications data register performs two functions in the serial communications interface; i.e. it acts as the receive data register when it is read and as the transmit data register when it is written. Figure 5-6 shows this register as two separate registers, namely: the receive data register (RDR) and the transmit data register (TDR). As shown in Figure 5-6, the TDR (transmit data register) provides the parallel interface from the internal data bus to the transmit shift register and the receive data register (RDR) provides the interface from the receive shift register to the internal data bus.

When SCDAT is read, it becomes the receive data register and contains the last byte of data received. The receive data register, represented above, is a read-only register containing the last byte of data received from the shift register for the internal data bus. The RDRF bit (receive data register full bit in the serial communications status register) is set to indicate that a byte has been transferred from the input serial shift register to the serial communications data register. The transfer is synchronized with the receiver bit rate clock (from the receive control) as shown in Figure 5-6. All data is received least-significant-bit first.

When SCDAT is written, it becomes the transmit data register and contains the next byte of data to be transmitted. The transmit data register, also represented above, is a write-only register containing the next byte of data to be applied to the transmit shift register from the internal data bus. As long as the transmitter is enabled, data stored in the serial communications data register is transferred to the transmit shift register (after the current byte in the shift register has been transmitted). The transfer from the SCDAT to the transmit shift register is synchronized with the bit rate clock (from the transmit control) as shown in Figure 5-6. All data is transmitted least-significant-bit first.

5.7.2 Serial Communications Control Register 1 (SCCR1)

7	6	5	4	3	2	1	0	
R8	T8	–	M	WAKE	–	–	–	$0E

The serial communications control register 1 (SCCR1) provides the control bits which: 1) determine the word length (either 8 or 9 bits), and 2) selects the method used for the wake-up feature. Bits 6 and 7 provide a location for storing the ninth bit for longer bytes.

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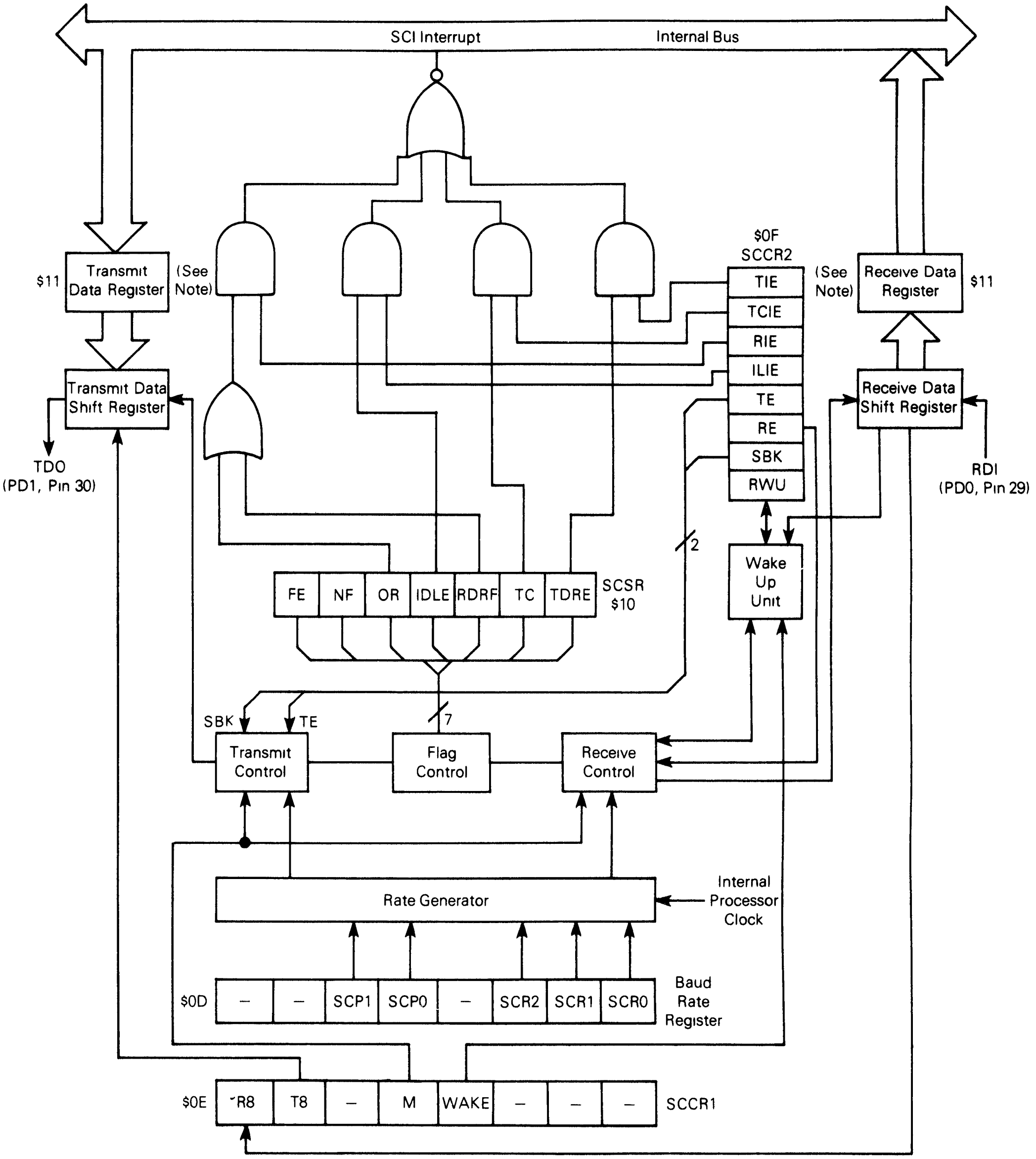


NOTE The Serial Communications Data Register (SCDAT) is controlled by the internal R/W signal It is the transmit data register when written and receive data register when read

Figure 5-6. Serial Communications Interface Block Diagram

B7, R8 If the M bit is a one, then this bit provides a storage location for the ninth bit in the receive data byte. Reset does not affect this bit.

B6, T8 If the M bit is a one, then this bit provides a storage location for the ninth bit in the transmit data byte. Reset does not affect this bit.

B4, M The option of the word length is selected by the configuration of this bit and is shown below. Reset does not affect this bit.

0 = 1 start bit, 8 data bits, 1 stop bit
1 = 1 start bit, 9 data bits, 1 stop bit

B3, WAKE This bit allows the user to select the method for receiver "wake up". If the WAKE bit is a logic zero, an idle line condition will "wake up" the receiver If the WAKE bit is set to a logic one, the system acknowledges an address bit (most significant bit). The address bit is dependent on both the WAKE bit and the M bit level (table shown below). (Additionally, the receiver does not use the wake-up feature unless the RWU control bit in serial communications control register 2 is set as discussed below.) Reset does not affect this bit

Wake	M	Method of Receiver "Wake-Up"
0	X	Detection of an idle line allows the next data byte received to cause the receive data register to fill and produce an RDRF flag.
1	0	Detection of a received one in the eighth data bit allows an RDRF flag and associated error flags.
1	1	Detection of a received one in the ninth data bit allows an RDRF flag and associated error flags.

5.7.3 Serial Communications Control Register 2 (SCCR2)

7	6	5	4	3	2	1	0	
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	$0F

The serial communications control register 2 (SCCR2) provides the control bits which: individually enable/disable the transmitter or receiver, enable the system interrupts, and provide the wake-up enable bit and a "send break code" bit. Each of these bits is described below (The individual flags are discussed in the **5.7.4 Serial Communications Status Register**.)

B7, TIE When the transmit interrupt enable bit is set, the SCI interrupt occurs provided TDRE is set (see Figure 5-6) When TIE is clear, the TDRE interrupt is disabled. Reset clears the TIE bit.

B6, TCIE When the transmission complete interrupt enable bit is set, the SCI interrupt occurs provided TC is set (see Figure 5-6). When TCIE is clear, the TC interrupt is disabled. Reset clears the TCIE bit.

B5, RIE	When the receive interrupt enable bit is set, the SCI interrupt occurs provided OR is set or RDRF is set (see Figure 5-6). When RIE is clear, the OR and RDRF interrupts are disabled. Reset clears the RIE bit.
B4, ILIE	When the idle line interrupt enable bit is set, the SCI interrupt occurs provided IDLE is set (see Figure 5-6). When ILIE is clear, the IDLE interrupt is disabled. Reset clears the ILIE bit.
B3, TE	When the transmit enable bit is set, the transmit shift register output is applied to the TDO line. Depending on the state of control bit M in serial communications control register 1, a preamble of 10 (M = 0) or 11 (M = 1) consecutive ones is transmitted when software sets the TE bit from a cleared state. If a transmission is in progress, and TE is written to a zero, then the transmitter will wait until after the present byte has been transmitted before placing the TDO pin in the idle high-impedance state. If the TE bit has been written to a zero and then set to a one before the current byte is transmitted, the transmitter will wait until that byte is transmitted and will then initiate transmission of a new preamble. After the preamble is transmitted, and provided the TDRE bit is set (no new data to transmit), the line remains idle (driven high while TE = 1); otherwise, normal transmission occurs. This function allows the user to "neatly" terminate a transmission sequence. After loading the last byte in the serial communications data register and receiving the interrupt from TDRE, indicating the data has been transferred into the shift register, the user should clear TE. The last byte will then be transmitted and the line will go idle (high impedance). Reset clears the TE bit.
B2, RE	When the receive enable bit is set, the receiver is enabled. When RE is clear, the receiver is disabled and all of the status bits associated with the receiver (RDRF, IDLE, OR, NF, and FE) are inhibited. Reset clears the RE bit.
B1, RWU	When the receiver wake-up bit is set, it enables the "wake up" function. The type of "wake up" mode for the receiver is determined by the WAKE bit discussed above (in the SCCR1). When the RWU bit is set, no status flags will be set. Flags which were set previously will not be cleared when RWU is set. If the WAKE bit is cleared, RWU is cleared after receiving 10 (M = 0) or 11 (M = 1) consecutive ones. Under these conditions, RWU cannot be set if the line is idle. If the WAKE bit is set, RWU is cleared after receiving an address bit. The RDRF flag will then be set and the address byte will be stored in the receiver data register. Reset clears the RWU bit.
B0, SBK	When the send break bit is set the transmitter sends zeros in some number equal to a multiple of the data format bits. If the SBK bit is toggled set and clear, the transmitter sends 10 (M = 0) or 11 (M = 1) zeros and then reverts to idle or sending data. The actual number of zeros sent when SBK is toggled depends on the data format set by the M bit in the serial communications control register 1; therefore, the break code will be synchronous with respect to the data stream. At the completion of the break code, the transmitter sends at least one high bit to guarantee recognition of a valid start bit. Reset clears the SBK bit.

5.7.4 Serial Communications Status Register (SCSR)

7	6	5	4	3	2	1	0	
TDRE	TC	RDRF	IDLE	OR	NF	FE	–	$10

The serial communications status register (SCSR) provides inputs to the interrupt logic circuits for generation of the SCI system interrupt. In addition, a noise flag bit and a framing error bit are also contained in the SCSR.

B7, TDRE — The transmit data register empty bit is set to indicate that the contents of the serial communications data register have been transferred to the transmit serial shift register. If the TDRE bit is clear, it indicates that the transfer has not yet occurred and a write to the serial communications data register will overwrite the previous value. The TDRE bit is cleared by accessing the serial communications status register (with TDRE set), followed by writing to the serial communications data register. Data can not be transmitted unless the serial communications status register is accessed before writing to the serial communications data register to clear the TDRE flag bit Reset sets the TDRE bit

B6, TC — The transmit complete bit is set at the end of a data frame, preamble, or break condition if:

1. TE=1, TDRE=1, and no pending data, preamble, or break is to be transmitted; or
2. TE=0, and the data, preamble, or break (in the transmit shift register) has been transmitted.

The TC bit is a status flag which indicates that one of the above conditions has occurred. The TC bit is cleared by accessing the serial communications status register (with TC set), followed by writing to the serial communications data register. It does not inhibit the transmitter function in any way. Reset sets the TC bit.

B5, RDRF — When the receive data register full bit is set, it indicates that the receiver serial shift register is transferred to the serial communications data register If multiple errors are detected in any one received word, the NF, FE, and RDRF bits will be affected as appropriate during the same clock cycle. The RDRF bit is cleared when the serial communications status register is accessed (with RDRF set) followed by a read of the serial communications data register. Reset clears the RDRF bit.

B4, IDLE — When the idle line detect bit is set, it indicates that a receiver idle line is detected (receipt of a minimum number of ones to constitute the number of bits in the byte format). The minimum number of ones needed will be 10 (M=0) or 11 (M=1). This allows a receiver that is not in the wake-up mode to detect the end of a message, detect the preamble of a new message, or to resynchronize with the transmitter. The IDLE bit is cleared by accessing the serial communications status register (with IDLE set) followed by a read of the serial communications data register. The IDLE bit will not be set again until after an RDRF has been set; i.e., a new idle line occurs. The IDLE bit is not set by an idle line when the receiver "wakes up" from the wake-up mode. Reset clears the IDLE bit.

B3, OR	When the overrun error bit is set, it indicates that the next byte is ready to be transferred from the receive shift register to the serial communications data register when it is already full (RDRF bit is set). Data transfer is then inhibited until the RDRF bit is cleared. Data in the serial communications data register is valid in this case, but additional data received during an overrun condition (including the byte causing the overrun) will be lost. The OR bit is cleared when the serial communications status register is accessed (with OR set), followed by a read of the serial communications data register. Reset clears the OR bit.
B2, NF	The noise flag bit is set if there is noise on a "valid" start bit or if there is noise on any of the data bits or if there is noise on the stop bit. It is not set by noise on the idle line nor by invalid (false) start bits. If there is noise, the NF bit is not set until the RDRF flag is set. Each data bit is sampled three times as described above in RECEIVE DATA IN and shown in Figure 5-3. The NF bit represents the status of the byte in the serial communications data register. For the byte being received (shifted in) there will also be a "working" noise flag the value of which will be transferred to the NF bit when the serial data is loaded into the serial communications data register. The NF bit does not generate an interrupt because the RDRF bit gets set with NF and can be used to generate the interrupt. The NF bit is cleared when the serial communications status register is accessed (with NF set), followed by a read of the serial communications data register. Reset clears the NF bit.
B1, FE	The framing error bit is set when the byte boundaries in the bit stream are not synchronized with the receiver bit counter (generated by a "lost" stop bit). The byte is transferred to the serial communications data register and the RDRF bit is set. The FE bit does not generate an interrupt because the RDRF bit is set at the same time as FE and can be used to generate the interrupt. Note that if the byte received causes a framing error and it will also cause an overrun if transferred to the serial communications data register, then the overrun bit will be set, but not the framing error bit, and the byte will not be transferred to the serial communications data register. The FE bit is cleared when the serial communications status register is accessed (with FE set) followed by a read of the serial communications data register. Reset clears the FE bit.

5.7.5 Baud Rate Register

7	6	5	4	3	2	1	0	
–	–	SCP1	SCP0	–	SCR2	SCR1	SCR0	$0D

The baud rate register provides the means for selecting different baud rates which may be used as the rate control for the transmitter and receiver. The SCP0-SCP1 bits function as a prescaler for the

SCR0-SCR2 bits. Together, these five bits provide multiple, baud rate combinations for a given crystal frequency.

B5, SCP1
B4, SCP0

These two bits in the baud rate register are used as a prescaler to increase the range of standard baud rates controlled by the SCR0-SCR2 bits. A table of the prescaler internal processor clock division versus bit levels is provided below. Reset clears SCP1-SCP0 bits (divide-by-one).

SCP1	SCP0	Internal Processor Clock Divide By
0	0	1
0	1	3
1	0	4
1	1	13

B2, SCR2
B1, SCR1
B0, SCR0

These three bits in the baud rate register are used to select the baud rates of both the transmitter and receiver. A table of baud rates versus bit levels is shown below. Reset does not affect the SCR2-SCR0 bits.

SCR2	SCR1	SCR0	Prescaler Output Divide By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

The diagram of Figure 5-7 and Tables 5-1 and 5-2 illustrate the divided chain used to obtain the baud rate clock (transmit clock). Note that there is a fixed rate divide-by-16 between the receive clock (RT) and the transmit clock (Tx). The actual divider chain is controlled by the combined SCP0-SCP1 and SCR0-SCR2 bits in the baud rate register as illustrated. All divided frequencies shown in the first table represent the final transmit clock (the actual baud rate) resulting from the internal processor clock division shown in the "divide-by" column only (prescaler division only) The second table illustrates how the prescaler output can be further divided by action of the SCI select bits (SCR0-SCR2). For example, assume that a 9600 Hz baud rate is required with a 2.4576 MHz external crystal. In this case the prescaler bits (SCP0-SCP1) could be configured as a divide-by-one or a divide-by-four. If a divide-by-four prescaler is used, then the SCR0-SCR2 bits must be configured as a divide-by-two. This results in a divide-by-128 of the internal processor clock to produce a 9600 Hz baud rate clock. Using the same crystal, the 9600 baud rate can be obtained with a prescaler divide-by-one and the SCR0-SCR2 bits configured for a divide-by-eight.

NOTE

The crystal frequency is internally divided-by-two to generate the internal processor clock.

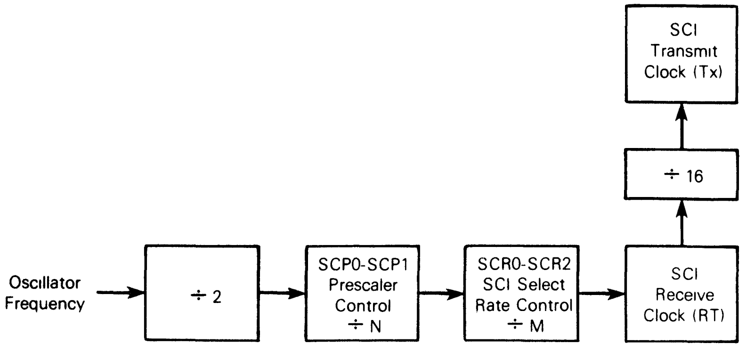


Figure 5-7. Rate Generator Division

Table 5-1. Prescaler Highest Baud Rate Frequency Output

SCP Bit		Clock* Divided By	Crystal Frequency MHz				
1	0		4.194304	4.0	2.4576	2.0	1.8432
0	0	1	131 072 kHz	125 000 kHz	76 80 kHz	62 50 kHz	57 60 kHz
0	1	3	43 691 kHz	41 666 kHz	25 60 kHz	20 833 kHz	19 20 kHz
1	0	4	32 768 kHz	31 250 kHz	19 20 kHz	15 625 kHz	14 40 kHz
1	1	13	10 082 kHz	9600 Hz	5 907 kHz	4800 Hz	4430 Hz

*The clock in the "Clock Divided By" column is the internal processor clock

NOTE The divided frequencies shown in Table 5-1 represent baud rates which are the highest transmit baud rate (Tx) that can be obtained by a specific crystal frequency and only using the prescaler division Lower baud rates may be obtained by providing a further division using the SCI rate select bits as shown below for some representative prescaler outputs

Table 5-2. Transmit Baud Rate Output For a Given Prescaler Output

SCR Bits			Divide By	Representative Highest Prescaler Baud Rate Output				
2	1	0		131.072 kHz	32.768 kHz	76.80 kHz	19.20 kHz	9600 Hz
0	0	0	1	131 072 kHz	32 768 kHz	76 80 kHz	19 20 kHz	9600 Hz
0	0	1	2	65 536 kHz	16 384 kHz	38 40 kHz	9600 Hz	4800 Hz
0	1	0	4	32 768 kHz	8 192 kHz	19 20 kHz	4800 Hz	2400 Hz
0	1	1	8	16 384 kHz	4 096 kHz	9600 Hz	2400 Hz	1200 Hz
1	0	0	16	8 192 kHz	2 048 kHz	4800 Hz	1200 Hz	600 Hz
1	0	1	32	4 096 kHz	1 024 kHz	2400 Hz	600 Hz	300 Hz
1	1	0	64	2 048 kHz	512 Hz	1200 Hz	300 Hz	150 Hz
1	1	1	128	1 024 kHz	256 Hz	600 Hz	150 Hz	75 Hz

NOTE· Table 5-2 illustrates how the SCI select bits can be used to provide lower transmitter baud rates by further dividing the prescaler output frequency The five examples are only representative samples In all cases, the baud rates shown are transmit baud rates (transmit clock) and the receiver clock is 16 times higher in frequency than the actual baud rate

SECTION 6
SERIAL PERIPHERAL INTERFACE (SPI)

6.1 INTRODUCTION AND FEATURES

6.1.1 Introduction

The serial peripheral interface (SPI) is an interface built into the MCU which allows several MCUs, or one MCU plus peripheral devices, to be interconnected within a single "black box" or on the same printed circuit board. In a serial peripheral interface (SPI), separate wires (signals) are required for data and clock. In the SPI format, the clock is not included in the data stream and must be furnished as a separate signal. An SPI system may be configured in one containing one master MCU and several slave MCUs, or in a system in which an MCU is capable of being either a master or a slave.

Figure 6-1 illustrates a typical multicomputer system configuration. Figure 6-1 represents a system of five different MCUs in which there are one master and four slaves (0, 1, 2, 3). In this system four basic lines (signals) are required for the MOSI (master out slave in), MISO (master in slave out), SCK (serial clock), and $\overline{SS}$ (slave select) lines.

6.1.2 Features

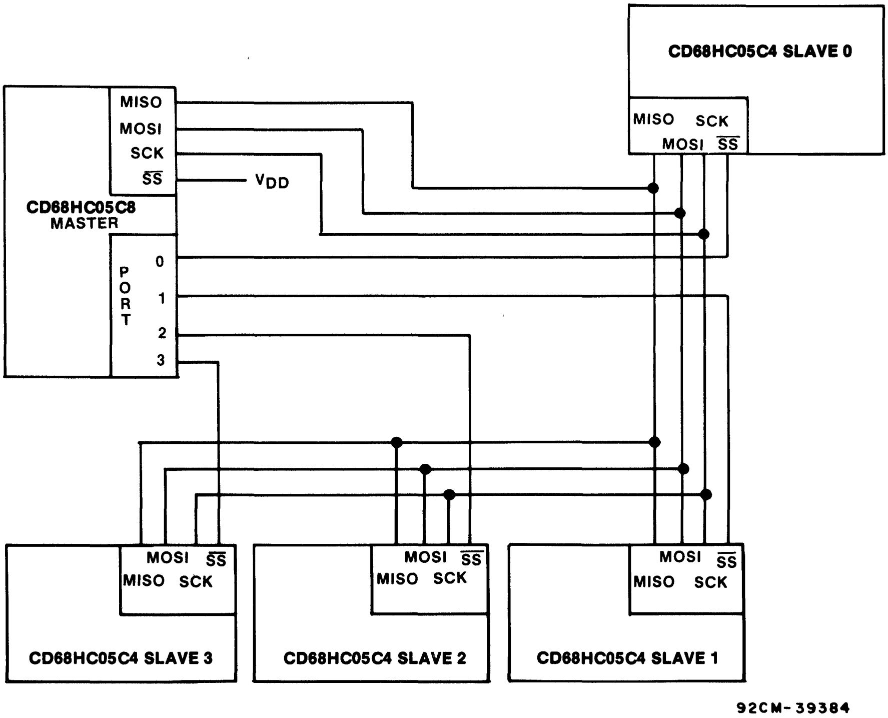
- Full duplex, three-wire synchronous transfers
- Master or slave operation
- 1.05 MHz (maximum) master bit frequency
- 2.1 MHz (maximum) slave bit frequency
- Four programmable master bit rates
- Programmable clock polarity and phase
- End of transmission interrupt flag
- Write collision flag protection
- Master-Master mode fault protection capability

6.2 SIGNAL DESCRIPTION

The four basic signals (MOSI, MISO, SCK, and $\overline{SS}$) discussed above are described in the following paragraphs. Each signal function is described for both the master and slave mode.

6.2.1 Master Out Slave In (MOSI)

The MOSI pin is configured as a data output in a master (mode) device and as a data input in a slave (mode) device. In this manner data is transferred serially from a master to a slave on this line; most



Single Master, Four Slaves

Figure 6-1. Master-Slave System Configuration

significant bit first, least significant bit last. The timing diagrams of Figure 6-2 summarize the SPI timing diagram shown in Section 9, and show the relationship between data and clock (SCK). As shown in Figure 6-2, four possible timing relationships may be chosen by using control bits CPOL and CPHA. The master device always allows data to be applied on the MOSI line a half-cycle before the clock edge (SCK) in order for the slave device to latch the data.

NOTE

Both the slave device(s) and a master device must be programmed to similar timing modes for proper data transfer.

When the master device transmits data to a second (slave) device via the MOSI line, the slave device responds by sending data to the master device via the MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal (one which is provided by the master device). Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receiver-full status bits. A single status bit (SPIF) is used to signify that the I/O operation is complete.

Configuration of the MOSI pin is a function of the MSTR bit in the serial peripheral control register (SPCR, location $0A). When a device is operating as a master, the MOSI pin is an output because the program in firmware sets the MSTR bit to a logic one.

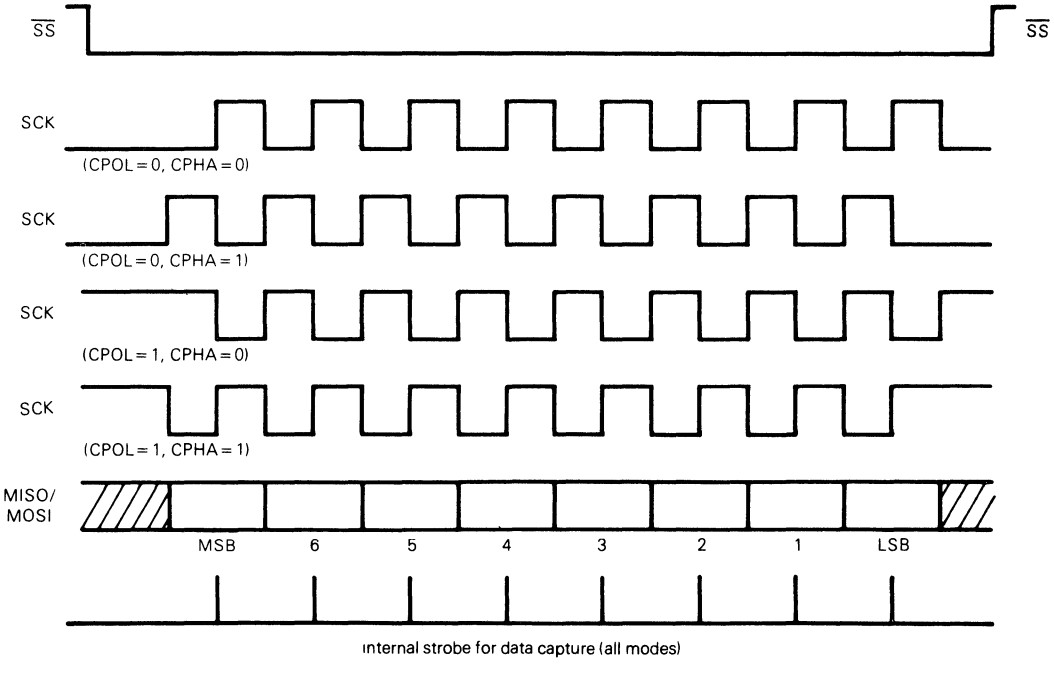


Figure 6-2. Data Clock Timing Diagram

CDP68HC05C4, CDP68HC05C8

6.2.2 Master In Slave Out (MISO)

The MISO pin is configured as an input in a master (mode) device and as an output in a slave (mode) device. In this manner data is transferred serially from a slave to a master on this line; most significant bit first, least significant bit last. The MISO pin of a slave device is placed in the high-impedance state if it is not selected by the master; i.e., its $\overline{SS}$ pin is a logic one. The timing diagram of Figure 6-2 shows the relationship between data and clock (SCK). As shown in Figure 6-2, four possible timing relationships may be chosen by using control bits CPOL and CPHA. The master device always allows data to be applied on the MOSI line a half-cycle before the clock edge (SCK) in order for the slave device to latch the data.

NOTE

> The slave device(s) and a master device must be programmed to similar timing modes for proper data transfer.

When the master device transmits data to a slave device via the MOSI line, the slave device responds by sending data to the master device via the MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal (one which is provided by the master device). Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receiver-full status bits. A single status bit (SPIF) in the serial peripheral status register (SPSR, location $0B) is used to signify that the I/O operation is complete.

In the master device, the MSTR control bit in the serial peripheral control register (SPCR, location $0A) is set to a logic one (by the program) to allow the master device to receive data on its MISO pin. In the slave device, its MISO pin is enabled by the logic level of the $\overline{SS}$ pin; i.e., if $\overline{SS}=1$ then the MISO pin is placed in the high-impedance state, whereas, if $\overline{SS}=0$ the MISO pin is an output for the slave device.

6.2.3 Slave Select ($\overline{SS}$)

The slave select ($\overline{SS}$) pin is a fixed input (PD5, pin 34), which receives an active low signal that is generated by the master device to enable slave device(s) to accept data. To ensure that data will be accepted by a slave device, the $\overline{SS}$ signal line must be a logic low prior to occurrence of SCK (system clock) and must remain low until after the last (eighth) SCK cycle. Figure 6-2 illustrates the relationship between SCK and the data for two different level combinations of CPHA, when $\overline{SS}$ is pulled low. These are: 1) with CPHA = 1 or 0, the first bit of data is applied to the MISO line for transfer, and 2) when CPHA = 0 the slave device is prevented from writing to its data register. Refer to the WCOL status flag in the serial peripheral status register (location $0B) description for further information on the effects that the $\overline{SS}$ input and CPHA control bit have on the I/O data register. A high level $\overline{SS}$ signal forces the MISO (master in slave out) line to the high-impedance state. Also, SCK and the MOSI (master out slave in) line are ignored by a slave device when its $\overline{SS}$ signal is high.

When a device is a master, it constantly monitors its $\overline{SS}$ signal input for a logic low. The master device will become a slave device any time its $\overline{SS}$ signal input is detected low. This ensures that there is only one master controlling the $\overline{SS}$ line for a particular system. When the $\overline{SS}$ line is detected low, it clears the MSTR control bit (serial peripheral control register, location $0A). Also, control bit SPE in the serial peripheral control register is cleared which causes the serial peripheral interface (SPI) to be disabled (port D SPI pins become inputs). The MODF flag bit in the serial peripheral status register (location $0B) is also set to indicate to the master device that another device is attempting to become a master. Two devices attempting to be outputs are normally the result of a software error; however, a system could be configured which would contain a default master which would automatically "take-over" and restart the system.

6.2.4 Serial Clock (SCK)

The serial clock is used to synchronize the movement of data both in and out of the device through its MOSI and MISO pins. The master and slave devices are capable of exchanging a data byte of information during a sequence of eight clock pulses. Since the SCK is generated by the master device, the SCK line becomes an input on all slave devices and synchronizes slave data transfer. The type of clock and its relationship to data are controlled by the CPOL and CPHA bits in the serial peripheral control register (location $0A) discussed below. Refer to Figure 6-2 for timing.

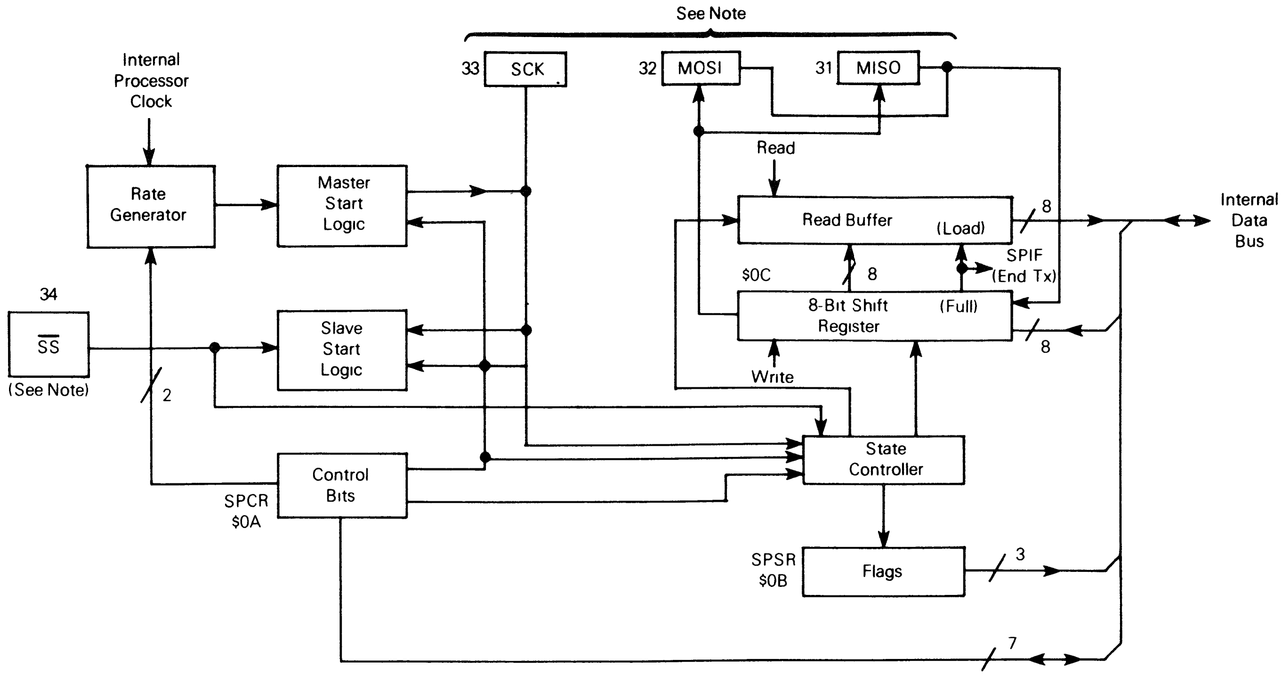
The master device generates the SCK through a circuit driven by the internal processor clock. Two bits (SPR0 and SPR1) in the serial peripheral control register (location $0A) of the master device select the clock rate. The master device uses the SCK to latch incoming slave device data on the MISO line and shifts out data to the slave device on the MOSI line. Both master and slave devices must be operated in the same timing mode as controlled by the CPOL and CPHA bit in the serial peripheral control register. In the slave device, SPR0, SPR1 have no effect on the operation of the serial peripheral interface. Timing is shown in Figure 6-2.

6.3 FUNCTIONAL DESCRIPTION

A block diagram of the serial peripheral interface (SPI) is shown in Figure 6-3. In a master configuration, the master start logic receives an input from the CPU (in the form of a write to the SPI rate generator) and originates the system clock (SCK) based on the internal processor clock. This clock is also used internally to control the state controller as well as the 8-bit shift register. As a master device, data is parallel loaded into the 8-bit shift register (from the internal bus) during a write cycle and then shifted out serially to the MOSI pin for application to the slave device(s). During a read cycle, data is applied serially from a slave device via the MISO pin to the 8-bit shift register After the 8-bit shift register is loaded, its data is parallel transferred to the read buffer and then is made available to the internal data bus during a CPU read cycle.

In a slave configuration, the slave start logic receives a logic low (from a master device) at the $\overline{SS}$ pin and a system clock input (from the same master device) at the SCK pin. Thus, the slave is synchronized with the master. Data from the master is received serially at the slave MOSI pin and loads the 8-bit shift register. After the 8-bit shift register is loaded, its data is parallel transferred to the read buffer and then is made available to the internal data bus during a CPU read cycle. During a write cycle, data is parallel loaded into the 8-bit shift register from the internal data bus and then shifted out serially to the MISO pin for application to the master device.

Figure 6-4 illustrates the MOSI, MISO, and SCK master-slave interconnections. Note that in Figure 6-4 the master $\overline{SS}$ pin is tied to a logic high and the slave $\overline{SS}$ pin is a logic low. Figure 6-1 provides a larger system connection for these same pins. Note that in Figure 6-1, all $\overline{SS}$ pins are connected to a port pin of a master/slave device. In this case any of the devices can be a slave.



NOTE The $\overline{SS}$, SCK, MOSI, and MISO are external pins which provide the following functions

a MOSI – Provides serial output to slave unit(s) when device is configured as a master Receives serial input from master unit when device is configured as a slave unit

b MISO – Receives serial input from slave unit(s) when device is configured as a master Provides serial output to master when device is configured as a slave unit

c SCK – Provides system clock when device is configured as a master unit Receives system clock when device is configured as a slave unit

d $\overline{SS}$ – Provides a logic low to select a slave device for a transfer with a master device

Figure 6-3. Serial Peripheral Interface Block Diagram

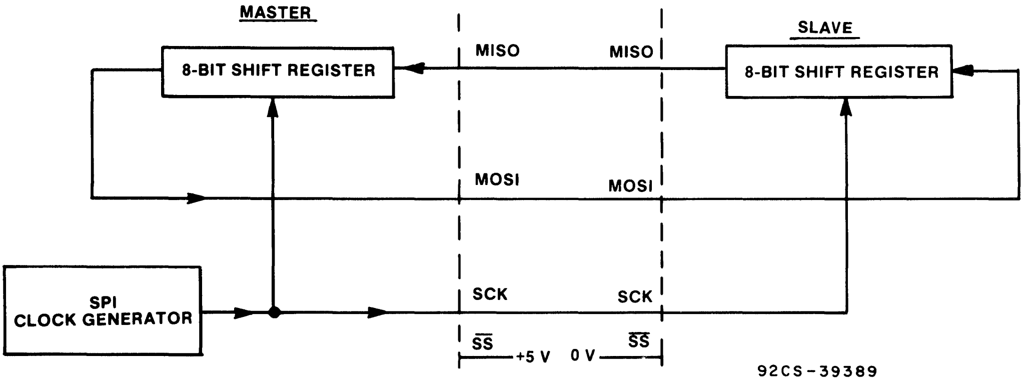


Figure 6-4. Serial Peripheral Interface Master-Slave Interconnection

6.4 REGISTERS

There are three registers in the serial parallel interface which provide control, status, and data storage functions. These registers which include the serial peripheral control register (SPCR, location $0A), serial peripheral status register (SPSR, location $0B), and serial peripheral data I/O register (SPDR, location $0C) are described below

6.4.1 Serial Peripheral Control Register (SPCR)

7	6	5	4	3	2	1	0	
SPIE	SPE	–	MSTR	CPOL	CPHA	SPR1	SPR0	$0A

The serial peripheral control register bits are defined as follows

B7, SPIE	When the serial peripheral interrupt enable bit is high, it allows the occurrence of a processor interrupt, and forces the proper vector to be loaded into the program counter if the serial peripheral status register flag bit (SPIF and/or MODF) is set to a logic one It does not inhibit the setting of a status bit The SPIE bit is cleared by reset.
B6, SPE	When the serial peripheral output enable control bit is set, all output drive is applied to the external pins and the system is enabled When the SPE bit is set, it enables the SPI system by connecting it to the external pins thus allowing it to interface with the external SPI bus. The pins that are defined as output depend on which mode (master or slave) the device is in. Because the SPE bit is cleared by reset, the SPI system is not connected to the external pins upon reset
B4, MSTR	The master bit determines whether the device is a master or a slave If the MSTR bit is a logic zero it indicates a slave device and a logic one denotes a master device. If the master mode is selected, the function of the SCK pin changes from an input to an output and the function of the MISO and MOSI pins are reversed. This allows the user to wire device pins MISO to MISO, and MOSI to MOSI, and SCK to SCK without incident The MSTR bit is cleared by reset; therefore, the device is always placed in the slave mode during reset.

B3, CPOL — The clock polarity bit controls the normal or steady state value of the clock when data is not being transferred. The CPOL bit affects both the master and slave modes. It must be used in conjunction with the clock phase control bit (CPHA) to produce the wanted clock-data relationship between a master and a slave device. When the CPOL bit is a logic zero, it produces a steady state low value at the SCK pin of the master device. If the CPOL bit is a logic one, a high value is produced at the SCK pin of the master device when data is not being transferred. The CPOL bit is not affected by reset. Refer to Figure 6-2.

B2, CPHA — The clock phase bit controls the relationship between the data on the MISO and MOSI pins and the clock produced or received at the SCK pin. This control has effect in both the master and slave modes. It must be used in conjunction with the clock polarity control bit (CPOL) to produce the wanted clock-data relation. The CPHA bit in general selects the clock edge which captures data and allows it to change states. It has its greatest impact on the first bit transmitted (MSB) in that it does or does not allow a clock transition before the first data capture edge. The CPHA bit is not affected by reset. Refer to Figure 6-2.

B1, SPR1
B0, SPR0 — These two serial peripheral rate bits select one of four baud rates to be used as SCK if the device is a master; however they have no effect in the slave mode. The slave device is capable of shifting data in and out at a maximum rate which is equal to the CPU clock. A rate table is given below for the generation of the SCK from the master. The SPR1 and SPR0 bits are not affected by reset.

SPR1	SPR0	Internal Processor Clock Divide By
0	0	2
0	1	4
1	0	16
1	1	32

6.4.2 Serial Peripheral Status Register (SPSR)

7	6	5	4	3	2	1	0	
SPIF	WCOL	–	MODF	–	–	–	–	$0B

The status flags which generate a serial peripheral interface (SPI) interrupt may be blocked by the SPIE control bit in the serial peripheral control register. The WCOL bit does not cause an interrupt. The serial peripheral status register bits are defined as follows:

B7, SPIF — The serial peripheral data transfer flag bit notifies the user that a data transfer between the device and an external device has been completed. With the completion of the data transfer, SPIF is set, and if SPIE is set, a serial peripheral interrupt (SPI) is generated. During the clock cycle that SPIF is being set, a copy of the received data byte in the shift register is moved to a buffer. When the data register is read, it is the buffer that is read. During an overrun condition, when the master device has sent several bytes of data and the slave device has not responded to the first SPIF, only the first byte sent is contained in the receiver buffer and all other bytes are lost.

The transfer of data is initiated by the master device writing its serial peripheral data register.

Clearing the SPIF bit is accomplished by a software sequence of accessing the serial peripheral status register while SPIF is set and followed by a write to or a read of the serial peripheral data register. While SPIF is set, all writes to the serial peripheral data register are inhibited until the serial peripheral status register is read. This occurs in the master device. In the slave device, SPIF can be cleared (using a similar sequence) during a second transmission; however, it must be cleared before the second SPIF in order to prevent an overrun condition. The SPIF bit is cleared by reset.

B6, WCOL The function of the write collision status bit is to notify the user that an attempt was made to write the serial peripheral data register while a data transfer was taking place with an external device. The transfer continues uninterrupted; therefore, a write will be unsuccessful. A "read collision" will never occur since the received data byte is placed in a buffer in which access is always synchronous with the MCU operation. If a "write collision" occurs, WCOL is set but no SPI interrupt is generated. The WCOL bit is a status flag only.

Clearing the WCOL bit is accomplished by a software sequence of accessing the serial peripheral status register while WCOL is set, followed by 1) a read of the serial peripheral data register prior to the SPIF bit being set, or 2) a read or write of the serial peripheral data register after the SPIF bit is set. A write to the serial peripheral data register (SPDR) prior to the SPIF bit being set, will result in generation of another WCOL status flag. Both the SPIF and WCOL bits will be cleared in the same sequence If a second transfer has started while trying to clear (the previously set) SPIF and WCOL bits with a clearing sequence containing a write to the serial peripheral data register, only the SPIF bit will be cleared.

A collision of a write to the serial peripheral data register while an external data transfer is taking place can occur in both the master mode and the slave mode, although with proper programming the master device should have sufficient information to preclude this collision.

Collision in the master device is defined as a write of the serial peripheral data register while the internal rate clock (SCK) is in the process of transfer. The signal on the $\overline{SS}$ pin is always high on the master device.

A collision in a slave device is defined in two separate modes. One problem arises in a slave device when the CPHA control bit is a logic zero. When CPHA is a logic zero, data is latched with the occurrence of the first clock transition. The slave device does not have any way of knowing when that transition will occur; therefore, the slave device collision occurs when it attempts to write the serial peripheral data register after its $\overline{SS}$ pin has been pulled low. The $\overline{SS}$ pin of the slave device freezes the data in its serial peripheral data register and does not allow it to be altered if the CPHA bit is a logic zero. The master device must raise the $\overline{SS}$ pin of the slave device high between each byte it transfers to the slave device

The second collision mode is defined for the state of the CPHA control bit being a logic one. With the CPHA bit set, the slave device will be receiving a clock (SCK) edge prior to the latch of the first data transfer. This first clock edge will freeze the data in the slave device I/O register and allow the msb onto the external MISO pin of the slave device. The $\overline{SS}$ pin low state enables the slave device but the drive onto the MISO pin does not take place until the first data transfer clock edge. The WCOL bit will only be set if the I/O register is accessed while a transfer is taking place. By definition of the second collision mode, a master device might hold a slave device $\overline{SS}$ pin low during a transfer of several bytes of data without a problem.

A special case of WCOL occurs in the slave device. This happens when the master device starts a transfer sequence (an edge or SCK for CPHA = 1; or an active $\overline{SS}$ transition for CPHA = 0) at the same time the slave device CPU is writing to its serial peripheral interface data register. In this case it is assumed that the data byte written (in the slave device serial peripheral interface) is lost and the contents of the slave device read buffer becomes the byte that is transferred. Because the master device receives back the last byte transmitted, the master device can detect that a fatal WCOL occurred.

Since the slave device is operating asynchronously with the master device, the WCOL bit may be used as an indicator of a collision occurrence. This helps alleviate the user from a strict real-time programming effort. The WCOL bit is cleared by reset.

B4, MODF The function of the mode fault flag is defined for the master mode (device). If the device is a slave device the MODF bit will be prevented from toggling from a logic zero to a logic one; however, this does not prevent the device from being in the slave mode with the MODF bit set. The MODF bit is normally a logic zero and is set only when the master device has its $\overline{SS}$ pin pulled low. Toggling the MODF bit to a logic one affects the internal serial peripheral interface (SPI) system in the following ways:

1. MODF is set and SPI interrupt is generated if SPIE = 1.
2. The SPE bit is forced to a logic zero. This blocks all output drive from the device, disables the SPI system.
3. The MSTR bit is forced to a logic zero, thus forcing the device into the slave mode.

Clearing the MODF is accomplished by a software sequence of accessing the serial peripheral status register while MODF is set followed by a write to the serial peripheral control register. Control bits SPE and MSTR may be restored to their original set state during this clearing sequence or after the MODF bit has been cleared. Hardware does not allow the user to set the SPE and MSTR bit while MODF is a logic one unless it is during the proper clearing sequence. The MODF flag bit indicates that there might have been a multi-master conflict for system control and allows a proper exit from system operation to a reset or default system state. The MODF bit is cleared by reset.

6.4.3 Serial Peripheral Data I/O Register (SPDR)

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td></td></tr>
<tr><td colspan="8">Serial Peripheral Data I/O Register</td><td>$0C</td></tr>
</table>

The serial peripheral data I/O register is used to transmit and receive data on the serial bus. Only a write to this register will initiate transmission/reception of another byte and this will only occur in the master device. A slave device writing to its data I/O register will not initiate a transmission. At the completion of transmitting a byte of data, the SPIF status bit is set in both the master and slave devices. A write or read of the serial peripheral data I/O register, after accessing the serial peripheral status register with SPIF set, will clear SPIF.

During the clock cycle that the SPIF bit is being set, a copy of the received data byte in the shift register is being moved to a buffer. When the user reads the serial peripheral data I/O register, the buffer is actually being read. During an overrun condition, when the master device has sent several bytes of data and the slave device has not internally responded to clear the first SPIF, only the first byte is contained in the receive buffer of the slave device; all others are lost. The user may read the buffer at any time. The first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated or an overrun condition will exist.

A write to the serial peripheral data I/O register is not buffered and places data directly into the shift register for transmission.

The ability to access the serial peripheral data I/O register is limited when a transmission is taking place. It is important to read the discussion defining the WCOL and SPIF status bits to understand the limits on using the serial peripheral data I/O register.

6.5 SERIAL PERIPHERAL INTERFACE (SPI) SYSTEM CONSIDERATIONS

There are two types of SPI systems; single master system and multi-master-systems. Figure 6-1 illustrates both of these systems and a discussion of each is provided below.

Figure 6-1a illustrates how a typical single master system may be configured, using an CDP6805 HCMOS family device as the master and four CDP6805 HCMOS family devices as slaves. As shown, the MOSI, MISO, and SCK pins are all wired to equivalent pins on each of the five devices. The master device generates the SCK clock, the slave devices all receive it. Since the CDP6805 HCMOS master device is the bus master, it internally controls the function of its MOSI and MISO lines, thus writing data to the slave devices on the MOSI and reading data from the slave devices on the MISO lines. The master device selects the individual slave devices by using four pins of a parallel port to control the four $\overline{SS}$ pins of the slave devices. A slave device is selected when the master device pulls its $\overline{SS}$ pin low. The $\overline{SS}$ pins are pulled high during reset since the master device ports will be forced to be inputs at that time, thus disabling the slave devices Note that the slave devices do not have to be enabled in a mutually exclusive fashion except to prevent bus contention on the MISO line. For example, three slave devices, enabled for a transfer, are permissible if only one has the capability of being read by the master. An example of this is a write to several display drivers to clear a display with a single I/O operation. To ensure that proper data transmission is occurring between the master device and a slave device, the master device may have the slave device respond with a previously received data byte (this data byte could be inverted or at least be a byte that is different from the last one sent by the master device). The master device will always receive the previous byte back from the slave device if all MISO and MOSI lines are connected and the slave has not written its data I/O register. Other transmission security methods might be defined using ports for handshake lines or data bytes with command fields.

A multi-master system may also be configured by the user. A system of this type is shown in Figure 6-1b. An exchange of master control could be implemented using a handshake method through the I/O ports or by an exchange of code messages through the serial peripheral interface system. The major device control that plays a part in this system is the MSTR bit in the serial peripheral control register and the MODF bit in the serial peripheral status register.

SECTION 7
EFFECTS OF STOP AND WAIT MODES ON THE TIMER AND SERIAL SYSTEMS

7.1 INTRODUCTION

The STOP and WAIT instructions have different effects on the programmable timer, serial communications interface (SCI), and serial peripheral interface (SPI) systems. These different effects are discussed separately below.

7.2 STOP MODE

When the processor executes the STOP instruction, the internal oscillator is turned off. This halts all internal CPU processing including the operation of the programmable timer, serial communications interface, and serial peripheral interface The only way for the MCU to "wake up" from the stop mode is by receipt of an external interrupt (logic low on $\overline{\text{IRQ}}$ pin) or by the detection of a reset (logic low on $\overline{\text{RESET}}$ pin or a power-on reset). The effects of the stop mode on each of the MCU systems (Timer, SCI, and SPI) are described separately

7.2.1 Timer During Stop Mode

When the MCU enters the stop mode, the timer counter stops counting (the internal processor clock is stopped) and remains at that particular count value until the stop mode is exited by an interrupt (if exited by reset the counter is forced to $FFFC) If the stop mode is exited by an external low on the $\overline{\text{IRQ}}$ pin, then the counter resumes from its stopped value as if nothing had happened Another feature of the programmable timer, in the stop mode, is that if at least one valid input capture edge occurs at the TCAP pin, the input capture detect circuitry is armed. This action does not set any timer flags or "wake up" the MCU, but when the MCU does "wake up" there will be an active input capture flag (and data) from that first valid edge which occurred during the stop mode. If the stop mode is exited by an external reset (logic low on $\overline{\text{RESET}}$ pin), then no such input capture flag or data action takes place even if there was a valid input capture edge (at the TCAP pin) during the MCU stop mode.

7.2.2 SCI During Stop Mode

When the MCU enters the stop mode, the baud rate generator which drives the receiver and transmitter is shut down. This essentially stops all SCI activity The receiver is unable to receive and transmitter is unable to transmit. If the STOP instruction is executed during a transmitter transfer, that transfer is halted. When the stop mode is exited, that particular transmission resumes (if the exit is the result of a low input to the $\overline{\text{IRQ}}$ pin). Since the previous transmission resumes after an $\overline{\text{IRQ}}$ interrupt stop mode exit, the user should ensure that the SCI transmitter is in the idle state when the STOP instruction is executed If the receiver is receiving data when the STOP instruction is executed, received data sampling is stopped (baud rate generator stops) and the rest of the data is lost. For the above reasons, all SCI transactions should be in the idle state when the STOP instruction is executed.

7.2.3 SPI During Stop Mode

When the MCU enters the stop mode, the baud rate generator which drives the SPI shuts down. This essentially stops all master mode SPI operation, thus the master SPI is unable to transmit or receive any data. If the STOP instruction is executed during an SPI transfer, that transfer is halted until the MCU exits the stop mode (provided it is an exit resulting from a logic low on the $\overline{\text{IRQ}}$ pin). If the stop mode is exited by a reset, then the appropriate control/status bits are cleared and the SPI is disabled. If the device is in the slave mode when the STOP instruction is executed, the slave SPI will still operate. It can still accept data and clock information in addition to transmitting its own data back to a master device.

At the end of a possible transmission with a slave SPI in the stop mode, no flags are set until a logic low $\overline{\text{IRQ}}$ input results in an MCU "wake up". Caution should be observed when operating the SPI (as a slave) during the stop mode because none of the protection circuitry (write collision, mode fault, etc.) is active.

It should also be noted that when the MCU enters the stop mode all enabled output drivers (TDO, TCMP, MISO, MOSI, and SCK ports) remain active and any sourcing currents from these outputs will be part of the total supply current required by the device.

7.3 WAIT MODE

When the MCU enters the wait mode, the CPU clock is halted. All CPU action is suspended; however, the timer, SCI, and SPI systems remain active. In fact an interrupt from the timer, SCI, or SPI (in addition to a logic low on the $\overline{\text{IRQ}}$ or $\overline{\text{RESET}}$ pins) causes the processor to exit the wait mode. Since the three systems mentioned above operate as they do in the normal mode, only a general discussion of the wait mode is provided below.

The wait mode power consumption depends on how many systems are active. The power consumption will be highest when all the systems (timer, TCMP, SCI, and SPI) are active. The power consumption will be the least when the SCI and SPI systems are disabled (timer operation cannot be disabled in the wait mode). If a non-reset exit from the wait mode is performed (i.e., timer overflow interrupt exit), the state of the remaining systems will be unchanged. If a reset exit from the wait mode is performed all the systems revert to the disabled reset state.

SECTION 8
INSTRUCTION SET AND ADDRESSING MODES

8.1 INSTRUCTION SET

The MCU has a set of 62 basic instructions. They can be divided into five different types register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables

All of the instructions used in the CDP6805 CMOS Family are used in the CDP68HC05C4 MCU, plus an additional one; the multiply (MUL) instruction This instruction allows for unsigned multiplication of the contents of the accumulator (A) and the index register (X) The high order product is then stored in the index register and the low order product is stored in the accumulator. A detailed definition of the MUL instruction is shown below

Operation: $X{:}A \leftarrow X*A$

Description: Multiplies the eight bits in the index register by the eight bits in the accumulator to obtain a 16-bit unsigned number in the concatenated accumulator and index register.

Condition Codes:

H: Cleared
I: Not affected
N: Not affected
Z: Not affected
C. Cleared

Source Form(s): MUL

Addressing Mode	Cycles	Bytes	Opcode
Inherent	11	1	$42

8.1.1 Register/Memory Instructions

Most of these instructions use two operands. The first operand is either the accumulator or the index register. The second operand is obtained from memory using one of the addressing modes. The operand for the jump unconditional (JMP) and jump to subroutine (JSR) instructions is the program counter. Refer to Table 8-1.

8.1.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read-modify-write sequence since it does not modify the value. Refer to Table 8-2.

Table 8-1. Register/Memory Instructions

		Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
Function	Mnem.	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from Memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in Memory	STA	–	–	–	B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in Memory	STX	–	–	–	BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add Memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add Memory and Carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract Memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND Memory to A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR Memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump Unconditional	JMP	–	–	–	BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to Subroutine	JSR	–	–	–	BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

Table 8-2. Read-Modify-Write Instructions

		Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (2's Complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate Left Thru Carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate Right Thru Carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical Shift Left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical Shift Right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic Shift Right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for Negative or Zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5
Multiply	MUL	42	1	11	–	–	–	–	–	–	–	–	–	–	–	–

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8.1.3 Branch Instructions

Most branch instructions test the state of the condition code register and if certain criteria are met, a branch is executed. This adds an offset between − 127 and + 128 to the current program counter. Refer to Table 8-3.

Table 8-3. Branch Instructions

Function	Mnemonic	Relative Addressing Mode Op Code	 # Bytes	 # Cycles
Branch Always	BRA	20	2	3
Branch Never	BRN	21	2	3
Branch IFF Higher	BHI	22	2	3
Branch IFF Lower or Same	BLS	23	2	3
Branch IFF Carry Clear	BCC	24	2	3
(Branch IFF Higher or Same)	(BHS)	24	2	3
Branch IFF Carry Set	BCS	25	2	3
(Branch IFF Lower)	(BLO)	25	2	3
Branch IFF Not Equal	BNE	26	2	3
Branch IFF Equal	BEQ	27	2	3
Branch IFF Half Carry Clear	BHCC	28	2	3
Branch IFF Half Carry Set	BHCS	29	2	3
Branch IFF Plus	BPL	2A	2	3
Branch IFF Minus	BMI	2B	2	3
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	3
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	3
Branch IFF Interrupt Line is Low	BIL	2E	2	3
Branch IFF Interrupt Line is High	BIH	2F	2	3
Branch to Subroutine	BSR	AD	2	6

8.1.4 Bit Manipulation Instructions

The MCU is capable of setting or clearing any bit which resides in the first 256 bytes of the memory space except for ROM, port D data location ($03), serial peripheral status register ($0B), serial communications status register ($10), timer status register ($13), and timer input capture register ($14-$15). All port registers, port DDRs, timer, two serial systems, on-chip RAM, and 48 bytes of ROM reside in the first 256 bytes (page zero). An additional feature allows the software to test and branch on the state of any bit within the first 256 locations. The bit set, bit clear, and bit test and branch functions are all implemented with a single instruction. For the test and branch instructions, the value of the bit tested is automatically placed in the carry bit of the condition code register. Refer to Table 8-4.

Table 8-4. Bit Manipulation Instructions

		Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is Set	BRSET n (n=0 7)	–	–	–	2•n	3	5
Branch IFF Bit n is Clear	BRCLR n (n=0 7)	–	–	–	01+2•n	3	5
Set Bit n	BSET n (n=0 7)	10+2•n	2	5	–	–	–
Clear Bit n	BCLR n (n=0 7)	11+2•n	2	5	–	–	–

8.1.5 Control Instructions

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 8-5.

Table 8-5. Control Instructions

Function	Mnemonic	Inherent		
		Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	10
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

8.1.6 Alphabetical Listing

The complete instruction set is given in alphabetical order in Table 8-6.

8.1.7 Opcode Map

Table 8-7 is an opcode map for the instructions used on the MCU.

8.2 ADDRESSING MODES

The MCU uses ten different addressing modes to provide the programmer with an opportunity to optimize the code to all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables, and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions, while the longest instructions (three bytes) permit accessing tables throughout memory. Short absolute (direct) and long absolute (extended) addressing are also included. One and two byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory. Table 8-7 shows the addressing modes for each instruction, with the effects each instruction has on the condition code register.

The term "effective address" (EA) is used in describing the various addressing modes, and is defined as the byte address to or from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate "contents of" the location or register referred to; e g , (PC) indicates the contents of the location pointed to by the PC. An arrow indicates "is replaced by", and a colon indicates concatenation of two bytes.

Table 8-6. Instruction Set

Mnemonic	Addressing Modes										Condition Codes				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/ Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
ADD		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
AND		X	X	X		X	X	X			●	●	Λ	Λ	●
ASL	X		X			X	X				●	●	Λ	Λ	Λ
ASR	X		X			X	X				●	●	Λ	Λ	Λ
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	Λ	Λ	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	Λ
BRSET										X	●	●	●	●	Λ
BSET									X		●	●	●	●	●
BSR					X						●	●	●	●	●
CLC	X										●	●	●	●	0
CLI	X										●	0	●	●	●
CLR	X		X			X	X				●	●	0	1	●
CMP		X	X	X		X	X	X			●	●	Λ	Λ	Λ

COM	X		X			X	X				●	●	Λ	Λ	1
CPX		X	X	X		X	X	X			●	●	Λ	Λ	Λ
DEC	X		X			X	X				●	●	Λ	Λ	●
EOR		X	X	X		X	X	X			●	●	Λ	Λ	●
INC	X		X			X	X				●	●	Λ	Λ	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	Λ	Λ	●
LDX		X	X	X		X	X	X			●	●	Λ	Λ	●
LSL	X		X			X	X				●	●	Λ	Λ	Λ
LSR	X		X			X	X				●	●	0	Λ	Λ
MUL	X										0	●	●	●	0
NEG	X		X			X	X				●	●	Λ	Λ	Λ
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	Λ	Λ	●
ROL	X		X			X	X				●	●	Λ	Λ	Λ
ROR	X		X			X	X				●	●	Λ	Λ	Λ
RSP	X										●	●	●	●	●
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	Λ	Λ	●
STOP	X										●	0	●	●	●
STX			X	X		X	X	X			●	●	Λ	Λ	●
SUB		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	Λ	Λ	●
TXA	X										●	●	●	●	●
WAIT	X										●	0	●	●	●

Condition Code Symbols

H	Half Carry (From Bit 3)	Λ	Test and Set if True Cleared Otherwise
I	Interrupt Mask	●	Not Affected
N	Negate (Sign Bit)	?	Load CC Register From Stack
Z	Zero	0	Cleared
C	Carry/Borrow	1	Set

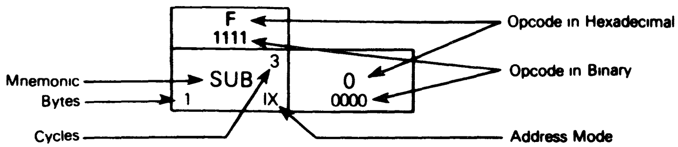
Table 8-7. HCMOS Instruction Set Opcode Map

	Bit Manipulation		Branch	Read/Modify/Write					Control		Register/Memory						
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
Hi / Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Hi / Low
0 0000	5 BRSET0 3 BTB	5 BSET0 2 BSC	3 BRA 2 REL	5 NEG 2 DIR	3 NEG 1 INH	3 NEG 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0 0000
1 0001	5 BRCLR0 3 BTB	5 BCLR0 2 BSC	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1 0001
2 0010	5 BRSET1 3 BTB	5 BSET1 2 BSC	3 BHI 2 REL		11 MUL 1 INH						2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2 0010
3 0011	5 BRCLR1 3 BTB	5 BCLR1 2 BSC	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3 0011
4 0100	5 BRSET2 3 BTB	5 BSET2 2 BSC	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4 0100
5 0101	5 BRCLR2 3 BTB	5 BCLR2 2 BSC	3 BCS 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5 0101
6 0110	5 BRSET3 3 BTB	5 BSET3 2 BSC	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6 0110
7 0111	5 BRCLR3 3 BTB	5 BCLR3 2 BSC	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7 0111
8 1000	5 BRSET4 3 BTB	5 BSET4 2 BSC	3 BHCC 2 REL	5 LSL 2 DIR	3 LSLA 1 INH	3 LSLX 1 INH	6 LSL 2 IX1	5 LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8 1000
9 1001	5 BRCLR4 3 BTB	5 BCLR4 2 BSC	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9 1001
A 1010	5 BRSET5 3 BTB	5 BSET5 2 BSC	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A 1010
B 1011	5 BRCLR5 3 BTB	5 BCLR5 2 BSC	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B 1011
C 1100	5 BRSET6 3 BTB	5 BSET6 2 BSC	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C 1100
D 1101	5 BRCLR6 3 BTB	5 BCLR6 2 BSC	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D 1101
E 1110	5 BRSET7 3 BTB	5 BSET7 2 BSC	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E 1110
F 1111	5 BRCLR7 3 BTB	5 BCLR7 2 BSC	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F 1111

Abbreviations for Address Modes

INH	Inherent
A	Accumulator
X	Index Register
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
BTB	Bit Test and Branch
IX	Indexed (No Offset)
IX1	Indexed, 1 Byte (8-Bit) Offset
IX2	Indexed, 2 Byte (16-Bit) Offset

LEGEND



8.2.1 Inherent

In inherent instructions, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, and no other arguments, are included in this mode.

8.2.2 Immediate

In immediate addressing, the operand is contained in the byte immediately following the opcode. Immediate addressing is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

$$EA = PC + 1;\ PC \leftarrow PC + 2$$

8.2.3 Direct

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two byte instruction. This includes all on-chip RAM and I/O registers, and 128 bytes of on-chip ROM. Direct addressing is efficient in both memory and time.

$$EA = (PC + 1);\ PC \leftarrow PC + 2$$

$$\text{Address Bus High} \leftarrow 0;\ \text{Address Bus Low} \leftarrow (PC + 1)$$

8.2.4 Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing modes are capable of referencing arguments anywhere in memory with a single three-byte instruction.

$$EA = (PC + 1):(PC + 2);\ PC \leftarrow PC + 3$$

$$\text{Address Bus High} \leftarrow (PC + 1);\ \text{Address Bus Low} \leftarrow (PC + 2)$$

8.2.5 Indexed, No Offset

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is used to move a pointer through a table or to address a frequently referenced RAM or I/O location.

$$EA = X;\ PC \leftarrow PC + 1$$

$$\text{Address Bus High} \leftarrow 0;\ \text{Address Bus Low} \leftarrow X$$

8.2.6 Indexed, 8-Bit Offset

Here the EA is obtained by adding the contents of the byte following the opcode to that of the index register; therefore, the operand is located anywhere within the lowest 511 memory locations. For example, this mode of addressing is useful for selecting the mth element in a n element table. All instructions are two bytes. The content of the index register (X) is not changed. The content of

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(PC+1) is an unsigned 8-bit integer. One byte offset indexing permits look-up tables to be easily accessed in either RAM or ROM.

$$EA = X + (PC+1);\ PC \leftarrow PC+2$$
$$\text{Address Bus High} \leftarrow K;\ \text{Address Bus Low} \leftarrow X + (PC+1)$$

where:

K = The carry from the addition of X + (PC + 1)

8.2.7 Indexed, 16-Bit Offset

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed 8-bit offset, except that this three byte instruction allows tables to be anywhere in memory (e.g., jump tables in ROM). The content of the index register is not changed.

$$EA = X + [(PC+1):(PC+2))];\ PC \leftarrow PC+3$$
$$\text{Address Bus High} \leftarrow (PC+1) + K;$$
$$\text{Address Bus Low} \leftarrow X + (PC+2)$$

where:

K = The carry from the addition of X + (PC + 2)

8.2.8 Relative

Relative addressing is only used in branch instructions. In relative addressing, the content of the 8-bit signed byte following the opcode (the offset) is added to the PC if and only if the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is limited to the range of − 126 to + 129 bytes from the branch instruction opcode location.

$$EA = PC + 2 + (PC+1);\ PC \leftarrow EA \text{ if branch taken;}$$
$$\text{otherwise, } EA = PC \leftarrow PC+2$$

8.2.9 Bit Set/Clear

Direct addressing and bit addressing are combined in instructions which set and clear individual memory and I/O bits. In the bit set and clear instructions, the byte is specified as a direct address in the location following the opcode. The first 256 addressable locations are thus accessed. The bit to be modified within that byte is specified in the first three bits of the opcode. The bit set and clear instructions occupy two bytes, one for the opcode (including the bit number) and the other to address the byte which contains the bit of interest.

$$EA = (PC+1);\ PC \leftarrow PC+2$$
$$\text{Address Bus High} \leftarrow 0;\ \text{Address Bus Low} \leftarrow (PC+1)$$

8.2.10 Bit Test and Branch

Bit test and branch is a combination of direct addressing, bit set/clear addressing, and relative addressing. The actual bit to be tested, within the byte, is specified within the low order nibble of the opcode. The address of the data byte to be tested is located via a direct address in the location following the opcode byte (EA1). The signed relative 8-bit offset is in the third byte (EA2) and is added to the PC if the specified bit is set or cleared in the specified memory location. This single three byte instruction allows the program to branch based on the condition of any bit in the first 256 locations of memory.

$$EA1 = (PC + 1)$$

$$\text{Address Bus High} \leftarrow 0;\ \text{Address Bus Low} \leftarrow (PC + 1)$$

$$EA2 = PC + 3 + (PC + 2);\ PC \leftarrow EA2 \text{ if branch taken;}$$

$$\text{otherwise, } PC \leftarrow PC + 3$$

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SECTION 9
ELECTRICAL SPECIFICATIONS

9.1 INTRODUCTION

This section contains the electrical specifications and associated timing information for the CDP68HC05C4

9.2 MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.5 to +7	V
Input Voltage	V_{in}	V_{SS}-0.3 to V_{DD}+0.3	V
Self-Check Mode ($\overline{IRQ}$ Pin Only)	V_{in}	V_{SS}-0.3 to 2xV_{DD}+0.3	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	I	25	mA
Operating Temperature Range	T_A	-40 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e g , either V_{SS} or V_{DD})

9.3 THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance	θ_{JA}		
Ceramic Dual-In-Line		50	
Plastic Dual-In-Line		100	°C/W
Plastic Chip Carrier		70	

V_{DD}=4.5 V

Pins	R1	R2	C
PA0-PA7, PB0-PB7, PC0-PC7, PD6	3 26 kΩ	2 38 kΩ	50 pF
PD1-PD4	1 9 kΩ	2 26 kΩ	200 pF

V_{DD}=3.0 V

Pins	R1	R2	C
PA0-PA7, PB0-PB7, PC0-PC7, PD6	10 91 kΩ	6 32 kΩ	50 pF
PD1-PD4	6 kΩ	6 kΩ	200 pF

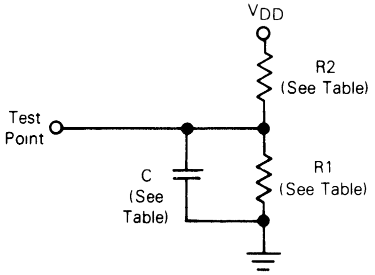

Figure 9-1. Equivalent Test Load

9.4 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$, Watts – Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins – User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is

$$P_D = K - (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A

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9.5 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5 V dc ± 10%, V_{SS} = 0 V dc, T_A = -40°C to +125°C unless otherwise noted)

Characteristic	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Output Voltage, $I_{Load} \le 10\ \mu A$	V_{OL}	—	—	0.1	V
	V_{OH}	V_{DD}-0.1	—	—	
Output High Voltage					V
(I_{Load}=0.8 mA) PA0-PA7, PB0-PB7, PC0-PC7, TCMP (See Figure 9-2)	V_{OH}	V_{DD}-0.8	—	—	
(I_{Load}=1.6 mA) PD1-PD4 (See Figure 9-3)	V_{OH}	V_{DD}-0.8	—	—	
Output Low Voltage (See Figure 9-4) (I_{Load}=1.6 mA) PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD4, TCMP	V_{OL}	—	—	0.4	V
Input High Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input Low Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PD7, TCAP, $\overline{IRQ}$ $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
Data Retention Mode (0° to 70°C)	V_{RM}	2	—	—	V
Supply Current (See Notes)					
Run (See Figures 9-5 and 9-6)	I_{DD}	—	3.5	7	mA
Wait (See Figures 9-5 and 9-6)	I_{DD}	—	1.6	4	mA
Stop (See Figure 9-6)					
25°C	I_{DD}	—	2	50	μA
-40° to +125°C	I_{DD}	—	—	250	μA
I/O Ports Hi-Z Leakage Current PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD4	I_{IL}	—	—	±10	μA
Input Current $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0, PD5, PD7	I_{in}	—	—	±1	μA
Capacitance					pF
Ports (as Input or Output)	C_{out}	—	—	12	
$\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0-PD5, PD7	C_{in}	—	—	8	

NOTES:

1. All values shown reflect average measurements.
2. Typical values at midpoint of voltage range, 25°C only.
3. Wait I_{DD}: Only timer system active (SPE=TE=RE=0). If SPI, SCI active (SPE=TE=RE=1) add 10% current draw.
4. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square-wave clock source (f_{OSC}=4.2 MHz), all inputs 0.2 V from rail, no DC loads, less than 50 pF on all outputs, C_L=20 pF on OSC2.
5. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL}=0.2 V, V_{IH}=V_{DD}-0.2 V.
6. Stop I_{DD} measured with OSC1=V_{SS}.
7. Wait I_{DD} is affected linearly by the OSC2 capacitance.

9.6 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3 V dc ± 10%, V_{SS} = 0 V dc, T_A = -40°C to +125°C unless otherwise noted)

Characteristic	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Output Voltage, $I_{Load} \leq 10\ \mu A$	V_{OL}	—	—	0.1	V
	V_{OH}	V_{DD}-0.1	—	—	
Output High Voltage					
(I_{Load}=0.2 mA) PA0-PA7, PB0-PB7, PC0-PC7, TCMP (See Figure 9-2)	V_{OH}	V_{DD}-0.3	—	—	V
(I_{Load}=0.4 mA) PD1-PD4 (See Figure 9-3)	V_{OH}	V_{DD}-0.3	—	—	
Output Low Voltage (See Figure 9-4) (I_{Load}=0.4 mA) PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD4, TCMP	V_{OL}	—	—	0.3	V
Input High Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input Low Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PD7, TCAP, $\overline{IRQ}$ $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
Data Retention Mode (0° to 70°C)	V_{RM}	2	—	—	V
Supply Current (See Notes)					
Run (See Figures 9-5 and 9-7)	I_{DD}	—	1	2.5	mA
Wait (See Figures 9-5 and 9-7)	I_{DD}	—	1	2.5	mA
Stop (See Figure 9-7)					
25°C	I_{DD}	—	0.5	1.4	µA
-40° to +125°C	I_{DD}	—	—	175	µA
I/O Ports Hi-Z Leakage Current PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD4	I_{IL}	—	—	±10	µA
Input Current $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0, PD5, PD7	I_{in}	—	—	±1	µA
Capacitance					
Ports (as Input or Output)	C_{out}	—	—	12	pF
$\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0-PD5, PD7	C_{in}	—	—	8	

NOTES:

1. All values shown reflect average measurements.
2. Typical values at midpoint of voltage range, 25°C only.
3. Wait I_{DD}: Only timer system active (SPE=TE=RE=0). If SPI, SCI active (SPE=TE=RE=1) add 10% current draw.
4. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square-wave clock source (f_{OSC}=2 MHz), all inputs 0.2 V from rail, no DC loads, less than 50 pF on all outputs, C_L=20 pF on OSC2.
5. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL}=0.2 V, V_{IH}=V_{DD}-0.2 V.
6. Stop I_{DD} measured with OSC1=V_{SS}.
7. Wait I_{DD} is affected linearly by the OSC2 capacitance.

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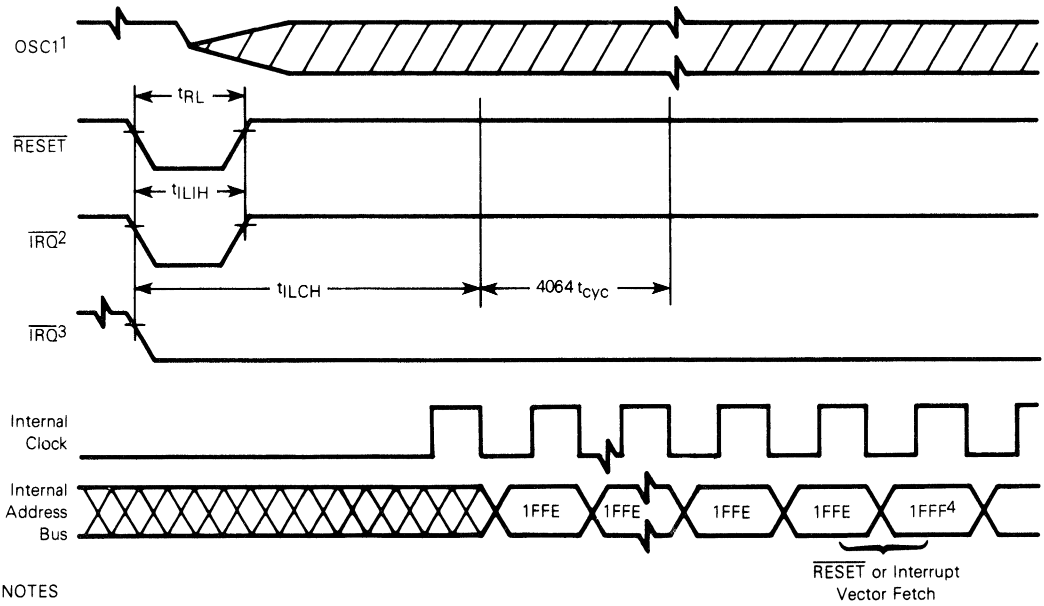
9.7 CONTROL TIMING (V_{DD}=5.0 Vdc ±10%, V_{SS}=0 Vdc, T_A= −55 to +125°C)

Characteristic	Symbol	Limits		Unit
		Min	Max	
Frequency of Operation				
Crystal Option	f_{osc}	–	4 2	MHz
External Clock Option	f_{osc}	dc	4 2	MHz
Internal Operating Frequency				
Crystal (f_{osc} ÷ 2)	f_{op}	–	2 1	MHz
External Clock (f_{osc} ÷ 2)	f_{op}	dc	2 1	MHz
Cycle Time (See Figure 3-1)	t_{cyc}	480	–	ns
Crystal Oscillator Startup Time (See Figure 3-1)	t_{OXOV}	–	100	ms
Stop Recovery Startup Time (Crystal Oscillator) (See Figure 9-3)	t_{ILCH}	–	100	ms
$\overline{\text{RESET}}$ Pulse Width (See Figure 3-2)	t_{RL}	1 5	–	t_{cyc}
Timer				
Resolution**	t_{RESL}	4 0	–	t_{cyc}
Input Capture Pulse Width (See Figure 9-4)	t_{TH}, t_{TL}	125	–	ns
Input Capture Pulse Period (See Figure 9-4)	t_{TLTL}	***	–	t_{cyc}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 3-4)	t_{ILIH}	125	–	ns
Interrupt Pulse Period (See Figure 3-4)	t_{ILIL}	*	–	t_{cyc}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	–	ns

*The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}

**Since a 2-bit prescaler in the timer must count four internal cycles (t_{cyc}), this is the limiting minimum factor in determining the timer resolution

***The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}



NOTES
1 Represents the internal gating of the OSC1 pin
2 $\overline{\text{IRQ}}$ pin edge-sensitive mask option
3 $\overline{\text{IRQ}}$ pin level and edge-sensitive mask option.
4 $\overline{\text{RESET}}$ vector address shown for timing example

Figure 9-3. Stop Recovery Timing Diagram

9.8 CONTROL TIMING (V_{DD}=3.0 Vdc ±10%, V_{SS}=0 Vdc, T_A= −55 to +125°C)

Characteristic	Symbol	Limits		Unit
		Min	Max	
Frequency of Operation				
Crystal Option	f_{osc}	–	2.0	MHz
External Clock Option	f_{osc}	dc	2.0	MHz
Internal Operating Frequency				
Crystal (f_{osc} ÷ 2)	f_{op}	–	1.0	MHz
External Clock (f_{osc} ÷ 2)	f_{op}	dc	1.0	MHz
Cycle Time (See Figure 3-1)	t_{cyc}	1000	–	ns
Crystal Oscillator Startup Time (See Figure 3-1)	t_{OXOV}	–	100	ms
Stop Recovery Startup Time (Crystal Oscillator) (See Figure 9-3)	t_{ILCH}	–	100	ms
$\overline{RESET}$ Pulse Width – Excluding Power-Up (See Figure 3-1)	t_{RL}	1.5	–	t_{cyc}
Timer				
Resolution**	t_{RESL}	4.0	–	t_{cyc}
Input Capture Pulse Width (See Figure 9-4)	t_{TH}, t_{TL}	250	–	ns
Input Capture Pulse Period (See Figure 9-4)	t_{TLTL}	***	–	t_{cyc}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 3-4)	t_{ILIH}	250	–	ns
Interrupt Pulse Period (See Figure 3-4)	t_{ILIL}	*	–	t_{cyc}
OSC1 Pulse Width	t_{OH}, t_{OL}	200	–	ns

*The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}

**Since a 2-bit prescaler in the timer must count four internal cycles (t_{cyc}), this is the limiting minimum factor in determining the timer resolution.

***The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}

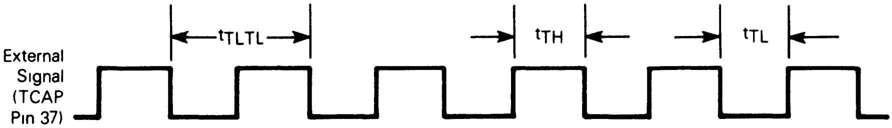


Figure 9-4. Timer Relationships

CDP68HC05C4, CDP68HC05C8

9.9 SERIAL PERIPHERAL INTERFACE (SPI) TIMING (Figure 9-5)

(V_{DD}=5.0 Vdc ±10%, V_{SS}=0 Vdc, T_A= -40 to +125°)

			Limits		
Num.	**Characteristic**	**Symbol**	**Min**	**Max**	**Unit**
	Operating Frequency				
	Master	$f_{op(m)}$	dc	0 5	f_{op}***
	Slave	$f_{op(s)}$	dc	2 1	MHz
1	Cycle Time				
	Master	$t_{cyc(m)}$	2 0	—	t_{cyc}
	Slave	$t_{cyc(s)}$	480	—	ns
2	Enable Lead Time				
	Master	$t_{lead(m)}$	*	—	
	Slave	$t_{lead(S)}$	240	—	ns
3	Enable Lag Time				
	Master	$t_{lag(m)}$	*	—	
	Slave	$t_{lag(S)}$	240	—	ns
4	Clock (SCK) High Time				
	Master	$t_{w(SCKH)m}$	340	—	ns
	Slave	$t_{w(SCKH)s}$	190	—	ns
5	Clock (SCK) Low Time				
	Master	$t_{w(SCKL)m}$	340	—	ns
	Slave	$t_{w(SCKL)s}$	190	—	ns
6	Data Setup Time (Inputs)				
	Master	$t_{su(m)}$	100	—	ns
	Slave	$t_{su(s)}$	100	—	ns
7	Data Hold Time (Inputs)				
	Master	$t_{h(m)}$	100	—	ns
	Slave	$t_{h(s)}$	100	—	ns
8	Access Time (Time to data active from high impedance state)				
	Slave	t_a	0	120	ns
9	Disable Time (Hold Time to High-Impedance State)				
	Slave	t_{dis}	—	240	ns
10	Data Valid				
	Master (Before Capture Edge)	$t_{v(m)}$	0 25	—	$t_{cyc(m)}$
	Slave (After Enable Edge)**	$t_{v(s)}$	—	240	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{ho(m)}$	0 25	—	$t_{cyc(m)}$
	Slave (After Enable Edge)	$t_{ho(s)}$	0	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF)				
	SPI Outputs (SCK, MOSI, MISO)	t_{rm}	—	100	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	t_{rs}	—	2 0	μs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF)				
	SPI Outputs (SCK, MOSI, MISO)	t_{fm}	—	100	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	t_{fs}	—	2 0	μs

*Signal production depends on software

**Assumes 200 pF load on all SPI pins

***Note that the unit this specification uses is f_{op} (internal operating frequency), not MHz! In the master mode the SPI bus is capable of running at one-half of the device's internal operating frequency, therefore 1.05 MHz maximum.

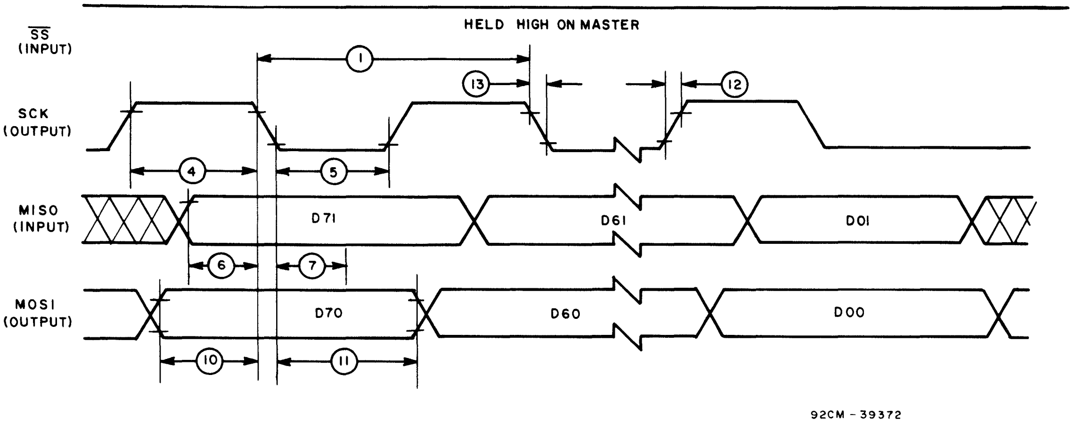
9.10 SERIAL PERIPHERAL INTERFACE (SPI) TIMING (Figure 9-5)
(V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = -40 to +125°C)

			Limits		
Num.	**Characteristic**	**Symbol**	**Min**	**Max**	**Unit**
	Operating Frequency				
	Master	$f_{op(m)}$	dc	0.5	f_{op}***
	Slave	$f_{op(s)}$	dc	1.0	MHz
1	Cycle Time				
	Master	$t_{cyc(m)}$	2.0	—	t_{cyc}
	Slave	$t_{cyc(s)}$	1.0	—	μs
2	Enable Lead Time				
	Master	$t_{lead(m)}$	*	—	
	Slave	$t_{lead(S)}$	500	—	ns
3	Enable Lag Time				
	Master	$t_{lag(m)}$	*	—	
	Slave	$t_{lag(S)}$	500	—	ns
4	Clock (SCK) High Time				
	Master	$t_{w(SCKH)m}$	720	—	μs
	Slave	$t_{w(SCKH)s}$	400	—	ns
5	Clock (SCK) Low Time				
	Master	$t_{w(SCKL)m}$	720	—	μs
	Slave	$t_{w(SCKL)s}$	400	—	ns
6	Data Setup Time (Inputs)				
	Master	$t_{su(m)}$	200	—	ns
	Slave	$t_{su(s)}$	200	—	ns
7	Data Hold Time (Inputs)				
	Master	$t_{h(m)}$	200	—	ns
	Slave	$t_{h(s)}$	200	—	ns
8	Access Time (Time to data active from high impedance state)				
	Slave	t_a	0	250	ns
9	Disable Time (Hold Time to High-Impedance State)				
	Slave	t_{dis}	—	500	ns
10	Data Valid				
	Master (Before Capture Edge)	$t_{v(m)}$	0.25	—	$t_{cyc(m)}$
	Slave (After Enable Edge)**	$t_{v(s)}$	—	500	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{ho(m)}$	0 25	—	$t_{cyc(m)}$
	Slave (After Enable Edge)	$t_{ho(s)}$	0	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF)				
	SPI Outputs (SCK, MOSI, MISO)	t_{rm}	—	200	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	t_{rs}	—	2 0	μs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF)				
	SPI Outputs (SCK, MOSI, MISO)	t_{fm}	—	200	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	t_{fs}	—	2 0	μs

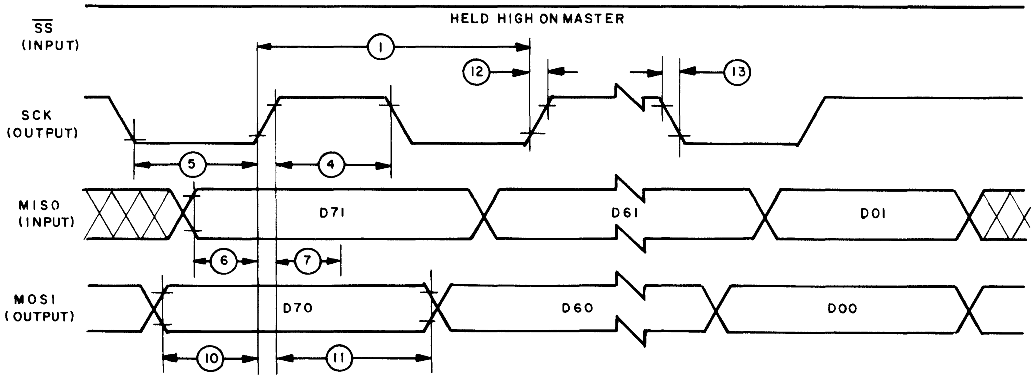
*Signal production depends on software

**Assumes 200 pF load on all SPI pins

***Note that the unit this specification uses is f_{op} (internal operating frequency), not MHz! In the master mode the SPI bus is capable of running at one-half of the device's internal operating frequency, therefore 0.5 MHz maximum.



(a) SPI Master Timing CPOL = 0, CPHA = 1



(b) SPI Master Timing CPOL = 1, CPHA = 1

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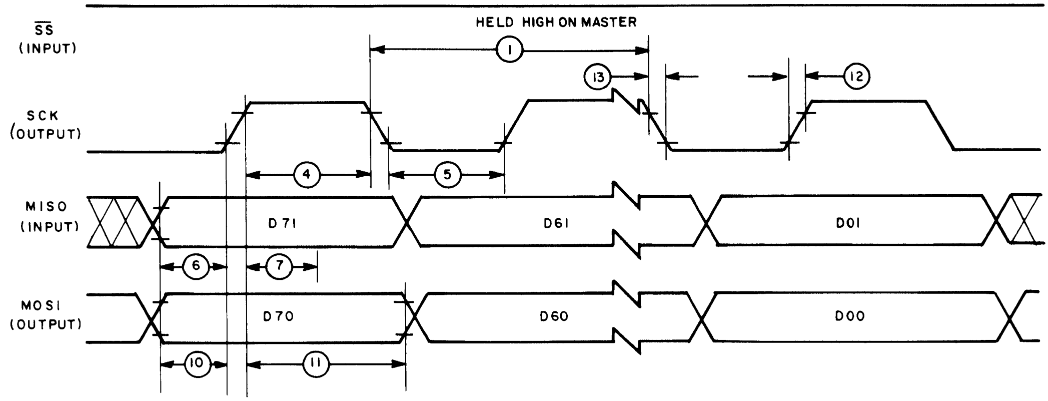
NOTE: MEASUREMENT POINTS ARE V_{OL}, V_{OH}, V_{IL}, V_{IH}

Figure 9-5. Timing Diagrams



(c) SPI Master Timing CPOL = 0, CPHA = 0

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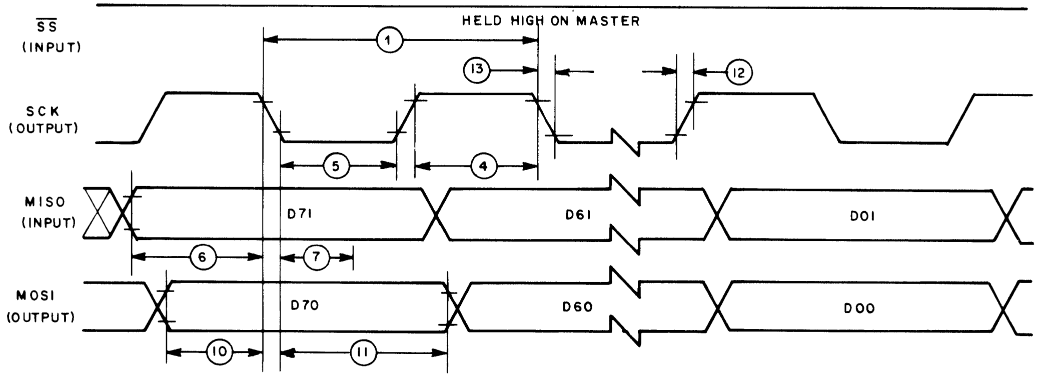

(d) SPI Master Timing CPOL = 1, CPHA = 0

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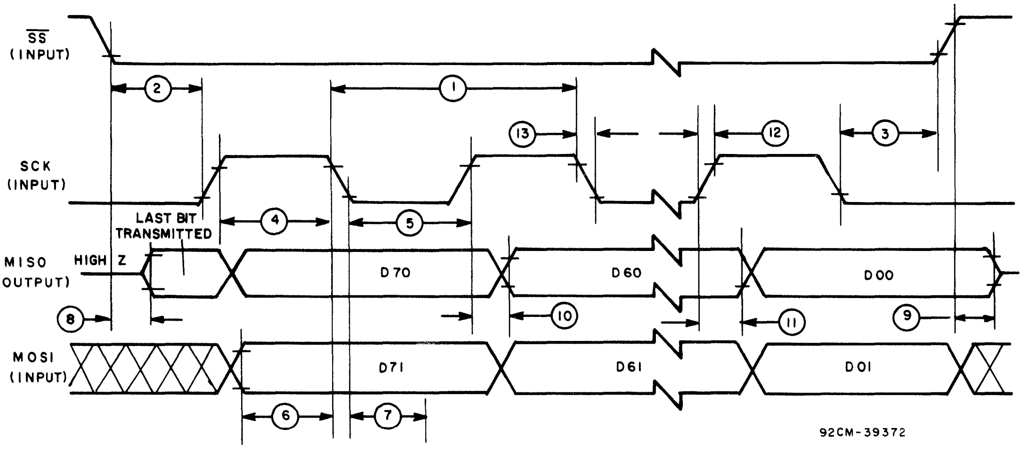
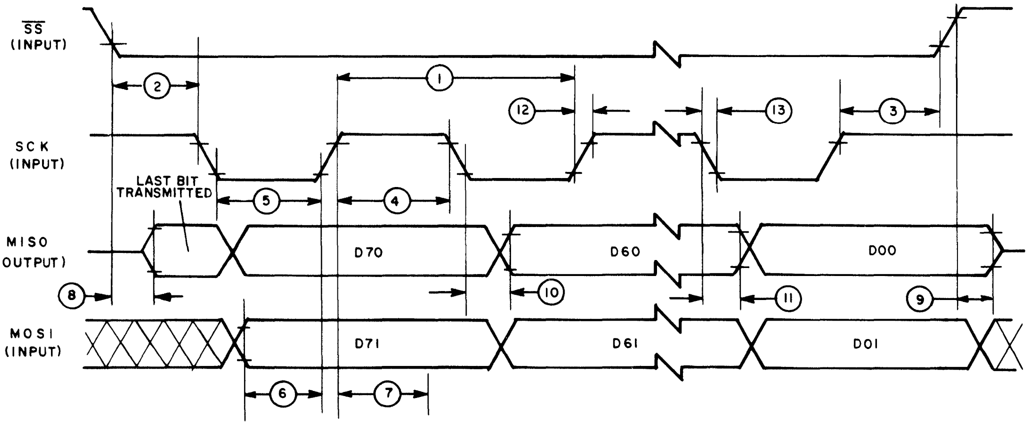
NOTE: MEASUREMENT POINTS ARE V_{OL}, V_{OH}, V_{IL} AND V_{IH}

Figure 9-5. Timing Diagrams (Continued)



(e) SPI Slave Timing CPOL = 0, CPHA = 1



(f) SPI Slave Timing CPOL = 1, CPHA = 1

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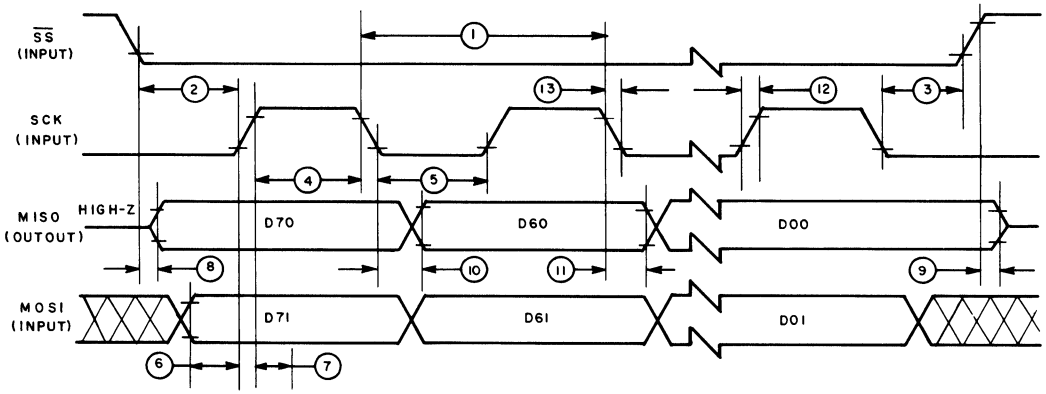
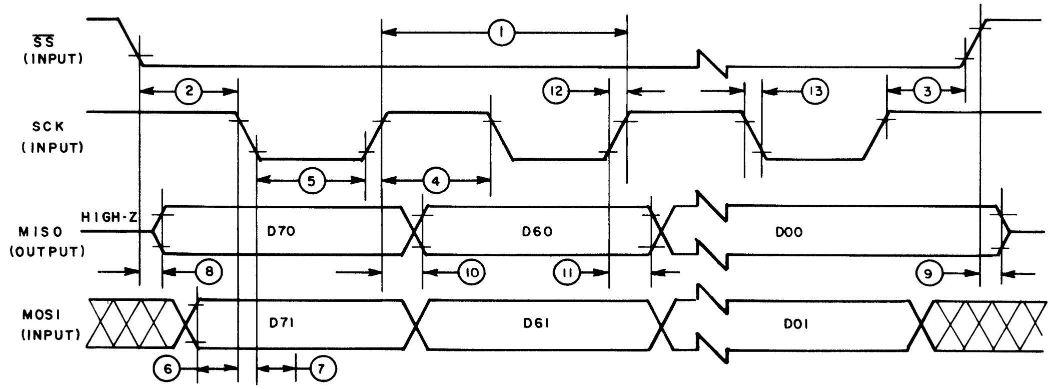
NOTE: MEASUREMENT POINTS ARE V_{OL}, V_{OH}, V_{IL}, AND V_{IH}.

Figure 9-5. Timing Diagrams (Continued)



(g) SPI Slave Timing CPOL=0, CPHA=0



(h) SPI Slave Timing CPOL=1, CPHA=0

NOTE: MEASUREMENT POINTS ARE V_{OL}, V_{OH}, V_{IL} AND V_{IH}

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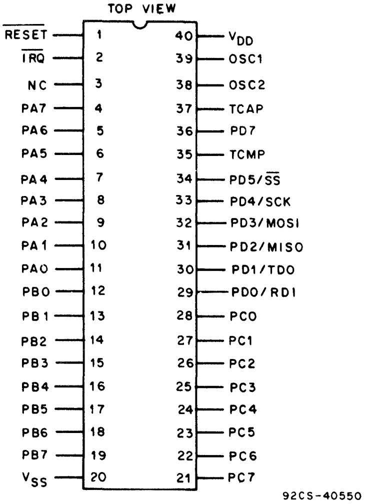
Figure 9-5. Timing Diagrams (Continued)

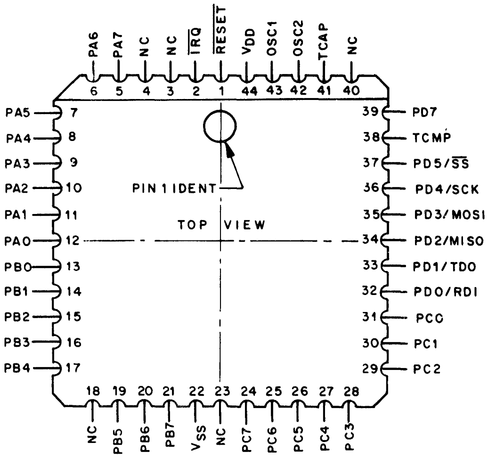
SECTION 11
MECHANICAL DATA

This section contains the pin assignment and package dimension diagrams for the CDP68HC05C4 and CDP68HC05C8 microcomputers.

11.1 TERMINAL ASSIGNMENTS



TERMINAL ASSIGNMENT
D Suffix - 40-Lead Dual-In-Line Side-Brazed Ceramic Package
E Suffix - 40-Lead Dual-In-Line Plastic Package



NC = NO CONNECTION

TERMINAL ASSIGNMENT
Q Suffix - 44 Lead Plastic Chip-Carrier (PCC) Package

CDP68HC05D2

HCMOS Microcomputer

Introduction

General

The CDP68HC05D2 Microcomputer Unit (MCU) belongs to the CDP6805 Family of Microcomputers This 8-bit MCU contains on-chip oscillator CPU, RAM, ROM, I/O, and Timer The fully static design allows operation at frequencies down to DC, further reducing its already low-power consumption. It is a low-power processor designed for low-end to mid-range applications in the telecommunications, consumer, automotive, and industrial markets where very low power consumption constitutes an important factor.

The CDP68HC05D2 is supplied in a 40-lead hermetic dual-in-line side brazed ceramic package (D suffix), a 40-lead dual-in-line plastic package (E suffix), and a 44-lead Plastic Chip Carrier (Q suffix).

Specific Features

- *Typical power:*
  - *Operating, 25 mW*
  - *WAIT, 7.5 mW*
  - *STOP, 5 μW*
- *Fully static operation*
- *96 bytes of on-chip RAM*
- *2176 bytes of on-chip ROM*
- *31 I/O lines*
- *12 programmable open-drain output lines*
- *On-chip oscillator for Timer*
- *2.1 MHz internal operating frequency*
- *Internal 16-bit timer*
- *Serial Peripheral Interface (SPI)*
- *External ($\overline{\text{IRQ}}$), timer, Port B, and Serial Interrupts*
- *Self check mode*
- *Single 2.5 to 6 volt supply (**2-V data retention mode**)*
- *RC or crystal on-chip oscillator*
- *8x8 multiply instruction*
- *True bit manipulation*
- *Indexed addressing for tables*
- *Memory mapped I/O*

Functional Pin Descriptions

V_{DD} and V_{SS}

Power is supplied to the MCU using these two pins V_{DD} is power and V_{SS} is ground.

N.C.

The pin labelled N.C. should be left disconnected.

$\overline{\text{IRQ}}$ (Maskable Interrupt Request)

IRQ is a programmable option which provides two different choices of interrupt triggering sensitivity. These options are. 1) negative edge-sensitive triggering only, or 2) both negative edge-sensitive and level-sensitive triggering. In the latter case, either type of input to the $\overline{\text{IRQ}}$ pin will produce the interrupt. The MCU completes the current instruction before it responds to the interrupt request. When the $\overline{\text{IRQ}}$ pin goes low for at least one t_{ILIH}, a logic one is latched internally to signify that an interrupt has been requested. When the MCU completes its current instruction, the interrupt latch is tested. If the interrupt latch contains a logic one, and the interrupt mask bit (I bit) in the condition code register is clear, the MCU then begins the interrupt sequence. If the option is selected to include level-sensitive triggering, then the $\overline{\text{IRQ}}$ input requires an external resistor to V_{DD} for "wire-OR" operation. See the INTERRUPTS section for more detail.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ input is not required for startup but can be used to reset the MCU internal state and provide an orderly software startup procedure. Refer to the RESETs section for a detailed description

3

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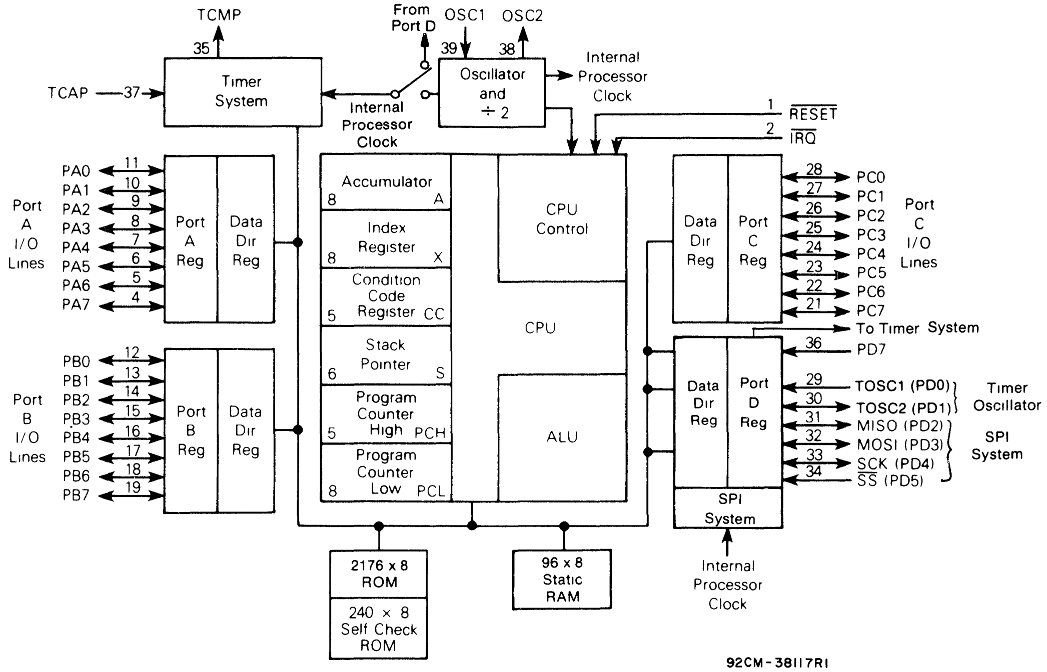


Fig. 1 — CDP68HC05D2 CMOS microcomputer block diagram.

TCAP

The TCAP input controls the input capture feature for the on-chip programmable timer system Refer to the INPUT CAPTURE REGISTER section for additional information

TCMP

The TCMP pin (35) provides an output for the output compare feature of the on-chip timer system. Refer to the OUTPUT COMPARE REGISTER section for additional information.

OSC1, OSC2

The CDP68HC05D2 can be configured to accept either a crystal input or an RC network to control the internal oscillator. This option is mask selectable. The internal clocks are derived by a divide-by-two of the internal oscillator frequency (f_{OSC}).

CRYSTAL.

The circuit shown in Fig. 2(b) is recommended when using a crystal. The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{OSC} in the control timing charts. Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and startup stabilization time. Refer to the Electrical Characteristics Table.

CERAMIC RESONATOR

A ceramic resonator may be used in place of the crystal in cost-sensitive applications. The circuit in Fig. 2(b) is recommended when using a ceramic resonator. Fig. 2(a) lists the recommended capacitance and feedback resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

RC.

If the RC oscillator option is selected, then a resistor is connected to the oscillator pins as shown in Fig. 2(d).

EXTERNAL CLOCK.

An external clock should be applied to the OSC1 input with the OSC2 input not connected, as shown in Fig. 2(e). An external clock may be used with either the RC or crystal oscillator option. The t_{OXOV} or t_{ILCH} specifications do not apply when using an external clock input. The equivalent specification of the external clock should be used in lieu of t_{OXOV} or T_{ILCH}.

PA0-PA7

These eight I/O input comprise port A. The state of any pin is software programmable and all port A lines are configured as input during power-on or reset. These lines are open-drain software programmable. Refer to INPUT/OUTPUT PROGRAMMABLE paragraph below for a detailed description of I/O programming.

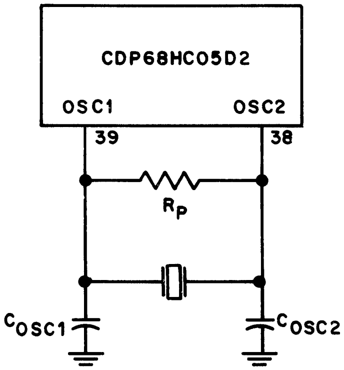
Crystal

	2 MHz	4 MHz	Units
R_{SMAX}	400	75	Ω
C_0	5	7	pF
C_1	0.008	0.012	μF
C_{OSC1}	15-40	15-30	pF
C_{OSC2}	15-30	15-25	pF
R_P	10	10	MΩ
Q	30	40	K

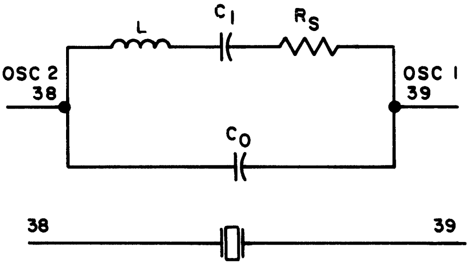
Ceramic Resonator

	2-4 MHz	Units
R_S (typical)	10	Ω
C_0	40	pF
C_1	4.3	pF
C_{OSC1}	30	pF
C_{OSC2}	30	pF
R_P	1-10	MΩ
Q	1250	—

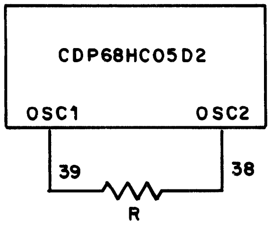
(a) Crystal/Ceramic Resonator Parameters



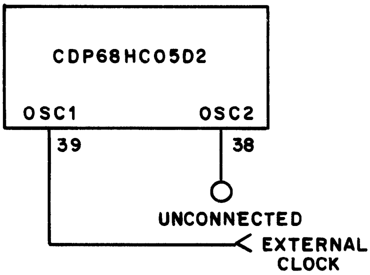
(b) Crystal Oscillator Connections



(c) Equivalent Crystal Circuit



(d) RC Oscillator Connections



(e) External Clock Source Connections

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Fig. 2 — Oscillator Connections

CDP68HC05D2

PB0-PB7

These eight lines comprise port B. The state of any pin is software programmable and all port B lines are configured as input during power-on or reset. These lines may be configured to generate interrupts. Refer to port B interrupt section. Refer to INPUT/OUTPUT PROGRAMMING paragraph below for a detailed description of I/O programming

PC0-PC7

These eight lines comprise port C. The state of any pin is software programmable and all port C lines are configured as input during power-on or reset. Refer to INPUT/OUTPUT PROGRAMMING paragraph below for a detailed description of I/O programming.

PD0-PD5, PD7

These seven lines comprise Port D. Four pins (PD2-PD5) are individually programmable as either inputs or outputs. PD7 is always an input line. PD0-PD5 lines are set as inputs on power-on or reset. The enabled Timer and SPI special functions listed below affect the pins on this port. PD0-PD1 (referred to as TOSC1, TOSC2) are used to control the oscillator for the timer in the external clock mode. If the external clock mode is not used, these pins are configured as inputs only. See sections EXTERNAL TIMER OSCILLATOR and SPECIAL PURPOSE PORT. MOSI is the SPI Serial Data Output (in Master Mode) MISO is the SPI Serial Data Input (in Master Mode). SCK is the clock for the SPI (configured as output in the Master Mode). SS is the Slave Select input for the SPI.

Note: It is recommended that all unused inputs (except OSC2) and I/O ports configured as inputs be tied to an appropriate logic level (e.g. either V_{DD} or V_{SS}).

Parallel I/O

The I/O register section is found in the first 32 bytes of memory and includes the following.

- Three programmable parallel ports (Ports A, B, and C).
- One port (Port D) with three input lines and four programmable lines which share its external pins with Serial Peripheral Interface (SPI) and Timer functions.

The general memory arrangement for each system has a control register, followed by a status register, followed by a data register. A CPU read of any undefined/unused bits will obtain a value of "0". The register assignment may be found in Table II.

Input/Output Programming

Parallel Ports

Ports A, B, and C may be programmed as an input or an output under software control. The direction of the pins is determined by the state of the corresponding bit in the port data direction register (DDR). Each 8-bit port has an associated 8-bit data direction register. Any port A, port B, or port C pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared to a logic zero. At power-on or reset all DDRs are cleared, which configure all port A, B, and C pins as inputs. The data direction registers are capable of being written to or read by the processor. **Refer to Fig. 3 and Table I. During the programmed output** state, a read of the data register actually reads the value of the output data latch and not the I/O pin.

As an option for Port A, the eight Port A outputs (PA0-PA7) can be programmed to be open drain outputs when bit 0 in the Special Port Control/Status register is set and their DDR bits are set. Also, the setting of the "Wired-OR" Mode (WOM) bit in the SPI Control Register will cause Port D lines 2-5 (when programmed as outputs) to be open drain

SPECIAL PURPOSE PORT

Port D contains four individually programmable bi-directional lines (PD2-PD5) and three input lines (PD0, PD1, and PD7). The direction of the four bi-directional lines is determined by the state of the data direction register (DDR). Each of these four lines has an associated DDR bit. The validity of a port bit is determined by whether the SPI system and external timer oscillator are enabled or disabled. When the SPI system is disabled, lines PD2-PD5 behave as normal I/O lines and the corresponding DDR bits determine whether the lines are inputs or outputs. Lines PD0 and PD1 are inputs when the external timer oscillator is not used. However, once the external timer oscillator has been enabled, PD1 will become an output-only line until the processor is reset.

A write to bits 0, 1, 6, and 7 of the Port D Data Direction Register will have no effect. A read of DDR bits 0, 1, 6, and 7 will always return zeros.

Note: When using the Serial Peripheral Interface (SPI), bit 5 of Port D is dedicated as the Slave Select (SS) input when the SPI system is enabled In SPI Slave Mode, DDR bit 5 has no meaning or effect In SPI Master Mode, DDR bit 5 determines whether Port D bit 5 is an error detect input to the SPI (DDR bit clear) or a general purpose output line (DDR bit set)

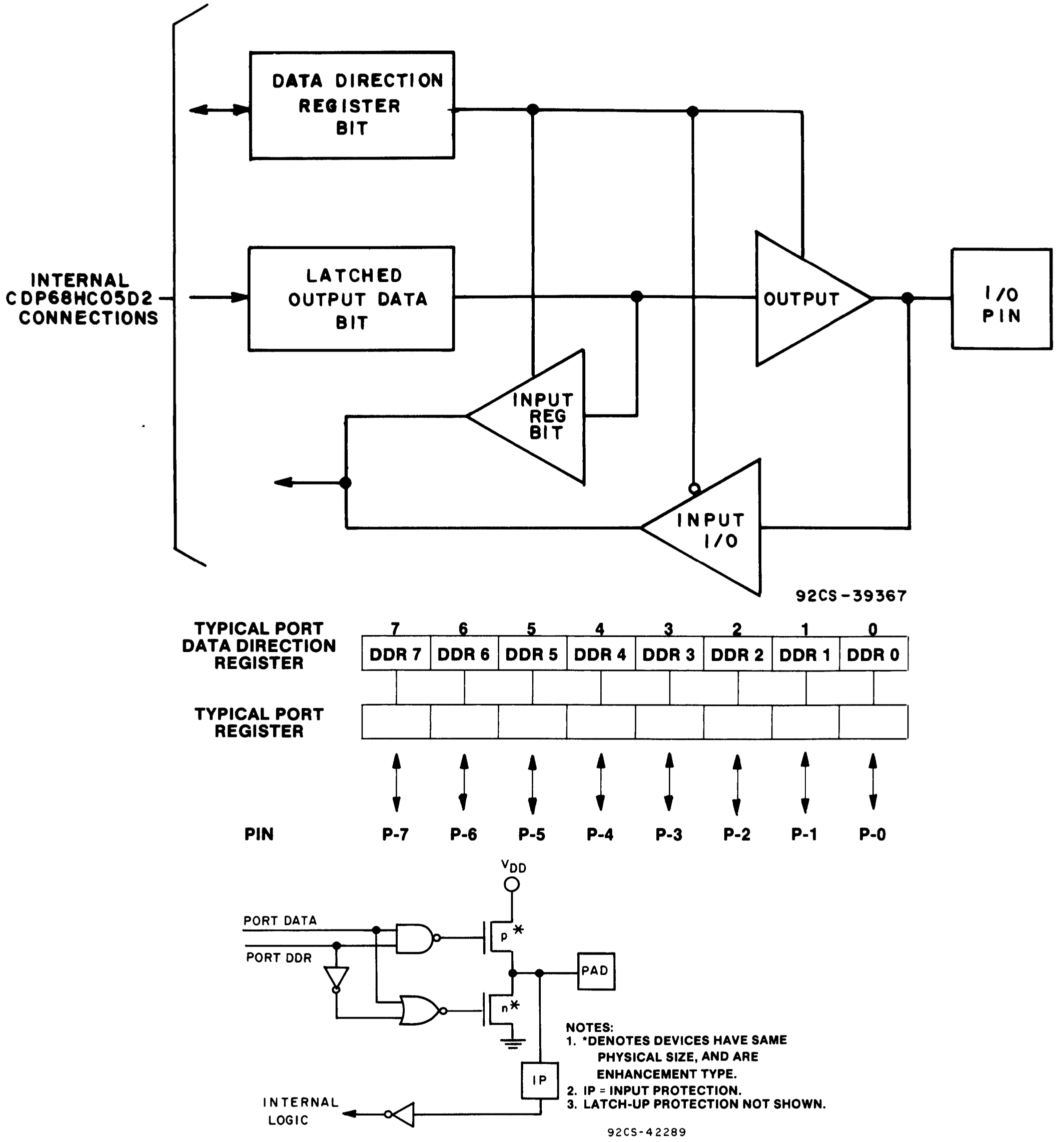
For bits 2, 3, and 4 (MISO, MOSI, and SCK), if the SPI is enabled and expects the bit to be an input, it will be an input regardless of the state of the DDR bit. If the SPI is enabled and expects the bit to be an output, it will be an output ONLY if the DDR bit is set.

Memory

The CDP68HC05D2 has a total address space of 8192 bytes. **The address map is shown in Fig. 4. The CDP68HC05D2 has** implemented 2550 bytes of the address locations.

The first 256 bytes of memory (page zero) is comprised of the I/O port locations, timer locations, 128 bytes of ROM and 96 bytes of RAM. The next 2048 bytes comprise the user ROM. The 16 highest address bytes contain the reset and interrupt vectors.

The stack pointer is used to address data stored on the stack. Data is stored on the stack during interrupts and subroutine calls. At power-up, the stack pointer is set to $00FF and it is decremented as data is pushed on the stack. When data is removed from the stack, the stack pointer is incremented. A maximum of 64 bytes of RAM is available for stack usage. Since most programs use only a small part of the allocated stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are usable for **program data storage. See Fig. 4 for details on stacking order.**



NOTES:
1. *DENOTES DEVICES HAVE SAME PHYSICAL SIZE, AND ARE ENHANCEMENT TYPE.
2. IP = INPUT PROTECTION.
3. LATCH-UP PROTECTION NOT SHOWN.

Fig. 3 - Typical Parallel Port I/O Circuitry

Table I - I/O Pin Functions

R/$\overline{W}$*	DDR	I/O Pin Function
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

*R/$\overline{W}$ is an internal signal.

CDP68HC05D2

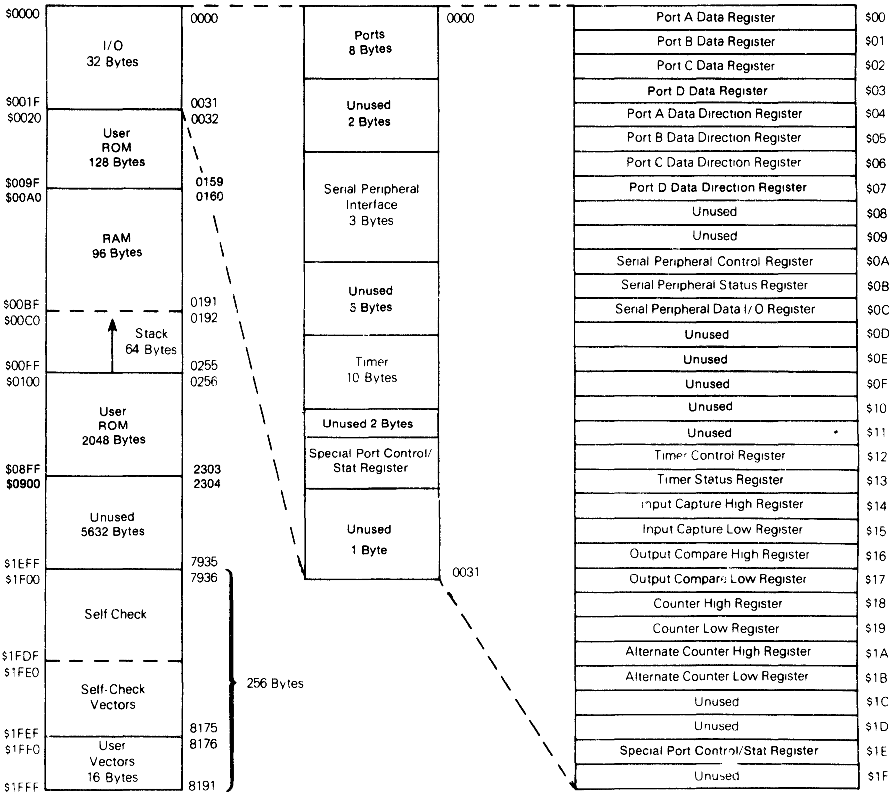


Fig. 4 - Address Map

Table II — CDP68HC05D2 I/O Registers

ADDRESS	DATA									DATA							
$0000-$001F	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
00 Port A Data									10 Unused	—	—	—	—	—	—	—	—
01 Port B Data									11 Unused	—	—	—	—	—	—	—	—
02 Port C Data									12 Timer Control	ICIE	OCIE	TOIE	EOE	ECC	—	IEDG	OLVL
03 Port D Data		*							13 Timer Status	ICF	OCF	TOF	—	—	—	—	—
04 Port A DDR									14 Capture High								
05 Port B DDR									15 Capture Low								
06 Port C DDR									16 Compare High								
07 Port D DDR	—	—					—	—	17 Compare Low								
08 Unused	—	—	—	—	—	—	—	—	18 Counter High								
09 Unused	—	—	—	—	—	—	—	—	19 Counter Low								
0A SPI Control	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	1A Dual TM High								
0B SPI Status	SPIF	WCOL	—	MODF	—	—	—	—	1B Dual TM Low								
0C SPI Data									1C Unused	—	—	—	—	—	—	—	—
0D Unused	—	—	—	—	—	—	—	—	1D Unused	—	—	—	—	—	—	—	—
0E Unused	—	—	—	—	—	—	—	—	1E Special Port	PBIF	—	—	—	—	DLY	PBIE	PAOD
									Cntl/STAT								
OF Unused	—	—	—	—	—	—	—	—	1F Unused	—	—	—	—	—	—	—	—

* = dedicated as TCMP output
— = unused bits

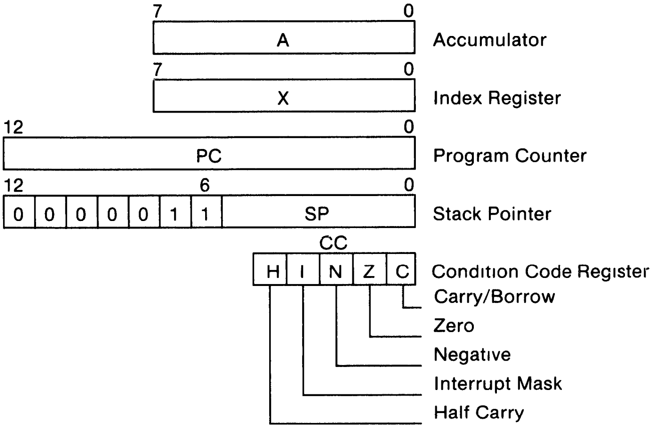
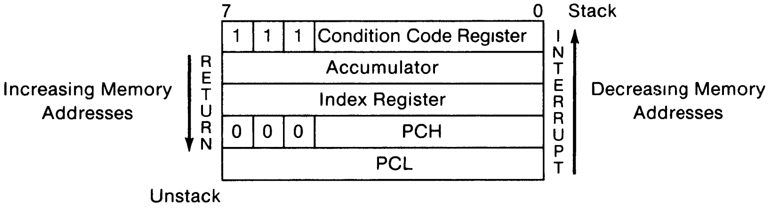


Fig. 5 - Programming model.


7
0
Stack
1 1 1 Condition Code Register
Accumulator
Index Register
0 0 0 PCH
PCL
RETURN
INTERRUPT
Increasing Memory Addresses
Decreasing Memory Addresses
Unstack

Note: Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc Pulling from the stack is in the reverse order

Fig. 6 - Stacking order.

CPU Registers

The CDP68HC05D2 CPU contains five registers, as shown in the programming model of Fig. 5. The interrupt stacking order is shown in Fig. 6.

Accumulator (A)

The accumulator is an 8-bit general-purpose register used to hold operands, results of the arithmetic calculations, and data manipulations.

Index Register (X)

The x register is an 8-bit register which is used during the indexed modes of addressing. It provides an 8-bit value which is used to create an effective address. The index register is also used for data manipulations with the read-modify-write type of instructions and as a temporary storage register when not performing addressing operations.

Program Counter (PC)

The program counter is a 13-bit register that contains the address of the next instruction to be executed by the processor.

Stack Pointer (SP)

The stack pointer is a 13-bit register containing the address of the next free locations on the push-down/pop-up stack. When accessing memory; the seven most significant bits are permanently configured to 0000011. These seven bits are appended to the six least significant register bits to produce an address within the range of $00FF to $00C0. The

CDP68HC05D2

stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts During external or power-on reset, and during a reset stack pointer (RSP), instruction, the stack pointer is set to its upper limit ($00FF) Nested interrupt and/or subroutines may use up to 64 (decimal) locations. When the 64 locations are exceeded, the stack pointer wraps around and points to its upper limit ($00FF), losing the previously stored information. A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five RAM bytes.

Condition Code Register (CC)

The condition code register is a 5-bit register which indicates the results of the instruction just executed as well as the state of the processor These bits can be individually tested by a program and specified action taken as a result of their state. Each bit is explained in the following paragraphs.

HALF CARRY BIT (H).

The H bit is set to a one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H bit is useful in binary-coded decimal subroutines.

INTERRUPT MASK BIT (I).

When the I bit is set, all interrupts are disabled. Clearing this bit enables the interrupts. If an external interrupt occurs while the I bit is set, the interrupt is latched and is processed after the I bit is next cleared; therefore, no interrupts are lost because of the I bit being set An internal interrupt can be lost if it is cleared while the I bit is set (refer to PROGRAMMABLE TIMER, SERIAL PERIPHERAL INTERFACE, and PORT B INTERRUPT sections for more information.

NEGATIVE (N).

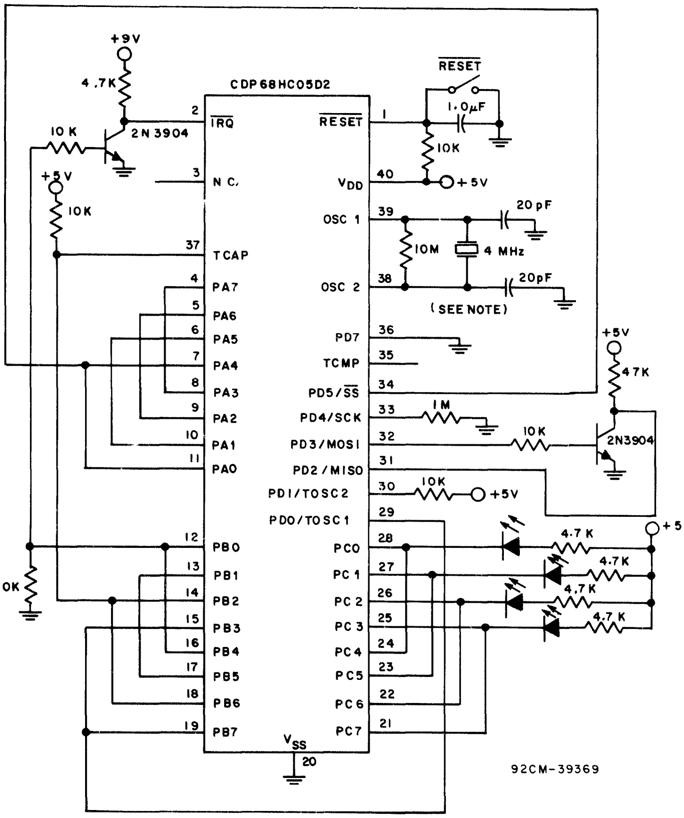
When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation is negative (bit 7 in the result is a logic one).

ZERO (Z).

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation is zero.

CARRY/BORROW (C).

Indicates that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts, and rotates.



NOTE
THE RC OSCILLATOR OPTION MAY ALSO BE USED IN THIS CIRCUIT

Fig. 7 - Self-Check Circuit Schematic Diagram

Self-Check

The CDP68HC05D2 contains in mask ROM address locations $1F00 to $1FEF, a program designed to check the part's integrity with a minimum of support hardware The self-check capability of the CDP68HC05D2 MCU provides an internal check to determine if the device is functional. Self-check is performed using the circuit shown in the schematic diagram of Fig. 7. As shown in the diagram, port C pins PC0-PC3 are monitored (light-emitting diodes are shown but other devices could be used) for the self-check results The self-check mode is entered by applying a 9Vdc input (through a 4 7 kilohm resistor) to the $\overline{\text{IRQ}}$ pin (2), a 5Vdc input (through a 10-kilohm resistor) to the TCAP pin (37), a 5Vdc input (through a 10K resistor) to Port B, bit 2 (pin 14), and then depressing the reset switch to execute a reset After reset, the following six tests are performed automatically·

I/O — Functionally exercises ports A, B, and C
RAM — Counter test for each RAM byte
Timer — Tracks counter register and checks OCF flag
ROM — Exclusive OR with odd ones parity result
SPI — Transmission test with check for SPIF, WCOL, and MODF flags
INTERRUPTS — Tests external, timer, Port B and SPI interrupts

Self-check results (using LEDs as monitors) are shown in Table III. The following subroutines are available to user programs and do not require any external hardware.

Table III. Self-Check Results

PC3	PC2	PC1	PC0	Remarks
1	0	0	1	Bad I/O
1	0	1	0	Bad RAM
1	0	1	1	Bad Timer
1	1	0	0	Bad Port D and/or Timer Oscillator
1	1	0	1	Bad ROM
1	1	1	0	Bad SPI
1	1	1	1	Bad Interrupts or $\overline{\text{IRQ}}$ Request
Flashing				Good Device
All Others				Bad Device, Bad Port C, etc.

0 indicates LED on; 1 indicates LED is off

TIMER TEST SUBROUTINE

This subroutine returns with the Z bit cleared if any error is detected; otherwise, the Z bit is set. This subroutine is called at location $1F0E. The output compare register is first set to the current timer state. Because the timer is free-running and has only a divide-by-four prescaler, each timer count cannot be tested. The test reads the timer once every 10 counts (40 cycles) and checks for correct counting. The test tracks the counter until the timer wraps around, triggering the output compare flag in the timer status register. RAM locations $00A0 and $00A1 are overwritten. Upon return to the user's program, X=40 If the test passed, A=0.

ROM CHECKSUM SUBROUTINE

This subroutine returns with the Z bit cleared if any error is detected; otherwise, the Z bit is set. This subroutine is called at location $1F93 with RAM location $00A3 equal to $01 and A = 0. A short routine is set up and executed in RAM to compute a checksum of the entire ROM pattern. Upon return to the user's program, X=0 If the test passed, A=0 RAM locations $00A0 through $00A3 are overwritten

RESETS

The CDP68HC05D2 has two reset modes· an active low external reset pin ($\overline{\text{RESET}}$) and a power-on reset function, refer to Fig. 8.

$\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ input pin is used to reset the MCU to provide an orderly software startup procedure When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one and one-half t_{cyc}. The $\overline{\text{RESET}}$ pin contains an internal Schmitt Trigger as part of its input to improve noise immunity

Power-On-Reset

The power-on reset occurs when a positive transition is detected on V_{DD}. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage There is no provision for power-down reset. The power-on circuitry provides for a delay from the time that the oscillator becomes active upon power-up or when exiting the STOP mode.

Associated with the mask programmable CPU oscillator option in the D2 is a mask option for controlling the timeout which occurs at power-on or when exiting the STOP mode. The user has a mask option of selecting a 4064 t_{cyc} delay (meant for use with the crystal oscillator option) or a 2 cycle timeout permitting faster startups with the RC oscillator mask option or external oscillator.

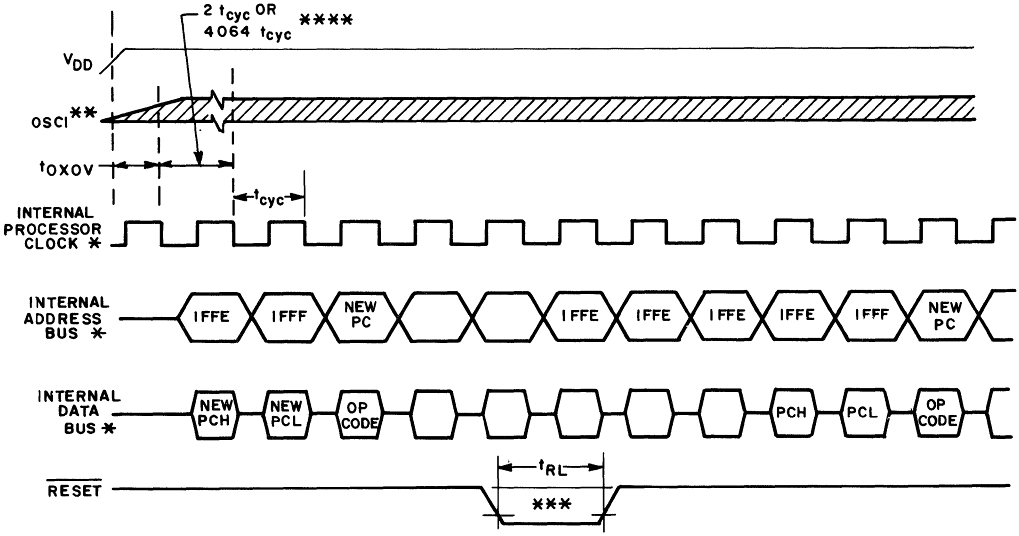
To permit use of an external oscillator with crystal mask option and a two cycle delay when exiting from STOP, bit 2 (DLY) of the Special Port Control/Status Register (memory location $001E), when set, will override the 4064 cycle mask-programmable delay and force a two cycle timeout Since this bit is reset at power-on, the power-on delay will remain as mask-programmed.

If the external $\overline{\text{RESET}}$ pin is low at the end of the delay timeout, the processor remains in the reset condition until the $\overline{\text{RESET}}$ goes high. Table IV shows the actions of the two resets on internal circuits, but not necessarily in order of occurrence.

Interrupts

Systems often require that normal processing be interrupted so that some external event may be serviced. The CDP68HC05D2 may be interrupted by one of five different methods: either one of four maskable hardware interrupts ($\overline{\text{IRQ}}$, SPI, PBINT, or Timer) and one non-maskable software interrupt (SWI). Interrupts such as Timer and SPI have several flags which will cause the interrupt. Generally, interrupt flags are located in read-only status registers, while their equivalent enable bits are located in associated control registers If the enable bit is a logic zero it blocks the interrupt from occurring but does not inhibit the flag from being set Reset clears all enable bits to preclude interrupts during the reset procedure

The general sequence for clearing an interrupt is a software sequence of first accessing the status register while the interrupt flag is set, followed by a read or write of an associated register When any of these interrupts occur, and if the enable bit is a logic one, normal processing is suspended at the end of the current instruction execution. Interrupts cause the processor registers to be saved on the stack (see Fig. 6) and the interrupt mask (I bit) set to prevent



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* INTERNAL TIMING SIGNAL AND BUS INFORMATION NOT AVAILABLE EXTERNALLY.
** OSC1 LINE IS NOT MEANT TO REPRESENT FREQUENCY. IT IS ONLY USED TO REPRESENT TIME.
*** THE NEXT RISING EDGE OF THE INTERNAL PROCESSOR CLOCK FOLLOWING THE RISING EDGE OF $\overline{\text{RESET}}$ INITIATES THE RESET SEQUENCE.
**** DELAY IS MASK PROGRAMMABLE.

Fig. 8 - Power-On Reset and $\overline{RESET}$

Table IV. Reset Action on Internal Circuit

Condition
Timer Prescaler reset to zero state
Timer counter configured to $FFFC
Timer output compare (TCMP) bit reset to zero
All timer interrupt enable bits cleared (ICIE, OCIE, and TOIE) to disable timer interrupts. The OLVL timer bit is also cleared by reset.
All data direction registers cleared to zero (input)
Configure stack pointer to $00FF
Force internal address bus to restart vector ($1FFE-$1FFF)
Set I bit in condition code register to a logic one
Clear STOP latch*
Clear external interrupt latch
Clear WAIT latch
Disable SPI (serial output enable control bit SPE=0). Other SPI bits cleared by reset include: SPIE, MSTR, SPIF, WCOL, and MODF.
Clear serial interrupt enable bit
Place SPI system in slave mode (MSTR=0)
Timer oscillator disabled and 3-stated
CPU oscillator connected to timer
Reset Port B interrupt enable
DWOM bit reset
PAOD bit reset
Reset DLY bit in special control/status register

*Indicates that timeout still occurs with $\overline{\text{RESET}}$ pin additional interrupts. The appropriate interrupt vector then points to the starting address of the interrupt service routine (refer to Fig. 4 for vector location). Upon completion of the interrupt service routine, the RTI instruction (which is normally a part of the service routine) causes the register contents to be recovered from the stack followed by a return to normal processing. The stack order is shown in Fig. 6.

Note: The interrupt mask bit (I bit) will be cleared upon returning from the interrupt if and only if the corresponding bit stored in the stack is zero The priority of the various interrupts is as follows (highest priority to lowest priority:

RESET → * → EXT INT → TIMER → SPI → Port B

*is any instruction or the SWI service routine

A discussion of interrupts, plus a table listing vector addresses for all interrupts including reset, in the CDP68HC05D2 is provided in Table V

Table V. Vector Address for Interrupts and Reset

Register	Flag Name	Interrupts	CPU Interrupt	Vector Address
N/A	N/A	Reset	$\overline{\text{RESET}}$	$1FFE-$1FFF
N/A	N/A	Software	$\overline{\text{SWI}}$	$1FFC-$1FFD
N/A	N/A	External Interrupt	$\overline{\text{IRQ}}$	$1FFA-$1FFB
Timer Status	ICF	Input Capture	TIMER	$1FF8-$1FF9
	OCF	Output Compare		
	TOF	Timer Overflow		
SPI Status	SPIF	Transfer Complete	SPI	$1FF4-$1FF5
	MODF	Mode Fault		
Special Port c/s	PBIF	Port B	PB	$1FF2-$1FF3

Hardware Controlled Interrupt Sequence

The following three functions ($\overline{\text{RESET}}$, STOP, and WAIT) are not in the strictest sense an interrupt; however, they are acted upon in a similar manner. Flowcharts for hardware interrupts are shown in Fig. 9, and for STOP and WAIT are provided in Fig. 10. A discussion is provided below:

- A low input on the $\overline{\text{RESET}}$ input pin causes the program to vector to its starting address which is specified by the contents of memory locations $1FFE and $1FFF. The I bit in the condition code register is also set. Much of the MCU is configured to a known state during this type of reset as previously described in the RESET paragraph.
- STOP — The STOP instruction causes the oscillator to be turned off and the processor to "sleep" until an external interrupt ($\overline{\text{IRQ}}$), Port B interrupt, Timer interrupt (if using an external timer clock), or $\overline{\text{RESET}}$ occurs.
- WAIT — The WAIT instruction causes all processor clocks to stop, but leaves the Timer and SPI clocks running. This "rest" state of the processor can be cleared by reset, an external interrupt ($\overline{\text{IRQ}}$), Timer interrupt, SPI interrupt, or Port B interrupt. There are no special wait vectors for these individual interrupts.

Software Interrupt (SWI)

The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask (I bit) in the condition code register. The interrupt service routine address is specified by the contents of memory location $1FFC and $1FFD.

External Interrupt

If the interrupt mask (I bit) of the condition code register has been cleared and the external interrupt pin ($\overline{\text{IRQ}}$) has gone low, then the external interrupt is recognized. When the interrupt is recognized, the current state of the CPU is pushed onto the stack and the I bit is set. This masks further interrupts until the present one is serviced. The interrupt service routine address is specified by the content of memory location $1FFA and $1FFB. Either a level-sensitive and negative edge-sensitive trigger, or a negative edge-sensitive only trigger are available as a mask option. Fig. 11 shows both a functional and mode timing diagram for the interrupt line. The timing diagram shows two different treatments of the interrupt line ($\overline{\text{IRQ}}$) to the processor. The first method shows single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the number of cycles required to execute the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an RTI occurs). The second configuration shows several interrupt lines "wire-ORed" to form the interrupts at the processor. Thus, if after servicing one interrupt the interrupt line remains low, then the next interrupt is recognized.

Note: The internal interrupt latch is cleared in the first part of the service routine, therefore, one (and only one) external interrupt pulse could be latched during t_{ILIL} and serviced as soon as the I bit is cleared

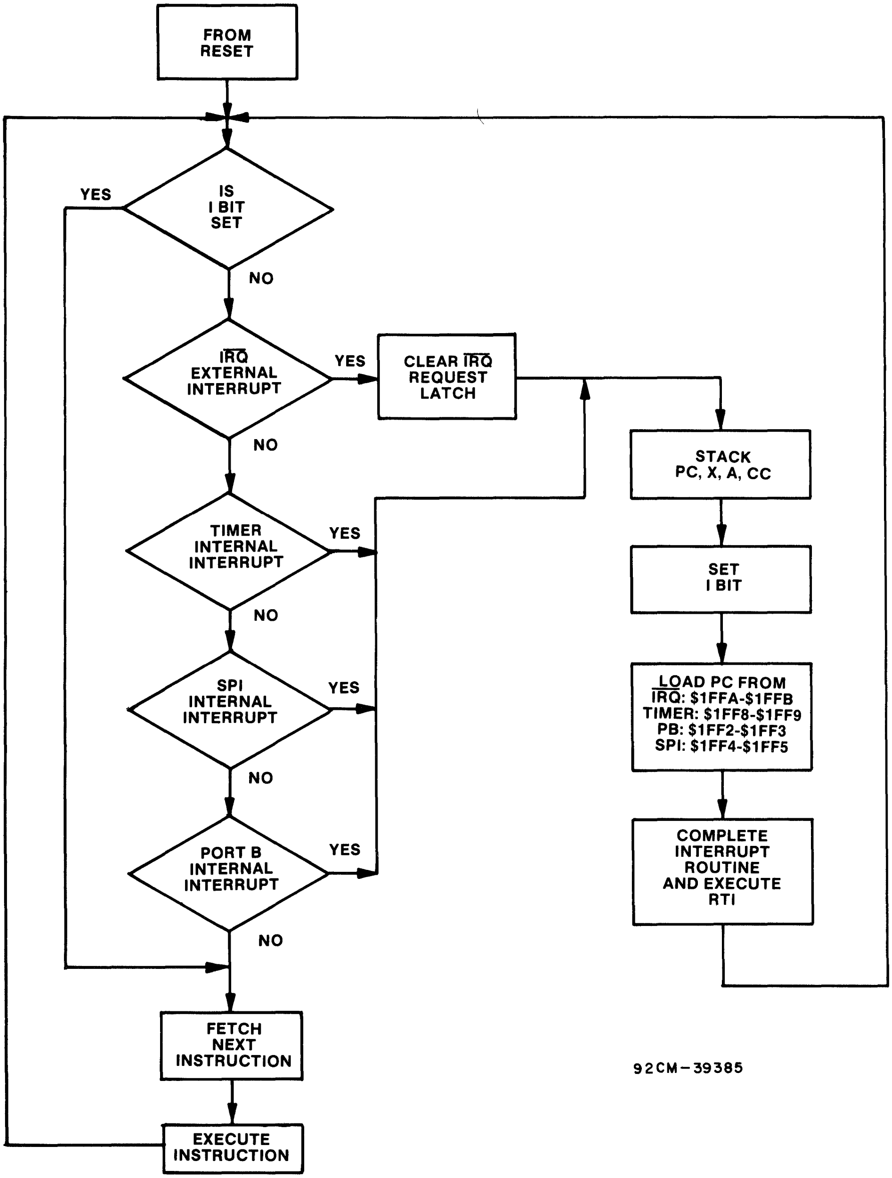
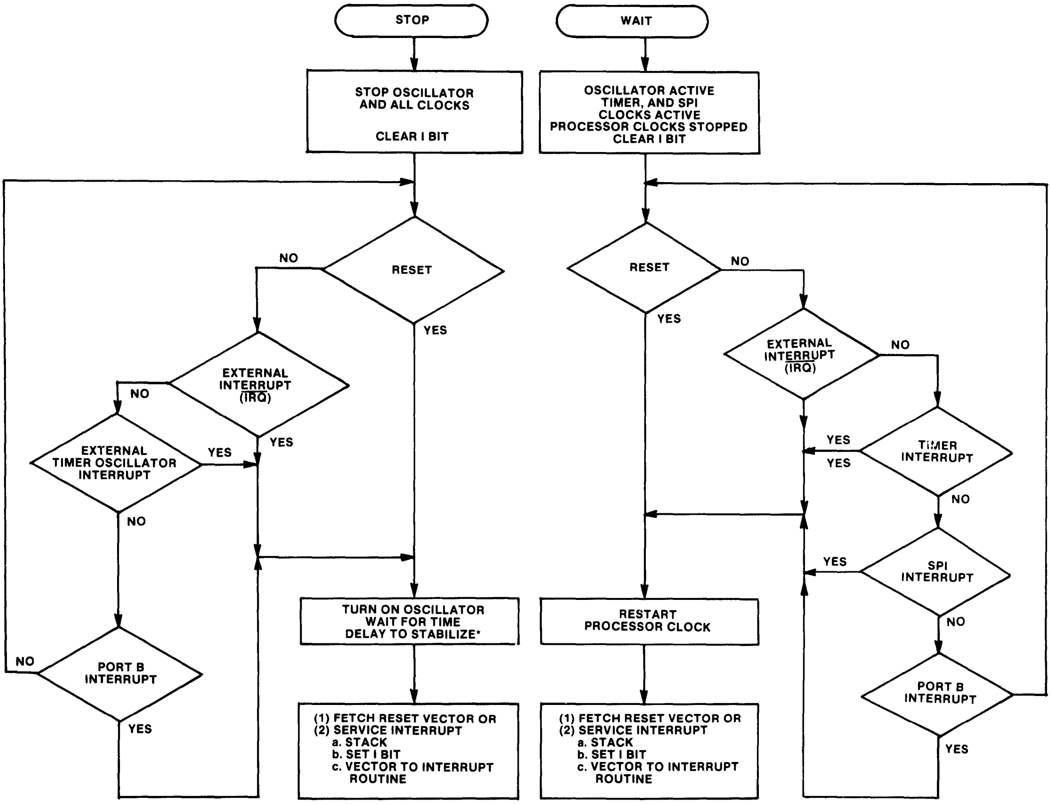


Fig. 9 - Hardware Interrupt Flowchart


STOP
STOP OSCILLATOR AND ALL CLOCKS
CLEAR I BIT
RESET
NO
YES
EXTERNAL INTERRUPT ($\overline{IRQ}$)
NO
YES
EXTERNAL TIMER OSCILLATOR INTERRUPT
YES
NO
PORT B INTERRUPT
NO
YES
TURN ON OSCILLATOR WAIT FOR TIME DELAY TO STABILIZE*
(1) FETCH RESET VECTOR OR
(2) SERVICE INTERRUPT
a. STACK
b. SET I BIT
c. VECTOR TO INTERRUPT ROUTINE
WAIT
OSCILLATOR ACTIVE TIMER, AND SPI CLOCKS ACTIVE PROCESSOR CLOCKS STOPPED CLEAR I BIT
RESET
NO
YES
EXTERNAL INTERRUPT ($\overline{IRQ}$)
NO
YES
TIMER INTERRUPT
YES
NO
SPI INTERRUPT
YES
NO
PORT B INTERRUPT
YES
RESTART PROCESSOR CLOCK
(1) FETCH RESET VECTOR OR
(2) SERVICE INTERRUPT
a. STACK
b. SET I BIT
c. VECTOR TO INTERRUPT ROUTINE

*DELAY IS PROGRAMMABLE AS 4064 OR 2 MACHINE CYCLES

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Fig. 10 - STOP/WAIT Flowcharts

Timer Interrupt

There are three different timer interrupt flags that will cause a timer interrupt whenever they are set and enabled. These three interrupt flags are found in the three most significant bits of the timer status register (TSR, location $13) and all three will vector to the same interrupt service routine ($1FF8-$1FF9). The three timer interrupt conditions are timer overflow, output compare, and input capture.

All interrupt flags have corresponding enable bits (ICIE, OCIE, and TOIE) in the timer control register (TCR, location $12). Reset clears all enable bits, thus preventing an interrupt from occurring during the reset period. The actual processor interrupt is generated only if the I bit in the condition code register is also cleared. When the interrupt is recognized, the current machine state is pushed onto the stack and I bit is set. This masks further interrupts until the present one is serviced. The interrupt service routine address is specified by the contents of memory location $1FF8 and $1FF9. The general sequence for clearing an interrupt is a software sequence of accessing the status register while the flag is set, followed by a read or write of an associated register. Refer to the PROGRAMMABLE TIMER section for additional information about the timer circuitry.

Serial Peripheral Interface (SPI) Interrupts

An interrupt in the serial peripheral interface (SPI) occurs when one of the interrupt flag bits in the serial peripheral status register (Location $0B) is set, provided the I bit in the condition code register is clear and the enable bit in the serial peripheral control register (location $0A) is enabled When the interrupt is recognized, the current state of the machine is pushed onto the stack and the I bit in the condition code register is set. This masks further interrupts until the present one is serviced. The SPI interrupt causes the program counter to vector to memory location $1FF4 and $1FF5 which contains the starting address of the interrupt

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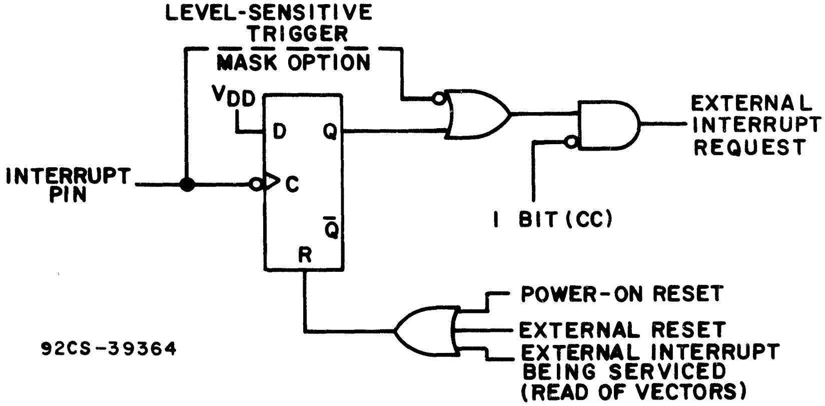
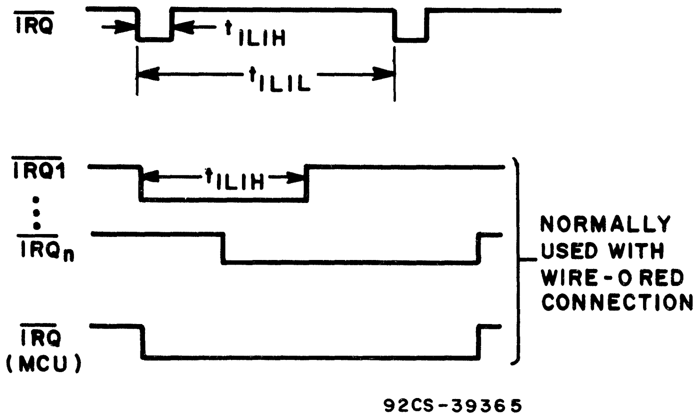


(a) Interrupt Function Diagram



Edge-Sensitive Trigger Condition
The minimum pulse width (t_{ILIH}) is either 125 ns ($V_{DD}=5$ V) or 250 ns (V_{DD} = 3 V). The period t_{ILIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routine plus 21 t_{cyc} cycles.

Level-Sensitive Trigger Condition
If after servicing an interrupt the IRQ remains low, then the next interrupt is recognized.

(b) Interrupt Mode Diagram

Fig. 11 - External Interrupt

service routine. Software in the serial peripheral interrupt service routine must determine the priority and cause of the SPI interrupt by examining the interrupt flag bits located in the SPI status register. The general sequence for clearing an interrupt is a software sequence of accessing the status register while the flag is set, followed by a read or write of an associated register. Refer to SERIAL PERIPHERAL INTERFACE section for a description of the SPI system and its interrupts.

Port B Interrupt

A Port B interrupt will occur when any one of the eight port lines (PB0-PB7) is pulled to a low level, provided the interrupt mask bit of the condition code register is clear and the enable bit (Bit 1) in the Special Port control register (Memory location $001E) is enabled. Before enabling Port B interrupts, PB0 through PB7 should be programmed as inputs, i.e., their corresponding DDR bits must be 0.

A Port B interrupt will set the Port B interrupt flag (PBIF) located in the Special Port Control/Status register (bit 7), cause the current state of the machine to be pushed onto the stack, and set the I-bit in the condition code register. This masks further interrupts until the present one is serviced. The Port B interrupt causes the Program Counter to vector to memory locations $1FF2 and $1FF3 which contain the starting address of the interrupt service routine. To clear a Port B interrupt, the user must read the Special Port Control/Status register followed by a read of Port B.

The purpose of this interrupt is to provide easy use of the PB0-PB7 lines as sensor inputs, such as in keyboard scanning. For systems where the keyboard response is not interrupt driven, this interrupt can be disabled. Programming any of these lines as outputs inhibits them from generating an interrupt.

Port B interrupts will cause an exit from the stop mode provided that the Port B interrupt enable bit is set. Port B interrupt vector is located at $1FF2, $1FF3.

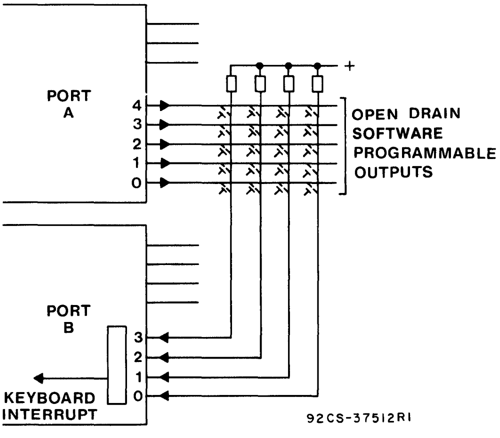


Fig. 12 - Keyboard interface.

STOP Instruction

The STOP instruction places the CDP68HC05D2 in its lowest power consumption mode. In the STOP mode the intenal oscillator is turned off, causing all internal processing to **be halted; refer to Fig. 10. During the STOP mode, the I bit in** the condition code register is cleared to enable external interrupts. All other registers and memory remain unaltered and all input/output lines remain unchanged. This continues until an external interrupt ($\overline{IRQ}$), port B interrupt, external timer oscillator interrupt, or reset is sensed, at which time the internal oscillator is turned on. These interrupts cause the program counter to vector to their respective interrupt vector locations ($1FFA and $1FFB, $1FF2 and $1FF3, $1FF8 and $1FF9, and $1FFE and $1FFF, respectively) which contain the starting addresses of the interrupt service routines.

WAIT Instruction

The WAIT instruction places the CDP68HC05D2 in a low power consumption mode, but the WAIT mode consumes somewhat more power than the stop MODE In the WAIT mode, the internal clock remains active, and all CPU processing is stopped; however, the programmable timer and serial peripheral interface systems remain active. Refer to **Fig. 10. During the WAIT mode, the I bit in the condition** code register is cleared to enable all interrupts. All other registers and memory remain unaltered and all parallel input/output lines remain unchanged. This continues until any interrupt or reset is sensed. At this time the program counter vectors to the memory location ($1FF2 through $1FFF) which contains the starting address of the interrupt or reset service routine

Data Retention Mode

The contents of RAM and CPU registers are retained at supply voltages as low as 2 Vdc. This is referred to as the data retention mode, where the data is held, but the device is not guaranteed to operate.

PROGRAMMABLE TIMER

The programmable timer, which is preceded by a fixed divide-by-four prescaler, can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from several microseconds to many seconds. A block **diagram of the timer is shown in Fig. 15 and timing diagrams are shown in Figs. 16 through 19.**

Because the timer has a 16-bit architecture, each specific functional segment (capability) is represented by two registers. These registers contain the high and low byte of that functional segment. Generally, accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

Note: The I bit in the condition code register should be set while manipulating both the high and low byte register of a specific timer function to ensure that an interrupt does not occur. This prevents interrupts from occurring between the time that the high and low bytes are accessed

The programmable timer capabilities are provided by using the following ten addressable 8-bit registers (note the high and low represent the significance of the byte). A description of each register is provided in the following pages.

Timer Control Register (TCR) location $12,
Timer Status Register (TSR) location $13,
Input Capture High Register location $14,
Input Capture Low Register location $15,
Output Compare High Register location $16,
Output Compare Low Register location $17,
Counter High Register location $18,
Counter Low Register location $19,
Alternate Counter High Register location $1A, and
Alternate Counter Low Register location $1B.

External Timer Oscillator

In addition to clocking the CDP68HC05D2's internal 16-bit timer with the CPU clock, a separate oscillator circuit may

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be used by connecting an RC or crystal circuit to pins 29 and 30 (TOSC1 and TOSC2). The circuits shown in Figs. 13(b) and 13(c) are recommended when using a crystal. This oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{tosc} in the Control Timing Tables at the end of this specification. See Fig. 13(a) for the RC circuit.

When not using the external timer oscillator feature these pins function as input lines. However, once the external timer oscillator has been enabled, PD1 will become an output only line until the processor is reset.

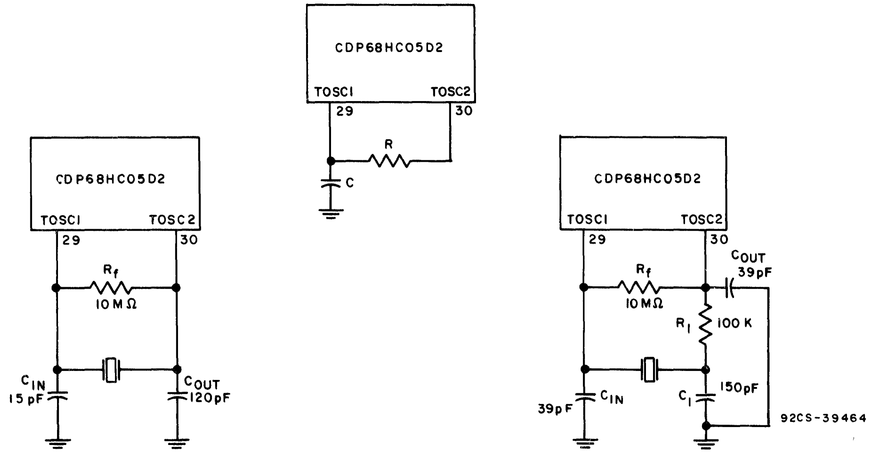
The EOE (External Oscillator Enable bit 4) and ECC (External Clock Connect bit 3) bits in the Timer Control Register control the external timer oscillator. If bit 3 (ECC) in the timer control register is set, the internal clock input to the timer is disabled and the clock to the timer is connected to the external timer oscillator This clock can be either a crystal or RC oscillator. Since this mode of operation permits the timer to continue running when the CPU is in the stop mode, timer interrupts, if enabled, will still occur and can be used to exit from the stop mode. Fig. 14 shows the timer oscillator controls. The frequency of the external oscillator must be less than one-quarter the CPU oscillator frequency.

The procedures for using this circuit are:

- Crystal Oscillator Operation — First set the EOE bit to start the crystal oscillating. When oscillation has stabilized, the ECC bit can be set to begin clocking the timer with the external timer oscillator. This time delay may vary depending upon crystal frequency and manufacturer.
- RC Oscillator Operation — When it is desired to clock the timer from an RC timer oscillator, set both the EOE and the ECC bits at the same time in order to keep power consumption minimal.
- No external timer oscillator being used — If the EOE bit is never set, the oscillator will remain in its high impedance state allowing its pins to be used as PD0 and PD1 input lines. In this case, these pins function as normal inputs and should not be left floating.
- Timer Oscillator used for event counting — Set both the EOE and ECC bits and drive the timer oscillator input pin with the event signal which is to be counted. If EOE remains reset and only ECC is set, the event signal can be connected to the timer oscillator output pin, and the input can be used as a Port D input line.

Fig. 13 - External Timer Oscillator Connections

(a) RC Oscillator Connections



(b) Crystal Oscillator connections for crystal speeds above approx. 400 KHz. The C_{in} and C_{out} values may vary depending upon crystal manufacturer.

(c) Crystal Oscillator connections for crystal speeds below approx. 400 KHz. The C_{in}, C_1 and R_1 values shown work well for most 32.768 KHz crystals; however, sizes may vary depending upon crystal frequency manufacturer.

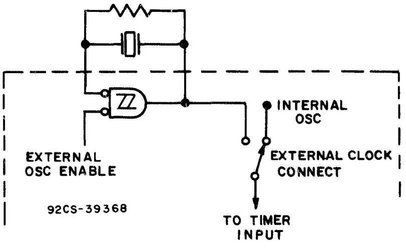


Fig. 14 - External Timer Oscillator Controls

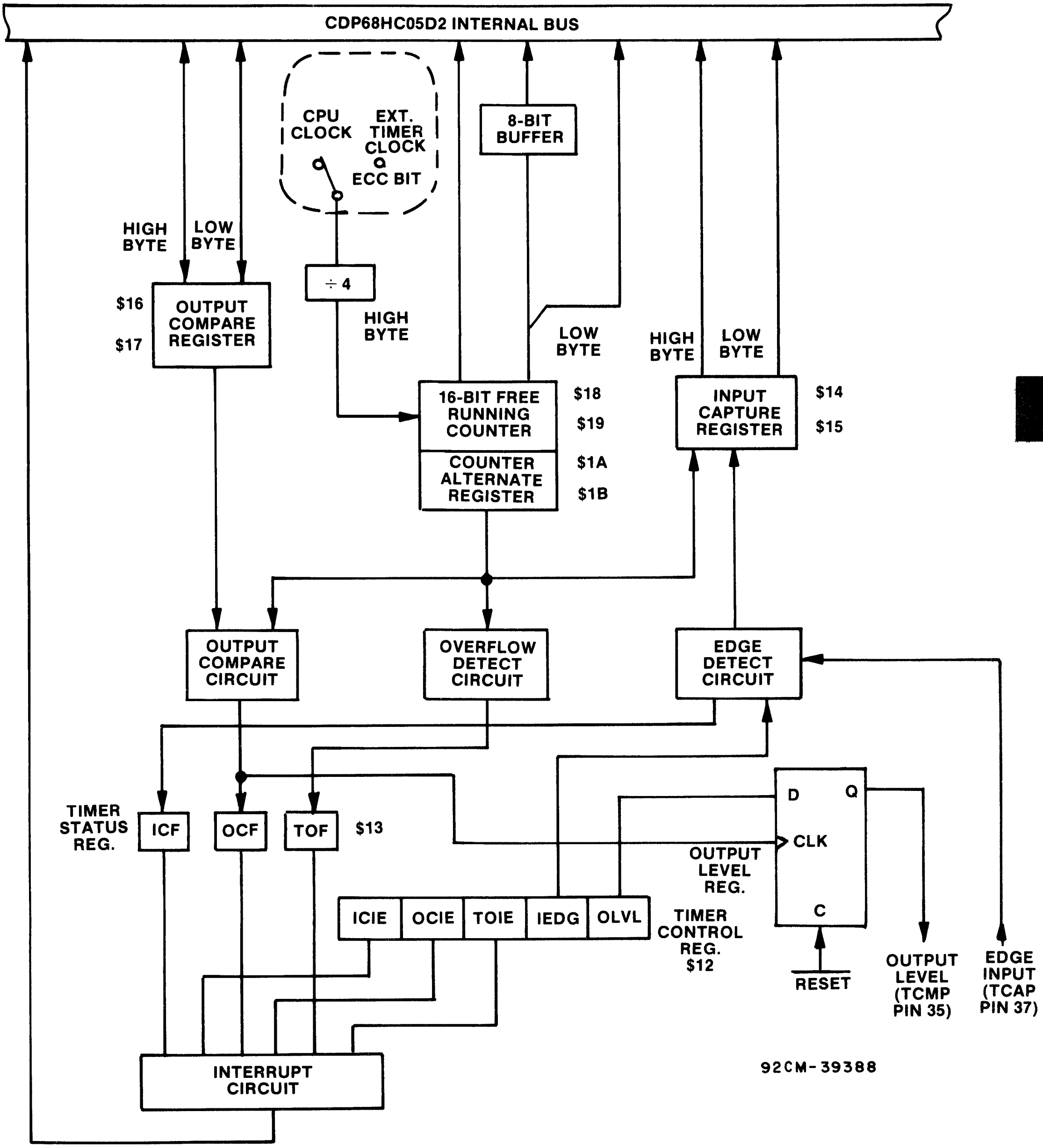


Fig. 15 - Programmable Timer Block Diagram

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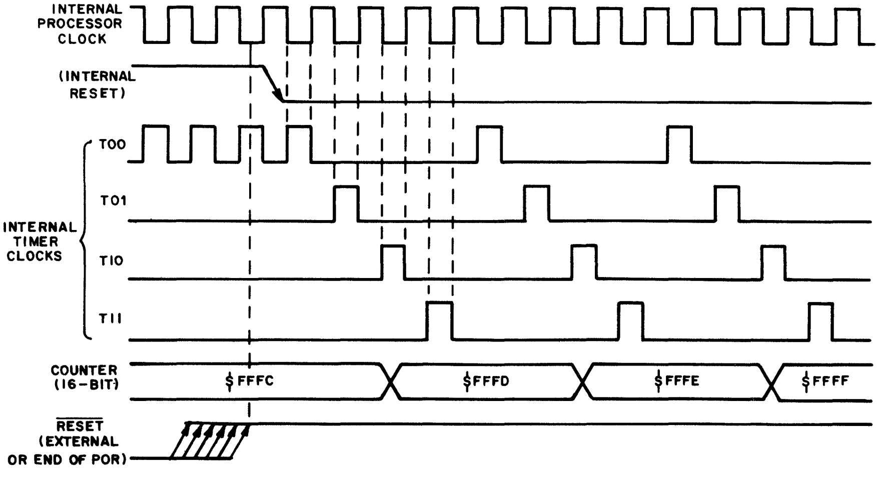
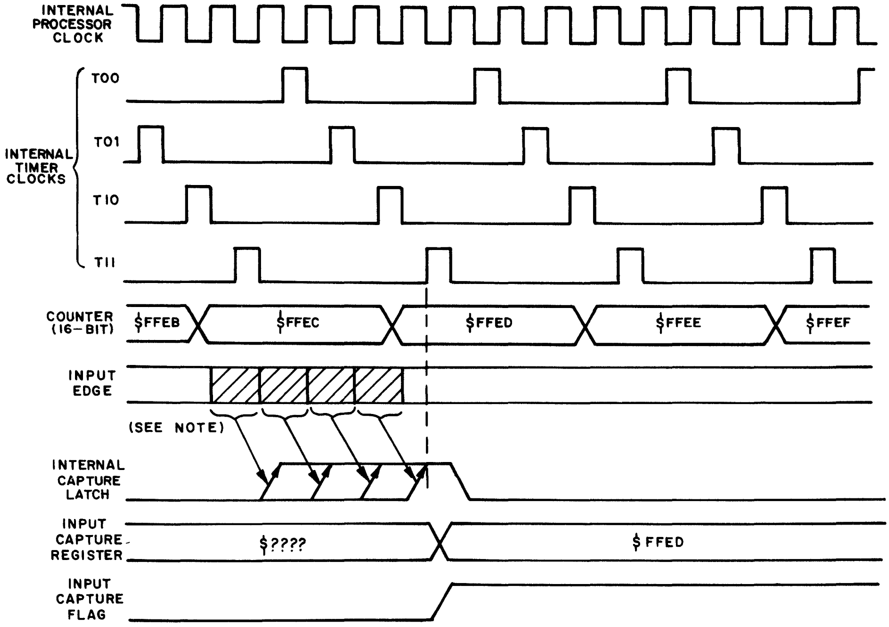


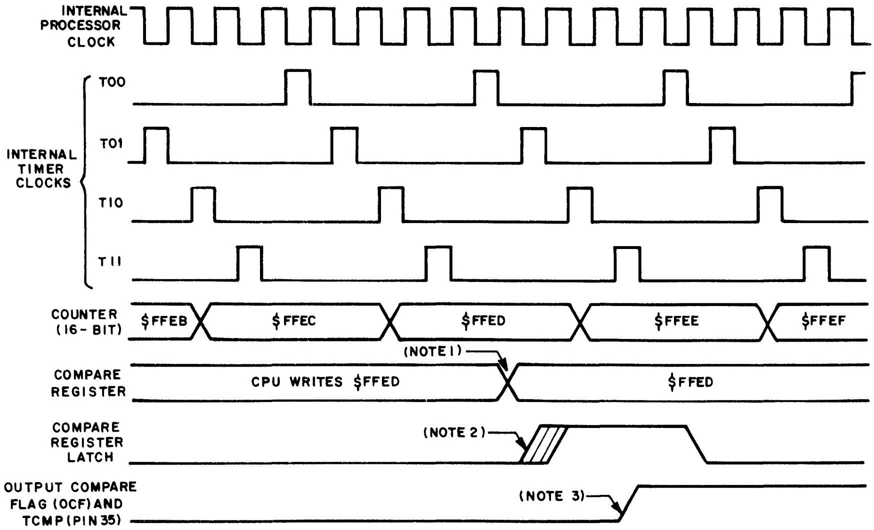
NOTE:
THE COUNTER REGISTER AND TIMER CONTROL REGISTER ARE THE ONLY ONES AFFECTED BY RESET.

Fig. 16 - Timer State Timing Diagram For Reset



NOTE:
IF THE INPUT EDGE OCCURS IN THE SHADED AREA FROM ONE TIMER STATE T10 TO THE OTHER TIMER STATE T10, THE INPUT CAPTURE FLAG IS SET DURING THE NEXT STATE T11

Fig. 17 - Timer State Timing Diagram For Input Capture



NOTES:
1. THE CPU WRITE TO THE COMPARE REGISTER MAY TAKE PLACE AT ANY TIME, BUT A COMPARE ONLY OCCURS AT TIMER STATE T01 THUS, A 4-CYCLE DIFFERENCE MAY EXIST BETWEEN THE WRITE TO THE COMPARE REGISTER AND THE ACTUAL COMPARE
2. INTERNAL COMPARE TAKES PLACE DURING TIMER STATE T01
3. OCF IS SET AT THE TIMER STATE T11 WHICH FOLLOWS THE COMPARISON MATCH ($FFED IN THIS EXAMPLE)

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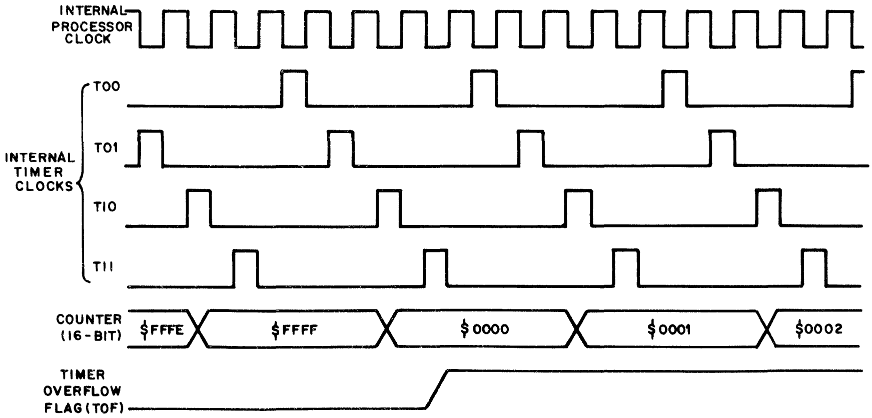
Fig. 18 - Timer State Timing Diagram For Output Compare



NOTE·
THE TOF BIT IS SET AT TIMER STATE T11 (TRANSITION OF COUNTER FROM $FFFF TO $0000). IT IS CLEARED BY A READ OF THE TIMER STATUS REGISTER DURING THE INTERNAL PROCESSOR CLOCK HIGH TIME FOLLOWED BY A READ OF THE COUNTER LOW REGISTER.

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Fig. 19 - Timer State Diagram For Timer Overflow

Counter

The key element in the programmable timer is a 16-bit free-running counter, or counter register, preceded by a prescaler which divides the internal processor clock by four The prescaler gives the timer a resolution of 2.0 microseconds if the internal processor clock is 2.0 MHz. The counter is clocked to increasing values during the low portion of the internal processor clock. Software can read the counter at any time without affecting its value

The double-byte free-running counter can be read from either of two locations $18-$19 (called counter register at this location), or $1A-$1B (counter alternate register at this location) A read sequence containing only a read of the least significant byte of the free-running counter ($19, $1B) will receive the count value at the time of the read. If a read of the free-running counter or counter alternate register first addresses the most significant byte ($18, $1A) it causes the least significant byte ($19, $1B) to be transferred to a buffer. This buffer value remains fixed after the first most significant byte "read" even if the user reads the most significant byte several times. This buffer is accessed when reading the free-running counter or counter alternate register least significant byte ($19 or $1B), and thus completes a read sequence of the total counter value. Note that in reading either the free-running counter or counter alternate register, if the most significant byte is read, the least significant byte must also be read in order to complete the sequence.

The free-running counter is configured to $FFFC during reset and is always a read-only register. During a power-on-reset (POR), the counter is also configured to $FFFC and begins running after the oscillator startup delay. Because the free-running counter is 16 bits preceded by a fixed divide-by-four prescaler, the value in the free-running counter repeats every 262,144 MPU internal processor clock cycles. When the counter rolls over from $FFFF to $0000, the timer overflow flag (TOF) bit is set. An interrupt can also be enabled when counter rollover occurs by setting its interrupt enable bit (TOIE).

Output Compare Register

The output compare register is a 16-bit register, which is made up of two 8-bit registers at locations $16 (most significant byte) and $17 (least significant byte). The output compare register can be used for several purposes, such as, controlling an output waveform or indicating when a period of time has elapsed The output compare register is unique in that all bits are readable and writeable and are not altered by the timer hardware Reset does not affect the contents of this register and if the compare function is not utilized, the two bytes of the output compare register can be used as storage locations.

The contents of the output compare register are compared with the contents of the free-running counter once during every four internal processor clocks. If a match is found, the corresponding output compare flag (OCF) bit is set and the corresponding output level (OLVL) bit is clocked (by the output compare circuit pulse) to an output level register. The values in the output compare register and the output level bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit, OCIE, is set.

After a processor write cycle to the output compare register containing the most significant byte ($16), the output compare function is inhibited until the least significant byte ($17) is also written. The user must write both bytes (locations) if the most significant byte is written first A write made only to the least significant byte ($17) will not inhibit the compare function The free-running counter is updated every four internal processor clock cycles due to the internal prescaler. The minimum time required to update the output compare register is a function of the software program rather than the internal program

A processor write may be made to either byte of the output compare register without affecting the other byte. The output level (OLVL) bit is clocked to the output level register regardless of whether the output compare flag (OCF) is set or clear.

Because neither the output compare flag (OCF bit) nor output compare register is affected by reset, care must be exercised when initializing the output compare function with software. The following procedure is recommended:

(1) Write the high byte of the output compare register to inhibit further compares until the low byte is written.
(2) Read the timer status register to arm the OCF if it is already set.
(3) Write the output compare register low byte to enable the output compare function with the flag clear.

The advantage of this procedure is to prevent the OCF bit from being set between the time it is read and the write to the output compare register. A software example is shown below.

```
B7  16  STA  OCMPHI   INHIBIT OUTPUT COMPARE
B6  13  LDA  TSTAT    ARM OCF BIT IF SET
BF  17  STX  OCMPLD   READY FOR NEXT COMPARE
```

Input Capture Register

The two 8-bit registers which make up the 16-bit input capture register are read-only and are used to latch the value of the free-running counter after a defined transition is sensed by the corresponding input capture edge detector. The level transition which triggers the counter transfer is defined by the corresponding input edge bit (IEDG). Reset does not affect the contents of the input capture register.

The result obtained by an input capture will be one more than the value of the free-running counter on the rising edge of the internal processor clock preceding the external **transition (refer to timing diagram shown in Fig. 17). This** delay is required for external synchronization. Resolution is affected by the prescaler allowing the timer to only increment every four internal processor clock cycles

The free-running counter contents are transferred to the input capture register on each proper signal transition regardless of whether the input capture flag (ICF) is set or clear. The input capture register always contains the free-running counter value which corresponds to the most recent input capture.

After a read of the most significant byte of the input capture register ($14), counter transfer is inhibited until the least significant byte ($15) of the input capture register is also read. This characteristic forces the minimum pulse period attainable to be determined by the time used in the capture software routine and its interaction with the main program. A polling routine using instructions such as BRSET, BRA, LDA, STA, INCX, CMPX, and BEG might take 34 machine cycles to complete The free-running counter increments every four internal processor clock cycles due to the prescaler. A read of the least significant byte ($15) of the input capture register does not inhibit the free-running counter transfer. Again, minimum pulse periods are ones which allow software to read the least significant byte ($15) and perform the needed operations. There is no conflict between the read of the input capture register and the free-running counter since they occur on opposite edges of the internal processor clock.

Timer Control Register (TCR)

The timer control register (TCR, location $12) is an 8-bit read/write register which contains seven control bits. Three of these bits control interrupts associated with each of the three flag bits found in the timer status register (discussed below). The other four bits control: 1) which edge is significant to the input capture edge detector (i.e., negative or positive), 2) the next value to be clocked to the output level register in response to a successful output compare, 3) the source of the timer clock, and 4) whether the external timer oscillator is enabled. The timer control register and the free-running counter are the only sections of the timer affected by reset. The TCMP pin is forced low during external reset and stays low until a valid compare changes it to a high. The timer control register is illustrated below followed by a definition of each bit.

7	6	5	4	3	2	1	0	
ICIE	OCIE	TOIE	EOE	ECC	0	IEDG	OLVL	$12

B7, ICIE	If the input capture interrupt enable (ICIE) bit is set, a timer interrupt is enabled when the ICF status flag (in the timer status register) is set. If the ICIE bit is clear, the interrupt is inhibited. The ICIE bit is cleared by reset.
B6, OCIE	If the output compare interrupt enable (OCIE) bit is set, a timer interrupt is enabled whenever the OCF status flag is set. If the OCIE bit is clear, the interrupt is inhibited. The OCIE bit is cleared by reset.
B5, TOIE	If the timer overflow interrupt enable (TOIE) bit is set, a timer interrupt is enabled whenever the TOF status flag (in the timer status register) is set If the TOIE bit is clear, the interrupt is inhibited. The TOIE bit is cleared by reset.
B4, EOE	External Oscillator Enable — If set, the external timer oscillator is enabled. If it is then cleared, the inverter between pins 29 and 30 is prevented from switching and cannot be used in a crystal or RC oscillator. This bit is cleared by reset which configures both TOSC1 and TOSC2 as inputs.
B3, ECC	If the external clock connect (ECC) is set, the internal clock input to the timer is disabled and the timer oscillator is connected to the input to the timer It is cleared by reset. Accuracy of the timer count is not guaranteed while this bit is switched.
B1, IEDG	The value of the input edge (IEDG) bit determines which level transition on pin 37 will trigger a free-running counter transfer to the input capture register. Reset clears the IEDG bit. 0 = negative edge 1 = positive edge
B0, OLVL	The value of the output level (OLVL) bit is clocked into the output level register by the next successful output compare and will appear at pin 35. This bit and the output level register are cleared by reset. 0 = low output 1 = high output

Timer Status Register (TSR)

The timer status register (TSR) is an 8-bit register of which the three most significant bits contain read-only status information. These three bits indicate the following:

1. A proper transition has taken place at pin 37 with an accompanying transfer of the free-running counter contents to the intput capture register,
2. A match has been found between the free-running counter and the output compare register, and
3. A free-running counter transition from $FFFF to $0000 has been sensed (timer overflow)

The timer status register is illustrated below followed by a definition of each bit. Refer to timing diagrams shown in **Fig. 16, 17, and 18 for timing relationship to the timer status register bits.**

7	6	5	4	3	2	1	0	
ICF	OCF	TOF	0	0	0	0	0	$13

B7, ICF	The input capture flag (ICF) is set when a proper edge has been sensed by the input capture edge detector. It is cleared by a processor read of the timer status register (with ICF set) followed by reading the low byte ($15) of the input capture register. Reset does not affect the input compare flag.
B6, OCF	The output compare flag (OCF) is set when the output compare register contents matches the contents of the free-running counter. The OCF is cleared by reading the timer status register (with the OCF set) and then writing to the low byte ($17) of the output compare register. Reset does not affect the output compare flag.
B5, TOF	The timer overflow flag (TOF) bit is set by a transition of the free-running counter from $FFFF to $0000 It is cleared by reading the timer status register (with TOF set) followed by a read of the free-running counter least significant byte ($19). Reset does not affect the TOF bit.

Reading the timer status register satisfies the first condition required to clear any status bits which happened to be set during the access. The only remaining step is to provide an access of the register which is associated with the status bit. Typically, this presents no problem for the input capture and output compare functions.

A problem can occur when using the timer overflow function and reading the free-running counter at random times to measure an elapsed time. Without incorporating the proper precautions into software, the timer overflow flag could unintentionally be cleared if: 1) the timer status register is read when TOF is set, and 2) the least significant byte of the free-running counter is read but not for the purpose of servicing the flag. The counter alternate register at address $1A and $1B contains the same value as the free-running counter (at address $18 and $19); therefore, this

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alternate register can be read at any time without affecting the timer overflow flag in the timer status register.

During STOP and WAIT instructions, the programmable timer functions as follows if using the CPU clock: during the wait mode, the timer continues to operate normally and may generate an interrupt to trigger the CPU out of the wait state; during the stop mode, the timer holds at its current state, retaining all data, and resumes operation from this point when an external interrupt is received. If using an external timer oscillator the timer will continue to count and generate interrupts.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is a four wire synchronous serial communication system with separate wires for input data, output data, clock and slave select. A master MCU, which produces the clocking signal, initiates the exchange of data bytes with a slave MCU or peripheral device such as an LCD display driver or an A/D converter. A diagram of the control, status, and data registers may be found in the section labelled "Registers". The SPI system registers are found at addresses $000A-$000C. The SPI output drivers may be switched off to allow the user access to external pins for use as parallel inputs to Port D. Upon power-up or reset the SPI output drivers will be initialized in the off state. The serial system enable bit which controls the output drivers and other functional inhibits is the SPE bit found in the serial control register.

Fig. 20 illustrates two different system configurations **Fig. 20**a represents a system of five different MCUs in which there are one master and four slaves (0, 1, 2, 3). In this system four basic lines (signals) are required for the MOSI (master out, slave in), MISO (master in, slave out), SCK (serial clock), and $\overline{\text{SS}}$ (slave select) lines. **Fig. 20**b represents a system of three MCUs in which each MCU is capable of being a master or a slave. The SPI interface is well-suited for multiprocessor communications.

Features

- Full duplex, three-wire synchronous transfers
- Master or slave operation
- 1.05 MHz (maximum) master bit frequency
- 2.1 MHz (maximum) slave bit frequency
- Four programmable master bit rates
- Programmable clock polarity and phase
- End of transmission interrupt flag
- Write collision flag protection
- Master-Master mode fault protection capability

Signal Description

The four basic signals (MOSI, MISO, SCK, and $\overline{\text{SS}}$) discussed above are described in the following paragraphs. Each signal function is described for both the master and slave mode.

Master Out Slave In (MOSI)

The MOSI pin is configured as a data output in a master (mode) device and as a data input in a slave (mode) device. In this manner data is transferred serially from a master to a slave on this line; most significant bit first, least significant bit last. The timing diagrams of **Fig. 21** summarize the SPI timing diagram and show the relationship between data and clock (SCK). As shown in **Fig. 21** four possible timing relationships may be chosen by using control bits CPOL and CPHA. The master device always allows data to be applied on the MOSI line a half-cycle before the clock edge (SCK) in order for the slave device to latch the data.

Note: Both the slave device(s) and a master device must be programmed to similar timing modes for proper data transfer

When the master device transmits data to a second (slave) device via the MOSI line, the slave device responds by sending data to the master device via the MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal (one which is provided by the master device). Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receiver-full status bits. A single status bit (SPIF) is used to signify that the I/O operation is complete.

Configuration of the MOSI pin is a function of the MSTR bit in the serial peripheral control register (SPCR, loction $0A). Setting the MSTR bit will place the device in the Master mode and cause the MOSI pin to be an output.

Note: The Port D Data Direction Register bit 3 must be set for the MOSI pin to transfer data in the Master mode

Master In Slave Out (MISO)

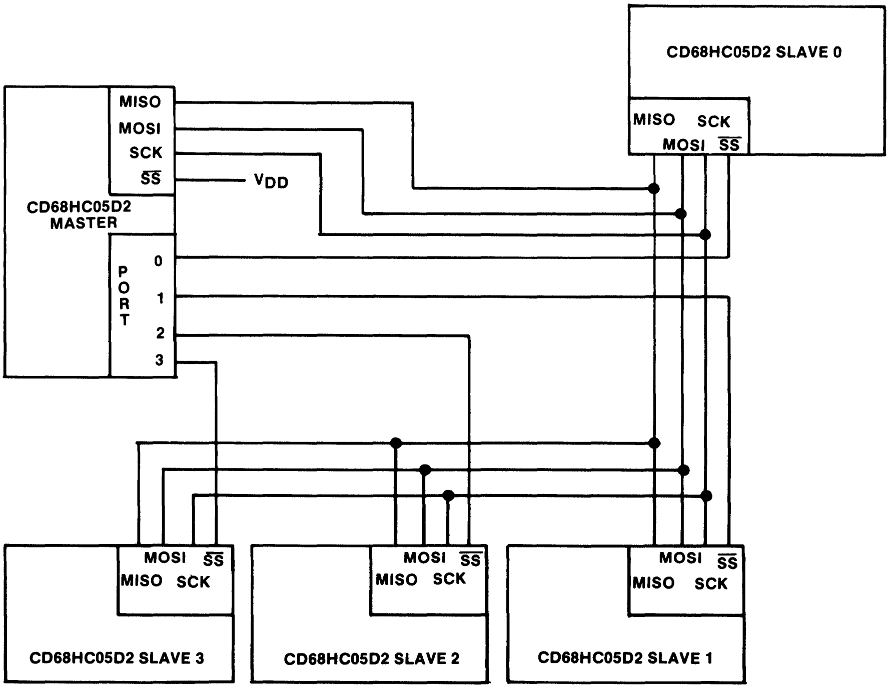
The MISO pin is configured as an input in a master (mode) device and as an output in a slave (mode) device In this manner data is transferred serially from a slave to a master on this line; most significant bit first, least significant bit last. The MISO pin of a slave device is placed in the high-impedance state if it is not selected by the master; i.e., its $\overline{\text{SS}}$ pin is a logic one. The timing diagram of **Fig. 21** shows the relationship between data and clock (SCK) As shown in **Fig. 21**, four possible timing relationships may be chosen by using control bits CPOL and CPHA. The master device always allows data to be applied on the MOSI line a half-cycle before the clock edge (SCK) in order for the slave device to latch the data.

Note: The slave device (s) and a master device must be programmed to similar timing modes for proper data transfer

When the master device transmits data to a slave device via the MOSI line, the slave device responds by sending data to the master device via the MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal (one which is provided by the master device). Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receiver-full status bits. A single status bit (SPIF) in the serial peripheral status register (SPSR, location $0B) is used to signify that the I/O operation is complete.

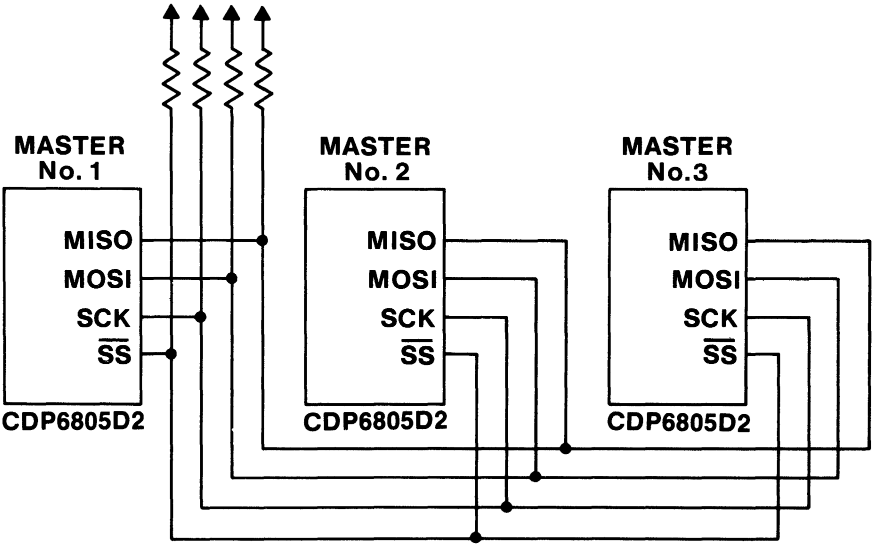
In the master device, the MSTR control bit in the serial peripheral control register (SPCR, location $0A) is set to a logic one (by the program) to allow the master device to receive data on its MISO pin. In the slave device, its MISO pin is enabled by the logic level of the $\overline{\text{SS}}$ pin; i.e., if $\overline{\text{SS}}$=1 then the MISO pin is placed in the high-impedance state, whereas, if $\overline{\text{SS}}$=0 the MISO pin is an output for the slave device

Note: The Port D Data Direction Register bit 2 must be set for the MISO pin to transfer data in the slave mode



(a) Single Master, Four Slaves

92CM-39384



(b) Multimaster System

92CS-37494

Fig. 20 - Master-Slave System Configuration

CDP68HC05D2

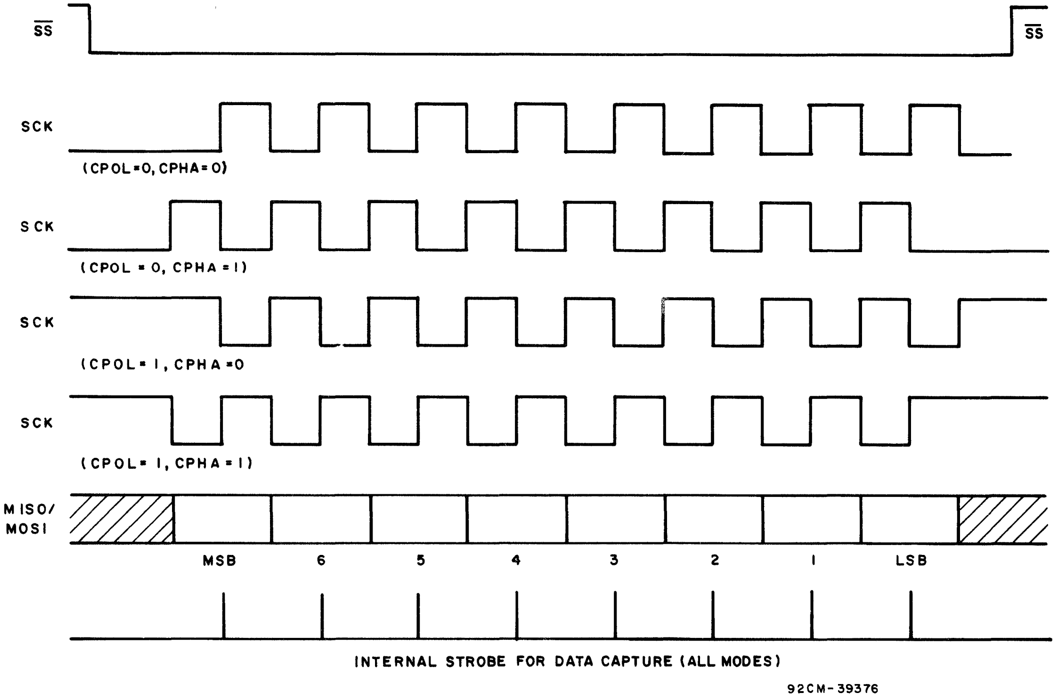


Fig. 21 - Data Clock Timing Diagram

Slave Select ($\overline{SS}$)

In the slave mode the slave select ($\overline{SS}$) pin is an input (PD5, pin 34), which receives an active low signal that is generated by the master device to enable slave device(s) to accept data. To ensure that data will be accepted by a slave device, the $\overline{SS}$ signal line must be a logic low prior to occurrence of SCK (system clock) and must remain low until after the last (eighth) SCK cycle. Fig. 21 illustrates the relationship between SCK and the data for two different level combinations of CPHA, when $\overline{SS}$ is pulled low. These are: 1) with CPHA=1 of 0, the first bit of data is applied to the MISO line for transfer, and 2) when CPHA = 0 the slave device is prevented from writing to its data register. Refer to the WCOL status flag in the serial peripheral status register (location $0B) description for further information on the effects that the SS input and CPHA control bit have on the I/O data register. A high level SS signal forces the MISO (master in, slave out) line to the high-impedance state. Also, SCK and the MOSI (master out, slave in) line are ignored by a slave device when its $\overline{SS}$ signal is high.

When a device is a master, it monitors its $\overline{SS}$ signal for a logic low, provided that Port D bit 5 is cleared. See Note. The master device will become a slave device any time its $\overline{SS}$ signal is detected low. This ensures that there is only one master controlling the $\overline{SS}$ line for a particular system. When the $\overline{SS}$ line is detected low, it clears the MSTR control bit (serial peripheral control register, location $0A). Also, control bit SPE in the serial peripheral control register is cleared which causes the serial peripheral interface (SPI) to be disabled (port D SPI pins become inputs). The MODF flag bit in the serial peripheral status register (location $0B) is also set to indicate to the master device that another device is attempting to become a master. Two devices attempting to be outputs are normally the result of a software error; however, a system could be configured which would contain a default master which would automatically "take over" and restart the system.

Note: In the master mode Port D DDR bit 5 determines whether Port D bit 5 ($\overline{SS}$) is an error detect input to the SPI (DDR bit 5 clear) or a general-purpose output line (DDR bit 5 set), that can be used to strobe the $\overline{SS}$ lines of slaves

Serial Clock (SCK)

The serial clock is used to synchronize the movement of data both in and out of the device through its MOSI and MISO pins. The master and slave devices are capable of exchanging a data byte of information during a sequence of eight clock pulses. Since the SCK is generated by the master device, the SCK line becomes an input on all slave devices and synchronizes slave data transfer. The type of clock and its relationship to data are controlled by the CPOL and CPHA bits in the serial peripheral control register (location $0A) discussed below. Refer to Fig. 21 for timing.

The master device generates the SCK through a circuit driven by the internal processor clock. Two bits (SPR0 and SPR1) in the serial peripheral control register (location $0A) of the master device select the clock rate. The master device uses the SCK to latch incoming slave device data on the MISO line and shifts out data to the slave on the MOSI line. Both master and slave devices must be operated in the same timing mode as controlled by the CPOL and CPHA bit in the serial peripheral control register. In the slave device, SPR0 and SPR1 have no effect on the operation of the Serial Peripheral Interface. Timing is shown in Fig. 21.

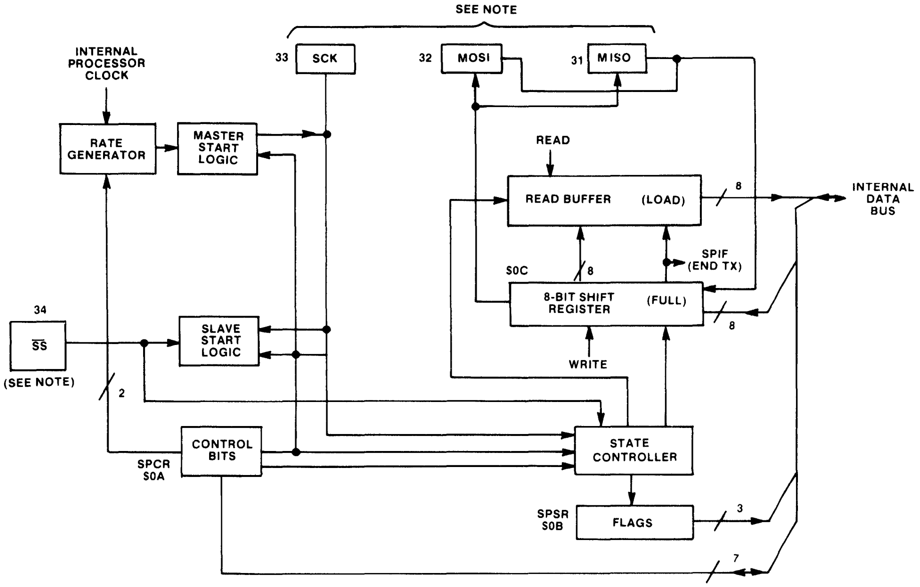
Note: The Port D Data Direction Register bit 4 must be set for the SCK pin to generate (output) a SCK signal

Functional Description

A block diagram of the serial peripheral interface (SPI) is shown in Fig. 22. In a master configuration the master start logic receives an input from the CPU (in the form of a write to the SPI rate generator) and originates the system clock (SCK) based on the internal processor clock. This clock is also used internally to control the state controller as well as the 8-bit shift register. As a master device, data is parallel loaded into the 8-bit shift register (from the internal bus) during a write cycle and then shifted out serially to the MOSI pin for application to the slave device(s). During a read cycle, data is applied serially from a slave device via the MISO pin to the 8-bit shift register After the 8-bit shift register is loaded, its data is parallel transferred to the read buffer and then is made available to the internal data bus during a CPU read cycle

In a slave configuration, the slave start logic receives a logic low (from a master device) at the $\overline{SS}$ pin and a system clock input (from the same master device) at the SCK pin Thus, the slave is synchronized with the master Data from the master is received serially at the slave MOSI pin and loads the 8-bit shift register After the 8-bit shift register is loaded, its data is parallel transferred to the read buffer and then is made available to the internal data bus during a CPU read cycle. During a write cycle, data is parallel loaded into the 8-bit shift register from the internal data bus and then shifted out serially to the MISO pin for application to the master device

Fig. 23 illustrates the MOSI, MISO, and SCK master-slave interconnections. Note that in Fig. 23 the master $\overline{SS}$ pin is tied to a logic high and the slave $\overline{SS}$ pin is a logic low. Fig 21a provides a larger system connection for these same pins. Note that in Fig. 20(a), all $\overline{SS}$ pins are connected to a port pin of a master/slave device. In this case any of the devices can be a slave.



NOTES
THE $\overline{SS}$, SCK, MOSI, AND MISO ARE EXTERNAL PINS WHICH PROVIDE THE FOLLOWING FUNCTIONS
(a) MOSI-PROVIDES SERIAL OUTPUT TO SLAVE UNIT(S) WHEN DEVICE IS CONFIGURED AS A MASTER RECEIVES SERIAL INPUT FROM MASTER UNIT WHEN DEVICE IS CONFIGURED AS A SLAVE UNIT
(b) MISO-RECEIVES SERIAL INPUT FROM SLAVE UNIT(S) WHEN DEVICE IS CONFIGURED AS A MASTER PROVIDES SERIAL OUTPUT TO MASTER WHEN DEVICE IS CONFIGURED AS A SLAVE UNIT
(c) SCK -PROVIDES SYSTEM CLOCK WHEN DEVICE IS CONFIGURED AS A MASTER UNIT RECEIVES SYSTEM CLOCK WHEN DEVICE IS CONFIGURED AS A SLAVE UNIT
(d) $\overline{SS}$ -PROVIDES A LOGIC LOW TO SELECT A SLAVE DEVICE FOR A TRANSFER WITH A MASTER DEVICE

92CM-39390

Fig. 22 - Serial Peripheral Interface Block Diagram

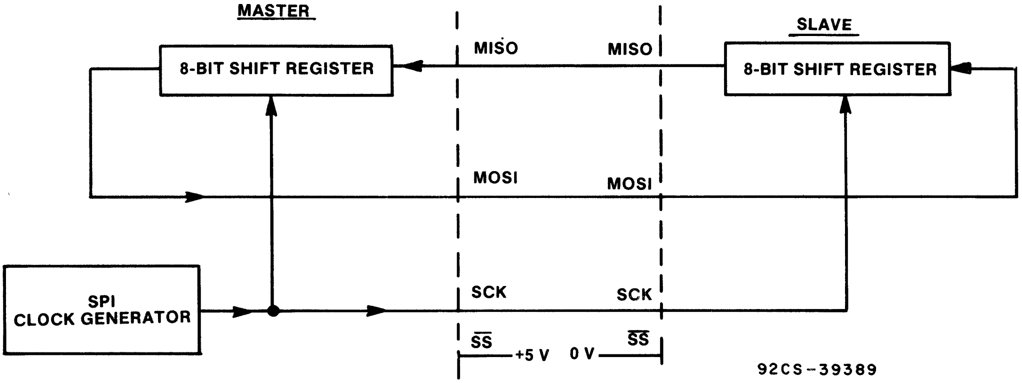


Fig. 23 - Serial Peripheral Interface Master-Slave Interconnection

Registers

There are three registers in the serial parallel interface which provide control, status, and data storage functions These registers, which include the serial peripheral control register (SPCR, location $0A), serial peripheral status register (SPSR, location $0B), and serial peripheral data I/O register (SPDR, location $0C) are described below.

Note: In addition, the Port D Data Direction Register (DDR) must be properly configured See note in the section labelled "Input/Output Programming-Special-Purpose Port"

Serial Peripheral Control Register (SPCR)

7	6	5	4	3	2	1	0	
SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	$0A

The serial peripheral control register bits are defined as follows.

B7, SPIE	When the serial peripheral interrupt enable bit is high, it allows the occurrence of a processor interrupt, and forces the proper vector to be loaded into the program counter if the serial peripheral status register flag bit (SPIF and/or MODF) is set to a logic one. It does not inhibit the setting of a status bit. The SPIE bit is cleared by reset.
B6, SPE	When the serial peripheral output enable control bit is set, all output drive is applied to the external pins and the system is enabled. When the SPE bit is set, it enables the SPI system by connecting it to the external pins thus allowing it to interface with the external SPI bus. The pins that are defined as output depend on which mode (master or slave) the device is in Because the SPE bit is cleared by reset, the SPI system is not connected to the external pins upon reset.
B5, DWOM	The Port D Wire-OR Mode bit controls the output buffers for Port D bits 2 through 5 If DWOM=1, the four Port D output buffers behave as open-drain outputs. If DWOM=0, the four Port D output buffers operate as normal CMOS outputs. DWOM is cleared by reset.
B4, MSTR	The master bit determines whether the device is a master or a slave. If the MSTR bit is a logic zero it indicates a slave device and a logic one denotes a master device. If the master mode is selected, the function of the SCK pin changes from an input to an output and the function of the MISO and MOSI pins are reversed. This allows the user to wire device pins MISO to MISO, and MOSI to MOSI and SCK to SCK without incident. The MSTR bit is cleared by reset, therefore, the device is always placed in the slave mode during reset.
B3, CPOL	The clock polarity bit controls the normal or steady state value of the clock when data is not being transferred. The CPOL bit affects both the master and slave modes It must be used in conjunction with the clock phase control bit (CPHA) to produce the wanted clock-data relationship between a master and a slave device. When the CPOL bit is a logic zero, it produces a steady state low value at the SCK pin of the master device If the CPOL bit is a logic one, a high value is produced at the SCK pin of the master device when data is not being transferred. The CPOL bit is not affected by **reset. Refer to Fig. 21.**
B2, CPHA	The clock phase bit controls the relationship between the data on the MISO and MOSI pins and the clock produced or received at the SCK pin. This control has effect in both the master and slave modes. It must be used in conjunction with the clock polarity control bit (CPOL) to produce the wanted clock-data relation. The CPHA bit in general selects the clock edge which captures data and allows it to change states. It has its greatest impact on the first bit transmitted (MSB) in that it does or does not allow a clock transition before the first data capture edge. The CPHA bit is not affected by **reset. Refer to Fig. 21.**
B1, SPR1 B0, SPR0	These two serial peripheral rate bits select one of four baud rates to be used as SCK if the device is a master; however, they have no effect in the slave mode. The slave device is

capable of shifting data in and out at a maximum rate which is equal to the CPU clock (maximum = 2.1 MHz). A rate table is given below for the generation of the SCK from the master The SPR1 and SPR0 bits are not affected by reset

SPR1	SPR0	Internal Processor Clock Divide By
0	0	2
0	1	4
1	0	16
1	1	32

Serial Peripheral Status Register (SPSR)

7	6	5	4	3	2	1	0	
SPIF	WCOL	—	MODF	—	—	—	—	$0B

The status flags which generate a serial peripheral interface (SPI) interrupt will not be blocked by the SPIE control bit in the serial peripheral control register; however, the interrupt will be blocked The WCOL bit does not cause an interrupt. The serial peripheral status register bits are defined as follows:

B7, SPIF The serial peripheral data transfer flag bit notifies the user that a data transfer between the device and an external device has been completed. With the completion of the data transfer, SPIF is set, and if SPIE is set, a serial peripheral interrupt (SPI) is generated. During the clock cycle that SPIF is being set, a copy of the received data byte in the shift register is moved to a buffer When the data register is read, it is the buffer that is read. During an overrun condition, when the master device has sent several bytes of data and the slave device has not responded to the first SPIF, only the first byte sent is contained in the receiver buffer and all other bytes are lost.

The transfer of data is initiated by the master device writing its serial peripheral data register.

Clearing the SPIF bit is accomplished by a software sequence of accessing the serial peripheral status register while SPIF is set and followed by a write to or a read of the serial peripheral data register. While SPIF is set, all writes to the serial peripheral data register are inhibited until the proper clearing sequence is followed. This occurs in the master device. In the slave device, SPIF can be cleared (using a similar sequence) during a second transmission, however, it must be cleared before the second SPIF in order to prevent an overrun condition The SPIF bit is cleared by reset

B6, WCOL The function of the write collision status bit is to notify the user that an attempt was made to write the serial peripheral data register while a data transfer was taking place with an external device The transfer continues uninterrupted; therefore, a write will be unsuccessful. A "read collision" will never occur since the received data byte is placed in a buffer in which access is always synchronous with the MCU operation. If a "write collision" occurs, WCOL is set but no SPI interrupt is generated. The WCOL bit is a status flag only.

Clearing the WCOL bit is accomplished by a software sequence of accessing the serial peripheral status register while WCOL is set, followed by 1) a read of the serial peripheral data register prior to the SPIF bit being set, or 2) a read or write of the serial peripheral data register after the SPIF bit is set. A write to the serial peripheral data register (SPDR) prior to the SPIF bit being set, will result in generation of another WCOL status flag. Both the SPIF and WCOL bits will be cleared in the same sequence. If a second transfer has started while trying to clear (the previously set) SPIF and WCOL bits with a clearing sequence containing a write to the serial peripheral data register, only the SPIF bit will be cleared.

A collision of a write to the serial peripheral data register while an external data transfer is taking place can occur in both the master mode and the slave mode, although with the proper programming the master device should have sufficient information to preclude this collision.

Collision in the master device is defined as a write of the serial peripheral data register while the internal rate clock (SCK) is in the process of transfer. The signal on the SS pin is always high on the master device.

A collision in a slave device is defined in two separate modes. One problem arises in a slave device when the CPHA control bit is a logic zero. When CPHA is a logic zero, data is latched with the occurrence of the first clock transition. The slave device does not have any way of knowing when that transition will occur; therefore, the slave device collision occurs when it attempts to write the serial peripheral data register after its $\overline{SS}$ pin has been pulled low. The $\overline{SS}$ pin of the slave device freezes the data in its serial peripheral data register and does not allow it to be altered if the CPHA bit is a logic zero. The master device must raise the $\overline{SS}$ pin of the slave device high between each byte it transfers to the slave device

The second collision mode is defined for the state of CPHA control bit being a logic one. With the CPHA bit set, the slave device will be receiving a clock (SCK) edge prior to the latch of the first data transfer. This first clock edge will freeze the data in the slave device I/O register and allow the MSB onto the external MISO pin of the slave device. The $\overline{SS}$ pin low state enables the slave device but the drive onto the MISO pin does not take place until the first data transfer clock edge. The WCOL bit will only be set if the I/O register is accessed while a transfer is taking place. By definition of the second collision mode, a master device might hold a slave device $\overline{SS}$ pin low during a transfer of several bytes of data without a problem.

A special case of WCOL occurs in the slave device. This happens when the master device starts a transfer sequence (an edge of SCK for CPHA=1; or an active $\overline{SS}$ transition for CPHA=0) at the same time the slave device CPU is writing to its serial peripheral interface data register. In this case it is assumed that the data byte written (in the slave device serial peripheral interface) is lost and the contents of the slave device read buffer become the byte that is transferred. Because the master device receives back the last byte transmitted, the master device can detect that a fatal WCOL occurred.

Because the slave device is operating asynchronously with the master device, the WCOL bit may be used as an indicator of a collision occurrence. This helps alleviate the user from a strict real-time programming effort The WCOL bit is cleared by reset.

Bit 4 MODF The function of the mode fault flag (MODF) is defined for the master mode device. If the device is a slave device, the MODF bit will be prevented from toggling from a logic zero to a logic one; however, this does not prevent the device from being in the slave mode with the MODF bit set The MODF bit is normally a logic zero and is set only when the master device has its $\overline{SS}$ pin pulled low. Toggling the MODF bit to a logic one affects the internal serial peripheral interface (SPI) system in the following ways.

1. MODF is set and SPI interrupt is generated if SPIE=1
2. The SPE bit is forced to a logic zero This blocks all output drive from the device, disabled the SPI system.
3. The MSTR bit is forced to a logic zero, thus forcing the device into the slave mode.

Clearing the MODF is accomplished by a software sequence of accessing the serial peripheral status register while MODF is set followed by a write to the serial peripheral control register. Control bits SPE and MSTR may be restored to their original set state during this clearing sequence or after the MODF bit has been cleared. Hardware does not allow the user to set the SPE and MSTR bit while MODF is a logic one unless it is during the proper clearing sequence. The MODF flag bit indicates that there might have been a multi-master conflict for system control and allows a proper exit from system operation to a reset or default system state. The MODF bit is cleared by reset.

Serial Peripheral Data I/O Register (SPDR)

7	6	5	4	3	2	1	0
Serial Peripheral Data I/O Register							

The serial peripheral data I/O register is used to transmit and receive data on the serial bus. Only a write to this register will initiate transmission/reception of another byte and this will only occur in the master device. A slave device writing to its data I/O register will not initiate a transmission. At the completion of transmitting a byte of data, the SPIF status bit is set in both the master and slave devices. A write or read of the serial peripheral data I/O register, after accessing the serial peripheral status register with SPIF set, will clear SPIF.

During the clock cycle that the SPIF bit is being set, a copy of the received data byte in the shift register is being moved to a buffer. When the user reads the serial peripheral data I/O register, the buffer is actually being read. During an overrun condition, when the master device has sent several bytes of data and the slave device has not internally responded to clear the first SPIF, only the first byte is contained in the receive buffer of the slave device; all others are lost The user may read the buffer at any time The first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated or an overrun condition will exist.

A write to the serial peripheral data I/O register is not buffered and places data directly into the shift register for transmission

The ability to access the serial peripheral data I/O register is limited when a transmission is taking place. It is important to read the discussion defining the WCOL and SPIF status bits to understand the limits on using the serial peripheral data I/O register.

Serial Peripheral Interface (SPI) System Considerations

There are two types of SPI systems: single master system and multi-master systems. **Figure 20** illustrates both of these systems and a discussion of each is provided below.

Figure 20 a illustrates how a typical single master system may be configured, using a CDP6805 CMOS Family device as the master and four CDP6805 CMOS Family devices as slaves As shown, the MOSI, MISO, and SCK pins are all wired to equivalent pins on each of the five devices. The master device generates the SCK clock, the slave devices all receive it. Because the CDP6805 CMOS master device is the bus master, it internally controls the function of its MOSI and MISO lines, thus writing data to the slave devices on the MOSI and reading data from the slave devices on the MISO lines. The master device selects the individual slave devices by using four pins of a parallel port to control the four $\overline{SS}$ pins of the slave devices. A slave device is selected when the master device pulls its $\overline{SS}$ pin low. The $\overline{SS}$ pins are pulled high during reset because the master device ports will be forced to be inputs at that time, thus disabling the slave devices. Notice that the slave devices do not have to be enabled in a mutually exclusive fashion except to prevent bus contention on the MISO line. For example, three slave devices enabled for a transfer are permissible if only one has the capability of being read by the master. An example of this is a write to several display drivers to clear a display with a single I/O operation. To ensure that proper data transmission is occurring between the master device and a slave device, the master device may have the slave device respond with a previously received data byte (this data byte could be inverted or at least be a byte that is different from the last one sent by the master device). The master device will always receive the previous byte back from the slave device if all MISO and MOSI lines are connected and the slave has not written to its data I/O register. Other transmission security methods might be defined using ports for handshake lines or data bytes with command fields.

A multi-master system may also be configured by the user. A system of this type is shown in **Figure 20b**. An exchange of master control could be implemented by an exchange of code messages through the serial peripheral interface system. The major device control that plays a part in this system is the MSTR bit in the serial peripheral control register and the MODF bit in the serial peripheral status register. Note that the DWOM bit would also be set to prevent bus contention. For additional information on this configuration and SPI in general, refer to RCA Application Note ICAN 7264 entitled "Versatile Serial Protocol for a Microcomputer-Peripheral Interface."

Effects of Stop and Wait Modes on the Timer and Serial System

The STOP and WAIT instructions have different effects on the programmable timer and serial peripheral interface (SPI) system These different effects are discussed separately below

Stop Mode

When the processor executes the STOP instruction, the internal oscillator is turned off This halts all internal CPU processing and the serial peripheral interface The programmable timer will only continue to count if an external timer oscillator is used. The only way for the MCU to "wake up" from the stop mode is by receipt of an external interrupt (logic low on $\overline{\text{IRQ}}$ pin), an external timer oscillator interrupt, a Port B interrupt or by the detection of a reset (logic low on $\overline{\text{RESET}}$ pin or a power-on reset). The effects of the stop mode on each of the MCU systems (Timer and SPI) are described separately.

Timer During Stop Mode

When the MCU enters the STOP mode, the timer will continue to count and generate interrupts if using an external timer oscillator. If using the CPU clock to clock the timer, the timer counter stops counting (the internal processor clock is stopped) and remains at that particular count value until the stop mode is exited by an interrupt (if exited by reset the counter is forced to $FFFC). If the stop mode is exited by an external low on the $\overline{\text{IRQ}}$ pin, then the counter resumes from its stopped value as if nothing had happened. Another feature of the programmable timer, in the stop mode, is that if at least one valid input capture edge occurs at the TCAP pin, the input capture detect circuitry is armed This action does not set any timer flags or "wake up" the MCU, but when the MCU does "wake up" there will be an active input capture flag (and data) from that first valid edge which occurred during the stop mode If the stop mode is exited by an external reset (logic low on $\overline{\text{RESET}}$ pin), then no such input capture flag or data action takes place even if there was a valid input capture edge (at the TCAP pin) during the MCU stop mode

SPI During Stop Mode

When the MCU enters the stop mode, the baud rate generator which drives the SPI shuts down. This essentially stops all master mode SPI operation, thus the master SPI is unable to transmit or receive any data If the STOP instruction is executed during an SPI transfer, that transfer is halted until the MCU exits the stop mode (provided it is an exit resulting from a logic low on the $\overline{\text{IRQ}}$ pin) If the stop mode is exited by a reset, then the appropriate control/status bits are cleared and the SPI is disabled If the device is in the slave mode when the STOP instruction is executed, the slave SPI will still operate. It can still accept data and clock information in addition to transmitting its own data back to a master device.

At the end of a possible transmission with a slave SPI in the STOP mode, no flags are set until a logic low $\overline{\text{IRQ}}$ input results in an MCU "wake up". Caution should be observed when operating the SPI (as a slave) during the stop mode because none of the protection circuitry (write collision, mode fault, etc.) is active.

It should also be noted that when the MCU enters the stop mode all enabled output drivers (TDO, TCMP, MISO, MOSI, and SCK ports) remain active and any sourcing currents from these outputs will be part of the total supply current required by the device

Wait Mode

When the MCU enters the wait mode, the CPU clock is halted All CPU action is suspended; however, the timer and SPI systems remain active. In fact an interrupt from the timer or SPI (in addition to a logic low on the $\overline{\text{IRQ}}$ or $\overline{\text{RESET}}$ pins or a Port B interrupt, if enabled) causes the processor to exit the wait mode. Since the three systems mentioned above operate as they do in the normal mode, only a general discussion of the wait mode is provided below.

The wait mode power consumption depends on how many systems are active. The power consumption will be highest when all the systems (timer, TCMP and SPI) are active. The power consumption will be the least when the SPI system is disabled (timer operation cannot be disabled in the wait mode). If a non-reset exit from the wait mode is performed (i.e., timer overflow interrupt exit), the state of the remaining systems will be unchanged. If a reset exit from the wait mode is performed all the systems revert to the disabled reset state.

Instruction Set

The MCU has a set of 62 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

All of the instructions used in the CDP6805 CMOS Family are used in the CDP68HC05D2 MCU, plus an additional one; the multiply (MUL) instruction. This instruction allows for unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high order product is then stored in the index register and the low order product is stored in the accumulator. A detailed definition of the MUL instruction is shown below.

Operation: X A ← X*A

Description: Multiplies the eight bits in the index register by the eight bits in the accumulator to obtain a 16-bit unsigned number in the concatenated accumulator and index register.

Condition Codes:
H: Cleared
I: Not affected
N: Not affected
Z: Not affected
C: Cleared

Source Form(s): MUL

Addressing Mode	Cycles	Bytes	Opcode
Inherent	11	1	$42

Register/Memory Instructions

Most of these instructions use two operands. The first operand is either the accumulator or the index register. The second operand is obtained from memory using one of the addressing modes. The operand for the jump unconditional (JMP) and jump to subroutine (JSR) instructions is the program counter Refer to Table VI.

Ready-Modify-Write Instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read/modify/write sequence since it does not modify the value. Refer to Table VII.

Table VI — Register/Memory Instructions

		Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
Function	Mnem	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from Memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in Memory	STA	—	—	—	B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in Memory	STX	—	—	—	BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add Memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add Memory and Carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract Memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND Memory to A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR Memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR Memory with A	EOR	AB	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump Unconditional	JMP	—	—	—	BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to Subroutine	JSR	—	—	—	BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

Table VII — Read-Modify-Write Instructions

		Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (2's Complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate Left Thru Carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate Right Thru Carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical Shift Left	LSL	48	1	3	58	1	3	38	2	5	78		5	68	2	6
Logical Shift Right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic Shift Right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for Negative or Zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5
Multiply	MUL	42	1	11	—	—	—	—	—	—	—	—	—	—	—	—

Branch Instructions

Most branch instructions test the state of the condition code register and, if certain criteria are met, a branch is executed. This adds an offset between -127 and +128 to the current program counter. Refer to Table VIII.

Table VIII — Branch Instructions

		Relative Addressing Mode		
Function	**Mnemonic**	**Op Code**	**# Bytes**	**# Cycles**
Branch Always	BRA	20	2	3
Branch Never	BRN	21	2	3
Branch IFF Higher	BHI	22	2	3
Branch IFF Lower or Same	BLS	23	2	3
Branch IFF Carry Clear	BCC	24	2	3
(Branch IFF Higher or Same)	(BHS)	24	2	3
Branch IFF Carry Set	BCS	25	2	3
(Branch IFF Lower)	(BLO)	25	2	3
Branch IFF Not Equal	BNE	26	2	3
Branch IFF Equal	BEQ	27	2	3
Branch IFF Half Carry Clear	BHCC	28	2	3
Branch IFF Half Carry Set	BHCS	29	2	3
Branch IFF Plus	BPL	2A	2	3
Branch IFF Minus	BMI	2B	2	3
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	3
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	3
Branch IFF Interrupt Line is Low	BIL	2E	2	3
Branch IFF Interrupt Line is High	BIH	2F	2	3
Branch to Subroutine	BSR	AD	2	6

Bit Manipulation Instructions

The MCU is capable of setting or clearing any bit which resides in the first 256 bytes of the memory space except for ROM, port D data location ($03) bits 0, 1, 6, 7, serial peripheral status register ($0B), timer status register ($13), and timer input capture register ($14, $15). All port registers, DDRs, timer, serial system, on-chip RAM, and 128 bytes of ROM reside in the first 256 bytes (pages zero). An additional feature allows the software to test and branch on the state of any bit within the first 256 locations. The bit set, bit clear, and bit test and branch functions are all implemented with a single instruction. For the test and branch instructions, the value of the bit tested is automatically placed in the carry bit of the condition code register. Refer to Table IX.

Table XI — Bit Manipulation Instructions

		Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
Function	**Mnemonic**	**Op Code**	**# Bytes**	**# Cycles**	**Op Code**	**# Bytes**	**# Cycles**
Branch IFF Bit n is Set	BRSET n (n=0...7)	—	—	—	2•n	3	5
Branch IFF Bit n is Clear	BRCLR n (n=0...7)	—	—	—	01 + 2•n	3	5
Set Bit n	BSET n (n=0...7)	10 + 2•n	2	5	—	—	—
Clear Bit n	BCLR n (n=0...7)	11 + 2•n	2	5	—	—	—

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Control Instructions

These instructions are register reference instructions and are used to control processor operation during a program execution. Refer to Table X.

Table X — Control Instructions

		Inherent		
Function	Mnemonic	Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	10
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

Alphabetical Listing

The complete instruction set is given in alphabetical order in Table XI.

Opcode Map

Table XII is an opcode map for the instructions used on the MCU.

Addressing Modes

The MCU uses ten different addressing modes to provide the programmer with an opportunity to optimize the code to all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables, and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions, while the longest instructions (three bytes) permit accessing tables throughout memory. Short absolute (direct) and long absolute (extended) addressing are also included. One and two byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory. Table XII shows the addressing modes for each instruction, with the effects each instruction has on the condition code register.

The term "effective address" (EA) is used in describing the various addressing modes, and is defined as the byte address to or from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate "contents of" the location or register referred to; e.g., (PC) indicates the contents of the location pointed to by the PC. An arrow indicates "is replaced by", and a colon indicates concatenation of two bytes.

Table XI — Instruction Set

	Addressing Modes										Condition Codes				
Mnemonic	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/ Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			A	●	A	A	A
ADD		X	X	X		X	X	X			A	●	A	A	A
AND		X	X	X		X	X	X			●	●	A	A	●
ASL	X		X			X	X				●	●	A	A	A
ASR	X		X			X	X				●	●	A	A	A
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	A	A	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	A
BRSET										X	●	●	●	●	A
BSET									X		●	●	●	●	●
BSR					X						●	●	●	●	●
CLC	X										●	●	●	●	0
CLI	X										●	0	●	●	●
CLR	X		X			X	X				●	●	0	1	●
CMP		X	X	X		X	X	X			●	●	A	A	A
COM	X		X			X	X				●	●	A	A	1
CPX		X	X	X		X	X	X			●	●	A	A	A
DEC	X		X			X	X				●	●	A	A	●
EOR		X	X	X		X	X	X			●	●	A	A	●
INC	X		X			X	X				●	●	A	A	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	A	A	●
LDX		X	X	X		X	X	X			●	●	A	A	●
LSL	X		X			X	X				●	●	A	A	A
LSR	X		X			X	X				●	●	0	A	A
MUL	X										0	●	●	●	0
NEG	X		X			X	X				●	●	A	A	A
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	A	A	●
ROL	X		X			X	X				●	●	A	A	A
ROR	X		X			X	X				●	●	A	A	A
RSP	X										●	●	●	●	●
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	A	A	A
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	A	A	●
STOP	X										●	0	●	●	●
STX			X	X		X	X	X			●	●	A	A	●
SUB		X	X	X		X	X	X			●	●	A	A	A
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	A	A	●
TXA	X										●	●	●	●	●
WAIT	X										●	0	●	●	●

Condition Code Symbols:

H	Half Carry (From Bit 3)	Z	Zero	●	Not Affected	0	Cleared
I	Interrupt Mask	C	Carry/Borrow	?	Load CC Register From Stack	1	Set
N	Negate (Sign Bit)	A	Test and Set if True Cleared Otherwise				

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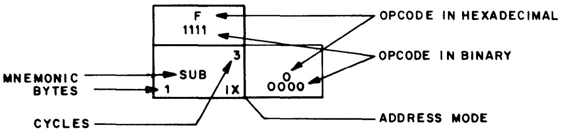
Table XII — CDP68HC05D2 HCMOS Instruction Set Opcode Map

	Bit Manipulation		Branch	Read/Modify/Write					Control		Register/Memory						
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
Hi Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Hi Low
0 0000	5 BRSET0 3 BTB	5 BSET0 2 BSC	3 BRA 2 REL	5 NEG 2 DIR	3 NEG 1 INH	3 NEG 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RT1 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0 0000
1 0001	5 BRCLR0 3 BTB	5 BCLR0 2 BSC	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1 0001
2 0010	5 BRSET1 3 BTB	5 BSET1 2 BSC	3 BHI 2 REL		11 MUL 1 INH						2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2 0010
3 0011	5 BRCLR1 3 BTB	5 BCLR1 2 BSC	3 BLS 2 REL	5 COM 3 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3 0011
4 0100	5 BRSET2 3 BTB	5 BSET2 2 BSC	3 BCC 2 REL	5 LSR 2 DTR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4 0100
5 0101	5 BRCLR2 3 BTB	5 BCLR2 2 BSC	3 BCS 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5 0101
6 0110	5 BRSET3 3 BTB	5 BSET3 2 BSC	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6 0110
7 0111	5 BRCLR3 3 BTB	5 BCLR3 2 BSC	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7 0111
8 1000	5 BRSET4 3 BTB	5 BSET4 2 BSC	3 BHCC 2 REL	5 LSL 2 DIR	3 LSLA 1 INH	3 LSLX 1 INH	6 LSL 2 IX1	5 LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8 1000
9 1001	5 BRCLR4 3 BTB	5 BCLR4 2 BSC	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9 1001
A 1010	5 BRSET5 3 BTB	5 BSET5 2 BSC	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A 1010
B 1011	5 BRCLR5 3 BTB	5 BCLR5 2 BSC	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B 1011
C 1100	5 BRSET6 3 BTB	5 BSET6 2 BSC	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	5 INCX 1 INH	5 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C 1100
D 1101	5 BRCLR6 3 BTB	5 BCLR6 2 BSC	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D 1101
E 1110	5 BRSET7 3 BTB	5 BSET7 2 BSC	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E 1110
F 1111	5 BRCLR7 3 BTB	5 BCLR7 2 BSC	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F 1111

Abbreviations for Address Modes

INH	Inherent	REL	Relative
A	Accumulator	BSC	Bit Set/Clear
X	Index Register	BTB	Bit Test and Branch
IMM	Immediate	IX	Indexed (No Offset)
DIR	Direct	IX1	Indexed 1 Byte (8-Bit) Offset
EXT	Extended	IX2	Indexed 2 Byte (16-Bit) Offset

LEGEND



Inherent

In inherent instructions, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, and no other arguments, are included in this mode.

Immediate

In immediate addressing, the operand is contained in the byte immediately following the opcode Immediate addressing is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

$$EA = PC + 1; PC \leftarrow PC + 2$$

Direct

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two byte instruction. This includes all on-chip RAM and I/O registers, and 128 bytes of on-chip ROM. Direct addressing is efficient in both memory and time

$$EA = (PC + 1); PC \leftarrow PC + 2$$

Address Bus High ← 0; Address Bus Low ← (PC+1)

Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing modes are capable of referencing arguments anywhere in memory with a single three-byte instruction.

$$EA = (PC + 1):(PC + 2); PC \leftarrow PC + 3$$

Address Bus High ← (PC + 1); Address Bus Low ← (PC+2)

Indexed, No Offset

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is used to move a pointer through a table or to address a frequently referenced RAM or I/O location.

$$EA = X; PC \leftarrow PC + 1$$

Address Bus High ← 0; Address Bus Low ← X

Indexed, 8-Bit Offset

Here the EA is obtained by adding the contents of the byte following the opcode to that of the index register; therefore, the operand is located anywhere within the lowest 511 memory locations. For example, this mode of addressing is useful for selecting the mth element in a n element table. All instructions are two bytes. The content of the index register (X) is not changed. The content of (PC+1) is an unsigned 8-bit integer. One byte offset indexing permits look-up tables to be easily accessed in either RAM or ROM.

$$EA = X + (PC + 1);\ PC \leftarrow PC + 2$$

$$\text{Address Bus High} \leftarrow K;\ \text{Address Bus Low} \leftarrow X + (PC + 1)$$

where;

K = The carry from the addition of $X + (PC + 1)$

Indexed, 16-Bit Offset

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed 8-bit offset, except that this three byte instruction allows tables to be anywhere in memory (e.g., jump tables in ROM). The content of the index register is not changed

$$EA = X + [(PC + 1):(PC + 2))];\ PC \leftarrow PC + 3$$

$$\text{Address Bus High} \leftarrow (PC + 1) + K;$$

$$\text{Address Bus Low} \leftarrow X + (PC + 2)$$

where:

K = The carry from the addition of $X + (PC + 2)$

Relative

Relative addressing is used only in branch instructions. In relative addressing, the content of the 8-bit signed byte following the opcode (the offset) is added to the PC if and only if the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is limited to the range of -126 to +129 bytes from the branch instruction opcode location.

$$EA = PC + 2 + (PC + 1);\ PC \leftarrow EA \text{ if branch taken;}$$

$$\text{otherwise, } EA = PC \leftarrow PC + 2$$

Bit Set/Clear

Direct addressing and bit addressing are combined in instructions which set and clear individual memory and I/O bits. In the bit set and clear instructions, the byte is specified as a direct address in the location following the opcode. The first 256 addressable locations are thus accessed The bit to be modified within that byte is specified in the first three bits of the opcode. The bit set and clear instructions occupy two bytes, one for the opcode (including the bit number) and the other to address the byte which contains the bit of interest.

$$EA = (PC + 1);\ PC \leftarrow PC + 2$$

$$\text{Address Bus High} \leftarrow 0;\ \text{Address Bus Low} \leftarrow (PC + 1)$$

Bit Test and Branch

Bit test and branch is a combination of direct addressing, bit set/clear addressing, and relative addressing. The actual bit to be tested, within the byte, is specified within the low order nibble of the opcode. The address of the data byte to be tested is located via a direct address in the location following the opcode byte (EA1). The signed relative 8-bit offset is in the third byte (EA2) and is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any bit in the first 256 locations of memory.

$$EA1 = (PC + 1)$$

$$\text{Address Bus High} \leftarrow 0;\ \text{Address Bus Low} \leftarrow (PC + 1)$$

$$EA2 = PC + 3 + (PC + 2),\ PC \leftarrow EA2 \text{ if branch taken;}$$

$$\text{otherwise, } PC \leftarrow PC + 3$$

Device Characteristics

MAXIMUM RATINGS *(Voltages Referenced to V_{SS})*

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{in}	V_{SS} -0.5 to V_{DD} +0.5	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	I	25	mA
Operating Temperature Range	T_A	-40 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance Ceramic Plastic Plastic Chip Carrier	θJA	50 100 70	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

V_{DD} = 4.5 V

Pins	R1	R2	C
PA0-PA7, PB0-PB7, PC0-PC7, PD6	3.26 kΩ	2.38 kΩ	50 pF
PD1-PD4	1.9 kΩ	2.26 kΩ	200 pF

V_{DD} = 3.0 V

Pins	R1	R2	C
PA0-PA7, PB0-PB7, PC0-PC7, PD6	10.91 kΩ	6.32 kΩ	50 pF
PD1-PD4	6 kΩ	6 kΩ	200 pF

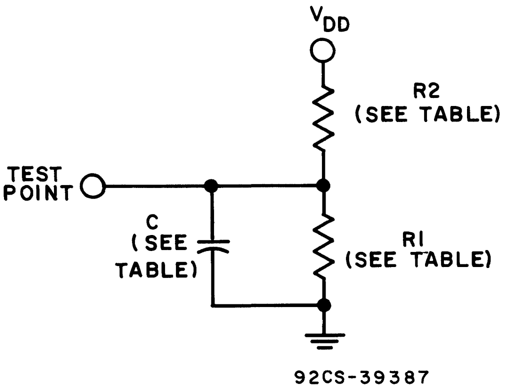


Fig. 24 - Equivalent Test Load

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K + (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS *(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = -40°C to +125°C unless otherwise noted)*

Characteristic	Symbol	Limits			Unit
		Min	Typ	Max	
Output Voltage, $I_{LOAD} \leq 10.0\ \mu A$	V_{OL} V_{OH}	— V_{DD}-0.1	— —	0.1 —	V V
Output High Voltage (I_{Load} = 0.8 mA) PA0-PA7, PB0-PB7, PC0-PC7, TCMP (I_{Load} = 1.6 mA) PD1-PD4	 V_{OH} V_{OH}	 V_{DD}-0.8 V_{DD}-0.8	 — —	 — —	 V V
Output Low Voltage (I_{Load} = 1.6 mA) PA0-PA7, PB0-PB7, PC0-PC7, PD2-PD5, TCMP	 V_{OL}	 —	 —	 0.4	 V
Input High Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PD7, TCAP, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, OSC1	 V_{IH}	 0.7 x V_{DD}	 —	 V_{DD}	 V
Input Low Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PD7, TCAP, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, OSC1	 V_{IL}	 V_{SS}	 —	 0.2 x V_{DD}	 V
Total Supply Current (C_L = 50 pF on Ports, no dc Loads, t_{cyc} = 500 ns, (V_{IL} = 0.2 V, V_{IH} = V_{DD} - 0.2V) No external timer oscillator RUN WAIT (See Note) STOP (See Note)	 I_{DD} I_{DD} I_{DD}	 — — —	 4 1.5 1.0	 TBD TBD TBD	 mA mA µA
Total Supply Current (C_L = 50 pF on Ports, no dc Loads, t_{cyc} = 500 ns, (V_{IL} = 0.2 V, V_{IN} = V_{DD} - 0.2V) 32.768 KHz external timer crystal oscillator for circuit as shown in Fig. 13(c). RUN WAIT (See Note) STOP (See Note)	 I_{DD} I_{DD} I_{DD}	 — — —	 4.5 2.0 500	 TBD TBD TBD	 mA mA µA
I/O Ports Hi-Z Leakage Current PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD5	 I_{IL}	 —	 —	 ±10	 µA
Input Current $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, TCAP, OSC1, PD0, PD7	 I_{in}	 —	 —	 ±1	 µA
Capacitance Ports (as input or output) $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, TCAP, OSC1, PD0-PD5, PD7	 C_{out} C_{in}	 — —	 — —	 12 8	 pF pF

NOTE: Measured under the following conditions:

1. All ports are configured as input, V_{IL} = 0.2 V, V_{IH} = V_{DD} - 0.2 V.
2. No load on TCMP, C_L = 20 pF on OSC2
3. OSC1 is a square wave with V_{IL} = 0.2 V, V_{IH} = V_{DD} - 0.2 V
4. SPE = 0

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DC ELECTRICAL CHARACTERISTICS *(V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = -40°C to +125°C unless otherwise noted)*

Characteristic	Symbol	Limits			Unit
		Min	Typ	Max	
Output Voltage, $I_{LOAD} \leq 10.0\ \mu A$	V_{OL} V_{OH}	— V_{DD}-0.1	— —	0.1 —	V V
Output High Voltage (I_{Load} = 0.2 mA) PA0-PA7, PB0-PB7, PC0-PC7, TCMP, PD5 (I_{Load} = 0.4 mA) PD1-PD4	 V_{OH} V_{OH}	 V_{DD}-0.3 V_{DD}-0.3	 — —	 — —	 V V
Output Low Voltage (I_{Load} = 0.4 mA) PA0-PA7, PB0-PB7, PC0-PC7, PD2-PD5, TCMP	V_{OL}	—	—	0.3	V
Input High Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PD7, TCAP, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, OSC1	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input Low Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PD7, TCAP, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, OSC1	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
Total Supply Current (C_L = 50 pF on Ports, no dc Loads, t_{cyc} = 1000 ns, (V_{IL} = 0.2 V, V_{IH} = V_{DD} - 0.2V) No external timer oscillator RUN WAIT (See Note) STOP (See Note)	 I_{DD} I_{DD} I_{DD}	 — — —	 1.4 500 1	 TBD TBD TBD	 mA μA μA
Total Supply Current (C_L = 50 pF on Ports, no dc Loads, t_{cyc} = 1000 ns, (V_{IL} = 0.2 V, V_{IH} = V_{DD} - 0.2V) 32 768 KHz external timer crystal oscillator circuit as shown in **Fig. 13(c)**. RUN WAIT (See Note) STOP (See Note)	 I_{DD} I_{DD} I_{DD}	 — — —	 1.5 600 100	 TBD TBD TBD	 mA μA μA
I/O Ports Hi-Z Leakage Current PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD5	I_{IL}	—	—	±10	μA
Input Current $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, TCAP, OSC1, PD0, PD7	I_{in}	—	—	±1	μA
Capacitance Ports (as input or output) $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, TCAP, OSC1, PD0-PD5, PD7	 C_{out} C_{in}	 — —	 — —	 12 8	 pF pF

NOTE: Measured under the following conditions:

1. All ports are configured as input, V_{IL} = 0.2 V, V_{IH} = V_{DD} - 0.2 V.
2. No load on TCMP, C_L = 20 pF on OSC2.
3. OSC1 is a square wave with V_{IL} = 0.2 V, V_{IH} = V_{DD} - 0.2 V
4. SPE = 0

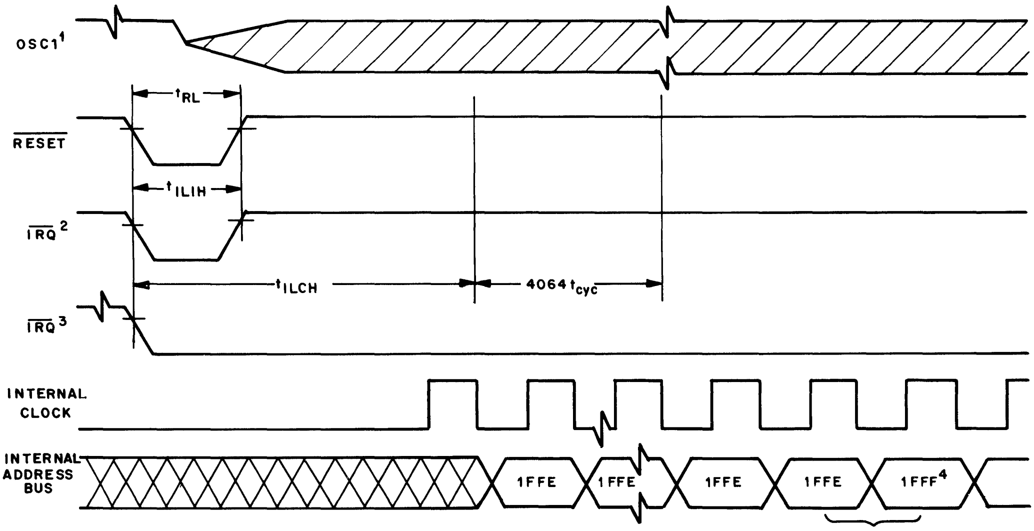
CONTROL TIMING *(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = -40°C to +125°C)*

Characteristic	Symbol	Limits Min	Limits Max	Unit
Frequency of Operation				
Crystal Option	f_{osc}	—	4.2	MHz
External Clock Option	f_{osc}	dc	4 2	MHz
Internal Operating Frequency				
Crystal (f_{osc} ÷ 2)	f_{op}	—	2.1	MHz
External Clock (f_{osc} ÷ 2)	f_{op}	dc	2.1	MHz
Cycle Time **(See Figu [illegible])**	t_{cyc}	480	—	ns
Crystal Oscillator Startup Time **(See Figure 8)**	t_{OXOV}	—	100	ms
Stop Recovery Startup Time (Crystal Oscillator) **(See Figure 25)**	t_{ILCH}	—	100	ms
RESET Pulse Width **(See Figure 9)**	t_{RL}	1.5	—	t_{cyc}
Timer				
Resolution**	t_{RESL}	4.0	—	t_{cyc}
Input Capture Pulse Width **(See Figure 26)**	t_{TH}, t_{TL}	125	—	ns
Input Capture Pulse Period **(See Figure 26)**	t_{TLTL}	***	—	t_{cyc}
Interrupt Pulse Width Low (Edge-Triggered) **(See Figure 11)**	t_{ILIH}	125	—	ns
Interrupt Pulse Period **(See Figure 11)**	t_{ILIL}	*	—	t_{cyc}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	—	ns
External Timer Oscillator frequency of operation	f_{tosc}	—	f_{osc} ÷ 4	f_{osc}

*The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

**Since a 2-bit prescaler in the timer must count four internal cycles (t_{cyc}), this is the limiting minimum factor in determining the timer resolution

***The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}



NOTES:
1. REPRESENTS THE INTERNAL GATING OF THE OSC1 PIN.
2. IRQ PIN EDGE-SENSITIVE MASK OPTION.
3. IRQ PIN LEVEL AND EDGE-SENSITIVE MASK OPTION.
4. RESET VECTOR ADDRESS SHOWN FOR TIMING EXAMPLE.

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Fig. 25 - Stop Recovery Timing Diagram

CONTROL TIMING ($V_{DD} = 3.0$ Vdc ± 10%, $V_{SS} = 0$ Vdc, $T_A = -40°C$ to $+125°C$)

Characteristic	Symbol	Limits		Unit
		Min	Max	
Frequency of Operation				
Crystal Option	f_{osc}	—	2.0	MHz
External Clock Option	f_{osc}	dc	2.0	MHz
Internal Operating Frequency				
Crystal ($f_{osc} \div 2$)	f_{op}	—	1.0	MHz
External Clock ($f_{osc} \div 2$)	f_{op}	dc	1.0	MHz
Cycle Time **(See Figure 8)**	t_{cyc}	1000	—	ns
Crystal Oscillator Startup Time **(See Figure 8)**	t_{OXOV}	—	100	ms
Stop Recovery Startup Time (Crystal Oscillator) **(See Figure 25)**	t_{ILCH}	—	100	ms
RESET Pulse Width - Excluding Power-Up **(See Figure 8)**	t_{RL}	1.5	—	t_{cyc}
Timer				
Resolution**	t_{RESL}	4.0	—	t_{cyc}
Input Capture Pulse Width **(See Figure 26)**	t_{TH}, t_{TL}	250	—	ns
Input Capture Pulse Period **(See Figure 26)**	t_{TLTL}	***	—	t_{cyc}
Interrupt Pulse Width Low (Edge-Triggered) **(See Figure 11)**	t_{ILIH}	250	—	ns
Interrupt Pulse Period **(See Figure 11)**	t_{ILIL}	*	—	t_{cyc}
OSC1 Pulse Width	t_{OH}, t_{OL}	200	—	ns
External timer oscillator frequency of operation	f_{tosc}	—	$f_{osc} \div 4$	f_{osc}

*The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

**Since a 2-bit prescaler in the timer must count four internal cycles (t_{cyc}), this is the limiting minimum factor in determining the timer resolution.

***The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

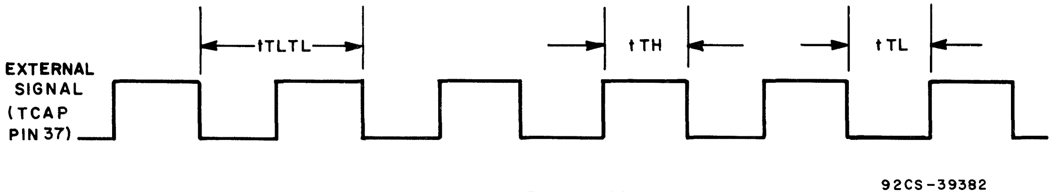

Fig. 26 - Timer Relationships

SERIAL PERIPHERAL INTERFACE (SPI) TIMING (Figure 29)

($V_{DD} = 5.0$ Vdc ± 10%, $V_{SS} = 0$ Vdc, $T_A = -40°C$ to $+125°C$)

Num.	Characteristic	Symbol	Limits		Unit
			Min	Max	
	Operating Frequency				
	Master	$f_{op(m)}$	dc	0.5	f_{op}***
	Slave	$f_{op(s)}$	dc	2.1	MHz
1	Cycle Time				
	Master	$t_{cyc(m)}$	2.0	—	t_{cyc}
	Slave	$t_{cyc(s)}$	480	—	ns
2	Enable Lead Time				
	Master	$t_{lead(m)}$	*	—	
	Slave	$t_{lead(S)}$	240	—	ns
3	Enable Lag Time				
	Master	$t_{lag(m)}$	*	—	
	Slave	$t_{lag(S)}$	240	—	ns
4	Clock (SCK) High Time				
	Master	$t_{w(SCKH)m}$	340	—	ns
	Slave	$t_{w(SCKH)s}$	190	—	ns
5	Clock (SCK) Low Time				
	Master	$t_{w(SCKL)m}$	340	—	ns
	Slave	$t_{w(SCKL)s}$	190	—	ns
6	Data Setup Time (Inputs)				
	Master	$t_{su(m)}$	100	—	ns
	Slave	$t_{su(s)}$	100	—	ns
7	Data Hold Time (Inputs)				
	Master	$t_{h(m)}$	100	—	ns
	Slave	$t_{h(s)}$	100	—	ns
8	Access Time (Time to data active from high impedance state)				
	Slave	t_a	0	120	ns
9	Disable Time (Hold Time to High-Impedance State)				
	Slave	t_{dis}	—	240	ns
10	Data Valid				
	Master (Before Capture Edge)	$t_{v(m)}$	0.25	—	$t_{cyc(m)}$
	Slave (After Enable Edge)**	$t_{v(s)}$	—	240	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{ho(m)}$	0.25	—	$t_{cyc(m)}$
	Slave (After Enable Edge)	$t_{ho(s)}$	0	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, $C_L = 200$ pF)				
	SPI Outputs (SCK, MOSI, MISO)	t_{rm}	—	100	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	t_{rs}	—	2.0	μs
13	Fall Time (70% V_{DD} to 20% V_{DD}, $C_L = 200$ pF)				
	SPI Outputs (SCK, MOSI, MISO)	t_{fm}	—	100	ns
	SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	t_{fs}	—	2.0	μs

*Signal production depends on software

**Assumes 200 pF load on all SPI pins

***Note that the unit this specification uses is f_{op} (internal operating frequency), not MHz! In the master mode the SPI bus is capable of running at one-half of the device's internal operating frequency, therefore 1.05 MHz maximum.

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SERIAL PERIPHERAL INTERFACE (SPI) TIMING (Figure 29)

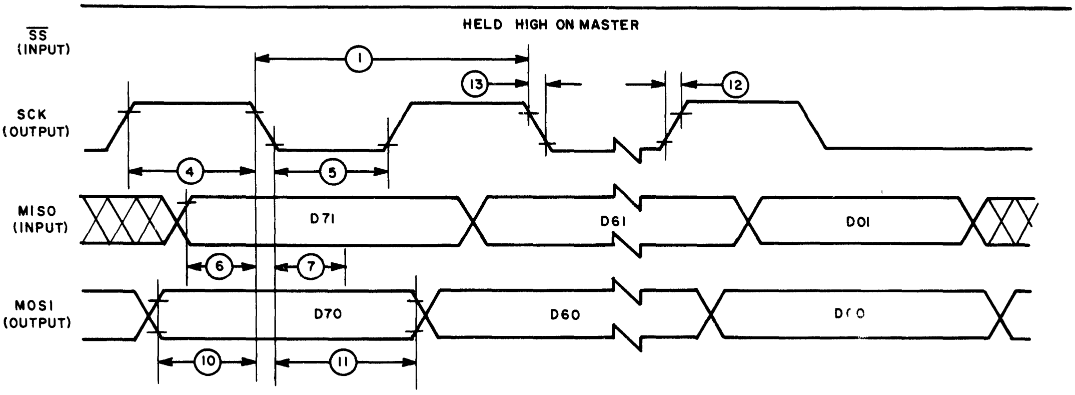
(V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = -40°C to +125°C)

Num.	Characteristic	Symbol	Limits		Unit
			Min	Max	
	Operating Frequency Master Slave	 $f_{op(m)}$ $f_{op(s)}$	 dc dc	 0.5 1.0	 f_{op}*** MHz
1	Cycle Time Master Slave	 $t_{cyc(m)}$ $t_{cyc(s)}$	 2.0 1.0	 — —	 t_{cyc} µs
2	Enable Lead Time Master Slave	 $t_{lead(m)}$ $t_{lead(S)}$	 * 500	 — —	 ns
3	Enable Lag Time Master Slave	 $t_{lag(m)}$ $t_{lag(S)}$	 * 500	 — —	 ns
4	Clock (SCK) High Time Master Slave	 $t_{w(SCKH)m}$ $t_{w(SCKH)s}$	 720 400	 — —	 µs ns
5	Clock (SCK) Low Time Master Slave	 $t_{w(SCKL)m}$ $t_{w(SCKL)s}$	 720 400	 — —	 µs ns
6	Data Setup Time (Inputs) Master Slave	 $t_{su(m)}$ $t_{su(s)}$	 200 200	 — —	 ns ns
7	Data Hold Time (Inputs) Master Slave	 $t_{h(m)}$ $t_{h(s)}$	 200 200	 — —	 ns ns
8	Access Time (Time to data active from high impedance state) Slave	 t_a	 0	 250	 ns
9	Disable Time (Hold Time to High-Impedance State) Slave	 t_{dis}	 —	 500	 ns
10	Data Valid Master (Before Capture Edge) Slave (After Enable Edge)**	 $t_{v(m)}$ $t_{v(s)}$	 0.25 —	 — 500	 $t_{cyc(m)}$ ns
11	Data Hold Time (Outputs) Master (After Capture Edge) Slave (After Enable Edge)	 $t_{ho(m)}$ $t_{ho(s)}$	 0.25 0	 — —	 $t_{cyc(m)}$ ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, MISO) SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	 t_{rm} t_{rs}	 — —	 200 2.0	 ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, MISO) SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	 t_{fm} t_{fs}	 — —	 200 2.0	 ns µs

*Signal production depends on software

**Assumes 200 pF load on all SPI pins.

***Note that the unit this specification uses is f_{op} (internal operating frequency), not MHz! In the master mode the SPI bus is capable of running at one-half of the device's internal operating frequency, therefore 0.5 MHz maximum.



(a) SPI Master Timing CPOL = 0, CPHA = 1

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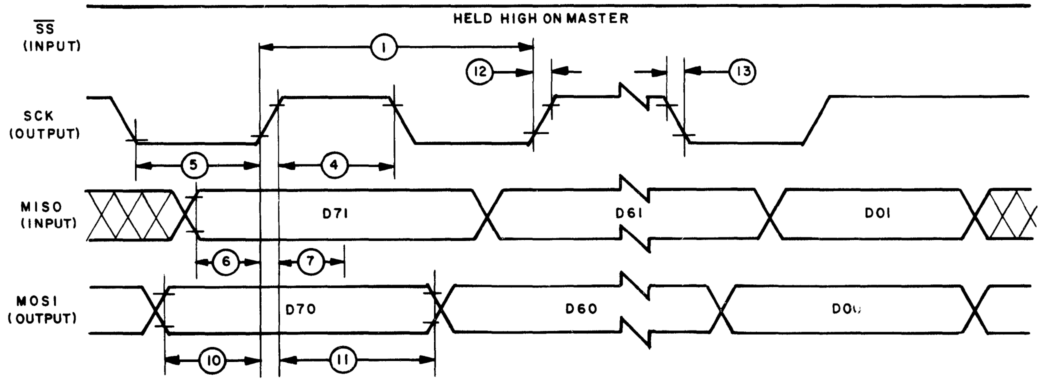

(b) SPI Master Timing CPOL = 1, CPHA = 1

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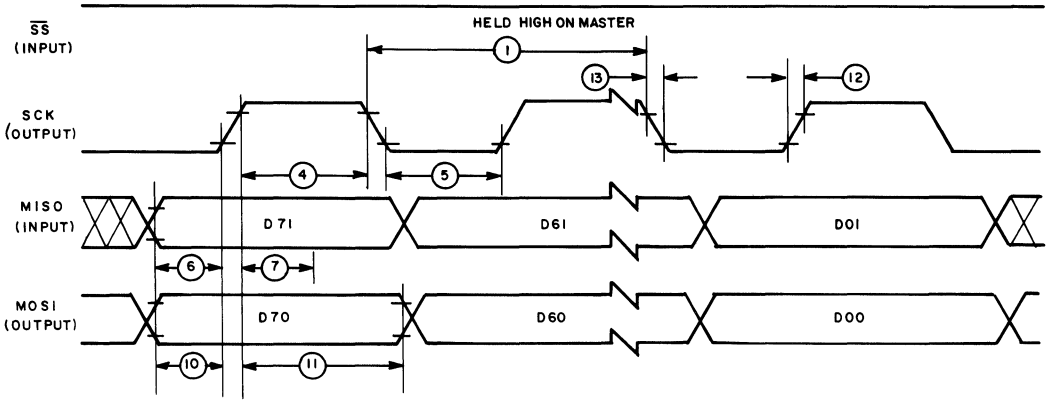
NOTE: MEASUREMENT POINTS ARE V_{OL}, V_{OH}, V_{IL}, V_{IH}

Fig. 27 - Timing Diagrams



(c) SPI Master Timing CPOL = 0, CPHA = 0

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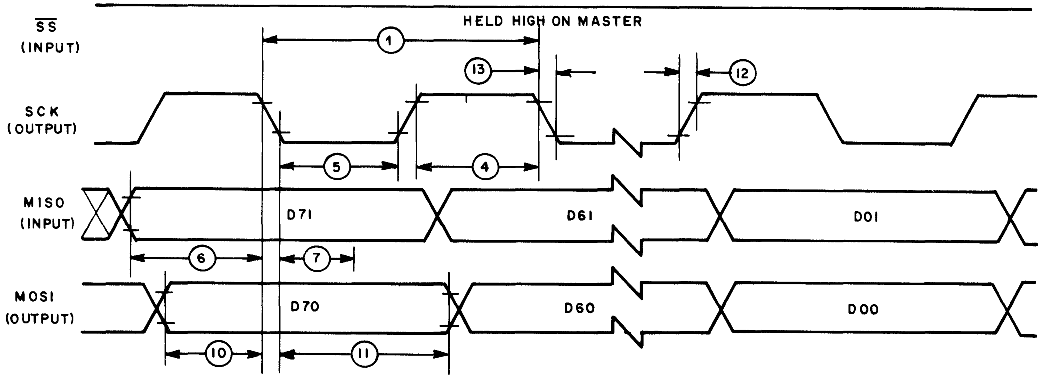

(d) SPI Master Timing CPOL = 1, CPHA = 0

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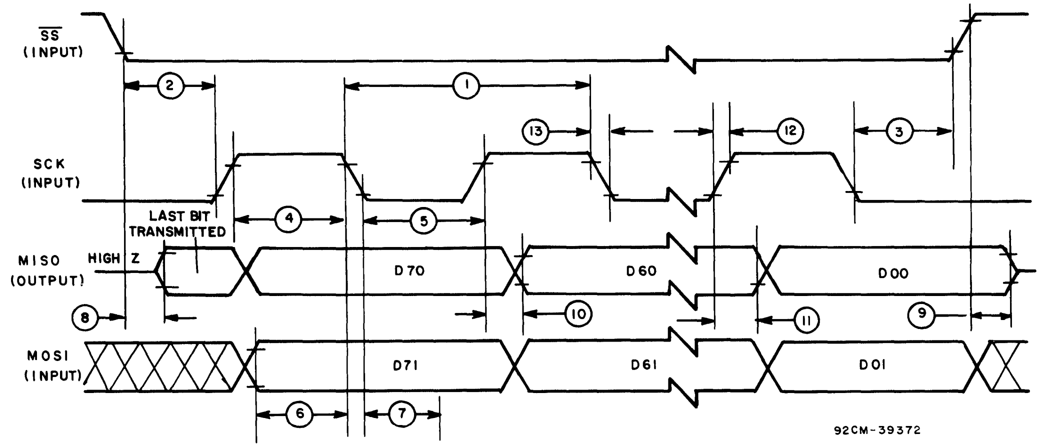
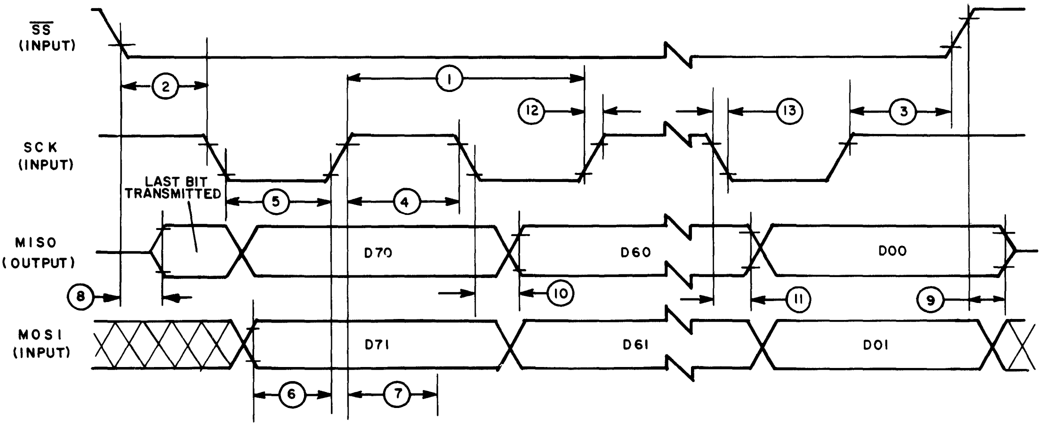
NOTE: MEASUREMENT POINTS ARE V_{OL}, V_{OH}, V_{IL} AND V_{IH}

Fig. 27 - Timing Diagrams (Continued)



(e) SPI Slave Timing CPOL = 0, CPHA = 1



(f) SPI Slave Timing CPOL = 1, CPHA = 1

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NOTE: MEASUREMENT POINTS ARE V_{OL}, V_{OH}, V_{IL}, AND V_{IH}.

Fig. 27 - Timing Diagrams (Continued)

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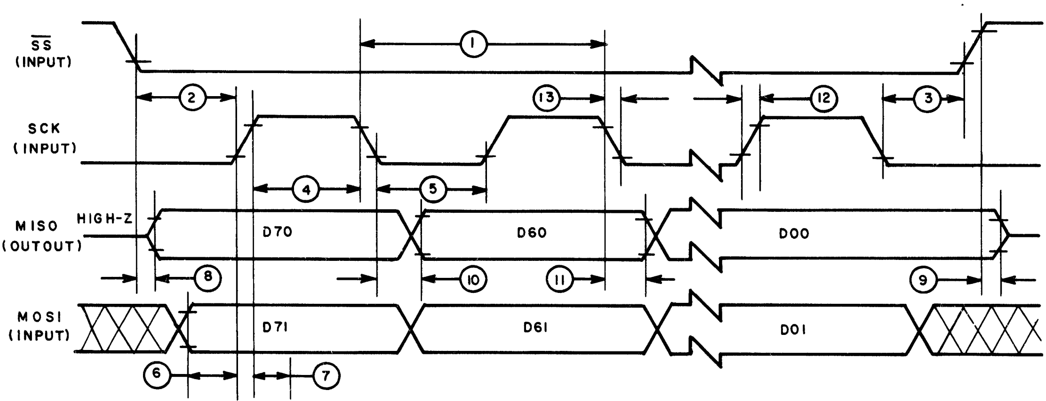
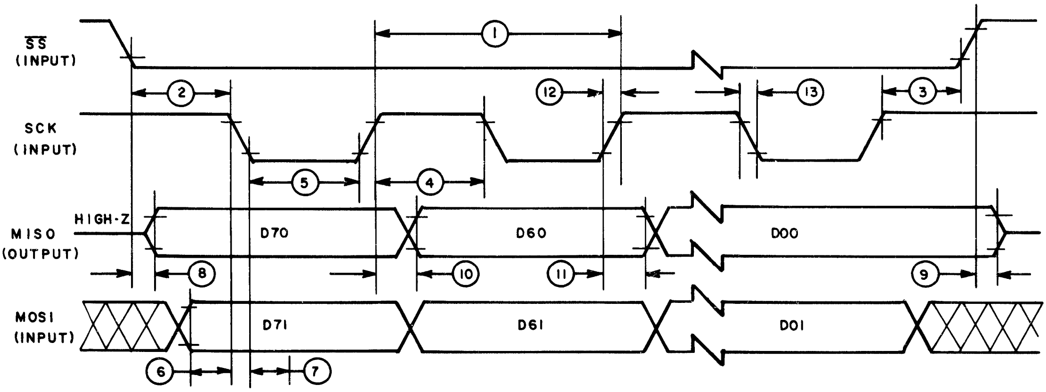


(g) SPI Slave Timing CPOL = 0, CPHA = 0



(h) SPI Slave Timing CPOL = 1, CPHA = 0

NOTE: MEASUREMENT POINTS ARE V_{OL}, V_{OH}, V_{IL} AND V_{IH}

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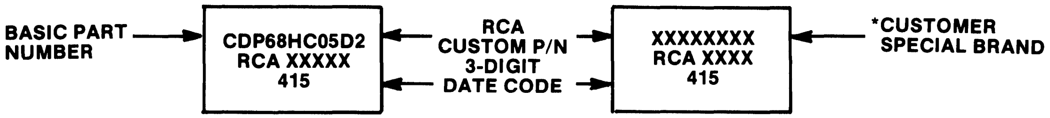
Fig. 27 - Timing Diagrams (Concluded)

Branding:

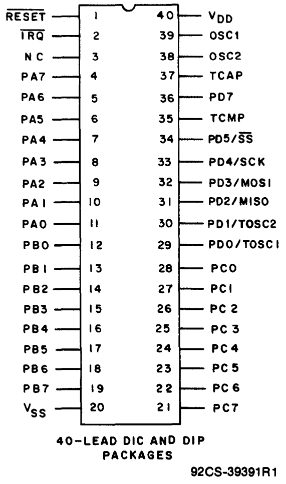
The packages (DIC, DIP, or PCC) in which the RCA custom Microcomputers are supplied are branded with both the basic type number and an RCA custom part number. Please refer to both numbers when discussing a custom Microcomputer order with RCA representatives. RCA can accommodate special requirements of customers. The standard format is as follows:



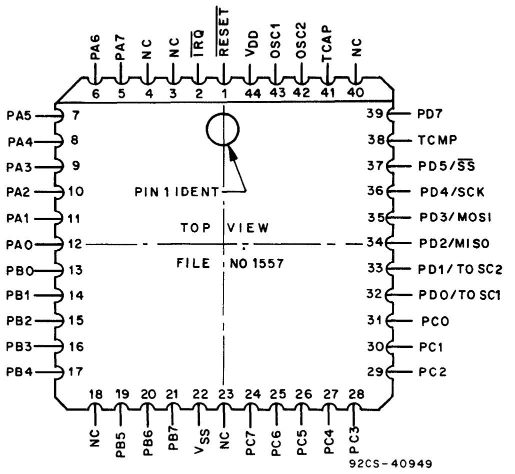
*CUSTOMER SPECIAL BRAND (UP TO 10 CHARACTERS FOR DIC. 13 CHARACTERS FOR DIP).

Mechanical Data

Terminal Assignments



D Suffix - 40-Lead Dual-In-Line Side-Brazed Ceramic Package
E Suffix - 40-Lead Dual-In-Line Plastic Package

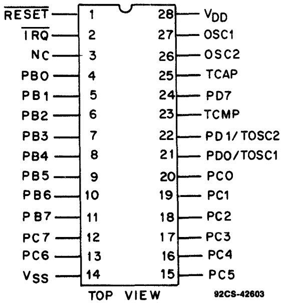


N C = no connection

Q Suffix - 44-Lead Plastic Chip-Carrier Package

CDP68HC05D2A

Product Preview



TERMINAL ASSIGNMENT

CMOS High-Performance Silicon-Gate 8-Bit Microcomputer

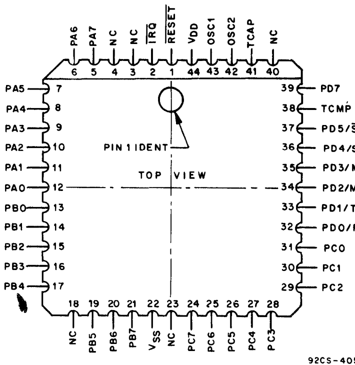
Features:

- *Typical power:*
  Operating, 25 mW
  WAIT, 7.5 mW
  STOP, 5 μW
- *Fully static operation*
- *96 bytes of on-chip RAM*
- *2176 bytes of on-chip ROM*
- *16 I/O and 3-input lines*
- *2.1-MHz internal operating frequency*
- *Internal 16-bit timer*
- *Separate external timer oscillator*
- *External (IRQ), timer, and Port B interrupts*
- *Self-check mode*
- *Single 2.5 to 6-volt supply*
- *RC or crystal on-chip oscillator*
- *8 x 8 multiply instruction*
- *True bit manipulation*
- *Indexed addressing for tables*
- *Memory mapped I/O*

The CDP68HC05D2A Microcomputer Unit (MCU) is a 28-pin version of the 40-pin CDP68HC05D2. In order to accomplish the lower pin count, Port A and lines 2 to 5 of Port D (the SPI bus) are removed in the CDP68HC05D2A, resulting in 12 fewer I/O lines. All other features and functions are identical to those of CDP68HC05D2. Refer to GE publication TSM-204A, "Technical Specifications for the RCA HCMOS Microcomputer CDP68HC05D2." This 8-bit MCU contains on-chip oscillator CPU, RAM, ROM, I/O, and Timer. The fully static design allows operation at frequencies down to DC, further reducing its already low-power consumption. It is a low-power processor designed for low-end to mid-range applications in the telecommunications, consumer, automotive, and industrial markets where low cost and very low power consumption constitute important factors.

The CDP68HC05D2A is supplied in a 28-lead dual-in-line plastic package (E suffix) and a 28-lead plastic chip-carrier package (Q suffix).

TERMINAL ASSIGNMENT



NC = NO CONNECTION

28-Lead Plastic Chip-Carrier Package (Q Suffix)

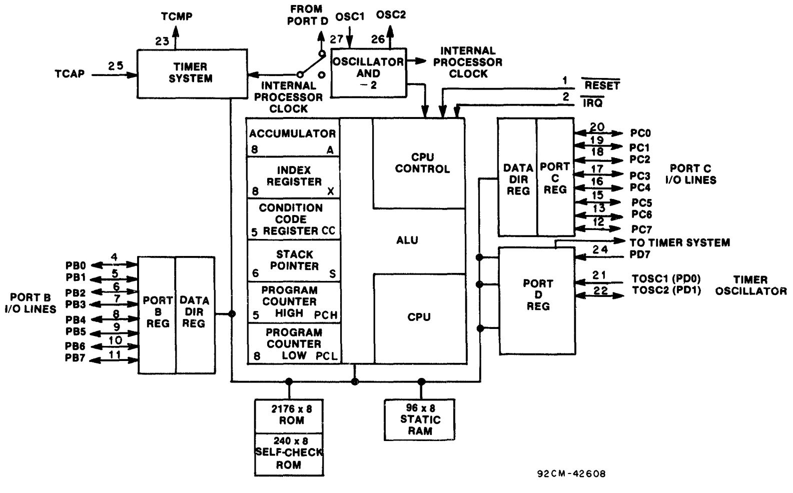
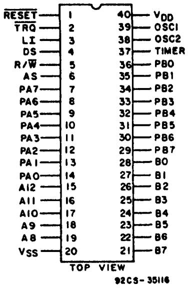


Fig. 1 - CDP68HC05D2A CMOS microcomputer block diagram.

File Number **2100**

CDP6805E2, CDP6805E2C



TERMINAL ASSIGNMENT

CMOS 8-Bit Microprocessor

Hardware Features:

- *Typical full speed operating power of 35 mW @ 5 V*
- *Typical WAIT mode power of 5 mW*
- *Typical STOP mode power of 25 μW*
- *112 bytes of on-chip RAM*
- *16 bidirectional I/O lines*
- *Internal 8-bit timer with software programmable 7-bit prescaler*
- *External timer input*
- *Full external and timer interrupts*
- *Multiplexed address/data bus*
- *Master reset and power-on reset*
- *Capable of addressing up to 8K bytes of external memory*
- *Single 3- to 6-volt supply*
- *On-chip oscillator*
- *40-pin dual-in-line package*
- *44-lead plastic chip-carrier package*

The CDP6805E2 Microprocessor Unit (MPU) belongs to the CDP6805 Family of CMOS Microcomputers. This 8-bit fully static and expandable microprocessor contains a CPU, on-chip RAM, I/O, and Timer. It is a low-power, low-cost processor designed for mid-range applications in the consumer, automotive, industrial, and communications markets where very low power consumption constitutes an important factor. The following are the major features of the CDP6805E2 MPU.

Software Features:

- *Efficient use of program space*
- *Versatile interrupt handling*
- *True bit manipulation*
- *Addressing modes with indexed addressing for tables*
- *Efficient instruction set*
- *Memory mapped I/O*
- *Two power saving standby modes*

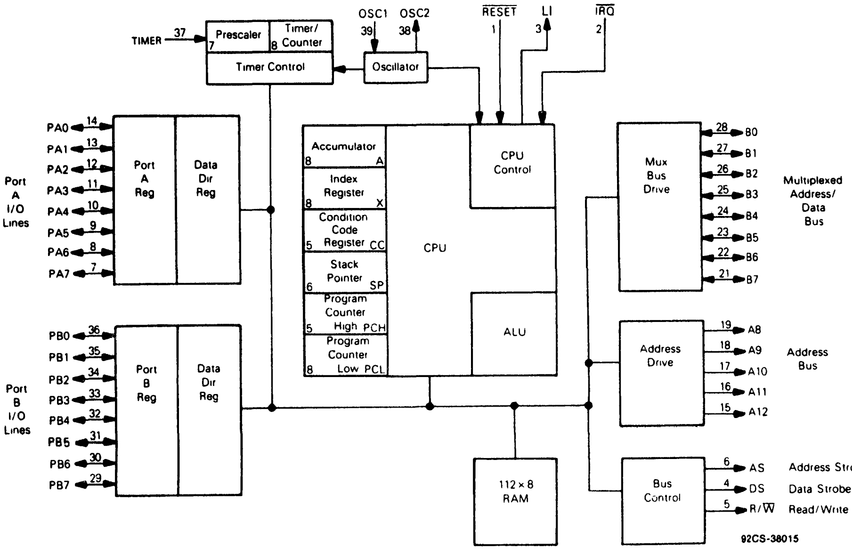


Fig. 1 - Block diagram.

CDP6805E2, CDP6805E2C

MAXIMUM RATINGS (voltages referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0 3 to +8 0	V
All Input Voltages Except OSC1	V_{in}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range CDP6805E2 CDP6805E2C	T_A	T_L to T_H 0 to 70 −40 to 85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

DC ELECTRICAL CHARACTERISTICS 3.0 V (V_{DD}=3 Vdc, V_{SS}=0, T_A=T_L to T_H, unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Output Voltage $I_{LOAD} \leq 10.0\ \mu A$	V_{OL}	–	0 1	V
	V_{OH}	$V_{DD}-0.1$	–	
Total Supply Current (C_L=50 pF – no DC loads) t_{cyc}=5 µs				
Run (V_{IL}=0.2 V, V_{IH}=V_{DD}−0.2 V)	I_{DD}	–	1 3	mA
Wait (Test Conditions – See Note Below)	I_{DD}	–	200	µA
Stop (Test Conditions – See Note Below)	I_{DD}	–	100	µA
Output High Voltage				
(I_{LOAD}=0 25 mA) A8-A12,B0-B7	V_{OH}	2 7	–	V
(I_{LOAD}=0 1 mA) PA0-PA7, PB0-PB7	V_{OH}	2.7	–	V
(I_{LOAD}=0 25 mA) DS, AS, R/$\overline{W}$	V_{OH}	2 7	–	V
Output Low Voltage				
(I_{LOAD}=0.25 mA) A8-A12, B0-B7	V_{OL}	–	0 3	V
(I_{LOAD}=0.25 mA) PA0-PA7, PB0-PB7	V_{OL}	–	0 3	V
(I_{LOAD}=0.25 mA) DS, AS, R/$\overline{W}$	V_{OL}	–	0 3	V
Input High Voltage				
PA0-PA7, PB0-PB7, B0-B7	V_{IH}	2 1	–	V
TIMER, $\overline{IRQ}$, $\overline{RESET}$	V_{IH}	2 5	–	V
OSC1	V_{IH}	2.1	–	V
Input Low Voltage (All inputs)	V_{IL}	–	0 5	V
Frequency of Operation				
Crystal	f_{OSC}	0.032	1 0	MHz
External Clock	f_{OSC}	DC	1 0	MHz
Input Current $\overline{RESET}$, $\overline{IRQ}$, Timer, OSC1	I_{in}	–	±1	µA
Three-State Output Leakage PA0-OA7, PB0-PB7, B0-B7	I_{TSL}	–	±10	µA
Capacitance $\overline{RESET}$, $\overline{IRQ}$, Timer	C_{in}	–	8 0	pF
Capacitance DS, AS, R/$\overline{W}$, A8-A12, PA0-PA7, PB0-PB7, B0-B7	C_{out}	–	12 0	pF

NOTE Test conditions for Quiescent Current Values are:

Port A and B programmed as inputs.

V_{IL}=0 2 V for PA0-PA7, PB0-PB7, and B0-B7

V_{IH}=V_{DD} – 0 2 V for $\overline{RESET}$, $\overline{IRQ}$, and Timer.

OSC1 input is a squarewave from V_{SS}+0.2 V to V_{DD} – 0.2 V.

OSC2 output load (including tester) is 35 pF maximum.

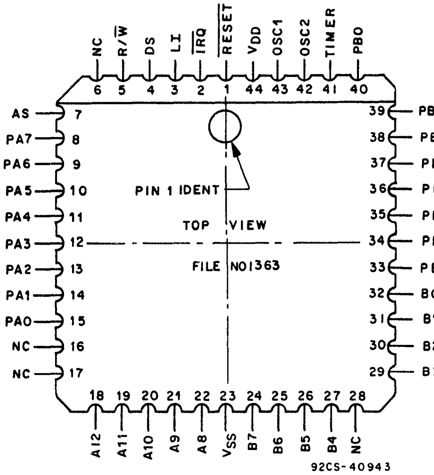
Wait mode I_{DD} is affected linearly by this capacitance

DC ELECTRICAL CHARACTERISTICS 5.0 V (V_{DD}=5 Vdc ± 10%, V_{SS}=0, T_A=T_L to T_H, unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Output Voltage $I_{LOAD} \leq 10.0\ \mu A$	V_{OL}	–	0.1	V
	V_{OH}	V_{DD} – 0.1	–	V
Total Supply Current (C_L = 130 pF – On Bus, C_L = 50 pF – On Ports, No DC Loads, t_{cyc} = 1.0 μs Run (V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V)	I_{DD}	–	10	mA
Wait (Test Conditions – See Note Below)	I_{DD}	–	1.5	mA
Stop (Test Conditions – See Note Below)	I_{DD}	–	200	μA
Output High Voltage (I_{LOAD} = 1.6 mA) A8-A12, B0-B7	V_{OH}	4.1	–	V
(I_{LOAD} = 0.36 mA) PA0-PA7, PB0-PB7	V_{OH}	4.1	–	V
(I_{LOAD} = 1.6 mA) DS, AS, R/$\overline{W}$	V_{OH}	4.1	–	V
Output Low Voltage (I_{LOAD} = 1.6 mA) A8-A12, B0-B7	V_{OL}	–	0.4	V
(I_{LOAD} = 1.6 mA) PA0-PA7, PB0-PB7	V_{OL}	–	0.4	V
(I_{LOAD} = 1.6 mA) DS, AS, R/$\overline{W}$	V_{OL}	–	0.4	V
Input High Voltage PA0-PA7, PB0-PB7, B0-B7	V_{IH}	V_{DD} – 2.0	–	V
TIMER, $\overline{IRQ}$, $\overline{RESET}$	V_{IH}	V_{DD} – 0.8	–	V
OSC1	V_{IH}	V_{DD} – 1.5	–	V
Input Low Voltage (All Inputs)	V_{IL}	–	0.8	V
Frequency of Operation Crystal	f_{OSC}	0.032	5.0	MHz
External Clock	f_{OSC}	DC	5.0	MHz
Input Current $\overline{RESET}$, $\overline{IRQ}$, Timer, OSC1	I_{in}	–	± 1	μA
Three-State Output Leakage PA0-PA7, PB0-PB7, B0-B7	I_{TSI}	–	± 10	μA
Capacitance $\overline{RESET}$, $\overline{IRQ}$, Timer	C_{in}	–	8.0	pF
Capacitance DS, AS, R/$\overline{W}$, A8-A12, PA0-PA7, PB0-PB7, B0-B7	C_{out}	–	12.0	pF

NOTE Test conditions for Quiescent Current Values are
Port A and B programmed as inputs
V_{IL} = 0.2 V for PA0-PA7, PB0-PB7, and B0-B7
V_{IH} = V_{DD} – 0.2 V for $\overline{RESET}$, $\overline{IRQ}$, and Timer
OSC1 input is a squarewave from V_{SS} + 0.2 V to V_{DD} – 0.2 V
OSC2 output load (including tester) is 35 pF maximum
Wait mode (I_{DD}) is affected linearly by this capacitance

TERMINAL ASSIGNMENT



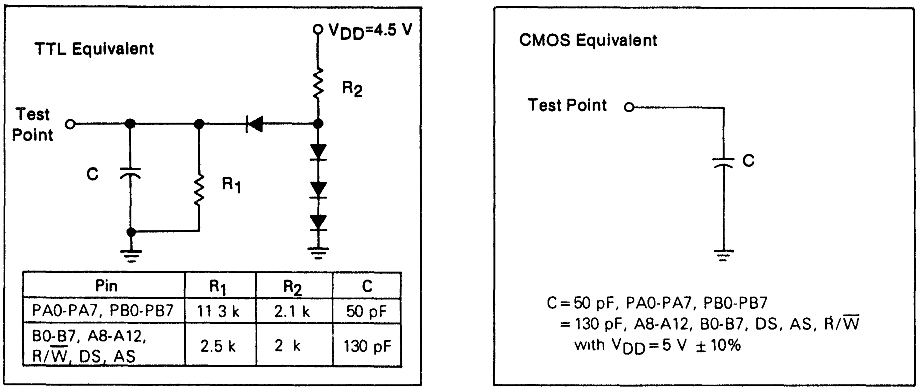
44-Lead Plastic Chip-Carrier (PCC) Package
(Q suffix)

CDP6805E2, CDP6805E2C

TABLE 1 — CONTROL TIMING ($V_{SS}=0$, $T_A=T_L$ to T_H)

		$V_{DD}=3$ V $f_{OSC}=1$ MHz			$V_{DD}=5$ V ± 10% $f_{OSC}=5$ MHz			
Characteristics	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
I/O Port Timing — Input Setup Time (Figure 3)	t_{PVASL}	500	–	–	250	–	–	ns
Input Hold Time (Figure 3)	t_{ASLPX}	100	–	–	100	–	–	ns
Output Delay Time (Figure 3)	t_{ASLPV}	–	–	0	–	–	0	ns
Interrupt Setup Time (Figure 6)	t_{ILASL}	2	–	–	0.4	–	–	μs
Crystal Oscillator Startup Time (Figure 5)	t_{OXOV}	–	30	300	–	15	100	ms
Wait Recovery Startup Time (Figure 7)	t_{IVASH}	–	–	10	–	–	2	μs
Stop Recovery Startup Time (Crystal Oscillator) (Figure 8)	t_{ILASH}	–	30	300	–	15	100	ms
Required Interrupt Release (Figure 6)	t_{DSLIH}	–	–	5	–	–	1 0	μs
Timer Pulse Width (Figure 7)	t_{TH}, t_{TL}	0.5	–	–	0.5	–	–	t_{cyc}
Reset Pulse Width (Figure 5)	t_{RL}	5.2	–	–	1 05	–	–	μs
Timer Period (Figure 7)	t_{TLTL}	1.0	–	–	1 0	–	–	t_{cyc}
Interrupt Pulse Width Low (Figure 16)	t_{ILIH}	1 0	–	–	1 0	–	–	t_{cyc}
Interrupt Pulse Period (Figure 16)	t_{ILIL}	*	–	–	*	–	–	t_{cyc}
Oscillator Cycle Period (1/5 of t_{cyc})	t_{OLOL}	1000	–	–	200	–	–	ms
OSC1 Pulse Width High	t_{OH}	350	–	–	75	–	–	ns
OSC1 Pulse Width Low	t_{OL}	350	–	–	75	–	–	ns

*The minimum period t_{ILIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routine plus 20 t_{cyc} cycles.



Pin	R_1	R_2	C
PA0-PA7, PB0-PB7	11 3 k	2.1 k	50 pF
B0-B7, A8-A12, R/$\overline{W}$, DS, AS	2.5 k	2 k	130 pF

C = 50 pF, PA0-PA7, PB0-PB7
= 130 pF, A8-A12, B0-B7, DS, AS, R/$\overline{W}$
with $V_{DD}=5$ V ±10%

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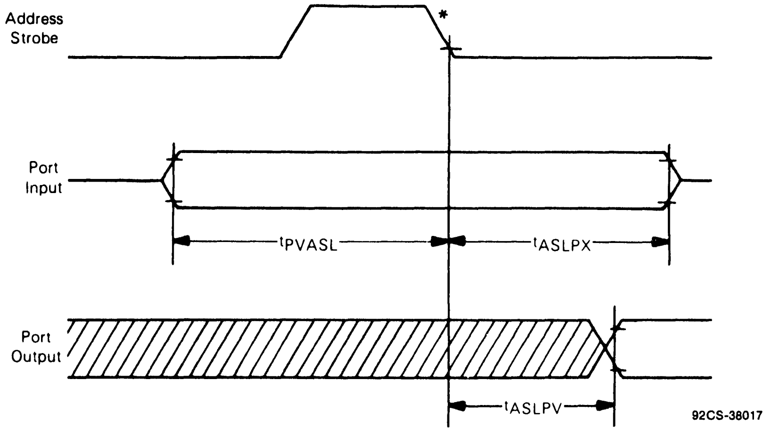
Fig. 2 - Equivalent test-load circuits.

($V_{LOW}=0.8$ V, $V_{HIGH}=V_{DD}-2$ V, $V_{DD}=5\pm10\%$
Temp = 0° to 70°C, C_L on Port = 50 pF, $f_{OSC}=5$ MHz)

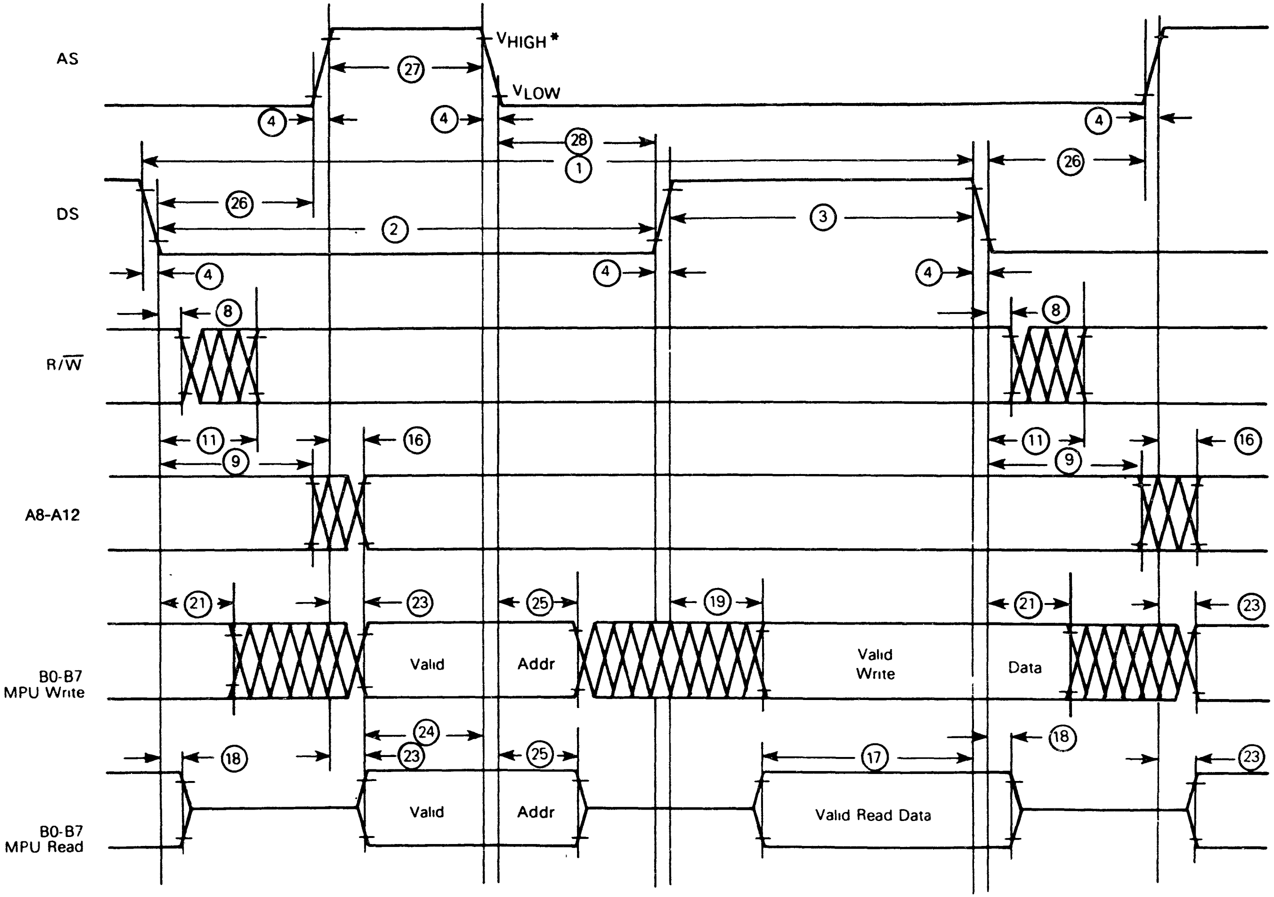


*The address strobe of the first cycle of the next instruction as shown in Table 11

Fig. 3 - I/O port timing waveforms.

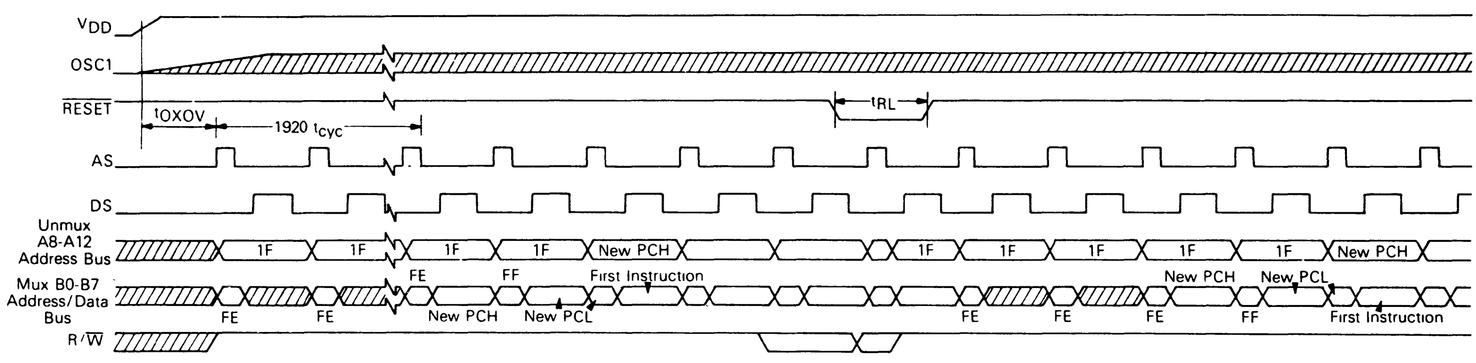
TABLE 2 — BUS TIMING ($T_A=T_L$ to T_H, $V_{SS}=0$ V) See Figure 4

Num	Characteristics	Symbol	$f_{OSC}=1$ MHz, $V_{DD}=3$ V 50 pF Load		$f_{OSC}=5$ MHz $V_{DD}=5$ V $\pm10\%$, 1 TTL and 130 pF Load		Unit
			Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	5000	DC	1000	DC	ns
2	Pulse Width, $\overline{DS}$ Low	PW_{EL}	2800	–	560	–	ns
3	Pulse Width, DS High or $\overline{RD}$, $\overline{WR}$, Low	PW_{EH}	1800	–	375	–	ns
4	Clock Transition	t_r, t_f	–	100	–	30	ns
8	R/$\overline{W}$ Hold	t_{RWH}	10	–	10	–	ns
9	Non-Muxed Address Hold	t_{AH}	800	–	100	–	ns
11	R/$\overline{W}$ Delay from DS Fall	t_{AD}	–	500	–	300	ns
16	Non-Muxed Address Delay from AS Rise	t_{ADH}	0	200	0	100	ns
17	MPU Read Data Setup	t_{DSR}	200	–	115	–	ns
18	Read Data Hold	t_{DHR}	0	1000	0	160	ns
19	MPU Data Delay, Write	t_{DDW}	–	0	–	120	ns
21	Write Data Hold	t_{DHW}	800	–	55	–	ns
23	Muxed Address Delay from AS Rise	t_{BHD}	0	250	0	120	ns
24	Muxed Address Valid to AS Fall	t_{ASL}	600	–	55	–	ns
25	Muxed Address Hold	t_{AHL}	250	750	60	180	ns
26	Delay DS Fall to AS Rise	t_{ASD}	800	–	160	–	ns
27	Pulse Width, AS High	PW_{ASH}	850	–	175	–	ns
28	Delay, AS Fall to DS Rise	t_{ASED}	800	–	160	–	ns

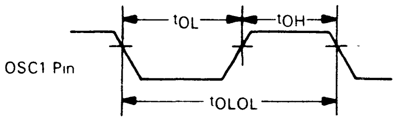


* V_{HIGH} = -2 V, V_{LOW} = 0.5 V for V_{DD} = 3 V
V_{HIGH} = V_{DD} -2 V, V_{LOW} = 0.8 V for V_{DD} = 5 V ± 10 %

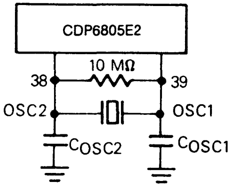
Fig. 4 - Bus timing waveforms.



Oscillator Waveform



Crystal Oscillator Connections



Crystal Parameters Representative Frequencies

	5 MHz	4 MHz	1 MHz
RS max	50Ω	75Ω	400Ω
C0	8 pF	7 pF	5 pF
C1	0.02 pF	0.012 pF	0.008 pF
Q	50 k	40 k	30 k
C_{OSC1}	15-30 pF	15-30 pF	15-40 pF
C_{OSC2}	15-25 pF	15-25 pF	15-30 pF

Crystal Circuit

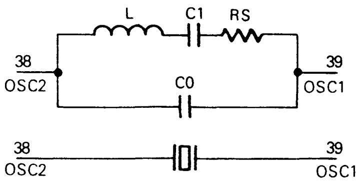


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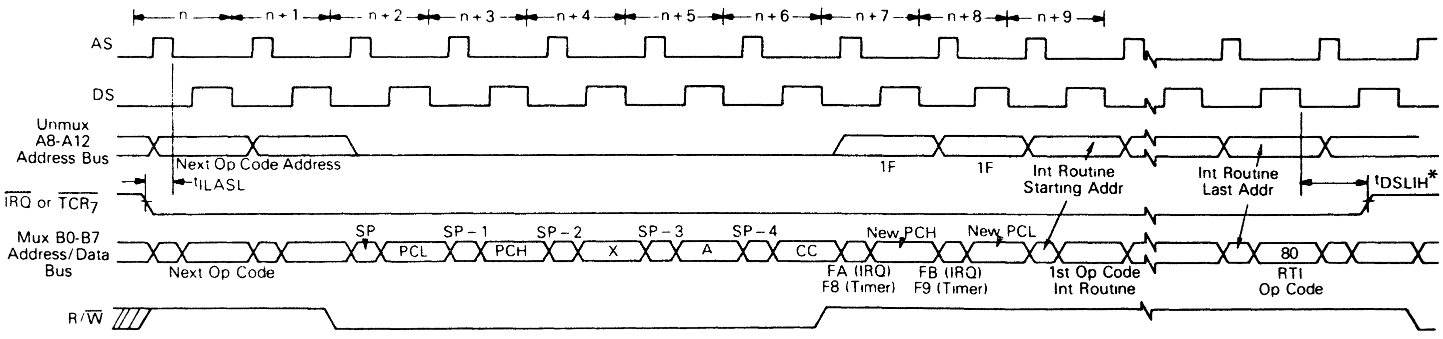
Fig. 5 - Power-on reset and $\overline{\text{reset}}$ timing waveforms.



*t_{DSLIH} – The interrupting device must release the IRQ line within this time to prevent subsequent recognition of the same interrupt

Fig. 6 - $\overline{IRQ}$ and $\overline{TCR_7}$ interrupt timing waveforms.

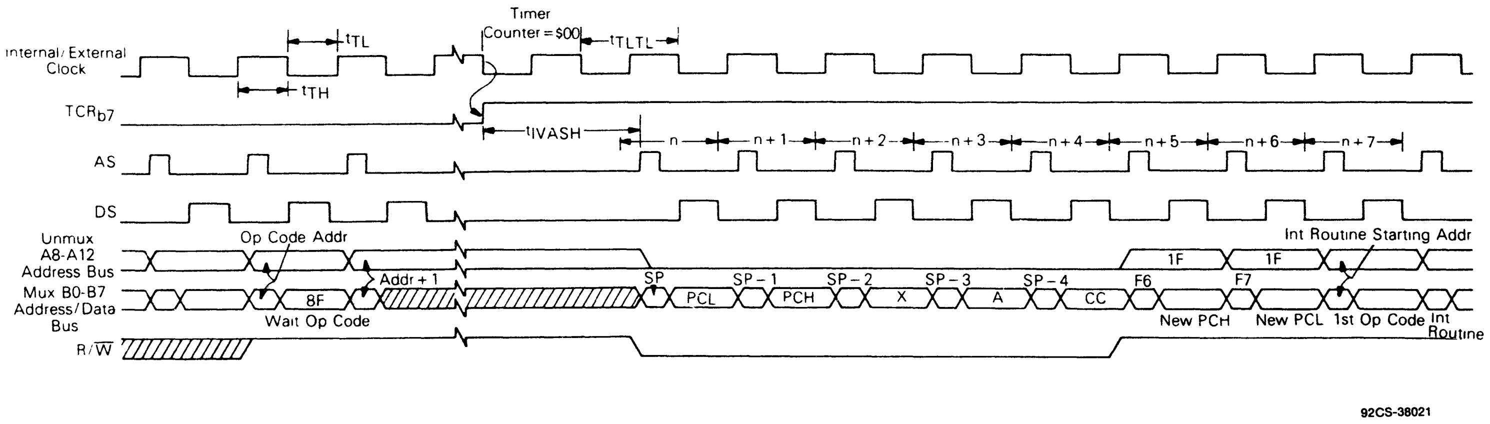
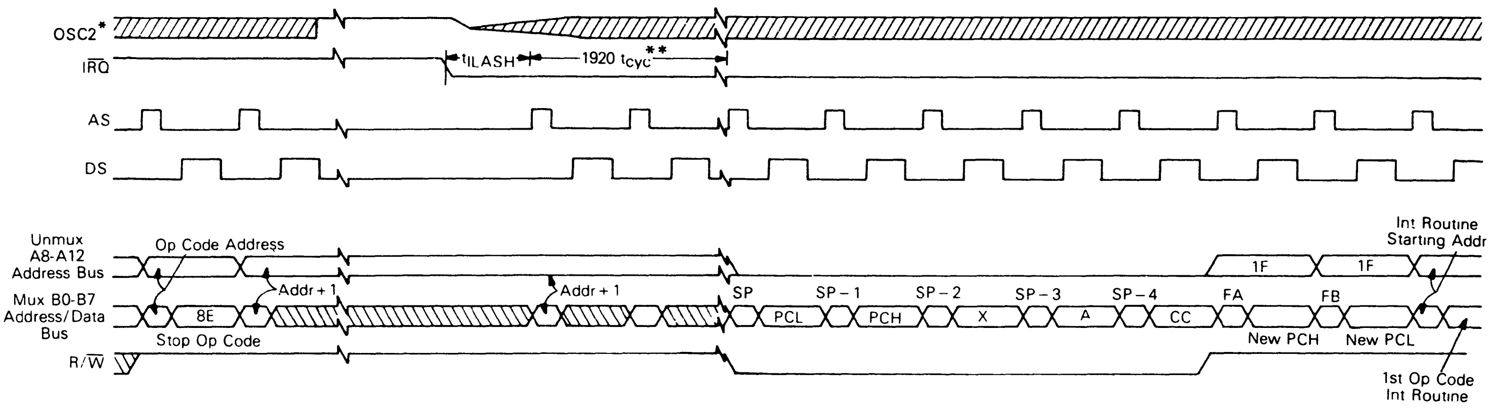


Fig. 7 - Timer interrupt after WAIT instruction timing waveforms.



* Represents the internal gating of the OSC1 input pin.

** t_{cyc} is one instruction cycle (for $f_{OSC} = 5$ MHz, $t_{cyc} = 1$ μs)

Fig. 8 - Interrupt recovery from STOP instruction timing waveforms.

3

CDP6805E2, CDP6805E2C

FUNCTIONAL PIN DESCRIPTION

V_{DD} and V_{SS} – V_{DD} and V_{SS} provide power to the chip V_{DD} provides power and V_{SS} is ground

$\overline{\text{IRQ}}$ (Maskable Interrupt Request) – $\overline{\text{IRQ}}$ is a level-sensitive and edge sensitive input which can be used to request an interrupt sequence The MPU completes the current instruction before it responds to the request If $\overline{\text{IRQ}}$ is low and the interrupt mask bit (I-bit) in the Condition Code Register is clear, the MPU begins an interrupt sequence at the end of the current instruction The interrupt circuit recognizes both a "Wire ORed" level as well as pulses on the $\overline{\text{IRQ}}$ line (see Interrupt Section for more details) $\overline{\text{IRQ}}$ requires an external resistor to V_{DD} for "Wire OR" operation

$\overline{\text{RESET}}$ – The $\overline{\text{RESET}}$ input is not required for start-up but can be used to reset the MPU's internal state and provide an orderly software start-up procedure Refer to the RESET section for a detailed description

TIMER – The TIMER input is used for clocking the on-chip timer. Refer to TIMER section for a detailed description

AS (Address Strobe) – Address Strobe (AS) is an output strobe used to indicate the presence of an address on the 8-bit multiplexed bus. The AS line is used to demultiplex the eight least significant address bits from the data bus. A latch controlled by Address Strobe should capture addresses on the negative edge. This output is capable of driving one standard TTL load and 130 pF and is available at $f_{OSC} \div 5$ when the MPU is not in the WAIT or STOP states.

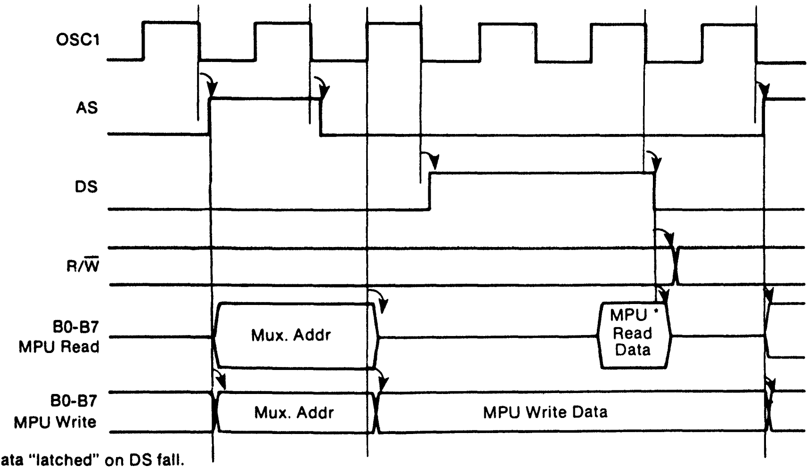
DS (Data Strobe) – This output is used to transfer data to or from a peripheral or memory. DS occurs anytime the MPU does a data read or write. DS also occurs when the MPU does a data transfer to or from the MPU's internal memory Refer to Table 2 and Figure 4 for timing characteristics This output is capable of driving one standard TTL load and 130 pF. DS is a continuous signal at $f_{OSC} \div 5$ when the MPU is not in WAIT or STOP state. Some bus cycles are redundant reads of op code bytes

R/$\overline{\text{W}}$ (Read/Write) – The R/$\overline{\text{W}}$ output is used to indicate the direction of data transfer for both internal memory and I/O registers, and external peripheral devices and memories. This output is used to indicate to a selected peripheral whether the MPU is going to read or write data on the next Data Strobe (R/$\overline{\text{W}}$ low = processor write; R/$\overline{\text{W}}$ high = processor read). The R/$\overline{\text{W}}$ output is capable of driving one standard TTL load and 130 pF. The normal standby state is Read (high)

A8-A15 (High Order Address Lines) – The A8-A15 output lines constitute the higher order non-multiplexed addresses Each output line is capable of driving one standard TTL load and 130 pF

B0-B7 (Address/Data Bus) – The B0-B7 bidirectional lines constitute the lower order addresses and data. These lines are multiplexed, with address present at Address Strobe time and data present at Data Strobe time When in the data mode, these lines are bidirectional, transferring data to and from memory and peripheral devices as indicated by the R/$\overline{\text{W}}$ pin As outputs in either the data or address modes, these lines are capable of driving one standard TTL load and 130 pF

OSC1, OSC2 – The CDP6805E3 provides for two types of oscillator inputs — crystal circuit or external clock. The two oscillator pins are used to interface to a crystal circuit, as shown in Figure 5. If an external clock is used, it must be connected to OSC1 The input at these pins is divided by five to form the cycle rate seen on the AS and DS pins The frequency range is specified by f_{OSC} The OSC1 to bus transitions relationships are provided in Figure 9 for system designs using oscillators slower than 5 MHz



* Read data "latched" on DS fall.

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Fig. 9 - OSC1 to bus transitions timing waveforms.

Crystal – The circuit shown in Figure 5 is recommended when using a crystal The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{OSC} in the electrical characteristics table An external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time.

External Clock – An external clock should be applied to the OSC1 input with the OSC2 input not connected, as shown in Figure 10

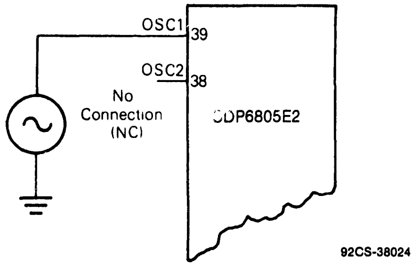
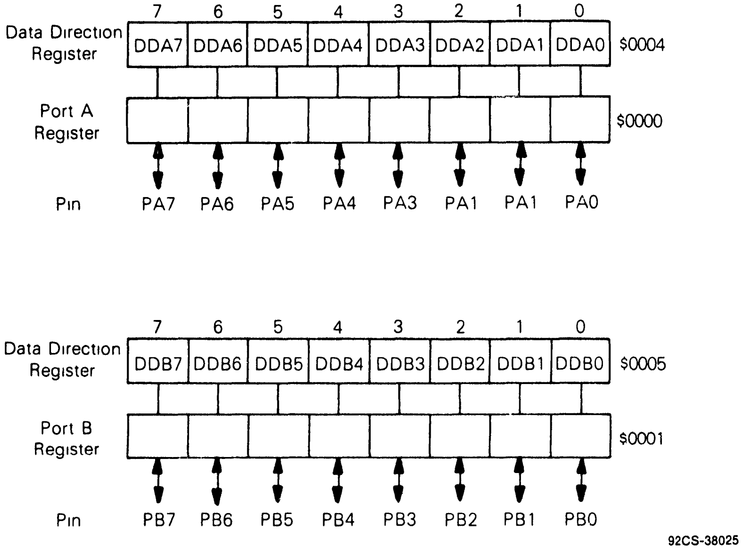


Fig. 10 - External clock connection.

LI (Load Instruction) – This output is used to indicate that a fetch of the next opcode is in progress. LI remains low during an External or Timer interrupt The LI output is only used for certain debugging and test systems For normal operations this pin is not connected. The LI output is capable of driving one standard TTL load and 50 pF This signal overlaps Data Strobe

PA0-PA7 – These eight pins constitute Input/Output Port A. Each line is individually programmed to be either an input or output under software control via its Data Direction Register as shown below. An I/O pin is programmed as an output when the corresponding DDR bit is set to a "1," and as an input when it is set to a "0" In the output mode the bits are latched and appear on the corresponding output pins. An MPU read of the port bits programmed as outputs reflect the last value written to that location. When programmed as an input, the input data bit(s) are not latched An MPU read of the port bits programmed as inputs reflects the current status of the corresponding input pins The Read/Write port timing is shown in Figure 3 See typical I/O Port Circuitry in Figure 11. During a Power-On Reset or external $\overline{\text{RESET}}$ all lines are configured as inputs (zero in Data Direction Register) The output port register is not initialized by reset The TTL compatible three-state output buffers are capable of driving one standard TTL load and 50 pF The DDR is a read/write register

PB0-PB7 – These eight pins interface to Input/Output Port B Refer to PA0-PA7 description for details of operation



CDP6805E2, CDP6805E2C

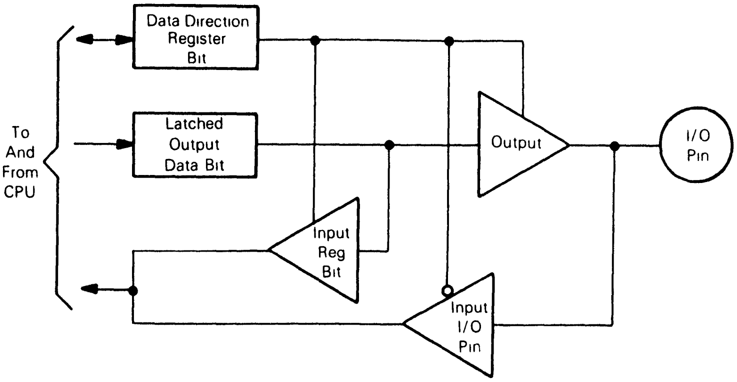


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Fig. 11 - Typical I/O port circuitry.

TABLE 3 – I/O PIN FUNCTIONS

R/$\overline{W}$	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode Data is written into the output data latch
0	1	Data is written into the output data latch and output to the I/O pin
1	0	The state of the I/O pin is read
1	1	The I/O pin is in an output mode The output data latch is read

MEMORY ADDRESSING

The CDP6805E2 is capable of addressing 8192 bytes of memory and I/O registers. The address space is divided into internal memory space and external memory space, as shown in Figure 12.

The internal memory space is located within the first 128 bytes of memory (first half of page zero) and is comprised of the I/O port locations, timer locations, and 112 bytes of RAM. The MPU can read from or write to any of these locations. A program write to on-chip locations is repeated on the external bus to permit off-chip memory to duplicate the content of on-chip memory. Program reads to on-chip locations also appear on the external bus, but the MPU accepts data only from the addressed on-chip location. Any read data appearing on the input bus is ignored.

The stack pointer is used to address data stored on the stack. Data is stored on the stack during interrupts and subroutine calls At power up, the stack pointer is set to $7F and it is decremented as data is pushed onto the stack When data is removed from the stack, the stack pointer is incremented A maximum of 64 bytes of RAM is available for stack usage. Since most programs use only a small part of the allotted stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are usable for program data storage

All memory locations above location $007F are part of the external memory map. In addition, ten locations in the I/O portion of the lower 128 bytes of memory space, as shown in Figure 12, are part of the external memory map All of the external memory space is user definable except the highest 10 locations Locations $1FF6 to $1FFF of the external address space are reserved for interrupt and reset vectors (see Figure 12).

REGISTERS

The CDP6805E2 contains five registers as shown in the programming model in Figure 13 The interrupt stacking order is shown in Figure 14

ACCUMULATOR (A) – This Accumulator is an 8-bit general purpose register used for arithmetic calculations and data manipulations.

INDEX REGISTER (X) – The X register is an 8-bit register which is used during the indexed modes of addressing It provides an 8-bit operand which is used to create an effective address The index register is also used for data manipulations with the Read/Modify/Write type of instructions and as a temporary storage register when not performing addressing operations

PROGRAM COUNTER (PC) – The program counter is a 13-bit register that contains the address of the next instruction to be executed by the processor

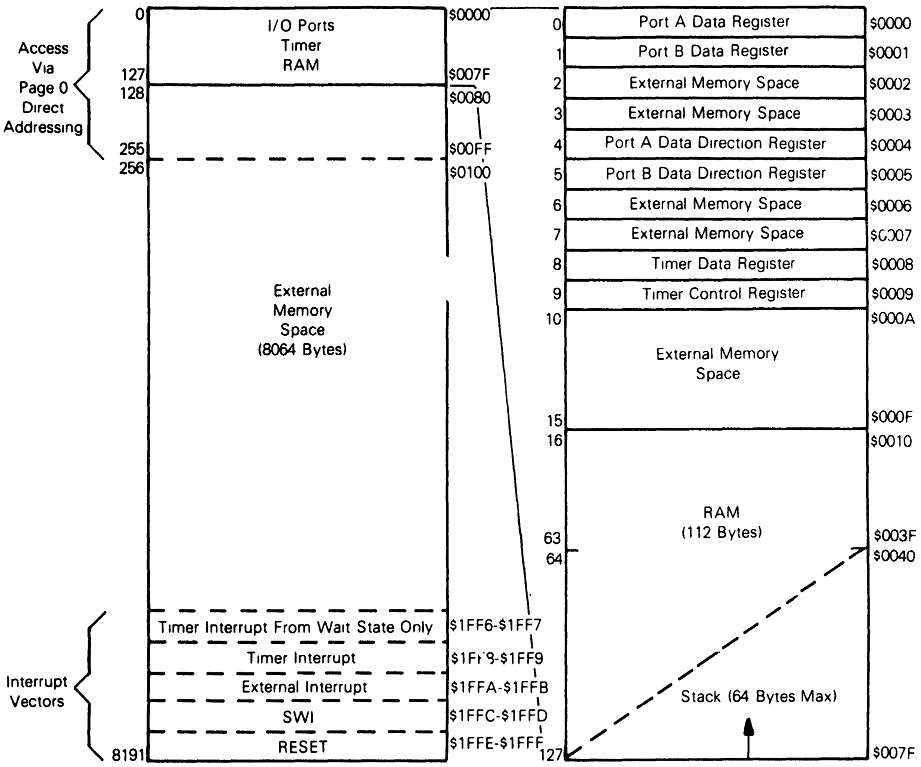

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Fig. 12 - Address map.

CDP6805E2, CDP6805E2C

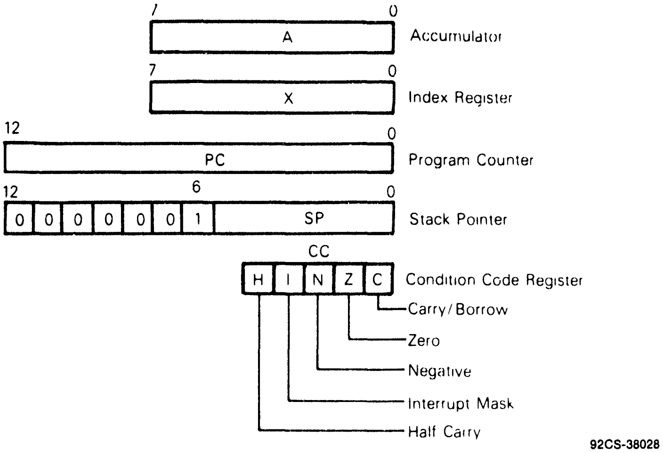
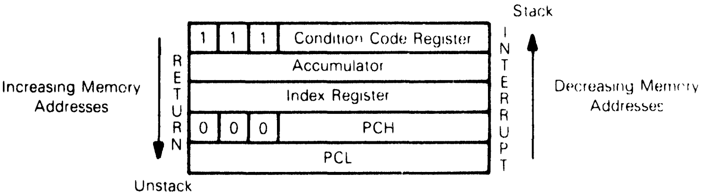


Fig. 13 - Programming model.


Stack
1 1 1 Condition Code Register
Accumulator
Index Register
0 0 0 PCH
PCL
Increasing Memory Addresses
RETURN
Unstack
INTERRUPT
Decreasing Memory Addresses

NOTE Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc Pulling from the stack is in the reverse order

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Fig. 14 - Stacking order.

STACK POINTER (SP) – The stack pointer is a 13-bit register containing the address of the next free location on the stack When accessing memory, the seven most-significant bits are permanently set to 0000001. They are appended to the six least-significant register bits to produce an address within the range of $007F to $0040. The stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts. During external or power-on reset, and during a "reset stack pointer" instruction, the stack pointer is set to its upper limit ($007F). Nested interrupts and/or subroutines may use up to 64 (decimal) locations, beyond which the stack pointer "wraps around" and points to its upper limit thereby losing the previously stored information A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five bytes

CONDITION CODE REGISTER (CC) – The condition code register is a 5-bit register in which each bit is used to indicate the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state Each of the five bits is explained below

Half Carry Bit (H) – The H-bit is set to a one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H-bit is useful in Binary Coded Decimal addition subroutines.

Interrupt Mask Bit (I) – When the I-bit is set, both the external interrupt and the timer interrupt are disabled Clearing this bit enables the above interrupts. If an interrupt occurs while the I-bit is set, the interrupt is latched and will be processed when the I-bit is next cleared

Negative Bit (N) – When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (bit 7 in the result is a logical one)

Zero Bit (Z) – When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero

Carry Bit (C) – The C-bit is set when a carry or a borrow out of the ALU occurs during an arithmetic instruction. The C-bit is also modified during bit test, shift, rotate, and branch types of instruction

RESETS

The CDP6805E2 has two reset modes: an active low external reset pin ($\overline{\text{RESET}}$) and a Power-On Reset function, refer to Figure 5

$\overline{\text{RESET}}$ (Pin #1) – The $\overline{\text{RESET}}$ input pin is used to reset the MPU and provide an orderly software start-up procedure. When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one t_{cyc}. The $\overline{\text{RESET}}$ pin is provided with a Schmitt Trigger to improve its noise immunity capability.

Power-On Reset – The Power-on Reset occurs when a positive transition is detected on V_{DD}. The Power-on Reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. There is no provision for a power-down reset. The power-on circuitry provides for a 1920 t_{cyc} delay from the time of the first oscillator operation. If the external reset pin is low at the end of the 1920 t_{cyc} time out, the processor remains in the reset condition.

Either of the two types of reset conditions causes the following to occur:

- Timer control register interrupt request bit (bit 7) is cleared to a "0".
- Timer control register interrupt mask bit (bit 6) is set to a "1".
- All data direction register bits are cleared to a "0" (inputs).
- Stack pointer is set to $007F.
- The address bus is forced to the reset vector ($1FFE, $1FFF).
- Condition code register interrupt mask bit (I) is set to a "1".
- STOP and WAIT latches are reset.
- External interrupt latch is reset.

All other functions, such as other registers (including output ports) the timer, etc., are not cleared by the reset conditions.

INTERRUPTS

The CDP6805E2 is capable of operation with three different interrupts, two hardware (timer interrupt and external interrupt) and one software (SWI). When any of these interrupts occur, normal processing is suspended at the end of the current instruction execution. All of the program registers (the machine state) are pushed onto the stack, refer to Figure 14 for stacking order The appropriate vector pointing to the starting address of the interrupt service routine is then fetched, refer to Figure 15 for the interrupt sequence.

The priority of the various interrupts from highest to lowest is as follows·

RESET→*→External Interrupt→Timer Interrupt

TIMER INTERRUPT – If the timer mask bit (TCR6) is cleared, then each time the timer decrements to zero (transitions from $01 to $00) an interrupt request is generated The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared When the interrupt is recognized, the current state of the machine is pushed onto the stack and the I-bit in the condition code register is set This masks further interrupts until the present one is serviced The processor now vectors to the timer interrupt service routine. The address for this service routine is specified by the contents of $1FF8 and $1FF9. The contents of $1FF6 and $1FF7 specify the service routine. Also, software must be used to clear the timer interrupt request bit (TCR7). At the end of the timer interrupt service routine, the software normally executes an RTI instruction which restores the machine state and starts executing the interrupted program.

EXTERNAL INTERRUPT – If the interrupt mask bit of the condition code register is cleared and the external interrupt pin $\overline{\text{IRQ}}$ is "low," then the external interrupt occurs The action of the external interrupt is identical to the timer interrupt with the exception that the service routine address is specified by the contents of $1FFA and $1FFB The interrupt logic recognizes both a "wire ORed" level and pulses on the external interrupt line Figure 16 shows both a functional diagram and timing for the interrupt line The timing diagram shows two different treatments of the interrupt line ($\overline{\text{IRQ}}$) to the processor The first configuration shows many interrupt lines "wire ORed" to form the interrupts at the processor Thus, if after servicing an interrupt the $\overline{\text{IRQ}}$ remains low, then the next interrupt is recognized The second method is single pulses on the interrupt line spaced far enough apart to be service. The minimum time between pulses is a function of the length of the interrupt service routine. Once a pulse occurs, the next pulse should not occur until the MPU software has exited the routine (an RTI occurs) This time (t_{ILIL}) is obtained by adding 20 instruction cycles (one cycle $t_{cyc}=5/f_{OSC}$) to the total number of cycles it takes to complete the service routine including the RTI instruction; refer to Figure 6.

SOFTWARE INTERRUPT (SWI) – The software interrupt is an executable instruction The action of the SWI instruction is similar to the hardware interrupts The SWI is executed regardless of the state of the interrupt mask in the condition code register. The service routine address is specified by the contents of memory locations $1FFC and $1FFD See Figure 15 for Interrupt and Instruction Processing Flowchart

The following three functions are not strictly interrupts, however, they are tied very closely to the interrupts These functions are $\overline{\text{RESET}}$, STOP, WAIT

$\overline{\text{RESET}}$ – The $\overline{\text{RESET}}$ input pin and the internal Power-on Reset function each cause the program to vector to an initialization program This vector is specified by the contents of memory locations $1FFE and $1FFF The interrupt mask of the condition code register is also set Refer to RESET section for details

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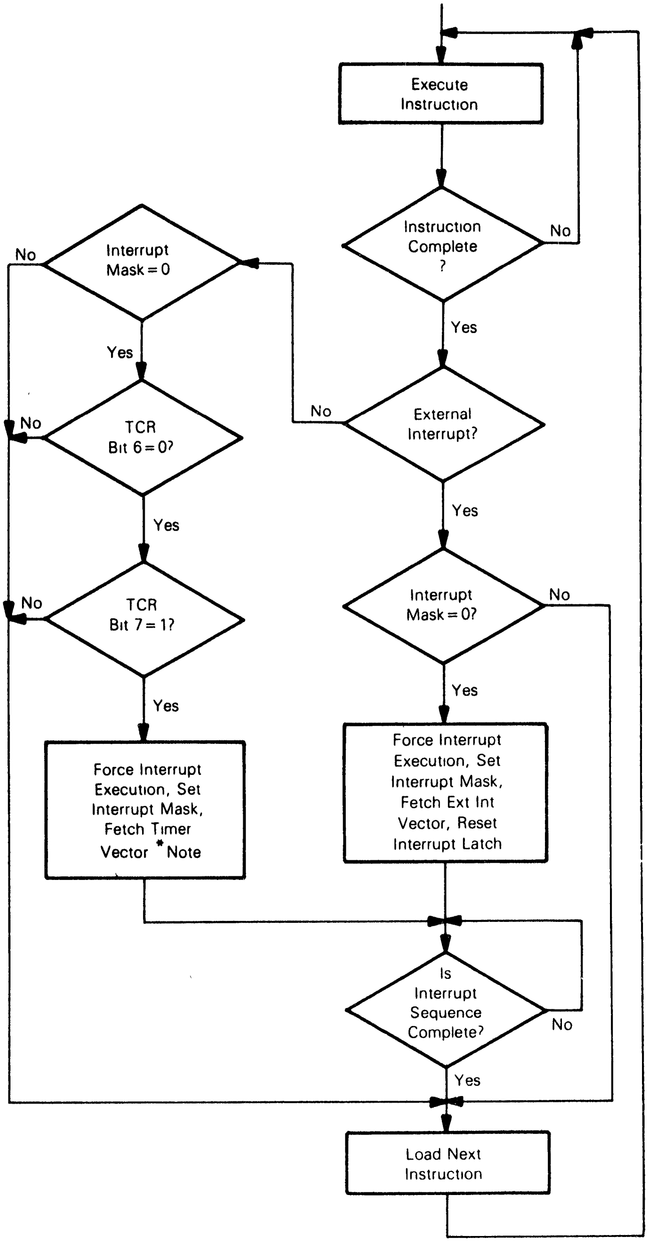
*Any current instruction including SWI.


Execute Instruction
Instruction Complete ?
No
Yes
External Interrupt?
No
Yes
Interrupt Mask = 0?
No
Yes
Force Interrupt Execution, Set Interrupt Mask, Fetch Ext Int Vector, Reset Interrupt Latch
Interrupt Mask = 0
No
Yes
TCR Bit 6 = 0?
No
Yes
TCR Bit 7 = 1?
No
Yes
Force Interrupt Execution, Set Interrupt Mask, Fetch Timer Vector *Note
Is Interrupt Sequence Complete?
No
Yes
Load Next Instruction

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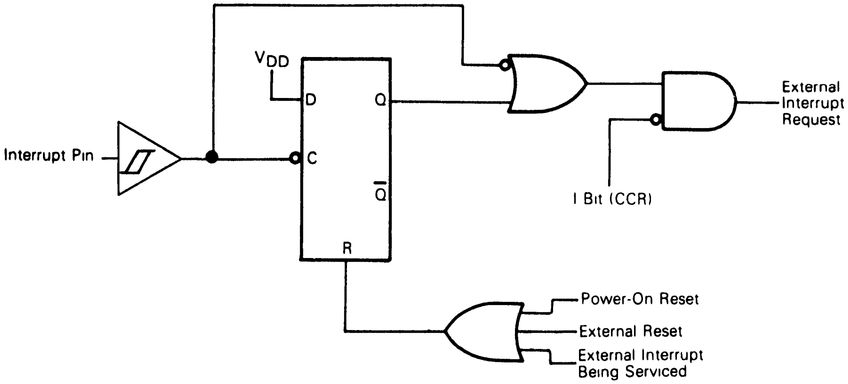
*NOTE: The clear of TCR bit 7 must be accomplished with software.

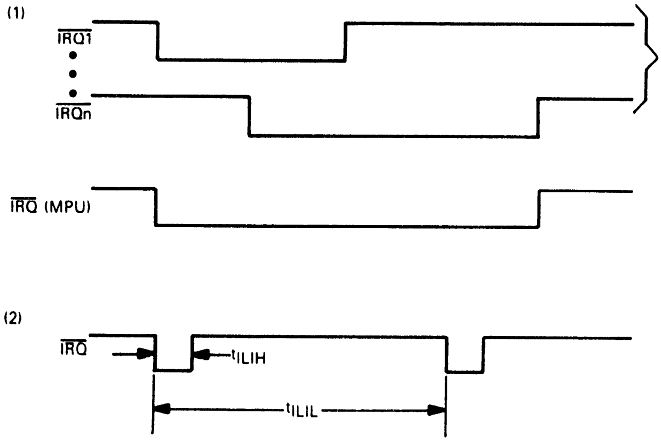
Fig. 15 - Interrupt and instruction processing flowchart.

CDP6805E2, CDP6805E2C

(a) Interrupt Functional Diagram



(b) Interrupt Mode Diagram



Wire OR'ed Condition
(If after servicing an interrupt the $\overline{IRQ}$ remains low, then the next interrupt is recognized)

Pulse Condition

The minimum pulse width (t_{ILIH}) is one t_{cyc} The period t_{ILIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routine plus 20 t_{cyc} cycles

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Fig. 16 - External interrupt.

CDP6805E2, CDP6805E2C

STOP – The STOP instruction places the CDP6805E2 in a low power consumption mode. In the STOP function the internal oscillator is turned off, causing all internal processing and the timer to be halted, refer to Figure 17. The DS and AS lines go to a low state and the R/$\overline{W}$ line goes to a high state. The multiplexed address/data bus goes to the data input state. The high order address lines remain at the address of the next instruction. The MPU remains in the STOP mode until an external interrupt or reset occurs; refer to Figure 8 and 17.

During the STOP mode, timer control register (TCR) bits 6 and 7 are altered to remove any pending timer interrupt requests and to disable any further timer interrupts. External interrupts are enabled in the condition code register. All other registers and memory remain unaltered. All I/O lines remain unchanged.

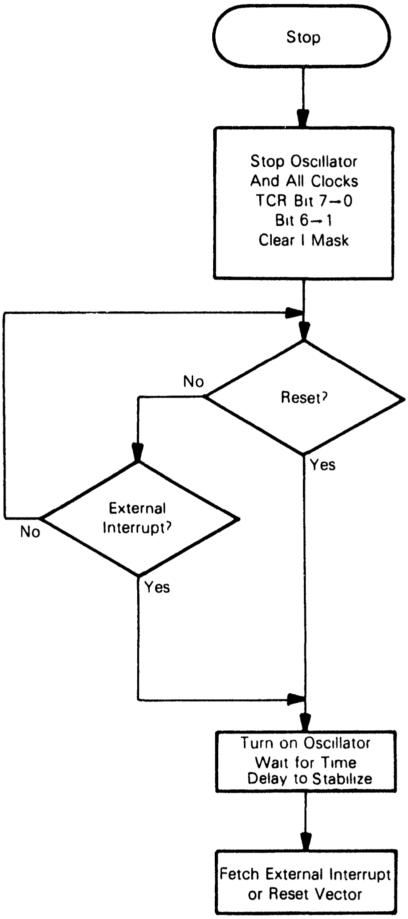

Fig. 17 - Stop function flowchart.

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WAIT – The WAIT instruction places the CDP6805E2 in a low power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode; refer to Table 1. In the WAIT function, the internal clock is disabled from all internal circuitry except the Timer circuit, refer to Figure 18. Thus, all internal processing is halted except the Timer which is allowed to count in a normal sequence. The R/$\overline{W}$ line goes to a high state, the multiplexed address/data bus goes to the data input state, and the DS and AS lines go to the low state. The high order address lines remain at the address of the next instruction. The MPU remains in this state until an external interrupt, timer interrupt, or a reset occurs, refer to Figures 7 and 18.

During the WAIT mode, the I-bit in the condition code register is cleared to enable interrupts. All other registers, memory, and I/O lines remain in their last state. The timer may be enabled to allow a periodic exit from the WAIT mode.If an external and a timer interrupt occur at the same time, the external interrupt is serviced first, then, if the timer interrupt request is not cleared in the external interrupt routine, the normal timer interrupt (not the timer WAIT interrupt) is serviced since the MCU is no longer in the WAIT mode.

TIMER

The MPU timer contains a single 8-bit software programmable counter with 7-bit software selectable prescaler. The counter may be preset under program control and decrements towards zero. When the counter decrements to zero, the timer interrupt request bit, i.e., bit 7 of the Timer Control Register (TCR) is set. Then if the timer interrupt is not masked, i.e., bit 6 of the TCR and the I-bit in the Condition Code Register are both cleared, the processor receives an interrupt. After completion of the current instruction, the processor proceeds to store the appropriate registers on the stack, and then fetches the timer vector address from locations \$1FF8 and \$1FF9 in order to begin servicing the interrupt, unless it was in locations \$1FF6 and \$1FF7 the WAIT mode.

The counter continues to count after it reaches zero, allowing the software to determine the number of internal or external input clocks since the timer interrupt request bit was set. The counter may be read at any time by the processor without disturbing the count. The contents of the counter becomes stable prior to the read portion of a cycle and does not change during the read. The timer interrupt request bit remains set until cleared by the software. If this happens before the timer interrupt is serviced, the interrupt is lost. TCR7 may also be used as a scanned status bit in a non-interrupt mode of operation (TCR6 = 1).

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer. Bit 0, bit 1, and bit 2 of the TCR are programmed to choose the appropriate prescaler output which is used as the counter input. The processor cannot write into or read from the prescaler, however, its contents are cleared to all "0's" by the write operation into TCR when bit 3 of the written data equals 1, which allows for truncation-free counting.

The Timer input can be configured for three different operating modes, plus a disable mode depending on the value written to the TCR4, TCR5 control bits. Refer to the TIMER CONTROL REGISTER section.

Timer Input Mode 1 – If TCR4 and TCR5 are both programmed to a "0", the input to the Timer is from an internal clock and the Timer input is disabled. The internal clock mode can be used for periodic interrupt generation, as well

CDP6805E2, CDP6805E2C

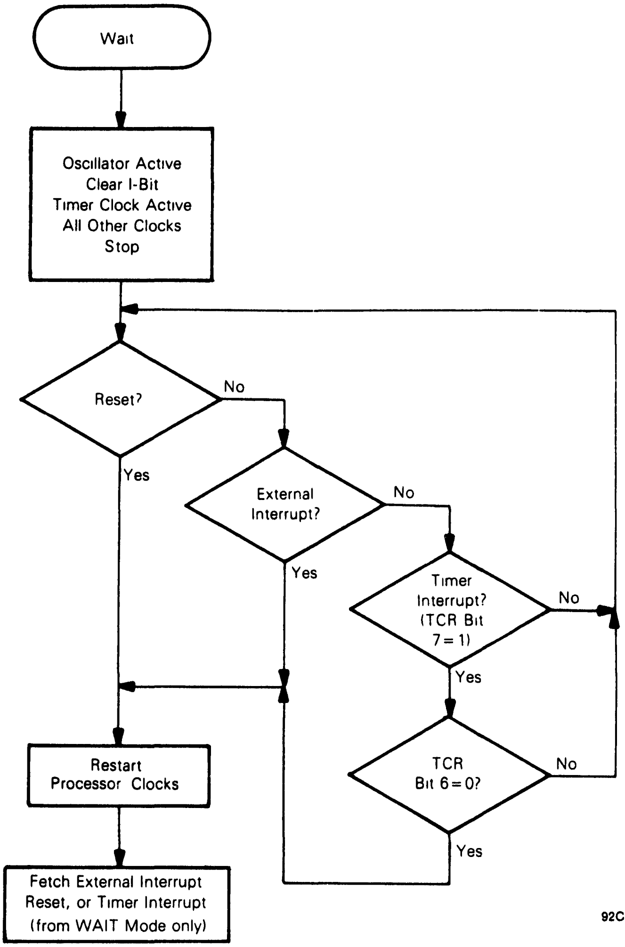

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Fig. 18 - Wait function flowchart.

as a reference in frequency and event measurement. The internal clock is the instruction cycle clock and is coincident with Address Strobe (AS) except during a WAIT instruction. During a WAIT instruction the AS pin goes to a low state but the internal clock to the Timer continues to run at its normal rate.

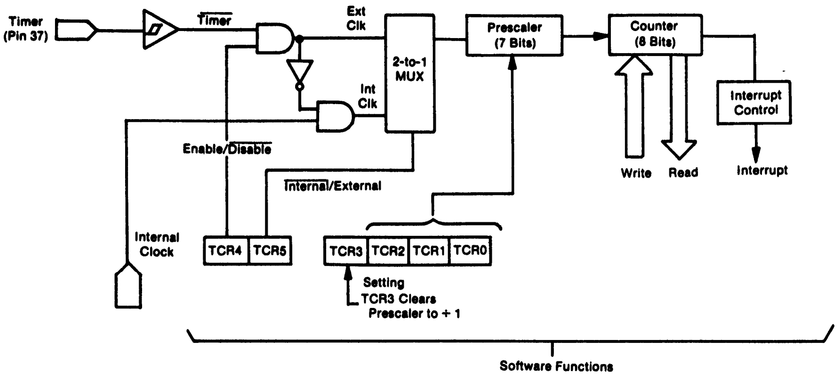
Timer Input Mode 2 – With TCR4=1 and TCR5=0, the internal clock and the TIMER input pin are ANDed together to form the Timer input signal. This mode can be used to measure external pulse widths. The external pulse simply turns on the internal clock for the duration of the pulse. The resolution of the count in this mode is ±1 clock and therefore accuracy improves with longer input pulse widths.

Timer Input Mode 3 – If TCR4=0 and TCR5=1, then all inputs to the Timer are disabled.

Timer Input Mode 4 – If TCR4=1 and TCR5=1, the internal clock input to the Timer is disabled and the TIMER input pin becomes the input to the Timer. The external Timer pin can, in this mode, be used to count external events as well as external frequencies for generating periodic interrupts.

Figure 19 shows a block diagram of the Timer subsystem Power-on Reset and the STOP instruction cause the counter to be set to $FO

CDP6805E2, CDP6805E2C



NOTES:
1. Prescaler and 8-bit counter are clocked falling edge of the internal clock (AS) or external input.
2. Counter is written to during Data Strobe (DS) and counts down continuously.

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Fig. 19 - Timer block diagram.

Timer Control Register (TCR)

7	6	5	4	3	2	1	0
TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0

All bits in this register except bit 3 are Read/Write bits.

TCR7 – Timer interrupt request bit: bit used to indicate the timer interrupt when it is logic "1".

1 – Set whenever the counter decrements to zero, or under program control.

0 – Cleared on external reset, power-on reset, STOP instruction, or program control.

TCR6 – Timer interrupt mask bit: when this bit is a logic "1" it inhibits the timer interrupt to the processor.

1 – Set on external reset, power-on reset, STOP instruction, or program control.

0 – Cleared under program control.

TCR5 – External or internal bit: selects the input clock source to be either the external timer pin or the internal clock. (Unaffected by $\overline{\text{RESET}}$.)

1 – Select external clock source

0 – Select internal clock source (AS).

TCR4 – External enable bit: control bit used to enable the external timer pin. (Unaffected by $\overline{\text{RESET}}$.)

1 – Enable external timer pin.

0 – Disable external timer pin.

TCR5	TCR4	
0	0	Internal clock (AS) to Timer
0	1	AND of internal clock (AS) and TIMER pin to Timer
1	0	Inputs to Timer disabled
1	1	TIMER pin to Timer

Refer to Figure 19 for Logic Representation.

TCR3 – Timer Prescaler Reset bit: writing a "1" to this bit resets the prescaler to zero. A read of this location always indicates a "0" (Unaffected by $\overline{\text{RESET}}$.)

TCR2, TCR1, TCR0 – Prescaler address bits: decoded to select one of eight taps on the prescaler. (Unaffected by $\overline{\text{RESET}}$.)

Prescaler

TCR2	TCR1	TCR0	Result
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	÷128

INSTRUCTION SET

The MPU has a set of 61 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

REGISTER/MEMORY INSTRUCTIONS – Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 4.

READ/MODIFY/WRITE INSTRUCTIONS – These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read/modify/write sequence since it does not modify the value. Refer to Table 5.

BRANCH INSTRUCTIONS – This set of instructions branches if a particular condition is met, otherwise no operation is performed. Branch instructions are two byte instructions. Refer to Table 6.

BIT MANIPULATION INSTRUCTIONS – The MPU is capable of setting or clearing any bit which resides in the first 256 bytes of the memory space, where all port registers, port DDRs, timer, timer control, and on-chip RAM reside. An additional feature allows the software to test and branch on the state of any bit within these 256 locations. The bit set, bit clear and bit test and branch functions are all implemented with a single instruction. For the test and branch instructions the value of the bit tested is also placed in the carry bit of the Condition Code Register. Refer to Table 7 for instruction cycle timing.

CONTROL INSTRUCTIONS – These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 8 for instruction cycle timing.

ALPHABETICAL LISTING – The complete instruction set is given in alphabetical order in Table 9.

OPCODE MAP SUMMARY – Table 10 is an opcode map for the instructions used on the MCU.

ADDRESSING MODES

The MPU uses ten different addressing modes to give the programmer an opportunity to optimize the code to all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions, while the longest instructions (three bytes) permit tables throughout memory. Short and long absolute addressing is also included. Two byte direct addressing instructions access all data bytes in most applications Extended addressing permits jump instructions to reach all memory. Table 9 shows the addressing modes for each instruction, with the effects each instruction has on the Condition Code Register. An opcode map is shown in Table 10.

The term "Effective Address" or EA is used in describing the various addressing modes, which is defined as the address to or from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate "contents of," an arrow indicates "is replaced by" and a colon indicates concatenation of two bytes.

Inherent – In inherent instructions all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, and no other arguments, are included in this mode.

Immediate – In immediate addressing, the operand is contained in the byte immediately following the opcode. Immediate addressing is used to access constants which do not change during program execution (e g , a constant used to initialize a loop counter).

$$EA = PC + 1;\ PC \leftarrow PC + 2$$

Direct – In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two byte instruction. This includes all on-chip RAM and I/O registers and up to 128 bytes of off-chip ROM. Direct addressing is efficient in both memory and speed.

$$EA = (PC + 1);\ PC \leftarrow PC + 2$$
$$\text{Address Bus High} \leftarrow 0;\ \text{Address Bus Low} \leftarrow (PC + 1)$$

Extended – In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing modes are capable of referencing arguments anywhere in memory with a single three byte instruction.

$$EA = (PC + 1):(PC + 2);\ PC \leftarrow PC + 3$$
$$\text{Address Bus High} \leftarrow (PC + 1);\ \text{Address Bus Low} \leftarrow (PC + 2)$$

Indexed, No-Offset – In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is used to move a pointer through a table or to address a frequently referenced RAM or I/O location.

$$EA = X,\ PC \leftarrow PC + 1$$
$$\text{Address Bus High} \leftarrow 0;\ \text{Address Bus Low} \leftarrow X$$

TABLE 4 — REGISTER/MEMORY INSTRUCTIONS

		Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from Memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in Memory	STA	—	—	—	B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in Memory	STX	—	—	—	BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add Memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add Memory and Carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract Memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND Memory to A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR Memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump Unconditional	JMP	—	—	—	BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to Subroutine	JSR	—	—	—	BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

TABLE 5 — READ/MODIFY/WRITE INSTRUCTIONS

		Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (2's Complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate Left Thru Carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate Right Thru Carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical Shift Left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical Shift Right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic Shift Right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for Negative or Zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5

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TABLE 6 — BRANCH INSTRUCTIONS

Function	Mnemonic	Relative Addressing Mode Op Code	 # Bytes	 # Cycles
Branch Always	BRA	20	2	3
Branch Never	BRN	21	2	3
Branch IFF Higher	BHI	22	2	3
Branch IFF Lower or Same	BLS	23	2	3
Branch IFF Carry Clear	BCC	24	2	3
(Branch IFF Higher or Same)	(BHS)	24	2	3
Branch IFF Carry Set	BCS	25	2	3
(Branch IFF Lower)	(BLO)	25	2	3
Branch IFF Not Equal	BNE	26	2	3
Branch IFF Equal	BEQ	27	2	3
Branch IFF Half Carry Clear	BHCC	28	2	3
Branch IFF Half Carry Set	BHCS	29	2	3
Branch IFF Plus	BPL	2A	2	3
Branch IFF Minus	BMI	2B	2	3
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	3
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	3
Branch IFF Interrupt Line is Low	BIL	2E	2	3
Branch IFF Interrupt Line is High	BIH	2F	2	3
Branch to Subroutine	BSR	AD	2	6

TABLE 7 — BIT MANIPULATION INSTRUCTIONS

<table>
<tr><th rowspan="3">Function</th><th rowspan="3">Mnemonic</th><th colspan="6">Addressing Modes</th></tr>
<tr><th colspan="3">Bit Set/Clear</th><th colspan="3">Bit Test and Branch</th></tr>
<tr><th>Op Code</th><th># Bytes</th><th># Cycles</th><th>Op Code</th><th># Bytes</th><th># Cycles</th></tr>
<tr><td>Branch IFF Bit n is Set</td><td>BRSET n (n=0 .7)</td><td>–</td><td>–</td><td>–</td><td>2•n</td><td>3</td><td>5</td></tr>
<tr><td>Branch IFF Bit n is Clear</td><td>BRCLR n (n=0 7)</td><td>–</td><td>–</td><td>–</td><td>01+2•n</td><td>3</td><td>5</td></tr>
<tr><td>Set Bit n</td><td>BSET n (n=0 .7)</td><td>10+2•n</td><td>2</td><td>5</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>Clear Bit n</td><td>BCLR n (n=0 7)</td><td>11+2•n</td><td>2</td><td>5</td><td>–</td><td>–</td><td>–</td></tr>
</table>

TABLE 8 — CONTROL INSTRUCTIONS

Function	Mnemonic	Inherent Op Code	 # Bytes	 # Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	10
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

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TABLE 9 - INSTRUCTION SET

	Addressing Modes										Condition Codes				
Mnemonic	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/ Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
ADD		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
AND		X	X	X		X	X	X			●	●	Λ	Λ	●
ASL	X		X			X	X				●	●	Λ	Λ	Λ
ASR	X		X			X	X				●	●	Λ	Λ	Λ
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	Λ	Λ	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	Λ
BRSET										X	●	●	●	●	Λ
BSET									X		●	●	●	●	●
BSR					X						●	●	●	●	●
CLC	X										●	●	●	●	0
CLI	X										●	0	●	●	●
CLR	X		X			X	X				●	●	0	1	●
CMP		X	X	X		X	X	X			●	●	Λ	Λ	Λ
COM	X		X			X	X				●	●	Λ	Λ	1
CPX		X	X	X		X	X	X			●	●	Λ	Λ	Λ
DEC	X		X			X	X				●	●	Λ	Λ	●
EOR		X	X	X		X	X	X			●	●	Λ	Λ	●
INC	X		X			X	X				●	●	Λ	Λ	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	Λ	Λ	●
LDX		X	X	X		X	X	X			●	●	Λ	Λ	●
LSL	X		X			X	X				●	●	Λ	Λ	Λ
LSR	X		X			X	X				●	●	0	Λ	Λ
NEG	X		X			X	X				●	●	Λ	Λ	Λ
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	Λ	Λ	●
ROL	X		X			X	X				●	●	Λ	Λ	Λ
ROR	X		X			X	X				●	●	Λ	Λ	Λ
RSP	X										●	●	●	●	●
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	Λ	Λ	●
STOP	X										●	0	●	●	●
STX			X	X		X	X	X			●	●	Λ	Λ	●
SUB		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	Λ	Λ	●
TXA	X										●	●	●	●	●
WAIT	X										●	0	●	●	●

Condition Code Symbols

H	Half Carry (From Bit 3)	Λ	Test and Set if True Cleared Otherwise
I	Interrupt Mask	●	Not Affected
N	Negative (Sign Bit)	?	Load CC Register From Stack
Z	Zero	0	Cleared
C	Carry/Borrow	1	Set

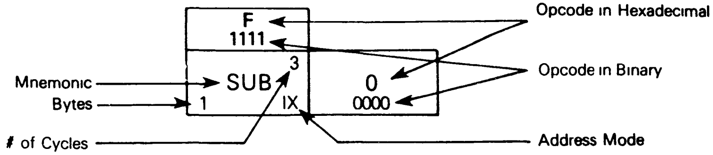
TABLE 10 — CDP6805E2 INSTRUCTION SET OPCODE MAP

	Bit Manipulation		Branch	Read/Modify/Write					Control		Register/Memory						
	BTB	BSC	REL	DIR	INH(A)	INH(X)	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
Hi / Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Hi / Low
0 0000	5 BRSET0 3 BTB	5 BSET0 2 BSC	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH	3 NEGX 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0 0000
1 0001	5 BRCLR0 3 BTB	5 BCLR0 2 BSC	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1 0001
2 0010	5 BRSET1 3 BTB	5 BSET1 2 BSC	3 BHI 2 REL								2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2 0010
3 0011	5 BRCLR1 3 BTB	5 BCLR1 2 BSC	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3 0011
4 0100	5 BRSET2 3 BTB	5 BSET2 2 BSC	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4 0100
5 0101	5 BRCLR2 3 BTB	5 BCLR2 2 BSC	3 BCS 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5 0101
6 0110	5 BRSET3 3 BTB	5 BSET3 2 BSC	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6 0110
7 0111	5 BRCLR3 3 BTB	5 BCLR3 2 BSC	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7 0111
8 1000	5 BRSET4 3 BTB	5 BSET4 2 BSC	3 BHCC 2 REL	5 LSL 2 DIR	3 LSLA 1 INH	3 LSLX 1 INH	6 LSL 2 IX1	5 LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8 1000
9 1001	5 BRCLR4 3 BTB	5 BCLR4 2 BSC	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9 1001
A 1010	5 BRSET5 3 BTB	5 BSET5 2 BSC	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A 1010
B 1011	5 BRCLR5 3 BTB	5 BCLR5 2 BSC	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B 1011
C 1100	5 BRSET6 3 BTB	5 BSET6 2 BSC	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C 1100
D 1101	5 BRCLR6 3 BTB	5 BCLR6 2 BSC	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D 1101
E 1110	5 BRSET7 3 BTB	5 BSET7 2 BSC	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E 1110
F 1111	5 BRCLR7 3 BTB	5 BCLR7 2 BSC	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F 1111

Abbreviations for Address Modes

INH	Inherent
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
BTB	Bit Test and Branch
IX	Indexed (No Offset)
IX1	Indexed, 1 Byte (8-Bit) Offset
IX2	Indexed, 2 Byte (16-Bit) Offset
*	CMOS Versions Only

LEGEND



Indexed, 8-bit Offset – Here the EA is obtained by adding the contents of the byte following the opcode to that of the index register The operand is therefore located anywhere within the lowest 511 memory locations For example, this mode of addressing is useful for selecting the m-th element in an n element table All instructions are two bytes The contents of the index register (X) is not changed The contents of (PC + 1) is an unsigned 8-bit integer One byte offset indexing permits look-up tables to be easily accessed in either RAM or ROM

$$EA = X + (PC + 1),\ PC \leftarrow PC + 2$$

$$\text{Address Bus High} \leftarrow K;\ \text{Address Bus Low} \leftarrow X + (PC + 1)$$

$$\text{Where: } K = \text{The carry from the addition of } X + (PC + 1)$$

Indexed, 16-Bit Offset – In the indexed, 16-bit offset addressing mode the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed 8-bit offset, except that this three byte instruction allows tables to be anywhere in memory (e g , jump tables in ROM) The content of the index register is not changed.

$$EA = X + [(PC + 1)\ (PC + 2)],\ PC \leftarrow PC + 3$$

$$\text{Address Bus High} \leftarrow (PC + 1) + K,$$

$$\text{Address Bus Low} \leftarrow X + (PC + 2)$$

$$\text{Where } K = \text{The carry from the addition of } X + (PC + 2)$$

Relative – Relative addressing is only used in branch instructions In relative addressing the contents of the 8-bit signed byte following the opcode (the offset) is added to the PC if and only if the branch condition is true Otherwise, control proceeds to the next instruction The span of relative addressing is limited to the range of – 126 to + 129 bytes from the branch instruction opcode location

$$EA = PC + 2 + (PC + 1);\ PC \leftarrow EA \text{ if branch taken;}$$

$$\text{otherwise } PC \leftarrow PC + 2$$

Bit Set/Clear – Direct addressing and bit addressing are combined in instructions which set and clear individual memory and I/O bits. In the bit set and clear instructions, the byte is specified as a direct address in the location following the opcode The first 256 addressable locations are thus accessed The bit to be modified within that byte is specified with three bits of the opcode. The bit set and clear instructions occupy two bytes, one for the opcode (including the bit number) and the second to address the byte which contains the bit of interest.

$$EA = (PC + 1),\ PC \leftarrow PC + 2$$

$$\text{Address Bus High} \leftarrow 0,\ \text{Address Bus Low} \leftarrow (PC + 1)$$

Bit Test and Branch – Bit test and branch is a combination of direct addressing, bit addressing and relative addressing The bit address and condition (set or clear) to be tested is part of the opcode The address of the byte to be tested is in the single byte immediately following the opcode byte (EA1) The signed relative 8-bit offset is in the third byte (EA2) and is added to the PC if the specified bit is set or clear in the specified memory location. This single three byte instruction allows the program to branch based on the condition of any bit in the first 256 locations of memory.

$$EA1 = (PC + 1)$$

$$\text{Address Bus High} \leftarrow 0;\ \text{Address Bus Low} \leftarrow (PC + 1)$$

$$EA2 = PC + 3 + (PC + 2);\ PC \leftarrow EA2 \text{ if branch taken;}$$

$$\text{otherwise } PC \leftarrow PC + 3$$

SYSTEM CONFIGURATION

Figures 20 through 25 show in general terms how the CDP6805E2 bus structure may be utilized. Specified interface details vary with the various peripheral and memory devices employed.

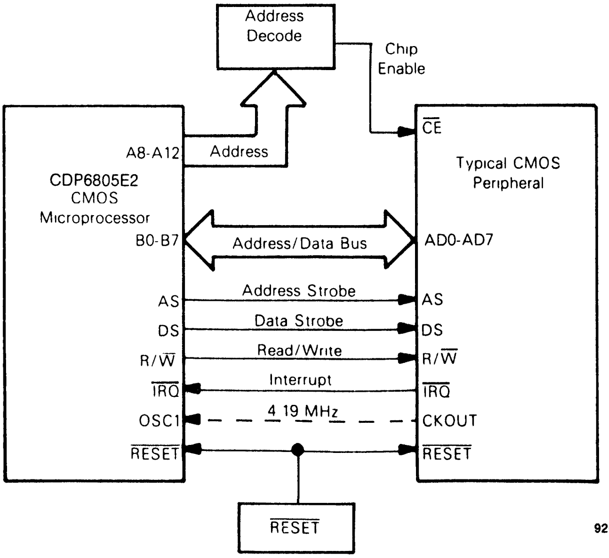


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Fig. 20 - Connection to CMOS peripherals.

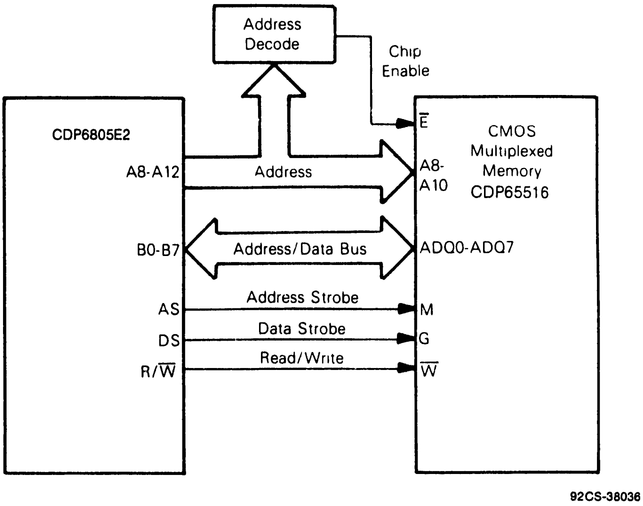
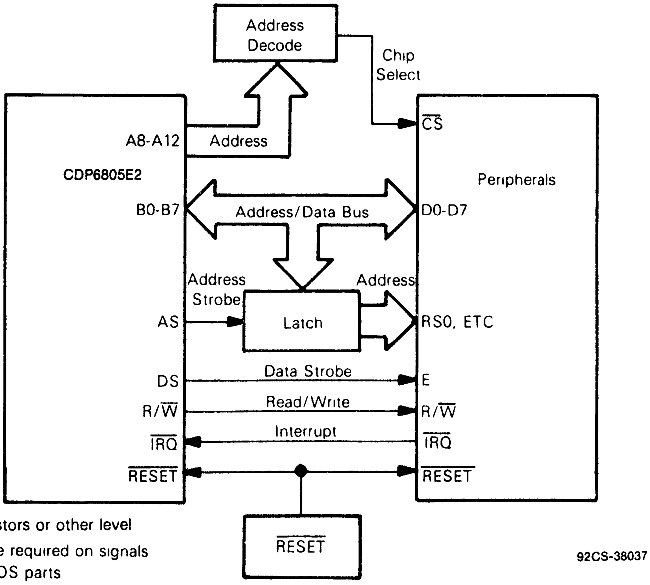


Fig. 21 - Connection to CMOS multiplexed memories.



NOTE In some cases, pullup resistors or other level shifting techniques may be required on signals going from NMOS to CMOS parts

Fig. 22 - Connection to peripherals.

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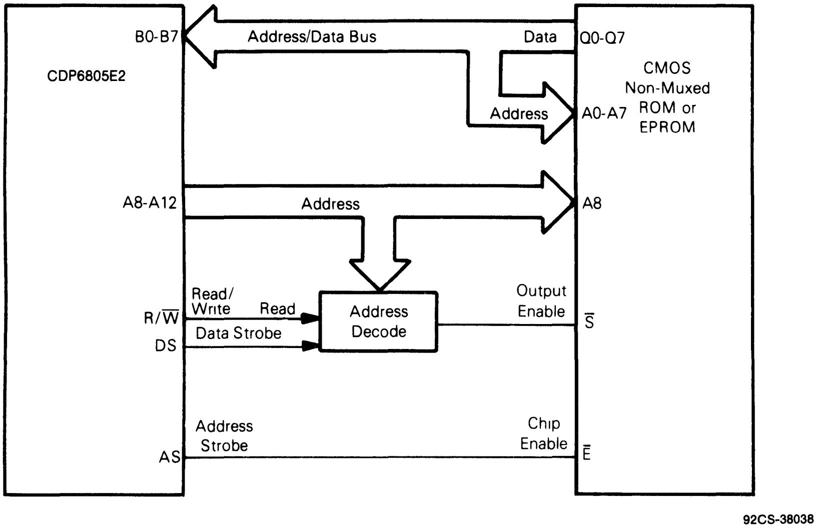

Fig. 23 - Connection to latch non-multiplexed CMOS ROM or EPROM.

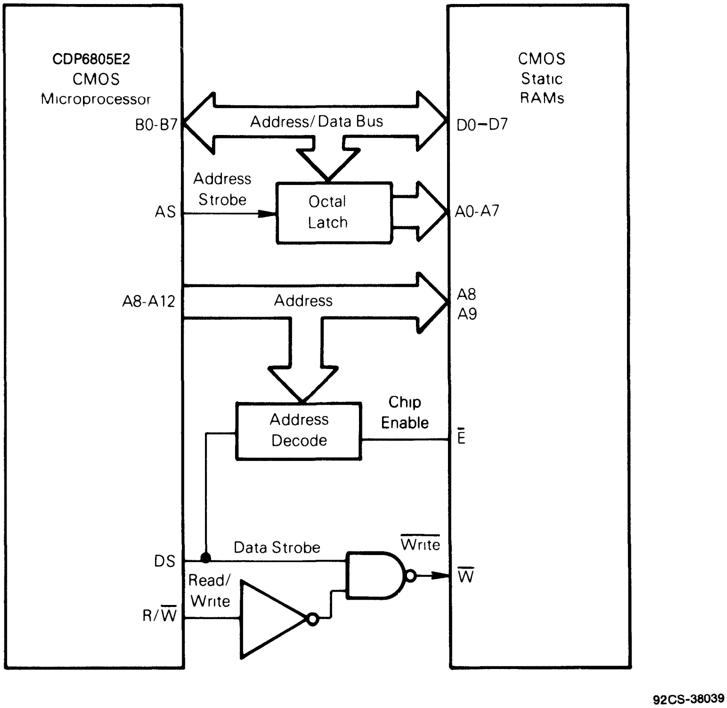

Fig. 24 - Connection to static CMOS RAMs.

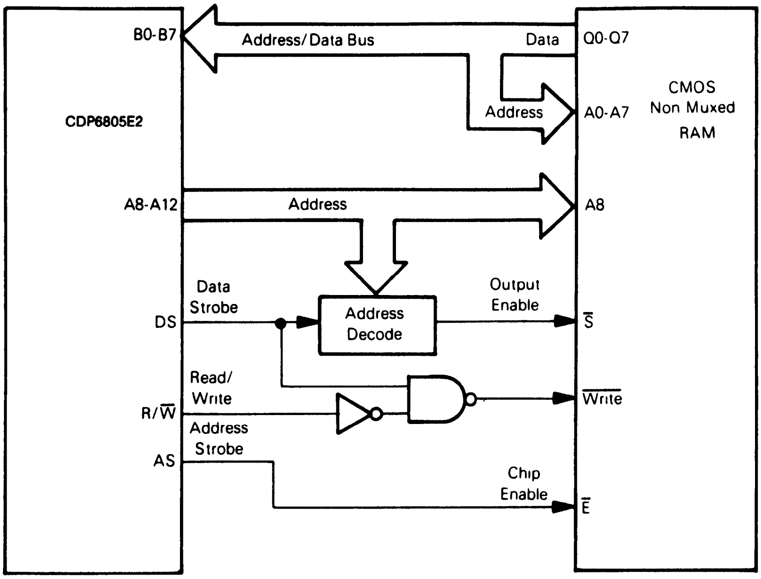

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Fig. 25 - Connection to latched non-multiplexed CMOS RAM.

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Table 11 provides a detailed description of the information present on the Bus, the Read/Write (R/$\overline{W}$) pin and the Load Instruction (LI) pin during each cycle for each instruction.

This information is useful in comparing actual with expected results during debug of both software and hardware as the control program is executed. The information is categorized in groups according to addressing mode and number of cycles per instruction.

TABLE 11 — SUMMARY OF CYCLE BY CYCLE OPERATION

Address Mode Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$ Pin	LI Pin	Data Bus
Inherent						
LSR LSL ASR NEG CLR ROL COM ROR DEC INC TST	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address +1	1	0	Op Code Next Instruction
		3	Op Code Address +1	1	0	Op Code Next Instruction
TAX CLC SEC STOP CLI SEI RSP WAIT NOP TXA	2	1	Op Code Address	1	1	Op Code
		2	Op Code Address +1	1	0	Op Code Next Instruction
RTS	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address +1	1	0	Op Code Next Instruction
		3	Stack Pointer	1	0	Irrelevant Data
		4	Stack Pointer +1	1	0	Irrelevant Data
		5	Stack Pointer +2	1	0	Irrelevant Data
		6	New Op Code Address	1	0	New Op Code
SWI	10	1	Op Code Address	1	1	Op Code
		2	Op Code Address +1	1	0	Op Code Next Instruction
		3	Stack Pointer	0	0	Return Address (LO Byte)
		4	Stack Pointer −1	0	0	Return Address (HI Byte)
		5	Stack Pointer −2	0	0	Contents of Index Register
		6	Stack Pointer −3	0	0	Contents of Accumulator
		7	Stack Pointer −4	0	0	Contents of CC Register
		8	Vector Address 1FFC (Hex)	1	0	Address of Int Routine (HI Byte)
		9	Vector Address 1FFD (Hex)	1	0	Address of Int. Routine (LO Byte)
		10	Interrupt Routine Starting Address	1	0	Interrupt Routine First Opcode
RTI	9	1	Op Code Address	1	1	Op Code
		2	Op Code Address +1	1	0	Op Code Next Instruction
		3	Stack Pointer	1	0	Irrelevant Data
		4	Stack Pointer +1	1	0	Irrelevant Data
		5	Stack Pointer +2	1	0	Irrelevant Data
		6	Stack Pointer +3	1	0	Irrelevant Data
		7	Stack Pointer +4	1	0	Irrelevant Data
		8	Stack Pointer +5	1	0	Irrelevant Data
		9	New Op Code Address	1	0	New Op Code
Immediate						
ADC EOR CPX ADD LDA LDX AND ORA BIT SBC CMB SUB	2	1	Op Code Address	1	1	Op Code
		2	Op Code Address +1	1	0	Operand Data
Bit Set/Clear						
BSET n BCLR n	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address +1	1	0	Address of Operand
		3	Address of Operand	1	0	Operand Data
		4	Address of Operand	1	0	Operand Data
		5	Address of Operand	0	0	Manipulated Data
Bit Test and Branch						
BRSET n BRCLR n	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address +1	1	0	Address of Operand
		3	Address of Operand	1	0	Operand Data
		4	Op Code Address +2	1	0	Branch Offset
		5	Op Code Address +2	1	0	Branch Offset
Relative						
BCC BHI BNE BEQ BCS BPL BHCC BLS BIL BMC BRN BHCS BIH BMI BMS BRA	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address +1	1	0	Branch Offset
		3	Op Code Address +1	1	0	Branch Offset
BSR	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address +1	1	0	Branch Offset
		3	Op Code Address +1	1	0	Branch Offset
		4	Subroutine Starting Address	1	0	First Subroutine Op Code
		5	Stack Pointer	0	0	Return Address (LO Byte)
		6	Stack Pointer −1	0	0	Return Address (HI Byte)

TABLE 11 — SUMMARY OF CYCLE BY CYCLE OPERATION (CONTINUED)

Address Mode Instructions	Cycles	Cycles #	Address Bus	R/$\overline{W}$ Pin	LI Pin	Data Bus
Direct						
JMP	2	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Jump Address
ADC EOR CPX ADD LDA LDX AND ORA BIT SBC CMP SUB	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Address of Operand	1	0	Operand Data
TST	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Address of Operand	1	0	Operand Data
		4	Op Code Address + 2	1	0	Op Code Next Instruction
STA STX	4	1	Op Code Address	1	1	Op Code
		2	Op Code Adrress + 1	1	0	Address of Operand
		3	Op Code Address + 1	1	0	Address of Operand
		4	Address of Operand	0	0	Operand Data
LSL LSR DEC ASR NEG INC CLR ROL COM ROR	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Operand Address	1	0	Current Operand Data
		4	Operand Address	1	0	Current Operand Data
		5	Operand Address	0	0	New Operand Data
JSR	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Subroutine Address (LO Byte)
		3	Subroutine Starting Address	1	0	1st Subroutine Op Code
		4	Stack Pointer	0	0	Return Address (LO Byte)
		5	Stack Pointer − 1	0	0	Return Address (HI Byte)
Extended						
JMP	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Jump Address (HI Byte)
		3	Op Code Address + 2	1	0	Jump Address (LO Byte)
ADC BIT ORA ADD CMP LDX AND EOR SBC CPX LDA SUB	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address Operand (HI Byte)
		3	Op Code Address + 2	1	0	Address Operand (LO Byte)
		4	Address of Operand	1	0	Operand Data
STA STX	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand (HI Byte)
		3	Op Code Address + 2	1	0	Address of Operand (LO Byte)
		4	Op Code Address + 2	1	0	Address of Operand (LO Byte)
		5	Address of Operand	0	0	Operand Data
JSR	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Subroutine (HI Byte)
		3	Op Code Address + 2	1	0	Address of Subroutine (LO Byte)
		4	Subroutine Starting Address	1	0	1st Subroutine Op Code
		5	Stack Pointer	0	0	Return Address (LO Byte)
		6	Stack Pointer − 1	0	0	Return Address (HI Byte)
Indexed, No-Offset						
JMP	2	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
ADC EOR CPX ADD LDA LDX AND ORA BIT SBC CMP SUB	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Index Register	1	0	Operand Data
TST	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Index Register	1	0	Operand Data
		4	Op Code Address + 1	1	0	Op Code Next Instruction
STA STX	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Op Code Address + 1	1	0	Op Code Next Instruction
		4	Index Register	0	0	Operand Data
LSL LSR DEC ASR NEG INC CLR ROL COM ROR	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Index Register	1	0	Current Operand Data
		4	Index Register	1	0	Current Operand Data
		5	Index Register	0	0	New Operand Data
JSR	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Index Register	1	0	1st Subroutine Op Code
		4	Stack Pointer	0	0	Return Address (LO Byte)
		5	Stack Pointer − 1	0	0	Return Address (HI Byte)

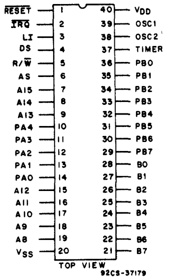
TABLE 11 — SUMMARY OF CYCLE BY CYCLE OPERATION (CONTINUED)

Address Mode Instructions	Cycles	Cycles #	Address Bus	$R/\overline{W}$ Pin	LI Pin	Data Bus
Indexed 8-Bit Offset						
JMP	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
ADC EOR CPX ADD LDA LDX AND ORA CMP SUB BIT SBC	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	Operand Data
STA STX	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Op Code Address + 1	1	0	Offset
		5	Index Register + Offset	0	0	Operand Data
TST	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	Operand Data
		5	Op Code Address + 2	1	0	Op Code Next Instruction
LSL LSR ASR NEG CLR ROL COM ROR DEC INC	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	Current Operand Data
		5	Index Register + Offset	1	0	Current Operand Data
		6	Index Register + Offset	0	0	New Operand Data
JSR	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	1st Subroutine Op Code
		5	Stack Pointer	0	0	Return Address LO Byte
		6	Stack Pointer − 1	0	0	Return Address HI Byte
Indexed, 16-Bit Offset						
JMP	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
ADC CMP SUB ADD EOR SBC AND ORA CPX LDA BIT LDX	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
		5	Index Register + Offset	1	0	Operand Data
STA STX	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
		5	Op Code Address + 2	1	0	Offset (LO Byte)
		6	Index Register + Offset	0	0	Operand Data
JSR	7	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
		5	Index Register + Offset	1	0	1st Subroutine Op Code
		6	Stack Pointer	0	0	Return Address (LO Byte)
		7	Stack Pointer − 1	0	0	Return Address (HO Byte)

TABLE 11 — SUMMARY OF CYCLE BY CYCLE OPERATION (CONTINUED)

Instructions	Cycles	Cycles #	Address Bus	$\overline{\text{RESET}}$ Pin	R/$\overline{\text{W}}$ Pin	LI Pin	Data Bus
Other Functions							
Hardware $\overline{\text{RESET}}$	5		$1FFE	0	1	0	Irrelevant Data
			$1FFE	0	1	0	Irrelevant Data
		1	$1FFE	1	1	0	Irrelevant Data
		2	$1FFE	1	1	0	Irrelevant Data
		3	$1FFE	1	1	0	Vector High
		4	$1FFF	1	1	0	Vector Low
		5	Reset Vector	1	1	0	Op Code
Power on Reset	1922	1	$1FFE	1	1	0	Irrelevant Data
		• • •	• • •	• • •	• • •	• • •	• • •
		1919	$1FFE	1	1	0	Irrelevant Data
		1920	$1FFE	1	1	0	Vector High
		1921	$1FFF	1	1	0	Vector Low
		1922	Reset Vector	1	1	0	Op Code
Instruction	**Cycles**	**Cycles #**	**Address Bus**	**$\overline{\text{IRQ}}$ Pin**	**R/$\overline{\text{W}}$ Pin**	**LI Pin**	**Data Bus**
$\overline{\text{IRQ}}$ Interrupt (Timer Vector $1FF8, $1FF9)	10		Last Cycle of Previous Instruction	0	X	0	X
		1	Next Op Code Address	0	1	0	Irrelevant Data
		2	Next Op Code Address	X	1	0	Irrelevant Data
		3	SP	X	0	0	Return Address (LO Byte)
		4	SP − 1	X	0	0	Return Address (HI Byte)
		5	SP − 2	X	0	0	Contents Index Reg
		6	SP − 3	X	0	0	Contents Accumulator
		7	SP − 4	X	0	0	Contents CC Register
		8	$1FFA	X	1	0	Vector High
		9	$1FFB	X	1	0	Vector Low
		10	$\overline{\text{IRQ}}$ Vector	X	1	0	Int Routine First

CDP6805E3, CDP6805E3C



TERMINAL ASSIGNMENT

CMOS 8-Bit Microprocessor

Hardware Features:

- *64K address space version of CMOS 6805E2*
- *Typical full speed operating power of 35 mW @ 5 V*
- *Typical WAIT mode power of 5 mW*
- *Typical STOP mode power of 25 μW*
- *112 bytes of on-chip RAM*
- *13 bidirectional I/O lines*
- *Internal 8-bit timer with software programmable 7-bit prescaler*
- *External timer input*
- *Full external and timer interrupts*
- *Multiplexed address/data bus*
- *Master reset and power-on reset*
- *Capable of addressing up to 64K bytes of external memory*
- *Single 3- to 6-volt supply*
- *On-chip oscillator*

Software Features:

- *Similar to the CDP6805E2, F2, and G2*
- *Efficient use of program space*
- *Versatile interrupt handling*
- *Memory mapped I/O*
- *True bit manipulation*
- *Addressing modes with indexed addressing for tables*
- *Efficient instruction set*
- *Two power savings standby modes*

The CDP6805E3 Microprocessor Unit (MPU) belongs to the CDP6805 Family of CMOS Microcomputers. This 8-bit fully static and expandable microprocessor contains a CPU, on-chip RAM, I/O, and Timer. It is a low-power, low-cost processor designed for mid-range applications in the consumer, automotive, industrial, and communications markets where very low power consumption constitutes an important factor. The major features of the CDP6805E3 are listed under "Hardware Features" and "Software Features".

The CDP6805E3 is supplied in a 40-lead hermetic dual-in-line ceramic package (D suffix), a 40-lead dual-in-line plastic package (E suffix), and a 44-lead plastic chip-carrier package (Q suffix).

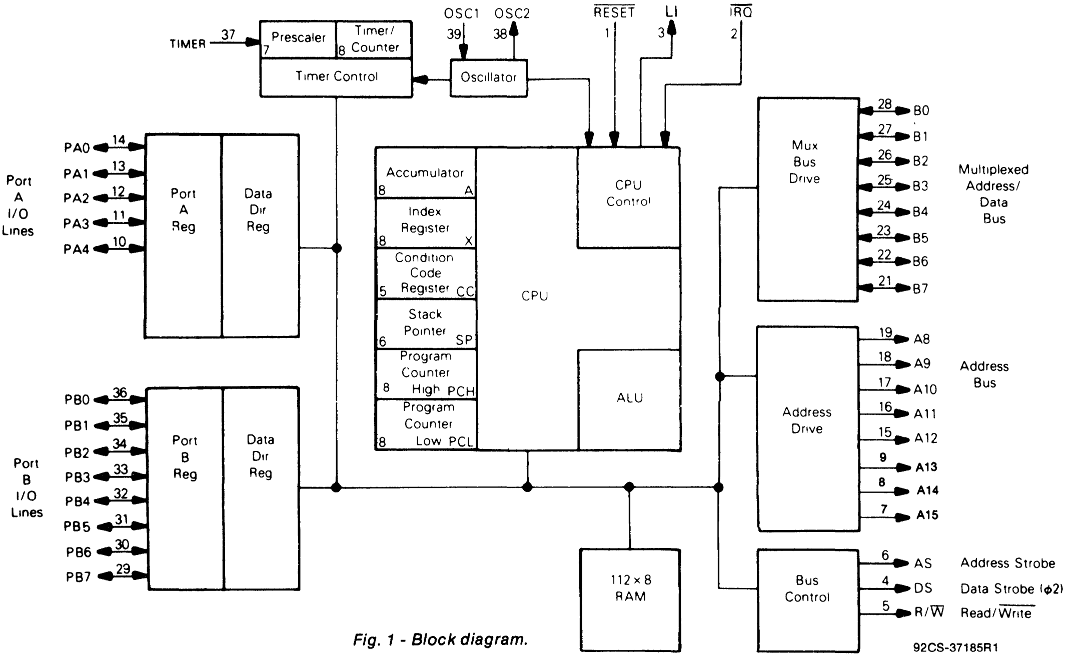


Fig. 1 - Block diagram.

File Number **1503**

MAXIMUM RATINGS (voltages referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0 3 to +8	V
All Input Voltages Except OSC1	V_{in}	V_{SS}−0 5 to V_{DD}+0.5	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range CDP6805E3 CDP6805E3C	T_A	T_L to T_H 0 to 70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

DC ELECTRICAL CHARACTERISTICS 3 V (V_{DD}=3 Vdc, V_{SS}=0, T_A=T_L to T_H, unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Output Voltage $I_{LOAD} \leq 10\,\mu A$	V_{OL} V_{OH}	– V_{DD}−0 1	0 1 –	V
Total Supply Current (C_L=50 pF – no DC loads) t_{cyc}=5 μs				
Run (V_{IL}=0 2 V, V_{IH}=V_{DD}−0 2 V)	I_{DD}	–	1 3	mA
Wait (Test Conditions – See Note Below)	I_{DD}	–	200	μA
Stop (Test Conditions – See Note Below)	I_{DD}	–	100	μA
Output High Voltage				
(I_{LOAD}=0 25 mA) A8-A15, B0-B7	V_{OH}	2 7	–	V
(I_{LOAD}=0 1 mA) PA0-PA4, PB0-PB7	V_{OH}	2 7	–	V
(I_{LOAD}=0 25 mA) DS, AS, R/$\overline{W}$	V_{OH}	2 7	–	V
Output Low Voltage				
(I_{LOAD}=0 25 mA) A8-A15, B0-B7	V_{OL}	–	0 3	V
(I_{LOAD}=0 25 mA) PA0-PA4, PB0-PB7	V_{OL}	–	0 3	V
(I_{LOAD}=0 25 mA) DS, AS, R/$\overline{W}$	V_{OL}	–	0 3	V
Input High Voltage				
PA0-PA4, PB0-PB7, B0-B7	V_{IH}	2 1	–	V
TIMER, $\overline{IRQ}$, $\overline{RESET}$	V_{IH}	2 5	–	V
OSC1	V_{IH}	2 1	–	V
Input Low Voltage (All inputs)	V_{IL}	–	0 5	V
Frequency of Operation				
Crystal	f_{OSC}	0 032	1	MHz
External Clock	f_{OSC}	DC	1	MHz
Input Current $\overline{RESET}$, $\overline{IRQ}$, Timer, OSC1	I_{in}	–	±1	μA
Three-State Output Leakage PA0-PA4, PB0-PB7, B0-B7	I_{TSL}	–	±10	μA
Capacitance $\overline{RESET}$, $\overline{IRQ}$, Timer	C_{in}	–	8	pF
Capacitance DS, AS, R/$\overline{W}$, A8-A15, PA0-PA4, PB0-PB7, B0-B7	C_{out}	–	12	pF

NOTE Test conditions for Quiescent Current Values are
Port A and B programmed as inputs
V_{IL}=0 2 V for PA0-PA4, PB0-PB7, and B0-B7
V_{IH}=V_{DD} – 0 2 V for $\overline{RESET}$, $\overline{IRQ}$, and Timer
OSC1 input is a squarewave from V_{SS}+0 2 V to V_{DD} – 0 2 V
OSC2 output load (including tester) is 35 pF maximum
Wait mode I_{DD} is affected linearly by this capacitance

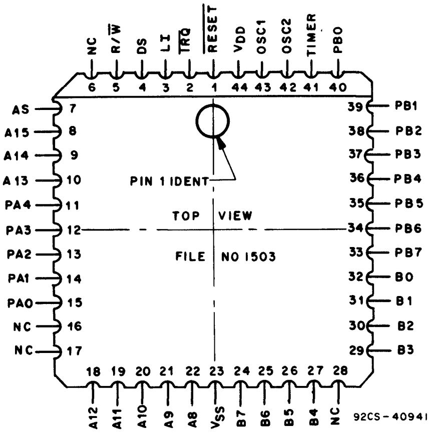
CDP6805E3, CDP6805E3C

DC ELECTRICAL CHARACTERISTICS 5 V (V_{DD}=5 Vdc ± 10%, V_{SS}=0, T_A=T_L to T_H, unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Output Voltage $I_{LOAD} \leq 10\,\mu A$	V_{OL} V_{OH}	– V_{DD} - 0.1	0.1 –	V V
Total Supply Current (C_L = 130 pF – On Bus, C_L = 50 pF – On Ports, No DC Loads, t_{cyc} = 1 μs Run (V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V)	I_{DD}	–	10	mA
Wait (Test Conditions – See Note Below)	I_{DD}	–	1.5	mA
Stop (Test Conditions – See Note Below)	I_{DD}	–	200	μA
Output High Voltage (I_{LOAD} = 1.6 mA) A8-A15, B0-B7	V_{OH}	4.1	–	V
(I_{LOAD} = 0.36 mA) PA0-PA4, PB0-PB7	V_{OH}	4.1	–	V
(I_{LOAD} = 1.6 mA) DS, AS, R/$\overline{W}$	V_{OH}	4.1	–	V
Output Low Voltage (I_{LOAD} = 1.6 mA) A8-A15, B0-B7	V_{OL}	–	0.4	V
(I_{LOAD} = 1.6 mA) PA0-PA4, PB0-PB7	V_{OL}	–	0.4	V
(I_{LOAD} = 1.6 mA) DS, AS, R/$\overline{W}$	V_{OL}	–	0.4	V
Input High Voltage **PA0-PA4, PB0-PB7, B0-B7**	V_{IH}	V_{DD} - 2	–	V
TIMER, $\overline{IRQ}$, $\overline{RESET}$	V_{IH}	V_{DD} - 0.8	–	V
OSC1	V_{IH}	V_{DD} - 1.5	–	V
Input Low Voltage (All Inputs)	V_{IL}	–	0.8	V
Frequency of Operation Crystal	f_{OSC}	0.032	5	MHz
External Clock	f_{OSC}	DC	5	MHz
Input Current $\overline{RESET}$, $\overline{IRQ}$, Timer, OSC1	I_{in}	–	± 1	μA
Three-State Output Leakage PA0-PA4, PB0-PB7, B0-B7	I_{TSI}	–	± 10	μA
Capacitance $\overline{RESET}$, $\overline{IRQ}$, Timer	C_{in}	–	8	pF
Capacitance DS, AS, R/$\overline{W}$, A8-A15, PA0-PA4, PB0-PB7, B0-B7	C_{out}	–	12	pF

NOTE Test conditions for Quiescent Current Values are
Port A and B programmed as inputs
V_{IL} = 0.2 V for PA0-PA4, PB0-PB7, and B0-B7
V_{IH} = V_{DD} – 0.2 V for $\overline{RESET}$, $\overline{IRQ}$, and Timer
OSC1 input is a squarewave from V_{SS} + 0.2 V to V_{DD} – 0.2 V
OSC2 output load (including tester) is 35 pF maximum
Wait mode (I_{DD}) is affected linearly by this capacitance

TERMINAL ASSIGNMENT



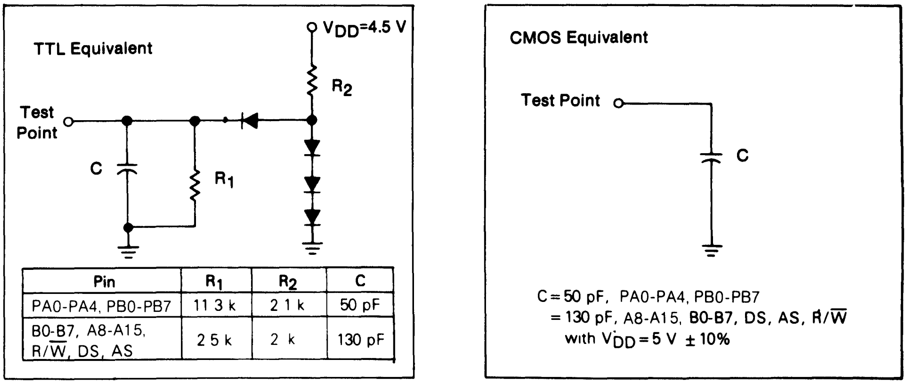
Plastic Chip-Carrier Package

CDP6805E3, CDP6805E3C

TABLE 1 – CONTROL TIMING (V_{SS}=0, T_A=T_L to T_H)

		V_{DD}=3 V f_{OSC}=1 MHz			V_{DD}=5 V) ± 10% f_{OSC}=5 MHz			
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I/O Port Timing – Input Setup Time (Figure 3)	t_{PVASL}	500	–	–	250	–	–	ns
Input Hold Time (Figure 3)	t_{ASLPX}	100	–	–	100	–	–	ns
Output Delay Time (Figure 3)	t_{ASLPV}	–	–	0	–	–	0	ns
Interrupt Setup Time (Figure 6)	t_{ILASL}	2	–	–	0.4	–	–	µs
Crystal Oscillator Startup Time (Figure 5)	t_{OXOV}	–	30	300	–	15	100	ms
Wait Recovery Startup Time (Figure 7)	t_{IVASH}	–	–	10	–	–	2	µs
Stop Recovery Startup Time (Crystal Oscillator) (Figure 8)	t_{ILASH}	–	30	300	–	15	100	ms
Required Interrupt Release (Figure 6)	t_{DSLIH}	–	–	5	–	–	1	µs
Timer Pulse Width (Figure 7)	t_{TH}, t_{TL}	0.5	–	–	0.5	–	–	t_{cyc}
Reset Pulse Width (Figure 5)	t_{RL}	5.2	–	–	1.05	–	–	µs
Timer Period (Figure 7)	t_{TLTL}	1	–	–	1	–	–	t_{cyc}
Interrupt Pulse Width Low (Figure 16)	t_{ILIH}	1	–	–	1	–	–	t_{cyc}
Interrupt Pulse Period (Figure 16)	t_{ILIL}	*	–	–	*	–	–	t_{cyc}
Oscillator Cycle Period (1/5 of t_{cyc})	t_{OLOL}	1000	–	–	200	–	–	ms
OSC1 Pulse Width High	t_{OH}	350	–	–	75	–	–	ns
OSC1 Pulse Width Low	t_{OL}	350	–	–	75	–	–	ns

*The minimum period t_{ILIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routine plus 20 t_{cyc} cycles

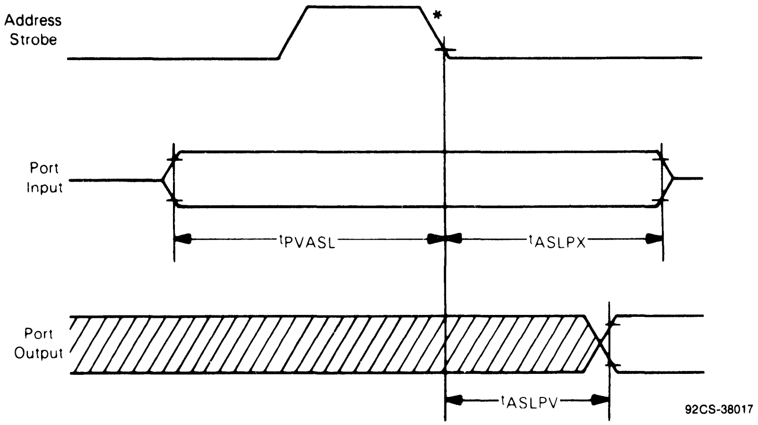


Pin	R_1	R_2	C
PA0-PA4, PB0-PB7	11.3 k	2.1 k	50 pF
B0-B7, A8-A15, R/$\overline{W}$, DS, AS	2.5 k	2 k	130 pF

C = 50 pF, PA0-PA4, PB0-PB7
= 130 pF, A8-A15, B0-B7, DS, AS, R/$\overline{W}$
with V_{DD} = 5 V ± 10%

Fig. 2 - Equivalent test-load circuits.

(V_{LOW}=0.8 V, V_{HIGH}=V_{DD}−2 V, V_{DD}=5 ±10%
Temp=0° to 70°C, C_L on Port=50 pF, f_{OSC}=5 MHz)

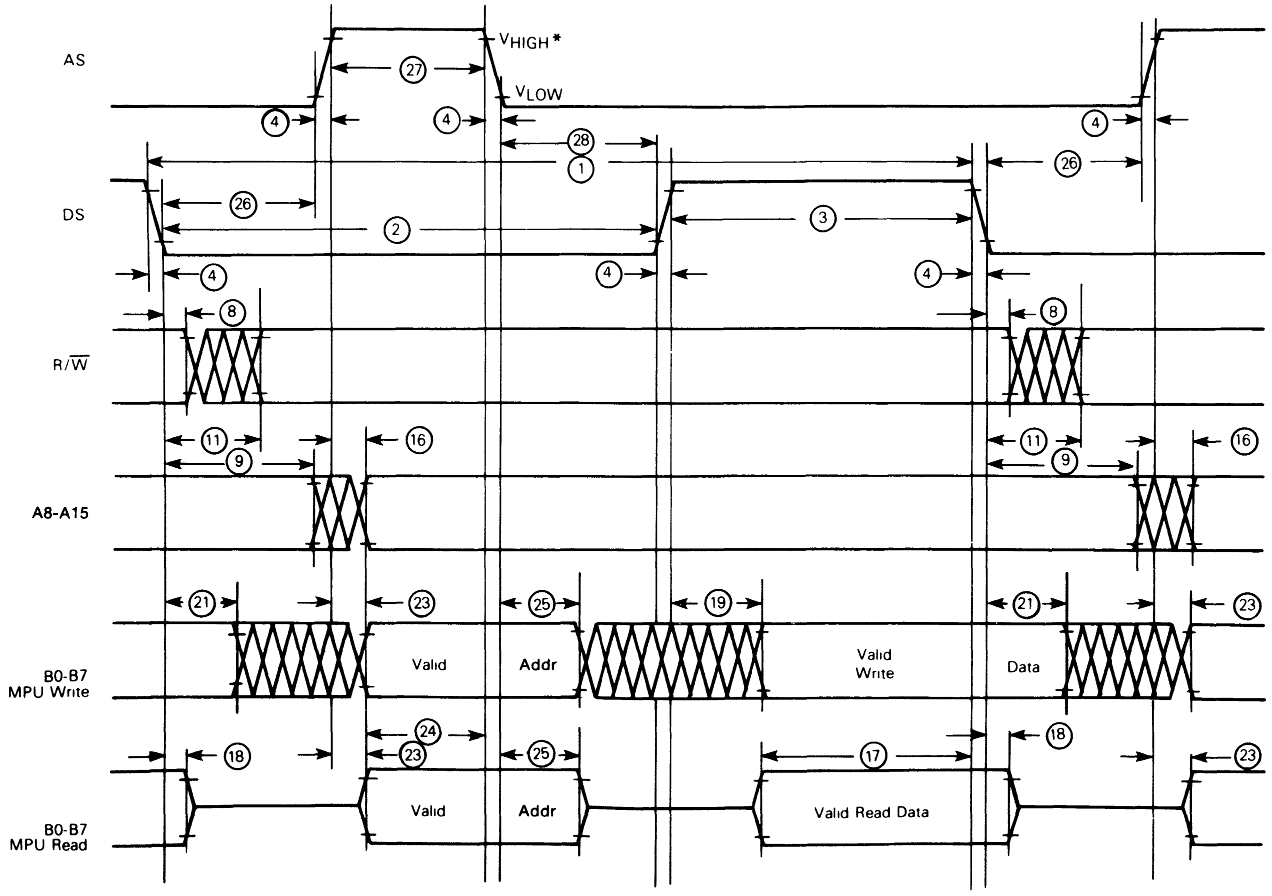


*The address strobe of the first cycle of the next instruction as shown in Table 11

Fig. 3 - I/O port timing waveforms.

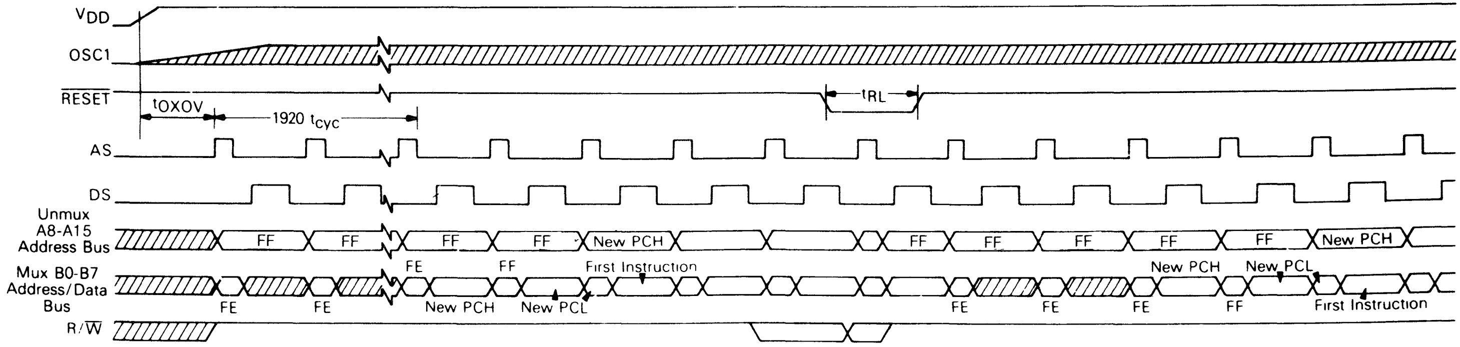
TABLE 2 — BUS TIMING (T_A=T_L to T_H, V_{SS}=0 V) See Figure 4

Num	Characteristics	Symbol	f_{OSC}=1 MHz, V_{DD}=3 V 50 pF Load		f_{OSC}=5 MHz V_{DD}=5 V ±10%, 1 TTL and 130 pF Load		Unit
			Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	5000	DC	1000	DC	ns
2	Pulse Width, $\overline{DS}$ Low	PW_{EL}	2800	–	560	–	ns
3	Pulse Width, DS High or $\overline{RD}$, $\overline{WR}$, Low	PW_{EH}	1800	–	375	–	ns
4	Clock Transition	t_r, t_f	–	100	–	30	ns
8	R/$\overline{W}$ Hold	t_{RWH}	10	–	10	–	ns
9	Non-Muxed Address Hold	t_{AH}	800	–	100	–	ns
11	R/$\overline{W}$ Delay from DS Fall	t_{AD}	–	500	–	300	ns
16	Non-Muxed Address Delay from AS Rise	t_{ADH}	0	200	0	100	ns
17	MPU Read Data Setup	t_{DSR}	200	–	115	–	ns
18	Read Data Hold	t_{DHR}	0	1000	0	160	ns
19	MPU Data Delay, Write	t_{DDW}	–	0	–	120	ns
21	Write Data Hold	t_{DHW}	800	–	55	–	ns
23	Muxed Address Delay from AS Rise	t_{BHD}	0	250	0	120	ns
24	Muxed Address Valid to AS Fall	t_{ASL}	600	–	55	–	ns
25	Muxed Address Hold	t_{AHL}	250	750	60	180	ns
26	Delay DS Fall to AS Rise	t_{ASD}	800	–	160	–	ns
27	Pulse Width, AS High	PW_{ASH}	850	–	175	–	ns
28	Delay, AS Fall to DS Rise	t_{ASED}	800	–	160	–	ns

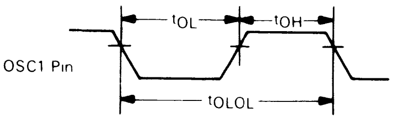


* V_{HIGH} = -2 V, V_{LOW} = 0.5 V for V_{DD} = 3 V
V_{HIGH} = V_{DD} -2 V, V_{LOW} = 0.8 V for V_{DD} = 5 V ± 10 %

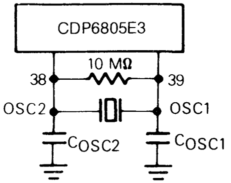
Fig. 4 - Bus timing waveforms.



Oscillator Waveform



Crystal Oscillator Connections



Crystal Parameters Representative Frequencies

	5 MHz	4 MHz	1 MHz
RS max	50Ω	75Ω	400Ω
C0	8 pF	7 pF	5 pF
C1	0.02 pF	0.012 pF	0.008 pF
Q	50 k	40 k	30 k
C_{OSC1}	15-30 pF	15-30 pF	15-40 pF
C_{OSC2}	15-25 pF	15-25 pF	15-30 pF

Crystal Circuit

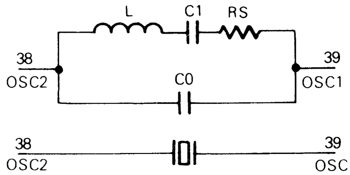


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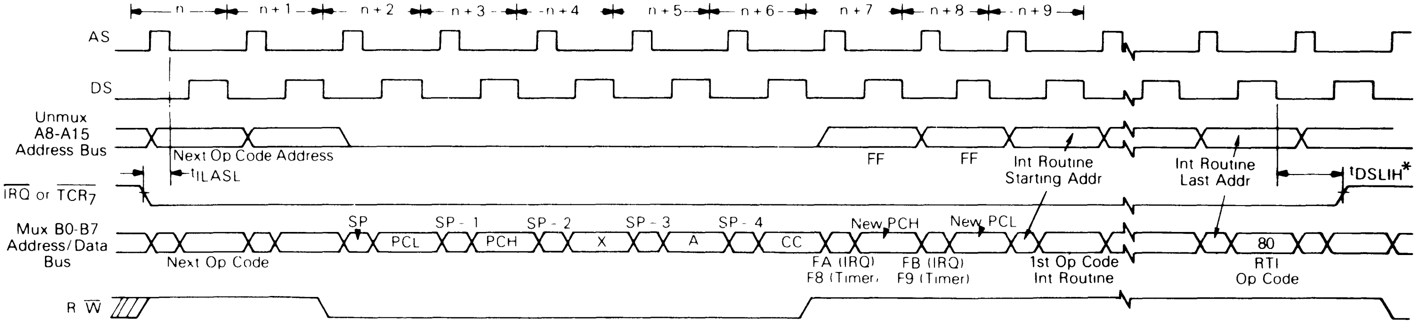
Fig. 5 – Power-on reset and $\overline{\text{reset}}$ timing waveforms.



*t_{DSLIH} The interrupting device must release the IRQ line within this time to prevent subsequent recognition of the same interrupt

Fig. 6 - $\overline{IRQ}$ and $\overline{TCR_7}$ interrupt timing waveforms.

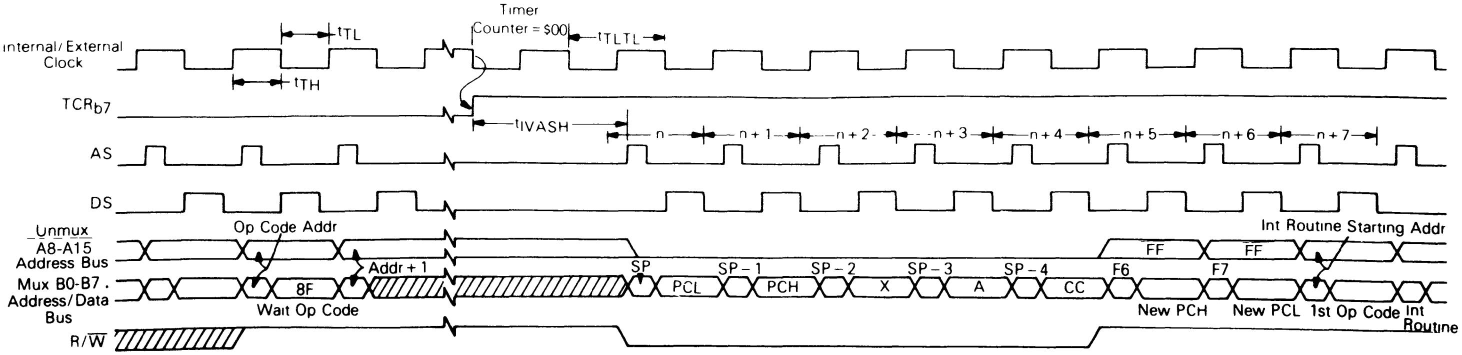
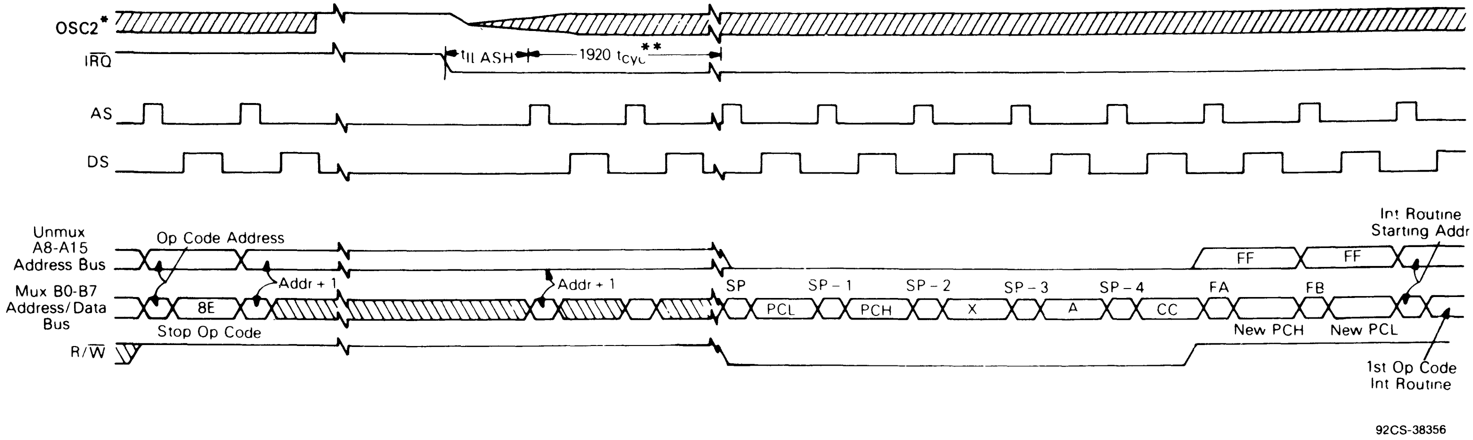


Fig. 7 - Timer interrupt after WAIT instruction timing waveforms.

3



*Represents the internal gating of the OSC1 input pin

**t_{cyc} is one instruction cycle (for $f_{OSC} = 5$ MHz, $t_{cyc} = 1$ µs)

Fig. 8 - Interrupt recovery from STOP instruction timing waveforms.

FUNCTIONAL PIN DESCRIPTION

V_{DD} and V_{SS} – V_{DD} and V_{SS} provide power to the chip V_{DD} provides power and V_{SS} is ground

$\overline{IRQ}$ (Maskable Interrupt Request) – $\overline{IRQ}$ is a level-sensitive and edge sensitive input which can be used to request an interrupt sequence The MPU completes the current instruction before it responds to the request IF $\overline{IRQ}$ is low and the interrupt mask bit (I-bit) in the Condition Code Register is clear, the MPU begins an interrupt sequence at the end of the current instruction The interrupt circuit recognizes both a "Wire ORed" level as well as pulses on the $\overline{IRQ}$ line (see Interrupt Section for more details) $\overline{IRQ}$ requires an external resistor to V_{DD} for "Wire OR" operation

$\overline{RESET}$ – The $\overline{RESET}$ input is not required for start-up but can be used to reset the MPU's internal state and provide an orderly software start-up procedure Refer to the RESET section for a detailed description

TIMER – The TIMER input is used for clocking the on-chip timer Refer to TIMER section for a detailed description

AS (Address Strobe) – Address Strobe (AS) is an output strobe used to indicate the presence of an address on the 8-bit multiplexed bus The AS line is used to demultiplex the eight least significant address bits from the data bus A latch controlled by Address Strobe should capture addresses on the negative edge This output is capable of driving one standard TTL load and 130 pF and is available at f_{OSC} – 5 when the MPU is not in the WAIT or STOP states

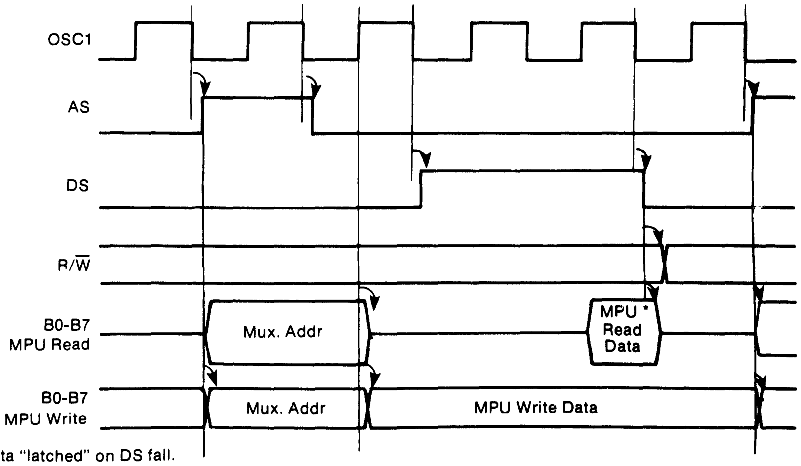
DS (Data Strobe) – This output is used to transfer data to or from a peripheral or memory DS occurs anytime the MPU does a data read or write DS also occurs when the MPU does a data transfer to or from the MPU's internal memory Refer to Table 2 and Figure 4 for timing characteristics This output is capable of driving one standard TTL load and 130 pF DS is a continuous signal at f_{OSC} ÷ 5 when the MPU is not in WAIT or STOP state. Some bus cycles are redundant reads of op code bytes

R/$\overline{W}$ (Read/Write) – The R/$\overline{W}$ output is used to indicate the direction of data transfer for both internal memory and I/O registers, and external peripheral devices and memories. This output is used to indicate to a selected peripheral whether the MPU is going to read or write data on the next Data Strobe (R/$\overline{W}$ low = processor write; R/$\overline{W}$ high = processor read) The R/$\overline{W}$ output is capable of driving one standard TTL load and 130 pF The normal standby state is Read (high)

A8-A15 (High Order Address Lines) — The A8-A15 output lines constitute the higher order non-multiplexed addresses Each output line is capable of driving one standard TTL load and 130 pF

B0-B7 (Address/Data Bus) – The B0-B7 bidirectional lines constitute the lower order addresses and data. These lines are multiplexed, with address present at Address Strobe time and data present at Data Strobe time. When in the data mode, these lines are bidirectional, transferring data to and from memory and peripheral devices as indicated by the R/$\overline{W}$ pin As outputs in either the data or address modes, these lines are capable of driving one standard TTL load and 130 pF

OSC1, OSC2 — The CDP6805E3 provides for two types of oscillator inputs — crystal circuit or external clock. The two oscillator pins are used to interface to a crystal circuit, as shown in Figure 5 If an external clock is used, it must be connected to OSC1 The input at these pins is divided by five to form the cycle rate seen on the AS and DS pins The frequency range is specified by f_{OSC} The OSC1 to bus transitions relationships are provided in Figure 9 for system designs using oscillators slower than 5 MHz



* Read data "latched" on DS fall.

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Fig. 9 - OSC1 to bus transitions timing waveforms.

CDP6805E3,. CDP6805E3C

Crystal – The circuit shown in Figure 5 is recommended when using a crystal The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{OSC} in the electrical characteristics table. An external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time

External Clock – An external clock should be applied to the OSC1 input with the OSC2 input not connected, as shown in Figure 10

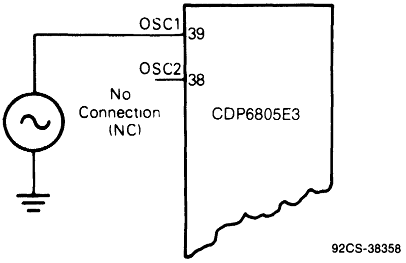
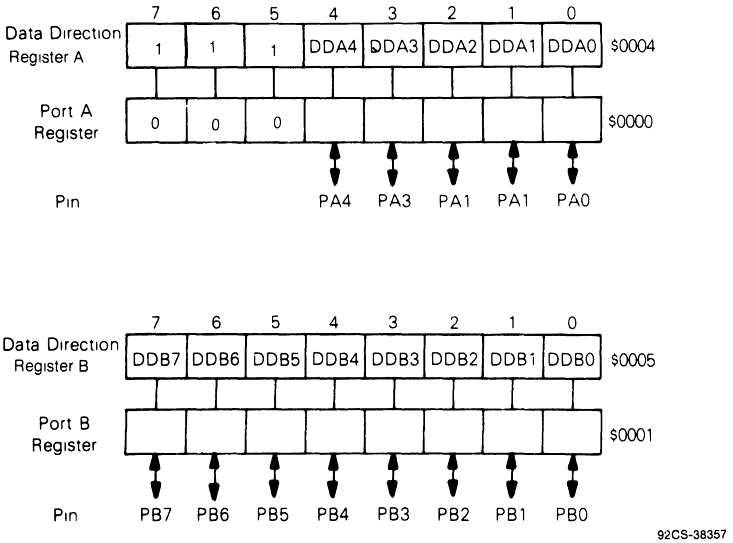


Fig. 10 - External clock connection.

LI (Load Instruction) – This output is used to indicate that a fetch of the next opcode is in progress LI remains low during an External or Timer interrupt The LI output is only used for certain debugging and test systems For normal operations this pin is not connected The LI output is capable of driving one standard TTL load and 50 pF This signal overlaps Data Strobe

PA0-PA4 — These five pins constitute Input/Output Port A. Each line is individually programmed to be either an input or output under software control via its Data Direction Register as shown below An I/O pin is programmed as an output when the corresponding DDR bit is set to a "1", and as an input when it is set to a "0" In the output mode the bits are latched and appear on the corresponding output pins An MPU read of the port bits programmed as outputs reflect the last value written to that location When programmed as an input, the input data bit(s) are not latched An MPU read of the port bits programmed as inputs reflects the current status of the corresponding input pins The Read/Write port timing is shown in Figure 3 See typical I/O Port Circuitry in Figure 11 During a Power-On Reset or external $\overline{\text{RESET}}$ all lines are configured as inputs (zero in Data Direction Register) The latched output data is not initialized by reset The TTL compatible three-state output buffers are capable of driving one standard TTL load and 50 pF. The DDR is a read/write register Bits 7-5 of the DDR "A" will be always read as "1" and bits 7-5 of the Port "A" Register will be read as "0"

PB0-PB7 – These eight pins interface to Input/Output Port B Refer to PA0-PA4 description for details of operation



	7	6	5	4	3	2	1	0	
Data Direction Register A	1	1	1	DDA4	DDA3	DDA2	DDA1	DDA0	$0004
Port A Register	0	0	0						$0000
Pin				PA4	PA3	PA1	PA1	PA0	

	7	6	5	4	3	2	1	0	
Data Direction Register B	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	$0005
Port B Register									$0001
Pin	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	

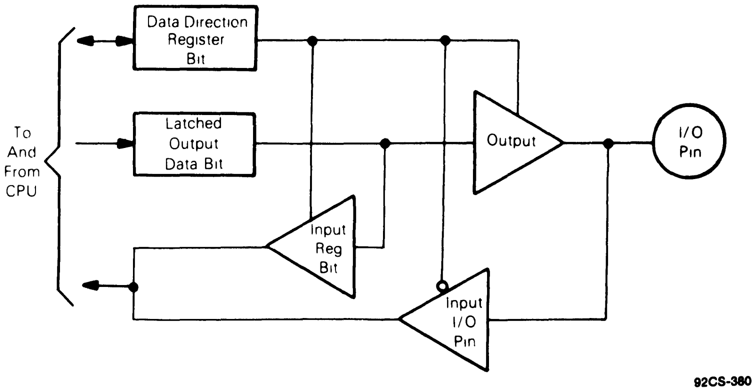


Fig. 11 - Typical I/O port circuitry.

TABLE 3 — I/O PIN FUNCTIONS

R/$\overline{W}$	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode Data is written into the output data latch
0	1	Data is written into the output data latch and output to the I/O pin
1	0	The state of the I/O pin is read
1	1	The I/O pin is in an output mode The output data latch is read

MEMORY ADDRESSING

The CDP6805E3 is capable of addressing 65536 bytes of memory and I/O registers The address space is divided into internal memory space and external memory space, as shown in Figure 12.

The internal memory space is located within the first 128 bytes of memory (first half of page zero) and is comprised of the I/O port locations, timer locations, and 112 bytes of RAM The MPU can read from or write to any of these locations A program write to on-chip locations is repeated on the external bus to permit off-chip memory to duplicate the content of on-chip memory Program reads to on-chip locations also appear on the external bus, but the MPU accepts data only from the addressed on-chip location Any read data appearing on the input bus is ignored

The stack pointer is used to address data stored on the stack Data is stored on the stack during interrupts and subroutine calls At power up, the stack pointer is set to $7F and it is decremented as data is pushed onto the stack When data is removed from the stack, the stack pointer is incremented A maximum of 64 bytes of RAM is available for stack usage Since most programs use only a small part of the allotted stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are usable for program data storage

All memory locations above location $007F are part of the external memory map In addition, ten locations in the I/O portion of the lower 128 bytes of memory space, as shown in Figure 12, are part of the external memory map. All of the external memory space is user definable except the highest 10 locations. Locations $FFF6 to $FFFF of the external address space are reserved for interrupt and reset vectors (see Figure 12).

REGISTERS

The CDP6805E3 contains five registers as shown in the programming model in Figure 13. The interrupt stacking order is shown in Figure 14.

ACCUMULATOR (A) — This Accumulator is an 8-bit general purpose register used for arithmetic calculations and data manipulations

INDEX REGISTER (X) — The X register is an 8-bit register which is used during the indexed modes of addressing. It provides an 8-bit operand which is used to create an effective address The index register is also used for data manipulations with the Read/Modify/Write type of instructions and as a temporary storage register when not performing addressing operations

PROGRAM COUNTER (PC) — The program counter is a 16-bit register that contains the address of the next instruction to be executed by the processor.

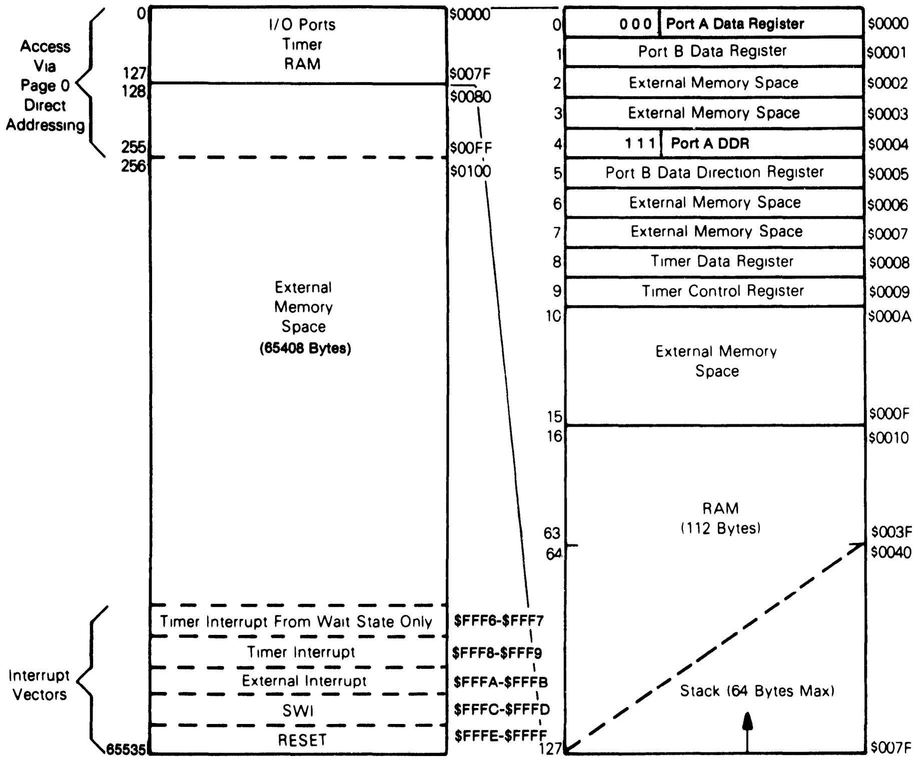


Fig. 12 - Address map.

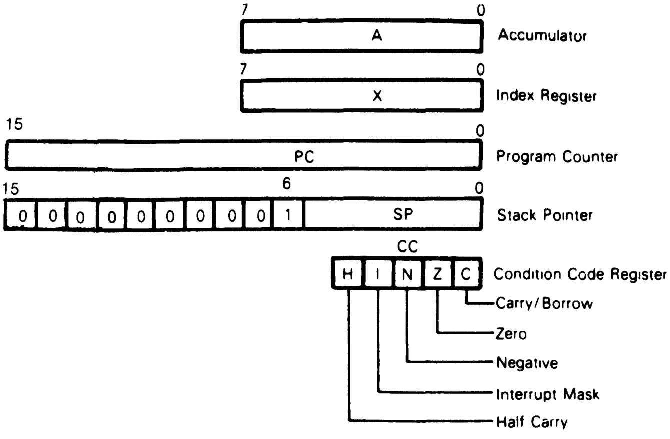
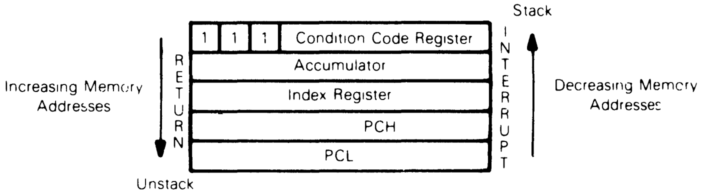


Fig. 13 - Programming model.


Stack
1 1 1 Condition Code Register
Accumulator
Index Register
PCH
PCL
RETURN
INTERRUPT
Increasing Memory Addresses
Decreasing Memory Addresses
Unstack
92CS-38361

NOTE Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc Pulling from the stack is in the reverse order

Fig. 14 - Stacking order.

STACK POINTER (SP) — The stack pointer is a 16-bit register containing the address of the next free location on the stack When accessing memory, the ten most-significant bits are permanently set to 000 000 0001 They are appended to the six least-significant register bits to produce an address within the range of $007F to $0040. The stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts During external or power-on reset, and during a "reset stack pointer" instruction, the stack pointer is set to its upper limit ($007F) Nested interrupts and/or subroutines may be use up to 64 (decimal) locations, beyond which the stack pointer "wraps around" and points to its upper limit thereby losing the previously stored information A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five bytes

CONDITION CODE REGISTER (CC) -- The condition code register is a 5-bit register in which each bit is used to indicate the results of the instruction just executed These bits can be individually tested by a program and specific action taken as a result of their state Each of the five bits is explained below

Half Carry Bit (H) – The H-bit is set to a one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction The H-bit is useful in Binary Coded Decimal addition subroutines.

Interrupt Mask Bit (I) – When the I-bit is set, both the external interrupt and the timer interrupt are disabled. Clearing this bit enables the above interrupts. If an interrupt occurs while the I-bit is set, the interrupt is latched and will be processed when the I-bit is next cleared.

Negative Bit (N) – When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (bit 7 in the result is a logical one).

Zero Bit (Z) – When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Carry Bit (C) – The C-bit is set when a carry or a borrow out of the ALU occurs during an arithmetic instruction The C-bit is also modified during bit test, shift, rotate, and branch types of instruction.

RESETS

The CDP6805E3 has two reset modes: an active low external reset pin ($\overline{\text{RESET}}$) and a Power-On Reset function, refer to Figure 5

$\overline{\text{RESET}}$ (Pin #1) – The $\overline{\text{RESET}}$ input pin is used to reset the MPU and provide an orderly software start-up procedure. When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one t_{cyc} The $\overline{\text{RESET}}$ pin is provided with a Schmitt Trigger to improve its noise immunity capability.

Power-On Reset – The Power-on Reset occurs when a positive transition is detected on V_{DD} The Power-on Reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage There is no provision for a power-down reset The power-on circuitry provides for a 1920 t_{cyc} delay from the time of the first oscillator operation. If the external reset pin is low at the end of the 1920 t_{cyc} time out, the processor remains in the reset condition.

Either of the two types of reset conditions causes the following to occur:

- Timer control register interrupt request bit (bit 7) is cleared to a "0"
- Timer control register interrupt mask bit (bit 6) is set to a "1".
- All data direction register bits are cleared to a "0" (inputs) - except Port "A" DDR Bits 7-5.
- Stack pointer is set to $007F
- The address bus is forced to the reset vector ($FFFE, $FFFF).
- Condition code register interrupt mask bit (I) is set to a "1".
- STOP and WAIT latches are reset
- External interrupt latch is reset

All other functions, such as other registers (including output ports) the timer, etc , are not cleared by the reset conditions.

INTERRUPTS

The CDP6805E3 is capable of operation with three different interrupts, two hardware (timer interrupt and external interrupt) and one software (SWI) When any of these interrupts occur, normal processing is suspended at the end of the current instruction execution All of the program registers (the machine state) are pushed onto the stack, refer to Figure 14 for stacking order The appropriate vector pointing to the starting address of the interrupt service routine is then fetched; refer to Figure 15 for the interrupt sequence

The priority of the various interrupts from highest to lowest is as follows

RESET→*→External Interrupt→Timer Interrupt

TIMER INTERRUPT – If the timer mask bit (TCR6) is cleared, then each time the timer decrements to zero (transitions from $01 to $00) an interrupt request is generated The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the I-bit in the condition code register is set. This masks further interrupts until the present one is serviced. The processor now vectors to the timer interrupt service routine. The address for this service routine is specified by the contents of $FFF8 and $FFF9. The contents of $FFF6 and $FFF7 specify the service routine if the processor is in the WAIT mode. Also, software must be used to clear the timer interrupt request bit (TCR7). At the end of the timer interrupt service routine, the software normally executes an RTI instruction which restores the machine state and starts executing the interrupted program.

EXTERNAL INTERRUPT – If the interrupt mask bit of the condition code register is cleared and the external interrupt pin $\overline{\text{IRQ}}$ is "low," then the external interrupt occurs The action of the external interrupt is identical to the timer interrupt with the exception that the service routine address is specified by the contents of $FFFA and $FFFB. The interrupt logic recognizes both a "wire ORed" level and pulses on the external interrupt line Figure 16 shows both a functional diagram and timing for the interrupt line The timing diagram shows two different treatments of the interrupt line ($\overline{\text{IRQ}}$) to the processor The first configuration shows many interrupt lines "wire ORed" to form the interrupts at the processor Thus, if after servicing an interrupt the $\overline{\text{IRQ}}$ remains low, then the next interrupt is recognized The second method is single pulses on the interrupt line spaced far enough apart to be service. The minimum time between pulses is a function of the length of the interrupt service routine. Once a pulse occurs, the next pulse should not occur until the MPU software has exited the routine (an RTI occurs). This time (t_{ILIL}) is obtained by adding 20 instruction cycles (one cycle $t_{cyc}=5/f_{OSC}$) to the total number of cycles it takes to complete the service routine including the RTI instruction; refer to Figure 6.

SOFTWARE INTERRUPT (SWI) – The software interrupt is an executable instruction The action of the SWI instruction is similar to the hardware interrupts The SWI is executed regardless of the state of the interrupt mask in the condition code register The service routine address is specified by the contents of memory locations $FFFC and $FFFD See Figure 15 for Interrupt and Instruction Processing Flowchart.

The following three functions are not strictly interrupts, however, they are tied very closely to the interrupts These functions are $\overline{\text{RESET}}$, STOP, WAIT

$\overline{\text{RESET}}$ – The $\overline{\text{RESET}}$ input pin and the internal Power-on Reset function each cause the program to vector to an initialization program This vector is specified by the contents of memory locations $FFFE and $FFFF The interrupt mask of the condition code register is also set. Refer to RESET selection for details

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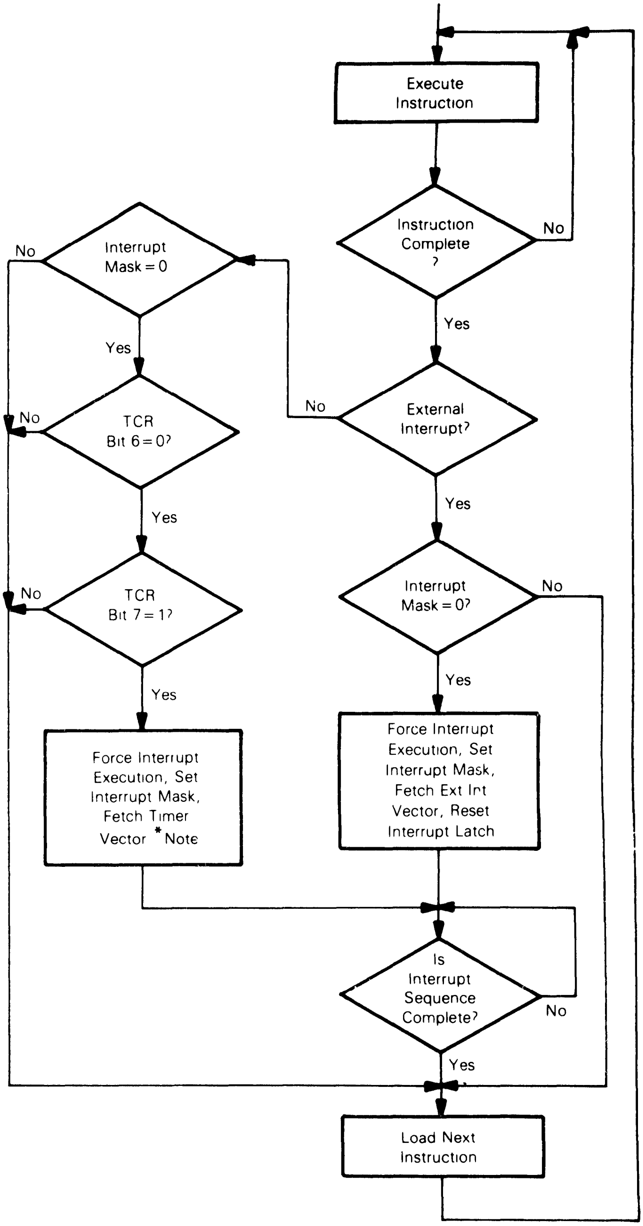
*Any current instruction including SWI


Execute Instruction
Instruction Complete ?
No
Yes
External Interrupt?
No
Yes
Interrupt Mask = 0?
No
Yes
Force Interrupt Execution, Set Interrupt Mask, Fetch Ext Int Vector, Reset Interrupt Latch
Interrupt Mask = 0
No
Yes
TCR Bit 6 = 0?
No
Yes
TCR Bit 7 = 1?
No
Yes
Force Interrupt Execution, Set Interrupt Mask, Fetch Timer Vector *Note
Is Interrupt Sequence Complete?
No
Yes
Load Next Instruction

*NOTE The clear of TCR bit 7 must be accomplished with software

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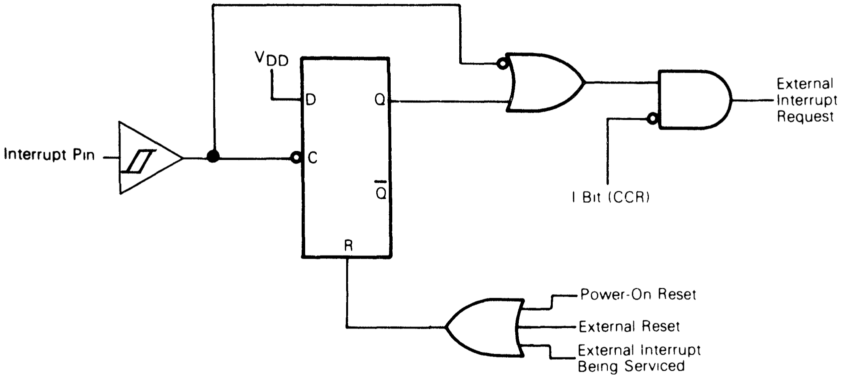
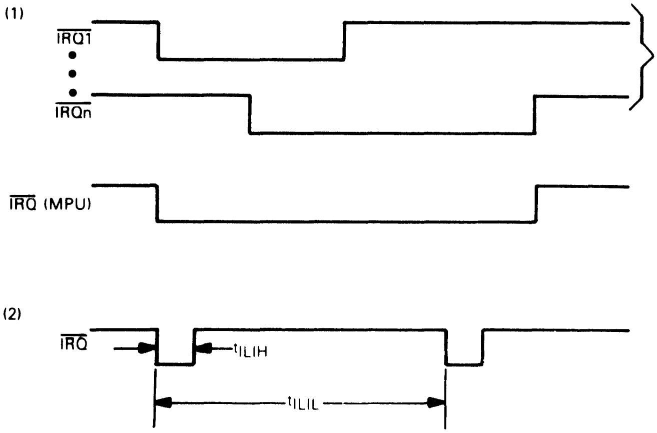
Fig. 15 - Interrupt and instruction processing flowchart.

(a) Interrupt Functional Diagram



(b) Interrupt Mode Diagram



Wire OR'ed Condition
(If after servicing an interrupt the $\overline{IRQ}$ remains low, then the next interrupt is recognized)

Pulse Condition

The minimum pulse width (t_{ILIH}) is one t_{cyc} The period t_{ILIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routine plus 20 t_{cyc} cycles

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Fig. 16 - External interrupt.

STOP — The STOP instruction places the CDP6805E3 in a low power consumption mode In the STOP function the internal oscillator is turned off, causing all internal processing and the timer to be halted; refer to Figure 17. The DS and AS lines go to a low state and the R/$\overline{W}$ line goes to a high state The multiplexed address/data bus goes to the data input state The high order address lines remain at the address of the next instruction The MPU remains in the STOP mode until an external interrupt or reset occurs; refer to Figure 8 and 17.

During the STOP mode, timer control register (TCR) bits 6 and 7 are altered to remove any pending timer interrupt requests and to disable any further timer interrupts External interrupts are enabled in the condition code register All other registers and memory remain unaltered All I/O lines remain unchanged

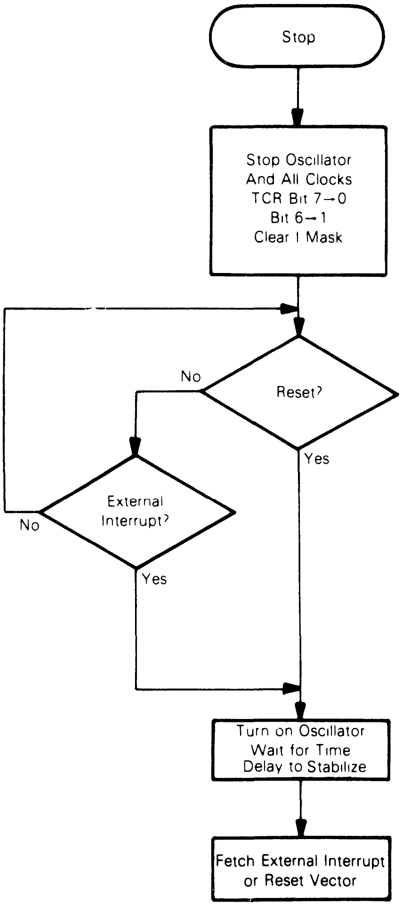

Fig. 17 - Stop function flowchart.

WAIT – The WAIT instruction places the CDP6805E3 in a low power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode; refer to Table 1 In the WAIT function, the internal clock is disabled from all internal circuitry except the Timer circuit; refer to Figure 18 Thus, all internal processing is halted except the Timer which is allowed to count in a normal sequence. The R/$\overline{W}$ line goes to a high state, the multiplexed address/data bus goes to the data input state, and the DS and AS lines go to the low state The high order address lines remain at the address of the next instruction. The MPU remains in this state until an external interrupt, timer interrupt, or a reset occurs, refer to Figures 7 and 18

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During the WAIT mode, the I-bit in the condition code register is cleared to enable interrupts. All other registers, memory, and I/O lines remain in their last state The timer may be enabled to allow a periodic exit from the WAIT mode If an external and a timer interrupt occur at the same time, the external interrupt is serviced first, then, if the timer interrupt request is not cleared in the external interrupt routine, the normal timer interrupt (not the timer WAIT interrupt) is serviced since the MCU is no longer in the WAIT mode

TIMER

The MPU timer contains a single 8-bit software programmable counter with 7-bit software selectable prescaler. The counter may be preset under program control and decrements towards zero When the counter decrements to zero, the timer interrupt request bit, i e , bit 7 of the Timer Control Register (TCR) is set Then if the timer interrupt is not masked, i e , bit 6 of the TCR and the I-bit in the Condition Code Register are both cleared, the processor receives an interrupt After completion of the current instruction, the processor proceeds to store the appropriate registers on the stack, and then fetches the timer vector address from locations $FFF8 and $FFF9 in order to begin servicing the interrupt, unless it was in locations $FFF6 and $FFF7 the WAIT mode

The counter continues to count after it reaches zero, allowing the software to determine the number of internal or external input clocks since the timer interrupt request bit was set The counter may be read at any time by the processor without disturbing the count The contents of the counter becomes stable prior to the read portion of a cycle and does not change during the read The timer interrupt request bit remains set until cleared by the software If this happens before the timer interrupt is serviced, the interrupt is lost. TCR7 may also be used as a scanned status bit in a non-interrupt mode of operation (TCR6 = 1)

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer Bit 0, bit 1, and bit 2 of the TCR are programmed to choose the appropriate prescaler output which is used as the counter input The processor cannot write into or read from the prescaler, however, its contents are cleared to all "0's" by the write operation into TCR when bit 3 of the written data equals 1, which allows for truncation-free counting

The Timer input can be configured for three different operating modes, plus a disable mode depending on the value written to the TCR4, TCR5 control bits. Refer to the TIMER CONTROL REGISTER section.

Timer Input Mode 1 – If TCR4 and TCR5 are both programmed to a "0", the input to the Timer is from an internal clock and the Timer input is disabled. The internal clock mode can be used for periodic interrupt generation, as well

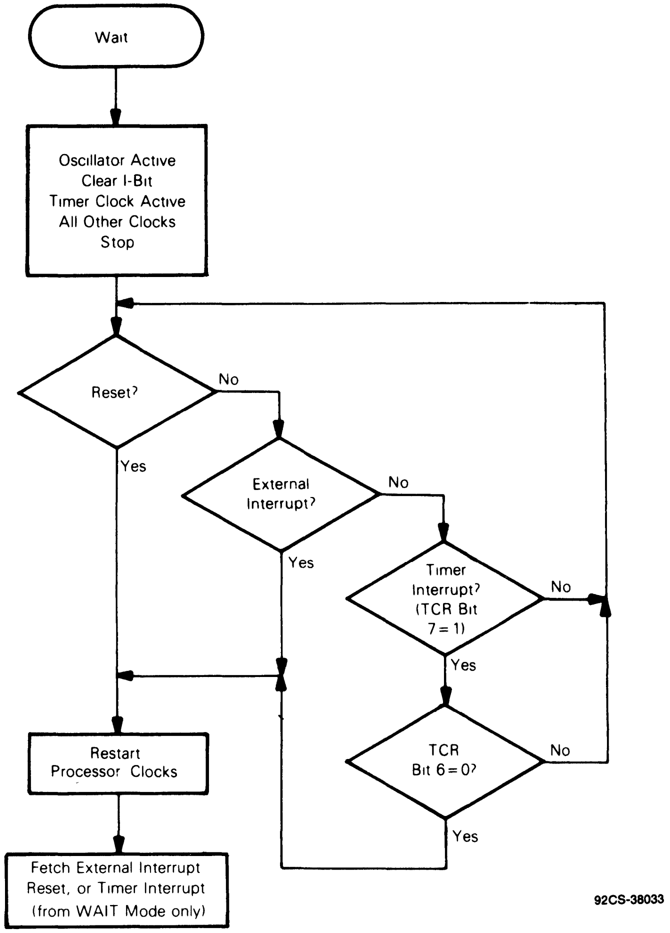


Fig. 18 - Wait function flowchart.

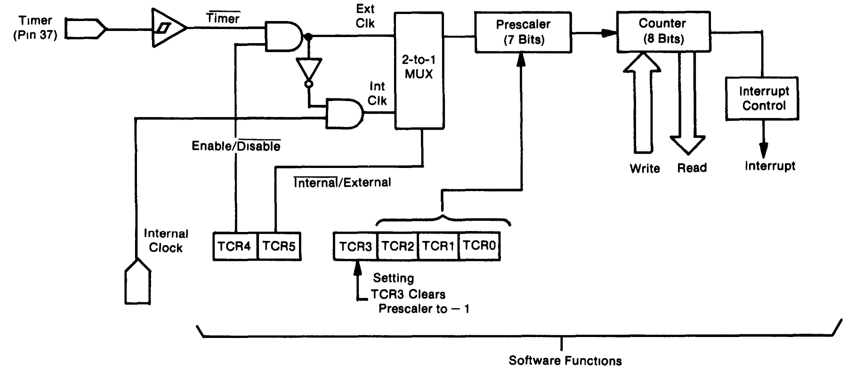
as a reference in frequency and event measurement The internal clock is the instruction cycle clock and is coincident with Address Strobe (AS) except during a WAIT instruction. During a WAIT instruction the AS pin goes to a low state but the internal clock to the Timer continues to run at its normal rate.

Timer Input Mode 2 – With TCR4=1 and TCR5=0, the internal clock and the TIMER input pin are ANDed together to form the Timer input signal. This mode can be used to measure external pulse widths The external pulse simply turns on the internal clock for the duration of the pulse. The resolution of the count in this mode is ±1 clock and therefore accuracy improves with longer input pulse widths.

Timer Input Mode 3 – If TCR4=0 and TCR5=1, then all inputs to the Timer are disabled

Timer Input Mode 4 – If TCR4=1 and TCR5=1, the internal clock input to the Timer is disabled and the TIMER input pin becomes the input to the Timer. The external Timer pin can, in this mode, be used to count external events as well as external frequencies for generating periodic interrupts.

Figure 19 shows a block diagram of the Timer subsystem Power-on Reset and the STOP instruction cause the counter to be set to $FO



NOTES
1 Prescaler and 8-bit counter are clocked falling edge of the internal clock (AS) or external input
2 Counter is written to during Data Strobe (DS) and counts down continuously

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Fig. 19 - Timer block diagram.

Timer Control Register (TCR)

7	6	5	4	3	2	1	0
TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0

All bits in this register except bit 3 are Read/Write bits

TCR7 – Timer interrupt request bit bit used to indicate the timer interrupt when it is logic "1"

1 – Set whenever the counter decrements to zero, or under program control
0 – Cleared on external reset, power-on reset, STOP instruction, or program control

TCR6 – Timer interrupt mask bit when this bit is a logic "1" it inhibits the timer interrupt to the processor

1 – Set on external reset, power-on reset, STOP instruction, or program control
0 – Cleared under program control

TCR5 – External or internal bit selects the input clock source to be either the external timer pin or the internal clock (Unaffected by $\overline{\text{RESET}}$)

1 – Select external clock source
0 – Select internal clock source (AS)

TCR4 – External enable bit control bit used to enable the external timer pin (Unaffected by $\overline{\text{RESET}}$)

1 – Enable external timer pin
0 – Disable external timer pin

TCR5	TCR4	
0	0	Internal clock (AS) to Timer
0	1	AND of internal clock (AS) and TIMER pin to Timer
1	0	Inputs to Timer disabled
1	1	TIMER pin to Timer

Refer to Figure 19 for Logic Representation

TCR3 – Timer Prescaler Reset bit writing a "1" to this bit resets the prescaler to zero A read of this location always indicates a "0 " (Unaffected by $\overline{\text{RESET}}$)

TCR2, TCR1, TCR0 – Prescaler address bits decoded to select one of eight taps on the prescaler (Unaffected by $\overline{\text{RESET}}$)

Prescaler

TCR2	TCR1	TCR0	Result
0	0	0	−1
0	0	1	−2
0	1	0	−4
0	1	1	−8
1	0	0	−16
1	0	1	÷32
1	1	0	÷64
1	1	1	÷128

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INSTRUCTION SET

The MPU has a set of 61 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

REGISTER/MEMORY INSTRUCTIONS – Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 4

READ/MODIFY/WRITE INSTRUCTIONS – These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register The test for negative or zero (TST) instruction is an exception to the read/modify/write sequence since it does not modify the value Refer to Table 5

BRANCH INSTRUCTIONS – This set of instructions branches if a particular condition is met, otherwise no operation is performed. Branch instructions are two byte instructions Refer to Table 6

BIT MANIPULATION INSTRUCTIONS – The MPU is capable of setting or clearing any bit which resides in the first 256 bytes of the memory space, where all port registers, port DDRs, timer, timer control, and on-chip RAM reside An additional feature allows the software to test and branch on the state of any bit within these 256 locations The bit set, bit clear and bit test and branch functions are all implemented with a single instruction For the test and branch instructions the value of the bit tested is also placed in the carry bit of the Condition Code Register Refer to Table 7 for instruction cycle timing

CONTROL INSTRUCTIONS – These instructions are register reference instructions and are used to control processor operation during program execution Refer to Table 8 for instruction cycle timing

ALPHABETICAL LISTING – The complete instruction set is given in alphabetical order in Table 9

OPCODE MAP SUMMARY – Table 10 is an opcode map for the instructions used on the MCU

ADDRESSING MODES

The MPU uses ten different addressing modes to give the programmer an opportunity to optimize the code to all situations The various indexed addressing modes make it possible to locate data tables, code conversion tables and scaling tables anywhere in the memory space Short indexed accesses are single byte instructions, while the longest instructions (three bytes) permit tables throughout memory Short and long absolute addressing is also included Two byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory. Table 9 shows the addressing modes for each instruction, with the effects each instruction has on the Condition Code Register. An opcode map is shown in Table 10.

The term "Effective Address" or EA is used in describing the various addressing modes, which is defined as the address to or from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate "contents of," an arrow indicates "is replaced by" and a colon indicates concatenation of two bytes

Inherent – In inherent instructions all the information necessary to execute the instruction is contained in the opcode Operations specifying only the index register or accumulator, and no other arguments, are included in this mode

Immediate – In immediate addressing, the operand is contained in the byte immediately following the opcode Immediate addressing is used to access constants which do not change during program execution (e.g , a constant used to initialize a loop counter)

$$EA = PC + 1,\ PC \leftarrow PC + 2$$

Direct – In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two byte instruction. This includes all on-chip RAM and I/O registers and up to 128 bytes of off-chip ROM Direct addressing is efficient in both memory and speed

$$EA = (PC + 1),\ PC \leftarrow PC + 2$$

Address Bus High ← 0, Address Bus Low ← (PC + 1)

Extended – In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode Instructions with extended addressing modes are capable of referencing arguments anywhere in memory with a single three byte instruction

$$EA = (PC + 1)\ (PC + 2),\ PC \leftarrow PC + 3$$

Address Bus High ← (PC + 1), Address Bus Low ← (PC + 2)

Indexed, No-Offset – In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register Thus, this addressing mode can access the first 256 memory locations These instructions are only one byte long This mode is used to move a pointer through a table or to address a frequently referenced RAM or I/O location

$$EA = X,\ PC \leftarrow PC + 1$$

Address Bus High ← 0, Address Bus Low ← X

TABLE 4 — REGISTER/MEMORY INSTRUCTIONS

		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
Function	**Mnemonic**	**Op Code**	**# Bytes**	**# Cycles**	**Op Code**	**# Bytes**	**# Cycles**	**Op Code**	**# Bytes**	**# Cycles**	**Op Code**	**# Bytes**	**# Cycles**	**Op Code**	**# Bytes**	**# Cycles**	**Op Code**	**# Bytes**	**# Cycles**
Load A from Memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from Memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in Memory	STA	–	–	–	B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in Memory	STX	–	–	–	BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add Memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add Memory and Carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract Memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND Memory to A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR Memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump Unconditional	JMP	–	–	–	BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to Subroutine	JSR	–	–	–	BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

TABLE 5 — READ/MODIFY/WRITE INSTRUCTIONS

		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8-Bit Offset)		
Function	**Mnemonic**	**Op Code**	**# Bytes**	**# Cycles**	**Op Code**	**# Bytes**	**# Cycles**	**Op Code**	**# Bytes**	**# Cycles**	**Op Code**	**# Bytes**	**# Cycles**	**Op Code**	**# Bytes**	**# Cycles**
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (2's Complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate Left Thru Carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate Right Thru Carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical Shift Left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical Shift Right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic Shift Right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for Negative or Zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5

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TABLE 6 — BRANCH INSTRUCTIONS

		Relative Addressing Mode		
Function	Mnemonic	Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	3
Branch Never	BRN	21	2	3
Branch IFF Higher	BHI	22	2	3
Branch IFF Lower or Same	BLS	23	2	3
Branch IFF Carry Clear	BCC	24	2	3
(Branch IFF Higher or Same)	(BHS)	24	2	3
Branch IFF Carry Set	BCS	25	2	3
(Branch IFF Lower)	(BLO)	25	2	3
Branch IFF Not Equal	BNE	26	2	3
Branch IFF Equal	BEQ	27	2	3
Branch IFF Half Carry Clear	BHCC	28	2	3
Branch IFF Half Carry Set	BHCS	29	2	3
Branch IFF Plus	BPL	2A	2	3
Branch IFF Minus	BMI	2B	2	3
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	3
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	3
Branch IFF Interrupt Line is Low	BIL	2E	2	3
Branch IFF Interrupt Line is High	BIH	2F	2	3
Branch to Subroutine	BSR	AD	2	6

TABLE 7 — BIT MANIPULATION INSTRUCTIONS

		Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is Set	BRSET n (n=0 7)	–	–	–	2•n	3	5
Branch IFF Bit n is Clear	BRCLR n (n=0 7)	–	–	–	01+2•n	3	5
Set Bit n	BSET n (n=0 7)	10+2•n	2	5	–	–	–
Clear Bit n	BCLR n (n=0 7)	11+2•n	2	5	–	–	–

TABLE 8 — CONTROL INSTRUCTIONS

		Inherent		
Function	Mnemonic	Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	10
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

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TABLE 9 - INSTRUCTION SET

Mnemonic	Addressing Modes										Condition Codes				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/ Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
ADD		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
AND		X	X	X		X	X	X			●	●	Λ	Λ	●
ASL	X		X			X	X				●	●	Λ	Λ	Λ
ASR	X		X			X	X				●	●	Λ	Λ	Λ
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	Λ	Λ	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	Λ
BRSET										X	●	●	●	●	Λ
BSET									X		●	●	●	●	●
BSR					X						●	●	●	●	●
CLC	X										●	●	●	●	0
CLI	X										●	0	●	●	●
CLR	X		X			X	X				●	●	0	1	●
CMP		X	X	X		X	X	X			●	●	Λ	Λ	Λ
COM	X		X			X	X				●	●	Λ	Λ	1
CPX		X	X	X		X	X	X			●	●	Λ	Λ	Λ
DEC	X		X			X	X				●	●	Λ	Λ	●
EOR		X	X	X		X	X	X			●	●	Λ	Λ	●
INC	X		X			X	X				●	●	Λ	Λ	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	Λ	Λ	●
LDX		X	X	X		X	X	X			●	●	Λ	Λ	●
LSL	X		X			X	X				●	●	Λ	Λ	Λ
LSR	X		X			X	X				●	●	0	Λ	Λ
NEG	X		X			X	X				●	●	Λ	Λ	Λ
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	Λ	Λ	●
ROL	X		X			X	X				●	●	Λ	Λ	Λ
ROR	X		X			X	X				●	●	Λ	Λ	Λ
RSP	X										●	●	●	●	●
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	Λ	Λ	●
STOP	X										●	0	●	●	●
STX			X	X		X	X	X			●	●	Λ	Λ	●
SUB		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	Λ	Λ	●
TXA	X										●	●	●	●	●
WAIT	X										●	0	●	●	●

Condition Code Symbols

H	Half Carry (From Bit 3)
I	Interrupt Mask
N	Negative (Sign Bit)
Z	Zero
C	Carry/Borrow
Λ	Test and Set if True Cleared Otherwise
●	Not Affected
?	Load CC Register From Stack
0	Cleared
1	Set

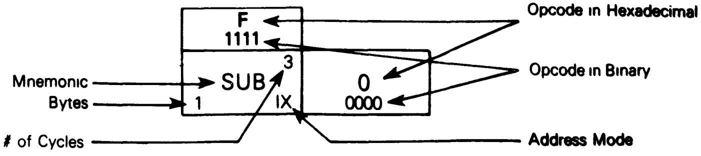
TABLE 10 — CDP6805E3 INSTRUCTION SET OPCODE MAP

	Bit Manipulation		Branch	Read/Modify/Write					Control		Register/Memory						
	BTB	BSC	REL	DIR	INH(A)	INH(X)	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
Hi / Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Hi / Low
0 0000	5 BRSET0 3 BTB	5 BSET0 2 BSC	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH	3 NEGX 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0 0000
1 0001	5 BRCLR0 3 BTB	5 BCLR0 2 BSC	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1 0001
2 0010	5 BRSET1 3 BTB	5 BSET1 2 BSC	3 BHI 2 REL								2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2 0010
3 0011	5 BRCLR1 3 BTB	5 BCLR1 2 BSC	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3 0011
4 0100	5 BRSET2 3 BTB	5 BSET2 2 BSC	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4 0100
5 0101	5 BRCLR2 3 BTB	5 BCLR2 2 BSC	3 BCS 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5 0101
6 0110	5 BRSET3 3 BTB	5 BSET3 2 BSC	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6 0110
7 0111	5 BRCLR3 3 BTB	5 BCLR3 2 BSC	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7 0111
8 1000	5 BRSET4 3 BTB	5 BSET4 2 BSC	3 BHCC 2 REL	5 LSL 2 DIR	3 LSLA 1 INH	3 LSLX 1 INH	6 LSL 2 IX1	5 LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8 1000
9 1001	5 BRCLR4 3 BTB	5 BCLR4 2 BSC	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9 1001
A 1010	5 BRSET5 3 BTB	5 BSET5 2 BSC	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A 1010
B 1011	5 BRCLR5 3 BTB	5 BCLR5 2 BSC	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B 1011
C 1100	5 BRSET6 3 BTB	5 BSET6 2 BSC	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C 1100
D 1101	5 BRCLR6 3 BTB	5 BCLR6 2 BSC	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D 1101
E 1110	5 BRSET7 3 BTB	5 BSET7 2 BSC	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E 1110
F 1111	5 BRCLR7 3 BTB	5 BCLR7 2 BSC	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F 1111

Abbreviations for Address Modes

INH	Inherent
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
BTB	Bit Test and Branch
IX	Indexed (No Offset)
IX1	Indexed, 1 Byte (8-Bit) Offset
IX2	Indexed, 2 Byte (16-Bit) Offset
•	CMOS Versions Only

LEGEND



Indexed, 8-bit Offset – Here the EA is obtained by adding the contents of the byte following the opcode to that of the index register The operand is therefore located anywhere within the lowest 511 memory locations. For example, this mode of addressing is useful for selecting the m-th element in an n element table All instructions are two bytes The contents of the index register (X) is not changed The contents of (PC + 1) is an unsigned 8-bit integer One byte offset indexing permits look-up tables to be easily accessed in either RAM or ROM

$$EA = X + (PC + 1),\ PC \leftarrow PC + 2$$
Address Bus High ← K, Address Bus Low ← $X + (PC + 1)$
Where K = The carry from the addition of $X + (PC + 1)$

Indexed, 16-Bit Offset – In the indexed, 16-bit offset addressing mode the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode This addressing mode can be used in a manner similar to indexed 8-bit offset, except that this three byte instruction allows tables to be anywhere in memory (e g , jump tables in ROM) The content of the index register is not changed

$$EA = X + [(PC + 1)\ (PC + 2)],\ PC \leftarrow PC + 3$$
Address Bus High ← $(PC + 1) + K$,
Address Bus Low ← $X + (PC + 2)$
Where K = The carry from the addition of $X + (PC + 2)$

Relative – Relative addressing is only used in branch instructions In relative addressing the contents of the 8-bit signed byte following the opcode (the offset) is added to the PC if and only if the branch condition is true Otherwise, control proceeds to the next instruction The span of relative addressing is limited to the range of – 126 to + 129 bytes from the branch instruction opcode location

$EA = PC + 2 + (PC + 1),\ PC \leftarrow EA$ if branch taken,
otherwise $PC \leftarrow PC + 2$

Bit Set/Clear – Direct addressing and bit addressing are combined in instructions which set and clear individual memory and I/O bits In the bit set and clear instructions, the byte is specified as a direct address in the location following the opcode The first 256 addressable locations are thus accessed The bit to be modified within that byte is specified with three bits of the opcode The bit set and clear instructions occupy two bytes, one for the opcode (including the bit number) and the second to address the byte which contains the bit of interest

$$EA = (PC + 1),\ PC \leftarrow PC + 2$$
Address Bus High ← 0, Address Bus Low ← $(PC + 1)$

Bit Test and Branch – Bit test and branch is a combination of direct addressing, bit addressing and relative addressing The bit address and condition (set or clear) to be tested is part of the opcode The address of the byte to be tested is in the single byte immediately following the opcode byte (EA1) The signed relative 8-bit offset is in the third byte (EA2) and is added to the PC if the specified bit is set or clear in the specified memory location This single three byte instruction allows the program to branch based on the condition of any bit in the first 256 locations of memory

$$EA1 = (PC + 1)$$
Address Bus High ← 0, Address Bus Low ← $(PC + 1)$
$EA2 = PC + 3 + (PC + 2),\ PC \leftarrow EA2$ if branch taken,
otherwise $PC \leftarrow PC + 3$

SYSTEM CONFIGURATION

Figures 20 through 25 show in general terms how the CDP6805E3 bus structure may be utilized. Specified interface details vary with the various peripheral and memory devices employed

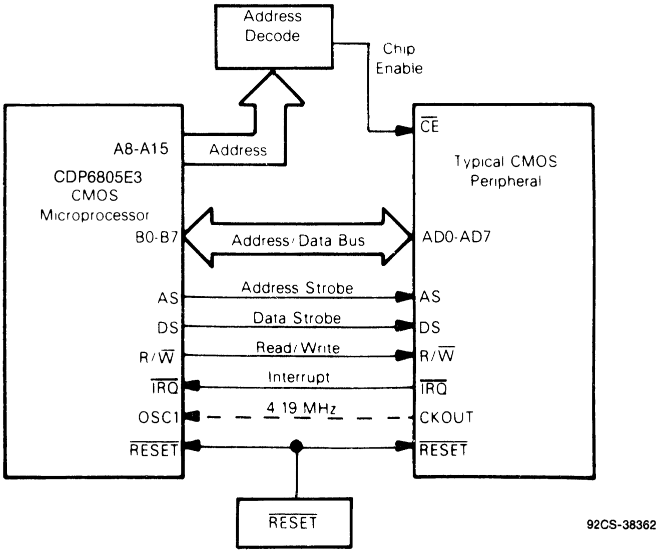
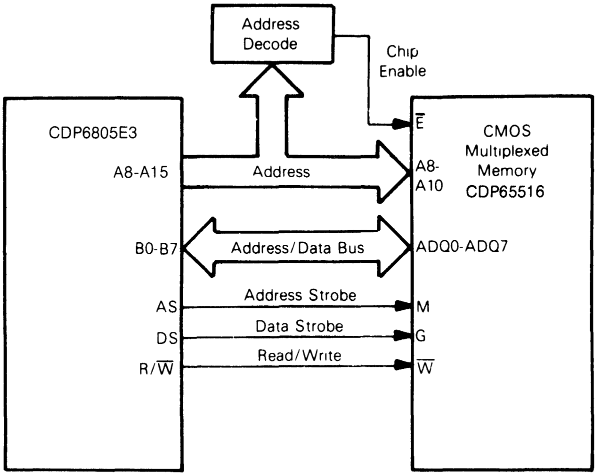


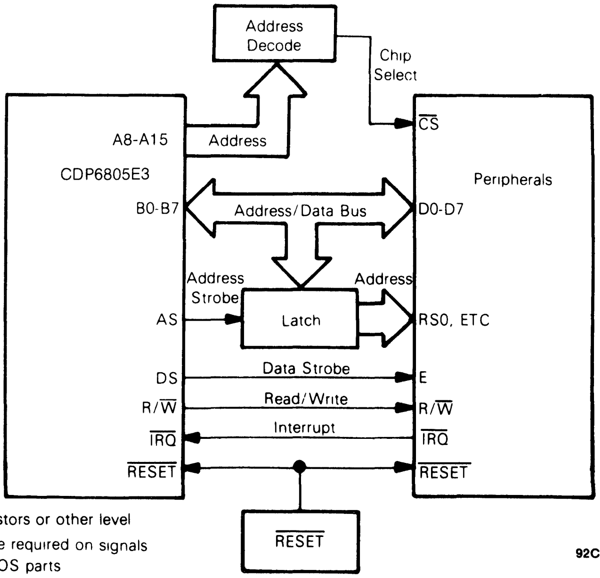
Fig. 20 - Connection to CMOS peripherals.

CDP6805E3, CDP6805E3C



92CS-38363

Fig. 21 - Connection to CMOS multiplexed memories.



NOTE In some cases, pullup resistors or other level shifting techniques may be required on signals going from NMOS to CMOS parts

92CS-38364

Fig. 22 - Connection to peripherals.

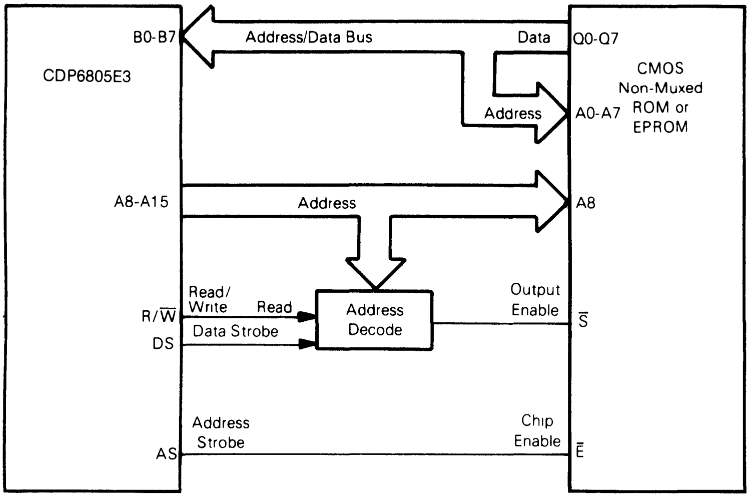


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Fig. 23 - Connection to latch non-multiplexed CMOS ROM or EPROM.

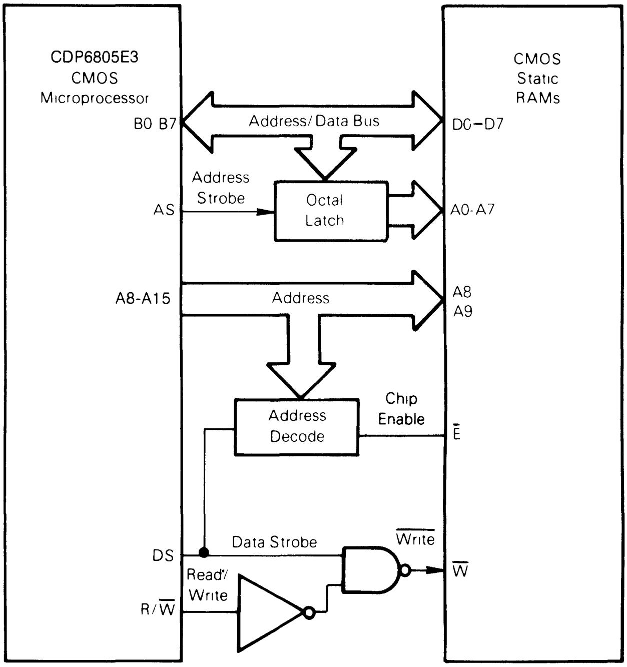

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Fig. 24 - Connection to static CMOS RAMs.

CDP6805E3, CDP6805E3C

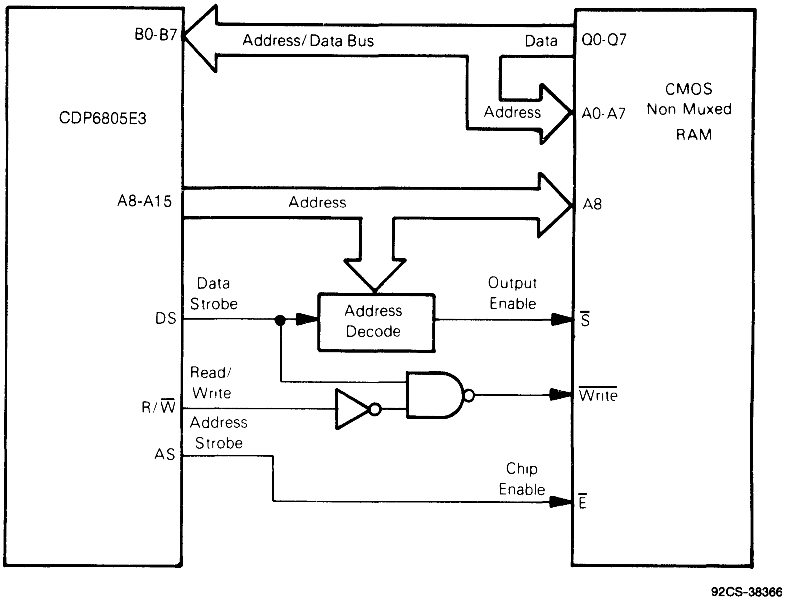


Fig. 25 - Connection to latched non-multiplexed CMOS RAM.

Table 11 provides a detailed description of the information present on the Bus, the Read/Write (R/$\overline{W}$) pin and the Load Instruction (LI) pin during each cycle for each instruction.

This information is useful in comparing actual with expected results during debug of both software and hardware as the control program is executed. The information is categorized in groups according to addressing mode and number of cycles per instruction.

TABLE 11 — SUMMARY OF CYCLE BY CYCLE OPERATION

Address Mode Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$ Pin	LI Pin	Data Bus
Inherent						
LSR LSL ASR NEG CLR ROL COM ROR DEC INC TST	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Op Code Address + 1	1	0	Op Code Next Instruction
TAX CLC SEC STOP CLI SEI RSP WAIT NOP TXA	2	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
RTS	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Stack Pointer	1	0	Irrelevant Data
		4	Stack Pointer + 1	1	0	Irrelevant Data
		5	Stack Pointer + 2	1	0	Irrelevant Data
		6	New Op Code Address	1	0	New Op Code
SWI	10	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Stack Pointer	0	0	Return Address (LO Byte)
		4	Stack Pointer − 1	0	0	Return Address (HI Byte)
		5	Stack Pointer − 2	0	0	Contents of Index Register
		6	Stack Pointer − 3	0	0	Contents of Accumulator
		7	Stack Pointer − 4	0	0	Contents of CC Register
		8	Vector Address FFFC (Hex)	1	0	Address of Int Routine (HI Byte)
		9	Vector Address FFFD (Hex)	1	0	Address of Int. Routine (LO Byte)
		10	Interrupt Routine Starting Address	1	0	Interrupt Routine First Opcode
RTI	9	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Stack Pointer	1	0	Irrelevant Data
		4	Stack Pointer + 1	1	0	Irrelevant Data
		5	Stack Pointer + 2	1	0	Irrelevant Data
		6	Stack Pointer + 3	1	0	Irrelevant Data
		7	Stack Pointer + 4	1	0	Irrelevant Data
		8	Stack Pointer + 5	1	0	Irrelevant Data
		9	New Op Code Address	1	0	New Op Code
Immediate						
ADC EOR CPX ADD LDA LDX AND ORA BIT SBC CMB SUB	2	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Operand Data
Bit Set/Clear						
BSET n BCLR n	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Address of Operand	1	0	Operand Data
		4	Address of Operand	1	0	Operand Data
		5	Address of Operand	0	0	Manipulated Data
Bit Test and Branch						
BRSET n BRCLR n	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Address of Operand	1	0	Operand Data
		4	Op Code Address + 2	1	0	Branch Offset
		5	Op Code Address + 2	1	0	Branch Offset
Relative						
BCC BHI BNE BEQ BCS BPL BHCC BLS BIL BMC BRN BHCS BIH BMI BMS BRA	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Branch Offset
		3	Op Code Address + 1	1	0	Branch Offset
BSR	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Branch Offset
		3	Op Code Address + 1	1	0	Branch Offset
		4	Subroutine Starting Address	1	0	First Subroutine Op Code
		5	Stack Pointer	0	0	Return Address (LO Byte)
		6	Stack Pointer − 1	0	0	Return Address (HI Byte)

CDP6805E3, CDP6805E3C

TABLE 11 — SUMMARY OF CYCLE BY CYCLE OPERATION (CONTINUED)

Address Mode Instructions	Cycles	Cycles #	Address Bus	R/$\overline{W}$ Pin	LI Pin	Data Bus
Direct						
JMP	2	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Jump Address
ADC EOR CPX ADD LDA LDX AND ORA BIT SBC CMP SUB	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Address of Operand	1	0	Operand Data
TST	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Address of Operand	1	0	Operand Data
		4	Op Code Address + 2	1	0	Op Code Next Instruction
STA STX	4	1	Op Code Address	1	1	Op Code
		2	Op Code Adrress + 1	1	0	Address of Operand
		3	Op Code Address + 1	1	0	Address of Operand
		4	Address of Operand	0	0	Operand Data
LSL LSR DEC ASR NEG INC CLR ROL COM ROR	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand
		3	Operand Address	1	0	Current Operand Data
		4	Operand Address	1	0	Current Operand Data
		5	Operand Address	0	0	New Operand Data
JSR	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Subroutine Address (LO Byte)
		3	Subroutine Starting Address	1	0	1st Subroutine Op Code
		4	Stack Pointer	0	0	Return Address (LO Byte)
		5	Stack Pointer − 1	0	0	Return Address (HI Byte)
Extended						
JMP	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Jump Address (HI Byte)
		3	Op Code Address + 2	1	0	Jump Address (LO Byte)
ADC BIT ORA ADD CMP LDX AND EOR SBC CPX LDA SUB	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address Operand (HI Byte)
		3	Op Code Address + 2	1	0	Address Operand (LO Byte)
		4	Address of Operand	1	0	Operand Data
STA STX	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Operand (HI Byte)
		3	Op Code Address + 2	1	0	Address of Operand (LO Byte)
		4	Op Code Address + 2	1	0	Address of Operand (LO Byte)
		5	Address of Operand	0	0	Operand Data
JSR	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Address of Subroutine (HI Byte)
		3	Op Code Address + 2	1	0	Address of Subroutine (LO Byte)
		4	Subroutine Starting Address	1	0	1st Subroutine Op Code
		5	Stack Pointer	0	0	Return Address (LO Byte)
		6	Stack Pointer − 1	0	0	Return Address (HI Byte)
Indexed, No-Offset						
JMP	2	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
ADC EOR CPX ADD LDA LDX AND ORA BIT SBC CMP SUB	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Index Register	1	0	Operand Data
TST	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Index Register	1	0	Operand Data
		4	Op Code Address + 1	1	0	Op Code Next Instruction
STA STX	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Op Code Address + 1	1	0	Op Code Next Instruction
		4	Index Register	0	0	Operand Data
LSL LSR DEC ASR NEG INC CLR ROL COM ROR	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Index Register	1	0	Current Operand Data
		4	Index Register	1	0	Current Operand Data
		5	Index Register	0	0	New Operand Data
JSR	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Op Code Next Instruction
		3	Index Register	1	0	1st Subroutine Op Code
		4	Stack Pointer	0	0	Return Address (LO Byte)
		5	Stack Pointer − 1	0	0	Return Address (HI Byte)

CDP6805E3, CDP6805E3C

TABLE 11 — SUMMARY OF CYCLE BY CYCLE OPERATION (CONTINUED)

Address Mode Instructions	Cycles	Cycles #	Address Bus	R/$\overline{W}$ Pin	LI Pin	Data Bus
Indexed 8-Bit Offset						
JMP	3	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
ADC EOR CPX ADD LDA LDX AND ORA CMP SUB BIT SBC	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	Operand Data
STA STX	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Op Code Address + 1	1	0	Offset
		5	Index Register + Offset	0	0	Operand Data
TST	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	Operand Data
		5	Op Code Address + 2	1	0	Op Code Next Instruction
LSL LSR ASR NEG CLR ROL COM ROR DEC INC	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	Current Operand Data
		5	Index Register + Offset	1	0	Current Operand Data
		6	Index Register + Offset	0	0	New Operand Data
JSR	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset
		3	Op Code Address + 1	1	0	Offset
		4	Index Register + Offset	1	0	1st Subroutine Op Code
		5	Stack Pointer	0	0	Return Address LO Byte
		6	Stack Pointer − 1	0	0	Return Address HI Byte
Indexed, 16-Bit Offset						
JMP	4	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
ADC CMP SUB ADD EOR SBC AND ORA CPX LDA BIT LDX	5	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
		5	Index Register + Offset	1	0	Operand Data
STA STX	6	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
		5	Op Code Address + 2	1	0	Offset (LO Byte)
		6	Index Register + Offset	0	0	Operand Data
JSR	7	1	Op Code Address	1	1	Op Code
		2	Op Code Address + 1	1	0	Offset (HI Byte)
		3	Op Code Address + 2	1	0	Offset (LO Byte)
		4	Op Code Address + 2	1	0	Offset (LO Byte)
		5	Index Register + Offset	1	0	1st Subroutine Op Code
		6	Stack Pointer	0	0	Return Address (LO Byte)
		7	Stack Pointer − 1	0	0	Return Address (HO Byte)

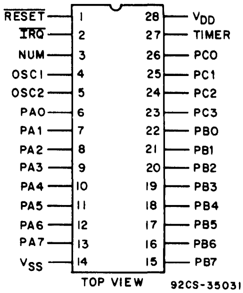
CDP6805E3, CDP6805E3C

TABLE 11 – SUMMARY OF CYCLE BY CYCLE OPERATION (CONTINUED)

Instructions	Cycles	Cycles #	Address Bus	$\overline{\text{RESET}}$ Pin	R/$\overline{\text{W}}$ Pin	LI Pin	Data Bus
Other Functions							
Hardware $\overline{\text{RESET}}$	5		$FFFE	0	1	0	Irrelevant Data
			$FFFE	0	1	0	Irrelevant Data
		1	$FFFE	1	1	0	Irrelevant Data
		2	$FFFE	1	1	0	Irrelevant Data
		3	$FFFE	1	1	0	Vector High
		4	$FFFF	1	1	0	Vector Low
		5	Reset Vector	1	1	0	Op Code
Power on Reset	1922	1	$FFFF	1	1	0	Irrelevant Data
		• • •	• • •	• • •	• • •	• • •	• • •
		1919	$FFFE	1	1	0	Irrelevant Data
		1920	$FFFE	1	1	0	Vector High
		1921	$FFFF	1	1	0	Vector Low
		1922	Reset Vector	1	1	0	Op Code
Instruction	**Cycles**	**Cycles #**	**Address Bus**	**$\overline{\text{IRQ}}$ Pin**	**R/$\overline{\text{W}}$ Pin**	**LI Pin**	**Data Bus**
$\overline{\text{IRQ}}$ Interrupt	10		Last Cycle of Previous Instruction	0	X	0	X
		1	Next Op Code Address	0	1	0	Irrelevant Data
		2	Next Op Code Address	X	1	0	Irrelevant Data
		3	SP	X	0	0	Return Address (LO Byte)
		4	SP – 1	X	0	0	Return Address (HI Byte)
		5	SP – 2	X	0	0	Contents Index Reg
		6	SP – 3	X	0	0	Contents Accumulator
		7	SP – 4	X	0	0	Contents CC Register
		8	See Note Below	X	1	0	Vector High
		9	See Note Below	X	1	0	Vector Low
		10	$\overline{\text{IRQ}}$ Vector	X	1	0	Int Routine First

NOTE: Interrupt Cycles.	Ext. Int Address	Timer Int Address	Timer Int From Wait Address
Cycle #8	$FFFA	$FFF8	$FFF6
Cycle #9	$FFFB	$FFF9	$FFF7

CDP6805F2, CDP6805F2C



TERMINAL ASSIGNMENT

CMOS High-Performance Silicon-Gate 8-Bit Microcomputer

Hardware Features:

- *Typical full speed operating power of 10 mW at 5 V*
- *Typical WAIT mode power of 3 mW*
- *Typical STOP mode power of 5 μW*
- *64 bytes of on-chip RAM*
- *1089 bytes of on-chip ROM*
- *16 bidirectional I/O lines*
- *4 input-only lines*
- *Internal 8-bit timer with software programmable 7-bit prescaler*
- *External timer input*
- *External and timer interrupts*
- *Master reset and power-on reset*
- *Single 3 to 6 volt supply*
- *On-chip oscillator*
- *1 μs cycle time*

The CDP6805F2 Microcomputer Unit (MCU) belongs to the CDP6805 Family of CMOS Microcomputers. This 8-bit MCU contains on-chip oscillator CPU, RAM, ROM, I/O, and Timer. Fully static design allows operation at frequencies down to DC, further reducing its already low-power consumption. It is a low-power processor designed for low-end to mid-range applications in the consumer, automotive, industrial, and communications markets where very low power consumption constitutes an important factor.

Software Features:

- *Versatile interrupt handling*
- *True bit manipulation*
- *10 addressing modes*
- *Efficient instruction set*
- *Memory-mapped I/O*
- *User-callable self-check routines*
- *Two power-saving standby modes*

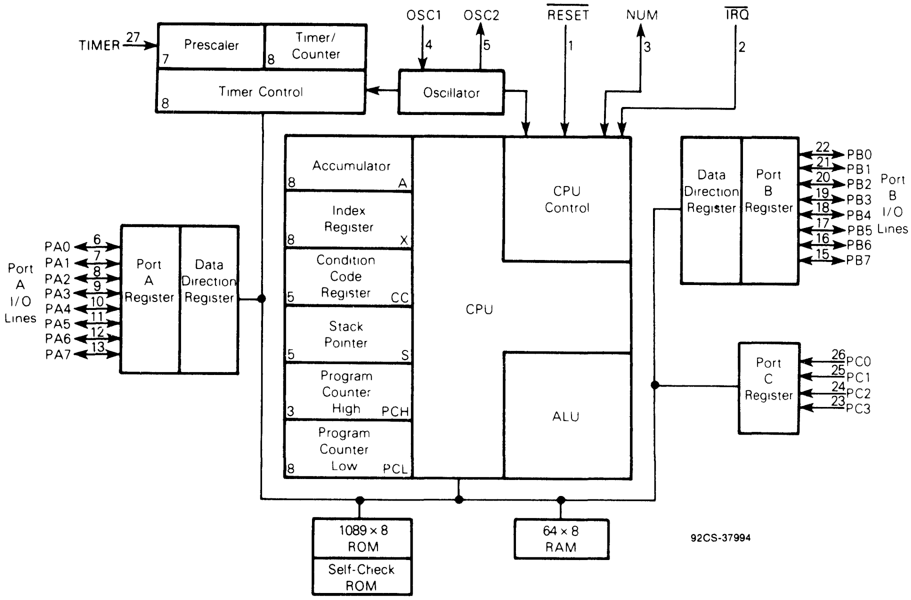


Fig. 1 - CDP6805F2 CMOS microcomputer block diagram

File Number **1369**

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0 3 to +8	V
All Input Voltages Except OSC1	V_{in}	V_{SS}−0 5 to V_{DD}+0 5	V
Current Drain per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range CDP6805F2 CDP6805F2C	T_A	T_L to T_H 0 to 70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

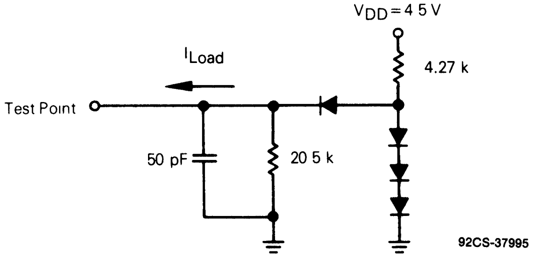


Fig. 2 - Equivalent test load.

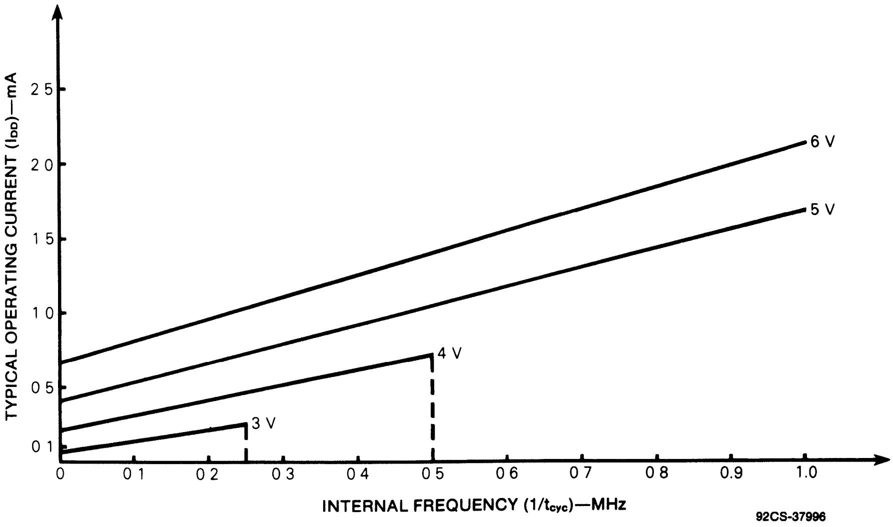


Fig. 3 - Typical operating current vs. internal frequency.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted) (See Note 1)

Characteristics	Symbol	Min	Max	Unit
Output Voltage, $I_{Load} \leq 10\ 0\ \mu A$	V_{OL} V_{OH}	– $V_{DD} - 0\ 1$	0 1 –	V
Output High Voltage ($I_{Load} = -200\ \mu A$) PA0-PA7, PB0-PB7	V_{OH}	4 1	–	V
Output Low Voltage, ($I_{Load} = 800\ \mu A$) PA0-PA7, PB0-PB7	V_{OL}	–	0 4	V
Input High Voltage Ports PA0-PA7, PB0-PB7, PC0-PC3 TIMER, $\overline{IRQ}$, $\overline{RESET}$ OSC1	V_{IH}	 $V_{DD} - 2$ $V_{DD} - 0\ 8$ $V_{DD} - 1\ 5$	 V_{DD} V_{DD} V_{DD}	V
Input Low Voltage, All Inputs	V_{IL}	V_{SS}	0 8	V
Total Supply Current (C_L = 50 pF on Ports, No dc Loads, $t_{cyc} = 1\ \mu s$) RUN (Measured During Self-Check, $V_{IL} = 0\ 2$ V, $V_{IH} = V_{DD} - 0\ 2$ V) WAIT (See Note 2) STOP (See Note 2)	I_{DD}	 – – –	 4 1.5 150	 mA mA μA
I/O Ports Input Leakage — PA0-PA7, PB0-PB7	I_{IL}	–	± 10	μA
Input Current — $\overline{RESET}$, $\overline{IRQ}$, TIMER, OSC1, PC0-PC3	I_{in}	–	± 1	μA
Output Capacitance — Ports A and B	C_{out}	–	12	pF
Input Capacitance — $\overline{RESET}$, $\overline{IRQ}$, TIMER, OSC1, PC0-PC3	C_{in}	–	8	pF

NOTES

1 Electrical Characteristics for V_{DD} = 3 V available soon

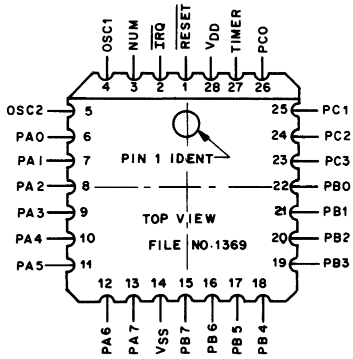
2 Test Conditions for I_{DD} are as follows
All ports programmed as inputs
$V_{IL} = 0\ 2$ V (PA0-PA7, PB0-PB7, PC0-PC3)
$V_{IH} = V_{DD} - 0\ 2$ V for $\overline{RESET}$, $\overline{IRQ}$, TIMER
OSC1 input is a square wave from 0 2 V to $V_{DD} - 0\ 2$ V
OSC2 output load = 20 pF (WAIT I_{DD} is affected linearly by the OSC2 capacitance)

TABLE 1 — CONTROL TIMING CHARACTERISTICS (V_{DD} = 5 Vdc ± 10%, V_{SS} = 0, $T_A = T_L$ to T_H, f_{osc} = 4 MHz, $t_{cyc} = 1\ \mu s$)

Characteristics	Symbol	Min	Max	Unit
Crystal Oscillator Startup Time (See Figure 5)	t_{OXOV}	–	100	ms
Stop Recovery Startup Time — Crystal Oscillator (See Figure 6)	t_{ILCH}	–	100	ms
Timer Pulse Width (See Figure 4)	t_{TH}, t_{TL}	0 5	–	t_{cyc}
Reset Pulse Width (See Figure 5)	t_{RL}	1 5	–	t_{cyc}
Timer Period (See Figure 4)	t_{TLTL}	1	–	t_{cyc}
Interrupt Pulse Width (See Figure 15)	t_{ILIH}	1	–	t_{cyc}
Interrupt Pulse Period (See Figure 15)	t_{ILIL}	*	–	t_{cyc}
OSC1 Pulse Width (See Figure 7)	t_{OH}, t_{OL}	100	–	ns
Cycle Time	t_{cyc}	1000	–	ns
Frequency of Operation Crystal External Clock	f_{osc}	 – dc	 4 4	MHz

*The minimum period, t_{ILIL}, should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routines plus 20 t_{cyc} cycles

TERMINAL ASSIGNMENT



28-Lead Plastic Chip-Carrier Package
(Q Suffix)

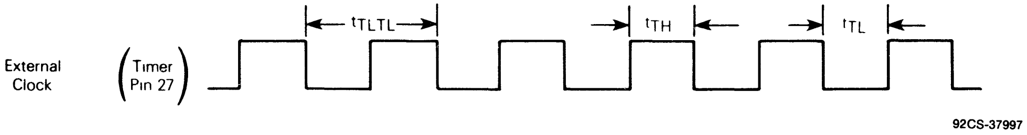
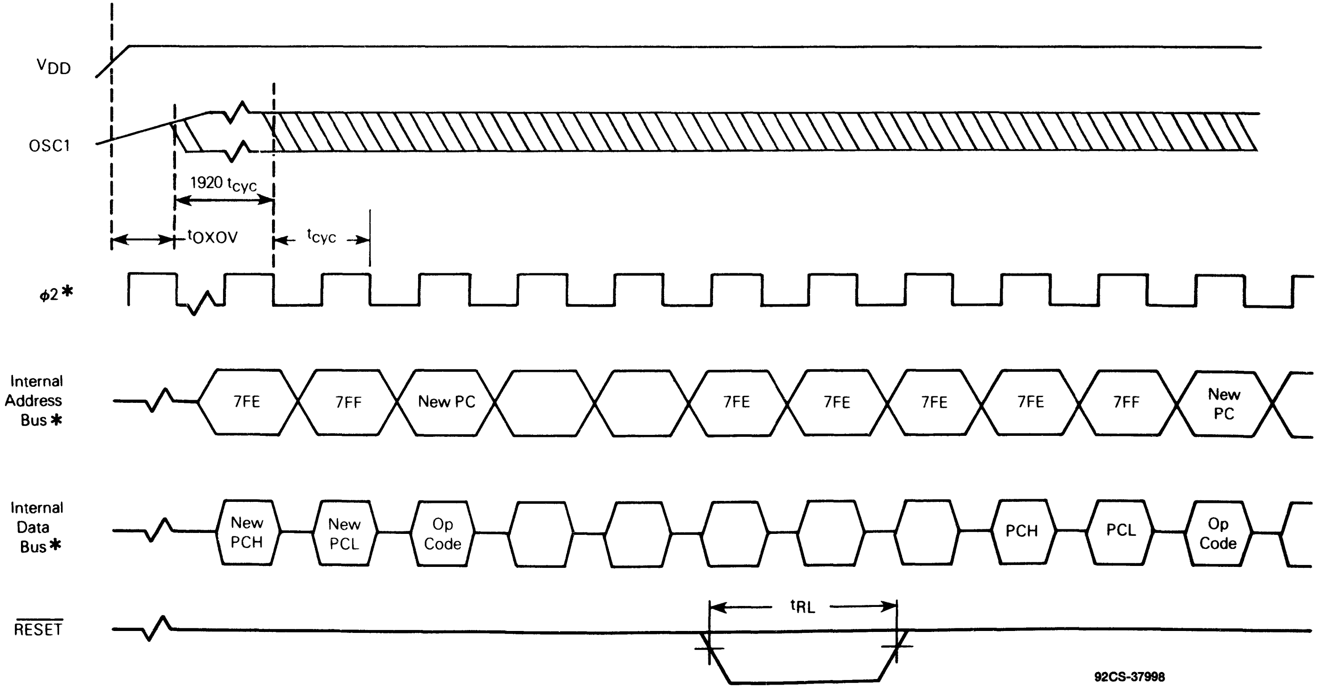


Fig. 4 - Timer relationships.



* Internal timing signal not available externally

Fig. 5 - Power-on RESET and $\overline{\text{RESET}}$.

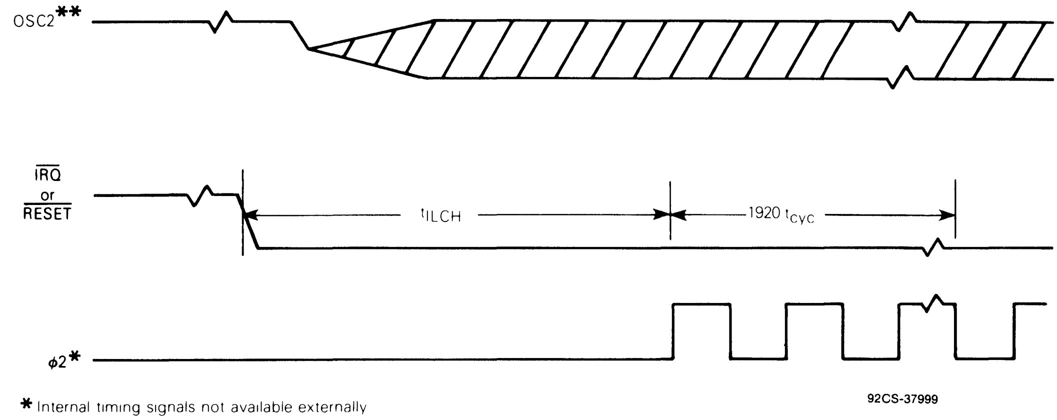

OSC2**
IRQ or RESET
t_{ILCH}
1920 t_{CYC}
φ2*
* Internal timing signals not available externally
** Represents the internal gating of the OSC1 input pin
92CS-37999

Fig. 6 - Stop recovery.

FUNCTIONAL PIN DESCRIPTION

V_{DD} and V_{SS}

Power is supplied to the MCU using these two pins V_{DD} is power and V_{SS} is ground

$\overline{IRQ}$ (MASKABLE INTERRUPT REQUEST)

$\overline{IRQ}$ is photomask option selectable with the choice of interrupt sensitivity being both level and negative edge or negative edge only The MCU completes the current instruction before it responds to the request If $\overline{IRQ}$ is low and the interrupt mask bit (I bit) in the condition code register is clear, the MCU begins an interrupt sequence at the end of the current instruction

If the photomask option is selected to include level sensitivity, then the $\overline{IRQ}$ input requires an external resistor to V_{DD} for "wire-OR" operation See the Interrupt section for more detail

$\overline{RESET}$

The $\overline{RESET}$ input is not required for start-up but can be used to reset the MCU's internal state and provide an orderly software start-up procedure Refer to the Resets section for a detailed description

TIMER

The TIMER input may be used as an external clock for the on-chip timer Refer to the Timer section for a detailed description

NUM (NON-USER MODE)

This pin is intended for use in self-check only User applications should leave this pin connected to ground through a 10 kilohm resistor

OSC1, OSC2

The **CDP6805F2** can be configured to accept either a crystal input or an RC network Additionally, the internal clocks can be derived from either a divide-by-two or divide-by-four of the external frequency (f_{OSC}) Both of these options are photomask selectable

RC – If the RC oscillator option is selected, then a resistor is connected to the oscillator pins as shown in Figure 7(b) The relationship between R and f_{OSC} is shown in Figure 8

CRYSTAL – The circuit shown in Figure 7(a) is recommended when using a crystal The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{OSC} in the electical characteristics table Using an external CMOS oscillator is suggested when crystals outside the specified ranges are to be used The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time Crystal frequency limits are also affected by V_{DD} Refer to Table 1, Control Timing Characteristics, for limits

EXTERNAL CLOCK – An external clock should be applied to the OSC1 input with the OSC2 input not connected, as shown in Figure 7(c) An external clock may be used with either the RC or crystal oscillator mask option t_{OXOV} or t_{ILCH} do not apply when using an external clock input

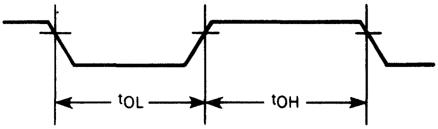
PA0-PA7

These eight I/O lines comprise Port A The state of any pin is software programmable Refer to the Input/Output Programming section for a detailed description

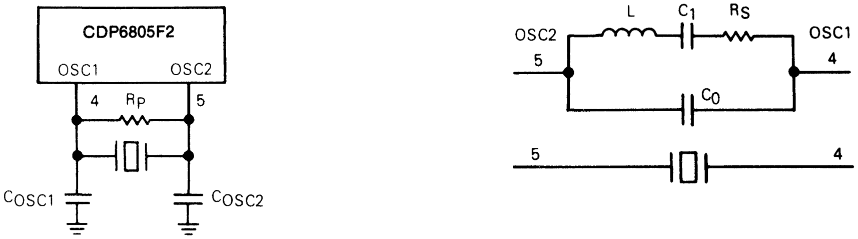
Crystal Parameters

	1 MHz	4 MHz	Units
R_{SMAX}	400	75	Ω
C_0	5	7	pF
C_1	0.008	0.012	µF
C_{OSC1}	15-40	15-30	pF
C_{OSC2}	15-30	15-25	pF
R_P	10	10	MΩ
Q	30 k	40 k	–

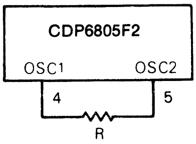
Oscillator Waveform



(a) Crystal Oscillator Connections and Equivalent Crystal Circuit



(b) RC Oscillator Connection



(c) External Clock Source Connections

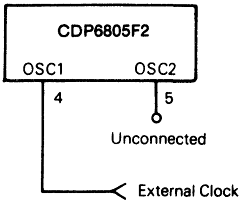


Fig. 7 - Oscillator connections.

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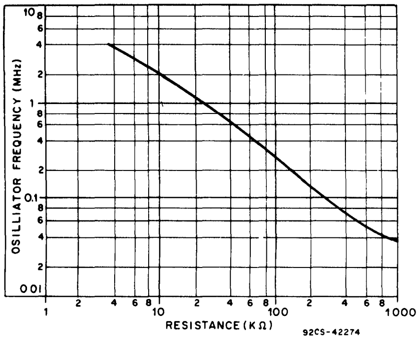

R (kΩ)

Fig. 8 - Typical frequency vs. resistance for RC oscillator option only.

PB0-PB7

These eight lines comprise Port B. The state of any pin is software programmable. Refer to the Input/Output Programming section for a detailed description.

PC0-PC3

These four lines comprise Port C, a fixed input port. When Port C is read, the four most-significant bits on the data bus are "1s". There is no data direction register associated with Port C.

INPUT/OUTPUT PROGRAMMING

Any Port A or B pin may be software programmed as an input or output by the state of the corresponding bit in the port data direction register (DDR). A pin is configured as an output if its corresponding DDR bit is set to a logic "1". A pin is configured as an input if its corresponding DDR bit is cleared to a logic "0". At reset, all DDRs are cleared, which configures all port pins as inputs. A port pin configured as an output will output the data in the corresponding bit of its port data latch. Refer to Figure 9 and Table 2.

(a)

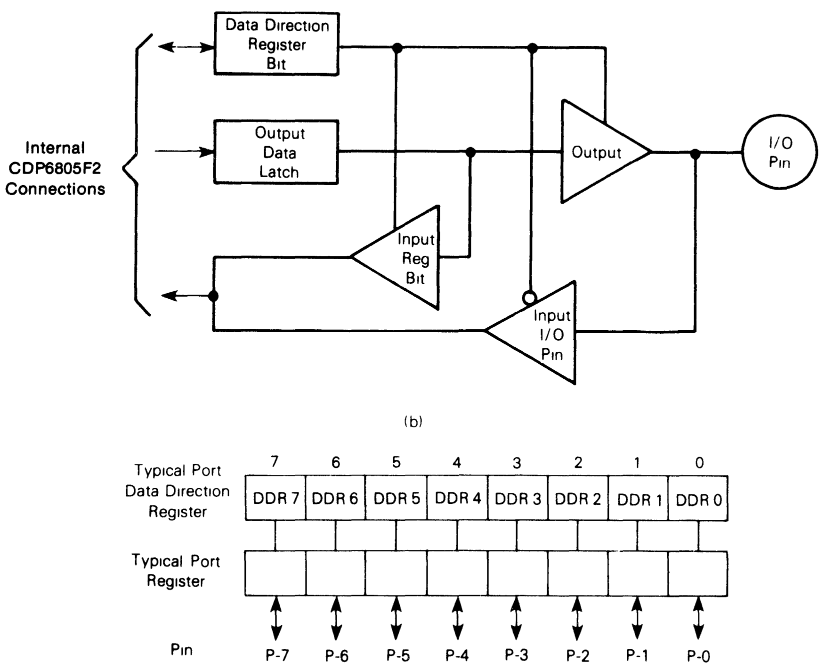

Fig. 9 - Typical I/O port circuitry.

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TABLE 2 — I/O PIN FUNCTIONS

R/$\overline{W}$	DDR	I/O Pin Function
0	0	The I/O pin is in input mode. Data is written into the output data latch
0	1	Data is written into the output data latch and output to the I/O pin
1	0	The state of the I/O pin is read
1	1	The I/O pin is in an output mode. The output data latch is read

CDP6805F2, CDP6805F2C

SELF-CHECK

The **CDP6805F2** self-check is performed using the circuit in Figure 10 Self-check is initiated by tying NUM and TIMER pins to a logic "1" then executing a reset After reset, the following five tests are executed automatically

I/O — Functionally Exercise Ports A, B, C

RAM — Walking Bit Test

ROM — Exclusive OR with ODD "1s" Parity Result

Timer — Functionally Exercise Timer

Interrupts — Functionally Exercise External and Timer Interrupts

Self-check results are shown in Table 3 The following subroutines are available to user programs and do not require any external hardware

TABLE 3 — SELF-CHECK RESULTS

PB3	PB2	PB1	PB0	Remarks
1	0	1	1	Bad Timer
1	1	0	0	Bad RAM
1	1	0	1	Bad ROM
1	1	1	0	Bad Interrupt or Request Flag
All Cycling				Good Part
All Others				Bad Part

RAM SELF-CHECK SUBROUTINE

Returns with the Z bit clear if any error is detected, otherwise, the Z bit is set

The RAM test must be called with the stack pointer at $7F and the accumulator zeroed When run, the test checks every RAM cell except for $7F and $7E which are assumed to contain the return address.

A and X are modified. All RAM locations except the top 2 are modified. (Enter at location $78B.)

ROM CHECKSUM SUBROUTINE

Returns with Z bit cleared if any error was found; otherwise Z = 1, X = 0 on return, and A is zero if the test passed. RAM locations **$41-$44** are overwritten (Enter at location $7A4)

TIMER TEST SUBROUTINE

Return with Z bit cleared if any error was found; otherwise Z = 1

This routine runs a simple test on the timer In order to work correctly as a user subroutine, the internal clock must be the clocking source and interrupts must be disabled. Also, on exit, the clock will be running and the interrupt mask will not be set, so the caller must protect himself from interrupts if necessary

A and X register contents are lost, this routine counts how many times the clock counts in 128 cycles. The number of counts should be a power of two since the prescaler is a power of two If not, the timer probably is not counting correctly The routine also detects if the timer is running at all. (Enter at location $7BE)

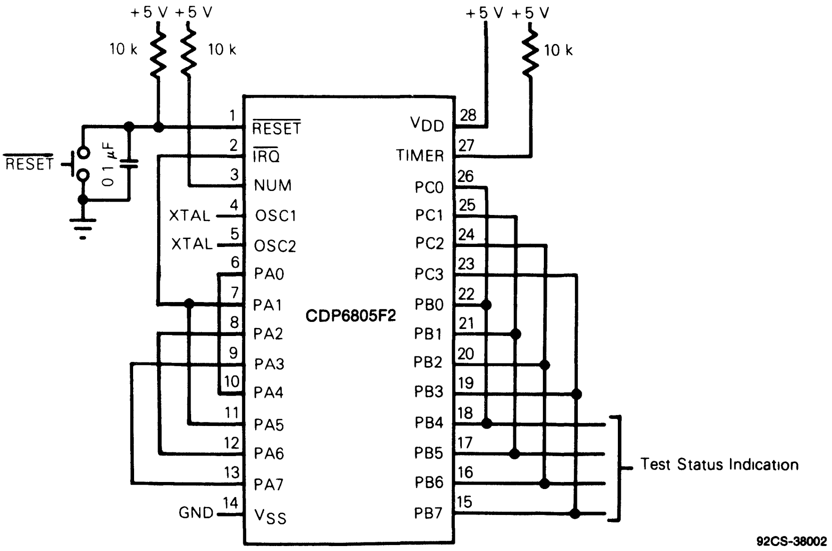


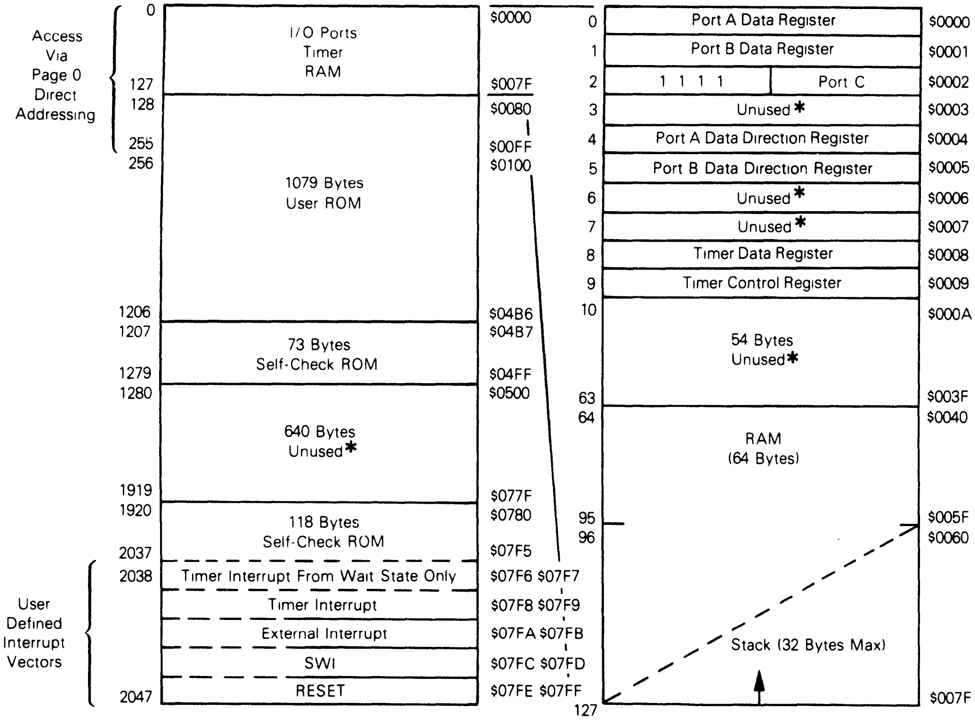
Fig. 10 - Self-check pinout configuration.

MEMORY

The **CDP6805F2** has a total address space of 2048 bytes of memory and I/O registers. The address space is shown in Figure 11.

The first 128 bytes of memory (first half of page zero) is comprised of the I/O port locations, timer locations, and 64 bytes of RAM. The next 1079 bytes comprise the user ROM. The 10 highest address bytes contain the reset and interrupt vectors

The stack pointer is used to address data stored on the stack. Data is stored on the stack during interrupts and subroutine calls. At power-up, the stack pointer is set to $7F and it is decremented as data is pushed on the stack. When data is removed from the stack, the stack pointer is incremented. A maximum of 32 bytes of RAM are available for stack usage. Since most programs use only a small part of the allocated stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are available for program data storage



* Reads of unused locations undefined

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Fig. 11 - Address map.

REGISTERS

The **CDP6805F2** contains five registers as shown in the programming model (Figure 12) The interrupt stacking order is shown in Figure 13

ACCUMULATOR (A)

This accumulator is an 8-bit general purpose register used to hold operands and results of the arithmetic calculations and data manipulations

INDEX REGISTER (X)

The X register is an 8-bit register which is used during the indexed modes of addressing It provides the 8-bit operand which is used to create an effective address The index register is also used for data manipulations with the read-modify-write type of instructions and as a temporary storage register when not performing addressing operations

PROGRAM COUNTER (PC)

The program counter is an 11-bit register that contains the address of the next instruction to be executed by the processor.

STACK POINTER (SP)

The stack pointer is an 11-bit register containing the address of the next free location on the stack. When accessing memory, the six most-significant bits are appended to the five least-significant register bits to produce an address within the range of $7F to $60. The stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts During external or power-on reset, and during a "reset stack pointer" instruction, the stack pointer is set to its upper limit ($7F). Nested interrupts and/or subroutines may use up to 32 (decimal) locations beyond which the stack pointer "wraps around" and points to its upper limit thereby losing the previously stored information A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five bytes.

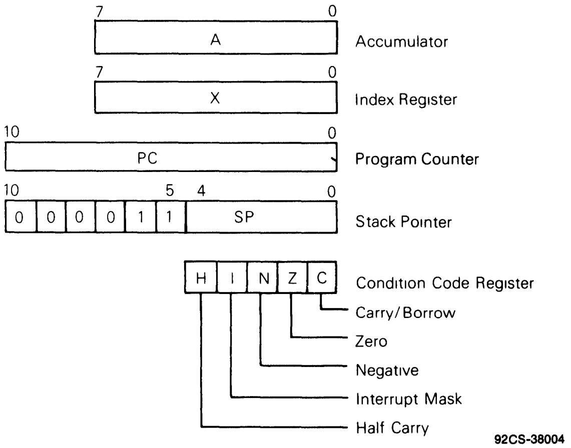
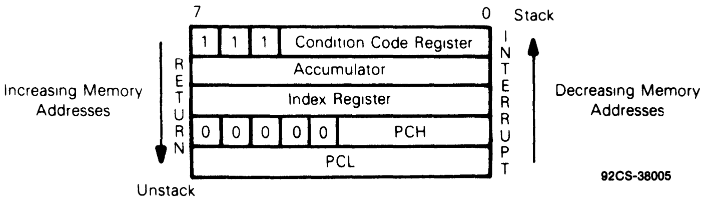


Fig. 12 - Programming model.



NOTE Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc Pulling from the stack is in the reverse order

Fig. 13 - Stacking order.

CONDITION CODE REGISTER (CC)

The condition code register is a 5-bit register which indicates the results of the instruction just executed These bits can be individually tested by a program and specific action taken as a result of their state Each bit is explained in the following paragraphs.

HALF CARRY BIT (H) – The H bit is set to a "1" when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction The H bit is useful in binary coded decimal subroutines

INTERRUPT MASK BIT (I) – When the I bit is set, both the external interrupt and the timer interrupt are disabled Clearing this bit enables the above interrupts If an interrupt occurs while the I bit is set, the interrupt is latched and is processed when the I bit is next cleared

NEGATIVE (N) – Indicates that the result of the last arithmetic, logical, or data manipulation is negative (bit 7 in the result is a logical "1")

ZERO (Z) – Indicates that the result of the last arithmetic, logical, or data manipulation is zero

CARRY/BORROW (C) – Indicates that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation This bit is also affected during bit test and branch instructions, shifts, and rotates

RESETS

The **CDP6805F2** has two reset modes an active low external reset pin ($\overline{\text{RESET}}$) and a power-on reset function, refer to Figure 5

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ input pin is used to reset the MCU to provide an orderly software start-up procedure When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one t_{RL} The $\overline{\text{RESET}}$ pin is provided with a Schmitt Trigger input to improve its noise immunity.

POWER-ON RESET

The power-on reset occurs when a positive transition is detected on V_{DD} The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage There is no provision for a power-down reset The power-on circuitry provides for a 1920 t_{cyc} delay from the time of the first oscillator operation If the external $\overline{\text{RESET}}$ pin is low at the end of the 1920 time out, the processor remains in the reset condition.

Either of the two types of reset conditions causes the following to occur

- Timer control register interrupt request bit (TCR7) is cleared to a "0"
- Timer control register interrupt mask bit (TCR6) is set to a "1"
- All data direction register bits are cleared to a "0" All ports are defined as inputs
- Stack pointer is set to $7F
- The internal address bus is forced to the reset vector ($7FE, $7FF).
- Condition code register interrupt mask bit (I) is set to a "1"
- STOP and WAIT latches are reset
- External interrupt latch is reset

All other functions, such as other registers (including output ports), the timer, etc , are not cleared by the reset conditions

INTERRUPTS

Systems often require that normal processing be interrupted so that some external event may be serviced The **CDP6805F2** may be interrupted by one of three different methods, either one of two maskable interrupts (external input or timer) or a non-maskable software interrupt (SWI)

Interrupts cause the processor registers to be saved on the stack and the interrupt mask set to prevent additional interrupts The RTI instruction causes the register contents to be recovered from the stack and return to normal processing The stacking order is shown in Figure 13

Unlike $\overline{\text{RESET}}$, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction execution is complete

When the current instruction is complete, the processor checks all pending hardware interrupts and if unmasked, proceeds with interrupt processing, otherwise, the next instruction is fetched and executed Note that masked interrupts are latched for later interrupt service

If both an external interrupt and a timer interrupt are pending at the end of an instruction execution, the external interrupt is serviced first The SWI is executed as any other instruction Refer to Figure 14 for the interrupt and instruction processing sequence

CDP6805F2, CDP6805F2C

TIMER INTERRUPT

Each time the timer decrements to zero (transitions from \$01 to \$00), the timer interrupt request bit (TCR7) is set. The processor is interrupted only if the timer mask bit (TCR6) and interrupt mask bit (I bit) are both cleared. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This mask prevents further interrupts until the present one is serviced. The processor now vectors to the timer interrupt service routine. The address for this service routine is specified by the contents of \$7F8 and \$7F9 unless the processor is in a WAIT mode, in which case the contents of \$7F6 and \$7F7 specify the timer service routine address. Software must be used to clear the timer interrupt request bit (TCR7). At the end of the timer interrupt service routine, the software normally executes an RTI instruction which restores the machine state and starts executing the interrupted program.

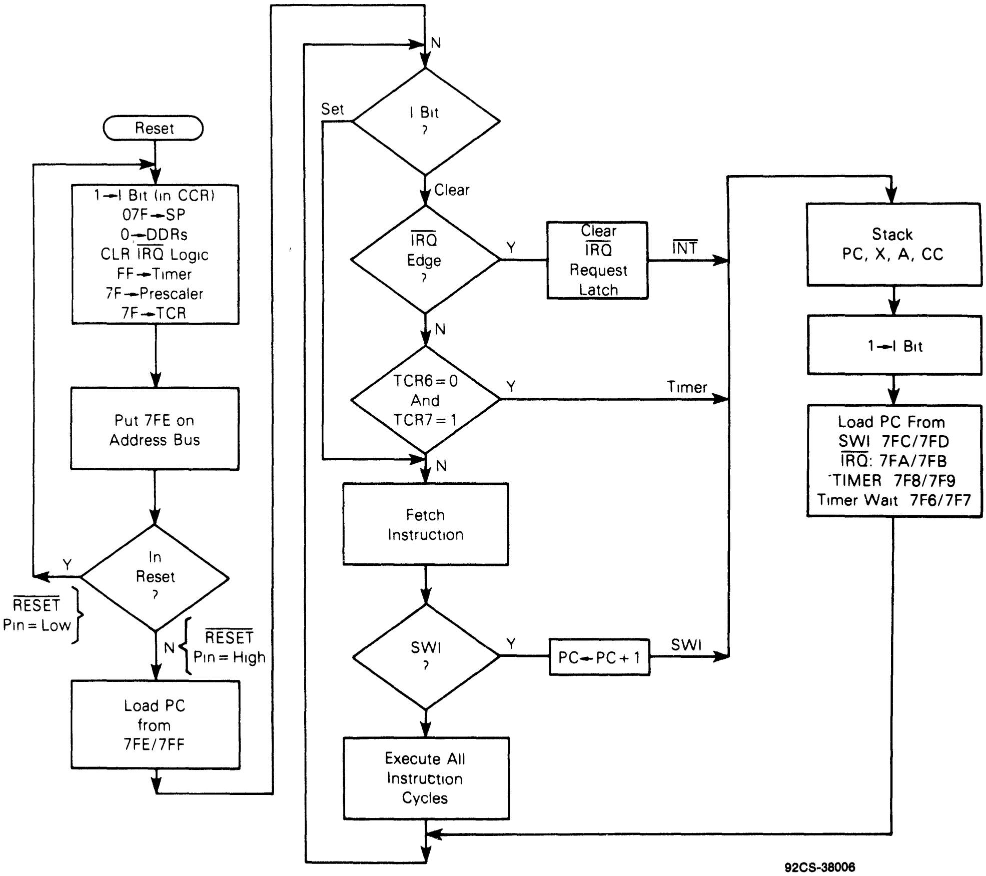


Fig. 14 - RESET and INTERRUPT processing flowchart.

CDP6805F2, CDP6805F2C

EXTERNAL INTERRUPT

Either level- and edge-sensitive or edge-sensitive only inputs are available as mask options. If the interrupt mask bit of the condition code register is cleared and the external interrupt pin ($\overline{IRQ}$) is "low" or a negative edge has set the internal interrupt flip-flop, then the external interrupt occurs. The action of the external interrupt is identical to the timer except that the service routine address is specified by the contents of \$7FA and \$7FB. Figure 15 shows both a functional diagram and timing for the interrupt line. The timing diagram shows two different treatments of the interrupt line ($\overline{IRQ}$) to the processor. The first method is single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the length of the interrupt service routine. Once a pulse occurs, the next pulse should not occur until the MPU software has exited the routine (an RTI occurs). This time (t_{ILIL}) is obtained by adding 20 instruction cycles (t_{cyc}) to the total number of cycles it takes to complete the service routine including the RTI instruction; refer to Figure 15. The second configuration shows many interrupt lines "wire ORed" to form the interrupts at the processor. Thus, if after servicing an interrupt the $\overline{IRQ}$ remains low, then the next interrupt is recognized.

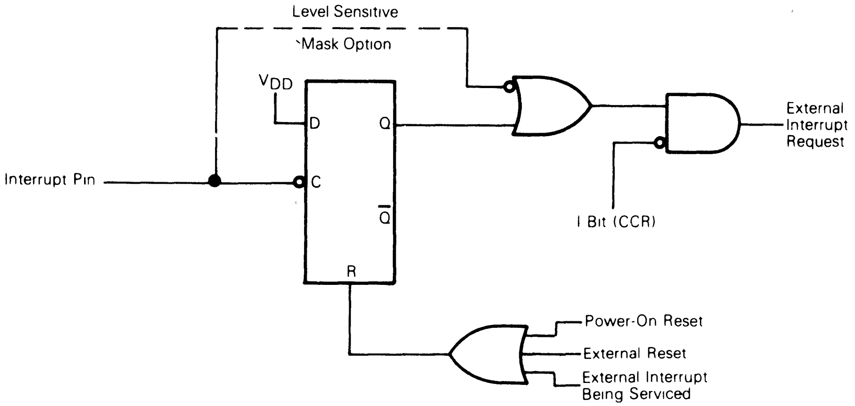
SOFTWARE INTERRUPT (SWI)

The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask in the condition code register. The service routine address is specified by the contents of memory locations \$7FC and \$7FD.

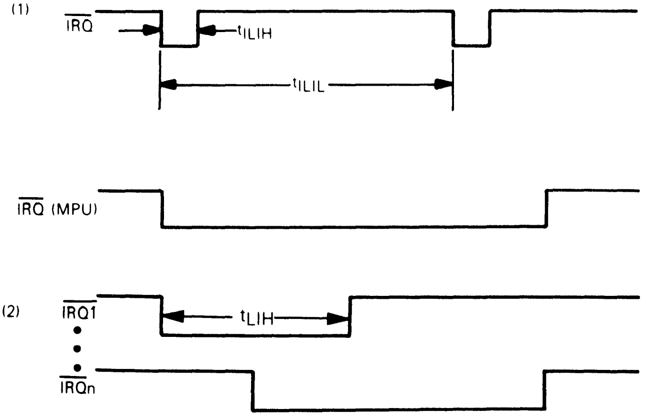
The following three functions are not strictly interrupts, however, they are tied very closely to the interrupts. These functions are $\overline{RESET}$, STOP, and WAIT.

$\overline{RESET}$ – The $\overline{RESET}$ input pin and the internal power-on reset function each cause the program to vector to an initialization program. This vector is specified by the contents

(a) Interrupt Functional Diagram



(b) Interrupt Mode Diagram



Edge Condition

The minimum pulse width (t_{ILIH}) is one t_{cyc}. The period t_{ILIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routine plus 20 t_{cyc} cycles.

Mask Optional Level Sensitive

If after servicing an interrupt the $\overline{IRQ}$ remains low, then the next interrupt is recognized.

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Fig. 15 - External interrupt.

of memory locations $7FE and $7FF The interrupt mask of the condition code register is also set. See preceding section on Reset for details.

STOP – The STOP instruction places the **CDP6805F2** in its lowest power consumption mode In the STOP function, the internal oscillator is turned off causing all internal processing and the timer to be halted; refer to Figure 16

During the STOP mode, timer control register (TCR) bits 6 and 7 are altered to remove any pending timer interrupt requests and to disable any further timing interrupts. External interrupts are enabled in the condition code register. All other registers and memory remain unaltered All I/O lines remain unchanged The processor can only be brought out of the STOP mode by an external $\overline{\text{IRQ}}$ or $\overline{\text{RESET}}$.

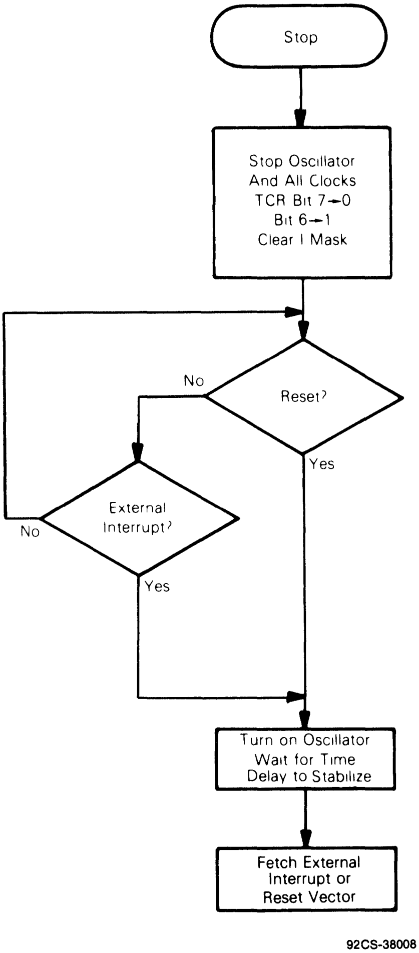

Stop
Stop Oscillator And All Clocks TCR Bit 7→0 Bit 6→1 Clear I Mask
No
Reset?
Yes
No
External Interrupt?
Yes
Turn on Oscillator Wait for Time Delay to Stabilize
Fetch External Interrupt or Reset Vector
92CS-38008

Fig. 16 - Stop function flowchart.

WAIT – The WAIT instruction places the **CDP6805F2** in a low-power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode. In the WAIT mode, the internal clock is disabled from all internal circuitry except the timer circuit; refer to Figure 17. Thus, all internal processing is halted, however, the timer continues to count normally.

During the WAIT mode, the I bit in the condition code register is cleared to enable interrupts. All other registers, memory, and I/O lines remain in their last state. The timer may be enabled by software prior to entering the WAIT mode to allow a periodic exit from the WAIT mode. If an external and a timer interrupt occur at the same time, the external interrupt is serviced first; then, if the timer interrupt request is not cleared in the external interrupt routine, the normal timer interrupt (not the timer WAIT interrupt) is serviced since the MCU is no longer in the WAIT mode.

TIMER

The MCU timer contains an 8-bit software programmable counter with a 7-bit software selectable prescaler. Figure 18 contains a block diagram of the timer. The counter may be preset under program control and decrements towards zero. When the counter decrements to zero, the timer interrupt request bit (i.e , bit 7 of the timer control register (TCR)) is set. Then, if the timer interrupt is not masked (i.e., bit 6 of the TCR and the I bit in the condition code register are both cleared) the processor receives an interrupt. After completion of the current instruction, the processor proceeds to store the appropriate registers on the stack and then fetches the timer vector address from locations $7F8 and $7F9 (or $7F6 and $7F7 if in the WAIT mode) in order to begin servicing

The counter continues to count after it reaches zero allowing the software to determine the number of internal or external input clocks since the timer interrupt request bit was set The counter may be read at any time by the processor without disturbing the count The contents of the counter become stable, prior to the read portion of a cycle, and do not change during the read. The timer interrupt request bit remains set until cleared by the software. TCR7 may also be used as a scanned status bit in a non-interrupt mode of operation (TCR6 = 1).

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer. Bit 0, bit 1, and bit 2 of the TCR are programmed to choose the appropriate prescaler output within the range of ÷ 1 to ÷ 128 which is used as the counter input. The processor cannot write into or read from the prescaler, however, its contents are cleared to all "0s" by the write operation into TCR when bit 3 of the written data equals one. This allows for truncation-free counting.

The timer input can be configured for three different operating modes plus a disable mode depending on the value written to the TCR4 and TCR5 control bits. Refer to the Timer Control Register section.

TIMER INPUT MODE 1

If TCR5 and TCR4 are both programmed to a "0", the input to the timer is from an internal clock and the TIMER input pin is disabled. The internal clock mode can be used for

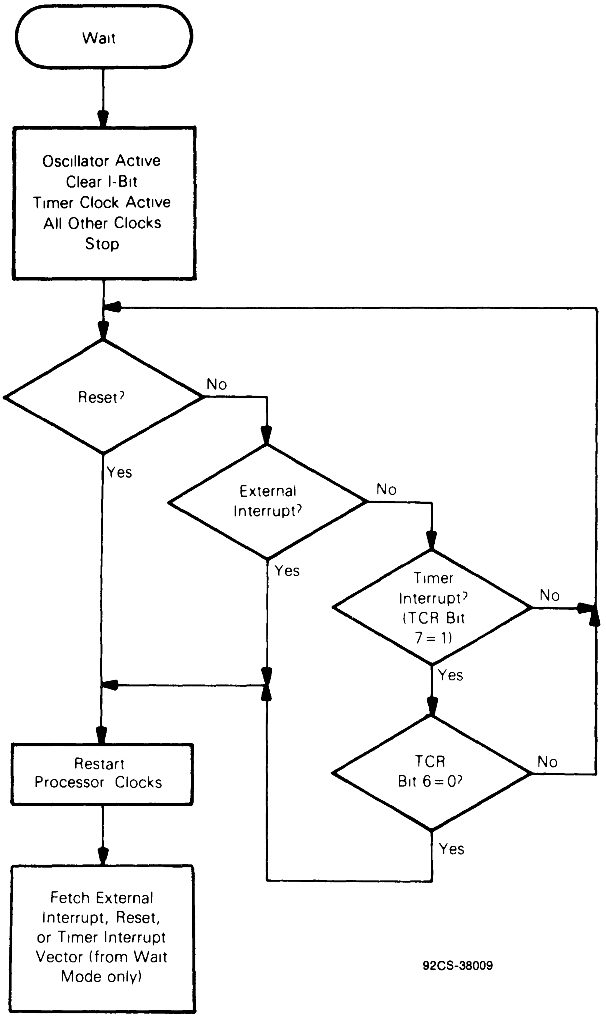


Fig. 17 - WAIT function flowchart.

periodic interrupt generation as well as a reference in frequency and event measurement The internal clock is the instruction cycle clock During a WAIT instruction, the internal clock to the timer continues to run at its normal rate

TIMER INPUT MODE 2

With TCR5=0 and TCR4=1, the internal clock and the TIMER input pin are ANDed to form the timer input signal. This mode can be used to measure external pulse widths The external timer input pulse simply turns on the internal clock for the duration of the pulse The resolution of the count in this mode is ± one internal clock and therefore, accuracy improves with longer input pulse widths

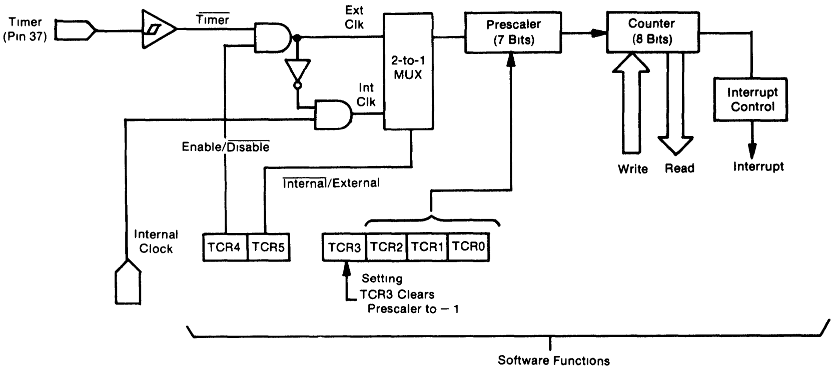
TIMER INPUT MODE 3

If TCR5=1 and TCR4=0, all inputs to the timer are disabled

TIMER INPUT MODE 4

If TCR5=1 and TCR4=1, the internal clock input to the timer is disabled and the TIMER input pin becomes the input to the timer The timer can, in this mode, be used to count external events as well as external frequencies for generating periodic interrupts The counter is clocked on the falling edge of the external signal

Figure 18 shows a block diagram of the timer subsystem Power-on reset and the STOP instruction invalidate the contents of the counter



NOTES
1 Prescaler and 8-bit counter are clocked falling edge of the internal clock (AS) or external input
2 Counter is written to during Data Strobe (DS) and counts down continuously

92CM-38034R1

Fig. 18 - Programmable timer/counter block diagram.

TIMER CONTROL REGISTER (TCR)

7	6	5	4	3	2	1	0
TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0

All bits in this register except bit 3 are read/write bits

TCR7 – Timer interrupt request bit bit used to indicate the timer interrupt when it is logic "1"
1 – Set whenever the counter decrements to zero or under program control
0 – Cleared on external $\overline{\text{RESET}}$, power-on reset, STOP instruction, or program control

TCR6 – Timer interrupt mask bit when this bit is a logic "1", it inhibits the timer interrupt to the processor
1 – Set on external $\overline{\text{RESET}}$, power-on reset, STOP instruction, or program control
0 – Cleared under program control

TCR5 – External or internal bit selects the input clock source to be either the external timer pin or the internal clock (Unaffected by $\overline{\text{RESET}}$)
1 – Select external clock source
0 – Select internal clock source

TCR4 – External enable bit control bit used to enable the external TIMER pin (Unaffected by $\overline{\text{RESET}}$)
1 – Enable external TIMER pin
0 – Disable external TIMER pin

TCR5	TCR4	
0	0	Internal Clock to Timer
0	1	AND of Internal Clock and TIMER Pin to Timer
1	0	Inputs to Timer Disabled
1	1	TIMER Pin to Timer

TCR3 – Timer Prescaler Reset bit: writing a "1" to this bit resets the prescaler to zero A read of this location always indicates "0" (Unaffected by $\overline{\text{RESET}}$)

TCR2, TCR1, TCR0 – Prescaler select bits: decoded to select one of eight outputs on the prescaler. (Unaffected by $\overline{\text{RESET}}$)

Prescaler

TCR2	TCR1	TCR0	Result
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	÷128

INSTRUCTION SET

The MCU has a set of 61 basic instructions. They can be divided into five different types: register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

REGISTER/MEMORY INSTRUCTIONS

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The operand for the jump unconditional (JMP) and jump to subroutine (JSR) instructions is the program counter. Refer to Table 4.

READ-MODIFY-WRITE INSTRUCTIONS

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read-modify-write sequence since it does not modify the value Refer to Table 5

BRANCH INSTRUCTIONS

Most branch instructions test the state of the condition code register and, if certain criteria are met, a branch is executed. This adds an offset between − 127 and + 128 to the current program counter. Refer to Table 6

BIT MANIPULATION INSTRUCTIONS

The MCU is capable of setting or clearing any bit which resides in the first 128 bytes of the memory space where all port registers, port DDRs, timer, timer control, and on-chip RAM reside. An additional feature allows the software to test and branch on the state of any bit within the first 256 locations. The bit set, bit clear, and bit test and branch functions are implemented with a single instruction For the test and branch instructions, the value of the bit tested is also placed in the carry bit of the condition code register Refer to Table 7

CONTROL INSTRUCTIONS

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 8.

OPCODE MAP

Table 9 is an opcode map for the instructions used on the MCU

ALPHABETICAL LISTING

The complete instruction set is given in alphabetical order in Table 10

ADDRESSING MODES

The MCU uses ten different addressing modes to provide the programmer with an opportunity to optimize the code to all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables, and scaling tables anywhere in the memory space. Short indexed accesses are single-byte instructions while the longest instructions (three bytes) permit tables throughout memory Short and long absolute addressing is also included Two-byte direct addressing instructions access all data bytes in most applications Extended addressing permits jump instructions to reach all memory. Table 10 shows the addressing modes for each instruction with the effects each instruction has on the condition code register An opcode map is shown in Table 9

The term "Effective Address" (EA) is defined as the byte address to or from which the argument for an instruction is fetched or stored The ten addressing modes of the processor are described below Parentheses are used to indicate "contents of," an arrow indicates "is replaced by," and a colon indicates "concatenation of two bytes."

INHERENT

In inherent instructions, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index registers or accumulator and no other arguments are included in this mode.

IMMEDIATE

In immediate addressing, the operand is contained in the byte immediately following the opcode. Immediate addressing is used to access constants which do not change during program execution (e g , a constant used to initialize a loop counter).

$$EA = PC + 1;\ PC \leftarrow PC + 2$$

DIRECT

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction. This includes all on-chip RAM and I/O registers and 128 bytes of on-chip ROM Direct addressing is efficient in both memory and time

$$EA = (PC + 1),\ PC + PC + 2$$

$$\text{Address Bus High} \leftarrow 0,\ \text{Address Bus Low} \leftarrow (PC + 1)$$

EXTENDED

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode Instructions with extended addressing modes are capable of referencing arguments anywhere in memory with a single three-byte instruction

$$EA = (PC + 1){:}(PC + 2);\ PC \leftarrow PC + 3$$

$$\text{Address Bus High} \leftarrow (PC + 1),\ \text{Address Bus Low} \leftarrow (PC + 2)$$

INDEXED, NO-OFFSET

In the indexed, no-offset addressing mode, the effective address of the argument is contained in the 8-bit index register Thus, this addressing mode can access the first 256 memory locations These instructions are only one byte long. This mode is used to move a pointer through a table or to address a frequently referenced RAM or I/O location.

$$EA = X,\ PC \leftarrow PC + 1$$

$$\text{Address Bus High} \leftarrow 0;\ \text{Address Bus Low} \leftarrow X$$

INDEXED, 8-BIT OFFSET

Here the EA is obtained by adding the contents of the byte following the opcode to that of the index register, therefore, the operand is located anywhere within the lowest 511 memory locations For example, this mode of addressing is useful for selecting the mth element in an n element table. All instructions are two bytes. The content of the index register

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(X) is not changed The content of (PC+1) is an unsigned 8-bit integer One-byte offset indexing permits look-up tables to be easily accessed in either RAM or ROM.

$$EA = X + (PC+1);\ PC \leftarrow PC+2$$

Address Bus High ← K, Address Bus Low ← X + (PC + 1)

where K = The carry from the addition of X + (PC + 1)

INDEXED, 16-BIT OFFSET

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode This addressing mode can be used in a manner similar to indexed 8-bit offset, except that this three-byte instruction allows tables to be anywhere in memory (e.g., jump tables in ROM). The content of the index register is not changed.

$$EA = X + [(PC+1)\ (PC+2)];\ PC \leftarrow PC+3$$

Address Bus High ← (PC + 1) + K,

Address Bus Low ← X + (PC + 2)

where K = The carry from the addition of X + (PC + 2)

RELATIVE

Relative addressing is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte following the opcode (the offset) is added to the PC if and only if the branch condition is true Otherwise, control proceeds to the next instruction The span of relative addressing is limited to the range of − 126 to + 129 bytes from the branch instruction opcode location

$$EA = PC + 2 + (PC+1);\ PC \leftarrow EA \text{ if branch taken; otherwise, } PC \leftarrow PC+2$$

BIT SET/CLEAR

Direct addressing and bit addressing are combined in instructions which set and clear individual memory and I/O bits. In the bit set and clear instructions, the byte is specified as a direct address in the location following the opcode. The first 128 addressable locations are thus accessed. The bit to be modified within that byte is specified with three bits of the opcode. The bit set and clear instructions occupy two bytes: one for the opcode (including the bit number) and the second for addressing the byte which contains the bit of interest.

$$EA = (PC+1);\ PC \leftarrow PC+2$$

Address Bus High ← 0; Address Bus Low ← (PC + 1)

BIT TEST AND BRANCH

Bit test and branch is a combination of direct addressing, bit addressing, and relative addressing. The bit address and condition (set or clear) to be tested is part of the opcode. The address of the byte to be tested is in the single byte immediately following the opcode byte (EA1). The signed relative 8-bit offset is in the third byte (EA2) and is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any bit in the first 256 locations of memory.

$$EA1 = (PC+1)$$

Address Bus High ← 0; Address Bus Low ← (PC + 1)

$$EA2 = PC + 3 + (PC+2);\ PC \leftarrow EA2 \text{ if branch taken; otherwise, } PC \leftarrow PC+3$$

TABLE 4 — REGISTER/MEMORY INSTRUCTIONS

		Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from Memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in Memory	STA	–	–	–	B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in Memory	STX	–	–	–	BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add Memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add Memory and Carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract Memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND Memory to A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR Memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump Unconditional	JMP	–	–	–	BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to Subroutine	JSR	–	–	–	BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

TABLE 5 — READ-MODIFY-WRITE INSTRUCTIONS

		Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (2's Complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate Left Thru Carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate Right Thru Carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical Shift Left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical Shift Right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic Shift Right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for Negative or Zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5

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TABLE 6 — BRANCH INSTRUCTIONS

		Relative Addressing Mode		
Function	Mnemonic	Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	3
Branch Never	BRN	21	2	3
Branch IFF Higher	BHI	22	2	3
Branch IFF Lower or Same	BLS	23	2	3
Branch IFF Carry Clear	BCC	24	2	3
(Branch IFF Higher or Same)	(BHS)	24	2	3
Branch IFF Carry Set	BCS	25	2	3
(Branch IFF Lower)	(BLO)	25	2	3
Branch IFF Not Equal	BNE	26	2	3
Branch IFF Equal	BEQ	27	2	3
Branch IFF Half Carry Clear	BHCC	28	2	3
Branch IFF Half Carry Set	BHCS	29	2	3
Branch IFF Plus	BPL	2A	2	3
Branch IFF Minus	BMI	2B	2	3
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	3
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	3
Branch IFF Interrupt Line is Low	BIL	2E	2	3
Branch IFF Interrupt Line is High	BIH	2F	2	3
Branch to Subroutine	BSR	AD	2	6

TABLE 7 — BIT MANIPULATION INSTRUCTIONS

		Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is Set	BRSET n (n=0 7)	–	–	–	2•n	3	5
Branch IFF Bit n is Clear	BRCLR n (n=0 7)	–	–	–	01+2•n	3	5
Set Bit n	BSET n (n=0 7)	10+2•n	2	5	–	–	–
Clear Bit n	BCLR n (n=0 7)	11+2•n	2	5	–	–	–

TABLE 8 — CONTROL INSTRUCTIONS

		Inherent		
Function	Mnemonic	Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	10
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

TABLE 9— INSTRUCTION SET OPCODE MAP

	Bit Manipulation		Branch	Read-Modify-Write					Control		Register/Memory						
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
Hi / Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Hi / Low
0 0000	5 BRSET0 3 BTB	5 BSET0 2 BSC	3 BRA 2 REL	5 NEG 2 DIR	3 NEG 1 INH	3 NEG 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0 0000
1 0001	5 BRCLR0 3 BTB	5 BCLR0 2 BSC	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1 0001
2 0010	5 BRSET1 3 BTB	5 BSET1 2 BSC	3 BHI 2 REL								2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2 0010
3 0011	5 BRCLR1 3 BTB	5 BCLR1 2 BSC	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3 0011
4 0100	5 BRSET2 3 BTB	5 BSET2 2 BSC	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4 0100
5 0101	5 BRCLR2 3 BTB	5 BCLR2 2 BSC	3 BCS 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5 0101
6 0110	5 BRSET3 3 BTB	5 BSET3 2 BSC	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6 0110
7 0111	5 BRCLR3 3 BTB	5 BCLR3 2 BSC	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7 0111
8 1000	5 BRSET4 3 BTB	5 BSET4 2 BSC	3 BHCC 2 REL	5 LSL 2 DIR	3 LSLA 1 INH	3 LSLX 1 INH	6 LSL 2 IX1	5 LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8 1000
9 1001	5 BRCLR4 3 BTB	5 BCLR4 2 BSC	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9 1001
A 1010	5 BRSET5 3 BTB	5 BSET5 2 BSC	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A 1010
B 1011	5 BRCLR5 3 BTB	5 BCLR5 2 BSC	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B 1011
C 1100	5 BRSET6 3 BTB	5 BSET6 2 BSC	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C 1100
D 1101	5 BRCLR6 3 BTB	5 BCLR6 2 BSC	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D 1101
E 1110	5 BRSET7 3 BTB	5 BSET7 2 BSC	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E 1110
F 1111	5 BRCLR7 3 BTB	5 BCLR7 2 BSC	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F 1111

Abbreviations for Address Modes

INH	Inherent
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
BTB	Bit Test and Branch
IX	Indexed (No Offset)
IX1	Indexed, 1 Byte (8-Bit) Offset
IX2	Indexed, 2 Byte (16-Bit) Offset

LEGEND

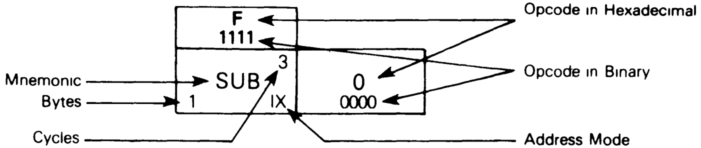

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TABLE 10 — INSTRUCTION SET

Mnemonic	Addressing Modes										Condition Codes				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/ Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
ADD		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
AND		X	X	X		X	X	X			●	●	Λ	Λ	●
ASL	X		X			X	X				●	●	Λ	Λ	Λ
ASR	X		X			X	X				●	●	Λ	Λ	Λ
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	Λ	Λ	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	Λ
BRSET										X	●	●	●	●	Λ
BSET									X		●	●	●	●	●
BSR					X						●	●	●	●	●
CLC	X										●	●	●	●	0
CLI	X										●	0	●	●	●
CLR	X		X			X	X				●	●	0	1	●
CMP		X	X	X		X	X	X			●	●	Λ	Λ	Λ
COM	X		X			X	X				●	●	Λ	Λ	1
CPX		X	X	X		X	X	X			●	●	Λ	Λ	Λ
DEC	X		X			X	X				●	●	Λ	Λ	●
EOR		X	X	X		X	X	X			●	●	Λ	Λ	●
INC	X		X			X	X				●	●	Λ	Λ	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	Λ	Λ	●
LDX		X	X	X		X	X	X			●	●	Λ	Λ	●
LSL	X		X			X	X				●	●	Λ	Λ	Λ
LSR	X		X			X	X				●	●	0	Λ	Λ
NEG	X		X			X	X				●	●	Λ	Λ	Λ
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	Λ	Λ	●
ROL	X		X			X	X				●	●	Λ	Λ	Λ
ROR	X		X			X	X				●	●	Λ	Λ	Λ
RSP	X										●	●	●	●	●
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	Λ	Λ	●
STOP	X										●	0	●	●	●
STX			X	X		X	X	X			●	●	Λ	Λ	●
SUB		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	Λ	Λ	●
TXA	X										●	●	●	●	●
WAIT	X										●	0	●	●	●

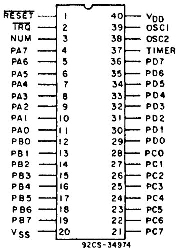
Condition Code Symbols

H	Half Carry (From Bit 3)	Λ	Test and Set if True Cleared Otherwise
I	Interrupt Mask	●	Not Affected
N	Negative (Sign Bit)	?	Load CC Register From Stack
Z	Zero	0	Cleared
C	Carry/Borrow	1	Set

Product Preview

CDP6805G2, CDP6805G2C

TERMINAL ASSIGNMENT



TOP VIEW

CMOS High-Performance Silicon-Gate 8-Bit Microcomputer

Features:

- *Typical full speed operating power of 12 mW at 5 V*
- *Typical WAIT mode power of 4 mW*
- *Typical STOP mode power of 5 μW*
- *Fully static operation*
- *112 bytes of on-chip RAM*
- *2106 bytes of on-chip ROM*
- *32 bidirectional I/O lines*
- *High current drive*
- *Internal 8-bit timer with software programmable 7-bit prescaler*
- *External timer input*
- *External and timer interrupts*
- *Self-check mode*
- *Master reset and power-on reset*
- *Single 3 to 6 volt supply*
- *On-chip oscillator with RC or crystal mask options*
- *True bit manipulation*
- *Addressing modes with indexed addressing for tables*

The CDP6805G2 Microcomputer Unit (MCU) belongs to the CDP6805 Family of Microcomputers This 8-bit MCU contains on-chip oscillator CPU, RAM, ROM, I/O, and Timer. The fully static design allows operation at frequencies down to DC, further reducing its already low-power consumption. It is a low-power processor designed for low-end to mid-range applications in the consumer, automotive, industrial, and communications markets where very low power consumption constitutes an important factor.

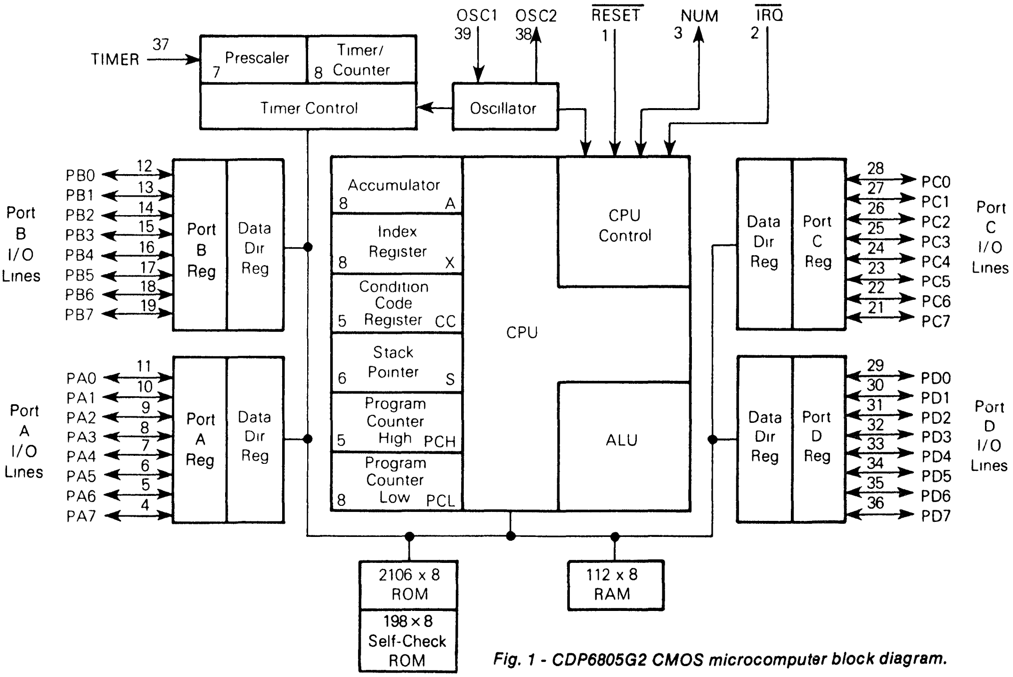


Fig. 1 - CDP6805G2 CMOS microcomputer block diagram.

CDP6805G2, CDP6805G2C

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +8	V
All Input Voltages Except OSC1	V_{in}	V_{SS}-0.5 to V_{DD}+0.5	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range CDP6805G2 CDP6805G2C	T_A	T_L T_H 0 to +70 -40 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Current Drain Total (PD4-PD7 only)	I_{OH}	40	mA

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance Plastic Ceramic	– θ_{JA}	100 50	– °C/W

This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs except OSC2 and NUM are tied to an appropriate logic voltage level (e g., either V_{SS} or V_{DD}).

Port	R_1	R_2
B and C	24.3 kΩ	4.32 kΩ
A, PD0-PD3	1.21 kΩ	3.1 kΩ
PD4-PD7	300 Ω	1.64 kΩ

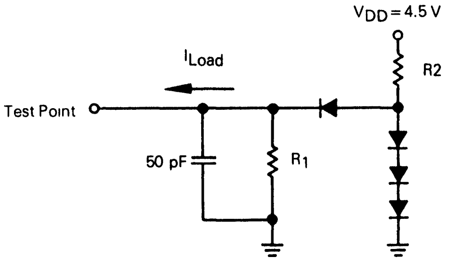


Fig. 2 - Equivalent test load.

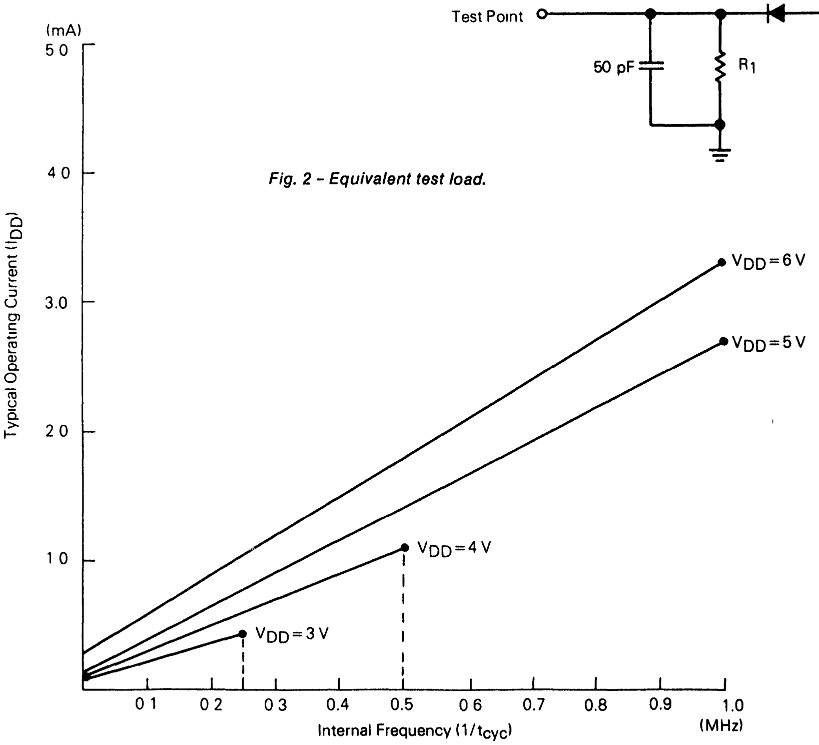


Fig. 3 - Typical operating current vs. internal frequency.

CDP6805G2, CDP6805G2C

DC ELECTRICAL CHARACTERISTICS (V_{DD}=3 Vdc, V_{SS}=0 Vdc, $T_A=T_L$ to T_H, unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Output Voltage $I_{Load} \le 1\ \mu A$	V_{OL}	–	0.1	V
	V_{OH}	$V_{DD}-0.1$	–	V
Output High Voltage (I_{Load} = – 50 μA) PB0-PB7, PC0-PC7	V_{OH}	1.4	–	V
(I_{Load} = -0.5 mA) PA0-PA7, PD0-PD3	V_{OH}	1.4	–	V
(I_{Load} = -2 mA) PD4-PD7	V_{OH}	1.4	–	V
Output Low Voltage (I_{Load} = 300 μA) All Ports PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	V_{OL}	–	0.3	V
Input High Voltage Ports PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	V_{IH}	2.7	V_{DD}	V
TIMER, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$	V_{IH}	2.7	V_{DD}	V
OSC1	V_{IH}	2.7	V_{DD}	V
Input Low Voltage All Inputs	V_{IL}	V_{SS}	0.3	V
Total Supply Current (no dc Loads, t_{cyc}=5 μs) RUN (measured during self-check, V_{IL}=0.1 V, $V_{IH}=V_{DD}$-0.1 V)	I_{DD}	–	0.5	mA
WAIT (See Note)	I_{DD}	–	200	μA
STOP (See Note)	I_{DD}	–	100	μA
I/O Ports Input Leakage PA0-PA7, PB0- PB7, PC0-PC7, PD0-PD7	I_{IL}	–	5	μA
Input Current $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, TIMER, OSC1	I_{in}	–	±1	μA
Capacitance Ports	C_{out}	–	12	pF
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, TIMER, OSC1	C_{in}	–	8	pF

DC ELECTRICAL CHARACTERISTICS (V_{DD}=5 Vdc ± 10%, V_{SS}=0 Vdc, $T_A=T_L$ to T_H, unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Output Voltage $I_{Load} \le 10\ \mu A$	V_{OL}	–	0.1	V
	V_{OH}	$V_{DD}-0.1$	–	V
Output High Voltage (I_{Load} = – 100 μA) PB0-PB7, PC0-PC7	V_{OH}	2.4	–	V
(I_{Load} = – 2 mA) PA0-PA7, PD0-PD3	V_{OH}	2.4	–	V
(I_{Load} = – 8 mA) PD4-PD7	V_{OH}	2.4	–	V
Output Low Voltage (I_{Load} = 800 μA) All Ports PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	V_{OL}	–	0.4	V
Input High Voltage Ports PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	V_{IH}	$V_{DD}-2$	V_{DD}	V
TIMER, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, OSC1	V_{IH}	$V_{DD}-0.8$	V_{DD}	V
Input Low Voltage All Inputs	V_{IL}	V_{SS}	0.8	V
Total Supply Current (C_L = 50 pF on Ports, no dc Loads, t_{cyc} = 1 μs) RUN (measured during self-check, V_{IL} = 0.2 V, $V_{IH}=V_{DD}-0.2$ V)	I_{DD}	–	4	mA
WAIT (See Note)	I_{DD}	–	1.5	mA
STOP (See Note)	I_{DD}	–	150	μA
I/O Ports Input Leakage PA0-PA7, PB0- PB7, PC0-PC7, PD0-PD7	I_{IL}	–	±10	μA
Input Current $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, TIMER, OSC1	I_{in}	–	±1	μA
Capacitance Ports	C_{out}	–	12	pF
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, TIMER, OSC1	C_{in}	–	8	pF

NOTE: Test conditions for I_{DD} are as follows.
All ports programmed as inputs
V_{IL} = 0.2 V (PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7)
$V_{IH}=V_{DD}-0.2$ V for $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, TIMER
OSC1 input is a squarewave from 0.2 V to $V_{DD}-0.2$ V
OSC2 output load = 20 pF (wait I_{DD} is affected linearly by the OSC2 capacitance)

TABLE 1 — CONTROL TIMING

(V_{DD}=5 Vdc ±10%, V_{SS}=0, T_A=T_L to T_H, f_{osc}=4 MHz)

Characteristics	Symbol	Min	Max	Unit
Crystal Oscillator Startup Time (Figure 5)	t_{OXOV}	–	100	ms
Stop Recovery Startup Time (Crystal Oscillator) (Figure 6)	t_{ILCH}	–	100	ms
Timer Pulse Width (Figure 4)	t_{TH}, t_{TL}	0.5	–	t_{cyc}
Reset Pulse Width (Figure 5)	t_{RL}	1.5	–	t_{cyc}
Timer Period (Figure 4)	t_{TLTL}	1	–	t_{cyc}
Interrupt Pulse Width Low (Figure 15)	t_{ILIH}	1	–	t_{cyc}
Interrupt Pulse Period (Figure 15)	t_{ILIL}	*	–	t_{cyc}
OSC1 Pulse Width	t_{OH}, t_{OL}	100	–	ns
Cycle Time	t_{cyc}	1000	–	ns
Frequency of Operation Crystal	f_{osc}	–	4	MHz
External Clock	f_{osc}	DC		MHz

*The minimum period t_{ILIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routines plus 20 t_{cyc} cycles

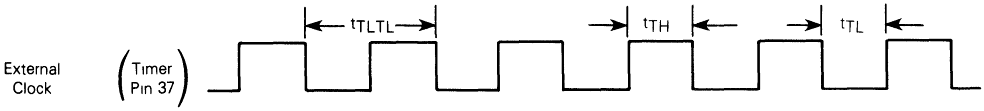
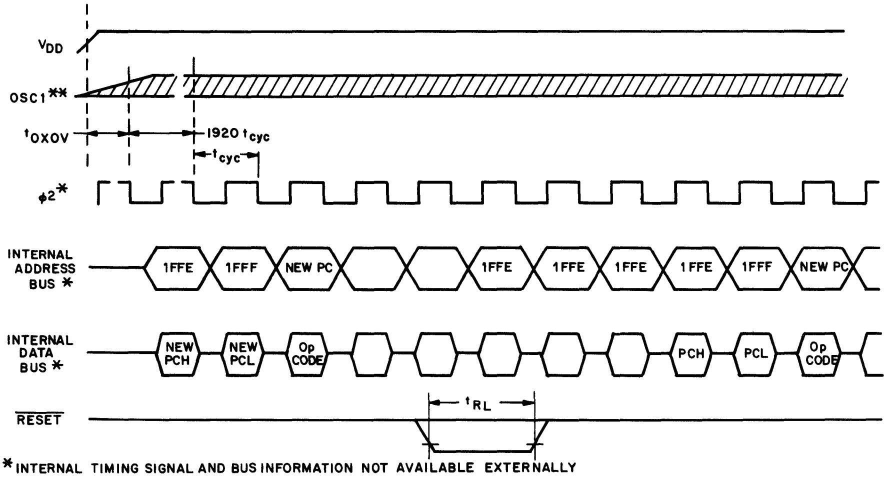


Fig. 4 - Timer relationships.



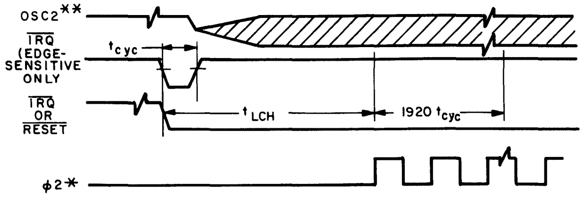
*INTERNAL TIMING SIGNAL AND BUS INFORMATION NOT AVAILABLE EXTERNALLY

**OSC1 LINE IS NOT MEANT TO REPRESENT FREQUENCY.
IT IS ONLY USED TO REPRESENT TIME.

92CM-38103

Fig. 5 - Power-on RESET and $\overline{RESET}$.

CDP6805G2, CDP6805G2C


OSC2**
$\overline{\text{IRQ}}$ (EDGE-SENSITIVE ONLY)
t_{cyc}
$\overline{\text{IRQ}}$ OR $\overline{\text{RESET}}$
t_{LCH}
1920 t_{cyc}
$\phi2$*

* INTERNAL TIMING SIGNALS NOT AVAILABLE EXTERNALLY.

** REPRESENTS THE INTERNAL GATING OF THE OSC1 INPUT PIN.

92CS-38101

Fig. 6 - Stop recovery and power-on RESET.

FUNCTIONAL PIN DESCRIPTION

V_{DD} and V_{SS}

Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is ground.

$\overline{\text{IRQ}}$ (MASKABLE INTERRUPT REQUEST)

$\overline{\text{IRQ}}$ is mask option selectable with the choice of interrupt sensitivity being both level- and negative-edge or negative-edge only.The MCU completes the current instruction before it responds to the request. If $\overline{\text{IRQ}}$ is low and the interrupt mask bit (I bit) in the condition code register is clear, the MCU begins an interrupt sequence at the end of the current instruction.

If the mask option is selected to include level sensitivity, then the $\overline{\text{IRQ}}$ input requires an external resistor to V_{DD} for "wire-OR" operation. See the Interrupt section for more detail

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ input is not required for start-up but can be used to reset the MCU's internal state and provide an orderly software start-up procedure. Refer to the Reset section for a detailed description

TIMER

The TIMER input may be used as an external clock for the on-chip timer Refer to Timer section for a detailed description.

NUM — NON-USER MODE

This pin is intended for use in self-check only User applications should connect this pin to ground through a 10 kΩ resistor

OSC1, OSC2

The CDP6805G2 can be configured to accept either a crystal input or an RC network. Additionally, the internal clocks can be derived by either a divide-by-two or divide-by-four of the external frequency (f_{OSC}). Both of these options are mask selectable.

RC — If the RC oscillator option is selected, then a resistor is connected to the oscillator pins as shown in Figure 7(b) The relationship between R and f_{OSC} is shown in Figure 8.

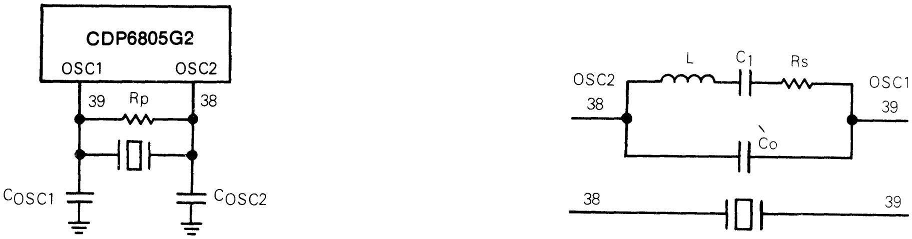
CRYSTAL — The circuit shown in Figure 7(a) is recommended when using a crystal. The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{OSC} in the electrical characteristics table. Using an external CMOS oscillator is suggested when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time Crystal frequency limits are also affected by V_{DD}. Refer to Control Timing Characteristics for limits. See Table 1

EXTERNAL CLOCK — An external clock should be applied to the OSC1 input with the OSC2 input not connected, as shown in Figure 7(c). An external clock may be used with either the RC or crystal oscillator mask option. t_{OXOV} or t_{ILCH} do not apply when using an external clock input.

CDP6805G2, CDP6805G2C

	1 MHz	4 MHz	Units
R_{SMAX}	400	75	Ω
C_0	5	7	pF
C_1	0 008	0 012	µF
C_{OSC1}	15-40	15-30	pF
C_{OSC2}	15-30	15-25	pF
R_P	10	10	MΩ
Q	30	40	–

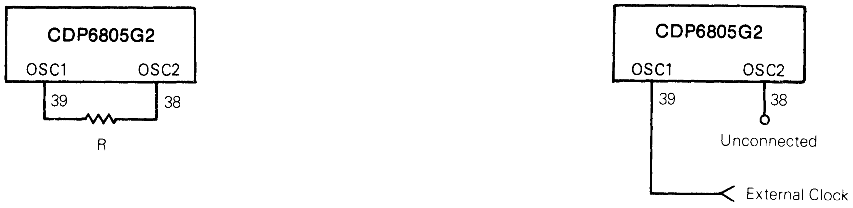
Crystal Parameters



Crystal Oscillator Connections

Equivalent Crystal Circuit

(a)



(b) RC Oscillator Connection

(c) External Clock Source Connections

Fig. 7 - Oscillator connections.

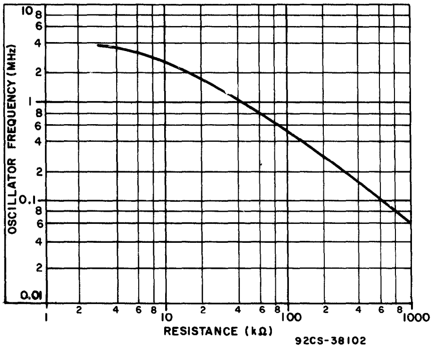


Fig. 8 - Typical frequency vs. resistance for RC oscillator option only.

PA0-PA7

These eight I/O lines comprise Port A The state of any pin is software programmable Refer to Input/Output Programming section for a detailed description

PB0-PB7

These eight lines comprise Port B The state of any pin is software programmable Refer to Input/Output Programming section for a detailed description

PC0-PC7

These eight lines comprise Port C The state of any pin is software programmable Refer to the Input/Output Programming section for a detailed description

PD0-PD7

These eight lines comprise Port D PD4-PD7 also are capable of driving LED's directly. The state of any pin is software programmable. Refer to the Input/Output Programing section for a detailed description

INPUT/OUTPUT PROGRAMMING

Any port pin may be software programmed as an input or output by the state of the corresponding bit in the port Data Direction Register (DDR) A pin is configured as an output if its corresponding DDR bit is set to a logic '1 ' A pin is configured as an input if its corresponding DDR bit is cleared to a logic '0 ' At reset, all DDRs are cleared, which configures all port pins as inputs A port pin configured as an output will output the data in the corresponding bit of its port data latch Refer to Figure 9 and Table 2

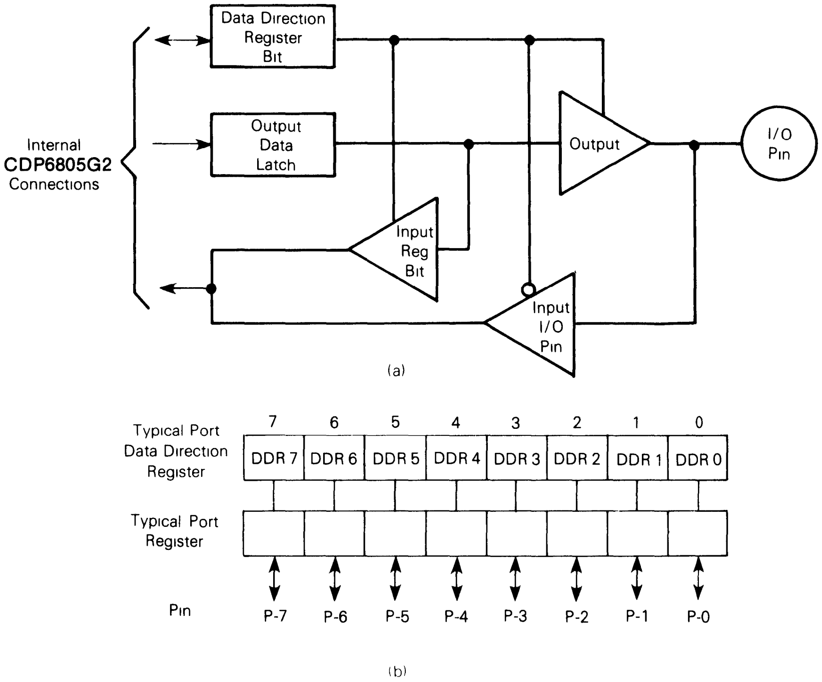


Fig. 9 - Typical port I/O circuitry.

TABLE 2 — I/O PIN FUNCTIONS

$R/\overline{W}$	DDR	I/O Pin Function
0	0	The I/O pin is in input mode Data is written into the output data latch
0	1	Data is written into the output data latch and output to the I/O pin
1	0	The state of the I/O pin is read
1	1	The I/O pin is in an output mode The output data latch is read

CDP6805G2, CDP6805G2C

SELF-CHECK

The CDP6805G2 self-check is performed using the circuit in Figure 10. Self-check is initiated by tying NUM and TIMER pins to a logic 1 then executing a reset. After reset, five subroutines are called that execute the following tests:

I/O – Functionally exercise port A, B, C, D
RAM – Walking bit test
ROM – Exclusive OR with odd 1's parity result
Timer – Functionally exercise timer
Interrupts – Functionally exercise external and timer interrupts

Self-check results are shown in Table 3. The following subroutines are available to user programs and do not require any external hardware

RAM SELF-CHECK SUBROUTINE

Returns with the Z-bit clear if any error is detected; otherwise the Z-bit is set

The RAM test must be called with the stack pointer at $07F When run, the test checks every RAM cell except for $07F and $07E which are assumed to contain the return address.

A and X are modified. All RAM locations except the top 2 are modified. (Enter at location $1F80.)

ROM CHECKSUM SUBROUTINE

Returns with Z-bit cleared if any error was found, otherwise Z = 1. X = 0 on return, and A is zero if the test passed. RAM locations $040-$043 are overwritten. (Enter at location $1F9B.)

TIMER TEST SUBROUTINE

Return with Z-bit cleared if any error was found; otherwise Z = 1.

This routine runs a simple test on the timer In order to work correctly as a user subroutine, the internal clock must be the clocking source and interrupts must be disabled. Also, on exit, the clock will be running and the interrupt mask not set so the caller must protect himself from interrupts if necessary

A and X register contents are lost; this routine counts how many times the clock counts in 128 cycles. The number of counts should be a power of two since the prescaler is a power of two. If not, the timer probably is not counting correctly. The routine also detects if the timer is running at all. (Enter at location $1FB5.)

MEMORY

The CDP6805G2 has a total address space of 8192 bytes of memory and I/O registers. The address space is shown in Figure 11.

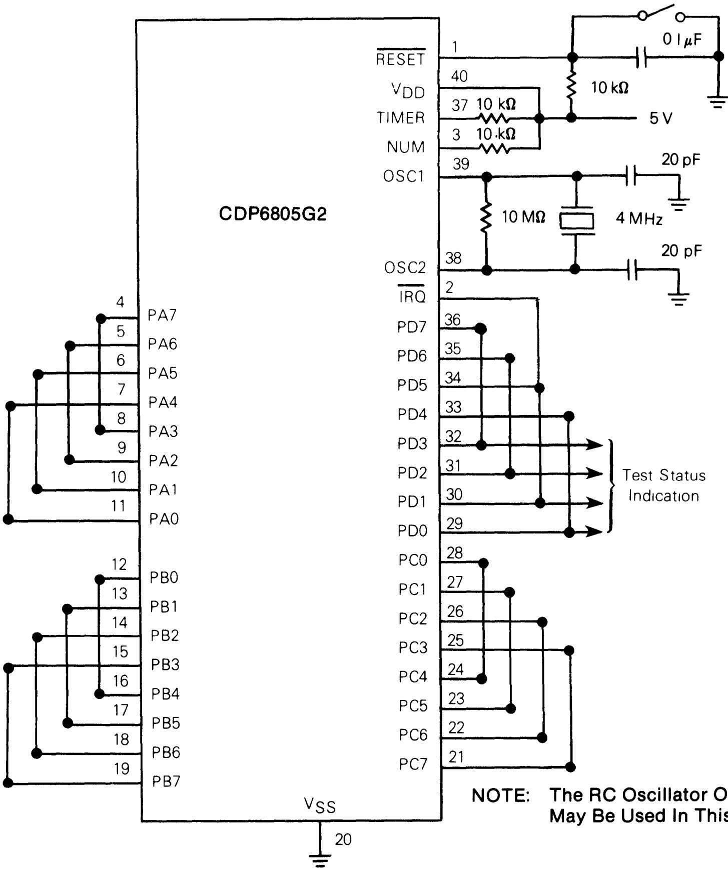
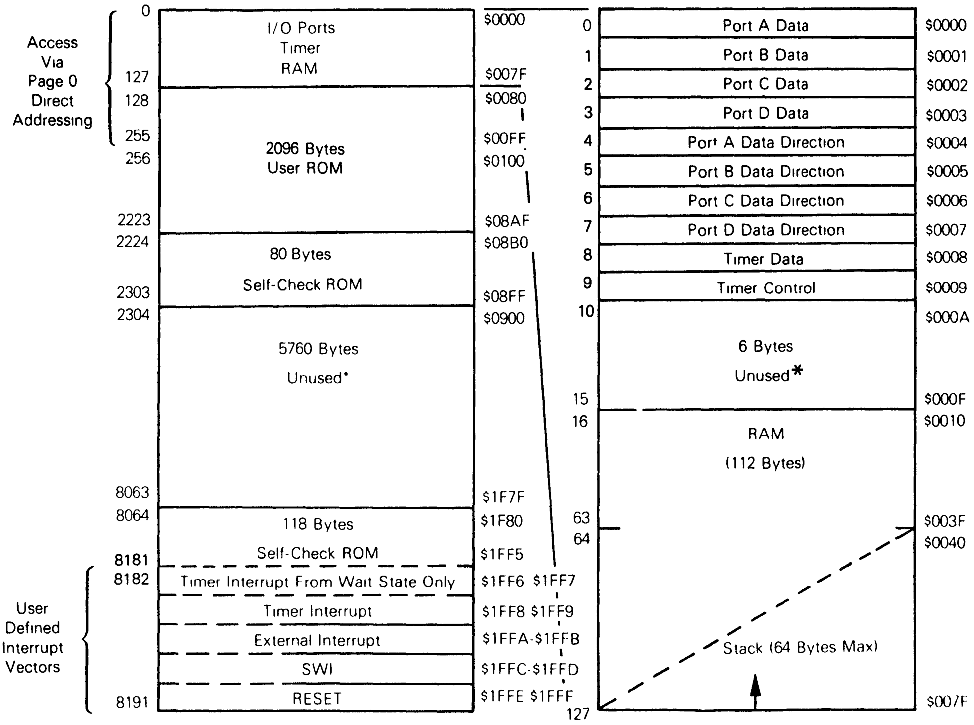


Fig. 10 - Self-check circuit.

TABLE 3 — SELF-CHECK RESULTS

PD3	PD2	PD1	PD0	Remarks
1	0	1	0	Bad I/O
1	0	1	1	Bad Timer
1	1	0	0	Bad RAM
1	1	0	1	Bad ROM
1	1	1	0	Bad Interrupt or Request Flag
All Cycling				Good Part
All Others				Bad Part



*Reads of unused locations undefined

Fig. 11 - Address map.

The first 128 bytes of memory (first half of page zero) is comprised of the I/O port locations, timer locations, and 112 bytes of RAM The next 2096 bytes comprise the user ROM The 10 highest address bytes contain the reset and interrupt vectors

The stack pointer is used to address data stored on the stack Data is stored on the stack during interrupts and subroutine calls At power-up, the stack pointer is set to $007F and it is decremented as data is pushed on the stack When data is removed from the stack, the stack pointer is incremented A maximum of 64 bytes of RAM is available for stack usage Since most programs use only a small part of the allocated stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are usable for program data storage

REGISTERS

The CDP6805G2 contains five registers as shown in the programming model in Figure 12. The interrupt stacking order is shown in Figure 13.

ACCUMULATOR (A)

This accumulator is an 8-bit general purpose register used for arithmetic calculations and data manipulations

INDEX REGISTER (X)

The X register is an 8-bit register which is used during the indexed modes of addressing It provides an 8-bit operand which is used to create an effective address The index register is also used for data manipulations with the read/modify/write type of instructions and as a temporary storage register when not performing addressing operations

PROGRAM COUNTER (PC)

The program counter is a 13-bit register that contains the address of the next instruction to be executed by the processor

STACK POINTER (SP)

The stack pointer is a 13-bit register containing the address of the next free location on the stack When accessing memory, the seven most-significant bits are permanently set to 0000001 These seven bits are appended to the six least-significant register bits to produce an address within the range of $007F to $0040 The stack area of RAM is used to store the return address on subroutine calls and the

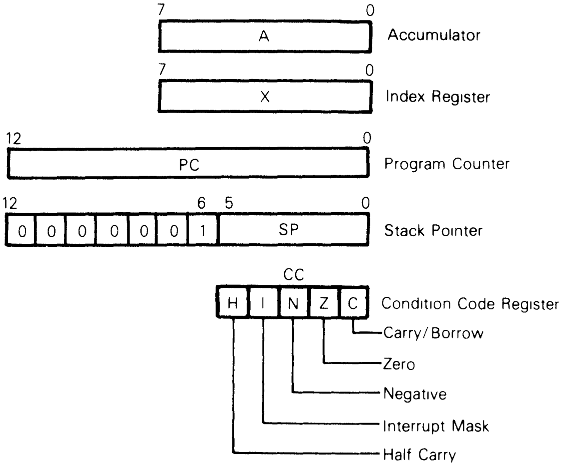
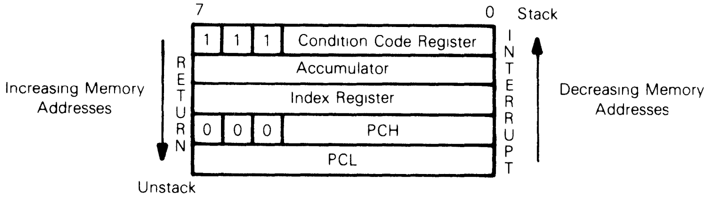


Fig. 12 - Programming Model.



NOTE Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc Pulling from the stack is in the reverse order

Fig. 13 - Stacking order.

machine state during interrupts During external or power-on reset, and during a "reset stack pointer" instruction, the stack pointer is set to its upper limit ($007F) Nested interrupts and/or subroutines may use up to 64 (decimal) locations, beyond which the stack pointer "wraps around" and points to its upper limit thereby losing the previously stored information A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five bytes

CONDITION CODE REGISTER (CC)

The condition code register is a 5-bit register which indicates the results of the instruction just executed These bits can be individually tested by a program and specific action taken as a result of their state Each bit is explained in the following paragraphs

HALF CARRY BITS (H) — The H-bit is set to a one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction The H-bit is useful in binary coded decimal subroutines

INTERRUPT MASK BIT (I) — When the I-bit is set, both the external interrupt and the timer interrupt are disabled Clearing this bit enables the above interrupts If an interrupt occurs while the I-bit is set, the interrupt is latched and is processed when the I-bit is next cleared.

NEGATIVE (N) — Indicates that the result of the last arithmetic, logical, or data manipulation is negative (bit 7 in the result is a logical one)

ZERO (Z) — Indicates that the result of the last arithmetic, logical, or data manipulation is zero.

CARRY/BORROW (C) — Indicates that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation This bit is also affected during bit test and branch instructions, shifts, and rotates

RESETS

The CDP6805G2 has two reset modes: an active low external reset pin ($\overline{\text{RESET}}$) and a power-on reset function; refer to Figure 5.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ input pin is used to reset the MCU to provide an orderly software start-up procedure When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one t_{cyc} The $\overline{\text{RESET}}$ pin is provided with a Schmitt Trigger input to improve its noise immunity

POWER-ON RESET

The power-on reset occurs when a positive transition is detected on V_{DD}. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. There is no provision for a power-down reset The power-on circuitry provides for a 1920 t_{cyc} delay from the time of the first oscillator operation If the external RESET pin is low at the end of the 1920 t_{cyc} time out, the processor remains in the reset condition

Either of the two types of reset conditions causes the following to occur

- Timer control register interrupt request bit TCR7 is cleared to a "0"
- Timer control register interrupt mask bit TCR6 is set to a "1"
- All data direction register bits are cleared to a "0" All ports are defined as inputs
- Stack pointer is set to $007F
- The internal address bus is forced to the reset vector ($1FFE, $1FFF)
- Condition code register interrupt mask bit (I) is set to a "1"
- STOP and WAIT latches are reset
- External interrupt latch is reset

All other functions, such as other registers (including output ports), the timer, etc , are not cleared by the reset conditions

INTERRUPTS

The CDP6805G2 may be interrupted by one of three different methods: either one of two maskable hardware interrupts (external input or timer) or a nonmaskable software interrupt (SWI). Systems often require that normal processing be interrupted so that some external event may be serviced.

Interrupts cause the processor registers to be saved on the stack and the interrupt mask (I bit) set to prevent additional interrupts. The RTI instruction causes the register contents to be recovered from the stack followed by a return to normal processing. The stack order is shown in Figure 13.

Unlike $\overline{\text{RESET}}$, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction execution is complete.

Note

The current instruction is considered to be the one already fetched and being operated on.

When the current instruction is complete, the processor checks all pending hardware interrupts and if unmasked (I bit clear), proceeds with interrupt processing; otherwise, the next instruction is fetched and executed. Note that masked interrupts are latched for later interrupt service.

If both an external interrupt and a timer interrupt are pending at the end of an instruction execution, the external interrupt is serviced first. The SWI is executed the same as any other instruction and as such takes precedence over hardware interrupts only if the I bit is set (hardware interrupts masked). Refer to Figure 14 for the interrupt and instruction processing sequence.

Table 4 shows the execution priority of the $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$ and timer interrupts, and instructions (including the software interrupts, SWI). Two conditions are shown, one with the I bit set and the other with I bit clear; however, in either case $\overline{\text{RESET}}$ has the highest priority of execution. If the I bit is set as per Table 4(a), the second highest priority is assigned to any instruction including SWI. This is illustrated in Figure 14 which shows that the $\overline{\text{IRQ}}$ or Timer interrupts are not executed when the I bit is set. If the I bit is cleared as per Table 4(b), the priorities change in that the next instruction (SWI or other instruction) is not fetched until after the $\overline{\text{IRQ}}$ and Timer interrupts have been recognized (and serviced). Also, when the I bit is clear, if both $\overline{\text{IRQ}}$ and Timer interrupts are pending, the $\overline{\text{IRQ}}$ interrupt is always serviced before the Timer interrupt.

*Any current instruction including SWI

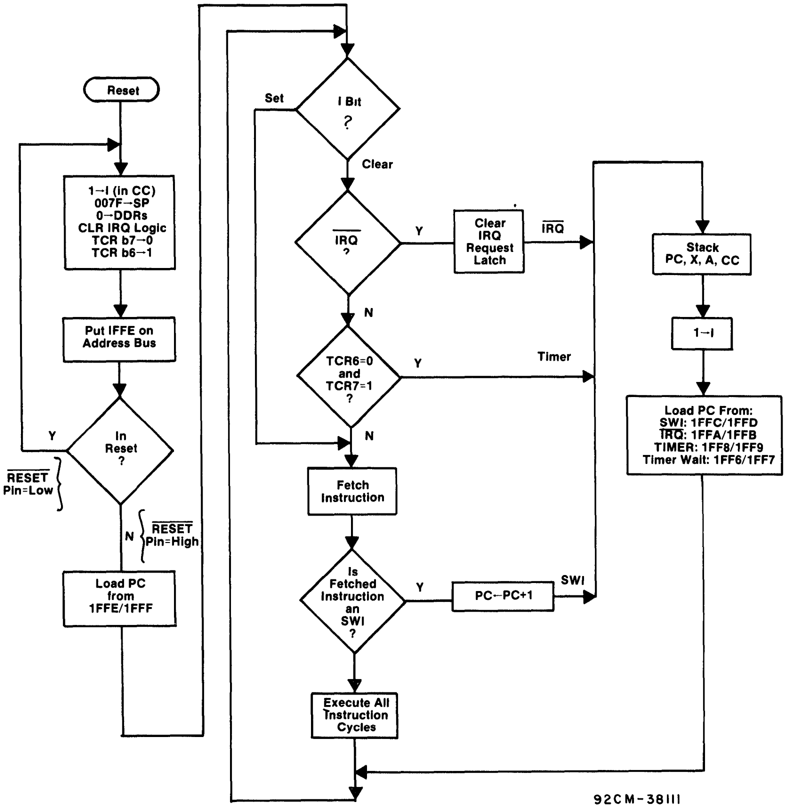


Fig. 14 - $\overline{\text{RESET}}$ and INTERRUPT processing flowchart.

TABLE 4 - INTERRUPT/INSTRUCTION EXECUTION PRIORITY AND VECTOR ADDRESS

(a) I Bit Set

Interrupt/Instruction	Priority	Vector Address
$\overline{\text{RESET}}$	1	$1FFE-$1FFF
SWI (or Other Instruction)	2	$1FFC-$1FFD

NOTE: $\overline{\text{IRQ}}$ and Timer Interrupts are not executed when the I bit is set; therefore, they are not shown.

(b) I Bit Clear

Interrupt/Instruction	Priority	Vector Address
$\overline{\text{RESET}}$	1	$1FFE-$1FFF
$\overline{\text{IRQ}}$	2	$1FFA-$1FFB
Timer	3	$1FF8-$1FF9 $1FF6-$1FF7*
SWI (or other Instruction)	4	$1FFC-$1FFD

* The Timer vector address from the WAIT mode is $1FF6-$1FF7.

Note

Processing is such that at the end of the current instruction execution, the I bit is tested and if set the next instruction (including SWI) is fetched. If the I bit is cleared, the hardware interrupt latches are tested, and if no hardware interrupt is pending, the program falls through and the next instruction is fetched.

TIMER INTERRUPT

If the timer interrupt mask bit (TCR6) is cleared, then each time the timer decrements to zero (transitions from $01 to $00) an interrupt request is generated. The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks further interrupts until the present one is serviced. The processor now vectors to the timer interrupt service routine. The address for this service routine is specified by the contents of $1FF8 and $1FF9 unless the processor is in a WAIT mode in which case the contents of $1FF6 and $1FF7 specify the timer service routine address. Software must be used to clear the timer interrupt request bit (TCR7). At the end of the timer interrupt service routine, the software normally executes an RTI instruction which restores the machine state and starts executing the interrupted program.

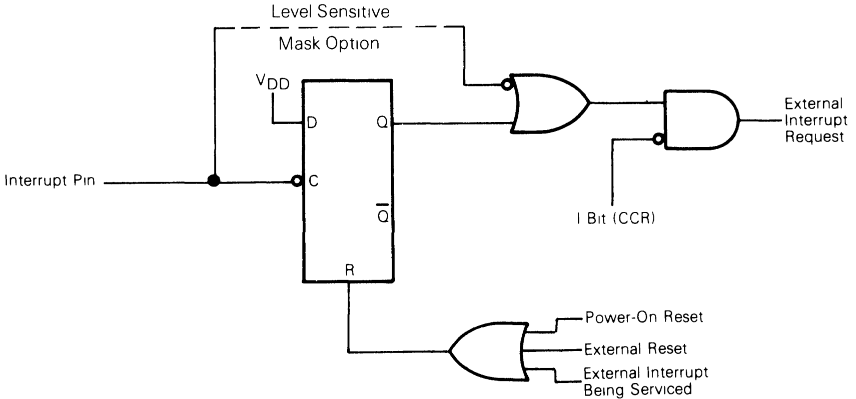
EXTERNAL INTERRUPT

If the interrupt mask bit of the condition code register is cleared and the external interrupt pin ($\overline{\text{IRQ}}$) is low, then the external interrupt occurs. The action of the external interrupt is identical to the timer interrupt with the exception that the service routine address is specified by the contents of $1FFA and $1FFB. Either a level- and edge-sensitive trigger (or edge-sensitive only) are available as mask options. Figure 15 shows both a functional diagram and timing for the interrupt line. The timing diagram shows two different treatments of the interrupt line ($\overline{\text{IRQ}}$) to the processor. The first method is single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the length of the interrupt service routine. Once a pulse occurs, the next pulse should not occur until the MPU software has exited the routine (an RTI occurs). This time (t_{ILIL}) is obtained by adding 20 instruction cycles (t_{cyc}) to the total number of cycles is takes to complete the service routine including the RTI instruction; refer to Figure 15. The second configuration shows many interrupt lines "wire-ORed" to form the interrupts at the processor. Thus, if after servicing an interrupt the $\overline{\text{IRQ}}$ remains low, then the next interrupt is recognized.

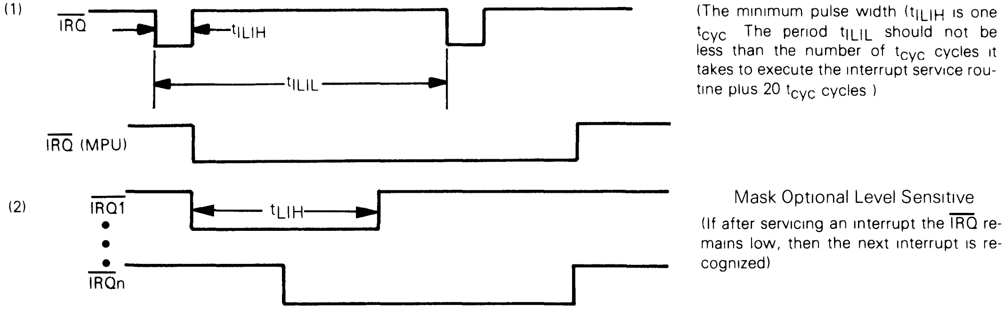
SOFTWARE INTERRUPT (SWI)

The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask in the condition code register. The service routine address is specified by the contents of memory locations $1FFC and $1FFD. See Figure 14 for interrupt and instruction processing flowchart.

(a) Interrupt Functional Diagram



(b) Interrupt Mode Diagram



Edge Condition

(The minimum pulse width (t_{ILIH} is one t_{cyc}. The period t_{ILIL} should not be less than the number of t_{cyc} cycles it takes to execute the interrupt service routine plus 20 t_{cyc} cycles.)

Mask Optional Level Sensitive

(If after servicing an interrupt the $\overline{\text{IRQ}}$ remains low, then the next interrupt is recognized)

Fig. 15 - External interrupt.

STOP

The STOP instruction places the CDP6805G2 in its lowest power consumption mode. In the STOP function the internal oscillator is turned off, causing all internal processing and the timer to be halted; refer to Figure 16.

During the STOP mode, timer control register (TCR) bits 6 and 7 are altered to remove any pending timer interrupt requests and to disable any further timer interrupts The timer prescaler is cleared External interrupts are enabled in the condition code register. All other registers and memory remain unaltered All I/O lines remain unchanged.

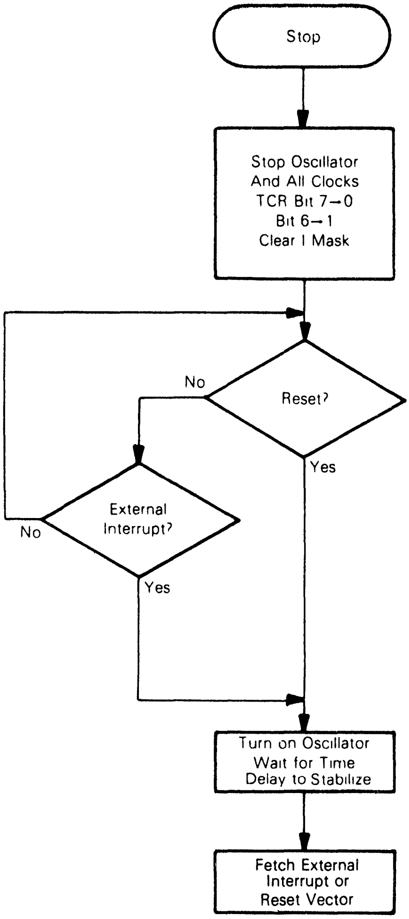


Fig. 16 - Stop function flowchart.

WAIT

The WAIT instruction places the CDP6805G2 in a low power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode. In the WAIT mode, the internal clock is diabled from all internal circuitry except the timer circuit; refer to Figure 17. Thus, all internal processing is halted; however, the timer continues to count normally.

During the Wait mode, the I-bit in the condition code register is cleared to enable interrupts. All other registers, memory, and I/O lines remain in their last state. The timer may be enabled to allow a periodic exit from the Wait mode. If an external and a timer interrupt occur at the same time, the external interrupt is serviced first; then, if the timer interrupt request is not cleared in the external interrupt routine,the normal timer interrupt (not the timer Wait interrupt) is serviced since the MCU is no longer in the WAIT mode.

TIMER

The MCU timer contains a 8-bit software programmable counter with7-bit software selectable prescaler. The counter may be present under program control and decrements towards zero. When the counter decrements to zero, the timer interrupt request bit, i.e., bit 7 of the timer control register (TRC), is set. Then, if the timer interrupt is not masked, i.e., bit 6 of the TCR and the I-bit in the condition code register are both cleared, the processor receives an interrupt. After completion of the current instruction, the processor proceeds to store the appropriate registers on the stack, and then fetches the timer vector address from locations $1FF8 and $1FF9 (or $1FF6 and $1FF7 if in the WAIT mode) in order to beging servicing.

The counter continues to count after it reaches zero, allowing the software to determine the number of internal or external input clocks since the timer interrupt request bit was set. The counter may be read at any time by the processor without disturbing the count. The contents of the counter becomes stable prior to the read portion of a cycle and does not change during the read. The timer interrupt request bit remains set until cleared by the software. If a read occurs before the timer interrupt is serviced, the interrupt is lost. TCR7 may also be used as a scanned status bit in a non-interrupt mode of operation (TCR6=1).

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer. Bit 0, bit 1, and bit 2 of the TCR are programmed to choose the appropriate prescaler output which is used as the counter input. The processor cannot write into or read from the prescaler; however, its contents are clearedto all "0's" by the write operation into TCR when bit 3 of the written data equals 1. This allows for truncation-free counting.

The timer input can be configured for three different operating modes, plus a disable mode depending on the value written to the TCR4, TCR5 control bits. Refer to the Timer Control Register section.

TIMER INPUT MODE 1

If TCR4 and TCR5 are both programmed to a "0," the input to the timer is from an internal clock and the TIMER input pin is disabled. The internal clock mode can be used for periodic interrupt generation, as well as a reference in frequency and event measurement. The internal clock is the instruction cycle clock. During a WAIT instruction, the internal clock to the timer continues to run at its normal rate.

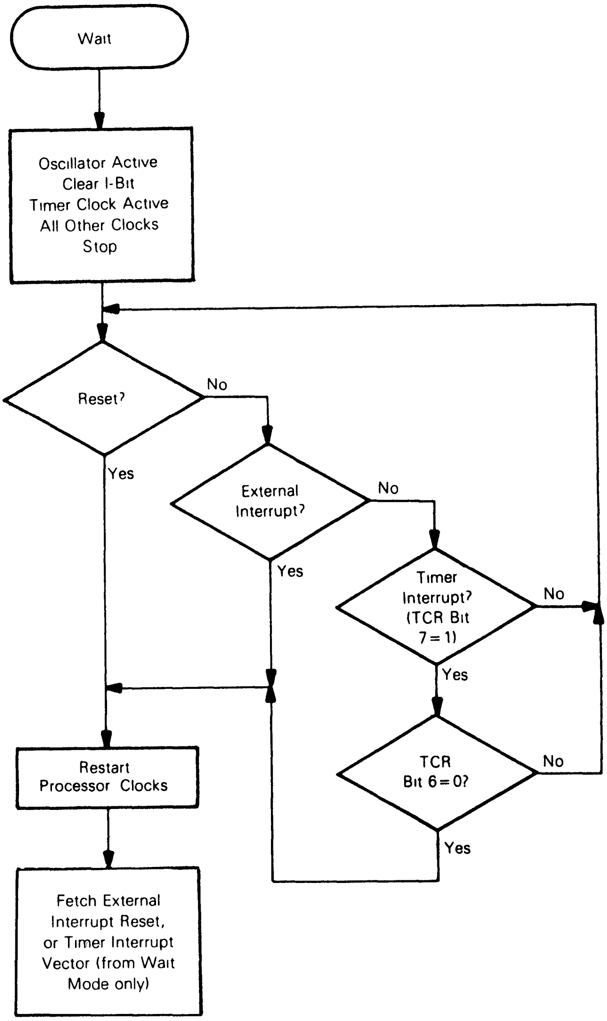


Fig. 17 - Wait function flowchart.

TIMER INPUT MODE 2

With TCR4=1 and TCR5=0, the internal clock and the TIMER input pin are ANDed together to form the timer input signal This mode can be used to measure external pulse widths The external pulse simply turns on the internal clock for the duration of the pulse The resolution of the count in this mode is ±1 clock and, therefore, accuracy improves with longer input pulse widths

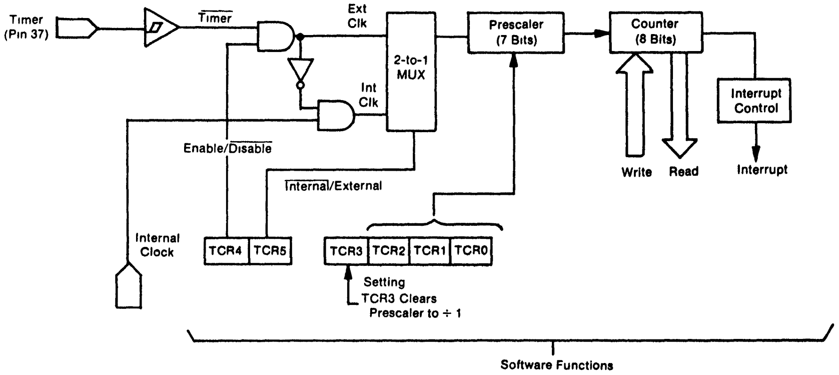
TIMER INPUT MODE 3

If TCR4=0 and TCR5=1, then all inputs to the Timer are disabled

TIMER INPUT MODE 4

If TCR4=1 and TCR5=1, the internal clock input to the Timer is disabled and the TIMER input pin becomes the input to the Timer. The timer can, in this mode, be used to count external events as well as external frequencies for generating periodic interrupts. The counter is clocked on the falling edge of the external signal.

Figure 18 shows a block diagram of the Timer subsystem. Power-on Reset and the STOP instruction cause the counter to be set to $F0.



NOTES
1. Prescaler and 8-bit counter are clocked falling edge of the internal clock (AS) or external input
2. Counter is written to during Data Strobe (DS) and counts down continuously.

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Fig. 18 - Simplified timer control logic block diagram.

Timer Control Register (TCR)

7	6	5	4	3	2	1	0
TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0

All bits in this register except bit 3 are Read/Write bits.

TCR7 – Timer interrupt request bit: bit used to indicate the timer interrupt when it is logic "1".

1 – Set whenever the counter decrements to zero, or under program control.

0 – Cleared on external reset, power-on reset, STOP instruction, or program control.

TCR6 – Timer interrupt mask bit when this bit is a logic "1" it inhibits the timer interrupt to the processor.

1 – Set on external reset, power-on reset, STOP instruction, or program control.

0 – Cleared under program control

TCR5 – External or internal bit selects the input clock source to be either the external timer pin or the internal clock. (Unaffected by $\overline{\text{RESET}}$)

1 – Select external clock source.

0 – Select internal clock source (AS).

TCR4 – External enable bit control bit used to enable the external timer pin. (Unaffected by $\overline{\text{RESET}}$.)

1 – Enable external timer pin.

0 – Disable external timer pin

TCR5	TCR4	
0	0	Internal clock to Timer
0	1	AND of internal clock and TIMER pin to Timer
1	0	Inputs to Timer disabled
1	1	TIMER pin to Timer

Refer to Figure 18 for Logic Representation.

TCR3 – Timer Prescaler Reset bit: writing a "1" to this bit resets the prescaler to zero. A read of this location always indicates a "0". (Unaffected by $\overline{\text{RESET}}$.)

TCR2, TCR1, TCR0 – Prescaler select bits: decoded to select one of eight taps on the prescaler. (Unaffected by $\overline{\text{RESET}}$.)

Prescaler

TCR2	TCR1	TCR0	Result
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	÷128

INSTRUCTION SET

The MCU has a set of 61 basic instructions They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables

REGISTER/MEMORY INSTRUCTIONS

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The operand for the jump unconditional (JMP) and jump to subroutine (JSR) instructions is the program counter. Refer to Table 5.

READ/MODIFY/WRITE INSTRUCTIONS

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register The test for negative or zero (TST) instruction is an exception to the read/modify/write sequence since it does not modify the value Refer to Table 6.

BRANCH INSTRUCTIONS

Most branch instructions test the state of the Condition Code Register and if certain criteria are met, a branch is executed This adds an offset between + 128 and − 127 to the current program counter. Refer to Table 7.

BIT MANIPULATION INSTRUCTIONS

The MPU is capable of setting or clearing any bit which resides in the first 256 bytes of the memory space, where all port registers, port DDR's, timer, timer control, and on-chip RAM reside. An additional feature allows the software to test and branch on the state of any bit within these 256 locations. The bit set, bit clear and bit test and branch functions are all implemented with a single instruction. For the test and branch instructions the value of the bit tested is also placed in the carry bit of the Condition Code Register. Refer to Table 8 for instruction cycle timing.

CONTROL INSTRUCTIONS

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 9 for instruction cycle timing.

ALPHABETICAL LISTING

The complete instruction set is given in alphabetical order in Table 11.

OPCODE MAP

Table 10 is an opcode map for the instructions used on the MCU.

ADDRESSING MODES

The MCU uses ten different addressing modes to give the programmer an opportunity to optimize the code to all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables and scalling tables anywhere in the memory space. Short indexed accesses are single byte instructions, while the longest instructions (three bytes) permit tables throughout memory. Short and long absolute addressing is also included One and two byte direct addressing instructions access all data bytes inmost applications Extended addressing permits jump instructions to reach all memory Tabie 11 shows the addressing modes for each instruction, with the effects each instruction has on the Condition Code Register An opcode map is shown in Table 10.

The term "Effective Address" (EA) is used in describing the various addressing modes, which is defined as the byte address to or from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate "contents of," an arrow indicates "is replaced by" and a colon indicates concatenation of two bytes.

INHERENT

In inherent instructions all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, and no other arguments, are included in this mode.

IMMEDIATE

In immediate addressing, the operand is contained in the byte immediately following the opcode. Immediate addressing is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

$$EA = PC + 1;\ PC \leftarrow PC + 2$$

DIRECT

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two byte instruction. This includes all on-chip RAM and I/O registers and 128 bytes of on-chip ROM. Direct addressing is efficient in both memory and time.

$$EA = (PC + 1);\ PC \leftarrow PC + 2$$

$$\text{Address Bus High} \leftarrow 0;\ \text{Address Bus Low} \leftarrow (PC + 1)$$

EXTENDED

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing modes are capable of referencing arguments anywhere in memory with a single three byte instruction.

$$EA = (PC + 1):(PC + 2);\ PC \leftarrow PC + 3$$

$$\text{Address Bus High} \leftarrow (PC + 1);\ \text{Address Bus Low} \leftarrow (PC + 2)$$

INDEXED, NO-OFFSET

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long and therefore are more efficient. This mode is used to move a pointer through a table or to address a frequency referenced RAM or I/O location.

$$EA = X;\ PC \leftarrow PC + 1$$

$$\text{Address Bus High} \leftarrow 0;\ \text{Address Bus Low} \leftarrow X$$

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INDEXED, 8-BIT OFFSET

Here the EA is obtained by adding the contents of the byte following the opcode to that of the index register. The operand is therefore located anywhere within the lowest 511 memory locations. For example, this mode of addressing is useful for selecting the m-th element in an n element table. All instructions are two bytes. The contents of the index register (X) is not changed. The contents of (PC + 1) is an unsigned 8-bit integer. One byte offset indexing permits look-up tables to be easily accessed in either RAM or ROM.

$$EA = X + (PC + 1);\ PC \leftarrow PC + 2$$

Address Bus High←K, Address Bus Low←X+(PC+1)
Where K=The carry from the addition of X+(PC+1)

INDEXED, 16-BIT OFFSET

In the indexed, 16-bit offset addressing mode the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed 8-bit offset, except that this three byte instruction allows tables to be anywhere in memory (e.g., jump tables in ROM).

$$EA = X + [(PC+1)\ (PC+2)],\ PC \leftarrow PC + 3$$

Address Bus High←(PC+1)+K,
Address Bus Low←X+(PC+2)
Where K=The carry from the addition of X+(PC+2)

RELATIVE

Relative addressing is only used in branch instructions. In relative addressing the contents of the 8-bit signed byte following the opcode (the offset) is added to the PC if and only if the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is limited to the range of -126 to +129 bytes from the branch instruction opcode location.

BIT SET/CLEAR

Direct addressing and bit addressing are combined in instructions which set and clear individual memory and I/O bits In the bit set and clear instructions, the byte is specified as a direct address in the location following the opcode The first 256 addressable locations are thus accessed The bit to be modified within that byte is specified with three bits of the opcode The bit set and clear instructions occupy two bytes, one for the opcode (including the bit number) and the second to address the byte which contains the bit of interest

$$EA = (PC+1),\ PC \leftarrow PC + 2$$

Address Bus High←0, Address Bus Low←(PC+1)

BIT TEST AND BRANCH

Bit test and branch is a combination of direct addressing, bit addressing and relative addressing The bit address and condition (set or clear) to be tested is part of the opcode The address of the byte to be tested is in the single byte immediately following the opcode byte (EA1) The signed relative 8-bit offset is in the third byte (EA2) and is added to the PC if the specified bit is set or clear in the specified memory location This single three byte instruction allows the program to branch based on the condition of any bit in the first 256 locations of memory

$$EA1 = (PC+1)$$

Address Bus High←0, Address Bus Low←(PC+1)

$$EA2 = PC + 3 + (PC+2),\ PC \leftarrow EA2 \text{ if branch taken, otherwise } PC \leftarrow PC + 3$$

TABLE 5 - REGISTER/MEMORY INSTRUCTIONS

		Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from Memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in Memory	STA	–	–	–	B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in Memory	STX	–	–	–	BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add Memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add Memory and Carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract Memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND Memory to A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR Memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump Unconditional	JMP	–	–	–	BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to Subroutine	JSR	–	–	–	BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

TABLE 6 - READ/MODIFY/WRITE INSTRUCTIONS

		Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (2's Complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate Left Thru Carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate Right Thru Carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical Shift Left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical Shift Right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic Shift Right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for Negative or Zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5

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TABLE 7 - BRANCH INSTRUCTIONS

		Relative Addressing Mode		
Function	Mnemonic	Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	3
Branch Never	BRN	21	2	3
Branch IFF Higher	BHI	22	2	3
Branch IFF Lower or Same	BLS	23	2	3
Branch IFF Carry Clear	BCC	24	2	3
(Branch IFF Higher or Same)	(BHS)	24	2	3
Branch IFF Carry Set	BCS	25	2	3
(Branch IFF Lower)	(BLO)	25	2	3
Branch IFF Not Equal	BNE	26	2	3
Branch IFF Equal	BEQ	27	2	3
Branch IFF Half Carry Clear	BHCC	28	2	3
Branch IFF Half Carry Set	BHCS	29	2	3
Branch IFF Plus	BPL	2A	2	3
Branch IFF Minus	BMI	2B	2	3
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	3
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	3
Branch IFF Interrupt Line is Low	BIL	2E	2	3
Branch IFF Interrupt Line is High	BIH	2F	2	3
Branch to Subroutine	BSR	AD	2	6

TABLE 8 - BIT MANIPULATION INSTRUCTIONS

		Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is Set	BRSET n (n=0 7)	–	–	–	2•n	3	5
Branch IFF Bit n is Clear	BRCLR n (n=0 7)	–	–	–	01+2•n	3	5
Set Bit n	BSET n (n=0 7)	10+2•n	2	5	–	–	–
Clear Bit n	BCLR n (n=0 7)	11+2•n	2	5	–	–	–

TABLE 9 - CONTROL INSTRUCTIONS

		Inherent		
Function	Mnemonic	Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	10
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

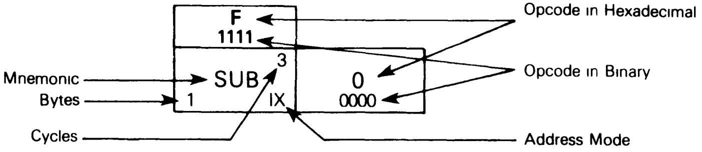
TABLE 10 - INSTRUCTION SET OPCODE MAP

	Bit Manipulation		Branch	Read/Modify/Write					Control		Register/Memory						
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
Hi Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Hi Low
0 0000	5 BRSET0 3 BTB	5 BSET0 2 BSC	3 BRA 2 REL	5 NEG 2 DIR	3 NEG 1 INH	3 NEG 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0 0000
1 0001	5 BRCLR0 3 BTB	5 BCLR0 2 BSC	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1 0001
2 0010	5 BRSET1 3 BTB	5 BSET1 2 BSC	3 BHI 2 REL								2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2 0010
3 0011	5 BRCLR1 3 BTB	5 BCLR1 2 BSC	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3 0011
4 0100	5 BRSET2 3 BTB	5 BSET2 2 BSC	3 BCC 2 REL	5 LSR 2 DTR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4 0100
5 0101	5 BRCLR2 3 BTB	5 BCLR2 2 BSC	3 BCS 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5 0101
6 0110	5 BRSET3 3 BTB	5 BSET3 2 BSC	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6 0110
7 0111	5 BRCLR3 3 BTB	5 BCLR3 2 BSC	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7 0111
8 1000	5 BRSET4 3 BTB	5 BSET4 2 BSC	3 BHCC 2 REL	5 LSL 2 DIR	3 LSLA 1 INH	3 LSLX 1 INH	6 LSL 2 IX1	5 LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8 1000
9 1001	5 BRCLR4 3 BTB	5 BCLR4 2 BSC	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9 1001
A 1010	5 BRSET5 3 BTB	5 BSET5 2 BSC	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A 1010
B 1011	5 BRCLR5 3 BTB	5 BCLR5 2 BSC	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B 1011
C 1100	5 BRSET6 3 BTB	5 BSET6 2 BSC	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C 1100
D 1101	5 BRCLR6 3 BTB	5 BCLR6 2 BSC	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D 1101
E 1110	5 BRSET7 3 BTB	5 BSET7 2 BSC	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E 1110
F 1111	5 BRCLR7 3 BTB	5 BCLR7 2 BSC	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F 1111

Abbreviations for Address Modes

INH	Inherent
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
BTB	Bit Test and Branch
IX	Indexed (No Offset)
IX1	Indexed, 1 Byte (8-Bit) Offset
IX2	Indexed, 2 Byte (16-Bit) Offset

LEGEND



CDP6805G2, CDP6805G2C

TABLE 11 - INSTRUCTION SET

Mnemonic	Addressing Modes										Condition Codes				
	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/ Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
ADD		X	X	X		X	X	X			Λ	●	Λ	Λ	Λ
AND		X	X	X		X	X	X			●	●	Λ	Λ	●
ASL	X		X			X	X				●	●	Λ	Λ	Λ
ASR	X		X			X	X				●	●	Λ	Λ	Λ
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	Λ	Λ	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	Λ
BRSET										X	●	●	●	●	Λ
BSET									X		●	●	●	●	●
BSR					X						●	●	●	●	●
CLC	X										●	●	●	●	0
CLI	X										●	0	●	●	●
CLR	X		X			X	X				●	●	0	1	●
CMP		X	X	X		X	X	X			●	●	Λ	Λ	Λ
COM	X		X			X	X				●	●	Λ	Λ	1
CPX		X	X	X		X	X	X			●	●	Λ	Λ	Λ
DEC	X		X			X	X				●	●	Λ	Λ	●
EOR		X	X	X		X	X	X			●	●	Λ	Λ	●
INC	X		X			X	X				●	●	Λ	Λ	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	Λ	Λ	●
LDX		X	X	X		X	X	X			●	●	Λ	Λ	●
LSL	X		X			X	X				●	●	Λ	Λ	Λ
LSR	X		X			X	X				●	●	0	Λ	Λ
NEG	X		X			X	X				●	●	Λ	Λ	Λ
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	Λ	Λ	●
ROL	X		X			X	X				●	●	Λ	Λ	Λ
ROR	X		X			X	X				●	●	Λ	Λ	Λ
RSP	X										●	●	●	●	●
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	Λ	Λ	●
STOP	X										●	0	●	●	●
STX			X	X		X	X	X			●	●	Λ	Λ	●
SUB		X	X	X		X	X	X			●	●	Λ	Λ	Λ
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	Λ	Λ	●
TXA	X										●	●	●	●	●
WAIT	X										●	0	●	●	●

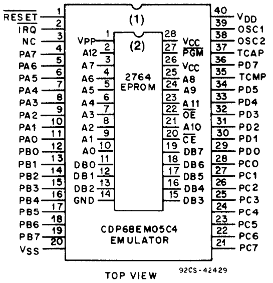
Condition Code Symbols

H	Half Carry (From Bit 3)	Λ	Test and Set if True Cleared Otherwise
I	Interrupt Mask	●	Not Affected
N	Negative (Sign Bit)	?	Load CC Register From Stack
Z	Zero	0	Cleared
C	Carry/Borrow	1	Set

Product Preview

CDP68EM05C4

TERMINAL ASSIGNMENT



40-Lead Piggyback Package

CMOS High-Performance Silicon-Gate 8-Bit Microcomputer Piggyback Emulator

Features:

- *All CDP68HC05C4 hardware and software features*
- *Un-multiplexed external address, data, and READ control lines*
- *Full 8K byte address space available (7984 bytes available externally)*
- *176 bytes of on-chip RAM, no ROM*
- *Direct interface to industry standard EPROMs*
- *40-lead piggyback package (1) with 28 hole socket for 2764 EPROM (2)*
- *Also can be used for CDP68HC05C8 emulation*

The CDP68EM05C4 Emulator device, a functional equivalent to the CDP68HC05C4 microcomputer, is designed to permit prototype development and preproduction of systems for mask-programmed applications. Data and address bus, as well as control signals are externally available.

In addition to this feature, the CDP68EM05C4 Emulator differs from the CDP68HC05C4 in the following ways:

1) Memory locations which are occupied by ROM on the CDP68HC05C4 are accessed as external locations with the CDP68EM05C4 Emulator intended to interface to a programmable ROM.
2) Mask-programmable options (CPU oscillator type and external interrupt sense) are fixed in hardware. Four variations are available with the following suffix for each part: EC, ELC, ER and ELR. The nomenclature is described below:
   a) CPU oscillator = crystal/ceramic resonator-C or resistor-R.
   b) External interrupt request = negative edge and level sensitive-EL, or edge only sensitive-E.

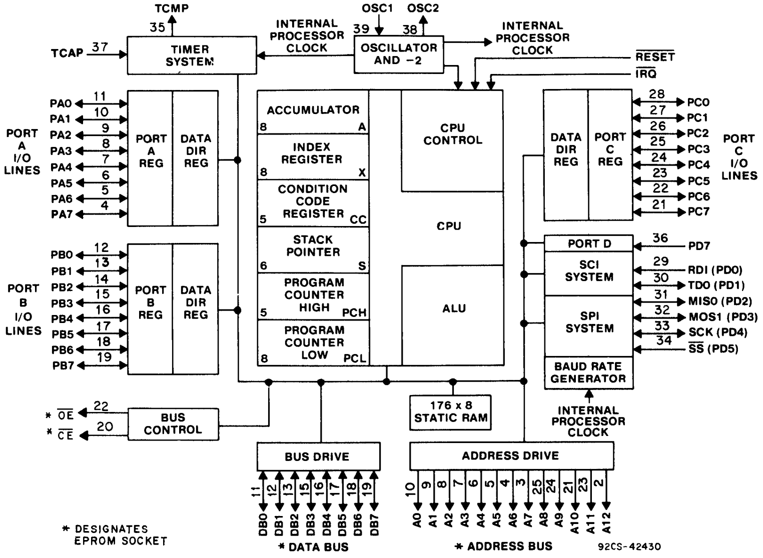


Fig. 1 - CDP68EM05C4 CMOS microcomputer block diagram.

File Number **1961**

CDP68EM05C4

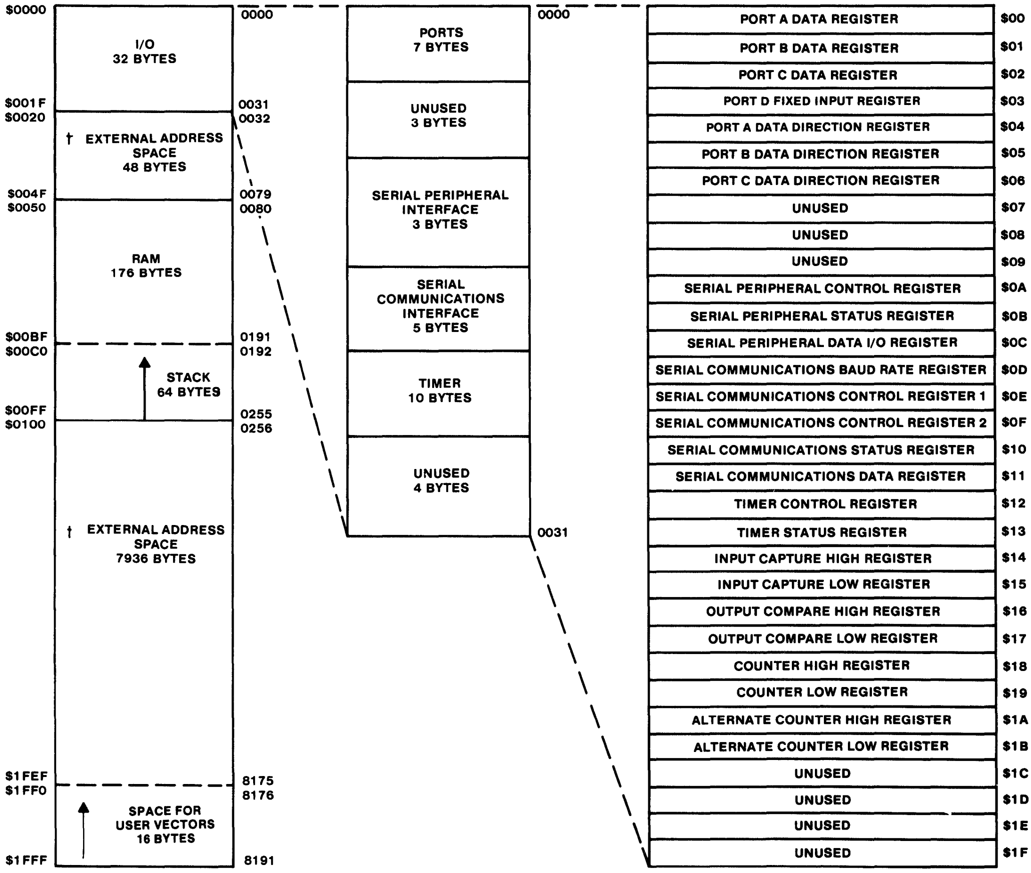
Memory

The CDP68EM05C4 Emulator has a total address space of 8192 bytes. The CDP68EM05C4 Emulator has implemented 208 bytes of the address locations for I/O and internal RAM. The remainder is available for external memory. The first 256 bytes of memory (page zero) is comprised of the I/O port locations, timer locations, 48 bytes of external address space and 176 bytes of RAM. The next 7936 bytes are available to address external memory. The address map is shown in figure 2. The functions of the internally addressable peripherals can be found in the CDP68HC05C4 data sheet, File No. TSM-203.

Functional Pin Description

The following list includes only those additional pins that differ in function from those on the CDP68HC05C4 microcomputer. See the CDP68HC05C4 data sheet, File No. TSM-203, for the remaining pins which are common.

A0-A12	-Address lines 0 through 12.
DB0-BD7	-Bidirectional 8-bit non-multiplexed data bus with TTL inputs.
$\overline{\text{OE}}$	-Output Enable: An output signal used for selecting external memory space. A low level indicates when external ROM is being accessed. The Output Enable signal will not go true, however, when addressing the 7 unused locations in the 32 bytes of the I/O space even though the address lines will be valid.
$\overline{\text{CE}}$	-Chip Enable: A status output which indicates direction of data flow with respect to external or internal memory (a low level indicates a read from memory space). A read of internal memory or I/O will place data on the external data bus. When addressing external memory, this signal in conjunction with $\overline{\text{OE}}$, will enable a READ access from a piggyback EPROM.


$0000
I/O
32 BYTES
$001F
$0020
† EXTERNAL ADDRESS SPACE
48 BYTES
$004F
$0050
RAM
176 BYTES
$00BF
$00C0
STACK
64 BYTES
$00FF
$0100
† EXTERNAL ADDRESS SPACE
7936 BYTES
$1FEF
$1FF0
SPACE FOR USER VECTORS
16 BYTES
$1FFF
0000
0031
0032
0079
0080
0191
0192
0255
0256
8175
8176
8191
PORTS
7 BYTES
UNUSED
3 BYTES
SERIAL PERIPHERAL INTERFACE
3 BYTES
SERIAL COMMUNICATIONS INTERFACE
5 BYTES
TIMER
10 BYTES
UNUSED
4 BYTES
0000
0031
PORT A DATA REGISTER $00
PORT B DATA REGISTER $01
PORT C DATA REGISTER $02
PORT D FIXED INPUT REGISTER $03
PORT A DATA DIRECTION REGISTER $04
PORT B DATA DIRECTION REGISTER $05
PORT C DATA DIRECTION REGISTER $06
UNUSED $07
UNUSED $08
UNUSED $09
SERIAL PERIPHERAL CONTROL REGISTER $0A
SERIAL PERIPHERAL STATUS REGISTER $0B
SERIAL PERIPHERAL DATA I/O REGISTER $0C
SERIAL COMMUNICATIONS BAUD RATE REGISTER $0D
SERIAL COMMUNICATIONS CONTROL REGISTER 1 $0E
SERIAL COMMUNICATIONS CONTROL REGISTER 2 $0F
SERIAL COMMUNICATIONS STATUS REGISTER $10
SERIAL COMMUNICATIONS DATA REGISTER $11
TIMER CONTROL REGISTER $12
TIMER STATUS REGISTER $13
INPUT CAPTURE HIGH REGISTER $14
INPUT CAPTURE LOW REGISTER $15
OUTPUT COMPARE HIGH REGISTER $16
OUTPUT COMPARE LOW REGISTER $17
COUNTER HIGH REGISTER $18
COUNTER LOW REGISTER $19
ALTERNATE COUNTER HIGH REGISTER $1A
ALTERNATE COUNTER LOW REGISTER $1B
UNUSED $1C
UNUSED $1D
UNUSED $1E
UNUSED $1F

† - OE ACTIVE IN THIS SPACE

92CM-39782RI

Fig. 2 - Address map.

$\overline{\text{IRQ}}$ (Maskable Interrupt Request)

Interrupt input which is negative edge and level sensitive. Either type of input to the $\overline{\text{IRQ}}$ pin will produce the interrupt. The MCU completes the current instruction before it responds to the interrupt request. When the $\overline{\text{IRQ}}$ pin goes low for at least one t_{ILIH} as defined in the CDP68HC05C4 data sheet, a logic one is latched internally to signify that an interrupt has been requested. When the MCU completes it's current instruction, the interrupt latch is tested. If the interrupt latch contains a logic one, and the interrupt mask bit (I bit) in the condition code register is clear, the MCU then begins the interrupt sequence. The $\overline{\text{IRQ}}$ input requires an external resistor to V_{DD} for "wire-OR" operation.

OSC1, OSC2

A NAND gate is connected between these two pads (OSC2 = output) for use as a crystal or ceramic resonator oscillator with a STOP clock mode. The internal clocks are derived by a divide-by-2 of the internal oscillator frequency (f_{osc}). Alternatively, an external clock may be used by applying the external clock signal to the OSC1 input with the OSC2 input not connected.

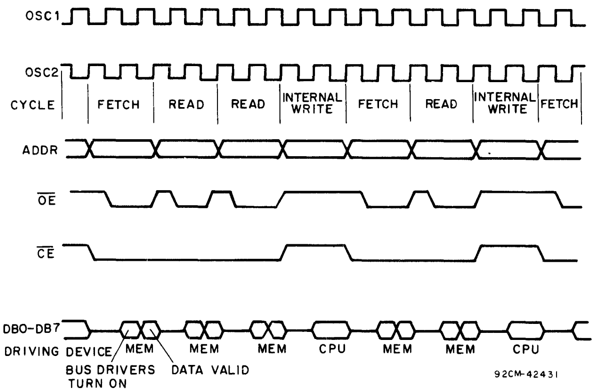


Fig. 3 - Typical cycle timing for the CDP68EM05C4 emulator.

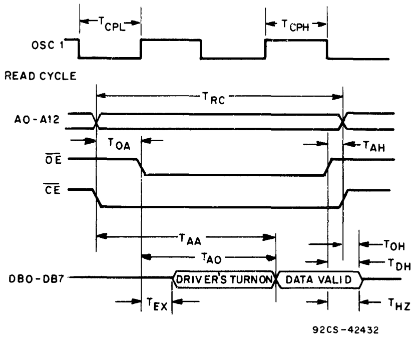


Fig. 4 - Control timing diagram for the CDP68EM05C4 emulator.

CDP68EM05C4

CDP68EM05C4 EMULATION CHIP READ CYCLE TIMING OBJECTIVE SPECIFICATIONS:
V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 25°C

PARAMETER		LIMITS		UNITS
		MIN.	MAX.	
External Input Oscillator Pulse Width, Low or High	T_{CPL}, T_{CPH}	90	—	ns
Read Cycle	TRC(P)	476	—	
Address Before $\overline{\text{OE}}$	TOA(P)	50	—	
Access Time From $\overline{\text{OE}}$	TAO(M)	—	200	
Access Time From Stable Address	TAA(M)	—	350	
Access Time From $\overline{\text{CE}}$	TAA(M)	—	350	
Data Bus Driven From $\overline{\text{OE}}$	TEX(M)	0	—	
Address Hold Time After $\overline{\text{OE}}$	TAH(P)	0	—	
Data Hold Time After Address	TOH(M)	0	—	
Data Hold Time After $\overline{\text{OE}}$	TDH(M)	0	—	
$\overline{\text{OE}}$ High to Data Bus Not Driven	THZ(M)	0	60	

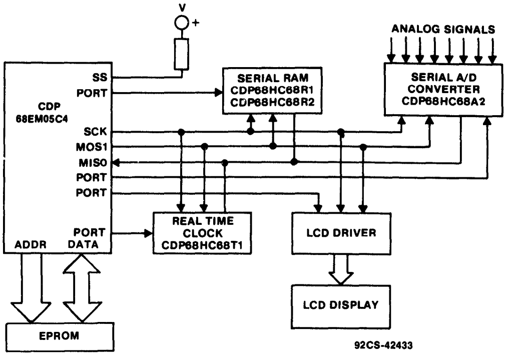


Fig. 5 - Emulation with the serial peripheral interface (SPI) bus system.

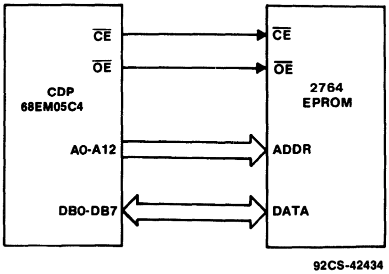
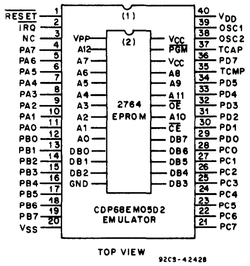


Fig. 6 - CDP68EM05C4 emulator interfaced with 2764 EPROM.

Product Preview

CDP68EM05D2

TERMINAL ASSIGNMENT



40-Lead Piggyback Package

CMOS High-Performance Silicon-Gate 8-Bit Microcomputer Piggyback Emulator

Features:

- *All CDP68HC05D2 hardware and software features*
- *Un-multiplexed external address, data, and READ control lines*
- *Full 8K byte address space available (8064 bytes available externally)*
- *96 bytes of on-chip RAM, no ROM*
- *Direct interface to industry standard EPROMs*
- *40-lead piggyback package (1) with 28-hole socket for 2764 EPROM (2)*

The CDP68EM05D2 Emulator device, a functional equivalent to the CDP68HC05D2 microcomputer, is designed to permit prototype development and preproduction of systems for mask-programmed applications. Data and address bus, as well as control signals are externally available.

In addition to this feature, the CDP68EM05D2 Emulator differs from the CDP68HC05D2 in the following ways:

1) Memory locations which are occupied by ROM on the CDP68HC05D2 are accessed as external locations with the CDP68EM05D2 Emulator intended to interface to a programmable ROM.

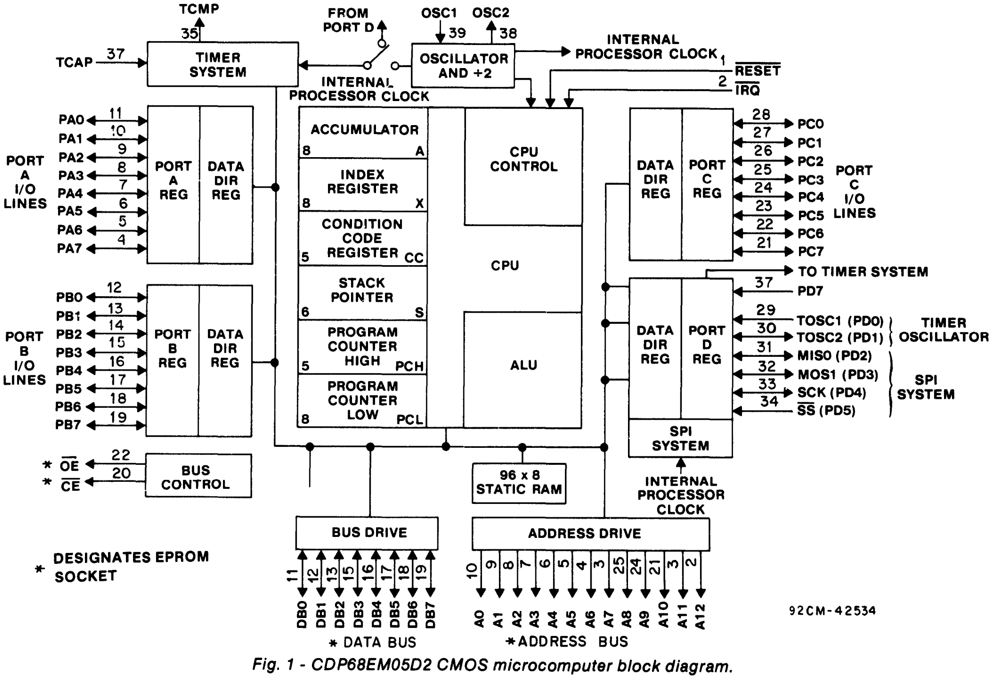


Fig. 1 - CDP68EM05D2 CMOS microcomputer block diagram.

2) Mask-programmable options (CPU oscillator type and external interrupt sense) are fixed in hardware. Only one version of these options is available in the emulator.

   These are:

   a) CPU oscillator = crystal or ceramic resonator.
   b) External interrupt request = negative edge and level sensitive.
   c) Start-up delay for power-on RESET or exit from STOP mode = 4064 cycles.

Memory

The CDP68EM05D2 Emulator has a total address space of 8192 bytes. The CDP68EM05D2 Emulator has implemented 208 bytes of the address locations for I/O and internal RAM. The remainder is available for external memory. The first 256 bytes of memory (page zero) is comprised of the I/O port locations, timer locations, 48 bytes of external address space and 176 bytes of RAM. The next 7936 bytes are available to address external memory. The address map is shown in figure 2. The functions of the internally addressable peripherals can be found in the CDP68HC05D2 data sheet, File No. TSM-204.

Functional Pin Description

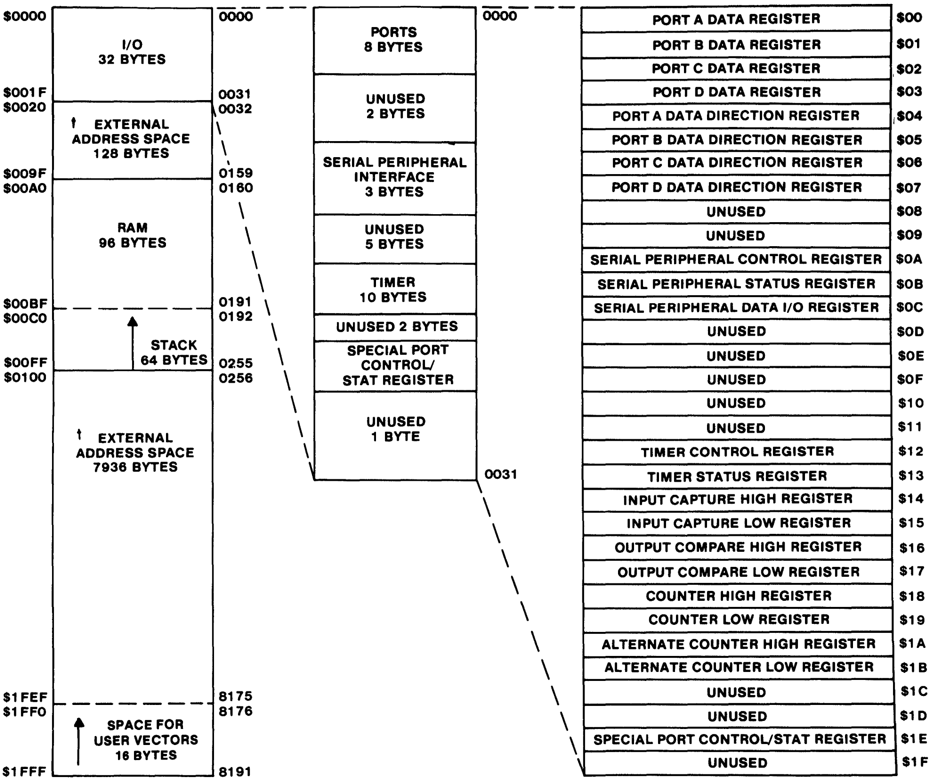
The following list includes only those additional pins that differ in function from those on the CDP68HC05D2 microcomputer. See the CDP68HC05D2 data sheet, File No. TSM-204, for the remaining pins which are common.

A0-A12 -Address lines 0 through 12.

DB0-BD7 -Bidirectional 8-bit non-multiplexed data bus with TTL inputs.

$\overline{OE}$ -Output Enable: An output signal used for selecting external memory space. A low level indicates when external ROM is being accessed. The Output Enable signal will not go true, however, when addressing the 10 unused locations in the 32 bytes of the I/O space even though the address lines will be valid.

$\overline{CE}$ -Chip Enable: A status output which indicates direction of data flow with respect to external or internal memory space). A read of internal memory or I/O will place data on the external data bus. When addressing external memory, this signal in conjunction with $\overline{OE}$, will enable a READ access from a piggyback EPROM.



PORT A DATA REGISTER	$00
PORT B DATA REGISTER	$01
PORT C DATA REGISTER	$02
PORT D DATA REGISTER	$03
PORT A DATA DIRECTION REGISTER	$04
PORT B DATA DIRECTION REGISTER	$05
PORT C DATA DIRECTION REGISTER	$06
PORT D DATA DIRECTION REGISTER	$07
UNUSED	$08
UNUSED	$09
SERIAL PERIPHERAL CONTROL REGISTER	$0A
SERIAL PERIPHERAL STATUS REGISTER	$0B
SERIAL PERIPHERAL DATA I/O REGISTER	$0C
UNUSED	$0D
UNUSED	$0E
UNUSED	$0F
UNUSED	$10
UNUSED	$11
TIMER CONTROL REGISTER	$12
TIMER STATUS REGISTER	$13
INPUT CAPTURE HIGH REGISTER	$14
INPUT CAPTURE LOW REGISTER	$15
OUTPUT COMPARE HIGH REGISTER	$16
OUTPUT COMPARE LOW REGISTER	$17
COUNTER HIGH REGISTER	$18
COUNTER LOW REGISTER	$19
ALTERNATE COUNTER HIGH REGISTER	$1A
ALTERNATE COUNTER LOW REGISTER	$1B
UNUSED	$1C
UNUSED	$1D
SPECIAL PORT CONTROL/STAT REGISTER	$1E
UNUSED	$1F

† - OE ACTIVE IN THIS SPACE

92CM-42535

Fig. 2 - Address map.

$\overline{\text{IRQ}}$ (Maskable Interrupt Request)

Interrupt input which is negative edge and level sensitive. Either type of input to the $\overline{\text{IRQ}}$ pin will produce the interrupt. The MCU completes the current instruction before it responds to the interrupt request. When the $\overline{\text{IRQ}}$ pin goes low for at least one t_{ILIH} as defined in the CDP68HC05D2 data sheet, a logic one is latched internally to signify that an interrupt has been requested. When the MCU completes it's current instruction, the interrupt latch is tested. If the interrupt latch contains a logic one, and the interrupt mask bit (I bit) in the condition code register is clear, the MCU then begins the interrupt sequence. The $\overline{\text{IRQ}}$ input requires an external resistor to V_{DD} for "wire-OR" operation.

OSC1, OSC2

A NAND gate is connected between these two pads (OSC2 = output) for use as a crystal or ceramic resonator oscillator with a STOP clock mode. The internal clocks are derived by a divide-by-2 of the internal oscillator frequency (f_{osc}). Alternatively, an external clock may be used by applying the external clock signal to the OSC1 input with the OSC2 input not connected.

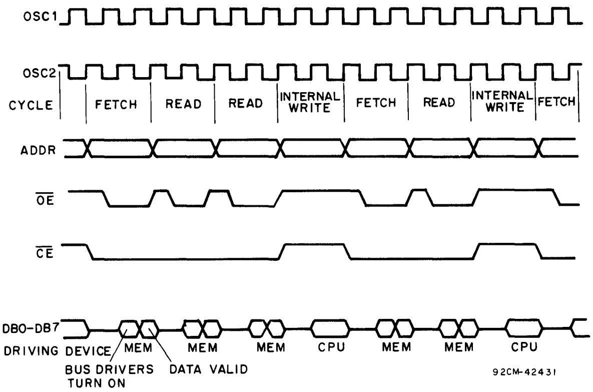


Fig. 3 - Typical cycle timing for the CDP68EM05D2 emulator.

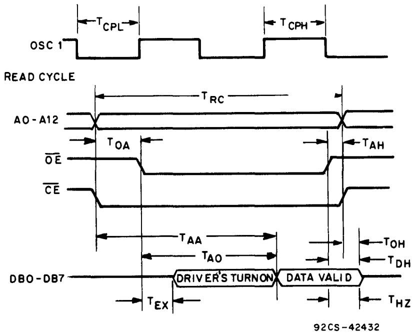


Fig. 4 - Control timing diagram for the CDP68EM05D2 emulator.

CDP68EM05D2

CDP68EM05D2 EMULATION CHIP READ CYCLE TIMING OBJECTIVE SPECIFICATIONS:
V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 25°C

PARAMETER		LIMITS		UNITS
		MIN.	MAX.	
External Input Oscillator Pulse Width, Low or High	T_{CPL}, T_{CPH}	90	—	
Read Cycle	TRC(P)	476	—	
Address Before $\overline{OE}$	TOA(P)	50	—	
Access Time From $\overline{OE}$	TAO(M)	—	200	
Access Time From Stable Address	TAA(M)	—	350	
Access Time From $\overline{CE}$	TAA(M)	—	350	ns
Data Bus Driven From $\overline{OE}$	TEX(M)	0	—	
Address Hold Time After $\overline{OE}$	TAH(P)	0	—	
Data Hold Time After Address	TOH(M)	0	—	
Data Hold Time After $\overline{OE}$	TDH(M)	0	—	
$\overline{OE}$ High to Data Bus Not Driven	THZ(M)	0	60	

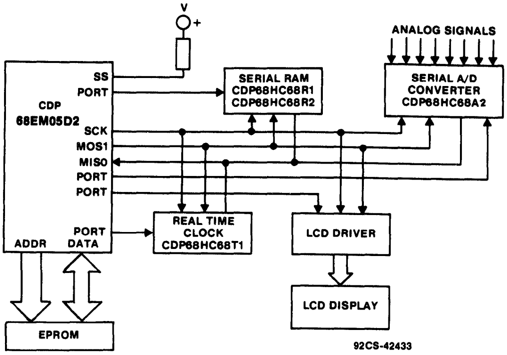


Fig. 5 - Emulation with the serial peripheral interface (SPI) bus system.

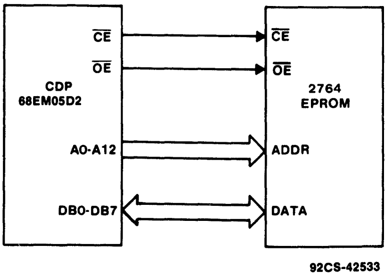


Fig. 6 - CDP68EM05D2 emulator interfaced with 2764 EPROM.

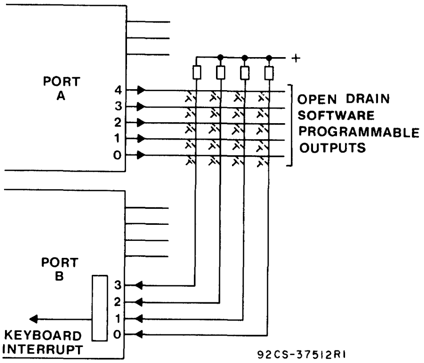


Fig. 7 - Keyboard interface to illustrate use of Open Drain Output Port.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} — V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD}, V_{CC} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

CMOS Peripherals
Technical Data

RCA CMOS peripherals represent the industry's largest number of CMOS peripherals with the broadest range of functions. Most of these devices can interface with 8-bit CMOS or NMOS micros with either multiplexed or non-multiplexed bus structures. There are many that can be interfaced directly without the need for additional "glue parts". The chart on the following page shows a listing of RCA CMOS peripherals and how they can be mixed and matched to bus structures other than the RCA CDP1800- series Micros.

RCA CMOS peripherals provide significant advantages in the requirements for space, weight, power, cost, and cooling when compared to typical NMOS microcomputer systems.

RCA CMOS Peripherals

Can be used with CMOS and NMOS Processors

RCA I/O TYPE	DESCRIPTION AND FUNCTION	MICROPROCESSOR BUS						INPUT LEVELS	FANOUT[2] (TTL LOADS)
			MULTIPLEXED			NON-MULTIPLEXED			
		RCA	RCA/ MOTOROLA	INTEL	INTEL/ NSC	ZILOG	ROCKWELL		
		1800 SERIES	68HC05 6805	8048, 8051 80C48,80C51 8049, 80C49 8088	8085 80C85 NSC800	Z80	6502 65C02		
I/O PORTS									
CDP1851	PROGRAMMABLE I/O PORT	YES	NOTE 1	NOTE 1	NOTE 1	YES	YES	CMOS	1
CDP1852	BYTE-WIDE I/O PORT	YES	YES	YES	YES	YES	YES	CMOS	1
CDP1872	8-BIT INPUT PORT	YES	YES	YES	YES	YES	YES	CMOS	3
CDP1874	8-BIT INPUT PORT	YES	YES	YES	YES	YES	YES	CMOS	3
CDP1875	8-BIT INPUT PORT	YES	YES	YES	YES	YES	YES	CMOS	3
CDP6823	PARALLEL INTERFACE (MOTEL BUS)	NO	YES	YES	YES	NO	NO	CMOS	1
MEMORY I/O DECODERS									
CDP1853	N-BIT 1 OF 8 DECODER	YES	YES	YES	YES	YES	YES	CMOS	1
CDP1881	6-BIT LATCH/DECODER	YES	YES	YES	YES	YES	YES	CMOS	1
CDP1882	6-BIT LATCH/DECODER	YES	YES	YES	YES	YES	YES	CMOS	1
CDP1883	7-BIT LATCH/DECODER	YES	YES	YES	YES	YES	YES	CMOS	1
SERIAL I/O									
CDP1854A*	UART	YES	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	CMOS	1
CDP6402	UART	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	CMOS	1
CDP65C51	UART (WITH BAUD RATE GEN.)	NOTE 1	USE 6853	USE 6853	USE 6853	NOTE 1	YES	TTL	1
CDP6853	UART (MOTEL BUS, WITH BAUD RATE GEN.)	USE 65C51	YES	YES	YES	USE 65C51	USE 65C51	TTL	1
SPI I/O									
CDP68HC68A2	SPI A/D CONVERTER	NOTE 1	YES	YES	NOTE 1	NOTE 1	NOTE 1	CMOS	1
CDP68HC68P1	SPI SINGLE PORT I/O	NOTE 1	YES	YES	NOTE 1	NOTE 1	NOTE 1	CMOS	1
CDP68HC68R1	SPI RAM 128 x 8-BIT	NOTE 1	YES	YES	NOTE 1	NOTE 1	NOTE 1	CMOS	1
CDP68HC68R2	SPI RAM 256 x 8-BIT	NOTE 1	YES	YES	NOTE 1	NOTE 1	NOTE 1	CMOS	1
CDP68HC68T1	SPI REAL-TIME CLOCK	NOTE 1	YES	YES	NOTE 1	NOTE 1	NOTE 1	CMOS	1
MULTIPLY/ DIVIDE									
CDP1855	8-BIT PROGRAMMABLE MDU	YES	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	CMOS	1
KEYBOARD INTERFACE									
CDP1871A	KEYBOARD ENCODER	YES	NOTE 1	NOTE 1	NOTE 1	NOTE 1	NOTE 1	CMOS	
TIMER FUNCTIONS									
CDP1878	DUAL COUNTER-TIMER	YES	NOTE 1	NOTE 1	NOTE 1	YES	YES	CMOS	1
CDP1879	REAL-TIME CLOCK	YES	USE 6818	USE 6818	USE 6818	YES	YES	CMOS	1
CDP6818	REAL-TIME CLOCK/RAM (MOTEL BUS)	NOTE 1	YES	YES	YES	NOTE 1	NOTE 1	CMOS	1
INTERRUPT CONTROL									
CDP1877	PROGRAMMABLE INTERRUPT CONTROLLER (PIC)	YES	NO	NO	NO	NO	NO	CMOS	1

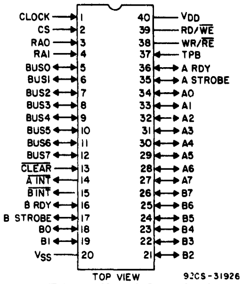
*Operating in 1800 compatible mode (mode 1). Otherwise see CDP6402 for mode 0 information.

NOTES:
1. Yes but requires additional "glue parts"
2. 1 TTL load, i.e., ≤ 0.4 V at 1.6 mA.

CDP1851, CDP1851C

CMOS Programmable I/O Interface

TERMINAL ASSIGNMENT



40-LEAD DIL PACKAGES

Features:

- *20 Programmable I/O Lines*
- *Programmable for Operation in Four Modes:*
  - *Input*
  - *Output*
  - *Bidirectional*
  - *Bit-programmable*
- *Operates in Either I/O or Memory Space*

The RCA CDP1851 and CDP1851C are CMOS programmable two-port I/Os designed for use as general-purpose I/O devices. They are directly compatible with CDP1800 series microprocessors functioning at maximum clock frequency. Each port can be programmed in either byte-I/O or bit-programmable modes for interfacing with peripheral devices such as printers and keyboards.

Both ports A and B can be separately programmed to be 8 bit input or output ports with handshaking control lines, RDY and STROBE. Only port A can be programmed to be a bidirectional port. This configuration provides a means for communicating with a peripheral device or microprocessor system on a single 8 bit bus for both transmitting and receiving data. Handshaking signals are provided to maintain proper bus access control. Port A handshaking lines are used for input control and port B handshaking lines are used for output; therefore port B must be in the bit-programmable mode where handshaking is not used.

Ports A and B can be separately bit programmed so that each individual line can be designated as an input or output line. The handshaking lines may also be individually programmed as input or output when port A is not in bidirectional mode.

The CDP1851 has a supply-voltage range of 4 to 10.5 V, and the CDP1851C has a range of 4 to 6.5 V Both types are supplied in 40-lead dual-in-line plastic (E suffix) or hermetic ceramic (D suffix) packages. The CDP1851C is also available in chip form (H suffix).

CDP1851 Programming Modes

Mode	(8) Port A Data Pins	(2) Port A Handshaking Pins	(8) Port B Data Pins	(2) Port B Handshaking Pins
Input	Accept input data	READY, STROBE	Accept input data	READY, STROBE
Output	Output data	READY, STROBE	Output data	READY, STROBE
Bidirectional (Port A only)	Transfer input/ output data	Input handshaking for Port A	Must be previously set to bit-programmable mode	Output handshaking for Port A
Bit-Programmable	Programmed individually as inputs or outputs	Programmed individually as inputs or outputs	Programmed individually as inputs or outputs	Programmed individually as inputs or outputs

File Number **1056**

CDP1851, CDP1851C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltage referenced to V_{SS} Terminal)	
CDP1851	-0.5 to +11 V
CDP1851C	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Lineary at 12 mW/°C to 200 mW
For T_A = -55 to 100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D)	Derate Lineary at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Type)	40 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1851		CDP1851C		
	MIN.	MAX.	MIN.	MAX.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

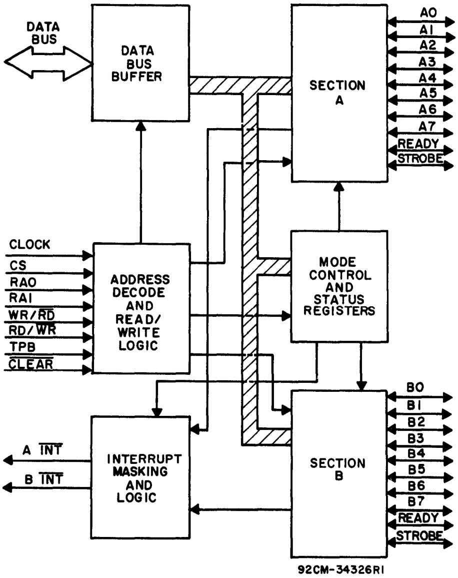


Fig. 1 - Functional diagram for CDP1851 and CDP1851C.

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1851			CDP1851C			
				Min.	Typ.•	Max.	Min.	Typ.•	Max.	
Quiescent Device Current I_{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	μA
	—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current I_{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source) Current I_{OH}	4.6	0, 5	5	-1.15	-2.3	—	-1.15	-2.3	—	
	9.5	0, 10	10	-2.6	-5.2	—	—	—	—	
Output Voltage Low-Level V_{OL}‡	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level V_{OH}‡	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	
	0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	
	0.5, 9.5	—	10	7	—	—	—	—	—	
Input Leakage Current I_{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	μA
		0, 10	10	—	—	±2	—	—	—	
3-State Output Leakage Current I_{OUT}	0, 5	0, 5	5	—	—	±1	—	—	±1	
	0, 10	0, 10	10	—	—	±1	—	—	—	
Operating Current I_{DD1}Δ	—	0, 5	5	—	1.5	3	—	1.5	3	mA
	—	0, 10	10	—	6	12	—	—	—	
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	

•Typical values are for T_A = 25°C and nominal V_{DD}.

‡I_{OL} = I_{OH} = 1 μA.

ΔOperating current is measured at 200 kHz for V_{DD} = 5 V and 400 kHz for V_{DD} = 10 V, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2 MHz).

FUNCTIONAL DESCRIPTION

The CDP1851 has four modes of operation: input, output, bidirectional, and bit-programmable. Port A is programmable in all modes; port B is programmable in all but the bidirectional mode. A control byte must be loaded into the control register to program the ports. In the input and output modes, each port has two handshaking signals, STROBE and RDY. In the bidirectional mode, port A has four handshaking signals: A RDY and A STROBE for input, B RDY and B STROBE for output. If port A is programmed in the bidirectional mode, port B must be programmed in the bit-programmable mode. Each terminal of port A or B may be individually programmed for input or output in the bit-programmable mode. Since handshaking is not used in this mode, the RDY and STROBE lines may also be used for bit-programming if port A is not in the bidirectional mode.

Input Mode

When a peripheral device has data to input, it sends a STROBE pulse to the PIO. The leading edge of this pulse clears the RDY line, inhibiting further transmission from the peripheral. The trailing edge of the STROBE pulse latches the data into the PIO buffer register and also activates the $\overline{\text{INT}}$ line to signal the CPU to read this data. The $\overline{\text{INT}}$ pin can be wired to the $\overline{\text{INT}}$ pin of the CPU or the $\overline{\text{EF}}$ lines for polling. The CPU then executes an input or a load instruction, depending on the mapping technique used. In either case the proper code must be asserted on the RA0, RA1, and CS lines to read the buffer register (see Table VI).

The $\overline{\text{INT}}$ line is deactivated on the leading edge of TPB. The trailing edge of TPB sets the RDY line to signal the peripheral that the port is ready to be loaded with new data. If RDY is low when the input mode is entered (i.e. after a reset), a "dummy" read must be done to set RDY high and signal the peripheral device that the port is ready to be loaded.

CDP1851, CDP1851C

FUNCTIONAL DESCRIPTION (Cont'd)

Output Mode

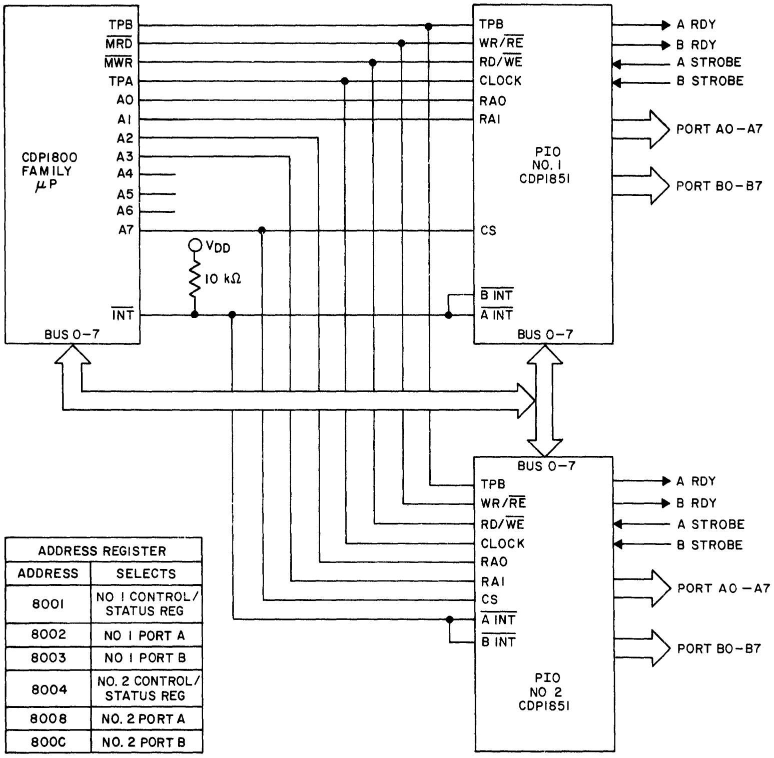
A peripheral STROBE pulse sent to the PIO generates an interrupt to signal the CPU that the peripheral device is ready for data. The CPU executes the proper output or store instruction. Data are than read from memory and placed on the bus. The data are latched into the port buffer at the end of the window when RE/$\overline{\text{WE}}$ = 0 and WR/$\overline{\text{RE}}$ = 1. The RDY line is also set at this time, indicating to the peripheral that there is data in the port buffer. The $\overline{\text{INT}}$ line is deactivated at the beginning of the window. After the peripheral reads valid port data, it can send another STROBE pulse, clearing the RDY line and activating the $\overline{\text{INT}}$ line as in the input mode.

Bidirectional Mode

This mode programs port A to function as both an input and output port. The bidirectional feature allows the peripheral to control port direction by using both sets of handshake signals. The port A handshaking pins are used to control input data from peripheral to PIO, while the port B handshaking pins are used to control output data from PIO to peripheral. Data are transferred in the same manner as the input and output modes. Since $\overline{\text{A INT}}$ is used for both input and output, the status register must be read to determine what condition caused $\overline{\text{A INT}}$ to be activated (see Table V).

Bit—Programmable Mode

This mode allows individual bits of port A or port B to be programmed as inputs or outputs. To output data to bits programmed as outputs, the CPU loads a data byte into the 8 bit port as in the output mode (no handshaking). Only bits programmed for outputs latch this data. Data must be stable when reading from bits programmed as inputs, since the input bits do not latch. When the CDP1851 inputs data to the CPU the CPU also reads the output bits latched during the last output cycle. The RDY and STROBE lines may be used for I/O by using the STROBE/RDY I/O control byte in table II. An additional feature available in the bit-programmable mode is the ability to generate interrupts based on input/output byte combinations. These interrupts can be programmed to occur on logic conditions (AND, OR, NAND, and NOR) generated by the eight I/O lines of each port (The STROBE and RDY lines cannot generate interrupts).



ADDRESS REGISTER	
ADDRESS	SELECTS
8001	NO 1 CONTROL/ STATUS REG
8002	NO 1 PORT A
8003	NO 1 PORT B
8004	NO. 2 CONTROL/ STATUS REG
8008	NO. 2 PORT A
800C	NO. 2 PORT B

92CM-31924

Fig. 2 - Memory space I/O. This configuration allows up to four CDP1851s to occupy memory space 8XXX with no additional hardware (A4 - A5 and A6 - A7 are used as RA0 and RA1 on the third and fourth PIO's).

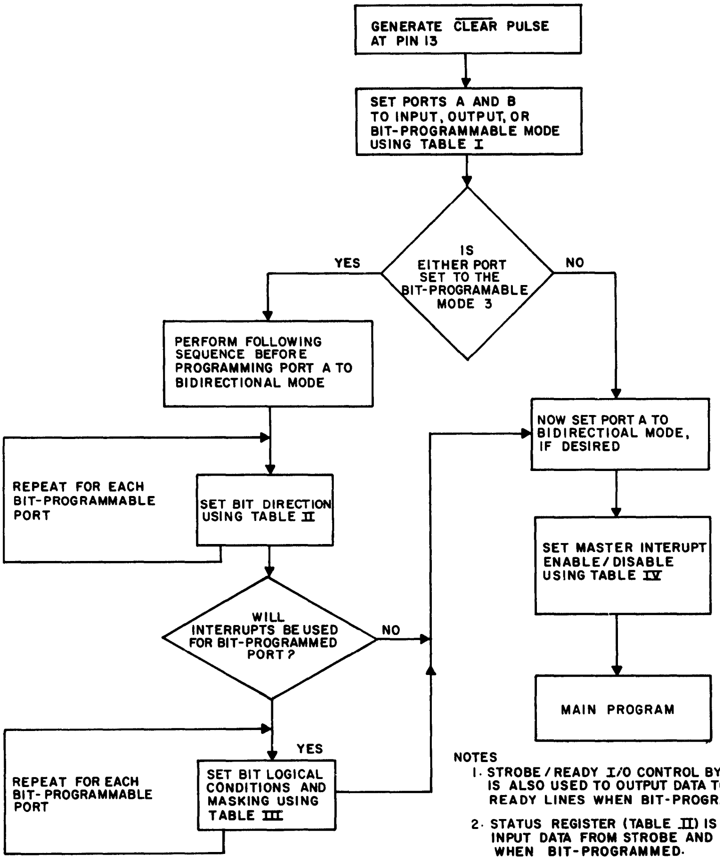
PROGRAMMING

1. **Initialization and Controls**
   The CDP1851 PIO must be cleared by a low on the $\overline{\text{CLEAR}}$ input during power-on to set it for programming. Once programmed, modes can be changed without clearing except when exiting the bit-programmable mode. A low on the $\overline{\text{CLEAR}}$ input sets both ports to the input modes, disables interrupts, unmasks all bit-programmed interrupt bits, and resets the status register, A RDY, and B RDY.

2. **Mode Setting**
   The control register must be sequentially loaded with the appropriate mode set control bytes in order as shown in table I (i.e. input mode then output mode, etc.). Port A is set with the SET A bit = 1 and port B is set with the SET B bit = 1. If a port is set to the bit-programmable mode, the bit-programming control byte from table II must be loaded. A bit is programmed for output with the I/O bit = 1 and for input with the I/O bit = 0. The STROBE and RDY lines may be programmed for input or output with the STROBE/RDY control byte of table II. Input data on the STROBE and RDY lines is detected by reading the status register. When using the STROBE or RDY lines for output, the control byte must be loaded every time output data is to be changed. To program logical conditions that will generate an interrupt, the interrupt control byte of table III must be loaded. An interrupt mask of the eight I/O lines may be loaded next, if bit D4 (mask follows) of the interrupt control byte = 1. The I/O lines are masked if the corresponding bit of the interrupt mask register is 1, otherwise it is monitored. Any combination of masked bits are permissable, except all bits masked (mask = FF).

3. **$\overline{\text{INT}}$ Enable/Disable**
   To enable or disable the $\overline{\text{INT}}$ line in all modes, the interrupt ENABLE/DISABLE byte must be loaded (see Table IV). Interrupts can also be detected by reading the status register see table V. All interrupts should be disabled when programming or false interrupts may occur. The $\overline{\text{INT}}$ outputs are open drain NMOS devices that allow wired ORing (use 10K pull-up registers).

A FLOW CHART GUIDE TO CDP1851 MODE PROGRAMMING


GENERATE CLEAR PULSE AT PIN 13
SET PORTS A AND B TO INPUT, OUTPUT, OR BIT-PROGRAMMABLE MODE USING TABLE I
IS EITHER PORT SET TO THE BIT-PROGRAMABLE MODE 3
YES
NO
PERFORM FOLLOWING SEQUENCE BEFORE PROGRAMMING PORT A TO BIDIRECTIONAL MODE
REPEAT FOR EACH BIT-PROGRAMMABLE PORT
SET BIT DIRECTION USING TABLE II
WILL INTERRUPTS BE USED FOR BIT-PROGRAMMED PORT?
NO
YES
REPEAT FOR EACH BIT-PROGRAMMABLE PORT
SET BIT LOGICAL CONDITIONS AND MASKING USING TABLE III
NOW SET PORT A TO BIDIRECTIOAL MODE, IF DESIRED
SET MASTER INTERUPT ENABLE/DISABLE USING TABLE IV
MAIN PROGRAM

NOTES
1. STROBE/READY I/O CONTROL BYTE (TABLE II) IS ALSO USED TO OUTPUT DATA TO STROBE AND READY LINES WHEN BIT-PROGRAMMED.
2. STATUS REGISTER (TABLE II) IS USED TO INPUT DATA FROM STROBE AND READY LINES WHEN BIT-PROGRAMMED.
3. INTERRUPT STATUS IS ALSO READ FROM STATUS REGISTER.

92CM-34508

TABLE I [RA1=0, RA0=1]

MODE SET *	7	6	5	4	3	2	1	0
Input	0	0	X	Set B	Set A	X	1	1
Output	0	1	X	Set B	Set A	X	1	1
Bit-Programmable	1	1	X	Set B	Set A	X	1	1
Bidirectional	1	0	X	X	Set A	X	1	1

* Modes should be set in order as shown in Table I

If either port is set for bit-programmable mode, the two following control bytes should immediately follow:

TABLE II [RA1=0, RA0=1]

Bit-Programming	7	6	5	4	3	2	1	0
	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
STROBE/RDY I/O ControlΔ	D7	D6	D5	D4	D3	D2	D1	D0

ΔOutput = 1
ΔInput = 0

(D1) 0 = Port A, 1 = Port B
(D2) 0 = No change to RDY line function, 1 = Change per bit (D6)
(D3) 0 = No change to STROBE line function, 1 = Change per bit (D7)
(D4) RDY line output data
(D5) STROBE line output data
(D6) RDY line used as:
Output = 1
Input = 0
(D7) STROBE line used as:
Output = 1
Input = 0

If interrupts will be used for either bit-programmed port, the following control bytes should be loaded:

TABLE III [RA1=0, RA0=1]

INTERRUPT CONTROL	7	6	5	4	3	2	1	0
Logical Conditions and Mask	0	D6	D5	D4	D3	1	0	1

(D3) 0 = Port A, 1 = Port B
(D4) 0 = No change in mask, 1 = Mask follows (See TABLE IIIa)
(D5) (D6) 0, 0 = NAND; 1, 0 = OR; 0, 1 = NOR; 1, 1 = AND

TABLE IIIa [RA1=0, RA0=1]

INTERRUPT CONTROL	7	6	5	4	3	2	1	0
Mask Register (If D4 = 1)	B7 Mask	B6 Mask	B5 Mask	B4 Mask	B3 Mask	B2 Mask	B1 Mask	B0 Mask

If Bn Mask = 1 then mask Bit (for n = 0 to 7)

TABLE IV **[RA1=0, RA0=1]**

	7	6	5	4	3	2	1	0
Interrupt Enable/Disable	$\overline{\text{INT}}$ Enable	X	X	X	A/B	0	0	1

$\overline{\text{INT}}$ Enable = 1, $\overline{\text{INT}}$ Enabled
= 0, $\overline{\text{INT}}$ Disabled

A/B = 0, Port A
= 1, Port B

TABLE V **[RA1=0, RA0=1]**

	7	6	5	4	3	2	1	0
Status Register	D7	D6	D5	D4	D3	D2	D1	D0

(D0) $\overline{\text{B INT}}$ status (1 means set) } All Modes
(D1) $\overline{\text{A INT}}$ status (1 means set) }
(D2) 1 = $\overline{\text{A INT}}$ was caused by A STROBE } Bidirectional Mode Only
(D3) 1 = $\overline{\text{A INT}}$ was caused by B STROBE }

(D4) A RDY input data } Bit-Programmable Mode
(D5) A STROBE input data }
(D6) B RDY input data }
(D7) B STROBE input data }

TABLE VI — CPU CONTROLS

CS *	RA1	RA0	RD/$\overline{\text{WE}}$	WR/$\overline{\text{RE}}$	Action
0	X	X	X	X	No-op bus 3-stated
X	0	0	X	X	No-op bus 3-stated
X	X	X	0	0	No-op bus 3-stated
X	X	X	1	1	No-op bus 3-stated
X	X	X	1	1	No-op bus 3-stated
1	0	1	1	0	Read * status register
1	0	1	0	1	Load control register
1	1	0	1	0	Read * port A
1	1	0	0	1	Load port A
1	1	1	1	0	Read * port B
1	1	1	0	1	Load port B

* Read = RD/$\overline{\text{WE}}$ = 1 and WR/$\overline{\text{RE}}$ = 0 is latched on trailing edge of CLOCK.

TABLE VII — MEMORY I/O USE

	RD/$\overline{\text{WE}}$ Input	WR/$\overline{\text{RE}}$ Input	TPB Input	} PIO Terminals
I/O Space	$\overline{\text{MRD}}$	TPB	TPB	} CPU Terminals
Memory Space	$\overline{\text{MWR}}$	$\overline{\text{MRD}}$	TPB	

FUNCTION PIN DEFINITION

CLOCK (Input):

Positive input pulse that latches READ and CS on its trailing edge.

CS — CHIP SELECT (Input)

A high-level voltage at this input selects the CDP1851 PIO.

RA0 — REGISTER ADDRESS 0 (Input):

This input and RA1 are used to select either the ports or the control/status registers.

RA1 — REGISTER ADDRESS 1 (Input):

See RA0

BUS 0 — BUS 7:

Bidirectional CPU data bus.

$\overline{\text{CLEAR}}$ (Input)

A low-level voltage at this input resets both ports to the input mode, and also resets the status register. A RDY, B RDY, and interrupt enable (disabling interrupts).

$\overline{\text{A INT}}$ — $\overline{\text{A INTERRUPT}}$ (Output):

A low-level voltage at this output indicates the presence of one of the interrupt conditions listed in Table III. This output is an open-drain NMOS device (to allow wired ORing) and must be tied to a pullup resistor, normally 10 kΩ.

FUNCTION PIN DEFINITION (Cont'd)

$\overline{\text{B INT}}$ — $\overline{\text{B INTERRUPT}}$ (Output):

A low-level voltage at this output indicates the presence of one of the interrupt conditions listed in Table III. This output is also an open-drain NMOS device and must be tied to a pullup resistor.

B RDY — B READY (Output):

This output is a handshaking or data bit I/O line in the bit-programmable mode.

B STROBE (Input):

An input handshaking line for port B in the input and output modes, and for port A when it is in the bidirectional mode. It can be used as a data bit I/O line in the bit-programmable mode except when port A is not programmed as bidirectional.

B 0 — B 7:

Data input or output lines for port B.

V_{SS}:

Ground

A 0 — A 7:

Data input or output lines for port A.

A STROBE (Input):

An input handshaking line for port A in the input, output, and bidirectional modes. It can also be used as a data bit I/O line when port A is in the bit-programmable mode.

A RDY — A READY (Output):

A output handshaking line or data bit I/O line.

TPB (Input):

A positive input pulse used as a data load, set, or reset strobe.

WR/$\overline{\text{RE}}$ — WRITE/$\overline{\text{READ ENABLE}}$ (Input):

A positive input used to write data from the CDP1851 to the CPU bus.

RD/$\overline{\text{WE}}$ — READ/$\overline{\text{WRITE ENABLE}}$ (Input):

A positive input used to read data from the CPU bus to the CDP1851 bus.

V_{DD}:

Positive supply voltage.

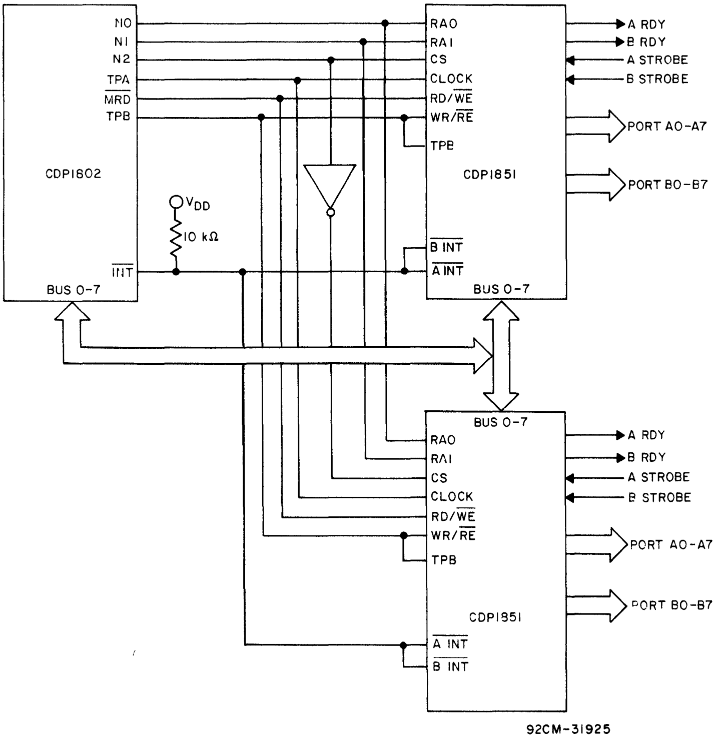


Fig. 3 - I/O space I/O.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC	V_{DD} (V)	LIMITS CDP1851			LIMITS CDP1851C			UNITS
		Min.	Typ.•	Max.+	Min.	Typ.•	Max.+	
Input Mode see Figs. 4 and 5								
Minimum Setup Times:	5	—	50	75	—	50	75	ns
Chip Select to CLOCK t_{CSCL}	10	—	25	40	—	—	—	
RD/$\overline{WE}$ to CLOCK t_{RWCL}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
WR/$\overline{RE}$ to CLOCK t_{WRCL}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
Data in to STROBE t_{DIST}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
Minimum Hold Times:	5	—	75	120	—	75	120	
Chip Select After CLOCK t_{HCSCL}	10	—	40	60	—	—	—	
Address After TPB T_{HATPB}	5	—	-50	0	—	-50	0	
	10	—	-25	0	—	—	—	
Data In After STROBE t_{HSTDI}	5	—	50	75	—	50	75	
	10	—	25	40	—	—	—	
Data Bus Out After Address t_{HADOH}	5	50	325	500	50	325	500	
	10	25	165	250	—	—	—	
Propagation Delay Times:	5	—	200	300	—	200	300	
TPB to $\overline{INT}$ t_{PINT}	10	—	100	150	—	—	—	
STROBE to $\overline{INT}$ t_{STINT}	5	—	200	300	—	200	300	
	10	—	100	150	—	—	—	
TPB to RDY t_{TPRDY}	5	—	250	375	—	250	375	
	10	—	125	200	—	—	—	
STROBE to RDY t_{STRDY}	5	—	260	400	—	260	400	
	10	—	130	200	—	—	—	
Minimum Pulse Widths:	5	—	75	120	—	75	120	
CLOCK t_{WCL}	10	—	40	60	—	—	—	
TPB t_{WTPB}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
STROBE t_{WST}	5	—	100	150	—	100	150	
	10	—	50	75	—	—	—	
Access Time, Address to Data	5	—	325	500	—	325	500	
Bus Out t_{ADA}	10	—	165	250	—	—	—	

•Typical values are for T_A = 25°C and nominal voltages.

+Maximum limits of minimum characteristics are the values above which all devices function.

CDP1851, CDP1851C

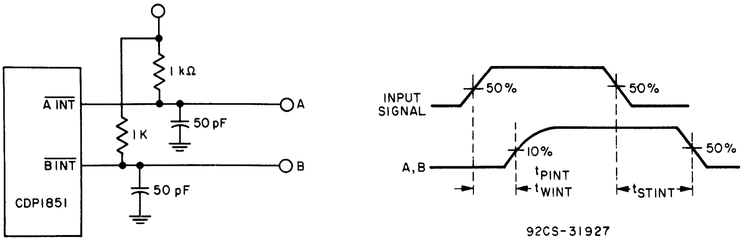


Fig. 4 - Interrupt signal propagation delay time test circuit and waveforms.

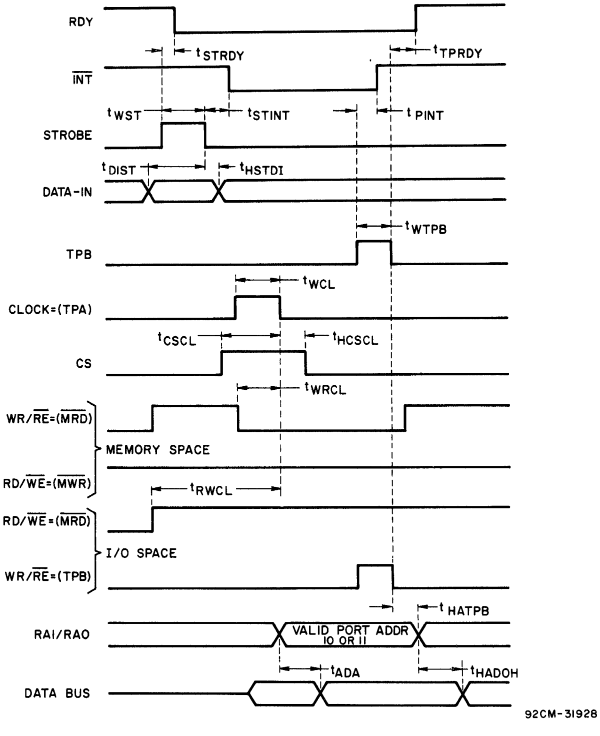


Fig. 5 - Input mode timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

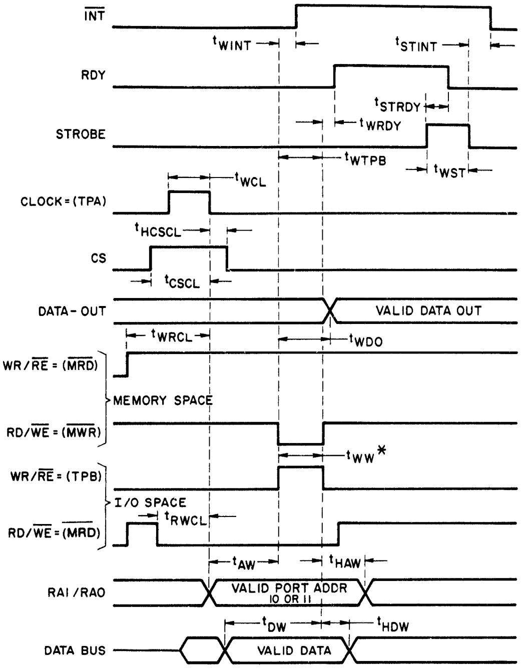
CHARACTERISTIC	V_{DD} (V)		LIMITS					UNITS
			CDP1851		CDP1851C			
		Min.	Typ.•	Max.+	Min.	Typ.•	Max.+	
Output Mode see Figs. 4 and 6								
Minimum Setup Times: Chip Select to CLOCK t_{CSCL}	5	—	50	75	—	50	75	ns
	10	—	25	40	—	—	—	
RD/$\overline{\text{WE}}$ to CLOCK t_{RWCL}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
WR/$\overline{\text{RE}}$ to CLOCK t_{WRCL}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
Address to WRITE * t_{AW}	5	—	50	75	—	50	75	
	10	—	25	40	—	—	—	
Data Bus to WRITE * t_{DW}	5	—	80	120	—	80	120	
	10	—	40	60	—	—	—	
Minimum Hold Times: Chip Select After CLOCK t_{HCSCL}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
Address After WRITE * t_{HAW}	5	—	50	75	—	50	75	
	10	—	25	40	—	—	—	
Data Bus After WRITE * t_{HDW}	5	—	50	75	—	50	75	
	10	—	25	40	—	—	—	
Propagation Delay Times: WRITE * to Data Out t_{WDO}	5	—	225	350	—	225	350	
	10	—	125	200	—	—	—	
WRITE * to $\overline{\text{INT}}$ t_{WINT}	5	—	300	450	—	300	450	
	10	—	150	225	—	—	—	
WRITE * to RDY t_{WRDY}	5	—	350	525	—	350	525	
	10	—	175	275	—	—	—	
STROBE to $\overline{\text{INT}}$ t_{STINT}	5	—	200	300	—	200	300	
	10	—	100	150	—	—	—	
STROBE to RDY t_{STRDY}	5	—	260	400	—	260	400	
	10	—	130	200	—	—	—	
Minimum Pulse Widths: CLOCK t_{WCL}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
STROBE t_{WST}	5	—	100	150	—	100	150	
	10	—	50	75	—	—	—	
WRITE * t_{WW}	5	—	175	275	—	175	275	
	10	—	90	150	—	—	—	

* WRITE is the overlap of RD/$\overline{\text{WE}}$ = 0 and WR/$\overline{\text{RE}}$ = 1.

•Typical values are for T_A = 25°C and nominal voltages.

+Maximum limits of minimum characteristics are the values above which all devices function.

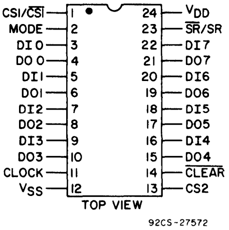
CDP1851, CDP1851C



* WRITE IS THE OVERLAP OF WR/RE = 1 AND RD/WE = 0

Fig. 6 - Output mode timing waveforms.

CDP1852, CDP1852C



CDP1852, CDP1852C
TERMINAL ASSIGNMENT

Byte-Wide Input/Output Port

Features:
- *Static silicon-gate CMOS circuitry*
- *Parallel 8-bit data register and buffer*
- *Handshaking via service request flip-flop*
- *Low quiescent and operating power*
- *Interfaces directly with CDP1800-series microprocessors*
- *Single voltage supply*
- *Full military temperature range (−55° C to +125° C)*

The RCA-CDP1852 and CDP1852C are parallel, 8-bit, mode-programmable input/output ports. They are compatible and will interface directly with CDP1800 series microprocessors. They are also useful as 8-bit address latches when used with the CDP1800 multiplexed address bus and as I/O ports in general-purpose applications.

The mode control is used to program the device as an input port (mode=0) or as an output port (mode=1). The $\overline{SR}$/SR output can be used as a signal to indicate when data is ready to be transferred. In the input mode, a peripheral device can strobe data into the CDP1852, and a microprocessor can read that data by device selection. In the output mode, a microprocessor strobes data into the CDP1852, and handshaking is established with a peripheral device when the CDP1852 is deselected.

In the input mode, data at the data-in terminals (D10-D17) is strobed into the port's 8-bit register by a high (1) level on the clock line. The negative high-to-low transition of the clock latches the data in the register and sets the service request output low ($\overline{SR}$/SR=0). When CS1/$\overline{CS1}$ and CS2 are high (CS1/$\overline{CS1}$ and CS2=1), the 3-state output drivers are enabled and data in the 8-bit register appear at the data-out terminals (D00-D07). When either CS1/$\overline{CS1}$ or CS2 goes low (CS1/$\overline{CS1}$ or CS2=0), the data-out terminals are tri-stated and the service request output returns high ($\overline{SR}$/SR=1).

In the output mode, the output drivers are enabled at all times. Data at the data-in terminals (D10-D17) is strobed into the 8-bit register when CS1/$\overline{CS1}$ is low (CS1/$\overline{CS1}$=0) and CS2 and the clock are high (1), and are present at the data-out terminals (D00-D07). The negative high-to-low transition of the clock latches the data in the register. The $\overline{SR}$/SR output goes high ($\overline{SR}$/SR=1) when the device is deselected (CS1/$\overline{CS1}$=1 or CS2=0) and returns low ($\overline{SR}$/SR=0) on the following trailing edge of the clock.

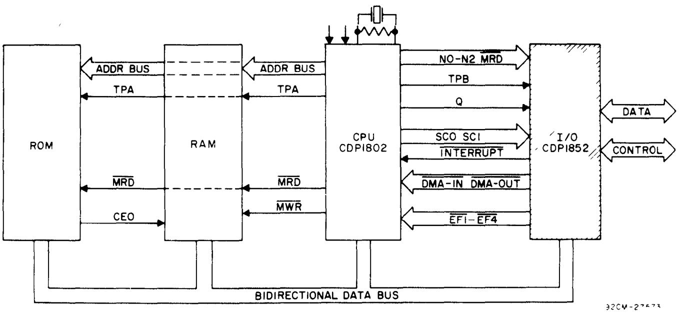


Fig. 1 - Typical CDP1802 microprocessor system.

File Number **1166**

CDP1852, CDP1852C

A $\overline{\text{CLEAR}}$ control is provided for resetting the port's register (D00-D07 = 0) and service request flip-flop (input mode: $\overline{SR}$/SR=1 and output mode: $\overline{SR}$/SR=0).

The CDP1852 is functionally identical to the CDP1852C. The CDP1852 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1852C has a recommended operating voltage range of 4 to 6.5 volts.

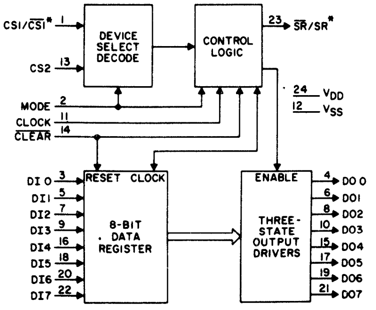
The CDP1852 and CDP1852C are supplied in 24-lead, hermetic, dual-in-line ceramic packages (D suffix), in 24-lead dual-in-line plastic packages (E suffix). The CDP1852C is also available in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal
CDP1852 .... −0.5 to +11 V
CDP1852C .... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D).
For $T_A = -40$ to $+60°$C (PACKAGE TYPE E) .... 500 mW
For $T_A = +60$ to $+85°$C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
For $T_A = -55$ to $+100°$C (PACKAGE TYPE D) .... 500 mW
For $T_A = +100$ to $+125°$C (PACKAGE TYPE D) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, H .... −55 to +125°C
PACKAGE TYPE E .... −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING).
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max .... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1852		CDP1852C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	



* POLARITY DEPENDS ON MODE

	MODE 0	MODE 1
P1	CS1	$\overline{\text{CS1}}$
P23	$\overline{SR}$	SR

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Fig 2 - Block diagram of CDP1852.

CDP1852, CDP1852C

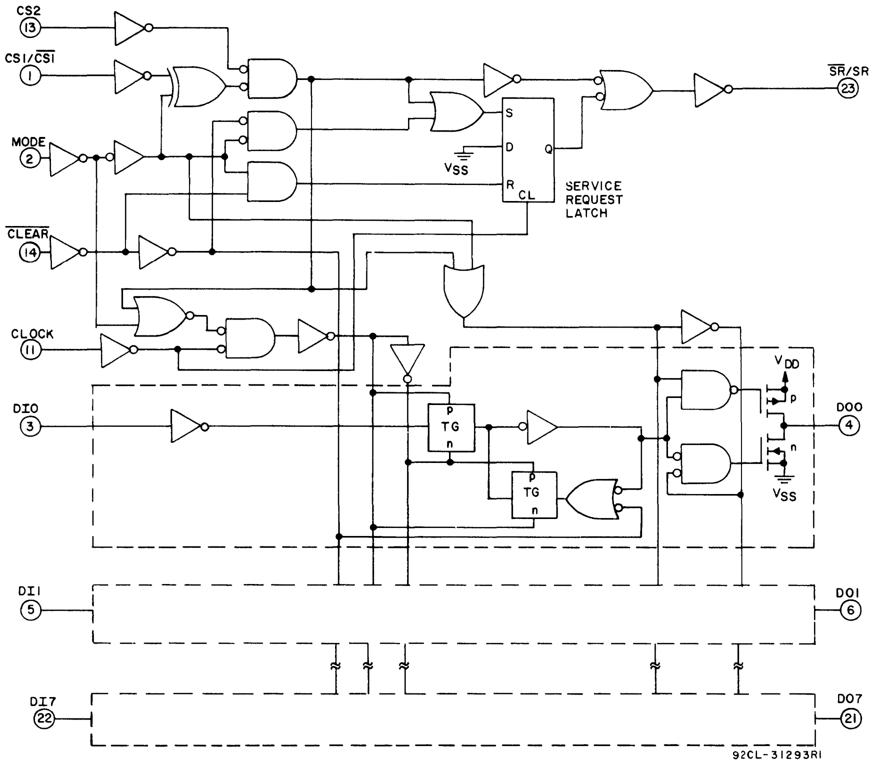


Fig 3 - CDP1852 logic diagram

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85° C

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1852			CDP1852C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	—	0,5	5	—	—	10	—	—	50	μA
	—	0,10	10	—	—	100	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0,10	10	3	6	—	—	—	—	
Output High Drive (Source) Current, I_{OH}	4.6	0,5	5	−1.15	−2.3	—	−1.15	−2.3	—	
	9.5	0,10	10	−3	−6	—	—	—	—	
Output Voltage Low Level, V_{OL}†	—	0,5	5	—	0	0.1	—	0	0.1	V
	—	0,10	10	—	0	0.1	—	—	—	
Output Voltage High Level, V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	

CDP1852, CDP1852C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$ (Cont'd)

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1852			CDP1852C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input Current, I_{IN}	—	0,5	5	—	—	±1	—	—	±1	µA
	—	0,10	10	—	—	±2	—	—	—	
3-State Output Leakage Current, I_{OUT}	0,5	0,5	5	—	—	±1	—	—	±1	
	0,10	0,10	10	—	—	±2	—	—	—	
Operating Current, I_{DD1}‡	—	0,5	5	—	130	300	—	150	300	
	—	0,10	10	—	550	800	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	5	7.5	—	—	—	

*Typical values are for $T_A = 25°C$ and nominal V_{DD}.

†$I_{OL} = I_{OH} = 1\ \mu A$

‡Operating current is measured at 2 MHz in an CDP1802 system with open outputs and a program of 6N55, 6NAA, 6N55, 6NAA, ------.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$, $V_{DD} = \pm 5\%$, t_r, $t_f = 20$ ns, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100$ pF, and 1 TTL Load

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNITS
		Min.	Typ.*	Max.	
MODE 0 — Input Port (Fig. 4)					
Minimum Select Pulse Width, t_{SW}	5	—	180	360	ns
	10	—	90	180	
Minimum Write Pulse Width, t_{WW}	5	—	90	180	
	10	—	45	90	
Minimum Clear Pulse Width, t_{CLR}	5	—	80	160	
	10	—	40	80	
Minimum Data Setup Time, t_{DS}	5	—	-10	0	
	10	—	-5	0	
Mininum Data Hold Time, t_{DH}	5	—	75	150	
	10	—	35	75	
Data Out Hold Time, t_{DOH}†	5	30	185	370	
	10	15	100	200	
Propagation Delay Times, t_{PLH}, t_{PHL}: Select to Data Out†, t_{SDO}	5	30	185	370	
	10	15	100	200	
Clear to SR, T_{RSR}	5	—	170	340	
	10	—	85	170	
Clock to SR, t_{CSR}	5	—	110	220	
	10	—	55	110	
Select to SR, t_{SSR}	5	—	120	240	
	10	—	60	120	

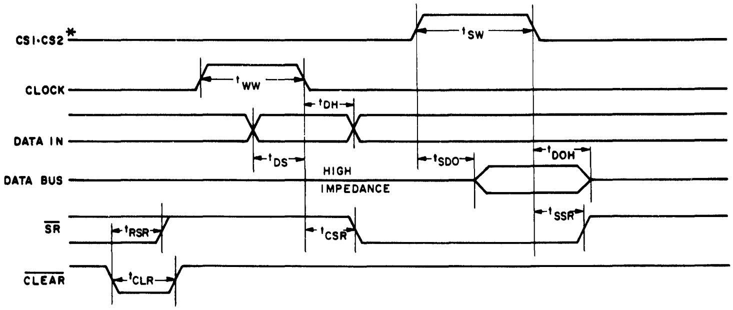
†Minimum value is measured from CS2, maximum value is measured from CS1/$\overline{CS1}$

*Typical values are for $T_A = 25°C$ and nominal V_{DD}

INPUT PORT MODE 0 — TYPICAL OPERATION

General Operation

When the mode control is tied to VSS, the CDP1852 becomes an input port. In this mode, the peripheral device places data into the CDP1852 with a strobe pulse and the CDP1852 signals the microprocessor that data is ready to be transferred on the strobe's trailing edge via the $\overline{SR}$ output line. The CDP1802 then issues an input instruction that enables the CDP1852 to place the information from the peripheral device on the data bus to be entered into a memory location and the accumulator of the microprocessor.



* CSI·CS2 IS THE OVERLAP OF CSI=I AND CS2=I

MODE 0 TRUTH TABLE

CLOCK	†CS1-CS2	$\overline{CLEAR}$	Data Out Equals
X	0	X	High Impedance
0	1	0	0
0	1	1	Data Latch
1	1	X	Data In

†CS1 CS2 CS1 1 CS2 1

SERVICE REQUEST TRUTH TABLE

CLOCK ↓	CS1 or CS2 or $\overline{CLEAR}$ ↓
$\overline{SR}$/SR 0	$\overline{SR}$/SR 1

92CM-31292R2

Fig. 4 - MODE 0 input port timing waveforms and truth tables.

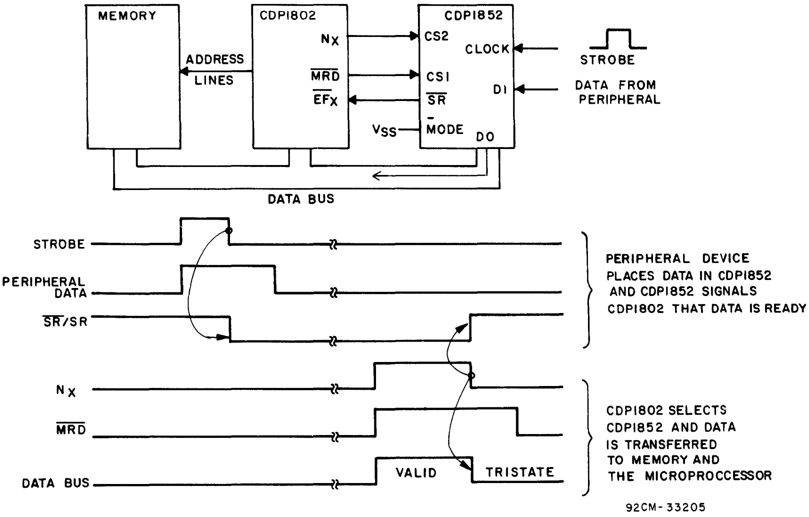

MEMORY
ADDRESS LINES
CDPI802
NX
MRD
EFX
CDPI852
CS2
CLOCK
CSI
SR
DI
VSS
MODE
DO
STROBE
DATA FROM PERIPHERAL
DATA BUS
STROBE
PERIPHERAL DATA
SR/SR
NX
MRD
DATA BUS
VALID
TRISTATE
PERIPHERAL DEVICE PLACES DATA IN CDPI852 AND CDPI852 SIGNALS CDPI802 THAT DATA IS READY
CDPI802 SELECTS CDPI852 AND DATA IS TRANSFERRED TO MEMORY AND THE MICROPROCCESSOR
92CM-33205

Fig. 5 - Input port mode 0 functional diagram and waveforms - typical operation.

Detailed Operation (See Fig. 5)

The STROBE from the peripheral device places DATA into the 8-bit register of the CDP1852 when it goes high and latches the DATA on its trailing edge. The $\overline{SR}$ output is set low on the strobe's trailing edge. This output is connected to a flag line of the CDP1802 microprocessor and software polling will determine that the flag line has gone low and peripheral data is ready to be transferred. The CDP1802 then issues an input instruction that places an N_x line high. With the $\overline{MRD}$ line also high, the CDP1852 is selected and its output drivers place the DATA from the peripheral device on the DATA BUS. When the CDP1802 selected the CDP1852, it also selected and addressed the memory via one of the 16 internal address registers selected by an internal "X" register. The data from the CDP1852 is therefore entered into the memory [Bus → M(R(X))]. The data is also transferred to the D register (accumulator) in the microprocessor (Bus → D). When the CDP1802's execute cycle is completed, the CDP1852 is deselected by the N_x line returning low and its data output pins are tri-stated. The $\overline{SR}$ output returns high.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$, $V_{DD} = \pm 5\%$, t_r, $t_f = 20$ ns, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100$ pF, and 1 TTL Load

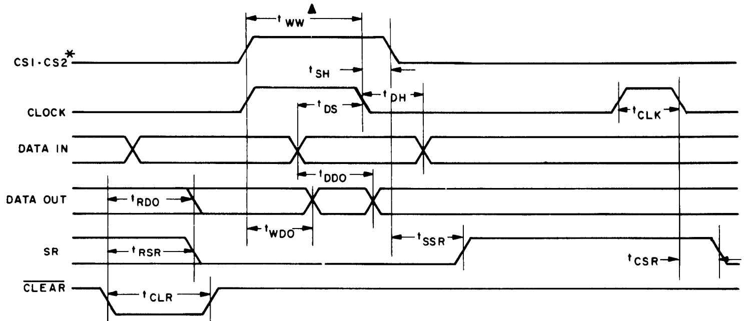
CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Typ.*	LIMITS Max.	UNITS
MODE 1 — Output Port (Fig. 6)					
Minimum Clock Pulse Width, t_{CLK}	5	—	130	260	ns
	10	—	65	130	
Minimum Write Pulse Width, t_{WW}	5	—	130	260	
	10	—	65	130	
Minimum Clear Pulse Width, t_{CLR}	5	—	60	120	
	10	—	30	60	
Minimum Data Setup Time, t_{DS}	5	—	-10	0	
	10	—	-5	0	
Minimum Data Hold Time, t_{DH}	5	—	75	150	
	10	—	35	75	
Minimum Select-after-Clock	5	—	-10	0	
Hold Time, t_{SH}	10	—	-5	0	
Propagation Delay Times, t_{PLH}, t_{PHL}:	5	—	140	280	
Clear to Data Out, t_{RDO}	10	—	70	140	
Write to Data Out, t_{WDO}	5	—	220	440	
	10	—	110	220	
Data In to Data Out, t_{DDO}	5	—	100	200	
	10	—	50	100	
Clear to SR, t_{RSR}	5	—	120	240	
	10	—	60	120	
Clock to SR, t_{CSR}	5	—	120	240	
	10	—	60	120	
Select to SR, t_{SSR}	5	—	120	240	
	10	—	60	120	

*Typical values are for $T_A = 25°C$ and nominal V_{DD}

OUTPUT PORT MODE 1 — TYPICAL OPERATION

General Operation

Connecting the mode control to V_{DD} configures the CDP1852 as an output port. The output drivers are always on in this mode, so any data in the 8-bit register will be present at the data-out lines when the CDP1852 is selected. The N line and $\overline{MRD}$ connections between the CDP1852 and CDP1802 remain the same as in the input mode configuration, but now the clock input of the CDP1852 is tied to the TPB output of the CDP1802 and the SR output of the CDP1852 will be used to signal the peripheral device that valid data is present on its input lines. The microprocessor issues an output instruction, and data from the memory is strobed into the CDP1852 with the TPB pulse. When the CDP1852 is deselected, the SR output goes high to signal the peripheral device.



* CSI·CS2 IS THE OVERLAP OF $\overline{CSI}$ = 0 AND CS2 = 1
▲ WRITE IS THE OVERLAP OF CSI·CS2 AND CLOCK

MODE 1 TRUTH TABLE

CLOCK	$\overline{CS1}$-CS2	$\overline{CLEAR}$	Data Out Equals
0	X	0	0
0	X	1	Data Latch
X	0	1	Data Latch
1	1	X	Data In

$\overline{CS1}$ CS2 $\overline{CS1}$ 0 CS2 1

SERVICE REQUEST TRUTH TABLE

$\overline{CS1}$ ▲ or CS2 ▼	CLOCK or $\overline{CLEAR}$ ⤶
$\overline{SR}$ SR 1	$\overline{SR}$ SR 0

92CM-31295R1

Fig 6 - MODE 1 output port timing waveforms and truth tables

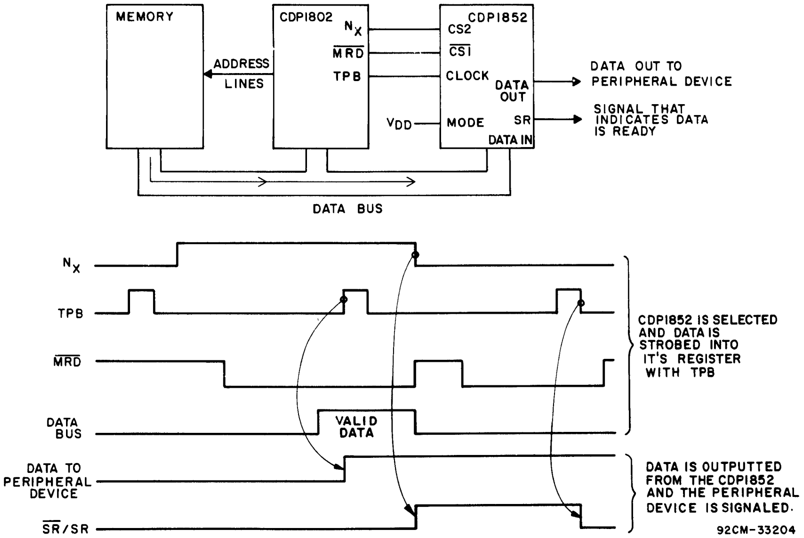

MEMORY
CDP1802
N_X
$\overline{MRD}$
TPB
ADDRESS LINES
CDP1852
CS2
$\overline{CS1}$
CLOCK
DATA OUT
MODE
SR
DATA IN
VDD
DATA OUT TO PERIPHERAL DEVICE
SIGNAL THAT INDICATES DATA IS READY
DATA BUS
N_X
TPB
$\overline{MRD}$
DATA BUS
VALID DATA
DATA TO PERIPHERAL DEVICE
$\overline{SR}$/SR
CDP1852 IS SELECTED AND DATA IS STROBED INTO IT'S REGISTER WITH TPB
DATA IS OUTPUTTED FROM THE CDP1852 AND THE PERIPHERAL DEVICE IS SIGNALED.
92CM-33204

Fig. 7 - Output port mode 1 functional diagram and waveforms - typical operation

Detailed Operation (See Fig 7)

The CDP1802 issues an output instruction The N_x line goes high and the $\overline{MRD}$ line goes low. The memory is accessed M(R(X)) → BUS and places data on the DATA BUS This data are strobed into the 8-bit register of the CDP1852 when TPB goes high and latched on the TPB's trailing edge. The valid data thus appears on the CDP1852 output lines. When the CDP1802 output instruction cycle is complete, the N_x line goes low and the SR output goes high SR will remain high until the trailing edge of the next TPB pulse, when it will return low.

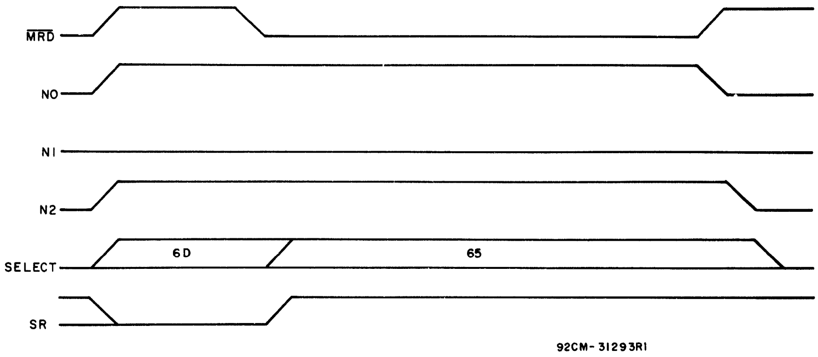


Fig. 8 - Execution of a "65" output instruction showing momentary selection of input port "D".

Application Information

In a CDP1800 series microprocessor-based system where $\overline{MRD}$ is used to distinguish between INP and OUT instructions, an INP instruction is assumed to occur at the beginning of every I/O cycle because $\overline{MRD}$ starts high Therefore, at the start of an OUT instruction, which uses the same 3-bit N code as that used for selection of an input port, the input device is selected for a short time (see Fig. 8). This condition forces SR low and sets the internal SR latch (see Fig. 3). In a small system with unique N codes for inputs and outputs, this situation does not arise. Using the CDP1853 N-bit decoder or equivalent logic to decode the N lines after TPA prevents dual selection in larger systems (see Fig. 9 and Fig. 10).

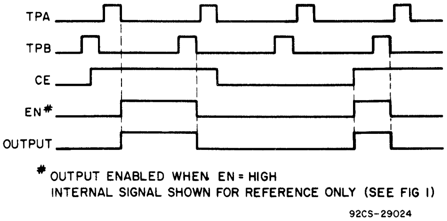

TPA
TPB
CE
EN*
OUTPUT
* OUTPUT ENABLED WHEN EN = HIGH
INTERNAL SIGNAL SHOWN FOR REFERENCE ONLY (SEE FIG 1)
92CS-29024

Fig 9 - CDP1853 timing waveforms

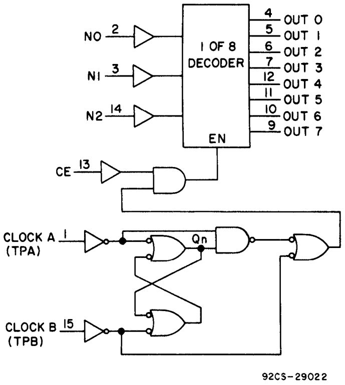
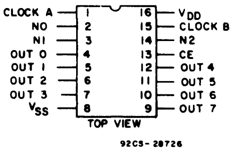


Fig 10 - CDP1853 functional diagram.

CDP1853, CDP1853C

TERMINAL ASSIGNMENT



N-Bit 1 of 8 Decoder

Features:

- *Provides direct control of up to 7 input and 7 output devices*
- *CHIP ENABLE (CE) allows easy expansion for multi-level I/O systems*

The RCA-CDP1853 and CDP1853C are 1 of 8 decoders designed for use in general purpose microprocessor systems. These devices, which are functionally identical, are specifically designed for use as gated N-bit decoders and interface directly with the 1800-series microprocessors without additional components. The CDP1853 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1853C has a recommended operating voltage range of 4 to 6.5 volts.

When CHIP ENABLE (CE) is high, the selected output will be true (high) from the trailing edge of CLOCK A (high-to-low transition) to the trailing edge of CLOCK B (high-to-low transition). All outputs will be low when the device is not selected (CE=0) and during conditions of CLOCK A and CLOCK B as shown in Fig. 2. The CDP1853 inputs N0, N1, N2, CLOCK A, and CLOCK B are connected to an 1800 series microprocessor outputs N0, N1, N2, TPA, and TPB respectively, when used to decode I/O commands as shown in Fig. 5. The CHIP ENABLE (CE) input provides the capability for multiple levels of decoding as shown in Fig. 6.

The CDP1853 can also be used as a general 1 of 8 decoder for I/O and memory system applications as shown in Fig. 4.

The CDP1853 and CDP1853C are supplied in hermetic 16-lead dual-in-line ceramic (D suffix) and plastic (E suffix) packages.

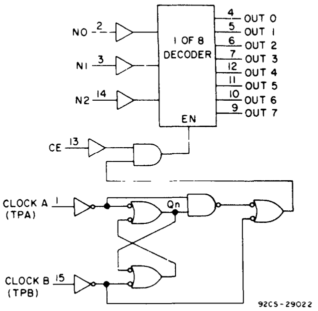


Fig. 1 - CDP1853 functional diagram.

TRUTH TABLE

CE	CL A	CL B	EN
1	0	0	Qn-1*
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

N2	N1	N0	EN	0	1	2	3	4	5	6	7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

1 = High level 0 = Low level X = Don't care
*Qn-1 = Enable remains in previous state.

CDP1853, CDP1853C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (All voltage values referenced to V_{SS} terminal	
CDP1853	−0.5 to + 11 V
CDP1853C	−0.5 to + 7 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
OPERATING-TEMPERATURE RANGE (T_A):	
CERAMIC PACKAGES (D SUFFIX TYPES)	−55 to + 125°C
PLASTIC PACKAGES (E SUFFIX TYPES)	−40 to + 85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to + 150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ±1/32 inch (1.59±0.79 mm) from case for 10 s max.	+265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C. Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1853			CDP1853C			
	VO (V)	VIN (V)	VDD (V)	Min.	Typ.†	Max.	Min.	Typ.†	Max.	
Quiescent Device Current, I_L	–	–	5	–	1	10	–	5	50	μA
	–	–	10	–	10	100	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	–	1.6	3.2	–	mA
	0.5	0,10	10	2.6	5.2	–	–	–	–	
Output High Drive (Source Current) I_{OH}	4.6	0,5	5	-1.15	-2.3	–	-1.15	-2.3	–	mA
	9.5	0,10	10	-2.6	-5.2	–	–	–	–	
Output Voltage Low-Level ▲ V_{OL}	–	0,5	5	–	0	0.1	–	0	0.1	V
	–	0,10	10	–	0	0.1	–	–	–	
Output Voltage High Level V_{OH}	–	0,5	5	4.9	5	–	4.9	5	–	
	–	0,10	10	9.9	10	–	–	–	–	
Input Low Voltage V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	1,9	–	10	–	–	3	–	–	–	
Input High Voltage V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	1,9	–	10	7	–	–	–	–	–	
Input Leakage Current I_{IN}	Any	0,5	5	–	–	±1	–	–	±1	μA
	Input	0,10	10	–	–	±1	–	–	–	
Operating Current I_{DD1}*	0,5	0,5	5	–	50	100	–	50	100	μA
	0,10	0,10	10	–	150	300	–	–	–	
Input Capacitance C_{IN}	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance C_{OUT}	–	–	–	–	10	15	–	10	15	pF

† Typical values are for T_A = 25°C and nominal voltage.

* Operating current measured in a CDP1802 system at 2MHz with outputs floating.

▲ $I_{OL} = I_{OH} = 1 \mu A$

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

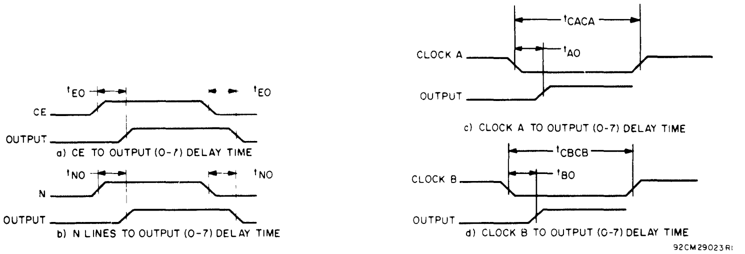
CHARACTERISTIC	LIMITS				UNITS
	CDP1853		CDP1853C		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD}=± 5%, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, t_r, t_f = 20 ns, C_L = 100pF

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		CDP1853		CDP1853C		
		Typ.	Max.	Typ.	Max.	
Propagation Delay Time: CE to Output, t_{EOH}, t_{EOL}	5	175	275	175	275	ns
	10	90	150	–	–	
N to Outputs, t_{NOH}, t_{NOL}	5	225	350	225	350	ns
	10	120	200	–	–	
Clock A to Output, t_{AO}	5	200	300	200	300	ns
	10	100	150	–	–	
Clock B to Output, t_{BO}	5	175	275	175	275	ns
	10	90	150	–	–	
Minimum Pulse Widths: Clock A, t_{CACA}	5	50	75	50	75	ns
	10	25	50	–	–	
Clock B, t_{CBCB}	5	50	75	50	75	
	10	25	50	–	–	

Note 1: Maximum limits of minimum characteristics are the values above which all devices function.

Note 2: Typical values are for T_A = 25°C and nominal voltages.



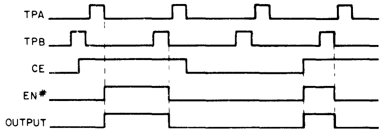
a) CE TO OUTPUT (O-7) DELAY TIME

b) N LINES TO OUTPUT (O-7) DELAY TIME

c) CLOCK A TO OUTPUT (O-7) DELAY TIME

d) CLOCK B TO OUTPUT (O-7) DELAY TIME

Fig 2 – Propagation delay time diagrams.



* OUTPUT ENABLED WHEN EN = HIGH
INTERNAL SIGNAL SHOWN FOR REFERENCE ONLY (SEE FIG 1)

Fig. 3 – Timing diagram.

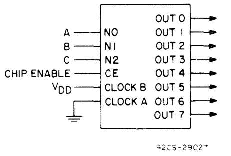


Fig. 4 – N-bit decoder used as a 1 of 8 decoder.

CDP1853, CDP1853C

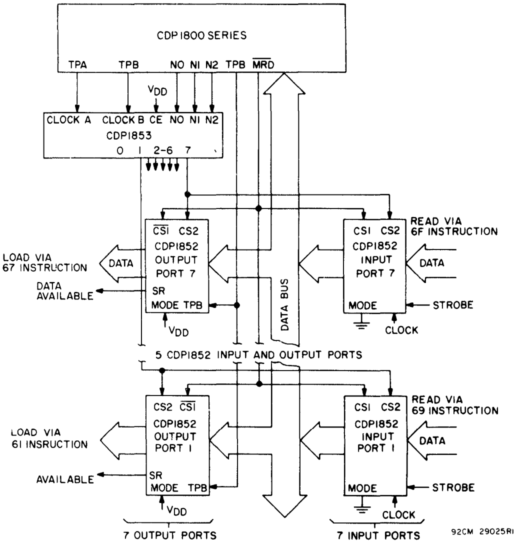


Fig. 5 – N-bit decoder in a one-level I/O system.

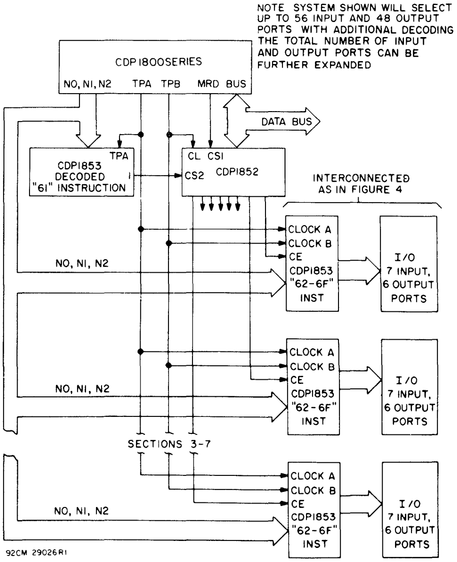
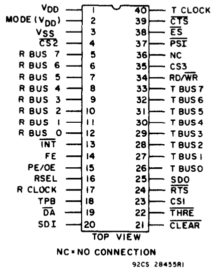

NOTE SYSTEM SHOWN WILL SELECT UP TO 56 INPUT AND 48 OUTPUT PORTS WITH ADDITIONAL DECODING THE TOTAL NUMBER OF INPUT AND OUTPUT PORTS CAN BE FURTHER EXPANDED

Fig. 6 – Two-level I/O using CDP1853 and CDP1852.

CDP1854A, CDP1854AC



Mode 1
Terminal Assignment

Programmable Universal Asynchronous Receiver/Transmitter (UART)

Features:

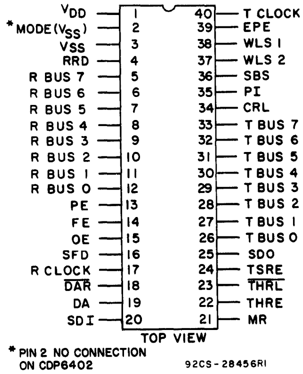
- *Two operating modes:*
  Mode 0-functionally compatible with industry types such as the TR1602A
  Mode 1-interfaces directly with CDP1800-series microprocessors without additional components
- *Full- or half-duplex operation*
- *Parity, framing, and overrun error detection*
- *Baud rate-DC to 200 K bits/sec @ V_{DD}=5 V*
  DC to 400 K bits/sec @ V_{DD}=10 V
- *Fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1½, or 2 stop bits*
- *False start bit detection*

The RCA CDP1854A and CDP1854AC are silicon-gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data. For example, these UARTs can be used to interface between a peripheral or terminal with serial I/O ports and the 8-bit CDP1800-series microprocessor parallel data bus system. The CDP1854A is capable of full duplex operation, i.e., simultaneous conversion of serial input data to parallel output data and parallel input data to serial output data.

The CDP1854A UART can be programmed to operate in one of two modes by using the mode control input. When the mode input is high (MODE=1), the CDP1854A is directly compatible with the CDP1800-series microprocessor system without additional interface circuitry. When the mode input is low (MODE=0), the device is functionally compatible with industry standard UART's such as the TR1602A. It is also pin compatible with these types, except that pin 2 is used for the mode control input instead of a V_{GG}=−12 V supply connection.

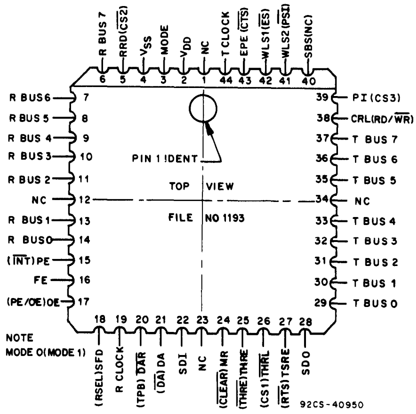
The CDP1854A and the CDP1854AC are functionally identical. The CDP1854A has a recommended operating-voltage range of 4-10.5 volts, and the CDP1854AC has a recommended operating-voltage range of 4-6.5 volts.

The CDP1854A and CDP1854AC are supplied in hermetic 40-lead dual-in-line ceramic packages (D suffix), in 40-lead dual-in-line plastic packages (E suffix), and in 44-lead plastic chip-carrier packages (Q suffix). The CDP1854AC is also available in chip form (H suffix).



Mode 0
Terminal Assignment

TERMINAL ASSIGNMENT



44-Lead Plastic Chip-Carrier Package
(Q Suffix)

File Number **1193**

CDP1854A, CDP1854AC

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltage referenced to V_{SS} terminal)	
CDP1854A	-0.5 to +11 V
CDP1854AC	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to 100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -40 to +85°C (PACKAGE TYPE Q)*	500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E and Q	-40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

Mode Input High (Mode = 1)

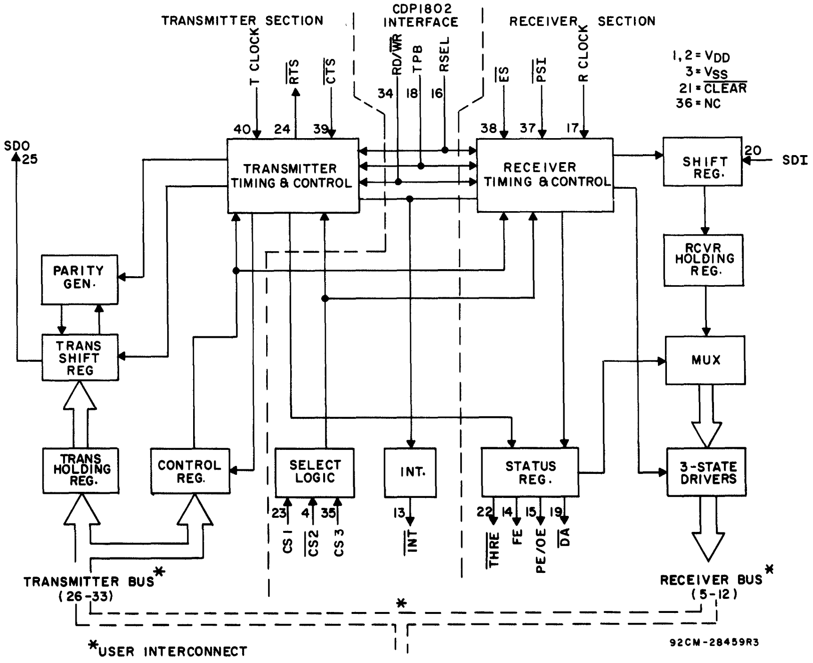


Fig. 1 - Mode 1 block diagram (CDP1800-series microprocessor compatible).

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, unless otherwise noted.

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1854A			CDP1854AC			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	µA
	—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current, I_{OL} (Except pins 24 and 25)	0.4	0, 5	5	1	2	—	1	2	—	mA
	0.5	0, 10	10	2	4	—	—	—	—	
Output High Drive (Source) Current, I_{OH}	4.6	0, 5	5	−0.55	−1.1	—	−0.55	−1.1	—	mA
	9.5	0, 10	10	−1.3	−2.6	—	—	—	—	
Output Low Drive (Sink) Current, I_{OL} Pins 24 and 25	0.4	0, 5	5	1.6	3.5	—	1.6	3.5	—	mA
	0.5	0, 10	10	3.2	7	—	—	—	—	
Output Voltage Low-Level, V_{OL}*	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High-Level, V_{OH} *	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	
Input Current, I_{IN}	—	0, 5	5	—	—	±1	—	—	±1	µA
	—	0, 10	10	—	—	±2	—	—	—	
3-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	—	—	±1	—	—	±1	µA
	0, 10	0, 10	10	—	—	±10	—	—	—	
Operating Current, I_{DD1}#	—	0, 5	5	—	1.5	—	—	1.5	—	mA
	—	0, 10	10	—	6	—	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	

*Typical values are for T_A=25° C. *I_{OL}=I_{OH}=1 µA.

#Operating current is measured at 200 kHz for V_{DD}=5 V and 400 kHz for V_{DD}=10 V in a CDP1800-series microprocessor system, with open outputs

RECOMMENDED OPERATING CONDITIONS at T_A=Full Package Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD}	CDP1854A		CDP1854AC		
	V	Min.	Max.	Min.	Max.	
DC Operating-Voltage Range	—	4	10.5	4	6.5	V
Input Voltage Range	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Baud Rate (Receive or Transmit)	5	—	200	—	200	K bits /sec
	10	—	400	—	—	

CDP1854A, CDP1854AC

Functional Definitions for CDP1854A Terminals
Mode 1
CDP1800-Series Microprocessor Compatible
SIGNAL: FUNCTION

V_{DD}:
Positive supply voltage

MODE SELECT (MODE):
A high-level voltage at this input selects CDP1800-series microprocessor Mode operation.

V_{SS}:
Ground

CHIP SELECT 2 (CS2):
A low-level voltage at this input together with CS1 and CS3 selects the CDP1854A UART.

RECEIVER BUS (R BUS 7 - R BUS 0):
Receiver parallel data outputs (may be externally connected to corresponding transmitter bus terminals).

INTERRUPT (INT):
A low-level voltage at this output indicates the presence of one or more of the interrupt conditions listed in Table I.

FRAMING ERROR (FE):
A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register.

PARITY ERROR or OVERRUN ERROR (PE/OE):
A high-level voltage at this output indicates that either the PE or OE bit in the Status Register has been set (see Status Register Bit Assignment, Table II.

REGISTER SELECT (RSEL):
This input is used to choose either the Control/Status Registers (high input) or the transmitter/receiver data registers (low input) according to the truth table in Table III.

RECEIVER CLOCK (RCLOCK):
Clock input with a frequency 16 times the desired receiver shift rate.

TPB:
A positive input pulse used as a data load or reset strobe.

DATA AVAILABLE (DA):
A low-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):
Serial data received on this input line enters the Receiver Shift Register at a point determined by the character length. A high-level input voltage must be present when data is not being received.

CLEAR (CLEAR):
A low-level voltage at this input resets the Interrupt Flip-Flop, Receiver Holding Register, Control Register, and Status Register, and sets SERIAL DATA OUT (SDO) high.

TRANSMITTER HOLDING REGISTER EMPTY (THRE):
A low-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

CHIP SELECT 1 (CS1):
A high-level voltage at this input together with CS2 and CS3 selects the UART.

REQUEST TO SEND (RTS):
This output signal tells the peripheral to get ready to receive data. CLEAR TO SEND (CTS) is the response from the peripheral. RTS is set to a low-level voltage when data is latched in the Transmitter Holding Register or TR is set high, and is reset high when both the Transmitter Holding Register and Transmitter Shift Register are empty and TR is low.

SERIAL DATA OUTPUT (SDO):
The contents of the Transmitter Shift Register [start bit, data bits, parity bit, and stop bit(s)] are serially shifted out on this output. When no character is being transmitted, a high level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):
Transmitter parallel data input. These may be externally connected to corresponding Receiver bus terminals.

RD/WR:
A low-level voltage at this input gates data from the transmitter bus to the Transmitter Holding Register or the Control Register as chosen by register select. A high-level voltage gates data from the Receiver Holding Register or the Status Register, as chosen by register select, to the receiver bus.

CHIP SELECT 3 (CS3):
With high-level voltage at this input together with CS1 and CS2 selects the UART.

PERIPHERAL STATUS INTERRUPT (PSI):
A high-to-low transition on this input line sets a bit in the Status Register and causes an INTERRUPT (INT=low).

EXTERNAL STATUS (ES):
A low-level voltage at this input sets a bit in the Status Register.

CLEAR TO SEND (CTS):
When this input from peripheral is high, transfer of a character to the Transmitter Shift Register and shifting of serial data out is inhibited.

TRANSMITTER CLOCK (TCLOCK):
Clock input with a frequency 16 times the desired transmitter shift rate.

Table I — Interrupt Set and Reset Conditions

SET* (INT = LOW)	RESET (INT = HIGH)	
CAUSE	**CONDITION**	**TIME**
DA (Receipt of data)	Read of data	TPB leading edge
THRE★ (Ability to reload)	Read of status or write of character	TPB leading edge
THRE · TSRE (Transmitter done)	Read of status or write of character	TPB leading edge
$\overline{\text{PSI}}$ (Negative edge)	Read of status	TPB trailing edge
$\overline{\text{CTS}}$ (Positive edge when $\overline{\text{THRE} \cdot \text{TSRE}}$)	Read of status	TPB leading edge

*Interrupts will occur only after the IE bit in the Control Register (see Table IV) has been set.

★THRE will cause an interrupt only after the TR bit in the Control Register (see Table IV) has been set

Table II — Status Register Bit Assignment

Bit	7	6	5	4	3	2	1	0
Signal	THRE	TSRE	PSI	ES	FE	PE	OE	DA
Also Available at Terminal	22*	—	—	—	14	15	15	19*

*Polarity reversed at output terminal.

Bit Signal: Function

0—DATA AVAILABLE (DA):
When set high, this bit indicates that an entire character has been received and transferred to the Receiver Holding Register. This signal is also available at Term. 19 but with its polarity reversed.

1—OVERRUN ERROR (OE):
When set high, this bit indicates that the Data Available bit was not reset before the next character was transferred to the Receiver Holding Register. This signal OR'ed with PE is output at Term. 15.

2—PARITY ERROR (PE):
When set high, this bit indicates that the received parity bit does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal OR'ed with OE is output at Term. 15.

3—FRAMING ERROR (FE):
When set high, this bit indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal is also available at Term. 14.

4—EXTERNAL STATUS (ES):
This bit is set high by a low-level input at Term. 38 ($\overline{\text{ES}}$).

5—PERIPHERAL STATUS INTERRUPT (PSI):
This bit is set high by a high-to-low voltage transition of Term. 37 ($\overline{\text{PSI}}$). The INTERRUPT output (Term. 13) is also asserted ($\overline{\text{INT}}$=low) when this bit is set.

6—TRANSMITTER SHIFT REGISTER EMPTY (TSRE):
When set high, this bit indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains set until the start of transmission of the next character.

7—TRANSMITTER HOLDING REGISTER EMPTY (THRE):
When set high, this bit indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character. Setting this bit also sets the $\overline{\text{THRE}}$ output (Term. 22) low and causes an INTERRUPT ($\overline{\text{INT}}$=low), if TR is high.

CDP1854A, CDP1854AC

Description of Mode 1 Operation CDP1800-Series Microprocessor Compatible (Mode Input=V_{DD})

1. Initialization and Controls

In the CDP1800-series microprocessor compatible mode, the CDP1854A is configured to receive commands and send status via the microprocessor data bus. The register connected to the transmitter bus or the receiver bus is determined by the RD/$\overline{\text{WR}}$ and RSEL inputs as follows:

Table III — Register Selection Summary

RSEL	RD/$\overline{\text{WR}}$	Function
Low	Low	Load Transmitter Holding Register from Transmitter Bus
Low	High	Read Receiver Holding Register from Receiver Bus
High	Low	Load Control Register from Transmitter Bus
High	High	Read Status Register from Receiver Bus

In this mode the CDP1854A is compatible with a bidirectional bus system. The receiver and transmitter buses are connected to the bus. CDP1800-series microprocessor I/O control output signals can be connected directly to the CDP1854A inputs as shown in Fig. 2. The CLEAR input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting SERIAL DATA OUT (SDO) high. The Control Register is loaded from the Transmitter Bus in order to determine the operating configuration for the UART. Data is transferred from the Transmitter Bus inputs to the Control Register during TPB when the UART is selected (CS1 · $\overline{\text{CS2}}$ · CS3=1) and the Control Register is designated (RSEL=H, RD/$\overline{\text{WR}}$=L). The CDP1854A also has a Status Register which can be read onto the Receiver Bus (R BUS 0 - R BUS 7) in order to determine the status of the UART. Some of these status bits are also available at separate terminals as indicated in Table II.

2. Transmitter Operation

Before beginning to transmit, the TRANSMIT REQUEST (TR) bit in the Control Register (see bit assignment, Table IV) is set. Loading the Control Register with TR=1 (bit 7=high) inhibits changing the other control bits. Therefore two loads are required: one to format the UART, the second to set TR. When TR has been set, a $\overline{\text{TRANSMITTER HOLDING REGISTER EMPTY}}$ ($\overline{\text{THRE}}$) interrupt will occur, signalling the microprocessor that the Transmitter Holding Register is empty and may be loaded. Setting TR also causes assertion of a low-level on the REQUEST TO SEND ($\overline{\text{RTS}}$) output to the peripheral. It is not necessary to set TR for proper operation for the UART. If desired, it can be used to enable $\overline{\text{THRE}}$ interrupts and to generate the $\overline{\text{RTS}}$ signal. The Transmitter Holding Register is loaded from the bus by TPB during execution of an output instruction. The CDP1854A is selected by CS1 · $\overline{\text{CS2}}$ · CS3=1, and the Holding Register is selected by RSEL=L and RD/$\overline{\text{WR}}$=L. When the $\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$) input, which can be connected to a peripheral device output, goes low, the Transmitter Shift Register will be loaded from the Transmitter Holding Register and data transmission will begin. If $\overline{\text{CTS}}$ is always low, the Transmitter Shift Register will be loaded on the first high-to-low edge of the clock which occurs at least 1/2 clock period after the trailing edge of TPB and transmission of a start bit will occur 1/2 clock period later (see Fig. 3). Parity (if programmed) and stop bit(s) will be transmitted following the last data bit. If the word length selected is less than 8 bits, the most significant unused bits in the transmitter shift register will not be transmitted.

One transmitter clock period after the Transmitter Shift Register is loaded from the Transmitter Holding Register, the $\overline{\text{THRE}}$ signal will go low and an interrupt will occur ($\overline{\text{INT}}$ goes low). The next character to be transmitted can then be loaded into the Transmitter Holding Register for transmission with its start bit immediately following the last stop bit of the previous character. This cycle can be repeated until the last character is transmitted, at which time a final THRE · TSRE interrupt will occur. This interrupt signals the microprocessor that TR can be turned off. This is done by reloading the original control byte in the Control Register with the TR bit = 0, thus terminating the $\overline{\text{REQUEST TO SEND}}$ ($\overline{\text{RTS}}$) signal.

SERIAL DATA OUT (SDO) can be held low by setting the BREAK bit in the Control Register (see Table IV). SDO is held low until the BREAK bit is reset.

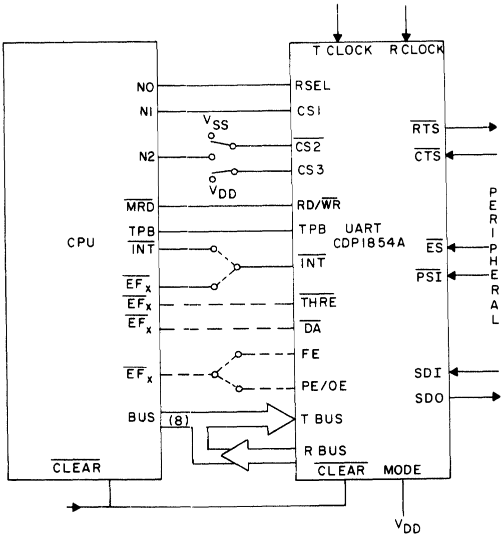


Fig. 2 - Recommended CDP1800-series connection, Mode 1 (non-interrupt driven system).

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After detection of the first high-to-low transition on the SDI line, a valid start bit is verified by checking for a low-level input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed) and stop bit(s) are shifted into the Receiver Shift Register by clock pulse 7-1/2 in each bit time. The parity bit (if programmed) is checked and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output level) are loaded into the unused most significant bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) status bit is set. One half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) status bits become valid for the character in the Receiver Holding Register. At this time, the Data Available status bit is also set and the DATA AVAILABLE (DA) and INTERRUPT (INT) outputs go low, signalling the microprocessor that a received character is ready. The microprocessor responds by executing an input instruction. The UART's 3-state bus drivers are enabled when the UART is selected (CS1 · $\overline{\text{CS2}}$ · CS3=1) and RD/$\overline{\text{WR}}$=high. Status can be read when RSEL=high. Data is read when RSEL=low. When reading data, TPB latches data in the microprocessor and resets DATA AVAILABLE ($\overline{\text{DA}}$) in the UART. The preceding sequence is repeated for each serial character which is received from the peripheral.

4. Peripheral Interface

In addition to serial data in and out, four signals are provided for communication with a peripheral. The REQUEST TO SEND ($\overline{\text{RTS}}$) output signal alerts the peripheral to get ready to receive data. The CLEAR TO SEND ($\overline{\text{CTS}}$) input signal is the response, signalling that the peripheral is ready. The EXTERNAL STATUS ($\overline{\text{ES}}$) input latches a peripheral status level, and the PERIPHERAL STATUS INTERRUPT ($\overline{\text{PSI}}$) input senses a status edge (high-to-low) and also generates an interrupt. For example, the modem DATA CARRIER DETECT line could be connected to the PSI input on the UART in order to signal the microprocessor that transmission failed because of loss of the carrier on the communications line. The PSI and ES bits are stored in the Status Register (see Table II).

Table IV — Control Register Bit Assignment

Bit	7	6	5	4	3	2	1	0
Signal	TR	BREAK	IE	WLS2	WLS1	SBS	EPE	PI

Bit Signal: Function

0—PARITY INHIBIT (PI):
When set high parity generation and verification are inhibited and the PE Status bit is held low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission, and EPE is ignored.

1—EVEN PARITY ENABLE (EPE):
When set high, even parity is generated by the transmitter and checked by the receiver. When low, odd parity is selected.

2—STOP BIT SELECT (SBS):
See table below.

3—WORD LENGTH SELECT 1 (WLS1):
See table below.

4—WORD LENGTH SELECT 2 (WLS2):
See table below.

5—INTERRUPT ENABLE (IE).
When set high $\overline{\text{THRE}}$, DA, THRE · TSRE, $\overline{\text{CTS}}$, and PSI interrupts are enabled (see Interrupt Conditions, Table I).

6—TRANSMIT BREAK (BREAK):
Holds SDO low when set. Once the break bit in the control register has been set high, SDO will stay low until the break bit is reset low and one of the following occurs: $\overline{\text{CLEAR}}$ goes low; $\overline{\text{CTS}}$ goes high; or a word is transmitted. (The transmitted word will not be valid since there can be no start bit if SDO is already low. SDO can be set high without intermediate transitions by transmitting a word consisting of all zeros).

7—TRANSMIT REQUEST (TR):
When set high, $\overline{\text{RTS}}$ is set low and data transfer through the transmitter is initiated by the initial $\overline{\text{THRE}}$ interrupt. (When loading the Control Register from the bus, this (TR) bit inhibits changing of other control flip-flops)

Bit 4	Bit 3	Bit 2	Function
WLS2	**WLS1**	**SBS**	
0	0	0	5 data bits, 1 stop bit
0	0	1	5 data bits, 1.5 stop bits
0	1	0	6 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	1	1	8 data bits, 2 stop bits

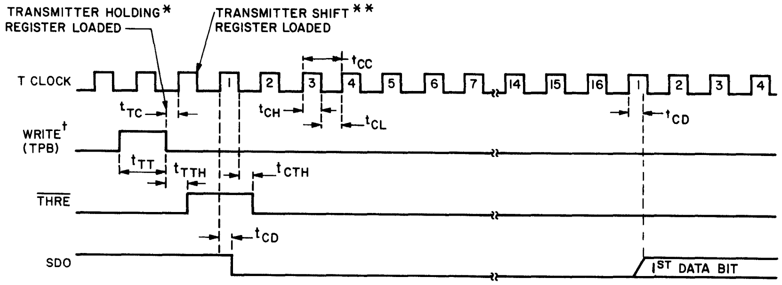
CDP1854A, CDP1854AC

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ±5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=100 pF, see Fig. 3.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			Typ.†	Max.*	Typ.†	Max.*	
Transmitter Timing — Mode 1							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	—	—	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	—	—	
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	—	—	
TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	—	—	
Minimum Setup Time: TPB to Clock	t_{TC}	5	175	225	175	225	ns
		10	90	150	—	—	
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	—	—	
TPB to $\overline{\text{THRE}}$	t_{TTH}	5	200	300	200	300	ns
		10	100	150	—	—	
Clock to $\overline{\text{THRE}}$	t_{CTH}	5	200	300	200	300	ns
		10	100	150	—	—	

†Typical values are for T_A=25°C and nominal voltages.

*Maximum limits of minimum characteristics are the values above which all devices function



* THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF TPB

** THE TRANSMITTER SHIFT REGISTER IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD + t_{TC} AFTER THE TRAILING EDGE OF TPB, AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER

† WRITE IS THE OVERLAP OF TPB, CSI, AND CS3 = 1 AND $\overline{\text{CS3}}$, RD/$\overline{\text{WR}}$ = 0

92CM-31878

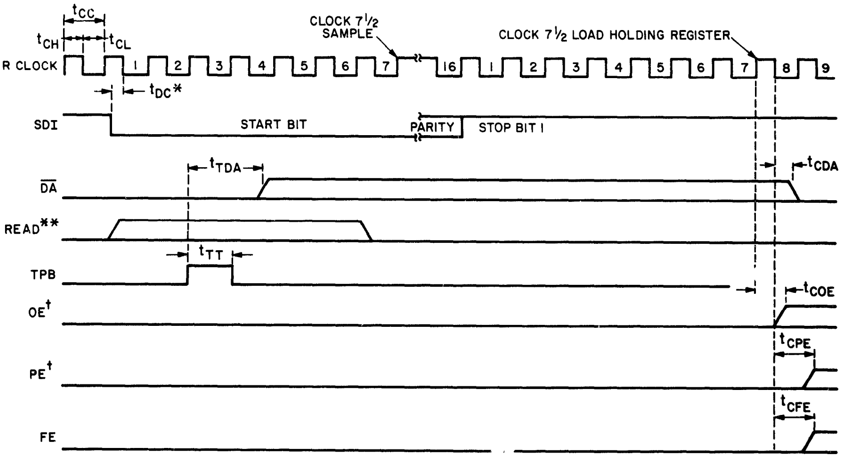
Fig. 3 - Transmitter timing diagram - Mode 1.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ±5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=100 pF, see Fig. 4.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			Typ.†	Max.*	Typ.†	Max.*	
Receiver Timing — Mode 1							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	—	—	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	—	—	
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	—	—	
TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	—	—	
Minimum Setup Time: Data Start Bit to Clock	t_{DC}	5	100	150	100	150	ns
		10	50	75	—	—	
Propagation Delay Time: TPB to $\overline{\text{DATA AVAILABLE}}$	t_{TDA}	5	220	325	220	325	ns
		10	110	175	—	—	
Clock to $\overline{\text{DATA AVAILABLE}}$	t_{CDA}	5	220	325	220	325	ns
		10	110	175	—	—	
Clock to Overrun Error	t_{COE}	5	210	300	210	300	ns
		10	105	150	—	—	
Clock to Parity Error	t_{CPE}	5	240	375	240	375	ns
		10	120	175	—	—	
Clock to Framing Error	t_{CFE}	5	200	300	200	300	ns
		10	100	150	—	—	

†Typical values are for T_A=25° C and nominal voltages.

*Maximum limits of minimum characteristics are the values above which all devices function.



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

** READ IS THE OVERLAP OF CS1, CS3, RD/$\overline{\text{WR}}$=1 AND $\overline{\text{CS2}}$=0.
IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE

† OE AND PE SHARE TERMINAL 15 AND ARE ALSO AVAILABLE AS TWO SEPARATE BITS IN THE STATUS REGISTER

Fig. 4 - Mode 1 receiver timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ±5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=100 pF, see Fig. 5.

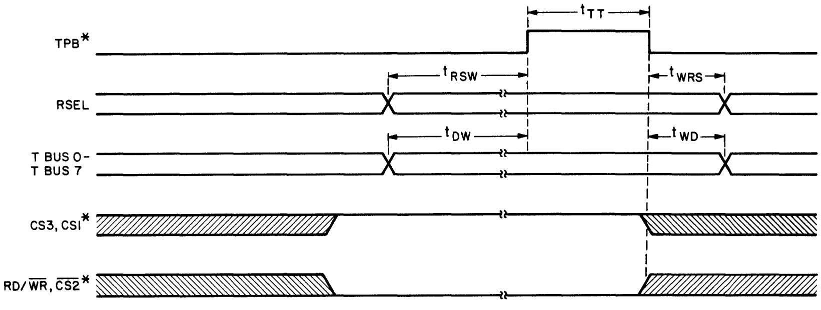
CHARACTERISTIC		V_{DD} (V)	LIMITS CDP1854A Typ.†	LIMITS CDP1854A Max.*	LIMITS CDP1854AC Typ.†	LIMITS CDP1854AC Max.*	UNITS
CPU Interface — WRITE Timing — Mode 1							
Minimum Pulse Width: TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	—	—	
Minimum Setup Time: RSEL to Write	t_{RSW}	5	50	75	50	75	ns
		10	25	40	—	—	
Data to Write	t_{DW}	5	-30	0	-30	0	ns
		10	-15	0	—	—	
Minimum Hold Time: RSEL after Write	t_{WRS}	5	50	75	50	75	ns
		10	25	40	—	—	
Data after Write	t_{WD}	5	75	125	75	125	ns
		10	40	60	—	—	

†Typical values are for T_A=25°C and nominal voltages.
*Maximum limits of minimum characteristics are the values above which all devices function.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ±5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=100 pF, see Fig. 6.

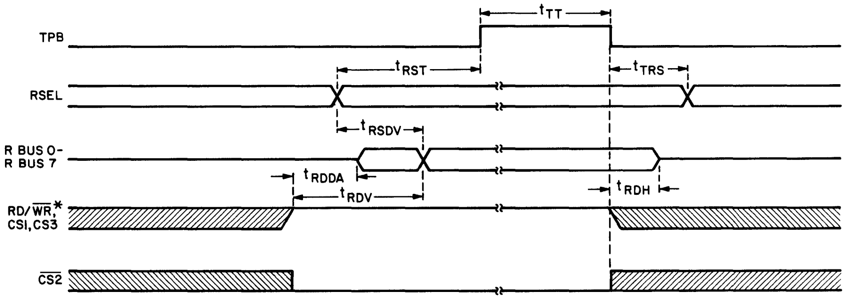
CHARACTERISTIC		V_{DD} (V)	LIMITS CDP1854A Min.	LIMITS CDP1854A Typ.†	LIMITS CDP1854A Max.*	LIMITS CDP1854AC Min.	LIMITS CDP1854AC Typ.†	LIMITS CDP1854AC Max.*	UNITS
CPU Interface — READ Timing — Mode 1									
Minimum Pulse Width: TPB	t_{TT}	5	—	100	150	—	100	150	ns
		10	—	50	75	—	—	—	
Minimum Setup Time: RSEL to TPB	t_{RST}	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Minimum Hold Time: RSEL after TPB	t_{TRS}	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Read to Data Access Time	t_{RDDA}	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
Read to Data Valid Time	t_{RDV}	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
RSEL to Data Valid Time	t_{RSDV}	5	—	150	225	—	150	225	ns
		10	—	75	125	—	—	—	
Hold Time: Data after Read	t_{RDH}	5	50	150	—	50	150	—	ns
		10	25	75	—	—	—	—	

†Typical values are for T_A=25°C and nominal voltages.
*Maximum limits of minimum characteristics are the values above which all devices function.



* WRITE IS THE OVERLAP OF TPB, CS1, CS3 = 1 AND $\overline{CS2}$, RD/$\overline{WR}$ = 0

Fig. 5 - Mode 1 CPU interface (WRITE) timing diagram.



* READ IS THE OVERLAP OF CS1, CS3, RD/$\overline{WR}$ = 1 AND $\overline{CS2}$ = 0

Fig. 6 - Mode 1 CPU interface (READ) timing diagram.

Mode Input Low (Mode = 0)

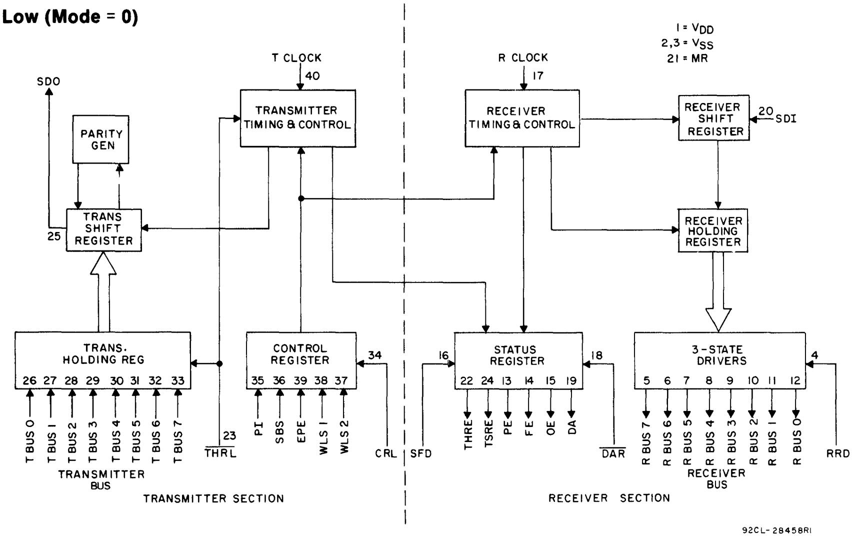


Fig. 7 - Mode 0 block diagram (industry standard compatible).

CDP1854A, CDP1854AC

Functional Definitions for CDP1854A Terminals
Standard Mode 0

SIGNAL: FUNCTION

V_{DD}:
Positive supply voltage.

MODE SELECT (MODE):
A low-level voltage at this input selects Standard Mode 0 Operation.

V_{SS}:
Ground.

RECEIVER REGISTER DISCONNECT (RRD):
A high-level voltage applied to this input disconnects the Receiver Holding Register from the Receiver Bus.

RECEIVER BUS (R BUS 7 - R BUS 0):
Receiver parallel data outputs.

PARITY ERROR (PE):
A high-level voltage at this output indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This output is updated each time a character is transferred to the Receiver Holding Register. PE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

FRAMING ERROR (FE):
A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

OVERRUN ERROR (OE):
A high-level voltage at this output indicates that the DATA AVAILABLE (DA) flag was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

STATUS FLAG DISCONNECT (SFD):
A high-level voltage applied to this input disables the 3-state output drivers for PE, FE, OE, DA, and THRE, allowing these status outputs to be bus connected.

RECEIVER CLOCK (RCLOCK):
Clock input with a frequency 16 times the desired receiver shift rate.

$\overline{\text{DATA AVAILABLE RESET}}$ ($\overline{\text{DAR}}$):
A low-level voltage applied to this input resets the DA flip-flop.

DATA AVAILABLE (DA):
A high-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):
Serial data received at this input enters the receiver shift register at a point determined by the character length. A high-level voltage must be present when data is not being received.

MASTER RESET (MR):
A high-level voltage at this input resets the Receiver Holding Register, Control Register, and Status Register, and sets the serial data output high.

TRANSMITTER HOLDING REGISTER EMPTY (THRE):
A high-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

$\overline{\text{TRANSMITTER HOLDING REGISTER LOAD}}$ ($\overline{\text{THRL}}$):
A low-level voltage applied to this input enters the character on the bus into the Transmitter Holding Register. Data is latched on the trailing edge of this signal.

TRANSMITTER SHIFT REGISTER EMPTY (TSRE):
A high-level voltage at this output indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains at this level until the start of transmission of the next character.

SERIAL DATA OUTPUT (SDO):
The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s)) are serially shifted out on this output. When no character is being transmitted, a high-level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):
Transmitter parallel data inputs.

CONTROL REGISTER LOAD (CRL):
A high-level voltage at this input loads the Control Register with the control bits (PI, EPE, SBS, WLS1, WLS2). This line may be strobed or hardwired to a high-level input voltage.

PARITY INHIBIT (PI):
A high-level voltage at this input inhibits the parity generation and verification circuits and will clamp the PE output low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission.

STOP BIT SELECT (SBS):
This input selects the number of stop bits to be transmitted after the parity bit. A high-level selects two stop bits, a low-level selects one stop bit. Selection of two stop bits with five data bits programmed selects 1.5 stop bits.

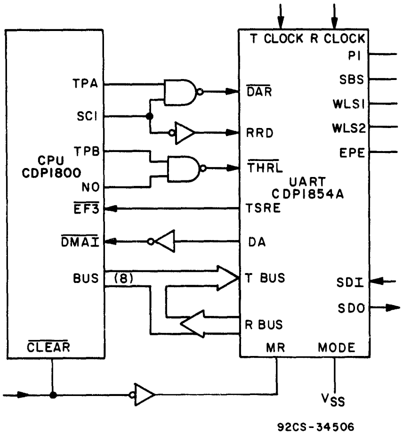


Fig. 8 - Mode 0 connection diagram.

WORD LENGTH SELECT 2 (WLS2):
WORD LENGTH SELECT 1 (WLS1):
These two inputs select the character length (exclusive of parity) as follows:

WLS2	WLS1	Word Length
Low	Low	5 Bits
Low	High	6 Bits
High	Low	7 Bits
High	High	8 Bits

EVEN PARITY ENABLE (EPE):
A high-level voltage at this input selects even parity to be generated by the transmitter and checked by the receiver. A low-level input selects odd parity.

TRANSMITTER CLOCK (TCLOCK):
Clock input with a frequency 16 times the desired transmitter shift rate.

Description of Standard Mode 0 Operation (Mode Input=V_{SS})

1. Initialization and Controls

The MASTER RESET (MR) input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting the SERIAL DATA OUTPUT (SDO) signal high. Timing is generated from the clock inputs, Transmitter Clock (TCLOCK) and Receiver Clock (RCLOCK), at a frequency equal to 16 times the serial data bit rate. When the receiver data input rate and the transmitter data output rate are the same, the TCLOCK and RCLOCK inputs may be connected together. The CONTROL REGISTER LOAD (CRL) input is pulsed to store the control inputs PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECT (SBS), and WORD LENGTH SELECTs (WLS1 and WLS2). These inputs may be hardwired to the proper voltage levels (V_{SS} or V_{DD}) instead of being dynamically set and CRL may be hardwired to V_{DD}. The CDP1854A is then ready for transmitter and/or receiver operation.

2. Transmitter Operation

For the transmitter timing diagram refer to Fig. 10. At the beginning of a typical transmitting sequence the Transmitter Holding Register is empty (THRE is HIGH). A character is transferred from the transmitter bus to the Transmitter holding Register by applying a low pulse to the $\overline{\text{TRANSMITTER HOLDING REGISTER LOAD (THRL)}}$ input causing THRE to go low. If the Transmitter Shift Register is empty (TSRE is HIGH) and the clock is low, on the next high-to-low transition of the clock the character is loaded into the Transmitter Shift Register preceded by a start bit. Serial data transmission begins 1/2 clock period later with a start bit and 5-8 data bits followed by the parity bit (if programmed) and stop bit(s). The THRE output signal goes high 1/2 clock period later on the high-to-low transition of the clock. When THRE goes high, another character can be loaded into the Transmitter Holding Register for transmission beginning with a start bit immediately following the last stop bit of the previous character. This process is repeated until all characters have been transmitted. When transmission is complete, THRE and Transmitter Shift Register Empty (TSRE) will both be high. The format of serial data is shown in Fig. 12. Duration of each serial output data bit is determined by the transmitter clock frequency (f_{CLOCK}) and will be 16/f CLOCK.

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After the detection of a high-to-low transition on the SDI line, a divide-by-16 counter is enabled and a valid start bit is verified by checking for a low-level input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed), and stop bit(s) are shifted into the Receiver Shift Register at clock pulse 7-1/2 in each bit time. If programmed, the parity bit is checked, and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output voltage level) are loaded into the unused most significant bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) signal is raised. One-half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) signals become valid for the character in the Receiver Holding Register. The DA signal is also raised at this time. The 3-state output drivers for DA, OE, PE and FE are enabled when STATUS FLAG DISCONNECT (SFD) is low. When RECEIVER REGISTER DISCONNECT (RRD) goes low, the receiver bus 3-state output drivers are enabled and data is available at the RECEIVER BUS (R BUS 0 - R BUS 7) outputs. Applying a negative pulse to the $\overline{\text{DATA AVAILABLE RESET (DAR)}}$ resets DA. The preceding sequence of operation is repeated for each serial character received. A receiver timing diagram is shown in Fig. 11.

CDP1854A, CDP1854AC

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ±5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=100 pF, see Fig. 9.

CHARACTERISTIC		V_{DD} (V)	LIMITS CDP1854A Typ.†	CDP1854A Max.*	CDP1854AC Typ.†	CDP1854AC Max.*	UNITS
Interface Timing — Mode 0							
Minimum Pulse Width: CRL	t_{CRL}	5	100	150	100	150	ns
		10	50	75	—	—	
Minimum Pulse Width: MR	t_{MR}	5	200	400	200	400	ns
		10	100	200	—	—	
Minimum Setup Time: Control Word to CRL	t_{CWC}	5	40	80	40	80	ns
		10	20	50	—	—	
Minimum Hold Time: Control Word after CRL	t_{CCW}	5	100	150	100	150	ns
		10	50	75	—	—	
Propagation Delay Time: SFD High to SOD	t_{SFDH}	5	200	300	200	300	ns
		10	100	150	—	—	
SFD Low to SOD	t_{SFDL}	5	75	120	75	120	ns
		10	40	60	—	—	
RRD High to Receiver Register High Impedance	t_{RRDH}	5	200	300	200	300	ns
		10	100	150	—	—	
RRD Low to Receiver Register Active	t_{RRDL}	5	100	150	100	150	ns
		10	50	75	—	—	

†Typical values are for T_A=25° C and nominal voltages.
*Maximum limits of minimum characteristics are the values above which all devices function.

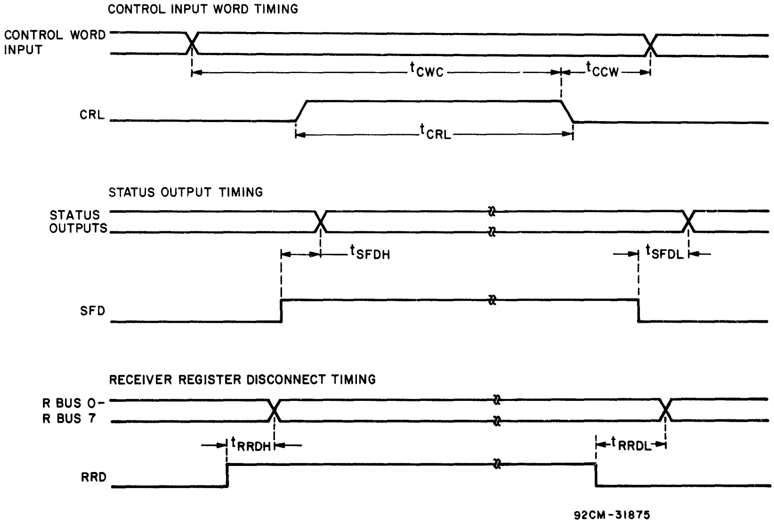


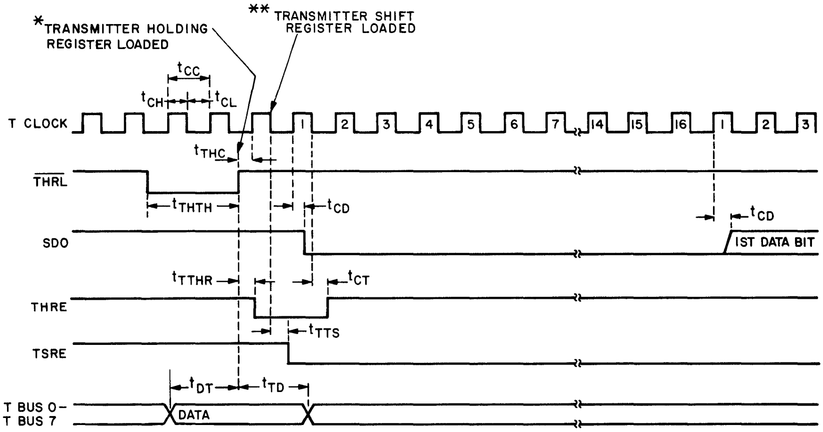
Fig. 9 - Mode 0 interface timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ±5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=100 pF, see Fig. 10.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			Typ.†	Max.*	Typ.†	Max.*	
Transmitter Timing — Mode 0							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	—	—	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	—	—	
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	—	—	
$\overline{\text{THRL}}$	t_{THTH}	5	100	150	100	150	ns
		10	50	75	—	—	
Minimum Setup Time: $\overline{\text{THRL}}$ to Clock	t_{THC}	5	175	275	175	275	ns
		10	90	150	—	—	
Data to $\overline{\text{THRL}}$	t_{DT}	5	20	50	20	50	ns
		10	0	40	—	—	
Minimum Hold Time: Data after $\overline{\text{THRL}}$	t_{TD}	5	80	120	80	120	ns
		10	40	60	—	—	
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	—	—	
Clock to THRE	t_{CT}	5	200	300	200	300	ns
		10	100	150	—	—	
$\overline{\text{THRL}}$ to THRE	t_{TTHR}	5	200	300	200	300	ns
		10	100	150	—	—	
Clock to TSRE	t_{TTS}	5	200	300	200	300	ns
		10	100	150	—	—	

†Typical values are for T_A=25°C and nominal voltages.

*Maximum limits of minimum characteristics are the values above which all devices function.



* THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF $\overline{\text{THRL}}$

** THE TRANSMITTER SHIFT REGISTER, IF EMPTY, IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD+t_{THC} AFTER THE TRAILING EDGE OF $\overline{\text{THRL}}$, AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER

92CM-31876R1

Fig. 10 - Mode 0 transmitter timing diagram.

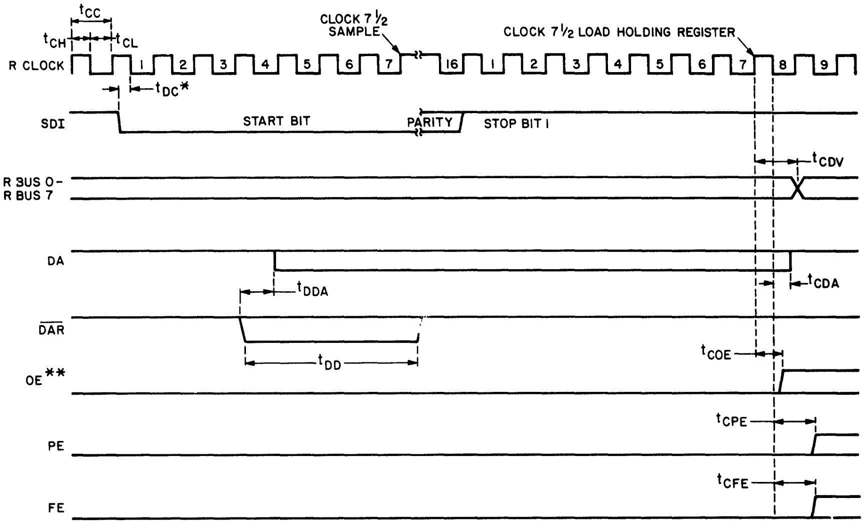
CDP1854A, CDP1854AC

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ±5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=100 pF, see Fig. 11.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			Typ.†	Max.*	Typ.†	Max.*	
Receiver Timing — Mode 0							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	—	—	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	—	—	
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	—	—	
$\overline{\text{DATA AVAILABLE RESET}}$	t_{DD}	5	50	75	50	75	ns
		10	25	40	—	—	
Minimum Setup Time: Data Start Bit to Clock	t_{DC}	5	100	150	100	150	ns
		10	50	75	—	—	
Propagation Delay Time: $\overline{\text{DATA AVAILABLE RESET}}$ to Data Available	t_{DDA}	5	150	225	150	225	ns
		10	75	125	—	—	
Clock to Data Valid	t_{CDV}	5	225	325	225	325	ns
		10	110	175	—	—	
Clock to Data Available	t_{CDA}	5	225	325	225	325	ns
		10	110	175	—	—	
Clock to Overrun Error	t_{COE}	5	210	300	210	300	ns
		10	100	150	—	—	
Clock to Parity Error	t_{CPE}	5	240	375	240	375	ns
		10	120	175	—	—	
Clock to Framing Error	t_{CFE}	5	200	300	200	300	ns
		10	100	150	—	—	

†Typical values are for T_A=25°C and nominal voltages.

*Maximum limits of minimum characteristics are the values above which all devices function.



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK

** IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE

92CM-31877

Fig. 11 - Mode 0 receiver timing diagram.

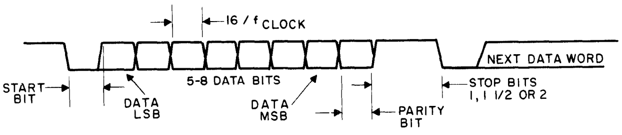


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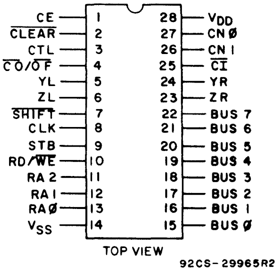
Fig. 12 - Serial data word format.

CDP1855, CDP1855C



TERMINAL ASSIGNMENT

8-Bit Programmable Multiply/Divide Unit

Features:

- *Cascadable up to 4 units for 32-bit by 32-bit multiply or 64 ÷ 32 bit divide*
- *8-bit by 8-bit multiply or 16 ÷ 18 bit divide in 5.6 μs at 5 V or 2.8 μs at 10 V*
- *Direct interface to CDP1800 series microprocessors*
- *Easy interface to other 8-bit microprocessors*
- *Significantly increases throughput of microprocessor used for arithmetic calculations*

The RCA-CDP1855 and CDP1855C are CMOS 8-bit multiply/divide units which can be used to greatly increase the capabilities of 8-bit microprocessors. They perform multiply and divide operations on unsigned, binary operators. In general, microprocessors do not contain multiple or divide instructions and even efficiently coded multiply or divide subroutines require considerable memory and execution time. These multiply/divide units directly interface to the CDP1800 series microprocessors via the N-lines and can easily be configured to fit in either the memory or I/O space of other 8-bit microprocessors.

The multiple/divide unit is based on a method of multiplying by add and shift right operations and dividing by subtract and shift left operations. The device is structured to permit cascading identical units to handle operands up to 32 bits.

The CDP1855 and CDP1855C are functionally identical. They differ in that the CDP1855 has a recommended operating voltage range of 4 - 10.5 volts, and the CDP1855C, a recommended operating voltage range of 4 - 6.5 volts.

The CDP1855 and CDP1855C types are supplied in a 28-lead hermetic dual-in-line ceramic package (D suffix) and in a 28-lead dual-in-line plastic package (E suffix). The CDP1855C is also available in chip form (H suffix).

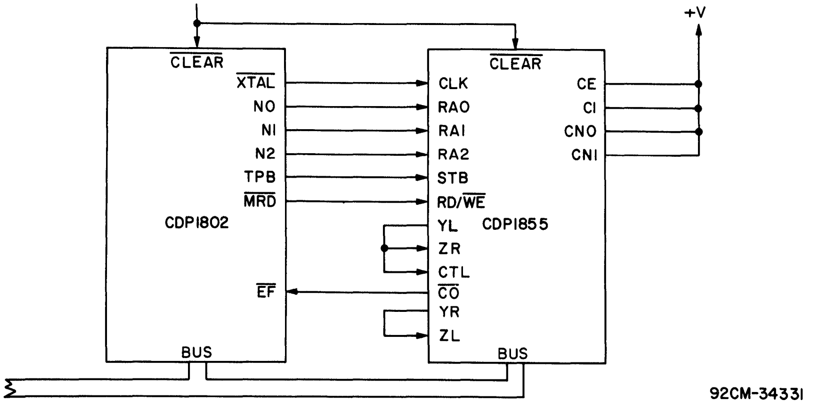


Fig. 1 - Circuit configuration for MDU addressed as an I/O device.

File Number **1053**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)

CDP1855	-0.5 to +11 V
CDP1855C	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Lineary at 12 mW/°C to 200 mW
For T_A = -55 to 100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D)	Derate Lineary at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ± 10%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1855			CDP1855C			
				Min.	Typ.•	Max.	Min.	Typ.•	Max.	
Quiescent Device Current I_{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	µA
	—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current I_{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source) Current I_{OH}	4.6	0, 5	5	-1.15	-2.3	—	-1.15	-2.3	—	
	9.5	0, 10	10	-2.6	-5.2	—	—	—	—	
Output Voltage Low-Level V_{OL}‡	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level V_{OH}‡	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	
	0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	
	0.5, 9.5	—	10	7	—	—	—	—	—	
Input Leakage Current I_{IN}	—	0, 5	5	—	—	±1	—	—	±1	µA
	—	0, 10	10	—	—	±1	—	—	—	
3-State Output Leakage Current I_{OUT}	0, 5	0, 5	5	—	—	±1	—	—	±1	
	0, 10	0, 10	10	—	—	±10	—	—	—	
Operating Current I_{DD1}#	—	0, 5	5	—	1.5	—	—	1.5	3	mA
	—	0, 10	10	—	6	12	—	—	—	
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	

•Typical values are for T_A = 25°C and nominal V_{DD}.

#Operating current is measured at 3.2 MHz with open outputs.

‡I_{OL} = I_{OH} = 1 µA.

CDP1855, CDP1855C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1855 Min.	LIMITS CDP1855 Max.	LIMITS CDP1855C Min.	LIMITS CDP1855C Max.	UNITS
DC Operating Voltage Range	—	4	10.5	4	6.5	V
Input Voltage Range	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	
Maximum Input Clock Frequency	5	3.2	—	3.2	—	MHz
	10	6.4	—	—	—	
Minimum 8 x 8 Multiply (16 ÷ 8 Divide) Time	5	—	5.6	—	5.6	µs
	10	—	2.8	—	—	

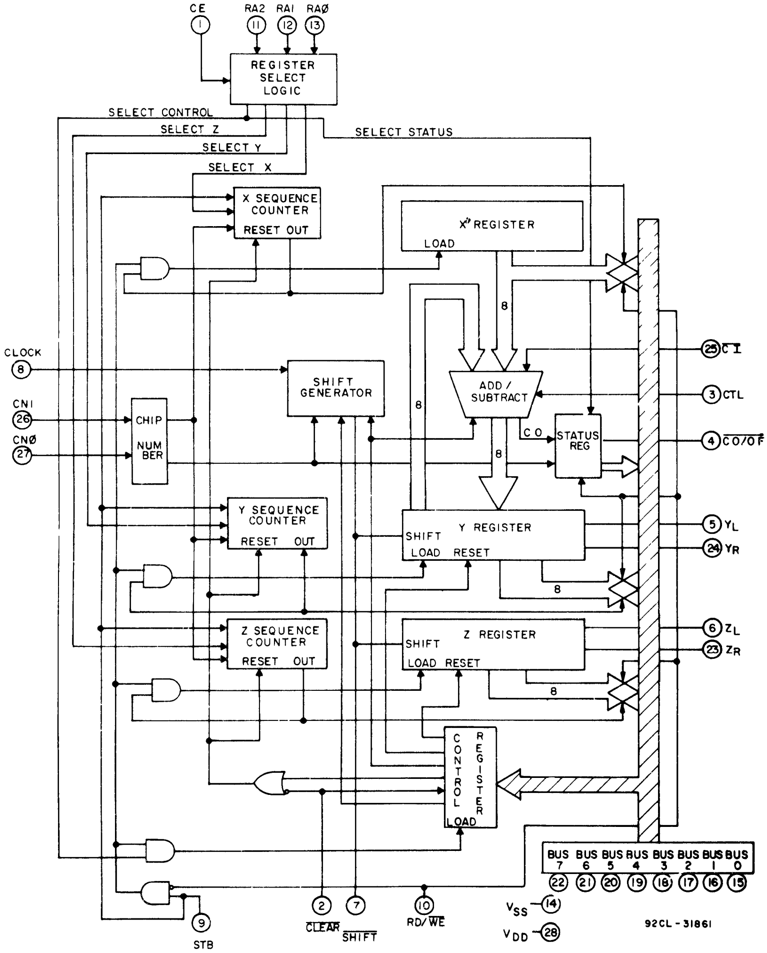


Fig. 2 - Block diagram of CDP1855 and CDP1855C.

FUNCTIONAL DESCRIPTION

The CDP1855 is a multiply-divide unit (MDU) designed to be compatible with CDP1800 series microprocessor systems. It can, in fact, be interfaced to most 8-bit microprocessors (see Fig. 5). The CDP1855 performs binary multiply or divide operations as directed by the microprocessor. It can do a 16N-bit by 8N-bit divide yielding an 8N-bit result plus and 8N-bit remainder. The multiply is an 8N-bit by 8N-bit operation with a 16N-bit result. The "N" represent the number of cascaded CDP1855's and can be 1, 2, 3 or 4. All operations require 8N + 1 shift pulses (See "DELAY NEEDED WITH AND WITHOUT PRESCALER" Pg. 7).

The CDP1855 contains three registers, X, Y, and Z, which are loaded with the operands prior to an operation and contain the results at the completion. In addition, the control register must be loaded to initiate a multiply or divide There is also a status register which contains an overflow flag as shown in the "CONTROL REGISTER BIT ASSIGNMENT TABLE" The register address lines (RAO-RA1) are used to select the appropriate register for loading or reading. The $RD/\overline{WE}$ and STB lines are used in conjunction with the RA lines to determine the exact MDU response (See "CONTROL TRUTH TABLE")

When multiple MDU's are cascaded, the loading of each register is done sequentially. For example, the first selection of register X for loading loads the most significant CDP1855, the second loads the next significant, and so on. Registers are also read out sequentially. This is accomplished by internal counters on each MDU which are decremented by STB during each register selection. When the counter matches the chip number (CN1, CN0 lines), the device is selected. These counters must be cleared with a clear on pin 2 or with bit 6 in the control word (See "CONTROL REGISTER BIT ASSIGNMENT TABLE") in order to start each sequence of accesses with the most significant device.

The CDP1855 has a built in clock prescaler which can be selected via bit 7 in the control register. The prescaler may be necessary in cascaded systems operating at high frequencies or in systems where a suitable clock frequency is not readily available. Without the prescaler select, the shift frequency is equal to the clock input frequency. With the prescaler selected, the rate depends on the number of MDU's as defined by bits 4 and 5 of the control word (See "CONTROL REGISTER BIT ASSIGNMENT TABLE").

1. For one MDU, the clock frequency is divided by 2.
2. For two MDU's the clock frequency is divided by 4.
3. For 3 or 4 MDU's, the clock frequency is divided by 8.

OPERATION

1. Initialization and Controls

The CDP1855 must be cleared by a low on pin 2 during power-on which prevents bus contention problems at the Y_L, Y_R and Z_L, Z_R terminals and also resets the sequence counters and the shift pulse generator.

Prior to loading any other registers the control register must be loaded to specify the number of MDU's being used (See "CONTROL REGISTER BIT ASSIGNMENT TABLE").

Once the number of devices has been specified and the sequence counters cleared with a clear pulse or bit 6 of the control word, the X, Y, and Z registers can be loaded as defined in the "CONTROL TRUTH TABLE". All bytes of the X register can be loaded, then all bytes of the Y, and then all bytes of the Z, or they can be loaded randomly. Succcessive loads to a given register will always proceed sequentially from the most significant byte to the least significant byte, as previously described Resetting the sequence counters select the most significant MDU. In a four MDU system, loading all MDU's results in the sequence counter pointing to the first MDU again In all other configurations (1, 2, or 3 MDU's), the sequence counter must be reset prior to each series of register reads or writes.

2. Divide Operation

For the divide operation, the divisor is loaded in the X register The dividend is loaded in the Y and Z registers with the more significant half in the Y register and the less significant half in the Z register. These registers may be loaded in any order, and after loading is completed, a control word is loaded to specify a divide operation and the number of MDU's and also to reset the sequence counters and Y or Z register and select the clock option if desired. Clearing the sequence counters with bit 6 will set the MDU's up for reading the results.

The X register will be unaltered by the operation. The quotient will be in the Z register while the remainder will be in the Y register. An overflow will be indicated by the $\overline{CO}/\overline{OF}$ of the most significant MDU and can also be determined by reading the status byte

While the CDP1855 is specified to perform 16 by 8-bit divides, if the quotient of a divide operation exceeds the size of the Z register(s) (8N-bits - where N is the number of cascaded CDP1855's) the overflow bit in the Status Register will be set. Neither the quotient in Z nor the remainder in Y will represent a valid answer This will always be the result of a division performed when the divisor (X) is equal to or less than the most significant 8N-bits of the dividend (Y)

The MDU can still be used for such computations if the divide is done in two steps The dividend is split into two parts—the more significant 8N-bits and the less significant 8N-bits—and a divide done on each part Each step yields an 8N-bit result for a total quotient of 16N-bits.

The first step consists of dividing the more significant 8N-bits by the divisor This is done by clearing the Y register(s), loading the Z register(s) with the more significant 8N-bits of the dividend, and loading the X register(s) with the divisor A division is performed and the resultant value in Z represents the more significant 8N-bits of the final quotient The Z register(s) value must be unloaded and saved by the processor

A second division is performed using the remainder from the first division (in Y) as the more significant 8N-bits of the dividend and the less significant half of the original dividend loaded into the Z register The divisor in X remains unaltered and is, by definition, larger than the remainder from the first division which is in Y The resulting value in Z becomes the less significant 8N-bits of the final quotient and the value in Y is, as usual, the remainder

Extending this technique to more steps allows division of any size number by an 8N-bit divisor

Note that division by zero is never permitted and must be tested for and handled in software

The following example illustrates the use of this algorithm

Example:
Assume three MDU's capable of a by 24-bit division The problem is to divide 00F273,491C06H by 0003B4H

Step 1	000000	,	00F273	/	0003B4	=	000041	R=0001BF
	Y		Z(MS)		X		Z1	Y1
Step 2	0001BF	,	491C06	/	0003B4	=	78C936	R=00000E
	Y1		Z(LS)		X		Z2	Y2
Result:	000041	,	78C936		R=00000E			
	Z1		Z2		Y2			

OPERATION (Cont'd)

The Z register can simply be reset using bit 2 of the control word and another divide can be done in order to further divide the remainder.

3. Multiply Operation

For a multiply operation the two numbers to be multiplied are loaded in the X and Z registers The result is in the Y and Z register with Y being the more significant half and Z the less significant half. The X register will be unchanged after the operation is completed

The original contents of the Y register are added to the product of X and Z Bit 3 of the control word will reset register Y to 0 if desired.

FUNCTIONAL DESCRIPTION OF CDP1855 TERMINALS

CE - CHIP ENABLE (Input):

A high on this pin enables the CDP1855 MDU to respond to the select lines. All cascaded MDU's must be enabled together. CE also controls the tristate C.O./O.F., output of the most significant MDU.

CLEAR (Input):

The CDP1855 MDU(s) must be cleared upon power-on with a low-on this pin. The clear signal resets the sequence counters, the shift pulse generator, and bits 0 and 1 of the control register.

CTL — CONTROL (Input):

This is an input pin. All CTL pins must be wired together and to the Y_L of the most significant CDP1855 MDU and to the Z_R of the least significant CDP1855 MDU. This signal is used to indicate whether the registers are to be operated on or only shifted.

C.O./O.F. — CARRY OUT/OVER FLOW (Output):

This is a tristate output pin. It is the CDP1855 Carry Out signal and is connected to CI (CARRY-IN) of the next more significant CDP1855 MDU, except for on the most significant MDU. On that MDU it is an overflow indicator and is enabled when chip enables is true. A low on this pin indicates that an overflow has occured. The overflow signal is latched each time the control register is loaded, but is only meaningful after a divide command.

Y_L, Y_R — Y-LEFT, Y-RIGHT:

These are tristate bi-directional pins for data transfer between the Y registers of cascaded CDP1855 MDU's. The Y_R pin is an output and Y_L is an input during a multiply and the reverse is true at all other times. The Y_L pin must be connected to the Y_R pin of the next more significant MDU. An exception is that the Y_L pin of the most significant CDP1855 MDU must be connected to the Z_R pin of the least significant MDU and to the CTL pins of all MDU's. Also the Y_R pin of the least significant MDU is tiexd to the Z_L pin of the most significant MDU.

Z_L, Z_R — Z-LEFT, Z-RIGHT:

These are tristate bi-directional pins for data transfers between the "Z" registers of cascaded MDU's. The Z_R pin is an output and Z_L is an input during a multiply and the reverse is true at all other times. The Z_L pin must be tied to the Y_R pin of the next more significant MDU. An exception is that the Z_L pin of the most significant MDU must be connected to the Y_R pin of the least significant MDU. Also, the Z_R pin of the least significant MDU is tied to the Y_L of the most significant MDU.

SHIFT — SHIFT CLOCK:

This is a tristate bi-directional pin. It is an output on the most significant MDU. And an input on all other MDU's. It provides the MDU system timing pulses. All SHIFT pins must be connected together for cascaded operation. A maximum of the 8N +1 shifts are required for an operation where "N" equals the number of MDU devices that are cascaded.

CLK — CLOCK (Input):

This pin should be grounded on all but the most significant MDU. There is an optional reduction of clock frequency available on this pin if so desired, controlled by bit 7 of the control byte.

STB — STROBE (Input):

When RD/WE is low data is latched from bus lines on the falling edge of this signal. It may be asynchronous to the clock. Strobe also increments the selected register's sequence counter during reads and writes. TPB would be used in CDP1800 systems.

RD/WE — READ/WRITE ENABLE (Input):

This signal defines whether the selected register is to be read from or written to. In 1800 systems use MRD if MDU's are addressed as I/O devices, MWR is used if MDU's are addressed as memory devices.

RA2, RA1, RA0 — REGISTER ADDRESS (Input):

These input signals define which register is to be read from or written to. It can be seen in the "CONTROL TRUTH TABLE" that RA2 can be used as a chip enable. It is identifical to the CE pin, except only CE controls the tristate C O./O.F on the most significant MDU. In 1800 systems use N lines if MDU's are used as I/O devices, use address lines or function of address lines if MDU's are used as memory devices.

BUS 0 — BUS 7 - BUS LINES:

Tristate bi-directional bus for direct interface with CDP1800 series and other 8-bit microprocessors.

Z_R — Z-RIGHT:

See Pin 6.

Y_R — Y-RIGHT:

See Pin 5.

CI — CARRY IN (Input):

This is an input for the carry from the next less significant MDU. On the least significant MDU it must be high (V_{DD}) on all others it must be connected to the CO pin of the next less significant MDU

CN1, CN0 — CHIP NUMBER (Input):

These two input pins are wired high or low to indicate the MDU position in the cascaded chain. Both are high for the most significant MDU regardless of how many CDP1855 MDU's are used. Then CN1 = high and CN0 = low for the next MDU and so forth.

V_{SS} — GROUND:

Power supply line.

V_{DD} — V+·

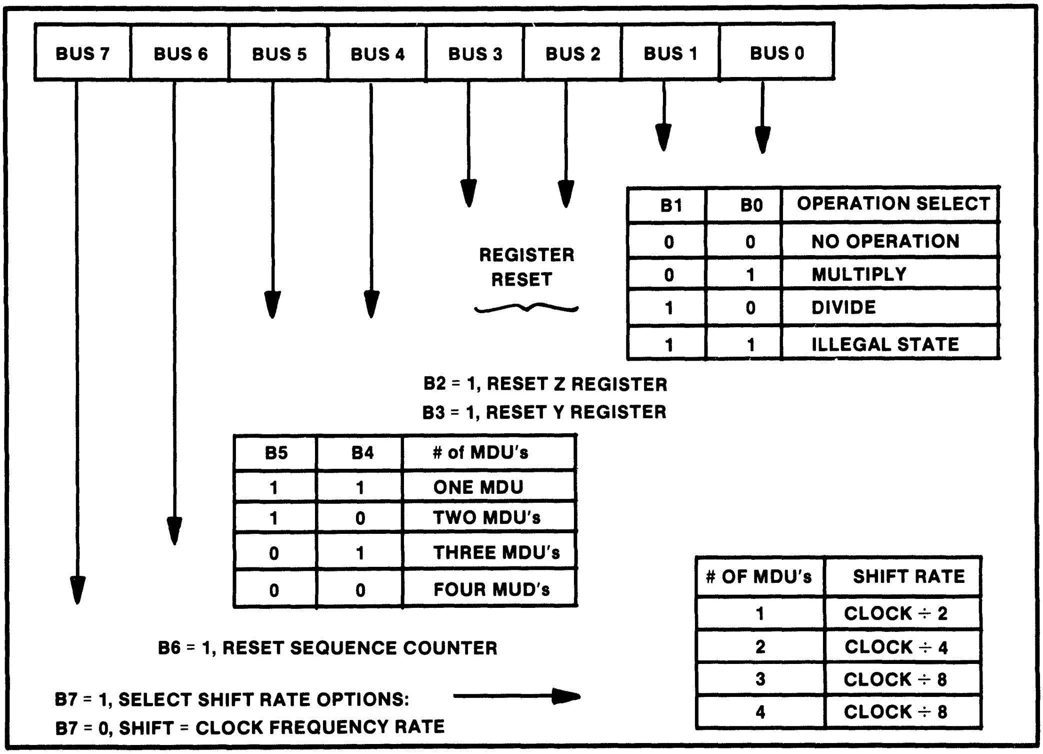
Power supply line.

CONTROL TRUTH TABLE

INPUTS*						
CE	RA2 (N2)	RA1 (N1)	RA0 (N0)	RD/$\overline{\text{WE}}$ (MRD)	STB (TPB)	RESPONSE
0	X	X	X	X	X	NO ACTION (BUS FLOATS)
X	0	X	X	X	X	NO ACTION (BUS FLOATS)
1	1	0	0	1	X	X TO BUS } INCREMENT SEQUENCE
1	1	0	1	1	X	Z TO BUS } COUNTER WHEN
1	1	1	0	1	X	Y TO BUS } STB AND RD = 1
1	1	1	1	1	X	STATUS TO BUS
1	1	0	0	0	1	LOAD X FROM BUS } INCREMENT
1	1	0	1	0	1	LOAD Z FROM BUS } SEQUENCE
1	1	1	0	0	1	LOAD Y FROM BUS } COUNTER
1	1	1	1	0	1	LOAD CONTROL REGISTER
1	1	X	X	0	0	NO ACTION (BUS FLOATS)

* ( ) = 1800 system signals. 1 = High Level, 0 = Low Level, X = High or Low Level.

CONTROL REGISTER BIT ASSIGNMENT TABLE



B1	B0	OPERATION SELECT
0	0	NO OPERATION
0	1	MULTIPLY
1	0	DIVIDE
1	1	ILLEGAL STATE

B2 = 1, RESET Z REGISTER

B3 = 1, RESET Y REGISTER

B5	B4	# of MDU's
1	1	ONE MDU
1	0	TWO MDU's
0	1	THREE MDU's
0	0	FOUR MUD's

B6 = 1, RESET SEQUENCE COUNTER

B7 = 1, SELECT SHIFT RATE OPTIONS: →

B7 = 0, SHIFT = CLOCK FREQUENCY RATE

# OF MDU's	SHIFT RATE
1	CLOCK ÷ 2
2	CLOCK ÷ 4
3	CLOCK ÷ 8
4	CLOCK ÷ 8

STATUS REGISTER

	Status Byte
Bit	7 6 5 4 3 2 1 0
Output	0 0 0 0 0 0 0 O.F.
	O.F. = 1 if overflow (only valid after a divide has been done)

NOTE: Bits 1 — 7 are read as 0 always

DELAY NEEDED WITH AND WITHOUT PRESCALER

8N+1 Shifts/Operation at 1 Clock Cycle/Shift
N = Number of MDU's **S = Shift Rate**

Number of MDU's	No Prescaler		With Prescaler		
	Shifts Needed = 8N+1	Machine Cycles Needed*	Shifts Needed = S (8N+1)	Machine Cycles Needed*	Shift Rate
1	9	2 (1 NOP)	18	3 (1 NOP)	2
2	17	2 (1 NOP)	68	9 (3 NOPs)	4
3	25	3 (1 NOP)	200	25 (9 NOPs)	8
4	33	4 (2 NOPs)	264	33 (11 NOPs)	8

*NOP instruction is shown for machine cycles needed (3/NOP). Other instructions may be used.

CDP1855 INTERFACING SCHEMES

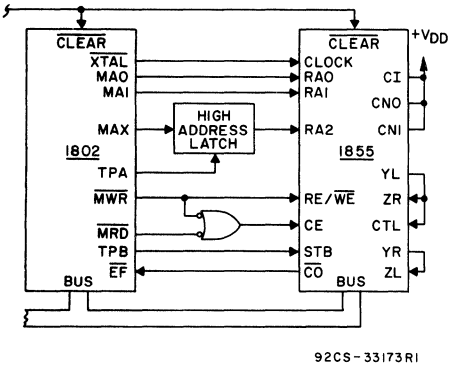


Fig. 3 - Required connection for memory mapped addressing of the MDU.

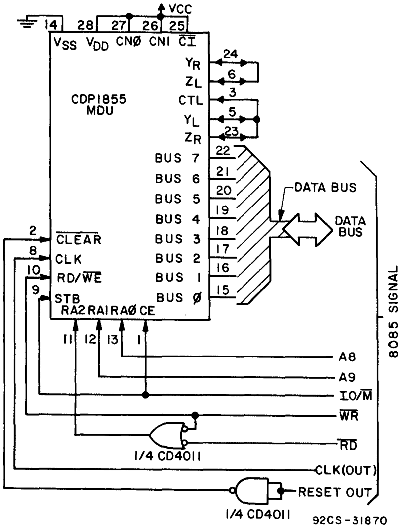


Fig. 4 - Interfacing the CDP1855 to an 8085 microprocessor as an I/O device.

PROGRAMMING EXAMPLE FOR MULTIPLICATION

For a 24-bit x 24-bit multiply using the system shown in Figure 5, the following is an assembly listing of a program to multiply $201F7C_{16}$ by $723C09_{16}$:

```
MEMORY      OP        LINE         ASSEMBLY
LOCATION    CODE      NO.          LANGUAGE
 0000       F830;     0001         LDI 030H
 0002       A2;       0002         PLO R2            ..LOAD 30 INTO R2.0
 0003       F800;     0003         LDI 00H
 0005       B2;       0004         PHI R2            ..LOAD 00 INTO R2.1 (R2=0030)
 0006       6758;     0005         OUT 7; DC 058H    ..LOAD CONTROL REGISTERS
 0008       ;         0006                           ..SPECIFYING THREE MDU'S,
 0008       ;         0007                           ..RESET THE Y REGISTER AND
 0008       ;         0008                           ..SEQUENCE COUNTER
 0008       6420;     0009         OUT 4; DC 020H    ..LOAD MSB OF X REGISTER
 000A       ;         0010                           ..WITH 20
 000A       641F;     0011         OUT 4; DC 01FH    ..LOAD NEXT MSB OF X REG
 000C       ;         0012                           ..WITH 1F
 000C       647C;     0013         OUT 4; DC 07CH    ..LOAD LSB OF X REGISTER
 000E       ;         0014                           ..WITH 7C
 000E       6572;     0015         OUT 5; DC 072H    ..LOAD MSB OF Z REGISTER
 0010       ;         0016                           ..WITH 72
 0010       653C;     0017         OUT 5; DC 03CH    ..LOAD NEXT MSB OF Z REG
 0012       ;         0018                           ..WITH 3C
 0012       6509;     0019         OUT 5; DC 09H     ..LOAD LSB OF Z REGISTER
 0014       ;         0020                           ..WITH 09
 0014       6759;     0021         OUT 7; DC 059H    ..LOAD CONTROL REGISTERS
 0016       ;         0022                           ..RESETTING Y REGISTERS
 0016       ;         0023                           ..AND SEQUENCE COUNTERS
 0016       ;         0024                           ..AND STARTING MULTIPLY
 0016       ;         0025                           ..OPERATION
                      DELAY FOR MULTIPLY TO FINISH
 0016       E2;       0026         SEX R2
 0017       6E60;     0027         INP 6; IRX        ..MSB OF RESULTS IS STORED
 0019       ;         0028                           ..AT LOCATION 0030
 0019       6E60;     0029         INP 6; IRX
 001B       6E60;     0030         INP 6; IRX
 001D       6D60;     0031         INP 5; IRX
 001F       6D60;     0032         INP 5; IRX
 0021       6D;       0033         INP 5             ..COMPLETE LOADING RESULT
 0022       ;         0034                           ..INTO MEMORY LOCATIONS
 0022       ;         0035                           ..0030 TO 0035
 0022       ;         0036                           ..RESULTS=0E558DBA2B5C
 0022       3022;     0037 STOP    BR STOP
 0024       ;         0038         END
 0000
```

The result of $201F7C_{16}$ x $723C09_{16}$ is 0E558DBA2B5C = 157606127972276_{10}. It will be stored in memory as follows:

LOC	BYTE
0030	0E
31	55
32	8D
33	BA
34	2B
35	5C

BEFORE MULTIPLY

	MDU1	MDU2	MDU3
Register X	20	1F	7C
Register Y	00	00	00
Register Z	72	3C	09

AFTER MULTIPLY

	MDU1	MDU2	MDU3
Register X	20	1F	7C
Register Y	0E	55	8D
Register Z	BA	2B	5C

PROGRAMMING EXAMPLE FOR DIVISION

```
MEMORY      OP          LINE     ASSEMBLY
LOCATION    CODE        NO.      LANGUAGE
0000        ;           0001     Program example for a 16 bit by 8 bit divide using 1 CDP1855 MDU
0000        ;           0002 . . Gives a 16 bit answer with 8 bit remainder
0000        ;           0003
0000        68C22000;   0004     RLDI R2,2000H           . . Answer is stored at 2000 hex
0004        ;           0005                             .   Register 2 points to it
0004        68C33000;   0006     RLDI R3,3000H           .   Dividend is stored at 3000 hex
0008        ,           0007                                 Register 3 points to it
0008        68C44000,   0008     RLDI R4,4000H           .   Divisor is stored at 4000 hex
000C        ;           0009                                 Register 4 points to it
000C        ;           0010
000C        E067F0;     0011     SEX R0, OUT 7; DC OF0H      Write to the control register to use
000F        ,           0012                                 clock / 2; 1 MDU; reset sequence
000F        ;           0013                             .   counter, and no operation
000F        ;           0014
000F        E464;       0015     SEX R4, OUT 4               Load the divisor into the X register
0011        ;           0016
0011        E06600;     0017     SEX R0; OUT 6; DC 0         Load 0 into the Y register
0014        E365;       0018     SEX R3, OUT 5               Load the most significant 8 bits of
0016        ;           0019                             .   the dividend into the Z register
0016        ,           0020
0016        E067F2;     0021     SEX R0; OUT 7, DC 0F2H  .   Do the first divide, also resets the
0019        ;           0022                             . . sequence counter
0019        ,           0023
0019        E26D60;     0024     SEX R2, INP 5; IRX      .   Read and store the most significant
001C        ,           0025                             .   8 bits of the answer at 2000 hex
001C        ,           0026
001C        E067F0;     0027     SEX R0; OUT 7, DC 0F0H  . . Reset the sequence counter
001F        ;           0028
001F        E365,       0029     SEX R3, OUT 5           . . Load the 8 least significant 8 bits
0021        ,           0030                                 of the original dividend into the Z
0021        ;           0031                             .   register
0021        ;           0032
0021        E067F2;     0033     SEX R0, OUT 7; DC 0F2H      Do the second division
0024        ;           0034
0024        E26D60,     0035     SEX R2, INP 5, IRX          Read and store the least significant
0027        ,           0036                             .   8 bits of the answer at 2001 hex
0027        6E,         0037     INP 6                       Read and store the remainder at 2002
0028        ,           0038                                 hex
0000
```

For the divide operation (Fig. 5), the formula is:

$$\frac{Y_3Y_2Y_1Z_3Z_2Z_1}{X_3X_2X_1} = Z_3Z_2Z_1 + \frac{Y_3Y_2Y_1}{X_3X_2X_1}$$

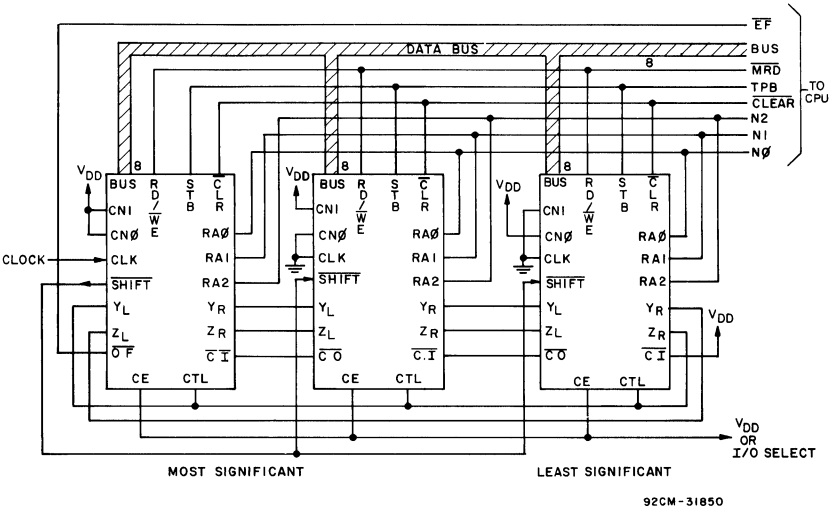


Fig. 5 - Cascading three MDU's (CDP1855) in an 1800 system with MDU's being accessed as I/O ports in programming example.

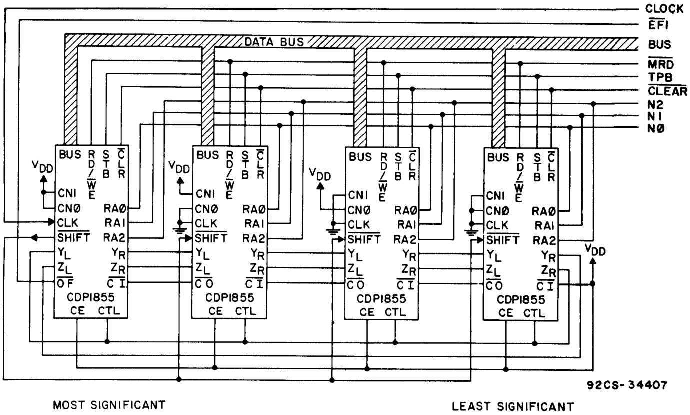


Fig. 6 - Cascading four MDU's (CDP1855).

CDP1855, CDP1855C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ±5% t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF (See Fig. 7)

CHARACTERISTIC•		V_{DD} (V)	LIMITS						UNITS
			CDP1855			CDP1855C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Operation Timing									
Maximum Clock Frequency+		5	3.2	4	—	3.2	4	—	MHz
		10	6.4	8	—	—	—	—	
Maximum Shift Frequency (1 Device)Δ		5	1.6	2	—	1.6	2	—	
		10	3.2	4	—	—	—	—	
Minimum Clock Width	t_{CLK0}	5	—	100	150	—	100	150	ns
	t_{CLK1}	10	—	50	75	—	—	—	
Minimum Clock Period	t_{CLK}	5	—	250	312	—	250	312	
		10	—	125	156	—	—	—	
Clock to Shift Prop. Delay	t_{CSH}	5	—	200	300	—	200	300	
		10	—	100	150	—	—	—	
Minimum C.I. to Shift Setup	t_{SU}	5	—	50	67	—	50	67	
		10	—	25	33	—	—	—	
C.O. from Shift Prop. Delay	t_{PLH}	5	—	450	600	—	450	600	
	t_{PHL}	10	—	225	300	—	—	—	
Minimum C.I. from Shift Hold	t_H	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Minimum Register Input Setup	t_{SU}	5	—	-20	10	—	-20	10	
		10	—	-10	10	—	—	—	
Register after Shift Delay	t_{PLH}	5	—	400	600	—	400	600	
	t_{PHL}	10	—	200	300	—	—	—	
Minimum Register after Shift Hold	t_H	5	—	50	100	—	50	100	
		10	—	25	50	—	—	—	
C.O. from C.I. Prop. Delay	t_{PLH}	5	—	100	150	—	100	150	
	t_{PHL}	10	—	50	75	—	—	—	
Register from C.I. Prop. Delay	t_{PLH}	5	—	80	120	—	80	120	
	t_{PHL}	10	—	40	60	—	—	—	

•Maximum limits of minimum characteristics are the values above which all devices function.

*Typical values are for T_A = 25° C and nominal voltages.

+Clock frequency and pulse width are given for systems using the internal clock option of the CDP1855. Clock frequency equals shift frequency for systems not using the internal clock option.

ΔShift period for cascading of devices is increased by an amount equal to the $\overline{\text{C.I.}}$ to $\overline{\text{C.O.}}$ Prop. Delay for each device added.

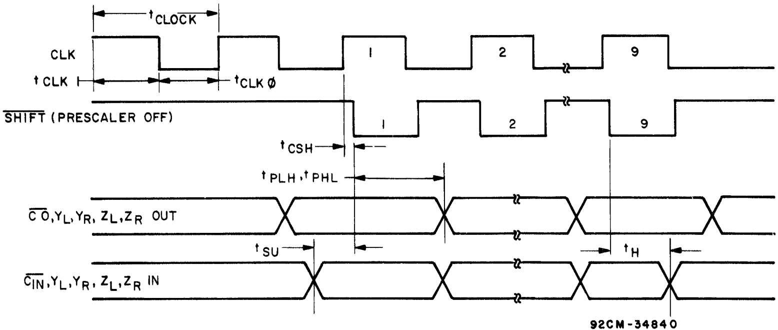

t_{CLOCK}
CLK
1
2
9
t_{CLK}
t_{CLK0}
$\overline{\text{SHIFT}}$ (PRESCALER OFF)
1
2
9
t_{CSH}
t_{PLH}, t_{PHL}
$\overline{\text{CO}}$, Y_L, Y_R, Z_L, Z_R OUT
t_{SU}
t_H
$\overline{\text{CIN}}$, Y_L, Y_R, Z_L, Z_R IN
92CM-34840

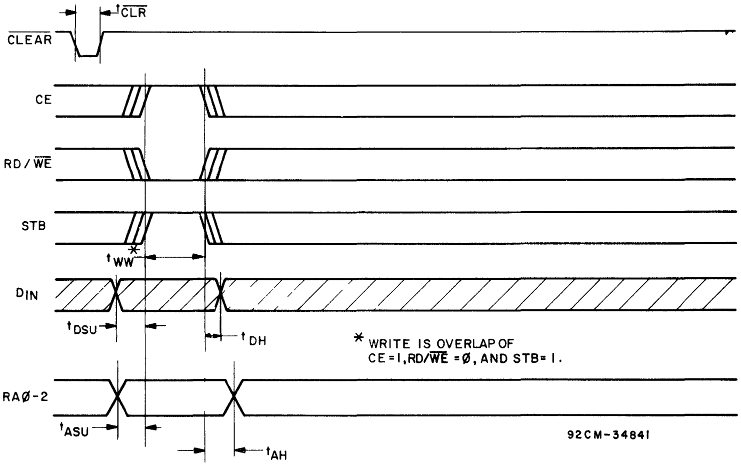
Fig. 7 - Operation timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ±5% t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF (See Fig. 8)

CHARACTERISTIC•		V_{DD} (V)	LIMITS						UNITS
			CDP1855			CDP1855C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Write Cycle									
Minimum Clear Pulse Width	$t_{\overline{CLR}}$	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Minimum Write Pulse Width	t_{WW}	5	—	150	225	—	150	225	
		10	—	75	115	—	—	—	
Minimum Data-In Setup	t_{DSU}	5	—	-75	0	—	-75	0	
		10	—	-40	0	—	—	—	
Minimum Data-In-Hold	t_{DH}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Minimum Address to Write Setup	t_{ASU}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Minimum Address after Write Hold	t_{AH}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	

•Maximum limits of minimum characteristics are the values above which all devices function.

*Typical values are for T_A = 25° C and nominal voltages.



* WRITE IS OVERLAP OF CE = 1, RD/$\overline{WE}$ = 0, AND STB = 1.

Fig. 8 - Write timing diagram.

CDP1855, CDP1855C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ±5% t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF (See Fig. 9)

CHARACTERISTIC•		V_{DD} (V)	LIMITS						UNITS
			CDP1855			CDP1855C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Read Cycle									
CE to Data Out Active	t_{CDO}	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
CE to Data Access	t_{CA}	5	—	300	450	—	300	450	
		10	—	150	225	—	—	—	
Address to Data Access	t_{AA}	5	—	300	450	—	300	450	
		10	—	150	225	—	—	—	
Data Out Hold after CE	t_{DOH}	5	50	150	225	50	150	225	
		10	25	75	115	—	—	—	
Data Out Hold after Read	t_{DOH}	5	50	150	225	50	150	225	
		10	25	75	115	—	—	—	
Read to Data Out Active	t_{RDO}	5	—	200	300	—	200	300	
		10	—	100	150	—	—	—	
Read to Data Access	t_{RA}	5	—	200	300	—	200	300	
		10	—	100	150	—	—	—	
Strobe to Data Access	t_{SA}	5	50	200	300	50	200	300	
		10	25	100	150	—	—	—	
Minimum Strobe Width	t_{SW}	5	—	150	225	—	150	225	
		10	—	75	115	—	—	—	

•Maximum limits of minimum characteristics are the values above which all devices function.

*Typical values are for T_A = 25° C and nominal voltages.

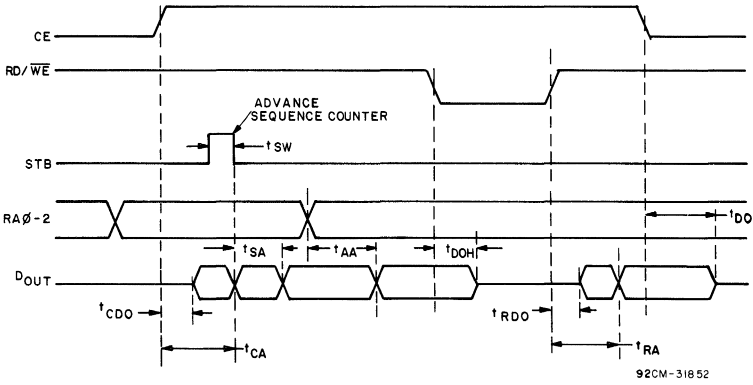
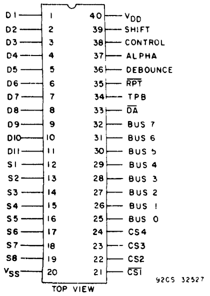


Fig. 9 - Read timing diagram.

CDP1871A, CDP1871AC



TERMINAL ASSIGNMENT

CMOS Keyboard Encoder

Features:

- *Directly interfaces with CDP1800-series microprocessors*
- *Low power dissipation*
- *3-state outputs*
- *Scans and generates code for 53 key ASCII keyboard plus 32 HEX keys (SPST mechanical contact switches)*
- *Shift, control, and alpha lock inputs*
- *RC-controlled debounce circuitry*
- *Single 4 to 10.5 V supply (CDP1871A); 4 to 6.5 V (CDP1871AC)*
- *N-key lockout*

The RCA-CDP1871A is a keyboard encoder designed to directly interface between a CDP1800-series microprocessor and a mechanical keyboard array, providing up to 53 ASCII coded keys and 32 HEX coded keys, as shown in the system diagram (Fig. 1).

The keyboard may consist of simple single-pole single-throw (SPST) mechanical switches. Inputs are provided for alpha-lock, control, and shift functions, allowing 160 unique codes. An external R-C input is available for user-selectable debounce times. The N-key lock-out feature prevents unwanted key codes if two or more keys are pressed simultaneously.

The CDP1871A and CDP1871AC are functionally identical. They differ in that the CDP1871A has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1871AC has a recommended operating voltage range of 4 to 6.5 volts. These types are supplied in 40-lead dual-in-line ceramic packages (D suffix), and 40-lead dual-in-line plastic packages (E suffix), and 44-lead plastic chip-carrier packages (Q suffix).

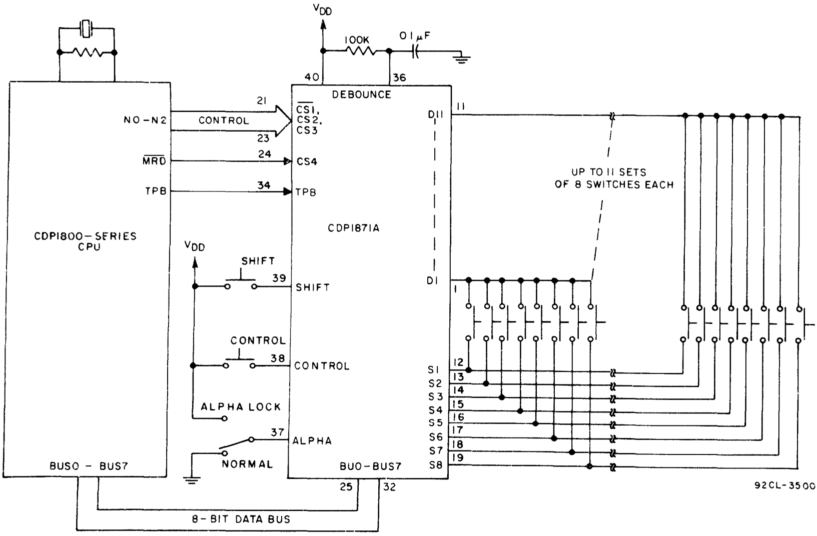


Fig. 1 - Typical CDP1800-series microprocessor system using the CDP1871A.

File Number **1374**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltage referenced to V_{SS} terminal)	
CDP1871A	-0.5 to +11 V
CDP1871AC	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -40 to +85°C (PACKAGE TYPE Q)*	500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E and Q	-40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

RECOMMENDED OPERATING CONDITIONS *at T_A = -40 to +85° C*

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1871AD CDP1871AE		CDP1871ACD CDP1871ACE		
			MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range			4	10.5	4	6.5	V
Recommended Input Voltage Range			V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Clock Input Frequency, TPB	f_{CL}	5	DC	0.4	DC	0.4	MHz
(Keyboard Capacitance = 200 pF)		10	DC	0.8	—	—	

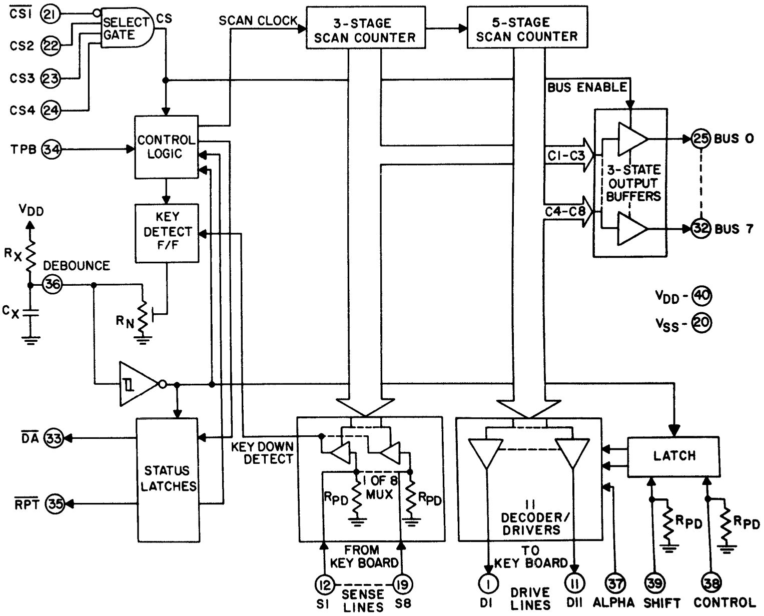


Fig 2 — CDP1871A block diagram.

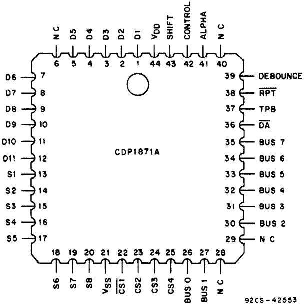
92CM-34522

STATIC ELECTRICAL CHARACTERISTIC at T_A = *−40 to +85° C, except as noted*

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	VIN (V)	V_{DD} (V)	CDP1871AD CDP1871AE			CDP1871ACD CDP1871ACE			
				MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Quiescent Device	—	0,5	5	—	0.1	50	—	1	200	μA
Current I_{DD}	—	0,10	10	—	1	200	—	—	—	
Output Low Drive (sink) Current	0.4	0,5	5	0.5	1	—	0.5	1	—	mA
(except debounce and D1-D11) I_{OL}	0.5	0,10	10	1	2	—	—	—	—	
	0.4	0,5	5	0.75	1 5	—	0 75	1.5	—	
Debounce I_{OL}	0.5	0,10	10	1	2	—	—	—	—	
	0.4	0,5	5	.05	0.1	—	.05	0.1	—	
D1-D11 I_{OL}	0.5	0,10	10	0.1	0.2	—	—	—	—	
Output High Drive (Source) Current	4.6	0,5	5	-0.3	-0.6	—	-0.3	-0.6	—	
I_{OH}	9.5	0,10	10	-0.75	-1.5	—	—	—	—	
Input Low Voltage	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
(except Debounce) V_{IL}	1,9	—	10	—	—	3	—	—	—	
Input High Voltage	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
(except Debounce) V_{IH}	1,9	—	10	7	—	—	—	—	—	
Debounce Schmitt Trigger										
Input Voltage	0.4	—	5	2.0	3.3	4.0	2.0	3.3	4.0	
Positive Trigger Voltage V_D	0.5	—	10	4.0	6.3	8.0	—	—	—	
	0.4	—	5	0.8	1.8	3.0	0.8	1.8	3.0	
Negative Trigger Voltage V_N	0.5	—	10	1.9	4.0	6.0	—	—	—	
	0.4	0,5	5	0.3	1.6	2.6	0.3	1.6	2.6	
Hysteresis V_H	0.5	0,10	10	0.7	2.3	4.7	—	—	—	
Output Voltage Low Level	—	0,5	5	—	0	.05	—	0	.05	
V_{OL}	—	0,10	10	—	0	.05	—	—	—	
Output Voltage High Level	—	0,5	5	4.95	5	—	4.95	5	—	
V_{OH}	—	0,10	10	9.95	10	—	—	—	—	
Input Leakage Current	—	0,5	5	- -	.01	1	—	.01	1	μA
(except S1-S8, Shift, Control) I_{IN}	—	0,10	10	—	.01	1	—	—	—	
3-State Output Leakage Current	0.5	0,5	5	—	.01	1	—	.02	2	
I_{OUT}	0,10	0,10	10	—	.02	2	—	—	—	
Pull-Down Resistor Value (S1-S8, Shift, Control) R_{PD}	—	—	—	7	14	24	7	14	24	kΩ
Operating Current I_{oper} (All-outputs f_{CL} = 0.4 MHz	0.5,4.5	0,5	5	—	0.6	—	—	0.6	—	mA
unloaded) f_{CL} = 0.8 MHz	1,9	0,10	10	—	2.7	—	—	—	—	

*Typical values are for T_A = +25° C. and nominal V_{DD}

TERMINAL ASSIGNMENT



44-Lead Plastic Chip-Carrier Package
(Q suffix)

FUNCTIONAL DESCRIPTION OF CDP1871A TERMINALS

D1 — D11 (Outputs):

Drive lines for the 11 x 8 keyboard switch matrix. These outputs are connected through the external switch matrix to the sense lines (S1 — S8).

S1 — S8 (Inputs):

Sense lines for the 11 x 8 keyboard maxtrix. These inputs have internal pull-down resistors and are driven high by appropriate drive line when a keyboard switch is closed.

$\overline{\text{CS1}}$, CS2, CS3, CS4 (Inputs):

Chip select inputs, which are used to enable the tri-state data bus outputs (BUS 0 — BUS 7) and to enable the resetting of the status flag ($\overline{\text{DA}}$), which occurs on the low-to-high transition of TPB. These four inputs are normally connected to the N-lines (N0-N2) and $\overline{\text{MRD}}$ output of the CDP1800-series microprocessor. (Table 2)

BUS 0 — BUS 7 (Outputs):

Tri-state data bus outputs which provide the ASII and HEX codes of the detected keys. The outputs are normally connected to the BUS 0 — BUS 7 terminals of the CDP1800-series microprocessor.

$\overline{\text{DA}}$ (Output):

The data available output flag which is set low when a valid key closure is detected. It is reset high by the low-to-high transition of TPB when data is read from the CDP1871A. This output is normally connected to a flag input ($\overline{\text{EF1}}$-$\overline{\text{EF4}}$) of the CDP1800-series microprocessor.

TPB (Input):

The input clock used to drive the scan generator and reset the status flag ($\overline{\text{DA}}$). This input is normally connected to the TPB output of the CDP1800-series microprocessor.

$\overline{\text{RPT}}$ (Output):

The repeat output flag which is used to indicate that a key is still closed after data has been read from the CDP1871A ($\overline{\text{DA}}$ = high). It remains low as long as the key is closed and is used for an autorepeat function, under CPU control. This output is normally connected to a flag input ($\overline{\text{EF1}}$-$\overline{\text{EF4}}$) of the CDP1800-series microprocessor.

DEBOUNCE(Input):

This input is connected to the junction of an external resistor to V_{DD} and capacitor to V_{SS}. It provides a debounce time delay ($t \cong RC$) after the release of a key. If a debounce is not desired, the external pull-up resistor is still required.

ALPHA, SHIFT, CONTROL (Inputs):

A high on the SHIFT or CONTROL inputs will be internally latched (after the debounce time) and the drive and sense line decoding will be modified as shown in Table 3. They are normally connected to the keyboard, but produce no code by themselves. The SHIFT and CONTROL inputs have internal pull-down resistors to simplify use with momentary contact switches. The ALPHA input is not latched and is designed for a standard SPDT switch to provide an alpha-lock function. When ALPHA = 1 the drive and sense line decoding will be modified as shown in Table 3.

V_{DD}, V_{SS}:

V_{DD} is the positive supply voltage input. V_{SS} is the most negative supply voltage terminal and is normal connected to ground. All outputs swing from V_{SS} to V_{DD}. The recommended input voltage swing is from V_{SS} to V_{DD}.

TABLE 1 — SWITCH INPUT FUNCTIONS

CONTROL	SHIFT	ALPHA	KEY FUNCTION
0	0	0	NORMAL
1	X	X	CONTROL
0	1	X	SHIFT
0	0	1	ALPHA

X = DON'T CARE

TABLE 2 — VALID N-LINE CONNECTIONS

CPU	CDP1871A SIGNAL				CPU INPUT INSTRUCTION
	CS4	CS3	CS2	$\overline{\text{CS1}}$	
CDP1800- SERIES SIGNAL	$\overline{\text{MRD}}$	N2	N0	N1	INP5
	$\overline{\text{MRD}}$	N0	N1	N2	INP3
	$\overline{\text{MRD}}$	N2	N1	N0	INP6

TABLE 3 — DRIVE AND SENSE LINE KEYBOARD CONNECTIONS‡

SENSE LINES	DRIVE LINES																
	D$_1$		D$_2$		D$_3$		D$_4$		D$_5$		D$_6$		D$_7$	D$_8$†	D$_9$†	D$_{10}$†	D$_{11}$†
S$_1$	SP	0	(	8		@	H	H	P	P	X	X	SPACE	80_{16}	88_{16}	90_{16}	98_{16}
	0	⬚	8	⬚	@	NUL	h	BS	p	DLE	x	CAN					
S$_2$	!	1	)	9	A	A	I	I	Q	Q	Y	Y	⬚	81_{16}	89_{16}	91_{16}	99_{16}
	1	⬚	9	⬚	a	SOH	i	HT	q	DC1	y	EM					
S$_3$	"	2	*	:	B	B	J	J	R	R	Z	Z	LINE FEED	82_{16}	$8A_{16}$	92_{16}	$9A_{16}$
	2	⬚	:	⬚	b	STX	j	LF	r	DC2	z	SUB					
S$_4$	#	3	+	;	C	C	K	K	S	S	{	[	ESCAPE	83_{16}	$8B_{16}$	93_{16}	$9B_{16}$
	3	⬚	;	⬚	c	ETX	k	VT	s	DC3	[	ESC					
S$_5$	$	4	<	,	D	D	L	L	T	T	¦	\	⬚	84_{16}	$8C_{16}$	94_{16}	$9C_{16}$
	4	⬚	,	⬚	d	EOT	l	FF	t	DC4	\	FS					
S$_6$	%	5	=	-	E	E	M	M	U	U	}	]	CARRAIGE RETURN	85_{16}	$8D_{16}$	95_{16}	$9D_{16}$
	5	⬚	-	⬚	e	ENQ	m	CR	u	NAK	]	GS					
S$_7$	&	6	>	.	F	F	N	N	V	V	~	↑	⬚	86_{16}	$8E_{16}$	96_{16}	$9E_{16}$
	6	⬚	.	⬚	f	ACK	n	SO	v	SYN	↑	RS					
S$_8$	'	7	?	/	G	G	O	O	W	W	DEL	—	DELETE	87_{16}	$8F_{16}$	97_{16}	$9F_{16}$
	7	⬚	/	⬚	g	BEL	o	SI	w	ETB	—	US					

KEY.

SHIFT*	ALPHA*
NORMAL	CONTROL*

*CONTROL overrides SHIFT and ALPHA ⬚ = NO RESPONSE

‡Showing ASCII outputs for all combinations with and without SHIFT, ALPHA LOCK and CONTROL
†Drive lines 8, 9, 10, and 11 generate non-ASCII hex values which can be used for special codes

TABLE 4 — HEXIDECIMAL VALUES OF ASCII CHARACTERS

						MSD							
					b7 →	0	0	0	0	1	1	1	1
					b6 →	0	0	1	1	0	0	1	1
	BITS				b5 →	0	1	0	1	0	1	0	1
	b4	b3	b2	b1	HEX ↓→	0	1	2	3	4	5	6	7
LSD	0	0	0	0	0	NUL	DLE	SP	0	@	P	\	p
	0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
	0	0	1	0	2	STX	DC2	"	2	B	R	b	r
	0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
	0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
	0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
	0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
	0	1	1	1	7	BEL	ETB	/	7	G	W	g	w
	1	0	0	0	8	BS	CAN	(	8	H	X	h	x
	1	0	0	1	9	HT	EM	)	9	I	Y	i	y
	1	0	1	0	A	LF	SUB	*	.	J	Z	j	z
	1	0	1	1	B	VT	ESC	+	;	K	[	k	{
	1	1	0	0	C	FF	FS	,	<	L	\	l	¦
	1	1	0	1	D	CR	GS	-	=	M	]	m	}
	1	1	1	0	E	SO	RS	.	>	N	↑	n	~
	1	1	1	1	F	SI	US	/	?	O	—	o	DEL

OPERATION

The CDP1871A is made up of two major sections: the counter/scan-selection logic and the control logic (Fig. 2). The counter and scan-selection logic scans the keyboard array using the drive lines (D1-D11) and the sense lines (S1-S8). The outputs of the internal 5-stage scancounter are conditionally encoded by the ALPHA, SHIFT, and CONTROL inputs (Table 1, Table 3) and are used to drive the D1-D11 output lines high one at a time. Each D1-D11 output may drive up to eight keys, which are sampled by the sense line inputs (S1-S8). The S1-S8 inputs are enabled by the internal 3-stage scancounter.

The control logic interfaces with the CDP1800-series I/O and timing signals to establish timing and status conditions for the CDP1871A.

The TPB input clocks the scancounters and is also used to reset the Data Available output ($\overline{\text{DA}}$). When a valid keydown condition is detected on a sense line, the control logic inhibits the clock to the scancounters on the next low-to-high transition of TPB and the $\overline{\text{DA}}$ output is set low. The scancounter outputs (C1-C8) represent the ASCII and HEX key codes and are used to drive the BUS 0 — BUS 7 outputs, which interface directly to the CDP1800-Series data bus. The BUS 0 — BUS 7 outputs, which are normally tri-stated, are enabled by decoding the CS inputs during a CPU input instruction (Table 2). The low-to-high transition of TPB during the input instruction resets the $\overline{\text{DA}}$ output high. Once the $\overline{\text{DA}}$ output has been reset, it cannot go low again until the present key is released and a new keydown condition is detected. (This prevents unwanted repeated keycode outputs which may be caused by fast software routines).

After the depressed key is released and the debounce delay (determined by RX, CX) has occurred, the scan clock inhibit is removed, allowing the scancounters to advance on the following high-to-low transitions of TPB. This provides an N-key lockout feature, which prevents the entry of erroneous codes when two or more keys are pressed simultaneously. The first key pressed in the scanning order is recognized, while all other keys pressed are ignored until the first key is released and read by the CPU, at which time the next key pressed in the scanning order is detected. If the first key remains closed after the CPU reads the data and resets the $\overline{\text{DA}}$ output, on the low-to-high transition of TPB, an auxiliary signal ($\overline{\text{RPT}}$) is generated and is available to the CPU to indicate an auto-repeat condition. The $\overline{\text{RPT}}$ output is reset high at the end of the debounce delay after the depressed key is released.

The DEBOUNCE input provides a terminal connection for an external user-selected RC circuit to eliminate false detection of a keydown condition caused by keyboard noise. The operation of the DEBOUNCE circuit is shown in Fig. 2 (Pin 36). When a valid keydown is detected, the on-chip active-resistor device (R_N) is enabled and the external capacitor (C_X) is discharged, providing a key closure debounce time $\cong R_N C_X$. This discharge is sensed by the Schmitt-tigger inverter, which clocks the $\overline{\text{DA}}$ flip-flop (latching the $\overline{\text{DA}}$ output low and inhibiting the scan clock). (The $\overline{\text{DA}}$ F/F is reset by the low-to-high transition of TPB when the CS inputs are enabled). When a valid key-release is detected R_N is disabled and C_X begins to charge through the external resistor (R_X), providing a key-release debounce time $\cong R_X C_X$. This charge time is again sensed by the Schmitt-trigger inverter, enabling the scan clock to continue on the next high-to-low transitions of TPB, after the current keycode data is read by the CPU.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A -40 to +85° C, V_{DD} ±5%*

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1871AD CDP1871AE			CDP1871ACD CDP1871ACE			
		MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Clock Cycle Time t_{CC}	5	—	—	—	—	—	—	NOTE 1
	10	—	—	—	—	—	—	
Clock Pulse Width High t_{CWH}	5	100	40	—	100	40	—	ns
	10	50	20	—	—	—	—	
Data Available Valid Delay t_{DAL}	5	—	260	500	—	260	500	ns
	10	—	130	250	—	—	—	
Data Available Invalid Delay t_{DAH}	5	—	70	150	—	70	150	ns
	10	—	35	75	—	—	—	
Scan Count Delay (Non-Repeat) t_{CD1}	5	—	850	1900	—	850	1900	ns
	10	—	425	950	—	—	—	
Data Out Valid Delay t_{CDV}	5	—	120	250	—	120	250	ns
	10	—	60	125	—	—	—	
Data Out Hold Time t_{CDH}	5	—	100	200	—	100	200	ns
	10	—	50	100	—	—	—	
Repeat Valid Delay t_{RPL}	5	—	150	400	—	150	400	ns
	10	—	75	200	—	—	—	
Repeat Invalid Delay t_{RPH}	5	—	350	700	—	350	700	ns
	10	—	170	350	—	—	—	

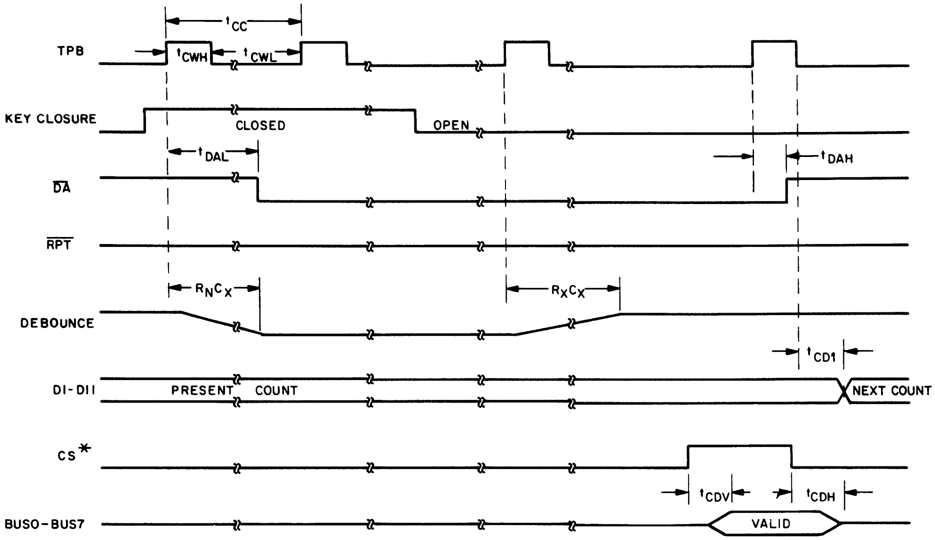
*Typical Values are for $T_A = +25°C$ and nominal V_{DD}

Note 1: $t_{cc} = t_{CWH} + t_{CWL}$

$t_{CWL} = t_{CD1} + KC$

k = 0.9 ns per pF

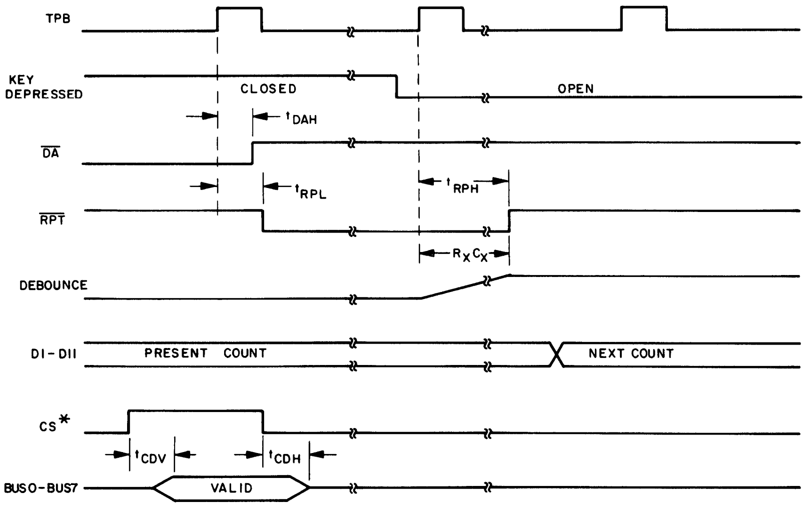
c = keyboard capacitance (pF)



* CS = $\overline{\text{CS1}}$ • CS2 • CS3 • CS4
$\overline{\text{CS1}}$, CS2, CS3 = CPU N-LINES
CS4 ($\overline{\text{MRD}}$) IS HIGH FOR CPU INPUT INSTRUCTION

92CM-35006

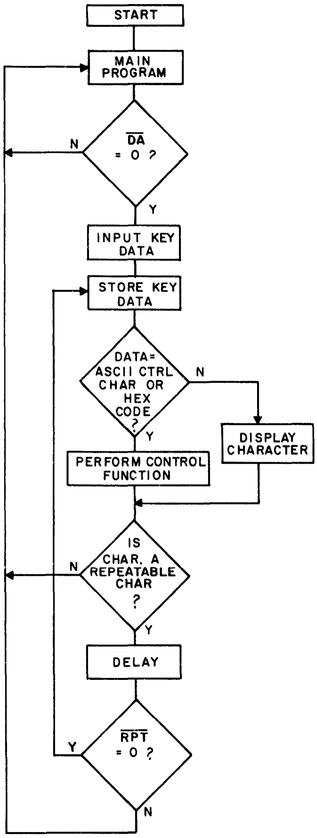
Fig 3 — CDP1871A dynamic timing diagram (non-repeat)



* CS = $\overline{\text{CS1}}$ • CS2 • CS3 • CS4
CS = $\overline{\text{CS1}}$, CS2, CS3 = (CPU N-LINES)
CS4 ($\overline{\text{MRD}}$) IS HIGH FOR CPU INPUT INSTRUCTION

92CM-35007

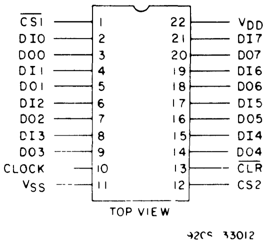
Fig 4 — CDP1871A dynamic timing diagram (repeat).



92CM-32530R1

Fig. 5 — Typical system software flowchart for CDP1871A, CDP1871AC

CDP1872C, CDP1874C, CDP1875C



CDP1872C Input Port
TERMINAL ASSIGNMENT

High-Speed 8-Bit Input and Output Ports

Features:

- *Parallel 8-bit input/output register with buffered outputs*
- *High-speed data-in to data-out:*
  85 ns (max.) at V_{DD} = 5 V
- *Flexible applications in microprocessor systems as buffers and latches*
- *High order address-latch capability in CDP1800 series microprocessor systems*
- *Output sink current = 5 mA (min.) at V_{DD} = 5 V*
- *3-state output - CDP1872C and CDP1874C*

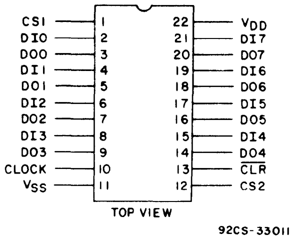
The RCA-CDP1872C, CDP1874C and CDP1875C devices are high-speed 8-bit parallel input and output ports designed for use in the CDP1800 microprocessor system and for general use in other microprocessor systems. The CDP1872C and CDP1874C are 8-bit input ports; the CDP1875C is an 8-bit output port.

These devices have flexible capabilities as buffers and data latches and are reset by $\overline{\text{CLR}}$ input when the data strobe is not active.

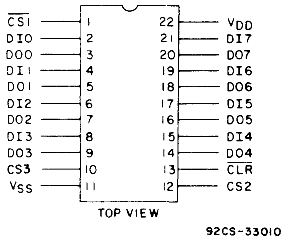
The CDP1872C and CDP1874C are functionally identical except for device selects. The CDP1872C has one active low and one active high select; the CDP1874C has two active high device selects. These devices also feature 3-state outputs when deselected. Data is strobed into the register on the leading edge of the CLOCK and latched on the trailing edge of the CLOCK.

The CDP1875C is an output port with data latched into the registers when the device selects are active. There are two active high and one active low selects. The output buffers are enabled at all times.

These devices are supplied in 22-lead hermetic, dual-in-line side-brazed ceramic packages (D suffix) and in 22-lead dual-in-line plastic package (E suffix).



CDP1874C Input Port
TERMINAL ASSIGNMENT



CDP1875C Output Port
TERMINAL ASSIGNMENT

CDP1872C, CDP1874C, CDP1875C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) .... -0.5 to +7 V
(Voltage referenced to V_{SS} Terminal)
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D).
For T_A = -40°C to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60°C to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55°C to +100°C (PACKAGE TYPE D) .... 500 mW
For T_A = +100°C to +125°C (PACKAGE TYPE D) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A - FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPE D .... -55°C to +125°C
PACKAGE TYPE E .... -40°C to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = -40°C to +85°C.
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS ALL TYPES	UNITS
DC Operating-Voltage Range	4 to 6.5	V
Input Voltage Range	V_{SS} to V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40°C to +85°C, V_{DD} ± 5%, except as noted

CHARACTERISTIC		TEST CONDITIONS			LIMITS ALL TYPES			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN.	TYP. •	MAX.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	25	50	μA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	5	10	—	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-4	-7	—	
Output Voltage Low-Level *	V_{OL}	—	0, 5	5	—	0	0.1	V
Output Voltage High-Level *	V_{OH}	—	0, 5	5	4.9	5	—	
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	—	1.5	
Input High Voltage	V_{IH}	0.5,4.5	—	5	3.5	—	—	
Input Leakage Current	I_{IN}	—	0, 5	5	—	—	±1	μA
3-State Output Leakage Current #	I_{OUT}	0, 5	0, 5	5	—	—	±5	
Input Capacitance	C_{IN}	—	—	—	—	15	—	pF
Output Capacitance #	C_{OUT}	—	—	—	—	15	—	

• Typical values are for T_A = 25°C and V_{DD} ±5%.
* I_{OL} = I_{OH} = 1 μA.
# For CDP1872C and CDP1874C only.

CDP1872C, CDP1874C, CDP1875C

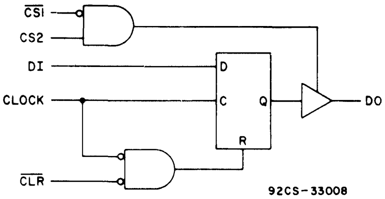


Fig. 1 - Equivalent logic diagram (1 of 8 latches shown) for CDP1872C.

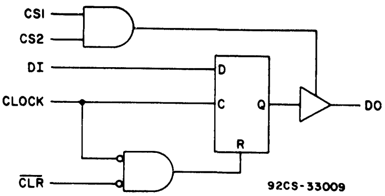


Fig. 2 - Equivalent logic diagram (1 of 8 latches shown) for CDP1874C.

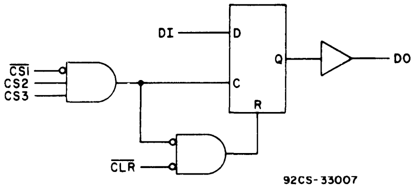


Fig. 3 - Equivalent logic diagram (1 of 8 latches shown) for CDP1875C.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V, t_r, t_f = 10 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 150 pF

CHARACTERISTIC		LIMITS		UNITS
		CDP1872C CDP1874C		
		TYP. •	MAX. †	
Input Port (Fig. 4)				
Output Enable	t_{EN}	45	90	ns
Output Disable	t_{DIS}	45	90	
Clock to Data Out	t_{CLO}	45	90	
$\overline{\text{Clear}}$ to Output	t_{CRO}	80	160	
Data In to Data Out	t_{DIO}	50	85	
Minimum Data Setup Time	t_{DSU}	10	30	
Data Hold Time	t_{DH}	10	30	
Minimum Clock Pulse Width	t_{CL}	30	60	
Minimum $\overline{\text{Clear}}$ Pulse Width	t_{CR}	30	60	

• Typical values are for T_A = 25°C and V_{DD} ±5%.

† Maximum values are for T_A = 85°C and V_{DD} ±5%.

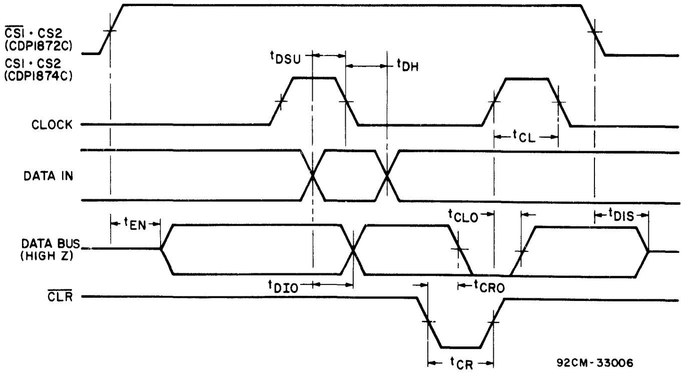


Fig. 4 - Timing waveforms for CDP1872C and CDP1874C (input-port types).

CDP1872C, CDP1874C, CDP1875C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25° C, V_{DD} = 5 V, t_r, t_f = 10 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 150 pF

CHARACTERISTIC		LIMITS		UNITS
		CDP1875C		
		TYP. •	MAX. †	
Output Port (Fig. 5)				
Clock to Data Out	t_{CLO}	50	100	ns
$\overline{\text{Clear}}$ to Output	t_{CRO}	80	160	
Data In to Data Out	t_{DIO}	50	85	
Minimum Data Setup Time	t_{DS}	10	30	
Data Hold Time	t_{DH}	10	30	
Minimum $\overline{\text{Clear}}$ Pulse Width	t_{CR}	30	60	

• Typical values are for T_A = 25° C and V_{DD} ±5%.
† Maximum values are for T_A = 85° C and V_{DD} ±5%.

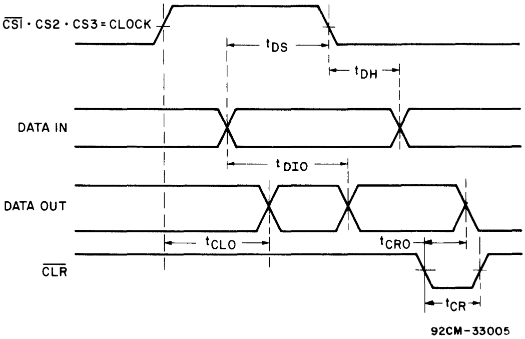


Fig. 5 - Timing waveforms for CDP1875C (output port).

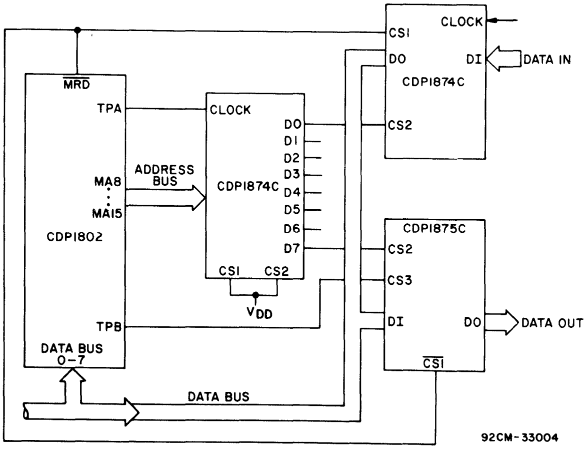


Fig. 6 - CDP1874C used as an input port and address latch with CDP1875C used as an output port.

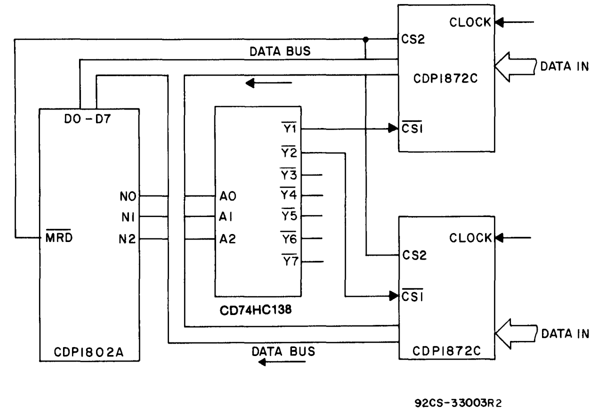


Fig. 7 - CDP1872C used as an input port and selected by CD74HC138.

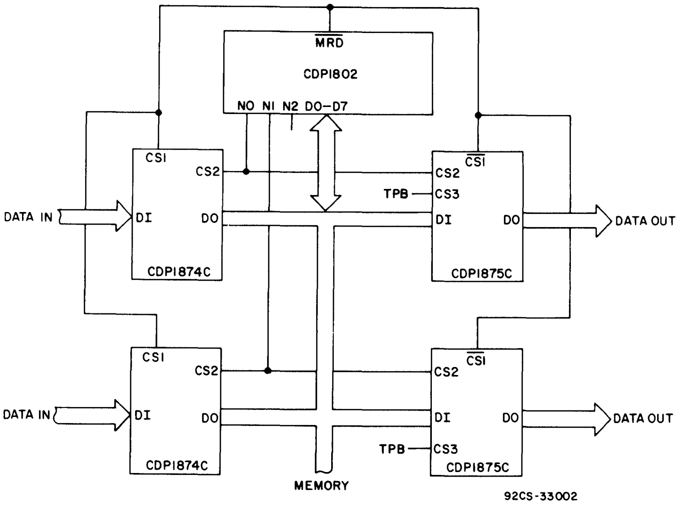
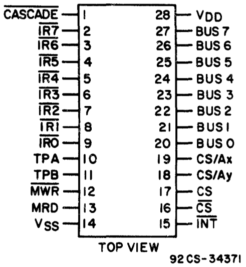


Fig. 8-CDP1874C and CDP1875C used as input/output buffers.

CDP1877, CDP1877C



TERMINAL ASSIGNMENT

Programmable Interrupt Controller (PIC)

Features:

- *Compatible with CDP1800 series*
- *Programmable long branch vector address and vector interval*
- *8 levels of interrupt per chip*
- *Easily expandable*
- *Latched interrupt requests*
- *Hard wired interrupt priorities*
- *Memory mapped*
- *Multiple chip select inputs to minimize address space requirements*

The RCA-CDP1877 and CDP1877C• are programmable 8-level interrupt controllers designed for use in CDP1800-series microprocessor systems. They provide added versatilty by extending the number of permissible interrupts from 1 to N in increments of 8.

When a high to low transition occurs on any of the PIC interrupt lines ($\overline{\text{IR0}}$ to $\overline{\text{IR7}}$), it will be latched and, unless the request is masked, it will cause the $\overline{\text{INTERRUPT}}$ line on the PIC and consequently the $\overline{\text{INTERRUPT}}$ input on the CPU to go low.

The CPU accesses the PIC by having interrupt vector register R(1) loaded with the memory address of the PIC. After the interrupt S3 cycle, this register value will appear at the CPU address bus, causing the CPU to fetch an instruction from the PIC. This fetch cycle clears the interrupt request latch bit to accept a new high-to-low transition, and also causes the PIC to issue a long branch instruction (CO) followed by the preprogrammed vector address written into the PIC's address registers, causing the CPU to branch to the address corresponding to the highest priority active interrupt request.

- • Formerly RCA-Dev. Type No. TA10911 and TA10911C, respectively.

If no other unmasked interrupts are pending, the $\overline{\text{INTERRUPT}}$ output of the PIC will return high. When an interupt is requested on a masked interrupt line, it will be latched but it will not cause the PIC $\overline{\text{INTERRUPT}}$ output to go low. All pending interrupts, masked and unmasked, will be indicated by a "1" in the corresponding bit of the status register. Reading of the status register will clear all pending interrupt request latches.

Several PICs can be cascaded together by connecting the $\overline{\text{INTERRUPT}}$ output of one chip to the $\overline{\text{CASCADE}}$ input of another. Each cascaded PIC provides 8 additional interrupt levels to the system. The number of units cascadable depends on the amount of memory space and the extent of the address decoding in the system.

Interrupts are prioritized in descending order; $\overline{\text{IR7}}$ has the highest and $\overline{\text{IR0}}$ has the lowest priority.

The CDP1877 and CDP1877C are functionally identical. They differ in that the CDP1877 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1877C has a recommended operating voltage range of 4 to 6.5 volts. They types are supplied in 28-lead dual-in-line ceramic packages (D suffix), and 28-lead dual-in-line plastic packages (E suffix).

Programmable Interrupt Controller (PIC) Programming Model

BUS 7			PAGE REGISTER				BUS 0	
A15	A14	A13	A12	A11	A10	A9	A8	WRITE ONLY

BUS 7			CONTROL REGISTER				BUS 0	
B7	B6	B5	B4	B3	B2	B1	B0	WRITE ONLY

BUS 7			MASK REGISTER				BUS 0	
M7	M6	M5	M4	M3	M2	M1	M0	WRITE ONLY

BUS 7			STATUS REGISTER				BUS 0	
S7	S6	S5	S4	S3	S2	S1	S0	READ ONLY

BUS 7			POLLING REGISTER				BUS 0	
P7	P6	P5	P4	P3	P2	P1	P0	READ ONLY

File Number **1319**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal)
CDP1877 .... −0.5 to +11 V
CDP1877C .... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A=−40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A=−55 to +100°C (PACKAGE TYPE D) .... 500 mW
For T_A=+100 to 125°C (PACKAGE TYPE D) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D .... −55 to +125°C
PACKAGE TYPE E .... −40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85°C, V_{DD} ±5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1877			CDP1877C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device	—	0, 5	5	—	0.01	50	—	0.02	200	µA
Current I_{DD}	—	0, 10	10	—	1	200	—	—	—	
Output Low Drive	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
(Sink) Current I_{OL}	0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive	4.6	0, 5	5	−1.15	−2.3	—	−1.15	−2.3	—	
(Source) Current I_{OH}	9.5	0, 10	10	−2.6	−5.2	—	—	—	—	
Output Voltage	—	0, 5	5	—	0	0.1	—	0	0.1	V
Low-Level V_{OL}‡	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage	—	0, 5	5	4.9	5	—	4.9	5	—	
High Level V_{OH}‡	—	0, 10	10	9.9	10	—	—	—	—	
Input Low	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
Voltage V_{IL}	0.5,9.5	—	10	—	—	3	—	—	—	
Input High	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
Voltage V_{IH}	0.5,9.5	—	10	7	—	—	—	—	—	
Input Leakage	Any	0, 5	5	—	—	±1	—	—	±1	µA
Current I_{IN}	Input	0, 10	10	—	—	±2	—	—	—	
3-State Output Leakage	0, 5	0, 5	5	—	$\pm10^{-4}$	±1	—	$\pm10^{-4}$	±1	
Current I_{OUT}	0, 10	0, 10	10	—	$\pm10^{-4}$	±10	—	—	—	
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device			5	—	0.5	1.0	—	0.5	1.0	mA
Current I_{OPER}#			10	—	1.9	3.0	—	—	—	

*Typical values are for T_A=25°C and nominal V_{DD}. ‡I_{OL}=I_{OH}=1 µA.

# Operating current measured under worst-case conditions in a 3.2-MHz CDP1802A system: one PIC access per instruction cycle.

CDP1877, CDP1877C

OPERATING CONDITIONS at T_A=Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1877		CDP1877C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

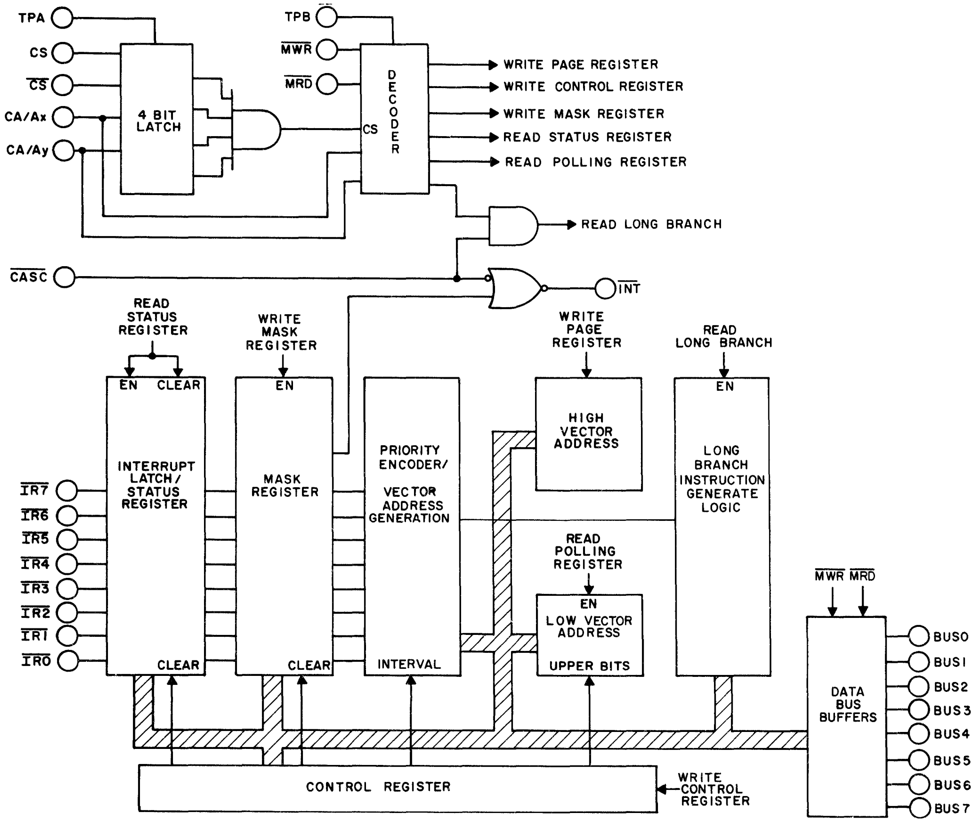


Fig. 1 - Functional diagram for CDP1877.

92CL-34372

Functional Definitions for CDP1877 and CDP1877C Terminals

TERMINAL	USAGE	TYPE
V_{DD}—V_{SS}	Power	
BUS0—BUS7	Data bus—Communicates information to and from CPU	Bidirectional
$\overline{IR0}$—$\overline{IR7}$	Interrupt Request Lines	Input
$\overline{INTERRUPT}$	Interrupt to CPU	Output
$\overline{MRD}$, $\overline{MWR}$	Read/Write controls from CPU	Input
TPA, TPB	Timing pulses from CPU	Input
CS, $\overline{CS}$	Chip selects, Enable Chip if valid during TPA	Input
CS/Ax, CS/Ay	Used as a Chip Select during TPA and as a Register address during Read/Write Operations	Input
$\overline{CASCADE}$	Used for cascading several PIC units. The $\overline{INTERRUPT}$ output from a higher priority PIC can be tied to this input, or the input can be tied to Vdd if cascading is not used.	Input

PIC Programming Model

INTERNAL REGISTERS

The PIC has three write-only programmable registers and two read-only registers.

Page Register

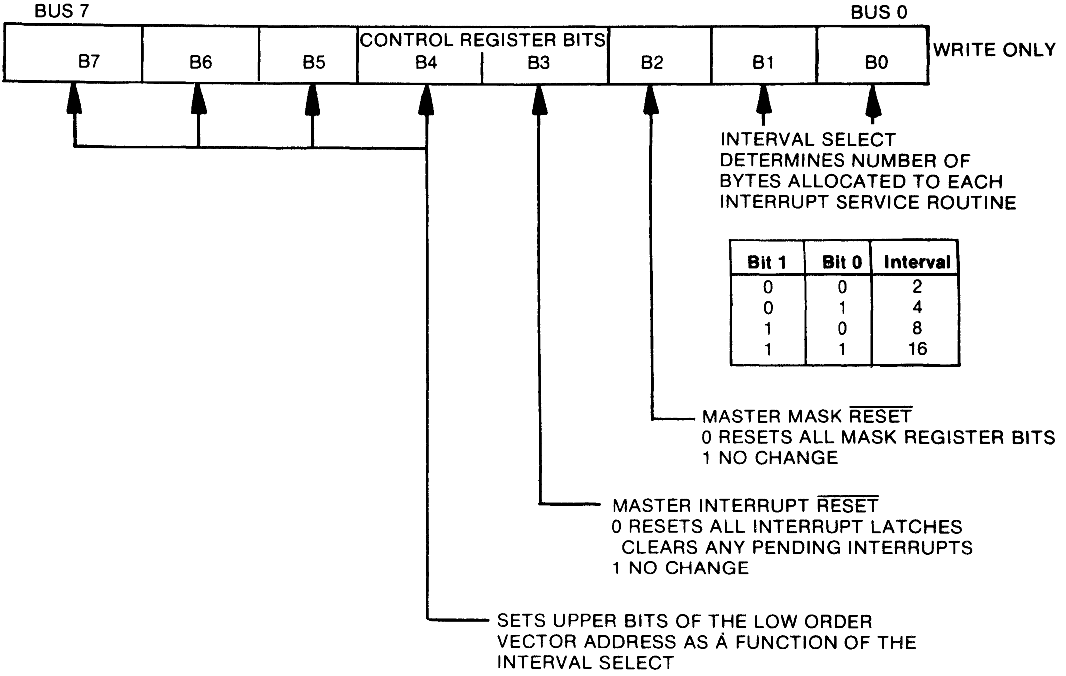
This write only register contains the high order vector address the device will issue in response to an interupt request. This high-order address will be the same for any of the 8 possible interrupt requests; thus, interrupt vectoring differs only in location within a specified page.

BUS 7 — BUS 0

			PAGE REGISTER BITS					
A15	A14	A13	A12	A11	A10	A9	A8	WRITE ONLY

Control Register

The upper nibble of this write-only register contains the low order vector address the device will issue in response to an interrupt request. The lower nibble is used for a master interrupt reset, master mask reset and for interval select.



INTERVAL SELECT
DETERMINES NUMBER OF
BYTES ALLOCATED TO EACH
INTERRUPT SERVICE ROUTINE

Bit 1	Bit 0	Interval
0	0	2
0	1	4
1	0	8
1	1	16

MASTER MASK $\overline{\text{RESET}}$
0 RESETS ALL MASK REGISTER BITS
1 NO CHANGE

MASTER INTERRUPT $\overline{\text{RESET}}$
0 RESETS ALL INTERRUPT LATCHES
CLEARS ANY PENDING INTERRUPTS
1 NO CHANGE

SETS UPPER BITS OF THE LOW ORDER
VECTOR ADDRESS AS A FUNCTION OF THE
INTERVAL SELECT

THE LOW ORDER VECTOR ADDRESS WILL BE SET ACCORDING TO THE TABLE BELOW:

INTERVAL SELECTED-NO. OF BYTES	LOW ADDRESS BITS BIT B7	BIT B6	BIT B5	BIT B4
2	SETS A7	SETS A6	SETS A5	SET A4
4	SETS A7	SETS A6	SETS A5	X
8	SETS A7	SETS A6	X	X
16	SETS A7	X	X	X

X=DON'T CARE

NOTE: All DON'T CARE Addresses and Addresses A0-A3 are determined by interrupt request.

Mask Register

A "1" written into any location in this write only register will mask the corresponding interrupt request line. All interrupt inputs (except $\overline{\text{CASCADE}}$) are maskable.

BUS 7							BUS 0	
			MASK BITS					WRITE ONLY
M7	M6	M5	M4	M3	M2	M1	M0	

Status Register

In this read only register a "1" will be present in the corresponding bit location for every masked or unmasked pending interrupt.

BUS 7							BUS 0	
			STATUS BITS					READ ONLY
S7	S6	S5	S4	S3	S2	S1	S0	

Polling Register

This read only register provides the low order vector address and is used to identify the source of interrupt if a polling technique, rather than interrupt servicing, is used.

BUS 7							BUS 0	
			POLLING BITS					READ ONLY
P7	P6	P5	P4	P3	P2	P1	P0	

RESPONSE TO INTERRUPT (AFTER S3 CYCLE)

The PIC's response to interrogation by the CPU is always 3 bytes long, placed on the data bus in consecutive bytes in the following format:

First (Instruction) Byte:

LONG BRANCH INSTRUCTION - CO (Hex)

BUS 7							BUS 0
1	1	0	0	0	0	0	0

Second (High-Order Address) Byte

This byte is the High-Order vector Address that was written into the PIC's Page Register by the user. The PIC does not alter this value in any way.

High-Order Vector Address

BUS 7							BUS 0
A15	A14	A13	A12	A11	A10	A9	A8

Third (Low-Order Address) Bytes

INTERVAL 2

BUS 7							BUS 0
A7	A6	A5	A4	▨ I2	▨ I1	▨ I0	0

INTERVAL 4

BUS 7							BUS 0
A7	A6	A5	▨ I2	▨ I1	▨ I0	0	0

INTERVAL 8

BUS 7							BUS 0
A7	A6	▨ I2	▨ I1	▨ I0	0	0	0

INTERVAL 16

BUS 7							BUS 0
A7	▨ I2	▨ I1	▨ I0	0	0	0	0

▨ Indicates active interrupt input number (binary 0 to 7).

Bits indicated by Ax (x=4 to 7) are the same as programmed into the Control Register. All other bits are generated by the PIC.

REGISTER ADDRESSES

In order to read/write or obtain an interrupt vector from any PIC in the system, all chip selects (CS/Ax, CS/Ay, CS, $\overline{CS}$) must be valid during TPA.

CS/Ax and CS/Ay are multiplexed addresses; both must be high during TPA, and set according to this table during TPB to access the proper register.

CS/Ax	CS/Ay	$\overline{RD}$	$\overline{WR}$	ACTION TAKEN
1	0	0	1	READ Long Branch instruction and vector for highest priority unmasked interrupt pending.
1	0	1	0	WRITE to Page Register
0	1	1	0	WRITE to Control Register
0	0	0	1	READ Status Register
0	0	1	0	WRITE to Mask Register
0	1	0	1	READ Polling Register (Used to identify INTERRUPT source if Polling technique rather than INTERRUPT service is used.)
1	1	X	X	Unused condition

CDP1877, CDP1877C

PIC Application Examples

Example I—Single PIC Application

Fig. 2 shows all the connections required between CPU and PIC to handle eight levels of interrupt control.

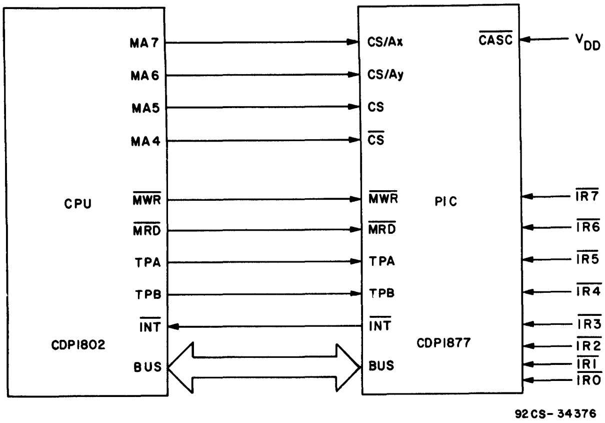


Fig. 2 - PIC and CPU connection diagram.

Programming

Programming the PIC consists of the following steps:

1. Disable interrupt at CPU.
2. Reset Master Interrupt Bit, B3, of Control Register.
3. Write a "1" into the Interrupt Input bit location of the Mask Register, if masking is desired.
4. Write the High-Order Address byte into the Page Register.
5. Write the Low-Order Address and the vector interval into the Control Register.
6. Program R(1) of the CPU to point to the PIC so that the Long Branch instruction can be read from the PIC during the Interrupt Service routine.

Values for Example I with LOCATION 84E0 arbitrarily chosen as the Vector Address with interval of eight bytes, $\overline{\text{IR4}}$ pending, is shown in Table I.

In deriving the above addresses, all DON'T CARE bits are assumed to be 0.

When an INTERRUPT ($\overline{\text{IR4}}$) is received by the CPU, it will address the PIC and will branch to the interrupt service routine.

The three bytes generated by the PIC will be:

1st Byte=$C0_H$
2nd Byte=84_H
3rd Byte=$E0_H$

Table I — Register Address Values

REGISTER	REGISTER ADDRESS	OPERATION	DATA BYTE
MASK	E000H	WRITE	00_H
CONTROL	E040H	WRITE	CE_H
PAGE	E080H	WRITE	84_H
STATUS	E000H	READ	10_H
POLLING	E040H	READ	E0H
R(1) (IN CPU)	E080H	—	—

Example II—Multi-PIC Application

Fig. 3 shows all the connections required between CPU and PICs to handle sixteen levels of interrupt control.

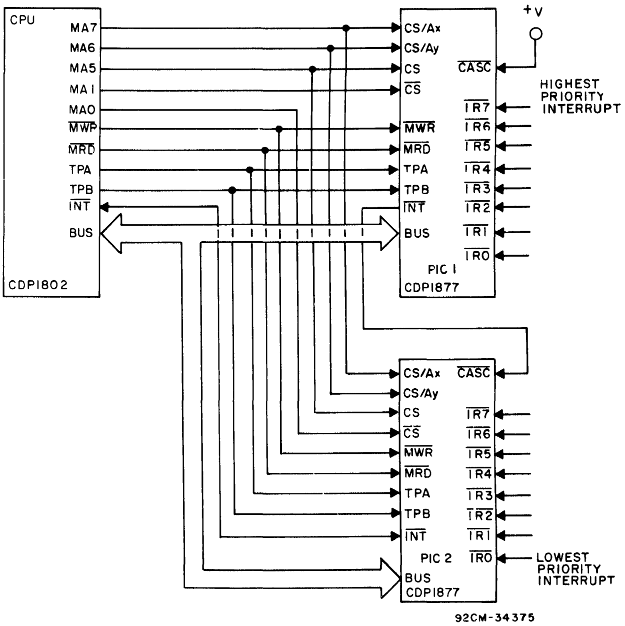


Fig. 3 - PICs and CPU connection diagram.

Register Address Assignments

The low-byte register address for any WRITE or READ operation is the same as shown in Table I.

The high-byte register differs for each PIC because of the linear addressing technique shown in the example:

PIC 1=111XXX01 (E1$_{H}$ FOR X=0)
PIC 2=111XXX10 (E2$_{H}$ FOR X=0)

The R(1) vector address is unchanged. This address will select both PICs simultaneously (R(1).1=111XXX00=E0$_{H}$). Internal CDP1877 logic controls which PIC will respond when an interrupt request is serviced.

Additional PIC Application Comments

The interval select options provide significant flexibility for interrupt routine memory allocations:

- The 2-byte interval allows one to dedicate a full page to interrupt servicing, with variable space between routines, by specifying indirect vectoring with 2 byte short branch instructions on the current page.
- The 4-byte interval allows for a 3 byte long branch to any location in memory where the interrupt service routine is located. The branch can be preceded by a Save Instruction to save previous contents of X and P on the stack.
- The 8-byte and 16-byte intervals allow enough space to perform a service routine without indirect vectoring. The amount of interval memory can be increased even further if all 8 INTERRUPTS are not required. Thus a 4-level interrupt system could use alternate $\overline{IR}$ Inputs, and expand the interval to 16 and 32 bytes, respectively.

The 4 Chip Selects allow one to conserve total allotted memory space to the PIC. For one chip, a total of 4 address lines could be used to select the device, mapping it into as little as 4-K of memory space. Note that this selection technique is the only one that allows the PIC to work properly in the system: I/O mapping cannot be used because the PIC must work within the CDP1800 interrupt structure to define the vector address. Decoded signals also will not work because the chip selects must be valid on the trailing edge of TPA.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, V_{DD} ±5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=50 pF

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1877			CDP1877C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Address to TPA Setup Time	t_{AS}	5	60	—	—	60	—	—	ns
		10	40	—	—	—	—	—	
Address to TPA Hold Time	t_{AH}	5	60	—	—	60	—	—	
		10	40	—	—	—	—	—	
Data Valid after TPB	t_{DTPB}	5	370	—	—	370	—	—	
		10	210	310	—	—	—	—	
Data Hold Time from Write	t_{HW}	5	30	—	—	30	—	—	
		10	40	—	—	—	—	—	
Address to Valid Data Access Time	t_{DR}	5	—	340	490	—	340	490	
		10	—	125	230	—	—	—	
Data Setup Time to Write	t_{DSU}	5	0	—	—	0	—	—	
		10	0	—	—	—	—	—	
Address Hold from TPB	t_{HTPB}	5	80	—	—	80	—	—	
		10	40	—	—	—	—	—	
Minimum $\overline{MWR}$ Pulse Width	$t_{\overline{MWR}}$	5	130	—	—	130	—	—	
		10	60	—	—	—	—	—	
Minimum $\overline{IR}$ Pulse Width	$t_{\overline{IRX}}$	5	130	—	—	130	—	—	
		10	60	—	—	—	—	—	

* Typical values are for T_A=25°C and V_{DD} ±5%.

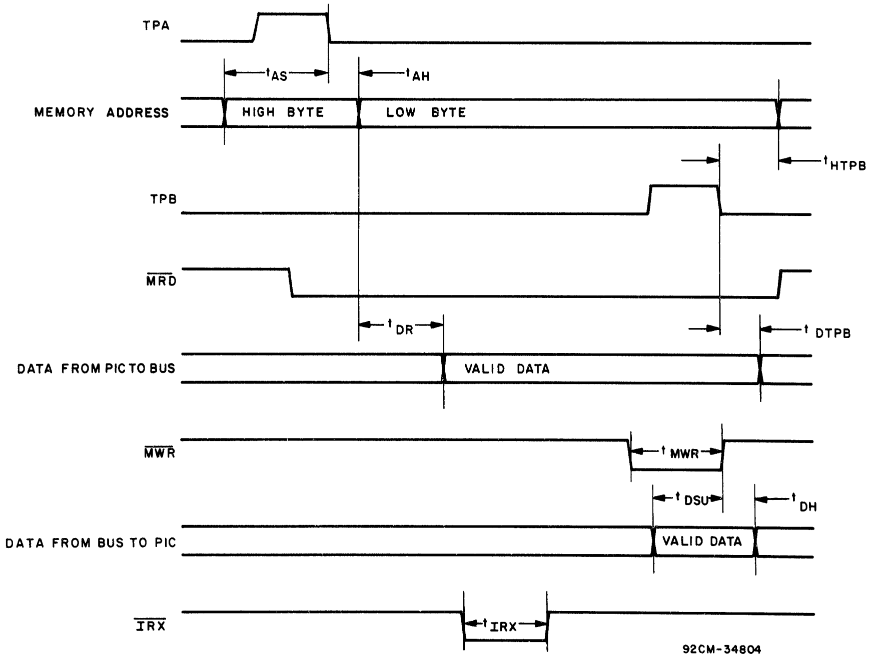
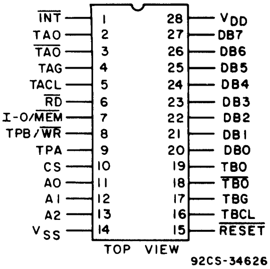


Fig. 4 - Timing waveforms for CDP1877.

CDP1878, CDP1878C



TERMINAL ASSIGNMENT

CMOS Dual Counter-Timer

Features:

- *Compatible with general-purpose and CDP1800-series microprocessor systems*
- *Two 16-bit down-counters and two 8-bit control registers*
- *5 modes including a versatile variable-duty cycle mode*
- *Programmable gate-level select*
- *Two-complemented output pins for each counter-timer*
- *Software-controlled interrupt output*
- *Addressable in memory space or CDP1800-series I/O space*

The RCA-CDP1878 and CDP1878C[Δ] are dual counter-timers consisting of two 16-bit programmable down counters that are independently controlled by separate control registers. The value in the registers determine the mode of operation and control functions. Counters and registers are directly addressable in memory space by any general-industry-type microprocessors, in addition to input/output mapping with the CDP1800-series microprocessors.

Each counter-timer can be configured in five modes with the additional flexibility of gate-level control. The control registers in addition to mode formatting, allow software start and stop, interrupt enable, and an optional read control that allows a stable readout from the counters. Each counter-timer has software control of a common interrupt output with an interrupt status register indicating which counter-timer has timed out.

In addition to the interrupt output, true and complemented outputs are provided for each counter-timer for control of peripheral devices.

The CDP1878 and CDP1878C are functionally identical. They differ in that the CDP1878 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1878C has a recommended operating voltage range of 4 to 6.5 volts. These types are supplied in 28-lead dual-in-line ceramic packages (D suffix), and 28-lead dual-in-line plastic packages (E suffix).

[Δ] Formerly RCA Dev. Type No. TA10981 and TA10981C, respectivel

Table I - Mode Description

Mode		Function	Application
1	Timeout	Outputs change when clock decrements counter to "0"	Event counter
2	Timeout Strobe	One clockwide output pulse when clock decrements counter to "0"	Trigger pulse
3	Gate-Controlled One Shot	Outputs change when clock decrements counter to "0". Retriggerable	Time-delay generation
4	Rate Generator	Repetitive clockwide output pulse	Time-base generator
5	Variable-Duty Cycle	Repetitive output with programmed duty cycle	Motor control

OPERATING CONDITIONS at T_A=Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1878		CDP1878C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	
Maximum Clock Input Rise or Fall Time t_r, t_f	—	5	—	5	μs
Minimum Clock Pulse Width t_{WL}, t_{WH}	200	—	200	—	ns
Maximum Clock Input Frequency, f_{CL}	DC	1	DC	1	MHz

File Number **1341**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltage referenced to V_{SS} terminal)	
CDP1878	-0.5 to +11 V
CDP1878C	-0 5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A=-40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A=+60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 12 mW/° C to 200 mW
For T_A=-55 to +100° C (PACKAGE TYPE D)	500 mW
For T_A=+100 to 125° C (PACKAGE TYPE D)	Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A).	
PACKAGE TYPE D	-55 to +125° C
PACKAGE TYPE E	-40 to +85° C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING).	
At distance 1/16 ± 1/32 in. (1 59 ± 0.79 mm) from case for 10 s max	+265° C

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, V_{DD} ±5%, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS						UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1878			CDP1878C			
					Min.	Typ.•	Max.	Min.	Typ.•	Max.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	μA
		—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
		0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	—	-1.15	-2.3	—	
		9.5	0, 10	10	-2.6	-5.2	—	—	—	—	
Output Voltage Low-Level	V_{OL}‡	—	0, 5	5	—	0	0.1	—	0	0.1	V
		—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level	V_{OH}‡	—	0, 5	5	4.9	5	—	4.9	5	—	
		—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	
		0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage	V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	
		0.5, 9.5	—	10	7	—	—	—	—	—	
Input Leakage Current	I_{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	μA
			0, 10	10	—	—	±2	—	—	—	
Operating Current	I_{DD1}Δ	—	0, 5	5	—	1.5	3	—	1.5	3	mA
		—	0, 10	10	—	6	12	—	—	—	
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	—	10	15	

•Typical values are for T_A=25° C and nominal V_{DD} ‡I_{OL}=I_{OH}=1 μA.

ΔOperating current is measured at 200 kHz for V_{DD}=5 V and 400 kHz for V_{DD}=10 V, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2 MHz)

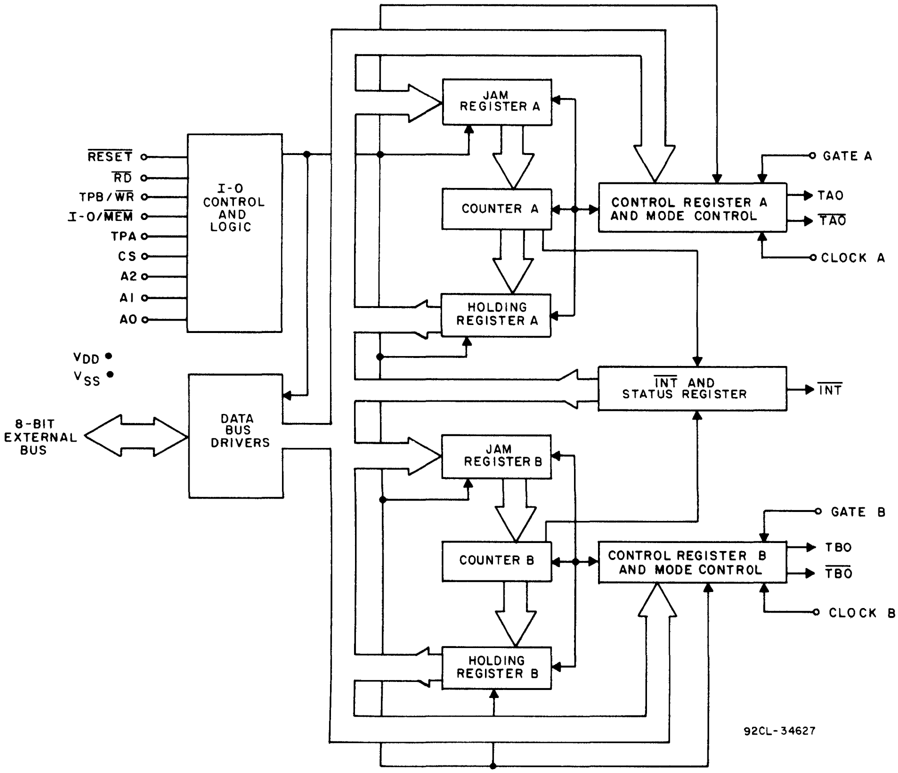


Fig. 1 - Functional diagram CDP1878 and CDP1878C.

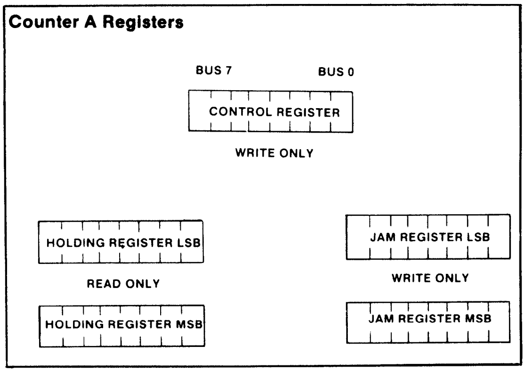
Functional Definitions for CDP1878 and CDP1878C Terminals

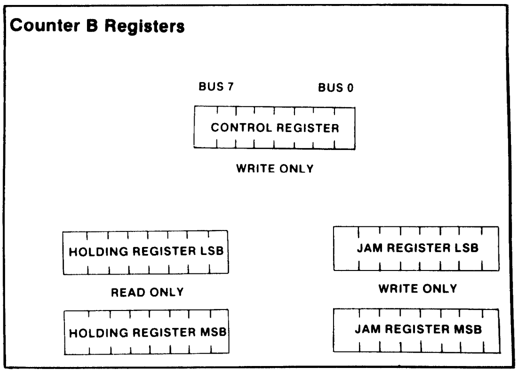
TERMINAL	USAGE	TERMINAL	USAGE
V_{DD}-V_{SS}	Power		
DB0-DB7	Data to and from device	CS	Active high input that enables device
TPB/$\overline{WR}$, $\overline{RD}$	Directional control signals	$\overline{INT}$	Low when counter is "0"
A0, A1, A2	Addresses that select counters or registers	$\overline{RESET}$	When active, TAO, TBO are low, $\overline{TAO}$, $\overline{TBO}$ are high. Interrupt status register is cleared
TACL, TBCL	Clocks used to decrement counters		
TAG, TBG	Gate inputs that control counters	I-O/$\overline{MEM}$	Tied high in CDP1800 input/output mode, otherwise tied low
TAO, $\overline{TAO}$	Complemented outputs of Timer A		
TBO, $\overline{TBO}$	Complemented outputs of Timer B		
TPA	Used with CDP1800-series processors, tied high otherwise		

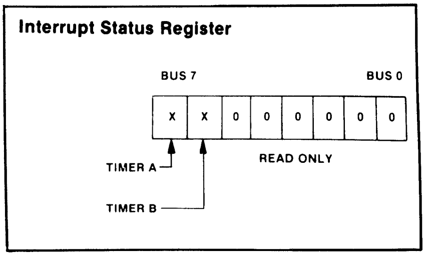
REGISTER TRUTH TABLE

ADDRESS			ACTIVE		REGISTER OPERATION
A2	A1	A0	TPB/$\overline{WR}$	$\overline{RD}$	
1	1	0	X		Write Counter A MSB
1	1	0		X	Read Counter A MSB
0	1	0	X		Write Counter A LSB
0	1	0		X	Read Counter A LSB
1	0	0	X		Control Register A
1	1	1	X		Write Counter B MSB
1	1	1		X	Read Counter B MSB
0	1	1	X		Write Counter B LSB
0	1	1		X	Read Counter B LSB
1	0	1	X		Control Register B
1	0	0		X	Interrupt Status Register
1	0	1		X	
0	0	0			Not Used
0	0	1			Not Used

PROGRAMMING MODEL







Functional Description—See Fig. 1

The dual counter-timer consists of two programmable 16-bit down counters, separately addressable and controlled by two independent 8-bit control registers. The word in the control register determines the mode and type of operation that the counter-timer performs. Writing to or reading from a counter or register is enabled by selective addressing during a write or read cycle. The data is placed on the data bus by the microprocessor during the write cycle or read from the counter during the read cycle. Data to and from the counters and to the control registers is in binary format.

Each counter-timer consists of three parts. The first is the counter itself, a 16-bit down counter that is decremented on the trailing edge of the clock input. The second is the jam register that receives the data when the counter is written to. The word in the control register determines when the jam register value is placed into the counter. The third part is the holding register that places the counter value on the data bus when the counter is read.

When the counter has decremented to zero, three events occur. The first involves the common interrupt output pin that, if enabled, becomes active low. The second is the setting of a bit in the interrupt status register. This register can be read to determine which counter-timer has timed out. The third event is the logic change of the complemented output pins.

In addition to the clock input used to decrement the counter, a gate input is available to enable or initiate operation. The counter-timers are independent and can have different mode operations.

Write Operation

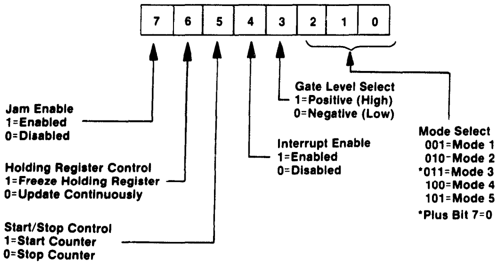
The counters and registers are separately addressable and are programmed via the data bus when the chip is selected with the TPB/$\overline{\text{WR}}$ pin active. Normal sequencing requires that the counter jam register be loaded first with the required value (most significant and least significant byte in any order), and then the control register be accessed and loaded with the control word. The trailing edge of the TPB/$\overline{\text{WR}}$ pulse will latch the control word into the control register. The trailing edge of the first clock to occur with gate valid will cause the counter to be jammed with its initial value. The counter will decrement on the trailing edge of succeeding clocks as long as the gate is valid, until it reaches zero. The output levels will then change, and if enabled, the interrupt output will become active and the appropriate timer bit will be set in the interrupt status register. The interrupt output and the interrupt status register can be cleared (to their inactive state) by addressing the control register with the TPB/$\overline{\text{WR}}$ line active. For example, if counter A times out, control register A must be accessed to reset the interrupt output high and reset the timer A bit in the status register low. Timer B bit in the status register will be unaffected.

Read Operation

Each counter has a holding register that is continuously being updated by the counter and is accessed when the counter is addressed during read cycles. Counter reads are accomplished by halting the holding register and then reading it, or by reading the holding register directly. If the holding register is read directly, data will appear on the bus if the counters are addressed with the $\overline{\text{RD}}$ line active. However, if the clock decrements the counter between the two read operations (most and least significant byte), an inaccurate value will be read. To preclude this from happening, writing a "1" into bit 6 of the control register and then addressing and reading the counter will result in a stable reading. This operation prevents the holding register from being updated by the counter and does not affect the counter's operation.

The interrupt status register is read by addressing either control register with the $\overline{\text{RD}}$ line active. A "1" in bit 7 indicates Timer A has timed out and a "1" in bit 6 indicates Timer B has timed out. Bits 0-5 are zeros.

Control Register



Bits 0, 1 and 2 — Mode Selects—See Mode Timing Diagrams (Figs. 2, 3, 4, 5 and 6).

	Bit 7	Bit 2	Bit 1	Bit 0
Mode 1 — Timeout	—	0	0	1
Mode 2 — Timeout Strobe	—	0	1	0
Mode 3 — Gate Controlled One Shot	0	0	1	1
Mode 4 — Rate Generator	—	1	0	0
Mode 5 — Variable-Duty Cycle	—	1	0	1
No Mode selected. Counter outputs unaffected.	—	0	0	0

Note: When selecting a mode, the timer outputs TAO and TBO are set low, and $\overline{\text{TAO}}$ and $\overline{\text{TBO}}$ are set high. If bits 0, 1 and 2 are all zero's when the control register is loaded, no mode is selected, and the counter-timer outputs are unaffected. Issuing mode 6 will cause an indeterminate condition of the counter, issuing mode 7 is equivalent to issuing mode 5.

CDP1878, CDP1878C

Bit 3—Gate level select—All modes require an enabling signal on the gate to allow counter operation. This enabling signal is either a level or a pulse (edge). Positive gate level or edge enabling is selected by writing a "1" into this bit and negative (low) enabling is selected when bit 3 is "0".

Bit 4—Interrupt enable—Setting this bit to "1" enables the $\overline{\text{INT}}$ output, and setting it to "0" disables it. When reset, the $\overline{\text{INT}}$ output is at a high level. If the interrupt enable bit in the control register is enabled and the counter decrements to zero, the $\overline{\text{INT}}$ output will go low and will not return high until the counter-timer is reset or the selected control register is written to. Example: If timer B times out, control register B must be accessed to reset the $\overline{\text{INT}}$ output high. If the interrupt enable bit is set to "0", the counter's timeout will have no effect on the $\overline{\text{INT}}$ output.

In mode 5, the variable-duty cycle mode, the $\overline{\text{INT}}$ pin will become active low when the MSB in the counter has decremented to zero.

Bit 5—Start/stop control—This bit controls the clock input to the counter and must be set to "1" to enable it. Writing a "0" into this location will halt operation of the counter. Operation will not resume until the bit is set to "1".

Bit 6—Holding register control—Since the counter may be decrementing during a read cycle, writing a "1" into this location will hold a stable value in the hold register for subsequent read operations. Rewriting a "1" into bit 6 will cause an update in the holding register on the next trailing clock edge. If this location contains a "0", the holding register will be updated continuously by the value in the counter.

Bit 7—Jam enable—When this bit is set to "1" during a write to the control register, the 16-bit value in the jam register will be available to the counter; TAO and TBO are reset low and $\overline{\text{TAO}}$ and $\overline{\text{TBO}}$ are set high. On the trailing edge of the first input clock signal with the gate valid this value will be latched in the counter, the counter outputs TAO and TBO will be set high and the $\overline{\text{TAO}}$ and $\overline{\text{TBO}}$ will be reset low. Setting bit 7 to "0" will leave the counter value unaffected. This location should be set to "0" any time a write to the control register must be performed without changing the present counter value. If the value in the jam register has not been changed, writing a "1" into bit 7 of the control register with zeros in bits 0, 1, and 2 (mode select) will reload the counter with the old value and leave the mode unchanged. If the value in the jam register is changed, then the next write to the control register (with bit 7 a "1") must include a valid mode select (i.e., at least 1 of the bits 0, 1, or 2 must be a "1").

In mode 3, the hardware start is enabled by writing a "0" into bit 7. If a "1" is written to bit 7, the timeout will start immediately and mode 3 will resemble mode 1.

MODE DESCRIPTIONS

Mode		Control Register	Gate Control
1	Timeout	X X X X X 0 0 1 BUS 7 BUS 0	Selectable High or Low Level Enables Operation

Mode 1:
After the count is loaded into the jam register and the control register is written to with the jam-enable bit high on the trailing edge of the first clock after the gate is valid, TXO goes high and $\overline{\text{TXO}}$ goes low. The input clock decrements the counter as long as the gate remains valid. When it reaches zero, TXO goes low and $\overline{\text{TXO}}$ goes high, and if enabled, the interrupt output is set low. Writing to the counter while it is decrementing has no effect on the counter value unless the control register is subsequently written to with the jam-enable bit high. After timeout the counter remains at FFFF unless reloaded.

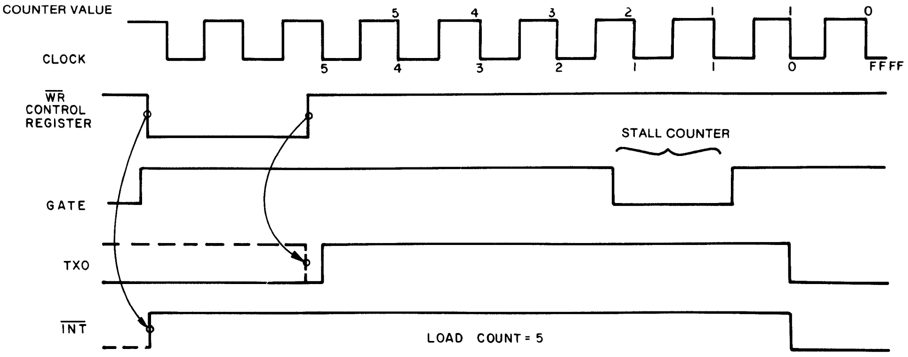


Fig. 2 - Timeout (mode 1) timing waveforms.

Mode		Control Register	Gate Control
2	Timeout Strobe	X X X X X 0 1 0 BUS 7 BUS 0	Selectable High or Low Level Enables Operation

Mode 2:
Operation of this mode is the same as mode 1, except the outputs will change for one clock period only and then return to the condition of TXO high and $\overline{TXO}$ low, and the counter is reloaded.

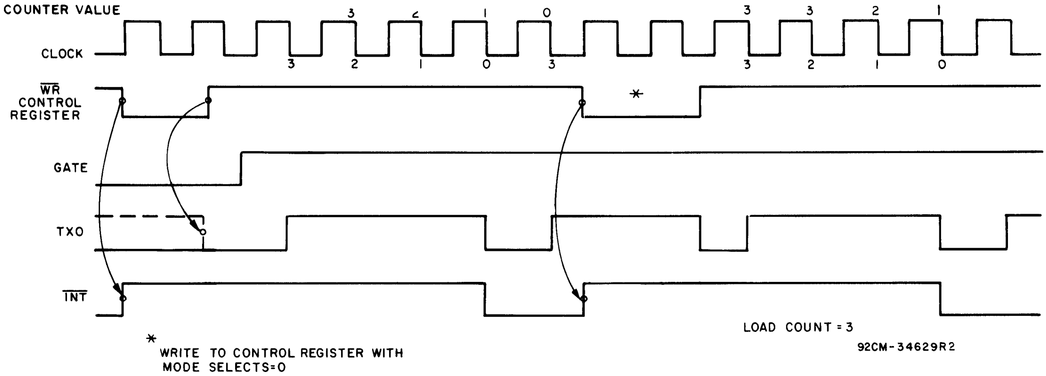


Fig. 3 - Timeout strobe (mode 2) timing waveforms.

Mode		Control Register	Gate Control
3	Gate Controlled One Shot	0 X X X X 0 1 1 BUS 7 BUS 0	Selectable Positive or Negative Going Edge Initiates Operation

Mode 3:
After the jam register is loaded with the required value, the gate edge will initiate this mode. TXO will be set high, and $\overline{TXO}$ will be set low. The clock will decrement the counter. When zero is reached, TXO will go low and $\overline{TXO}$ will be high, and the interrupt output will be set low. The counter is retriggerable: While the counter is decrementing, a gate edge or write to the control register with the jam-enable bit high, will load the counter with the jam register value and restart the one-shot operation.

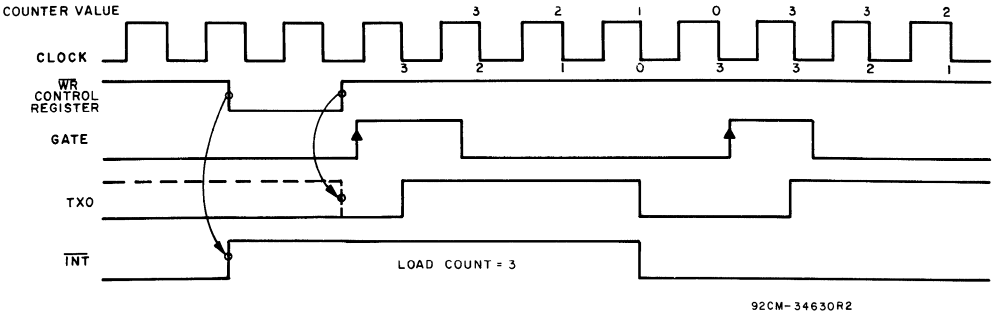


Fig. 4 - Gate controlled one-shot (mode 3) timing waveforms.

CDP1878, CDP1878C

Mode		Control Register	Gate Control
4	Rate Generator	X X X X X 1 0 0 BUS 7 BUS 0	Selectable High or Low Level Enables Operation

Mode 4:

A repetitive clock-wide output pulse will be output, with the time between pulses equal to the counter's value, (trailing edge to leading edge). This model is software started with a write to the control register if the gate level is valid. If the counter is written to while decrementing, the new value will not affect the counter's operation until the present timeout has concluded, unless the control register is written to with the jam-enable bit high. If the gate input (TAG or TBG) is used to start this mode. The first cycle following the gate going true is indeterminate.

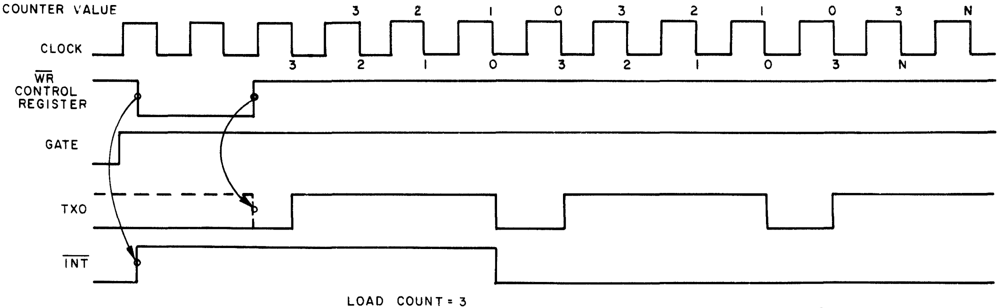


Fig. 5 - Rate generators (mode 4) timing waveforms.

Mode		Control Register	Gate Control
5	Variable Duty Cycle	X X X X X 1 0 1 BUS 7 BUS 0	Selectable High or Low Level Enables Operation

Mode 5:

After the mode is initiated, the outputs will remain at one level until the clock decrements the least significant byte of the counter to N+1. The outputs will then change level and the counter decrements the most significant byte to N+1. The process will then repeat, resulting in a repetitive output with a duty cycle directly controlled by the value in the counter. The output period will be equal to LSB+MSB+2.

The interrupt output will become active after the MSB is loaded into the counter and decrements to zero.

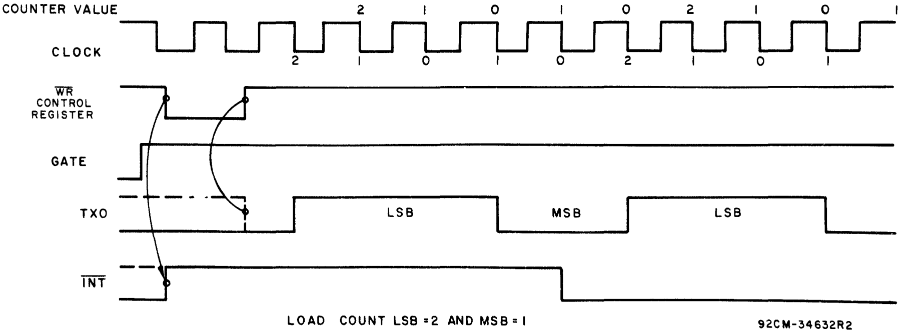


Fig. 6 - Variable-duty cycle (mode 5) timing waveforms.

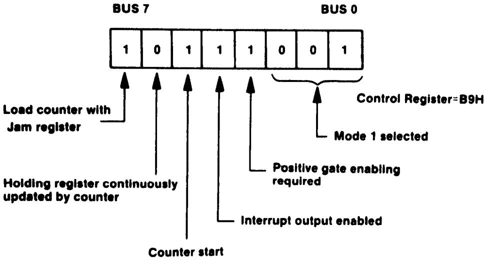
Note:

In order to avoid unwanted starts when selecting mode 3 or 4, the gate signal must be set to the opposite level that will be programmed.

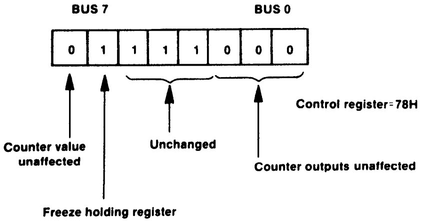
Setting the Control Register

The following will illustrate a counter write and subsequent reads that places stable, accurate values on the data bus from the counter-timer.

The counter is addressed and the required values are loaded with a write operation. The control register is addressed next and loaded with B9H.


BUS 7
BUS 0
1
0
1
1
1
0
0
1
Control Register=B9H
Load counter with Jam register
Mode 1 selected
Positive gate enabling required
Holding register continuously updated by counter
Interrupt output enabled
Counter start

The counter will now decrement with each input clock pulse while the gate is valid. Assuming the counter has not decremented to zero and its value is to be read without affecting the counter's operation, a write to the control register is performed. 78H is loaded into the control register.



The counter is addressed and read operations are performed.

Function Pin Definition

DB7-DB0—8-bit bidirectional bus used to transfer binary information between the microprocessor and the dual counter-timer.

V_{DD}, V_{SS}—Power and ground for device.

A0, A1, and A2—Addresses used to select counters or registers.

TPB/$\overline{\text{WR}}$, $\overline{\text{RD}}$—Directional signals that determine whether data will be placed on the bus from a counter or the interrupt status register ($\overline{\text{RD}}$ active) (memory mapped), or data on the bus will be placed into a counter or control register (TPB/$\overline{\text{WR}}$ active). The following connections are required between the microprocessor and the counter-timer in the CDP1800-series input/output mapping mode.

Microprocessor	Counter-Timer
$\overline{\text{MRD}}$	$\overline{\text{RD}}$
TPB	TPB/$\overline{\text{WR}}$
TPA	TPA
N Lines	Address Lines

and I-O/$\overline{\text{MEM}}$ to V_{DD}.

During an output instruction, data from the memory is strobed into the counter-timer during TPB when $\overline{\text{RD}}$ is active, and latched on TPB's trailing edge. Data is read from the counter-timer when $\overline{\text{RD}}$ is not active between the trailing edges of TPA and TPB. (See Figs. 10, 11, and 12.)

TACL, TBCL—Clocks used to decrement the counter.

TAG, TBG—Gate inputs used to control counter.

TAO, $\overline{\text{TAO}}$—Complemented outputs of Timer A.

TBO, $\overline{\text{TBO}}$—Complemented outputs of Timer B.

$\overline{\text{INT}}$—Common interrupt output. Active when counter decrements to zero.

$\overline{\text{RESET}}$—Active low signal that resets counter outputs (TAO, TBO low, $\overline{\text{TAO}}$, $\overline{\text{TBO}}$ high). The interrupt output is set high and the status register is cleared.

I-O/$\overline{\text{MEM}}$—Tied high in CDP1800-series input/output mode, otherwise tied low.

TPA—Tied to TPA of the CDP1800-series microprocessors. During memory mapping, it is used to latch the high order address bit for the chip select. In the CDP1800 input/output mode, it is used to gate the N lines. When the counter-timer is used with other microprocessors, or when the high order address of the CDP1800-series microprocessors is externally latched, it is connected to V_{DD}.

CS—An active high signal that enables the device.

CDP1878, CDP1878C

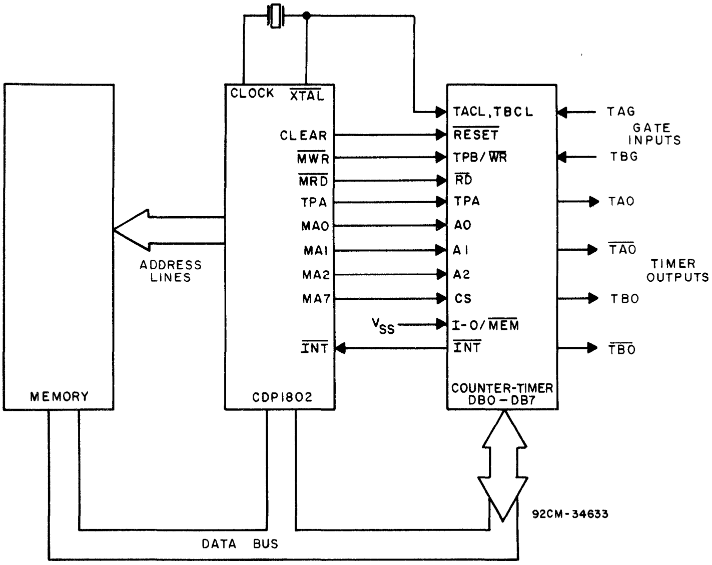


Fig. 7 - Typical CDP1802 memory-mapped system.

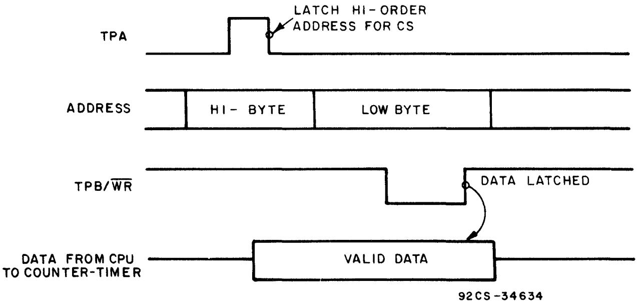


Fig. 8 - CDP1800-series memory-mapping write cycle timing waveforms.

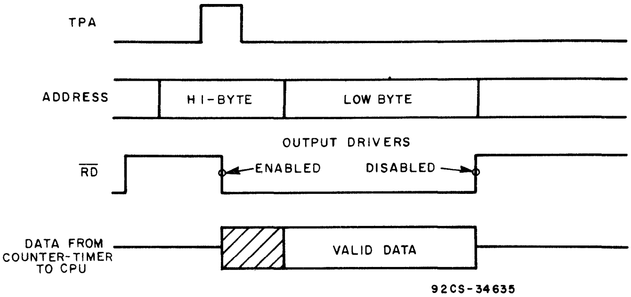


Fig. 9 - CDP1800-series memory-mapping read cycle timing waveforms.

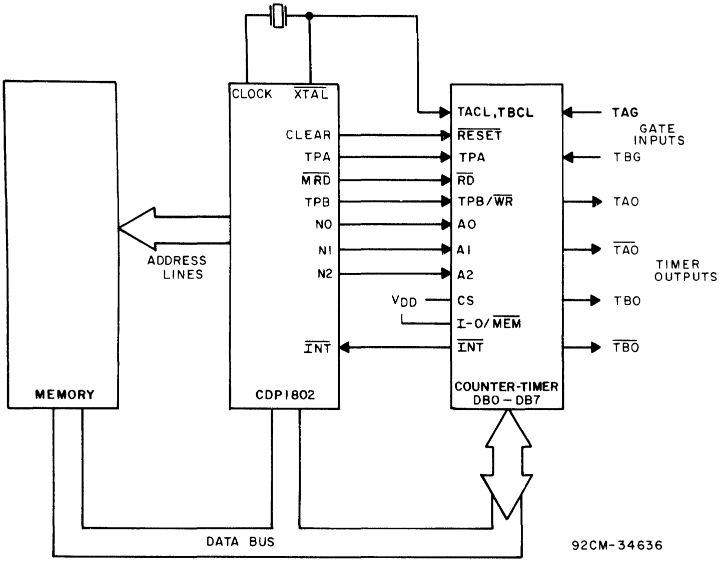


Fig 10 - Typical CDP1802 input/output-mapped system.

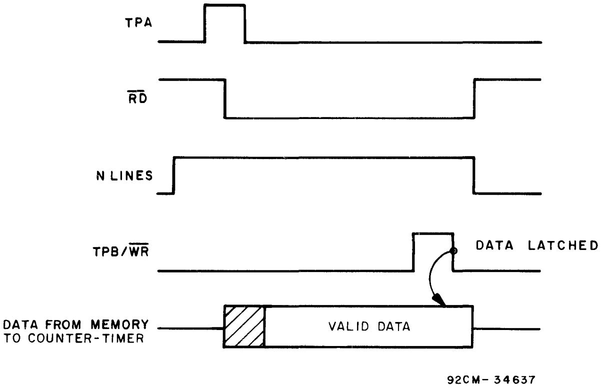


Fig. 11 - CDP1800-series input/output-mapping timing waveforms with output instruction.

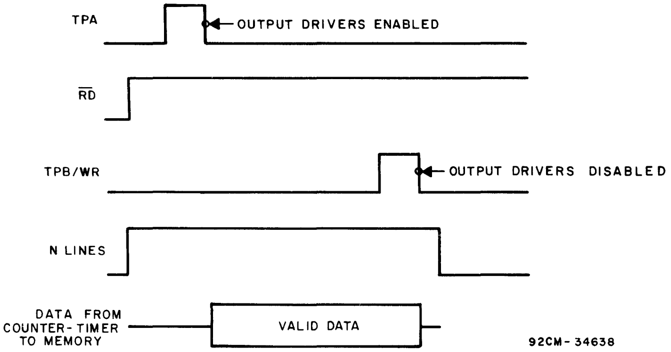


Fig. 12 - CDP1800-series input/output-mapping timing waveforms with input instruction.

CDP1878, CDP1878C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, V_{DD}=5 V ± 5%,
Input t_r,t_f=10 ns; C_L=50 pF and 1 TTL Load

CHARACTERISTIC		LIMITS			UNITS
		Min.†	Typ.•	Max.	
Read Cycle Times (see Fig. 13)					
Data Access from Address	t_{DA}	—	350	—	ns
Read Pulse Width	t_{RD}	400	—	—	
Data Access from $\overline{\text{Read}}$	t_{DR}	—	250	—	
Address Hold after $\overline{\text{Read}}$	t_{RH}	0	—	—	
Output Hold after $\overline{\text{Read}}$	t_{DH}	50	—	—	
Chip Select Setup to TPA	t_{CS}	50	—	—	

†Time required by a limit device to allow for the indicated function.
•Typical values are for T_A=25° C and nominal V_{DD}.

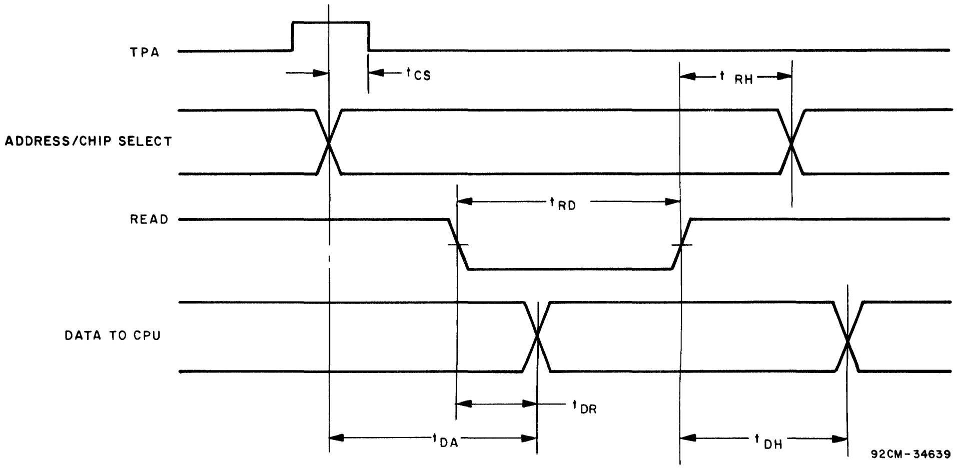


Fig. 13 - Read cycle timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, V_{DD}=5 V ± 5%, Input t_r,t_f=10 ns; C_L=50 pF and 1 TTL Load

CHARACTERISTIC		LIMITS			UNITS
		Min.†	Typ.•	Max.	
Write Cycle Times (see Fig. 14)					
Address Setup to $\overline{\text{Write}}$	t_{AS}	150	—	—	ns
$\overline{\text{Write}}$ Pulse Width	t_{WR}	150	—	—	
Data Setup to $\overline{\text{Write}}$	t_{DS}	200	—	—	
Address Hold after $\overline{\text{Write}}$	t_{AH}	50	—	—	
Data Hold after $\overline{\text{Write}}$	t_{WH}	50	—	—	
Chip Select Setup to TPA	t_{CS}	50	—	—	

†Time required by a limit device to allow for the indicated function.

•Typical values are for T_A=25° C and nominal V_{DD}.

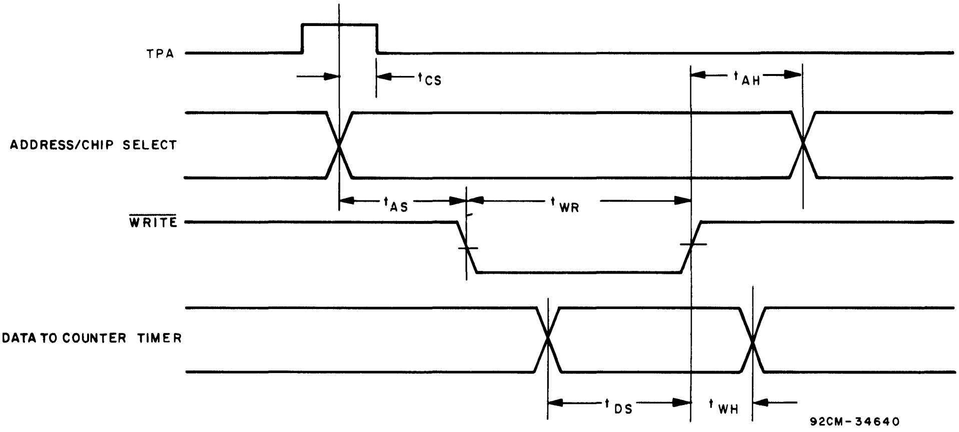
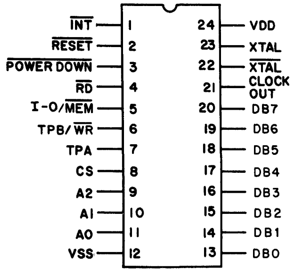


Fig. 14 - Write cycle timing waveforms.

CDP1879, CDP1879C-1



92CS-34345R1

TERMINAL ASSIGNMENT

CMOS Real-Time Clock

Features

- *CPU interface for use with general-purpose microprocessors*
- *Time of day/calendar*
- *Reads seconds, minutes, hours*
- *Reads day of month and month*
- *Alarm circuit with seconds, minutes or hours operation*
- *Power down mode*
- *Separate clock output selects 1 of 15 square wave signals*
- *Interrupt output activated by clock output and/or alarm circuit*
- *Data integrity sampling for clock rollover eliminated*
- *On-board oscillator 4.19 MHz, 2.09 MHz or 1.048 MHz*
  @ 10 V (CDP1879) crystal operation
  4.19 MHz, 2.09 MHz, 1.048 MHz or 32 kHz @ 5 V
  (CDP1879C-1) crystal operation
  4.19 MHz, 2.09 MHz, 1.048 MHz or 32 kHz
  @ 10 V or 5 V external clock operation
- *Addressable in memory space or CDP1800 series I/O mode*
- *Low standby (timekeeping) voltage with external clock*

The CDP1879 real-time clock supplies time and calendar information from seconds to months in BCD format. It consists of 5 separately addressable and programmable counters that divide down an oscillator input. The clock input can have any one of 4 possible frequencies, allowing flexibility in the choice of crystal or external clock sources. Using an external 32-kHz clock source, timekeeping can be performed down to 2.5 V (see Standby (Timekeeping) Voltage Operation).

The device can be memory-mapped for use with any general-purpose microprocessor and has the additional capability of operating in the CDP1800-series input/output mode.

The real-time clock functions as a time-of-day/calendar with an alarm capability that can be set for combinations of seconds, minutes or hours. Alarm time is configured by loading alarm latches that activate an interrupt output through a comparator when the counter and alarm latch values are equal.

Fifteen selectable square-wave signals are available as a separate clock output signal and can also activate the interrupt output. A status register is available to indicate the interrupt source. The value in an 8-bit control register determines the operational characteristics of the device, by selecting the prescaler divisor and the clock output, and controls the load and alarm functions.

A transparent "freeze" circuit precludes clock rollover during counter and latch access times to assure stable and accurate values in the counters and alarm latches.

The CDP1879 is functionally identical to the CDP1879C-1. The CDP1879 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1879C-1 has a recommended operating voltage range of 4 to 6.5 volts. The CDP1879 and the CDP1879C-1 are supplied in 24-lead hermetic dual-in-line side-brazed ceramic packages (D suffix) and 24-lead dual-in-line plastic packages (E suffix).

CDP1879 MODES OF OPERATION

OPERATION	FUNCTION
Read	1. Seconds, minutes, hours, date and month counters 2. Status register to identify interrupt source
Write	1. Control register to set device operation 2. Seconds, minutes, hours, date and month counters 3. Alarm latches for alarm time
Power Down	1. Tri-state interrupt output with active alarm or clock out circuitry for wake-up control. 2. Data bus and address inputs are "DON'T CARE".
Interrupt	1. Clock out as source 2. Alarm time as source 3. Either interrupt can occur during normal or power down mode

File Number **1360**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1879 .... -0.5 to +11 V
CDP1879C-1 .... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/° C to 200 mW
For T_A = -55 to +100° C (PACKAGE TYPE D) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D) .... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 40 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D, H .... -55 to +125° C
PACKAGE TYPE E .... -40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg}) .... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 in (1.59 ± 0.79 mm) from case for 10 s max .... +265° C

OPERATING CONDITIONS at T_A=Full Package-Temperature Range, unless otherwise noted.
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1879		CDP1879C-1		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	
DC Standby (Timekeeping) Voltage* V_{STBY}					V
T_A = -40° to +85°C†	3	—	3	—	
T_A = 0° to +70° C	2.5	—	2.5	—	
Clock Input Rise or Fall Time t_r, t_f					µs
V_{DD} = 5 V	—	10	—	10	
V_{DD} = 10 V	—	1	—	—	

*Timekeeping function only, no READ/WRITE accesses, 32-kHz external frequency source only, no crystal operation.

†See Standby (Timekeeping) Voltage Operation, Page 11.

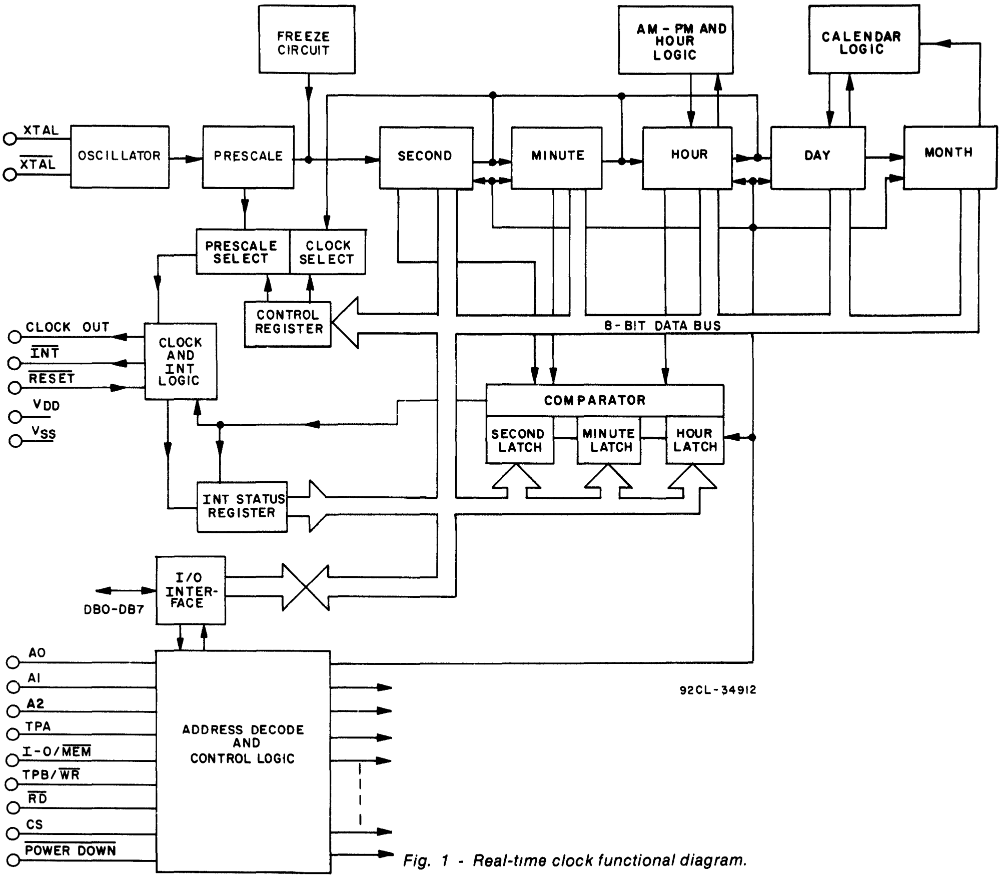


Fig. 1 - Real-time clock functional diagram.

TABLE I

Control Register Bit Assignment	
Bit 1, 0	
Frequency 00	32768 Hz
Select 01	1.048576 MHz
10	2.097152 MHz
11	4.194304 MHz
Bit 2	
Start/Stop	1 = Start 0 = Stop
Bit 3	
Counter/Latch Control "0" = Write to counter and disable alarm "1" = Write to & enable alarm Clock Select	
Bits 7, 6, 5, 4	
0000 — disable μs	1000 — 62.5 ms
0001 — 488.2 μs	1001 — 125 ms
0010 — 976.5 μs	1010 — 250 ms
0011 — 1953.1 μs	1011 — 500 ms
0100 — 3906.2 μs	1100 — sec.
0101 — 7812.5 μs	1101 — min.
0110 — 15.625 ms	1110 — hour
0111 — 31.25 ms	1111 — day

TABLE II

Addresses	A2	A1	A0
Latch, Counter Seconds	0	1	0
Latch, Counter Minutes	0	1	1
Latch, Counter Hours	1	0	0
Counter, Day	1	0	1
Counter, Month	1	1	0
Control, Register	1	1	1
Status Register	1	1	1

MSB of hours counters (Bit 7) is an AM-PM bit. 0 = AM; 1 = PM.

Bit 6 of hours counter controls 12/24 hr. 1 = 12 hr: 0 = 24 hr.

Status Register: Bit 7 MSB = alarm
Interrupt Source: Bit 6 = clock

MSB of Month Counter (Bit 7) is a Leap Year Bit 0 = No, 1 = Yes.

CDP1879, CDP1879C-1

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C V_{DD} ± 5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1879			CDP1879C-1			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.•	Max.	Min.	Typ.•	Max.	
Quiescent Device Current I_{DD}		0, 5	5	—	0.01	50	—	0.02	200	µA
		0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink)	0.4	0, 5	5	1.8	4	—	—	—	—	mA
Current, Data Bus & $\overline{INT}$ I_{OL}	0.5	0, 10	10	3.6	7	—	—	—	—	
Output High Drive (Source)	4.6	0, 5	5	-1.1	-2.3	—	-1.1	-2.3	—	
Current, Data Bus & $\overline{INT}$ I_{OH}	9.5	0, 10	10	-2.6	-4.4	—	—	—	—	
Output Low Drive (Sink)	0.4	0, 5	5	0.6	1.4	—	0.6	1.4	—	
Current, Clock Out I_{OL}	0.5	0, 10	10	1.2	3	—	—	—	—	
Output High Drive (Source)	4.6	0, 5	5	-1.1	-2.3	—	-1.1	-2.3	—	
Current, Clock Out I_{OH}	9.5	0, 10	10	-2.6	-4.4	—	—	—	—	
Output Low Drive (Sink)	0.4	0, 5	5	0.2	0.9	—	0.2	0.9	—	
Current, $\overline{XTAL}$ Out I_{OL}	0.5	0, 10	10	0.4	2	—	—	—	—	
Output High Drive (Source)	4.6	0, 5	5	-0.15	-0.4		-0.15	-0.4	—	
Current, $\overline{XTAL}$ Out I_{OH}	9.5	0, 10	10	-0.3	-0.7	—	—	—	—	
Output Voltage	—	0, 5	5	—	0	0.1	—	0	0.1	V
Low-Level V_{OL}‡	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage	—	0, 5	5	4.9	5	—	4.9	5	—	
High Level V_{OH}‡	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	
Input Leakage Current I_{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	µA
		0, 10	10	—	—	±2	—	—	—	
3-State Output	0, 5	0 ,5	5	—	—	±1	—	—	±1	
Leakage Current I_{OUT}	0, 10	0, 10	10	—	—	±1	—	—	—	
Operating Current *										
External Clock 32 kHz	—	—	5	—	0.01	0.15	—	0.01	0.15	mA
1 MHz	—	—	5	—	0.2	1	—	0.2	1	
2 MHz	—	—	5	—	0.35	1.5	—	0.35	1.5	
4 MHz	—	—	5	—	0.7	2	—	0.7	2	
32 kHz	—	—	10	—	0.03	0.25	—	—	—	
1 MHz	—	—	10	—	0.4	2	—	—	—	
2 MHz	—	—	10	—	0.8	3	—	—	—	
4 MHz	—	—	10	—	1.6	4.5	—	—	—	
XTAL Oscillator** 32 kHz	—	—	5	—	0.1	0.25	—	0.1	0.25	
1 MHz	—	—	5	—	0.3	0.5	—	0.3	0.5	
2 MHz	—	—	5	—	0.4	0.6	—	0.4	0.6	
4 MHz	—	—	5	—	0.6	0.8	—	0.6	0.8	
1 MHz	—	—	10	—	1.6	3	—	—	—	
2 MHz	—	—	10	—	1.8	3.5	—	—	—	
4 MHz	—	—	10	—	2	5	—	—	—	
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	
Maximum Clock Rise t_r,t_f	—	—	5	—	—	10	—	—	10	µs
and Fall Times	—	—	10	—	—	1	—	—	—	

•Typical values are for T_A = 25° C and nominal V_{DD}.

‡I_{OL} = I_{OH} = 1 µA.

*Operating current measured with clockout = 488.2 µs and no load;

** See Table III and Fig. 6 for oscillator circuit information.

CDP1879, CDP1879C-1

PROGRAMMING MODEL

WRITE AND READ REGISTERS

BCD FORMAT

DB7	DB0
TENS 0-5	UNITS 0-9

SECONDS COUNTER (00-59)

DB7	DB0
TENS 0-5	UNITS 0-9

MINUTES COUNTER (00-59)

DB7	DB6		DB0
X	X	TENS 0-2	UNITS 0-9

HOURS COUNTER (01-12 or 00-23)
DB7 0=AM, 1=PM
DB6 0=24 HR, 1=12 HR

DB7	DB0
TENS 0-3	UNITS 0-9

DAY OF MONTH COUNTER
(01-28, 29, 30, 31)

DB7		DB0
X	TENS 0 or 1	UNITS 0-9

MONTH COUNTER

(JAN=1 DEC=12)
DB7 0=NO LEAP YEAR
1=LEAP YEAR

WRITE ONLY REGISTERS

DB7							DB0
7	6	5	4	3	2	1	0

CONTROL REGISTER

DB0-DB1 - FREQUENCY SELECT
DB2 - START/STOP
DB3 - COUNTER/ALARM LATCH CONTROL
DB4-DB7 - CLOCK OUTPUT SELECT

DB7	DB0
TENS 0-5	UNITS 0-9

SECONDS ALARM LATCH (00-59)

DB7	DB0
TENS 0-5	UNITS 0-9

MINUTES ALARM LATCH (00-59)

DB7	DB6		DB0
X	X	TENS 0-2	UNITS 0-9

HOURS ALARM LATCH (01-12 or 00-23)
12 HR, DB7=0 AM, 1=PM
24 HR, DB7=X

READ ONLY REGISTER

DB7	DB6						DB0
X	X	0	0	0	0	0	0

INTERRUPT STATUS REGISTER
DB7=1 ALARM CIRCUIT ACTIVATED $\overline{\text{INT}}$.
DB6=1 CLOCK OUTPUT ACTIVATED $\overline{\text{INT}}$.

REGISTER TRUTH TABLE

ADDRESS			ACTIVE SIGNAL		BIT 3 CONTROL REGISTER	REGISTER OPERATION
A2	A1	A0	TPB/$\overline{\text{WR}}$	$\overline{\text{RD}}$		
0	1	0	X	—	0	Write Seconds Counter
0	1	0	—	X	0	Read Seconds Counter
0	1	1	X	—	0	Write Minutes Counter
0	1	1	—	X	0	Read Minutes Counter
1	0	0	X	—	0	Write Hours Counter
1	0	0	—	X	0	Read Hours Counter
1	0	1	X	—	0	Write Date Counter
1	0	1	—	X	0	Read Date Counter
1	1	0	X	—	0	Write Month Counter
1	1	0	—	X	0	Read Month Counter
0	1	0	X	—	1	Write Seconds Alarm Latch
0	1	1	X	—	1	Write Minutes Alarm Latch
1	0	0	X	—	1	Write Hours Alarm Latch
1	1	1	X	—	—	Write Control Register
1	1	1	—	X	—	Read Int. Status Register

GENERAL OPERATION

The real-time clock contains seconds, minutes, and hours, date and month counters that hold time of day/calendar information (see Fig. 2). The frequency of an intrinsic oscillator is divided down to supply a once-a-second signal to the counter series string. The counters are separately addressable and can be written to or read from

The real-time clock contains seconds, minutes and hour write-only alarm latches that store the alarm time (see Fig. 3). When the value of the alarm latches and counters are equal, the interrupt output is activated. The interrupt output can also be activated by a clock output transition The clock output is derived from the prescaler and counters and can be one of 15 square-wave signals. The value in the read-only interrupt status register identifies the interrupt source

Operational control of the real-time clock is determined by the byte in a write-only control register. The 8-bit value in this register determines the correct divisor for the prescaler, a data direction and alarm enable bit, clock output select, and start/stop control (see Fig. 4).

Data transfer and addressing are accomplished in two modes of operation, memory mapping and I/O mapping using the CDP1800-series microprocessors. The mode is selected by the level on an input pin. (I-O/$\overline{\text{MEM}}$). Memory mapping implies use of the address lines as chip selects and address inputs using linear selection or partial or full decoding methods. I/O mapping with the CDP1800-series microprocessors involves use of the N line outputs in conjunction with input and output instructions to transfer data to and from memory.

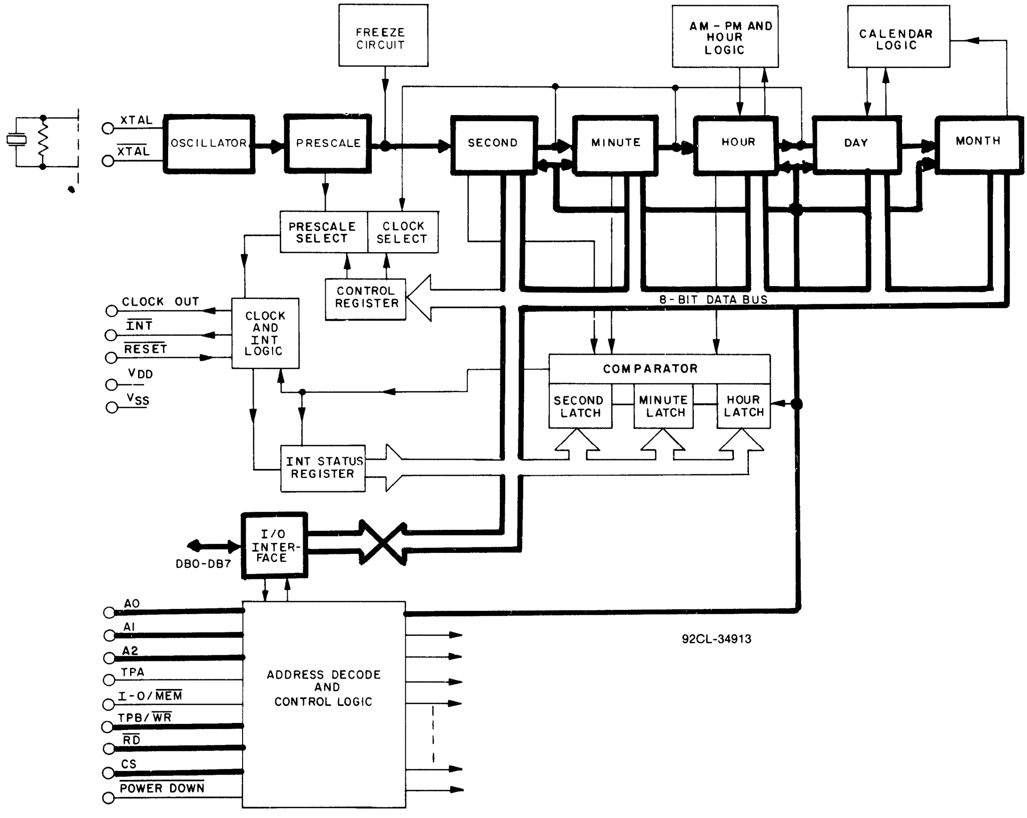


Fig. 2 - Functional diagram - time counters highlighted.

CDP1879, CDP1879C-1

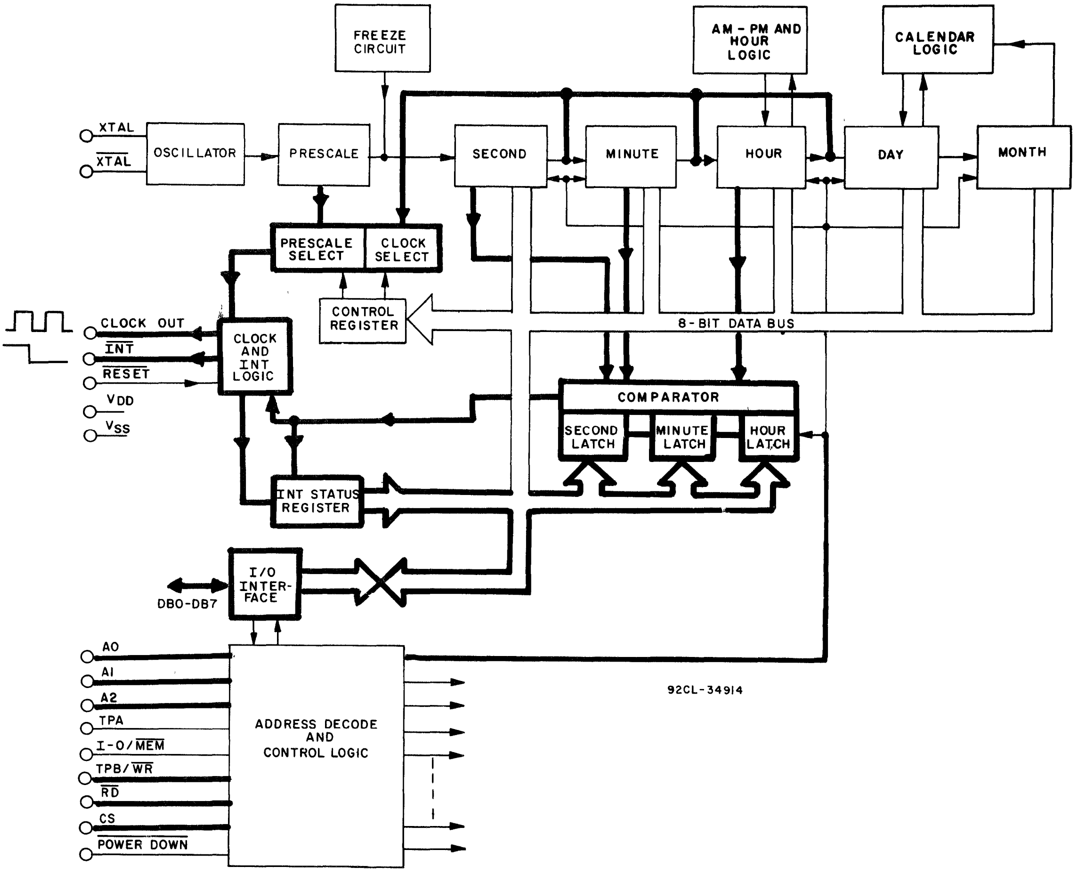


Fig. 3 - Functional diagram - alarm circuit, clock output, interrupt, and status registers highlighted

OPERATIONAL SEQUENCE

Power is applied and the real-time clock is reset. This sets the interrupt output pin high. After the CS pin is set high and with address 7 on the address input lines, the control register is loaded via the data bus to configure the clock.

With selective addressing, the seconds through month counters are then written to and loaded to set the current time. The real-time clock will now hold the current "wall clock" time, with an accuracy determined by the crystal or external clock used. If the alarm function is desired, the control register is accessed and loaded again. This new byte will allow subsequent time data to be entered into the seconds, minutes and hours alarm latches. This sequence is also used when selecting one of the 15 available clock-out signals.

If the alarm function was selected, the interrupt output pin will be set low when the values in the seconds, minutes and hour alarm latches match those in the seconds, minutes and hour counters.

If one of the 15 sub second-to-day clock outputs is selected by the byte in the control register, the clock output pin toggles at that frequency (50% duty cycle). The interrupt output will also be set low on the first clock out negative transition. The interrupt source (alarm or clock out) can be determined by reading the interrupt status register. The clock output can be deselected by placing zero in the upper nibble of the control register if the alarm function is selected as the only interrupt source.

COUNTERS (See Fig. 2)

The counter section consists of an on-board oscillator, a prescaler and 5 counters that hold the time of day/calendar information.

1 of 4 possible external crystals determine the frequency of the on-board oscillator (32,768 Hz, 1.048576 MHz, 2.097152 MHz, 4.194304 MHz). The oscillator output is divided down by a prescaler that supplies a once-a-second pulse to the counters. The seconds counter divides the pulse by 60 and its output clocks the minute counter every 60 seconds. Further division by the minutes, hours, day of month and month counters result in 5 counters holding data that reflects the time/calendar from seconds to months. The counters are addressed separately and BCD data is transferred to and from via the data bus. The most significant

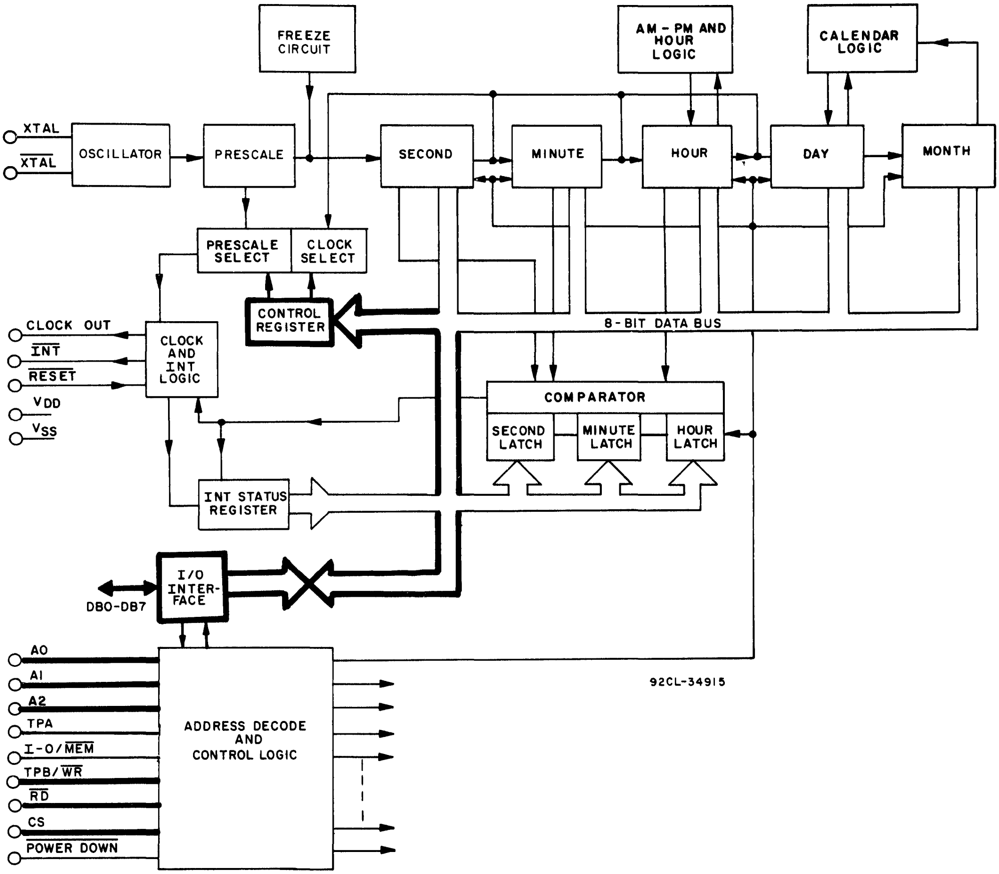


Fig. 4 - Functional diagram - control register highlighted.

bit of the hours counter (Bit 7) is user programmed to indicate AM or PM and will be inverted every 12th hour. (0 = AM, 1 = PM). Bit 6 of the hours counter is user programmed to enable the hours counter for 12 or 24 hour operation. (0 = 24, 1 = 12). If 24-hour operation is selected, the AM-PM bit is "don't care", but still toggles every 12th hour. Writing to the seconds counter resets the last 7 stages of the prescaler, allowing time accuracy to approximately 1/100 of a second.

The most significant bit of the month counter is a Leap Year bit. If it is set to "1", the counter will count to February 29, then roll to March 1. If set to "0" it will go to March 1st after February 28th.

ALARM AND INTERRUPT STATUS REGISTER (See Fig. 3)

The alarm circuit consists of 1) seconds, minutes and hour alarm latches that hold the alarm time, 2) the outputs of the seconds, minutes and hour counters, and 3) a comparator that drives an interrupt output. The comparator senses the counter and alarm latch values and activates the interrupt output (active low) when they are equal.

The write-only alarm latches have the same addresses as their comparable counters. Bit 3 in the control register determines data direction to the latches or counters and alarm enabling. For example, during a write cycle, if bit 3 in the control register is a "1", addressing the seconds counter or alarm latch will load the seconds alarm latch from the data bus and will enable the alarm function. Conversely, if bit 3 in the control register is a "0", addressing the seconds counter or alarm latch during a write cycle will place the value on the data bus into the seconds counter and will disable the alarm function. The interrupt output can be activated by the alarm circuit or the clock output. When an interrupt occurs, the upper two bits of the interrupt status register identify the interrupt source. The interrupt status register has the same address as the control register. Addressing the interrupt status register with the RD line active will place these register bits on the data bus. Bits 0-5 are held low. A "1" in bit 6 represents a clock output transition as the interrupt source. A "1" in bit 7 will identify the alarm circuit as the interrupt source.

Activating the reset pin (active low) resets the hour latch to "30" which prevents a match between alarm and time registers during an initialization procedure. Activating the reset pin or writing to the control register resets the interrupt output (high) and clears the interrupt status register.

CDP1879, CDP1879C-1

CLOCK OUTPUT (See Table I and Fig. 3)

One of 15 counter and prescaler overflows can be selected as a 50% duty cycle output signal that is available at the "clock out" pin. The frequency is selected by the upper nibble in the control register. For example, selecting a one-second clock output will result in a repetitive signal that will be high for 500 ms and low for the same period. The high-to-low transition of the output signal will set the clock bit in the status register and activate the interrupt output. The level of the "clock out" signal is derived from the value in the counter. Example: if hours clock is selected and the minutes counter holds 4 minutes, the clock out will be low for 26 minutes and high for 30 minutes. Thereafter, the clock out will toggle at a 50% duty cycle rate.

CONTROL REGISTER (See Table I and Fig. 4)

BIT BIT

7	6	5	4	3	2	1	0

CONTROL REGISTER BYTE

The 8-bit value in the control register determines the following:

1. **Bit 0 and 1 — Frequency Select** — Since there are one of 4 possible crystals the oscillator in the real-time clock can operate with, these bit levels determine the prescaler divisor so that an accurate one second pulse is supplied to the counter series string.

BIT 1	BIT 0	FREQUENCY
0	0	32,768 Hz
0	1	1.048576 MHz
1	0	2.097152 MHz
1	1	4.194304 MHz

2. **Bit 2 — Start-Stop Control** — Counter enabling is controlled by the value at this location. A "1" will allow the counters to function and a "0" in this location will disable the counters.
3. **Bit 3 — Counter/Latch Control** — The level at this location controls two functions. It is required since the counters and alarm latches have the same addresses.
    1) A "0" in bit 3 will direct subsequent data to or from the counter selected and the alarm function will be disabled.
    2) A "1" in bit 3 will direct subsequent data to or from the alarm latch and will enable the alarm.
4. **Bits 4 to 7 — Clock Select** — These bits select one of 15 square-wave signals that will be present at the "clock-out" pin. If bits 4 to 7 are zero's, the clock output pin will be high. If a clock is selected, the first high-to-low clock out transition will activate the interrupt pin (active low) and place a "1" in bit 6 of the status register. Writing to the control register or activating the reset pin will set the interrupt pin high and reset the interrupt status register.

Normal operation requires the control register to be written to and loaded first with a control word. However, subsequent writing to a counter if a "clock out" is selected may cause an interrupt out signal. Therefore, "clock-out" should be deselected by writing zero's into bits 4 through 7 if the interrupt is used. When the counters are loaded, the control register is again written to with the value in the upper nibble selecting the "clock out" signal. See Table I.

READ AND WRITE SIGNALS

When the I-O/MEM pin is low, the real-time clock is enabled for memory mapped operation. Data on the bus is placed in, or read from a counter, alarm latch or register by 1) placing the CS pin high, 2) selective addressing, 3) placing the TPB/WR pin low during a write cycle with the RD pin high or 4) setting the RD pin low during a read cycle with the TPB/WR pin high.

The I/O mapping mode used with the CDP1800 series microprocessor is selected by setting the I-O/MEM pin high. The TPB/WR pin on the real-time clock is connected to the TPB output pin of the microprocessor. Data on the bus is written to or read from the counters, latches and registers by 1) placing the CS pin high, 2) selective addressing utilizing the microprocessor N lines and I/O instructions, 3) placing the TPB/WR pin high with the RD pin low during an output or write operation (data is latched on TPB's trailing edge), 4) setting the RD line high during an input or read operation. Data is placed on the bus by the real-time clock between the trailing edges of TPA and TPB.

FREEZE CIRCUIT

Since writing to or reading from the counters or alarm latches is performed asynchronously, the once-a-second signal from the prescaler may pulse the counter series string during these operations. This can result in erroneous data. To avoid this occurring, a transparent "freeze" circuit is incorporated into the real-time clock. This circuit is designed to trap and hold the one-second input clock transition if it occurs during access times. When the operations are completed, it is inserted into the counter series string. To utilize the "freeze" circuit, address "1" (A0 = 1, A1 = 0, A2 = 0) is selected first while performing a write operation. Read or write accesses may now be performed with assurance the data is stable. All operations must be concluded within 250 ms of the address "1" access. If memory mapping any dummy write operation after selecting address "1" will set the "freeze" circuit. If using the I/O mode, a 61 output instruction will perform the same function. There is no time restriction on subsequent accesses as long as the read or write operations are preceded by selecting address "1".

POWER DOWN

Power down operation is initiated with a low signal on the "POWER DOWN" input pin. In conjunction with the interrupt output, it is used to supply external control circuits with a 3 level control signal. The operating current is not appreciably reduced during "POWER DOWN" operation. When power down is initiated, any inputs on the address or data bus are ignored. The clock output is set low. The interrupt output is tri-stated. If enabled previously, the alarm circuitry is active and will set the interrupt output pin low when alarm time occurs. The interrupt output will also go low if a clock was selected and an internal high-to-low transition occurs during power down. The clock output pin will remain low. If power down is initiated in the middle of a read or write sequence, it will not become activated until the read or write cycle is completed.

PIN FUNCTIONS

V_{DD}, V_{SS} — Power and ground for device.

DB0 — DB7 — DATA BUS — 8-bit bidirectional bus that transfers BCD data to and from the counters, latches and registers.

A0, A1, A2 — Address inputs that select a counter, latch or register to read from or write to.

TPA — Strobe input used to latch the value on the chip select pin. CS is latched on the trailing edge of TPA. During memory mapping, it is used to latch the high order address bit used for the chip select. When the real-time clock is used with other microprocessors, or when the high order address of the CDP1800 series microprocessor is externally latched, it is connected to V_{DD}. In the input/output mode, it is used to gate the N lines.

I-O/$\overline{\text{MEM}}$ — Tied low during memory mapping and high when the input/output mode of the CDP1800 series microprocessor is used.

$\overline{\text{RD}}$, TPB/$\overline{\text{WR}}$ — DIRECTION SIGNALS — Active signals that determine data direction flow. In the memory mapped mode, data is placed on the bus from the counters or status register when $\overline{\text{RD}}$ pin is active.

Data is transferred to a counter, latch or the control register when $\overline{\text{RD}}$ is high and TPB/$\overline{\text{WR}}$ is active and latched on the trailing edge (low to high) of the TPB/$\overline{\text{WR}}$ signal.

In the input/output mode, data is placed on the bus from a counter or status register when $\overline{\text{RD}}$ is not active between the trailing edges of TPA and TPB. Data on the bus is written to a counter, latch, or the control register during TPB when $\overline{\text{RD}}$ is active and latched on TPB's trailing edge. The following connections are required between the microprocessor and real-time clock in the CDP1800 series I/O mode.

MICROPROCESSOR	REAL-TIME CLOCK
$\overline{\text{MRD}}$	$\overline{\text{RD}}$
TPB	TPB/$\overline{\text{WR}}$
TPA	TPA
N LINES	ADDRESS LINES
I-O/$\overline{\text{MEM}}$	V_{DD}

CS — CHIP SELECT — Used to enable or disable the inputs and outputs. TPA is used to strobe and latch a positive level on this pin to enable the device.

XTAL AND $\overline{\text{XTAL}}$ — The frequency of the internal oscillator is determined by the value of the crystal connected to these pins. "XTAL" may be driven directly by an external frequency source.

CLOCK OUT — 1 of 15 square wave frequencies will appear at this pin when selected. During power down, this pin will be placed low, and will be high during normal operation when the clock is deselected.

$\overline{\text{POWER DOWN}}$ — POWER DOWN CONTROL — A low on this pin will place the device in the power down mode.

$\overline{\text{INT}}$ — Interrupt Output — A low on this pin indicates an active alarm time or high-to-low transition of the "clock out" signal.

$\overline{\text{RESET}}$ — A low on this pin clears the status register and places the interrupt output pin high.

FREQUENCY INPUT REQUIREMENTS

The Real-Time Clock operates with the following frequency input sources:

1. An external crystal that is used with the on-board oscillator. The oscillator is biased by a large feedback resistor and oscillates at the crystal frequency (see Fig. 6, Table III).
2. An external frequency input that is supplied at the XTAL input. $\overline{\text{XTAL}}$ is left open (see Fig. 5). A typical external oscillator circuit is shown in Fig. 7 in section, "Standby (Timekeeping) VOLTAGE OPERATION".

TABLE III - Typical Oscillator Circuit Parameters for Suggested Oscillator Circuit, see Fig. 6

PARAMETERS	4.197 MHz	2.097 MHz	1.049 MHz	32768 Hz*	UNITS
R_f	22	22	22	22	MΩ
C_O	39	39	39	39	pF
C_I	5	5	5	5	pF
R_S	—	—	—	200	KΩ
C_L	—	—	—	91	pF
Crystal Impedance	73	200	200	50K (max.)	Ω

*CDP1879C-1 only

FREQUENCY INPUT REQUIREMENTS (Cont'd)

Design Considerations for Stable Crystal Oscillation

1. Stray capacitances should be minimized for best oscillator performance. Circuit board traces should be kept to a maximum of 1 inch, and there should be no parallel traces.
2. A signal line or power source line must not cross or go near the oscillator circuit line.
3. It is advisable to put a 0.1-microfarad capacitor between VDD and VSS of the CDP1879.

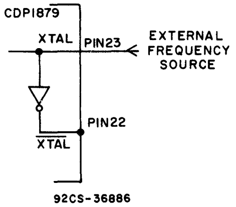


Fig. 5 - Connections for an external-frequency source applied to real-time clock.

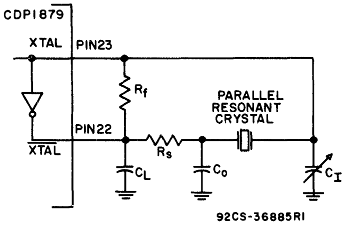


Fig. 6 - Suggested oscillator circuit applied to real-time clock (see Table III).

STANDBY (TIMEKEEPING) VOLTAGE OPERATION

When any one of the four specified crystals is used with the on-board oscillator, the Real-Time Clock can operate at a minimum of 4 volts VDD. However, at 32 kHz the clock will run (timekeeping only, no device READ/WRITE accesses) down to 3 volts at -40° to +85° C and 2.5 volts at 0° to +70° C. To achieve this low voltage operation, an external 32-kHz clock source must be supplied at the XTAL input (see Fig. 7). The standby requirements for CHIP SELECT/DESELECT are listed in Table IV, and Fig. 8 indicates the timing waveforms. Fig. 9 illustrates the typical timekeeping curve over the full temperature range.

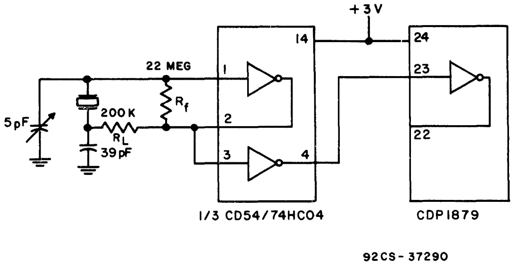


Fig. 7 - Typical external clock-source circuit.

Table IV - Standby (Timekeeping) Characteristics at Full-Temperature Range

CHARACTERISTIC		VDD (V)	VSTBY (V)	LIMITS				UNITS
				CDP1879		CDP1879C-1		
				Min.	Max.	Min.	Max.	
Chip Deselect to Standby (Timekeeping) Voltage Time	tCSTBY	5	2.5, 3	2	—	2	—	µs
		10	2.5, 3	1	—	—	—	
Recovery to Normal Operation Time	tRC	5	2.5, 3	2	—	2	—	
		10	2.5, 3	1	—	—	—	

STANDBY (TIMEKEEPING) VOLTAGE OPERATION (Cont'd)

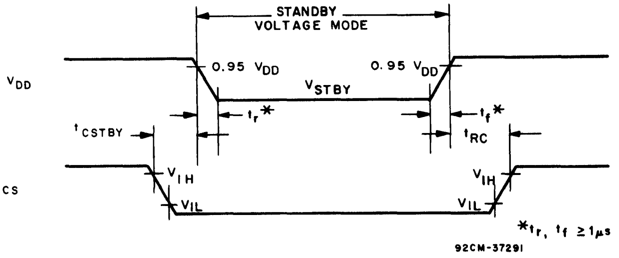


Fig. 8 - Standby (timekeeping) voltage- and timing-waveforms.

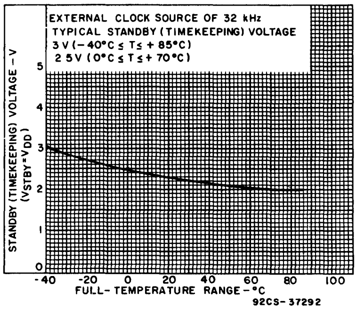


Fig. 9 - Typical standby (timekeeping) voltage vs. full-temperature range.

APPLICATIONS

A typical application for this real-time clock is as a wake-up control to a CPU to reduce total system power in intermittent-use systems. A hookup diagram illustrating this feature is shown in Fig. 10. In this configuration, the alarm and power-down features of the CDP1879 are utilized in the control of the sleep and wake-up states of the CPU. A typical shut-down/start-up sequence for this system could proceed as follows:

1. The CPU has finished a current task and will be inactive for the next six hours.
2. The CPU loads the CDP1879 alarm registers with the desired wake-up time.
3. The CDP1800 Q output is set high, which stops the CPU oscillator (as an alternative, in an NMOS system, power to all components except the clock chip could be shut off).
4. This Q output signal is received by the CDP1879 as a power-down signal.
5. The CDP1879 tri-states the interrupt output pin.
6. The CDP1879 eventually times out, and sets an alarm by driving the $\overline{\text{INT}}$ output low.
7. The alarm signal resets the CPU (to avoid oscillator start-up problems) and flags the processor for a warm-start routine.
8. The CPU, once into its normal software sequence, writes to the CDP1879 control register to reset the interrupt request.

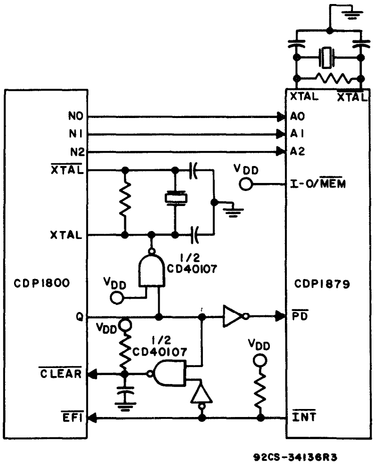


Fig. 10 - CPU wake-up circuit using the CDP1879 real-time clock.

CDP1879, CDP1879C-1

APPLICATIONS (Cont'd)

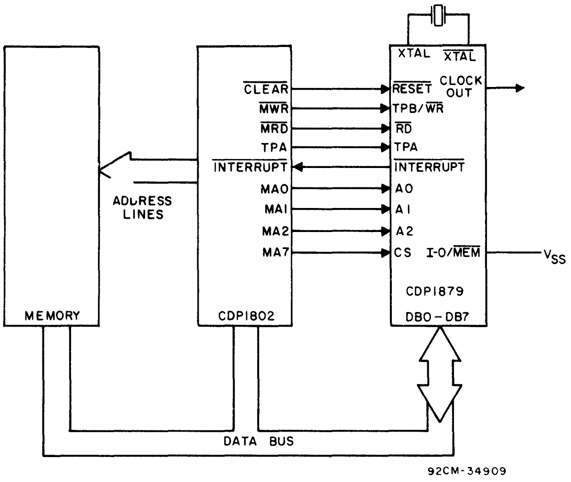


Fig. 11 - Typical CDP1802 memory-mapped system.

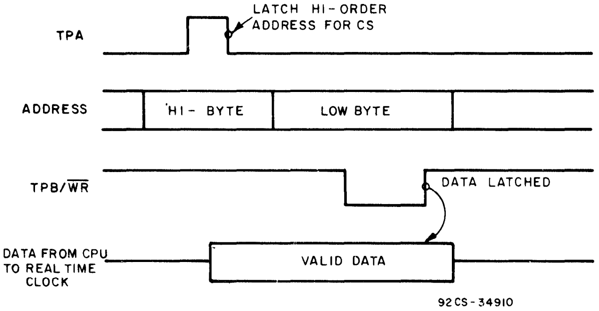


Fig. 12 - CDP1800-series memory-mapped write-cycle timing waveforms.

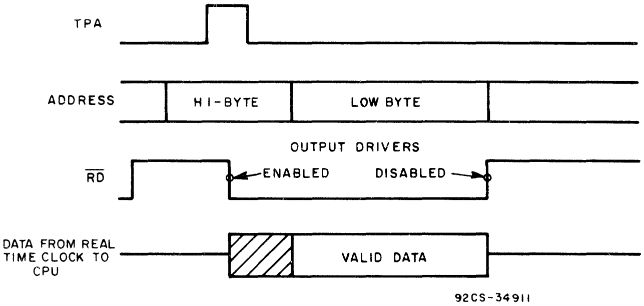
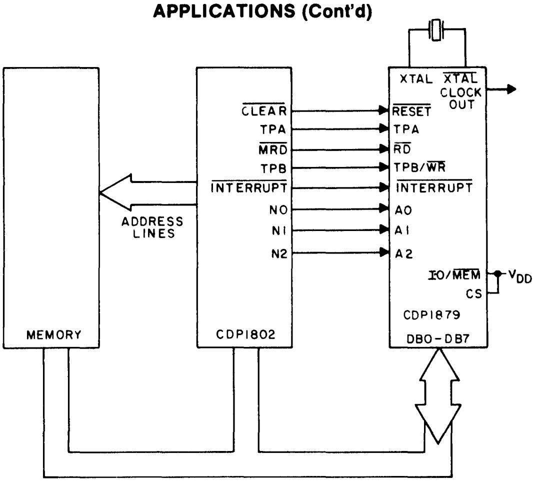


Fig. 13 - CDP1800-series memory-mapped read-cycle timing waveforms.

APPLICATIONS (Cont'd)



92CM-34905

Fig. 14 - Typical CDP1802 input/output-mapped system.

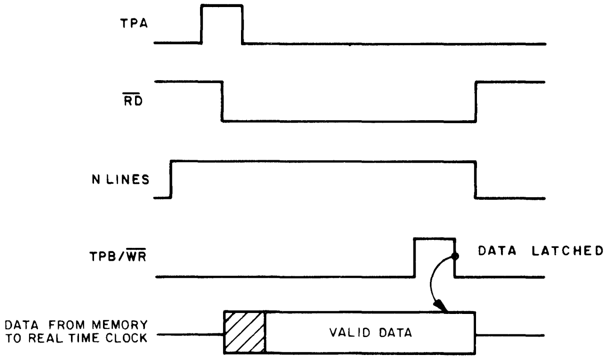


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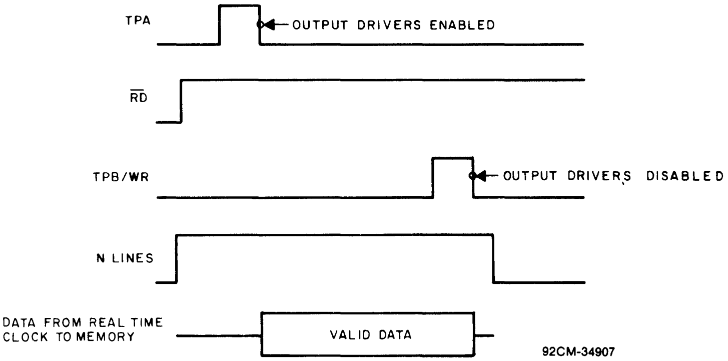
Fig. 15 - CDP1800-series input/output-mapping timing waveforms with output instruction



92CM-34907

Fig. 16 - CDP1800-series input/output-mapping timing waveforms with input instruction

CDP1879, CDP1879C-1

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C,
Input t_r, t_f = 10 ns, C_L = 50 pF

CHARACTERISTIC Read Cycle Times (see Fig. 17)		V_{DD} (V)	LIMITS				UNITS
			CDP1879		CDP1879C-1		
			Min.†	Max.	Min.†	Max.	
Data Access from Address	t_{DA}	5 10	— —	400 190	— —	400 —	ns
$\overline{\text{Read}}$ Pulse Width	t_{RD}	5 10	270 160	— —	270 —	— —	
Data Access from $\overline{\text{Read}}$	t_{DR}	5 10	— —	375 170	— —	375 —	
Address Hold after $\overline{\text{Read}}$	t_{RH}	5 10	0 0	— —	0 —	— —	
Output Hold after $\overline{\text{Read}}$	t_{DH}	5 10	50 40	230 130	50 —	230 —	
Chip Select Setup to TPA	t_{CS}	5 10	50 30	— —	50 —	— —	

†Time required by a limit device to allow for the indicated function

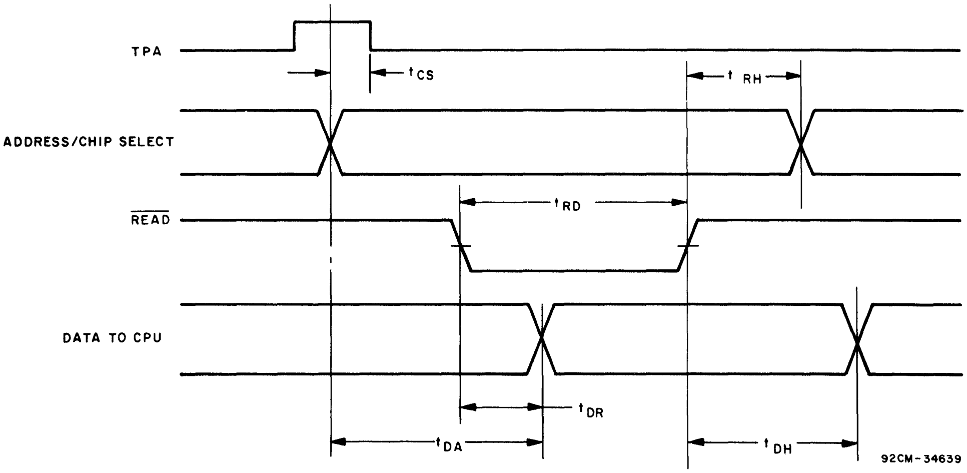


Fig. 17 - Read-cycle timing waveforms.

CDP1879, CDP1879C-1

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, Input t_r, t_f = 10 ns, C_L = 50 pF

CHARACTERISTIC Write Cycle Times (see Fig. 18)		V_{DD} (V)	LIMITS				UNITS
			CDP1879		CDP1879C-1		
			Min.†	Max.	Min.†	Max.	
Address Setup to $\overline{\text{Write}}$	t_{AS}	5	225	—	225	—	ns
		10	110	—	—	—	
$\overline{\text{Write}}$ Pulse Width	t_{WR}	5	150	—	150	—	
		10	70	—	—	—	
Data Setup to $\overline{\text{Write}}$	t_{DS}	5	65	—	65	—	
		10	30	—	—	—	
Address Hold after $\overline{\text{Write}}$	t_{AH}	5	0	—	0	—	
		10	0	—	—	—	
Data Hold after $\overline{\text{Write}}$	t_{WH}	5	150	—	150	—	
		10	80	—	—	—	
Chip Select Setup to TPA	t_{CS}	5	50	—	50	—	
		10	30	—	—	—	

†Time required by a limit device to allow for the indicated function.

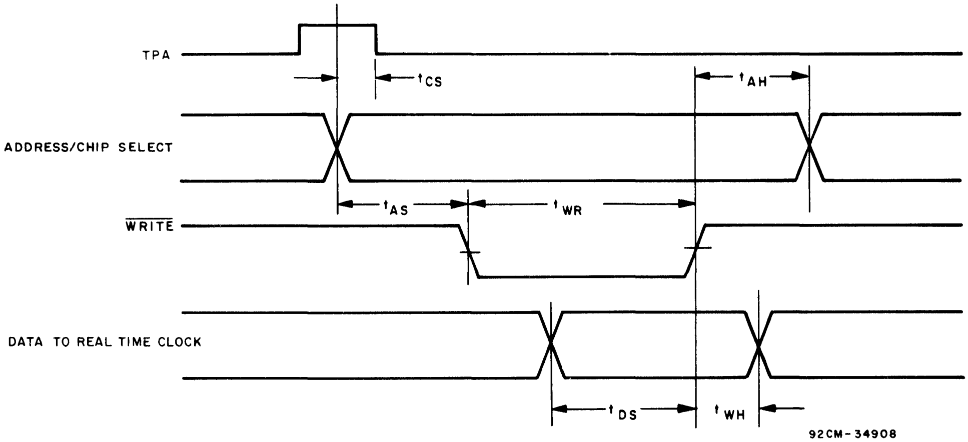
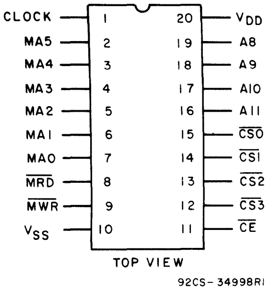


Fig. 18 - Write-cycle timing waveforms.

CDP1881, CDP1881C,
CDP1882, CDP1882C

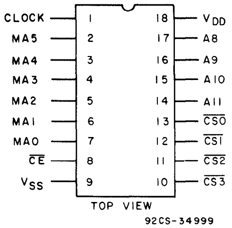


CDP1881, CDP1881C
TERMINAL ASSIGNMENT

CMOS 6-Bit Latch and Decoder Memory Interfaces

Features

- *Performs memory address latch and decoder functions multiplexed or non-multiplexed*
- *Decodes up to 16 K-bytes of memory*
- *Interfaces directly with CDP1800-series microprocessors at maximum clock frequency*
- *Can replace existing CDP1866 and CDP1867 (upward speed and function capability)*



CDP1882, CDP1882C
TERMINAL ASSIGNMENT

The RCA-CDP1881 and CDP1882 are CMOS 6-bit memory latch and decoder circuits intended for use in CDP1800 series microprocessor systems. They can interface directly with the multiplexed address bus of this system at maximum clock frequency, and up to four 4K x 8-bit memories to provide a 16K-byte memory system. With four 2K x 8-bit memories an 8K-byte system can be decoded.

The devices are also compatible with non-multiplexed address bus microprocessors. By connecting the clock input to V_{DD}, the latches are in the data-following mode and the decoded outputs can be used in general-purpose memory-system applications.

The CDP1881 and CDP1882 are intended for use with 2K or 4K-byte RAMs and are identical except that in the CDP1882 $\overline{MWR}$ and $\overline{MRD}$ are excluded.

The CDP1881 and CDP1882 are functionally identical to the CDP1881C and the CDP1882C. They differ in that the CDP1881 and CDP1882 have a recommended operating voltage range of 4 to 10 5 volts and their C versions have a recommended operating voltage range of 4 to 6.5 volts.

The CDP1881 and CDP1882 are supplied in 20-lead and 18-lead packages, respectively. The CDP1881 is supplied only in a dual-in-line plastic package (E suffix). The CDP1882 is supplied in dual-in-line, hermetic side-brazed ceramic (D suffix) and in plastic (E suffix) packages.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltage referenced to V_{SS} terminal)	
CDP1881 and CDP1882	-0.5 to +11 V
CDP1881C and CDP1882C	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0 5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 12 mW/° C to 200 mW
For T_A -55 to +100° C (PACKAGE TYPE D)	500 mW
For T_A = +100 to 125° C (PACKAGE TYPE D)	Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125° C
PACKAGE TYPE E	-40 to +85° C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max	+265° C

File Number **1367**

CDP1881, CDP1881C, CDP1882, CDP1882C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range.
For maximum relibility, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1881, CDP1882		CDP1881C, CDP1882C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1881 CDP1882			CDP1881C CDP1882C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current I_{DD}	—	0, 5	5	—	1	10	—	5	50	μA
	—	0, 10	10	—	10	100	—	—	—	
Output Low Drive (Sink) Current I_{OL}	0.4	0,5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0, 10	10	3.2	6.4	—	—	—	—	
Output High Drive (Source) Current I_{OH}	4.6	0, 5	5	-1.15	-2.3	—	-1.15	-2.3	—	
	9.5	0, 10	10	-2.3	-4.6	—	—	—	—	
Output Voltage Low-Level V_{OL}‡	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High-Level V_{OH}‡	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	
	1, 9	—	10	—	—	3	—	—	—	
Input High Voltage V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	
	1, 9	—	10	7	—	—	—	—	—	
Input Leakage Current I_{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	μA
		0, 10	10	—	—	±2	—	—	—	
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current I_{DD1} Δ	0, 5	0, 5	5	—	—	2	—	—	2	mA
	0, 10	0, 10	10	—	—	4	—	—	—	
Minimum Data Retention Voltage V_{DR}	V_{DD} = V_{DR}			—	2	2.4	—	2	2.4	V
Data Retention Current I_{DR}	V_{DD} = 2.4 V			—	0.01	1	—	0.5	5	μA

*Typical values are for T_A = 25° C

‡I_{OL} = I_{OH} = 1 μA

ΔOperating current is measured at 200 kHz for V_{DD} = 5 V and 400 kHz for V_{DD} = 10 V, with outputs open circuit. (Equivalent to typical CDP1800 system at 3.2 MHz, 5-V; and 6.4 MHz, 10-V).

CDP1881, CDP1881C, CDP1882, CDP1882C

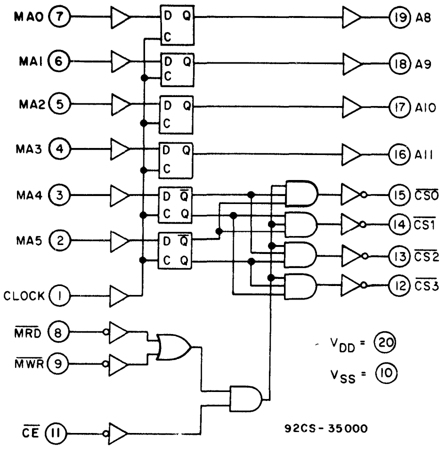

MA0 7
MA1 6
MA2 5
MA3 4
MA4 3
MA5 2
CLOCK 1
$\overline{\mathrm{MRD}}$ 8
$\overline{\mathrm{MWR}}$ 9
$\overline{\mathrm{CE}}$ 11
D Q C
D $\overline{\mathrm{Q}}$ C Q
19 A8
18 A9
17 A10
16 A11
15 $\overline{\mathrm{CS0}}$
14 $\overline{\mathrm{CS1}}$
13 $\overline{\mathrm{CS2}}$
12 $\overline{\mathrm{CS3}}$
V_{DD} = 20
V_{SS} = 10
92CS-35000

Fig. 1 - Functional diagram for the CDP1881, CDP1881C.

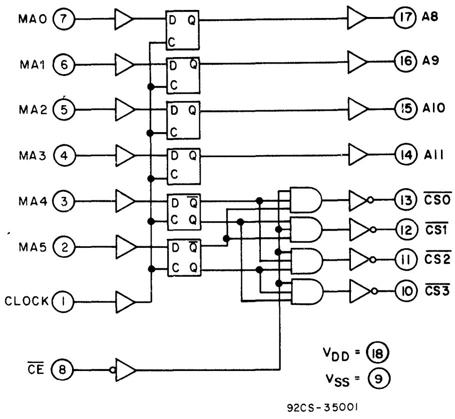

MA0 7
MA1 6
MA2 5
MA3 4
MA4 3
MA5 2
CLOCK 1
$\overline{\mathrm{CE}}$ 8
D Q C
D $\overline{\mathrm{Q}}$ C Q
17 A8
16 A9
15 A10
14 A11
13 $\overline{\mathrm{CS0}}$
12 $\overline{\mathrm{CS1}}$
11 $\overline{\mathrm{CS2}}$
10 $\overline{\mathrm{CS3}}$
V_{DD} = 18
V_{SS} = 9
92CS-35001

Fig. 2 - Functional diagram for the CDP1882, CDP1882C.

TRUTH TABLES for the CDP1881, CDP1881C and CDP1882, CDP1882C.

INPUTS						OUTPUTS			
$\overline{\mathrm{MWR}}$Δ	$\overline{\mathrm{MRD}}$Δ	$\overline{\mathrm{CE}}$	CLK	MA4	MA5	$\overline{\mathrm{CS0}}$	$\overline{\mathrm{CS1}}$	$\overline{\mathrm{CS2}}$	$\overline{\mathrm{CS3}}$
1	1	X	X	X	X	1	1	1	1
X	X	1	X	X	X	1	1	1	1
0	X	0	1	0	0	0	1	1	1
0	X	0	1	1	0	1	0	1	1
0	X	0	1	0	1	1	1	0	1
0	X	0	1	1	1	1	1	1	0
0	X	0	0	X	X	PREVIOUS STATE			
X	0	0	1	0	0	0	1	1	1
X	0	0	1	1	0	1	0	1	1
X	0	0	1	0	1	1	1	0	1
X	0	0	1	1	1	1	1	1	0
X	0	0	0	X	X	PREVIOUS STATE			

ΔCDP1881, CDP1881C Only

INPUTS			OUTPUTS
$\overline{\mathrm{CE}}$	CLK	MA0, MA1, MA2, MA3	A8, A9, A10, A11
X	1	1	1
X	1	0	0
X	0	X	PREVIOUS STATE

Logic 1 = High, Logic 0 = Low, X = Don't Care

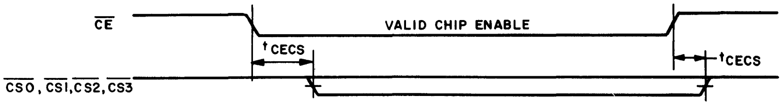
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF, See Fig. 3.

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1881, CDP1882			CDP1881C, CDP1882C			
			Min.	Typ.•	Max.Δ	Min.	Typ.•	Max.Δ	
Minimum Setup Time, Memory Address to CLOCK,	t_{MACL}	5	—	10	35	—	10	35	ns
		10	—	8	25	—	—	—	
Minimum Hold Time, Memory Address After CLOCK,	t_{CLMA}	5	—	8	25	—	8	25	
		10	—	8	25	—	—	—	
Minimum CLOCK Pulse Width	t_{CLCL}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Propagation Delay Times: $\overline{\text{Chip Enable}}$ to $\overline{\text{Chip Select}}$	t_{CECS}	5	—	75	150	—	75	150	
		10	—	45	100	—	—	—	
$\overline{\text{MRD}}$ or $\overline{\text{MWR}}$ to $\overline{\text{Chip Select}}$*	t_{MCS}	5	—	75	150	—	75	150	
		10	—	40	100	—	—	—	
CLOCK to $\overline{\text{Chip Select}}$	t_{CLCS}	5	—	100	175	—	100	175	
		10	—	65	125	—	—	—	
CLOCK to Address	t_{CLA}	5	—	100	175	—	100	175	
		10	—	65	125	—	—	—	
Memory Address to $\overline{\text{Chip Select}}$	t_{MACS}	5	—	100	175	—	100	175	
		10	—	75	125	—	—	—	
Memory Address to Address	t_{MAA}	5	—	80	125	—	80	125	
		10	—	40	60	—	—	—	

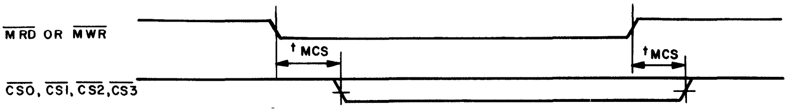
•Typical values are for T_A = 25° C.

ΔMaximum limits of minimum characteristics are the values above which all devices function.

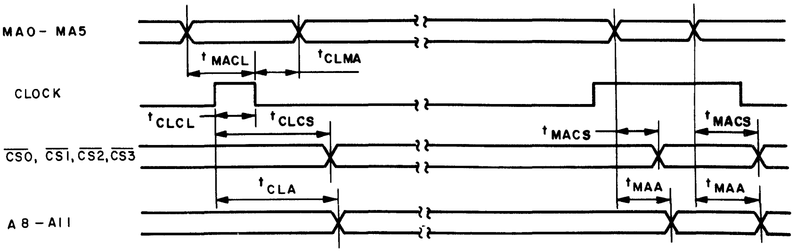
*For the CDP1881 and CDP1881C types only.



(a) CHIP ENABLE TO CHIP SELECT PROPAGATION DELAY



(b) MRD OR MWR TO CHIP SELECT PROPAGATION DELAY (CDP1881, CDP1881C ONLY)



(c) MEMORY ADDRESS SETUP AND HOLD TIME

92CM-37295

Fig. 3 - CDP1881 and CDP1882 timing waveforms.

CDP1881, CDP1881C, CDP1882, CDP1882C

SIGNAL DESCRIPTIONS/PIN FUNCTIONS

CLOCK: Latch-Input Control - a high at the clock input will allow data to pass through the latch to the output pin. Data is latched on the high to low transition of the clock input. This input is connected to TPA in CDP1800-series systems.

MA0-MA3: Address inputs to the high-byte address latches.

MA4, MA5: High-byte address inputs decoded to produce chip selects $\overline{\text{CS0}}$ - $\overline{\text{CS3}}$.

$\overline{\text{MRD}}$, $\overline{\text{MWR}}$: MEMORY READ ($\overline{\text{MRD}}$) and MEMORY WRITE ($\overline{\text{MWR}}$) signal inputs on the CDP1881, CDP1881C A low at either input, when the $\overline{\text{CE}}$ pin is low, will enable the decoder chip select outputs ($\overline{\text{CS0}}$ - $\overline{\text{CS3}}$).

$\overline{\text{CE}}$: CHIP ENABLE input - a low at the $\overline{\text{CE}}$ input of CDP1882, CDP1882C will enable the chip select decoder A low at the $\overline{\text{CE}}$ input of CDP1881, CDP1881C, coincident with a low at either the $\overline{\text{MRD}}$ or $\overline{\text{MWR}}$ pin, will enable the chip select decoder A high on this pin forces $\overline{\text{CS0}}$, $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, and $\overline{\text{CS3}}$ to a high (false) state.

A8-A11: Latched high-byte address outputs.

$\overline{\text{CS0}}$-$\overline{\text{CS3}}$: One of four latched and decoded Chip Select outputs.

VDD, VSS: Power and ground pins, respectively.

APPLICATION INFORMATION

The CDP1881 and CDP1882 can interface directly with the multiplexed address bus of the CDP1800-series microprocessor family at maximum clock frequency. A single CDP1881 or CDP1882 is capable of decoding up to 16K-bytes of memory.

The CDP1881 is provided with $\overline{\text{MRD}}$ and $\overline{\text{MWR}}$ inputs for controlling bus contention, and is especially useful for interfacing with RAMs that do not have an output enable function ($\overline{\text{OE}}$). Fig. 4 shows the CDP1881 in a minimum system configuration which includes the CDP1833 ROM (1K x 8) and two 2K x 8 RAMS. The CDP1881, in this example performs the following functions:

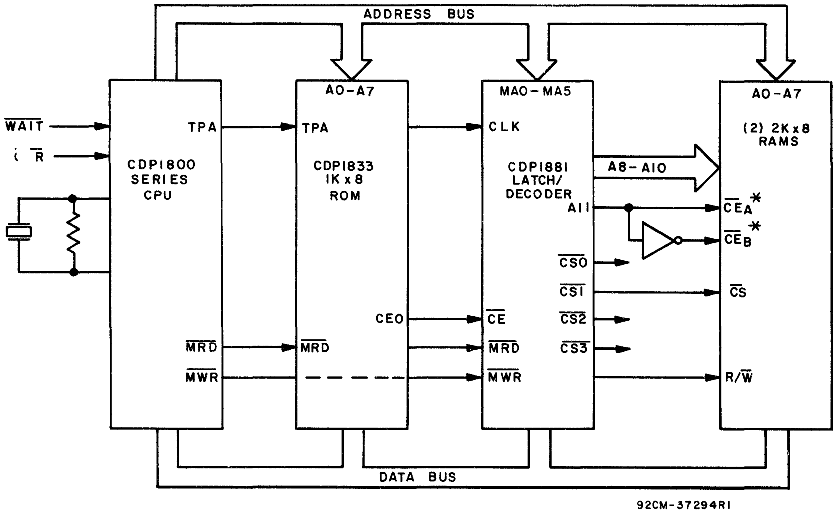
(1) Latch and decode high-order address bits for use as chip selects.

(2) Gate chip selects with $\overline{\text{MRD}}$ and $\overline{\text{MWR}}$ to prevent bus contention with the CPU

(3) Latch high-order address bits A8 to A11.

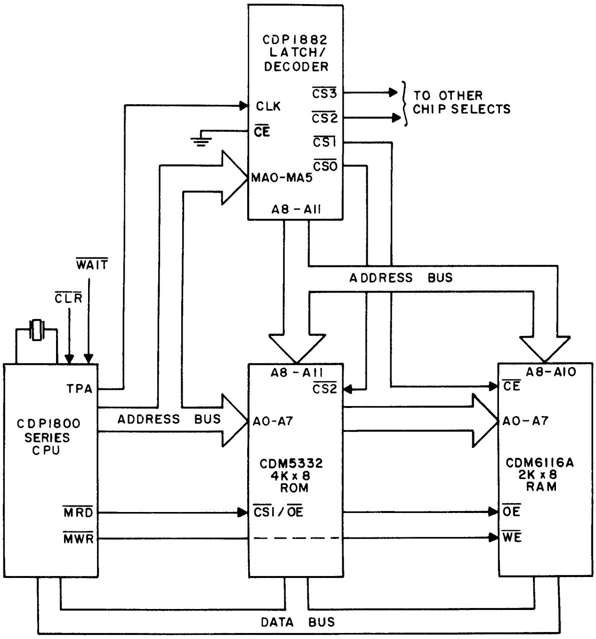
A system using the CDP1882 is shown in Fig. 5. The CDP1882 performs the memory address latch and decoder functions. Note that the RAM has an output enable ($\overline{\text{OE}}$) pin which eliminates the need for $\overline{\text{MRD}}$ and $\overline{\text{MWR}}$ inputs on the latch/decoder. Instead, the $\overline{\text{MRD}}$ line is connected directly to the RAM output enable ($\overline{\text{OE}}$) pin

In Fig. 6 the CDP1882 is used to decode a 16K-byte ROM system consisting of four CDM5332s.



* $\overline{\text{CE}}_A$ = $\overline{\text{CE}}$ RAM No 1
$\overline{\text{CE}}_B$ = $\overline{\text{CE}}$ RAM No 2

Fig. 4 - Minimum 1800-system using the CDP1881



92CM-36399R1

Fig. 5 - CDP1800-series system using the CDP1882.

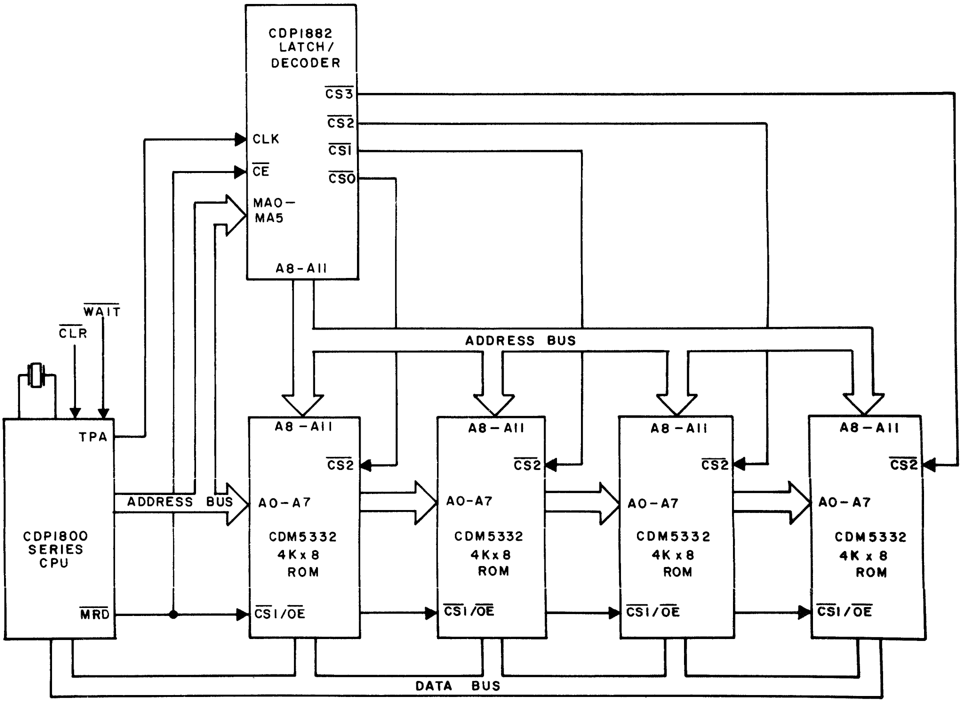
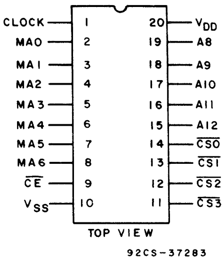


Fig. 6 - 16K-byte ROM systems using the CDP1882.

92CM-37293

CDP1883, CDP1883C



CDP1883, CDP1883C
TERMINAL ASSIGNMENT

CMOS 7-Bit Latch and Decoder Memory Interfaces

Features:

- *Performs memory address latch and decoder functions multiplexed or non-multiplexed*
- *Interfaces directly with the CDP1800-series microprocessors*
- *Allows decoding for systems up to 32K bytes*

The RCA-CDP1883 is a CMOS 7-bit memory latch and decoder circuit intended for use in CDP1800-series microprocessor systems It can serve as a direct interface between the multiplexed address bus of this system and up to four 8K x 8-bit memories to implement a 32K-byte memory system With four 4K x 8-bit memories, a 16K-byte system can be decoded

The device is also compatible with non-multiplexed address bus microprocessors By connecting the clock input to V_{DD}, the latches are in the data-following mode and the decoded outputs can be used in general-purpose memory-system applications

The CDP1833 is compatible with CDP1800-series microprocessors operating at maximum clock frequency.

The CDP1883 and CDP1883C are functionally identical. They differ in that the CDP1883 has a recommended operating voltage range of 4 to 10.5 volts and the C version has a recommended operating voltage range of 4 to 6.5 volts

The CDP1883 and CDP1883C are supplied in 20-lead, dual-in-line plastic packages (E suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY—VOLTAGE RANGE, (V_{DD}) (Voltage referenced to V_{SS} terminal)	
CDP1883	-0 5 to +11 V
CDP1883C	-0 5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0 5 to V_{DD} +0 5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A=-40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A=FULL PACKAGE-TEMPERATURE RANGE	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPE E	-40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 in (1 59 ± 0 79 mm) from case for 10 s max	+265°C

File Number **1507**

OPERATING CONDITIONS at T_A=Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1883		CDP1883C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, Except as Noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1883			CDP1883C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current I_{DD}	—	0, 5	5	—	1	10	—	5	50	µA
	—	0, 10	10	—	10	100	—	—	—	
Output Low Drive (Sink) Current I_{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0, 10	10	3.2	6.4	—	—	—	—	
Output High Drive (Source) Current I_{OH}	4.6	0, 5	5	-1.15	-2.3	—	-1.15	-2.3	—	
	9.5	0, 10	10	-2.3	-4.6	—	—	—	—	
Output Voltage Low-Level V_{OL}‡	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High-Level V_{OH}‡	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	
	0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	
	0.5, 9.5	—	10	7	—	—	—	—	—	
Input Leakage Current I_{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	µA
		0, 10	10	—	—	±2	—	—	—	
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current I_{DD1}Δ	0, 5	0, 5	5	—	—	2	—	—	2	mA
	0, 10	0, 10	10	—	—	4	—	—	—	
Minimum Data Retention Voltage V_{DR}	V_{DD} = V_{DR}			—	2	2.4	—	2	2.4	V
Data Retention Current I_{DR}	V_{DD} = 2 4 V			—	0.01	1	—	0.5	5	µA

*Typical values are for T_A = 25° C

‡I_{OL} = I_{OH} = 1 µA

ΔOperating current is measured at 200 kHz for V_{DD} = 5 V and 400 kHz for V_{DD} = 10 V, with outputs open circuit.

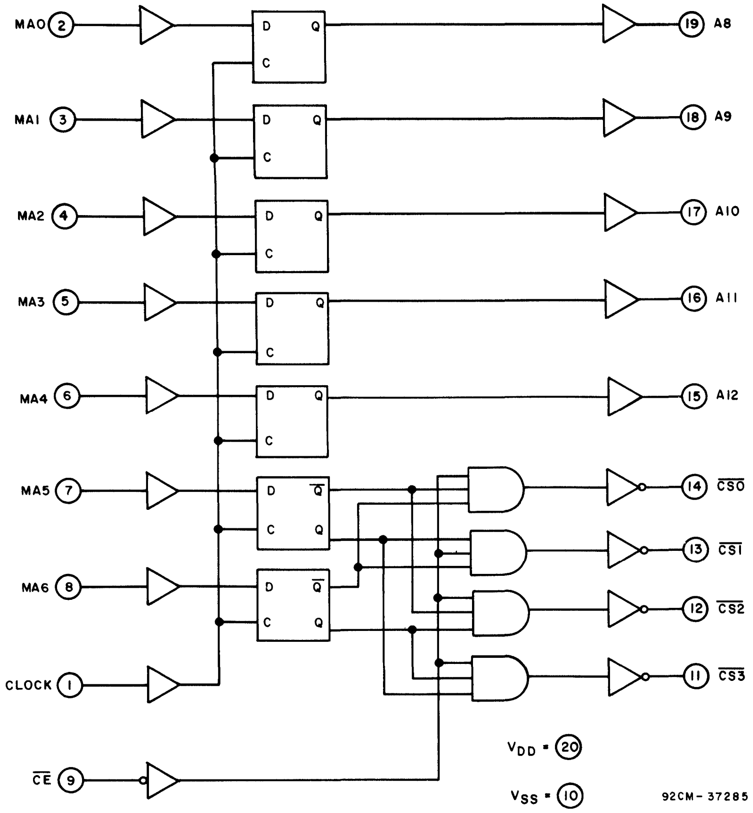


Fig. 1 - Functional diagram for the CDP1883, CDP1883C.

SIGNAL DESCRIPTIONS/PIN FUNCTIONS

CLOCK: Latch Input Control—a high on the clock input will allow data to pass through the latch to the output pin Data is latched on the high-to-low transition of the clock input. This pin is connected to TPA in the CDP1800 system and tied to V_{DD} for other applications.

MA0-MA4: address inputs to the high byte address latches

MA5-MA6: high byte address inputs decoded to produce chip selects $\overline{CS0}$-$\overline{CS3}$

$\overline{CE}$: CHIP ENABLE input A low on this pin will enable the chip select decoder. A high on this pin forces the $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, and $\overline{CS3}$ outputs to a high (false) state.

A8-A12: latched high-byte address outputs.

$\overline{CS0}$-$\overline{CS3}$: one of four latched and decoded Chip Select outputs.

V_{DD}, V_{SS}: power and ground pins, respectively.

TRUTH TABLES FOR CDP1883, CDP1833C

INPUTS				OUTPUTS			
$\overline{CE}$	CLK	MA5	MA6	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
0	1	0	0	0	1	1	1
0	1	1	0	1	0	1	1
0	1	0	1	1	1	0	1
0	1	1	1	1	1	1	0
0	0	X	X	PREVIOUS STATE			
1	X	X	X	1	1	1	1

INPUTS			OUTPUTS
$\overline{CE}$	CLK	MA0-4	A8-A12
X	1	1	1
X	1	0	0
X	0	X	PREVIOUS STATE

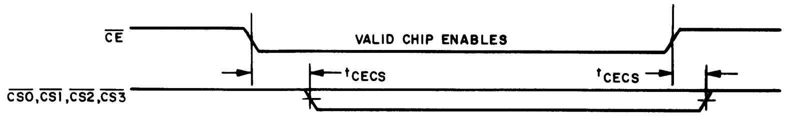
X = DON'T CARE

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85°C, V_{DD} ± 5%, t_r,t_r=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=100 pF. See Fig. 2.

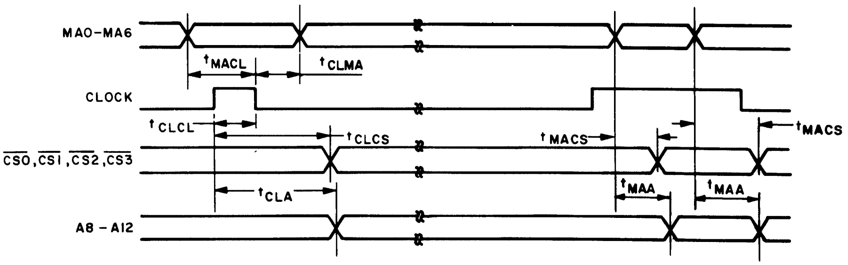
CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1883			CDP1883C			
			Min.	Typ.•	Max.Δ	Min.	Typ.•	Max.Δ	
Minimum Setup Time, Memory Address to CLOCK	t_{MACL}	5	—	10	35	—	10	35	ns
		10	—	8	25	—	—	—	
Minimum Hold Time, Memory Address After CLOCK	t_{CLMA}	5	—	8	25	—	8	25	
		10	—	8	25	—	—	—	
Minimum CLOCK Pulse Width	t_{CLCL}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Propagation Delay Times: $\overline{\text{Chip Enable}}$ to $\overline{\text{Chip Select}}$	t_{CECS}	5	—	75	150	—	75	150	
		10	—	45	100	—	—	—	
CLOCK to $\overline{\text{Chip Select}}$	t_{CLCS}	5	—	100	175	—	100	175	
		10	—	65	125	—	—	—	
CLOCK to Address,	t_{CLA}	5	—	100	175	—	100	175	
		10	—	65	125	—	—	—	
Memory Address to $\overline{\text{Chip Select}}$	t_{MACS}	5	—	100	175	—	100	175	
		10	—	75	125	—	—	—	
Memory Address to Address	t_{MAA}	5	—	80	125	—	80	125	
		10	—	40	60	—	—	—	

•Typical values are for T_A = 25°C

ΔMaximum limits of minimum characteristics are the values above which all devices function


$\overline{CE}$
VALID CHIP ENABLES
t_{CECS}
t_{CECS}
$\overline{CS0}$,$\overline{CS1}$,$\overline{CS2}$,$\overline{CS3}$

(a) $\overline{\text{CHIP ENABLE}}$ TO $\overline{\text{CHIP SELECT}}$ PROPAGATION DELAY



(b) MEMORY ADDRESS SETUP AND HOLD TIME

92CM-37284

Fig. 2 - CDP1883 timing waveforms.

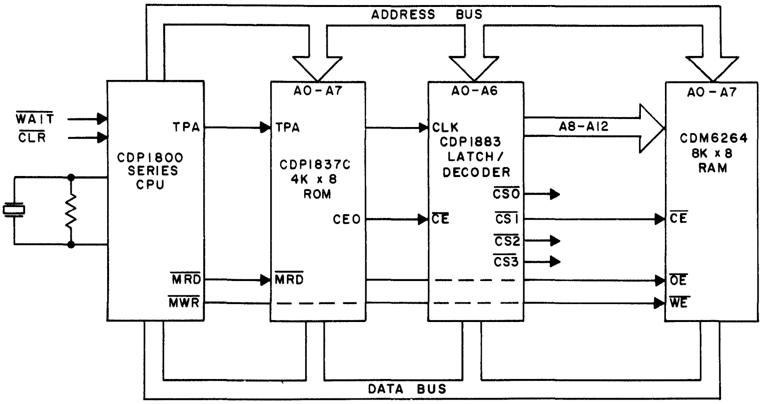
CDP1883, CDP1883C

APPLICATION INFORMATION

The CDP1883 and CDP1883C can be interfaced, without external components, with CDP1800-series microprocessor systems. These microprocessors feature a multiplexed address bus and provide an address latch signal (TPA) that is used as the Clock input of the CDP1883

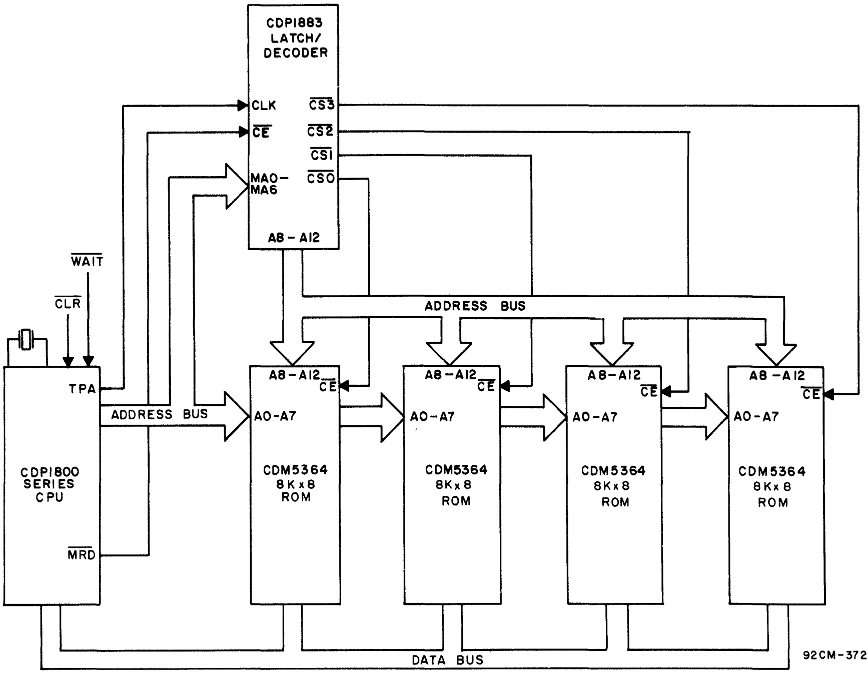
This signal is used to latch 7 bits of the high-order address. The lower five high-order address inputs are latched and held to be used with the eight lower-order address inputs to access an 8K x 8-bit memory. The two upper high-order address inputs are latched and decoded for use as chip selects.

The latched address and decoding functions of the CDP1883 and CDP1883C allow them to operate with 32K-byte memory systems. In addition, smaller memory systems can be configured with 4K x 8-bit or smaller memories, or a mix of memory sizes up to 8K x 8-bit.



92CM-37281

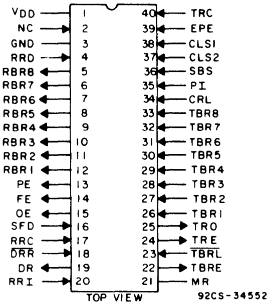
Fig. 3 - Minimum 1800-system using the CDP1883 to interface with an 8K x 8-bit memory.



92CM-37282

Fig 4 - 32K-byte ROM system using the CDP1883.

CDP6402, CDP6402C



TERMINAL ASSIGNMENT

CMOS Universal Asynchronous Receiver/Transmitter (UART)

Features:

- Low-power CMOS circuitry — 7.5 mW typ. at 3.2 MHz (max. freq.) at $V_{DD} = 5$ V
- *Baud rate - DC to 200K bits/sec (max.) at $V_{DD} = 5$ V, 85°C DC to 400K bits/sec (max.) at $V_{DD} = 10$ V, 85°C*
- *4 V to 10.5 operation*
- *Automatic data formatting and status generation*
- *Fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1.5, or 2 stop bits*
- *Operating-temperature range: (CDP6402D, CD) -55 to +125° (CDP6402E, CE) -40 to +85° C*
- *Replaces industry types IM6402 and HD6402*

The RCA CDP6402 and CDP6402C are silicon-gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits for interfacing computers or microprocessors to asynchronous serial data channels. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data channels. The receiver converts serial start, data, parity, and stop bits to parallel data verifying proper code transmission, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start parity and stop bits.

The data word can be 5, 6, 7 or 8 bits in length. Parity may be odd, even or inhibited. Stop bits can be 1, 1.5, or 2 (when transmitting 5-bit code).

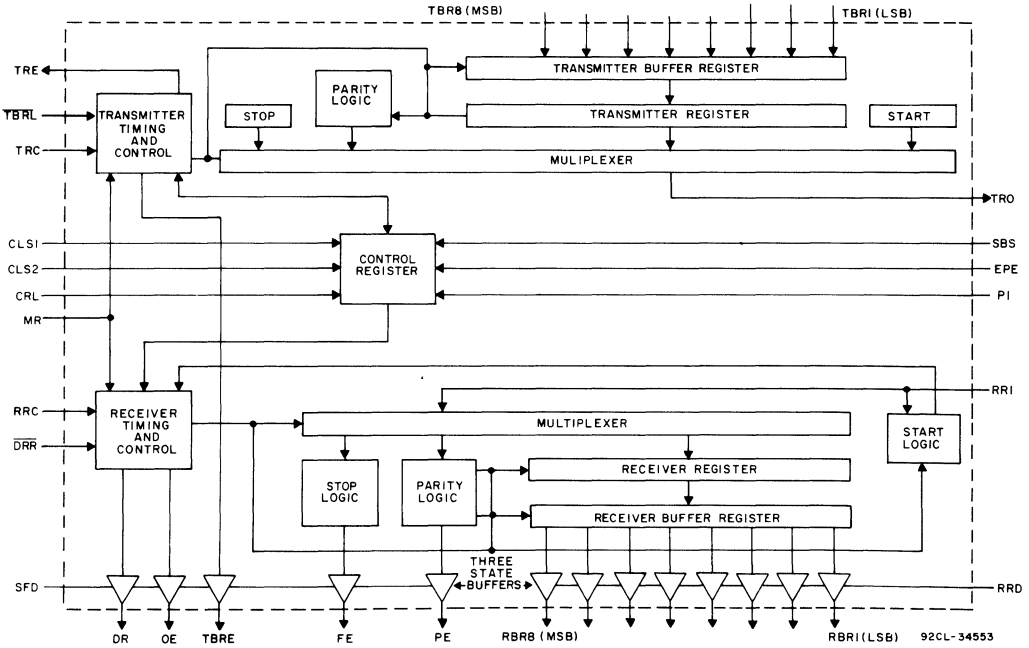


Fig. 1 - Functional block diagram.

File Number **1328**

CDP6402, CDP6402C

The CDP6402 and CDP6402C can be used in a wide range of applications including modems, printers, peripherals, video terminals, remote data acquisition systems, and serial data links for distributed processing systems.

The CDP6402 and CDP6402C are functionally identical. They differ in that the CDP6402 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP6402C has a recommended operating voltage range of 4 to 6.5 volts. Both types are supplied in 40-lead dual-in-line ceramic packages (D suffix), and 40-lead dual-in-line plastic packages (E suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltage referenced to V_{SS} Terminal)	
CDP6402	-0.5 to +11 V
CDP6402C	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	± 100 µA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Lineary at 12 mW/° C to 200 mW
For T_A = -55 to 100° C (PACKAGE TYPE D)	500 mW
For T_A = + 100 to +125° C (PACKAGE TYPE D)	Derate Lineary at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A).	
PACKAGE TYPE D	-55 to +125° C
PACKAGE TYPE E	-40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0 79 mm) from case for 10 s max.	+265° C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP6402		CDP6402C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, V_{DD} ±10%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP6402			CDP6402C			
				Min.	Typ.•	Max.	Min.	Typ.•	Max.	
Quiescent Device Current I_{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	µA
	—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current I_{OL}	0.4	0, 5	5	2	4	—	1.2	2.4	—	mA
	0.5	0, 10	10	5	7	—	—	—	—	
Output High Drive (Source) Current I_{OH}	4.6	0, 5	5	-0.55	-1.1	—	-0.55	-1.1	—	
	9.5	0, 10	10	-1.3	-2.6	—	—	—	—	
Output Voltage Low-Level V_{OL}‡	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level V_{OH}‡	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage V_{IL}	0.5, 4.5	—	5	—	—	0.8	—	—	0.8	
	0.5, 9.5	—	10	—	—	0.2 V_{DD}	—	—	—	
Input High Voltage V_{IH}	0.5, 4.5	—	5	V_{DD}-2	—	—	V_{DD}-2	—	—	
	0.5, 9.5	—	10	7	—	—	—	—	—	
Input Leakage Current I_{IN}	Any Input	0, 5	5	—	$\pm10^{-4}$	±1	—		±1	µA
		0, 10	10	—	$\pm10^{-4}$	±2	—	—	—	
3-State Output Leakage Current I_{OUT}	0, 5	0, 5	5	—	$\pm10^{-4}$	±1	—	$\pm10^{-4}$	±1	
	0, 10	0, 10	10	—	$\pm10^{-4}$	±10	—	—	—	
Operating Current, I_{DD1}‡	—	0, 5	5	—	1.5	—	—	1.5	—	mA
	—	0, 10	10	—	10	—	—	—	—	
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	

•Typical values are for T_A=25° C and nominal V_{DD}. ‡I_{OL}=I_{OH}=1 µA.

#Operating current is measured at 200 kHz or V_{DD} = 5 V and 400 kHz for V_{DD} = 10 V, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2 MHz).

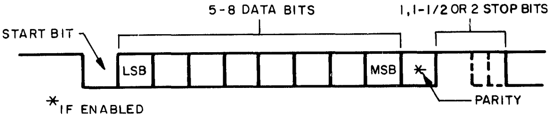
DESCRIPTION OF OPERATION

Initialization and Controls

A positive pulse on the MASTER RESET (MR) input resets the control, status, and receiver buffer registers, and sets the serial output (TRO) High. Timing is generated from the clock inputs RRC and TRC at a frequency equal to 16 times the serial data bit rate. The RRC and TRC inputs may be driven by a common clock, or may be driven independently by two different clocks. The CONTROL REGISTER LOAD (CRL) input is strobed to load control bits for PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECTS (SBS), and CHARACTER LENGTH SELECTS (CLS1 and CLS2). These inputs may be hand wired to V_{SS} or V_{DD} with CRL to V_{DD}. When the initialization is completed, the UART is ready for receiver and/or transmitter operations.

Transmitter Operation

The transmitter section accepts parallel data, formats it, and transmits it in serial form (Fig. 2) on the TRO terminal.

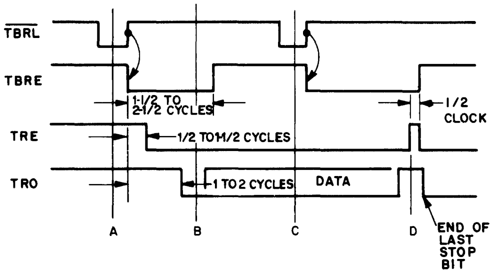


92CS-34554

Fig. 2 - Serial data format.

Transmitter timing is shown in Fig. 3. (A) Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the $\overline{TBRL}$ input. Valid data must be present at least t_{DT} prior to, and t_{TD} following, the rising edge of $\overline{TBRL}$. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. (B) The rising edge of $\overline{TBRL}$ clears TBRE. ½ to 1½ cycles later, depending on when the $\overline{TBRL}$ pulse occurs with respect to TRC, data is transferred to the transmitter register and TRE is cleared. TBRE is set to a logic High one cycle after that.

Output data is clocked by TRC. The clock rate is 16 times the data rate. (C) A second pulse on $\overline{TBRL}$ loads data into the transmitter buffer register Data transfer to the transmitter register is delayed until transmission of the current character is complete. (D) Data is automatically transferred to the transmitter register and transmission of that character begins.

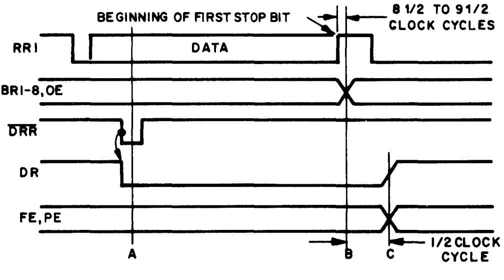


92CS-38054R1

Fig. 3 - Transmitter timing waveforms.

Receiver Operation

Data is received in serial form at the RRI input. When no data is being received, RRI input must remain high. The data is clocked through the RRC. The clock rate is 16 times the data rate. Receiver timing is shown in Fig. 4.



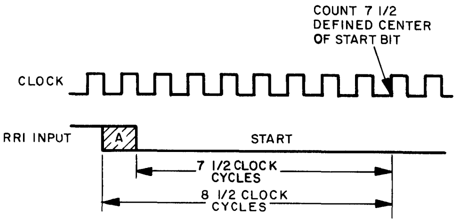
92CS-34559R2

Fig. 4 - Receiver timing waveforms.

(A) A low level on $\overline{DRR}$ clears the DR line. (B) During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OE indicates overruns. An overrun occurs when DR has not been cleared before the present character was transferred to the RBR. (C) 1/2 clock cycle later DR is set to a logic high and FE is evaluated. A logic high on FE indicates an invalid stop bit was received A logic high on PE indicates a parity error.

Start Bit Detection

The receiver uses a 16X clock for timing (Fig. 5) The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7 1/2. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle, ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at 9 clocks into the first stop bit.



92CS-34558

Fig. 5 - Start bit timing waveforms.

CDP6402, CDP6402C

Table I - Control Word Function

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

X = Don't Care

Table II - Function Pin Definition

PIN	SYMBOL	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	N/C	No Connection
3	GND	Ground (V_{SS})
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register ouputs RBR1-RBR8 to a high impedance state
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs Word formats less than 8 characters are right justified to RBR1
6	RBR7	See Pin 5 - RBR8
7	RBR6	
8	RBR5	
9	RBR4	
10	RBR3	
11	RBR2	
12	RBR1	
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits The output is active until parity matches on a succeeding character When parity is inhibited, this output is low
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if DRR has been performed (i.e., DRR; active low).
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE and DR, and sets TRE, TBRE, and TRO. TRE is actually set on the first rising edge of TRC after MR goes high. MR should be strobed after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.

Table II - Function Pin Definition (Cont'd)

PIN	SYMBOL	DESCRIPTION
23	$\overline{\text{TBRL}}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{\text{TBRL}}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8 For character formats less than 8-bits, the TBR8, 7, and 6 Inputs are ignored corresponding to the programmed word length
27	TBR2	See Pin 26 - TBR1
28	TBR3	
29	TBR4	
30	TBR5	
31	TBR6	
32	TBR7	
33	TBR8	
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits) (CLS1 high CLS2 low 6-bits) (CLS1 low CLS2 high 7-bits) (CLS1 high CLS2 high 8-bits).
38	CLS1*	See Pin 37 - CLS2
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity A low level selects odd parity
40	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

*See Table I (Control Word Function)

CDP6402, CDP6402C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC †	V_{DD} (V)	LIMITS				UNITS
		CDP6402		CDP6402C		
		Typ.•	Max.Δ	Typ.•	Max.Δ	
System Timing (See Fig. 6)						
Minimum Pulse Width: CRL t_{CRL}	5 10	50 40	150 100	50 —	150 —	ns
Minimum Setup Time Control Word to CRL t_{CWC}	5 10	20 0	50 40	20 —	50 —	
Minimum Hold Time Control Word after CRL t_{CCW}	5 10	40 20	60 30	40 —	60 —	
Propagation Delay Time SFD High to SOD t_{SFDH}	5 10	130 100	200 150	130 —	200 —	
SFD Low to SOD t_{SFDL}	5 10	130 40	200 60	130 —	200 —	
RRD High to Receiver Register High Impedance t_{RRDH}	5 10	80 40	150 70	80 —	150 —	
RRD Low to Receiver Register Active t_{RRDL}	5 10	80 40	150 70	80 —	150 —	
Minimum Pulse Width: MR	5 10	200 100	400 200	200 —	400 —	

•Typical values for T_A = 25° C and nominal V_{DD}.

ΔMaximum limits of minimum characteristics are the values above which all devices function.

†All measurements are made at the 50% point of the transition except tri-state measurements

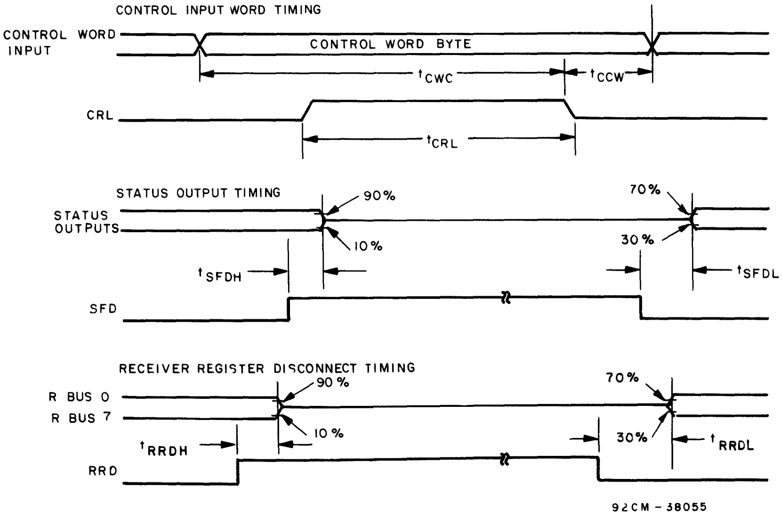


Fig. 6 - System timing waveforms.

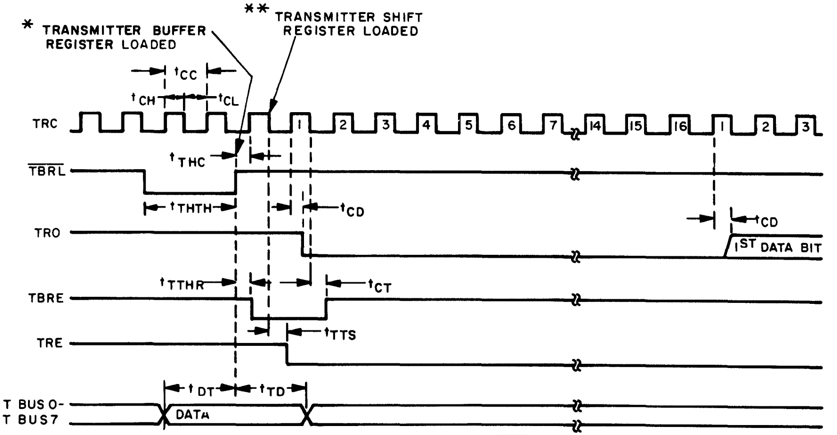
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC†		V_{DD} (V)	LIMITS CDP6402 Typ.•	LIMITS CDP6402 Max.Δ	LIMITS CDP6402C Typ.•	LIMITS CDP6402C Max.Δ	UNITS
Transmitter Timing (See Fig. 7)							
Minimum Clock Period (TRC)	t_{CC}	5	250	310	250	310	ns
		10	125	155	—	—	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	100	125	100	125	
		10	75	100	—	—	
Clock High Level	t_{CH}	5	100	125	100	125	
		10	75	100	—	—	
$\overline{\text{TBRL}}$	t_{THTH}	5	80	200	80	200	
		10	40	100	—	—	
Minimum Setup Time: $\overline{\text{TBRL}}$ to Clock	t_{THC}	5	175	275	175	275	
		10	90	150	—	—	
Data to $\overline{\text{TBRL}}$ ↗	t_{DT}	5	20	50	20	50	
		10	0	40	—	—	
Minimum Hold Time: Data after $\overline{\text{TBRL}}$ ↗	t_{TD}	5	40	60	40	60	
		10	20	30	—	—	
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5	300	450	300	450	
		10	150	225	—	—	
Clock to TBRE	t_{CT}	5	330	400	330	400	
		10	100	150	—	—	
$\overline{\text{TBRL}}$ to TBRE	t_{TTHR}	5	200	300	200	300	
		10	100	150	—	—	
Clock to TRE	t_{TTS}	5	330	400	330	400	
		10	100	150	—	—	

•Typical values for T_A = 25° C and nominal V_{DD}.

ΔMaximum limits of minimum characteristics are the values above which all devices function.

†All measurements are made at the 50% point of the transition except tri-state measurements.



* THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF $\overline{\text{TBRL}}$

** THE TRANSMITTER SHIFT REGISTER, IF EMPTY, IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD + t_{THC} AFTER THE TRAILING EDGE OF $\overline{\text{TBRL}}$ AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER

Fig. 7 - Transmitter timing waveforms.

CDP6402, CDP6402C

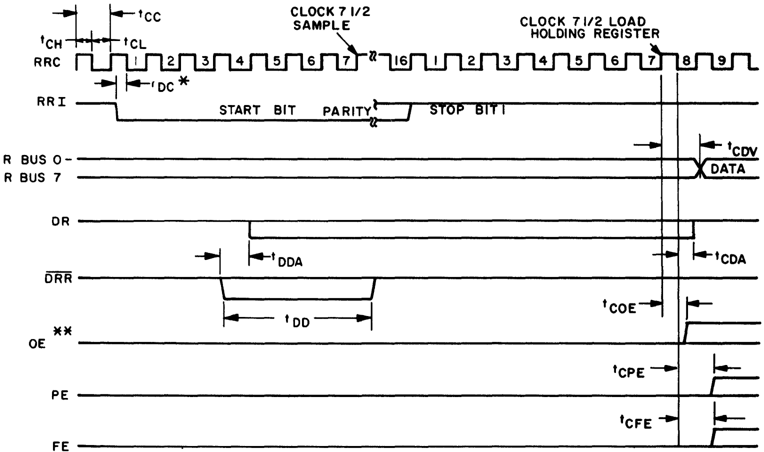
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC †		V_{DD} (V)	LIMITS				UNITS
			CDP6402		CDP6402C		
			Typ.•	Max.△	Typ.•	Max.△	
Receiver Timing (See Fig. 8)							
Minimum Clock Period (RRC)	t_{CC}	5 10	250 125	310 155	250 —	310 —	ns
Minimum Pulse Width: Clock Low Level	t_{CL}	5 10	100 75	125 100	100 —	125 —	
Clock High Level	t_{CH}	5 10	100 75	125 100	100 —	125 —	
$\overline{\text{DATA RECEIVED RESET}}$	t_{DD}	5 10	50 25	75 40	50 —	75 —	
Minimum Setup Time: Data Start Bit to Clock	t_{DC}	5 10	100 50	150 75	100 —	150 —	
Propagation Delay Time: $\overline{\text{DATA RECEIVED RESET}}$ to Data Received	t_{DDA}	5 10	150 75	250 125	150 —	250 —	
Clock to Data Valid	t_{CDV}	5 10	275 110	400 175	275 —	400 —	
Clock to DR	t_{CDA}	5 10	275 110	400 175	275 —	400 —	
Clock to Overrun Error	t_{COE}	5 10	275 100	400 150	275 —	400 —	
Clock to Parity Error	t_{CPE}	5 10	240 120	375 175	240 —	375 —	
Clock to Framing Error	t_{CFE}	5 10	200 100	300 150	200 —	300 —	

•Typical values for T_A = 25° C and nominal V_{DD}.

△Maximum limits of minimum characteristics are the values above which all devices function.

†All measurements are made at the 50% point of the transition except tri-state measurements.



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK

** IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE

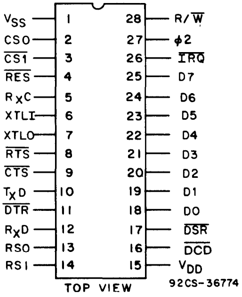
Fig. 8 - Receiver timing waveforms.

Advance Information

CDP65C51

CMOS Asynchronous Communications Interface Adapter (ACIA)

TERMINAL ASSIGNMENT


V_{SS} 1
CS0 2
$\overline{\text{CS1}}$ 3
$\overline{\text{RES}}$ 4
R_XC 5
XTLI 6
XTLO 7
$\overline{\text{RTS}}$ 8
$\overline{\text{CTS}}$ 9
T_XD 10
$\overline{\text{DTR}}$ 11
R_XD 12
RS0 13
RS1 14
28 R/$\overline{\text{W}}$
27 φ2
26 $\overline{\text{IRQ}}$
25 D7
24 D6
23 D5
22 D4
21 D3
20 D2
19 D1
18 D0
17 $\overline{\text{DSR}}$
16 $\overline{\text{DCD}}$
15 V_{DD}
TOP VIEW
92CS-36774

Features:

- *Compatible with 8-bit microprocessors*
- *Full duplex operation with buffered receiver and transmitter*
- *Data set/modem control functions*
- *Internal baud-rate generator with 15 programmable baud rates (50 to 19,200)*
- *Program-selectable internally or externally controlled receiver rate*
- *Operates at baud rates up to 250,000 via proper crystal or clock selection*
- *Programmable word lengths, number of stop bits, and parity-bit generation and detection*
- *Programmable interrupt control*
- *Program reset*
- *Program-selectable serial echo mode*
- *Two chip selects*
- *4-MHz, 2 MHz or 1 MHz operation (CDP65C51-4, CDP65C51-2, CDP65C51-1, respectively)*
- *Single 3 V to 6 V power supply*
- *Full TTL compatibility*

The RCA-CDP65C51 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program-controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The CDP65C51 has an internal baud-rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or 1/16 times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at 1/16 times an external clock rate The CDP65C51 has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, 1½, or 2 stop bits

The CDP65C51 is designed for maximum programmed control from the CPU, to simplify hardware implementation. Three separate registers permit the CPU to easily select the CDP65C51 operating modes and data-checking parameters and determine operational status.

The **Command Register** controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{\text{RTS}}$ line, receiver interrupt control, and the state of the $\overline{\text{DTR}}$ line.

The **Control Register** controls the number of stop bits, word length, receiver clock source, and baud rate.

The **Status Register** indicates the states of the $\overline{\text{IRQ}}$, $\overline{\text{DSR}}$, and $\overline{\text{DCD}}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the CDP65C51 Transmit and Receive circuits.

The CDP65C51-1, CDP65C51-2, and CDP65C51-4 are capable of interfacing with microprocessors with cycle times of 1 MHz, 2 MHz and 4 MHz, respectively.

The CDP65C51 is supplied in 28-lead, hermetic, dual-in-line side brazed ceramic packages (D suffix), in 28-lead, dual-in-line plastic packages (E suffix) and in 28-lead dual-in-line small-outline (SO) packages (M) suffix.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltage referenced to V_{SS} terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +85°C (PACKAGE TYPE M)*	425 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E and M	-40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

RECOMMENDED OPERATING CONDITIONS at T_A = -40° to +85°C
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

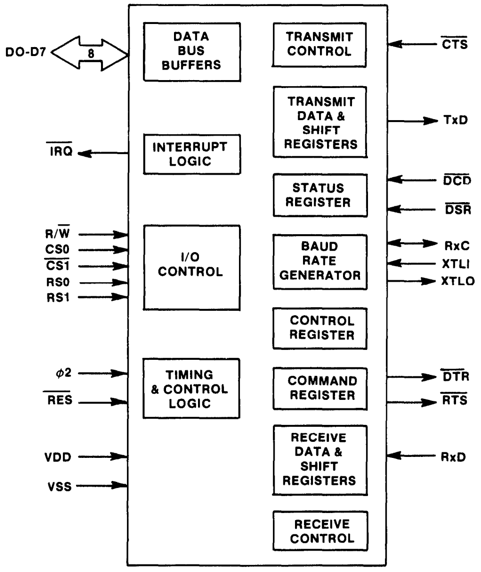
CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating Voltage Range	3	6	V
Input Voltage Range	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40° to +85°C, V_{DD} = 5V ± 5%

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Quiescent Device Current	I_{DD}	—	50	200	μA
Output Low Current (Sinking): V_{OL} = 0.4 V (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$	I_{OL}	1.6	—	—	mA
Output High Current (Sourcing): V_{OH} = 4.6 V (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	I_{OH}	-1.6	—	—	mA
Output Low Voltage: I_{LOAD} = 1.6 mA (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	—	—	0.4	V
Output High Voltage: I_{LOAD} = -1.6 mA (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	V_{OH}	4.6	—	—	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Input High Voltage (Except XTLI and XTLO) (XTLI and XTLO)	V_{IH}	 2 3	 — —	 V_{DD} V_{DD}	V
Input Leakage Current: V_{IN} = 0 to 5 V (ϕ2, R/$\overline{W}$, $\overline{RES}$, CS0, $\overline{CS1}$, RS0, RS1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	—	—	±1	μA
Input Leakage Current for High Impedance State (D0-D7)	I_{TSI}	—	—	±1.2	μA
Output Leakage Current (off state): V_{OUT} = 5 V ($\overline{IRQ}$)	I_{OFF}	—	—	2	μA
Input Capacitance (except XTLI and XTLO)	C_{IN}	—	—	10	pF
Output Capacitance	C_{OUT}	—	—	10	pF

CDP65C51 INTERFACE REQUIREMENTS

This section describes the interface requirements for the CDP65C51 ACIA. Fig. 1 is the Interface Diagram and the Terminal Diagram shows the pin-out configuration for the CDP65C51.



92CM-36860

Fig. 1 - CDP65C51 interface diagram.

MICROPROCESSOR INTERFACE SIGNAL DESCRIPTION

$\overline{\text{RES}}$ (Reset) (4)

During system initialization a low on the $\overline{\text{RES}}$ input will cause a hardware reset to occur. The Command Register and the Control Register will be cleared. The Status Register will be cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the $\overline{\text{DSR}}$ and $\overline{\text{DCD}}$ lines, and the **transmitter Empty bit, which will be set. A hardware reset is required after power-up.**

φ2 (Input Clock) (27)

The input clock is the system φ2 clock and is used to clock all data transfers between the system microprocessor and the CDP65C51.

R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$) (28)

The R/$\overline{\text{W}}$ input, generated by the microprocessor, is used to control the direction of data transfers. A high on the R/$\overline{\text{W}}$ pin allows the processor to read the data supplied by the CDP65C51, a low allows a write to the CDP65C51.

$\overline{\text{IRQ}}$ (Interrupt Request) (26)

The $\overline{\text{IRQ}}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{\text{IRQ}}$ microprocessor input. Normally at high level, $\overline{\text{IRQ}}$ goes low when an interrupt occurs.

D0-D7 (Data Bus) (18-25)

The D0-D7 pins are the eight data lines used to transfer data between the processor and the CDP65C51. These lines are bi-directional and are normally high-impedance except during Read cycles when the CDP65C51 is selected.

CS0, $\overline{\text{CS1}}$ (Chip Selects) (2, 3)

The two chip-select inputs are normally connected to the processor address lines either directly or through decoders. The CDP65C51 is selected when CS0 is high and $\overline{\text{CS1}}$ is low.

RS0, RS1 (Register Selects) (13, 14)

The two register-select lines are normally connected to the processor address lines to allow the processor to select the various CDP65C51 internal registers. The following table shows the internal register-select coding.

TABLE I

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command Register and bit 2 in the Status Register. The Control Register is unchanged by a Programmed Reset. It should be noted that the Programmed Reset is slightly different from the Hardware Reset ($\overline{\text{RES}}$); these differences are shown in Figs. 3, 4 and 5.

ACIA/MODEM INTERFACE SIGNAL DESCRIPTION

XTLI, XTLO (Crystal Pins) (6, 7)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates (see "Generation of Non-Standard Baud Rates"). Alternatively, an externally generated clock may be used to drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

TxD (Transmit Data) (10)

The TxD output line is used to transfer serial NRZ (nonreturn-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or under control of an external clock. This selection is made by programming the Control Register.

RxD (Receive Data) (12)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or under the control of an externally generated receiver clock. The selection is made by programming the Control Register.

CDP65C51 INTERFACE REQUIREMENTS (Cont'd)

RxC (Receive Clock) (5)

The RxC is a bidirectional pin which serves as either the receiver 16X clock input or the receiver 16X clock output. The latter mode results if the internal baud-rate generator is selected for receiver data clocking.

$\overline{\text{RTS}}$ (Request to Send) (8)

The $\overline{\text{RTS}}$ output pin is used to control the modem from the processor. The state of the $\overline{\text{RTS}}$ pin is determined by the contents of the Command Register.

$\overline{\text{CTS}}$ (Clear to Send) (9)

The $\overline{\text{CTS}}$ input pin is used to control the transmitter operation. The enable state is with $\overline{\text{CTS}}$ low. The transmitter is automatically disabled if $\overline{\text{CTS}}$ is high.

$\overline{\text{DTR}}$ (Data Terminal Ready) (11)

This output pin is used to indicate the status of the CDP65C51 to the modem. A low on $\overline{\text{DTR}}$ indicates the CDP65C51 is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{\text{DSR}}$ (Data Set Ready) (17)

The $\overline{\text{DSR}}$ input pin is used to indicate to the CDP65C51 the status of the modem. A low indicates the "ready" state and a high, "not-ready".

$\overline{\text{DCD}}$ (Data Carrier Detect) (16)

The $\overline{\text{DCD}}$ input pin is used to indicate to the CDP65C51 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

CDP65C51 INTERNAL ORGANIZATION

This section provides a functional description of the CDP65C51 A block diagram of the CDP65C51 is presented in Fig. 2.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bidirectional. When the R/$\overline{\text{W}}$ line is high and the chip is selected, the Data Bus Buffer passes the data to the system data lines from the CDP65C51 internal data bus. When the R/$\overline{\text{W}}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the system data bus to the internal data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{\text{IRQ}}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{\text{DCD}}$) logic and the Data Set Ready ($\overline{\text{DSR}}$) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers in preparation for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Register Select and Chip Select and Read/Write lines as described in Table I, previously.

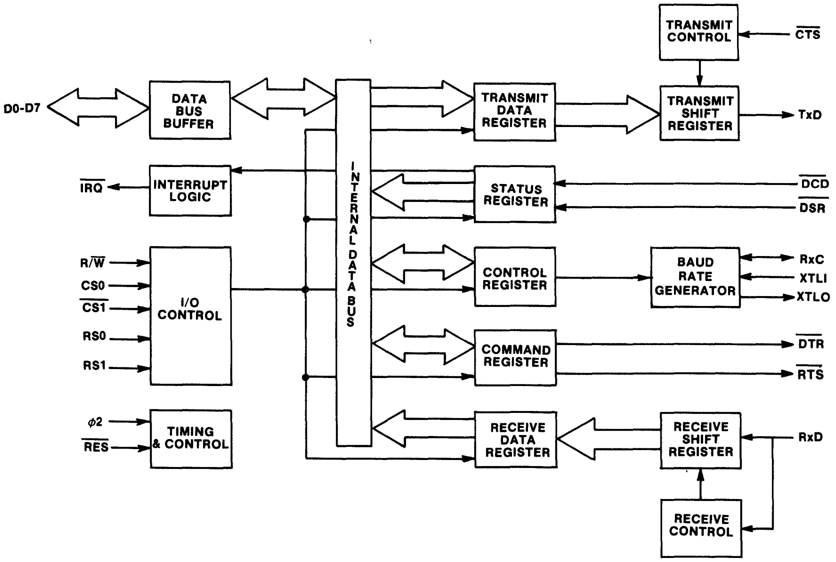


Fig. 2 - Internal organization. 92CM-36890R1

CDP65C51 INTERNAL ORGANIZATION (Cont'd)

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus and the registers, the Data Bus Buffer, and the microprocessor data bus, and the hardware reset features.

Timing is controlled by the system $\phi 2$ clock input. The chip will perform data transfers to or from the microcomputer data bus during the $\phi 2$ high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset $(\overline{RES})$ line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the CDP65C51 Transmit and Receive circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care".

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

STATUS REGISTER

Fig. 3 indicates the format of the CDP65C51 Status Register. A description of each status bit follows.

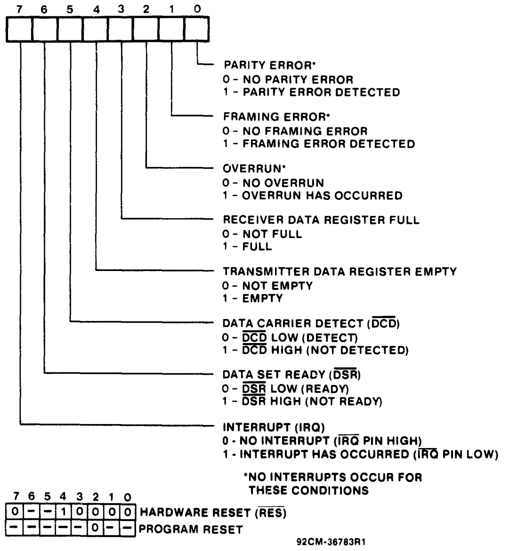

7 6 5 4 3 2 1 0
PARITY ERROR*
0 - NO PARITY ERROR
1 - PARITY ERROR DETECTED
FRAMING ERROR*
0 - NO FRAMING ERROR
1 - FRAMING ERROR DETECTED
OVERRUN*
0 - NO OVERRUN
1 - OVERRUN HAS OCCURRED
RECEIVER DATA REGISTER FULL
0 - NOT FULL
1 - FULL
TRANSMITTER DATA REGISTER EMPTY
0 - NOT EMPTY
1 - EMPTY
DATA CARRIER DETECT (DCD)
0 - DCD LOW (DETECT)
1 - DCD HIGH (NOT DETECTED)
DATA SET READY (DSR)
0 - DSR LOW (READY)
1 - DSR HIGH (NOT READY)
INTERRUPT (IRQ)
0 - NO INTERRUPT (IRQ PIN HIGH)
1 - INTERRUPT HAS OCCURRED (IRQ PIN LOW)
*NO INTERRUPTS OCCUR FOR THESE CONDITIONS
7 6 5 4 3 2 1 0
0 - - 1 0 0 0 0 HARDWARE RESET (RES)
- - - - - 0 - - PROGRAM RESET
92CM-36783R1

Fig. 3 - Status register format.

Receiver Data Register Full (Bit 3)

This bit goes to a "1" when the CDP65C51 transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a "0" when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a "1" when the CDP65C51 transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a "0" when the processor writes new data onto the Transmitter Data Register.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the CDP65C51. A "0" indicates a low level (true condition) and a "1" indicates a high (false). Whenever either of these inputs changes state, an immediate processor interrupt occurs, unless the CDP65C51 is disabled (bit 0 of the Command Register is a "0"). When the interrupt occurs, the status bits will indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until the Status Register is interrogated by the processor. At that time, another interrupt will immediately occur and the status bits will reflect the new input levels.

Framing Error (Bit 1), Overrun (Bit 2), and Parity Error (Bit 0)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified.

Interrupt (Bit 7)

This bit goes to a "0" when the Status Register has been read by the processor, and goes to a "1" whenever any kind of interrupt occurs.

CONTROL REGISTER

The Control Register selects the desired transmitter baud rate, receiver clock source, word length, and the number of stop bits.

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits, set by the processor, select the Transmitter baud rate, which can be at 1/16 an external clock rate or one of 15 other rates controlled by the internal baud-rate generator as shown in Fig. 4.

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A "0" causes the Receiver to operate at a baud rate of 1/16 an external clock. A "1" causes the Receiver to operate at the same baud rate as is selected for the transmitter as shown in Fig. 4.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits). Fig. 4 shows the configuration for each number of bits desired.

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A "0" always indicates one stop bit. A "1" indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, and 2 stop bits in all other configurations.

CDP65C51 INTERNAL ORGANIZATION (Cont'd)

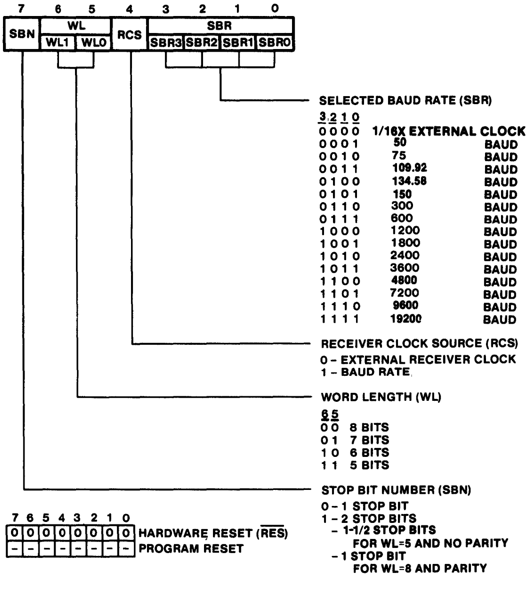


Fig. 4 - CDP65C51 control register.

COMMAND REGISTER

The Command Register controls specific modes and functions (Fig. 5).

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{DTR}$) line. A "0" indicates the microcomputer system is not ready by setting the $\overline{DTR}$ line high. A "1" indicates the microcomputer system is ready by setting the $\overline{DTR}$ line low. When the DTR bit is set to a "0", the receiver and transmitter are both disabled.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a "1". The Receiver interrupt is enabled when this bit is set to a "0" and Bit 0 is set to a "1".

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{RTS}$) line and the Transmitter interrupt. Fig. 5 shows the various configurations of the $\overline{RTS}$ line and Transmit Interrupt bit settings.

Receiver Echo Mode (Bit 4)

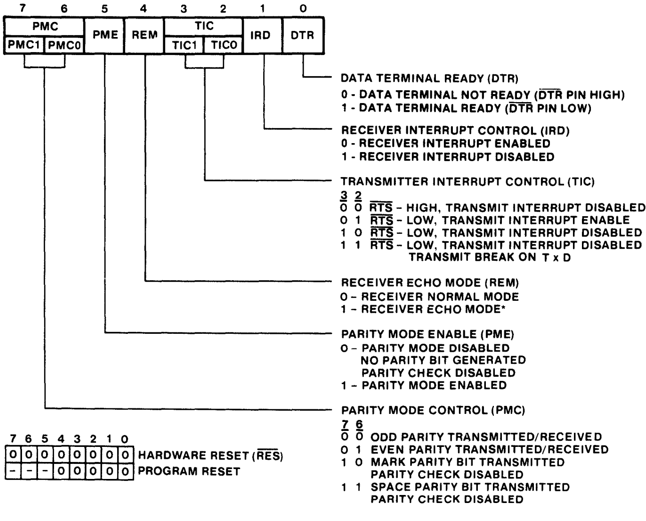
This bit enables the Receiver Echo Mode. Bits 2 and 3 must be zero. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by ½ bit time. A "1" enables the Receiver Echo Mode. A "0" bit disables the mode.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A "0" disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A "1" bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check). Fig. 5 shows the possible bit configurations for the Parity Mode Control bits.


7 6 5 4 3 2 1 0
PMC
PMC1
PMC0
PME
REM
TIC
TIC1
TIC0
IRD
DTR
DATA TERMINAL READY (DTR)
0 - DATA TERMINAL NOT READY ($\overline{DTR}$ PIN HIGH)
1 - DATA TERMINAL READY ($\overline{DTR}$ PIN LOW)
RECEIVER INTERRUPT CONTROL (IRD)
0 - RECEIVER INTERRUPT ENABLED
1 - RECEIVER INTERRUPT DISABLED
TRANSMITTER INTERRUPT CONTROL (TIC)
3 2
0 0 $\overline{RTS}$ - HIGH, TRANSMIT INTERRUPT DISABLED*
0 1 $\overline{RTS}$ - LOW, TRANSMIT INTERRUPT ENABLE
1 0 $\overline{RTS}$ - LOW, TRANSMIT INTERRUPT DISABLED
1 1 $\overline{RTS}$ - LOW, TRANSMIT INTERRUPT DISABLED TRANSMIT BREAK ON T x D
RECEIVER ECHO MODE (REM)
0 - RECEIVER NORMAL MODE
1 - RECEIVER ECHO MODE*
PARITY MODE ENABLE (PME)
0 - PARITY MODE DISABLED NO PARITY BIT GENERATED PARITY CHECK DISABLED
1 - PARITY MODE ENABLED
PARITY MODE CONTROL (PMC)
7 6
0 0 ODD PARITY TRANSMITTED/RECEIVED
0 1 EVEN PARITY TRANSMITTED/RECEIVED
1 0 MARK PARITY BIT TRANSMITTED PARITY CHECK DISABLED
1 1 SPACE PARITY BIT TRANSMITTED PARITY CHECK DISABLED
7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0 HARDWARE RESET ($\overline{RES}$)
- - - 0 0 0 0 0 PROGRAM RESET

*BITS 2 AND 3 MUST BE ZERO FOR RECEIVER ECHO MODE $\overline{RTS}$ WILL BE LOW

Fig. 5 - CDP65C51 command register. 92CM-36790R1

CDP65C51 INTERNAL ORGANIZATION (Cont'd)

TRANSMITTER AND RECEIVER

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the CDP65C51. Fig. 6 shows the Transmitter and Receiver layout.

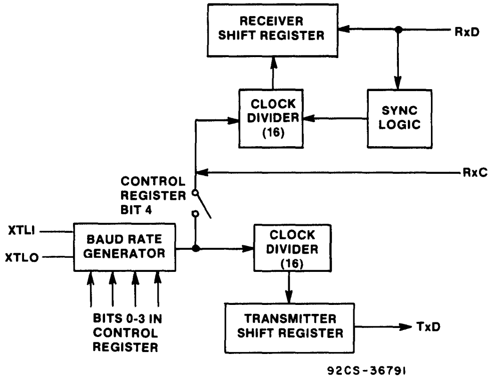


Fig. 6 - Transmitter receiver clock circuits.

CDP65C51 OPERATION

TRANSMITTER AND RECEIVER OPERATION

Continuous Data Transmit (Fig. 7)

In the normal operating mode, the processor interrupt (IRQ) is used to signal when the CDP65C51 is ready to accept the next data word to be transmitted. This interrupt occurs at the beginnning of the Start Bit When the processor reads the Status Register of the CDP65C51, the interrupt is cleared. The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted.

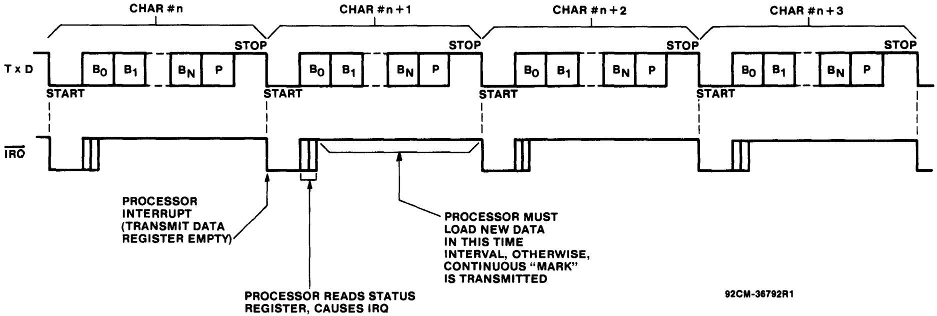

CHAR #n
CHAR #n+1
CHAR #n+2
CHAR #n+3
TxD
STOP
START
B0
B1
BN
P
IRQ
PROCESSOR INTERRUPT (TRANSMIT DATA REGISTER EMPTY)
PROCESSOR MUST LOAD NEW DATA IN THIS TIME INTERVAL, OTHERWISE, CONTINUOUS "MARK" IS TRANSMITTED
PROCESSOR READS STATUS REGISTER, CAUSES IRQ TO CLEAR
92CM-36792R1

Fig. 7 - Continuous data transmit.

Continuous Data Receive (Fig. 8)

Similar to the above case, the normal mode is to generate a processor interrupt when the CDP65C51 has received a full data word. This occurs at about the 8/16 point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the Overrun condition occurs.

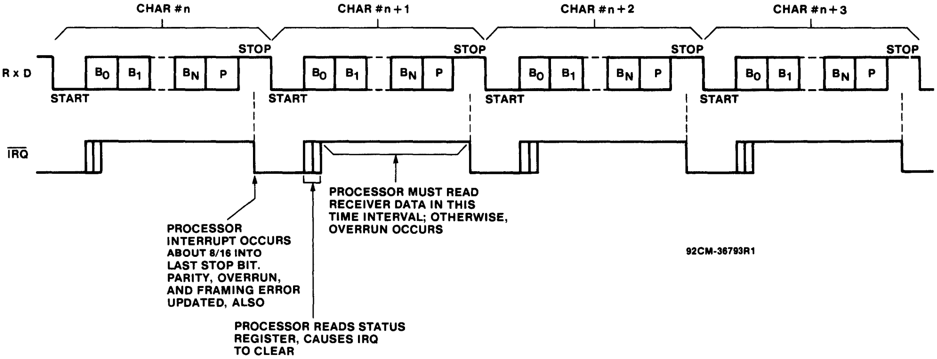

CHAR #n
CHAR #n+1
CHAR #n+2
CHAR #n+3
RxD
STOP
START
B0
B1
BN
P
IRQ
PROCESSOR MUST READ RECEIVER DATA IN THIS TIME INTERVAL; OTHERWISE, OVERRUN OCCURS
PROCESSOR INTERRUPT OCCURS ABOUT 8/16 INTO LAST STOP BIT. PARITY, OVERRUN, AND FRAMING ERROR UPDATED, ALSO
PROCESSOR READS STATUS REGISTER, CAUSES IRQ TO CLEAR
92CM-36793R1

Fig. 8 - Continuous data receive.

CDP65C51 OPERATION (Cont'd)

Transmit Data Register Not Loaded By Processor (Fig. 9)

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line will go to the "MARK" condition until the data is loaded. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word.

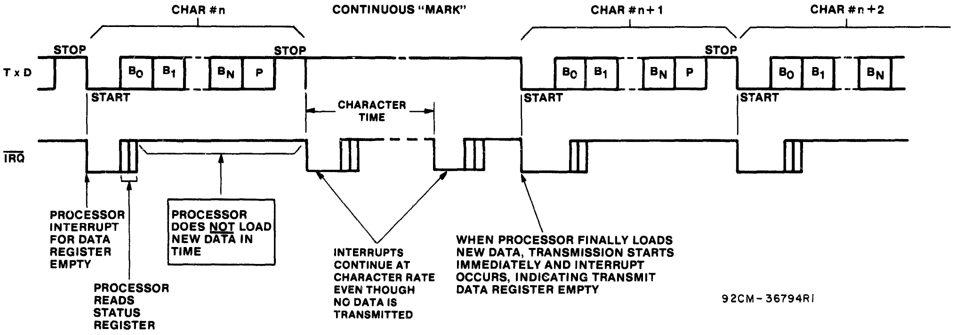

CHAR #n
CONTINUOUS "MARK"
CHAR #n+1
CHAR #n+2
STOP
STOP
STOP
TxD
B_0
B_1
B_N
P
START
CHARACTER TIME
START
START
$\overline{IRQ}$
PROCESSOR INTERRUPT FOR DATA REGISTER EMPTY
PROCESSOR DOES NOT LOAD NEW DATA IN TIME
PROCESSOR READS STATUS REGISTER
INTERRUPTS CONTINUE AT CHARACTER RATE EVEN THOUGH NO DATA IS TRANSMITTED
WHEN PROCESSOR FINALLY LOADS NEW DATA, TRANSMISSION STARTS IMMEDIATELY AND INTERRUPT OCCURS, INDICATING TRANSMIT DATA REGISTER EMPTY
92CM-36794R1

Fig. 9 - Transmit data register not loaded by processor.

Effect of $\overline{\text{CTS}}$ on Transmitter (Fig. 10)

$\overline{\text{CTS}}$ is the Clear-to-Send signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line immediately goes to the "MARK" condition. Interrupts continue at the same rate, but the Status Register does not indicate that the Transmit Data Register is empty. Since there is no status bit for $\overline{\text{CTS}}$, the processor must deduce that $\overline{\text{CTS}}$ has gone to the False (high) state. This is covered later. $\overline{\text{CTS}}$ is a transmit control line only, and has no effect on the CDP65C51 Receiver Operation.

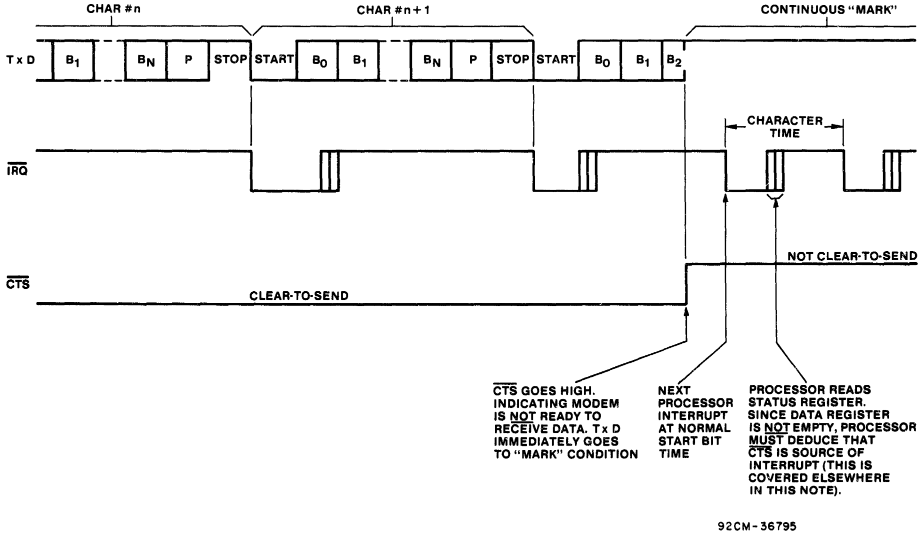

CHAR #n
CHAR #n+1
CONTINUOUS "MARK"
TxD
B_1
B_N
P
STOP
START
B_0
B_1
B_N
P
STOP
START
B_0
B_1
B_2
CHARACTER TIME
$\overline{IRQ}$
NOT CLEAR-TO-SEND
$\overline{CTS}$
CLEAR-TO-SEND
$\overline{CTS}$ GOES HIGH, INDICATING MODEM IS NOT READY TO RECEIVE DATA. TxD IMMEDIATELY GOES TO "MARK" CONDITION
NEXT PROCESSOR INTERRUPT AT NORMAL START BIT TIME
PROCESSOR READS STATUS REGISTER. SINCE DATA REGISTER IS NOT EMPTY, PROCESSOR MUST DEDUCE THAT $\overline{CTS}$ IS SOURCE OF INTERRUPT (THIS IS COVERED ELSEWHERE IN THIS NOTE).
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Fig. 10 - Effect of $\overline{\text{CTS}}$ on transmitter.

CDP65C51 OPERATION (Cont'd)

Effect of Overrun on Receiver (Fig. 11)

If the processor does not read the Receiver Data Register in the allocated time, then, when the following interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost.

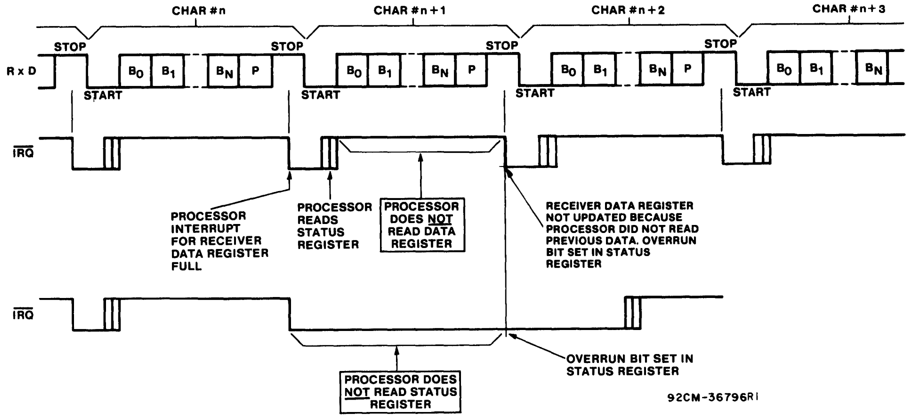
CHAR #n
CHAR #n+1
CHAR #n+2
CHAR #n+3
STOP
STOP
STOP
STOP
RxD
B0
B1
BN
P
START
START
START
START
IRQ
PROCESSOR INTERRUPT FOR RECEIVER DATA REGISTER FULL
PROCESSOR READS STATUS REGISTER
PROCESSOR DOES NOT READ DATA REGISTER
RECEIVER DATA REGISTER NOT UPDATED BECAUSE PROCESSOR DID NOT READ PREVIOUS DATA. OVERRUN BIT SET IN STATUS REGISTER
IRQ
PROCESSOR DOES NOT READ STATUS REGISTER
OVERRUN BIT SET IN STATUS REGISTER
92CM-36796RI

Fig. 11 - *Effect of overrun on receiver.*

Echo Mode Timing (Fig. 12)

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by ½ of the bit time.

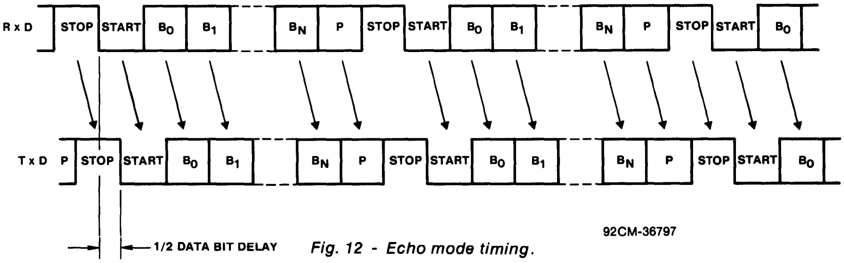

Fig. 12 - *Echo mode timing.*

Effect of $\overline{\text{CTS}}$ on Echo Mode Operation (Fig. 13)

See "Effect of $\overline{\text{CTS}}$ on Transmitter" for the effect of $\overline{\text{CTS}}$ on the Transmitter. Receiver operation is unaffected by $\overline{\text{CTS}}$, so, in Echo Mode, the Transmitter is affected in the same way as "Effect of $\overline{\text{CTS}}$ on Transmitter". In this case however, the processor interrupts signify that the Receiver Data Register is full, so the processor has no way of knowing that the Transmitter has ceased to echo.

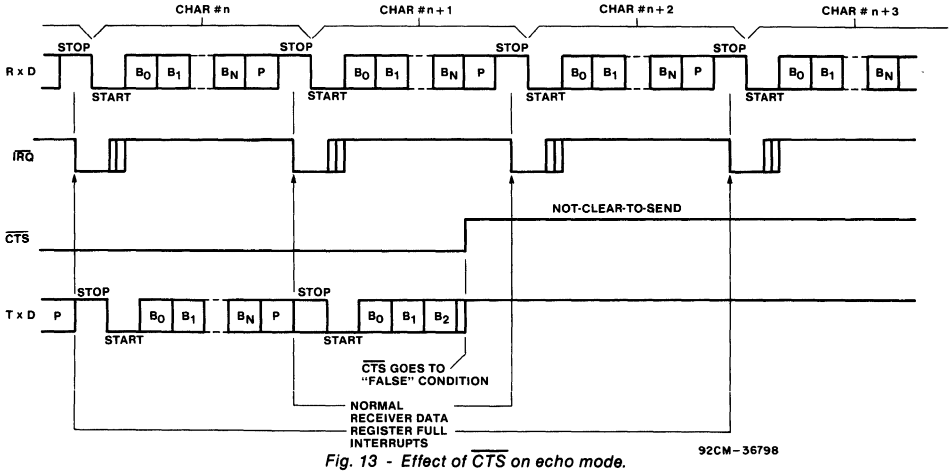

Fig. 13 - *Effect of $\overline{\text{CTS}}$ on echo mode.*

CDP65C51 OPERATION (Cont'd)

Overrun in Echo Mode (Fig. 14)

If Overrun occurs in Echo Mode, the Receiver is affected the same way as described in "Effect of Overrun on Receiver".

For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor.

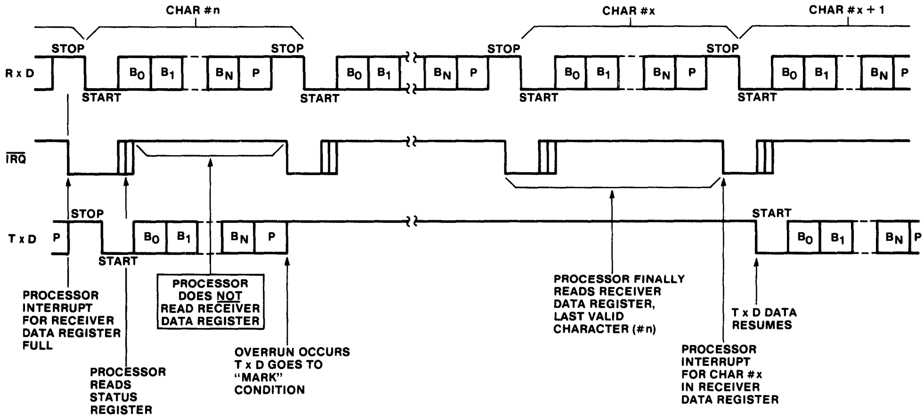
CHAR #n
CHAR #x
CHAR #x + 1
STOP
START
R x D
$\overline{IRQ}$
T x D
B_0
B_1
B_N
P
PROCESSOR INTERRUPT FOR RECEIVER DATA REGISTER FULL
PROCESSOR READS STATUS REGISTER
PROCESSOR DOES NOT READ RECEIVER DATA REGISTER
OVERRUN OCCURS T x D GOES TO "MARK" CONDITION
PROCESSOR FINALLY READS RECEIVER DATA REGISTER, LAST VALID CHARACTER (#n)
PROCESSOR INTERRUPT FOR CHAR #x IN RECEIVER DATA REGISTER
T x D DATA RESUMES

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Fig. 14 - Overrun in echo mode.

Framing Error (Fig. 15)

Framing Error is caused by the absence of Stop Bit(s) on received data. The status bit is set when the processor interrupt occurs. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received.

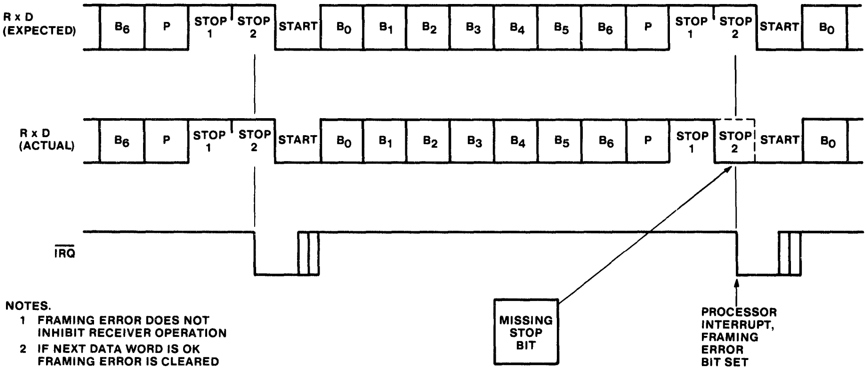
R x D (EXPECTED)
R x D (ACTUAL)
$\overline{IRQ}$
B_0
B_1
B_2
B_3
B_4
B_5
B_6
P
STOP 1
STOP 2
START
MISSING STOP BIT
PROCESSOR INTERRUPT, FRAMING ERROR BIT SET
NOTES.
1 FRAMING ERROR DOES NOT INHIBIT RECEIVER OPERATION
2 IF NEXT DATA WORD IS OK FRAMING ERROR IS CLEARED

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Fig. 15 - Framing error.

CDP65C51 OPERATION (Cont'd)

Effect of $\overline{\text{DCD}}$ on Receiver (Fig. 16)

$\overline{\text{DCD}}$ is a modem output used to indicate the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data (RxD on the CDP65C51 some time later). The CDP65C51 will cause a processor interrupt whenever $\overline{\text{DCD}}$ changes state and will indicate this condition via the Status Register. Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the CDP65C51 automatically checks the level of the $\overline{\text{DCD}}$ line, and if it has changed, another interrupt occurs.

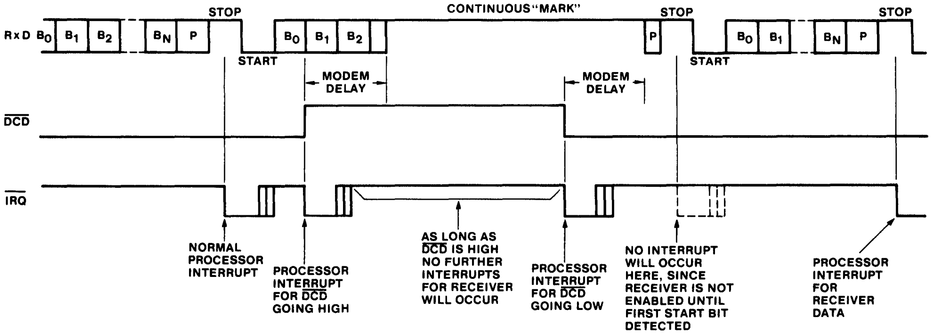
STOP
CONTINUOUS "MARK"
STOP
STOP
RxD
B0
B1
B2
BN
P
B0
B1
B2
P
B0
B1
BN
P
START
MODEM DELAY
MODEM DELAY
START
DCD
IRQ
NORMAL PROCESSOR INTERRUPT
PROCESSOR INTERRUPT FOR DCD GOING HIGH
AS LONG AS DCD IS HIGH NO FURTHER INTERRUPTS FOR RECEIVER WILL OCCUR
PROCESSOR INTERRUPT FOR DCD GOING LOW
NO INTERRUPT WILL OCCUR HERE, SINCE RECEIVER IS NOT ENABLED UNTIL FIRST START BIT DETECTED
PROCESSOR INTERRUPT FOR RECEIVER DATA

Fig. 16 - Effect of $\overline{\text{DCD}}$ on receiver.

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Timing with 1½ Stop Bits (Fig. 17)

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the processor interrupt for Receiver Data Register Full occurs halfway through the trailing half-Stop Bit.

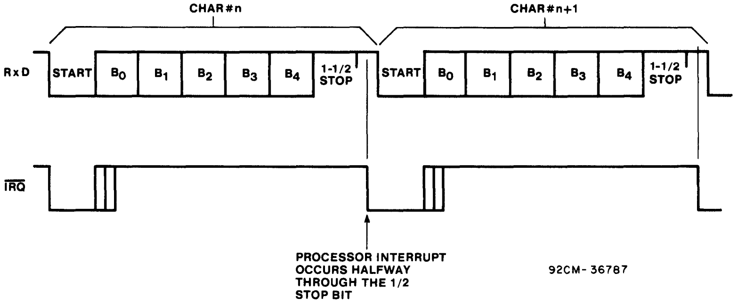

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Fig. 17 - Timing with 1-1/2 stop bits.

Transmit Continuous "BREAK" (Fig. 18)

This mode is selected via the CDP65C51 Command Register and causes the Transmitter to send continuous "BREAK" characters after both the transmitter and transmitter-holding registers have been emptied. When the Command Register is programmed back to normal transmit mode, a Stop Bit is generated and normal transmission continues.

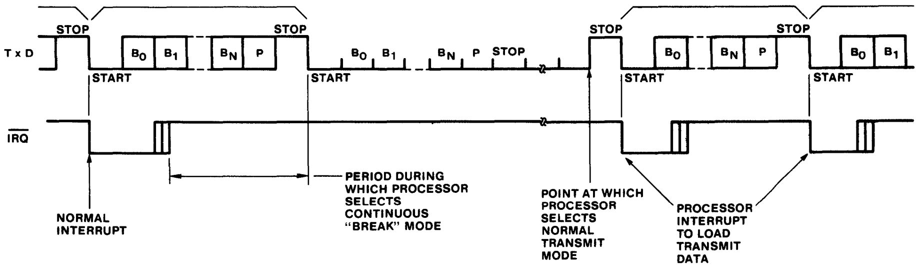
STOP
STOP
STOP
STOP
TxD
B0
B1
BN
P
B0
B1
BN
P
STOP
B0
BN
P
B0
B1
START
START
START
START
IRQ
NORMAL INTERRUPT
PERIOD DURING WHICH PROCESSOR SELECTS CONTINUOUS "BREAK" MODE
POINT AT WHICH PROCESSOR SELECTS NORMAL TRANSMIT MODE
PROCESSOR INTERRUPT TO LOAD TRANSMIT DATA

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Fig. 18 - Transmit continuous "BREAK".

CDP65C51 OPERATION (Cont'd)

Receive Continuous "BREAK" (Fig. 19)

In the event the modem transmits continuous "BREAK" characters, the CDP65C51 will terminate receiving. Reception will resume only after a Stop Bit is encountered by the CDP65C51.

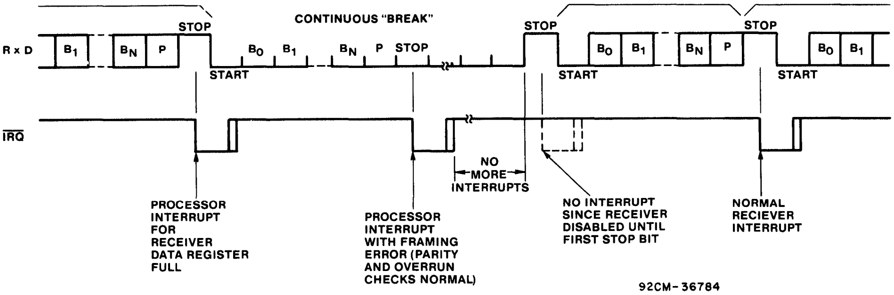

STOP
CONTINUOUS "BREAK"
STOP
STOP
R x D
B_1
B_N
P
B_0
B_1
B_N
P
STOP
B_0
B_1
B_N
P
B_0
B_1
START
START
START
$\overline{\text{IRQ}}$
NO MORE INTERRUPTS
PROCESSOR INTERRUPT FOR RECEIVER DATA REGISTER FULL
PROCESSOR INTERRUPT WITH FRAMING ERROR (PARITY AND OVERRUN CHECKS NORMAL)
NO INTERRUPT SINCE RECEIVER DISABLED UNTIL FIRST STOP BIT
NORMAL RECIEVER INTERRUPT
92CM-36784

Fig. 19 - Receive continuous "BREAK".

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the CDP65C51 should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 (IRQ). Subsequent transitions on $\overline{\text{DSR}}$ and $\overline{\text{DCD}}$ will cause another interrupt

2. Check IRQ Bit

   If not set, interrupt source is not the CDP65C51.

3. Check $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both "0" (modem "on-line") and they are unchanged then the remaining bits must be checked.

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2)

   Only if Receiver Data Register is Full.

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

7. If none of the above, then $\overline{\text{CTS}}$ must have gone to the False (high) state

PROGRAMMED RESET OPERATION

A program reset occurs when the processor performs a write operation to the CDP65C51 with RS0 high and RS1 low. The program reset operates somewhat different from the hardware reset ($\overline{\text{RES}}$ pin) and is described as follows:

1. Internal registers are not completely cleared. The data sheet indicates the effect of a program reset on internal registers.
2. The $\overline{\text{DTR}}$ line goes high immediately.
3. Receiver and transmitter interrupts are disabled immediately. If $\overline{\text{IRQ}}$ is low when the reset occurs, it stays low until serviced, unless interrupt was caused by $\overline{\text{DCD}}$ or $\overline{\text{DSR}}$ transition.
4. $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ interrupts disabled immediately. If $\overline{\text{IRQ}}$ is low and was caused by $\overline{\text{DCD}}$ or $\overline{\text{DSR}}$, then it goes high, also $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ status bits subsequently will follow the input lines, although no interrupt will occur.
5. Overrun cleared, if set.

MISCELLANEOUS NOTES ON OPERATION

1. If Echo Mode is selected, $\overline{\text{RTS}}$ goes low.
2. If Bit 0 of Command Register is "0" (disabled), then·
   a) All interrupts disabled, including those caused by $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ transitions.
   b) Receiver disabled, but a character currently being received will be completed first.
   c) Transmitter is disabled after both the Transmit Data and Transmit Shift Registers have been emptied.
3. Odd parity occurs when the sum of all the "1" bits in the data word (including the parity bit) is odd.
4. In the Receive Mode, the received parity bit does not go into the Receiver Data Register, but is used to generate parity error for the Status Register.
5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.
6. If the RxD line inadvertently goes low and then high during the first 9 receiver clocks after a Stop Bit; a false Start Bit will result.

   For false Start Bit detection, the CDP65C51 does not begin to receive data, instead, only a true Start Bit initiates receiver operation.

7. A precaution to consider with the crystal oscillator circuit is:

   The XTLI input may be used as an external clock input. The XTLO pin must be floating and may not be used for any other function.

8. $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ transitions, although causing immediate processor interrupts, have no effect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be terminated either to Gnd or V_{DD}.

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the CDP65C51 Control Register.

The divisors, then, are determined by bits 0-3 in the Control Register and their values are shown in Table II.

CDP65C51 OPERATION (Cont'd)

Table II - Divisor Selection for the CDP65C51

CONTROL REGISTER BITS				DIVISOR SELECTED FOR THE INTERNAL COUNTER	BAUD RATE GENERATED WITH 1.8432 MHz	BAUD RATE GENERATED WITH FREQUENCY (F)
3	**2**	**1**	**0**			
0	0	0	0	No Divisor Selected	1/16 of External Clock at Pin XTLI	1/16 of External Clock at Pin XTLI
0	0	0	1	36,864	$\frac{1.8432 \times 10^6}{36,864} = 50$	$\frac{F}{36,864}$
0	0	1	0	24,576	$\frac{1.8432 \times 10^6}{24,576} = 75$	$\frac{F}{24,576}$
0	0	1	1	16,768	$\frac{1.8432 \times 10^6}{16,768} = 109.92$	$\frac{F}{16,768}$
0	1	0	0	13,696	$\frac{1.8432 \times 10^6}{13,696} = 134.58$	$\frac{F}{13,696}$
0	1	0	1	12,288	$\frac{1.8432 \times 10^6}{12,288} = 150$	$\frac{F}{12,288}$
0	1	1	0	6,144	$\frac{1.8432 \times 10^6}{6,144} = 300$	$\frac{F}{6,144}$
0	1	1	1	3,072	$\frac{1.8432 \times 10^6}{3,072} = 600$	$\frac{F}{3,072}$
1	0	0	0	1,536	$\frac{1.8432 \times 10^6}{1,536} = 1200$	$\frac{F}{1,536}$
1	0	0	1	1,024	$\frac{1.8432 \times 10^6}{1,024} = 1800$	$\frac{F}{1,024}$
1	0	1	0	768	$\frac{1.8432 \times 10^6}{768} = 2400$	$\frac{F}{768}$
1	0	1	1	512	$\frac{1.8432 \times 10^6}{512} = 3600$	$\frac{F}{512}$
1	1	0	0	384	$\frac{1.8432 \times 10^6}{384} = 4800$	$\frac{F}{384}$
1	1	0	1	256	$\frac{1.8432 \times 10^6}{256} = 7200$	$\frac{F}{256}$
1	1	1	0	192	$\frac{1.8432 \times 10^6}{192} = 9600$	$\frac{F}{192}$
1	1	1	1	96	$\frac{1.8432 \times 10^6}{96} = 19200$	$\frac{F}{96}$

Generating Other Baud Rates

By using a different crystal, other baud rates may be generated These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the CDP65C51 with an off-chip oscillator to achieve the same thing. In this case, XTLI (pin 6) must be the clock input and XTLO (pin 7) must be a no-connect.

DIAGNOSTIC LOOP—BACK OPERATING MODES

A simplified block diagram for a system incorporating a CDP65C51 ACIA is shown in Fig. 20.

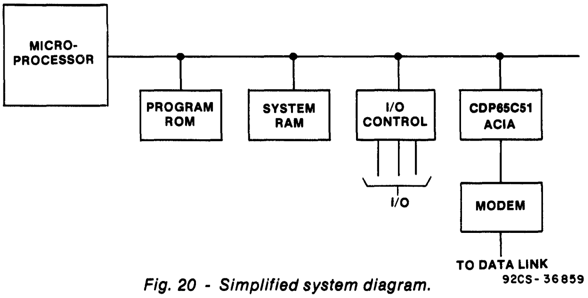


Fig. 20 - Simplified system diagram.

CDP65C51 OPERATION (Cont'd)

Occasionally it may be desirable to include in the system a facility for "loop-back" diagnostic testing, of which there are two kinds:

1. Local Loop-Back

   Loop-back from the point of view of the processor. In this case, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

2. Remote Loop-Back

   Loop-back from the point of view of the Data Link and Modem. In this case, the processor, itself, is disconnected and all received data is immediately retransmitted, so the system on the other end of the Data Link may operate independent of the local system.

The CDP65C51 does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry.

Fig. 21 indicates the necessary logic to be used with the CDP65C51.

The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

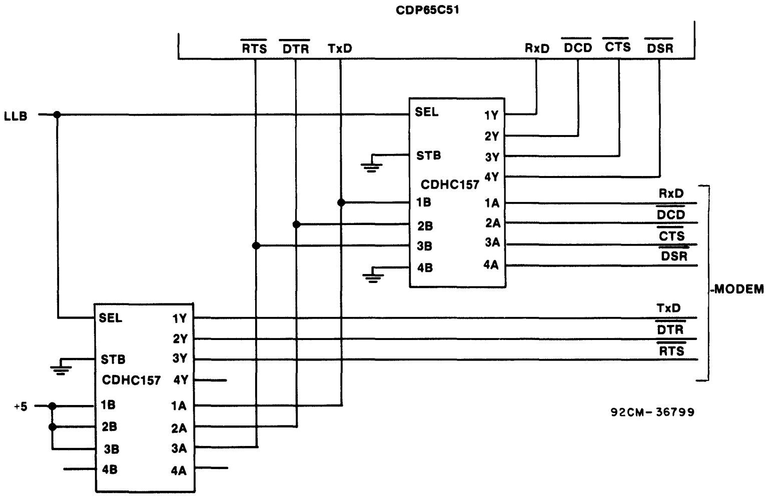
1. Disables outputs TxD, $\overline{\text{DTR}}$, and $\overline{\text{RTS}}$ (to Modem).
2. Disables inputs RxD, $\overline{\text{DCD}}$, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs:
   a) TxD to RxD
   b) $\overline{\text{DTR}}$ to $\overline{\text{DCD}}$
   c) $\overline{\text{RTS}}$ to $\overline{\text{CTS}}$

LLB may be tied to a peripheral control pin to provide processor control of local loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

Remote loop-back does not require this circuitry, so LLB must be set low. However, the processor must select the following:

1. Control Register bit 4 must be "1", so that the transmitter clock = receiver clock.
2. Command Register bit 4 must be "1" to select Echo Mode.
3. Command Register bits 3 and 2 must be "1" and "0", respectively, to disable transmitter interrupts.
4. Command Register bit 1 must be "0" to disable receiver interrupts.

In this way, the system retransmits received data without any effect on the local system.



NOTES: 1. HIGH ON LLB SELECTS LOCAL LOOP-BACK MODE.
2. HIGH ON HC157 SELECT INPUT GATES "B" INPUTS TO "Y" OUTPUTS; LOW GATES "A" TO "Y".

Fig. 21 - Loop-back circuit schematic.

DYNAMIC ELECTRICAL CHARACTERISTICS—READ/WRITE CYCLE
V_{DD} = 5V ± 5%, T_A = -40 to +85° C, C_L = 75 pF

CHARACTERISTIC		LIMITS						UNITS
		CDP65C51-1		CDP65C51-2		CDP65C51-4		
		Min.	Max.	Min.	Max.	Min.	Max.	
Cycle Time	t_{CYC}	1	—	0.5	—	0.25	—	µs
ϕ2 Pulse Width	t_C	400	—	200	—	100	—	ns
Address Set-Up Time	t_{AC}	120	—	60	—	30	—	ns
Address Hold Time	t_{CAH}	0	—	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WC}	120	—	60	—	30	—	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	—	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	120	—	60	—	35	—	ns
Data Bus Hold Time	t_{HW}	20	—	10	—	5	—	ns
Read Access Time (Valid Data)	t_{CDR}	—	200	—	150	—	50	ns
Read Hold Time	t_{HR}	20	—	10	—	10	—	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	—	20	—	10	—	ns

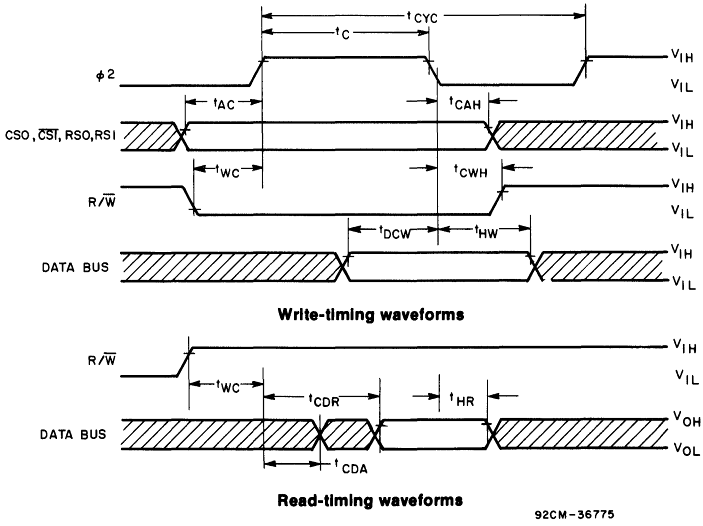


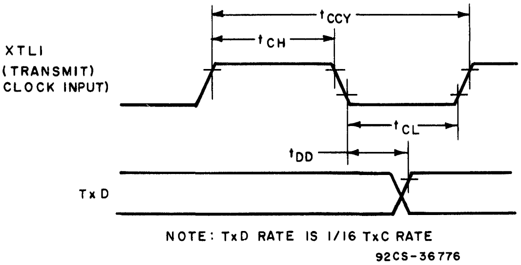
Fig. 22 - Timing waveforms

DYNAMIC ELECTRICAL CHARACTERISTICS—TRANSMIT/RECEIVE, See Figs. 23, 24 and 25.
V_{DD} = 5V ± 5%, T_A = -40 to +85° C

CHARACTERISTIC		LIMITS						UNITS
		CDP65C51-1		CDP65C51-2		CDP65C51-4		
		Min.	Max.	Min.	Max.	Min.	Max.	
Transmit/Receive Clock Rate	t_{CCY}	400*	—	325	—	250	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	145	—	110	—	
Transmit/Receive Clock Low Time	t_{CL}	175	—	145	—	110	—	
$\overline{\text{XTLI}}$ to TxD Propagation Delay	t_{DD}	—	500	—	410	—	315	
$\overline{\text{RTS}}$ Propagation Delay	t_{DLY}	—	500	—	410	—	315	
$\overline{\text{IRQ}}$ Propagation Delay (Clear)	$t_{\overline{IRQ}}$	—	500	—	410	—	315	
$\overline{\text{RES}}$ Pulse Width	$t_{\overline{RES}}$	400	—	300	—	200	—	

(t_r,t_f = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate=$\frac{1}{16 \times T_{CCY}}$



NOTE: TxD RATE IS 1/16 TxC RATE

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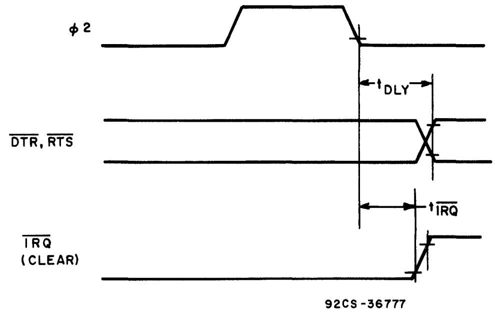
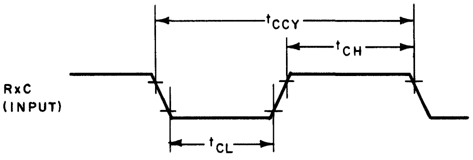
Fig. 23 - Transmit-timing waveforms with external clock.



92CS-36777

Fig. 24 - Interrupt-and output-timing waveforms.



NOTE: RxD RATE IS 1/16 RxC RATE

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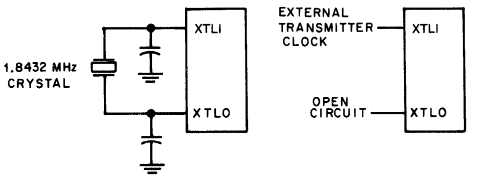
Fig. 25 - Receive external clock timing waveforms.



C = 10-50 pF

INTERNAL CLOCK

EXTERNAL CLOCK

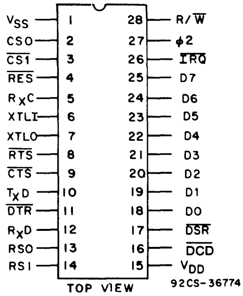
92CS-42341

Fig. 26 - Transmitter clock generation.

Advance Information

CDP65C51A

TERMINAL ASSIGNMENT



CMOS Asynchronous Communications Interface Adapter (ACIA)

Features:

- *Compatible with 8-bit microprocessors*
- *Full duplex operation with buffered receiver and transmitter*
- *Data set/modem control functions*
- *Internal baud-rate generator with 15 programmable baud rates (50 to 19,200)*
- *Program-selectable internally or externally controlled receiver rate*
- *Operates at baud rates up to 250,000 via proper crystal or clock selection*

The RCA-CDP65C51A Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program-controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems. The CDP65C51A is identical to the RCA-CDP65C51 except for the implementation of the $\overline{CTS}$ function. If a not-clear-to-send signal is received during the transmission of a character, the CDP65C51A will first allow completion of that transmission, and then disable the transmitter.

The CDP65C51A has an internal baud-rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or 1/16 times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at 1/16 times an external clock rate. The CDP65C51A has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, 1½, or 2 stop bits.

The CDP65C51A is designed for maximum programmed control from the CPU, to simplify hardware implementation. Three separate registers permit the CPU to easily select the CDP65C51A operating modes and data-checking parameters and determine operational status.

The **Command Register** controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{RTS}$ line, receiver interrupt control, and the state of the $\overline{DTR}$ line.

- *Programmable word lengths, number of stop bits, and parity-bit generation and detection*
- *Programmable interrupt control*
- *Program reset*
- *Program-selectable serial echo mode*
- *Two chip selects*
- *4 MHz, 2 MHz or 1 MHz operation (CDP65C51A-4, CDP65C51A-2, CDP65C51A-1, respectively)*
- *Single 3 V to 6 V power supply*
- *Full TTL compatibility*
- *Synchronous $\overline{CTS}$ operation*

The **Control Register** controls the number of stop bits, word length, receiver clock source, and baud rate.

The **Status Register** indicates the states of the $\overline{IRQ}$, $\overline{DSR}$, and $\overline{DCD}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing, and Parity Error conditions.

The Transmitter and Receiver Data Registers are used for temporary data storage by the CDP65C51A Transmit and Receive circuits.

The CDP65C51A-1, CDP65C51A-2, and CDP65C51A-4 are capable of interfacing with microprocessors with cycle times of 1 MHz, 2 MHz and 4 MHz, respectively.

The CDP65C51A is supplied in 28-lead, hermetic, dual-in-line side brazed ceramic packages (D suffix), in 28-lead, dual-in-line plastic packages (E suffix) and in 28-lead dual-in-line small-outline (SO) packages (M) suffix.

File Number **1928**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltage referenced to V_{SS} terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +85°C (PACKAGE TYPE M)*	425 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A).	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E and M	-40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

RECOMMENDED OPERATING CONDITIONS at T_A = -40° to +85°C
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating Voltage Range	3	6	V
Input Voltage Range	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40° to +85°C, V_{DD} = 5V ± 5%

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Quiescent Device Current	I_{DD}	—	50	200	µA
Output Low Current (Sinking): V_{OL} = 0.4 V (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$	I_{OL}	1.6	—	—	mA
Output High Current (Sourcing): V_{OH} = 4.6 V (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	I_{OH}	-1.6	—	—	mA
Output Low Voltage: I_{LOAD} = 1.6 mA (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	—	—	0.4	V
Output High Voltage: I_{LOAD} = -1.6 mA (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	V_{OH}	4.6	—	—	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Input High Voltage	V_{IH}				V
(Except XTLI and XTLO)		2	—	V_{DD}	
(XTLI and XTLO)		3	—	V_{DD}	
Input Leakage Current: V_{IN} = 0 to 5 V (ϕ2, R/$\overline{W}$, $\overline{RES}$, CS0, $\overline{CS1}$, RS0, RS1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	—	—	±1	µA
Input Leakage Current for High Impedance State (D0-D7)	I_{TSI}	—	—	±1.2	µA
Output Leakage Current (off state): V_{OUT} = 5 V ($\overline{IRQ}$)	I_{OFF}	—	—	2	µA
Input Capacitance (except XTLI and XTLO)	C_{IN}	—	—	10	pF
Output Capacitance	C_{OUT}	—	—	10	pF

CDP65C51A INTERFACE REQUIREMENTS

This section describes the interface requirements for the CDP65C51A ACIA. Fig. 1 is the Interface Diagram and the Terminal Diagram shows the pin-out configuration for the CDP65C51A.

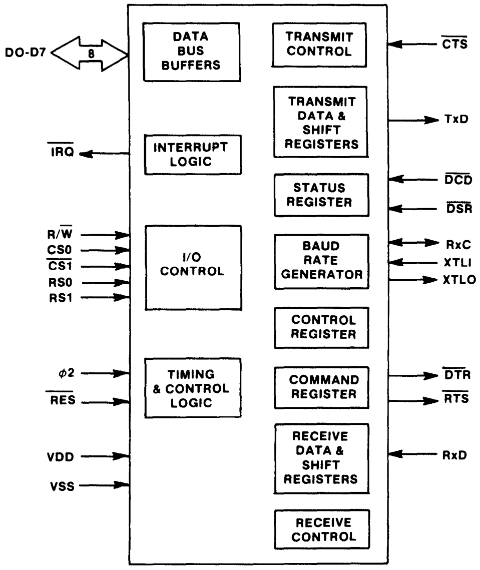


Fig. 1 - CDP65C51A interface diagram.

MICROPROCESSOR INTERFACE SIGNAL DESCRIPTION

$\overline{\text{RES}}$ (Reset) (4)

During system initialization a low on the $\overline{\text{RES}}$ input will cause a hardware reset to occur. The Command Register and the Control Register will be cleared. The Status Register will be cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the $\overline{\text{DSR}}$ and $\overline{\text{DCD}}$ lines, and the transmitter Empty bit, which will be set. A hardware reset is required after power-up.

ϕ2 (Input Clock) (27)

The input clock is the system ϕ2 clock and is used to clock all data transfers between the system microprocessor and the CDP65C51A.

R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$) (28)

The R/$\overline{\text{W}}$ input, generated by the microprocessor, is used to control the direction of data transfers. A high on the R/$\overline{\text{W}}$ pin allows the processor to read the data supplied by the CDP65C51A, a low allows a write to the CDP65C51A.

$\overline{\text{IRQ}}$ (Interrupt Request) (26)

The $\overline{\text{IRQ}}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{\text{IRQ}}$ microprocessor input. Normally at high level, $\overline{\text{IRQ}}$ goes low when an interrupt occurs.

D0-D7 (Data Bus) (18-25)

The D0-D7 pins are the eight data lines used to transfer data between the processor and the CDP65C51A. These lines are bi-directional and are normally high-impedance except during Read cycles when the CDP65C51A is selected.

CS0, $\overline{\text{CS1}}$ (Chip Selects) (2, 3)

The two chip-select inputs are normally connected to the processor address lines either directly or through decoders. The CDP65C51A is selected when CS0 is high and $\overline{\text{CS1}}$ is low.

RS0, RS1 (Register Selects) (13, 14)

The two register-select lines are normally connected to the processor address lines to allow the processor to select the various CDP65C51A internal registers. The following table shows the internal register-select coding.

TABLE I

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command Register and bit 2 in the Status Register. The Control Register is unchanged by a Programmed Reset. It should be noted that the Programmed Reset is slightly different from the Hardware Reset ($\overline{\text{RES}}$); these differences are shown in Figs. 3, 4 and 5.

ACIA/MODEM INTERFACE SIGNAL DESCRIPTION

XTLI, XTLO (Crystal Pins) (6, 7)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates (see "Generation of Non-Standard Baud Rates"). Alternatively, an externally generated clock may be used to drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

TxD (Transmit Data) (10)

The TxD output line is used to transfer serial NRZ (nonreturn-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or under control of an external clock. This selection is made by programming the Control Register.

RxD (Receive Data) (12)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or under the control of an externally generated receiver clock. The selection is made by programming the Control Register.

CDP65C51A INTERFACE REQUIREMENTS (Cont'd)

ACIA/MODEM INTERFACE SIGNAL DESCRIPTION (Cont'd)

RxC (Receive Clock) (5)

The RxC is a bi-directional pin which serves as either the receiver 16X clock input or the receiver 16X clock output. The latter mode results if the internal baud-rate generator is selected for receiver data clocking.

$\overline{\text{RTS}}$ (Request to Send) (8)

The $\overline{\text{RTS}}$ output pin is used to control the modem from the processor. The state of the $\overline{\text{RTS}}$ pin is determined by the contents of the Command Register.

$\overline{\text{CTS}}$ (Clear to Send) (9)

The $\overline{\text{CTS}}$ input pin is used to control the transmitter operation. The enable state is with $\overline{\text{CTS}}$ low. The transmitter is automatically disabled if $\overline{\text{CTS}}$ is high.

$\overline{\text{DTR}}$ (Data Terminal Ready) (11)

This output pin is used to indicate the status of the CDP65C51A to the modem. A low on $\overline{\text{DTR}}$ indicates the CDP65C51A is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{\text{DSR}}$ (Data Set Ready) (17)

The $\overline{\text{DSR}}$ input pin is used to indicate to the CDP65C51A the status of the modem. A low indicates the "ready" state and a high, "not-ready".

$\overline{\text{DCD}}$ (Data Carrier Detect) (16)

The $\overline{\text{DCD}}$ input pin is used to indicate to the CDP65C51A the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

CDP65C51A INTERNAL ORGANIZATION

This section provides a functional description of the CDP65C51A. A block diagram of the CDP65C51A is presented in Fig. 2.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the R/$\overline{\text{W}}$ line is high and the chip is selected, the Data Bus Buffer passes the data to the system data lines from the CDP65C51A internal data bus. When the R/$\overline{\text{W}}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the system data bus to the internal data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{\text{IRQ}}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{\text{DCD}}$) logic and the Data Set Ready ($\overline{\text{DSR}}$) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers in preparation for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Register Select and Chip Select and Read/Write lines as described in Table I, previously.

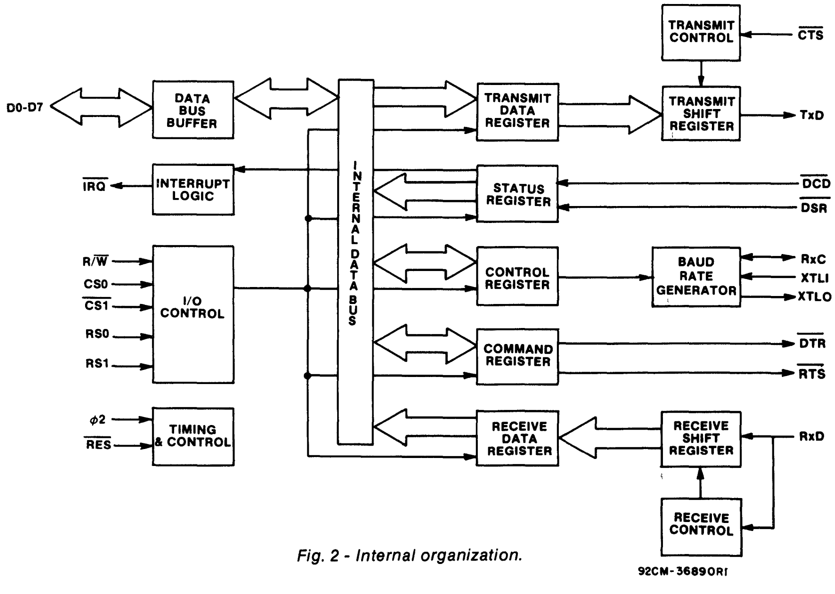


Fig. 2 - Internal organization.

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CDP65C51A INTERNAL ORGANIZATION (Cont'd)

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus and the registers, the Data Bus Buffer, and the microprocessor data bus, and the hardware reset features.

Timing is controlled by the system $\phi 2$ clock input. The chip will perform data transfers to or from the microcomputer data bus during the $\phi 2$ high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{RES}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the CDP65C51A Transmit and Receive circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care".

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

STATUS REGISTER

Fig. 3 indicates the format of the CDP65C51A Status Register. A description of each status bit follows.

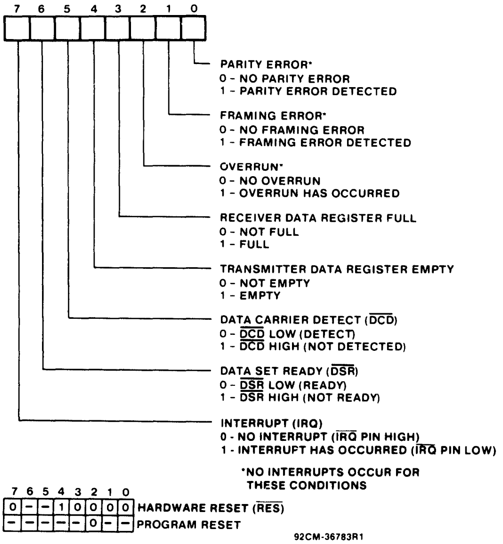

7 6 5 4 3 2 1 0
PARITY ERROR*
0 - NO PARITY ERROR
1 - PARITY ERROR DETECTED
FRAMING ERROR*
0 - NO FRAMING ERROR
1 - FRAMING ERROR DETECTED
OVERRUN*
0 - NO OVERRUN
1 - OVERRUN HAS OCCURRED
RECEIVER DATA REGISTER FULL
0 - NOT FULL
1 - FULL
TRANSMITTER DATA REGISTER EMPTY
0 - NOT EMPTY
1 - EMPTY
DATA CARRIER DETECT (DCD)
0 - DCD LOW (DETECT)
1 - DCD HIGH (NOT DETECTED)
DATA SET READY (DSR)
0 - DSR LOW (READY)
1 - DSR HIGH (NOT READY)
INTERRUPT (IRQ)
0 - NO INTERRUPT (IRQ PIN HIGH)
1 - INTERRUPT HAS OCCURRED (IRQ PIN LOW)
*NO INTERRUPTS OCCUR FOR THESE CONDITIONS
7 6 5 4 3 2 1 0
0 - - 1 0 0 0 0 HARDWARE RESET (RES)
- - - - - 0 - - PROGRAM RESET
92CM-36783R1

Fig. 3 - Status register format.

Receiver Data Register Full (Bit 3)

This bit goes to a "1" when the CDP65C51A transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a "0" when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a "1" when the CDP65C51A transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a "0" when the processor writes new data onto the Transmitter Data Register.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the CDP65C51A. A "0" indicates a low level (true condition) and a "1" indicates a high (false). Whenever either of these inputs changes state, an immediate processor interrupt occurs, unless the CDP65C51A is disabled (bit 0 of the Command Register is a "0"). When the interrupt occurs, the status bits will indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until the Status Register is interrogated by the processor. At that time, another interrupt will immediately occur and the status bits will reflect the new input levels.

Framing Error (Bit 1), Overrun (Bit 2), and Parity Error (Bit 0)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified.

Interrupt (Bit 7)

This bit goes to a "0" when the Status Register has been read by the processor, and goes to a "1" whenever any kind of interrupt occurs.

CONTROL REGISTER

The Control Register selects the desired transmitter baud rate, receiver clock source, word length, and the number of stop bits.

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits, set by the processor, select the Transmitter baud rate, which can be at 1/16 an external clock rate or one of 15 other rates controlled by the internal baud rate generator as shown in Fig. 4.

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A "0" causes the Receiver to operate at a baud rate of 1/16 an external clock. A "1" causes the Receiver to operate at the same baud rate as is selected for the transmitter as shown in Fig. 4.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits). Fig. 4 shows the configuration for each number of bits desired.

CDP65C51A

CDP65C51A INTERNAL ORGANIZATION (Cont'd)

CONTROL REGISTER (Cont'd)

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A "0" always indicates one stop bit. A "1" indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, and 2 stop bits in all other configurations.

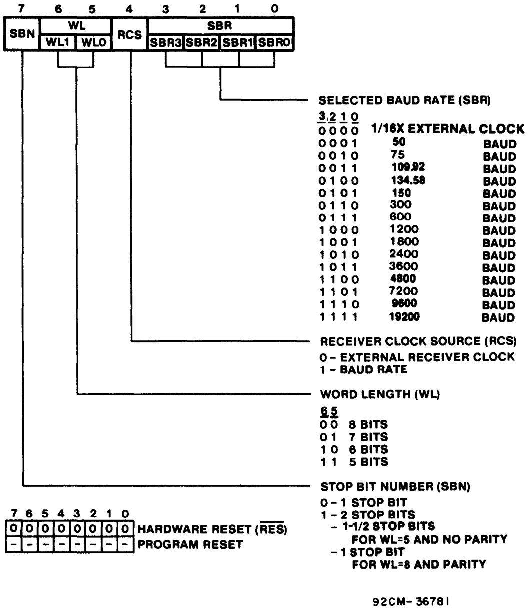


Fig. 4 - CDP65C51A control register.

COMMAND REGISTER

The Command Register controls specific modes and functions (Fig. 5).

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{\text{DTR}}$) line. A "0" indicates the microcomputer system is not ready by setting the $\overline{\text{DTR}}$ line high. A "1" indicates the microcomputer system is ready by setting the $\overline{\text{DTR}}$ line low. When the DTR bit is set to a "0", the receiver and transmitter are both disabled.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a "1". The Receiver interrupt is enabled when this bit is set to a "0" and Bit 0 is set to a "1".

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{\text{RTS}}$) line and the Transmitter interrupt. Fig. 5 shows the various configurations of the $\overline{\text{RTS}}$ line and Transmit Interrupt bit settings.

Receiver Echo Mode (Bit 4)

This bit enables the Receiver Echo Mode. Bits 2 and 3 must be zero. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by ½ bit time. A "1" enables the Receiver Echo Mode. A "0" bit disables the mode.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A "0" disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A "1" bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check). Fig. 5 shows the possible bit configurations for the Parity Mode Control bits.

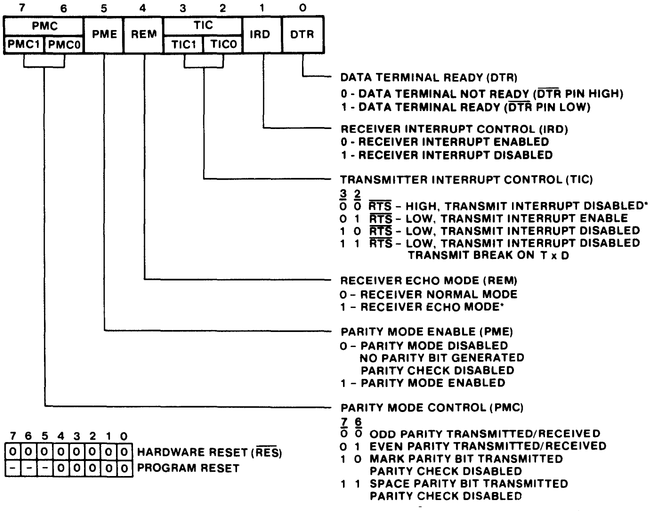

7 6 5 4 3 2 1 0
PMC
PMC1
PMC0
PME
REM
TIC
TIC1
TIC0
IRD
DTR
DATA TERMINAL READY (DTR)
0 - DATA TERMINAL NOT READY (DTR PIN HIGH)
1 - DATA TERMINAL READY (DTR PIN LOW)
RECEIVER INTERRUPT CONTROL (IRD)
0 - RECEIVER INTERRUPT ENABLED
1 - RECEIVER INTERRUPT DISABLED
TRANSMITTER INTERRUPT CONTROL (TIC)
3 2
0 0 RTS - HIGH, TRANSMIT INTERRUPT DISABLED*
0 1 RTS - LOW, TRANSMIT INTERRUPT ENABLE
1 0 RTS - LOW, TRANSMIT INTERRUPT DISABLED
1 1 RTS - LOW, TRANSMIT INTERRUPT DISABLED TRANSMIT BREAK ON T x D
RECEIVER ECHO MODE (REM)
0 - RECEIVER NORMAL MODE
1 - RECEIVER ECHO MODE*
PARITY MODE ENABLE (PME)
0 - PARITY MODE DISABLED NO PARITY BIT GENERATED PARITY CHECK DISABLED
1 - PARITY MODE ENABLED
PARITY MODE CONTROL (PMC)
7 6
0 0 ODD PARITY TRANSMITTED/RECEIVED
0 1 EVEN PARITY TRANSMITTED/RECEIVED
1 0 MARK PARITY BIT TRANSMITTED PARITY CHECK DISABLED
1 1 SPACE PARITY BIT TRANSMITTED PARITY CHECK DISABLED
7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0 HARDWARE RESET (RES)
- - - 0 0 0 0 0 PROGRAM RESET
* BITS 2 AND 3 MUST BE ZERO FOR RECEIVER ECHO MODE RTS WILL BE LOW
92CM-36790R1

Fig. 5 - CDP65C51A command register.

CDP65C51A INTERNAL ORGANIZATION (Cont'd)

TRANSMITTER AND RECEIVER

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the CDP65C51A. Fig. 6 shows the Transmitter and Receiver layout.

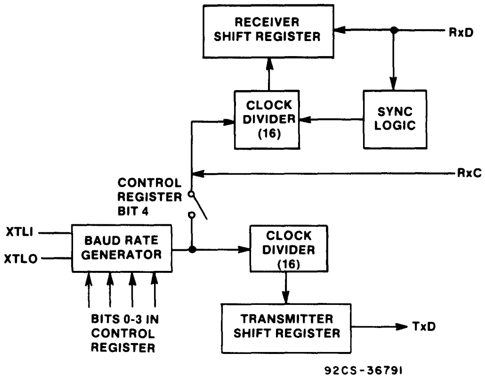


Fig. 6 - Transmitter receiver clock circuits.

CDP65C51A OPERATION

TRANSMITTER AND RECEIVER OPERATION

Continuous Data Transmit (Fig. 7)

In the normal operating mode, the processor interrupt ($\overline{IRQ}$) is used to signal when the CDP65C51A is ready to accept the next data word to be transmitted. This interrupt occurs at the beginnning of the Start Bit. When the processor reads the Status Register of the CDP65C51A, the interrupt is cleared. The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted.

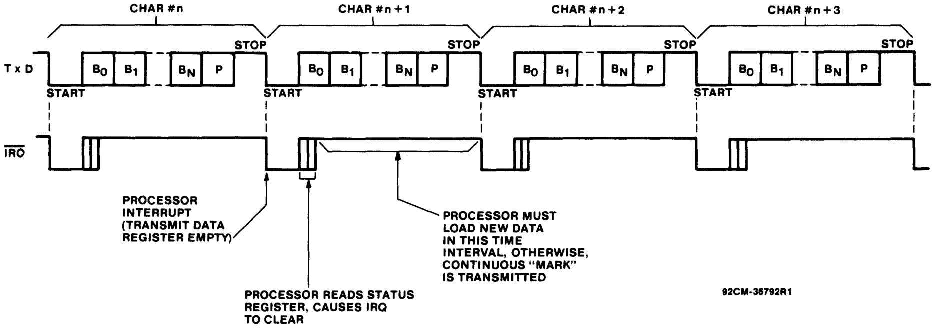

CHAR #n
CHAR #n+1
CHAR #n+2
CHAR #n+3
STOP
TxD
B0
B1
BN
P
START
IRQ
PROCESSOR INTERRUPT (TRANSMIT DATA REGISTER EMPTY)
PROCESSOR MUST LOAD NEW DATA IN THIS TIME INTERVAL, OTHERWISE, CONTINUOUS "MARK" IS TRANSMITTED
PROCESSOR READS STATUS REGISTER, CAUSES IRQ TO CLEAR
92CM-36792R1

Fig. 7 - Continuous data transmit.

CDP65C51A OPERATION (Cont'd)

TRANSMITTER AND RECEIVER OPERATION (Cont'd)

Continuous Data Receive (Fig. 8)

Similar to the above case, the normal mode is to generate a processor interrupt when the CDP65C51A has received a full data word. This occurs at about the 8/16 point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the Overrun condition occurs.

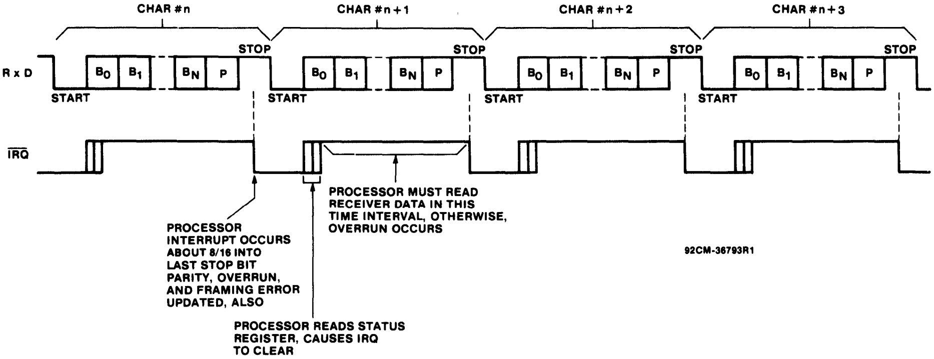

CHAR #n
CHAR #n+1
CHAR #n+2
CHAR #n+3
STOP
RxD
B0
B1
BN
P
START
IRQ
PROCESSOR MUST READ RECEIVER DATA IN THIS TIME INTERVAL, OTHERWISE, OVERRUN OCCURS
PROCESSOR INTERRUPT OCCURS ABOUT 8/16 INTO LAST STOP BIT PARITY, OVERRUN, AND FRAMING ERROR UPDATED, ALSO
PROCESSOR READS STATUS REGISTER, CAUSES IRQ TO CLEAR
92CM-36793R1

Fig. 8 - Continuous data receive.

Transmit Data Register Not Loaded By Processor (Fig. 9)

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line will go to the "MARK" condition until the data is loaded. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word.

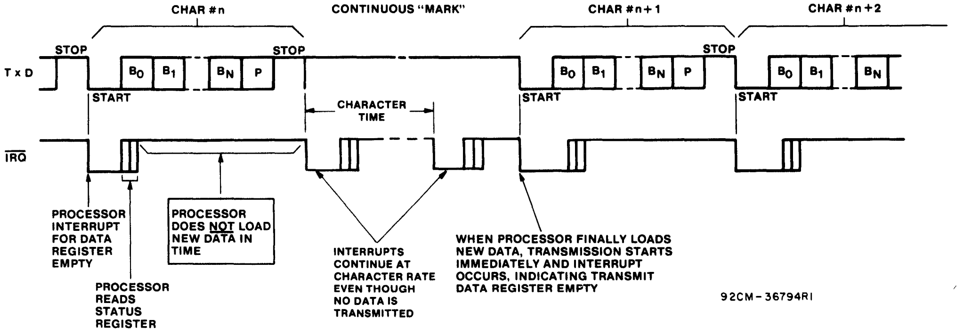

CHAR #n
CONTINUOUS "MARK"
CHAR #n+1
CHAR #n+2
STOP
TxD
B0
B1
BN
P
START
CHARACTER TIME
IRQ
PROCESSOR INTERRUPT FOR DATA REGISTER EMPTY
PROCESSOR DOES NOT LOAD NEW DATA IN TIME
PROCESSOR READS STATUS REGISTER
INTERRUPTS CONTINUE AT CHARACTER RATE EVEN THOUGH NO DATA IS TRANSMITTED
WHEN PROCESSOR FINALLY LOADS NEW DATA, TRANSMISSION STARTS IMMEDIATELY AND INTERRUPT OCCURS, INDICATING TRANSMIT DATA REGISTER EMPTY
92CM-36794RI

Fig. 9 - Transmit data register not loaded by processor.

CDP65C51A OPERATION (Cont'd)

TRANSMITTER AND RECEIVER OPERATION (Cont'd)

Effect of $\overline{\text{CTS}}$ on Transmitter (Fig. 10)

$\overline{\text{CTS}}$ is the Clear-to-Send signal generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line goes to the "MARK" condition following the complete transmission of any character which is currently being shifted out of the Transmitter Shift Register. Since there is no status bit for $\overline{\text{CTS}}$, the processor must deduce that $\overline{\text{CTS}}$ has gone to the False (high) state. This is covered later. $\overline{\text{CTS}}$ is a transmit control line only, and has no effect on the CDP65C51A Receiver Operation. Normal transmission will resume when $\overline{\text{CTS}}$ goes low again.

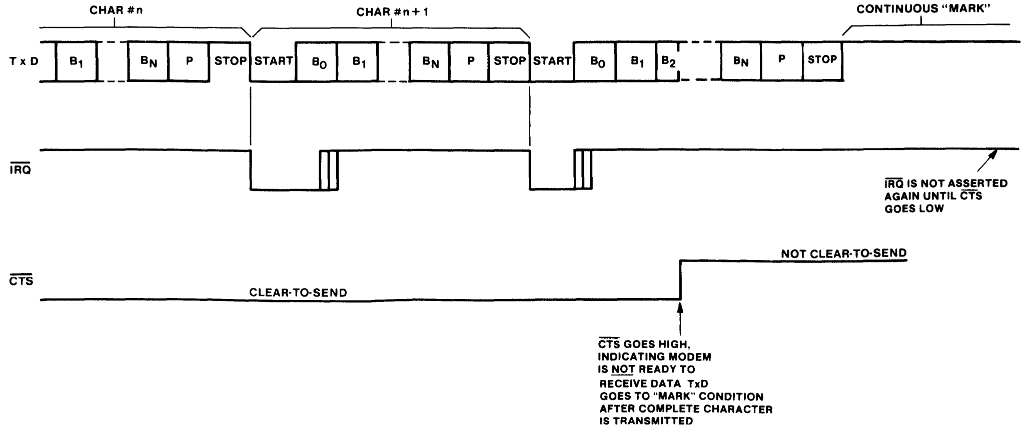

CHAR #n
CHAR #n+1
CONTINUOUS "MARK"
TxD
B1
BN
P
STOP
START
B0
B1
BN
P
STOP
START
B0
B1
B2
BN
P
STOP
IRQ
IRQ IS NOT ASSERTED AGAIN UNTIL CTS GOES LOW
NOT CLEAR-TO-SEND
CTS
CLEAR-TO-SEND
CTS GOES HIGH, INDICATING MODEM IS NOT READY TO RECEIVE DATA TxD GOES TO "MARK" CONDITION AFTER COMPLETE CHARACTER IS TRANSMITTED
92CM-42327

Fig. 10 - Effect of $\overline{\text{CTS}}$ on transmitter.

Effect of Overrun on Receiver (Fig. 11)

If the processor does not read the Receiver Data Register in the allocated time, then, when the following interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost.

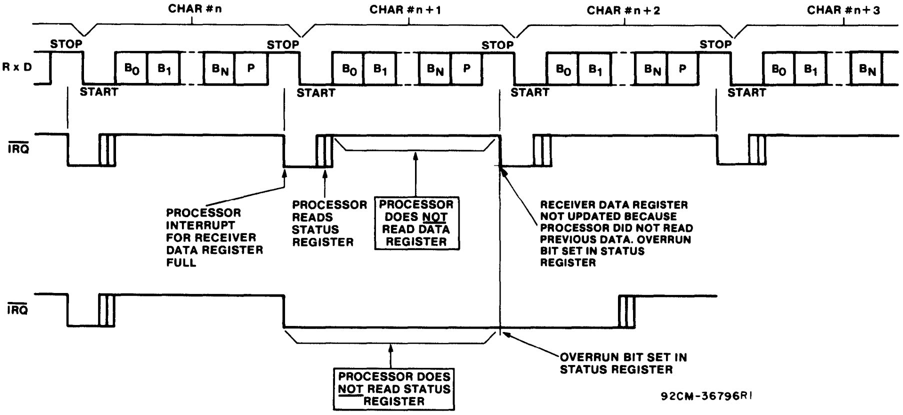

CHAR #n
CHAR #n+1
CHAR #n+2
CHAR #n+3
STOP
STOP
STOP
STOP
RxD
B0
B1
BN
P
START
START
START
START
IRQ
PROCESSOR INTERRUPT FOR RECEIVER DATA REGISTER FULL
PROCESSOR READS STATUS REGISTER
PROCESSOR DOES NOT READ DATA REGISTER
RECEIVER DATA REGISTER NOT UPDATED BECAUSE PROCESSOR DID NOT READ PREVIOUS DATA. OVERRUN BIT SET IN STATUS REGISTER
IRQ
PROCESSOR DOES NOT READ STATUS REGISTER
OVERRUN BIT SET IN STATUS REGISTER
92CM-36796R1

Fig. 11 - Effect of overrun on receiver.

CDP65C51A OPERATION (Cont'd)

TRANSMITTER AND RECEIVER OPERATION (Cont'd)

Echo Mode Timing (Fig. 12)

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by ½ of the bit time.

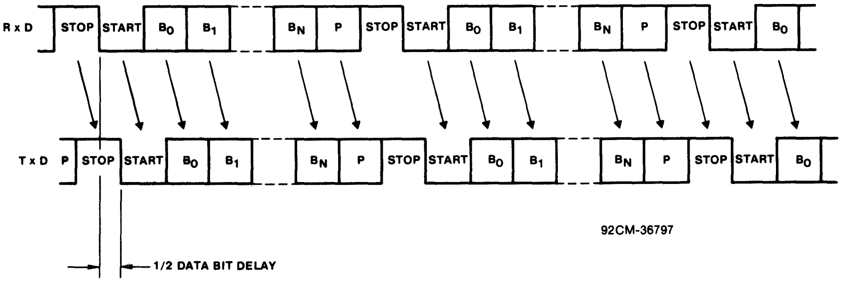


Fig. 12 - Echo mode timing.

Effect of $\overline{\text{CTS}}$ on Echo Mode Operation (Fig. 13)

See "Effect of $\overline{\text{CTS}}$ on Transmitter" for the effect of $\overline{\text{CTS}}$ on the Transmitter. Receiver operation is unaffected by $\overline{\text{CTS}}$, so, in Echo Mode, the Transmitter is affected in the same way as "Effect of $\overline{\text{CTS}}$ on Transmitter". In this case however, the processor interrupts signify that the Receiver Data Register is full, so the processor has no way of knowing that the Transmitter has ceased to echo.

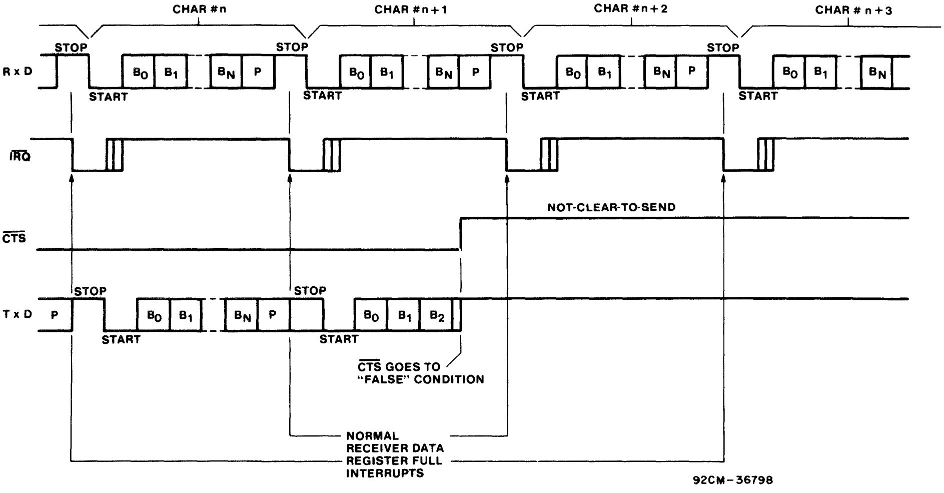


Fig. 13 - Effect of $\overline{\text{CTS}}$ on echo mode.

CDP65C51A OPERATION (Cont'd)

TRANSMITTER AND RECEIVER OPERATION (Cont'd)

Overrun in Echo Mode (Fig. 14)

If Overrun occurs in Echo Mode, the Receiver is affected the same way as described in "Effect of Overrun on Receiver".

For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor.

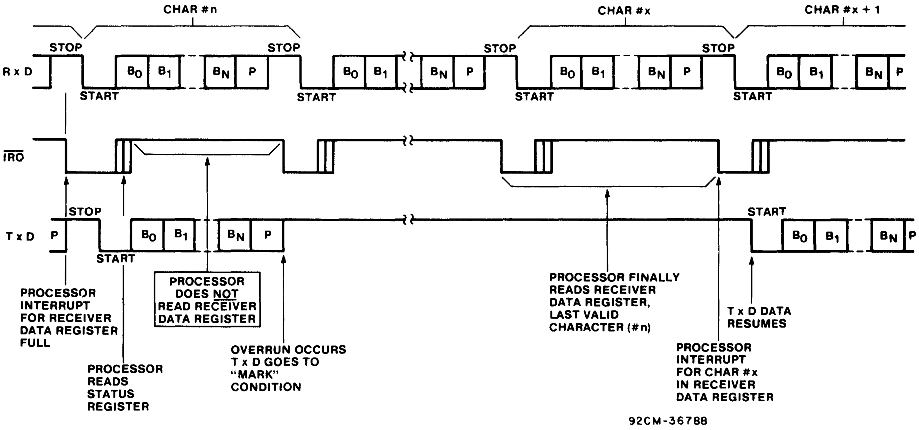

CHAR #n
CHAR #x
CHAR #x + 1
STOP
STOP
STOP
STOP
R x D
B_0
B_1
B_N
P
START
START
START
START
IRQ
STOP
START
T x D
P
PROCESSOR INTERRUPT FOR RECEIVER DATA REGISTER FULL
PROCESSOR DOES NOT READ RECEIVER DATA REGISTER
PROCESSOR READS STATUS REGISTER
OVERRUN OCCURS T x D GOES TO "MARK" CONDITION
PROCESSOR FINALLY READS RECEIVER DATA REGISTER, LAST VALID CHARACTER (#n)
T x D DATA RESUMES
PROCESSOR INTERRUPT FOR CHAR #x IN RECEIVER DATA REGISTER
92CM-36788

Fig. 14 - Overrun in echo mode.

Framing Error (Fig. 15)

Framing Error is caused by the absence of Stop Bit(s) on received data. The status bit is set when the processor interrupt occurs. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received.

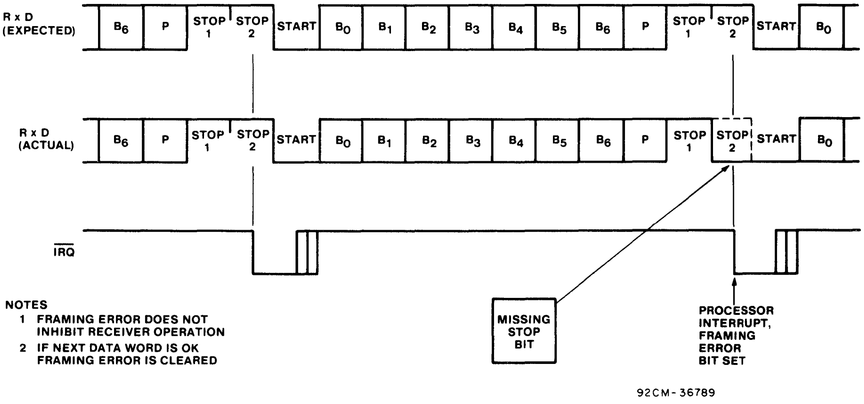

R x D (EXPECTED)
R x D (ACTUAL)
B_6
P
STOP 1
STOP 2
START
B_0
B_1
B_2
B_3
B_4
B_5
IRQ
NOTES
1 FRAMING ERROR DOES NOT INHIBIT RECEIVER OPERATION
2 IF NEXT DATA WORD IS OK FRAMING ERROR IS CLEARED
MISSING STOP BIT
PROCESSOR INTERRUPT, FRAMING ERROR BIT SET
92CM-36789

Fig. 15 - Framing error.

CDP65C51A OPERATION (Cont'd)

TRANSMITTER AND RECEIVER OPERATION (Cont'd)

Effect of $\overline{\text{DCD}}$ on Receiver (Fig. 16)

$\overline{\text{DCD}}$ is a modem output used to indicate the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data (RxD on the CDP65C51A some time later). The CDP65C51A will cause a processor interrupt whenever $\overline{\text{DCD}}$ changes state and will indicate this condition via the Status Register. Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the CDP65C51A automatically checks the level of the $\overline{\text{DCD}}$ line, and if it has changed, another interrupt occurs.

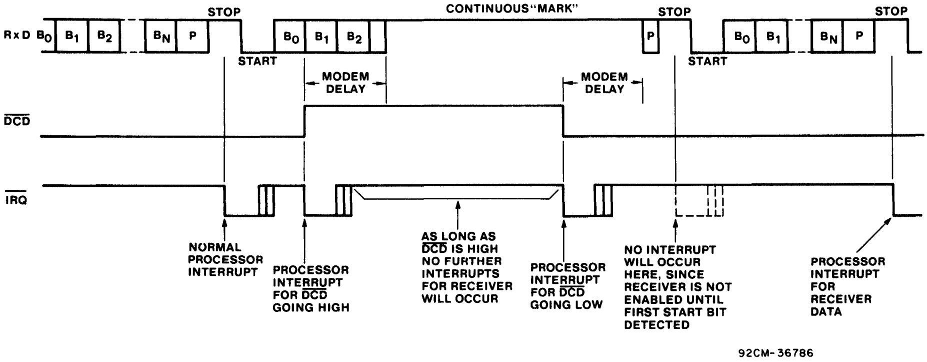

STOP
CONTINUOUS "MARK"
STOP
STOP
RxD
B0
B1
B2
BN
P
START
B0
B1
B2
MODEM DELAY
MODEM DELAY
P
START
B0
B1
BN
P
DCD
IRQ
NORMAL PROCESSOR INTERRUPT
PROCESSOR INTERRUPT FOR DCD GOING HIGH
AS LONG AS DCD IS HIGH NO FURTHER INTERRUPTS FOR RECEIVER WILL OCCUR
PROCESSOR INTERRUPT FOR DCD GOING LOW
NO INTERRUPT WILL OCCUR HERE, SINCE RECEIVER IS NOT ENABLED UNTIL FIRST START BIT DETECTED
PROCESSOR INTERRUPT FOR RECEIVER DATA
92CM-36786

Fig. 16 - Effect of $\overline{\text{DCD}}$ on receiver.

Timing with 1½ Stop Bits (Fig. 17)

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the processor interrupt for Receiver Data Register Full occurs halfway through the trailing half-Stop Bit.

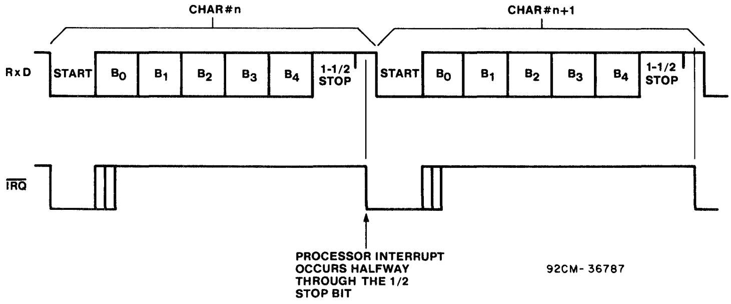


Fig. 17 - Timing with 1-1/2 stop bits.

CDP65C51A OPERATION (Cont'd)

TRANSMITTER AND RECEIVER OPERATION (Cont'd)

Transmit Continuous "BREAK" (Fig. 18)

This mode is selected via the CDP65C51A Command Register and causes the Transmitter to send continuous "BREAK" characters after both the transmitter and transmitter-holding registers have been emptied. When the Command Register is programmed back to normal transmit mode, a Stop Bit is generated and normal transmission continues.

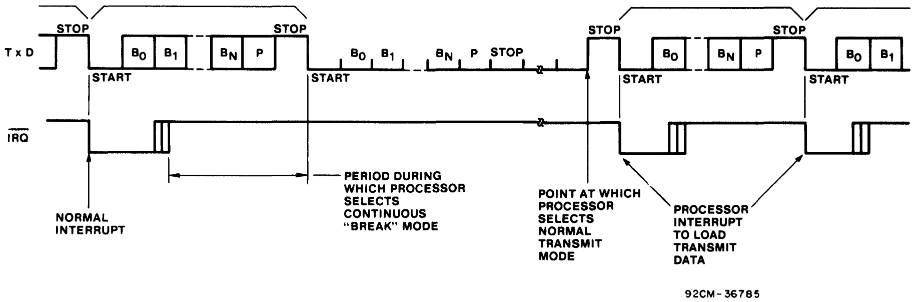

STOP
STOP
STOP
STOP
TxD
B_0
B_1
B_N
P
B_0
B_1
B_N
P
STOP
B_0
B_N
P
B_0
B_1
START
START
START
START
IRQ
PERIOD DURING WHICH PROCESSOR SELECTS CONTINUOUS "BREAK" MODE
NORMAL INTERRUPT
POINT AT WHICH PROCESSOR SELECTS NORMAL TRANSMIT MODE
PROCESSOR INTERRUPT TO LOAD TRANSMIT DATA
92CM-36785

Fig. 18 - Transmit continuous "BREAK".

Receive Continuous "BREAK" (Fig. 19)

In the event the modem transmits continuous "BREAK" characters, the CDP65C51A will terminate receiving. Reception will resume only after a Stop Bit is encountered by the CDP65C51A.

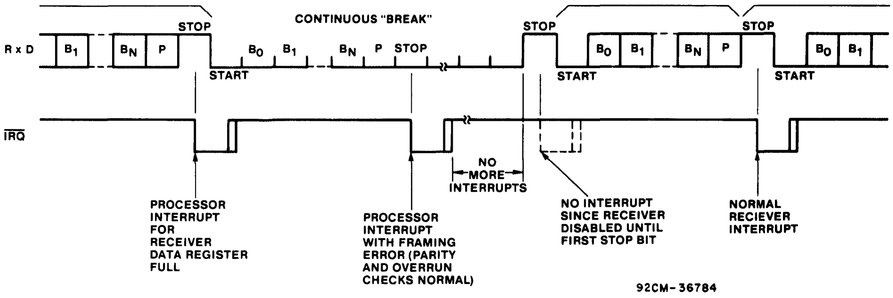

CONTINUOUS "BREAK"
STOP
STOP
STOP
RxD
B_1
B_N
P
B_0
B_1
B_N
P
STOP
B_0
B_1
B_N
P
B_0
B_1
START
START
START
IRQ
NO MORE INTERRUPTS
PROCESSOR INTERRUPT FOR RECEIVER DATA REGISTER FULL
PROCESSOR INTERRUPT WITH FRAMING ERROR (PARITY AND OVERRUN CHECKS NORMAL)
NO INTERRUPT SINCE RECEIVER DISABLED UNTIL FIRST STOP BIT
NORMAL RECIEVER INTERRUPT
92CM-36784

Fig. 19 - Receive continuous "BREAK".

CDP65C51A OPERATION (Cont'd)

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the CDP65C51A should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 (IRQ). Subsequent transitions on $\overline{\text{DSR}}$ and $\overline{\text{DCD}}$ will cause another interrupt.

2. Check IRQ Bit

   If not set, interrupt source is not the CDP65C51A.

3. Check $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both "0" (modem "on-line") and they are unchanged then the remaining bits must be checked.

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2)

   Only if Receiver Data Register is Full.

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

7. If none of the above, then $\overline{\text{CTS}}$ must have gone to the False (high) state.

PROGRAMMED RESET OPERATION

A program reset occurs when the processor performs a write operation to the CDP65C51A with RS0 high and RS1 low. The program reset operates somewhat different from the hardware reset ($\overline{\text{RES}}$ pin) and is described as follows:

1. Internal registers are not completely cleared. The data sheet indicates the effect of a program reset on internal registers.
2. The $\overline{\text{DTR}}$ line goes high immediately.
3. Receiver and transmitter interrupts are disabled immediately. If $\overline{\text{IRQ}}$ is low when the reset occurs, it stays low until serviced, unless interrupt was caused by $\overline{\text{DCD}}$ or $\overline{\text{DSR}}$ transition.
4. $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ interrupts disabled immediately. If $\overline{\text{IRQ}}$ is low and was caused by $\overline{\text{DCD}}$ or $\overline{\text{DSR}}$, then it goes high, also $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ status bits subsequently will follow the input lines, although no interrupt will occur.
5. Overrun cleared, if set.

MISCELLANEOUS NOTES ON OPERATION

1. If Echo Mode is selected, $\overline{\text{RTS}}$ goes low.
2. If Bit 0 of Command Register is "0" (disabled), then:
   a) All interrupts disabled, including those caused by $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ transitions.
   b) Receiver disabled, but a character currently being received will be completed first.
   c) Transmitter is disabled after both the Transmit Data and Transmit Shift Registers have been emptied.
3. Odd parity occurs when the sum of all the "1" bits in the data word (including the parity bit) is odd.
4. In the Receive Mode, the received parity bit does not go into the Receiver Data Register, but is used to generate parity error for the Status Register.
5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.
6. If the RxD line inadvertently goes low and then high during the first 9 receiver clocks after a Stop Bit; a false Start Bit will result.

   For false Start Bit detection, the CDP65C51A does not begin to receive data, instead, only a true Start Bit initiates receiver operation.

7. A precaution to consider with the crystal oscillator circuit is:

   The XTLI input may be used as an external clock input. The XTLO pin must be floating and may not be used for any other function.

8. $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ transitions, although causing immediate processor interrupts, have no effect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be terminated either to Gnd or V_{DD}.

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the CDP65C51A Control Register.

The divisors, then, are determined by bits 0-3 in the Control Register and their values are shown in Table II.

Generating Other Baud Rates

By using a different crystal, other baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the CDP65C51A with an off-chip oscillator to achieve the same thing. In this case, XTLI (pin 6) must be the clock input and XTLO (pin 7) must be a no-connect.

CDP65C51A OPERATION (Cont'd)

Table II - Divisor Selection for the CDP65C51A

CONTROL REGISTER BITS				DIVISOR SELECTED FOR THE INTERNAL COUNTER	BAUD RATE GENERATED WITH 1.8432 MHz	BAUD RATE GENERATED WITH FREQUENCY (F)
3	2	1	0			
0	0	0	0	No Divisor Selected	1/16 of External Clock at Pin XTLI	1/16 of External Clock at Pin XTLI
0	0	0	1	36,864	$\frac{1.8432 \times 10^6}{36,864} = 50$	$\frac{F}{36,864}$
0	0	1	0	24,576	$\frac{1.8432 \times 10^6}{24,576} = 75$	$\frac{F}{24,576}$
0	0	1	1	16,768	$\frac{1.8432 \times 10^6}{16,768} = 109.92$	$\frac{F}{16,768}$
0	1	0	0	13,696	$\frac{1.8432 \times 10^6}{13,696} = 134.58$	$\frac{F}{13,696}$
0	1	0	1	12,288	$\frac{1.8432 \times 10^6}{12,288} = 150$	$\frac{F}{12,288}$
0	1	1	0	6,144	$\frac{1.8432 \times 10^6}{6,144} = 300$	$\frac{F}{6,144}$
0	1	1	1	3,072	$\frac{1.8432 \times 10^6}{3,072} = 600$	$\frac{F}{3,072}$
1	0	0	0	1,536	$\frac{1.8432 \times 10^6}{1,536} = 1200$	$\frac{F}{1,536}$
1	0	0	1	1,024	$\frac{1.8432 \times 10^6}{1,024} = 1800$	$\frac{F}{1,024}$
1	0	1	0	768	$\frac{1.8432 \times 10^6}{768} = 2400$	$\frac{F}{768}$
1	0	1	1	512	$\frac{1.8432 \times 10^6}{512} = 3600$	$\frac{F}{512}$
1	1	0	0	384	$\frac{1.8432 \times 10^6}{384} = 4800$	$\frac{F}{384}$
1	1	0	1	256	$\frac{1.8432 \times 10^6}{256} = 7200$	$\frac{F}{256}$
1	1	1	0	192	$\frac{1.8432 \times 10^6}{192} = 9600$	$\frac{F}{192}$
1	1	1	1	96	$\frac{1.8432 \times 10^6}{96} = 19200$	$\frac{F}{96}$

DIAGNOSTIC LOOP-BACK OPERATING MODES

A simplified block diagram for a system incorporating a CDP65C51A ACIA is shown in Fig. 20.

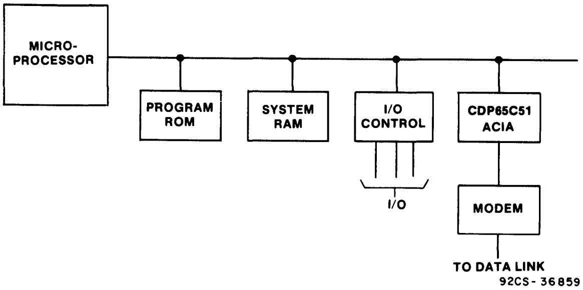


Fig. 20 - Simplified system diagram.

CDP65C51A OPERATION (Cont'd)

DIAGNOSTIC LOOP-BACK OPERATING MODES (Cont'd)

Occasionally it may be desirable to include in the system a facility for "loop-back" diagnostic testing, of which there are two kinds:

1. Local Loop-Back

   Loop-back from the point of view of the processor. In this case, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

2. Remote Loop-Back

   Loop-back from the point of view of the Data Link and Modem. In this case, the processor, itself, is disconnected and all received data is immediately retransmitted, so the system on the other end of the Data Link may operate independent of the local system.

The CDP65C51A does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry.

Fig. 21 indicates the necessary logic to be used with the CDP65C51A.

The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB = high does the following:

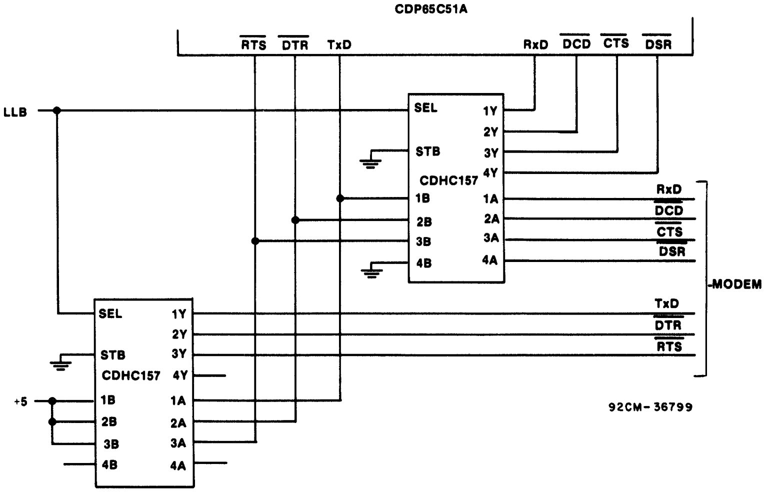
1. Disables outputs TxD, $\overline{DTR}$, and $\overline{RTS}$ (to Modem).
2. Disables inputs RxD, $\overline{DCD}$, $\overline{CTS}$, $\overline{DSR}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs:
   a) TxD to RxD
   b) $\overline{DTR}$ to $\overline{DCD}$
   c) $\overline{RTS}$ to $\overline{CTS}$

LLB may be tied to a peripheral control pin to provide processor control of local loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

Remote loop-back does not require this circuitry, so LLB must be set low. However, the processor must select the following:

1. Control Register bit 4 must be "1", so that the transmitter clock = receiver clock.
2. Command Register bit 4 must be "1" to select Echo Mode.
3. Command Register bits 3 and 2 must be "1" and "0", respectively, to disable transmitter interrupts.
4. Command Register bit 1 must be "0" to disable receiver interrupts.

In this way, the system retransmits received data without any effect on the local system.



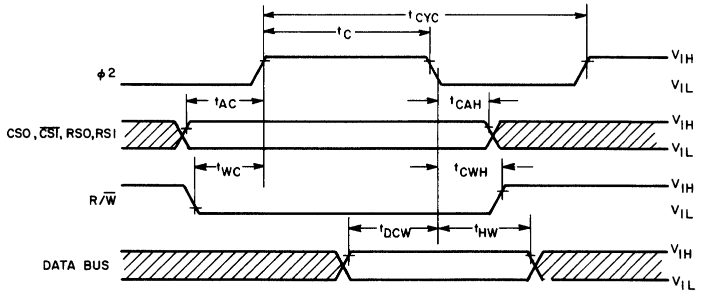
NOTES: 1. HIGH ON LLB SELECTS LOCAL LOOP-BACK MODE.
2. HIGH ON HC157 SELECT INPUT GATES "B" INPUTS TO "Y" OUTPUTS; LOW GATES "A" TO "Y".

Fig. 21 - Loop-back circuit schematic.

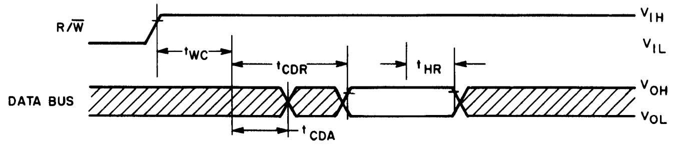
DYNAMIC ELECTRICAL CHARACTERISTICS—READ/WRITE CYCLE

V_{DD} = 5V ± 5%, T_A = -40 to +85° C, C_L = 75 pF

CHARACTERISTIC		LIMITS						UNITS
		CDP65C51-1		CDP65C51-2		CDP65C51-4		
		Min.	Max.	Min.	Max.	Min.	Max.	
Cycle Time	t_{CYC}	1	—	0.5	—	0.25	—	µs
ϕ2 Pulse Width	t_C	400	—	200	—	100	—	ns
Address Set-Up Time	t_{AC}	120	—	60	—	30	—	ns
Address Hold Time	t_{CAH}	0	—	0	—	0	—	ns
R/W Set-Up Time	t_{WC}	120	—	60	—	30	—	ns
R/W Hold Time	t_{CWH}	0	—	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	120	—	60	—	35	—	ns
Data Bus Hold Time	t_{HW}	20	—	10	—	5	—	ns
Read Access Time (Valid Data)	t_{CDR}	—	200	—	150	—	50	ns
Read Hold Time	t_{HR}	20	—	10	—	10	—	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	—	20	—	10	—	ns



Write-timing waveforms



Read-timing waveforms

Fig. 22 - Timing waveforms.

CDP65C51A

DYNAMIC ELECTRICAL CHARACTERISTICS—TRANSMIT/RECEIVE, See Figs. 23, 24 and 25.
V_{DD} = 5V ± 5%, T_A = -40 to +85°C

CHARACTERISTIC		LIMITS						UNITS
		CDP65C51-1		CDP65C51-2		CDP65C51-4		
		Min.	Max.	Min.	Max.	Min.	Max.	
Transmit/Receive Clock Rate	t_{CCY}	400*	—	325	—	250	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	145	—	110	—	
Transmit/Receive Clock Low Time	t_{CL}	175	—	145	—	110	—	
XTLI to TxD Propagation Delay	t_{DD}	—	500	—	410	—	315	
RTS Propagation Delay	t_{DLY}	—	500	—	410	—	315	
IRQ Propagation Delay (Clear)	t_{IRQ}	—	500	—	410	—	315	
RES Pulse Width	t_{RES}	400	—	300	—	200	—	

(t_r, t_f = 10 to 30 ns)

* The baud rate with external clocking is: Baud Rate = $\dfrac{1}{16 \times T_{CCY}}$

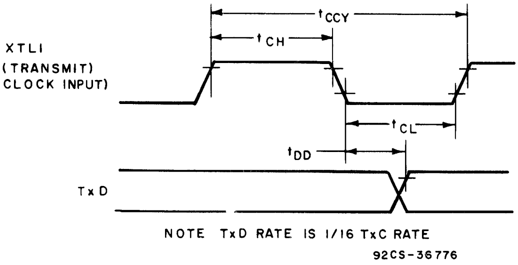


Fig. 23 - Transmit-timing waveforms with external clock.

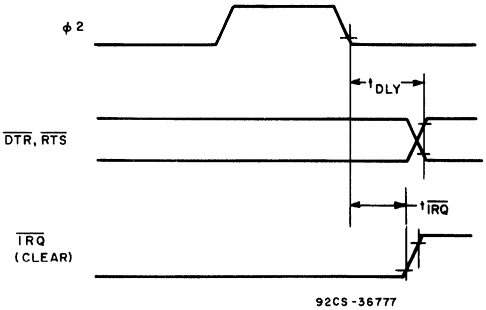


Fig. 24 - Interrupt-and output-timing waveforms.

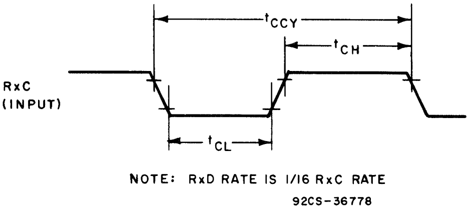


Fig. 25 - Receive external clock timing waveforms.

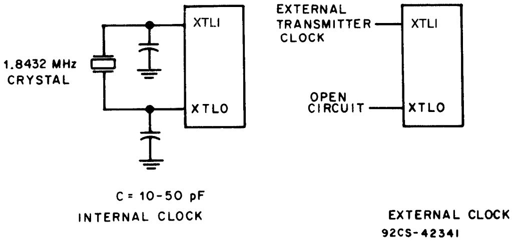
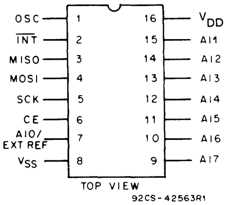


Fig. 26 - Transmitter clock generation.

Advance Information

CDP68HC68A2

CMOS Serial 10-Bit A/D Converter



TERMINAL ASSIGNMENT

Features:

- *10-bit resolution*
- *8-bit mode for single data byte transfers*
- *SPI (Serial Peripheral Interface) compatible*
- *Operates ratiometrically referencing V_{DD} or an external source*
- *14 µs 10-bit conversion time*
- *8 multiplexed analog input channels*
- *Independent channel select*
- *Three modes of operation*
- *On chip oscillator*
- *Low power CMOS circuitry*
- *Intrinsic sample and hold*
- *16-lead dual-in-line plastic package*
- *20-lead dual-in-line small-outline plastic package*

The CDP68HC68A2 is a CMOS 8- or 10-bit successive approximation analog to digital converter (A/D) with a standard RCA/Motorola Serial Peripheral Interface (SPI) bus and eight multiplexed analog inputs Voltage referencing is obtained from either the V_{DD} pin or an external precision reference for the sacrifice of one channel when enabled. The operating range of the converter includes the entire V_{DD} to V_{SS} voltage range for each of the eight inputs.

The CDP68HC68A2 implements a switched capacitor, successive approximation A/D conversion technique which provides an inherent sample-and-hold function. An on-chip Schmitt oscillator provides the internal timing of the A/D converter It can be driven by an external oscillator or system clock in the external mode, or can be connected to a single external capacitor to provide an independent clock in the internal mode. The minimum 10-bit conversion time per input is 14-microseconds/channel. Each conversion in the 10-bit mode requires 14 oscillator clock pulses where 12 are required in the 8-bit mode allowing a 12-microsecond/-channel conversion time

A unique feature of the CDP68HC68A2 allows any combination of the eight input channels to be selected and converted in ascending channel order in any one of three modes. The mode selection enables single, multiple or continuous channel conversion operation. The device has three READ/WRITE registers which are used to select the mode of operation, input channels, and starting address. The 10-bit conversion data is stored (right justified) in two 8-bit bytes. The most significant byte contains two status bits which may be monitored by the microcomputer. An 8-bit mode is available which performs a faster eight bit

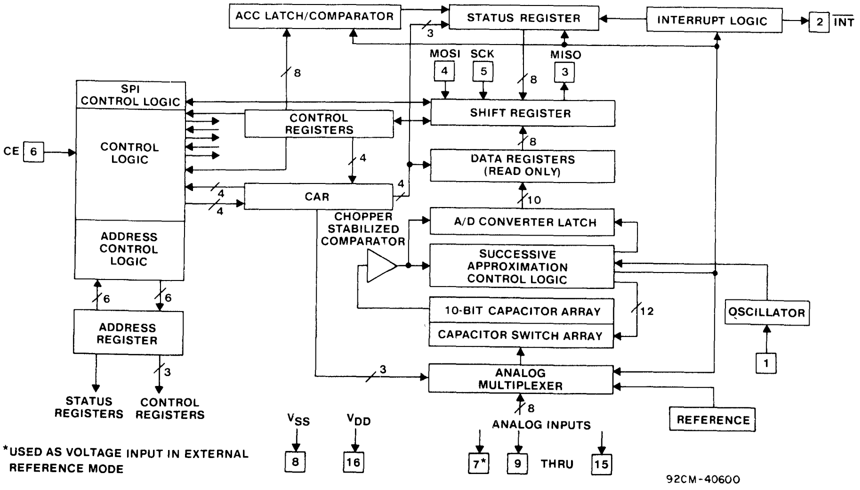


Fig. 1 - Block diagram of the CDP68HC68A2.

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conversion and stores the data in a single eight bit byte. In the 10-bit mode, all 16 data bytes are addressable and in the 8-bit mode only the eight bit data byte is accessible in each of eight data bytes. A READ only STATUS register is available to monitor the status of the Conversion and the current channel address. This register can be used for system polling or the $\overline{\text{INT}}$ pin can be used for interrupt driven communications.

The CDP68HC68A2 is available in a 16-lead dual-in-line plastic package (E suffix) and in a 20-lead dual-in-line small-outline plastic package (M suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltage referenced to V_{SS} terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 12 mW/° C to 200 mW
For T_A = -40° C to +70° C (PACKAGE TYPE M) *	400 mW
For T_A = -70° C to +85° C (PACKAGE TYPE M) *	Derate Linearly at 6.0 mW/° C to 310 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	40 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE E and M	-40 to +85° C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

OPERATING CONDITIONS at T_A = -40° to +85° C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	3	6	V

Pin Descriptions

OSC (1) — Oscillator Input

A Schmitt input which provides the timing for the A/D conversion. The mode of this pin is selected in the Mode Select Register (MSR) and is either internal or external clocking. In the internal mode, a capacitor is externally connected to this pin causing the Schmitt input gate to oscillate at a frequency inversely proportional to the capacitance. In the external mode, the input may be driven directly by an external oscillator or system clock.

$\overline{\text{INT}}$ (2) — Active Low Interrupt Output

This output is driven from a single NFET pulldown transistor. A bit in the MSR enables or disables the $\overline{\text{INT}}$ output. The output is driven to a logical LOW state while enabled and activated, otherwise it will remain in a tri-state condition. The $\overline{\text{INT}}$ output function is only deactivated upon addressing the Status Register. The tri-state function can be advantageous to wire NAND interrupts while a pullup resistor can be used to drive the output to the logical HIGH state while inactive. The interrupt function cannot be enabled in mode 3.

MISO (3) — Master-In-Slave-Out Output

Data is serially shifted out at this pin Most Significant Bit first.

MOSI (4) — Master-Out-Slave-In Input

Data is serially shifted in on this pin Most Significant Bit first.

SCK (5) — Serial Clock Input

Provides the timing for the synchronous SPI interface circuitry.

CE (6) — Chip Enable Input

An active HIGH device enable. The CDP68HC68A2 must be enabled preceding SPI communications. While deactivated, the SPI logic is placed in a RESET state and the MISO line is tristated from driving the SPI bus synchronous with SCK.

AIn (7, 9-15) — Analog Inputs

These are the eight analog input channels which are multiplexed to the internal A/D converter. Each channel is selected by a corresponding bit in the Channel Select Register (CSR). When the VR bit in the MSR is enabled, the device is in the external voltage referencing mode and channel A0 (pin 7) is used as a full scale reference input.

V_{SS} (8) — Negative Power Supply

This pin is connected to the ground and establishes the negative reference to the analog inputs.

V_{DD} (16) — Positive Power Supply

This pin establishes the full-scale voltage range of the A/D converter when operating ratiometrically in the internal reference mode.

ELECTRICAL CHARACTERISTICS at T_A = 25° C, V_{DD} = 5 V, except as noted.

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
ACCURACY					
Differential Linearity Error	10-Bit Mode		±1.25	±2	LSB
Integral Linear Error	10-Bit Mode		±1.25	±2	LSB
Offset Error	10-Bit Mode	-1	3	4	LSB
Gain Error	10-Bit Mode	-1	1	2	LSB
ANALOG INPUTS: A10 THRU A17					
Input Resistance	In Series With Sample Caps		85		Ohms
Sample Capacitance	During Sample State		400		pF
Input Capacitance	During Hold State		20		pF
Input Current	@ V_{IN} = V_{REF}+ During Sample		+30		μA
	During Hold or Standby State			±1	μA
Input + Full Scale Range		V_{SS}		V_{DD} +.3	V
Input Bandwidth (3 dB)	From Input RC Time Constant		4.68		MHz
DIGITAL INPUTS: MOSI, SCK, CE T_A = -40°C to +85°C					
High Input Voltage V_{IH}	Over V_{DD} = 3 to 6 V	70			% of V_{DD}
Low Input Voltage V_{IL}	Over V_{DD} = 3 to 6 V			30	% of V_{DD}
Input Leakage				±1	μA
Input Capacitance	Room Temperature			10	pF
DIGITAL OUTPUTS: MISO, $\overline{INT}$ T_A = -40°C to +85°C					
High Level Output V_{OH}, MISO	I_{SOURCE} = 6 mA	4.25			V
Low Level Output V_{OL}, MISO, $\overline{INT}$	I_{SINK} = 6 mA			0.4	V
3-State Output Leakage I_{OUT}, MISO, $\overline{INT}$				±10	μA
TIMING PARAMETERS T_A = -40°C to +85°C					
Oscillator Frequency, f_{sample}	10-Bit Mode			1	MHz
Conversion Time (Including Sample Time)	10-Bit Mode 8-Bit Mode	14 Oscillator Cycles 12 Oscillator Cycles			
Sample Time (Pre-Encode)	8 Time Constants (8τ) Required	First 1.5 Oscillator ≥ 8τ			
Serial Clock (SCK) Frequency				1.5	MHz
SCK Pulse Width, T_P	Either SCK_a or SCK_b	150			ns
MOSI Setup Time, T_{DSU}	Prior to Leading Edge of T_P	60			ns
MOSI Hold Time, T_{DH}	After Leading Edge of T_P	60			ns
MISO Rise & Fall Time	200 pF Load			100	ns
MISO Propagation Delay, T_{DOD}	From Trailing SCK Edge			100	ns
I_{DD}	V_{DD} = 5 Volts, Continuous Operation		1.4	2	mA

Serial Data Format, Device Communication and Operation

1. Overview

To operate the CDP68HC68A2 A/D, it is required to access the control registers and program them for desired operation. This is performed serially over the SPI bus in a two phase sequence, each phase contains a minimum of one SPI transfer cycle. In phase I, the microcontrolling device sends an ADDRESS/CONTROL WRITE byte to initialize a register operation. This is followed by phase II, the REGISTER DATA ACCESS, which allows single or multiple byte READ or WRITE transfers depending on the state of the Chip Enable (CE). The following sections describe this operation in detail to more effectively use this SPI peripheral device.

2. SPI Logic

The Serial Peripheral Interface (SPI) on a peripheral device is used to communicate with a microcomputer, and was designed to meet timing specifications illustrated in figure 2. The bit order is MSB first and there are eight serial clock cycles to a SPI transfer cycle. A WRITE to the SPI peripheral is performed by generating data on the MOSI line synchronous to the SCK. A READ from the SPI peripheral requires a WRITE to be performed just to cycle the SCK input eight times, sometimes referred to as a 'DUMMY WRITE'. This is due to the full duplex nature of this SPI peripheral.

In the case of CDP6805 Microcontrollers, the Serial Clock Phase (CPHA) needs to be set to a logical HIGH, where a transition occurs before a strobe for valid data. As for the Serial Clock Polarity (CPOL) either (SCKa or SCKb) will be accepted, as the state of SCK is determined at the transition of Chip Enable (CE). The appropriate internal polarity of SCK is selected and maintained for the duration of the SPI transfer cycle (till CE is deasserted).

3. Addressing Modes

Following the initial ADDRESS/CONTROL WRITE transfer of phase I, there are two modes available to accessing registers during phase II. These are single byte transfers and multiple byte or burst type transfers. The more applicable method should be apparent based on system objectives. For example, where minimum communication overhead is a consideration, burst mode is used wherever possible.

Single byte transfers address a single register and perform a REGISTER DATA ACCESS to or from that register. Burst transfers are used to access one register followed by accesses to or from registers in ascending consecutive order. These accesses, will be READ or WRITE operations but not both. Single byte transfers are usually made where just one register need be accessed, in general, where burst transfers are not possible due to the addressing order or if accesses mix READ and WRITE operations. Single byte transfers access one register and require exactly two SPI transfers. Burst transfers access N registers and require N+1 SPI transfers.

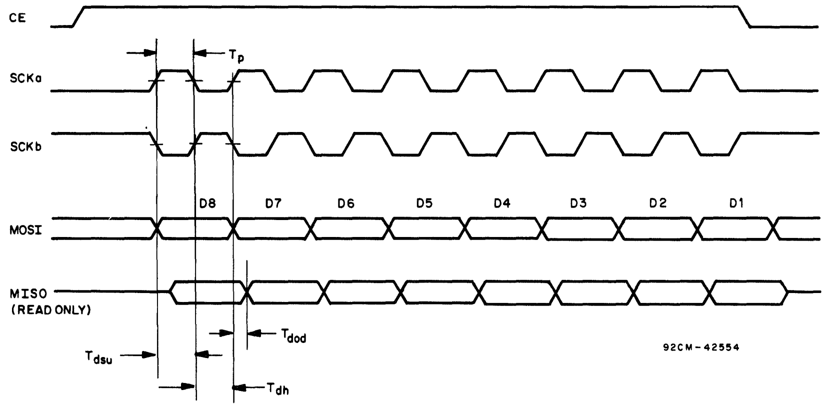
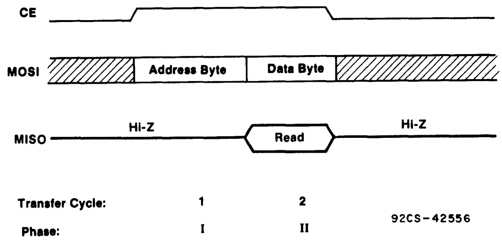


Fig. 2 - Timing diagram for serial peripheral interface.

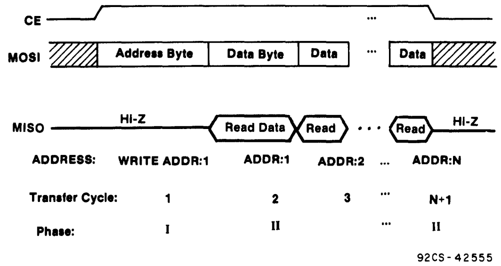
3.1 Device Addressing

To address the A/D registers internally, the A/D device first needs to be addressed externally by the microcontroller activating the Chip Enable of the A/D. After activating CE the A/D device awaits SPI transfer cycles for phase I, followed by phase II, see figure 3a and b for timing of the Single Byte or Burst Modes of communication. Refer to Note 1 for CE.

MISO always Hi impedance during Phase I, Phase II WRITE operations and when CE is inactive. Phase II READ operations will have valid READ Data on the MISO.



(a) *Single byte transfer.*
(Requires 2 SPI transfers)



(b) *Multiple (N) byte transfer.*
(Efficient device communication requiring N+1 SPI transfers)

Fig. 3 - Timing diagrams for (a) single byte transfer and (b) multiple (N) byte transfer.

During the (N+1) 'th Burst Mode Transfer, the address transferred will be N and is advanced internally to N+1 at the completion of that cycle. For example, if the initial address was 00 and N was desired to be 06, the address accessed in the 7th burst mode transfer will be address 06, yet internally the address will point to address 07 after transferring the contents of 06, see section 3.1.1 for details on the ADDRESS/CONTROL WRITE. The previous example applies to Control, Status and selected consecutive Data Registers. It does not apply to Data Registers which are not selected since they are skipped entirely, or not consecutive since the address is advanced more than an increment until the next selected channel is addressed, see Note 5 on Data Registers in Register allocation map, appendix, section 5.3.

3.1.1 ADDRESS/CONTROL WRITE (Phase I)

The ADDRESS/CONTROL WRITE phase is a dual purpose WRITE only operation that performs register addressing and READ/WRITE control. Phase I is invoked by the first SPI Transfer at the onset of activated CE. Both address and control are performed using eight bits, refer to figure 4 for bit descriptions. One of these bits (MSB) is used to designate READ or WRITE Phase II operations to follow. The remaining seven bits are used to designate a register address of which the following READ or WRITE operation is to be performed upon, see address map in appendix, section 5.3 for register allocation. To follow are details on bit descriptions.

BIT SIGNIFICANCE, most to least from left to right:

$\overline{\text{R}}$/W	0	0	A4	A3	A2	A1	A0

Fig. 4 - Address/Control write byte.

$\overline{\text{R}}$/W ($\overline{\text{READ}}$/WRITE)

This bit is used to control the data direction during the following SPI REGISTER DATA ACCESS (Phase II cycles). The bit is logically set HIGH or cleared LOW to initiate one or more REGISTER DATA ACCESS - WRITE or READ operations respectively. Either mode, once designated, will be maintained until CE is deactivated and a new ADDRESS/CONTROL WRITE (Phase I) is invoked.

UNUSED

The two unused bits must be cleared to the logical LOW state to address any of the internal registers of the CDP68HC68A2.

An:

The five ADDRESS bits A4-A0 are used to address the registers in accordance with the address allocation table of appendix, section 5.3. When addressing READ only Data Registers it should be noted that when in 10-bit mode, the A0 addresses the $\overline{\text{MOST}}$/LEAST SIGNIFICANT DATA REGISTER bytes when logically LOW and HIGH respectively. In the 8-bit mode the data register bytes are LOW byte only (Since there is no HIGH byte A0 is a 'don't care').

3.1.2 REGISTER DATA ACCESS (Phase II)

The ADDRESS/CONTROL WRITE in Phase I (one SPI transfer cycle) is followed by REGISTER DATA ACCESS during Phase II of the SPI transfers. This operation is either a READ or a WRITE depending on the operation previously designated by the ADDRESS/CONTROL WRITE byte. CE determines whether Phase II is to be a Single Byte or Burst transfer and when transfers terminate, see Note 1.

If CE is active for just one Phase II SPI transfer, it will only be a Single Byte transfer; however, if it remains asserted after the first Phase II SPI transfer, multiple byte transfers will proceed to occur. This is the Burst Mode. While in this mode, the address written in Phase I is incremented automatically at the completion of each register access. The CONTROL and STATUS Registers are accessed directly, and advanced by single address increments. Data Registers are advanced to the NEXT selected channel in the CSR. See Note 5 for limitations of Data and Control/Status accesses.

4. Control and Status Registers

There are three $\overline{\text{READ}}$/WRITE control registers and one READ only STATUS Register in the CDP68HC68A2. They are described in detail here and shown in the register allocation table in appendix section 5.3.

4.1 Mode Select Register (MSR)

ADDRESS: ($\overline{\text{R}}$/W)0001000	X	X	$\overline{\text{EXT}}$	VR	M8	IE	M1	M0

This READ/WRITE register is used to select the mode of operation as well as various functions of the device. Data is maintained in this register until new data is written, initially powers up with all bits cleared to logical zero. A WRITE to the MSR will clear the $\overline{\text{INT}}$ output and all STATUS bits.

Individual bits are described here:

TWO X BITS

Are "don't care" bits and can be in any state.

$\overline{\text{EXT}}$ (External Oscillator)

This bit selects the internal oscillator with a logical HIGH, or a logical LOW selects the external clock on pin 1.

VR (Voltage Reference)

This control bit is used to determine the voltage reference source of the A/D converter. A logical HIGH in this bit selects pin 7 (AI0) as the external reference input. A logical LOW in this bit establishes the V_{DD} voltage level as the reference for ratiometric operation.

M8 (Eight Bit Mode)

This bit selects either the 10-bit or 8-bit mode of operation. A logical LOW in this bit enables the 10-bit mode, while a logical HIGH enables the 8-bit mode.

IE (Interrupt Enable)

This control bit is used to enable or disable the $\overline{\text{INT}}$ output function. A logical HIGH in this bit enables the $\overline{\text{INT}}$ output function when operating in either modes 1 and 2. A logical low in this bit disables $\overline{\text{INT}}$ output function, maintaining pin 2 to a tristate condition. The status bits in the DATA and STATUS registers are not affected by the state of the IE control bit.

M1, M0 (Mode Select)

These two bits are set to select the mode of operation of the A/D converter. These modes are tabulated:

MODE SELECT

M1	M0	Mode	Function
0	0	0	IDLE
0	1	1	SINGLE CONVERSION
1	0	2	SINGLE SCANNING CONVERSION
1	1	3	CONTINUOUS SCANNING CONVERSION

4.2 Conversion Mode Descriptions

Operating the CDP68HC68A2 in these modes is generally performed by a WRITE sequence to the Mode Select Register (MSR), Channel Select Register (CSR) and Starting Address Register (SAR) with the desired Starting Channel Address. This is most efficient in the Burst Transfer mode, see appendix, section 5.3.2.1 dedicated to this topic. Conversions are invoked, following a WRITE to the SAR, on the addressed channel in the Channel Address Register (CAR).

4.2.1 IDLE

In this mode the internal A/D oscillator is disabled. Data is maintained from previous conversions in the STATUS and DATA registers and may be accessed. The IDLE mode can be invoked by a single (two Phase) WRITE to the MSR. If it is desired to access the control registers they should be written to in a burst sequence to set the Mode, and the SAR, and clear any status bits that may be set, see appendix, section 5.3.2.1.

4.2.2 SINGLE CONVERSION

Upon completion of any single conversion in mode 1, all status bits are set and the $\overline{\text{INT}}$ output activated (if enabled) and the converter interrupts awaiting a Data Register Access. The corresponding Data Register may then be read. In both 8- and 10-bit modes, this mode of operation will continue until a new command is issued by a WRITE to the MSR, CSR or conversions are aborted.

The first conversion will occur on the analog channel and digital address in the CAR after the SAR WRITE with the ENC bit set. Following conversions will be determined by selected channels and the Data Register access sequence controlling the CAR. After initially invoking this mode, the STATUS should be polled or hardware interruption can be used to wait for conversion completion before issueing a data retrieve sequence. Data conversions can be interleaved with Data Register READS along with the wait requirement. If hardware interrupts are dedicated to this process, conversions can be made and Data retrieved, all while maintaining CE active.

In the 8-bit mode there is only one Data Register byte associated with each channel; thus the channel address is automatically incremented after reading that register to the next selected, sequential channel and the next conversion initiated.

In the 10-bit mode, upon completion of reading the Most Significant Byte (MSB) of the appropriate channel address, the Channel Address is automatically incremented to the Least Significant Byte (LSB) at which time a conversion is initiated on the next selected channel. Reading the LSB Data Registers (invoking an automatic conversion) should be performed in the sequence: first the MSB then the LSB.

The Channel sequence is important in 8- or 10-bit modes in the burst mode, see Note 5. When in the Single Transfer mode, care should be taken to address the sequence of represented Channel Addresses, in the order which selected channels were converted. Since conversions occur after a READ of the previous channel converted, the NEXT channel read should be the latest one converted, a conversion is invoked on the NEXT selected channel when finished reading the current one.

An example, WRITE three control registers with SAR = 90 for ENC, SAE, with a CAR = 000 for channel zero, CSR must have CS0 = 1. After retrieving channel zero data, if CS1 = 0 (deselected) and CS2 = 1 (selected) (for instance CSR = FD), simply by waiting for the status INT bit to set (should read: 84 assuming that other channels are selected ACC will be clear) followed by writing address 04 will access the channel two data just converted.

4.2.3 SINGLE SCANNING CONVERSION

In mode 2, the first conversion, determined by the contents of the internal CAR, is initiated as described in the SINGLE CONVERSION mode description. Upon completion of the first conversion in this mode there is no interrupt, the channel address is automatically advanced to the next selected channel and a conversion initiated. Conversions continue until all of the selected channels have been converted. At that time the DV (10-bit mode only), INT, ACC status bits are updated and the $\overline{\text{INT}}$ output activated if enabled.

If hardware interrupts are not desired, polling of either the ACC or INT bits in the STATUS REGISTER will ensure conversions are complete. Functional differences in these bits are times at which they are cleared: The INT bit is cleared on a READ of the STATUS Register while the ACC is cleared after access to the associated Data Register. After conversion completion, the data registers may then be read. This sequence should be performed in the Burst Mode for simplicity, this will ensure the data read is truly the next selected channel without calculation due to this automatic addressing feature. In this fashion, less total SPI transfer cycles are necessary. Burst mode is absolutely necessary in the 10-bit mode. See Note 4 on 10-bit Data Register READS. Be aware of Note 2 when reading back Data.

4.2.4 CONTINUOUS SCANNING

In mode 3 all of the selected channels are continuously converted in sequence, beginning with the channel addressed by the SAR. The INT status bit and $\overline{\text{INT}}$ output are not valid in this mode and remain in a reset state. The conversions are initiated with a WRITE to the SAR. This mode is useful to convert, on short notice, analog channels which have been sampling in the background before attempting to read back the digital data; although when retrieving data the conversions will stop.

When in mode 3, the converter will run free and when data is accessed it will abort the operation. Conversion termination can be performed manually before read back and can be any one of the abort conditions. Writing to the SAR with SAE and ENC bits cleared to a logical LOW level, will wait to allow a conversion in progress to complete before termination. The CIP bit will clear after the current conversion has been terminated. See other abort conditions in appendix, section 5.2. If a conversion is terminated on a channel other than the highest selected one in a frame, there is a chance that some higher channels may actually be from the previous sample frame. More control of data retrieval can be gotten from monitoring of the converter Status Register.

The ACC, CIP, and CAR status bits (all in the STATUS REGISTER) can be monitored to determine the status of the converter, see Note 3. These status bits can be accessed and tested by polling the STATUS REGISTER over the SPI bus, see STATUS REGISTER, section 4.5. After the first pass through a frame of channel conversions, the ACC bit will be set. If the ACC bit has not yet been set, then less than all selected channels will have been converted. Reading the Status Register does not affect the converter. This allows the CIP bit (or any STATUS Register bits) to be polled awaiting the last conversion completion, or upon any desired conditions as best for the application, the proper sequence can be executed for DATA REGISTER access.

After invoking the CONTINUOUS MODE then aborting, monitoring the STATUS register can also supplement mode 3 termination by indicating the first channel converted. The NEXT selected channel in the CSR, following the last conversion, can be observed in the CAR. This happens to be the first channel converted and can be sent back as the first Data Register address for Data retrieval. A test for minimum of one full frame converted is made by testing ACC to be set to a logical HIGH in the CONTINUOUS SCANNING MODE. Knowing that all channels have been converted at least once, allows one to deduce that valid sample data will be read back. The remaining channels can be recovered in the burst mode. This allows fast data retrieval with the earliest channel converted recovered first. Use the burst mode for proper 10-bit operation, see Note 4. Be aware of Note 2 when reading back any data.

4.3 Channel Select Register (CSR)

ADDRESS: ($\overline{\text{R}}$/W)0010001	C7	C6	C5	C4	C3	C2	C1	C0

This READ/WRITE register is used to select the analog input channels. Each of the Cn bits is used to select the corresponding analog input channels, AIn. If the Cn bit is set to a logical HIGH, the corresponding input channel is selected. A logical LOW in a Channel Select bit deselects that channel. Data is maintained in the CSR until new data is written to this register. It is recommended to write to the CSR and reset all status bits whenever invoking conversion operations preceding a write to the SAR. This ensures proper CAR loading if the previous sequence was altered. This can be done in the burst mode, see appendix, section 5.3.2.1.

4.4 Starting Address Register (SAR)

ADDRESS: ($\overline{\text{R}}$/W)0010010	ENC	X	X	SAE	CA2	CA1	CA0	$\overline{\text{M}}$/L

This READ/WRITE register is used to initiate as well as abort conversions and access the Channel Address Register (CAR). Individual bits are described here:

ENC (Enable Conversion)

This bit is used to enable an A/D conversion. If this bit is HIGH, an applicable conversion operation is initiated upon completion of the WRITE to the SAR. If the bit is set to a logical LOW, no conversion is initiated. If a conversion is in progress and the SAR is written to with the ENC and the SAE bit set to a logical LOW, the current conversion will complete and subsequent conversions are inhibited. Useful for continuous mode.

Two "Don't Care" Bits XX

Are just that and are ignored when writing to the SAR. When reading these bits, they will always be at a logical LOW level.

SAE (Starting Address Enable bit)

A HIGH in this bit will allow the contents of the CAR to be set to the address determined by the three Channel Address bits in the SAR. If the bit is at a logical LOW, the channel address bits are not transferred to the internal Channel Address Register (CAR) and the CAR is maintained by the operation of the selected mode. After writing to the SAR once, this bit has no effect until written again; although it stays in the logical active HIGH state.

CAn (Write Binary Encoded Channel Address)

See appendix, section 5.1. These three bits, when written to, determine the new contents internal channel address register. It is usually loaded with the lowest selected channel, but may be loaded with another selected channel, causing that channel to be converted first; hence, the Starting Address Register or SAR, for which this register is named. Subsequent conversions will be performed on channels determined by the CSR. Reading the CAn bits will only indicate what was previously written to this register or if a Data Register access was made, it will be set to that channel address and can change as the Channel Address Increment logic causes the effect of writing to the CAR in the SAR.

$\overline{\text{M}}$/L (The MSByte/LSByte Bit)

This bit is used internally to address the MSB or LSB of 10-bit data registers. This is a READ/WRITE bit which can be set along with the CAR on an SAR WRITE or by addressing a Data Register. This bit can be read to request the current CAR byte order significance following a write to the SAR or a Data Register access when invoking 10-bit conversion (SAE and ENC bits set) or when in the 8-bit mode this bit functions but is not used.

4.5 Status Register

ADDRESS:
00010011

INT	ACC	CIP	0	CA2	CA1	CA0	0

This is a read only register used to monitor the status of the A/D converter. If the STATUS REGISTER is addressed in a read burst operation, the STATUS REGISTER remains selected as long as the CE is active, allowing continuous monitoring of the SPI I/O updates in a polling fashion. The internal Channel Address Register (CAR) is unaffected by reading the STATUS REGISTER; it is incremented in accordance with the mode and channels selected. The contents of the STATUS REGISTER are updated upon the completion of each conversion. If the status of the converter changes while the STATUS REGISTER is being read, the register is not updated until the completion of the read.

INT (Interrupt)

This status bit (active HIGH) provides an equivalent function as the $\overline{\text{INT}}$ pin (active LOW). The bit is set HIGH in modes 1 and 2 as described in the mode select register description. The INT bit is reset to a logical LOW by reading the STATUS REGISTER or writing to the MSR or CSR.

ACC (All Conversions Complete)

This Status bit indicates that conversions have been completed on all of the selected channels or a 'data frame'. The bit is set to logical HIGH when a data frame has been converted. It is reset to a logical LOW by reading any of the data registers or writing to either the MSR or CSR, and remains reset until a subsequent conversion is completed on a all selected channels. In 10-bit mode all DVn bits of selected channel Data Registers are active when this bit is active. It is unaffected by reading the STATUS REGISTER. Useful in modes 2 and 3. This bit will only set in mode 1 if conversions are invoked on all selected channels before there are any data register accesses.

CIP (Conversion In Progress)

This bit is set logically HIGH when a conversion is initiated and reset logically LOW upon completion of a conversion or by writing to either the MSR or CSR. It is unaffected by reading the STATUS REGISTER. Until termination, this bit will remain set in mode three while conversions are enabled.

CAn (Read-Only Channel Address)

These three binary encoded bits represent the current CAR. These address bits are set to the corresponding channel address after activating the internal auto-channel-increment logic. This happens at the end of each conversion and any time following a Register is accessed. Reading these bits while in the CONTINUOUS SCANNING mode will display the changing Channel Addresses of the converter. If the STATUS REGISTER is read while a conversion is initiated, the CAR is unaffected and the address bits are set to the new value upon completion of the read.

Two Zero Bits

These bits are always cleared to a logical LOW and do not function.

5. Appendix

To follow are various references from the preceeding Data Sheet:

5.1 Channel Address Register (CAR)

The channel address is stored and sequenced in the internal CAR. Although this register is not directly accessible, it can be written to by either the SAR or an access to a Data Register. It can be read through the STATUS REGISTER. The CAR has two purposes: it selects the appropriate analog input channel for the analog multiplexer and addresses the corresponding Data Register to be updated. It can be read to determine the $\overline{\text{MOST}}$/LEAST significant byte in the 10-bit mode. To follow is a table of channels of the CAR as seen in the STATUS Register and SAR.

Channel Map

CA2	CA1	CA0	Channel	Pin No.
0	0	0	0	7
0	0	1	1	15
0	1	0	2	14
0	1	1	3	13
1	0	0	4	12
1	0	1	5	11
1	1	0	6	10
1	1	1	7	9

5.1.1 SAR WRITE to the CAR

Writing to the CAR is possible by a direct WRITE to the SAR as noted above. If ENC is logically LOW and SAE is logically HIGH, the auto-increment logic will not be activated and the CAR will be loaded with the three bits of the SAR address and byte significance. This may be verified with a read of the STATUS REGISTER CAR set to the current value (not incremented to the NEXT selected channel address.) If conversions are enabled increment logic will be activated depending on the mode of operation and a selected channel will be pointed to. A read of the SAR will only reflect the value of the last update written to the CAR through one of the two methods of a direct SAR WRITE or a Data Register Access. The $\overline{\text{M}}$/L bit in this register is updated and can be read to request byte order status in the 10-bit mode.

Since the Channel Address Register (CAR) is the internal Data Register sequencer and multiplexer, the value of the CAR will be affected by a Data Register read sequence. This is most important in modes two and three where conversions and Data Retrieval are in two distinct phases of their own both dependent on the inital value of the CAR. In fact, an access to any Data Register will be equivalent to a WRITE to the CAR through the SAR. A complete Data Register READ sequence constitutes reading all selected channels, in this case the CAR value will return to the initial address position. The Burst Transfer mode will automatically perform this on the N+1'th cycle of the readback sequence following N channels converted. This is done by Phase I addressing of the first converted channel followed by N Phase II transfer cycles. Refer to Note 2 concerning incomplete READ sequences.

5.1.2 STATUS Register and SAR READ from CAR

The STATUS REGISTER can be read at any time to determine the Channel Address Register contents. Following a WRITE to the SAR with the SAE bit set, the CAR will be loaded with the start channel address. The actual value observed in the STATUS Register will depend on the state of the auto-increment logic since it is current. The auto-increment function depends on the conversion mode and the operation performed following an SAR WRITE. For instance, if in mode 1, a conversion resulted from the SAR WRITE (ENC set), the channel converted first was the Start Address. The observed address will be the NEXT selected channel (simultaneously initiating a conversion on it) following the channel written in the SAR. In mode 2 the entire frame of data (all selected channels) will have been converted and the CAR will contain the Start Address again ready to repeat the cycle, the last channel is incremented to the next or start channel, see Note 5. The current Most Significant or Least Significant Byte status is contained in the $\overline{\text{MOST}}$/LEAST bit in the SAR for monitoring.

5.2 Abort Conditions

Several illegal operations initiated while a conversion is in progress will cause the current conversion to abort. The data contained in the Data Register corresponding to the current channel conversion may or may not be preserved. The DV and DOV Status bits must be examined to determine the data integrity. The following table lists the conditions which will cause a conversion to abort immediately.

1. WRITE to the MSR.
2. WRITE to the CSR.
3. WRITE to SAR with SAE and/or ENC set to a logical HIGH.
4. Attempt to access any Data Register through the MISO pin. For example, transmitting a valid Read/Data register address control byte.

The exception of the abort conditions, which allows completion of a current conversion in progress, can be excuted by a WRITE to the SAR with the SAE and the ENC bits cleared to a logical LOW.

5.3 Register Allocation Table

This section describes the address map for the internal registers in the CDP68HC68A2. Special instructions are mentioned here for reading data registers. The address maps are also depicted here for clarity.

5.3.1 READ-ONLY DATA REGISTER ALLOCATION TABLE

ADDRESS								CHANNEL	
$\overline{R}$	0	0	A4	A3	A2	A1	A0	10-Bit Mode	8-Bit Mode
0	0	0	0	0	0	0	0	MSB - 0	0
0	0	0	0	0	0	0	1	LSB - 0	
0	0	0	0	0	0	1	0	MSB - 1	1
0	0	0	0	0	0	1	1	LSB - 1	
0	0	0	0	0	1	0	0	MSB - 2	2
0	0	0	0	0	1	0	1	LSB - 2	
0	0	0	0	0	1	1	0	MSB - 3	3
0	0	0	0	0	1	1	1	LSB - 3	
0	0	0	0	1	0	0	0	MSB - 4	4
0	0	0	0	1	0	0	1	LSB - 4	
0	0	0	0	1	0	1	0	MSB - 5	5
0	0	0	0	1	0	1	1	LSB - 5	
0	0	0	0	1	1	0	0	MSB - 6	6
0	0	0	0	1	1	0	1	LSB - 6	
0	0	0	0	1	1	1	0	MSB - 7	7
0	0	0	0	1	1	1	1	LSB - 7	

5.3.1.1 Data Register Access

After invoking conversions in any mode without hardware interrupts, deassertion of CE will be necessary to read the STATUS Register then again to address the Data Registers. Converted Digital Data is retrieved (and validated in 10-bit mode only) from the Data Registers. After a conversion is complete or terminated, the Starting Address (which should have been a selected channel) should be the first Data Register address read. The SAR can initially be set to any of the selected channels to affect the order in which the channel data is retrieved.

5.3.1.1.1 10-bit Mode

In the 10-bit mode, two data registers are associated with each analog input channel. Upon completion of the first conversion, the data is internally stored at the addresses designated by the CAR written in the SAR before converting. The most Significant Byte (MSB) contains the two status bits and the two most significant bits of the 10-bit A/D conversion data. The eight least significant data bits are stored in the Least Significant Byte (LSB). These sixteen registers are read only registers.

The following is the format of the Data Registers in the 10-bit Mode (refer to the register allocation table in appendix, section 5.3.1):

ADDRESS:
00000000(MSB)

DV0	DOV0	0	0	0	0	D9	D8

ADDRESS:
00000001(LSB)

D7	D6	D5	D4	D3	D2	D1	D0

• •
• •
• •

ADDRESS:
00001110(MSB)

DV7	DOV7	0	0	0	0	D9	D8

ADDRESS:
00001111(LSB)

D7	D6	D5	D4	D3	D2	D1	D0

The bits in these registers are described here in more detail:

DVn (Data Valid)

This status bit is used to determine the validity of the conversion stored in the data data register. The DV bit is set HIGH upon completion of an A/D conversion to the corresponding channel. The bit is reset to a logical LOW level when the register is read (see Note 4), or if the MSR, CSR, or SAR is written to. It is also possible for the DV bit to be reset if an abort condition arises while a register is being loaded.

Dn (Data bits)

These ten data bits represent the 10-bit conversion data for the corresponding input channel. The bits are stored (Right Justified) in the two, corresponding eight bit bytes upon completion of the conversion. The data is maintained in the register only until another conversion is completed.

DOVn (Data Overrun)

This status bit is set to a logical HIGH level upon completion of a data conversion to a channel already containing valid data which has not been read. It indicates whether or not the previous data has been overwritten. The bit is reset LOW by reading the register or performing a WRITE to the MSR, CSR or both.

5.3.1.1.2 8-bit Mode

In the 8-bit mode, an 8-bit conversion is performed on the selected channels and stored in the corresponding data register. The status bits associated with Data Registers in the 10-bit mode are not included in the 8-bit mode, thus the STATUS REGISTER must be monitored to determine the status of the conversions. Since the conversion data is stored in a single 8-bit byte in the 8-bit mode, the data for each channel can be obtained with a single read cycle, as compared to two read cycles required in the 10-bit mode. The $\overline{\text{MOST}}$/LEAST bit is a don't care when written to in the 8-bit mode. When reading the Data Registers in the burst mode, the address is automatically incremented to the next selected channel. The read sequence should be complete, see Note 2.

The following is the format of the Data Registers in the 8-bit Mode:

ADDRESS:
0000111X

D7	D6	D5	D4	D3	D2	D1	D0

•
•
•

ADDRESS.
0000000X

D7	D6	D5	D4	D3	D2	D1	D0

The bits in these registers are described here in more detail:

Dn (Data bits)

These eight data bits represent the 8-bit conversion data for the corresponding input channel. The bits are stored in a single eight bit byte upon completion of the conversion. The data is maintained in the register only until another conversion is completed.

5.3.1.1.3 Data Recovery Examples

A general method of implementation for any mode, single transfer or burst transfer is to build external software counter routines in the microcontroller. This method can require more code for more sophisticated designs, but works well when multiple modes are used. In this manner, channel activity in the CDP68HC68A2 is reconstructed for the requesting of appropriate channels within the device.

For Mode 1, a STATUS Register polling routine can wait for proper completion, then yield the next address to be converted (channel in CAR) for anticipation of channel Data Register Address to follow.

A simple method in mode 2 is to load the SAR with the lowest enabled channel then retrieve data beginning with that same address. Continue Phase II implementing the burst mode anticipating the rest of the selected channels to follow. For example CSR = AA, SAR = 92 readback channels 1, 3, 5, 7 in the Burst Mode beginning with address 02 (Channel 1). Four channels are converted then read back. Counting the number of CSR bits can determine total number of channels to retrieve.

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Another, more complicated mode 2 example follows: if converting channels 1, 3, 5, and 7 (SCR = AA), with SAR = 96. This starts conversions with channel 3. Upon completion, begin reading Data from Register address 06 (MSByte channel 3, possibly save CAn bits upon writing to the SAR) and retrieve channel 3 followed by 5, 7 then 1. On the readback in the burst mode the address logic is automatically incremented to the next selected channel.

5.3.2 CONTROL and READ ONLY STATUS REGISTER ALLOCATION

ADDRESS								REGISTER	
$\overline{R}$/W	0	0	A4	A3	A2	A1	A0		
0/1	0	0	1	0	0	0	0	MSR	MODE SELECT REGISTER
0/1	0	0	1	0	0	0	1	CSR	CHANNEL SELECT REGISTER
0/1	0	0	1	0	0	1	0	SAR	STARTING ADDRESS REGISTER
0	0	0	1	0	0	1	1	STATUS	STATUS REGISTER

5.3.2.1 Control and Status Register Burst Access

Control registers may be read or written to independently with Single Byte transfers, or sequentially with a Burst transfer. When WRITING to control registers for conversions, the initial address will be the MSR ($90) followed by SAR ($91) then the CAR ($92). Since they are ascending consecutive addresses, the WRITE Burst Mode can be used by addressing register $90 (Phase I) then perform three more SPI transfer cycles (Phase II) to get at the MSR, CSR and the SAR requiring four SPI cycles, If it were a read operation only, the address would change to ($10).

5.4 Analog Section

The purpose of this section is to familiarize the user with the analog interface circuitry necessary for proper operation as specified.

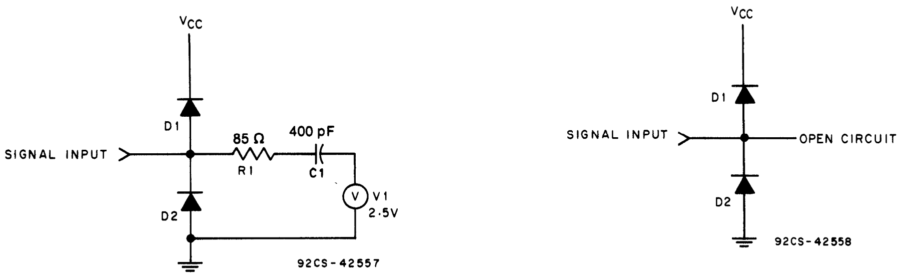
5.4.1 The Analog Input Mode

Shown here is a simplified equivalent circuit representing the input to the Analog to Digital Converter through the multiplexer as seen from each An pin.

Due to the nature of the switched capacitor array used for determination of the Digital Output Word, two important points are noted here:

1. A property of a capacitive input after sufficient charging (or discharging) has taken place, is the intrinsic sample and hold function, which is a feature in this case. This provides all that is necessary to accurately sample a point on an input waveform within the input bandwidth shown in the specifications, which is under 1.5 conversion oscillator cycles. If a resistor ladder A/D were used, an external sample and hold circuit would be required.
2. The input to the capacitor network appears as an RC network with a time constant and therefore places constraints on the source impedance. The charging time and therefore the accuracy of the conversion will be adversly affected by increasing the source impedance.

It is therefore recommended to set the conversion oscillator frequency in accordance with the input impedance in order to allow sufficient time (the 1.53 Tosc cycles) to sample a



(a) During sample time.

(b) During hold and idle time.

Fig. 5 - Equivalent circuit for signal input (a) during sample time and (b) during hold and idle time.

changing waveform through the modeled input low pass filter network which includes the input source in a series circuit with the internal impedance. Combined, this is the effective impedance.

The time constant (τ) for the input network is $R_{eff}C_{net}$.

$R_{eff} = R_s + R_{net}$, C_{net} = 400 pF, and $R_{net} = 85\Omega$.

$\tau = R_{eff}C_{net} = (R_s + 85\Omega)$ 400 pF.

8τ is required during the first 1.5 sample clock cycles to sufficiently encode 10-bit conversion. Therefore, $1.5\,T_s \geq 8\tau$ and $T_s \geq 5.33\ R_{eff}C$.

$T_s = 1/f_{sample}$, then $f_{sample} \leq [5.33\ (R_s + 85\Omega)\ 400\ \text{pF}]^{-1}$, $f_{sample} \leq (4.688 \times 10^8)/(R_s + 85\Omega)$.

For example, $R_s = 1000$ f_{sample} must be less than 432 kHz.

$T_s = 2.3\ \mu s$, this yields a 10-bit conversion time of 32 μs. An internal $C_{osc} \geq 68$ pF, see chart.

The maximum frequency is limited by the device specification, see characteristics. Conversely, by limiting the (R_s) Series input resistance:

$R_s \leq [(4.688\times10^8)/f_{sample}] - 85\Omega$.

For example, for a 1 MHz sample clock R_s max = 385Ω. Consequently, the 10-bit conversion time is $14\ T_s = 14\ \mu s$.

5.4.2 The Internal Schmitt Oscillator

Fig. 6 shows a simplified model of the Schmitt oscillator used to help familiarize the user with its operation. The following describes the characteristics of the internal oscillator frequency versus capacitance at 5 volts and 25° C

C (pF)	f (MHz)	C (pF)	f (MHz)
18.7	1.07	218.7	0.148
38.7	0.656	318.7	0.111
48.7	0.545	409.7	0.107
68.7	0.387	528.7	0.072
118.7	0.261	1018.7	0.040

Always remember, when measuring the oscillator, probe capacitance will affect frequency. An alternative to direct frequency measurement of the oscillator input is to measure the internal between successive interrupts in modes 1 and 2. A pullup-resistor on the $\overline{\text{INT}}$ pin will facilitate a positive swing.

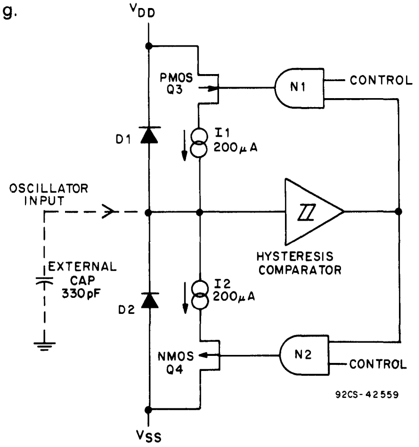


Fig. 6 - Equivalent circuit for oscillator input.

5.5 Notes

Note 1: When addressing the CDP68HC68A2, CE should always (especially important when more than one SPI peripheral are on the same SPI bus):

A) Be activated for the duration of both phases of a Single or Burst Mode transfer for a valid operation. This encompasses two SPI cycles for single byte transfers and greater than two SPI cycles for multiple byte transfer or burst mode.

B) Be deactivated some time before it is necessary to access the SPI bus for any other reason than to complete the last operation. This resets the SPI logic and tristates the MISO line from driving the SPI bus. Re-addressing will always be necessary after deassertion of the chip enable.

Note 2: The internal Channel Address Register (CAR) is affected by a Data Register access and will change the next START ADDRESS to be converted if the read sequence is incomplete. A READ sequence is complete when Data Registers READS exactly span all of the selected channels. Then, the CAR contents observed in the STATUS register will equal the initial value written to the SAR before Register Access and the SAE would not need to be activated. The effect of incomplete READ sequences can be avoided by always writing to all three of the CONTROL REGISTERS at the initialization of conversions. For example, addressing a WRITE to the MSR, CSR, then the SAR. This may be followed by addressing a read of the STATUS REGISTER if desired. Further conversions in the same mode may be initiated when the control register sequence is written with the CSR followed by the SAR. This sequence forces resetting of all status bits for successive operations.

Note 3: Status and Control Registers can be examined (read) without affecting the conversion.

Note 4: When in the burst mode, a Data Register, when first retrieved, will have already internally addressed the next corresponding selected channel Data Register. This occurs because the auto-increment logic activates at the end of a Data Register read. Because of this, it is necessary to complete the read of all valid channels in order to test the validity of the DV bit before the CE is deactivated. It appears most convenient and necessary in this case, to access channels from Starting Address to the last valid data conversion by the burst mode. Important in modes 2 and 3 since all conversions are complete when Data is retrieved and the DV bit cleared at the time of addressing.

Note 5: In the burst mode, the REGISTER ALLOCATION TABLES can be accessed and will auto-increment to sequential addresses and selected channels. While in the burst mode, both data register address and channel address beyond the highest selected channel is the lowest selected channel. This implies that re-addressing is necessary if control and status registers need to be accessed following data registers. For example, a READ of channel 7 (address 0F) will not be followed by a READ of the MSR, but Data Register 0 (address 00).

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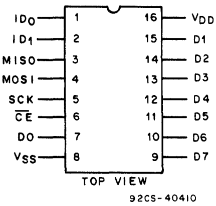
Advance Information



TERMINAL ASSIGNMENT

CMOS Single Port Input/Output

Features:

- *Fully static operation*
- *Operating voltage range 3-6 V*
- *Compatible with RCA/Motorola SPI bus*
- *2 external address pins tied to V_{DD} or V_{SS} to allow up to 4 devices to share the same chip enable*
- *Versatile bit-set and bit-clear capability*
- *Accepts either SCK clock polarity - SCK voltage level is latched when chip enable goes active*
- *All inputs are Schmitt-Trigger*
- *8-Bit I/O port - each bit can be individually programmed as an input or output via an 8-bit data direction register*
- *Programmable on-board comparator*
- *Simultaneous transfer of compare information to CPU during read or write - separate access not required*

The single port I/O is a serially addressed 8 bit Input/Output port that allows byte or individual bit control. It consists of three registers, an output buffer and control logic. Data is shifted in and out of the port via a shift register that utilizes the SPI (Serial Peripheral Interface) bus. The I/O port data flow is controlled by the Data Direction Register and data is stored in the Data Register that outputs or senses the logic levels at the buffered I/O pins. All inputs, including the serial interface are schmitt triggered. The device also features a compare function that compares the data register and port pin values for 4 programmable conditions and sets a software accessible flag if the condition is satisfied. The user also has the option of bit-set or bit-clear when writing to the data register.

The CDP68HC68P1 is supplied in 16-lead, hermetic, dual-in-line side-brazed ceramic (D suffix), 16-lead dual-in-line plastic (E suffix) and 16-lead, surface mount, (small outline), plastic (M suffix) packages.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltage referenced to V_{SS} terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to 125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)*	400 mW
For T_A = +70 to +85°C (PACKAGE TYPE M)*	Derate Linearly at 6 mW/°C to 310 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

RECOMMENDED OPERATING CONDITIONS AT T_A = -40° to +85° C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS ALL TYPES MIN.	LIMITS ALL TYPES MAX.	UNITS
DC Operating Voltage Range		3	6	V
Serial Clock Frequency	f_{SCK}			MHz
	V_{DD} = 3 V	—	1.05	
	V_{DD} = 4.5 V	—	2.1	
Input Voltage Range				V
	V_{IH}	—	V_{DD} + 0.3	
	V_{IL}	-0.3	—	

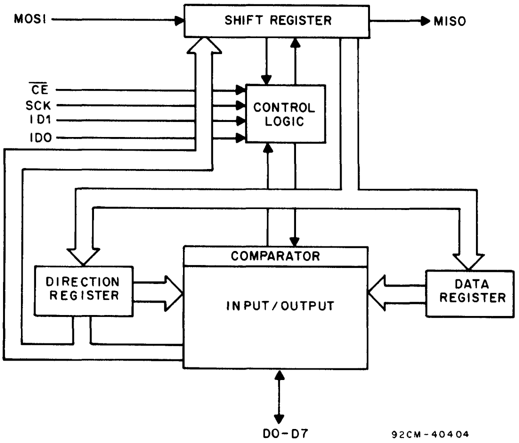


Fig. 1 - Single port I/O block diagram.

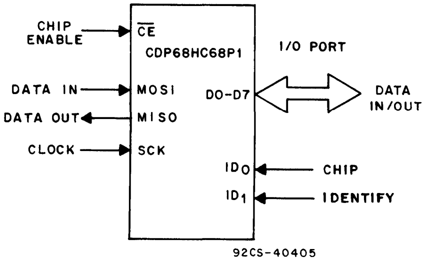


Fig. 2 - Single port I/O.

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STATIC ELECTRICAL CHARACTERISTICS AT T_A = -40 to +85° C, V_{DD} = 3.3 V ± 10%, Except as Noted

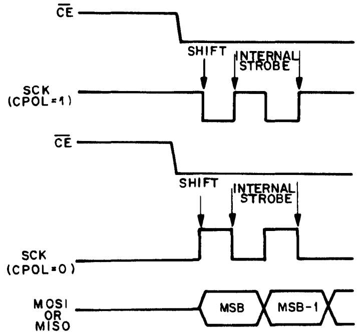
CHARACTERISTIC		CONDITIONS	LIMITS			UNITS
			MIN.	TYP. •	MAX.	
Standby Device Current	I_{DDS}	—	—	1	15	μA
Output Voltage High Level	V_{OH}	I_{OH} = -0.4 mA, V_{DD} = 3 V	2.7	—	—	V
Output Voltage Low Level	V_{OL}	I_{OL} = 0.4 mA, V_{DD} = 3 V	—	—	0.3	
Input Voltage						
D0-D7						
Positive Trigger Threshold	V_P	—	1.85	—	2.4	
Negative Trigger Threshold	V_N	—	0.85	—	1.35	
Hysteresis	V_{IH}	—	0.85	—	1.25	
Input Voltage						
ID0, ID1, MOSI, SCK, $\overline{CE}$						
Positive Trigger Threshold	V_P	—	1.3	—	1.9	
Negative Trigger Threshold	V_N	—	0.8	—	1.2	
Hysteresis	V_{IH}	—	0.5	—	0.95	
Input Leakage Current	I_{IN}	—	—	—	±1	μA
3-State Output Leakage Current	I_{OUT}	—	—	—	±10	
Operating Device Current	I_{OPER} #	V_{IN} = V_{IL}, V_{IH}	—	0.1	1	mA
Input Capacitance	C_{IN}	V_{IN} = 0 V, f = 1 MHz, T_A = 25° C	—	4	6	pF

• Typical values are for T_A = 25° C and nominal V_{DD}. # Outputs open circuited; cycle time = Min. t_{cycle}, duty = 100%.

STATIC ELECTRICAL CHARACTERISTICS AT T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Except as Noted

CHARACTERISTIC		CONDITIONS	LIMITS			UNITS
			MIN.	TYP. •	MAX.	
Standby Device Current	I_{DDS}	—	—	1	15	μA
Output Voltage High Level	V_{OH}	I_{OH} = -1.6 mA, V_{DD} = 4.5 V	3.7	—	—	V
Output Voltage Low Level	V_{OL}	I_{OL} = 1.6 mA, V_{DD} = 4.5 V	—	—	0.4	
Output Voltage High Level	V_{OH}	$I_{OH} \leq$ 20 μA, V_{DD} = 4.5 V	4.4	—	—	
Output Voltage Low Level	V_{OL}	$I_{OL} \leq$ 20 μA, V_{DD} = 4.5 V	—	—	0.1	
Input Voltage						
D0-D7						
Positive Trigger Threshold	V_P	—	2.15	—	3.05	
Negative Trigger Threshold	V_N	—	1.35	—	2	
Hysteresis	V_{IH}	—	0.8	—	1.2	
Input Voltage						
ID0, ID1,MOSI, SCK, $\overline{CE}$						
Positive Trigger Threshold	V_P	—	3.15	—	3.85	
Negative Trigger Threshold	V_N	—	1.7	—	2.25	
Hysteresis	V_{IH}	—	1.3	—	1.7	
Input Leakage Current	I_{IN}	—	—	—	±1	μA
3-State Output Leakage Current	I_{OUT}	—	—	—	±10	
Operating Device Current	I_{OPER}#	V_{IN} = V_{IL}, V_{IH}	—	0.2	2	mA
Input Capacitance	C_{IN}	V_{IN} = 0 V, f = 1 MHz, T_A = 25° C	—	4	6	pF

• Typical values are for T_A = 25° C and nominal V_{DD}. # Outputs open circuited; cycle time = Min. t_{cycle}, duty = 100%.



92CS-40397

NOTE
CPOL AND CPHA ARE BITS IN THE CDP68HC05C4 and CDP68HC05D2 MCU CONTROL REGISTER AND DETERMINE INACTIVE CLOCK POLARITY AND PHASE CPHA MUST ALWAYS EQUAL 1

Fig. 3 - Data transfers utlizing clock input.

Introduction

The single port I/O is serially accessed via a 3 wire plus chip enable synchronous bus. It features 8 data pins that are programmed as inputs or outputs. Serial access consists of a two-byte operation. The first byte shifted in is the control byte that configures the device. The second byte transferred is the data byte that is read from or written to the data register or data direction register. This data byte can also be programmed to act as a mask to set or clear individual bits.

Functional Description

The single port I/O consists of three byte-wide registers, (data direction, data and shift) an input/output buffer and control logic circuitry. (See fig. 1, block diagram). Data is transferred between the I/O data and data direction registers via the shift register. Once the I/O port is selected, the first byte shifted in to the shift register is the control byte that register selects, (the Data or Data direction register), determines data transfer direction (read or write) and sets the compare feature and function (mask or data) of the byte immediately following the control byte, the data byte. (See Addressing the Single Port I/O) Each bit of the data register may be individually programmed as an input or output. A logic low in a data direction bit programs that pin as an input, a logic high makes it an output. A read operation of data register pins programmed as inputs reflects the current logic level present at the buffered port pins. A read operation of those data register pins programmed as outputs indicates the last value written to that location. At power-up, all port pins are configured as unterminated inputs. Two chip identify pins are used to allow up to 4 I/O ports to share the same chip enable signal. The first two bits shifted in are compared with the hardwired levels at the chip identify pins to enable the selected I/O for serial data transfer. Note that when chip enable becomes true, the compare flag is latched for all devices sharing the same chip enable.

Compare Function

The value of a port pin (D0-D7), configured as an input, is compared with the corresponding bit value (DR0-DR7) stored in the Data Register. Pins configured as outputs are assumed to have the same value as the corresponding bit stored in the Data Register. The compare function is programmed via C01 and C00 (CM1, CM0) of the Address Byte. The following values for CM1 and CM0 will sense one of four separate conditions:

CM1	CM0	Condition
0	0	- at least one non-match
0	1	- all match
1	0	- all are non-match
1	1	- at least one match

The compare flag is set to one when the programmed condition is satisfied. Otherwise, the flag is cleared to zero. The compare flag is latched when the device is enabled (a transition of $\overline{CE}$ from "High" to "Low").

CDP68HC68P1

Data Format

During write operations, the data byte that follows the control byte is normally the data word that is transferred to the data or data direction register. Control bits 2 and 3 (DF0 and DF1) change the interpetation of this data as listed below. Note that one or more bits can be set or cleared in either register without having to write to bits not requiring change.

C03 DF1	C02 DF0	OPERATION
0	X	Data following the control word will be written to the selected register.
1	0	Data following the control word is a mask. Those bits which are a 1 will cause that register flip-flop to be cleared to 0. Those which are a 0 will cause that register flip-flop to be unchanged.
1	1	Data following the control word is a mask. Those bits which are a 1 will cause that register flip-flop to be set to 1; those which are a 0 will cause that register flip-flop to be unchanged.

for example,

CONTROL	DATA	PREVIOUS REGISTER VALUE	NEW REGISTER VALUE
C07 C06 C05 1 0 X C01 C00	11110000	10101010	11110000
C07 C06 C05 1 1 1 C01 C00	11110000	10101010	11111010
C07 C06 C05 1 1 0 C01 C00	11110000	10101010	00001010
C07 C06 C05 1 1 X C01 C00	00000000	10101010	10101010

X = Don't Care

Addressing the Single Port I/O

The Serial Peripheral Interface (SPI) utilized by the I/O Port is a serial synchronous bus for control and data transfers. It consists of a SCK clock input pin that shifts data out of the I/O port (MISO, MASTER IN, SLAVE OUT) and latches data presented at the input pin, MOSI (master out, slave in). Data is transferring in most significant bit first. There is one SCK clock for each bit transferred and bits are transferred in groups of eight.

When the I/O port is selected by bringing the chip enable pin low, the logic level at the SCK input is sampled to determine the internal latching and shift polarity for input and output signals on the SPI. (See Fig. 3).

The first byte shifted in when the chip is selected is always the control byte followed by one or more bytes that become data or a mask for the data and data direction register. As the control byte is being shifted in one the MOSI line, data on the MOSI line shifts out. (See Fig. 4).

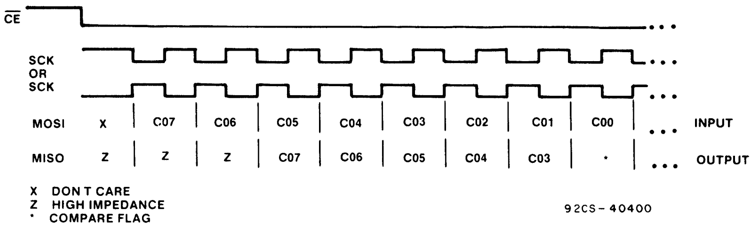


Fig. 4 - Control byte.

C07 (ID1), C06 (ID0): Chip-Identify bits

C05 (RS): Register Select. When RS is low, the data register is selected. When RS is high, the Direction Register is selected.

C04 ($\overline{R}$/W): $\overline{\text{Read}}$/Write. Low when data is to be transferred from the SPI I/O to the CPU (read) and high when the I/O is receiving data from the CPU (write).

C03 (DF1), C02 (DF0): Data Format Bits. These have meaning only when $\overline{R}$/W is high. During a write operation, DF1 and DF0 control how the byte following the control word is interpreted. See "DATA FORMAT".

C01 (CM1), C00 (CM0): Compare Mode Select. These bits select one of four events which will set the internal Condition Flag. (See "COMPARE OPERATION")

Read Operation

During a read operation, the CPU transfers data from the I/O by first sending a control byte on the MOSI line while the chip-selected I/O sends compare information followed by one or more data bytes on the MISO line.

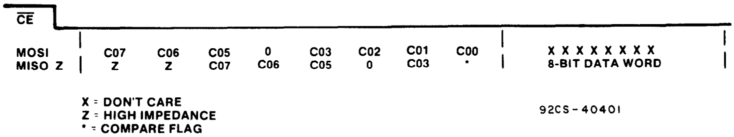
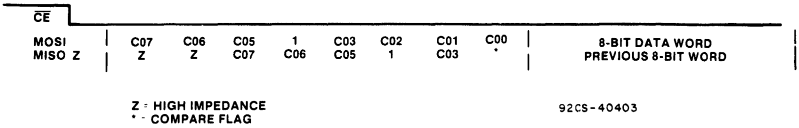


Fig. 5 - Read bytes.

The selected register will be continuously read if $\overline{CE}$ is held low after the first data byte is shifted out.

Write Operation

During a write operation, the data byte follows the control byte for the selected register. While this byte is being shifted in, old data from that register is shifted out. If CE remains low after the data byte is shifted in, MISO becomes high impedance and the new data is placed in the selected register.



At the time the eighth data bit is strobed into the data pins (D0-D7) will change as indicated in Fig. 7.

Fig. 6 - Write bytes.

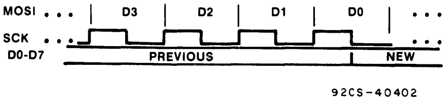


Fig. 7 - Port-pin data changes.

Pin Description

ID0, ID1

Chip identify pins, normally tied to V_{DD} or V_{SS}. The 4 possible combinations of these pins allow 4 I/Os to share a common chip enable. When the levels at these pins match those of the identify bits in the control word, the serial bus is enabled. The chip identify pins will retain their previous logic state if the lines driving them become Hi-Z.

MISO

Master-in, Slave out pin. Data bytes are shifted out at this pin most significant bit first. When the chip enable signal is high, this pin is Hi-Z.

MOSI

Master-out, Slave in pin. Data bytes are shifted in at this pin most significant bit first. This pin will retain its previous logic state if its driving line becomes Hi-Z.

SCK

Serial clock input. This input causes serial data to be latched from the MOSI input and shifted out on the MISO output.

$\overline{\text{CE}}$

A negative chip enable input. A high to low transition on this pin latches the inactive SCK polarity and compare flag and indicates the start of a data transfer. The serial interface logic is enabled only when CE is low. This pin will retain its previous logic state if its driving line becomes Hi-Z.

D0-D7

I/O Port pins. Individual programmable inputs or outputs.

V_{DD} and V_{SS}

Positive and negative power supply line.

All pins except the power supply lines and MISO have Schmitt-trigger buffered inputs.

DYNAMIC ELECTRICAL CHARACTERISTICS - BUS TIMING V_{DD} ± 10%, V_{SS} = 0 V dc, T_A = -40° to +85°C, C_L = 200 pF. See Figs. 8 and 9.

CHARACTERISTIC		LIMITS (ALL TYPES)				UNITS
		V_{DD} = 3.3 V		V_{DD} = 5 V		
		MIN.	MAX.	MIN.	MAX.	
Chip Enable Set-Up Time	t_{EVCV}	200	—	100	—	ns
Chip Enable after Clock Hold Time	t_{CVEX}	250	—	125	—	
Clock Width High	t_{WH}	400	—	200	—	
Clock Width Low	t_{WL}	400	—	200	—	
Data In to Clock Set-Up Time	t_{DVCV}	200	—	100	—	
Data In after Clock Hold Time	t_{CVDX}	200	—	100	—	
Clock to Data Propagation Delay	t_{CVDV}	—	200	—	100	
Chip Disable to Output High Z	t_{EXQZ}	—	200	—	100	
Output Rise Time	t_r	—	200	—	100	
Output Fall Time	t_f	—	200	—	100	
Clock to Data Out Active	t_{CVQX}	—	200	—	100	
Clock Recovery Time	t_{REC}	200	—	200	—	

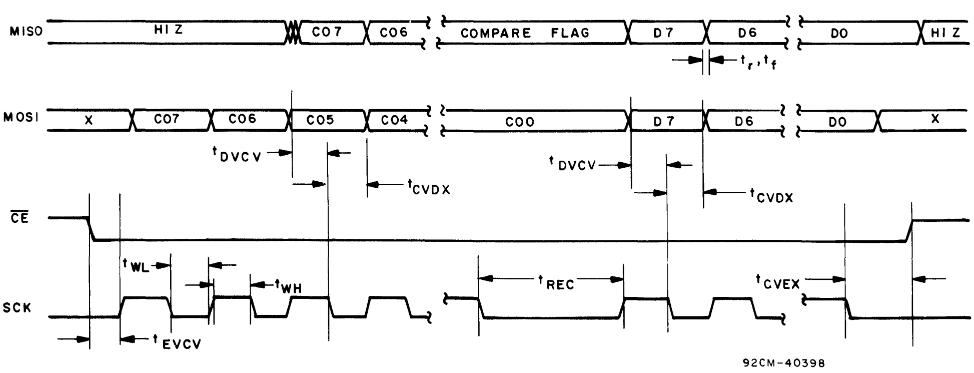


Fig. 8 - Write cycle timing waveforms.

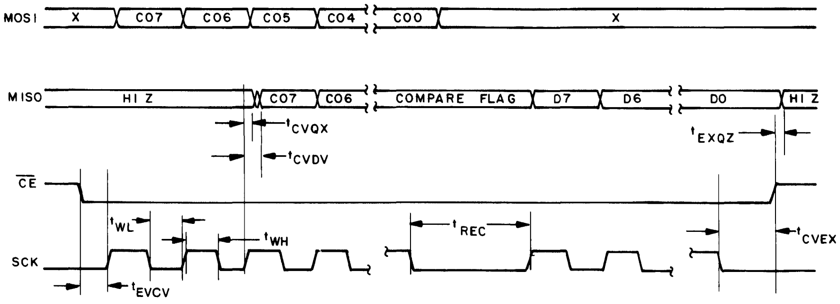
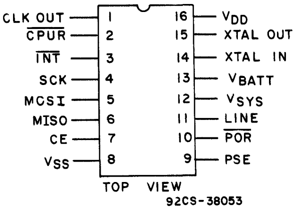


Fig. 9 - Read cycle timing waveforms.

CDP68HC68T1

Advance Information



TERMINAL ASSIGNMENT

CMOS Real-Time Clock with RAM and Power Sense/Control

Features:

- *SPI (Serial Peripheral Interface)*
- *Full clock features: sec., min., hrs. (12/24, AM/PM), day of week, date, month, year, (0-99), auto leap year*
- *32-word x 8-bit RAM*
- *Seconds, minutes, hours alarm*
- *Automatic power loss detection*
- *Minimum standby (timekeeping) voltages: 2.2 volts*
- *Selectable crystal or 50/60-Hz line input*
- *Buffered clock output*
- *Battery input pin that powers oscillator and also connects to the V_{DD} pin when main power fails*
- *Three independent interrupt modes: alarm, periodic or power-down sense*

The CDP68HC68T1, real-time clock provides a time/calendar function, a 32 byte static RAM and a 3-wire serial peripheral interface (SPI bus). The primary function of the clock is to divide down a frequency input that can be supplied by the on-board oscillator in conjunction with an external crystal or by an external clock source. The clock either operates with a 32+kHz, 1+MHz, 2+MHz or 4+MHz crystal or it can be driven by an external clock source at the same frequencies. In addition, the frequency can be selected to allow operation from a 50 or 60-Hz input. The time registers furnish seconds, minutes, and hours data while the calendar registers offer day of week, date, month and year information. The data in the time/calendar registers is in BCD format. In addition, 12 or 24-hour operation can be selected with an AM-PM indicator available in the 12-hour mode. The T1 has a separate clock output that supplies one of 7 selectable frequencies.

Computer handshaking is established with a "wired or" interrupt output. The interrupt can be activated by any one of three separate internal sources. The first is an alarm circuit that consists of seconds, minutes and hours alarm latches that trigger the interrupt when they are in coincidence with the value in the seconds, minutes and hours time counters. The second interrupt source is one of 15 periodic signals that range from subsecond to daily intervals. The final interrupt source is from the power-sense circuit that is used with the LINE input pin to monitor power failures. Two other pins, the power supply enable (PSE) output and the V_{SYS} input are used for external power control. The $\overline{CPUR}$ reset output pin is available for power-down operation and is activated under software control. $\overline{CPUR}$ is also activated by a watchdog circuit that if enabled requires the CPU to toggle the CE pin periodically without a serial data transfer.

The CDP68HC68T1 is available in a 16-lead hermetic dual-in-line ceramic package (D suffix), in a 16-lead dual-in-line plastic package (E suffix), and in a 20-lead small-outline plastic package (M suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltage referenced to V_{SS} terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS EXCEPT LINE	-0.5 to V_{DD} +0.5 V
$V_{SYS} \leq V_{DD}$ + 1.5 V	
DC INPUT CURRENT, ANY ONE INPUT (LINE INPUT, -10 mA)	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 12 mW/° C to 200 mW
For T_A = -55 to +100° C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D)	Derate Linearly at 12 mW/° C to 200 mW
For T_A = -40° to +70° C (PACKAGE TYPE M) *	400 mW
For T_A = +70° to +85° C (PACKAGE TYPE M) *	Derate linearly at 6.0 mW/° C to 310 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	40 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125° C
PACKAGE TYPE E and M	-40 to +85° C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent

File Number **1547**

OPERATING CONDITIONS at T_A = -40° to +85°C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS		UNITS
		Min.	Max.	
DC Operating Voltage Range		3	6	V
DC Standby (Timekeeping) Voltage *	V_{STBY}	2.2	—	
Input Voltage Range	V_{IH}	0.7 V_{DD}	V_{DD} + 0.3	
(Except Line Input)	V_{IL}	-0.3	0.3 V_{DD}	
Serial Clock Frequency (V_{DD} = 4.5 V)	f_{SCK}	—	2.1	MHz

* Timekeeping function only, no READ/WRITE accesses

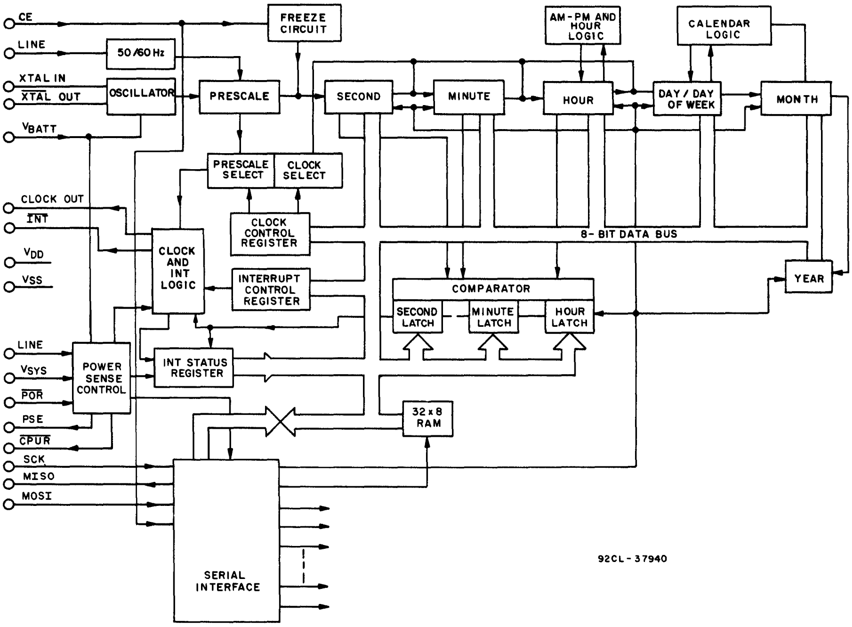


Fig. 1 - Real-time clock functional diagram.

CDP68HC68T1

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = V_{BATT} = 5 V ± 5%, Except as Noted

<table>
<tr><th rowspan="3">CHARACTERISTIC</th><th rowspan="3">CONDITIONS</th><th colspan="5">LIMITS</th><th rowspan="3">UNITS</th></tr>
<tr><th colspan="5">CDP68HC68T1</th></tr>
<tr><th>MIN.</th><th colspan="2">TYP.•</th><th colspan="2">MAX.</th></tr>
<tr><td>Quiescent Device Current I_{DD}</td><td>—</td><td>—</td><td colspan="2">1</td><td colspan="2">10</td><td>µA</td></tr>
<tr><td>Output Voltage High Level V_{OH}</td><td>I_{OH} = -1.6 mA, V_{DD} = 4.5 V</td><td>3.7</td><td colspan="2">—</td><td colspan="2">—</td><td rowspan="4">V</td></tr>
<tr><td>Output Voltage Low Level V_{OL}</td><td>I_{OL} = 1.6 mA, V_{DD} = 4.5 V</td><td>—</td><td colspan="2">—</td><td colspan="2">0.4</td></tr>
<tr><td>Output Voltage High Level V_{OH}</td><td>$I_{OH} \leq 10$ µA, V_{DD} = 4.5 V</td><td>4.4</td><td colspan="2">—</td><td colspan="2">—</td></tr>
<tr><td>Output Voltage Low Level V_{OL}</td><td>$I_{OL} \leq 10$ µA, V_{DD} = 4.5 V</td><td>—</td><td colspan="2">—</td><td colspan="2">0.1</td></tr>
<tr><td>Input Leakage Current I_{IN}</td><td>—</td><td>—</td><td colspan="2">—</td><td colspan="2">±1</td><td rowspan="2">µA</td></tr>
<tr><td>3-State Output Leakage Current I_{OUT}</td><td>—</td><td>—</td><td colspan="2">—</td><td colspan="2">±10</td></tr>
<tr><td rowspan="4">Operating Current#
(I_D + I_b) V_{DD} = V_B = 5 V
Crystal Operation</td><td>32 kHz</td><td>—</td><td colspan="2">0.08</td><td colspan="2">0.1</td><td rowspan="8">mA</td></tr>
<tr><td>1 MHz</td><td>—</td><td colspan="2">0.5</td><td colspan="2">0.6</td></tr>
<tr><td>2 MHz</td><td>—</td><td colspan="2">0.7</td><td colspan="2">0.84</td></tr>
<tr><td>4 MHz</td><td>—</td><td colspan="2">1</td><td colspan="2">1.2</td></tr>
<tr><td rowspan="4">Pin 14
External Clock (Squarewave)#
(I_D + I_b) V_{DD} = V_B = 5 V</td><td>32 kHz</td><td>—</td><td colspan="2">0.02</td><td colspan="2">0.024</td></tr>
<tr><td>1 MHz</td><td>—</td><td colspan="2">0.1</td><td colspan="2">0.12</td></tr>
<tr><td>2 MHz</td><td>—</td><td colspan="2">0.2</td><td colspan="2">0.24</td></tr>
<tr><td>4 MHz</td><td>—</td><td colspan="2">0.4</td><td colspan="2">0.5</td></tr>
<tr><td rowspan="4">Standby Current# I_b
V_B = 3 V
Crystal Operation</td><td>32 kHz</td><td>—</td><td colspan="2">20</td><td colspan="2">25</td><td rowspan="6">µA</td></tr>
<tr><td>1 MHz</td><td>—</td><td colspan="2">200</td><td colspan="2">250</td></tr>
<tr><td>2 MHz</td><td>—</td><td colspan="2">300</td><td colspan="2">360</td></tr>
<tr><td>4 MHz</td><td>—</td><td colspan="2">500</td><td colspan="2">600</td></tr>
<tr><td rowspan="5">Operating Current#
V_{DD} = 5 V, V_B = 3 V
Crystal Operation</td><td rowspan="2">32 kHz</td><td rowspan="2">—</td><td>I_D</td><td>I_B</td><td>I_D</td><td>I_B</td></tr>
<tr><td>25</td><td>15</td><td>30</td><td>20</td></tr>
<tr><td>1 MHz</td><td>—</td><td>0.08</td><td>0.15</td><td>0.1</td><td>0.18</td><td rowspan="3">mA</td></tr>
<tr><td>2 MHz</td><td>—</td><td>0.15</td><td>0.25</td><td>0.18</td><td>0.3</td></tr>
<tr><td>4 MHz</td><td>—</td><td>0.3</td><td>0.4</td><td>0.36</td><td>0.5</td></tr>
<tr><td>Standby Current# I_b
V_B = 2.2 V
Crystal Operation</td><td>32 kHz</td><td>—</td><td colspan="2">10</td><td colspan="2">12</td><td>µA</td></tr>
<tr><td>Input Capacitance C_{IN}</td><td>V_{IN} = 0, T_A = 25°C</td><td>—</td><td colspan="2">—</td><td colspan="2">2</td><td>pF</td></tr>
<tr><td>Maximum Rise and Fall Times t_r, t_f
(Except XTAL Input and $\overline{POR}$ Pin 10)</td><td>—</td><td>—</td><td colspan="2">—</td><td colspan="2">2</td><td>µs</td></tr>
<tr><td>Input Voltage (Line Input Pin Only, Power-Sense Mode)</td><td>—</td><td>0</td><td colspan="2">10</td><td colspan="2">12</td><td rowspan="2">V</td></tr>
<tr><td>$V_{SYS} > V_B$ V_t
(For V_B Not Internally Connected to V_{DD})</td><td>—</td><td>—</td><td colspan="2">0.7</td><td colspan="2">—</td></tr>
<tr><td>Power-On Reset ($\overline{POR}$) Pulse Width</td><td></td><td>100</td><td colspan="2">75</td><td colspan="2">—</td><td>ns</td></tr>
</table>

• Typical values are for T_A = 25°C and nominal V_{DD}.

# Clock Out (Pin 1) disabled, outputs open-circuited. No serial access cycles.

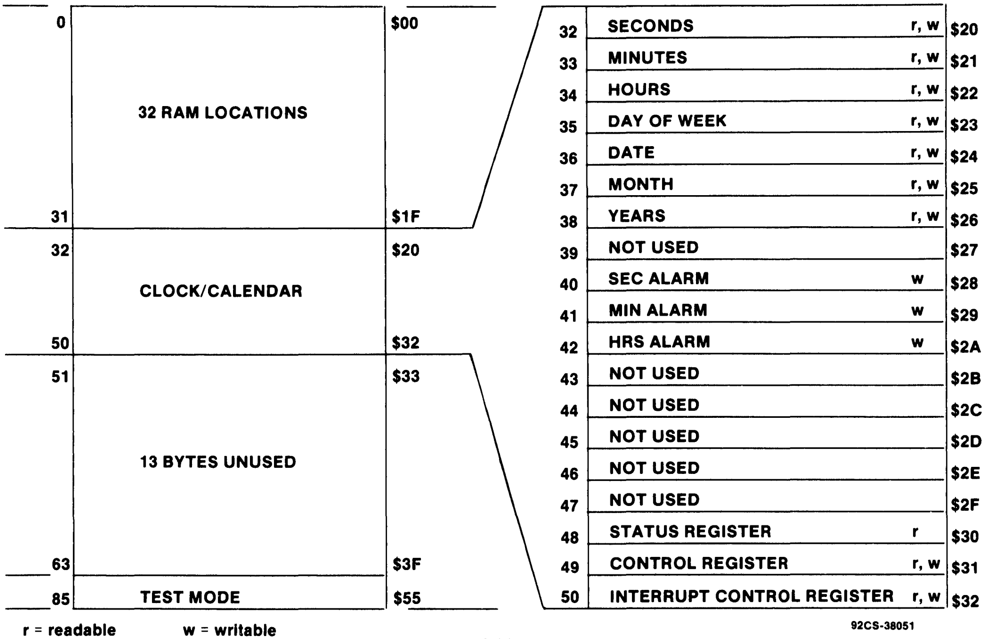


Fig. 2 - Address map.

TABLE I - Clock/Calendar and Alarm Data Modes

ADDRESS LOCATION (H)	FUNCTION	DECIMAL RANGE	BCD DATA RANGE	BCD DATE • EXAMPLE
20	Seconds	0-59	00-59	18
21	Minutes	0-59	00-59	49
22	* Hours 12 Hour Mode	1-12	81-92 (AM) A1-B2 (PM)	A3
	Hours 24 Hour Mode	0-23	00-23	15
23	Day of the Week (Sunday = 1)	1-7	01-07	03
24	Day of the Month (Date)	1-31	01-31	29
25	Month Jan = 1, Dec = 12	1-12	01-12	10
26	Years	0-99	00-99	85
28	Alarm Seconds	0-59	00-59	18
29	Alarm Minutes	0-59	00-59	49
2A	** Alarm Hours 12 Hour Mode	1-12	01-12 (AM) 21-32 (PM)	23
	Alarm Hours 24 Hour Mode	0-23	00-23	15

• Example 3:49·18, Tuesday, Oct. 29, 1985.

* Most significant Bit, D7, is "0" for 24 hours, and "1" for 12 hour mode. Data Bit D5 is "1" for P.M and "0" for A.M. in 12 hour mode.

** Alarm hours, Data Bit D5 is "1" for P.M and "0" for A M. in 12 hour mode. Data Bits D7 and D6 are DON'T CARE.

PROGRAMMERS MODEL - CLOCK REGISTERS

HEX ADDRESS	WRITE/READ REGISTERS DB7		DB0	NAME
20	TENS 0-5		UNITS 0-9	SECONDS (00-59)
21	TENS 0-5		UNITS 0-9	MINUTES (00-59)
22	12 HR. 24	X PM/AM TENS 0-2	UNITS 0-9	DB7, 1 = 12 HR, 0 = 24 HR DB5 = 1 PM, 0 = AM HOURS (01-12 OR 00-23)
23	X X X X		X UNITS 1-7	SUNDAY = 1 DAY OF WK (01-07)
24	TENS 0-3		UNITS 0-9	(DATE) DAY OF MONTH (01-28, 29, 30, 31)
25	TENS 0-1		UNITS 0-9	MONTH (01-12) - JAN = 1, DEC = 12
26	TENS 0-9		UNITS 0-9	YEARS (00-99)
31	7 6 5 4		3 2 1 0	CONTROL
32	7 6 5 4		3 2 1 0	INTERRUPT

WRITE ONLY REGISTERS

HEX ADDRESS					NAME
28	TENS 0-5			UNITS 0-9	ALARM SECONDS (00-59)
29	TENS 0-5			UNITS 0-9	ALARM MINUTES (00-59)
2A	X	X	PM/AM TENS 0-2	UNITS 0-9	ALARM HOURS (01-12 or 00-23) PLUS AM/PM IN 12 HR. MODE PM = 1, AM = 0

READ ONLY REGISTER

30	7	6	5	4	3	2	1	0	STATUS

NOTE: X = DON'T CARE WRITES
X = 0 WHEN READ

RAM DATA BYTE

BIT 7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

HEX ADDRESS 00-1F

92CM-38059

FUNCTIONAL DESCRIPTION

The SPI real-time clock consists of a clock/calendar and a 32 x 8 RAM. Communications is established via the SPI (Serial Peripheral Interface) bus. In addition to the clock/calendar data from seconds to years, and system flexibility provided by the 32-byte RAM, the clock features computer handshaking with an interrupt output and a separate squarewave clock output that can be one of 7 different frequencies. An alarm circuit is available that compares the alarm latches with the seconds, minutes and hours time counters and activates the interrupt output when they are equal. The clock is specifically designed to aid in power-down/up applications and offers several pins to aid the designer of battery back-up systems.

Mode Select

The voltage level that is present at the V_{SYS} input pin at the end of power-on-reset selects the device to be in the single supply or battery back-up mode.

Single-Supply Mode—If V_{SYS} is a logic high when power-on-reset is completed, CLK OUT, PSE and CPUR will be enabled and the device will be completely operational. CPUR will be placed low if the logic level at the V_{SYS} pin goes low. If the output signals CLK OUT, PSE and CPUR are disabled due to a power-down instruction, V_{SYS} brought to a logic low and then to a logic high will re-enable these outputs. An example of the single-supply mode is where only one supply is available and V_{DD}, V_{BATT} and V_{SYS} are tied together to the supply.

Battery Back-up Mode—If V_{SYS} is a logic low at the end of power-on-reset, CLK OUT, PSE and CPUR and the CE pin will be disabled (CLK OUT, PSE and CPUR low). This condition will be held until V_{SYS} rises to a threshold (about 0.7 volt) above V_{BATT}. The outputs CLK OUT, PSE and CPUR will then be enabled and the device will be operational. If V_{SYS} falls below a threshold above V_{BATT}, the outputs CLK OUT, PSE and CPUR will be disabled. An example of battery back-up operation occurs if V_{SYS} is tied to V_{DD} and V_{DD} is not connected to a supply when a battery is connected to the V_{BATT} pin. (See Pin Functions V_{BATT} for Battery Back-up Operation)

CLOCK/CALENDAR (See Figs. 1 and 2.)

The clock/calendar portion of this device consists of a long string of counters that is toggled by a 1-Hz input. The 1-Hz input is generated by a prescaler driven by an on-board oscillator that utilizes one of four possible external crystals or that can be driven by an external clock source. The 1-Hz trigger to the counters can also be supplied by a 50 or 60-Hz input source that is connected to the LINE input pin.

The time counters offer seconds, minutes and hours data in 12 or 24-hour format. An AM/PM indicator is available that once set, toggles every 12 hours. The calendar counters consist of day (day of week), date (day of month), month and years information. Data in the counters is in BCD format. The hours counter utilizes BCD for hour data plus bits for 12/24 hour and AM/PM. The 7 time counters are accessed serially at addresses 20H through 26H. (See Table I).

RAM

The real-time clock also has a static 32 x 8 RAM that is located at addresses 00-1FH. Transmitting the address/control word with bit 5 low selects RAM access. Bits 0 through 4 select the RAM location.

ALARM

The alarm is set by accessing the three alarm latches and loading the required data. The alarm latches consist of seconds, minutes and hours registers. When their outputs equal the values in the seconds, minutes and hours time counters, an interrupt is generated. The interrupt output will go low if the alarm bit in the Interrupt Control register is set high. The alarm interrupt bit in the Status register is set when the interrupt occurs.* To preclude a false interrupt when loading the time counters, the alarm interrupt bit should be set low in the Interrupt Control register. This procedure is not required when the alarm time is set.

WATCHDOG FUNCTION (See Fig. 6.)

When bit 7 in the Interrupt Control register is set high, the Clock's CE (chip enable) pin must be toggled at a regular interval without a serial data transfer. If the CE is not toggled, the clock will supply a CPU reset pulse and bit 6 in the Status Register will be set. Typical service and reset times are listed below.

	50 Hz		60 Hz		XTAL	
	Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
Service Time	—	10ms	—	8.3ms	—	7.8ms
Reset Time	20	40ms	16.7	33.3ms	15.6	31.3ms

CLOCK OUT

The value in the 3 least significant bits of the Clock Control register selects one of seven possible output frequencies. (See Clock Control Register). This squarewave signal is available at the CLK OUT pin. When Power-Down operation is initiated, the output is set low.

CONTROL REGISTERS AND STATUS REGISTERS

The operation of the Real-Time Clock is controlled by the Clock Control and Interrupt Control registers. Both registers are read-write registers. Another register, the Status register, is available to indicate the operating conditions. The Status register is a read-only register.

POWER CONTROL

Power control is composed of two operations, Power Sense and Power Down/Up. Two pins are involved in power sensing, the LINE input pin and the $\overline{\text{INT}}$ output pin. Two additional pins are utilized during power-down/up operation. They are the PSE (Power Supply Enable) output pin and V_{SYS} input pin.

POWER SENSING (See Fig. 3.)

When Power Sensing is enabled (Bit 5 = 1 in Interrupt Control Register), AC transitions are sensed at the LINE input pin. Threshold detectors determine when transitions cease. After a delay of 2.68 to 4.64 ms plus the external input circuit RC time constant, an interrupt is generated and a bit is set in the status register. This bit can then be sampled to see if system power has turned back on. See PIN FUNCTIONS, LINE PIN. The power-sense circuitry operates by sensing the level of the voltage presented at the line input pin. This voltage is centered around V_{DD} and as long as it is either plus or minus a threshold (about 1 volt) from V_{DD} a power-sense failure will not be indicated. With an ac signal present, remaining in this V_{DD} window longer than a minimum of 2.68 ms will activate the power-sense circuit. The larger the amplitude of the ac signal, the less time it

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*See PIN FUNCTIONS, $\overline{\text{INT}}$ PIN.

CDP68HC68T1

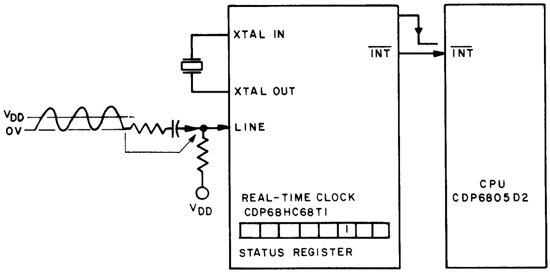

Fig. 3 - Power-sensing functional diagram.

spends in the V_{DD} window and the less likely a power failure will be detected. A 60-Hz, 10 V_{p-p} sinewave voltage is an applicable signal to present at the LINE input pin to set up the power-sense function.

POWER DOWN (See Fig. 4.)

Power down is a processor-directed operation. A bit is set in the Interrupt Control Register to initiate operation. 3 pins are affected. The PSE (Power Supply Enable) output, normally high, is placed low. The CLK OUT is placed low. The $\overline{\text{CPUR}}$ output, connected to the processors reset input is also placed low. In addition, the Serial Interface is disabled.

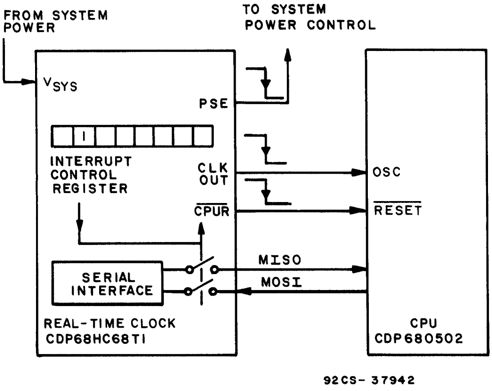

Fig. 4 - Power-down functional diagram.

POWER UP (See Figs. 5 and 6.)

Two conditions will terminate the Power-Down mode. The first condition (See Fig. 5) requires an interrupt. The interrupt can be generated by the alarm circuit, the programmable periodic interrupt signal, or the power-sense circuit.

The second condition that releases Power Down occurs when the level on the V_{SYS} pin rises about 1 volt above the level at the V_{BATT} input, after previously falling to the level of V_{BATT} (See Fig.6) in the Battery Back-up Mode or V_{SYS} falls to logic low and returns high in the Single Supply Mode.

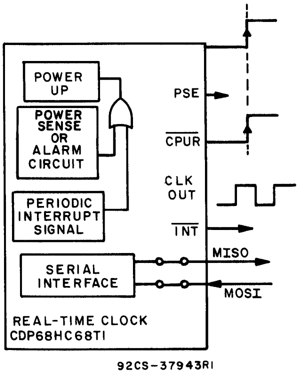

Fig. 5 - Power-up functional diagram (initiated by Interrupt Signal).

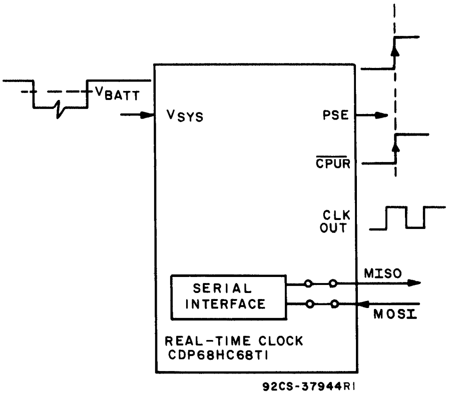

Fig. 6 - Power-up functional diagram (initiated by a rise in voltage on the "V_{SYS}" pin).

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PIN FUNCTIONS

CLK OUT—Clock output pin. One of 7 frequencies can be selected (or this output can be set low) by the levels of the three LSB's in the clock-control register. If a frequency is selected, it will toggle with a 50% duty cycle except 2 Hz in the 50-Hz timebase mode. (Ex. if 1 Hz is selected, the output will be high for 500 ms and low for the same period.) During power-down operation (bit 6 in Interrupt Control Register set to "1"), the clock-output pin will be set low.

$\overline{\text{CPUR}}$—CPU reset output pin. This pin functions as an N-channel only, open-drain output and requires an external pull-up resistor.

$\overline{\text{INT}}$—Interrupt output pin. This output is driven from a single NFET pull-down transistor and must be tied to an external pull-up resistor. The output is activated to a low level when:

1. Power-sense operation is selected (B5 = 1 in Interrupt Control Register) and a power failure occurs.
2. A previously set alarm time occurs. The alarm bit in the status register and interrupt-out signal are delayed 30.5 μs when 32-kHz operation is selected and 15.3 μs for 2-MHz and 7.6 μs for 4-MHz. (See important application note.)
3. A previously selected periodic interrupt signal activates.

The status register must be read to set the Interrupt output high after the selected periodic interval occurs. This is also true when conditions 1 and 2 activate the interrupt. If power down had been previously selected, the interrupt will also reset the power-down functions.

SCK, MOSI, MISO—See Serial Peripheral Interface (SPI) section in this data sheet.

CE—A positive chip-enable input. A low level at this input holds the serial interface logic in a reset state. This pin is also used for the watchdog function.

V_{SS}—The negative power-supply pin that is connected to ground.

PSE—Power-supply enable output pin. This pin is used to control power to the system. The pin is set high when:

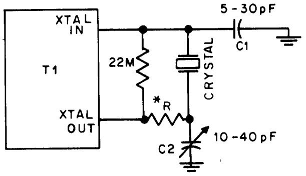
1. V_{SYS} rises above the V_{BATT} voltage after V_{SYS} was placed low by a system failure.
2. An interrupt occurs.
3. A power-on reset (if V_{SYS} is a logic high).

The PSE pin is set low by writing a high into bit 6 (power-down bit) in the Interrupt Control Register.

$\overline{\text{POR}}$—Power-on reset. A Schmitt-trigger input that generates a power-on internal reset signal using an external R-C network. Both control registers and frequency dividers for the oscillator and line input are reset. The status register is reset except for the first time up bit (B4), which is set. Single supply or battery back-up operation is selected at the end of $\overline{\text{POR}}$.

LINE—This input is used for two functions. The first function utilizes the input signal as the frequency source for the timekeeping counters. This function is selected by setting bit 6 in the Clock Control Register. The second function enables the line input to sense a power failure. Threshold detectors operating above and below V_{DD} sense an ac voltage loss. Bit 5 must be set to "1" in the Interrupt Control Register and crystal or external clock source operation is required. Bit 6 in the Clock Control Register must be low to select XTAL operation.

OSCILLATOR CIRCUIT—The CDP68HC68T1 has an on-board 150K resistor that is switched in series with its internal inverter when 32-kHz is selected via the clock-control register. Note: When first powered up the series resistor is not part of the oscillator circuit. (The CDP68HC68T1 sets up for a 4-MHz oscillator.)



ALL FREQUENCYS
RECOMMENDED OSCILLATOR CIRCUIT.
C1, C2 VALUES CRYSTAL DEPENDENT

*R USED FOR 32 KHz OPERATION ONLY
100 K - 300 K RANGE AS SPECIFIED
BY CRYSTAL MANUFACTURER.

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Fig. 7 - Oscillator circuit.

V_{SYS}—This input is connected to the system voltage. After the CPU initiates power down by setting bit 6 in the Interrupt Control Register to "1", the level on this pin will terminate power down if it rises about 0.7 volt above the level at the V_{BATT} input pin after previously falling below V_{BATT} + 0.7 volt. When power down is terminated, the PSE pin will return high and the Clock Output will be enabled. The $\overline{\text{CPUR}}$ output pin will also return high. The logic level present at this pin at the end of $\overline{\text{POR}}$ determines the CDP68HC68T1's operating mode.

V_{BATT}—The oscillator power source. The positive terminal of the battery should be connected to this pin. When the level on the V_{SYS} pin falls below V_{BATT} +0.7 volt, the V_{BATT} pin will be internally connected to the V_{DD} pin. When the voltage on V_{SYS} rises a threshold above (~ 0.7 V) the voltage on V_{BATT}, the connection from V_{BATT} to the V_{DD} pin is opened. When the "LINE" input is used as the frequency source, V_{BATT} may be tied to V_{DD} or V_{SS}. The "XTAL IN" pin must be at V_{SS} if V_{BATT} is at V_{SS}. If V_{BATT} is connected to V_{DD}, the "XTAL IN" pin can be tied to V_{SS} or V_{DD}.

XTAL IN, XTAL OUT—These pins are connected to a 32,768-Hz, 1.048576-MHz, 2.097152-MHz or 4.194304-MHz crystal. If an external clock is used, it should be connected to "XTAL IN" with "XTAL OUT" left open.

V_{DD}—The positive power-supply pin.

REGISTERS

CLOCK CONTROL REGISTER (Write/Read) - Address 31H

D7	D6	D5	D4	D3	D2	D1	D0
START $\overline{\text{STOP}}$	LINE $\overline{\text{XTAL}}$	XTAL SEL 1	XTAL SEL 0	50 Hz $\overline{\text{60 Hz}}$	CLK OUT 2	CLK OUT 1	CLK OUT 0

CLOCK CONTROL REGISTER

START-STOP—A high written into this bit will enable the counter stages of the clock circuitry. A low will hold all bits reset in the divider chain from 32 Hz to 1 Hz. A clock out selected by bits 0, 1 and 2 will not be affected by the stop function except the 1 and 2-Hz outputs.

LINE-XTAL—When this bit is set high, clock operation will use the 50 or 60-cycle input present at the LINE input pin. When the bit is low, the crystal input will generate the 1-Hz time update.

XTAL SELECT—One of 4 possible crystals is selected by value in these two bits.

0 = 4.194304 MHz
1 = 2.097152 MHz
2 = 1.048576 MHz
3 = 32,768 Hz

50-60 Hz—50 Hz is selected as the line input frequency when this bit is set high. A low will select 60 Hz. The power-sense bit in the Interrupt Control Register must be set low for line frequency operation.

CLOCK OUT—The three bits specify one of the 7 frequencies to be used as the squarewave clock output.

0 = XTAL
1 = XTAL/2
2 = XTAL/4
3 = XTAL/8
4 = Disable (low output)
5 = 1 Hz
6 = 2 Hz
7 = 50 or 60 Hz
XTAL Operation = 64 Hz

All bits are reset by a power-on reset. Therefore, the XTAL is selected as the clock output at this time.

INTERRUPT CONTROL REGISTER

WATCHDOG—When this bit is set high, the watchdog operation will be enabled. This function requires the CPU to toggle the CE pin periodically without a serial-transfer requirement. In the event this does not occur, a CPU reset will be issued. Status register must be read before re-enabling watchdog.

POWER DOWN—A high in this location will initiate a power down. A CPU reset will occur, the CLK OUT and PSE output pins will be set low and the serial interface will be disabled.

POWER SENSE—This bit is used to enable the line input pin to sense a power failure. It is set high for this function. When power sense is selected, the input to the 50/60-Hz prescaler is disconnected. Therefore, crystal operation is required when power sense is enabled. An interrupt is generated when a power failure is sensed and the power sense and Interrupt True bit in the Status Register are set. When power sense is activated, a "0" must be written to this location followed by a "1" to re-enable power sense.

ALARM—The output of the alarm comparator is enabled when this bit is set high. When a comparison occurs between the seconds, minutes and hours time and alarm counters, the interrupt output is activated. When loading the time counters, this bit should be set low to avoid a false interrupt. This is not required when loading the alarm counters. See PIN FUNCTIONS, $\overline{\text{INT}}$ for explanation of alarm delay.

PERIODIC SELECT—The value in these 4 bits will select the frequency of the periodic output. (See Table I).

INTERRUPT CONTROL REGISTER (Write/Read) - Address 32H

D7	D6	D5	D4	D3	D2	D1	D0
WATCHDOG	POWER DOWN	POWER SENSE	ALARM	PERIODIC SELECT			

All bits are reset by power-on reset.

Table I - Periodic Interrupt Output

D0-D3 VALUE	PERIODIC-INTERRUPT OUTPUT FREQUENCY	FREQUENCY TIMEBASE	
		XTAL	LINE
0	Disable		
1	2048 Hz	X	
2	1024 Hz	X	
3	512 Hz	X	
4	256 Hz	X	
5	128 Hz	X	
6	64 Hz	X	
	50 or 60 Hz		X
7	32 Hz	X	
8	16 Hz	X	
9	8 Hz	X	
10	4 Hz	X	
11	2 Hz	X	X
12	1 Hz	X	X
13	Minute	X	X
14	Hour	X	X
15	Day	X	X

STATUS REGISTER (Read Only) - Address 30H

D7	D6	D5	D4	D3	D2	D1	D0
0	WATCHDOG	TEST MODE	FIRST TIME UP	INTERRUPT TRUE	POWER SENSE INTERRUPT	ALARM INTERRUPT	CLOCK INTERRUPT

WATCHDOG - If this bit is set high, the watchdog circuit has detected a CPU failure.

TEST MODE - When this bit is set high, the device is in the TEST MODE.

FIRST-TIME UP - Power-on reset sets this bit high. This signifies that data in the RAM and Clock is not valid and should be initialized.

INTERRUPT TRUE - A high in this bit signifies that one of the three interrupts (Power Sense, Alarm, and Clock) is valid.

POWER-SENSE INTERRUPT - This bit set high signifies that the power-sense circuit has generated an interrupt.

ALARM INTERRUPT - When the seconds, minutes and hours time and alarm counter are equal, this bit will be set high. Status Register must be read before Loading Interrupt Control Register for valid alarm indication after alarm activates.

CLOCK INTERRUPT - A periodic interrupt will set this bit high.

All bits are reset by a power-on reset except the "FIRST-TIME UP" which is set. All bits except the power-sense bit are reset after a read of this register.

SERIAL PERIPHERAL INTERFACE (SPI)

PIN SIGNAL DESCRIPTION

SCK (Serial Clock Input)* - This input causes serial data to be latched from the MOSI input and shifted out on the MISO output.

MOSI (Master Out/Slave In)* - Data bytes are shifted in at this pin, most significant bit (MSB) first.

MISO (Master In/Slave Out) - Data bytes are shifted out at this pin, most signficant bit (MSB) first.

CE (Chip Enable)** - A positive chip-enable input. A low level at this input holds the serial interface logic in a reset state, and disables the output driver at the MISO pin.

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* These inputs will retain their previous state if the line driving them goes into a High-Z state.

** The CE input has as internal pull-down device—if the input is in a low state before going to a High Z, the input can be left in a High Z.

TRUTH TABLE

MODE	SIGNAL			
	CE	SCK	MOSI	MISO
DISABLED RESET	L	INPUT DISABLED	INPUT DISABLED	HIGH Z

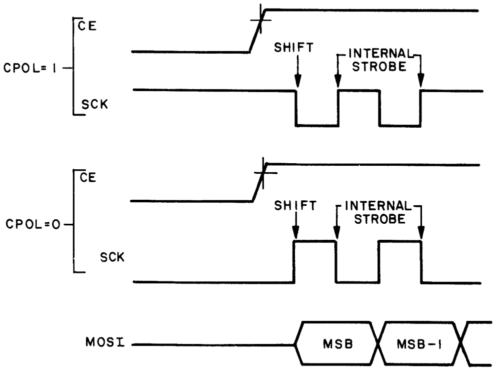
WRITE	H	CPOL = 1 ↑
		CPOL = 0 ↓
			DATA BIT
			LATCH
				HIGH Z

READ	H	CPOL = 1 ↓
		CPOL = 0 ↑
			X	NEXT DATA
				BIT SHIFTED
				OUT Δ

Δ MISO remains at a High Z until 8 bits of data are ready to be shifted out during a READ. It remains at a High Z during the entire WRITE cycle.

FUNCTIONAL DESCRIPTION

The Serial Peripheral Interface (SPI) utilized by the CDP68HC68T1 is a serial synchronous bus for address and data transfers. The clock, which is generated by the microcomputer, is active only during address and data transfers In systems using the CDP68HC05C4 or CDP68HC05D2, the inactive clock polarity is determined by the CPOL bit in the microcomputer's control register. A unique feature of the CDP68HC68T1 is that it automatically determines the level of the inactive clock by sampling SCK when CE becomes active (see Fig. 8). Input data (MOSI) is latched internally on the Internal Strobe edge and output data (MISO) is shifted out on the Shift edge, as defined by Fig. 8. There is one clock for each data bit transferred (address as well as data bits are transferred in groups of 8).



NOTE: "CPOL" IS A BIT THAT IS SET IN THE MICROCOMPUTER'S CONTROL REGISTER

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Fig. 8 - Serial RAM clock (SCK) as a function of MCU clock polarity (CPOL).

ADDRESS AND DATA FORMAT

There are three types of serial transfer.

1. Address Control - Fig. 9
2. READ or WRITE Data - Fig. 10
3. Watchdog Reset (actually a non-transfer) - Fig. 11

The Address/Control and Data bytes are shifted MSB first, into the serial data input (MOSI) and out of the serial data output (MISO).

Any transfer of data requires an Address/Control byte to specify a Write or Read operation and to select a Clock or RAM location, followed by one or more bytes of data.

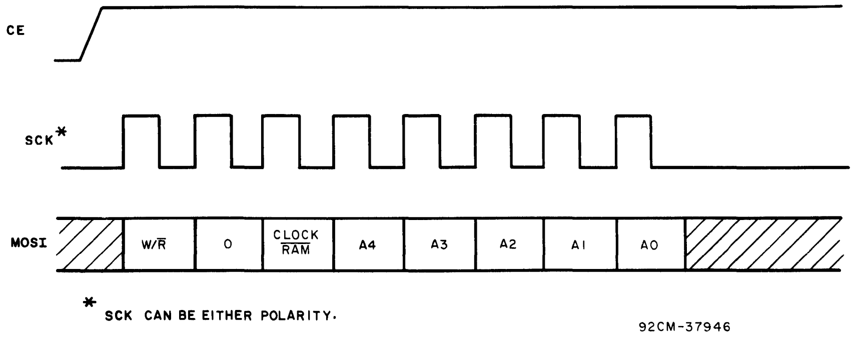
Data is transferred out of MISO for a Read and into MOSI for a Write operation.

ADDRESS/CONTROL BYTE - Fig. 9

It is always the first byte received after CE goes true. To transmit a new address, CE must first go false and then true again. Bit 5 is used to select between Clock and RAM locations.

BIT→7	6	5	4	3	2	1	0
$W/\overline{R}$	**0**	**CLK $\overline{\text{RAM}}$**	**A4**	**A3**	**A2**	**A1**	**A0**

0-4	**A0-A4**	Selects 5-Bit HEX Address of RAM or specifies Clock Register.
5	**CLOCK/$\overline{\text{RAM}}$**	Most Significant Address Bit. If equal to "1", A0 through A4 selects a Clock Register. If equal to "0", A0 through A4 selects one of 32 RAM locations.
6	**0**	Must be set to "0" when not in Test Mode
7	**W/R**	W/R = "1" initiates one or more WRITE cycles. W/R = "0", initiates one or more READ cycles.



* SCK CAN BE EITHER POLARITY.

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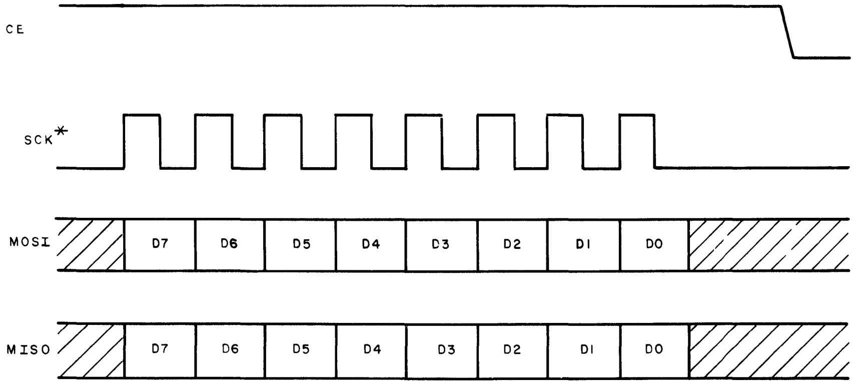
Fig. 9 - Address/Control byte-transfer waveforms.

READ/WRITE DATA - (See Fig. 10)

Read/Write data follows the Address/Control byte.

BIT 7	6	5	4	3	2	1	0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**



* SCK CAN BE EITHER POLARITY

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Fig. 10 - Read/Write data-transfer waveforms.

CDP68HC68T1

WATCHDOG RESET - (See Fig. 11)

When watchdog operation is selected, CE must be toggled periodically or a CPU reset will be outputted.

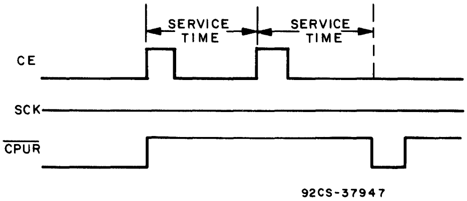


Fig. 11 - Watchdog operation waveforms.

ADDRESS AND DATA

Data transfers can occur one byte at a time (Fig. 12) or in a multibyte burst mode (Fig. 13). After the Real-Time Clock is enabled, an Address/Control word is sent to select the CLOCK or RAM and select the type of operation (i.e., Read or Write). For a single-byte Read or Write, one byte is transferred to or from the clock register or RAM location specified in the Address/Control byte and the Real-Time Clock is then disabled. Write cycle causes the latched clock register or RAM address to automatically increment. Incrementing continues after each transfer until the device is disabled. After incrementing to 1FH the address will "wrap" to 00H and continue. Therefore, when the RAM is selected the address will "wrap" to 00H and when the clock is selected the address will "wrap" 20H.

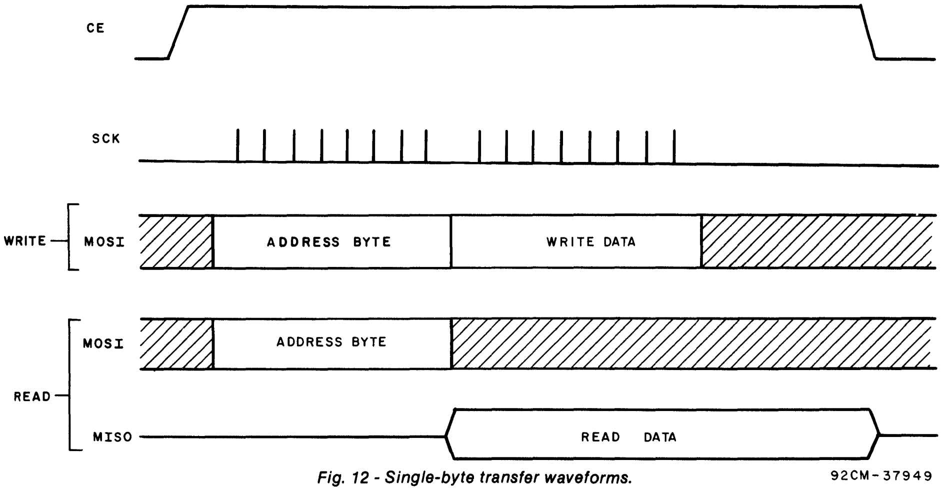


Fig. 12 - Single-byte transfer waveforms.

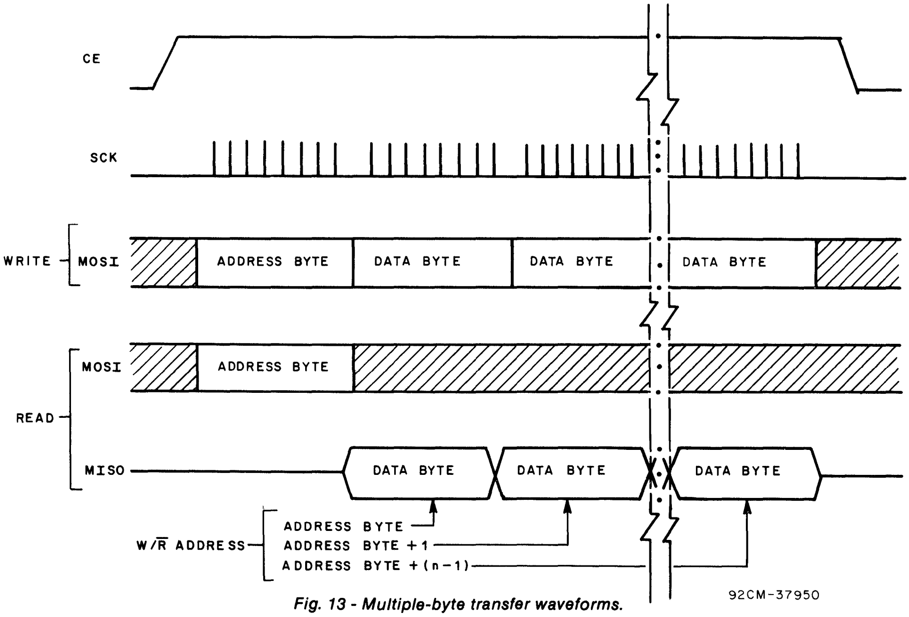


Fig. 13 - Multiple-byte transfer waveforms.

DYNAMIC CHARACTERISTICS

DYNAMIC ELECTRICAL CHARACTERISTICS-BUS TIMING $V_{DD} \pm 10\%$, $V_{SS} = 0$ V dc, $T_A = -40°$C to $+85°$C, $C_L = 200$ pF, see Figs. 14 and 15

IDENT. NO.	CHARACTERISTIC		LIMITS (ALL TYPES)				UNITS
			V_{DD} = 3.3 V		V_{DD} = 5 V		
			Min.	Max.	Min.	Max.	
①	Chip Enable Set-Up Time	t_{EVCV}	200	—	100	—	ns
②	Chip Enable After Clock Hold Time	t_{CVEX}	250	—	125	—	
③	Clock Width High	t_{WH}	400	—	200	—	
④	Clock Width Low	t_{WL}	400	—	200	—	
⑤	Data In to Clock Set-Up Time	t_{DVCV}	200	—	100	—	
⑦	Clock to Data Propagation Delay	t_{CVDV}	—	200	—	100	
⑧	Chip Disable to Output High Z	t_{EXQZ}	—	200	—	100	
⑪	Output Rise Time	t_r	—	200	—	100	
⑫	Output Fall Time	t_f	—	200	—	100	
Ⓐ	Data In After Clock Hold Time	t_{CVDX}	200	—	100	—	
Ⓑ	Clock to Data Out Active	t_{CVQX}	—	200	—	100	
Ⓒ	Clock Recovery Time	t_{REC}	200	—	200	—	

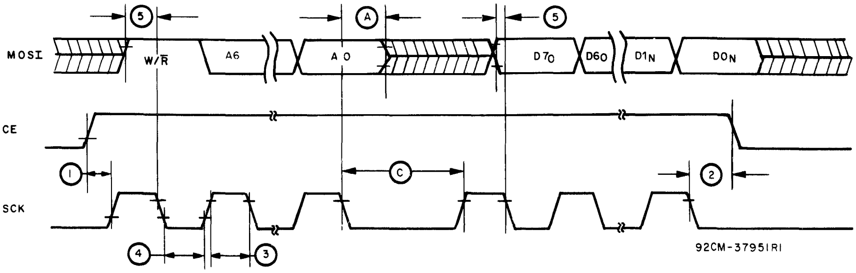


Fig. 14 - WRITE-cycle timing waveforms.

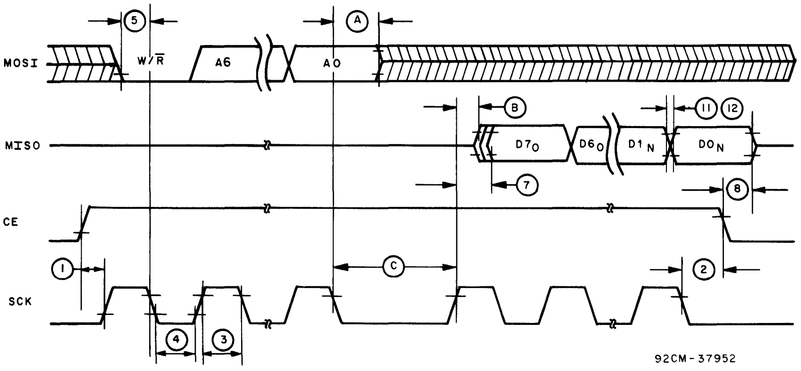
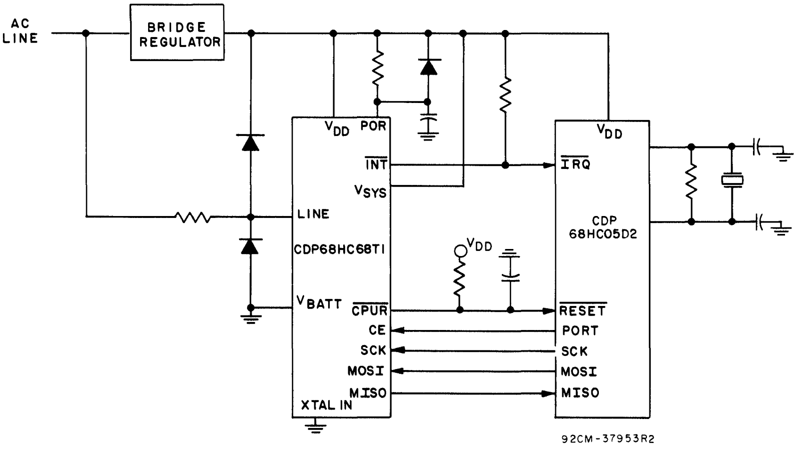


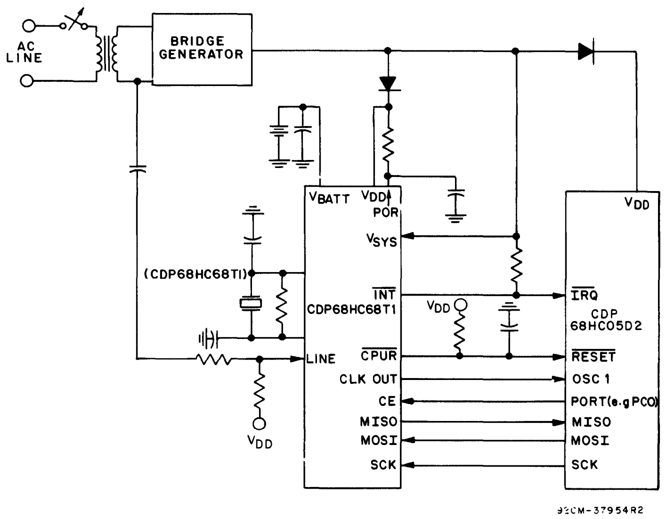
Fig. 15 - READ-cycle timing waveforms.

SYSTEM DIAGRAMS



Example of a system in which power is always on. Clock circuit driven by line input frequency.

Fig. 16 - Power-on always system diagram.



Example of a system in which the power is controlled by an external source. The LINE input pin can sense when the switch opens by use of the POWER-SENSE INTERRUPT. The CDP68HC68T1 crystal drives the clock input to the CPU using the CLK OUT pin. On power down when $V_{SYS} < V_{BATT} + 0.7$ V. V_{BATT} will power the CDP68HC68T1. A threshold detect activates a p-channel switch, connecting V_{BATT} to V_{DD}. V_{BATT} always supplies power to the oscillator, keeping voltage frequency variation to a minimum.

Fig. 17 - Externally-controlled power system diagram.

A Procedure for Power-Down Operation might consist of the following:

1. Set power-sense operation by writing bit 5 high in the Interrupt Control Register.
2. When an interrupt occurs, the CPU reads the status register to determine the interrupt source.
3. Sensing a power failure, the CPU does the necessary housekeeping to prepare for shutdown.
4. The CPU reads the status register again after several milliseconds to determine validity of power failure.
5. The CPU sets power-down bit 6 and disables all interrupts in the Interrupt Control Register when power down is verified. This causes the CPU reset and clock out to be held low and disconnects the serial interface.
6. When power returns and V_{SYS} rises above V_{BATT}, power down is terminated. The CPU reset is released and serial communication is established.

CDP68HC68T1

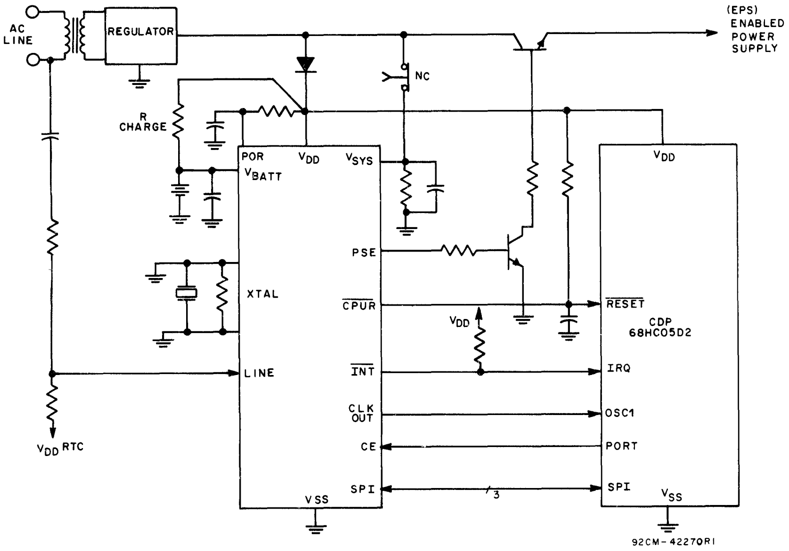
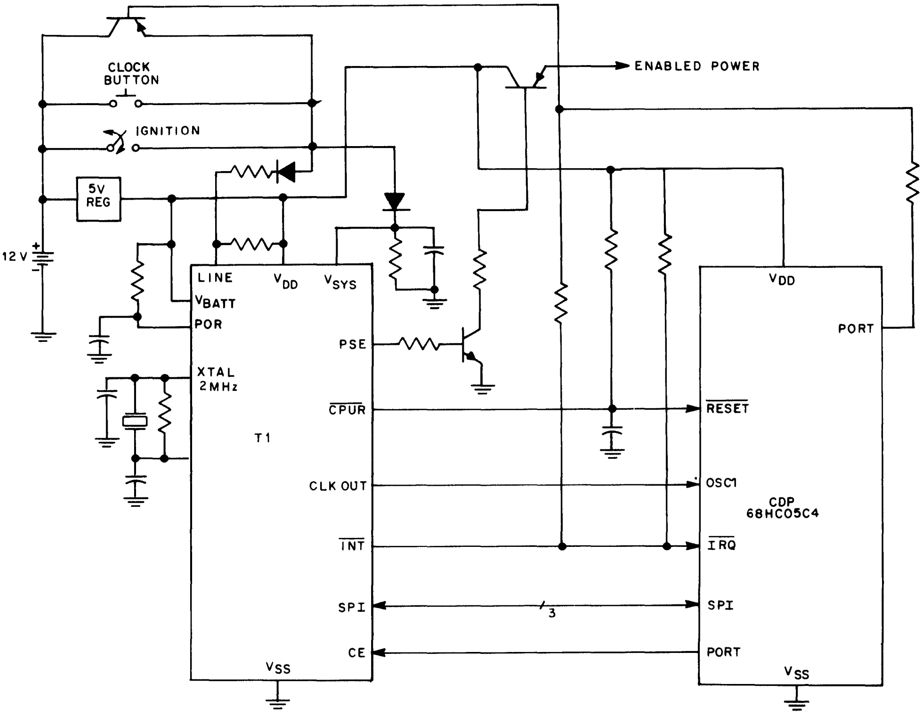


Fig. 18 - Example of a system with a battery back-up.



92CM-42271

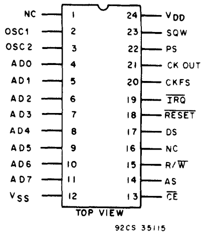
Example of an automotive system. The V_{SYS} and LINE inputs can be used to sense the ignition turning on and off. An external switch is included to activate the system without turning on the ignition. Also, the CMOS CPU is not powered down with the system V_{DD}, but is held in a low power reset mode during power down. When restoring power the CDP68HC68T1 will enable the CLK OUT pin and set the PSE and CPUR high.

Fig. 19 - Automotive system diagram.

IMPORTANT APPLICATION NOTE:

Those units with a code of 6 PG have delayed alarm interrupts of 8.3 ms regardless of CDP68HC68T1's operating frequency. (See PIN FUNCTIONS, $\overline{\text{INT}}$.) In addition, reading the status register before delayed alarm activates will disable alarm signal.

CDP6818



TERMINAL ASSIGNMENT

CMOS Real-Time Clock with RAM

Features:

- *Low-Power, High-Speed, High-Density CMOS*
- *Internal Time Base and Oscillator*
- *Counts Seconds, Minutes, and Hours of the Day*
- *Counts Days of the Week, Date, Month, and Year*
- *3 V to 6 V Operation*
- *Time Base Input Options: 4.194304 MHz, 1.048576 MHz, or 32.768 kHz*
- *Time Base Oscillator for Parallel Resonant Crystals*
- *40 to 200 µW Typical Operating Power at Low Frequency Time Base*
- *4.0 to 20 mW Typical Operating Power at High Frequency Time Base*
- *Binary or BCD Representation of Time, Calendar, and Alarm*
- *12- or 24-Hour Clock with AM and PM in 12-Hour Mode*
- *Daylight Savings Time Option*
- *Automatic End of Month Recognition*
- *Automatic Leap Year Compensation*
- *Microprocessor Bus Compatible*
- *MOTEL Circuit for Bus Universality*
- *Multiplexed Bus for Pin Efficiency*
- *Interfaced with Software as 64 RAM Locations*
- *14 Bytes of Clock and Control Registers*
- *50 Bytes of General Purpose RAM*
- *Status Bit Indicates Data Integrity*
- *Bus Compatible Interrupt Signals (IRQ)*
- *Three Interrupts are Separately Software Maskable and Testable*
  - *Time-of-Day Alarm, Once-per-Second to Once-per-Day*
  - *Periodic Rates from 30.5 µs to 500 ms*
  - *End-of-Clock Update Cycle*
- *Programmable Square-Wave Output Signal*
- *Clock Output May Be Used as Microprocessor Clock Input*
  - *At Time Base Frequency +1 or +4*
- *24-Pin Dual-In-Line Package*

The CDP6818 Real-Time Clock plus RAM is a peripheral device which includes the unique MOTEL concept for use with many 8-bit microprocessors, microcomputers, and larger computers. This device combines three unique features: a complete time-of-day clock with alarm and one hundred year calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of low-power static RAM. The CDP6818 uses high-speed CMOS technology to interface with 1 MHz processor buses, while consuming very little power.

The Real-Time Clock plus RAM has two distinct uses. First, it is designed as a battery powered CMOS device (in an otherwise NMOS/TTL system) including all the common battery backed-up functions such as RAM, time, and calendar. Secondly, the CDP6818 may be used with a CMOS microprocessor to relieve the software of the timekeeping workload and to extend the available RAM of an MPU such as the CDP6805E2.

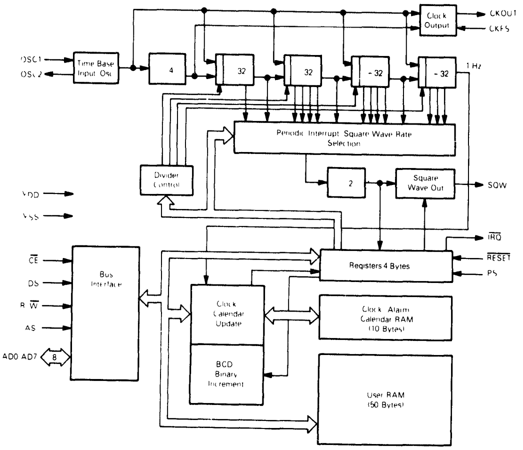


Fig. 1 - Block diagram.

File Number **1375**

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0 3 to +8	V
All Input Voltages	V_{in}	V_{SS}−0 5 to V_{DD}+0 5	V
Current Drain per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

DC ELECTRICAL CHARACTERISTICS (V_{DD}=5 Vdc ±10%, V_{SS}=0 Vdc, T_A=0° to 70°C unless otherwise noted)

Characteristics		Symbol	Min	Max	Unit
Frequency of Operation		f_{osc}	32.768	4194.304	kHz
Output Voltage		V_{OL}	−	0.1	V
I_{Load}< 10 μA		V_{OH}	V_{DD}−0.1	−	
I_{DD} − Bus Idle (External clock) CKOUT = f_{osc}, C_L = 15 pF; SQW Disabled, $\overline{CE}$ = V_{DD}−0 2, C_L (OSC2) = 10 pF					
f_{osc}=4 194304 MHz		I_{DD1}	−	3	mA
f_{osc}=1 048516 MHz		I_{DD2}	−	0.8	mA
f_{osc}=32 768 kHz		I_{DD3}	−	50	μA
I_{DD} − Quiescent f_{osc}=DC; OSC1=DC, All Other Inputs=V_{DD}−0 2 V, No Clock		I_{DD4}	−	50	μA
Output High Voltage AD0-AD7 CKOUT (I_{Load}= −1.6 mA, SQW, I_{Load}= −1.0 mA)		V_{OH}	4 1	−	V
Output Low Voltage AD0-AD7 CKOUT (I_{Load}=1 6 mA, $\overline{IRQ}$, and SQW, I_{Load}=1 0 mA)		V_{OL}	−	0.4	V
Input High Voltage	CKFS, AD0-AD7, DS, AS, R/$\overline{W}$, $\overline{CE}$, PS	V_{IH}	V_{DD}−2	V_{DD}	V
	$\overline{RESET}$		V_{DD}−0.8	V_{DD}	
	OSC1		V_{DD}−1	V_{DD}	
Input Low Voltage	AD0-AD7, DS, AS, R/$\overline{W}$, $\overline{CE}$	V_{IL}	V_{SS}	0.8	V
	CKFS, PS, $\overline{RESET}$		V_{SS}	0.8	
	OSC1		V_{SS}	0.8	
Input Current	All Inputs	I_{in}	−	±1	μA
Three-State Leakage	AD0-AD7	I_{TSL}	−	±10	μA

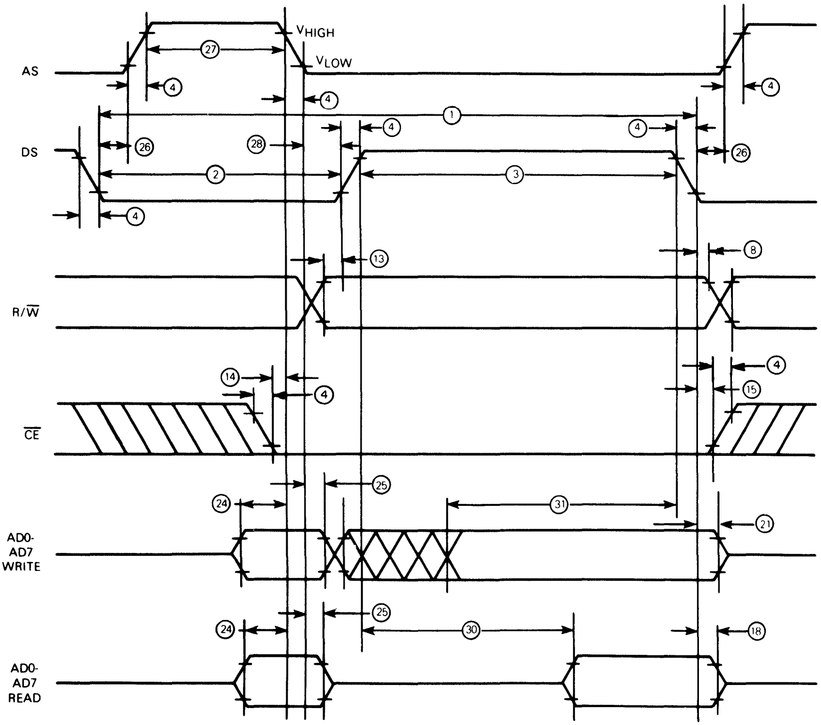
DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3 Vdc, V_{SS} = 0 Voc, T_A = 0° to 70°C unless otherwise noted)

Characteristics		Symbol	Min	Max	Unit
Frequency of Operation		f_{osc}	32.768	32.768	kHz
Output Voltage		V_{OL}	—	0.1	V
I_{LOAD} < 10 μ A		V_{OH}	V_{DD}-0.1	—	
I_{DD}— Bus Idle CKOUT = f_{osc}, C_L = 15 pF, SQW Disabled, $\overline{CE}$ = V_{DD}-0.2, C_L (OSC2) = 10 pF f_{osc} = 32.768 kHz		I_{DD3}	—	50	μA
I_{DD}— Quiscent f_{osc} = DS; OSC1=DC, All Other Inputs = V_{DD}-0 2 V, No Clock		I_{DD4}	—	50	μA
Output High Voltage (L_{Load} = -0.25 mA, All Outputs)		V_{OH}	2.7	—	V
Output Low Voltage (I_{Load} = 0 25 mA, All Outputs)		V_{OL}	—	0.3	V
Input High Voltage	AD0-AD7, DS, AS, R/$\overline{W}$, $\overline{CE}$,	V_{IH}	2.1	V_{DD}	V
	$\overline{RESET}$, CKFS, PS, OSC1		2.5	V_{DD}	
Input Low Voltage (All Inputs)		V_{IL}	V_{SS}	0.5	V
Input Current	All Inputs	I_{in}	—	±1	μA
Three-State Leakage	$\overline{IRQ}$, AD0-AD7	I_{TSL}	—	±10	μA

BUS TIMING

Ident. Number	Characteristics	Symbol	V_{DD} = 3.0 V 50 pF Load		V_{DD} = 5.0 V ± 10% 2 TTL and 130 pF Load		Unit
			Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	5000	—	953	dc	ns
2	Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High	PW_{EL}	1000	—	300	—	ns
3	Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low	PW_{EH}	1500	—	325	—	ns
4	Input Rise and Fall Time	t_r, t_f	—	100	—	30	ns
8	$R/\overline{W}$ Hold Time	t_{RWH}	10	—	10	—	ns
13	$R/\overline{W}$ Setup Time Before DS/E	t_{RWS}	200	—	80	—	ns
14	Chip Enable Setup Time Before AS/ALE Fall	t_{CS}	200	★	55	★	ns
15	Chip Enable Hold Time	t_{CH}	10	—	0	—	ns
18	Read Data Hold Time	t_{DHR}	10	1000	10	100	ns
21	Write Data Hold Time	t_{DHW}	100	—	0	—	ns
24	Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	200	—	50	—	ns
25	Muxed Address Hold Time	t_{AHL}	100	—	20	—	ns
26	Delay Time DS/E to AS/ALE Rise	t_{ASD}	500	—	50	—	ns
27	Pulse Width, AS/ALE High	PW_{ASH}	600	—	135	—	ns
28	Delay Time, AS/ALE to DS/E Rise	t_{ASED}	500	—	60	—	ns
30	Peripheral Output Data Delay Time from DS/E or $\overline{RD}$	t_{DDR}	1300	—	20	240	ns
31	Peripheral Data Setup Time	t_{DSW}	1500	—	200	—	ns

NOTE: Designations E, ALE, $\overline{RD}$, and $\overline{WR}$ refer to signals from alternative microprocessor signals
★See Important Application Notice (refer to Fig 23)



NOTE $V_{HIGH}=V_{DD}-2.0$ V, $V_{LOW}=0.8$ V, for $V_{DD}=5.0$ V ± 10%

Fig. 2 — CDP6818 bus timing waveforms

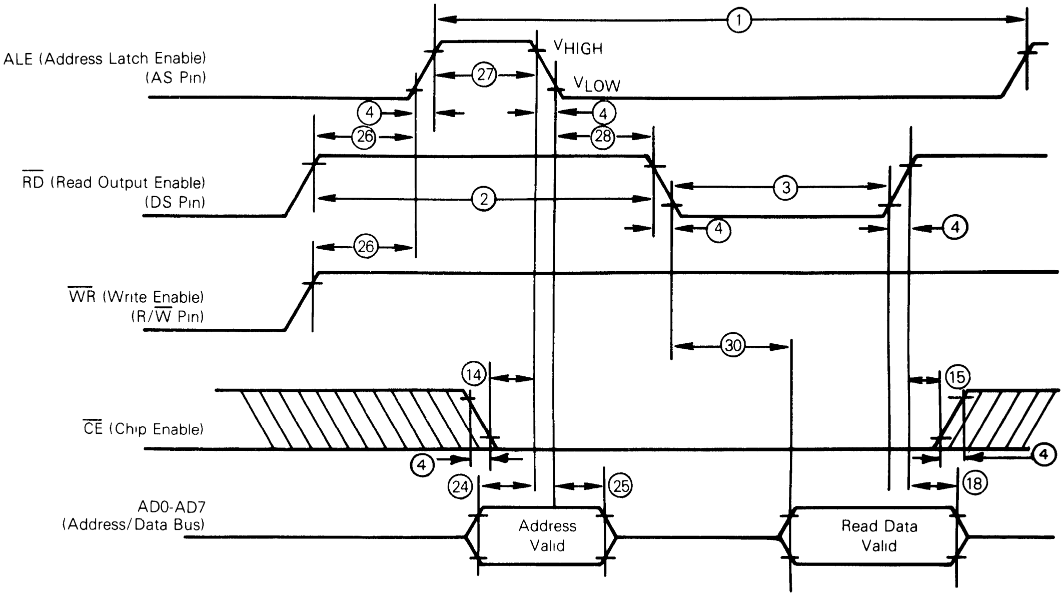
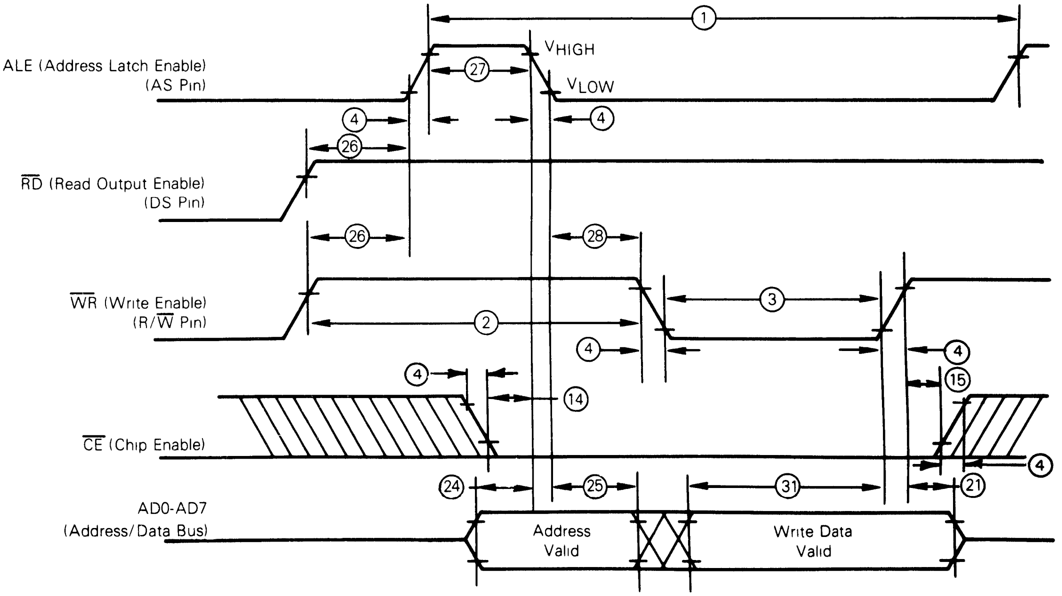


Fig 3 — Bus-read timing competitor multiplexed bus.



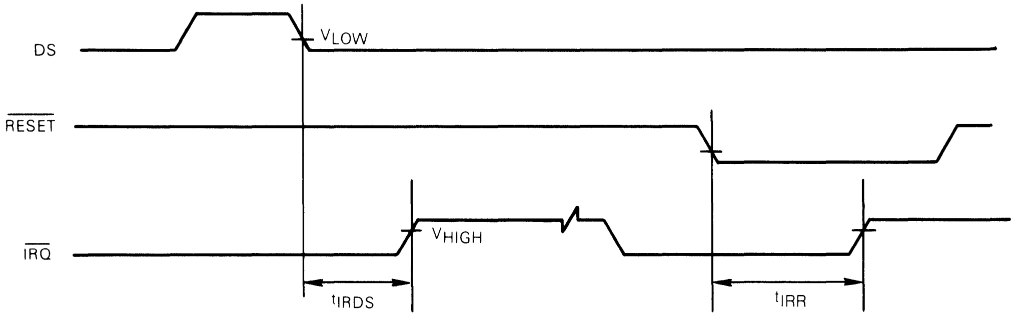
NOTE $V_{HIGH} = V_{DD} - 2\ 0$ V, $V_{LOW} = 0\ 8$ V, for $V_{DD} = 5\ 0$ V ±10%

Fig. 4 — Bus-write timing competitor multiplexed bus.

CDP6818

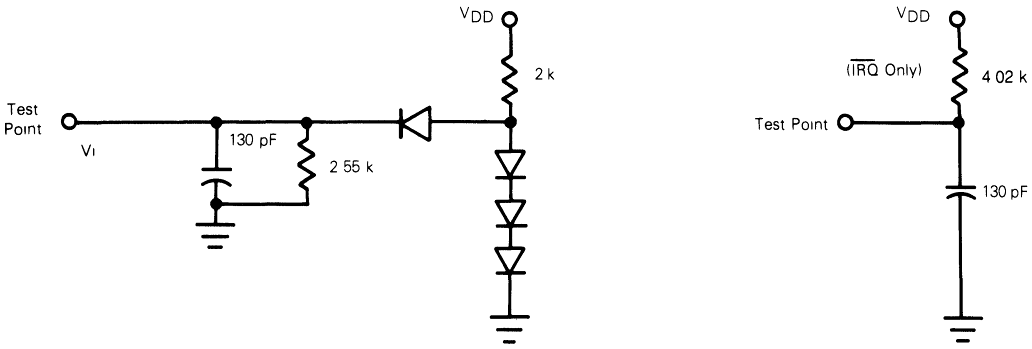
TABLE 1 — SWITCHING CHARACTERISTICS (V_{DD}=5 Vdc ±10%, V_{SS}=0 Vdc, T_A=0° to 70°C)

Description	Symbol	Min	Max	Unit
Oscillator Startup	t_{RC}	—	100	ms
Reset Pulse Width	t_{RWL}	5	—	µs
Reset Delay Time	t_{RLH}	5	—	µs
Power Sense Pulse Width	t_{PWL}	5	—	µs
Power Sense Delay Time	t_{PLH}	5	—	µs
$\overline{IRQ}$ Release from DS	t_{IRDS}	—	2	µs
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}	—	2	µs
VRT Bit Delay	t_{VRTD}	—	2	µs



NOTE V_{HIGH} = V_{DD} − 2.0 V, V_{LOW} = 0.8 V, for V_{DD} = 5.0 V ±10%

Fig. 5 — $\overline{IRQ}$ release delay timing waveforms.



All Outputs Except OSC2 (See Figure 10)

Fig. 6 — TTL equivalent test load.

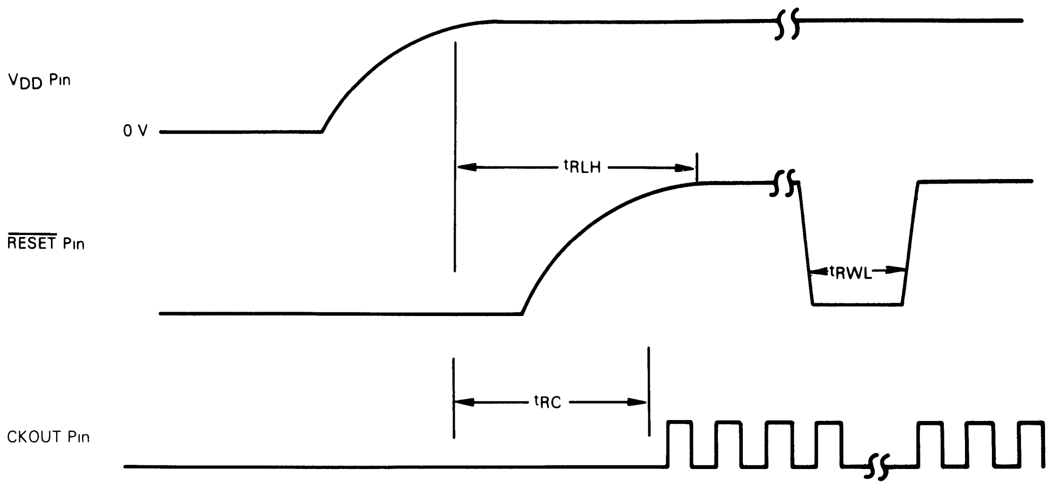
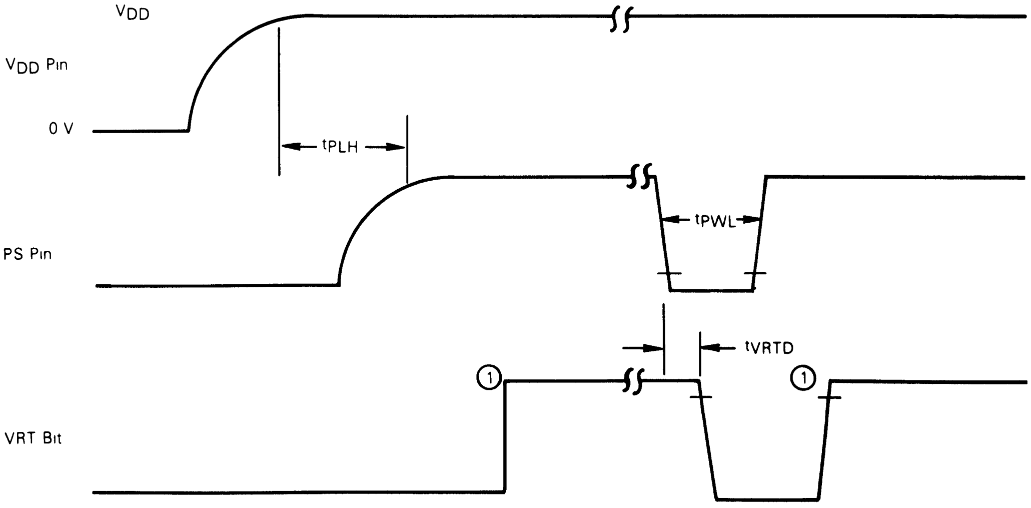


Fig. 7 — Power-up timing waveforms.



① The VRT bit is set to a "1" by reading Control Register #D The VRT Bit can only be cleared by pulling the PS Pin low (see REGISTER D ($OD))

Fig. 8 — Conditions that clear VRT bit timing waveforms.

MOTEL

The MOTEL circuit is a new concept that permits the CDP6818 to be directly interfaced with many types of microprocessors No external logic is needed to adapt to the differences in bus control signals from common multiplexed bus microprocessors

Practically all microprocessors interface with one of two synchronous bus structures

The MOTEL circuit is built into peripheral and memory ICs to permit direct connection to either type of bus An industry standard bus structure is now available The MOTEL concept is shown logically in Figure 9.

MOTEL selects one of two interpretations of two pins In the 6805 case, DS and R/$\overline{W}$ are gated together to produce the internal read enable The internal write enable is a similar gating of the inverse of R/$\overline{W}$ With competitor buses, the inversion of $\overline{RD}$ and $\overline{WR}$ create functionally identical internal read and write enable signals

The CDP6818 automatically selects the processor type by using AS/ALE to latch the state of the DS/$\overline{RD}$ pin Since DS is always low and $\overline{RD}$ is always high during AS and ALE, the latch automatically indicates which processor type is connected.

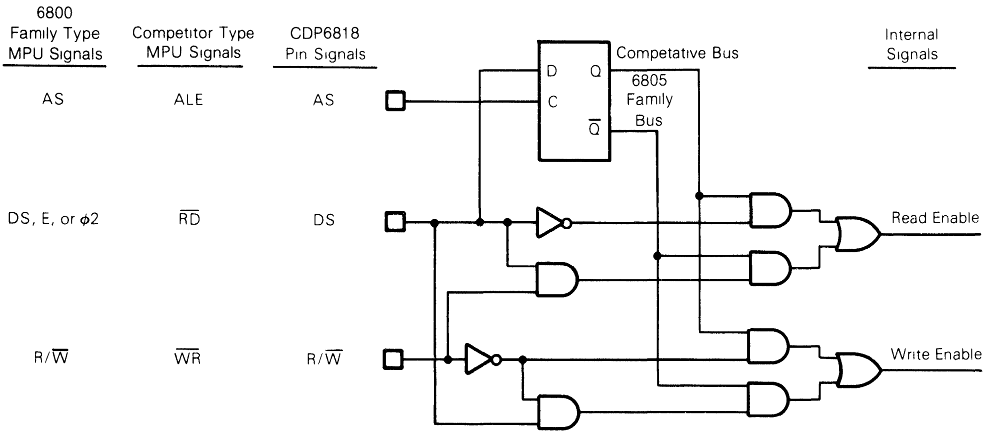


Fig. 9 — Functional diagram of MOTEL circuit

SIGNAL DESCRIPTIONS

The block diagram in Figure 1, shows the pin connection with the major internal functions of the CDP6818 Real-Time Clock plus RAM The following paragraphs describe the function of each pin

V_{DD}, V_{SS}

DC power is provided to the part on these two pins, V_{DD} being the most positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

OSC1, OSC2 – TIME BASE, INPUTS

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304 MHz, 1.048576 MHz, or 32.768 kHz may be connected to OSC1 as shown in Figure 10 The time-base frequency to be used is chosen in Register A.

The on-chip oscillator is designed for a parallel resonant AT cut crystal at 4 194304 MHz or 1.048576 MHz frequencies The crystal connections are shown in Figure 11 and the crystal characteristics in Figure 12

CKOUT – CLOCK OUT, OUTPUT

The CKOUT pin is an output at the time-base frequency divided by 1 or 4 A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 2

CKFS – CLOCK OUT FREQUENCY SELECT, INPUT

The CKOUT pin is an output at the time-base frequency divided by 1 or 4 CKFS tied to V_{DD} causes CKOUT to be the same frequency as the time base at the OSC1 pin When CKFS is at V_{SS}, CKOUT is the OSC1 time-base frequency divided by four. Table 2 summarizes the effect of CKFS

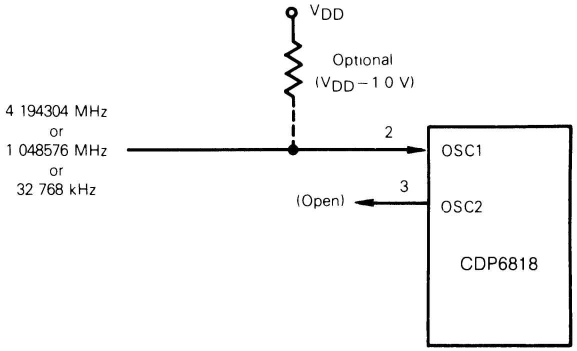
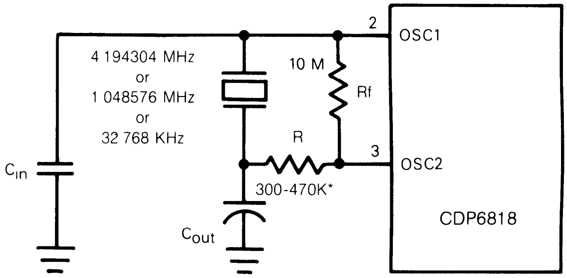


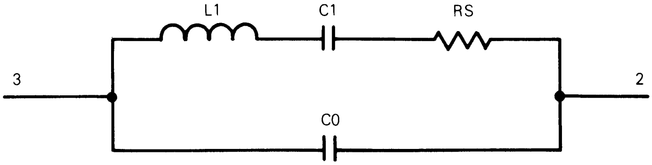
Fig 10 — External Time-base connection

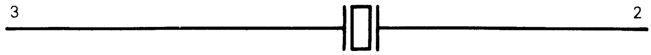


*32 768 KHz — Consult manufacturers specification

Fig 11 — Crystal oscillator connection

Crystal Equivalent Circuit





f_{osc}	**4.194304 MHz.**	**1.048576 MHz**	**32.768 KHz**
Rs max	75 Ω	700 Ω	50 K
C0 max	7 pF	5 pF	1.7 pF
C1	0 012 pF	0.008 pF	0 003 pF
C_{in}/C_{out}	15-30 pF	15-40 pF	10-22 pF
Q	50 k	35 k	30 k
R	—	—	300-470 K
R_f	10M	10M	22M

Fig. 12 — Crystal parameters

TABLE 2 — CLOCK OUTPUT FREQUENCIES

Time Base (OSC1) Frequency	Clock Frequency Select Pin (CKFS)	Clock Frequency Output Pin (CKOUT)
4 194304 MHz	High	4 194304 MHz
4 194304 MHz	Low	1 048576 MHz
1 048576 MHz	High	1 048576 MHz
1 048576 MHz	Low	262 144 kHz
32 768 kHz	High	32 768 kHz
32 768 kHz	Low	8 192 kHz

SQW — SQUARE WAVE, OUTPUT

The SQW pin can output a signal one of 15 of the 22 internal-divider stages The frequency and output enable of the SQW may be altered by programming Register A, as shown in Table 5 The SQW signal may be turned on and off using a bit in Register B

AD0-AD7 — MULTIPLEXED BIDIRECTIONAL ADDRESS/DATA BUS

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data Address-then-data multiplexing does not slow the access time of the CDP6818 since the bus reversal from address to data is occurring during the internal RAM access time

The address must be valid just prior to the fall of AS/ALE at which time the CDP6818 latches the address from AD0 to AD5 Valid write data must be presented and held stable during the latter portion of the DS or $\overline{WR}$ pulses In a read cycle, the CDP6818 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses, then ceases driving the bus (returns the output drivers to three-state) when DS falls in this case of MOTEL or $\overline{RD}$ rises in the other case

AS — MULTIPLEXED ADDRESS STROBE, INPUT

A positive going multiplexed address strobe pulse serves to demultiplex the bus The falling edge of AS or ALE causes the address to be latched within the CDP6818 The automatic MOTEL circuitry in the CDP6818 also latches the state of the DS pin with the falling edge of AS or ALE

DS — DATA STROBE OR READ, INPUT

The DS pin has two interpretations via the MOTEL circuit When emanating from a 6800 type processor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and $\phi 2$ ($\phi 2$ clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus In write cycles, the trailing edge of DS causes the Real-Time Clock plus RAM to latch the written data

The second MOTEL interpretation of DS is that of $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ emanating from a competitor type processor In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data This interpretation of DS is also the same as an output-enable signal on a typical memory

The MOTEL circuit, within the CDP6818, latches the state of the DS pin on the falling edge of AS/ALE When the 6800 mode of MOTEL is desired DS must be low during AS/ALE, which is the case with the CDP6805 family of multiplexed bus processors To insure the competitor mode of MOTEL, the DS pin must remain high during the time AS/ALE is high

R/$\overline{W}$ — READ/WRITE, INPUT

The MOTEL circuit treats the R/$\overline{W}$ pin in one of two ways When a 6805 type processor is connected, R/$\overline{W}$ is a level which indicates whether the current cycle is a read or write A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high, whereas a write cycle is a low on R/$\overline{W}$ during DS

The second interpretation of R/$\overline{W}$ is as a negative write pulse, $\overline{WR}$, $\overline{MEMW}$, and $\overline{I/OW}$ from competitor type processors The MOTEL circuit in this mode gives R/$\overline{W}$ pin the same meaning as the write ($\overline{W}$) pulse on many generic RAMs

$\overline{CE}$ — CHIP ENABLE, INPUT

The chip-enable ($\overline{CE}$) signal must be asserted (low) for a bus cycle in which the CDP6818 is to be accessed $\overline{CE}$ is not latched and must be stable during DS and AS (in the 6805 mode of MOTEL) and during $\overline{RD}$ and $\overline{WR}$ (in the competitor mode) Bus cycles which take place without asserting $\overline{CE}$ cause no actions to take place within the CDP6818 When $\overline{CE}$ is high, the multiplexed bus output is in a high-impedance state

When $\overline{CE}$ is high, all address, data, DS, and R/$\overline{W}$ inputs from the processor are disconnected within the CDP6818 This permits the CDP6818 to be isolated from a powered-down processor When $\overline{CE}$ is held high, an unpowered device cannot receive power through the input pins from the real-time clock power source Battery power consumption can thus be reduced by using a pullup resistor or active clamp on $\overline{CE}$ when the main power is off

$\overline{IRQ}$ — INTERRUPT REQUEST, OUTPUT

The $\overline{IRQ}$ pin is an active low output of the CDP6818 that may be used as an interrupt input to a processor The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set To clear the $\overline{IRQ}$ pin, the processor program normally reads Register C The $\overline{RESET}$ pin also clears pending interrupts

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high-impedance state Multiple interrupting devices may thus be connected to an $\overline{IRQ}$ bus with one pullup at the processor

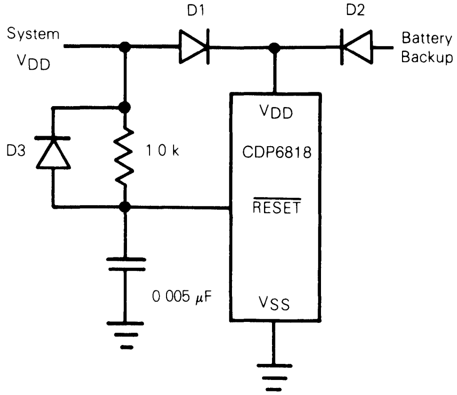
$\overline{RESET}$ — RESET, INPUT

The $\overline{RESET}$ pin does not affect the clock, calendar, or RAM functions On the powerup, the $\overline{RESET}$ pin must be held low for the specified time, t_{RLH}, in order to allow the power supply to stabilize Figure 13 shows a typical representation of the $\overline{RESET}$ pin circuit

When $\overline{RESET}$ is low the following occurs

a) Periodic Interrupt Enable (PIE) bit is cleared to zero,
b) Alarm Interrupt Enable (AIE) bit is cleared to zero,
c) Update ended Interrupt Enable (UIE) bit is cleared to zero,
d) Update ended Interrupt Flag (UF) bit is cleared to zero,
e) Interrupt Request status Flag (IRQF) bit is cleared to zero,
f) Periodic Interrupt Flag (PF) bit is cleared to zero,

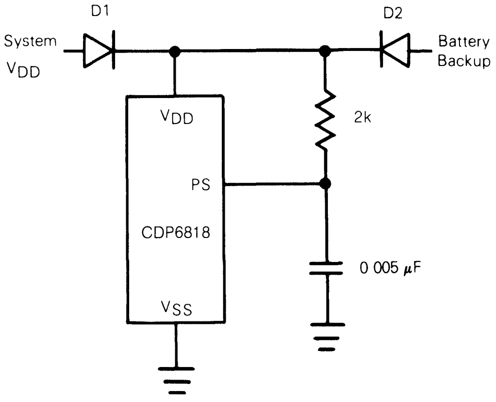
g) Alarm Interrupt Flag (AF) bit is cleared to zero,
h) $\overline{IRQ}$ pin is in high-impedance state, and
i) Square Wave output Enable (SQWE) bit is cleared to zero



D1 = D2 = D3 = 1N4148 or Equivalent

Note If the RTC is isolated from the MPU or MCU power by a diode drop, care must be taken to meet V_{in} requirements

Fig. 13 — Typical power-up delay circuit for $\overline{RESET}$



D1 = D2 = 1N4148 or Equivalent

Fig. 14 — Typical power-up delay circuit for POWER SENSE.

PS — POWER SENSE, INPUT

The power-sense pin is used in the control of the valid RAM and time (VRT) bit in Register D. When the PS pin is low the VRT bit is cleared to zero

During powerup, the PS pin must be externally held low for the specified time, t_{PL} As power is applied the VTR bit remains low indicating that the contents of the RAM, time registers, and calendar are not guaranteed. When normal operation commences PS should be permitted to go high after a powerup to allow the VRT bit to be set by a read of Register D Figure 14 shows a typical circuit connection for the power-sense pin

POWER-DOWN CONSIDERATIONS

In most systems, the CDP6818 must continue to keep time when system power is removed. In such systems, a conversion from system power to an alternate power supply, usually a battery, must be made During the transition from system to battery power, the designer of a battery backed-up RTC system must protect data integrity, minimize power consumption, and ensure hardware reliability.

The chip enable ($\overline{CE}$) pin controls all bus inputs (R/$\overline{W}$, DS, AS, AD0-AD7) $\overline{CE}$, when negated, disallows any unintended modification of the RTC data by the bus. $\overline{CE}$ also reduces power consumption by reducing the number of transitions seen internally

Power consumption may be further reduced by removing resistive and capacitive loads from the clock out (CKOUT) pin and the squarewave (SQW) pin

During and after the power source conversion, the V_{IN} maximum specification must never be exceeded. Failure to meet the V_{IN} maximum specification can cause a virtual SCR to appear which may result in excessive current drain and destruction of the part

ADDRESS MAP

Figure 15 shows the address map of the CDP6818 The memory consists of 50 general purpose RAM bytes, 10 RAM bytes which normally contain the time, calendar, and alarm data, and four control and status bytes All 64 bytes are directly readable and writable by the processor program except Registers C and D which are read only Bit 7 of Register A and the high order bit of the seconds byte are also read only. Bit 7, of the second byte, always reads "0". The contents of the four control and status registers are described in the Register section

TIME, CALENDAR, AND ALARM LOCATIONS

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations The contents of the 10 time, calendar, and alarm byte may be either binary or binary-coded decimal (BCD)

CDP6818

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD The SET bit may now be cleared to allow updates Once initialized the real-time clock makes all updates in the selected data mode The data mode cannot be changed without reinitializing the 10 data bytes

Table 3 shows the binary and BCD formats of the 10 time, calendar, and alarm locations The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23 The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high-order bit of the hours byte represents PM when it is a "1"

The time, calendar, and alarm bytes are not always accessable by the processor program Once-per-second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition If any of the 10 bytes are read at this time, the data outputs are undefined The update lockout time is 248 μs at the 4 194304 MHz and 1 048567 MHz time bases and 1948 μs for the 32 768 kHz time base The Update Cycle section shows how to accommodate the update cycle in the processor program

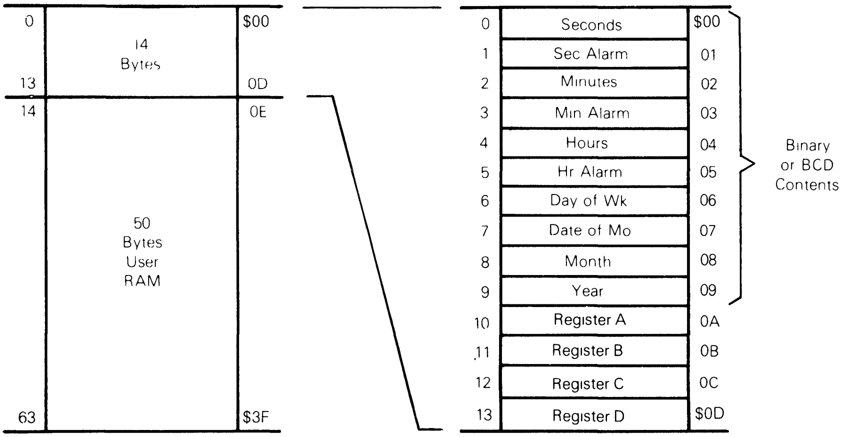


Fig. 15 — Address map.

TABLE 3 — TIME, CALENDAR, AND ALARM DATA MODES

Address Location	Function	Decimal Range	Range		Example*	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0	Seconds	0-59	$00-$3B	$00-$59	15	21
1	Seconds Alarm	0-59	$00-$3B	$00-$59	15	21
2	Minutes	0-59	$00-$3B	$00-$59	3A	58
3	Minutes Alarm	0-59	$00-$3B	$00-$59	3A	58
4	Hours (12 Hour Mode)	1-12	$01-$0C (AM) and $81-$8C (PM)	$01-$12 (AM) and $81-$92 (PM)	05	05
	Hours (24 Hour Mode)	0-23	$00-$17	$00-$23	05	05
5	Hours Alarm (12 Hour Mode)	1-12	$01-$0C (AM) and $81-$8C (PM)	$01-$12 (AM) and $81-$92 (PM)	05	05
	Hours Alarm (24 Hour Mode)	0-23	$00-$17	$00-23	05	05
6	Day of the Week Sunday = 1	1-7	$01-$ 07	$01-$07	05	05
7	Day of the Month	1-31	$01-$1F	$01-$31	0F	15
8	Month	1-12	$01-$0C	$01-$12	02	02
9	Year	0-99	$00-$63	$00-$99	4F	79

*Example 5 58 21 Thursday February 15 1979 (Time is A M)

The three alarm bytes may be used in two ways. When the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high The alternate usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any hexadecimal byte from C0 to FF That is, the two most-significant bits of each byte, when set to "1", create a "don't care" situation An alarm interrupt each hour is created with a "don't care" code in the hours alarm location Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second

STATIC CMOS RAM

The 50 general purpose RAM bytes are not dedicated within the CDP6818 They can be used by the processor program, and are fully available during the update cycle

When time and calendar information must use battery back-up, very frequently there is other non-volatile data that must be retained when main power is removed The 50 user RAM bytes serve the need for low-power CMOS battery-backed storage, and extend the RAM available to the program

When further CMOS RAM is needed, additional CDP6818S may be included in the system The time/calendar functions may be disabled by holding the DV0-DV2 dividers, in Register A, in the reset state or by setting the SET bit in CR2 Register B or by removing the oscillator Holding the dividers in reset prevents interrupts or SQW output from operating while setting the SET bit allows these functions to occur With the dividers clear, the available user RAM is extended to 59 bytes Bit 7 of Register A, Registers C and D, and the high-order Bit of the seconds byte cannot effectively be used as general purpose RAM

INTERRUPTS

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor The alarm interrupt may be programmed to occur at rates from once-per-second to one-a-day The periodic interrupt may be selected for rates from half-a-second to 30 517 μs The update-ended interrupt may be used to indicate to the program that an update cycle is completed Each of these independent interrupt conditions are described in greater detail in other sections

The processor program selects which interrupts, if any, it wishes to receive Three bits in Register B enable the three interrupts Writing a "1" to a interrupt-enable bit permits that interrupt to be initiated when the event occurs A "0" in the interrupt-enable bit prohibits the IRQ pin from being asserted due to the interrupt cause

If an interrupt flag is already set when the interrupt becomes enabled, the $\overline{\text{IRQ}}$ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs a flag bit is set to a "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The "interrupt" flag bit becomes a status bit, which the software interrogates, when it wishes. When the software detects that the flag is set, it is an indication to software that the "interrupt" event occurred since the bit was last read.

However, there is one precaution The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C so the bits which are set are stable throughout the read cycle All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held until after the read cycle One, two, or three flag bits may be found to be set when Register C is read The program should inspect all utilized flag bits every time Register C is read to insure that no interrupts are lost

The second flag bit usage method is with fully enabled interrupts When an interrupt-flag bit is set and the corresponding interrupt-enable bit is also set, the $\overline{\text{IRQ}}$ pin is asserted low $\overline{\text{IRQ}}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a "1" whenever the $\overline{\text{IRQ}}$ pin is being driven low

The processor program can determine that the RTC initiated the interrupt by reading Register C A "1" in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the part. The act of reading Register C clears all the then-active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt-mask bits set and service each interrupt which is set Again, more than one interrupt-flag bit may be set.

DIVIDER STAGES

The CDP6818 has 22 binary-divider stages following the time base as shown in Figure 1 The output of the dividers is a 1 Hz signal to the update-cycle logic. The dividers are controlled by three divider bits (DV2, DV1, and DV0) in Register A.

DIVIDER CONTROL

The divider-control bits have three uses, as shown in Table 4 Three usable operating time bases may be selected (4 194304 MHz, 1.048576 MHz, or 32.768 kHz) The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one second later The divider-control bits are also used to facilitate testing the CDP6818

TABLE 4 — DIVIDER CONFIGURATIONS

Time-Base Frequency	Divider Bits Register A			Operation Mode	Divider Reset	Bypass First N-Divider Bits
	DV2	DV1	DV0			
4 194304 MHz	0	0	0	Yes	-	N=0
1 048576 MHz	0	0	1	Yes	–	N=2
32 768 kHz	0	1	0	Yes	–	N=7
Any	1	1	0	No	Yes	–
Any	1	1	1	No	Yes	–

Note Other combinations of divider bits are used for test purposes only

SQUARE-WAVE OUTPUT SELECTION

Fifteen of the 22 divider taps are made available to a 1-of-15 selector as shown in Figure 1 The first purpose of selecting a divider tap is to generate a square-wave output signal on the SQW pin Four bits in Register A establish the square-wave frequency as listed in Table 5 The SQW frequency selection shares the 1-of-15 selector with periodic interrupts

Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square-wave enable (SQWE) bit in Register B Altering the divider, square-wave output selection bits, or the SQW output-enable bit may generate an asymetrical waveform at the time of execution The square-wave output pin has a number of potential uses For example, it can serve as a frequency standard for external use, a frequency synthesizer, or could be used to generate one or more audio tones under program control

PERIODIC INTERRUPT SELECTION

The periodic interrupt allows the $\overline{\mathrm{IRQ}}$ pin to be triggered from once every 500 ms to once every 30 517 μs The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day

Table 5 shows that the periodic interrupt rate is selected with the same Register A bits which select the square-wave frequency Changing one also changes the other But each function may be separately enabled so that a program could switch between the two features or use both The SQW pin is enabled by the SQWE bit. Similarly the periodic interrupt is enabled by the PIE bit in Register B

Periodic interrupt is usable by practically all real-time systems It can be used to scan for all forms of inputs from contact closures to serial receive bits on bytes It can be used in multiplexing displays or with software counters to measure inputs, create output intervals, or await the next needed software function

TABLE 5 — PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY

Rate Select Control Register A				4.194304 or 1.048576 MHz Time Base		32.768 kHz Time Base	
RS3	RS2	RS1	RS0	Periodic Interrupt Rate t_{PI}	SQW Output Frequency	Periodic Interrupt Rate t_{PI}	SQW Output Frequency
0	0	0	0	None	None	None	None
0	0	0	1	30 517 μs	32 768 kHz	3 90625 ms	256 Hz
0	0	1	0	61 035 μs	16 384 kHz	7 8125 ms	128 Hz
0	0	1	1	122 070 μs	8 192 kHz	122 070 μs	8 192 kHz
0	1	0	0	244 141 μs	4 096 kHz	244 141 μs	4 096 kHz
0	1	0	1	488 281 μs	2 048 kHz	488 281 μs	2 048 kHz
0	1	1	0	976 562 μs	1 024 kHz	976 562 μs	1 024 kHz
0	1	1	1	1 953125 ms	512 Hz	1 953125 ms	512 Hz
1	0	0	0	3 90625 ms	256 Hz	3 90625 ms	256 Hz
1	0	0	1	7 8125 ms	128 Hz	7 8125 ms	128 Hz
1	0	1	0	15 625 ms	64 Hz	15 625 ms	64 Hz
1	0	1	1	31 25 ms	32 Hz	31 25 ms	32 Hz
1	1	0	0	62 5 ms	16 Hz	62 5 ms	16 Hz
1	1	0	1	125 ms	8 Hz	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz	500 ms	2 Hz

UPDATE CYCLE

The CDP6818 executes an update cycle once-per-second, assuming one of the proper time bases is in place, the divider is not clear, and the SET bit in Register B is clear The SET bit in the "1" state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions

With a 4 194304 MHz or 1 048576 MHz time base the update cycle takes 248 µs while a 32 768 kHz time base update cycle takes 1984 µs During the update cycle, the time, calendar, and alarm bytes are not accessable by the processor program The CDP6818 protects the program from reading transitional data This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle If the processor reads these RAM locations before the update is complete the output will be undefined The update in progress (UIP) status bit is set during the interval

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts Three methods of accommodating nonavailability during update are usable by the program In discussing the three methods it is assumed that at random points user programs are able to call a subroutine to obtain the time of day

The first method of avoiding the update cycle uses the update-ended interrupt If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information During this time a display could be updated or the information could be transfered to continuously available RAM Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not The UIP bit will pulse once-per-second Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts After the UIP bit goes high, the update cycle begins 244 µs later Therefore, if a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed If a "1" is read in the UIP bit, the time/calendar data may not be valid The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs

The third method uses a periodic interrupt to determine if an update cycle is in progress The UIP bit in Register A is set high between the setting of the PF bit on Register C (see Figure 16). Periodic interrupts that occur at intervals greater than $t_{BUC} + t_{UC}$ allow valid time and date information to be read at each occurrence of the periodic interrupt. The reads should be completed within $(T_{PI} \div 2) + t_{BUC}$ to insure that data is not read during the update cycle To properly set the internal counters for Daylight Savings Time operation, the user must set the time at least two seconds before the rollover will occur Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

REGISTERS

The CDP6818 has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle

REGISTER A ($0A)

MSB LSB

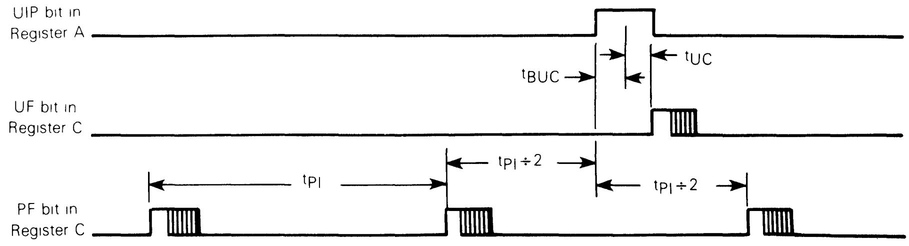
b7	b6	b5	b4	b3	b2	b1	b0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

Read/Write Register except UIP

UIP – The update in progress (UIP) bit is a status flag that may be monitored by the program When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244 µs (for all time bases). This is detailed in Table 6. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero – it is not in transition The UIP bit is a read-only bit, and is not affected by Reset Writing the SET bit in Register B to a "1" inhibits any update cycle and then clears the UIP status bit.

TABLE 6 – UPDATE CYCLE TIMES

UIP Bit	Time Base (OSC1)	Update Cycle Time (t_{UC})	Minimum Time Before Update Cycle (t_{BUC})
1	4 194304 MHz	248 µs	–
1	1 048576 MHz	248 µs	–
1	32 768 kHz	1984 µs	–
0	4 194304 MHz	–	244 µs
0	1 048576 MHz	–	244 µs
0	32 768 kHz	–	244 µs



t_{PI} = Periodic Interrupt Time Interval (500 ms, 250 ms, 125 ms, 62 5 ms etc per Table 5)
t_{UC} = Update Cycle Time (248 µs or 1984 µs)
t_{BUC} = Delay Time Before Update Cycle (244 µs)

Fig. 16 — Update-ended and periodic interrupt relationships.

DV2, DV1, DV0 – Three bits are used to permit the program to select various conditions of the 22-stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use Table 4 shows that time bases of 4 194304 MHz, 1 048576 MHz, and 32 768 kHz may be used The divider selection bits are also used to reset the divider chain When the time/calendar is first initialized, the program may start the divider at the precise time stored in the RAM When the divider reset is removed the first update cycle begins one-half second later These three read/write bits are not affected by RESET

RS3, RS2, RS1, RS0 – The four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output The tape selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt The program may do one of the following. 1) enable the interrupt with the PIE bit, 2) enable the SQW output pin with the SQWE bit, 3) enable both at the same time at the same rate, or 4) enable neither Table 5 lists the periodic interrupt rates and the square-wave frequencies that may be chosen with the RS bits These four bits are read/write bits which are not affected by RESET

REGISTER B ($0B)

Read/Write Register

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET – When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is read/write bit which is not modified but RESET or internal functions of the CDP6818

PIE — The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit in Register C to cause the IRQ pin to be driven low A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Register A A zero in PIE blocks IRQ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate PIE is not modified by any internal CDP6818 functions, but is cleared to "0" by a RESET

AIE – The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an IRQ signal The RESET pin clears AIE to "0". The internal functions do not affect the AIE bit

UIE – The UIE (update-ended interrupt enable) bit is a read/write bit which enables the update-end flage (UF) bit to assert IRQ The RESET pin going low or the SET bit going high clears the UIE bit

SQWE – When the square-wave enable (SQWE) bit is set to a "1" by the program, a square-wave signal at the frequency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a zero the SQW pin is held low. The state of SQWE is cleared by the RESET pin. SQWE is a read/write bit

DM – The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or RESET A "1" in DM signifies binary data, while a "0" in DM specifies binary-coded-decimal (BCD) data

24/12 – The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a "0") This is a read/write bit, which is affected only by the software

DSE – The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1") On the last Sunday in April the time increments from 1 59 59 AM to 3 00 00 AM On the last Sunday in October when the time first reaches 1 59 59 AM it changes to 1 00 00 AM These special updates do not occur when the DSE bit is a "0" DSE is not changed by any internal operations or RESET

REGISTER C ($0C)

Read-Only Register

MSB							LSB
b7	b6	b5	b4	b3	b	b1	b0
IRQF	PF	AF	UF	0	0	0	0

IRQF – The interrupt request flag (IRQF) is set to a "1" when one or more of the following are true

PF = PIE = "1"

AF = AIE = "1"

UF = UIE = "1"

i e , IRQF = PF•PIE + AF•AIE + UF•UIE

Any time the IRQF bit is a "1", the IRQ pin is driven low All flag bits are cleared after Register C is read by the program or when the RESET pin is low

PF – The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain The RS3 to RS0 bits establish the periodic rate PF is set to a "1" independent of the state of the PIE bit PF being a "1" initiates an IRQ signal and sets the IRQF bit when PIE is also a "1 " The PF bit is cleared by a RESET or a software read of Register C

AF – A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the IRQ pin to go low, and a "1" to appear in the IRQF bit, when the AIE bit also is a "1 " A RESET or a read of Register C clears AF

UF – The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting IRQ. UF is cleared by a Register C read or a RESET.

b3 TO b0 – The unused bits of Status Register 1 are read as "0's" They can not be written.

REGISTER D ($0D)

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

Read Only Register

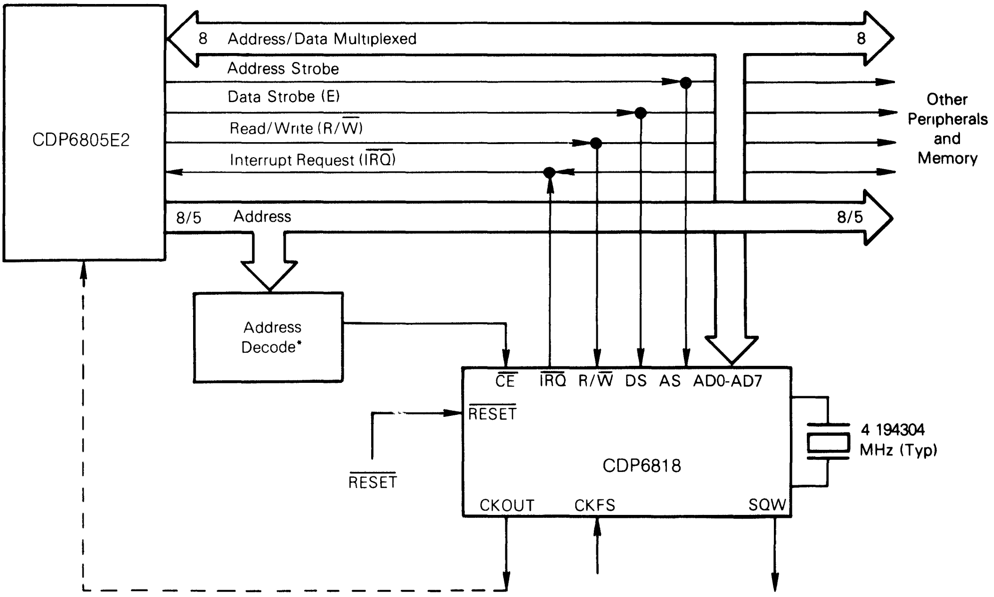
VRT – The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected A "0" appears in the VRT bit when the power-sense pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read/only bit which is not modified by the $\overline{\text{RESET}}$ pin The VRT bit can only be set by reading Register D

b6 TO b0 – The remaining bits of Register D are unused They cannot be written, but are always read as "0's "

TYPICAL INTERFACING

The CDP6818 is best suited for use with microprocessors which generate an address-then-data multiplexed bus. Figures 17 and 18 show typical interfaces to bus-compatible processors These interfaces assume that the address decoding can be done quickly. However, if standard metal-gate CMOS gates are used the $\overline{\text{CE}}$ setup time may be violated. Figure 19 illustrates an alternative method of chip selection which will accommodate such slower decoding.

The CDP6818 can be interfaced to single-chip microcomputers (MCU) by using eleven port lines as shown in Figure 20. Non-multiplexed bus microprocessors can be interfaced with additional support



*QMOS decoder

Fig. 17 — CDP6818 interfaced to CDP6805E2 compatible multiplexed bus microprocessors.

CDP6818

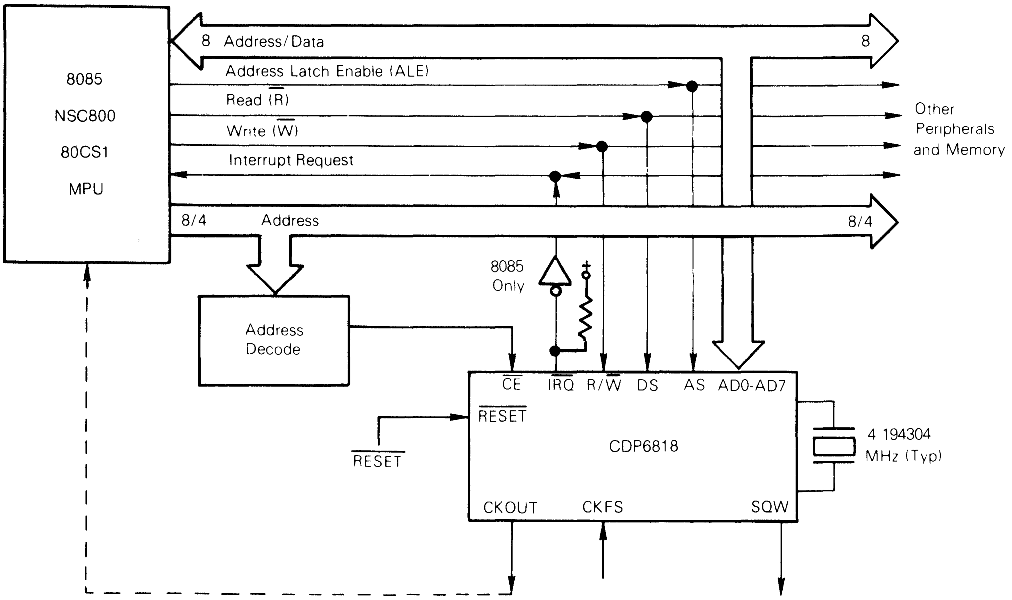
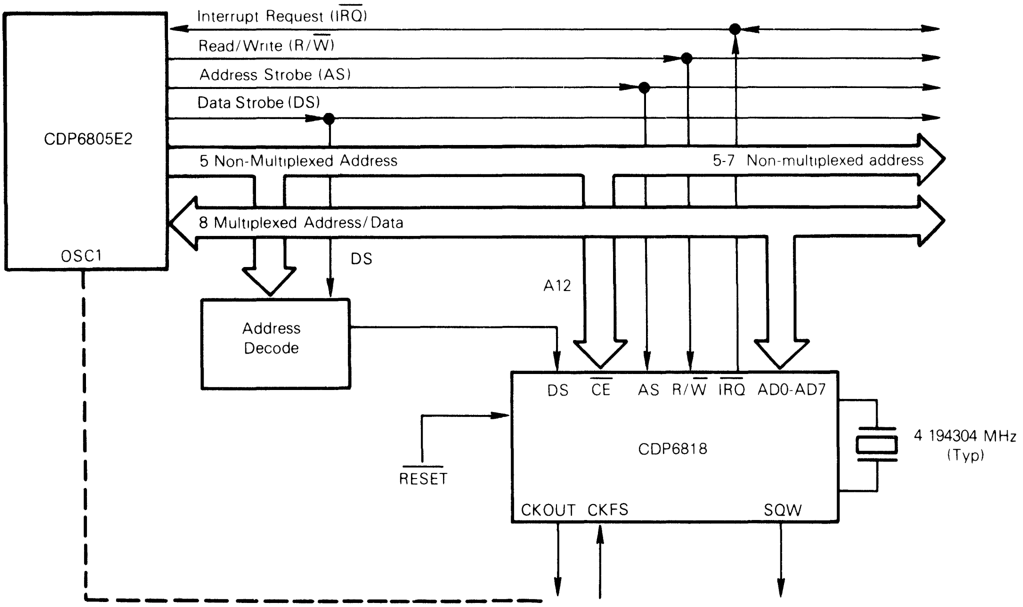


Fig. 18 — CDP6818 interfaced to competitor compatible multiplexed bus microprocessors



This illustrates the use of CMOS gating for address decoding

Fig. 19 — CDP6818 interface to CDP6805E2 CMOS multiplexed microprocessor with slow address decoding

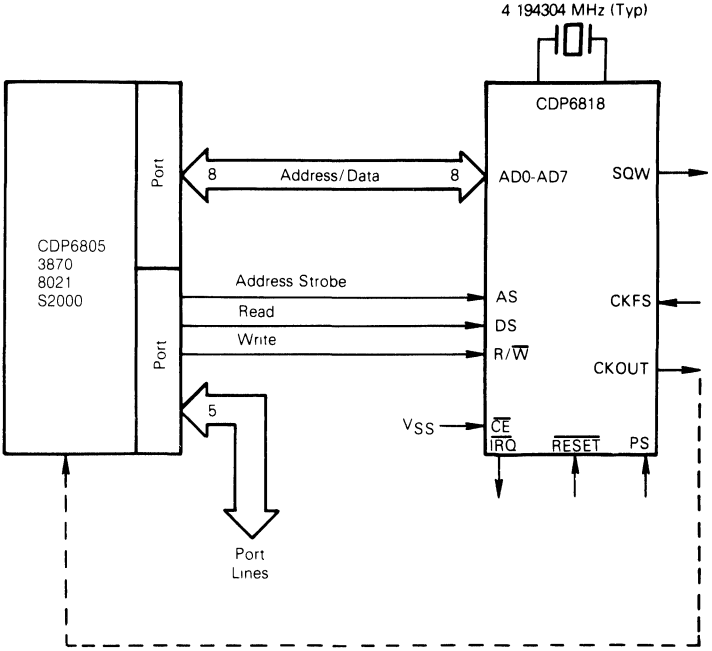


Fig. 20 — CDP6818 interfaced with the ports of a typical single-chip microcomputer.

There is one method of using the multiplexed bus CDP6818 with non-multiplexed bus processors The interface uses available bus control signals to multiplex the address and data bus together

An example using either the 6800, 6802, 6808, or 6809 microprocessor is shown in Figure 21

Figure 22 illustrates the subroutines which may be used for data transfers in a non-multiplexed system The subroutines should be entered with the registers containing the following data

Accumulator A· The address of the RTC to be accessed.
Accumulator B Write The data to be written
Read. The data read from the RTC

The RTC is mapped to two consecutive memory locations RTC and RTC + 1 as shown in Figure 21

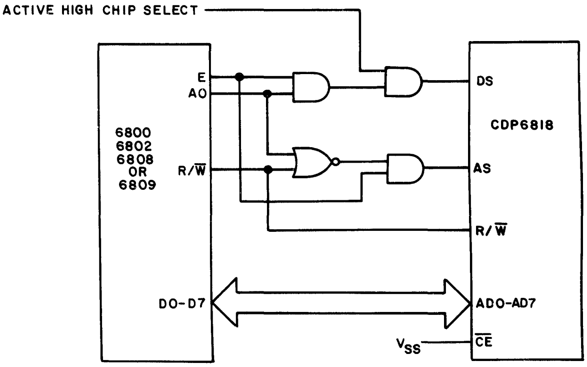


Fig. 21 — CDP6818 interfaced with Motorola type processors

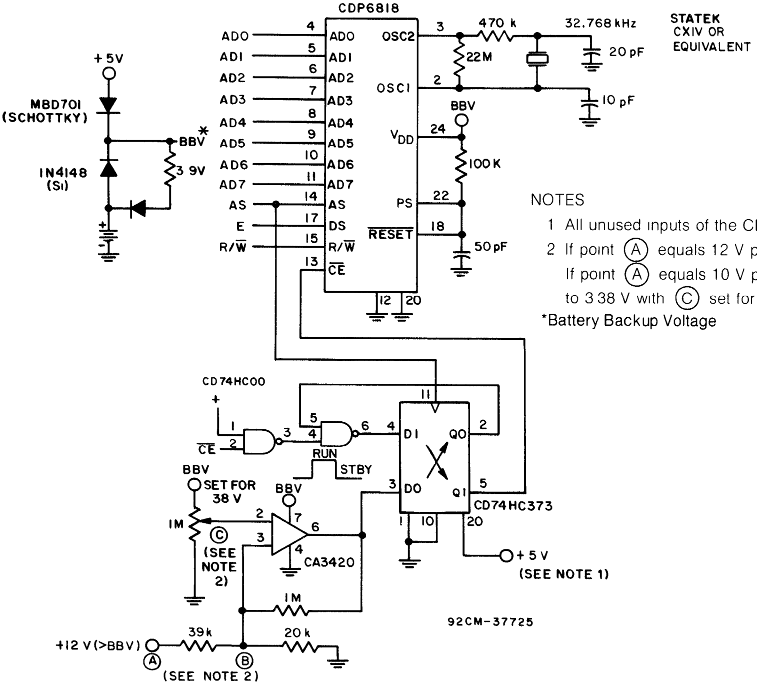
FIGURE 22 — SUBROUTINE FOR READING AND WRITING THE CDP6818 WITH A NON-MULTIPLEXED BUS

```
READ    STA    RTC      Generate AS and Latch Data from ACCA
        LDAB   RTC+1    Generate DS and Get Data
        RTS

WRITE   STA    RTC      Generate AS and Latch Data from ACCA
        STAB   RTC+1    Generate DS and Store Data
        RTS
```

IMPORTANT APPLICATION NOTICE

The CDP6818 with a bottom brand code of 6RR requires a synchronization of the $\overline{CE}$ pin with address strobe The following circuit will satisfy that condition and also shows a typical application of power down circuitry If $\overline{CE}$ is grounded at all times (no power down required) the following circuit need not be used



NOTES

1 All unused inputs of the CD74HC373 must be grounded

2 If point Ⓐ equals 12 V point Ⓑ should be equal to 4 06 V
If point Ⓐ equals 10 V point Ⓑ should be equal to 3 38 V with Ⓒ set for 3 18 V

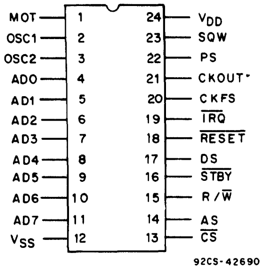
*Battery Backup Voltage

Fig 23 — Typical Application Circuit

Advance Information

CDP6818A

TERMINAL ASSIGNMENT



24-Lead Dual-In-Line Package

CMOS Real-Time Clock Plus RAM

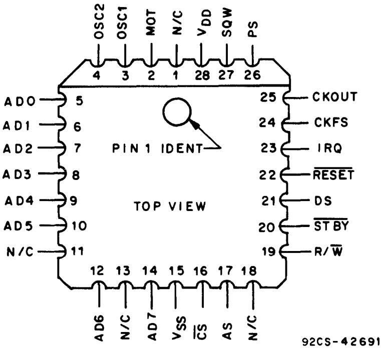
Features:

- *Low-power, high-speed CMOS*
- *Internal time base and oscillator*
- *Counts seconds, minutes, and hours of the day*
- *Counts days of the week, date, month, and year*
- *3 V to 6 V operation*
- *Time base input options: 4.194304 MHz, 1.048576 MHz, or 32.768 kHz*
- *Time base oscillator for parallel resonant crystals*
- *40 to 200 µW typical operating power at low frequency time base*
- *4.0 to 20 mW typical operating power at high frequency time base*

The CDP6818A Real-Time Clock plus RAM is a peripheral device which includes the unique MOTEL concept for use with various microprocessors, microcomputers, and larger computers. This part combines three unique features: a complete time-of-day clock with alarm and one hundred year calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of low-power static RAM. The CDP6818A uses high-speed CMOS technology to interface with 1 MHz processor buses, while consuming very little power.

The Real-Time Clock plus RAM has two distinct uses. First, it is designed as a battery powered CMOS part (in an otherwise NMOS/TTL system) including all the common battery backed-up functions such as RAM, time, and calendar. Secondly, the CDP6818A may be used with a CMOS microprocessor to relieve the software of the timekeeping workload and to extend the available RAM of an MPU such as the CDP6805E2.

TERMINAL ASSIGNMENT



28-Lead Plastic Chip-Carrier Package (Q Suffix)

- *Binary or BCD representation of time, calendar, and alarm*
- *12- or 24-hour clock with AM and PM in 12-hour mode*
- *Daylight savings time option*
- *Automatic end of month recognition*
- *Automatic leap year compensation*
- *Microprocessor bus compatible*
- *Selectable between Motorola and competitor bus timing*
- *Multiplexed bus for pin efficiency*
- *Interfaced with software as 64 RAM locations*
- *14 bytes of clock and control registers*
- *50 bytes of general purpose RAM*
- *Status bit indicates data integrity*
- *Bus compatible interrupt signals ($\overline{IRQ}$)*
- *Three interrupts are separately software maskable and testable*
    - *Time-of-day alarm, Once-per-second to Once-per-day*
    - *Periodic rates from 30.5 µs to 500 ms*
    - *End-of-clock update cycle*
- *Programmable square-wave output signal*
- *Clock output may be used as microprocessor clock input at time base frequency ÷1 or ÷4*

The CDP6818A is supplied in a 24-lead dual-in-line plastic package (E suffix), in a 24-lead dual-in-line side-brazed ceramic package (D suffix) and in a 28-lead plastic chip carrier package (Q suffix).

CDP6818A

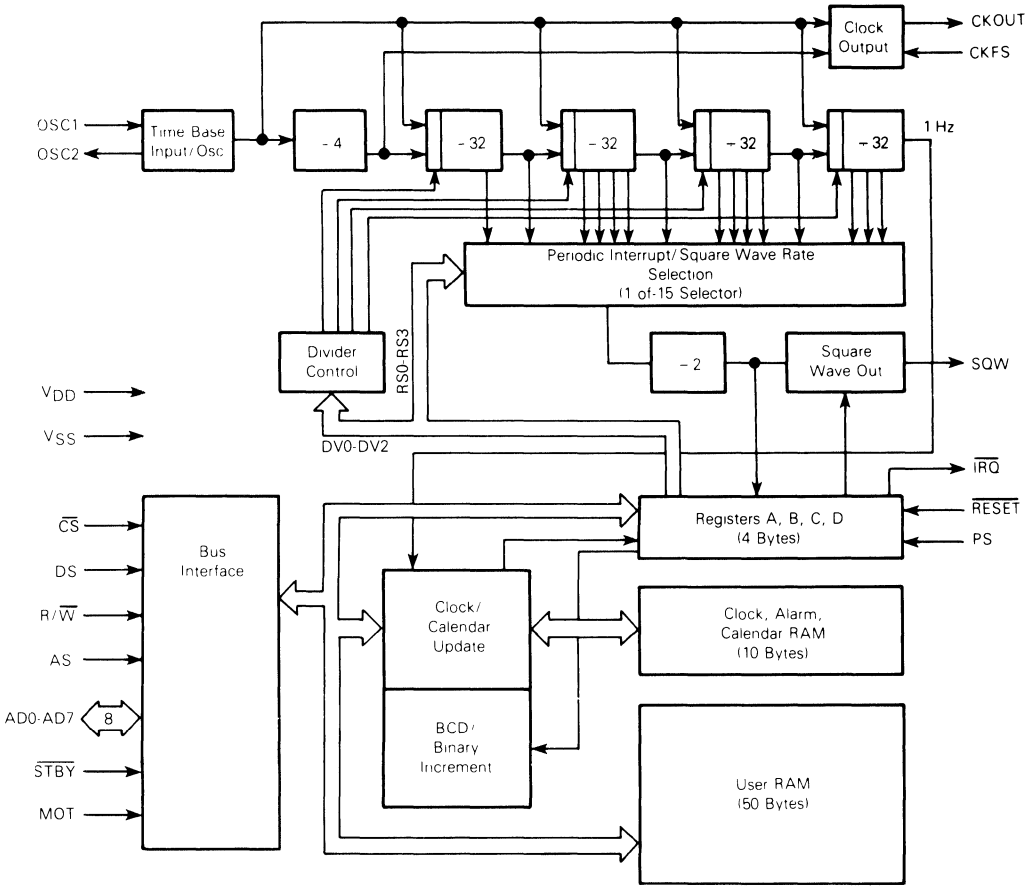


Fig. 1 - Block diagram.

92CS-42692

MAXIMUM RATINGS (*Voltages referenced to V_{SS}*)

SUPPLY VOLTAGE, V_{DD}	-0.3 to +8.0 V
ALL INPUT VOLTAGE, V_{IN}	V_{SS} -0.5 to V_{DD} +0.5 V
CURRENT DRAIN PER PIN EXCLUDING V_{DD} and V_{SS}, I	10 mA
OPERATING TEMPERATURE RANGE, $T_A = T_L$ to T_H	
CDP6818A	0 to 70°C
CDP6818AC	-40 to 85°C
STORAGE TEMPERATURE RANGE, T_{stg}	-55 to +150°C

THERMAL CHARACTERISTICS

THERMAL RESISTANCE, θ_{JA}	
Plastic (E Suffix)	120°C/W
Ceramic (D Suffix)	50°C/W
Chip-Carrier (Q Suffix)*	80°C/W

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \leq (V_{IN}$ or $V_{OUT}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H Unless Otherwise Noted)

CHARACTERISTIC		LIMITS		UNITS
		MIN.	MAX.	
Frequency of Operation	f_{osc}	32.768	32.768	kHz
Output Voltage	V_{OL}	—	0.1	V
I_{Load} < 10 μA	V_{OH}	V_{DD}-0.1	—	
I_{DD} - Bus Idle CKOUT = f_{osc}, C_L = 15 pF; SQW Disabled, $\overline{\text{STBY}}$ = 0.2 V; C_L (OSC2) = 10 pF f_{osc} = 32.768 kHz	I_{DD3}	—	50	μA
I_{DD} - Quiescent f_{osc} = DC; OSC1 = DC; All Other Inputs = V_{DD}-0.2 V; No Clock	I_{DD4}	—	50	μA
Output High Voltage (I_{Load} = -0.25 mA, All Outputs)	V_{OH}	2.7	—	V
Output Low Voltage (I_{Load} = 0.25 mA, All Outputs)	V_{OL}	—	0.3	V
Input High Voltage	V_{IH}			V
$\overline{\text{STBY}}$, AD0-AD7, DS, AS, R/$\overline{\text{W}}$, $\overline{\text{CS}}$		2.1	V_{DD}	
$\overline{\text{RESET}}$, CKFS, PS, OSC1		2.5	V_{DD}	
MOT		V_{DD}	V_{DD}	
Input Low Voltage	V_{IL}			V
$\overline{\text{STBY}}$, AD0-AD7, DS, AS, R/$\overline{\text{W}}$, $\overline{\text{CS}}$, CKFS, PS, $\overline{\text{RESET}}$, OSC1		V_{SS}	0.5	
MOT		V_{SS}	V_{SS}	
Input Current	I_{in}			μA
AS, DS, R/$\overline{\text{W}}$		—	±10	
MOT, OSC1, $\overline{\text{CE}}$, $\overline{\text{STBY}}$, $\overline{\text{RESET}}$, CKFS, PS		—	±1	
Three-State Leakage $\overline{\text{IRQ}}$, AD0-AD7	I_{TSL}	—	±10	μA

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 Vdc ± 10%, V_{SS} = 0 Vdc; T_A = T_L to T_H Unless Otherwise Noted)

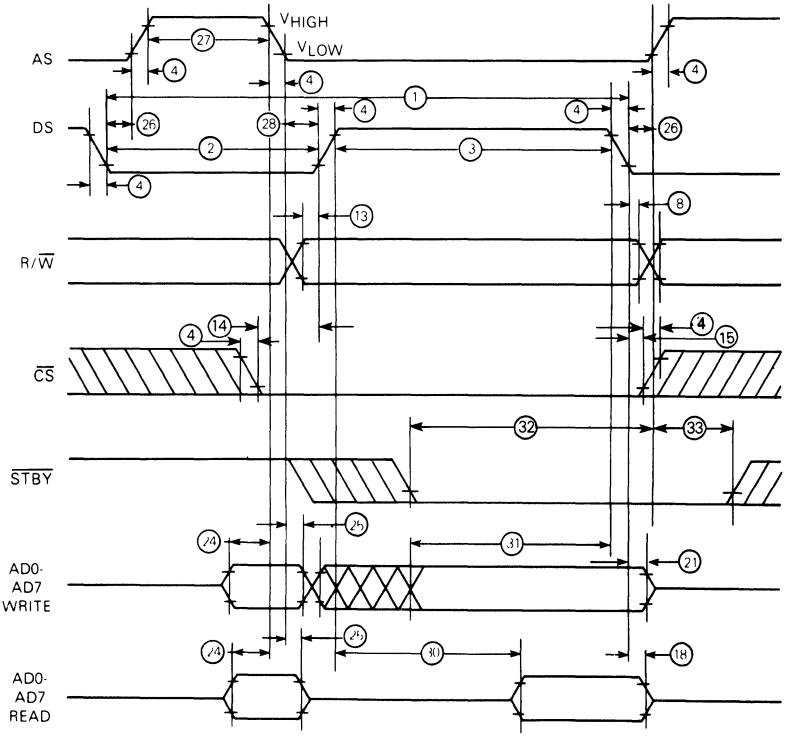
CHARACTERISTIC		LIMITS		UNITS
		MIN.	MAX.	
Frequency of Operation	f_{osc}	32.768	4194.304	kHz
Output Voltage	V_{OL}	—	0.1	V
I_{Load} < 10 μA	V_{OH}	V_{DD}-0.1	—	
I_{DD} - Bus Idle (External Clock) CKOUT = f_{osc}, C_L = 15 pF; SQW Disabled, $\overline{\text{STBY}}$ = 0.2 V; C_L (OSC2) = 10 pF				
f_{osc} = 4.194304 MHz	I_{DD1}	—	3	mA
f_{osc} = 1.048516 MHz	I_{DD2}	—	800	μA
f_{osc} = 32.768 kHz	I_{DD3}	—	50	μA
I_{DD} - Quiescent f_{osc} = DC; OSC1 = DC; All Other Inputs = V_{DD}-0.2 V; No Clock	I_{DD4}	—	50	μA
Output High Voltage (I_{Load} = -1.6 mA, AD0-AD7, CKOUT) (I_{Load} = -1.0 mA, SQW)	V_{OH}	4.1	—	V
Output Low Voltage (I_{Load} = 1.5 mA, AD0-AD7, CKOUT) (I_{Load} = 1.0 mA, $\overline{\text{IRQ}}$ and SQW)	V_{OL}	—	0.4	V
Input High Voltage	V_{IH}			V
$\overline{\text{STBY}}$, CFKS, AD0-AD7, DS, AS, R/$\overline{\text{W}}$, $\overline{\text{CS}}$, PS		V_{DD}-2.0	V_{DD}	
$\overline{\text{RESET}}$		V_{DD}-0.8	V_{DD}	
OSC1		V_{DD}-1.0	V_{DD}	
MOT		V_{DD}	V_{DD}	
Input Low Voltage	V_{IL}			V
CKFS, PS, $\overline{\text{RESET}}$, $\overline{\text{STBY}}$, AD0-AD7, DS, AS, R/$\overline{\text{W}}$, $\overline{\text{CS}}$, OSC1		V_{SS}	0.8	
MOT		V_{SS}	V_{SS}	
Input Current	I_{in}			μA
AS, DS, R/$\overline{\text{W}}$		—	±10	
MOT, OSC1, $\overline{\text{CE}}$, $\overline{\text{STBY}}$, $\overline{\text{RESET}}$, CKFS, PS		—	±1	
Three-State Leakage $\overline{\text{IRQ}}$, AD0-AD7	I_{TSL}	—	±10	μA

CDP6818A

BUS TIMING

IDENT. NO.	CHARACTERISTIC		V_{DD} = 3.0 V 50 pF LOAD		V_{DD} = 5.0 V ± 10% 1 TTL & 130 pF LOAD		UNITS
			MIN.	MAX.	MIN.	MAX.	
1	Cycle Time	t_{cyc}	5000	—	953	dc	ns
2	Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High	PW_{EL}	1000	—	300	—	ns
3	Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low	PW_{EH}	1500	—	325	—	ns
4	Input Rise and Fall Time	t_r, t_f	—	100	—	30	ns
8	R/$\overline{W}$ Hold Time	t_{RWH}	10	—	10	—	ns
13	R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}	200	—	80	—	ns
14	Chip Select Setup Time Before DS, $\overline{WR}$, or $\overline{RD}$	t_{CS}	200	—	25	—	ns
15	Chip Select Hold Time	t_{CH}	10	—	0	—	ns
18	Read Data Hold Time	t_{DHR}	10	1000	10	100	ns
21	Write Data Hold Time	t_{DHW}	100	—	0	—	ns
24	Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	200	—	50	—	ns
25	Muxed Address Hold Time	t_{AHL}	100	—	20	—	ns
26	Delay Time DS/E to AS/ALE Rise	t_{ASD}	500	—	50	—	ns
27	Pulse Width, AS/ALE High	PW_{ASH}	600	—	135	—	ns
28	Delay Time, AS/ALE to DS/E Rise	t_{ASED}	500	—	60	—	ns
30	Peripheral Output Data Delay Time from DS/E or $\overline{RD}$	t_{DDR}	1300	—	20	240	ns
31	Peripheral Data Setup Time	t_{DSW}	1500	—	200	—	ns
32	$\overline{STBY}$ Setup Time Before AS/ALE Rise	t_{SBS}	20	—	20	—	ns
33	$\overline{STBY}$ Hold Time After AS/ALE Fall	t_{SBH}	100	—	50	—	ns

NOTE: Designations E, ALE, RD, and WR Refer to signals from alternative microprocessor signals.



Note $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5.0$ V ± 10% for outputs only
$V_{HIGH} = 2.0$ V, $V_{LOW} = 0.5$ V for $V_{DD} = 3.0$ V for outputs only

92CS-42693

Fig. 2 - CDP6818A bus timing.

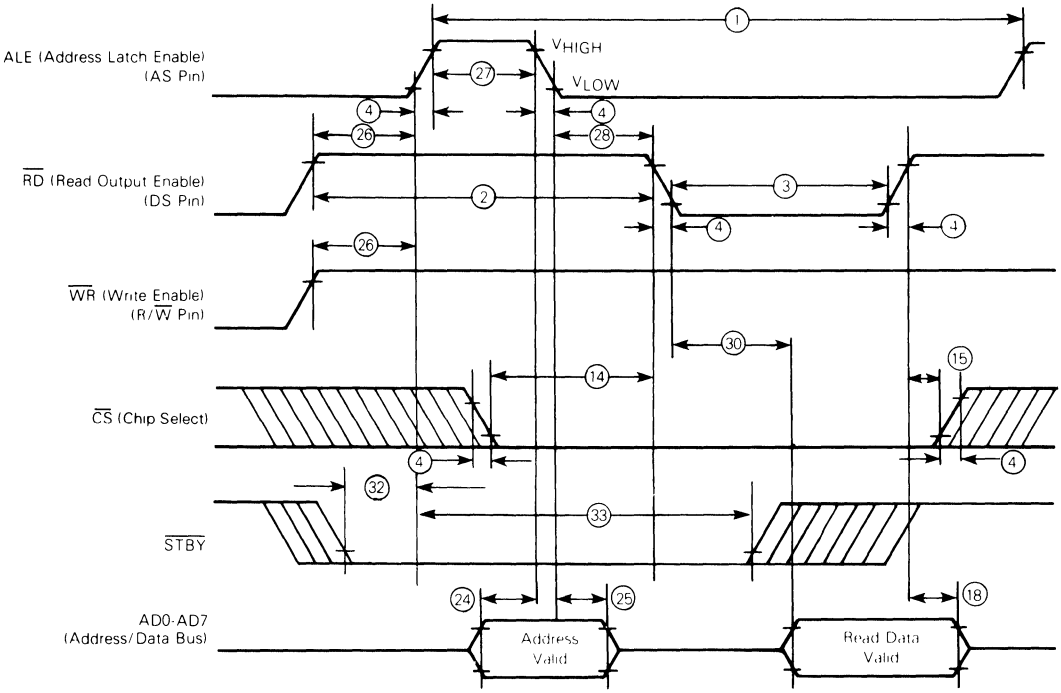
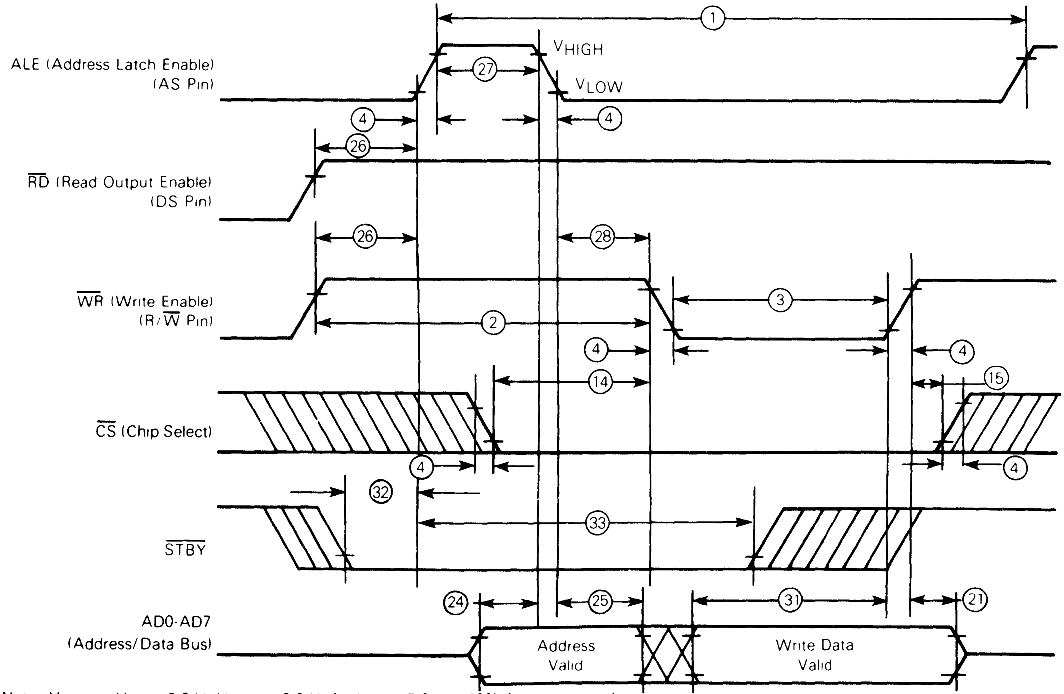


Fig. 3 - Bus read timing competitor multiplexed bus.

92CS-42694



Note $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5.0$ V ± 10% for outputs only
$V_{HIGH} = 2.0$ V, $V_{LOW} = 0.5$ V, for $V_{DD} = 3.0$ V for outputs only

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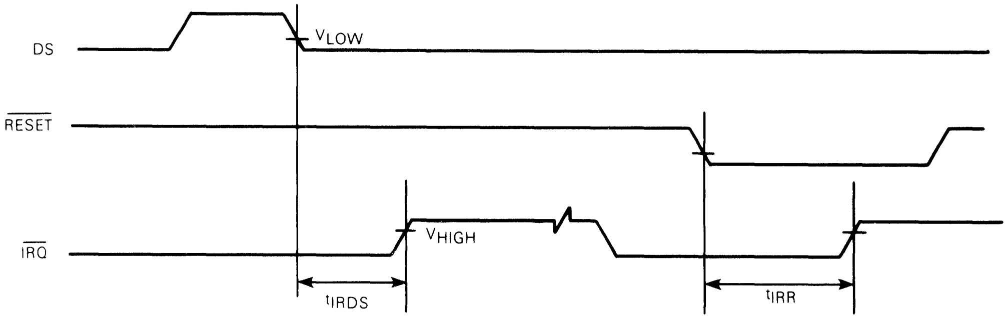
Fig. 4 - Bus write timing competitor multiplexed bus.

CDP6818A

TABLE 1 - SWITCHING CHARACTERISTICS (V_{SS} = 0 Vdc, T_A = T_L to T_H)

CHARACTERISTIC		V_{DD} = 3.0 Vdc		V_{DD} = 5.0 Vdc ± 10%		UNITS
		MIN.	MAX.	MIN.	MAX.	
Oscillator Startup	t_{RC}	—	300	—	100	ms
Reset Pulse Width	t_{RWL}	25	—	5	—	μs
Reset Delay Time	t_{RLH}	25	—	5	—	μs
Power Sense Pulse Width	t_{PWL}	25	—	5	—	μs
Power Sense Delay Time	t_{PLH}	25	—	5	—	μs
$\overline{IRQ}$ Release from DS	t_{IRDS}	—	10	—	2	μs
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}	—	10	—	2	μs
VRT Bit Delay	t_{VRTD}	—	10	—	2	μs



NOTE $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5.0$ V ± 10%

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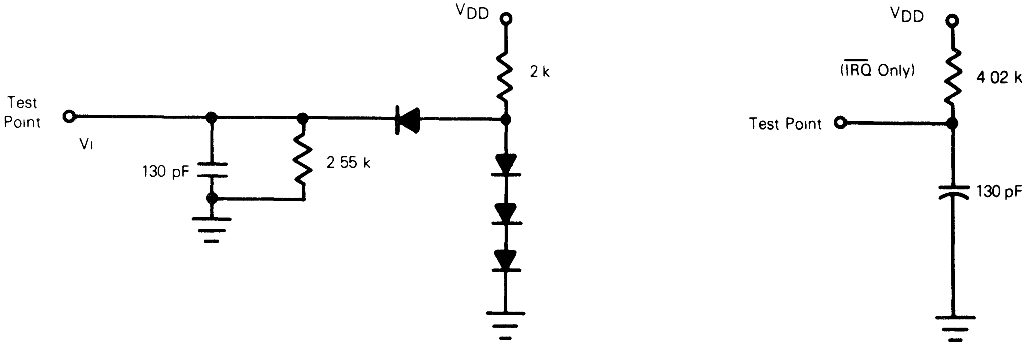
Fig. 5 - $\overline{IRQ}$ release delay.



All Outputs Except OSC2 (See Figure 10)

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Fig. 6 - TTL equivalent test load.

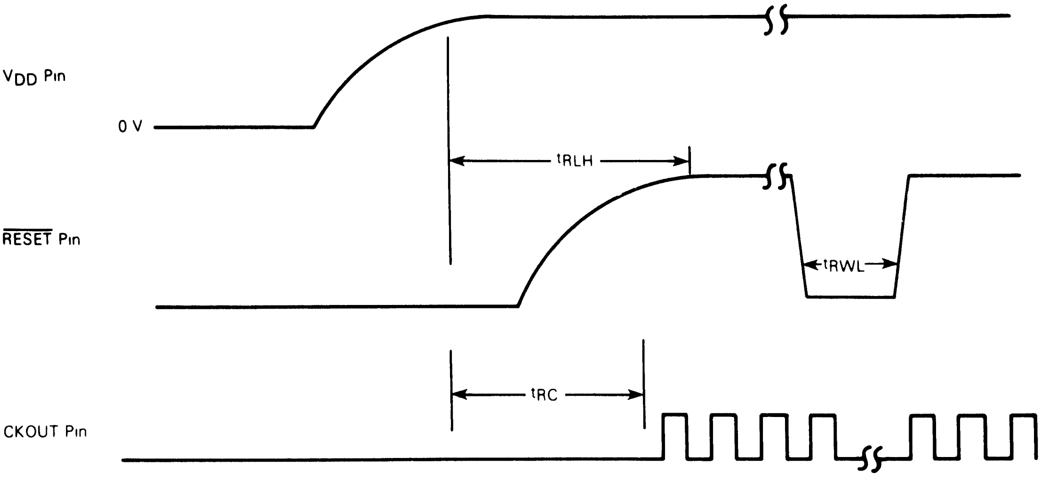
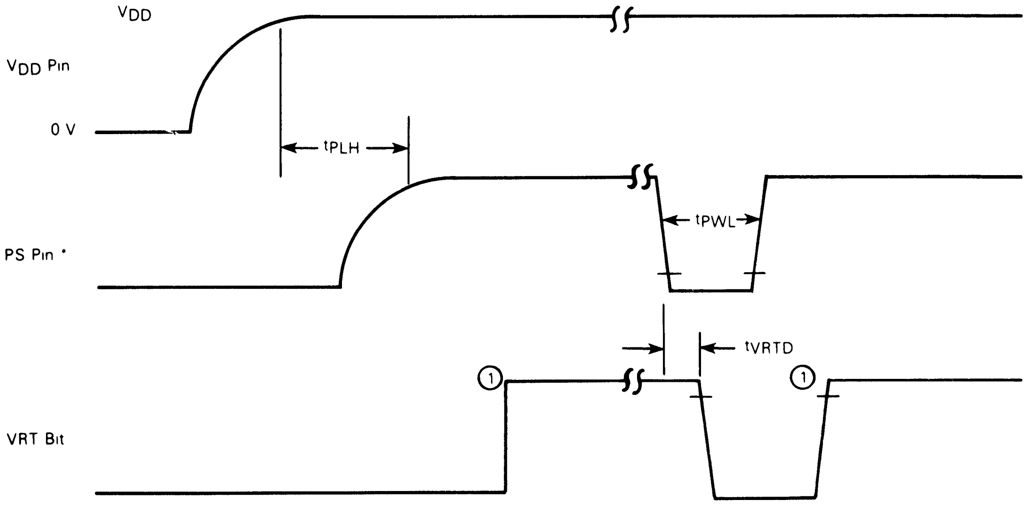


Fig. 7 - Power-up.



① The VRT bit is set to a "1" by reading Register d The VRT bit can only be cleared by pulling the PS pin low (see **REGISTER D ($0D)**)

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Fig. 8 - Conditions that clear VRT bit.

SIGNAL DESCRIPTIONS

The block diagram in Figure 1, shows the pin connection with the major internal functions of the CDP6818A Real-Time Clock plus RAM. The following paragraphs describe the function of each pin.

V_{DD}, V_{SS}

DC power is provided to the part on these two pins V_{DD} being the more positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

MOT - MOTEL

The MOT pin offers flexibility when choosing bus type. When tied to V_{DD}, GE/RCA timing is used. When tied to V_{SS}, competitor timing is used. The MOT pin must be hardwired to the V_{DD} or V_{SS} supply and cannot be switched during operation of the CDP6818A.

OSC1, OSC2 - Time Base, Inputs

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304 MHz, 1.048576 MHz, or 32.768 KHz may be connected to OSC1 as shown in Figure 9. The internal time-base frequency to be used is chosen in Register A.

The on-chip oscillator is designed for a parallel resonant AT cut crystal at 4.194304 MHz, 1.048576 MHz or 32.768 kHz frequencies. The crystal connections are shown in Figure 10 and the crystal characteristics in Figure 11.

CKOUT - Clock Out, Output

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 2.

CKFS - Clock Out Frequency Select, Input

When the CKFS pin is tied to V_{DD}, it causes CKOUT to be the same frequency as the time base at the OSC1 pin. When CKFS is tied to V_{SS}, CKOUT is the OSC1 time-base frequency divided by four. Table 2 summarizes the effect of CKFS.

TABLE 2 - CLOCK OUTPUT FREQUENCIES

TIME BASE (OSC1) FREQUENCY	CLOCK FREQUENCY SELECT PIN (CKFS)	CLOCK FREQUENCY OUTPUT PIN (CKOUT)
4.194304 MHz	High	4.194304 MHz
4.194304 MHz	Low	1.048576 MHz
1.048576 MHz	High	1.048576 MHz
1.048576 MHz	Low	262.144 KHz
32.768 kHz	High	32.768 kHz
32.768 KHz	Low	8.192 KHz

SQW - Square Wave, Output

The SQW pin can output a signal from one of the 15 taps provided by the 22 internal-divider stages. The frequency of the SQW may be altered by programming Register A, as shown in Table 5. The SQW signal may be turned on and off using the SQWE bit in Register B.

AD0-AD7 - Multiplexed Bidirectional Address/Data Bus

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data. Address-then-data multiplexing does not slow the access time of the CDP6818A since the bus reversal from address to data is occurring during the internal RAM access time.

The address must be valid just prior to the fall of AS/ALE at which time the CDP6818A latches the address from AD0 to AD5. Valid write data must be presented and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle, the CDP6818A outputs eight bits of data during the latter portion of the DS or $\overline{RD}$ pulses, then ceases driving the bus (returns the output drivers to the high-impedance state) when DS falls in the 6800 type or $\overline{RD}$ rises in the other case.

AS - Multiplexed Address Strobe, Input

A positive going multiplexed address strobe pulse serves to demultiplex the bus. The falling edge of AS or ALE causes the address to be latched within the CDP6818A.

DS - Data Strobe or Read, Input

The DS pin has two interpretations via the MOTEL circuit. When emanating from a 6800 type processor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and $\phi 2$ ($\phi 2$ clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the Real-Time Clock puls RAM to latch the written data.

The second MOTEL interpretation of DS is that of $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ emanating from the competitor type processor. In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data. This interpretation of DS is also the same as an output-enable signal on a typical memory.

R/$\overline{W}$ - Read/Write, Input

The MOTEL circuit treats the R/$\overline{W}$ pin in one of two ways. When a 6800 type processor is connected, R/$\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high, whereas a write cycle is a low on R/$\overline{W}$ during DS.

The second interpretation of R/$\overline{W}$ is as a negative write pulse, $\overline{WR}$, $\overline{MEMW}$, and $\overline{I/OW}$ from competitor type processors. The MOTEL circuit in this mode gives R/$\overline{W}$ pin the same meaning as the write ($\overline{W}$) pulse on many generic RAMS.

$\overline{CS}$ - Chip Select, Input

The chip-select ($\overline{CS}$) signal must be asserted (low) for a bus cycle in which the CDP6818A is to be accessed. $\overline{CS}$ is not latched and must be stable during DS and AS (6800 type of MOTEL) and during $\overline{RD}$ and $\overline{WR}$. Bus cycles which take place without asserting $\overline{CS}$ cause no actions to take place within the CDP6818A. When $\overline{CS}$ is not used, it should be grounded. (See Figure 20).

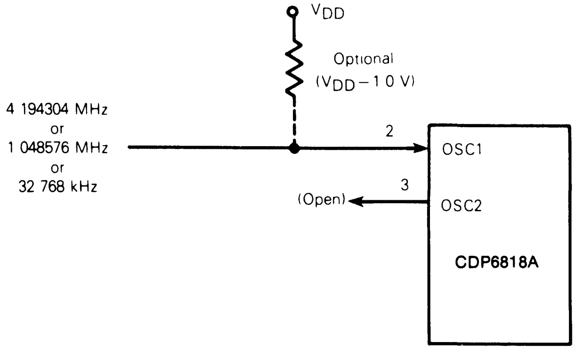
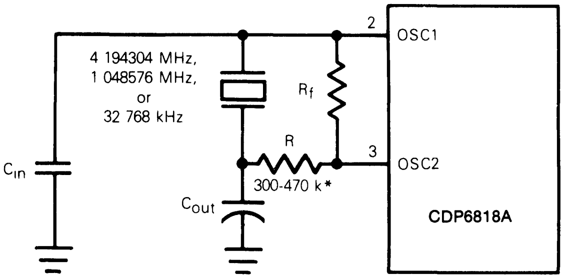


Fig. 9 - External time-base connection.



*32 768 kHz Only — Consult Crystal Manufacturer's Specification

Fig. 10 - Crystal oscillator connection.

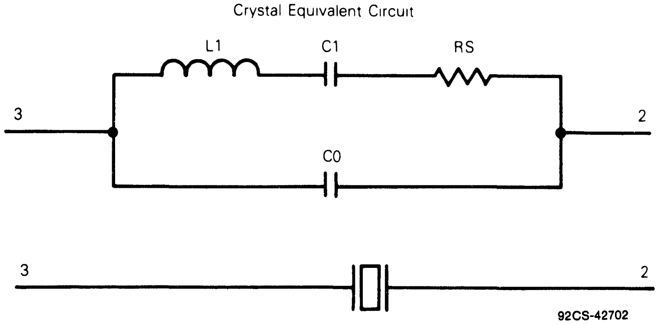

Crystal Equivalent Circuit

Fig. 11 - Crystal parameters.

f_{osc}	4.194304 MHz	1.048576 MHz	32.768 kHz
RS (Maximum)	75 Ω	700 Ω	50 k
C0 (Maximum)	7 pF	5 pF	1.7 pF
C1	0.012 pF	0.008 pF	0.003 pF
Q	50 k	35 k	30 k
C_{in}/C_{out}	15-30 pF	15-40 pF	10-22 pF
R	—	—	300-470 k
R_f	10 M	10 M	22 M

$\overline{IRQ}$ - Interrupt Request, Output

The $\overline{IRQ}$ pin is an active low output of the CDP6818A that may be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the processor program normally reads Register C. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high-impedance state. Multiple interrupting devices may thus be connected to an $\overline{IRQ}$ bus with one pullup at the processor.

$\overline{RESET}$ - RESET, Input

The $\overline{RESET}$ pin does not affect the clock, calendar, or RAM functions. On powerup, the $\overline{RESET}$ pin must be held low for the specified time, t_{RLH}, in order to allow the power supply to stabilize. Figure 12 shows a typical representation of the $\overline{RESET}$ pin circuit.

When $\overline{RESET}$ is low the following occurs:

a) Periodic Interrupt Enable (PIE) bit is cleared to zero,
b) Alarm Interrupt Enable (AIE) bit is cleared to zero,
c) Alarm Interrupt Enable (AIE) bit is cleared to zero,
d) Update ended Interrupt Flag (UF) bit is cleared to zero,
e) Interrupt Request status Flag (IRQF) bit is cleared to zero,
f) Periodic Interrupt Flag (PF) bit is cleared to zero,
g) The part is not accessible.
h) Alarm Interrupt Flag (AF) bit is cleared to zero,
i) $\overline{IRQ}$ pin is in high-impedance state, and
j) Square Wave output Enable (SQWE) bit is cleared to zero.

$\overline{STBY}$ - Stand-by

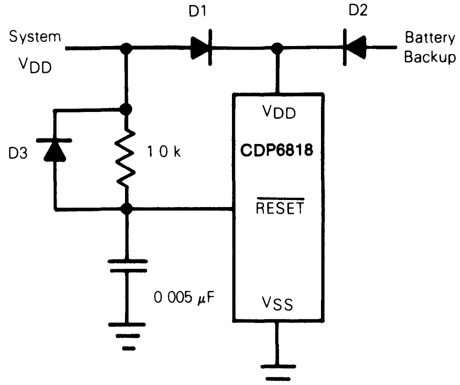
The $\overline{STBY}$ pin, when active, prevents access to the CDP6818A making it ideal for battery back-up applications. Stand-by operation incorporates a transparent latch. After data strobe (DS) goes low ($\overline{RD}$ or $\overline{WR}$ rises), $\overline{STBY}$ is recognized as a valid signal.

The $\overline{STBY}$ signal is totally asynchronous. Its transparent latch is opened by the falling edge of DS (rising edge of $\overline{RD}$ or $\overline{WR}$) and clocked by the rising edge of AS (ALE). Therefore, for $\overline{STBY}$ to be recognized, DS and AS should occur in pairs. When $\overline{STBY}$ goes low before the falling edge of DS (rising edge of $\overline{WR}$ or $\overline{RD}$), the current cycle is completed at that edge and the next cycle will not be executed.

PS - Power Sense, Input

The power-sense pin is used in the control of the valid RAM and time (VRT) bit in Register D. When the PS pin is low the WRT bit is cleared to zero.

When using the VRT feature during powerup, the PS pin must be externally held low for the specified t_{PLH} time. As power is applied, the VRT bit remains low indicating that the contents of the RAM, time registers, and calendar are not guaranteed. PS must go high after powerup to allow the VRT bit to be set by a read of register D.

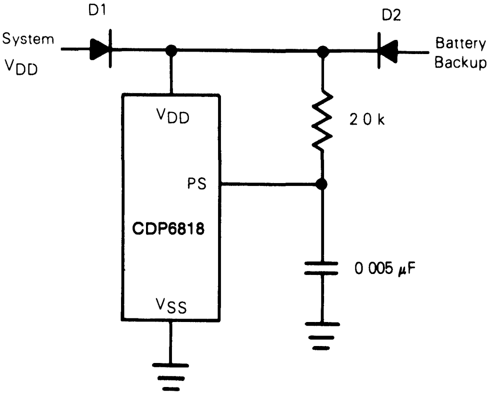


D1 = D2 = D3 = 1N4148 or Equivalent

Note If the RTC is isolated from the MPU or MCU power by a diode drop, care must be taken to meet V_{in} requirements

92CS-42703

Fig. 12 - Typical power-up delay circuit for reset.



D1 = D2 = 1N4148 or Equivalent

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Fig. 13 - Typical power-up delay circuit for power sense.

Power-Down Considerations

In most systems, the CDP6818A must continue to keep time when system power is removed. In such systems, a conversion from system power to an alternate power supply, usually a battery, must be made. During the transition from system to battery power, the designer of a battery backed-up RTC system must protect data integrity, minimize power consumption, and ensure hardware reliability.

The stand-by ($\overline{STBY}$) pin controls all bus inputs (R/$\overline{W}$, DS, AS, AD0-AD7) $\overline{STBY}$, when negated, disallows any unintended modification of the RTC data by the bus. $\overline{STBY}$ also reduces power consumption by reducing the number of transitions seen internally.

Power consumption may be further reduced by removing resistive and capacitive loads from the clock out (CKOUT) pin and the squarewave (SQW) pin.

During and after the power source conversion, the V_{IN} maximum specification must never be exceeded. Failure to meet the V_{IN} maximum specification can cause a virtual SCR to appear which may result in excessive current drain and destruction of the part.

Address Map

Figure 14 shows the address map of the CDP6818A. The memory consists of 50 general purpose RAM bytes, 10 RAM bytes which normally contain the time, calendar, and alarm data, and four control and status bytes. All 64 bytes are directly readable and writable by the processor program except for the following: 1) Registers C and D are read only, 2) bit 7 of Register A is read only, and 3) the high-order bit of the seconds byte is read only. The contents of four control and status registers (A, B, C, and D) are described in **REGISTERS.**

Time, Calendar, and Alarm Locations

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occuring. The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized the real-time clock makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the 10 data bytes.

Table 3 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high-order bit of the hours byte represent PM when it is a "1".

The time, calendar, and alarm bytes are not always accessible by the processor program. Once per second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 248 μs at the 4.194304 MHz and 1.048567 MHz time bases and 1948 μs for the 32.768 kHz time base. The Update Cycle section shows how to accommodate the update cycle in the processor program.

The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any hexadecimal byte from CO to FF. That is, the two most-significant bits of each byte, when set to "1", create a "don't care" situation. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

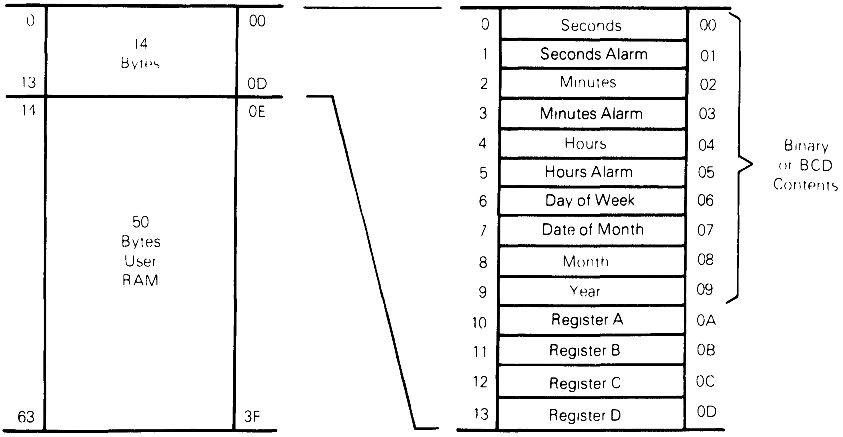


Fig. 14 - Address map.

CDP6818A

TABLE 3 - TIME, CALENDAR, AND ALARM DATA MODES

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE		EXAMPLE *	
			BINARY DATA MODE	BCD DATA MODE	BINARY DATE MODE	BCD DATA MODE
0	Seconds	0-59	$00-$3B	$00-$59	15	21
1	Seconds Alarm	0-59	$00-$3B	$00-$59	15	21
2	Minutes	0-59	$00-$3B	$00-$59	3A	58
3	Minutes Alarm	0-59	$00-$3B	$00-$59	3A	58
4	Hours (12 Hour Mode)	1-12	$01-$0C (AM) and $81-$8C (PM)	$01-$12 (AM) and $81-$92 (PM)	05	05
	Hours (24 Hour Mode)	0-23	$00-$17	$00-$23	05	05
5	Hours Alarm (12 Hour Mode)	1-12	$01-$0C (AM) and $81-$8C (PM)	$01-$12 (AM) and $81-$92 (PM)	05	05
	Hours Alarm (24 Hour Mode)	0-23	$00-$17	$00-23	05	05
6	Day of the Week Sunday = 1	1-7	$01-$07	$01-$07	05	05
7	Date of the Month	1-31	$01-$1F	$01-$31	0F	15
8	Month	1-12	$01-$0C	$01-$12	02	02
9	Year	0-99	$00-$63	$00-$99	4F	79

* Example: 5:58:21 Thursday 15 February 1979 (time is AM)

Static CMOS RAM

The 50 general purpose RAM bytes are not dedicated within the CDP6818A. They can be used by the processor program, and are fully available during the update cycle.

When time and calendar information must use battery back-up very frequently there is other non-volatile data that must be retained when main power is removed. The 50 user RAM bytes serve the need for low-power CMOS battery-backed storage, and extend the RAM available to the program.

When further CMOS RAM is needed, additional CDP6818As may be included in the system. The time/calendar functions may be disabled by holding the DV0-DV2 dividers, in Register A, in the reset state by setting the SET bit in Register B or by removing the oscillator. Holding the dividers in reset prevents interrupts or SQW output from operating while setting the SET bit allows these functions to occur. With the dividers clear, the available user RAM is extended to 59 bytes. The high-order bit of the seconds byte, bit 7 or Register A, and all bits of Register C and D cannot effectively be used as general purpose RAM.

Interrupts

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from once-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517 μs. The update-ended interrupt may be used to indicate to the program that an update cycle is completed. Each of these independent interrupt conditions are described in greater detail in other sections.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a "1" to a interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in the interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the $\overline{IRQ}$ pin is immediately activiated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, a flag bit is set to a "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The "interrupt" flag bit becomes a status bit, which the software interrogates, when it wishes. When the software detects that the flag is set, it is an indication to software that the "interrupt" event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C so the bits which are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held after the read cycle. One, two or three flag bits may be found to be set when Register C is used. The program should inspect all utilized flag bits every time Register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt-flag bit is set and the corresponding interrupt-enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enables bits both set. The IRQF bit in Register C is a "1" whenever the $\overline{IRQ}$ pin is being driven low.

The processor program can determine that the RTC initiated the interrupt by reading Register C. A "1" in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the part. The act of reading Register C clears all the then-active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt-mask bits set and service each interrupt which is set. Again, more than one interrupt-flag bit may be set.

Divider Stages

The CDP6818A has 22 binary-divider stages following the time base as shown in Figure 1. The output of the dividers is a 1 Hz signal to the update-cycle logic. The dividers are controlled by three divider bits (DV2, DV1, and DV0) in Register A.

Divider Control

The divider-control bits have three uses, as shown in Table 4. Three usable operating time bases may be selected (4.194304 MHz, 1.048576 MHz, or 32.768 kHz). The divider chain may be held at reset, which allows precision setting of the time, when the divider is changed from reset to an operating time base, the first update cycle is one-half second later. The divider-control bits are also used to facilitate testing the CDP6818A.

Square-Wave Output Selection

Fifteen of the 22 divider taps are made available to a 1-of-15 selector as shown in Figure 1. The first purpose of selecting a divider tap is to generate a square-wave output signal at the SQW pin. The RS0-RS3 bits in Register A establish the square-wave frequency as listed in Table 5. The SQW frequency selection shares the 1-of-15 selector with periodic interrupts.

Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square-wave output selection bits, or the SQWE output-enable bit may generate an asymmetrical waveform at the time of execution. The square-wave output pin has a number of potential uses. For example, it can serve as a frequency standard for external use, a frequency synthesizer, or could be used to generate one or more audio tones under program control.

Periodic Interrupt Selection

The periodic interrupt allows the $\overline{IRQ}$ pin to be triggered from once every 500 ms to once every 30.517 µs. The periodic interrupt is separate from the alarm interrupt which may be output from once per second to once per day.

Table 5 shows that the periodic interrupt rate is selected with the same Register A bits which select the square-wave frequency. Changing one also changes the other. But each function may be separately enabled so that a program could switch between the two features or use both. The SQW pin is enabled by the SQWE bit in Register B. Similarly the periodic interrupt is enabled by the PIE bit in Register B.

Periodic interrupt is usable by practically all real-time systems. It can be used to scan for all forms of inputs from contact closures to serial receive bits or bytes. It can be used in multiplexing displays or with software counters to measure inputs, create output intervals, or await the next needed software function.

Update Cycle

The CDP6818A executes an update cycle once per second, assuming one of the proper time bases is in place, the DV0-DV2 divider is not clear, and the SET bit in Register B is clear. The SET bit in the "1" state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the second byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 4.194304 MHz or 1.048576 MHz time base the update cycle takes 248 µs while a 32.768 kHz time base update cycle takes 1984 µs. During the update cycle, the time, calendar, and alarm bytes are not accessible by the processor program. The CDP6818A protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete, the output will be undefined. The update in progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating nonavailability during update are usable by the program. In discussing the three methods, it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. During this time a display could be updated or the information could be transferred to continuously available RAM. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once per second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes high, the update cycle begins 244 µs later. Therefore, if a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. If a "1" is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to reach valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 15). Periodic interrupts that occur at a rate of greater than t_{BUC} + t_{UC} allow valid time and date information to be read at each occurrence of the periodic interrupt. The reads should be completed within (T_{PI} ÷ 2) + t_{BUC} to ensure that data is not read during the update cycle.

To properly setup the internal counters for daylight savings time operation, the user must set the time at least two seconds before the rollover will occur. Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

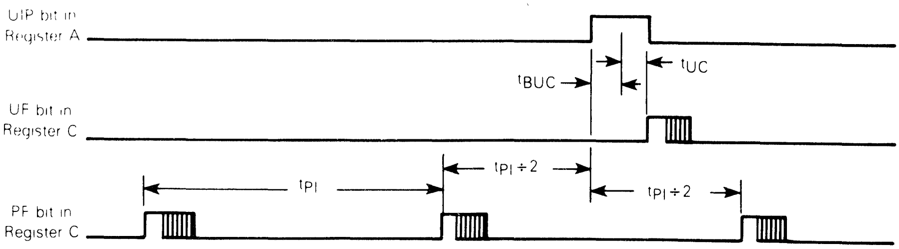
TABLE 4 - DIVIDER CONFIGURATIONS

TIME-BASE FREQUENCY	DIVIDER BITS REGISTER A			OPERATION MODE	DIVIDER RESET	BYPASS FIRST N-DIVIDER BITS
	DV2	DV1	DV0			
4.194304 MHz	0	0	0	Yes	—	N = 0
1.048576 MHz	0	0	1	Yes	—	N = 2
32.768 kHz	0	1	0	Yes	—	N = 7
Any	1	1	0	No	Yes	—
Any	1	1	1	No	Yes	—

Note: Other combinations of divider bits are used for test purposes only.

TABLE 5 - PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY

SELECT BITS REGISTER A				4.194304 or 1.048576 MHz TIME BASE		32.768 kHz TIME BASE	
RS3	RS2	RS1	RS0	PERIODIC INTERRUPT RATE t_{PI}	SQW OUTPUT FREQUENCY	PERIODIC INTERRUPT RATE t_{PI}	SQW OUTPUT FREQUENCY
0	0	0	0	None	None	None	None
0	0	0	1	30.517 µs	32.768 kHz	3.90625 ms	256 Hz
0	0	1	0	61.035 µs	16.384 kHz	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz	244.141 µs	4.096 kHz
0	1	0	1	488.281 µs	2.048 kHz	488.281 µs	2.048 kHz
0	1	1	0	976.562 µs	1.024 kHz	976.562 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz	500 ms	2 Hz



t_{PI} = Periodic Interrupt Time Interval (500 ms, 250 ms, 125 ms, 62.5 ms, etc per Table 5)
t_{UC} = Update Cycle Time (248 µs or 1984 µs)
t_{BUC} = Delay Time Before Update Cycle (244 µs)

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Fig. 15 - Update-ended and periodic interrupt relationship.

REGISTERS

The CDP6818A has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

REGISTER A ($0A)

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

Read/Write Register except UIP

UIP

The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1", the update cycle is in progress or will soon begin. When UIP is a "0", the update cycle is not in progress and will not be for at least 244 µs (for all time bases). This is detailed in Table 6. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero — it is not in transition. The UIP bit is read-only bit, and is not affected by Reset. Writing the SET bit in Register B to a "1" inhibits any update cycle and then clears the UIP status bit.

TABLE 6 - UPDATE CYCLE TIMES

UIP BIT	TIME BASE (OSC1)	UPDATE CYCLE TIME (t_{UC})	MINIMUM TIME BEFORE UPDATE CYCLE (t_{BUC})
1	4.194304 MHz	248 µs	—
1	1.048576 MHz	248 µs	—
1	32.768 kHz	1984 µs	—
0	4.194304 MHz	—	244 µs
0	1.048576 MHz	—	244 µs
0	32.768 kHz	—	244 µs

DV2, DV1, DV0

Three bits are used to permit the program to select various conditions of the 22-stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use. Table 4 shows that time bases of 4.194304 MHz, 1.048576 MHz, and 32.768 kHz may be used. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider at the precise time stored in the RAM. When the divider reset is removed, the first update cycle begins one-half second later. These three read/write bits are not affected by $\overline{\text{RESET}}$.

RS3, RS2, RS1, RS0

The four rate selection bits select one of 15 tapes on the 22-stage divider, or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The program may do one of the following: 1) enable the interrupt with the PIE bit, 2) enable the SQW output pin with the SQWE bit, 3) enable both at the same time at the same rate, or 4) enable neither Table 5 lists the periodic interrupt rates and the square-wave frequencies that may be chosen with the RS bits. These four bits are read/write bits which are not affected by $\overline{\text{RESET}}$.

REGISTER B ($0B)

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

Read/Write Register

SET

When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initalize the time and calendar bytes without an update occurring in the midst of initalizing. SET is a read/write bit which is not modified by $\overline{\text{RESET}}$ or internal functions of the CDP6818A.

PIE

The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit in Register C to cause the $\overline{\text{IRQ}}$ pin to be driven low. A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Register A. A zero in PIE blocks $\overline{\text{IRQ}}$ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by an internal CDP6818A functions, but is cleared to "0" by a $\overline{\text{RESET}}$.

AIE

The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) bit in Register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three times bytes equal the three alarm bytes (including a "don't care" alarm code by binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to "0". The internal functions do not affect the AIE bit.

UIE

The UIE (update-ended interrupt enable) bit is a read/write bit which enables the update-end flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears the UIE bit.

SQWE

When the square-wave enable (SQWE) bit is set to a "1" by the program, a square-wave signal at the frequency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a zero the SQW pin is held low. The state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. SQWE is a read/write bit.

DM

The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or $\overline{\text{RESET}}$. A "1" in DM signifies binary data, while a "0" in DM specifies binary-coded-decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a "0"). This is a read/write bit, which is affected only by software.

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DSE

The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1"). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or reset.

REGISTER C ($0C)

MSB … LSB

b7	b6	b5	b4	b3	b2	b1	b0	Read-Only Register
IRQF	PF	AF	UF	0	0	0	0	

IRQF

The interrupt request flag (IRQF) is set to a "1" when one or more of the following are true:

PF=PIE="1"
AF=AIE="1"
UF=UIE="1"
i.e., IRQF = PF•PIE+AF•AIE+UF•UIE

Any time the IRQF bit is a "1", the $\overline{\text{IRQ}}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{\text{RESET}}$ pin is low.

PF

The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an $\overline{\text{IRQ}}$ signal and sets the IRQF bit when PIE is also a "1". The PF bit is cleared by a $\overline{\text{RESET}}$ or a software read of Register C.

AF

A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the $\overline{\text{IRQ}}$ pin to go low, and a "1" to appear in the IRQF bit, when the AIE bit also is a "1". A $\overline{\text{RESET}}$ or a read of Register C clears AF.

UF

The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting $\overline{\text{IRQ}}$. UF is cleared by a Register C read or a $\overline{\text{RESET}}$.

b3 to b0

The unused bits of Status Register 1 are read as "0's". They can not be written.

REGISTER D ($0D)

MSB … LSB

b7	b6	b5	b4	b3	b2	b1	b0	Read-Only Register
VRT	0	0	0	0	0	0	0	

VRT

The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power-sense pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read only bit which is not modified by the $\overline{\text{RESET}}$ pin. The VRT bit can only be set by reading Register D.

b6 to b0

The remaining bits of Register D are unused. They cannot be written, but are always read as "0's."

TYPICAL INTERFACING

The CDP6818A is best suited for use with microprocessors which generate an address-then-data multiplexed bus. Figures 16 and 17 show typical interfaces to bus-compatible processors. These interfaces assume that the address decoding can be done quickly. However, if standard metalgate CMOS gates are used, the $\overline{\text{CS}}$ setup time may be violated. Figure 18 illustrates an alternative method of chip selection which will accommodate such slower decoding.

The CDP6818A can be interfaced to single-chip microcomputers (MCU) by using eleven port lines as shown in Figure 19. Non-multiplexed bus microprocessors can be interfaced with additional support.

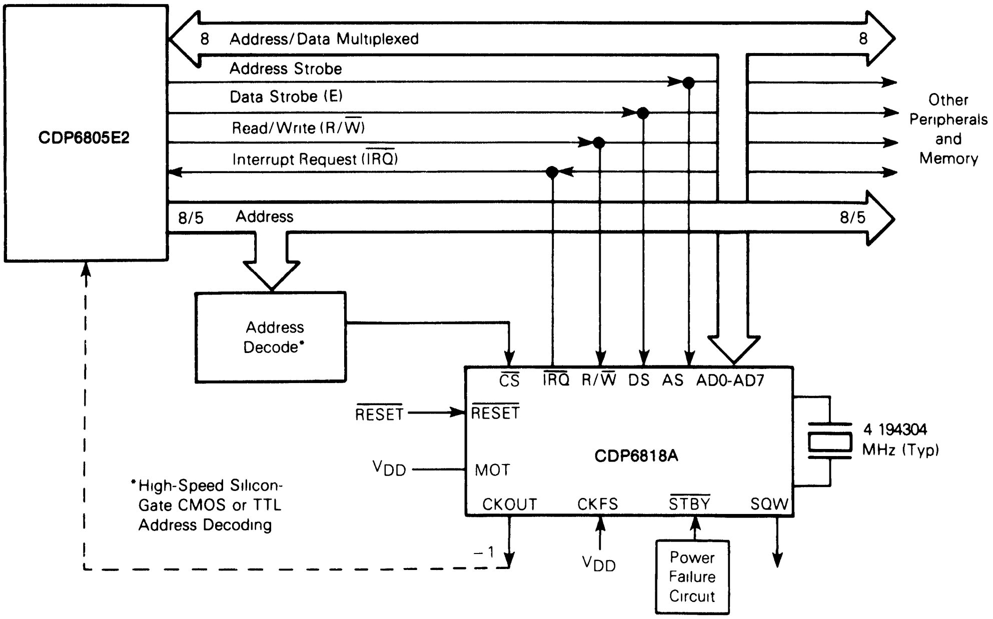
There is one method of using the multiplexed bus CDP6818A with non-multiplexed bus processors. The interface uses available bus control signals to multiplex the address and data bus together.

An example using either the MC6800, MC6802, MC6808, or MC6809 microprocessor is shown in Figure 20. When the CDP6818A is I/O mapped as shown in Figure 19 and 20, the AS and DS inputs should be left in a low state when the part is not being accessed. Refer to the $\overline{\text{STBY}}$ pin description for the conditions which must be met before $\overline{\text{STBY}}$ can be recognized.

Figure 21 illustrates the subroutines which may be used for data transfers in a non-multiplexed system. The subroutines should be entered with the registers containing the following data:

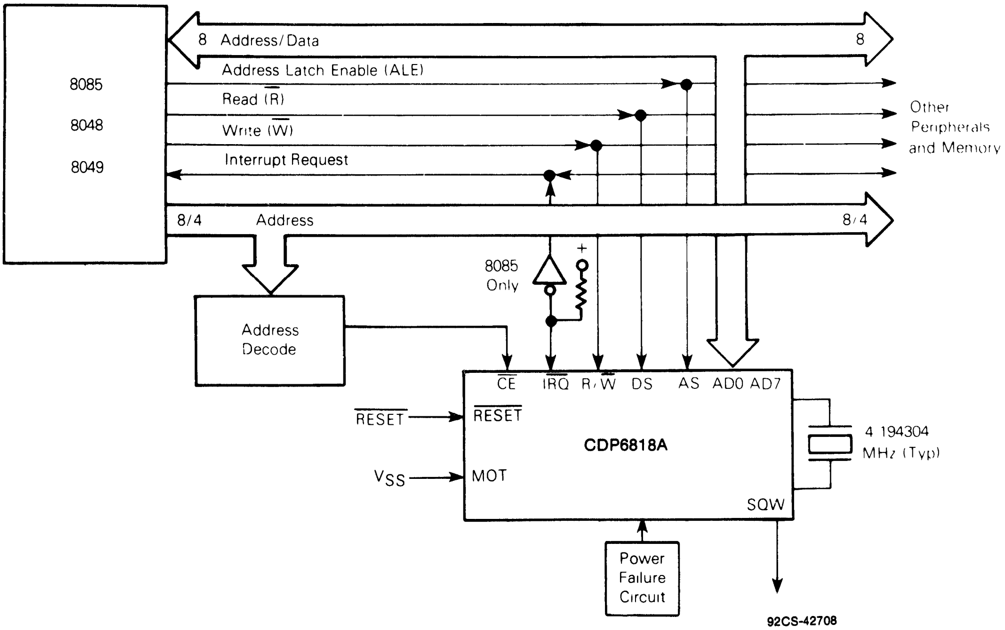
Accumulator A: The address of the RTC to be accessed.
Accumulator B: Write: The data to be written.
Read: The data read from the RTC.

The RTC is mapped to two consecutive memory locations — RTC and RTC + 1 as shown in Figure 20.



92CS-42707

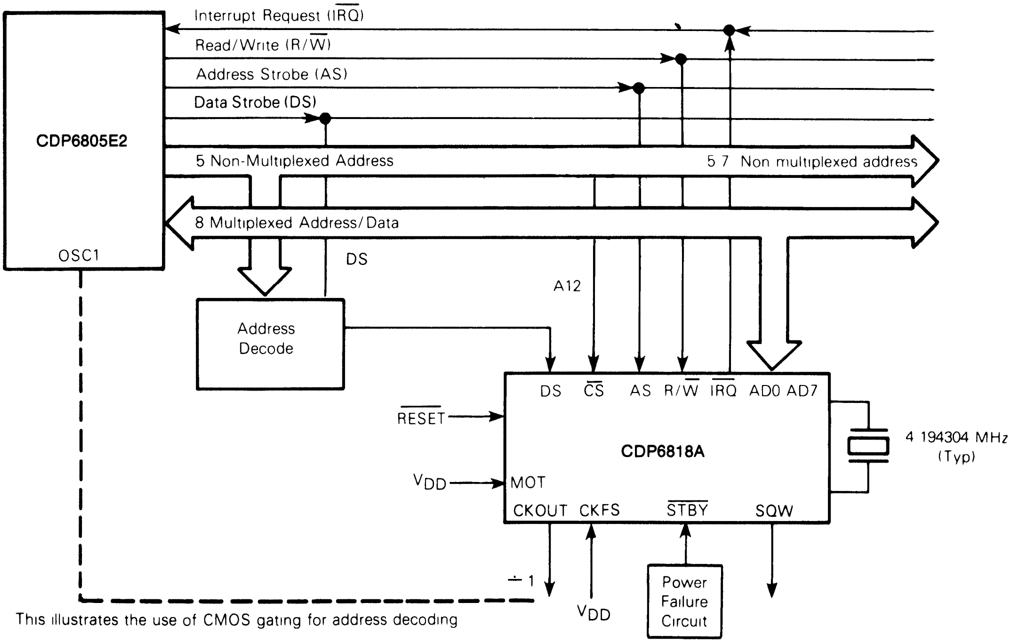
Fig. 16 - CDP6818A interfaced with Motorola compatible multiplexed bus microprocessors.



92CS-42708

Fig. 17 - CDP6818A interfaced with competitor compatible multiplexed bus microprocessors.

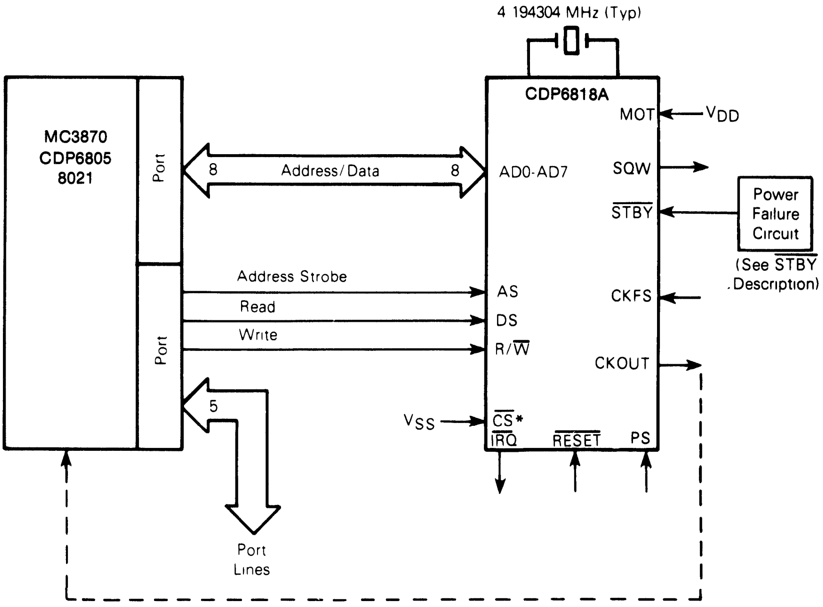
CDP6818A



This illustrates the use of CMOS gating for address decoding

92CS-42709

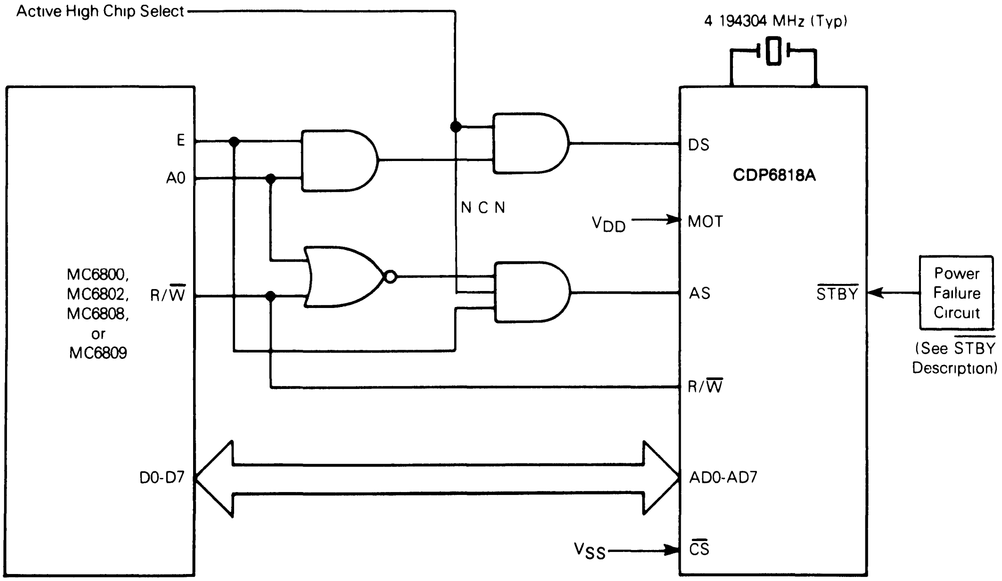
Fig. 18 - CDP6818A interfaced with CDP6805E2 CMOS multiplexed microprocessor with slow addressing decoding.



*NOTE CS can be controlled by a port pin (if available)

92CS-42710

Fig. 19 - CDP6818A interfaced with the ports of A typical single chip microcomputer.



92CS-42723

Fig. 20 - CDP6818A interfaced with Motorola Processors.

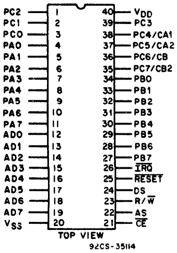
```
READ     STA     RTC       Generate AS and Latch Data from ACCA
         LDAB    RTC + 1   Generate DS and Get Data
         RTS

WRITE    STA     RTC       Generate AS and Latch Data from ACCA
         STAB    RTC + 1   Generate DS and Store Data
         RTS
```

Fig. 21 - Subroutine for reading and writing the CDP6818A with a non-multiplexed bus.

CDP6823

Advance Information

TERMINAL ASSIGNMENT



40-Lead Packages

CMOS Parallel Interface

Features:

- *24 individual programmed I/O pins*
- *MOTEL circuit for bus compatibility with many microprocessors*
- *Multiplexed bus compatible with: CDP6805E2 and competitive microprocessors*
- *Data direction registers for ports A, B, and C*
- *Reset input to clear interrupts and initialize internal registers*
- *Four port C I/O pins may be used as Control Lines for:*
  - *Four interruput inputs*
  - *Input byte latch*
  - *Output pulse*
  - *Handshake activity*
- *15 registers addressed as memory locations*
- *Handshake control logic for input and output peripheral operation*
- *Interrupt output pin*
- *3 volt to 5.5 volt operating V_{DD}*

The RCA-CDP6823 CMOS parallel interface (CPI) provides a universal means of interfacing external signals with the CDP6805E2 CMOS microprocessor and other multiplexed bus microprocessors. The unique MOTEL circuit on-chip allows direct interfacing to most industry CMOS microprocessors, as well as many NMOS MPUs.

The CDP6823 CPI includes three bidirectional 8-bit ports or 24 I/O pins. Each I/O line may be separately established as an input or an output under program control via data direction registers associated with each port. Using the bit change and test instructions of the CDP6805E2, each individual I/O pin can be separately accessed. All port registers are read/write bytes to accommodate read-modify-write instructions.

The CDP6823 is supplied in a 40-lead hermetic dual-in-line side-brazed ceramic package (D suffix), in a 40-lead dual-in-line plastic package (E suffix) and in a 44-lead plastic chip-carrier package (Q suffix).

The RCA-CDP6823 is equivalent to and is a direct replacement for the industry type MC146823.

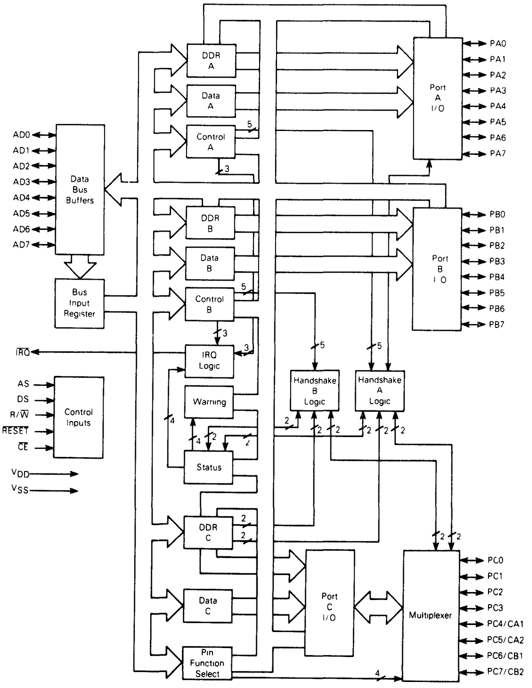
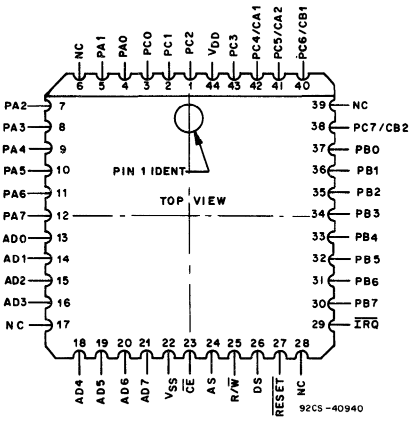


Fig. 1 - Functional block diagram.

TERMINAL ASSIGNMENT



44-Lead Plastic Chip-Carrier Package

File Number **1377**

MAXIMUM RATINGS (Voltages reference to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +8	V
All Input Voltages	V_{in}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Current Drain per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range	T_A	**-40 to +85**	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

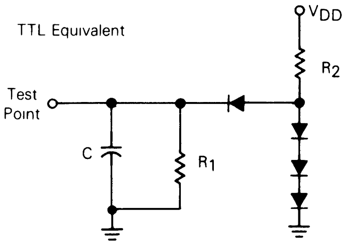
Characteristics	Symbol	Value	Unit
Thermal Resistance Ceramic Dual-In-Line Plastic Dual-In-Line Plastic Chip-Carrier	θ_{JA}	 50 100 70	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \geq (V_{in}$ or $V_{out}) \geq V_{DD}$. Leakage currents are reduced and reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5$ Vdc ±10%, $V_{SS}=0$ Vdc, $T_A=0°C$ to 70°C, unless otherwise noted)

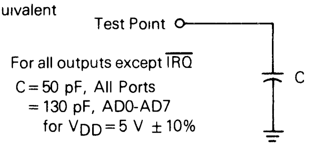
Parameter	Symbol	Min	Max	Unit
Output Voltage ($I_{Load} \leq 10$ µA)	V_{OL} V_{OH}	– $V_{DD}-0.1$	0.1 –	V V
Output High Voltage ($I_{Load}=-1.6$ mA) AD0-AD7 ($I_{Load}=-0.2$ mA) PA0-PA7, PC0-PC7 ($I_{Load}=-0.36$ mA) PB0-PB7	 V_{OH} V_{OH} V_{OH}	 4.1 4.1 4.1	 V_{DD} V_{DD} V_{DD}	V
Output Low Voltage ($I_{Load}=1.6$ mA) AD0-AD7, PB0-PB7 ($I_{Load}=0.8$ mA) PA0-PA7, PC0-PC7 ($I_{Load}=1$ mA) $\overline{IRQ}$	 V_{OL} V_{OL} V_{OL}	 V_{SS} V_{SS} V_{SS}	 0.4 0.4 0.4	V
Input High Voltage, AD0-AD7, AS, DS, R/$\overline{W}$, $\overline{CE}$, PA0-PA7, PB0-PB7, PC0-PC7 $\overline{RESET}$	V_{IH} V_{IH}	$V_{DD}-2.0$ $V_{DD}-0.8$	V_{DD} V_{DD}	V
Input Low Voltage (All Inputs)	V_{IL}	V_{SS}	0.8	V
Quiescent Current — No dc Loads (All Ports Programmed as Inputs, All Inputs = $V_{DD}-0.2$ V)	I_{DD}	–	160	µA
Total Supply Current (All Ports Programmed as Inputs, CE = V_{IL}, $t_{cyc}=1$ µs)	I_{DD}	–	3	mA
Input Current, $\overline{CE}$, AS, R/$\overline{W}$, DS, $\overline{RESET}$	I_{in}	–	±1	µA
Hi-Z State Leakage, AD0-AD7, PA0-PA7, PB0-PB7, PC0-PC7	I_{TSL}	–	±10	µA

TTL Equivalent

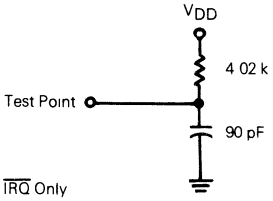


Pin	R1	R2	C
AD0-AD7	2.55k	2 k	130 pF
PA0-PA7, PC0-PC7	20k	4.32k	50 pF
PB0-PB7	11.5k	2.1k	50 pF

CMOS Equivalent



For all outputs except $\overline{IRQ}$
C = 50 pF, All Ports
= 130 pF, AD0-AD7
for $V_{DD}=5$ V ±10%



$\overline{IRQ}$ Only

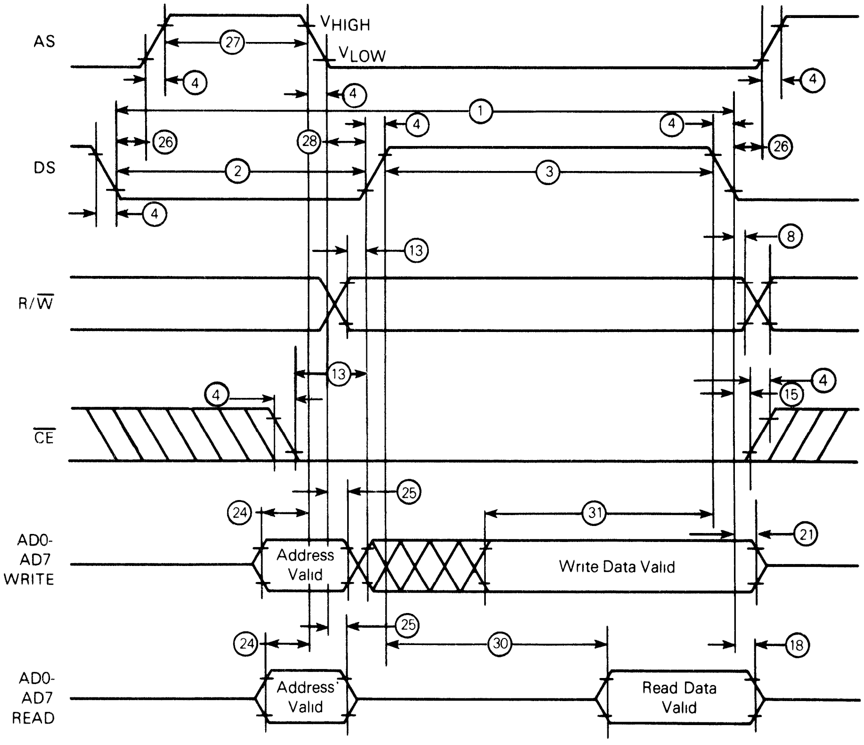
Fig. 2 - Equivalent test loads.

CDP6823

BUS TIMING (V_{DD} = 5 Vdc ±10%, V_{SS} = 0 Vdc, T_A = 0° to 70°C, unless otherwise noted)

Ident. Number	Characteristics	Symbol	Min	Max	Unit
1	Cycle Time	t_{cyc}	1000	dc	ns
2	Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High	PW_{EL}	300	–	ns
3	Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low	PW_{EH}	325	–	ns
4	Input Rise and Fall Time	t_r, t_f	–	30	ns
8	R/$\overline{W}$ Hold Time	t_{RWH}	10	–	ns
13	R/$\overline{W}$ and $\overline{CE}$ Setup Time Before DS/E	t_{RWS}	25	–	ns
15	Chip Enable Hold Time	t_{CH}	0	–	ns
18	Read Data Hold Time	t_{DHR}	10	100	ns
21	Write Data Hold Time	t_{DHW}	0	–	ns
24	Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	25	–	ns
25	Muxed Address Hold Time	t_{AHL}	20	–	ns
26	Delay Time DS/E to AS/ALE Rise	t_{ASD}	60	–	ns
27	Pulse Width, AS/ALE High	PW_{ASH}	170	–	ns
28	Delay Time, AS/ALE to DS/E Rise	t_{ASED}	60	–	ns
30	Peripheral Output Data Delay Time from DS/E or $\overline{RD}$	t_{DDR}	20	240	ns
31	Peripheral Data Setup Time	t_{DSW}	220	–	ns

NOTE Designations E, ALE, $\overline{RD}$, and $\overline{WR}$ refer to signals from alternative microprocessor signals



NOTE $V_{HIGH} = V_{DD} - 2$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5$ V ±10%

Fig. 3 - Bus timing diagram.

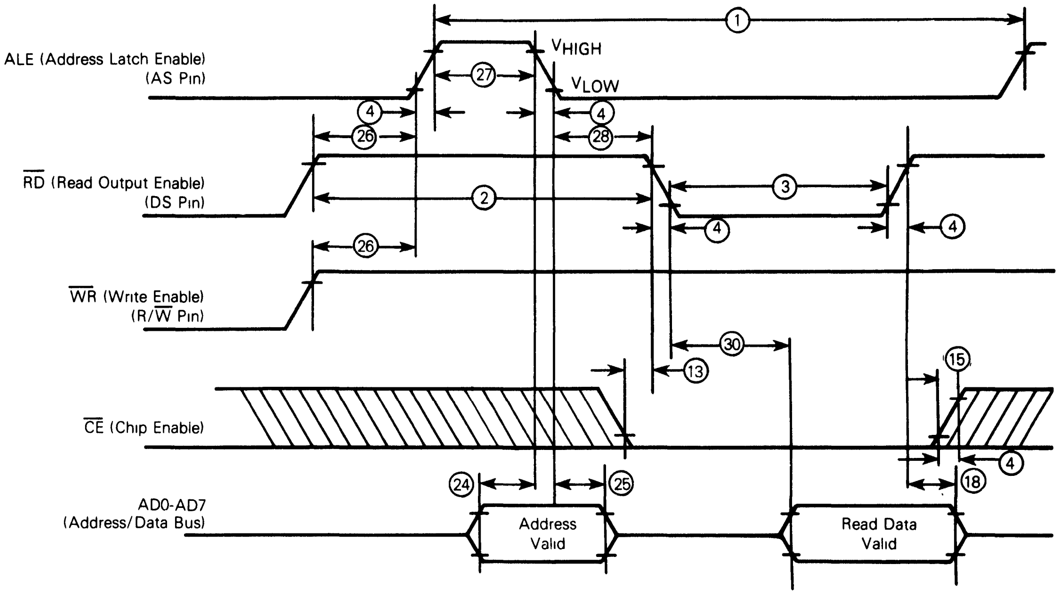
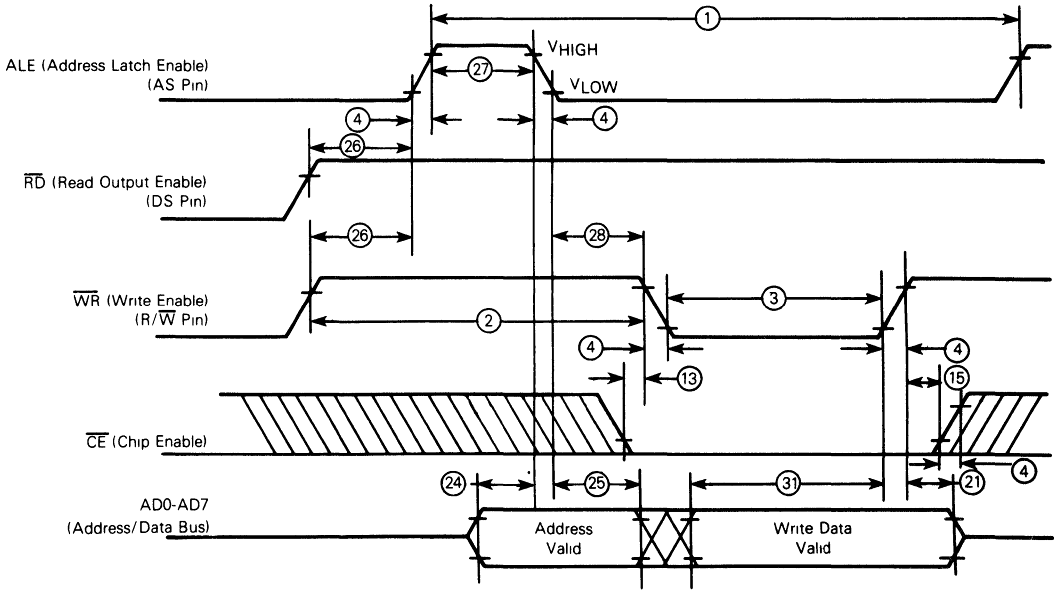


Fig. 4 - Bus READ timing competitor multiplexed bus.



NOTE $V_{HIGH} = V_{DD} - 2$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5$ V ± 10%

Fig. 5 - Bus WRITE timing competitor multiplexed bus.

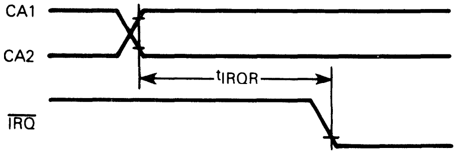
CDP6823

CONTROL TIMING (V_{DD}=5 Vdc ±10%, V_{SS}=0 Vdc, T_A=0°C to 70°C)

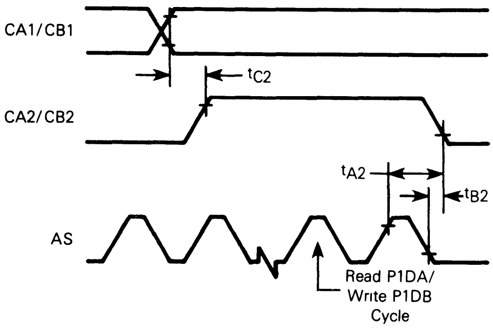
Parameter	Symbol	Min	Max	Unit
Interrupt Response (Input Modes 1 and 3)	t_{IRQR}	TBD	–	μs
Delay, CA1 (CB1) Active Transition to CA2 (CB2) High (Output Mode 0)	t_{C2}	TBD	–	μs
Delay, CA2 Transition from Positive Edge of AS (Output Modes 0 and 1)	t_{A2}	TBD	–	μs
Delay, CB2 Transition from Negative Edge of AS (Output Modes 0 and 1)	t_{B2}	TBD	–	μs
CA2/CB2 Pulse Width (Output Mode 1)	t_{PW}	TBD	TBD	ns
Delay, V_{DD} Rise to $\overline{RESET}$ High	t_{RLH}	TBD	–	μs
Pulse Width, $\overline{RESET}$	t_{RW}	TBD	–	ns

TBD = To be determined

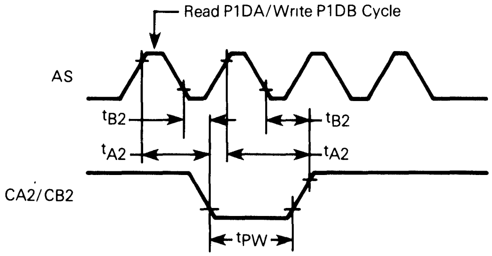
$\overline{IRQ}$ RESPONSE (INPUT MODES 1 AND 3)



CA2/CB2 DELAY (OUTPUT MODE 0)



CA2/CB2 DELAY (OUTPUT MODE 1)



$\overline{RESET}$

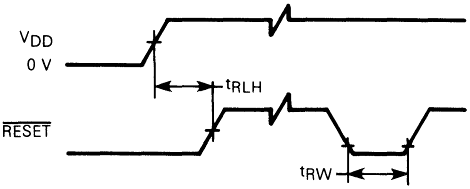


Fig. 6 - Control timing diagrams.

GENERAL DESCRIPTION

The CDP6823, CMOS parallel interface (CPI), contains 24 individual bidirectional I/O lines configured in three 8-bit ports. The 15 internal registers, which control the mode of operation and contain the status of the port pins, are accessed via an 8-bit multiplexed address/data bus. The lower four address bits (AD0-AD3) of the multiplexed address bus determine which register is to be accessed (see Register Address Map shown below). The four address bits (AD4, AD5, AD6, and AD7) must be separately decoded to position this memory map within each 256-byte address space available via the 8-bit multiplexed address bus. For more detailed information, refer to **REGISTER DESCRIPTION**.

REGISTER ADDRESS MAP

0	Port A Data, Clear CA1 Interrupt	P1DA
1	Port A Data, Clear CA2 Interrupt	P2DA
2	Port A Data	PDA
3	Port B Data	PDB
4	Port C Data	PDC
5	Not Used	–
6	Data Direction Register for Port A	DDRA
7	Data Direction Register for Port B	DDRB
8	Data Direction Register for Port C	DDRC
9	Control Register for Port A	CRA
A	Control Register for Port B	CRB
B	Pin Function Select Register for Port C	FSR
C	Port B Data, Clear CB1 Interrupt	P1DB
D	Port B Data, Clear CB2 Interrupt	P2DB
E	Handshake/Interrupt Status Register	HSR
F	Handshake Over-Run Warning Register	HWR

The CPI is implemented with the MOTEL circuit which allows direct interface with either of the two major multiplexed microprocessor bus types. A detailed description of the MOTEL circuit is provided in the **MOTEL** section.

Three data direction registers (DDRs), one for each port, determine which pins are outputs and which are inputs. A logic zero on a DDR bit configures its associated pin as an input; and a logic one configures the pin as an output. Upon reset, the DDRs are cleared to logic zero to configure all port pins as inputs.

Actual port data may be read or written via the port data registers (PDA, PDB, and PDC). Ports A and B each have two additional data registers (P1DA and P2DA - P1DB and P2DB) which are used to clear the associated handshake/interrupt status register bits (HSA1 and HSA2 - HSB1 and HSB2), respectively. Port A may also be configured as an 8-bit latch when used with CA1. Reset has no effect on the contents of the port data registers. Users are advised to initialize the port data registers before changing any port pin to an output.

Four pins on port C (PC4/CA1, PC5/CA2, PC6/CB1, and PC7/CB2) may additionally be programmed as handshake lines for ports A and B via the port C function select register (FSR). Both ports A and B have one input-only line and one bidirectional handshake line each associated with them. The handshake lines may be programmed to perform a variety of tasks such as interrupt requests, setting flags, latching data, and data transfer requests and/or acknowledgments. The handshake functions are programmed via control registers A and B (CRA and CRB). Additional information may be found in **PIN DESCRIPTIONS, REGISTER DESCRIPTION,** or **HANDSHAKE OPERATION**.

MOTEL

The MOTEL circuit is a concept that permits the CDP6823 to be directly interfaced with different types of multiplexed bus microprocessors without any additional external logic. For a more detailed description of the multiplexed bus, see **MULTIPLEXED BIDIRECTIONAL ADDRESS/DATA BUS (AD0-AD7)**. Most multiplexed microprocessors use one of two synchronous buses to interface peripherals. An industry standard bus structure is now available.

The MOTEL circuit is built into peripheral and memory ICs to permit direct connection to either type of bus. The MOTEL concept is shown logically in Fig. 7.

The microprocessor type is automatically selected by the MOTEL circuit through latching the state of the DS/$\overline{\text{RD}}$ pin with AS/ALE. Since DS is always low during AS and $\overline{\text{RD}}$ is always high during ALE, the latch automatically indicates with which type microprocessor bus it is interfaced.

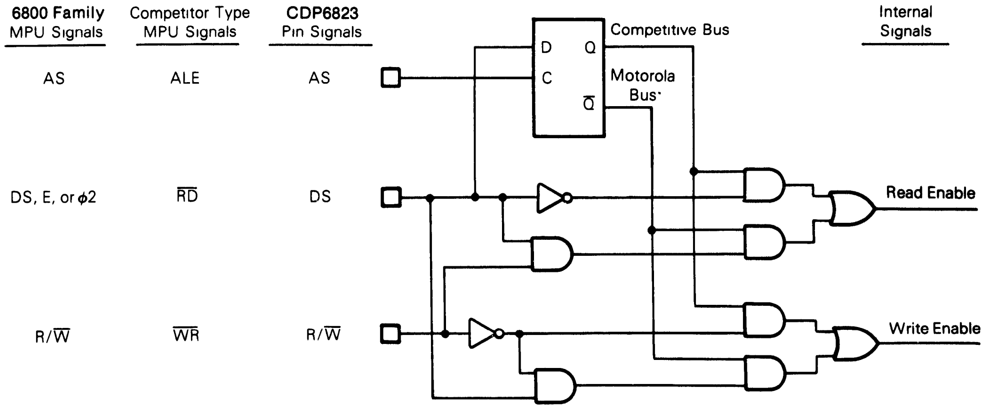


Fig. 7 - Functional diagram of MOTEL circuit.

PIN DESCRIPTION

The following paragraphs contain a brief description of the input and output pins. References (if applicable) are given to other paragraphs that contain more detail about the function being performed.

Multiplexed Bidirectional Address/Data Bus (AD0-AD7)

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion of the bus cycle for data. Address-then-data multiplexing does not slow the access time of the CDP6823 since the bus reversal from address to data is occurring during the internal register access time.

The address must be valid t_{ASL} prior to the fall of AS/ALE at which time the CDP6823 latches the address present on the AD0-AD3 pins. Valid write data must be presented and held stable during the latter portion of the DS or $\overline{\mathrm{WR}}$ pulses, In a read cycle, the CDP6823 outputs eight bits of data during the latter portion of the DS or $\overline{\mathrm{RD}}$ pulses, then ceases driving the bus (returns the output drivers to high impedance) t_{DHR} hold time after DS falls in this case of MOTEL or $\overline{\mathrm{RD}}$ rises in the other case.

Address Strobe (AS)

The address strobe input pulse serves to demultiplex the bus. The falling edge of AS or ALE causes the addresses AD0-AD3 to be latched within the CDP6823. The automatic MOTEL circuit in the CDP6823 also latches the state of the DS pin with the falling edge of AS or ALE.

Data Strobe or Read (DS)

The DS input pin has two interpretations via the MOTEL circuit. When generated by a Motorola microprocessor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), or $\phi 2$ ($\phi 2$ clock). During read cycles, DS or $\overline{\mathrm{RD}}$ signifies the time that the CPI is to drive the bidirectional bus. In write cycles, the trailing edge of DS or rising edge of $\overline{\mathrm{WR}}$ causes the parallel interface to latch the written data present on the bidirectional bus.

The second MOTEL interpretation of DS is that of $\overline{\mathrm{RD}}$, $\overline{\mathrm{MEMR}}$, or $\overline{\mathrm{I/OR}}$ originating from a competitor-type micro processor. In this case, DS identifies the time period when the parallel interface drives the bus with read data. This interpretation of DS is also the same as an output-enable signal on a typical memory.

The MOTEL circuit, within the CDP6823, latches the state of the DS pin on the falling edge of AS/ALE. When the mode of MOTEL is desired DS must be low during AS/ALE, which is the case with the multiplexed bus microprocessors. To insure the competitor mode of MOTEL, the DS pin must remain high during the time AS/ALE is high.

Read/Write (R/$\overline{\mathrm{W}}$)

The MOTEL circuit treats the R/$\overline{\mathrm{W}}$ input pin in one of two ways. The microprocessor is connected, R/$\overline{\mathrm{W}}$ is a level which indicates whether the current cycle is a read or write A read cycle is indicated with a high level on R/$\overline{\mathrm{W}}$ while DS is high, whereas a write cycle is a low on R/$\overline{\mathrm{W}}$ while DS is high.

The second interpretation of R/$\overline{\mathrm{W}}$ is as a negative write pulse, $\overline{\mathrm{WR}}$, $\overline{\mathrm{MEMW}}$, and $\overline{\mathrm{I/OW}}$ from competitor-type micro processors. The MOTEL circuit in this mode gives the R/$\overline{\mathrm{W}}$ pin the same meaning as the write ($\overline{\mathrm{W}}$) pulse on many generic RAMs.

Chip Enable ($\overline{\mathrm{CE}}$)

The $\overline{\mathrm{CE}}$ input signal must be asserted (low) for the bus cycle in which the CDP6823 is to be accessed. $\overline{\mathrm{CE}}$ is not latched and must be stable prior to and during DS (in the 6805 mode of MOTEL) and prior to and during $\overline{\mathrm{RD}}$ and $\overline{\mathrm{WR}}$ (in the competitor mode of MOTEL). Bus cycles which take place without asserting $\overline{\mathrm{CE}}$ cause no actions to take place within the CDP6823. When $\overline{\mathrm{CE}}$ is high, the multiplexed bus output is in a high-impedance state.

When $\overline{\mathrm{CE}}$ is high, all data, DS, and R/$\overline{\mathrm{W}}$ inputs from the microprocessor are disconnected within the CDP6823. This permits the CDP6823 to be isolated from a powered-down microprocessor.

Reset ($\overline{\mathrm{RESET}}$)

The $\overline{\mathrm{RESET}}$ input pin is an active-low line that is used to restore all register bits, except the port data register bits, to logical zeros. After reset, all port lines are configured as inputs and no interrupt or handshake lines are enabled.

Interrupt Request ($\overline{\mathrm{IRQ}}$)

The $\overline{\mathrm{IRQ}}$ output line is an open-drain active-low signal that may be used to interrupt the microprocessor with a service request. The "open-drain" output allows this and other interrupt request lines to be wire ORed with a pullup resistor. The $\overline{\mathrm{IRQ}}$ line is low when bit 7 of the status register is high. Bit 7 (IRQF) of the handshake/interrupt status register (HSR) is set if any enabled handshake transition occurs; and its associated control register bit is set to allow interrupts. Refer to **INTERRUPT DESCRIPTION** or **HANDSHAKE OPERATION** for additional information.

Port A, Bidirectional I/O Lines (PA0-PA7)

Each line of port A, PA0-PA7, is individually programmable as either an input or output via its data direction register (DDRA). An I/O pin is an input when its corresponding DDR bit is a logic zero and an output when the DDR bit is a logic one. See Fig. 8 for typical I/O circuitry and Table 1 for I/O operation.

TABLE 1 — PORT DATA REGISTER ACCESSES (ALL PORTS)

R/$\overline{\mathrm{W}}$	DDR Bit	Results
0	0	The I/O pin is in input mode Data is written into the output data latch
0	1	Data is written into the output data latch and output to the I/O pin
1	0	The state of the I/O pin is read
1	1	The I/O pin is in an output mode The output data latch is read

There are three data registers associated with port A: PDA, P1DA, and P2DA. P1DA and P2DA are accessed when certain handshake activity is desired. See **HANDSHAKE OPERATION** for more information.

Data written to the port A data register, PDA, is latched into the port A output latch regardless of the state of the DDRA. Data written to P1DA or P2DA is ignored and has no affect upon the output data latch or the I/O lines. An MPU read of port bits programmed as outputs reflect the last value written to the PDA register. Port A pins programmed as inputs may be latched via the handshake line PC4/CA1 (see

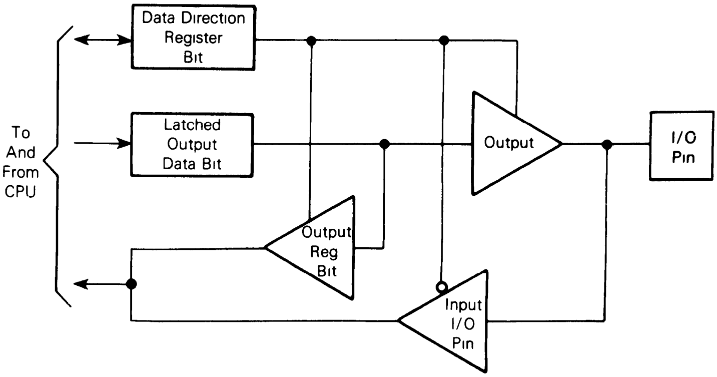


Fig. 8 - Typical port I/O circuitry.

HANDSHAKE OPERATION) and latched input data may be read via any of the three port A data registers. If the port A input latch feature is not enabled, an MPU read of any port A data register reflects the current status of the port A input pins if the corresponding DDRA bits equal zero. Reset has no effect upon the contents of the port A data register; however, all pins will be placed in the input mode (all DDRA bits forced to equal zero) and all handshake lines will be disabled.

Port B Bidirectional I/O Lines (PB0-PB7)
Each line of port B, PB0-PB7, is individually programmable as either an input or an output via its data direction register (DDRB). An I/O pin is an input when its corresponding DDR bit is a logic zero and an output when the DDR bit is a logic one.

There are three data registers associated with port B: PDB, P1DB, and P2DB. PDB is used for simple port B data reads and writes. P1DB and P2DB are accessed when certain handshake activity is desired. See **HANDSHAKE OPERATION** for more information.

Data written to PDB or P1DB data register is latched into the port B output latch regardless of the state of the DDRB. An MPU read of port bits programmed as outputs reflect the last value written to a port B data register. An MPU read of any port B register reflects the current status of the input pins whose DDRB bits equal zero. Reset has no effect upon the contents of the port B data register; however, all pins will be placed in the input mode (all DDRB bits forced to equal zero) and all handshake lines will be disabled.

Port C, Bidirectional I/O Lines (PC0-PC3)
Each line of port C, PC0-PC3, is individually programmable as either an input or an output via its data direction register (DDRC). An I/O pin is an input when its corresponding DDR bit is a logic zero and an output when the DDR bit is a logic one. Port C data register (PDC) is used for simple port C data reads and writes.

Data written into PDC is latched into the port C data latch regardless of the state of the DDRC. An MPU read of port C bits programmed as outputs reflect the last value written to the PDC register. An MPU read of the port C register reflects the current status of the corresponding input pins whose DDRC bits equal zero. Reset has no effect upon the contents of the port C data register; however, all pins will be placed in the input mode (all DDRC bits forced to equal zero) and all handshake lines will be disabled.

Port C Bidirectional I/O Line or Port A Input Handshake Line (PC4/CA1)
This line may be programmed as either a simple port C I/O line or as a handshake line for port A via the port C function select register (FSR). If programmed as a port C I/O pin, PC4/CA1 performs as described in the PC0-PC3 pin description. If programmed as a port A handshake line, PC4/CA1 performs as described in **HANDSHAKE OPERATION**.

Port C Bidirectional I/O Line or Port A Bidirectional Handshake Line (PC5/CA2)
This line may be programmed as either a simple port C I/O line or as a handshake line for port A via the port C function select register (FSR). If programmed as a port C I/O pin, PC5/CA2 performs as described in the PC0-PC3 pin description. If programmed as a port A handshake line, PC5/CA2 performs as described in **HANDSHAKE OPERATION**.

Port C Bidirectional I/O Line or Port B Input Handshake Line (PC6/CB1)
This line may be programmed as either a simple port C I/O line or as a handshake line for port B via the port C function select register (FSR). If programmed as a port C I/O pin, PC6/CB1 performs as described in the PC0-PC3 pin description. If programmed as a port B handshake line, PC6/CB1 performs as described in **HANDSHAKE OPERATION**.

Port C Bidirectional I/O Line or Port B Bidirectional Handshake Line (PC7/CB2)
This line may be programmed as either a simple port C I/O line or as a handshake line for port B via the port C function select register (FSR). If programmed as a port C I/O line, PC7/CB2 performs as described in the PC0-PC3 pin description. If programmed as a port B handshake line, PC7/CB2 performs as described in **HANDSHAKE OPERATION**.

HANDSHAKE OPERATION

Up to four port C pins can be configured as handshake lines for ports A and B (one input-only and one bidirectional line for each port) via the port C function select register (FSR). The direction of data flow for the two bidirectional handshake lines (CA2 and CB2) is determined by bits 5 and 7, respectively, of the port C data direction register (DDRC). Actual handshake operation is defined by the appropriate port control register (CRA or CRB).

The control registers allow each handshake line to be programmed to operate in one of four modes. CA2 and CB2 each have four input and four output modes. For detailed information, see Tables 2 and 3.

A summary of the handshake modes is given in the input and output sections that follow. All handshake activity is disabled by reset.

Input

Handshake lines programmed as inputs operate in any of four different modes as defined by the control registers (see Table 2). A bit in the handshake/interrupt status register (HSR) is set to a logic one on an active transition of any handshake line programmed as an input. Modes 0 and 1 define a negative transition as active; modes 2 and 3 define a positive transition as active. If modes 1 or 3 are selected on any input handshake line then the active transition of that line results in the IRQF bit of the HSR being set to a logic one and causes the interrupt line ($\overline{\text{IRQ}}$) to go low. $\overline{\text{IRQ}}$ is released by clearing the HSR bits that are input handshake lines which have interrupts enabled.

If an active transition occurs while the associated HSR bit is set to a logic one, the corresponding bit in the handshake warning register (HWR) is set to a logic one indicating that service of at least one active transition was missed. An HWR bit is cleared to a logic zero by first accessing the appropriate port data register, to clear the appropriate HSR status bit, followed by a read of the HWR.

TABLE 2 — INPUT HANDSHAKE MODES

Mode	Control Register Bits*	Active Edge	Status Bit In HSR	$\overline{\text{IRQ}}$ Pin
0	00	– Edge	Set high on active edge	Disabled
1	01	– Edge	Set high on active edge	Goes low when corresponding status flag in HSR goes high
2	10	+ Edge	Set high on active edge	Disabled
3	11	+ Edge	Set high on active edge	Goes low when corresponding status flag in HSR goes high

* Cleared to logic zero on reset

TABLE 3 — OUTPUT HANDSHAKE LINES (CA2 AND CB2 ONLY)

Mode	Control Register CRA(B) Bits 3 and 4*	Handshake Line Set High	Handshake Line Cleared Low	Default Level
0	00	Handshake set high on active transition of CA1 input. Handshake set high on active transition of CB1 input.	Read of P1DA or a read of P2DA while HSA1 is cleared. Write of port B P1DB or write of P2DB while HSB1 is cleared.	High
1	01	High on the first positive (negative) transition of AS while CA2 (CB2) is low.	Low on the first positive (negative) transition on AS following a read (write) of port A(B) data registers P1DA(B) or P2DA(B).	High
2	10	Never	Always	Low
3	11	Always	Never	High

* Cleared to logic zero on reset

Input Latch
Port A input-only handshake line (PC4/CA1) can be programmed to function as a latch enable for port A input data via CA1 LE (bit 2 of CRA). If CA1 LE is programmed to a logic one, an active transition of PC4/CA1 will latch the current status of the port A input pins into all three port A data registers (PDA, P1DA, and P2DA). When CA1 LE is enabled, port A and PC4/CA1 function as an 8-bit transparent latch; that is, if the HSA1 bit in the HSR is a logic zero then a read of any port A register reflects the current state of the port A input pins and corresponding bits of the output data latch for port A output pins. If HSA1 is a logic one, a read of any port A data register reflects the state of the port A input pins when HSA1 was set and the corresponding bits of the port A output data latch for port A output pins.

Further transitions of PC4/CA1 result only in setting the HWA1 bit in the HWR and do not relatch data into the port A registers. Latched data is released only by clearing HSA1 in the HSR to a logic zero (HSA1 is cleared by reading P1DA).

Output
Each bidirectional handshake line programmed as an output by the DDRC operates in one of four modes as described in Table 3. Modes 2 and 3 force the output handshake line to reflect the state of bit 4 in the appropriate control register.

In modes 0 and 1, PC5/CA2 is forced low during the cycle following a read of P1DA or a read of P2DA while HSA1 is cleared. PC7/CB2 is forced low during the cycle following a write to P1DB or a write to P2DB while HSB1 is cleared. Because of these differences, port A is the preferred input port and port B is the preferred output port.

In mode 0, PC5/CA2 (PC7/CB2) is set high by an active transition of PC4/CA1 (PC6/CB1). In mode 1, PC5/CA2 (PC7/CB2) is set high in the cycle following the cycle in which PC5/CA2 (PC7/CB2) goes low. Mode 1 forces a low-going pulse on PC5/CA2 (PC7/CB2) following a read (write) of P1DA (P1DB) or P2DA (P2DB) that is approximately one cycle time wide.

When entering an output handshake mode for the first time after a reset, the handshake line outputs the default level as listed in Table 3.

INTERRUPT DESCRIPTION

The CDP6823 allows an MPU interrupt request ($\overline{IRQ}$ low) via the input handshake lines. The input handshake line, operating in modes 1 or 3 as defined by the control registers (CRA and CRB), causes $\overline{IRQ}$ to go low when IRQF (interrupt flag) in the HSR is set to a logic one. $\overline{IRQ}$ is released when IRQF is cleared. See **Handshake/Interrupt Status Register** under **REGISTER DESCRIPTION** for additional information.

REGISTER DESCRIPTION

The CDP6823 has 15 registers (see Fig. 1) which define the mode of operation and status of the port pins. The following paragraphs describe these registers.

Register Names:
Control Register A (CRA)
Control Register B (CRB)

Register Addresses:
$9 (CRA)
$A (CRB)

Register Bits:

	7	6	5	4	3	2	1	0
$9	X	X	X	CA2 Mode		CA1 LE	CA1 Mode	
$A	X	X	X	CB2 Mode		X	CB1 Mode	

Purpose:
These two registers control the handshake and interrupt activity for those pins defined as handshake lines by the port C function select register (FSR).

Description:
CA2 and CB2 are programmed as inputs or outputs via the associated DDRC bits. Each handshake line is controlled by two mode bits. Bit 2 of CRA enables the Port A latch for an active CA1 transition. Table 2 describes the input handshake modes (CA1, CB1, CA2, CB2) and Table 3 describes the output handshake modes for CA2 and CB2.

Register Names:
Port A Data Registers (PDA, P1DA, P2DA)

Register Addresses:
$2 (PDA), $0 (P1DA), $1 (P2DA)

Register Bits:

7	6	5	4	3	2	1	0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Purpose:
These three registers serve different purposes. PDA is used to read input data and latch data written to the port A output pins. P1DA and P2DA are used to read input data and to affect handshake and status activity for PC4/CA1 and PC5/CA2. If enabled, port A input data may be latched into the three port A data registers on an active PC4/CA1 transition as described in **HANDSHAKE OPERATION**.

Description:

Data written into PDA is latched into the port A output latch (see Fig. 3) regardless of the state of DDRA. Output pins, as defined by DDRA, assume the logic levels of the corresponding bits in the PDA output latch. The PDA output latch allows the user to read the state of the port A output data. If the input latch is not enabled, a read of any port A data register reflects the current state of the port A input pins as defined by DDRA and the contents of the output latch for output pins. Writes into P1DA or P2DA have no effect upon the output pins or the output data latch. Users are recommended to initialize the port A output latch before changing any pin to an output via the DDRA.

MPU accesses of P1DA or P2DA are primarily used to affect handshake and status activity. A summary of the effects on the status and warning bits of port A data register accesses is given in Table 4. For more information, see **HANDSHAKE OPERATION** and **Control Register A (CRA)** under **REGISTER DESCRIPTION**. Reset has no effect upon the contents of any port A data register.

Register Names:

Port B Data Registers (PDB, P1DB, P2DB)

Register Addresses:

· $3 (PDB), $C (P1DB), $D (P2DB)

Register Bits:

7	6	5	4	3	2	1	0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Purpose:

These three registers serve different purposes. The Port B data registers are used to read input data and to latch data written to the port B output pins. Writes to PDB and P1DB affect the contents of the output data latch while writes to P2DB do not affect the output data latch. P1DB and P2DB accesses additionally affect handshake and status activity for PC6/CB1 and PC7/CB2.

Description:

Data written into PDB and P1DB port B registers is latched into the port B output latch (see Fig. 3) regardless of the state of DDRB. Output pins, as defined by DDRB, assume the logic levels of the corresponding bits in the port B output latch. Reads of any port B data registers reflect the contents of the output data latch for output pins and the current state of the input pins (as determined by DDRB). Users are recommended to initialize the port B output latch before changing any pin to an output via the DDRB.

MPU accesses of P1DB or P2DB are primarily used to affect handshake and status activity. A summary of the effects on status and warning register bits of port B data register accesses is given in Table 5. For more information, see **HANDSHAKE OPERATION** or **Control Register B (CRB)** under **REGISTER DESCRIPTION**. Reset has no effect upon the contents of any port B data register.

TABLE 4 — SUMMARY OF EFFECTS ON HANDSHAKE STATUS, WARNING BITS, AND OUTPUT LATCH BY PORT A DATA REGISTER ACCESSES

Register Accessed	HSR Bit	HWR Bit	Handshake Reaction	Output Latch	
				Read	Write
PDA	None	None	None	Yes	Yes
P1DA	HSA1 cleared to a logic zero	HWA1 loaded into buffer latch	CA2 goes low if output modes 0 or 1 are selected in the CRA	Yes	No
P2DA	HSA2 cleared to a logic zero	HWA2 loaded into buffer latch	CA2 goes low if output modes 0 or 1 are selected in the CRA	Yes	No

TABLE 5 — SUMMARY OF EFFECTS ON HANDSHAKE STATUS, WARNING BITS, AND OUTPUT LATCH BY PORT B DATA REGISTER ACCESSES

Register Accessed	HSR Bit	HWR Bit	Handshake Reaction	Output Latch	
				Read	Write
PDB	None	None	None	Yes	Yes
P1DB	HSB1 cleared to a logic zero	HWB1 loaded into buffer latch	CB2 goes low if output modes 0 or 1 are selected in the CRB	Yes	Yes
P2DB	HSB2 cleared to a logic zero	HWA2 loaded into buffer latch	CB2 goes low if output modes 0 or 1 are selected in CRB	Yes	No

Register Name:
Port C Data Register (PDC)

Register Address:
$4

Register Bits:

7	6	5	4	3	2	1	0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Purpose:
The port C data register (PDC) is used to read input data and to latch data written to the output pins.

Description:
Data is written into the port C output latch (see Fig. 3) regardless of the state of DDRC. Any port C pin defined as a handshake line by the port C function select register (FSR) is not affected by PDC. Output pins, as defined by DDRC, assume logic levels of the corresponding bits in the port C output latch. A read of PDC reflects the contents of the output latch for output pins and the current state of the input pins (as reflected in the DDRC). Reset has no effect upon the contents of PDC. Users are recommended to initialize the port C output data latch before changing any pin to an output via the DDRC.

Register Name:
Data Direction Register for Port A (B) (C)

Register Address:
$6 ($7) ($8)

Register Bits:

7	6	5	4	3	2	1	0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Purpose:
Each of the three data direction registers (DDRA, DDRB, and DDRC) define the direction of data flow of the port pins for ports A, B, and C.

Description:
A logic zero in a DDR bit places the corresponding port pin in the input mode. A logic one in a DDR bit places the corresponding pin in the output mode. Any port C pins defined as bidirectional handshake lines also use the port C DDR (DDRC). Input-only handshake lines are not affected by DDRC. Reset clears all DDR bits to logic zero configuring all port pins as inputs. The DDRs have no write-inhibit control over the port data output latches. Data may be written to the port data registers even though the pins are configured as inputs.

Register Name:
Port C Pin Function Select Register (FSR)

Register Address:
$B

Register Bits:

7	6	5	4	3	2	1	0
CFB2	CFB1	CFA2	CFA1	XX	XX	XX	XX

Purpose:
The port C pin function select register defines whether the multifunction port C pins are to operate as "normal" port C lines or as handshake lines.

Description:
A logic zero in any FSR bit defines the corresponding port C pin as a "normal" I/O pin. A logic one in any valid FSR bit defines the corresponding port C pin as a handshake line. Pins defined as handshake lines function according to the contents of control register A (CRA) or control register B (CRB). The port C data direction register (DDRC) is valid regardless of FSR contents for all pins except PC4/CA1 and PC6/CB1. Transitions on port C pins not defined as handshake pins do not effect the handshake/interrupt status register. Reset clears all FSR bits to a logic zero. Users are recommended to initialize the data direction and control registers before modifying the FSR.

Register Name:
Handshake/Interrupt Status Register (HSR)

Register Address:
$E

Register Bits:

7	6	5	4	3	2	1	0
IRQF	XX	XX	XX	HSB2	HSA2	HSB1	HSA1

Purpose:
The handshake interrupt status register is a read-only flag register that may be used during a polling routine to determine if any enabled input handshake transition, as defined by the control register (CRA and CRB), has occurred.

Description:
If an enabled input handshake transition occurs then the appropriate HSR bit (HSB2, HSA2, HSB1, or HSA1) is set. The $\overline{\text{IRQ}}$ flag bit (bit 7, IRQF) is set when one or more of the HSR bits 0-3 and their corresponding control register bits are set to a logic one as shown in the following equation:

$$\text{Bit } 7 = \text{IRQF} = [\text{HSB2} \bullet \text{CRB2}(3)] + [\text{HSA2} \bullet \text{CRA2}(3)] + [\text{HSB1} \bullet \text{CRB1}(0)] + [\text{HSA1} \bullet \text{CRA1}(0)]$$

The numbers in ( ) indicate which bit in the control register enables the interrupt.

Handshake/interrupt status register bits are cleared by accessing the appropriate port data register. The following table lists the HSR bit and the port data register that must be accessed to clear the bit.

To Clear HSR Bit	Access Register
HSB2	P2DB
HSA2	P2DA
HSB1	P1DB
HSA1	P1DA

Reset clears all handshake/interrupt status register bits to a logic zero.

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Register Name:
Handshake Warning Register (HWR)

Register Address:
$F

Register Bits:

7	6	5	4	3	2	1	0
XX	XX	XX	XX	HWB2	HWA2	HWB1	HWA1

Purpose:
The warning register is a read-only flag register that may be used to determine if a second attempt to set a handshake/interrupt status register bit has been made before the original had been serviced.

Description:
Each bit in the handshake/interrupt status register, except IRQF, has a corresponding bit in the handshake warning register. If an attempt is made to set a bit in the handshake/interrupt status register that is already set, then the corresponding bit in the handshake warning register is also set. An attempt is the occurrence of any enabled input handshake transition as defined by the control registers.

A handshake warning register bit is cleared by first reading the appropriate data register then reading the handshake warning register. Reading the data register (either P1DA, P2DA, P1DB, or P2DB) loads a buffer latch with the proper bit in the handshake warning register (HWA1, HWA2, HWB1, and HWB2, respectively). The next read of the handshake warning register clears the appropriate bit without affecting the other three handshake warning register bits. The upper four bits, HWR4-HWR7, always read as logic zeros. If a port data register is not read before reading the handshake warning register, then the handshake warning register bits will remain unaffected. Reset clears all HWR bits to a logic zero.

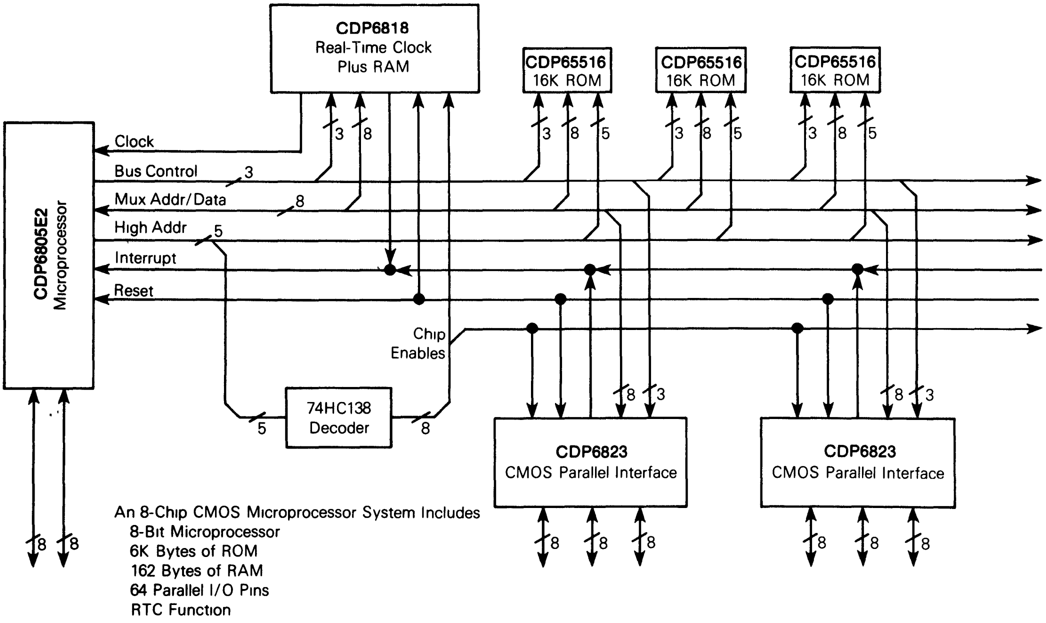
Recommended status register handling sequence:

1. Read status register	(User determines which if any enabled handshake transition occurred)
2. Read/write port data indicated by status register	(Clears associated status bit and latches appropriate warning register bit in the buffer latch)
3. Read warning register	(Latched warning bit is cleared and the remaining bits are unaffected)

TYPICAL INTERFACING

The CDP6823 is best suited for use with microprocessors which generate an address-then-data-multiplexed bus. Fig. 9 shows the CDP6823 in a typical CMOS system that uses the CDP6805E2 CMOS MPU. Other multiplexed microprocessors can be used as easily.

A single-chip microcomputer (MCU) may be interfaced with 11 port lines as shown in Fig. 10. This interface also requires some software overhead to gain up to 13 additional I/O lines and the CDP6823 handshake lines.



An 8-Chip CMOS Microprocessor System Includes
8-Bit Microprocessor
6K Bytes of ROM
162 Bytes of RAM
64 Parallel I/O Pins
RTC Function

Fig. 9 - A typical CMOS microprocessor system.

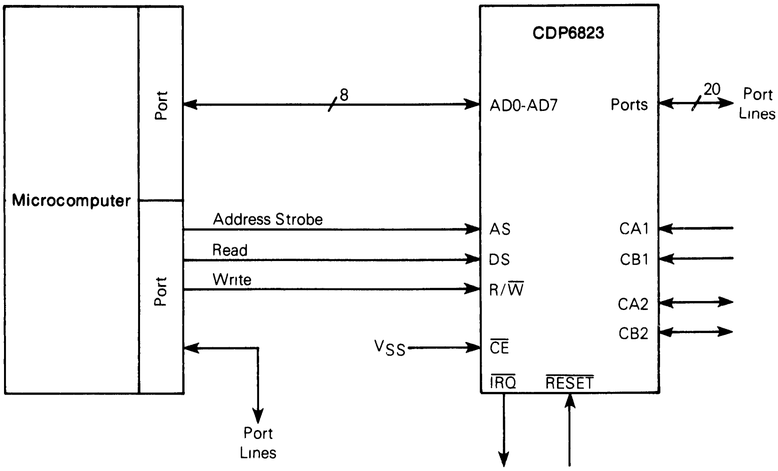
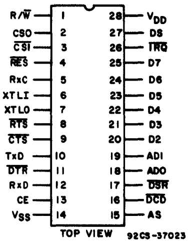


Fig. 10 - CDP6823 interfaced with the ports of a typical single-chip microprocessor.

CDP6853

Product Preview



TERMINAL ASSIGNMENT

CMOS Asynchronous Communications Interface Adapter (ACIA) with MOTEL Bus

Features:

- *Compatible with 8-bit microprocessors*
- *Multiplexed Address/Data Bus (MOTEL Bus)*
- *Full duplex operation with buffered receiver and transmitter*
- *Data set/modem control functions*
- *Internal baud rate generator with 15 programmable baud rates (50 to 19,200)*
- *Operates at baud rates up to 250,000 via proper crystal or clock selection*

The RCA-CDP6853 Asynchronous Communications Interface Adapter (ACIA) provides an easily implemented, program controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

The CDP6853 has an internal baud rate generator. This feature eliminates the need for multiple component support circuits, a crystal being the only other part required. The Transmitter baud rate can be selected under program control to be either 1 of 15 different rates from 50 to 19,200 baud, or at 1/16 times an external clock rate. The Receiver baud rate may be selected under program control to be either the Transmitter rate, or at 1/16 times an external clock rate. The CDP6853 has programmable word lengths of 5, 6, 7, or 8 bits; even, odd, or no parity; 1, 1½, or 2 stop bits.

The CDP6853 is designed for maximum programmed control from the CPU, to simplify hardware implementation. Three separate registers permit the CPU to easily select the CDP6853 operating modes and data checking parameters and determine operational status.

The Command Register controls parity, receiver echo mode, transmitter interrupt control, the state of the $\overline{RTS}$ line, receiver interrupt control, and the state of the $\overline{DTR}$ line.

The Control Register controls the number of stop bits, word length, receiver clock source, and baud rate.

The Status Register indicates the states of the $\overline{IRQ}$, $\overline{DSR}$, and $\overline{DCD}$ lines, Transmitter and Receiver Data Registers, and Overrun, Framing and Parity Error conditions.

- *Program-selectable internally or externally controlled receiver rate*
- *Programmable word lengths, number of stop bits, and parity bit generation and detection*
- *Programmable interrupt control*
- *Program reset*
- *Program-selectable serial echo mode*
- *Two chip selects*
- *One chip enable*
- *Single 3V to 6V power supply*
- *Full TTL compatibility*
- *4-MHz, 2-MHz, or 1-MHz operation (CDP6853-4, CDP6853-2, CDP6853-1, respectively)*

The Transmitter and Receiver Data Registers are used for temporary data storage by the CDP6853 Transmit and Receiver circuits.

The MOTEL Bus allows interfacing to 6805 and 8085 type multiplexed address data bus.

The CDP6853-1, CDP6853-2, and CDP6853-4 are capable of interfacing with microprocessors with cycle times of 1-MHz, 2-MHz, and 4-MHz, respectively.

The CDP6853 is supplied in 28-lead, hermetic, dual-in-line side-brazed ceramic (D suffix) and in 28-lead, dual-in-line plastic (E suffix) packages.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal) .... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A=-40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A=+60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A=-55 to +100° C (PACKAGE TYPE D) .... 500 mW
For T_A=+100 to 125° C (PACKAGE TYPE D) .... Derate Linearly at 8 mW/° C to 300 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D .... -55 to +125° C
PACKAGE TYPE E .... -40 to +85° C
STORAGE-TEMPERATURE RANGE (T_{stg}) .... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C

RECOMMENDED OPERATING CONDITIONS at T_A = -40° to +85° C
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating Voltage Range	3	6	V
Input Voltage Range	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40° to +85° C, V_{DD} = 5 V ± 5%

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Quiescent Device Current	I_{DD}	—	50	200	µA
Output Low Current (Sinking): V_{OL} = 0.4 V (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	I_{OL}	1.6	—	—	mA
Output High Current (Sourcing): V_{OH} = 4.6 V (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	I_{OH}	-1.6	—	—	mA
Output Low Voltage: I_{LOAD} = 1.6 mA (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	—	—	0.4	V
Output High Voltage: I_{LOAD} = -1.6 mA (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	V_{OH}	4.6	—	—	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Input High Voltage	V_{IH}				V
(Except XTLI and XTLO)		2	—	V_{DD}	
(XTLI and XTLO)		3	—	V_{DD}	
Input Leakage Current: V_{IN} = 0 to 5 V (R/$\overline{W}$, $\overline{RES}$, CS0, $\overline{CS1}$, CE, DS, AS, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	—	—	± 1	µA
Input Leakage Current for High Impedance State (D0-D7)	I_{TSI}	—	—	± 1.2	µA
Output Leakage Current (off state): V_{OUT} = 5 V ($\overline{IRQ}$)	I_{OFF}	—	—	2	µA
Input Capacitance (except XTLI and XTLO)	C_{IN}	—	—	10	pF
Output Capacitance	C_{OUT}	—	—	10	pF

CDP6853

CDP6853 INTERFACE REQUIREMENTS

This section describes the interface requirements for the CDP6853 ACIA. Fig. 1 is the Interface Diagram and the Terminal Diagram shows the pin-out configuration for the CDP6853.

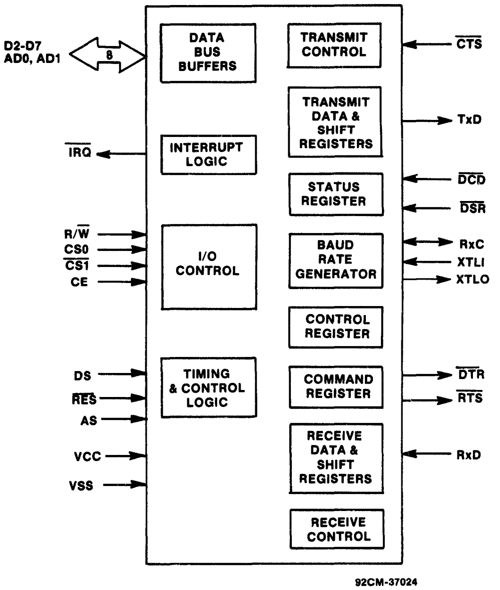


Fig. 1 - CDP6853 interface diagram.

MICROPROCESSOR INTERFACE SIGNAL DESCRIPTION

RES (Reset) (4)

During system initialization a low on the RES input will cause a hardware reset to occur. The Command Register and the Control Register will be cleared. The Status Register will be cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the DSR and DCD lines, and the transmitter Empty bit, which will be set. A hardware reset is required after power-up.

R/W (Read/Write) (1)

The MOTEL circuit treats the R/W pin in one of two ways. When a 6805 type processor is connected, R/W is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/W while DS is high, whereas a write cycle is a low on R/W during DS.

The second interpretation of R/W is as a negative write pulse, WR, MEMW, and I/OW from competitor type processors. The MOTEL circuit in this mode gives R/W pin the same meaning as the write (W) pulse on many generic RAMs.

IRQ (Interrupt Request) (26)

The IRQ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common IRQ microprocessor input. Normally a high level, IRQ goes low when an interrupt occurs.

D2-D7 (Data Bus) (20-25)

The D2-D7 pins are the eight data lines used to transfer data between the processor and the CDP6853. These lines are bi-directional and are normally high-impedance except during Read cycles when the CDP6853 is selected.

CE, CS0, CS1 (Chip Selects) (2,3,13)

The two chip select and the one chip enable inputs are normally connected to the processor address lines either directly or through decoders. The CDP6853 is selected when CS0 is high, CS1 is low, and CE is high.

AD0, AD1 (Multiplexed Bidirectional Address/Data Bits) (18,19)

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data. Address-then-data multiplexing does not slow the access time of the CDP6853 since the bus reversal from address to data is occurring during the internal RAM access time.

The address must be valid just prior to the fall of AS/ALE at which time the CDP6853 latches the address from AD0 to AD1. Valid write data must be presented and held stable during the latter portion of the DS or WR pulses. In a read cycle, the CDP6853 outputs 8 bits of data during the latter portion of the DS or RD pulses, then ceases driving the bus (returns the output drivers to three-state) when DS falls in this case of MOTEL or RD rises in the other case. The following table shows internal register select coding:

TABLE I

AD1	AD0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Only the Command and Control registers are read/write. The programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command register and bit 2 in the Status register. The Control Register is unchanged by a Programmed Reset. It should be noted that the Programmed Reset is slightly different from the Hardware Reset (RES); these differences are shown in Figs. 4, 5, and 6.

ACIA/MODEM INTERFACE SIGNAL DESCRIPTION

XTLI, XTLO (Crystal Pins) (6,7)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates (see "Generation of Non-Standard Baud Rates"). Alternatively, an externally generated clock may be used to drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

TxD (Transmit Data) (10)

The TxD output line is used to transfer serial NRZ (nonreturn-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected or under control of an external clock. This selection is made by programming the Control Register.

CDP6853 INTERFACE REQUIREMENTS (Cont'd)

RxD (Receive Data) (12)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or under the control of an externally generated receiver clock. The selection is made by programming the Control Register.

RxC (Receive Clock) (5)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{\text{RTS}}$ (Request to Send) (8)

The $\overline{\text{RTS}}$ output pin is used to control the modem from the processor. The state of the $\overline{\text{RTS}}$ pin is determined by the contents of the Command Register.

$\overline{\text{CTS}}$ (Clear to Send) (9)

The $\overline{\text{CTS}}$ input pin is used to control the transmitter operation. The enable state is with $\overline{\text{CTS}}$ low. The transmitter is automatically disabled if $\overline{\text{CTS}}$ is high.

$\overline{\text{DTR}}$ (Data Terminal Ready) (11)

This output pin is used to indicate the status of the CDP6853 to the modem. A low on $\overline{\text{DTR}}$ indicates the CDP6853 is enabled, a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{\text{DSR}}$ (Data Set Ready) (17)

The $\overline{\text{DSR}}$ input pin is used to indicate to the CDP6853 the status of the modem. A low indicates the "ready" state and a high, "not-ready".

$\overline{\text{DCD}}$ (Data Carrier Detect) (16)

The $\overline{\text{DCD}}$ input pin is used to indicate to the CDP6853 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

DS (Data Strobe or Read) (27)

The DS pin has two interpretations via the MOTEL circuit. When emanating from a 6800 type processor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and $\phi 2$ ($\phi 2$ clock). During read cycles, DS signifies the time that the ACIA is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the ACIA to latch the written data.

The second MOTEL interpretation of DS is that of $\overline{\text{RD}}$, $\overline{\text{MEMR}}$, or $\overline{\text{I/OR}}$ emanating from an 8085 type processor. In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data. This interpretation of DS is also the same as an output-enable signal on a typical memory.

The MOTEL circuit, within the CDP6853 latches the state of the DS pin on the falling edge of AS/ALE. When the 6800 mode of MOTEL is desired DS must be low during AS/ALE, which is the case with the CDP6805 family of multiplexed bus processors. To insure the 8085 mode of MOTEL, the DS pin must remain high during the time AS/ALE is high.

AS (Multiplexed Address Strobe) (15)

A positive-going multiplexed address strobe pulse serves to demultiplex AD0 and AD1. The falling edge of AS or ALE causes the address to be latched within the CDP6853. The automatic MOTEL circuitry in the CDP6853 also latches the state of the DS pin with the falling edge of AS or ALE.

MOTEL

The MOTEL circuit is a new concept that permits the CDP6853 to be directly interfaced with many types of microprocessors. No external logic is needed to adapt to the differences in bus control signals from common multiplexed bus microprocessors.

Practically all microprocessors interface with one of two synchronous bus structures.

The MOTEL circuit is built into peripheral and memory ICs to permit direct connection to either type of bus. An industry-standard bus structure is now available. The MOTEL concept is shown logically in Fig. 2.

MOTEL selects one of two interpretations of two pins. In the 6805 case, DS and R/$\overline{\text{W}}$ are gated together to produce the internal read enable. The internal write enable is a similar gating of the inverse of R/$\overline{\text{W}}$. With 8085 Family buses, the inversion of $\overline{\text{RD}}$ and $\overline{\text{WR}}$ create functionally identical internal read and write enable signals.

The CDP6853 automatically selects the processor type by using AS/ALE to latch the state of the DS/$\overline{\text{RD}}$ pin. Since DS is always low and $\overline{\text{RD}}$ is always high during AS and ALE, the latch automatically indicates which processor type is connected.

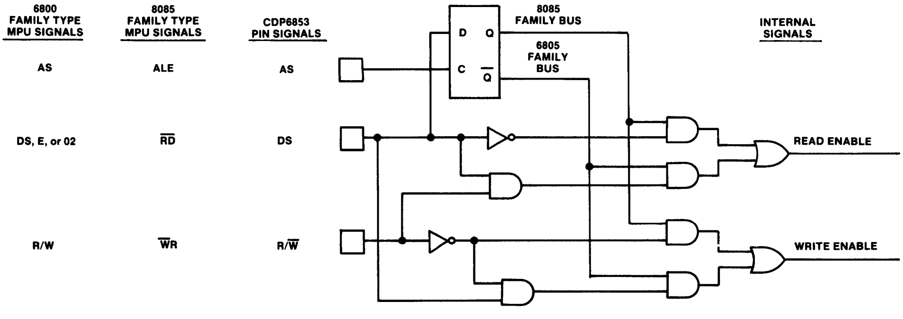


Fig. 2 - Functional diagram of MOTEL circuit.

CDP6853 INTERNAL ORGANIZATION

This section provides a functional description of the CDP6853. A block diagram of the CDP6853 is presented in Fig. 3.

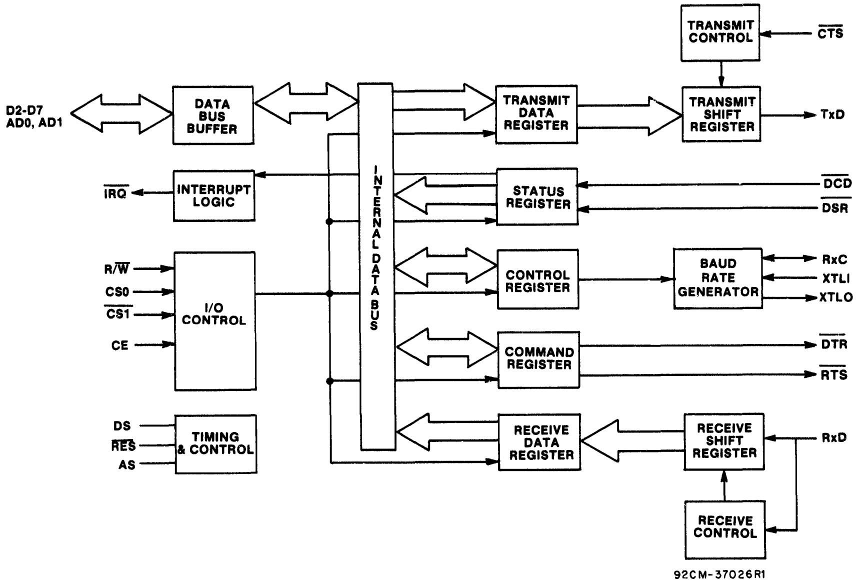


Fig. 3 - Internal organization.

DATA BUS BUFFERS

The Data Bus Buffer interfaces the system data lines to the internal data bus. The Data Bus Buffer is bi-directional. When the R/$\overline{\text{W}}$ line is high and the chip is selected, the Data Bus Buffer passes the data to the system data lines from the CDP6853 internal data bus. When the R/$\overline{\text{W}}$ line is low and the chip is selected, the Data Bus Buffer writes the data from the system data bus to the internal data bus.

INTERRUPT LOGIC

The Interrupt Logic will cause the $\overline{\text{IRQ}}$ line to the microprocessor to go low when conditions are met that require the attention of the microprocessor. The conditions which can cause an interrupt will set bit 7 and the appropriate bit of bits 3 through 6 in the Status Register if enabled. Bits 5 and 6 correspond to the Data Carrier Detect ($\overline{\text{DCD}}$) logic and the Data Set Ready ($\overline{\text{DSR}}$) logic. Bits 3 and 4 correspond to the Receiver Data Register full and the Transmitter Data Register empty conditions. These conditions can cause an interrupt request if enabled by the Command Register.

I/O CONTROL

The I/O Control Logic controls the selection of internal registers in preparation for a data transfer on the internal data bus and the direction of the transfer to or from the register.

The registers are selected by the Register Select and Chip Select and Read/Write lines as described in Table I, previously.

TIMING AND CONTROL

The Timing and Control logic controls the timing of data transfers on the internal data bus and the registers, the Data Bus Buffer, and the microprocessor data bus, and the hardware reset features.

Timing is controlled by the system $\phi 2$ clock input. The chip will perform data transfers to or from the microcomputer data bus during the $\phi 2$ high period when selected.

All registers will be initialized by the Timing and Control Logic when the Reset ($\overline{\text{RES}}$) line goes low. See the individual register description for the state of the registers following a hardware reset.

TRANSMITTER AND RECEIVER DATA REGISTERS

These registers are used as temporary data storage for the CDP6853 Transmit and Receive Circuits. Both the Transmitter and Receiver are selected by a Register Select 0 (RS0) and Register Select 1 (RS1) low condition. The Read/Write line determines which actually uses the internal data bus; the Transmitter Data Register is write only and the Receiver Data Register is read only.

Bit 0 is the first bit to be transmitted from the Transmitter Data Register (least significant bit first). The higher order bits follow in order. Unused bits in this register are "don't care".

The Receiver Data Register holds the first received data bit in bit 0 (least significant bit first). Unused high-order bits are "0". Parity bits are not contained in the Receiver Data Register. They are stripped off after being used for parity checking.

STATUS REGISTER

Fig. 4 indicates the format of the CDP6853 Status Register. A description of each status bit follows.

CDP6853 INTERNAL ORGANIZATION (Cont'd)

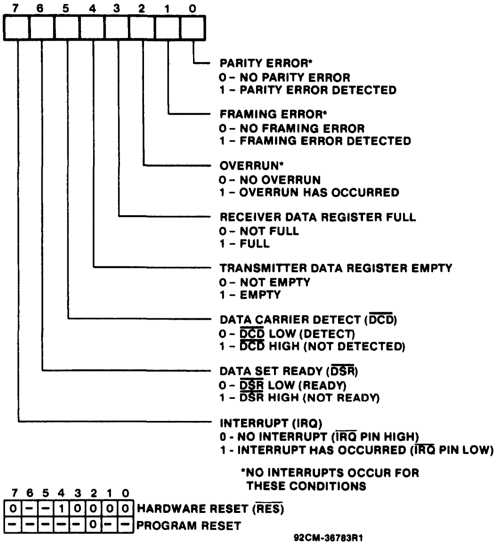

7 6 5 4 3 2 1 0
PARITY ERROR*
0 – NO PARITY ERROR
1 – PARITY ERROR DETECTED
FRAMING ERROR*
0 – NO FRAMING ERROR
1 – FRAMING ERROR DETECTED
OVERRUN*
0 – NO OVERRUN
1 – OVERRUN HAS OCCURRED
RECEIVER DATA REGISTER FULL
0 – NOT FULL
1 – FULL
TRANSMITTER DATA REGISTER EMPTY
0 – NOT EMPTY
1 – EMPTY
DATA CARRIER DETECT ($\overline{DCD}$)
0 – $\overline{DCD}$ LOW (DETECT)
1 – $\overline{DCD}$ HIGH (NOT DETECTED)
DATA SET READY ($\overline{DSR}$)
0 – $\overline{DSR}$ LOW (READY)
1 – $\overline{DSR}$ HIGH (NOT READY)
INTERRUPT (IRQ)
0 - NO INTERRUPT ($\overline{IRQ}$ PIN HIGH)
1 - INTERRUPT HAS OCCURRED ($\overline{IRQ}$ PIN LOW)
*NO INTERRUPTS OCCUR FOR THESE CONDITIONS
7 6 5 4 3 2 1 0
0 – – 1 0 0 0 0 HARDWARE RESET ($\overline{RES}$)
– – – – – 0 – – PROGRAM RESET
92CM-36783R1

Fig. 4 – Status register format.

Receiver Data Register Full (Bit 3)

This bit goes to a "1" when the CDP6853 transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a "0" when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a "1" when the CDP6853 transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a "0" when the processor writes new data onto the Transmitter Data Register.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the CDP6853. A "0" indicates a low level (true condition) and a "1" indicates a high (false). Whenever either of these inputs change state, an immediate processor interrupt occurs, unless the CDP6853 is disabled (bit 0 of the Command Register is a "0"). When the interrupt occurs, the status bits will indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until the Status Register is interrogated by the processor. At that time, another interrupt will immediately occur and the status bits will reflect the new input levels.

Framing Error (Bit 1), Overrun (2), and Parity Error (Bit 0)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified.

Interrupt (Bit 7)

This bit goes to a "0" when the Status Register has been read by the processor, and goes to a "1" whenever any kind of interrupt occurs.

CONTROL REGISTER

The Control Register selects the desired transmitter baud rate, receiver clock source, word length, and the number of stop bits.

Selected Baud Rate (Bits 0,1,2,3)

These bits, set by the processor, select the Transmitter baud rate, which can be at 1/16 an external clock rate or one of 15 other rates controlled by the internal baud rate generator as shown in Fig. 5.

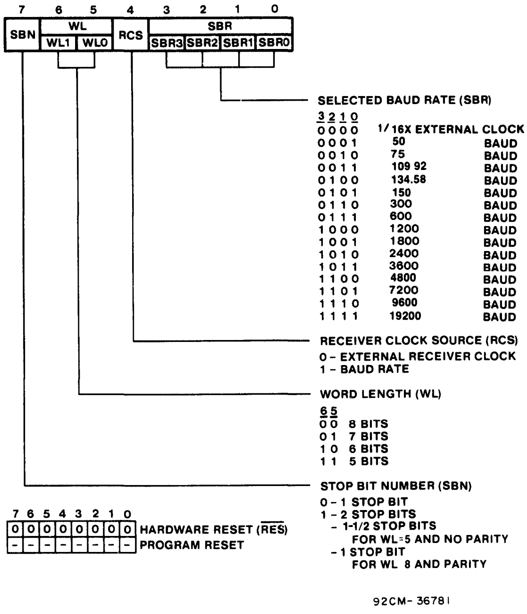


Fig. 5 - CDP6853 control register.

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A "0" causes the Receiver to operate at a baud rate of 1/16 an external clock. A "1" causes the Receiver to operate at the same baud rate as is selected for the transmitter as shown in Fig. 5.

Word Length (Bits 5,6)

These bits determine the word length to be used (5, 6, 7 or 8 bits). Fig. 5 shows the configuration for each number of bits desired.

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A "0" always indicates one stop bit. A "1" indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, and 2 stop bits in all other configurations.

CDP6853

CDP6853 INTERNAL ORGANIZATION (Cont'd)

COMMAND REGISTER

The Command Register controls specific modes and functions (Fig. 6).

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{DTR}$) line. A "0" indicates the microcomputer system is not ready by setting the $\overline{DTR}$ line high. A "1" indicates the microcomputer system is ready by setting the $\overline{DTR}$ line low. When the DTR bit is set to a "0", the receiver and transmitter are both disabled.

Receiver Interrupt Control (Bit 1)

This bit disables the Receiver from generating an interrupt when set to a "1". The Receiver interrupt is enabled when this bit is set to a "0" and Bit 0 is set to a "1".

Transmitter Interrupt Control (Bits 2,3)

These bits control the state of the Ready to Send ($\overline{RTS}$) line and the Transmitter interrupt. Fig. 6 shows the various configurations of the $\overline{RTS}$ line and Transmit Interrupt bit settings.

Receiver Echo Mode (Bit 4)

This bit enables the Receiver Echo Mode. Bits 2 and 3 must also be zero. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by ½ bit time. A "1" enables the Receiver Echo Mode. A "0" bit disables the mode.

Parity Mode Enable (Bit 5)

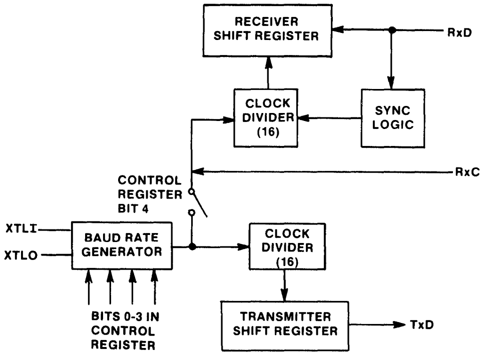
This bit enables parity bit generation and checking. A "0" disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A "1" bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6,7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check). Fig. 6 shows the possible bit configurations for the Parity Mode Control bits.

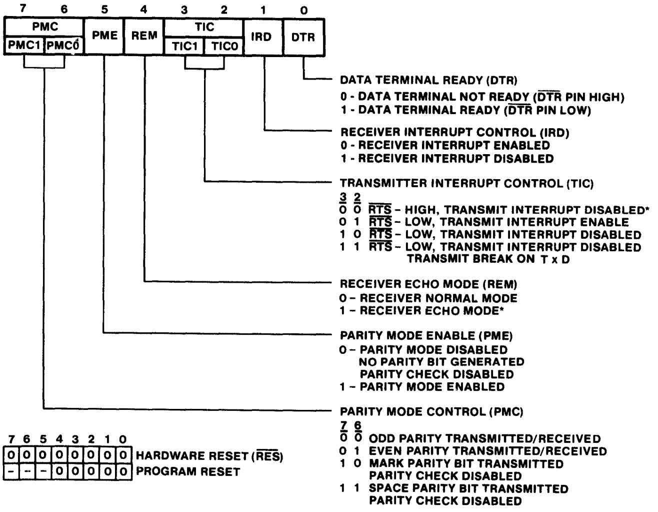
TRANSMITTER AND RECEIVER

Bits 0-3 of the Control Register select divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the CDP6853. Fig. 7 shows the transmitter and Receiver layout.



92CS-36791

Fig. 7 - Transmitter receiver clock circuits.


7 6 5 4 3 2 1 0
PMC
PMC1
PMC0
PME
REM
TIC
TIC1
TIC0
IRD
DTR
DATA TERMINAL READY (DTR)
0 - DATA TERMINAL NOT READY (DTR PIN HIGH)
1 - DATA TERMINAL READY (DTR PIN LOW)
RECEIVER INTERRUPT CONTROL (IRD)
0 - RECEIVER INTERRUPT ENABLED
1 - RECEIVER INTERRUPT DISABLED
TRANSMITTER INTERRUPT CONTROL (TIC)
3 2
0 0 RTS - HIGH, TRANSMIT INTERRUPT DISABLED*
0 1 RTS - LOW, TRANSMIT INTERRUPT ENABLE
1 0 RTS - LOW, TRANSMIT INTERRUPT DISABLED
1 1 RTS - LOW, TRANSMIT INTERRUPT DISABLED TRANSMIT BREAK ON T x D
RECEIVER ECHO MODE (REM)
0 - RECEIVER NORMAL MODE
1 - RECEIVER ECHO MODE*
PARITY MODE ENABLE (PME)
0 - PARITY MODE DISABLED NO PARITY BIT GENERATED PARITY CHECK DISABLED
1 - PARITY MODE ENABLED
PARITY MODE CONTROL (PMC)
7 6
0 0 ODD PARITY TRANSMITTED/RECEIVED
0 1 EVEN PARITY TRANSMITTED/RECEIVED
1 0 MARK PARITY BIT TRANSMITTED PARITY CHECK DISABLED
1 1 SPACE PARITY BIT TRANSMITTED PARITY CHECK DISABLED
7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0 HARDWARE RESET (RES)
- - - 0 0 0 0 0 PROGRAM RESET

*BITS 2 AND 3 MUST BE ZERO FOR RECEIVER ECHO MODE $\overline{RTS}$ WILL BE LOW.

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Fig. 6 - CDP6853 command register.

CDP6853 OPERATION (Cont'd)

TRANSMITTER AND RECEIVER OPERATION

Continuous Data Transmit (Fig. 8)

In the normal operating mode, the processor interrupt ($\overline{IRQ}$) is used to signal when the CDP6853 is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the CDP6853, the interrupt is cleared. The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "MARK" will be transmitted.

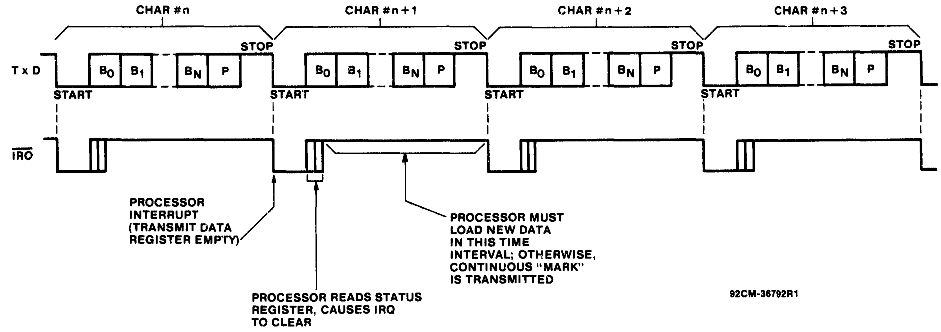

CHAR #n
CHAR #n+1
CHAR #n+2
CHAR #n+3
STOP
TxD
B0
B1
BN
P
START
IRQ
PROCESSOR INTERRUPT (TRANSMIT DATA REGISTER EMPTY)
PROCESSOR MUST LOAD NEW DATA IN THIS TIME INTERVAL; OTHERWISE, CONTINUOUS "MARK" IS TRANSMITTED
PROCESSOR READS STATUS REGISTER, CAUSES IRQ TO CLEAR
92CM-36792R1

Fig. 8 - Continuous data transmit.

Continuous Data Receive (Fig. 9)

Similar to the above case, the normal mode is to generate a processor interrupt when the CDP6853 has received a full data word. This occurs at about the 8/16 point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the Overrun condition occurs.

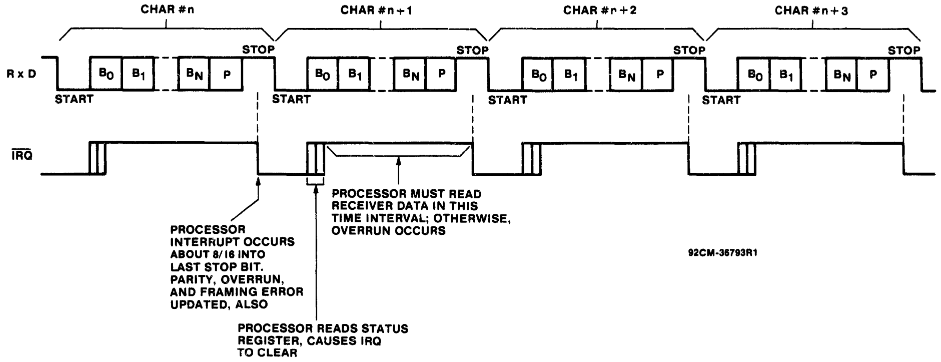

CHAR #n
CHAR #n+1
CHAR #n+2
CHAR #n+3
STOP
RxD
B0
B1
BN
P
START
IRQ
PROCESSOR INTERRUPT OCCURS ABOUT 8/16 INTO LAST STOP BIT. PARITY, OVERRUN, AND FRAMING ERROR UPDATED, ALSO
PROCESSOR MUST READ RECEIVER DATA IN THIS TIME INTERVAL; OTHERWISE, OVERRUN OCCURS
PROCESSOR READS STATUS REGISTER, CAUSES IRQ TO CLEAR
92CM-36793R1

Fig. 9 - Continuous data receive.

CDP6853 OPERATION (Cont'd)

Transmit Data Register Not Loaded By Processor (Fig. 10)

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line will go to the "MARK" condition until the data is loaded. $\overline{\text{IRQ}}$ interrupts continue to occur at the same rate as previously, except no data is transmitted. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word.

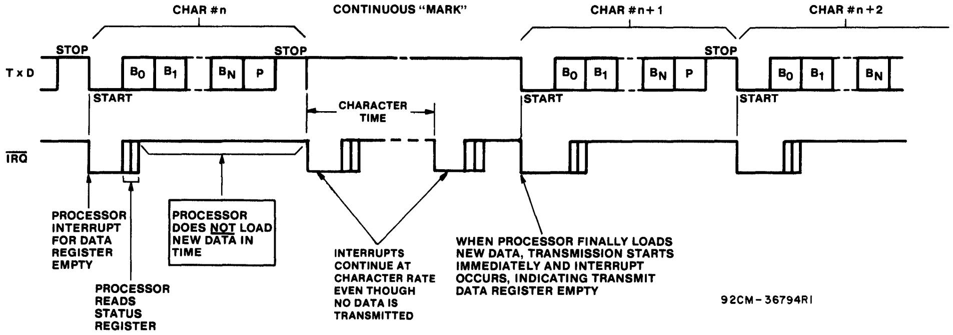

CHAR #n
CONTINUOUS "MARK"
CHAR #n+1
CHAR #n+2
STOP
STOP
STOP
TxD
B_0
B_1
B_N
P
START
START
START
CHARACTER TIME
$\overline{\text{IRQ}}$
PROCESSOR INTERRUPT FOR DATA REGISTER EMPTY
PROCESSOR DOES NOT LOAD NEW DATA IN TIME
PROCESSOR READS STATUS REGISTER
INTERRUPTS CONTINUE AT CHARACTER RATE EVEN THOUGH NO DATA IS TRANSMITTED
WHEN PROCESSOR FINALLY LOADS NEW DATA, TRANSMISSION STARTS IMMEDIATELY AND INTERRUPT OCCURS, INDICATING TRANSMIT DATA REGISTER EMPTY
92CM-36794RI

Fig. 10 - Transmit data register not loaded by processor.

Effect of $\overline{\text{CTS}}$ on Transmitter (Fig. 11)

$\overline{\text{CTS}}$ is the Clear-to-Send Signal generated by the modem. It is normally low (True State) but may go high in the event of some modem problems. When this occurs, the TxD line immediately goes to the "MARK" condition. Interrupts continue at the same rate, but the Status Register does not indicate that the Transmit Data Register is empty. Since there is no status bit for $\overline{\text{CTS}}$, the processor must deduce that $\overline{\text{CTS}}$ has gone to the FALSE (high) state. This is covered later. $\overline{\text{CTS}}$ is a transmit control line only, and has no effect on the CDP6853 Receiver Operation.

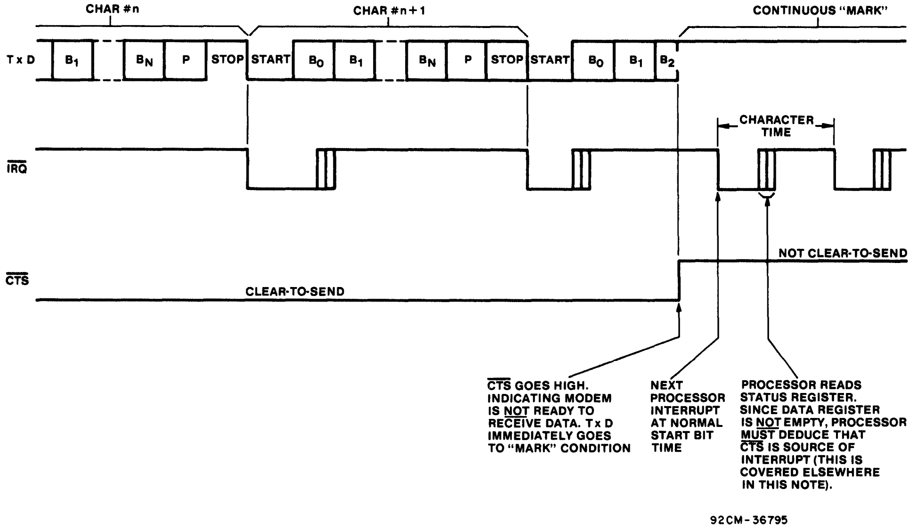

CHAR #n
CHAR #n+1
CONTINUOUS "MARK"
TxD
B_1
B_N
P
STOP
START
B_0
B_1
B_N
P
STOP
START
B_0
B_1
B_2
CHARACTER TIME
$\overline{\text{IRQ}}$
NOT CLEAR-TO-SEND
$\overline{\text{CTS}}$
CLEAR-TO-SEND
$\overline{\text{CTS}}$ GOES HIGH. INDICATING MODEM IS NOT READY TO RECEIVE DATA. TxD IMMEDIATELY GOES TO "MARK" CONDITION
NEXT PROCESSOR INTERRUPT AT NORMAL START BIT TIME
PROCESSOR READS STATUS REGISTER. SINCE DATA REGISTER IS NOT EMPTY, PROCESSOR MUST DEDUCE THAT $\overline{\text{CTS}}$ IS SOURCE OF INTERRUPT (THIS IS COVERED ELSEWHERE IN THIS NOTE).
92CM-36795

Fig. 11 - Effect of $\overline{\text{CTS}}$ on transmitter.

CDP6853 OPERATION (Cont'd)

Effect of Overrun on Receiver (Fig. 12)

If the processor does not read the Receiver Data Register in the allocated time, then, when the following interrupt occurs, the new data word is not transferred to the Receiver Data Register, but the Overrun status bit is set. Thus, the Data Register will contain the last valid data word received and all following data is lost.

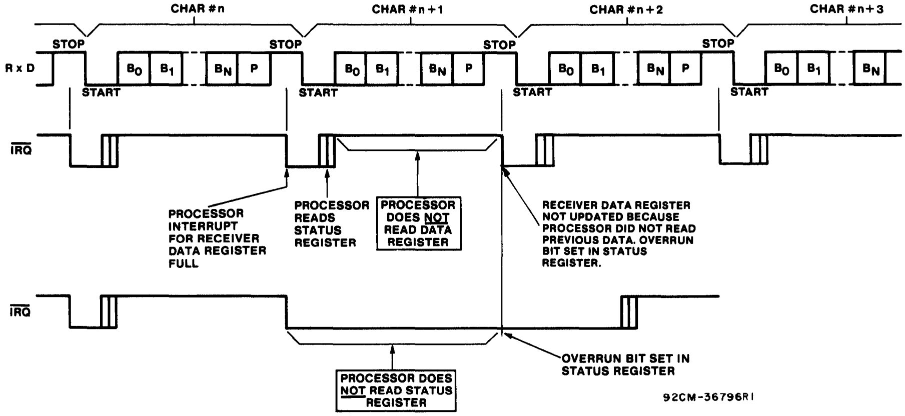

CHAR #n
CHAR #n+1
CHAR #n+2
CHAR #n+3
STOP
STOP
STOP
STOP
RxD
B0
B1
BN
P
START
START
START
START
IRQ
PROCESSOR INTERRUPT FOR RECEIVER DATA REGISTER FULL
PROCESSOR READS STATUS REGISTER
PROCESSOR DOES NOT READ DATA REGISTER
RECEIVER DATA REGISTER NOT UPDATED BECAUSE PROCESSOR DID NOT READ PREVIOUS DATA. OVERRUN BIT SET IN STATUS REGISTER.
IRQ
PROCESSOR DOES NOT READ STATUS REGISTER
OVERRUN BIT SET IN STATUS REGISTER
92CM-36796R1

Fig. 12 - Effect of overrun on receiver.

Echo Mode Timing (Fig. 13)

In Echo Mode, the TxD line re-transmits the data on the RxD line, delayed by ½ of the bit time.

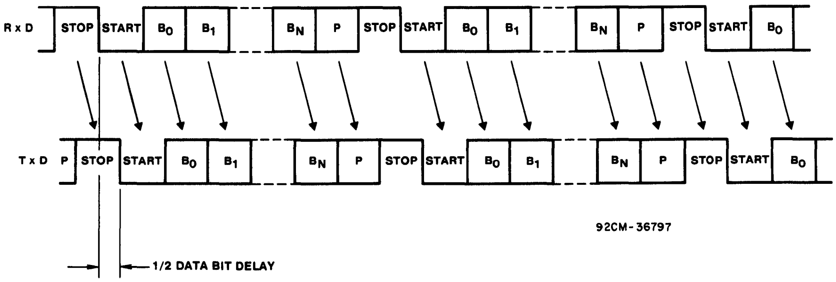


Fig. 13 - Echo mode timing.

CDP6853 OPERATION (Cont'd)

Effect of $\overline{CTS}$ on Echo Mode Operation (Fig. 14)

See "Effect of $\overline{CTS}$ on Transmitter" for the effect of $\overline{CTS}$ on the Transmitter. Receiver operation is unaffected by $\overline{CTS}$, so, in Echo Mode, the Transmitter is affected in the same way as "Effect of $\overline{CTS}$ on Transmitter". In this case, however, the processor interrupts signify that the Receiver Data Register is full, so the processor has no way of knowing that the Transmitter has ceased to echo.

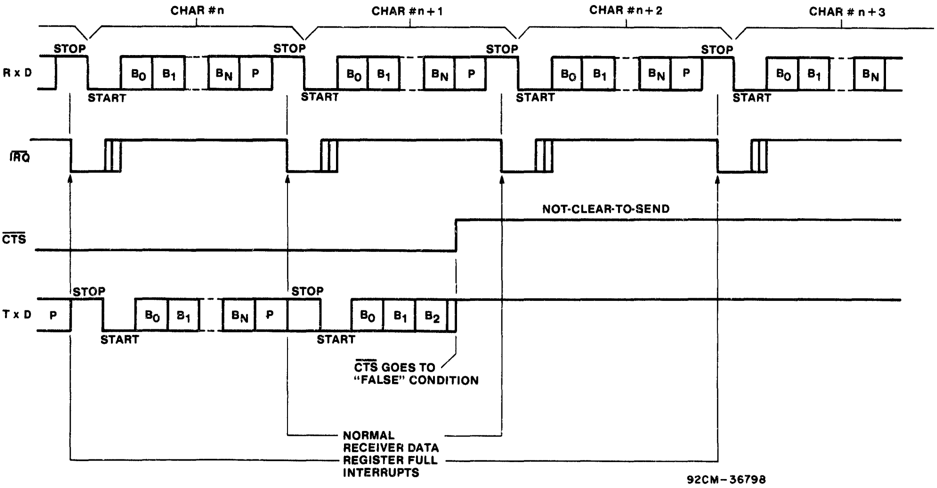


Fig. 14 - Effect of $\overline{CTS}$ on echo mode.

Overrun in Echo Mode (Fig. 15)

If Overrun occurs in Echo Mode, the Receiver is affected the same way as described in "Effect of Overrun on Receiver". For the re-transmitted data, when overrun occurs, the TxD line goes to the "MARK" condition until the first Start Bit after the Receiver Data Register is read by the processor.

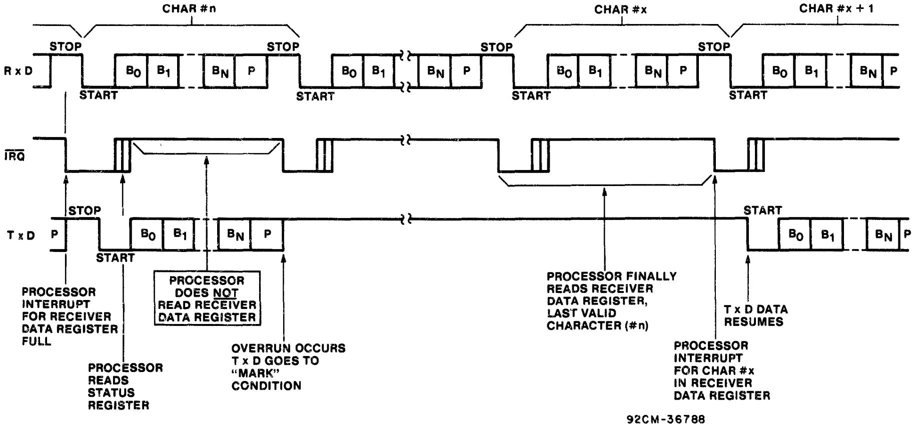
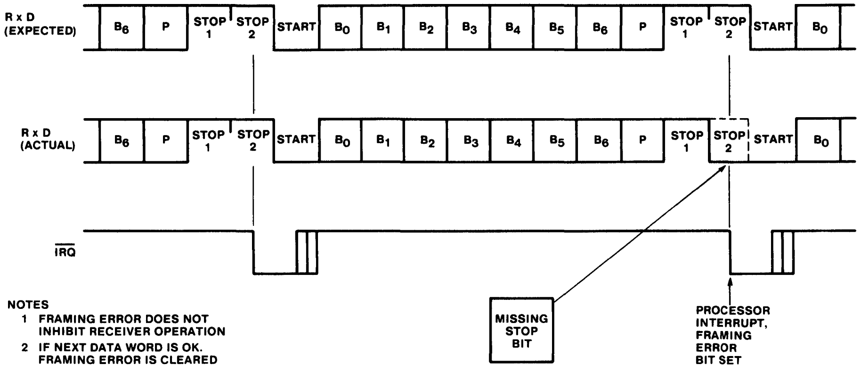

CHAR #n
CHAR #x
CHAR #x + 1
STOP
RxD
START
B0 B1 BN P
$\overline{IRQ}$
TxD
PROCESSOR INTERRUPT FOR RECEIVER DATA REGISTER FULL
PROCESSOR READS STATUS REGISTER
PROCESSOR DOES NOT READ RECEIVER DATA REGISTER
OVERRUN OCCURS TxD GOES TO "MARK" CONDITION
PROCESSOR FINALLY READS RECEIVER DATA REGISTER, LAST VALID CHARACTER (#n)
PROCESSOR INTERRUPT FOR CHAR #x IN RECEIVER DATA REGISTER
TxD DATA RESUMES
92CM-36788

Fig. 15 - Overrun in echo mode.

CDP6853 OPERATION (Cont'd)

Framing Error (Fig. 16)

Framing Error is caused by the absence of Stop Bit(s) on received data. The status bit is set when the processor interrupt occurs. Subsequent data words are tested for Framing Error separately, so the status bit will always reflect the last data word received.



NOTES
1 FRAMING ERROR DOES NOT INHIBIT RECEIVER OPERATION
2 IF NEXT DATA WORD IS OK. FRAMING ERROR IS CLEARED

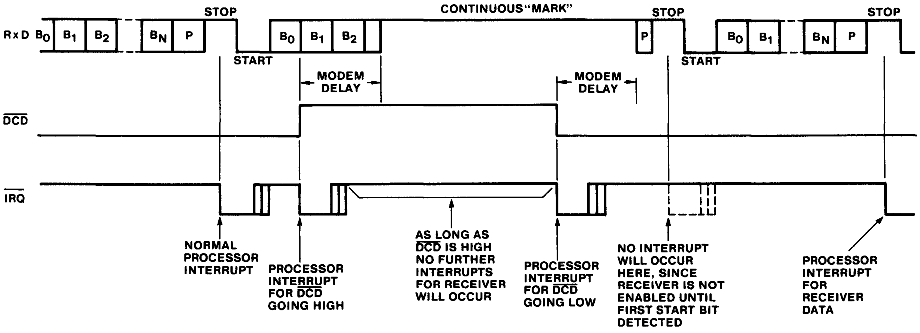
92CM-36789

Fig. 16 - Framing error.

Effect of $\overline{DCD}$ on Receiver (Fig. 17)

$\overline{DCD}$ is a modem output used to indicate the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data (RxD on the CDP6853 some time later. The CDP6853 will cause a processor interrupt whenever $\overline{DCD}$ changes state and will indicate this condition via the Status Register.

Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the CDP6853 automatically checks the level of the $\overline{DCD}$ line, and if it has changed, another interrupt occurs.


RxD
B0
B1
B2
BN
P
STOP
START
B0
B1
B2
CONTINUOUS "MARK"
MODEM DELAY
MODEM DELAY
P
STOP
START
B0
B1
BN
P
STOP
$\overline{DCD}$
$\overline{IRQ}$
NORMAL PROCESSOR INTERRUPT
PROCESSOR INTERRUPT FOR $\overline{DCD}$ GOING HIGH
AS LONG AS $\overline{DCD}$ IS HIGH NO FURTHER INTERRUPTS FOR RECEIVER WILL OCCUR
PROCESSOR INTERRUPT FOR $\overline{DCD}$ GOING LOW
NO INTERRUPT WILL OCCUR HERE, SINCE RECEIVER IS NOT ENABLED UNTIL FIRST START BIT DETECTED
PROCESSOR INTERRUPT FOR RECEIVER DATA

92CM-36786

Fig. 17 - Effect of $\overline{DCD}$ on receiver.

CDP6853 OPERATION (Cont'd)

Timing with 1½ Stop Bits (Fig. 18)

It is possible to select 1½ Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the processor interrupt for Receiver Data Register Full occurs halfway through the trailing half-Stop Bit.

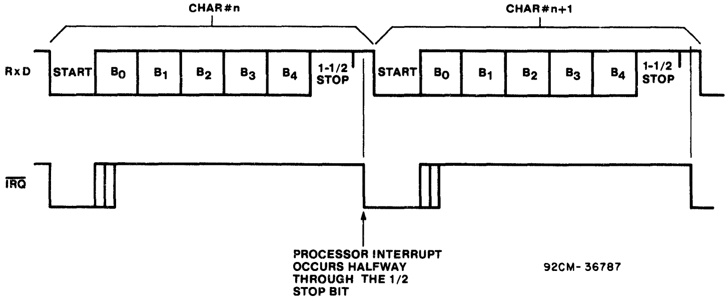


Fig. 18 - Timing with 1-1/2 stop bits.

Transmit Continuous "BREAK" (Fig. 19)

This mode is selected via the CDP6853 Command Register and causes the Transmitter to send continuous "BREAK" characters after both the transmitter and transmitter-holding registers have been emptied. When the Command Register is programmed back to normal transmit mode, a Stop Bit is generated and normal transmission continues.

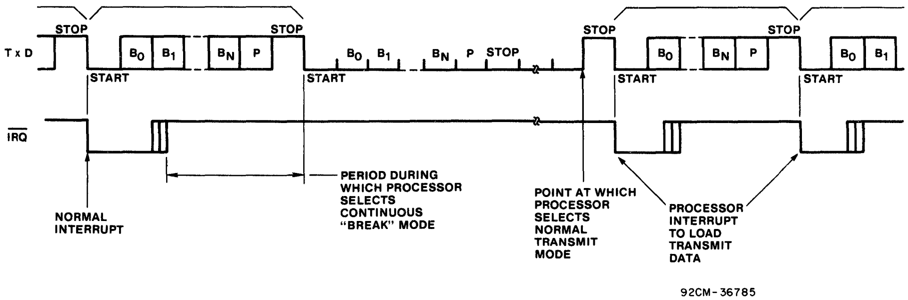

STOP
STOP
STOP
STOP
TxD
B0
B1
BN
P
START
IRQ
PERIOD DURING WHICH PROCESSOR SELECTS CONTINUOUS "BREAK" MODE
NORMAL INTERRUPT
POINT AT WHICH PROCESSOR SELECTS NORMAL TRANSMIT MODE
PROCESSOR INTERRUPT TO LOAD TRANSMIT DATA
92CM-36785

Fig. 19 - Transmit continuous "BREAK".

Receive Continuous "BREAK" (Fig. 20)

In the event the modem transmits continuous "BREAK" characters, the CDP6853 will terminate receiving. Reception will resume only after a Stop Bit is encountered by the CDP6853.

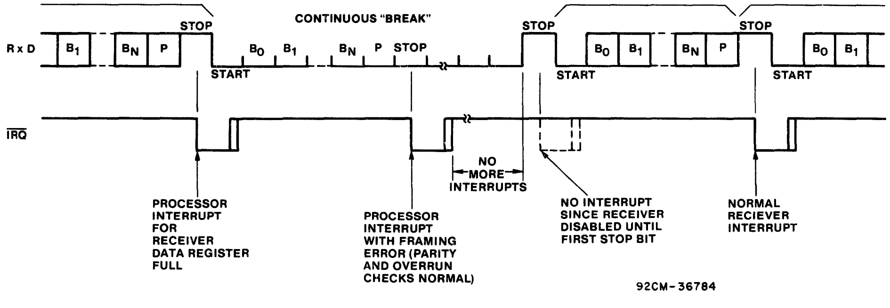

CONTINUOUS "BREAK"
STOP
STOP
STOP
RxD
B0
B1
BN
P
START
IRQ
NO MORE INTERRUPTS
PROCESSOR INTERRUPT FOR RECEIVER DATA REGISTER FULL
PROCESSOR INTERRUPT WITH FRAMING ERROR (PARITY AND OVERRUN CHECKS NORMAL)
NO INTERRUPT SINCE RECEIVER DISABLED UNTIL FIRST STOP BIT
NORMAL RECIEVER INTERRUPT
92CM-36784

Fig. 20 - Receive continuous "BREAK".

CDP6853 OPERATION (Cont'd)

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the CDP6853 should be interrogated, as follows:

1. Read Status Register

   This operation automatically clears Bit 7 (IRQ). Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.

2. Check IRQ Bit

   If not set, interrupt source is not the CDP6853.

3. Check $\overline{DCD}$ and $\overline{DSR}$

   These must be compared to their previous levels, which must have been saved by the processor. If they are both "0" (modem "on-line") and they are unchanged then the remaining bits must be checked.

4. Check RDRF (Bit 3)

   Check for Receiver Data Register Full.

5. Check Parity, Overrun, and Framing Error (Bits 0-2)

   Only if Receiver Data Register is Full.

6. Check TDRE (Bit 4)

   Check for Transmitter Data Register Empty.

7. If none of the above, then $\overline{CTS}$ must have gone to the FALSE (high) state.

PROGRAMMED RESET OPERATION

A program reset occurs when the processor performs a write operation to the CDP6853 with AD0 high and AD1 low. The program reset operates somewhat different from the hardware reset ($\overline{RES}$ pin) and is described as follows:

1. Internal registers are not completely cleared. The data sheet indicates the effect of a program reset on internal registers.
2. The $\overline{DTR}$ line goes high immediately.
3. Receiver and transmitter interrupts are disabled immediately. If $\overline{IRQ}$ is low when the reset occurs, it stays low until serviced, unless interrupt was caused by $\overline{DCD}$ or $\overline{DSR}$ transition.
4. $\overline{DCD}$ and $\overline{DSR}$ interrupts disabled immediately. If $\overline{IRQ}$ is low and was caused by $\overline{DCD}$ or $\overline{DSR}$, then it goes high, also $\overline{DCD}$ and $\overline{DSR}$ status bits subsequently will follow the input lines, although no interrupt will occur.
5. Overrun cleared, if set.

MISCELLANEOUS NOTES ON OPERATION

1. If Echo Mode is selected, $\overline{RTS}$ goes low.
2. If Bit 0 of Command Register is "0" (disabled), then:
   a) All interrupts disabled, including those caused by $\overline{DCD}$ and $\overline{DSR}$ transitions.
   b) Receiver disabled, but a character currently being received will be completed first.
   c) Transmitter is disabled after both the Transmit Data and Transmit Shift Registers have been emptied
3. Odd parity occurs when the sum of all the "1" bits in the data word (including the parity bit) is odd.
4. In the receive mode, the received parity bit does not go into the Receiver Data Register, but is used to generate parity error for the Status Register.
5. Transmitter and Receiver may be in full operation simultaneously. This is "full-duplex" mode.
6. If the RxD line inadvertently goes low and then high during the first 9 receiver clocks after a Stop Bit; will result in a false Start Bit.

   For false Start Bit detection, the CDP6853 does not begin to receive data, instead, only a true Start Bit initiates receiver operation.

7. Precautions to consider with the crystal oscillator circuit:

   The XTLI input may be used as an external clock input. The XTLO pin must be floating and may not be used for any other function.

8. $\overline{DCD}$ and $\overline{DSR}$ transitions, although causing immediate processor interrupts, have no effect on transmitter operation. Data will continue to be sent, unless the processor forces transmitter to turn off. Since these are high-impedance inputs, they must not be permitted to float (un-connected). If unused, they must be terminated either to GND or V_{DD}.

GENERATION OF NON-STANDARD BAUD RATES

Divisors

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the CDP6853 Control Register.

The divisors, then, are determined by bits 0-3 in the Control Register and their values are shown in Table II.

Generating Other Baud Rates

By using a different crystal, other baud rates may be generated. These can be determined by:

$$\text{Baud Rate} = \frac{\text{Crystal Frequency}}{\text{Divisor}}$$

Furthermore, it is possible to drive the CDP6853 with an off-chip oscillator to achieve the same thing. In this case, XTLI (pin 6) must be the clock input and XTLO (pin 7) must be a no-connect.

DIAGNOSTIC LOOP-BACK OPERATING MODES

A simplified block diagram for a system incorporating a CDP6853 ACIA is shown in Fig. 21.

Occasionally it may be desirable to include in the system a facility for "loop-back" diagnostic testing, of which there are two kinds:

1. Local Loop-Back

   Loop-back from the point of view of the processor. In this case, the Modem and Data Link must be effectively disconnected and the ACIA transmitter connected back to its own receiver, so that the processor can perform diagnostic checks on the system, excluding the actual data channel.

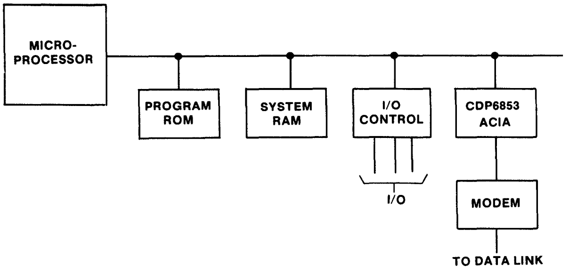
2. Remote Loop-Back

   Loop-back from the point of view of the Data Link and Modem. In this case, the processor, itself, is disconnected and all received data is immediately retransmitted, so the system on the other end of the Data Link may operate independent of the local system.

CDP6853 OPERATION (Cont'd)

Table II - Divisor Selection for the CDP6853

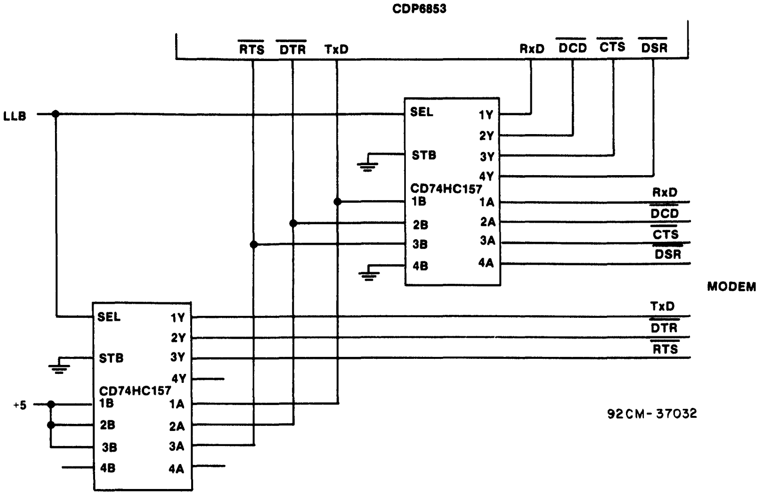
CONTROL REGISTER BITS				DIVISOR SELECTED FOR THE INTERNAL COUNTER	BAUD RATE GENERATED WITH 1.8432 MHz CRYSTAL	BAUD RATE GENERATED WITH A CRYSTAL OF FREQUENCY (F)
3	2	1	0			
0	0	0	0	No Divisor Selected	1/16 of External Clock at Pin XTLI	1/16 of External Clock at Pin XTLI
0	0	0	1	36,864	$\frac{1.8432 \times 10^6}{36{,}864} = 50$	$\frac{F}{36{,}864}$
0	0	1	0	24,576	$\frac{1.8432 \times 10^6}{24{,}576} = 75$	$\frac{F}{24{,}576}$
0	0	1	1	16,768	$\frac{1.8432 \times 10^6}{16{,}768} = 109.92$	$\frac{F}{16{,}768}$
0	1	0	0	13,696	$\frac{1.8432 \times 10^6}{13{,}696} = 134.58$	$\frac{F}{13{,}696}$
0	1	0	1	12,288	$\frac{1.8432 \times 10^6}{12{,}288} = 150$	$\frac{F}{12{,}288}$
0	1	1	0	6,144	$\frac{1.8432 \times 10^6}{6{,}144} = 300$	$\frac{F}{6{,}144}$
0	1	1	1	3,072	$\frac{1.8432 \times 10^6}{3{,}072} = 600$	$\frac{F}{3{,}072}$
1	0	0	0	1,536	$\frac{1.8432 \times 10^6}{1{,}536} = 1200$	$\frac{F}{1{,}536}$
1	0	0	1	1,024	$\frac{1.8432 \times 10^6}{1{,}024} = 1800$	$\frac{F}{1{,}024}$
1	0	1	0	768	$\frac{1.8432 \times 10^6}{768} = 2400$	$\frac{F}{768}$
1	0	1	1	512	$\frac{1.8432 \times 10^6}{512} = 3600$	$\frac{F}{512}$
1	1	0	0	384	$\frac{1.8432 \times 10^6}{384} = 4800$	$\frac{F}{384}$
1	1	0	1	256	$\frac{1.8432 \times 10^6}{256} = 7200$	$\frac{F}{256}$
1	1	1	0	192	$\frac{1.8432 \times 10^6}{192} = 9600$	$\frac{F}{192}$
1	1	1	1	96	$\frac{1.8432 \times 10^6}{96} = 19200$	$\frac{F}{96}$



92CS-37022

Fig. 21 - Simplified system diagram.

CDP6853 OPERATION (Cont'd)



NOTES: 1. HIGH ON LLB SELECTS LOCAL LOOP-BACK MODE.
2. HIGH ON CD74HC157 SELECT INPUT GATES "B" INPUTS TO "Y" OUTPUTS; LOW GATES "A" TO "Y".

Fig. 22 - Loop-back circuit schematic.

The CDP6853 does not contain automatic loop-back operating modes, but they may be implemented with the addition of a small amount of external circuitry.

Fig. 22 indicates the necessary logic to be used with the CDP6853.

The LLB line is the positive-true signal to enable local loop-back operation. Essentially, LLB=high does the following:

1. Disables outputs TxD, $\overline{DTR}$, and $\overline{RTS}$ (to Modem).
2. Disables inputs RxD, $\overline{DCD}$, $\overline{CTS}$, $\overline{DSR}$ (from Modem).
3. Connects transmitter outputs to respective receiver inputs:
   a) TxD to RxD
   b) $\overline{DTR}$ to $\overline{DCD}$
   c) $\overline{RTS}$ to $\overline{CTS}$

LLB may be tied to a peripheral control pin to provide processor control of local loop-back operation. In this way, the processor can easily perform local loop-back diagnostic testing.

Remote loop-back does not require this circuitry, so LLB must be set low. However, the processor must select the following:

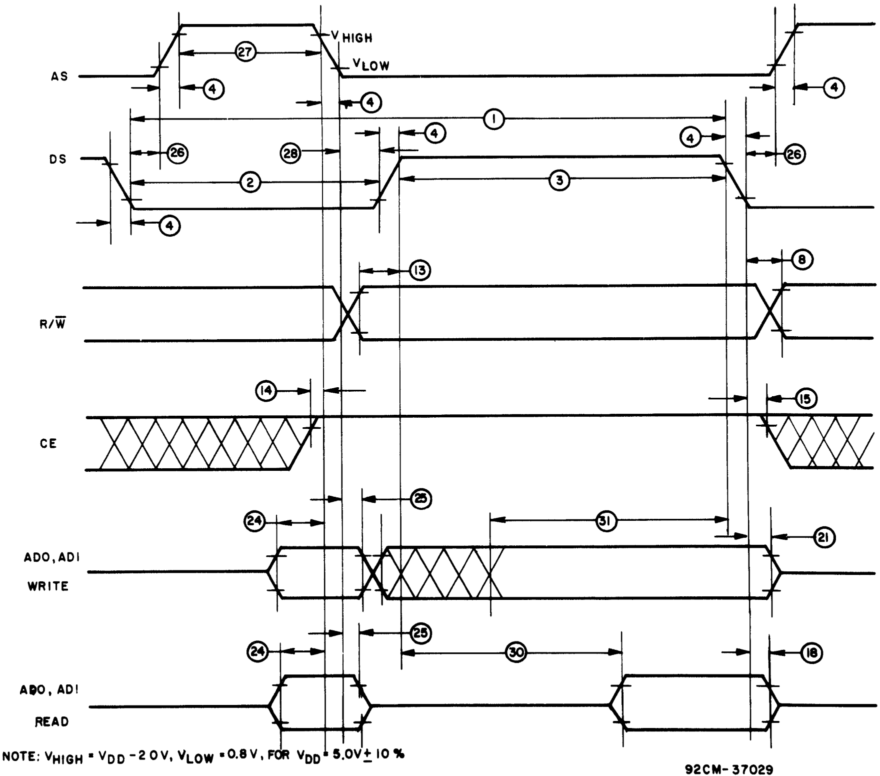
1. Control Register bit 4 must be "1", so that the transmitter clock=receiver clock.
2. Command Register bit 4 must be "1" to select Echo Mode.
3. Command Register bits 3 and 2 must be "1" and "0", respectively, to disable transmitter interrupts.
4. Command Register bit 1 must be "0" to disable receiver interrupts.

In this way, the system re-transmits received data without any effect on the local system.

DYNAMIC ELECTRICAL CHARACTERISTICS—BUS TIMING, V_{DD} = 5 V dc ± 5%, V_{SS} = 0 V dc, T_A = -40 to +85° C, C_L = 75 pF, See Figs. 23, 24, 25.

IDENT. NUMBER	CHARACTERISTIC		LIMITS						UNITS
			CDP6853-1		CDP6853-2		CDP6853-4		
			Min.	Max.	Min.	Max.	Min.	Max.	
1	Cycle Time	t_{CYC}	953	DC	500	DC	250	DC	ns
2	Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High	PW_{EL}	300	—	125	—	90	—	
3	Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low	PW_{EH}	325	—	145	—	70	—	
4	Clock Rise and Fall Time	t_r, t_f	—	30	—	30	—	30	
8	R/$\overline{W}$ Hold Time	t_{RWH}	10	—	10	—	5	—	
13	R/W Set-up Time Before DS/E	t_{RWS}	15	—	10	—	5	—	
14	Chip Enable Set-up Time Before AS/ALE Fall	t_{CS}	55	—	20	—	10	—	
15	Chip Enable Hold Time	t_{CH}	0	—	0	—	0	—	
18	Read Data Hold Time	t_{DHR}	10	100	10	40	10	20	
21	Write Data Hold Time	t_{DHW}	0	—	0	—	0	—	
24	Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	50	—	20	—	10	—	
25	Muxed Address Hold Time	t_{AHL}	50	—	15	—	5	—	
26	Delay Time, DS/E to AS/ALE Rise	t_{ASD}	50	—	0	—	0	—	
27	Pulse Width, AS/ALE High	PW_{ASH}	100	—	45	—	20	—	
28	Delay Time, AS/ALE to DS/E Rise	t_{ASED}	90	—	20	—	10	—	
30	Peripheral Output Data Delay Time From DS/E or $\overline{RD}$	t_{DDR}	20	240	10	70	5	35	
31	Peripheral Data Set-up Time	t_{DSW}	220	—	110	—	55	—	

NOTE: Designations E, ALE, RD and WR refer to signals from non-6805 type microprocessors.



NOTE: $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V, FOR $V_{DD} = 5.0$V ± 10 %

92CM-37029

Fig. 23 - Bus timing waveforms of CDP6853.

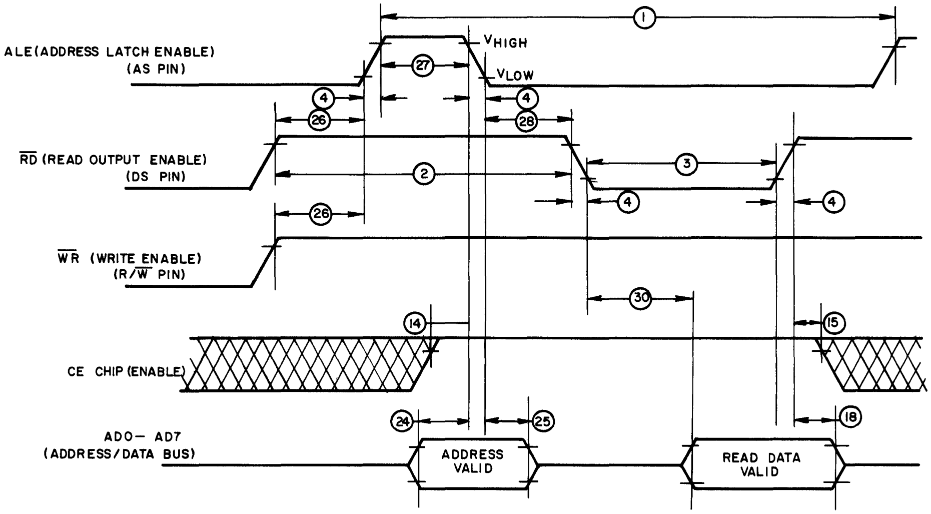
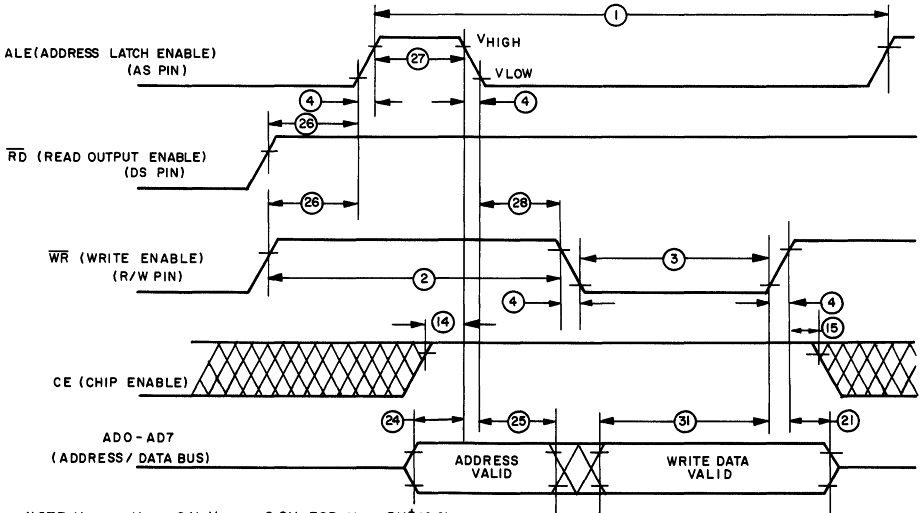


Fig. 24 - Bus-read timing waveforms of 8085 multiplexed bus. 92CM-37031



NOTE: $V_{HIGH} = V_{DD} - 2\text{ V}$, $V_{LOW} = 0.8\text{V}$, FOR $V_{DD} = 5\text{V} \pm 10\%$

92CM-37030

Fig. 25 - Bus-write timing waveforms of 8085 multiplexed bus.

DYNAMIC ELECTRICAL CHARACTERISTICS - TRANSMIT/RECEIVE, See Figs. 26, 27 and 28.
V_{DD} = 5 V ± 5%, T_A = -40° to +85°C

CHARACTERISTIC		LIMITS						UNITS
		CDP6853-1		CDP6853-2		CDP6853-4		
		Min.	Max.	Min.	Max.	Min.	Max.	
Transmit/Receive Clock Rate	t_{CCY}	400*	—	325	—	250	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	145	—	110	—	
Transmit/Receive Clock Low Time	t_{CL}	175	—	145	—	110	—	
XTLI to TxD Propagation Delay	t_{DD}	—	500	—	410	—	315	
$\overline{\text{RTS}}$ Propagation Delay	t_{DLY}	—	500	—	410	—	315	
$\overline{\text{IRQ}}$ Propagation Delay (Clear)	$t_{\overline{IRQ}}$	—	500	—	410	—	315	
$\overline{\text{RES}}$ Pulse Width	$t_{\overline{RES}}$	400	—	300	—	200	—	

(t_r,t_f = 10 to 30 ns)
*The baud rate with external clocking is: $\text{Baud Rate} = \frac{1}{16 \times T_{CCY}}$

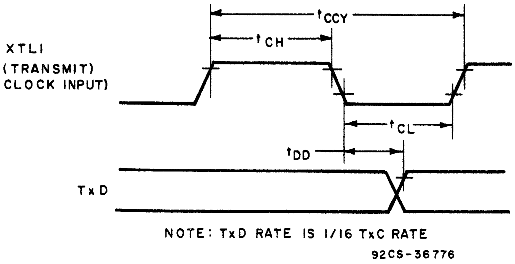


Fig. 26 - Transmit-timing waveforms with external clock.

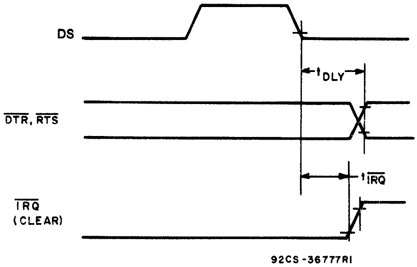


Fig. 27 - Interrupt- and output-timing waveforms.

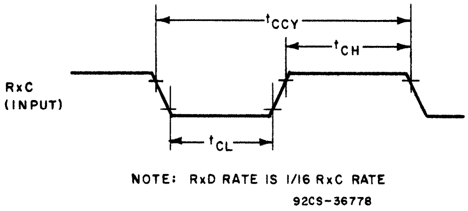


Fig. 28 - Receive external clock timing waveforms.

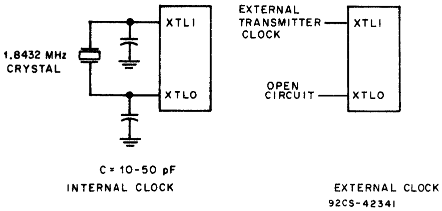


Fig. 29 - Transmitter clock generation.

CMOS Random-Access Memories (RAMs)

Technical Data

RCA offers a large selection of fully static CMOS random-access-memories (RAMs) with densities from 32K-bytes down to 32-bytes. These RAMs feature low standby current, 2-volt minimum memory data retention for battery backup, and CDP1800-series compatible parts.

Industry-standard pinout devices are represented by the MWS- and CDM- series prefixes.

The folowing pages contain Cross-Reference Guides for the CDM- series of 16K, 64K, and 256K static CMOS RAMs.

RAM Cross-Reference Guide

16K RAMS

Note: An RCA equivalent type may not be identical with other manufacturer's type in every detail.
Refer to published data for further information.

RCA 2048X8 CMOS STATIC RAM COMPARISON CHART (b)

Mfr.	Type	Access Time (nS)	Standby Current		RCA Nearest Equivalent Type*
			CMOS (μA)	TTL (mA)	
FUJITSU	MB8416	200	10	2	CDM6116A-2
	MB8416-X	200	10	2	CDM6116A-9
	MB8416A-12	120			CDM6116A-3
	MB8416A-15	150			CDM6116A-3
HARRIS	HM65162-5	90	100	8	CDM6116A-3
	HM65162-9	90	100	9	CDM6116A-9
	HM65162S-5	55	100	8	CDM6116A-3
	HM65162S-9	55	100	9	CDM6116A-9
	HM65162B-5	70	50	8	CDM6116A-3
	HM65162B-9	70	50	9	CDM6116A-9
	HM65162C-9	90	1000	9	CDM6116A-9
HITACHI	HM6116P-2	120	2000	15	CDM6116A-3
	HM6116P-3	150	2000	15	CDM6116A-3
	HM6116P-4	200	2000	15	CDM6116A-2
	HM6116I/PI-2	120	2000	20	CDM6116A-9
	HM6116I/PI-3	150	2000	20	CDM6116A-9
HITACHI	HM6116I/PI-4	200	2000	20	CDM6116A-9
	HM6116LI-2	120	200	20	CDM6116A-9
	HM6116LI-3	150	200	20	CDM6116A-9
	HM6116LI-4	200	200	20	CDM6116A-9
	HM6116LP-2	120	50	12	CDM6116A-3
	HM6116LP-3	150	50	12	CDM6116A-3
	HM6116LP-4	200	50	12	CDM6116A-2
	HM6116LPI-2	120	100	20	CDM6116A-9
	HM6116LPI-3	150	100	20	CDM6116A-9
	HM6116LPI-4	200	100	20	CDM6116A-9
	HM6116AP-10	100	2000	4	CDM6116A-3
	HM6116AP-12	120	2000	4	CDM6116A-3
	HM6116AP-15	150	2000	4	CDM6116A-3
	HM6116AP-20	200	2000	4	CDM6116A-2
	HM6116ALP-10	100	50	3	CDM6116A-3
	HM6116ALP-12	120	50	3	CDM6116A-3
	HM6116ALP-15	150	50	3	CDM6116A-3
	HM6116ALP-20	200	50	3	CDM6116A-2

*Determine the appropriate package designator (suffix letter) from the RCA Data Sheet

RCA 2048 X 8 CMOS STATIC RAMS (b)

RCA Type (a) (All 24 Pin Packages)	Operating Supply Voltage Range	Electrical Characteristic Temperature Range	Address Access Time (nS)	Chip Enable Access Time (nS)	Standby Current		Data Retention Current (3V) (μA)	Operating Supply Current (d) (mA)	TTL Compatible? (c)
					CMOS (μA)	TTL (mA)			
CDM6116A-2	4 5-5 5V	0° to 70°C	200	200	30	2	15	35	Yes
CDM6116A-3	4 5-5 5V	0° to 70°C	150	150	50	2	25	35	Yes
CDM6116A-9	4 5-5 5V	-40 to 85°C	250	250	100	2	50	40	Yes

(a) D suffix added for ceramic package, E suffix for plastic All RCA RAMS shown are asynchronous types
(b) Specifications at Vdd = 5V unless otherwise noted
(c) Noise immunity levels VIL = 0 8V, VIH = 2.2V.
(d) Outputs open circuited Cycle Time = Min tcycle, $V_{IN} = V_{IL}, V_{IH}$

RAM Cross-Reference Guide

16K RAMS

Note: An RCA equivalent type may not be identical with other manufacturer's type in every detail.
Refer to published data for further information.

RCA 2048 X 8 CMOS STATIC RAM COMPARISON CHART (b)

Mfr.	Type	Access Time (nS)	Standby Current		RCA Nearest Equivalent Type*
			CMOS (µA)	TTL (mA)	
IDT	IDT6116S70	70	2000	15	CDM6116A-3
	IDT6116S90	90	2000	15/20	CDM6116A-3/A-9
	IDT6116S120	120	2000	15/20	CDM6116A-3/A-9
	IDT6116S150	150	2000	20	CDM6116A-9
	IDT6116L90	90	100/200	15/20	CDM6116A-3/A-9
	IDT6116L120	120	100/200	12/15	CDM6116A-3/A-9
	IDT6116L150	150	100/200	12	CDM6116A-3/A-9
NEC	µPD446-3	150	10		CDM6116A-3/A-9
	µPD446-2	200	10		CDM6116A-3/A-9
	µPD446-1	250	10		CDM6116A-9
	µPD446	450	10		CDM6116A-9
OKI	MSM5128-12	120	50	7	CDM6116A-3/A-9
	MSM5128-15	150	50	7	CDM6116A-3/A-9
	MSM5128-20	200	50	7	CDM6116A-3/A-9

Mfr.	Type	Access Time (nS)	Standby Current		RCA Nearest Equivalent Type*
			CMOS (µA)	TTL (mA)	
SMOS	SRM2016C15	150	50	2	CDM6116A-3
	SRM2016C20	200	50	2	CDM6116A-2
	SRM2016C25	250	50	2	CDM6116A-2
SSS	SCM6116-1	100	2000	12	CDM6116A-3
	SCM6116-2	120	2000	12	CDM6116A-3
	SCM6116-3	150	2000	12	ODM6116A-3
	SCM6116L-1	100	50	12	CDM6116A-3
	SCM6116L-2	120	50	12	CDM6116A-3
	SCM6116L-3	150	50	12	CDM6116A-3
TOSHIBA	TC5517AP	250	30	3	CDM6116A-2
	TC5517AP-2	200	30	3	CDM6116A-2/A-9
	TC5517APL	250	1@60°C	3	CDM6116A-9
	TC5517APL-2	200	1@60°C	3	CDM6116A-2/A-9
	TC5517BP-20	200	30	3	CDM6116A-2/A-9
	TC5517BPL-20	200	1@60°C	3	CDM6116A-2/A-3

*Determine the appropriate package designator (suffix letter) from the RCA Data Sheet

RCA 2048 X 8 CMOS STATIC RAMS (b)

RCA Type (a) (All 24 Pin Packages)	Operating Supply Voltage Range	Electrical Characteristic Temperature Range	Address Access Time (nS)	Chip Enable Access Time (nS)	Standby Current		Data Retention Current (3V) (µA)	Operating Supply Current (d) (mA)	TTL Compatible? (c)
					CMOS (µA)	TTL (mA)			
CDM6116A-2	4 5-5.5V	0° to 70°C	200	200	30	2	15	35	Yes
CDM6116A-3	4 5-5 5V	0° to 70°C	150	150	50	2	25	35	Yes
CDM6116A-9	4 5-5 5V	-40 to 85°C	250	250	100	2	50	40	Yes

(a) D suffix added for ceramic package, E suffix for plastic All RCA RAMS shown are asynchronous types
(b) Specifications at Vdd = 5V unless otherwise noted
(c) Noise immunity levels VIL = 0 8V, VIH = 2.2 V.
(d) Outputs open circuited Cycle Time = Min tcycle, $V_{IN} = V_{IL}, V_{IH}$

RAM Cross-Reference Guide

64K RAMs

Note: An RCA equivalent type may not be identical with other manufacturer's type in every detail. Refer to published data for further information.

RCA 8192 x 8 CMOS STATIC RAM COMPARISON CHART (b)

Mfr.	Type	Access Time (ns)	Standby Current		GE/RCA Nearest Equivalent Type*		Mfr.	Type	Access Time (ns)	Standby Current		GE/RCA Nearest Equivalent Type*
			CMOS (µA)	TTL (mA)						CMOS (µA)	TTL (mA)	
AMD	AM99CL88-15	150	100	1	CDM6264-3		NEC	µPD4464-15	150	10		CDM6264.3
								µPD4464-20	200	10		CDM6264-3
FUJITSU	MB8464-15	150	2000		CDM6264-3							
	MB8464-15L	150	200		CDM6264-3		S-MOS	SRM2064C-15	150	100	3	CDM6264-3
HITACHI	HM6264-15	150	2000	3	CDM6264-3		TOSHIBA	TC5564PL-15	150	1 @ 60° C	2	CDM6264-2I
	HM6264LP-15	150	100	3	CDM6264-3			TC5564PL-20	200	1 @ 60° C	2	CDM6264-2I
								TC5565PL-15	150	100	3	CDM6264-3

*Determine the appropriate package designator (suffix letter) from the RCA Data Sheet.

RCA 8192 x 8 CMOS STATIC RAMs (b)

RCA Type (a) (All 28-Pin Packages)	Operating Supply Voltage Range	Electrical Characteristic Temperature Range	Address Access Time (ns)	Chip Enable Access Time (ns)	Standby Current		Data Retention Current (3 V) (µA)	Operating Supply Current (d) (mA)	TTL Compatible? (c)
					CMOS (µA)	TTL (mA)			
CDM6264-3	4.5-5.5 V	0° TO 70° C	150	150	100	3	50	45	YES
CDM6264-2I	4.5-5.5 V	-40° TO +85° C	200	200	200	4	100	45	YES

(a) D suffix added for ceramic package. E suffix for plastic. All RCA RAMs shown are asynchronous types.

(b) Specifications at V_{DD} = 5 V unless otherwise noted.

(c) Noise immunity levels V_{IL} = 0.8 V, V_{IH} = 2.2 V.

(d) Outputs open circuited. Cycle Time = Min. t_{cycle}; V_{IN} = V_{IL}, V_{IH}.

RAM Cross-Reference Guide

256K RAMs

Note: An RCA equivalent type may not be identical with other manufacturer's type in every detail.
Refer to published data for further information.

RCA 32,768 x 8 CMOS STATIC RAM COMPARISON CHART (b)

Mfr.	Type	Access Time (ns)	Standby Current		GE/RCA Nearest Equivalent Type*	Mfr.	Type	Access Time (ns)	Standby Current		GE/RCA Nearest Equivalent Type*
			CMOS (μA)	TTL (mA)					CMOS (μA)	TTL (mA)	
TOSHIBA	TC55257P-10	100	1000	3	CDM62256-10	NEC	μPD43256-10	100	2000		CDM62256-10
	TC55257P-12	120	1000	3	CDM62256-10		μPD43256-10L	100	100		CDM62256-10
	TC55257PL-10	100	100	3	CDM62256-10						
	TC55257PL-12	120	100	3	CDM62256-10	S-MOS	SRM20256C-10	100	100	3	CDM62256-10
FUJITSU	MB84256-10	100	1000	3	CDM62256-10						
	MB84256-12	120	1000	3	CDM62256-10						
	MB84256-10L	100	100	3							
	MB84256-12L	120	100	3							
HITACHI	HM62256P-10	100	2000	3	CDM62256-10						
	HM62256P-12	120	2000	3	CDM62256-10						
	HM62256P-15	150	2000	3	CDM62256-10						
	HM62256LP-10	100	100	3	CDM62256-10						
	HM62256LP-12	120	100	3	CDM62256-10						
	HM62256LP-15	150	100	3	CDM62256-10						

*Determine the appropriate package designator (suffix letter) from the RCA Data Sheet.

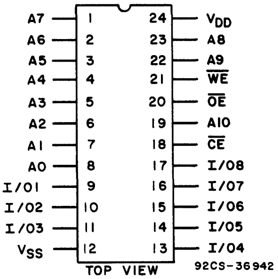
RCA 32,768 x 8 CMOS STATIC RAMs (b)

RCA Type (a) (All 28-Pin Packages)	Operating Supply Voltage Range	Electrical Characteristic Temperature Range	Address Access Time (ns)	Chip Enable Access Time (ns)	Standby Current		Data Retention Current (3 V) (μA)	Operating Supply Current (d) (mA)	TTL Compatible? (c)
					CMOS (μA)	TTL (mA)			
CDM6264-10	4.5-5.5 V	0° TO 70°C	100	100	100	3	50	70	YES
CDM6264-10I	4.5-5.5 V	-40° TO +85°C	100	100	200	3	100	70	YES
CDM6264-12I	4.5-5.5 V	-40° TO +85°C	120	120	200	3	100	70	YES

(a) D suffix added for ceramic package. E suffix for plastic. All RCA RAMs shown are asynchronous types.
(b) Specifications at V_{DD} = 5 V unless otherwise noted.
(c) Noise immunity levels V_{IL} = 0.8 V, V_{IH} = 2.2 V.
(d) Outputs open circuited. Cycle Time = Min. t_{cycle}; $V_{IN} = V_{IL}, V_{IH}$.

CDM6116A

Product Preview



TERMINAL ASSIGNMENT

CMOS 2048-Word by 8-Bit Static RAM

Features:

- *Fully static operation*
- *Single power supply: 4.5 V to 5.5 V*
- *All inputs and outputs directly TTL compatible*
- *3-state outputs*
- *Industry standard 24-pin configuration*
- *Chip-enable gates address buffers for minimum standby current*
- *Data retention voltage: 2 V min.*

The RCA-CDM6116A is a CMOS 2048-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This device has common data inputs and data outputs and utilizes a single power supply of 4.5 V to 5.5 V. A chip-enable input and an output-enable input are provided for memory expansion and output buffer control.

The chip enable ($\overline{CE}$) gates the address and output buffers and powers down the chip to the low power standby mode.

The output enable ($\overline{OE}$) controls the output buffers to eliminate bus contention.

The CDM6116A-2 and CDM6116A-3 are supplied in a 24-lead dual-in-line plastic package (E suffix). The CDM-6116A-9 is supplied in a 24-lead dual-in-line plastic package (E suffix) and a 24-lead dual-in-line side-brazed ceramic package (D suffix).

	CDM6116A-2	CDM6116A-3	CDM6116A-9
Access Time (max.)	200 ns	150 ns	250 ns
Output Enable Time (max.)	120 ns	60 ns	150 ns
Operating Temperature	0° to +70° C		-40° to +85° C
Operating Current (max.)	35 mA	35 mA	40 mA
Standby Current I_{DDS1} (max.)	30 μA	50 μA	100 μA

OPERATING CONDITIONS at T_A = 0 to +70° C, (CDM6116A-2, CDM6116A-3); T_A = -40° to +85° C (CDM6116A-9)
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS ALL TYPES		UNITS
		MIN.	MAX.	
DC Operating Voltage Range		4.5	5.5	V
Input Voltage Range	V_{IH}	2.2	V_{DD} + 0.3	
	V_{IL}	-0.3	0.8	
Input Signal Rise or Fall Time Δ	t_r, t_f	—	5	μs

Δ Input signal rise and fall times longer than the maximum value can cause loss of stored data in the selected mode.

File Number **1472**

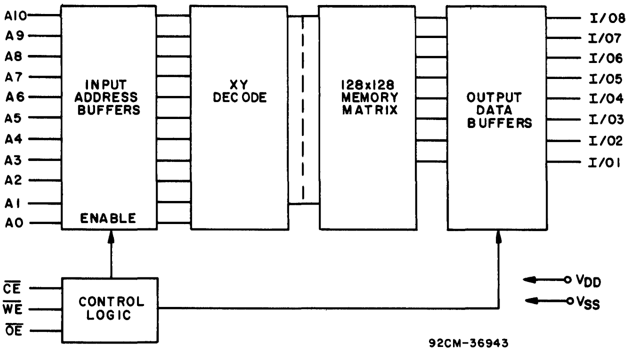


Fig. 1 - Functional block diagram.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0 TO A10	MODE	I/01 TO I/08	DEVICE CURRENT
H	X	X	X	NOT SELECTED	HIGH Z	STANDBY
L	L	H	STABLE	READ	DATA OUT	ACTIVE
L	H	L	STABLE	WRITE	DATA IN	ACTIVE
L	L	L	STABLE	WRITE	DATA IN	ACTIVE

L = LOW H = HIGH X = H or L

MAXIMUM RATINGS, *Absolute-Maximum Ratings*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):	
(Voltage referenced to V_{SS} terminal)	-0.3 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.3 to +7 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40° to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60° to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40° to +85° C (PACKAGE TYPE D)	500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
CDM6116A-2, CDM6116A-3 (PACKAGE TYPE E)	0 to +70° C
CDM6116A-9 (PACKAGE TYPES D, E)	-40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg})	-55 to +125° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to +70° C (CDM6116A-2, CDM6116A-3); T_A = -40° to +85° C (CDM6116A-9), V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC	CONDITIONS	LIMITS									UNITS
		CDM6116A-2			CDM6116A-3			CDM6116A-9			
		MIN.	TYP.•	MAX.	MIN.	TYP.•	MAX.	MIN.	TYP.•	MAX.	
Standby Device Current I_{DDS}	$\overline{CE} = V_{IH}$	—	0.6	2	—	0.6	2	—	0.3	2	mA
I_{DDS1}	$\overline{CE} = V_{DD}$–0.2 V	—	1	30	—	1	50	—	1	100	μA
Output Voltage Low Level V_{OL} Max.	I_{OL} = 2.1 mA	—	—	0.4	—	—	0.4	—	—	0.4	V
	I_{OL} = 1 μA	—	0.1	—	—	0.1	—	—	0.1	—	
Output Voltage High Level V_{OH} Min.	I_{OH} = -1 mA	2.4	—	—	2.4	—	—	2.4	—	—	V
	I_{OH} = -1 μA	—	V_{DD}-0.1	—	—	V_{DD}-0.1	—	—	V_{DD}-0.1	—	
Input Leakage Current I_{IN} Max.	V_{DD} = 5.5 V V_{IN} = 0 V to V_{DD}	—	±0.1	±2	—	±0.1	±2	—	±0.1	±2	μA
3-State Output Leakage Current I_{OUT}	$\overline{CE}$ or $\overline{OE} = V_{IH}$ $V_{I/O}$ = 0 V to V_{DD}	—	±0.5	±2	—	±0.5	±2	—	±0.5	±2	
Operating Device Current I_{OPER}#	$V_{IN} = V_{IL}, V_{IH}$	—	20	35	—	20	35	—	28	40	mA
Input Capacitance C_{IN}	V_{IN} = 0 V, f = 1 MHz, T_A = 25° C	—	4	6	—	4	6	—	4	6	pF
Output Capacitance $C_{I/O}$	$V_{I/O}$ = 0 V, f = 1 MHz, T_A = 25° C	—	6	8	—	6	8	—	6	8	

•Typical values are for T_A = 25° C and nominal V_{DD}.

#Outputs open circuited; cycle time = Min. t_{cycle}, duty = 100%.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0 to +70° C (CDM6116A-2, CDM6116A-3); T_A = -40° to +85° C (CDM6116A-9), V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns; C_L = 100 pF and 1 TTL Load, Input Pulse Levels: 0.8 V to 2.4 V

CHARACTERISTIC **Read Cycle Times See Fig. 2**		LIMITS						UNITS
		CDM6116A-2		CDM6116A-3		CDM6116A-9		
		MIN.†	MAX.	MIN.†	MAX.	MIN.†	MAX.	
Read Cycle Time	t_{RC}	200	—	150	—	250	—	ns
Address Access Time	t_{AA}	—	200	—	150	—	250	
Chip Enable Access Time	t_{ACE}	—	200	—	150	—	250	
Chip Enable to Output Active	t_{CX}	15	—	15	—	15	—	
Output Enable to Output Valid	t_{OEV}	—	120	—	60	—	150	
Output Enable to Output Active	t_{OEX}	15	—	15	—	15	—	
Chip Disable to Output "High Z"	t_{CHZ}	0	60	0	50	0	80	
Output Disable to Output "High Z"	t_{OHZ}	0	60	0	50	0	80	
Output Hold from Address Change	t_{OH}	15	—	15	—	15	—	

†Time required by a limit device to allow for the indicated function.

SIGNAL DESCRIPTIONS

A0-A10 (Address Inputs): These inputs must be stable prior to a write operation, but may change asynchronously during read operations.

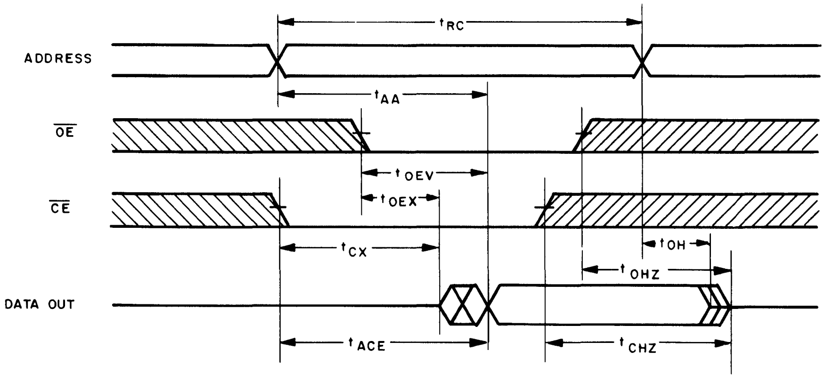
I/01-I/08: 8-bit tristate data bus.

$\overline{CE}$ (Chip Enable): Powers down chip, disables Read and Write functions, and gates off address inputs.

$\overline{OE}$ (Output Enable): Enables tristate outputs if $\overline{CE}$ is low and $\overline{WE}$ is high.

$\overline{WE}$ (Write Enable): Enables Write function, if $\overline{CE}$ is low. $\overline{WE}$ will dominate if both $\overline{WE}$ and $\overline{OE}$ are low (i.e., the bus will be tristated and a Write will occur).

V_{DD}, V_{SS}: Power supply connections.



$\overline{WE}$ IS HIGH DURING READ CYCLE
TIMING MEASUREMENT REFERENCE
LEVEL IS 1.5V

92CM-36944

Fig. 2 - Read-cycle timing waveforms

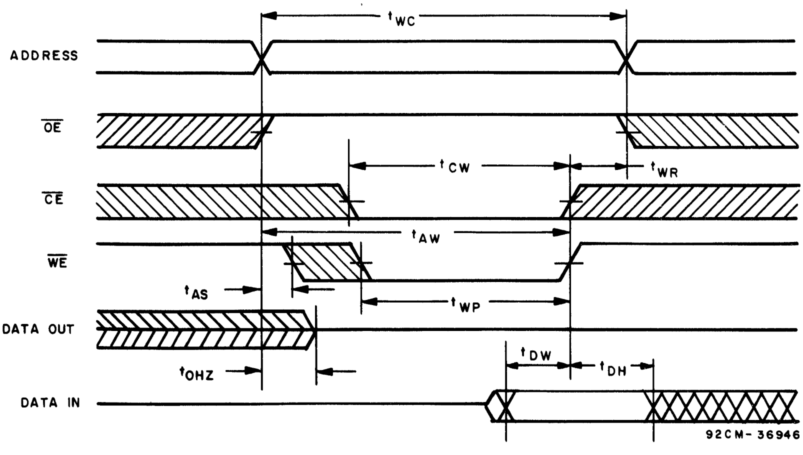
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0 to +70° C (CDM6116A-2, CDM6116A-3); T_A = -40° to +85° C (CDM6116A-9), V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns; C_L = 100 pF and 1 TTL Load, Input Pulse Levels: 0.8 V to 2.4 V

CHARACTERISTIC **Write Cycle Times See Fig. 3**		LIMITS						UNITS
		CDM6116A-2		CDM6116A-3		CDM6116A-9		
		MIN.†	MAX.	MIN.†	MAX.	MIN.†	MAX.	
Write Cycle Time	t_{WC}	200	—	150	—	250	—	ns
Chip Enable to End of WRITE	t_{CW}	160	—	90	—	200	—	
Address Valid to End of WRITE	t_{AW}	160	—	90	—	200	—	
Address Setup Time	t_{AS}	0	—	0	—	0	—	
Write Pulse Width	t_{WP}	160	—	90	—	200	—	
Write Recovery Time	t_{WR}	10	—	0	—	10	—	
Output Disable to Output "High Z"	t_{OHZ}	0	60	0	50	0	80	
Write to Output "High Z"	t_{WHZ}	0	60	0	40	0	80	
Input Data Setup Time	t_{DW}	80	—	50	—	100	—	
Input Data Hold Time	t_{DH}	10	—	5	—	10	—	
Output Active from End of Write	t_{OW}	10	—	10	—	10	—	

†Time required by a limit device to allow for the indicated function.

CDM6116A

WRITE CYCLE 1



WRITE CYCLE 2 - $\overline{OE}$ = LOW

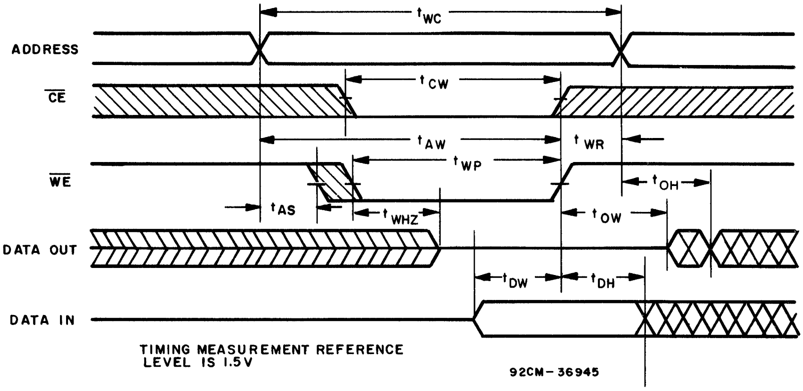


Fig. 3 - Write-cycle timing waveforms.

DATA RETENTION CHARACTERISTICS at T_A = 0 to 70° C (CDM6116A-2, CDM6116A-3); T_A = -40 to +85° C (CDM6116A-9), Unless otherwise noted, See Fig. 4.

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Minimum Data Retention Voltage V_{DR}	CDM6116A-2, CDM6116A-3	$\overline{CE} \geq V_{DD} - 0.2$ V	2	—	V
	CDM6116A-9	T_A = -40 to 0° C T_A = 0 to +85° C $\overline{CE} \geq V_{DD} - 0.2$ V	4.5 2	— —	
Data Retention Quiescent Current $I_{DD}DR$•	CDM6116A-2	V_{DD} = 3 V, $\overline{CE} \geq 2.8$ V	—	15	µA
	CDM6116A-3	V_{DD} = 3 V, $\overline{CE} \geq 2.8$ V	—	25	
	CDM6116A-9	T_A = 0 to +85° C V_{DD} = 3 V, $\overline{CE} \geq 2.8$ V	—	50	
Chip Disable to Data Retention Time t_{CDR}		See Fig. 4	0	—	ns
Recovery to Normal Operation Time t_R		See Fig. 4	*t_{RC}	—	

•$I_{DD}DR$ = 7.5 µA max. at T_A = 0 to +40° C for CDM6116A-2 and CDM6116A-3.

*t_{RC} = Read Cycle Time.

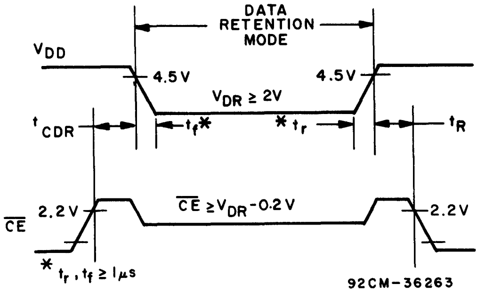
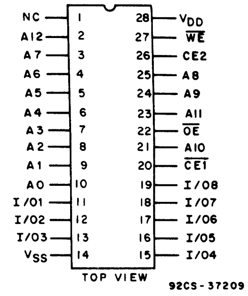


Fig. 4 - Low V_{DD} data retention timing waveforms.

CDM6264



TERMINAL ASSIGNMENT

CMOS 8192-Word by 8-Bit LSI Static RAM

Features:
- *Fully static operation*
- *Single power supply: 4.5 V to 5.5 V*
- *All inputs and outputs directly TTL compatible*
- *Industry standard 28-pin configuration*
- *Input address buffers gated off with chip disable*
- *3-state outputs*

The RCA-CDM6264 is a 8192-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This device has common data input and data output and utilizes a single power supply of 4.5 V to 5.5 V.

Either chip enable ($\overline{\text{CE1}}$ or CE2), when not valid, will gate off the address and output buffers and power down the chip to minimum standby power with inputs toggling. The output enable ($\overline{\text{OE}}$) controls the output buffers to eliminate bus contention.

The CDM6264 is supplied in a 28-lead dual-in-line plastic (E suffix) package.

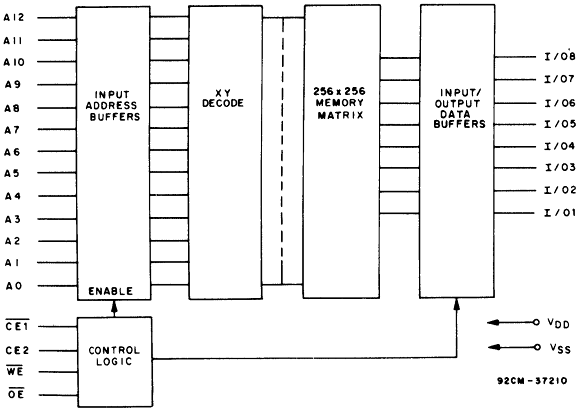


Fig. 1 - Functional block diagram.

	CDM6264-3	CDM6264-2I
Access Time (max)	150 ns	200 ns
Output Enable Time (max.)	70 ns	70 ns
Operating Current (max.)	45 mA	45 mA
Standby Current I_{DDS1} (max.)	100 μA	200 μA
Operating Temp. Range:	0°C to +70°C	-40°C to +85°C
Data Retention Voltage: $0°C \le T_A \le +70°C$ $0°C \le T_A \le +85°C$ $-40°C \le T_A < 0°C$	 2 V min — —	 — 2 V min 4 V min.

TRUTH TABLE

$\overline{\text{CE1}}$	CE2	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A0 TO A12	MODE	DATA I/O	DEVICE CURRENT
H	X	X	X	X	NOT SELECTED	HIGH Z	STANDBY
X	L	X	X	X	NOT SELECTED	HIGH Z	STANDBY
L	H	L	H	STABLE	READ	DATA OUT	ACTIVE
L	H	X	L	STABLE	WRITE	DATA IN	ACTIVE
L	H	H	H	STABLE	OUTPUT DISABLE	HIGH Z	ACTIVE

L = LOW H = HIGH X = H OR L

File Number **1505**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):	
(Voltage referenced to V_{SS} terminal)	-0.3 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.3 to +7 V
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40° to +60° C	500 mW
For T_A = +60° to +85° C	Derate linearly at 8 mW/° C to 300 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
CDM6264-3	0° to +70° C
CDM6264-2I	-40° to +85° C
STORAGE TEMPERATURE RANGE (T_{stg})	-55 to +125° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C

OPERATING CONDITIONS at T_A = 0° to +70° C (CDM6264-3); T_A = -40° to +85° C (CDM6264-2I)
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS ALL TYPES MIN.	MAX.	UNITS
DC Operating Voltage Range		4.5	5.5	V
Input Voltage Range	V_{IH}	2.2	V_{DD} + 0.3	
	V_{IL}	-0.3	0.8	
Input Signal Rise or Fall Time$^{\Delta}$	t_r, t_f	—	5	µs

ΔInput signal rise and fall times with a duration greater than the maximum value can cause loss of stored data in the selected mode.

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0° to +70° C (CDM6264-3); T_A = -40° to +85° C (CDM6264-2I), V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS	LIMITS CDM6264-3 Min.	Typ.•	Max.	CDM6264-2I Min.	Typ.•	Max.	UNITS
Standby Device Current	I_{DDS}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}	—	1.5	3	—	2	4	mA
	I_{DDS1}	$\overline{CE1}$=CE2 ≥ V_{DD}-0.2 V or CE2 ≤ 0.2 V	—	5	100	—	10	200	µA
Output Voltage Low Level	V_{OL} Max.	I_{OL}=2.1 mA	—	—	0.4	—	—	0.4	V
		I_{OL}=1 µA	—	0.1	—	—	0.1	—	
Output Voltage High Level	V_{OH} Min.	I_{OH}=-1 mA	2.4	—	—	2.4	—	—	
		I_{OH}=-1 µA	—	V_{DD}-0.1	—	—	V_{DD}-0.1	—	
Input Leakage Current	I_{IN} Max.	V_{IN}=0 V to V_{DD}	—	±0.1	±2	—	±0.1	±2	µA
3-State Output Leakage Current	I_{OUT}	$V_{I/O}$=0 V to V_{DD}	—	±0.5	±2	—	±0.5	±2	
Operating Device Current	I_{OPER1}#	V_{IN}=V_{IL}, V_{IH} t_{cyc}=1 µs	—	4.5	9	—	7.5	15	mA
		t_{cyc}=min. cycle time	—	22.5	45	—	22.5	45	
	I_{OPER2}#	V_{IN}=0.2 V, t_{cyc}=1 µs	—	2	4	—	5	10	
		V_{DD}-0.2 V t_{cyc}=min. cycle time	—	20	40	—	20	40	
Input Capacitance	C_{IN}	V_{IN}=0 V, f=1 MHz, T_A=25° C	—	4	6	—	4	6	pF
Output Capacitance	$C_{I/O}$	$V_{I/O}$=0 V, f=1 MHz, T_A=25° C	—	6	8	—	6	8	

•Typical values are for T_A=25° C and nominal V_{DD}.

#Outputs open circuited.

CDM6264

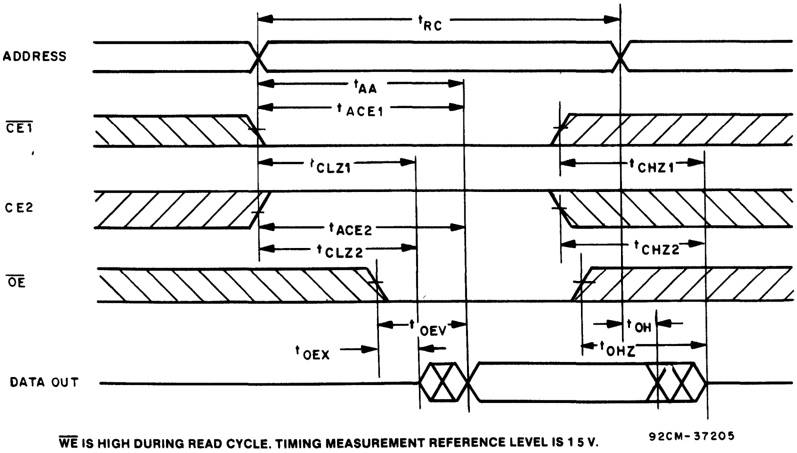
SIGNAL DESCRIPTIONS

A0-A12 (Address Inputs):	These inputs must be stable prior to a write operation, but may change asynchronously during read functions.
I/01-I/08:	8-bit tristate data bus.
$\overline{\text{CE1}}$, CE2 (Chip Enable):	Either chip enable, when not true, powers down the chip, disables Read and Write functions, and gates off address and output buffers.
$\overline{\text{OE}}$ (Output Enable):	Enables tristate outputs if $\overline{\text{CE1}}$ and CE2 are valid and $\overline{\text{WE}}$ is high.
$\overline{\text{WE}}$ (Write Enable):	Enables Write function, if $\overline{\text{CE1}}$ and CE2 are valid. $\overline{\text{WE}}$ will dominate if both $\overline{\text{WE}}$ and $\overline{\text{OE}}$ are low (i.e., the bus will be tristated and a Write will occur).
V_{DD}, V_{SS}:	Power supply connections.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0° to +70° C (CDM6264-3); T_A = -40° to +85° C (CDM6264-2I), V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns; C_L = 100 pF and 1 TTL Load, Input Pulse Levels: 0.8 V to 2.4 V

CHARACTERISTIC		LIMITS				UNITS
		CDM6264-3		CDM6264-2I		
Read Cycle Times, See Fig. 2		**MIN.†**	**MAX.**	**MIN.†**	**MAX.**	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	
Chip Enable Access Time	t_{ACE1},t_{ACE2}	—	150	—	200	
Chip Enable to Output Active	t_{CLZ1},t_{CLZ2}	10	—	10	—	
Output Enable to Output Valid	t_{OEV}	—	70	—	70	
Output Enable to Output Active	t_{OEX}	5	—	5	—	
Chip Disable to Output "High Z"	t_{CHZ1},t_{CHZ2}	0	70	0	70	
Output Disable to Output "High Z"	t_{OHZ}	0	60	0	60	
Output Hold from Address Change	t_{OH}	30	—	30	—	

† Time required by a limit device to allow for the indicated function.



$\overline{\text{WE}}$ IS HIGH DURING READ CYCLE. TIMING MEASUREMENT REFERENCE LEVEL IS 1 5 V.

92CM-37205

Fig. 2 - Read-cycle timing waveforms.

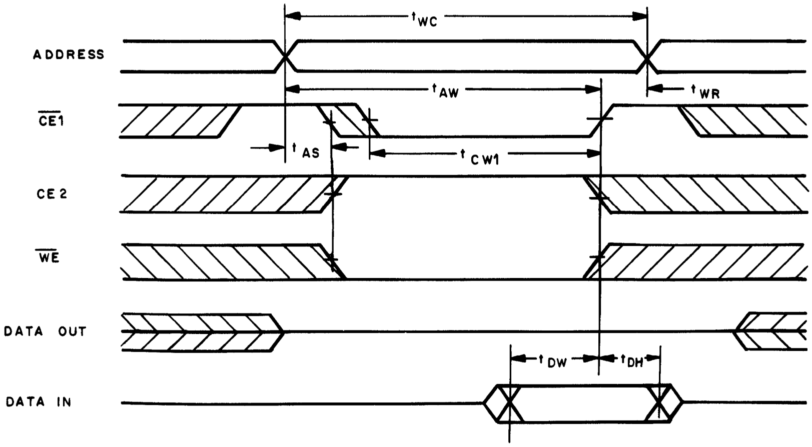
CDM6264

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0° to +70°C (CDM6264-3); T_A = -40° to +85°C (CDM6264-2I), V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns; C_L = 100 pF and 1 TTL Load, Input Pulse Levels: 0.8 V to 2.4 V

CHARACTERISTIC Write Cycle Times, See Fig. 3		LIMITS				UNITS
		CDM6264-3		CDM6264-2I		
		MIN.†	MAX.	MIN.†	MAX.	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable to End of WRITE	t_{CW1},t_{CW2}	120	—	170	—	
Address Valid to End of WRITE	t_{AW}	120	—	170	—	
Address Setup Time	t_{AS}	0	—	0	—	
Write Enable Width	t_{WW}	100	—	120	—	
Write Recovery Time	t_{WR}	0	—	0	—	
Write to Output "High Z"	t_{WHZ}	—	70	—	80	
Input Data Setup Time	t_{DW}	60	—	80	—	
Input Data Hold Time	t_{DH}	0	—	0	—	
Output Active from End of Write	t_{OW}	10	—	10	—	

†Time required by a limit device to allow for the indicated function.

WRITE CYCLE 1 ($\overline{CE1}$ CONTROL)



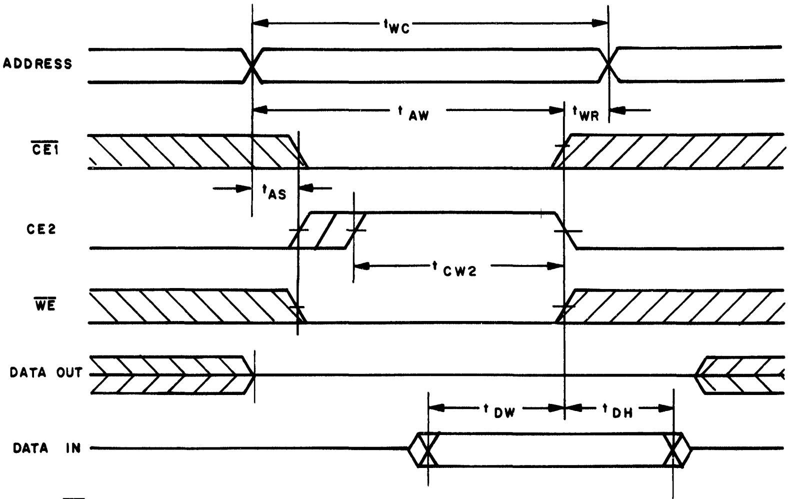
IN A $\overline{CE1}$ OR CE2 CONTROLLED WRITE CYCLE, THE OUTPUT BUFFERS REMAIN IN A HIGH IMPEDANCE STATE, WHETHER $\overline{OE}$ IS HIGH OR LOW.
TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

92CM-37204

Fig. 3 - Write-cycle timing waveforms.

CDM6264

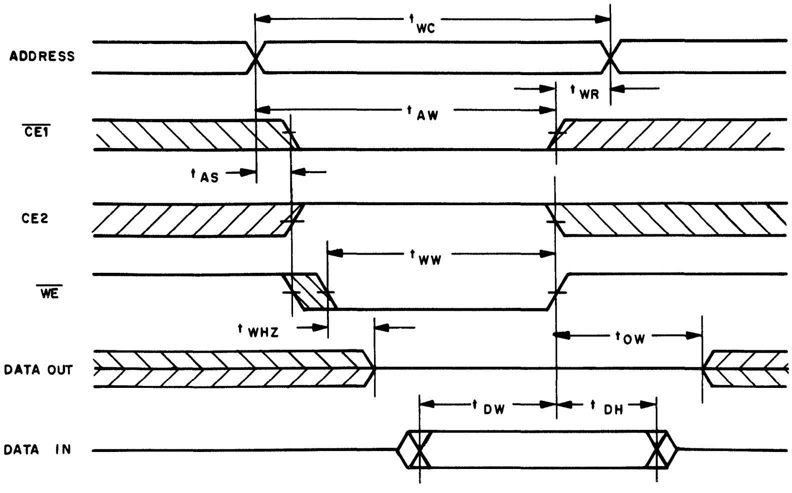
WRITE CYCLE 2 (CE2 CONTROL)



IN A $\overline{CE1}$ OR CE2 CONTROLLED WRITE CYCLE, THE OUTPUT BUFFERS REMAIN IN A HIGH IMPEDANCE STATE, WHETHER $\overline{OE}$ IS HIGH OR LOW.
TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

92CM-37206

WRITE CYCLE 3 ($\overline{WE}$ CONTROL)



IF $\overline{OE}$ IS HIGH DURING A $\overline{WE}$ CONTROLLED WRITE CYCLE,
THE OUTPUT BUFFERS REMAIN IN A HIGH IMPEDANCE STATE IN THIS PERIOD.
TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V

92CS-37207

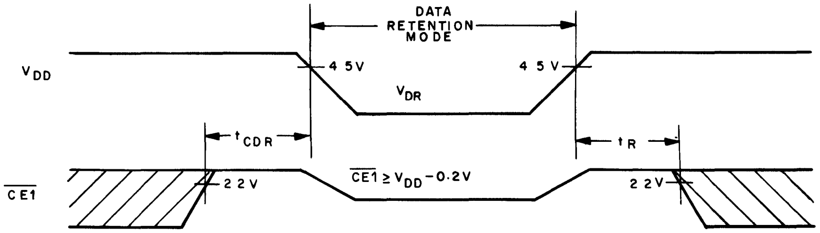
Fig. 3 - Write-cycle timing waveforms (cont'd).

DATA RETENTION CHARACTERISTICS, See Fig. 4.

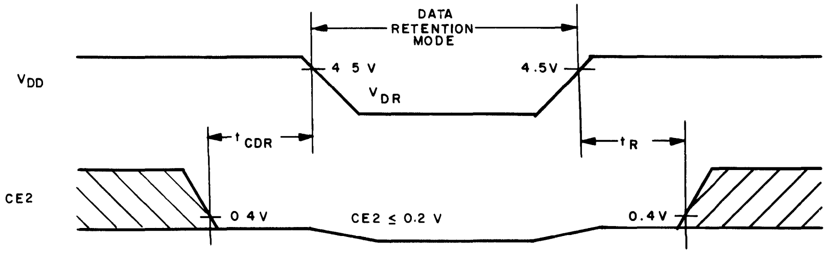
CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			CDM6264-3		CDM6264-2I		
			Min.	Max.	Min.	Max.	
Minimum Data Retention Voltage	V_{DR}	$\overline{CE1} \geq V_{DD}$-0.2 V, or CE2 ≤ 0.2 V: 0°C ≤ T_A ≤ +70°C	2	—	—	—	V
		0°C ≤ T_A ≤ +85°C	—	—	2	—	
		-40°C ≤ T_A < 0°C	—	—	4	—	
Data Retention Quiescent Current	$I_{DD}DR$	$\overline{CE1}$, CE2 ≥ V_{DD}-0.2 V, or CE2 ≤ 0.2 V: V_{DD} = 3 V, 0°C ≤ T_A ≤ +70°C	—	50	—	—	µA
		V_{DD} = 3 V, 0°C ≤ T_A ≤ +85°C	—	—	—	100	
		V_{DD} = 4 V, -40°C ≤ T_A < 0°C	—	—	—	100	
Chip Disable to Data Retention Time	t_{CDR}	See Fig. 4	0	—	0	—	ns
Recovery to Normal Operation Time	t_R	See Fig. 4	$^*t_{RC}$	—	$^*t_{RC}$	—	

$^*t_{RC}$ = Read Cycle Time

DATA RETENTION WAVEFORM 1 ($\overline{CE1}$ CONTROL)



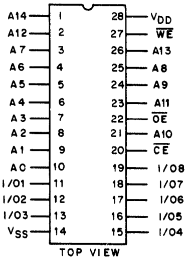
DATA RETENTION WAVEFORM 2 (CE2 CONTROL)



92CM-37208

Fig 4 - Low V_{DD} data-retention timing waveforms.

CDM62256



TERMINAL ASSIGNMENT

CMOS 32,768-Word by 8-Bit LSI Static RAM

Features:

- *Fully static operation*
- *Single power supply: 4.5 V to 5.5 V*
- *All inputs and outputs directly TTL compatible*
- *Industry standard 28-pin configuration*
- *Input address buffers gated off with chip disable*
- *Low standby and operating power: I_{DDS1} = 2 μA typical, I_{DDA} = 70 mA maximum*
- *3-state outputs*
- *Extended operating temperature range*

The RCA-CDM62256 is a 32,768-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This device has common data input and data output and utilizes a single power supply of 4.5 V to 5.5 V. Chip Enable ($\overline{CE}$) gates the address and output buffers and powers down the chip to the low power standby mode. The output enable ($\overline{OE}$) controls the output buffers to eliminate bus contention.

The CDM62256-10 has an operating temperature range of 0° to +70° C. The CDM62256-10I and CDM62256-12I have an operating temperature range of -40° to +85° C.

The CDM62256 is supplied in 28-lead, hermetic, dual-in-line, side-brazed ceramic packages (D suffix), in 28-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

	CDM62256-10	CDM62256-10I	CDM62256-12I
Access Time (max.)	100 ns	100 ns	120 ns
Output Enable Time (max.)	50 ns	50 ns	60 ns
Operating Current (max.)	70 mA	70 mA	70 mA
Standby Current I_{DDS1} (max.)	100 μA	200 μA	200 μA
Operating Temp. Range	0° to +70° C	-40° to +85° C	
Data Retention Voltage:			
$0° \leq T_A \leq +70° C$	2 V min.	—	—
$0° \leq T_A \leq +85° C$	—	2 V min.	2 V min.
$-40° \leq T_A < 0° C$	—	4.5 V min.	4.5 V min.

RECOMMENDED DC OPERATING CONDITIONS at T_A = 0 to +70° C (CDM62256-10); T_A = -40° to +85° C (CM62256-10I, CDM62256-12I) For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS			UNITS
		MIN.	TYP.	MAX.	
DC Operating Voltage Range	V_{DD}	4.5	5	5.5	V
Input Voltage Range	V_{IH}	2.2	3.5	V_{DD} +0.3	
	V_{IL}	-0.3 Δ	0	0.8	

Δ Min V_{IL} = -1.0 V for pulse width ≤ 50 ns

MAXIMUM RATINGS, *Absolute-Maximum Values*

* DC SUPPLY-VOLTAGE RANGE, (V_{DD}): .... -0.5 to +7 V
* INPUT VOLTAGE RANGE, (V_{IN}) .... -0.5 ** to +7 V
* INPUT/OUTPUT VOLTAGE RANGE ($V_{I/O}$) .... -0.5 ** to V_{DD} +0.3 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40° to +75°C (PACKAGE TYPE E) .... 500 mW
For T_A = +75° to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 420 mW
For T_A = -40° to +85°C (PACKAGE TYPE D) .... 500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
CDM62256-10 (PACKAGE TYPES D AND E) .... 0 to +70°C
CDM62256-10I, 12I (PACKAGE TYPES D AND E) .... -40° to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... -55° to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

---

* (Voltage referenced to V_{SS} terminal)
** Min V_{IN}, $V_{I/O}$ = -1 V for pulse width ≤ 50 ns

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0 to A14	DATA I/O	MODE	DEVICE CURRENT
H	X	X	X	Hi-Z	Standby	I_{DDS}
L	X	L	Stable	D_{IN}	Write	I_{DDA}
L	L	H	Stable	D_{OUT}	Read	I_{DDA}
L	H	H	Stable	Hi-Z	Output disable	I_{DDA}

L = Low, H = High, X = H or L

PIN IDENTIFICATION	
A0 TO A14	ADDRESS INPUT
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
I/O 1 TO 8	DATA I/O
VDD	POWER SUPPLY (5 V)
VSS	POWER SUPPLY (0 V)

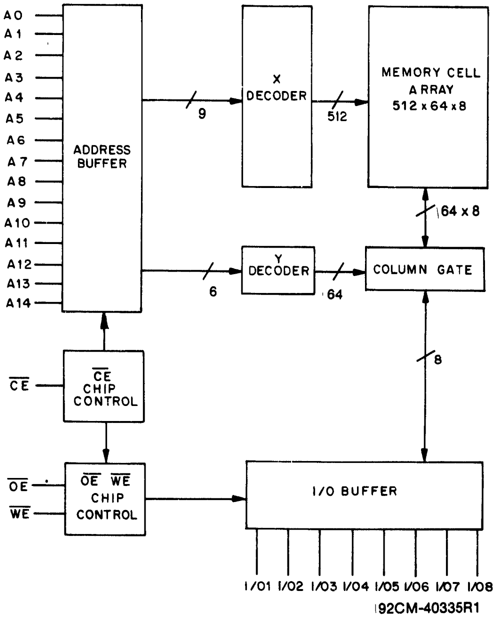


Fig. 1 - Functional block diagram.

CDM62256

ELECTRICAL CHARACTERISTICS at T_A = 0° to +70° C (CDM62256-10); T_A = -40° to +85° C (CDM62256-10I, CDM62256-12I); V_{DD} = 5 V ± 10%, except as noted.

DC Electrical Characteristics

CHARACTERISTIC		TEST CONDITIONS	LIMITS									UNITS
			CDM62256-10			CDM62256-10I			CDM62256-12I			
			MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Input Leakage	I_{LI}	V_I = 0 to V_{DD}	-1	—	1	-1	—	1	-1	—	1	µA
Standby Supply Current	I_{DDS}	$\overline{CE}$ = V_{IH}	—	1.5	3.0	—	1.5	3.0	—	1.5	3.0	mA
	I_{DDS1}	$\overline{CE}$ ≥ V_{DD}-0.2 V	—	2	100	—	2	200	—	2	200	µA
Average Operating Current	I_{DDA}	V_I = V_{IL}, V_{IH} I_{IO} = 0 mA t_{cyc} = Min	—	40	70	—	40	70	—	37	70	mA
Operating Supply Current	I_{DDO}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0 mA	—	35	65	—	35	65	—	35	65	mA
Output Leakage	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{DD}	-1	—	1	-1	—	1	-1	—	1	µA
High Level Output Voltage	V_{OH}	I_{OH} = -1.0 mA	2.4	V_{DD}-0.1	—	2.4	V_{DD}-0.1	—	2.4	V_{DD}-0.1	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 2.1 mA	—	0.2	0.4	—	0.2	0.4	—	0.2	0.4	V

* Typical values are measured at T_A = 25° C and V_{DD} = 5.0 V

Terminal Capacitance (f = 1 MHz, T_A = 25° C)

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Address Capacitance	C_{ADD}	V_{ADD} = 0 V	—	—	10	pF
Input Capacitance	C_I	V_I = 0 V	—	—	10	pF
I/O Terminal Capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	—	—	10	pF

SIGNAL DESCRIPTIONS

A0-A14 (Address Inputs): These inputs must be stable prior to a write operation, but may change asynchronously during read operations.

I/01-I/08: 8-bit 3-state data bus.

$\overline{CE}$ (Chip Enable): Powers down chip, disables Read and Write functions, and gates off address inputs.

$\overline{OE}$ (Output Enable): Enables 3-state outputs if $\overline{CE}$ is low and $\overline{WE}$ is high.

$\overline{WE}$ (Write Enable): Enables Write function, if $\overline{CE}$ is low $\overline{WE}$ will dominate if both $\overline{WE}$ and $\overline{OE}$ are low (i.e., the bus will be 3-stated and a Write will occur).

V_{DD}, V_{SS}: Power supply connections.

AC ELECTRICAL CHARACTERISTICS at T_A = 0° to +70° C (CDM62256-10); T_A = -40° to +85° C (CDM62256-10I, CDM62256-12I); V_{DD} = 5 V ± 10%

Read Cycle

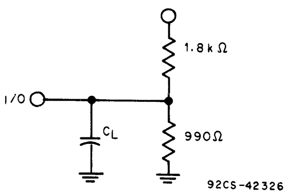
CHARACTERISTIC		A.C. TEST CONDITIONS	LIMITS				UNITS
			CDM62256-10 CDM62256-10I		CDM62256-12I		
			MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	1	100	—	120	—	ns
Address Access Time	t_{AA}		—	100	—	120	
Chip Enable Access Time	t_{ACE}		—	100	—	120	
Output Enable Access Time	t_{OEV}		—	50	—	60	
Chip Enable to Output Active	t_{CLZ}	2	10	—	10	—	
Chip Disable to Output 'High Z'	t_{CHZ}		—	35	—	40	
Output Enable to Output Active	t_{OLZ}		5	—	5	—	
Output Disable to Output 'High Z'	t_{OHZ}		—	35	—	40	
Output Hold From Address Change	t_{OH}	1	10	—	10	—	

Write Cycle

CHARACTERISTIC		A.C. TEST CONDITIONS	LIMITS				UNITS
			CDM62256-10 CDM62256-10I		CDM62256-12I		
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	1	100	—	120	—	ns
Chip Enable to End of Write	t_{CW}		80	—	85	—	
Address Valid to End of Write	t_{AW}		80	—	85	—	
Address Setup Time	t_{AS}		0	—	0	—	
Write Pulse Width	t_{WP}		75	—	80	—	
Write Recovery Time	t_{WR}		0	—	0	—	
Input Data Set Time	t_{DW}		45	—	50	—	
Input Data Hold Time	t_{DH}		0	—	0	—	
Write to Output 'High Z'	t_{WHZ}	2	—	35	—	40	
Ouput Active From End of Write	t_{OW}		10	—	10	—	

Test Condition: 1

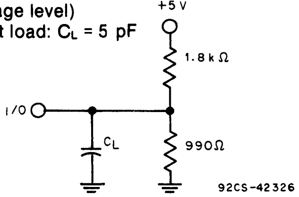
1. Input pulse level: 0.6 V to 2.4 V
2. t_r, t_f = 5 ns
3. Input and output timing reference levels: 1.5 V
4. Output load: C_L = 100 pF



C_L = 100 pF (Includes Jig Capacitance)

Test Condition: 2

1. Input pulse level: 0.6 V to 2.4 V
2. t_r, t_f = 5 ns
3. Input timing reference levels: 1.5 V
4. Output timing reference levels:
   ±200 mV (the level displaced from stable output voltage level)
5. Output load: C_L = 5 pF

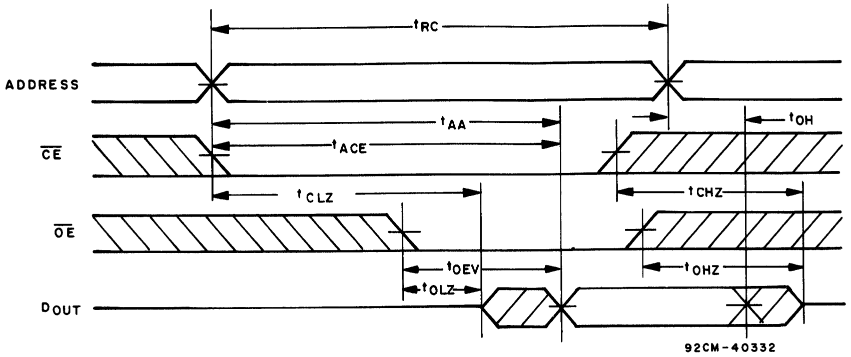


C_L = 5 pF (Includes Jig Capacitance)

CDM62256

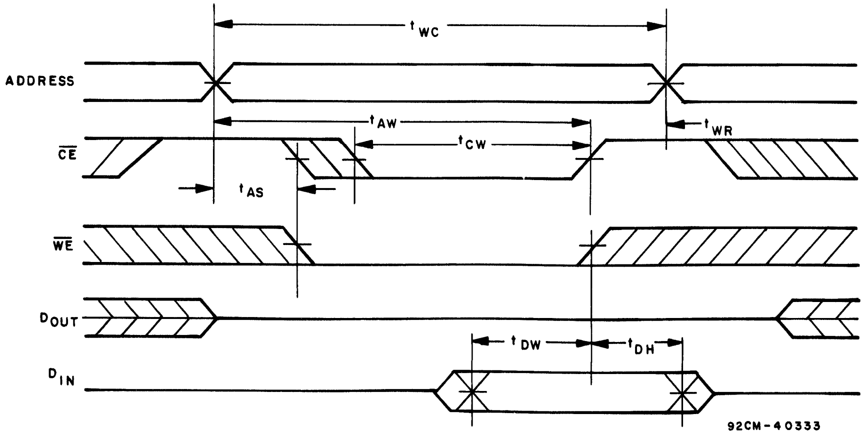
TIMING CHARTS

Read Cycle



NOTE: DURING READ CYCLE TIME, $\overline{WE}$ IS TO BE "H" LEVEL.

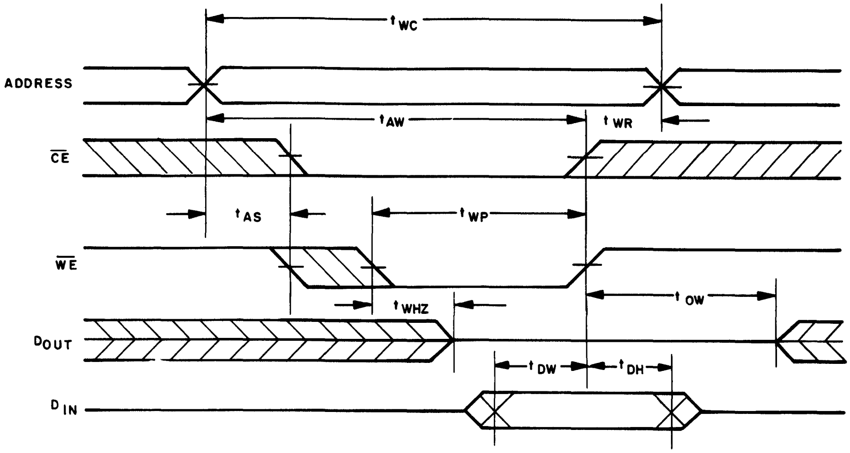
Write Cycle 1 ($\overline{CE}$ Control)



NOTE: DURING WRITE CYCLE TIME THAT IS CONTROLLED BY $\overline{CE}$, OUTPUT BUFFER IS HIGH IMPEDANCE WHETHER $\overline{OE}$ LEVEL IS "H" OR "L".

TIMING CHARTS (Continued)

Write Cycle 2 ($\overline{WE}$ Control)



NOTE: DURING WRITE CYCLE TIME THAT IS CONTROLLED BY $\overline{WE}$, OUTPUT BUFFER IS HIGH IMPEDANCE.

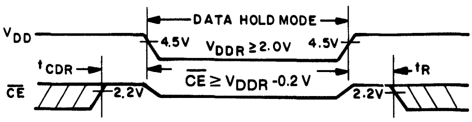
92CM-40334

DATA RETENTION CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		CDM62256-10		CDM62256-10I CDM62256-12I		
		MIN.	MAX.	MIN.	MAX.	
Minimum Data Retention Voltage V_{DR}	$\overline{CE} \geq V_{DD}$-0.2 V, 0° C $\leq T_A \leq$ +70° C	2	—	—	—	V
	0° C $\leq T_A \leq$ +85° C	—	—	2	—	
	-40° C $\leq T_A <$ 0° C	—	—	4.5	—	
Data Retention Quiescent Current $I_{DD}DR$	$\overline{CE} \geq V_{DD}$-0.2 V, V_{DD}=3 V, 0° C $\leq T_A \leq$ +70° C	—	50	—	—	µA
	V_{DD}=3 V, 0° C $\leq T_A \leq$ +85° C	—	—	—	100	
	V_{DD}=4.5 V, -40° C $\leq T_A <$ 0° C	—	—	—	100	
Chip Disable to Data Retention Time t_{CDR}	—	0	—	0	—	ns
Recovery to Normal Operation Time t_R	—	*t_{RC}	—	*t_{RC}	—	

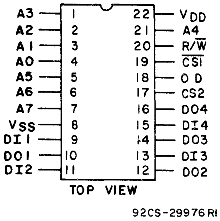
*t_{RC} = Read Cycle Time.

DATA RETENTION TIMING



92CS-40336R1

CDP1822, CDP1822C



CDP1822, CDP1822C
TERMINAL ASSIGNMENTS

256-Word by 4-Bit LSI Static Random-Access Memory

Features:

- *Low operating current-8 mA at V_{DD}=5 V and cycle time=1 µs*
- *Industry standard pinout*
- *Two Chip-Select inputs-simple memory expansion*
- *Memory retention for standby battery voltage of 2 V min.*
- *Output-Disable for common I/O systems*
- *3-state data output for bus-oriented systems*
- *Separate data inputs and outputs*

The RCA-CDP1822 and CDP1822C are 256-word by 4-bit static random-access memories designed for use in memory systems where high speed, low operating current, and simplicity in use are desirable. The CDP1822 features high speed and a wide operating voltage range. Both types have separate data inputs and outputs and utilize single power supplies of 4 to 6.5 volts for the CDP1822C and 4 to 10.5 volts for the CDP1822.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. The Output Disable input allows these RAMs to be used in common data Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input condition. The output assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or CS2.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5-V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

The CDP1822 and CDP1822C types are supplied in 22-lead hermetic dual-in-line side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix). The CDP1822C is also available in chip form (H suffix).

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	Chip Select 1 $\overline{CS}_1$	Chip Select 2 CS_2	Output Disable OD	Read/$\overline{\text{Write}}$ $R/\overline{W}$	
Read	0	1	0	1	Read
Write	0	1	0	0	Data In
Write	0	1	1	0	High Impedance
Standby	1	X	X	X	High Impedance
Standby	X	0	X	X	High Impedance
Output Disable	X	X	1	X	High Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1822		CDP1822C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltage referenced to V_{SS} Terminal)	
CDP1822	-0.5 to +11 V
CDP1822C	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A=-40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A=+60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 12 mW/° C to 200 mW
For T_A=-55 to +100° C (PACKAGE TYPE D)	500 mW
For T_A=+100 to +125° C (PACKAGE TYPE D)	Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPE D	-55 to +125° C
PACKAGE TYPE E	-40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 in (1 59 ± 0 79 mm) from case for 10 s max	+265° C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, Except as Noted

CHARACTERISTIC	TEST CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1822			CDP1822C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device	—	0, 5	5	—	—	500	—	—	500	μA
Current, I_{DD}	—	0, 10	10	—	—	1000	—	—	—	
Output Voltage: Low-Level, V_{OL}	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
High-Level, V_{OH}	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	
Output Low (Sink)	0.4	0, 5	5	2	4	—	2	4	—	mA
Current, I_{OL}	0.5	0, 10	10	4.5	9	—	—	—	—	
Output High (Source)	4.6	0, 5	5	-1	-2	—	-1	-2	—	
Current, I_{OH}	9.5	0, 10	10	-2.2	-4.4	—	—	—	—	
Input Current, I_{IN}	—	0, 5	5	—	—	±5	—	—	±5	μA
	—	0, 10	10	—	—	±10	—	—	—	
3-State Output	0, 5	0, 5	5	—	—	±5	—	—	±5	
Leakage Current I_{OUT}	0, 10	0, 10	10	—	—	±10	—	—	—	
Operating Current, I_{DD1}†	—	0, 5	5	—	4	8	—	4	8	mA
	—	0, 10	10	—	8	16	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	

†Outputs open circuited, cycle time = 1 μs

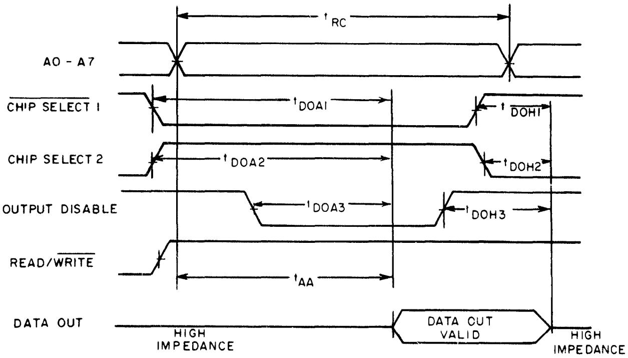
*Typical values are for T_A = 25° C and nominal V_{DD}

CDP1822, CDP1822C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ±5%, Input t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS CDP1822 Min.†			LIMITS CDP1822C Min.†			UNITS
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Read Cycle Times (Fig. 1)								
Read Cycle t_{RC}	5	450	—	—	450	—	—	ns
	10	250	—	—	—	—	—	
Access from Address t_{AA}	5	—	250	450	—	250	450	
	10	—	150	250	—	—	—	
Output Valid from $\overline{\text{Chip-Select}}$ 1 t_{DOA1}	5	—	250	450	—	250	450	
	10	—	150	250	—	—	—	
Output Valid from Chip-Select 2 t_{DOA2}	5	—	250	450	—	250	450	
	10	—	150	250	—	—	—	
Output Valid from Output Disable t_{DOA3}	5	—	—	200	—	—	200	
	10	—	—	110	—	—	—	
Output Hold from $\overline{\text{Chip-Select}}$ 1 t_{DOH1}	5	20	—	—	20	—	—	
	10	20	—	—	—	—	—	
Output Hold from Chip-Select 2 t_{DOH2}	5	20	—	—	20	—	—	
	10	20	—	—	—	—	—	
Output Hold from Output Disable t_{DOH3}	5	20	—	—	20	—	—	
	10	20	—	—	--	—	—	

†Time required by a limit device to allow for indicated function
*Typical values are for T_A = 25° C and nominal V_{DD}



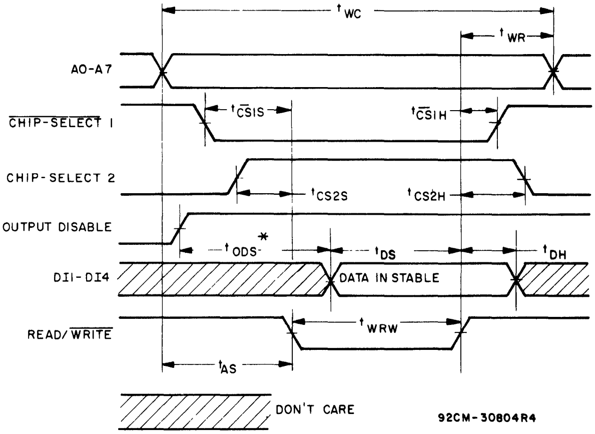
92CM-30244R4

Fig 1 - Read cycle timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ±5%, Input t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
	V_{DD} (V)	CDP1822			CDP1822C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Write Cycle Times (Fig. 2)								
Write Cycle t_{WC}	5	500	—	—	500	—	—	ns
	10	300	—	—	—	—	—	
Address Set-Up t_{AS}	5	200	—	—	200	—	—	
	10	110	—	—	—	—	—	
Write Recovery t_{WR}	5	50	—	—	50	—	—	
	10	40	—	—	—	—	—	
Write Width t_{WRW}	5	250	—	—	250	—	—	
	10	150	—	—	—	—	—	
Input Data Set-Up Time t_{DS}	5	250	—	—	250	—	—	
	10	150	—	—	—	—	—	
Data In Hold t_{DH}	5	50	—	—	50	—	—	
	10	40	—	—	—	—	—	
$\overline{\text{Chip-Select}}$ 1 Set-Up $t_{\overline{CS}1S}$	5	200	—	—	200	—	—	
	10	110	—	—	—	—	—	
Chip-Select 2 Set-Up t_{CS2S}	5	200	—	—	200	—	—	
	10	110	—	—	—	—	—	
$\overline{\text{Chip-Select}}$ 1 Hold $t_{\overline{CS}1H}$	5	0	—	—	0	—	—	
	10	0	—	—	0	—	—	
Chip-Select 2 Hold t_{CS2H}	5	0	—	—	0	—	—	
	10	0	—	—	0	—	—	
Output Disable Set-Up t_{ODS}	5	200	—	—	200	—	—	
	10	110	—	—	—	—	—	

†Time required by a limit device to allow for indicated function.
*Typical values are for T_A = 25° C and nominal V_{DD}



* t_{ODS} IS REQUIRED FOR COMMON I/O OPERATION ONLY, FOR SEPARATE I/O OPERATIONS, OUTPUT DISABLE IS DON'T CARE

Fig. 2 - Write cycle timing waveforms.

CDP1822, CDP1822C

DATA RETENTION CHARACTERISTICS at T_A = -40 to +85° C, see Fig. 3

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
	V_{DR} (V)	V_{DD} (V)	CDP1822			CDP1822C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Min Data Retention Voltage, V_{DR}	—	—	—	1.5	2	—	1.5	2	V
Data Retention Quiescent Current, I_{DD}	2	—	—	30	100	—	30	100	μA
Chip Deselect to Data Retention Time, t_{CDR}	—	5	600	—	—	600	—	—	ns
	—	10	300	—	—	—	—	—	
Recovery to Normal Operation Time, t_{RC}	—	5	600	—	—	600	—	—	
	—	10	300	—	—	—	—	—	
V_{DD} to V_{DR} Rise and Fall Time t_r, t_f	2	5	1	—	—	1	—	—	μs

*Typical values are for T_A = 25° C and nominal V_{DD}

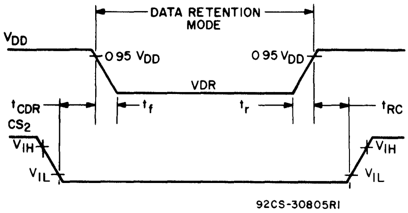


Fig. 3 - Low V_{DD} data retention timing waveforms

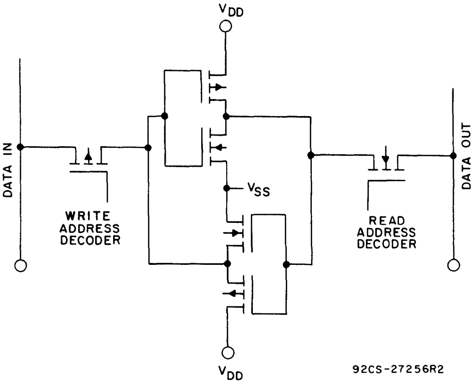


Fig. 4 - Memory cell configuration.

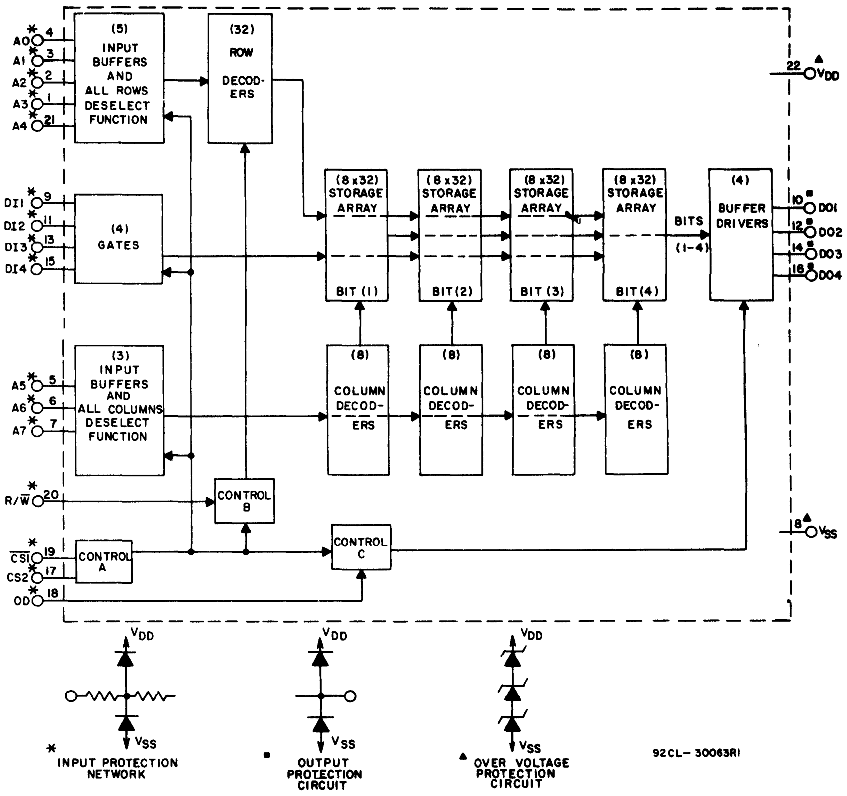


Fig. 5 - Functional block diagram for CDP1822 and CDP1822C.

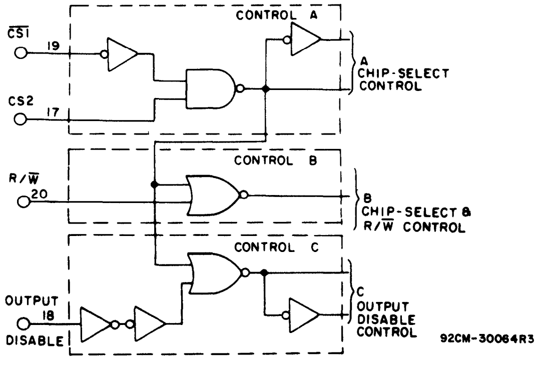
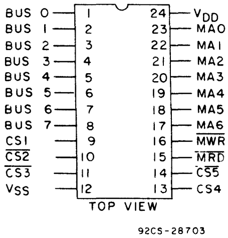


Fig. 6 - Logic diagram of controls for CDP1822 and CDP1822C.

CDP1823, CDP1823C



TERMINAL ASSIGNMENT

128-Word x 8-Bit Static Random-Access Memory

Features:

- *Fast access time:*
  450 ns at V_{DD}= 5 V;
  250 ns at V_{DD} = 10 V
- *Common data inputs and outputs*
- *Multiple-chip select inputs to simplify memory system expansion*

The RCA-CDP1823 and CDP1823C are 128-word by 8-bit CMOS SOS static random-access memories. These memories are compatible with general-purpose microprocessors. The two memories are functionally identical. They differ in that the CDP1823 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1823C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1823 memory has 8 common data input and data output terminals for direct connection to a bidirectional data bus and is operated from a single voltage supply. Five chip-select inputs are provided to simplify memory-system expansion. In order to enable the CDP1823, the chip-select inputs $\overline{CS2}$, $\overline{CS3}$, and $\overline{CS5}$ require a low input signal, and the chip-select inputs CS1 and CS4 require a high input signal.

The $\overline{MRD}$ signal enables all 8 output drivers when in the low state and should be in a high state during a write cycle.

After valid data appear at the output, the address inputs may be changed immediately. Output data will be valid until either the $\overline{MRD}$ signal goes high, the device is deselected, or t_{AA} (access time) after address changes.

The CDP1823 and CDP1823C are supplied in hermetic 24-lead dual-in-line ceramic packages (D suffix), and in 24-lead dual-in-line plastic packages (E suffix).

OPERATIONAL MODES

Function	$\overline{MRD}$	$\overline{MWR}$	**CS1**	$\overline{CS2}$	$\overline{CS3}$	**CS4**	$\overline{CS5}$	**Bus Terminal State**
READ	0	X	1	0	0	1	0	Storage State of Addressed Word
WRITE	1	0	1	0	0	1	0	Input High-Impedance
STAND-BY (ACTIVE)	1	1	1	0	0	1	0	High-Impedance
NOT SELECTED	X	X	0	X	X	X	X	High-Impedance
	X	X	X	1	X	X	X	
	X	X	X	X	1	X	X	
	X	X	X	X	X	0	X	
	X	X	X	X	X	X	1	

Logic 1 = High   Lcgic 0 = Low   X = Don't Care

File Number **1198**

OPERATING CONDITIONS at T_A = FULL PACKAGE-TEMPERATURE RANGE

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1823D		CDP1823CD		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1823 .... −0.5 to +11 V
CDP1823C .... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGES (D SUFFIX TYPES)................................ −55 to +125 °C
PLASTIC PACKAGES (E SUFFIX TYPES).................................. −40 to +85 °C
STORAGE TEMPERATURE RANGE (T_{stg}).................................. −65 to +150 °C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.................... +265 °C

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to + 85° C, Except as noted

CHARACTERISTICS	TEST CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1823			CDP1823C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device —	—	0,5	5	—	—	500	—	—	500	μA
Current, I_{DD}	—	0,10	10	—	—	1000	—	—	—	
Output Voltage:	—	0,5	5	—	0	0.1	—	0	0.1	V
Low-Level, V_{OL}	—	0,10	10	—	0	0.1	—	—	—	
High-Level, V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	
Output Low (Sink)	0.4	0,5	5	2	4	—	2	4	—	mA
Current, I_{OL}	0.5	0,10	10	4.5	9	—	—	—	—	
Output High (Source)	4.6	0,5	5	-1	-2	—	-1	-2	—	
Current, I_{OH}	9.5	0,10	10	-2.2	-4.4	—	—	—	—	
Input Current, I_{IN}	Any Input	0,5	5	—	—	±5	—	—	±5	μA
		0,10	10	—	—	±10	—	—	—	
3-State Output	0,5	0,5	5	—	—	±5	—	—	±5	
Leakage Current, I_{OUT}	0,10	0,10	10	—	—	±10	—	—	—	
Operating Current, I_{DD1}†	—	0,5	5	—	4	8	—	4	8	mA
	—	0,10	10	—	8	16	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	

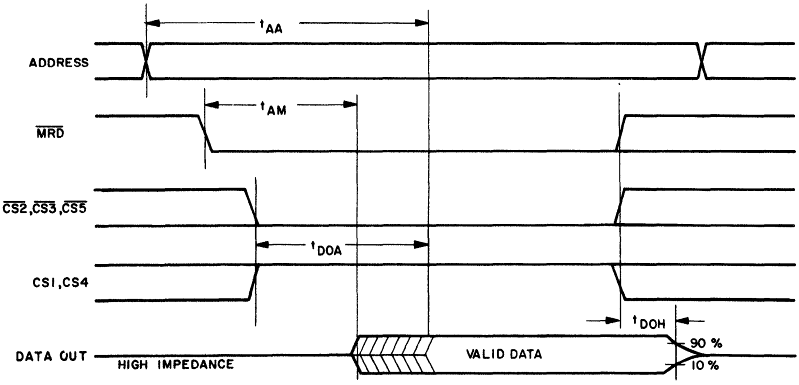
†Outputs open circuited; cycle time = 1 μs.
*Typical values are for T_A = 25° C and nominal V_{DD}.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85 °C, V_{DD} ± 5%, t_r,t_f = 20 ns, C_L = 100 pF.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1823			CDP1823C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Read Cycle (See Fig. 1)								
Access Time From Address Change, t_{AA}	5	—	275	450	—	275	450	ns
	10	—	150	250	—	—	—	
Access Time From Chip Select, t_{DOA}	5	—	150	250	—	150	250	
	10	—	100	150	—	—	—	
$\overline{MRD}$ to Output Active, t_{AM}	5	—	150	250	—	150	250	
	10	—	100	150	—	—	—	
Data Hold Time After Read, t_{DOH}	5	25	50	75	25	50	75	
	10	15	25	40	—	—	—	

*Typical values are at T_A = 25 °C and nominal voltage.

†Time required by a limit device to allow for the indicated function.



NOTE: $\overline{MWR}$ IS HIGH DURING READ OPERATION.
TIMING MEASUREMENT REFERENCE IS 0.5 V_{DD}.

92CM-31942R1

Fig. 1 - Read cycle timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $C_L = 100$ pF.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1823			CDP1823C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Write Cycle (See Fig. 2)								
Write Recovery, tWR	5	75	—	—	75	—	—	ns
	10	50	—	—	—	—	—	
Write Cycle, t_{WC}	5	400	—	—	400	—	—	
	10	225	—	—	—	—	—	
Write Pulse Width, tWRW	5	200	—	—	200	—	—	
	10	100	—	—	—	—	—	
Address Setup Time, tAS	5	125	—	—	125	—	—	
	10	75	—	—	—	—	—	
Data Setup Time, tDS	5	100	—	—	100	—	—	
	10	75	—	—	—	—	—	
Data Hold Time From $\overline{MWR}$, t_{DH}	5	75	—	—	75	—	—	
	10	50	—	—	—	—	—	

*Typical values are at $T_A = 25$ °C and nominal voltage.

†Time required by a limit device to allow for the indicated function.

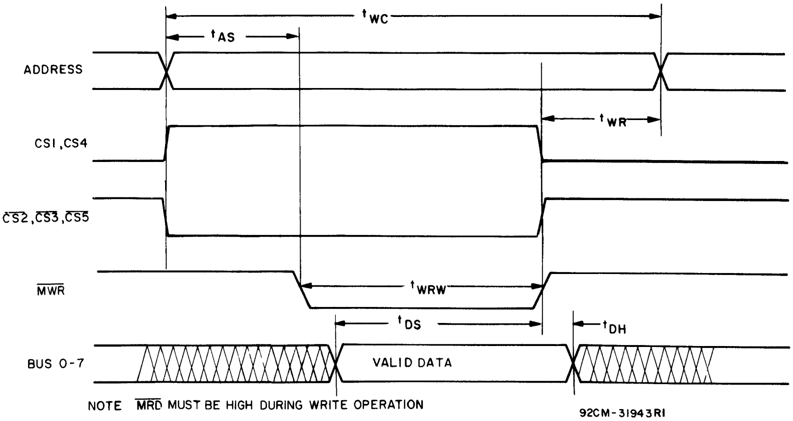


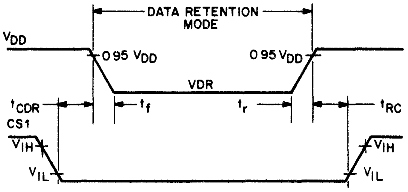
Fig. 2 - Write cycle timing diagram.

CDP1823, CDP1823C

DATA RETENTION CHARACTERISTICS at T_A = −40 to +85° C; see Fig. 3

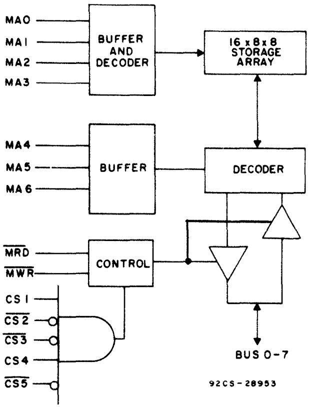
CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			CDP1823			CDP1823C			
	V_{DR} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Min. Data Retention Voltage, V_{DR}	—	—	—	1.5	2	—	1.5	2	V
Data Retention Quiescent Current, I_{DD}	2	—	—	30	100	—	30	100	μA
Chip Deselect to Data Retention Time, t_{CDR}	—	5	600	—	—	600	—	—	ns
	—	10	300	—	—	—	—	—	
Recovery to Normal Operation Time, t_{RC}	—	5	600	—	—	600	—	—	
	—	10	300	—	—	—	—	—	
V_{DD} to V_{DR} Rise and Fall Time t_r,t_f	2	5	1	—	—	1	—	—	μs

*Typical values are for T_A = 25° C and nominal V_{DD}.



92CS-30805RI

Fig. 3 - Low V_{DD} data retention timing waveforms.



Functional Diagram

Fig. 4 - Functional diagram.

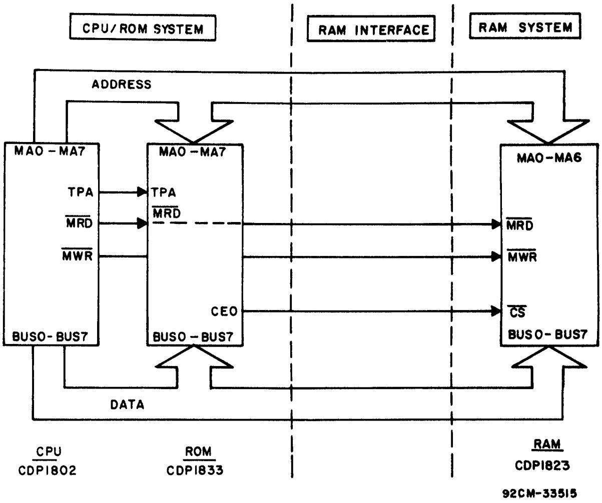
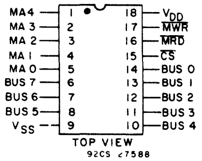


Fig. 5 - CDP1823 (128 x 8) minimum system (128 x 8)

CDP1824, CDP1824C



Terminal Assignment

32-Word x 8-Bit Static Random-Access Memory

Features:

- Access time:
  710 ns at V_{DD}=5 V,
  320 ns at V_{DD}=10 V
- No precharge or clock required

The RCA-CDP1824 and CDP1824C types are 32-word x 8-bit fully static CMOS random-access memories for use in CDP1800 series microprocessor systems. These parts are compatible with the CDP1802 microprocessor and will interface directly without additional components.

The CDP1824 is fully decoded and does not require a precharge or clocking signal for proper operation. It has common input and output and is operated from a single voltage supply. The $\overline{MRD}$ signal (output disable control) enables the three-state output drivers, and overrides the $\overline{MWR}$ signal. A $\overline{CS}$ input is provided for memory expansion.

The CDP1824C is functionally identical to the CDP1824. The CDP1824 has an operating range of 4 to 10.5 volts, and the CDP1824C has an operating voltage range of 4 to 6.5 volts. The CDP1824 and CDP1824C types are supplied in 18-lead hermetic dual-in-line ceramic packages (D suffix) and in 18-lead dual-in-line plastic packages (E suffix).

OPERATIONAL MODES

Function	$\overline{CS}$	$\overline{MRD}$	$\overline{MWR}$	Data Pins Status
READ	0	0	X	Output: High/ Low Dependent on Data
WRITE	0	1	0	Input: Output Disabled
Not Selected	1	X	X	Output Disabled: High-Impedance State
Standby	0	1	1	

Logic 1 = High   Logic 0 = Low   X = Don't Care

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (All voltage values referenced to V_{SS} terminal)	
CDP1824	−0.5 to +11 V
CDP1824C	−0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
OPERATING-TEMPERATURE RANGE (T_A).	
CERAMIC PACKAGES (D SUFFIX TYPES)	−55 to +125°C
PLASTIC PACKAGES (E SUFFIX TYPES)	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

File Number **1103**

OPERATING CONDITIONS at T_A = Full Package-Temperature Range
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
	V_{DD} (V)	CDP1824D CDP1824E		CDP1824CD CDP1824CE		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range	–	4	10.5	4	6.5	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise or Fall Time,▲ t_r,t_f	5	–	5	–	5	µs
	10	–	2	–	–	

▲ Input signal rise or fall times longer than these maxima can cause loss of stored data in either the selected or deselected mode.

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to + 85°C, Except as noted

CHARACTERISTICS	TEST CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1824			CDP1824C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	—	—	5	—	25	50	—	100	200	µA
	—	—	10	—	250	500	—	—	—	
Output Voltage: Low-Level, V_{OL}	—	0,5	5	—	0	0.1	—	0	0.1	V
	—	0,10	10	—	0	0.1	—	—	—	
High-Level, V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
	1,9	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	1,9	—	10	7	—	—	—	—	—	
Output Low (Sink) Current, I_{OL}	0.4	0,5	5	1.8	2.2	—	1.8	2.2	—	mA
	0.5	0,10	10	3.6	4.5	—	—	—	—	
Output High (Source) Current, I_{OH}	4.6	0,5	5	-0.9	-1.1	—	-0.9	-1.1	—	
	9.5	0,10	10	-1.8	-2.2	—	—	—	—	
Input Current, I_{IN}	Any input	0,5	5	—	±0.1	±1	—	±0.1	±1	µA
		0,10	10	—	±0.1	±1	—	—	—	
3-State Output Leakage Current, I_{OUT}	0,5	0,5	5	—	±0.2	±2	—	±0.2	±2	
	0,10	0,10	10	—	±0.2	±2	—	—	—	
Operating Current, I_{DD1}†	—	0,5	5	—	4	8	—	4	8	mA
	—	0,10	10	—	8	16	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	

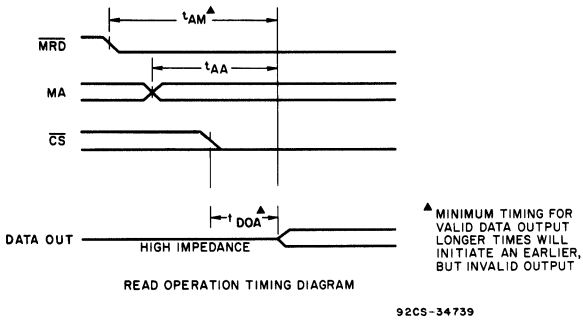
†Outputs open circuited; cycle time = 1 µs.
*Typical values are for T_A = 25°C and nominal V_{DD}.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD} ±5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200 kΩ; See Fig. 1.

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1824D CDP1824E			CDP1824CD CDP1824CE			
		Min.#	Typ.●	Max.	Min.#	Typ.●	Max.	
Read Operation								
Access Time From Address Change, t_{AA}	5	–	400	710	–	400	710	ns
	10	–	200	320	–	–	–	
Access Time From Chip Select, t_{DOA}	5	–	300	710	–	300	710	ns
	10	–	150	320	–	–	–	
Output Active From $\overline{\text{MRD}}$, t_{AM}	5	–	300	710	–	300	710	ns
	10	–	150	320	–	–	–	

# Time required by a limit device to allow for the indicated function

● Time required by a typical device to allow for the indicated function Typical values are for T_A = 25°C and nominal V_{DD}.



▲MINIMUM TIMING FOR VALID DATA OUTPUT LONGER TIMES WILL INITIATE AN EARLIER, BUT INVALID OUTPUT

READ OPERATION TIMING DIAGRAM

Fig. 1 - Read cycle timing diagram.

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1824. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1824 is used with the CDP1802 microprocessor:

t_{WW} = 2 t_C
t_{AH} = 1.0 t_C
t_{AS} = 4.5 t_C

$$\left.\begin{array}{l} t_{DH} = 1.0\ t_C \\ t_{DS} = 5.5\ t_C \end{array}\right\}\ \text{Data transfers from CDP1802 to memory}$$

$\overline{\text{MRD}}$ occurs one clock period (t_C) earlier than the address bits MA0-MA7.

$$\text{where } t_C = \frac{1}{\text{CDP1802 clock frequency}}$$

The CDP1824 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD} ±5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200 kΩ; See Fig. 2.

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1824D CDP1824E			CDP1824CD CDP1824CE			
		Min.#	Typ.●	Max.	Min.#	Typ.●	Max.	
Write Operation								
Write Pulse Width, t_{WRW}	5 10	390 180	200 150	– –	390 –	200 –	– –	ns
Data Setup Time, t_{DS}	5 10	390 180	100 50	– –	390 –	100 –	– –	ns
Data Hold Time, t_{DH}	5 10	70 35	40 20	– –	70 –	40 –	– –	ns
Chip Select Setup Time, t_{CS}	5 10	425 215	210 110	– –	425 –	210 –	– –	ns
Address Setup Time, t_{AS}	5 10	640 390	500 300	– –	640 –	500 –	– –	ns

# Time required by a limit device to allow for the indicated function

● Time required by a typical device to allow for the indicated function. Typical values are for T_A = 25°C and nominal V_{DD}

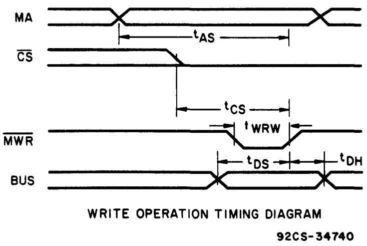


Fig. 2 - Write cycle timing diagram.

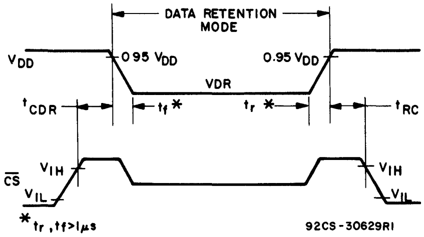


Fig. 3 - Low V_{DD} data retention waveforms and timing diagram.

CDP1824, CDP1824C

DATA RETENTION CHARACTERISTICS at T_A = –40 to +85°C; See Fig. 3.

CHARACTERISTIC	TEST CONDITIONS		CDP1824		CDP1824C		UNITS
		V_{DD} (V)	Min.	Max.	Min.	Max.	
Data Retention Voltage, V_{DR}		–	2.5	–	2.5	–	V
Data Retention Quiescent Current, I_{DD}	V_{DR} = 2.5 V	–	–	10	–	40	μA
Chip Deselect to Data Retention Time, t_{CDR}	V_{DR} = 2.5 V	5 10	600 300	– –	600 –	– –	ns
Recovery to Normal Operation Time, t_{RC}	V_{DR} = 2.5 V	5 10	600 300	– –	600 –	– –	

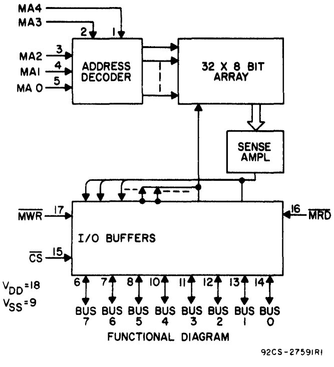


Fig. 4 - Functional diagram.

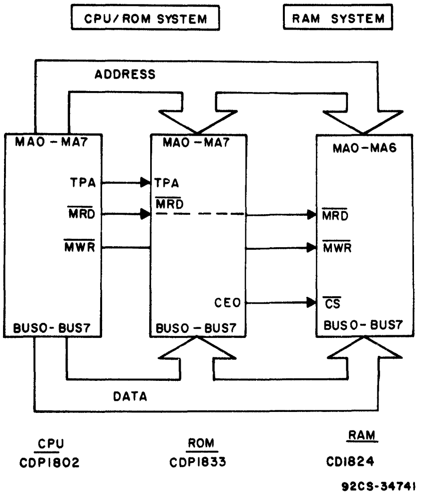
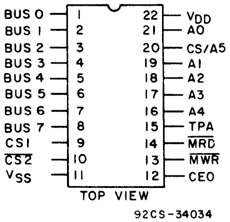


Fig. 5 - CDP1824 (128 x 8) minimum system (128 x 8)

CDP1826C



TERMINAL ASSIGNMENT

CMOS 64-Word x 8-Bit Static Random-Access Memory

Features:

- *Ideal for small, low-power RAM Memory requirements in microprocessor and microcomputer applications*
- *Interfaces with CDP1800-series microprocessors without additional address decoding*
- *Daisy chain feature to further reduce external decoding needs*
- *Multiple chip-select inputs for versatility*
- *Single voltage supply*
- *No clock or precharge required*

The RCA CDP1826C is a general-purpose, fully static, 64-word x 8-bit random-access memory, for use in CDP1800 series or other microprocessor systems where minimum component count and/or price performance and simplicity in use are desirable.

The CDP1826C has 8 common data input and data-output terminals with 3-state capability for direct connection to a standard bi-directional data bus Two chip-select inputs — CS1 and $\overline{\text{CS2}}$ — are provided to simplify memory-system expansion. An additional select pin, CS/A5, is provided to enable the CDP1826C to be selected directly from the CDP1800 multiplexed address bus without additional latching or decoding In an 1800 system, the CS/A5 pin can be tied to any MA address line from the CDP1800 processor. A TPA input is provided to latch the high-order bit of this address line as a chip-select for the CDP1826C. If this CS/A5 input is latched high, and if CS = 1 and $\overline{\text{CS2}}$ = 0 at the appropriate time in the memory cycle, the CDP1826C will be enabled for writing or reading. In a non-1800 system, the TPA pin can be tied high, and the CS/A5 pin can be used as a normal address input

The six input-address buffers are gated with the chip-select function to reduce standby current when the device is deselected, as well as to provide for a simplified power down mode by reducing address buffer sensitivity to long fall times from address drivers which are being powered down

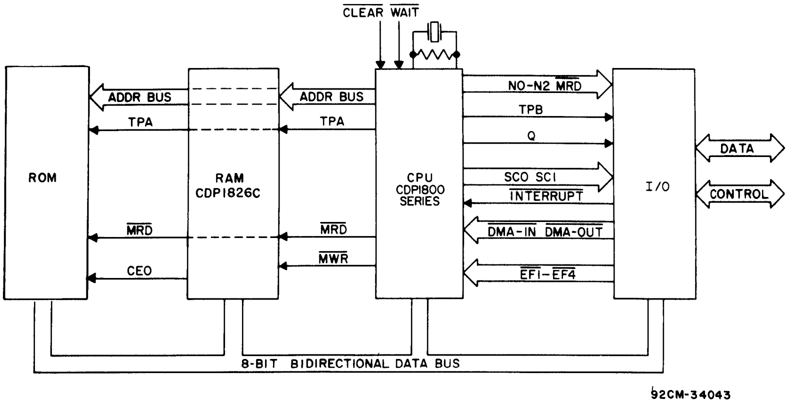

$\overline{\text{CLEAR}}$
$\overline{\text{WAIT}}$
ROM
ADDR BUS
TPA
$\overline{\text{MRD}}$
CEO
RAM
CDP1826C
ADDR BUS
TPA
$\overline{\text{MRD}}$
$\overline{\text{MWR}}$
CPU
CDP1800
SERIES
NO-N2 $\overline{\text{MRD}}$
TPB
Q
SCO SCI
$\overline{\text{INTERRUPT}}$
$\overline{\text{DMA-IN}}$ $\overline{\text{DMA-OUT}}$
$\overline{\text{EF1}}$-$\overline{\text{EF4}}$
I/O
DATA
CONTROL
8-BIT BIDIRECTIONAL DATA BUS
92CM-34043

Fig 1 - Typical CDP1802 microcprocessor system

File Number **1311**

Two memory control signals, $\overline{\text{MRD}}$ and $\overline{\text{MWR}}$, are provided for reading from and writing to the CDP1826C. The logic is designed so that $\overline{\text{MWR}}$ overrides $\overline{\text{MRD}}$, allowing the chip to be controlled from a single R/$\overline{\text{W}}$ line

For such an interface, the $\overline{\text{MRD}}$ line can be tied to V_{SS}, with the $\overline{\text{MWR}}$ line connected to R/$\overline{\text{W}}$.

A CHIP ENABLE OUTPUT is provided for daisy-chaining to additional memories or I/O devices. This output is high whenever the chip-select function selects the CDP1826C, which deselects any other chip which has its $\overline{\text{CS}}$ input connected to the CDP1826C CEO output. The connected chip is selected when the CDP1826C is de-selected and the $\overline{\text{MRD}}$ input is low. Thus, the CEO is only active for a read cycle and can be set up so that a CEO of another device can feed the $\overline{\text{MRD}}$ of the CDP1826C, which in turn selects a third chip in the daisy chain.

The CDP1826C has a recommended operating voltage of 4.5 to 5.5 V and is supplied in 22-lead hermetic dual-in-line side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix). The CDP1826C is also available in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	−0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A = −40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 12 mW/° C to 200 mW
For T_A = −55 to +100° C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D)	Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPE D	−55 to +125° C
PACKAGE TYPE E	−40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265° C

RECOMMENDED OPERATING CONDITIONS *at T_A = Full Package Temperature Range.*
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	CDP1826C		
	MIN.	MAX.	
DC Operating Voltage Range	4.5	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	
Input Signal Rise or Fall Time t_r, t_f V_{DD} = 5 V	—	10	µs

STATIC ELECTRICAL CHARACTERISTICS *at $T_A = -40$ to $+85°C$, $V_{DD} = 5V \pm 5\%$ except as noted*

CHARACTERISTIC		CONDITIONS		LIMITS			UNITS
		V_O (V)	V_{IN} (V)	CDP1826C			
				MIN.	TYP.•	MAX.	
Quiescent Device Current	I_{DD}	—	0,V_{DD}	—	5	50	µA
Output Low Drive (Sink) Current	I_{OL} BUS	0.4	0,V_{DD}	1.6	3.2	—	mA
	I_{OL} CEO			0.8	1.6	—	
Output High Drive (Sink) Current	I_{OH} BUS	V_{DD}-0.4	0,V_{DD}	-1.0	-1.5	—	
	I_{OH} CEO			-0.6	-1.0	—	
Output Voltage Low Level	V_{OL}	—	0,V_{DD}	—	0	0.1	V
Output Voltage High Level	V_{OH}	—	0,V_{DD}	V_{DD}-0.1	V_{DD}	—	
Input Low Voltage	V_{IL}		—	—	—	1.5	
Input High Voltage	V_{IH}		—	3.5	—	—	
Input Leakage Current	I_{IN}	Any Input	0,V_{DD}	—	±0.1	±1	µA
3-State Output Leakage Current	I_{OUT}	0,V_{DD}	0,V_{DD}	—	±0.1	±1	
Operating Device Current	I_{OPER}†	—	0,V_{DD}	—	5	10	mA
Input Capacitance	C_{IN}	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	0,V_{DD}	—	10	15	

•Typical values are for $T_A = 25°C$ and nominal V_{DD}.
†Outputs open circuited, cycle times = 1 µs

Signal Descriptions

A0-A4, CS/A5 (Address Inputs):

These inputs must be stable prior to a write operation, but may change asynchronously during Read operations.

In an 1800 system, the multiplexed high-order address bit at pin CS/A5 can be latched at the end of TPA A high level will provide a valid chip select for the CDP1826C. The low-order address bit which appears after TPA is used for data word selection. In non-1800 systems, TPA can be tied high to disable the latch and allow the CS/A5 pin to function as a normal address input.

BUS 0 — BUS 7: 8-bit 3-state common input/output data bus.

TPA: High-order address strobe input. The high-order address bit at input CS/A5 is latched on the high-to-low transition of the TPA input. Tie TPA high to disable the CS/A5 latch feature.

CS1, $\overline{\text{CS2}}$ (Chip Selector):

Either chip select (CS1 or $\overline{\text{CS2}}$), when not valid, powers down the chip, disables READ and WRITE functions, and gates off the address and output buffers.

$\overline{\text{MRD}}$, $\overline{\text{MWR}}$: Read and Write control signals. $\overline{\text{MWR}}$ overides $\overline{\text{MRD}}$, allowing the CDP1826C to be controlled from a single R/$\overline{\text{W}}$ line.

CEO (Chip Enable Output):

Allows daisy chaining to additional memories. CEO is high whenever the CDP1826C is selected. CEO is only active (low) for a Read cycle with the CDP1826C deselected and the $\overline{\text{MRD}}$ input low.

V_{DD}, V_{SS}: Power supply connections.

CDP1826C

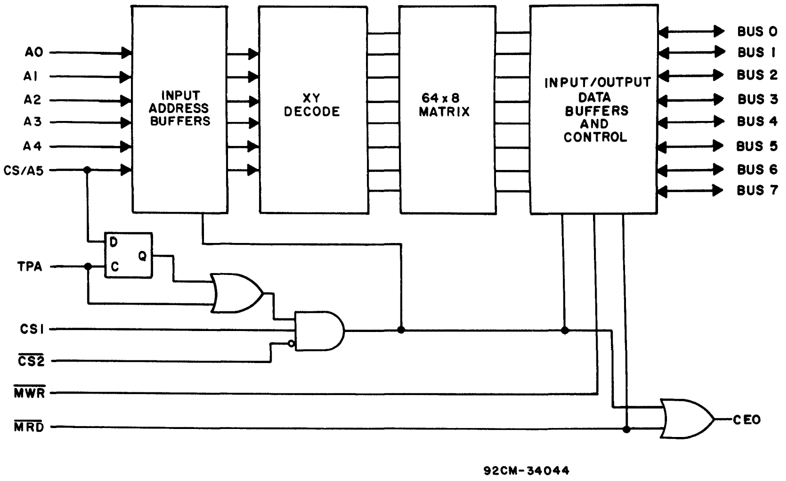
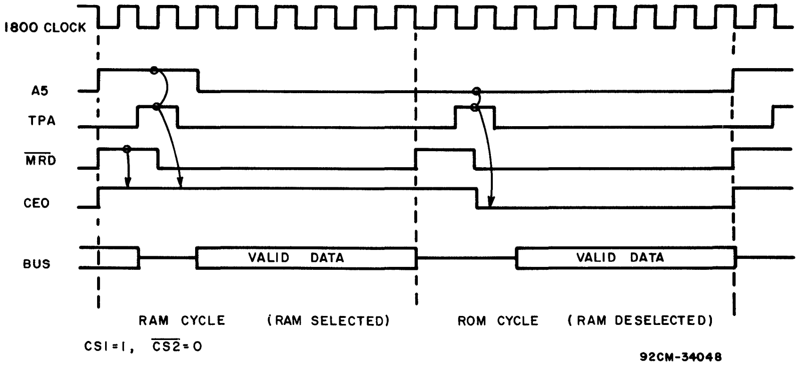


Fig. 2 - Functional diagram



OPERATING MODES

	FUNCTION	$\overline{MRD}$	$\overline{MWR}$	CS1·$\overline{CS2}$	TPA	CS/A5#	CEO
CDP1800 MODE	WRITE	X	0	1	⎍	1	1
	READ	0	1	1	⎍	1	1
	DESELECT	1	1	1	⎍	1	1
	DESELECT	1	X	0	X	X	1
	DESELECT	0	X	0	X	X	0
	DESELECT	1	X	X	⎍	0	1
	DESELECT	0	X	X	⎍	0	0
NON-CDP1800 MODE	WRITE	X	0	1	1	X	1
	READ	0	1	1	1	X	1
	DESELECT	1	1	1	1	X	1
	DESELECT	1	X	0	1	X	1
	DESELECT	0	X	0	1	X	0

FOR CDP1800 MODE, REFERS TO HIGH ORDER MEMORY ADDRESS BIT LEVEL AT TIME WHEN TPA ↓ TRANSITION TAKES PLACE

Fig 3 - Chip Enable Output timing waveforms for CDP1800-based systems.

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = -40$ to $+85°C$, $V_{DD} = 5\ V \pm 5\%$, Input $t_r, t_f = 10$ ns; $C_L = 50$ pF and 1 TTL Load*

CHARACTERISTIC		LIMITS		UNITS
		CDP1826C		
	MIN.†	TYP.•	MAX.	
Read — Cycle Times (Figs. 4 and 5)				
Address to TPA Setup t_{ASH}	100	—	—	ns
Address to TPA Hold t_{AH}	100	—	—	
Access from Address Change T_{AA}	—	500	1000	
TPA Pulse Width t_{PAW}	200	—	—	
Output Valid from $\overline{MRD}$ t_{AM}	—	500	1000	
Access from Chip Select t_{AC}	—	500	1000	
CEO Delay from TPA ↘ Edge t_{CA}	—	150	300	
$\overline{MRD}$ to CEO Delay t_{MC}	75	—	—	
Output High Z from Invalid $\overline{MRD}$ t_{RHZ}	—	—	125	
Output High Z from Chip Deselect t_{SHZ}	—	—	225	

†Time required by a limit device to allow for the indicated function
•Typical values are for $T_A = 25°C$ and nominal V_{DD}.

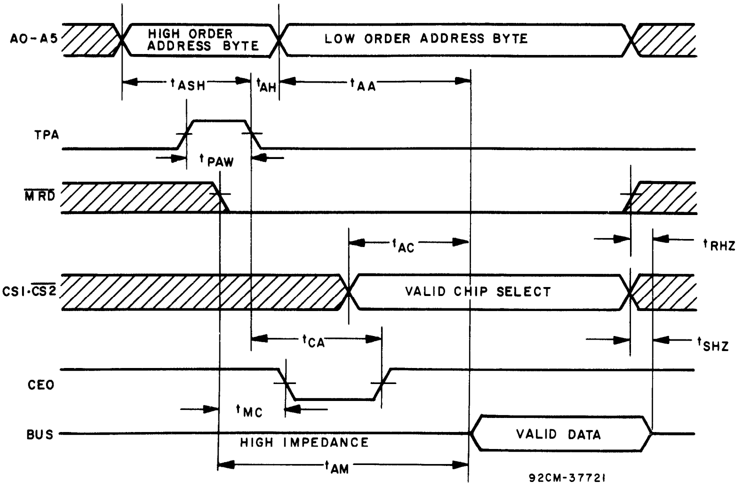


Fig. 4 - Timing waveforms for Read-cycle 1.

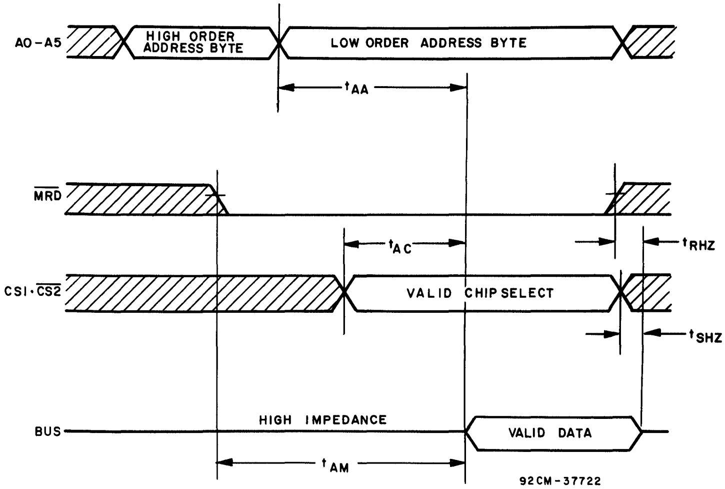


Fig. 5 - Timing waveforms for Read-cycle 2 [TPA-High].

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = -40$ to $+85°$ C, $V_{DD} = 5$ V ±5%, Input $t_r, t_f = 10$ ns; $C_L = 50$ pF and 1 TTL Load*

CHARACTERISTIC	LIMITS			UNITS
	CDP1826C			
	MIN.†	TYP.•	MAX.	
Write-Cycle Times (Figs. 6 and 7)				
Address to TPA Setup, High Byte t_{ASH}	100	—	—	ns
Address to TPA Hold t_{AH}	100	—	—	
Address Setup Low Byte t_{ASL}	500	250	—	
TPA Pulse Width t_{PAW}	200	—	—	
Chip Select Setup t_{CS}	700	350	—	
Write Pulse Width t_{WW}	300	200	—	
Write Recovery t_{WR}	100	—	—	
Data Setup t_{DS}	400	200	—	
Data Hold from End of $\overline{MWR}$ t_{DH1}	100	50	—	
Data Hold from End of Chip Select t_{DH2}	125	50	—	

†Time required by a limit device to allow for the indicated function.
•Typical values are for $T_A = 25°$C and nominal V_{DD}.

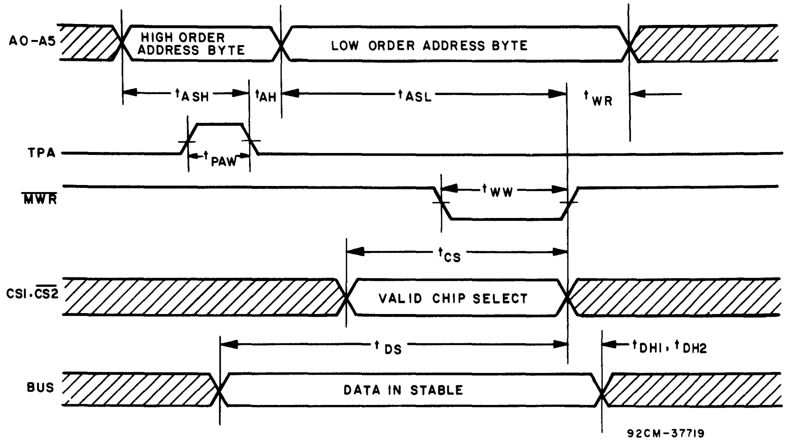


Fig. 6 - Timing waveforms for Write-cycle 1

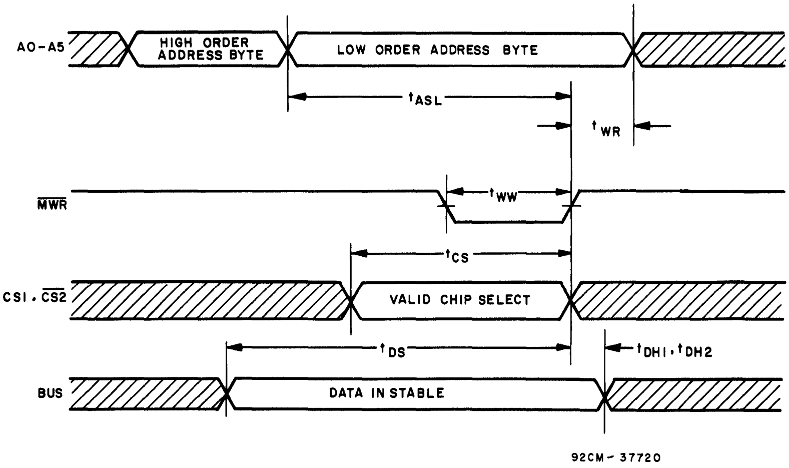


Fig. 7 - Timing waveforms for Write-cycle 2 [TPA=High].

CDP1826C

DATA RETENTION CHARACTERISTICS *at $T_A = -40$ to $+85°C$; see Fig. 8*

CHARACTERISTIC	TEST CONDITIONS		LIMITS CDP1826C			UNITS
	V_{DR} (V)	V_{DD} (V)	MIN.	TYP.•	MAX.	
Min. Data Retention Voltage V_{DR}	—	—	—	2	2.5	V
Data Retention Quiescent Current I_{DD}	2.5	—	—	5	25	μA
Chip Deselect to Data Retention Time t_{CDR}	—	5	600	—	—	ns
Recovery to Normal Operation Time t_{RC}	—	5	600	—	—	
V_{DD} to V_{DR} Rise and Fall Time t_r, t_f	2.5	5	1	—	—	μs

•Typical values are for $T_A = 25°C$ and nominal V_{DD}

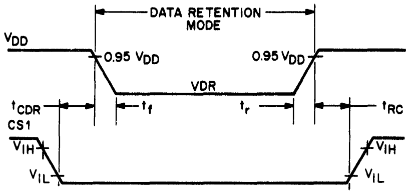


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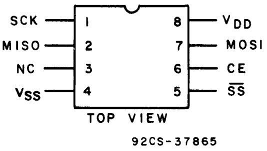
Fig. 8 - Low V_{DD} data retention timing waveforms.

Product Preview

CDP68HC68R1, CDP68HC68R2

CMOS 128-Word (CDP68HC68R1) and 256-Word (CDP68HC68R2) by 8-Bit Static RAMs



TERMINAL ASSIGNMENT

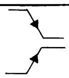
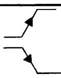
Features:

- *Fully static operation*
- *Operating voltage range: 3 V to 5.5 V*
- *Typical standby current=1 µA*
- *Directly compatible with RCA/Motorola SPI bus*
- *Separate data input and three-state data output pins*
- *Input data and clock buffers gated off with chip enable*
- *Automatic sequencing for fast multiple-byte accesses*
- *Low minimum data retention voltage: 2 V*
- *Wide operating temperature range: −40° C to +85° C*

The RCA CDP68HC68R1 and CDP68HC68R2 are 128-word and 256-word by 8-bit static random-access memories, respectively. The memories are intended for use in systems utilizing a synchronous serial three-wire (clock, data in, and data out) interface where minimum package size, interconnect wiring, low power, and simplicity of use are desirable. These parts will interface directly with RCA's CDP68HC05D2, CDP68HC05C4, and CDP68HC05C8 microcomputers (providing the CPHA bit in the microcomputer's SPI Control Register is set equal to 1). The CDP68HC68R1 and CDP68HC68R2 are also compatible with general-purpose microcomputers, including RCA's CDP1804A and CDP6805 family, by utilizing I/O bits for the SPI (Serial Peripheral Interface) bus. Other industry microcomputers such as the 80C51 can also interface to these serial RAM's.

The CDP68HC68R1 and CDP68HC68R2 are supplied in 8-lead plastic Mini-DIP packages (E suffix).

TRUTH TABLE

MODE	SIGNAL				
	CE	$\overline{SS}$	SCK	MOSI	MISO
DISABLED & RESET	L X	X H	INPUT DISABLED	INPUT DISABLED	HIGH Z
READ OR WRITE	H	L	CPOL=0,  CPOL=1,	DATA BIT LATCH	HIGH Z DURING WRITE, CURRENT DATA BIT DURING READ
SHIFT	H	L	CPOL=0,  CPOL=1,	X	NEXT DATA BIT

NOTE:
MISO remains at a High Z until 8 bits of data are ready to be shifted out during a Read and it remains at a HIGH Z during the entire Write cycle.
The CPHA bit must be set = 1 in the Serial Perpherial Control Register of 6805 microcomputers in order to Communicate with these devices.

File Number **1544**

CDP68HC68R1, CDP68HC68R2

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):	
(All voltage values referenced to V_{SS} terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)·	
For T_A=-40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A=FULL PACKAGE-TEMPERATURE RANGE	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE E	-40° to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 0.79 mm) from case for 10 s max.	+265°C

OPERATING CONDITIONS at T_A = -40° to +85°C
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS ALL TYPES MIN.	LIMITS ALL TYPES MAX.	UNITS
DC Operating Voltage Range		3	5.5	V
Input Voltage Range	V_{IH}	0.7 V_{DD}	V_{DD} +0.3	
	V_{IL}	-0.3	0.2 V_{DD}	
Serial Clock Frequency	f_{SCK}			MHz
	V_{DD}=3 V	—	1.05	
	V_{DD}=4.5 V	—	2.1	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = 3.3 V ±10%, Except as Noted

CHARACTERISTIC	CONDITIONS	LIMITS CDP68HC68R1 MIN.	CDP68HC68R1 TYP.•	CDP68HC68R1 MAX.	CDP68HC68R2 MIN.	CDP68HC68R2 TYP.•	CDP68HC68R2 MAX.	UNITS
Standby Device Current I_{DDS}	—	—	1	15	—	1	50	μA
Output Voltage High Level V_{OH}	I_{OH}=-0.4 mA, V_{DD}=3 V	2.7	—	—	2.7	—	—	V
Output Voltage Low Level V_{OL}	I_{OL}=0.4 mA, V_{DD}=3 V	—	—	0.3	—	—	0.3	
Input Leakage Current, I_{IN}	—	—	*	±1	—	*	±1	μA
3-State Output Leakage Current, I_{OUT}	—	—	—	±10	—	—	±10	
Operating Device Current I_{OPER}#	V_{IN}=V_{IL},V_{IH}	—	5	10	—	5	10	mA
Input Capacitance, C_{IN}	V_{IN}=0 V, f=1 MHz, T_A=25°C	—	4	6	—	4	6	pF

•Typical values are for T_A = 25°C and nominal V_{DD}.

#Outputs open circuited; cycle time = Min. t_{cycle}, duty = 100%.

*Typical input current values (high and low) for pins 1, 5, 6, 7, approximately 100 nA due to presence of feedback transistor. Pin 6 is an exception - I_{in}(high) typically 1 nA.

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ±10%, Except as Noted

CHARACTERISTIC	CONDITIONS	LIMITS						UNITS
		CDP68HC68R1			CDP68HC68R2			
		MIN.	TYP.•	MAX.	MIN.	TYP.•	MAX.	
Standby Device Current I_{DDS}	—	—	1	15	—	1	50	µA
Output Voltage High Level V_{OH}	I_{OH}=-1.6 mA, V_{DD}=4.5 V	3.7	—	—	3.7	—	—	V
Output Voltage Low Level V_{OL}	I_{OL}=1.6 mA, V_{DD}=4.5 V	—	—	0.4	—	—	0.4	
Output Voltage High Level V_{OH}	$I_{OH} \leq 10$ µA, V_{DD}=4.5 V	4.4	—	—	4.4	—	—	
Output Voltage Low Level V_{OL}	$I_{OL} \leq 10$ µA, V_{DD}=4.5 V	—	—	0.1	—	—	0.1	
Input Leakage Current, I_{IN}	—	—	*	±1	—	*	±1	µA
3-State Output Leakage Current, I_{OUT}	—	—	—	±10	—	—	±10	
Operating Device Current I_{OPER}#	V_{IN}=V_{IL},V_{IH}	—	5	10	—	5	10	mA
Input Capacitance, C_{IN}	V_{IN}=0 V, f=1 MHz, T_A=25° C	—	4	6	—	4	6	pF

•Typical values are for T_A = 25° C and nominal V_{DD}.

#Outputs open circuited; cycle time = Min. t_{cycle}, duty = 100%.

*Typical input current values (high and low) for pins 1, 5, 6, 7, approximately 100 nA due to presence of feedback transistor. Pin 6 is an exception - I_{in}(high) typically 1 nA.

PIN SIGNAL DESCRIPTION

SCK (Serial Clock Input)* - This input causes serial data to be latched from the MOSI input and shifted out on the MISO output.

MOSI (Master Out/Slave In)* - Data bytes are shifted in at this pin most significant bit (MSB) first.

MISO (Master In/Slave Out)* - Data bytes are shifted out at this pin most significant bit (MSB) first.

$\overline{SS}$ (Slave Select)* - A negative chip select input. A high level at this input holds the serial interface logic in a reset state.

CE (Chip Enable)** - A positive chip enable input. A low level at this input holds the serial interface logic in a reset state.

CE · SS - This is a logical function of CE and $\overline{SS}$ used throughout this data sheet to simplify diagrams. CE · SS = 1 when pin 5 is low and pin 6 is high. CE · SS = 0 at all other times.

FUNCTIONAL DESCRIPTION

The Serial Peripheral Interface (SPI) utilized by the CDP68HC68R1 and CDP68HC68R2, is a serial synchronous bus for address and data transfers. The clock, which is generated by the microcomputer, is active only during address and data transfers. In systems using the CDP68HC05C4, CDP68HC05C8 or CDP68HC05D2, the inactive clock polarity is determined by the CPOL bit in the microcomputer's control register. A unique feature of the CDP68HC68R1 and CDP68HC68R2 is that they automatically determine the level of the inactive clock by sampling SCK when CE • SS becomes active (see Fig. 1). Input data (MOSI) is latched internally on the Internal Strobe edge and output data (MISO) is shifted out on the Shift edge, as defined by Fig. 1. There is one clock for each data bit transferred (address as well as data bits are transferred in groups of 8).

ADDRESS AND DATA FORMAT

The address and data bytes are shifted MSB first into the serial data input (MOSI) and out of the serial data output (MISO). The Address/Control byte (see Fig. 2b) contains a Write/$\overline{\text{Read}}$ bit and a 7-bit address. Any transfer of data requires an Address/Control byte to specify a RAM location, followed by one or more bytes of data. Data is transferred out of MISO for a Read and into MOSI for a Write. Address/Control bytes are recognizable because they are the first byte transferred following a valid CE · SS (except for Page select bytes, see PAGE SELECTION). To transmit a new address, CE · SS must first go false and then true again.

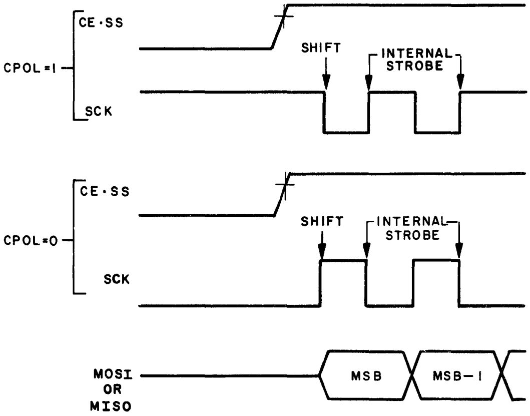


Fig. 1 - Serial RAM clock (SCK) as a function of MCU clock polarity (CPOL).

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*These inputs will retain their previous state if the line driving them goes into a HIGH-Z state.

**The CE input has an internal pull-down device—if the input is driven to a low state before going to a HIGH Z.

a. Page/Device Byte (CDP68HC68R2 Only)

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	X	**X**	**X**	**X**	**X**	**X**	**X**	**A7**

b. Address/Control Byte

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	W/$\overline{R}$	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**

A0-A6 The seven least significant RAM address bits, sufficient to address 128 bytes.

W/$\overline{R}$ Read or Write data transfer control bit. W/$\overline{R}$ = 0 initiates one or more memory read cycles. W/$\overline{R}$ = 1 initiates one or more memory write cycles.

c. Data Byte

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

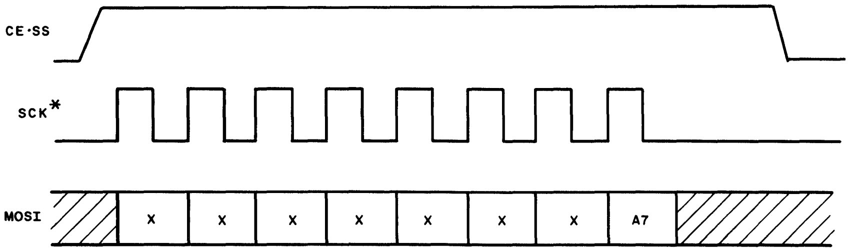
Fig. 2 - Serial byte format.

PAGE SELECTION (CDP68HC68R2 Only)

For the CDP68HC68R2, a Page/Device byte is sent from the microcomputer before the Address/Control byte. Because the Address/Control byte is limited to 128 addresses, the CDP68HC68R2 is divided into two 128-byte pages. A page select is accomplished by enabling the CDP68HC68R2, transmitting the Page/Device Select byte (see Fig. 2a), and finally disabling the device prior to any more data transfers. The Page/Device byte is recognizable because it is the only time that a single byte is transferred to the RAM before CE · SS is disabled (see Fig. 3). The page select is latched and remains until changed or is incremented during a burst transfer (see next section).

ADDRESS AND DATA

Data transfers can occur one byte at a time (Fig. 4) or in a multi-byte burst mode (Fig. 5). After the chip is enabled, an address word is sent to select one of the 128 bytes (on the selected page) and specify the type of operation (i.e., Read or Write). For a single byte Read or Write (Fig. 4), one byte is transferred to or from the location specified in the Address/Control byte; the device is then disabled. Additional reading or writing requires re-enabling the RAM and providing a new Address/Control byte. If the RAM is not disabled, additional bytes can be read or written in a burst mode (Fig. 5). Each Read or Write cycle causes the latched



* SCK CAN BE EITHER POLARITY.

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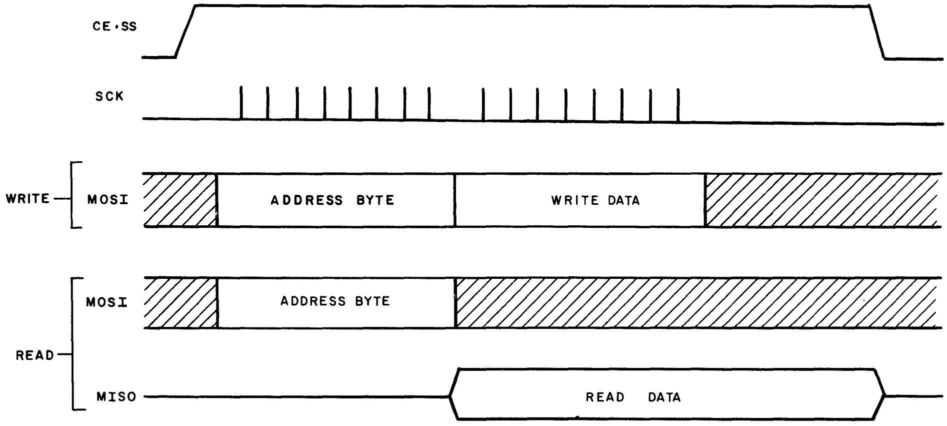
Fig. 3 - Page/Device Select byte transfer waveforms.



92CM-37717

Fig. 4 - Single-byte transfer.

CDP68HC68R1, CDP68HC68R2

RAM address to automatically increment. Incrementing continues after each transfer until the device is disabled. After incrementing to 7FH on the CDP68HC68R1 or to FFH on the CDP68HC68R2, the address will recycle to 00H and continue. Note that incrementing past 7FH on the CDP-68HC68R2 causes the address to go to location 80H (i.e., location 00H of page 1). The programmer must take care to keep track when crossing page boundaries.

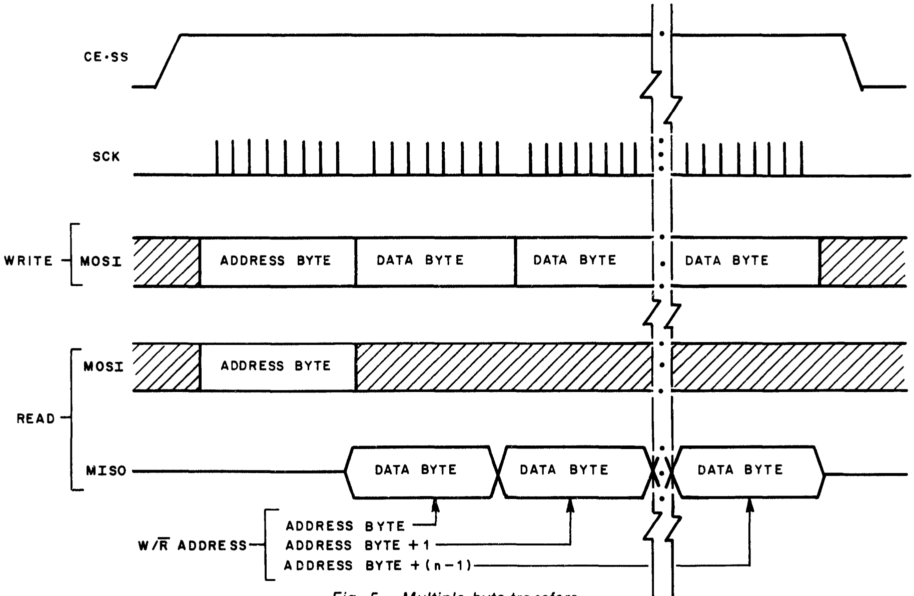


Fig. 5 - Multiple-byte transfers.

DYNAMIC ELECTRICAL CHARACTERISTICS - BUS TIMING V_{DD} ±10%, V_{SS} = 0 V dc, T_A = -40° to +85° C, C_L = 200 pF. See Figs. 6, 7 and 8.

IDENT. NUMBER	CHARACTERISTIC		LIMITS (ALL TYPES)				UNITS
			V_{DD}=3.3 V		V_{DD}=5 V		
			Min.	Max.	Min.	Max.	
①	Chip Enable Set-Up Time	t_{EVCV}	200	—	100	—	ns
②	Chip Enable after Clock Hold Time	t_{CVEX}	250	—	125	—	
③	Clock Width High	t_{WH}	400	—	200	—	
④	Clock Width Low	t_{WL}	400	—	200	—	
⑤	Data In to Clock Set-Up Time	t_{DVCV}	200	—	100	—	
⑥	Data In after Clock Hold Time	t_{CVDX}	200	—	100	—	
⑦	Clock to Data Propagation Delay	t_{CVDV}	—	200	—	100	
⑧	Chip Disable to Output High Z	t_{EXQZ}	—	200	—	100	
⑪	Output Rise Time	t_r	—	200	—	100	
⑫	Output Fall Time	t_f	—	200	—	100	
Ⓐ	Clock to Data Out Active	t_{CVQX}	—	200	—	100	
Ⓑ	Clock Recovery Time	t_{REC}	200	—	200	—	

CDP68HC68R1, CDP68HC68R2

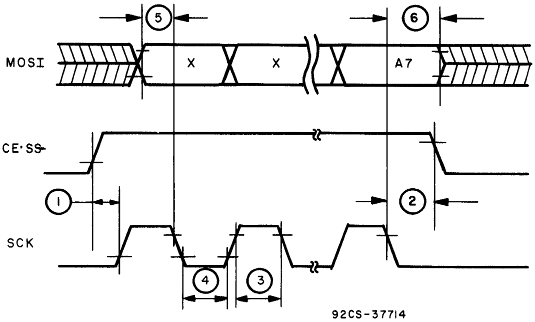


Fig. 6 - Page/Device byte timing waveforms.

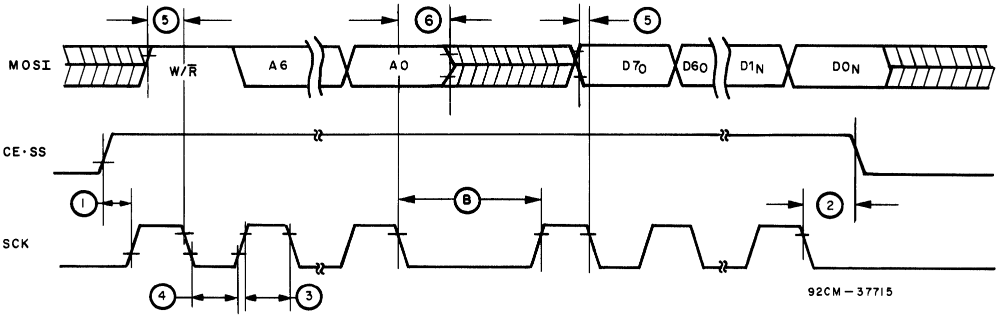


Fig. 7 - WRITE cycle timing waveforms.

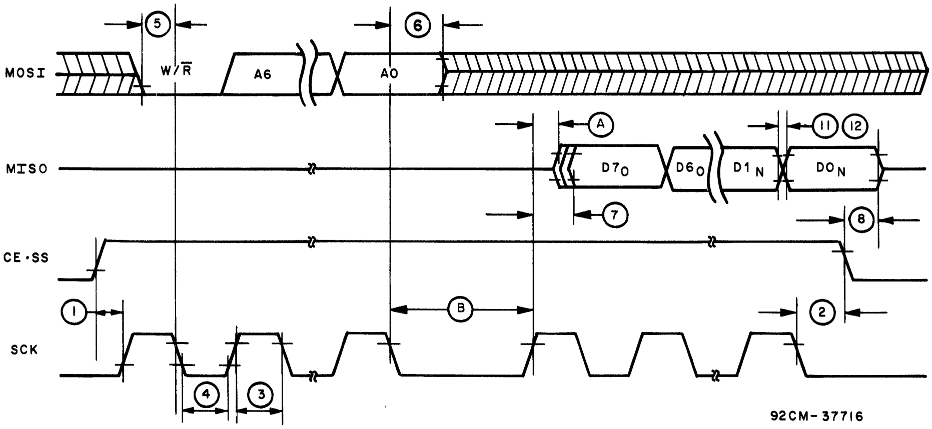
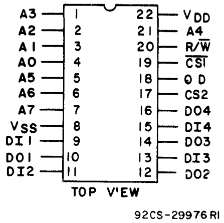


Fig. 8 - READ cycle timing waveforms.

DATA RETENTION CHARACTERISTICS at T_A = -40° to +85° C

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			ALL TYPES		
			MIN.	MAX.	
Minimum Data Retention Voltage	V_{DR}	$\overline{CS} \geq V_{DD} - 0.2$ V	2	—	V
Data Retention Quiescent Current	$I_{DD}DR$	$V_{DD} = 2$ V, $CE = V_{SS}$	—	1	μA

MWS5101



TERMINAL ASSIGNMENT

256-Word by 4-Bit LSI Static Random-Access Memory

Features:

- *Industry standard pinout*
- *Very low operating current-8 mA at V_{DD} = 5 V and cycle time = 1 µs*
- *Two Chip-Select inputs-simple memory expansion*
- *Memory retention for standby battery voltage of 2 V min*
- *Output-Disable for common I/O systems*
- *3-state data output for bus-oriented systems*
- *Separate data inputs and outputs*

The RCA-MWS5101 is a 256-word by 4-bit static random-access memory designed for use in memory systems where high speed, very low operating current, and simplicity in use are desirable. It has separate data inputs and outputs and utilizes a single power supply of 4 to 6.5 volts.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input condition. The output assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS}1$ and/or CS2.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5-V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

For applications requiring wider temperature and operating voltage ranges, the mechanically and functionally equivalent static RAM, RCA-CDP1822, may be used

The MWS5101 types are supplied in 22-lead hermetic dual-in-line, side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	Chip Select 1 $\overline{CS1}$	Chip Select 2 CS2	Output Disable OD	Read/$\overline{\text{Write}}$ R/$\overline{W}$	
READ	0	1	0	1	Read
WRITE	0	1	0	0	Data In
WRITE	0	1	1	0	High Impedance
STANDBY	1	X	X	X	High Impedance
STANDBY	X	0	X	X	High Impedance
OUTPUT DISABLE	X	X	1	X	High Impedance

Logic 1 = High   Logic 0 = Low   X = Don't Care

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})	
(All voltage referenced to V_{SS} terminal)	–0.5 to –7 V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A = –40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100° C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D)	Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPE D	–55 to +125° C
PACKAGE TYPE E	–40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg})	–65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1 59 ± 0 79 mm) from case for 10 s max	+265° C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS ALL TYPES Min.	LIMITS ALL TYPES Max.	UNITS
DC Operating-Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70°C, V_{DD} = 5 V ±5%.

CHARACTERISTIC		TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{IN} (V)	LIMITS MWS5101D MWS5101E Min.	Typ.●	Max.	UNITS
Quiescent Device Current, I_{DD}	L2 Types	–	0,5	–	25	50	µA
	L3 Types	–	0,5	–	100	200	
Output Voltage: Low-Level, V_{OL}		–	0,5	–	0	0.1	V
High-Level, V_{OH}		–	0,5	4.9	5	–	
Input Low Voltage, V_{IL}		–	–	–	–	1.5	
Input High Voltage, V_{IH}		–	–	3.5	–	–	
Output Low (Sink) Current, I_{OL}		0.4	0,5	2	4	–	mA
Output High (Source) Current, I_{OH}		4.6	0,5	–1	–2	–	
Input Current, I_{IN}		–	0,5	–	–	± 5	µA
3-State Output Leakage Current, I_{OUT}	L2 Types	0,5	0,5	–	–	± 5	
	L3 Types	0,5	0,5	–	–	± 5	
Operating Current, I_{DD1}#		–	0,5	–	4	8	mA
Input Capacitance, C_{IN}		–	–	–	5	7.5	pF
Output Capacitance, C_{OUT}		–	–	–	10	15	

● Typical values are for T_A = 25°C and nominal V_{DD}.

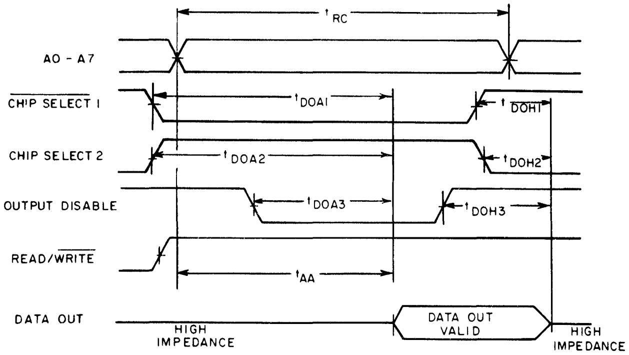
# Outputs open-circuited, cycle time=1 µs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70°C, V_{DD} = 5 V ±5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC	LIMITS						UNITS
	MWS5101D, MWS5101E						
	L2 Types			L3 Types			
	Min.†	Typ.●	Max.	Min.†	Typ.●	Max.	
Read Cycle Times (Fig. 1)							
Read Cycle t_{RC}	250	–	–	350	–	–	ns
Access from Address t_{AA}	–	150	250	–	200	350	
Output Valid from $\overline{\text{Chip-Select}}$ 1 t_{DOA1}	–	150	250	–	200	350	
Output Valid from Chip-Select 2 t_{DOA2}	–	150	250	–	200	350	
Output Valid from Output Disable t_{DOA3}	–	–	110	–	–	150	
Output Hold from $\overline{\text{Chip-Select}}$ 1 t_{DOH1}	20	–	–	20	–	–	
Output Hold from Chip-Select 2 t_{DOH2}	20	–	–	20	–	–	
Output Hold from Output Disable t_{DOH3}	20	–	–	20	–	–	

† Time required by a limit device to allow for the indicated function

● Typical values are for T_A = 25°C and nominal V_{DD}



92CM-30244R4

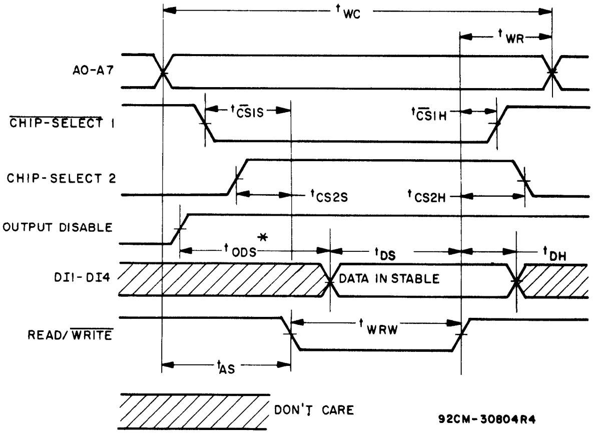
Fig. 1 - Read cycle timing waveforms

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70°C, V_{DD} = 5 V ±5%, t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC	LIMITS						UNITS
	MWS5101D, MWS5101E						
	L2 Types			L3 Types			
	Min.†	Typ.●	Max.	Min.†	Typ.●	Max.	
Write Cycle Times (Fig. 2)							
Write Cycle t_{WC}	300	–	–	400	–	–	ns
Address Setup t_{AS}	110	–	–	150	–	–	
Write Recovery t_{WR}	40	–	–	50	–	–	
Write Width t_{WRW}	150	–	–	200	–	–	
Input Data Setup Time t_{DS}	150	–	–	200	–	–	
Data In Hold t_{DH}	40	–	–	50	–	–	
$\overline{\text{Chip-Select}}$ 1 Setup $t_{\overline{CS}1S}$	110	–	–	150	–	–	
Chip-Select 2 Setup t_{CS2S}	110	–	–	150	–	–	
$\overline{\text{Chip-Select}}$ 1 Hold $t_{\overline{CS}1H}$	0	–	–	0	–	–	
Chip-Select 2 Hold t_{CS2H}	0	–	–	0	-	-	
Output Disable Setup t_{ODS}	110	–	–	150	–	–	

† Time required by a limit device to allow for the indicated function

● Typical values are for T_A = 25°C and nominal V_{DD}



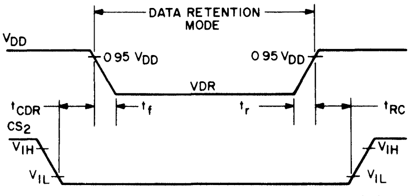
* t_{ODS} IS REQUIRED FOR COMMON I/O OPERATION ONLY, FOR SEPARATE I/O OPERATIONS, OUTPUT DISABLE IS DON'T CARE

Fig. 2 - Write cycle timing waveforms.

DATA RETENTION CHARACTERISTICS at $T_A = 0$ to 70° C; See Fig. 3

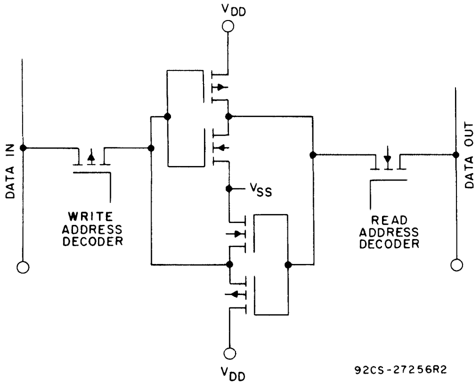
CHARACTERISTIC		TEST CONDITIONS		LIMITS			UNITS
		V_{DR} (V)	V_{DD} (V)	All Types			
				Min.	Typ.●	Max.	
Minimum Data Retention Voltage, V_{DR}		–	–	–	1.5	2	V
Data Retention Quiescent Current, I_{DD}	L2 Types	2	–	–	2	10	µA
	L3 Types			–	5	50	
Chip Deselect to Data Retention Time, t_{CDR}		–	5	600	–	–	ns
Recovery to Normal Operation Time, t_{RC}		–	5	600	–	–	
V_{DD} to V_{DR} Rise and Fall Time t_r, t_f		2	5	1	–	–	µs

● Typical values are for $T_A = 25^{\circ}C$ and nominal V_{DD}



92CS-30805R1

Fig. 3 - Low V_{DD} data retention timing waveforms.



92CS-27256R2

Fig. 4 - Memory cell configuration

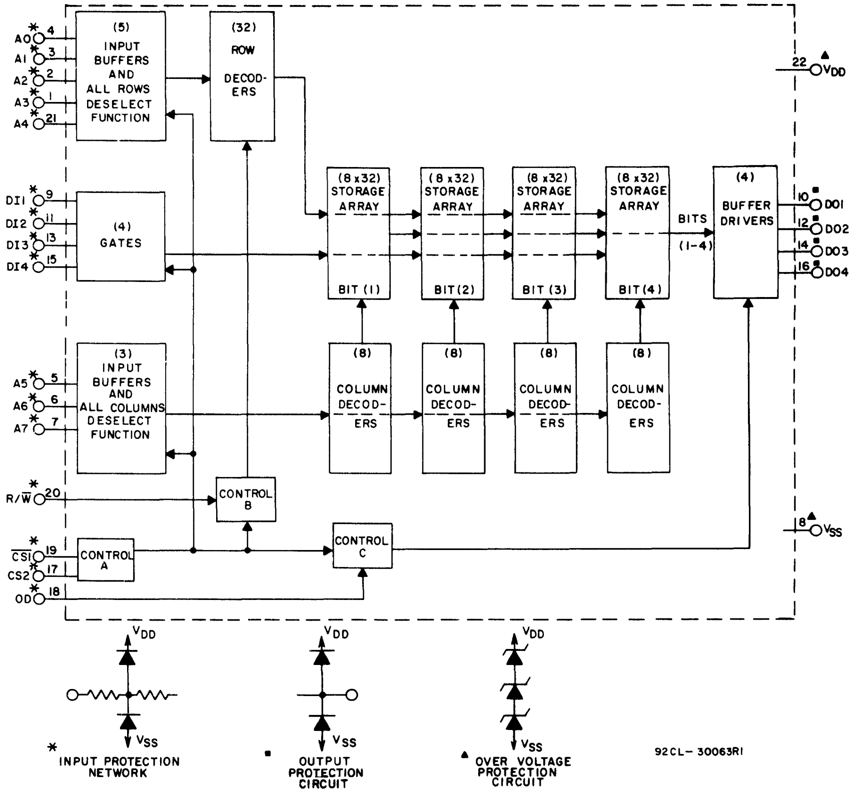


Fig 5 - Functional block diagram for MWS5101

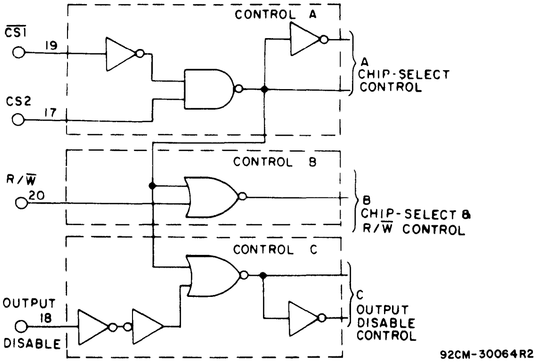
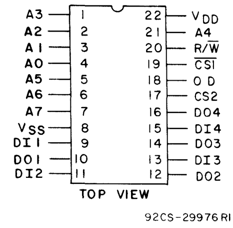


Fig 6 - Logic diagram of controls for MWS5101.

MWS5101A



TERMINAL ASSIGNMENT

256-Word by 4-Bit LSI Static Random-Access Memory

Features:

- *Industry standard pinout*
- *Very low operating current-8 mA at $V_{DD} = 5$ V and cycle time = 1 µs*
- *Two Chip-Select inputs-simple memory expansion*
- *Memory retention for standby battery voltage of 2 V min.*
- *TTL compatible*
- *Output-Disable for common I/O systems*
- *3-state data output for bus-oriented systems*
- *Separate data inputs and outputs*

The RCA-MWS5101A is a 256-word by 4-bit static random-access memory designed for use in memory systems where high speed, very low operating current, and simplicity in use are desirable It has separate data inputs and outputs and utilizes a single power supply of 4 to 6 5 volts.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. The Output Disable input allows these RAM's to be used in common data Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input condition. The output assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{\text{CS1}}$ and/or CS2

For applications requiring CMOS compatibility over wider operating voltage and temperature ranges, the mechanical and functional equivalent RCA-CDP1822 static RAM may be used

The MWS5101A types are supplied in 22-lead hermetic dual-in-line, side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	$\overline{\text{Chip Select 1}}$ $\overline{\text{CS1}}$	Chip Select 2 CS2	Output Disable OD	Read/$\overline{\text{Write}}$ R/$\overline{\text{W}}$	
READ	0	1	0	1	Read
WRITE	0	1	0	0	Data In
WRITE	0	1	1	0	High Impedance
STANDBY	1	X	X	X	High Impedance
STANDBY	X	0	X	X	High Impedance
OUTPUT DISABLE	X	X	1	X	High Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

File Number **1207**

OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS ALL TYPES Min.	LIMITS ALL TYPES Max.	UNITS
DC Operating-Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})

(All voltage referenced to V_{SS} terminal) .... −0.5 to −7 V

INPUT VOLTAGE RANGE, ALL INPUTS .... −0.5 to V_{DD} + 0.5 V

DC INPUT CURRENT, ANY ONE INPUT .... ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = −40 to +60°C (PACKAGE TYPE E) .... 500 mW

For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW

For T_A = −55 to +100°C (PACKAGE TYPE D) .... 500 mW

For T_A = +100 to +125°C (PACKAGE TYPE D) .... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW

OPERATING-TEMPERATURE RANGE (T_A).

PACKAGE TYPE D .... −55 to +125°C

PACKAGE TYPE E .... −40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) .... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70 °C, V_{DD} = 5 V

CHARACTERISTIC		TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{IN} (V)	LIMITS MWS5101AD MWS5101AE Min.	Typ.*	Max.	UNITS
Quiescent Device Current, I_{DD}	L2 Types	—	0, 5	—	25	50	μA
	L3 Types	—	0, 5	—	100	200	
Output Voltage: Low-Level,	V_{OL}	—	0, 5	—	0	0.1	V
High-Level,	V_{OH}	—	0, 5	4.9	5	—	
Input Low Voltage,	V_{IL}	—	—	—	—	0.65	
Input High Voltage,	V_{IH}	—	—	2.2	—	—	
Output Low (Sink) Current,	I_{OL}	0.4	0, 5	2	4	—	mA
Output High (Source) Current,	I_{OH}	4.6	0, 5	−1	−2	—	
Input Current,	I_{IN}	—	0, 5	—	—	±5	μA
3-State Output Leakage Current, I_{OUT}	L2 Types	0, 5	0, 5	—	—	±5	
	L3 Types	0, 5	0, 5	—	—	±5	
Operating Current,	I_{DD1}#	—	0, 5	—	4	8	mA
Input Capacitance,	C_{IN}	—	—	—	5	7.5	pF
Output Capacitance,	C_{OUT}	—	—	—	10	15	

*Typical values are for T_A = 25°C and nominal V_{DD}.

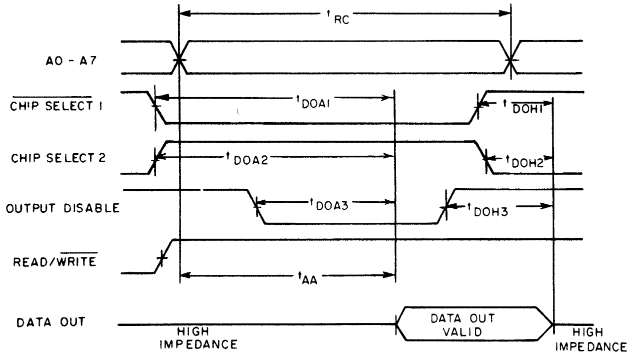
#Outputs open-circuited; cycle time = 1 μs.

MWS5101A

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, t_r,t_f = 20 ns, C_L = 50 pF and 1 TTL Load

CHARACTERISTIC	LIMITS						UNITS
	MWS5101AD, MWS5101AE						
	L2 Types			L3 Types			
	Min.†	Typ.•	Max.	Min†	Typ.•	Max.	
Read Cycle Times (Fig. 1)							
Read Cycle t_{RC}	250	—	—	350	—	—	ns
Access from Address t_{AA}	—	150	250	—	200	350	
Output Valid from $\overline{\text{Chip-Select}}$ 1 t_{DOA1}	—	150	250	—	200	350	
Output Valid from Chip-Select 2 t_{DOA2}	—	150	250	—	200	350	
Output Valid from Output Disable t_{DOA3}	—	—	110	—	—	150	
Output Hold from $\overline{\text{Chip-Select}}$ 1 t_{DOH1}	20	—	—	20	—	—	
Output Hold from Chip-Select 2 t_{DOH2}	20	—	—	20	—	—	
Output Hold from Output Disable t_{DOH3}	20	—	—	20	—	—	

†Time required by a limit device to allow for the indicated function.
•Typical values are for T_A = 25 °C and nominal V_{DD}.



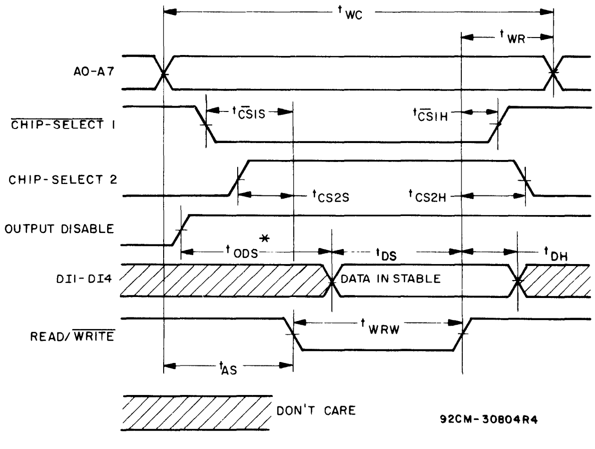
92CM-30244R4

Fig. 1 - Read cycle timing waveforms

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 0$ to 70 °C, $V_{DD} = 5$ V ±5%, $t_r, t_f = 20$ ns, $C_L = 50$ pF and 1 TTL Load

CHARACTERISTIC	LIMITS						UNITS
	MWS5101AD, MWS5101AE						
	L2 Types			L3 Types			
	Min.†	Typ.•	Max.	Min†	Typ.•	Max.	
Write Cycle Times (Fig. 2)							
Write Cycle t_{WC}	300	—	—	400	—	—	ns
Address Setup t_{AS}	110	—	—	150	—	—	
Write Recovery t_{WR}	40	—	—	50	—	—	
Write Width t_{WRW}	150	—	—	200	—	—	
Input Data Setup Time t_{DS}	150	—	—	200	—	—	
Data In Hold t_{DH}	40	—	—	50	—	—	
$\overline{\text{Chip-Select}}$ 1 Setup t_{CS1S}	110	—	—	150	—	—	
Chip-Select 2 Setup t_{CS2S}	110	—	—	150	—	—	
$\overline{\text{Chip-Select}}$ 1 Hold t_{CS1H}	0	—	—	0	—	—	
Chip-Select 2 Hold t_{CS2H}	0	—	—	0	—	—	
Output Disable Setup t_{ODS}	110	—	—	150	—	—	

†Time required by a limit device to allow for the indicated function.
•Typical values are for $T_A = 25$ °C and nominal V_{DD}.



* t_{ODS} IS REQUIRED FOR COMMON I/O OPERATION ONLY, FOR SEPARATE I/O OPERATIONS, OUTPUT DISABLE IS DON'T CARE

Fig 2 - Write cycle timing waveforms

DATA RETENTION CHARACTERISTICS at T_A = 0 to 70° C; See Fig. 3.

CHARACTERISTIC		TEST CONDITIONS		LIMITS			UNITS
				All Types			
		V_{DR} (V)	V_{DD} (V)	Min.	Typ.*	Max.	
Minimum Data Retention Voltage, V_{DR}		—	—	—	1.5	2	V
Data Retention Quiescent Current, I_{DD}	L2 Types	2	—	—	2	10	µA
	L3 Types		—	—	5	50	
Chip Deselect to Data Retention Time, t_{CDR}		—	5	600	—	—	ns
Recovery to Normal Operation Time, t_{RC}		—	5	600	—	—	
V_{DD} to V_{DR} Rise and Fall Time t_r,t_f		2	5	1	—	—	µs

*Typical values are for $T_A = 25$ °C.

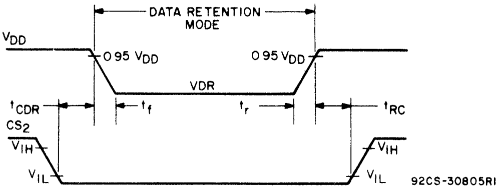


Fig. 3 - Low V_{DD} data retention timing waveforms

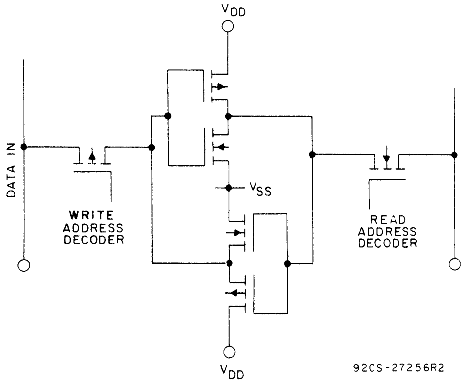


Fig. 4 - Memory cell configuration

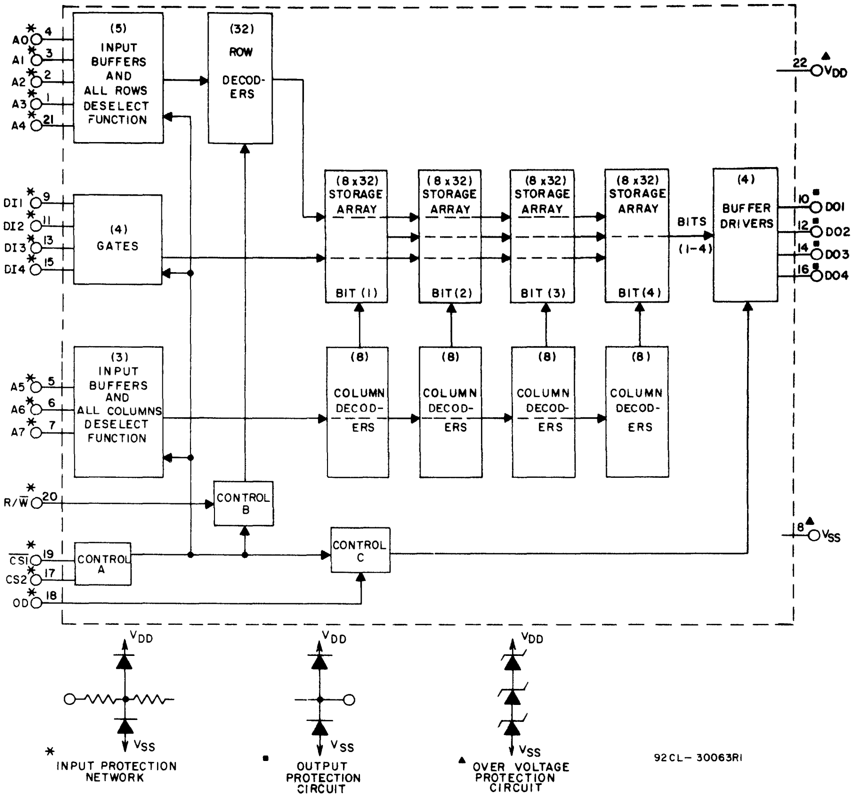


Fig 5 - Functional block diagram for MWS5101A.

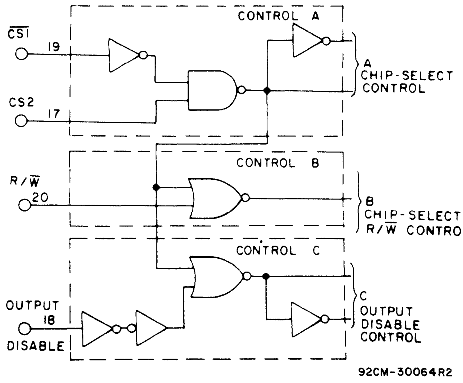
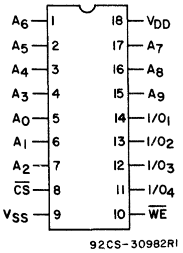


Fig 6 - Logic diagram of controls for MWS5101A.

MWS5114



TERMINAL ASSIGNMENT

CMOS 1024-Word by 4-Bit LSI Static RAM

Features:

- *Fully static operation*
- *Industry standard 1024 x 4 pinout (same as pinouts for 6514, 2114, 9114, and 4045 types)*
- *Common data input and output*
- *Memory retention for stand-by battery voltage as low as 2 V min.*
- *All inputs and outputs directly TTL compatible*
- *3-state outputs*
- *Low standby and operating power*

The RCA-MWS5114 is a 1024-word by 4-bit static random-access memory that uses the RCA ion-implanted silicon gate complementary MOS (CMOS) technology. It is designed for use in memory systems where low power and simplicity in use are desirable. This type has common data input and data output and utilizes a single power supply of 4.5 V to 6.5 V.

The MWS5114 is supplied in 18-lead, hermetic, dual-in-line side-brazed ceramic packages (D suffix) and in 18-lead dual-in-line plastic packages (E suffix).

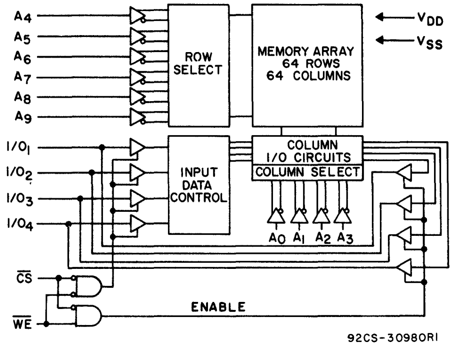


Fig. 1 — Functional block diagram for MWS5114

OPERATIONAL MODES			
FUNCTION	**$\overline{CS}$**	**$\overline{WE}$**	**DATA PINS**
Read	0	1	Output: Dependent on data
Write	0	0	Input
Not Selected	1	X	High-Impedance

File Number **1325**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal .... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/° C to 200mW
For T_A = -55 to +100° C (PACKAGE TYPE D) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D) .... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D .... -55 to +125° C
PACKAGE TYPE E .... -40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg}) .... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C

OPERATING CONDITIONS at T_A = -40° C to +85° C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating-Voltage Range	4.5	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS *at T_A = 0 to +70° C, V_{DD} ±5%, Except as noted*

CHARACTERISTIC	CONDITIONS			LIMITS									UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	MWS 5114-3			MWS 5114-2			MWS 5114-1			
				MIN.	TYP.•	MAX.	MIN.	TYP.•	MAX.	MIN.	TYP.•	MAX.	
Quiescent Device Current I_{DD} Max.	—	0,5	5	—	75	100	—	75	100	—	75	250	µA
Output Voltage Low Level V_{OL} Max.	—	0,5	5	—	0	0.1	—	0	0.1	—	0	0.1	V
High Level V_{OH} Min.	—	0,5	5	4.9	5	—	4.9	5	—	4.9	5	—	
Input Voltage Low Level V_{IL} Max.	0.5,4.5	—	5	—	1.2	0.8	—	1.2	0.8	—	1.2	0.8	
High Level V_{IH} Min.	0.5,4.5	—	5	2.4	—	—	2.4	—	—	2.4	—	—	
Output Current (Sink) I_{OL} Min.	0.4	0,5	5	2	4	—	2	4	—	2	4	—	mA
(Source) I_{OH} Max.	4.6	0,5	5	-0.4	-1	—	-0.4	-1	—	-0.4	-1	—	
Input Current I_{IN} Max.$^{\Delta}$	—	0,5	5	—	±0.1	±5	—	±0.1	±5	—	±0.1	±5	µA
3-State Output Leakage Current I_{OUT}*	0,5	0,5	5	—	±0.5	±5	—	±0.5	±5	—	±0.5	±5	
Operating Device Current I_{DD1}#	—	0,5	5	—	4	8	—	4	8	—	4	8	mA
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	—	10	15	

•Typical values are for T_A = 25° C and nominal V_{DD}.

ΔAll inputs in parallel.

#Outputs open circuited; cycle time = 1 µs.

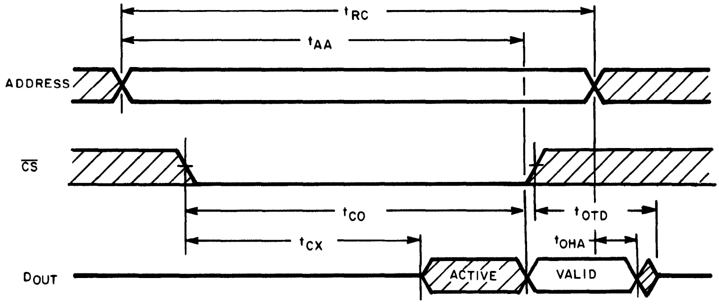
*All outputs in parallel

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 0 to +70° C, V_{DD} = 5 V ±5%, Input t_r, t_f = 10 ns; C_L = 50 pF and 1 TTL Load*

CHARACTERISTIC	LIMITS									UNITS
	MWS 5114-3			MWS 5114-2			MWS 5114-1			
	MIN.†	TYP.*	MAX.	MIN.†	TYP.*	MAX.	MIN.†	TYP.*	MAX.	
Read Cycle Times See Fig. 2										
Read Cycle t_{RC}	200	160	—	250	200	—	300	250	—	ns
Access t_{AA}	—	160	200	—	200	250	—	250	300	
Chip Selection to Output Valid t_{CO}	—	110	150	—	150	200	—	200	250	
Chip Selection to Output Active t_{CX}	20	100	—	20	100	—	20	100	—	
Output 3-state from Deselection t_{OTD}	—	75	125	—	75	125	—	75	125	
Output Hold from Address Change t_{OHA}	50	100	—	50	100	—	50	100	—	

† Time required by a limit device to allow for the indicated function.

•Typical values are for T_A = 25° C and nominal V_{DD}.



NOTE
$\overline{WE}$ IS HIGH DURING THE READ CYCLE.
TIMING MEASUREMENT REF LEVEL IS 1.5 V

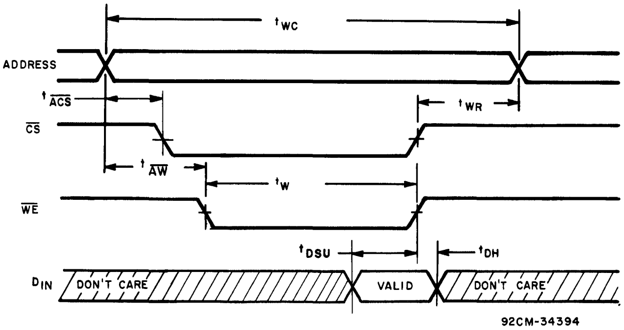
Fig. 2 — Read cycle waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 0 to +70° C, V_{DD} = 5V ±5%, Input t_r,t_f = 10 ns; C_L = 50 pF and 1 TTL Load*

CHARACTERISTIC		LIMITS									UNITS
		MWS 5114-3			MWS 5114-2			MWS 5114-1			
		MIN.†	TYP.•	MAX.	MIN.†	TYP.•	MAX.	MIN.†	TYP.•	MAX.	
Write Cycle Times See Fig. 3											
Write Cycle	t_{WC}	200	160	—	250	200	—	300	220	—	ns
Write	t_W	125	100	—	150	120	—	200	140	—	
Write Release	t_{WR}	50	40	—	50	40	—	50	40	—	
Address To Chip Select Set-Up Time	$t_{\overline{ACS}}$	0	0	—	0	0	—	0	0	—	
Address To Write Set-up Time	$t_{\overline{AW}}$	25	20	—	50	40	—	50	40	—	
Data to Write Set-up Time	t_{DSU}	75	50	—	75	50	—	75	50	—	
Data Hold From Write	t_{DH}	30	10	—	30	10	—	30	10	—	

† Time required by a limit device to allow for the indicated function.

•Typical values are for T_A = 25° C and nominal V_{DD}.



NOTE: $\overline{WE}$ IS LOW DURING THE WRITE CYCLE
TIMING MEASUREMENT REF. LEVEL IS 1.5 V

Fig. 3 — Write cycle waveforms.

MWS5114

DATA RETENTION CHARACTERISTICS *at T_A = 0 to 70° C; See Fig. 4.*

CHARACTERISTIC		TEST CONDITIONS		LIMITS ALL TYPES			UNITS
		V_{DR} (V)	V_{DD} (V)	MIN.	TYP.*	MAX.	
Minimum Data Retention Voltage	V_{DR}	—	—	2	—	—	V
Data Retention Quiescent Current, I_{DD}	MWS 5114-3	2	—	—	25	50	µA
	MWS 5114-2		—	—	25	50	
	MWS 5114-1		—	—	60	125	
Chip Deselect to Data Retention Time,	t_{CDR}	—	5	300	—	—	ns
Recovery to Normal Operation Time,	t_{RC}	—	5	300	—	—	
V_{DD} to V_{DR} Rise and Fall Time	t_r, t_f	2	5	1	—	—	µs

*Typical values are for T_A = 25° C and nominal V_{DD}.

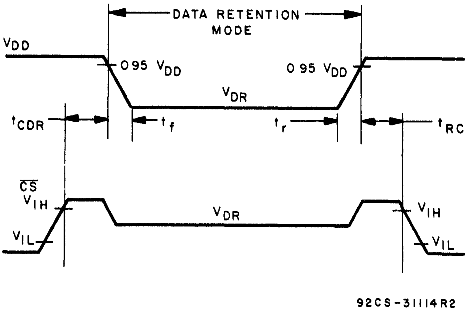


Fig. 4 — Low V_{DD} data retention timing waveforms.

CMOS Read-Only Memories (ROM s)

Technical Data

RCA offers a large selection of CMOS read-only-memories (ROM s) that can be masked-programmed to meet customer application requirements. These ROM s feature the following characteristics:

- CMOS Technology
- Low Power
- High Noise Immunity
- Full Temperature Range

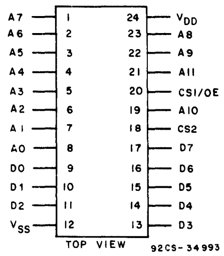
Space efficient memory cells provide small chip size for cost effectiveness, and JEDEC standard pinouts allow interchangeability with industry standard NMOS ROM s and EPROM s.

BYTE-WIDE CMOS AND NMOS ROM's

Manufacturer	**4K x 8**		**8K x 8**		**16K x 8**	**32K x 8**	
	24-Pin†	**24-Pin•**	**24-Pin**	**28-Pin†**	**28-Pin†**	**28-Pin†**	**28-Pin•**
RCA	**CDM5332***	**CDM5333***	**CDM5364***	**CDM5365***	**CDM53128***	**CDM53256***	
AMI	S2333	S68A332	S68A364 S68B364	S2364	S23128		
CSG	2333	2332	2364		23128		
EA	EA8332B	EA8332A	EA8364				
Fairchild	F3533	F3532					
Fujitsu			MB8364				
GI	R03-9333	R03-9332	R03-9364				
GTE		2332					
Hitachi			HN61365* HN61366*	HN61364*	HN613128*	HN613256*	HN61256*
Intel	2332A						
Intersil		IM7332	IM7364				
Maruman		MIC2332	MIC2364				
Micropower			MP2364C*	MP2365*			MP2325*
Motorola		MCM68A332	MCM68B364				
Mostek			MK36000	MK37000			
National		MM52132	MM52164				
NEC			µPD2364A	µPD2364E µPD23C64E*	µPD23128A µPD23C128E*	µPD23256A µPD23C256E*	
OKI					MSM38128		
Panasonic		MN2332					
Rockwell			R2364A	R2364B			
S-MOS			SMM2364*	SMM2365*		SMM6326*	SMM6325*
Signetics		2632A	2664		23128		
SSS		SCM5532* SCM23C32*				SCM23C256*	
Supertex		CM3200*	CM6400A* 23S665	CM6400* 23S664			
Synertek	SY2333	SY2332	SY2364A	SY2365A	SY23128		
TI		TMS4732	TMS4764				
Toshiba			TMM2366 TC5365*	TMM2365 TC5364*	TMM23128	TMM23256 TC53257*	
VLSI				VT2365	VT23128		

* CMOS parts, all others are NMOS
† JEDEC Version B
• JEDEC Version A

CDM5332, CDM5333



CDM5332
TERMINAL ASSIGNMENT

CMOS 4096-Word x 8-Bit Static Read-Only Memory

Features:

- *Low power replacement for NMOS ROMs*
- *Choice of two industry standard pinouts:*
  CDM5332 is pin compatible with INTEL 2732 and 2332A
  CDM5333 is pin compatible with Supertex CM3200, TI TMS 4732, Motorola MCM 68732 and MCM 68A332
- *Fast access time: 350 ns max.*
- *TTL input and output compatible*
- *Three state outputs*
- *Two programmable chip selects*

The RCA CDM5332 and CDM5333 are 32,768-bit mask-programmable CMOS Read-Only Memories organized as 4096 eight-bit words. They are designed to be used with a wide variety of general-purpose microprocessor systems, including RCA CDP1800- and CDP6805-series systems. Two inputs, CS1/OE and CS2, are provided for memory expansion and output buffer control. CS2 gates the address and output buffers and powers down the chip to the standby mode. CS1/OE controls the output buffers to eliminate bus contention. The active polarity for each chip select is user mask-programmable.

The CDM5332 and CDM5333 differ only in terminal assignments and are pin compatible with standard industry types. CDM5332 is pin compatible with Intel 2732 and 2332A. CDM5333 is pin compatible with Supertex CM3200, T.I. TMS4732, and Motorola MCM68732 and MCM68A332.

The CDM5332 and CDM5333 are supplied in 24-lead dual-in-line ceramic packages (D suffix) and 24-lead dual-in-line plastic packages (E suffix).

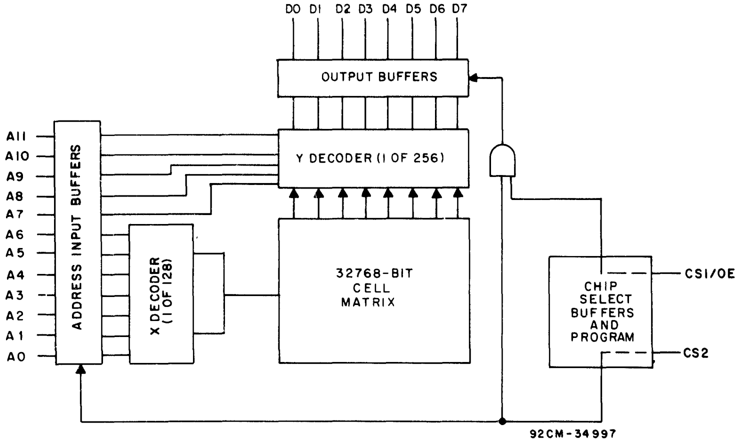
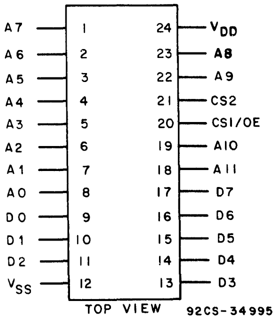


Fig. 1 - Functional block diagram.



CDM5333
TERMINAL ASSIGNMENT

File Number **1366**

CDM5332, CDM5333

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltage referenced to V_{SS} terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to VDD +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 12 mW/° C to 200 mW
For T_A = -55 to +100° C (PACKAGE TYPE D)	500 mW
For T_A = +100 to 125° C (PACKAGE TYPE D)	Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125° C
PACKAGE TYPE E	-40 to +85° C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C

RECOMMENDED OPERATING CONDITIONS at T_A = -40 to +85° C
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	Vss	VDD	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS		LIMITS ALL TYPES			UNITS
		Vo (V)	VIN (V)	Min.	Typ.•	Max.	
Quiescent Device Current	I_{DD}Δ	—	0, V_{DD}	—	2	50	μA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, V_{DD}	2.4	4	—	mA
Output High Drive (Source) Current	I_{OH}	V_{DD} -0.4	0, V_{DD}	-1.2	-2	—	
Output Voltage Low-Level	V_{OL}	—	0, V_{DD}	—	0	0.1	V
Output Voltage High-Level	V_{OH}	—	0, V_{DD}	V_{DD} -0.1	V_{DD}	—	
Input Low Voltage	V_{IL}	0.5, V_{DD} -0.5	—	—	—	0.8	
Input High Voltage	V_{IH}	0.5, V_{DD} -0.5	—	2.4	—	—	
Input Leakage Current	I_{IN}	—	0, V_{DD}	—	—	±1	μA
3-State Output Leakage Current	I_{OUT}	0, V_{DD}	0, V_{DD}	—	—	±1	
Input Capacitance	C_{IN}	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	10	15	
Standby Device Current	I_{SBY}Δ	—	0.8 V,2.4 V	—	0.25	0.5	mA
Operating Device Current	I_{OPER}Δ	—	0.8 V,2.4 V	—	15	25	

ΔSee chart on page 3 for test conditions

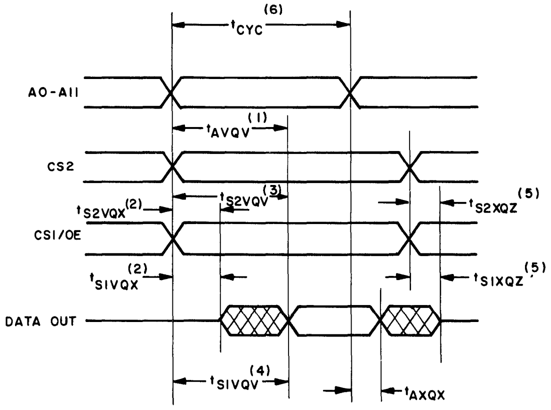
•Typical values are for T_A = 25° C and nominal V_{DD}.

$^{\Delta}$STATIC CHARACTERISTIC Device Current Test Conditions:

CHARACTERISTIC	CHIP SELECT STATUS	ADDRESS INPUT TO TOGGLE FREQUENCY	OUTPUT LOADING
I_{DD} Quiescent Device Current	Any Chip Select Disabled	0	Open Circuit
I_{SBY} — Standby Device Current	CS2 Disabled at TTL Level	1 MHz	Open Circuit
I_{OPER} — Operating Device Current	CS2 Active CS1 Don't Care	1 MHz	Open Circuit

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Input t_r,t_f = 10 ns; C_L = 100 pF, and 1 TTL Load; Input Pulse Levels: 0.8 V to 2.2 V

CHARACTERISTIC		LIMITS		UNITS
		Min.	Max.	
Address Access Time	t_{AVQV}	—	350	ns
CS2 Enable to Output Active	t_{S2VQX}	10	—	
CS1/OE Enable to Output Active	t_{S1VQX}	0	—	
CS2 Enable Access	t_{S2VQV}	—	350	
CS1/OE Enable to Output Valid	t_{S1VQV}	—	150	
Data Hold After Address	t_{AXQX}	50	—	
CS2 Disable to Output High Z	t_{S2XQZ}	—	120	
CS1/OE Disable to Output High Z	t_{S1XQZ}	—	120	
Cycle Time	t_{CYC}	350	—	



NOTES:
1. (1) **Assumes t_{S1VQV} and t_{S2VQV} are satisfied.**
2. (2) **Output Active requires both CS1/OE and CS2 Active.**
3. (3) **Assumes t_{AVQV} and t_{S1VQV} are satisfied.**
4. (4) **Assumes t_{AVQV} and t_{S2VQV} are satisfied.**
5. (5) **Either invalid CS1/OE or CS2 causes Output High Z.**
6. (6) **Generates 50-ns Valid Output Pulses (i.e., t_{CYC}-t_{AVQV}+t_{AXQX}).**

NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

92CM- 36678

Fig. 2 - Timing waveforms.

CDM5332, CDM5333

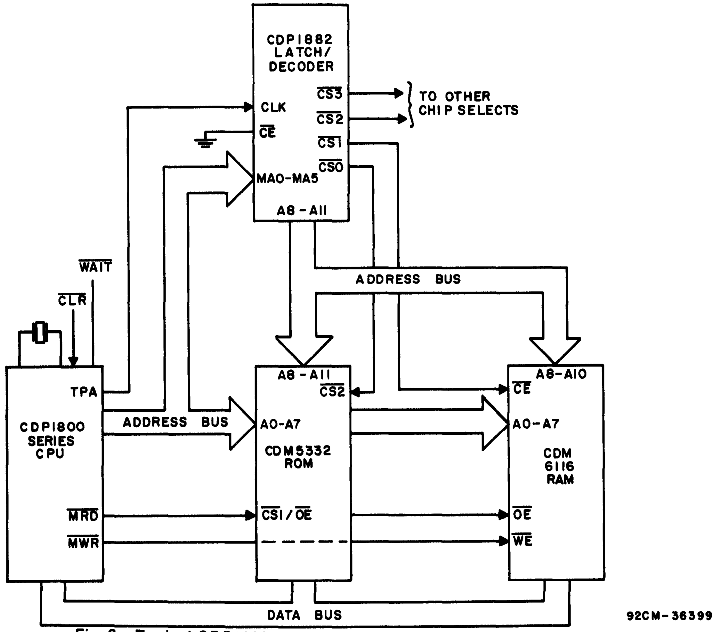
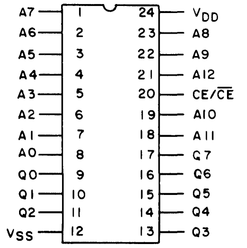


Fig. 3 - Typical CDP1800 series microprocessor system.

CDM5364, CDM5364A



CDM5364
TERMINAL ASSIGNMENT

CMOS 8192-Word by 8-Bit LSI Static ROMS

Features:
- *Asynchronous operation*
- *Fast access time - 250 ns max.*
- *Low standby and operating power:*
  I_{SBY2} = 2 μA typical (CDM5364)
  I_{DDS} = 2 μA typical (CDM5364A)
  I_{OPER2} = 10 mA max. at t_{cyc} = 1 μs
  = 30 mA max. at t_{cyc} = 250 ns
- *Automatic power down*
- *TTL input and output compatible*
- *24-pin JEDEC standard pin out:*
  Pin compatible with Motorola MCM68764 and MCM68766 EPROMs
- *Choice of pin 20 function:*
  Mask-programmable CE (CDM5364)
  Mask-programmable CS (CDM5364A)

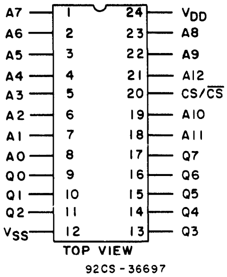
The RCA CDM5364 and CDM5364A are 65,536-bit mask-programmable CMOS Read Only Memories organized as 8192 eight-bit words. They are characterized by fast access time and low-power dissipation, and are designed to be used with a wide variety of general purpose microprocessor systems, including RCA-CDP1800-and CDP6805-series systems. The CDM5364 and CDM5364A differ in the function for pin 20.

The CDM5364 provides a chip enable input at pin 20, which gates the address buffers and output drivers, providing a low power standby mode.

The CDM5364A has a chip select input at pin 20. As a chip select input, pin 20 controls only the output drivers providing fast output enable time. The polarities of the chip enable and the chip select inputs are user mask-programmable.

Both the CDM5364 and CDM5364A provide automatic power-down and data hold while the address inputs are stable.

The CDM5364 and CDM5364A are supplied in 24-lead hermetic, dual-in-line side-brazed ceramic packages (D suffix), and in 24-lead dual-in-line plastic packages (E suffix).



CDM5364A
TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltage referenced to V_{SS} terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to 125°C (PACKAGE TYPE D)	Derate Linearly at 8 mW/°C to 300 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C

CDM5364, CDM5364A

RECOMMENDED OPERATING CONDITIONS at T_A = -40 to +85°C
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS CDM5364, CDM5364A		UNITS
	Min.	Max.	
DC Operating Voltage Range	4	6	V
Input Voltage Range	V_{SS}	V_{DD}	

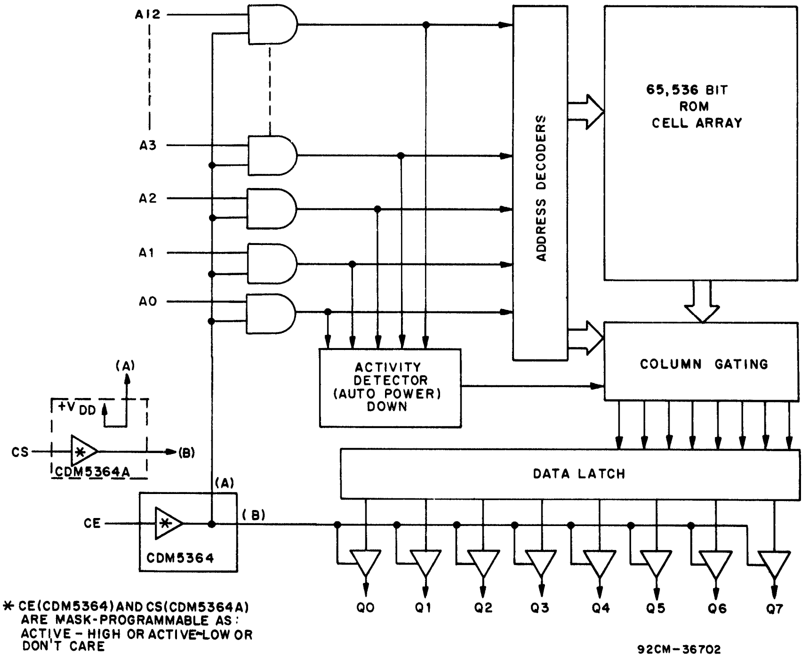


Fig. 1 - Functional block diagram.

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS	LIMITS CDM5364 Min.	Typ.•	Max.	UNITS
Average Operating Device Current[a]	I_{OPER1}[d]	V_{IN} = V_{IL}, V_{IH}, CE = V_{IH}, ($\overline{CE}$ = V_{IL}) t_{cyc} = 1 µs	—	—	15	mA
		t_{cyc} = 250 ns	—	—	35	
	I_{OPER2}[e]	V_{IN} = 0.2 V, V_{DD} -0.2 V, CE = V_{DD} -0.2 V, ($\overline{CE}$ = 0.2 V) t_{cyc} = 1 µs	—	—	10	
		t_{cyc} = 250 ns	—	—	30	
DC Active Device Current[b]	I_{ACT1}[d]	V_{IN} = V_{IL}, V_{IH}, CE = V_{IH}, ($\overline{CE}$ = V_{IL})	—	—	15	mA
	I_{ACT2}[e]	V_{IN} = 0.2 V, V_{DD} -0.2 V, CE = V_{DD} -0.2 V, ($\overline{CE}$ = 0.2 V)	—	—	50	µA
Standby Device Current[c]	I_{SBY1}[d]	V_{IN} = V_{IL}, V_{IH}, CE = V_{IL}, ($\overline{CE}$ = V_{IH})	—	—	1.5	mA
	I_{SBY2}[e]	V_{IN} = 0.2 V, V_{DD} -0.2V, CE = 0.2 V, ($\overline{CE}$ = V_{DD} -0.2 V)	—	2	50	µA
Output Voltage Low-Level	V_{OL}	I_{OL} = 3.2 mA	—	—	0.4	V
Output Voltage High-Level	V_{OH}	I_{OH} = -3.2 mA	2.4	—	—	
Input Low Voltage	V_{IL}	—	—	—	0.8	
Input High Voltage	V_{IH}	—	2.2	—	—	
Input Leakage Current (Any Input)	I_{IN}	$V_{SS} \leq V_{IN} \leq V_{DD}$	—	—	±1	µA
3-State Output Leakage Current	I_{OUT}	$V_{SS} \leq V_{OUT} \leq V_{DD}$	—	—	±1	
Input Capacitance	C_{IN}	f = 1 MHz, T_A = 25°C	—	5	10	pF
Output Capacitance	C_{OUT}	f = 1 MHz, T_A = 25°C	—	6	12	

•Typical values are for T_A = 25° C and nominal V_{DD}

[a] Address inputs toggling, chip enabled outputs open circuit.

[b] Inputs stable, chip enabled, outputs open circuit

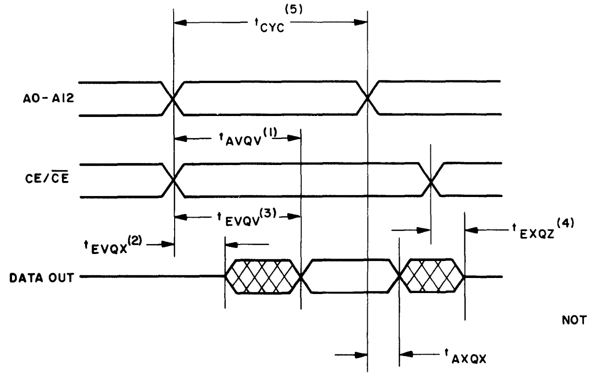
[c] Independent of address input activity, chip disabled

[d] TTL inputs

[e] CMOS inputs

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 10%,
Input t_r, t_f = 10 ns; C_L = 100 pF, and 1 TTL Load; Input Pulse Levels: 0.8 V to 2.2 V — See Fig. 2

CHARACTERISTIC		LIMITS CDM5364 Min.	Max.	UNITS
Address Access Time	t_{AVQV}	—	250	ns
Chip Enable to Output Active	t_{EVQX}	0	—	
Chip Enable Access	t_{EVQV}	—	250	
Data Hold after Address	t_{AXQX}	10	—	
Chip Disable to Output High Z	t_{EXQZ}	—	90	
Cycle Time	t_{CYC}	250	—	



NOTES:

(1) Assumes t_{EVQV} is satisfied.
(2) Output Active requires Chip Enable Active.
(3) Assumes t_{AVQV} is satisfied.
(4) Invalid Chip Enable causes Output High Z.
(5) Generates 10-ns Valid Output Pulses (i.e., t_{CYC}-t_{AVQV}+t_{AXQX}).

NOTE TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V

92CM-36699

Fig. 2 - Timing waveforms

CDM5364, CDM5364A

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS	LIMITS CDM5364A			UNITS
			Min.	Typ.•	Max.	
Average Operating Device Current[a]		$V_{IN} = V_{IL}, V_{IH}$; $CS = V_{IH}$; ($\overline{CS} = V_{IL}$) t_{cyc} = 1 µs	—	—	15	mA
	I_{OPER1}[d]	t_{cyc} = 250 ns	—	—	35	
	I_{OPER2}[e]	V_{IN} = 0.2 V, V_{DD} -0.2 V; CS = V_{DD} -0.2 V; ($\overline{CS}$ = 0.2 V) t_{cyc} = 1 µs	—	—	10	
		t_{cyc} = 250 ns	—	—	30	
DC Active Device Current[b]	I_{ACT1}[d]	$V_{IN} = V_{IL}, V_{IH}$; $CS = V_{IH}$; ($\overline{CS} = V_{IL}$)	—	—	15	mA
	I_{ACT2}[e]	V_{IN} = 0.2 V, V_{DD} -0.2 V; CS = V_{DD} -0.2 V; ($\overline{CS}$ = 0.2 V)	—	—	50	µA
Quiescent Device Current[c]	I_{DDS}[e]	V_{IN} = 0.2 V, V_{DD} -0.2V; CS = 0.2 V; ($\overline{CS}$ = V_{DD} -0 2 V)	—	2	50	µA
Output Voltage Low-Level	V_{OL}	I_{OL} = 3.2 mA	—	—	0.4	V
Output Voltage High-Level	V_{OH}	I_{OH} = -3 2 mA	2.4	—	—	
Input Low Voltage	V_{IL}	—	—	—	0.8	
Input High Voltage	V_{IH}	—	2.2	—	—	
Input Leakage Current (Any Input)	I_{IN}	$V_{SS} \leq V_{IN} \leq V_{DD}$	—	—	±1	µA
3-State Output Leakage Current	I_{OUT}	$V_{SS} \leq V_{OUT} \leq V_{DD}$	—	—	±1	
Input Capacitance	C_{IN}	f = 1 MHz, T_A = 25°C	—	5	10	pF
Output Capacitance	C_{OUT}	f = 1 MHz, T_A = 25°C	—	6	12	

•Typical values are for T_A = 25° C and nominal V_{DD}.

[a] Address inputs toggling, chip selected outputs open circuit.

[b] Inputs stable, chip selected outputs open circuit

[c] Inputs stable, chip deselected.

[d] TTL inputs.

[e] CMOS inputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns; C_L = 100 pF, and 1 TTL Load; Input Pulse Levels: 0.8 V to 2.2 V — See Fig. 3

CHARACTERISTIC		LIMITS CDM5364A		UNITS
		Min.	Max.	
Address Access Time	t_{AVQV}	—	250	ns
Chip Select to Output Active	t_{SVQX}	0	—	
Chip Select to Output Valid	t_{SVQV}	—	90	
Data Hold after Address	t_{AXQX}	10	—	
Chip Deselect to Output High Z	t_{SXQZ}	—	70	
Cycle Time	t_{CYC}	250	—	

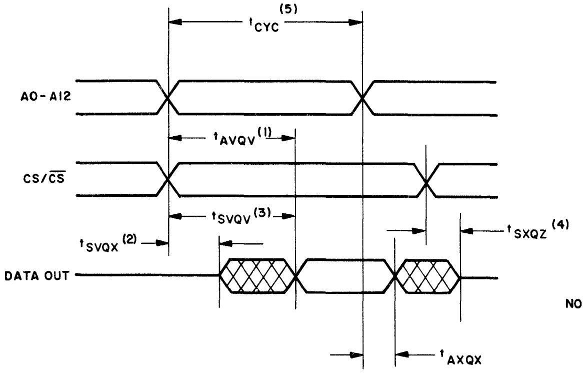


Fig 3 - Timing waveforms

NOTES:
1. (1) **Assumes t_{SVQV} is satisfied.**
2. (2) **Output Active requires Chip Select Active.**
3. (3) **Assumes t_{AVQV} is satisfied.**
4. (4) **Invalid Chip Select causes Output High Z.**
5. (5) **Generates 10-ns Valid Output Pulses (i.e., t_{CYC}-t_{AVQV}+t_{AXQX}).**

NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V

92CM-36700

APPLICATION INFORMATION

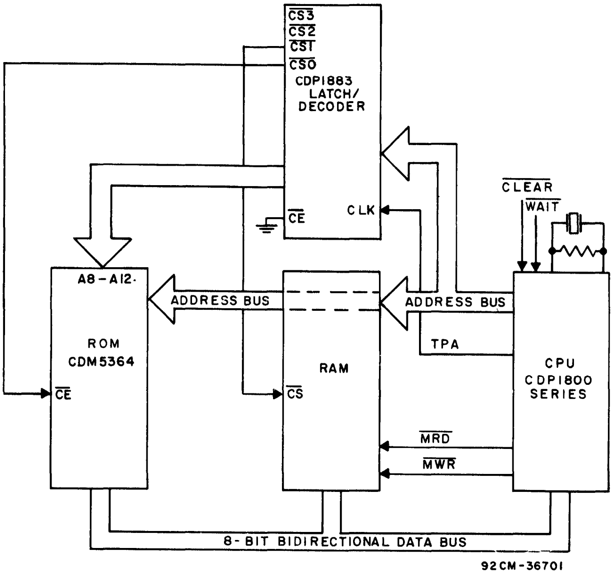
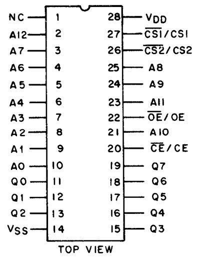


Fig. 4 - Typical CDP1800 series microprocessor system.

Decoupling Capacitors

The CDM5364 and CDM5364A operate with a low average dc power supply current that varies with cycle time. However, the CDM5364 and CDM5364A are large ROMs with many internal nodes. Precharging of selected nodes during portions of the memory cycle results in short duration peak currents that can be much higher than the average dc value. The rise and fall times of the peak current pulses can have a value sufficient to generate unwanted system noise components. To minimize or eliminate the effects of the current spikes, a 0.1 μF ceramic decoupling capacitor is recommended between the VDD and VSS pins of every ROM device.

CDM5365



TERMINAL ASSIGNMENT

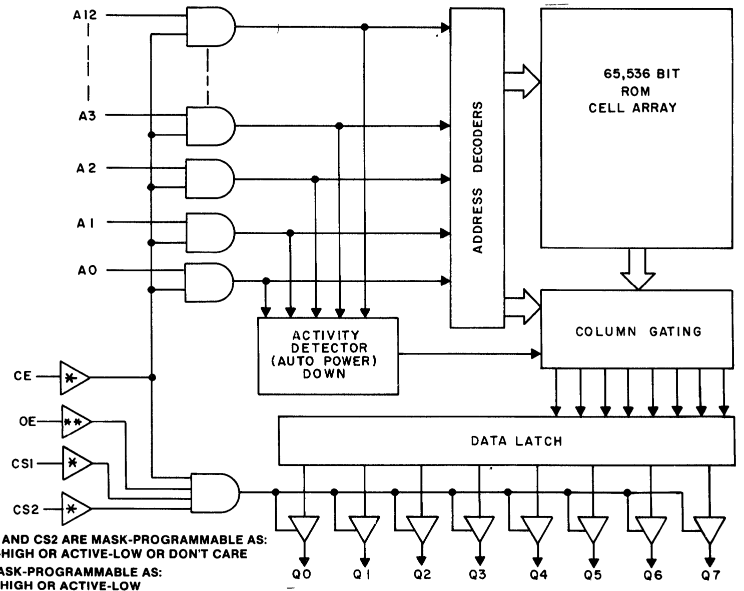
CMOS 8192-Word by 8-Bit LSI Static ROM

Features:

- *Asynchronous operation*
- *Fast access time - 250 ns max.*
- *Low standby and operating power -*
  - *$I_{SBY2}=2\ \mu A$ typical*
  - *$I_{OPER2}=10$ mA max. at $t_{cyc}=1\ \mu s$;*
  - *$=30$ mA max. at $t_{cyc}=250$ ns*
- *Automatic power-down*
- *Mask-programmable chip enable, chip selects, and output enable*
- *TTL input and output compatible*
- *28-pin JEDEC standard pin out: Pin compatible with the 2764 EPROM*

The RCA-CDM5365 is a 65,536-bit asynchronous mask-programmable CMOS READ-ONLY memory organized as 8192 eight-bit words. The CDM5365 is designed to be used with a wide range of general-purpose microprocessor systems, including the RCA CDP1800- and CDP6805-series systems. Two chip selects, one chip enable, and an output enable function are provided for memory expansion and output buffer control. The chip enable gates the address and output buffers and powers down the chip to the standby mode. The two chip selects and the output enable control only the output buffers. The polarities of the chip enable, chip selects, and the output enable are user mask-programmable.

The CDM5365 is supplied in 28-lead, hermetic, dual-in-line side-brazed ceramic (D suffix), and 28-lead dual-in-line plastic (E suffix) packages.



*** CE, CS1 AND CS2 ARE MASK-PROGRAMMABLE AS: ACTIVE-HIGH OR ACTIVE-LOW OR DON'T CARE**

*** * OE IS MASK-PROGRAMMABLE AS: ACTIVE-HIGH OR ACTIVE-LOW**

Fig. 1 - Functional block diagram.

File Number **1466**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltage referenced to V_{SS} terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE D)	500 mW
For T_A = +100 to 125° C (PACKAGE TYPE D)	Derate Linearly at 8 mW/° C to 300 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125° C
PACKAGE TYPE E	-40 to +85° C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265° C

RECOMMENDED OPERATING CONDITIONS at T_A = -40 to +85° C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating Voltage Range	4	6	V
Input Voltage Range	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS	LIMITS			UNITS
			Min.	Typ.[•]	Max.	
Average Operating Device Current[a]		$V_{IN} = V_{IL}, V_{IH}$; CE = V_{IH}; ($\overline{CE} = V_{IL}$) t_{cyc} = 1 µs	—	—	15	mA
	I_{OPER1}[d]	t_{cyc} = 250 ns	—	—	35	
	I_{OPER2}[e]	V_{IN} = 0.2 V, V_{DD} -0.2 V; CE = V_{DD} -0.2 V; ($\overline{CE}$=0.2 V) t_{cyc}=1 µs	—	—	10	
		t_{cyc} = 250 ns	—	—	30	
DC Active Device Current[b]	I_{ACT1}[d]	$V_{IN}=V_{IL}, V_{IH}$; CE=V_{IH}; ($\overline{CE}=V_{IL}$)	—	—	15	mA
	I_{ACT2}[e]	V_{IN}=0.2 V, V_{DD} -0.2 V; CE=V_{DD} -0.2 V; ($\overline{CE}$=0.2 V)	—	—	50	µA
Standby Device Current[c]	I_{SBY1}[d]	$V_{IN}=V_{IL}, V_{IH}$; CE=V_{IL}; ($\overline{CE}=V_{IH}$)	—	—	1.5	mA
	I_{SBY2}[e]	V_{IN}=0.2 V, V_{DD} -0.2 V; CE=0.2 V; ($\overline{CE}=V_{DD}$ -0.2 V)	—	2	50	µA
Output Voltage Low-Level	V_{OL}	I_{OL} = 3.2 mA	—	—	0.4	V
Output Voltage High-Level	V_{OH}	I_{OH} = -3.2 mA	2.4	—	—	
Input Low Voltage	V_{IL}	—	—	—	0.8	
Input High Voltage	V_{IH}	—	2.2	—	—	
Input Leakage Current (Any Input)	I_{IN}	$V_{SS} \leq V_{IN} \leq V_{DD}$	—	—	±1	µA
3-State Output Leakage Current	I_{OUT}	$V_{SS} \leq V_{OUT} \leq V_{DD}$	—	—	±1	
Input Capacitance	C_{IN}	f = 1 MHz, T_A = 25° C	—	5	10	pF
Output Capacitance	C_{OUT}	f = 1 MHz, T_A = 25° C	—	6	12	

[•] Typical values are for T_A=25° C and nominal V_{DD}.

[a] Address inputs toggling, chip enabled, outputs open circuit.

[b] Inputs stable, chip enabled, outputs open circuit.

[c] Independent of address input activity, chip disabled.

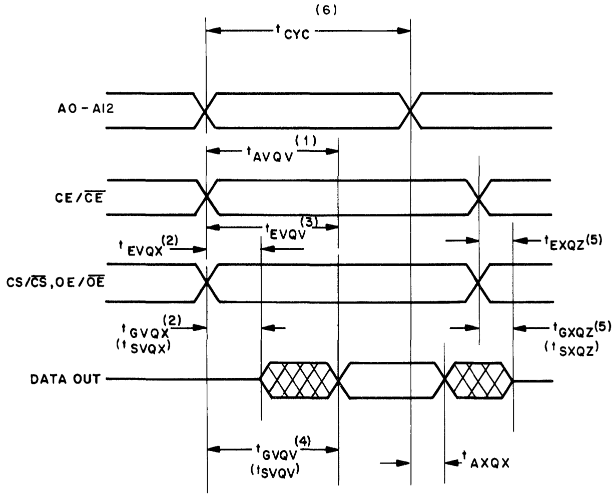
[d] TTL inputs.

[e] CMOS inputs.

CDM5365

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} =5 V ± 10%, Input t_r, t_f = 10 ns; C_L = 100 pF, and 1 TTL Load; Input Pulse Levels: 0.8 V to 2.2 V

CHARACTERISTIC		LIMITS		UNITS
		Min.	Max.	
Address Access Time	t_{AVQV}	—	250	ns
Chip Enable to Output Active	t_{EVQX}	0	—	
Output Enable to Output Active	t_{GVQX}	0	—	
Chip Select to Output Active	t_{SVQX}	0	—	
Chip Enable Access	t_{EVQV}	—	250	
Output Enable to Output Valid	t_{GVQV}	—	90	
Chip Select to Output Valid	t_{SVQV}	—	90	
Data Hold After Address	t_{AXQX}	10	—	
Chip Disable to Output High Z	t_{EXQZ}	—	90	
Output Disable to Output High Z	t_{GXQZ}	—	70	
Chip Deselect to Output High Z	t_{SXQZ}	—	70	
Cycle Time	t_{CYC}	250	—	



NOTES:
(1) Assumes t_{SVQV}, t_{GVQV}, and t_{EVQV} are satisfied
(2) Output Active requires Chip Enable, Output Enable and Chip Selects Active.
(3) Assumes t_{AVQV}, t_{SVQV}, and t_{GVQV} are satisfied.
(4) Assumes t_{AVQV} and t_{EVQV} are satisfied.
(5) Either Invalid Chip Enable, Chip Select, or Output Enable causes Output High Z.
(6) Generates 10-ns Valid Output Pulses (i.e., $t_{CYC}-t_{AVQV}+t_{AXQX}$).

92CM-36632

NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

Fig. 2 - Timing waveforms.

APPLICATION INFORMATION

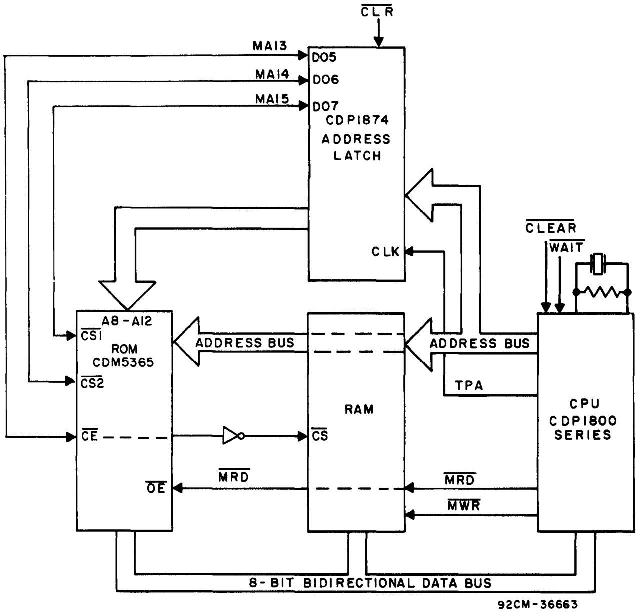
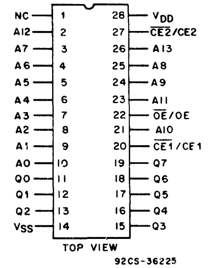


Fig. 3 - Typical CDP1800 series microprocessor system.

Decoupling Capacitors

The CDM5365 operates with a low average dc power supply current that varies with cycle time. However, the CDM5365 is a large ROM with many internal nodes. Pre-charging of selected nodes during portions of the memory cycle results in short duration peak currents that can be much higher than the average dc value. The rise and fall times of the peak current pulses can have a value sufficient to generate unwanted system noise components. To minimize or eliminate the effects of the current spikes, a 0.1-μF ceramic decoupling capacitor is recommended between the V_{DD} and V_{SS} pins of every ROM device.

CDM53128



TERMINAL ASSIGNMENT

CMOS 16,384-Word by 8-Bit LSI Static ROM

Features:

- *Asynchronous operation*
- *Fast access time - 250 ns max.*
- *Low standby and operating power -*
  - *I_{SBY2}=2 μA typical*
  - *I_{OPER2}=10 mA max. at t_{CYC}=1 μs;*
  - *=30 mA max. at t_{CYC}=250 ns*
- *Automatic power-down*
- *Mask-programmable chip enables and output enable*
- *TTL input and output compatible*
- *28-pin JEDEC standard pin out*

The RCA-CDM53128 is a 131,072-bit asynchronous mask-programmable CMOS READ-ONLY memory organized as 16,384 eight-bit words. The CDM53128 is designed to be used with a wide range of general-purpose microprocessor systems, including the RCA CDP1800 series system. Two chip-enable inputs and an output enable function are provided for memory expansion and output buffer control. Either chip enable (CE1 or CE2) can gate the address and output buffers and power down the chip to the standby mode. The output enable (OE) controls the output buffers to eliminate bus contention. The polarity of each chip enable and the output enable are user mask-programmable.

The CDM53128 is supplied in 28-lead, hermetic, dual-in-line side-brazed ceramic (D suffix), and in 28-lead dual-in-line plastic (E suffix) packages.

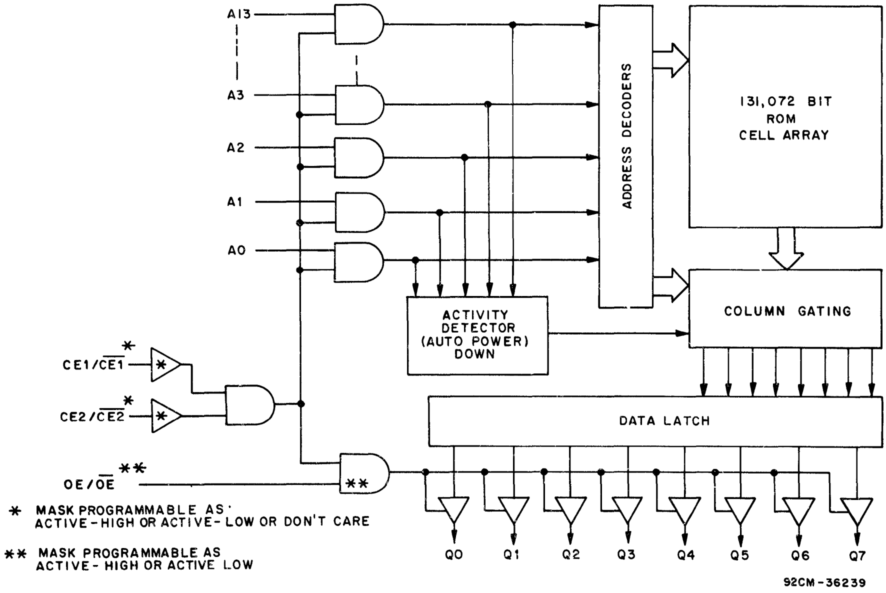

A13
A3
A2
A1
A0
ADDRESS DECODERS
131,072 BIT ROM CELL ARRAY
COLUMN GATING
ACTIVITY DETECTOR (AUTO POWER) DOWN
DATA LATCH
CE1/CE1 *
CE2/CE2 *
OE/OE **
* MASK PROGRAMMABLE AS ACTIVE-HIGH OR ACTIVE-LOW OR DON'T CARE
** MASK PROGRAMMABLE AS ACTIVE-HIGH OR ACTIVE LOW
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
92CM-36239

Fig. 1 - Functional block diagram.

File Number **1454**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltage referenced to V_{SS} terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 8 mW/°C to 300 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS	LIMITS ALL TYPES			UNITS
			Min.	Typ.•	Max.	
Average Operating Device Current[a]	I_{OPER1}[d]	V_{IN} = V_{IL}, V_{IH}; CE1 and CE2= V_{IH}; ($\overline{CE1}$ and $\overline{CE2}$ = V_{IL}) t_{cyc} = 1 µs	—	—	15	mA
		t_{cyc} = 250 ns	—	—	35	
	I_{OPER2}[e]	V_{IN} = 0.2 V, V_{DD} -0.2 V; CE1 & CE2 = V_{DD} -0.2 V; ($\overline{CE1}$ & $\overline{CE2}$=0.2 V) t_{cyc}=1 µs	—	5	10	
		t_{cyc} = 250 ns	—	15	30	
DC Active Device Current[b]	I_{ACT1}[d]	V_{IN} = V_{IL}, V_{IH}; CE1 and CE2= V_{IH}; ($\overline{CE1}$ and $\overline{CE2}$ = V_{IL})	—	—	15	mA
	I_{ACT2}[e]	V_{IN} = 0.2 V, V_{DD} -0.2 V; CE1 & CE2=V_{DD} -0.2 V; ($\overline{CE1}$ & $\overline{CE2}$ = 0.2 V)	—	—	50	µA
Standby Device Current[c]	I_{SBY1}[d]	V_{IN} = V_{IL}, V_{IH}; CE1 or CE2= V_{IL}; ($\overline{CE1}$ or $\overline{CE2}$=V_{IH})	—	—	3	mA
	I_{SBY2}[e]	V_{IN} = 0.2 V, V_{DD} -0.2 V; CE1 or CE2 = 0.2 V; ($\overline{CE1}$ or $\overline{CE2}$ = V_{DD} -0.2 V)	—	2	50	µA
Output Voltage Low-Level	V_{OL}	I_{OL} = 3.2 mA	—	—	0.4	V
Output Voltage High-Level	V_{OH}	I_{OH} = -3.2 mA	2.4	—	—	
Input Low Voltage	V_{IL}	—	—	—	0.8	
Input High Voltage	V_{IH}	—	2.2	—	—	
Input Leakage Current (Any Input)	I_{IN}	$V_{SS} \leq V_{IN} \leq V_{DD}$	—	—	±1	µA
3-State Output Leakage Current	I_{OUT}	$V_{SS} \leq V_{OUT} \leq V_{DD}$	—	—	±1	
Input Capacitance	C_{IN}	f = 1 MHz, T_A = 25°C	—	5	10	pF
Output Capacitance	C_{OUT}	f = 1 MHz, T_A = 25°C	—	6	12	

•Typical values are for T_A=25°C and nominal V_{DD}.

[a] Address inputs toggling, chip enabled, outputs open circuit.

[b] Inputs stable, chip enabled, outputs open circuit.

[c] Independent of address input activity, chip disabled.

[d] TTL inputs.

[e] CMOS inputs.

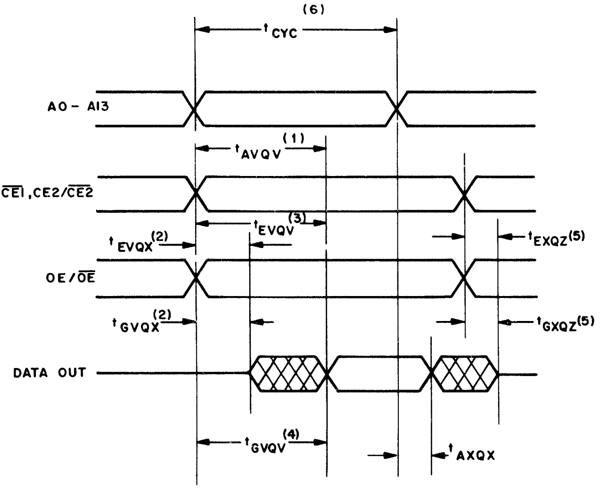
CDM53128

RECOMMENDED OPERATING CONDITIONS at T_A = -40 to +85°C
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating Voltage Range	4	6	V
Input Voltage Range	V_{SS}	V_{DD}	

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns; C_L = 100 pF, and 1 TTL Load; Input Pulse Levels: 0.8 V to 2.2 V

CHARACTERISTIC		LIMITS		UNITS
		Min.	Max.	
Address Access Time	t_{AVQV}	—	250	ns
Chip Enable to Output Active	t_{EVQX}	0	—	
Output Enable to Output Active	t_{GVQX}	0	—	
Chip Enable Access	t_{EVQV}	—	250	
Output Enable to Output Valid	t_{GVQV}	—	90	
Data Hold After Address	t_{AXQX}	10	—	
Chip Disable to Output High Z	t_{EXQZ}	—	90	
Output Disable to Output High Z	t_{GXQZ}	—	70	
Cycle Time	t_{CYC}	250	—	



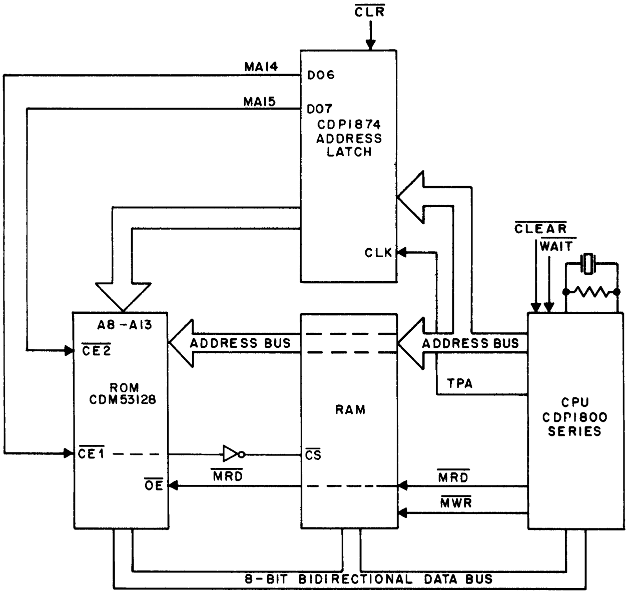
NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

NOTES·
(1) Assumes t_{GVQV} & t_{EVQV} are satisified.
(2) Output Active requires both Chip Enables & Output Enable Active.
(3) Assumes t_{AVQV} & t_{GVQV} are satisfied.
(4) Assumes t_{AVQV} & t_{EVQV} are satisfied.
(5) Either Invalid Chip Enable or Output Enable causes Output High Z.
(6) Generates 10 ns Valid Output Pulses (i.e., $t_{CYC}-t_{AVQV}+t_{AXQX}$)

92CM-36407R1

Fig. 2 - Timing waveforms.

APPLICATION INFORMATION



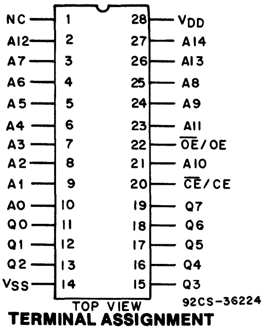
92CM- 36217

Fig. 3 - Typical CDP1800 series microprocessor system.

Decoupling Capacitors

The CDM53128 operates with a low average dc power supply current that varies with cycle time. However, the CDM53128 is a large ROM with many internal nodes. Precharging of selected nodes during portions of the memory cycle results in short duration peak currents that can be much higher than the average dc value. The rise and fall times of the peak current pulses can have a value sufficient to generate unwanted system noise components. To minimize or eliminate the effects of the current spikes, a 0.1-μF ceramic decoupling capacitor is recommended between the V_{DD} and V_{SS} pins of every ROM device.

CDM53256



TERMINAL ASSIGNMENT

CMOS 32,768-Word by 8-Bit LSI Static ROM

Features:

- *Asynchronous operation*
- *Fast access time - 250 ns max.*
- *Low standby and operating power -*
  - I_{SBY2} = *2 μA typical*
  - I_{OPER2} = *12 mA max. at* t_{cyc} = *1 μs*
  - = *36 mA max. at* t_{cyc} = *250 ns*
- *Automatic power down*
- *Mask-programmable chip enable and output enable*
- *TTL input and output compatible*
- *28-pin JEDEC standard pin out: Pin compatible with the 27256 EPROM*

The RCA-CDM53256 is a 262,144-bit asynchronous mask-programmble, CMOS READ-ONLY memory organized as 32,768 eight-bit words. The CDM53256 is designed to be used with a wide range of general-purpose microprocessor systems, including the RCA CDP1800 series system. One chip enable input and an output enable function are provided for memory expansion and output buffer control. Chip enable (CE) gates the address and output buffers and powers down the chip to the standby mode. The output enable (OE) controls the output buffers to eliminate bus contention. The polarities of the chip enable and the output enable are user mask-programmble.

The CDM53256 is supplied in 28-lead, hermetic, dual-in-line side-brazed ceramic (D suffix), in 28-lead dual-in-line plastic (E suffix) and in 28-lead small-outline (SO) plastic (M suffix) packages.

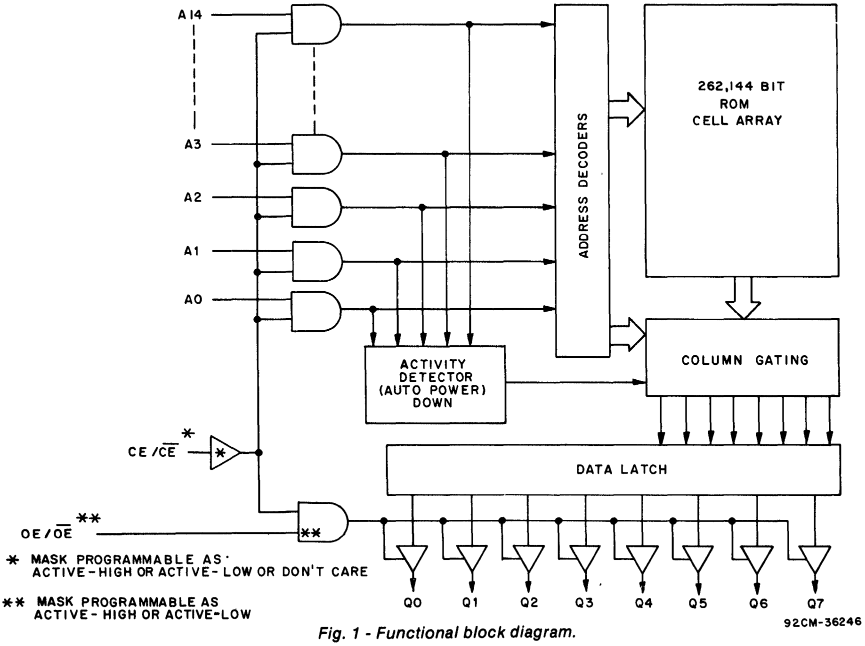

A14
A3
A2
A1
A0
ADDRESS DECODERS
262,144 BIT ROM CELL ARRAY
COLUMN GATING
ACTIVITY DETECTOR (AUTO POWER) DOWN
DATA LATCH
CE/$\overline{CE}$ *
OE/$\overline{OE}$ **
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
* MASK PROGRAMMABLE AS ACTIVE-HIGH OR ACTIVE-LOW OR DON'T CARE
** MASK PROGRAMMABLE AS ACTIVE-HIGH OR ACTIVE-LOW
92CM-36246

Fig. 1 - Functional block diagram.

File Number **1453**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltage referenced to V_{SS} terminal)	-0.5 to +7V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +85°C (PACKAGE TYPE M)*	425 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E and M	-40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C

*Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

RECOMMENDED OPERATING CONDITIONS at T_A = -40 to +85°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating Voltage Range	4	6	V
Input Voltage Range	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS	LIMITS ALL TYPES			UNITS
			Min.	Typ.•	Max.	
Average Operating Device Current[a]	I_{OPER1}[d]	V_{IN} = V_{IL}, V_{IH}, CE = V_{IH}, ($\overline{CE}$ = V_{IL}) t_{cyc} = 1 μs	—	—	16	mA
		t_{cyc} = 250 ns	—	—	40	
	I_{OPER2}[e]	V_{IN} = 0 2 V, V_{DD} -0.2 V; CE = V_{DD} -0 2 V; ($\overline{CE}$ = 0.2 V) t_{cyc} = 1 μs	—	—	12	
		t_{cyc} = 250 ns	—	—	36	
DC Active Device Current[b]	I_{ACT1}[d]	V_{IN} = V_{IL}, V_{IH}; CE = V_{IH}, ($\overline{CE}$ = VIL)	—	—	15	mA
	I_{ACT2}[e]	V_{IN} = 0 2 V, V_{DD} -0.2 V; CE = V_{DD} -0 2 V, ($\overline{CE}$ = 0 2 V)	—	—	50	μA
Standby Device Current[c]	I_{SBY1}[d]	V_{IN} = V_{IL}, V_{IH}, CE = V_{IL}, ($\overline{CE}$ = V_{IH})	—	—	1.5	mA
	I_{SBY2}[e]	V_{IN} = 0 2 V, V_{DD} -0 2 V; CE = 0.2 V, ($\overline{CE}$ = V_{DD} -0.2 V)	—	2	50	μA
Output Voltage Low-Level	V_{OL}	I_{OL} = 3.2 mA	—	—	0.4	V
Output Voltage High-Level	V_{OH}	I_{OH} = -3.2 mA	2.4	—	—	
Input Low Voltage	V_{IL}	—	—	—	0.8	
Input High Voltage	V_{IH}	—	2.2	—	—	
Input Leakage Current (Any Input)	I_{IN}	$V_{SS} \leq V_{IN} \leq V_{DD}$	—	—	±1	μA
3-State Output Leakage Current	I_{OUT}	$V_{SS} \leq V_{OUT} \leq V_{DD}$	—	—	±1	
Input Capacitance	C_{IN}	f = 1 MHz, T_A = 25°C	—	5	10	pF
Output Capacitance	C_{OUT}	f = 1 MHz, T_A = 25°C	—	6	12	

•Typical values are for T_A = 25°C and nominal V_{DD}.

[a] Address inputs toggling, chip enabled, outputs open circuit.

[b] Inputs stable, chip enabled, outputs open circuit.

[c] Independent of address input activity, chip disabled.

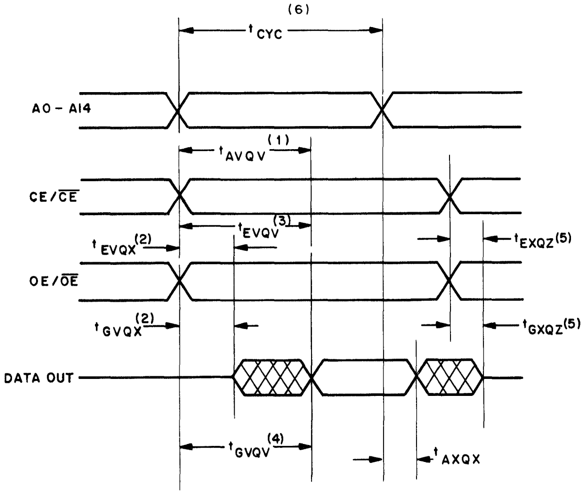
[d] TTL inputs.

[e] CMOS inputs.

CDM53256

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns; C_L = 100 pF, and 1 TTL Load; Input Pulse Levels: 0.8 V to 2.2 V

CHARACTERISTICS		LIMITS		UNITS
		Min.	Max.	
Address access time	t_{AVQV}	—	250	ns
Chip enable to output active	t_{EVQX}	0	—	
Output enable to output active	t_{GVQX}	0	—	
Chip enable access	t_{EVQV}	—	250	
Output enable to output valid	t_{GVQV}	—	90	
Data hold after address	t_{AXQX}	10	—	
Chip disable to output high Z	t_{EXQZ}	—	90	
Output disable to output high Z	t_{GXQZ}	—	70	
Cycle time	t_{CYC}	250	—	



NOTES:
(1) Assumes t_{GVQV} & t_{EVQV} are satisifed.
(2) Output Active requires both Chip Enable & Output Enable Active.
(3) Assumes t_{AVQV} & t_{GVQV} are satisified.
(4) Assumes t_{AVQV} & t_{EVQV} are satisified.
(5) Either Invalid Chip Enable or Output Enable causes Output High Z
(6) Generates 10 ns Valid Output Pulses (i.e., t_{CYC}-t_{AVQV}+t_{AXQX})

NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

92CM-36238

Fig. 2 - Timing waveforms.

APPLICATION INFORMATION

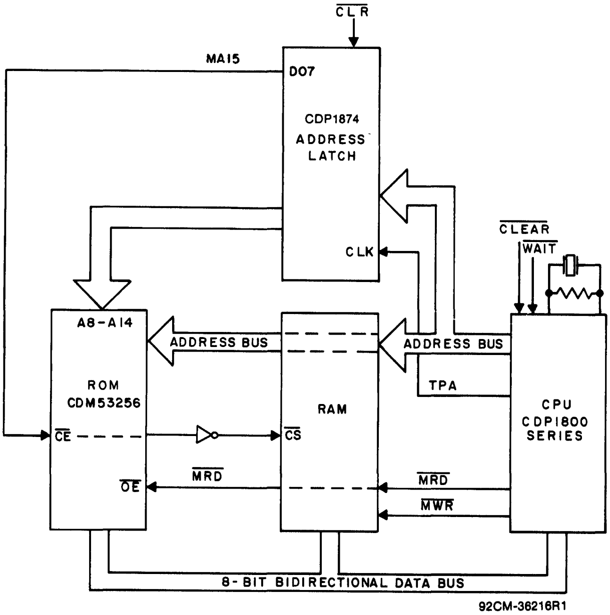


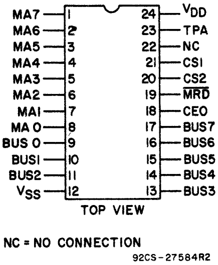
Fig. 3 - Typical CDP1800 series microprocessor system.

Decoupling Capacitors

The CDM53256 operates with a low average dc power supply current that varies with cycle time. However, CDM53256 is a large ROM with many internal nodes. Precharging of selected nodes during portions of the memory cycle results in short duration peak currents that can be much higher than the average dc value. The rise and fall times of the peak current pulses can have a value sufficient to generate unwanted system noise components. To minimize or eliminate the effects of the current spikes, a 0.1 μF ceramic decoupling capacitor is recommended between the VDD and VSS pins of every ROM device.

CDP1831, CDP1831C

Product Preview



Terminal Assignment

512-Word x 8-Bit Static Read-Only Memory

Features:

- *Compatible with CDP1800 and CD4000-series devices*
- *On-chip address latch*
- *Interfaces with CDP1802 microprocessor without additional components*
- *Optional programmable location within 64K memory space*
- *Three-state outputs*

The RCA-CDP 1831 and CDP1831C types are 4096-bit mask-programmable CMOS read-only memories organized as 512 words x 8 bits and are completely static; no clocks required. They will directly interface with CDP1800-series micro-processors without additional components.

The CDP1831 and CDP1831C respond to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 512-word block within 64K memory space. The polarity of the high address strobe (TPA), and CS1 and CS2 are user mask-program-

The Chip-Enable output signal (CEO) goes "high" when the device is selected, and is intended for use an an output disable control for RAM memory in a microprocessor system.

The CDP 1831C is functionally identical to the CDP1831. The CDP1831 has an operating voltage range of 4 to 10.5 volts, and the CDP1831C has an operating voltage range of 4 to 6.5 volts.

The CDP1831 and CDP1831C types are supplied in 24-lead hermetic dual-in-line, side-brazed ceramic packages (D suffix) and in 24-lead dual-in-line plastic packages (E suffix). The CDP1831C is also available in chip form (H suffix).

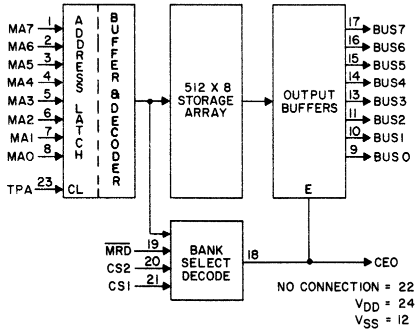


Fig. 1 - Functional diagram. 92CS-27587R3

File Number **1104**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(All voltage values referenced to V_{SS} terminal)

CDP1831	−0.5 to +11 V
CDP1831C	−0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPE D	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1831		CDP1831C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1831			CDP1831C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	—	5	5	—	0.01	50	—	0.02	200	μA
	—	10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	0.55	—	—	0.55	—	—	mA
	0.5	0,10	10	1.30	—	—	—	—	—	
Output High Drive (Source) Current, I_{OH}	4.6	0,5	5	−0.35	—	—	−0.35	—	—	
	9.5	0,10	10	−0.65	—	—	—	—	—	
Output Voltage Low-Level, V_{OL}	—	0,5	5	—	0	0.1	—	0	0.1	V
	—	0,10	10	—	0	0.1	—	—	—	
Output Voltage High Level, V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
	1,9	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	1,9	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any	0,5	5	—	$\pm10^{-4}$	±1	—	—	±1	mA
	Input	0,10	10	—	$\pm10^{-4}$	±2	—	—	—	
3-State Output Leakage Current, I_{OUT}	0,5	0,5	5	—	$\pm10^{-4}$	±1	—	—	±1	
	0,10	0,10	10	—	$\pm10^{-4}$	±2	—	—	—	
Input Capacitance, C_{in}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{out}	—	—	—	—	10	15	—	10	15	
Operating Current, I_{DD1}†	—	0,5	5	—	5	10	—	5	10	mA
	—	0,10	10	—	10	20	—	—	—	

*Typical values are for "one" T_A = 25°C and nominal V_{DD}

†Outputs open-circuited, cycle time = 2.5 μs

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$, V_{DD} ±5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1831			CDP1831C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Access Time from Address Change, t_{AA}	5	—	850	1000	—	850	1000	ns
	10	—	350	400	—	—	—	
Access Time from Chip Select, t_{ACS}	5	—	700	800	—	700	800	
	10	—	250	300	—	—	—	
Chip Select Delay, t_{CS}	5	—	600	—	—	600	—	
	10	—	200	300	—	—	—	
Address Setup Time, t_{AS}	5	50	—	—	50	—	—	
	10	25	—	—	—	—	—	
Address Hold Time, t_{AH}	5	150	—	—	150	—	—	
	10	75	—	—	—	—	—	
Read Delay, $t_{\overline{MRD}}$	5	—	300	500	—	300	500	
	10	—	100	150	—	—	—	
Chip Enable Output Delay from Address, t_{CA}	5	—	500	600	—	500	600	
	10	—	200	250	—	—	—	
Bus Contention Delay, t_D	5	—	200	350	—	200	350	
	10	—	100	150	—	—	—	
TPA Pulse Width, t_{PAW}	5	200	—	—	200	—	—	
	10	70	—	—	—	—	—	

†Time required by a limit device to allow for the indicated function.

*Time required by a typical device to allow for the indicated function Typical values are for T_A = 25°C and nominal V_{DD}

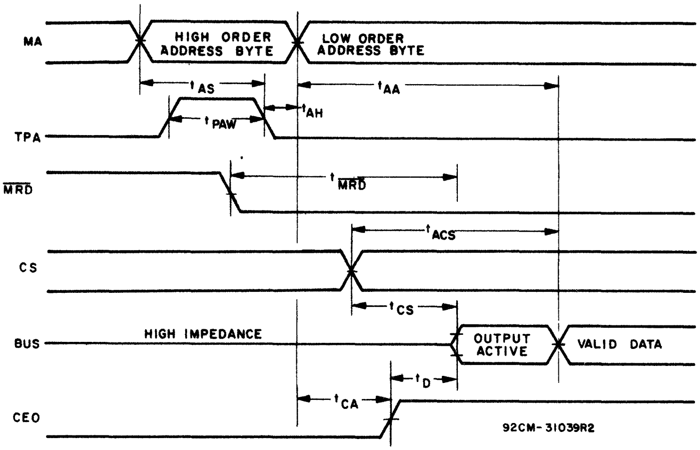


Fig. 2 - Timing waveforms.

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1831. When used directly with a CDP1800-series microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1831 is used with a CDP1800-series microprocessor:

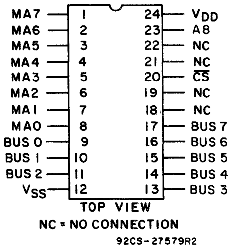
$t_{AH} = 0.5\ t_c$
$t_{PAW} = 1\ t_c$
$\overline{\text{MRD}}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

$$\text{where } t_c = \frac{1}{\text{CPU clock frequency}}$$

CDP1832, CDP1832C

Product Preview

TERMINAL ASSIGNMENT



512-Word x 8-Bit Static Read-Only Memory

Features:

- *Compatible with CDP1800 and CD4000-series devices*
- *Functional replacement for industry type 2704 512 x 8 EPROM*
- *Three-state outputs*

The RCA CDP1832 and CDP1832C types are 4096-bit mask-programmable CMOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems.

The CDP1832 ROMs are completely static; no clocks are required.

A Chip-Select input ($\overline{CS}$) is provided for memory expansion. Outputs are enabled when $\overline{CS}$=0.

The CDP1832 is a pin-for-pin compatible replacement for the industry types 2704 EPROM.

The CDP1832C is functionally identical to the CDP1832. The CDP1832 has an operating voltage range of 4 to 10.5 volts, and the CDP1832C has an operating voltage range of 4 to 6.5 volts.

The CDP1832 and CDP1832C are supplied in 24-lead, hermetic, dual-in-line, side-brazed, ceramic packages (D suffix) and in 24-lead dual-in-line plastic packages (E suffix). The CDP1832C is also available in chip form (H suffix).

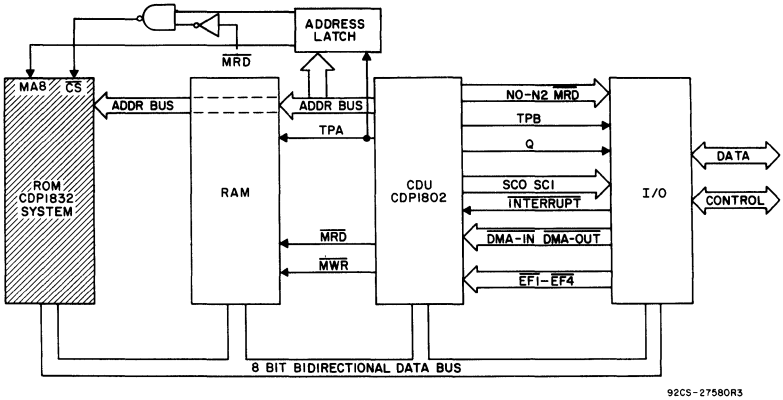


Fig. 1 - Typical CDP1802 microprocessor system.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltage referenced to V_{SS} terminal)	
CDP1832	-0.5 to +11 V
CDP1832C	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A=-40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mV/°C to 200 mW
For T_A=-55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A=+100 to 125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

OPERATING CONDITIONS at T_A=Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1832		CDP1832C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

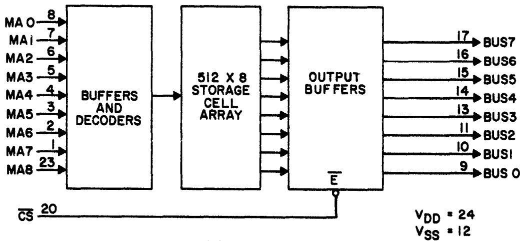


Fig. 2 - Functional diagram.

CDP1832, CDP1832C

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, V_{DD} ±5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1832			CDP1832C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	—	5	5	—	0.01	50	—	0.02	200	µA
	—	10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0, 5	5	0.55	—	—	0.55	—	—	mA
	0.5	0, 10	10	1.30	—	—	—	—	—	
Output High Drive (Source) Current, I_{OH}	4.6	0, 5	5	-0.35	—	—	-0.35	—	—	
	9.5	0, 10	10	-0.65	—	—	—	—	—	
Output Voltage Low-Level, V_{OL}	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level, V_{OH}	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
	1, 9	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	1, 9	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any	0, 5	5	—	$\pm10^{-4}$	±1	—	$\pm10^{-4}$	±1	µA
	Input	0, 10	10	—	$\pm10^{-4}$	±2	—	—	—	
3-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	—	$\pm10^{-4}$	±1	—	$\pm10^{-4}$	±1	
	0, 10	0, 10	10	—	$\pm10^{-4}$	±2	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current, I_{DD1}†	—	0, 5	5	—	5	10	—	5	10	mA
	—	0, 10	10	—	10	20	—	—	—	

*Typical values are for T_A=25°C and nominal V_{DD}.

†Outputs open-circuited; cycle time=2.5 µs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, V_{DD} ±5%, Input t_r,t_f=10 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1832			CDP1832C			
		Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Access Time From Address Change, t_{AA}	5	—	850	1000	—	850	1000	ns
	10	—	400	500	—	—	—	
Access Time From Chip Select, t_{ACS}	5	—	400	550	—	400	550	
	10	—	200	250	—	—	—	
Chip Select Delay, t_{CS}	5	—	200	250	—	200	250	
	10	—	100	130	—	—	—	

* Time required by a typical device to allow for the indicated function. Typical values are for T_A=25° C and nominal V_{DD}.

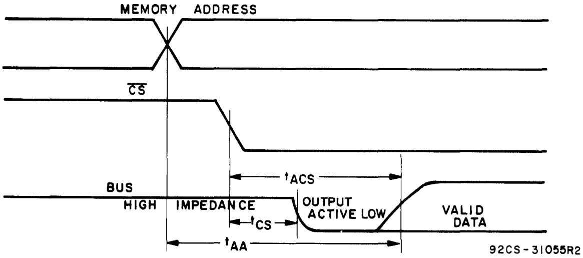
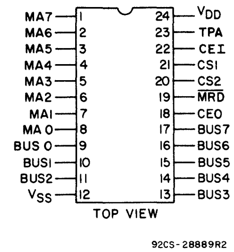


Fig. 3 - Timing waveforms.

CDP1833, CDP1833C, CDP1833BC

CMOS 1024-Word x 8-Bit Static Read-Only Memory



TERMINAL ASSIGNMENT

Features:

- *CDP1833BC is compatible with the CDP1802BC 5 MHz microprocessor*
- *On-chip address latch*
- *Interfaces with CDP1800-series microprocessors without additional components*
- *Optional programmable location within 64K memory space*
- *Three-state outputs*

The RCA-CDP1833, CDP1833C, and CDP1833BC are static 8192-bit mask-programmable CMOS read-only memories organized as 1024-words x 8 bits and are completely static; no clocks are required. They will directly interface with the CDP1800-series microprocessors without additional components.

The CDP1833, CDP1833C, and CDP1833BC respond to a 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 1024-word block within 64K memory space. The polarity of the high-address strobe (TPA), CEI, CS1, and CS2 are user mask-programmable.

The Chip-Enable output signal (CEO) is "high" when the device is selected. Terminals CEO and CEI can be connected in a daisy chain to control selection of RAM memory in a microprocessor system without additional components.

The CDP1833C and CDP1833BC are functionally identical to the CDP1833. The CDP1833 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1833C and CDP1833BC have a recommended operating voltage range of 4 to 6.5 volts. The CDP1833BC is designed to interface with the CDP1802BC microprocessor.

The CDP1833, CDP1833C, and CDP1833BC are supplied in 24-lead hermetic dual-in-line side-brazed ceramic package (D suffix) and 24-lead dual-in-line plastic package (E suffix). The CDP1833C is also available in chip form (H suffix).

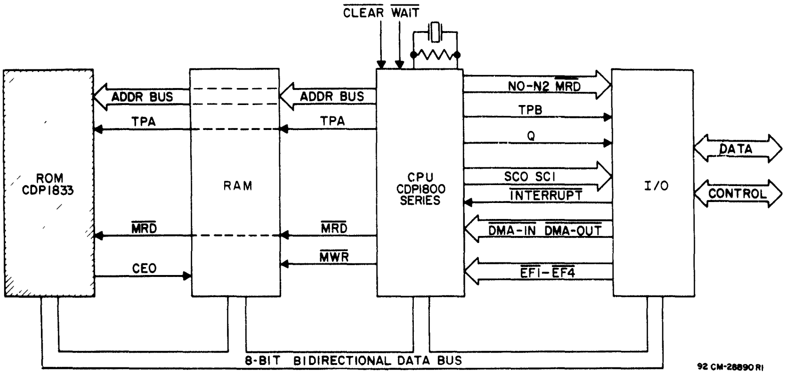


Fig. 1 - Typical CDP1800 Series microprocessor system.

File Number **1135**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltage referenced to V_{SS} terminal)	
CDP1833	-0.5 to +11 V
CDP1833C, CDP1833BC	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D).	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 12 mV/° C to 200 mW
For T_A = -55 to +100° C (PACKAGE TYPE D)	500 mW
For T_A = +100 to 125° C (PACKAGE TYPE D)	Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Packages)	100 mW
OPERATING-TEMPERATURE RANGE (T_A)·	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1 59 ± 0.79 mm) from case for 10 s max	+265°C

OPERATING CONDITIONS at T_A = -40° to +85° C
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1833		CDP1833C, CDP1833BC		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

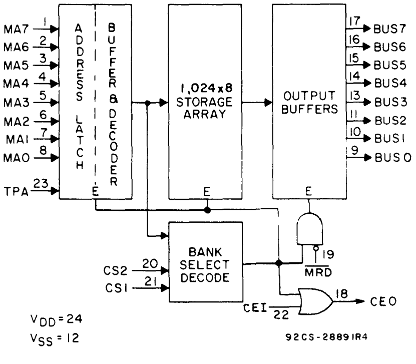


Fig. 2 - Functional diagram.

CDP1833, CDP1833C, CDP1833BC

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1833			CDP1833C, CDP1833BC			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current I_{DD}	—	5	5	—	0.01	50	—	0.02	200	µA
	—	10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current I_{OL}	0.4	0, 5	5	0.8	—	—	0.8	—	—	mA
	0.5	0, 10	10	1.8	—	—	—	—	—	
Output High Drive (Source) Current I_{OH}	4.6	0, 5	5	-0.8	—	—	-0.8	—	—	
	9 5	0, 10	10	-1.8	—	—	—	—	—	
Output Voltage Low-Level V_{OL}	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level V_{OH}	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
	1, 9	—	10	—	—	3	—	—	—	
Input High Voltage V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	1, 9	—	10	7	—	—	—	—	—	
Input Leakage Current I_{IN}	Any Input	0, 5	5	—	$\pm 10^{-4}$	±1	—	$\pm 10^{-4}$	±1	µA
		0, 10	10	—	$\pm 10^{-4}$	±2	—	—	—	
3-State Output Current I_{OUT}	0, 5	0, 5	5	—	$\pm 10^{-4}$	±1	—	$\pm 10^{-4}$	±1	
	0, 10	0, 10	10	—	$\pm 10^{-4}$	±2	—	—	—	
Operating Device Current I_{DD1}†	—	0, 5	5	—	7	10	—	7	10	mA
	—	0, 10	10	—	14	20	—	—	—	
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	

* Typical values are for T_A = 25° C and nominal V_{DD}.

† Outputs open-circuit; cycle time = 2.5 µs

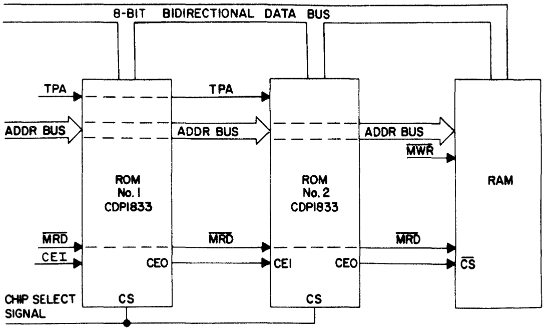


Fig. 3 - Daisy chaining CDP1833's.

"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between ROM and RAM in a user system. In the above configuration, if ROM #1 was masked-programmed for memory locations $0000\text{-}03FF_{16}$ and ROM #2 masked-programmed for memory locations $0400_{16}\text{-}07FF_{16}$, for address from $0000\text{-}07FF_{16}$ the RAM would be disabled and the ROM enabled. For locations above $07FF_{16}$ the ROM's would be disabled and the RAM enabled.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to =85° C, V_{DD} ± 5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CDP1833			CDP1833C			CDP1833BC			
	V_{DD} (V)	Min.#	Typ.•	Max.	Min.#	Typ.•	Max.	Min.#	Typ.•	Max.	
Access Time From Address Change t_{AA}	5	—	650	775	—	650	775	—	575	700	ns
	10	—	350	425	—	—	—	—	—	—	
Access Time From Chip Select t_{ACS}	5	—	500	625	—	500	625	—	475	600	
	10	—	275	310	—	—	—	—	—	—	
Chip Select Delay t_{CS}	5	—	250	320	—	250	320	—	250	320	
	10	—	125	180	—	—	—	—	—	—	
Address Setup Time t_{AS}	5	75	50	—	75	50	—	75	50	—	
	10	40	25	—	—	—	—	—	—	—	
Address Hold Time t_{AH}	5	100	75	—	100	75	—	75	50	—	
	10	50	30	—	—	—	—	—	—	—	
Read Delay $t_{\overline{MRD}}$	5	—	400	500	—	400	500	—	400	500	
	10	—	200	275	—	—	—	—	—	—	
Chip Enable Output Delay from Address t_{CA}	5	—	120	170	—	120	170	—	120	170	
	10	—	70	100	—	—	—	—	—	—	
Bus Contention Delay t_D	5	—	220	270	—	220	270	—	220	270	
	10	—	130	150	—	—	—	—	—	—	
TPA Pulse Width t_{PAW}	5	200	—	—	200	—	—	175	—	—	
	10	70	—	—	—	—	—	—	—	—	
Chip Enable In to Chip Enable Out Delay t_{CEIO}	5	—	200	250	—	200	250	—	200	250	
	10	—	100	150	—	—	—	—	—	—	

# Time required by a limit device to allow for the indicated function.

• Time required by a typical device to allow for the indicated function. Typical values are for T_A = 25° C and nominal voltages

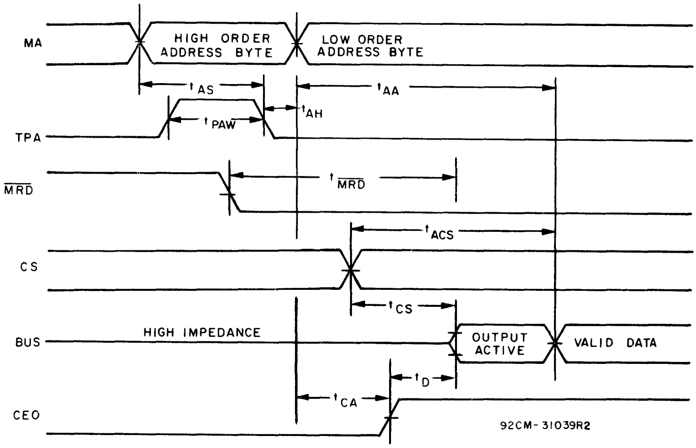


Fig. 4 - Timing waveforms.

CDP1833, CDP1833C, CDP1833BC

Note:

The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1833. When used directly with a CDP1800-series microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

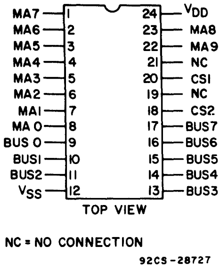
The following general timing relationships will hold when the CDP1833 is used with a CDP1800-series microprocessor.

$t_{AH} = 0.5\ t_C$
$t_{PAW} = 1\ t_C$

$\overline{MRD}$ occurs one clock period (t_C) earlier than the address bits MA0-MA7.

$$\text{where } t_C = \frac{1}{\text{CPU clock frequency}}$$

CDP1834, CDP1834C



TERMINAL ASSIGNMENT

1028-Word x 8-Bit Static Read-Only Memory

Features:

- *Industry pin compatible*
- *Three-state outputs*

The RCA-CDP1834 and CDP1834C are 8192-bit mask-programmable CMOS read-only memories organized as 1024-words x 8-bits and designed for use in CDP1800-series microprocessor systems. The CDP1834-series ROM's are completely static; no clocks are required

Two Chip-Select inputs (CS1, CS2) are provided for memory expansion. The polarity of each Chip-Select is user mask-programmable. The CDP1834-series is pin-compatible with industry type 2708 EPROM. The CDP1834C is functionally identical to the CDP1834. The CDP1834 has a recommended operating voltage range of 4 to 10.5 volts and the CDP1834C has a recommended operating voltage range of 4 to 6.5 volts. The CDP1834 and the CDP1834C are supplied in 24-lead dual-in-line ceramic packages (D suffix) and in 24-lead dual-in-line plastic packages (E suffix). The CDP1834C is also available in chip form (H suffix).

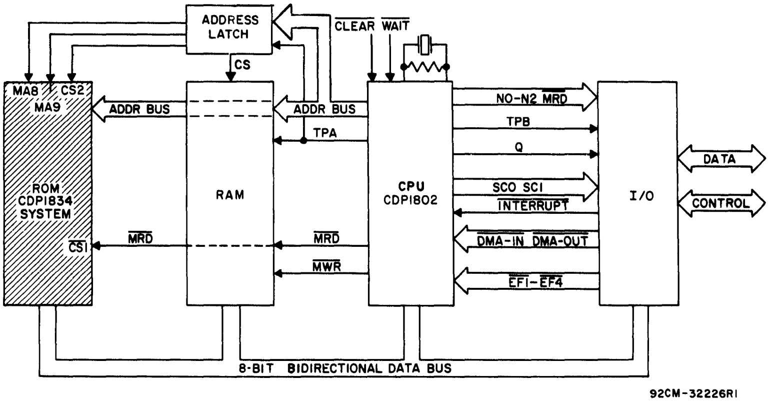


Fig 1 - Typical CDP1802 microprocessor system.

File Number **1143**

CDP1834, CDP1834C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})·	
(All voltage values referenced to V_{SS} terminal)	
CDP1834	0.5 to +11 V
CDP1834C	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = 100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = FULL PACKAGE-TEMPERATURE RANGE	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} 5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1834			CDP1834C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current I_{DD}	—	5	5	—	0.01	50	—	0.02	200	µA
	—	10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current I_{OL}	0.4	0, 5	5	0.8	—	—	0.8	—	—	mA
	0.5	0, 10	10	1.8	—	—	—	—	—	
Output High Drive (Source) Current I_{OH}	4.6	0, 5	5	-0.8	—	—	-0.8	—	—	
	9.5	0, 10	10	-1.8	—	—	—	—	—	
Output Voltage Low-Level V_{OL}	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level V_{OH}	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	
	1, 9	—	10	—	—	3	—	—	—	
Input High Voltage V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	
	1, 9	—	10	7	—	—	—	—	—	
Input Leakage Current I_{IN}	Any	0, 5	5	—	—	±1	—	—	±1	µA
	Input	0, 10	10	—	—	±2	—	—	—	
3-State Output Leakage Current I_{OUT}	0, 5	5	5	—	—	±1	—	—	±1	
	0, 10	10	10	—	—	±2	—	—	—	
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current I_{DD1}†	—	0, 5	5	—	7	10	—	7	10	mA
	—	0, 10	10	—	14	20	—	—	—	

*Typical values are for T_A = 25°C and nominal V_{DD}.

†Outputs open-circuited; cycle time = 2.5 µs.

CDP1834, CDP1834C

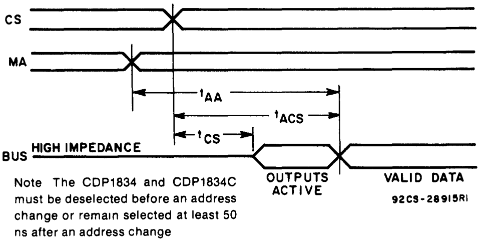
OPERATING CONDITIONS at T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1834		CDP1834C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to + 85°C, V_{DD} ± 5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1834			CDP1834C			
		Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Access Time from Address Change, t_{AA}	5	—	575	750	—	575	750	ns
	10	—	350	425	—	—	—	
Access Time from Chip Select, t_{ACS}	5	—	600	700	—	600	700	ns
	10	—	325	410	—	—	—	
Chip Select Delay, t_{CS}	5	—	480	580	—	480	580	ns
	10	—	250	340	—	—	—	

*Typical values are for T_A = 25°C and nominal V_{DD}.



Note The CDP1834 and CDP1834C must be deselected before an address change or remain selected at least 50 ns after an address change

Fig. 2 - Timing waveforms.

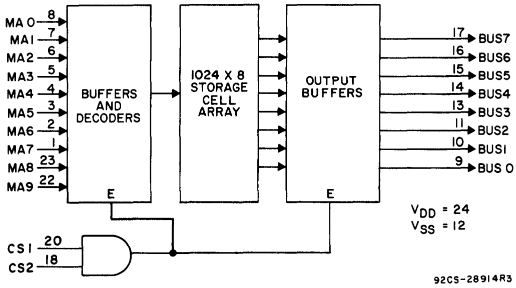
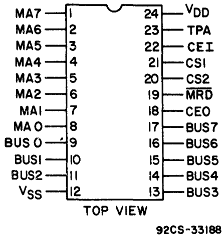


Fig. 3 - Functional diagram.

CDP1835C

CMOS 2048-Word x 8-Bit Static Read-Only Memory



TERMINAL ASSIGNMENT

Features:

- *Interfaces with CDP1800-series microprocessors ($f_{clock} \leq 5$ MHz) without additional components*
- *On-chip address latch*
- *On-chip address decoder provides programmable location within 64K memory space*
- *Three-state outputs*

The RCA-CDP1835C is a 16384-bit mask-programmable CMOS read-only memory, organized as 2048 words x 8 bits and is completely static: no clocks required. It will directly interface with CDP1800-series microprocessors that have clock frequencies up to 5 MHz without additional components.

The CDP1835C responds to a 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 2048-word block of 64K memory space. The polarity of the high address strobe (TPA), $\overline{\text{MRD}}$, CEI, CS1, and CS2 are user mask-programmable.

The Chip-Enable output signal (CEO) is "high" when the device is selected. Terminals CEO and CEI can be connected in a daisy chain to control selection of RAM memory in a microprocessor system without additional components.

The CDP1835C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1835C is supplied in 24-lead heremetic dual-in-line side-brazed ceramic packages (D suffix) and 24-lead dual-in-line plastic packages (E suffix).

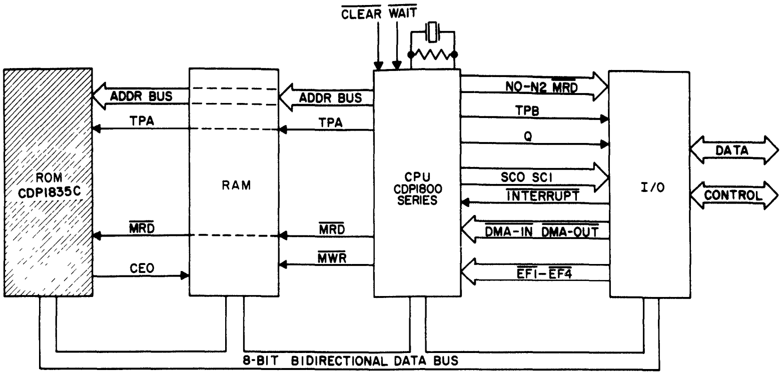


Fig. 1 - Typical CDP1800 Series microprocessor system.

MAXIMUM RATING, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (All voltages referenced to V_{SS} terminal)	-0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR For T_A = FULL PACKAGE-TEMPERATURE RANGE	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) At distance 1/16 ± 1/32 in (1.59 ± 0.79 mm) from case for 10 s max	+265°C

OPERATING CONDITIONS at T_A = FULL PACKAGE-TEMPERATURE RANGE

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS CDP1835C		UNITS
	Min.	Max.	
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	

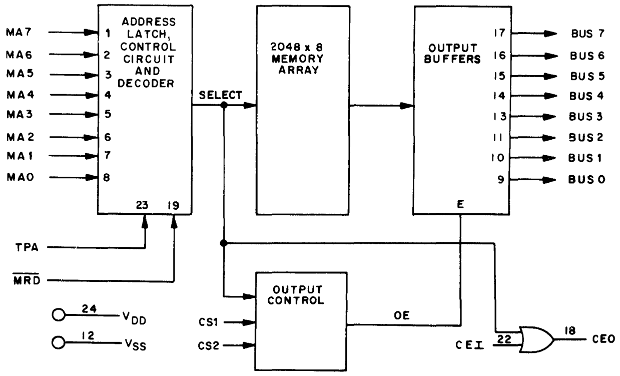


Fig. 2 - Functional block diagram.

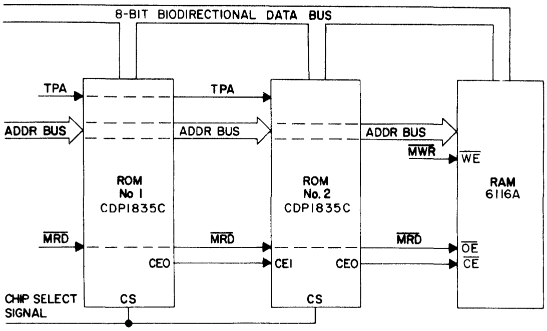
CDP1835C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 5%, except as noted

CHARACTERISTIC		CONDITIONS		LIMITS			UNITS
		V_O (V)	V_{IN} (V)	CDP1835C			
				Min.	Typ.*	Max.	
Quiescent Device Current	I_{DD}	—	0, V_{DD}	—	5	50	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, V_{DD}	0.8	1.6	—	mA
Output High Drive (Source) Current	I_{OH}	V_{DD} -0.4	0, V_{DD}	-0.8	-1.6	—	
Output Voltage Low-Level	V_{OL}	—	0, V_{DD}	—	0	0.1	V
Output Voltage High-Level	V_{OH}	—	0, V_{DD}	V_{DD} -0.1	V_{DD}	—	
Input Low Voltage	V_{IL}	V_{DD} -0.5	—	—	—	1.5	
Input High Voltage	V_{IH}	V_{DD} -0.5	—	3.5	—	—	
Input Leakage Current (Any Input)	I_{IN}	—	0, V_{DD}	—	—	±1	µA
3-State Output Leakage Current	I_{OUT}	0, V_{DD}	0, V_{DD}	—	—	±2	
Operating Device Current	I_{OPER}•	—	0, V_{DD}	—	5	10	mA
Input Capacitance	C_{IN}	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	10	15	

*Typical values are for T_A = 25° C and nominal V_{DD}.

•Outputs open circuited; cycle time 1 µs.



92CS-33190R3

Fig 3 - Typical use of daisy chaining feature of the CDP1835C.

"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between ROM and RAM in a user system In the above configuration, if ROM No. 1 was masked-programmed for memory locations 0000-07FF$_{16}$ and ROM No. 2 masked-programmed for memory locations 0800$_{16}$-0FFF$_{16}$, for addresses from 0000-0FFF$_{16}$, the RAM would be disabled and one of the ROMs enabled. For locations above 0FFF$_{16}$, the ROM's would be disabled and the RAM enabled

Signal Descriptions

MA0-MA7: 16-bit multiplexed address inputs. The high-byte address bits are strobed into the on-chip address lath with the trailing edge of TPA. High-byte bits A11, A12, A13, A14 and A15 are polarity mask-programmable for use as chip enable inputs for memory expansion.

$\overline{\text{MRD}}$: Memory read input. Controls the output buffers and Chip Enable Output (CEO), and powers down the ROM. $\overline{\text{MRD}}$ must be valid on or before the trailing edge of TPA. When $\overline{\text{MRD}}$ is not valid, the output buffers are tri-stated. The active polarity of $\overline{\text{MRD}}$ is mask-programmable.

CS1, CS2: Mask-programmable chip-select inputs. The chip-select inputs control the data output buffers only (not CEO). The output buffers will be tri-stated when either CS1 or CS2 is not valid

TPA: The trailing edge of TPA is used to latch the high-byte of the 16-bit multiplexed address. The ROM is enabled after the trailing edge of TPA ($\overline{\text{MRD}}$ active). The active polarity of TPA is mask-programmable.

CEI, CEO: The Chip Enable Input (CEI), in conjunction with the Chip Enable Output (CEO) can be used in a "Daisy Chain" configuration to avoid memory conflicts between ROM and RAM. CEO is high when the ROM is enabled (i.e., $\overline{\text{MRD}}$ is low, TPA toggled) or CEI is active. The active polarity of CEI is mask-programmable.

BUS0-BUS7: 8-Bit Tri-State data bus.

VDD, VSS: Power supply connections

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5V ± 5%
Input t_r, t_f = 10 ns, C_L = 100 pF, and 1 TTL Load

CHARACTERISTIC		LIMITS CDP1835C		UNITS
		Min.	Max.	
Access Time from Address Change	t_{AVQV}	—	500	ns
Chip Select to Output Active	t_{SVQX}	0	200	
Address Setup Time	t_{AS}	50	—	
Address Hold Time	t_{AH}	50	—	
$\overline{\text{MRD}}$ Setup Time *	t_{RSU}	0	—	
Chip Enable Output Delay from TPA	t_{CA}	—	125	
Output Delay from TPA	t_D	—	200	
TPA Pulse Width	t_{PAW}	125	—	
Chip Enable In to Chip Enable Out Delay	t_{CEIO}	—	100	
Chip Select to Output Valid	t_{SVQV}	—	200	
Chip Deselect to Output High Z	t_{SXQZ}	—	200	
$\overline{\text{MRD}}$ to CEO Low	t_{RXCL}	—	150	
$\overline{\text{MRD}}$ to Output High Z	t_{RXQZ}	—	200	

* $\overline{\text{MRD}}$ must be valid on or before the trailing edge of TPA. (Output will be tri-stated and the ROM powered down when $\overline{\text{MRD}}$ is not valid.)

CDP1835C

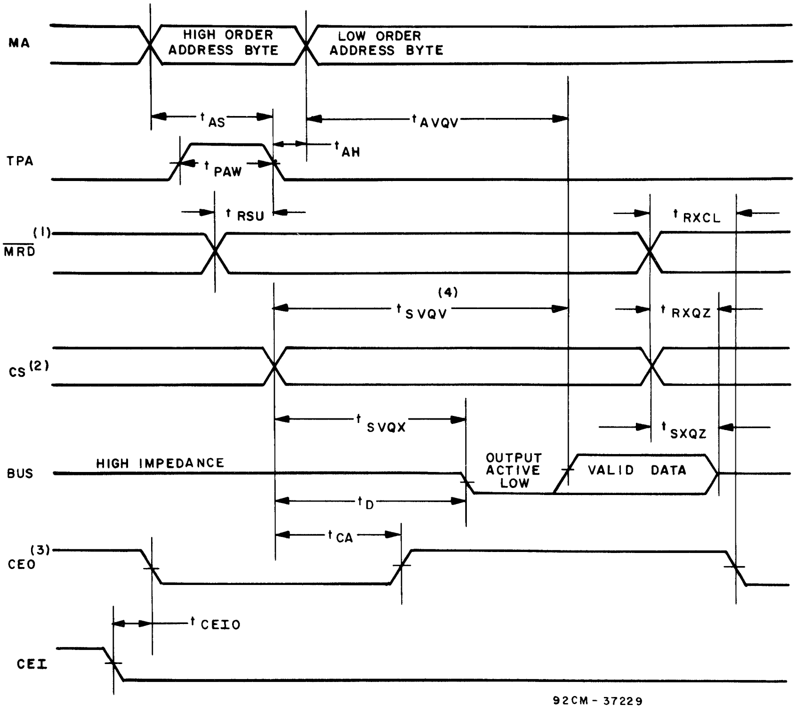


Fig 4 - Timing diagram.

Notes:

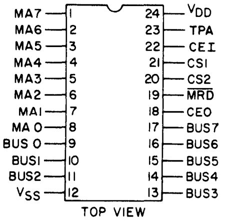
(1) $\overline{\text{MRD}}$ must be valid on or before the trailing edge of TPA. (Output will be tri-stated and the ROM powered down when $\overline{\text{MRD}}$ is not valid.

(2) CS (CS1 and CS2) controls the output buffers only. Output will be tri-stated when either CS1 or CS2 is not valid.

(3) CEO is high when ROM is enabled.

(4) Provided t_{AVQV} is satisfied.

CDP1837C



92CS-28889R2

TERMINAL ASSIGNMENT

4096-Word x 8-Bit Static Read-Only Memory

Features:

- *Interfaces with CDP1800-series microprocessors ($f_{clock} \leq 5$ MHz) without additional components*
- *On-chip address latch*
- *On-chip address decoder provides programmable location within 64K memory space*
- *Three-state outputs*

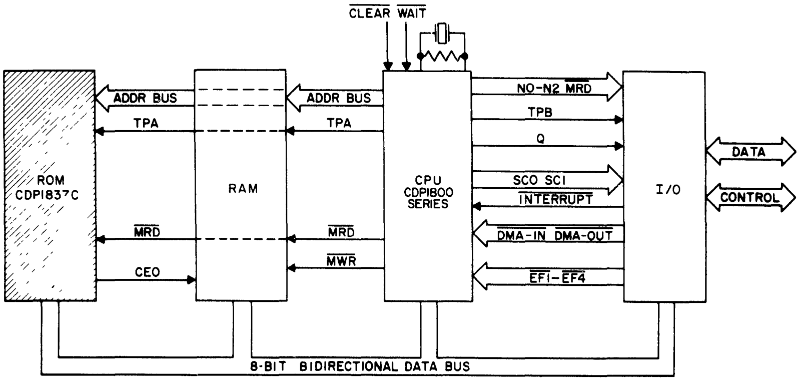
The RCA-CDP1837C is a 32768-bit mask-programmable CMOS read-only memory, organized as 4096 words x 8 bits and is completely static: no clocks required. It will directly interface with CDP1800-series microprocessors, having clock frequencies up to 5 MHz, without additional components.

The CDP1837C responds to a 16-bit address multiplexed on 8 address lines Address latches are provided on chip for storing the high byte address data. By mask option, this ROM can be programmed to operate in any 4096-word block of 64-K memory space. The polarity of the high address strobe (TPA), $\overline{MRD}$, CEI, CS1, and CS2 are user mask-programmable.

The Chip-Enable output signal (CEO) is "high" when the device is selected. Terminals CEO and CEI can be connected in a daisy chain to control selection of RAM memory in a microprocessor system without additional components.

The CDP1837C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1837C is supplied in 24-lead heremetic dual-in-line side-brazed ceramic packages (D suffix) and 24-lead dual-in-line plastic packages (E suffix).



92CM-35120

Fig. 1 - Typical CDP1800 Series microprocessor system.

File Number **1381**

CDP1837C

MAXIMUM RATING, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltages referenced to V_{SS} terminal) .... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPE D) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPE D .... -55 to +125°C
PACKAGE TYPE E .... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 in (1 59 ± 0 79 mm) from case for 10 s max .... +265°C

OPERATING CONDITIONS at T_A = FULL PACKAGE-TEMPERATURE RANGE

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	LIMITS		UNITS
	CDP1837C		
	MIN.	MAX.	
Supply-Voltage Range	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	

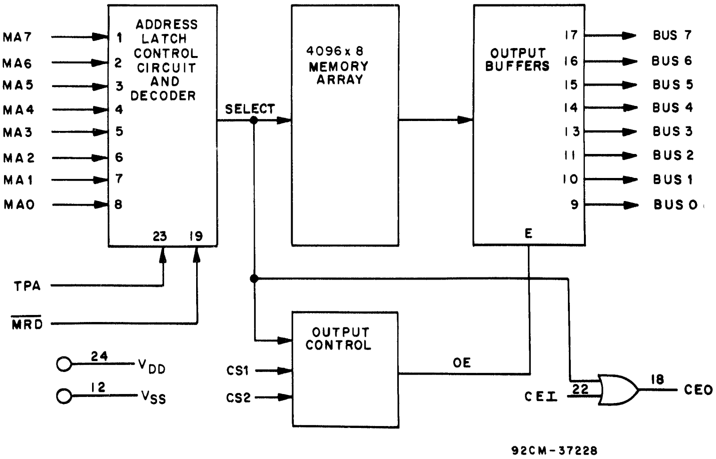


Fig. 2 - Functional block diagram.

CDP1837C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 5%, except as noted

CHARACTERISTIC		CONDITIONS		LIMITS			UNITS
				CDP1837C			
		V_O (V)	V_{IN} (V)	Min.	Typ.*	Max.	
Quiescent Device Current	I_{DD}	—	0, V_{DD}	—	5	50	µA
Output Low Drive (Sink) Current	I_{OL}	0 4	0, V_{DD}	0 8	1.6	—	mA
Output High Drive (Source) Current	I_{OH}	V_{DD} -0.4	0, V_{DD}	-0.8	-1.6	—	
Output Voltage Low-Level	V_{OL}	—	0, V_{DD}	—	0	0.1	V
Output Voltage High-Level	V_{OH}	—	0, V_{DD}	V_{DD} -0.1	V_{DD}	—	
Input Low Voltage	V_{IL}	V_{DD} -0.5	—	—	—	1 5	
Input High Voltage	V_{IH}	V_{DD} -0.5	—	3.5	—	—	
Input Current	I_{IN}	—	0, V_{DD}	—	—	±1	µA
3-State Output Leakage Current	I_{OUT}	0, V_{DD}	0, V_{DD}	—	—	±2	
Operating Device Current	I_{OPER}•	—	0, V_{DD}	—	5	10	mA
Input Capacitance	C_{IN}	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	10	15	

*Typical values are for T_A = 25° C and nominal V_{DD}.

•Outputs open circuited; cycle time 1 µs.

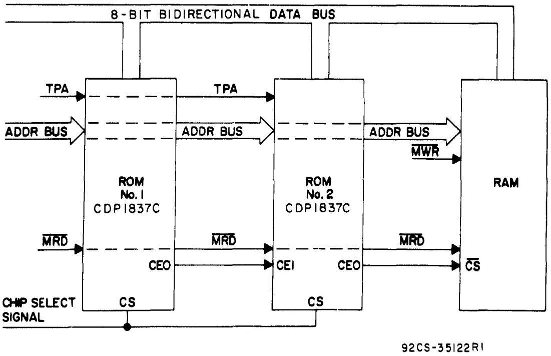


Fig. 3 - Daisy chaining CDP1837C's.

"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between ROM and RAM in a user system. In the above configuration, if ROM No. 1 was masked-programmed for memory locations 0000-0FFF$_{16}$ and ROM No. 2 masked-programmed for memory locations 1000$_{16}$-1FFF$_{16}$, for addresses from 0000-1FFF$_{16}$, the RAM would be disabled and one of the ROMs enabled. For locations above 1FFF$_{16}$, the ROM's would be disabled and the RAM enabled.

CDP1837C

Signal Descriptions

MA0-MA7: 16-bit multiplexed address inputs. The high-byte address are strobed into the on-chip address latch with the trailing edge of TPA. High-byte bits A12, A13, A14 and A15 are polarity mask-programmable for use as chip enable inputs for memory expansion.

$\overline{\text{MRD}}$: Memory read input. Controls the output buffers and Chip Enable Output (CEO), and powers down the ROM. $\overline{\text{MRD}}$ must be valid on or before the trailing edge of TPA. When $\overline{\text{MRD}}$ is not valid, the output buffers are tri-stated. The active polarity of $\overline{\text{MRD}}$ is mask-programmable.

CS1, CS2: Mask-programmable chip-select inputs. The chip-select inputs control the output buffers only (not CEO). The output buffers will be tri-stated when either CS1 or CS2 is not valid.

TPA: The trailing edge of TPA is used to latch the high byte of the 16-bit multiplexed address. The ROM is enabled after the trailing edge of TPA ($\overline{\text{MRD}}$ active). The active polarity of TPA is mask-programmable.

CEI, CEO: The Chip Enable Input (CEI), in conjunction with the Chip Enable Output (CEO) can be used in a "Daisy Chain" configuration to avoid memory conflicts between ROM and RAM. CEO is high when the ROM is enabled (i.e., $\overline{\text{MRD}}$ is low, TPA toggled) or CEI is active. The active polarity of CEI is mask-programmable.

BUS0-BUS7: 8-Bit Tri-State data bus.

VDD, VSS: Power supply connections

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5V ± 5%
Input t_r, t_f = 10 ns, C_L = 100 pF, and 1 TTL Load

CHARACTERISTIC		LIMITS CDP1837C		UNITS
		Min.	Max.	
Access Time from Address Change	t_{AVQV}	—	500	ns
Chip Select to Output Active	t_{SVQX}	0	200	
Address Setup Time	t_{AS}	50	—	
Address Hold Time	t_{AH}	50	—	
$\overline{\text{MRD}}$ Setup Time *	t_{RSU}	0	—	
Chip Enable Output Delay from TPA	t_{CA}	—	125	
Output Delay from TPA	t_D	—	200	
TPA Pulse Width	t_{PAW}	125	—	
Chip Enable In to Chip Enable Out Delay	t_{CEIO}	—	100	
Chip Select to Output Valid	t_{SVQV}	—	200	
Chip Deselect to Output High Z	t_{SXQZ}	—	200	
$\overline{\text{MRD}}$ to CEO Low	t_{RXCL}	—	150	
$\overline{\text{MRD}}$ to Output High Z	t_{RXQZ}	—	200	

* $\overline{\text{MRD}}$ must be valid on or before the trailing edge of TPA. (Output will be Tri-Stated and the ROM powered down when $\overline{\text{MRD}}$ is not valid.)

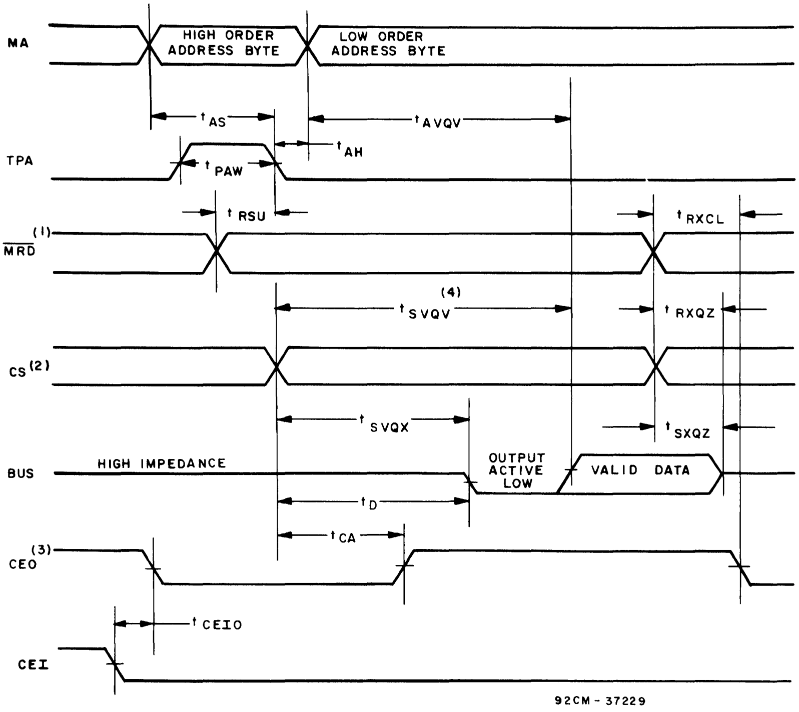


Fig 4 - Timing diagram

Notes:

(1) $\overline{\text{MRD}}$ must be valid on or before the trailing edge of TPA. (Output will be tri-stated and the ROM powered down when $\overline{\text{MRD}}$ is not valid.

(2) CS (CS1 and CS2) controls the output buffers only. Output will be tri-stated when either CS1 or CS2 is not valid.

(3) CEO is high when ROM is enabled.

(4) Provided t_{AVQV} is satisfied.

High-Reliability Microprocessors, Memories, and Peripherals

7

High-Reliability Microprocessor, Memories and Peripherals
Non-Radiation Hardened CMOS LSI Devices

Features:

- *Low power consumption*
- *Fully Static*
- *Single power supply*
- *Full military temperature range*
- *High noise immunity*
- *Complete family which includes RAMs, ROMs, and I/Os*
- *Full CMOS CDP1802 microrocessor*

The RCA high-reliability slash-series of CMOS LSI microprocessor, memories, and peripherals are ideally suited for military applications such as mobile ground equipment that must be battery operated and exposed to harsh environments. Use of a high-reliable, all CMOS LSI technology provides low power operation throughout the military temperature range.

The 'Slash 3' suffix following the type designation indicates that the devices are screened to military specifications as described in the lot screening sequence on the next page.

CDP1800 Series

The RCA CDP1800 series offers a complete line of CMOS microprocessor, and associated memory and peripheral devices. The heart of the series is the CDP1802A central processing unit (CPU). This unit, which features CMOS register-based architecture, offers 16 internal registers to facilitate data manipulation and to reduce the need for additional devices. The need for external devices is even further reduced by use of on-chip clock, DMA, and single phase operation.

The microprocessor uses CMOS technology, designed on a single chip to maintain low power drain intended for multi-system applications requiring general-purpose CPU-s, large memory address space, and extensive external I/O for use with optimized peripherals.

The RCA CDP1800-series memory/microprocessor product line offers the system designer exceptional flexibility in hardware/software tradeoffs. In addition this product line includes a programmable I/O, universal asynchronous receiver-transmitter (UART), directly interfaceable random-access memories (RAMs) and read-only memories (ROMs).

The RCA-CDP1800 Slash(/) Series memories are designed for use in memory systems where high speed, low operating current, and simplicity in use are desirable. These devices feature excellent noise immunity. These types have separate data inputs and outputs and utilize a single power supply of 4 to 6.5 volts.

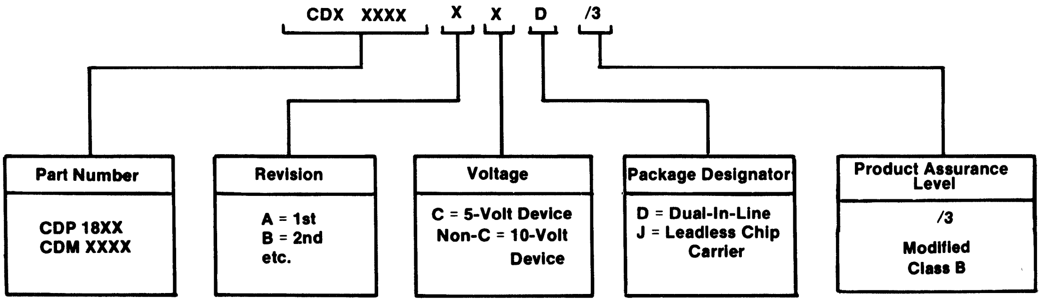
General-Purpose Memories

In addition to the memories designed to interface directly with CDP1800-series RCA also features a line of general-purpose memories. These memories include industry-standard ROM's that can be mask-programmed to meet customer application requirements. These ROMs feature: low-power CMOS technology with high-noise immunity and full-temperature-range characteristics.

The list of memories also includes fully static CMOS RAMs with densities up to 32K-bytes, low operating power, low standby current, and memory retention for 2 to 2.5 volt minimum standby battery voltage.

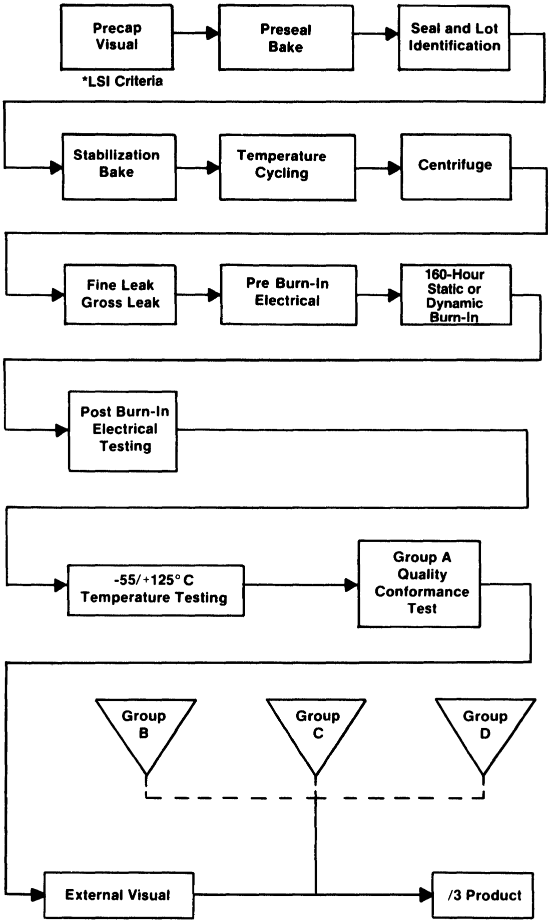
The standard versions of these devices are screened to the RCA "Slash 3" (Modified Class B) screening sequence.

Guide to the Part Number, Package Designator, and Product Assurance Level of RCA High-Reliability CDP18XX Series.



Non-Radiation Hardened CMOS LSI Devices

Product Flow Chart
GE Solid State Product Assurance Level /3
*Modified Class B Screening



Optional Groups B, C and D Inspection Lot Conformance Testing are performed only if specifically ordered.

Data Supplied

Data supplied with /3 Product consists of:
- a) A Certificate of Processing and Screening Compliance,
- b) An Attribute Summary of Group A results,
- c) Group B, C, and D Attribute Test results (when ordered).

Non-Radiation Hardened CMOS LSI Devices

High-Reliability LSI Microprocessor Memories and Peripherals

Lot Screening Tests - /3 Screening

SCREEN	METHOD (MIL-STD-883)	REQMT.	NOTES
Internal Visual	Cond. B Modified for LSI Visual	100%	1, 2
Pre-Seal Bake	—	100%	
Stablization Bake	1008 Cond. C (150°C Min.) 24 Hours	100%	
Temperature Cycling	1010 (-65°C to 150°C) Cond. C	100%	
Constant Acceleration (Centrifuge)	2001 Cond. E (30,000 G) Y1 Dir.	100%	4
Seal	1014		
A) Fine	A or B	100%	
B) Gross	C	100%	
Initial (Pre Burn-In) Electrical Parameters at 25°C	Per Applicable Device Spec.	100%	
Burn-In	1015, 160 Hrs @ 125°C	100%	3
Interim (Post Burn-In) Electrical Parameters at 25°C	Per Applicable Device Spec.	100%	
Final Electrical Test @ -55/125°C	Per Applicable Device Spec.	100%	
Group A Quality Conformance Test	5005	Sample	
External Visual	2009	100%	

NOTES:

Note 1. **Internal Visual Inspection Modified for LSI**
Internal Visual Inspection is performed to MIL-STD-883, Method 2010, Condition B **except** as follows:

A. **High Magnification Inspection** is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required.

B. **Metallization Voids (3.2.1.2)**
Criteria 3.2.1.1a Metallization Scratches, and 3.2.1.2a Metallization Voids shall also apply to metallization over a passivation step (3.2.1.1d, 3.2.1.2b). Underlying oxide must also be exposed.

C. **Metallization Alignment (3.2.1.7)**
Diffusion and Passivation Layer(s) Faults (3.2.0)
High magnification inspection is performed at 200X to 300X, applied to the center and two opposite corners of the chip, consisting only of the area exposed to the immediate field of view.

D. **Scribing and Die Defects (3.2.3)**
In addition: A crack that exceeds 5.0 mils in length must also point to or cross a scribe grid line to be unacceptable. Semi-circular cracks that point away from the active circuit are acceptable.

Note 2. **SOS Technology Devices;** CDP1821, 1822, 1823, CDM5114 Only

1. Diffusion faults are not applicable. SOS devices are inspected for complete islands, bridging between islands and missing adjacent contacts from a row in a contact chain.
2. The 1.0 mil wire clearance criteria is not applicable.
3. Passivation faults are not applicable because a second free flow oxide is used prior to metallization.
4. Oxide gate bridge inspection is not applicable.
5. Semi-circular cracks not in an active area which start and end at the pellet edge area are acceptable.

Note 3. See Individual Data Sheets for Burn-In Circuits

Note 4. 40-Lead DIC Packages use 20,000 G centrifuge.

Non-Radiation Hardened CMOS LSI Devices

Index to the RCA High-Reliability Microprocessor, Memories and Peripherals Devices (Non-Radiation Hardened)

RCA PART NO.	CIRCUIT FUNCTION	DATA FILE NO.
CDM5114CD/3	4K Static RAM 1024-Word by 4-Bit	1716
CDM5332CD/3	32K Static ROM 4096-Word by 8-Bit	1965
CDM6116ACD/3	16K Static RAM 2048-Word by 8-Bit	1688
CDM6116BCD/3	16K Static RAM (Small Chip Version) 2048-Word by 8-Bit	2083
CDM6264CD/3	64K Static RAM 8192-Word by 8-Bit	1709
CDM6264ACD/3	64K Static RAM 8192-Word by 8-Bit	1837
CDM6264ACJ/3	64K Static RAM 8192-Word by 8-Bit	1837
CDM6264BCD/3	64K Static RAM 8192-Word by 8-Bit	1930
CDM6264BCJ/3	64 Static RAM 8192-Word by 8-Bit	1930
CDM62256CD/3	256K Static RAM 32,768-Word by 8-Bit	1931
CDM62256CJ/3	256K Static RAM 32,768-Word by 8-Bit	1931
CDP1802ACD/3	8-Bit Microprocessor	1441
CDP1802AD/3	8-Bit Microprocessor	1441
CDP1821CD/3	1K Static Ram 1024-Word by 11-Bit	1329
CDP1822CD/3	1K Static RAM 256-Word by 4-Bit	1330
CDP1823CD/3	1K Static RAM 128-Word by 8-Bit	1334
CDP1824CD/3	0.256K Static RAM 32-Word by 8-Bit	1717
CDP1824D/3	0.256K Static RAM 32-Word by 8-Bit	1717
CDP1831CD/3	4K Static ROM 512-Word by 8-Bit CDP1802 Compatable	—
CDP1831D/3	4K Static ROM 512-Word by 8-Bit CDP1802 Compatable	—
CDP1832CD/3	4K Static ROM 512-Word by 8-Bit 2704 Replacement	1712
CDP1832D/3	4K Static ROM 512-Word by 8-Bit 2704 Replacement	1712
CDP1833CD/3	8K Static ROM 1024-Word by 8-Bit CDP1802 Compatable	—
CDP1833D/3	8K Static ROM 1024-Word by 8-Bit CDP1802 Compatable	—
CDP1834CD/3	8K Static ROM 1024-Word by 8-Bit 2708 Replacement	1714
CDP1834D/3	8K Static ROM 1024-Word by 8-Bit 2708 Replacement	1714
CDP1852CD/3	Byte-Wide Input/ Output Port Mode Programmable	1694
CDP1852D/3	Byte-Wide Input/ Output Port Mode Programmable	1694
CDP1853CD/3	N-Bit 1 of 8 Decoders	1713
CDP1853D/3	N-Bit 1 of 8 Decoders	1713
CDP1854ACD/3	Programmable Universal Asynchronous Receiver/ Transmitter (UART)	1715
CDP1854AD/3	Programmable Universal Asynchronous Receiver/ Transmitter (UART)	1715

Data for these devices is available in the High-Reliability DATABOOK SSD-230 or from their respective data sheets.

Radiation-Hardened CMOS/SOS RAMs

RCA rad-hard memories use CMOS/SOS technology and are designed for use in memory systems where low power and simplicity in use are desired. The CMM5114 and CMM5104 have TTL compatibility on all I/O terminals. The CMM6167 is CMOS compatible.

Radiation Features

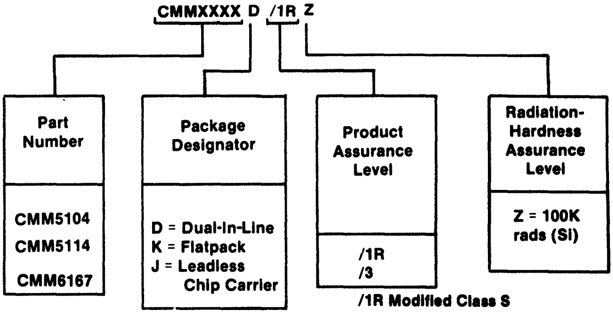
CMOS/SOS technology permits operation in high-radiation environments. It is insensitive to neutrons, cannot latch up at any dose rate and is resistant to single-event upset caused by cosmic rays or heavy ions.

Radiation Tolerance for the Rad-Hard CMOS/SOS Memories

Total Dose	≥ 1 x 10^5 Rads (Si)
* Latch-Up	Not Possible
* Transient Upset	≥ 1 x 10^{10} Rads (Si)/sec
* Transient Survival	≥ 1 x 10^{12} Rads (Si)/sec
Single-Event-Upset (SEU)	< 10^{-9} Errors/Bit/day (typically)

* Inherent property of SOS.

Guide to the Part Number, Package Designator, and Product Assurance Level of High-Reliability CMM5104/CMM5114/CMM6167 Series.



/1R Modified Class S
/3 Modified Class B

The /1RZ devices are ideal for aerospace applications. The /3 devices are suitable for non-critical radiation requirements.

Index to Rad-Hard CMOS/SOS RAMs

DEVICE	DESCRIPTION	PACKAGE (24 TERMINAL)	DATA FILE NO.
CMM5104/1RZ	4096-Word x 1-Bit Static RAM	DIC Flat Pack LCC	1456
CMM5114/1RZ	1024-Word x 4-Bit Static RAM	DIC Flat Pack LCC	1465
CMM5114A/1RZ	1024-Word x 4-Bit Static RAM (Gated Address)	DIC Flat Pack LCC	2081
CMM6167/1RZ	16,384-Word x 1-Bit Static RAM	Flat Pack	1831
CMM5114A/3	1024-Word x 4-Bit Static RAM (Gated Address)	DIC Flat Pack LCC	2082

Data for these devices is available in the High-Reliability DATABOOK, SSD-230B or from their respective data sheets.

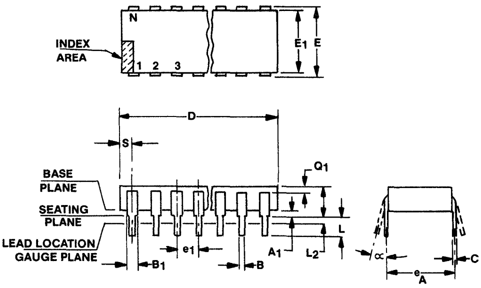
Dimensional Outlines

8

Dual-In-Line Packages

Dual-In-Line Side-Brazed Ceramic Packages

D SUFFIX



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5 1982.
3. Leads within .13mm (.005 in.) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
4. e_1 and e_A applies in zone L_2 when unit installed.
5. α applies to spread leads prior to installation.
6. N is the number of terminal positions.
7. Outlines on which the seating plane is coincident with the base plane (A_1 = O), terminals lead standoffs are not required, and B_1 may equal B along any part of the lead above the seating/base plane.
8. E_1 does not include particles of package materials.
9. This dimension shall be measured with the device seated in the seating plane gauge JEDEC Outline No. GS-3.
10. Controlling Dimension: INCH.

(D) Suffix (JEDEC MO-036-AD)
16-Lead Dual-In-Line
Side-Brazed Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.105	.175	2.67	4.44	9
A_1	.025	.055	.64	1.39	9
B	.015	.021	.381	.533	
B_1	.038	.060	.97	1.52	
C	.008	.012	.204	.304	
D	.770	.830	19.56	21.08	
E	.290	.325	7.37	8.25	
E_1	.280	.310	7.12	7.87	8
e_1	.100 TP		2.54 TP		3, 4
e_A	.300 TP		7.62 TP		3, 4
L	.125	.175	3.18	4.44	
L_2	.000	.030	.00	.76	
α	0°	15°	0°	15°	5
N	16		16		6
Q_1	.010	—	.25	—	
S	.020	.065	.51	1.65	

92CS-42880

(D) Suffix (JEDEC MO-036-AE)
18-Lead Dual-In-Line
Side-Brazed Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.105	.175	2.67	4.44	9
A_1	.025	.055	.64	1.39	9
B	.015	.021	.381	.533	
B_1	.038	.060	.97	1.52	
C	.008	.012	.204	.304	
D	.880	.930	22.36	23.62	
E	.290	.325	7.37	8.25	
E_1	.280	.310	7.12	7.87	8
e_1	.100 TP		2.54 TP		3, 4
e_A	.300 TP		7.62 TP		3, 4
L	.125	.175	3.18	4.44	9
L_2	.000	.030	.00	.76	
α	0°	15°	0°	15°	5
N	18		18		6
Q_1	.010	—	.25	—	
S	.030	.065	.77	1.65	

92CS-42881

(D) Suffix (JEDEC MO-037-AA)
22-Lead Dual-In-Line
Side-Brazed Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.090	.175	2.29	4.44	9
A_1	.025	.055	.64	1.39	9
B	.015	.023	.381	.584	
B_1	.038	.060	.97	1.52	
C	.008	.012	.204	.304	
D	1.040	1.120	26.42	28.44	
E	.395	.420	10.04	10.66	
E_1	.380	.410	9.66	10.41	8
e_1	.100 TP		2.54 TP		3, 4
e_A	.400 TP		10.16 TP		3, 4
L	.125	.175	3.18	4.44	9
L_2	.000	.030	.00	.76	
α	0°	15°	0°	15°	
N	22		22		
Q_1	.010	—	.25	—	
S	.035	.065	.89	1.65	

92CS-42882

(D) Suffix (JEDEC MO-038-AA)
24-Lead Dual-In-Line
Side-Brazed Ceramic Package

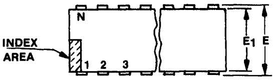
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.085	.190	2.2	4.8	9
A_1	.020	.070	.51	1.77	9
B	.015	.023	.381	.584	
B_1	.038	.060	.97	1.52	
C	.008	.012	.204	.304	
D	1.180	1.220	29.88	30.98	
E	.595	.625	15.12	15.87	
E_1	.575	.610	14.61	15.49	8
e_1	.100 TP		2.54 TP		3, 4
e_A	.600 TP		15.24 TP		3, 4
L	.125	.175	3.18	4.44	9
L_2	.000	.030	.00	.76	
α	0°	15°	0°	15°	
N	24		24		
Q_1	.010	—	.25	—	
S	.030	.065	.77	1.65	

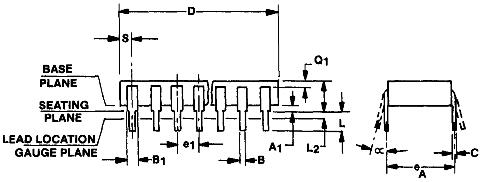
92CS-42883

Dual-In-Line Packages

Dual-In-Line Side-Brazed Ceramic Packages

D SUFFIX





NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5 1982.
3. Leads within .13mm (.005 in.) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
4. e_1 and e_A applies in zone L_2 when unit installed.
5. ∝ applies to spread leads prior to installation.
6. N is the number of terminal positions.
7. Outlines on which the seating plane is coincident with the base plane A_1 = O), terminals lead standoffs are not required, and B_1 may equal B along any part of the lead above the seating/base plane.
8. E_1 does not include particles of package materials.
9. This dimension shall be measured with the device seated in the seating plane gauge JEDEC Outline No. GS-3.
10. Controlling Dimension: INCH.

(D) Suffix (JEDEC MO-038-AB) 28-Lead Dual-In-Line Side-Brazed Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.085	.190	2.2	4.8	9
A_1	.020	.070	.51	1.77	9
B	.015	.023	.381	.584	
B_1	.038	.060	.97	1.52	
C	.008	.012	.204	.304	
D	1.380	1.430	35.06	36.22	
E	.595	.625	15.12	15.87	
E_1	0.580	.610	14.74	15.49	8
e_1	.100 TP		2.54 TP		3, 4
e_A	.600 TP		15.24 TP		3, 4
L	.125	.175	3.18	4.44	9
L_2	.000	.030	.00	.76	
∝	0°	15°	0°	15°	
N	28		28		
Q_1	.010	—	.25	—	
S	.030	.065	.77	1.65	

92CS-42884

(D) Suffix (JEDEC MO-038-AC) 40-Lead Dual-In-Line Side-Brazed Ceramic Package

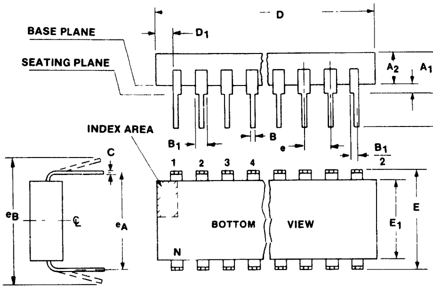
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.085	.190	2.2	4.8	9
A_1	.020	.070	.51	1.77	9
B	.015	.023	.381	.584	
B_1	.038	.060	.97	1.52	
C	.008	.012	.204	.304	
D	1.980	2.030	50.30	51.56	
E	.595	.625	15.12	15.87	
E_1	.580	.610	14.74	15.49	8
e_1	.100 TP		2.54 TP		3, 4
e_A	.600 TP		15.24 TP		3, 4
L	.125	.175	3.18	4.44	9
L_2	.000	.030	.00	.76	
∝	0°	15°	0°	15°	
N	40		40		
Q_1	.010	—	.25	—	
S	.030	.065	.77	1.65	

92CS-42885

Dual-In-Line Packages

Dual-In-Line Plastic Packages

E SUFFIX



(E) Suffix (JEDEC MS-001-AB)
8-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.348	0.430	8.84	10.92	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	8		8		11

92CS-39998

(E) Suffix (JEDEC MS-001-AC)
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

92CS-39901

(E) Suffix (JEDEC MS-001-AA)
16-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

92CS-39900

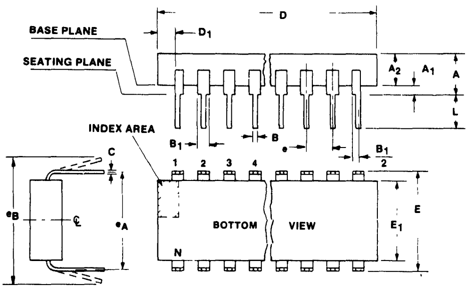
Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions $1, N, \frac{N}{2}, \frac{N}{2}+1$.
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm)
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

Dual-In-Line Packages

Dual-In-Line Plastic Packages

E SUFFIX



(E) Suffix (JEDEC MS-001-AD)
18-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.845	0.925	21.47	23.49	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	18		18		11

92CS-39996

(E) Suffix (JEDEC MS-001-AE)
20-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.5	26.9	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	20		20		11

92CS-39997

(E) Suffix (JEDEC MS-001-AF)
24-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

92CS-39943

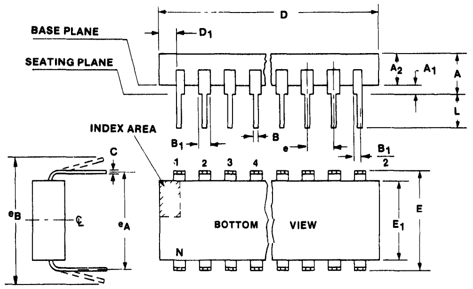
Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions $1, N, \frac{N}{2}, \frac{N}{2}+1$.
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

Dual-In-Line Packages

Dual-In-Line Plastic Packages

E SUFFIX



(E) Suffix (JEDEC MS-010-AA)
22-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.125	0.195	3.18	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.050	1.120	26.67	28.44	4
D_1	0.005	—	0.13	—	12
E	0.390	0.425	9.91	10.79	5
E_1	0.330	0.380	8.39	9.65	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.400 BSC		10.16 BSC		9
e_B	—	0.500	—	12.70	10
L	0.115	0.160	2.93	4.06	9
N	22		22		11

92CS-39999

(E) Suffix (JEDEC MS-011-AA)
24-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.250	—	6.35	9
A_1	0.015	—	0.39	—	9
A_2	0.125	0.195	3.18	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.150	1.290	29.3	32.7	4
D_1	0.005	—	0.13	—	12
E	0.600	0.625	15.24	15.87	5
E_1	0.485	0.580	12.32	14.73	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.600 BSC		15.24 BSC		9
e_B	—	0.700	—	17.78	10
L	0.115	0.200	2.93	5.08	9
N	24		24		11

92CS-40000

(E) Suffix (JEDEC MS-011-AB)
28-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.250	—	6.35	9
A_1	0.015	—	0.39	—	9
A_2	0.125	0.195	3.18	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.380	1.565	35.1	39.7	4
D_1	0.005	—	0.13	—	12
E	0.600	0.625	15.24	15.87	5
E_1	0.485	0.580	12.32	14.73	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.600 BSC		15.24 BSC		9
e_B	—	0.700	—	17.78	10
L	0.115	0.200	2.93	5.08	9
N	28		28		11

92CS-40001

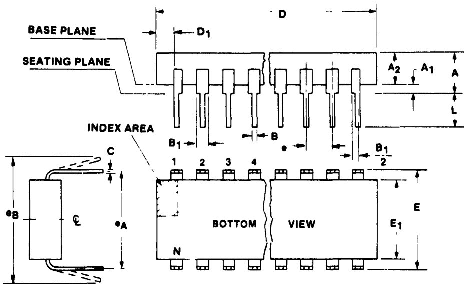
Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

Dual-In-Line Packages

Dual-In-Line Plastic Packages

E SUFFIX



(E) Suffix (JEDEC MS-011-AC)
40-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.250	—	6.35	9
A_1	0.015	—	0.39	—	9
A_2	0.125	0.195	3.18	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.980	2.095	50.3	53.2	4
D_1	0.005	—	0.13	—	12
E	0.600	0.625	15.24	15.87	5
E_1	0.485	0.580	12.32	14.73	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.600 BSC		15.24 BSC		9
e_B	—	0.700	—	17.78	10
L	0.115	0.200	2.93	5.08	9
N	40		40		11

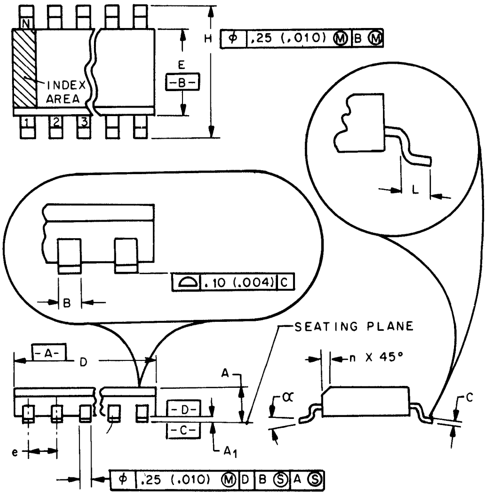
92CS-42886

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions $1, N, \frac{N}{2}, \frac{N}{2}+1$.
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

Small-Outline (SO) Plastic Packages

M SUFFIX



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "D" is a reference datum.
4. "A" and "B" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

(M) Suffix (JEDEC MS-013AA) 16-Lead Dual-In-Line Small-Outline Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0 0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.0200	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.3977	0.4133	10.10	10.50	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-39433R1

(M) Suffix (JEDEC MS-013AC) 20-Lead Dual-In-Line Small-Outline Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.0200	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.4961	0.5118	12.60	13.00	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38926R2

M Suffix (JEDEC MS-013AE) 28-Lead Dual-In-Line Small-Outline (SO) Package

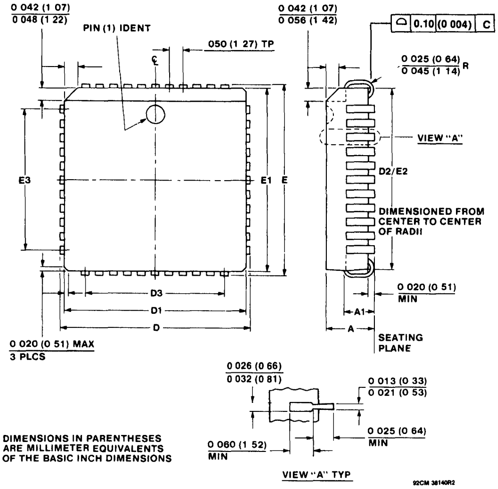
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.004	0.0118	0.1	0.3	
B	0.0138	0.02	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.6969	0.7125	17.7	18.1	4
E	0.2914	0.2992	7.4	7.6	4
e	0.05 BSC		1.27 BSC		
H	0.394	0.419	10.0	10.65	
h	0.01	0.029	0.25	0.75	5
L	0.016	0.05	0.4	1.27	6
N	28		28		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-39434R1

Plastic Chip-Carrier Packages

Q SUFFIX



NOTES:

1. **To be determined at seating plane.**
2. **Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.254 mm/0.010 in.**
3. **"N" is the number of terminal positions.**
4. **Controlling dimensions: inch.**

(Q) SUFFIX (JEDEC MO-047AB)
28-Lead Plastic Chip-Carrier Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.165	0.180	4.20	4.57	
A_1	0.090	0.120	2.29	3.04	
D	0.485	0.495	12.32	12.57	
D_1	0.450	0.456	11.430	11.582	2
D_2	0.390	0.430	9.91	10.92	1
D_3	0.300 REF		7.62 BSC		
E	0.485	0.495	12.32	12.57	
E_1	0.450	0.456	11.430	11.582	2
E_2	0.390	0.430	9.91	10.92	1
E_3	0.300 REF		7.62 BSC		
N	28		28		3

92CM-39435

(Q) SUFFIX (JEDEC MO-047AC)
44-Lead Plastic Chip-Carrier Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.165	0.180	4.20	4.57	
A_1	0.090	0.120	2.29	3.04	
D	0.685	0.695	17.40	17.65	
D_1	0.650	0.656	16.510	16.662	2
D_2	0.590	0.630	14.99	16.00	1
D_3	0.500 REF		12.70 BSC		
E	0.685	0.695	17.40	17.65	
E_1	0.650	0.656	16.510	16.662	2
E_2	0.590	0.630	14.99	16.00	1
E_3	0.500 REF		12.70 BSC		
N	44		44		3

92CM-38140R1

Application Notes

Number	Title
ICAN-6315	COS/MOS Interfacing Simplified
ICAN-6416	An Introduction to Microprocessors and the RCA COSMAC COS/MOS Microprocessor
ICAN-6525	Guide to Better Handling and Operation of CMOS Integrated Circuits
ICAN-6536	Use of CMOS ROM'S CDP1831 and CDP1832 with the RCA Microprocessor Evaluation Kit CDP18S020
ICAN-6537	Use of CMOS RAM CDP1824 with Microprocessor Evaluation Kit CDP18S020
ICAN-6538	Use of the CDP1852 8-Bit I/O Port with RCA Microprocessor Evaluation Kit CDP18S020
ICAN-6539	Use of CMOS-SOS RAM CDP1822 with RCA Microprocessor Evaluation Kit CDP18S020
ICAN-6562	Register-Based Output Function for RCA COSMAC Microprocessors
ICAN-6565	Design of Clock Generators for Use with RCA COSMAC Microprocessor CDP1802
ICAN-6581	Power-on Reset/Run Circuits for the RCA CDP1802 COSMAC Microprocessor
ICAN-6595	Interfacing Analog and Digital Displays with CMOS Integrated Circuits
ICAN-6602	Interfacing COS/MOS with Other Logic Families
ICAN-6611	Keyboard Scan Routine for Use with RCA COSMAC Microterminal CDP18S021
ICAN-6632	Use of the CDP1854 UART with RCA Microprocessor Evaluation Kit CDP18S020 or EK/Assembler-Editor Design Kit CDP180S024
ICAN-6635	Use of CMOS ROM'S CDP1833 and CDP1834 with the RCA Microprocessor Evaluation Kit CDP18S020 and the EK/Assembler-Editor Design Kit CDP18S024
ICAN-6677	Software Control of Microprocessor-Based Realtime Clock
ICAN-6693	CDP1802-Based Designs Using the 8253 Programmable Counter/Timer
ICAN-6704	Optimizing Hardware/Software Trade-Offs RCA CDP1802 Microprocessor Applications
ICAN-6834	Microprocessor Control for Color-TV Receivers
ICAN-6842	16-Bit Operations in the CDP1802 Microprocessor
ICAN-6847	Programming 2732 PROM'S with the CDP18S480 PROM Programmer
ICAN-6901	CDP1802 Microprocessor-Based Setback Thermostat
ICAN-6907	A Counter/Timer for COSMAC Systems
ICAN-6918	A Methodology for Programming COSMAC 1802 Applications Using Higher-Level Languages
ICAN-6928	Interfacing PLM Code to CDOS System Functions
ICAN-6934	Cassette Tape I/O for COSMAC Microprocessor Systems
ICAN-6943	Designing Minimum Nonvolatile Memory Systems with CMOS Static RAMs
ICAN-6957	CDP1804 and CDP1805 Processors Improve System Performance and Lower Chip Count
ICAN-6968	New CMOS CDP1800-Series Processors Reduce Chip Count
ICAN-6970	Understanding and Using the CDP1855 Multiply/Divide Unit
ICAN-6971	New CMOS CDP1800-Series Processors Enhance System Performance
ICAN-6991	A Slave CDP1802 Serial Printer Buffer System
ICAN-7009	New CDP1805 Microprocessor Upgrades CDP1800-Based Systems
ICAN-7020	Multimicroprocessor-based Transistor Test Equipment
ICAN-7023	CDP1800-Series Peripherals - Building Blocks of a Complete Processor Family
ICAN-7029	Low-Power Techniques for Use with CMOS CDP1800-Based Systems
ICAN-7063	Understanding the CDP1851 Programmable I/O
ICAN-7079	CDP1800-Series Multiprocessing for Maximum Performance
ICAN-7116	New CMOS Counting Functions for Real-Time Applications
ICAN-7144	Real-Time Interrupts Using the CDP1804A/5A/6A CMOS Microprocessor
ICAN-7197	Keyless Entry System Using the CDP6805F2 8-Bit Microcomputer Unit
ICAN-7198	Bicycle Computer Using the CDP6805G2 Microcomputer
ICAN-7199	CDP6805 CMOS Family Emulator
ICAN-7200	Monitor for the CDP6805G2 Microcomputer
ICAN-7201	CBUG05 Debug Monitor Program for the CDP6805E2 Microprocessor Unit
ICAN-7264	Versatile Serial Protocol for a Microcomputer-Peripheral Interface
ICAN-7275	User's Guide to the CDP1879 and CDP1879C1 CMOS Real-Time Clocks
ICAN-7364	CDP6805 MICROS Converting Interrupts
ICAN-7374	The CDP1871A Keyboard Encoder
ICAN-8601	CDP68HC05C4 Monitor and Real-Time Controller
ICAN-8633	Versatile Serial Peripheral Interface
ICAN-8723	Interfacing Serial EEPROMS to CDP6805 Microcomputers

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