Rockwell

PARALLEL PROCESSING SYSTEM (PPS)
DATA SHEET

PPS-4/2 CENTRAL PROCESSOR UNIT (CPU)

DESCRIPTION

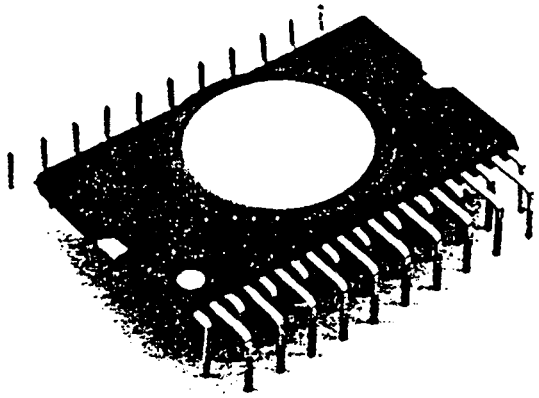
Rockwell introduces two new microcomputer circuit devices which provide a flexible system for cost sensitive applications. The two circuits comprise a CPU chip (P/N 11660 described in this data sheet) and a combination Memory and I/O chip (P/N A17XX described in data sheet Number 29000 D28). These chips may be used as a complete two chip microprocessor or with other Rockwell circuits of the PPS-4 family to provide a broad spectrum of system functions at lower costs than previously attainable.

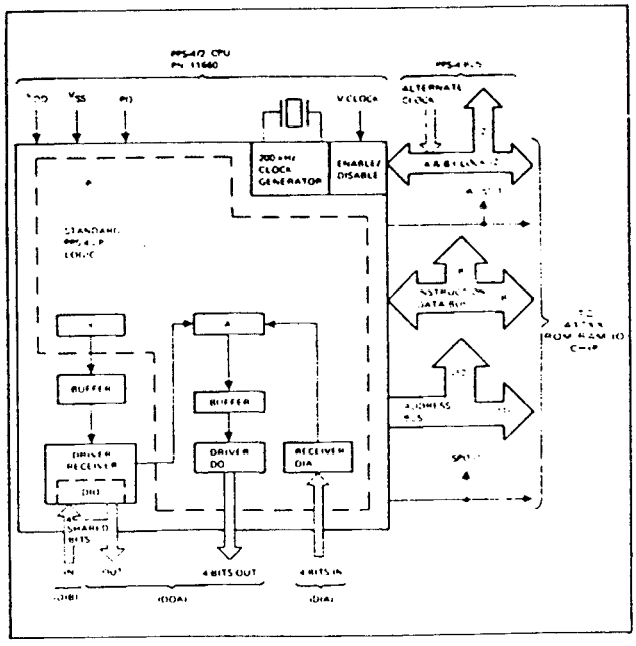
The PPS-4/2 System has been designed to provide a basic two circuit microcomputer which is optimized for applications requiring low cost and high performance. The two circuits provide all the computing power and applications flexibility which would require five or more of the conventional PPS-4 circuits to implement. The PPS-4/2 may be expanded to more complex applications by using any of the large family of PPS-4 circuits so that the cost of more complex systems may be reduced.

The PPS-4/2 CPU uses an identical instruction set as the PPS-4 CPU but includes the clock generator function within the CPU circuit as well. When a conventional NTSC color TV crystal (3.579545 MHz) is connected to the XTAL 1 and XTAL 0 pins and the VCLOCK pin is connected to VDD, the CPU circuit will generate the 198.864 kHz system clock signals. These signals, A and $\overline{B}$, are used internally in the CPU and are made available to all of the PPS-4/2 and PPS-4 circuits in the system.

An additional feature in the PPS-4/2 CPU is an expanded discrete output capability. This capability is achieved by using the same instruction (DOA) as in the PPS-4 CPU but providing more I/O control. In the PPS-4 the DOA instruction causes the contents of the accumulator (A) to be transferred to an output buffer and then retained until another DOA instruction is executed. The contents of this buffer controls the output drivers. In the PPS-4/2 CPU this same function is performed but, additionally, the contents of the X register are transferred to a similar second set of buffers and drivers (DIO) so that the DOA instruction causes 8 bits to be available to external devices. The current drive capability of all outputs are approximately twice that of the PPS-4 CPU discretes.

The PPS-4/2 CPU automatically floats all output lines when power is turned on. Functionally there are no other differences between the PPS-4 and the PPS-4/2 CPU's. However, the PPS-4/2 CPU also has the capability of directly driving low-power LED display segments. Fluorescent displays can also be driven if the system includes the appropriate power supply for the higher voltage display.





PPS-4/2 CPU Simplified Block Diagram

FEATURES

- Self-contained Clock
- PPS-4 Instruction Set
- Expanded I/O Using Discrete I/O Commands
- Direct LED Segment or Fluorescent Display Compatibility
- PPS-4 Bus System Compatibility
- 5 Microsecond Cycle Time
- 100 pf Bus Drive Capability

Specifications subject to change without notice
Revision 1, March 1976

W

Supply Voltage:

VDD = -17 Volts ±5%
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)

VSS = 0 Volts (Gnd.)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequency:

199 kHz

Device Power Consumption:

600 mw

Input Capacitance:

<5 pf

Input Leakage:

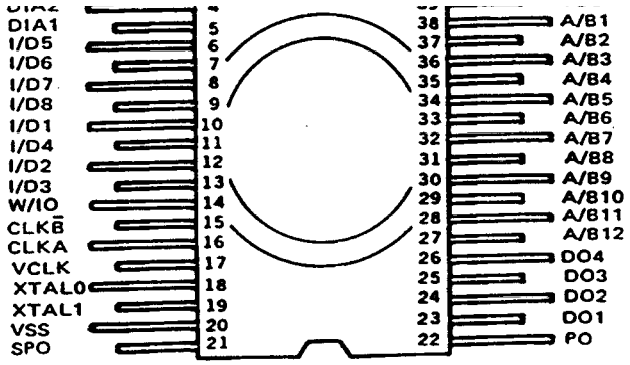
<10 ua

Operating Temperature (TA):

0°C to 70°C. (TA = 25°C unless otherwise specified.)

Storage Temperature:

-55°C to 120°C.



PPS-4/2 CPU Pin Configurations

ABSOLUTE MAXIMUM RATINGS

Supply Voltage

|VDD-VSS| = 27 volts maximum.

Input Voltage with respect to VSS
-27 volts maximum.

Maximum positive voltage on any pin +0.3 volts.

FUNCTION		SYMBOL	LIMITS (VSS = 0V) MIN	TYP	MAX	LIMITS (VSS = +5V) MIN	TYP	MAX	UNIT	TEST CONDITIONS
Supply Current (Average)		I_{DD}		26	35		26	35	mA	VDD = -17.85V VSS = 0V F = 256 kHz T_A = 25°C
Input and Output Characteristics — System Bus										VDD = -17V ±5% VSS = 0V
I/D_{5-8}	I/D_{1-4}	V_{IH} V_{IL}	-1.5 -6.5		+0.3 -17.85	+3.5 -1.5		+5.3 -12.85	V V	
	A/B_{1-12} W/IO	V_{OH} V_{OL}	-1.0 -7.5		+0.3 -17.85	+4.0 -2.5		+5.3 -12.85	V V	
SPO		V_{OH} V_{OL}	-0.5 -8.5		+0.3 -17.85	+4.5 -3.5		+5.3 -12.85	V V	
CLKA	when VCLK = VSS	V_{IH} V_{IL}	-0.5		+0.3	+4.5		+5.3	V	
$CLK\overline{B}$	when VCLK = VDD	V_{OH} V_{OL}	-10.0		-17.85	-5.0		-12.85	V	OR
Input and Output Characteristics — External Interface										
DIO_{1-4}	DIA_{1-4}	V_{IH} V_{IL}	-2.5 -7.0		+0.3 -17.85	+2.5 -2.0		+5.3 -12.85	V V	
	DO_{1-4}	V_{OH} V_{OL}	NOTE 1 floating (≥5M)			NOTE 1 floating (≥5M)			Ω	
PO		V_{IH} V_{IL}	-2.5 -12.0		+0.3 -17.85	+2.5 -8.0		+5.3 -12.85	V V	VDD = -12V ±5% VSS = +5V ±5%
XTAL0, XTAL1		W_{EXCIT}	9		11	9		11	mW	

NOTE: 1. Output driven to VSS with maximum "ON" resistance (RON_{MAX}) of 1.0K ohms and maximum drive current (I_{MAX}) of 2.7 ma.

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