Rockwell

R6500 Microcomputer System APPLICATION NOTE

Using R65XX Family Peripheral Devices With The Z80 CPU

INTRODUCTION

Many microprocessor system designs using the Z80 Central Processor Unit could be greatly improved by using the Rockwell R65XX series peripheral devices. Members of this family – such as the R6522 Versatile Interface Adapter, the R6545 CRT Controller, the R6520 Peripheral Interface Adapter, and the R6551 ACIA – may prove to be both cost-effective and versatile in Z80 based designs. This application note presents one possible approach to the interfacing of the Z80 bus to the R65XX, which will allow the system designer greater freedom to select the best possible compliment of I/O designs for use in a Z80 system.

TIMING DIFFERENCES

Some basic timing differences exist between the Z80 and the R65XX bus.

Z80 Timing

The Z80 I/O cycle timing diagrams are shown in Figure 1. Note that all data transfers are controlled by the Ø0 clock. A Z80 I/O cycle has four clock periods. During the first clock period, T1, the Port address is placed on the Address Bus and, for a write cycle, the processor places the output data on the Data Bus. During T2, the $\overline{IORQ}$ line is asserted, to indicate an I/O cycle is occurring, and either the $\overline{RD}$ or $\overline{WR}$ line is taken low, to indicate an input or output, respectively. The processor then automatically inserts a WAIT state, Tw. An additional WAIT cycle may be externally inserted by taking the $\overline{WAIT}$ line low during Tw. In this case, the next cycle will also be a WAIT state. During the final period, T3, the data is latched into the processor on a read cycle and $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ are released.

R65XX Timing

Figure 2 shows the R65XX timing diagram. All data transfers take place during a single cycle of the phase-two (Ø2) clock. During the first half of the cycle (Ø2 low), the address of the memory or peripheral is placed on the Address Bus and the R/$\overline{W}$ line is asserted. On the rising edge of Ø2, the address and R/$\overline{W}$ status are latched into the R65XX peripheral device. Then, during the Ø2 high period, the data is placed on the data bus by either the CPU or the peripheral, depending on the state of the R/$\overline{W}$ line. The data is latched on the falling edge of the Ø2 clock.

INTERFACE TIMING

Figure 3 shows the necessary timing relationships between the Z80 CPU and the R65XX peripheral series. It should be noted that the Ø2 clock is derived from the Z80 Ø0 clock by a divide-by-two function. In order to operate correctly, the Ø2 clock must be low at the start of a Z80 I/O cycle. The Z80 processor, however, does not always execute an even number of Ø0 cycles between I/O cycles. This may result in the generated Ø2 being out of phase by one-half of a cycle at the beginning of a Z80 I/O cycle. Figure 4 shows the relationships when Ø2 is high at the beginning of a Z80 I/O cycle. It is necessary to insert an additional WAIT state into the Z80 I/O cycle in order to delay the Z80 data transfer until Ø2 has the proper relationship.

The Circuit

Figure 5 shows a circuit which can be used to realize this interface. Note that this circuit can be built with only four Low Power Shottky TTL packages. The Z80 Ø0 clock is divided by two by the 74LS73. This output is then used as the Ø2 clock by the R65XX peripheral. It is also compared with Ø0, $\overline{IORQ}$, and R65XX $\overline{SELECT}$, to determine if a WAIT state is necessary. A WAIT state is generated for one Ø0 cycle by the second half of the 74LS73. The $\overline{IORQ}$ is delayed by half of the 74LS74 and gated with the R65XX $\overline{SELECT}$ to form the $\overline{CS}$ input. The $\overline{WR}$ signal is synchronized with Ø2 and used as the R65XX R/$\overline{W}$ input.

It should be noted that the output driving the $\overline{WAIT}$ input may need to be buffered with an open-collector driver if other system devices are to generate Z80 wait states.

In order to maintain speed compatibility, a Z80 CPU operating at 2-MHz can be used with 1-MHz R65XX parts, and a 4-MHz Z80 requires the use of 2-MHz R65XXA series parts.

Specifications subject to change without notice
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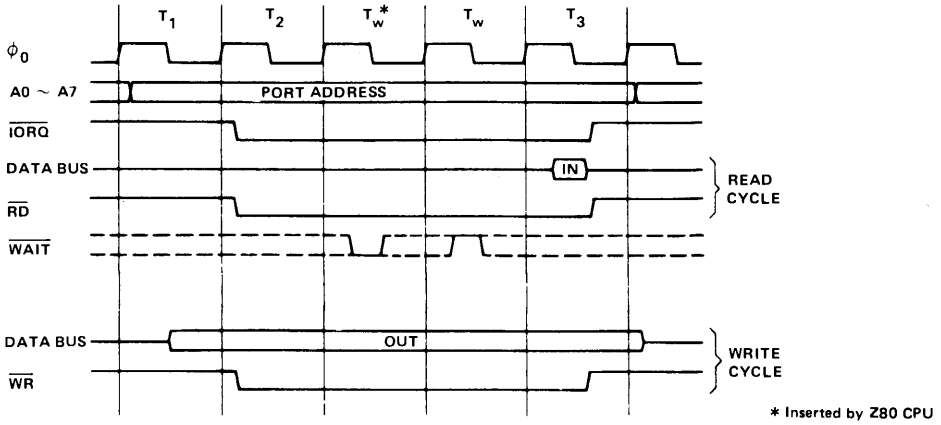
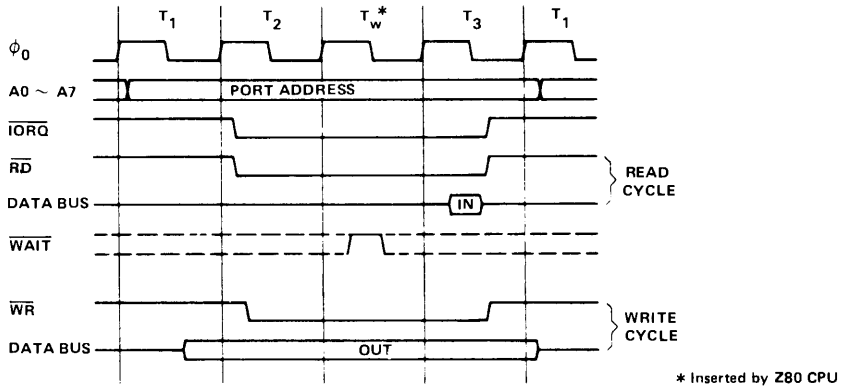
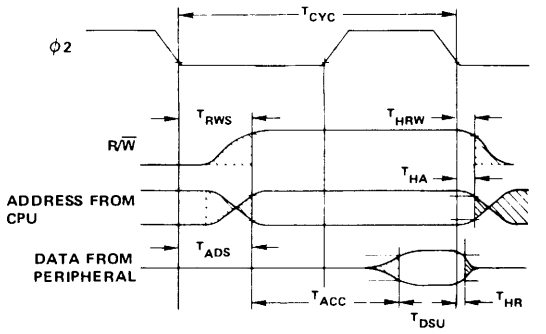


Input or Output Cycles With Wait States

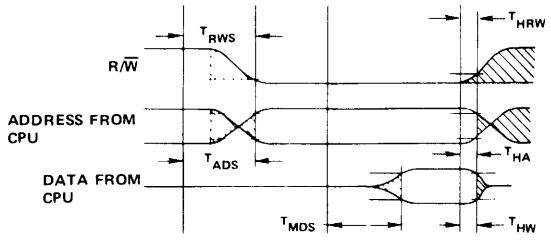


Input or Output Cycles

Figure 1. Z80 I/O Cycle Timing



Timing for Reading Data From External Memory



Timing for Writing Data to External Memory

Figure 2. R65XX I/O Cycle Timing

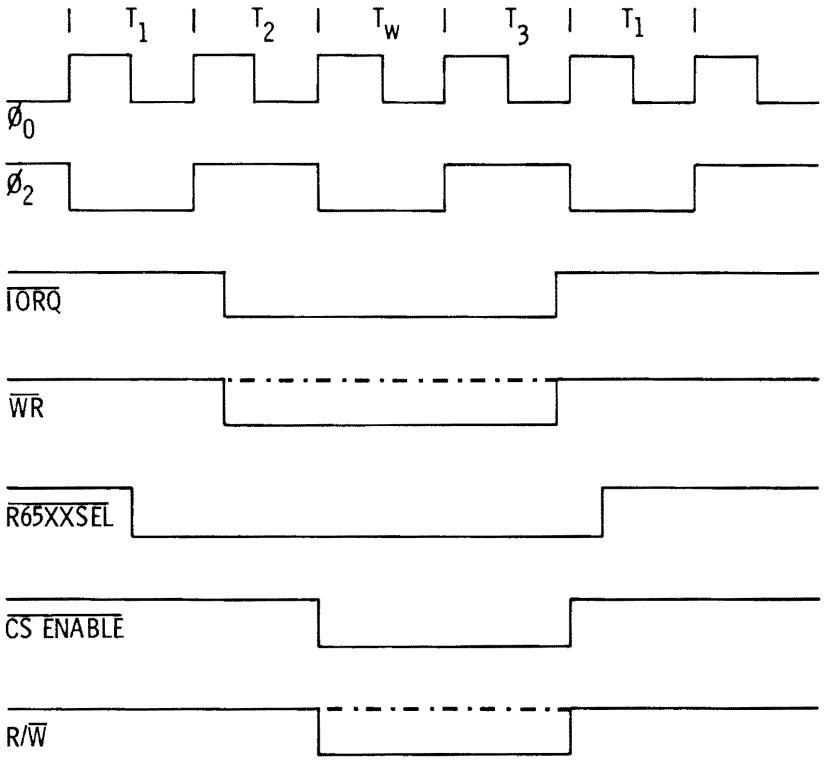


Figure 3. Z80 CPU to R65XX Interface Timing

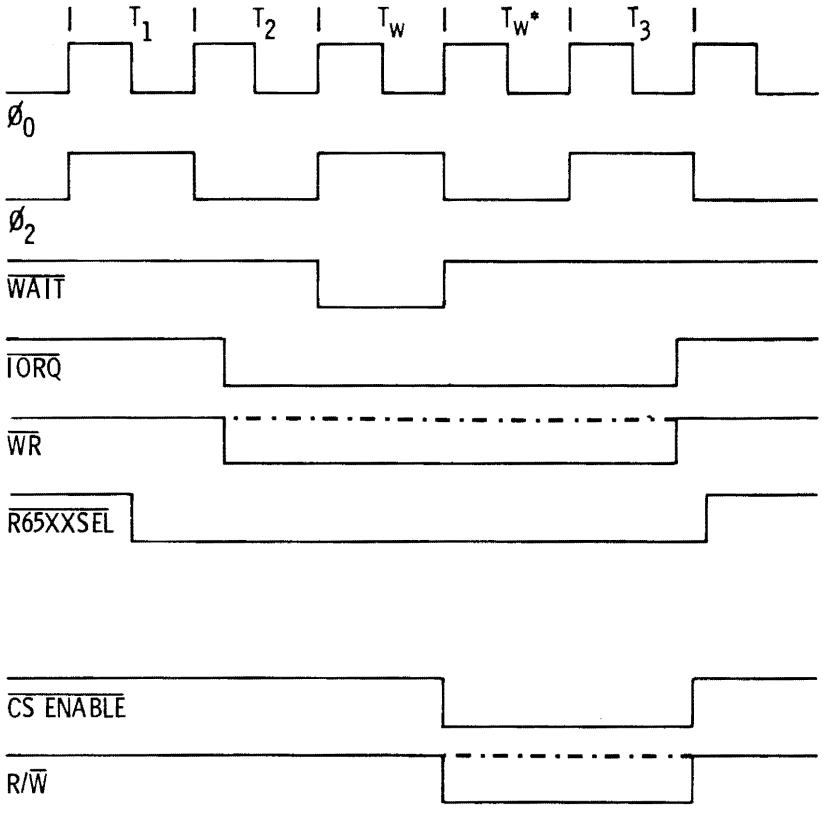


Figure 4. Z80 CPU to R65XX Interface Timing

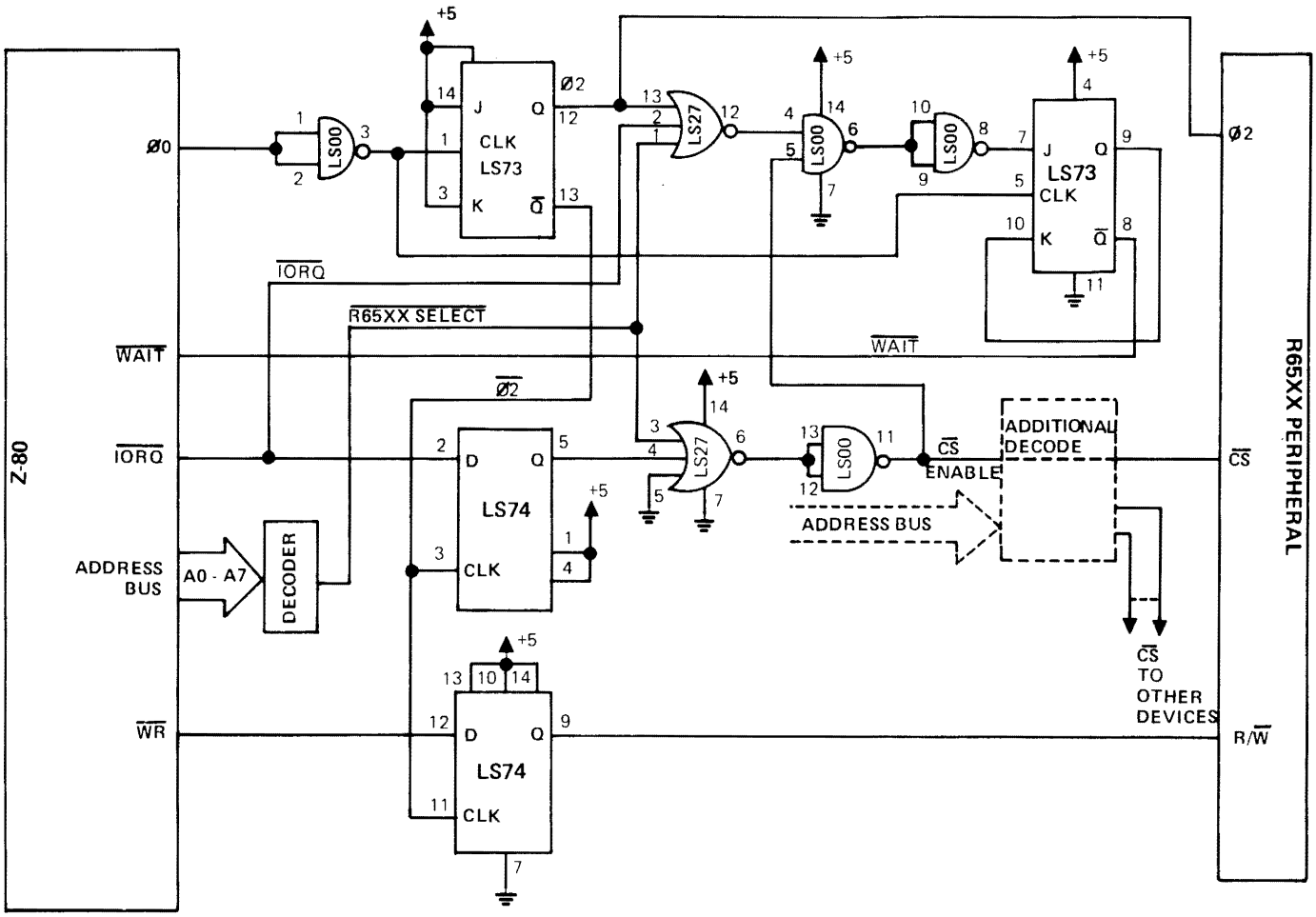


Figure 5. Z80 CPU to R65XX Peripheral Interface