1 PRODUCT OVERVIEW(PRELIMINARY)

INTRODUCTION

SAMSUNG's S3C2410X01 16/32-bit RISC microprocessor is designed to provide a cost-effective, low power, small die size and high performance micro-controller solution for hand-held devices and general applications. To reduce total system cost, S3C2410X01 also provides the following : separate 16KB Instruction and 16KB Data Cache, MMU to handle virtual memory management, LCD controller(STN & TFT), NAND Flash Boot loader, System Manager(chip select logic, SDRAM controller), 3-ch UART with handshake, 4-ch DMA, 4-ch Timers with PWM, I/O Ports, RTC, 8-ch 10-bit ADC and Touch screen interface, IIC-BUS interface, IIS-BUS interface, USB Host, USB Device, SD Host & Multi-Media Card Interface, 2-ch SPI and PLL for clock generation.

The S3C2410X01 was developed using an ARM920T core, 0.18um CMOS standard cells and a memory complier. Its low-power, simple , elegant and fully static design is particularly suitable for cost-sensitive and power sensitive applications. Also S3C2410X01 adopts a new bus architecture, AMBA (Advanced Microcontroller Bus Architecture)

An outstanding feature of the S3C2410X01 is its CPU core, a 16/32-bit ARM920T RISC processor designed by Advanced RISC Machines, Ltd. The ARM920T implements MMU, AMBA BUS, and Harvard cache architecture with separate 16KB instruction and 16KB data caches, each with a 8-word line length.

By providing complete set of common system peripherals, the S3C2410X01 minimizes overall system costs and eliminates the need to configure additional components. The integrated on-chip functions that are described in this document include:

- 1.8V int., 1.8V/2.5V/3.3V memory, 3.3V external I/O microprocessor with 16KB I-Cache/16KB D-Cache/MMU.
- External memory controller. (SDRAM Control, Chip Select logic)
- LCD controller (up to 4K color STN and 64K color TFT) with 1-ch LCD-dedicated DMA.
- 4-ch DMAs with external request pins
- 3-ch UART with handshake(IrDA1.0, 16-byte FIFO) / 2-ch SPI
- 1-ch multi-master IIC-BUS/1-ch IIS-BUS controller
- SD Host interface version 1.0 & Multi-Media Card Protocol version 2.11 compatible
- 2-port USB Host /1- port USB Device(ver 1.1)
- 4-ch PWM timers & 1-ch internal timer
- Watch Dog Timer
- 117-bit general purpose I/O ports / 24-ch external interrupt source
- Power control: Normal, Slow, Idle, Stop and Power-off mode
- 8-ch 10-bit ADC and Touch screen interface.
- RTC with calendar function.
- On-chip clock generator with PLL

FEATURES

Architecture

- Integrated system for hand-held devices and general embedded applications.
- 16/32-Bit RISC architecture and powerful instruction set with ARM920T CPU core.
- Enhanced ARM architecture MMU to support WinCE, EPOC 32 and Linux.
- Instruction cache, data cache, write buffer and Physical address TAG RAM to reduce the effect of main memory bandwidth and latency on performance.
- ARM920T CPU core supports the ARM debug architecture and has a Tracking ICE mode.
- Internal AMBA(Advanced Microcontroller Bus Architecture) (AMBA2.0, AHB/APB)

System Manager

- Little/Big Endian support.
- Address space : 128M byte for each bank(Total 1G-Byte)
- Supports programmable 8/16/32-bit data bus width for each bank.
- Fixed bank start address from 0 bank to 6 bank.
- Programmable bank start address and bank size for 7 bank.
- 8 memory banks.
  - 6 memory banks for ROM(NOR & NAND Flash), SRAM etc.
  - 2 memory banks for ROM(NOR & NAND Flash)/SRAM/Synchronous DRAM
- Fully Programmable access cycles for all memory banks.
- Supports external wait signal to expend the bus cycle.
- Supports self-refresh mode in SDRAM for power-down.

NAND Flash Boot Loader

- Support booting from NAND flash memory.
- 4KB internal buffer for booting

Cache Memory

- 64 way set-associative cache with I-Cache(16KB) and D-Cache(16KB).
- 8-words per line with one valid bit and two dirty bits per line
- Pseudo random or round robin replacement algorithm.
- Write through or write back cache operation to update the main memory.
- The write buffer can hold 16 words of data and four address.

Clock & Power Manager

- The on-chip MPLL and UPLL
  UPLL makes the clock for operating USB Host/Device.
  MPLL makes the clock for operating MCU at maximum 200Mhz @ 1.8V
- Clock can be fed selectively to each function block by software.
- Power mode: Normal, Slow, Idle, Stop mode and Power_off mode.
  Normal mode : Normal operating mode.
  Slow mode : Low frequency clock without PLL.
  Idle mode : Stop the clock for only CPU.
  Stop mode: All clocks are stopped.
  Power_off mode: The CORE power including all peripherals is shut down.
- Wake up by EINT[7:0] or RTC alarm interrupt from Stop mode.

Interrupt Controller

- 55 Interrupt sources
  (1 Watch dog timer, 5 Timer, 9 UART, 24 External interrupts, 4 DMA, 2 RTC, 2 ADC, 1 IIC, 2 SPI, 1 SDI, 2 USB, 1 LCD, 1 Battery Fault)
- Level/Edge mode on external interrupt source.
- Programmable polarity of edge and level.
- Supports FIQ (Fast Interrupt request) for very urgent interrupt request.

Timer with PWM (Pulse Width Modulation)

- 4-ch 16-bit Timer with PWM / 1-ch 16-bit internal timer with DMA-based or interrupt-based operation
- Programmable duty cycle, frequency, and polarity
- Dead-zone generation.
- Supports external clock source.

RTC (Real Time Clock)

- Full clock feature: msec, sec, min, hour, day, week, month, year.
- 32.768 KHz operation.
- Alarm interrupt.
- Time tick interrupt

General purpose input/output ports

- 24 external interrupt ports
- 93 multiplexed input/output ports

UART

- 3-channel UART with DMA-based or interrupt-based operation
- Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive
- Supports H/W handshaking during transmit/receive
- Programmable baud rate
- Supports IrDA 1.0
- Loop back mode for testing
- Each channel has internal 16-byte Tx FIFO and 16-byte Rx FIFO.

DMA Controller

- 4-ch DMA controller.
- Support memory to memory, IO to memory, memory to IO, IO to IO
- Burst transfer mode to enhance the transfer rate.

A/D Converter & Touch Screen Interface

- 8-ch multiplexed ADC.
- Max. 500KSPS and 10-bit Resolution.

LCD Controller

STN LCD displays Feature

- Supports 3 types of STN LCD panels ; 4-bit dual scan, 4-bit single scan, 8-bit single scan display type.
- Supports the monochrome, 4 gray levels, 16gray levels, 256 colors and 4096 colors for STN LCD.
- Supports multiple screen size

  Typical actual screen size : 800x600, 640x480, 320x240, 160x160 and etc

  Maximum virtual screen size(256 color mode) : 4096x1024, 2048x2048, 1024x4096 etc.

TFT(Thin Film Transistor) color displays Feature

- Supports 1, 2, 4 or 8 bpp (bit-per-pixel) palette color displays for color TFT.
- Supports 16 bpp non-palette true-color displays for color TFT.
- Supports maximum 32K(64K using intensity) color TFT at 16 bpp mode.
- Supports multiple screen size

  Typical actual screen size : 640x480, 320x240 and etc

  Recommended maximum screen size : 800x600 (8 bpp, 32bit SDRAM @80MHz)

  Maximum virtual screen size(16 bpp mode) : 2048x1024 etc

Watch-dog Timer

- 16-bit Watchdog Timer.
- Interrupt request or system reset at time-out.

IIC-BUS Interface

- 1-ch Multi-Master IIC-Bus.
- Serial, 8-bit oriented and bi-directional data transfers can be made at up to 100 Kbit/s in the standard mode or up to 400 Kbit/s in the fast mode.

IIS-BUS Interface

- 1-ch IIS-bus for audio interface with DMA-based operation.
- Serial, 8/16bit per channel data transfers.
- 128 Bytes(64-Byte + 64-Byte) FIFO for receive/transmit.
- Supports IIS format and MSB-justified data format.

USB Host

- 2-port USB Host
- Complies with OHCI Rev. 1.0
- Compatible with the USB Specification version 1.1

USB Device

- 1-port USB Device.
- 5 Endpoints for USB Device.
- Compatible with the USB Specification version 1.1

SD Host Interface

- SD Memory Card Protocol version 1.0 compatible
- SDIO Card Protocol version 1.0 compatible
- 64 Bytes FIFO for Tx/Rx
- DMA based or Interrupt based operation
- Multimedia Card Protocol version 2.11 compatible

SPI Interface

- 2-ch Serial Peripheral Interface Protocol version 2.11 compatible
- 2x8 bits Shift register for receive/transmit.
- DMA-based or interrupt-based operation.

Operating Voltage Range

- Core : 1.8V Memory : 1.8V / 2.5V / 3.3V I/O : 3.3V

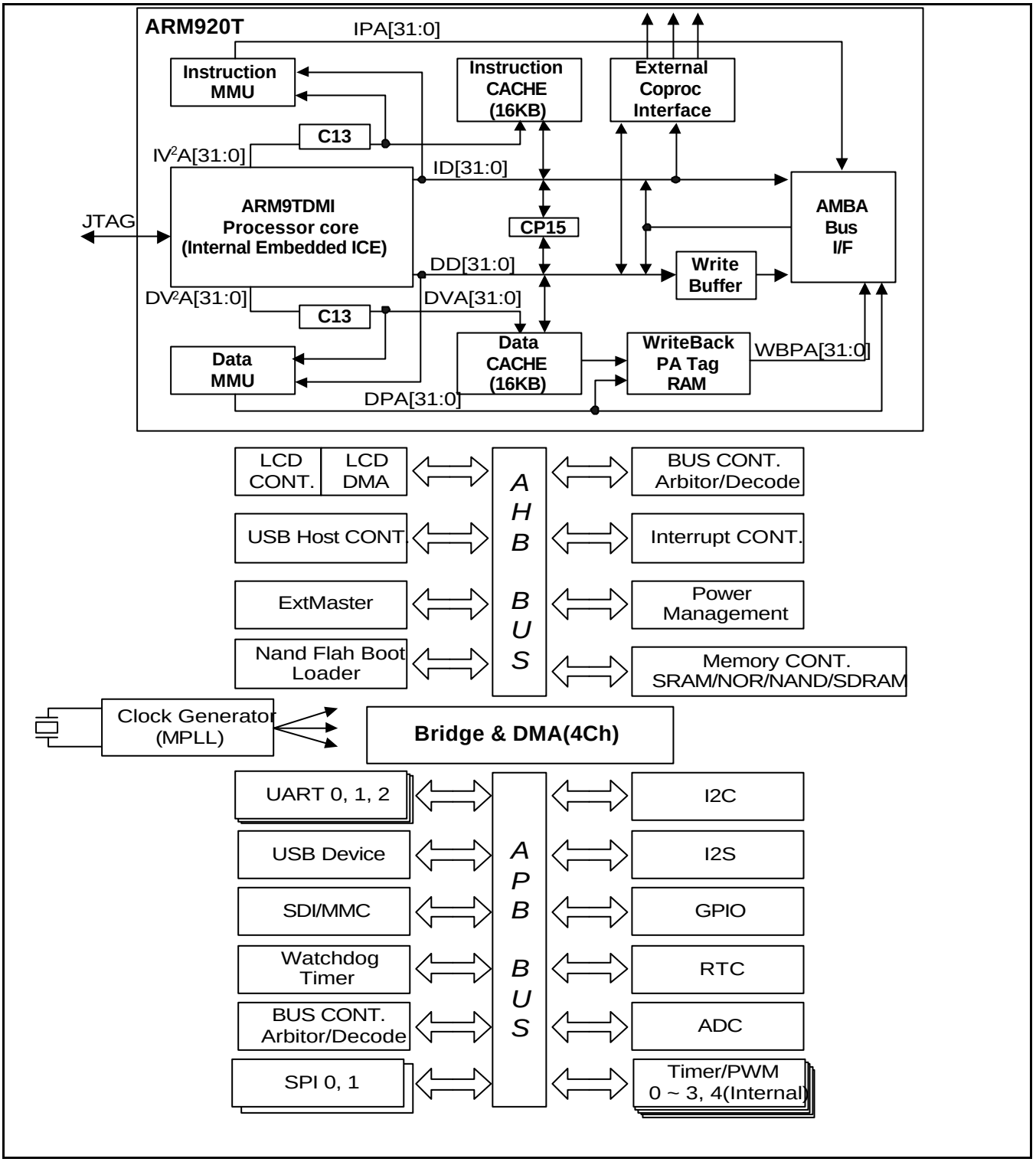
Operating Frequency

- Up to 200 Mhz

Package

- 272 FBGA

BLOCK DIAGRAM



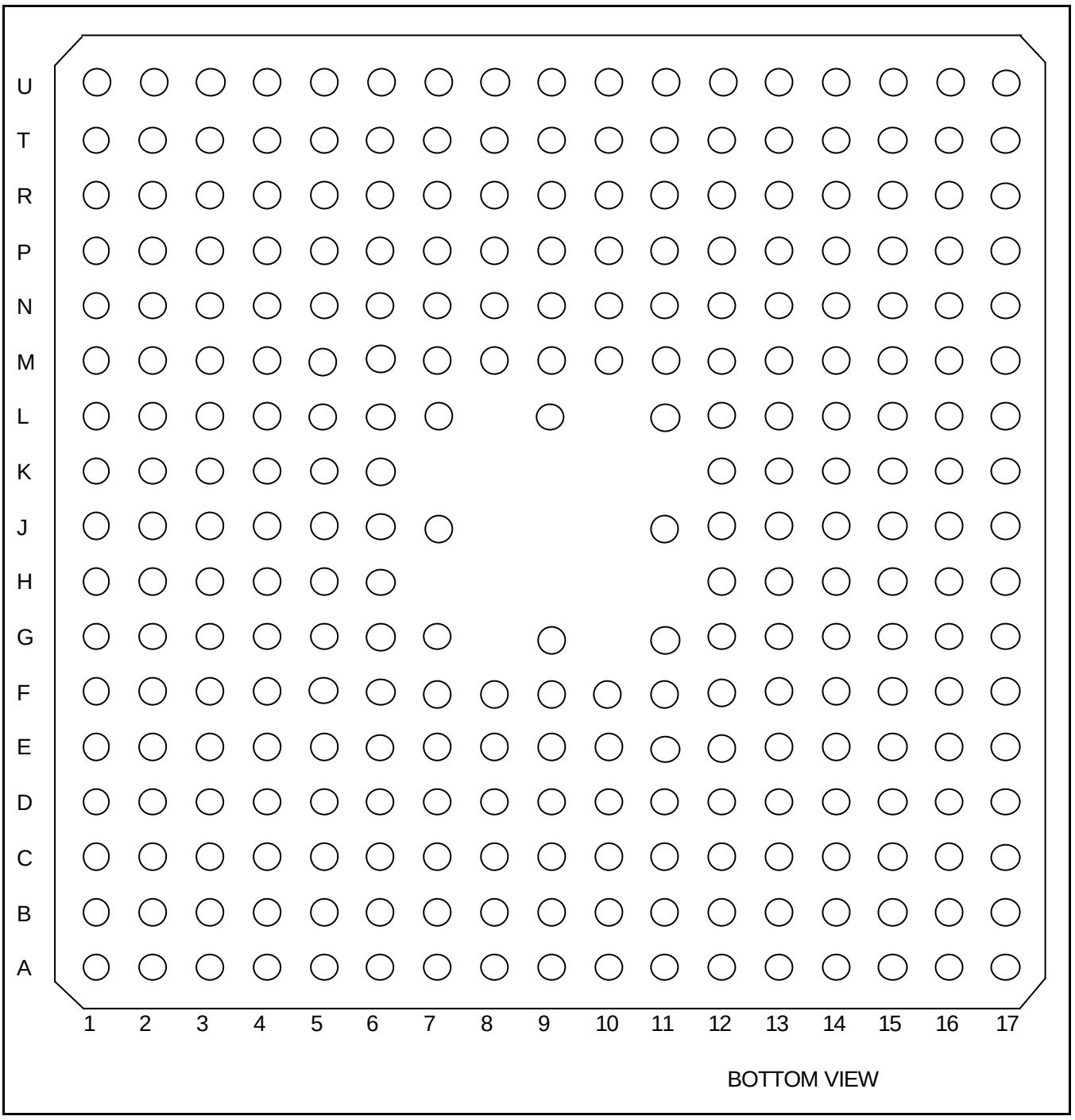


Figure 1-3. S3C2410X01 Pin Assignments (272 FBGA)

Table 1-1. 272-Pin LQFP Pin Assignment

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @STOP	I/O State @PWR_off	I/O State @nRESET	I/O Type
D4	DATA21	DATA21	Hi-z	Hi-z	Hi-z	I	u50
E5	DATA22	DATA22	Hi-z	Hi-z	Hi-z	I	u50
B1	DATA23	DATA23	Hi-z	Hi-z	Hi-z	I	u50
C2	VSSOP	VSSOP	P	P	P	P	s3o
C1	VDDMOP	VDDMOP	P	P	P	P	d3o
D3	DATA24	DATA24	Hi-z	Hi-z	Hi-z	I	u50
D2	DATA25	DATA25	Hi-z	Hi-z	Hi-z	I	u50
E3	DATA26	DATA26	Hi-z	Hi-z	Hi-z	I	u50
E4	DATA27	DATA27	Hi-z	Hi-z	Hi-z	I	u50
D1	DATA28	DATA28	Hi-z	Hi-z	Hi-z	I	u50
G6	DATA29	DATA29	Hi-z	Hi-z	Hi-z	I	u50
E2	DATA30	DATA30	Hi-z	Hi-z	Hi-z	I	u50
J7	DATA31	DATA31	Hi-z	Hi-z	Hi-z	I	u50
E1	VSSOP	VSSOP	P	P	P	P	s3o
F3	VSSOP	VSSOP	P	P	P	P	s3o
F4	TOUT0/GPB0	GPB0	–/–	–/–	O(L)/–	I	t8
F2	TOUT1/GPB1	GPB1	–/–	–/–	O(L)/–	I	t8
F5	TOUT2/GPB2	GPB2	–/–	–/–	O(L)/–	I	t8
F1	TOUT3/GPB3	GPB3	–/–	–/–	O(L)/–	I	t8
G2	TCLK0/GPB4	GPB4	–/–	–/–	–/–	I	t8
H6	nXBACK/GPB5	GPB5	–/–	–/–	–/–	O	t8
G4	nXBREQ/GPB6	GPB6	–/–	–/–	–/–	I	t8
H5	nXDACK1/GPB7	GPB7	–/–	–/–	–/–	O	t8
G3	VDDalive	VDDalive	P	P	P	P	d1i
J6	VDDiarm	VDDiarm	P	P	P	P	d1c
G5	VSSiarm	VSSiarm	P	P	P	P	s3i
J5	nXDREQ1/GPB8	GPB8	–/–	–/–	–/–	I	t8
G1	nXDACK0/GPB9	GPB9	–/–	–/–	–/–	O	t8
H4	nXDREQ0/GPB10	GPB10	–/–	–/–	–/–	I	t8
H2	nTRST	nTRST	I	I	I	I	is
H3	TCK	TCK	I	I	I	I	is
H1	TDI	TDI	I	I	I	I	is
J2	TMS	TMS	I	I	I	I	is

Table 1-1. 272-Pin LQFP Pin Assignment(Continued)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @STOP	I/O State @PWR_off	I/O State @nRESET	I/O Type
J4	TDO	TDO	O	O	O	O	is
K6	LEND/GPC0	GPC0	–/–	–/–	O(L)/–	I	t8
J3	VCLK/GPC1	GPC1	–/–	–/–	O(L)/–	I	t8
J1	VLINE/GPC2	GPC2	–/–	–/–	O(L)/–	I	t8
K4	VDDiarm	VDDiarm	P	P	P	P	d1c
K2	VSSiarm	VSSiarm	P	P	P	P	s3i
K1	VM/GPC4	GPC4	–/–	–/–	O(L)/–	I	t8
K3	VFRAME/GPC3	GPC3	–/–	–/–	O(L)/–	I	t8
L5	VDDOP	VDDOP	P	P	P	P	d3o
K5	VSSOP	VSSOP	P	P	P	P	s3o
L4	LCDVF0/GPC5	GPC5	–/–	–/–	O(L)/–	I	t8
L6	LCDVF1/GPC6	GPC6	–/–	–/–	O(L)/–	I	t8
L3	LCDVF2/GPC7	GPC7	–/–	–/–	O(L)/–	I	t8
L1	VD0/GPC8	GPC8	–/–	–/–	O(L)/–	I	t8
L2	VD1/GPC9	GPC9	–/–	–/–	O(L)/–	I	t8
M1	VD2/GPC10	GPC10	–/–	–/–	O(L)/–	I	t8
M2	VD3/GPC11	GPC11	–/–	–/–	O(L)/–	I	t8
M4	VDDiarm	VDDiarm	P	P	P	P	d1c
M5	VSSiarm	VSSiarm	P	P	P	P	s3i
N1	VD4/GPC12	GPC12	–/–	–/–	O(L)/–	I	t8
N2	VD5/GPC13	GPC13	–/–	–/–	O(L)/–	I	t8
M3	VD6/GPC14	GPC14	–/–	–/–	O(L)/–	I	t8
N4	VD7/GPC15	GPC15	–/–	–/–	O(L)/–	I	t8
N3	VD8/GPD0	GPD0	–/–	–/–	O(L)/–	I	t8
P1	VD9/GPD1	GPD1	–/–	–/–	O(L)/–	I	t8
L7	VD10/GPD2	GPD2	–/–	–/–	O(L)/–	I	t8
P3	VD11/GPD3	GPD3	–/–	–/–	O(L)/–	I	t8
P2	VD12/GPD4	GPD4	–/–	–/–	O(L)/–	I	t8
R2	VDDiarm	VDDiarm	P	P	P	P	d1c
R1	VSSiarm	VSSiarm	P	P	P	P	s3i
T2	VD13/GPD5	GPD5	–/–	–/–	O(L)/–	I	t8
R3	VD14/GPD6	GPD6	–/–	–/–	O(L)/–	I	t8
T1	VD15/GPD7	GPD7	–/–	–/–	O(L)/–	I	t8

Table 1-1. 272-Pin LQFP Pin Assignment(Continued)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @STOP	I/O State @PWR_off	I/O State @nRESET	I/O Type
U1	VD16/GPD8	GPD8	–/–	–/–	O(L)/–	I	t8
M6	VD17/GPD9	GPD9	–/–	–/–	O(L)/–	I	t8
P4	VD18/GPD10	GPD10	–/–	–/–	O(L)/–	I	t8
N5	VD19/GPD11	GPD11	–/–	–/–	O(L)/–	I	t8
U2	VD20/GPD12	GPD12	–/–	–/–	O(L)/–	I	t8
T3	VD21/GPD13	GPD13	–/–	–/–	O(L)/–	I	t8
U3	VD22/nSS1/GPD14	GPD14	–/–	–/–	O(L)/–	I	t8
R4	VD23/nSS0/GPD15	GPD15	–/–	–/–	O(L)/–	I	t8
R5	VDDiarm	VDDiarm	P	P	P	P	d1c
T4	VSSiarm	VSSiarm	P	P	P	P	s3i
M7	VDDOP	VDDOP	P	P	P	P	d3o
U4	VSSOP	VSSOP	P	P	P	P	s3o
P5	I2SLRCK/GPE0	GPE0	–/–	–/–	O(L)/–	I	t8
T5	I2SSCLK/GPE1	GPE1	–/–	–/–	O(L)/–	I	t8
L9	CDCLK/GPE2	GPE2	–/–	–/–	O(L)/–	I	t8
U5	I2SSDI/nSS0/GPE3	GPE3	–/–/–	–/–/–	–/–/–	I	t8
P6	I2SSDO/I2SSDI/GPE4	GPE4	–/–/–	–/–/–	O(L)/–/–	I	t8
R6	SDCLK/GPE5	GPE5	–/–	–/–	O(L)/–	I	t8
T6	SDCMD/GPE6	GPE6	–/–	–/–	Hi-z/–	I	t8
N6	SDDAT0/GPE7	GPE7	–/–	–/–	Hi-z/–	I	t8
U6	SDDAT1/GPE8	GPE8	–/–	–/–	Hi-z/–	I	t8
P7	SDDAT2/GPE9	GPE9	–/–	–/–	Hi-z/–	I	t8
M8	SDDAT3/GPE10	GPE10	–/–	–/–	Hi-z/–	I	t8
T7	SPIMISO0/GPE11	GPE11	–/–	–/–	Hi-z/–	I	t8
N8	SPIMOSI0/GPE12	GPE12	–/–	–/–	Hi-z/–	I	t8
R7	SPICLK0/GPE13	GPE13	–/–	–/–	Hi-z/–	I	t8
M9	VDDiarm	VDDiarm	P	P	P	P	d1c
N7	VSSiarm	VSSiarm	P	P	P	P	s3i
N9	IICSCL/GPE14	GPE14	–/–	–/–	Hi-z/–	I	d8
U7	IICSDA/GPE15	GPE15	–/–	–/–	Hi-z/–	I	d8
P8	EINT8/GPG0	GPG0	–/–	–/–	–/–	I	t8
T8	EINT9/GPG1	GPG1	–/–	–/–	–/–	I	t8
R8	EINT10/nSS0/GPG2	GPG2	–/–/–	–/–/–	–/–/–	I	t8

Table 1-1. 272-Pin LQFP Pin Assignment(Continued)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @STOP	I/O State @PWR_off	I/O State @nRESET	I/O Type
U8	EINT11/nSS1/GPG3	GPG3	–/–/–	–/–/–	–/–/–	I	t8
T9	EINT12/LCD_PWREN /GPG4	GPG4	–/–/–	–/–/–	–/O(L)/–	I	t8
P9	EINT13/SPIMISO1/GPG5	GPG5	–/–/–	–/–/–	–/Hi-z/–	I	t8
M10	EINT14/SPIMOSI1/GPG6	GPG6	–/–/–	–/–/–	–/Hi-z/–	I	t8
R9	VSSOP	VSSOP	P	P	P	P	s3o
U9	VDDOP	VDDOP	P	P	P	P	d3o
P10	VDDiarm	VDDiarm	P	P	P	P	d1c
T10	VSSiarm	VSSiarm	P	P	P	P	s3i
U10	EINT15/SPICLK1/GPG7	GPG7	–/–/–	–/–/–	–/Hi-z/–	I	t8
R10	EINT16/GPG8	GPG8	–/–	–/–	–/–	I	t6
N11	EINT17/GPG9	GPG9	–/–	–/–	–/–	I	t6
N10	EINT18/GPG10	GPG10	–/–	–/–	–/–	I	t6
P11	EINT19/TCLK1/GPG11	GPG11	–/–/–	–/–/–	–/–/–	I	t12
M11	EINT20/XMON/GPG12	GPG12	–/–/–	–/–/–	–/O(L)/–	I	t12
R11	EINT21/nXPON/GPG13	GPG13	–/–/–	–/–/–	–/O(L)/–	I	t12
U11	EINT22/YMON/GPG14	GPG14	–/–/–	–/–/–	–/O(L)/–	I	t12
T11	EINT23/nYPON/GPG15	GPG15	–/–/–	–/–/–	–/O(L)/–	I	t12
U12	CLKOUT0/GPH9	GPH9	–/–	–/–	O(L)/–	I	t12
T12	CLKOUT1/GPH10	GPH10	–/–	–/–	O(L)/–	I	t12
P12	DP1/PDP0	DP1	–	–	–	AI	us
N12	DN1/PDN0	DN1	–	–	–	AI	us
U13	DP0	DP0	–	–	–	AI	us
T13	DN0	DN0	–	–	–	AI	us
R12	NCON1	NCON1	–	–	–	I	us
P13	NCON0	NCON0	–	–	–	I	us
R13	OM3	OM3	–	–	–	I	is
U14	OM2	OM2	–	–	–	I	is
L11	OM1	OM1	–	–	–	I	is
R14	OM0	OM0	–	–	–	I	is
T14	VSSOP	VSSOP	P	P	P	P	s3o
T15	VSSA_ADC	VSSA_ADC	P	P	P	P	s3t
U15	Vref	Vref	–	–	–	AI	ia
T16	AIN0	AIN0	–	–	–	AI	r10

Table 1-1. 272-Pin LQFP Pin Assignment(Continued)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @STOP	I/O State @PWR_off	I/O State @nRESET	I/O Type
R15	AIN1	AIN1	–	–	–	AI	r10
U16	AIN2	AIN2	–	–	–	AI	r10
U17	AIN3	AIN3	–	–	–	AI	r10
M12	AIN4	AIN4	–	–	–	AI	r10
P14	AIN5	AIN5	–	–	–	AI	r10
N13	AIN6	AIN6	–	–	–	AI	r10
T17	AIN7	AIN7	–	–	–	AI	r10
R16	VDDA_ADC	VDDA_ADC	P	P	P	P	d3t
R17	XTOrtc	XTOrtc	–	–	–	AO	gp
P15	XTIrtc	XTIrtc	–	–	–	AI	gp
P16	RTCVDD	RTCVDD	P	P	P	P	d1i
N15	VDDi_MPLL	VDDi_MPLL	P	P	P	P	d1c
N14	VSSi_MPLL	VSSi_MPLL	P	P	P	P	s3i
P17	MPLLCAP	MPLLCAP	–	–	–	AI	gp
L12	VDDi_UPLL	VDDi_UPLL	P	P	P	P	d1c
N16	VSSi_UPLL	VSSi_UPLL	P	P	P	P	s3i
J11	UPLLCAP	UPLLCAP	–	–	–	AI	gp
N17	VDDOP	VDDOP	P	P	P	P	d3o
M14	EINT0/GPF0	GPF0	–/–	–/–	–/–	I	t8
M15	EINT1/GPF1	GPF1	–/–	–/–	–/–	I	t8
M16	EINT2/GPF2	GPF2	–/–	–/–	–/–	I	t8
M13	EINT3/GPF3	GPF3	–/–	–/–	–/–	I	t8
M17	EINT4/GPF4	GPF4	–/–	–/–	–/–	I	t8
L16	EINT5/GPF5	GPF5	–/–	–/–	–/–	I	t8
K12	EINT6/GPF6	GPF6	–/–	–/–	–/–	I	t8
L14	EINT7/GPF7	GPF7	–/–	–/–	–/–	I	t8
K13	UCLK/GPH8	GPH8	–/–	–/–	–/–	I	t8
L13	nCTS0/GPH0	GPH0	–/–	–/–	–/–	I	t8
J12	nRTS0/GPH1	GPH1	–/–	–/–	O(H)/–	I	t8
L15	TXD0/GPH2	GPH2	–/–	–/–	O(H)/–	I	t8
J13	RXD0/GPH3	GPH3	–/–	–/–	–/–	I	t8
L17	TXD1/GPH4	GPH4	–/–	–/–	O(H)/–	I	t8
K14	RXD1/GPH5	GPH5	–/–	–/–	–/–	I	t8

Table 1-1. 272-Pin LQFP Pin Assignment(Continued)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @STOP	I/O State @PWR_off	I/O State @nRESET	I/O Type
K16	TXD2/nRTS1/GPH6	GPH6	–/–	–/–	O(H)/–	I	t8
K15	RXD2/nCTS1/GPH7	GPH7	–/–	–/–	–/–	I	t8
K17	BATT_FLT	BATT_FLT	–	–	–	I	is
J16	nRSTOUT/GPA21	nRSTOUT	–/–	–/–	O(L)/–	O	b8
J14	PWREN	PWREN	O(H)	O(H)	O(L)	O	b8
H12	nRESET	nRESET	–	–	–	I	is
J15	VDDalive	VDDalive	P	P	P	P	d1i
J17	EXTCLK	EXTCLK	–	–	–	AI	is
H14	VDDi	VDDi	P	P	P	P	d1c
H16	XTOpll	XTOpll	–	–	–	AO	m26
H17	XTIpll	XTIpll	–	–	–	AI	m26
H15	VSSi	VSSi	P	P	P	P	s3i
G13	VSSOP	VSSOP	P	P	P	P	s3o
H13	VDDMOP	VDDMOP	P	P	P	P	d3o
G14	nFCE/GPA22	nFCE	O(H)/–	O(H)/–	O(H)/–	O	b8
G12	nFRE/GPA20	nFRE	O(H)/–	O(H)/–	O(H)/–	O	b8
G15	nFWE/GPA19	nFWE	O(H)/–	O(H)/–	O(H)/–	O	b8
G17	ALE/GPA18	ALE	O(L)/–	O(L)/–	O(L)/–	O	b8
G16	CLE/GPA17	CLE	O(L)/–	O(L)/–	O(L)/–	O	b8
F17	nWAIT	nWAIT	–	–	–	I	is
F16	nGCS7	nGCS7	Hi-z	Pre or Hi-z	O(H)	O	ot
F14	nGCS6	nGCS6	Hi-z	Pre or Hi-z	O(H)	O	ot
F13	nGCS5/GPA16	nGCS5	Hi-z	Pre or Hi-z	O(H)/–	O	ot
E17	nGCS4/GPA15	nGCS4	Hi-z	Pre or Hi-z	O(H)/–	O	ot
F15	nGCS3/GPA14	nGCS3	Hi-z	Pre or Hi-z	O(H)/–	O	ot
E16	nGCS2/GPA13	nGCS2	Hi-z	Pre or Hi-z	O(H)/–	O	ot
E15	nGCS1/GPA12	nGCS1	Hi-z	Pre or Hi-z	O(H)/–	O	ot
E14	nGCS0	nGCS0	Hi-z	Pre or Hi-z	O(H)	O	ot
D17	SCKE	SCKE	Hi-z	O(L)	O(L)	O	ot
G11	VSSOP	VSSOP	P	P	P	P	s3o
D15	SCLK1	SCLK1	Hi-z	O(L)	O(L)	O	t16
D16	VDDi	VDDi	P	P	P	P	d1c
C17	SCLK0	SCLK0	Hi-z	O(L)	O(L)	O	t16

Table 1-1. 272-Pin LQFP Pin Assignment(Continued)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @STOP	I/O State @PWR_off	I/O State @nRESET	I/O Type
C16	VSSi	VSSi	P	P	P	P	s3i
B16	nWE	nWE	Hi-z	Pre or Hi-z	O(H)	O(H)	ot
C15	nOE	nOE	Hi-z	Pre or Hi-z	O(H)	O(H)	ot
B17	nBE0	nBE0	Hi-z	Pre or Hi-z	O(H)	O(H)	ot
A17	nBE1	nBE1	Hi-z	Pre or Hi-z	O(H)	O(H)	ot
F12	nBE2	nBE2	Hi-z	Pre or Hi-z	O(H)	O(H)	ot
E13	nBE3	nBE3	Hi-z	Pre or Hi-z	O(H)	O(H)	ot
D14	nSRAS	nSRAS	Hi-z	Pre or Hi-z	O(H)	O(H)	ot
A16	nSCAS	nSCAS	Hi-z	Pre or Hi-z	O(H)	O(H)	ot
B15	VDDMOP	VDDMOP	P	P	P	P	d3o
A15	VSSOP	VSSOP	P	P	P	P	s3o
C14	ADDR0/GPA0	ADDR0	Hi-z/–	Pre or Hi-z/–	O(L)/–	O(L)	ot
C13	ADDR1	ADDR1	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
B14	ADDR2	ADDR2	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
D13	ADDR3	ADDR3	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
A14	ADDR4	ADDR4	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
F11	ADDR5	ADDR5	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
B13	ADDR6	ADDR6	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
G9	ADDR7	ADDR7	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
A13	ADDR8	ADDR8	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
D12	ADDR9	ADDR9	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
C12	VSSOP	VSSOP	P	P	P	P	s3o
B12	VDDMOP	VDDMOP	P	P	P	P	d3o
E12	ADDR10	ADDR10	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
A12	ADDR11	ADDR11	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
B11	VDDi	VDDi	P	P	P	P	d1c
D11	VSSi	VSSi	P	P	P	P	s3i
F10	ADDR12	ADDR12	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
C11	ADDR13	ADDR13	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
E10	ADDR14	ADDR14	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
E11	ADDR15	ADDR15	Hi-z	Pre or Hi-z	O(L)	O(L)	ot
F9	ADDR16/GPA1	ADDR16	Hi-z	Pre or Hi-z/–	O(L)/–	O(L)	ot
A11	ADDR17/GPA2	ADDR17	Hi-z	Pre or Hi-z/–	O(L)/–	O(L)	ot

Table 1-1. 272-Pin LQFP Pin Assignment(Continued)

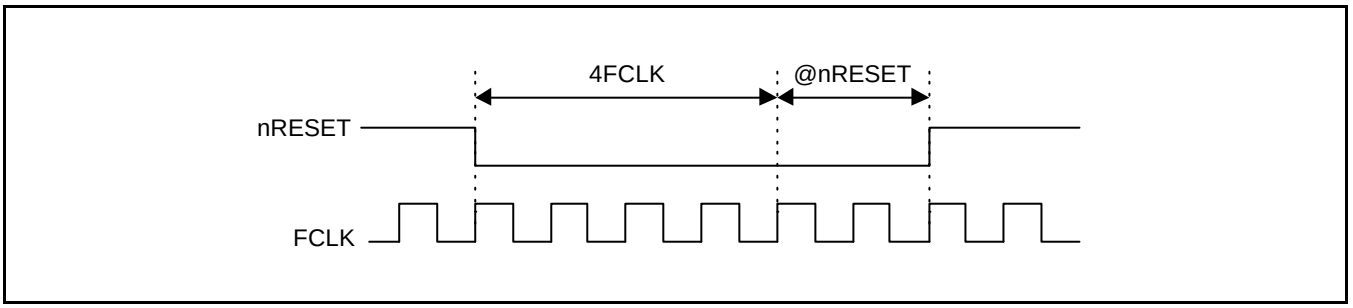
Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @STOP	I/O State @PWR_off	I/O State @nRESET	I/O Type
E9	VSSOP	VSSOP	P	P	P	P	s3o
D10	ADDR18/GPA3	ADDR18	Hi-z/–	Pre or Hi-z/–	O(L)	O(L)	ot
B10	ADDR19/GPA4	ADDR19	Hi-z/–	Pre or Hi-z/–	O(L)	O(L)	ot
C10	ADDR20/GPA5	ADDR20	Hi-z/–	Pre or Hi-z/–	O(L)	O(L)	ot
A10	ADDR21/GPA6	ADDR21	Hi-z/–	Pre or Hi-z/–	O(L)	O(L)	ot
B9	ADDR22/GPA7	ADDR22	Hi-z/–	Pre or Hi-z/–	O(L)	O(L)	ot
D9	ADDR23/GPA8	ADDR23	Hi-z/–	Pre or Hi-z/–	O(L)	O(L)	ot
C9	ADDR24/GPA9	ADDR24	Hi-z/–	Pre or Hi-z/–	O(L)	O(L)	ot
A9	ADDR25/GPA10	ADDR25	Hi-z/–	Pre or Hi-z/–	O(L)	O(L)	ot
D8	ADDR26/GPA11	ADDR26	Hi-z/–	Pre or Hi-z/–	O(L)	O(L)	ot
F8	VDDi	VDDi	P	P	P	P	d1c
B8	VSSi	VSSi	P	P	P	P	s3i
A8	VDDMOP	VDDMOP	P	P	P	P	d3o
C8	VSSOP	VSSOP	P	P	P	P	s3o
E7	DATA0	DATA0	Hi-z	Hi-z	Hi-z	Hi-z	u50
D7	DATA1	DATA1	Hi-z	Hi-z	Hi-z	Hi-z	u50
E8	DATA2	DATA2	Hi-z	Hi-z	Hi-z	Hi-z	u50
C7	DATA3	DATA3	Hi-z	Hi-z	Hi-z	Hi-z	u50
F7	DATA4	DATA4	Hi-z	Hi-z	Hi-z	Hi-z	u50
A7	DATA5	DATA5	Hi-z	Hi-z	Hi-z	Hi-z	u50
B7	DATA6	DATA6	Hi-z	Hi-z	Hi-z	Hi-z	u50
A6	DATA7	DATA7	Hi-z	Hi-z	Hi-z	Hi-z	u50
B6	VDDMOP	VDDMOP	P	P	P	P	d3o
D6	VSSOP	VSSOP	P	P	P	P	s3o
E6	DATA8	DATA8	Hi-z	Hi-z	Hi-z	Hi-z	u50
A5	DATA9	DATA9	Hi-z	Hi-z	Hi-z	Hi-z	u50
B5	DATA10	DATA10	Hi-z	Hi-z	Hi-z	Hi-z	u50
D5	DATA11	DATA11	Hi-z	Hi-z	Hi-z	Hi-z	u50
C6	DATA12	DATA12	Hi-z	Hi-z	Hi-z	Hi-z	u50
A4	DATA13	DATA13	Hi-z	Hi-z	Hi-z	Hi-z	u50
C5	DATA14	DATA14	Hi-z	Hi-z	Hi-z	Hi-z	u50
B4	DATA15	DATA15	Hi-z	Hi-z	Hi-z	Hi-z	u50
G7	VDDMOP	VDDMOP	P	P	P	P	d3o

Table 1-1. 272-Pin LQFP Pin Assignment(Continued)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @STOP	I/O State @PWR_off	I/O State @nRESET	I/O Type
A3	VSSOP	VSSOP	P	P	P	P	s3o
C4	VDDi	VDDi	P	P	P	P	d1c
B2	VSSi	VSSi	P	P	P	P	s3i
B3	DATA16	DATA16	Hi-z	Hi-z	Hi-z	Hi-z	u50
C3	DATA17	DATA17	Hi-z	Hi-z	Hi-z	Hi-z	u50
A2	DATA18	DATA18	Hi-z	Hi-z	Hi-z	Hi-z	u50
F6	DATA19	DATA19	Hi-z	Hi-z	Hi-z	Hi-z	u50
A1	DATA20	DATA20	Hi-z	Hi-z	Hi-z	Hi-z	u50

NOTES:

1. The @BUS REQ. shows the pin states at the external bus, which is used by the other bus master. The @STOP shows the pin states when S3C2410 is in STOP mode.
2. '–' mark indicates the unchanged pin state at STOP mode or Bus Request mode.
3. Hi-z or Pre means Hi-z or Previous state and which is determined by the setting of MISCCR register.
4. AI/AO means analog input/output.
5. P, I, and O mean power, input and output respectively.
6. The I/O state @nRESET shows the pin status in the below @nRESET duration.



7. The below table shows the I/O types and descriptions.

I/O Type	Descriptions
d1i(vdd1ih), s3i(vss3i)	1.8V Vdd/Vss for internal logic
d1c(vdd1ih_core), s3i(vss3i)	1.8V Vdd/Vss for internal logic without input driver
d3o(vdd3op), s3o(vss3op)	3.3V Vdd/Vss for external logic
d3t(vdd3t_abb), s3t(vss3t_abb)	3.3V Vdd/Vss for analog circuitry
is(phis)	Input pad, LVCMOS schmitt-trigger level
us(pbusb)	USB pad
ot(phot8)	Output pad, tri-state, Io=8mA
b8(phob8)	Output pad, Io=8mA
t16(phot16sm)	Output pad, tri-state, medium slew rate, Io=16mA
r10(phiar10_abb)	Analog input pad with 10-ohm resistor
ia(phia_abb)	Analog input pad
gp(phgpad_option)	Pad for analog pin
m26(phsoscm26)	Oscillator cell with enable and feedback resistor
u50(phbsu50ct12sm)	Bi-directional pad, LVCMOS schmitt-trigger, 50Kohm pull-up resistor with control, tri-state, Io=12mA
t6(phbsu100ct6sm)	Bi-directional pad, LVCMOS schmitt-trigger, 100Kohm pull-up resistor with control, tri-state, Io=6mA
t8(phbsu100ct8sm)	Bi-directional pad, LVCMOS schmitt-trigger, 100Kohm pull-up resistor with control, tri-state, Io=8mA
t12(phbsu100ct12sm)	Bi-directional pad, LVCMOS schmitt-trigger, 100Kohm pull-up resistor with control, tri-state, Io=12mA
d8(phbsu100cd8sm)	Bi-directional pad, LVCMOS schmitt-trigger, 100Kohm pull-up resistor with control, open-drain, Io=8mA

SIGNAL DESCRIPTIONS

Table 1-2. S3C2410 Signal Descriptions

Signal	I/O	Description
BUS CONTROLLER		
OM[1:0]	I	OM[1:0] sets S3C2410 in the TEST mode, which is used only at fabrication. Also, it determines the bus width of nGCS0. The pull-up/down resistor determines the logic level during the RESET cycle. 00:Nand-boot 01:16-bit 10:32-bit 11:Test mode
ADDR[26:0]	O	ADDR[26:0] (Address Bus) outputs the memory address of the corresponding bank .
DATA[31:0]	IO	DATA[31:0] (Data Bus) inputs data during memory read and outputs data during memory write. The bus width is programmable among 8/16/32-bit.
nGCS[7:0]	O	nGCS[7:0] (General Chip Select) are activated when the address of a memory is within the address region of each bank. The number of access cycles and the bank size can be programmed.
nWE	O	nWE (Write Enable) indicates that the current bus cycle is a write cycle.
nOE	O	nOE (Output Enable) indicates that the current bus cycle is a read cycle.
nXBREQ	I	nXBREQ (Bus Hold Request) allows another bus master to request control of the local bus. BACK active indicates that bus control has been granted.
nXBACK	O	nXBACK (Bus Hold Acknowledge) indicates that the S3C2410 has surrendered control of the local bus to another bus master.
nWAIT	I	nWAIT requests to prolong a current bus cycle. As long as nWAIT is L, the current bus cycle cannot be completed.
DRAM/SDRAM/SRAM		
nSRAS	O	SDRAM Row Address Strobe
nSCAS	O	SDRAM Column Address Strobe
nSCS[1:0]	O	SDRAM Chip Select
DQM[3:0]	O	SDRAM Data Mask
SCLK[1:0]	O	SDRAM Clock
SCKE	O	SDRAM Clock Enable
nBE[3:0]	O	Upper Byte/Lower Byte Enable(In case of 16-bit SRAM)
nWBE[3:0]	O	Write Byte Enable
NAND FLASH		
CLE	O	Command Latch Enable
ALE	O	Address Latch Enable
nFCE	O	Nand Flash Chip Enable
nFRE	O	Nand Flash Read Enable
nFWE	O	Nand Flash Write Enable
NCON[1:0]	I	Nand Flash Configuration

Table 1-2. S3C2410 Signal Descriptions (Continued)

Signal	I/O	Description
LCD CONTROL UNIT		
VD[23:0]	O	**STN/TFT:** LCD Data Bus
VCLK	O	**STN/TFT:** LCD clock signal
VFRAME	O	**STN:** LCD Frame signal
VLINE	O	**STN:** LCD line signal
VM	O	**STN:** VM alternates the polarity of the row and column voltage
VSYNC	O	**TFT:** Vertical synchronous signal
HSYNC	O	**TFT:** Horizontal synchronous signal
VDEN	O	**TFT:** Data enable signal
LEND	O	**TFT:** Line End signal
LCDVF[2:0]	O	**TFT:** Timing control signal for specific TFT LCD
INTERRUPT CONTROL UNIT		
EINT[23:0]	I	External Interrupt request
DMA		
nXDREQ[1:0]	I	External DMA request
nXDACK[1:0]	O	External DMA acknowledge
UART		
RxD[2:0]	I	UART receives data input
TxD[2:0]	O	UART transmits data output
nCTS[1:0]	I	UART clear to send input signal
nRTS[1:0]	O	UART request to send output signal
UCLK	I	UART clock signal
IIC-BUS		
IICSDA	IO	IIC-bus data
IICSCL	IO	IIC-bus clock
IIS-BUS		
I2SLRCK	IO	IIS-bus channel select clock
I2SSDO	O	IIS-bus serial data output
I2SSDI	I	IIS-bus serial data input
I2SSCLK	IO	IIS-bus serial clock
CDCLK	O	CODEC system clock

Table 1-2. S3C2410 Signal Descriptions (Continued)

Signal	I/O	Description
ADC		
AIN[7:0]	AI	ADC input[7:0]
Vref	AI	ADC Vref
TOUCH SCREEN		
nXPON	O	Plus X-axis on-off control signal
XMON	O	Minus X-axis on-off control signal
nYPON	O	Plus Y-axis on-off control signal
YMON	O	Minus Y-axis on-off control signal
USB HOST		
DN[1:0]	IO	DATA(–) from USB host
DP[1:0]	IO	DATA(+) from USB host
USB DEVICE		
PDN0	IO	DATA(–) for USB peripheral
PDP0	IO	DATA(+) for USB peripheral
SPI		
SPIMISO[1:0]	IO	SPIMISO is the master data input line, when SPI is configured as a master. When SPI is configured as a slave, these pins reverse its role.
SPIMOSI[1:0]	IO	SPIMOSI is the master data output line, when SPI is configured as a master. When SPI is configured as a slave, these pins reverse its role.
SPICLK[1:0]	IO	SPI clock
nSS[1:0]	I	SPI chip select(only for slave mode)
MMC		
SDDAT[3:0]	IO	SD receive/transmit data
SDCMD	IO	SD receive response/ transmit command
SDCLK	O	SD clock
GENERAL PORT		
GPn[116:0]	IO	General input/output ports (some ports are output only)
TIMMER/PWM		
TOUT[3:0]	O	Timer output[3:0]
TCLK[1:0]	I	External timer clock input

Table 1-2. S3C2410 Signal Descriptions (Continued)

Signal	I/O	Description
JTAG TEST LOGIC		
nTRST	I	nTRST(TAP Controller Reset) resets the TAP controller at start. If debugger is used, A 10K pull-up resistor has to be connected. If debugger(black ICE) is not used, nTRST pin must be at L or low active pulse.
TMS	I	TMS (TAP Controller Mode Select) controls the sequence of the TAP controller's states. A 10K pull-up resistor has to be connected to TMS pin.
TCK	I	TCK (TAP Controller Clock) provides the clock input for the JTAG logic. A 10K pull-up resistor must be connected to TCK pin.
TDI	I	TDI (TAP Controller Data Input) is the serial input for test instructions and data. A 10K pull-up resistor must be connected to TDI pin.
TDO	O	TDO (TAP Controller Data Output) is the serial output for test instructions and data.
RESET & CLOCK & POWER		
nRESET	ST	nRESET suspends any operation in progress and places S3C2410 into a known reset state. For a reset, nRESET must be held to L level for at least 4 FCLK after the processor power has been stabilized.
nRSTOUT	O	For external device reset control(nRSTOUT = nRESET & nWDTRST & SW_RESET)
PWREN	O	1.8V core power on-off control signal
BATT_FLT	I	Probe for battery state(Does not wake up at stop mode in case of low battery state)
OM[3:2]	I	OM[3:2] determines how the clock is made. OM[3:2] = 00b, Crystal is used for MPLL CLK source and UPLL CLK source. OM[3:2] = 01b, Crystal is used for MPLL CLK source and EXTCLK is used for UPLL CLK source. OM[3:2] = 10b, EXTCLK is used for MPLL CLK source and Crystal is used for UPLL CLK source. OM[3:2] = 11b, EXTCLK is used for MPLL CLK source and UPLL CLK source.
EXTCLK	I	External clock source. When OM[3:2] = 11b, EXTCLK is used for MPLL CLK source and UPLL CLK source. When OM[3:2] = 10b, EXTCLK is used for MPLL CLK source only. When OM[3:2] = 01b, EXTCLK is used for UPLL CLK source only. If it isn't used, it has to be H (3.3V).
XTIpll	AI	Crystal Input for internal osc circuit. When OM[3:2] = 00b, XTIpll is used for MPLL CLK source and UPLL CLK source. When OM[3:2] = 01b, XTIpll is used for MPLL CLK source only. When OM[3:2] = 10b, XTIpll is used for UPLL CLK source only. If it isn't used, XTIpll has to be H (3.3V).
XTOpll	AO	Crystal Output for internal osc circuit. When OM[3:2] = 00b, XTIpll is used for MPLL CLK source and UPLL CLK source. When OM[3:2] = 01b, XTIpll is used for MPLL CLK source only. When OM[3:2] = 10b, XTIpll is used for UPLL CLK source only. If it isn't used, it has to be a floating pin.

Table 1-2. S3C2410 Signal Descriptions (Continued)

Signal	I/O	Description
RESET & CLOCK & POWER (continued)		
MPLLCAP	AI	Loop filter capacitor for main clock.
UPLLCAP	AI	Loop filter capacitor for USB clock.
XTIrtc	AI	32 KHz crystal input for RTC.
XTOrtc	AO	32 KHz crystal output for RTC.
CLKOUT[1:0]	O	Clock output signal. The CLKSEL of MISCCR register configures the clock output mode among the MPLL CLK, UPLL CLK, FCLK, HCLK, PCLK.
POWER		
VDDalive	P	S3C2410 reset block and port status register VDD(1.8V). It should be always supplied whether in normal mode or in power-off mode.
VDDi/VDDiarm	P	S3C2410 core logic VDD(1.8V) for CPU.
VSSi/VSSiarm	P	S3C2410 core logic VSS
VDDi_MPLL	P	S3C2410 MPLL analog and digital VDD (1.8 V).
VSSi_MPLL	P	S3C2410 MPLL analog and digital VSS.
VDDOP	P	S3C2410 I/O port VDD(3.3V)
VDDMOP	P	S3C2410 Memory I/O VDD 3.3V : SCLK up to 100MHz 2.5V : SCLK up to 85MHz 1.8V : SCLK up to 66MHz
VSSOP	P	S3C2410 I/O port VSS
RTCVDD	P	RTC VDD (1.8 V, Not support 3.3V) (This pin must be connected to power properly if RTC isn't used)
VDDi_UPLL	P	S3C2410 UPLL analog and digital VDD (1.8V)
VSSi_UPLL	P	S3C2410 UPLL analog and digital VSS
VDDA_ADC	P	S3C2410 ADC VDD(3.3V)
VSSA_ADC	P	S3C2410 ADC VSS

NOTES:
1. I/O means input/output.
2. AI/AO means analog input/output.
3. ST means schmitt-trigger.
4. P means power.

S3C2410 SPECIAL REGISTERS

Table 1-3. S3C2410 Special Registers

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
MEMORY CONTROLLER					
BWSCON	0x48000000	←	W	R/W	Bus Width & Wait Status Control
BANKCON0	0x48000004				Boot ROM Control
BANKCON1	0x48000008				BANK1 Control
BANKCON2	0x4800000C				BANK2 Control
BANKCON3	0x48000010				BANK3 Control
BANKCON4	0x48000014				BANK4 Control
BANKCON5	0x48000018				BANK5 Control
BANKCON6	0x4800001C				BANK6 Control
BANKCON7	0x48000020				BANK7 Control
REFRESH	0x48000024				DRAM/SDRAM Refresh Control
BANKSIZE	0x48000028				Flexible Bank Size
MRSRB6	0x4800002C				Mode register set for SDRAM
MRSRB7	0x48000030				Mode register set for SDRAM

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
USB HOST CONTROLLER					
HcRevision	0x49000000	←	W		Control and Status Group
HcControl	0x49000004				
HcCommonStatus	0x49000008				
HcInterruptStatus	0x4900000c				
HcInterruptEnable	0x49000010				
HcInterruptDisable	0x49000014				
HcHCCA	0x49000018				Memory Pointer Group
HcPeriodCuttentED	0x4900001c				
HcControlHeadED	0x49000020				
HcControlCurrentED	0x49000024				
HcBulkHeadED	0x49000028				
HcBulkCurrentED	0x4900002c				
HcDoneHead	0x49000030				
HcRmInterval	0x49000034				Frame Counter Group
HcFmRemaining	0x49000038				
HcFmNumber	0x4900003c				
HcPeriodicStart	0x49000040				
HcLSThreshold	0x49000044				
HcRhDescriptorA	0x49000048				Root Hub Group
HcRhDescriptorB	0x4900004c				
HcRhStatus	0x49000050				
HcRhPortStatus1	0x49000054				
HcRhPortStatus2	0x49000058				
INTERRUPT CONTROLLER					
SRCPND	0X4a000000	←	W	R/W	Interrupt Request Status
INTMOD	0X4a000004			W	Interrupt Mode Control
INTMSK	0X4a000008			R/W	Interrupt Mask Control
PRIORITY	0X4a00000a			W	IRQ Priority Control
INTPND	0X4a000010			R/W	Interrupt Request Status
INTOFFSET	0X4a000014			R	Interrupt request source offset
SUBSRCPND	0X4a000018			R/W	Sub source pending
INTSUBMSK	0X4a00001c			R/W	Interrupt sub mask

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
DMA					
DISRC0	0x4b000000	←	W	R/W	DMA 0 Initial Source
DISRCC0	0x4b000004				DMA 0 Initial Source Control
DIDST0	0x4b000008				DMA 0 Initial Destination
DIDSTC0	0x4b00000c				DMA 0 Initial Destination Control
DCON0	0x4b000010				DMA 0 Control
DSTAT0	0x4b000014			R	DMA 0 Count
DCSRC0	0x4b000018				DMA 0 Current Source
DCDST0	0x4b00001c				DMA 0 Current Destination
DMASKTRIG0	0x4b000020	←	W	R/W	DMA 0 Mask Trigger
DISRC1	0x4b000040				DMA 1 Initial Source
DISRCC1	0x4b000044				DMA 1 Initial Source Control
DIDST1	0x4b000048				DMA 1 Initial Destination
DIDSTC1	0x4b00004c				DMA 1 Initial Destination Control
DCON1	0x4b000050				DMA 1 Control
DSTAT1	0x4b000054			R	DMA 1 Count
DCSRC1	0x4b000058				DMA 1 Current Source
DCDST1	0x4b00005c	←	W		DMA 1 Current Destination
DMASKTRIG1	0x4b000060			R/W	DMA 1 Mask Trigger
DISRC2	0x4b000080				DMA 2 Initial Source
DISRCC2	0x4b000084				DMA 2 Initial Source Control
DIDST2	0x4b000088				DMA 2 Initial Destination
DIDSTC2	0x4b00008c				DMA 2 Initial Destination Control
DCON2	0x4b000090				DMA 2 Control
DSTAT2	0x4b000094			R	DMA 2 Count
DCSRC2	0x4b000098	←	W		DMA 2 Current Source
DCDST2	0x4b00009c				DMA 2 Current Destination
DMASKTRIG2	0x4b0000a0			R/W	DMA 2 Mask Trigger

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
DMA(Continued)					
DISRC3	0x4b0000c0	←	W	R/W	DMA 3 Initial Source
DISRCC3	0x4b0000c4				DMA 3 Initial Source Control
DIDST3	0x4b0000c8				DMA 3 Initial Destination
DIDSTC3	0x4b0000cc				DMA 3 Initial Destination Control
DCON3	0x4b0000d0				DMA 3 Control
DSTAT3	0x4b0000d4			R	DMA 3 Count
DCSRC3	0x4b0000d8				DMA 3 Current Source
DCDST3	0x4b0000dc				DMA 3 Current Destination
DMASKTRIG3	0x4b0000e0			R/W	DMA 3 Mask Trigger

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
CLOCK & POWER MANAGEMENT					
LOCKTIME	0x4c00_0000	←	W	R/W	PLL Lock Time Counter
MPLLCON	0x4c00_0004				MPLL Control
UPLLCON	0x4c00_0008				UPLL Control
CLKCON	0x4c00_000C				Clock Generator Control
CLKSLOW	0x4c00_0010				Slow Clock Control
CLKDIVN	0x4c00_0014				Clock divider Control
LCD CONTROLLER					
LCDCON1	0X4d000000	←	W	R/W	LCD Control 1
LCDCON2	0X4d000004				LCD Control 2
LCDCON3	0X4d000008				LCD Control 3
LCDCON4	0X4d00000C				LCD Control 4
LCDCON5	0X4d000010				LCD Control 5
LCDSADDR1	0X4d000014				STN/TFT: Frame Buffer Start Address1
LCDSADDR2	0X4d000018				STN/TFT: Frame Buffer Start Address2
LCDSADDR3	0X4d00001C				STN/TFT: Virtual Screen Address Set
REDLUT	0X4d000020				STN: Red Lookup Table
GREENLUT	0X14A00024				STN: Green Lookup Table
BLUELUT	0X4d000028				STN: Blue Lookup Table
DITHMODE	0X4d00004C				STN: Dithering Mode
TPAL	0X4d000050				TFT: Temporary Palette
LCDINTPND	0X4d000054				LCD Interrupt Pending
LCDSRCPND	0X4d000058				LCD Interrupt Source
LCDINTMSK	0X4d00005C				LCD Interrupt Mask
LPCSEL	0X4d000060				LPC3600 Control

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
NAND FLASH					
NFCONF	0x4E00_0000	←	W	R/W	NAND Flash Configuration
NFCMD	0x4E00_0004				NAND Flash Command
NFADDR	0x4E00_0008				NAND Flash Address
NFDATA	0x4E00_000C				NAND Flash Data
NFSTAT	0x4E00_0010			R	NAND Flash Operation Status
NFECC	0x4E00_0014			R/W	NAND Flash ECC

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
UART					
ULCON0	0x50000000	←	W	R/W	UART 0 Line Control
UCON0	0x50000004				UART 0 Control
UFCON0	0x50000008				UART 0 FIFO Control
UMCON0	0x5000000c				UART 0 Modem Control
UTRSTAT0	0x50000010			R	UART 0 Tx/Rx Status
UERSTAT0	0x50000014				UART 0 Rx Error Status
UFSTAT0	0x50000018				UART 0 FIFO Status
UMSTAT0	0x5000001c				UART 0 Modem Status
UTXH0	0x50000023	0x50000020	B	W	UART 0 Transmission Hold
URXH0	0x50000027	0x50000024		R	UART 0 Receive Buffer
UBRDIV0	0x50000028	←	W	R/W	UART 0 Baud Rate Divisor
ULCON1	0x50004000	←	W	R/W	UART 1 Line Control
UCON1	0x50004004				UART 1 Control
UFCON1	0x50004008				UART 1 FIFO Control
UMCON1	0x5000400c				UART 1 Modem Control
UTRSTAT1	0x50004010			R	UART 1 Tx/Rx Status
UERSTAT1	0x50004014				UART 1 Rx Error Status
UFSTAT1	0x50004018				UART 1 FIFO Status
UMSTAT1	0x5000401c				UART 1 Modem Status
UTXH1	0x50004023	0x50004020	B	W	UART 1 Transmission Hold
URXH1	0x50004027	0x50004024		R	UART 1 Receive Buffer
UBRDIV1	0x50004028	←	W	R/W	UART 1 Baud Rate Divisor
ULCON2	0x50008000	←	W	R/W	UART 2 Line Control
UCON2	0x50008004				UART 2 Control
UFCON2	0x50008008				UART 2 FIFO Control
UTRSTAT2	0x50008010			R	UART 2 Tx/Rx Status
UERSTAT2	0x50008014				UART 2 Rx Error Status
UFSTAT2	0x50008018				UART 2 FIFO Status
UTXH2	0x50008023	0x50008020	B	W	UART 2 Transmission Hold
URXH2	0x50008027	0x50008024		R	UART 2 Receive Buffer
UBRDIV2	0x50008028	←	W	R/W	UART 2 Baud Rate Divisor

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
PWM TIMER					
TCFG0	0x51000000	←	W	R/W	Timer Configuration
TCFG1	0x51000004				Timer Configuration
TCON	0x51000008				Timer Control
TCNTB0	0x5100000c				Timer Count Buffer 0
TCMPB0	0x51000010				Timer Compare Buffer 0
TCNTO0	0x51000014			R	Timer Count Observation 0
TCNTB1	0x51000018			R/W	Timer Count Buffer 1
TCMPB1	0x5100001c				Timer Compare Buffer 1
TCNTO1	0x51000020			R	Timer Count Observation 1
TCNTB2	0x51000024			R/W	Timer Count Buffer 2
TCMPB2	0x51000028				Timer Compare Buffer 2
TCNTO2	0x5100002c			R	Timer Count Observation 2
TCNTB3	0x51000030			R/W	Timer Count Buffer 3
TCMPB3	0x51000034				Timer Compare Buffer 3
TCNTO3	0x51000038			R	Timer Count Observation 3
TCNTB4	0x5100003c			R/W	Timer Count Buffer 4
TCNTO4	0x51000040			R	Timer Count Observation 4

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
USB DEVICE					
FUNC_ADDR_REG	0x52000143	0x52000140	B	R/W	Function Address
PWR_REG	0x52000147	0x52000144			Power Management
EP_INT_REG	0x5200014b	0x52000148			EP Interrupt Pending and Clear
USB_INT_REG	0x5200015b	0x52000158			USB Interrupt Pending and Clear
EP_INT_EN_REG	0x5200015f	0x5200015c			Interrupt Enable
USB_INT_EN_REG	0x5200016f	0x5200016c			Interrupt Enbale
FRAME_NUM1_REG	0x52000173	0x52000170		R	Frame Number Lower Byte
INDEX_REG	0x5200017b	0x52000178		R/W	Register Index
EP0_CSR	0x52000187	0x52000184			Endpoint 0 Status
IN_CSR1_REG	0x52000187	0x52000184			In Endpoint Control Status
IN_CSR2_REG	0x5200018b	0x52000188			In Endpoint Control Status
MAXP_REG	0x5200018f	0x5200018c			Endpoint Max Packet
OUT_CSR1_REG	0x52000193	0x52000190			Out Endpoint Control Status
OUT_CSR2_REG	0x52000197	0x52000194			Out Endpoint Control Status
OUT_FIFO_CNT1_REG	0x5200019b	0x52000198		R	Endpoint Out Write Count
OUT_FIFO_CNT2_REG	0x5200019f	0x5200019c			Endpoint Out Write Count
EP0_FIFO	0x520001c3	0x520001c0		R/W	Endpoint 0 FIFO
EP1_FIFO	0x520001c7	0x520001c4			Endpoint 1 FIFO
EP2_FIFO	0x520001cb	0x520001c8			Endpoint 2 FIFO
EP3_FIFO	0x520001cf	0x520001cc			Endpoint 3 FIFO
EP4_FIFO	0x520001d3	0x520001d0			Endpoint 4 FIFO
EP1_DMA_CON	0x52000203	0x52000200			EP1 DMA Interface Control
EP1_DMA_UNIT	0x52000207	0x52000204			EP1 DMA Tx Unit Counter
EP1_DMA_FIFO	0x5200020b	0x52000208			EP1 DMA Tx FIFO Counter
EP1_DMA_TX_LO	0x5200020f	0x5200020c			EP1 DMA Total Tx Counter
EP1_DMA_TX_MD	0x52000213	0x52000210			EP1 DMA Total Tx Counter
EP1_DMA_TX_HI	0x52000217	0x52000214			EP1 DMA Total Tx Counter

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/Write	Function
USB DEVICE(Continued)					
EP2_DMA_CON	0x5200021b	0x52000218	B	R/W	EP2 DMA Interface Control
EP2_DMA_UNIT	0x5200021f	0x5200021c			EP2 DMA Tx Unit Counter
EP2_DMA_FIFO	0x52000223	0x52000220			EP2 DMA Tx FIFO Counter
EP2_DMA_TX_LO	0x52000227	0x52000224			EP2 DMA Total Tx Counter
EP2_DMA_TX_MD	0x5200022b	0x52000228			EP2 DMA Total Tx Counter
EP2_DMA_TX_HI	0x5200022f	0x5200022c			EP2 DMA Total Tx Counter
EP3_DMA_CON	0x52000243	0x52000240			EP3 DMA Interface Control
EP3_DMA_UNIT	0x52000247	0x52000244			EP3 DMA Tx Unit Counter
EP3_DMA_FIFO	0x5200024b	0x52000248			EP3 DMA Tx FIFO Counter
EP3_DMA_TX_LO	0x5200024f	0x5200024c			EP3 DMA Total Tx Counter
EP3_DMA_TX_MD	0x52000253	0x52000250			EP3 DMA Total Tx Counter
EP3_DMA_TX_HI	0x52000257	0x52000254			EP3 DMA Total Tx Counter
EP4_DMA_CON	0x5200025b	0x52000258			EP4 DMA Interface Control
EP4_DMA_UNIT	0x5200025f	0x5200025c			EP4 DMA Tx Unit Counter
EP4_DMA_FIFO	0x52000263	0x52000260			EP4 DMA Tx FIFO Counter
EP4_DMA_TX_LO	0x52000267	0x52000264			EP4 DMA Total Tx Counter
EP4_DMA_TX_MD	0x5200026b	0x52000268			EP4 DMA Total Tx Counter
EP4_DMA_TX_HI	0x5200026f	0x5200026c			EP4 DMA Total Tx Counter

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
WATCHDOG TIMER					
WTCON	0x52000000	←	W	R/W	Watch-Dog Timer Mode
WTDAT	0x52000004				Watch-Dog Timer Data
WTCNT	0x52000008				Watch-Dog Timer Count
IIC					
IICCON	0x54000000	←	W	R/W	IIC Control
IICSTAT	0x54000004				IIC Status
IICADD	0x54000008				IIC Address
IICDS	0x5400000c				IIC Data Shift
IIS					
IISCON	0x55000000,02	0x55000000	HW,W	R/W	IIS Control
IISMOD	0x55000004,06	0x55000004	HW,W		IIS Mode
IISPSR	0x55000008,0a	0x55000008	HW,W		IIS Prescaler
IISFCON	0x5500000c,0e	0x5500000c	HW,W		IIS FIFO Control
IISFIF	0x55000012	0x55000010	HW		IIS FIFO Entry

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
I/O PORT					
GPACON	0x56000000	←	W	R/W	Port A Control
GPADAT	0x56000004				Port A Data
GPBCON	0x56000010				Port B Control
GPBDAT	0x56000014				Port B Data
GPBUP	0x56000018				Pull-up Control B
GPCCON	0x56000020				Port C Control
GPCDAT	0x56000024				Port C Data
GPCUP	0x56000028				Pull-up Control C
GPDCON	0x56000030				Port D Control
GPDDAT	0x56000034				Port D Data
GPDUP	0x56000038				Pull-up Control D
GPECON	0x56000040				Port E Control
GPEDAT	0x56000044				Port E Data
GPEUP	0x56000048				Pull-up Control E
GPFCON	0x56000050				Port F Control
GPFDAT	0x56000054				Port F Data
GPFUP	0x56000058				Pull-up Control F
GPGCON	0x56000060				Port G Control
GPGDAT	0x56000064				Port G Data
GPGUP	0x56000068				Pull-up Control G
GPHCON	0x56000070				Port H Control
GPHDAT	0x56000074				Port H Data
GPHUP	0x56000078				Pull-up Control H

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
I/O PORT(Continued)					
MISCCR	0x56000080	←	W	R/W	Miscellaneous Control
DCKCON	0x56000084				DCLK0/1 Control
EXTINT0	0x56000088				External Interrupt Control
EXTINT1	0x5600008c				External Interrupt Control
EXTINT2	0x56000090				External Interrupt Filter Control
EINTFLT0	0x56000094				External Interrupt Filter Control
EINTFLT1	0x56000098				External Interrupt Filter Control
EINTFLT2	0x5600009c				External Interrupt Filter Control
EINTFLT3	0x560000a0				External Interrupt Filter Control
EINTMASK	0x560000a4				External Interrupt Mask
EINTPEND0	0x560000a8				External Interrupt Pending
GSTATUS0	0x560000ac				External Pin Status
GSTATUS1	0x560000b0				External Pin Status

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
RTC					
RTCCON	0x57000043	0x57000040	B	R/W	RTC Control
TICINT	0x57000047	0x57000044			Tick time count
RTCALM	0x57000053	0x57000050			RTC Alarm Control
ALMSEC	0x57000057	0x57000054			Alarm Second
ALMMIN	0x5700005b	0x57000058			Alarm Minute
ALMHOUR	0x5700005f	0x5700005c			Alarm Hour
ALMDAY	0x57000063	0x57000060			Alarm Day
ALMMON	0x57000067	0x57000064			Alarm Month
ALMYEAR	0x5700006b	0x57000068			Alarm Year
RTCRST	0x5700006f	0x5700006c			RTC Round Reset
BCDSEC	0x57000073	0x57000070			BCD Second
BCDMIN	0x57000077	0x57000074			BCD Minute
BCDHOUR	0x5700007b	0x57000078			BCD Hour
BCDDAY	0x5700007f	0x5700007c			BCD Day
BCDDATE	0x57000083	0x57000080			BCD Date
BCDMON	0x57000087	0x57000084			BCD Month
BCDYEAR	0x5700008b	0x57000088			BCD Year
A/D CONVERTER					
ADCCON	0x58000000	←	W	R/W	ADC Control
ADCTSC	0x58000004				ADC Touch Screen Control
ADCDLY	0x58000008				ADC Start or Interval Delay
ADCDAT0	0x5800000c			R	ADC Conversion Data
ADCDAT1	0x58000010				ADC Conversion Data
SPI					
SPCON	0x59000000	←	W	R/W	SPI Control
SPSTA	0x59000004			R	SPI Status
SPPIN	0x59000008			R/W	SPI Pin Control
SPPRE	0x5900000c				SPI Baud Rate Prescaler
SPTDAT	0x59000010				SPI Tx Data
SPRDAT	0x59000014			R	SPI Rx Data

Table 1-3. S3C2410 Special Registers (Continued)

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
SD INTERFACE					
SDICON	0x5a000000	←	W	R/W	SDI Control
SDIPRE	0x5a000004				SDI Buad Rate Prescaler
SDICmdArg	0x5a000008				SDI Command Argument
SDICmdCon	0x5a00000c				SDI Command Control
SDICmdSta	0x5a000010			R/(C)	SDI Command Status
SDIRSP0	0x5a000014			R	SDI Response
SDIRSP1	0x5a000018				SDI Response
SDIRSP2	0x5a00001c				SDI Response
SDIRSP3	0x5a000020				SDI Response
SDIDTimer	0x5a000024			R/W	SDI Data / Busy Timer
SDIBSize	0x5a000028				SDI Block Size
SDIDatCon	0x5a00002c				SDI Data control
SDIDatCnt	0x5a000030			R	SDI Data Remain Counter
SDIDatSta	0x5a000034			R/(C)	SDI Data Status
SDIFSTA	0x5a000038			R	SDI FIFO Status
SDIDAT	0x5a00003f	0x5a00003c	B	R/W	SDI Data
SDIIntMsk	0x5a000040	←	W		SDI Interrupt Mask

IMPORTANT NOTES ABOUT S3C2410 SPECIAL REGISTERS

1. In the little endian mode, L. endian address must be used. In the big endian mode, B. endian address must be used.
2. The special registers have to be accessed by the recommended access unit.
3. All registers except ADC registers, RTC registers and UART registers must be read/written in word unit (32bit) at little/big endian.
4. It is very important that the ADC registers, RTC registers and UART registers be read/written by the specified access unit and the specified address. Moreover, one must carefully consider which endian mode is used.
5. W: 32-bit register, which must be accessed by LDR/STR or int type pointer(int *).

HW: 16-bit register, which must be accessed by LDRH/STRH or short int type pointer(short int *).
B: 8-bit register, which must be accessed by LDRB/STRB or char type pointer(char int *).

5 MEMORY CONTROLLER(Preliminary)

OVERVIEW

The S3C2410X01 memory controller provides the necessary memory control signals for external memory access. S3C2410X01 has the following features;

— Little/Big endian(selectable by a S/W)

— Address space: 128Mbytes per each bank (total 1GB:8 banks)

— Programmable access size(8/16/32-bit) for all banks except bank0(16/32-bit)

— Total 8 memory banks
6 memory banks for ROM, SRAM etc.
2 memory banks for ROM, SRAM, SDRAM etc .

— 7 fixed memory bank start address and programmble bank size

— 1 flexible memory bank start address and programmable bank size

— Programmable access cycles for all memory banks

— External wait to extend the bus cycles

— Supports self-refresh and power down mode in SDRAM

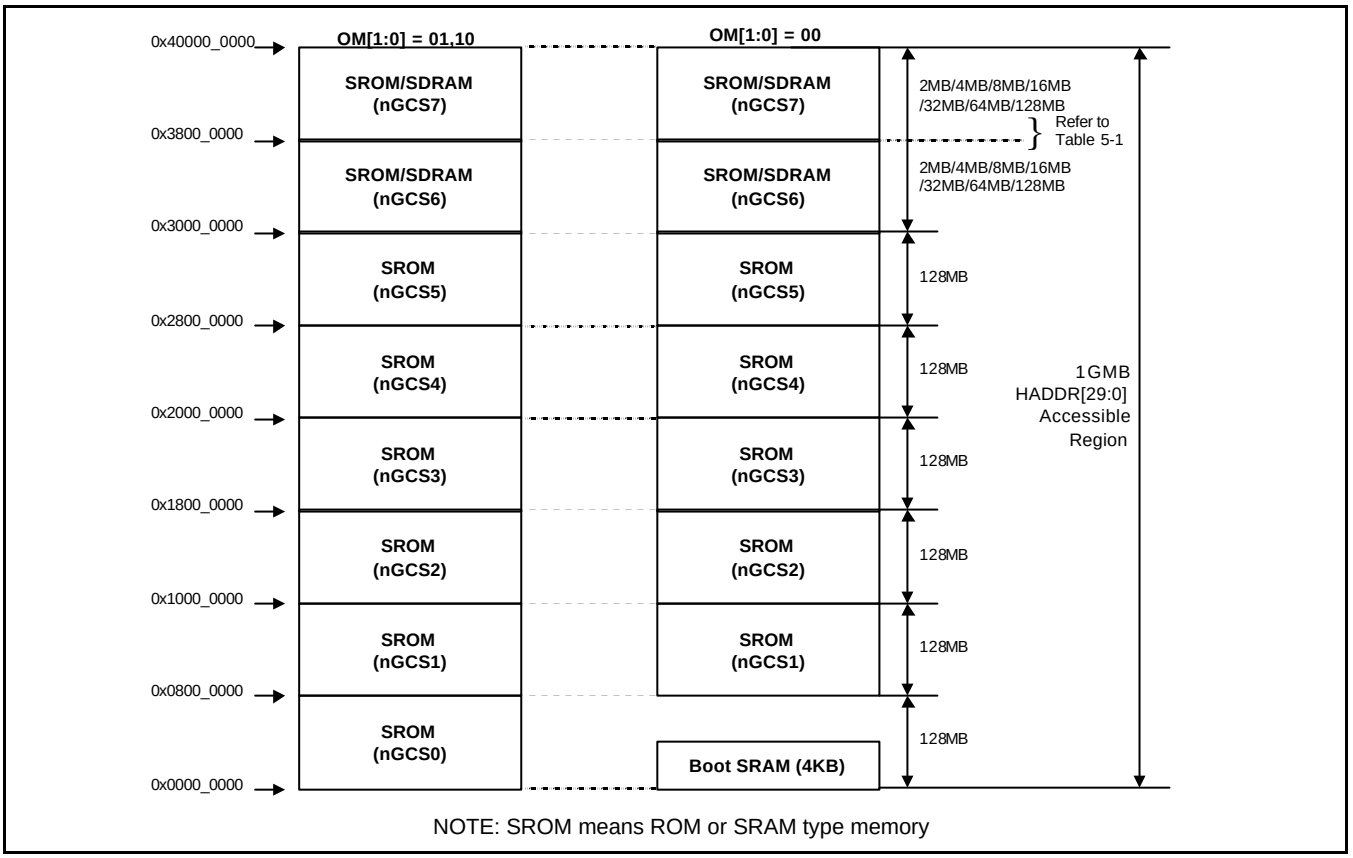


Figure 5-1. S3C2410X01 Memory Map after Reset

Table 5-1. Bank 6/7 Address

Address	2MB	4MB	8MB	16MB	32MB	64MB	128MB
Bank 6							
Start address	0x3000_0000	0x3000_0000	0x3000_0000	0x3000_0000	0x3000_0000	0x3000_0000	0x3000_0000
End address	0x301f_ffff	0x303f_ffff	0x307f_ffff	0x30ff_ffff	0x31ff_ffff	0x33ff_ffff	0x37ff_ffff
Bank 7							
Start address	0x3020_0000	0x3040_0000	0x3080_0000	0x3100_0000	0x3200_0000	0x3400_0000	0x3800_0000
End address	0x303f_ffff	0x307f_ffff	0x30ff_ffff	0x31ff_ffff	0x33ff_ffff	0x37ff_ffff	0x3fff_ffff

NOTE : Bank 6 and 7 must have the same memory size.

FUNCTION DESCRIPTION

BANK0 BUS WIDTH

The data bus width of BANK0 (nGCS0) should be configured as one of 16-bit and 32-bit. Because the BANK0 is the booting ROM bank(map to 0x0000_0000), the bus width of BANK0 should be determined before the first ROM access, which will be determined by the logic level of OM[1:0] at Reset.

OM1 (Operating Mode 1)	OM0 (Operating Mode 0)	Booting ROM Data width
0	0	Nand Flash Mode
0	1	16-bit
1	0	32-bit
1	1	Test Mode

MEMORY(SROM/SDRAM) ADDRESS PIN CONNECTIONS

MEMORY ADDR. PIN	S3C2410X01 ADDR. @ 8-bit DATA BUS	S3C2410X01 ADDR. @ 16-bit DATA BUS	S3C2410X01 ADDR. @ 32-bit DATA BUS
A0	A0	A1	A2
A1	A1	A2	A3
. . .	. . .	. . .	. . .

SDRAM BANK ADDRESS PIN CONNECTION

Table 5-2. SDRAM Bank Address configuration

Bank Size	Bus Width	Base Component	Memory Configuration	Bank Address
2MByte	x8	16Mbit	(1M x 8 x 2Bank) x 1	A20
	x16		(512K x 16 x 2B) x 1	
4MB	x8	16Mb	(2M x 4 x 2B) x 2	A21
	x16		(1M x 8 x 2B) x 2	
	x32		(512K x 16 x 2B) x 2	
8MB	x16	16Mb	(2M x 4 x 2B) x 4	A22
	x32		(1M x 8x 2B) x 4	
	x8	64Mb	(4M x 8 x 2B) x 1	
	x8		(2M x 8 x 4B) x 1	A[22:21]
	x16		(2M x 16 x 2B) x 1	A22
	x16		(1M x 16 x 4B) x 1	A[22:21]
	x32		(512K x 32 x 4B) x 1	
16MB	x32	16Mb	(2M x 4 x 2B) x 8	A23
	x8	64Mb	(8M x 4 x 2B) x 2	
	x8		(4M x 4 x 4B) x 2	A[23:22]
	x16		(4M x 8 x 2B) x 2	A23
	x16		(2M x 8 x 4B) x 2	A[23:22]
	x32		(2M x 16 x 2B) x 2	A23
	x32		(1M x 16 x 4B) x 2	A[23:22]
	x8	128Mb	(4M x 8 x 4B) x 1	
	x16		(2M x 16 x 4B) x 1	
32MB	x16	64Mb	(8M x 4 x 2B) x 4	A24
	x16		(4M x 4 x 4B) x 4	A[24:23]
	x32		(4M x 8 x 2B) x 4	A24
	x32		(2M x 8 x 4B) x 4	A[24:23]
	x16	128Mb	(4M x 8 x 4B) x 2	
	x32		(2M x 16 x 4B) x 2	
	x8	256Mb	(8M x 8 x 4B) x 1	
	x16		(4M x 16 x 4B) x 1	
64MB	x32	128Mb	(4M x 8 x 4B) x 4	A[25:24]
	x16	256Mb	(8M x 8 x 4B) x 2	
	x32		(4M x 16 x 4B) x 2	
	x8	512Mb	(16M x 8 x 4B) x 1	
128MB	x32	256Mbit	(8M x 8 x 4Bank) x 4	A[26:25]
	x8	512Mb	(32M x 4 x 4B) x 2	
	x16		(16M x 8 x 4B) x 2	

nWAIT PIN OPERATION

If the WAIT corresponding each memory bank is enabled, the nOE duration should be prolonged by the external nWAIT pin while the memory bank is active. nWAIT is checked from tacc-1. nOE will be deasserted at the next clock after sampling that nWAIT is high. nWE signal have same relation with nOE as 5-14..

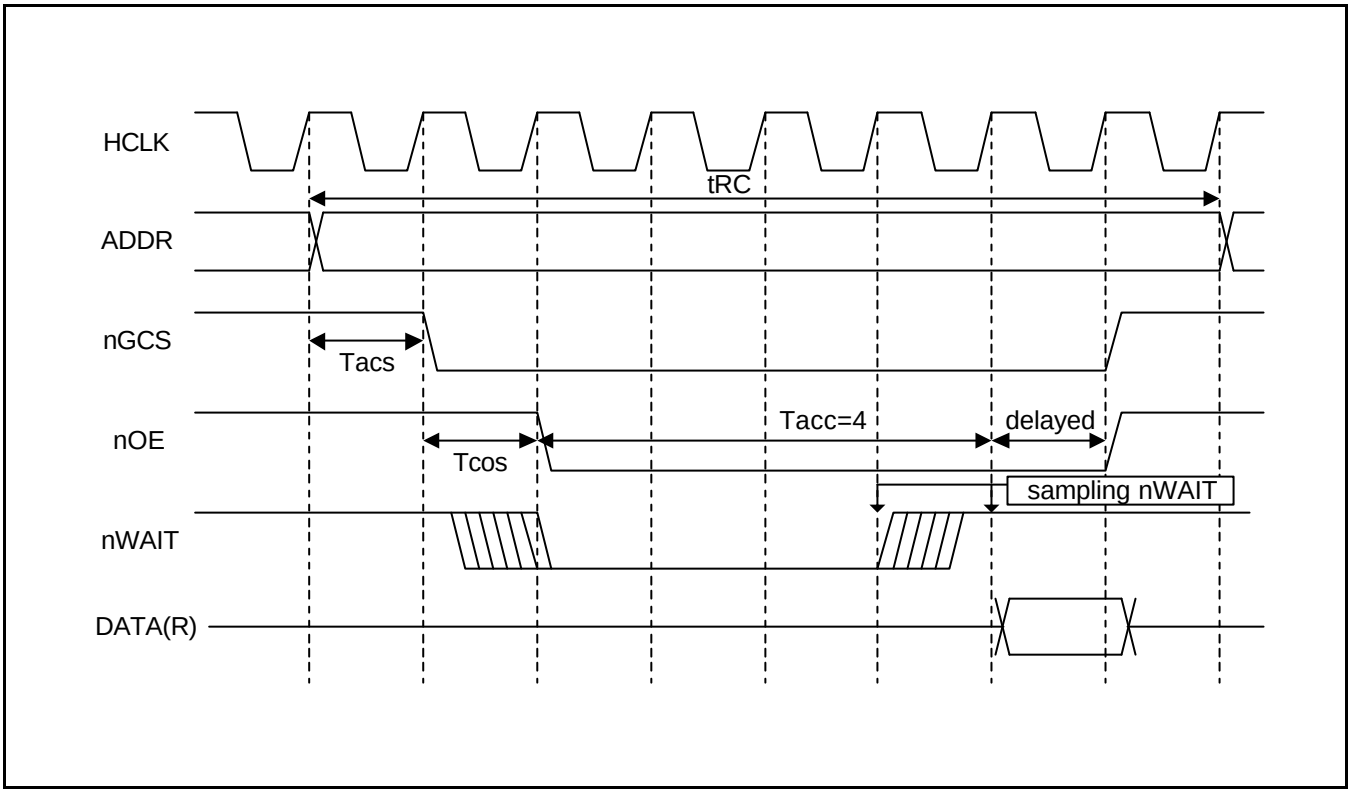


Figure 5-2. S3C2410X01 External nWAIT Timing Diagram.(Tacc=4)

nXBREQ/nXBACK Pin Operation

If nXBREQ is asserted, S3C2410X01 will respond by lowering nXBACK. If nXBACK=L, the address/data bus and memory control signals are in Hi-Z state as shown in Table 1-1. When nXBREQ is de-asserted, the nXBACK will be de-asserted.

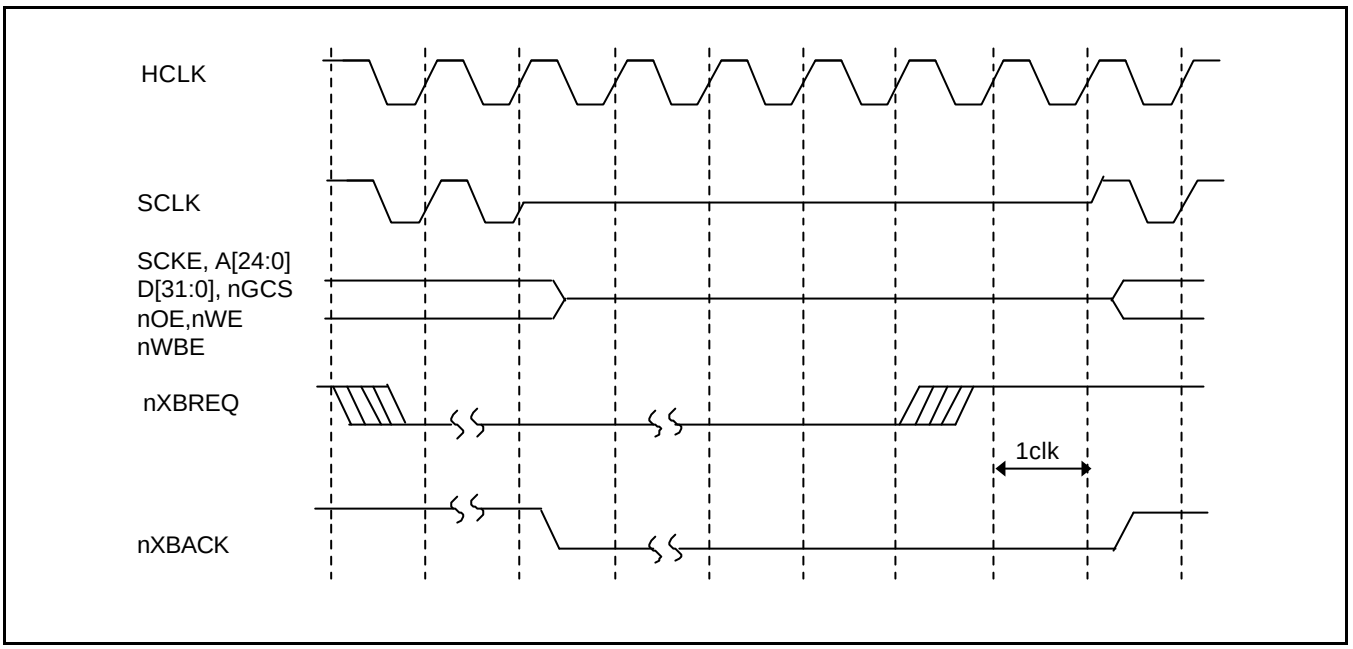


Figure 5-3. S3C2410X01 nXBREQ/nXBACK Timing Diagram.

ROM Memory Interface Example

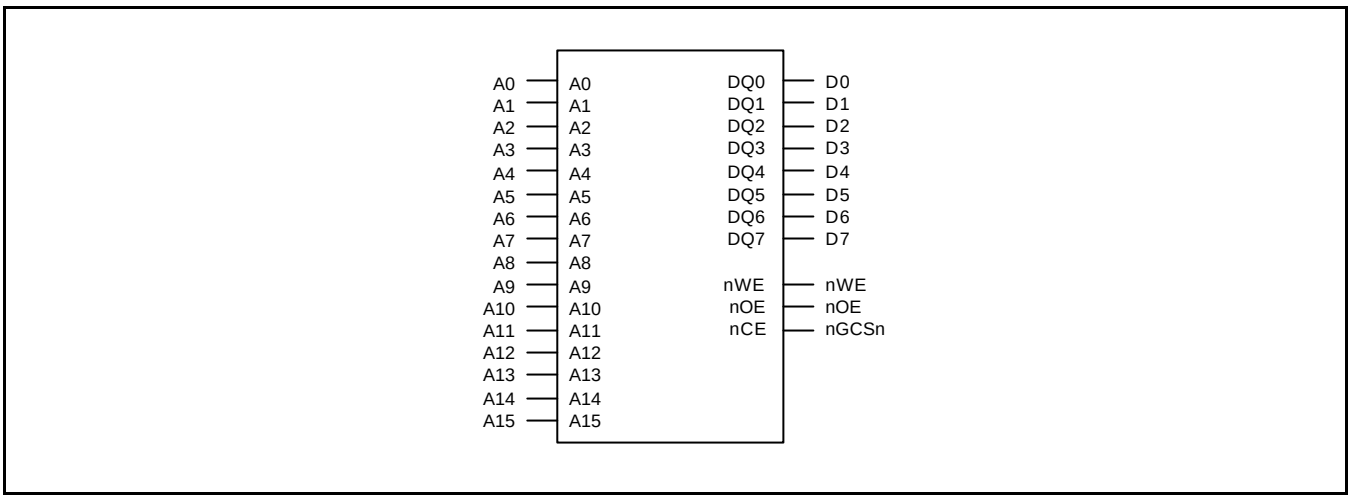


Figure 5-4. Memory Interface with 8bit ROM

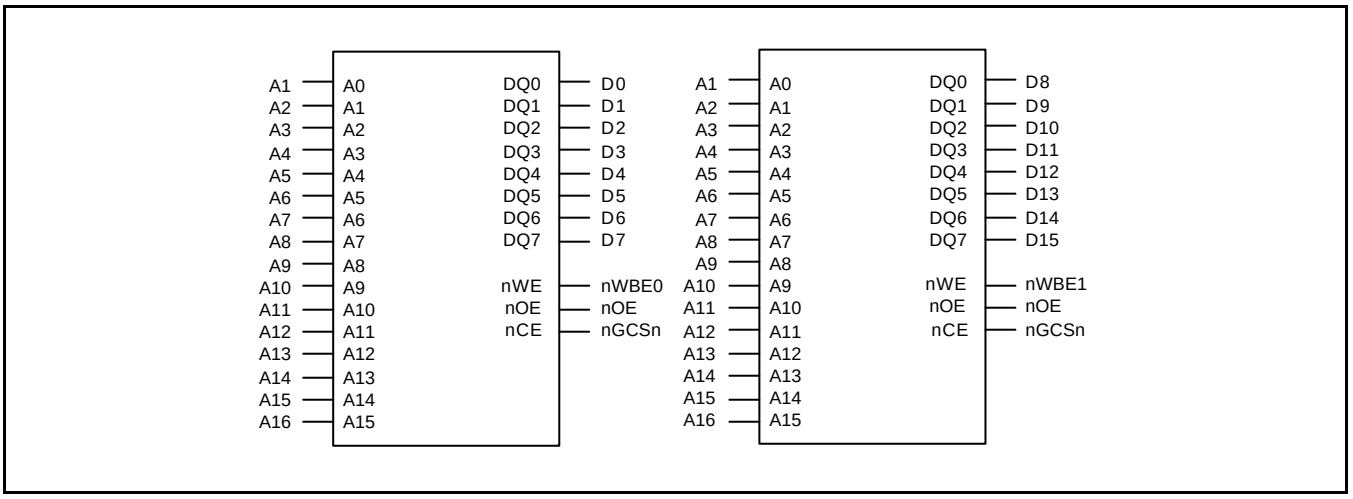


Figure 5-5. Memory Interface with 8bit ROM x 2

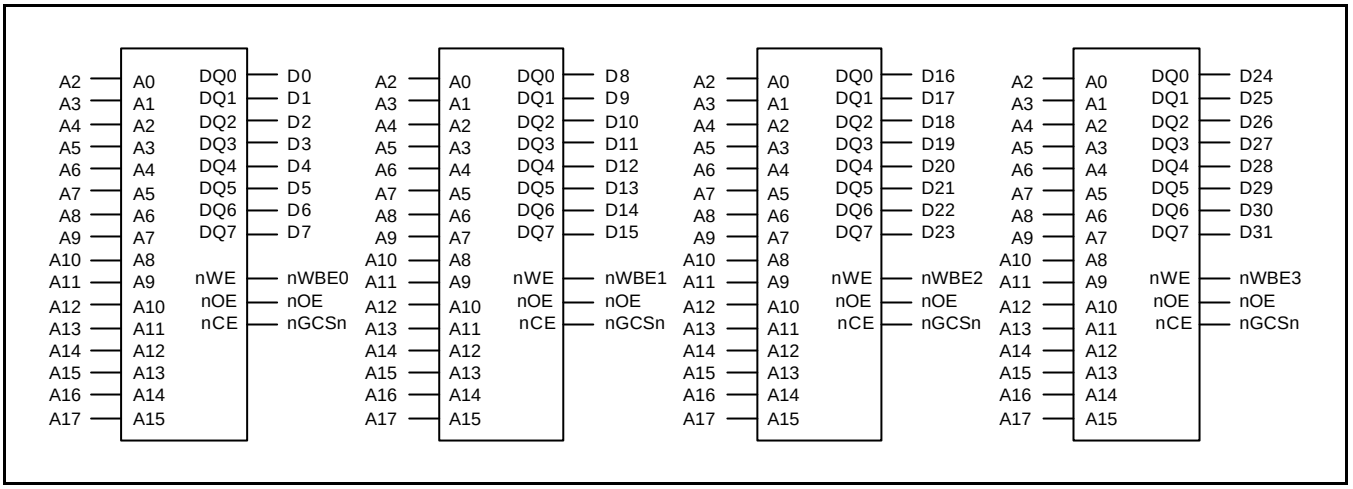


Figure 5-6. Memory Interface with 8bit ROM x 4

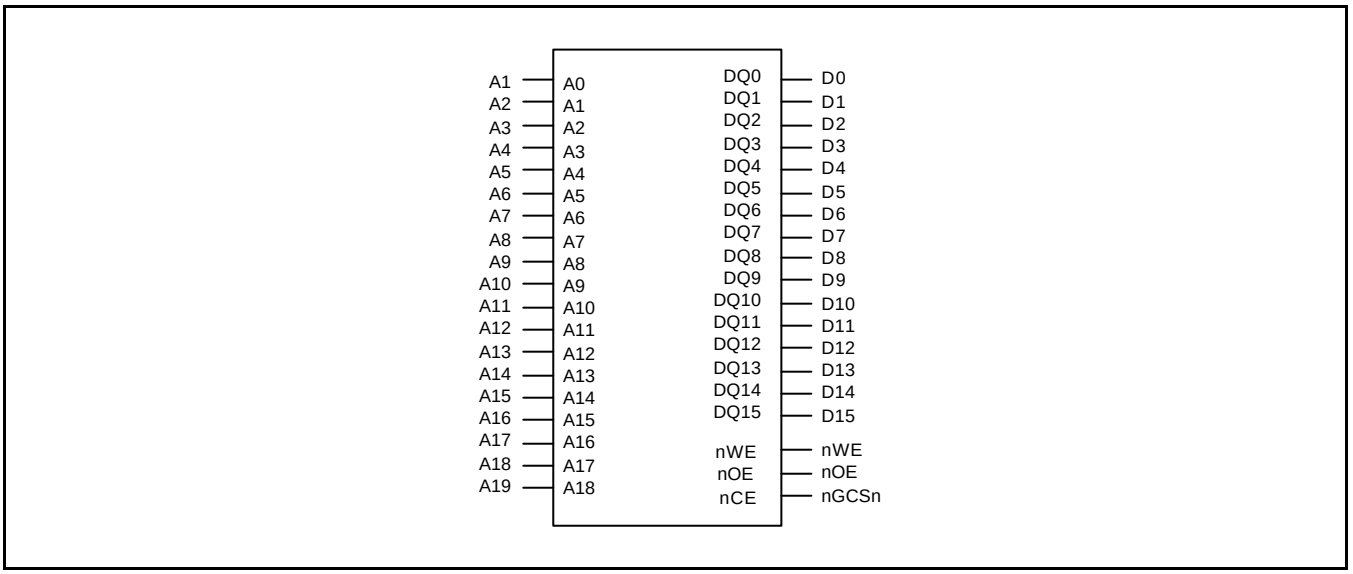


Figure 5-7. Memory Interface with 16bit ROM

SRAM Memory Interface Example

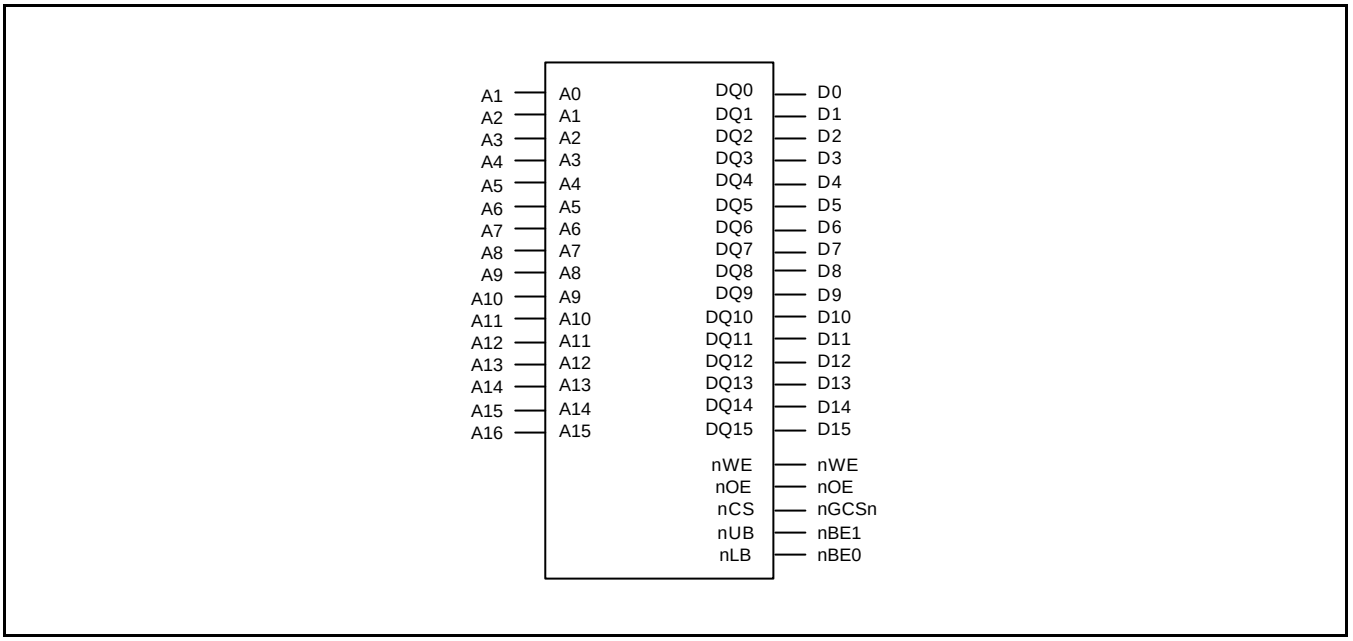


Figure 5-8. Memory Interface with 16bit SRAM

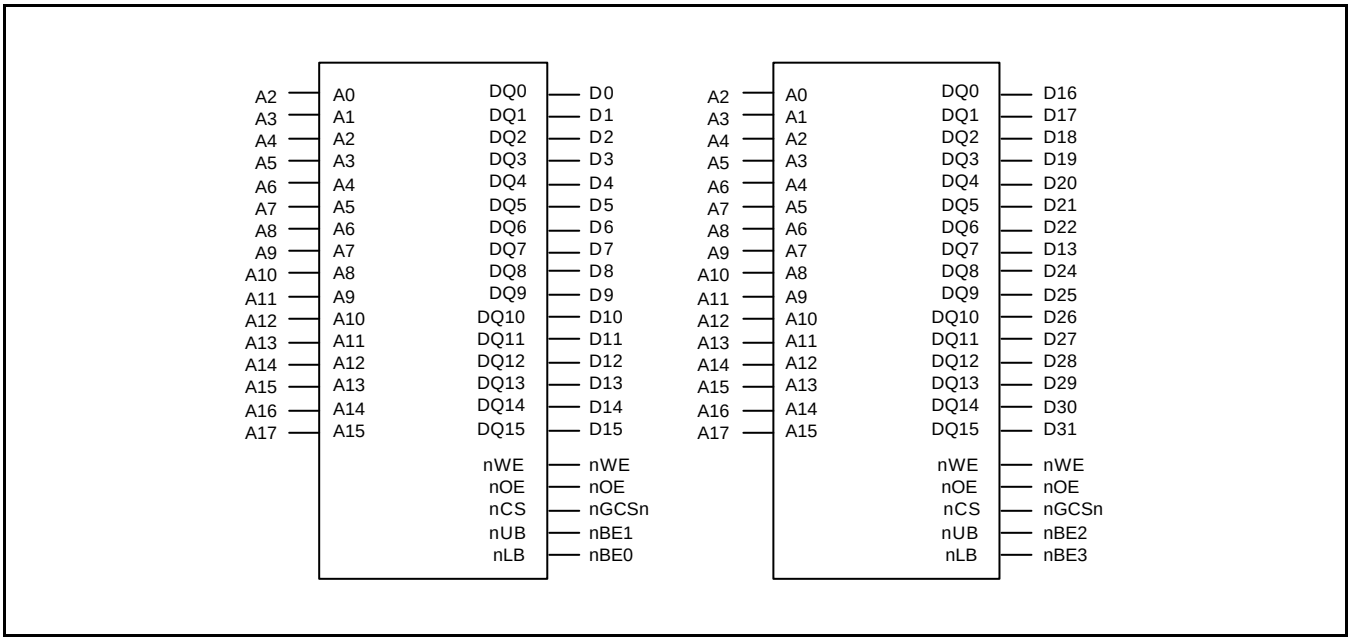


Figure 5-9. Memory Interface with 16bit SRAM x 2

SDRAM Memory Interface Example

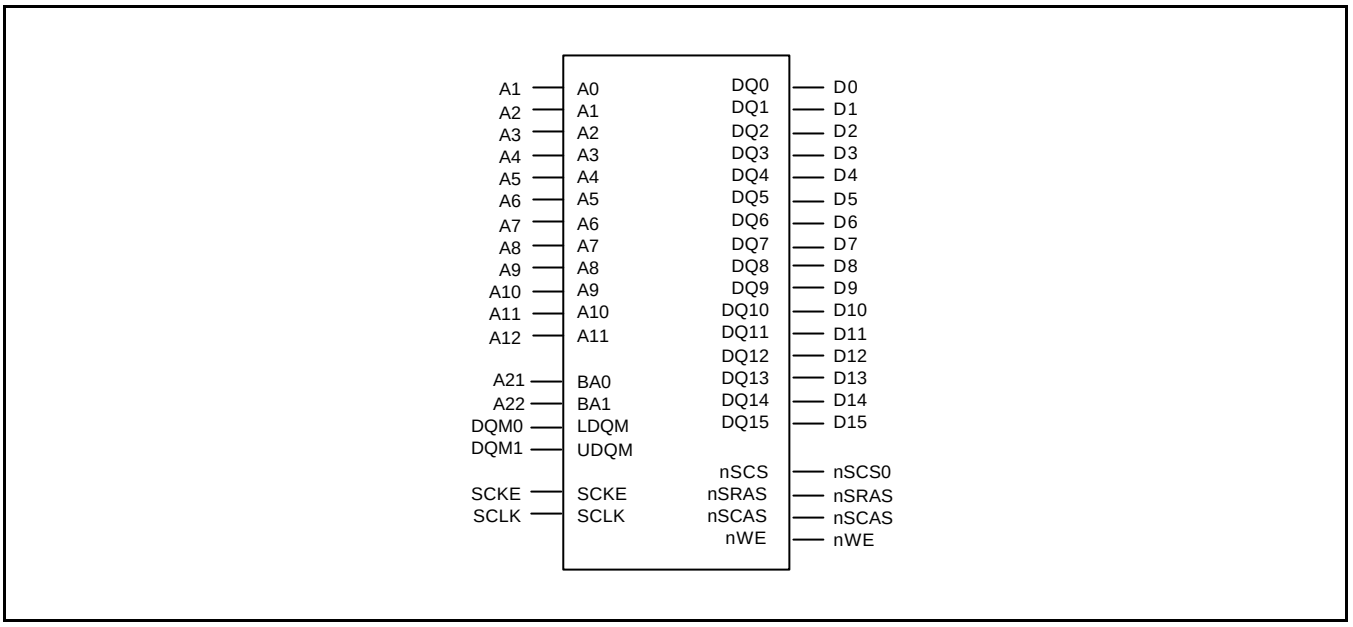


Figure 5-10. Memory Interface with 16bit SDRAM(4Mx16, 4bank)

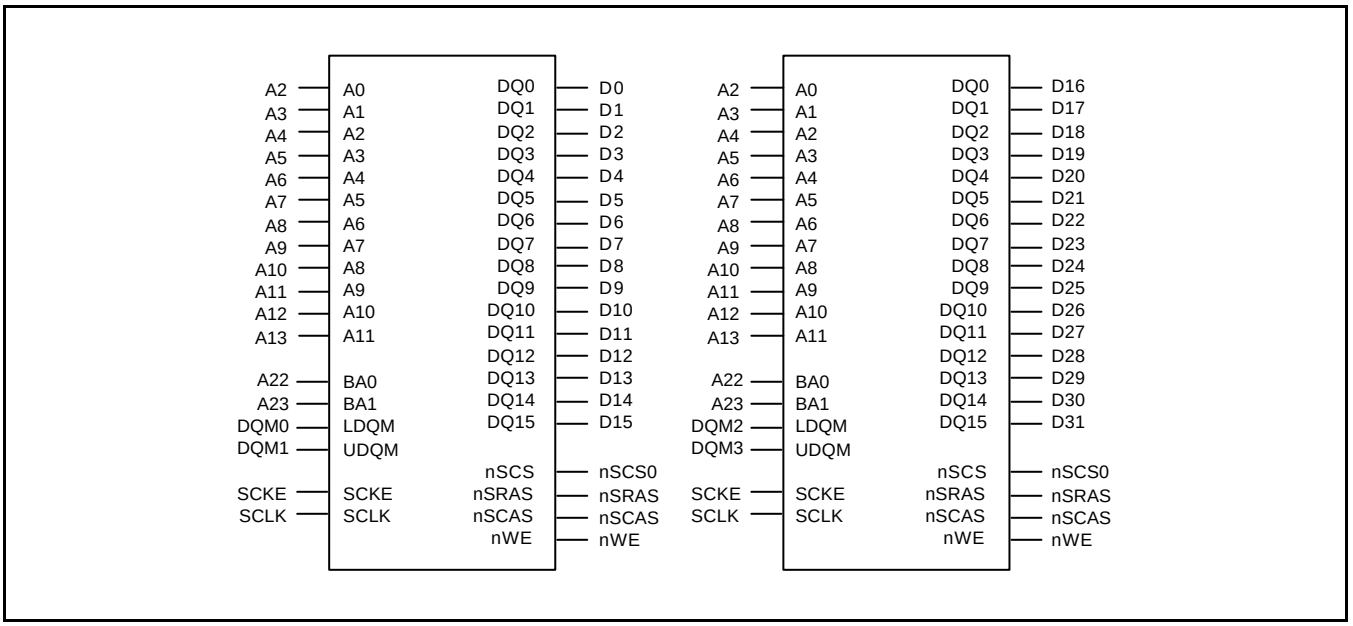


Figure 5-11. Memory Interface with 16bit SDRAM(4Mx16 * 2ea, 4bank)

NOTE : Please refer to Table 5-2 the Bank Address configurations of SDRAM.

PROGRAMMABLE ACCESS CYCLE

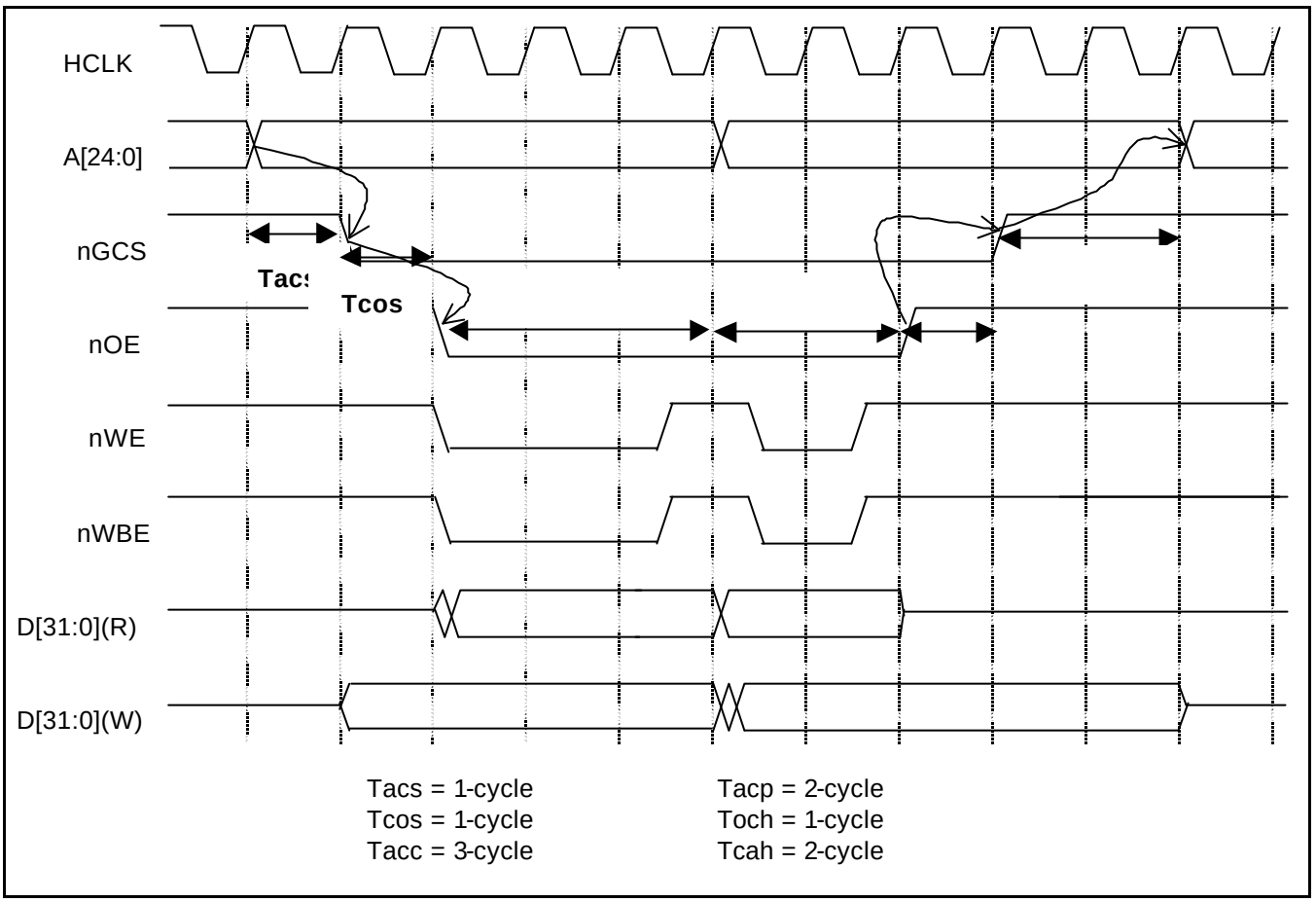


Figure 5-12. S3C2410X01 nGCS Timing Diagram.

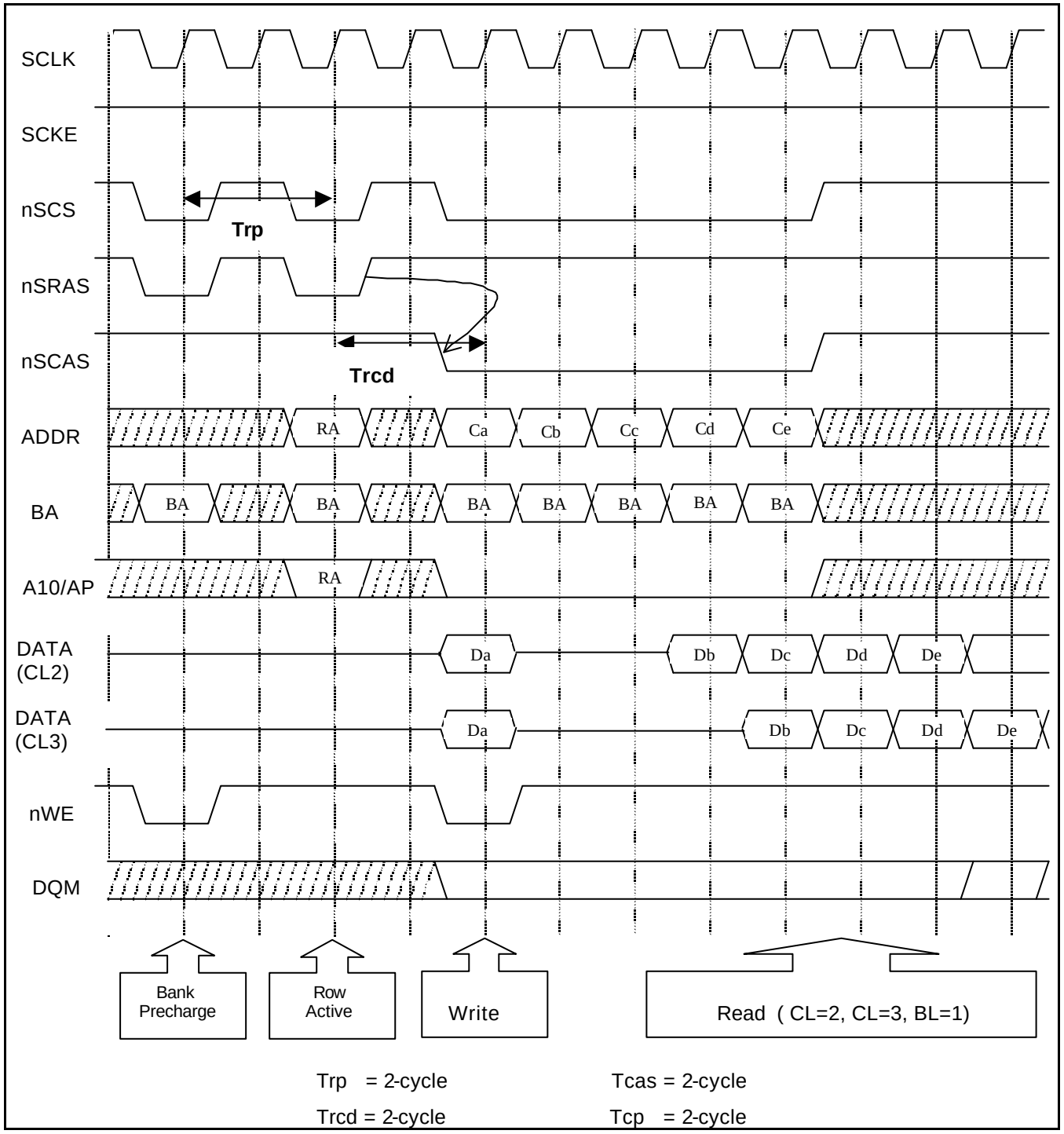


Figure 5-13. S3C2410X01 SDRAM Timing Diagram

BUS WIDTH & WAIT CONTROL REGISTER (BWSCON)

Register	Address	R/W	Description	Reset Value
BWSCON	0x48000000	R/W	Bus Width & Wait Status Control Register	0x000000

BWSCON	Bit	Description	Initial state
ST7	[31]	This bit determines SRAM for using UB/LB for bank 7 0 = Not using UB/LB (The pins are dedicated nWBE[3:0]) 1 = Using UB/LB (The pins are dedicated nBE[3:0])	0
WS7	[30]	This bit determines WAIT status for bank 7 0 = WAIT disable 1 = WAIT enable	0
DW7	[29:28]	These two bits determine data bus width for bank 7 00 = 8-bit 01 = 16-bit, 10 = 32-bit	0
ST6	[27]	This bit determines SRAM for using UB/LB for bank 6 0 = Not using UB/LB (The pins are dedicated nWBE[3:0]) 1 = Using UB/LB (The pins are dedicated nBE[3:0])	0
WS6	[26]	This bit determines WAIT status for bank 6 0 = WAIT disable, 1 = WAIT enable	0
DW6	[25:24]	These two bits determine data bus width for bank 6 00 = 8-bit 01 = 16-bit, 10 = 32-bit	0
ST5	[23]	This bit determines SRAM for using UB/LB for bank 5 0 = Not using UB/LB (The pins are dedicated nWBE[3:0]) 1 = Using UB/LB (The pins are dedicated nBE[3:0])	0
WS5	[22]	This bit determines WAIT status for bank 5 0 = WAIT disable, 1 = WAIT enable	0
DW5	[21:20]	These two bits determine data bus width for bank 5 00 = 8-bit 01 = 16-bit, 10 = 32-bit	0
ST4	[19]	This bit determines SRAM for using UB/LB for bank 4 0 = Not using UB/LB (The pins are dedicated nWBE[3:0]) 1 = Using UB/LB (The pins are dedicated nBE[3:0])	0
WS4	[18]	This bit determines WAIT status for bank 4 0 = WAIT disable 1 = WAIT enable	0
DW4	[17:16]	These two bits determine data bus width for bank 4 00 = 8-bit 01 = 16-bit, 10 = 32-bit	0
ST3	[15]	This bit determines SRAM for using UB/LB for bank 3 0 = Not using UB/LB (The pins are dedicated nWBE[3:0]) 1 = Using UB/LB (The pins are dedicated nBE[3:0])	0
WS3	[14]	This bit determines WAIT status for bank 3 0 = WAIT disable 1 = WAIT enable	0
DW3	[13:12]	These two bits determine data bus width for bank 3 00 = 8-bit 01 = 16-bit, 10 = 32-bit	0
ST2	[11]	This bit determines SRAM for using UB/LB for bank 2 0 = Not using UB/LB (The pins are dedicated nWBE[3:0]) 1 = Using UB/LB (The pins are dedicated nBE[3:0])	0

BUS WIDTH & WAIT CONTROL REGISTER (BWSCON)(Continued)

WS2	[10]	This bit determines WAIT status for bank 2 0 = WAIT disable 1 = WAIT enable	0
DW2	[9:8]	These two bits determine data bus width for bank 2 00 = 8-bit 01 = 16-bit, 10 = 32-bit	0
ST1	[7]	This bit determines SRAM for using UB/LB for bank 1 0 = Not using UB/LB (The pins are dedicated nWBE[3:0]) 1 = Using UB/LB (The pins are dedicated nBE[3:0])	0
WS1	[6]	This bit determines WAIT status for bank 1 0 = WAIT disable, 1 = WAIT enable	0
DW1	[5:4]	These two bits determine data bus width for bank 1 00 = 8-bit 01 = 16-bit, 10 = 32-bit	0
DW0	[2:1]	Indicates data bus width for bank 0 (read only) 01 = 16-bit, 10 = 32-bit The states are selected by OM[1:0] pins	-
Reserved	[0]		-

NOTE :

1. All types of master clock in this memory controller correspond to the bus clock.
   For example, HCLK in SRAM is same as the bus clock, and SCLK in SDRAM is also the same as the bus clock. In this chapter (Memory Controller), one clock means one bus clock.
2. nBE[3:0] is the 'AND' signal nWBE[3:0] and nOE

BANK CONTROL REGISTER (BANKCONn: nGCS0-nGCS5)

Register	Address	R/W	Description	Reset Value
BANKCON0	0x48000004	R/W	Bank 0 control register	0x0700
BANKCON1	0x48000008	R/W	Bank 1 control register	0x0700
BANKCON2	0x4800000C	R/W	Bank 2 control register	0x0700
BANKCON3	0x48000010	R/W	Bank 3 control register	0x0700
BANKCON4	0x48000014	R/W	Bank 4 control register	0x0700
BANKCON5	0x48000018	R/W	Bank 5 control register	0x0700

BANKCONn	Bit	Description	Initial State
Tacs	[14:13]	Address set-up time before nGCSn 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tcos	[12:11]	Chip selection set-up time before nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tacc	[10:8]	Access cycle 000 = 1 clock 001 = 2 clocks 010 = 3 clocks 011 = 4 clocks 100 = 6 clocks 101 = 8 clocks 110 = 10 clocks 111 = 14 clocks NOTE: When nWAIT signal is used, Tacc ≥ 4 clocks.	111
Toch	[7:6]	Chip selection hold time after nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	000
Tcah	[5:4]	Address holding time after nGCSn 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tacp	[3:2]	Page mode access cycle @ Page mode 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = 6 clocks	00
PMC	[1:0]	Page mode configuration 00 = normal (1 data) 01 = 4 data 10 = 8 data 11 = 16 data	00

BANK CONTROL REGISTER (BANKCONn: nGCS6-nGCS7)

Register	Address	R/W	Description	Reset Value
BANKCON6	0x4800001C	R/W	Bank 6 control register	0x18008
BANKCON7	0x48000020	R/W	Bank 7 control register	0x18008

BANKCONn	Bit	Description	Initial State
MT	[16:15]	These two bits determine the memory type for bank6 and bank7 00 = ROM or SRAM 01 = Reserved(Don't use) 10 = Reserved(Don't use) 11 = Sync. DRAM	11
Memory Type = ROM or SRAM [MT=00] (15-bit)			
Tacs	[14:13]	Address set-up time before nGCS 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tcos	[12:11]	Chip selection set-up time before nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tacc	[10:8]	Access cycle 000 = 1 clock 001 = 2 clocks 010 = 3 clocks 011 = 4 clocks 100 = 6 clocks 101 = 8 clocks 110 = 10 clocks 111 = 14 clocks	111
Toch	[7:6]	Chip selection hold time after nOE 00 = 0 clock 01 = 1 clock 10 = 2 clocks 11 = 4 clocks	00
Tcah	[5:4]	Address hold time after nGCSn 00 = 0 clock 01 = 1clock 10 = 2 clocks 11 = 4 clocks	00
Tacp	[3:2]	Page mode access cycle @ Page mode 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = 6 clocks	00
PMC	[1:0]	Page mode configuration 00 = normal (1 data) 01 = 4 consecutive accesses 10 = 8 consecutive accesses 11 = 16 consecutive accesses	00
Memory Type = SDRAM [MT=11] (4-bit)			
Trcd	[3:2]	RAS to CAS delay 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks	10
SCAN	[1:0]	Column address number 00 = 8-bit 01 = 9-bit 10= 10-bit	00

SUPPORTED BANK 6 / 7 MEMORY CONFIGURATION

Bank	Support		
Bank7	SROM	SDRAM	SDRAM

Bank6	SDRAM	SROM	SDRAM

NOTE : SROM means ROM or SRAM type memory

REFRESH CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
REFRESH	0x48000024	R/W	SDRAM refresh control register	0xac0000

REFRESH	Bit	Description	Initial State
REFEN	[23]	SDRAM Refresh Enable 0 = Disable 1 = Enable(self or CBR/auto refresh)	1
TREFMD	[22]	SDRAM Refresh Mode 0 = CBR/Auto Refresh 1 = Self Refresh In self-refresh time, the SDRAM control signals are driven to the appropriate level.	0
Trp	[21:20]	SDRAM RAS pre-charge Time 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = Not support	10
Trc	[19:18]	SDRAM RC minimum Time 00 = 4 clocks 01 = 5 clocks 10 = 6 clocks 11 = 7 clocks	11
Reserved	[17:16]	Not use	00
Reserved	[15:11]	Not use	0000
Refresh Counter	[10:0]	SDRAM refresh count value. Please, refer to chap. 6 SDRAM refresh controller bus priority section. Refresh period = (2^{11}-refresh_count+1)/HCLK Ex) If refresh period is 15.6 us and HCLK is 60 MHz, the refresh count is as follows; refresh count = 2^{11} + 1 - 60x15.6 = 1113	0

BANKSIZE REGISTER

Register	Address	R/W	Description	Reset Value
BANKSIZE	0x48000028	R/W	Flexible bank size register	0x0

BANKSIZE	Bit	Description	Initial State
SCLKE_EN	[5]	SDRAM power down mode enable control by SCKE 0 = SDRAM power down mode disable 1 = SDRAM power down mode enable	0
SCLK_EN	[4]	SCLK is enabled only during SDRAM access cycle for reducing power consumption. When SDRAM isn't be accessed, SCLK is 'L' level. 0 = SCLK is always active 1 = SCLK is active only during the access (recommended)	0
Reserved	[3]	Not use	0
BK76MAP	[2:0]	BANK6/7 memory map 010 = 128MB/128MB 001 = 64MB/64MB 000 = 32M/32M 111 = 16M/16M 110 = 8M/8M 101 = 4M/4M 100 = 2M/2M	010

SDRAM MODE REGISTER SET REGISTER (MRSR)

Register	Address	R/W	Description	Reset Value
MRSRB6	0x4800002C	R/W	Mode register set register bank6	xxx
MRSRB7	0x48000030	R/W	Mode register set register bank7	xxx

MRSR	Bit	Description	Initial State
Reserved	[11:10]	Not use	-
WBL	[9]	Write burst length 0 : Burst(Fixed) 1 : reserved	x
TM	[8:7]	Test mode 00: mode register set(Fixed) 01, 10, 11: reserved	xx
CL	[6:4]	CAS latency 000 = 1 clock, 010 = 2 clocks, 011=3 clocks the others : reserved	xxx
BT	[3]	Burst type 0: sequential(Fixed) 1: reserved	x
BL	[2:0]	Burst length 000: 1(Fixed) the others : reserved	xxx

NOTE : MRSR register must not be reconfigured while the code is running on SDRAM.

IMPORTANT NOTE : In STOP mode/SL_IDLE mode, SDRAM has to enter the SDRAM self-refresh mode.

6 CLOCK & POWER MANAGEMENT (Preliminary)

OVERVIEW

The clock & power management unit consists of 3 parts, clock control, USB control, and power control.

The Clock control logic in S3C2410X01 can generate the required clock signals, FCLK for CPU, HCLK for the AHB bus peripherals, and PCLK for the APB bus peripherals. There are two PLL in S3C2410X01. One is for FCLK,HCLK, and PCLK, the other is dedicated for USB block(48Mhz). The clock control logic can make slow clock without PLL and connect/disconnect the clock to each peripheral block by S/W, which will reduce the power consumption.

In the power control logic, S3C2410X01 has various power management schemes to keep optimal power consumption for a given task. The power management in S3C2410X01 consists of five modes : NORMAL mode, SLOW mode, IDLE mode and STOP mode.

NORMAL mode is used to supply clocks to CPU as well as all peripherals in S3C2410X01. In this case, the power consumption will be maximized when all peripherals are turned on. The user can control the operation of peripherals by S/W. For example, if a timer is not needed, the user can disconnect the clock to the timer to reduce power.

SLOW mode is non-PLL mode. Unlike the Normal mode, the Slow mode uses an external clock(XTIpll or EXTCLK) directly as FCLK in S3C2410X01 without PLL. In this case, the power consumption depends on the frequency of the external clock only. The power consumption due to PLL itself is excluded.

IDLE mode disconnects the clock(FCLK) only to CPU core while it supplies the clock to all peripherals. By using IDLE mode, power consumption due to CPU core can be reduced. Any interrupt request to CPU can wake-up from Idle mode.

STOP mode freezes all clocks to the CPU as well as peripherals by disabling PLLs. The power consumption is only due to the leakage current in S3C2410X01, which is uA unit. The wake-up from STOP mode can be done by activating external interrupt pins or RTC alarm.

FUNCTION DESCRIPTION

CLOCK ARCHITECTURE

Figure 6-1 shows a block diagram of the clock architecture. The main clock source comes from an external crystal(XTIpll) or external clock(EXTCLK). The clock generator consists of an oscillator block(Oscillation Amplifier) which is connected to an external crystal, and also has two PLLs (Phase-Locked-Loop) which generate the high frequency clock required in S3C2410X01.

CLOCK SOURCE SELECTION

Table 6-1 shows the relationship between the combination of mode control pins (OM3 and OM2) and the selection of source clock for S3C2410X01. The OM[3:2] status is latched internally by referring the OM3 and OM2 pins at the rising edge of nRESET.

Table 6-1. Clock source selection at boot-up

Mode OM[3:2]	MPLL state	UPLL state	Main Clock source	USB Clock source
00	On	On	Crystal	Crystal
01	On	On	Crystal	EXTCLK
10	On	On	EXTCLK	Crystal
11	On	On	EXTCLK	EXTCLK

NOTES.

1. Although the MPLL starts just after a reset, the MPLL output(Mpll) isn't used as the system clock until the S/W writes valid settings to the MPLLCON register. Before this valid setting, the clock from external crystal or EXTCLK source will be used as the system clock directly. Even if the user wants to maintain the default value of MPLLCON register, the user should write the same value into MPLLCON register.

2. OM[3:2] is used to determine test mode when OM[1:0] is 11.

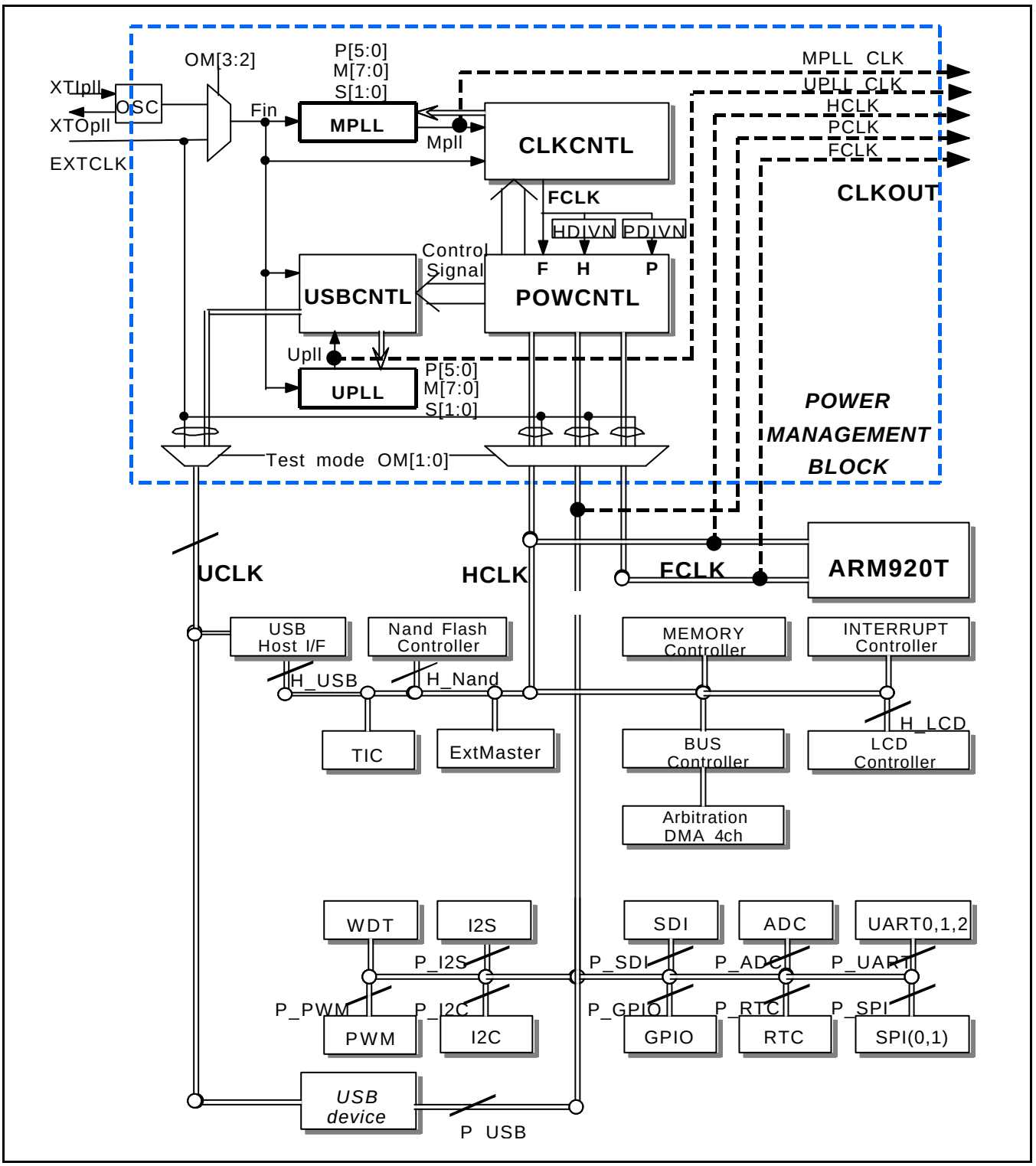


Figure 6-1. Clock Generator Block Diagram

PLL (PHASE-LOCKED-LOOP)

The MPLL within the clock generator is the circuit which synchronizes an output signal with a reference input signal in frequency and phase. In this application, it includes the following basic blocks (Figure 6-2 shows the clock generator block diagram); the VCO(Voltage Controlled Oscillator) to generate the output frequency proportional to input DC voltage, the divider P to divide the input frequency(Fin) by p, the divider M to divide the VCO output frequency by m which is input to PFD(Phase Frequency Detector), the divider S to divide the VCO output frequency by s which is Mpll(the output frequency from MPLL block), the phase difference detector, charge pump, and loop filter. The output clock frequency Mpll is related to the reference input clock frequency Fin by the following equation:

$$Mpll = (m * Fin) / (p * 2^s)$$

m = M (the value for divider M)+ 8, p = P(the value for divider P) + 2

The UPLL within the clock generator is same as the MPLL in every aspect.

The following sections describe the operation of the PLL, that includes the phase difference detector, charge pump, VCO (Voltage controlled oscillator), and loop filter.

Phase Difference Detector(PFD)

The PFD monitors the phase difference between the Fref (the reference frequency as shown in Fig. 6-2) and Fvco, and generates a control signal(tracking signal) when it detects a difference.

Charge Pump(PUMP)

The charge pump converts the PFD control signal into a proportional charge in voltage across the external filter that drives the VCO.

Loop Filter

The control signal that the PFD generates for the charge pump, may generate large excursions(ripples) each time the Fvco is compared to the Fref. To avoid overloading the VCO, a low pass filter samples and filters the high-frequency components out of the control signal. The filter is typically a single-pole RC filter consisting of a resistor and capacitor.

A recommended capacitance in the external loop filter(Capacitance as shown in Figure 6-2) is TBD pF or above.

Voltage Controlled Oscillator (VCO)

The output voltage from the loop filter drives the VCO, causing its oscillation frequency to increase or decrease linearly as a function of variations in average voltage. When the Fvco matches Fref in terms of frequency as well as phase, the PFD stops sending a control signal to the charge pump, which in turn stabilizes the input voltage to the loop filter. The VCO frequency then remains constant, and the PLL remains locked onto the system clock.

Usual Conditions for PLL & Clock Generator

The following conditions are generally used.

Loop filter capacitance	5 pF
External X-tal frequency	10 ~ 20 Mhz *
External capacitance used for X-tal	15 ~ 22 pF

* Value could be changed.

** FCLK must be more than three times X-tal or EXTCLK (FCLK ≥ 3X-tal or 3EXTCLK)

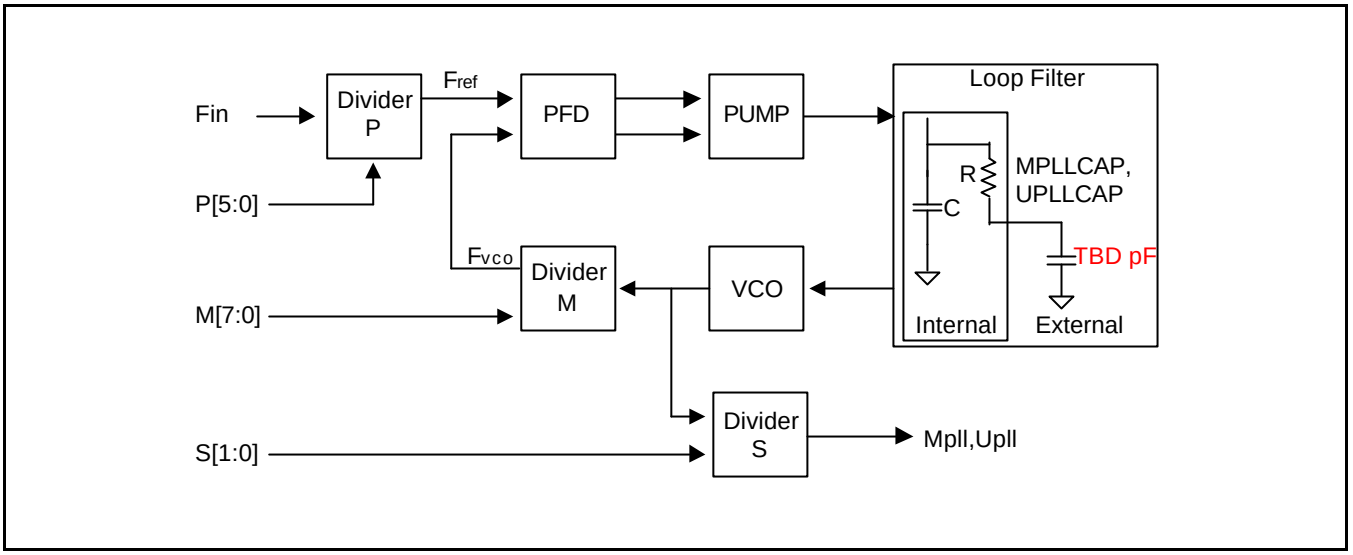


Figure 6-2. PLL (Phase-Locked Loop) Block Diagram

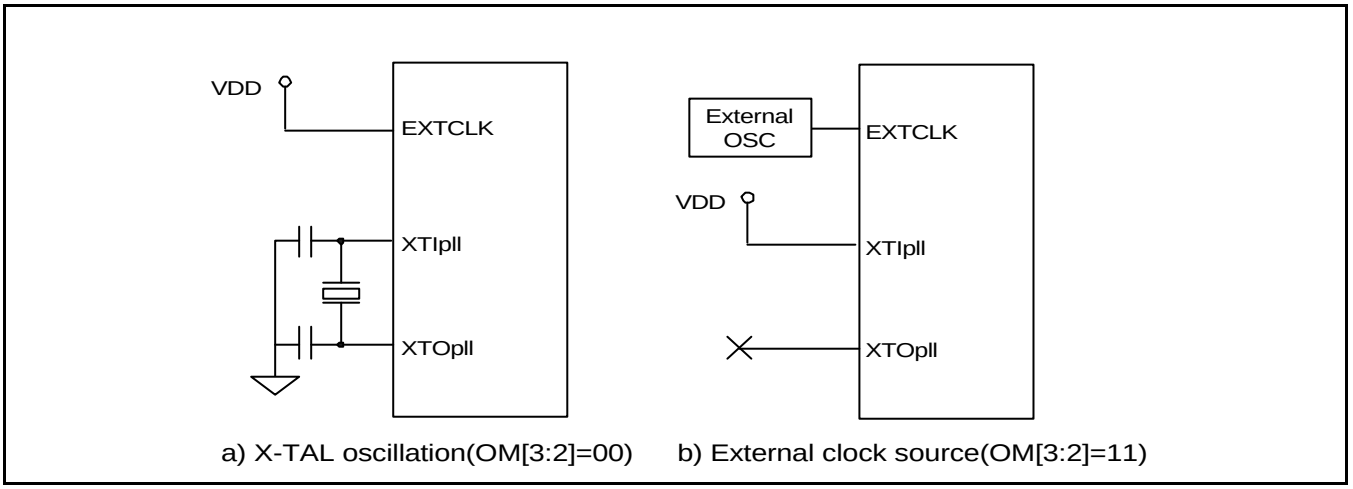


Figure 6-3. Main Oscillator Circuit Examples

CLOCK CONTROL LOGIC

The clock control logic determines the clock source to be used, i.e., the PLL clock(Mpll) or the direct external clock(XTIpll or EXTCLK). When PLL is configured to a new frequency value, the clock control logic disables the FCLK until the PLL output is stabilized using the PLL locking time. The clock control logic is also activated at power-on reset and wake-up from power-down mode.

PLL Lock Time

The lock time is the minimum time required for PLL output stabilization. The lock time should be a minimum of 150us. After reset and wake-up from STOP mode, respectively, the lock-time is inserted automatically by the internal logic with lock time count register. The automatically inserted lock time is calculated as follows;

t_lock(the PLL lock time by H/W logic) = (1/ Fin) x n, (n = M_LTIME,U_LTIME value)

Power-On Reset(XTIpll)

Figure 6-4 shows the clock behavior during the power-on reset sequence. The crystal oscillator begins oscillation within several milliseconds. When nRESET is released after the stabilization of OSC(XTIpll) clock, the PLL starts to operate according to the default PLL configuration. However PLL is commonly known to be unstable after power-on reset, so Fin fed directly to FCLK instead of the Mpll(PLL output) before the S/W newly configures the PLLCON. Even if the user wants to use the default value of PLLCON register after reset, user should write the same value into PLLCON register by S/W.

The PLL begins the lockup sequence again toward the new frequency only after the S/W configures the PLL with a new frequency. FCLK can be configured to be PLL output (Mpll) immediately after lock time.

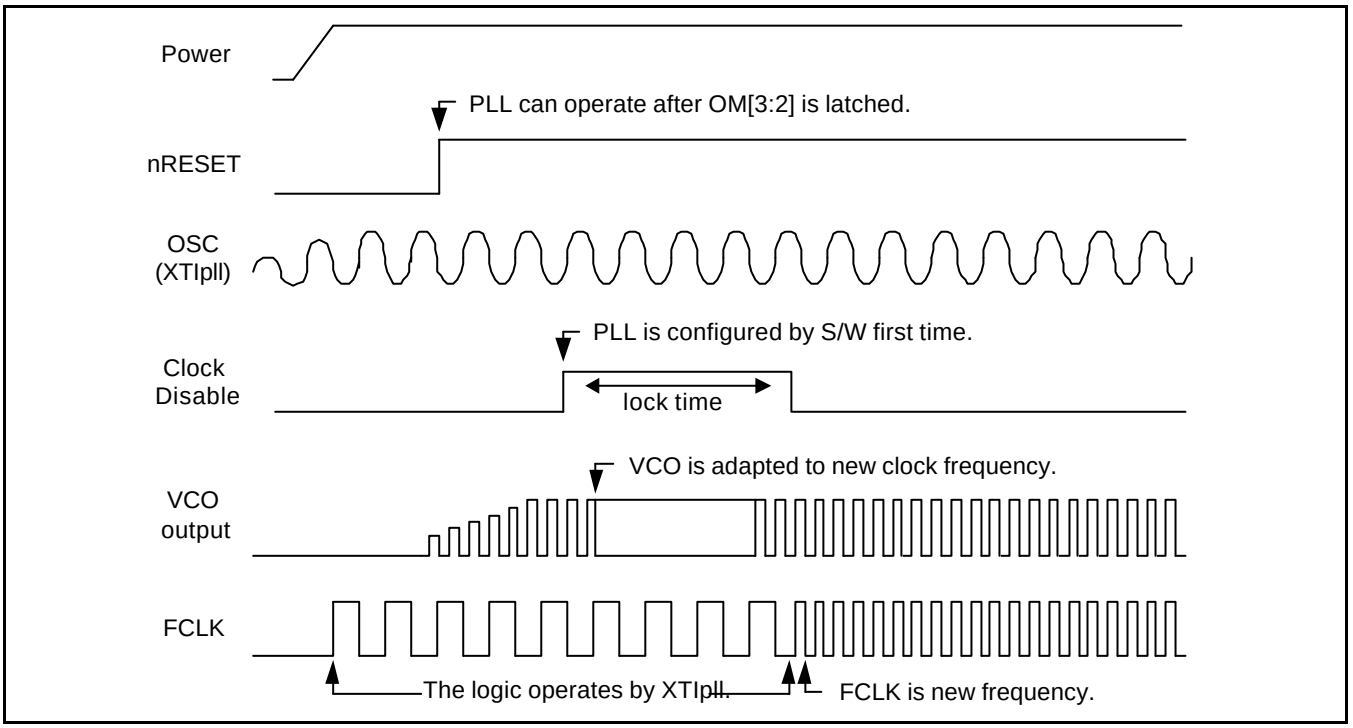


Figure 6-4. Power-On Reset Sequence(When the external clock source is a crystal oscillator.)

Change PLL Settings In Normal Operation Mode

During the operation of S3C2410X01 in NORMAL mode, if the user wants to change the frequency by writing the PMS value, the PLL lock time is automatically inserted. During the lock time, the clock is not supplied to the internal blocks in S3C2410X01. The timing diagram is as follow.

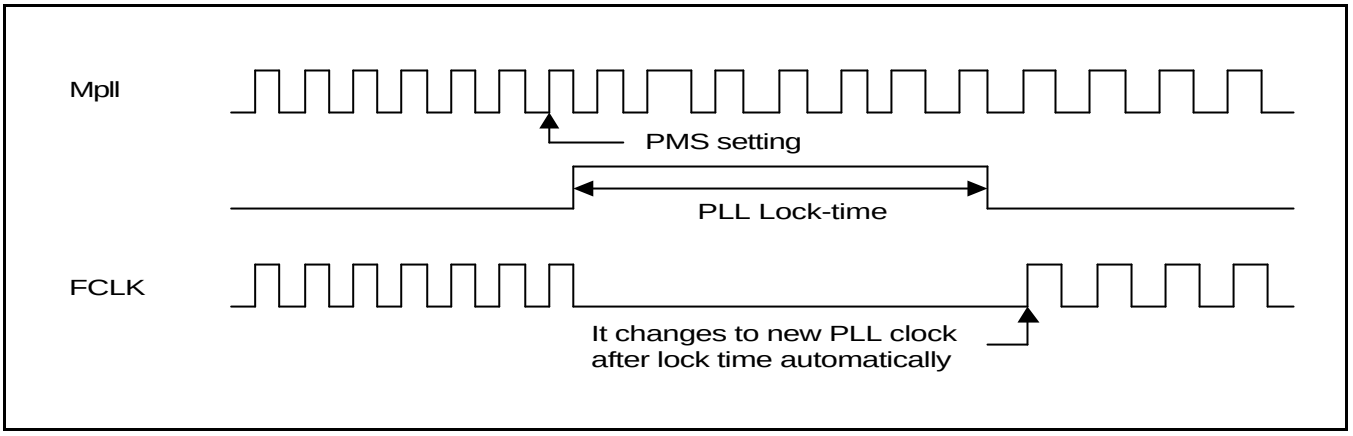
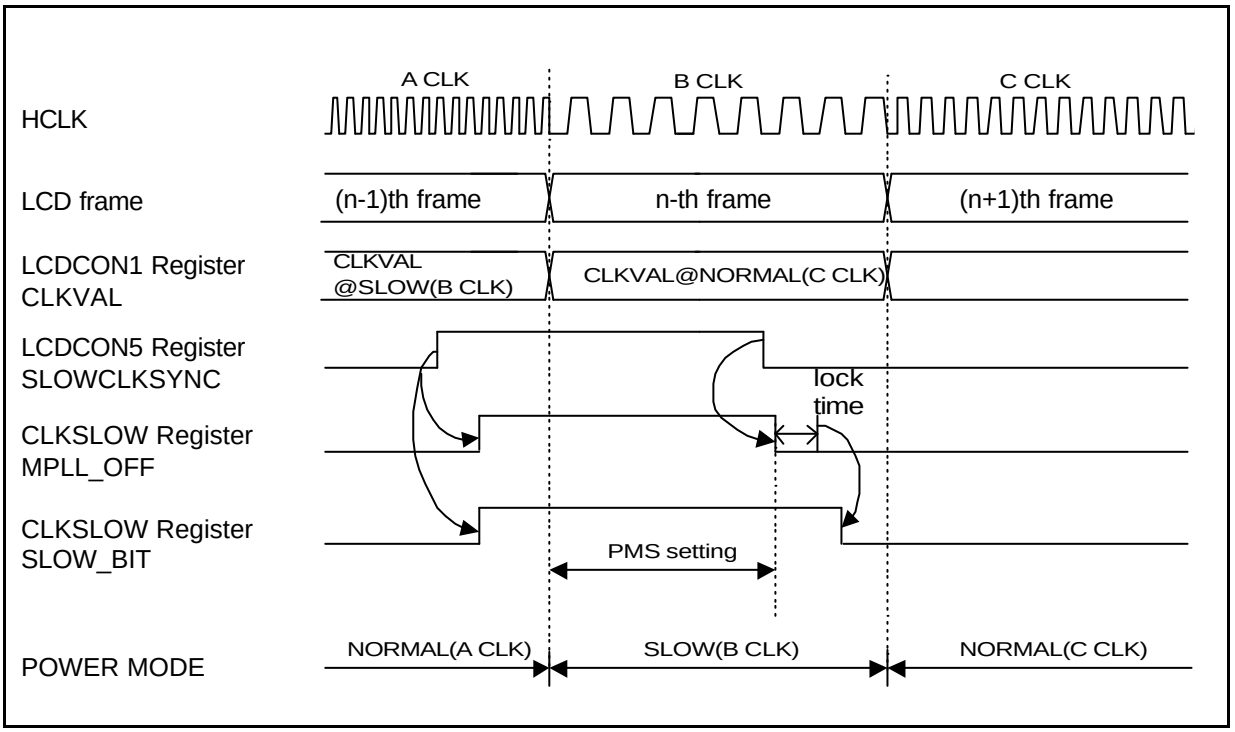


Figure 6-5. The case that changes Slow clock by setting PMS value

NOTE: Changing PMS value can cause problem in LCD display. Because changed PMS value means changed CLKVAL of LCD control register. In this case, the user has to use SLOW mode like the below.



FCLK, HCLK, PCLK

FCLK is used by ARM920T.
HCLK is used for AHB bus which is used by ARM920T, the memory controller, the interrupt controller, LCD controller, the DMA and the USB host block.
PCLK is used for APB bus which is used by the peripherals such as WDT,IIS,I2C,PWM timer, MMC interface, ADC, UART, GPIO, RTC and SPI.

S3C2410X01 supports selection of Dividing Ratio between FCLK, HLCK and PCLK. This ratio is determined by HDIVN and PDIVN of CLKDIVN control register.

HDIVN	PDIVN	FCLK	HCLK	PCLK	Divide Ratio
0	**0**	FCLK	FCLK	FCLK	1 : 1 : 1(Default)
0	**1**	FCLK	FCLK	FCLK / 2	1 : 1 : 2
1	**0**	FCLK	FCLK / 2	FCLK / 2	1 : 2 : 2
1	**1**	FCLK	FCLK / 2	FCLK / 4	1 : 2 : 4

When PMS value is set, CLKDIVN register should be set after PMS setting. This setting value of CLKDIVN is valid after PLL Lock-time. Which is also available for reset and changing Power Management Mode.
In other case, the setting value of CLKDIVN register is valid after 1.5 HCLK. But 1HCLK can be validated the value of CLKDIVN register changed from Default(1:1:1) to other Divide Ratio(1:1:2, 1:2:2 and 1:2:4)

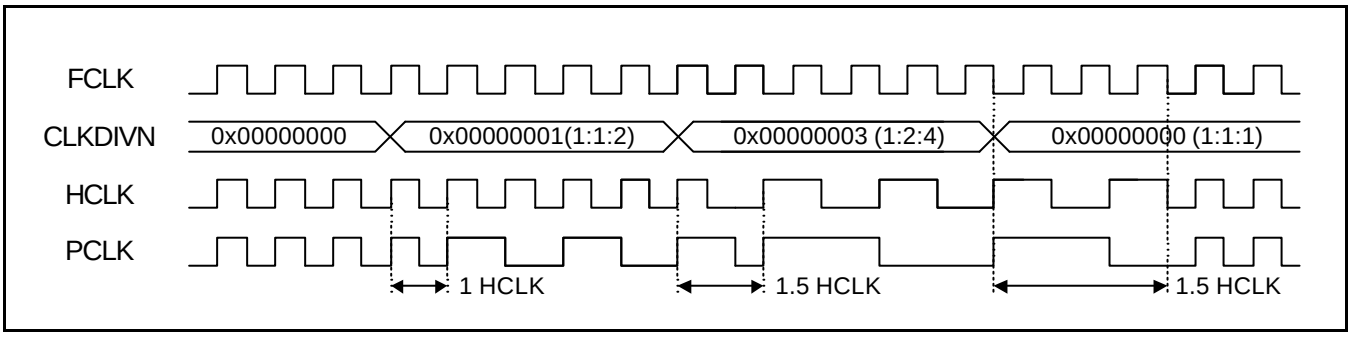


Figure 6-6. Example that changes CLKDIVN register value

NOTE : CLKDIVN should be set carefully not to exceed the limit of HCLK & PCLK.

USB Clock Control

USB host interface and USB device interface needs 48Mhz clock. In S3C2410X01, The USB dedicated PLL(UPLL) generates 48Mhz for USB. UCLK doesn't fed until the PLL(UPLL) is configured. USB PLL(UPLL) will be turned off during STOP mode automatically. Also, USB PLL(UPLL) will be turned on after exiting STOP mode if UCLK_ON bit is enabled in CLKSLOW register.

Condition	UCLK state	UPLL state
After reset	XTI_{PLL} or EXTCLK	on
After configuring UPLL	L : during PLL lock time 48Mhz: after PLL lock time	on
UPLL is turned off by CLKSLOW register	XTI_{PLL} or EXTCLK	off

UPLL is turned on by CLKSLOW register	48Mhz	on

POWER MANAGEMENT

The power management block controls the system clocks by software for the reduction of power consumption in S3C2410X01. These schemes are related to PLL, clock control logic(FCLK,HCLK,PCLK) and wake-up signal. The Figure 6-7 depicts the clock distribution of S3C2410X01.

S3C2410X01 has five power-down modes. The following section describes each power managing mode. The transition between the modes is not allowed freely. For available transitions among the modes, please refer to Figure 6-8.

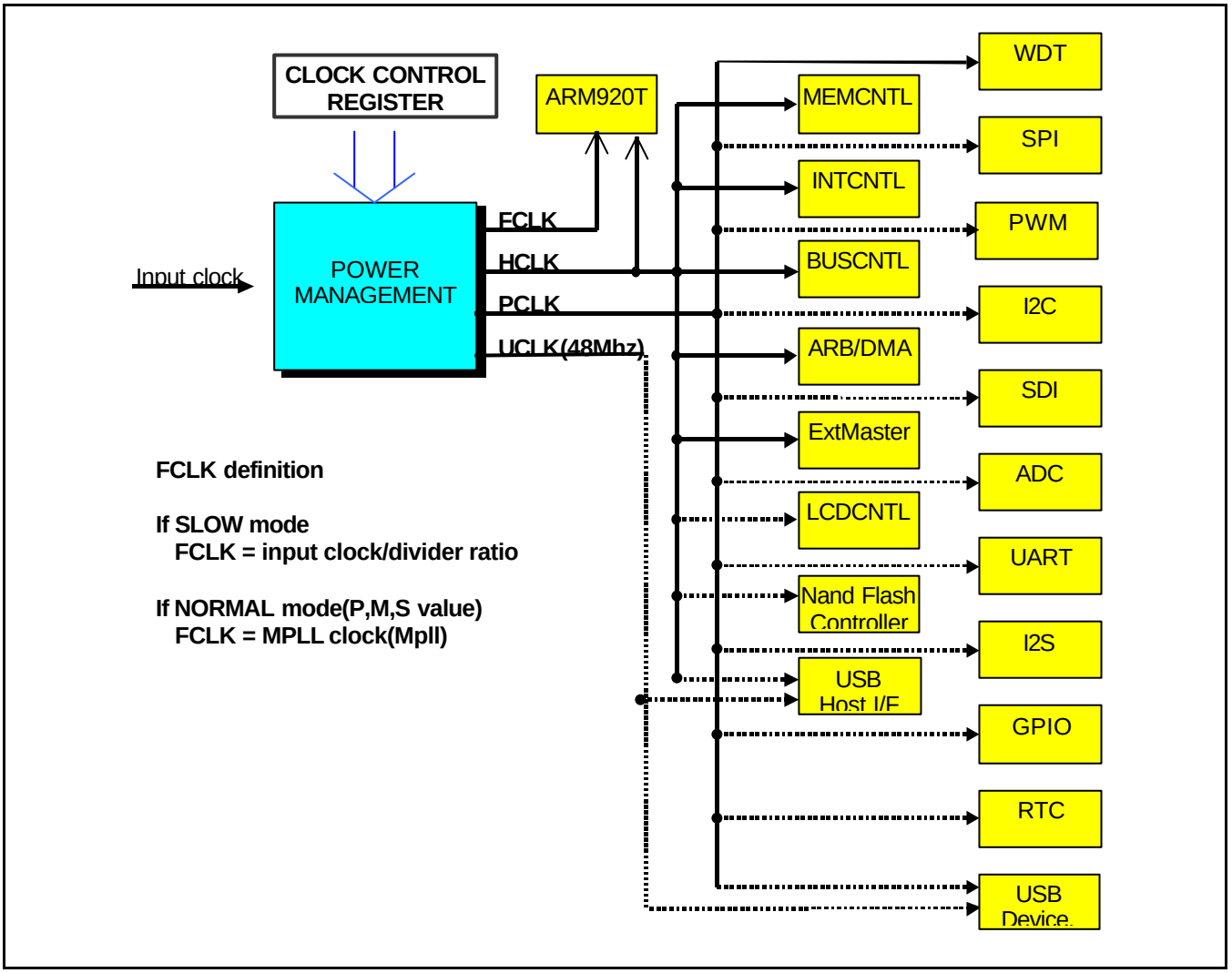


Figure 6-7. The Clock Distribution Block Diagram

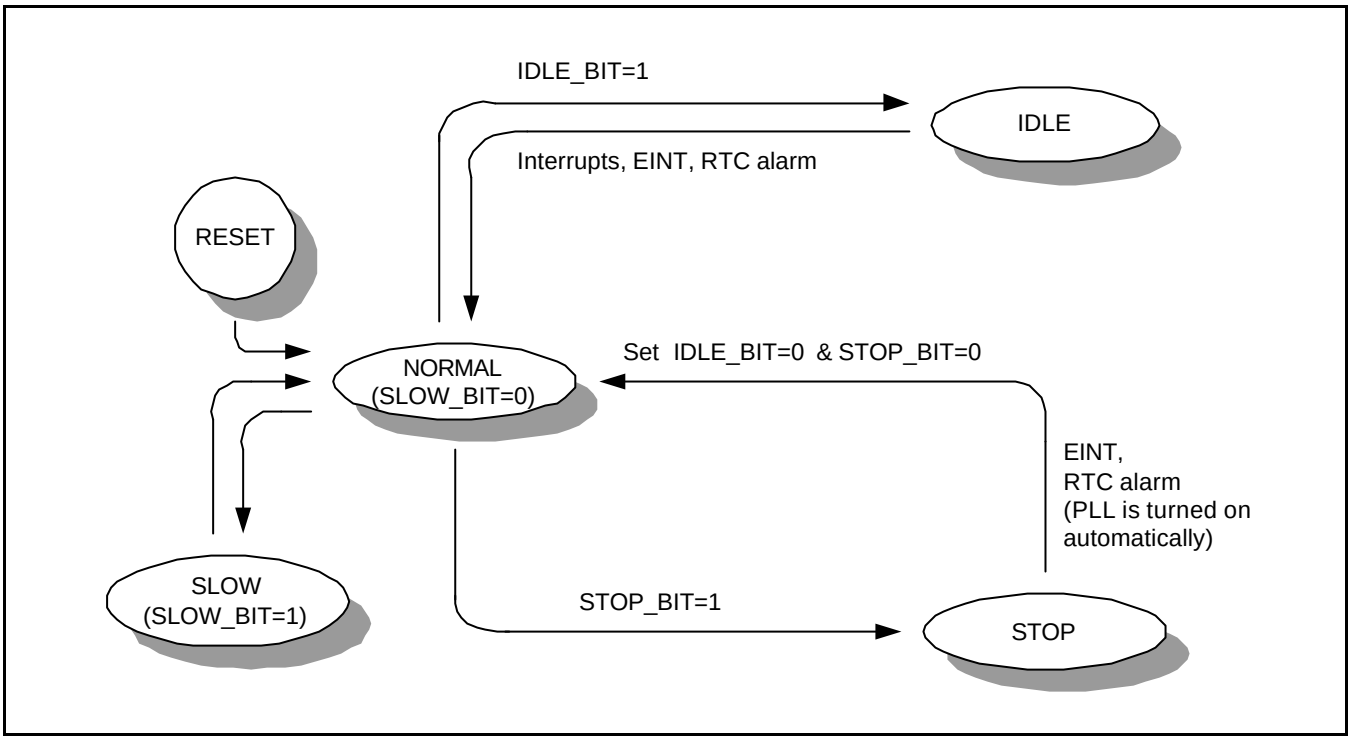


Figure 6-8. Power Management State Machine

Table 6-2. Functional Block Clock State In Each Power Mode

Mode	ARM920T	AHB Modules(1), WDT	LCD	APB Modules(2), USB host	UCLK
NORMAL	O	O	SEL	SEL	SEL
IDLE	X	O	SEL	SEL	SEL
STOP	X	X	X	X(3)	X
SLOW	O	O	SEL	SEL	SEL

NOTE. 1. USB host and RTC are excluded.
2. WDT is excluded.
3. RTC interface is turned off in STOP mode but RTC Timer is always turned on.
4. SEL: selectable, O: turned on, X: turned off

NORMAL Mode

In normal mode, all peripherals and the basic blocks(power management block, CPU core, bus controller, memory controller, interrupt controller, DMA, and external master) may operate fully. But, the clock to each peripheral, except the basic blocks, can be stopped selectively by S/W to reduce power consumption.

IDLE Mode

In IDLE mode, the clock to CPU core is stopped except bus controller, memory controller, interrupt controller, and power management block. To exit IDLE mode, EINT[7:0], or RTC alarm interrupt, or the other interrupts should be activated. (If users are willing to use EINT, GPIO block has to be turned on before the activation).

STOP Mode

In STOP mode, all clocks are stopped for minimum power consumption. Therefore, the PLL and oscillator circuit are also stopped. Just after exiting the STOP mode, only NORMAL mode is available. In Figure 6-8, the user must return from STOP mode to NORMAL mode. To exit from STOP mode, EINT[7:0] or RTC alarm has to be activated and CLKCON register is set properly.

DRAM has to be in self-refresh mode during STOP mode to retain valid memory data.

LCD must be stopped before STOP mode, because DRAM can't be accessed when it' s in self-refresh mode.

All interrupts should be masked, because DRAM can't be accessed when it' s in self-refresh mode.
(Even though all interrupts are masked, EINT can wake-up S3C2410X01 with the attribute of EXTINT0 register.)

If MMU is turned on, TLB fill operation should not be allowed after entering STOP mode because SDRAM is entered the self-refresh mode. So, The TLB should be filled in advance. Please refer to our reference code.

The S3C2410X01 can exit from STOP mode by EINT[7:0](external interrupts) or RTC alarm. During the wake-up sequences, the crystal oscillator and PLL may begin to operate. The lock time is also needed to stabilize FCLK. The lock time is inserted automatically and guaranteed by power management logic. During this lock time the clock is not supplied. Just after wake-up sequences wake-up interrupt(RTC alarm or external interrupt) is requested.

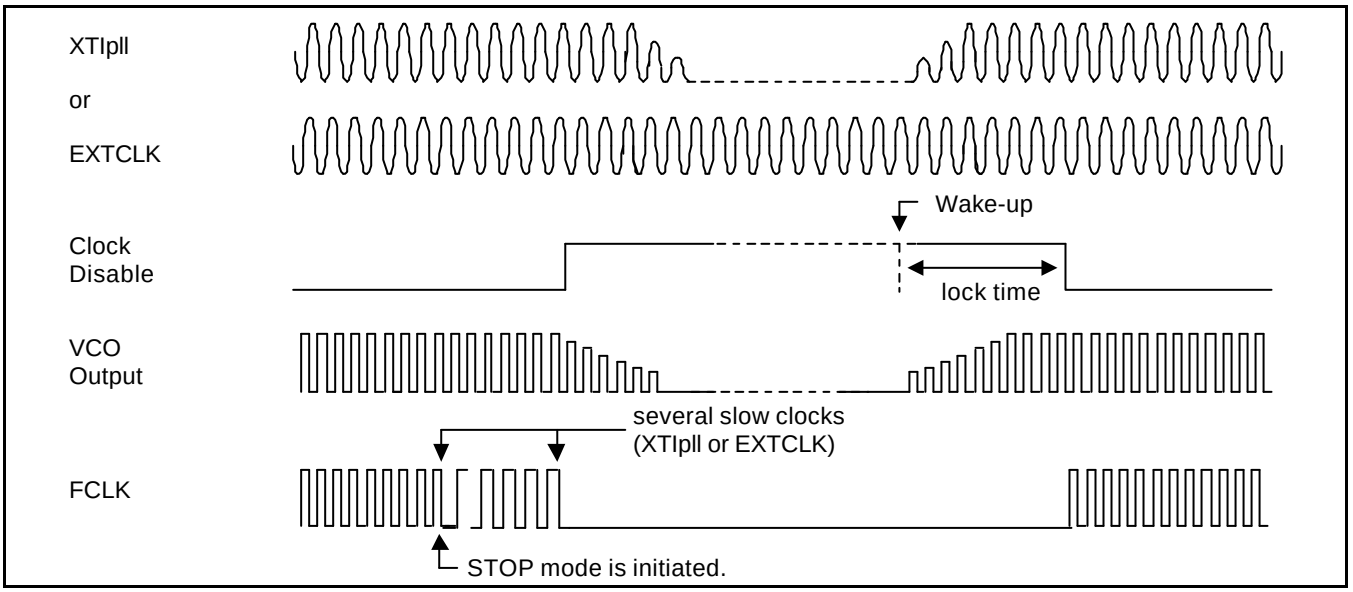


Figure 6-9. Entering STOP Mode and Exiting STOP mode (Wake-up)

SLOW Mode (Non-PLL Mode)

Power consumption can be reduced in the SLOW mode by applying a slow clock and excluding the power consumption from the PLL, itself. The FCLK is the frequency of divide_by_n of the input clock(XTIpll or EXTCLK) without PLL. The divider ratio is determined by SLOW_VAL in the CLKSLOW control register and CLKDIVN control register.

Table 6-3. CLKSLOW and CLKDIVN Register Settings for SLOW Clock

SLOW_VAL	FCLK	HCLK		PCLK		UCLK
		1/1 Option (HDIVN=0)	1/2 Option (HDIVN=1)	1/1 Option (PDIVN=0)	1/2 Option (PDIVN=1)	
0 0 0	EXTCLK or XTIpll / 1	EXTCLK or XTIpll / 1	EXTCLK or XTIpll / 2	HCLK	HCLK / 2	48Mhz
0 0 1	EXTCLK or XTIpll / 2	EXTCLK or XTIpll / 2	EXTCLK or XTIpll / 4	HCLK	HCLK / 2	48Mhz
0 1 0	EXTCLK or XTIpll / 4	EXTCLK or XTIpll / 4	EXTCLK or XTIpll / 8	HCLK	HCLK / 2	48Mhz
0 1 1	EXTCLK or XTIpll / 6	EXTCLK or XTIpll / 6	EXTCLK or XTIpll / 12	HCLK	HCLK / 2	48Mhz
1 0 0	EXTCLK or XTIpll / 8	EXTCLK or XTIpll / 8	EXTCLK or XTIpll / 16	HCLK	HCLK / 2	48Mhz
1 0 1	EXTCLK or XTIpll / 10	EXTCLK or XTIpll / 10	EXTCLK or XTIpll / 20	HCLK	HCLK / 2	48Mhz
1 1 0	EXTCLK or XTIpll / 12	EXTCLK or XTIpll / 12	EXTCLK or XTIpll / 24	HCLK	HCLK / 2	48Mhz
1 1 1	EXTCLK or XTIpll / 14	EXTCLK or XTIpll / 14	EXTCLK or XTIpll / 28	HCLK	HCLK / 2	48Mhz

In SLOW mode, the PLL will be turned off to reduce the PLL power consumption. When PLL is turned off in SLOW mode and users change power mode from SLOW mode to NORMAL mode, the PLL needs clock stabilization time(PLL lock time). This PLL stabilization time is automatically inserted by the internal logic with lock time count register. The PLL stability time will take 150us after PLL is turn on. During PLL lock time, the FCLK is SLOW clock.

Users can change the frequency by enabling SLOW mode bit in CLKSLOW register in PLL on state. The SLOW clock is generated during SLOW mode. The timing diagram is in Figure 6-11.

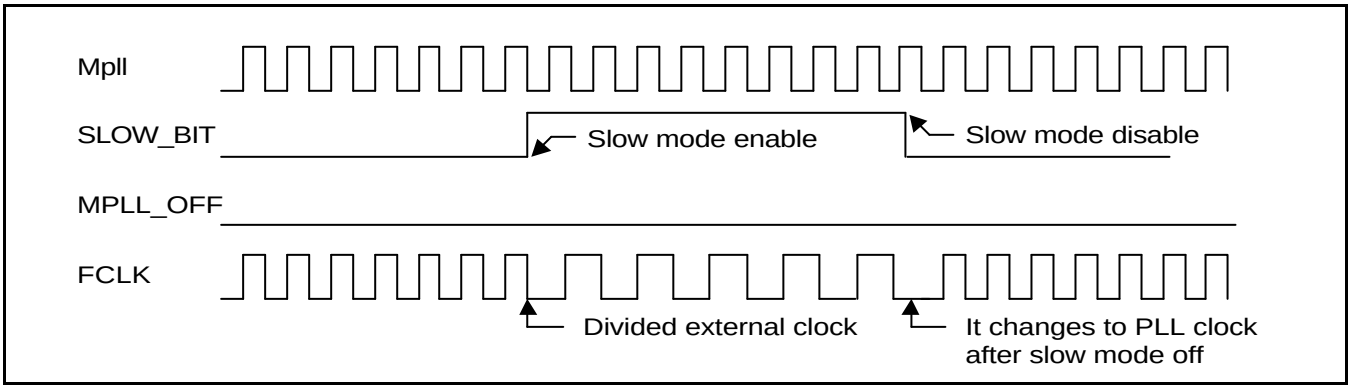


Figure 6-11. The case that Exit_from_Slow_mode command is issued in PLL on state

If users exit from SLOW mode to Normal mode by disabling the SLOW_BIT in the CLKSLOW register after PLL lock time, the frequency is changed just after SLOW mode is disabled. The timing diagram is in Figure 6-12.

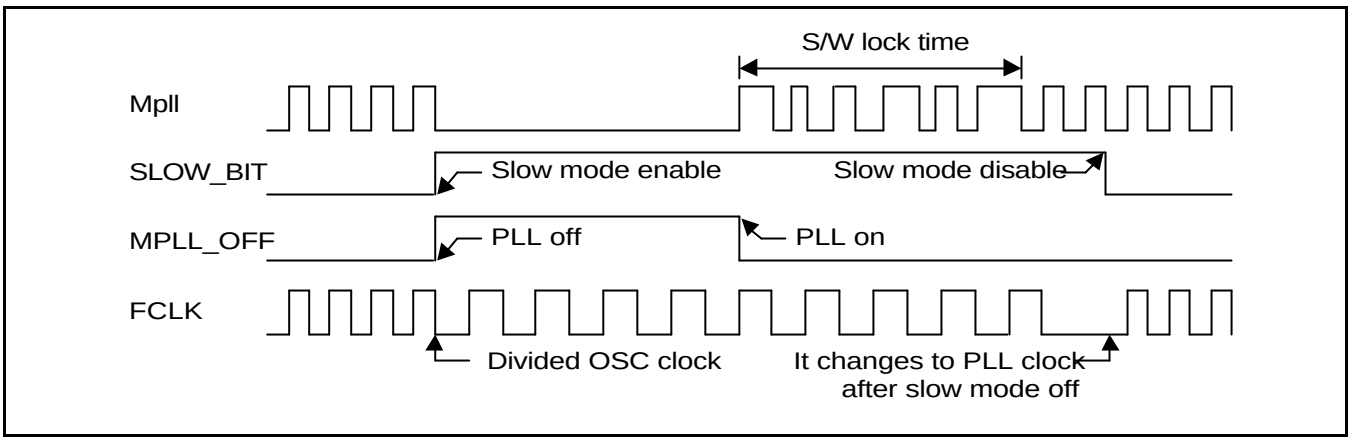


Figure 6-12. The case that Exit_from_Slow_mode command is issued after lock time is end

If users exit from SLOW mode to Normal mode by disabling SLOW_BIT and MPLL_OFF bit simultaneously in CLKSLOW register, the frequency is changed just after the PLL lock time. The timing diagram is as follow.

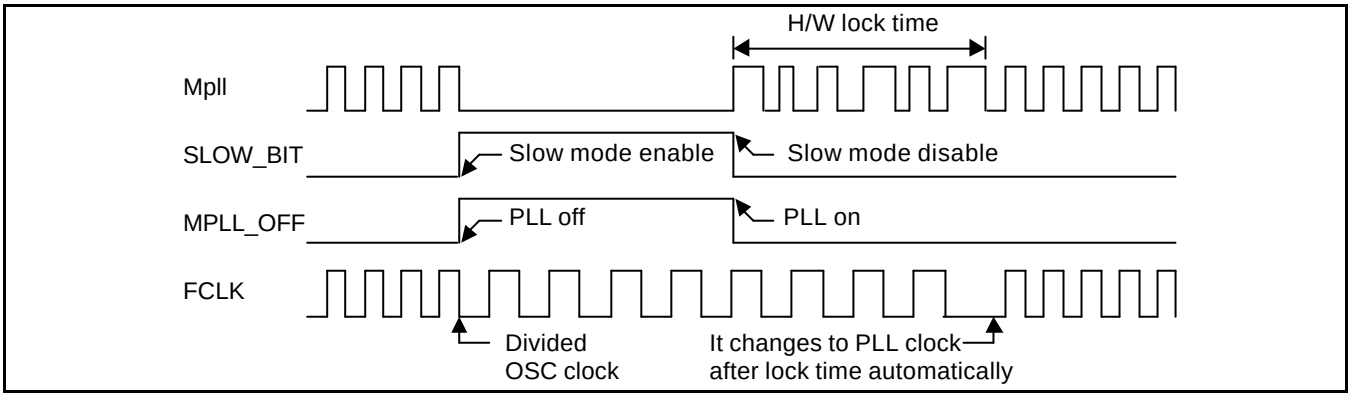


Figure 6-13. The case that the Exit_from_Slow_mode command and the instant PLL_on command is issued simultaneously.

Wake-Up from STOP mode

When the S3C2410X01 is woken up from power down mode(STOP mode) by an EINT[7:0] or a RTC alarm interrupt, the PLL is turned on automatically. But S3C2410X01 is not in NORMAL mode yet. Because the configuration of the CLKCON is ignored. So, the user has to set CLKCON register.

After the wake-up from STOP mode, the processor is not in NORMAL mode as explained above. The new value, which reflects the new state, has to be re-written into the CLKCON register. Eventually, the processor state will be changed from STOP mode to Normal mode.

Table 6-4. The Status of PLL and FCLK After Wake-Up

Mode before wake-up	PLL on/off after wake up	FCLK after wake up and before the lock time	FCLK after the lock time by internal logic
STOP	off → on	no clock	normal mode clock
IDLE	unchanged	unchanged	unchanged

Signaling EINT[7:0] For Wake-Up

The S3C2410X01 can be woken up from STOP mode only if the following conditions are met.

a) Level signal(H or L) or edge signal(rising or falling or both) is asserted on EINTn input pin.
b) EINTn pin has to be configured as EINT in the GPIO control register.

It is important to configure the EINTn in the GPIO control register as an external interrupt pins. For wake-up, we need H/L level or rising/falling edge or both edge signals on EINTn pin.

Just after wake-up the corresponding EINTn pin will not be used for wake-up. This means that these pins can be used as external interrupt request pins again.

Entering IDLE Mode

If CLKCON[2] is set to 1 to enter the IDLE mode, S3C2410X01 will enter into IDLE mode after some delay(until when the power control logic receives ACK signal from the CPU wrapper).

PLL On/Off

The PLL can only be turned off for power saving in slow mode. If PLL is turned off in any other mode, MCU operation is not guaranteed.

When the processor is in SLOW mode and tries to change its state into other state requiring that PLL be turned on, then SLOW_BIT should be clear to move to another state after PLL stabilization.

PnUPs register and STOP mode

In STOP mode, the data bus(D[31:0] or D[15:0]) is Hi-z state.

But, because of the characteristics of I/O pad, the data bus pull-up resistors have to be turned on to reduce the power consumption in STOP mode. D[31:0] pin pull-up resistors can be controlled by the GPIO control register(MISCCR).

OUTPUT PORT State and STOP mode

If output is L, the current will be consumed through the internal parasitic resistance; if the output is H, the current will not be consumed. If a port is configured as an output port, the current consumption can be reduced if the output state is H.

The output ports are recommended to be in H state to reduce STOP mode current consumption.

ADC Power Down

The ADC has an additional power-down bit(STDBM) in ADCCON. If S3C2410X01 enters the STOP mode, the ADC should enter it's own power-down mode.

CLOCK GENERATOR & POWER MANAGEMENT SPECIAL REGISTER

LOCK TIME COUNT REGISTER (LOCKTIME)

Register	Address	R/W	Description	Reset Value
LOCKTIME	0x4c00_0000	R/W	PLL lock time count register	0x00ffffff

LOCKTIME	Bit	Description	Initial State
U_LTIME	[23:12]	UPLL lock time count value for UCLK. (U_LTIME>150uS)	0xfff
M_LTIME	[11:0]	MPLL lock time count value for FCLK,HCLK,PCLK (M_LTIME>150uS)	0xfff

PLL CONTROL REGISTER (MPLLCON,UPLLCON)

*Mpll = (m * Fin) / (p * 2^s)*
m = (MDIV + 8), p = (PDIV + 2), s = SDIV

PLL VALUE SELECTION GUIDE

1. Fout = m * Fin / p*s, where : m=M+8, p=P+2, s=2^s
2. Fin/(25*p) < 16.7e6/m < Fin/(10*p)
3. 0.7 < 6.48/sqrt(m) < 1.8
4. (Fin/p)*m < 330e6

Register	Address	R/W	Description	Reset Value
MPLLCON	0x4c00_0004	R/W	MPLL configuration register	0x0005c080
UPLLCON	0x4c00_0008	R/W	UPLL configuration register	0x00028080

PLLCON	Bit	Description	Initial State
MDIV	[19:12]	Main divider control	0x5c / 0x28
PDIV	[9:4]	Pre-divider control	0x08 / 0x08
SDIV	[1:0]	Post divider control	0x0 / 0x0

CAUTION : WHEN YOU SET MPLL&UPLL VALUES SIMULTANEOUSLY, MPLL VALUE MPLL VALUE FIRST AND THEN UPLL VALUE SHOULD BE SET.

PLL VALUE SELECTION GUIDE

It' s difficult to find the proper PLL value. So, We recommended referring to the following PLL value recommendation table.

Input Frequency	Output Frequency	MDIV	PDIV	SDIV
12.00Mhz	11.289Mhz	N/A	N/A	N/A
12.00Mhz	16.934Mhz	N/A	N/A	N/A
12.00Mhz	22.50Mhz	N/A	N/A	N/A
12.00Mhz	33.75Mhz	82	2	3
12.00Mhz	45.00Mhz	82	1	3
12.00Mhz	50.70Mhz	161	3	3
12.00Mhz	56.25Mhz	142	2	3
12.00Mhz	67.50Mhz	82	2	2
12.00Mhz	79.00Mhz	71	1	2
12.00Mhz	84.75Mhz	105	2	2
12.00Mhz	90.00Mhz	112	2	2
12.00Mhz	101.25Mhz	127	2	2
12.00Mhz	113.00Mhz	105	1	2
12.00Mhz	118.50Mhz	150	2	2
12.00Mhz	124.00Mhz	116	1	2
12.00Mhz	135.00Mhz	82	2	1
12.00Mhz	147.00Mhz	90	2	1
12.00Mhz	152.00Mhz	68	1	1
12.00Mhz	158.00Mhz	71	1	1
12.00Mhz	170.00Mhz	77	1	1
12.00Mhz	180.00Mhz	82	1	1
12.00Mhz	186.00Mhz	85	1	1
12.00Mhz	192.00Mhz	88	1	1
12.00Mhz	202.80Mhz	161	3	1
12.00Mhz	214.50Mhz	135	2	1
12.00Mhz	220.00Mhz	102	1	1
12.00Mhz	226.00Mhz	105	1	1
12.00Mhz	237.00Mhz	150	2	1

CLOCK CONTROL REGISTER (CLKCON)

Register	Address	R/W	Description	Reset Value
CLKCON	0x4c00_000C	R/W	Clock generator control Register	0xffff0

CLKCON	Bit	Description	Initial State
SPI	[18]	Controls PCLK into SPI block 0 = Disable, 1 = Enable	1
IIS	[17]	Controls PCLK into IIS block 0 = Disable, 1 = Enable	1
IIC	[16]	Controls PCLK into IIC block 0 = Disable, 1 = Enable	1
ADC(&Touch Screen)	[15]	Controls PCLK into ADC block 0 = Disable, 1 = Enable	1
RTC	[14]	Controls PCLK into RTC control block. Even if this bit is cleared to 0, RTC timer is alive. 0 = Disable, 1 = Enable	1
GPIO	[13]	Controls PCLK into GPIO block 0 = Disable, 1 = Enable	1
UART2	[12]	Controls PCLK into UART2 block 0 = Disable, 1 = Enable	1
UART1	[11]	Controls PCLK into UART1 block 0 = Disable, 1 = Enable	1
UART0	[10]	Controls PCLK into UART0 block 0 = Disable, 1 = Enable	1
SDI	[9]	Controls PCLK into SDI interface block 0 = Disable, 1 = Enable	1
PWMTIMER	[8]	Controls PCLK into PWMTIMER block 0 = Disable, 1 = Enable	1
USB device	[7]	Controls PCLK into USB device block 0 = Disable, 1 = Enable	1
USB host	[6]	Controls HCLK into USB host block 0 = Disable, 1 = Enable	1
LCDC	[5]	Controls HCLK into LCDC block 0 = Disable, 1 = Enable	1
Nand Flash Controller	[4]	Controls HCLK into Nand Flash Controller block 0 = Disable, 1 = Enable	1
Reserved	[3]	Reserved	0
IDLE BIT	[2]	Enters IDLE mode. This bit isn't be cleared automatically. 0 = Disable, 1 = Transition to IDLE mode	0
Reserved	[1]	Reserved	0
STOP BIT	[0]	Enters STOP mode. This bit isn't be cleared automatically.	0

		0 = Disable 1 = Transition to STOP mode	

CLOCK SLOW CONTROL REGISTER (CLKSLOW)

Register	Address	R/W	Description	Reset Value
CLKSLOW	0x4c00_0010	R/W	Slow clock control register	0x00000004

CLKSLOW	Bit	Description	Initial State
UCLK_ON	[7]	0: UCLK ON (UPLL is also turned on and the UPLL lock time is inserted automatically.) 1: UCLK OFF(UPLL is also turned off)	0
Reserved	[6]	Reserved	-
MPLL_OFF	[5]	0 : PLL is turned on. After PLL stabilization time (minimum 150us), SLOW_BIT can be cleared to 0. 1 : PLL is turned off. PLL is turned off only when SLOW_BIT is 1.	0
SLOW_BIT	[4]	0 : FCLK = Mpll (MPLL output) 1: SLOW mode FCLK = input clock / (2 x SLOW_VAL) (SLOW_VAL > 0) FCLK = input clock (SLOW_VAL = 0) input clock = XTIpll or EXTCLK	0
SLOW_VAL	[2:0]	The divider value for the slow clock when SLOW_BIT is on.	0x4

CLOCK DIVIDER CONTROL REGISTER (CLKDIVN)

Register	Address	R/W	Description	Reset Value
CLKDIVN	0x4c00_0014	R/W	Clock divider control register	0x00000000

CLKDIVN	Bit	Description	Initial State
HDIVN	[1]	0: HCLK has the clock same as the FCLK 1: HCLK has the clock same as the FCLK/2	0
PDIVN	[0]	0: PCLK has the clock same as the HCLK 1: PCLK has the clock same as the HCLK/2	0

7 BUS PRIORITIES (Preliminary)

OVERVIEW

The bus arbitration logic determines the priorities of bus masters. It supports a combination of rotation priority mode and fixed priority mode.

BUS PRIORITY MAP

In S3C2410X01, there are eleven bus masters, i.e., DRAM refresh controller, LCD_DMA, DMA0, DMA1, DMA2, DMA3, USB_HOST_DMA, EXT_BUS_MASTER, TIC (Test interface controller), and ARM920T. The priorities among these bus masters after a reset are as follows :

1. DRAM refresh controller
2. LCD_DMA
3. DMA0
4. DMA1
5. DMA2
6. DMA3
7. USB_HOST_DMA (USB host DMA)
8. EXT_BUS_MASTER (External bus master)
9. TIC
10. ARM920T
11. Reserved

Among those bus masters, four DMAs operate under the rotation priority, while others run under the fixed priority.

8 DMA (Preliminary)

OVERVIEW

S3C2410X01 supports four-channel DMA controller that is located between the system bus and the peripheral bus. Each channel of DMA controller can perform data movements between devices in the system bus and/or peripheral bus with no restrictions. In other words, each channel can handle the following four cases: 1) both source and destination are in the system bus, 2) source is in the system bus while destination is in the peripheral bus, 3) source is in the peripheral bus while destination is in the system bus, 4) both source and destination are in the peripheral bus.

The main advantage of DMA is that it can transfer the data without CPU intervention. The operation of DMA can be initiated by S/W, the request from internal peripherals or the external request pins.

DMA REQUEST SOURCES

Each channel of DMA controller can select one of DMA request source among four DMA sources if H/W DMA request mode is selected by DCON register. (Note that if S/W request mode is selected, this DMA request sources have no meaning at all.) The four DMA sources for each channel are as follows.

	Source0	Source1	Source2	Source3	Source4
Ch-0	nXDREQ0	UART0	MMC	Timer	USB device EP1
Ch-1	nXDREQ1	UART1	I2SSDI	SPI	USB device EP2
Ch-2	I2SSDO	I2SSDI	MMC	Timer	USB device EP3
Ch-3	UART2	MMC	SPI	Timer	USB device EP4

Table 8-1. DMA request sources for each channel

Here, nXDREQ0 and nXDREQ1 represent two external sources(External Devices), and I2SSDO and I2SSDI represent IIS transmitting and receiving, respectively.

DMA OPERATION

The details of DMA operation can be explained using three-state FSM(finite state machine) as follows:

State-1. As an initial state, it waits for the DMA request. If it comes, go to state-2. At this state, DMA ACK and INT REQ are 0.

State-2. In this state, DMA ACK becomes 1 and the counter(CURR_TC) is loaded from DCON[19:0] register. Note that DMA ACK becomes 1 and remains 1 until it is cleared later.

State-3. In this state, sub-FSM handling the atomic operation of DMA is initiated. The sub-FSM reads the data from the source address and then writes it to destination address. In this operation, data size and transfer size (single or burst) are considered. This operation is repeated until the counter(CURR_TC) becomes 0 in the whole service mode, while performed only once in a single service mode. The main FSM (this FSM) counts down the CURR_TC when the sub-FSM finishes each of atomic operation. In addition, this main FSM asserts the INT REQ signal when CURR_TC becomes 0 and the interrupt setting of DCON[29] register is set to 1. In addition, it clears DMA ACK if one of the following conditions are met.

1) CURR_TC becomes 0 in the whole service mode
2) atomic operation finishes in the single service mode.

Note that in the single service mode, these three states of main FSM are performed and then stops, and waits for another DMA REQ. And if DMA REQ comes in all three states are repeated. Therefore, DMA ACK is asserted and then de-asserted for each atomic transfer. In contrast, in the whole service mode, main FSM waits at state-3 until CURR_TC becomes 0. Therefore, DMA ACK is asserted during all the transfers and then de-asserted when TC reaches 0.

However, INT REQ is asserted only if CURR_TC becomes 0 regardless of the service mode (single service mode or whole service mode).

EXTERNAL DMA DREQ/DACK PROTOCOL

There are three types of external DMA request/acknowledge protocols (Single service Demand, Single service Handshake and Whole service Handshake mode). Each type defines how the signals like DMA request and acknowledge are related to these protocols.

Basic DMA Timing

The DMA service means paired Reads and Writes cycles during DMA operation, which is one DMA operation. The Fig. 8-1 shows the basic Timing in the DMA operation of the S3C2410X01.

- The setup time and the delay time of XnXDREQ and XnXDACK are same in all the modes.
- If the completion of XnXDREQ meets its setup time, it is synchronized twice and then XnXDACK is asserted.
- After assertion of XnXDACK, DMA requests the bus and if it gets the bus it performs its operations. XnXDACK is deasserted when DMA operation finishes.

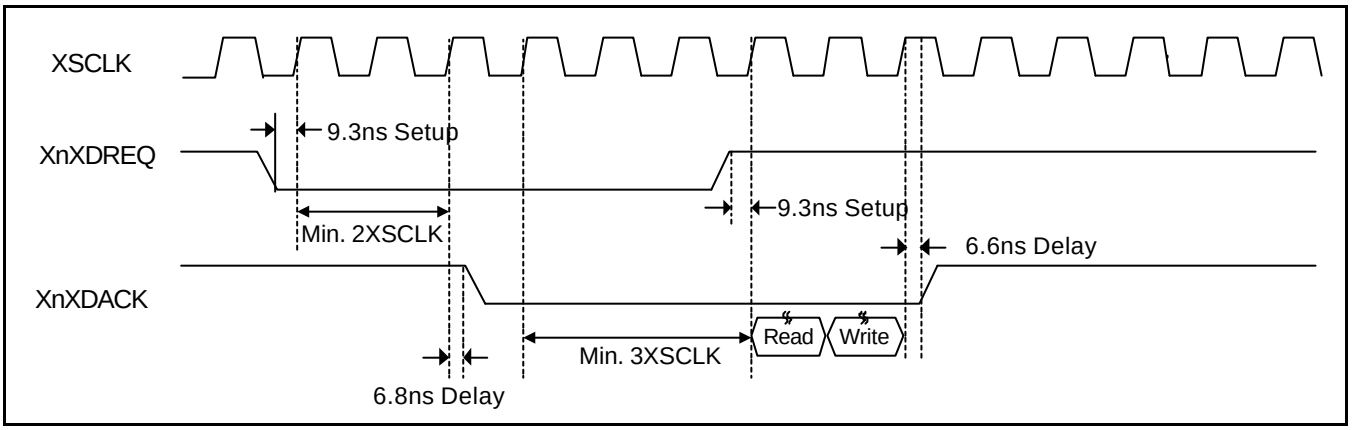


Figure 8-1. Basic DMA Timing Diagram

Demand/Handshake Mode Comparison – Related to the Protocol between XnXDREQ and XnXDACK

These are two different modes related to the protocol between XnXDREQ and XnXDACK. Fig. 8-2 shows the differences between these two modes i.e., Demand and Handshake modes.

At the end of one transfer(Single/Burst transfer), DMA checks the state of double-synched XnXDREQ.

Demand mode

- If XnXDREQ remains asserted, the next transfer starts immediately. Otherwise it waits for XnXDREQ to be asserted.

Handshake mode

- If XnXDREQ is deasserted, DMA deasserts XnXDACK in 2cycles. Otherwise it waits until XnXDREQ is deasserted.

  Caution : XnXDREQ has to be asserted(low) only after the deassertion(high) of XnXDACK.

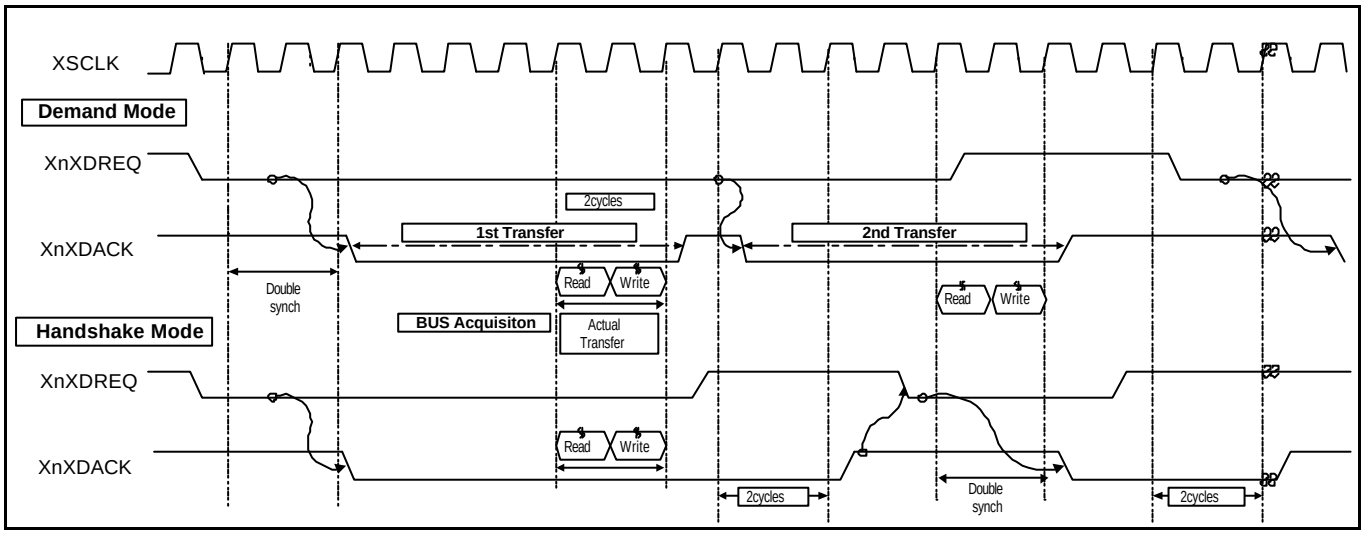


Figure 8-2. Demand/Handshake Mode Comparison

Transfer Size

- There are two different transfer sizes; single and Burst 4.
- DMA holds the bus firmly during the transfer of these chunk of data, thus other bus masters can not get the bus.

Burst 4 Transfer Size

4 sequential Reads and 4 sequential Writes are performed in the Burst 4 Transfer.

* NOTE: Single Transfer size : One read and one write are performed.

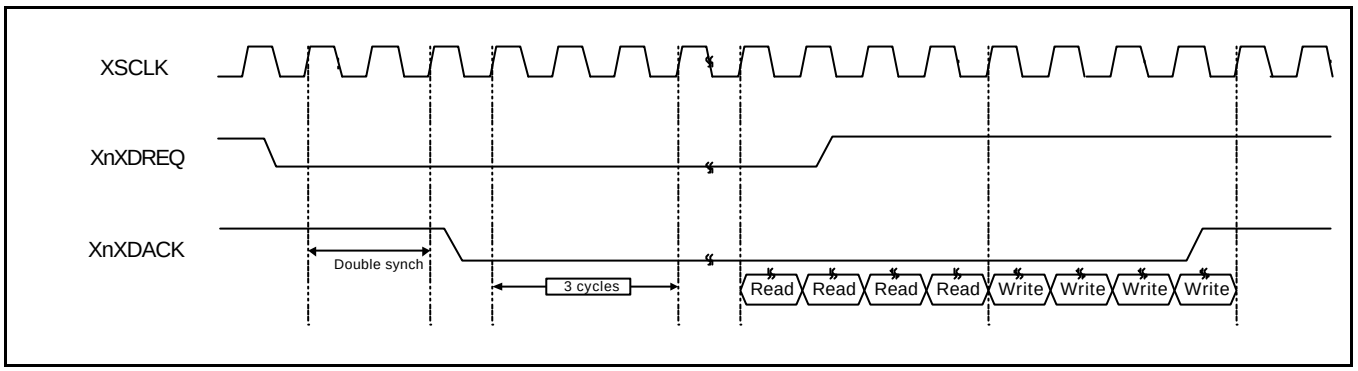


Figure 8-3. Burst 4 Transfer size

Examples of possible cases

Single service, Demand Mode, Single Transfer Size

The assertion of XnXDREQ is need for every unit transfer(Single service mode), the operation continues while the XnXDREQ is asserted(Demand mode), and one pair of Read and Write(Single transfer size) is performed.

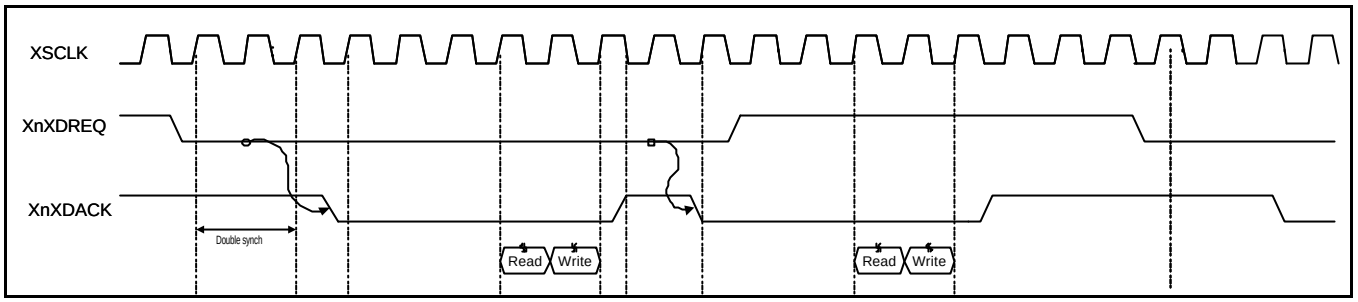


Figure 8-4. Single service, Demand Mode, Single Transfer Size

Single service/Handshake Mode, Single Transfer Size

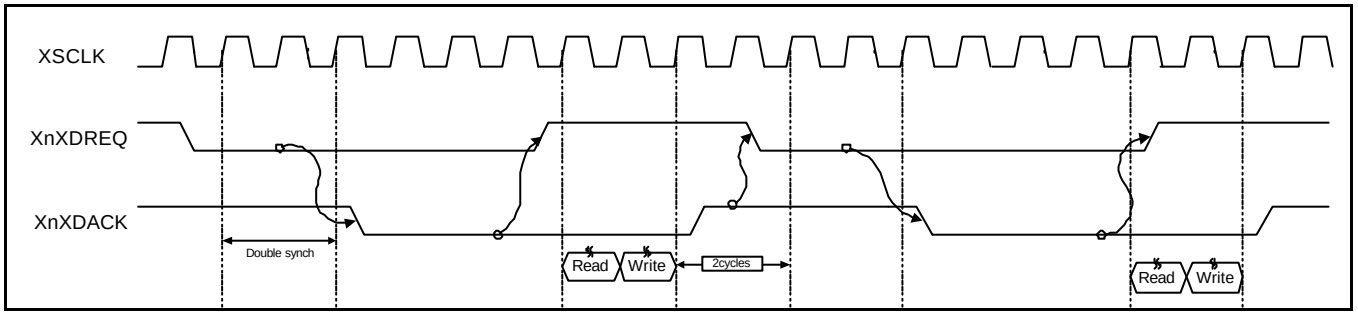


Figure 8-5. Single service, Handshake Mode, Single Transfer Size

Whole service/Handshake Mode, Single Transfer Size

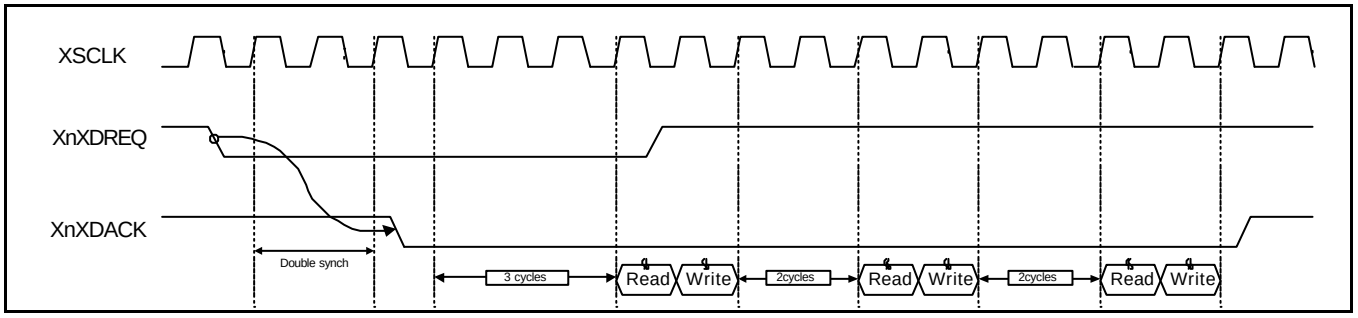


Figure 8-6. Whole service, Handshake Mode, Single Transfer Size

DMA SPECIAL REGISTERS

There are seven control registers for each DMA channel. (Since there are four channels, the total number of control registers is 32.) Four of them are to control the DMA transfer, and other three are to see the status of DMA controller. The details of those registers are as follows.

DMA INITIAL SOURCE REGISTER (DISRC)

Register	Address	R/W	Description	Reset Value
DISRC0	0x4b000000	R/W	DMA 0 Initial Source Register	0x00000000
DISRC1	0x4b000040	R/W	DMA 1 Initial Source Register	0x00000000
DISRC2	0x4b000080	R/W	DMA 2 Initial Source Register	0x00000000
DISRC3	0x4b0000c0	R/W	DMA 3 Initial Source Register	0x00000000

DISRCn	Bit	Description	Initial State
S_ADDR	[30:0]	These bits are the base address (start address) of source data to transfer. This value will be loaded into CURR_SRC only if the CURR_SRC is 0 and the DMA ACK is 1.	0x00000000

DMA INITIAL SOURCE CONTROL REGISTER (DISRCC)

Register	Address	R/W	Description	Reset Value
DISRCC0	0x4b000004	R/W	DMA 0 Initial Source Control Register	0x00000000
DISRCC1	0x4b000044	R/W	DMA 1 Initial Source Control Register	0x00000000
DISRCC2	0x4b000084	R/W	DMA 2 Initial Source Control Register	0x00000000
DISRCC3	0x4b0000c4	R/W	DMA 3 Initial Source Control Register	0x00000000

DISRCn	Bit	Description	Initial State
LOC	[1]	Bit 1 is used to select the location of source. 0: the source is in the system bus (AHB), 1: the source is in the peripheral bus (APB)	0
INC	[0]	Bit 0 is used to select the address increment. 0 = Increment 1= Fixed If it is 0, the address is increased by its data size after each transfer in burst and single transfer mode. If it is 1, the address is not changed after the transfer (In the burst mode, address is increased during the burst transfer, but the address is recovered to its first value after the transfer).	0

DMA INITIAL DESTINATION REGISTER (DIDST)

Register	Address	R/W	Description	Reset Value
DIDST0	0x4b000008	R/W	DMA 0 Initial Destination Register	0x00000000
DIDST1	0x4b000048	R/W	DMA 1 Initial Destination Register	0x00000000
DIDST2	0x4b000088	R/W	DMA 2 Initial Destination Register	0x00000000
DIDST3	0x4b0000c8	R/W	DMA 3 Initial Destination Register	0x00000000

DIDSTn	Bit	Description	Initial State
D_ADDR	[30:0]	These bits are the base address (start address) of destination for the transfer. This value will be loaded into CURR_SRC only if the CURR_DST is 0 and the DMA ACK is 1.	0x00000000

DMA INITIAL DESTINATION CONTROL REGISTER (DIDSTC)

Register	Address	R/W	Description	Reset Value
DIDSTC0	0x4b00000c	R/W	DMA 0 Initial Destination Control Register	0x00000000
DIDSTC1	0x4b00004c	R/W	DMA 1 Initial Destination Control Register	0x00000000
DIDSTC2	0x4b00008c	R/W	DMA 2 Initial Destination Control Register	0x00000000
DIDSTC3	0x4b0000cc	R/W	DMA 3 Initial Destination Control Register	0x00000000

DIDSTn	Bit	Description	Initial State
LOC	[1]	Bit 1 is used to select the location of destination. 0: the destination is in the system bus (AHB). 1: the destination is in the peripheral bus (APB).	0
INC	[0]	Bit 0 is used to select the address increment. 0 = Increment 1= Fixed If it is 0, the address is increased by its data size after each transfer in burst and single transfer mode. If it is 1, the address is not changed after the transfer (In the burst mode, address is increased during the burst transfer, but the address is recovered to its first value after the transfer).	0

DMA CONTROL REGISTER (DCON)

Register	Address	R/W	Description	Reset Value
DCON0	0x4b000010	R/W	DMA 0 Control Register	0x00000000
DCON1	0x4b000050	R/W	DMA 1 Control Register	0x00000000
DCON2	0x4b000090	R/W	DMA 2 Control Register	0x00000000
DCON3	0x4b0000d0	R/W	DMA 3 Control Register	0x00000000

DCONn	Bit	Description	Initial State
DMD_HS	[31]	Select one between demand mode and handshake mode. 0 : demand mode is selected 1 : handshake mode is selected. In both modes, DMA controller starts its transfer and asserts DACK for a given asserted DREQ. The difference between two modes is whether it waits for the de-asserted DACK or not. In handshake mode, DMA controller waits for the de-asserted DREQ before starting a new transfer. If it sees the de-asserted DREQ, it de-asserts DACK and waits for another asserted DREQ. In contrast, in the demand mode, DMA controller does not wait until the DREQ is de-asserted. It just de-asserts DACK and then starts another transfer if DREQ is asserted. We recommend using handshake mode for external DMA request sources to prevent unintended starts of new transfers.	0
SYNC	[30]	Select DREQ/DACK synchronization. 0: DREQ and DACK are synchronized to PCLK (APB clock). 1: DREQ and DACK are synchronized to HCLK (AHB clock). Therefore, devices attached to AHB system bus, this bit has to be set to 1, while those attached to APB system, it should be set to 0. For the devices attached to external system, user should select this bit depending on whether the external system is synchronized with AHB system or APB system.	0
INT	[29]	Enable/Disable the interrupt setting for CURR_TC(terminal count) 0: CURR_TC interrupt is disabled. user has to look the transfer count in the status register. (i.e., polling) 1: interrupt request is generated when all the transfer is done (i.e., CURR_TC becomes 0).	0
TSZ	[28]	Select the transfer size of an atomic transfer (i.e., transfer performed at each time DMA owns the bus before releasing the bus). 0: a unit transfer is performed. 1: a burst transfer of length four is performed.	0

DCONn	Bit	Description	Initial State
SERVMODE	[27]	Select the service mode between single service mode and whole service mode. 0: single service mode is selected in which after each atomic transfer (single or burst of length four) DMA stops and waits for another DMA request. 1: whole service mode is selected in which one request gets atomic transfers to be repeated until the transfer count reaches to 0. In this mode, additional request is not required. Here, note that even in the whole service mode, DMA releases the bus after each atomic transfer and then tries to re-get the bus to prevent starving of other bus masters.	0
HWSRCSEL	[26:24]	Select DMA request source for each DMA. DCON0: 000:nXDREQ0 001:UART0 010:MMC 011:Timer 100:USB device EP1 DCON1: 000:nXDREQ1 001:UART1 010:I2SSDI 011:SPI 100:USB device EP2 DCON2: 000:I2SSDO 001:I2SSDI 010:MMC 011:Timer 100:USB device EP3 DCON3: 000:UART2 001:MMC 010:SPI 011:Timer 100:USB device EP4 This bits control the 4-1 MUX to select the DMA request source of each DMA. These bits have meanings if and only if H/W request mode is selected by DCONn[23].	00
SWHW_SEL	[23]	Select the DMA source between software (S/W request mode) and hardware (H/W request mode). 0: S/W request mode is selected and DMA is triggered by setting SW_TRIG bit of DMASKTRIG control register. 1: DMA source selected by bit[25:24] is used to trigger the DMA operation.	0
RELOAD	[22]	Set the reload on/off option. 0: auto reload is performed when a current value of transfer count becomes 0 (i.e., all the required transfers are performed). 1: DMA channel(DMA REQ) is turned off when a current value of transfer count becomes 0. The channel on/off bit(DMASKTRIGn[1]) is set to 0(DREQ off) to prevent unintended further start of new DMA operation	0
DSZ	[21:20]	Data size to be transferred. 00 = Byte 01 = Half word 10 = Word 11 = reserved	00
TC	[19:0]	Initial transfer count (or transfer beat). Note that the actual number of bytes that are transferred is computed by the following equation: DSZ x TSZ x TC, where DSZ, TSZ(1 or 4), and TC represent data size (DCONn[21:20]), transfer size (DCONn[27]), and initial transfer count, respectively. This value will be loaded into CURR_SRC only if the CURR_SRC is 0 and the DMA ACK is 1.	00000

DMA STATUS REGISTER (DSTAT)

Register	Address	R/W	Description	Reset Value
DSTAT0	0x4b000014	R	DMA 0 Count Register	000000h
DSTAT1	0x4b000054	R	DMA 1 Count Register	000000h
DSTAT2	0x4b000094	R	DMA 2 Count Register	000000h
DSTAT3	0x4b0000d4	R	DMA 3 Count Register	000000h

DSTATn	Bit	Description	Initial State
STAT	[21:20]	Status of this DMA controller. 00: It indicates that DMA controller is ready for another DMA request. 01: It indicates that DMA controller is busy for transfers.	00b
CURR_TC	[19:0]	Current value of transfer count. Note that transfer count is initially set to the value of DCONn[19:0] register and decreased by one at the end of every atomic transfer.	00000h

DMA CURRENT SOURCE REGISTER (DCSRC)

Register	Address	R/W	Description	Reset Value
DCSRC0	0x4b000018	R	DMA 0 Current Source Register	0x00000000
DCSRC1	0x4b000058	R	DMA 1 Current Source Register	0x00000000
DCSRC2	0x4b000098	R	DMA 2 Current Source Register	0x00000000
DCSRC3	0x4b0000d8	R	DMA 3 Current Source Register	0x00000000

DCSRCn	Bit	Description	Initial State
CURR_SRC	[30:0]	Current source address for DMAn.	0x00000000

CURRENT DESTINATION REGISTER (DCDST)

Register	Address	R/W	Description	Reset Value
DCDST0	0x4b00001c	R	DMA 0 Current Destination Register	0x00000000
DCDST1	0x4b00005c	R	DMA 1 Current Destination Register	0x00000000
DCDST2	0x4b00009c	R	DMA 2 Current Destination Register	0x00000000
DCDST3	0x4b0000dc	R	DMA 3 Current Destination Register	0x00000000

DCDSTn	Bit	Description	Initial State
CURR_DST	[30:0]	Current destination address for DMAn.	0x00000000

DMA MASK TRIGGER REGISTER (DMASKTRIG)

Register	Address	R/W	Description	Reset Value
DMASKTRIG0	0x4b000020	R/W	DMA 0 Mask Trigger Register	000
DMASKTRIG1	0x4b000060	R/W	DMA 1 Mask Trigger Register	000
DMASKTRIG2	0x4b0000a0	R/W	DMA 2 Mask Trigger Register	000
DMASKTRIG3	0x4b0000e0	R/W	DMA 3 Mask Trigger Register	000

DMASKTRIGn	Bit	Description	Initial State
STOP	[2]	Stop the DMA operation. 1: DMA stops as soon as the current atomic transfer ends. If there is no current running atomic transfer, DMA stops immediately. The CURR_TC, CURR_SRC, CURR_DST will be 0. NOTE: Due to possible current atomic transfer, "stop" may take several cycles. The finish of "stopping" operation (i.e., actual stop time) can be detected by waiting until the channel on/off bit(DMASKTRIGn[1]) is set to off. This stop is "actual stop".	0
ON_OFF	[1]	DMA channel on/off bit. 0: DMA channel is turned off. (DMA request to this channel is ignored.) 1: DMA channel is turned on and the DMA request is handled. This bit is automatically set to off if we set the DCONn[22] bit to "no auto reload" and/or STOP bit of DMASKTRIGn to "stop". Note that when DCON[22] bit is "no auto reload", this bit becomes 0 when CURR_TC reaches 0. If the STOP bit is 1, this bit becomes 0 as soon as the current atomic transfer finishes. NOTE. This bit should not be changed manually during DMA operations (i.e., this has to be changed only by using DCON[22] or STOP bit.)	0
SW_TRIG	[0]	Trigger the DMA channel in S/W request mode. 1: it requests a DMA operation to this controller. However, note that for this trigger to have effects S/W request mode has to be selected (DCONn[23]) and channel ON_OFF bit has to be set to 1 (channel on). When DMA operation starts, this bit is cleared automatically.	0

NOTE. You can freely change the values of DISRC register, DIDST registers, and TC field of DCON register. Those changes take effect only after the finish of current transfer (i.e., when CURR_TC becomes 0). On the other hand, any change made to other registers and/or fields takes immediate effect. Therefore, be careful in changing those registers and fields.

9 I/O PORTS(Preliminary)

OVERVIEW

S3C2410X01 has 117 multi-functional input/output port pins. There are eight ports :

— Port A (GPA) : 23-output port

— Port B (GPB) : 11-in/out port

— Port C (GPC) : 16-in/out port

— Port D (GPD) : 16-in/out port

— Port E (GPE) : 16-in/out port

— Port F (GPF) : 8-in/out port

— Port G (GPG) : 16-in/out port

— Port H (GPH) : 11-in/out port

Each port can be easily configured by software to meet various system configuration and design requirements. You have to define which function of each pin is used before starting the main program. If the multiplexed functions on a pin are not used, the pin can be configured as I/O ports.

The initial pin states, before pin configurations, are configured elegantly to avoid some problem.

Table 9-1. S3C2410 Port Configuration Overview

Port A	Selectable Pin Functions			
GPA22	Output only	nFCE	–	–
GPA21	Output only	nRSTOUT	–	–
GPA20	Output only	nFRE	–	–
GPA19	Output only	nFWE	–	–
GPA18	Output only	ALE	–	–
GPA17	Output only	CLE	–	–
GPA16	Output only	nGCS5	–	–
GPA15	Output only	nGCS4	–	–
GPA14	Output only	nGCS3	–	–
GPA13	Output only	nGCS2	–	–
GPA12	Output only	nGCS1	–	–
GPA11	Output only	ADDR26	–	–
GPA10	Output only	ADDR25	–	–
GPA9	Output only	ADDR24	–	–
GPA8	Output only	ADDR23	–	–
GPA7	Output only	ADDR22	–	–
GPA6	Output only	ADDR21	–	–
GPA5	Output only	ADDR20	–	–
GPA4	Output only	ADDR19	–	–
GPA3	Output only	ADDR18	–	–
GPA2	Output only	ADDR17	–	–
GPA1	Output only	ADDR16	–	–
GPA0	Output only	ADDR0	–	–

Table 9-1. S3C2410 Port Configuration Overview (Continued)

Port B	Selectable Pin Functions			
GPB10	Input/output	nXDREQ0	–	–
GPB9	Input/output	nXDACK0	–	–
GPB8	Input/output	nXDREQ1	–	–
GPB7	Input/output	nXDACK1	–	–
GPB6	Input/output	nXBREQ	–	–
GPB5	Input/output	nXBACK	–	–
GPB4	Input/output	TCLK0	–	–
GPB3	Input/output	TOUT3	–	–
GPB2	Input/output	TOUT2	–	–
GPB1	Input/output	TOUT1	–	–
GPB0	Input/output	TOUT0	–	–

Port C	Selectable Pin Functions			
GPC15	Input/output	VD7	–	–
GPC14	Input/output	VD6	–	–
GPC13	Input/output	VD5	–	–
GPC12	Input/output	VD4	–	–
GPC11	Input/output	VD3	–	–
GPC10	Input/output	VD2	–	–
GPC9	Input/output	VD1	–	–
GPC8	Input/output	VD0	–	–
GPC7	Input/output	LCDVF2	–	–
GPC6	Input/output	LCDVF1	–	–
GPC5	Input/output	LCDVF0	–	–
GPC4	Input/output	VM	–	–
GPC3	Input/output	VFRAME	–	–
GPC2	Input/output	VLINE	–	–
GPC1	Input/output	VCLK	–	–
GPC0	Input/output	LEND	–	–

Table 9-1. S3C2410 Port Configuration Overview (Continued)

Port D	Selectable Pin Functions			
GPD15	Input/output	VD23	nSS0	–
GPD14	Input/output	VD22	nSS1	–
GPD13	Input/output	VD21	–	–
GPD12	Input/output	VD20	–	–
GPD11	Input/output	VD19	–	–
GPD10	Input/output	VD18	–	–
GPD9	Input/output	VD17	–	–
GPD8	Input/output	VD16	–	–
GPD7	Input/output	VD15	–	–
GPD6	Input/output	VD14	–	–
GPD5	Input/output	VD13	–	–
GPD4	Input/output	VD12	–	–
GPD3	Input/output	VD11	–	–
GPD2	Input/output	VD10	–	–
GPD1	Input/output	VD9	–	–
GPD0	Input/output	VD8	–	–

Port E	Selectable Pin Functions			
GPE15	Input/output	IICSDA	–	–
GPE14	Input/output	IICSCL	–	–
GPE13	Input/output	SPICLK0	–	–
GPE12	Input/output	SPIMOSI0	–	–
GPE11	Input/output	SPIMISO0	–	–
GPE10	Input/output	SDDAT3	–	–
GPE9	Input/output	SDDAT2	–	–
GPE8	Input/output	SDDAT1	–	–
GPE7	Input/output	SDDAT0	–	–
GPE6	Input/output	SDCMD	–	–
GPE5	Input/output	SDCLK	–	–
GPE4	Input/output	I2SSDO	I2SSDI	–
GPE3	Input/output	I2SSDI	nSS0	–
GPE2	Input/output	CDCLK	–	–
GPE1	Input/output	I2SSCLK	–	–
GPE0	Input/output	I2SLRCK	–	–

Table 9-1. S3C2410 Port Configuration Overview (Continued)

Port F	Selectable Pin Functions			
GPF7	Input/output	EINT7	–	–
GPF6	Input/output	EINT6	–	–
GPF5	Input/output	EINT5	–	–
GPF4	Input/output	EINT4	–	–
GPF3	Input/output	EINT3	–	–
GPF2	Input/output	EINT2	–	–
GPF1	Input/output	EINT1	–	–
GPF0	Input/output	EINT0	–	–

Port G	Selectable Pin Functions			
GPG15	Input/output	EINT23	nYPON	–
GPG14	Input/output	EINT22	YMON	–
GPG13	Input/output	EINT21	nXPON	–
GPG12	Input/output	EINT20	XMON	–
GPG11	Input/output	EINT19	TCLK1	–
GPG10	Input/output	EINT18	–	–
GPG9	Input/output	EINT17	–	–
GPG8	Input/output	EINT16	–	–
GPG7	Input/output	EINT15	SPICLK1	–
GPG6	Input/output	EINT14	SPIMOSI1	–
GPG5	Input/output	EINT13	SPIMISO1	–
GPG4	Input/output	EINT12	LCD_PWREN	–
GPG3	Input/output	EINT11	nSS1	–
GPG2	Input/output	EINT10	nSS0	–
GPG1	Input/output	EINT9	–	–
GPG0	Input/output	EINT8	–	–

Table 9-1. S3C2410 Port Configuration Overview (Continued)

Port H	Selectable Pin Functions			
GPH10	Input/output	CLKOUT1	–	–
GPH9	Input/output	CLKOUT0	–	–
GPH8	Input/output	UCLK	–	–
GPH7	Input/output	RXD2	nCTS1	–
GPH6	Input/output	TXD2	nRTS1	–
GPH5	Input/output	RXD1	–	–
GPH4	Input/output	TXD1	–	–
GPH3	Input/output	RXD0	–	–
GPH2	Input/output	TXD0	–	–
GPH1	Input/output	nRTS0	–	–
GPH0	Input/output	nCTS0	–	–

PORT CONTROL DESCRIPTIONS

PORT CONFIGURATION REGISTER (GPACON-GPHCON)

In S3C2410X01, most pins are multiplexed pins. So, It is determined which function is selected for each pins. The PnCON (port control register) determines which function is used for each pin.

If PF0 – PF7 is used for the wakeup signal in power down mode, these ports must be configured in interrupt mode.

PORT DATA REGISTER (GPADAT-GPHDAT)

If Ports are configured as output ports, data can be written to the corresponding bit of PnDAT. If Ports are configured as input ports, the data can be read from the corresponding bit of PnDAT.

PORT PULL-UP REGISTER (GPBUP-GPHUP)

The port pull-up register controls the pull-up resister enable/disable of each port group. When the corresponding bit is 0, the pull-up resister of the pin is enabled. When 1, the pull-up resister is disabled.

If the port pull-up register is enabled then the pull-up resisters work without pin's functional setting (input, output, DATAn, EINTn and etc)

MISCELLANEOUS CONTROL REGISTER

This register controls DATA port pull-up resister, hi-z state or previous state in stop mode, USB pad, and CLKOUT selection.

EXTERNAL INTERRUPT CONTROL REGISTER

The 24 external interrupts are requested by various signaling methods. The EXTINT register configures the signaling method among the low level trigger, high level trigger, falling edge trigger, rising edge trigger, and both edge trigger for the external interrupt request

The 16 external interrupt pin has a digital filter.(Refer to EINTFLTn register)

Only 8 EINT pins (EINT [7:0]) are used for wake-up sources.

I/O PORT CONTROL REGISTER

PORT A CONTROL REGISTERS (GPACON, GPADAT)

Register	Address	R/W	Description	Reset Value
GPACON	0x56000000	R/W	Configures the pins of port A	0x7FFFFF
GPADAT	0x56000004	R/W	The data register for port A	Undefined
Reserved	0x56000008	-	Reserved	Undefined
Reserved	0x5600000C	-	Reserved	Undefined

GPACON	Bit	Description
GPA22	[22]	0 = Output 1 = nFCE
GPA21	[21]	0 = Output 1 = nRSTOUT (nRSTOUT = nRESET & nWDTRST & SW_RESET)
GPA20	[20]	0 = Output 1 = nFRE
GPA19	[19]	0 = Output 1 = nFWE
GPA18	[18]	0 = Output 1 = ALE
GPA17	[17]	0 = Output 1 = CLE
GPA16	[16]	0 = Output 1 = nGCS5
GPA15	[15]	0 = Output 1 = nGCS4
GPA14	[14]	0 = Output 1 = nGCS3
GPA13	[13]	0 = Output 1 = nGCS2
GPA12	[12]	0 = Output 1 = nGCS1
GPA11	[11]	0 = Output 1 = ADDR26
GPA10	[10]	0 = Output 1 = ADDR25
GPA9	[9]	0 = Output 1 = ADDR24
GPA8	[8]	0 = Output 1 = ADDR23
GPA7	[7]	0 = Output 1 = ADDR22
GPA6	[6]	0 = Output 1 = ADDR21
GPA5	[5]	0 = Output 1 = ADDR20
GPA4	[4]	0 = Output 1 = ADDR19
GPA3	[3]	0 = Output 1 = ADDR18
GPA2	[2]	0 = Output 1 = ADDR17
GPA1	[1]	0 = Output 1 = ADDR16
GPA0	[0]	0 = Output 1 = ADDR0

GPADAT	Bit	Description
GPA[22:0]	[22:0]	When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

PORT B CONTROL REGISTERS (GPBCON, GPBDAT, GPBUP)

Register	Address	R/W	Description	Reset Value
GPBCON	0x56000010	R/W	Configures the pins of port B	0x0
GPBDAT	0x56000014	R/W	The data register for port B	Undefined
GPBUP	0x56000018	R/W	Pull-up disable register for port B	0x0
Reserved	0x5600001C	-	Reserved	Undefined

PBCON	Bit	Description
GPB10	[21:20]	00 = Input 01 = Output 10 = nXDREQ0 11 = reserved
GPB9	[19:18]	00 = Input 01 = Output 10 = nXDACK0 11 = reserved
GPB8	[17:16]	00 = Input 01 = Output 10 = nXDREQ1 11 = Reserved
GPB7	[15:14]	00 = Input 01 = Output 10 = nXDACK1 11 = Reserved
GPB6	[13:12]	00 = Input 01 = Output 10 = nXBREQ 11 = reserved
GPB5	[11:10]	00 = Input 01 = Output 10 = nXBACK 11 = reserved
GPB4	[9:8]	00 = Input 01 = Output 10 = TCLK0 11 = reserved
GPB3	[7:6]	00 = Input 01 = Output 10 = TOUT3 11 = reserved
GPB2	[5:4]	00 = Input 01 = Output 10 = TOUT2 11 = reserved]
GPB1	[3:2]	00 = Input 01 = Output 10 = TOUT1 11 = reserved
GPB0	[1:0]	00 = Input 01 = Output 10 = TOUT0 11 = reserved

GPBDAT	Bit	Description
GPB[10:0]	[10:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPBUP	Bit	Description
GPB[10:0]	[10:0]	0 : The pull up function attached to to the corresponding port pin is enabled. 1 : The pull up function is disabled.

PORT C CONTROL REGISTERS (GPCCON, GPCDAT, GPCUP)

Register	Address	R/W	Description	Reset Value
GPCCON	0x56000020	R/W	Configures the pins of port C	0x0
GPCDAT	0x56000024	R/W	The data register for port C	Undefined
GPCUP	0x56000028	R/W	Pull-up disable register for port C	0x0
Reserved	0x5600002C	-	Reserved	Undefined

GPCCON	Bit	Description
GPC15	[31:30]	00 = Input 01 = Output 10 = VD[7] 11 = Reserved
GPC14	[29:28]	00 = Input 01 = Output 10 = VD[6] 11 = Reserved
GPC13	[27:26]	00 = Input 01 = Output 10 = VD[5] 11 = Reserved
GPC12	[25:24]	00 = Input 01 = Output 10 = VD[4] 11 = Reserved
GPC11	[23:22]	00 = Input 01 = Output 10 = VD[3] 11 = Reserved
GPC10	[21:20]	00 = Input 01 = Output 10 = VD[2] 11 = Reserved
GPC9	[19:18]	00 = Input 01 = Output 10 = VD[1] 11 = Reserved
GPC8	[17:16]	00 = Input 01 = Output 10 = VD[0] 11 = Reserved
GPC7	[15:14]	00 = Input 01 = Output 10 = LCDVF2 11 = Reserved
GPC6	[13:12]	00 = Input 01 = Output 10 = LCDVF1 11 = Reserved
GPC5	[11:10]	00 = Input 01 = Output 10 = LCDVF0 11 = Reserved
GPC4	[9:8]	00 = Input 01 = Output 10 = VM 11 = Reserved
GPC3	[7:6]	00 = Input 01 = Output 10 = VFRAME 11 = Reserved
GPC2	[5:4]	00 = Input 01 = Output 10 = VLINE 11 = Reserved
GPC1	[3:2]	00 = Input 01 = Output 10 = VCLK 11 = Reserved
GPC0	[1:0]	00 = Input 01 = Output 10 = LEND 11 = Reserved

GPCDAT	Bit	Description
GPC[15:0]	[15:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPCUP	Bit	Description
GPC[15:0]	[15:0]	0 : The pull up function attached to to the corresponding port pin is enabled. 1 : The pull up function is disabled.

PORT D CONTROL REGISTERS (GPDCON, GPDDAT, GPDUP)

Register	Address	R/W	Description	Reset Value
GPDCON	0x56000030	R/W	Configures the pins of port D	0x0
GPDDAT	0x56000034	R/W	The data register for port D	Undefined
GPDUP	0x56000038	R/W	Pull-up disable register for port D	0xF000
Reserved	0x5600003C	-	Reserved	Undefined

GPDCON	Bit	Description
GPD15	[31:30]	00 = Input 01 = Output 10 = VD23 11 = nSS0
GPD14	[29:28]	00 = Input 01 = Output 10 = VD22 11 = nSS1
GPD13	[27:26]	00 = Input 01 = Output 10 = VD21 11 = Reserved
GPD12	[25:24]	00 = Input 01 = Output 10 = VD20 11 = Reserved
GPD11	[23:22]	00 = Input 01 = Output 10 = VD19 11 = Reserved
GPD10	[21:20]	00 = Input 01 = Output 10 = VD18 11 = Reserved
GPD9	[19:18]	00 = Input 01 = Output 10 = VD17 11 = Reserved
GPD8	[17:16]	00 = Input 01 = Output 10 = VD16 11 = Reserved
GPD7	[15:14]	00 = Input 01 = Output 10 = VD15 11 = Reserved
GPD6	[13:12]	00 = Input 01 = Output 10 = VD14 11 = Reserved
GPD5	[11:10]	00 = Input 01 = Output 10 = VD13 11 = Reserved
GPD4	[9:8]	00 = Input 01 = Output 10 = VD12 11 = Reserved
GPD3	[7:6]	00 = Input 01 = Output 10 = VD11 11 = Reserved
GPD2	[5:4]	00 = Input 01 = Output 10 = VD10 11 = Reserved
GPD1	[3:2]	00 = Input 01 = Output 10 = VD9 11 = Reserved
GPD0	[1:0]	00 = Input 01 = Output 10 = VD8 11 = Reserved

GPDDAT	Bit	Description
GPD[15:0]	[15:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPDUP	Bit	Description
GPD[15:0]	[15:0]	0 : The pull up function attached to to the corresponding port pin is enabled. 1 : The pull up function is disabled. (GPD[15:12] are 'pull-up disabled' state at the initial condition.)

PORT E CONTROL REGISTERS (GPECON, GPEDAT, GPEUP)

Register	Address	R/W	Description	Reset Value
GPECON	0x56000040	R/W	Configures the pins of port E	0x0
GPEDAT	0x56000044	R/W	The data register for port E	Undefined
GPEUP	0x56000048	R/W	pull-up disable register for port E	0x0
Reserved	0x5600004C	-	Reserved	Undefined

PDCON	Bit	Description
GPE15	[31:30]	00 = Input 01 = Output 10 = IICSDA 11 = Reserved
GPE14	[29:28]	00 = Input 01 = Output 10 = IICSCL 11 = Reserved
GPE13	[27:26]	00 = Input 01 = Output 10 = SPICLK0 11 = Reserved
GPE12	[25:24]	00 = Input 01 = Output 10 = SPIMOSI0 11 = Reserved
GPE11	[23:22]	00 = Input 01 = Output 10 = SPIMISO0 11 = Reserved
GPE10	[21:20]	00 = Input 01 = Output 10 = SDDAT3 11 = Reserved
GPE9	[19:18]	00 = Input 01 = Output 10 = SDDAT2 11 = Reserved
GPE8	[17:16]	00 = Input 01 = Output 10 = SDDAT1 11 = Reserved
GPE7	[15:14]	00 = Input 01 = Output 10 = SDDAT0 11 = Reserved
GPE6	[13:12]	00 = Input 01 = Output 10 = SDCMD 11 = Reserved
GPE5	[11:10]	00 = Input 01 = Output 10 = SDCLK 11 = Reserved
GPE4	[9:8]	00 = Input 01 = Output 10 = I2SSDO 11 = I2SSDI
GPE3	[7:6]	00 = Input 01 = Output 10 = I2SSDI 11 = nSS0
GPE2	[5:4]	00 = Input 01 = Output 10 = CDCLK 11 = Reserved
GPE1	[3:2]	00 = Input 01 = Output 10 = I2SSCLK 11 = Reserved
GPE0	[1:0]	00 = Input 01 = Output 10 = I2SLRCK 11 = Reserved

GPEDAT	Bit	Description
GPE[15:0]	[15:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as a functional pin, the undefined value will be read.

PDUP	Bit	Description
GPE[15:0]	[15:0]	0 : The pull up function attached to to the corresponding port pin is enabled. 1 : The pull up function is disabled.

PORT F CONTROL REGISTERS (GPFCON, GPFDAT, GPFPU)

If GPF0 - GPF7 will be used for wake-up signals at power down mode, the ports will be set in interrupt mode.

Register	Address	R/W	Description	Reset Value
GPFCON	0x56000050	R/W	Configures the pins of port F	0x0
GPFDAT	0x56000054	R/W	The data register for port F	Undefined
GPFUP	0x56000058	R/W	Pull-up disable register for port F	0x0
Reserved	0x5600005C	-	Reserved	Undefined

PECON	Bit	Description	
GPF7	[15:14]	00 = Input 10 = EINT7	01 = Output 11 = Reserved
GPF6	[13:12]	00 = Input 10 = EINT6	01 = Output 11 = Reserved
GPF5	[11:10]	00 = Input 10 = EINT5	01 = Output 11 = Reserved
GPF4	[9:8]	00 = Input 10 = EINT4	01 = Output 11 = Reserved
GPF3	[7:6]	00 = Input 10 = EINT3	01 = Output 11 = Reserved
GPF2	[5:4]	00 = Input 10 = EINT2	01 = Output 11 = Reserved
GPF1	[3:2]	00 = Input 10 = EINT1	01 = Output 11 = Reserved
GPF0	[1:0]	00 = Input 10 = EINT0	01 = Output 11 = Reserved

NOTE :

GPFDAT	Bit	Description
GPF[7:0]	[7:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPFUP	Bit	Description
GPF[7:0]	[7:0]	0 : The pull up function attached to to the corresponding port pin is enabled. 1 : The pull up function is disabled.

PORT G CONTROL REGISTERS (GPGCON, GPGDAT, GPGUP)

Register	Address	R/W	Description	Reset Value
GPGCON	0x56000060	R/W	Configures the pins of port G	0x0
GPGDAT	0x56000064	R/W	The data register for port G	Undefined
GPGUP	0x56000068	R/W	Pull-up disable register for port G	0xF800
Reserved	0x5600006C	-	Reserved	Undefined

PECON	Bit	Description	
GPG15	[31:30]	00 = Input 10 = EINT23	01 = Output 11 = nYPON
GPG14	[29:28]	00 = Input 10 = EINT22	01 = Output 11 = YMON
GPG13	[27:26]	00 = Input 10 = EINT21	01 = Output 11 = nXPON
GPG12	[25:24]	00 = Input 10 = EINT20	01 = Output 11 = XMON
GPG11	[23:22]	00 = Input 10 = EINT19	01 = Output 11 = TCLK1
GPG10	[21:20]	00 = Input 10 = EINT18	01 = Output 11 = Reserved
GPG9	[19:18]	00 = Input 10 = EINT17	01 = Output 11 = Reserved
GPG8	[17:16]	00 = Input 10 = EINT16	01 = Output 11 = Reserved
GPG7	[15:14]	00 = Input 10 = EINT15	01 = Output 11 = SPICLK1
GPG6	[13:12]	00 = Input 10 = EINT14	01 = Output 11 = SPIMOSI1
GPG5	[11:10]	00 = Input 10 = EINT13	01 = Output 11 = SPIMISO1
GPG4	[9:8]	00 = Input 10 = EINT12	01 = Output 11 = LCD_PWRDN
GPG3	[7:6]	00 = Input 10 = EINT11	01 = Output 11 = nSS1
GPG2	[5:4]	00 = Input 10 = EINT10	01 = Output 11 = nSS0
GPG1	[3:2]	00 = Input 10 = EINT9	01 = Output 11 = Reserved
GPG0	[1:0]	00 = Input 10 = EINT8	01 = Output 11 = Reserved

GPGDAT	Bit	Description
GPG[15:0]	[15:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPGUP	Bit	Description
GPG[15:0]	[15:0]	0 : The pull up function attached to to the corresponding port pin is enabled. 1 : The pull up function is disabled. (GPG[15:11] are 'pull-up disabled' state at the initial condition.)

PORT H CONTROL REGISTERS (GPHCON, GPHDAT, GPHUP)

Register	Address	R/W	Description	Reset Value
GPHCON	0x56000070	R/W	Configures the pins of port H	0x0
GPHDAT	0x56000074	R/W	The data register for port H	Undefined
GPHUP	0x56000078	R/W	Pull-up disable register for port H	0x0
Reserved	0x5600007C	-	Reserved	Undefined

PECON	Bit	Description	
GPH10	[21:20]	00 = Input 10 = CLKOUT1	01 = Output 11 = Reserved
GPH9	[19:18]	00 = Input 10 = CLKOUT0	01 = Output 11 = Reserved
GPH8	[17:16]	00 = Input 10 = UCLK	01 = Output 11 = Reserved
GPH7	[15:14]	00 = Input 10 = RXD2	01 = Output 11 = nCTS1
GPH6	[13:12]	00 = Input 10 = TXD2	01 = Output 11 = nRTS1
GPH5	[11:10]	00 = Input 10 = RXD1	01 = Output 11 = Reserved
GPH4	[9:8]	00 = Input 10 = TXD1	01 = Output 11 = Reserved
GPH3	[7:6]	00 = Input 10 = RXD0	01 = Output 11 = reserved
GPH2	[5:4]	00 = Input 10 = TXD0	01 = Output 11 = Reserved
GPH1	[3:2]	00 = Input 10 = nRTS0	01 = Output 11 = Reserved
GPH0	[1:0]	00 = Input 10 = nCTS0	01 = Output 11 = Reserved

GPHDAT	Bit	Description
GPH[10:0]	[10:0]	When the port is configured as an input port, the corresponding bit is the pin state. When the port is configured as an output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

GPHUP	Bit	Description
GPH[10:0]	[10:0]	0 : The pull up function attached to to the corresponding port pin is enabled. 1 : The pull up function is disabled.

MISCELLANEOUS control register (MISCCR)

In STOP mode, the data bus (D[31:0] or D[15:0]) is Hi-Z state. But, because of the characteristics of IO pad, the data bus pull-up resisters have to be turned on to reduce the power consumption in STOP mode. D[31:0] pin pull-up resisters can be controlled by MISCCR register.
In STOP mode, memory control signals (A[26:0], nGCS[5:0], nWE, nOE, nBE:nWBE:DQM) can be selectable Hi-z state or previous state in order to protect memory mal-function by setting the HZ@STOP field in MISCCR register.
Pads related USB are controlled by this register for USB host, or for USB device.

Register	Address	R/W	Description	Reset Value
MISCCR	0x56000080	R/W	Miscellaneous control register	0x10330

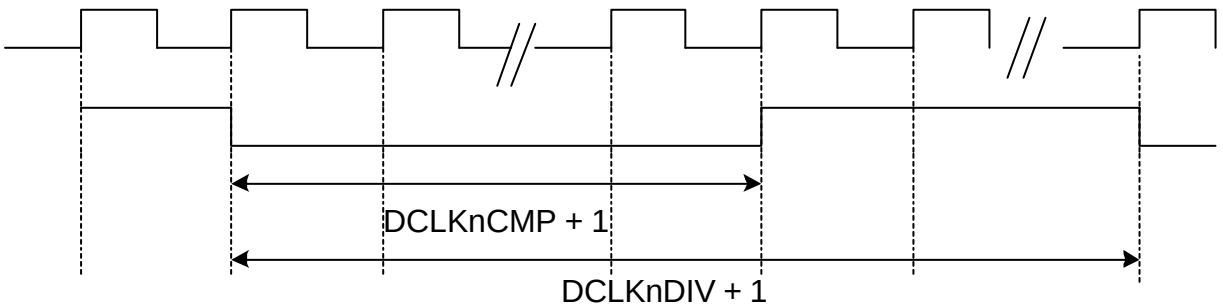
MISCCR	Bit	Description
nRSTCON	[16]	nRSTOUT software control(SW_RESET) 0 : nRSTOUT = 0, 1 : nRSTOUT = 1.
Reserved	[15:14]	00
USBSUSPND	[13:12]	[12] USB Port 0 mode 0 = Normal 1= Suspend [13] USB Port 1 mode 0 = Normal 1= Suspend
Reserved	[11]	0
CLKSEL1	[10:8]	000 = Select MPLL CLK with CLKOUT1 pad 001 = Select UPLL CLK with CLKOUT1 pad 010 = Select FCLK with CLKOUT1 pad 011 = Select HCLK with CLKOUT1 pad 100 = Select PCLK with CLKOUT1 pad 101 = Select DCLK1 with CLKOUT1 pad* 11x = Reserved
Reserved	[7]	0
CLKSEL0	[6:4]	000 = Select MPLL CLK with CLKOUT0 pad 001 = Select UPLL CLK with CLKOUT0 pad 010 = Select FCLK with CLKOUT0 pad 011 = Select HCLK with CLKOUT0 pad 100 = Select PCLK with CLKOUT0 pad 101 = Select DCLK0 with CLKOUT0 pad * 11x = Reserved
USBPAD	[3]	0 = Use pads related USB for USB device 1 = Use pads related USB for USB host
HZ@STOP	[2]	0 = HZ @ stop 1 = Previous state of PAD
SPUCR1	[1]	DATA[31:16] port pull-up resister 0 = Enabled 1 = Disabled
SPUCR0	[0]	DATA[15:0] port pull-up resister 0 = Enabled 1 = Disabled

NOTE : CLKOUT is prepared to monitor an internal clock situation (On/Off status or frequency)
DCLK0/1 means internal divide clock.

DCLK CONTROL REGISTERS (DCKCON)

Register	Address	R/W	Description	Reset Value
DCKCON	0x56000084	R/W	DCLK0/1 Control Register	0x0

DCKCON	Bit	Description
DCLK1CMP	[27:24]	DCLK1 Compare value clock toggle value. (< DCLK1DIV) If the DCLK1DIV is n, Low level duration is (n + 1). High level duration is ((DCLK1DIV + 1) – (n +1)).
DCLK1DIV	[23:20]	DCLK1 Divide value DCLK1 frequency = source clock / (DCLK1DIV + 1)
Reserved	[19:18]	00
DCLK1SelCK	[17]	Select DCLK1 source clock 0 = PCLK 1 = USBCLK (USB)
DCLK1EN	[16]	DCLK1 Enable 0 = Disable 1 = Enable
Reserved	[15:12]	0000
DCLK0CMP	[11:8]	DCLK0 Compare value clock toggle value. (< DCLK0DIV) If the DCLK0DIV is n, Low level duration is (n + 1). High level duration is ((DCLK0DIV + 1) – (n +1)).
DCLK0DIV	[7:4]	DCLK0 Divide value. DCLK0 frequency = source clock / (DCLK0DIV + 1)
Reserved	[3:2]	00
DCLK0SelCK	[1]	Select DCLK0 source clock 0 = PCLK 1 = USBCLK (USB)
DCLK0EN	[0]	DCLK0 Enable 0 = Disable 1 = Enable



EXTINTn (External Interrupt Control Register)

The 24 external interrupts can be requested by various signaling methods. The EXTINT register configures the signaling method between the level trigger and edge trigger for the external interrupt request, and also configures the signal polarity.

To recognize the level interrupt, the valid logic level on EXTINTn pin must be retained for 40ns at least because of the noise filter. (EINT[7:0])

Register	Address	R/W	Description	Reset Value
EXTINT0	0x56000088	R/W	External Interrupt control Register 0	0x0
EXTINT1	0x5600008C	R/W	External Interrupt control Register 1	0x0
EXTINT2	0x56000090	R/W	External Interrupt control Register 2	0x0

EXTINT0	Bit	Description
EINT7	[30:28]	Setting the signaling method of the EINT7. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT6	[26:24]	Setting the signaling method of the EINT6. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT5	[22:20]	Setting the signaling method of the EINT5. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT4	[18:16]	Setting the signaling method of the EINT4. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT3	[14:12]	Setting the signaling method of the EINT3. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT2	[10:8]	Setting the signaling method of the EINT2. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT1	[6:4]	Setting the signaling method of the EINT1. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
EINT0	[2:0]	Setting the signaling method of the EINT0. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered

EXTINT1	Bit	Description
FLTEN15	[31]	Filter Enable for EINT15 0 = Disable 1= Enable
EINT15	[30:28]	Setting the signaling method of the EINT15. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN14	[27]	Filter Enable for EINT14 0 = Disable 1= Enable
EINT14	[26:24]	Setting the signaling method of the EINT14. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN13	[23]	Filter Enable for EINT13 0 = Disable 1= Enable
EINT13	[22:20]	Setting the signaling method of the EINT13. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN12	[19]	Filter Enable for EINT12 0 = Disable 1= Enable
EINT12	[18:16]	Setting the signaling method of the EINT12. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN11	[15]	Filter Enable for EINT11 0 = Disable 1= Enable
EINT11	[14:12]	Setting the signaling method of the EINT11. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN10	[11]	Filter Enable for EINT10 0 = Disable 1= Enable
EINT10	[10:8]	Setting the signaling method of the EINT10. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN9	[7]	Filter Enable for EINT9 0 = Disable 1= Enable
EINT9	[6:4]	Setting the signaling method of the EINT9. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN8	[3]	Filter Enable for EINT8 0 = Disable 1= Enable
EINT8	[2:0]	Setting the signaling method of the EINT8. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered

EXTINT2	Bit	Description
FLTEN23	[31]	Filter Enable for EINT23 0 = Disable 1= Enable
EINT23	[30:28]	Setting the signaling method of the EINT23. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN22	[27]	Filter Enable for EINT22 0 = Disable 1= Enable
EINT22	[26:24]	Setting the signaling method of the EINT22. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN21	[23]	Filter Enable for EINT21 0 = Disable 1= Enable
EINT21	[22:20]	Setting the signaling method of the EINT21. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN20	[19]	Filter Enable for EINT20 0 = Disable 1= Enable
EINT20	[18:16]	Setting the signaling method of the EINT20. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN19	[15]	Filter Enable for EINT19 0 = Disable 1= Enable
EINT19	[14:12]	Setting the signaling method of the EINT19. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN18	[11]	Filter Enable for EINT18 0 = Disable 1= Enable
EINT18	[10:8]	Setting the signaling method of the EINT18. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN17	[7]	Filter Enable for EINT17 0 = Disable 1= Enable
EINT17	[6:4]	Setting the signaling method of the EINT17. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered
FLTEN16	[3]	Filter Enable for EINT16 0 = Disable 1= Enable
EINT16	[2:0]	Setting the signaling method of the EINT16. 000 = Low level 001 = High level 01x = Falling edge triggered 10x = Rising edge triggered 11x = Both edge triggered

EINTFLTn (External Interrupt Filter Register)

EINTFLTn control the length of filter for 16 external interrupts (EINT[23:8]).

Register	Address	R/W	Description	Reset Value
EINTFLT0	0x56000094	R/W	External Interrupt Control Register 0	0x0
EINTFLT1	0x56000098	R/W	External Interrupt Control Register 1	0x0
EINTFLT2	0x5600009C	R/W	External Interrupt Control Register 2	0x0
EINTFLT3	0x4C6000A0	R/W	External Interrupt Control Register 3	0x0

EINTFLT0	Bit	Description
FLTCLK11	[31]	Filter clock of EINT11 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT11	[30:24]	Filtering width of EINT11
FLTCLK10	[23]	Filter clock of EINT10 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT10	[22:16]	Filtering width of EINT10
FLTCLK9	[15]	Filter clock of EINT9 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT9	[14:8]	Filtering width of EINT9
FLTCLK8	[7]	Filter clock of EINT8 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT8	[6:0]	Filtering width of EINT8

EINTFLT1	Bit	Description
FLTCLK15	[31]	Filter clock of EINT15 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT15	[30:24]	Filtering width of EINT15
FLTCLK14	[23]	Filter clock of EINT14 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT14	[22:16]	Filtering width of EINT14
FLTCLK13	[15]	Filter clock of EINT13 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT13	[14:8]	Filtering width of EINT13
FLTCLK12	[7]	Filter clock of EINT12 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT12	[6:0]	Filtering width of EINT12

EINTFLT2	Bit	Description
FLTCLK19	[31]	Filter clock of EINT19 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT19	[30:24]	Filtering width of EINT19
FLTCLK18	[23]	Filter clock of EINT18 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT18	[22:16]	Filtering width of EINT18
FLTCLK17	[15]	Filter clock of EINT17 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT17	[14:8]	Filtering width of EINT17
FLTCLK16	[7]	Filter clock of EINT16 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT16	[6:0]	Filtering width of EINT16

EINTFLT3	Bit	Description
FLTCLK23	[31]	Filter clock of EINT23 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT23	[30:24]	Filtering width of EINT23
FLTCLK22	[23]	Filter clock of EINT22 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT22	[22:16]	Filtering width of EINT22
FLTCLK21	[15]	Filter clock of EINT21 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT21	[14:8]	Filtering width of EINT21
FLTCLK20	[7]	Filter clock of EINT20 0 = PCLK 1= EXTCLK/OSC_CLK (Selected by OM pin)
EINTFLT20	[6:0]	Filtering width of EINT20

EINTMASK (External Interrupt Mask Register)

Interrupt mask register for 20 external interrupts (EINT[23:4]).

Register	Address	R/W	Description	Reset Value
EINTMASK	0x560000A4	R/W	External interupt mask Register	0x00FFFFF0

EINTMASK	Bit	Description
EINT23	[23]	0 = Enable Interrupt 1= Masked
EINT22	[22]	0 = Enable Interrupt 1= Masked
EINT21	[21]	0 = Enable Interrupt 1= Masked
EINT20	[20]	0 = Enable Interrupt 1= Masked
EINT19	[19]	0 = Enable Interrupt 1= Masked
EINT18	[18]	0 = Enable Interrupt 1= Masked
EINT17	[17]	0 = Enable Interrupt 1= Masked
EINT16	[16]	0 = Enable Interrupt 1= Masked
EINT15	[15]	0 = Enable Interrupt 1= Masked
EINT14	[14]	0 = Enable Interrupt 1= Masked
EINT13	[13]	0 = Enable Interrupt 1= Masked
EINT12	[12]	0 = Enable Interrupt 1= Masked
EINT11	[11]	0 = Enable Interrupt 1= Masked
EINT10	[10]	0 = Enable Interrupt 1= Masked
EINT9	[9]	0 = Enable Interrupt 1= Masked
EINT8	[8]	0 = Enable Interrupt 1= Masked
EINT7	[7]	0 = Enable Interrupt 1= Masked
EINT6	[6]	0 = Enable Interrupt 1= Masked
EINT5	[5]	0 = Enable Interrupt 1= Masked
EINT4	[4]	0 = Enable Interrupt 1= Masked
Reserved	[3:0]	0

EINTPENDn (External Interrupt Pending Registern)

Interrupt pending register for 20 external interrupts (EINT[23:4]).

Register	Address	R/W	Description	Reset Value
EINTPEND	0x560000A8	R/W	External Interupt Pending Register	0x0

EINTPEND	Bit	Description
EINT23	[23]	0 = Not occur 1= Occur interrupt It is cleared by writing “1”
EINT22	[22]	
EINT21	[21]	
EINT20	[20]	
EINT19	[19]	
EINT18	[18]	
EINT17	[17]	
EINT16	[16]	
EINT15	[15]	0 = Not occur 1= Occur interrupt It is cleared by writing “1”
EINT14	[14]	
EINT13	[13]	
EINT12	[12]	
EINT11	[11]	
EINT10	[10]	
EINT9	[9]	
EINT8	[8]	
EINT7	[7]	0 = Not occur 1= Occur interrupt It is cleared by writing “1”
EINT6	[6]	
EINT5	[5]	
EINT4	[4]	
Reserved	[3:0]	0

GSTATUSn (General Status Register)

Register	Address	R/W	Description	Reset Value
GSTATUS0	0x560000AC	R	External pin status	Undefined
GSTATUS1	0x560000B0	R/W	Chip ID	0x32410000

GSTATUS0	Bit	Description
nWAIT	[3]	Status of nWAIT pin
NCON1	[2]	Status of NCON1 pin
NCON0	[1]	Status of NCON0 pin
BATT_FLT	[0]	Status of BATT_FLT pin

GSTATUS1	Bit	Description
CHIP ID	[0]	ID register = 0x32410000

10 PWM TIMER(Preliminary)

OVERVIEW

The S3C2410X01 has five 16-bit timers. The timer 0, 1, 2, 3 have PWM function(Pulse Width Modulation). Timer 4 has an internal timer only with no output pins. Timer 0 has a dead-zone generator, which is used with a large current device.

Timer 0 and timer 1 share an 8-bit prescaler, timers 2, 3 and 4 share the other 8-bit prescaler. Each timer has a clock-divider which has 5 different divided signals (1/2, 1/4, 1/8, 1/16, TCLK). Each timer block receives its own clock signals from the clock-divider, which receives the clock from the corresponding 8-bit prescaler. The 8-bit prescaler is programmable and divides the PCLK according to the loading value, which is stored in TCFG0 and TCFG1 registers.

The timer count buffer register(TCNTBn) has an initial value which is loaded into the down-counter when the timer is enabled. The timer compare buffer register(TCMPBn) has an initial value which is loaded into the compare register to be compared with the down-counter value. This double buffering feature of TCNTBn and TCMPBn makes the timer generate a stable output when the frequency and duty ratio are changed.

Each timer has its own 16-bit down counter, which is driven by the timer clock. When the down counter reaches zero, the timer interrupt request is generated to inform the CPU that the timer operation has been completed. When the timer counter reaches zero, the value of corresponding TCNTBn is automatically loaded into the down counter to continue the next operation. However, if the timer stops, for example, by clearing the timer enable bit of TCONn during the timer running mode, the value of TCNTBn will not be reloaded into the counter.

The value of TCMPBn is used for PWM (pulse width modulation). The timer control logic changes the output level when the down-counter value matches the value of the compare register in the timer control logic. Therefore, the compare register determines the turn-on time(or turn-off time) of an PWM output.

FEATURE

- Five 16-bit timers
- Two 8-bit prescalers & Two 4-bit divider
- Programmable duty control of output waveform (PWM)
- Auto-reload mode or one-shot pulse mode
- Dead-zone generator

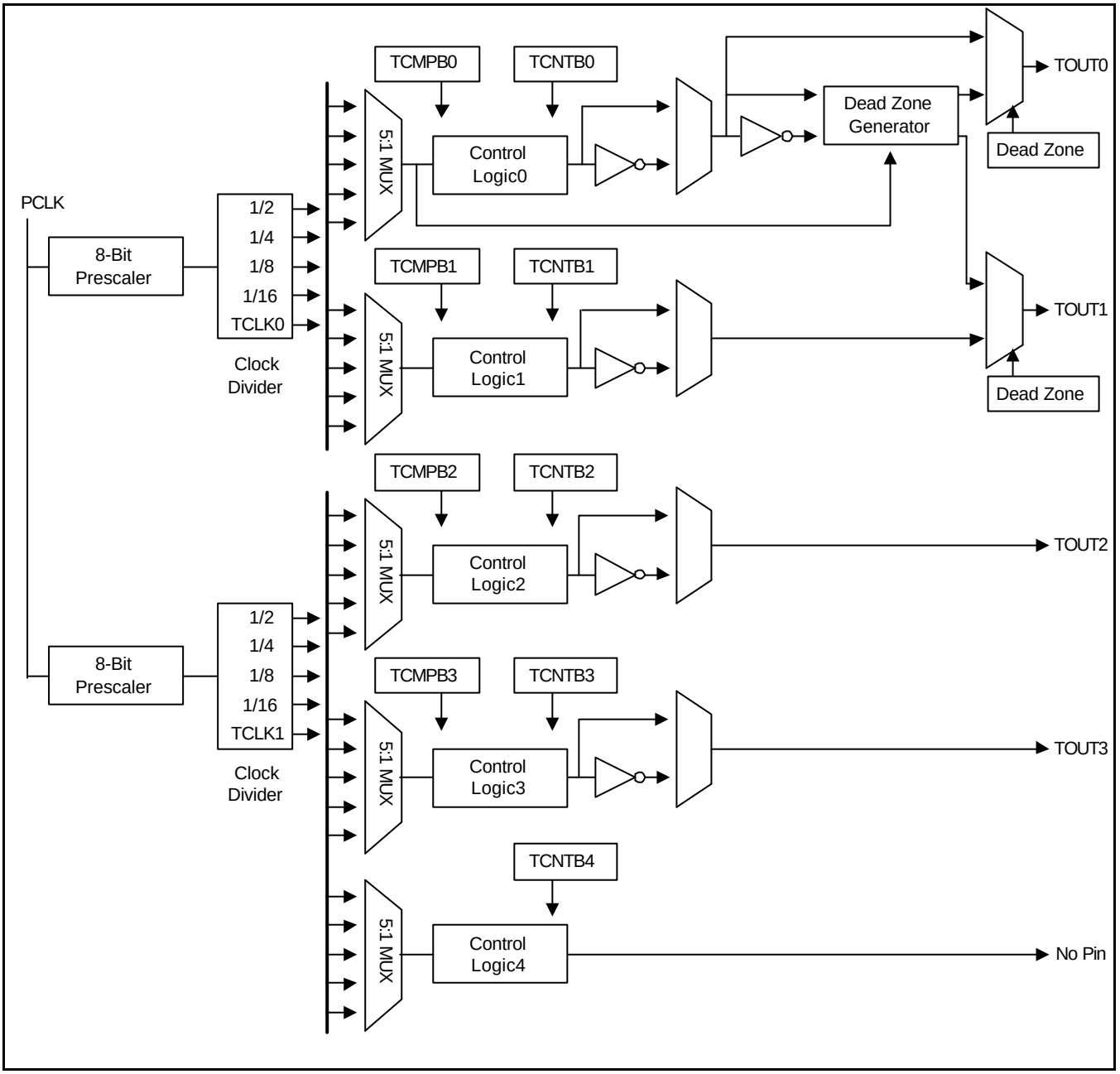


Figure 10-1. 16-bit PWM Timer Block Diagram

PWM TIMER OPERATION

PRESCALER & DIVIDER

An 8-bit prescaler and 4-bit divider make the following output frequencies:

4-bit divider settings	minimum resolution (prescaler = 0)	maximum resolution (prescaler = 255)	maximum interval (TCNTBn = 65535)
1/2 (PCLK = 66 MHz)	0.0303 us (33.0000 MHz)	7.7575 us (128.9063 KHz)	0.5084 sec
1/4 (PCLK = 66 MHz)	0.0606 us (16.5000 MHz)	15.5151 us (64.4531 KHz)	1.0168 sec
1/8 (PCLK = 66 MHz)	0.1212 us (8.2500 MHz)	31.0303 us (32.2266 KHz)	2.0336 sec
1/16 (PCLK = 66 MHz)	0.2424 us (4.1250 MHz)	62.0606 us (16.1133 KHz)	4.0671 sec

BASIC TIMER OPERATION

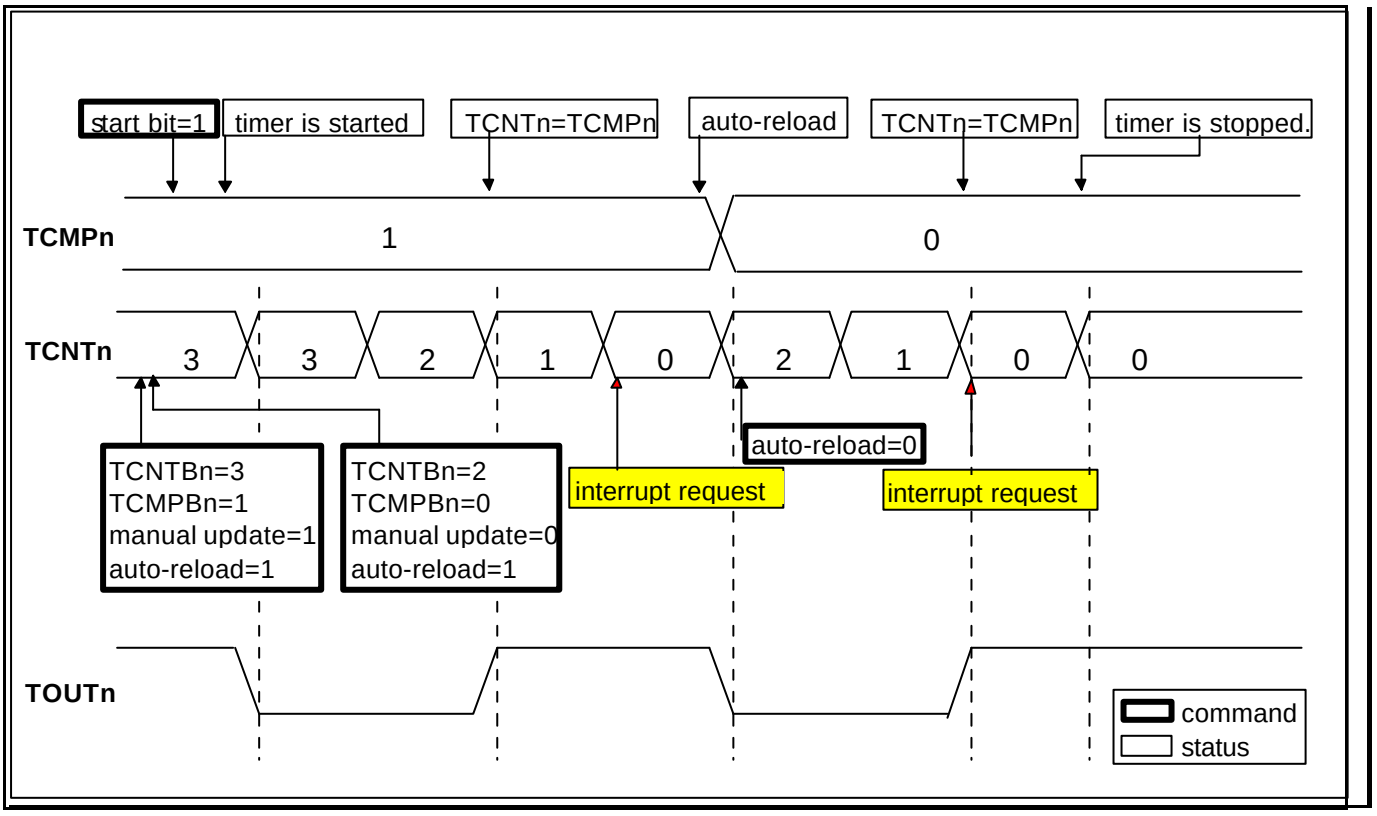


Figure 10-2. Timer operations

A timer (except the timer ch-5) has TCNTBn, TCNTn, TCMPBn and TCMPn. TCNTBn and TCMPBn are loaded into TCNTn and TCMPn when the timer reaches 0. When TCNTn reaches 0, the interrupt request will occur if the interrupt is enabled. (TCNTn and TCMPn are the names of the internal registers. The TCNTn register can be read from the TCNTOn register)

AUTO-RELOAD & DOUBLE BUFFERING

S3C2410X01 PWM Timers have a double buffering feature, which can change the reload value for the next timer operation without stopping the current timer operation. So, although the new timer value is set, a current timer operation is completed successfully.

The timer value can be written into TCNTBn (Timer Count Buffer register) and the current counter value of the timer can be read from TCNTOn (Timer Count Observation register). If TCNTBn is read, the read value is not the current state of the counter but the reload value for the next timer duration.

The auto-reload is the operation, which copies the TCNTBn into TCNTn when TCNTn reaches 0. The value, written into TCNTBn, is loaded to TCNTn only when the TCNTn reaches to 0 and auto-reload is enabled. If the TCNTn is 0 and the auto-reload bit is 0, the TCNTn does not operate any further.

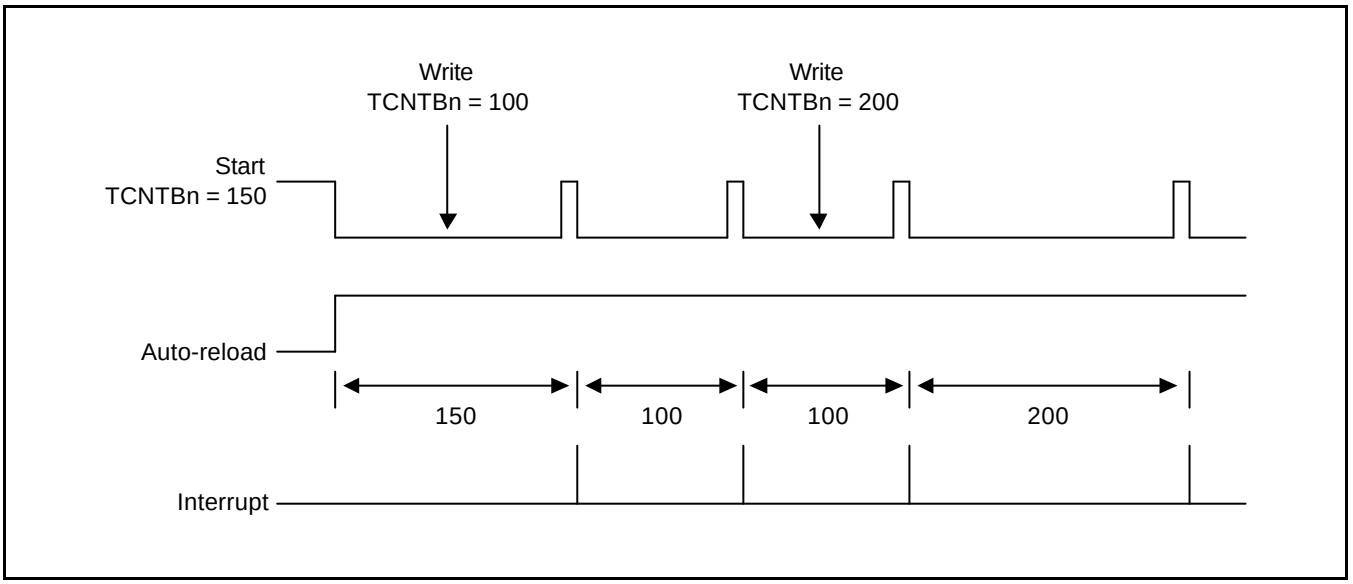


Figure 10-3. Example of Double Buffering Feature

TIMER INITIALIZATION USING MANUAL UPDATE BIT AND INVERTER BIT

Because an auto-reload operation of the timer occurs when the down counter reaches to 0, a starting value of the TCNTn has to be defined by the user at first. In this case, the starting value has to be loaded by the manual update bit. The sequence of starting a timer is as follows;

1) Write the initial value into TCNTBn and TCMPBn

2) Set the manual update bit of the corresponding timer. It is recommended to configure the inverter on/off bit. (whether use inverter or not)

3) Set start bit of corresponding timer to start the timer(At the same time, clear the manual update bit).

Also, if the timer is stopped by force, the TCNTn retains the counter value and is not reloaded from TCNTBn. If new value has to be set, manual update has to be done.

NOTE

Whenever TOUT inverter on/off bit is changed, the TOUTn logic value will be changed whether or not the timer runs. Therefore, it is desirable that the inverter on/off bit is configured with the manual update bit.

EXAMPLE OF A TIMER OPERATION

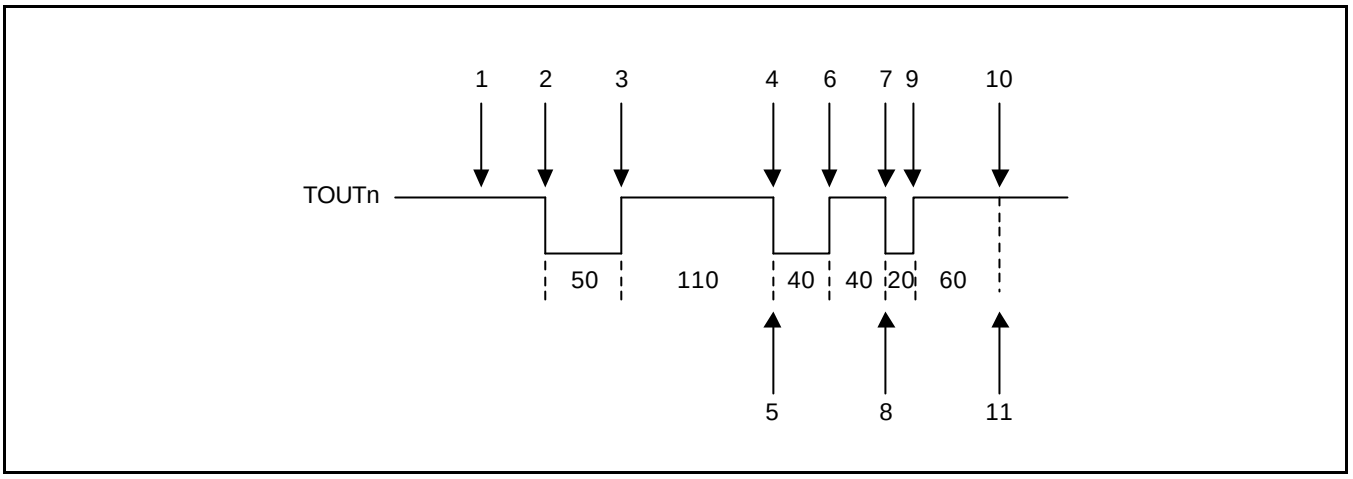


Figure 10-4. Example of a Timer Operation

The result of the following procedure is shown in Figure10-4;

1. Enable the auto-reload feature. Set the TCNTBn as 160 (50+110) and the TCMPBn as 110. Set the manual update bit and configure the inverter bit(on/off). The manual update bit sets TCNTn and TCMPn to the values of TCNTBn and TCMPBn, respectively.

   And then, set TCNTBn and TCMPBn as 80 (40+40) and 40, respectively, to determine the next reload value.
2. Set the start bit, provided that manual_update is 0 and inverter is off and auto-reload is on. The timer starts counting down after latency time within the timer resolution.
3. When TCNTn has the same value with TCMPn, the logic level of TOUTn is changed from low to high.
4. When TCNTn reaches 0, the interrupt request is generated and TCNTBn value is loaded into a temporary register. At the next timer tick, TCNTn is reloaded with the temporary register value(TCNTBn).
5. In the ISR(Interrupt Service Routine), the TCNTBn and TCMPBn are set as 80 (20+60) and 60, respectively, which is used for the next duration.
6. When TCNTn has the same value as TCMPn, the logic level of TOUTn is changed from low to high.
7. When TCNTn reaches 0, TCNTn is reloaded automatically with TCNTBn. At the same time, the interrupt request is generated.
8. In the ISR (Interrupt Service Routine), auto-reload and interrupt request are disabled to stop the timer.
9. When the value of TCNTn is same as TCMPn, the logic level of TOUTn is changed from low to high.
10. Even when TCNTn reaches to 0, TCNTn is not any more reloaded and the timer is stopped because auto-reload has been disabled.
11. No interrupt request is generated.

PWM (PULSE WIDTH MODULATION)

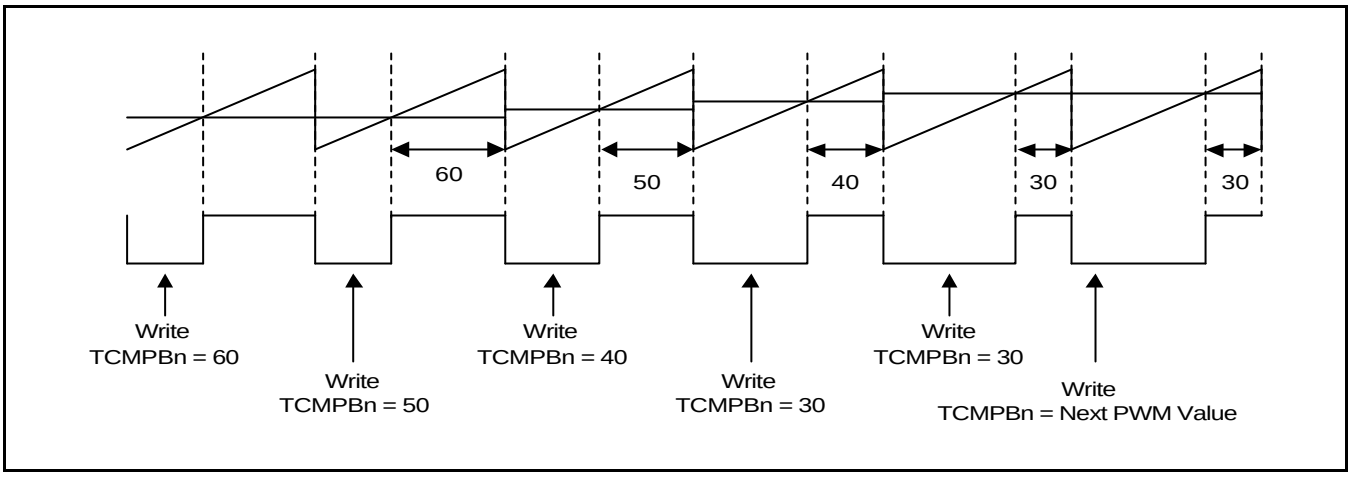


Figure 10-5. Example of PWM

PWM feature can be implemented by using the TCMPBn. PWM frequency is determined by TCNTBn. A PWM value is determined by TCMPBn in figure 10-5.

For a higher PWM value, decrease the TCMPBn value. For a lower PWM value, increase the TCMPBn value. If an output inverter is enabled, the increment/decrement may be reversed.

Because of the double buffering feature, TCMPBn, for a next PWM cycle, can be written at any point in the current PWM cycle by ISR or something else

OUTPUT LEVEL CONTROL

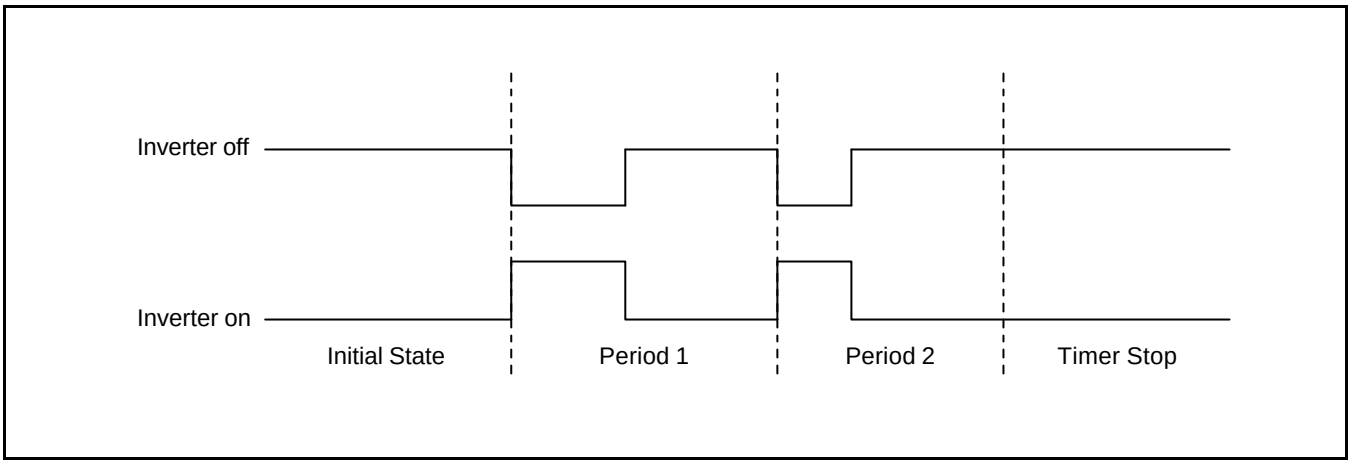


Figure 10-6. Inverter On/Off

The following methods can be used to maintain TOUT as high or low.(assume the inverter is off)

1. Turn off the auto-reload bit. And then, TOUTn goes to high level and the timer is stopped after TCNTn reaches to 0. This method is recommended.
2. Stop the timer by clearing the timer start/stop bit to 0. If TCNTn ≤ TCMPn, the output level is **high**. If TCNTn >TCMPn, the output level is **low**.
3. TOUTn can be inverted by the inverter on/off bit in TCON. The inverter removes the additional circuit to adjust the output level.

DEAD ZONE GENERATOR

The dead zone is for the PWM control in a power device. This feature is used to insert the time gap between a turn-off of a switching device and a turn on of another switching device. This time gap prohibits the two switching devices turning on simultaneously, even for a very short time.

TOUT0 is the PWM output. nTOUT0 is the inversion of the TOUT0. If the dead zone is enabled, the output wave form of TOUT0 and nTOUT0 will be TOUT0_DZ and nTOUT0_DZ, respectively. nTOUT0_DZ is routed to the TOUT1 pin.

In the dead zone interval, TOUT0_DZ and nTOUT0_DZ can never be turned on simultaneously.

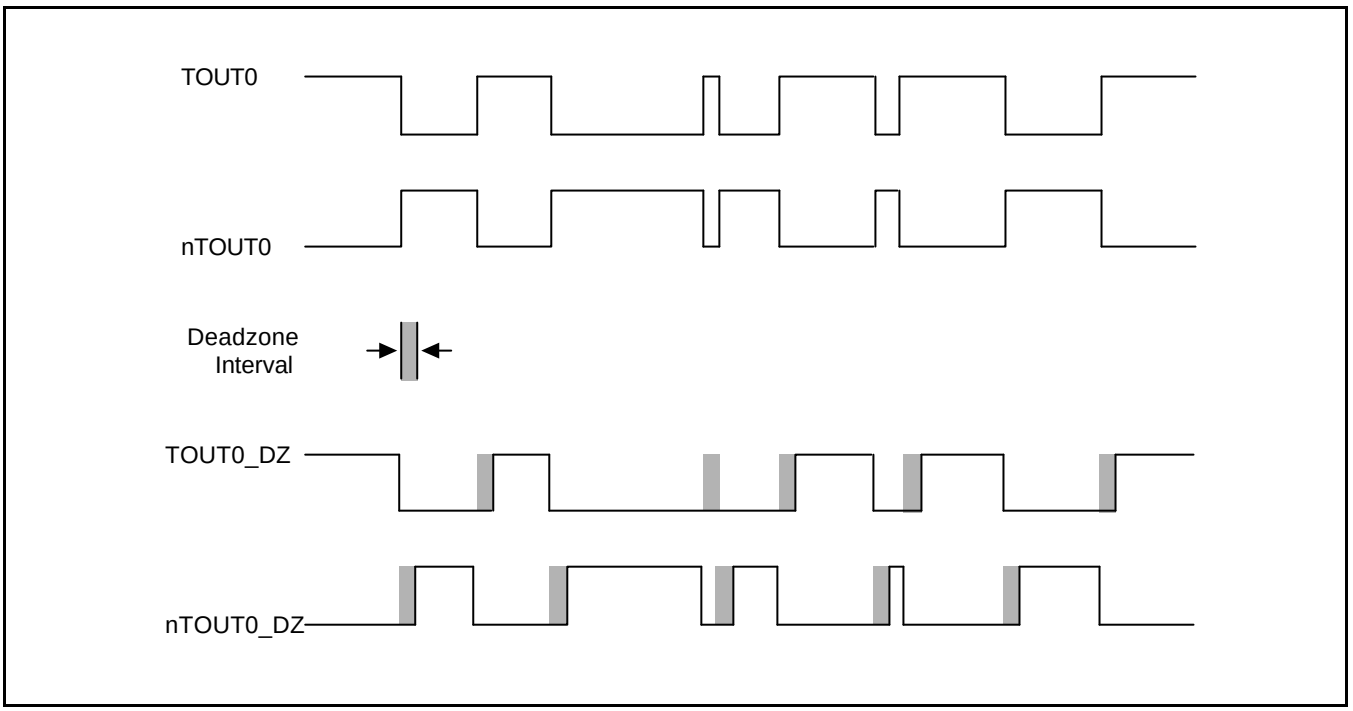


Figure 10-7. The Wave Form When a Dead Zone Feature is Enabled

DMA REQUEST MODE

The PWM timer can generate a DMA request at every specific times. The timer keeps DMA request signal (nDMA_REQ) low until the timer receives the ACK signal. When the timer receives the ACK signal, it makes the request signal inactive. The timer, which generates the DMA request, is determined by setting DMA mode bits(in TCFG1 register). If one of timers is configured as DMA request mode, that timer does not generate an interrupt request. The others can generate interrupt normally.

DMA mode configuration and DMA / interrupt operation

DMA mode	DMA request	Timer0 INT	Timer1 INT	Timer2 INT	Timer3 INT	Timer4 INT
0000	No select	ON	ON	ON	ON	ON
0001	Timer0	OFF	ON	ON	ON	ON
0010	Timer1	ON	OFF	ON	ON	ON
0011	Timer2	ON	ON	OFF	ON	ON
0100	Timer3	ON	ON	ON	OFF	ON
0101	Timer4	ON	ON	ON	ON	OFF
0110	No select	ON	ON	ON	ON	ON

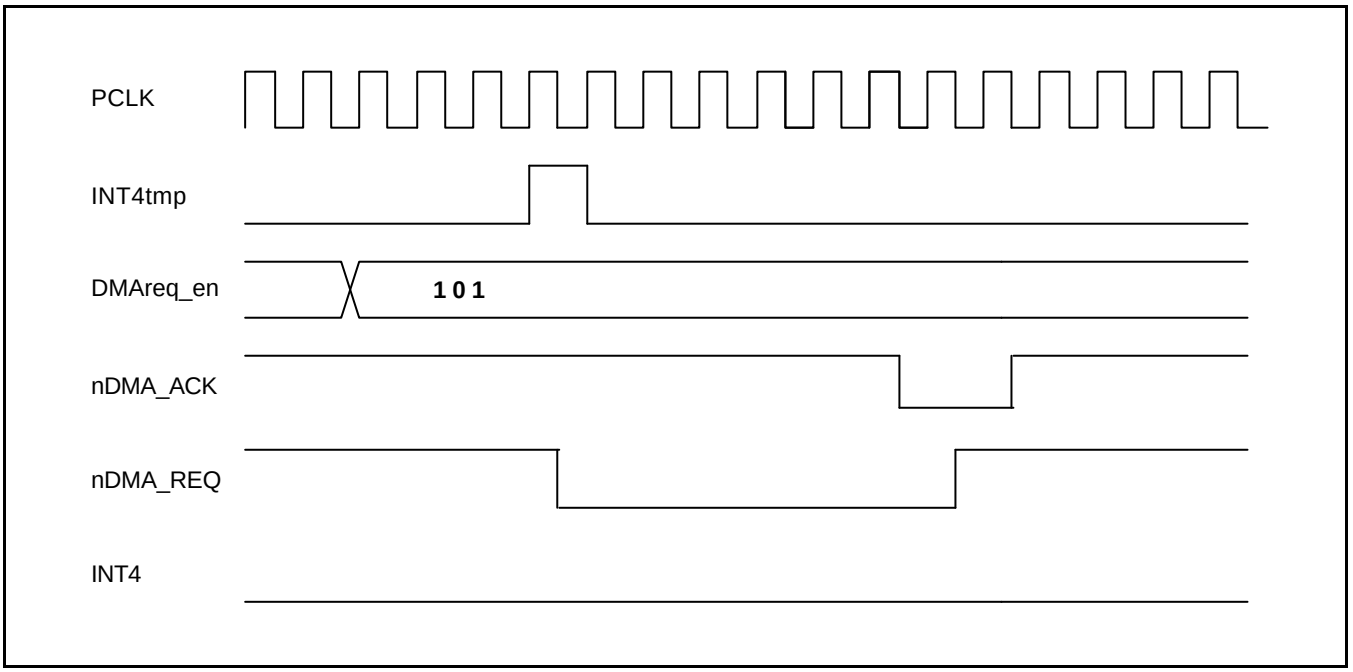


Figure 10-8. The Timer4 DMA mode operation

PWM TIMER CONTROL REGISTERS

TIMER CONFIGURATION REGISTER0 (TCFG0)

Timer input clock Frequency = PCLK / {prescaler value+1} / {divider value}
{prescaler value} = 0~255
{divider value} = 2, 4, 8, 16

Register	Address	R/W	Description	Reset Value
TCFG0	0x51000000	R/W	Configures the two 8-bit prescalers	0x00000000

TCFG0	Bit	Description	Initial State
Reserved	[31:24]		0x00
Dead zone length	[23:16]	These 8 bits determine the dead zone length. The 1 unit time of the dead zone length is equal to the 1 unit time of timer 0.	0x00
Prescaler 1	[15:8]	These 8 bits determine prescaler value for Timer 2, 3 and 4	0x00
Prescaler 0	[7:0]	These 8 bits determine prescaler value for Timer 0 and 1	0x00

TIMER CONFIGURATION REGISTER1 (TCFG1)

Register	Address	R/W	Description	Reset Value
TCFG1	0x51000004	R/W	5-MUX & DMA mode selecton register	0x00000000

TCFG1	Bit	Description	Initial State
Reserved	[31:24]		00000000
DMA mode	[23:20]	Select DMA request channel 0000 = No select(All interrupt) 0001 = Timer0 0010 = Timer1 0011 = Timer2 0100 = Timer3 0101 = Timer4 0110 = Reserved	0000
MUX 4	[19:16]	Select MUX input for PWM Timer4. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK1	0000
MUX 3	[15:12]	Select MUX input for PWM Timer3. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK1	0000
MUX 2	[11:8]	Select MUX input for PWM Timer2. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK1	0000
MUX 1	[7:4]	Select MUX input for PWM Timer1. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK0	0000
MUX 0	[3:0]	Select MUX input for PWM Timer0. 0000 = 1/2 0001 = 1/4 0010 = 1/8 0011 = 1/16 01xx = External TCLK0	0000

TIMER CONTROL REGISTER (TCON)

Register	Address	R/W	Description	Reset Value
TCON	0x51000008	R/W	Timer control register	0x00000000

TCON	Bit	Description	initial state
Timer 4 auto reload on/off	[22]	This bit determines auto reload on/off for Timer 4. 0 = One-shot 1 = Interval mode (auto reload)	0
Timer 4 manual update (note)	[21]	This bit determines the manual update for Timer 4. 0 = No operation 1 = Update TCNTB4	0
Timer 4 start/stop	[20]	This bit determines start/stop for Timer 4. 0 = Stop 1 = Start for Timer 4	0
Timer 3 auto reload on/off	[19]	This bit determines auto reload on/off for Timer 3. 0 = One-shot 1 = Interval mode (auto reload)	0
Timer 3 output inverter on/off	[18]	This bit determines output inverter on/off for Timer 3. 0 = Inverter off 1 = Inverter on for TOUT3	0
Timer 3 manual update (note)	[17]	This bit determine manual update for Timer 3. 0 = No operation 1 = Update TCNTB3, TCMPB3	0
Timer 3 start/stop	[16]	This bit determines start/stop for Timer 3. 0 = Stop 1 = Start for Timer 3	0
Timer 2 auto reload on/off	[15]	This bit determines auto reload on/off for Timer 2. 0 = One-shot 1 = Interval mode (auto reload)	0
Timer 2 output inverter on/off	[14]	This bit determines output inverter on/off for Timer 2. 0 = Inverter off 1 = Inverter on for TOUT2	0
Timer 2 manual update (note)	[13]	This bit determines the manual update for Timer 2. 0 = No operation 1 = Update TCNTB2, TCMPB2	0
Timer 2 start/stop	[12]	This bit determines start/stop for Timer 2. 0 = Stop 1 = Start for Timer 2	0
Timer 1 auto reload on/off	[11]	This bit determines the auto reload on/off for Timer1. 0 = One-shot 1 = Interval mode (auto reload)	0
Timer 1 output inverter on/off	[10]	This bit determines the output inverter on/off for Timer1. 0 = Inverter off 1 = Inverter on for TOUT1	0
Timer 1 manual update (note)	[9]	This bit determines the manual update for Timer 1. 0 = No operation 1 = Update TCNTB1, TCMPB1	0
Timer 1 start/stop	[8]	This bit determines start/stop for Timer 1. 0 = Stop 1 = Start for Timer 1	0

NOTE: This bit has to be cleared at next writing.

TCON(Continued)

TCON	Bit	Description	initial state
Dead zone enable	[4]	This bit determines the dead zone operation. 0 = Disable 1 = Enable	0
Timer 0 auto reload on/off	[3]	This bit determines auto reload on/off for Timer 0. 0 = One-shot 1 = Interval mode(auto reload)	0
Timer 0 output inverter on/off	[2]	This bit determines the output inverter on/off for Timer 0. 0 = Inverter off 1 = Inverter on for TOUT0	0
Timer 0 manual update (note)	[1]	This bit determines the manual update for Timer 0. 0 = No operation 1 = Update TCNTB0, TCMPB0	0
Timer 0 start/stop	[0]	This bit determines start/stop for Timer 0. 0 = Stop 1 = Start for Timer 0	0

NOTE: This bit has to be cleared at next writing.

TIMER 0 COUNT BUFFER REGISTER & COMPARE BUFFER REGISTER (TCNTB0, TCMPB0)

Register	Address	R/W	Description	Reset Value
TCNTB0	0x5100000C	R/W	Timer 0 count buffer register	0x00000000
TCMPB0	0x51000010	R/W	Timer 0 compare buffer register	0x00000000

TCMPB0	Bit	Description	Initial State
Timer 0 compare buffer register	[15:0]	Setting compare buffer value for Timer 0	0x00000000

TCNTB0	Bit	Description	Initial State
Timer 0 count buffer register	[15:0]	Setting count buffer value for Timer 0	0x00000000

TIMER 0 COUNT OBSERVATION REGISTER (TCNTO0)

Register	Address	R/W	Description	Reset Value
TCNTO0	0x51000014	R	Timer 0 count observation register	0x00000000

TCNTO0	Bit	Description	Initial State
Timer 0 observation register	[15:0]	Setting count observation value for Timer 0	0x00000000

TIMER 1 COUNT BUFFER REGISTER & COMPARE BUFFER REGISTER (TCNTB1, TCMPB1)

Register	Address	R/W	Description	Reset Value
TCNTB1	0x51000018	R/W	Timer 1 count buffer register	0x00000000
TCMPB1	0x5100001C	R/W	Timer 1 campare buffer register	0x00000000

TCMPB1	Bit	Description	Initial State
Timer 1 compare buffer register	[15:0]	Setting compare buffer value for Timer 1	0x00000000

TCNTB1	Bit	Description	Initial State
Timer 1 count buffer register	[15:0]	Setting count buffer value for Timer 1	0x00000000

Timer 1 Count Observation Register(TCNTO1)

Register	Address	R/W	Description	Reset Value
TCNTO1	0x51000020	R	Timer 1 count observation register	0x00000000

TCNTO1	Bit	Description	initial state
Timer 1 observation register	[15:0]	Setting count observation value for Timer 1	0x00000000

TIMER 2 COUNT BUFFER REGISTER & COMPARE BUFFER REGISTER (TCNTB2, TCMPB2)

Register	Address	R/W	Description	Reset Value
TCNTB2	0x51000024	R/W	Timer 2 count buffer register	0x00000000
TCMPB2	0x51000028	R/W	Timer 2 campare buffer register	0x00000000

TCMPB2	Bit	Description	Initial State
Timer 2 compare buffer register	[15:0]	Setting compare buffer value for Timer 2	0x00000000

TCNTB2	Bit	Description	Initial State
Timer 2 count buffer register	[15:0]	Setting count buffer value for Timer 2	0x00000000

TIMER 2 COUNT OBSERVATION REGISTER (TCNTO2)

Register	Address	R/W	Description	Reset Value
TCNTO2	0x5100002C	R	Timer 2 count observation register	0x00000000

TCNTO2	Bit	Description	Initial State
Timer 2 observation register	[15:0]	Setting count observation value for Timer 2	0x00000000

TIMER 3 COUNT BUFFER REGISTER & COMPARE BUFFER REGISTER (TCNTB3, TCMPB3)

Register	Address	R/W	Description	Reset Value
TCNTB3	0x51000030	R/W	Timer 3 count buffer register	0x00000000
TCMPB3	0x51000034	R/W	Timer 3 campare buffer register	0x00000000

TCMPB3	Bit	Description	Initial State
Timer 3 compare buffer register	[15:0]	Setting compare buffer value for Timer 3	0x00000000

TCNTB3	Bit	Description	Initial State
Timer 3 count buffer register	[15:0]	Setting count buffer value for Timer 3	0x00000000

TIMER 3 COUNT OBSERVATION REGISTER (TCNTO3)

Register	Address	R/W	Description	Reset Value
TCNTO3	0x51000038	R	Timer 3 count observation register	0x00000000

TCNTO3	Bit	Description	Initial State
Timer 3 observation register	[15:0]	Setting count observation value for Timer 3	0x00000000

TIMER 4 COUNT BUFFER REGISTER (TCNTB4)

Register	Address	R/W	Description	Reset Value
TCNTB4	0x5100003C	R/W	Timer 4 count buffer register	0x00000000

TCNTB4	Bit	Description	Initial State
Timer 4 count buffer register	[15:0]	Setting count buffer value for Timer 4	0x00000000

TIMER 4 COUNT OBSERVATION REGISTER (TCNTO4)

Register	Address	R/W	Description	Reset Value
TCNTO4	0x51000040	R	Timer 4 count observation register	0x00000000

TCNTO4	Bit	Description	Initial State
Timer 4 observation register	[15:0]	Setting count observation value for Timer 4	0x00000000

11 UART(Preliminary)

OVERVIEW

The S3C2410X01 UART (Universal Asynchronous Receiver and Transmitter) unit provides three independent asynchronous serial I/O (SIO) ports, each of which can operate in interrupt-based or DMA-based mode. In other words, UART can generate an interrupt or DMA request to transfer data between CPU and UART. It can support bit rates of up to 115.2K bps, when UART use system clock. If external device provides UART with UCLK, then UART can operates at more higher speed. Each UART channel contains two 16-byte FIFOs for receive and transmit.

The S3C2410X01 UART includes programmable baud-rates, infra-red (IR) transmit/receive, one or two stop bit insertion, 5-bit, 6-bit, 7-bit or 8-bit data width and parity checking.

Each UART contains a baud-rate generator, transmitter, receiver and control unit, as shown in Figure11-1. The baud-rate generator can be clocked by PCLK. The transmitter and the receiver contain 16-byte FIFOs and data shifters. Data, which is to be transmitted, is written to FIFO and then copied to the transmit shifter. It is then shifted out by the transmit data pin (TxDn). The received data is shifted from the receive data pin (RxDn), and then copied to FIFO from the shifter.

FEATURES

— RxD0, TxD0, RxD1, TxD1, RxD2, TxD2 with DMA-based or interrupt-based operation

— UART Ch 0, 1, 2 with IrDA 1.0 & 16-byte FIFO

— UART Ch 0, 1 with nRTS0, nCTS0, nRTS1, nCTS1

— Supports handshake transmit / receive

BLOCK DIAGRAM

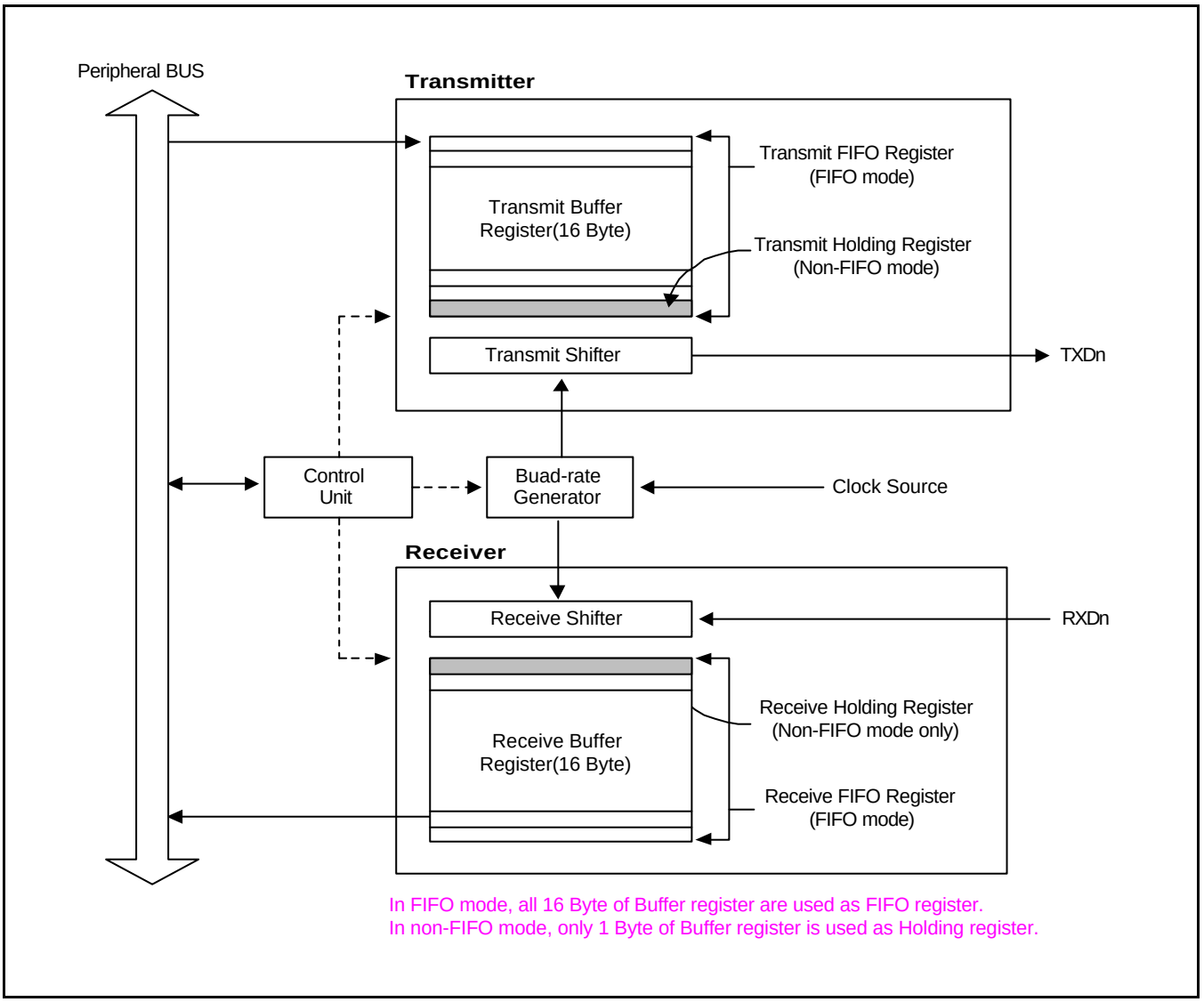


Figure 11-1. UART Block Diagram (with FIFO)

UART OPERATION

The following sections describe the UART operations that include data transmission, data reception, interrupt generation, baud-rate generation, loopback mode, infra-red mode, and auto flow control.

Data Transmission

The data frame for transmission is programmable. It consists of a start bit, 5 to 8 data bits, an optional parity bit and 1 to 2 stop bits, which can be specified by the line control register (ULCONn). The transmitter can also produce the break condition. The break condition forces the serial output to logic 0 state for one frame transmission time. This block transmits break signal after the present transmission word transmits perfectly. After the break signal transmission, it continously transmits data into the Tx FIFO (Tx holding register in the case of Non-FIFO mode).

Data Reception

Like the transmission, the data frame for reception is also programmable. It consists of a start bit, 5 to 8 data bits, an optional parity bit and 1 to 2 stop bits in the line control register (ULCONn). The receiver can detect overrun error, parity error, frame error and break condition, each of which can set an error flag.

— The overrun error indicates that new data has overwritten the old data before the old data has been read.

— The parity error indicates that the receiver has detected an unexpected parity condition.

— The frame error indicates that the received data does not have a valid stop bit.

— The break condition indicates that the RxDn input is held in the logic 0 state for a duration longer than one frame transmission time.

Receive time-out condition occurs when it does not receive data during the 3 word time(This interval follows the setting of Word Length bit) and the Rx FIFO is not empty in the FIFO mode.

Auto Flow Control(AFC)

S3C2410X01's UART 0 and UART 1 support auto flow control with nRTS and nCTS signals, in case, it would have to connect UART to UART. If users connect UART to a Modem, disable auto flow control bit in UMCONn register and control the signal of nRTS by software.

In AFC, nRTS is controlled by condition of the receiver and operation of transmitter is controlled by the nCTS signal. The UART's transmitter transfers the data in FIFO only when nCTS signal active(In AFC, nCTS means that the other UART's FIFO is ready to receive data). Before the UART receives data, nRTS has to be activated when its receive FIFO has a spare more than 2-byte and has to be inactivated when its receive FIFO has a spare under 1-byte(In AFC, nRTS means that its own receive FIFO is ready to receive data).

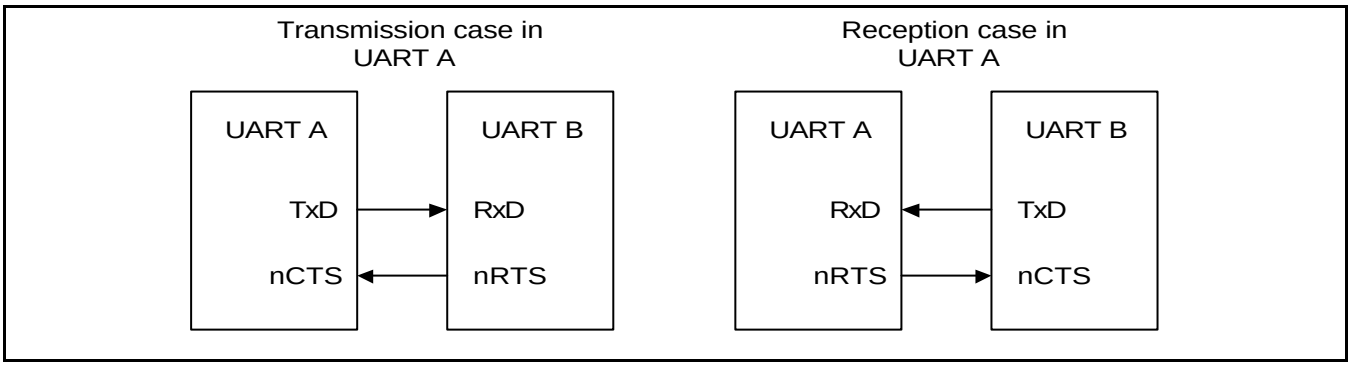


Figure 11-2. UART AFC interface

NOTE : UART 2 does not support AFC function, because S3C2410X01 has no nRTS2 and nCTS2.

Non Auto-Flow control (Controlling nRTS and nCTS by S/W) Example

Rx operation with FIFO

1. Select receive mode(Interrupt or DMA mode)
2. Check the value of Rx FIFO count in UFSTATn register. If the value is less than 15, users have to set the value of UMCONn[0] to '1'(activate nRTS), and if it is equal or larger than 15 users have to set the value to '0'(inactivate nRTS).
3. Repeat item 2.

Tx operation with FIFO

1. Select transmit mode (Interrupt or DMA mode)
2. Check the value of UMSTATn[0]. If the value is '1'(nCTS is activated), users write the data to Tx FIFO register.

RS-232C interface

If users connect to modem interface (not equal null modem), nRTS, nCTS, nDSR, nDTR, DCD and nRI signals are need. In this case, users control these signals with general I/O ports by S/W because the AFC does not support the RS-232C interface.

Interrupt/DMA Request Generation

Each UART of S3C2410X01 has seven status(Tx/Rx/Error) signals: Overrun error, Parity error, Frame error, Break, Receive buffer data ready, Transmit buffer empty, and Transmit shifter empty, all of which are indicated by the corresponding UART status register (UTRSTATn/UERSTATn).

The overrun error, parity error, frame error and break condition are referred to as the receive error status, each of which can cause the receive error status interrupt request, if the receive-error-status-interrupt-enable bit is set to one in the control register, UCONn. When a receive-error-status-interrupt-request is detected, the signal causing the request can be identified by reading the value of UERSTSTn.

When the receiver transfers the data of the receive shifter to the receive FIFO register in FIFO mode and the number of received data reaches Rx FIFO Trigger Level, Rx interrupt is generated, if Receive mode in control register(UCONn) is selected as 1(Interrupt request or polling mode).
In the Non-FIFO mode, transfering the data of the receive shifter to the receive holding register will cause Rx interrupt under the Interrupt request and polling mode.

When the transmitter transfers data from its transmit FIFO register to its transmit shifter and the number of data left in transmit FIFO reaches Tx FIFO Trigger Level, Tx interrupt is generated, if Transmit mode in control register is selected as Interrupt request or polling mode.
In the Non-FIFO mode, transfering data from the transmit holding register to the transmit shifter will cause Tx interrupt under the Interrupt request and polling mode.

If the Receive mode and Transmit mode in control register are selected as the DMAn request mode then DMAn request is occurred instead of Rx or Tx interrupt in the situation mentioned above.

Table 11-1. Interrupts in Connection with FIFO

Type	FIFO Mode	Non-FIFO Mode
Rx interrupt	Each time receive data reaches the trigger level of receive FIFO, the Rx interrupt will be generated. When the number of data in FIFO does not reaches Rx FIFO trigger Level and does not receive data during 3 word time(This interval follows the setting of Word Length bit), the Rx interrupt will be generated(receive time out).	Each time receive data becomes full, the receive holding register generates an interrupt.
Tx interrupt	Each time transmit data reaches the trigger level of transmit FIFO(Tx FIFO trigger Level), the Tx interrupt will be generated.	Each time transmit data become empty, the transmit holding register generates an interrupt.
Error interrupt	When frame error, parity error, and break signal are detected, these errors will generate an error interrupt. When it gets to the top of the receive FIFO without reading out data in it, the error interrupt will be generated(overrun error).	All errors generate an error interrupt immediately. However if another error occurs at the same time, only one interrupt is generated.

UART Error Status FIFO

UART has the error status FIFO besides the Rx FIFO register. The error status FIFO indicates which data, among FIFO registers, is received with an error. The error interrupt will be issued only when the data, which has an error, is ready to read out. To clear the error status FIFO, the URXHn with an error and UERSTATn must be read out.

For example,

It is assumed that the UART Rx FIFO receives A, B, C, D, E characters sequentially and the frame error occurrs while receiving 'B', and the parity error occurs while receiving 'D'.

Although the actual UART receive error occurred, the error interrupt will not be generated because the character, which was received with an error, has not been read yet. The error interrupt will occur when the character is read out.

Time	Sequence flow	Error interrupt	Note
#0	When no character is read out	-	
#1	A,B,C,D,E is received	-	
#2	After A is read out	The frame error(in B) interrupt occurs	The 'B' has to be read out
#3	After B is read out	-	
#4	After C is read out	The parity error(in D) interrupt occurs	The 'D' has to be read out
#5	After D is read out	-	
#6	After E is read out	-	

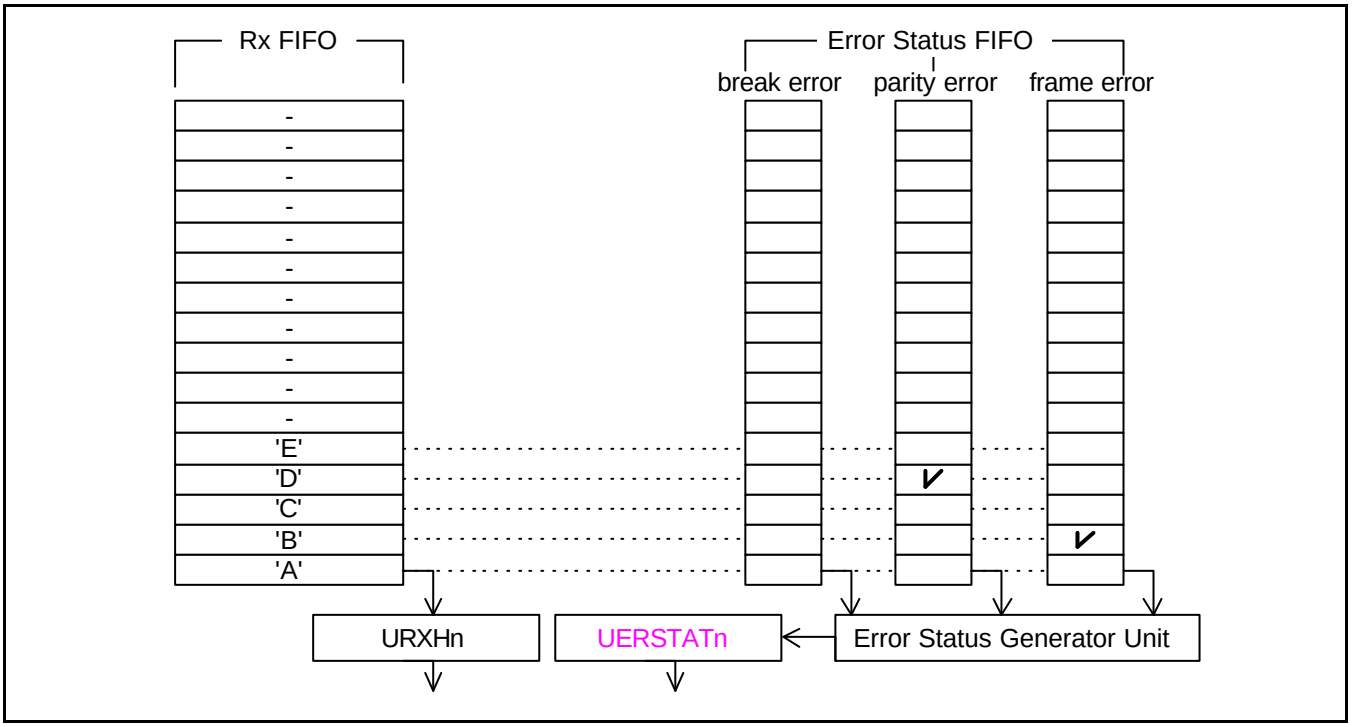


Figure 11-3. Example showing UART Receiving 5 Characters with 2 Errors

Baud-Rate Generation

Each UART's baud-rate generator provides the serial clock for transmitter and receiver. The source clock for the baud-rate generator can be selected with the S3C2410X01's internal system clock or UCLK. In other words, dividend can be selected by the setting of Clock Selection of UCONn. The baud-rate clock is generated by dividing the source clock(PCLK or UCLK) by 16 and a 16-bit divisor specified in the UART baud-rate divisor register (UBRDIVn). The UBRDIVn can be determined as follows:

UBRDIVn = (int)(PCLK/(bps *x 16)) -1*

where the divisor should be from 1 to (2^{16}-1).

For the accurate UART operation, S3C2410X01 also supports UCLK as a dividend.
If UCLK, supplied by external UART device or system, is used, then serial clock of UART is exactly synchronized with UCLK. So, user can get the more precision UART operation. The UBRDIVn can be determined as follows:

UBRDIVn = (int)(UCLK / (bps x 16)) –1

where the divisor should be from 1 to (2^{16}-1) and UCLK should be smaller than PCLK.

For example, if the baud-rate is 115200 bps and PCLK or UCLK is 40 MHz , UBRDIVn is:

UBRDIVn = (int)(40000000/(115200 x 16)) -1
= (int)(21.7) -1
= 21 -1 = 20

Loop-back Mode

The S3C2410X01 UART provides a test mode referred to as the loopback mode, to aid in isolating faults in the communication link. In this mode, the transmitted data is immediately received. This feature allows the processor to verify the internal transmit and to receive the data path of each SIO channel. This mode can be selected by setting the loopback-bit in the UART control register (UCONn).

Break Condition

The break is defined as a continuous low level signal for one frame transmission time on the transmit data output.

IR (Infra-Red) Mode

The S3C2410X01 UART block supports infra-red (IR) transmission and reception, which can be selected by setting the infra-red-mode bit in the UART line control register (ULCONn). The implementation of the mode is shown in Figure 11-3.

In IR transmit mode, the transmit period is pulsed at a rate of 3/16, the normal serial transmit rate (when the transmit data bit is zero); In IR receive mode, the receiver must detect the 3/16 pulsed period to recognize a zero value (refer to the frame timing diagrams shown in Figure 11-5 and 11-6).

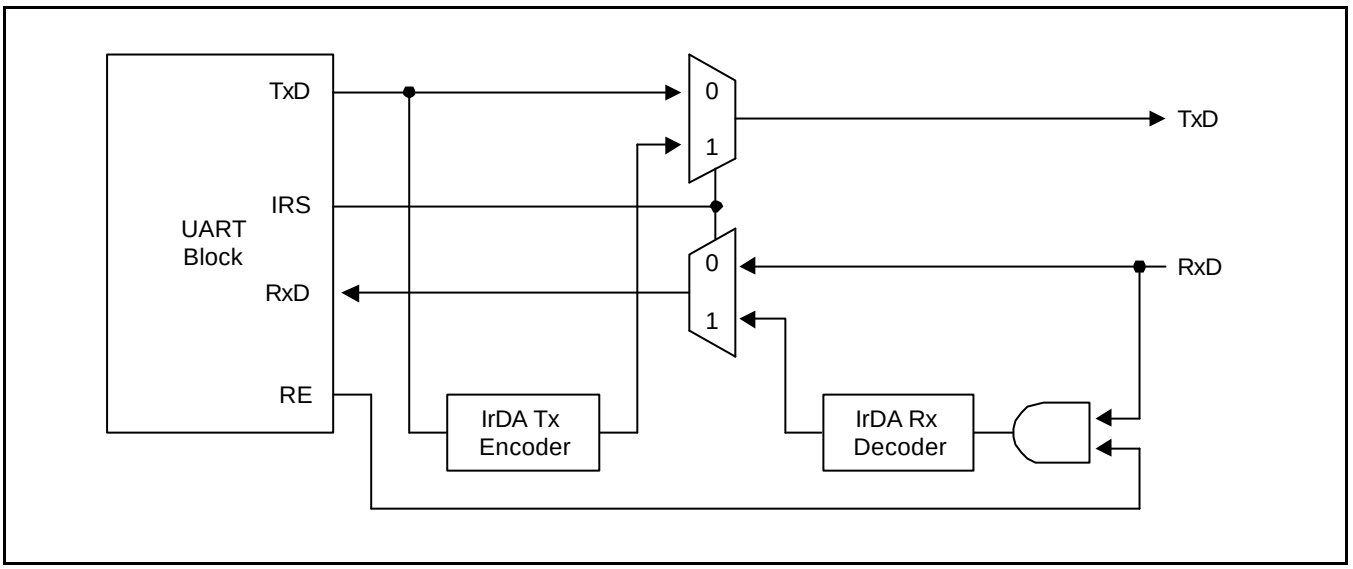


Figure 11-3. IrDA Function Block Diagram

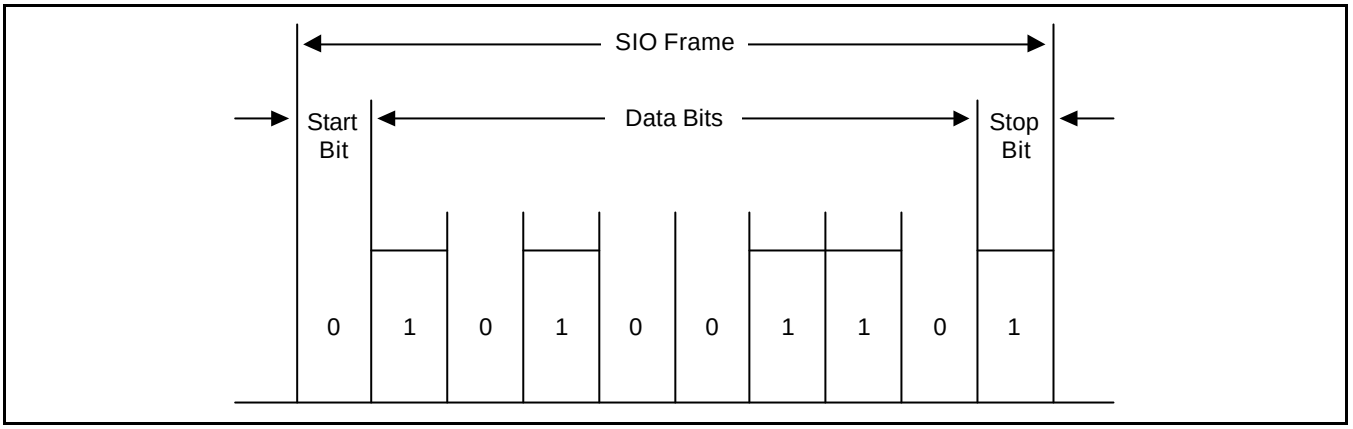


Figure 11-4. Serial I/O Frame Timing Diagram (Normal UART)

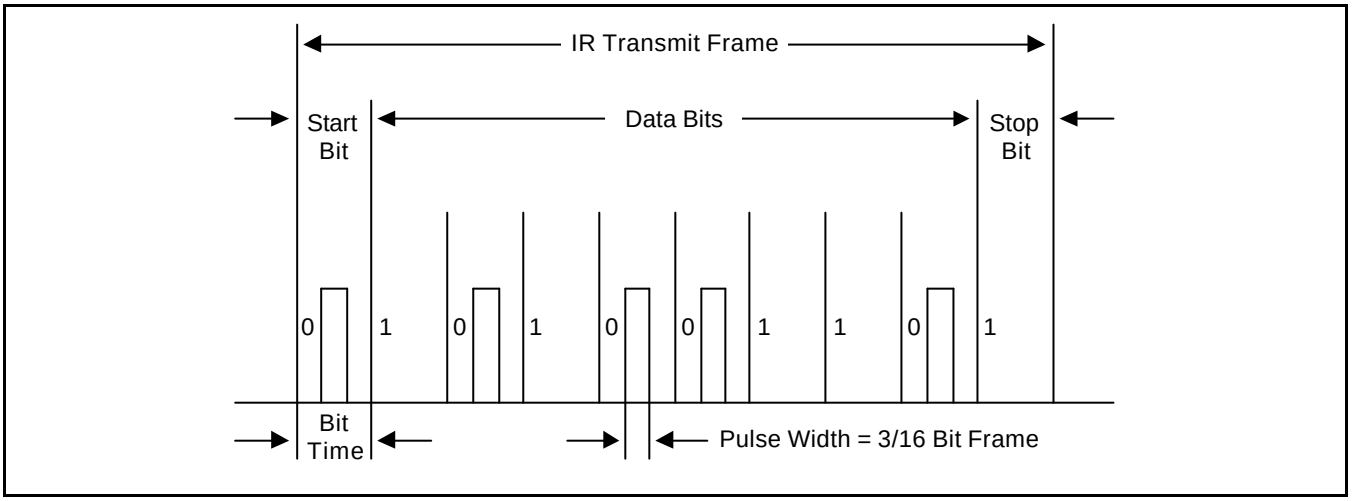


Figure 11-5. Infra-Red Transmit Mode Frame Timing Diagram

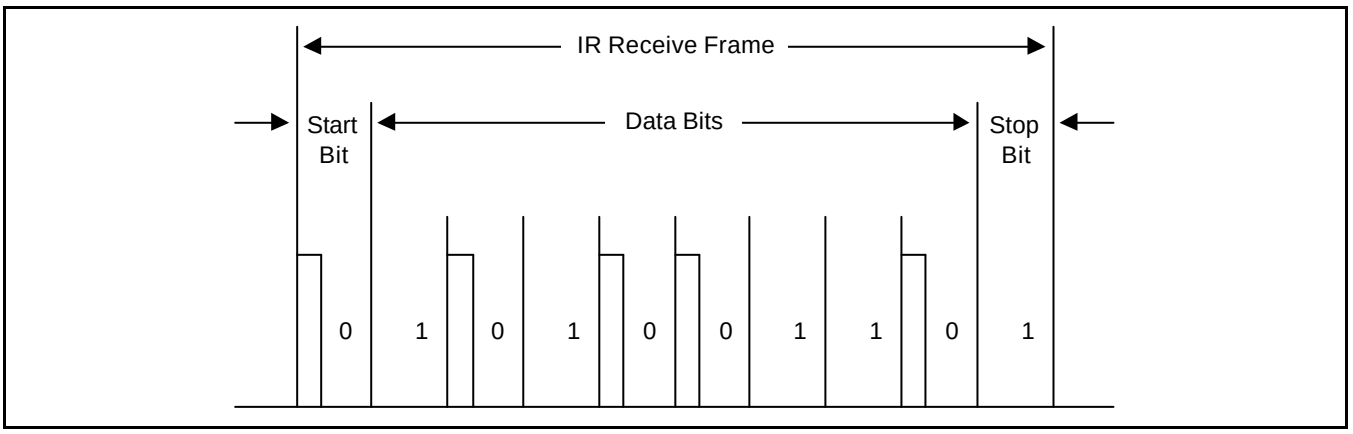


Figure 11-6. Infra-Red Receive Mode Frame Timing Diagram

UART SPECIAL REGISTERS

UART LINE CONTROL REGISTER

There are three UART line control registers, ULCON0, ULCON1, and ULCON2, in the UART block.

Register	Address	R/W	Description	Reset Value
ULCON0	0x50000000	R/W	UART channel 0 line control register	0x00
ULCON1	0x50004000	R/W	UART channel 1 line control register	0x00
ULCON2	0x50008000	R/W	UART channel 2 line control register	0x00

ULCONn	Bit	Description	Initial State
Reserved	[7]		0
Infra-Red Mode	[6]	The Infra-Red mode determines whether or not to use the Infra-Red mode. 0 = Normal mode operation 1 = Infra-Red Tx/Rx mode	0
Parity Mode	[5:3]	The parity mode specifies how parity generation and checking are to be performed during UART transmit and receive operation. 0xx = No parity 100 = Odd parity 101 = Even parity 110 = Parity forced/checked as 1 111 = Parity forced/checked as 0	000
Number of stop bit	[2]	The number of stop bits specifies how many stop bits are to be used to signal end-of-frame. 0 = One stop bit per frame 1 = Two stop bit per frame	0
Word length	[1:0]	The word length indicates the number of data bits to be transmitted or received per frame. 00 = 5-bits 01 = 6-bits 10 = 7-bits 11 = 8-bits	00

UART CONTROL REGISTER

There are three UART control registers, UCON0, UCON1 and UCON2, in the UART block.

Register	Address	R/W	Description	Reset Value
UCON0	0x50000004	R/W	UART channel 0 control register	0x00
UCON1	0x50004004	R/W	UART channel 1 control register	0x00
UCON2	0x50008004	R/W	UART channel 2 control register	0x00

UCONn	Bit	Description	Initial State
Clock selection	[10]	Select PCLK or UCLK for the UART baud rate. 0=PCLK : UBRDIVn = (int)(PCLK / (bps x 16)) -1 1=UCLK : UBRDIVn = (int)(UCLK / (bps x 16)) -1	0
Tx interrupt type	[9]	Interrupt request type 0 = Pulse (Interrupt is requested as soon as the Tx buffer becomes empty in Non-FIFO mode or reaches Tx FIFO Trigger Level in FIFO mode) 1 = Level (Interrupt is requested while Tx buffer is empty in Non-FIFO mode or reaches Tx FIFO Trigger Level in FIFO mode)	0
Rx interrupt type	[8]	Interrupt request type 0 = Pulse (Interrupt is requested the instant Rx buffer receives the data in Non-FIFO mode or reaches Rx FIFO Trigger Level in FIFO mode) 1 = Level (Interrupt is requested while Rx buffer is receiving data in Non-FIFO mode or reaches Rx FIFO Trigger Level in FIFO mode)	0
Rx time out enable	[7]	Enable/Disable Rx time out interrupt when UART FIFO is enabled. The interrupt is a receive interrupt. 0 = Disable 1 = Enable	0
Rx error status interrupt enable	[6]	This bit enables the UART to generate an interrupt if an exception, such as a break, frame error, parity error, or overrun error occurs during a receive operation. 0 = Do not generate receive error status interrupt 1 = Generate receive error status interrupt	0
Loop-back Mode	[5]	Setting loop-back bit to 1 causes the UART to enter the loop-back mode. This mode is provided for test purposes only. 0 = Normal operation 1 = Loop-back mode	0
Send Break Signal	[4]	Setting this bit causes the UART to send a break during 1 frame time. This bit is auto-cleared after sending the break signal. 0 = Normal transmit 1 = Send break signal	0

UART CONTROL REGISTER (CONTINUED)

Transmit Mode	[3:2]	These two bits determine which function is currently able to write Tx data to the UART transmit buffer register. 00 = Disable 01 = Interrupt request or polling mode 10 = DMA0 request (Only for UART0), DMA3 request (Only for UART2) 11 = DMA1 request (Only for UART1)	00
Receive Mode	[1:0]	These two bits determine which function is currently able to read data from UART receive buffer register. 00 = Disable 01 = Interrupt request or polling mode 10 = DMA0 request (Only for UART0), DMA3 request (Only for UART2) 11 = DMA1 request (Only for UART1)	00

Note : When the UART does not reach the FIFO trigger level and does not receive data during 3 word time in DMA receive mode with FIFO, the Rx interrupt will be generated (receive time out), and the users should check the FIFO status and read out the rest.

UART FIFO CONTROL REGISTER

There are three UART FIFO control registers, UFCON0, UFCON1 and UFCON2, in the UART block.

Register	Address	R/W	Description	Reset Value
UFCON0	0x50000008	R/W	UART channel 0 FIFO control register	0x0
UFCON1	0x50004008	R/W	UART channel 1 FIFO control register	0x0
UFCON2	0x50008008	R/W	UART channel 2 FIFO control register	0x0

UFCONn	Bit	Description	Initial State
Tx FIFO Trigger Level	[7:6]	These two bits determine the trigger level of transmit FIFO. 00 = Empty 01 = 4-byte 10 = 8-byte 11 = 12-byte	00
Rx FIFO Trigger Level	[5:4]	These two bits determine the trigger level of receive FIFO. 00 = 4-byte 01 = 8-byte 10 = 12-byte 11 = 16-byte	00
Reserved	[3]		0
Tx FIFO Reset	[2]	This bit is auto-cleared after resetting FIFO 0 = Normal 1= Tx FIFO reset	0
Rx FIFO Reset	[1]	This bit is auto-cleared after resetting FIFO 0 = Normal 1= Rx FIFO reset	0
FIFO Enable	[0]	0 = FIFO disable 1 = FIFO mode	0

Note : When the UART does not reach the FIFO trigger level and does not receive data during 3 word time in DMA receive mode with FIFO, the Rx interrupt will be generated(receive time out), and the users should check the FIFO status and read out the rest.

UART MODEM CONTROL REGISTER

There are two UART MODEM control registers, UMCON0 and UMCON1, in the UART block.

Register	Address	R/W	Description	Reset Value
UMCON0	0x5000000C	R/W	UART channel 0 Modem control register	0x0
UMCON1	0x5000400C	R/W	UART channel 1 Modem control register	0x0
Reserved	0x5000800C	-	Reserved	Undef

UMCONn	Bit	Description	Initial State
Reserved	[7:5]	These bits must be 0's	00
AFC(Auto Flow Control)	[4]	0 = Disable 1 = Enable	0
Reserved	[3:1]	These bits must be 0's	00
Request to Send	[0]	If AFC bit is enabled, this value will be ignored. In this case the S3C2410X01 will control nRTS automatically. If AFC bit is disabled, nRTS must be controlled by S/W. 0 = 'H' level(Inactivate nRTS) 1 = 'L' level(Activate nRTS)	0

NOTE : UART 2 does not support AFC function, because S3C2410X01 has no nRTS2 and nCTS2.

UART TX/RX STATUS REGISTER

There are three UART Tx/Rx status registers, UTRSTAT0, UTRSTAT1 and UTRSTAT2, in the UART block.

Register	Address	R/W	Description	Reset Value
UTRSTAT0	0x50000010	R	UART channel 0 Tx/Rx status register	0x6
UTRSTAT1	0x50004010	R	UART channel 1 Tx/Rx status register	0x6
UTRSTAT2	0x50008010	R	UART channel 2 Tx/Rx status register	0x6

UTRSTATn	Bit	Description	Initial State
Transmitter empty	[2]	This bit is automatically set to 1 when the transmit buffer register has no valid data to transmit and the transmit shift register is empty. 0 = Not empty 1 = Transmitter(transmit buffer & shifter register) empty	1
Transmit buffer empty	[1]	This bit is automatically set to 1 when transmit buffer register is empty. 0 =The buffer register is not empty 1 = Empty (In Non-FIFO mode, Interrupt or DMA is requested. In FIFO mode, Interrupt or DMA is requested, when Tx FIFO Trigger Level is set to 00(Empty)) If the UART uses the FIFO, users should check Tx FIFO Count bits and Tx FIFO Full bit in the UFSTAT register instead of this bit.	1
Receive buffer data ready	[0]	This bit is automatically set to 1 whenever receive buffer register contains valid data, received over the RXDn port. 0 = Empty 1 = The buffer register has a received data (In Non-FIFO mode, Interrupt or DMA is requested) If the UART uses the FIFO, users should check Rx FIFO Count bits and Rx FIFO Full bit in the UFSTAT register instead of this bit.	0

UART ERROR STATUS REGISTER

There are three UART Rx error status registers, UERSTAT0, UERSTAT1 and UERSTAT2, in the UART block.

Register	Address	R/W	Description	Reset Value
UERSTAT0	0x50000014	R	UART channel 0 Rx error status register	0x0
UERSTAT1	0x50004014	R	UART channel 1 Rx error status register	0x0
UERSTAT2	0x50008014	R	UART channel 2 Rx error status register	0x0

UERSTATn	Bit	Description	Initial State
Break Detect	[3]	This bit is automatically set to 1 to indicate that a break signal has been received. 0 = No break receive 1 = Break receive(Interrupt is requested)	0
Frame Error	[2]	This bit is automatically set to 1 whenever a frame error occurs during receive operation. 0 = No frame error during receive 1 = Frame error(Interrupt is requested)	0
Parity Error	[1]	This bit is automatically set to 1 whenever a parity error occurs during receive operation. 0 = No parity error during receive 1 = Parity error(Interrupt is requested)	0
Overrun Error	[0]	This bit is automatically set to 1 whenever an overrun error occurs during receive operation. 0 = No overrun error during receive 1 = Overrun error(Interrupt is requested)	0

NOTE : These bits (UERSATn[3:0]) are automatically cleared to 0 when the UART error status register is read.

UART FIFO STATUS REGISTER

There are three UART FIFO status registers, UFSTAT0, UFSTAT1 and UFSTAT2, in the UART block.

Register	Address	R/W	Description	Reset Value
UFSTAT0	0x50000018	R	UART channel 0 FIFO status register	0x00
UFSTAT1	0x50004018	R	UART channel 1 FIFO status register	0x00
UFSTAT2	0x50008018	R	UART channel 2 FIFO status register	0x00

UFSTATn	Bit	Description	Initial State
Reserved	[15:10]		0
Tx FIFO Full	[9]	This bit is automatically set to 1 whenever transmit FIFO is full during transmit operation 0 = 0-byte ≤ Tx FIFO data ≤ 15-byte 1 = Full	0
Rx FIFO Full	[8]	This bit is automatically set to 1 whenever receive FIFO is full during receive operation 0 = 0-byte ≤ Rx FIFO data ≤ 15-byte 1 = Full	0
Tx FIFO Count	[7:4]	Number of data in Tx FIFO	0
Rx FIFO Count	[3:0]	Number of data in Rx FIFO	0

UART MODEM STATUS REGISTER

There are two UART modem status registers, UMSTAT0, UMSTAT1 and UMSTAT2, in the UART block.

Register	Address	R/W	Description	Reset Value
UMSTAT0	0x5000001C	R	UART channel 0 Modem status register	0x0
UMSTAT1	0x5000401C	R	UART channel 1 Modem status register	0x0
Reserved	0x5000801C	-	Reserved	Undef

UMSTAT0	Bit	Description	Initial State
Reserved	[3]		0
Delta CTS	[2]	This bit indicates that the nCTS input to S3C2410X01 has changed state since the last time it was read by CPU. (Refer to Figure 11-7) 0 = Has not changed 1 = Has changed	0
Reserved	[1]		0
Clear to Send	[0]	0 = CTS signal is not activated(nCTS pin is high) 1 = CTS signal is activated(nCTS pin is low)	0

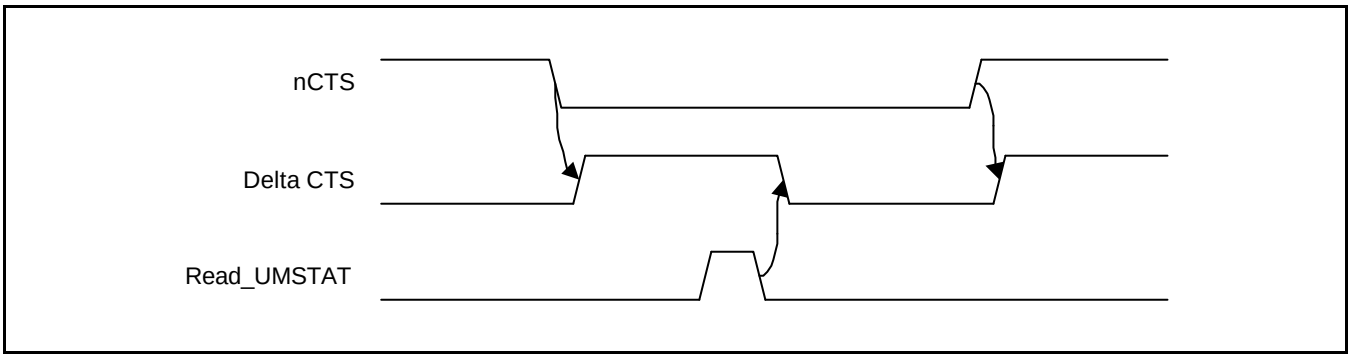


Figure 11-7. nCTS and Delta CTS Timing Diagram

UART TRANSMIT BUFFER REGISTER(HOLDING REGISTER & FIFO REGISTER)

There are three UART transmit buffer registers, UTXH0, UTXH1 and UTXH2, in the UART block.
UTXHn has an 8-bit data for transmission data.

Register	Address	R/W	Description	Reset Value
UTXH0	0x50000020(L) 0x50000023(B)	W (by byte)	UART channel 0 transmit buffer register	-
UTXH1	0x50004020(L) 0x50004023(B)	W (by byte)	UART channel 1 transmit buffer register	-
UTXH2	0x50008020(L) 0x50008023(B)	W (by byte)	UART channel 2 transmit buffer register	-

UTXHn	Bit	Description	Initial State
TXDATAn	[7:0]	Transmit data for UARTn	-

NOTE:

(L): When the endian mode is Little endian.
(B): When the endian mode is Big endian.

UART RECEIVE BUFFER REGISTER (HOLDING REGISTER & FIFO REGISTER)

There are three UART receive buffer registers, URXH0, URXH1 and URXH2, in the UART block.
URXHn has an 8-bit data for received data.

Register	Address	R/W	Description	Reset Value
URXH0	0x50000024(L) 0x50000027(B)	R (by byte)	UART channel 0 receive buffer register	-
URXH1	0x50004024(L) 0x50004027(B)	R (by byte)	UART channel 1 receive buffer register	-
URXH2	0x50008024(L) 0x50008027(B)	R (by byte)	UART channel 2 receive buffer register	-

URXHn	Bit	Description	Initial State
RXDATAn	[7:0]	Receive data for UARTn	-

NOTE:

When an overrun error occurs, the URXHn must be read. If not, the next received data will also make an overrun error, even though the overrun bit of UERSTATn had been cleared.

UART BAUD RATE DIVISOR REGISTER

There are three UART baud rate divisor registers, UBRDIV0, UBRDIV1 and UBRDIV2, in the UART block.
The value stored in the baud rate divisor register (UBRDIVn), is used to determine the serial Tx/Rx clock rate (baud rate) as follows:

UBRDIVn = (int)(PCLK / (bps x 16)) –1

or

UBRDIVn = (int)(UCLK / (bps x 16)) –1

where the divisor should be from 1 to (2^{16}-1) and UCLK should be smaller than PCLK.

For example, if the baud-rate is 115200 bps and PCLK or UCLK is 40 MHz , UBRDIVn is:

UBRDIVn = (int)(40000000 / (115200 x 16)) -1
= (int)(21.7) -1
= 21 -1 = 20

Register	Address	R/W	Description	Reset Value
UBRDIV0	0x50000028	R/W	Baud rate divisior register 0	-
UBRDIV1	0x50004028	R/W	Baud rate divisior register 1	-
UBRDIV2	0x50008028	R/W	Baud rate divisior register 2	-

UBRDIV n	Bit	Description	Initial State
UBRDIV	[15:0]	Baud rate division value UBRDIVn >0	-

12 USB HOST CONTROLLER

OVERVIEW

S3C2410 supports 2 port USB host interface as follows;

- OHCI Rev 1.0 compatible.
- USB Rev1.1 compatible
- 2 down stream ports.
- Support for both LowSpeed and HighSpeed USB devices

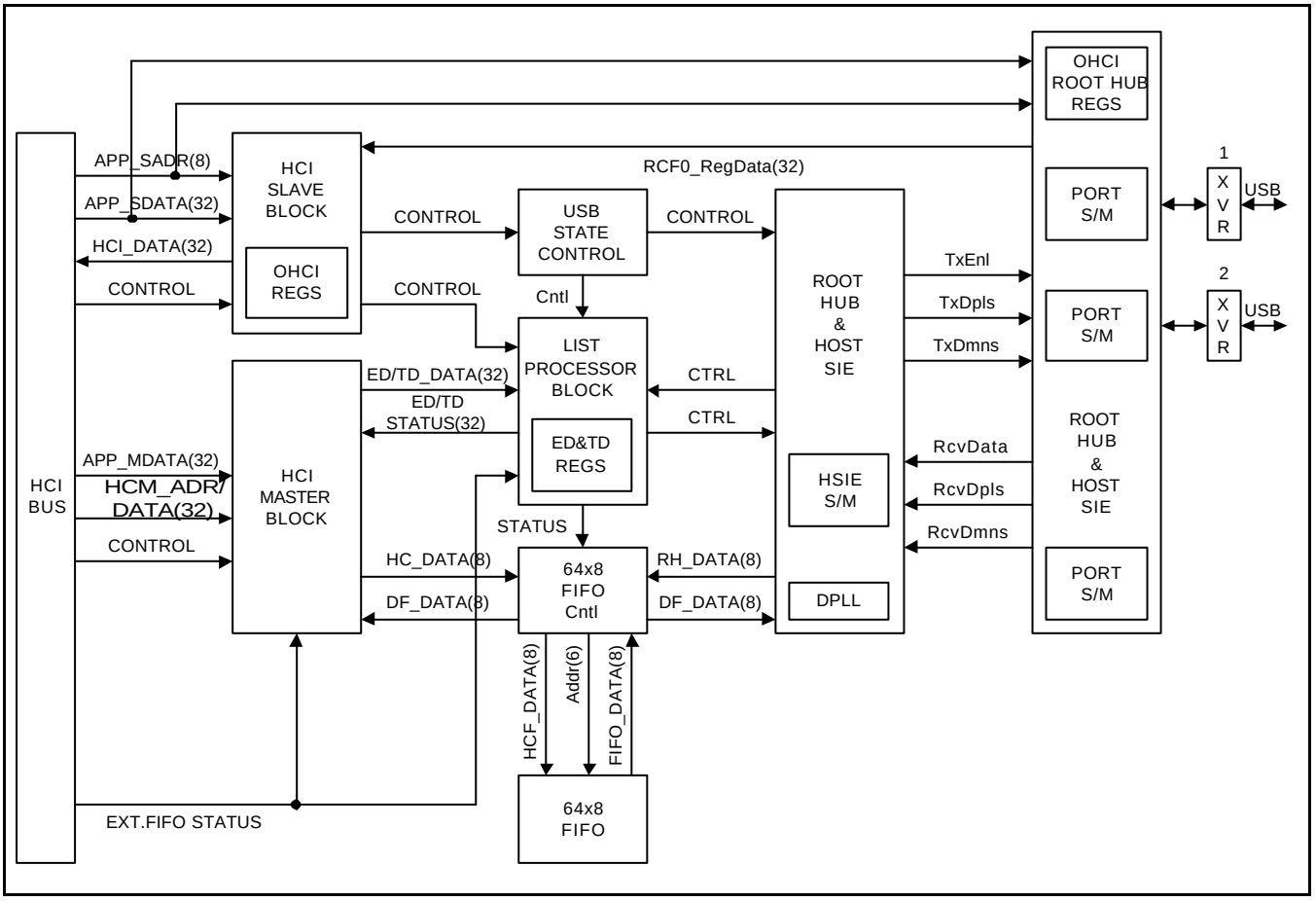


Figure 12-1. USB Host Controller Block Diagram

USB HOST CONTROLLER SPECIAL REGISTERS

The S3C2410 USB Host controller complies with OHCI Rev 1.0. Please refer to Open Host Controller Interface Rev 1.0 specification for detail information.

OHCI REGISTERS FOR USB HOST CONTROLLER

Register	Base Address	R/W	Description	Reset Value
HcRevision	0x14200000	–	Control and status group	–
HcControl	0x14200004	–		–
HcCommonStatus	0x14200008	–		–
HcInterruptStatus	0x1420000c	–		–
HcInterruptEnable	0x14200010	–		–
HcInterruptDisable	0x14200014	–		–
HcHCCA	0x14200018	–	Memory pointer group	–
HcPeriodCuttentED	0x1420001c	–		–
HcControlHeadED	0x14200020	–		–
HcControlCurrentED	0x14200024	–		–
HcBulkHeadED	0x14200028	–		–
HcBulkCurrentED	0x1420002c	–		–
HcDoneHead	0x14200030	–		–
HcRmInterval	0x14200034	–	Frame counter group	–
HcFmRemaining	0x14200038	–		–
HcFmNumber	0x1420003c	–		–
HcPeriodicStart	0x14200040	–		–
HcLSThreshold	0x14200044	–		–
HcRhDescriptorA	0x14200048	–	Root hub group	–
HcRhDescriptorB	0x1420004c	–		–
HcRhStatus	0x14200050	–		–
HcRhPortStatus1	0x14200054	–		–
HcRhPortStatus2	0x14200058	–		–

13 USB DEVICE

OVERVIEW

USB device controller is designed to provide a high performance full speed function controller solution with DMA I/F. USB device controller allows bulk transfer with DMA, interrupt transfer and control transfer.

The functions are as follows:

- Full speed USB device controller compatible with the USB specification version 1.1
- DMA interface for bulk transfer
- 5 endpoints with FIFO
  EP0: 16byte (Register)
  EP1: 64byte IN/OUT FIFO (dual port asynchronous RAM): interrupt or DMA
  EP2: 64byte IN/OUT FIFO (dual port asynchronous RAM): interrupt or DMA
  EP3: 64byte IN/OUT FIFO (dual port asynchronous RAM): interrupt or DMA
  EP4: 64byte IN/OUT FIFO (dual port asynchronous RAM): interrupt or DMA
- Integrated USB Transceiver

FEATURE

— Fully compliant with USB Specification Version 1.1

— Full speed (12Mbps) device

— Integrated USB Transceiver

— Supports control, interrupt and bulk transfer

— 5 endpoints with FIFO:
  One bi-directional control Endpoint with 16-byte FIFO (EP0)
  Four bi-directional bulk endpoint with 64-byte FIFO (EP1, EP2, EP3, EP4)

— Supports DMA interface for receive and transmit bulk endpoints. (EP1, EP2, EP3, EP4)

— Independent 64byte receive and transmit FIFO to maximize throughput

— Supports suspend and remote wake-up function

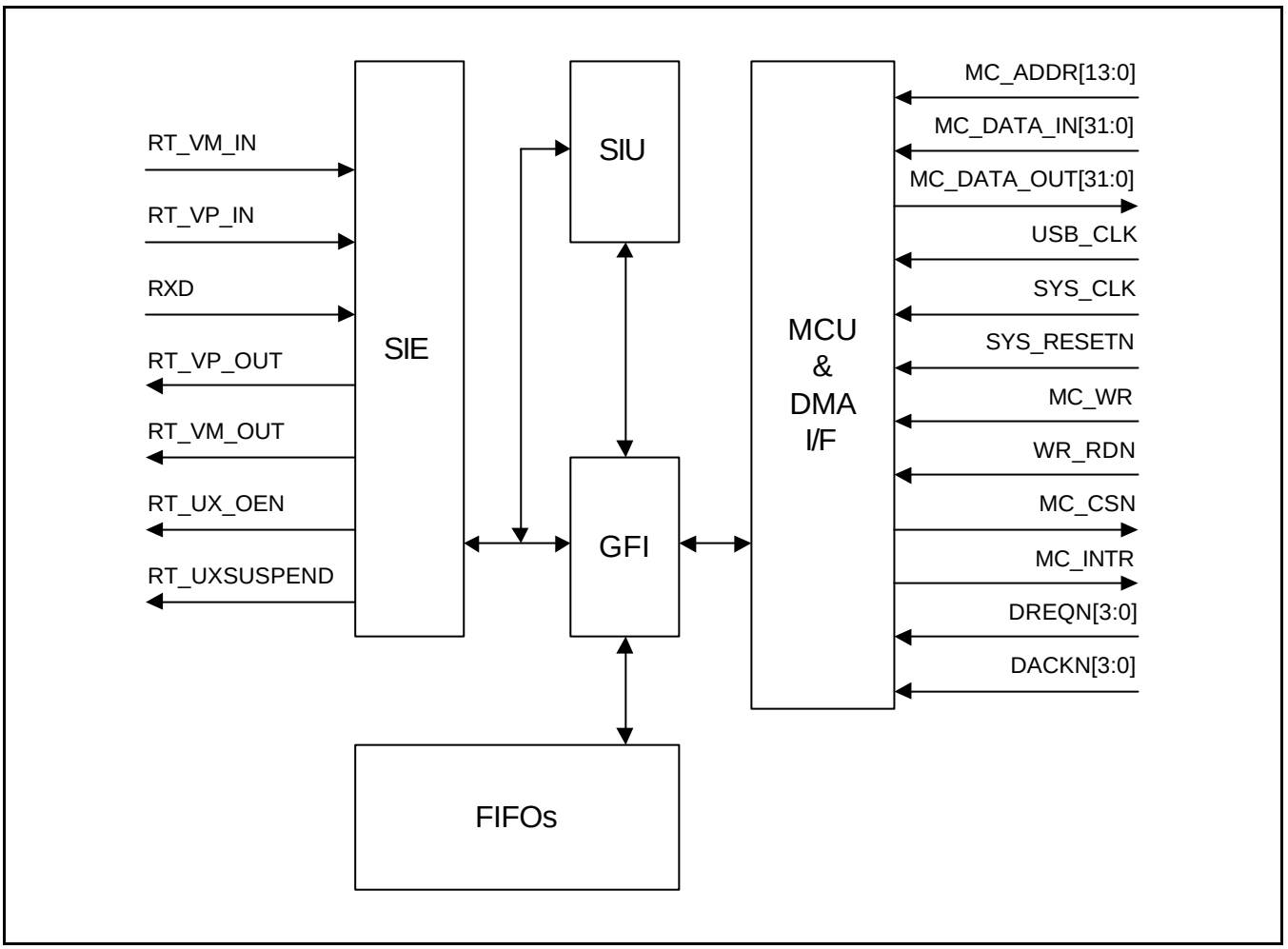


Figure 13-1. USB Device Block Diagram

USB DEVICE SPECIAL REGISTERS

This section describes the detail functionality about register set USB Device..
All special function register is byte access or word access. If you access byte mode offset-address is different in little endian and big endian. All reserved bit is zero.
Common indexed registers depend on INDEX_REG(offset address : 0X178) value. For example if you want to write EP0 CSR register, you must write ' 0x00' on INDEX_REG before writing IN CSR1 register.
All Register must be resettled after Host Reset Signaling.

Register Name	Description	Offset Address
NON INDEXED REGISTERS		
FUNC_ADDR_REG	Function address register	0x140(L) / 0x143(B)
PWR_REG	Power management register	0x144(L) / 0x147(B)
EP_INT_REG (EP0–EP4)	Endpoint interrupt register	0x148(L) / 0x14B(B)
USB_INT_REG	USB interrupt register	0x158(L) / 0x15B(B)
EP_INT_EN_REG (EP0–EP4)	Endpoint interrupt enable register	0x15C(L) / 0x15F(B)
USB_INT_EN_REG	USB Interrupt enable register	0x16C(L) / 0x16F(B)
FRAME_NUM1_REG	Frame number 1 register	0x170(L) / 0x173(B)
FRAME_NUM2_REG	Frame number 2 register	0x174(L) / 0x177(B)
INDEX_REG	Index register	0x178(L) / 0x17B(B)
EP0_FIFO_REG	Endpoint0 FIFO register	0x1C0(L) / 0x1C3(B)
EP1_FIFO_REG	Endpoint1 FIFO register	0x1C4(L) / 0x1C7(B)
EP2_FIFO_REG	Endpoint2 FIFO register	0x1C8(L) / 0x1CB(B)
EP3_FIFO_REG	Endpoint3 FIFO register	0x1CC(L) / 0x1CF(B)
EP4_FIFO_REG	Endpoint4 FIFO register	0x1D0(L) / 0x1D3(B)
EP1_DMA_CON	Endpoint1 DMA control register	0x200(L) / 0x203(B)
EP1_DMA_UNIT	Endpoint1 DMA Unit counter register	0x204(L) / 0x207(B)
EP1_DMA_FIFO	Endpoint1 DMA FIFO counter register	0x208(L) / 0x20B(B)
EP1_DMA_TTC_L	Endpoint1 DMA Transfer counter low-byte register	0x20C(L) / 0x20F(B)
EP1_DMA_TTC_M	Endpoint1 DMA Transfer counter middle-byte register	0x210(L) / 0x213(B)
EP1_DMA_TTC_H	Endpoint1 DMA Transfer counter high-byte register	0x214(L) / 0x217(B)

EP2_DMA_CON	Endpoint2 DMA control register	0x218(L) / 0x21B(B)
EP2_DMA_UNIT	Endpoint2 DMA Unit counter register	0x21C(L) / 0x21F(B)
EP2_DMA_FIFO	Endpoint2 DMA FIFO counter register	0x220(L) / 0x223(B)
EP2_DMA_TTC_L	Endpoint2 DMA Transfer counter low-byte register	0x224(L) / 0x227(B)
EP2_DMA_TTC_M	Endpoint2 DMA Transfer counter middle-byte register	0x228(L) / 0x22B(B)
EP2_DMA_TTC_H	Endpoint2 DMA Transfer counter high-byte register	0x22C(L) / 0x22F(B)
EP3_DMA_CON	Endpoint3 DMA control register	0x240(L) / 0x243(B)
EP3_DMA_UNIT	Endpoint3 DMA Unit counter register	0x244(L) / 0x247(B)
EP3_DMA_FIFO	Endpoint3 DMA FIFO counter register	0x248(L) / 0x24B(B)
EP3_DMA_TTC_L	Endpoint3 DMA Transfer counter low-byte register	0x24C(L) / 0x24F(B)
EP3_DMA_TTC_M	Endpoint3 DMA Transfer counter middle-byte register	0x250(L) / 0x253(B)
EP3_DMA_TTC_H	Endpoint3 DMA Transfer counter high-byte register	0x254(L) / 0x247(B)
EP4_DMA_CON	Endpoint4 DMA control register	0x258(L) / 0x25B(B)
EP4_DMA_UNIT	Endpoint4 DMA Unit counter register	0x25C(L) / 0x25F(B)
EP4_DMA_FIFO	Endpoint4 DMA FIFO counter register	0x260(L) / 0x263(B)
EP4_DMA_TTC_L	Endpoint4 DMA Transfer counter low-byte register	0x264(L) / 0x267(B)
EP4_DMA_TTC_M	Endpoint4 DMA Transfer counter middle-byte register	0x268(L) / 0x26B(B)
EP4_DMA_TTC_H	Endpoint4 DMA Transfer counter high-byte register	0x26C(L) / 0x26F(B)
COMMON INDEXED REGISTERS		
MAXP_REG	Endpoint MAX Packet register	0x18C(L) / 0x18F(B)
IN INDEXED REGISTERS		
IN_CSR1_REG	EP In Control status register 1	0x184(L) / 0x187(B)
IN_CSR2_REG	EP In Control status register 2	0x188(L) / 0x18B(B)
OUT INDEXED REGISTERS		
OUT_CSR1_REG	EP Out Control status register 1	0x190(L) / 0x193(B)
OUT_CSR2_REG	EP Out Control status register 2	0x194(L) / 0x197(B)
OUT_FIFO_CNT1_REG	EP Out Write count register 1	0x198(L) / 0x19B(B)
OUT_FIFO_CNT2_REG	EP Out Write count register 2	0x19C(L) / 0x19F(B)

FUNC_ADDR_REG

This register maintains the USB Device Address assigned by the host. The MCU writes the value received through a SET_ADDRESS descriptor to this register. This address is used for the next token.

Register	Address	R/W	Description	Reset Value
FUNC_ADDR_REG	0x5200_0140(L) 0x5200_0143(B)	R/W (byte)	Function address register	0x00

FUNC_ADDR_REG	Bit	MCU	USB	Description	Initial State
ADDR_UPDATE	[7]	R/W	R /CLEAR	The MCU sets this bit whenever it updates the FUNCTION_ADDR field in this register. This bit will be cleared by USB when DATA_END bit in EP0_CSR register.	0
FUNCTION_ADDR	[6:0]	R/W	R	The MCU write the unique address, assigned by host, to this field.	00

POWER MANAGEMENT REGISTER (PWR_REG)

This register is power control register in USB block.

Register	Address	R/W	Description	Reset Value
PWR_REG	0x5200_0144(L) 0x5200_0147(B)	R/W (byte)	Power management register	0x00

FUNC_ADDR	Bit	MCU	USB	Description	Initial State
Reserved	[31:9]				0
ISO_UPDATE	[7]	R/W	R	Used for ISO mode only. If set, GFI waits for a SOF token to set IN_PKT_RDY even though a packet to send is already loaded by MCU. If an IN token is received before a SOF token, then a zero length data packet will be sent.	0
Reserved	[6:4]	-	-	-	-
USB_RESET	[3]	R	SET	The USB sets this bit if reset signaling is received from the host. This bit remains set as long as reset signaling persists on the bus	0
MCU_RESUME	[2]	R/W	R /CLEAR	The MCU sets this bit for MCU resume. The USB generates the resume signaling depending RESUME CON Register, while this bit is set in suspend mode.	
SUSPEND_MODE	[1]	R	SET /CLEAR	This bit can be set by USB, automatically when the device enter into suspend mode. It is cleared under the following conditions 1) The MCU clears the MCU_RESUME bit by writing ‘ 0’ , to end remote resume signaling. 2) The resume signal form host is received.	0
SUSPEND_EN	[0]	R/W	R	Suspend mode enable control bit 0 = Disable(default). The device will not enter suspend mode. 1 = Enable suspend mode	0

INTERRUPT REGISTER (EP_INT_REG, USB_INT_REG)

The USB core has two interrupt registers.
These registers act as status registers for the MCU when it is interrupted. The bits are cleared by writing a ' 1' (not ' 0') to each bit that was set.
Once the MCU is interrupted, MCU should read the contents of interrupt-related registers and write back to clear the contents if it is necessary.

Register	Address	R/W	Description	Reset Value
EP_INT_REG	0x5200_0148(L) 0x5200_014B(B)	R/W (byte)	EP Interrupt pending/clear register	0x00

EP_INT_REG	Bit	MCU	USB	Description	Initial State
EP1~EP4 Interrupt	[4:1]	R /CLEAR	SET	**For BULK/INTERRUPT IN endpoints:** The USB sets this bit under the following conditions: 1. IN_PKT_RDY bit is cleared. 2. FIFO is flushed 3. SENT_STALL set. **For BULK/INTERRUPT OUT endpoints:** USB sets this bit under the following conditions: 1. Sets OUT_PKT_RDY bit 2. Sets SENT_STALL bit **For ISO IN endpoints:** the USB sets this bit under the following conditions: 1. UNDER_RUN bit is set 2. IN_PKT_RDY bit is cleared. 3. FIFO is flushed Note: conditions 1 and 2 are mutually exclusive **For ISO OUT endpoints:** USB sets this bit under the following conditions: 1. OUT_PKT_RDY bit is set 2. OVER RUN bit is set. Note: Conditions 1 and 2 are mutually exclusive.	0
EP0 Interrupt	[0]	R /CLEAR	SET	This bit corresponds to endpoint 0 interrupt The USB sets this bit under the following conditions: 1. OUT_PKT_RDY bit is set. 2. IN_PKT_RDY bit is cleared. 3. SENT_STALL bit is set 4. SETUP_END bit is set 5. DATA_END bit is cleared(Indicates end of control transfer)	0

Register	Address	R/W	Description	Reset Value
USB_INT_REG	0x5200_0158(L) 0x5200_015B(B)	R/W (byte)	USB Interrupt pending/clear register	0x00

USB_INT_REG	Bit	MCU	USB	Description	Initial State
RESET Interrupt	[2]	R /CLEAR	SET	The USB set this bit, when it receives reset signaling.	0
RESUME Interrupt	[1]	R /CLEAR	SET	The USB sets this bit, when it receives resume signaling, *while in suspend mode.* If the resume is due to a USB reset, then the MCU is first interrupted with a RESUME interrupt. Once the clocks resume and the SE0 condition persists for 3ms, USB RESET interrupt will be asserted.	0
SUSPEND Interrupt	[0]	R /CLEAR	SET	The USB sets this bit when it receives suspend signalizing. This bit is set whenever there is no activity for 3ms on the bus. Thus, if the MCU does not stop the clock after the first suspend interrupt, it will be continue to be interrupted every 3ms as long as there is no activity on the USB bus. By default this interrupt is disabled.	0

INTERRUPT ENABLE REGISTER (EP_INT_EN_REG, USB_INT_REG)

Corresponding to each interrupt register, there is an INTERRUPT ENABLE register (except resume interrupt enable). By default usb reset interrupt is enabled.

If bit = 0, the interrupt is disabled
If bit = 1, the interrupt is enabled

Register	Address	R/W	Description	Reset Value
EP_INT_EN_REG	0x1500_015C(L) 0x1500_015F(B)	R/W (byte)	Determines which interrupt is enabled.	0xFF

INT_MASK_REG	Bit	MCU	USB	Description	Initial State
EP4_INT_EN	[4]	R/W	R	EP4 Interrupt Enable bit 0 = Interrupt disable 1 = Enable	1
EP3_INT_EN	[3]	R/W	R	EP3 Interrupt Enable bit 0 = Interrupt disable 1 = Enable	1
EP2_INT_EN	[2]	R/W	R	EP2 Interrupt Enable bit 0 = Interrupt disable 1 = Enable	1
EP1_INT_EN	[1]	R/W	R	EP1 Interrupt Enable bit 0 = Interrupt disable 1 = Enable	1
EP0_INT_EN	[0]	R/W	R	EP0 Interrupt Enable bit 0 = Interrupt disable 1 = Enable	1

Register	Address	R/W	Description	Reset Value
USB_INT_EN_REG	0x1500_016C(L) 0x1500_016F(B)	R/W (byte)	Determines which interrupt is enabled.	0x04

INT_MASK_REG	Bit	MCU	USB	Description	Initial State
RESET_INT_EN	[2]	R/W	R	Reset interrupt enable bit 0 = Interrupt disable 1 = Enable	1
Reserved	[1]	-	-	-	0
SUSPEND_INT_EN	[0]	R/W	R	Suspend interrupt enable bit 0 = Interrupt disable 1 = Enable	0

FRAME NUMBER REGISTER (FPAME_NUM1_REG, FRAME_NUM2_REG)

When host transfer USB packet, there is frame number in SOF(Start Of Frame). The USB catch this frame number and load it into this register, automatically.

Register	Address	R/W	Description	Reset Value
FRAME_NUM1_REG	0x5200_0170(L) 0x5200_0173(B)	R (byte)	Frame number lower byte register	0x00

FRAME_NUM_REG	Bit	MCU	USB	Description	Initial State
FRAME_NUM1	[7:0]	R	W	Frame number lower byte value	00

Register	Address	R/W	Description	Reset Value
FRAME_NUM2_REG	0x5200_0174(L) 0x5200_0177(B)	R (byte)	Frame number higher byte register	0x00

FRAME_NUM_REG	Bit	MCU	USB	Description	Initial State
FRAME_NUM2	[7:0]	R	W	Frame number higher byte value	00

INDEX REGISTER (INDEX_REG)

This INDEX register is used to indicate certain endpoint registers effectively. MCU can access the endpoint registers(MAXP_REG,IN_CSR1_REG,IN_CSR2_REG,OUT_CSR1_REG,OUT_CSR2_REG,OUT_FIFO_CNT1_REG, OUT_FIFO_CNT2_REG) for an endpoint inside the core using the INDEX register.

Register	Address	R/W	Description	Reset Value
INDEX_REG	0x5200_0178(L) 0x5200_017B(B)	R/W (byte)	Register index register	0x00

INDEX_REG	Bit	MCU	USB	Description	Initial State
INDEX	[7:0]	R/W	R	It indicates a certain endpoint.	00

END POINT0 CONTROL STATUS REGISTER (EP0_CSR)

This register has the control and status bits for Endpoint 0. Since a control transaction involves both IN and OUT tokens, there is only one CSR register, mapped to the IN CSR1 register.

(share IN1_CSR and can access by writing index register "0" and read/write IN1_CSR)

Register	Address	R/W	Description	Reset Value
EP0_CSR	0x5200_0184(L) 0x5200_0187(B)	R/W (byte)	Endpoint 0 status register	0x00

EP0_CSR	Bit	MCU	USB	Description	Initial State
SERVICED_SETUP_END	[7]	W	CLEAR	The MCU should write a "1" to this bit to clear SETUP_END	0
SERVICED_OUT_PKT_RDY	[6]	W	CLEAR	The MCU should write a "1" to this bit to clear OUT_PKT_RDY	0
SEND_STALL	[5]	R/W	CLEAR	MCU should writes a "1" to this bit at the same time it clears OUT_PKT_RDY, if it decodes an invalid token. 0 = Finish the STALL condition 1 = The USB issues a STALL and shake to the current control transfer.	0
SETUP_END	[4]	R	SET	The USB sets this bit when a control transfer ends before DATA_END is set. When the USB sets this bit, an interrupt is generated to the MCU. When such a condition occurs, the USB flushes the FIFO and invalidates MCU access to the FIFO.	0
DATA_END	[3]	SET	CLEAR	The MCU sets this bit below conditions: 1. After loading the last packet of data into the FIFO, at the same time IN_PKT_RDY is set. 2. While it clears OUT_PKT_RDY after unloading the last packet of data. 3. For a zero length data phase.	0
SENT_STALL	[2]	CLEAR	SET	The USB sets this bit if a control transaction is stopped due to a protocol violation. An interrupt is generated when this bit is set. The MCU should write "0" to clear this bit.	0
IN_PKT_RDY	[1]	SET	CLEAR	The MCU sets this bit after writing a packet of data into EP0 FIFO. The USB clears this bit once the packet has been successfully sent to the host. An interrupt is generated when the USB clears this bit, so as the MCU to load the next packet. For a zero length data phase, the MCU sets DATA_END at the same time.	0
OUT_PKT_RDY	[0]	R	SET	The USB sets this bit once a valid token is written to the FIFO. An interrupt is generated when the USB sets this bit. The MCU clears this bit by writing a "1" to the SERVICED_OUT_PKT_RDY bit.	0

END POINT IN CONTROL STATUS REGISTER (IN_CSR1_REG, IN_CSR2_REG)

Register	Address	R/W	Description	Reset Value
IN_CSR1_REG	0x5200_0184(L) 0x5200_0187(B)	R/W (byte)	IN END POINT control status register1	0x00

IN_CSR1_REG	Bit	MCU	USB	Description	Initial State
Reserved	[7]	-	-	-	0
CLR_DATA_ TOGGLE	[6]	R/W	R/ CLEAR	This bit can be used in Set-up procedure. 0 : There are alternation of DATA0 and DATA1 1 : The data toggle bit is cleared and PID in packet will maintain DATA0	0
SENT_STALL	[5]	R/ CLEAR	SET	The USB sets this bit when an IN token issues a STALL handshake, after the MCU sets SEND_STALL bit to start STALL handshaking. When the USB issues a STALL handshake, IN_PKT_RDY is cleared	0
SEND_STALL	[4]	W/R	R	0 : The MCU clears this bit to finish the STALL condition. 1 : The MCU issues a STALL handshake to the USB.	0
FIFO_FLUSH	[3]	W/ CLEAR	CLEAR	The MCU sets this bit if it intends to flush the packet in Input-related FIFO. This bit is cleared by the USB when the FIFO is flushed. The MCU is interrupted when this happens. If a token is in process, the USB waits until the transmission is complete before FIFO flushing. If two packets are loaded into the FIFO, only first packet (The packet is intended to be sent to the host) is flushed, and the corresponding IN_PKT_RDY bit is cleared	0
UNDER_RUN	[2]	R/ CLEAR	Set	*Valid For Iso Mode Only* The USB sets this bit when in ISO mode, an IN token is received and the IN_PKT_RDY bit is not set. The USB sends a zero length data packet for such conditions, and the next packet that is loaded into the FIFO is flushed. This bit is cleared by writing 0.	0
Reserved	[1]	-	-	-	0
IN_PKT_RDY	[0	R/SET	CLEAR	The MCU sets this bit, after writing a packet of data into the FIFO. The USB clears this bit once the packet has been successfully sent to the host. An interrupt is generated when te USB clears this bit, so the MCU can load the next packet. While this bit is set, the MCU will not be able to write to the FIFO. If the SEND STALL bit is set by the MCU, this bit cannot be set.	0

Register	Address	R/W	Description	Reset Value
IN_CSR2_REG	0x5200_0188(L) 0x5200_018B(B)	R/W (byte)	IN END POINT control status register2	0x20

IN_CSR1_REG	Bit	MCU	USB	Description	Initial State
AUTO_SET	[7]	R/W	R	If set, whenever the MCU writes MAXP data, IN_PKT_RDY will automatically be set by the core, without any intervention from MCU. If the MCU writes less than MAXP data, then IN_PKT_RDY bit has to be set by the MCU.	0
ISO	[6]	R/W	R	*This bit is used only for endpoints whose transfer type is programmable.* ' 1' Configures endpoint to ISO mode ' 0' Configures endpoint to Bulk mode	0
MODE_IN	[5]	R/W	R	*This bit is used only for endpoints whose direction is programmable.* ' 1' Configures Endpoint Direction as IN ' 0' Configures Endpoint Direction as OUT	1
IN_DMA_INT_EN	[4]	R/W	R	This bit determines whether the interrupt should be issued, or not, when the EP1 IN_PKT_RDY condition happens. This is only useful for DMA mode. 0 = Interrupt enable, 1 = Interrupt Disable	0

END POINT OUT CONTROL STATUS REGISTER(OUT_CSR1_REG, OUT_CSR2_REG)

Register	Address	R/W	Description	Reset Value
OUT_CSR1_REG	0x5200_0190(L) 0x5200_0193(B)	R/W (byte)	End Point out control status register1	0x00

OUT_CSR1_REG	Bit	MCU	USB	Description	Initial State
CLR_DATA_TOGGLE	[7]	R/W	CLEAR	When the MCU writes a 1 to this bit, the data toggle sequence bit is reset to DATA0.	0
SENT_STALL	[6]	CLEAR /R	SET	The USB sets this bit when an OUT token is ended with a STALL handshake. The USB issues a stall handshake to the host if it sends more than MAXP data for the OUT TOKEN.	0
SEND_STALL	[5]	R/W	R	0 : The MCU clears this bit to end the STALL condition handshake, IN PKT RDY is cleared. 1 : The MCU issues a STALL handshake to the USB. The MCU clears this bit to end the STALL condition handshake, IN PKT RDY is cleared.	0
FIFO_FLUSH	[4]	R/W	CLEAR	The MCU write a 1 to flush the FIFO. This bit can be set only when OUT_PKT_RDY (D0) is set. The packet due to be unloaded by the MCU will be flushed.	0
DATA_ERROR	[3]	R	R/W	*This bit is valid only in ISO mode.* This bit should be sampled with OUT_PKT_RDY . When set, it indicates the data packet due to be unloaded by the MCU has an error (either bit stuffing or CRC). If two packets are loaded into the FIFO, and the second packet has an error, then this bit gets set only after the first packet is unloaded. This bit is automatically cleared when OUT_PKT_RDY gets cleared.	0
OVER_RUN	[2]	R/Clear	R/W	*This bit is valid only in ISO mode.* This bit is set if the core is not able to load an OUT ISO token into the FIFO. MCU clears this bit by writing 0.	0
Reserved	[1]	-	-	-	0
OUT_PKT_RDY	[0]	R/ CLEAR	SET	The USB sets this bit after it has loaded a packet of data into the FIFO. Once the MCU reads the packet from FIFO, this bit should be cleared by MCU. (Write a "0")	0

Register	Address	R/W	Description	Reset Value
OUT_CSR2_REG	0x5200_0194(L) 0x5200_0197(B)	R/W (byte)	End Point out control status register2	0x00

OUT_CSR2_REG	Bit	MCU	USB	Description	Initial State
AUTO_CLR	[7]	R/W	R	If MCU set, whenever the MCU reads data from the OUT FIFO, OUT_PKT_RDY will automatically be cleared by the logic, without any intervention from MCU.	0
ISO	[6]	R/W	R	This bit determines endpoint transfer type. ' 0' : Configures endpoint to Bulk mode. ' 1' : Configures endpoint to ISO mode	0
OUT_DMA_INT_EN	[5]	R/W	R	This bit determines whether the interrupt should be issued, or not. OUT_PKT_RDY condition happens. This is only useful for DMA mode 0 = Interrupt Enaebl 1 = Interrupt Disable	0

END POINT FIFO REGISTER (EPN_FIFO_REG)

To access EPn FIFO, the MCU should access EPn_FIFO_REG.

Register	Address	R/W	Description	Reset Value
EP0_FIFO	0x5200_01C0(L) 0x5200_01C3 (B)	R/W (byte)	End Point0 FIFO register	0xXX
EP1_FIFO	0x5200_01C4(L) 0x5200_01C7(B)	R/W (byte)	End Point1 FIFO register	0xXX
EP2_FIFO	0x5200_01C8(L) 0x5200_01CB(B)	R/W (byte)	End Point2 FIFO register	0xXX
EP3_FIFO	0x5200_01CC(L) 0x5200_01CF(B)	R/W (byte)	End Point3 FIFO register	0xXX
EP4_FIFO	0x5200_01D0(L) 0x5200_01D3(B)	R/W (byte)	End Point4 FIFO register	0xXX

EPn_FIFO	Bit	MCU	USB	Description	Initial State
FIFO_DATA	[7:0]	R/W	R/W	FIFO data value	0xXX

MAX PACKET REGISTER (MAXP_REG)

Register	Address	R/W	Description	Reset Value
MAXP_REG	0x5200_018C(L) 0x5200_018F(B)	R/W (byte)	End Point MAX packet register	0x01

MAXP_REG	Bit	MCU	USB	Description	Initial State
MAXP	[3:0]	R/W	R	0000 : Reserved 0001 : MAXP = 8 Byte 0010 : MAXP = 16 Byte 0100 : MAXP = 32 Byte 1000 : MAXP = 64 Byte	0001

END POINT OUT WRITE COUNT REGISTER(OUT_FIFO_CNT1_REG, OUT_FIFO_CNT2_REG)

These registers maintain the number of bytes in the packet due to be unloaded by the MCU.

Register	Address	R/W	Description	Reset Value
OUT_FIFO_CNT1_REG	0x5200_0198(L) 0x5200_019B(B)	R (byte)	End Point out write count register1	0x00

OUT_FIFO_CNT1_REG	Bit	MCU	USB	Description	Initial State
OUT_CNT_LOW	[7:0]	R	W	Lower byte of write count	00

Register	Address	R/W	Description	Reset Value
OUT_FIFO_CNT2_REG	0x5200_019C(L) 0x5200_019F(B)	R (byte)	End Point out write count register2	0x00

OUT_FIFO_CNT2_REG	Bit	MCU	USB	Description	Initial State
OUT_CNT_HIGH	[7:0]	R	W	Higher byte of write count	00

DMA INTERFACE CONTROL REGISTER (EPN_DMA_CON)

Register	Address	R/W	Description	Reset Value
EP1_DMA_CON	0x5200_0200(L) 0x5200_0203(B)	R/W (byte)	EP1 DMA interface control register	0x00
EP2_DMA_CON	0x5200_0218(L) 0x5200_021B(B)	R/W (byte)	EP2 DMA interface control register	0x00
EP3_DMA_CON	0x5200_0240(L) 0x5200_0243(B)	R/W (byte)	EP3 DMA interface control register	0x00
EP4_DMA_CON	0x5200_0258(L) 0x5200_025B(B)	R/W (byte)	EP4 DMA interface control register	0x00

EPn_DMA_CON	Bit	MCU	USB	Description	Initial State
IN_RUN_OB	[7]	R	W	IN DMA Run Observation	0
STATE	[6:4]	R	W	DMA State Monitoring	0
DEMAND_MODE	[3]	R/W	R	DMA Demand mode enable bit ' 0' : Demand mode disable ' 1' : Demand mode enable	0
OUT_RUN_OB / OUT_DMA_RUN	[2]	R/W	R/W	This bit function is separated write and read operation Write operation: ' 0' = Stop ' 1' = Run Read operation: OUT DMA Run Observation	0
IN_DMA_RUN	[1]	R/W	R	This bit is used to start DMA operation 0 = Stop 1 = Run	0
DMA_MODE_EN	[0]	R/W	R	This bit is used to set DMA mode 0 = Interrupt Mode 1 = DMA Mode	0

DMA UNIT COUNTER REGISTER (EPN_DMA_UNIT)

This register is valid in demand mode. In case not demand mode, this register value must be set ‘ 0x01’

Register	Address	R/W	Description	Reset Value
EP1_DMA_UNIT	0x5200_0204(L) 0x5200_0207(B)	R/W (byte)	EP1 DMA transfer unit counter base register	0x00
EP2_DMA_UNIT	0x5200_021C(L) 0x5200_021F(B)	R/W (byte)	EP2 DMA transfer unit counter base register	0x00
EP3_DMA_UNIT	0x5200_0244(L) 0x5200_0247(B)	R/W (byte)	EP3 DMA transfer unit counter base register	0x00
EP4_DMA_UNIT	0x5200_025C(L) 0x5200_025F(B)	R/W (byte)	EP4 DMA transfer unit counter base register	0x00

DMA_UNIT	Bit	MCU	USB	Description	Initial State
EPn_UNIT_CNT	[7:0]	R/W	R	EP DMA transfer unit counter value	0x00

DMA FIFO COUNTER REGISTER (EPN_DMA_FIFO)

This register has byte size in FIFO to be transferred by DMA. In case OUT_DMA_RUN enable, the value in OUT FIFO Write Count Register1 will be loaded in this register automatically. In case of IN DMA Mode, the MCU should set proper value by S/W.

Register	Address	R/W	Description	Reset Value
EP1_DMA_FIFO	0x5200_0208(L) 0x5200_020B(B)	R/W (byte)	EP1 DMA transfer FIFO counter base register	0x00
EP2_DMA_FIFO	0x5200_0220(L) 0x5200_0223(B)	R/W (byte)	EP2 DMA transfer FIFO counter base register	0x00
EP3_DMA_FIFO	0x5200_0248(L) 0x5200_024B(B)	R/W (byte)	EP3 DMA transfer FIFO counter base register	0x00
EP4_DMA_FIFO	0x5200_0260(L) 0x5200_0263(B)	R/W (byte)	EP4 DMA transfer FIFO counter base register	0x00

DMA_FIFO	Bit	MCU	USB	Description	Initial State
EPn_FIFO_CNT	[7:0]	R/W	R	EP DMA transfer FIFO counter value	0x00

DMA TOTAL TRANSFER COUNTER REGISTER (EPN_DMA_TTC_L, EPN_DMA_TTC_M, EPN_DMA_TTC_H)

This register should have total number of bytes to be transferred using DMA.(Total 24bit Counter)

Register	Address	R/W	Description	Reset Value
EP1_DMA_TTC_L	0x5200_020C(L) 0x5200_020F(B)	R/W (byte)	EP1 DMA total transfer counter(lower byte)	0x00
EP1_DMA_TTC_M	0x5200_0210(L) 0x5200_0213(B)	R/W (byte)	EP1 DMA total transfer counter(middle byte)	0x00
EP1_DMA_TTC_H	0x5200_0214(L) 0x5200_0217(B)	R/W (byte)	EP1 DMA total transfer counter(higher byte)	0x00
EP2_DMA_TTC_L	0x5200_0224(L) 0x5200_0227(B)	R/W (byte)	EP2 DMA total transfer counter(lower byte)	0x00
EP2_DMA_TTC_M	0x5200_0228(L) 0x5200_022B(B)	R/W (byte)	EP2 DMA total transfer counter(middle byte)	0x00
EP2_DMA_TTC_H	0x5200_022C(L) 0x5200_022F(B)	R/W (byte)	EP2 DMA total transfer counter(higher byte)	0x00
EP3_DMA_TTC_L	0x5200_024C(L) 0x5200_024F(B)	R/W (byte)	EP3 DMA total transfer counter(lower byte)	0x00
EP3_DMA_TTC_M	0x5200_0250(L) 0x5200_0253(B)	R/W (byte)	EP3 DMA total transfer counter(middle byte)	0x00
EP3_DMA_TTC_H	0x5200_0254(L) 0x5200_0257(B)	R/W (byte)	EP3 DMA total transfer counter(higher byte)	0x00
EP4_DMA_TTC_L	0x5200_0264(L) 0x5200_0267(B)	R/W (byte)	EP4 DMA total transfer counter(lower byte)	0x00
EP4_DMA_TTC_M	0x5200_0268(L) 0x5200_026B(B)	R/W (byte)	EP4 DMA total transfer counter(middle byte)	0x00
EP4_DMA_TTC_H	0x5200_026C(L) 0x5200_026F(B)	R/W (byte)	EP4 DMA total transfer counter(higher byte)	0x00

DMA_TX	Bit	MCU	USB	Description	Initial State
EPn_TTC_L	[7:0]	R/W	R	DMA total transfer count value(lower byte)	0x00
EPn_TTC_M	[7:0]	R/W	R	DMA total transfer count value(middle byte)	0x00
EPn_TTC_H	[7:0]	R/W	R	DMA total transfer count value(higher byte)	0x00

14 INTERRUPT CONTROLLER(Preliminary)

OVERVIEW

The interrupt controller in S3C2410X01 receives the request from 32interrupt sources. These interrupt sources are provided by internal peripheral such as the DMA controller, UART and IIC, etc. In these interrupt sources, the UARTn and EINTn interrupts are 'OR'ed to the interrupt controller.

The role of the interrupt controller is to ask for the FIQ or IRQ interrupt requests to the ARM920T core after the arbitration process when there are multiple interrupt requests from internal peripherals and external interrupt request pins.

The arbitration process is performed by the hardware priority logic and the result is written to the interrupt pending register and users notice that register to know which interrupt has been requested.

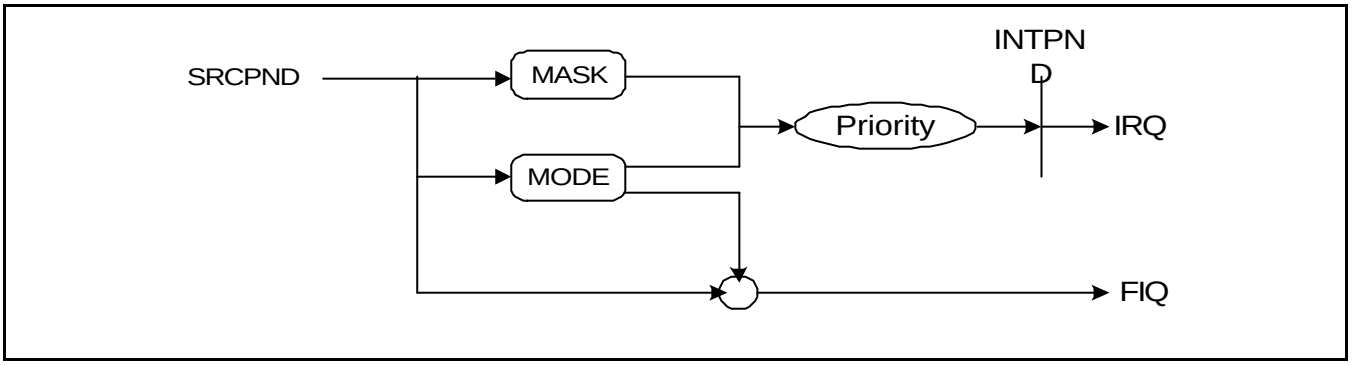


FIGURE 14-1. INTERRUPT PROCESS DIAGRAM

INTERRUPT CONTROLLER OPERATION

F-bit and I-bit of PSR (program status register)

If the F-bit of PSR (program status register in ARM920T CPU) is set to 1, the CPU does not accept the FIQ (fast interrupt request) from the interrupt controller. If I-bit of PSR (program status register in ARM920T CPU) is set to 1, the CPU does not accept the IRQ (interrupt request) from the interrupt controller. So, to enable the interrupt reception, the F-bit or I-bit of PSR has to be cleared to 0 and also the corresponding bit of INTMSK has to be set to 0.

Interrupt Mode

ARM920T has 2 types of interrupt mode, FIQ or IRQ. All the interrupt sources determine the mode of interrupt to be used at interrupt request.

Interrupt Pending Register

S3C2410X01 has two interrupt pending resisters. The one is source pending register(SRCPND), the other is interrupt pending register(INTPND). These pending registers indicate whether or not an interrupt request is pending. When the interrupt sources request interrupt service the corresponding bits of SRCPND register are set to 1, at the same time the only one bit of INTPND register is set to 1 automatically after arbitration process. If interrupts are masked, the corresponding bits of SRCPND register are set to 1, but the bit of INTPND register is not changed. When a pending bit of INTPND register is set, the interrupt service routine starts whenever the I-flag or F-flag is cleared to 0. The SRCPND and INTPND registers can be read and written, so the service routine must clear the pending condition by writing a 1 to the corresponding bit in SRCPND register first and then clear the pending condition in INTPND registers same method.

Interrupt Mask Register

Indicates that an interrupt has been disabled if the corresponding mask bit is 1. If an interrupt mask bit of INTMSK is 0, the interrupt will be serviced normally. If the corresponding mask bit is 1 and the interrupt is generated, the source pending bit will be set.

INTERRUPT SOURCES

Interrupt controller supports 32 interrupt sources as shown in below table. Two UART error interrupt requests are Ored to provide a single interrupt source to the interrupt controller.

Sources	Descriptions	Arbiter Group
INT_ADC	ADC EOC interrupt	ARB5
INT_RTC	RTC alarm interrupt	ARB5
INT_SPI1	SPI1 interrupt	ARB5
INT_UART0	UART0 Interrupt (ERR,RXD,TXD)	ARB5
INT_IIC	IIC interrupt	ARB4
INT_USBH	USB Host interrupt	ARB4
INT_USBD	USB Device interrupt	ARB4
reserved	reserved	ARB4
INT_UART1	UART1 Interrupt (ERR,RXD,TXD)	ARB4
INT_SPI0	SPI0 interrupt	ARB4
INT_SDI	SDI interrupt	ARB 3
INT_DMA3	DMA channel 3 interrupt	ARB3
INT_DMA2	DMA channel 2 interrupt	ARB3
INT_DMA1	DMA channel 1 interrupt	ARB3
INT_DMA0	DMA channel 0 interrupt	ARB3
INT_LCD	LCD interrupt	ARB3
INT_UART2	UART2 Interrupt (ERR,RXD,TXD)	ARB2
INT_TIMER4	Timer4 interrupt	ARB2
INT_TIMER3	Timer3 interrupt	ARB2
INT_TIMER2	Timer2 interrupt	ARB2
INT_TIMER1	Timer1 interrupt	ARB 2
INT_TIMER0	Timer0 interrupt	ARB2
INT_WDT	Watch-Dog timer interrupt	ARB1
INT_TICK	RTC Time tick interrupt	ARB1
BAT_FLT	Battery Fault interrupt	ARB1
reserved	reserved	ARB1
EINT8_23	External interrupt 8 – 23	ARB1
EINT4_7	External interrupt 4 – 7	ARB1
EINT3	External interrupt 3	ARB0
EINT2	External interrupt 2	ARB0
EINT1	External interrupt 1	ARB0
EINT0	External interrupt 0	ARB0

INTERRUPT PRIORITY GENERATING BLOCK

The priority logic for 32 interrupt requests is composed of seven rotation based arbiters: six first-level arbiters and one second-level arbiter as shown in the following figure.

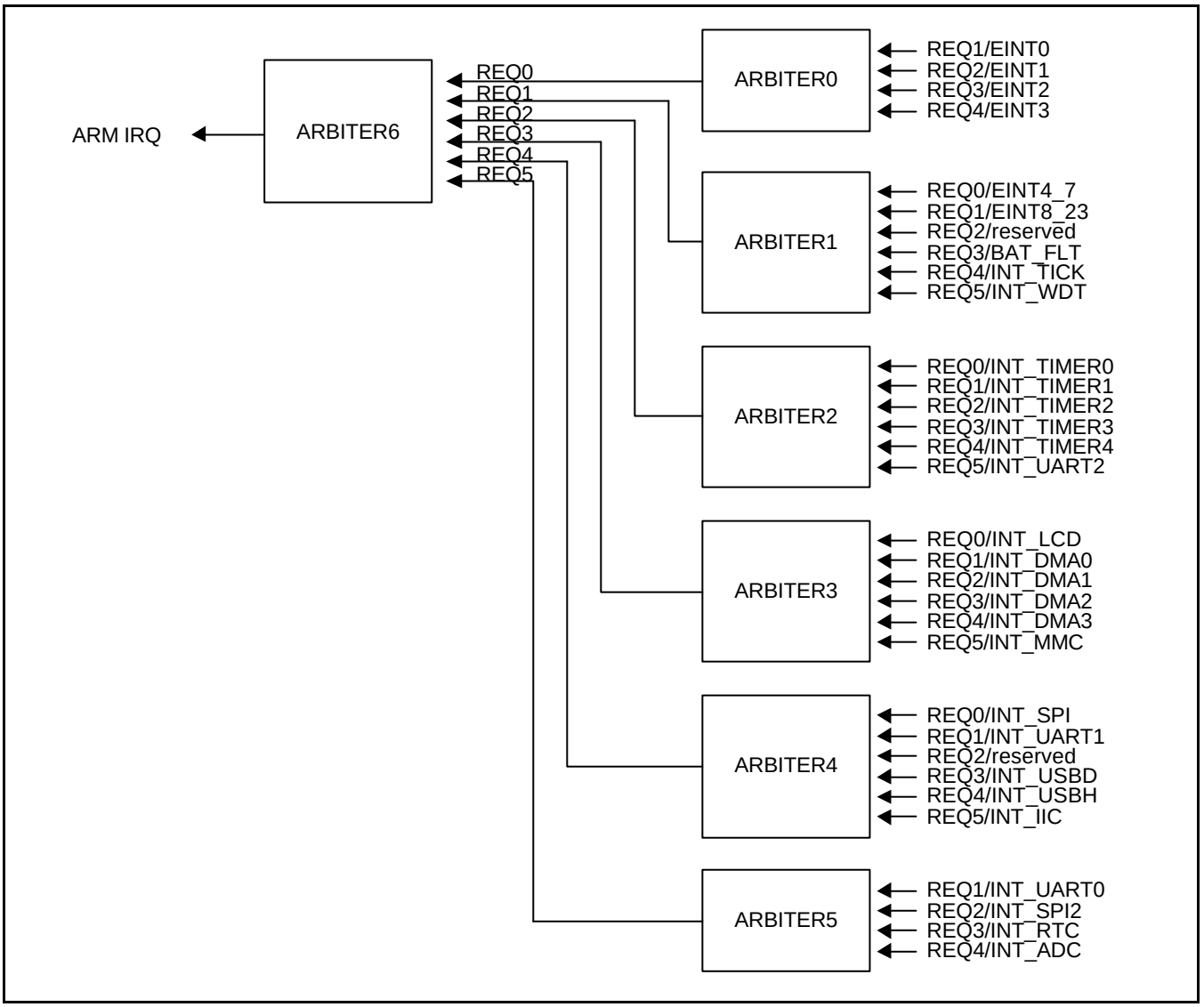


Figure 14-1. Priority Generating Block

INTERRUPT PRIORITY

Each arbiter can handle six interrupt requests based on the one bit arbiter mode control(ARB_MODE) and two bits of selection control signals(ARB_SEL) as follows:

If ARB_SEL bits are 00b, the priority order is REQ0, REQ1, REQ2, REQ3, REQ4, and REQ5.

If ARB_SEL bits are 01b, the priority order is REQ0, REQ2, REQ3, REQ4, REQ1, and REQ5.

If ARB_SEL bits are 10b, the priority order is REQ0, REQ3, REQ4, REQ1, REQ2, and REQ5.

If ARB_SEL bits are 11b, the priority order is REQ0, REQ4, REQ1, REQ2, REQ3, and REQ5.

Note that REQ0 of an arbiter is always the highest priority, and REQ5 is the lowest one. In addition, by changing the ARB_SEL bits, we can rotate the priority of REQ1 - REQ4.

Here, if ARB_MODE bit is set to 0, ARB_SEL bits are not automatically changed, thus the arbiter operates in the fixed priority mode. (Note that even in this mode, we can change the priority by manually changing the ARB_SEL bits.). On the other hand, if ARB_MODE bit is 1, ARB_SEL bits are changed in rotation fashion, e.g., if REQ1 is serviced, ARB_SEL bits are changed to 01b automatically so as to make REQ1 the lowest priority one. The detailed rule of ARB_SEL change is as follows.

If REQ0 or REQ5 is serviced, ARB_SEL bits are not changed at all.

If REQ1 is serviced, ARB_SEL bits are changed to 01b.

If REQ2 is serviced, ARB_SEL bits are changed to 10b.

If REQ3 is serviced, ARB_SEL bits are changed to 11b.

If REQ4 is serviced, ARB_SEL bits are changed to 00b.

INTERRUPT CONTROLLER SPECIAL REGISTERS

There are five control registers in the interrupt controller: source pending register, interrupt mode register, mask register, priority register, and interrupt pending register.

All the interrupt requests from the interrupt sources are first registered in the source pending register. They are divided into two groups based on the interrupt mode register, i.e., one FIQ request and the remaining IRQ requests. Arbitration process is performed for the multiple IRQ requests based on the priority register.

SOURCE PENDING REGISTER (SRCPND)

SRCPND register is composed of 32 bits each of which is related to an interrupt source. Each bit is set to 1 if the corresponding interrupt source generates the interrupt request and waits for the interrupt to be serviced. By reading this register, we can see the interrupt sources waiting for their requests to be serviced. Note that each bit of SRCPND register is automatically set by the interrupt sources regardless of the masking bits in the INTMASK register. In addition, it is not affected by the priority logic of interrupt controller.

In the interrupt service routine for a specific interrupt source, the corresponding bit of SRCPND register has to be cleared to get the interrupt request from the same source correctly. If you return from the ISR without clearing the bit, interrupt controller operates as if another interrupt request comes in from the same source. In other words, if a specific bit of SRCPND register is set to 1, it is always considered as a valid interrupt request waiting to be serviced.

The specific time to clear the corresponding bit depends on the user's requirement. The bottom line is that if you want to receive another valid request from the same source you should clear the corresponding bit first, and then enable the interrupt.

You can clear a specific bit of SRCPND register by writing a data to this register. It clears only the bit positions of SRCPND corresponding to those set to one in the data. The bit positions corresponding to those that are set to 0 in the data remains as they are with no change

Register	Address	R/W	Description	Reset Value
SRCPND	0X4a000000	R/W	Indicates the interrupt request status. 0 = The interrupt has not been requested 1 = The interrupt source has asserted the interrupt request	0x00000000

SRCPND	Bit	Description	Initial State
INT_ADC	[31]	0 = Not requested, 1 = Requested	0
INT_RTC	[30]	0 = Not requested, 1 = Requested	0
INT_SPI1	[29]	0 = Not requested, 1 = Requested	0
INT_UART0	[28]	0 = Not requested, 1 = Requested	0
INT_IIC	[27]	0 = Not requested, 1 = Requested	0
INT_USBH	[26]	0 = Not requested, 1 = Requested	0
INT_USBD	[25]	0 = Not requested, 1 = Requested	0
reserved	[24]	Not used	0
INT_UART1	[23]	0 = Not requested, 1 = Requested	0
INT_SPI0	[22]	0 = Not requested, 1 = Requested	0
INT_MMC	[21]	0 = Not requested, 1 = Requested	0
INT_DMA3	[20]	0 = Not requested, 1 = Requested	0
INT_DMA2	[19]	0 = Not requested, 1 = Requested	0
INT_DMA1	[18]	0 = Not requested, 1 = Requested	0
INT_DMA0	[17]	0 = Not requested, 1 = Requested	0
INT_LCD	[16]	0 = Not requested, 1 = Requested	0
INT_UART2	[15]	0 = Not requested, 1 = Requested	0
INT_TIMER4	[14]	0 = Not requested, 1 = Requested	0
INT_TIMER3	[13]	0 = Not requested, 1 = Requested	0
INT_TIMER2	[12]	0 = Not requested, 1 = Requested	0
INT_TIMER1	[11]	0 = Not requested, 1 = Requested	0
INT_TIMER0	[10]	0 = Not requested, 1 = Requested	0
INT_WDT	[9]	0 = Not requested, 1 = Requested	0
INT_TICK	[8]	0 = Not requested, 1 = Requested	0
BAT_FLT	[7]	0 = Not requested, 1 = Requested	0
reserved	[6]	Not used	0
EINT8_23	[5]	0 = Not requested, 1 = Requested	0
EINT4_7	[4]	0 = Not requested, 1 = Requested	0
EINT3	[3]	0 = Not requested, 1 = Requested	0
EINT2	[2]	0 = Not requested, 1 = Requested	0
EINT1	[1]	0 = Not requested, 1 = Requested	0
EINT0	[0]	0 = Not requested, 1 = Requested	0

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INTERRUPT MODE REGISTER (INTMOD)

This register is composed of 32 bits each of which is related to an interrupt source. If a specific bit is set to 1, the corresponding interrupt is processed in the FIQ (fast interrupt) mode. Otherwise, it is processed in the IRQ mode (normal interrupt).

Note that at most only one interrupt source can be serviced in the FIQ mode in the interrupt controller. (You should use the FIQ mode only for the urgent interrupt.) Thus, only one bit of INTMOD can be set to 1 at most.

Register	Address	R/W	Description	Reset Value
INTMOD	0X4a000004	R/W	Interrupt mode regiseter. 0 = IRQ mode 1 = FIQ mode	0x00000000

NOTE : If an interrupt mode is set to FIQ mode in INTMOD register, FIQ interrupt will not affect INTPND and INTOFFSET registers. The INTPND and INTOFFSET registers are valid only for IRQ mode interrupt source.

INTMOD	Bit	Description	Initial State
INT_ADC	[31]	0 = IRQ, 1 = FIQ	0
INT_RTC	[30]	0 = IRQ, 1 = FIQ	0
INT_SPI1	[29]	0 = IRQ, 1 = FIQ	0
INT_UART0	[28]	0 = IRQ, 1 = FIQ	0
INT_IIC	[27]	0 = IRQ, 1 = FIQ	0
INT_USBH	[26]	0 = IRQ, 1 = FIQ	0
INT_USBD	[25]	0 = IRQ, 1 = FIQ	0
reserved	[24]	Not used	0
INT_URRT1	[23]	0 = IRQ, 1 = FIQ	0
INT_SPI0	[22]	0 = IRQ, 1 = FIQ	0
INT_MMC	[21]	0 = IRQ, 1 = FIQ	0
INT_DMA3	[20]	0 = IRQ, 1 = FIQ	0
INT_DMA2	[19]	0 = IRQ, 1 = FIQ	0
INT_DMA1	[18]	0 = IRQ, 1 = FIQ	0
INT_DMA0	[17]	0 = IRQ, 1 = FIQ	0
INT_LCD	[16]	0 = IRQ, 1 = FIQ	0
INT_UART2	[15]	0 = IRQ, 1 = FIQ	0
INT_TIMER4	[14]	0 = IRQ, 1 = FIQ	0
INT_TIMER3	[13]	0 = IRQ, 1 = FIQ	0
INT_TIMER2	[12]	0 = IRQ, 1 = FIQ	0
INT_TIMER1	[11]	0 = IRQ, 1 = FIQ	0
INT_TIMER0	[10]	0 = IRQ, 1 = FIQ	0
INT_WDT	[9]	0 = IRQ, 1 = FIQ	0
INT_TICK	[8]	0 = IRQ, 1 = FIQ	0
BAT_FLT	[7]	0 = IRQ, 1 = FIQ	0
reserved	[6]	Not used	0
EINT8_23	[5]	0 = IRQ, 1 = FIQ	0
EINT4_7	[4]	0 = IRQ, 1 = FIQ	0
EINT3	[3]	0 = IRQ, 1 = FIQ	0
EINT2	[2]	0 = IRQ, 1 = FIQ	0
EINT1	[1]	0 = IRQ, 1 = FIQ	0
EINT0	[0]	0 = IRQ, 1 = FIQ	0

INTERRUPT MASK REGISTER (INTMSK)

Each of the 32 bits in the interrupt mask register is related to an interrupt source. If you set a specific bit to 1, the CPU does not service the interrupt request from the corresponding interrupt source. (Note that even in such a case, the corresponding bit of SRCPND register is set to 1). If the mask bit is 0, the interrupt request can be serviced.

Register	Address	R/W	Description	Reset Value
INTMSK	0X4a000008	R/W	Determines which interrupt source is masked. The masked interrupt source will not be serviced. 0 = Interrupt service is available 1 = Interrupt service is masked	0xffffffff

INTMSK	Bit	Description	Initial State
INT_ADC	[31]	0 = Service available, 1 = Masked	1
INT_RTC	[30]	0 = Service available, 1 = Masked	1
INT_SPI1	[29]	0 = Service available, 1 = Masked	1
INT_UART0	[28]	0 = Service available, 1 = Masked	1
INT_IIC	[27]	0 = Service available, 1 = Masked	1
INT_USBH	[26]	0 = Service available, 1 = Masked	1
INT_USBD	[25]	0 = Service available, 1 = Masked	1
reserved	[24]	Not used	1
INT_UART1	[23]	0 = Service available, 1 = Masked	1
INT_SPI0	[22]	0 = Service available, 1 = Masked	1
INT_MMC	[21]	0 = Service available, 1 = Masked	1
INT_DMA3	[20]	0 = Service available, 1 = Masked	1
INT_DMA2	[19]	0 = Service available, 1 = Masked	1
INT_DMA1	[18]	0 = Service available, 1 = Masked	1
INT_DMA0	[17]	0 = Service available, 1 = Masked	1
INT_LCD	[16]	Not used	1
INT_UART2	[15]	0 = Service available, 1 = Masked	1
INT_TIMER4	[14]	0 = Service available, 1 = Masked	1
INT_TIMER3	[13]	0 = Service available, 1 = Masked	1
INT_TIMER2	[12]	0 = Service available, 1 = Masked	1
INT_TIMER1	[11]	0 = Service available, 1 = Masked	1
INT_TIMER0	[10]	0 = Service available, 1 = Masked	1
INT_WDT	[9]	0 = Service available, 1 = Masked	1
INT_TICK	[8]	0 = Service available, 1 = Masked	1
BAT_FLT	[7]	0 = Service available, 1 = Masked	1
reserved	[6]	0 = Service available, 1 = Masked	1
EINT8_23	[5]	0 = Service available, 1 = Masked	1
EINT4_7	[4]	0 = Service available, 1 = Masked	1
EINT3	[3]	0 = Service available, 1 = Masked	1
EINT2	[2]	0 = Service available, 1 = Masked	1
EINT1	[1]	0 = Service available, 1 = Masked	1
EINT0	[0]	0 = Service available, 1 = Masked	1

PRIORITY REGISTER (PRIORITY)

Register	Address	R/W	Description	Reset Value
PRIORITY	0x4a00000c	R/W	IRQ priority control register	0x7f

PRIORITY	Bit	Description	Initial State
ARB_SEL6	[20:19]	Arbiter 6 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL5	[18:17]	Arbiter 5 group priority order set 00 = REQ 1-2-3-4 01 = REQ 2-3-4-1 10 = REQ 3-4-1-2 11 = REQ 4-1-2-3	0
ARB_SEL4	[16:15]	Arbiter 4 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL3	[14:13]	Arbiter 3 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL2	[12:11]	Arbiter 2 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL1	[10:9]	Arbiter 1 group priority order set 00 = REQ 0-1-2-3-4-5 01 = REQ 0-2-3-4-1-5 10 = REQ 0-3-4-1-2-5 11 = REQ 0-4-1-2-3-5	0
ARB_SEL0	[8:7]	Arbiter 0 group priority order set 00 = REQ 1-2-3-4 01 = REQ 2-3-4-1 10 = REQ 3-4-1-2 11 = REQ 4-1-2-3	0
ARB_MODE6	[6]	Arbiter 6 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
ARB_MODE5	[5]	Arbiter 5 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
ARB_MODE4	[4]	Arbiter 4 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
ARB_MODE3	[3]	Arbiter 3 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
ARB_MODE2	[2]	Arbiter 2 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
ARB_MODE1	[1]	Arbiter 1 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1
ARB_MODE0	[0]	Arbiter 0 group priority rotate enable 0 = Priority does not rotate, 1 = Priority rotate enable	1

INTERRUPT PENDING REGISTER (INTPND)

Each of the 32 bits in the interrupt pending register shows whether the corresponding interrupt request is the highest priority one that is unmasked and waits for the interrupt to be serviced. Since INTPND is located after the priority logic, only one bit can be set to 1 at most, and that is the very interrupt request generating IRQ to CPU. In interrupt service routine for IRQ, you can read this register to determine the interrupt source to be serviced among 32 sources.

Like the SRCPND, this register has to be cleared in the interrupt service routine after clearing SRCPND register. We can clear a specific bit of INTPND register by writing a data to this register. It clears only the bit positions of INTPND corresponding to those set to one in the data. The bit positions corresponding to those that are set to 0 in the data remains as they are with no change.

Register	Address	R/W	Description	Reset Value
INTPND	0X4a000010	R/W	Indicates the interrupt request status. 0 = The interrupt has not been requested 1 = The interrupt source has asserted the interrupt request	0x00000000

NOTE : If the FIQ mode interrupt is occurred, the corresponding bit of INTPND will not be turned on. Because the INTPND register is available only for IRQ mode interrupt.

INTPND	Bit	Description	Initial State

INT_ADC	[31]	0 = Not requested, 1 = Requested	0
INT_RTC	[30]	0 = Not requested, 1 = Requested	0
INT_SPI1	[29]	0 = Not requested, 1 = Requested	0
INT_UART0	[28]	0 = Not requested, 1 = Requested	0
INT_IIC	[27]	0 = Not requested, 1 = Requested	0
INT_USBH	[26]	0 = Not requested, 1 = Requested	0
INT_USBD	[25]	0 = Not requested, 1 = Requested	0
reserved	[24]	Not used	0
INT_UART1	[23]	0 = Not requested, 1 = Requested	0
INT_SPI0	[22]	0 = Not requested, 1 = Requested	0
INT_MMC	[21]	0 = Not requested, 1 = Requested	0
INT_DMA3	[20]	0 = Not requested, 1 = Requested	0
INT_DMA2	[19]	0 = Not requested, 1 = Requested	0
INT_DMA1	[18]	0 = Not requested, 1 = Requested	0
INT_DMA0	[17]	0 = Not requested, 1 = Requested	0
INT_LCD	[16]	0 = Not requested, 1 = Requested	0
INT_UART21	[15]	0 = Not requested, 1 = Requested	0
INT_TIMER4	[14]	0 = Not requested, 1 = Requested	0
INT_TIMER3	[13]	0 = Not requested, 1 = Requested	0
INT_TIMER2	[12]	0 = Not requested, 1 = Requested	0
INT_TIMER1	[11]	0 = Not requested, 1 = Requested	0
INT_TIMER0	[10]	0 = Not requested, 1 = Requested	0
INT_WDT	[9]	0 = Not requested, 1 = Requested	0
INT_TICK	[8]	0 = Not requested, 1 = Requested	0
BAT_FLT	[7]	0 = Not requested, 1 = Requested	0
reserved	[6]	Not used	0
EINT8_23	[5]	0 = Not requested, 1 = Requested	0
EINT4_7	[4]	0 = Not requested, 1 = Requested	0
EINT3	[3]	0 = Not requested, 1 = Requested	0
EINT2	[2]	0 = Not requested, 1 = Requested	0
EINT1	[1]	0 = Not requested, 1 = Requested	0
EINT0	[0]	0 = Not requested, 1 = Requested	0

INTERRUPT OFFSET REGISTER (INTOFFSET)

The number in the interrupt offset register shows which interrupt request of IRQ mode is in the INTPND register. This bit can be cleared automatically by clearing SRCPND and INTPND.

Register	Address	R/W	Description	Reset Value
INTOFFSET	0X4a000014	R	Indicates the IRQ interrupt request source	0x00000000

INT Source	The OFFSET value	INT Source	The OFFSET value
INT_ADC	31	INT_UART2	15
INT_RTC	30	INT_TIMER4	14
INT_SPI1	29	INT_TIMER3	13
INT_UART0	28	INT_TIMER2	12
INT_IIC	27	INT_TIMER1	11
INT_USBH	26	INT_TIMER0	10
INT_USBD	25	INT_WDT	9
reserved	24	INT_TICK	8
INT_UART1	23	BAT_FLT	7
INT_SPI0	22	reserved	6
INT_MMC	21	EINT8_23	5
INT_DMA3	20	EINT4_7	4
INT_DMA2	19	EINT3	3
INT_DMA1	18	EINT2	2
INT_DMA0	17	EINT1	1
INT_LCD	16	EINT0	0

NOTE : If the FIQ mode interrupt is occurred, the INTOFFSET will not be affected. Because the INTOFFSET register is available only for IRQ mode interrupt.

SUB SOURCE PENDING REGISTER (SUBSRCPND)

You can clear a specific bit of SUBSRCPND register by writing a data to this register. It clears only the bit positions of SRCPND corresponding to those set to one in the data. The bit positions corresponding to those that are set to 0 in the data remains as they are with no change.

Register	Address	R/W	Description	Reset Value
SUBSRCPND	0X4a0000018	R/W	Indicates the interrupt request status. 0 = The interrupt has not been requested 1 = The interrupt source has asserted the interrupt request	0x00000000

SUBSRCPND	Bit	Description	Initial State
reserved	[31:11]	Not used	0
INT_ADC	[10]	0 = Not requested, 1 = Requested	0
INT_TC	[9]	0 = Not requested, 1 = Requested	0
INT_ERR2	[8]	0 = Not requested, 1 = Requested	0
INT_TXD2	[7]	0 = Not requested, 1 = Requested	0
INT_RXD2	[6]	0 = Not requested, 1 = Requested	0
INT_ERR1	[5]	0 = Not requested, 1 = Requested	0
INT_TXD1	[4]	0 = Not requested, 1 = Requested	0
INT_RXD1	[3]	0 = Not requested, 1 = Requested	0
INT_ERR0	[2]	0 = Not requested, 1 = Requested	0
INT_TXD0	[1]	0 = Not requested, 1 = Requested	0
INT_RXD0	[0]	0 = Not requested, 1 = Requested	0

INTERRUPT SUB MASK REGISTER (INTSUBMSK)

Each of the 32 bits in the interrupt mask register is related to an interrupt source. If you set a specific bit to 1, the interrupt request from the corresponding interrupt source is not serviced by the CPU. (Note that even in such a case, the corresponding bit of SRCPND register is set to 1). If the mask bit is 0, the interrupt request can be serviced.

Register	Address	R/W	Description	Reset Value
INTSUBMSK	0X4a00001c	R/W	Determines which interrupt source is masked. The masked interrupt source will not be serviced. 0 = Interrupt service is available 1 = Interrupt service is masked	0x3777

INTSUBMSK	Bit	Description	Initial State
reserved	[31:11]	Not used	0
INT_ADC	[10]	0 = Service available, 1 = Masked	1
INT_TC	[9]	0 = Service available, 1 = Masked	1
INT_ERR2	[8]	0 = Service available, 1 = Masked	1
INT_TXD2	[7]	0 = Service available, 1 = Masked	1
INT_RXD2	[6]	0 = Service available, 1 = Masked	1
INT_ERR1	[5]	0 = Service available, 1 = Masked	1
INT_TXD1	[4]	0 = Service available, 1 = Masked	1
INT_RXD1	[3]	0 = Service available, 1 = Masked	1
INT_ERR0	[2]	0 = Service available, 1 = Masked	1
INT_TXD0	[1]	0 = Service available, 1 = Masked	1
INT_RXD0	[0]	0 = Service available, 1 = Masked	1

12/20/2001

15 LCD CONTROLLER (PRELIMINARY)

OVERVIEW

The LCD controller within S3C2410X01 consists of logic for transferring LCD image data from a video buffer located in system memory to an external LCD driver.

The LCD controller supports monochrome, 2-bit per pixel (4-level gray scale) or 4-bit per pixel (16-level gray scale) mode on a monochrome LCD, using a time-based dithering algorithm and FRC (Frame Rate Control) method and it can be interfaced with a color LCD panel at 8-bit per pixel (256-level color) and 12-bit per pixel (4096-level color) for interfacing with STN LCD.
It can support 1-bit per pixel, 2-bit per pixel, 4-bit per pixel, 8-bit per pixel for interfacing with the palettized TFT color LCD panel, 16-bit per pixel and 24-bit per pixel non-palettized true-color display.

The LCD controller can be programmed to support the different requirements on the screen related to the number of horizontal and vertical pixels, data line width for the data interface, interface timing, and refresh rate.

FEATURES

STN LCD displays features

— Supports 3 types of LCD panels: 4-bit dual scan, 4-bit single scan, 8-bit single scan display type.

— Supports the monochrome, 4 gray levels, and 16 gray levels .

— Supports 256 colors and 4096 colors for color STN LCD panel.

— Supports multiple screen size.
Typical actual screen sizes: 640x480, 320x240, 160x160 and etc
Maximum virtual screen size is 4Mbytes;
Maximum virtual screen size of 256 color mode: 4096x1024, 2048x2048, 1024x4096, etc

TFT LCD displays features

— Supports 1, 2, 4 or 8-bpp(bit per pixel) palettized color displays for TFT.

Supports 16-bpp non-palettized true-color displays for color TFT.

Supports 24-bpp non-palettized true-color displays for color TFT.

— Supports maximum 16M color TFT at 24bit per pixel mode.

— Supports multiple screen size.
Typical actual screen size: 800x600(16bpp), 640x480, 320x240, 160x160 and etc
Maximum virtual screen size is 4Mbytes;
Maximum virtual screen size of 64K color mode: 2048x1024 etc

COMMON FEATURES

Dedicated DMA supports to fetch the image data from video buffer located in system memory.

— Dedicated interrupt functions(INT_FrSyn, INT_FiCnt)

— The system memory is used as the display memory.

— Supports Multiple Virtual Display Screen.(Supports Hardware Horizontal/Vertical Scrolling)

— Programmable timing control for different display panels.

— Supports little and big-endian byte ordering, as well as WinCE data formats.

— Supports SEC TFT LCD panel(SAMSUNG 3.5″ Portrait / 256K Color /Reflective a-Si TFT LCD)
LTS350Q1-PD1 : TFT LCD panel with touch panel and front light unit
LTS350Q1-PD2 : TFT LCD panel only

EXTERNAL INTERFACE SIGNAL

VFRAME / VSYNC / STV: Frame synchronous signal(STN) / Vertical synchronous signal(TFT) / SEC TFT Signal

VLINE / HSYNC / CPV: Line synchronous pulse signal (STN) / Horizontal sync signal (TFT) / SEC TFT Signal

VCLK / LCD_HCLK: Pixel clock signal (STN / TFT) / SEC TFT Signal

VD[23:0]: LCD pixel data output ports (STN / TFT/ SEC TFT)

VM / VDEN / TP: AC bias signal for the LCD driver (STN) / Data enable signal (TFT) / SEC TFT Signal

LEND / STH: Line end signal (TFT) / SEC TFT Signal

LCD_PWREN: LCD panel power enable control signal

LCDVF0: SEC TFT Signal OE

LCDVF1: SEC TFT Signal REV

LCDVF2: SEC TFT Signal REVB

Total 33 output ports : data 24 bits, control 9 bits

CAUTION :
S3C2410X01 has HCLK. It means the clock of AHB bus.
Accidentally, SEC TFT LCD panel (LTS350Q1-PD1 and PD2) has HCLK(Horizontal Sampling Clock) also.
These two HCLK can cause a confusion. So, we' ll distinguish these signals as follows in this chapter;

HCLK of S3C2410X01 is HCLK.
HCLK of SEC TFT LCD panel (LTS350Q1-PD1 and PD2) is changed to LCD_HCLK.

BLOCK DIAGRAM

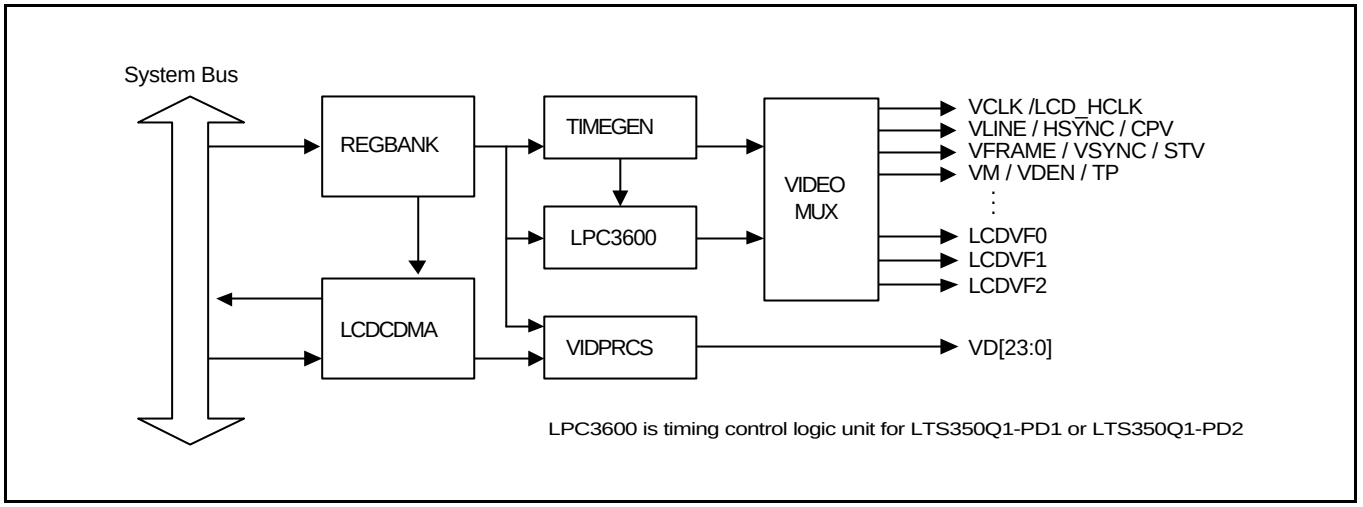


Figure 15-1. LCD Controller Block Diagram

The LCD controller within S3C2410X01 is used to transfer the video data and to generate the necessary control signals such as, VFRAME, VLINE, VCLK, VM and so on. As well as the control signals, S3C2410X01has the data ports for video data, which are VD[23:0] as shown in Figure 15-1. The LCD controller consists of a REGBANK, LCDCDMA, VIDPRCS, TIMEGEN, and LPC3600 (See Figure 15-1 LCD Controller Block Diagram). The REGBANK has 17 programmable register sets and 256x16 palette memory which are used to configure the LCD controller. The LCDCDMA is a dedicated DMA, which it can transfer the video data in frame memory to LCD driver, automatically. By using this special DMA, the video data can be displayed on the screen without CPU intervention. The VIDPRCS receives the video data from LCDCDMA and sends the video data through the VD[23:0] data ports to the LCD driver after changing them into a suitable data format, for example 4/8-bit single scan or 4-bit dual scan display mode. The TIMEGEN consists of programmable logic to support the variable requirement of interface timing and rates commonly found in different LCD drivers. The TIMEGEN block generates VFRAME, VLINE, VCLK, VM, and so on.

The description of data flow is as follows:

FIFO memory is present in the LCDCDMA. When FIFO is empty or partially empty, LCDCDMA requests data fetching from the frame memory based on the burst memory transfer mode(Consecutive memory fetching of 4 words(16 bytes) per one burst request without allowing the bus mastership to another bus master during the bus transfer). When this kind of transfer request is accepted by bus arbitrator in the memory controller, there will be four successive word data transfers from system memory to internal FIFO. The total size of FIFO is 28 words, which consists of 12 words FIFOL and 16 words FIFOH, respectively. The S3C2410X01 has two FIFOs because it needs to support the dual scan display mode. In case of single scan mode, one of them(FIFOH) can only be used.

STN LCD CONTROLLER OPERATION

TIMING GENERATOR

The TIMEGEN generates the control signals for LCD driver such as, VFRAME, VLINE, VCLK, and VM. These control signals are closely related to the configuration on the LCDCON1/2/3/4/5 register in the REGBANK. Based on these programmable configurations on the LCD control registers in REGBANK, the TIMEGEN can generate the programmable control signals suitable to support many different types of LCD drivers.

The VFRAME pulse is asserted for a duration of the entire first line at a frequency of once per frame. The VFRAME signal is asserted to bring the LCD's line pointer to the top of the display to start over.

The VM signal is used by the LCD driver to alternate the polarity of the row and column voltage which are used to turn the pixel on and off. The toggling rate of VM signal can be controlled by using the MMODE bit of LCDCON1 register and MVAL field of LCDCON4 register. If the MMODE bit is 0, the VM signal is configured to toggle on every frame. If the MMODE bit is 1, the VM signal is configured to toggle on the every event of the elapse of the specified number of VLINE by the MVAL[7:0] value. Figure 15-5 shows an example for MMODE=0 and for MMODE=1 with the value of MVAL[7:0]=0x2. When MMODE=1, the VM rate is related to MVAL[7:0], as shown below:

VM Rate = VLINE Rate / (2 * MVAL)

The VFRAME and VLINE pulse generation is controlled by the configurations of the HOZVAL field and the LINEVAL field in the LCDCON2/3 register. Each field is related to the LCD size and display mode. In other words, the HOZVAL and LINEVAL can be determined by the size of the LCD panel and the display mode according to the following equation:

HOZVAL = (Horizontal display size / Number of the valid VD data line)-1

In color mode: Horizontal display size = 3 * Number of Horizontal Pixel

In the 4-bit single scan display mode, number of valid VD data lines should be 4. In case of 4-bit dual scan display, the number of valid VD data lines should be 4 and in case of 8-bit single scan display mode, the number of valid VD data lines should be 8.

LINEVAL = (Vertical display size) -1: In case of single scan display type

LINEVAL = (Vertical display size / 2) -1: In case of dual scan display type

The rate of VCLK signal can be controlled by the CLKVAL field in the LCDCON1 register. The Table 15-1 defines the relationship of VCLK and CLKVAL. The minimum value of CLKVAL is 2.

VCLK(Hz)=HCLK/(CLKVAL x 2)

The frame rate is the VFRAM signal frequency. The frame rate is closely related to the field of WLH[1:0](VLINE pulse width) WDLY[1:0](the delay width of VCLK after VLINE pulse), HOZVAL, LINEBLANK, and LINEVAL in LCDCON1 and LCDCON2/3/4 registers as well as VCLK and HCLK. Most LCD drivers need their own adequate frame rate. The frame rate is calculated as follows;

frame_rate(Hz) = 1 / [{ (1/VCLK) x (HOZVAL+1)+(1/HCLK) x (**A**+**B**+(LINEBLANK x 8)) } x (LINEVAL+1)]

$$\boldsymbol{A} = 2^{(4+WLH)},\ \boldsymbol{B} = 2^{(4+WDLY)}$$

Table 15-1. Relation between VCLK and CLKVAL(STN, HCLK=60MHz)

CLKVAL	60MHz/X	VCLK
2	60 MHz/4	15.0 MHz
3	60 MHz/6	10.0 MHz
:	:	:
1023	60 MHz/2046	29.3 kHz

VIDEO OPERATION

The LCD controller within S3C2410X01 supports 8-bit color mode(256 color mode), 12-bit color mode(4096 color mode), 4 level gray scale mode, 16 level gray scale mode as well as the monochrome mode. When the gray or color mode is needed, the implementation of the shades of gray level or color should be followed by time-based dithering algorithm and FRC(Frame Rate Control) method can be used to implement the shades of gray or color from which selection can be made by using a programmable lockup table, which will be explained later. The monochrome mode bypasses these modules(FRC and lookup table) and basically serializes the data in FIFOH (and FIFOL if a dual scan display type is used) into 4-bit (or 8-bit if a 4-bit dual scan or 8-bit single scan display type is used) streams by shifting the video data to the LCD driver.

The following sections describe the operation on gray mode and color mode in terms of the lookup table and FRC.

Lookup Table

The S3C2410X01 can support the lookup table for various selection of color or gray level mapping. This kind of selection gives users flexibility. The lookup table is the palette which allows the selection on the level of color or gray(Selection on 4-gray levels among 16 gray levels in case of 4 gray mode, selection on 8 red levels among 16 levels, 8 green levels among 16 levels and 4 blue levels among 16 levels in case of 256 color mode). In other words, users can select 4 gray levels among 16 gray levels by using the lookup table in the 4 gray level mode.The gray levels cannot be selected in the 16 gray level mode; all 16 gray levels must be chosen among the possible 16 gray levels. In case of 256 color mode, 3 bits are allocated for red, 3 bits for green and 2 bits for blue. The 256 colors mean that the colors are formed from the combination of 8 red, 8 green and 4 blue levels(8x8x4 = 256). In the color mode, the lookup table can be used for suitable selections. Eight red levels can be selected among 16 possible red levels, 8 green levels among 16 green levels, and 4 blue levels among 16 blue levels. In case of 4096 color mode, of course there is no selection as in the 256 color mode.

Gray Mode Operation

Two gray modes are supported by the LCD controller within the S3C2410X01: 2-bit per pixel gray (4 level gray scale) or 4-bit per pixel gray (16 level gray scale). The 2-bit per pixel gray mode uses a lookup table(BLUELUT), which allows selection on 4 gray levels among 16 possible gray levels. The 2-bit per pixel gray lookup table uses the BULEVAL[15:0] in BLUELUT(Blue Lookup Table) register as same as blue lookup table in color mode. The gray level 0 will be denoted by BLUEVAL[3:0] value. If BLUEVAL[3:0] is 9, level 0 will be represented by gray level 9 among 16 gray levels. If BLUEVAL[3:0] is 15, level 0 will be represented by gray level 15 among 16 gray levels, and so on. As same as the above, level 1 will also be denoted by BLUEVAL[7:4], the level 2 by BLUEVAL[11:8], and the level 3 by BLUEVAL[15:12]. These four groups among BLUEVAL[15:0] will represent level 0, level 1, level 2, and level 3. In 16 gray levels, of course there is no selection as in the 16 gray levels.

256 Level Color Mode Operation

The LCD controller in S3C2410X01can support an 8-bit per pixel 256 color display mode. The color display mode can generate 256 levels of color using the dithering algorithm and FRC. The 8-bit per pixel are encoded into 3-bits for red, 3-bits for green, and 2-bits for blue. The color display mode uses separate lookup tables for red, green, and blue. Each lookup table uses the REDVAL[31:0] of REDLUT register, GREENVAL[31:0] of GREENLUT register, and BLUEVAL[15:0] of BLUELUT register as the programmable lookup table entries.

Similarly with the gray level display, 8 group or field of 4 bits in the REDLUR register, i.e., REDVAL[31:28], REDLUT[27:24], REDLUT[23:20], REDLUT[19:16], REDLUT[15:12], REDLUT[11:8], REDLUT[7:4], and REDLUT[3:0], are assigned to each red level. The possible combination of 4 bits(each field) is 16, and each red level should be assigned to one level among possible 16 cases. In other words, the user can select the suitable red level by using this type of lookup table. For green color, the GREENVAL[31:0] of the GREENLUT register is assigned as the lookup table, as was done in the case of red color. Similarly, the BLUEVAL[15:0] of the BLUELUT register is also assigned as a lookup table. For blue color, 2 bits are allocated for 4 blue levels, different from the 8 red or green levels.

4096 Level Color Mode Operation

The LCD controller in S3C2410X01can supports an 12-bit per pixel 4096 color display mode. The color display mode can generate 4096 levels of color using the dithering algorithm and FRC. The 12-bit per pixel are encoded into 4-bits for red, 4-bits for green, and 4-bits for blue. The 4096 color display mode does not use lookup tables.

DITHERING AND FRC (FRAME RATE CONTROL)

For STN LCD displays(except monochrome), video data must be processed by a dithering algorithm. The DITHFRC block has two functions, such as a Time-based Dithering Algorithm for reducing flicker and FRC(Frame Rate Control) for displaying gray and color level on the STN panel. The main principle of gray and color level display on the STN panel based on FRC is described. For example, to display the third gray (3/16) level from a total of 16 levels, the 3 times pixel should be on and 13 times pixel off. In other words, 3 frames should be selected among the 16 frames, of which 3 frames should have a pixel-on on a specific pixel while the remaining 13 frames should have a pixel-off on a specific pixel. These 16 frames should be displayed periodically. This is basic principle on how to display the gray level on the screen, so-called gray level display by FRC(Frame Rate Control). The actual example is shown in Table 15-2. To represent the 14th gray level in the table, we should have a 6/7 duty cycle, which mean that there are 6 times pixel-on and one time pixel-off. The other cases for all gray levels are also shown in Table 15-2.

In the STN LCD display, we should be reminded of one item, i.e., Flicker Noise due to the simultaneous pixel-on and -off on adjacent frames. For example, if all pixels on first frame are turned on and all pixels on next frame are turned off, the Flicker Noise will be maximized. To reduce the Flicker Noise on the screen, the average probability of pixel-on and -off between frames should be as same as possible. In order to realize this, the Time-based Dithering Algorithm, which varies the pattern of adjacent pixels on every frame, should be used. This is explained in detail. For the 16 gray level, FRC should have the following relationship between gray level and FRC. The 15th gray level should always have pixel-on, and the 14th gray level should have 6 times pixel-on and one times pixel-off, and the 13th gray level should have 4 times pixel-on and one times pixel-off, ,,,,,,,, , and the 0th gray level should always have pixel-off as shown in Table 15-2.

Table 15-2. Dither Duty Cycle Examples

Pre-dithered Data (gray level number)	Duty Cycle	Pre-dithered Data (gray level number)	Duty Cycle
15	1	7	1/2
14	6/7	6	3/7
13	4/5	5	2/5
12	3/4	4	1/3
11	5/7	3	1/4
10	2/3	2	1/5
9	3/5	1	1/7
8	4/7	0	0

Display Types

The LCD controller supports 3 types of LCD drivers: 4-bit dual scan, 4-bit single scan, and 8-bit single scan display mode. Figure 15-3 shows these 3 different display types for monochrome displays, and Figure 15-4 show these 3 different display types for color displays.

4-bit Dual Scan Display Type

A 4-bit dual scan display uses 8 parallel data lines to shift data to both the upper and lower halves of the display at the same time. The 4 bits of data in the 8 parallel data lines are shifted to the upper half and 4 bits of data is shifted to the lower half, as shown in Figure 15-3. The end of frame is reached when each half of the display has been shifted and transferred. The 8 pins (VD[7:0]) for the LCD output from the LCD controller can be directly connected to the LCD driver.

4-bit Single Scan Display Type

A 4-bit single scan display uses 4 parallel data lines to shift data to successive single horizontal lines of the display at a time, until the entire frame has been shifted and transferred. The 4 pins(VD[3:0]) for the LCD output from the LCD controller can be directly connected to the LCD driver, and the 4 pins(VD[7:4]) for the LCD output are not used.

8-bit Single Scan Display Type

An 8-bit single scan display uses 8 parallel data lines to shift data to successive single horizontal lines of the display at a time, until the entire frame has been shifted and transferred. The 8 pins (VD[7:0]) for the LCD output from the LCD controller can be directly connected to the LCD driver.

256 Color Displays

Color displays require 3 bits (Red, Green, Blue) of image data per pixel, resulting in a horizontal shift register of length 3 times the number of pixels per horizontal line. This RGB is shifted to the LCD driver as consecutive bits via the parallel data lines. Figure 15-4 shows the RGB and order of the pixels in the parallel data lines for the 3 types of color displays.

4096 Color Displays

Color displays require 3 bits (Red, Green, Blue) of image data per pixel, resulting in a horizontal shift register of length 3 times the number of pixels per horizontal line. This RGB is shifted to the LCD driver as consecutive bits via the parallel data lines. This RGB order is determined by the sequence of video data in video buffers.

MEMORY DATA FORMAT (STN, BSWP=0)

Mono 4-bit Dual Scan Display:

Video Buffer Memory:

Address	Data
0000H	A[31:0]
0004H	B[31:0]
•	
•	
•	
1000H	L[31:0]
1004H	M[31:0]
•	
•	
•	

LCD Panel

A[31] A[30] ..... A[0] B[31] B[30] ..... B[0] .....

L[31] L[30] ..... L[0] M[31] M[30] ..... M[0] .....

Mono 4-bit Single Scan Display & 8-bit Single Scan Display:

Video Buffer Memory:

Address	Data
0000H	A[31:0]
0004H	B[31:0]
0008H	C[31:0]
•	
•	
•	

LCD Panel

A[31] A[30] A[29] ..... A[0] B[31] B[30] ..... B[0] C[31] ..... C[0] ....

MEMORY DATA FORMAT (STN, BSWP=0) (CONTINUED)

In 4-level gray mode, 2 bits of video data correspond to 1 pixel.

In 16-level gray mode, 4 bits of video data correspond to 1 pixel.

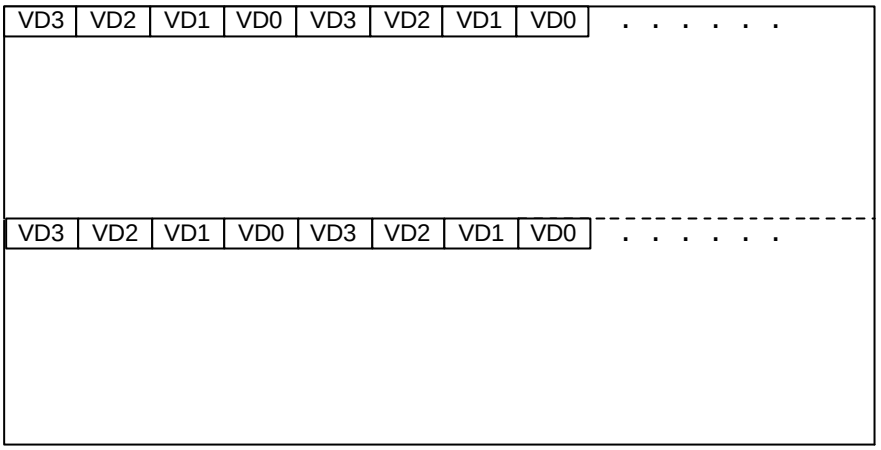
In 256 level color mode, 8 bits (3 bits of red, 3 bits of green, 2 bits of blue) of video data correspond to 1 pixel. The color data format in a byte is as follows;

Bit [7:5]	Bit [4:2]	Bit[1:0]
Red	Green	Blue

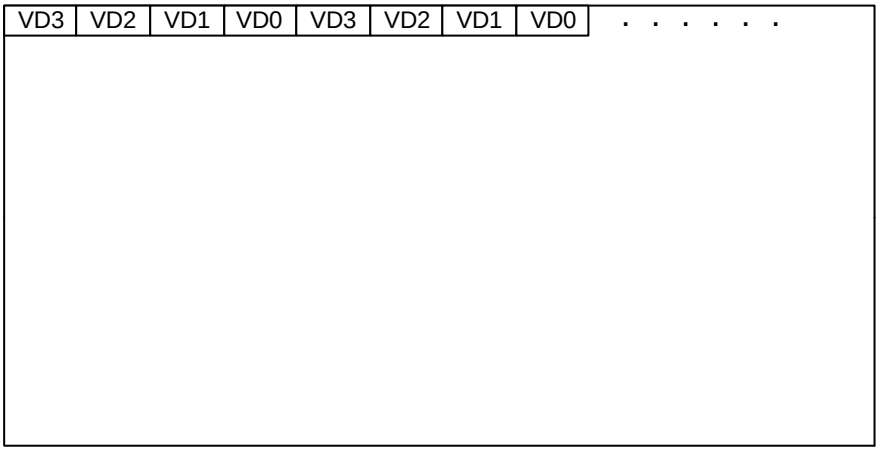
In 4096 level color mode, 12 bits (4 bits of red, 4 bits of green, 4 bits of blue) of video data correspond to 1 pixel. The color data format in words is as follows; (Video data must be reside at 3 word boundaries (8 pixel), as follows)

RGB order

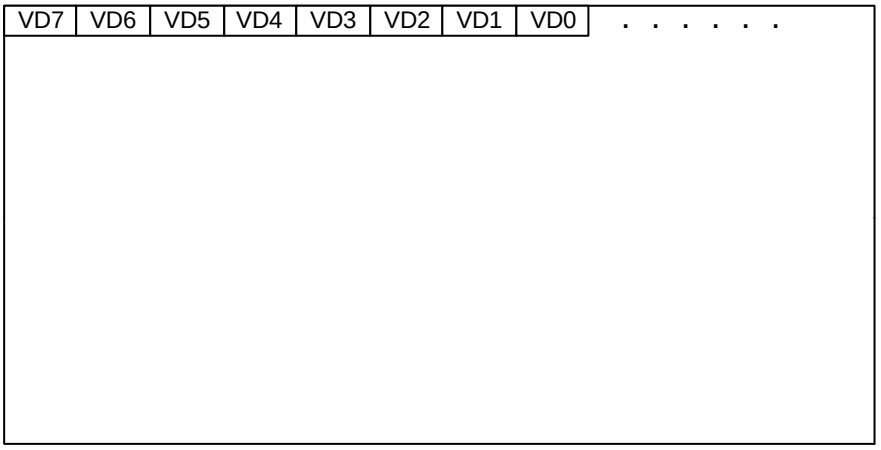
DATA	[31:28]	[27:24]	[23:20]	[19:16]	[15:12]	[11:8]	[7:4]	[3:0]
Word #1	Red(1)	Green(1)	Blue(1)	Red(2)	Green(2)	Blue(2)	Red(3)	Green(3)
Word #2	Blue(3)	Red(4)	Green(4)	Blue(4)	Red(5)	Green(5)	Blue(5)	Red(6)
Word #3	Green(6)	Blue(6)	Red(7)	Green(7)	Blue(7)	Red(8)	Green(8)	Blue(8)



4-bit Dual Scan Display

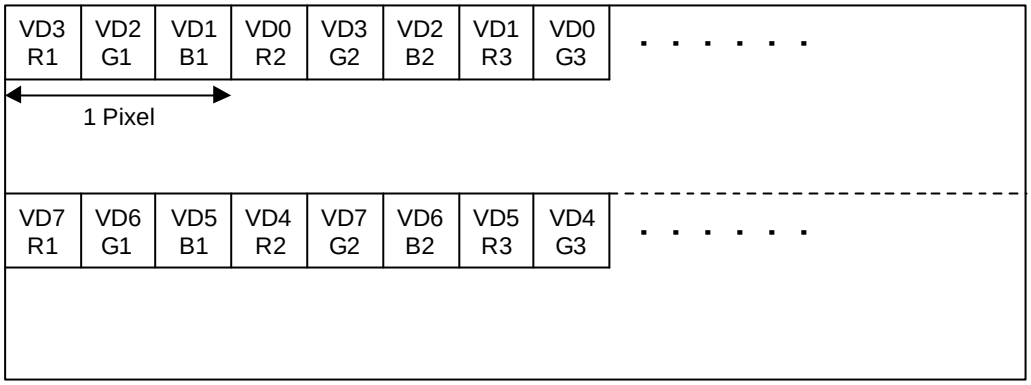


4-bit Single Scan Display

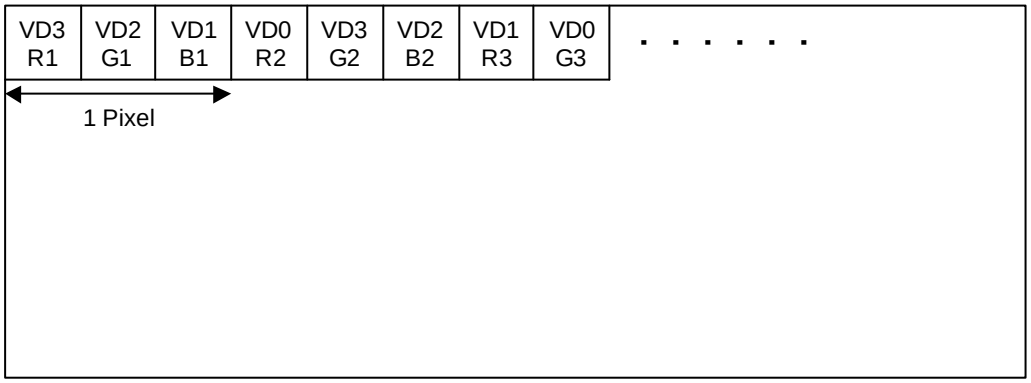


8-bit Single Scan Display

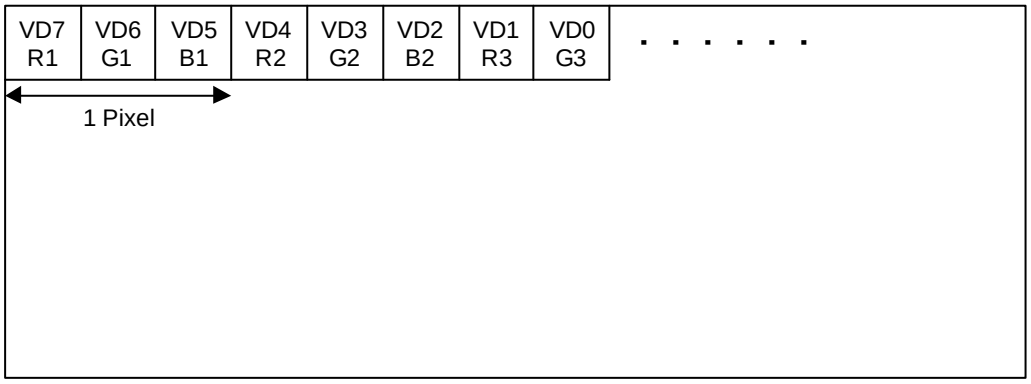
Figure 15-2. Monochrome Display Types (STN)



4-bit Dual Scan Display



4-bit Single Scan Display



8-bit Single Scan Display

Figure 15-3. Color Display Types (STN)

Timing Requirements

Image data should be transferred from the memory to the LCD driver using the VD[7:0] signal. VCLK signal is used to clock the data into the LCD driver's shift register. After each horizontal line of data has been shifted into the LCD driver's shift register, the VLINE signal is asserted to display the line on the panel.

The VM signal provides an AC signal for the display. It is used by the LCD to alternate the polarity of the row and column voltages, used to turn the pixels on and off, because the LCD plasma tends to deteriorate whenever subjected to a DC voltage. It can be configured to toggle on every frame or to toggle every programmable number of VLINE signals.

Figure 15-4 shows the timing requirements for the LCD driver interface.

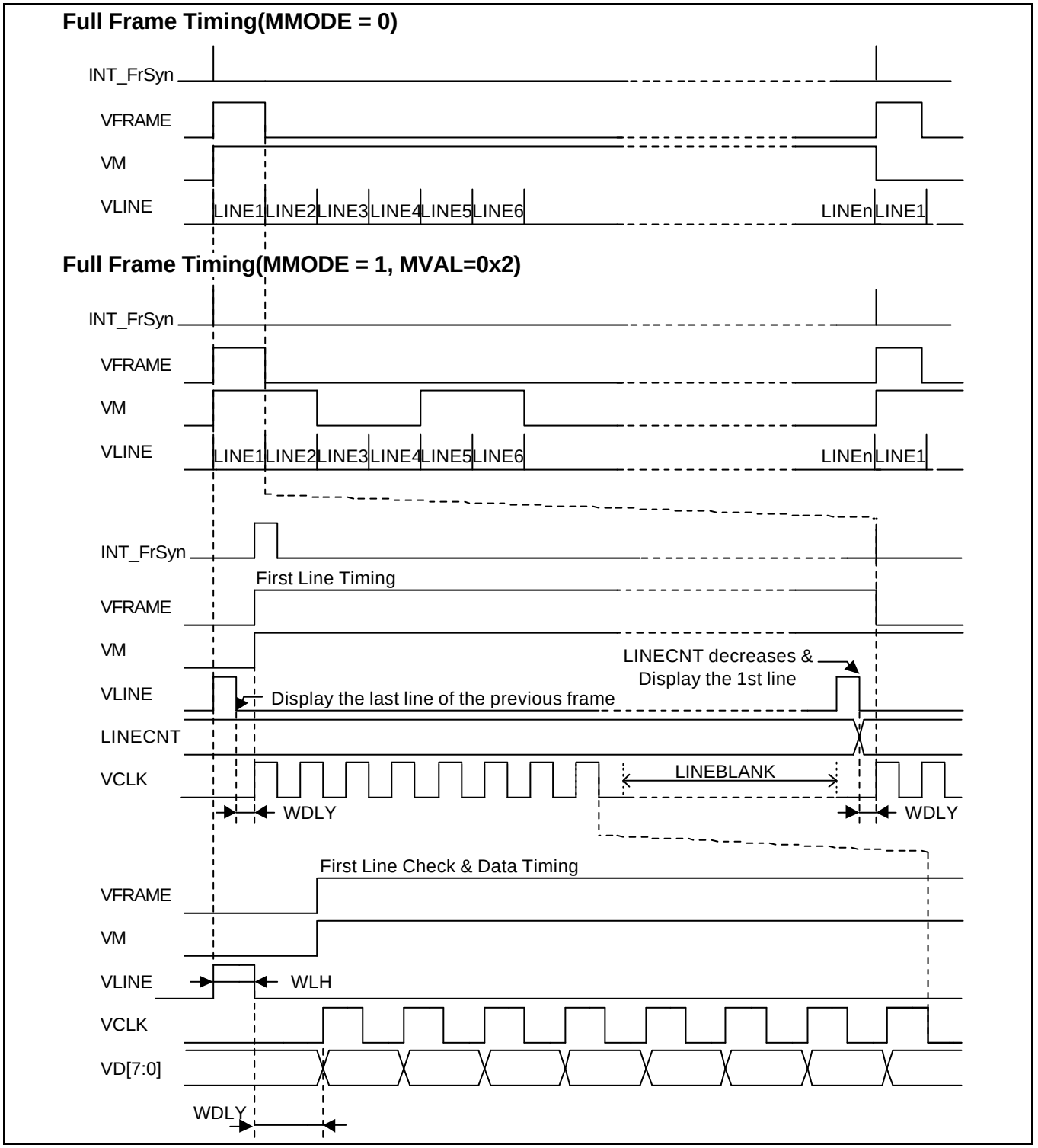


Figure 15-4. 8-bit Single Scan Display Type STN LCD Timing

TFT LCD CONTROLLER OPERATION

The TIMEGEN generates the control signals for LCD driver such as, VSYNC, HSYNC, VCLK, VDEN, and LEND signal. These control signals are highly related with the configuration on the LCDCON1/2/3/4/5 registers in the REGBANK. Base on these programmable configuration on the LCD control registers in REGBANK, the TIMEGEN can generate the programmable control signals suitable for the support of many different types of LCD drivers.

The VSYNC signal is asserted to cause the LCD's line pointer to start over at the top of the display.

The VSYNC and HSYNC pulse generation is controlled by the configuration of both the HOZVAL field and the LINEVAL field in the LCDCON2/3 registers. The HOZVAL and LINEVAL can be determined by the size of the LCD panel according to the following equations:

HOZVAL = (Horizontal display size) -1

LINEVAL = (Vertical display size) -1

The rate of VCLK signal can be controlled by the CLKVAL field in the LCDCON1 register. The table below defines the relationship of VCLK and CLKVAL. The minimum value of CLKVAL is 0.

VCLK(Hz)=HCLK/[(CLKVAL+1)x2]

The frame rate is VSYNC signal frequency. The frame rate is related with the field of VSYNC, VBPD, VFPD, LINEVAL, HSYNC, HBPD, HFPD, HOZVAL, CLKVAL in LCDCON1 and LCDCON2/3/4 registers. Most LCD driver need their own adequate frame rate. The frame rate is calculated as follows;

Frame Rate = 1/ [{ (VSPW+1) + (VBPD+1) + (LIINEVAL + 1) + (VFPD+1) } x {(HSPW+1) + (HBPD +1) + (HFPD+1) + (HOZVAL + 1) } x { 2 x (CLKVAL+1) / (HCLK) }]

Table 15-3. Relation between VCLK and CLKVAL(TFT, HCLK=60MHz)

CLKVAL	60MHz/X	VCLK
1	60 MHz/4	15.0 MHz
2	60 MHz/6	10.0 MHz
:	:	:
1023	60 MHz/2048	30.0 kHz

VIDEO OPERATION

The TFT LCD controller within S3C2410X01 supports 1, 2, 4 or 8 bpp(bit per pixel) palettized color displays and 16 or 24 bpp non-palettized true-color displays.

256 Color Palette

The S3C2410X01 can support the 256 color palette for various selection of color mapping. This kind of selection can give the flexibility to users

MEMORY DATA FORMAT (TFT)

In this chapter, we will show you some examples of each display mode.

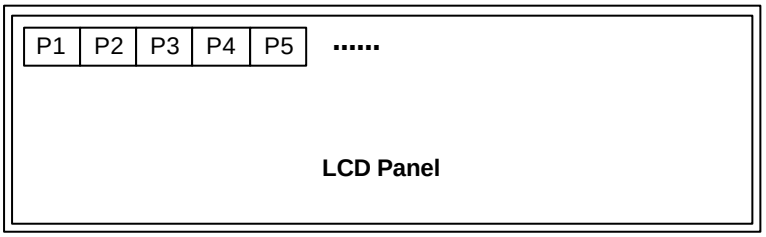
24BPP Display

(BSWP = 0, HWSWP = 0, BPP24BL = 0)

	D[31:24]	D[23:0]
000H	Dummy Bit	P1
004H	Dummy Bit	P2
008H	Dummy Bit	P3
...		

(BSWP = 0, HWSWP = 0, BPP24BL = 1)

	D[31:8]	D[7:0]
000H	P1	Dummy Bit
004H	P2	Dummy Bit
008H	P3	Dummy Bit
...		



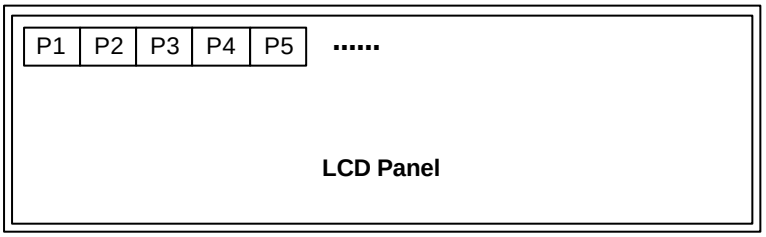
16BPP Display

(BSWP = 0, HWSWP = 0)

	D[31:16]	D[15:0]
000H	P1	P2
004H	P3	P4
008H	P5	P6
...		

(BSWP = 0, HWSWP = 1)

	D[31:16]	D[15:0]
000H	P2	P1
004H	P4	P3
008H	P6	P5
...		



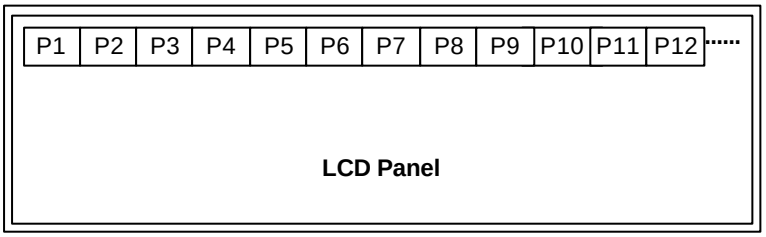
8BPP Display

(BSWP = 0, HWSWP = 0)

	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P1	P2	P3	P4
004H	P5	P6	P7	P8
008H	P9	P10	P11	P12
...				

(BSWP = 1, HWSWP = 0)

	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P4	P3	P2	P1
004H	P8	P7	P6	P5
008H	P12	P11	P10	P9
...				



4BPP Display

(BSWP = 0, HWSWP = 0)

	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
000H	P1	P2	P3	P4	P5	P6	P7	P8
004H	P9	P10	P11	P12	P13	P14	P15	P16
008H	P17	P18	P19	P20	P21	P22	P23	P24
…								

(BSWP = 1, HWSWP = 0)

	D[31:28]	D[27:24]	D[23:20]	D[19:16]	D[15:12]	D[11:8]	D[7:4]	D[3:0]
000H	P7	P8	P5	P6	P3	P4	P1	P2
004H	P15	P16	P13	P14	P11	P12	P9	P10
008H	P23	P24	P21	P22	P19	P20	P17	P18
…								

2BPP Display

(BSWP = 0, HWSWP = 0)

D	[31:30]	[29:28]	[27:26]	[25:24]	[23:22]	[21:20]	[19:18]	[17:16]
000H	P1	P2	P3	P4	P5	P6	P7	P8
004H	P17	P18	P19	P20	P21	P22	P23	P24
008H	P33	P34	P35	P36	P37	P38	P39	P40
…								

D	[15:14]	[13:12]	[11:10]	[9:8]	[7:6]	[5:4]	[3:2]	[1:0]
000H	P9	P10	P11	P12	P13	P14	P15	P16
004H	P25	P26	P27	P28	P29	P30	P31	P32
008H	P41	P42	P43	P44	P45	P46	P47	P48
…								

256 PALETTE USAGE(TFT)

Palette Configuration and Format Control

S3C2410X01 provides 256 color palette for TFT LCD Control.
The user can select 256 colors from the 64K colors through these two formats.
256 color palette consist of the 256(depth) × 16-bit SPSRAM. Palette supports 5:6:5(R:G:B) format and 5:5:5:1(R:G:B:I) format.
When the user use 5:5:5:1 format, the intensity data(I) is used as a common LSB bit of each RGB data. So, 5:5:5:1 format is same as R(5+I):G(5+I):B(5+I) format.
For example of 5:5:5:1 format, write palette like Table 15-5 and then connect VD pin to TFT LCD panel(R(5+I)=VD[23:19]+VD[18], VD[10] or VD[2], G(5+I)=VD[15:11]+ VD[18], VD[10] or VD[2], B(5+I)=VD[7:3]+ VD[18], VD[10] or VD[2].) At the last, Set FRM565 of LCDCON5 register to 0.

Table 15-4. 5:6:5 Format

INDEX\Bit Pos.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
00H	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	[1)]0X4D000400
01H	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0X4D000404
.....																	.....
FFH	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0X4D0007FC
Number of VD	23	22	21	20	19	15	14	13	12	11	10	7	6	5	4	3	

Table 15-5. 5:5:5:1 Format

INDEX\Bit Pos.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
00H	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	I	0X4D000400
01H	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	I	0X4D000404
.....																	.....
FFH	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	I	0X4D0007FC
Number of VD	23	22	21	20	19	15	14	13	12	11	7	6	5	4	3	[2)]	

NOTES:
1. 0x4D000400 is Palette start address.
2. VD18, VD10 and VD2 has same output value, I.
3. DATA[31:16] is invalid.

Palette Read/Write

When the user going to do Read/Write operation on the palette, VSTATUS of LCDCON5 register must be checked. Because Read/Write operation is prohibited during the ACTIVE status of VSTATUS.

Temporary Palette Configuration

S3C2410X01 supports that the user can fill a frame with one color without complex modification to fill the one color to the frame buffer or palette. The one colored frame can be displayed by the writing a value of the color which is displayed on LCD panel to TPALVAL of TPAL register and enable TPALEN.

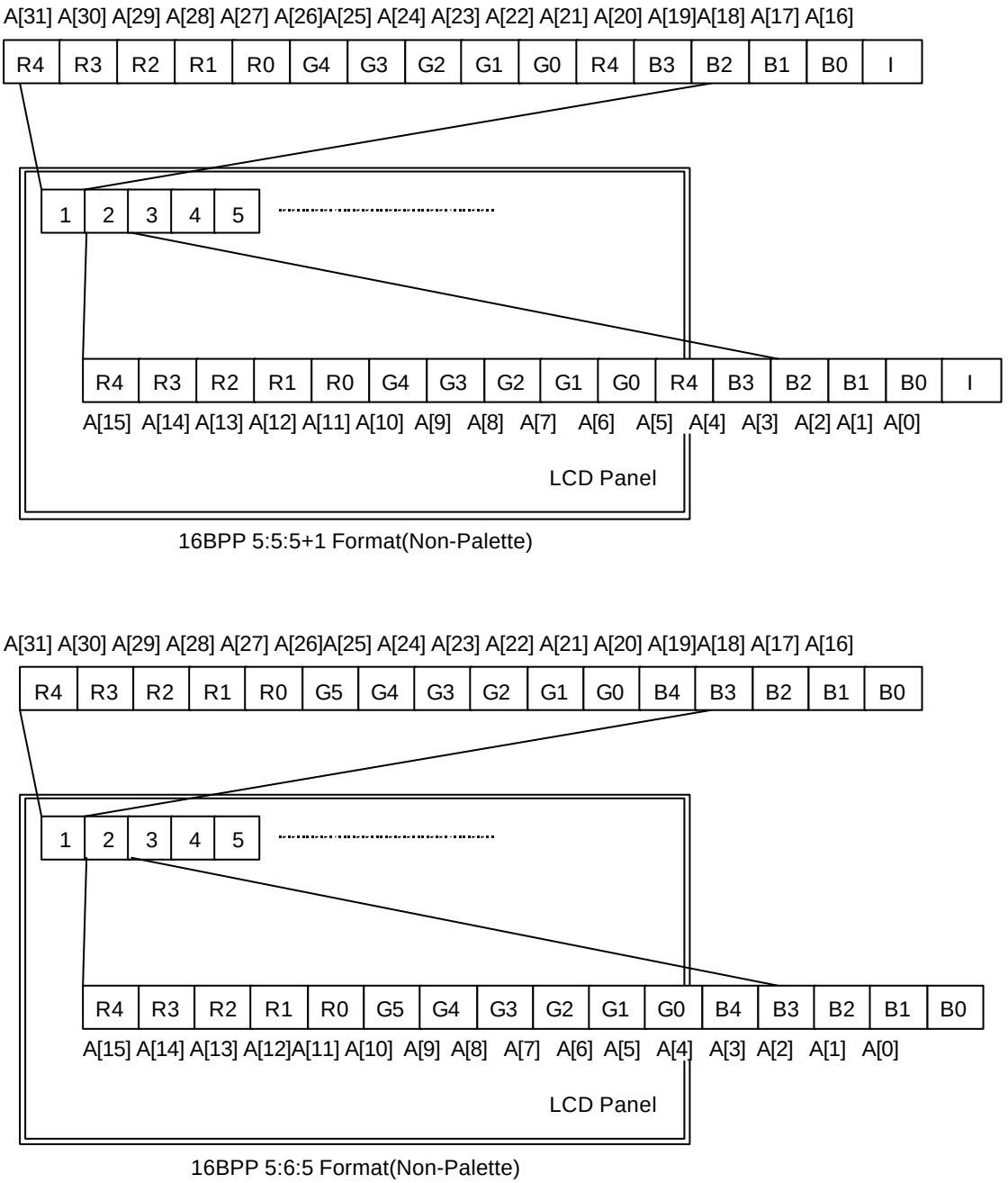


Figure 15-5. 16BPP Display Types (TFT)

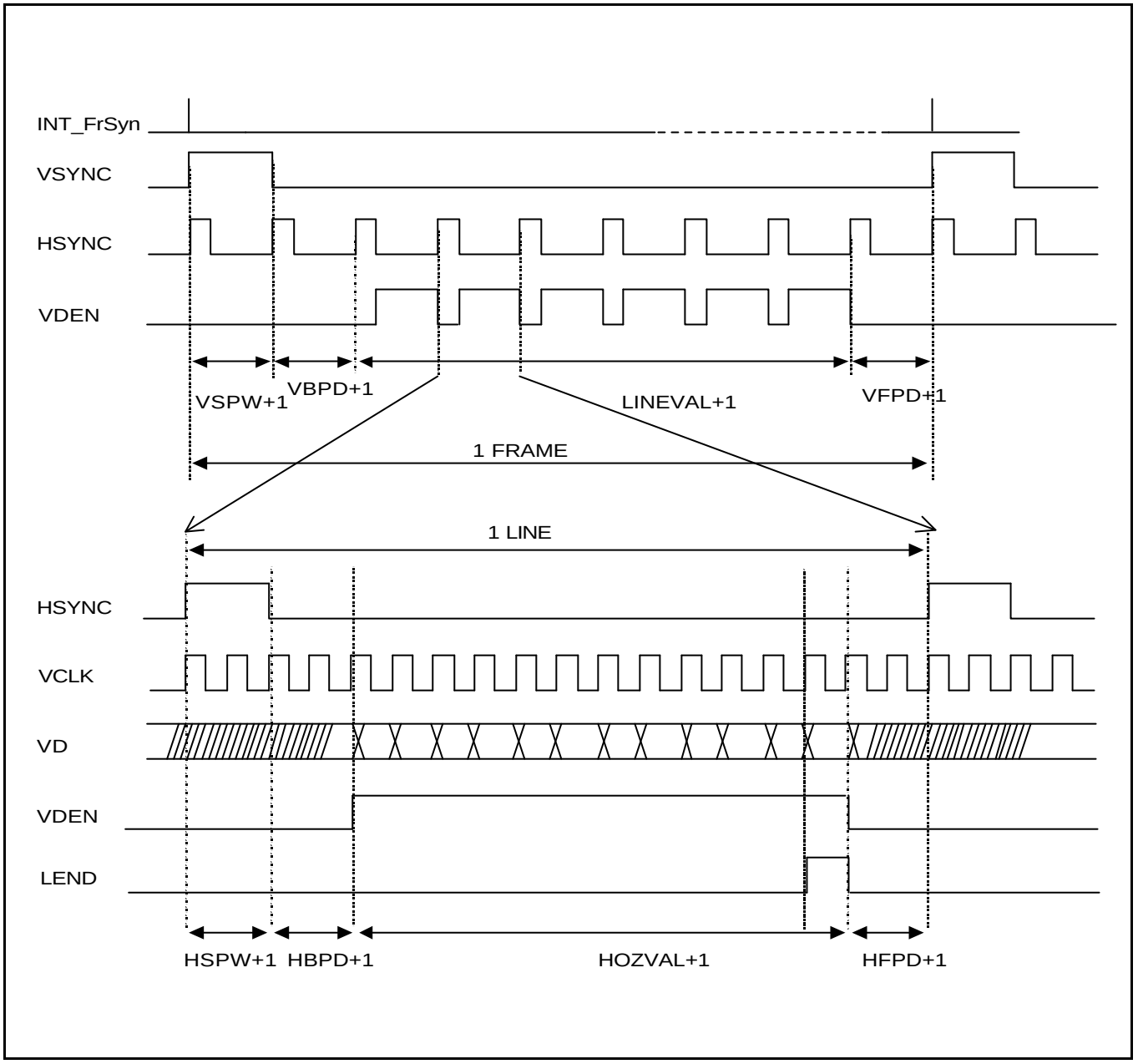


Figure 15-6. TFT LCD Timing Example

SAMSUNG TFT LCD PANEL(3.5² PORTRAIT / 256K COLOR /REFLECTIVE A-SI TFT LCD)

S3C2410X01 supports SEC TFT LCD panel(SAMSUNG 3.5″ Portrait / 256K Color /Reflective a-Si TFT LCD).

LTS350Q1-PD1 : TFT LCD panel with touch panel and front light unit
LTS350Q1-PD2 : TFT LCD panel only

S3C2410X01 provides timing signals as follows to use LTS350Q1-PD1 and PD2,;

STH : Horizontal Start Pulse
TP : Source Driver Data Load Pulse
INV : Digital Data Inversion
LCD_HCLK : Horizontal Sampling Clock
CPV : Vertical Shift Clock
STV : Vertical Start Pulse
OE : Gate On Enable
REV : Inversion Signal
REVB : Inversion Signal

So, LTS350Q1-PD1 and PD2 can be connected with S3C2410X01 without using the additional timing control logic. But user should apply Vcom generator circuit, various voltages, INV signal and Gray scale voltage generator circuit additionally, which are recommended by PRODUCT INFORMATION(SPEC) of LTS350Q1-PD1 and PD2.
Detail timing diagram is also described in PRODUCT INFORMATION(SPEC) of LTS350Q1-PD1 and PD2.

Please, refer to the documentation (PRODUCT INFORMATION of LTS350Q1-PD1 and PD2), which is prepared by AMLCD Technical customer center of Samsung Electronics Co.,LTD..

CAUTION :
S3C2410X01 has HCLK. It means the clock of AHB bus.
Accidentally, SEC TFT LCD panel (LTS350Q1-PD1 and PD2) has HCLK(Horizontal Sampling Clock) also.
These two HCLK can cause a confusion. So, we' ll distinguish these signals as follows in this chapter;

HCLK of S3C2410X01 is HCLK.
HCLK of SEC TFT LCD panel (LTS350Q1-PD1 and PD2) is changed to LCD_HCLK.

VIRTUAL DISPLAY (TFT/STN)

The S3C2410X01 supports hardware horizontal or vertical scrolling. If the screen is scrolled, the fields of LCDBASEU and LCDBASEL in LCDSADDR1/2 registers need to be changed(refer to Figure 15-8) but not the values of PAGEWIDTH and OFFSIZE.
The size of video buffer in which the image is stored should be larger than LCD panel screen size.

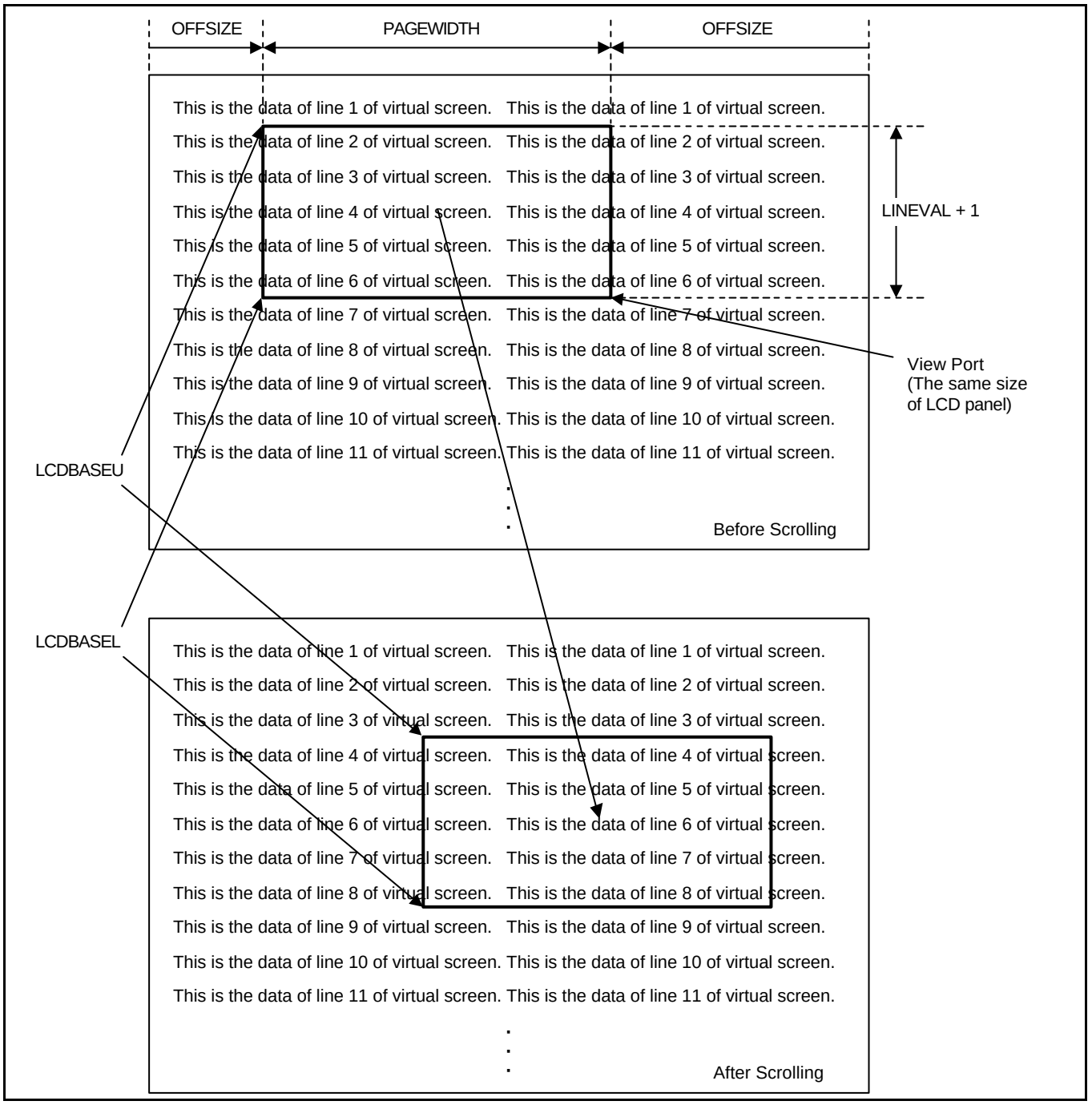


Figure 15-7. Example of Scrolling in Virtual Display (Single Scan)

LCD POWER ENABLE (STN/TFT)

S3C2410X01 provides PWREN function. When PWREN is set as enabling PWREN signal, then the output value of LCD_PWREN pin is controlled by ENVID. In other words, If LCD_PWREN pin is connected to power pin of LCD panel, then the power of LCD panel is controlled by the setting of ENVID automatically.
S3C2410X01 also supports INVPWREN bit to invert polarity of PWREN signal.

This function is available only when LCD panel has its own power on/off control port and that port is connected to LCD_PWREN pin.

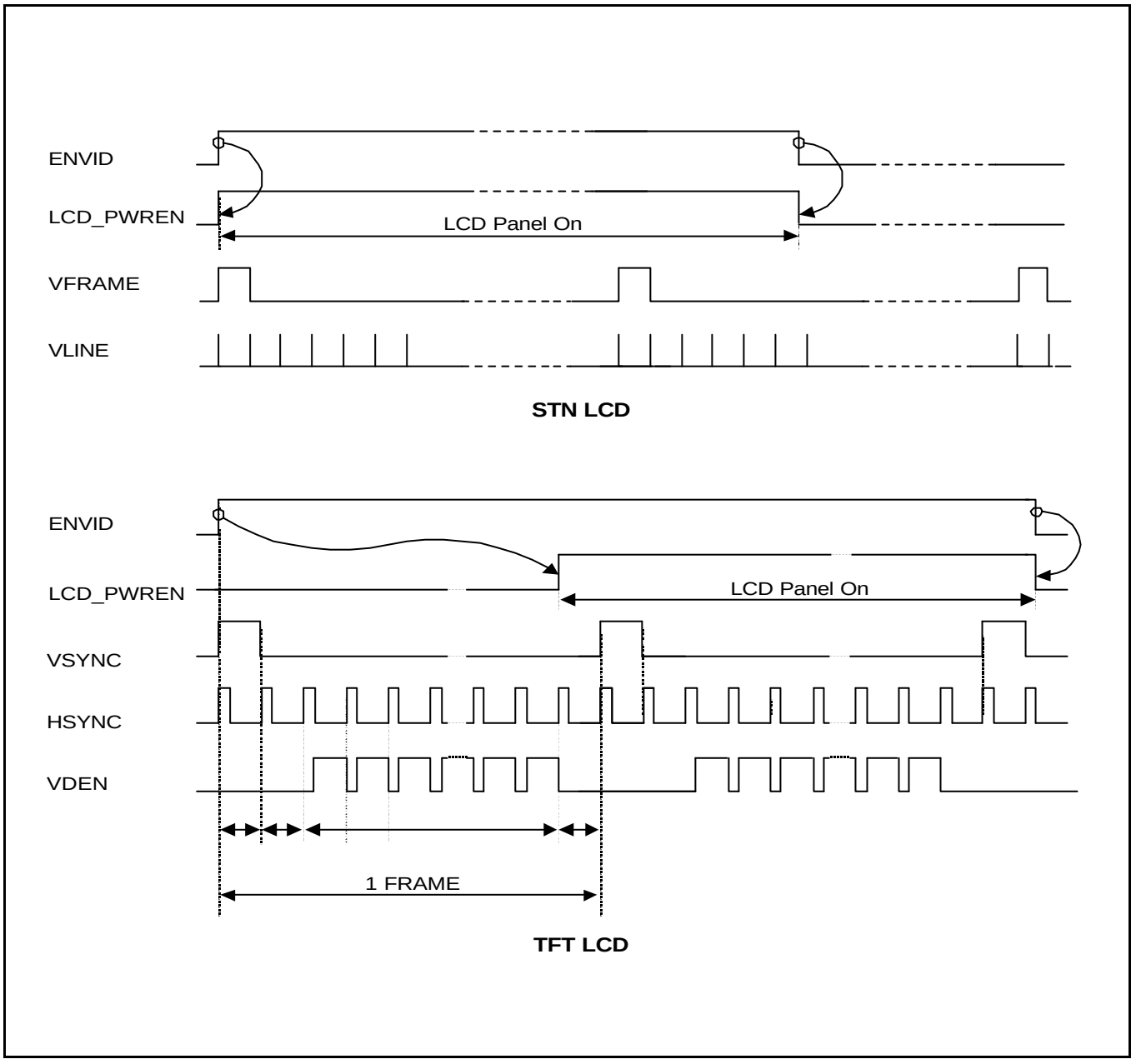


Figure 15-8. Example of PWREN function (PWREN=1, INVPWREN=0)

12/20/2001

LCD CONTROLLER SPECIAL REGISTERS

LCD Control 1 Register

Register	Address	R/W	Description	Reset Value
LCDCON1	0X4D000000	R/W	LCD control 1 register	0x00000000

LCDCON1	Bit	Description	Initial State
LINECNT (read only)	[27:18]	These bits provide the status of the line counter. Down count from LINEVAL to 0	0000000000
CLKVAL	[17:8]	These bits determine the rates of VCLK and CLKVAL[9:0]. **STN**: VCLK = HCLK / (CLKVAL x 2) (CLKVAL ≥ 2) **TFT**: VCLK = HCLK / [(CLKVAL+1) x 2] (CLKVAL ≥ 0)	0000000000
MMODE	[7]	This bit determines the toggle rate of the VM. 0 = Each Frame, 1 = The rate defined by the MVAL	0
PNRMODE	[6:5]	These bits select the display mode. 00 = 4-bit dual scan display mode(STN) 01 = 4-bit single scan display mode(STN) 10 = 8-bit single scan display mode(STN) 11 = TFT LCD panel	00
BPPMODE	[4:1]	These bits select the BPP (Bits Per Pixel) mode. 0000 = 1 bpp for STN, Monochrome mode3 0001 = 2 bpp for STN, 4-level gray mode 0010 = 4 bpp for STN, 16-level gray mode 0011 = 8 bpp for STN, color mode 0100 = 12 bpp for STN, color mode 1000 = 1 bpp for TFT 1001 = 2 bpp for TFT 1010 = 4 bpp for TFT 1011 = 8 bpp for TFT 1100 = 16 bpp for TFT 1101 = 24 bpp for TFT	0000
ENVID	[0]	LCD video output and the logic enable/disable. 0 = Disable the video output and the LCD control signal. 1 = Enable the video output and the LCD control signal.	0

LCD Control 2 Register

Register	Address	R/W	Description	Reset Value
LCDCON2	0X4D000004	R/W	LCD control 2 register	0x00000000

LCDCON2	Bit	Description	Initial State
VBPD	[31:24]	**TFT**: Vertical back porch is the number of inactive lines at the start of a frame, after vertical synchronization period. **STN**: These bits should be set to zero on STN LCD.	0x00
LINEVAL	[23:14]	**TFT/STN**: These bits determine the vertical size of LCD panel.	0000000000
VFPD	[13:6]	**TFT**: Vertical front porch is the number of inactive lines at the end of a frame, before vertical synchronization period. **STN**: These bits should be set to zero on STN LCD.	00000000
VSPW	[5:0]	**TFT**: Vertical sync pulse width determines the VSYNC pulse's high level width by counting the number of inactive lines. **STN**: These bits should be set to zero on STN LCD.	000000

LCD Control 3 Register

Register	Address	R/W	Description	Reset Value
LCDCON3	0X4D000008	R/W	LCD control 3 register	0x00000000

LCDCON3	Bit	Description	initial state
HBPD (TFT)	[25:19]	**TFT**: Horizontal back porch is the number of VCLK periods between the falling edge of HSYNC and the start of active data.	0000000
WDLY (STN)		**STN**: WDLY[1:0] bits determine the delay between VLINE and VCLK by counting the number of the HCLK. WDLY[7:2] are reserved. 00 = 16 HCLK, 01 = 32 HCLK, 10 = 64 HCLK, 11 = 128 HCLK	
HOZVAL	[18:8]	**TFT/STN**: These bits determine the horizontal size of LCD panel. HOZVAL has to be determined to meet the condition that total bytes of 1 line are 2n bytes. If the x size of LCD is 120 dot in mono mode, x=120 can not be supported because 1 line is consist of 15 bytes. Instead, x=128 in mono mode can be supported because 1 line is consisted of 16 bytes (2n). LCD panel driver will discard the additional 8 dot.	00000000000
HFPD (TFT)	[7:0]	**TFT**: Horizontal front porch is the number of VCLK periods between the end of active data and the rising edge of HSYNC.	0X00
LINEBLANK (STN)		**STN**: These bits indicate the blank time in one horizontal line duration time. These bits adjust the rate of the VLINE finely. The unit of LINEBLANK is HCLK X 8. Ex) If the value of LINEBLANK is 10, the blank time is inserted to VCLK during 80 HCLK.	

LCD Control 4 Register

Register	Address	R/W	Description	Reset Value
LCDCON4	0X4D00000C	R/W	LCD control 4 register	0x00000000

LCDCON4	Bit	Description	initial state
MVAL	[15:8]	**STN**: These bit define the rate at which the VM signal will toggle if the MMODE bit is set logic '1'.	0X00
HSPW(TFT)	[7:0]	**TFT**: Horizontal sync pulse width determines the HSYNC pulse's high level width by counting the number of the VCLK.	0X00
WLH(STN)		**STN**: WLH[1:0] bits determine the VLINE pulse's high level width by counting the number of the HCLK. WLH[7:2] are reserved. 00 = 16 HCLK, 01 = 32 HCLK, 10 = 64 HCLK, 11 = 128 HCLK	

LCD Control 5 Register

Register	Address	R/W	Description	Reset Value
LCDCON5	0X4D000010	R/W	LCD control 5 register	0x00000000

LCDCON5	Bit	Description	initial state
VSTATUS	[20:19]	**TFT**: Vertical Status (Read only) 00 = VSYNC 01 = BACK Porch 10 = ACTIVE 11 = FRONT Porch	00
HSTATUS	[18:17]	**TFT**: Horizontal Status (Read only) 00 = HSYNC 01 = BACK Porch 10 = ACTIVE 11 = FRONT Porch	00
Reserved	[16:13]	This bit is reserved and the value should be ‘ 0’ .	0
BPP24BL	[12]	**TFT**: This bit determines the order of 24 bpp video memory. 0 = LSB valid 1 = MSB Valid	0
FRM565	[11]	**TFT**: This bit selects the format of 16 bpp output video data. 0 = 5:5:5:1 Format 1 = 5:6:5 Format	0
INVVCLK	[10]	**STN/TFT**: This bit controls the polarity of the VCLK active edge. 0 = The video data is fetched at VCLK falling edge 1 = The video data is fetched at VCLK rising edge	0
INVVLINE	[9]	**STN/TFT**: This bit indicates the VLINE/HSYNC pulse polarity. 0 = normal 1 = inverted	0
INVVFRAME	[8]	**STN/TFT**: This bit indicates the VFRAME/VSYNC pulse polarity. 0 = normal 1 = inverted	0
INVVD	[7]	**STN/TFT**: This bit indicates the VD (video data) pulse polarity. 0 = Normal 1 = VD is inverted.	0

LCD Control 5 Register (Continued)

LCDCON5	Bit	Description	initial state
INVVDEN	[6]	**TFT**: This bit indicates the VDEN signal polarity. 0 = normal 1 = inverted	0
INVPWREN	[5]	**STN/TFT**: This bit indicates the PWREN signal polarity. 0 = normal 1 = inverted	0
INVENDLINE	[4]	**TFT**: This bit indicates the LEND signal polarity. 0 = normal 1 = inverted	0
PWREN	[3]	**STN/TFT**: LCD_PWREN output signal enable/disable.. 0 = Disable PWREN signal 1 = Enable PWREN signal	0
ENLEND	[2]	**TFT**: LEND output signal enable/disable. 0 = Disable LEND signal 1 = Enable LEND signal	0
BSWP	[1]	**STN/TFT**: Byte swap control bit 0 = Swap Disable 1 = Swap Enable	0
HWSWP	[0]	**STN/TFT**: Half-Word swap control bit 0 = Swap Disable 1 = Swap Enable	0

FRAME BUFFER START ADDRESS 1 REGISTER

Register	Address	R/W	Description	Reset Value
LCDSADDR1	0X4D000014	R/W	**STN/TFT**: Frame buffer start address 1 register	0x00000000

LCDSADDR1	Bit	Description	Initial State
LCDBANK	[29:21]	These bits indicate A[30:22] of the bank location for the video buffer in the system memory. LCDBANK value can not be changed even when moving the view port. LCD frame buffer should be inside aligned 4MB region, which ensures that LCDBANK value will not be changed when moving the view port. So, using the malloc() function the care should be taken.	0x00
LCDBASEU	[20:0]	For dual-scan LCD: These bits indicate A[21:1] of the start address of the upper address counter, which is for the upper frame memory of dual scan LCD or the frame memory of single scan LCD. For single-scan LCD: These bits indicate A[21:1] of the start address of the LCD frame buffer.	0x000000

FRAME Buffer Start Address 2 Register

Register	Address	R/W	Description	Reset Value
LCDSADDR2	0X4D000018	R/W	**STN/TFT**: Frame buffer start address 2 register	0x00000000

LCDSADDR2	Bit	Description	Initial State
LCDBASEL	[20:0]	For dual-scan LCD: These bits indicate A[21:1] of the start address of the lower address counter, which is used for the lower frame memory of dual scan LCD. For single scan LCD: These bits indicate A[21:1] of the end address of the LCD frame buffer. LCDBASEL = ((the fame end address) >>1) + 1 = LCDBASEU + (PAGEWIDTH+OFFSIZE)x(LINEVAL+1)	0x0000

NOTE: Users can change the LCDBASEU and LCDBASEL values for scrolling while LCD controller is turned on. But, users must not change the LCDBASEU and LCDBASEL registers at the end of FRAME by referring to the LINECNT field in LCDCON1 register. Because of the LCD FIFO fetches the next frame data prior to the change in the frame. So, if you change the frame, the pre-fetched FIFO data will be obsolete and LCD controller will display the incorrect screen. To check the LINECNT, interrutpt should be masked. If any interrupt is executed just after reading LINECNT, the read LINECNT value may be obsolete because of the execution time of ISR(interrupt service routine).

FRAME Buffer Start Address 3 Register

Register	Address	R/W	Description	Reset Value
LCDSADDR3	0X4D00001C	R/W	**STN/TFT**: Virtual screen address set	0x00000000

LCDSADDR3	Bit	Description	Initial State
OFFSIZE	[21:11]	Virtual screen offset size(the number of half words) This value defines the difference between the address of the last half word displayed on the previous LCD line and the address of the first half word to be displayed in the new LCD line.	00000000000
PAGEWIDTH	[10:0]	Virtual screen page width(the number of half words) This value defines the width of the view port in the frame	000000000

NOTE: The values of PAGEWIDTH and OFFSIZE must be changed when ENVID bit is 0.

Example 1. LCD panel = 320*240, 16gray, single scan
frame start address = 0x0c500000
offset dot number = 2048 dots (512 half words)

LINEVAL = 240-1 = 0xef
PAGEWIDTH = 320*4/16 = 0x50
OFFSIZE = 512 = 0x200
LCDBANK = 0x0c500000 >> 22 = 0x31
LCDBASEU = 0x100000 >> 1 = 0x80000
LCDBASEL = 0x80000 + (0x50 + 0x200) * (0xef + 1) = 0xa2b00

Example 2. LCD panel = 320*240, 16gray, dual scan
frame start address = 0x0c500000
offset dot number = 2048 dots (512 half words)

LINEVAL = 120-1 = 0x77
PAGEWIDTH = 320*4/16 = 0x50
OFFSIZE = 512 = 0x200
LCDBANK = 0x0c500000 >> 22 = 0x31
LCDBASEU = 0x100000 >> 1 = 0x80000
LCDBASEL = 0x80000 + (0x50 + 0x200) * (0x77 + 1) = 0x91580

Example 3. LCD panel = 320*240, color, single scan
frame start address = 0x0c500000
offset dot number = 1024 dots (512 half words)

LINEVAL = 240-1 = 0xef
PAGEWIDTH = 320*8/16 = 0xa0
OFFSIZE = 512 = 0x200
LCDBANK = 0x0c500000 >> 22 = 0x31
LCDBASEU = 0x100000 >> 1 = 0x80000
LCDBASEL = 0x80000 + (0xa0 + 0x200) * (0xef + 1) = 0xa7600

RED Lookup Table Register

Register	Address	R/W	Description	Reset Value
REDLUT	0X4D000020	R/W	**STN**:Red lookup table register	0x00000000

REDLUT	Bit	Description	Initial State
REDVAL	[31:0]	These bits define which of the 16 shades each of the 8 possible red combinations will choose. 000 = REDVAL[3:0], 001 = REDVAL[7:4] 010 = REDVAL[11:8], 011 = REDVAL[15:12] 100 = REDVAL[19:16], 101 = REDVAL[23:20] 110 = REDVAL[27:24], 111 = REDVAL[31:28]	0x00000000

GREEN Lookup Table Register

Register	Address	R/W	Description	Reset Value
GREENLUT	0X4D000024	R/W	**STN**:Green lookup table register	0x00000000

GREENLUT	Bit	Description	Initial State
GREENVAL	[31:0]	These bits define which of the 16 shades each of the 8 possible green combinations will choose. 000 = GREENVAL[3:0], 001 = GREENVAL[7:4] 010 = GREENVAL[11:8], 011 = GREENVAL[15:12] 100 = GREENVAL[19:16], 101 = GREENVAL[23:20] 110 = GREENVAL[27:24], 111 = GREENVAL[31:28]	0x00000000

BLUE Lookup Table Register

Register	Address	R/W	Description	Reset Value
BLUELUT	0X4D000028	R/W	**STN**:Blue lookup table register	0x0000

BULELUT	Bit	Description	Initial State
BLUEVAL	[15:0]	These bits define which of the 16 shades each of the 4 possible blue combinations will choose 00 = BLUEVAL[3:0], 01 = BLUEVAL[7:4] 10 = BLUEVAL[11:8], 11 = BLUEVAL[15:12]	0x0000

NOTE: Address from **0x14A0002C** to **0x14A00048** should not be used. This area is reserved for Test mode.

Dithering Mode Register

Register	Address	R/W	Description	Reset Value
DITHMODE	0X4D00004C	R/W	**STN**:Dithering Mode Register. This register reset value is 0x00000 But, user can change this value to 0x12210. (Please, refer to a sample program source for the latest value of this register).	0x00000

DITHMODE	Bit	Description	initial state
DITHMODE	[18:0]	Use one of following value for your LCD 0x00000 or 0x12210	0x00000

Temp Palette Register

Register	Address	R/W	Description	Reset Value
TPAL	0X4D000050	R/W	**TFT**:Temporary Palette Register. This register value will be video data at next frame	0x00000000

TPAL	Bit	Description	initial state
TPALEN	[24]	Temporary Palette Register enable bit 0 = Disable 1 = Enable	0
TPALVAL	[23:0]	Temporary Palette Value Register. TPALVAL[23:16] : RED TPALVAL[15:8] : GREEN TPALVAL[7:0] : BLUE	0x000000

LCD Interrupt Pending Register

Register	Address	R/W	Description	Reset Value
LCDINTPND	0X4D000054	R/W	Indicates the LCD interrupt request status.	0x0

LCDINTPND	Bit	Description	initial state
INT_FrSyn	[1]	LCD frame synchronized interrupt 0 = The interrupt has not been requested 1 = The frame has asserted the interrupt request	0
INT_FiCnt	[0]	LCD FIFO empty interrupt 0 = The interrupt has not been requested 1 = FIFO empty status has asserted the interrupt request	0

LCD Source Pending Register

Register	Address	R/W	Description	Reset Value
LCDSRCPND	0X4D000058	R/W	Indicates the LCD interrupt request status.	0x0

LCDSRCPND	Bit	Description	initial state
INT_FrSyn	[1]	LCD frame synchronized interrupt 0 = The interrupt has not been requested 1 = The frame has asserted the interrupt request	0
INT_FiCnt	[0]	LCD FIFO empty interrupt 0 = The interrupt has not been requested 1 = FIFO empty status has asserted the interrupt request	0

LCD Interrupt Mask Register

Register	Address	R/W	Description	Reset Value
LCDINTMSK	0X4D00005C	R/W	Determines which interrupt source is masked. The masked interrupt source will not be serviced.	0x0

LCDINTMSK	Bit	Description	initial state
FIWSEL	[2]	This bit determines the trigger level of LCD FIFO 0 = 4 words 1 = 8 words	
INT_FrSyn	[1]	Mask LCD frame synchronized interrupt 0 = The interrupt service is available 1 = The interrupt service is masked	0
INT_FiCnt	[0]	Mask LCD FIFO empty interrupt 0 = The interrupt service is available 1 = The interrupt service is masked	0

LPC3600 Control Register

Register	Address	R/W	Description	Reset Value
LPCSEL	0X4D000060	R/W	This register control the LPC3600 modes.	0x4

LPCSEL	Bit	Description	initial state
CPV_SEL	[3]	It is same as the LPC3600.	0
MODE_SEL	[2]	It is same as the LPC3600.	1
RES_SEL	[1]	It is same as the LPC3600.	0
LPC_EN	[0]	This bit determines LPC3600 Enable/Disable 0 = LPC3600 Disable 1 = LPC3600 Enable	0

Register Setting Guide (STN)

The LCD controller supports multiple screen sizes by special register setting.

The CLKVAL value determines the frequency of VCLK. The data transmission rate for the VD port of the LCD controller should be calculated, in order to determine the value of CLKVAL register.

The data transmission rate is given by the following equation:

CLKVAL has to be determined, such that the VCLK value is greater than the data transmission rate.

Data transmission rate = HS × VS × FR × MV
HS: Horizontal LCD size
VS: Vertical LCD size
FR: Frame rate
MV: Mode dependent value

Table 15-6. MV Value for Each Display Mode

Mode	MV Value
Mono, 4-bit single scan display	1/4
Mono, 8-bit single scan display or 4-bit dual scan display	1/8
4 level gray, 4-bit single scan display	1/4
4 level gray, 8-bit single scan display or 4-bit dual scan display	1/8
16 level gray, 4-bit single scan display	1/4
16 level gray, 8-bit single scan display or 4-bit dual scan display	1/8
Color, 4-bit single scan display	3/4
Color, 8-bit single scan display or 4-bit dual scan display	3/8

The LCDBASEU register value is the first address value of the frame buffer. The lowest 4 bits must be eliminated for burst 4 word access. The LCDBASEL register value is determined by LCD size and LCDBASEU. The LCDBASEL value is given by the following equation:

LCDBASEL = LCDBASEU + LCDBASEL offset

Example 1:

160 x 160, 4-level gray, 80 frame/sec, 4-bit single scan display, HCLK frequency is 60 MHz WLH = 1, WDLY = 1.

Data transmission rate = 160 × 160 × 80 × 1/4 = 512 kHz
CLKVAL = 58, VCLK = 517KHz
HOZVAL = 39, LINEVAL = 159

LINEBLANK =10

LCDBASEL = LCDBASEU + 3200

NOTE: The higher the system load is, the lower the cpu performance is.

Example 2 (Virtual screen register):

4 -level gray, Virtual screen size = 1024 x 1024, LCD size = 320 x 240, LCDBASEU = 0x64, 4-bit dual scan.

1 half-word = 8 pixels (4-level gray),
Virtual screen 1 line = 128 half-word = 1024 pixels,
LCD 1 line = 320 pixels = 40 half-word,
OFFSIZE = 128 - 40 = 88 = 0x58,
PAGEWIDTH = 40 = 0x28

LCDBASEL = LCDBASEU + (PAGEWIDTH + OFFSIZE) x (LINEVAL +1) = 100 + (40 +88) x 120 = 0x3C64

Gray Level Selection Guide

S3C2410X01LCD controller can generate 16 gray level using FRC(frame rate control). The FRC characteristics may cause unexpected patterns in gray level. These unwanted erronous patterns may be shown in fast response LCD or at lower frame rates.

Because the quality of LCD gray levels depends on LCD's own characteristics, the user has to select the good gray levels after viewing all gray levels on user's own LCD.

Please select the gray level quality through the following procedures.

1. Get the latest dithering pattern register value from SAMSUNG.
2. Display 16 gray bar in LCD.
3. Change the frame rate into an optimal value.
4. Change the VM alternating period to get the best quality.
5. As viewing 16 gray bars, select the good gray levels, which is displayed well on your LCD.
6. Use only the good gray levels for quality.

LCD Refresh Bus Bandwidth Calculation Guide

S3C2410X01LCD controller can supports various LCD display size. To select suitable LCD display size(for the flicker free LCD system application), the user have to consider the LCD refresh bus bandwidth determined by LCD display size, bit per pixel(bpp), frame rate, memory bus width, memory type and so on.

LCD Data Rate(Byte/s) = bpp x (Horizontal display size) x (Vertical display size) x (Frame rate) /8

LCD DMA Burst Count(Times/s) = LCD Data Rate(Byte/s) /16(Byte) ; LCD DMA using 4words(16Byte) burst

Pdma means LCD DMA access period. In other words, the value of Pdma is the period of four-beat burst(4-words burst) for video data fetch. So, Pdma is determined by memory type and memory setting.

Eventually, LCD System Load is determined by LCD DMA Burst Count and Pdma.

LCD System Load = LCD DMA Burst Count x Pdma

Example 3 :

640 x 480, 8bpp, 60 frame/sec, 16-bit data bus width, SDRAM(Trp=2HCLK / Trcd=2HCLK / CL=2HCLK) and HCLK frequency is 60 MHz

LCD Data Rate = $8 \times 640 \times 480 \times 60 / 8 = 18.432$Mbyte/s
LCD DMA Burst Count = 18.432 / 16 = 1.152M/s
Pdma = $(Trp+Trcd+CL+(2 \times 4)+1) \times (1/60MHz) = 0.250$ms
LCD System Load = $1.152 \times 250 = 0.288$

System Bus Occupation Rate = $(0.288/1) \times 100 = 28.8\%$

Register Setting Guide (TFT LCD)

The CLKVAL register value determines the frequency of VCLK and frame rate.

Frame Rate = 1/ [{ (VSPW+1) + (VBPD+1) + (LIINEVAL + 1) + (VFPD+1) } x {(HSPW+1) + (HBPD +1) + (HFPD+1) + (HOZVAL + 1) } x { 2 x (CLKVAL+1) / (HCLK) }]

For applications, the system timing must be considered to avoid under-run condition of the fifo of the lcd controller caused by memory bandwidth contention.

Example 4 :

TFT Resolution : 240 x 240,

VSPW =2 , VBPD =14, LINEVAL = 239, VFPD =4

HSPW =25, HBPD =15, HOZVAL = 239, HFPD =1

CLKVAL = 5

HCLK = 60 M (hz)

Below parameter must be referenced by LCD Size, and Driver specification:

VSPW, VBPD, LINEVAL, VFPD, HSPW, HBPD, HOZVAL, HFPD

If target frame rate is 60–70Hz then CLKVAL should be 5.

So, Frame Rate = 67Hz

16 ADC & TOUCH SCREEN INTERFACE (PRELIMINARY)

OVERVIEW

The 10-bit CMOS ADC (Analog to Digital Converter) of S3C2410X01 is a recycling type device with 8-channel analog inputs. It converts the analog input signal into 10-bit binary digital codes at a maximum conversion rate of 500KSPS with 2.5MHz A/D converter clock. A/D converter operates with on-chip sample-and-hold function and power down mode is supported.

S3C2410X01 supports Touch Screen Interface.
This function consists of touch screen panel, 4 external transistors, external voltage source, AIN[7] and one of AIN[6:0] (refer to the example, Figure 16-2).
Touch Screen Interface is controlling and selecting control signal (nYPON, YMON, nXPON and XMON) and analog pads (AIN[7] and one of AIN[6:0]) which are connected with pads of touch screen panel and the external transistor for X-position conversion and Y-position conversion.
Touch Screen Interface contains external transistor control logic and ADC interface logic with an interrupt generation logic.

FEATURES

- Resolution: 10-bit
- Differential Linearity Error: ± 1.0 LSB
- Integral Linearity Error: ± 2.0 LSB
- Maximum Conversion Rate: 500 KSPS
- Low Power Consumption
- Power Supply Voltage: 3.3V
- Analog Input Range: 0 ~ 3.3V
- On-chip sample-and-hold function
- Normal Conversion Mode
- Separate X/Y position conversion Mode
- Auto(Sequential) X/Y Position Conversion Mode
- Waiting for Interrupt Mode

ADC & TOUCH SCREEN INTERFACE OPERATION

BLOCK DIAGRAM

Figure 16-1 shows the functional block diagram of S3C2410X01 A/D converter and Touch Screen Interface. Note that the A/D converter device is a recycling type.
A pull-up resister is attached to AIN[7] on VDDA_ADC. So, XP pad of touch screen panel should be connected with AIN[7] of S3C2410X01 and YP pad of touch screen panel should be connected with one of AIN[6:0].

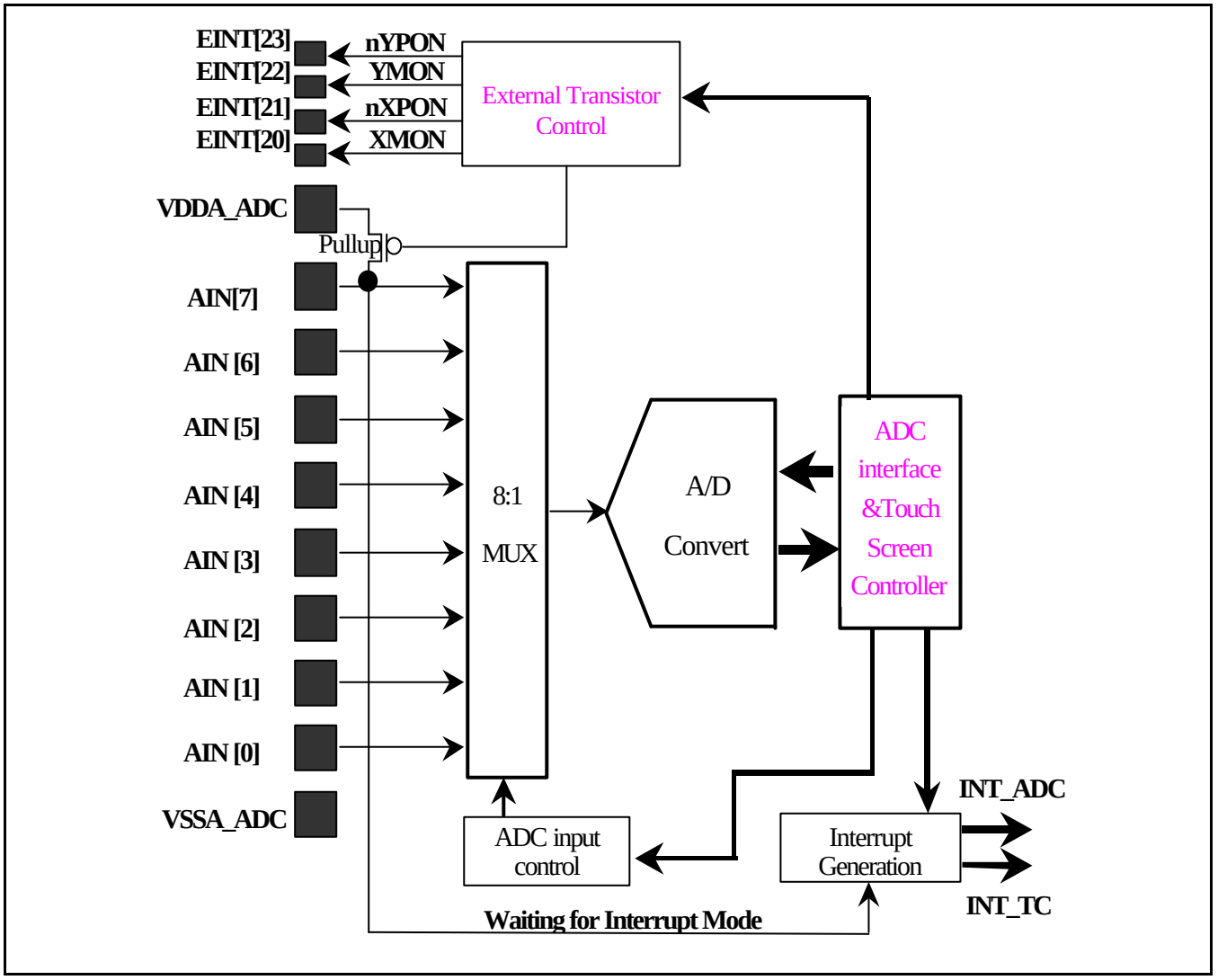


Figure 16-1. ADC and Touch Screen Interface Functional Block Diagram

EXAMPLE FOR TOUCH SCREEN

In this example, AIN[7] is connected with XP and AIN[6] is connected with YP pad of touch screen panel. Needless to say, AIN[5], AIN[4], AIN[3], AIN[2], AIN[1] or AIN[0] can be connected with YP instead of AIN[6]. To control pads of touch screen panel (XP, XM, YP and YM), 4 external transistor are applied and control signals, nYPON, YMON, nXPON and XMON are connected with 4 external transistor.

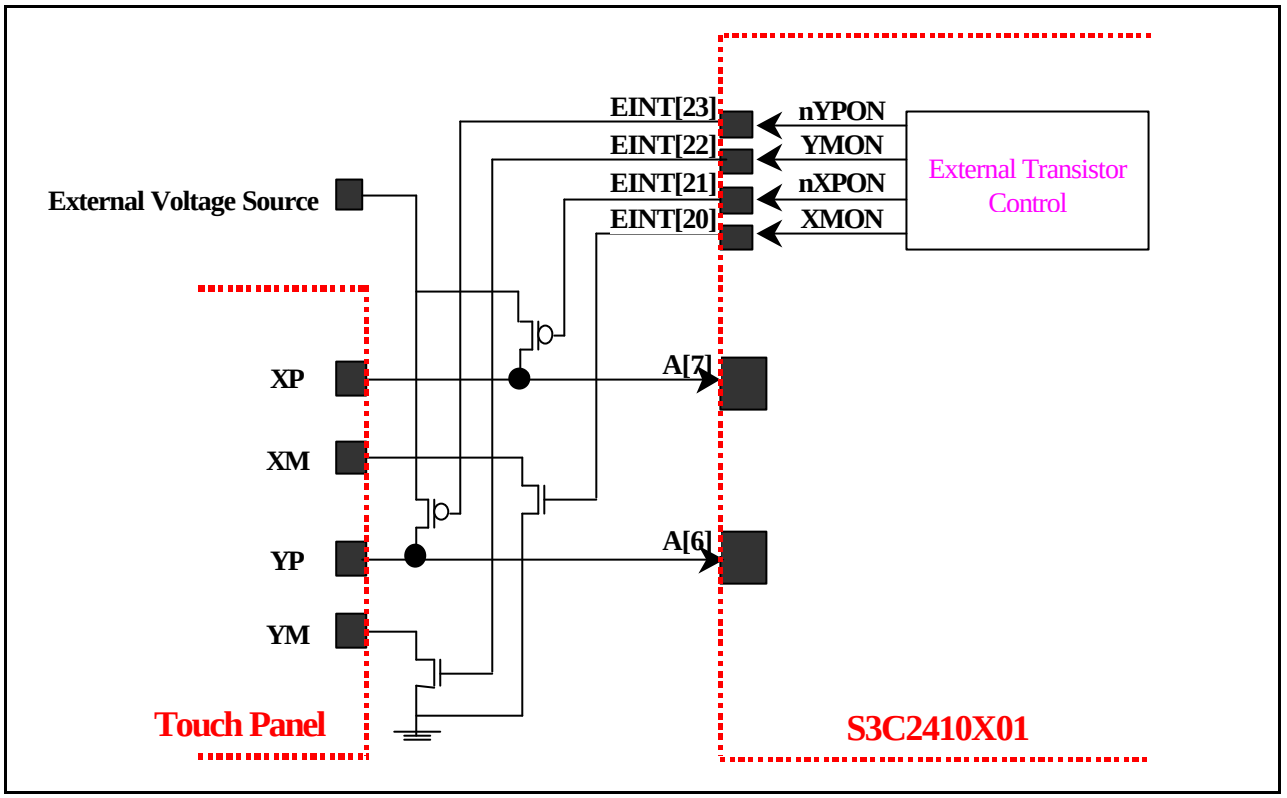


Figure 16-2. Example of ADC and Touch Screen Interface

1. Connect pads of touch screen panel to S3C2410X01 using external transistor(refer to Figure 16-2)
2. Select Separate X/Y Position Conversion Mode or Auto (Sequential) X/Y Position Conversion Mode to get X/Y position.
3. Set Touch Screen Interface to Waiting Interrupt Mode,
4. If interrupt occurs, then appropriate conversion (Separate X/Y Position Conversion Mode or Auto (Sequential) X/Y Position Conversion Mode) is activated.
5. After get the proper value about X/Y position, return to Waiting for Interrupt Mode. .

NOTE:

1. External voltage source should be 3.3 V.
2. Internal resistance of external transistor should be under 5 ohm.

FUNCTION DESCRIPTIONS

A/D Conversion Time

When the PCLK frequency is 50MHz and the prescaler value is 49, total 10-bit conversion time is as follows.

A/D converter freq. = 50MHz/(49+1) = 1MHz

Conversion time = 1/(1MHz / 5cycles) = 1/200KHz = 5 us

NOTE:
This A/D converter was designed to operate at maximum 2.5MHz clock, so the conversion rate can go up to 500 KSPS.

Touch Screen Interface Mode

1. Normal Conversion Mode

   Normal Conversion Mode (AUTO_PST = 0, XY_PST = 0) is the most likely used for General Purpose ADC Conversion. This mode can be initialized by setting the ADCCON and ADCTSC and completed with a read the XPDATA (Normal ADC) value of ADCDAT0 (ADC Data Register 0).

2. Separate X/Y Position Conversion Mode

   Touch Screen Controller can be operated by one of two Conversion Modes. Separate X/Y Position Conversion Mode is operated as the following way;
   X-Position Mode (AUTO_PST = 0 and XY_PST = 1) writes X-Position Conversion Data to XPDATA of ADCDAT0 register, After conversion, Touch Screen Interface generates the Interrupt source (INT_TC) to Interrupt Controller.
   Y-Position Mode (AUTO_PST = 0 and XY_PST = 2) writes Y-Position Conversion Data to YPDATA of ADCDAT1, After conversion, Touch Screen Interface generates the Interrupt source (INT_TC) to Interrupt Controller also.

Table 16-1. Condition of touch screen panel pads in Separate X/Y Position Conversion Mode.

	XP	XM	YP	YM
X Position Conversion	External Voltage	GND	AIN[n]	Hi-Z
Y Position Conversion	AIN[7]	Hi-Z	External Voltage	GND

3. Auto(Sequential) X/Y Position Conversion Mode

Auto (Sequential) X/Y Position Conversion Mode (AUTO_PST = 1 and XY_PST = 0) is operated as the following; Touch Screen Controller automatically converts X-Position and Y-Position. Touch Screen Controller writes X-measurement data to XPDATA of ADCDAT0, and then writes Y-measurement data to YPDATA of ADCDAT1. After Auto (Sequential) Position Conversion, Touch Screen Controller is generating Interrupt source(INT_TC) to Interrupt Controller.

Table 16-2. Condition of touch screen panel pads in Auto (Sequential) X/Y Position Conversion Mode.

	XP	XM	YP	YM
X Position Conversion	External Voltage	GND	AIN[n]	Hi-Z
Y Position Conversion	AIN[7]	Hi-Z	External Voltage	GND

4. Waiting for Interrupt Mode

When Touch Screen Controller is in Waiting for Interrupt Mode (YM_SEN = 1, XP_SEN = 1 and XY_PST = 3), Touch Screen Controller is waiting for Stylus down. Touch Screen Controller is generating Interrupt (INT_STY) signal when the Stylus is down on Touch Screen Panel.
After interrupt occurs, X and Y position can be read by the proper conversion mode (Separate X/Y position conversion Mode or Auto X/Y Position Conversion Mode).

Table 16-3. Condition of touch screen panel pads in Waiting for Interrupt Mode.

	XP	XM	YP	YM
Waiting for Interrupt Mode	Pull-up	Hi-Z	AIN[n]	GND

Standby Mode

Standby mode is activated when STDBM of ADCCON register is set to '1'. In this mode, A/D conversion operation is halted and XPDATA (Normal ADC) of ADCDAT0 and YPDATA of ADCDAT1 contain the previous converted data.

Programming Notes

1. The A/D converted data can be accessed by means of interrupt or polling method. With interrupt method the overall conversion time - from A/D converter start to converted data read - may be delayed because of the return time of interrupt service routine and data access time. With polling method, by checking the ADCCON[15] - end of conversion flag-bit, the read time from ADCDAT register can be determined.

2. Another way for starting A/D conversion is provided. After ADCCON[1] - A/D conversion start-by-read mode-is set to 1, A/D conversion starts simultaneously whenever converted data is read.

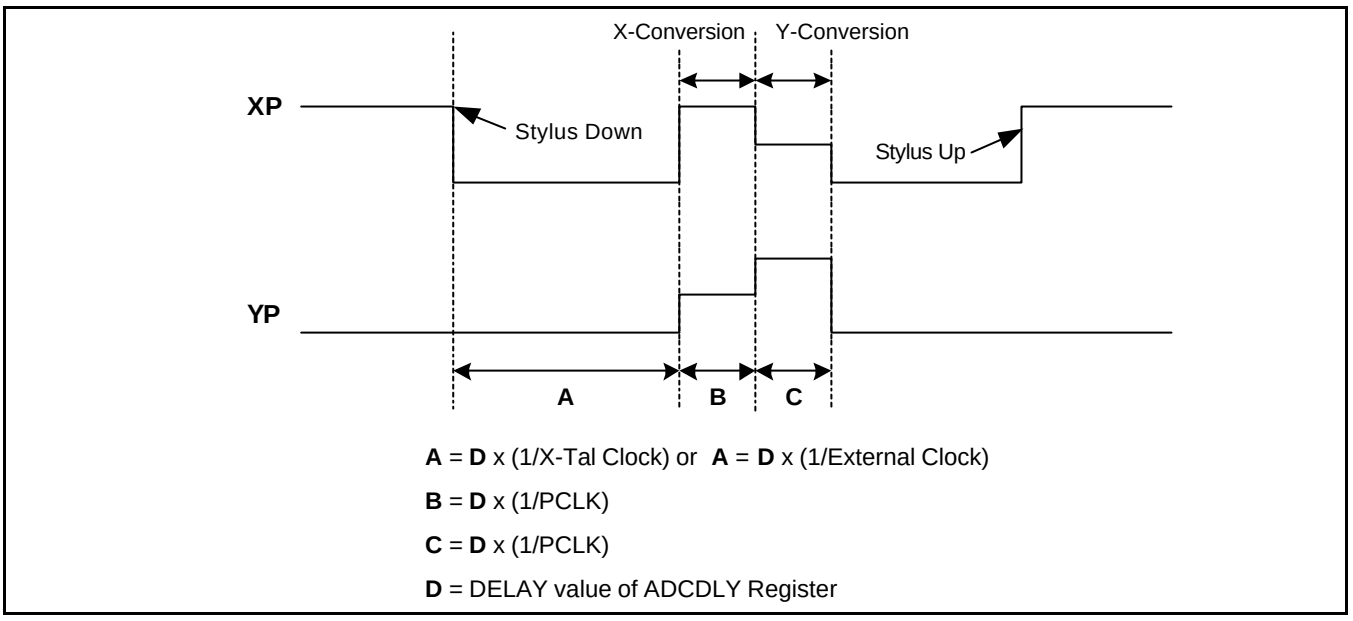


Figure 16-3 Timing Diagram at Auto (Sequential) X/Y Position Conversion Mode

ADC AND TOUCH SCREEN INTERFACE SPECIAL REGISTERS

ADC CONTROL REGISTER (ADCCON)

Register	Address	R/W	Description	Reset Value
ADCCON	0x5800_0000	R/W	ADC Control Register	0x3FC4

ADCCON	Bit	Description	Initial State
ECFLG	[15]	End of conversion flag(Read only) 0 = A/D conversion in process 1 = End of A/D conversion	0
PRSCEN	[14]	A/D converter prescaler enable 0 = Disable 1 = Enable	0
PRSCVL	[13:6]	A/D converter prescaler value Data value: 1 ~ 255 Note that division factor is (N+1) when prescaler value is N.	0xFF
SEL_MUX	[5:3]	Analog input channel select 000 = AIN 0 001 = AIN 1 010 = AIN 2 011 = AIN 3 100 = AIN 4 101 = AIN 5 110 = AIN 6 111 = AIN 7 (XP)	0
STDBM	[2]	Standby mode select 0 = Normal operation mode 1 = Standby mode	1
READ_ START	[1]	A/D conversion start by read 0 = Disable start by read operation 1 = Enable start by read operation	0
ENABLE_START	[0]	A/D conversion starts by setting this bit. If READ_START is enabled, this value is not valid. 0 = No operation 1 = A/D conversion starts and this bit is cleared after the start-up.	0

ADC TOUCH SCREEN CONTROL REGISTER (ADCTSC)

Register	Address	R/W	Description	Reset Value
ADCTSC	0x5800_0004	R/W	ADC Touch Screen Control Register	0x058

ADCTSC	Bit	Description	Initial State
UD_SEN	[8]	Stylus Up or Down Interrupt Signal 0 = Stylus Down Interrupt Signal. 1 = Stylus Up Interrupt Signal.	0
YM_SEN	[7]	Select output value of YMON 0 = YMON output is 0. (YM = Hi-Z) 1 = YMON output is 1. (YM = GND)	0
YP_SEN	[6]	Select output value of nYPON 0 = nYPON output is 0. (YP = External voltage) 1 = nYPON output is 1. (YP is connected with AIN[n])	1
XM_SEN	[5]	Select output value of XMON 0 = XMON output is 0. (XM = Hi-Z) 1 = XMON output is 1. (XM = GND)	0
XP_SEN	[4]	Select output value of nXPON 0 = nXPON output is 0. (XP = External voltage) 1 = nXPON output is 1. (XP is connected with AIN[7])	1
PULL_UP	[3]	Pull-up Switch Enable 0 = XP Pull-up Enable. 1 = XP Pull-up Disable.	1
AUTO_PST	[2]	Automatically sequencing conversion of X-Position and Y-Position 0 = Normal ADC conversion. 1 = Auto (Sequential) X/Y Position Conversion Mode.	0
XY_PST	[1:0]	Manually measurement of X-Position or Y-Position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	0

NOTE: AIN[n] means one of AIN[6:0].

ADC START DELAY REGISTER (ADCDLY)

Register	Address	R/W	Description	Reset Value
ADCDLY	0x5800_0008	R/W	ADC Start or Interval Delay Register	0x00ff

ADCDLY	Bit	Description	Initial State
DELAY	[15:0]	1) Normal Conversion Mode, Separate X/Y Position Conversion Mode, Auto (Sequential) X/Y Position Conversion Mode. → X/Y Position Conversion Delay Value. 2) Waiting for Interrupt Mode. When Stylus down occurs at Waiting for Interrupt Mode, generates Interrupt signal (INT_TC), having interval (several ms), for Auto X/Y Position conversion. **Note) Don' t use Zero value(0x0000)**	00ff

NOTE:

1. Before ADC conversion, Touch screen uses X-tal clock or EXTCLK (Waiting for Interrupt Mode).
2. During ADC conversion PCLK is used.

ADC CONVERSION DATA REGISTER (ADCDAT0)

Register	Address	R/W	Description	Reset Value
ADCDAT0	0x5800_000c	R	ADC Conversion Data Register	-

ADCDAT0	Bit	Description	Initial State
UPDOWN	[15]	Up or Down state of Stylus at Waiting for Interrupt Mode. 0 = Stylus down state. 1 = Stylus up state.	-
AUTO_PST	[14]	Automatic sequencing conversion of X-Position and Y-Position 0 = Normal ADC conversion. 1 = Sequencing measurement of X-position, Y-position.	-
XY_PST	[13:12]	Manually measurement of X-Position or Y-Position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	-
Reserved	[11:10]	Reserved	
XPDATA (Normal ADC)	[9:0]	X-Position Conversion data value (include Normal ADC Conversion data value) Data value : 0 ~ 3FF	-

ADC CONVERSION DATA REGISTER (ADCDAT1)

Register	Address	R/W	Description	Reset Value
ADCDAT1	0x5800_0010	R	ADC Conversion Data Register	-

ADCDAT1	Bit	Description	Initial State
UPDOWN	[15]	Up or Down state of Stylus at Waiting for Interrupt Mode. 0 = Stylus down state. 1 = Stylus up state.	-
AUTO_PST	[14]	Automatically sequencing conversion of X-Position and Y-Position 0 = Normal ADC conversion. 1 = Sequencing measurement of X-position, Y-position.	-
XY_PST	[13:12]	Manually measurement of X-Position or Y-Position. 00 = No operation mode 01 = X-position measurement 10 = Y-position measurement 11 = Waiting for Interrupt Mode	-
Reserved	[11:10]	Reserved	
YPDATA	[9:0]	Y-Position Conversion data value Data value : 0 ~ 3FF	-

17 RTC (REAL TIME CLOCK)(Preliminary)

OVERVIEW

The RTC (Real Time Clock) unit can be operated by the backup battery while the system power is off. The RTC can transmit 8-bit data to CPU as BCD (Binary Coded Decimal) values using the STRB/LDRB ARM operation. The data include second, minute, hour, date, day, month, and year. The RTC unit works with an external 32.768 KHz crystal and also can perform the alarm function.

FEATURE

— BCD number : second, minute, hour, date, day, month, year

— Leap year generator

— Alarm function : alarm interrupt or wake-up from power down mode.

— Year 2000 problem is removed.

— Independent power pin (RTCVDD)

— Supports millisecond tick time interrupt for RTOS kernel time tick.

— Round reset function

REAL TIME CLOCK OPERATION

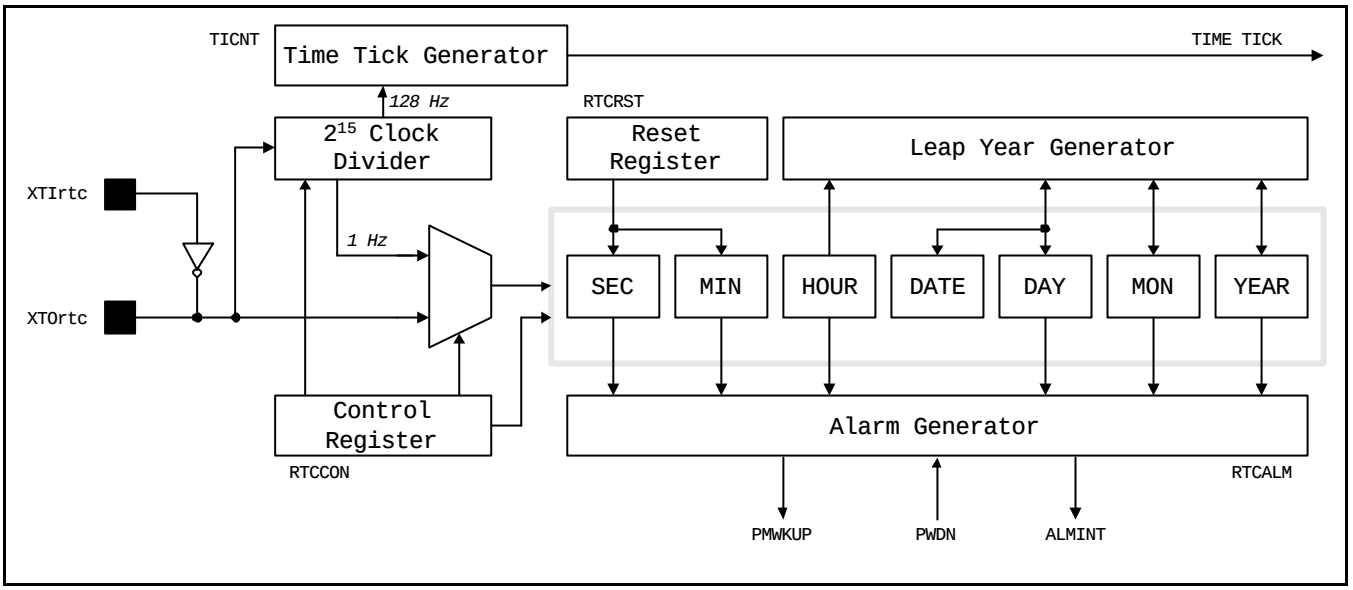


Figure 17-1. Real Time Clock Block Diagram

LEAP YEAR GENERATOR

This block can determine whether the last date of each month is 28, 29, 30, or 31, based on data from BCDDAY, BCDMON, and BCDYEAR. This block considers the leap year in deciding on the last date. An 8-bit counter can only represent 2 BCD digits, so it cannot decide whether 00 year is a leap year or not. For example, it can not discriminate between 1900 and 2000. To solve this problem, the RTC block in S3C2410X01 has hard-wired logic to support the leap year in 2000. Please note 1900 is not leap year while 2000 is leap year. Therefore, two digits of 00 in S3C2410X01 denote 2000, not 1900.

READ/WRITE REGISTERS

Bit 0 of the RTCCON register must be set to high in order to write the BCD register in RTC block. To display the sec., min., hour, date, month, and year, the CPU should read the data in BCDSEC, BCDMIN, BCDHOUR, BCDDAY, BCDDATE, BCDMON, and BCDYEAR registers, respectively, in the RTC block. However, a one second deviation may exist because multiple registers are read. For example, when the user reads the registers from BCDYEAR to BCDMIN, the result is assumed to be 2059(Year), 12(Month), 31(Date), 23(Hour) and 59(Minute). When the user read the BCDSEC register and the result is a value from 1 to 59(Second), there is no problem, but, if the result is 0 sec., the year, month, date, hour, and minute may be changed to 2060(Year), 1(Month), 1(Date), 0(Hour) and 0(Minute) because of the one second deviation that was mentioned. In this case, user should re-read from BCDYEAR to BCDSEC if BCDSEC is zero.

BACKUP BATTERY OPERATION

The RTC logic can be driven by the backup battery, which supplies the power through the RTCVDD pin into RTC block, even if the system power is off. When the system off, the interfaces of the CPU and RTC logic should be blocked, and the backup battery only drives the oscillation circuit and the BCD counters to minimize power dissipation.

ALARM FUNCTION

The RTC generates an alarm signal at a specified time in the power down mode or normal operation mode. In normal operation mode, the alarm interrupt (ALMINT) is activated. In the power down mode the power management wakeup (PMWKUP) signal is activated as well as the ALMINT. The RTC alarm register, RTCALM, determines the alarm enable/disable and the condition of the alarm time setting.

TICK TIME INTERRUPT

The RTC tick time is used for interrupt request. The TICNT register has an interrupt enable bit and the count value for the interrupt. The count value reaches '0' when the tick time interrupt occurs. Then the period of interrupt is as follow:

Period = (n+1) / 128 second
n : Tick time count value (1~127)

This RTC time tick may be used for RTOS(real time operating system) kernel time tick. If time tick is generated by RTC time tick, the time related function of RTOS will always synchronized with real time.

ROUND RESET FUNCTION

The round reset function can be performed by the RTC round reset register, RTCRST. The round boundary (30, 40, or 50 sec) of the second carry generation can be selected, and the second value is rounded to zero in the round reset. For example, when the current time is 23:37:47 and the round boundary is selected to 40 sec, the round reset changes the current time to 23:38:00.

NOTE

All RTC registers have to be accessed by the byte unit using the STRB,LDRB instructions or char type pointer.

32.768KHZ X-TAL CONNECTION EXAMPLE

The Figure 17-2 is an example circuit of the RTC unit oscillation at 32.768Khz.

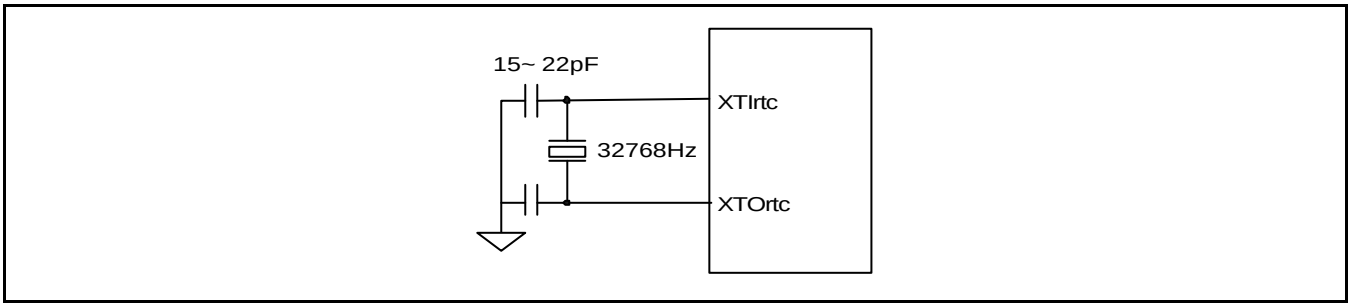


Figure 17-2. Main Oscillator Circuit Examples

REAL TIME CLOCK SPECIAL REGISTERS

REAL TIME CLOCK CONTROL REGISTER (RTCCON)

The RTCCON register consists of 4 bits such as the RTCEN, which controls the read/write enable of the BCD registers, CLKSEL, CNTSEL, and CLKRST for testing.

RTCEN bit can control all interfaces between the CPU and the RTC, so it should be set to 1 in an RTC control routine to enable data read/write after a system reset. Also before power off, the RTCEN bit should be cleared to 0 to prevent inadvertent writing into RTC registers.

Register	Address	R/W	Description	Reset Value
RTCCON	0x57000040(L) 0x57000043(B)	R/W (by byte)	RTC control Register	0x0

RTCCON	Bit	Description	Initial State
RTCEN	[0]	RTC control enable 0 = Disable NOTE : Only BCD time count and read operation can be performed. 1 = Enable	0
CLKSEL	[1]	BCD clock select 0 = XTAL $1/2^{15}$ divided clock 1 = Reserved (XTAL clock only for test)	0
CNTSEL	[2]	BCD count select 0 = Merge BCD counters 1 = Reserved (Separate BCD counters)	0
CLKRST	[3]	RTC clock count reset 0 = No reset, 1 = Reset	0

NOTES:

1. All RTC registers have to be accessed by byte unit using STRB and LDRB instructions or char type pointer.
2. (L): Little endian.
   (B): Big endian.

TICK TIME COUNT REGISTER (TICNT)

Register	Address	R/W	Description	Reset Value
TICNT	0x57000044(L) 0x57000047(B)	R/W (by byte)	Tick time count Register	0x0

TICNT	Bit	Description	Initial State
TICK INT ENABLE	[7]	Tick time interrupt enable 0 = Disable 1 = Enable	0
TICK TIME COUNT	[6:0]	Tick time count value. (1~127) This counter value decreases internally, and users can not read this real counter value in working.	000000

RTC ALARM CONTROL REGISTER (RTCALM)

RTCALM register determines the alarm enable and the alarm time. Note that the RTCALM register generates the alarm signal through both ALMINT and PMWKUP in power down mode, but only through ALMINT in the normal operation mode.

Register	Address	R/W	Description	Reset Value
RTCALM	0x57000050(L) 0x57000053(B)	R/W (by byte)	RTC alarm control Register	0x0

RTCALM	Bit	Description	Initial State
Reserved	[7]		0
ALMEN	[6]	Alarm global enable 0 = Disable, 1 = Enable	0
YEAREN	[5]	Year alarm enable 0 = Disable, 1 = Enable	0
MONREN	[4]	Month alarm enable 0 = Disable, 1 = Enable	0
DAYEN	[3]	Day alarm enable 0 = Disable, 1 = Enable	0
HOUREN	[2]	Hour alarm enable 0 = Disable, 1 = Enable	0
MINEN	[1]	Minute alarm enable 0 = Disable, 1 = Enable	0
SECEN	[0]	Second alarm enable 0 = Disable, 1 = Enable	0

ALARM SECOND DATA REGISTER (ALMSEC)

Register	Address	R/W	Description	Reset Value
ALMSEC	0x57000054(L) 0x57000057(B)	R/W (by byte)	Alarm second data Register	0x0

ALMSEC	Bit	Description	Initial State
Reserved	[7]		0
SECDATA	[6:4]	BCD value for alarm second from 0 to 5	000
	[3:0]	from 0 to 9	0000

ALARM MIN DATA REGISTER (ALMMIN)

Register	Address	R/W	Description	Reset Value
ALMMIN	0x57000058(L) 0x5700005B(B)	R/W (by byte)	Alarm minute data Register	0x00

ALMMIN	Bit	Description	Initial State
Reserved	[7]		0
MINDATA	[6:4]	BCD value for alarm minute from 0 to 5	000
	[3:0]	from 0 to 9	0000

ALARM HOUR DATA REGISTER (ALMHOUR)

Register	Address	R/W	Description	Reset Value
ALMHOUR	0x5700005C(L) 0x5700005F(B)	R/W (by byte)	Alarm hour data Register	0x0

ALMHOUR	Bit	Description	Initial State
Reserved	[7:6]		00
HOURDATA	[5:4]	BCD value for alarm hour from 0 to 2	00
	[3:0]	from 0 to 9	0000

ALARM DAY DATA REGISTER (ALMDAY)

Register	Address	R/W	Description	Reset Value
ALMDAY	0x57000060(L) 0x57000063(B)	R/W (by byte)	Alarm day data Register	0x01

ALMDAY	Bit	Description	Initial State
Reserved	[7:6]		00
DAYDATA	[5:4]	BCD value for alarm day, from 0 to 28, 29, 30, 31 from 0 to 3	00
	[3:0]	from 0 to 9	0001

ALARM MON DATA REGISTER (ALMMON)

Register	Address	R/W	Description	Reset Value
ALMMON	0x57000064(L) 0x57000067(B)	R/W (by byte)	Alarm month data Register	0x01

ALMMON	Bit	Description	Initial State
Reserved	[7:5]		00
MONDATA	[4]	BCD value for alarm month from 0 to 1	0
	[3:0]	from 0 to 9	0001

ALARM YEAR DATA REGISTER (ALMYEAR)

Register	Address	R/W	Description	Reset Value
ALMYEAR	0x57000068(L) 0x5700006B(B)	R/W (by byte)	Alarm year data Register	0x0

ALMYEAR	Bit	Description	Initial State
YEARDATA	[7:0]	BCD value for year from 00 to 99	0x0

RTC ROUND RESET REGISTER (RTCRST)

Register	Address	R/W	Description	Reset Value
RTCRST	0x5700006C(L) 0x5700006F(B)	R/W (by byte)	RTC round reset Register	0x0

RTCRST	Bit	Description	Initial State
SRSTEN	[3]	Round second reset enable 0 = Disable, 1 = Enable	0
SECCR	[2:0]	Round boundary for second carry generation. 011 = over than 30 sec 100 = over than 40 sec 101 = over than 50 sec **NOTE :** If other values(0,1,2,6,7) are set, no second carry is generated. But second value can be reset.	000

BCD SECOND REGISTER (BCDSEC)

Register	Address	R/W	Description	Reset Value
BCDSEC	0x57000070(L) 0x57000073(B)	R/W (by byte)	BCD second Register	Undefined

BCDSEC	Bit	Description	Initial State
SECDATA	[6:4]	BCD value for second from 0 to 5	-
	[3:0]	from 0 to 9	-

BCD MINUTE REGISTER (BCDMIN)

Register	Address	R/W	Description	Reset Value
BCDMIN	0x57000074(L) 0x57000077(B)	R/W (by byte)	BCD minute Register	Undefined

BCDMIN	Bit	Description	Initial State
MINDATA	[6:4]	BCD value for minute from 0 to 5	-
	[3:0]	from 0 to 9	-

BCD HOUR REGISTER (BCDHOUR)

Register	Address	R/W	Description	Reset Value
BCDHOUR	0x57000078(L) 0x5700007B(B)	R/W (by byte)	BCD hour Register	Undefined

BCDHOUR	Bit	Description	Initial State
Reserved	[7:6]		-
HOURDATA	[5:4]	BCD value for hour from 0 to 2	-
	[3:0]	from 0 to 9	-

BCD DAY REGISTER (BCDDAY)

Register	Address	R/W	Description	Reset Value
BCDDAY	0x5700007C(L) 0x5700007F(B)	R/W (by byte)	BCD day Register	Undefined

BCDDAY	Bit	Description	Initial State
Reserved	[7:6]		-
DAYDATA	[5:4]	BCD value for day from 0 to 3	-
	[3:0]	from 0 to 9	-

BCD DATE REGISTER (BCDDATE)

Register	Address	R/W	Description	Reset Value
BCDDATE	0x57000080(L) 0x57000083(B)	R/W (by byte)	BCD date Register	Undefined

BCDDATE	Bit	Description	Initial State
Reserved	[7:3]		-
DATEDATA	[2:0]	BCD value for date from 1 to 7	-

BCD MONTH REGISTER (BCDMON)

Register	Address	R/W	Description	Reset Value
BCDMON	0x57000084(L) 0x57000087(B)	R/W (by byte)	BCD month Register	Undefined

BCDMON	Bit	Description	Initial State
Reserved	[7:5]		-
MONDATA	[4]	BCD value for month from 0 to 1	-
	[3:0]	from 0 to 9	-

BCD YEAR REGISTER (BCDYEAR)

Register	Address	R/W	Description	Reset Value
BCDYEAR	0x57000088(L) 0x5700008B(B)	R/W (by byte)	BCD year Register	Undefined

BCDYEAR	Bit	Description	Initial State
YEARDATA	[7:0]	BCD value for year from 00 to 99	-

18 WATCH-DOG TIMER(Preliminary)

OVERVIEW

The S3C2410X01 watchdog timer is used to resume the controller operation when it had been disturbed by malfunctions such as noise and system errors. It can be used as a normal 16-bit interval timer to request interrupt service. The watchdog timer generates the reset signal for 128 PCLK cycles.

FEATURES

— Normal interval timer mode with interrupt request

— Internal reset signal is activated for 128 PCLK cycles when the timer count value reaches 0(time-out).

WATCH-DOG TIMER OPERATION

The functional block diagram of the watchdog timer is shown in Figure 18-1. The watchdog timer uses PCLK as its only source clock. To generate the corresponding watchdog timer clock, the PCLK frequency is prescaled first, and the resulting frequency is divided again.

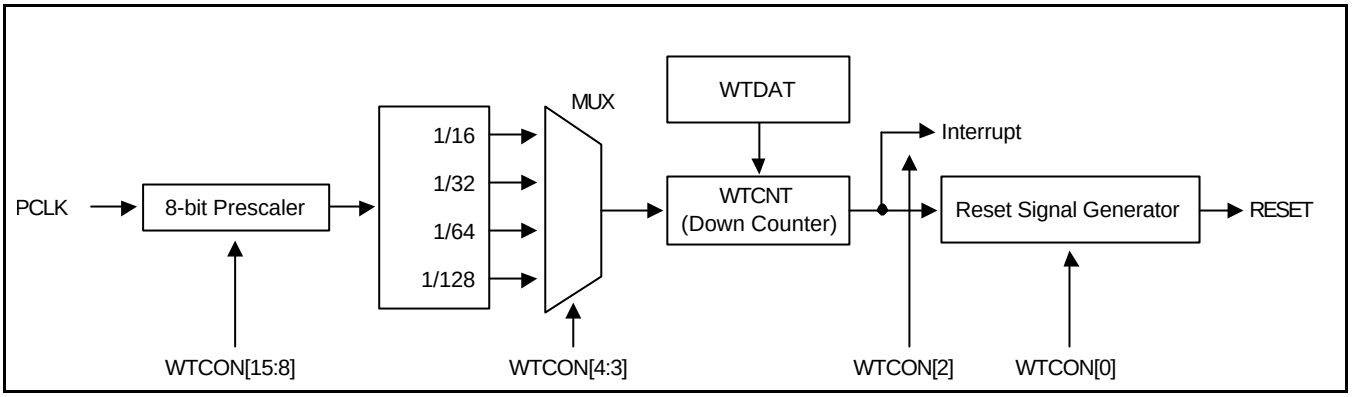


Figure 18-1. Watch-Dog Timer Block Diagram

The prescaler value and the frequency division factor are specified in the watchdog timer control register, WTCON. The valid prescaler values range from 0 to 2^8-1. The frequency division factor can be selected as 16, 32, 64, or 128.

Use the following equation to calculate the watchdog timer clock frequency and the duration of each timer clock cycle:

t_watchdog = 1/(PCLK / (Prescaler value + 1) / Division_factor)

WTDAT & WTCNT

When the watchdog timer is enabled first, the value of WTDAT (watchdog timer data register) cannot be automatically reloaded into the WTCNT (timer counter). For this reason, an initial value must be written to the watchdog timer count register, WTCNT, before the watchdog timer starts.

CONSIDERATION OF DEBUGGING ENVIRONMENT

When S3C2410X01 is in debug mode using Embedded ICE, the watch-dog timer must not operate.

The watch-dog timer can determine whether or not the current mode is the debug mode from the CPU core signal (DBGACK signal). Once the DBGACK signal is asserted, the reset output of the watch-dog timer is not activated when the watchdog timer is expired.

WATCH-DOG TIMER SPECIAL REGISTERS

WATCH-DOG TIMER CONTROL REGISTER (WTCON)

Using the Watch-Dog Timer Control register, WTCON, you can enable/disable the watch-dog timer, select the clock signal from 4 different sources, enable/disable interrupts, and enable/disable the watch-dog timer output.
The Watch-dog timer is used to resume the S3C2410X01 restart on mal-function after power-on; if controller restart is not desired, the Watch-dog timer should be disabled.

If the user wants to use the normal timer provided by the Watch-dog timer, please enable the interrupt and disable the Watch-dog timer.

Register	Address	R/W	Description	Reset Value
WTCON	0x52000000	R/W	Watch-dog timer control Register	0x8021

WTCON	Bit	Description	Initial State
Prescaler value	[15:8]	the prescaler value The valid range is from 0 to (2^8-1)	0x80
Reserved	[7:6]	Reserved. These two bits must be 00 in normal operation.	00
Watch-dog timer	[5]	Enable or disable bit of Watch-dog timer. 0 = Disable 1 = Enable	1
Clock select	[4:3]	This two bits determines the clock division factor 00 : 16 01 : 32 10 : 64 11 : 128	00
Interrupt generation	[2]	Enable or disable bit of the interrupt. 0 = Disable 1 = Enable	0
Reserved	[1]	Reserved. This bit must be 0 in normal operation	0
Reset enable/disable	[0]	Enable or disable bit of Watch-dog timer output for reset signal 1 : Asserts reset signal of the S3C2410X01 at watch-dog time-out 0 : dDsables the reset function of the watch-dog timer.	1

WATCH-DOG TIMER DATA REGISTER (WTDAT)

The watchdog timer data register, WTDAT is used to specify the time-out duration. The content of WTDAT can not be automatically loaded into the timer counter at initial watchdog timer operation. However, the first time-out occurs by using 0x8000(initial value), after then the value of WTDAT will be automatically reloaded into WTCNT.

Register	Address	R/W	Description	Reset Value
WTDAT	0x52000004	R/W	Watch-dog timer data Register	0x8000

WTDAT	Bit	Description	Initial State
count reload value	[15:0]	Watch-dog timer count value for reload.	0x8000

WATCH-DOG TIMER COUNT REGISTER (WTCNT)

The watchdog timer count register, WTCNT, contains the current count values for the watchdog timer during normal operation. Note that the content of the watchdog timer data register cannot be automatically loaded into the timer count register when the watchdog timer is enabled initially, so the watchdog timer count register must be set to an initial value before enabling it.

Register	Address	R/W	Description	Reset Value
WTCNT	0x52000008	R/W	Watch-dog timer count Register	0x8000

WTCNT	Bit	Description	Initial State
Count value	[15:0]	The current count value of the watch-dog timer	0x8000

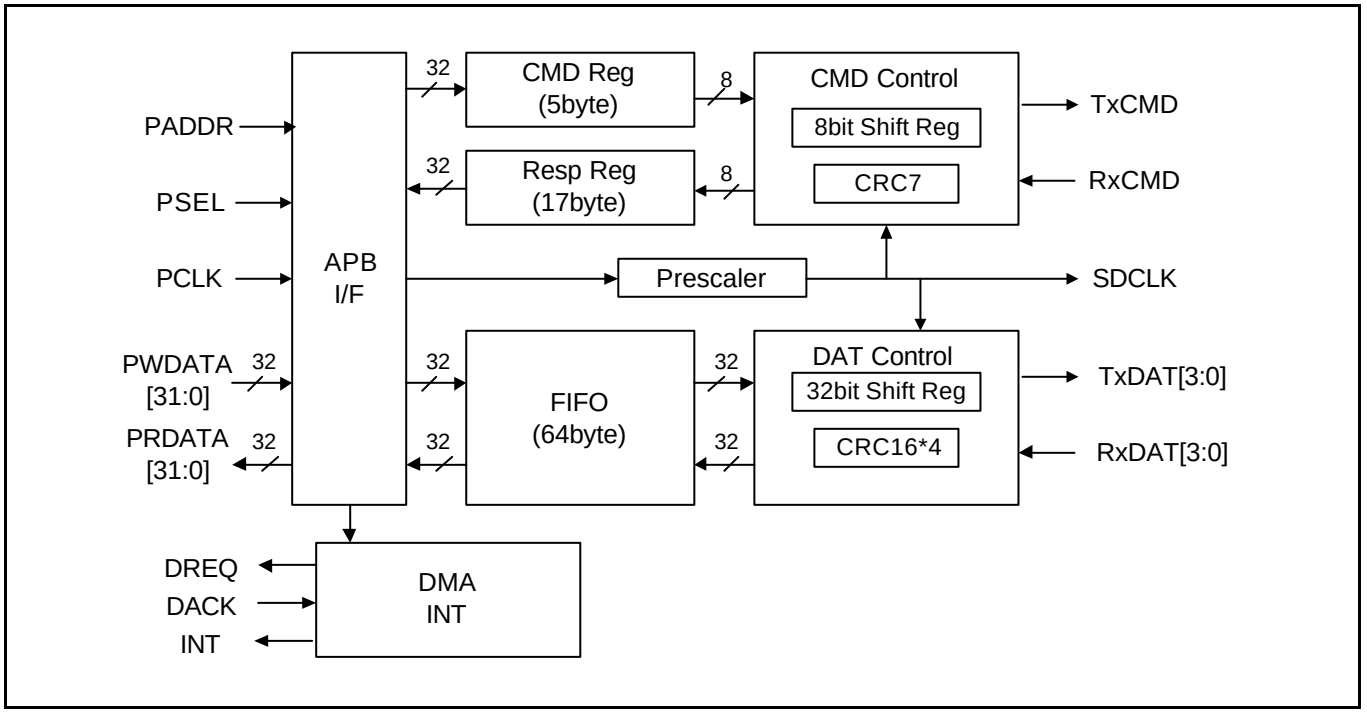
12/20/2001

19 SDI(Secure Digital Interface for SDIO)

Features

- SD Memory Card Spec(ver 1.0) / MMC Spec(2.11) compatible
- SDIO Card Spec(Ver 1.0) compatible
- 16 words(64 bytes) FIFO(depth 16) for data Tx/Rx
- 40-bit Command Register(SDICARG[31:0]+SDICCON[7:0])
- 136-bit Response Register(SDIRSPn[127:0]+ SDICSTA[7:0])
- 8-bit Prescaler logic (Freq. = System Clock / (2(P + 1)))
- CRC7 & CRC16 generator
- Normal, and DMA data transfer mode(byte or word transfer)
- 1bit / 4bit(wide bus) mode & block / stream mode switch support

BLOCK DIAGRAM



SD OPERATION

A serial clock line synchronizes shifting and sampling of the information on the five data lines. Making the appropriate bit settings to the SDIPRE register controls the transmission frequency. You can modify its frequency to adjust the baud rate data register value.

Programming Procedure(common)

To program the SDI modules, follow these basic steps:

1. Set SDICON to configure properly with clock and interrupt.
2. Set SDIPRE to configure with a proper value.
3. Wait 74 SDCLK clock cycle in order to initialize the card.

CMD Path Programming

1. Writes command argument(32-bit) to SDICARG register.
2. Determine command types and start command by setting SDICCON[8].
3. Confirm the end of SDI command operation when the specific flag of SDICSTA is set.
   – If the type of command is no-response type, the flag is SDICSTA[11].
   – If the type of command is with-response type, the flag is SDICSTA[9].
4. Clear the corresponding flag of the SDICSTA register by writing one to the flag bit.

DAT Path Programming

1. Write timeout period to SDIDTIMER register.
2. Write block size(block length) to SDIBSIZE register(normally 0x200 byte).
3. Determine the mode of block, wide bus, DMA, etc and start data transfer with setting SDIDCON register.
4. Write Tx-data to SDIDAT register while Tx FIFO is available by checking SDIFSTA(available, half or empty) register.
5. Read Rx-data from SDIDAT register while Rx FIFO is available by checking SDIFSTA(available, half or be last data) register.
6. Confirm the end of SDI data operation when the flag of data transfer finish(SDIDSTA[4]) is set.
7. Clear the corresponding flag of SDIDSTA register by writing one to the flag bit.

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SDIO OPERATION

There are two functions of SDIO operation: SDIO Interrupt receiving and Read Wait Request generation. These two functions can operate when RcvIOInt bit and RwaitEn bit of SDICON register is activated respectively. And two functions have the steps and conditions like below.

SDIO Interrupt

In SD 1bit mode, Interrupt is received through all range from SDDAT1 pin.

In SD 4bit mode, SDDAT1 pin is shared between data receiving and interrupts receiving.
When interrupt detection ranges(Interrupt Period) are :

1. Single Block : the time between A and B
   - A : 2clocks after the completion of a data packet
   - B : The completion of sending the end bit of the next with-data command
2. Multi Block, SDIDCON[21] = 0 : the time between A and B, restart interrupt detection range at C
   - A : 2clocks after the completion of a data packet
   - B : 2clocks after A
   - C : 2clocks after the end bit of the abort command response
3. Multi Block, SDIDCON[21] = 1 : the time between A and B, restart at A
   - A : 2clocks after the completion of a data packet
   - B : 2clocks after A
   - In case of last block, interrupt period begins at last A, but it does not end at B(CMD53 case)

Read Wait Request

Regardless of 1bit or 4bit mode, Read Wait Request signal transmits to SDDAT2 pin in condition of below.

- In read multiple operation, request signal transmission begins at 2clocks after the end of the data block
- Transmission ends when user write one to SDIDSTA[10]

SDI SPECIAL REGISTERS

SDI Control Register(SDICON)

Register	Address	R/W	Description	Reset Value
SDICON	0x5a00_0000	R/W	SDI Control Register	0x0

SDICON	Bit	Description	Initial Value
Byte Order Type(ByteOrder)	[4]	Determines byte order type when you read(write) data from(to) SD host FIFO with word boundary. 0 = Type A, 1 = Type B	0
Receive SDIO Interrupt from card (RcvIOInt)	[3]	Determines whether SD host receives SDIO Interrupt from the card or not(for SDIO). 0 = ignore, 1 = receive SDIO Interrupt	0
Read Wait Enable(RWaitEn)	[2]	Determines read wait request signal generate when SD host waits the next block in multiple block read mode. This bit needs to delay the next block to be transmitted from the card(for SDIO). 0 = disable(no generate), 1 = Read wait enable(use SDIO)	0
FIFO Reset(FRST)	[1]	Reset FIFO value. This bit is automatically clear. 0 = normal mode, 1 = FIFO reset	0
Clock Out Enable (ENCLK)	[0]	Determines whether FSCLK Out enable or not 0 = disable(prescaler off), 1 = clock enable	0

* Byte Order Type

- Type A : D[7:0] → D[15:8] → D[23:16] → D[31:24]
- Type B : D[31:24] → D[23:16] → D[15:8] → D[7:0]

SDI Baud Rate Prescaler Register(SDIPRE)

Register	Address	R/W	Description	Reset Value
SDIPRE	0x5a00_0004	R/W	SDI Buad Rate Prescaler Register	0x0

SDIPRE	Bit	Description	Initial Value
Prescaler Value	[7:0]	Determines SDI clock(SDCLK) rate as above equation. Baud rate = PCLK / 2 / (Prescaler value + 1)	0x00

SDI Command Argument Register(SDICARG)

Register	Address	R/W	Description	Reset Value
SDICARG	0x5a00_0008	R/W	SDI Command Argument Register	0x0

SDICARG	Bit	Description	Initial Value
CmdArg	[31:0]	Command Argument	0x00000000

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SDI Command Control Register(SDICCON)

Register	Address	R/W	Description	Reset Value
SDICCON	0x5a00_000c	R/W	SDI Command Control Register	0x0

SDICCON	Bit	Description	Initial Value
Abort Command (AbortCmd)	[12]	Determines whether command type is for abort(for SDIO). 0 = normal command, 1 = abort command(CMD12, CMD52)	0
Command with Data (WithData)	[11]	Determines whether command type is with data(for SDIO). 0 = without data, 1 = with data	0
LongRsp	[10]	Determines whether host receives a 136-bit long response or not 0 = short response, 1 = long response	0
WaitRsp	[9]	Determines whether host waits for a response or not 0 = no response, 1 = wait response	0
Command Start(CMST)	[8]	Determines whether command operation starts or not 0 = command ready, 1 = command start	0
CmdIndex	[7:0]	Command index with start 2bit(8bit)	0x00

SDI Command Status Register(SDICSTA)

Register	Address	R/W	Description	Reset Value
SDICSTA	0x5a00_0010	R/(W)	SDI Command Status Register	0x0

SDICSTA	Bit	Description	Initial Value
Response CRC Fail(RspCrc)	[12] R/W	CRC check failed when command response received. This flag is cleared by setting to one this bit. 0 = not detect, 1 = crc fail	0
Command Sent (CmdSent)	[11] R/W	Command sent(not concerned with response). This flag is cleared by setting to one this bit. 0 = not detect, 1 = command end	0
Command Time Out (CmdTout)	[10] R/W	Command response timeout(64clk). This flag is cleared by setting to one this bit. 0 = not detect, 1 = timeout	0
Response Receive End (RspFin)	[9] R/W	Command response received. This flag is cleared by setting to one this bit. 0 = not detect, 1 = response end	0
CMD line progress On (CmdOn)	[8] R	Command transfer in progress 0 = not detect, 1 = in progress	0
RspIndex	[7:0] R	Response index 6bit with start 2bit(8bit)	0x00

SDI Response Register 0(SDIRSP0)

Register	Address	R/W	Description	Reset Value
SDIRSP0	0x5a00_0014	R	SDI Response Register 0	0x0

SDIRSP0	Bit	Description	Initial Value
Response0	[31:0]	Card status[31:0](short), card status[127:96](long)	0x00000000

SDI Response Register 1(SDIRSP1)

Register	Address	R/W	Description	Reset Value
SDIRSP1	0x5a00_0018	R	SDI Response Register 1	0x0

SDIRSP1	Bit	Description	Initial Value
RCRC7	[31:24]	CRC7(with end bit, short), card status[95:88](long)	0x00
Response1	[23:0]	unused(short), card status[87:64](long)	0x000000

SDI Response Register 2(SDIRSP2)

Register	Address	R/W	Description	Reset Value
SDIRSP2	0x5a00_001c	R	SDI Response Register 2	0x0

SDIRSP2	Bit	Description	Initial Value
Response2	[31:0]	unused(short), card status[63:32](long)	0x00000000

SDI Response Register 3(SDIRSP3)

Register	Address	R/W	Description	Reset Value
SDIRSP3	0x5a00_0020	R	SDI Response Register 3	0x0

SDIRSP3	Bit	Description	Initial Value
Response3	[31:0]	unused(short), card status[31:0](long)	0x00000000

SDI Data / Busy Timer Register(SDIDTIMER)

Register	Address	R/W	Description	Reset Value
SDIDTIMER	0x5a00_0024	R/W	SDI Data / Busy Timer Register	0x0

SDIDTIMER	Bit	Description	Initial Value
DataTimer	[15:0]	Data / Busy timeout period(0~65535 cycle)	0x2000

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SDI Block Size Register(SDIBSIZE)

Register	Address	R/W	Description	Reset Value
SDIBSIZE	0x5a00_0028	R/W	SDI Block Size Register	0x0

SDIBSIZE	Bit	Description	Initial Value
BlkSize	[11:0]	Block Size value(0~4095 byte) , don' t care when stream mode	0x000

* In Case of multi block, BlkSize must be aligned to word(4byte) size.(BlkSize[1:0] = 00)

SDI Data Control Register(SDIDCON)

Register	Address	R/W	Description	Reset Value
SDIDCON	0x5a00_002c	R/W	SDI Data control Register	0x0

SDIDCON	Bit	Description	Initial Value
SDIO Interrupt Period Type (PrdType)	[21]	Determines whether SDIO Interrupt period is 2 cycle or extend more cycle when last data block is transferred(for SDIO). 0 = exactly 2 cycle, 1 = more cycle(likely single block)	0
Transmit After Response (TARSP)	[20]	Determines when data transmit start after response receive or not 0 = directly after DatMode set, 1 = after response receive(assume DatMode sets to 2' b11)	0
Receive After Command (RACMD)	[19]	Determines when data receive start after command sent or not 0 = directly after DatMode set, 1 = after command sent (assume DatMode sets to 2' b10)	0
Busy After Command (BACMD)	[18]	Determines when busy receive start after command sent or not 0 = directly after DatMode set, 1 = after command sent (assume DatMode sets to 2' b01)	0
Block mode (BlkMode)	[17]	Data transfer mode 0 = stream data transfer, 1 = block data transfer	0
Wide bus enable (WideBus)	[16]	Determines enable wide bus mode 0 = standard bus mode(only SDIDAT[0] used), 1 = wide bus mode(SDIDAT[3:0] used)	0
DMA Enable (EnDMA)	[15]	Enable DMA 0 = disable(polling), 1 = dma enable	0
Stop by force (STOP)	[14]	Determines whether data transfer stop by force or not 0 = normal, 1 = stop by force	0
Data Transfer Mode (DatMode)	[13:12]	Determines which direction of data transfer 00 = ready, 01 = only busy check start 10 = data receive start, 11 = data transmit start	00
BlkNum	[11:0]	Block Number(0~4095), don' t care when stream mode	0x000

* If you want one of TARSP, RACMD, BACMD bits(SDIDCON[20:18]) to " 1" , you need to write on SDIDCON register ahead of on SDICCON register.(always need for SDIO)

SDI Data Remain Counter Register(SDIDCNT)

Register	Address	R/W	Description	Reset Value
SDIDCNT	0x5a00_0030	R	SDI Data Remain Counter Register	0x0

SDIDCNT	Bit	Description	Initial Value
BlkNumCnt	[23:12]	Remaining Block number	0x000
BlkCnt	[11:0]	Remaining data byte of 1 block	0x000

SDI Data Status Register(SDIDSTA)

Register	Address	R/W	Description	Reset Value
SDIDSTA	0x5a00_0034	R/(W)	SDI Data Status Register	0x0

SDIDSTA	Bit	Description	Initial Value
Read Wait Request Occur (RWaitReq)	[10] R/W	Read wait request signal transmits to SD card. The request signal is stopped and this flag is cleared by setting to one this bit. 0 = not occur, 1 = Read wait request occur	0
SDIO Interrupt Detect(IOIntDet)	[9] R/W	SDIO interrupt detects. This flag is cleared by setting to one this bit. 0 = not detect, 1 = SDIO interrupt detect	0
FIFO Fail error (FFfail)	[8] R/W	FIFO fail error when FIFO occurs overrun / underrun / misaligned data saving. This flag is cleared by setting to one this bit. 0 = not detect, 1 = FIFO fail	0
CRC Status Fail(CrcSta)	[7] R/W	CRC Status error when data block sent(CRC check failed). This flag is cleared by setting to one this bit. 0 = not detect, 1 = crc status fail	0
Data Receive CRC Fail(DatCrc)	[6] R/W	Data block received error(CRC check failed). This flag is cleared by setting to one this bit. 0 = not detect, 1 = receive crc fail	0
Data Time Out(DatTout)	[5] R/W	Data / Busy receive timeout. This flag is cleared by setting to one this bit. 0 = not detect, 1 = timeout	0
Data Transfer Finish(DatFin)	[4] R/W	Data transfer completes(data counter is zero). This flag is cleared by setting to one this bit. 0 = not detect, 1 = data finish detect	0
Busy Finish (BusyFin)	[3] R/W	Only busy check finish. This flag is cleared by setting to one this bit 0 = not detect, 1 = busy finish detect	0
Start Bit Error(SbitErr)	[2] R/W	Start bit is not detected on all data signals in wide bus mode. This flag is cleared by setting to one this bit. 0 = not detect, 1 = command end	0
Tx Data progress On(TxDatOn)	[1] R	Data transmit in progress 0 = not active, 1 = data Tx in progress	0
Rx Data Progress On(RxDatOn)	[0] R	Data receive in progress 0 = not active, 1 = data Rx in progress	0

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SDI FIFO Status Register(SDIFSTA)

Register	Address	R/W	Description	Reset Value
SDIFSTA	0x5a00_0038	R	SDI FIFO Status Register	0x0

SDIFSTA	Bit	Description	Initial State
FIFO available Detect for Tx (TFDET)	[13]	This bit indicates that FIFO data is available for transmission when DatMode(SDIDCON[12]) is data transmit mode. If DMA mode is enable, SD host requests DMA operation. 0 = not detect(FIFO full), 1 = detect(0 ≤ FIFO ≤ 15)	0
FIFO available Detect for Rx (RFDET)	[12]	This bit indicates that FIFO data is available for reception when DatMode(SDIDCON[12]) is data receive mode. If DMA mode is enable, SD host requests DMA operation. 0 = not detect(FIFO empty), 1 = detect(1 ≤ FIFO ≤ 16)	0
Tx FIFO Half Full (TFHalf)	[11]	This bit sets to 1 whenever Tx FIFO is less than 33byte. 0 = 33 ≤ Tx FIFO ≤ 64, 1 = 0 ≤ Tx FIFO ≤ 32	0
Tx FIFO Empty (TFEmpty)	[10]	This bit sets to 1 whenever Tx FIFO is empty. 0 = 1 ≤ Tx FIFO ≤ 64, 1 = Empty(0byte)	0
Rx FIFO Last Data Ready (RFLast)	[9]	This bit sets to 1 whenever Rx FIFO has last data of all block. 0 = not received yet, 1 = Last data ready	0
Rx FIFO Full (RFFull)	[8]	This bit sets to 1 whenever Rx FIFO is full. 0 = 0 ≤ Rx FIFO ≤ 63, 1 = Full(64byte)	0
Rx FIFO Half Full (RFHalf)	[7]	This bit sets to 1 whenever Rx FIFO is more than 31byte. 0 = 0 ≤ Rx FIFO ≤ 31, 1 = 32 ≤ Rx FIFO ≤ 64	0
FIFO Count (FFCNT)	[6:0]	Number of data(byte) in FIFO	0000000

SDI Data Register(SDIDAT)

Register	Address	R/W	Description	Reset Value
SDIDAT	0x5a00_003c(Li/W, Li/B, Bi/W) 0x5a00_003f(Bi/B)	R/W	SDI Data Register	0x0

SDIDAT	Bit	Description	Initial State
Data Register	[31:0]	This field contains the data to be transmitted or received over the SDI channel	0x00000000

* (Li/W, Li/B) : Access by Word/Byte unit when endian mode is Little
* (Bi/W) : Access by Word unit when endian mode is Big
* (Bi/B) : Access by Byte unit when endian mode is Big

SDI Interrupt Mask Register(SDIIMSK)

Register	Address	R/W	Description	Reset Value
SDIIMSK	0x5a00_0040	R/W	SDI Interrupt Mask Register	0x0

SDICON	Bit	Description	Initial Value
RspCrc Interrupt Enable	[17]	Response CRC error interrupt. 0 = disable, 1 = interrupt enable	0
CmdSent Interrupt Enable	[16]	Command sent(without response) interrupt. 0 = disable, 1 = interrupt enable	0
CmdTout Interrupt Enable	[15]	Command response timeout interrupt. 0 = disable, 1 = interrupt enable	0
RspEnd Interrupt Enable	[14]	Command response received interrupt. 0 = disable, 1 = interrupt enable	0
RWaitReq Interrupt Enable	[13]	Read wait request interrupt. 0 = disable, 1 = interrupt enable	0
IOIntDet Interrupt Enable	[12]	SD host receives SDIO Interrupt from the card(for SDIO). 0 = disable, 1 = interrupt enable	0
FFfail Interrupt Enable	[11]	FIFO fail error interrupt. 0 = disable, 1 = interrupt enable	0
CrcSta Interrupt Enable	[10]	CRC status errors interrupt. 0 = disable, 1 = interrupt enable	0
DatCrc Interrupt Enable	[9]	Data CRC fail interrupt. 0 = disable, 1 = interrupt enable	0
DatTout Interrupt Enable	[8]	Data timeout interrupt. 0 = disable, 1 = interrupt enable	0
DatFin Interrupt Enable	[7]	Data counter zero interrupt. 0 = disable, 1 = interrupt enable	0
BusyFin Interrupt Enable	[6]	Busy checks complete interrupt. 0 = disable, 1 = interrupt enable	0
SBitErr Interrupt Enable	[5]	Start bit error interrupt. 0 = disable, 1 = interrupt enable	0
TFHalf Interrupt Enable	[4]	Tx FIFO half interrupt. 0 = disable, 1 = interrupt enable	0
TFEmpty Interrupt Enable	[3]	Tx FIFO empty interrupt. 0 = disable, 1 = interrupt enable	0
RFLast Interrupt Enable	[2]	Rx FIFO has last data interrupt. 0 = disable, 1 = interrupt enable	0
RFFull Interrupt Enable	[1]	Rx FIFO full interrupt. 0 = disable, 1 = interrupt enable	0
RFHalf Interrupt Enable	[0]	Rx FIFO half interrupt. 0 = disable, 1 = interrupt enable	0

20 IIC-BUS INTERFACE(Preliminary)

OVERVIEW

The S3C2410X RISC microprocessor can support a multi-master IIC-bus serial interface. A dedicated serial data line(SDA) and a serial clock line (SCL) carry information between bus masters and peripheral devices which are connected to the IIC-bus. The SDA and SCL lines are bi-directional.

In multi-master IIC-bus mode, multiple S3C2410X RISC microprocessors can receive or transmit serial data to or from slave devices. The master S3C2410X, which can initiate a data transfer over the IIC-bus, is responsible for terminating the transfer. Standard bus arbitration procedure is used in this IIC-bus in S3C2410X.

To control multi-master IIC-bus operations, values must be written to the following registers:

— Multi-master IIC-bus control register, IICCON

— Multi-master IIC-bus control/status register, IICSTAT

— Multi-master IIC-bus Tx/Rx data shift register, IICDS

— Multi-master IIC-bus address register, IICADD

When the IIC-bus is free, the SDA and SCL lines should be both at High level. A High-to-Low transition of SDA can initiate a Start condition. A Low-to-High transition of SDA can initiate a Stop condition while SCL remains steady at High Level.

The Start and Stop conditions can always be generated by the master devices. A 7-bit address value in the first data byte, which is put onto the bus after the Start condition has been initiated, can determine the slave device which the bus master device has selected. The 8^{th} bit determines the direction of the transfer (read or write).

Every data byte put onto the SDA line should total eight bits. The number of bytes which can be sent or received during the bus transfer operation is unlimited. Data is always sent from most-significant bit (MSB) first, and every byte should be immediately followed by an acknowledge (ACK) bit.

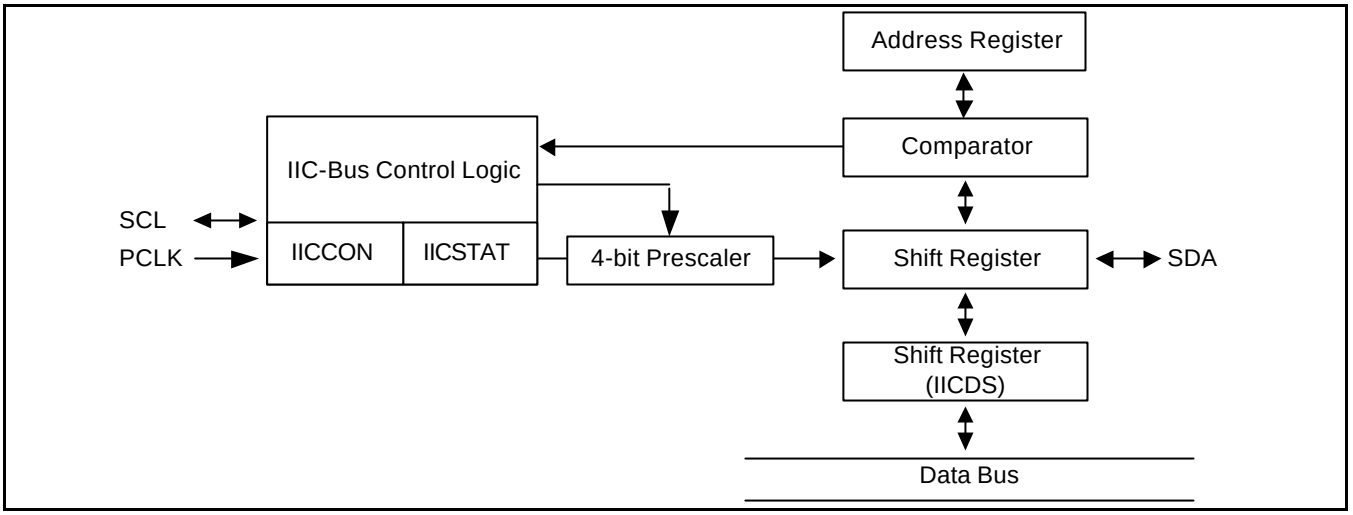

Figure 20-1. IIC-Bus Block Diagram

THE IIC-BUS INTERFACE

The S3C2410X IIC-bus interface has four operation modes:

— Master transmitter mode

— Master receive mode

— Slave transmitter mode

— Slave receive mode

Functional relationships among these operating modes are described below.

START AND STOP CONDITIONS

When the IIC-bus interface is inactive, it is usually in slave mode. In other words, the interface should be in slave mode before detecting a Start condition on the SDA line.(A Start condition can be initiated with a High-to-Low transition of the SDA line while the clock signal of SCL is High) When the interface state is changed to the master mode, a data transfer on the SDA line can be initiated and SCL signal generated.

A Start condition can transfer a one-byte serial data over the SDA line, and a stop condition can terminate the data transfer. A stop condition is a Low-to-High transition of the SDA line while SCL is High. Start and Stop conditions are always generated by the master. The IIC-bus is busy when a Start condition is generated. A few clocks after a Stop condition, the IIC-bus will be free, again.

When a master initiates a Start condition, it should send a slave address to notify the slave device. The one byte of address field consist of a 7-bit address and a 1-bit transfer direction indicator (that is, write or read).
If bit 8 is 0, it indicates a write operation(transmit operation); if bit 8 is 1, it indicates a request for data read(receive operation).

The master will finish the transfer operation by transmitting a Stop condition. If the master wants to continue the data transmission to the bus, it should generate another Start condition as well as a slave address. In this way, the read-write operation can be performed in various formats.

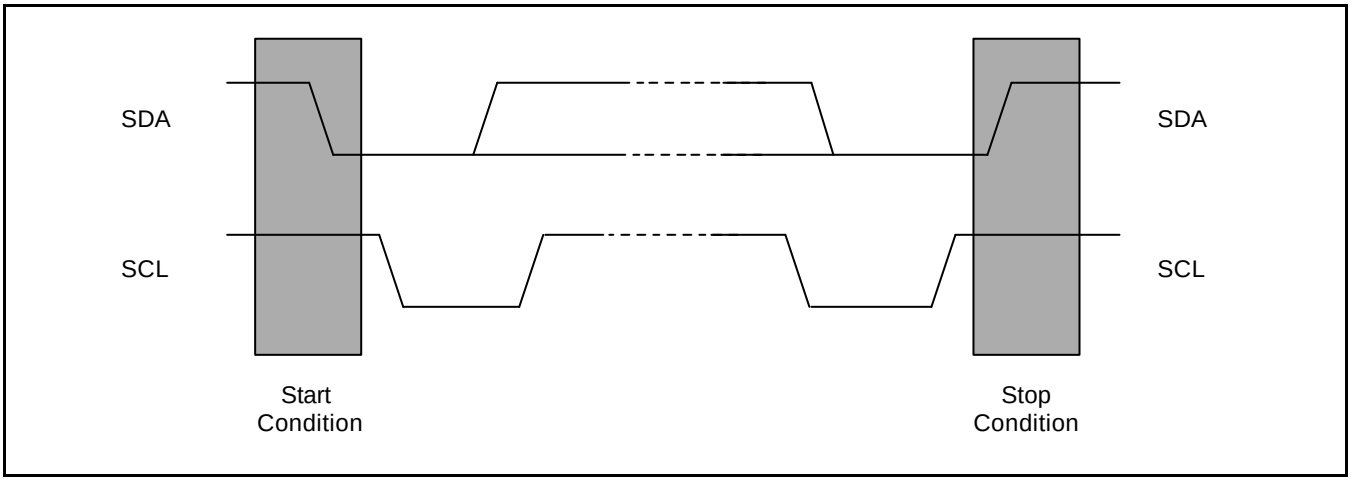

Figure 20-2. Start and Stop Condition

DATA TRANSFER FORMAT

Every byte placed on the SDA line should be eight bits in length. The number of bytes which can be transmitted per transfer is unlimited. The first byte following a Start condition should have the address field. The address field can be transmitted by the master when the IIC-bus is operating in master mode. Each byte should be followed by an acknowledgement (ACK) bit. The MSB bit of the serial data and addresses are always sent first.

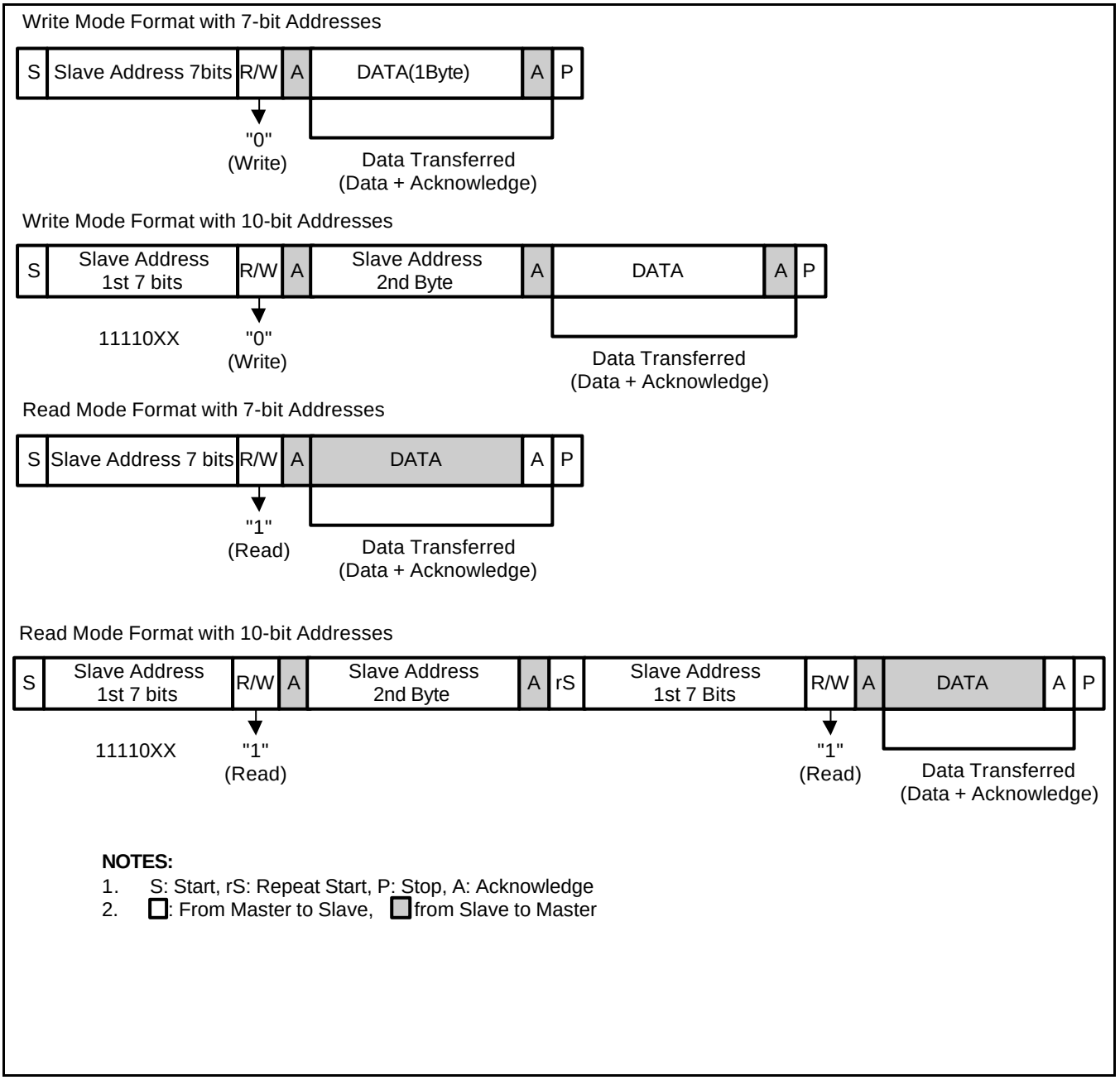

Figure 20-3. IIC-Bus Interface Data Format

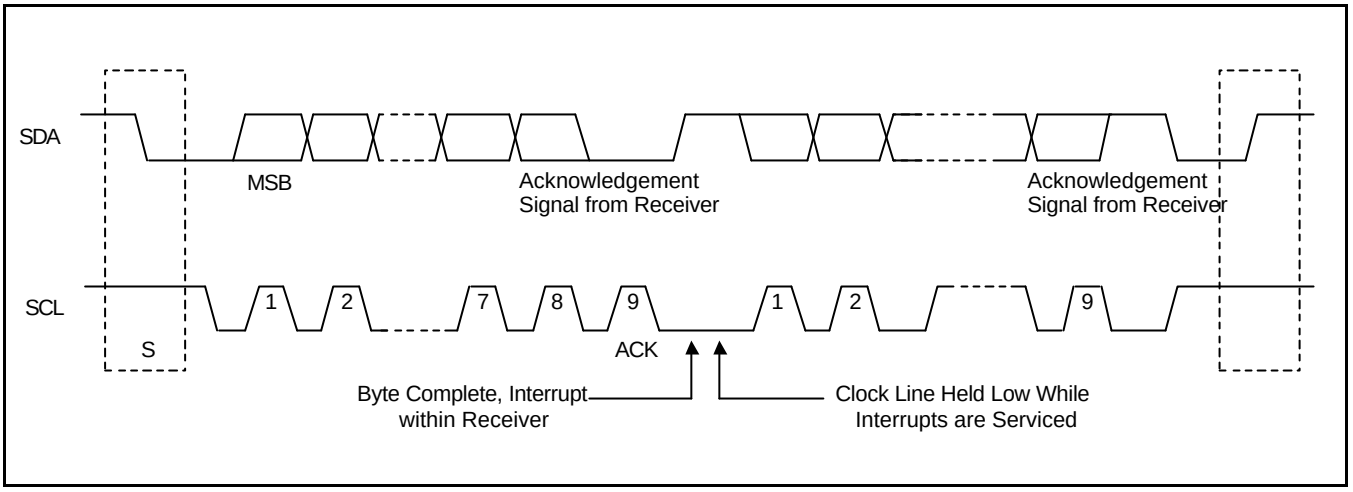

Figure 20-4. Data Transfer on the IIC-Bus

ACK SIGNAL TRANSMISSION

To finish a one-byte transfer operation completely, the receiver should send an ACK bit to the transmitter. The ACK pulse should occur at the ninth clock of the SCL line. Eight clocks are required for the one-byte data transfer. The master should generate the clock pulse required to transmit the ACK bit.

The transmitter should release the SDA line by making the SDA line High when the ACK clock pulse is received. The receiver should also drive the SDA line Low during the ACK clock pulse so that the SDA is Low during the High period of the ninth SCL pulse.

The ACK bit transmit function can be enabled or disabled by software (IICSTAT). However, the ACK pulse on the ninth clock of SCL is required to complete a one-byte data transfer operation.

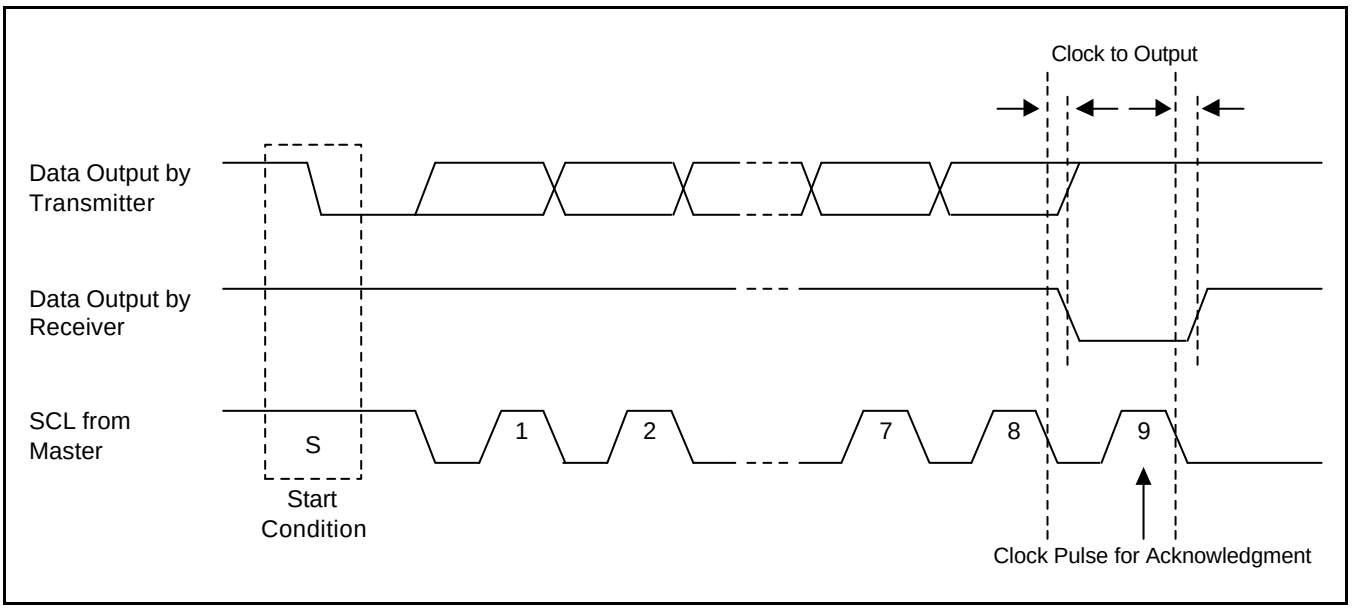

Figure 20-5. Acknowledge on the IIC-Bus

READ-WRITE OPERATION

In the transmitter mode, after the data is transferred, the IIC-bus interface will wait until IICDS(IIC-bus Data Shift Register) is written by a new data. Until the new data is written, the SCL line will be held low. After the new data is written to IICDS register, the SCL line will be released. The S3C2410X should hold the interrupt to identify the completion of current data transfer. After the CPU receives the interrupt request, it should write a new data into IICDS, again.

In the receive mode, after a data is received, the IIC-bus interface will wait until IICDS register is read. Until the new data is read out, the SCL line will be held low. After the new data is read out from IICDS register, the SCL line will be released. The S3C2410X should hold the interrupt to identify the completion of the new data reception. After the CPU receives the interrupt request, it should read the data from IICDS.

BUS ARBITRATION PROCEDURES

Arbitration takes place on the SDA line to prevent the contention on the bus between two masters. If a master with a SDA High level detects another master with a SDA active Low level, it will not initiate a data transfer because the current level on the bus does not correspond to its own. The arbitration procedure will be extended until the SDA line turns High.

However when the masters simultaneously lower the SDA line, each master should evaluate whether or not the mastership is allocated to itself. For the purpose of evaluation, each master should detect the address bits. While each master generates the slaver address, it should also detect the address bit on the SDA line because the lowering of SDA line is stronger than maintaining High on the line. For example, one master generates a Low as first address bit, while the other master is maintaining High. In this case, both masters will detect Low on the bus because Low is stronger than High even if first master is trying to maintain High on the line. When this happens, Low(as the first bit of address) -generating master will get the mastership and High(as the first bit of address) -generating master should withdraw the mastership. If both masters generate Low as the first bit of address, there should be an arbitration for second address bit, again. This arbitration will continue to the end of last address bit.

ABORT CONDITIONS

If a slave receiver can not acknowledge the confirmation of the slave address, it should hold the level of the SDA line High. In this case, the master should generate a Stop condition and to abort the transfer.

If a master receiver is involved in the aborted transfer, it should signal the end of the slave transmit operation by canceling the generation of an ACK after the last data byte received from the slave. The slave transmitter should then release the SDA to allow a master to generate a Stop condition.

CONFIGURING THE IIC-BUS

To control the frequency of the serial clock (SCL), the 4-bit prescaler value can be programmed in the IICCON register. The IIC-bus interface address is stored in the IIC-bus address register, IICADD. (By default, the IIC-bus interface address is an unknown value.)

FLOWCHARTS OF THE OPERATIONS IN EACH MODE

The following steps must be executed before any IIC Tx/Rx operations.

1) Write own slave address on IICADD register if needed.
2) Set IICCON Register.
   a) Enable interrupt
   b) Define SCL period
3) Set IICSTAT to enable Serial Output

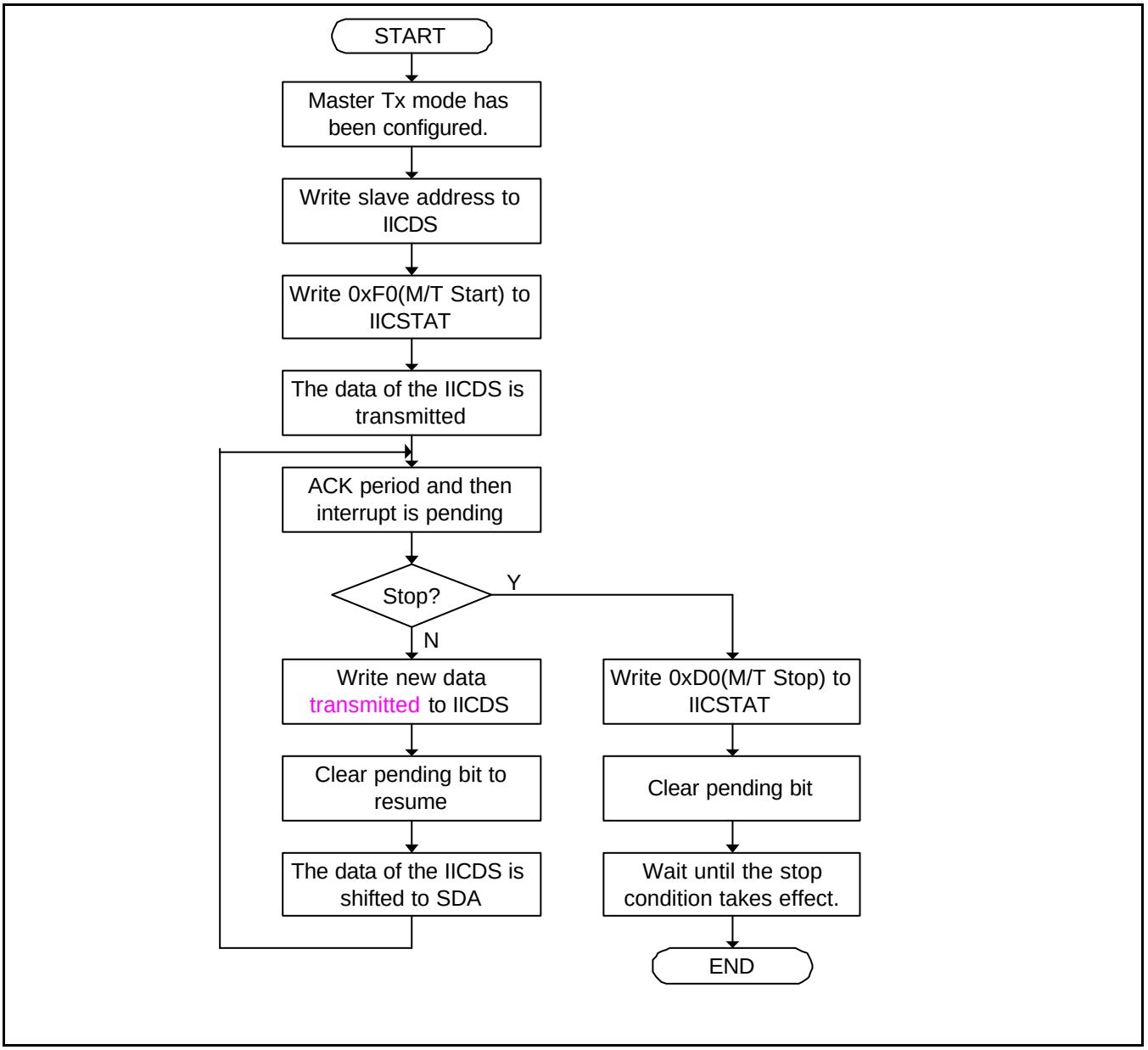

Figure 20-6 Operations for Master / Transmitter Mode

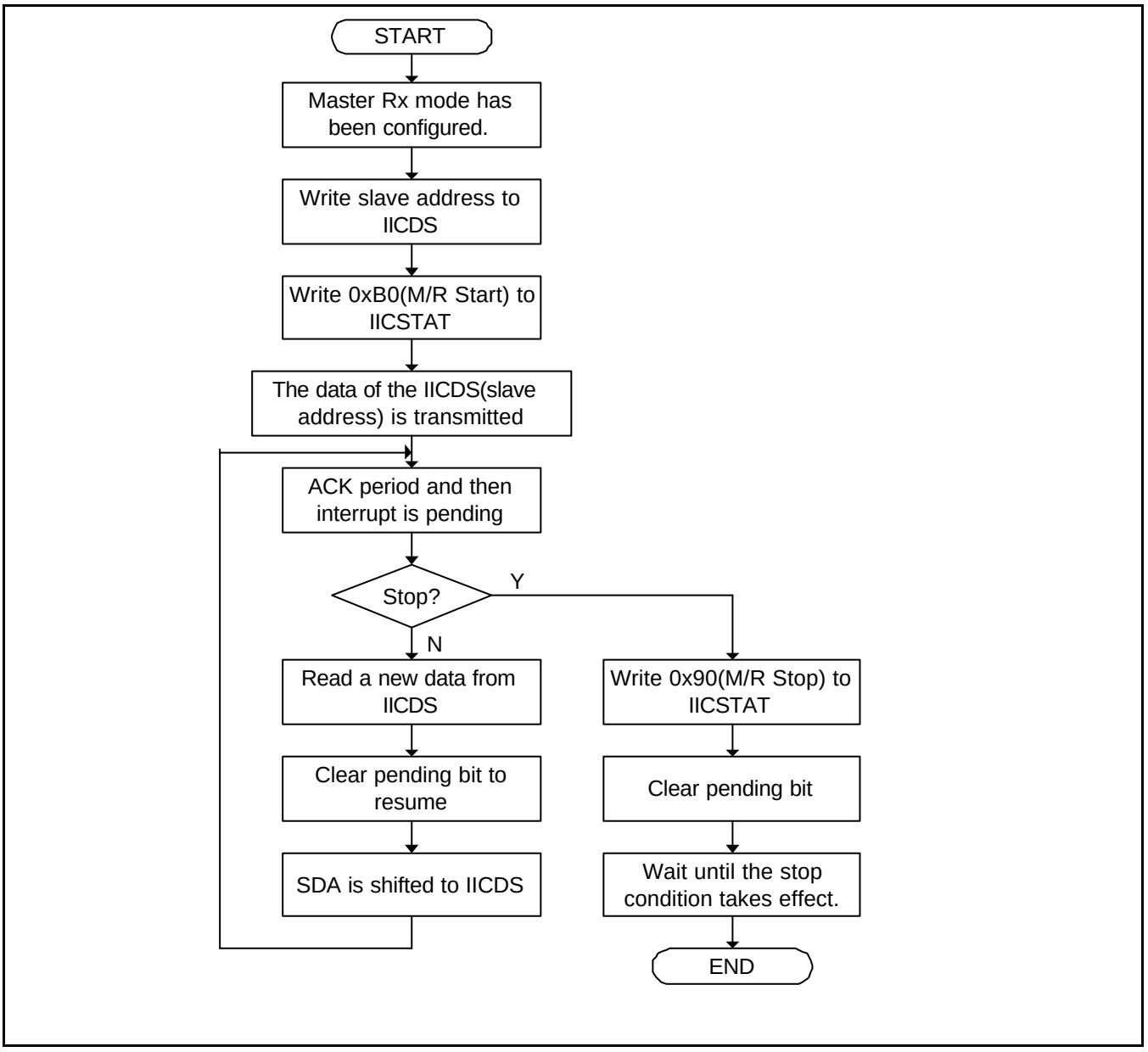

Figure 20-7 Operations for Master / Receiver Mode

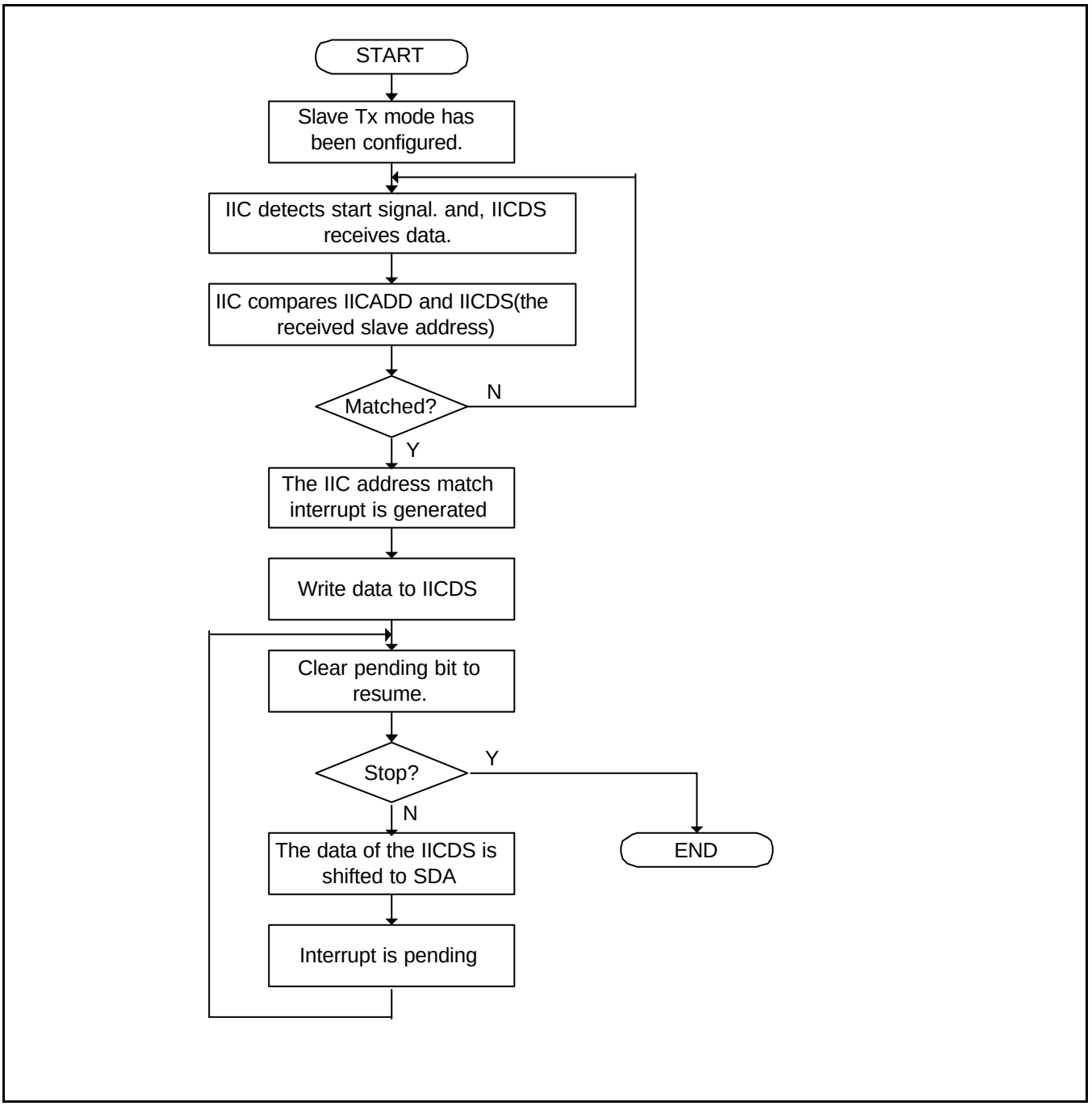

Figure 20-8 Operations for Slave / Transmitter Mode

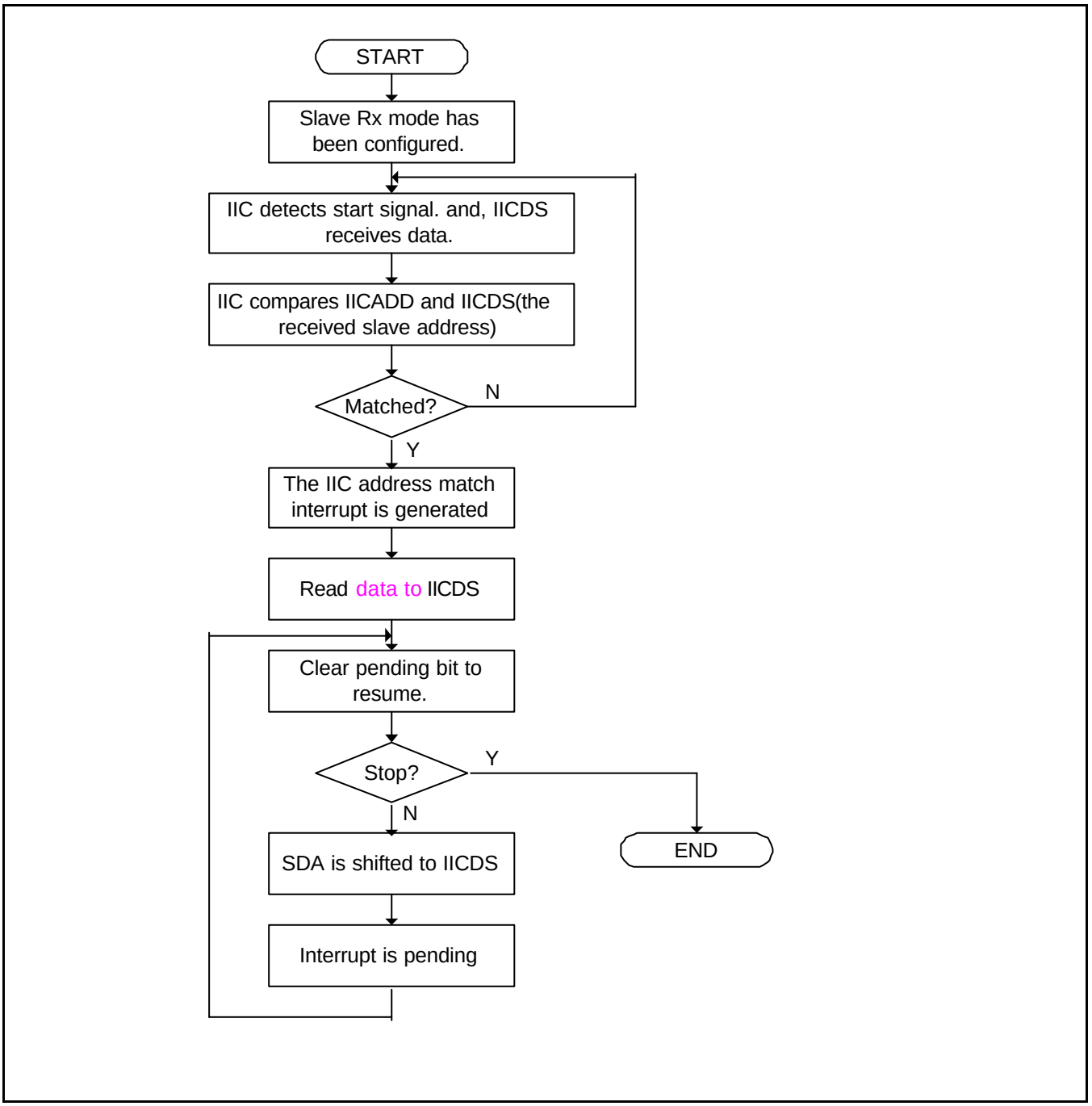

Figure 20-9 Operations for Slave / Receiver Mode

IIC-BUS INTERFACE SPECIAL REGISTERS

MULTI-MASTER IIC-BUS CONTROL REGISTER (IICCON)

Register	Address	R/W	Description	Reset Value
IICCON	0x54000000	R/W	IIC-Bus control register	0x0X

IICCON	Bit	Description	Initial State
Acknowledge generation (1)	[7]	IIC-bus acknowledge enable bit 0 = Disable 1 = Enable In Tx mode, the IICSDA is free in the ack time. In Rx mode, the IICSDA is L in the ack time.	0
Tx clock source selection	[6]	Source clock of IIC-bus transmit clock prescaler selection bit 0 = IICCLK = f_{PCLK}/16 1 = IICCLK = f_{PCLK}/512	0
Tx/Rx Interrupt (5)	[5]	IIC-Bus Tx/Rx interrupt enable/disable bit 0 = Disable, 1 = Enable	0
Interrupt pending flag (2) (3)	[4]	IIC-bus Tx/Rx interrupt pending flag. Writing 1 is impossible. When this bit is read as 1, the IICSCL is tied to L and the IIC is stopped. To resume the operation, clear this bit as 0. 0 = 1) No interrupt pending(when read), 2) Clear pending condition & Resume the operation (when write). 1 = 1) Interrupt is pending (when read) 2) N/A (when write)	0
Transmit clock value (4)	[3:0]	IIC-Bus transmit clock prescaler IIC-Bus transmit clock frequency is determined by this 4-bit prescaler value, according to the following formula: Tx clock = IICCLK/(IICCON[3:0]+1)	Undefined

NOTES:

1. Interfacing with EEPROM, the ack generation may be disabled before reading the last data in order to generate the STOP condition in Rx mode.
2. A IIC-bus interrupt occurs 1)when a 1-byte transmit or receive operation is completed, 2)when a general call or a slave address match occurs, or 3) if bus arbitration fails.
3. To time the setup time of IICSDA before IISSCL rising edge, IICDS has to be written before clearing the IIC interrupt pending bit.
4. IICCLK is determined by IICCON[6].
   Tx clock can vary by SCL transition time.
   When IICCON[6]=0, IICCON[3:0]=0x0 or 0x1 is not available.
5. If the IICON[5]=0, IICON[4] does not operate correctly.
   So, It is recommended to set IICCON[4]=1, although you does not use the IIC interrupt.

MULTI-MASTER IIC-BUS CONTROL/STATUS REGISTER (IICSTAT)

Register	Address	R/W	Description	Reset Value
IICSTAT	0x54000004	R/W	IIC-Bus control/status register	0x0

IICSTAT	Bit	Description	Initial State
Mode selection	[7:6]	IIC-bus master/slave Tx/Rx mode select bits: 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode	00
Busy signal status / START STOP condition	[5]	IIC-Bus busy signal status bit: 0 = read) Not busy(when read) write) STOP signal generation 1 = read) Busy(when read) write) START signal generation. The data in IICDS will be transferred automatically just after the start signal.	0
Serial output	[4]	IIC-bus data output enable/disable bit: 0 = Disable Rx/Tx, 1 = Enable Rx/Tx	0
Arbitration status flag	[3]	IIC-bus arbitration procedure status flag bit: 0 = Bus arbitration successful 1 = Bus arbitration failed during serial I/O	0
Address-as-slave status flag	[2]	IIC-bus address-as-slave status flag bit: 0 = Cleared when START/STOP condition was detected 1 = Received slave address matches the address value in the IICADD.	0
Address zero status flag	[1]	IIC-bus address zero status flag bit: 0 = Cleared when START/STOP condition was detected. 1 = Received slave address is 00000000b	0
Last-received bit status flag	[0]	IIC-bus last-received bit status flag bit 0 = Last-received bit is 0 (ACK was received) 1 = Last-received bit is 1 (ACK was not received)	0

MULTI-MASTER IIC-BUS ADDRESS REGISTER (IICADD)

Register	Address	R/W	Description	Reset Value
IICADD	0x54000008	R/W	IIC-Bus address register	0xXX

IICADD	Bit	Description	Initial State
Slave address	[7:0]	7-bit slave address, latched from the IIC-bus : When serial output enable = 0 in the IICSTAT, IICADD is write-enabled. The IICADD value can be read any time, regardless of the current serial output enable bit (IICSTAT) setting. Slave address = [7:1] Not mapped = [0]	XXXXXXXX

MULTI-MASTER IIC-BUS TRANSMIT/RECEIVE DATA SHIFT REGISTER (IICDS)

Register	Address	R/W	Description	Reset Value
IICDS	0x5400000C	R/W	IIC-Bus transmit/receive data shift register	0xXX

IICDS	Bit	Description	Initial State
Data shift	[7:0]	8-bit data shift register for IIC-bus Tx/Rx operation : When serial output enable = 1 in the IICSTAT, IICDS is write-enabled. The IICDS value can be read any time, regardless of the current serial output enable bit (IICSTAT) setting	XXXXXXXX

NOTES

21 IIS-BUS INTERFACE(PRELIMINARY)

OVERVIEW

Many digital audio systems are introduced into the consumer audio market, including compact disc, digital audio tapes, digital sound processors, and digital TV sound. The S3C2410X01 IIS(Inter-IC Sound) bus interface can be used to implement a CODEC interface to an external 8/16-bit stereo audio CODEC IC for mini-disc and portable applications. It supports the IIS bus data format and MSB-justified data format. IIS bus interface provides DMA transfer mode for FIFO access instead of an interrupt. It can transmit or receive data simultaneously as well as transmit or receive data only.

FEATURES

— IIS, MSB-justified format compatible

— 8/16-bit data per channel

— 16, 32, 48fs(sampling frequency) serial bit clock per channel

— 256, 384fs master clock

— Programmable frequency divider for master clock and CODEC clock

— 128 bytes(2 X 64) FIFO for transmit and receive

— Normal and DMA transfer mode

BLOCK DIAGRAM

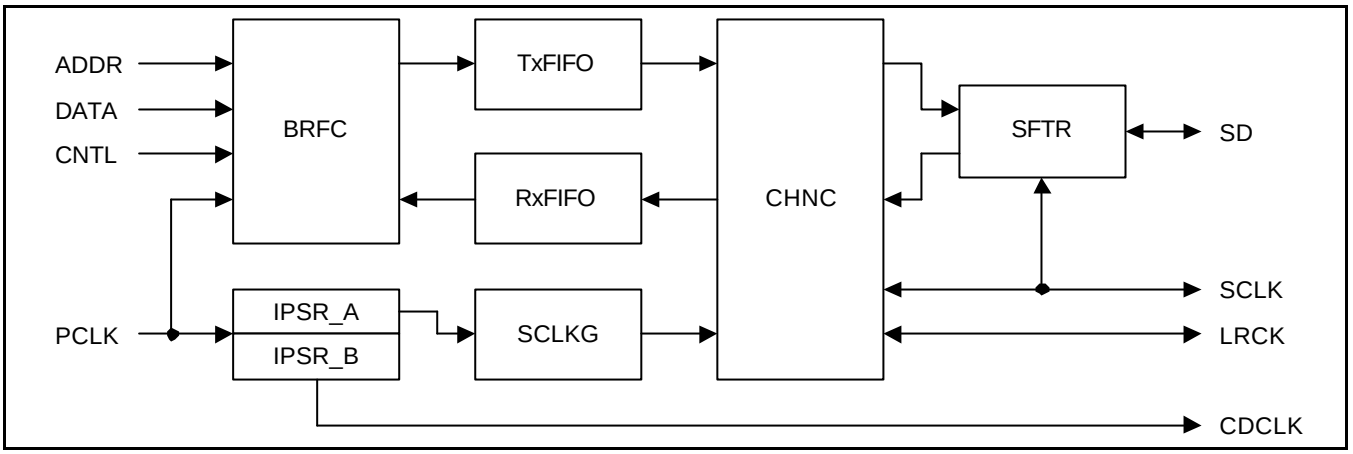

Figure 21-1. IIS-Bus Block Diagram

FUNCTIONAL DESCRIPTIONS

Bus interface, register bank, and state machine(BRFC) - Bus interface logic and FIFO access are controlled by the state machine.

5-bit dual prescaler(IPSR) - One prescaler is used as the master clock generator of the IIS bus interface and the other is used as the external CODEC clock generator.

64-byte FIFOs(TxFIFO, RxFIFO) - In transmit data transfer, data are written to TxFIFO, and, in the receive data transfer, data are read from RxFIFO.

Master IISCLK generator(SCLKG) - In master mode, serial bit clock is generated from the master clock.

Channel generator and state machine(CHNC) - IISCLK and IISLRCK are generated and controlled by the channel state machine.

16-bit shift register(SFTR) - Parallel data is shifted to serial data output in the transmit mode, and serial data input is shifted to parallel data in the receive mode.

TRANSMIT OR RECEIVE ONLY MODE

Normal transfer

IIS control register has FIFO ready flag bits for transmit and receive FIFO. When FIFO is ready to transmit data, the FIFO ready flag is set to '1' if transmit FIFO is not empty.
If transmit FIFO is empty, FIFO ready flag is set to '0'. When receive FIFO is not full, the FIFO ready flag for receive FIFO is set to '1' ; it indicates that FIFO is ready to receive data. If receive FIFO is full, FIFO ready flag is set to '0'. These flags can determine the time that CPU is to write or read FIFOs. Serial data can be transmitted or received while CPU is accessing transmit and receive FIFOs in this way.

DMA TRANSFER

In this mode, transmit or receive FIFO access is made by the DMA controller. DMA service request in transmit or receive mode is made by the FIFO ready flag automatically.

TRANSMIT AND RECEIVE MODE

In this mode, IIS bus interface can transmit and receive data simultaneously.

AUDIO SERIAL INTERFACE FORMAT

IIS-BUS FORMAT

The IIS bus has four lines, serial data input(IISDI), serial data output(IISDO), left/right channel select(IISLRCK), and serial bit clock(IISCLK); the device generating IISLRCK and IISCLK is the master.

Serial data is transmitted in 2's complement with the MSB first. The MSB is transmitted first because the transmitter and receiver may have different word lengths. It is not necessary for the transmitter to know how many bits the receiver can handle, nor does the receiver need to know how many bits are being transmitted.

When the system word length is greater than the transmitter word length, the word is truncated(least significant data bits are set to '0') for data transmission. If the receiver is sent more bits than its word length, the bits after the LSB are ignored. On the other hand, if the receiver is sent fewer bits than its word length, the missing bits are set to zero internally. And so, the MSB has a fixed position, whereas the position of the LSB depends on the word length. The transmitter always sends the MSB of the next word at one clock period after the IISLRCK change.

Serial data sent by the transmitter may be synchronized with either the trailing (HIGH to LOW) or the leading (LOW to HIGH) edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge.

The LR channel select line indicates the channel being transmitted. IISLRCK may change either on a trailing or leading edge of the serial clock, but it does not need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The IISLRCK line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word.

MSB(LEFT) JUSTIFIED

MSB / left justified bus has the same lines as the IIS format. It is only different with the IIS bus that transmitter always sends the MSB of the next word when the IISLRCK change.

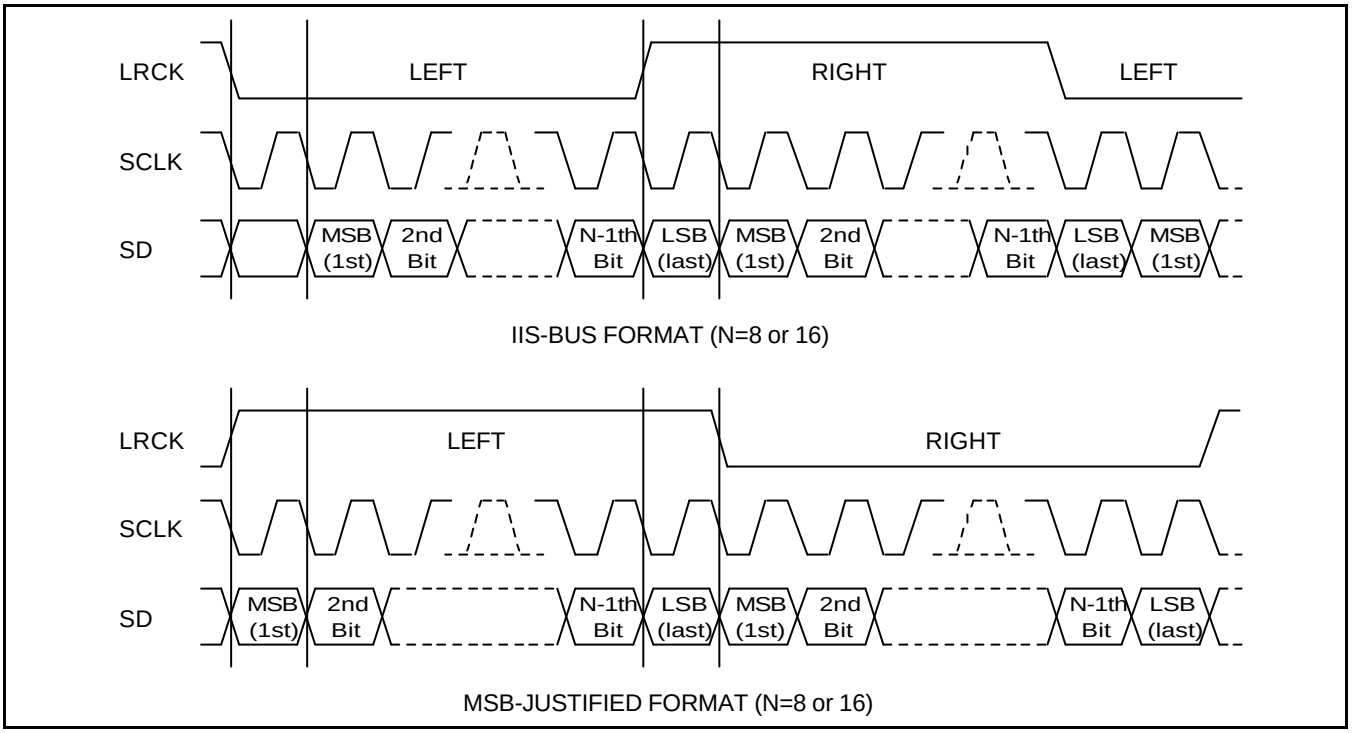

Figure 21-2. IIS-Bus and MSB(Left)-justified Data Interface Formats

SAMPLING FREQUENCY AND MASTER CLOCK

Master clock frequency(PCLK) can be selected by sampling frequency as shown in Table 21-1. Because PCLK is made by IIS prescaler, the prescaler value and PCLK type(256 or 384fs) should be determined properly. Serial bit clock frequency type(16/32/48fs) can be selected by the serial bit per channel and PCLK as shown in Table 21-2.

Table 21-1 CODEC clock (CODECLK = 256 or 384fs)

IISLRCK (fs)	8.000 KHz	11.025 KHz	16.000 KHz	22.050 KHz	32.000 KHz	44.100 KHz	48.000 KHz	64.000 KHz	88.200 KHz	96.000 KHz
CODECLK (MHz)	256fs									
	2.0480	2.8224	4.0960	5.6448	8.1920	11.2896	12.2880	16.3840	22.5792	24.5760
	384fs									
	3.0720	4.2336	6.1440	8.4672	12.2880	16.9344	18.4320	24.5760	33.8688	36.8640

Table 21-2 Usable serial bit clock frequency (IISCLK = 16 or 32 or 48fs)

Serial bit per channel	8-bit	16-bit
Serial clock frequency (IISCLK)		
@CODECLK = 256fs	16fs, 32fs	32fs
@CODECLK = 384fs	16fs, 32fs, 48fs	32fs, 48fs

IIS-BUS INTERFACE SPECIAL REGISTERS

IIS CONTROL REGISTER (IISCON)

Register	Address	R/W	Description	Reset Value
IISCON	0x15508000(Li/HW, Li/W, Bi/W) 0x15508002(Bi/HW)	R/W	IIS control register	0x100

IISCON	Bit	Description	Initial State
Left/Right channel index (Read only)	[8]	0 = Left 1 = Right	1
Transmit FIFO ready flag (Read only)	[7]	0 = Not ready (empty) 1 = Ready (not empty)	0
Receive FIFO ready flag (Read only)	[6]	0 = Not ready (full) 1 = Ready (not full)	0
Transmit DMA service request	[5]	0 = Disable 1 = Enable	0
Receive DMA service request	[4]	0 = Disable 1 = Enable	0
Transmit channel idle command	[3]	In Idle state the IISLRCK is inactive(Pause Tx) 0 = Not idle 1 = Idle	0
Receive channel idle command	[2]	In Idle state the IISLRCK is inactive(Pause Rx) 0 = Not idle 1 = Idle	0
IIS prescaler	[1]	0 = Disable 1 = Enable	0
IIS interface	[0]	0 = Disable (stop) 1 = Enable (start)	0

NOTES:

1. The IISCON register can be accessed by byte, halfword and word unit using STRB/STRH/STR and LDRB/LDRH/LDR instructions or char/short int/int type pointer in Little/Big endian mode.
2. (Li/HW/W) : Little/HalfWord/Word
   (Bi/HW/W) : Big/HalfWord/Word

IIS MODE REGISTER (IISMOD)

Register	Address	R/W	Description	Reset Value
IISMOD	0x15508004(Li/W, Li/HW, Bi/W) 0x15508006(Bi/HW)	R/W	IIS mode register	0x0

IISMOD	Bit	Description	Initial State
Master/slave mode select	[8]	0 = Master mode (IISLRCK and IISCLK are output mode) 1 = Slave mode (IISLRCK and IISCLK are input mode)	0
Transmit/receive mode select	[7:6]	00 = No transfer 01 = Receive mode 10 = Transmit mode 11 = Transmit and receive mode	00
Active level of left/right channel	[5]	0 = Low for left channel (High for right channel) 1 = High for left channel (Low for right channel)	0
Serial interface format	[4]	0 = IIS compatible format 1 = MSB(Left)-justified format	0
Serial data bit per channel	[3]	0 = 8-bit 1 = 16-bit	0
Master clock frequency select	[2]	0 = 256fs 1 = 384fs (fs : sampling frequency)	0
Serial bit clock frequency select	[1:0]	00 = 16fs 01 = 32fs 10 = 48fs 11 = N/A	00

NOTES:

1. The IISMOD register can be accessed by halfword and word unit using STRH/STR and LDRH/LDR instructions or short int/int type pointer in Little/Big endian mode.
2. (Li/HW/W) : Little/HalfWord/Word.
   (Bi/HW/W) : Big/HalfWord/Word.

IIS PRESCALER REGISTER (IISPSR)

Register	Address	R/W	Description	Reset Value
IISPSR	0x15508008(Li/HW, Li/W, Bi/W) 0x1550800A(Bi/HW)	R/W	IIS prescaler register	0x0

IISPSR	Bit	Description	Initial State
Prescaler control A	[9:5]	Data value : 0 ~ 31 NOTE : Prescaler A makes the master clock that is used the internal block and division factor is N+1.	00000
Prescaler control B	[4:0]	Data value : 0 ~ 31 NOTE : Prescaler B makes the master clock that is used the external block and division factor is N+1.	00000

NOTES:

1. The IISPSR register can be accessed by byte, halfword and word unit using STRB/STRH/STR and LDRB/LDRH/LDR instructions or char/short int/int type pointer in Little/Big endian mode.
2. (Li/HW/W) : Little/HalfWord/Word.
   (Bi/HW/W) : Big/HalfWord/Word.

IIS FIFO CONTROL REGISTER (IISFCON)

Register	Address	R/W	Description	Reset Value
IISFCON	0x1550800C(Li/HW, Li/W, Bi/W) 0x1550800E(Bi/HW)	R/W	IIS FIFO interface register	0x0

IISFCON	Bit	Description	Initial State
Transmit FIFO access mode select	[15]	0 = Normal 1 = DMA	0
Receive FIFO access mode select	[14]	0 = Normal 1 = DMA	0
Transmit FIFO	[13]	0 = Disable 1 = Enable	0
Receive FIFO	[12]	0 = Disable 1 = Enable	0
Transmit FIFO data count (Read only)	[11:6]	Data count value = 0 ~ 32	000000
Receive FIFO data count (Read only)	[5:0]	Data count value = 0 ~ 32	000000

NOTES:

1. The IISFCON register can be accessed by halfword and word unit using STRH/STR and LDRH/LDR instructions or short
   int/int type pointer in Little/Big endian mode.
2. (Li/HW/W) : Little/HalfWord/Word.
   (Bi/HW/W) : Big/HalfWord/Word.

IIS FIFO REGISTER (IISFIFO)

IIS bus interface contains two 16-byte FIFO for the transmit and receive mode. Each FIFO has 16-width and 24-depth form, which allows the FIFO to handles data by halfword unit regardless of valid data size. Transmit and receive FIFO access is performed through FIFO entry; the address of FENTRY is 0x15508010.

Register	Address	R/W	Description	Reset Value
IISFIFO	0x15508010(Li/HW) 0x15508012(Bi/HW)	R/W	IIS FIFO register	0x0

IISFIF	Bit	Description	Initial State
FENTRY	[15:0]	Transmit/Receive data for IIS	0x0

NOTES:

1. The IISFIFO register can be accessed by halfword and word unit using STRH and LDRH instructions or short int type pointer in Little/Big endian mode.
2. (Li/HW) : Little/HalfWord.
   (Bi/HW) : Big/HalfWord.

22 SPI INTERFACE (PRELIMINARY)

OVERVIEW

The S3C2410X01 Serial Peripheral Interface(SPI) can interface the serial data transfer. There are two SPI in S3C2410X01 and each SPI has two 8bit shift register for transmission and receiving, respectively. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially) 8bit serial data at a frequency determined by its corresponding control register settings. If you want only to transmit, you may treat the received data as dummy. Otherwise, if you want only to receive, you should transmit dummy '1' data.

There are 4 I/O pin signals associated with SPI transfers: the SCK, the MISO data line, the MOSI data line, and the active low /SS pin(input).

FEATURES

— SPI Protocol(ver 2.11) compatible

— 8-bit Shift Register for transmit

— 8-bit Shift Register for receive

— 8-bit Prescaler logic

— Polling, Interrupt, and DMA transfer mode

BLOCK DIAGRAM

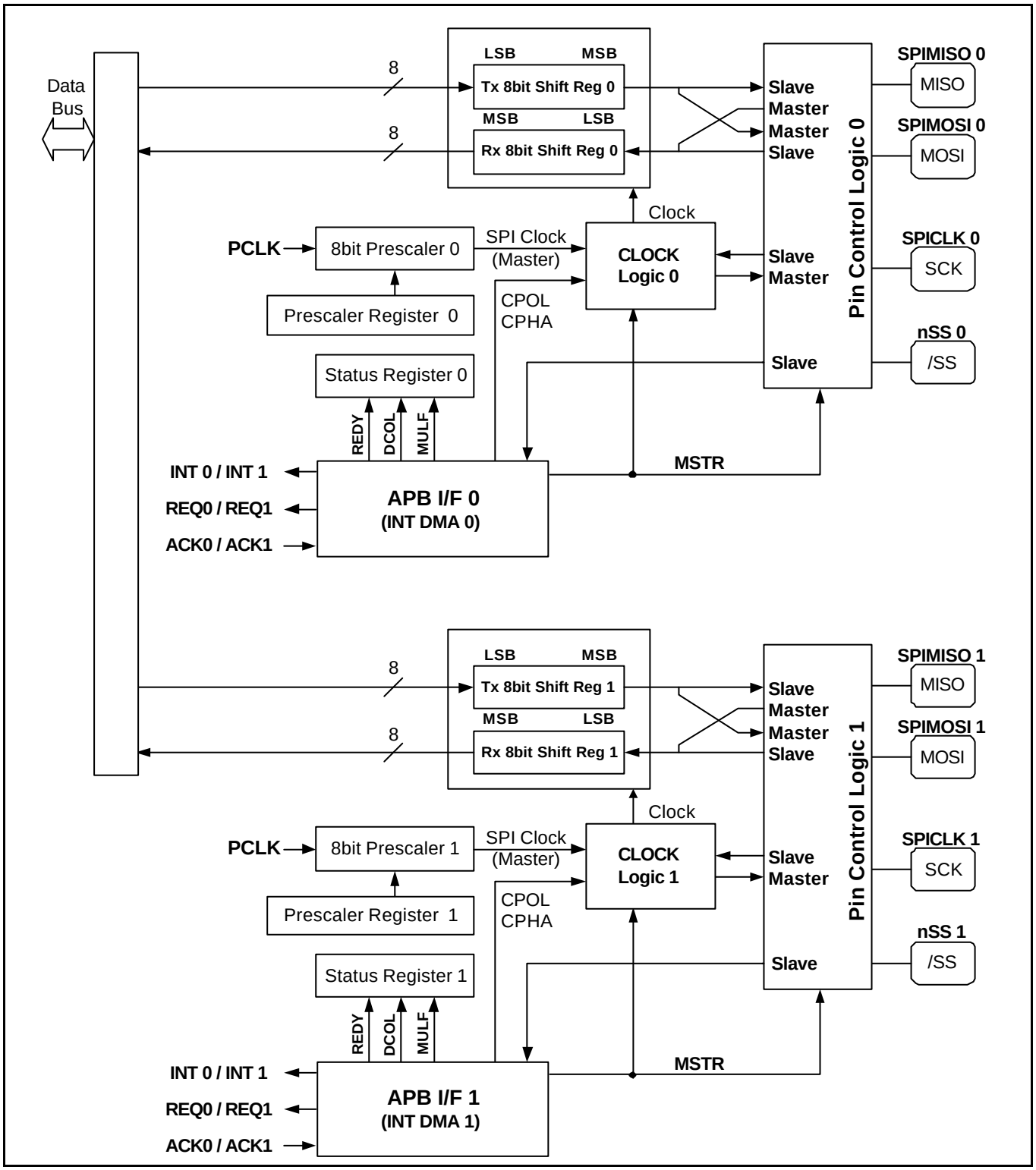

Figure 22-1. SPI Block Diagram

SPI OPERATION

Using the SPI interface, 8-bit data can be sending and receiving data simultaneously with an external device. A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. When SPI is the master, transmission frequency can be controlled by setting the appropriate bit to SPPREn register. You can modify its frequency to adjust the baud rate data register value. When SPI is a slave, other master supplies the clock. When a programmer writes byte data to SPTDATn register, SPI transmit and receive operation will start simultaneously. In some cases, nSS should be activated before writing byte data to SPTDATn.

Programming Procedure

When a byte data is written into the SPTDATn register, SPI starts to transmit if ENSCK and MSTR of SPCONn register are set. There is a typical programming procedure to operate an SPI card.

To program the SPI modules, follow these basic steps :

1. Set Baud Rate Prescaler Register(SPPREn)
2. Set SPCONn to configure properly the SPI module
3. Write data 0xFF to SPTDATn 10 times in order to initialize MMC or SD card
4. Set a GPIO pin, which acts as nSS, to low to activate the MMC or SD card.
5. Tx data → Check the status of Transfer Ready flag (REDY=1), and then write data to SPTDATn.
6. Rx data(1) : SPCONn's TAGD bit disable = normal mode

→ write 0xFF to SPTDATn, then confirm REDY to set, and then read data from Read Buffer

7. Rx data(2) : SPCONn's TAGD bit enable = Tx Auto Garbage Data mode

→ confirm REDY to set, and then read data from Read Buffer(then automatically start to transfer)

8. Set a GPIO pin, which acts as nSS, to high, to deactivate MMC or SD card.

SPI Transfer Format

S3C2410X01 supports 4 different format to transfer the data. Four waveforms are shown for SPICLK.

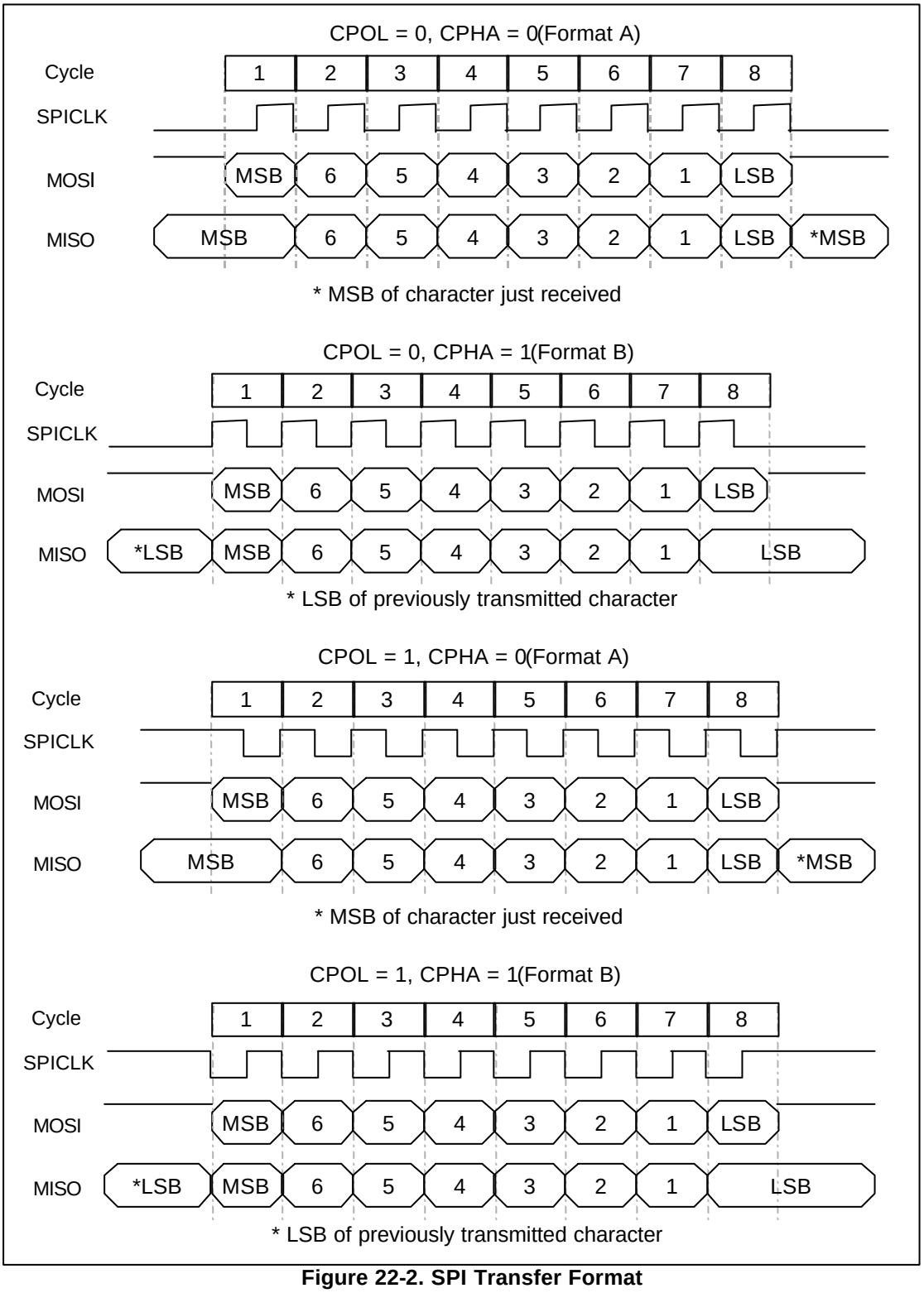

Figure 22-2. SPI Transfer Format

Steps for Transmit by DMA

1. The SPI is configured as DMA mode.
2. DMA is configured properly.
3. The SPI requests DMA service.
4. DMA transmits 1byte data to the SPI.
5. The SPI transmits the data to card.
6. Go to step 3 until DMA count is 0.
7. The SPI is configured as interrupt or polling mode with SMOD bits.

Steps for Receive by DMA

1. The SPI is configured as DMA start with SMOD bits and setting TAGD bit.
2. DMA is configured properly.
3. The SPI receives 1byte data from card.
4. The SPI requests DMA service.
5. DMA receives the data from the SPI.
6. Write data 0xFF automatically to SPTDATn.
7. Go to step 4 until DMA count is 0.
8. The SPI is configured as polling mode with SMOD bits and clearing TAGD bit.
9. If SPSTAn' s REDY flag is set, then read the last byte data.

NOTE: Total received data = DMA TC values + The last data in polling mode(step 9).
First DMA received data is dummy, so user can neglect that.

SPI SPECIAL REGISTERS

SPI CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
SPCON0	0x59000000	R/W	SPI Channel 0 Control Register	0x00
SPCON1	0x59000020	R/W	SPI Channel 1 Control Register	0x00

SPCONn	Bit	Description	Initial State
SPI Mode Select (SMOD)	[6:5]	Determines how and by what SPTDAT is read/written 00 = polling mode, 01 = interrupt mode 10 = DMA mode, 11 = reserved	00
SCK Enable (ENSCK)	[4]	Determines what you want SCK enable or not(only master) 0 = disable, 1 = enable	0
Master/Slave Select(MSTR)	[3]	Determines what mode you want master or slave 0 = slave, 1 = master **NOTE:** In slave mode, there should be set up time for master to initiate Tx / Rx.	0
Clock Polarity Select(CPOL)	[2]	Determines an active high or active low clock. 0 = active high, 1 = active low	0
Clock Phase Select(CPHA)	[1]	This bit selects one of two fundamentally different transfer formats. 0 = format A, 1 = format B	0
Tx Auto Garbage Data mode enable (TAGD)	[0]	This bit decides whether the receiving data only needs or not. 0 = normal mode, 1 = Tx auto garbage data mode **NOTE:** In normal mode, you only want to receive data, you should transmit dummy 0xFF data.	0

SPI STATUS REGISTER

Register	Address	R/W	Description	Reset Value
SPSTA0	0x59000004	R	SPI Channel 0 Status Register	0x01
SPSTA1	0x59000024	R	SPI Channel 1 Status Register	0x01

SPSTAn	Bit	Description	Initial State
Reserved	[7:3]		
Data Collision Error Flag(DCOL)	[2]	This flag is set if the SPTDATn is written or the SPRDATn is read while a transfer is in progress and cleared by reading the SPSTAn. 0 = not detect, 1 = collision error detect	0
Multi Master Error Flag (MULF)	[1]	This flag is set if the nSS signal goes to active low while the SPI is configured as a master, and SPPINn's ENMUL bit is multi master errors detect mode. MULF is cleared by reading SPSTAn. 0 = not detect, 1 = multi master error detect	0
Transfer Ready Flag (REDY)	[0]	This bit indicates that SPTDATn or SPRDATn is ready to transmit or receive. This flag is automatically cleared by writing data to SPTDATn. 0 = not ready, 1 = data Tx/Rx ready	1

SPI PIN CONTROL REGISTER

When the SPI system is enabled, the direction of pins is controlled by MSTR bit of SPCONn register except nSS pin. The direction of nSS pin is input always.
When the SPI is a master, nSS pin is used to check multi-master error, provided the SPPIN's ENMUL bit is active, and another GPIO should be used to select a slave.
If the SPI is configured as a slave, nSS pin is used to select SPI as a slave by one master.

Register	Address	R/W	Description	Reset Value
SPPIN0	0x59000008	R/W	SPI Channel 0 Pin Control Register	0x02
SPPIN1	0x59000028	R/W	SPI Channel 1 Pin Control Register	0x02

SPPINn	Bit	Description	Initial State
Reserved	[7:3]		
Multi Master error detect Enable (ENMUL)	[2]	The /SS pin is used as an input to detect multi master error when the SPI system is a master. 0 = disable(general purpose), 1 = multi master error detect enable	0
Reserved	[1]	This bit should be ‘ 1’ .	1
Master Out Keep(KEEP)	[0]	Determines MOSI drive or release when 1byte transmit finish(only master) 0 = release, 1 = drive the previous level	0

The SPIMISO(MISO) and SPIMOSI(MOSI) data pins are used for transmitting and receiving serial data. When the SPI is configured as a master, SPIMISO(MISO) is the master data input line, SPIMOSI(MOSI) is the master data output line, and SPICLK(SCK) is the clock output line. When as a slave, these pins reverse roles. In a multiple-master system, all SPICLK(SCK) pins are tied together, all SPIMOSI(MOSI) pins are tied together, and all SPIMISO(MISO) pins are tied together.

Only an SPI master can experience a multi master error, caused when a second SPI device becomes a master and selects this device as if it were a slave. When this type error is detected, the following actions are taken immediately. But you must previously set SPPINn’ s ENMUL bit if you want to detect this error.

1. The SPCONn's MSTR bit is forced to 0 to operate slave mode.
2. The SPSTAn's MULF flag is set, and an SPI interrupt is generated.

SPI Baud Rate Prescaler Register

Register	Address	R/W	Description	Reset Value
SPPRE0	0x5900000C	R/W	SPI Cannel 0 Baud Rate Prescaler Register	0x00
SPPRE1	0x5900002C	R/W	SPI Cannel 1 Baud Rate Prescaler Register	0x00

SPPREn	Bit	Description	Initial State
Prescaler Value	[7:0]	Determines SPI clock rate as above equation. Baud rate = PCLK / 2 / (Prescaler value + 1)	0x00

NOTE: Baud rate should be less than 25MHz.

SPI Tx Data Register

Register	Address	R/W	Description	Reset Value
SPTDAT0	0x59000010	R/W	SPI Channel 0 Tx Data Register	0x00
SPTDAT1	0x59000030	R/W	SPI Channel 1 Tx Data Register	0x00

SPTDATn	Bit	Description	Initial State
Tx Data Register	[7:0]	This field contains the data to be transmitted over the SPI channel	0x00

SPI Rx Data Register

Register	Address	R/W	Description	Reset Value
SPRDAT0	0x59000014	R	SPI Channel 0 Rx Data Register	0x00
SPRDAT1	0x59000034	R	SPI Channel 1 Rx Data Register	0x00

SPRDATn	Bit	Description	Initial State
Rx Data Register	[7:0]	This field contains the data to be received over the SPI channel	0x00

23 NAND FLASH CONTROLLER(Preliminary)

OVERVIEW

Recently, the NOR flash memory is expensive and SDRAM and NAND flash memory is inexpensive, some users want to execute boot code on NAND flash and execute the main code on SDRAM.

S3C2410X01 boot code can be executed on external NAND flash memory. In order to support NAND flash boot loader, there is an internal SRAM buffer. This internal SRAM buffer is called ‘ Steppingstone’ . When booting, the first 4-KB of the NAND flash memory will be loaded into Steppingstone and the boot code loaded into Steppingstone will be executed.

Generally, the boot code will copy NAND flash content to SDRAM. Using H/W ECC, the NAND flash data validity will be checked. After the copy, the main program will be executed on the SDRAM.

FEATURES

— NAND Flash mode: Support read/erase/program NAND flash memory

— Auto boot mode: The boot code is transferred into Steppingstone during reset duration. After the transfers, the boot code will be executed on the Steepingstone(Supports only little endian mode).

— Hardware ECC detecting block(H/W detecting and S/W correcting)

— The Steppingstone 4-KB internal SRAM buffer can be used for another purpose after NAND flash booting.

BLOCK DIAGRAM

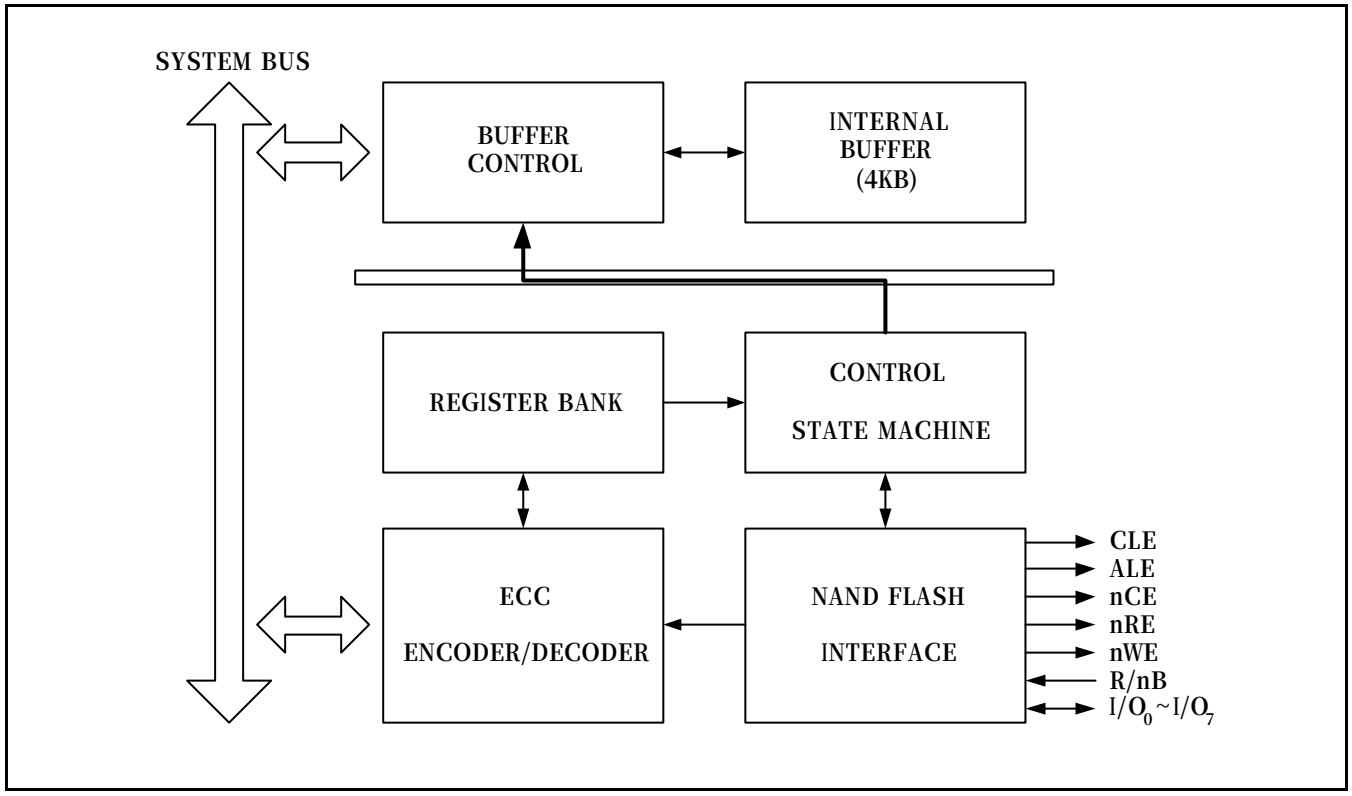

Figure 23-1. NAND Flash Controller Block Diagram

OPERATION SCHEME

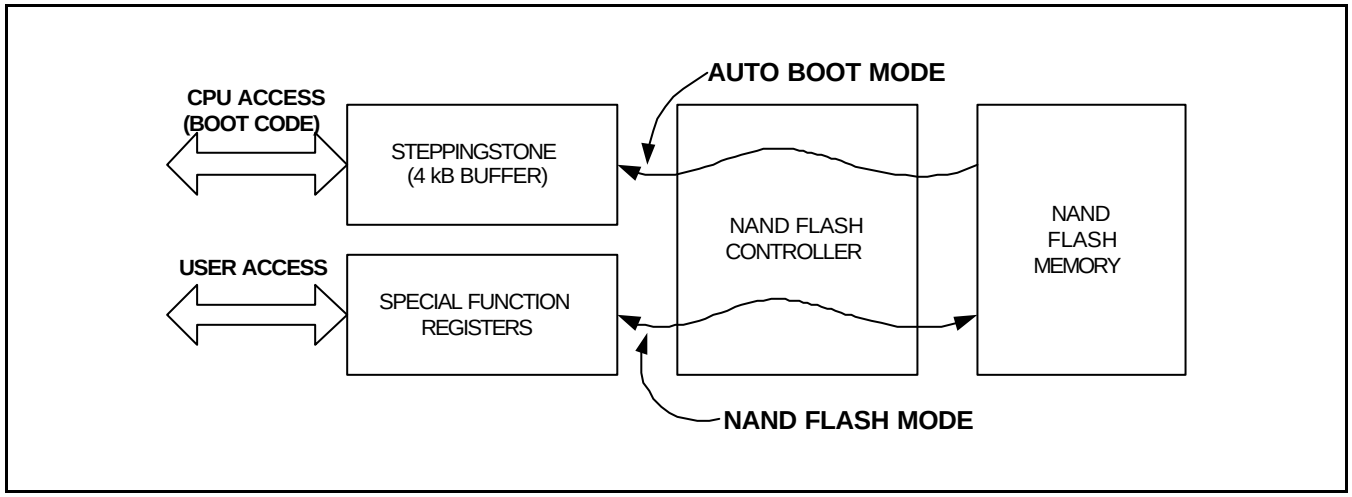

Figure 23-2. NAND Flash Operation Scheme

AUTO BOOT MODE SEQUENCE

1) Hardware reset is asserted.
2) If the auto boot mode is enabled, the first 4-KB of NAND flash memory is copied onto Steppingstone 4-KB internal buffer.
3) The Steppingstone is mapped to nGCS0
4) Hardware reset is released.
5) CPU starts to execute the boot code on the Steppingstone 4-KB internal buffer.

NOTE: During the auto boot mode, the ECC is not checked. So, The first 4-KB of NAND flash should have no bit error.

NAND FLASH MODE

1) Configure NAND flash configuration by NF_CONF register.
2) Write NAND flash command onto NF_CMD register.
3) Write NAND flash address onto NF_ADR register.
4) Read/Write data while checking NAND flash status by NF_STA register. R/nB signal should be checked before read operation or after program operation.

NAND FLASH MEMORY TIMING

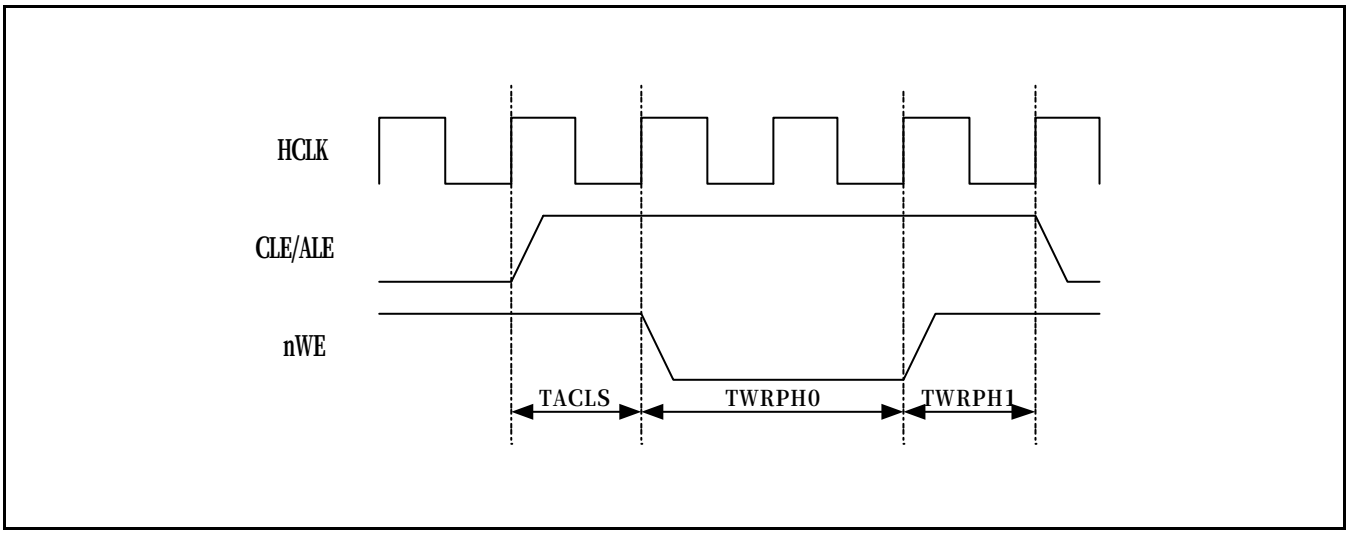

Figure 23-3. TACLS=0, TWRPH0=1, TWRPH1=0

PIN CONFIGURATION

D[7:0] : Data/Command/Address In/Out Port(shared with the data bus)

CLE : Command Latch Enable(Output)

ALE : Address Latch Enable(Output)

NFCE : NAND Flash Chip Enable(Output)

nFRE : NAND Flash Read Enable(Output)

nFWE : NAND Flash Write Enable(Output)

nWAIT : NAND Flash Ready/nBusy(Input)

BOOT AND NAND FLASH CONFIGURATIONS

1) OM[1:0] = 00b : Enable NAND Flash controller auto boot mode

2) NCON[0]: NAND Flash memory page size selection

0 : 256 Bytes/Page

1 : 512 Bytes/Page

3) NCON[1]: NAND Flash memory address step selection

0 : 3 Step addressing

1 : 4 Step addressing (for future device)

512 BYTE ECC PARITY CODE ASSIGNMENT TABLE

	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
ECC0	P64	P64’	P32	P32’	P16	P16’	P8	P8’
ECC1	P1024	P1024’	P512	P512’	P256	P256’	P128	P128’
ECC2	P4	P4’	P2	P2’	P1	P1’	P2048	P2048’

S3C2410 generates 512 bytes ECC Parity Code during Write / Read operation. ECC Parity Code consists of 3byte per 512byte data.

24bit ECC Parity Code = 18bit Line parity + 6bit Column Parity

ECC generator block executes the followings:

1) When MCU writes data to NAND, ECC generator block generates ECC code.
2) When MCU reads data from NAND, ECC generator block generates ECC code and compare it with pre-written ECC code.

NAND FLASH MEMORY MAPPING

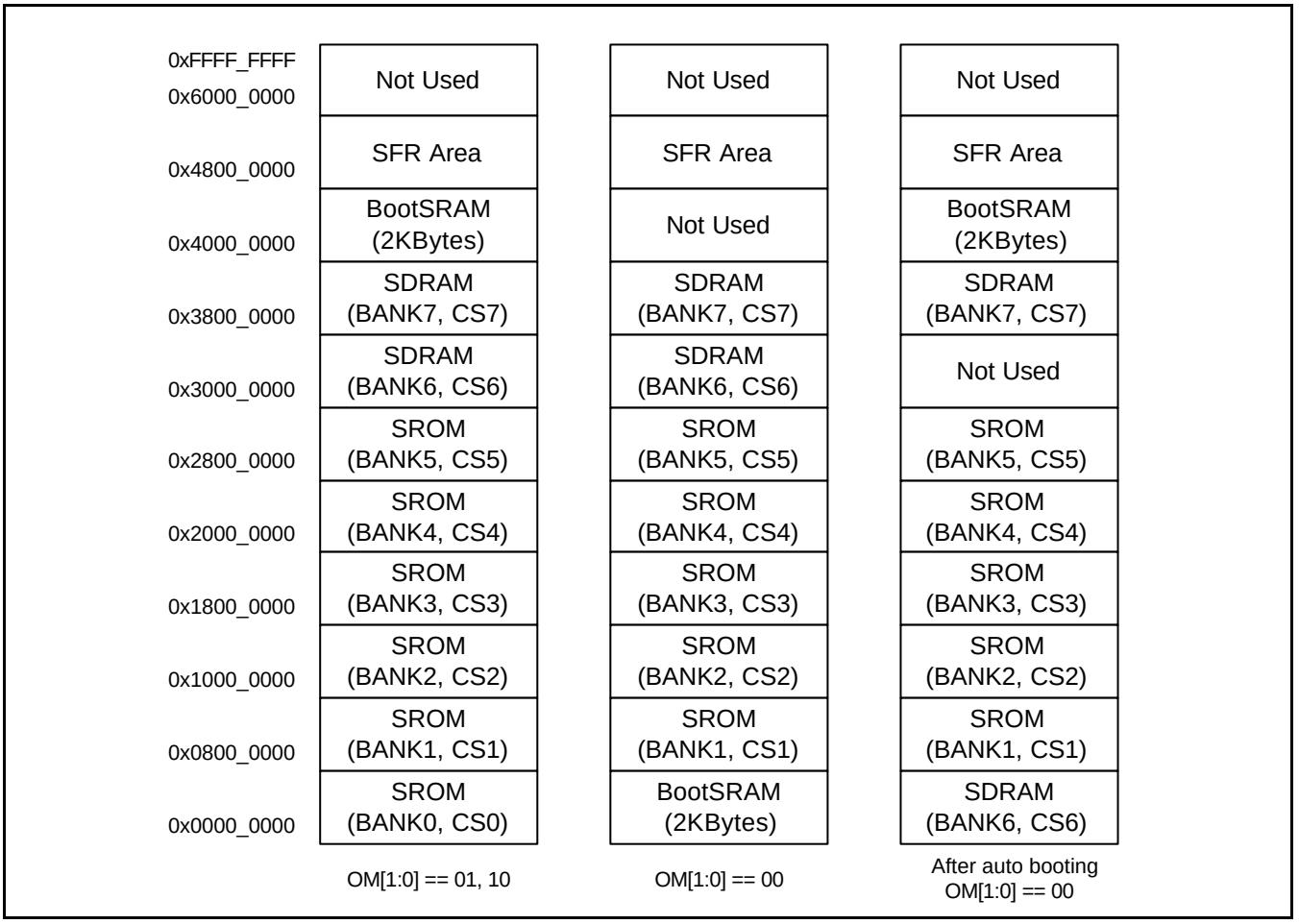

Figure 23-4. NAND Flash Memory Mapping

SPECIAL FUNCTION REGISTERS

NAND FLASH CONFIGURATION REGISTER(NF_CONF)

Register	Address	R/W	Description	Reset Value
NF_CONF	0x4e00_0000	R/W	NAND Flash configuration	–

NF_CONF	Bit	Description	Initial State
Enable/Disable	[15]	NAND Flash controller enable/disable 0 = Disable NAND Flash Controller 1 = Enable NAND Flash Controller After auto-boot, this bit is cleared to 0 automatically. If users want to access NAND flash memory, this bit must be set.	–
Auto load page size(Read only)	[14]	Auto Load Page Size of NAND Flash Memory 0 : 256 Bytes 1 : 512 Bytes	–
Addressing step (Read only)	[13]	Addressing step of NAND Flash Memory 0 : 3 Step address 1 : 4 Step address (for future device)	–
Initialize ECC	[12]	Initialize ECC decoder/encoder 0 : Not initialize ECC 1 : Initialize ECC (S3C2410 supports only 512bytes ECC checking so users should initialize ECC each 512bytes.)	0
NAND Flash Memory chip enable	[11]	NAND Flash Memory nFCE control 0 : NAND flash nFCE = L(active) 1 : NAND flash nFCE = H(inactive) (After auto-boot, nCE will be inactive.)	–
TACLS	[10:8]	CLE & ALE duration setting value(0~7) Duration = HCLK * (TACLS + 1)	
Reserved	[7]	Reserved	–
TWRPH0	[6:4]	TWRPH0 duration setting value(0~7) Duration = HCLK * (TWRPH0 + 1)	0
Reserved	[3]	Reserved	–
TWRPH1	[2:0]	TWRPH1 duration setting value(0~7) Duration = HCLK * (TWRPH1 + 1)	0

NAND FLASH COMMAND SET REGISTER(NF_CMD)

Register	Address	R/W	Description	Reset Value
NF_CMD	0x4e00_0004	R/W	NAND flash command set register	–

NF_CMD	Bit	Description	Initial State
Reserved	[15:8]	Reserved	–
Command	[7:0]	NAND Flash memory command value	0x00

NAND FLASH ADDRESS SET REGISTER(NF_ADR)

Register	Address	R/W	Description	Reset Value
NF_ADR	0x4e00_0008	R/W	NAND flash address set register	–

NF_ADR	Bit	Description	Initial State
Reserved	[15:8]	Reserved	–
Address	[7:0]	NAND flash memory address value	0x00

NAND FLASH DATA REGISTER(NF_DAT)

Register	Address	R/W	Description	Reset Value
NF_DAT	0x4e00_000c	R/W	NAND flash data register	–

NF_DAT	Bit	Description	Initial State
Reserved	[15:8]	Reserved	–
Data	[7:0]	NAND Flash read/program data value In case of write: Programming data In case of read: Read data.	–

NAND FLASH OPERATION STATUS REGISTER(NF_STA)

Register	Address	R/W	Description	Reset Value
NF_STA	0x4e00_0010	R	NAND Flash operation status	–

NF_STA	Bit	Description	Initial State
Auto-boot Done	[15]	Auto-boot mode operation completed Flag 0 : Not yet completed 1 : Auto boot operation is completed	–
Reserved	[14:12]	Reserved	–
CLE	[11]	CLE pin status	–
ALE	[10]	ALE pin status	–
nFRE	[9]	nFRE pin status	–
nFWE	[8]	nFWE pin status	–
Reserved	[7:1]	Reserved	–
RnB	[0]	NAND Flash memory ready/busy status. (This signal is checked through nWAIT pin.) 0 = NAND Flash memory busy 1 = NAND Flash memory ready to operate	–

NAND FLASH ECC REGISTER (NF_ECC)

Register	Address	R/W	Description	Reset Value
NF_ECC	0x4e00_0014	R/W	NAND Flash ECC(Error Correction Code) register	–

NF_ADDR	Bit	Description	Initial State
ECC2	[23:16]	Error Correction Code #2	–
ECC1	[15:8]	Error Correction Code #1	–
ECC0	[7:0]	Error Correction Code #0	–

25 MECHANICAL DATA (PRELIMINARY)

PACKAGE DIMENSIONS

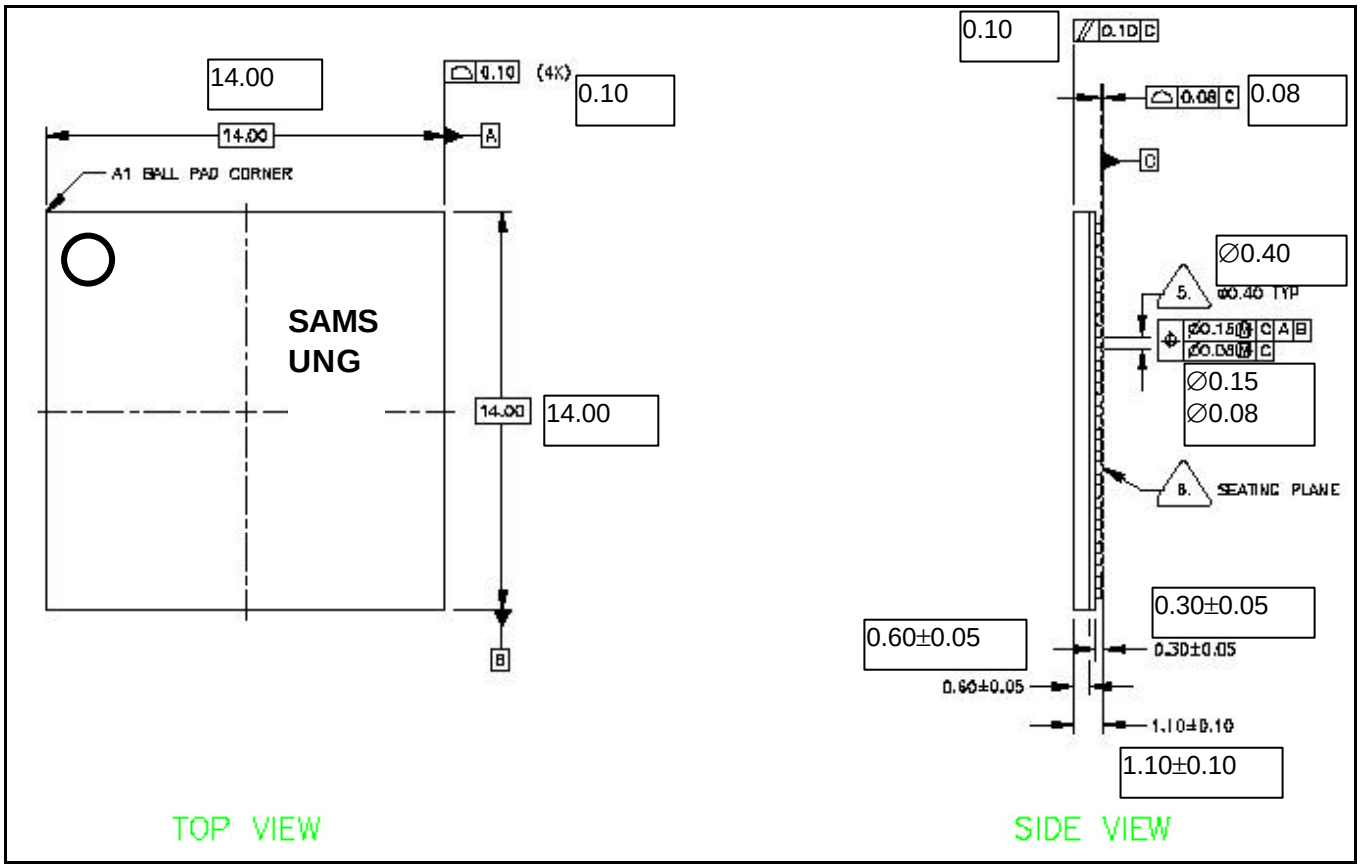

Figure 25-1. 272 PBGA Package Dimension 1

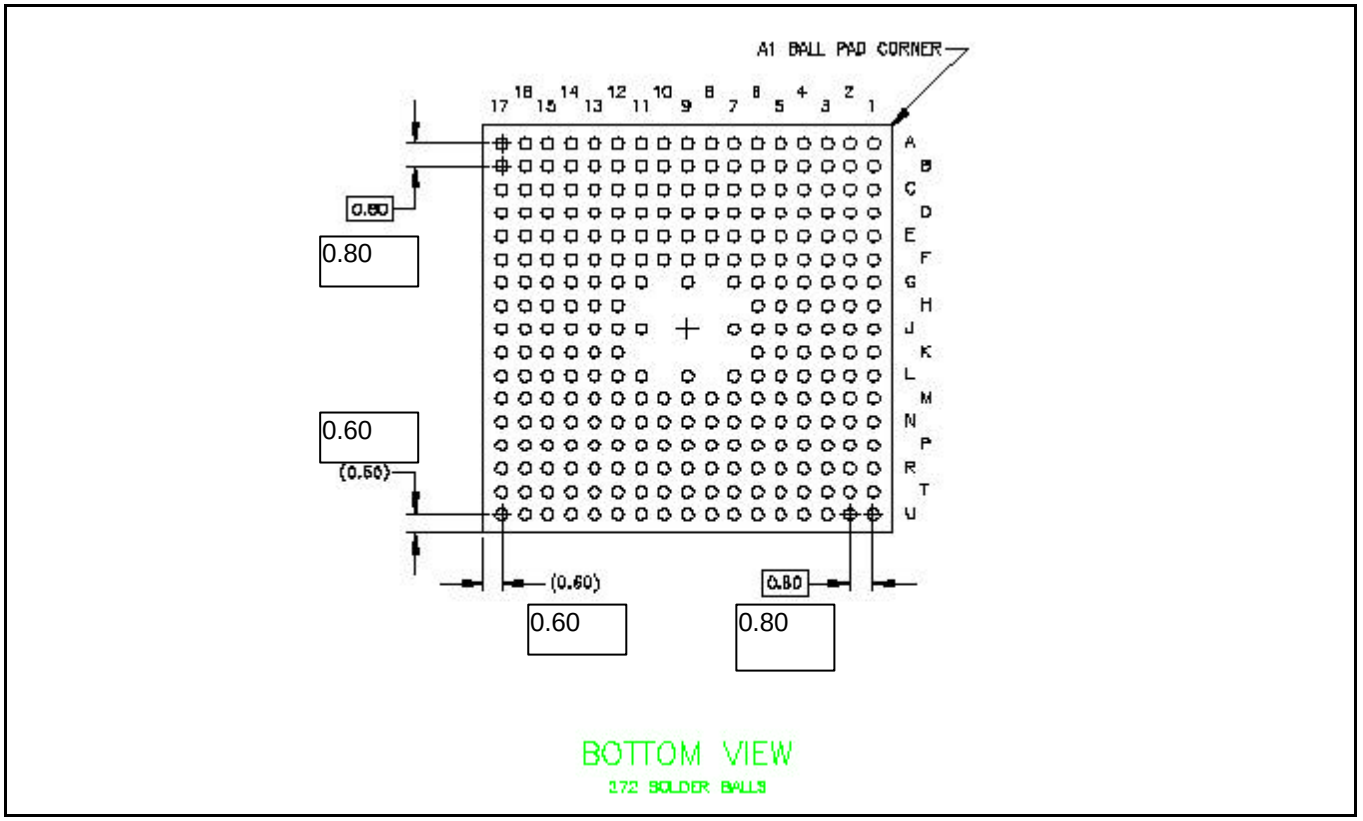

Figure 25-2. 272 PBGA Package Dimension 2