SAMSUNG ELECTRONICS

H/W Design Guide

S3C2440A

32-Bit RISC Microprocessor

October, 2007

REV 1.0

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S3C2440A 32-BIT RISC Microprocessor
H/W Design Guide, Revision 1.0

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0.2	Second Release. (Preliminary)	-	O. P. Shin	February,2005
1.0	Changed form. Updated on Page 3-7, 4-27, 4-28 and 6-1.	-	O. P. Shin S. Kim	October, 2007

This document presents design recommendations for the S3C2440A application processor. The S3C2440A application processor is the 32-bit version of the device. The guidelines presented in this document ensure maximum flexibility for board designers, while reducing the risk of board-related issues.

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1 INTRODUCTION

1. RELATED DOCUMENTATION

Reference the following documents for more information.

— S3C2440A User's Manual
— S3C2440A Application Notes

2. TERMINOLOGY

Terminology	Definition
Amplitude	Height of wave in waveform that is regularly changed. In other words, it means distance from the lowest to the highest part of waveform.
Bidirectional	Possible to transmit signal in both ways of the circuit. Driver and receiver device pins are connected to both ends of the circuit.
Buried Via	Via technique allowing connection from inner layer to inner layer of PCB, which is buried under the external surface of PCB. It is also used for interconnection of micro blind vias.
Capacitance	Capability to store charge. For electrostatic capacitance, unit “Farad” is used; 1 Farad means capability to store 1 C charge by using 1V voltage.
Crosstalk	A phenomenon that different circuit signals have effects on other signals by electric association. It may directly cause the deterioration of signal quality.
Damping	As time goes by, strength of signal (amplitude) is reduced.
Distortion	Transformation of signals generated between signal input and signal output from electronic circuit. This signal distortion indicates that waveform is changed to undesired form.
EMC	Electro Magnetic Compatibility, meaning electro magnetic phenomenon generated from PCB circuit.
Fan Out	The size of load that the device output can drive. It is expressed as the number of output lines to distribute the output of one gate in the electronic circuit.
FET	The Field Effect Transistor, being operated only by multiple carriers, is composed of unipolar element and characterized by voltage control system and slow operation speed.
Flight Time	Time taken for signal generated from the source terminal to reach the destination terminal: signal delay is generated by the length and thickness of cable and PCB dielectric constant. It is also called “Trace Propagation Delay Time”, which may cause Logic Function Error.
Glitch	Usual noise that seems like A Single Pulse, which can cause logical malfunctions.
Ground Bounce	Generated by the inductance element of power cable and as the result of change in current upon switching.
Impedance	Electric characteristics that all conductors have. If voltage is assigned between two conductors, it means resistance that prevents current stream. In case of PCB board or multichip module, the conductor could be regarded as a signal-layer pattern, and the other one as the power plane or ground plane.

2. TERMINOLOGY (Continued)

Terminology	Definition
Impedance Coupon	Designed to measure and check Trace Impedance on PCB.
Impedance Matching	The process of equalizing impedance on both circuits so that return loss cannot be generated if different circuits are connected. If Impedance does not match, signal is distorted or reflected wave is generated.
Impedance Mismatching	Mostly caused by Trace Branch (Topology), Termination, L.C Effect and Trace Impedance.
Inductance	If current is assigned to the coil after winding coil on the stick, there is an attribute to interfere current stream in the coil, which is called “Inductance”, and Henry (H) is used as its unit.
ISI	Inter-Symbol Interference (ISI) means that signal is affected if it is not in Steady State even until Next Cycle gets started. This effect causes the change of Flight Time and the increase of skew between signals, and consequently it may result in less timing margin.
Latency	Time taken for signal to move through the circuit.
LVDS	Low Voltage Differential Signaling (LVDS) means that signal with narrow width of voltage Swing (0.3 ~ 0.6V) is sent with DC level (1.2V) at differential pair, and the receiving party detects difference between the two signals.
Measuring Signal Delay	Multiple receivers often see different signals at different times. The worst-case settling time defines the maximum net delay.
Micro Blind Via	The way to minimize the size of via by forming ‘via’ using very small-sized laser-drill (usually 4um).
Microstrip Line	The signal line is placed on the outer layer and the ground plane is placed at the next neighboring layer.
Monotonicity	A factor for analyzing whether the rising or falling waveform is linear. Non-monotonic waveform around thresholds can cause logical malfunctions.
Network	Electrically connected between more than 2 components on Printed Circuit Board (PCB). The circuit is composed of basic circuit components (impedance, capacity, and inductance).
Network Length	Length of circuit connected between pads of the two Components.
Oscillation	Occurs when a signal displays non-monotonic behavior between the high and low threshold region.

2. TERMINOLOGY (Continued)

Terminology	Definition
Overshoot	Temporary phenomenon in which output waveform goes above the maximum base line if pulse waveform goes up in the electronic circuit (that is, signal exceeds the maximum voltage (Vdd) of the device pad). Excessive Under/Over Shoot has proportionally severe ring-back noise and the receiver component might be damaged.
Pad	Part created for wiring from the outside on Chip or PCB.
Pin	point of component package where it is possible to measure Signal Quality/ timing, and connect trace on the board.
Propagation	Refers to a phenomenon that signal and information generated from one place move to another place. For example, signal generated from Tx party through communication line is delivered to the Rx party. In addition, signal from one logic element in logic circuit is transmitted to the input of other logic elements.
Reflection Noise	Generated by the impedance mismatching of wiring and circuit element.
Ring-back	Noise rebound in reverse direction after Under/Overshoot. It might cause a functional failure due to logic violation. Based on High/Low Threshold Voltage, it is required to analyze how much margin exists.
Ringing	Waveform of output circuit is temporarily unstable because of a sudden change of input signal in electric/electronic circuits. It refers to noise rebound in reverse direction after Under/Overshoot and might cause a functional failure due to logic violation. Based on High/Low threshold voltage, it is required to analyze how much margin exits.
Schmitt-trigger	For signal received from input end, reference electrical potential is set up in advance. If input exceeds reference electrical potential, the circuit outputs value “1”, and if input signal is less than reference electrical potential, it outputs value “0”.
Settling Time	Level (Setting Limit) that does not cause the increase of next transition flight time, and it means time until oscillation is weakened.
Skew	Time difference generated between multiple signals. Multiple signals may have quite a big time difference at destination point due to the difference of load condition in the path. For sequential circuit, if you want to increase dynamic frequency, it is absolutely important to reduce clock skew.
SSO	Simultaneous Switching Output (SSO) Noise means that if all bits are changed to Vdd or Vss in the output circuit at the same time, there will be a big change of current in power circuit in a moment, and at this time, Ground Bounce is generated by inductance element on the ground side.

2. TERMINOLOGY (Continued)

Terminology	Definition
Stack-Up	Layer layout between layers on PCB.
Strip line	Signal line is inserted between upper and lower power planes in order to implement transmission line.
TBD	To Be Defined
Topology	Overall architecture of each device connected through any communication medium. For example, the architecture of peripherals connected through bus or that of computer connected through data communication network.
Undershoot	Temporary phenomenon in which output waveform goes below the minimum base line if pulse waveform drops in the electronic circuit (that is, signal does not exceed the minimum voltage (Vss) of the device pad). Excessive Under/Over Shoot proportionally has severe ring-back noise and the receiver component might be damaged.

NOTES

2 SYSTEM CONFIGURATIONS

1. BLOCK DIAGRAM

The S3C2440A includes the following components:

- Around 1.2V internal, 1.8V/2.5V/3.3V memory, 3.3V external I/O microprocessor with 16KB I-Cache/16KB D-Cache/MMU
- External memory controller (SDRAM Control and Chip Select logic)
- LCD controller (up to 4K color STN and 256K color TFT) with LCD-dedicated DMA
- 4-ch DMA controllers with external request pins
- 3-ch UARTs (IrDA1.0, 64-Byte Tx FIFO, and 64-Byte Rx FIFO)
- 2-ch SPIs
- IIC bus interface (multi-master support)
- IIS Audio CODEC interface
- AC'97 CODEC interface
- SD Host interface version 1.0 & MMC Protocol version 2.11 compatible
- 2-ch USB Host controller / 1-ch USB Device controller (Ver 1.1)
- 4-ch PWM timers / 1-ch Internal timer / Watch Dog Timer
- 8-ch 10-bit ADC and Touch screen interface
- RTC with calendar function
- Camera interface (Max. 4096 x 4096 pixels input support. 2048 x 2048 pixel input support for scaling)
- 130 General Purpose I/O ports / 24-ch external interrupt source
- Power control: Normal, Slow, Idle and Sleep mode
- On-chip clock generator with PLL

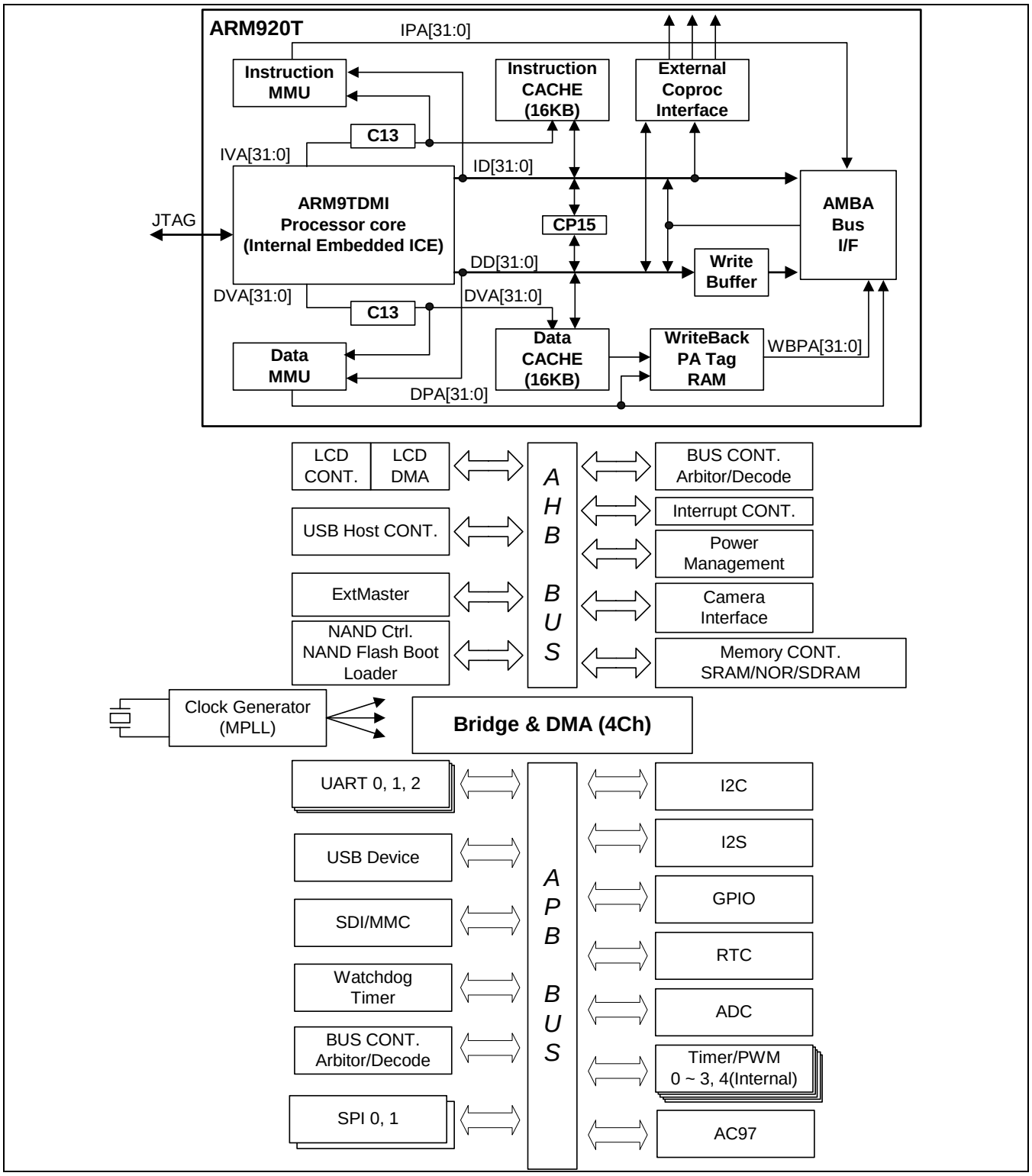


Figure 2-1. S3C2440A Block Diagram

2. MEMORY MAP

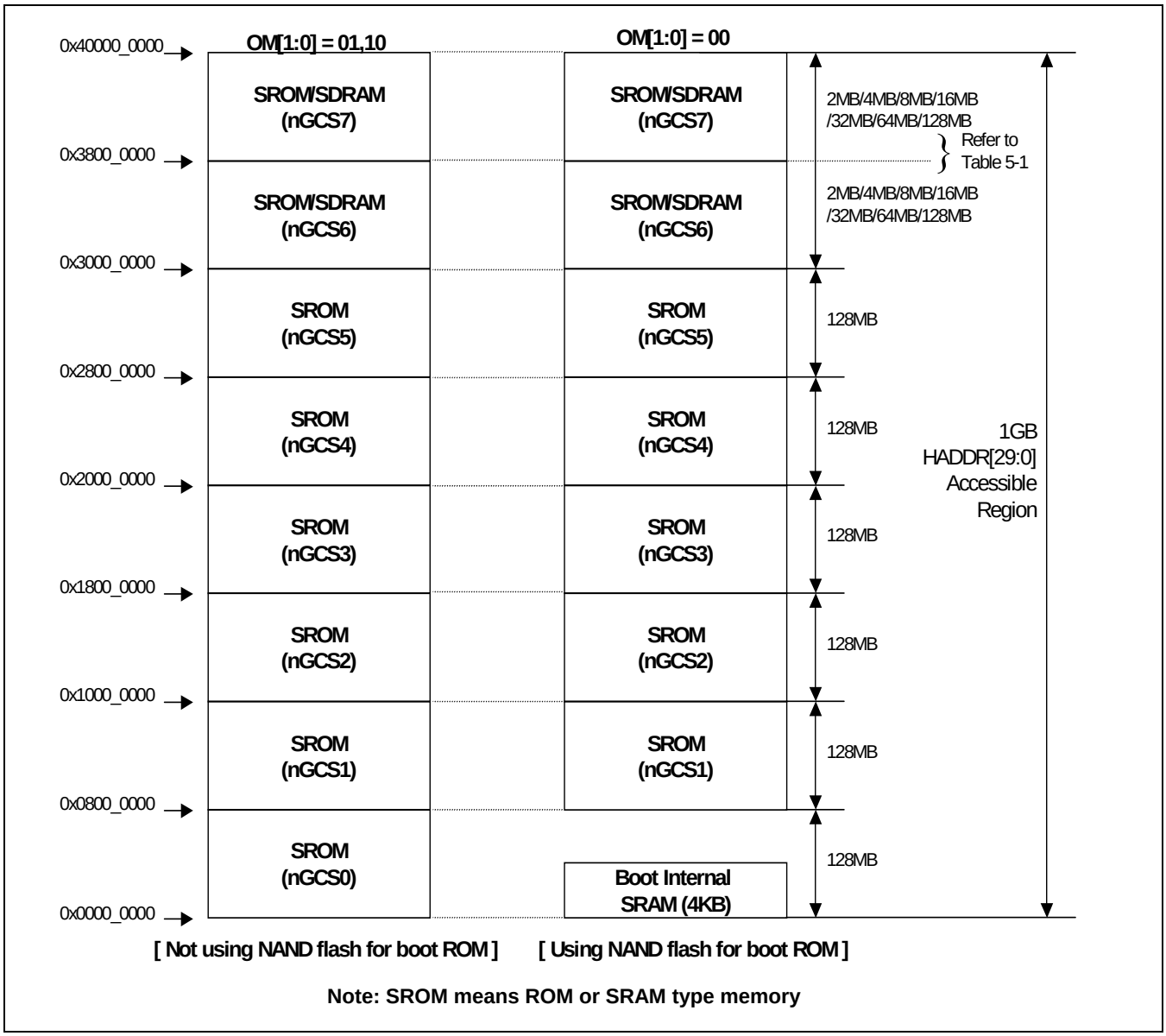


Figure 2-2. S3C2440A Memory Map after Reset

3. SDRAM BANK ADDRESS CONFIGURATION

Table 2-1. Bank 6/7 Addresses

Address	2MB	4MB	8MB	16MB	32MB	64MB	128MB
Bank 6							
Start address	0x3000_0000	0x3000_0000	0x3000_0000	0x3000_0000	0x3000_0000	0x3000_0000	0x3000_0000
End address	0x301F_FFFF	0X303F_FFFF	0X307F_FFFF	0X30FF_FFFF	0X31FF_FFFF	0X33FF_FFFF	0X37FF_FFFF
Bank 7							
Start address	0x3020_0000	0x3040_0000	0x3080_0000	0x3100_0000	0x3200_0000	0x3400_0000	0x3800_0000
End address	0X303F_FFFF	0X307F_FFFF	0X30FF_FFFF	0X31FF_FFFF	0X33FF_FFFF	0X37FF_FFFF	0X3FFF_FFFF

Note

Bank 6 and 7 must have the same memory size.

BANK0 BUS WIDTH

The data bus of BANK0 (nGCS0) should be configured with a width as one of 16-bit and 32-bit ones. Because the BANK0 works as the booting ROM bank (map to 0x0000_0000), the bus width of BANK0 should be determined before the first ROM access, which will depend on the logic level of OM[1:0] at Reset.

OM1 (Operating Mode 1)	OM0 (Operating Mode 0)	Booting ROM Data width
0	0	Nand Flash Mode
0	1	16-bit
1	0	32-bit
1	1	Test Mode

MEMORY (SROM/SDRAM) ADDRESS PIN CONNECTIONS

MEMORY ADDR. PIN	S3C2440A ADDR. @ 8-bit DATA BUS	S3C2440A ADDR. @ 16-bit DATA BUS	S3C2440A ADDR. @ 32-bit DATA BUS
A0	A0	A1	A2
A1	A1	A2	A3
. . .	. . .	. . .	. . .

SDRAM BANK ADDRESS PIN CONNECTION EXAMPLE

Table 2-2. SDRAM Bank Address Configuration Example

Bank Size	Bus Width	Base Component	Memory Configuration	Bank Address
2MByte	x8	16Mbit	(1M x 8 x 2Bank) x 1	A20
	x16		(512K x 16 x 2B) x 1	
4MB	x16		(1M x 8 x 2B) x 2	A21
	x16		(1M x 8 x 2B) x 2	
8MB	x16	16Mb	(2M x 4 x 2B) x 4	A22
	x32		(1M x 8x 2B) x 4	
	x8	64Mb	(4M x 8 x 2B) x 1	
	x8		(2M x 8 x 4B) x 1	A[22:21]
	x16		(2M x 16 x 2B) x 1	A22
	x16		(1M x 16 x 4B) x 1	A[22:21]
	x32		(512K x 32 x 4B) x 1	
16MB	x32	16Mb	(2M x 4 x 2B) x 8	A23
	x8	64Mb	(8M x 4 x 2B) x 2	
	x8		(4M x 4 x 4B) x 2	A[23:22]
	x16		(4M x 8 x 2B) x 2	A23
	x16		(2M x 8 x 4B) x 2	A[23:22]
	x32		(2M x 16 x 2B) x 2	A23
	x32		(1M x 16 x 4B) x 2	A[23:22]
	x8	128Mb	(4M x 8 x 4B) x 1	
	x16		(2M x 16 x 4B) x 1	
32MB	x16	64Mb	(8M x 4 x 2B) x 4	A24
	x16		(4M x 4 x 4B) x 4	A[24:23]
	x32		(4M x 8 x 2B) x 4	A24
	x32		(2M x 8 x 4B) x 4	A[24:23]
	x16	128Mb	(4M x 8 x 4B) x 2	
	x32		(2M x 16 x 4B) x 2	
	x8	256Mb	(8M x 8 x 4B) x 1	
	x16		(4M x 16 x 4B) x 1	
64MB	x32	128Mb	(4M x 8 x 4B) x 4	A[25:24]
	x16	256Mb	(8M x 8 x 4B) x 2	
	x32		(4M x 16 x 4B) x 2	
	x8	512Mb	(16M x 8 x 4B) x 1	
128MB	x32	256Mb	(8M x 8 x 4Bank) x 4	A[26:25]
	x8	512Mb	(32M x 4 x 4B) x 2	
	x16		(16M x 8 x 4B) x 2	
	x32		(8M x 16 x 4B) x 2	

4. MEMORY INTERFACE EXAMPLES (MEMORY BANK DESIGN)

ROM Memory Interface Examples

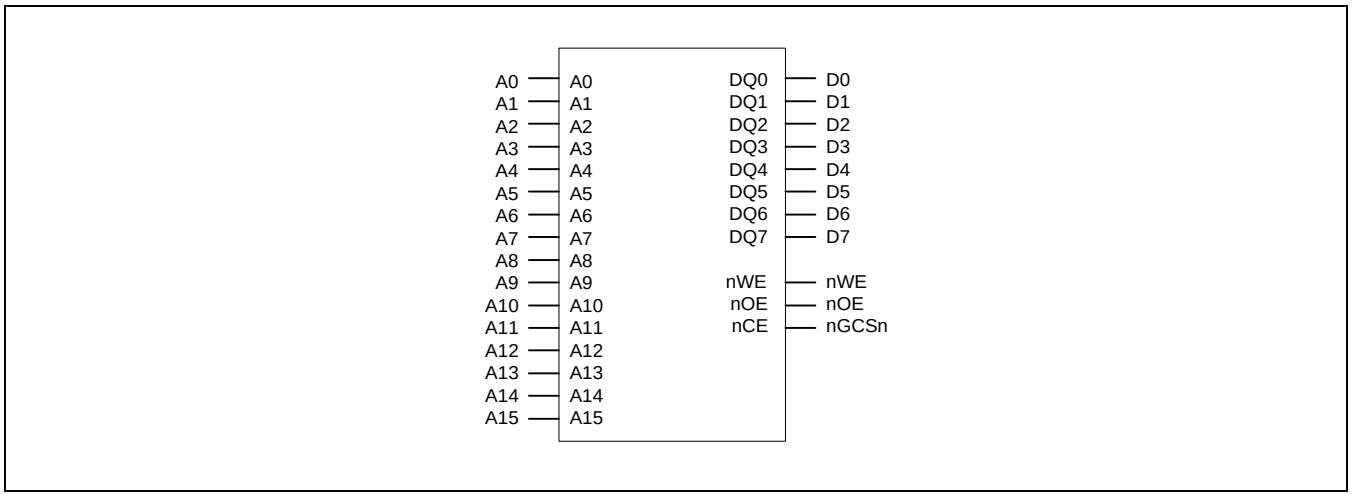


Figure 2-3. Memory Interface with 8-bit ROM

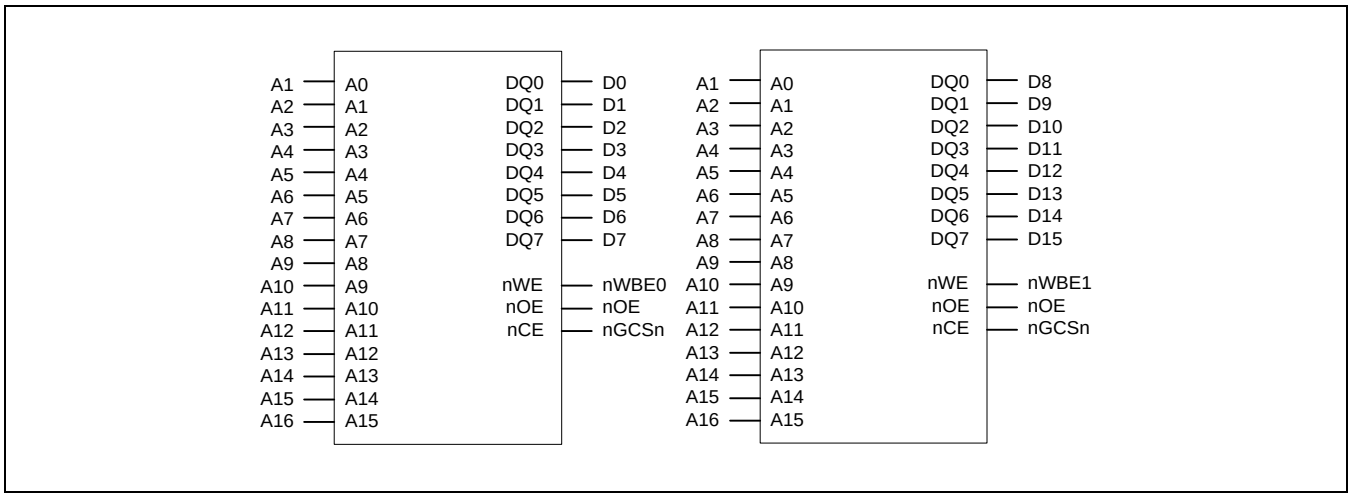


Figure 2-4. Memory Interface with 8-bit ROM x 2

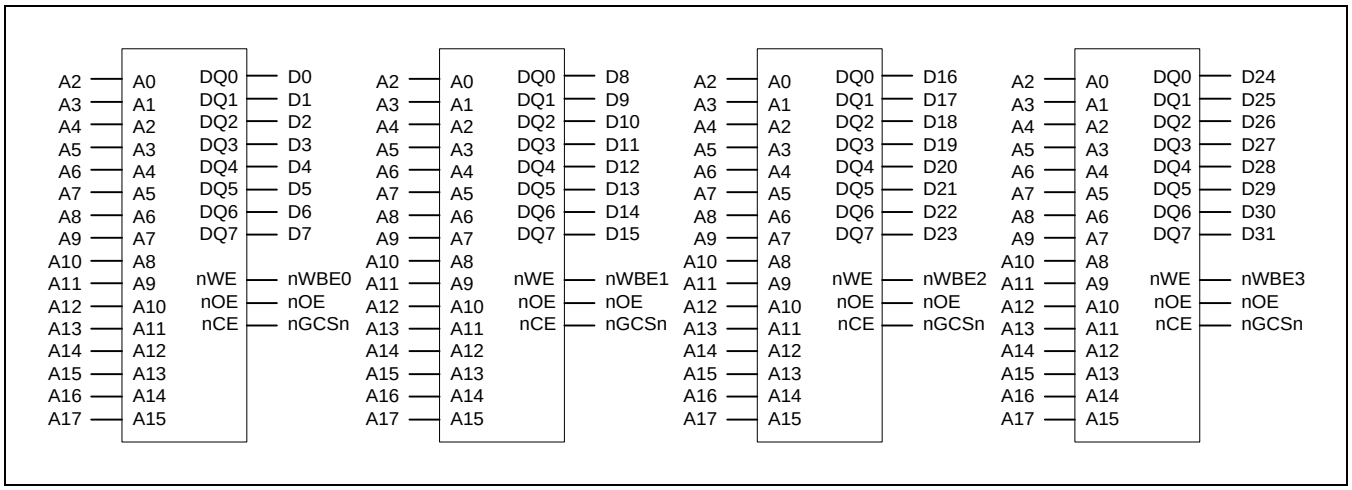


Figure 2-5. Memory Interface with 8-bit ROM x 4

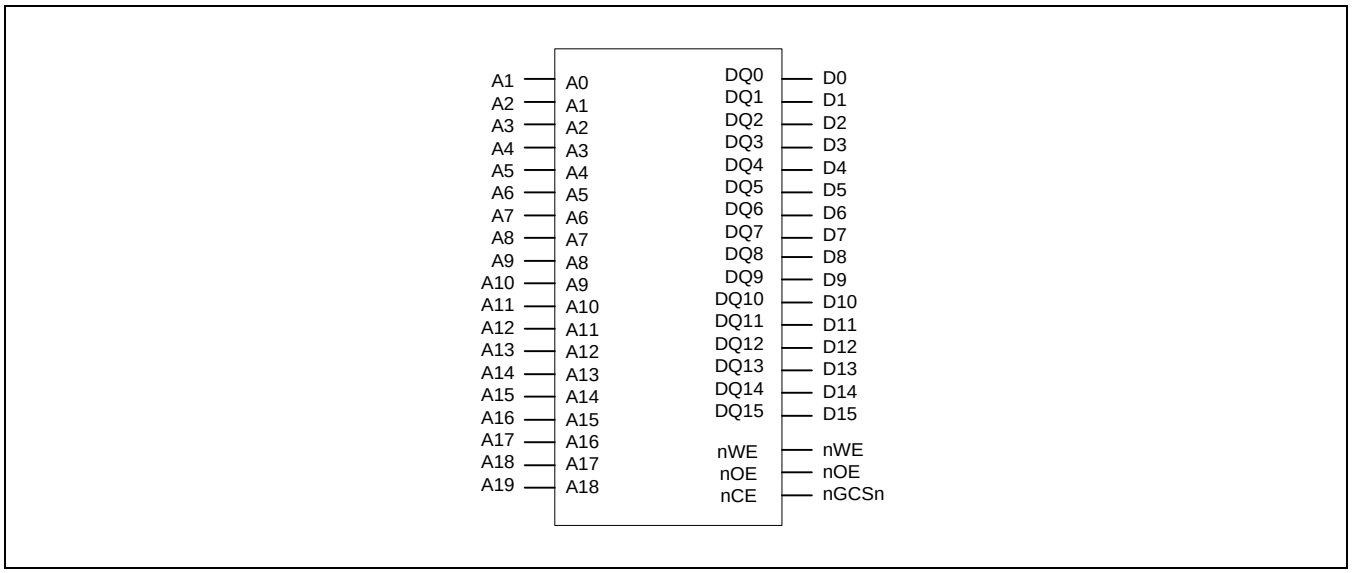


Figure 2-6. Memory Interface with 16-bit ROM

SRAM Memory Interface Examples

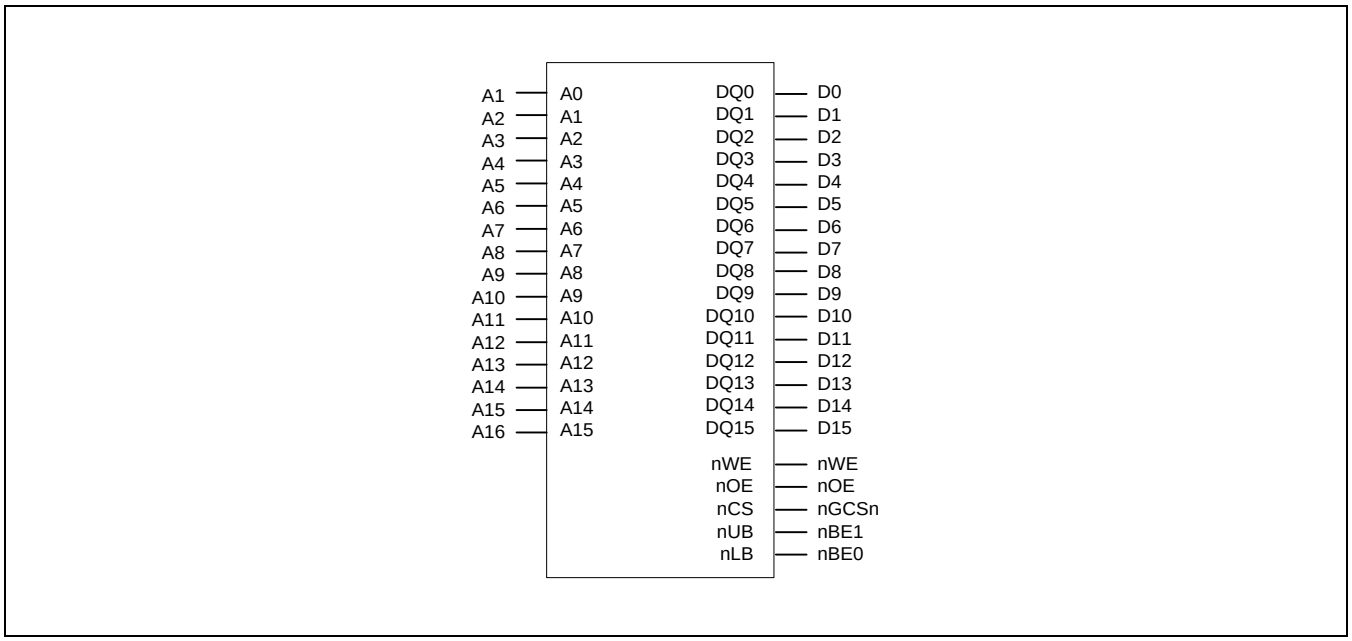


Figure 2-7. Memory Interface with 16-bit SRAM

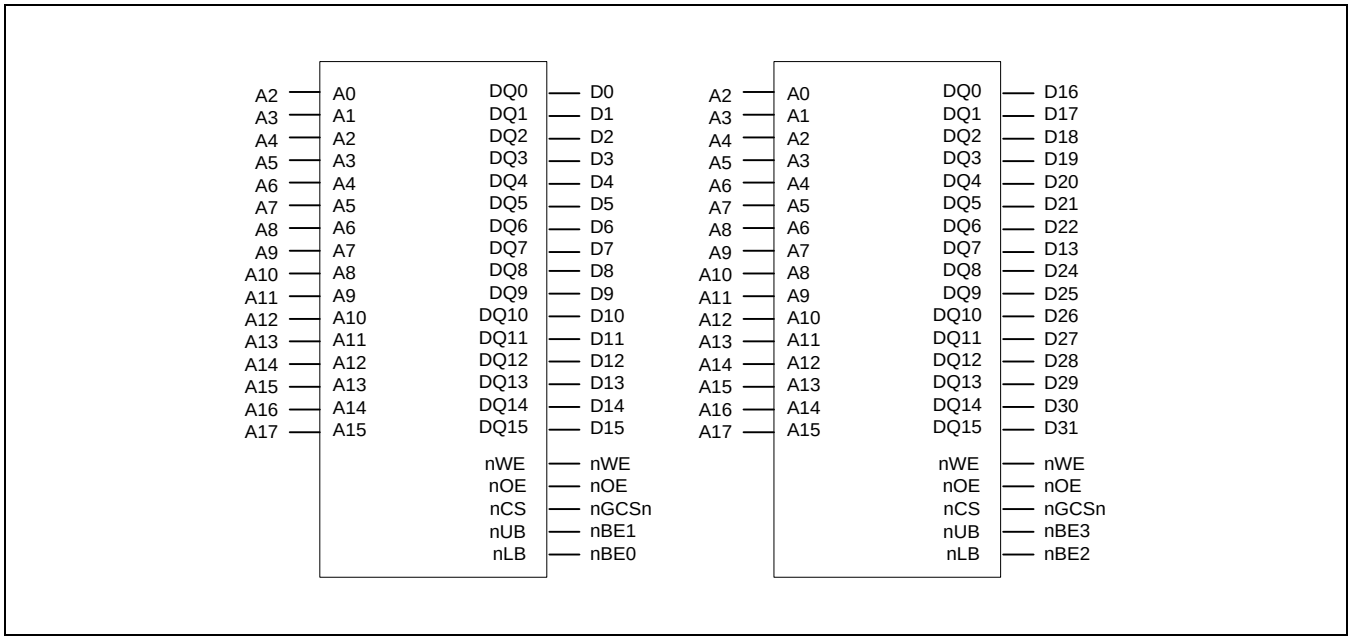


Figure 2-8. Memory Interface with 16-bit SRAM x 2

SDRAM Memory Interface Examples

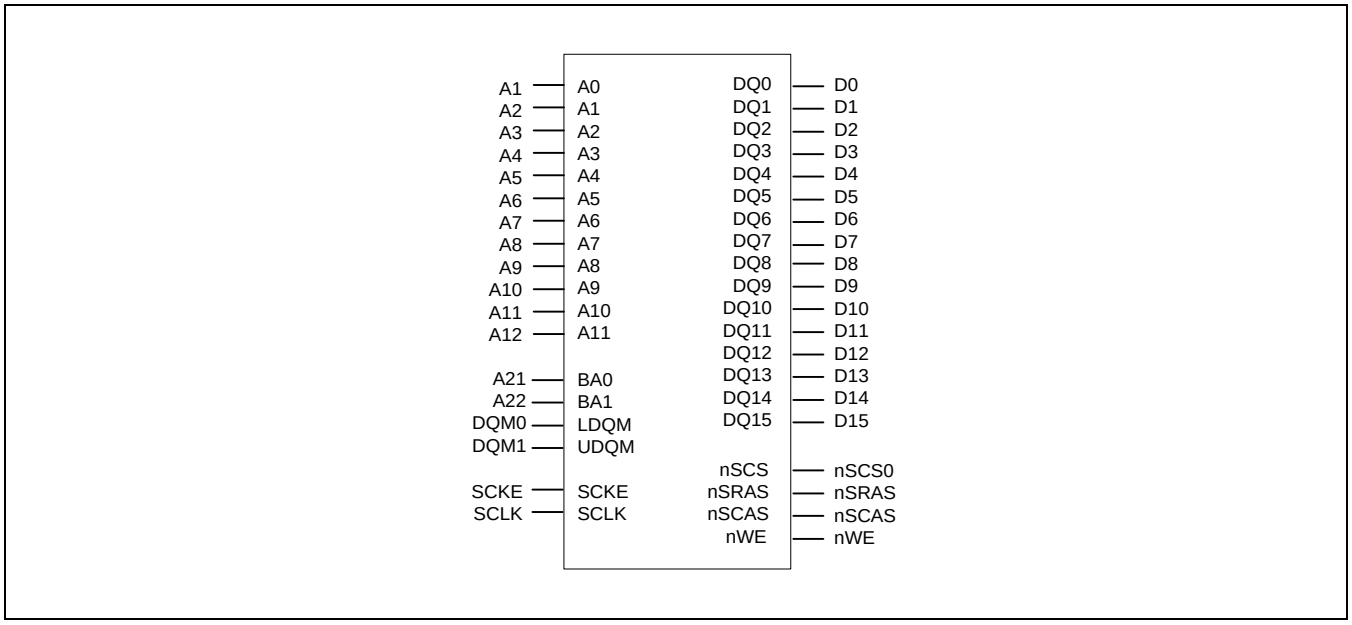


Figure 2-9. Memory Interface with 16-bit SDRAM (4Mx16, 4banks)

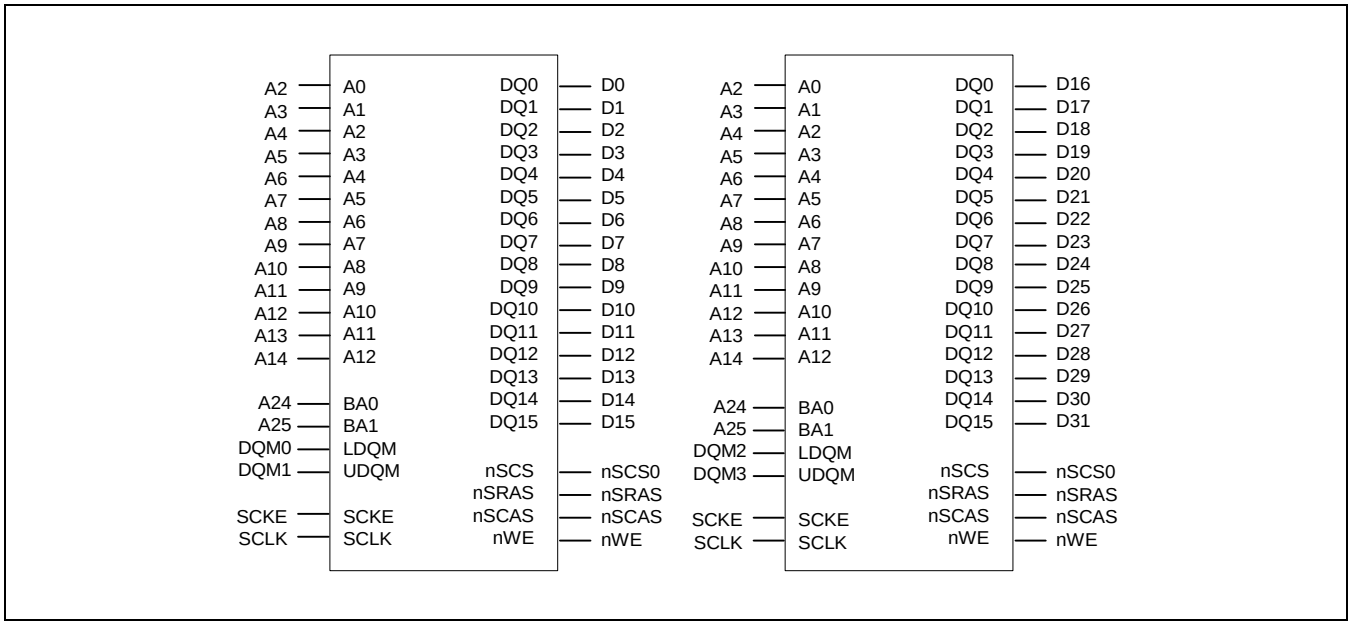


Figure 2-10. Memory Interface with 16-bit SDRAM (4Mx16x4Bank * 2ea)

Note

Refer to Table 2-2 for the Bank Address configurations of SDRAM

NOTES

3 POWERS AND CLOCK

1. OPERATING CONDITIONS

Table 3-1. Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Typ.	Min	Max	
DC supply voltage for alive block	$V_{DDalive}$	300MHz: 1.2V V_{DD} 400MHz: 1.3V V_{DD}	1.15 1.15	1.25 1.35	V
DC supply voltage for internal	V_{DDi} (1) V_{DDiarm}(1) V_{DDMPLL} V_{DDUPLL}	300MHz: 1.2V V_{DD} 400MHz: 1.3V V_{DD}	1.15 1.25	1.25 1.35	
DC supply voltage for I/O block	V_{DDOP}	3.3V V_{DD}	3.0	3.6	
DC supply voltage for memory interface	V_{DDMOP}	1.8V/2.5V/3.0V/3.3V V_{DD}	1.7	3.6	
DC supply voltage for analog core	V_{DD}	3.3V V_{DD}	3.0	3.6	
DC supply voltage for RTC	V_{DDRTC}	1.8V/2.5V/3.0V/3.3V V_{DD}	1.8	3.6	
DC input voltage	V_{IN}	3.3V Input buffer	– 0.3	V_{DDOP}+0.3	
		3.3V Interface / 5V Tolerant input buffer	– 0.3	5.25	
DC output voltage	V_{OUT}	3.3V Output buffer	– 0.3	V_{DDOP}+0.3	
Operating temperature	T_{OPR}	Industrial	–40 to 85		°C

NOTE: In the DVS(Dynamic Voltage Scaling) VDDi & VDDiarm can be supplied with 1.0V in Idle mode. Refer the Application Notes for detailed information.

2. ELECTRICAL SPECIFICATIONS

Table 3-2 and 3-3 define the DC electrical characteristics for the standard LVCMOS I/O buffers.

Table 3-2. Normal I/O PAD DC Electrical Characteristics

Normal I/O PAD DC Electrical Characteristics for Memory (V_{DDMOP} = 2.5V ± 0.2V, T_A = –40 to 85 °C)

Symbol	Parameters	Condition	Min	Typ.	Max	Unit
V_{IH}	High level input voltage					V
	LVCMOS interface		1.7			
V_{IL}	Low level input voltage					V
	LVCMOS interface				0.7	
VT	Switching threshold			$0.5V_{DD}$		V
VT+	Schmitt trigger, positive-going threshold	CMOS			2.0	V
VT–	Schmitt trigger, negative-going threshold	CMOS	0.8			V
I_{IH}	High level input current					µA
	Input buffer	$V_{IN} = V_{DD}$	–10		10	
I_{IL}	Low level input current					µA
	Input buffer	$V_{IN} = V_{SS}$	–10		10	
	Input buffer with pull-up		–60	–33	–10	
V_{OH}	High level output voltage					V
	Type B4 to B12	I_{OH} = – 1 µA	V_{DD} –0.05			
	Type B4	I_{OH} = – 4 mA	2.0			
	Type B6	I_{OH} = – 6 mA				
	Type B8	I_{OH} = – 8 mA				
	Type B10	I_{OH} = – 10 mA				
	Type B12	I_{OH} = – 12mA				
V_{OL}	Low level output voltage					V
	Type B4 to B12	I_{OL}= 1 µA			0.05	
	Type B4	I_{OL} = 4 mA			0.4	
	Type B6	I_{OL} = 6 mA				
	Type B8	I_{OL} = 8 mA				
	Type B10	I_{OL} = 10 mA				
	Type B12	I_{OL} = 12 mA				

NOTES:

1. Type B6 means 6mA output driver cell.
2. Type B8 means 8mA output driver cell.

Normal I/O PAD DC Electrical Characteristics for Memory (V_{DDMOP}=3.0V±0.3V, 3.3V±0.3V, T_A= –40 to 85 °C)

Symbol	Parameters	Condition	Min	Typ.	Max	Unit
V_{IH}	High level input voltage					V
	LVCMOS interface		2.0			
V_{IL}	Low level input voltage					V
	LVCMOS interface				0.8	
VT	Switching threshold			$0.5V_{DD}$		V
VT+	Schmitt trigger, positive-going threshold	CMOS			2.0	V
VT–	Schmitt trigger, negative-going threshold	CMOS	0.8			V
I_{IH}	High level input current					µA
	Input buffer	$V_{IN} = V_{DD}$	–10		10	
I_{IL}	Low level input current					µA
	Input buffer	$V_{IN} = V_{SS}$	–10		10	
	Input buffer with pull-up		–60	–33	–10	
V_{OH}	High level output voltage					V
	Type B4 to B12	I_{OH} = – 1 µA	V_{DD} – 0.05			
	Type B4	I_{OH} = – 4 mA	2.4			
	Type B6	I_{OH} = – 6 mA				
	Type B8	I_{OH} = – 8 mA				
	Type B10	I_{OH} = –10 mA				
	Type B12	I_{OH} = –12 mA				
V_{OL}	Low level output voltage					V
	Type B4 to B12	I_{OL} = 1 µA			0.05	
	Type B4	I_{OL} = 4 mA			0.4	
	Type B6	I_{OL} = 6 mA				
	Type B8	I_{OL} = 8 mA				
	Type B10	I_{OL} = 10 mA				
	Type B12	I_{OL} = 12 mA				

NOTES:

1. Type B6 means 6mA output driver cell.
2. Type B8 means 8mA output driver cell.
3. Type B12 means 12mA output driver cells.

Table 3-3. USB DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	High level input voltage	–	2.5	–	V
V_{IL}	Low level input voltage	–	–	0.8	V
I_{IH}	High level input current	Vin = 3.3V	–10	10	µA
I_{IL}	Low level input current	Vin = 0.0V	–10	10	µA
V_{OH}	Static output high	15K to GND	2.8	3.6	V
V_{OL}	Static output low	1.5K to 3.6V		0.3	V

3. POWER CONSUMPTION SPECIFICATIONS

Table 3-4. S3C2440 Power Supply Voltage and Current

Parameter	Value	Unit	Condition
Typical V_{DDi} / V_{DDOP}	1.3 / 3.3	V	Without DVS
Max. Operating frequency (FCLK)	400	MHz	–
Max. Operating frequency (HCLK)	133	MHz	–
Max. Operating frequency (PCLK)	67	MHz	–
Typical normal mode power (3) (Total V_{DDi} + V_{IO})	368	mW	(1)
Typical normal mode power (3) (Total V_{DDi} + VIO)	310	mW	(2)
Typical idle mode power (3) (Total V_{DDi} + V_{IO})	213	mW	FCLK = 400MHz (F:H:P = 1:3:6)
Typical slow mode power (3) (Total V_{DDi} + V_{IO})	97	mW	FCLK = 12MHz (F:H:P = 1:1:1)
Typical Sleep mode power (3)	380	µA	@1.2/3.3V, Room temperature All other I/O static.
Typical RTC power (3)	3	µA	@3.0V, Room temperature X-tal = 32.768kHz for RTC

NOTES:

1. I/D cache: ON, MMU: ON, Code on SRAM, FCLK: HCLK: PCLK = 400MHz: 133MHz: 66.7MHz
   : LCD ON (320x240x16bppx60Hz, color TFT): 13 kHz Timer internal mode (5 Channel run)
   : Audio (IIS&DMA, CDCLK=16.9MHz, LRCK=44.1kHz):Integer data quick sort (65536 EA)
2. Pocket PC 2003 MPEG play
3. The above power consumption data is measured in Room temperature with random sample (Lot #: KZZ1FS).

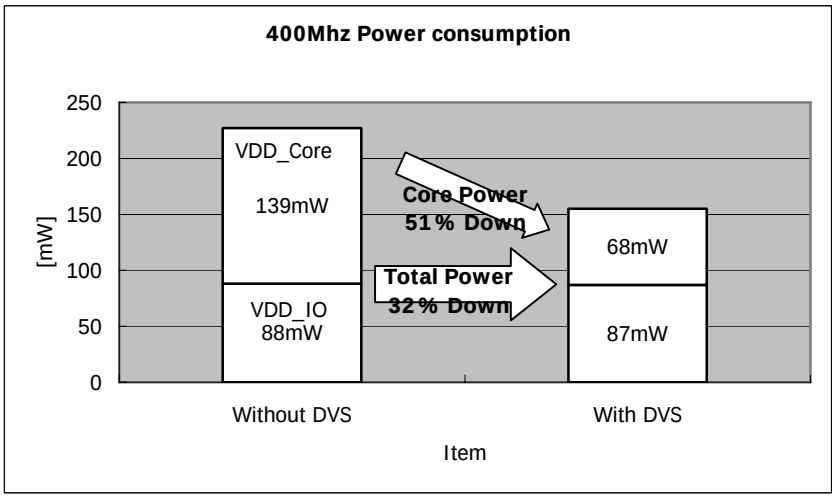


Figure 3-1. Power Consumption Example Comparison when Applied DVS Scheme

NOTE: (Condition) Current measure condition: Play Battlife.wma(bit rate=64kbps) on PPC2003 SMDK2440.
Core power:
Without DVS : VDDiarm/VDDi/VDDupll/VDDmpll/VDDalive = 1.3V
using DVS : VDDiarm/VDDi = 1.3V ⇔ 1.0V, VDDupll/VDDmpll/VDDalive = 1.3V
I/O Power : VDDOP/VDDMOP/VDDRTC/VDDADC=3.3V
Refer the Application notes for more information about DVS.

Table 3-5. Typical Current Decrease by CLKCON Register

FCLK: HCLK: PCLK = 300:100:50MHz, 1.2V (Random sample)

(Unit: mA)

Peripherals	NFC	LCD	USBH	USBD	Timer	SDI	UART	RTC	ADC	IIC	IIS	SPI	Camera	Total
Current	1.7	2.8	0.37	0.79	0.32	1.0	2.7	0.45	0.26	0.32	0.78	0.16	14.25	26.26

NOTE: This table includes power consumption of each peripheral. For example, If you do not use Camera and have turned off the Camera block by CLKCON register, then you can save the 14.25mA of internal block.

4. OSCILLATOR

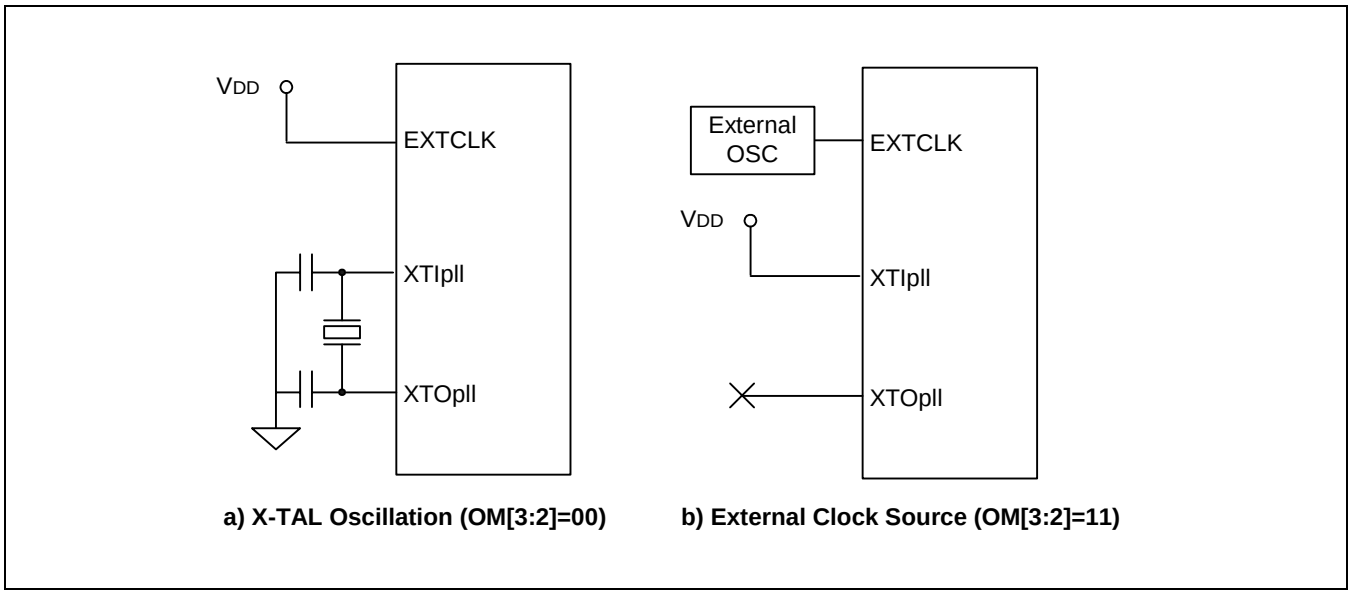
Usual Conditions for PLL & Clock Generator

PLL & Clock Generator generally uses the following conditions.

Loop filter capacitance	C_{LF}	MPLLCAP: 1.3 nF ± 5%
		UPLLCAP: 700 pF ± 5%
External X-tal frequency	–	12 – 20 MHz (note)
External capacitance used for X-tal	C_{EXT}	15 – 22 pF

NOTES:

1. The value could be changed.
2. $FCLK_{OUT}$ must be bigger than 200MHz (It does not mean that the ARM core has to run more than 200MHz).



a) X-TAL Oscillation (OM[3:2]=00) **b) External Clock Source (OM[3:2]=11)**

Figure 3-2. Main Oscillator Circuit Examples

5. RESET AND POWER AC TIMING

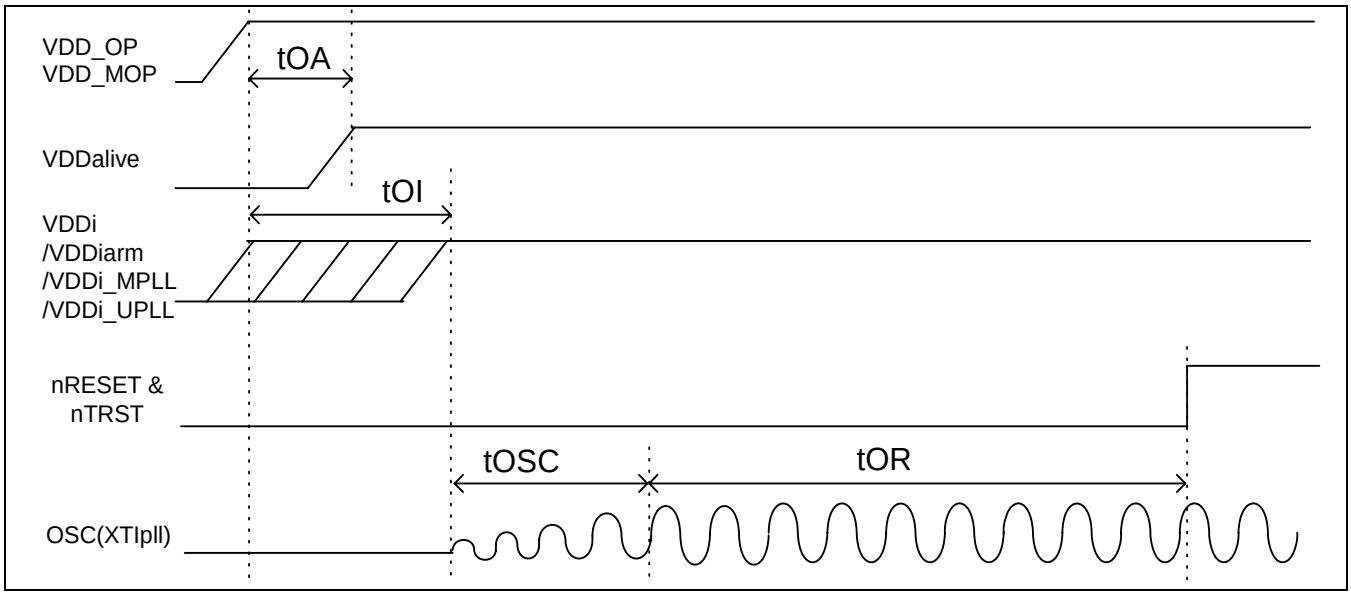


Figure 3-3. Power-On Reset Sequence (when the external clock source is a crystal oscillator. The OSC's frequency should be meet the specification which is 12 ~ 20Mhz)

Table 3-5. Power on Reset Timing Specifications

Symbol	Description	Min	Typical	Max	Units
tOA	VDDOpx(VDD_MOP) to VDDalive	0			ms
tOI	VDDOpx(VDD_MOP) to VDDi/VDDiarm/VDDi_MPLL/VDDi_UPLL	0			us
tOSC	VDDi/VDDiarm/VDDi_MPLL/VDDi_UPLL to Oscillator stabilization	2			ms
tOR	Oscillator stabilization to nRESET & nTRST high	1			us

NOTES

4 INTERFACES

1. DVS (Dynamic Voltage Scaling)

OVERVIEW

DVS (Dynamic Voltage Scaling) is useful to reduce power consumption in Idle mode.

The basic concept of DVS is to drop the Core and Internal voltage when those blocks don't need to operate heavily and reduce the power consumption.

There are two methods to reduce power consumption; one is drop the voltage while the internal blocks are not working or operating slowly though the system is running. The other is lengthening the system clock speed to reduce power consumption.

DVS uses the two methods, voltage scaling and change clocking.

When DVS is used, the Core power consumption can be reduced maximum by 50% of the core current.

While WMA is playing, Idle state rate is more than 80% and actual CPU operating rate is about 20%. If DVS is applied to this application, power can be saved during 80% Idle period.

POWER SCHEME FOR DVS

Applicable DVS power supply pins are VDDi (Internal block power) and VDDiarm (ARM920T power). To use DVS, the system power has to be supplied two variable voltages. One for normal operation, the other for lower level voltage (for DVS).

The DVS High and Low voltage is as follows.

Table 4-1. DVS voltage level

DVS Pins	Voltage spec.	Normal operating voltage	DVS low voltage
VDDiarm	300MHz: 1.2V(1.15V ~ 1.25V) 400MHz: 1.3V(1.25V ~ 1.35V)	300MHz: 1.2V 400MHz: 1.3V	Min 1.0V
VDDi	300MHz: 1.2V(1.15V ~ 1.25V) 400MHz: 1.3V(1.25V ~ 1.35V)	300MHz: 1.2V 400MHz: 1.3V	Min 1.0V

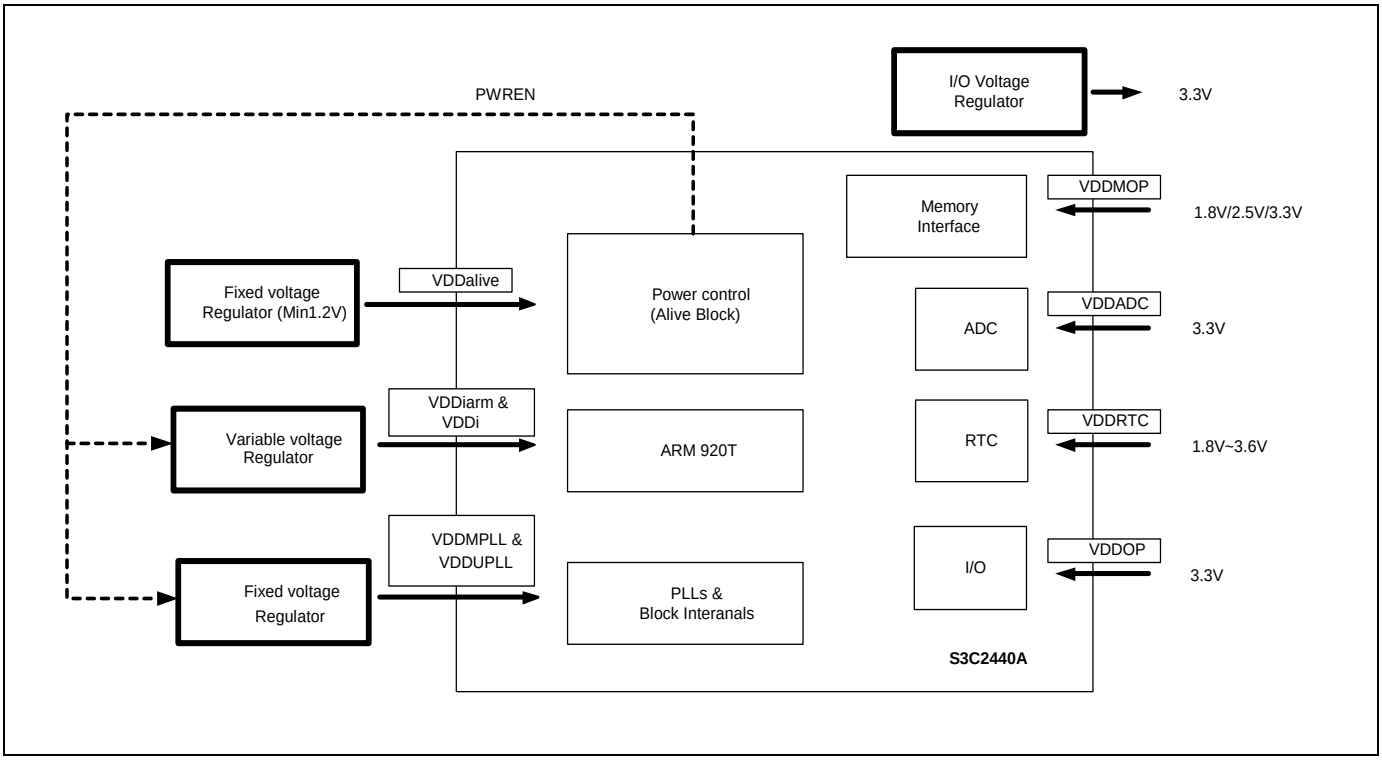


Figure 4-1. Power Scheme for DVS

The DVS scheme can be applied only for VDDiarm, but we strongly recommend using both VDDiarm and VDDi voltage. Refer the following Schematic diagram for DVS.

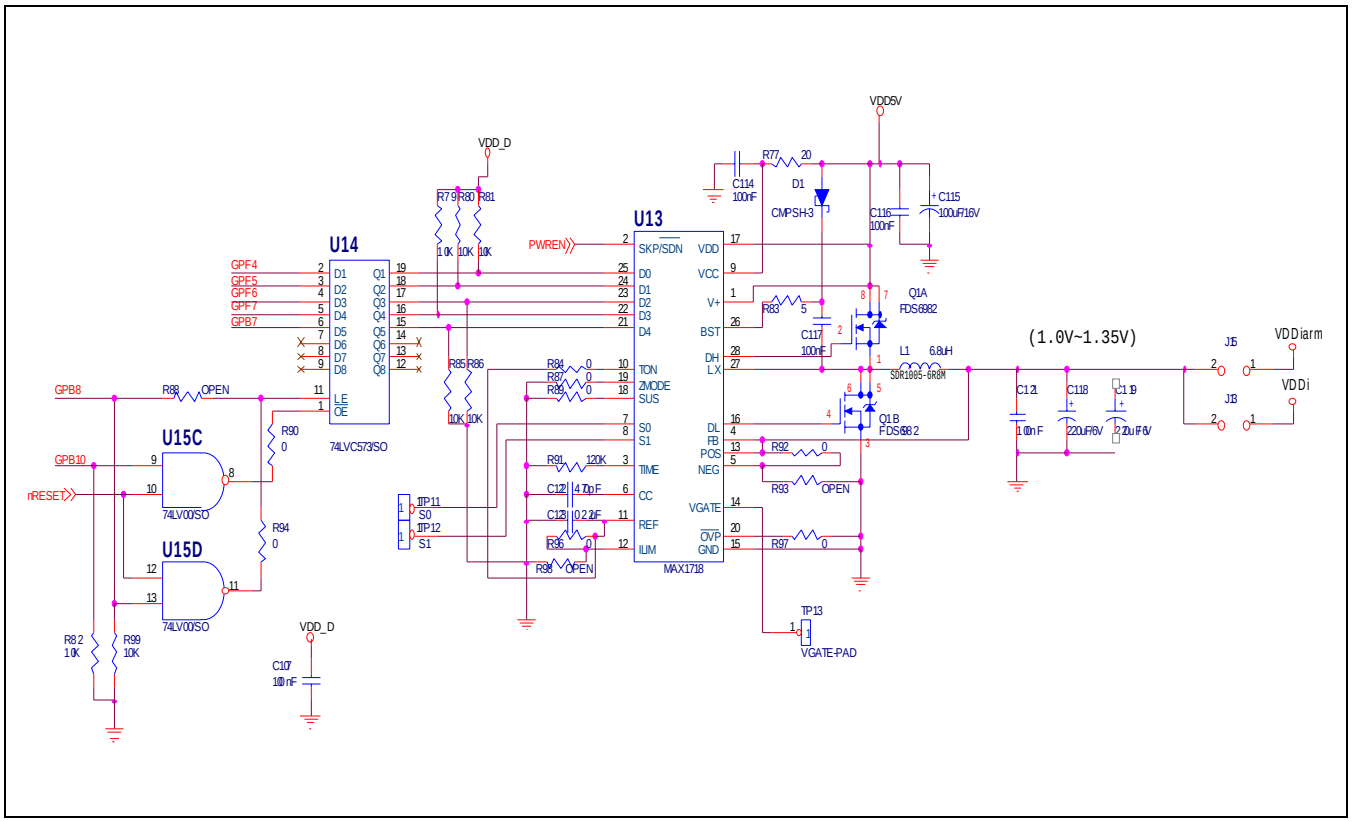


Figure 4-2. Power Regulator Example Diagram for DVS

DVS OPERATING DETAILS

DVS operating flow chart

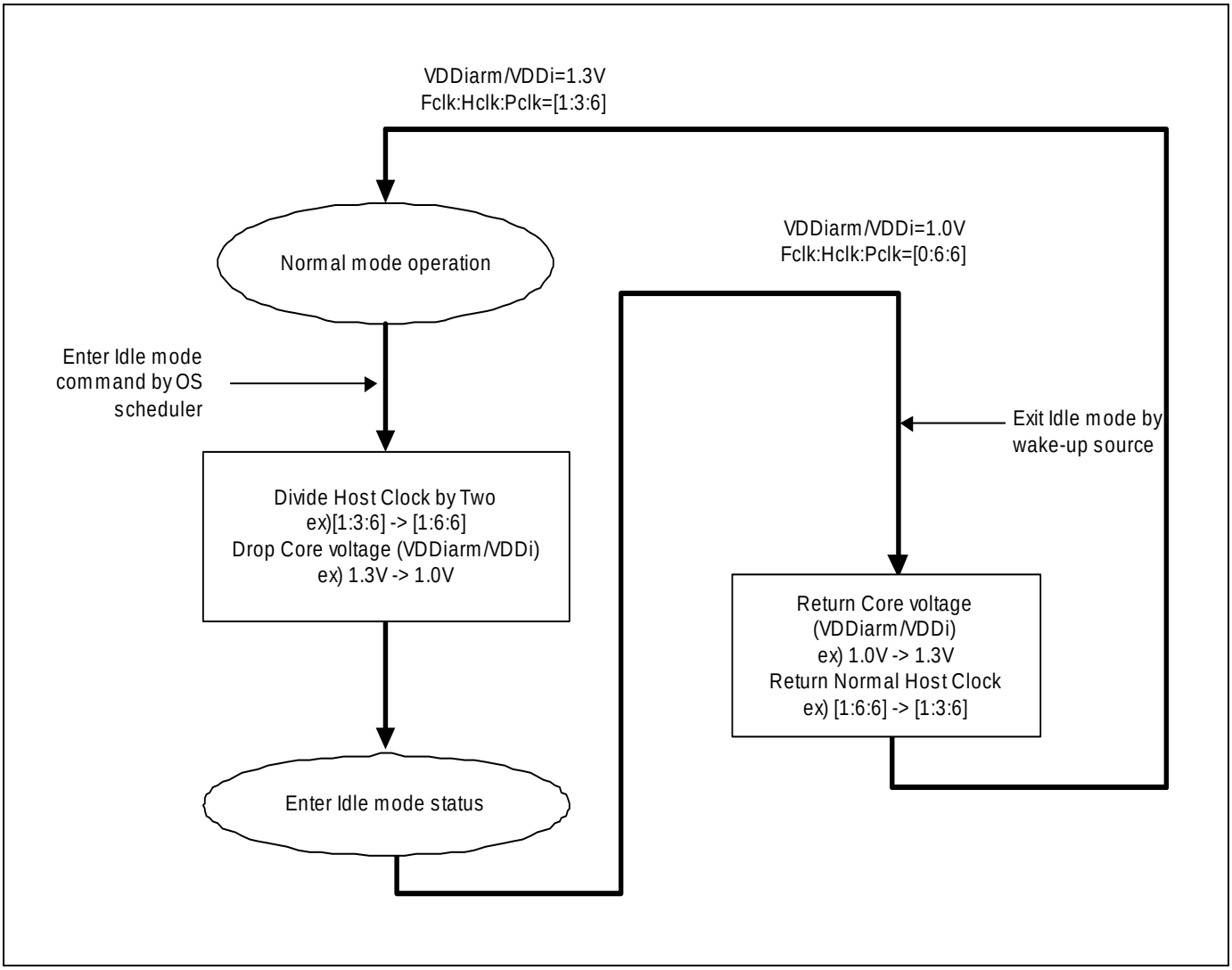


Figure 4-3. DVS Flow Chart Example (400MHz)

DVS SHCEME DESCRIPTION

Please contact the Samsung CS team for Detailed DVS scheme.

POWER CONSUMPTION OF DVS

Table 4-2 shows how much the power consumption will be reduced when using DVS.

Table 4-2. Core current Consumption

FCLK [MHz]	DVS Scheme application (VDDiarm/VDDi)	Core Power [mW]		Difference Without→With
		With DVS	Without DVS	
300	Running mode (1)	**51**	**74**	+23mW(45%)
	Idle mode (2)	**32**	**64**	+32mW{100%}
400	Running mode (1)	**68**	**139**	+71mW(104%)
	Idle mode (2)	**46**	**113**	+67mW(146%)

NOTE: Test condition

— Core current = I_VDDi + I_VDDiarm at 1.2V @300MHz, 1.3V @400MHz.
(Current of VDDalive/VDDUPLL/VDDMPLL are not included).

— For DVS the Core voltage will be down to 1.0V

Execute Batlife.wma file on PPC2003.

No threads ready to run on PPC2003

FCLK: HCLK: PCLK = (300:50:50) and (0:50:50) MHz for 300MHz,
(400:67:67) and (0:67:67) MHz for 400MHz.

FCLK: HCLK: PCLK = (300:100:50), (400:133:67) MHz

Sample #: KYC13AA

OS timer scheduler: 1msec~10msec.

As the upper table, Using DVS, the core power consumption will be reduced quite much

The followings are the 2440 total power consumption comparison between DVS is on and off with following condition.

— Core current = I_VDDi + I_VDDiarm + VDDalive + VDDUPLL + VDDMPLL at 1.2V @300MHz, 1.3V @400MHz.

2. MEMORY

MEMORY INTERFACE DESIGN

BOOT ROM DESIGN

After the system reset, the S3C2440A accesses 0x00000000 address and configuring some system variables. Therefore, this special code (boot ROM image) should be located on the address 0x0000_0000. Bus width of boot ROM can be selected by setting OM [1:0] pins.

Table 4-3. Data Bus Width for ROM Bank 0

OM [1:0]	Data Bus Width
00	NAND boot
01	16-bit (half-word)
10	32-bit (word)
11	Test mode

NAND BOOT DESIGN

Figure 4-4 shows a design with NAND boot.

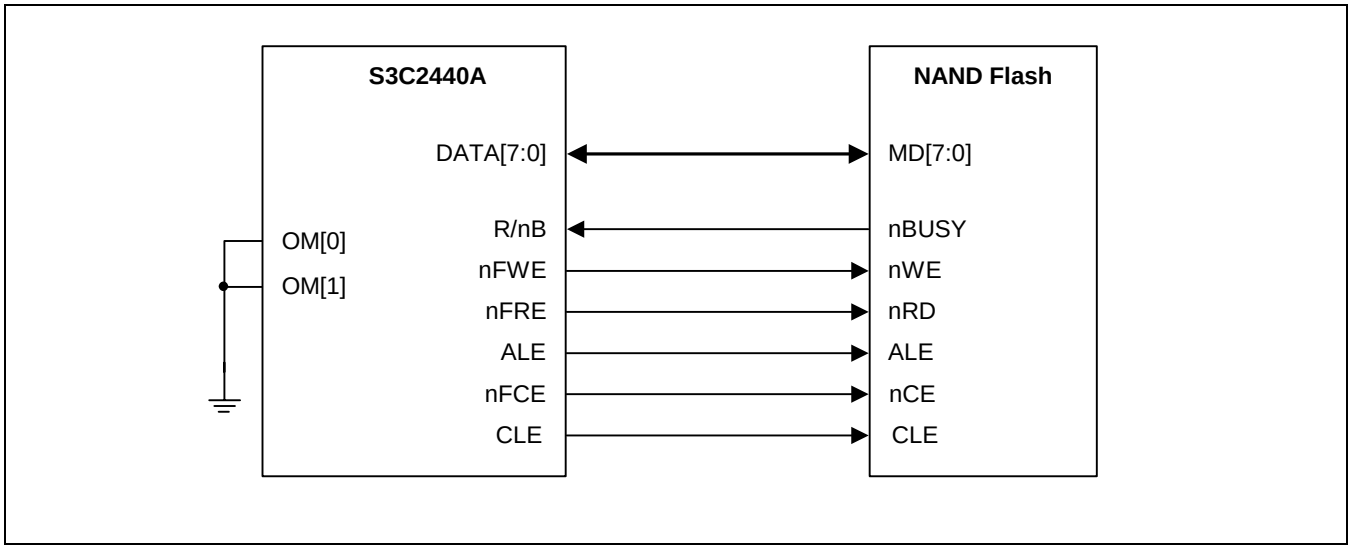


Figure 4-4. NAND Boot Design

MAKING NAND BOOT IMAGE

When making a NAND boot loader image, you can use the binary file that is made from compiling and linking.

HALFWORD BOOT ROM DESIGN WITH BYTE EEPROM/FLASH

Figure 4-5 shows a design with half-word boot ROM with byte EEPROM/Flash.

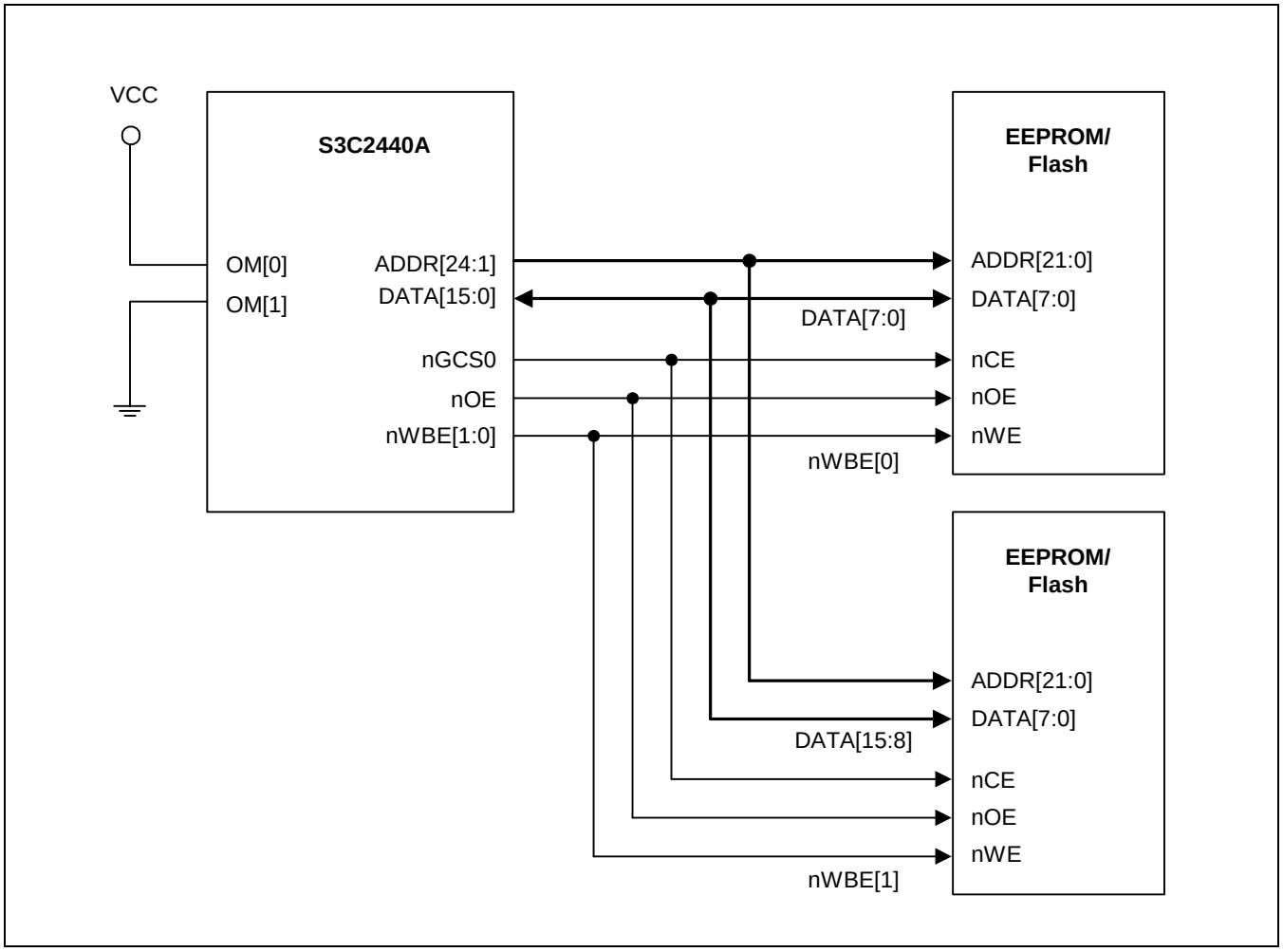


Figure 4-5. Half-word Boot ROM Design with Byte EEPROM/Flash

MAKING HALFWORD ROM IMAGE WITH BYTE EEPROM/FLASH

When make half-word ROM image, you can split two image files, EVEN and ODD.

Table 4-4. Relationship ROM Image and Endian

	Big Endian	Little Endian
DATA [7:0]	Odd	Even
DATA [15:8]	Even	Odd

HALFWORD BOOT ROM DESIGN WITH HALFWORD EEPROM/FLASH

Figure 4-6 shows a design with half-word boot ROM with byte EEPROM/Flash.

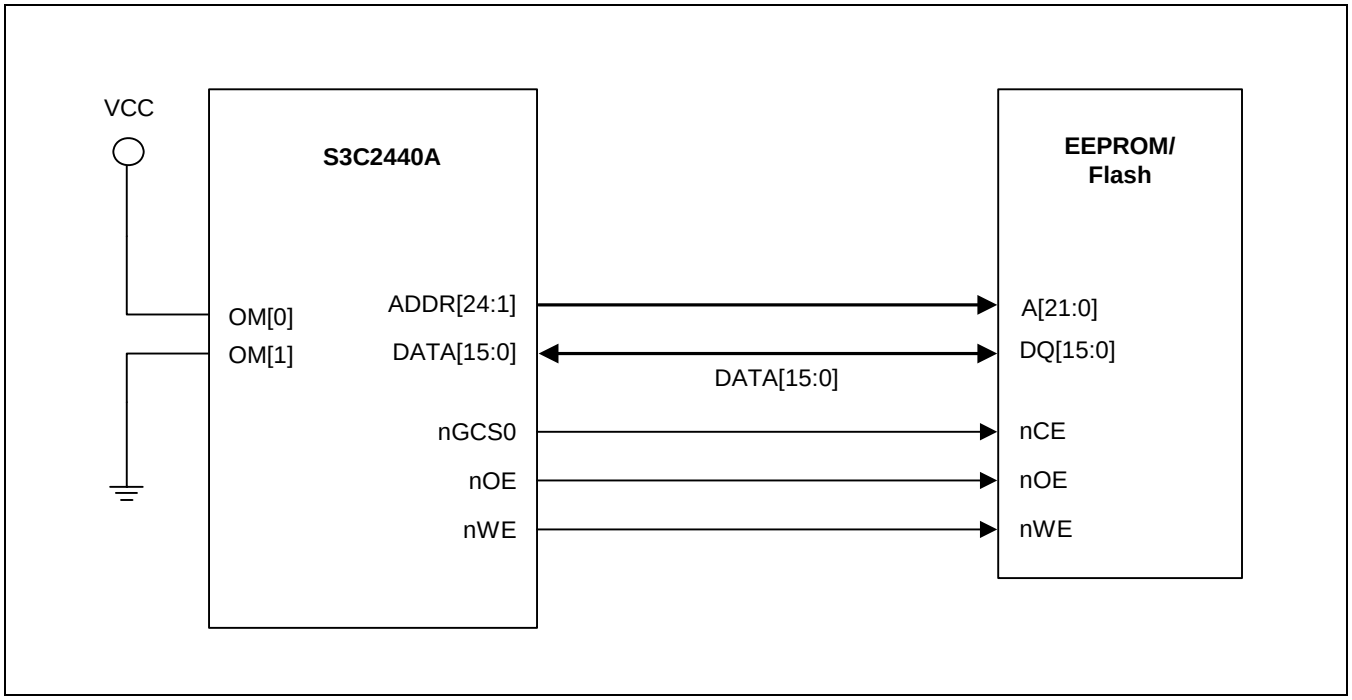


Figure 4-6. The Halfword Boot ROM Design with Halfword EEPROM/Flash

WORD BOOT ROM DESIGN WITH byte EEPROM/FLASH

Figure 4-7 shows a design with word boot ROM with byte EEPROM/Flash.

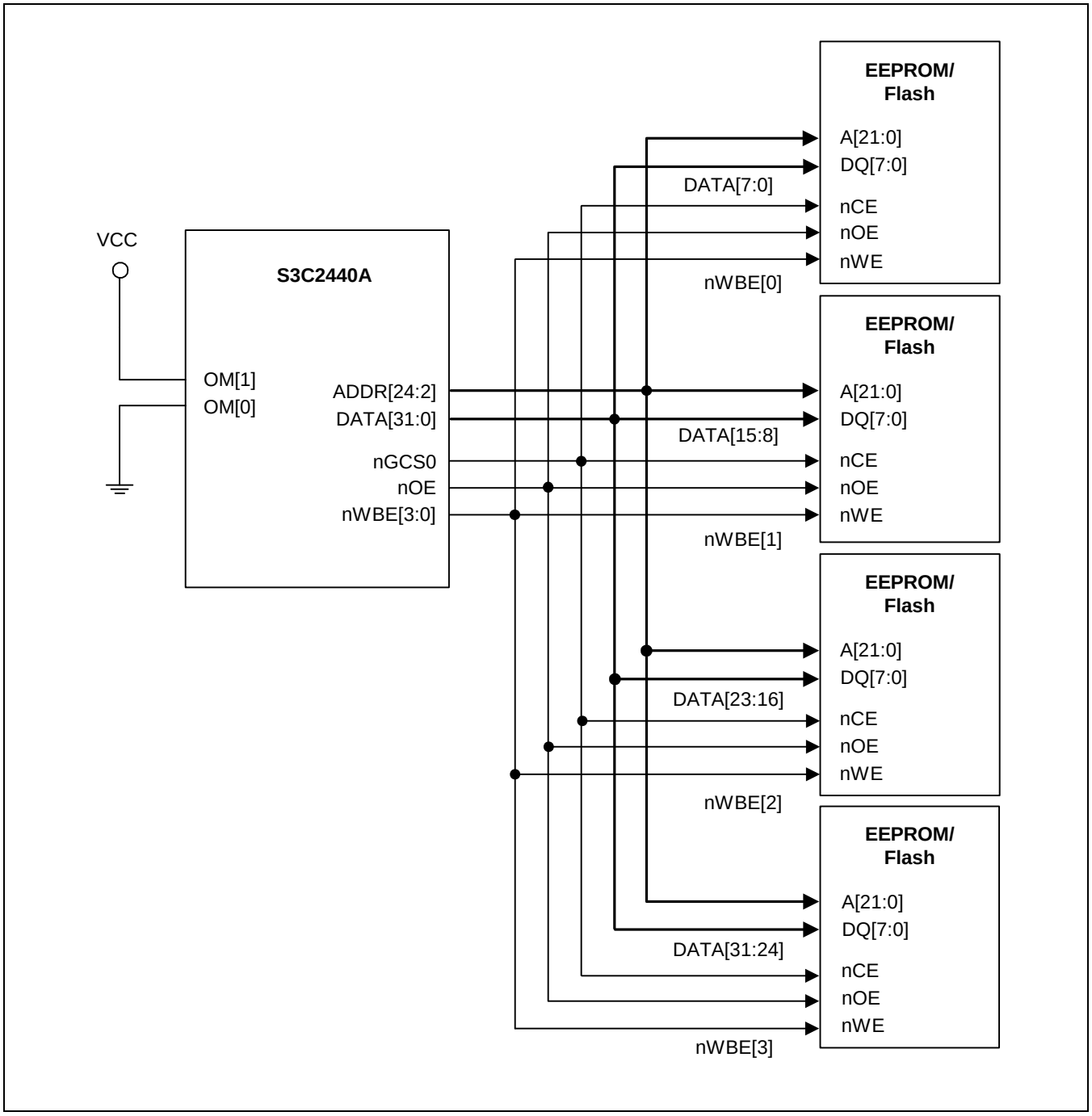
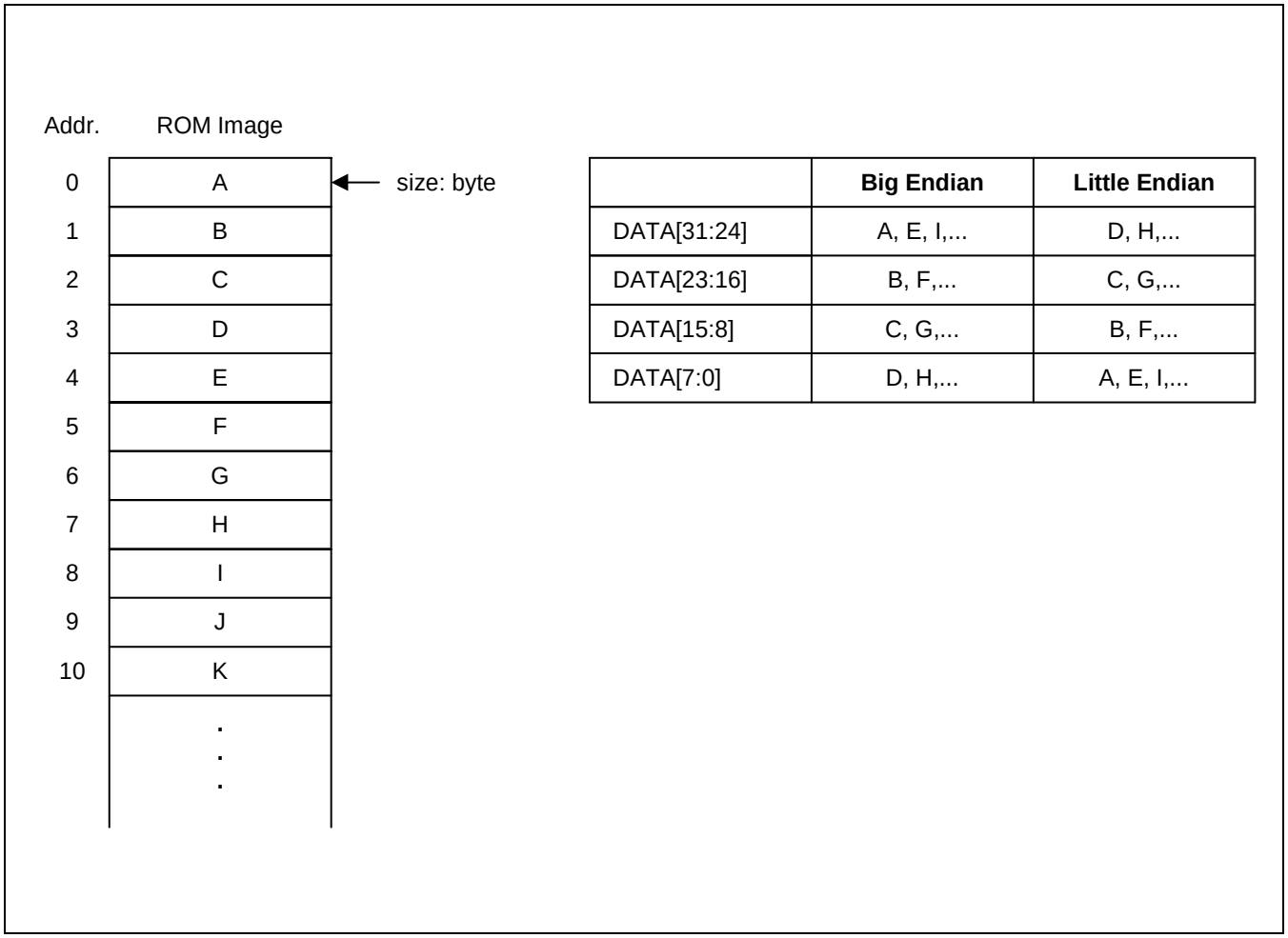


Figure 4-7. The Word Boot ROM Design with Byte EEPROM/Flash

MAKING WORD ROM IMAGE WITH BYTE EEPROM/FLASH

When you make a word ROM image, you can split it into four image files.



	Big Endian	Little Endian
DATA[31:24]	A, E, I,...	D, H,...
DATA[23:16]	B, F,...	C, G,...
DATA[15:8]	C, G,...	B, F,...
DATA[7:0]	D, H,...	A, E, I,...

Figure 4-8. Relationship of ROM Image and Endian

MEMORY BANK DESIGN AND CONTROL

The S3C2440A has six ROM/SRAM banks (including BANK0 for boot ROM) and two ROM/SRAM/SDRAM banks. The system manager on the S3C2440A can control access time, data bus width for each bank by S/W. The access time of ROM/SRAM banks and SDRAM banks is controlled by BANKCON0~5 and BANKCON6~7 control register on the system manager. The data bus width for each ROM/SRAM banks is controlled by BWSCON control register.

The ROM bank0 is used for boot ROM bank, therefore data bus width of bank0 is controlled by H/W. OM [1:0] is used for this purpose.

The control of BWSCON, BANKCON0-7, REFRESH, BANKSIZE, and MRSRB6/7 is performed during the system reset. A sample code for special register configuration is described below.

Sample code for special register configuration

```
        ; Set memory control registers
        LDR     r0, =SMRDATA
        LDR     r1, =BWSCON     ;BWSCON Address
        ADD     r2, r0, #52     ;End address of SMRDATA
0
        LDR     r3, [r0], #4
        STR     r3, [r1], #4
        CMP     r2, r0
        BNE     %B0
         .
         .
         .
         .
         .
         .
SMRDATA
         DCD 0x22111120         ;BWSCON
         DCD 0x00000700         ;GCS0
         DCD 0x00000700         ;GCS1
         DCD 0x00000700         ;GCS2
         DCD 0x00000700         ;GCS3
         DCD 0x00000700         ;GCS4
         DCD 0x00000700         ;GCS5
         DCD 0x00018005         ;GCS6 SDRAM(Trcd=3,SCAN=9)
         DCD 0x00018005         ;GCS7 SDRAM(Trcd=3,SCAN=9)
         DCD 0x008e0000+1113            ;Refresh(REFEN=1,TREFMD=0,Trp=2 clk,
                                ;       Trc=7 clk, Tchr=3 clk, Ref CNT)
         DCD 0x32               ;Bank size, 128MB/128MB
         DCD 0x30               ;MRSR 6(CL=3 clk)
         DCD 0x30               ;MRSR 7(CL=3 clk)
```

ROM/SRAM BANK DESIGN

The ROM/SRAM banks 1-7 can have a variety of width of data bus, and the bus width is controlled by S/W. A sample design for ROM/SRAM bank 1-7 is shown in Figure 4-9, Figure 4-10, Figure 4-11 and Figure 4-12.

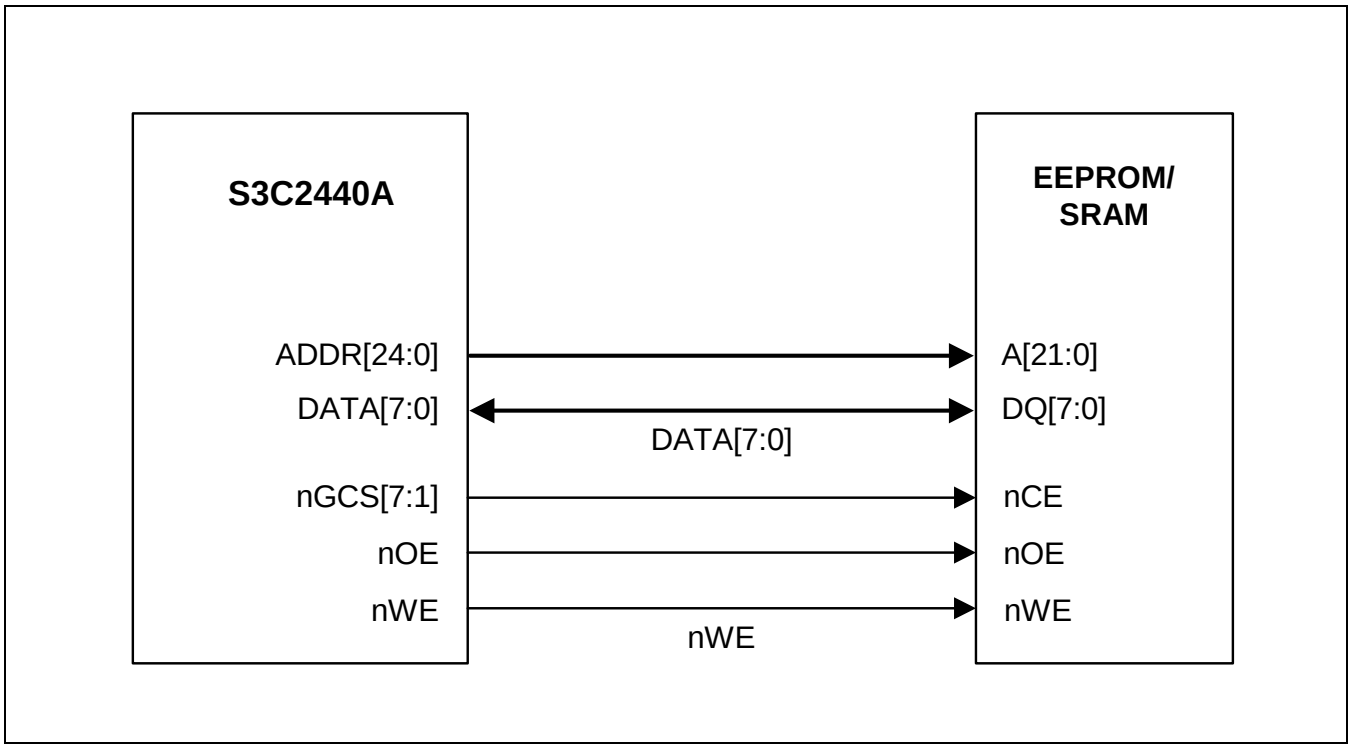


Figure 4-9. One-byte EEPROM/SRAM Bank Design

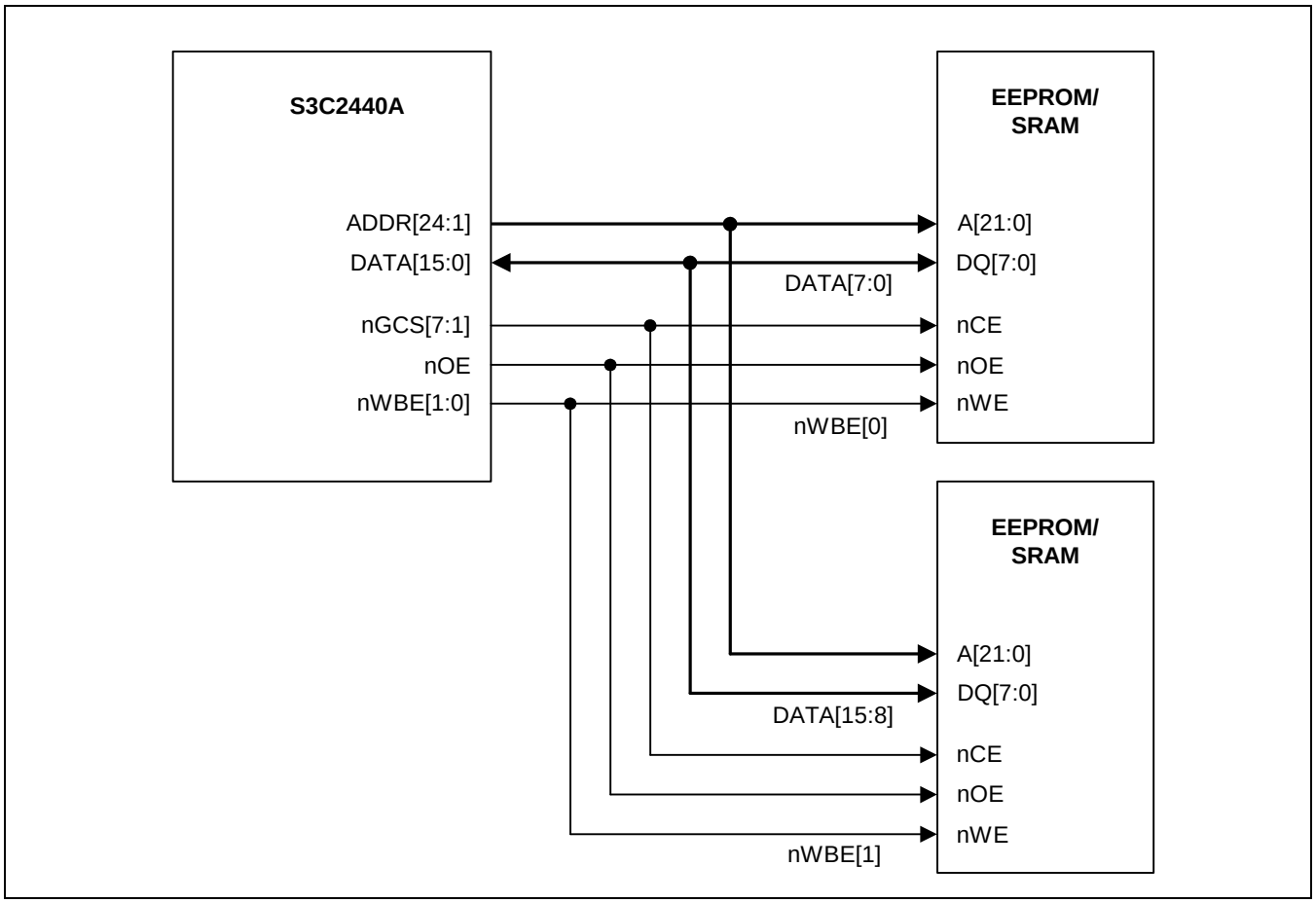


Figure 4-10. Halfword EEPROM/SRAM Bank Design

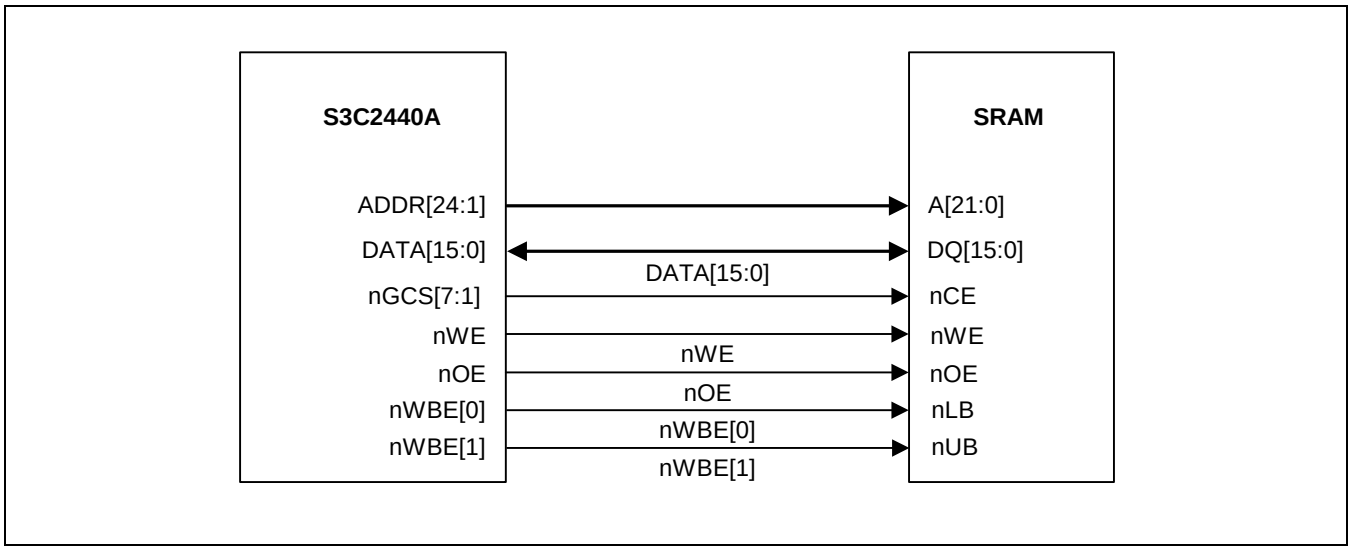


Figure 4-11. Halfword SRAM Bank Design with Halfword SRAM

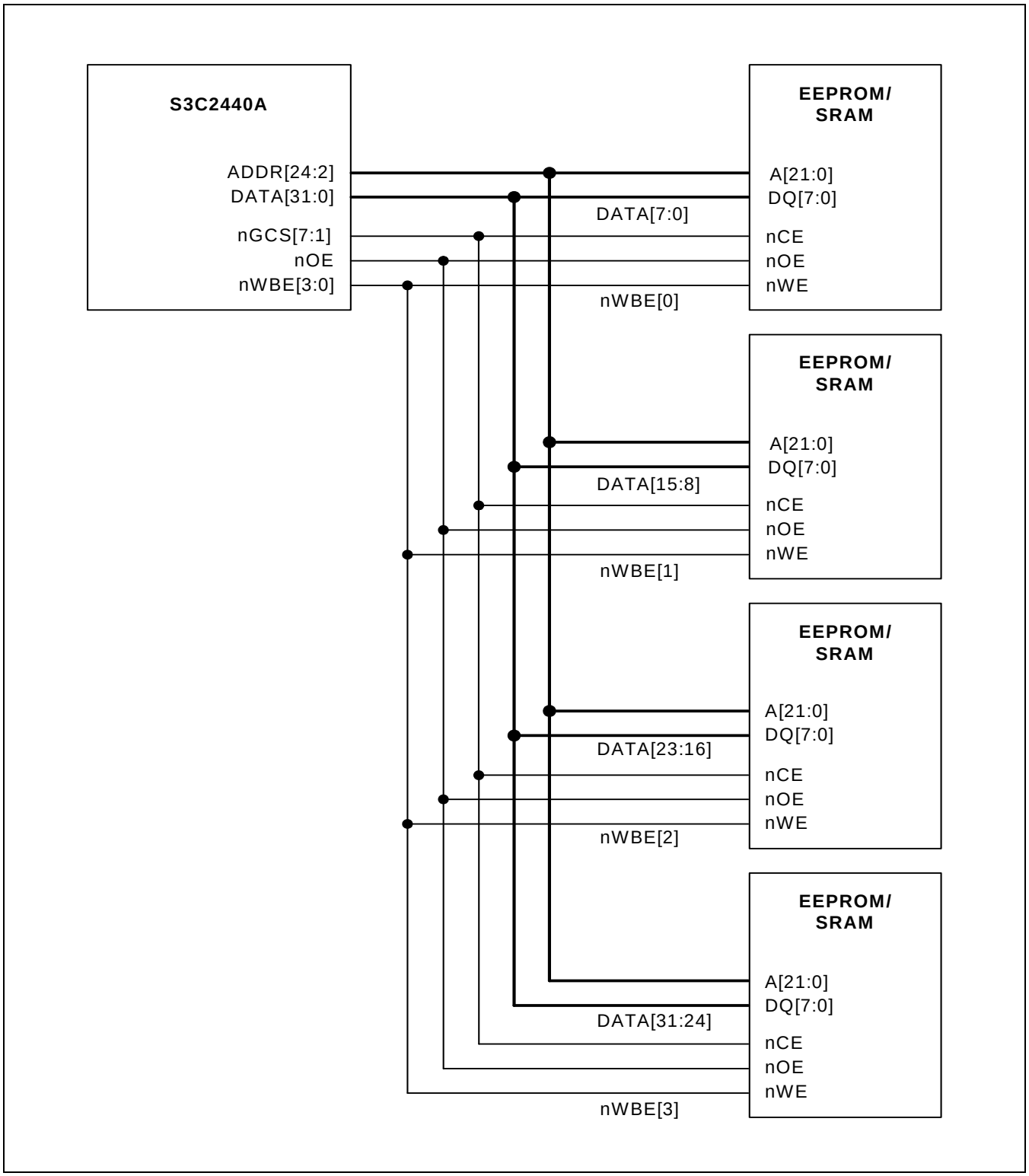


Figure 4-12. Word EEPROM/SRAM Bank Design

SDRAM BANK DESIGN

Table 4-5. SDRAM Bank Address Configuration

Bank Size	Bus Width	Base Component	Memory Configuration	Bank Address
2MByte	x8	16Mbit	(1M x 8 x 2Bank) x 1	A20
	x16		(512K x 16 x 2B) x 1	
4MB	x8	16Mb	(2M x 4 x 2B) x 2	A21
	x16		(1M x 8 x 2B) x 2	
	x32		(512K x 16 x 2B) x 2	
8MB	x16	16Mb	(2M x 4 x 2B) x 4	A22
	x32		(1M x 8x 2B) x 4	
	x8	64Mb	(4M x 8 x 2B) x 1	
	x8		(2M x 8 x 4B) x 1	A[22:21]
	x16		(2M x 16 x 2B) x 1	A22
	x16		(1M x 16 x 4B) x 1	A[22:21]
	x32		(512K x 32 x 4B) x 1	
16MB	x32	16Mb	(2M x 4 x 2B) x 8	A23
	x8	64Mb	(8M x 4 x 2B) x 2	
	x8		(4M x 4 x 4B) x 2	A[23:22]
	x16		(4M x 8 x 2B) x 2	A23
	x16		(2M x 8 x 4B) x 2	A[23:22]
	x32		(2M x 16 x 2B) x 2	A23
	x32		(1M x 16 x 4B) x 2	A[23:22]
	x8	128Mb	(4M x 8 x 4B) x 1	
	x16		(2M x 16 x 4B) x 1	
32MB	x16	64Mb	(8M x 4 x 2B) x 4	A24
	x16		(4M x 4 x 4B) x 4	A[24:23]
	x32		(4M x 8 x 2B) x 4	A24

Table 4-5. SDRAM Bank Address Configuration (Continued)

Bank Size	Bus Width	Base Component	Memory Configuration	Bank Address
32MB	x32	64Mb	(2M x 8 x 4B) x 4	A[24:23]
	x16	128Mb	(4M x 8 x 4B) x 2	
	x32		(2M x 16 x 4B) x 2	
	x8	256Mb	(8M x 8 x 4B) x 1	
	x16		(4M x 16 x 4B) x 1	
64MB	x32	128Mb	(4M x 8 x 4B) x 4	A[25:24]
	x16	256Mb	(8M x 8 x 4B) x 2	
	x32		(4M x 16 x 4B) x 2	
	x8	512Mb	(16M x 8 x 4B) x 1	
128MB	x32	256Mbit	(8M x 8 x 4Bank) x 4	A[26:25]
	x8	512Mb	(32M x 4 x 4B) x 2	
	x16		(16M x 8 x 4B) x 2	

The required SDRAM interface pin is CKE, SCLK, nSCS [1:0], nSCAS, nSRAS, DQM [3:0] and ADDR [12]/AP. The sample design with SDRAM is shown in Figure 4-13 and Figure 4-14.

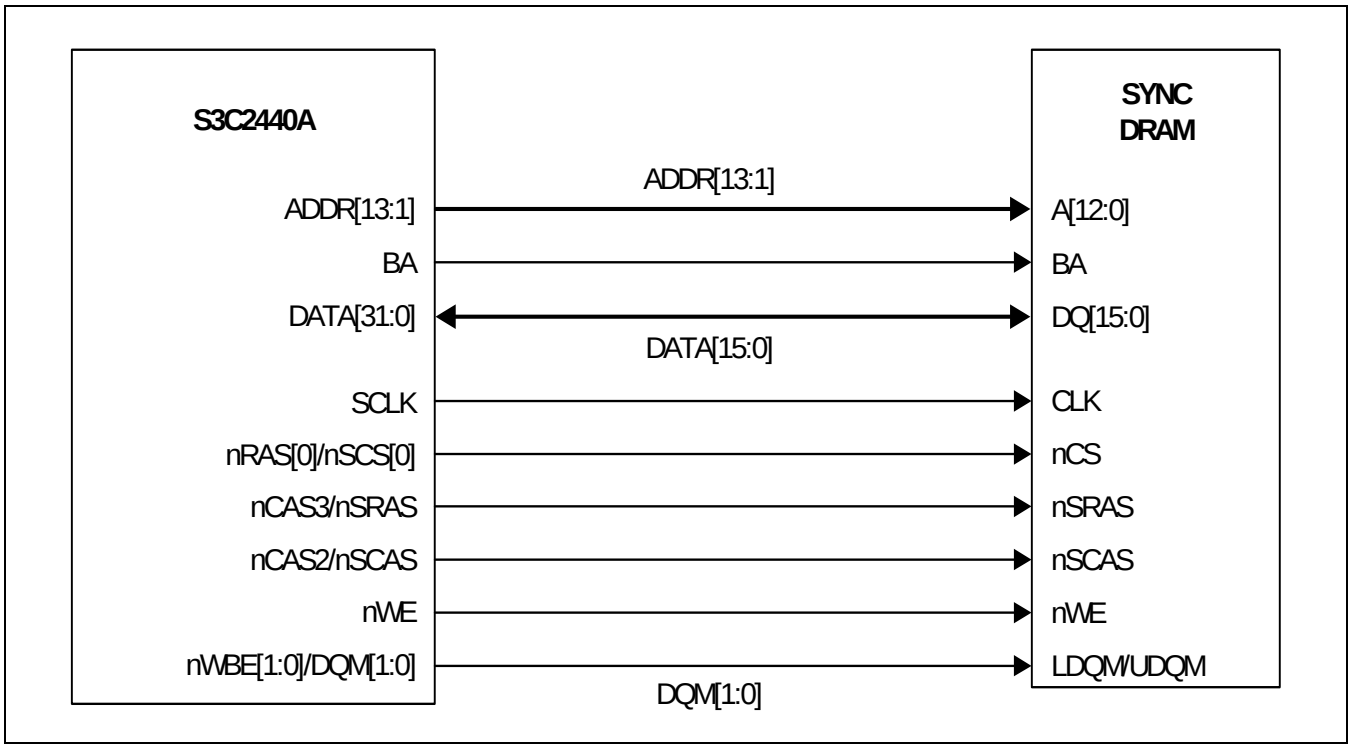


Figure 4-13. Halfword SDRAM Design with Halfword Component

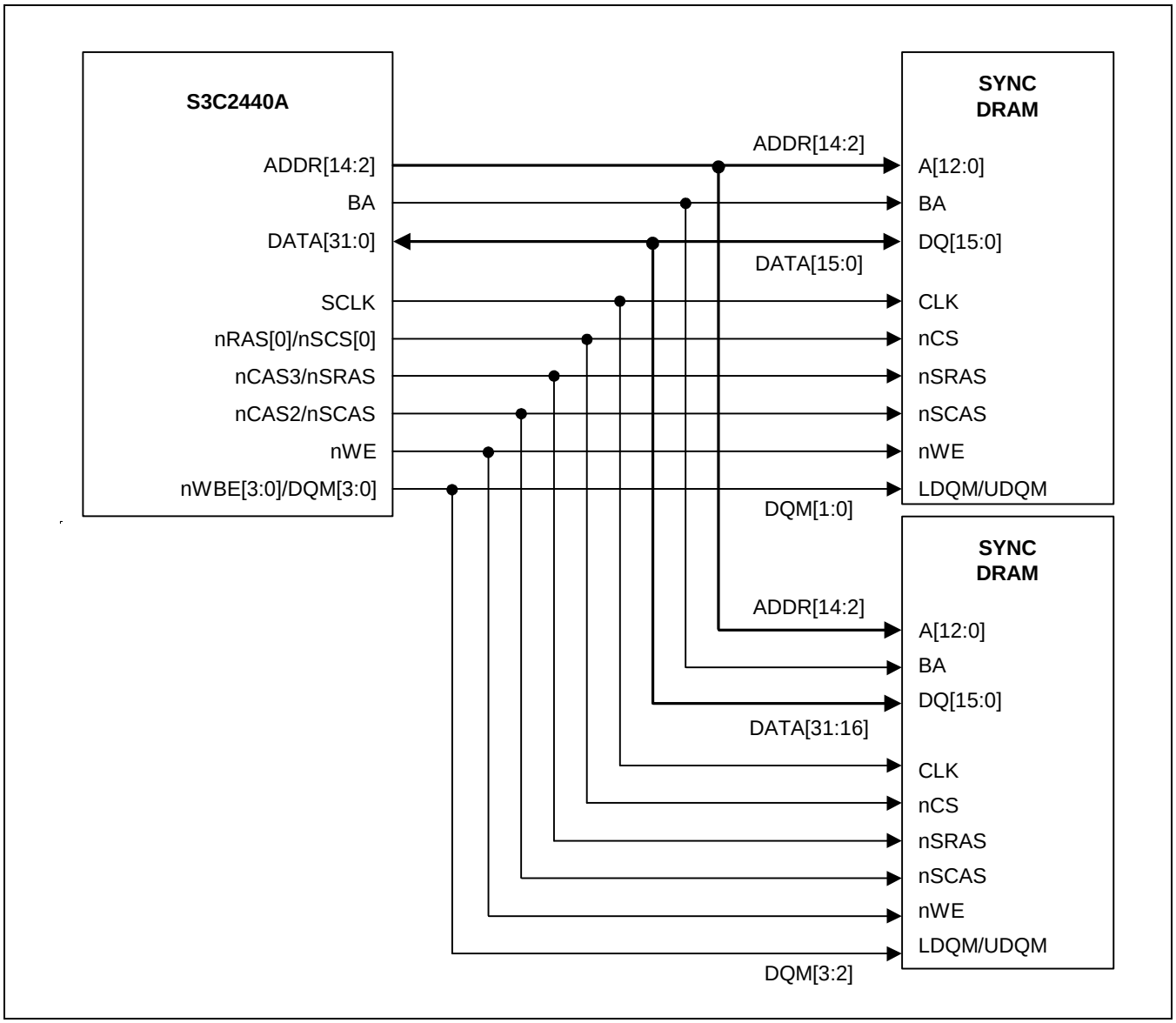


Figure 4-14. Word SDRAM Design with Half-word Component

3. NAND

Boot Rom Selection Guide

After the system reset, the S3C2440A accesses 0x00000000 address and configuring some system variables. Therefore, this special code (boot ROM image) should be located on the address 0x00000000. Booting device can be selected by setting OM [1:0] pins (Refer to Table 4-6).

Table 4-6. Booting device selection

OM0	OM1	Boot Memory
0	0	NAND boot
1	0	NOR boot (AMD)
0	1	Intel Strata boot

And also, H/W Information must be selected for Booting using flash memory.

Table 4-7. Booting device H/W Information

Pins	Description
NCON	NAND flash memory selection (Normal / Advance) 0: Normal NAND flash (256Words/512Bytes page size, 3/4 address cycle) 1: Advance NAND flash (1KWords/2KBytes page size, 4/5 address cycle)
GPG13	NAND flash memory page capacitance selection 0: Page=256Words(NCON = 0) or Page=1KWords(NCON = 1) 1: Page=512Bytes(NCON = 0) or Page=2KBytes(NCON = 1)
GPG14	NAND flash memory address cycle selection 0: 3 address cycle (NCON = 0) or 4 address cycle (NCON = 1) 1: 4 address cycle (NCON = 0) or 5 address cycle (NCON = 1)
GPG15	NAND flash memory bus width selection 0: 8-bit bus width 1: 16-bit bus width

NAND FLASH MEMORY CONFIGURATION

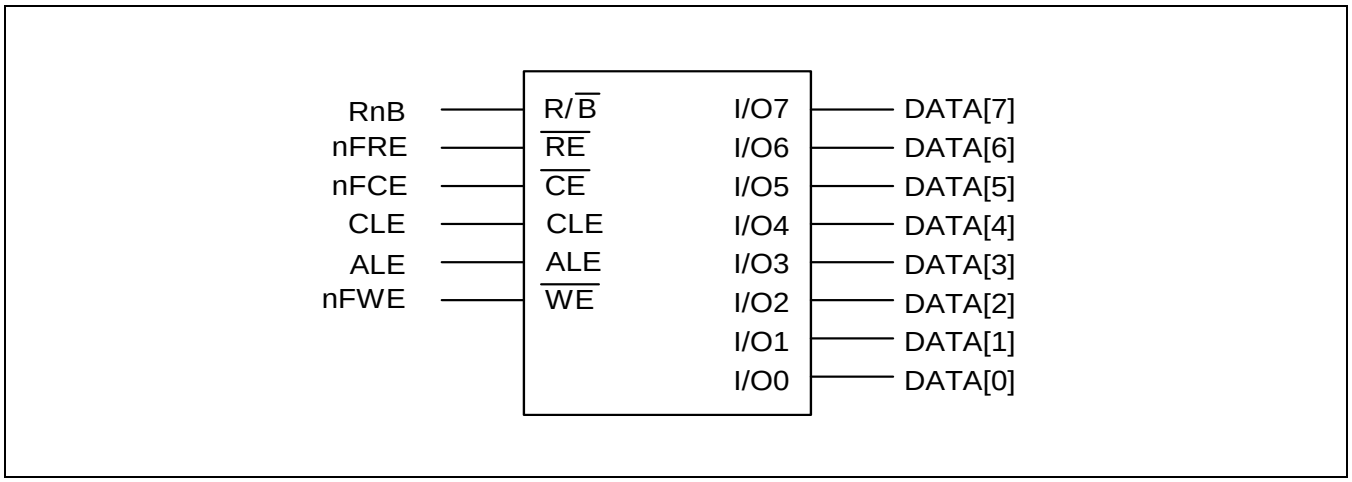


Figure 4-15. An 8-bit NAND Flash Memory Interface

When you write the address, the same address is issued from data [7:0] and data [15:8]

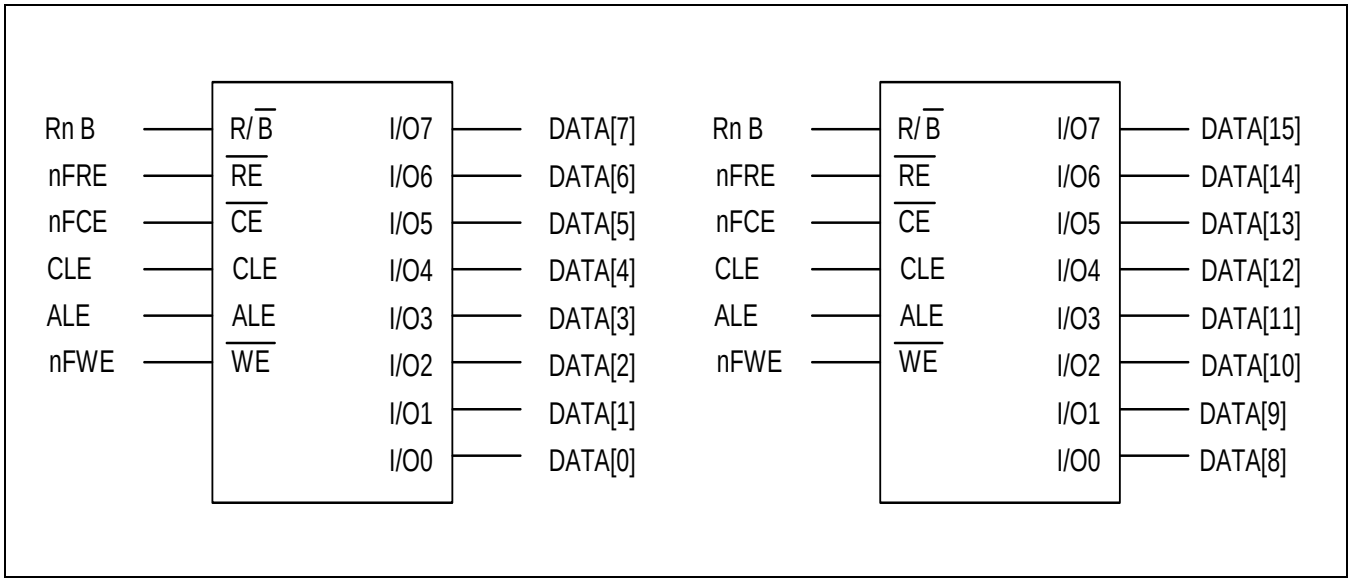


Figure 4-16. Two 8-bit NAND Flash Memory Interface

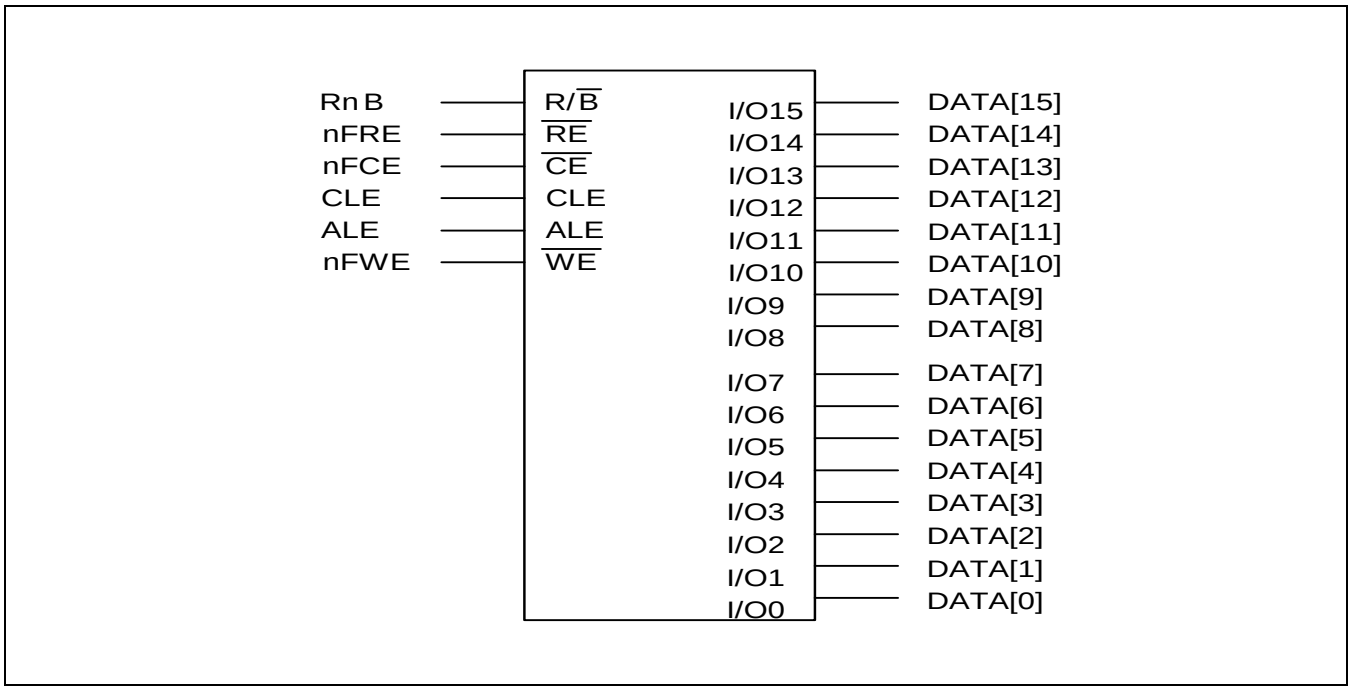


Figure 4-17. A 16-bit NAND Flash Memory Interface

NAND Boot Design Guide

NAND Flash controller signal functions are described in Table 4-8.

Table 4-8. NAND Flash Signal Description

Pins	Input/Output	Description
DATA [31:0]	Bidirectional	Input data during memory read and outputs data during memory write
nFCE	Output	Chip Select is activated when the address of a memory is within the address region of each bank
nFWE	Output	Write Enable indicates that the current bus cycle is a write cycle
nFRE	Output	Output Enable indicates that the current bus cycle is a read cycle
CLE	Output	NAND Flash Command Latch Enable
ALE	Output	NAND Flash Address Latch Enable
FRnB	Input	NAND Flash Ready and Busy
NCON	Input	NAND flash configuration If NAND flash controller isn't used, it has to be pull-up

Figure 4-18 shows a design with NAND boot memory. All applications processor signals are connected to the socket.

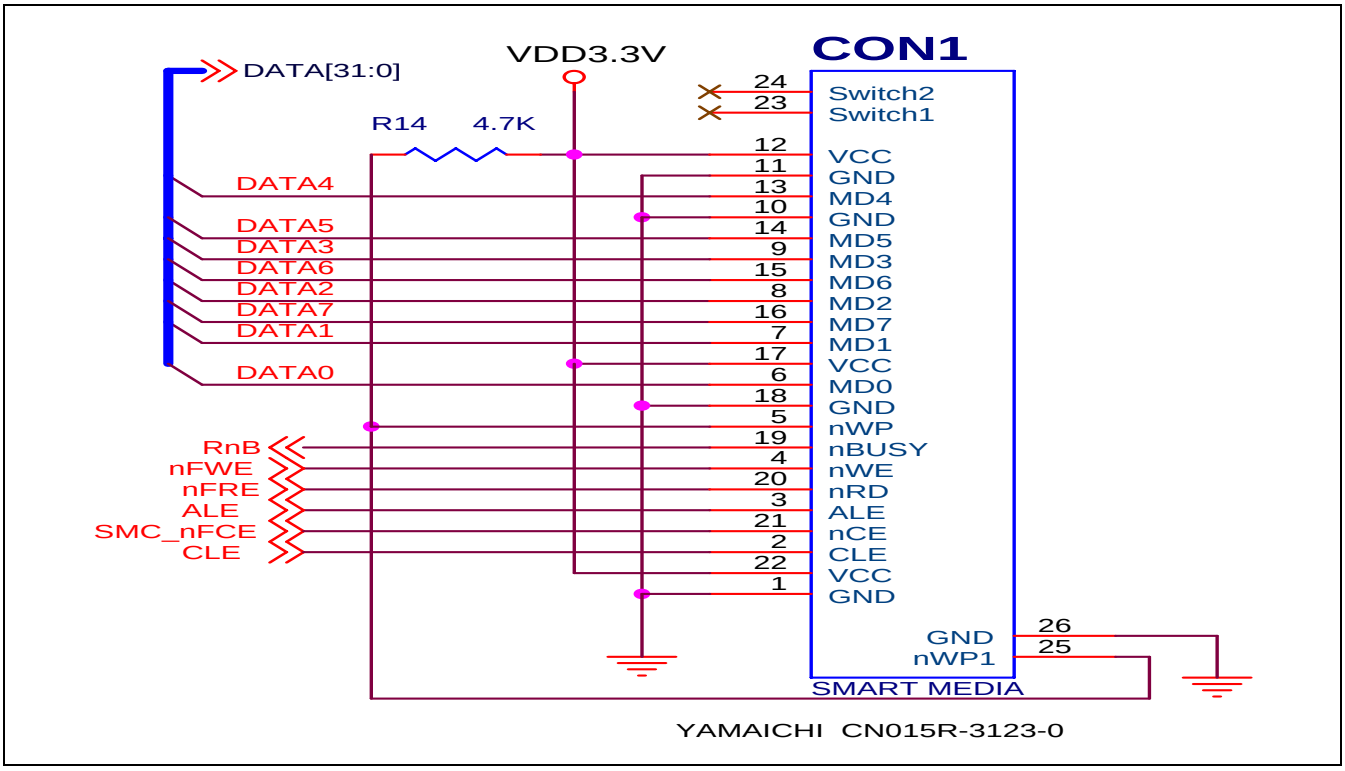


Figure 4-18. NAND Flash Circuit Example

Figure 4-19 shows a design when NAND Flash is not used

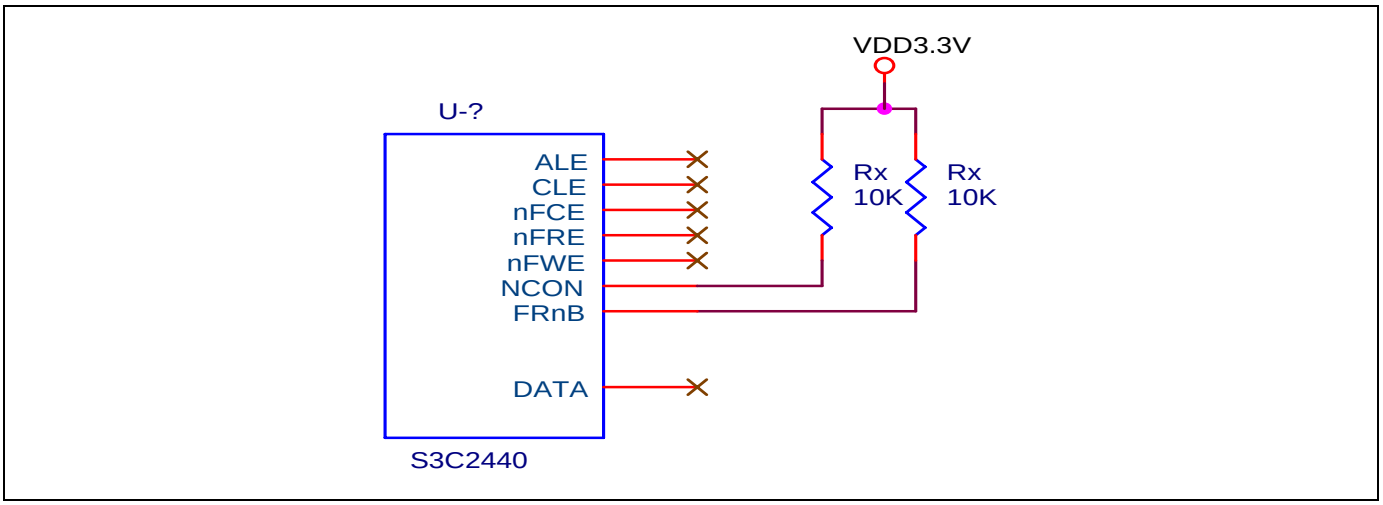


Figure 4-19. NAND Flash not used Circuit Example

4. UART

S3C2440A supports 3 UART channels. And each channel is capable of supporting IrDA 1.0 SIR (115.2Kbps).

When Using For RS-232 interface

Channel 0 can support flow control because RTS and CTS of that channel are pinned-out, whereas other two channels have data lines pinned-out without pinning out for flow control.

The Diagram below shows the example that connects channel 0 with RS-232 line driver/receiver chip.

However, when connecting channel 1 or 2 with RS-232 line driver/receiver chip, you should make pins related to flow control open.

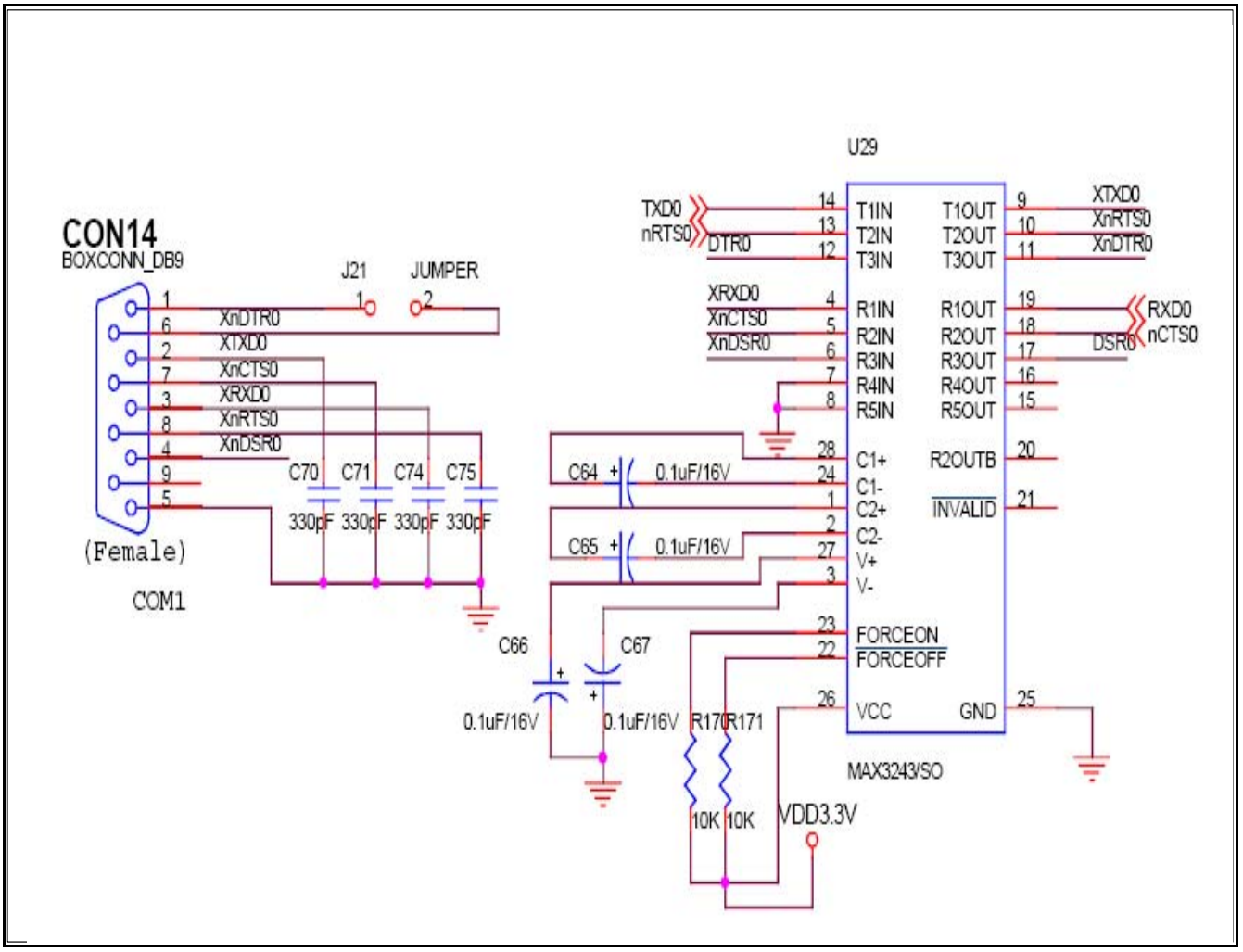


Figure 4-20. UART Connection Circuit Example

When Using For IrDA Interface

In this case, just connect arbitrary UART channel with IrDA transceiver that supports IrDA v1.0.

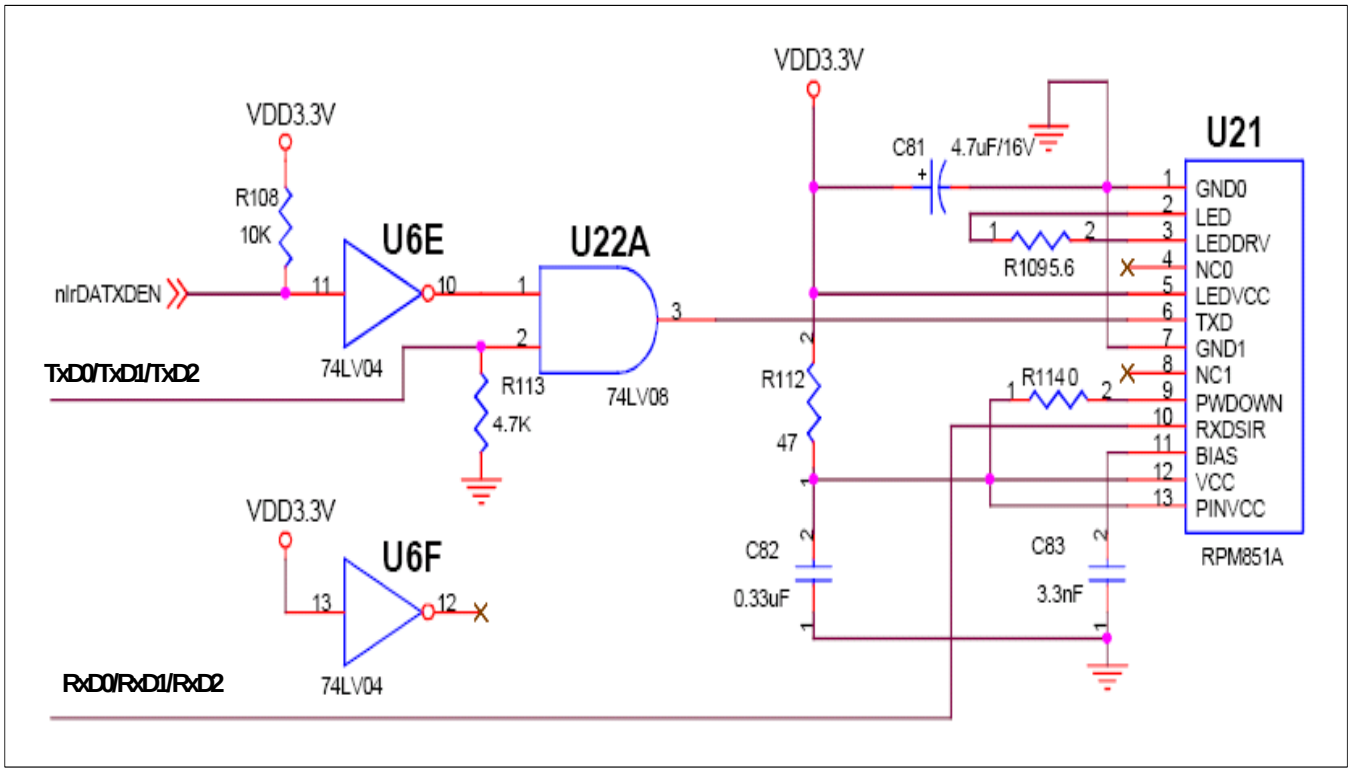


Figure 4-21. IrDA Connection Circuit Example

5. USB HOST / DEVICE

S3C2440A supports 2 USB host ports and 1 USB device port. USB host port 0 is only for Host, while USB host port 1 is for both USB host and USB device. So, you must pay attention to connection of USB host port 1 according to the application.

Connecting USB Host Port 0 with A-type Connector

S3C2440A USB host contains transceiver, but the transceiver doesn't buffer resistor and pull-down resistors. So, in order to connecting USB host port 0 with A-type connector, you need two resistors.

USB specification defines buffer impedance as 28Ω to 44Ω , and pull-down resistor as 15kΩ .

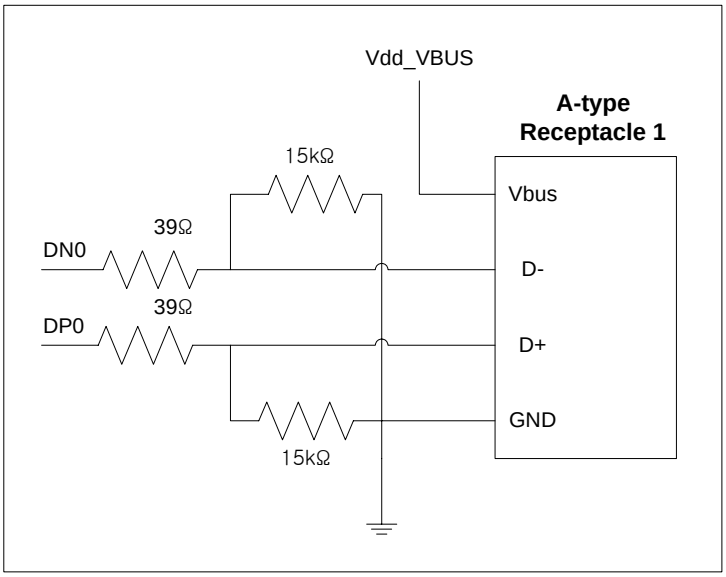


Figure 4-22. USB Host Connection Circuit Example with A-type Receptacle 1

Connecting USB Host Port1/USB Device Port0 with A-type Connector

In this case, just repeat like the description above.

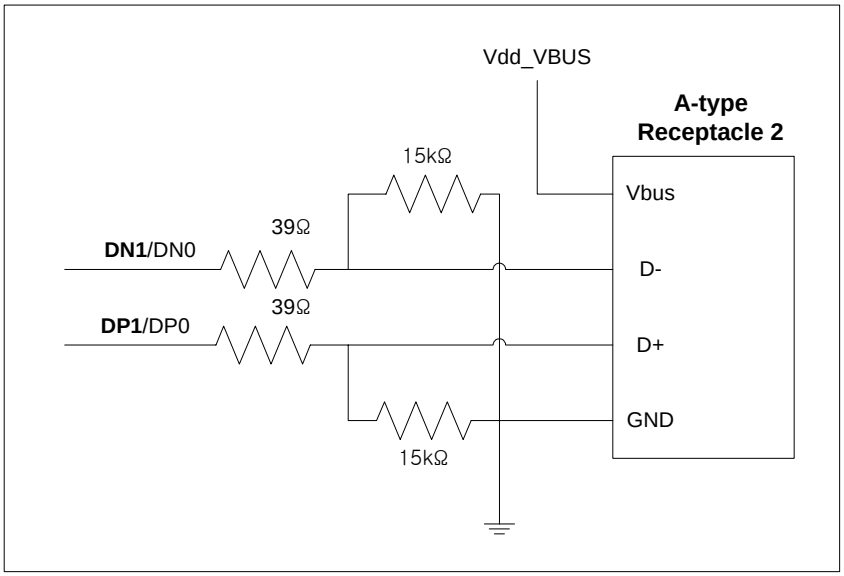


Figure 4-23. USB Host Connection Circuit Example with A-type Receptacle 2

Connecting USB Host Port1/USB Device Port0 with B-type Connector

When using USB host port1/USB device port0 for only USB device port, just connect like below diagram.

For your comprehension, additional explanation will be added. First, 39 Ω resistor is buffer impedance. And 470kΩ resistor is pull-down resistor for sleep mode, 1.5kΩ resistor stands for pull-up resistor specified in USB specification.

Additionally, AND gate of which inputs are EINT20/GPG12 and Vbus is a kind of trick making USB device connection/Disconnection recognized by USB host through S/W.

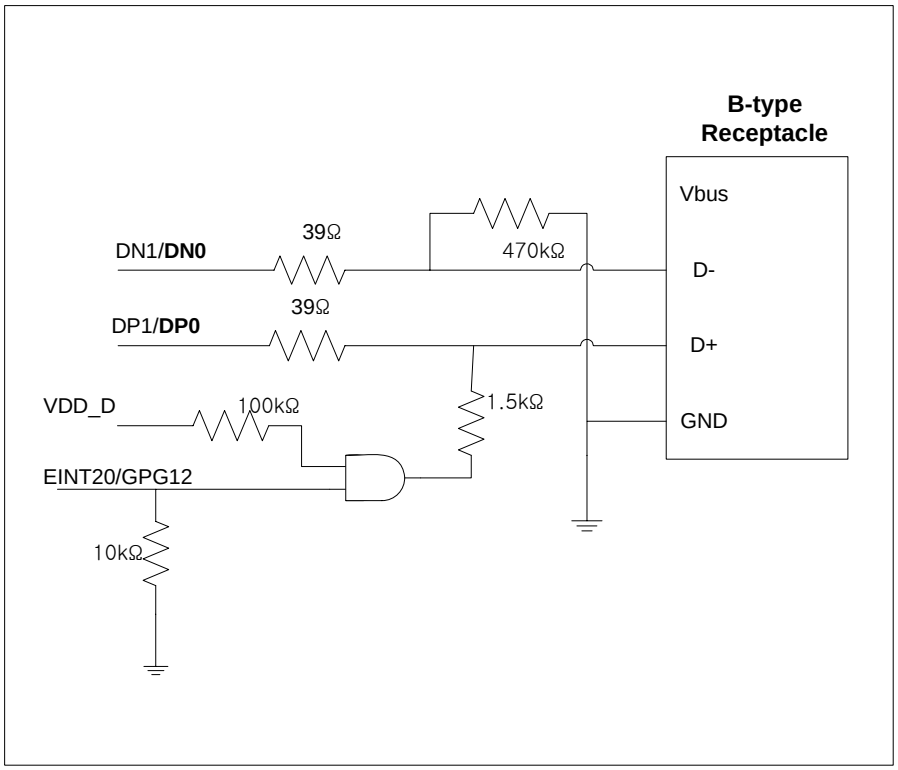


Figure 4-24. USB Device Connection Circuit Example with B-type Receptacle

Connection USB Host Port1/USB Device Port0 with A-type Connector/B-type Connector

As described before, USB host and device share DN1/DN0 pin and DP1/DP0 pin. Consequently, if you want to select one of two uses in the environment where both A-type connector and B-type connector exist around S3C2440A chip, you should connect or disconnect the port with connectors using jumpers.

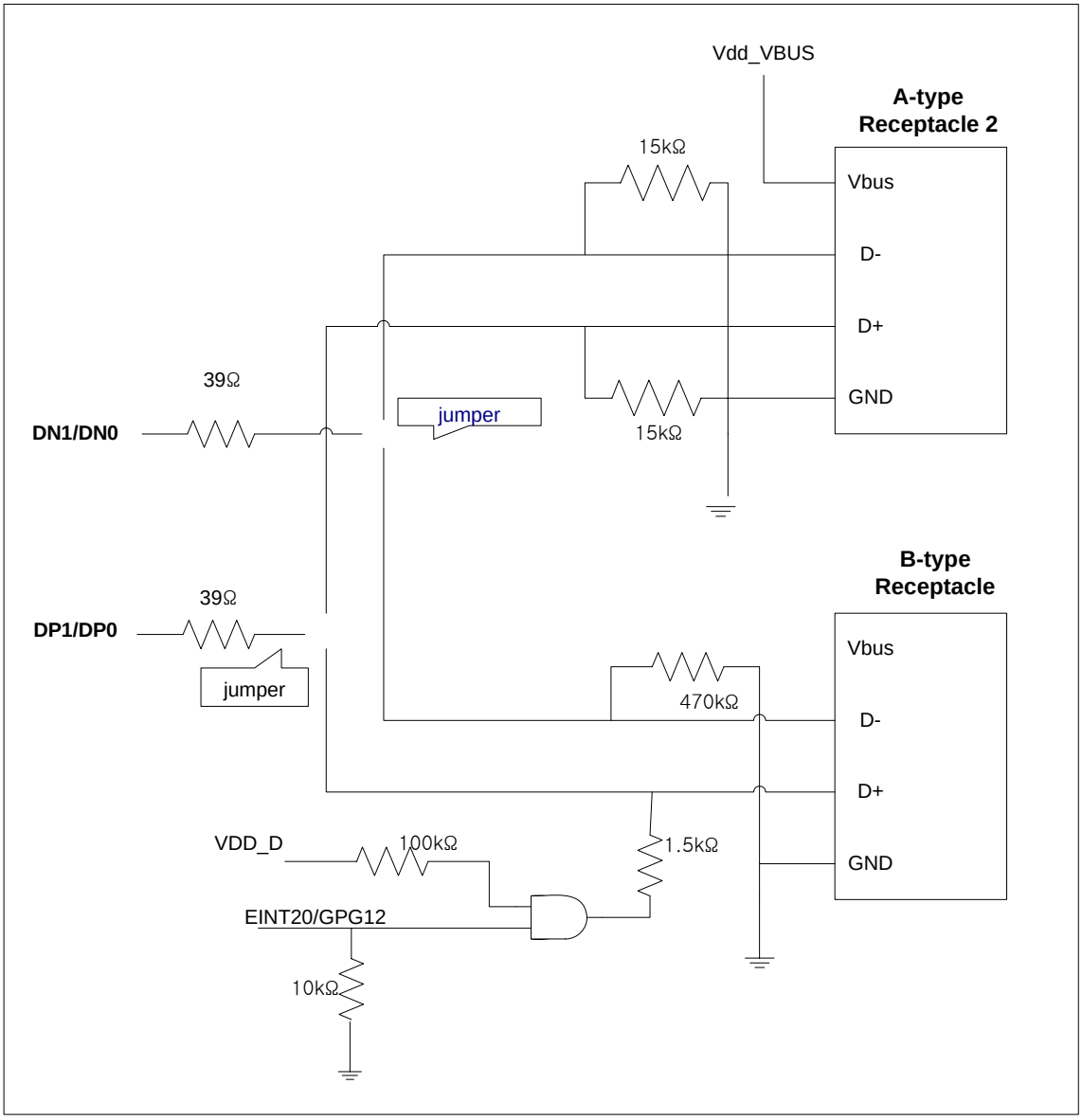


Figure 4-25. USB Host or Device Select Connection Circuit Example

6. LCD TFT / STN

Description

The LCD controller in the S3C2440A consists of the logic for transferring LCD image data from a video buffer located in system memory to an external LCD driver.

The LCD controller supports monochrome, 2-bit per pixel (4-level gray scale) or 4-bit per pixel (16-level gray scale) mode on a monochrome LCD, using a time-based dithering algorithm and Frame Rate Control (FRC) method and it can be interfaced with a color LCD panel at 8-bit per pixel (256-level color) and 12-bit per pixel (4096-level color) for interfacing with STN LCD.

It can support 1-bit per pixel, 2-bit per pixel, 4-bit per pixel, and 8-bit per pixel for interfacing with the palletized TFT color LCD panel, and 16-bit per pixel and 24-bit per pixel for non-palletized true-color display.

The LCD controller can be programmed to support different requirements on the screen related to the number of horizontal and vertical pixels, data line width for the data interface, interface timing, and refresh rate.

Schematics

The S3C2440A LCD interface example circuit is as follows:

- UG-32F04 (320x240 mono STN LCD) from SAMSUNG DISPLAY DEVICES CO., LTD. (refer to Figure 4-14)
  - TL497CAN can be used to make VEE (-25V).

- UG-24U03A (320x240 mono STN LCD) from SAMSUNG DISPLAY DEVICES CO., LTD. (refer to Figure 4-15)
  - The circuit on LCD module generates VEE.
  - VL is 2.4V typically.
  - DISPON H: display on, L: display off
  - nEL_ON H: EL off L: EL on

- KHS038AA1AA-G24 (256 color STN LCD) from KYOCERA Co. (refer to Figure 4-16)
  - DISP signal can be made using I/O port, or power control circuit or nRESET circuit.
  - V1-V5 can be made using the power circuit recommended by the LCD specification.

- LTS350Q1-PE1 (256K color TFT LCD) from SAMSUNG ELECTRONICS CO., LTD. (refer to Figure 4-17)
  - VDD_LCDI is typically 3.3V.

- LP104V2-W (262,144 color TFT LCD, 10.4”) from LG Philips (refer to Figure 4-18)
  - VDD_LCDI is typically 3.3V.

- V16C6448AB (640x480 TFT LCD) from PRIMEVIEW (refer to Figure 4-19)
  - VDD_LCDI, VD and control signal are typically 5.V.

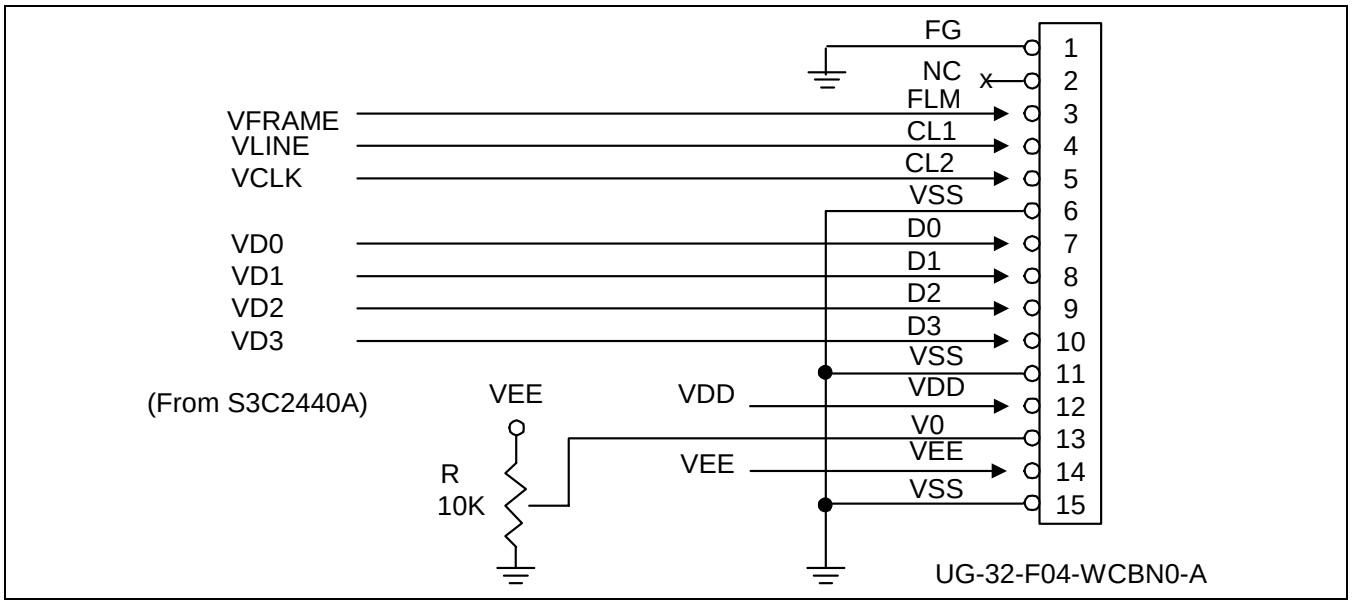


Figure 4-26. UG-32F04 Connection with S3C2440A (320x240 Mono STN LCD)

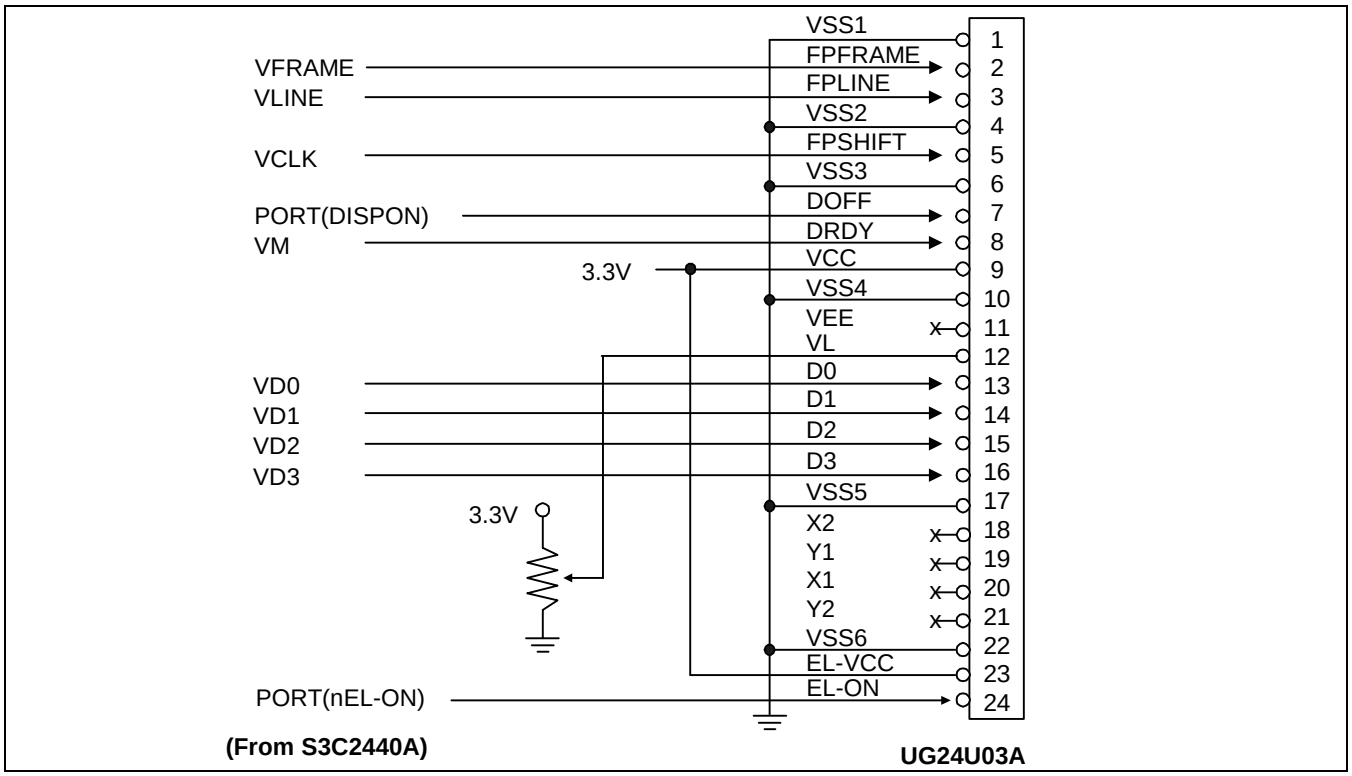


Figure 4-27. UG24U03A Connection with S3C2440A (320x240 Mono STN LCD)

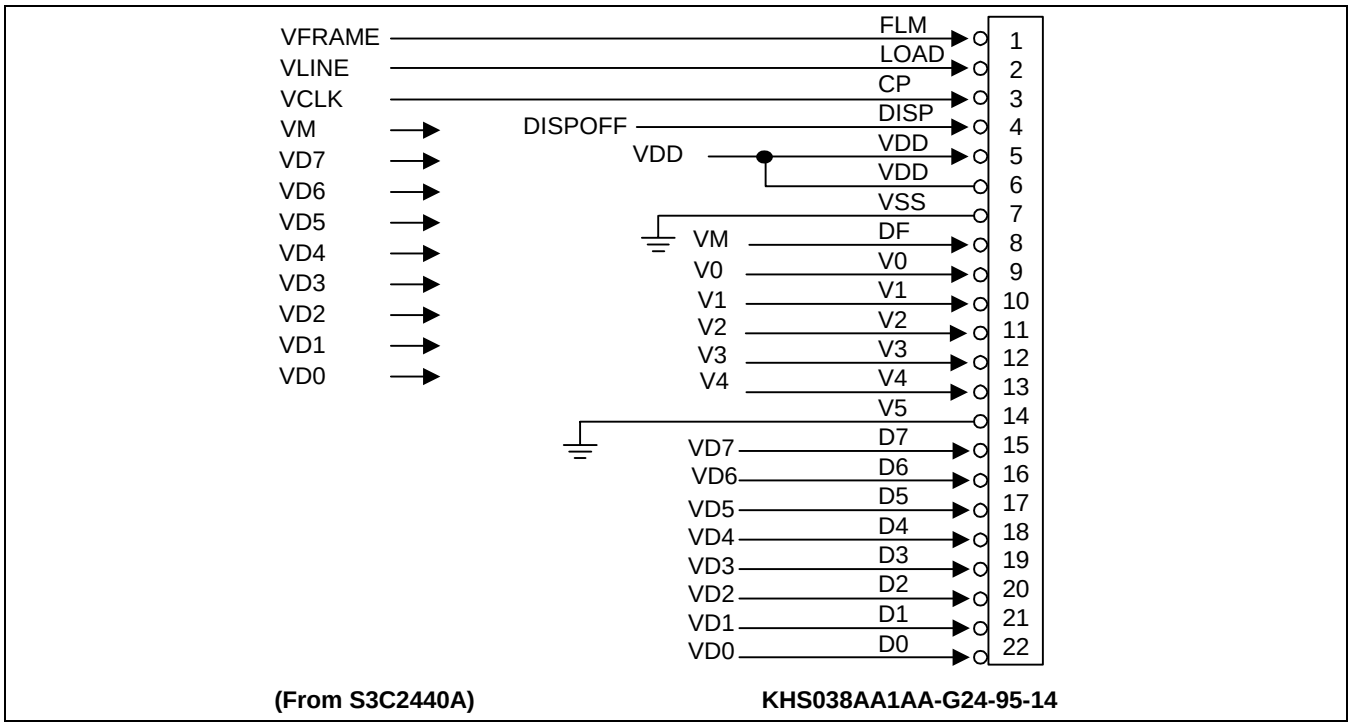


Figure 4-28. KHS038AA1AA-G24 Connection with S3C2440A (256 Color STN LCD)

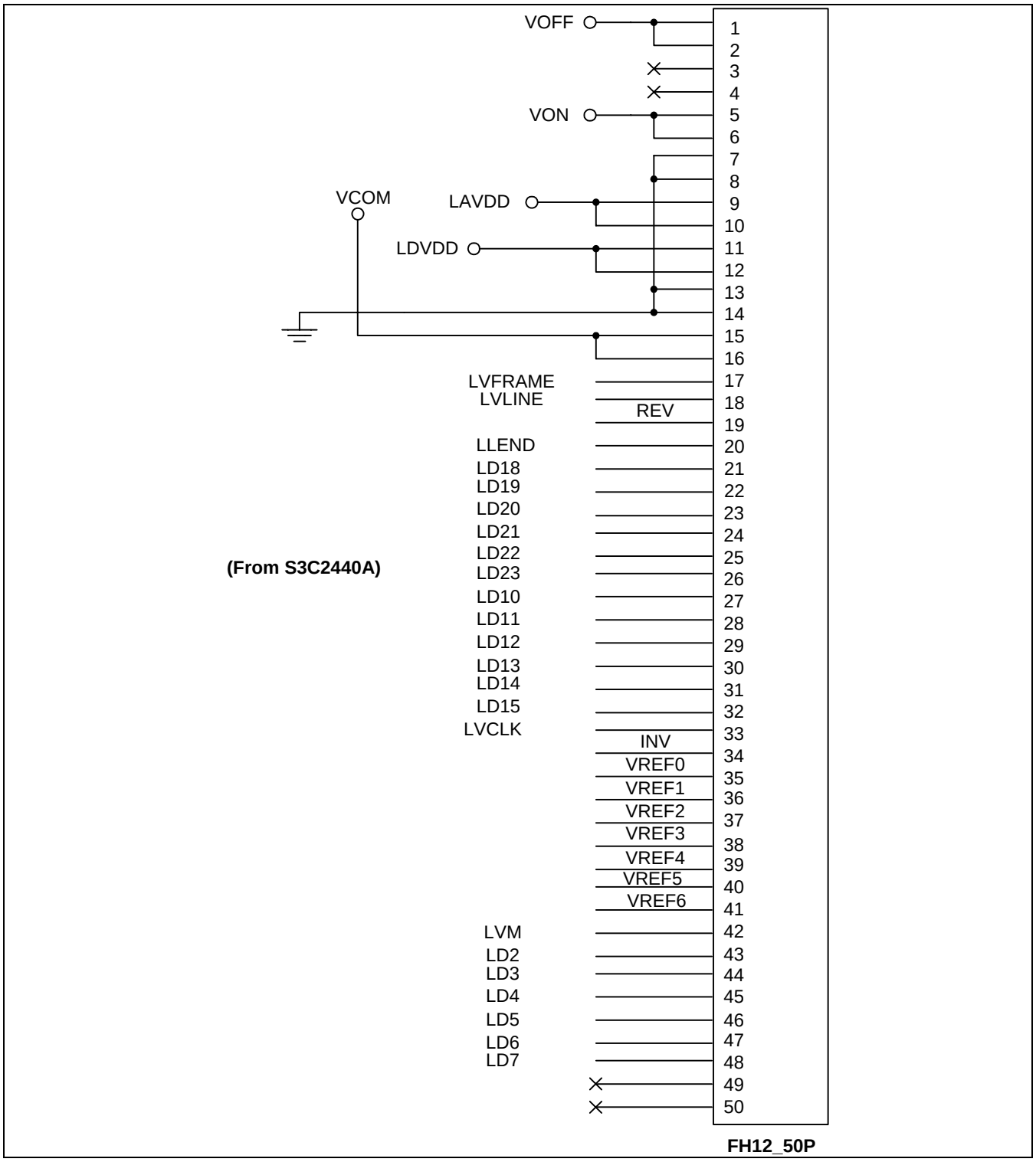


Figure 4-29. LTS350Q1-PE1 Connection with S3C2440A (Samsung 3.5” Transflective TFT LCD)

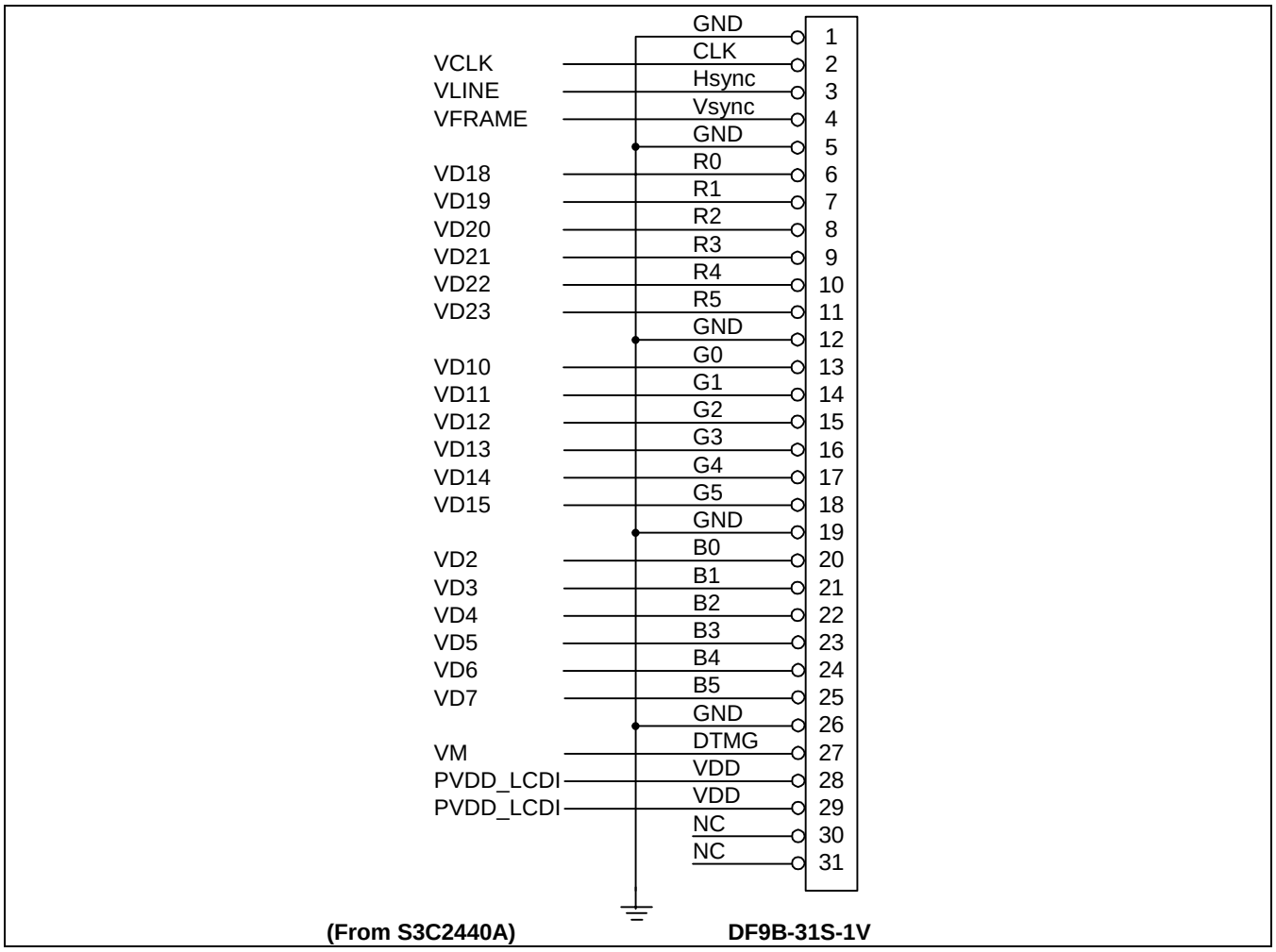


Figure 4-30. LP104V2-W Connection with S3C2440A (LG Philips 10.4” TFT LCD)

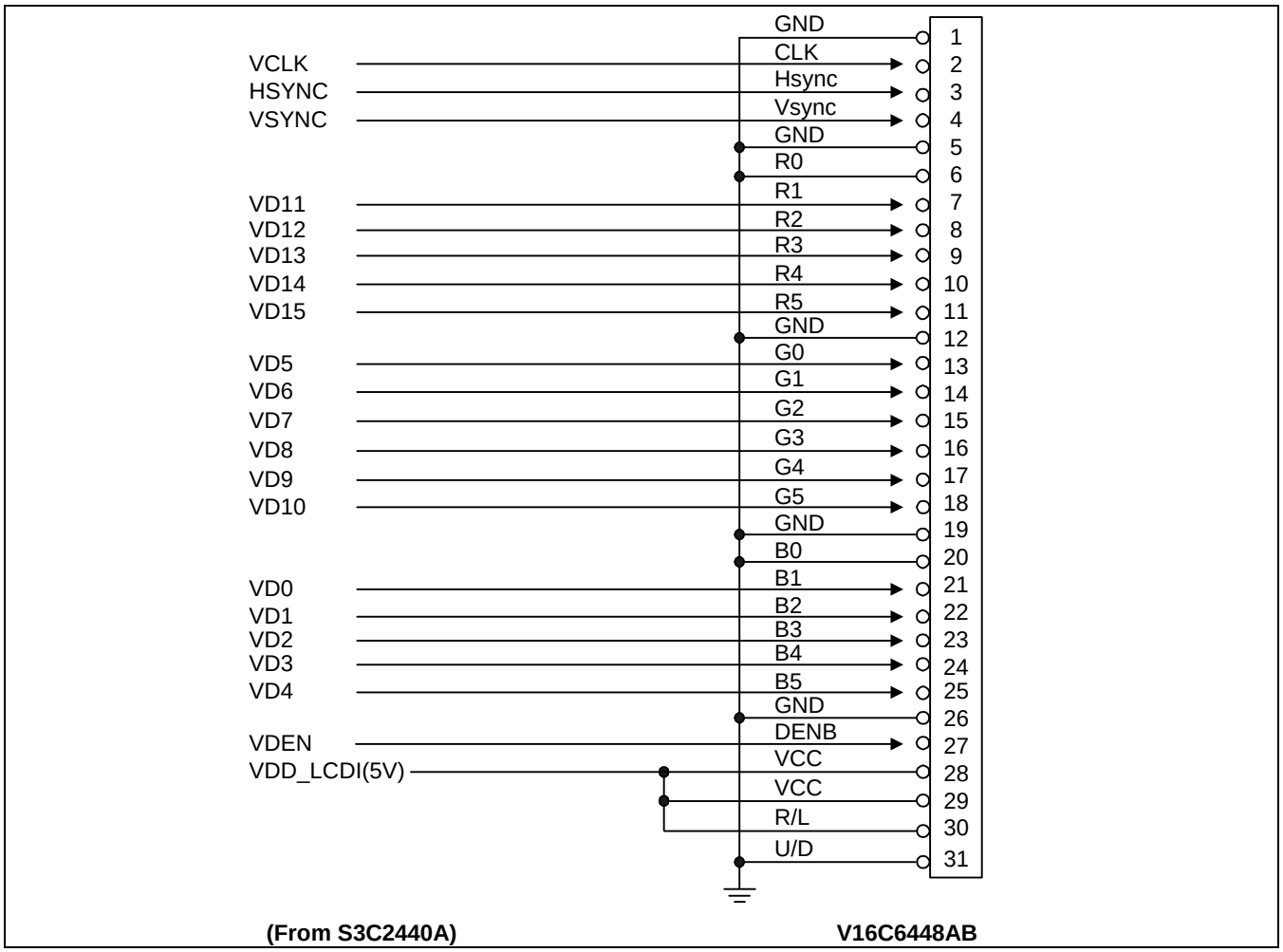


Figure 4-31. V16C6448AB Connection with S3C2440A (TFT LCD)

Not Used

- All Pin leave as a No Connect.
- VD [23:0], LCD_PWREN, VCLK, VFRAME, VLINE, VM, VSYNC, HSYNC, VDEN, LEND, STV, CPV, LCD_HCLK, TP, STH, LCD_LPCOE, LCD_LPCREV, LCD_LPCREVB

7. A/D Converters and Touch Screen

OVERVIEW

The 10-bit CMOS ADC (Analog to Digital Converter) is a recycling type device with 8-channel analog inputs. It converts the analog input signal into 10-bit binary digital codes at a maximum conversion rate of 500KSPS with 2.5MHz A/D converter clock. A/D converter operates with on-chip sample-and-hold function and power down mode is supported.

Touch Screen Interface can control/select pads (XP, XM, YP, YM) of the Touch Screen for X, Y position conversion. Touch Screen Interface contains Touch Screen Pads control logic and ADC interface logic with an interrupt generation logic.

ADC & TOUCH SCREEN INTERFACE OPERATION

BLOCK DIAGRAM

Figure 4-32 shows the functional block diagram of A/D converter and Touch Screen Interface. Note that the A/D converter device is a recycling type.

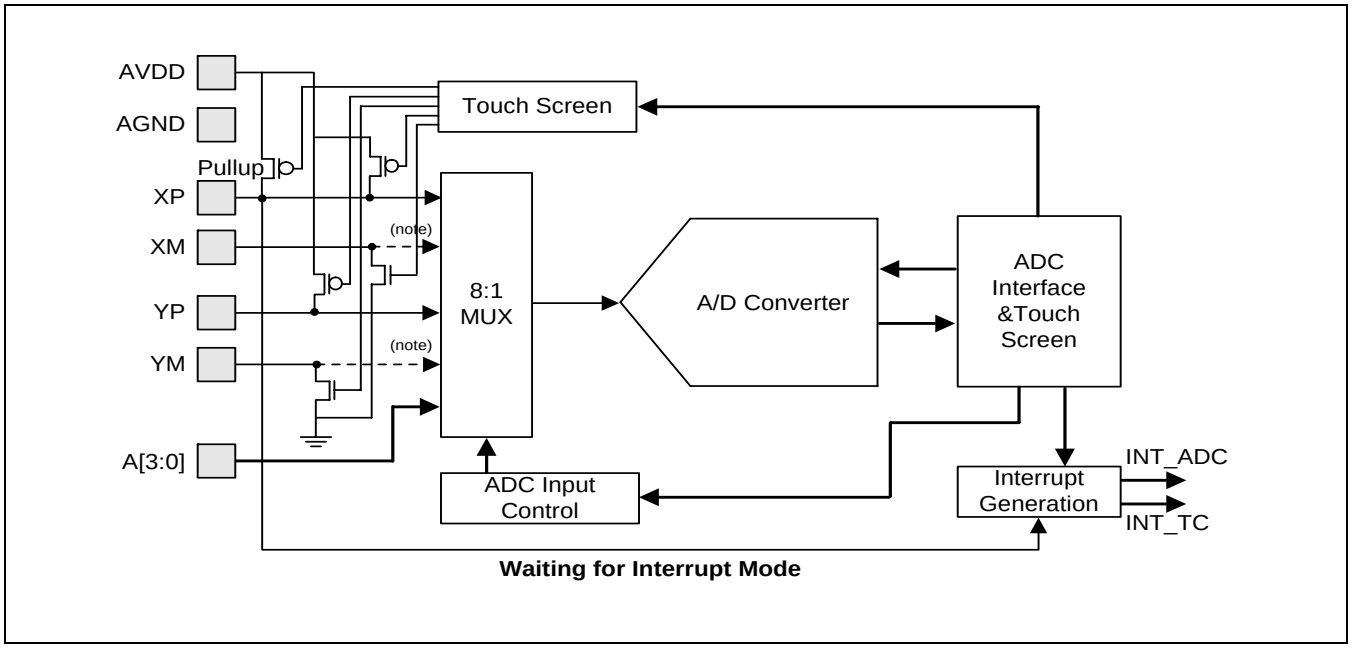


Figure 4-32. ADC and Touch Screen Interface Functional Block Diagram

NOTE: (symbol)

When Touch Screen device is used; XM or PM is only connected ground for Touch Screen I/F.
When Touch Screen device is not used, XM or PM is connecting Analog Input Signal for Normal ADC conversion.

Touch Screen Interface Mode

1. Normal Conversion Mode

   Single Conversion Mode is the most likely used for General Purpose ADC Conversion. This mode can be initialized by setting the ADCCON (ADC Control Register) and completed with a read and a write to the ADCDAT0 (ADC Data Register 0).

2. Separate X/Y position conversion Mode

   Touch Screen Controller can be operated by one of two Conversion Modes. Separate X/Y Position Conversion Mode is operated as the following way. X-Position Mode writes X-Position Conversion Data to ADCDAT0, so Touch Screen Interface generates the Interrupt source to Interrupt Controller. Y-Position Mode writes Y-Position Conversion Data to ADCDAT1, so Touch Screen Interface generates the Interrupt source to Interrupt Controller.

3. Auto (Sequential) X/Y Position Conversion Mode

   Auto (Sequential) X/Y Position Conversion Mode is operated as the following. Touch Screen Controller sequentially converts X-Position and Y-Position that is touched. After Touch controller writes X-measurement data to ADCDAT0 and writes Y-measurement data to ADCDAT1, Touch Screen Interface is generating Interrupt source to Interrupt Controller in Auto Position Conversion Mode.

4. Waiting for Interrupt Mode

   Touch Screen Controller generates interrupt (INT_TC) signal when the Stylus is down. Waiting for Interrupt Mode setting value is rADCTSC=0xd3; // XP_PU, XP_Dis, XM_Dis, YP_Dis, YM_En.

   After Touch Screen Controller generates interrupt signal (INT_TC), Waiting for interrupt Mode must be cleared. (XY_PST sets to the No operation Mode)

Standby Mode

Standby mode is activated when ADCCON [2] is set to '1'. In this mode, A/D conversion operation is halted and ADCDAT0, ADCDAT1 register contains the previous converted data.

Programming Notes

1. The A/D converted data can be accessed by means of interrupt or polling method. With interrupt method the overall conversion time - from A/D converter start to converted data read - may be delayed because of the return time of interrupt service routine and data access time. With polling method, by checking the ADCCON [15] - end of conversion flag-bit, the read time from ADCDAT register can be determined.
2. Another way for starting A/D conversion is provided. After ADCCON [1] - A/D conversion start-by-read mode-is set to 1, A/D conversion starts simultaneously whenever converted data is read.

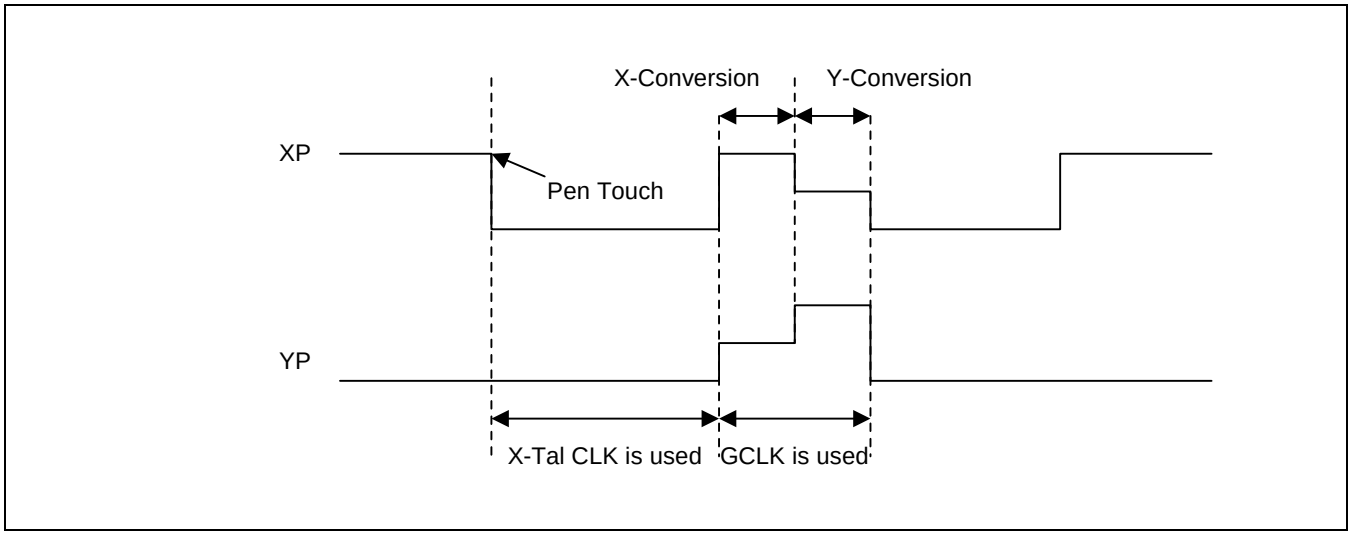


Figure 4-33. ADC and Touch Screen Operation signal

8. RTC

Description

The backup battery can operate the Real Time Clock (RTC) unit while the system power is off. The RTC can transmit 8-bit data to CPU as Binary Coded Decimal (BCD) values using the STRB/LDRB ARM operation. The data include the time by second, minute, hour, date, day, month, and year. The RTC unit works with an external 32.768kHz crystal and also can perform the alarm function.

Using RTC Unit

The schematics for an RTC connection are shown in Figure 4-34.

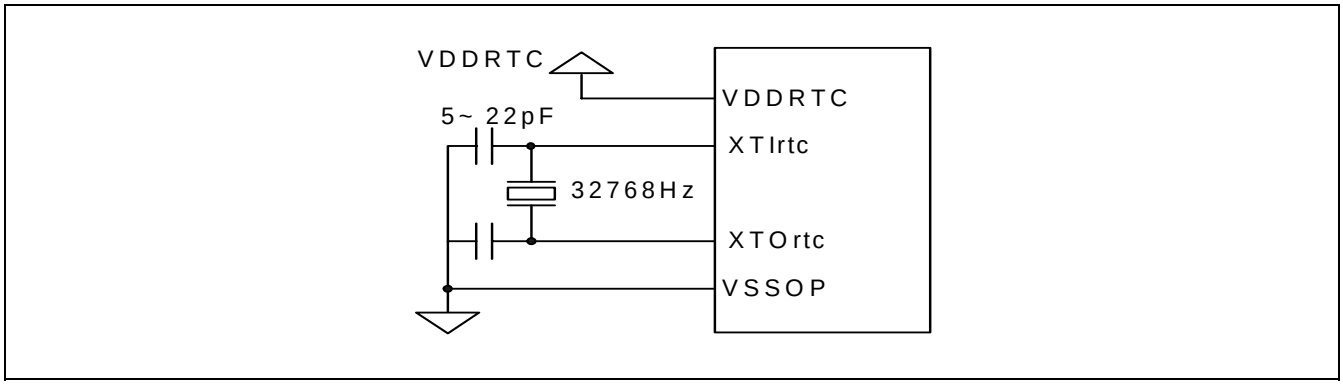


Figure 4-34. RTC Connection

The RTC unit works only with the attachment of a 32.768KHz crystal.
But depending on the parasitic capacitance of PCB etc., accuracy of the clock is not always good.
For a better accuracy of the clock, some adjustment is necessary.

The load capacitance (CL) of the crystal is a critical parameter. The CL is not the capacitance of the crystal itself. CL means an external capacitance in parallel with the crystal. Each crystal manufacturer offers several different CL value crystals with the same frequency. When a crystal is connected to an oscillator circuit, if the specified CL value and external capacitance value in parallel with the crystal are the same, the frequency will be the specified value at normal temperature (25°C).

For example, in the Figure 4-35,

When CP+C1×C2/(C1+C2) = CL, the crystal oscillates at its nominal frequency (32768Hz).
When CP+C1×C2/(C1+C2) > CL, the crystal oscillates slower than 32768Hz.
Further, when CP+C1×C2/(C1+C2) < CL, the crystal oscillates faster than 32768Hz.

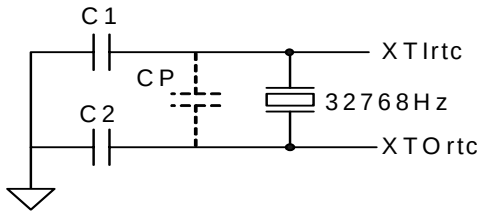


Figure 4-35. Example

If you choose a crystal with small CL, you can make C1 and C2 small and most characteristics will be improved.

Unused RTC Unit

The schematics for an unused RTC connection are shown in Figure 4-36.

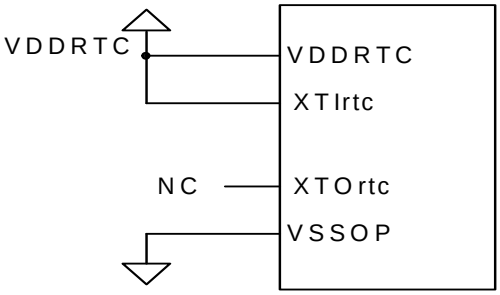


Figure 4-36. Unused RTC Connection Example

XTOrtc pin leaves as a No Connect.

9. SDI (Secure Digital Interface)

The SD Card is a low cost data storage and communication media. The SD Card supports the translation protocol from a standard SDI or Serial Peripheral Interface (SPI) bus to an application bus.

The SDI controller in the applications processor is compliant with The SD Memory Card Spec, Version1.0 System Specification and The MultiMedia Card System Specification, Version 2.11 and SDIO Card Spec, Version1.0. The SDI controller is capable of communicating with a card in SD or SPI mode. Your application is responsible for specifying the SDI controller communication mode.

Signal Description

SDI controller signal functions are described in Table 4-9.

The signals defined in the Physical Layer Specification of the SD Memory Card Specifications for an SD Card device are CLK, CMD, and DAT0-DAT3. The obvious difference is the number of DAT signals. In addition, the socket for an SD Card contains mechanical switches for write protect (WP) and card detect (CD).

Table 4-9. SDI Signal Description

Signal Name	Input/Output	Description
SDCLK	Output	Clock signal to SD Card
SDCMD	Bidirectional	Command line
SDDATA0 ~ SDDATA3	Bidirectional	Data line

How to Wire

Notice in the example schematic (Figure 4-10, “Applications Processor SD Card Signal Connections”) an SD Card socket is used. The signals on the socket are defined in Table 4-10.

Table 4-10. SD Card Socket Signals

Signal Name	Pin #
CD/DAT3	1
CMD	2
VSS1	3
VDD	4
CLK	5
VSS2	6
DAT0	7
DAT1	8
DAT2	9

The SDI controller can be connected to either an MMC device or an SD Card device, but you are limited to which device installs in which socket. Refer to Table 4-11 for information on sockets and device supported by the SDI controller.

Table 4-11. SDI Controller Supported Sockets and Devices

Sockets	Devices supported
SD Card socket	SD Card device MMC device
MMC socket	MMC device

Simplified Schematic

Figure 4-37 shows another SD Card socket. In this case, all applications processor signals are connected to the socket. This socket does not have a common signal for the write protect and card detect. Inserting a card into the socket may cause the write protect signal and will cause the card detect signal to change states and must be interpreted by the CPLD software.

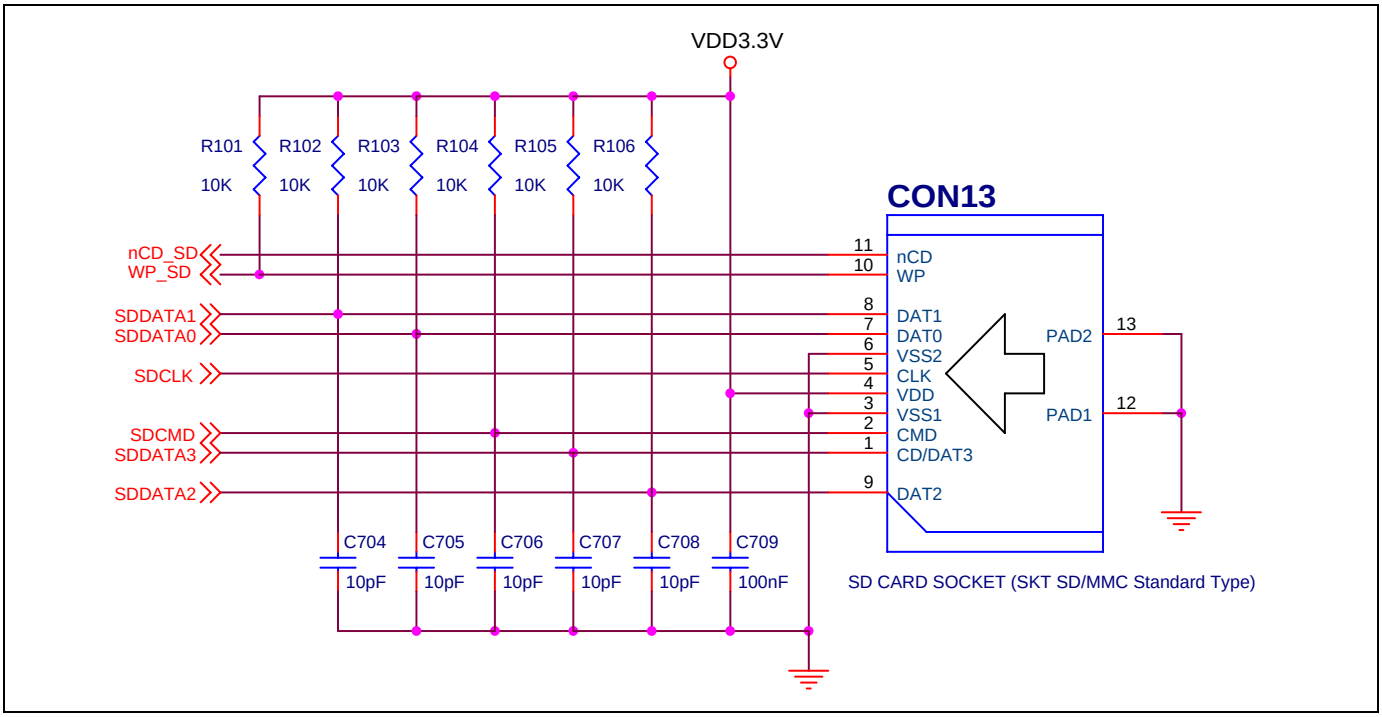


Figure 4-37. SD Card Circuit Diagram

Figure 4-38 shows a design when NAND Flash is not used

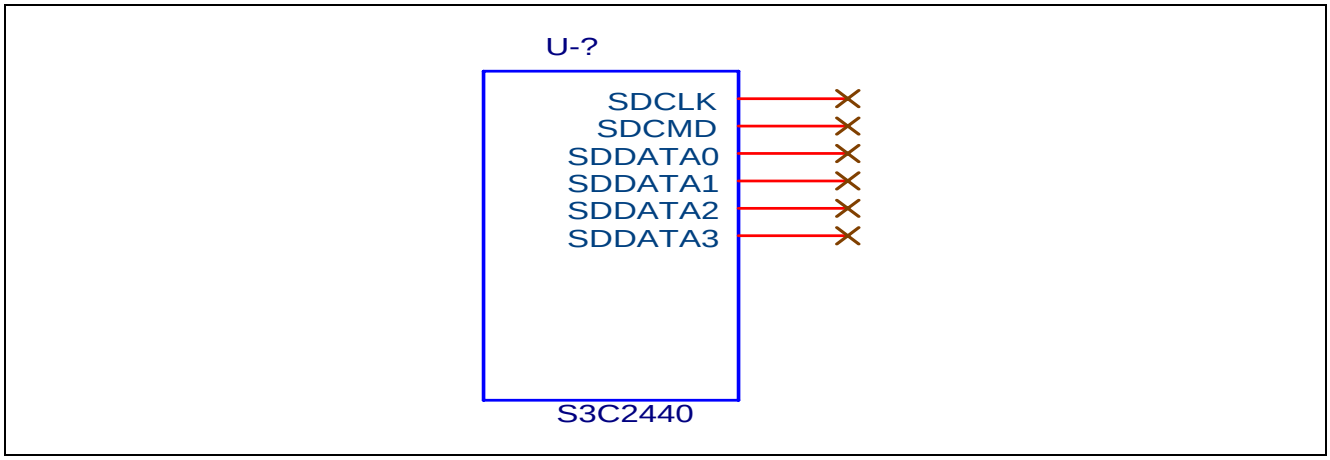


Figure 4-38. Circuit Diagram when not using SD card

Pull-up and Pull-down

Table 4-12 show the pull-up and pull-down resistors required for SD Card devices according to their respective specifications.

Table 4-12. SD Card Pull-up and Pull-down Resistors

Signal	Pull-up or Pull-down	Min	Max	Remark
CMD	Pull-up	10K	100K	Prevents bus floating
DAT0~DAT3	Pull-up	10K	100K	Prevents bus floating
WP1	Pull-up	-	-	Any value sufficient to prevent bus floating
NOTE: 1. This resistor is shown in the specification but the value is not specified				

10. IIC

S3C2440A supports a multi-master IIC-bus serial interface. If you just connect two IIC lines(SCL, SDA) with arbitrary IIC chip that supports IIC interface, the IIC communication will be possible.

Connecting S3C2440 IIC line with other IIC chip

This diagram shows a example connecting S3C2440 IIC lines with IIC lines of EEPROM. By the way, you should use pull-up resistors in order for data lines to maintain default HIGH state.

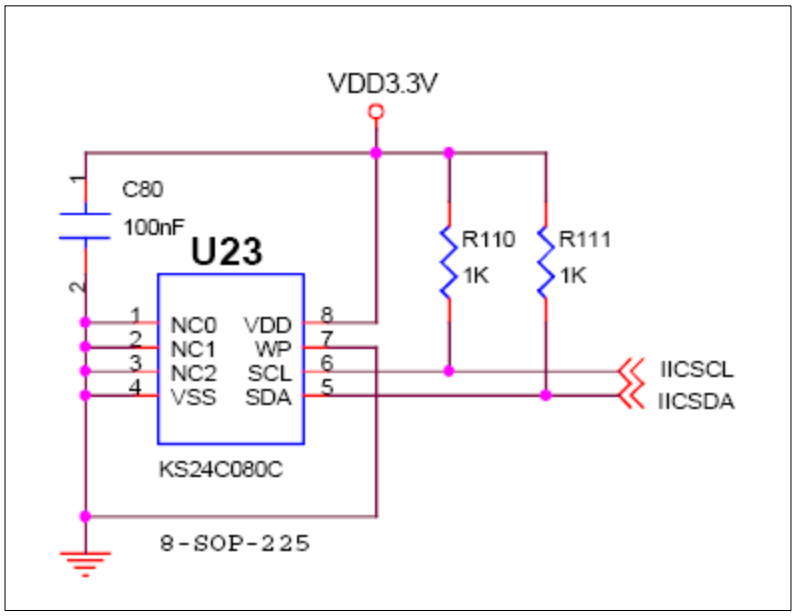


Figure 4-39. IIC Connection Circuit Example

11. IIS and AC97

IIS & AC97 INTERFACE

S3C2440A supports IIS interface and AC97 interface. But, you can't use two interfaces simultaneouly. And the interface pins are also GPIO pins. Consequently, you should pay attention to connecting the pins with outside ones.

When Using As general GPIO

The pins are basically 0,1,2,3 and 4 input pins of GPIO E port. You can use these pins by simply connecting these pins with external LEDs or buttons.

When Using As IIS interface

If you want to use these pins for IIS interface, just connect the pins like a diagram below. The IIS codec of this diagram is an arbitrary codec that supports IIS audio interface, and you can select any codec that is appropriate for your application.

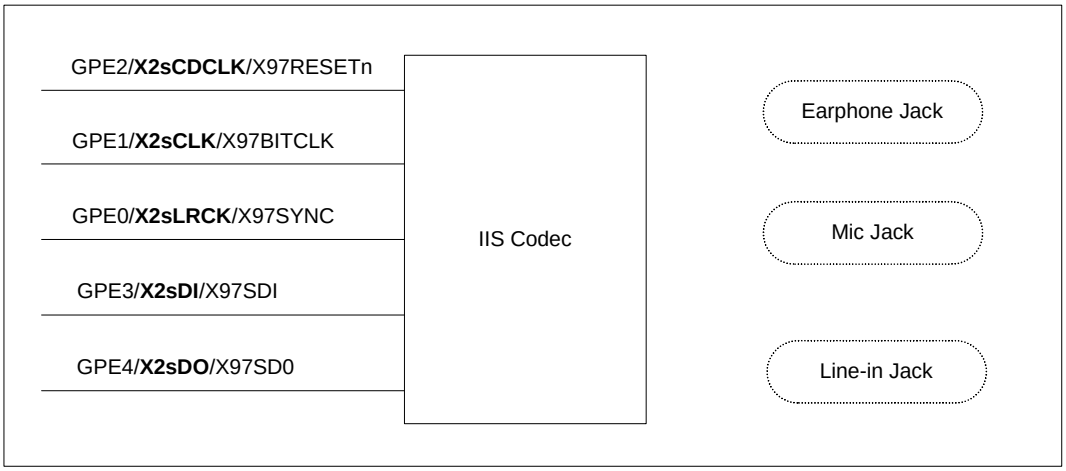


Figure 4-40. IIS Interface Signal

When Using As AC97 interface

In this case, just connect the corresponding pins like a diagram below. The A97 codec of this diagram is an arbitrary codec that supports A97 audio interface, and you can select any codec that is appropriate for your application.

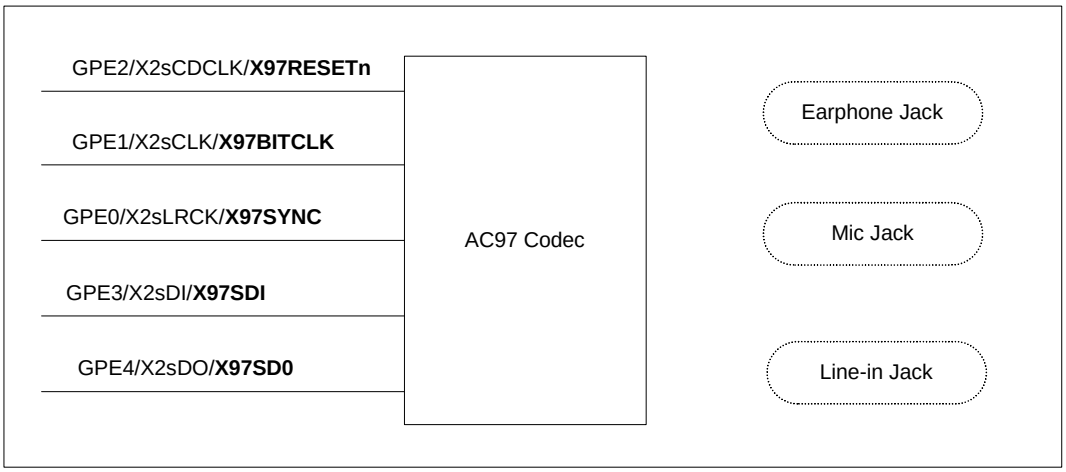


Figure 4-41. AC97 Interface Signal

When Using For IIS or AC97 Selectively

In this case, you should connect the pins with a selective codec by means of resisotrs, and should get rid of resistors that connecting the pins with unselective codec.

In this diagram, for example, if you want to use the pins for IIS codec interface, you should remove resistors, R6 ~R10,

You can also use a simple Mux/Demux chip instead of resistors.

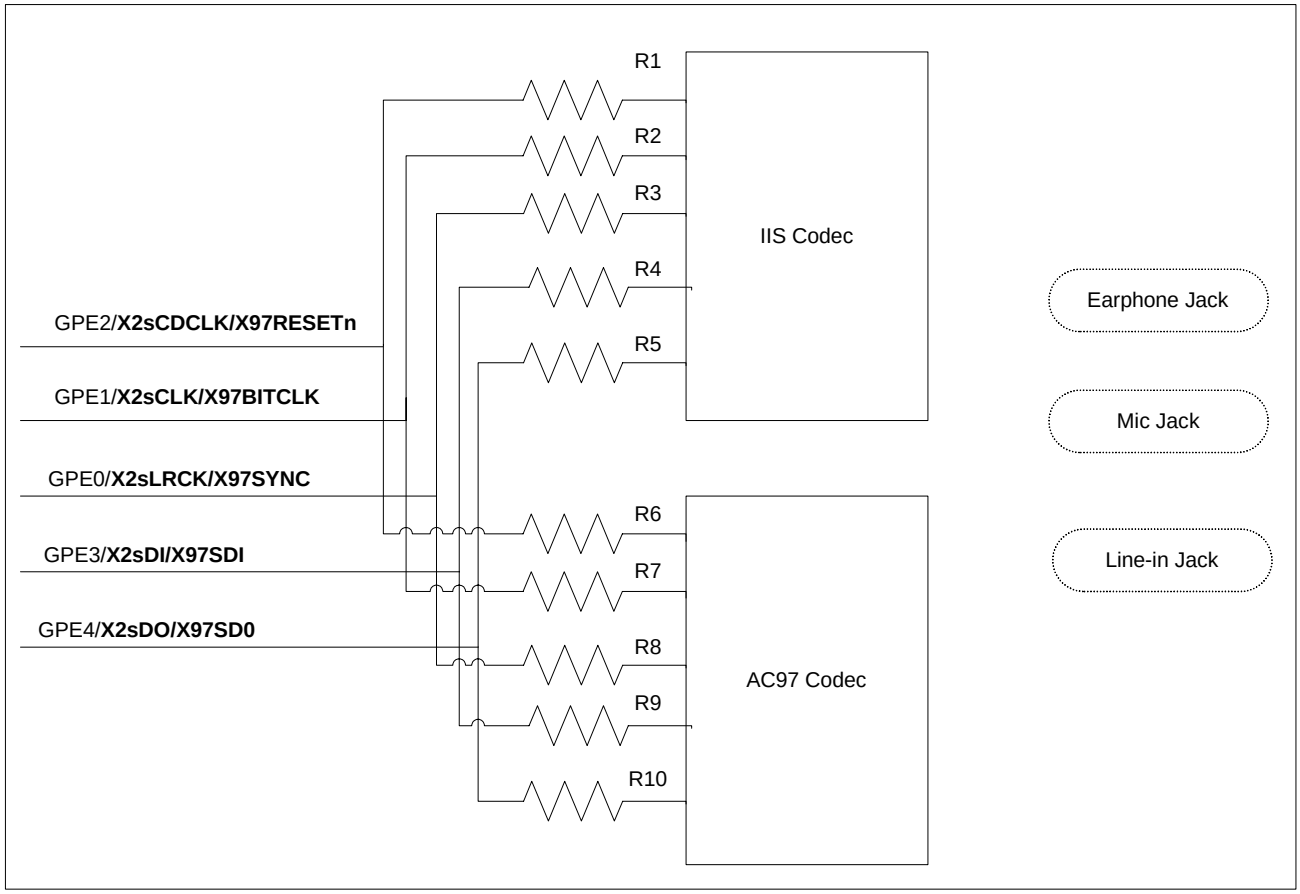


Figure 4-42. IIS or AC97 Interface Example

12. SPI

Description

The S3C2440A Serial Peripheral Interface (SPI) can interface with the serial data transfer. The S3C2440A includes two SPI, each of which has two 8-bit shift registers for transmission and receiving, respectively. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). 8-bit serial data at a frequency is determined by its corresponding control register settings. If you only want to transmit, receive data can be kept dummy. Otherwise, if you only want to receive, you should transmit dummy '1' data.

There are 4 I/O pin signals associated with SPI transfers: SCK (SPICLK0, 1), MISO (SPIMISO0, 1) data line, MOSI (SPIMOSI0,1) data line and active low /SS (nSS0,1) pin (input).

SPI Keyboard Interface

The schematics for a SPI-compatible keyboard encoder connection are shown in Figure 4-43.

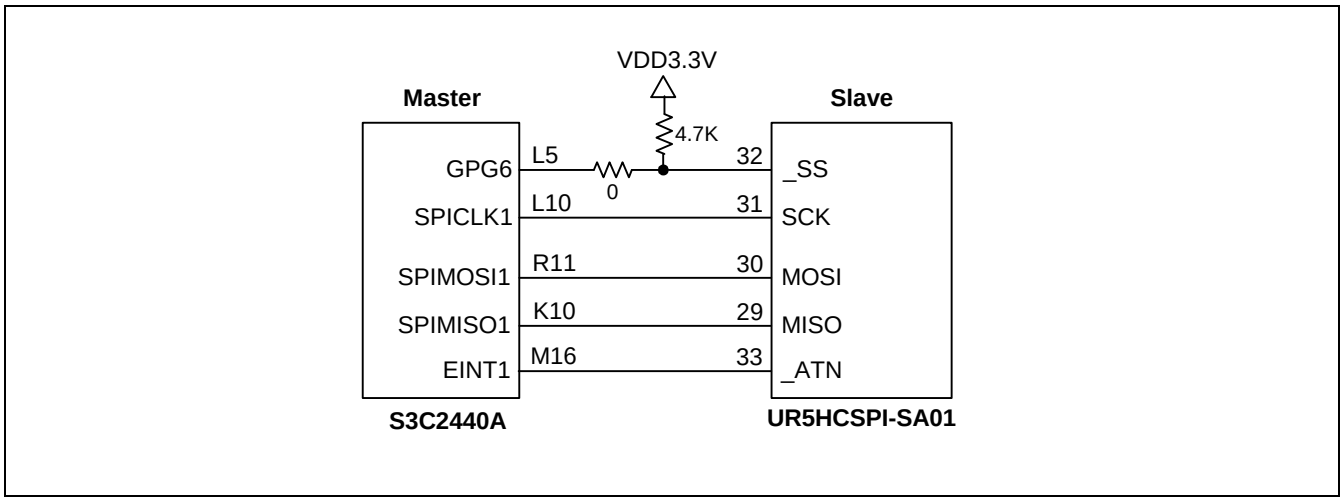


Figure 4-43. Keyboard with SPI Interface

These five signals implement the SPI interface. SPI keyboard encoder device acts as a slave on the SPI bus and S3C2440A as a Master. The _SS (Slave Select) pin must go high between successive characters in an SPI message or a write collision error results. The _ATN pin is asserted low each time the UR5HCSPI-SA01 has a packet ready for delivery.

When using SPI Master connected from GPIO pin of S3C2440A to SPI Chip Select pin, and when Slave connected to nSS pin.

The S3C2440A L5 pin connection 0 ohm resister is series protection resister. So, The resister value is used the right value resister in accordance with application.

13. CAMERA INTERFACE

DESCRIPTION

CAMIF (CAMera InterFace) within the S3C2440A consists of 7 parts – pattern mux, capturing unit, preview scaler, codec scaler, preview DMA, codec DMA, and SFR. The CAMIF supports ITU-R BT.601/656 YCbCr 8-bit standard. Maximum input size is 4096x4096 pixels (2048x2048 pixels for scaling) and two scalers exist. Preview scaler is dedicated to generate smaller size image like PIP (Picture In Picture) and codec scaler is dedicated to generate codec useful image like plane type YCbCr 4:2:0 or 4:2:2. Two-master DMAs can do mirror and rotate the captured image for mobile environments. These features are very useful in folder type cellular phones and the test pattern generated can be useful in calibration of input sync signals as CAMHREF, CAMVSYNC. Also, video sync signals and pixel clock polarity can be inverted in the CAMIF side by using register setting.

SIGNAL DESCRIPTION

Table 4-13. Camera Interface Signal Description

Name	I/O	Active	Description
CAMPCLK	I	–	Pixel clock, driven by the camera processor
CAMVSYNC	I	H/L	Frame sync, driven by the camera processor
CAMHREF	I	H/L	Horizontal sync, driven by the camera processor
CAMDATA [7:0]	I	–	Pixel data driven by the camera processor
CAMCLKOUT	O	–	Master clock to the camera processor
CAMRESET	O	H/L	Software reset or power down to the camera processor

NOTE: I/O direction is on the AP side. I: input, O: output

SCHEMATICS

The S3C2440 Camera Interface signal level is 3.3V. So if you use other signal level camera, you must translate the signal level using the Voltage Translator. (Refer to Figure 4-44)

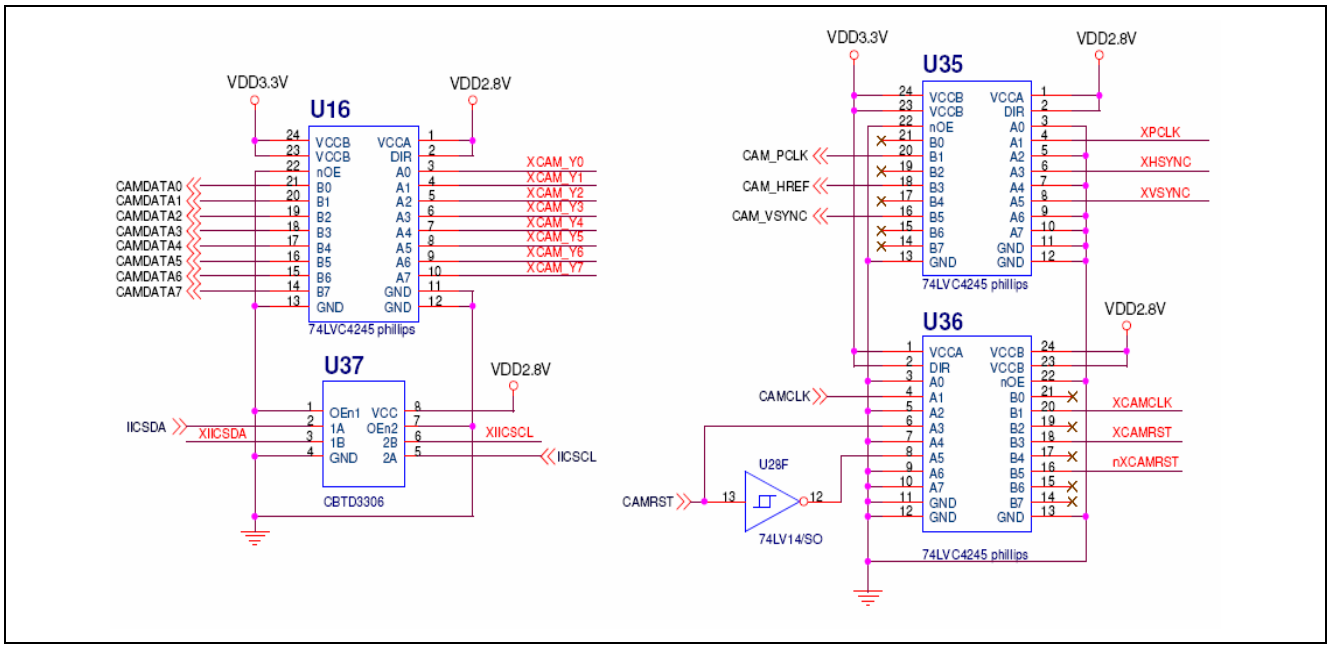


Figure 4-44. Camera Interface with Voltage Translation Example

The examples of S3C2440 Camera Interface are following.

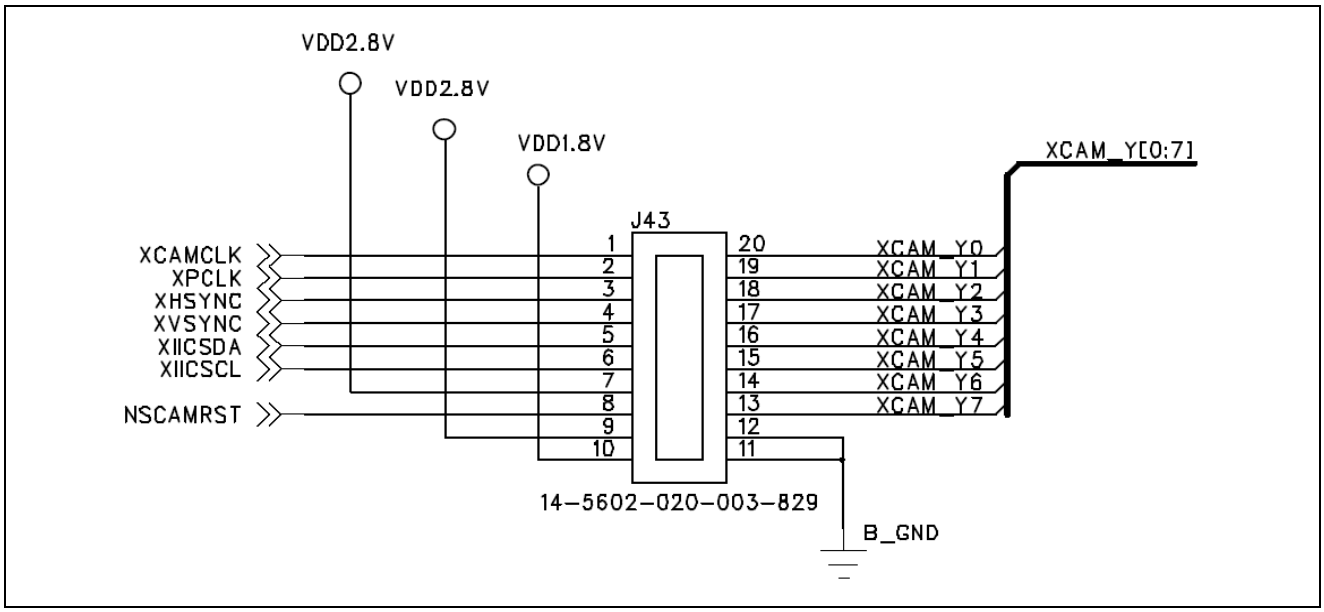


Figure 4-45. Camera Module: S5X3A1 V4220

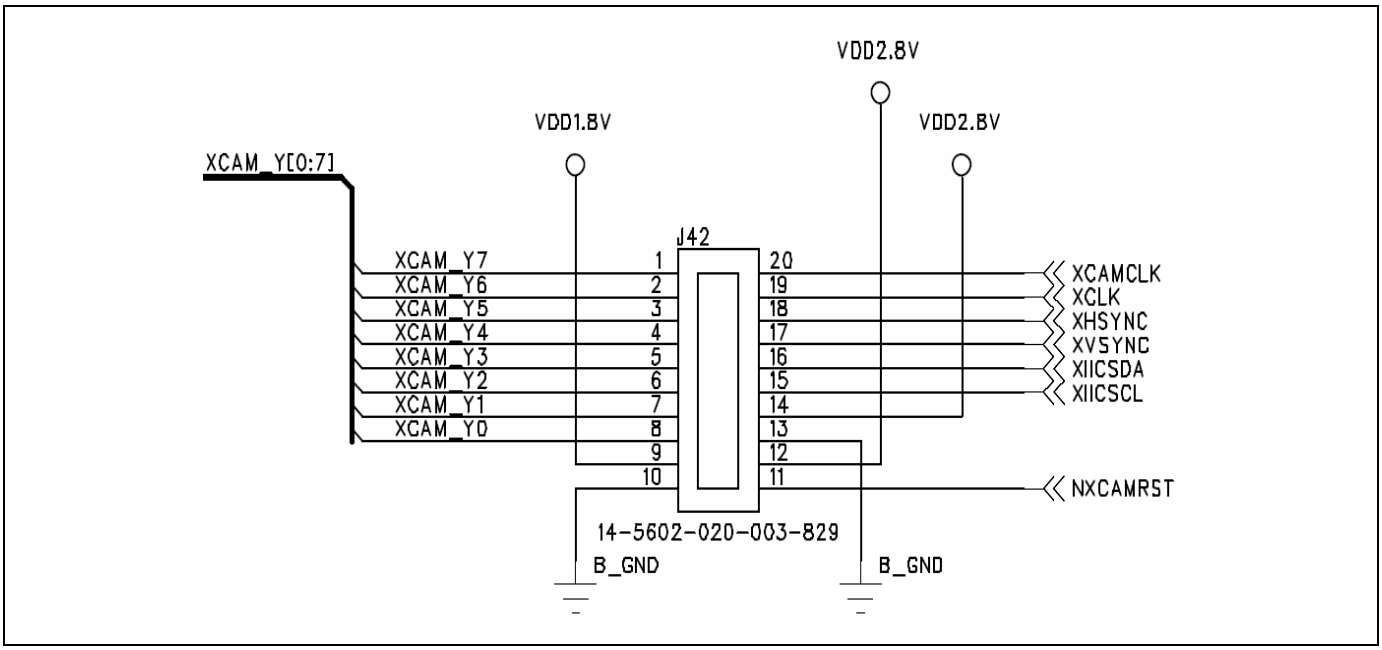


Figure 4-46. Camera Module: S5X532 STD-18

If not use Camera Interface, leave all pin as no connect.

14. JTAG / DEBUG PORT

Description

The S3C2440A has an Embedded ICE logic that provides debug solution from ARM. Embedded ICE logic is accessed through the Test Access Port (TAP) controller on the S3C2440A using the JTAG interface.

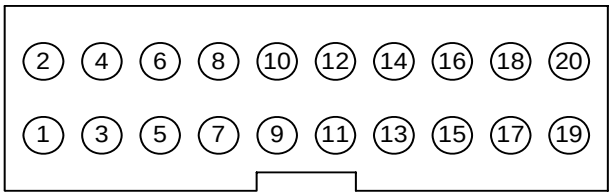
JTAG is testable via the IEEE 1149.1. Many use JTAG to control the address/data bus for Flash programming. JTAG is also a hardware debug port.

Schematics

Usually, the interface connector is a 20-way box header, and this plug is connected to the Embedded ICE logic interface module using 20-way IDC socket.

The JTAG port signals, nTRST, TDI, TMS and TCK have to be connected to pulled-up register (10K ohm) externally.

The pin configuration and a sample design are described in Figure 4-47 and Figure 4-48, respectively.



Pin	Name	Function
1	VTref	System Power
2	Vsupply	System Power
3	nTRST	Test reset, active low (connected pull-up reg.)
5	TDI	Test data in (connected pull-up reg.)
7	TMS	Test mode select (connected pull-up reg.)
9	TCK	Test clock (connected pull-up reg.)
11	RTCK	Return test clock (connected pull-down reg.)
13	TDO	Test data out
15	nSRST	Connected to nRESET and nTRST through 470 ohm resister
17	DBGRQ	NC
19	DBGACK	NC
4, 6, 8, 10, 12, 14, 16, 18, 20	GND	System Ground

Figure 4-47. MULTI-ICE Interface of JTAG Connector

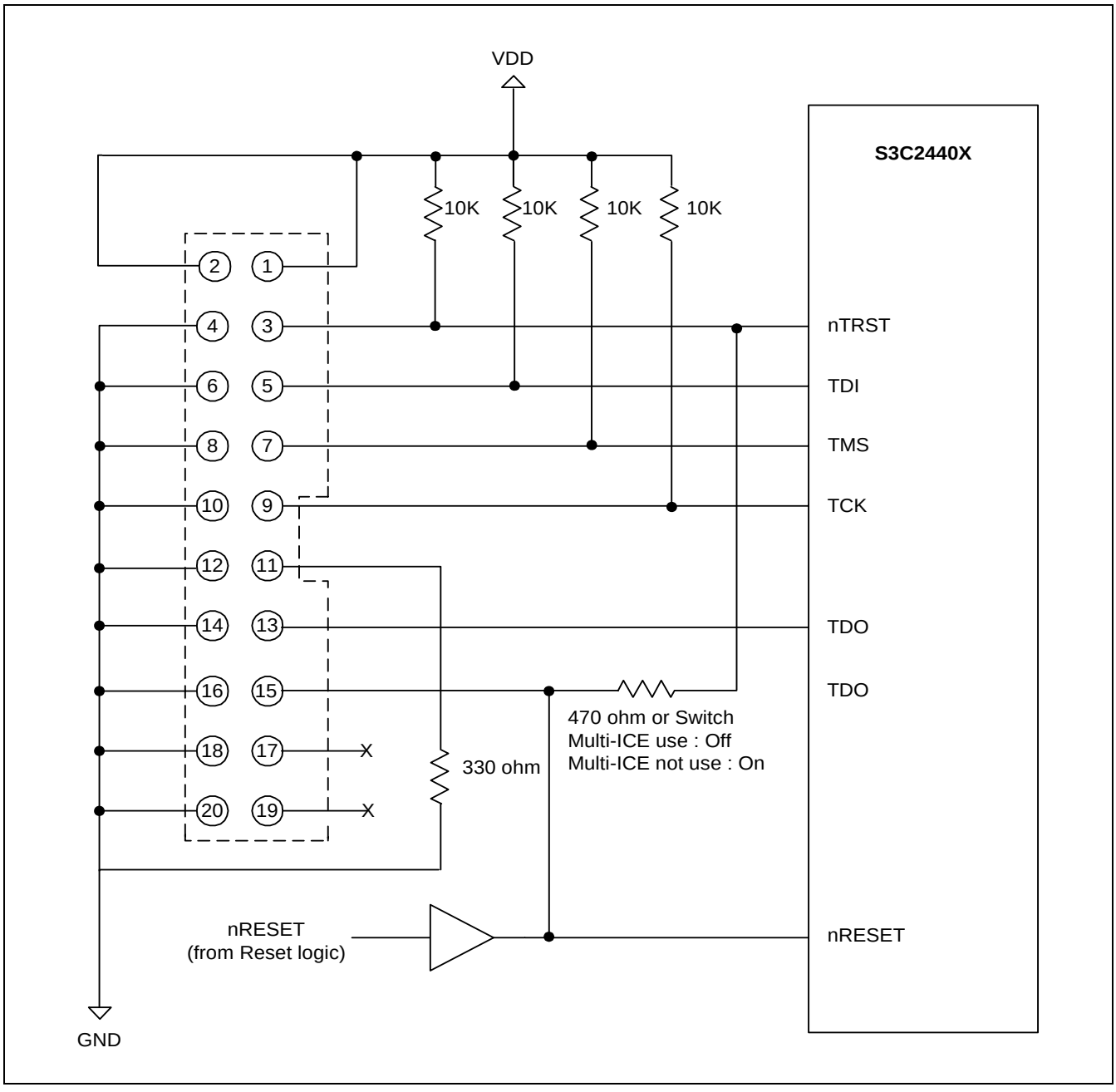


Figure 4-48. MULTI-ICE Interface Design Example

nTRST must be asserted during power-on. Use an external pull-up resistor (10Kohm) to VDDOP on nTRST to prevent spurious resets of the JTAG port when disconnected. Connect 470ohm series resistors to nRESET.

Do not connect pins 17 and 19.

15. HDD

HDD APPLICATION USING TRUE-IDE (PIO MODE) INTERFACE

The HDD can be adapted to the S3C2440A just add one de-mux between S3C2440A bus and CF connector.

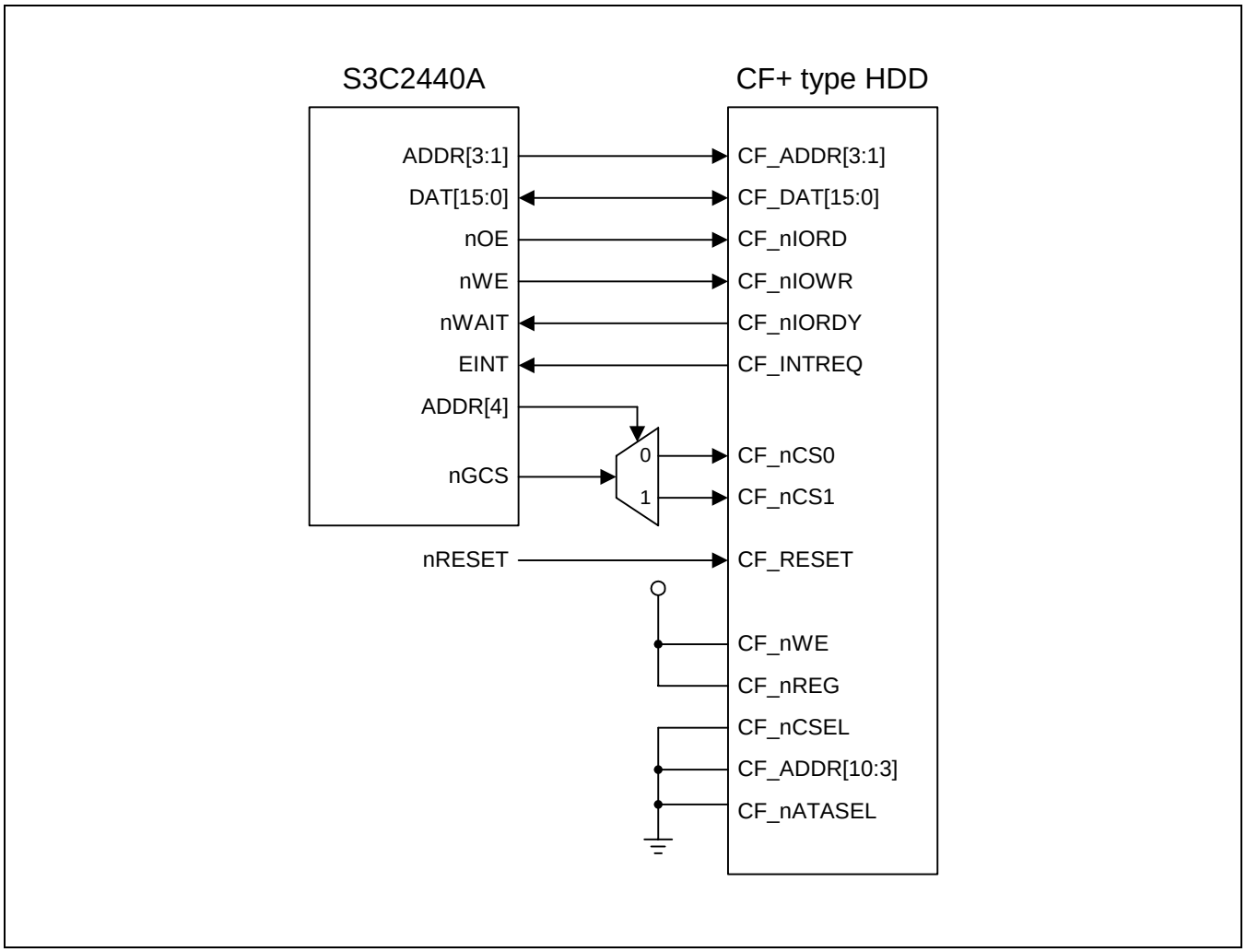


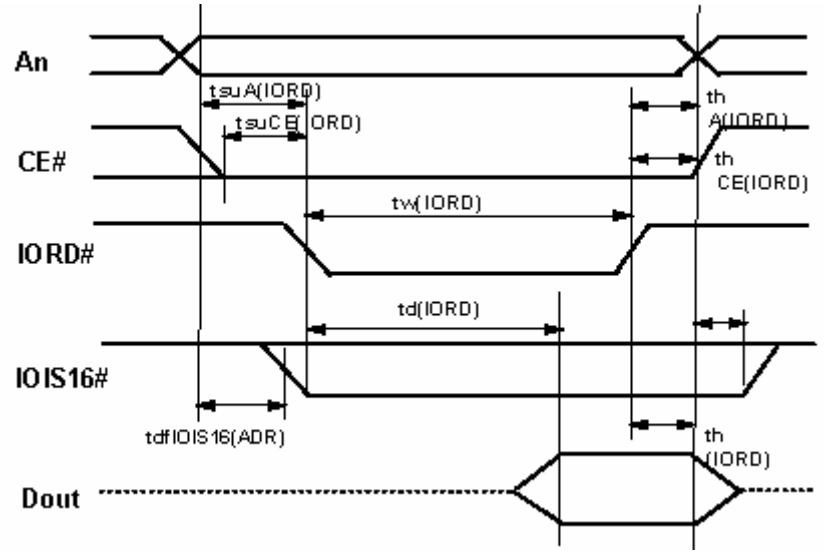
Figure 4-49. CF+ type HDD connection with S3C2440A

TIMING SPECIFICATION

The following table is the HITACHI microdrive timing specification, for examples.

Table 4-14. The timing specification of HITACHI microdrive

Symbol	Item	Minimum (ns)	Maximum (ns)
td (IORD)	Data delay after IORD		100
th (IORD)	Data hold following IORD	0	
tw (IORD)	IORD width time	165	
tsu A (IORD)	Address setup before IORD	70	
th A (IORD)	Address hold following IORD	20	
tsu CE (IORD)	CE setup before IORD	5	
th CE (IORD)	CE hold following IORD	20	



NOTE: IOIS16# is not used

Figure 4-50. PIO mode timing

Table 4-15. Comparison S3C2440A and HITACHI microdirve

S3C2440A	HDD
Tcos	tsu A (IORD)
Tacc	tw (IORD)
Tcoh	th CE (IORD)

NOTES

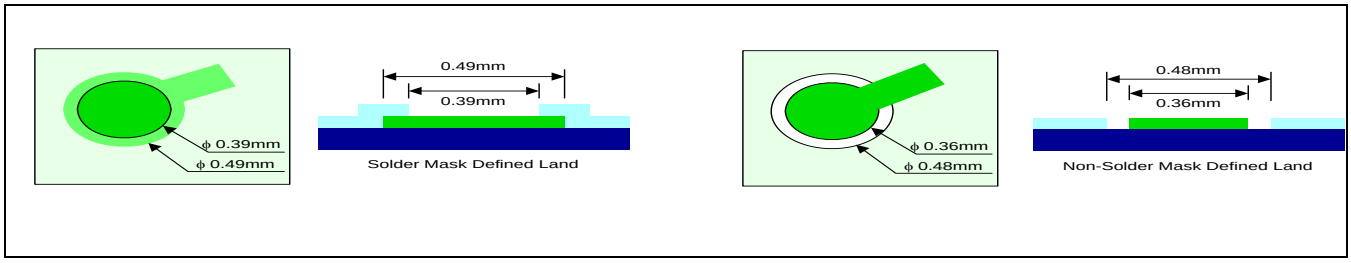
5 ROUTING GUIDES

1. LAND SIZE

It is of great importance to properly design the PCB land pad of FBGA package in terms of productivity of mass-produced board. It is better to match the size of PCB land pad with that of FBGA package. There are two methods for forming the land in PCB.

One is the solder mask defined method: The land copperplate is made bigger than its real size, and the solder mask is made in a desired size to determine the land area. Through this method, it is possible to accurately form the size of land, but relatively routing space is reduced because of large area of copperplate.

The other is the non-solder mask defined method: Land size is made smaller than the solder mask to form the land. The Land size is determined according to etching time generated in the course of producing PCB. This method is a little better for routing because of small area of copperplate, compared to the SMD method.



2. VIA HOLE

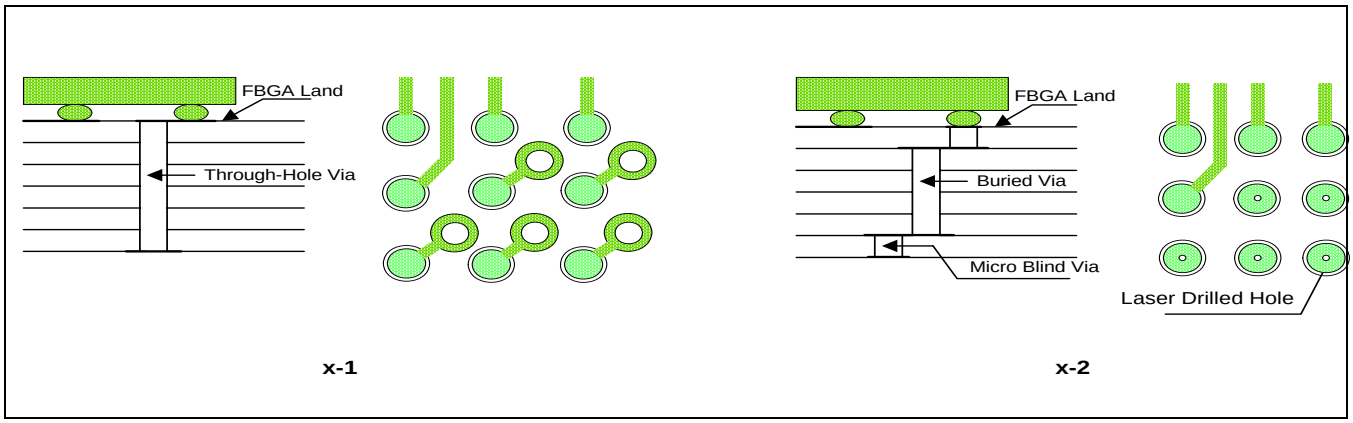
In multi-layered PCB, via is the only method to enable electrical connection of signals between layers. Using via properly facilitates the layout of parts. In case of highly integrated board, via size becomes more important. It is because the small-sized via allows more routing space and the increased insertion rate of parts.

The through-hole via is the most frequently used type of via. However, it is not suitable for PCB routing and component layout since it occupies much area of PCB. In particular, if the through-hole via is used for FBGA package, via hole matrix is formed on the opposite side of PCB, causing restriction in the layout of trace and component. (See Figure x-1)

If you want to facilitate routing on Board and increase the area of insertion for parts, it is more useful to use the following two via techniques.

Micro Blind Via: Possible to minimize the size of via by forming 'via' using very small-sized laser-drill (usually 4um). However, it is possible to connect one side of PCB only to the neighboring layer. When using the FBGA package, the user can get much space for routing, if the combination of PCB land and via is used (See Figure x-2). In addition, it facilitates both-side insertion because via does not appear on the opposite side of PCB.

Buried Via: Via technique allowing connection from inner layer to inner layer of PCB, which is buried under the external surface of PCB. It is also used to interconnect Micro blind vias. (See Figure x-2)



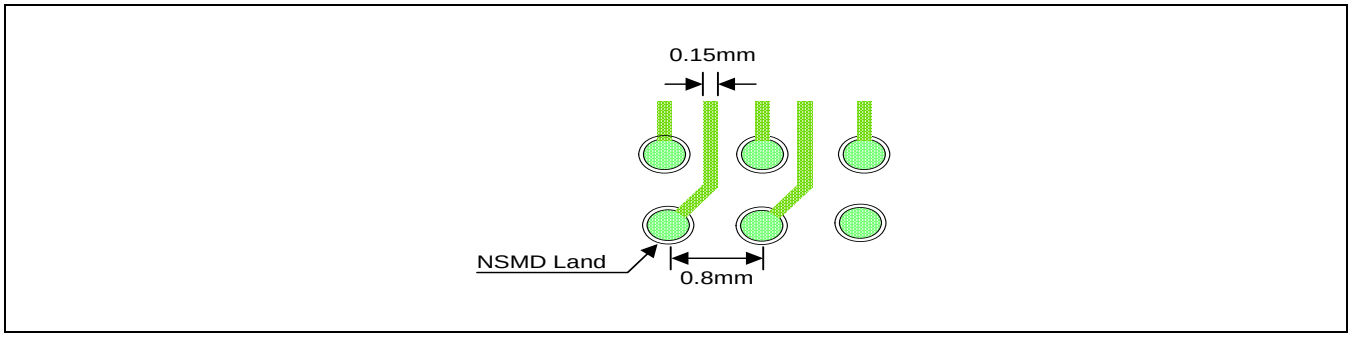
x-1 x-2

3. ROUTING GUIDE

TRACE WIDTH & CLEARANCE

This section describes how to perform routing while properly maintaining the width and interval of trace in FBGA package land.

It is required to extract many signal traces from narrow space and it is not easy for each trace to maintain desired characteristic impedance. Using too narrow trace might cause a problem in PCB manufacture and increase the costs of PCB manufacture. The following figure illustrates the width and interval of trace the user can observe when using the land pad as explained in the previous chapter. In normal case, we recommend the trace width of 0.1 ~ 0.15 mm.



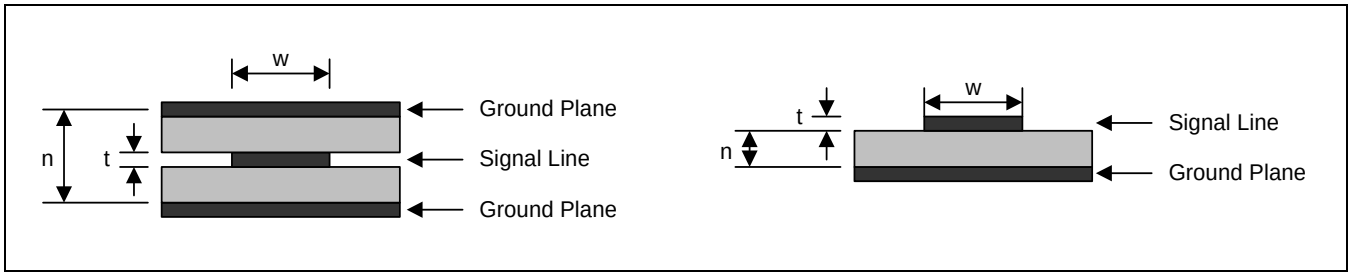
TRANSMISSION LINE IMPEDANCE

This section describes two-transmission line impedance's that can be implemented on the PCB.

Strip line: The signal line is inserted between upper and lower layer power planes in order to implement transmission line. It is advantageous in that clean signals can be transmitted because the power plane has shield effects on both sides, but it must pass the via in order to connect to the element.

Microstrip line: The signal line is placed on the outer layer and ground plane is placed at the next neighboring layer. This is easier to implement than the Strip line.

The following example illustrates characteristic impedance of the two transmission lines.



Transmission line capacitance, Inductance, Z0 and TPD can be calculated with PCB size and material dielectric constant.

For Stripline

$$Z_0 = \frac{60}{\sqrt{\varepsilon_R}} \ln \frac{4h}{0.67\pi w\,(0.8 + \frac{t}{w})}\ \Omega$$

$$t_{PD} = 1.017\sqrt{\varepsilon_R}\ ns/ft$$

$$C_0 = 1000\,\frac{t_{PD}}{Z_0}\ pF/ft$$

$$L_0 = Z_0^2 C_0\ pH/ft$$

For Microstrip

$$Z_0 = \frac{87}{\sqrt{\varepsilon_R + 1.41}} \ln \frac{5.98h}{0.8w + t}\ \Omega$$

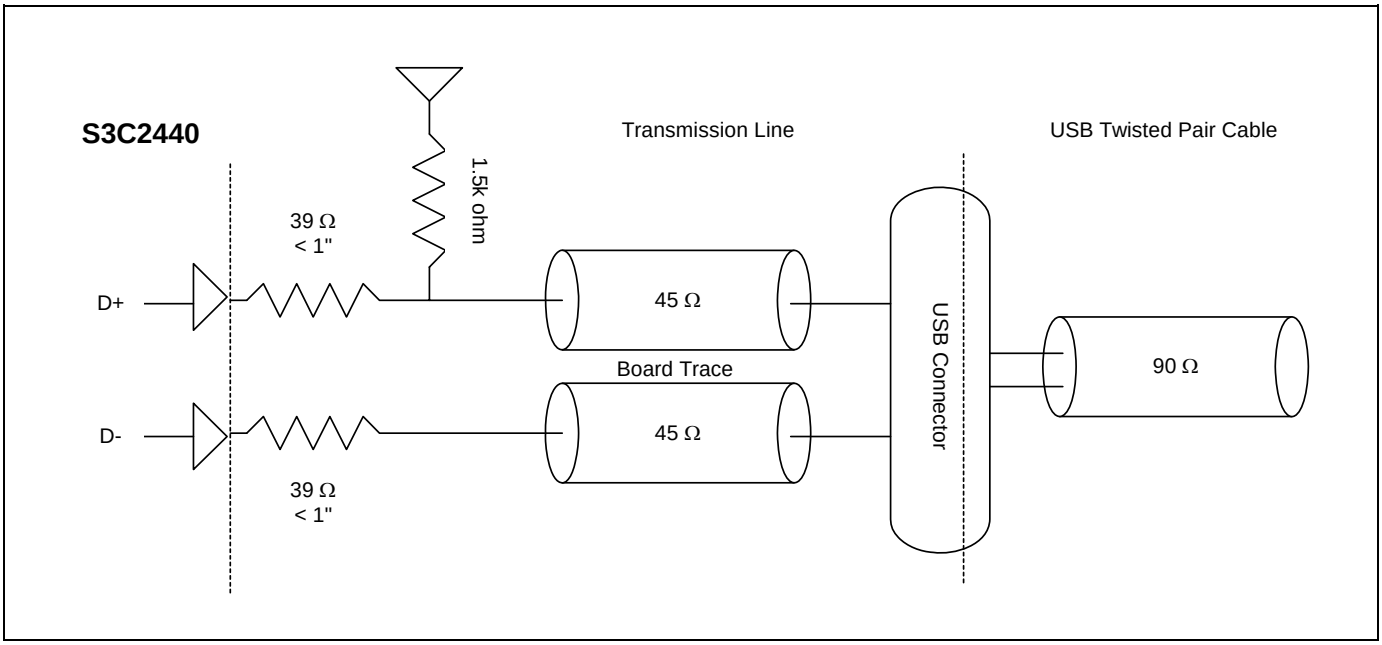
$$t_{PD} = 1.017\,\sqrt{0.457\varepsilon_R + 0.67}\ ns/ft$$

$$C_0 = 1000\,\frac{t_{PD}}{Z_0}\ pF/ft$$

$$L_0 = Z_0^2 C_0\ pH/ft$$

USB SIGNAL ROUTING

The following figure illustrates the recommended USB circuit.



— As USB signal is operated in differential mode and most of chip sets are composed of differential 90-ohm characteristic impedance, it is required to design the circuit with 90 ohm using the impedance calculator.

— As USB signal is bi-directional, it is required to perform parallel termination at the same impedance as characteristic impedance on both sides of Transmitter and Receiver.

— D+/D– Trace must be set to 45-Ohm Impedance and the length of Trace must be equal.

— To prevent cross-talk, D+/D– neighboring signals must be separated more than 2 times the USB D+/D– signal interval.

— If possible, impedance matching resistor and pull-up resistor must be placed closer to the S3C2440A D+/D– pin.

GUIDANCE NOTES FOR ROUTING

— All the SDRAM signals (nSCS, nSRAS, nSCAS, DQMn, SCKE, SCLK, ADDR and DATA) have to be similar in length. By our lab test result, this PCB routing method has enhanced the SDRAM I/O voltage margin up to 2.5V.

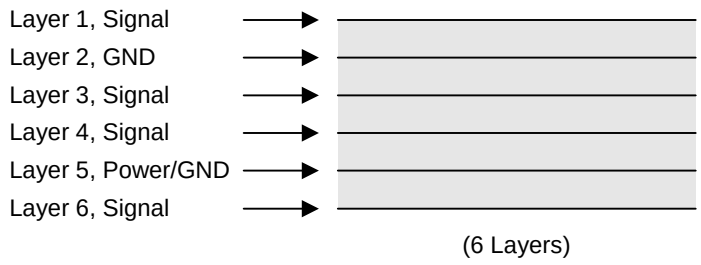
— SCLK0, SCLK1 are exactly the same signals. There are only two 16-bit SDRAM for 32-bit configuration. It is recommend using all SCLKn signals. (For example, SCLK0 for one SDRAM, SCLK1 for the other SDRAM)

— Power signal (GND, 1.2V, 3.3V) must be reinforced as soon as possible. Also, the bypass capacitor has to be nearest to the power pads.

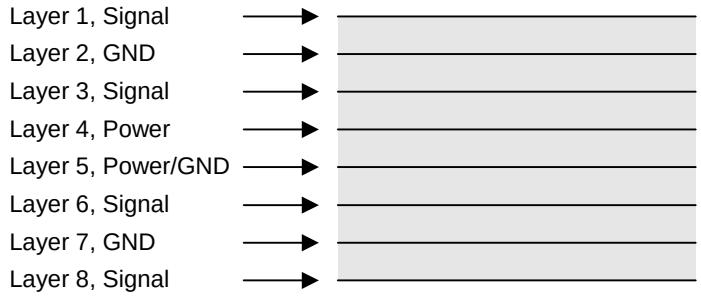
— All the memory signals are simulated at 35pF load. So, all capacitance including the board parasitic must be smaller than 35pF. The parasitic capacitance of the S3C2440 is typically 5pF.

4. LAYER STACK-UP

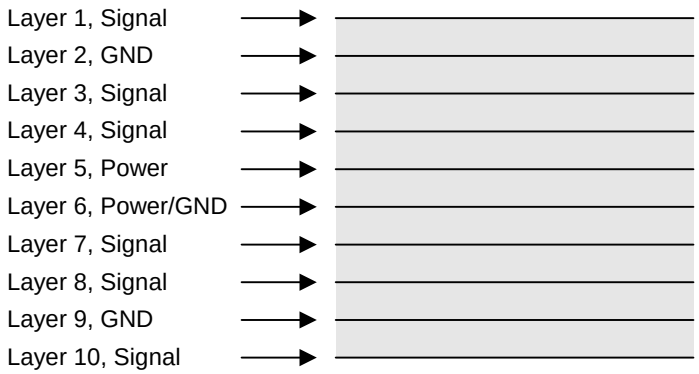
To easily implement the impedance line, the PWR or GND plane must be placed in the layer adjacent to the signal line. The following examples illustrate the proper use of layers.



(6 Layers)



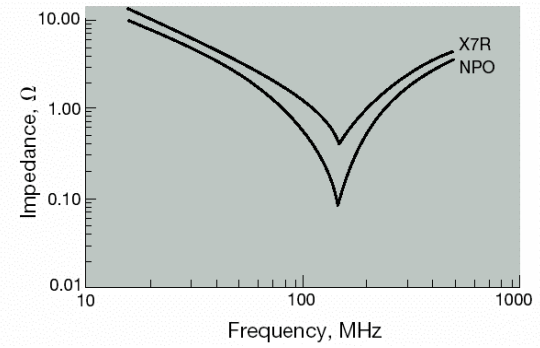
(8 Layers)



(10 Layers)

5. DECOUPLING CAP AND VIA HOLE LAYOUT

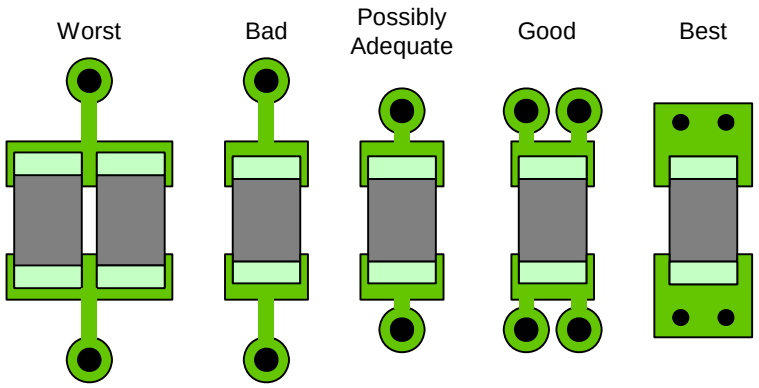
The decoupling capacitor of sufficient capacity must be placed in the high frequency switching device, for the supply of necessary power in the shortest distance. If dcap lacks capacity or supplied path impedance is too high, switching noise is generated and it becomes the source of radiation. Dcap must use a proper capacitor type according to the frequency. Since Dcap impedance is x= sqrt (r2+…) and parasitic inductance value can be dominant according to the frequency, be sure to use it in consideration of frequency bandwidth that acts as capacitor.



F = 1/(2×pi×sqrt (LC))

The Dcap must have enough capacity to supply power during the signal transition.

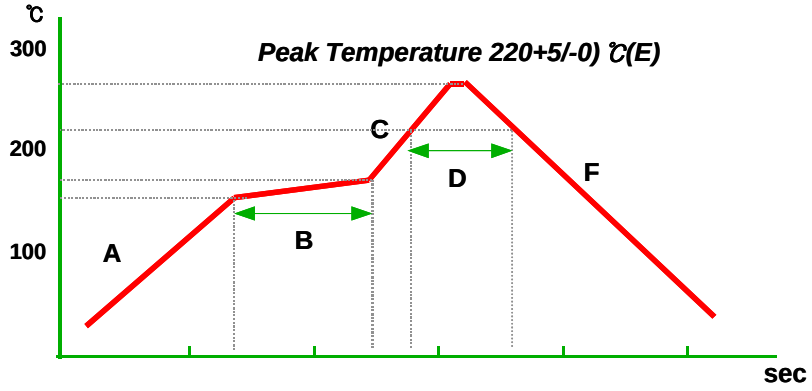
If possible, the decoupling capacitor must be basically placed closer to the power pin of a desired device. When using PCB pad, in addition, do not connect more than 2 decoupling capacitors to one via. The PWR/GND read trace used for decoupling capacitor installation must be routed short, if possible.



6. REFLOW PROFILE

IR Re-flow profile and Moisture Absorption condition for BGA package (leaded)

❖ **IR reflow Profile**



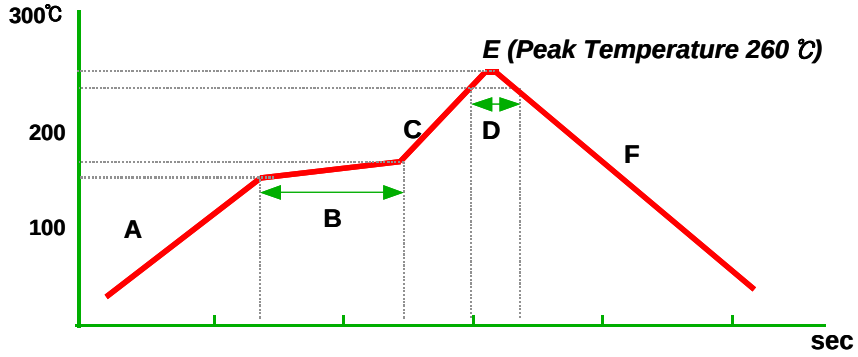
IR re-flow profile for Pre-conditioning						
Peak Temp.	Heat-up(A)	Pre-heat(B)	Heat-up(C)	Maintain(D)	Re-flow peak(E)	Cooling down(F)
Max. 225'C	3'C/sec below	140~160'C 60~120sec	3'C/sec below	60~150sec (Over 183'C)	Max. 220(+5/-0)'C 10sec +/-3sec	6'C/sec

IR Re-flow profile and Moisture Absorption condition for BGA package (Pb free)

❖ **IR sequence : Bake - Absorption - IR 3 times**

❖ **Moisture Absorption condition : 30'C/60%RH, 192hrs**

❖ **IR reflow Profile**



IR re-flow profile for Pre-conditioning						
Peak Temp.	Heat-up(A)	Pre-heat(B)	Heat-up(C)	Maintain(D)	Re-flow peak(E)	Cooling down(F)
Max. 260'C	3'C/sec Max.	160~190'C 90 ± 30sec	3'C/sec Max.	255'C+5, 0'C 10 ±3sec	Max. 260'C	6'C/sec Max.

7. EMI REDUCTION

— Close coupling between conductors of a pair not only reduces EMI, but it helps to ensure noise coupled onto the conductors will do so equally as common mode noise which will then be rejected by the receiver.

— Imbalance minimization is the other important factor in reducing EMI.

— The basic rule to follow is: if any discontinuity must be introduced in proximity to differential lines, it should be introduced equally to both members of the pair.

6 GPIO CONFIGURATIONS FOR SLEEP MODE

1. PIN CONFIGURATION TABLE IN SLEEP MODE

Pin Condition			Guide of Pin Configuration
Unused GPIO Pin		Which are configured as input	Pull-up enable
		Which are configured as output	Pull-up disable and output low
Input pin, which doesn't have internal pull-up control.		If external device doesn't always drive pin's level.	Pull-up enable by external pull-up resistor
Input pin, which is connected to external device		If external device's power is off.	Pull-up disable and external Pull-down
		If external device drives the level.	Pull-up disable
Output pin, which is connected to external device		If external device's power is off.	Output low
		If external device's power is on.	High or low (It depends on External device's status)
Data Bus	If memory power is off		Pull-up disable and external Pull-dwon
	If memory power is on	And external buffer does exist	If buffer can hold bus level, pull-up disables.
		And no external buffer	Pull-up enable

NOTE:
1. ADC should be set to Standby mode.
2. USB pads should be Suspend mode.

* This table is just for informational use only. User should consider his own board condition and application.

NOTES

7 PACKAGE

1. PIN ASSIGNMENTS

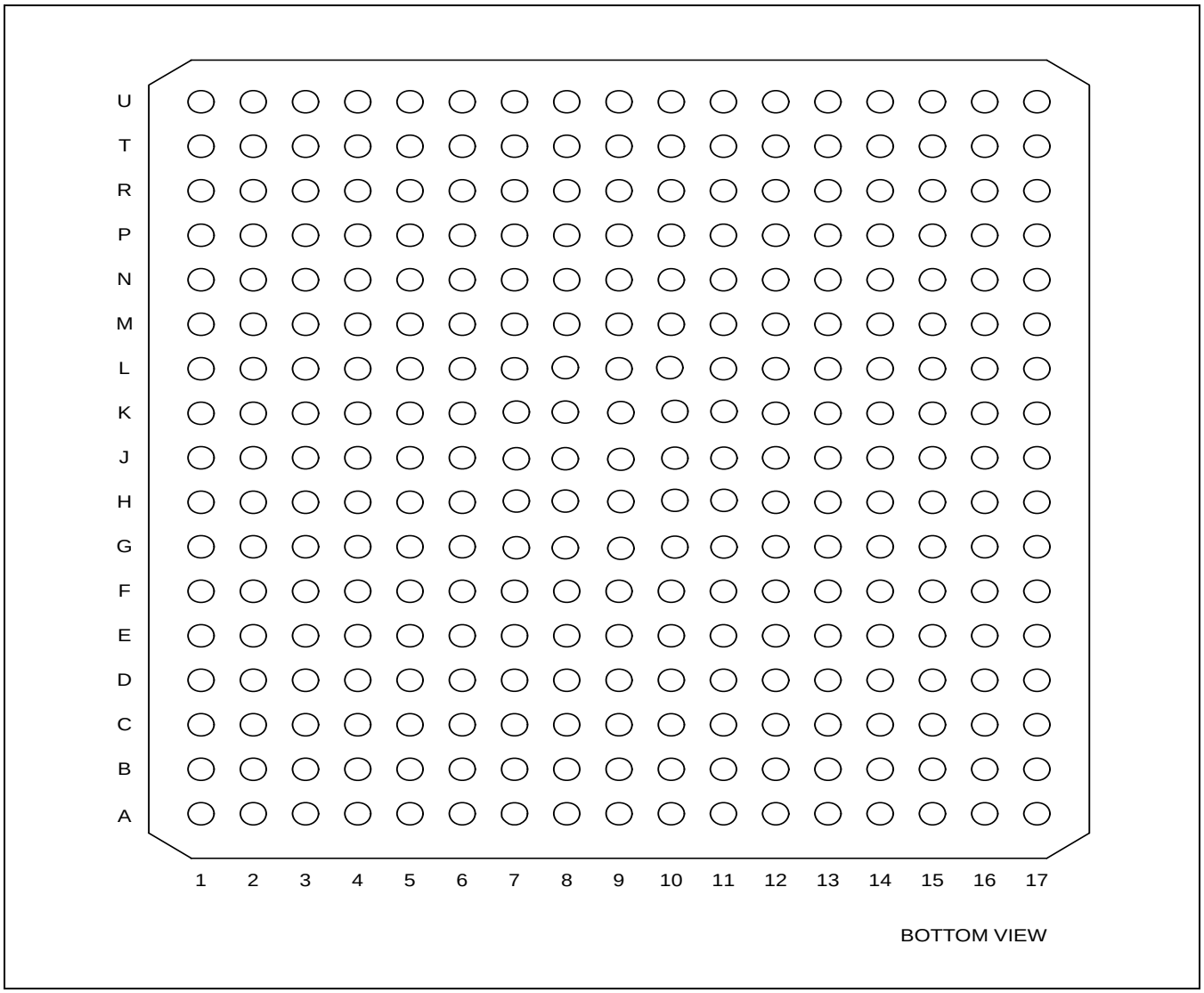


Figure 7-1. S3C2440A Pin Assignments (289-FBGA)

Table 7-1. 289-Pin FBGA Pin Assignments – Pin Number Order (Sheet 1 of 3)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A1	VDDi	C1	VDDMOP	E1	nFRE/GPA20
A2	SCKE	C2	nGCS5/GPA16	E2	VSSMOP
A3	VSSi	C3	nGCS2/GPA13	E3	nGCS7
A4	VSSi	C4	nGCS3/GPA14	E4	nWAIT
A5	VSSMOP	C5	nOE	E5	nBE3
A6	VDDi	C6	nSRAS	E6	nWE
A7	VSSMOP	C7	ADDR4	E7	ADDR1
A8	ADDR10	C8	ADDR11	E8	ADDR6
A9	VDDMOP	C9	ADDR15	E9	ADDR14
A10	VDDi	C10	ADDR21/GPA6	E10	ADDR23/GPA8
A11	VSSMOP	C11	ADDR24/GPA9	E11	DATA2
A12	VSSi	C12	DATA1	E12	DATA20
A13	DATA3	C13	DATA6	E13	DATA19
A14	DATA7	C14	DATA11	E14	DATA18
A15	VSSMOP	C15	DATA13	E15	DATA17
A16	VDDi	C16	DATA16	E16	DATA21
A17	DATA10	C17	VSSi	E17	DATA24
B1	VSSMOP	D1	ALE/GPA18	F1	VDDi
B2	nGCS1/GPA12	D2	nGCS6	F2	VSSi
B3	SCLK1	D3	nGCS4/GPA15	F3	nFWE/GPA19
B4	SCLK0	D4	nBE0	F4	nFCE/GPA22
B5	nBE1	D5	nBE2	F5	CLE/GPA17
B6	VDDMOP	D6	nSCAS	F6	nGCS0
B7	ADDR2	D7	ADDR7	F7	ADDR0/GPA0
B8	ADDR9	D8	ADDR5	F8	ADDR3
B9	ADDR12	D9	ADDR16/GPA1	F9	ADDR18/GPA3
B10	VSSi	D10	ADDR20/GPA5	F10	DATA4
B11	VDDi	D11	ADDR26/GPA11	F11	DATA5
B12	VDDMOP	D12	DATA0	F12	DATA27
B13	VSSMOP	D13	DATA8	F13	DATA31
B14	VDDMOP	D14	DATA14	F14	DATA26
B15	DATA9	D15	DATA12	F15	DATA22
B16	VDDMOP	D16	VSSMOP	F16	VDDi
B17	DATA15	D17	VSSMOP	F17	VDDMOP

Table 7-1. 289-Pin FBGA Pin Assignments – Pin Number Order (Sheet 2 of 3)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
G1	VSSOP	J1	VDDOP	L1	LEND/GPC0
G2	CAMHREF/GPJ10	J2	VDDiarm	L2	VDDiarm
G3	CAMDATA1/GPJ1	J3	CAMCLKOUT/GPJ11	L3	nXDACK0/GPB9
G4	VDDalive	J4	CAMRESET/GPJ12	L4	VCLK/GPC1
G5	CAMPCLK/GPJ8	J5	TOUT1/GPB1	L5	nXBREQ/GPB6
G6	FRnB	J6	TOUT0/GPB0	L6	VD1/GPC9
G7	CAMVSYNC/GPJ9	J7	TOUT2/GPB2	L7	VFRAME/GPC3
G8	ADDR8	J8	CAMDATA6/GPJ6	L8	I2SSDI/nSS0/GPE3
G9	ADDR17/GPA2	J9	SDDAT3/GPE10	L9	SPICLK0/GPE13
G10	ADDR25/GPA10	J10	EINT10/nSS0/GPG2	L10	EINT15/SPICLK1/GPG7
G11	DATA28	J11	TXD2/nRTS1/GPH6	L11	EINT22/GPG14
G12	DATA25	J12	PWREN	L12	Xtortc
G13	DATA23	J13	TCK	L13	EINT2/GPF2
G14	XTIpll	J14	TMS	L14	EINT5/GPF5
G15	XTOpll	J15	RXD2/nCTS1/GPH7	L15	EINT6/GPF6
G16	DATA29	J16	TDO	L16	EINT7/GPF7
G17	VSSi	J17	VDDalive	L17	nRTS0/GPH1
H1	VSSiarm	K1	VSSiarm	M1	VLINE/GPC2
H2	CAMDATA7/GPJ7	K2	nXBACK/GPB5	M2	LCD_LPCREV/GPC6
H3	CAMDATA4/GPJ4	K3	TOUT3/GPB3	M3	LCD_LPCOE/GPC5
H4	CAMDATA3/GPJ3	K4	TCLK0/GPB4	M4	VM/GPC4
H5	CAMDATA2/GPJ2	K5	nXDREQ1/GPB8	M5	VD9/GPD1
H6	CAMDATA0/GPJ0	K6	nXDREQ0/GPB10	M6	VD6/GPC14
H7	CAMDATA5/GPJ5	K7	nXDACK1/GPB7	M7	VD16/SPIMISO1/GPD8
H8	ADDR13	K8	SDCMD/GPE6	M8	SDDAT1/GPE8
H9	ADDR19/GPA4	K9	SPIMISO0/GPE11	M9	IICSDA/GPE15
H10	ADDR22/GPA7	K10	EINT13/SPIMISO1/GPG5	M10	EINT20/GPG12
H11	VSSOP1	K11	nCTS0/GPH0	M11	EINT17/nRTS1/GPG9
H12	EXTCLK	K12	VDDOP	M12	VSSA_UPLL
H13	DATA30	K13	TXD0/GPH2	M13	VDDA_UPLL
H14	nBATT_FLT	K14	RXD0/GPH3	M14	Xtirtc
H15	nTRST	K15	UARTCLK/GPH8	M15	EINT3/GPF3
H16	nRESET	K16	TXD1/GPH4	M16	EINT1/GPF1
H17	TDI	K17	RXD1/GPH5	M17	EINT4/GPF4

Table 7-1. 289-Pin FBGA Pin Assignments – Pin Number Order (Sheet 3 of 3)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
N1	VSSOP	R1	VD3/GPC11	U1	VDDiarm
N2	VD0/GPC8	R2	VD8/GPD0	U2	VDDiarm
N3	VD4/GPC12	R3	VD11/GPD3	U3	VSSOP
N4	VD2/GPC10	R4	VD13/GPD5	U4	VSSiarm
N5	VD10/GPD2	R5	VD18/SPICLK1/GPD10	U5	VD23/nSS0/GPD15
N6	VD15/GPD7	R6	VD21 /GPD13	U6	I2SSDO/I2SSDI/GPE4
N7	VD22/nSS1/GPD14	R7	I2SSCLK/GPE1	U7	VSSiarm
N8	SDCLK/GPE5	R8	SDDAT0/GPE7	U8	IICSCL/GPE14
N9	EINT8/GPG0	R9	CLKOUT0/GPH9	U9	VSSOP
N10	EINT18/nCTS1/GPG10	R10	EINT11/nSS1/GPG3	U10	VSSiarm
N11	DP0	R11	EINT14/SPIMOSI1/GPG6	U11	VDDi
N12	DN1/PDN0	R12	NCON	U12	EINT19/TCLK1/GPG11
N13	nRSTOUT/GPA21	R13	OM1	U13	EINT23/GPG15
N14	MPLLCAP	R14	AIN0	U14	DP1/PDP0
N15	VDD_RTC	R15	AIN2	U15	VSSOP
N16	VDDA_MPLL	R16	AIN6	U16	Vref
N17	EINT0/GPF0	R17	VSSA_MPLL	U17	AIN1
P1	LCD_LPCREVB/GPC7	T1	VSSiarm		
P2	VD5/GPC13	T2	VSSiarm		
P3	VD7/GPC15	T3	VDDOP		
P4	VD12/GPD4	T4	VD17/SPIMOSI1/GPD9		
P5	VD14/GPD6	T5	VD19/GPD11		
P6	VD20/GPD12	T6	VDDiarm		
P7	I2SLRCK/GPE0	T7	CDCLK/GPE2		
P8	SDDAT2/GPE9	T8	VDDiarm		
P9	SPIMOSI0/GPE12	T9	EINT9/GPG1		
P10	CLKOUT1/GPH10	T10	EINT16/GPG8		
P11	EINT12/LCD_PWREN	T11	EINT21/GPG13		
P12	DN0	T12	VDDOP		
P13	OM2	T13	OM3		
P14	VDDA_ADC	T14	VSSA_ADC		
P15	AIN3	T15	OM0		
P16	AIN7	T16	AIN4		
P17	UPLLCAP	T17	AIN5		

Table 7-2. S3C2440A 289-Pin FBGA Pin Assignments (Sheet 1 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
F7	ADDR0/GPA0	ADDR0	Hi-z/–	O(L)/–	O(L)	t10s
E7	ADDR1	ADDR1	Hi-z	O(L)	O(L)	t10s
B7	ADDR2	ADDR2	Hi-z	O(L)	O(L)	t10s
F8	ADDR3	ADDR3	Hi-z	O(L)	O(L)	t10s
C7	ADDR4	ADDR4	Hi-z	O(L)	O(L)	t10s
D8	ADDR5	ADDR5	Hi-z	O(L)	O(L)	t10s
E8	ADDR6	ADDR6	Hi-z	O(L)	O(L)	t10s
D7	ADDR7	ADDR7	Hi-z	O(L)	O(L)	t10s
G8	ADDR8	ADDR8	Hi-z	O(L)	O(L)	t10s
B8	ADDR9	ADDR9	Hi-z	O(L)	O(L)	t10s
A8	ADDR10	ADDR10	Hi-z	O(L)	O(L)	t10s
C8	ADDR11	ADDR11	Hi-z	O(L)	O(L)	t10s
B9	ADDR12	ADDR12	Hi-z	O(L)	O(L)	t10s
H8	ADDR13	ADDR13	Hi-z	O(L)	O(L)	t10s
E9	ADDR14	ADDR14	Hi-z	O(L)	O(L)	t10s
C9	ADDR15	ADDR15	Hi-z	O(L)	O(L)	t10s
D9	ADDR16/GPA1	ADDR16	Hi-z/–	O(L)/–	O(L)	t10s
G9	ADDR17/GPA2	ADDR17	Hi-z/–	O(L)/–	O(L)	t10s
F9	ADDR18/GPA3	ADDR18	Hi-z/–	O(L)/–	O(L)	t10s
H9	ADDR19/GPA4	ADDR19	Hi-z/–	O(L)/–	O(L)	t10s
D10	ADDR20/GPA5	ADDR20	Hi-z/–	O(L)/–	O(L)	t10s
C10	ADDR21/GPA6	ADDR21	Hi-z/–	O(L)/–	O(L)	t10s
H10	ADDR22/GPA7	ADDR22	Hi-z/–	O(L)/–	O(L)	t10s
E10	ADDR23/GPA8	ADDR23	Hi-z/–	O(L)/–	O(L)	t10s
C11	ADDR24/GPA9	ADDR24	Hi-z/–	O(L)/–	O(L)	t10s
G10	ADDR25/GPA10	ADDR25	Hi-z/–	O(L)/–	O(L)	t10s
D11	ADDR26/GPA11	ADDR26	Hi-z/–	O(L)/–	O(L)	t10s
R14	AIN0	AIN0	–	–	AI	r10
U17	AIN1	AIN1	–	–	AI	r10
R15	AIN2	AIN2	–	–	AI	r10
P15	AIN3	AIN3	–	–	AI	r10
T16	YM/AIN4	AIN4	–/–	–/–	AI	r10
T17	YP/AIN5	YP	–/–	–/–	AI	r10
R16	XM/AIN6	AIN6	–/–	–/–	AI	r10

Table 7-2. S3C2440A 289-Pin FBGA Pin Assignments (Sheet 2 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
P16	XP/AIN7	XP	–/–	–/–	AI	r10
H6	CAMDATA0/GPJ0	GPJ0	–/–	Hi-z/–	I	t8
G3	CAMDATA1/GPJ1	GPJ1	–/–	Hi-z/–	I	t8
H5	CAMDATA2/GPJ2	GPJ2	–/–	Hi-z/–	I	t8
H4	CAMDATA3/GPJ3	GPJ3	–/–	Hi-z/–	I	t8
H3	CAMDATA4/GPJ4	GPJ4	–/–	Hi-z/–	I	t8
H7	CAMDATA5/GPJ5	GPJ5	–/–	Hi-z/–	I	t8
J8	CAMDATA6/GPJ6	GPJ6	–/–	Hi-z/–	I	t8
H2	CAMDATA7/GPJ7	GPJ7	–/–	Hi-z/–	I	t8
G5	CAMPCLK/GPJ8	GPJ8	–/–	Hi-z/–	I	t8
G7	CAMVSYNC/GPJ9	GPJ9	–/–	Hi-z/–	I	t8
G2	CAMHREF/GPJ10	GPJ10	–/–	Hi-z/–	I	t8
J3	CAMPCLKOUT/GPJ1	GPJ11	–/–	O(L)/–	I	t8
J4	CAMRESET/GPJ12	GPJ12	–/–	O(L)/–	I	t8
D12	DATA0	DATA0	Hi-z	Hi-z,O(L)	I	b12s
C12	DATA1	DATA1	Hi-z	Hi-z,O(L)	I	b12s
E11	DATA2	DATA2	Hi-z	Hi-z,O(L)	I	b12s
A13	DATA3	DATA3	Hi-z	Hi-z,O(L)	I	b12s
F10	DATA4	DATA4	Hi-z	Hi-z,O(L)	I	b12s
F11	DATA5	DATA5	Hi-z	Hi-z,O(L)	I	b12s
C13	DATA6	DATA6	Hi-z	Hi-z,O(L)	I	b12s
A14	DATA7	DATA7	Hi-z	Hi-z,O(L)	I	b12s
D13	DATA8	DATA8	Hi-z	Hi-z,O(L)	I	b12s
B15	DATA9	DATA9	Hi-z	Hi-z,O(L)	I	b12s
A17	DATA10	DATA10	Hi-z	Hi-z,O(L)	I	b12s
C14	DATA11	DATA11	Hi-z	Hi-z,O(L)	I	b12s
D15	DATA12	DATA12	Hi-z	Hi-z,O(L)	I	b12s
C15	DATA13	DATA13	Hi-z	Hi-z,O(L)	I	b12s
D14	DATA14	DATA14	Hi-z	Hi-z,O(L)	I	b12s
B17	DATA15	DATA15	Hi-z	Hi-z,O(L)	I	b12s
C16	DATA16	DATA16	Hi-z	Hi-z,O(L)	I	b12s
E15	DATA17	DATA17	Hi-z	Hi-z,O(L)	I	b12s
E14	DATA18	DATA18	Hi-z	Hi-z,O(L)	I	b12s

Table 7-2. S3C2440A 289-Pin FBGA Pin Assignments (Sheet 3 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
E13	DATA19	DATA19	Hi-z	Hi-z,O(L)	I	b12s
E12	DATA20	DATA20	Hi-z	Hi-z,O(L)	I	b12s
E16	DATA21	DATA21	Hi-z	Hi-z,O(L)	I	b12s
F15	DATA22	DATA22	Hi-z	Hi-z,O(L)	I	b12s
G13	DATA23	DATA23	Hi-z	Hi-z,O(L)	I	b12s
E17	DATA24	DATA24	Hi-z	Hi-z,O(L)	I	b12s
G12	DATA25	DATA25	Hi-z	Hi-z,O(L)	I	b12s
F14	DATA26	DATA26	Hi-z	Hi-z,O(L)	I	b12s
F12	DATA27	DATA27	Hi-z	Hi-z,O(L)	I	b12s
G11	DATA28	DATA28	Hi-z	Hi-z,O(L)	I	b12s
G16	DATA29	DATA29	Hi-z	Hi-z,O(L)	I	b12s
H13	DATA30	DATA30	Hi-z	Hi-z,O(L)	I	b12s
F13	DATA31	DATA31	Hi-z	Hi-z,O(L)	I	b12s
P12	DN0	DN0	¤Ñ	¤Ñ	AI	us
N11	DP0	DP0	¤Ñ	¤Ñ	AI	us
N12	DN1/PDN0	DN1	–/–	¤Ñ	AI	us
U14	DP1/PDP0	DP1	–/–	¤Ñ	AI	us
N17	EINT0/GPF0	GPF0	–/–	Hi-z/–	I	t8
M16	EINT1/GPF1	GPF1	–/–	Hi-z/–	I	t8
L13	EINT2/GPF2	GPF2	–/–	Hi-z/–	I	t8
M15	EINT3/GPF3	GPF3	–/–	Hi-z/–	I	t8
M17	EINT4/GPF4	GPF4	–/–	Hi-z/–	I	t8
L14	EINT5/GPF5	GPF5	–/–	Hi-z/–	I	t8
L15	EINT6/GPF6	GPF6	–/–	Hi-z/–	I	t8
L16	EINT7/GPF7	GPF7	–/–	Hi-z/–	I	t8
N9	EINT8/GPG0	GPG0	–/–	Hi-z/–	I	t8
T9	EINT9/GPG1	GPG1	–/–	Hi-z/–	I	t8
J10	EINT10/nSS0/GPG2	GPG2	–/–/–	Hi-z/Hi-z/–	I	t8
R10	EINT11/nSS1/GPG3	GPG3	–/–/–	Hi-z/Hi-z/–	I	t8
P11	EINT12/LCD_PWREN/GPG4	GPG4	–/–/–	Hi-z/O(L)/–	I	t8
K10	EINT13/SPIMISO1/GPG5	GPG5	–/–/–	Hi-z/Hi-z/–	I	tt8
R11	EINT14/SPIMOSI1/GPG6	GPG6	–/–/–	Hi-z/Hi-z/–	I	tt8
L10	EINT15/SPICLK1/GPG7	GPG7	–/–/–	Hi-z/Hi-z/–	I	tt8

Table 7-2. S3C2440A 289-Pin FBGA Pin Assignments (Sheet 4 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
T10	EINT16/GPG8	GPG8	–/–	Hi-z/–	I	t8
M11	EINT17/nRTS1/GPG9	GPG9	–/–/–	Hi-z/O(H)/–	I	t8
N10	EINT18/nCTS1/GPG10	GPG10	–/–/–	Hi-z/Hi-z/–	I	t8
U12	EINT19/TCLK1/GPG11	GPG11	–/–/–	Hi-z/Hi-z/–	I	t12
M10	EINT20/GPG12	GPG12	–/–	Hi-z/–	I	t12
T11	EINT21/GPG13	GPG13	–/–	Hi-z/–	I	t12
L11	EINT22/GPG14	GPG14	–/–	Hi-z/–	I	t12
U13	EINT23/GPG15	GPG15	–/–	Hi-z/–	I	t12
H12	EXTCLK	EXTCLK	–	–	AI	is
P17	UPLLCAP	UPLLCAP	–	–	AI	r50
N14	MPLLCAP	MPLLCAP	–	–	AI	r50
H14	nBATT_FLT	nBATT_FLT	–	–	I	is
D4	nBE0	nBE0	Hi-z	Hi-z,O(H)	O(H)	t10s
B5	nBE1	nBE1	Hi-z	Hi-z,O(H)	O(H)	t10s
D5	nBE2	nBE2	Hi-z	Hi-z,O(H)	O(H)	t10s
E5	nBE3	nBE3	Hi-z	Hi-z,O(H)	O(H)	t10s
R12	NCON	NCON	–	–	I	is
G6	FRnB	FRnB	–	Hi-z,O(L)	I	d2s
F3	nFWE/GPA19	GPA19	O(H)/–	Hi-z,O(H)/–	O(H)	t10s
E1	nFRE/GPA20	GPA20	O(H)/–	Hi-z,O(H)/–	O(H)	t10s
F4	nFCE/GPA22	GPA21	O(H)/–	Hi-z,O(H)/–	O(H)	t10s
F5	CLE/GPA17	GPA17	O(L)/–	Hi-z,O(L)/–	O(L)	t10s
D1	ALE/GPA18	GPA18	O(L)/–	Hi-z,O(L)/–	O(L)	t10s
N13	nRSTOUT/GPA21	GPA21	–/–	O(L)/–	O(L)	b8
C5	nOE	nOE	Hi-z	Hi-z,O(H)	O(H)	t10s
H16	nRESET	nRESET	–	–	I	is
F6	nGCS0	nGCS0	Hi-z	Hi-z,O(H)	O(H)	t10s
B2	nGCS1/GPA12	GPA12	Hi-z/–	Hi-z,O(H)/–	O(H)	t10s
C3	nGCS2/GPA13	GPA13	Hi-z/–	Hi-z,O(H)/–	O(H)	t10s
C4	nGCS3/GPA14	GPA14	Hi-z/–	Hi-z,O(H)/–	O(H)	t10s
D3	nGCS4/GPA15	GPA15	Hi-z/–	Hi-z,O(H)/–	O(H)	t10s
C2	nGCS5/GPA16	GPA16	Hi-z/–	Hi-z,O(H)/–	O(H)	t10s
D2	nGCS6	nGCS6	Hi-z	Hi-z,O(H)	O(H)	t10s

Table 7-2. S3C2440A 289-Pin FBGA Pin Assignments (Sheet 5 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
E3	nGCS7	nGCS7	Hi-z	Hi-z,O(H)	O(H)	t10s
D6	nSCAS	nSCAS	Hi-z	Hi-z,O(H)	O(H)	t10s
C6	nSRAS	nSRAS	Hi-z	Hi-z,O(H)	O(H)	t10s
H15	nTRST	nTRST	I	–	I	is
E4	nWAIT	nWAIT	–	Hi-z,O(L)	I	d2s
E6	nWE	nWE	Hi-z	Hi-z,O(H)	O(H)	t10s
J6	TOUT0/GPB0	GPB0	–/–	O(L)/–	I	t8
J5	TOUT1/GPB1	GPB1	–/–	O(L)/–	I	t8
J7	TOUT2/GPB2	GPB2	–/–	O(L)/–	I	t8
K3	TOUT3/GPB3	GPB3	–/–	O(L)/–	I	t8
K4	TCLK0/GPB4	GPB4	–/–	–/–	I	t8
K2	nXBACK/GPB5	GPB5	–/–	O(H)/–	I	t8
L5	nXBREQ/GPB6	GPB6	–/–	–/–	I	t8
K7	nXDACK1/GPB7	GPB7	–/–	O(H)/–	I	t8
K5	nXDREQ1/GPB8	GPB8	–/–	–/–	I	t8
L3	nXDACK0/GPB9	GPB9	–/–	O(H)/–	I	t8
K6	nXDREQ0/GPB10	GPB10	–/–	–/–	I	t8
T15	OM0	OM0	–	–	I	is
R13	OM1	OM1	–	–	I	is
P13	OM2	OM2	–	–	I	is
T13	OM3	OM3	–	–	I	is
J12	PWREN	PWREN	O(H)	O(L)	O(H)	b8
K11	nCTS0/GPH0	GPH0	–/–	–/–	I	t8
L17	nRTS0/GPH1	GPH1	–/–	O(H)/–	I	t8
K13	TXD0/GPH2	GPH2	–/–	O(H)/–	I	t8
K14	RXD0/GPH3	GPH3	–/–	–/–	I	t8
K16	TXD1/GPH4	GPH4	–/–	O(H)/–	I	t8
K17	RXD1/GPH5	GPH5	–/–	–/–	I	t8
J11	TXD2/nRTS1/GPH6	GPH6	–/–/–	O(H)/O(H)/–	I	t8
J15	RXD2/nCTS1/GPH7	GPH7	–/–/–	Hi-z/Hi-z/–	I	t8
K15	UARTCLK/GPH8	GPH8	–/–	Hi-z/–	I	t8
R9	CLKOUT0/GPH9	GPH9	–/–	O(L)/–	I	t12
P10	CLKOUT1/GPH10	GPH10	–/–	O(L)/–	I	t12

Table 7-2. S3C2440A 289-Pin FBGA Pin Assignments (Sheet 6 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
A2	SCKE	SCKE	Hi-z	O(L)	O(H)	t10s
B4	SCLK0	SCLK0	Hi-z	O(L)	O(SCLK)	t12s
B3	SCLK1	SCLK1	Hi-z	O(L)	O(SCLK)	t12s
P7	I2SLRCK/GPE0	GPE0	–/–	Hi-z/–	I	t8
R7	I2SSCLK/GPE1	GPE1	–/–	Hi-z/–	I	t8
T7	CDCLK/GPE2	GPE2	–/–	Hi-z/–	I	t8
L8	I2SSDI/nSS0/GPE3	GPE3	–/–/–	Hi-z/Hi-z/–	I	t8
U6	I2SSDO/I2SSDI/GPE	GPE4	–/–/–	O(L)/Hi-z/–	I	t8
N8	SDCLK/GPE5	GPE5	–/–	O(L)/–	I	t8
K8	SDCMD/GPE6	GPE6	–/–	Hi-z/–	I	t8
R8	SDDAT0/GPE7	GPE7	–/–	Hi-z/–	I	t8
M8	SDDAT1/GPE8	GPE8	–/–	Hi-z/–	I	t8
P8	SDDAT2/GPE9	GPE9	–/–	Hi-z/–	I	t8
J9	SDDAT3/GPE10	GPE10	–/–	Hi-z/–	I	t8
K9	SPIMISO0/GPE11	GPE11	–/–	Hi-z/–	I	tt8
P9	SPIMOSI0/GPE12	GPE12	–/–	Hi-z/–	I	tt8
L9	SPICLK0/GPE13	GPE13	–/–	Hi-z/–	I	tt8
U8	IICSCL/GPE14	GPE14	–/–	Hi-z/–	I	d8
M9	IICSDA/GPE15	GPE15	–/–	Hi-z/–	I	d8
J13	TCK	TCK	I	–	I	is
H17	TDI	TDI	I	–	I	is
J16	TDO	TDO	O	O	O	ot
J14	TMS	TMS	I	–	I	is
L1	LEND/GPC0	GPC0	–/–	O(L)/–	I	t8
L4	VCLK/GPC1	GPC1	–/–	O(L)/–	I	t8
M1	VLINE/GPC2	GPC2	–/–	O(L)/–	I	t8
L7	VFRAME/GPC3	GPC3	–/–	O(L)/–	I	t8
M4	VM/GPC4	GPC4	–/–	O(L)/–	I	t8
M3	LCD_LPCOE/GPC5	GPC5	–/–	O(L)/–	I	t8
M2	LCD_LPCREV/GPC6	GPC6	–/–	O(L)/–	I	t8
P1	LCD_LPCREVB/GPC	GPC7	–/–	O(L)/–	I	t8
N2	VD0/GPC8	GPC8	–/–	O(L)/–	I	t8
L6	VD1/GPC9	GPC9	–/–	O(L)/–	I	t8

Table 7-2. S3C2440A 289-Pin FBGA Pin Assignments (Sheet 7 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
N4	VD2/GPC10	GPC10	–/–	O(L)/–	I	t8
R1	VD3/GPC11	GPC11	–/–	O(L)/–	I	t8
N3	VD4/GPC12	GPC12	–/–	O(L)/–	I	t8
P2	VD5/GPC13	GPC13	–/–	O(L)/–	I	t8
M6	VD6/GPC14	GPC14	–/–	O(L)/–	I	t8
P3	VD7/GPC15	GPC15	–/–	O(L)/–	I	t8
R2	VD8/GPD0	GPD0	–/–	O(L)/–	I	t8
M5	VD9/GPD1	GPD1	–/–	O(L)/–	I	t8
N5	VD10/GPD2	GPD2	–/–	O(L)/–	I	t8
R3	VD11/GPD3	GPD3	–/–	O(L)/–	I	t8
P4	VD12/GPD4	GPD4	–/–	O(L)/–	I	t8
R4	VD13/USBTXDN1/GPD5	GPD5	–/–/–	O(L)/O/–	I	t8
P5	VD14/USBTXDP1/GPD6	GPD6	–/–/–	O(L)/O/–	I	t8
N6	VD15/USBOEN1/GPD7	GPD7	–/–/–	O(L)/O/–	I	t8
M7	VD16/SPIMISO1/GPD8	GPD8	–/–/–	O(L)/Hi-z/–	I	tt8
T4	VD17/SPIMOSI1/GPD9	GPD9	–/–/–	O(L)/Hi-z/–	I	tt8
R5	VD18/SPICLK1/GPD10	GPD10	–/–/–	O(L)/Hi-z/–	I	tt8
T5	VD19/USBRXDP1/GPD11	GPD11	–/–/–	O(L)/Hi-z/–	I	t8
P6	VD20/USBRXDN1/GPD12	GPD12	–/–/–	O(L)/Hi-z/–	I	t8
R6	VD21/USBRXD1/GPD13	GPD13	–/–/–	O(L)/Hi-z/–	I	t8
N7	VD22/nSS1/GPD14	GPD14	–/–/–	O(L)/Hi-z/–	I	t8
U5	VD23/nSS0/GPD15	GPD15	–/–/–	O(L)/Hi-z/–	I	t8
U16	Vref	Vref	–	–	AI	ia
G14	XTIpll	XTIpll	–	–	AI	m26
M14	Xtirtc	Xtirtc	–	–	AI	nc
G15	XTOpll	XTOpll	–	–	AO	m26
L12	Xtortc	Xtortc	–	–	AO	nc
N15	VDD_RTC	VDD_RTC	P	P	P	drtc
P14	VDDA_ADC	VDDA_ADC	P	P	P	d33t
N16	VDDA_MPLL	VDDA_MPLL	P	P	P	d33t
M13	VDDA_UPLL	VDDA_UPLL	P	P	P	d33t
G4	VDDalive	VDDalive	P	P	P	d12i
J17	VDDalive	VDDalive	P	P	P	d12i

Table 7-2. S3C2440A 289-Pin FBGA Pin Assignments (Sheet 8 of 9)

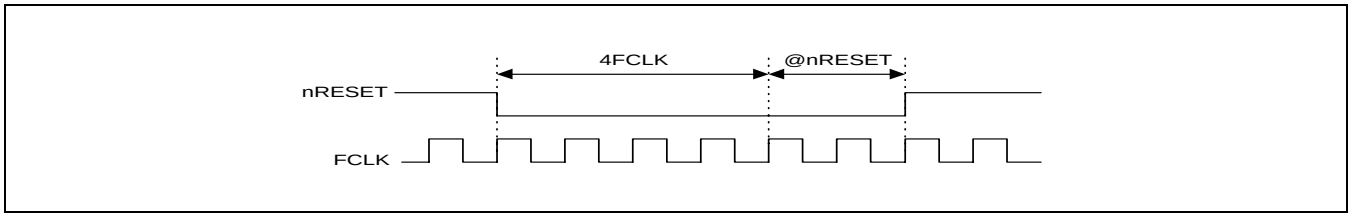
Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
A1	VDDi	VDDi	P	P	P	d12c
A10	VDDi	VDDi	P	P	P	d12c
A16	VDDi	VDDi	P	P	P	d12c
A6	VDDi	VDDi	P	P	P	d12c
B11	VDDi	VDDi	P	P	P	d12c
F1	VDDi	VDDi	P	P	P	d12c
F16	VDDi	VDDi	P	P	P	d12c
J2	VDDiarm	VDDiarm	P	P	P	d12c
L2	VDDiarm	VDDiarm	P	P	P	d12c
T6	VDDiarm	VDDiarm	P	P	P	d12c
T8	VDDiarm	VDDiarm	P	P	P	d12c
U1	VDDiarm	VDDiarm	P	P	P	d12c
U11	VDDi	VDDi	P	P	P	d12c
U2	VDDiarm	VDDiarm	P	P	P	d12c
A9	VDDMOP	VDDMOP	P	P	P	d33o
B12	VDDMOP	VDDMOP	P	P	P	d33o
B14	VDDMOP	VDDMOP	P	P	P	d33o
B16	VDDMOP	VDDMOP	P	P	P	d33o
B6	VDDMOP	VDDMOP	P	P	P	d33o
C1	VDDMOP	VDDMOP	P	P	P	d33o
F17	VDDMOP	VDDMOP	P	P	P	d33o
J1	VDDOP	VDDOP	P	P	P	d33o
T12	VDDOP	VDDOP	P	P	P	d33o
T3	VDDOP	VDDOP	P	P	P	d33o
K12	VDDOP	VDDOP	P	P	P	d33o
T14	VSSA_ADC	VSSA_ADC	P	P	P	st
R17	VSSA_MPLL	VSSA_MPLL	P	P	P	st
M12	VSSA_UPLL	VSSA_UPLL	P	P	P	st
A12	VSSi	VSSi	P	P	P	si
A3	VSSi	VSSi	P	P	P	si
A4	VSSi	VSSi	P	P	P	si
B10	VSSi	VSSi	P	P	P	si
C17	VSSi	VSSi	P	P	P	si

Table 7-2. S3C2440A 289-Pin FBGA Pin Assignments (Sheet 9 of 9)

Pin Number	Pin Name	Default Function	I/O State @BUS REQ	I/O State @Sleep	I/O State @nRESET	I/O Type
F2	VSSi	VSSi	P	P	P	si
G17	VSSi	VSSi	P	P	P	si
H1	VSSiarm	VSSiarm	P	P	P	si
K1	VSSiarm	VSSiarm	P	P	P	si
T1	VSSiarm	VSSiarm	P	P	P	si
T2	VSSiarm	VSSiarm	P	P	P	si
U10	VSSiarm	VSSiarm	P	P	P	si
U4	VSSiarm	VSSiarm	P	P	P	si
U7	VSSiarm	VSSiarm	P	P	P	si
A11	VSSMOP	VSSMOP	P	P	P	so
A15	VSSMOP	VSSMOP	P	P	P	so
A5	VSSMOP	VSSMOP	P	P	P	so
A7	VSSMOP	VSSMOP	P	P	P	so
B1	VSSMOP	VSSMOP	P	P	P	so
B13	VSSMOP	VSSMOP	P	P	P	so
D16	VSSMOP	VSSMOP	P	P	P	so
D17	VSSMOP	VSSMOP	P	P	P	so
E2	VSSMOP	VSSMOP	P	P	P	so
G1	VSSOP	VSSOP	P	P	P	so
N1	VSSOP	VSSOP	P	P	P	so
U15	VSSOP	VSSOP	P	P	P	so
U3	VSSOP	VSSOP	P	P	P	so
U9	VSSOP	VSSOP	P	P	P	so
H11	VSSOP	VSSOP	P	P	P	so

NOTES

1. The @BUS REQ. shows the pin state at the external bus, which is used by the other bus master.
2. ' – ' Mark indicates the unchanged pin state at Bus Request mode.
3. Hi-z or Pre means Hi-z or early state and it is determined by the setting of MISCCR register.
4. AI/AO means analog input/analog output.
5. P, O means power, and I input and output respectively.
6. The I/O state @nRESET shows the pin status in the @nRESET duration below.
7. The table below shows I/O types and the descriptions.



I/O Type	Descriptions
d12i(vdd12ih)	1.2V Vdd for alive power
d12c(vdd12ih_core), si(vssih)	1.2V Vdd/Vss for internal logic
d33o(vdd33oph), so(vssoph)	3.3V Vdd/Vss for external logic
d33t(vdd33th_abb), st(vssbbh_abb)	3.3V Vdd/Vss for analog circuitry
drtc(vdd30th_rtc)	3.0V Vdd for RTC power
t8(phbsu100ct8sm)	bi-directional pad, lvcmos Schmitt-trigger, 100kΩ pull-up resistor with control, tri-state, io=8mA
is(phis)	Input pad, LVCMOS Schmitt-trigger level
us(pbusb0)	USB pad
t10(phtot10cd)	5V tolerant output pad, Tri-state.
ot(phot8)	Output pad, tri-state, Io=8mA
b8(phob8)	Output pad, Io=8mA
t16(phot16sm)	Output pad, tri-state, medium slew rate, Io=16mA
r10(phiar10_abb)	Analog input pad with 10Ω resistor
ia(phia_abb)	Analog input pad
gp(phgpad_option)	Pad for analog pin
m26(phsoscm26_2440)	Oscillator cell with enable and feedback resistor
tt8(phtbsu100ct8sm)	5V tolerant bi-directional pad, LVCMOS Schmitt-trigger, 100kΩ pull-up resistor with control, tri -state, medium slew rate, Io=8mA
t12(phbsu100ct12sm)	Bi-directional pad, LVCMOS Schmitt-trigger, 100kΩ pull-up resistor with control, tri-state, Io=12mA
d2(phtod2)	5v tolerant output pad, Open Drain, Io=2mA
d8(phbsd8sm)	Bi-directional pad, LVCMOS Schmitt-trigger, Open Drain, Io=8mA
t10s(phtot10cd_10_2440x)	5V Tolerant output pad, LVCMOS, tri -state, output drive strength control, Io=4, 6, 8, 10mA
b12s(phtbsu100ct12cd_12_2440x)	5V tolerant bi-directional pad, LVCMOS Schmitt-trigger, 100kΩ pull-up resistor with control, tri -state, output drive strength control, Io=6,8,10,12mA
d2s(phtbsd2_2440x)	5V Tolerant bi-directional pad, LVCMOS Schmitt-trigger, open-drain, output drive strength ignore,
r50(phoar50_abb)	Analog output pad, 50kΩ resistor, separated bulk-bias
t12s(phtot12cd_12_2440x)	5V Tolerant output pad, LVCMOS, tri -state, output drive strength control, Io=6, 8, 12, 16mA
nc(phnc)	No connection pad

2. SIGNAL PIN DESCRIPTIONS

Table 7-3. S3C2440A Signal Pin Descriptions (Sheet 1 of 6)

Signal	I/O	Descriptions	
Bus Controller			
OM [1:0]	I	OM [1:0] sets S3C2440A in the TEST mode, which is used only at fabrication. Also, it determines the bus width of nGCS0. The pull-up/down resistor determines the logic level during RESET cycle. 00: NAND-boot 01: 16-bit 10: 32-bit 11: Test mode	
ADDR [26:0]	O	ADDR [26:0] (Address Bus) outputs the memory address of the corresponding bank.	
DATA [31:0]	IO	DATA [31:0] (Data Bus) inputs data during memory read and outputs data during memory write. The bus width is programmable among 8/16/32-bit.	
nGCS [7:0]	O	nGCS [7:0] (General Chip Select) are activated when the address of a memory is within the address region of each bank. The number of access cycles and the bank size can be programmed.	
nWE	O	nWE (Write Enable) indicates that the current bus cycle is a write cycle.	
nOE	O	nOE (Output Enable) indicates that the current bus cycle is a read cycle.	
nXBREQ	I	nXBREQ (Bus Hold Request) allows another bus master to request control of the local bus. BACK active indicates that bus control has been granted.	
nXBACK	O	nXBACK (Bus Hold Acknowledge) indicates that the S3C2440A has surrendered control of the local bus to another bus master.	
nWAIT	I	nWAIT requests to prolong a current bus cycle. As long as nWAIT is L, the current bus cycle cannot be completed.	
SDRAM/SRAM			
nSRAS	O	SDRAM row address strobe	
nSCAS	O	SDRAM column address strobe	
nSCS [1:0]	O	SDRAM chip select	
DQM [3:0]	O	SDRAM data mask	
SCLK [1:0]	O	SDRAM clock	
SCKE	O	SDRAM clock enable	
nBE [3:0]	O	Upper byte/lower byte enable (In case of 16-bit SRAM)	
nWBE [3:0]	O	Write byte enable	
NAND Flash			
CLE	O	Command latch enable	
ALE	O	Address latch enable	
nFCE	O	NAND flash chip enable	
nFRE	O	NAND flash read enable	
nFWE	O	NAND flash write enable	
NCON	I	NAND flash configuration	If NAND flash controller is not used, it has to be pull-up. (3.3V)
FRnB	I	NAND flash ready/busy	

Table 7-3. S3C2440A Signal Pin Descriptions (Sheet 2 of 6)

Signal	I/O	Descriptions
LCD Control Unit		
VD [23:0]	O	**STN/TFT/SEC TFT:** LCD Data Bus
LCD_PWREN	O	**STN/TFT/SEC TFT:** LCD panel power enable control signal
VCLK	O	**STN/TFT:** LCD clock signal
VFRAME	O	**STN:** LCD Frame signal
VLINE	O	**STN:** LCD line signal
VM	O	**STN:** VM alternates the polarity of the row and column voltage
VSYNC	O	**TFT:** Vertical synchronous signal
HSYNC	O	**TFT:** Horizontal synchronous signal
VDEN	O	**TFT:** Data enable signal
LEND	O	**TFT:** Line End signal
STV	O	**SEC TFT:** SEC (Samsung Electronics Company) TFT LCD panel control signal
CPV	O	**SEC TFT:** SEC (Samsung Electronics Company) TFT LCD panel control signal
LCD_HCLK	O	**SEC TFT:** SEC (Samsung Electronics Company) TFT LCD panel control signal
TP	O	**SEC TFT:** SEC (Samsung Electronics Company) TFT LCD panel control signal
STH	O	**SEC TFT:** SEC (Samsung Electronics Company) TFT LCD panel control signal
LCD_LPCOE	O	**SEC TFT:** Timing control signal for specific TFT LCD
LCD_LPCREV	O	**SEC TFT:** Timing control signal for specific TFT LCD
LCD_LPCREVB	O	**SEC TFT:** Timing control signal for specific TFT LCD
CAMERA Interface		
CAMRESET	O	Software reset to the camera
CAMCLKOUT	O	Master clock to the camera
CAMPCLK	I	Pixel clock from camera
CAMHREF	I	Horizontal sync signal from camera
CAMVSYNC	I	Vertical sync signal from camera
CAMDATA [7:0]	I	Pixel data for YCbCr
Interrupt Control Unit		
EINT [23:0]	I	External interrupt request
DMA		
nXDREQ[1:0]	I	External DMA request
nXDACK[1:0]	O	External DMA acknowledge

Table 7-3. S3C2440A Signal Pin Descriptions (Sheet 3 of 6)

Signal	I/O	Descriptions
UART		
RxD[2:0]	I	UART receives data input
TxD[2:0]	O	UART transmits data output
nCTS[1:0]	I	UART clear to send input signal
nRTS[1:0]	O	UART request to send output signal
UARTCLK	I	UART clock signal
ADC		
AIN [7:0]	AI	ADC input [7:0]. If it is not used pin, it has to be low (Ground).
Vref	AI	ADC Vref
IIC-Bus		
IICSDA	IO	IIC-bus data
IICSCL	IO	IIC-bus clock
IIS-Bus		
I2SLRCK	IO	IIS-bus channel select clock
I2SSDO	O	IIS-bus serial data output
I2SSDI	I	IIS-bus serial data input
I2SSCLK	IO	IIS-bus serial clock
CDCLK	O	CODEC system clock
Touch Screen		
nXPON	O	Plus X-axis on-off control signal
XMON	O	Minus X-axis on-off control signal
nYPON	O	Plus Y-axis on-off control signal
YMON	O	Minus Y-axis on-off control signal
USB Host		
DN [1:0]	IO	DATA (–) from USB host
DP [1:0]	IO	DATA (+) from USB host
USB Device		
PDN0	IO	DATA (–) for USB peripheral
PDP0	IO	DATA (+) for USB peripheral
SPI		
SPIMISO [1:0]	IO	SPIMISO is the master data input line, when SPI is configured as a master. When SPI is configured as a slave, these pins reverse its role.
SPIMOSI [1:0]	IO	SPIMOSI is the master data output line, when SPI is configured as a master. When SPI is configured as a slave, these pins reverse its role.
SPICLK [1:0]	IO	SPI clock
nSS [1:0]	I	SPI chip select (only for slave mode)

Table 7-3. S3C2440A Signal Pin Descriptions (Sheet 4 of 6)

Signal	I/O	Description
SD		
SDDAT [3:0]	IO	SD receive/transmit data
SDCMD	IO	SD receive response/ transmit command
SDCLK	O	SD clock
General Port		
GPn [116:0]	IO	General input/output ports (some ports are output only)
TIMMER/PWM		
TOUT [3:0]	O	Timer output [3:0]
TCLK [1:0]	I	External timer clock input
JTAG TEST LOGIC		
nTRST	I	nTRST(TAP Controller Reset) resets the TAP controller at start. If debugger is used, A 10K pull-up resistor has to be connected. If debugger (black ICE) is not used, nTRST pin must be issued by a low active pulse (Typically connected to nRESET).
TMS	I	TMS (TAP Controller Mode Select) controls the sequence of the TAP controller's states. A 10K pull-up resistor has to be connected to TMS pin.
TCK	I	TCK (TAP Controller Clock) provides the clock input for the JTAG logic. A 10K pull-up resistor must be connected to TCK pin.
TDI	I	TDI (TAP Controller Data Input) is the serial input for test instructions and data. A 10K pull-up resistor must be connected to TDI pin.
TDO	O	TDO (TAP Controller Data Output) is the serial output for test instructions and data.

Table 7-3. S3C2440A Signal Pin Descriptions (Sheet 5 of 6)

Signal	I/O	Description
Reset, Clock & Power		
XTOpll	AO	Crystal output for internal OSC circuit. When OM [3:2] = 00b, XTIpll is used for MPLL CLK source and UPLL CLK source. When OM [3:2] = 01b, XTIpll is used for MPLL CLK source only. When OM [3:2] = 10b, XTIpll is used for UPLL CLK source only. If it is not used, it has to be a floating pin.
MPLLCAP	AI	Loop filter capacitor for main clock.
UPLLCAP	AI	Loop filter capacitor for USB clock.
XTIrtc	AI	32 kHz crystal input for RTC. If it is not used, it has to be High (3.3V).
XTOrtc	AO	32 kHz crystal output for RTC. If it is not used, it has to be Float.
CLKOUT [1:0]	O	Clock output signal. The CLKSEL of MISCCR register configures the clock output mode among the MPLL CLK, UPLL CLK, FCLK, HCLK, and PCLK.
nRESET	ST	nRESET suspends any operation in progress and places S3C2440A into a known reset state. For a reset, nRESET must be held to L level for at least 4 FCLK after the processor power has been stabilized.
nRSTOUT	O	For external device reset control (nRSTOUT = nRESET & nWDTRST & SW_RESET)
PWREN	O	1.2V core power on-off control signal
nBATT_FLT	I	Probe for battery state (Does not wake up at Sleep mode in case of low battery state). If it isn't used, it has to be High (3.3V).
OM [3:2]	I	OM [3:2] determines how the clock is made. OM [3:2] = 00b, Crystal is used for MPLL CLK source and UPLL CLK source. OM [3:2] = 01b, Crystal is used for MPLL CLK source and EXTCLK is used for UPLL CLK source. OM [3:2] = 10b, EXTCLK is used for MPLL CLK source and Crystal is used for UPLL CLK source. OM [3:2] = 11b, EXTCLK is used for MPLL CLK source and UPLL CLK source.
EXTCLK	I	External clock source. When OM [3:2] = 11b, EXTCLK is used for MPLL CLK source and UPLL CLK source. When OM [3:2] = 10b, EXTCLK is used for MPLL CLK source only. When OM [3:2] = 01b, EXTCLK is used for UPLL CLK source only. If it is not used, it has to be High (3.3V).
XTIpll	AI	Crystal Input for internal OSC circuit. When OM [3:2] = 00b, XTIpll is used for MPLL CLK source and UPLL CLK source. When OM [3:2] = 01b, XTIpll is used for MPLL CLK source only. When OM [3:2] = 10b, XTIpll is used for UPLL CLK source only. If it is not used, XTIpll has to be High (3.3V).

Table 7-3. S3C2440A Signal Pin Descriptions (Sheet 6 of 6)

Signal	I/O	Description
Power		
VDDalive	P	S3C2440A reset block and port status register VDD (1.2V). It should be always supplied whether in normal mode or in Sleep mode.
VDDi/VDDiarm	P	S3C2440A core logic VDD (1.2V) for CPU.
VSSi/VSSiarm	P	S3C2440A core logic VSS
VDDi_MPLL	P	S3C2440A MPLL analog and digital VDD (1.2 V).
VSSi_MPLL	P	S3C2440A MPLL analog and digital VSS.
VDDOP	P	S3C2440A I/O port VDD (3.3V)
VDDMOP	P	S3C2440A memory I/O VDD 3.3V: SCLK up to 100MHz 2.5V: SCLK up to 80MHz
VSSOP	P	S3C2440A I/O port VSS
RTCVDD	P	RTC VDD (3.0V) (This pin must be connected to power properly if RTC isn't used)
VDDi_UPLL	P	S3C2440A UPLL analog and digital VDD (1.2V)
VSSi_UPLL	P	S3C2440A UPLL analog and digital VSS
VDDA_ADC	P	S3C2440A ADC VDD (3.3V)
VSSA_ADC	P	S3C2440A ADC VSS

NOTE:
1. I/O means input/output.
2. AI/AO means analog input/analog output.
3. ST means Schmitt-trigger.
4. P means power.

3. PACKAGE DIMENSIONS

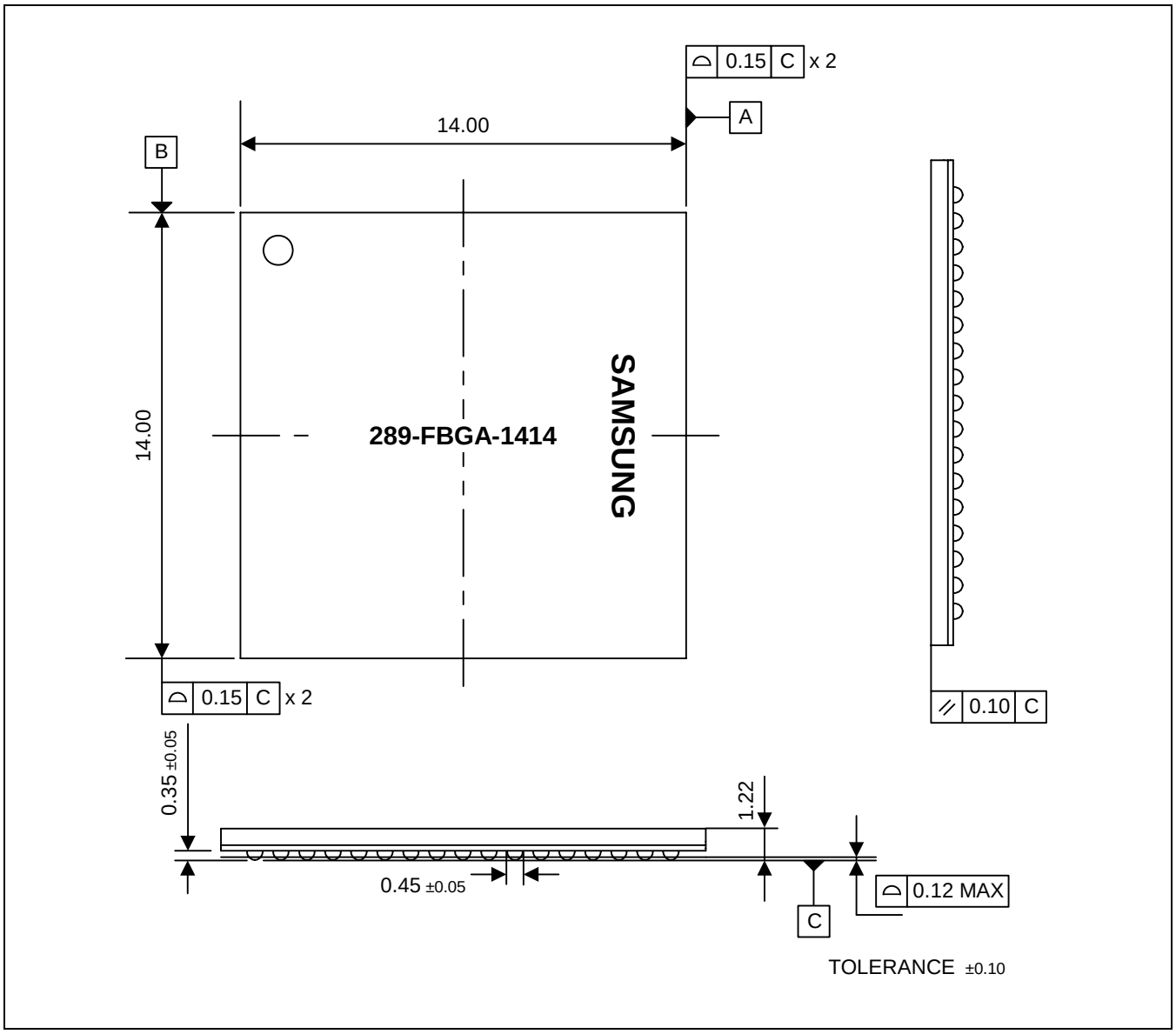


Figure 7-2. 289-FBGA-1414 Package Dimensions 1 (Top View)

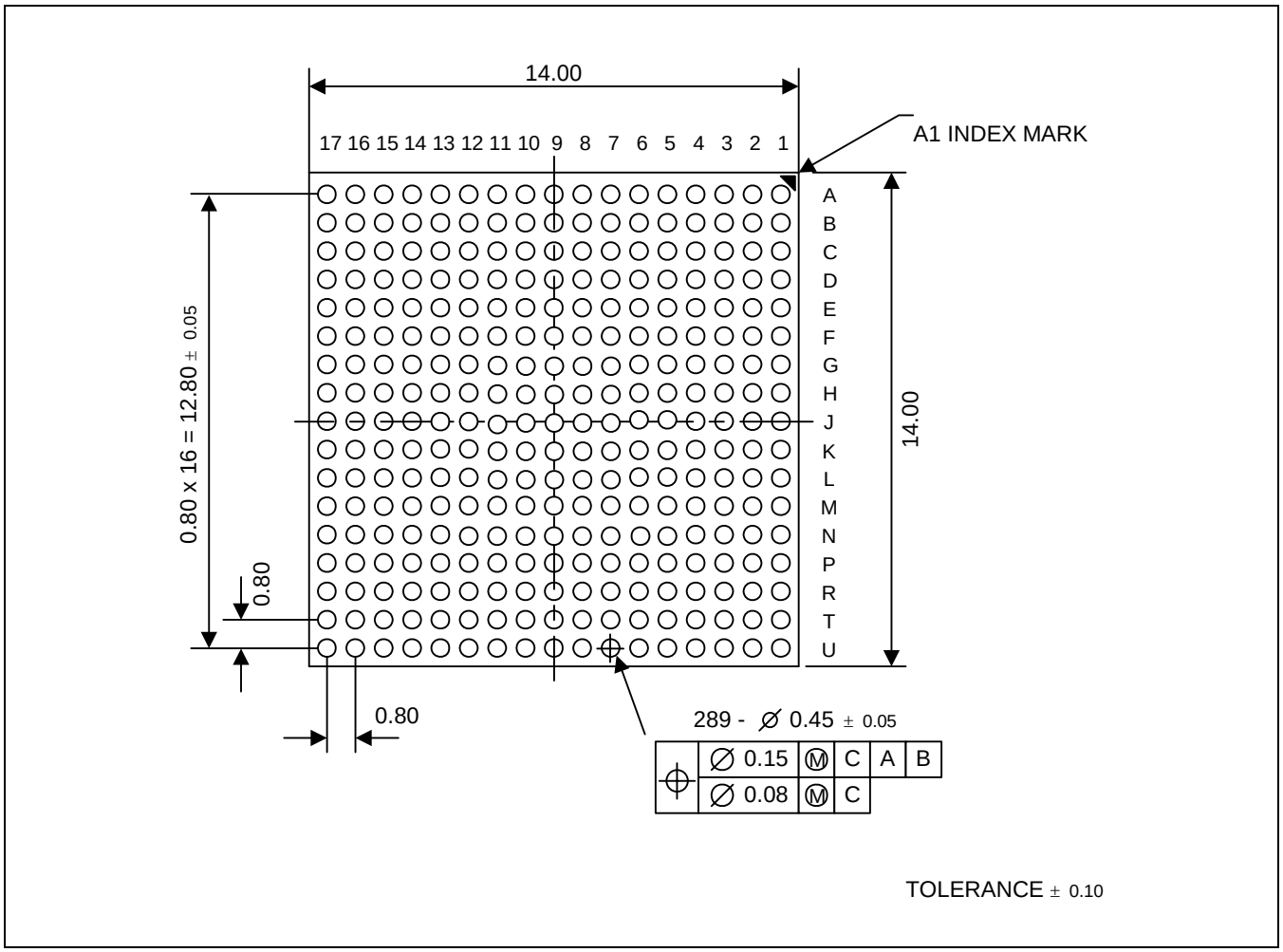


Figure 7-3. 289-FBGA-1414 Package Dimensions 2 (Bottom View)

4. BALL MATERIALS AND SURFACE PAD DIMENSION

Ball material: Normal SnPb (63:37), Pb-free Sn3.0Ag0.5Cu
Solder paste: Normal
Bottom Metal: Cu with Ni/Au layer
Recommended land open size is 0.39 – 0.41mm diameter.

8 CHECK LIST

1. SCHEMATIC REVIEW

Check Items	Recommendations		Checking
	Used	Unused	
Bus Controller			
OM [1:0]	10Kohm pull-up resistor to 3.3V and Connect to GND. Refer to in Table 2-3.	10Kohm pull-up resistor to 3.3V and Connect to GND. Refer to in Table 2-3.	
ADDR [26:0]	Connect to Address lines of External device.	Leave as a No Connect.	
DATA [31:0]	Connect to Data lines of External device.	Leave as a No Connect.	
nGCS [7:0]	Connect to Chip Select of External device.	Leave as a No Connect.	
nWE	Connect to Write Enable of External device.	Leave as a No Connect.	
nOE	Connect to Output Enable of External device.	Leave as a No Connect.	
nXBREQ	Connect to Bus Hold Request of External device.	10Kohm pull-up resistors to 3.3V.	
nXBACK	Connect to Bus Hold Acknowledge of External device.	Leave as a No Connect.	
nWAIT	Connect to Wait signal of External device. Pull-up required.	10Kohm pull-up resistors to 3.3V.	
SDRAM/SRAM			
nSRAS	Connect to SDRAM Row Address Strobe.	Leave as a No Connect.	
nSCAS	Connect to SDRAM Column Address Strobe.	Leave as a No Connect.	
nSCS [1:0]	Connect to SDRAM Chip Select.	Leave as a No Connect.	
DQM [3:0]	Connect to SDRAM Data Mask.	Leave as a No Connect.	
SCLK [1:0]	Connect to SDRAM Clock.	Leave as a No Connect.	
SCKE	Connect to SDRAM Clock Enable.	Leave as a No Connect.	
nBE [3:0]	Connect to Upper/Lower Byte Enable of External device.	Leave as a No Connect.	
nWBE [3:0]	Connect to Write Byte Enable of External device.	Leave as a No Connect.	

Check Items	Recommendations		Checking
	Used	Unused	
NAND Flash			
CLE	Connect to NAND Flash or External device Command Latch Enable.	Leave as a No Connect.	
ALE	Connect to NAND Flash or External device Address Latch Enable.	Leave as a No Connect.	
nFCE	Connect to NAND Flash Chip Enable.	Leave as a No Connect.	
nFRE	Connect to NAND Flash Read Enable.	Leave as a No Connect.	
nFWE	Connect to NAND Flash Write Enable.	Leave as a No Connect.	
NCON	10Kohm pull-up resistors to 3.3V or GND. Refer to Chapter 6, “NAND Flash Controller” in User’s Manual.	10Kohm pull-up resistors to 3.3V.	
FRnB	Connect to NAND Flash Ready/Busy. 10Kohm pull-up resistors to 3.3V.	10Kohm pull-up resistors to 3.3V.	
LCD Control Unit			
VD [23:0]	Connect to STN/TFT/SEC TFT LCD Data Lines.	Leave as a No Connect.	
LCD_PWREN	Connect to STN/TFT/SEC LCD Power Enable.	Leave as a No Connect.	
VCLK	Connect to STN/TFT LCD Clock.	Leave as a No Connect.	
VFRAME	Connect to STN LCD Frame.	Leave as a No Connect.	
VLINE	Connect to STN LCD Line.	Leave as a No Connect.	
VM	Connect to STN LCD VM.	Leave as a No Connect.	
VSYNC	Connect to TFT LCD Vertical Synchronous.	Leave as a No Connect.	
HSYNC	Connect to TFT LCD Horizontal Synchronous.	Leave as a No Connect.	
VDEN	Connect to TFT LCD Data Enable.	Leave as a No Connect.	
LEND	Connect to TFT LCD Line End.	Leave as a No Connect.	
STV	Connect to SEC TFT LCD panel control.	Leave as a No Connect.	
CPV	Connect to SEC TFT LCD panel control.	Leave as a No Connect.	
LCD_HCLK	Connect to SEC TFT LCD panel control.	Leave as a No Connect.	
TP	Connect to SEC TFT LCD panel control.	Leave as a No Connect.	
STH	Connect to SEC TFT LCD panel control.	Leave as a No Connect.	
LCD_LPCOE	Connect to SEC TFT LCD Timing control signal.	Leave as a No Connect.	
LCD_LPCREV	Connect to SEC TFT LCD Timing control signal.	Leave as a No Connect.	
LCD_LPCREVB	Connect to SEC TFT LCD Timing control signal.	Leave as a No Connect.	

Check Items	Recommendations		Checking
	Used	Unused	
Camera Interface			
CAMRESET	Connect to Camera Software Reset.	Leave as a No Connect.	
CAMCLKOUT	Connect to Camera Master Clock.	Leave as a No Connect.	
CAMPCLK	Connect to Camera Pixel Clock.	Leave as a No Connect.	
CAMHREF	Connect to Camera Horizontal Synchronous.	Leave as a No Connect.	
CAMVSYNC	Connect to Camera Vertical Synchronous.	Leave as a No Connect.	
CAMDATA [7:0]	Connect to Camera Pixel Data Lines.	Leave as a No Connect.	
Interrupt Control Unit			
EINT [23:0]	Connect to External Device Interrupt.	Leave as a No Connect.	
DMA			
nXDREQ[1:0]	Connect to External DMA Request.	Leave as a No Connect.	
nXDACK[1:0]	Connect to External DMA Acknowledge.	Leave as a No Connect.	
UART			
RxD[2:0]	Connect to UART Receives Data Lines.	Leave as a No Connect.	
TxD[2:0]	Connect to UART Transmits Data Lines.	Leave as a No Connect.	
nCTS[1:0]	Connect to UART Clear To Send.	Leave as a No Connect.	
nRTS[1:0]	Connect to UART Request To Send.	Leave as a No Connect.	
UARTCLK	Connect to UART Clock.	Leave as a No Connect.	
ADC			
AIN [7:0]	Connect to Analog signal.	Connect to GND.	
Vref	Connect to Analog Power 3.3V.	Connect to 3.3V.	
IIC-Bus			
IICSDA	Connect to IIC device Data. 1Kohm pull-up resistors to 3.3V.	Leave as a No Connect.	
IICSCL	Connect to IIC device Clock. 1Kohm pull-up resistors to 3.3V.	Leave as a No Connect.	
IIS-Bus			
I2SLRCK	Connect to CODEC Channel Clock.	Leave as a No Connect.	
I2SSDO	Connect to CODEC Data Input.	Leave as a No Connect.	
I2SSDI	Connect to CODEC Data Output.	Leave as a No Connect.	
I2SSCLK	Connect to CODEC Serial Clock.	Leave as a No Connect.	
CDCLK	Connect to CODEC System Clock.	Leave as a No Connect.	

Check Items	Recommendations		Checking
	Used	Unused	
Touch Screen			
nXPON	Connect to Touch Panel Plus X-axis on-off control.	Leave as a No Connect.	
XMON	Connect to Touch Panel Minus X-axis on-off control.	Leave as a No Connect.	
nYPON	Connect to Touch Panel Plus Y-axis on-off control.	Leave as a No Connect.	
YMON	Connect to Touch Panel Minus Y-axis on-off control.	Leave as a No Connect.	
USB Host			
DN [1:0]	Connect to USB Host Data Minus. Refer to USB Signal Routing.	Connect 15Kohm series resistors to GND.	
DP [1:0]	Connect to USB Host Data Plus. Refer to USB Signal Routing.	Connect 15Kohm series resistors to GND.	
USB Device			
PDN0	Connect to USB Device Data Minus. Refer to USB Signal Routing.	Connect 15Kohm series resistors to GND.	
PDP0	Connect to USB Device Data Plus. Refer to USB Signal Routing.	Connect 15Kohm series resistors to GND.	
SPI			
SPIMISO [1:0]	Connect to SPI device SPIMOSI.	Leave as a No Connect.	
SPIMOSI [1:0]	Connect to SPI device SPIMISO.	Leave as a No Connect.	
SPICLK [1:0]	Connect to SPI device Clock.	Leave as a No Connect.	
nSS [1:0]	Connect to SPI device Chip Select.	Leave as a No Connect.	
SD			
SDDAT [3:0]	Connect to SD Card Data Lines. 10Kohm pull-up resistors to 3.3V.	Leave as a No Connect.	
SDCMD	Connect to SD Card Command (Response). 10Kohm pull-up resistor to 3.3V.	Leave as a No Connect.	
SDCLK	Connect to SD Card Clock.	Leave as a No Connect.	
General Port			
GPn [116:0]	Connect to External Device.	Leave as a No Connect.	

Check Items	Recommendations		Checking
	Used	Unused	
Timer/PWM			
TOUT [3:0]	Connect to External Device Clock Input.	Leave as a No Connect.	
TCLK [1:0]	Connect to External Device Timer Clock Output.	Leave as a No Connect.	
JTAG Test Logic			
nTRST	Connect to JTAG Reset Port. 10Kohm pull-up resistors to 3.3V. Connect 470ohm series resistors to nRESET.	10Kohm pull-up resistors to 3.3V. Connect 470ohm series resistors to nRESET.	
TMS	Connect to JTAG Mode Select Port. 10Kohm pull-up resistors to 3.3V.	10Kohm pull-up resistors to 3.3V.	
TCK	Connect to JTAG Clock Port. 10Kohm pull-up resistors to 3.3V.	10Kohm pull-up resistors to 3.3V.	
TDI	Connect to JTAG Data Output Port. 10Kohm pull-up resistors to 3.3V.	10Kohm pull-up resistors to 3.3V.	
TDO	Connect to JTAG Data Input Port.	Leave as a No Connect.	
Clock			
OM [3:2]	4.7Kohm pull-up resistors to 3.3V and Connect to GND. Refer to in Table 2-3.	4.7Kohm pull-up resistors to 3.3V and Connect to GND. Refer to in Table 2-3.	
XTOpll XTIpll	Connect a 15 ~ 22pF capacitor from each signal to GND. Connect to 10 ~ 20MHz crystal oscillator.	XTOpll leave as a No Connect. XTIpll connect to High (3.3V).	
XTOrtc XTIrtc	Connect a 15 ~ 22pF capacitor from each signal to GND. Connect to crystal oscillator.	XTOrtc leave as a No Connect. XTIrtc connect to RTCVDD (3.3V).	
EXTCLK	Connect to External Clock Source (Oscillator).	Connect to High (3.3V).	
CLKOUT [1:0]	Connect to External device Clock Input.	Leave as a No Connect.	
MPLLCAP	Connect a 2.8nF capacitor to GND.	Connect a 2.8nF capacitor to GND.	
UPLLCAP	Connect a 700pF capacitor to GND.	Connect a 700pF capacitor to GND.	

Check Items	Recommendations		Checking
	Used	Unused	
Reset			
nRESET	Connect to Reset Circuit or Reset Button.	Connect to Reset Circuit or Reset Button.	
nRSTOUT	Connect to External Device Reset	Leave as a No Connect.	
PWREN	Connect to Core Power On/Off Control Signal.	Leave as a No Connect.	
nBATT_FLT	Connect to Probe Signal for Battery State.	Connect to High (3.3V).	
Power			
VDDalive	Connect to 1.2V Power Plane. It should be always supplied whether in Normal Mode or in Sleep Mode.	Connect to 1.2V Power Plane.	
VDDi/VDDiarm	Connect to 1.2V Power Plane.	Connect to 1.2V Power Plane.	
VSSi/VSSiarm	Connect to GND Plane.	Connect to GND Plane.	
VDDi_MPLL	Connect to 1.2V Power Plane.	Connect to 1.2V Power Plane.	
VSSi_MPLL	Connect to GND Plane.	Connect to GND Plane.	
VDDOP	Connect to 3.3V Power Plane.	Connect to 3.3V Power Plane.	
VDDMOP	Connect to 3.3V Power Plane (up to 100MHz). Connect to 2.5V Power Plane (up to 80MHz).	Connect to 3.3V Power Plane.	
VSSOP	Connect to GND Plane.	Connect to GND Plane.	
RTCVDD	Connect to 3.0V RTC Battery.	Connect to 3.3V Power Plane.	
VDDi_UPLL	Connect to 1.2V Power Plane.	Connect to 1.2V Power Plane.	
VSSi_UPLL	Connect to GND Plane.	Connect to GND Plane.	
VDDA_ADC	Connect to 3.3V Analog Power Plane.	Connect to 3.3V Analog Power Plane.	
VSSA_ADC	Connect to Analog GND Plane.	Connect to Analog GND Plane.	

9 SMDK2440 SCHEMATIC AND PART LIST

1. OVERVIEW

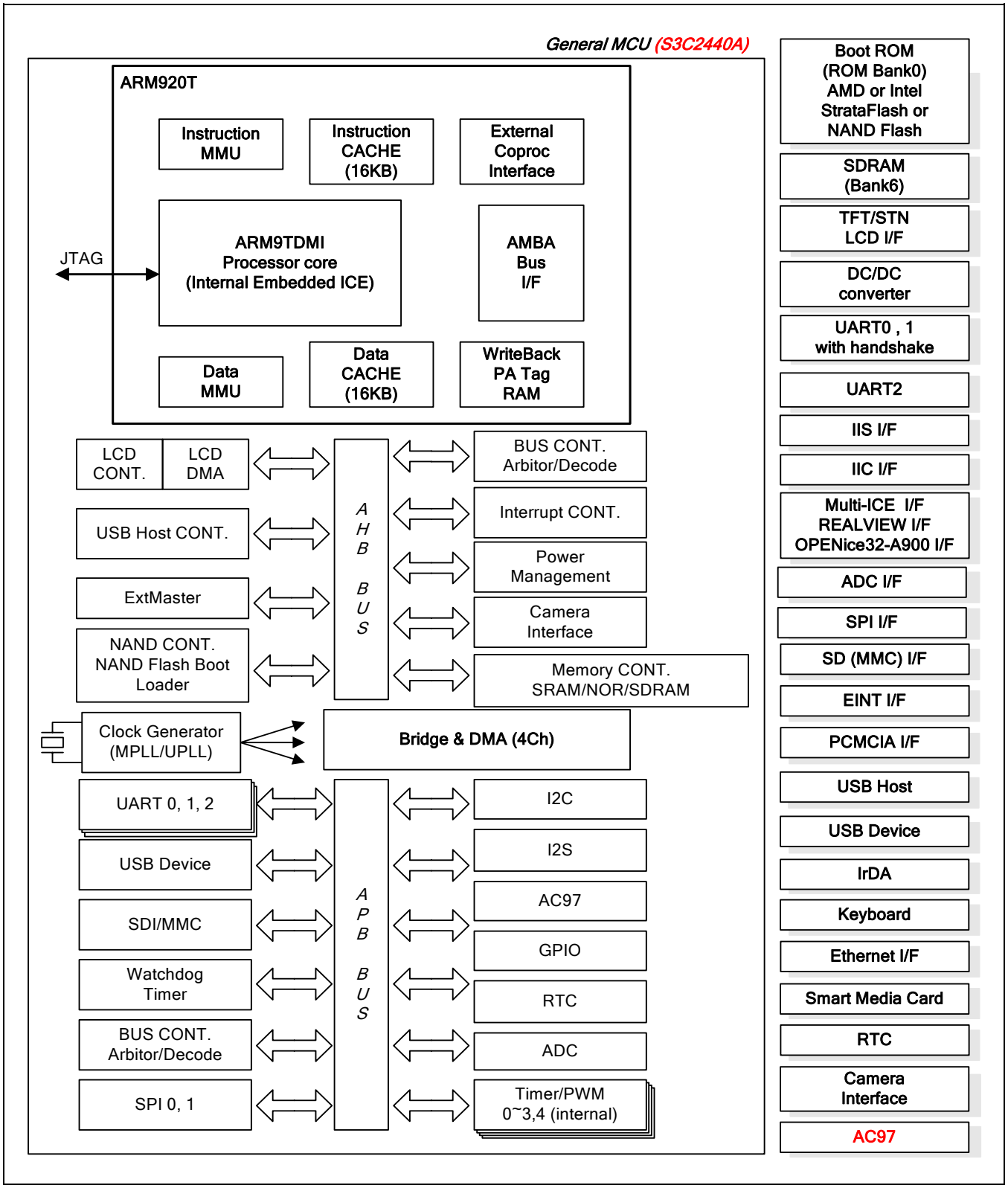
The SMDK2440 (S3C2440 Development Kit) shows the basic system-based hardware design that uses the S3C2440A. It can evaluate the basic operations of the S3C2440A and develop codes for it as well.

SMDK2440 is manufactured by MERITECH Co., Ltd and its website is www.mcukorea.com

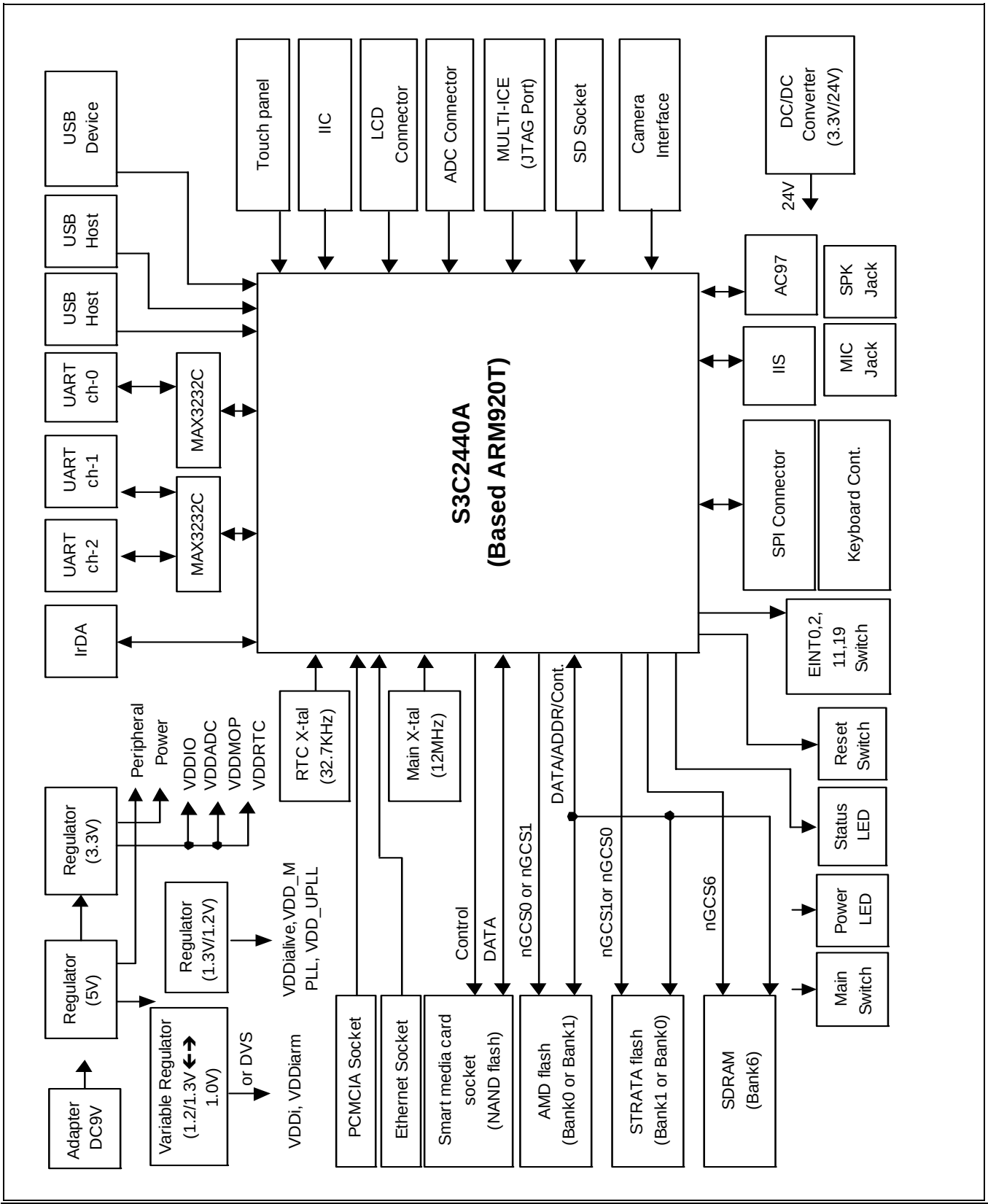
When the S3C2440A is contained in the SMDK2440, you can use an in-circuit emulator (MULTI-ICE/REALVIEW-ICE (RVI)/OPENice32-A900).

This allows you to test and debug a system design at the processor level. In addition, the S3C2440A with MULTI-ICE/ REALVIEW-ICE (RVI)/OPENice32-A900 capability can be debugged directly using the MULTI-ICE/ REALVIEW-ICE (RVI)/OPENice32-A900 interface.

2. SMDK2440 Function Block Diagram



2. Detailed SMDK2440 Board Diagram



3. SMDK2440 Schematic Diagram (Revision History)

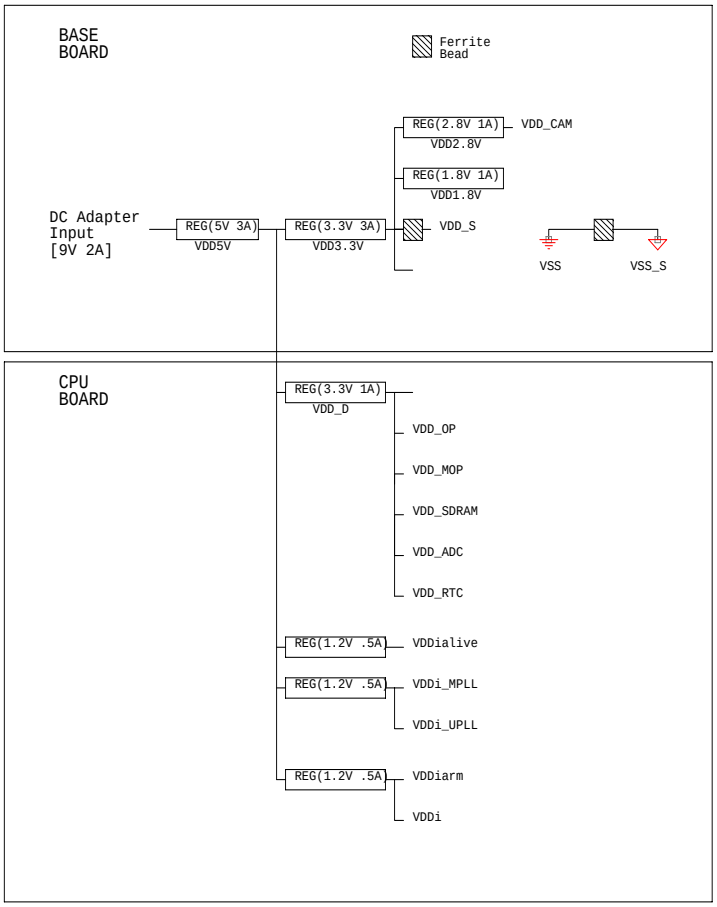
SMDK2440 Board (S3C2440X Evaluation Board)

PCB Revision	Date	Description
Ver : 0.17	Sep. 29, 2003	First preliminary version on samsung web site..
Ver : 0.18	Jan. 26, 2004	1. Modified the power supply circuit for using DVS mode. 2. Changed U11 pin of S3C2440A from VDDiarm to VDDi. 3. Changed PLL clock input from 12MHz to 16.9344MHz for using IIS exactly. 4. Added the AC'97 codec circuit. 5. Modified the camera interface circuit to use SAMSUNG Camera(s5x532) Module.
Ver : 0.19	Mar. 5, 2004	1. VDDalive power block was seperated from VDDi,pll. 2. Modified AC'97 codec circuit 3. Added USB detecting control circuit
Ver : 1.0	Jun. 28, 2004	1. VDDalive = 1.2V 2. VDDi, VDDiarm are connected with equal power source. 3. Modified the microphone jack circuit.

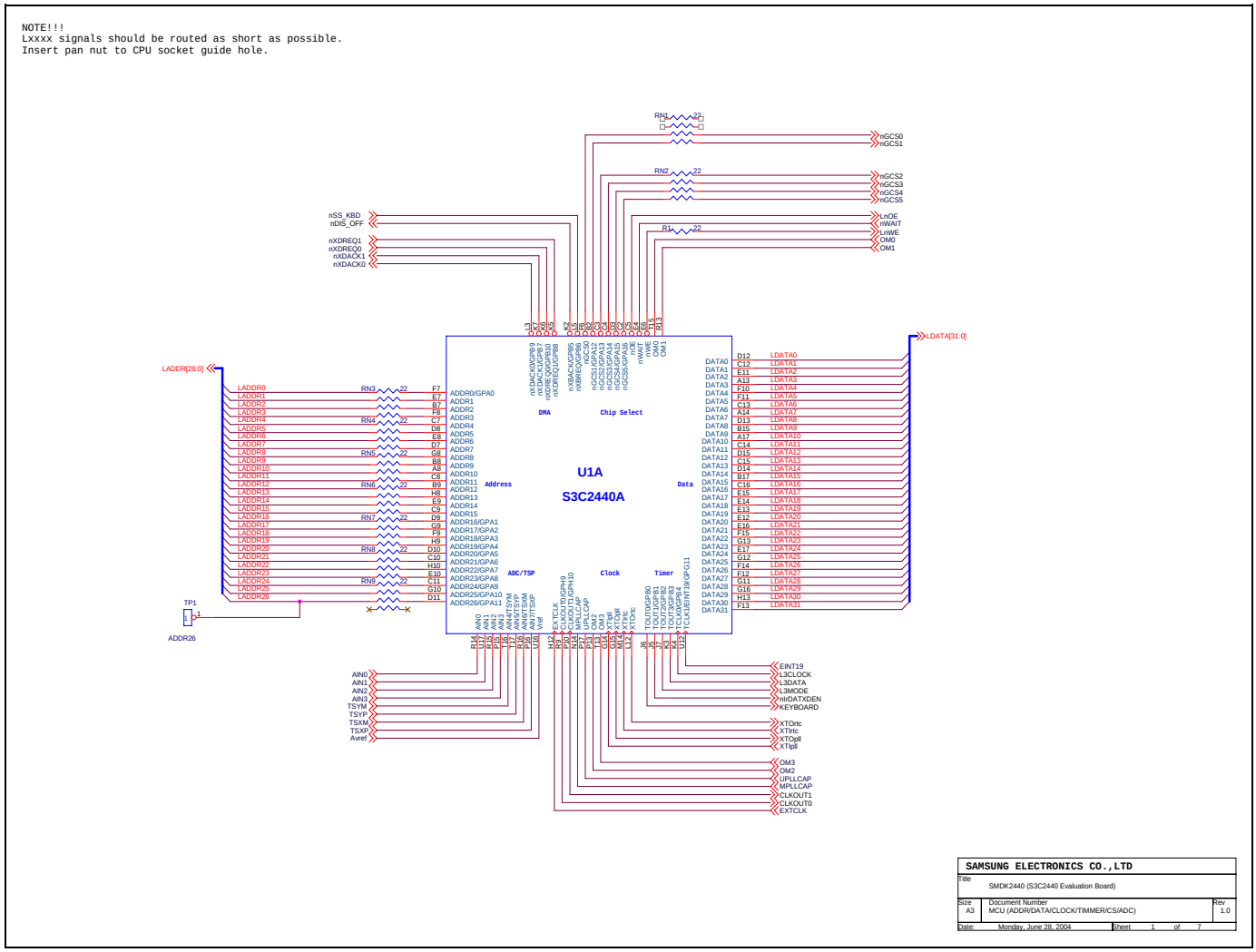
3. SMDK2440 Schematic Diagram (Table of Contents)

Table of contents

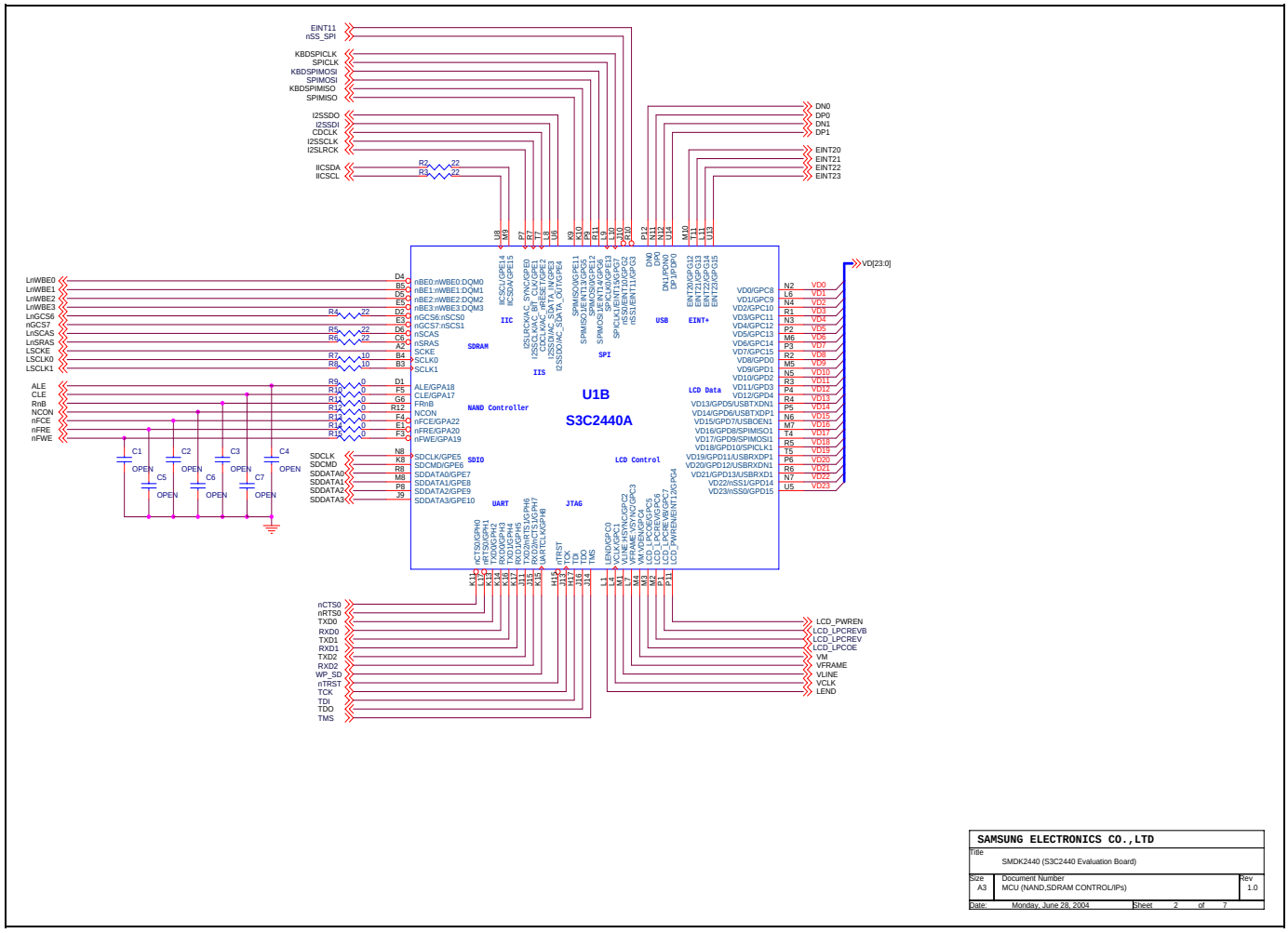
Diagram of power supply



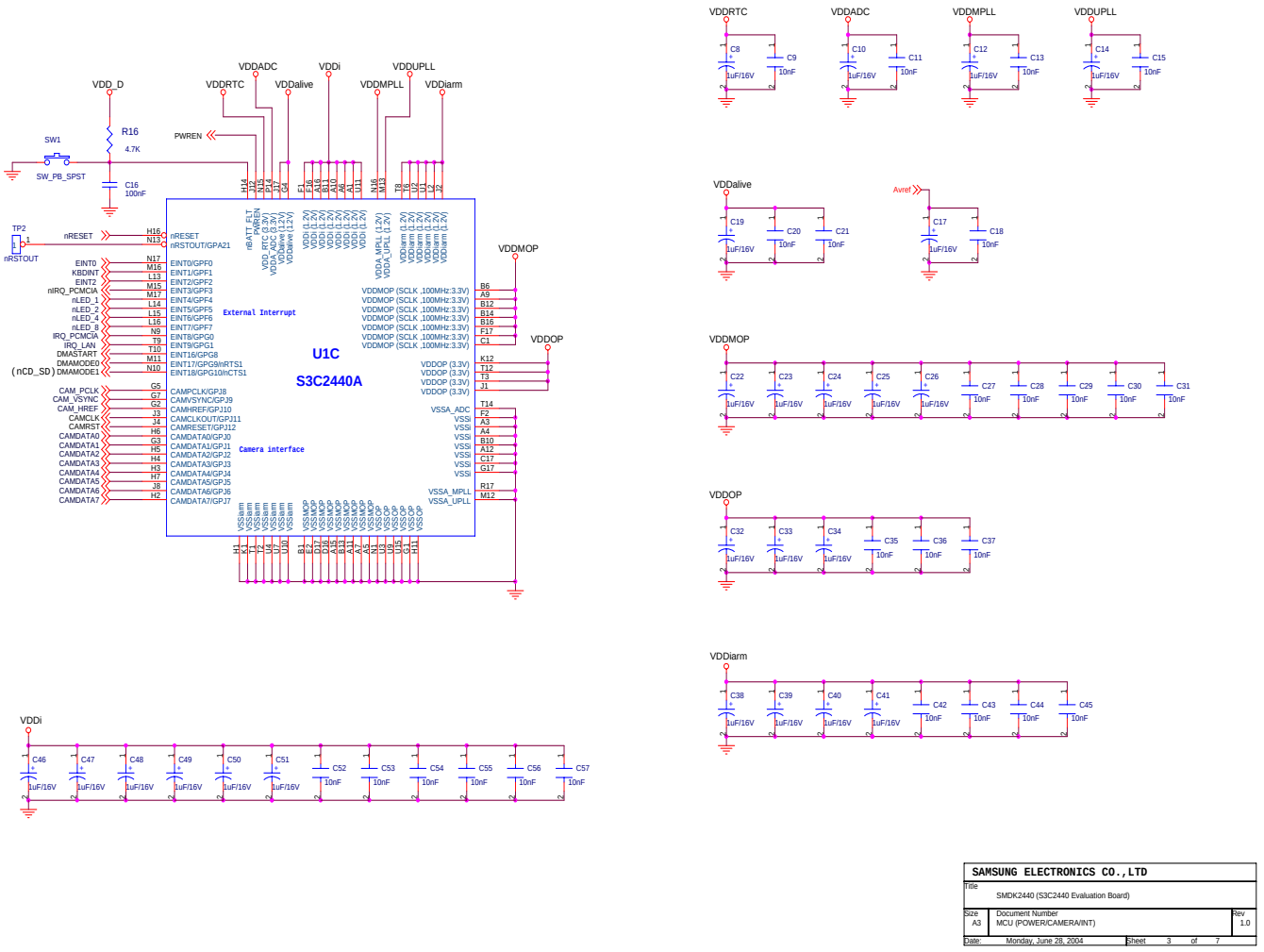
3. SMDK2440 Schematic Diagram (CPU Board) - Sheet 1 of 7



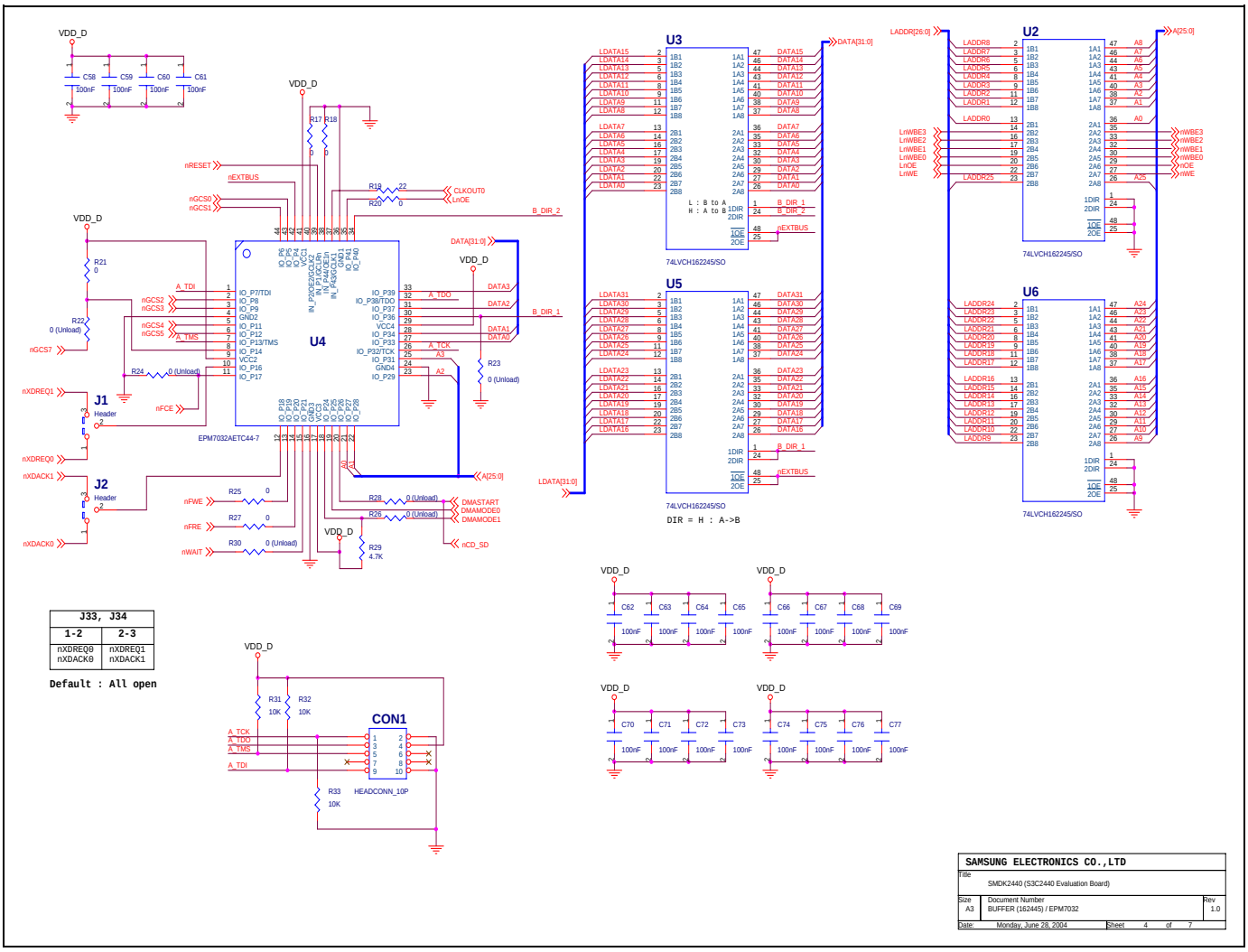
3. SMDK2440 Schematic Diagram (CPU Board) - Sheet 2 of 7



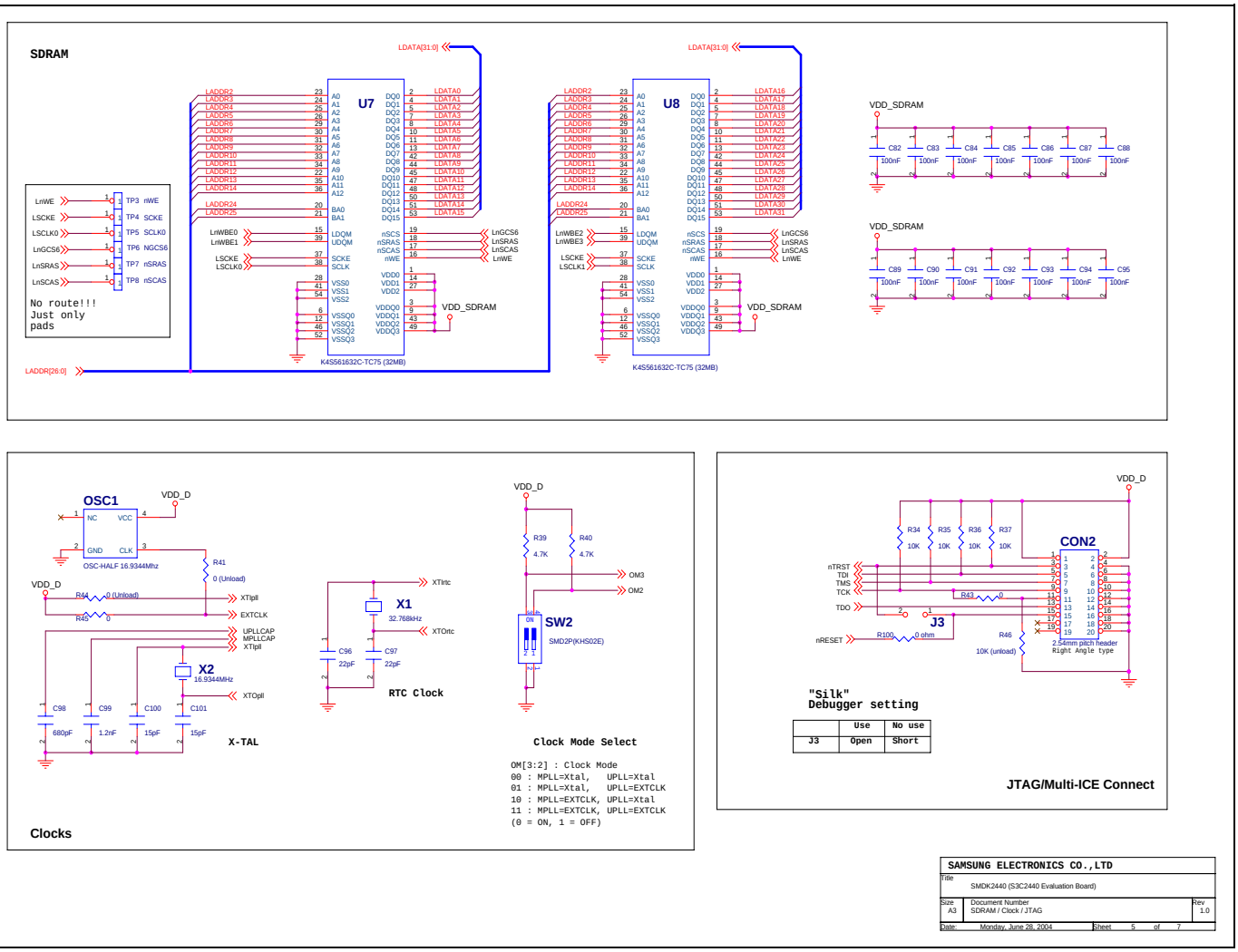
3. SMDK2440 Schematic Diagram (CPU Board) - Sheet 3 of 7



3. SMDK2440 Schematic Diagram (CPU Board) - Sheet 4 of 7

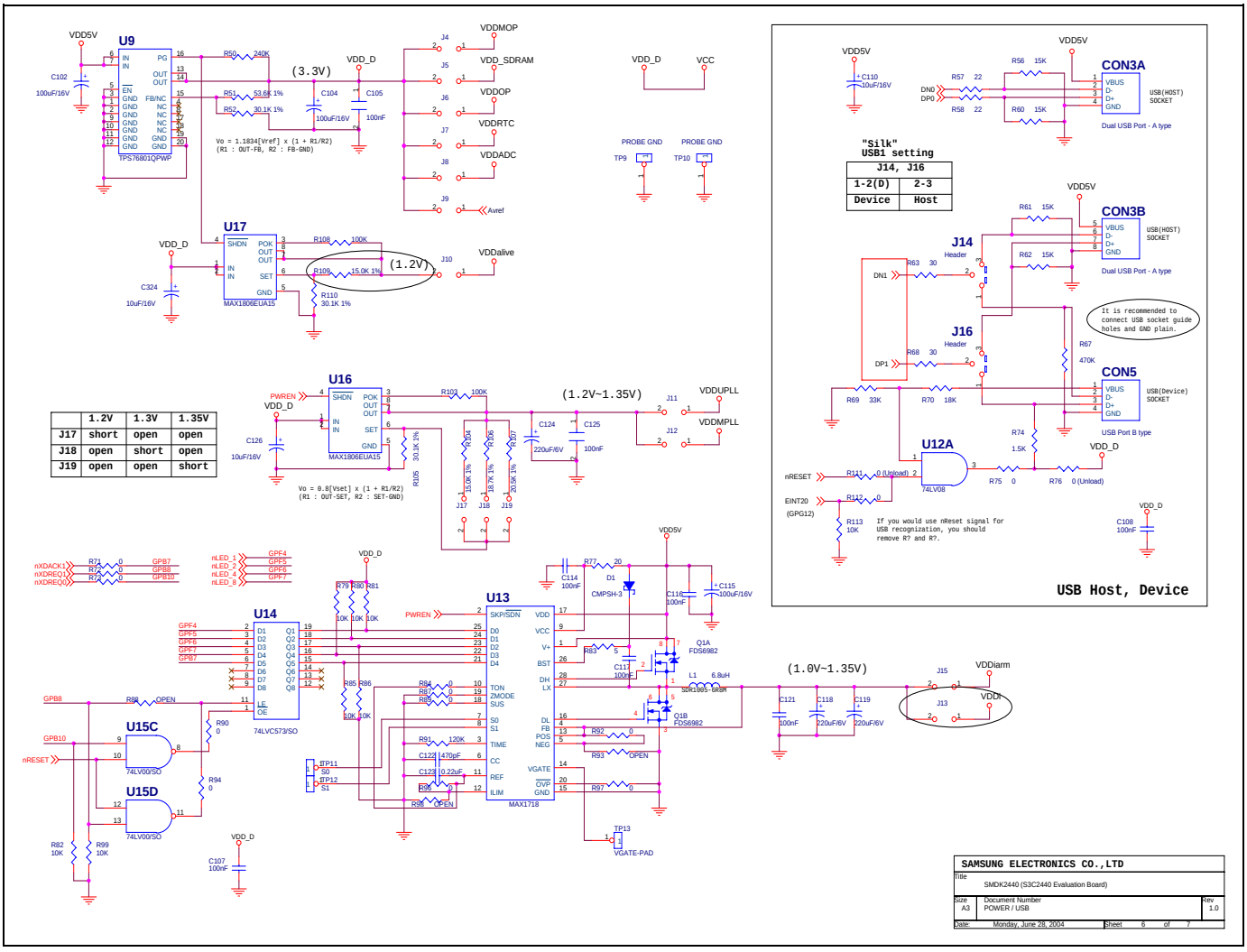


3. SMDK2440 Schematic Diagram (CPU Board) - Sheet 5 of 7

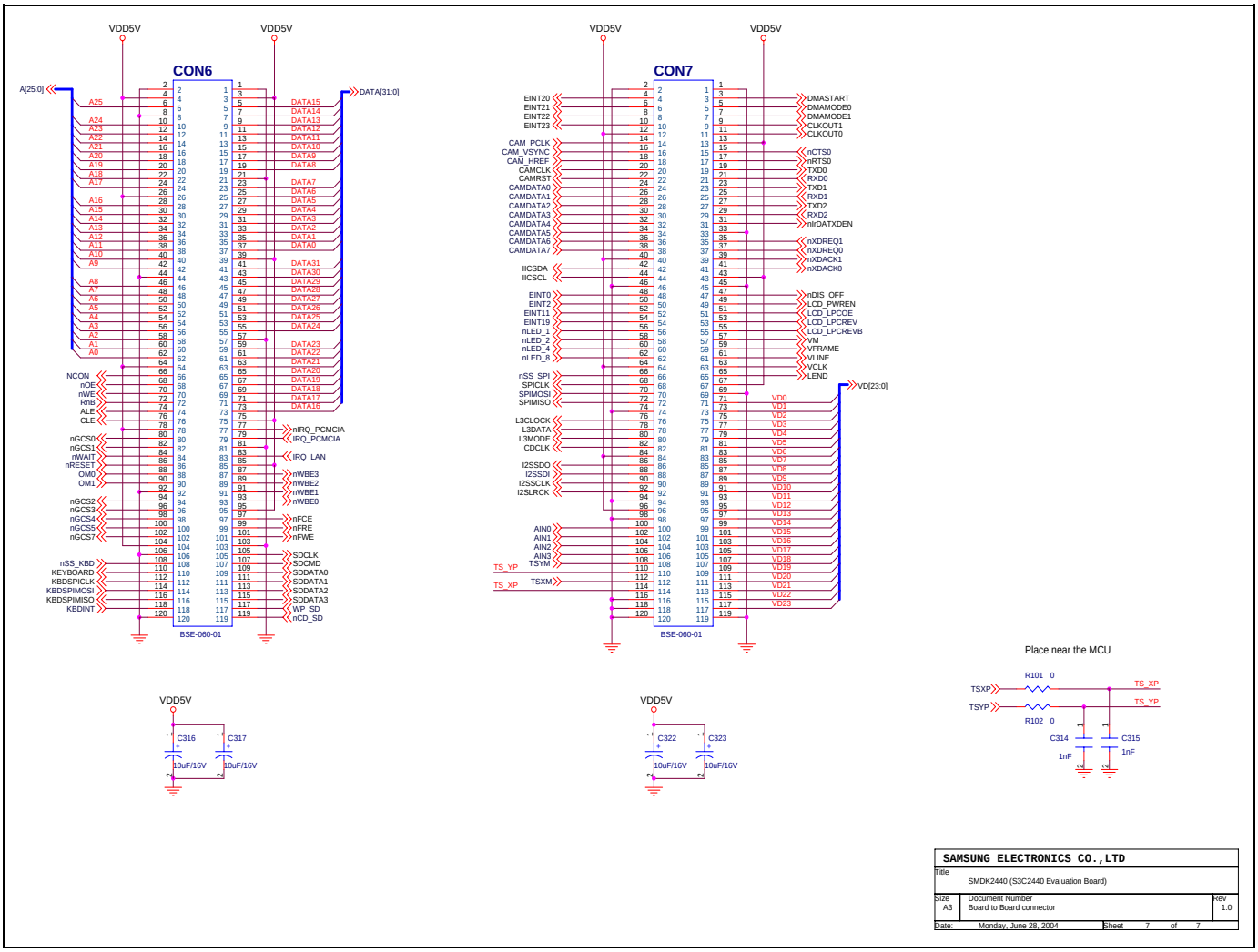


	Use	No use
J3	Open	Short

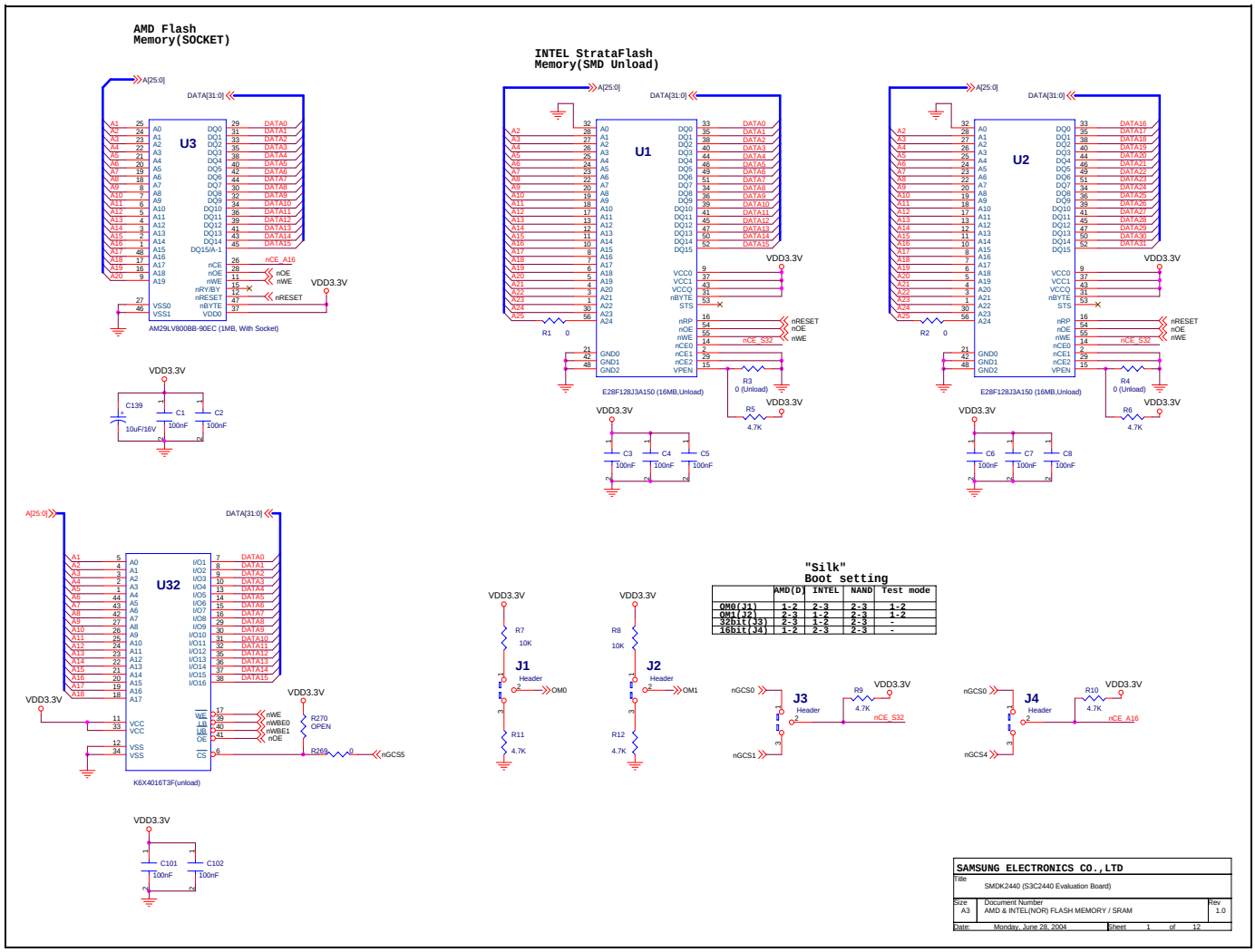
3. SMDK2440 Schematic Diagram (CPU Board) - Sheet 6 of 7



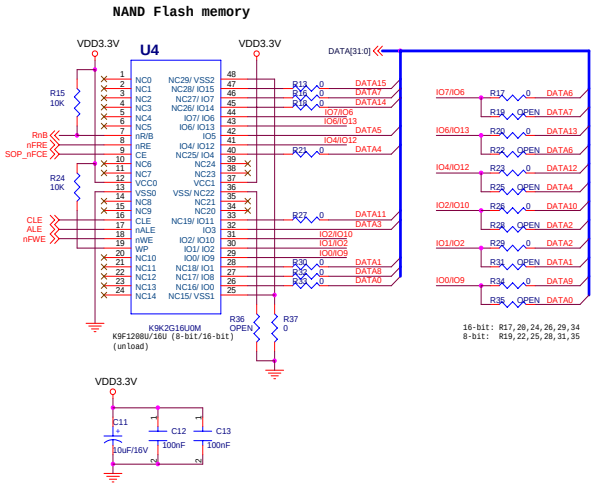
3. SMDK2440 Schematic Diagram (CPU Board) - Sheet 7 of 7

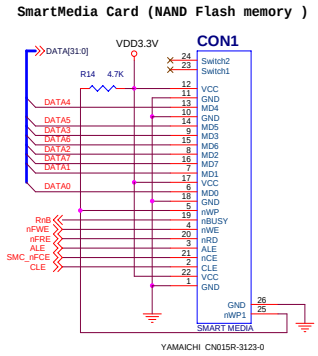


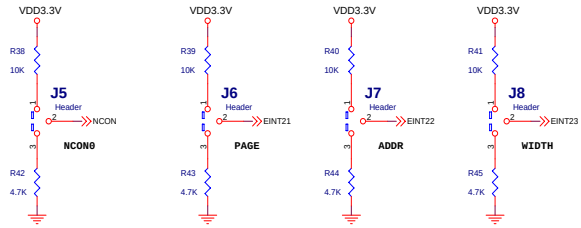
3. SMDK2440 Schematic Diagram (Base Board) - Sheet 1 of 12



3. SMDK2440 Schematic Diagram (Base Board) - Sheet 2 of 12







"Silk"
NAND setting

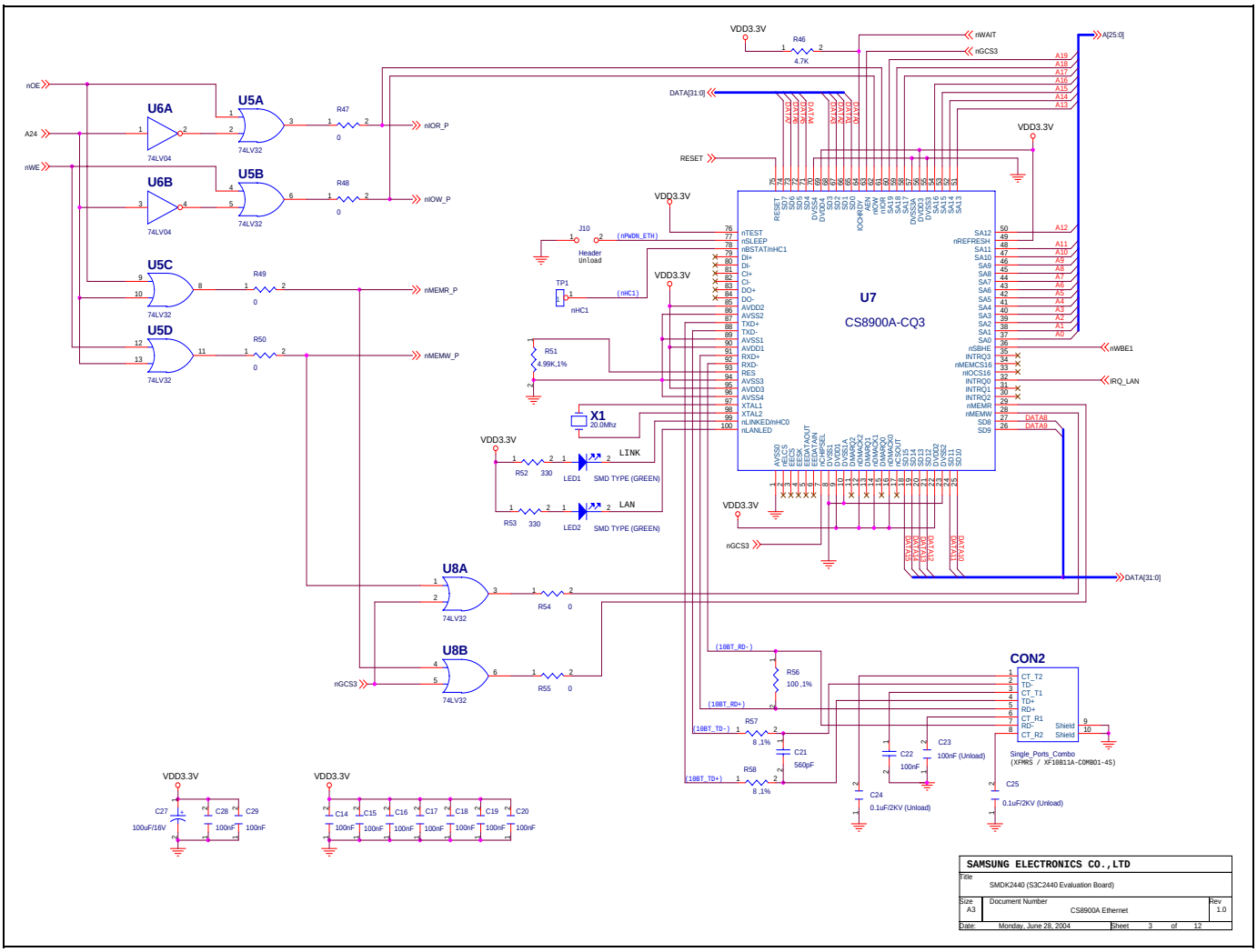
When OM[1:0]=2-3 (NAND boot)			
NCON0(J5)		Normal(2-3)(D)	Advanced(1-2)
PAGE	2-3	256	1024
(J6)	1-2	512(D)	2048
ADDR	2-3	3 cycle	4 cycle
(J7)	1-2	4 cycle(D)	5 cycle
WIDTH	2-3	8-bit bus(D)	
(J8)	1-2	16-bit bus	
NAND	2-3	SMC enable(D)	
(J9)	1-2	SOP enable	

Setting Example

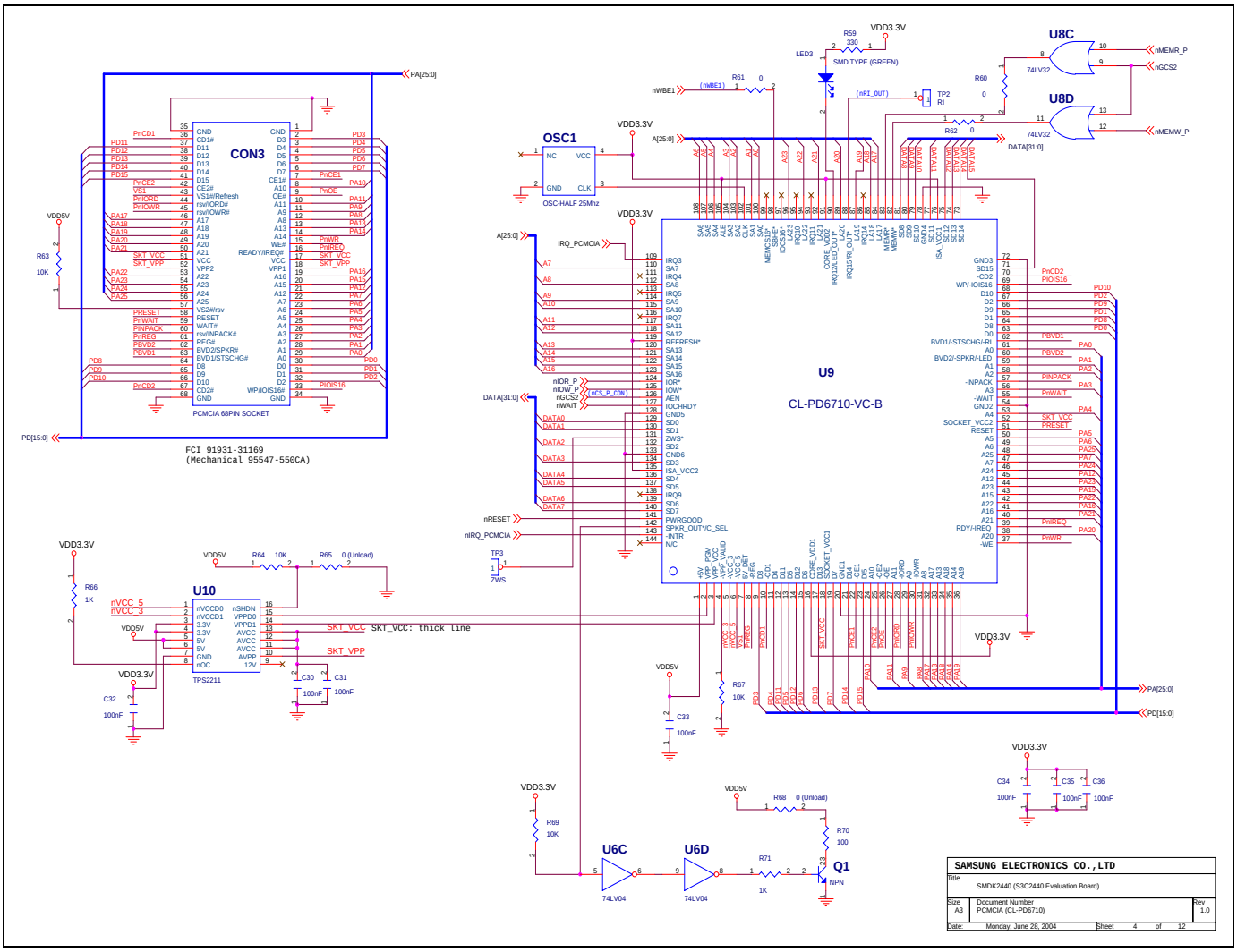
	SMC(K9S1208V0M)	K9K2G16U0M
J5	2-3	1-2
J6	1-2	2-3
J7	1-2	1-2
J8	2-3	1-2
J9	2-3	1-2

SAMSUNG ELECTRONICS CO.,LTD			
Title: SMDK2440 (S3C2440 Evaluation Board)			
Size: A3	Document Number: NAND(SAMSUNG) FLASH MEMORY		Rev: 1.0
Date: Monday, June 28, 2004	Sheet 2 of 12		

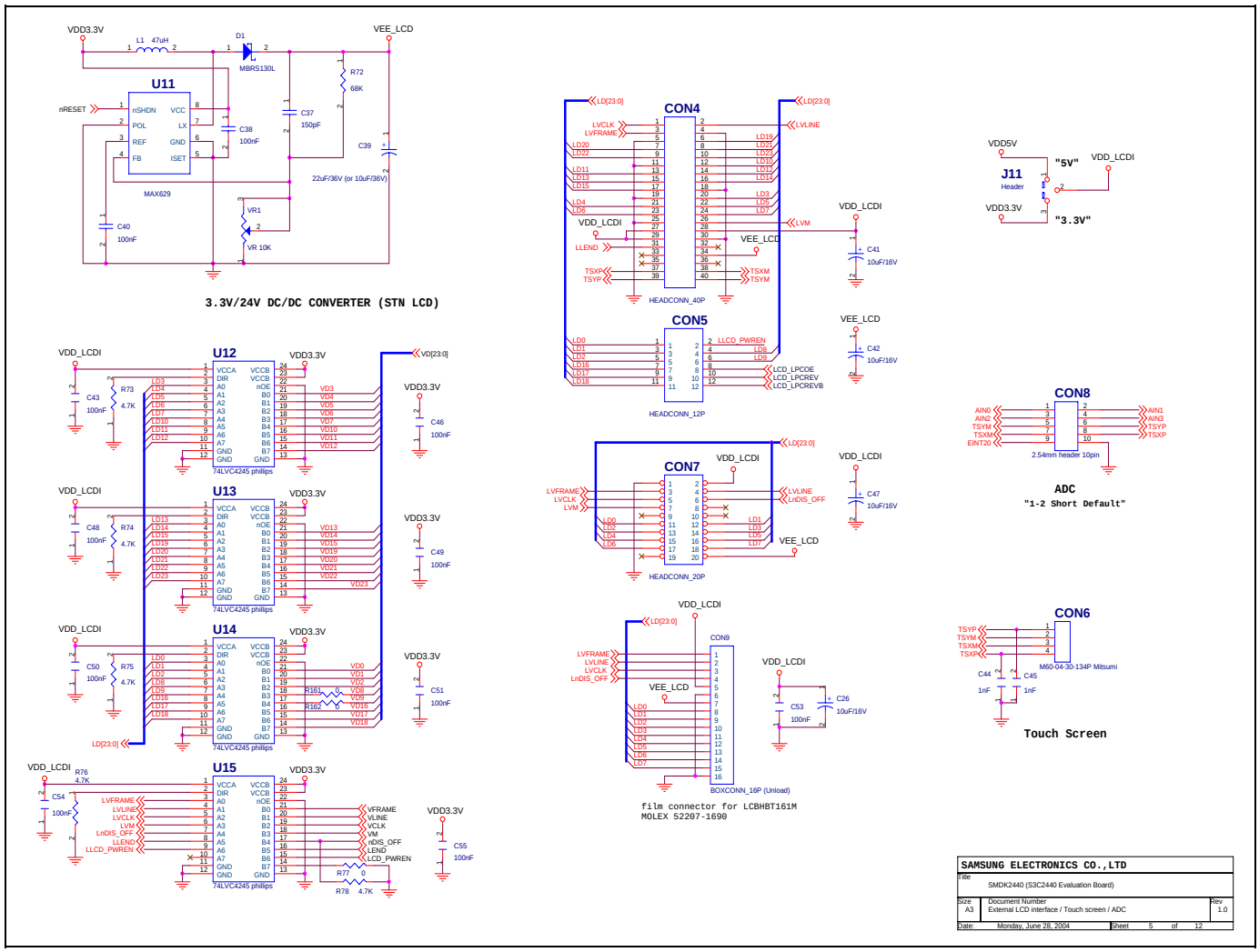
3. SMDK2440 Schematic Diagram (Base Board) - Sheet 3 of 12



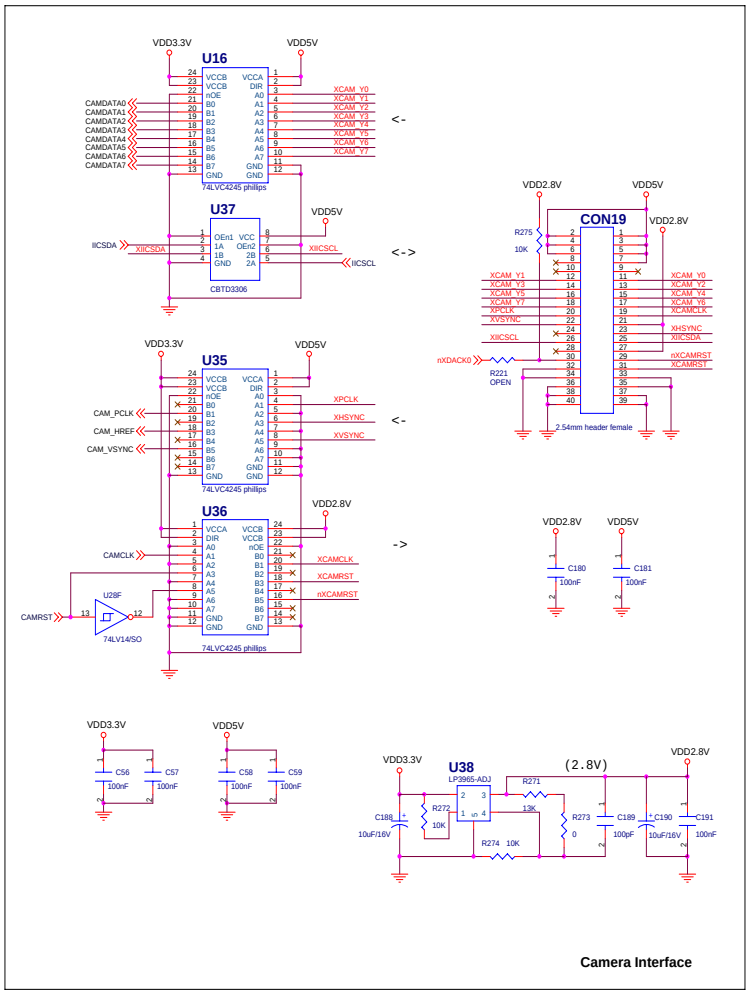
3. SMDK2440 Schematic Diagram (Base Board) - Sheet 4 of 12

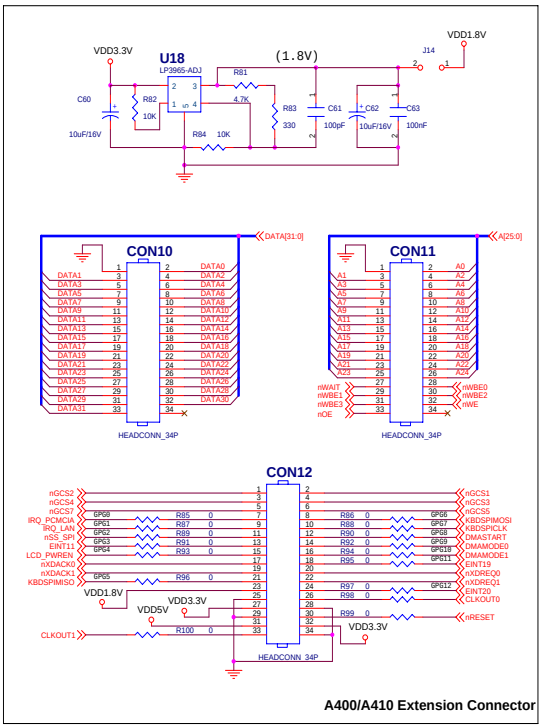


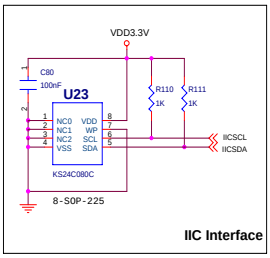
3. SMDK2440 Schematic Diagram (Base Board) - Sheet 5 of 12



3. SMDK2440 Schematic Diagram (Base Board) - Sheet 6 of 12







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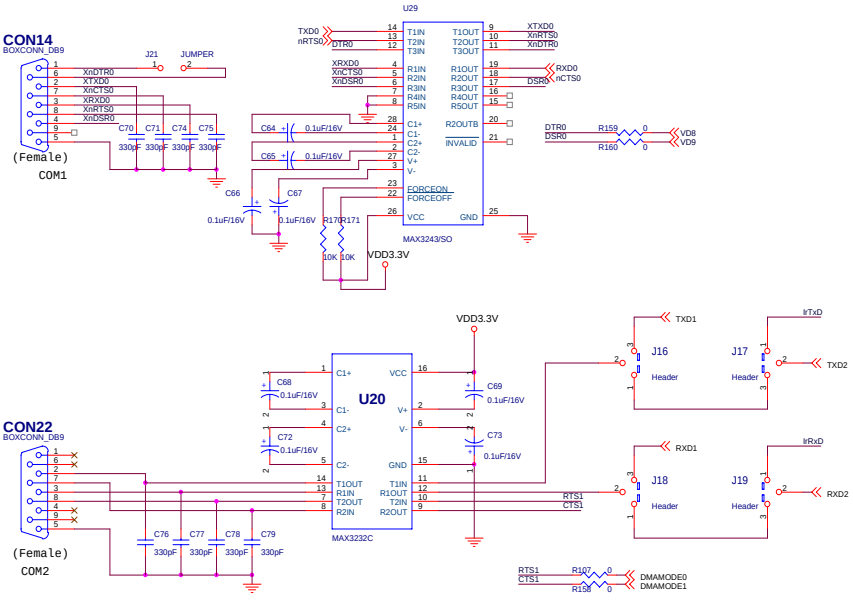
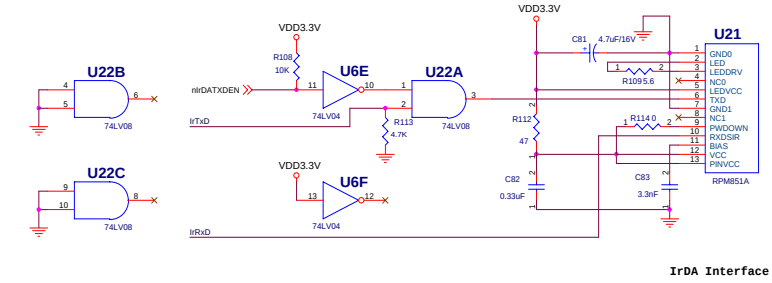
Size: A3	Document Number: Camera / Extension Connector / IIC	Rev: 1.0
Date: Monday, June 28, 2004	Sheet 6 of 12	

3. SMDK2440 Schematic Diagram (Base Board) - Sheet 7 of 12



UART Interface



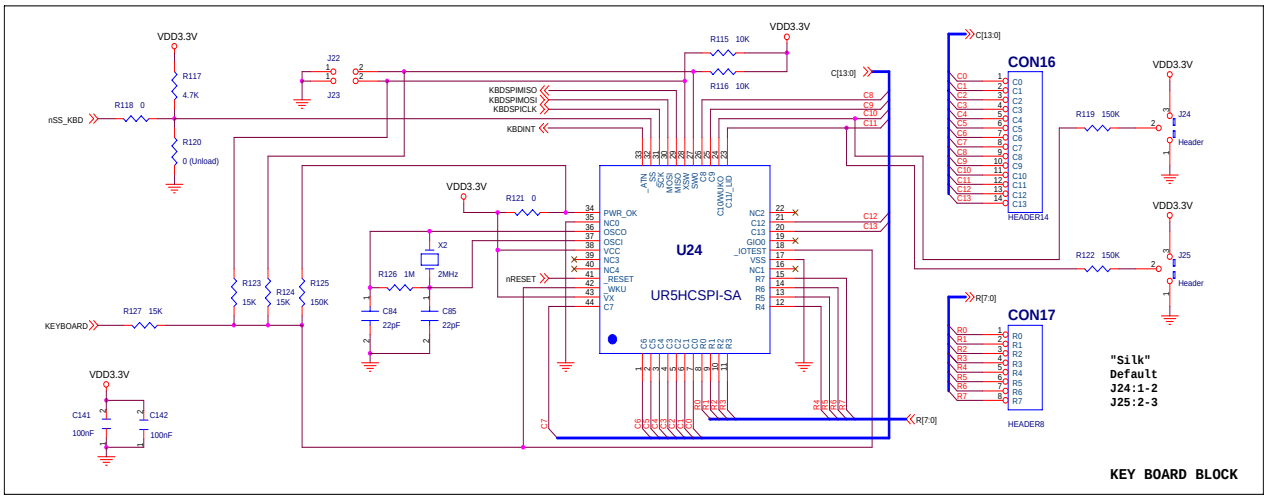
IrDA Interface

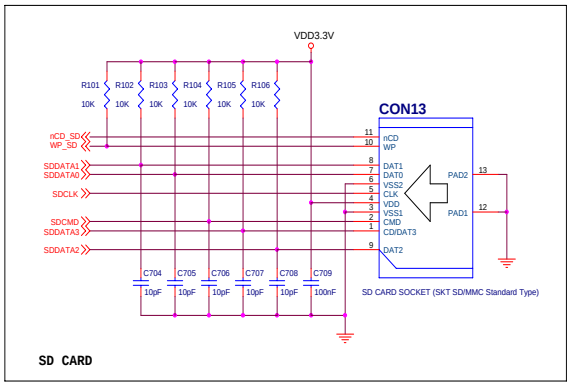
"Silk"

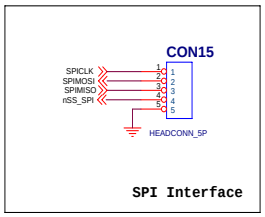
SIO 9P	J16,J18	J17,J19
COM2 UART1	2-3(D)	-
COM2 UART2	1-2	2-3
IrDA	-	1-2

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2440 (S3C2440 Evaluation Board)		
Size: A3	Document Number: UART / IrDA	Rev: 1.0
Date: Monday, June 28, 2004	Sheet 7 of 12	

3. SMDK2440 Schematic Diagram (Base Board) - Sheet 8 of 12

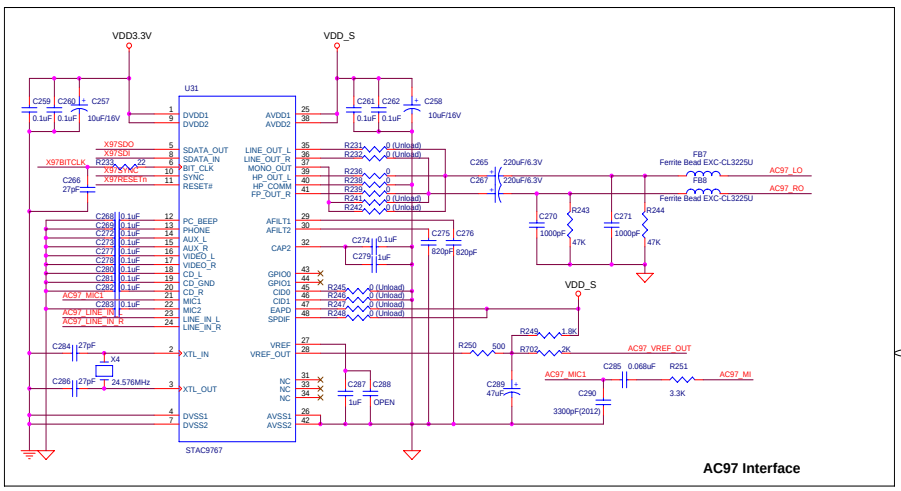


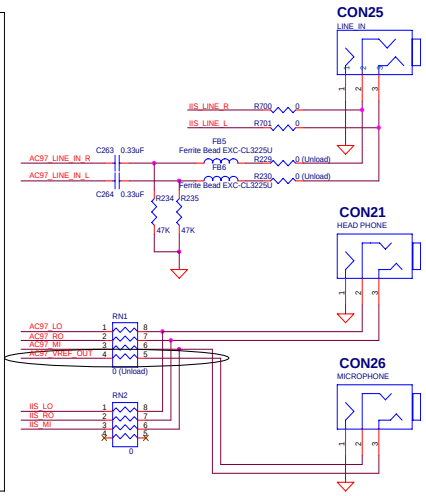




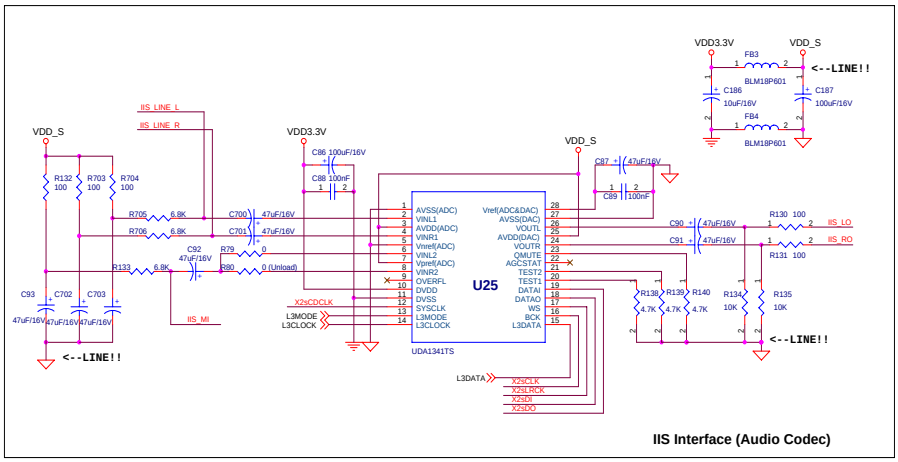
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2440 (S3C2440 Evaluation Board)		
Size: A3	Document Number: KEYBOARD / SPI / SDI	Rev: 1.0
Date: Monday, June 28, 2004	Sheet 8 of 12	

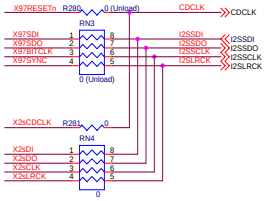
3. SMDK2440 Schematic Diagram (Base Board) - Sheet 9 of 12





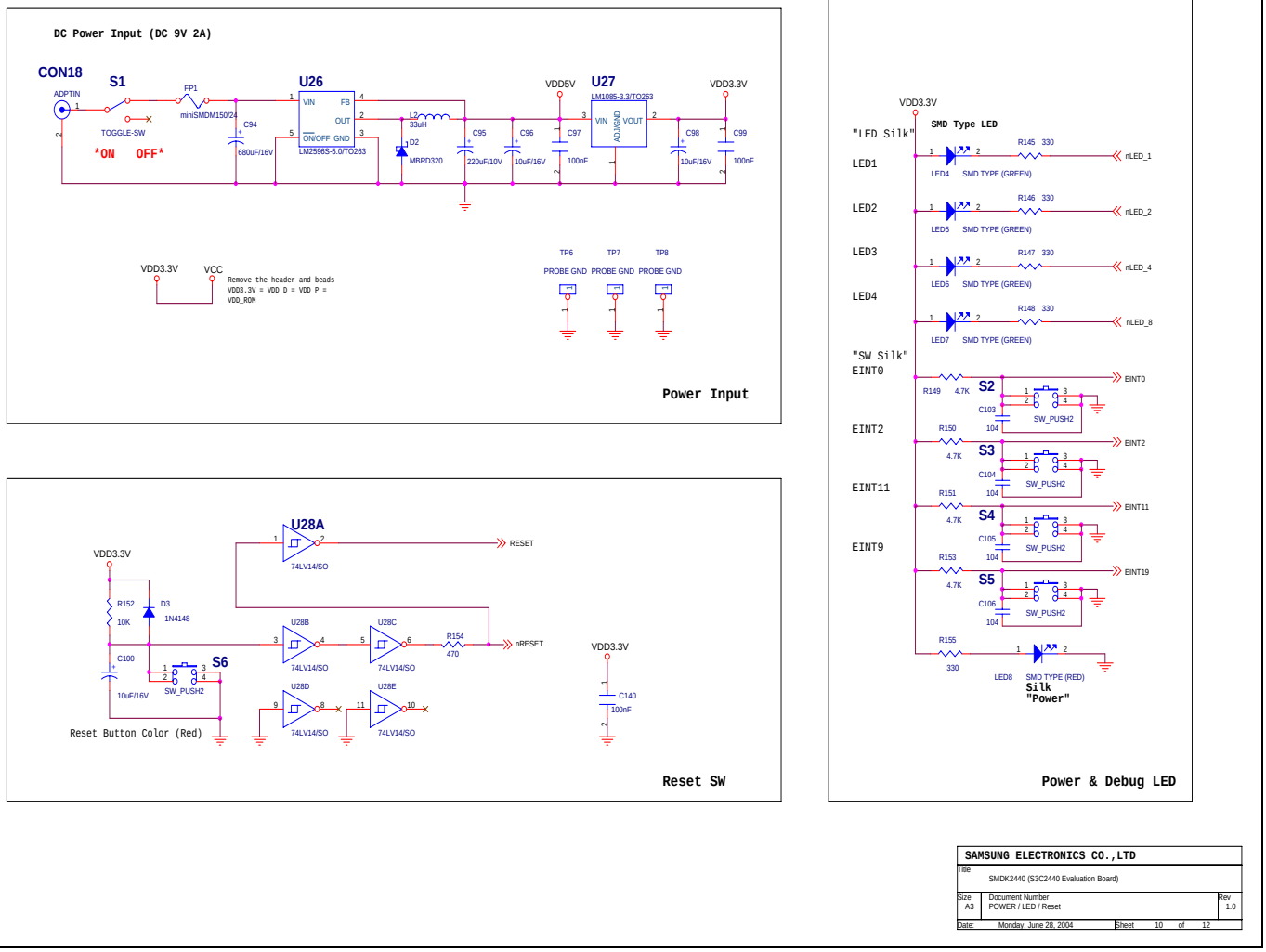
	AC'97	IIS
RN1, RN3, R280 R229, R230	SHORT	OPEN
RN2, RN4, R281 R700, R701	OPEN	SHORT



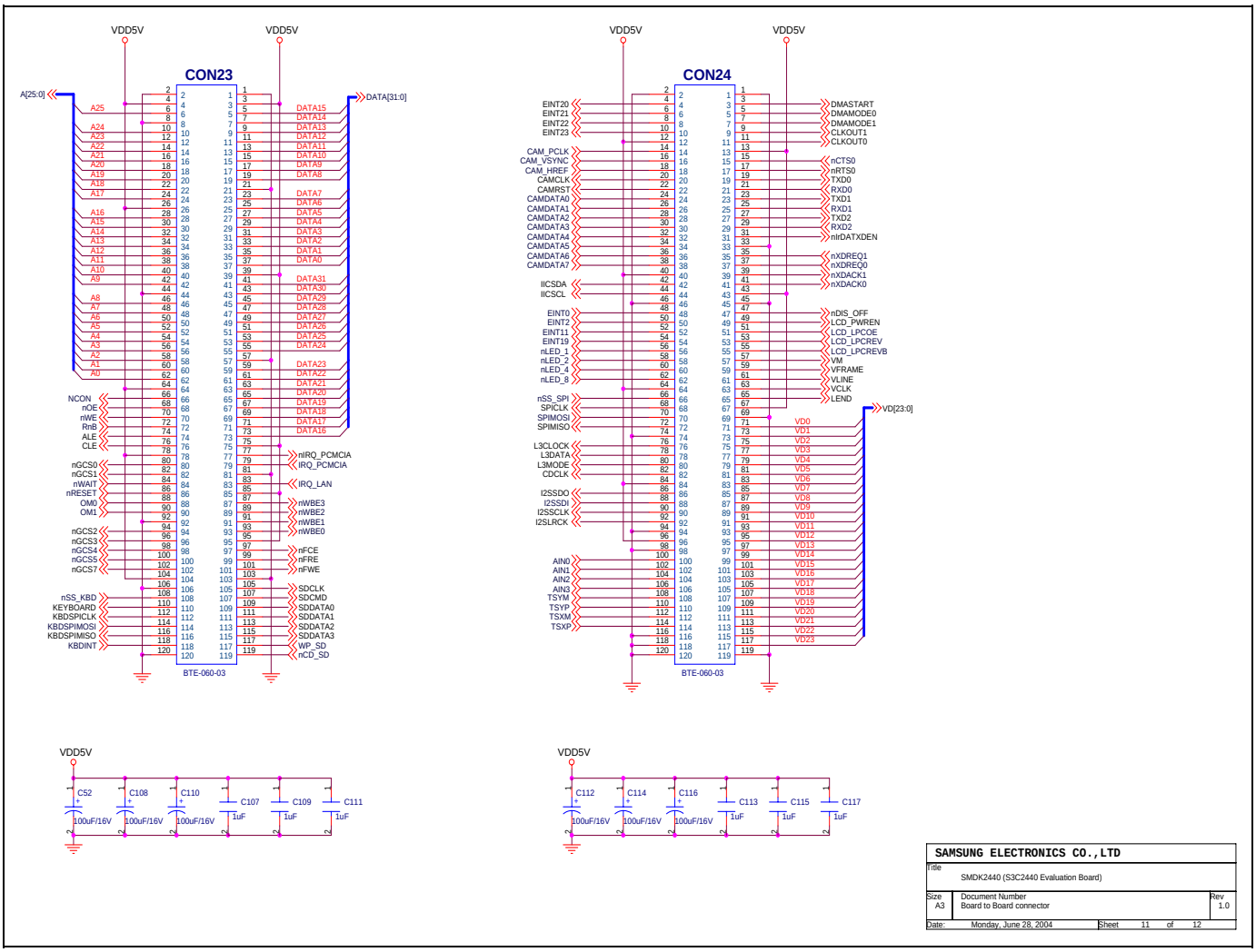


SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2440 (S3C2440 Evaluation Board)		
Size: A3	Document Number: AC97 / IIS (AUDIO)	Rev: 1.0
Date: Monday, June 28, 2004	Sheet 9 of 12	

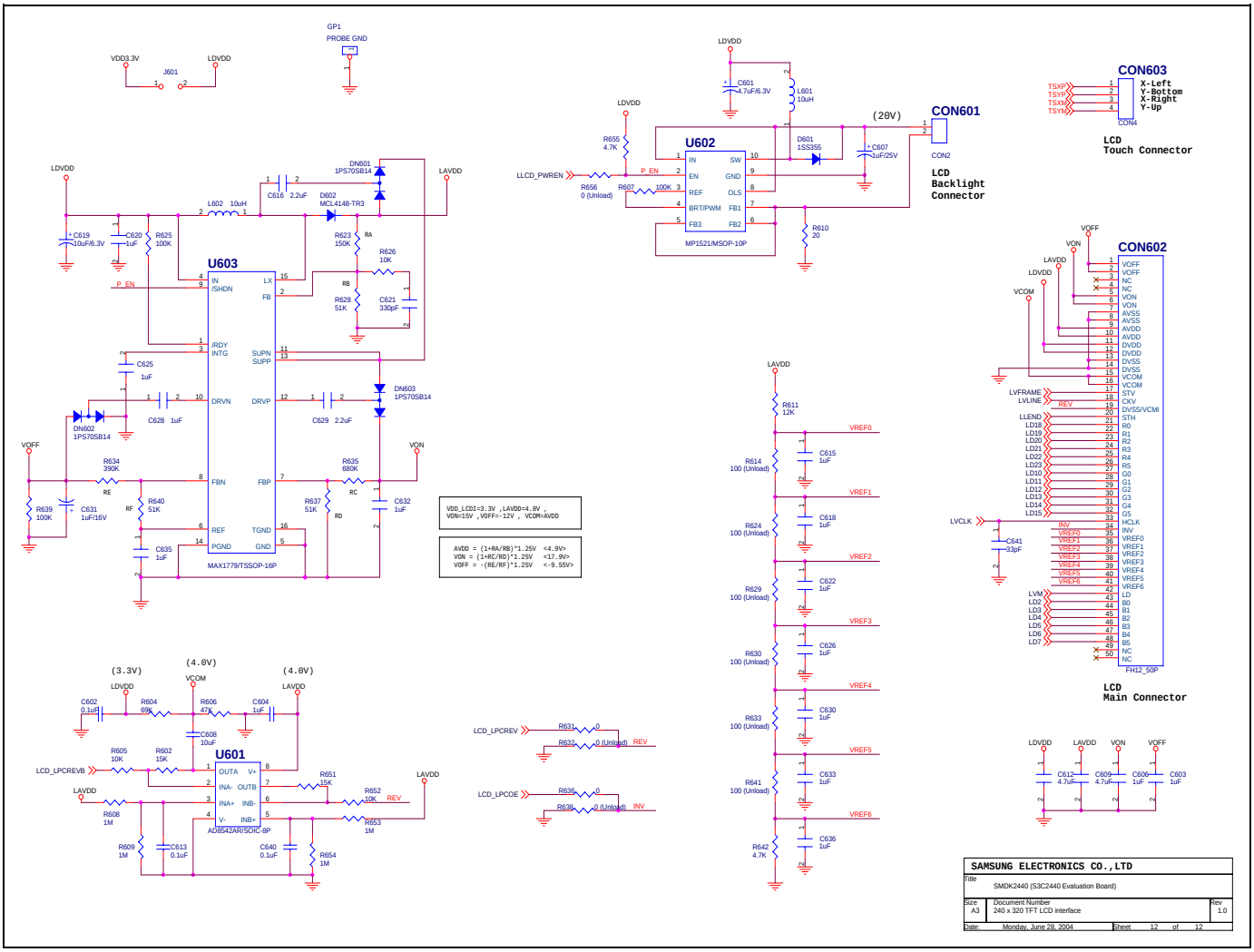
3. SMDK2440 Schematic Diagram (Base Board) - Sheet 10 of 12



3. SMDK2440 Schematic Diagram (Base Board) - Sheet 11 of 12



3. SMDK2440 Schematic Diagram (Base Board) - Sheet 12 of 12



4. SMDK2440 Part List (CPU Board) - Sheet 1 of 4

	ITEMS	DESCRIPTION	LOCATION	QTY
1	PROCESSOR	MCU S3C2440 (289BGA)	U1	1
2	CERAMIC CAP	SMD 1.2nF 1608	C99	1
3	CERAMIC CAP	SMD 100nF 1608	C16,C58~C77,C82~C95,C105,C107,C108,C114,C116,C117,C121,C125	43
4	CERAMIC CAP	SMD 10nF 1608	C9,C11,C13,C15,C18,C20,C21,C27~C31,C35~C37,C42~C45,C52~C57	26
5	CERAMIC CAP	SMD 15pF 1608	C100,C101	2
6	CERAMIC CAP	SMD 1nF 1608	C314,C315	2
7	CERAMIC CAP	SMD 220nF 1608	C123	1
8	CERAMIC CAP	SMD 22pF 1608	C97,C96	2
9	CERAMIC CAP	SMD 470pF 1608	C122	1
10	CERAMIC CAP	SMD 680pF 1608	C98	1
11	CONNECTOR	BSE-060-03-L-D-A	CON6,CON7	2
12	CONNECTOR HEADER	JTAG 3F-20PA(L) RIGHT ANGLE	CON2	1
13	CONNECTOR HEADER	MALE PIN 1x2	J3~J13,J15,J17~J19	15
14	CONNECTOR HEADER	MALE PIN 1x3	J1,J2,J14,J16	4
15	CONNECTOR HEADER	MALE PIN 2x5	CON1	1
16	DIODE	SMD Schottky Diode CMPSH-3 (SOT23)	D1	1
17	FET	SMD FET FDS6982 (SOP8)	Q1	1
18	IC	20V N-Channel Power Trench MOSFET FDS6574A(SOP8)	U11	1
19	IC	Octal D-type transparent latch with 5v tolerant inputs/outputs; 3state 74LVC573 (SSOP2-20)	U14	1
20	IC	MAX 7000A Programmable Logic Device EPM7032AE TC44-7	U4	1

4. SMDK2440 Part List (CPU Board) - Sheet 2 of 4

	ITEMS	DESCRIPTION	LOCATION	QTY
21	IC BUS TRANSCEIVER	3.3V CMOS 16-BIT BUS TRANSCEIVER WITH 5V TOLERANT I/O AND BUS-HOLD 74LVCH162245A(TSSOP48)	U2, U3, U5, U6	4
22	IC GATE	Quad 2-input AND gate 74LV08D (SOP14)	U12	1
23	IC GATE	Quad 2-input NAND gate 74LV00 (TSSOP14)	U15	1
24	IC REGULATOR	MAX1806EUA15	U16	1
25	IC REGULATOR	Micro power Low-Dropout (LDO) Voltage Regulator TPS76801QPWP (TSSOP20)	U9	1
26	IC REGULATOR	Notebook CPU Step-Down Controller for Intel Mobile Voltage Positioning MAX1718 (QSOP28)	U13	1
27	INDUCTOR	SMD 6.8uH (SDR1005-6R8M)	L1	1
28	OSCILLATOR	16.9344Mhz	OSC1	1
29	PIN	TEST PIN Gold Plated		2
30	RESISTOR	SMD 0 ohm 1608	R9~R15, R17, R18, R20, R21, R25, R27, R41, R43, R45, R47, R48, R71~R73, R75, R84, R87, R89, R90, R92, R94, R96, R97, R100, R101, R102	33
31	RESISTOR	SMD 1.5K ohm 1608	R74	1
32	RESISTOR	SMD 10 ohm 1608	R7, R8	2
33	RESISTOR	SMD 100k ohm 1608	R95, R103	2
34	RESISTOR	SMD 10K ohm 1608	R31~R37, R54, R79, R80, R81, R82, R85, R86, R99	15
35	RESISTOR	SMD 11.3K ohm, 1% 1608	R104	1
36	RESISTOR	SMD 120K ohm 1608	R91	1
37	RESISTOR	SMD 15K ohm 1608	R56, R60, R61, R62	4

4. SMDK2440 Part List (CPU Board) - Sheet 3 of 4

	ITEMS	DESCRIPTION	LOCATION	QTY
38	RESISTOR	SMD 15K ohm, 1% 1608	R106, R109	2
39	RESISTOR	SMD 18K ohm 1608	R70	1
40	RESISTOR	SMD 20 ohm 1608	R77	1
41	RESISTOR	SMD 20.5K ohm, 1% 1608	R107	1
42	RESISTOR	SMD 22 ohm 1608	R1~R6, R19, R57, R58	9
43	RESISTOR	SMD 240K ohm 1608	R50	1
44	RESISTOR	SMD 30 ohm 1608	R68, R63	2
45	RESISTOR	SMD 30.1K ohm, 1% 1608	R52, R105	2
46	RESISTOR	SMD 33K ohm 1608	R69	1
47	RESISTOR	SMD 4.7K ohm 1608	R16, R29, R39, R40	4
48	RESISTOR	SMD 470K ohm 1608	R67	1
49	RESISTOR	SMD 5 ohm 1608	R83	1
50	RESISTOR	SMD 53.6K ohm, 1% 1608	R51	1
51	RESISTOR	SMD ARRAY 22 ohm 3216 R-PACK	RN1~RN9	9
52	SDRAM	K4S561632C-TC75 (SSOP54)	U7, U8	2
53	SWITCH	TACT SW (RED)	SW1	1
54	TANTAL	SMD 100uF/16V 7343	C102, C104, C115	3
55	TANTAL	SMD 10uF/16V 3216	C110, C126, C316, C317, C322, C323	6
56	TANTAL	SMD 1uF/16V 3216	C8, C10, C12, C14, C17, C19, C22~C26, C32~C34, C38~C41, C46 ~ C51	24
57	TANTAL	SMD 220uF/16V 7343	C118, C119, C124	3
58	USB PORT	USB JACK B type	CON5	1
59	USB PORT	USB JACK Dual USB Port - A type	CON3	1
60	X-TAL	Crystal 32.768kHz	X1	1

4. SMDK2440 Part List (CPU Board) - Sheet 4 of 4

	ITEMS	DESCRIPTION	LOCATION	QTY
61	X-TAL	SMD Crystal 7050 94SMXD(16.9344Mhz)	X2	1
62	PCB	108x99x2t, FR-4, 8LAYER,Gold Plated		1
63	UNLOAD	OPEN (Unload)	C1~C7, R22, R23, R24, R26, R28, R30, R38, R44, R46, R64, R65, R66, R76, R88, R93, R98, R324, R325, U10	26

4. SMDK2440 Part List (Base Board) - Sheet 1 of 7

	ITEMS	DESCRIPTION	LOCATION	QTY
1	BEAD	SMD BLM31P601SG 3216	FB3, FB4	2
2	CERAMIC CAP	SMD 0.1uF 2012	C1~C10, C12~20,C22, C28~C36, C38, C40, C43~C46, C48~C59, C63, C80, C88, C89, C97, C99, C101~C104, C140~C142, C180, C181, C191, C602, C613, C640	64
3	CERAMIC CAP	SMD 100pF 2012	C61, C189	2
4	CERAMIC CAP	SMD 150pF 2012	C37	1
5	CERAMIC CAP	SMD 1uF 2012	C107, C109, C111, C113, C115, C117, C603, C604, C606, C614, C615, C618, C620, C622, C625, C626, C628, C630, C632, C633, C635, C636	22
6	CERAMIC CAP	SMD 2.2uF 2012	C616, C629	2
7	CERAMIC CAP	SMD 22pF 2012	C84, C85	2
8	CERAMIC CAP	SMD 3.3nF 2012	C83	1
9	CERAMIC CAP	SMD 330nF 2012	C82	1
10	CERAMIC CAP	SMD 330pF 2012	C70, C71, C74, C75, C76, C77, C78, C79, C621	9
11	CERAMIC CAP	SMD 33pF 2012	C617	1
12	CERAMIC CAP	SMD 4.7uF 3528	C601, C609, C612	3
13	CERAMIC CAP	SMD 47nF 2012	C605	1
14	CERAMIC CAP	SMD 560pF 2012	C21	1
15	CONDENSER	Electrolytic 220uF/10V (5x11) SHL	C95	1
16	CONDENSER	Electrolytic 680uF/16V (10x12.5) SHL	C94	1
17	CONNECTOR	5268-02,RIGHT ANGLE, BOX	CON6	1
18	CONNECTOR	BOX CONNECTOR DBED-9S (FEMALE)	CON14, CON22	2

4. SMDK2440 Part List (Base Board) - Sheet 2 of 7

	ITEMS	DESCRIPTION	LOCATION	QTY
19	CONNECTOR	BTE-060-03-L-D-A	CON23, CON24	2
20	CONNECTOR	HEADER 1x2	J14, J21, J22, J23, J601	5
21	CONNECTOR	PCMCIA 68PIN FRAME and SCOKET	CON3	1
22	CONNECTOR	SMART MEDIA CARD CN015R-3123-0 (TYPE31)	CON1	1
23	CONNECTOR FPC	4P CON	CON603	1
24	CONNECTOR FPC	Pitch=1.25mm 14PIN	CON16	1
25	CONNECTOR FPC	Pitch=1.25mm 8PIN	CON17	1
26	CONNECTOR HEADER	Female HEADER 2x16	CON19	1
27	CONNECTOR HEADER	MAIL HEADER 1x3	J1~J9, J11, J12, J16~J19, J24, J25	17
28	CONNECTOR HEADER	MAIL HEADER 1x5	CON15	1
29	CONNECTOR HEADER	MAIL HEADER 2x10	CON7	1
30	CONNECTOR HEADER	MAIL HEADER 2x17	CON10, CON11, CON12	3
31	CONNECTOR HEADER	MAIL HEADER 2x20	CON4	1
32	CONNECTOR HEADER	MAIL HEADER 2x5	CON8, CON5	2
33	CONNECTOR JACK	DC JACK	CON18	1
34	CONNECTOR JACK	STEREO JACK RT-30AWX	CON21	1
35	CONNECTOR LAN	XF10B11A-COMBO1-4S	CON2	1
36	CONNECTOR LCD	14_5602_020_001_829 (20P)	CON20	1
37	CONNECTOR LCD	14_5602_024_000_829 (24P)	CON25	1
38	CONNECTOR LCD	50Pin	CON602	1
39	CONNECTOR SOCKET	SD CARD SOCKET DC-PMS-1.0	CON13	1
40	DIODE	1N4148	D3	1
41	DIODE	SMD 1SS355	D601	1

4. SMDK2440 Part List (Base Board) - Sheet 3 of 7

	ITEMS	DESCRIPTION	LOCATION	QTY
42	DIODE	SMD DUAL Schottky Diode	DN601, DN602, DN603	3
43	DIODE	SMD Schottky Diode MCL4148-TR3	D602	1
44	DIODE	SMD Schottky Diode MBRD320	D2	1
45	DIODE	SMD Schottky Diode MBRS130L	D1	1
46	FUSE	POLY SWITCH miniSMDM150/24 (4836)	FP1	1
47	IC	Dual bus switch with level shifting CBTD3306 (SO8)	U37	1
48	IC	Hex Inverter 74LV04 (14SOP)	U6	1
49	IC	Hex inverting Schmitt-trigger 74LV14 (14SOP)	U28	1
50	IC	Octal dual supply translating transceiver 3-state 74LVC4245 (24SSOP)	U12~U16, U35, U36	7
51	IC	PC Card Host Adapters CL-PD6710 (144VQFP)	U9	1
52	IC	PC Card power-interface Switch TPS2211 (16SOP)	U10	1
53	IC	Quad 2-input AND gate 74LV08 (14SOP)	U22	1
54	IC	Quad 2-input OR gate 74LV32 (14SOP)	U5, U8	2
55	IC	RS-232 Line Driver/Receivers MAX3232C (16SOP)	U20	1
56	IC	RS-232 Line Driver/Receivers MAX3243 (28SSOP)	U29	1
57	IC	Very low-power SPI-interface keyboard encoder UR5HCSPI-SA (44QFP)	U24	1
58	IC	White LED driver MP1521/MSOP-10P	U602	1
59	IC CODEC	Economy audio CODEC for MiniDisc (MD) home stereo and portable applications UDA1341TS (28SSOP)	U25	1
60	IC COMPERATOR	IC COMPERATOR AD8542AR (8SOIC)	U601	1

4. SMDK2440 Part List (Base Board) - Sheet 4 of 7

	ITEMS	DESCRIPTION	LOCATION	QTY
61	IC CONVERTER	Low-power DC-DC Converter MAX629 (8SOP)	U11	1
62	IC CONVERTER	Low-Power Triple-Output TFT LCD DC-DC Converter MAX1779 (16TSSOP)	U603	1
63	IC EEPROM	EEPROM KS24C080C (8SOP)	U23	1
64	IC FLASH	FLASH MEMORY AM29LV800BB-90EC (48TSOP1)	U3	1
65	IC FLASH	NAND FLASH K9K2G16U0M (48TSOP1)	U4	1
66	IC LAN	Ethernet Controller CS8900A-CQ3 (100TQFP)	U7	1
67	INDUCTOR	SMD 10uH 2012	L601, L602	2
68	INDUCTOR	SMD 33uH 12x12	L2	1
69	INDUCTOR	SMD 47uH 3528	L1	1
70	IrDA	RPM851A	U21	1
71	LCD	LTS350Q1-PE1	LCD	1
72	LED	SMD TYPE (GREEN)	LED1~LED7	7
73	LED	SMD TYPE (RED)	LED8	1
74	MEMORY	K6X4016T3F-TB55 (44TSOP2)	U32	1
75	MICROPHONE	MICROPHONE (1.5V, 60dB)	MIC1	1
76	OSCILLATOR	OSC-HALF 25Mhz	OSC1	1
77	PIN	Gold Plated TEST PIN	GND	3
78	REGULATOR	1.5A Fast Ultra Low Dropout Linear Regulators LP3965-ADJ (SOT223-5)	U18, U38	2
79	REGULATOR	3A Low Dropout Positive Regulators LM1085-3.3 (TO263)	U27	1
80	REGULATOR	SIMPLE SWITCHER Power Converter 150 KHz 3A Step-Down Voltage Regulator LM2596S-5.0 (TO263-5)	U26	1

4. SMDK2440 Part List (Base Board) - Sheet 5 of 7

	ITEMS	DESCRIPTION	LOCATION	QTY
81	RESISTOR	DIP 1/4W 100 ohm 1%	R56	1
82	RESISTOR	DIP 1/4W 4.99K,1%	R51	1
83	RESISTOR	DIP 1/4W 47 ohm	R112	1
84	RESISTOR	DIP 1/4W 5.6 ohm	R109	1
85	RESISTOR	DIP 1/4W 8 ohm 1%	R57, R58	2
86	RESISTOR	SMD 100 ohm 2012	R70, R130~R132	4
87	RESISTOR	SMD 100K 2012	R607, R625, R639	3
88	RESISTOR	SMD 10K 2012	R7, R8, R15, R24, R38~R41, R63, R64, R67, R69, R82, R84, R101~R106, R108, R115, R116, R134, R135, R152, R156, R157, R170, R171, R272, R274, R275, R605, R626, R652	36
89	RESISTOR	SMD 13K 2012	R271	1
90	RESISTOR	SMD 15K 2012	R123, R124, R127, R651, R602	5
91	RESISTOR	SMD 1M 2012	R126, R608, R609, R653, R654	5
92	RESISTOR	SMD 330K 2012	R601	1
93	RESISTOR	SMD 4.7K 2012	R5, R6, R9~R12, R14, R42~R46, R73~R76, R78, R80, R81, R113, R117, R138~R140, R149~R151, R153, R642, R655	30
94	RESISTOR	SMD 470 ohm 2012	R154	1
95	RESISTOR	SMD 6.8K 2012	R133	1
96	RESISTOR	SMD 68K 2012	R72	1

4. SMDK2440 Part List (Base Board) - Sheet 6 of 7

	ITEMS	DESCRIPTION	LOCATION	QTY
97	RESISTOR	SMD 0 ohm 2012	R1, R2, R13, R16~R18, R20, R21, R23, R26, R27, R29, R30, R32~R34, R37, R47~R50, R54, R55, R60~R62, R77, R85~R100, R107, R114, R118, R121, R128, R136, R137, R141~R144, R158~R162, R180, R188, R221, R269, R273, R631, R636	66
98	RESISTOR	SMD 12K 2012	R611	1
99	RESISTOR	SMD 150K 2012	R119, R122, R125	3
100	RESISTOR	SMD 150K 2012	R623	1
101	RESISTOR	SMD 1K 2012	R66, R71, R110, R111	4
102	RESISTOR	SMD 26 ohm 2012	R610	1
103	RESISTOR	SMD 330 ohm 2012	R52, R53, R59, R83, R145, R146, R147, R148, R155	9
104	RESISTOR	SMD 390K 2012	R634	1
105	RESISTOR	SMD 47K 2012	R606	1
106	RESISTOR	SMD 51K 2012	R628, R637, R640	3
107	RESISTOR	SMD 680K 2012	R635	1
108	RESISTOR	SMD 69K 2012	R604	1
109	RESISTOR	Volume Resistor T93YA 10K	VR1	1
110	SHUNT	Short Pin 2pin (Red Color)		10
111	SOCKET	FLASH SOCKET 980020-48-01	U3	1
112	SWITCH	TACT (SMALL) BLACK	S2~S5	4
113	SWITCH	TACT (SMALL) RED	S6	1
114	SWITCH	TOGGLE MS24L244	S1	1
115	TANTAL	SMD 0.1uF/16V 3216	C64, C65, C66, C67, C68, C69, C72, C73	8

4. SMDK2440 Part List (Base Board) - Sheet 7 of 7

	ITEMS	DESCRIPTION	LOCATION	QTY
116	TANTAL	SMD 100uF/16V 7343	C27, C52, C86, C108, C110, C112, C114, C116, C187	9
117	TANTAL	SMD 10uF 3528	C608	1
118	TANTAL	SMD 10uF/16V 3528	C11, C26, C41, C42, C47, C60, C62, C98, C96, C100, C139, C186, C188, C190, C619	15
119	TANTAL	SMD 1uF/25V 3216	C607, C610, C611, C631	4
120	TANTAL	SMD 22uF/36V 7343	C39	1
121	TANTAL	SMD 4.7uF/16V 3528	C81	1
122	TANTAL	SMD 47uF/16V 7343	C87, C90, C91, C92, C93	5
123	TRANSISTOR	SMD MMBT3904 (SOT23)	Q1	1
124	X-TAL	Crystal 20.0Mhz (ATS49)	X1	1
125	X-TAL	Crystal 2MHz (ATS49)	X2	1
126	PCB	237X165X2t, FR-4, 8LAYER Gold Plated		1
127	UNLOAD	OPEN (UNLOAD)	C23~C25, CON9, J10, R3, R4, R19, R22, R25, R28, R31, R35, R36, R65, R68, R120, R129, R270, R614, R624, R629, R630, R632, R633, R638, R641, R656, U1, U2, U4, U32	32

NOTES