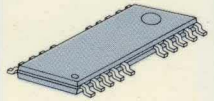
SAMSUNG

2110 - 4061

SAMSUNG
EXTENDED DATA OUT DRAM

MAY. 1994



- KM44C1004C/CL/CSL
- KM44V1004C/CL/CSL
- KM48C514B/BL/BLL
- KM48V514B/BL/BLL
- KM416C254B/BL/BLL
- KM416V254B/BL/BLL
- KM44C4004A/AL/ALL/ASL
- KM44C4104A/AL/ALL/ASL
- KM44V4004A/AL/ALL/ASL
- KM44V4104A/AL/ALL/ASL
- KM48C2004A/AL/ALL/ASL
- KM48C2104A/AL/ALL/ASL
- KM48V2004A/AL/ALL/ASL
- KM48V2104A/AL/ALL/ASL

PRINTED IN KOREA

Certified ISO 9001

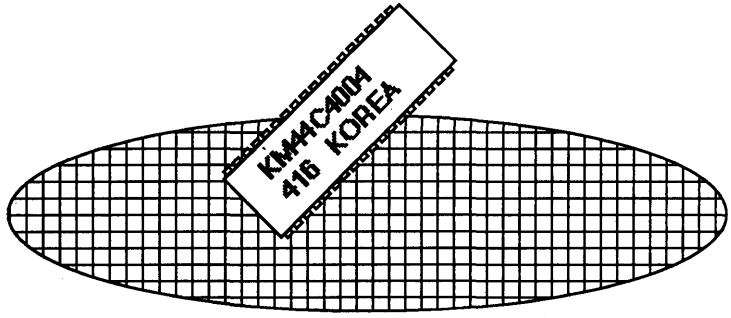
Certificate No FM 24651

SAMSUNG'S
EXTENDED DATA OUT DRAM

MAY. 1994

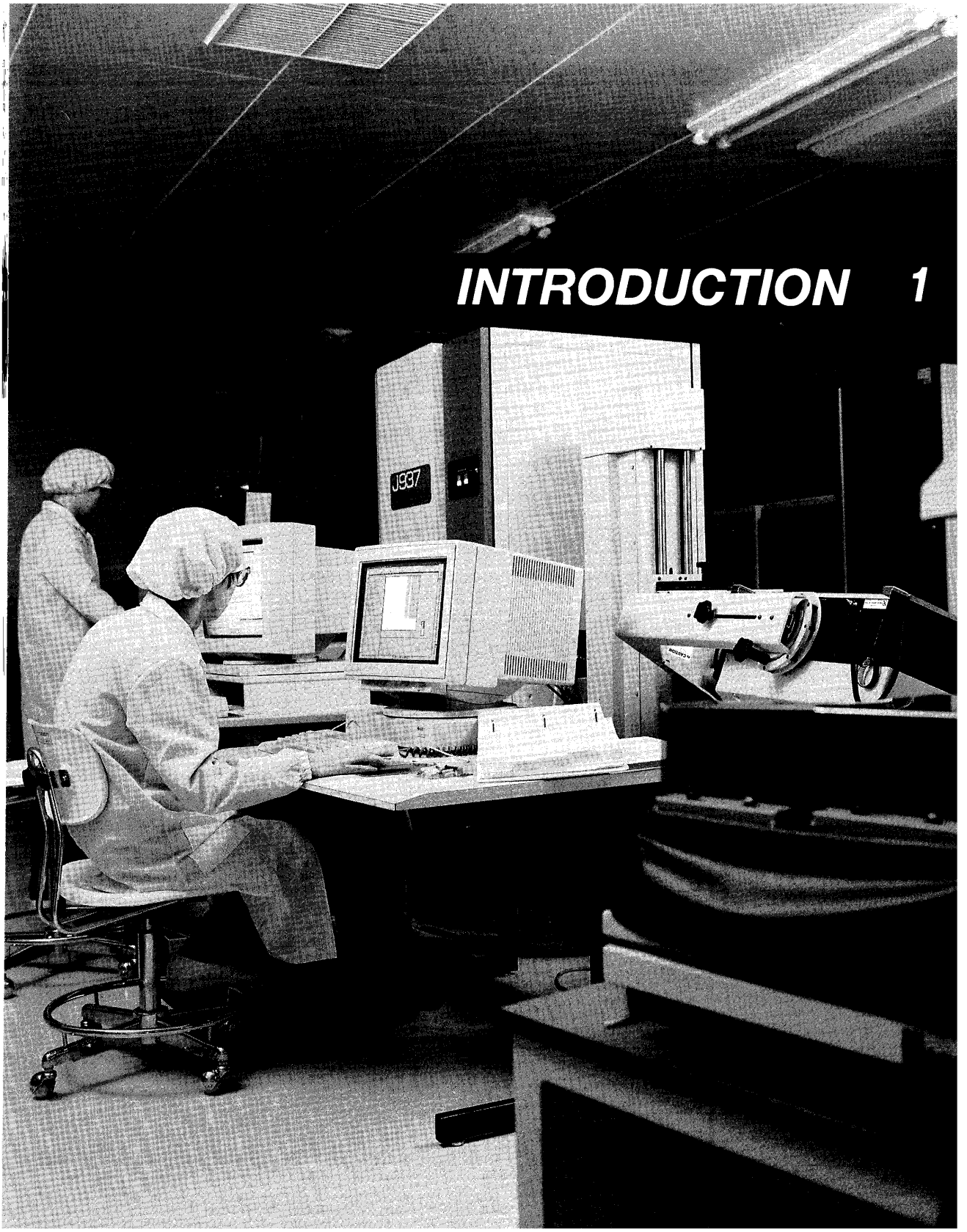
SAMSUNG

The following material can be used to introduce the new SAMSUNG's CMOS Extended Data Out DRAMs to SAMSUNG's customers.



SAMSUNG

CONTENTS



INTRODUCTION 1

INTRODUCTION

Newer systems require higher memory bandwidth to improve performance. Although memory performance has increased over time, but some system needs outpaced the bandwidth of modes like Fast-Page Mode(FPM) or Static-Column Mode(SCM) in DRAMs. The improved feature of FPM known as Extended Data-Out(EDO) can overcome the limitation of minimum page cycle time. The device with EDO feature accepts the column address for the next cycle without disabling the data output on the rising edge of $\overline{CAS}$ to achieve shorter cycle time than standard FPM.

What is EDO

In the conventional FPM read cycle, the data output buffers are turned off (High-Z) with the rising edge of $\overline{CAS}$. Even though $\overline{OE}$ stays LOW state (active), positive going edge of $\overline{CAS}$ will make the data output buffers disabled. Fig1 shows a typical FPM read cycle.

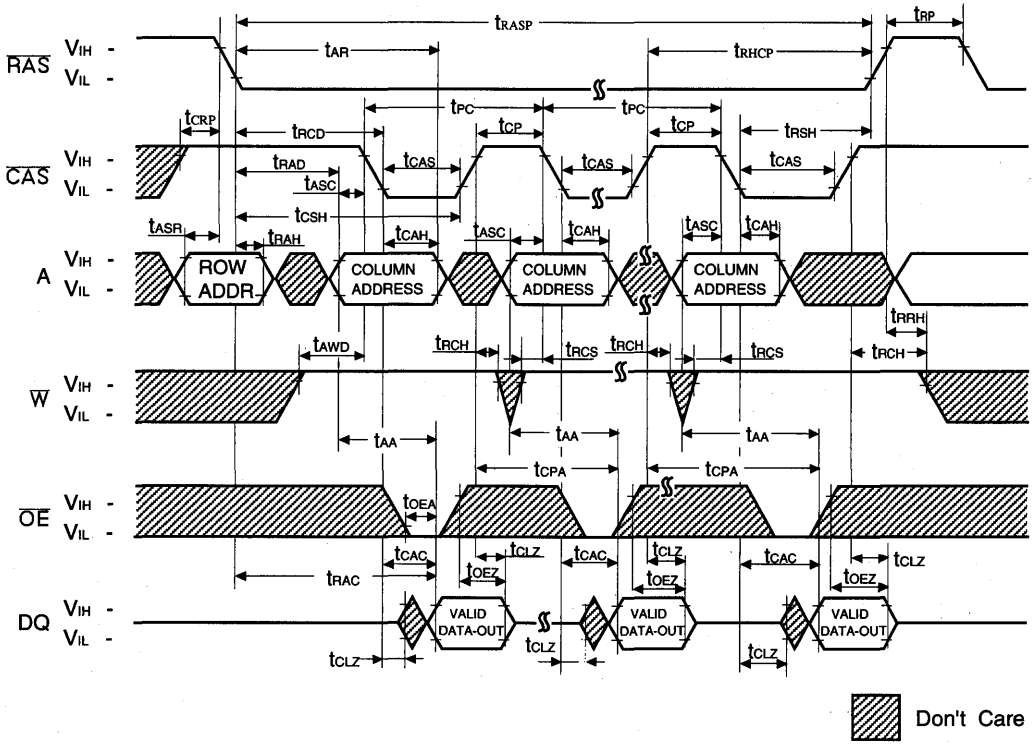


Fig.1 FAST PAGE MODE READ CYCLE

But during the $\overline{CAS}$ precharge time (tCP) of Extended Data Output mode, the data doesn't go invalid. EDO mode offers an accelerated Fast Page cycle, so called Hyper Page cycle, by moving the $\overline{CAS}$ high going edge earlier without effecting the data output buffers.DRAM read cycle and FPM read cycle are similar to EDO mode except valid data will be held as long as both $\overline{RAS}$ and $\overline{OE}$ are LOW. In EDO mode read cycle data output will be disabled by $\overline{OE}$ HIGH or $\overline{WE}$ LOW or both $\overline{RAS}$ and $\overline{CAS}$ HIGH. So when EDO DRAM is used in multiple banks, $\overline{OE}$ or $\overline{WE}$ may be the key clock to select the appropriate banks. These interleaving methods will be described later.

Advantage of EDO

The most important advantage is higher performance than FPM by Extended Data Out during the $\overline{CAS}$ precharge time(tCP). In page cycle, since data output does not go High-Z state at the rising edge of $\overline{CAS}$, tCP and $\overline{CAS}$ pulse width (tCAS) can be reduced. Consequentially EDO mode may reduce the total page cycle time to tHPC. EDO mode read cycle is shown in Fig.2.

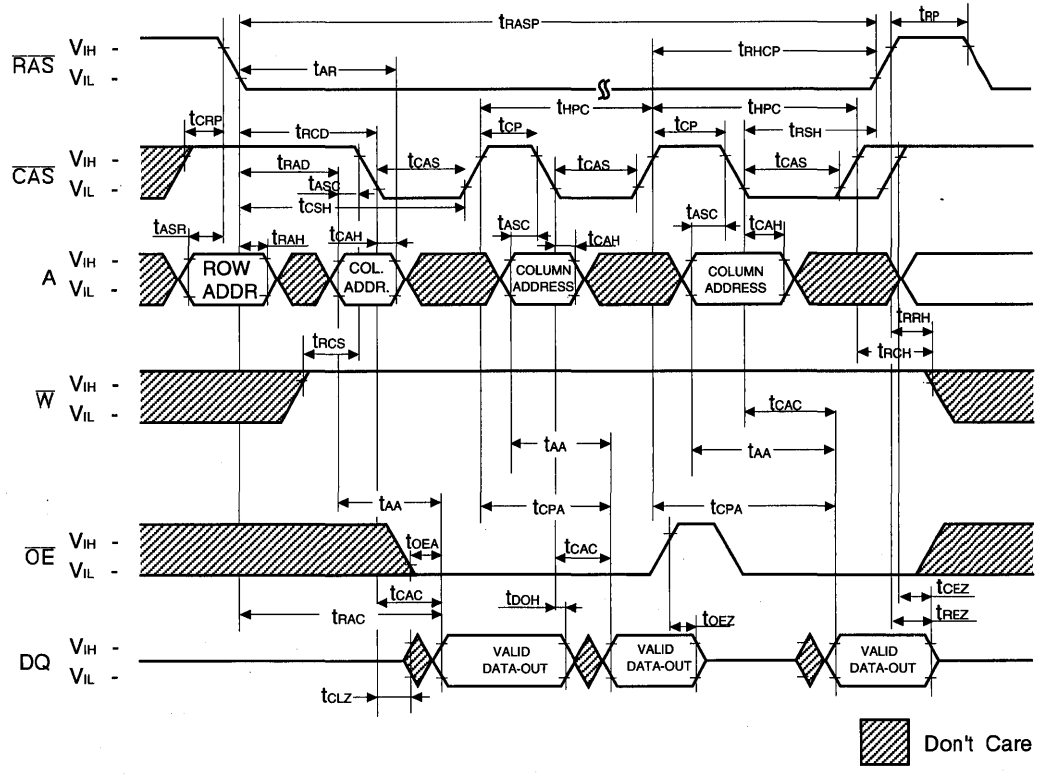


Fig.2 HYPER PAGE MODE READ CYCLE

Fig.3 shows how EDO page cycle (Hyper Page Cycle) time can be reduced, compared to FPM. In FPM (Fig.3.a), minimum fast page mode cycle time (tPC) is decided by summation of $\overline{CAS}$ precharge access time (tCPA) and transition time (tT), to guarantee the valid data access. Since tCPA is the longest access time in FPM, $\overline{CAS}$ cannot go HIGH before tCPA for the data out to be valid.

But in EDO mode page read cycle (Fig.3.b), tHPC may save the tCP. tCPA is still the longest access time, but data out is active in the $\overline{CAS}$ precharge time. In other words, $\overline{CAS}$ may go high before tCPA as long as the starting point of the next $\overline{CAS}$ cycle dose not hurt the previous access. Consequentially minimum tHPC can be decided as tCPA - (tCP+tT), but tCP and tCAS must be guaranteed the minimum value(10ns each at -6 part). In this way, the maximum bandwidth is increased from 40nsec in FPM to 24nsec in EDO page mode, up to 60% improvement for -6 parts. Table1 shows the important EDO mode AC parameters comparing to FPM's.

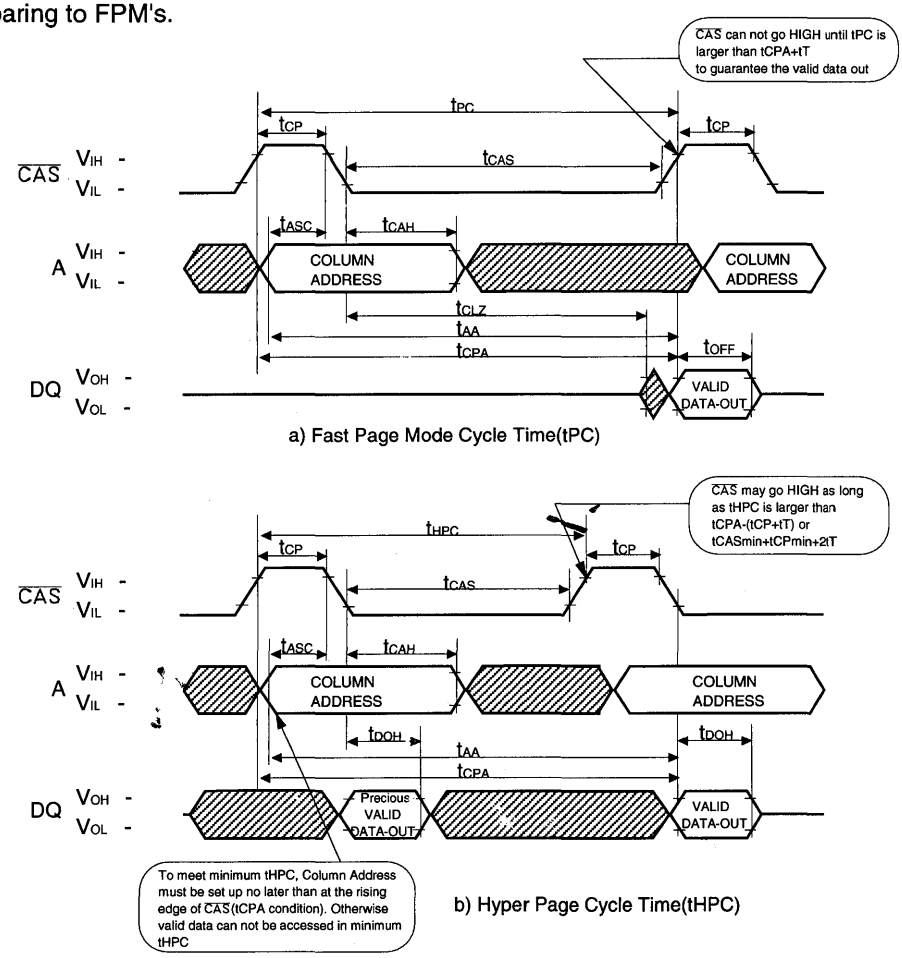
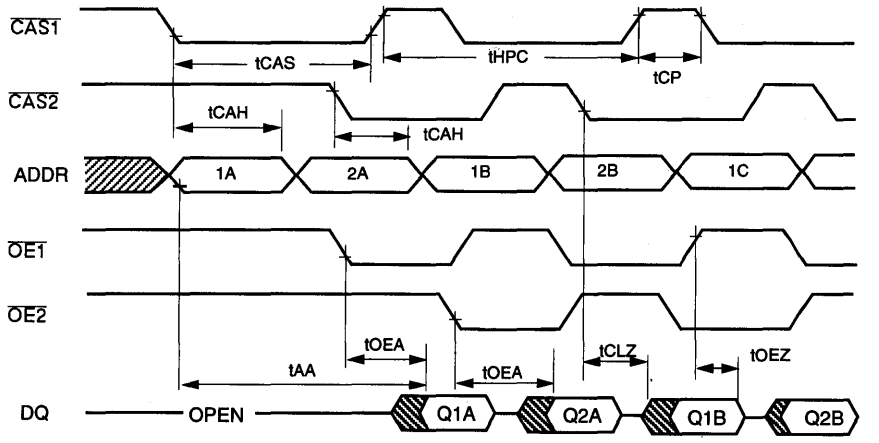


Fig.3 PAGE CYCLE TIME COMPARISON

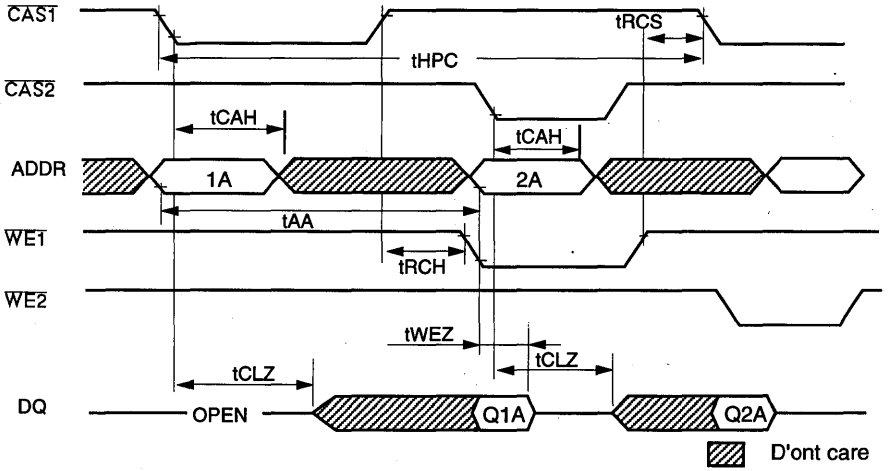
SAMSUNG ELECTRONICS

Interleaving Methods

In EDO DRAMs, $\overline{CAS}$ clock can not be used as selector of banks. Since the rising edge of $\overline{CAS}$ can not make data output High-Z state. $\overline{OE}$ and $\overline{WE}$ can be used to select or deselect the appropriate banks. If $\overline{CAS}$ is LOW, $\overline{OE}$ must be used and if $\overline{CAS}$ is HIGH, either $\overline{OE}$ or $\overline{WE}$ may be used as master select signal. The $\overline{OE}$ and $\overline{WE}$ interleaving methods are shown in Fig.4.



a)$\overline{OE}$ Controlled Interleaving



b) $\overline{WE}$ Controlled Interleaving

Fig.4 $\overline{OE}$ & $\overline{WE}$ Interleaving Methods

unit [ns]

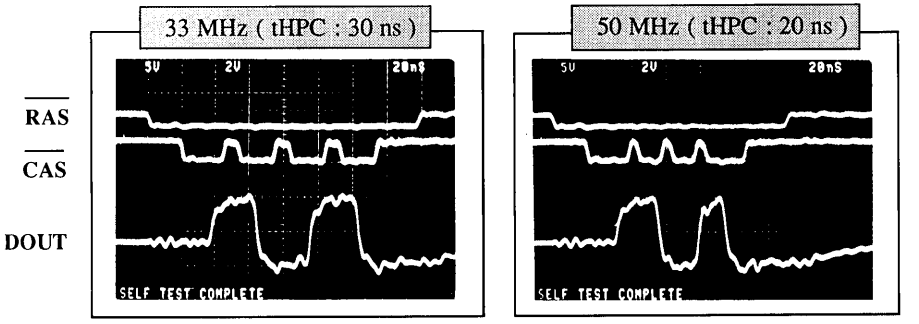
Parameter	Symbol	EDO	FPM
Page mode cycle time	tPC		40
Hyper page cycle time	tHPC	24	
$\overline{CAS}$ pulse width	tCAS	10	15
$\overline{CAS}$ precharge time	tCP	10	10
Column address hold time	tCAH	10	15
transition time	tT(min)	2	5
Output buffer turn off delay from $\overline{CAS}$	tCEZ(max)	15	15
Access time from $\overline{CAS}$ precharge	tCPA	35	35
Access time from column address	tAA	30	30

Table1 AC Parameter Comparison table

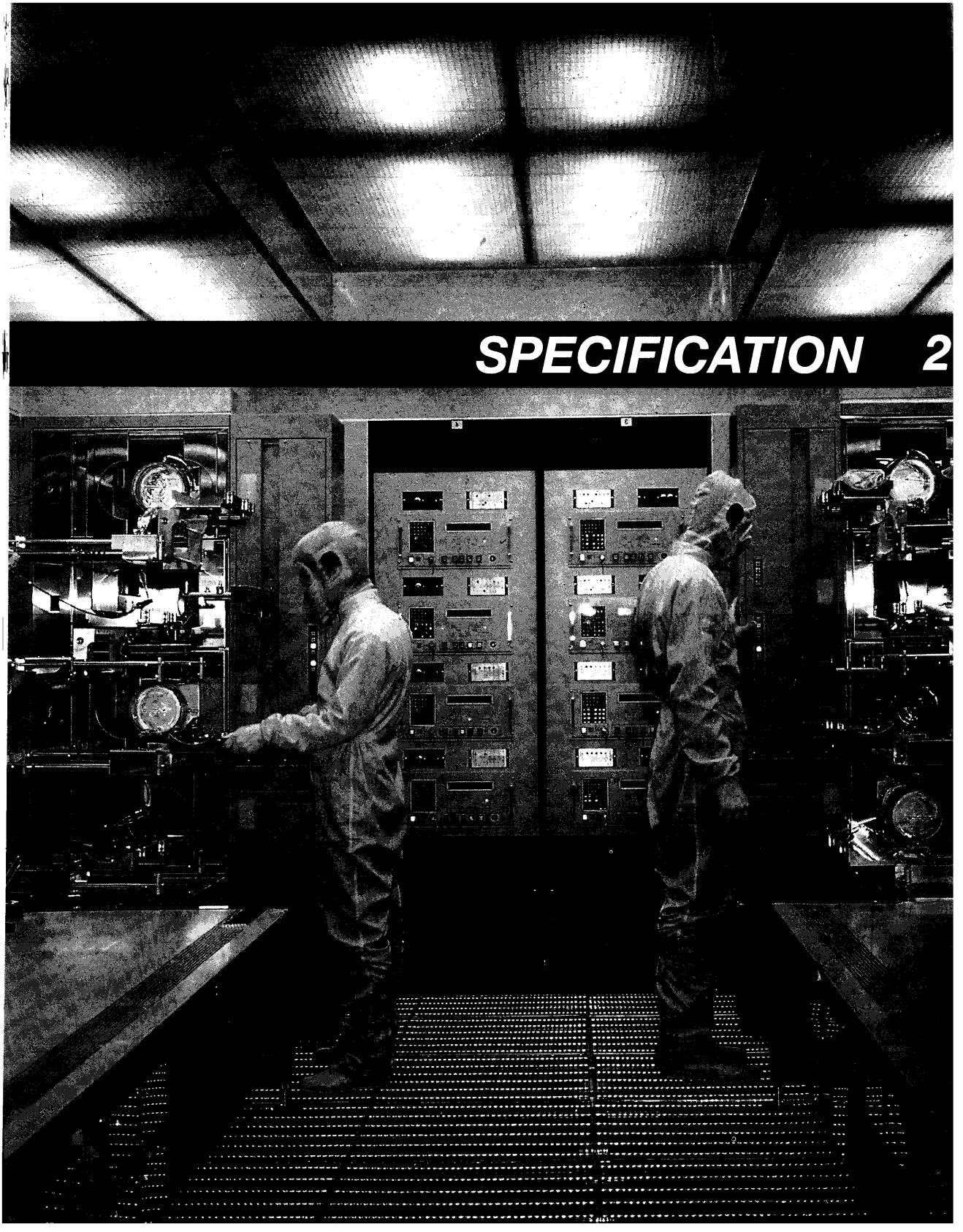
Data Out Waveform In EDO Mode

@Sample : KM416C254B , 300mil SOJ PKG
(256K X 16 , 512 Refresh , Fast Page with EDO)

@Condition : 5V / Room Temp.
tRCD : 20 ns
tCSH : 45 ns
4 Bit Page In EDO (Data Out 1 0 1 0)



SAMSUNG ELECTRONICS



SPECIFICATION 2

1M x 4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	tRAC	tCAC	tRC	tHPC
KM44C1004C/CL/CSL-5	50ns	13ns	90ns	20ns
KM44C1004C/CL/CSL-6	60ns	15ns	110ns	24ns
KM44C1004C/CL/CSL-7	70ns	20ns	130ns	29ns
KM44C1004C/CL/CSL-8	80ns	20ns	150ns	34ns

• Fast Page Mode with Extended data out
• $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
• $\overline{RAS}$-only and Hidden refresh capability
• Fast parallel test mode capability
• TTL compatible inputs and outputs
• Early Write or output enable controlled write
• Single +5V±10% power supply
• Refresh Cycle
  - 1024 cycle/16ms(Normal)
  - 1024 cycle/128ms(L-ver)
  - 1024 cycle/256ms(SL-ver)
• Power Dissipation
  - Standby : 5.5mW(Normal)
    1.1mW(L-ver)
    0.55mW(SL-ver)
  - Active(50/60/70/80) : 468/413/358/303mW
• JEDEC Standard pinout
• Available in Plastic DIP,SOJ,ZIP and TSOP(II)

GENERAL DESCRIPTION

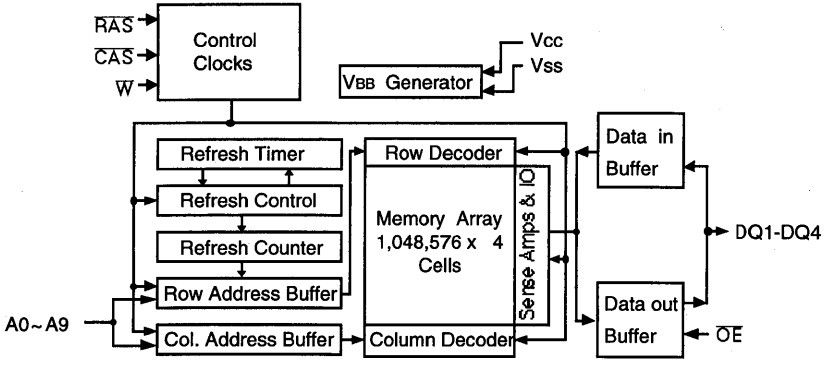
The Samsung KM44C1004C/CL/CSL is a CMOS high speed 1,048,576 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and minicomputers, graphics and high performance portable computers.

The KM44C1004C/CL/CSL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C1004C/CL/CSL is fabricated using Samsung's advanced CMOS process.

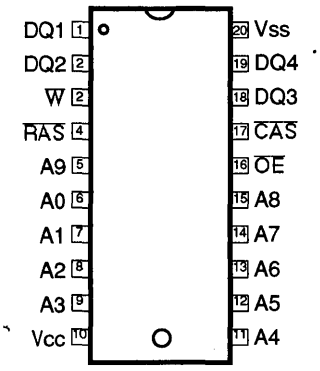
2

FUNCTIONAL BLOCK DIAGRAM

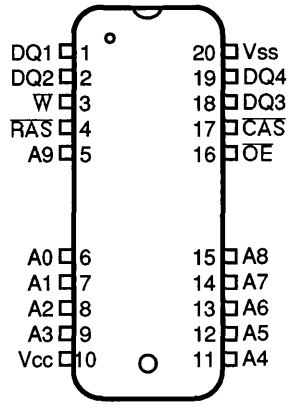


PIN CONFIGURATION (Top Views)

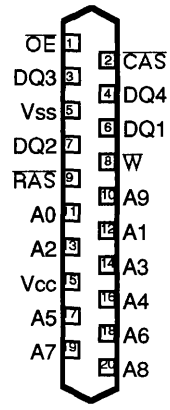
• KM44C1004CP/CLP/CSLP



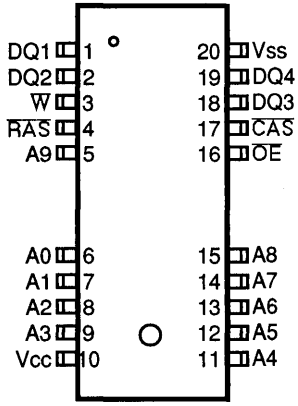
• KM44C1004CJ/CLJ/CSLJ



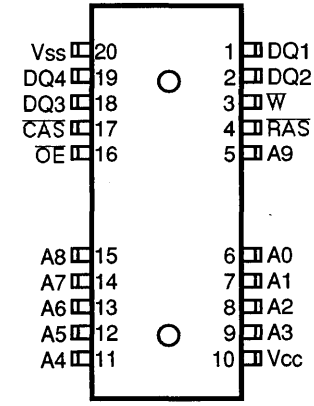
• KM44C1004CZ/CLZ/CSLZ



• KM44C1004CT/CLT/CSLT



• KM44C1004CTR/CLTR/CSLTR



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ1 - 4	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM44C1004C/CL/CSL-5	I_{CC1}		85	mA
	KM44C1004C/CL/CSL-6			75	mA
	KM44C1004C/CL/CSL-7			65	mA
	KM44C1004C/CL/CSL-8			55	mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C1004C	I_{CC2}		2	mA
	KM44C1004CL			1	mA
	KM44C1004CSL			1	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)	KM44C1004C/CL/CSL-5	I_{CC3}		85	mA
	KM44C1004C/CL/CSL-6			75	mA
	KM44C1004C/CL/CSL-7			65	mA
	KM44C1004C/CL/CSL-8			55	mA
EDO MODE CURRENT* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$,Address cycling @tHPC=min.)	KM44C1004C/CL/CSL-5	I_{CC4}		85	mA
	KM44C1004C/CL/CSL-6			75	mA
	KM44C1004C/CL/CSL-7			65	mA
	KM44C1004C/CL/CSL-8			55	mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)	KM44C1004C	I_{CC5}		1	mA
	KM44C1004CL			200	µA
	KM44C1004CSL			100	µA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM44C1004C/CL/CSL-5	I_{CC6}		85	mA
	KM44C1004C/CL/CSL-6			75	mA
	KM44C1004C/CL/CSL-7			65	mA
	KM44C1004C/CL/CSL-8			55	mA
Batery back-up current Average power supply current Battery back-up mode Input high voltage(V_{IH})=Vcc-0.2V Input low voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V DQ1-DQ4=Don't care t_{RC}= 125µs(L-ver), 250µs(SL-ver) t_{RAS}=t_{RAS} min~300ns	KM44C1004CL	I_{CC7}		300	µA
	KM44C1004CSL			150	µA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤Vcc+0.5V all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	µA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤Vcc)		$I_{O(L)}$	-10	10	µA
OUTPUT HIGH VOLTAGE LEVEL(I_{OH}=-5mA)		V_{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL(I_{OL}=4.2mA)		V_{OL}	-	0.4	V

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE(T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ1 - DQ4]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10% See notes 1,2)
Test condition: V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100 pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	7,14,15
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$ See notes 1,2)

Test condition: $V_{IH}/V_{IL}=2.4/0.8V$, $V_{OH}/V_{OL}=2.0/0.8V$, output loading $C_L=100$ pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period(Normal)	tREF		16		16		16		16	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Refresh period(SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		10		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		24		29		34		ns	16
Hyper Page read-modify-write cycle time	tHPRWC	64		73		88		98		ns	
$\overline{CAS}$ precharge time (Hyper Page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	7,14
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write commend set-up time(Test mode in)	tWTS	10		10		10		10		ns	12
Write commend hold time(Test mode in)	tWTH	10		10		10		10		ns	12
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	7,14,15
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width(Hyper Page Cycle)	tWPE	5		5		5		5		ns	

TEST MODE CYCLE

(Note. 12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	45		55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	tHPC	25		29		34		39		ns	
Hyper Page read-modify-write cycle time	tHPRWC	69		78		93		103		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

TEST MODE DESCRIPTION

The KM44C1004C/CL/CSL is the CMOS DRAM organized 1,048,576 words by 4 bit internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1Mx4 DRAM can be tested as if it were a 512Kx4 DRAM. $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", . And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time(1/2 in cases of N test pattern).

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min) the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
16. tASC≥tCPmin, Assume tT=2.0ns

1M x4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	tRAC	tCAC	tRC	tHPC
KM44V1004C/CL/CLL-6	60ns	15ns	110ns	24ns
KM44V1004C/CL/CLL-7	70ns	20ns	130ns	29ns
KM44V1004C/CL/CLL-8	80ns	20ns	150ns	34ns

• Fast Page Mode with Extended data out
• Self Refresh operation(LL-ver.)
• $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
• $\overline{RAS}$-only and Hidden refresh capability
• Fast parallel test mode capability
• TTL compatible inputs and outputs
• Early Write or output enable controlled write
• Single +3.3V± 0.3V power supply
• 1024 cycle/16ms refresh(Normal)
• 1024 cycle/128ms refresh(L/LL-ver)
• Power Dissipation
  - Standby : 3.6mW(Normal)
    0.36mW(L-ver)
    0.36mW(LL-ver)
  - Active(60/70/80) : 220/200/180mW
• JEDEC Standard pinout
• Available in Plastic DIP,SOJ, ZIP and TSOP(II)

GENERAL DESCRIPTION

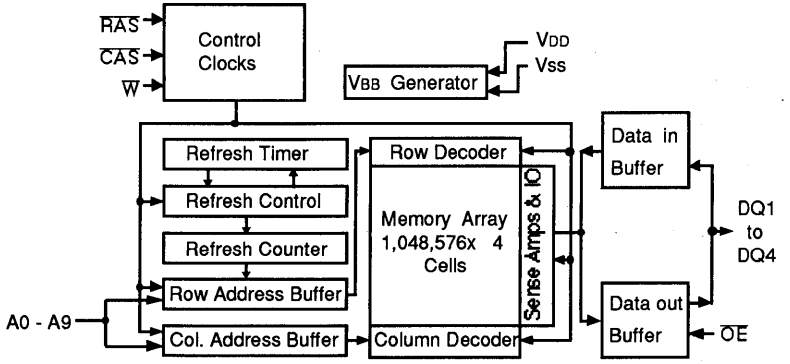
The Samsung KM44V1004C/CL/CLLis a CMOS high speed 1,048,576 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM44V1004C/CL/CLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44V1004C/CL/CLL is fabricated using Samsung's advanced CMOS process.

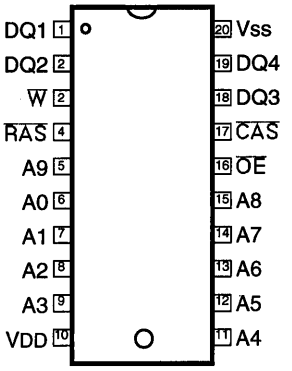
2

FUNCTIONAL BLOCK DIAGRAM

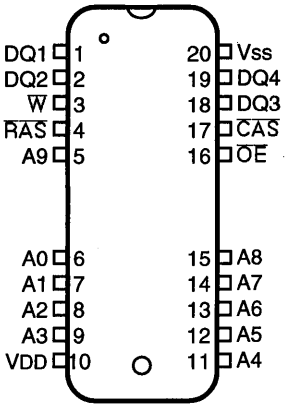


PIN CONFIGURATION (Top Views)

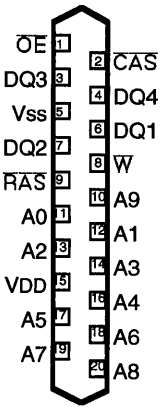
• KM44V1004CP/CLP/CLLP



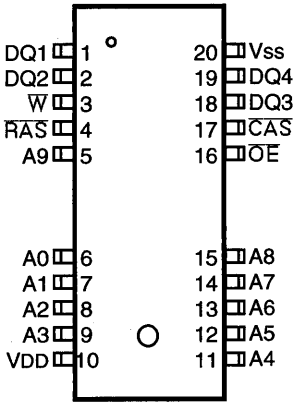
• KM44V1004CJ/CLJ/CLLJ



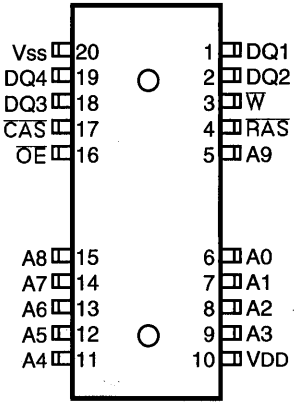
• KM44V1004CZ/CLZ/CLLZ



• KM44V1004CT/CLT/CLLT



• KM44V1004CTR/CLTR/CLLTR



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ1 - 4	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
VDD	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	VDD+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM44V1004C/CL/CLL-6 KM44V1004C/CL/CLL-7 KM44V1004C/CL/CLL-8	I_{CC1}		60 55 50	mA mA mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44V1004C KM44V1004CL KM44V1004CLL	I_{CC2}		500 500 500	uA uA uA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)	KM44V1004C/CL/CLL-6 KM44V1004C/CL/CLL-7 KM44V1004C/CL/CLL-8	I_{CC3}		60 55 50	mA mA mA
EDO MODE CURRENT* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$,Address cycling @tPC=min.)	KM44V1004C/CL/CLL-6 KM44V1004C/CL/CLL-7 KM44V1004C/CL/CLL-8	I_{CC4}		60 55 50	mA mA mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM44V1004C KM44V1004CL KM44V1004CLL	I_{CC5}		1 100 100	mA µA µA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM44V1004C/CL/CLL-6 KM44V1004C/CL/CLL-7 KM44V1004C/CL/CLL-8	I_{CC6}		60 55 50	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$ = $\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ1-DQ4 = Don't Care t_{RC} =125 µS, t_{RAS} =t_{RAS} min.~300 nS	KM44V1004CL	I_{CC7}		200	µA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=V_{IL} $\overline{W}$=$\overline{OE}$=A0-A9=V_{DD}-0.2V or 0.2V DQ1-DQ4=V_{DD}-0.2V, 0.2V or OPEN	KM44V1004CLL	I_{CC8}		150	µA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤V_{DD}+0.3V all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	µA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤V_{DD})		$I_{O(L)}$	-10	10	µA
OUTPUT HIGH VOLTAGE LEVEL(I_{OH}=-2mA)		V_{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL(I_{OL}=2mA)		V_{OL}	-	0.4	V

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE(T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ1 - DQ4]	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{DD}=3.3V±0.3V See notes 1,2)
Test Condition : V_{ih}/V_{il} = 2.0V/0.8V, V_{oh}/V_{ol} = 2.0V/0.8V, Output Loading C_L = 100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	15	3	20	3	20	ns	7,14,15
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	10	10K	15	10K	20	10K	ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		55		60		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	10		15		20		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{DD}=3.3V \pm 0.3V$ See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		15		15		ns	10
data hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period(Normal)	tREF		16		16		16	ms	
Refresh period(L-ver & LL-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		65		70		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		70		75		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		10		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		30		30		ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Hyper Page cycle time	tHPC	24		29		34		ns	16
Hyper page read-modify-write cycle time	tHPRWC	73		88		98		ns	
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7,14
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay form $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	7,14,15
Output buffer turn off delay form $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width(Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	17
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	17
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	17

TEST MODE CYCLE

(Note. 12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	18	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		70		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Hyper Page cycle time	tHPC	29		34		39		ns	16
Hyper page read-modify-write cycle time	tHPRWC	78		93		103		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time form $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

TEST MODE DESCRIPTION

The KM44V1004C/CL/CLL is the CMOS DRAM organized 1,048,576 words by 4 bit internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1Mx4 DRAM can be tested as if it were a 512Kx4 DRAM. $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", . And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time(1/2 in cases of N test pattern).

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min) the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
16. tASC≥tCPmin, Assume tT=2.0ns
17. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.(LL-ver.)

512K x 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	tRAC	tCAC	tRC	tHPC
KM48C514B/BL/BLL-5	50ns	17ns	90ns	20ns
KM48C514B/BL/BLL-6	60ns	17ns	110ns	24ns
KM48C514B/BL/BLL-7	70ns	20ns	130ns	29ns

- Fast Page Mode with Extended data out
- Self Refresh operation(LL-ver.)
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Dual +5± 10%power supply
- Refresh Cycle
  -1024 cycle/16ms (Normal)
  -1024 cycle/128ms (L/LL-ver)
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

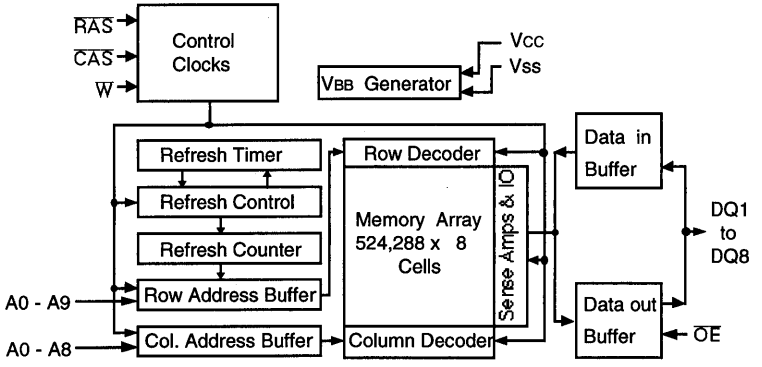
The Samsung KM48C514B/BL/BLL is a CMOS high speed 524,288 x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48C514B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48C514B/BL/BLL is fabricated using Samsung's advanced CMOS process.

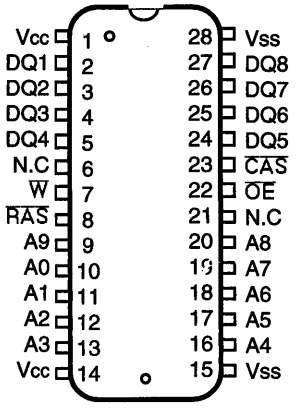
2

FUNCTIONAL BLOCK DIAGRAM

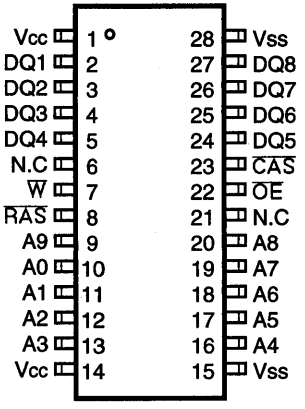


PIN CONFIGURATION (Top Views)

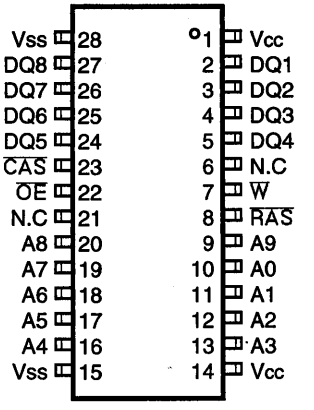
• KM48C514BJ/BLJ/BLLJ



• KM48C514BT/BLT/BLLT



• KM48C514BTR/BLTR/BLLTR



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ1 -8	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Outputs Enable
Vcc	Power(+5V)
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM48C514B/BL/BLL-5 KM48C514B/BL/BLL-6 KM48C514B/BL/BLL-7	I_{CC1}		85 70 65	mA mA mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48C514B KM48C514BL KM48C514BLL	I_{CC2}		2 2 2	mA mA mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)	KM48C514B/BL/BLL-5 KM48C514B/BL/BLL-6 KM48C514B/BL/BLL-7	I_{CC3}		85 70 65	mA mA mA
EDO MODE CURRENT* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$,Address cycling @tPC=min.)	KM48C514B/BL/BLL-5 KM48C514B/BL/BLL-6 KM48C514B/BL/BLL-7	I_{CC4}		65 55 50	mA mA mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM48C514B KM48C514BL KM48C514BLL	I_{CC5}		1 200 150	mA µA µA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM48C514B/BL/BLL-5 KM48C514B/BL/BLL-6 KM48C514B/BL/BLL-7	I_{CC6}		85 70 65	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH})=V_{CC}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$ = 0.2V DQ= Don't Care T_{RC} =125 µS, T_{RAS} =T_{RAS} min.~300 nS	KM48C514BL	I_{CC7}		300	µA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A0-A9=V_{CC}-0.2V or 0.2V DQ1-DQ8=V_{CC}-0.2V, 0.2V or OPEN	KM48C514BLL	I_{CC8}		200	µA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤V_{CC}+0.5V all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	µA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤VCC)		$I_{O(L)}$	-10	10	µA
OUTPUT HIGH VOLTAGE LEVEL(I_{OH}=-5mA)		V_{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL(I_{OL}=4.2mA)		V_{OL}	-	0.4	V

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE(T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance [DQ1 - DQ8]	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10%. See notes 1,2)
Test condition: V_{IH}/V_{IL}=2.4V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, output loading C_L=100 pF

Parameter	Symbol	- 5 (*)		- 6		- 7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	135		155		185		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		17		17		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	ns	7,14
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ hold time	tRSH	17		17		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	8	10,000	10	10,000	15	10,000	ns	15
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	33	20	43	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		50		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	

*** - 50ns Product : Output Loading(C_L)=50pF, Vcc=5V ± 5%**

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2)

Parameter	Symbol	-5 (*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		10		15		ns	10
data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-ver. & LL-ver.)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		42		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		95		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		60		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		65		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Hyper page cycle time	tHPC	20		24		29		ns	15
Hyper page read-modify-write cycle time	tHPRWC	62		71		81		ns	15
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	100K	60	100K	70	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		15		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		ns	
Out put buffer turn off delay form $\overline{OE}$	tOEZ	3	13	3	15	3	20	ns	12
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	12
$\overline{W}$ to data delay	tWED	13		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width (LL-ver)	tRASS	100		100		100		µs	13
$\overline{RAS}$ precharge time (LL-ver)	tRPS	90		110		130		ns	13
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		ns	13

*** - 50ns Product : Output Loading(C_L)=50pF, Vcc=5V ± 5%**

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min) the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
13. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.(LL-ver.)
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. tASC ≧ tCPmin , Assume tT = 2.0 ns

512K x 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	tRAC	tCAC	tRC	tHPC
KM48V514B/BL/BLL-6	60ns	17ns	110ns	24ns
KM48V514B/BL/BLL-7	70ns	20ns	130ns	29ns
KM48V514B/BL/BLL-8	80ns	20ns	150ns	34ns

• Fast Page Mode with Extended data out
• Self Refresh operation(LL-ver.)
• $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
• $\overline{RAS}$-only and Hidden refresh capability
• TTL compatible inputs and outputs
• Early Write or output enable controlled write
• Dual +3.3V± 0.3V power supply
• Refresh Cycle
-1024 cycle/16ms (Normal)
-1024 cycle/128ms (L/LL-ver)
• JEDEC Standard pinout
• Available in Plastic SOJ and TSOP(II)

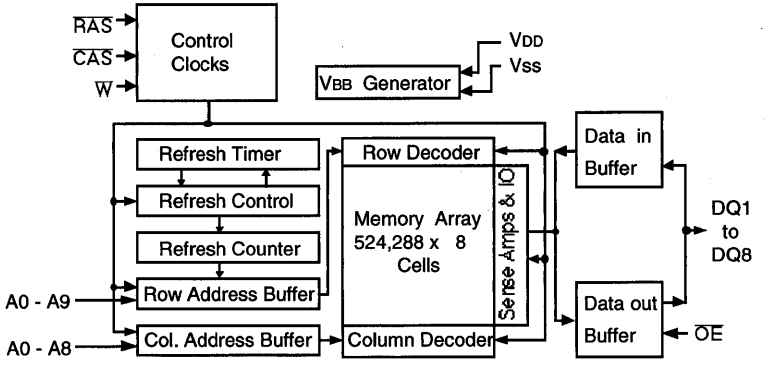
GENERAL DESCRIPTION

The Samsung KM48V514B/BL/BLL is a CMOS high speed 524,288 x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48V514B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48V514B/BL/BLL is fabricated using Samsung's advanced CMOS process.

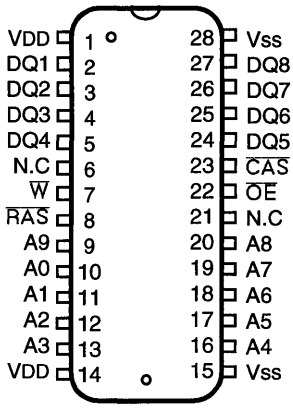
FUNCTIONAL BLOCK DIAGRAM



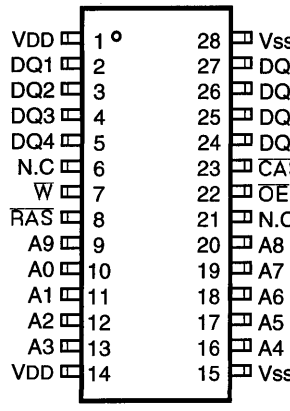
SAMSUNG ELECTRONIC CO., LTD. reserves the right to change products and specifications without notice.

PIN CONFIGURATION (Top Views)

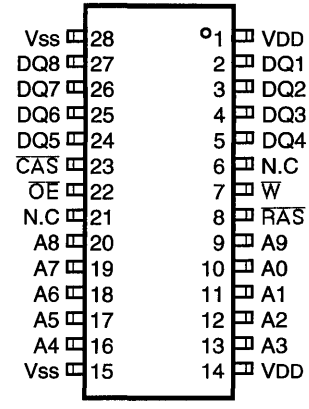
• KM48V514BJ/BLJ/BLLJ



• KM48V514BT/BLT/BLLT



• KM48V514BTR/BLTR/BLLTR



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ1 -8	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{DD}	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	VDD+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM48V514B/BL/BLL-6	I_{CC1}		70	mA
	KM48V514B/BL/BLL-7			65	mA
	KM48V514B/BL/BLL-8			60	mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48V514B	I_{CC2}		1	mA
	KM48V514BL			1	mA
	KM48V514BLL			1	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)	KM48V514B/BL/BLL-6	I_{CC3}		70	mA
	KM48V514B/BL/BLL-7			65	mA
	KM48V514B/BL/BLL-8			60	mA
EDO MODE CURRENT* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$,Address cycling @tPC=min.)	KM48V514B/BL/BLL-6	I_{CC4}		55	mA
	KM48V514B/BL/BLL-7			50	mA
	KM48V514B/BL/BLL-8			45	mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM48V514B	I_{CC5}		500	μA
	KM48V514BL			100	uA
	KM48V514BLL			100	uA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM48V514B/BL/BLL-6	I_{CC6}		70	mA
	KM48V514B/BL/BLL-7			65	mA
	KM48V514B/BL/BLL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$ = 0.2V DQ= Don't Care T_{RC} =125 μS, T_{RAS} =T_{RAS} min.~300 nS	KM48V514BL	I_{CC7}		200	μA
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=V_{IL} $\overline{W}$=$\overline{OE}$=A0-A9=V_{DD}-0.2V or 0.2V DQ1-DQ8=V_{DD}-0.2V, 0.2V or OPEN	KM48V514BLL	I_{CC8}		100	μA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤V_{DD}+0.3V all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤VDD)		$I_{O(L)}$	-10	10	μA
OUTPUT HIGH VOLTAGE LEVEL(I_{OH}=-2mA)		V_{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL(I_{OL}=2mA)		V_{OL}	-	0.4	V

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE(T_A=25°C, VDD=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ1 - DQ8]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V See notes 1,2)
Test Condition : V_{IH}/V_{IL} = 2.1V/0.8V, V_{oh}/V_{ol} = 2.0V/0.8V, Output Loading C_L = 100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		17		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	tRSH	17		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	10	10,000	15	10,000	20	10,000	ns	15
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{DD}=3.3V \pm 0.3V$ See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	15		15		15		ns	10
data hold time referenced to $\overline{RAS}$	tDHR	50		55		60		ns	6
Refresh period(Normal)	tREF		16		16		16	ms	
Refresh period(L-Ver, LL-Ver.)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	42		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Hyper Page cycle time	tHPC	24		29		34		ns	15
Hyper page read-modify-write cycle time	tHPRWC	76		81		91		ns	15
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7,12
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay form $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay form $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7,12
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width(Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	13
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	13
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	13

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min) the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
13. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.(LL-ver.)
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. tASC ≧ tCPmin , Assume tT = 2.0 ns

256K x 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	tRAC	tCAC	tRC	tHPC
KM416C254B/BL/BLL-5	50ns	17ns	90ns	20ns
KM416C254B/BL/BLL-6	60ns	17ns	110ns	24ns
KM416C254B/BL/BLL-7	70ns	20ns	130ns	29ns

• Fast Page Mode with Extended Data Out
• Byte word Read/Write operation
• $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
• $\overline{RAS}$-only and Hidden refresh capability
• Self Refresh operation (LL-ver)
• TTL compatible inputs and outputs
• Early Write or output enable controlled write
• Triple +5V±10% power supply
• Refresh Cycle
  - 512 cycle/8ms (Normal)
  - 512 cycle/64ms (L-version)
  - 512 cycle/128ms (LL-version)
• Power Dissipation
  - Standby : 5.5 mW (Normal)
    1.1 mW (L-version)
    0.83 mW (LL-version)
  - Active(50/60//70) : 605/495/440mW
• JEDEC Standard pinout
• Available in Plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

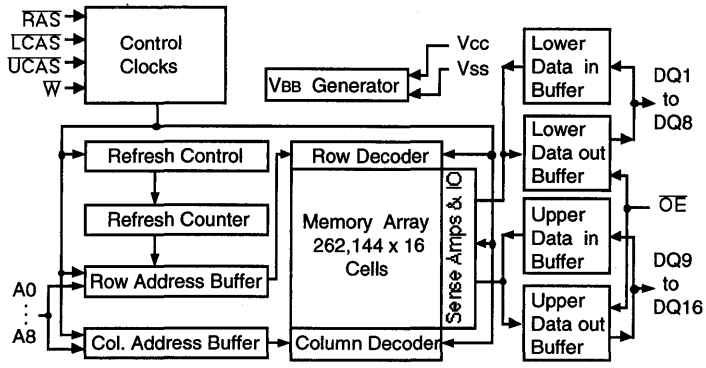
The Samsung KM416C254B/BL/BLL is a CMOS high speed 262,144 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance portable computers.

The KM416C254B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C254B/BL/BLL is fabricated using Samsung's advanced CMOS process.

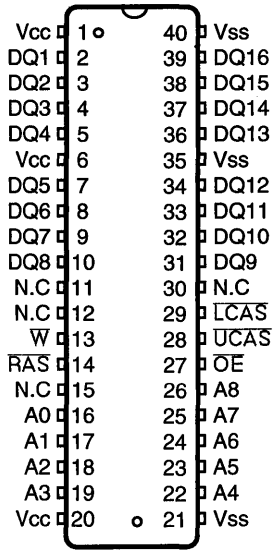
2

FUNCTIONAL BLOCK DIAGRAM

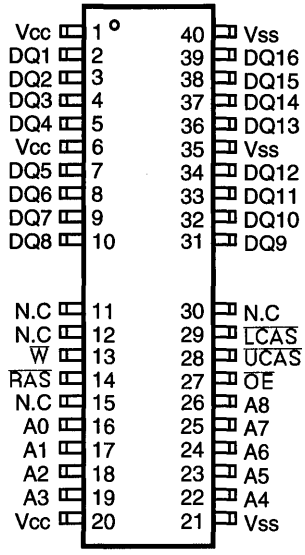


PIN CONFIGURATION (Top Views)

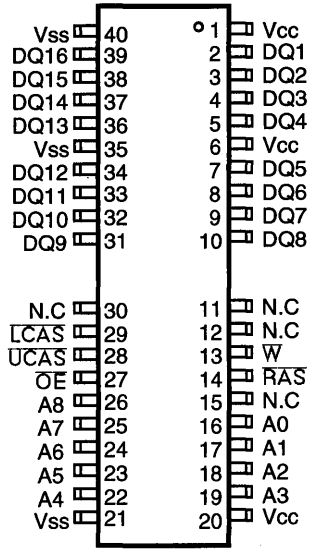
• KM416C254BJ/BLJ/BLLJ



• KM416C254BT/BLT/BLLT



• KM416C254BTR/BLTR/BLLTR



Pin Name	Pin Function
A0 - A8	Address Inputs
DQ1 -16	Data In/Out
Vss	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Outputs Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

KM416C254B Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1 -DQ8	DQ9 - DQ16	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM416C254B/BL/BLL-5	I_{CC1}		110	mA
	KM416C254B/BL/BLL-6			90	mA
	KM416C254B/BL/BLL-7			80	mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})		I_{CC2}		2	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)	KM416C254B/BL/BLL-5	I_{CC3}		110	mA
	KM416C254B/BL/BLL-6			90	mA
	KM416C254B/BL/BLL-7			80	mA
HYPER PAGE MODE CURRENT* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$,Address cycling @tHPC=min.)	KM416C254B/BL/BLL-5	I_{CC4}		70	mA
	KM416C254B/BL/BLL-6			60	mA
	KM416C254B/BL/BLL-7			55	mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=Vcc-0.2V)	KM416C254B	I_{CC5}		1	mA
	KM416C254BL			200	µA
	KM416C254BLL			150	µA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)	KM416C254B/BL/BLL-5	I_{CC6}		110	mA
	KM416C254B/BL/BLL-6			90	mA
	KM416C254B/BL/BLL-7			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH})=Vcc-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$ =0.2V DQ=Don't Care T_{RC} =125 µS(L-ver), T_{RAS} =T_{RAS} min.~300 nS	KM416C254BL	I_{CC7}		300	µA
Self Refresh Current $\overline{RAS}$ = $\overline{CAS}$ = 0.2V $\overline{W}$ = $\overline{OE}$ = A0 ~ A8 = Vcc-0.2V or 0.2V DQ1~16 = Vcc-0.2V, 0.2V or OPEN	KM416C254BLL	I_{CC8}		200	µA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤Vcc+0.5V all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	µA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤Vcc)		$I_{O(L)}$	-10	10	µA
OUTPUT HIGH VOLTAGE LEVEL(I_{OH}=-5mA)		V_{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL(I_{OL}=4.2mA)		V_{OL}	-	0.4	V

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper page cycle.

CAPACITANCE(T_A=25°C, V_{CC}=5.0V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ1 - DQ16]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2)
Test condition: V_{IH}/V_{IL}=2.4V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, output loading C_L=100 pF

Parameter	Symbol	-5 (*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	135		155		185		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		17		17		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	ns	7,14
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	17		17		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	ns	12
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	15
Column address hold time	tCAH	8		10		15		ns	15
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		50		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	18

*** - 50ns Product : Output Loading(C_L)=50pF, Vcc=5V ± 5%**

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$. See notes 1,2)

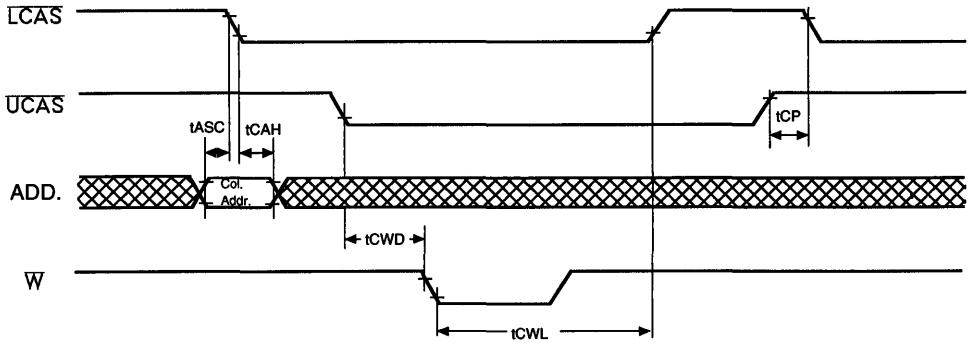
Parameter	Symbol	-5 (*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	10,21
Data hold time	tDH	10		10		15		ns	10,21
data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		ns	6
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-version)	tREF		64		64		64	ms	
Refresh period (LL-version)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		42		50		ns	8,17
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		95		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Hyper page cycle time	tHPC	20		24		29		ns	12
Hyper page read-modify-write cycle time	tHPRWC	62		71		86		ns	12
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		ns	16
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	100K	60	100K	70	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		15		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		ns	
Out put buffer turn off delay form $\overline{OE}$	tOEZ	3	13	3	15	3	20	ns	7
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	15	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	7
$\overline{W}$ to data delay	tWED	13		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width(Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width (LL-ver)	tRASS	100		100		100		us	13
$\overline{RAS}$ precharge time (LL-ver)	tRPS	90		110		130		ns	13
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		ns	13

*** - 50ns Product : Output Loading(C_L)=50pF, Vcc=5V $\pm$ 5%**

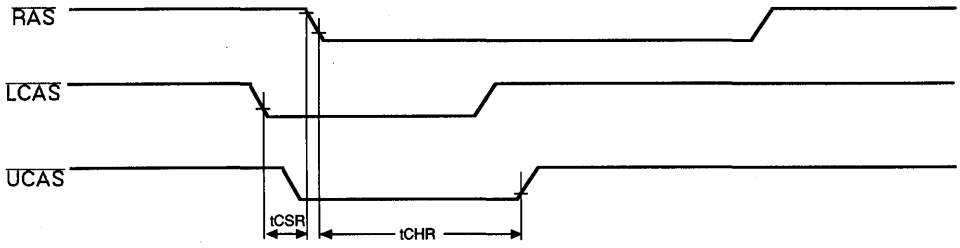
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min) the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the W leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. tASC ≧ tCPmin , Assume tT = 2.0 ns
13. 512 cycle of burst refresh must be executed within 8ms before and after self refresh, in order to meet refresh specification.(LL-ver.)
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
16. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
17. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

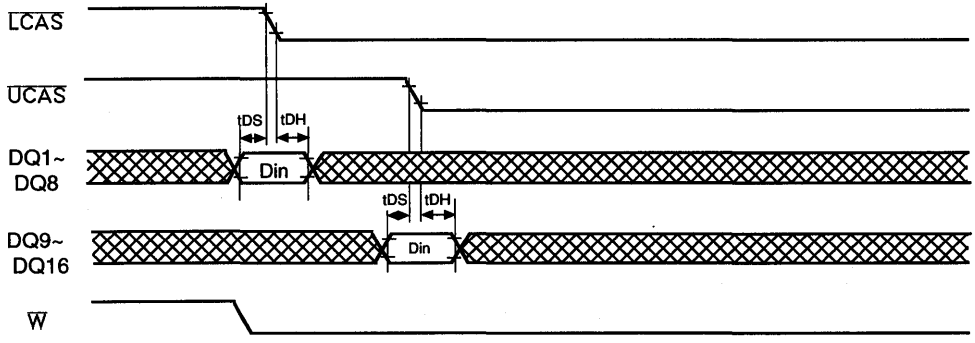
18. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



19. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
20. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



21. tDS, tDH is independently specified for lower byte D_{IN}(1~8), upper byte D_{IN}(9~16).



256K x 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	tRAC	tCAC	tRC	tHPC
KM416V254B/BL/BLL-6	60ns	17ns	110ns	24ns
KM416V254B/BL/BLL-7	70ns	20ns	130ns	29ns
KM416V254B/BL/BLL-8	80ns	20ns	150ns	34ns

• Fast Page Mode with Extended Data Out
• Byte word Read/Write operation
• $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
• $\overline{RAS}$-only and Hidden refresh capability
• Self Refresh operation(LL-ver)
• TTL compatible inputs and outputs
• Early Write or output enable controlled write
• Triple +3.3V±0.3V power supply
• Refresh Cycle
  - 512 cycle/8ms (Normal)
  - 512 cycle/64ms (L-ver)
  - 512 cycle/128ms (LL-ver)
• Power Dissipation
  - Standby : 5.5 mW (Normal)
    1.1 mW (L-ver)
    0.83 mW (LL-ver)
  - Active(60/70/80) : 495/440/413 mW
• JEDEC Standard pinout
• Available in Plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

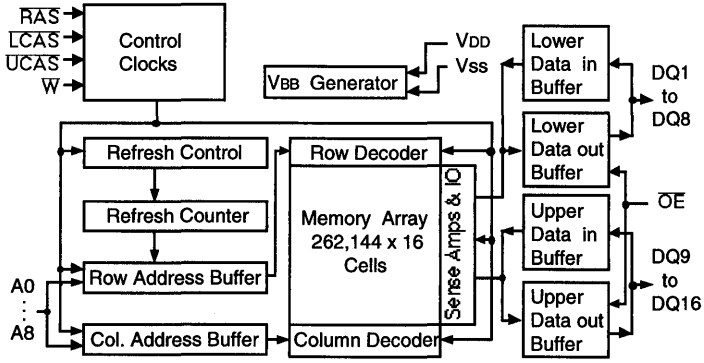
The Samsung KM416V254B/BL/BLL is a CMOS high speed 262,144 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance portable computers.

The KM416V254B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416V254B/BL/BLL is fabricated using Samsung's advanced CMOS process.

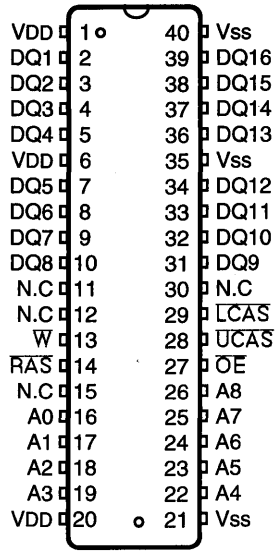
2

FUNCTIONAL BLOCK DIAGRAM

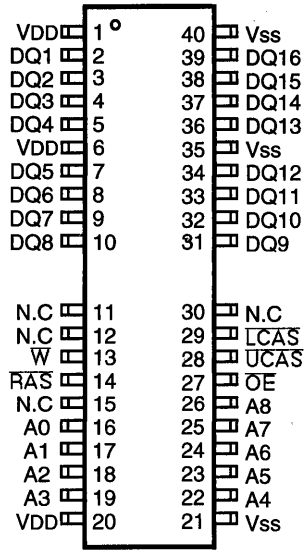


PIN CONFIGURATION (Top Views)

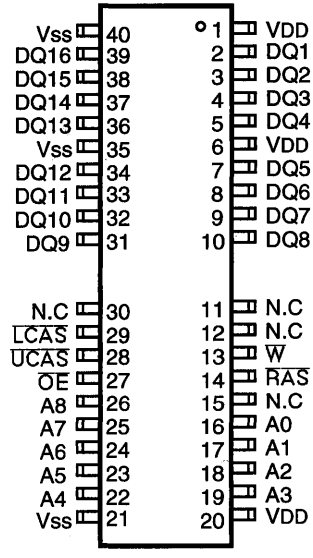
• KM416V254BJ/BLJ/BLLJ



• KM416V254BT/BLT/BLLT



• KM416V254BTR/BLTR/BLLTR



Pin Name	Pin Function
A0 - A8	Address Inputs
DQ1 -16	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{DD}	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 ~ 4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	VDD+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

KM416V254B Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1 -DQ8	DQ9 - DQ16	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM416V254B/BL/BLL-6 KM416V254B/BL/BLL-7 KM416V254B/BL/BLL-8	I_{CC1}		90 80 75	mA mA mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})	KM416V254B KM416V254BL KM416V254BLL	I_{CC2}		1 1 1	mA mA mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)	KM416V254B/BL/BLL-6 KM416V254B/BL/BLL-7 KM416V254B/BL/BLL-8	I_{CC3}		90 80 75	mA mA mA
HYPER PAGE MODE CURRENT* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$,Address cycling @tHPC=min.)	KM416V254B/BL/BLL-6 KM416V254B/BL/BLL-7 KM416V254B/BL/BLL-8	I_{CC4}		85 75 70	mA mA mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{DD}-0.2V)	KM416V254B KM416V254BL KM416V254BLL	I_{CC5}		500 100 100	uA µA µA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)	KM416V254B/BL/BLL-6 KM416V254B/BL/BLL-7 KM416V254B/BL/BLL-8	I_{CC6}		90 80 75	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH})=V_{DD}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$ = 0.2V DQ =Don't Care T_{RC} =125 µS(L-ver), T_{RAS} =T_{RAS} min.~300 nS	KM416V254BL	I_{CC7}		200	µA
Self Refresh Current $\overline{RAS}$ = $\overline{CAS}$ = 0.2V $\overline{W}$ = $\overline{OE}$ = A0 ~ A8 = V_{DD}-0.2V or 0.2V DQ1~16 = V_{DD}-0.2V, 0.2V or OPEN	KM416V254BLL	I_{CCS}		100	µA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤VDD+0.3V all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	µA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤VDD)		$I_{O(L)}$	-10	10	µA
OUTPUT HIGH VOLTAGE LEVEL(I_{OH}=-2mA)		V_{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL(I_{OL}= 2mA)		V_{OL}	-	0.4	V

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper page cycle.

CAPACITANCE(T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ1 - DQ16]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

Test Condition : V_{IH}/V_{IL} = 2.1V/0.8V, V_{OH}/V_{OL} = 2.0V/0.8V, Output Loading C_L = 100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		17		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	15	3	20	3	20	ns	7
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	tRSH	17		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	10	10,000	15	10,000	20	10,000	ns	12
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	14
Column address hold time	tCAH	10		15		15		ns	14
Column address hold time referenced to $\overline{RAS}$	tAR	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	18

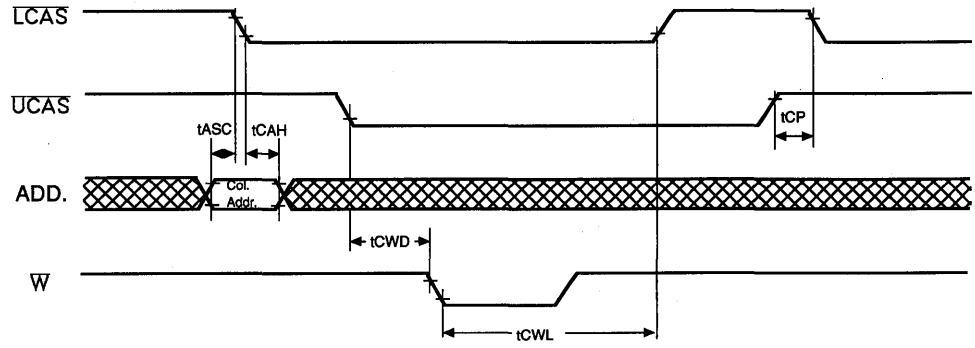
AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, V_{DD}=3.3V±0.3V, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	10,21
Data hold time	tDH	15		15		15		ns	10,21
data hold time referenced to $\overline{RAS}$	tDHR	50		55		60		ns	6
Refresh period(Normal)	tREF		8		8		8	ms	
Refresh period(L-Ver.)	tREF		64		64		64	ms	
Refresh period(LL-ver.)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	42		50		50		ns	8,16
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Hyper Page cycle time	tHPC	24		29		34		ns	12
Hyper page read-modify-write cycle time	tHPRWC	76		81		91		ns	
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	10		10		10		ns	15
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Out put buffer turn off delay from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay form $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	7,13
Output buffer turn off delay form $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width(Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	17
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	17
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	17

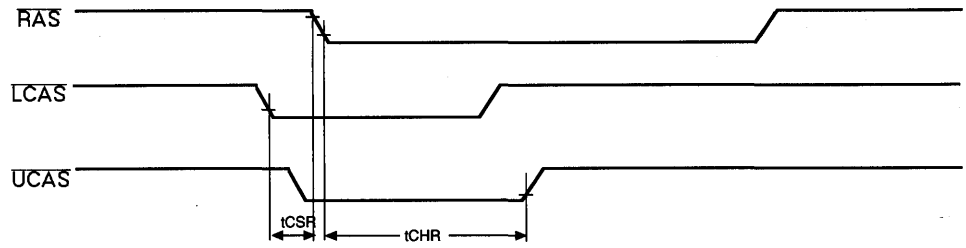
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min) the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. tASC ≧ tCPmin , Assume tT = 2.0 ns
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
14. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
15. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
16. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
17. 512 cycle of burst refresh must be executed within 8ms before and after self refresh, in order to meet refresh specification.(LL-ver.)

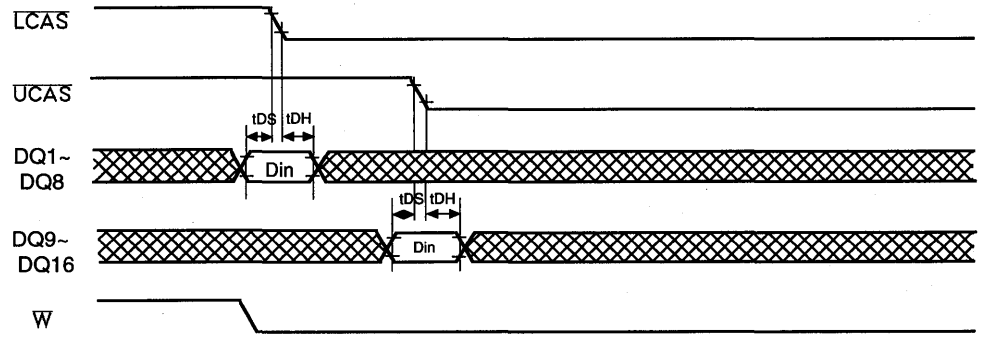
18. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



19. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
20. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



21. tDS, tDH is independently specified for lower byte D_{IN}(1~8), upper byte D_{IN}(9~16).



4M x 4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	tRAC	tCAC	tRC	tHPC
KM44C40(1)04A/AL/ALL/ASL-5	50ns	13ns	90ns	20ns
KM44C40(1)04A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44C40(1)04A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44C40(1)04A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- KM44C4004A/AL/ALL/ASL(4K Product)
- KM44C4104A/AL/ALL/ASL(2K Product)
- Fast Page Mode with Extended data out
- Self Refresh Operation(LL-Ver. only)
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Single +5V±10% power supply
- 4096 cycle/64ms refresh(normal DRAM)
- 4096 cycle/128ms refresh(Low power & self ref.)
- 4096 cycle/256ms refresh(Super low power)
- 2048 cycle/32ms refresh(normal DRAM)
- 2048 cycle/128ms refresh(Low power & self ref.)
- 2048 cycle/256ms refresh(Super low power)
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

The Samsung KM44C40(1)04A/AL/ALL/ASL is a CMOS high speed 4,194,304 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and minicomputers, graphics and high performance portable computers.

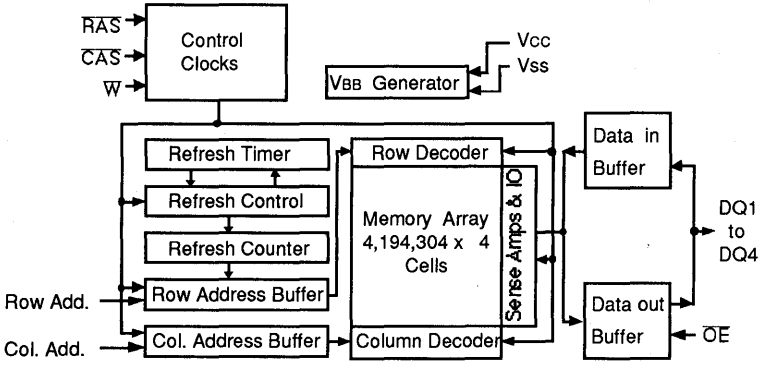
The KM44C40(1)04A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C40(1)04A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

ADDRESS

ADD \ Prod.	KM44C4004A(4K)	KM44C4104A(2K)
Row Add.	A0 - A11	A0 - A10
Col. Add.	A0 - A9	A0 - A10

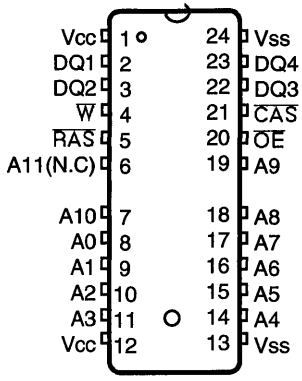
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

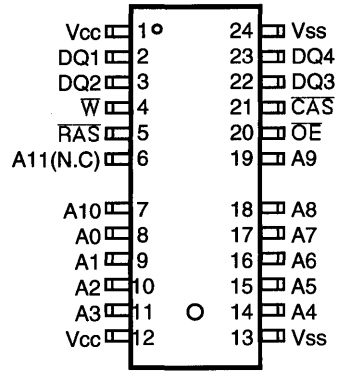
* Note : ( ) --> 2K Product

• KM44C40(1)04AJ/ALJ/ALLJ/ASLJ /AK/ALK/ALLK/ASLK



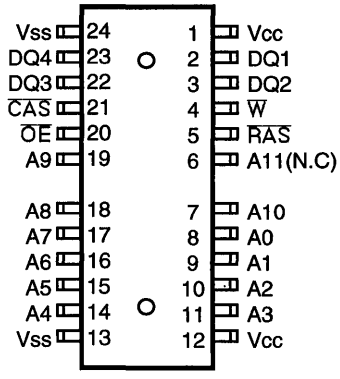
J : 400MIL
K: 300MIL

• KM44C40(1)04AT/ALT/ALLT/ASLT /AS/ALS/ALLS/ASLS



T: 400MIL(Forward)
S: 300MIL(Forward)

• KM44C40(1)04ATR/ALTR/ALLTR/ASLTR /ASR/ALSR/ALLSR/ASLSR



TR: 400MIL(Reverse)
SR: 300MIL(Reverse)

Pin Name	Pin Function
A0 - A11	Address Inputs(4K Product)
A0 - A10	Address Inputs(2K Product)
DQ1 -4	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{CC}	Power(+5V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM44C40(1)04A/AL/ALL/ASL-5	I_{CC1}		90(110)	mA
	KM44C40(1)04A/AL/ALL/ASL-6			80(100)	mA
	KM44C40(1)04A/AL/ALL/ASL-7			70(90)	mA
	KM44C40(1)04A/AL/ALL/ASL-8			60(80)	mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44C40(1)04A	I_{CC2}		2	mA
	KM44C40(1)04AL			1	mA
	KM44C40(1)04ALL			1	mA
	KM44C40(1)04ASL			1	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)	KM44C40(1)04A/AL/ALL/ASL-5	I_{CC3}		90(110)	mA
	KM44C40(1)04A/AL/ALL/ASL-6			80(100)	mA
	KM44C40(1)04A/AL/ALL/ASL-7			70(90)	mA
	KM44C40(1)04A/AL/ALL/ASL-8			60(80)	mA
EDO MODE CURRENT* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$,Address cycling @tHPC=min.)	KM44C40(1)04A/AL/ALL/ASL-5	I_{CC4}		130(140)	mA
	KM44C40(1)04A/AL/ALL/ASL-6			110(120)	mA
	KM44C40(1)04A/AL/ALL/ASL-7			95(105)	mA
	KM44C40(1)04A/AL/ALL/ASL-8			80(90)	mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)	KM44C40(1)04A	I_{CC5}		1	mA
	KM44C40(1)04AL			300	µA
	KM44C40(1)04ALL			200	µA
	KM44C40(1)04ASL			200	µA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM44C40(1)04A/AL/ALL/ASL-5	I_{CC6}		90(110)	mA
	KM44C40(1)04A/AL/ALL/ASL-6			80(100)	mA
	KM44C40(1)04A/AL/ALL/ASL-7			70(90)	mA
	KM44C40(1)04A/AL/ALL/ASL-8			60(80)	mA
Battery back-up current Average power supply current Battery back-up mode Input high voltage(V_{IH})=Vcc-0.2V Input low voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V DQ1-DQ4 = Don't care tRC(4K/2K)= 31.25/62.5µs(L-ver), 62.5/125µs(SL-ver) tRAS=tRASmin~300 ns	KM44C40(1)04AL	I_{CC7}		450(400)	µA
	KM44C40(1)04ASL			350(300)	µA
Self refresh current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A0 ~ A11(A10) = Vcc-0.2V or 0.2V DQ1 ~ DQ4= Vcc-0.2V, 0.2V or open	KM44C40(1)04ALL	I_{CC8}		300	µA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤Vcc+0.5V all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	µA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤Vcc)		$I_{O(L)}$	-10	10	µA
OUTPUT HIGH VOLTAGE LEVEL(I_{OH}=-5mA)		V_{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL(I_{OL}=4.2mA)		V_{OL}	-	0.4	V

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper page cycle.

CAPACITANCE(T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11(A10)]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ1 - DQ4]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10% See notes 1,2)
Test condition: V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100 pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	7,15
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	38		45		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC}=5.0V \pm 10\%$ See notes 1,2)

Test condition: $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading $C_L=100$ pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period[Normal(2K)]	tREF		64(32)		64(32)		64(32)		64(32)	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Refresh period(SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	62		71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	7
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write commend set-up time(Test mode in)	tWTS	10		10		10		10		ns	12
Write commend hold time(Test mode in)	tWTH	10		10		10		10		ns	12
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	7,15
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	7
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width(Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width (LL-ver)	tRASS	100		100		100		100		us	16
$\overline{RAS}$ precharge time (LL-ver)	tRPS	90		110		130		150		ns	16
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		-50		ns	16

SAMSUNG ELECTRONICS

TEST MODE CYCLE

(Note. 12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	tHPC	25		29		34		39		ns	
Hyper Page read-modify-write cycle time	tHPRWC	67		76		91		101		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

TEST MODE DESCRIPTI ON

The KM44C40(1)04A/AL/ALL/ASL is the CMOS DRAM organized 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4Mx4 DRAM can be tested as if it were a 1Mx4 DRAM. $\overline{W}$ and $\overline{CAS}$ **before** $\overline{RAS}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", . And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time(1/4 in cases of N test pattern).

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min) the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
16. 4096(2048) cycle of burst refresh must be executed within 64(32) ms before and after self refresh, in order to meet refresh specification.
17. tASC ≧ tCPmin , Assume tT = 2.0 ns

4M x 4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	tRAC	tCAC	tRC	tHPC
KM44V40(1)04A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44V40(1)04A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44V40(1)04A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- KM44V4004A/AL/ALL/ASL(4K Product)
- KM44V4104A/AL/ALL/ASL(2K Product)
- Fast Page Mode with Extended data out
- Self Refresh Operation(LL-Ver. only)
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Fast parallel test mode capability
- LVTTL compatible inputs and outputs
- Early Write or output enable controlled write
- Single +3.3V±0.3V power supply
- 4096 cycle/64ms refresh(normal DRAM)
- 4096 cycle/128ms refresh(Low power & self ref.)
- 4096 cycle/256ms refresh(Super low power)
- 2048 cycle/32ms refresh(normal DRAM)
- 2048 cycle/128ms refresh(Low power & self ref.)
- 2048 cycle/256ms refresh(Super low power)
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

The Samsung KM44V40(1)04A/AL/ALL/ASL is a CMOS high speed 4,194,304 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and minicomputers, graphics and high performance portable computers.

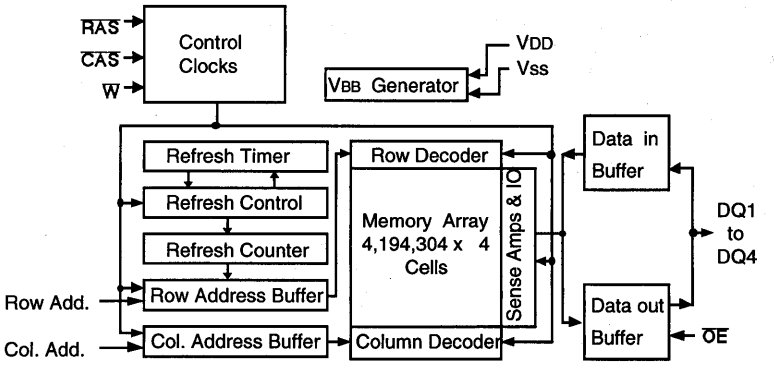
The KM44V40(1)04A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44V40(1)04A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

ADDRESS

ADD \ Prod.	KM44V4004A(4K)	KM44V4104A(2K)
Row Add.	A0 - A11	A0 - A10
Col. Add.	A0 - A9	A0 - A10

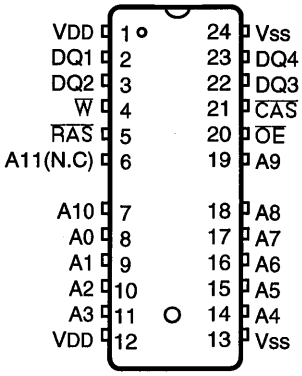
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

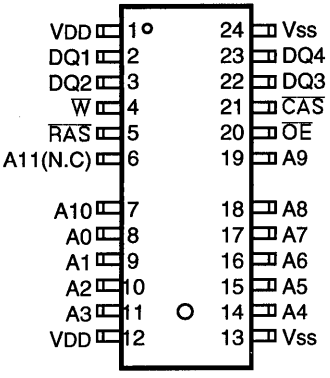
* Note : ( ) --> 2K Product

• KM44V40(1)04AJ/ALJ/ALLJ/ASLJ /AK/ALK/ALLK/ASLK



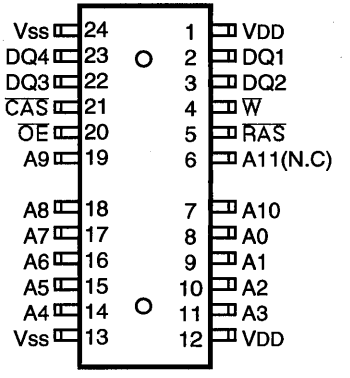
J : 400MIL
K: 300MIL

• KM44V40(1)04AT/ALT/ALLT/ASLT /AS/ALS/ALLS/ASLS



T: 400MIL(Forward)
S: 300MIL(Forward)

• KM44V40(1)04ATR/ALTR/ALLTR/ASLTR /ASR/ALSR/ALLSR/ASLSR



TR: 400MIL(Reverse)
SR: 300MIL(Reverse)

Pin Name	Pin Function
A0 - A11	Address Inputs(4K Product)
A0 - A10	Address Inputs(2K Product)
DQ1 -4	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{DD}	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	VDD+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM44V40(1)04A/AL/ALL/ASL-6	I_{CC1}		80(100)	mA
	KM44V40(1)04A/AL/ALL/ASL-7			70(90)	mA
	KM44V40(1)04A/AL/ALL/ASL-8			60(80)	mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM44V40(1)04A	I_{CC2}		2	mA
	KM44V40(1)04AL			1	mA
	KM44V40(1)04ALL			1	mA
	KM44V40(1)04ASL			1	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)	KM44V40(1)04A/AL/ALL/ASL-6	I_{CC3}		80(100)	mA
	KM44V40(1)04A/AL/ALL/ASL-7			70(90)	mA
	KM44V40(1)04A/AL/ALL/ASL-8			60(80)	mA
EDO MODE CURRENT* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$,Address cycling @tHPC=min.)	KM44V40(1)04A/AL/ALL/ASL-6	I_{CC4}		100(125)	mA
	KM44V40(1)04A/AL/ALL/ASL-7			90(105)	mA
	KM44V40(1)04A/AL/ALL/ASL-8			80(90)	mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM44V40(1)04A	I_{CC5}		1	mA
	KM44V40(1)04AL			300	µA
	KM44V40(1)04ALL			200	µA
	KM44V40(1)04ASL			200	µA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM44V40(1)04A/AL/ALL/ASL-6	I_{CC6}		80(100)	mA
	KM44V40(1)04A/AL/ALL/ASL-7			70(90)	mA
	KM44V40(1)04A/AL/ALL/ASL-8			60(80)	mA
Battery back-up current Average power supply current Battery back-up mode Input high voltage(V_{IH})=V_{DD}-0.2V Input low voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V DQ1 ~ DQ4 = Don't care tRC(4K/2K)= 31.25/62.5µs(L-ver), 62.5/125µs(SL-ver) tRAS=tRASmin~300 ns	KM44V40(1)04AL	I_{CC7}		450(400)	µA
	KM44V40(1)04ASL			350(300)	µA
Self refresh current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A0 ~ A11(A10) = V_{DD}-0.2V or 0.2V DQ1 ~ DQ4= V_{DD}-0.2V, 0.2V or open	KM44V40(1)04ALL	I_{CCS}		250	µA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤V_{DD}+0.3V all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	µA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤V_{DD})		$I_{O(L)}$	-10	10	µA
OUTPUT HIGH VOLTAGE LEVEL(I_{OH}=-2mA)		V_{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL(I_{OL}=2mA)		V_{OL}	-	0.4	V

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE(T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11(A10)]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ1 - DQ4]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)
Test condition : V_{IH}/V_{IL} = 2.0V/0.8V, V_{OH}/V_{OL} = 2.0V/0.8V, output loading C_L = 100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	15	3	20	3	20	ns	7,15
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	45		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		55		60		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	10		15		20		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, V_{DD}=3.3V±0.3V See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		15		15		ns	10
data hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period [4K(2K)]	tREF		64(32)		64(32)		64(32)	ms	
Refresh period(Low power & self refresh)	tREF		128		128		128	ms	
Refresh period(Super low power)	tREF		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		65		70		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		70		75		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		30		30		ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Hyper Page cycle time	tHPC	24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Out put buffer turn off delay from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7,14
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
Write command set-up time (test mode in)	tWTS	10		10		10		ns	
Write command hold time (test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	7,15
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width(Hyper Page Cycle)	tWPE	5		5		5		ns	

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{DD}=3.3V \pm 0.3V$ See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay form $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	7,14,15
Output buffer turn off delay form $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{RAS}$ pulse width (LL-Ver)	tRASS	100		100		100		µs	16
$\overline{RAS}$ precharge time (LL-Ver)	tRPS	110		130		150		ns	16
$\overline{CAS}$ hold time (LL-Ver)	tCHS	-50		-50		-50		ns	16

TEST MODE CYCLE (Note. 12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	50		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Hyper Page cycle time	tHPC	29		34		39		ns	
Hyper page read-modify-write cycle time	tHPRWC	76		91		101		ns	
$\overline{RAS}$ pulse width (EDO Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time form $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

TEST MODE DESCRIPTI ON

The KM44V40(1)04A/AL/ALL/ASL is the CMOS DRAM organized 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4Mx4 DRAM can be tested as if it were a 1Mx4 DRAM. **$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$** Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", . And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time(1/4 in cases of N test pattern).

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min) the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
16. 4096(2048) cycle of burst refresh must be executed within 64(32) ms before and after self refresh, in order to meet refresh specification.
17. tASC ≥ tCPmin , Assume tT = 2.0 ns

2M x 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	tRAC	tCAC	tRC	tHPC
KM48C20(1)04A/AL/ALL/ASL-5	50ns	13ns	90ns	20ns
KM48C20(1)04A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM48C20(1)04A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM48C20(1)04A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- KM48C2004A/AL/ALL/ASL(4K Product)
- KM48C2104A/AL/ALL/ASL(2K Product)
- Fast Page Mode with Extended data out
- Self Refresh Operation(LL-Ver. only)
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Single +5V±10% power supply
- 4096 cycle/64ms refresh(normal DRAM)
- 4096 cycle/128ms refresh(Low power & self ref.)
- 4096 cycle/256ms refresh(Super low power)
- 2048 cycle/32ms refresh(normal DRAM)
- 2048 cycle/128ms refresh(Low power & self ref.)
- 2048 cycle/256ms refresh(Super low power)
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

The Samsung KM48C20(1)04A/AL/ALL/ASL is a CMOS high speed 2,097,152 x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and minicomputers, graphics and high performance portable computers.

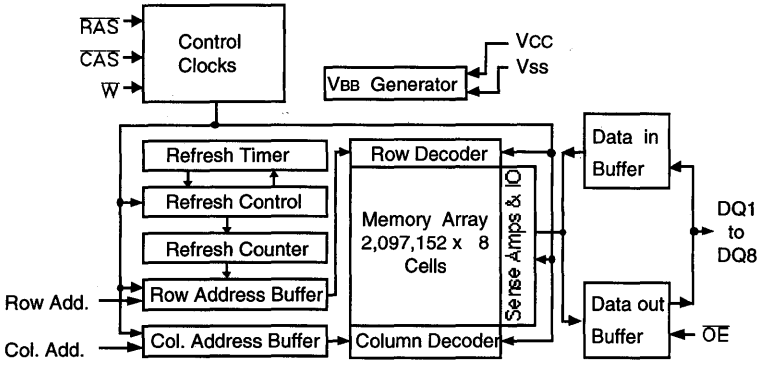
The KM48C20(1)04A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48C20(1)04A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

ADDRESS

ADD \ Prod.	KM48C2004A(4K)	KM48C2104A(2K)
Row Add.	A0 - A11	A0 - A10
Col. Add.	A0 - A8	A0 - A9

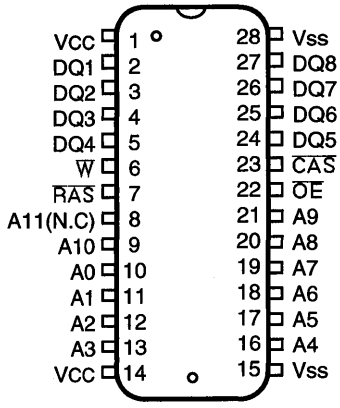
FUNCTIONAL BLOCK DIAGRAM



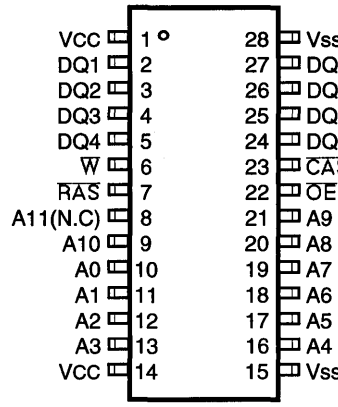
PIN CONFIGURATION (Top Views)

* Note : ( ) --> 2K Product

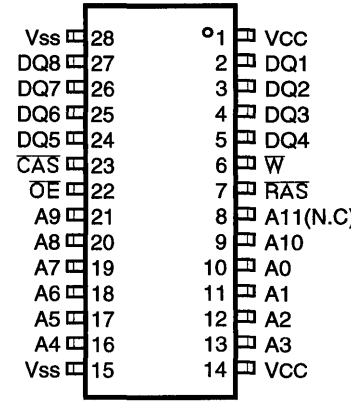
• KM48C20(1)04AJ/ALJ/ALLJ/ASLJ



• KM48C20(1)04AT/ALT/ALLT/ASLT



• KM48C20(1)04ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A0 - A11	Address Inputs(4K Product)
A0 - A10	Address Inputs(2K Product)
DQ1 -8	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM48C20(1)04A/AL/ALL/ASL-5	I_{CC1}		90(110)	mA
	KM48C20(1)04A/AL/ALL/ASL-6			80(100)	mA
	KM48C20(1)04A/AL/ALL/ASL-7			70(90)	mA
	KM48C20(1)04A/AL/ALL/ASL-8			60(80)	mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48C20(1)04A	I_{CC2}		2	mA
	KM48C20(1)04AL			1	mA
	KM48C20(1)04ALL			1	mA
	KM48C20(1)04ASL			1	mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)	KM48C20(1)04A/AL/ALL/ASL-5	I_{CC3}		90(110)	mA
	KM48C20(1)04A/AL/ALL/ASL-6			80(100)	mA
	KM48C20(1)04A/AL/ALL/ASL-7			70(90)	mA
	KM48C20(1)04A/AL/ALL/ASL-8			60(80)	mA
EDO MODE CURRENT* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$,Address cycling @tHPC=min.)	KM48C20(1)04A/AL/ALL/ASL-5	I_{CC4}		130(140)	mA
	KM48C20(1)04A/AL/ALL/ASL-6			110(120)	mA
	KM48C20(1)04A/AL/ALL/ASL-7			95(105)	mA
	KM48C20(1)04A/AL/ALL/ASL-8			80(90)	mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)	KM48C20(1)04A	I_{CC5}		1	mA
	KM48C20(1)04AL			300	µA
	KM48C20(1)04ALL			200	µA
	KM48C20(1)04ASL			200	µA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM48C20(1)04A/AL/ALL/ASL-5	I_{CC6}		90(110)	mA
	KM48C20(1)04A/AL/ALL/ASL-6			80(100)	mA
	KM48C20(1)04A/AL/ALL/ASL-7			70(90)	mA
	KM48C20(1)04A/AL/ALL/ASL-8			60(80)	mA
Battery back-up current Average power supply current Battery back-up mode Input high voltage(V_{IH})=Vcc-0.2V Input low voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V DQ1 ~ DQ8 = Don't care tRC(4K/2K)= 31.25/62.5µs(L-ver), 62.5/125µs(SL-ver) tRAS=tRASmin~300 ns	KM48C20(1)04AL	I_{CC7}		450(400)	µA
	KM48C20(1)04ASL			350(300)	µA
Self refresh current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A0 ~ A11(A10) = Vcc-0.2V or 0.2V DQ1 ~ DQ8= Vcc-0.2V, 0.2V or open	KM48C20(1)04ALL	I_{CCS}		300	µA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤Vcc + 0.5V all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	µA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤Vcc)		$I_{O(L)}$	-10	10	µA
OUTPUT HIGH VOLTAGE LEVEL(I_{OH}=-5mA)		V_{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL(I_{OL}=4.2mA)		V_{OL}	-	0.4	V

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper page cycle.

CAPACITANCE(T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11(A10)]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ1 - DQ8]	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC}=5.0V±10% See notes 1,2)
Test condition: V_{ih}/V_{il}=2.4V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, output loading C_L=100 pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	7,14,15
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	38		45		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	16
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$ See notes 1,2)

Test condition: $V_{ih}/V_{il}=2.4/0.8V$, $V_{oh}/V_{ol}=2.0/0.8V$, output loading $C_L=100$ pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period[Normal(2K)]	tREF		64(32)		64(32)		64(32)		64(32)	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Refresh period(SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	62		71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	7,14
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write commend set-up time(Test mode in)	tWTS	10		10		10		10		ns	12
Write commend hold time(Test mode in)	tWTH	10		10		10		10		ns	12
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	7,14,15
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width(Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width (LL-ver)	tRASS	100		100		100		100		us	16
$\overline{RAS}$ precharge time (LL-ver)	tRPS	90		110		130		150		ns	16
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		-50		ns	16

TEST MODE CYCLE

(Note. 12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	tHPC	25		29		34		39		ns	
Hyper Page read-modify-write cycle time	tHPRWC	67		76		91		101		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

TEST MODE DESCRIPTI ON

The KM48C20(1)04A/AL/ALL/ASL is the CMOS DRAM organized 2,097,152 words by 8 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4Mx4 DRAM can be tested as if it were a 1Mx8 DRAM. **$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$** Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", . And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time(1/2 in cases of N test pattern).

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min) the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
16. 4096(2048) cycle of burst refresh must be executed within 64(32) ms before and after self refresh, in order to meet refresh specification.
17. tASC ≥ tCPmin , Assume tT = 2.0 ns

2M x 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	tRAC	tCAC	tRC	tHPC
KM48V20(1)04A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM48V20(1)04A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM48V20(1)04A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

• KM48V2004A/AL/ALL/ASL(4K Product)
• KM48V2104A/AL/ALL/ASL(2K Product)
• Fast Page Mode with Extended data out
• Self Refresh Operation(LL-Ver. only)
• $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
• $\overline{RAS}$-only and Hidden refresh capability
• Fast parallel test mode capability
• LVTTL compatible inputs and outputs
• Early Write or output enable controlled write
• Single +3.3V±0.3V power supply
• 4096 cycle/64ms refresh(normal DRAM)
• 4096 cycle/128ms refresh(Low power & self ref.)
• 4096 cycle/256ms refresh(Super low power)
• 2048 cycle/32ms refresh(normal DRAM)
• 2048 cycle/128ms refresh(Low power & self ref.)
• 2048 cycle/256ms refresh(Super low power)
• JEDEC Standard pinout
• Available in Plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

The Samsung KM48V20(1)04A/AL/ALL/ASL is a CMOS high speed 2,097,152 x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and minicomputers, graphics and high performance portable computers.

The KM48V20(1)04A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$ -before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

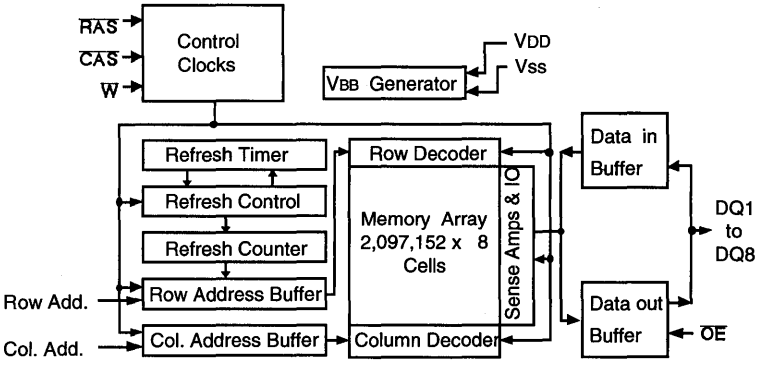
The KM48V20(1)04A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

2

ADDRESS

ADD \ Prod.	KM48V2004A(4K)	KM48V2104A(2K)
Row Add.	A0 - A11	A0 - A10
Col. Add.	A0 - A8	A0 - A9

FUNCTIONAL BLOCK DIAGRAM

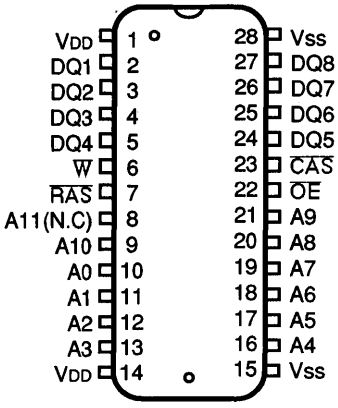


SAMSUNG ELECTRONICS

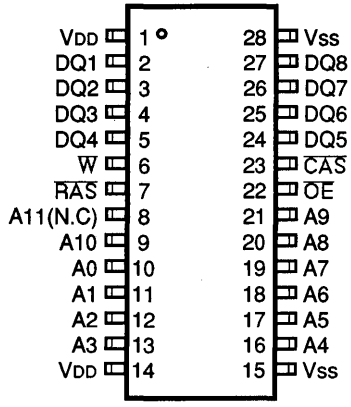
PIN CONFIGURATION (Top Views)

* Note : ( ) --> 2K Product

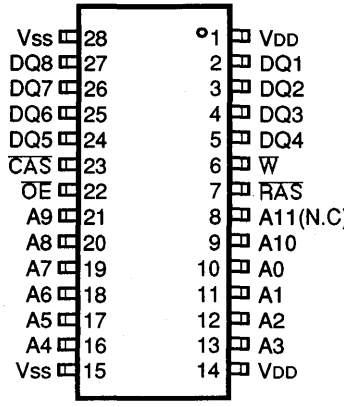
• KM48V20(1)04AJ/ALJ/ALLJ/ASLJ



• KM48V20(1)04AT/ALT/ALLT/ASLT



• KM48V20(1)04ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A0 - A11	Address Inputs(4K Product)
A0 - A10	Address Inputs(2K Product)
DQ1 -8	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
VDD	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	VDD+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
OPERATING CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM48V20(1)04A/AL/ALL/ASL-6 KM48V20(1)04A/AL/ALL/ASL-7 KM48V20(1)04A/AL/ALL/ASL-8	I_{CC1}		80(100) 70(90) 60(80)	mA mA mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})	KM48V20(1)04A KM48V20(1)04AL KM48V20(1)04ALL KM48V20(1)04ASL	I_{CC2}		2 1 1 1	mA mA mA mA
$\overline{RAS}$-ONLY REFRESH CURRENT* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)	KM48V20(1)04A/AL/ALL/ASL-6 KM48V20(1)04A/AL/ALL/ASL-7 KM48V20(1)04A/AL/ALL/ASL-8	I_{CC3}		80(100) 70(90) 60(80)	mA mA mA
EDO MODE CURRENT* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$,Address cycling @tHPC=min.)	KM48V20(1)04A/AL/ALL/ASL-6 KM48V20(1)04A/AL/ALL/ASL-7 KM48V20(1)04A/AL/ALL/ASL-8	I_{CC4}		100(125) 90(105) 80(90)	mA mA mA
STANDBY CURRENT ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{DD}-0.2V)	KM48V20(1)04A KM48V20(1)04AL KM48V20(1)04ALL KM48V20(1)04ASL	I_{CC5}		1 300 200 200	mA µA µA µA
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)	KM48V20(1)04A/AL/ALL/ASL-6 KM48V20(1)04A/AL/ALL/ASL-7 KM48V20(1)04A/AL/ALL/ASL-8	I_{CC6}		80(100) 70(90) 60(80)	mA mA mA
Battery back-up current Average power supply current Battery back-up mode Input high voltage(V_{IH})=V_{DD}-0.2V Input low voltage(V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V DQ1 ~ DQ8 = Don't care tRC(4K/2K)= 31.25/62.5µs(L-ver), 62.5/125µs(SL-ver) tRAS=tRASmin~300 ns	KM48V20(1)04AL KM48V20(1)04ASL	I_{CC7}		450(400) 350(300)	µA µA
Self refresh current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{W}$=$\overline{OE}$=A0 ~ A11(A10) = V_{DD}-0.2V or 0.2V DQ1 ~ DQ8= V_{DD}-0.2V, 0.2V or open	KM48V20(1)04ALL	I_{CC8}		250	µA
INPUT LEAKAGE CURRENT (Any input 0≤V_{IN}≤V_{DD}+0.3V all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	µA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤V_{DD})		$I_{O(L)}$	-10	10	µA
OUTPUT HIGH VOLTAGE LEVEL(I_{OH}=-2mA)		V_{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL(I_{OL}=2mA)		V_{OL}	-	0.4	V

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE(T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11(A10)]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ1 - DQ8]	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{DD}=3.3V±0.3V, See notes 1,2)
Test condition : V_{IH}/V_{IL} = 2.0V/0.8V, V_{OH}/V_{OL} = 2.0V/0.8V, output loading C_L = 100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	45		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	11
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	45		55		60		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	6
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		15		15		ns	9
Write command hold time referenced to $\overline{RAS}$	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	6
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	10		15		20		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{DD}=3.3V \pm 0.3V$ See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		15		15		ns	10
data hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period [4K(2K)]	tREF		64(32)		64(32)		64(32)	ms	
Refresh period(Low power & self refresh)	tREF		128		128		128	ms	
Refresh period(Super low power)	tREF		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		100		110		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		65		70		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		70		75		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		30		30		ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Hyper Page cycle time	tHPC	24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	71		86		96		ns	17
$\overline{CAS}$ precharge time (Hyper Page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	60	200,000	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Out put buffer turn off delay from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7,14
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
Write command set-up time (test mode in)	tWTS	10		10		10		ns	12
Write command hold time (test mode in)	tWTH	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	7,15
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width(Hyper Page Cycle)	tWPE	5		5		5		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{DD}=3.3V \pm 0.3V$ See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay form $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	7,14,15
Output buffer turn off delay form $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7,14
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{RAS}$ pulse width (LL-Ver)	tRASS	100		100		100		μs	16
$\overline{RAS}$ precharge time (LL-Ver)	tRPS	110		130		150		ns	16
$\overline{CAS}$ hold time (LL-Ver)	tCHS	-50		-50		-50		ns	16

TEST MODE CYCLE

(Note. 12)

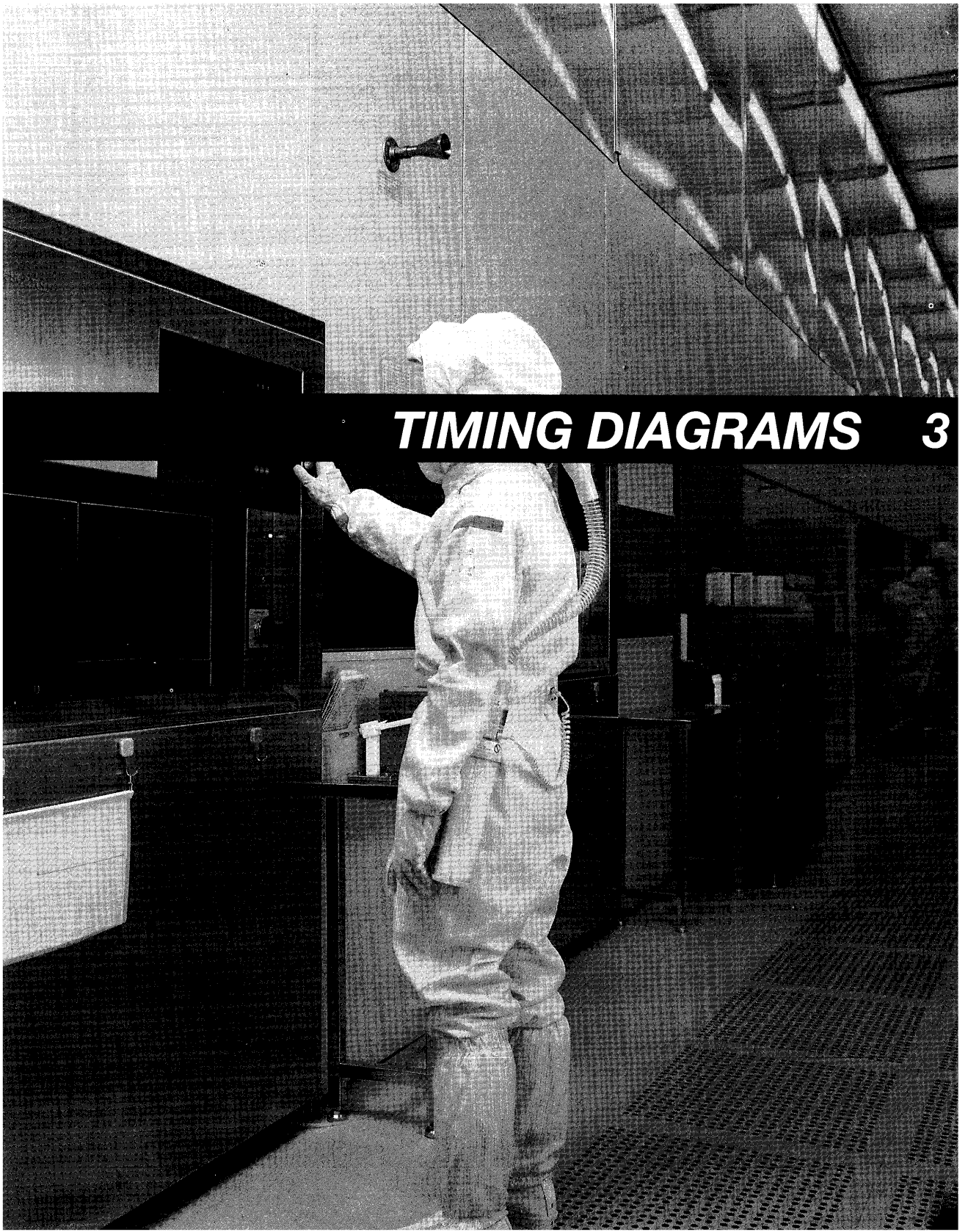
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	15	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	tRSH	20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	50		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	90		105		115		ns	8
Column address to $\overline{W}$ delay time	tAWD	60		70		75		ns	8
Hyper Page cycle time	tHPC	29		34		39		ns	
Hyper page read-modify-write cycle time	tHPRWC	76		91		101		ns	
$\overline{RAS}$ pulse width (EDO Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time form $\overline{CAS}$ precharge	tCPA		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	20		25		25		ns	

TEST MODE DESCRIPTI ON

The KM48V20(1)04A/AL/ALL/ASL is the CMOS DRAM organized 2,097,152 words by 8 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4Mx4 DRAM can be tested as if it were a 1Mx8 DRAM. **$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$** Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", . And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" peforms the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time(1/2 in cases of N test pattern).

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except tHPC and tHPRWC.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min) the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
16. 4096(2048) cycle of burst refresh must be executed within 64(32) ms before and after self refresh, in order to meet refresh specification.
17. tASC ≧ tCPmin , Assume tT = 2.0 ns



TIMING DIAGRAMS 3

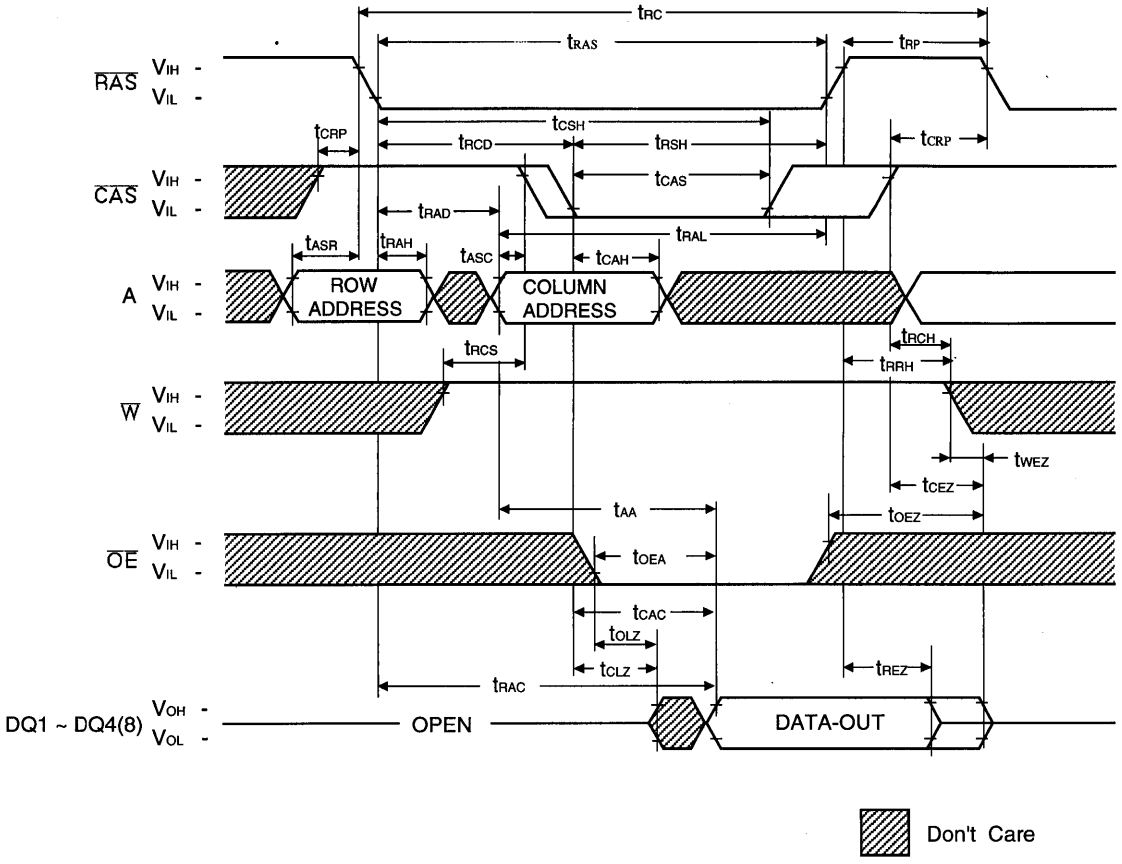
x4 & x8 Timing Diagram

Attached timing Diagram sets are adopted to x4 & x8 EDO DRAMs.

- KM44C1004C/CL/CSL
- KM44V1004C/CL/CSL
- KM48C514B/BL/BLL
- KM48V514B/BL/BLL
- KM44C4004A/AL/ALL/ASL
- KM44C4104A/AL/ALL/ASL
- KM44V4004A/AL/ALL/ASL
- KM44V4104A/AL/ALL/ASL
- KM48C2004A/AL/ALL/ASL
- KM48C2104A/AL/ALL/ASL
- KM48V2004A/AL/ALL/ASL
- KM48V2104A/AL/ALL/ASL

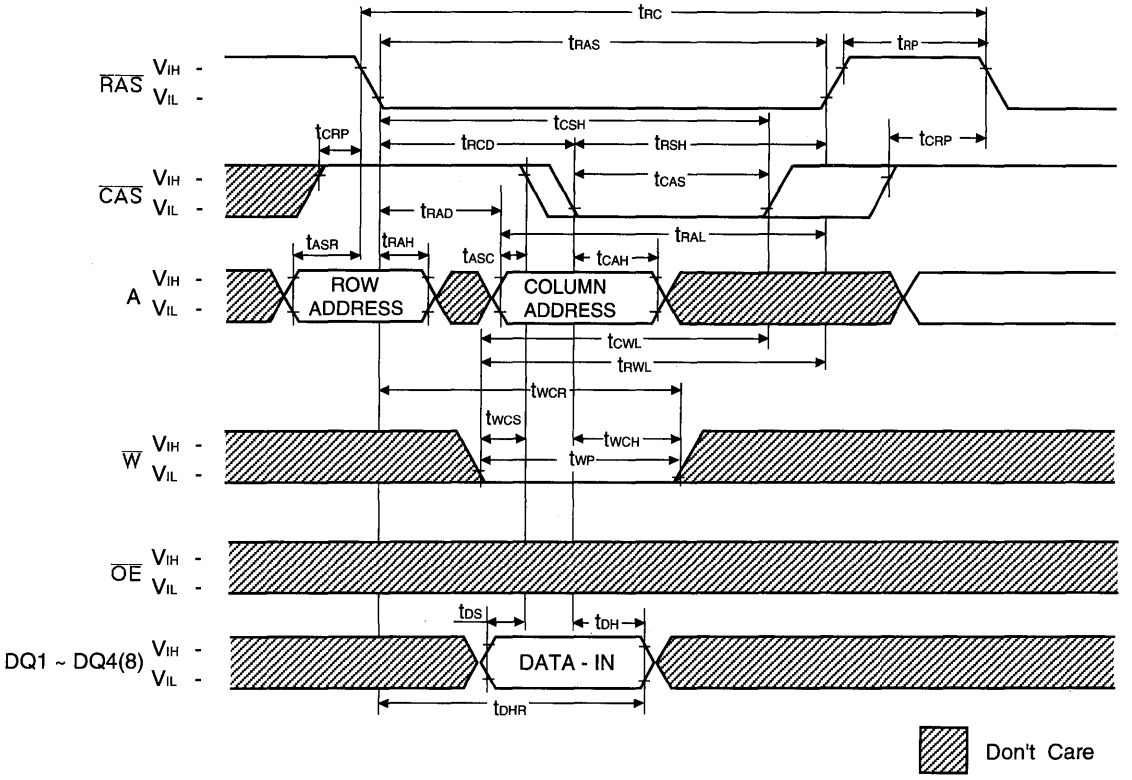
TIMING DIAGRAM

READ CYCLE



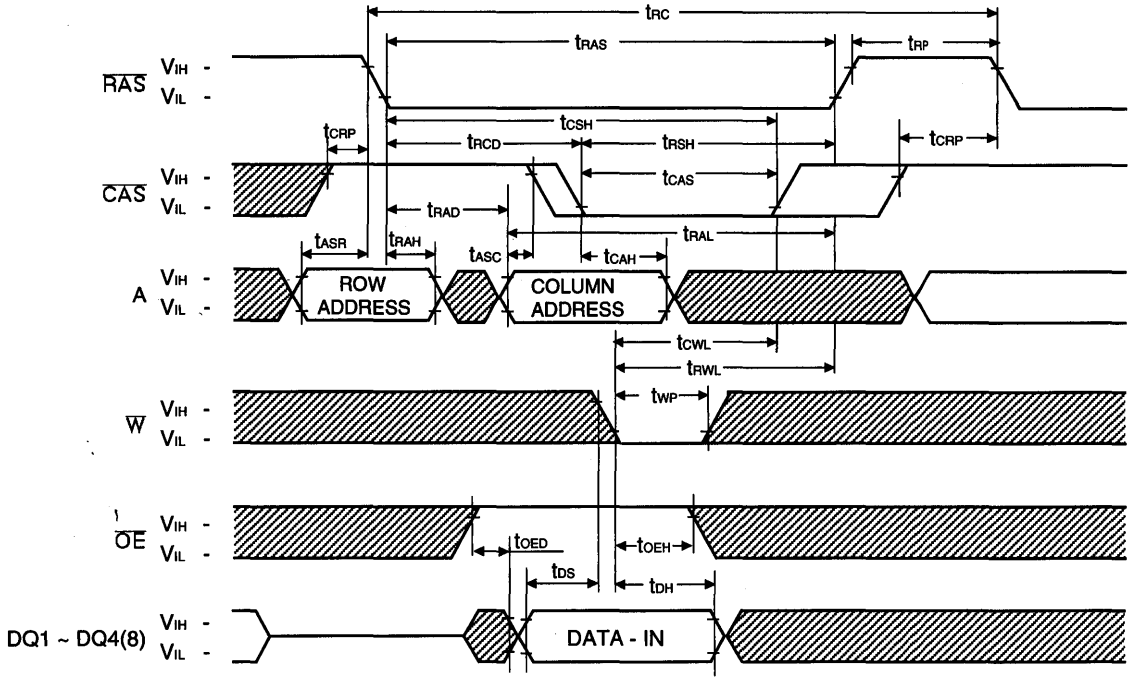
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



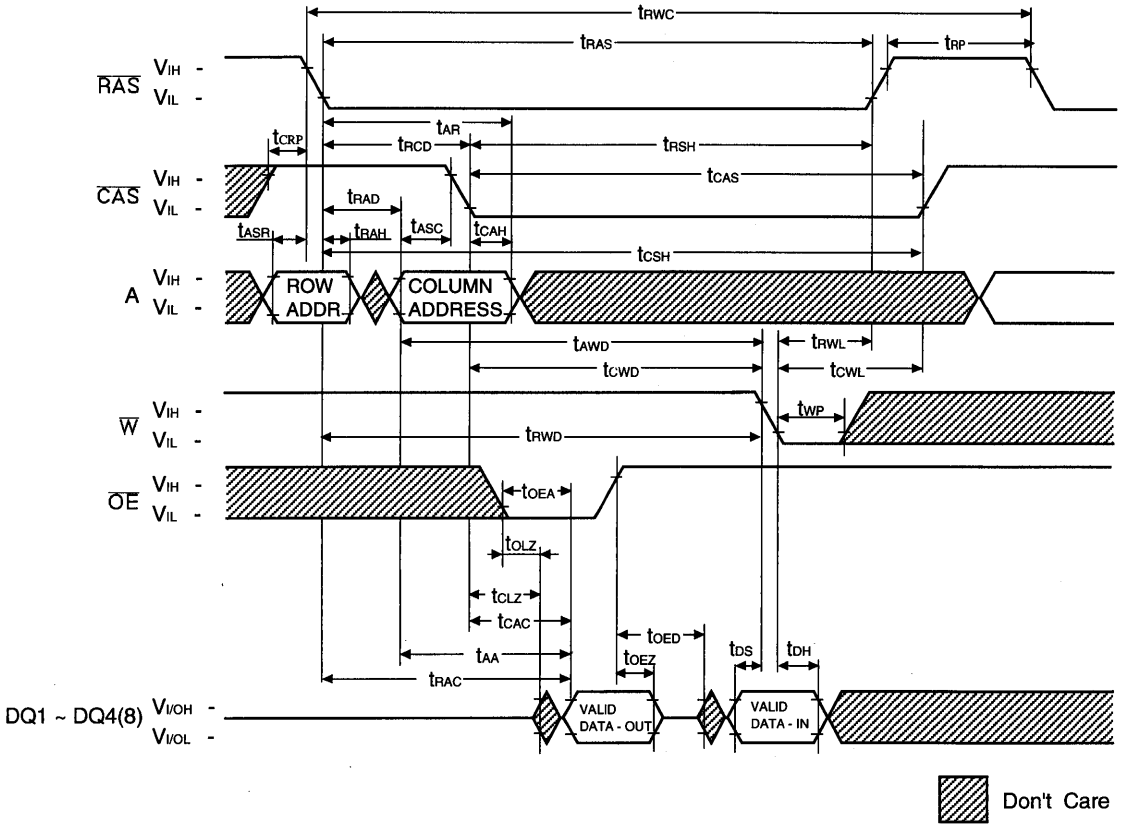
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



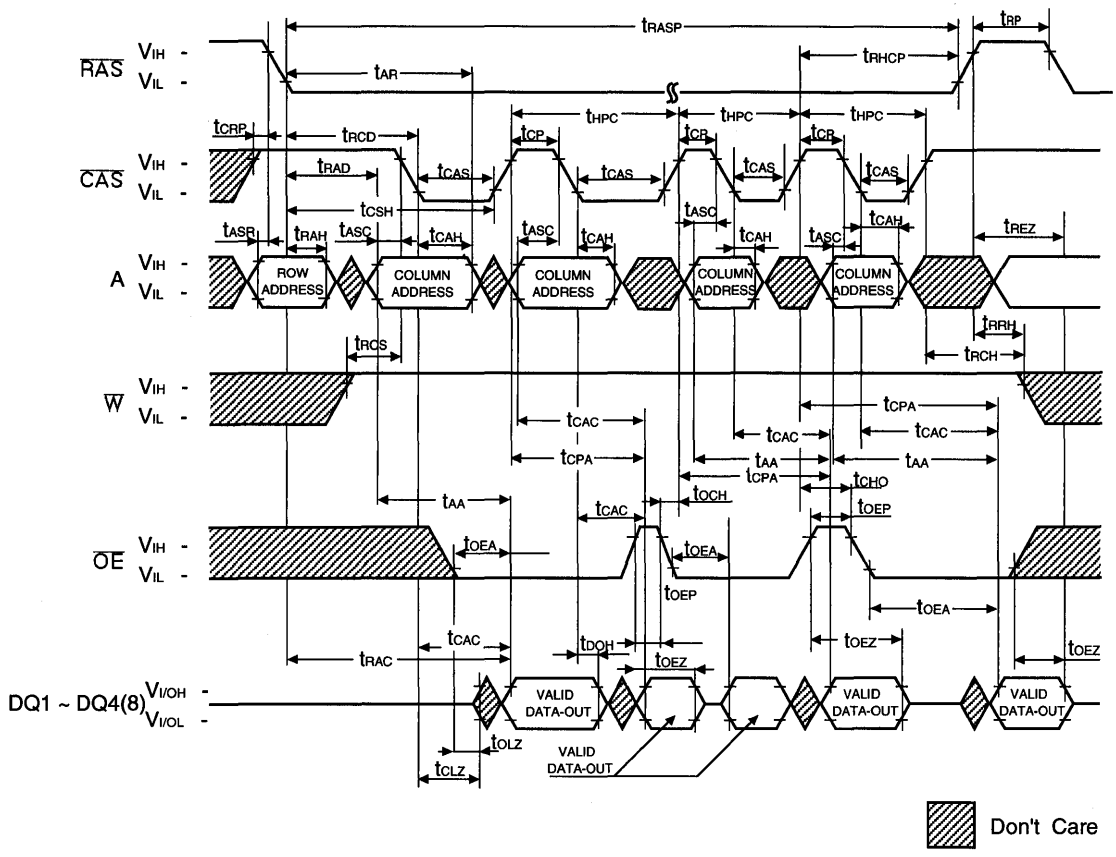
Don't Care

READ - MODIFY - WRITE CYCLE



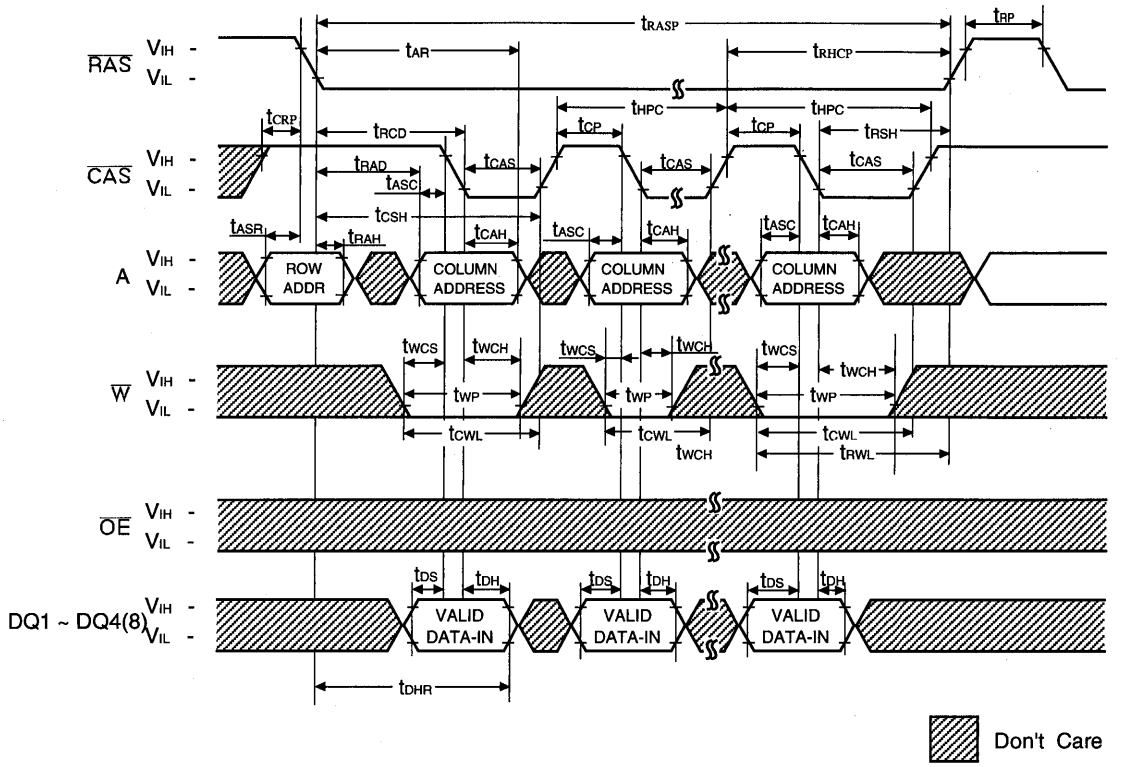
3

HYPER PAGE READ CYCLE

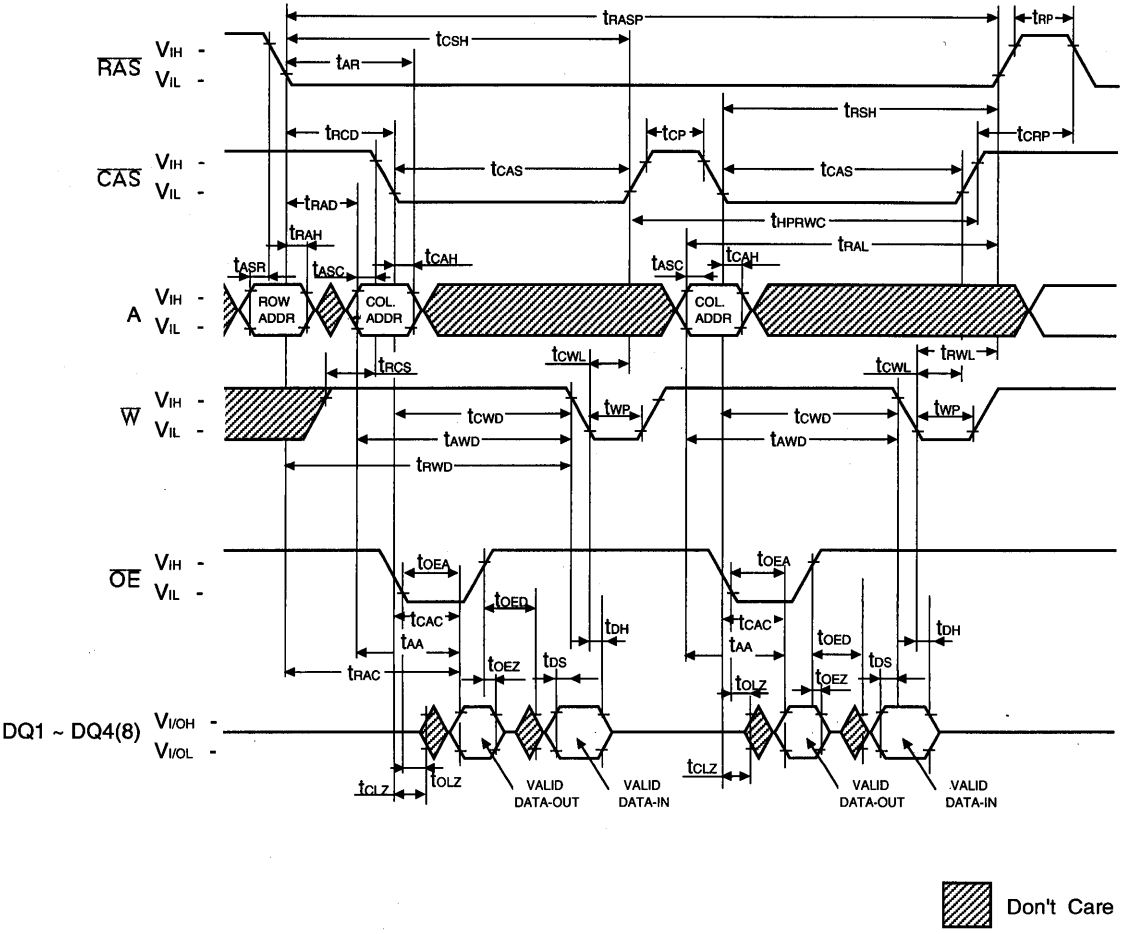


HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

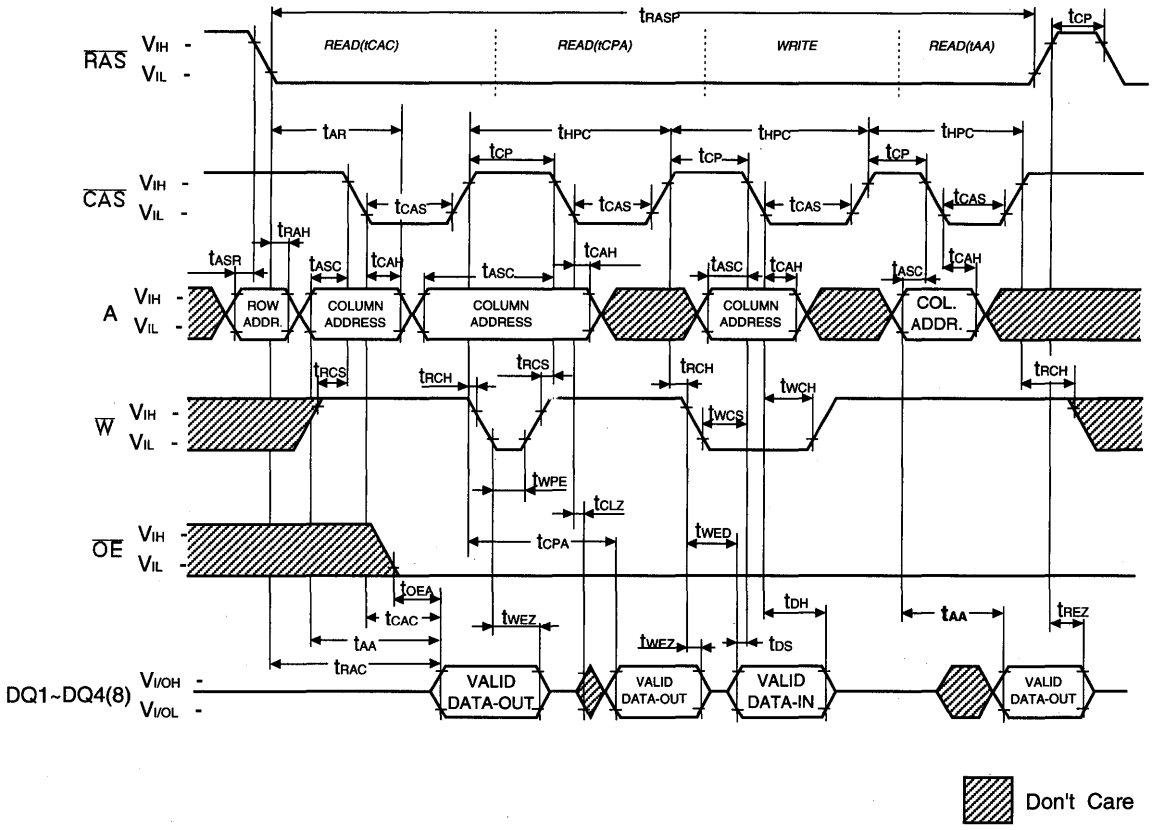


HYPER PAGE READ-MODIFY-WRITE CYCLE



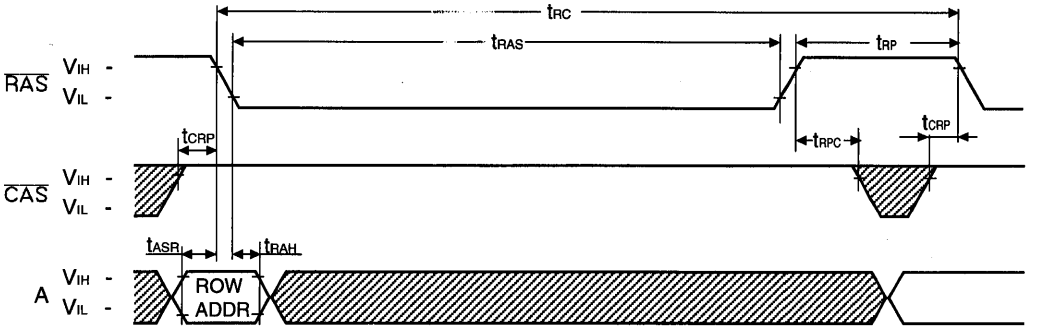
SAMSUNG ELECTRONICS

HYPER PAGE READ AND WRITE MIXED CYCLE



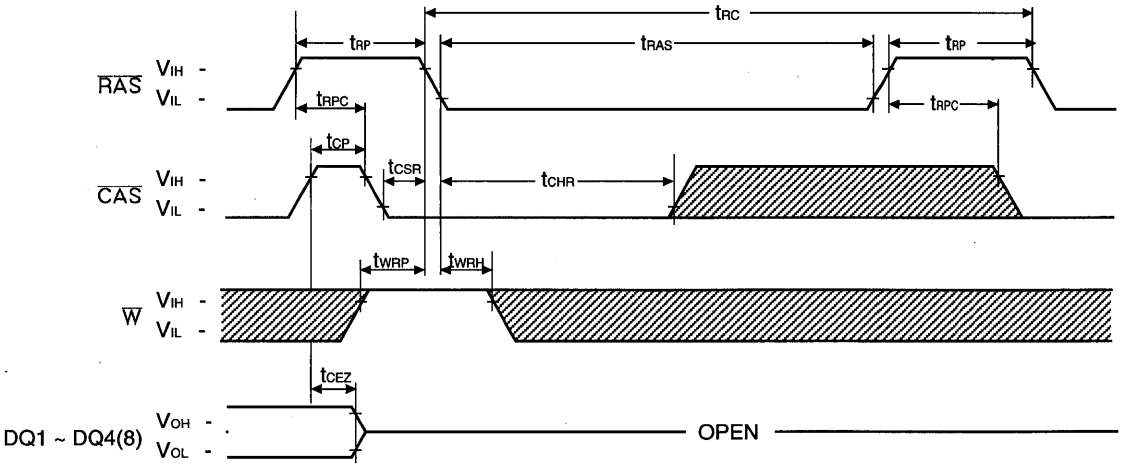
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

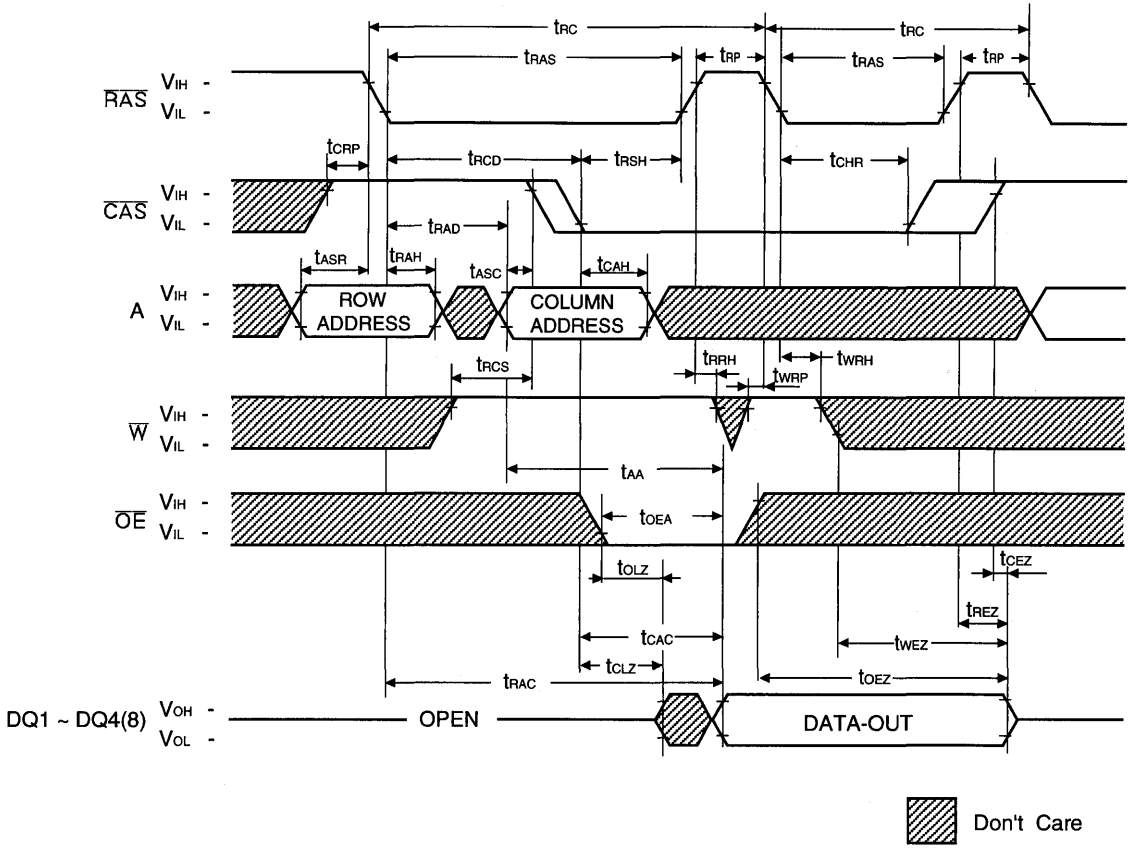
NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



Don't Care

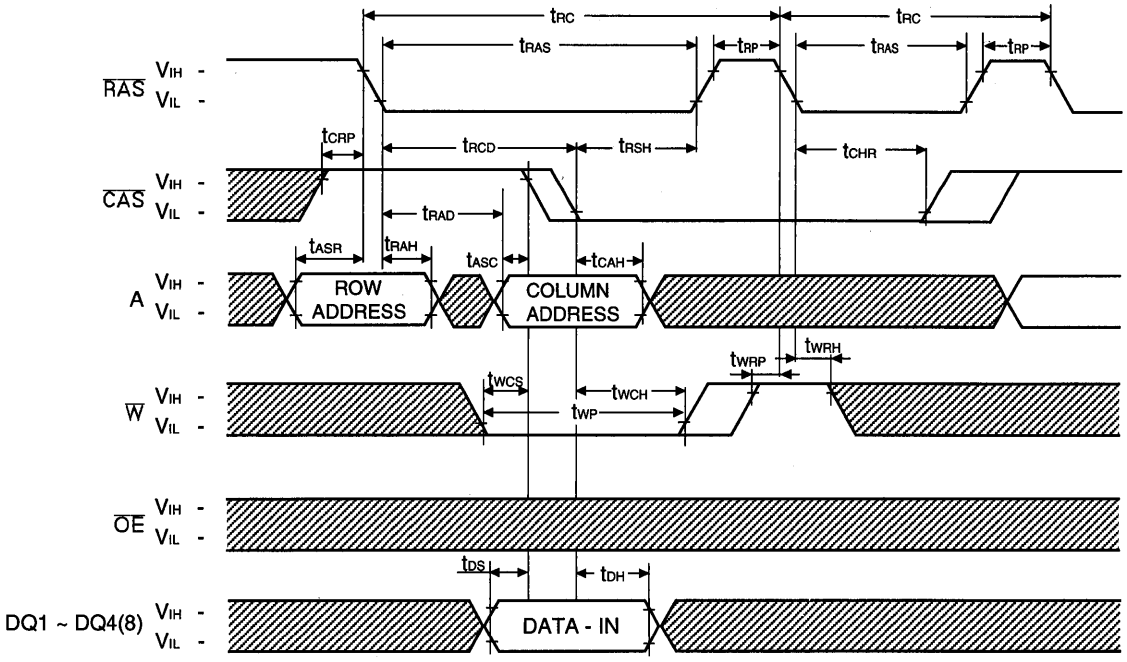
SAMSUNG ELECTRONICS

HIDDEN REFRESH CYCLE (READ)



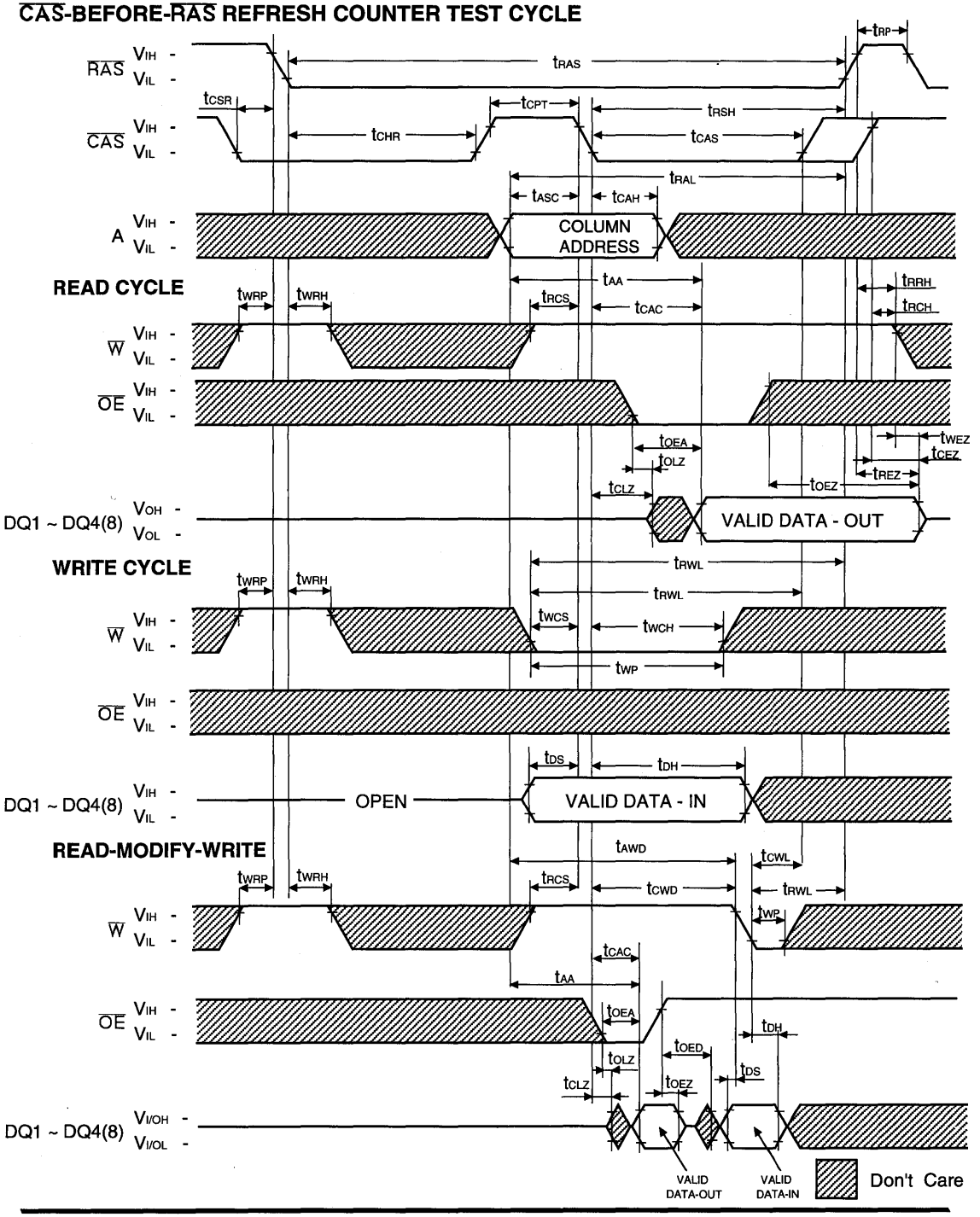
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



Don't Care

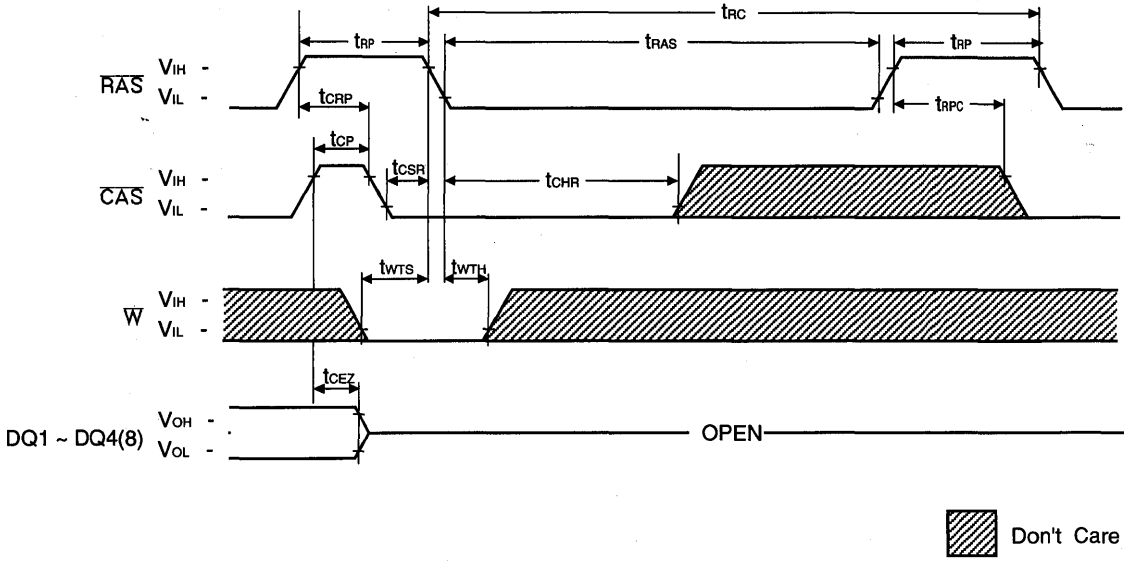
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



SAMSUNG ELECTRONICS

TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't Care



x16 Timing Diagram

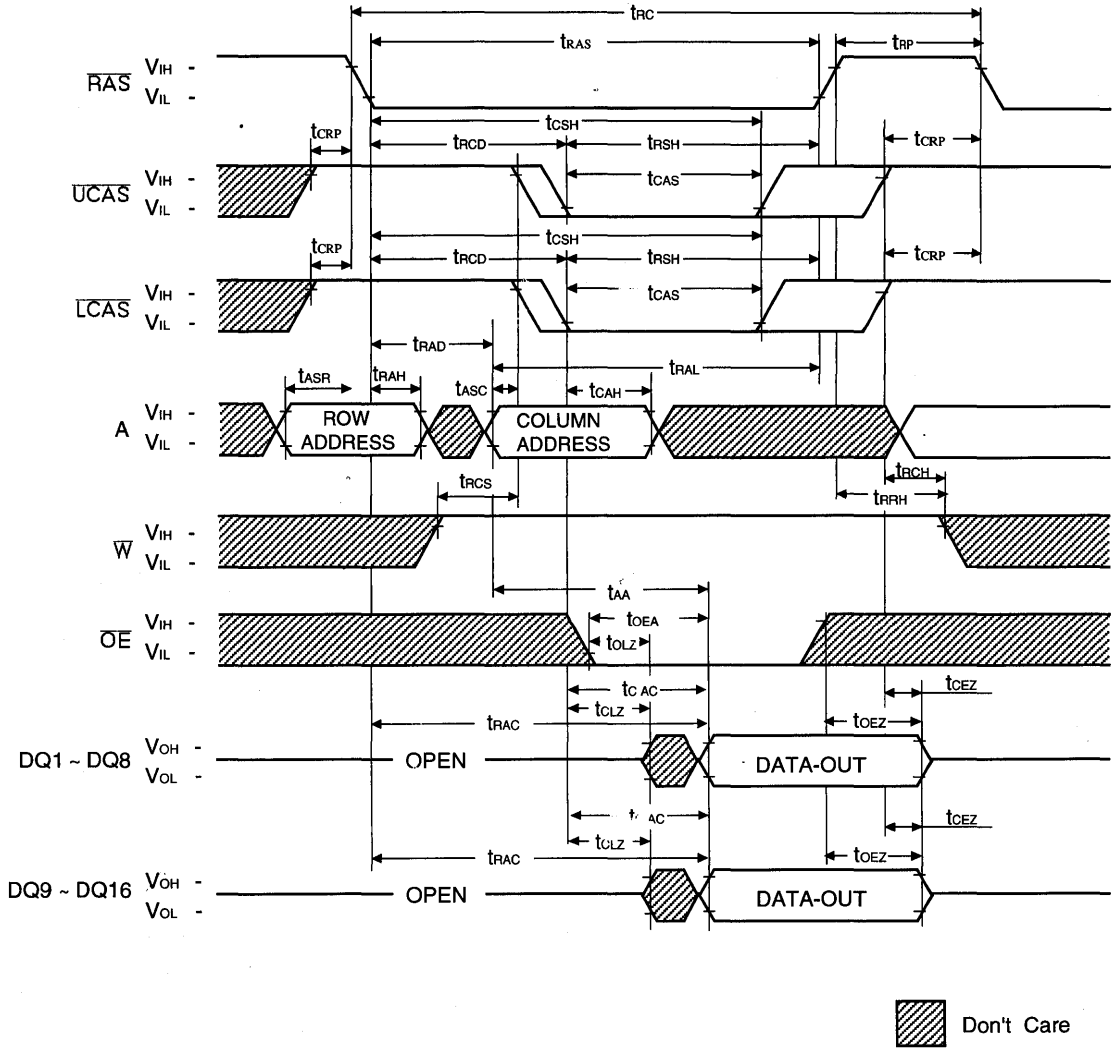
Attached timing Diagram set is adopted to x16 EDO DRAMs.

- KM416C254B/BL/BLL
- KM416V254B/BL/BLL

TIMING DIAGRAM

WORD READ CYCLE

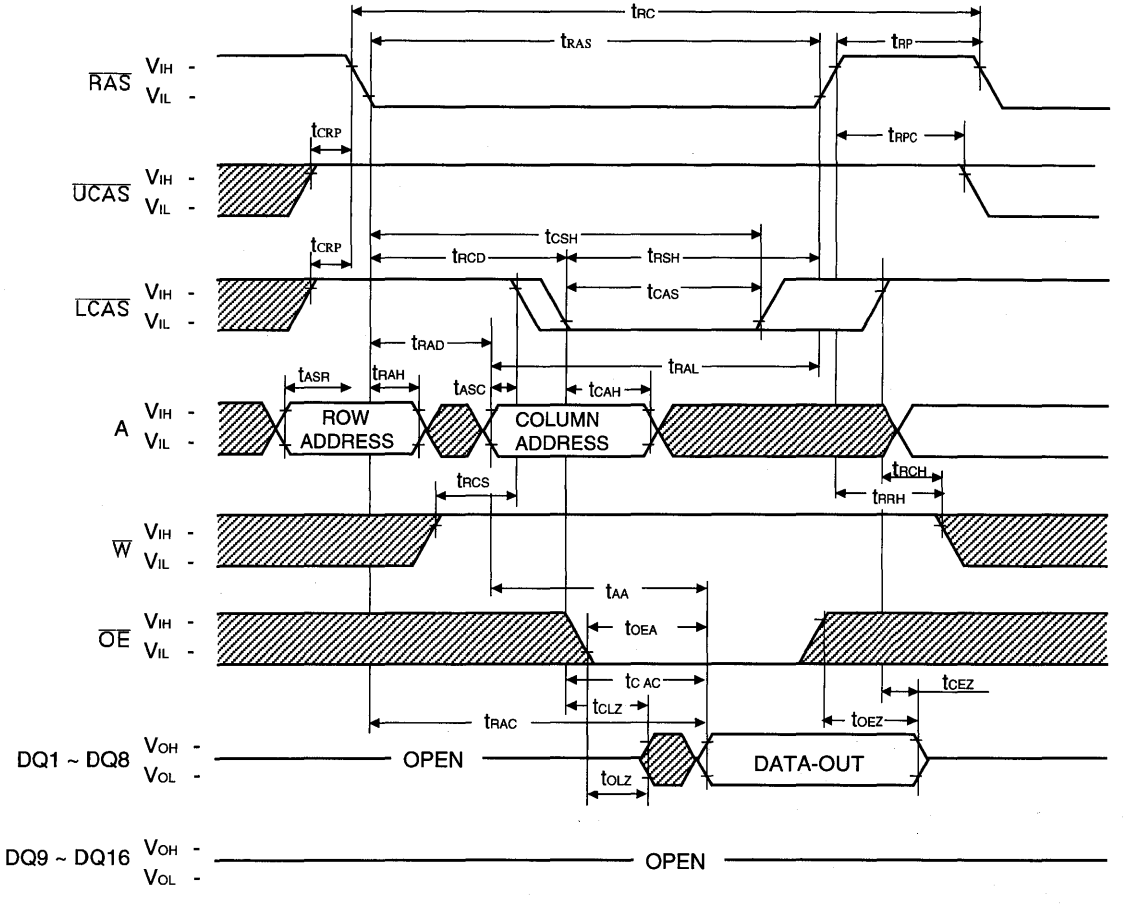
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

LOWER BYTE READ CYCLE

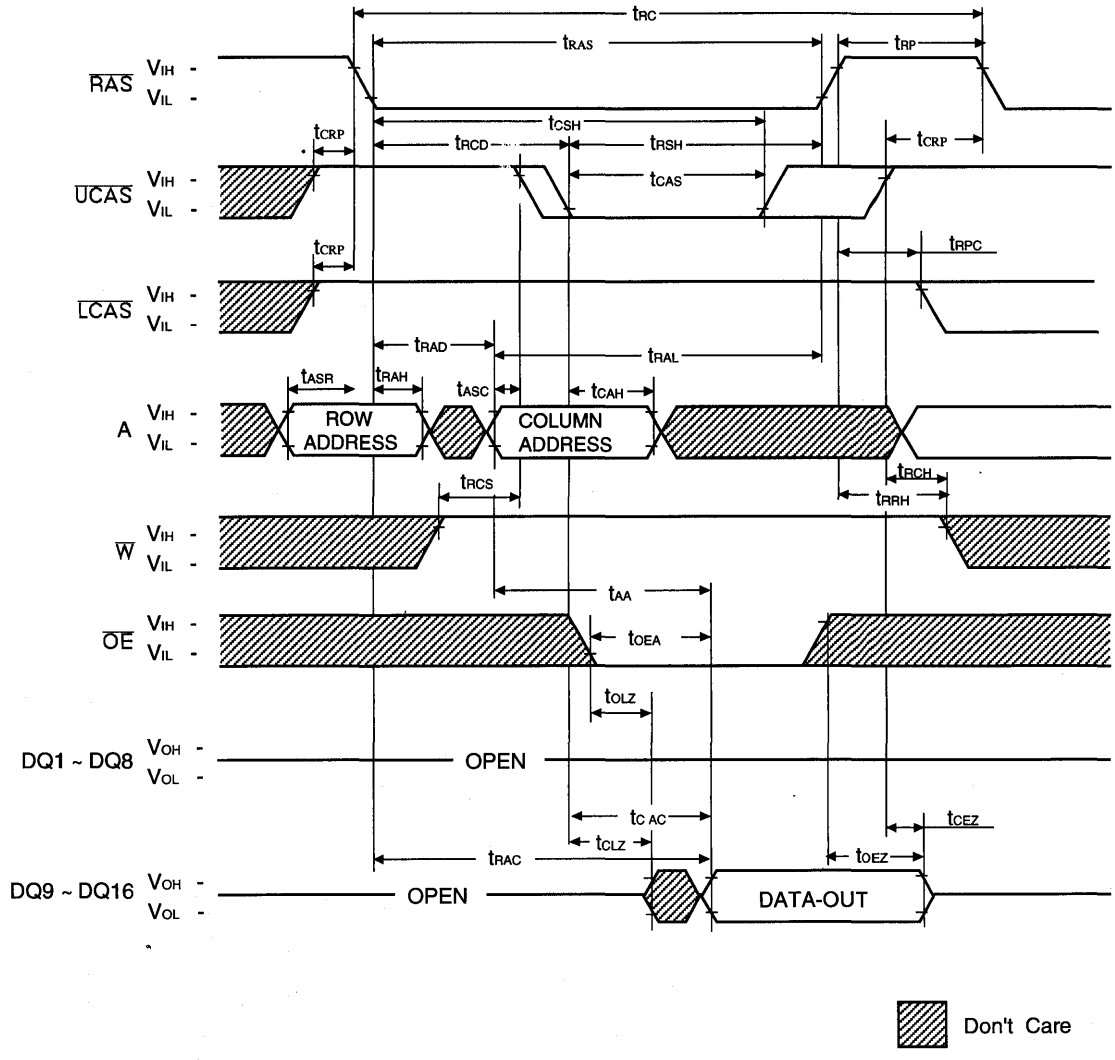
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

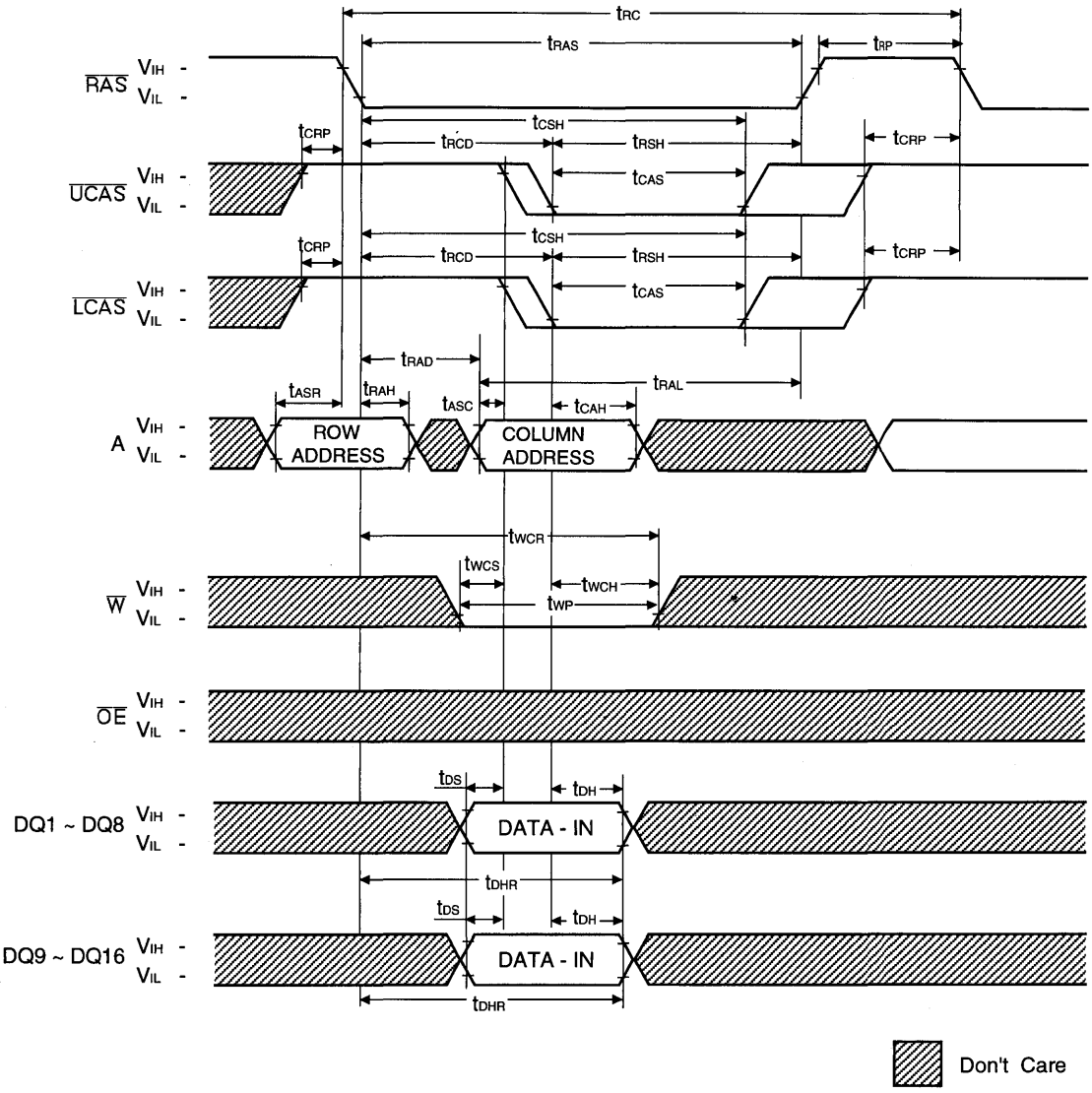
UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



WORD WRITE CYCLE (EARLY WRITE)

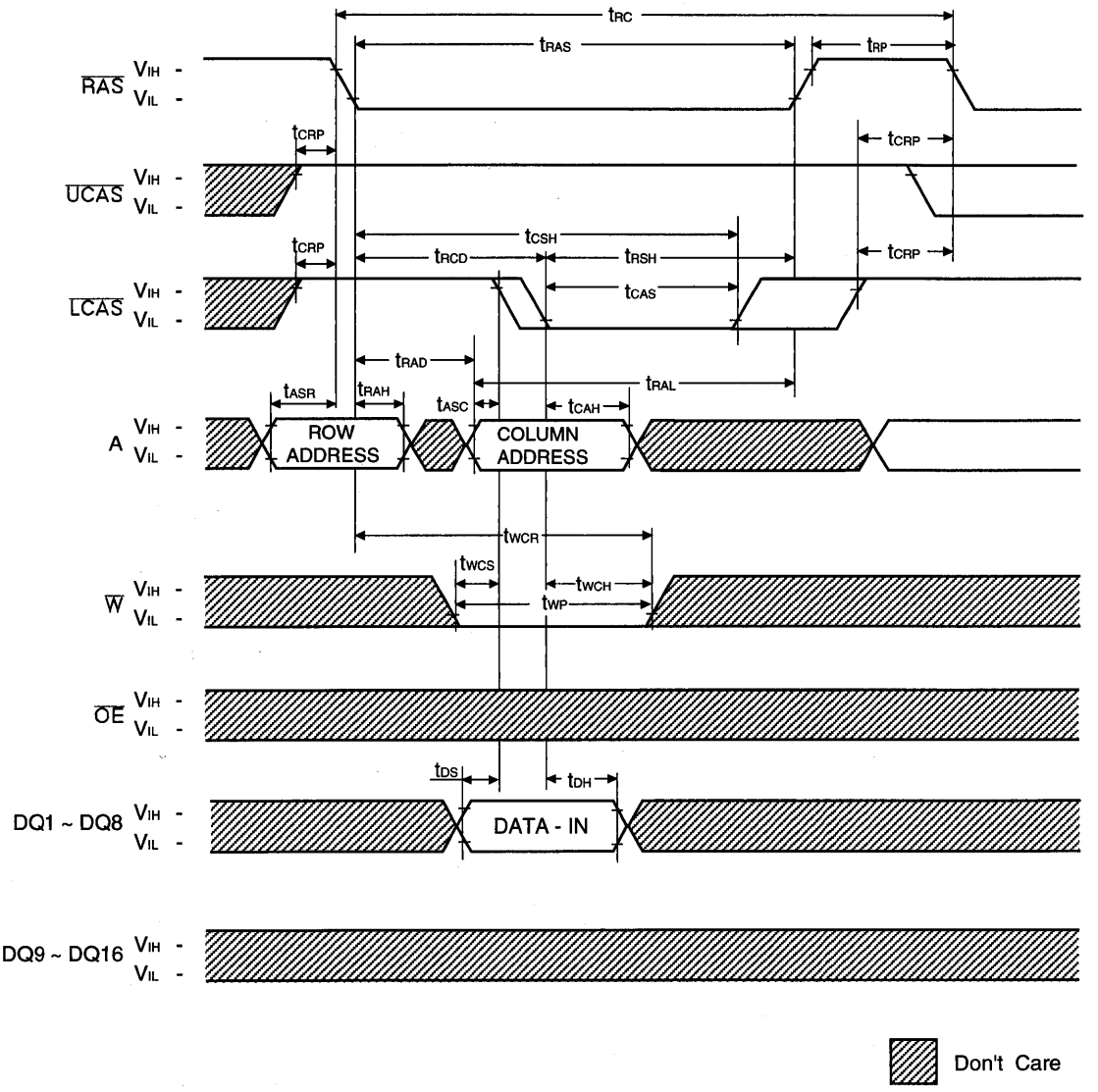
NOTE : D_{OUT} = OPEN



SAMSUNG ELECTRONICS

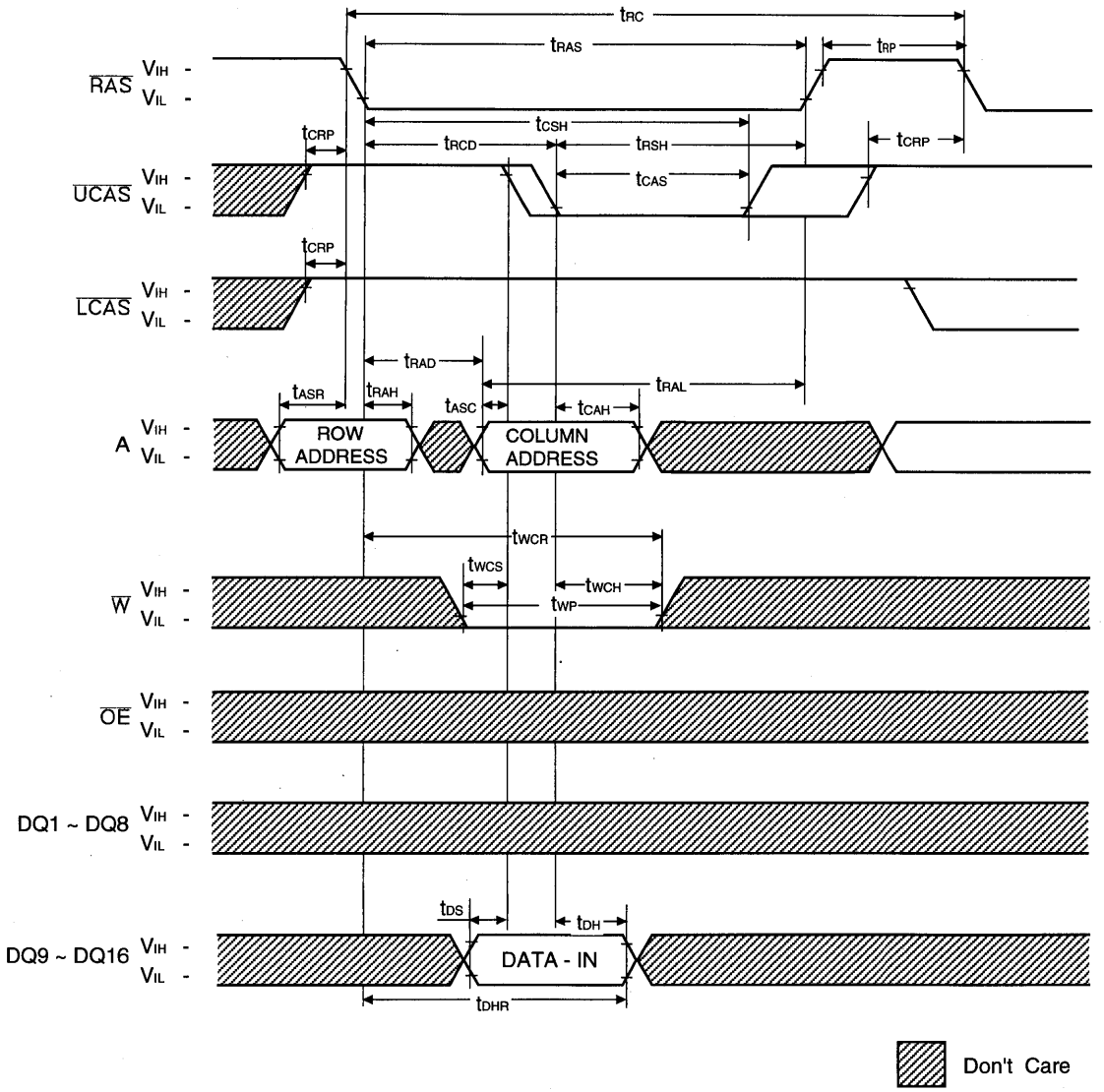
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



UPPER BYTE WRITE CYCLE (EARLY WRITE)

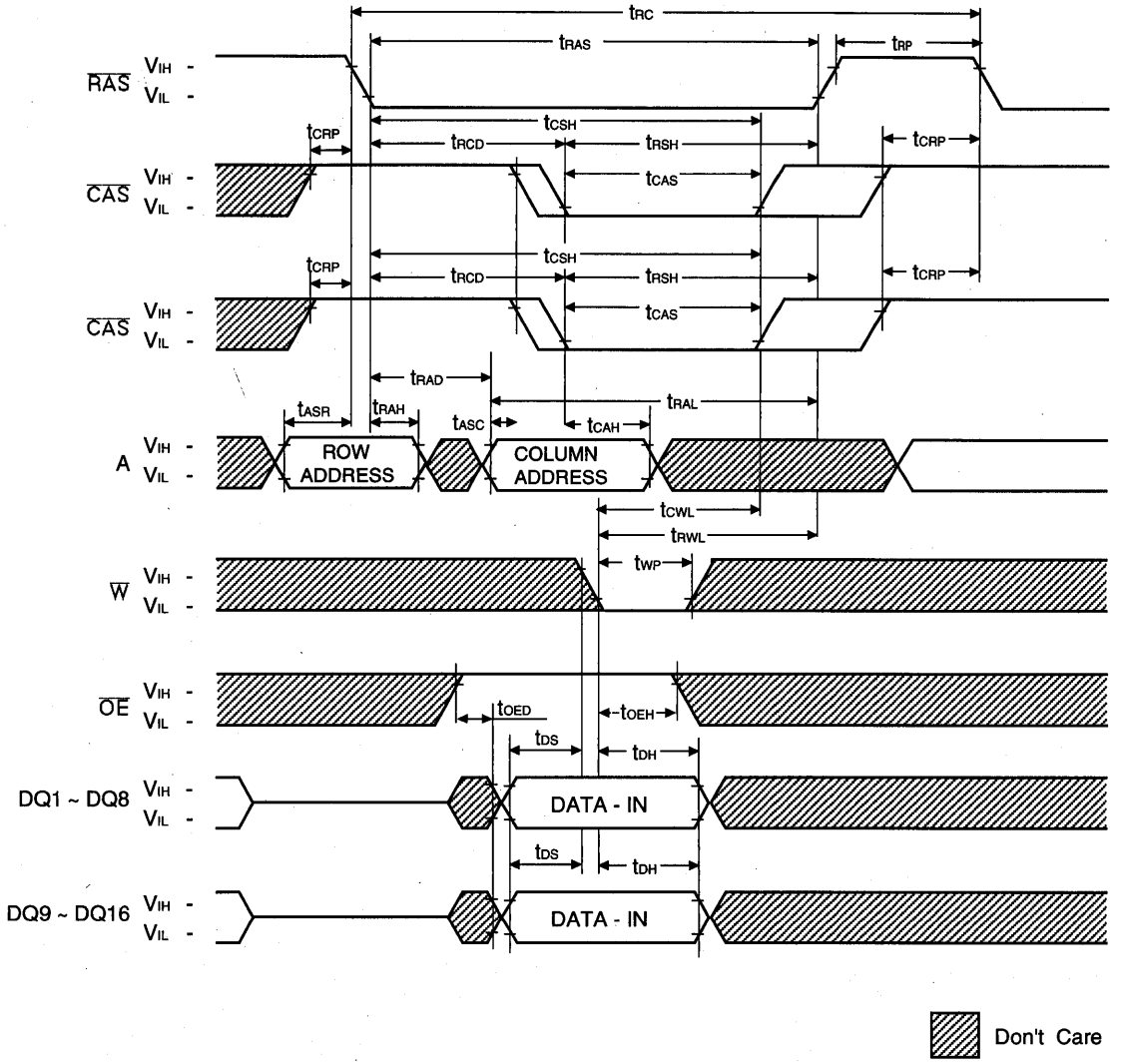
NOTE : D_{OUT} = OPEN



SAMSUNG ELECTRONICS

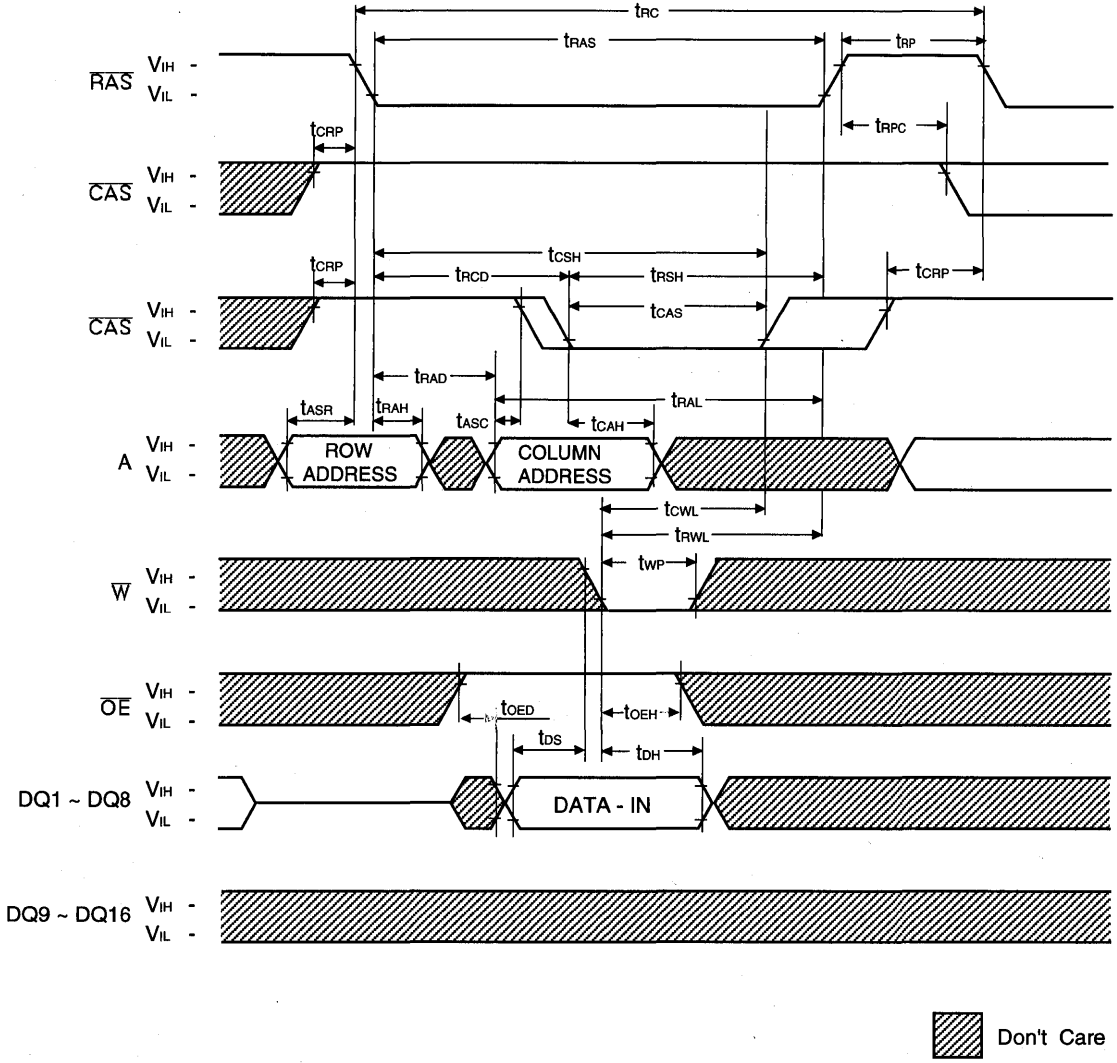
WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

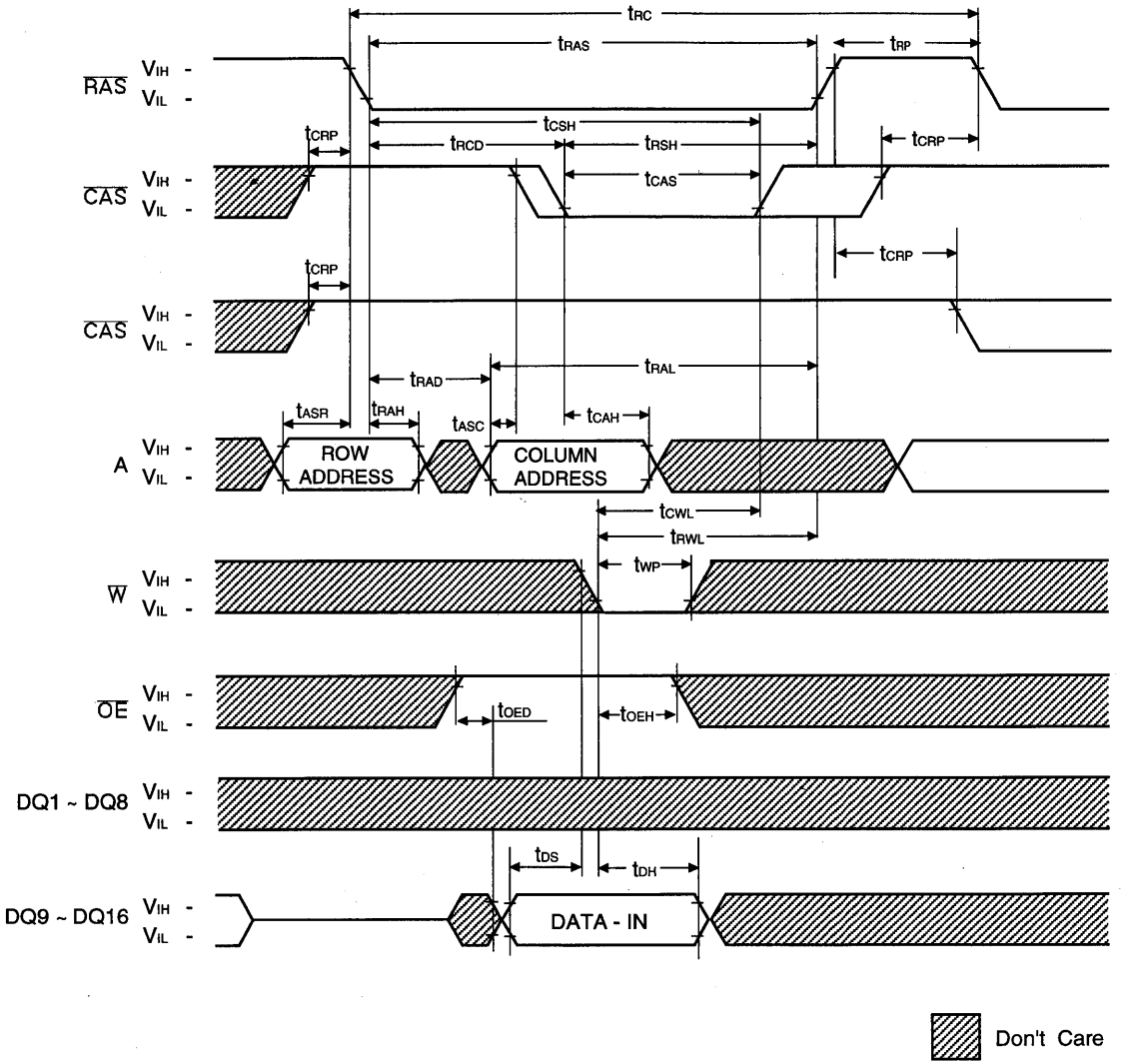


Don't Care

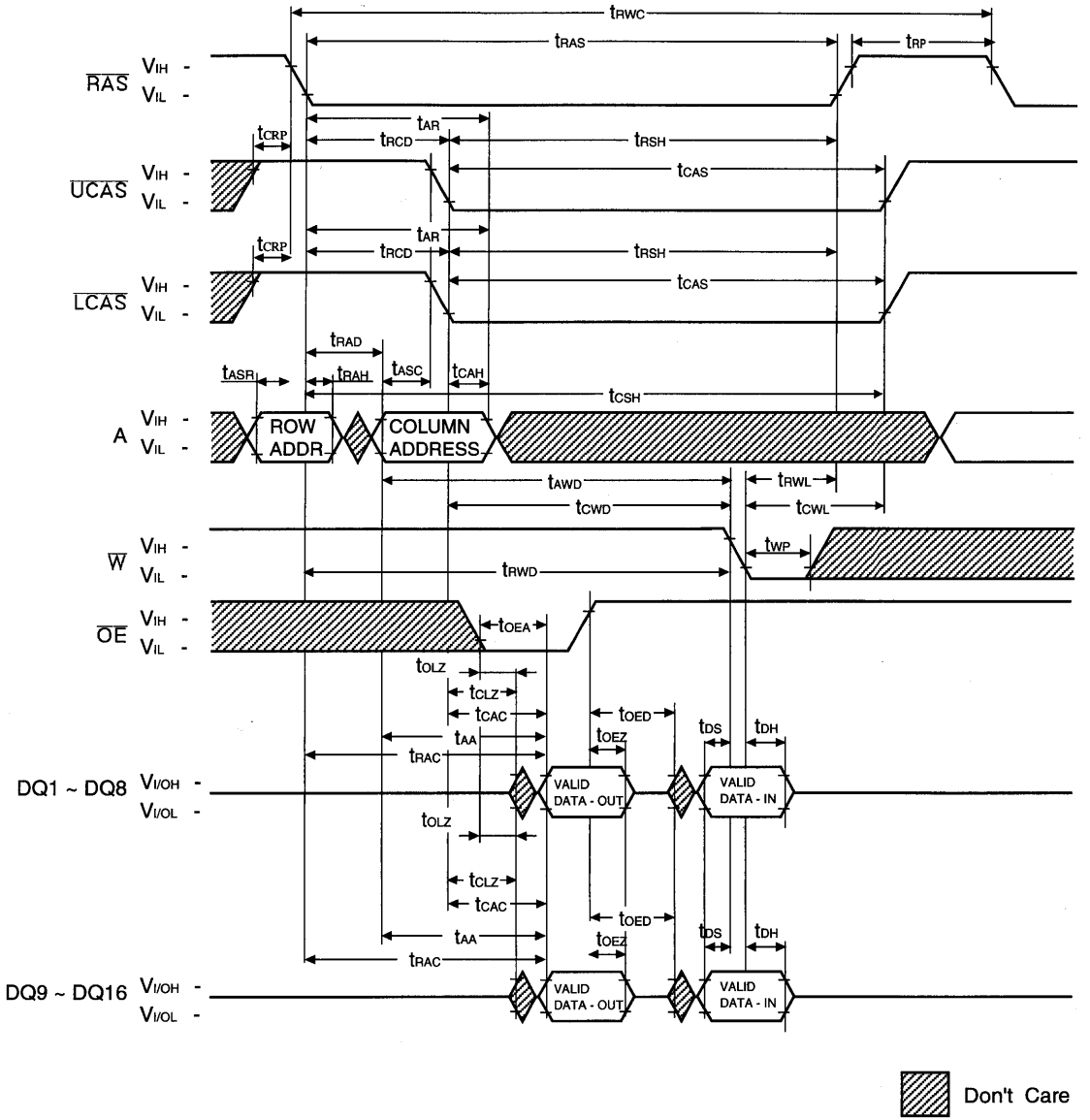
SAMSUNG ELECTRONICS

UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

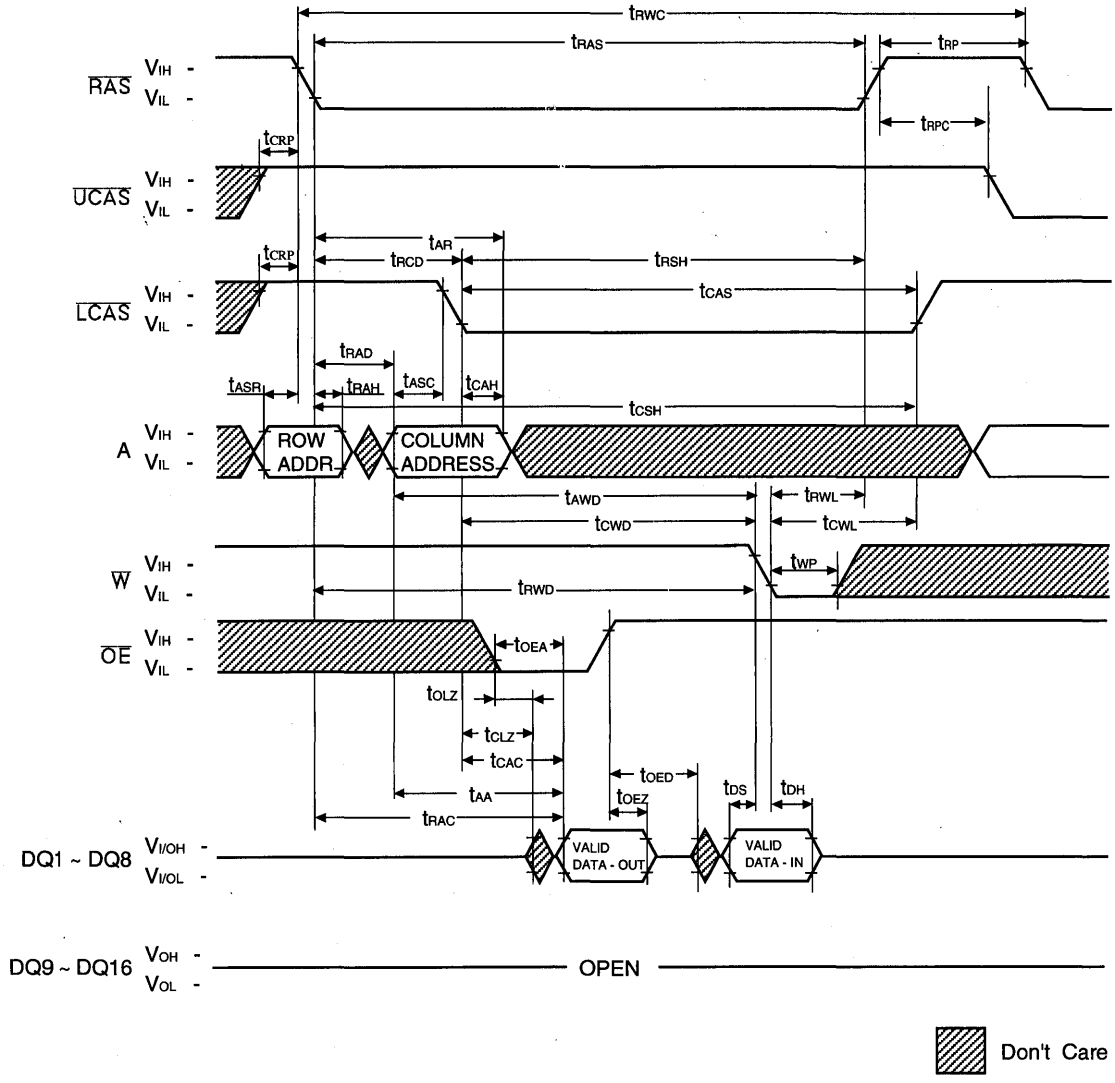


WORD READ - MODIFY - WRITE CYCLE

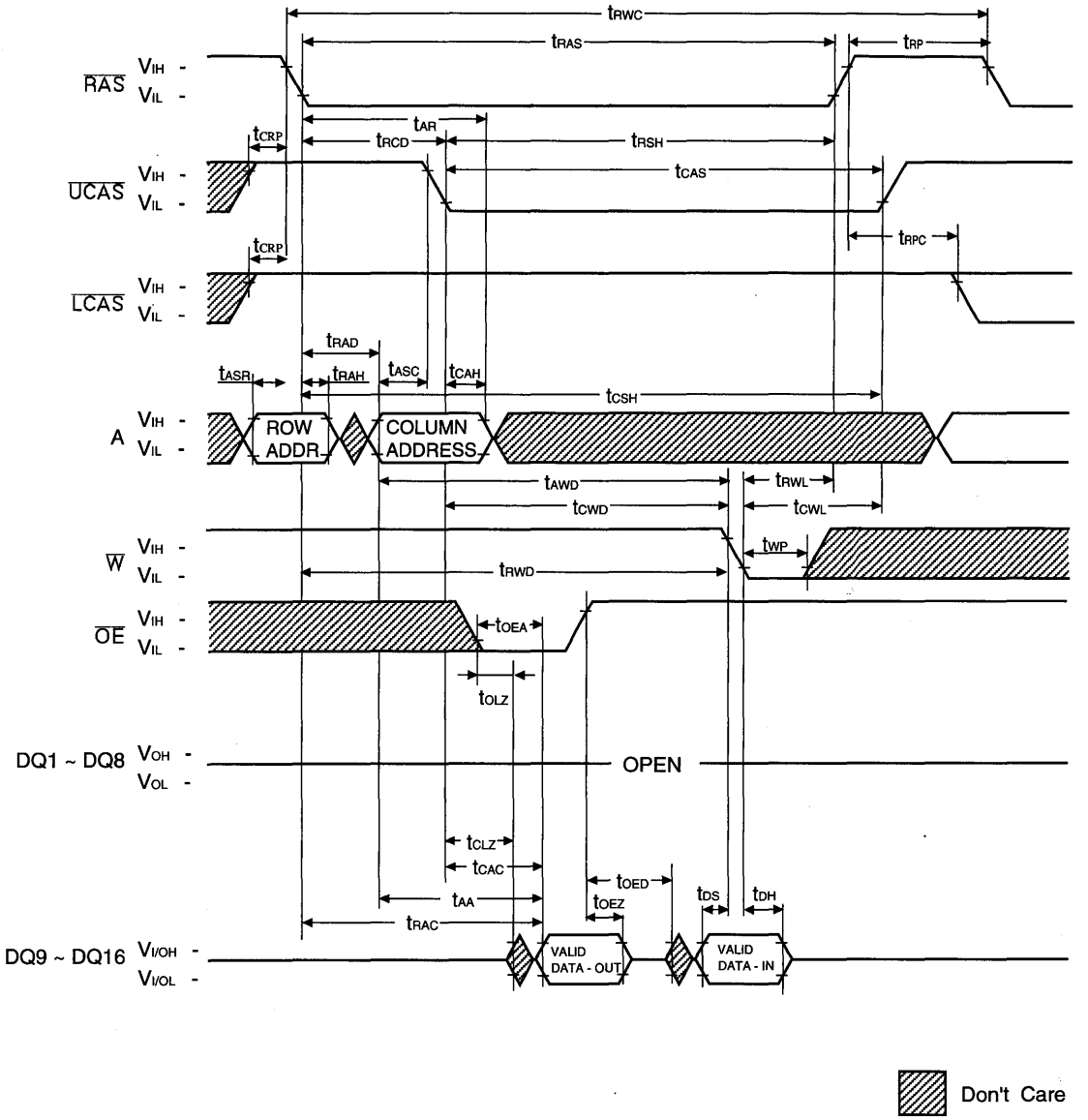


SAMSUNG ELECTRONICS

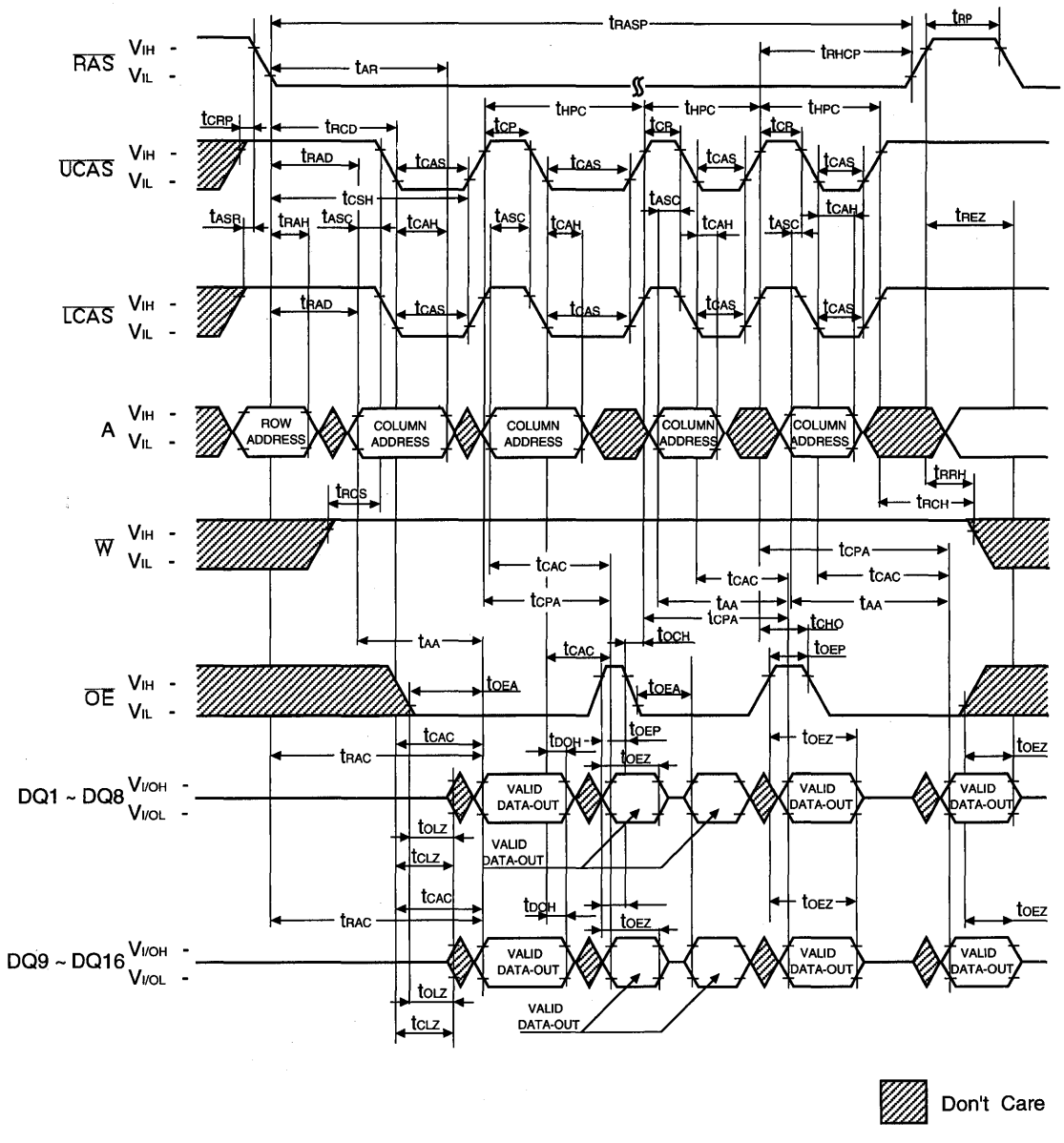
LOWER-BYTE READ - MODIFY - WRITE CYCLE



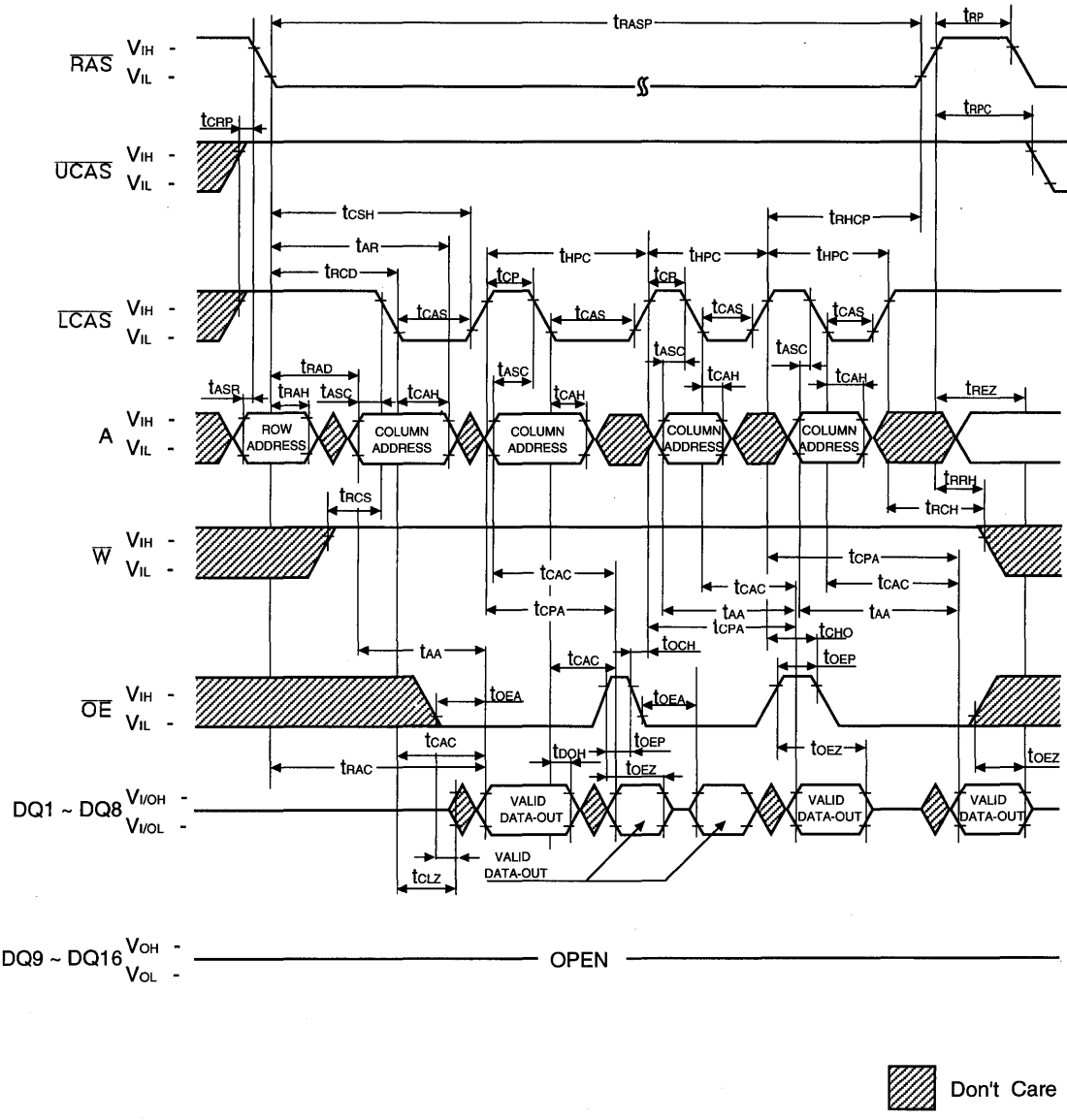
UPPER-BYTE READ - MODIFY - WRITE CYCLE



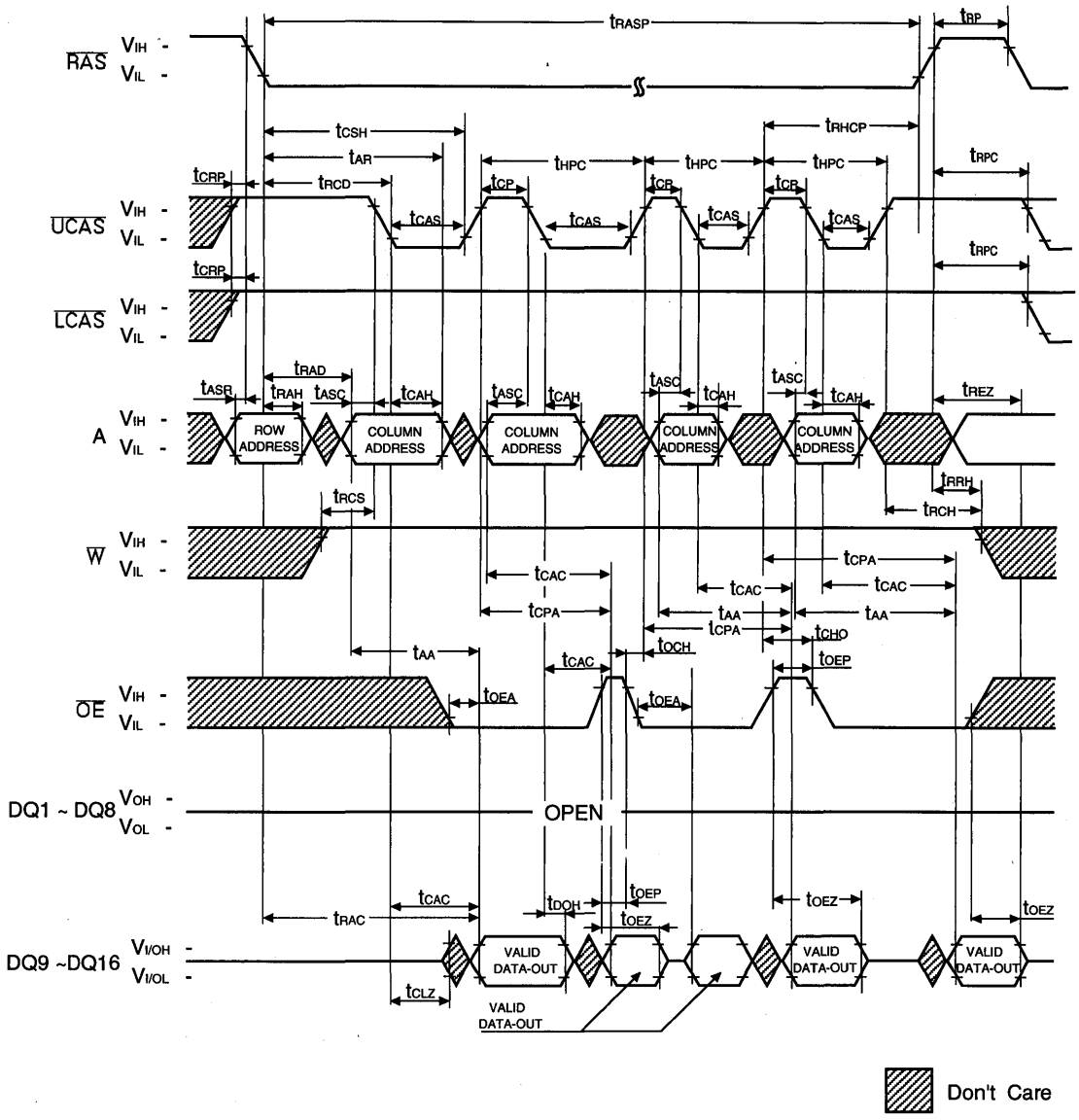
HYPER PAGE MODE WORD READ CYCLE



HYPER PAGE MODE LOWER BYTE READ CYCLE

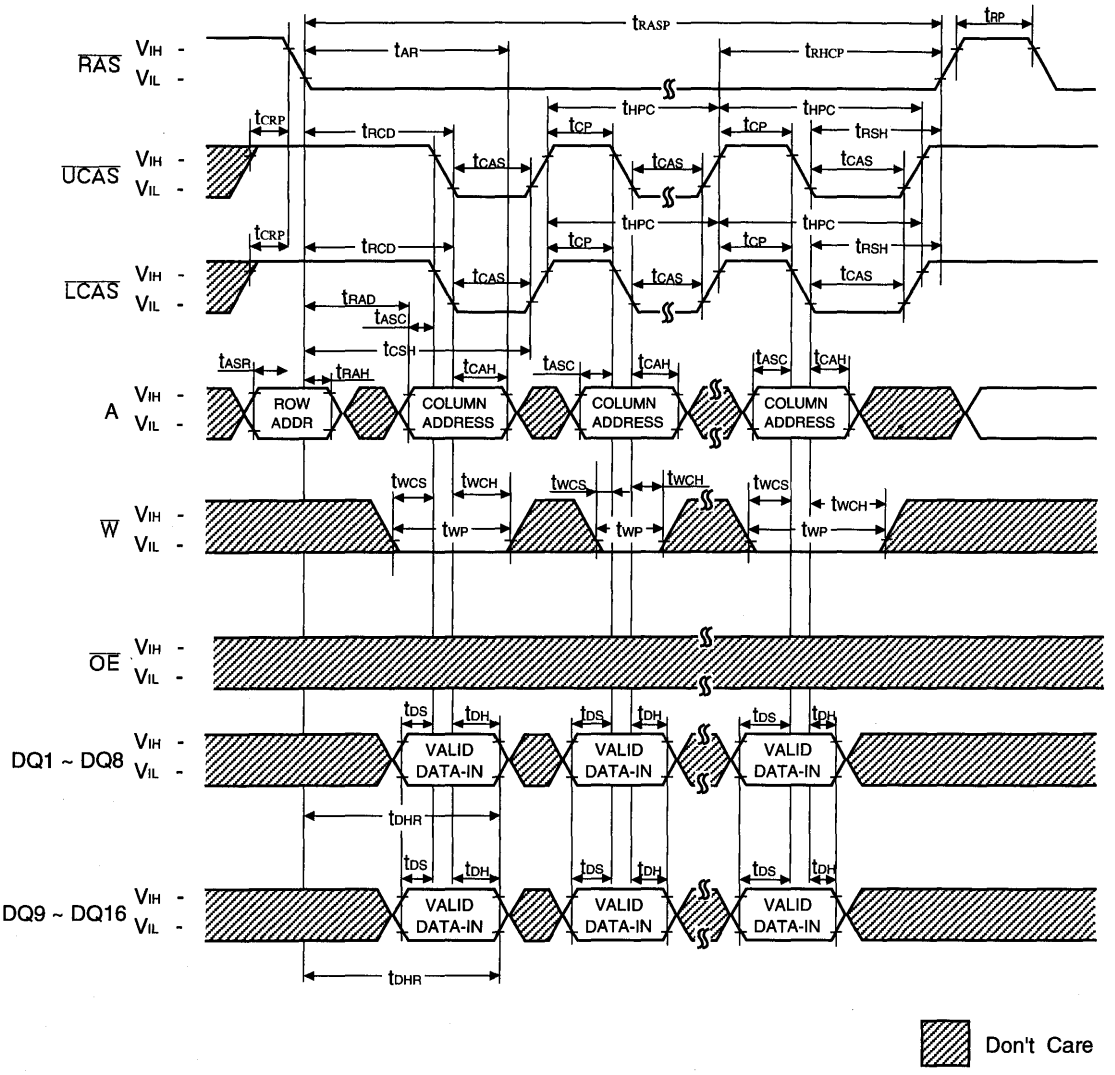


HYPER PAGE MODE UPPER BYTE READ CYCLE



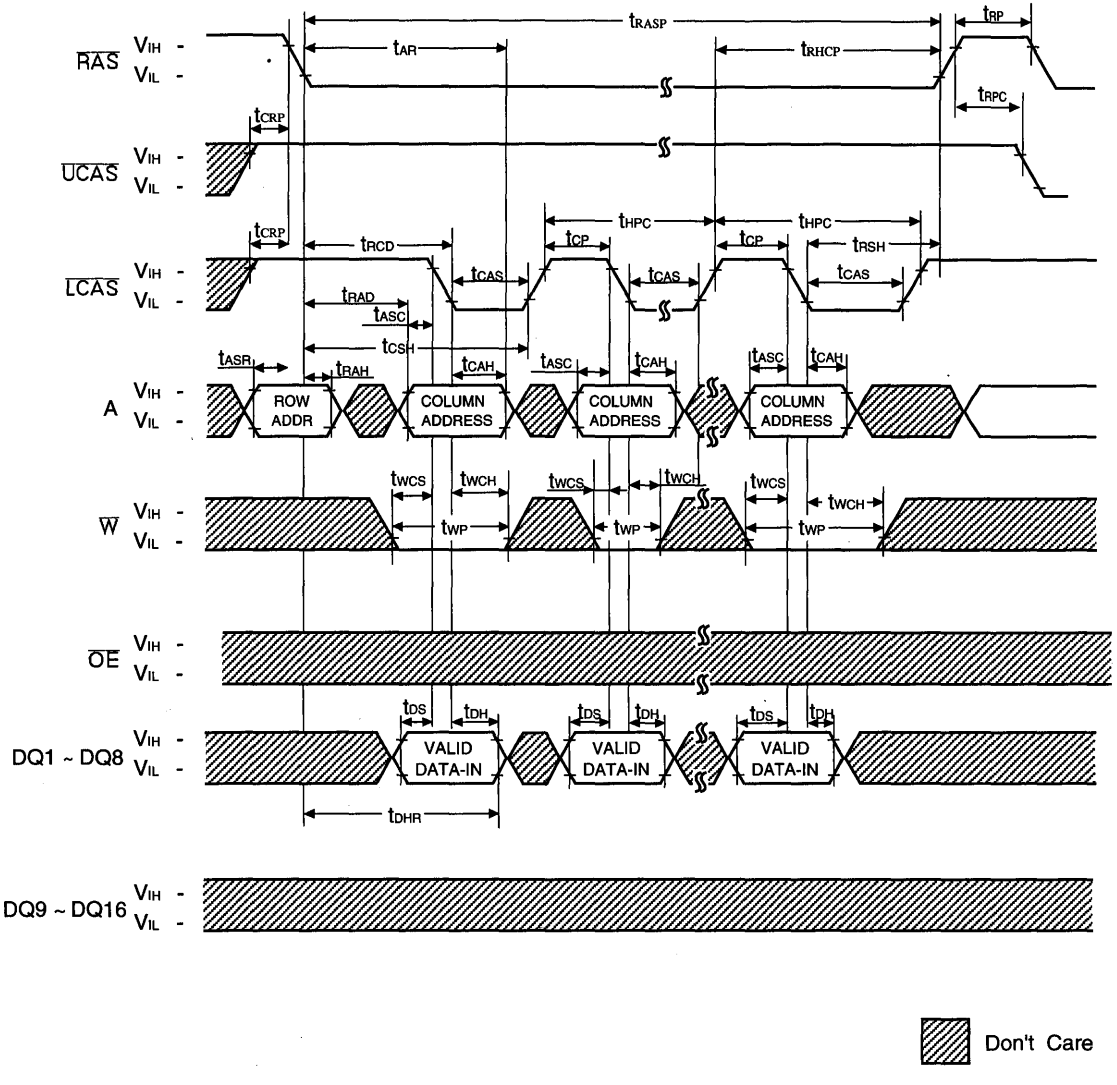
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

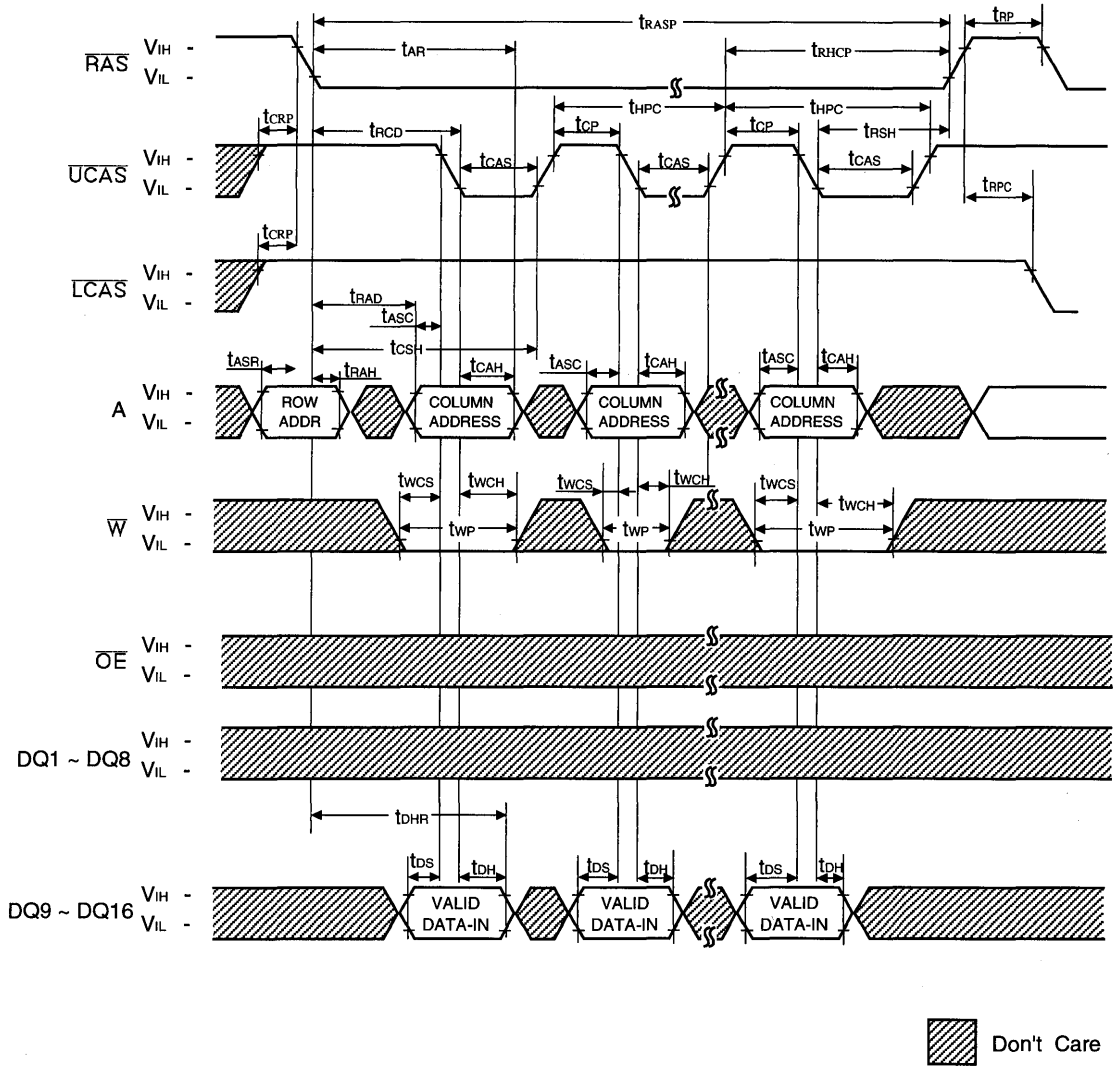
NOTE : D_{OUT} = Open



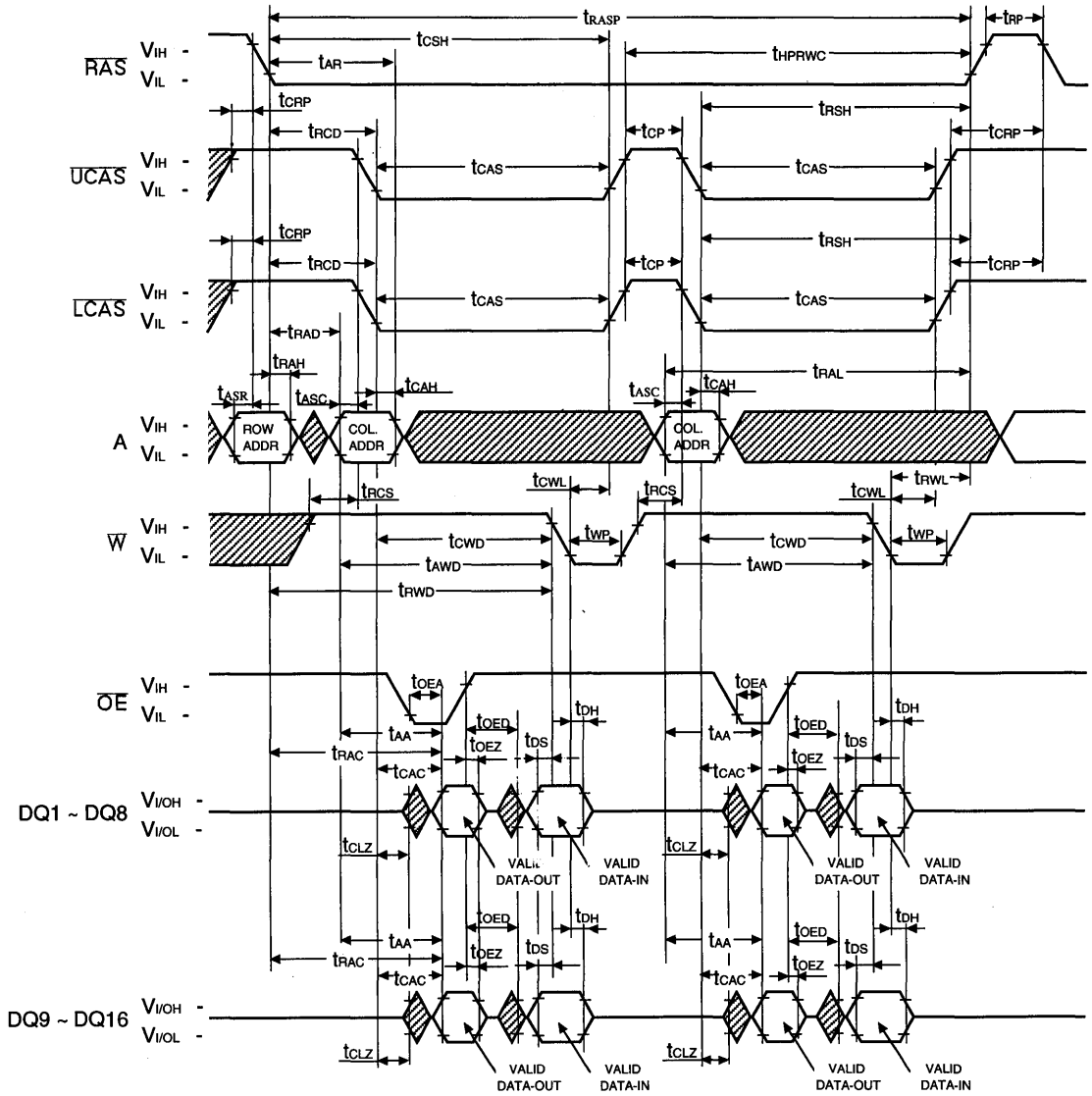
Don't Care

HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

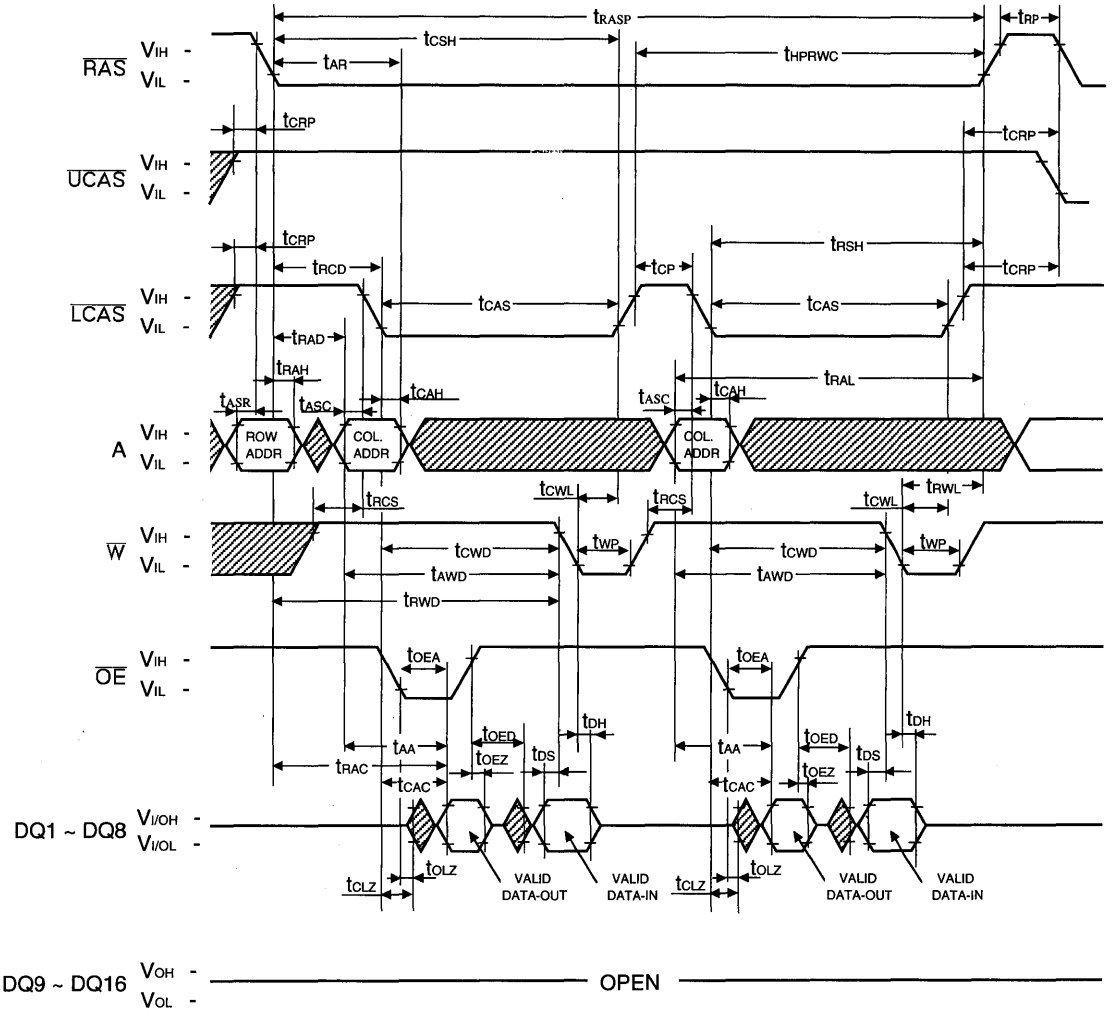


HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE



SAMSUNG ELECTRONICS

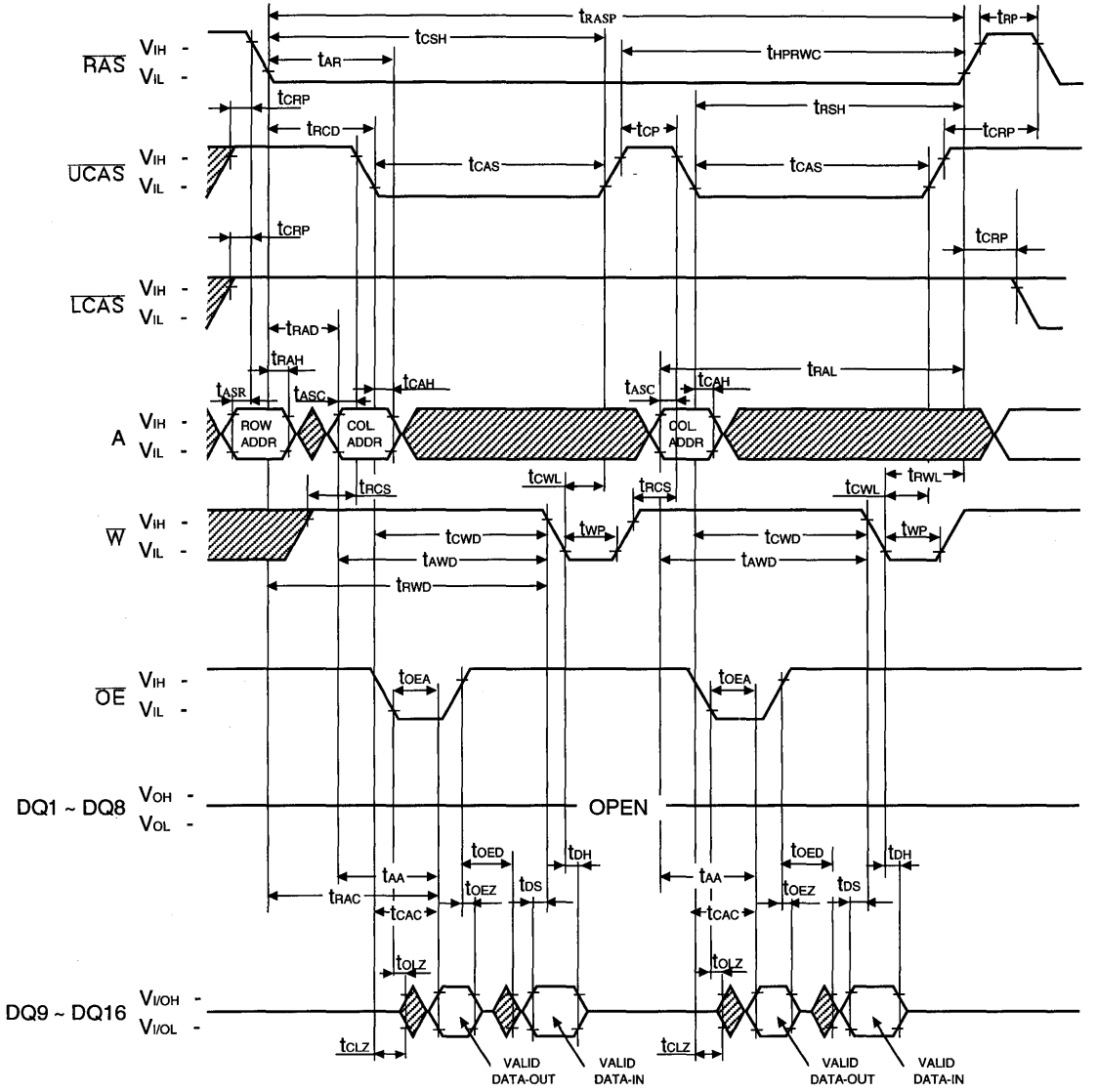
HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



Don't Care

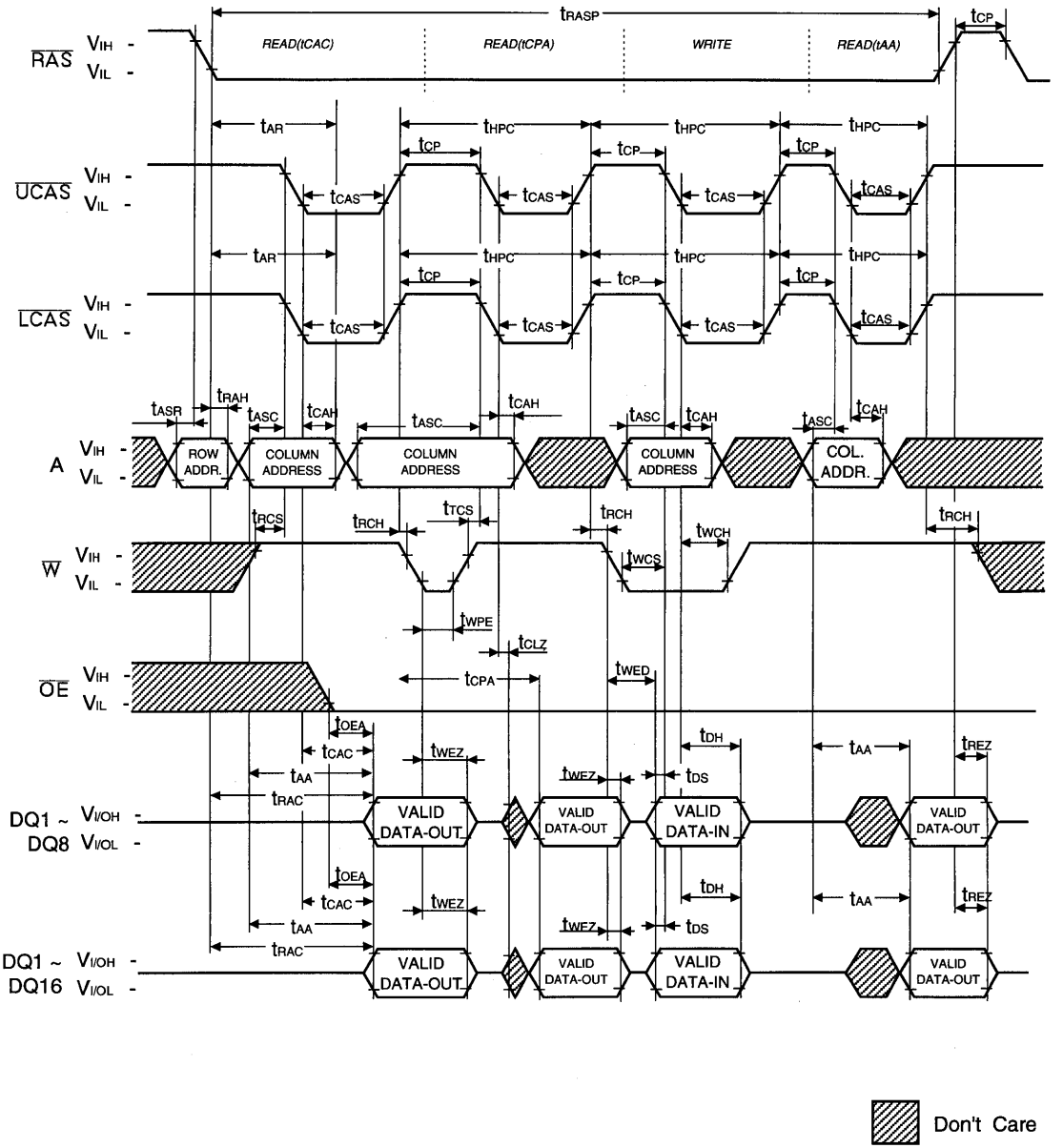
SAMSUNG ELECTRONICS

HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



Don't Care

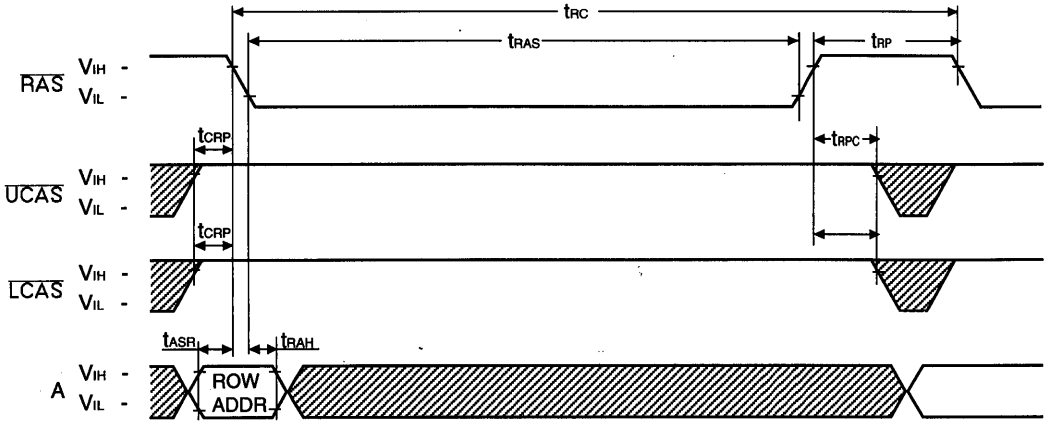
HYPER PAGE READ AND WRITE MIXED CYCLE



SAMSUNG ELECTRONICS

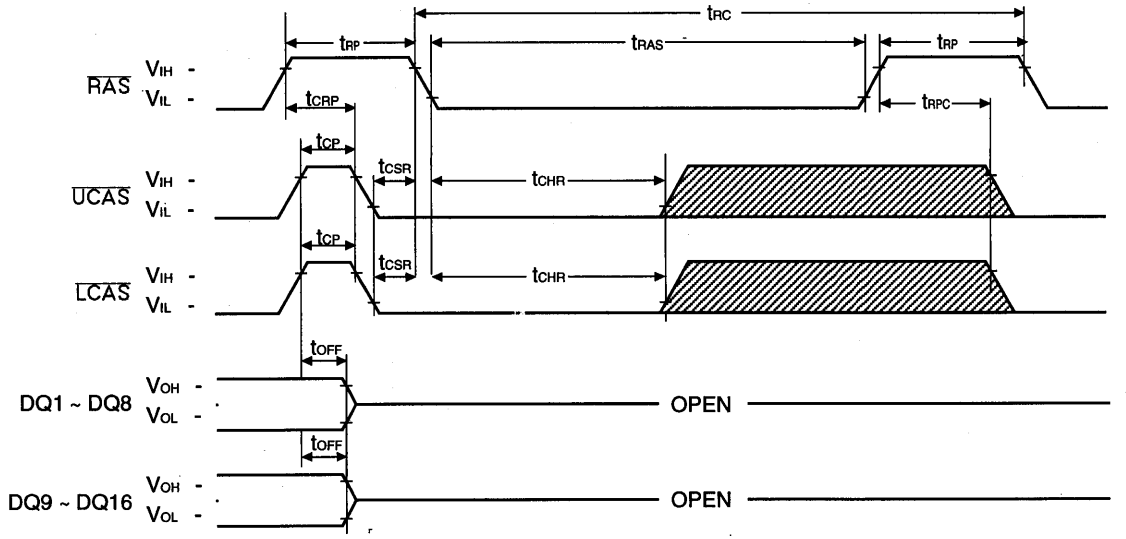
RAS-ONLY REFRESH CYCLE

NOTE : W, OE , DIN = Don't care
DOUT = Open



CAS-BEFORE-RAS REFRESH CYCLE

NOTE : W, OE, A = Don't Care

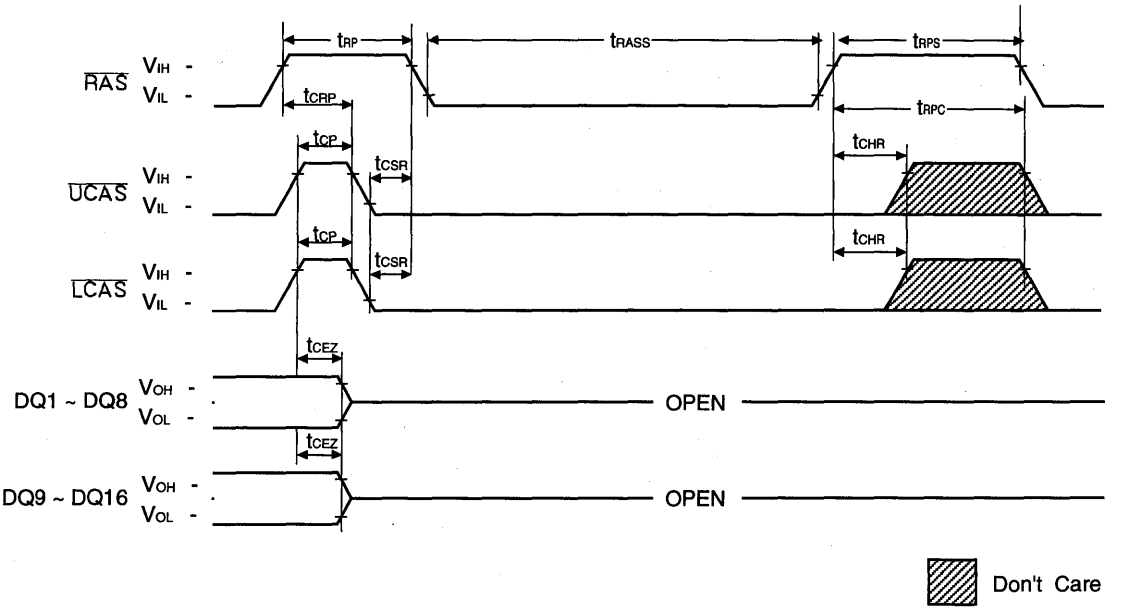


Don't Care

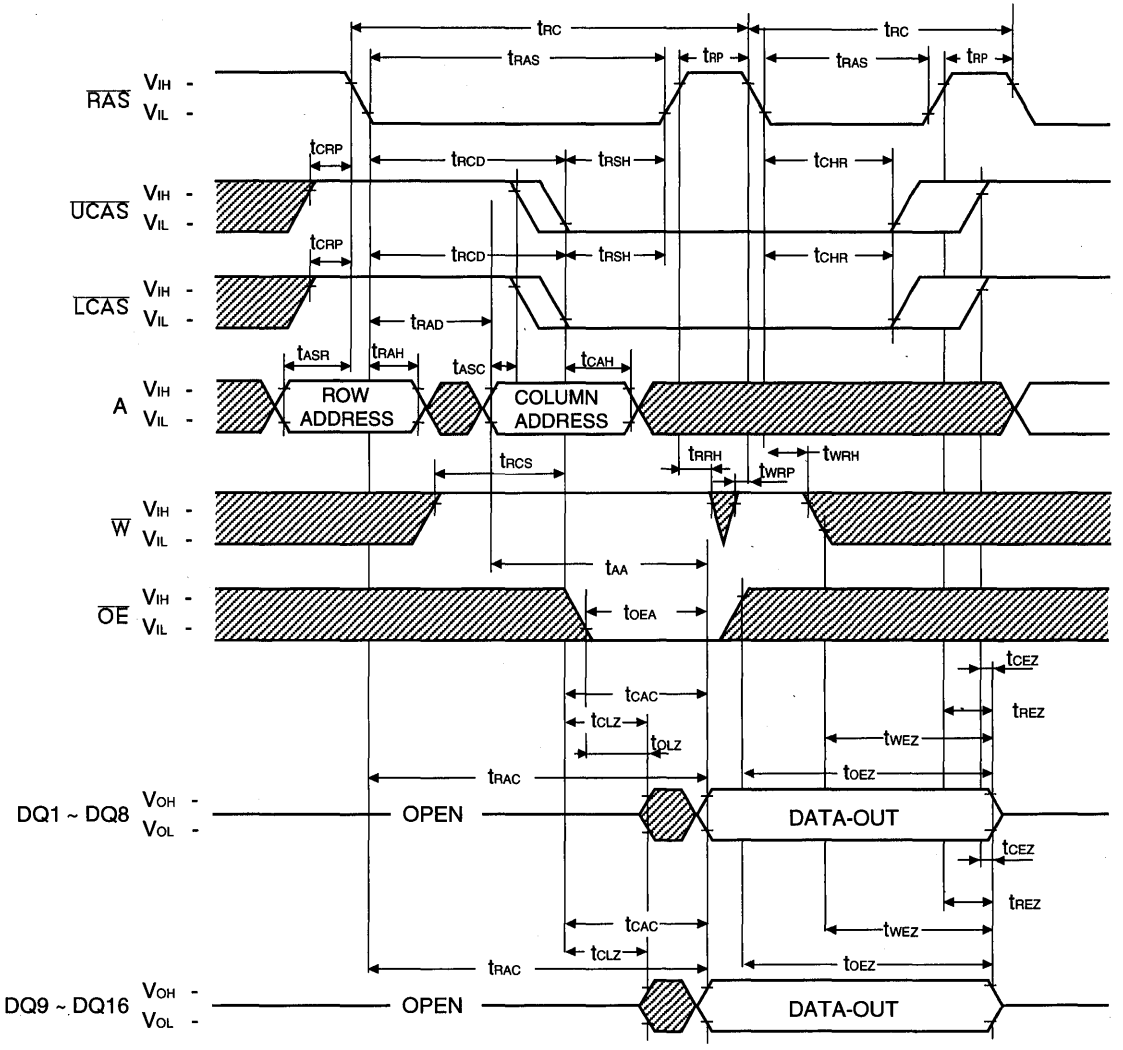
SAMSUNG ELECTRONICS

$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE(LL-version)

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



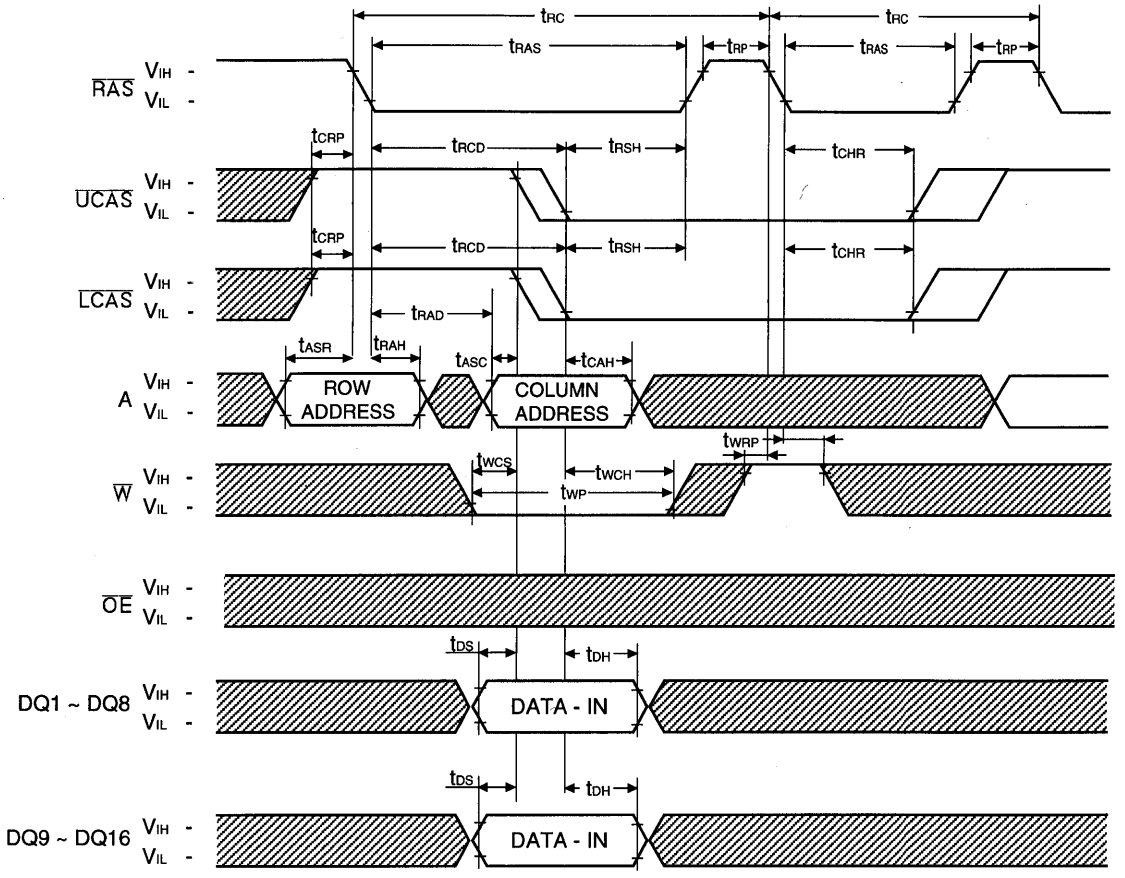
HIDDEN REFRESH CYCLE (READ)



SAMSUNG ELECTRONICS

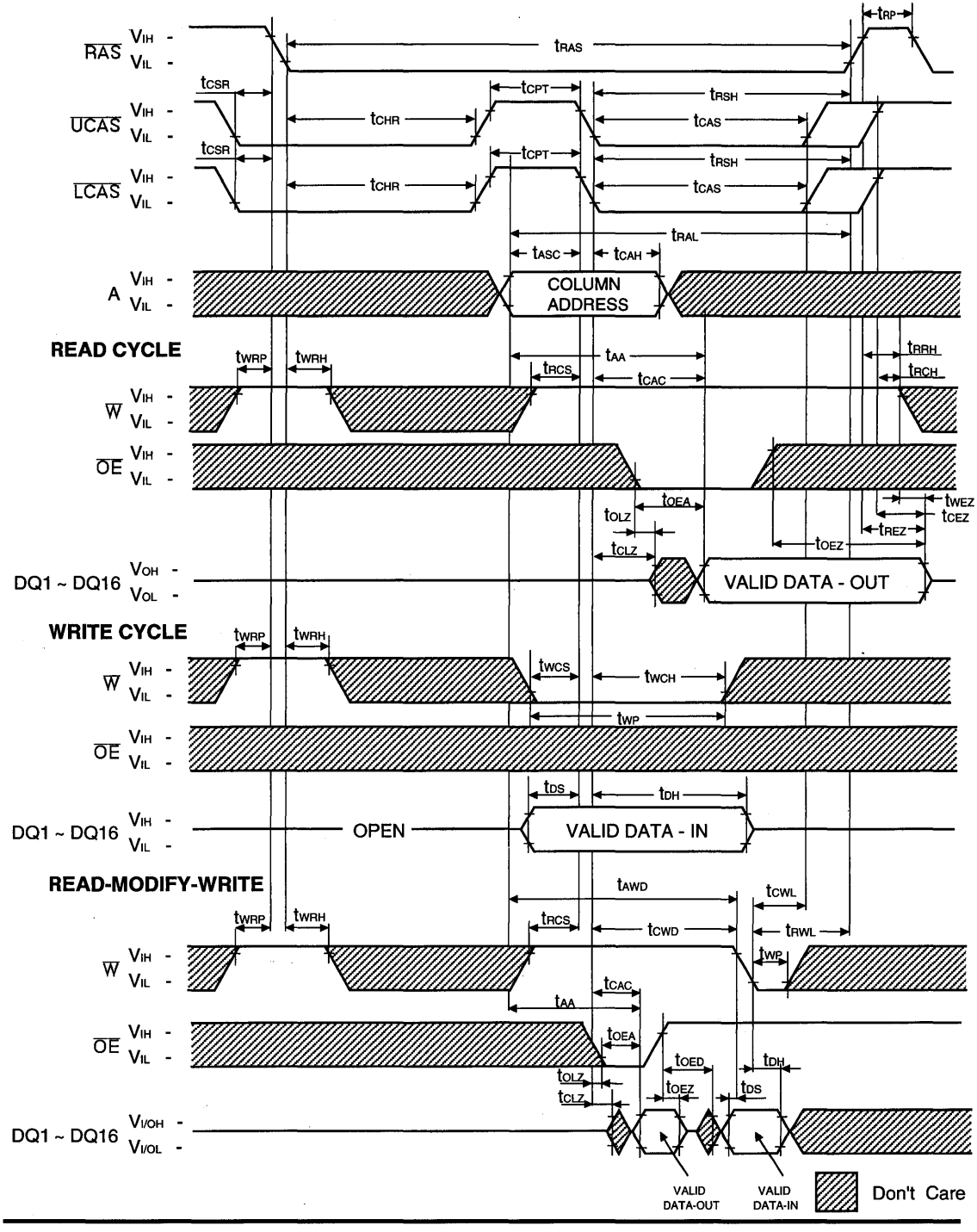
HIDDEN REFRESH CYCLE (WRITE)

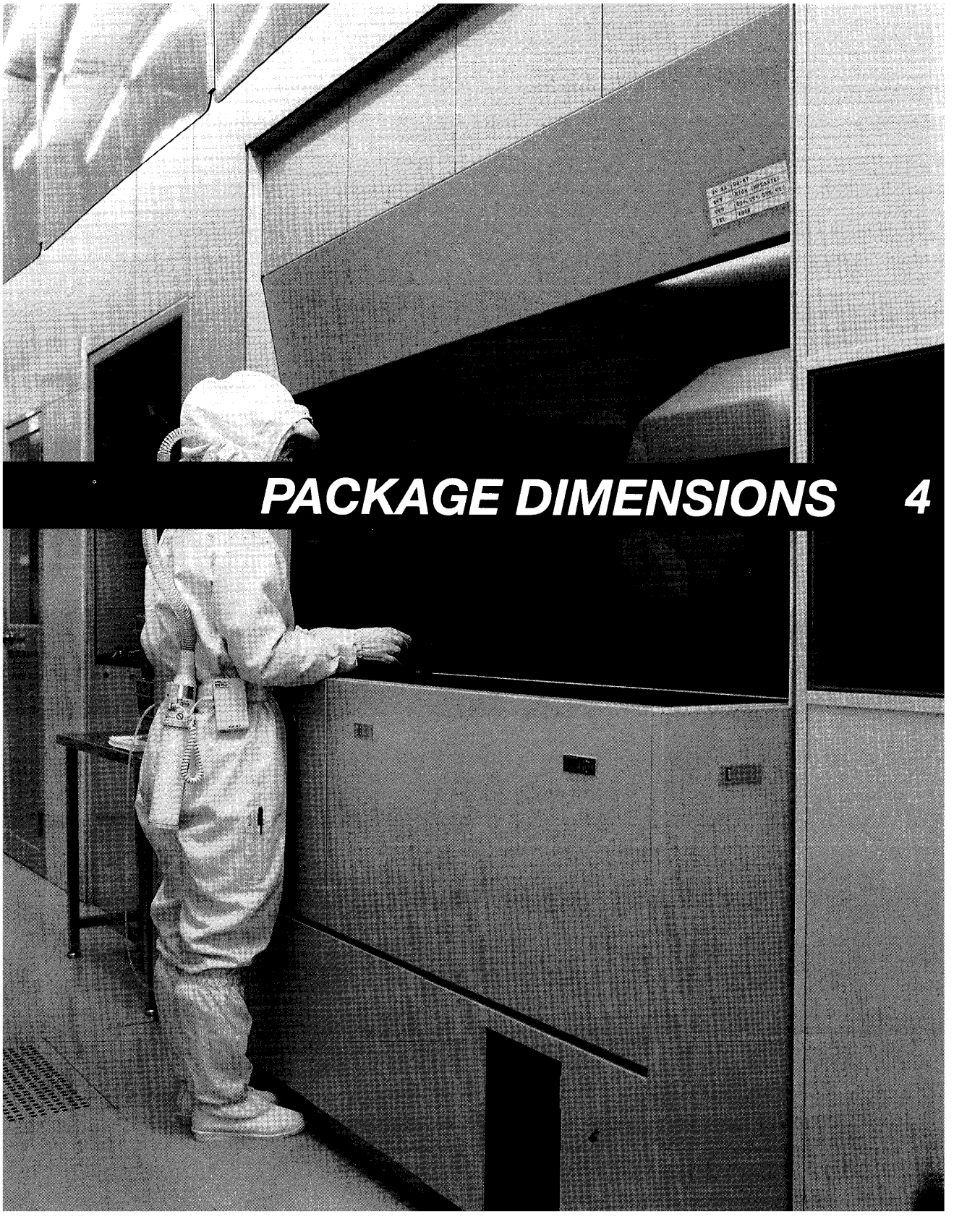
NOTE : D_{OUT} = OPEN



SAMSUNG ELECTRONICS

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

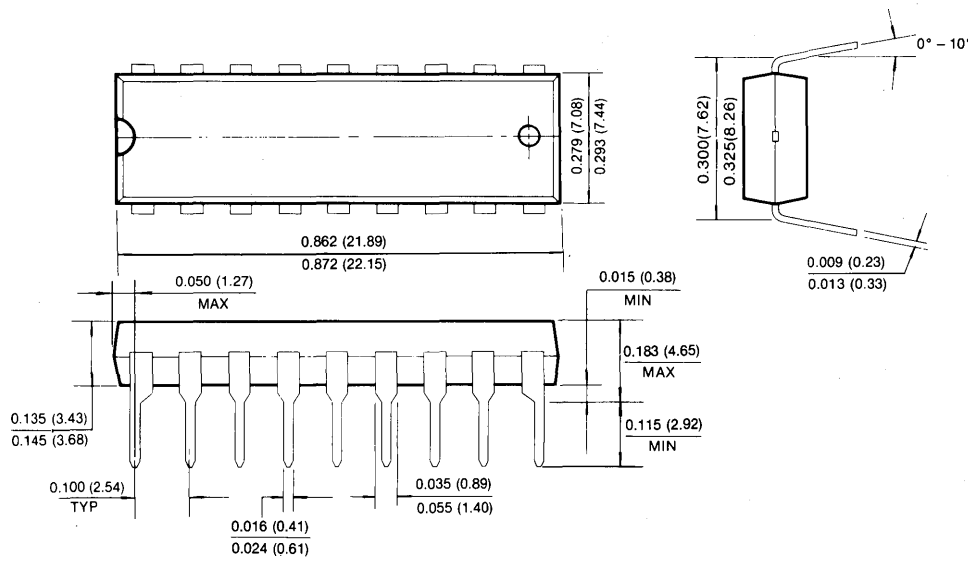




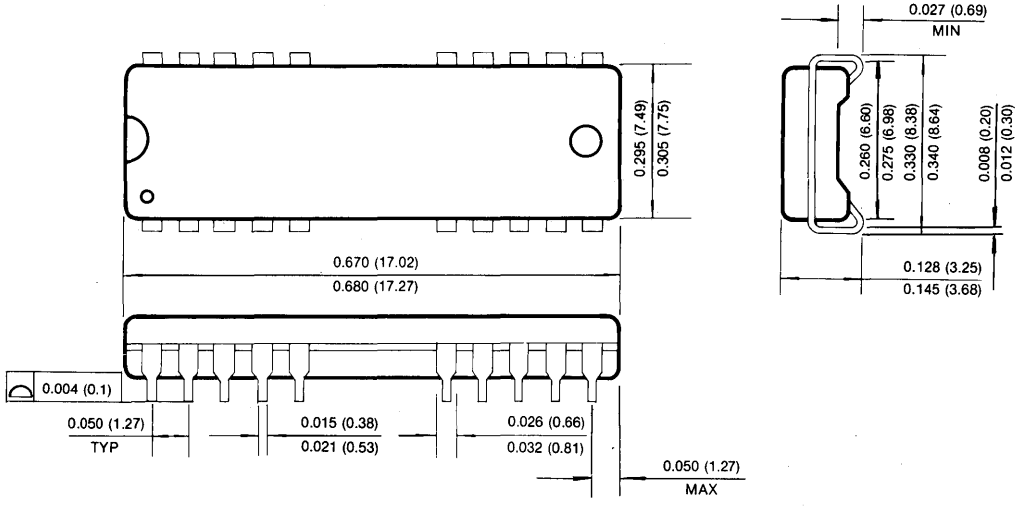
PACKAGE DIMENSIONS 4

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)



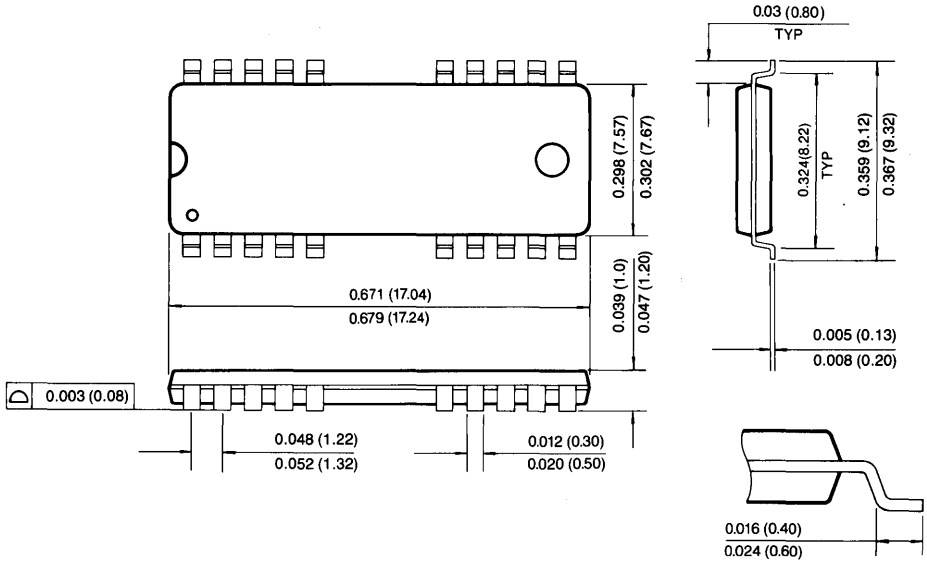
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



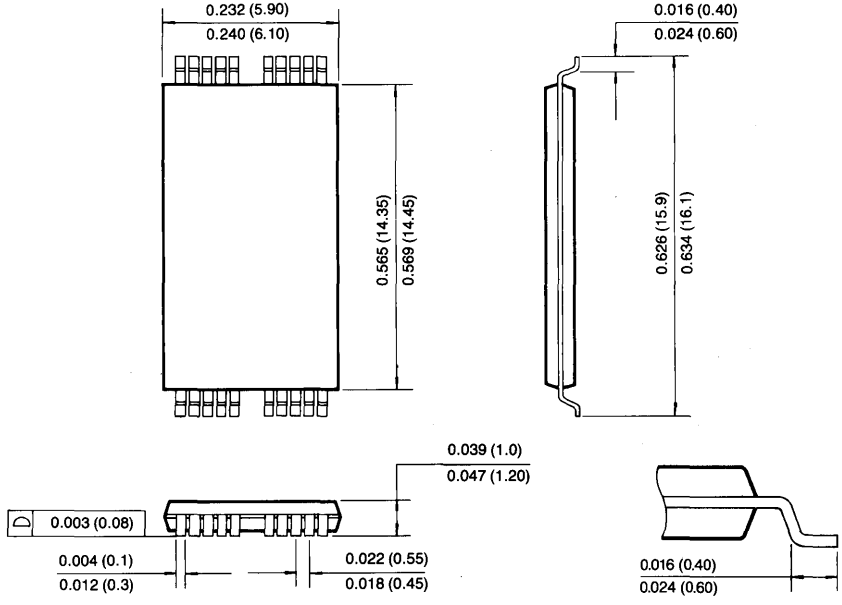
SAMSUNG ELECTRONICS

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)

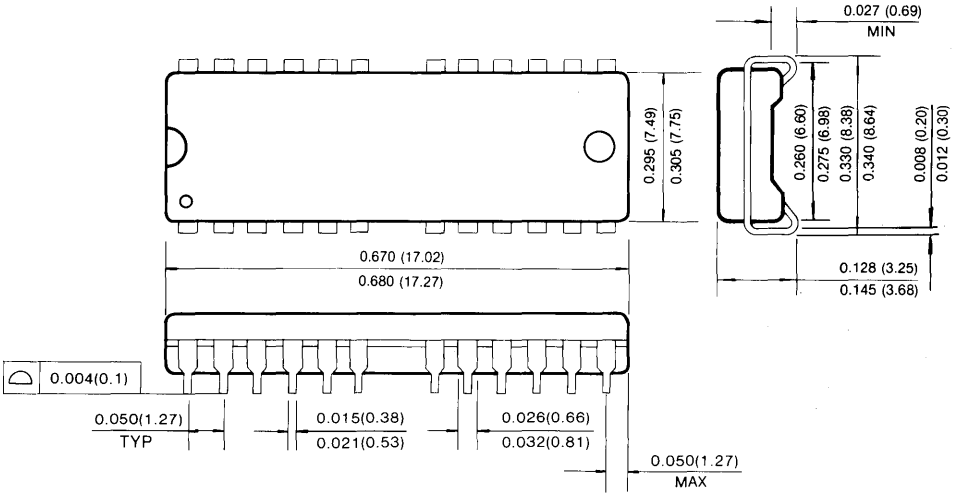


SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS

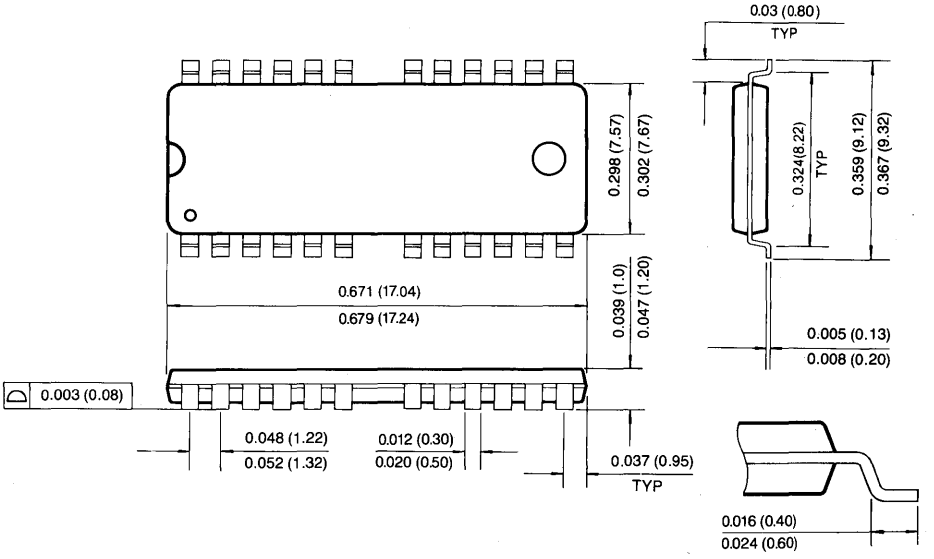
24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



4

24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

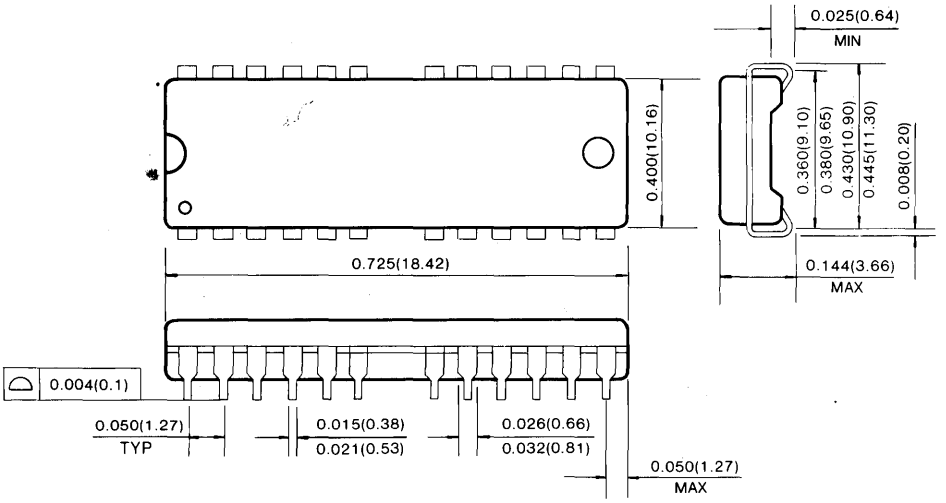


SAMSUNG ELECTRONICS

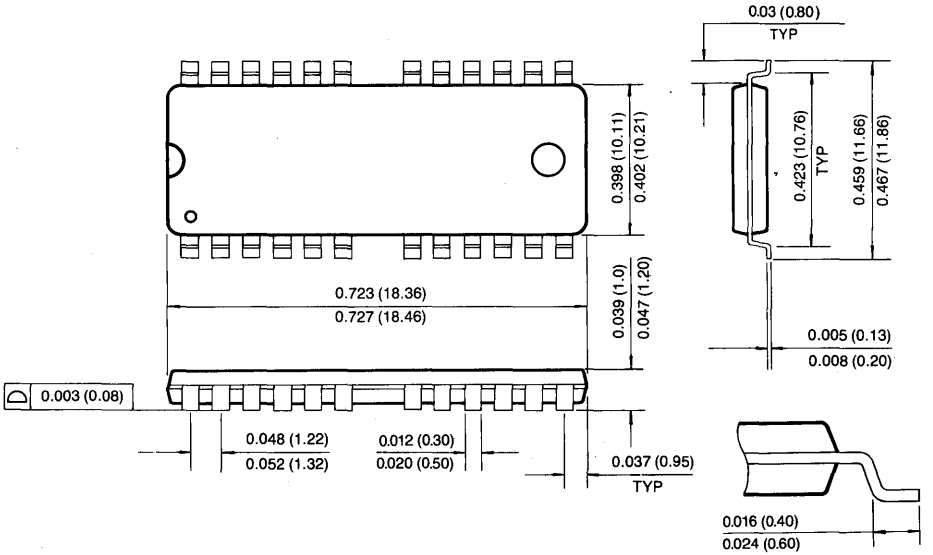
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)

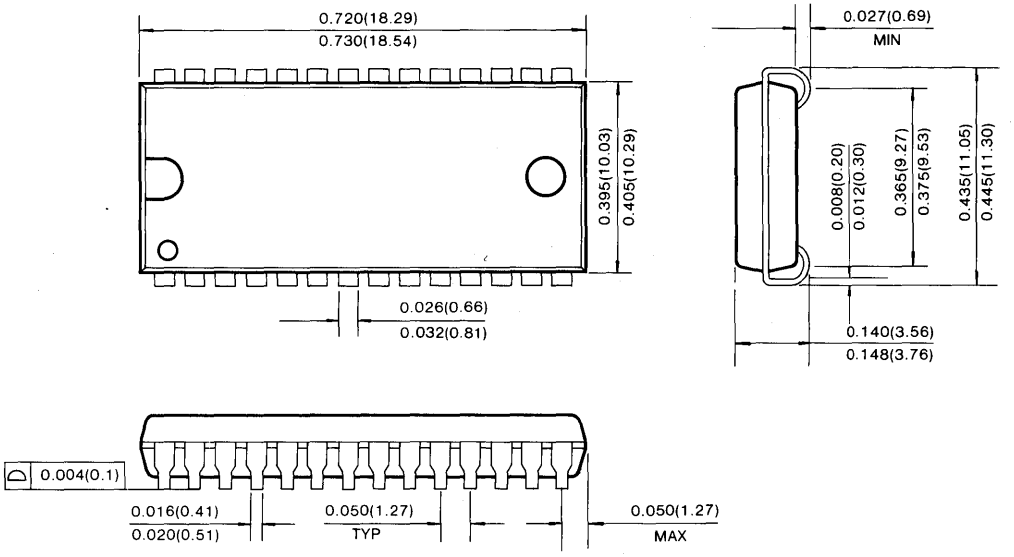


24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



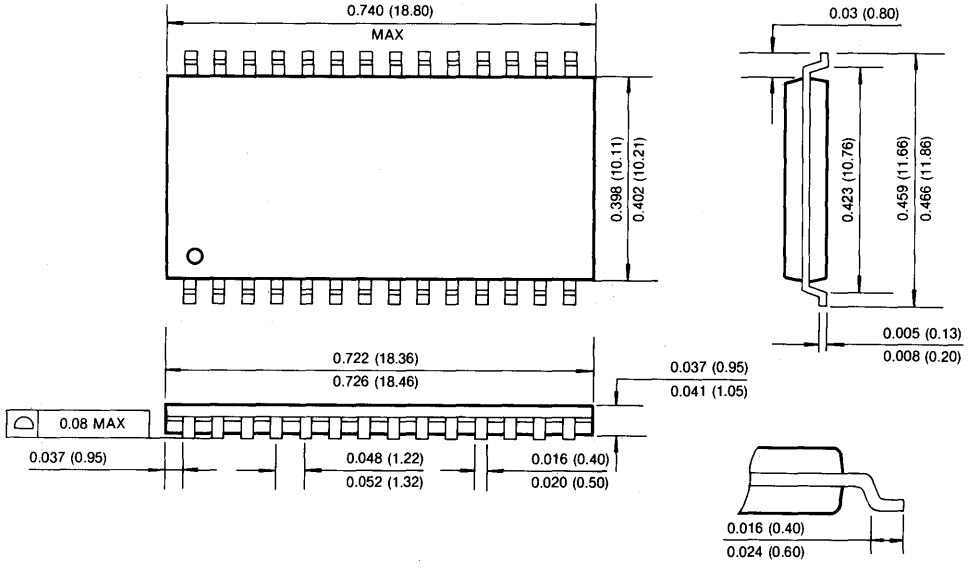
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

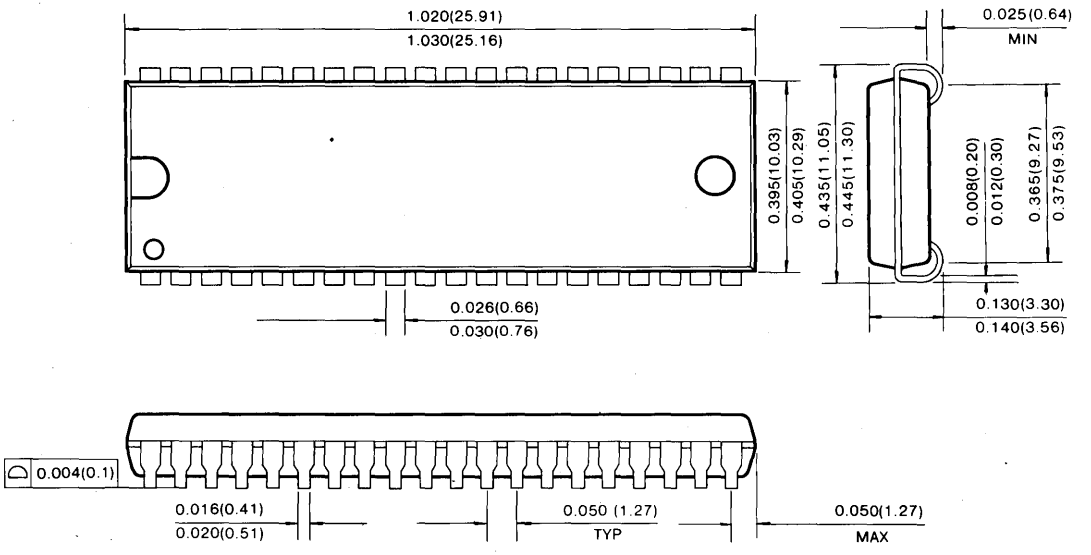
Units: Inches (millimeters)



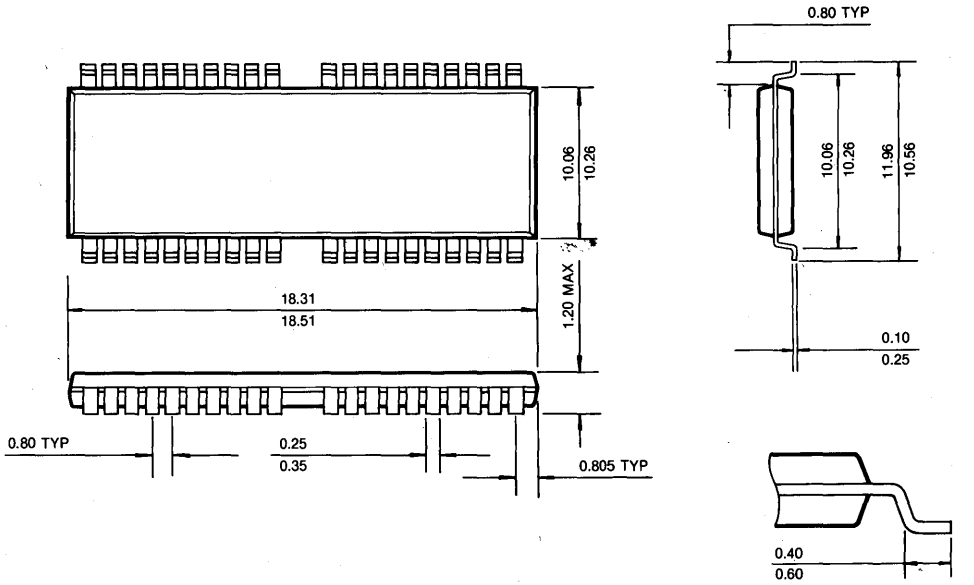
SAMSUNG ELECTRONICS

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



SAMSUNG ELECTRONICS

SALES OFFICES and MANUFACTURER'S REPRESENTATIVES

5

SAMSUNG SEMICONDUCTOR SALES OFFICES-U.S.A.

Northwest
3655 North First Street
San Jose, CA 95134
TEL: (408) 954-7000
FAX: (408) 954-7883

North Central
300 Park Boulevard
Suite 210
Itasca, IL 60143-2636
TEL: (708) 775-1050
FAX: (708) 775-1058

Northeast
119 Russell Street
Littleton, MA 01460
TEL: (508) 486-0700
FAX: (508) 486-8209

Southwest
16253 Laguna Canyon Road
Suite 100
Irvine, CA 92718
TEL: (714) 753-7530
FAX: (714) 753-7544

South Central
15851 Dallas Parkway
Suite 410
Dallas, TX 75248-3307
TEL: (214) 770-7970
FAX: (214) 770-7971

Southeast
802 Greenvalley Road
Suite 204
Greensboro, NC 27408
TEL: (919) 370-1600
FAX: (919) 370-1633

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

ALABAMA
SOUTHERN COMPONENT SALES
307 Clinton Ave. East — TEL: (205) 533-6500
Suite 413 — FAX: (205) 533-6578
Huntsville, AL 35801

ARIZONA
O'DONNELL ASSOCIATES — TEL: (602) 944-9542
2432 W. Peoria Ave. — FAX: (602) 861-2615
Suite 1026
Phoenix, AZ 85029
O'DONNELL ASSOCIATES — TEL: (602) 797-2047
11449 N. Copper Springs Trail — FAX: (602) 797-2047
Tucson, AZ 85737

CALIFORNIA
BESTRONICS — TEL: (619) 693-1111
9683 Tierro Granda Street — FAX: (619) 693-1963
Suite 102
San Diego, CA 92126
I-SQUARED — TEL: (408) 988-3400
3355-1 Scott Blvd. — FAX: (408) 988-2079
Suite 102
Santa Clara, CA 95054
WESTAR REP COMPANY — TEL: (714) 453-7900
15265 Alton Parkway — FAX: (714) 453-7930
Suite 400
Irvine, CA 92718
WESTAR REP COMPANY — TEL: (818) 880-0594
26500 Agoura Rd. — FAX: (818) 880-5013
Suite 204
Calabasas, CA 91302

CANADA
INTELATECH, INC. — TEL: (613) 762-8014
275 Michael Copeland Drive — FAX: (613) 253-1370
Kanata, Ontario K2M 2G2
INTELATECH, INC. — TEL: (514) 343-4877
3700 Griffith Street — FAX: (514) 343-4355
Suite 93
St. Laurent, Quebec H4T 1A7
INTELATECH, INC. — TEL: (905) 629-0082
5525 Orbitor Drive — FAX: (905) 629-1795
Suite 2
Mississauga, Ontario L4W4Y8

COLORADO
FRONT RANGE MARKETING — TEL: (303) 443-4780
3100 Arapahoe Road — FAX: (303) 447-0371
Suite 404
Boulder, CO 80303

FLORIDA
B/B TECH SALES — TEL: (305) 477-0341
3900 N.W. 79th Avenue — FAX: (305) 477-0343
Suite 636
Miami, FL 33166
DYNE-A-MARK — TEL: (407) 660-1661
500 Winderley Place — FAX: (407) 660-9407
Suite 110
Maitland, FL 32751
DYNE-A-MARK — TEL: (305) 485-3500
3355 N.W. 55th Street — FAX: (305) 485-6555
Fort Lauderdale, FL 33309
DYNE-A-MARK — TEL: (407) 725-7470
742 Penguin Ave., NE — FAX: (407) 984-2718
Palm Bay, FL 32905
DYNE-A-MARK — TEL: (813) 345-9411
7884 Tent Avenue S — FAX: (813) 345-3731
St. Petersburg, FL 33707

GEORGIA
SOUTH ATLANTIC COMPONENT SALES
3300 Holcomb Bridge Road — TEL: (404) 447-6154
Suite 210 — FAX: (404) 447-6714
Norcross, GA 30092

ILLINOIS
DAVIX INTERNATIONAL LTD.
1655 N. Arlington Heights Rd. — TEL: (708) 259-5300
Suite 204East — FAX: (708) 259-5428
Arlington Heights, IL 60004

INDIANA
GEN II MARKETING, INC. — TEL: (317) 848-3083
31 E. Main Street — FAX: (317) 848-1264
Carmel, IN 46032
GEN II MARKETING, INC — TEL: (219) 436-4485
1415 Magnavox Way — FAX: (219) 436-1977
Suite 130
Ft. Wayne, IN 46804

5

IOWA

ASSOCIATED ELECTRONIC MARKETERS, INC.
4001 Shady Oak — TEL: (319) 377-1129
Marion, IA 52302 — FAX: (319) 377-1539

KANSAS

ASSOCIATED ELECTRONIC MARKETERS, INC.
8843 Long St. — TEL: (913) 888-0022
Lenexa, KS 66215 — FAX: (913) 888-4848

KENTUCKY

GEN II MARKETING, INC. — TEL: (502) 894-9903
4012 Dupont Circle — FAX: (502) 893-2435
Suite 414
Louisville, KY 40207

MASSACHUSETTS

NEW TECH SOLUTIONS, INC. — TEL: (617) 229-8888
111 South Bedford Street — FAX: (617) 229-1614
Suite 102
Burlington, MA 01803

MICHIGAN

MICROTECH SALES — TEL: (313) 459-0200
9357 General Drive — FAX: (313) 459-0232
Suite 116
Plymouth, MI 48170

MINNESOTA

GP SALES, INC. — TEL: (612)831-2362
7600 Parklawn — FAX: (612) 831-2619
Suite 315
Edina, MN 55435

MISSOURI

ASSOCIATED ELECTRONIC MARKETERS, INC.
11520 St. Charles Rock Rd. — TEL: (314) 298-9900
Suite 131 — FAX: (314) 298-8660
Bridgeton, MO 63044

NEW YORK

NEPTUNE ELEC. — TEL: (516) 349-1600
255 Executive Dr. — FAX: (516) 349-1343
Suite 211
Plainview, NY 11803

T-SQUARED — TEL: (315) 699-1559
6170 Wynmoor Drive — FAX: (315) 699-1705
Cicero, NY 13039

T-SQUARED — TEL: (716) 924-9101
7353 Victor-Pittsford Road — FAX: (716) 924-4946
Victor, NY 14564

T-SQUARED — TEL: (607) 625-3983
1790 Pennsylvania Avenue — FAX: (607) 625-5294
Apalachin, NY 13732

NORTH CAROLINA

SOUTH ATLANTIC COMPONENT SALES
5200 Park Road — TEL: (704) 525-0510
Suite 103 — FAX: (704) 525-9714
Charlotte, NC 28209

SOUTH ATLANTIC COMPONENT SALES
4904 Waters Edge Drive — TEL: (919) 859-9970
Suite 268 — FAX: (919) 859-9974
Raleigh, NC 27606

OHIO

J.N. BAILEY & ASSOCIATES — TEL: (513) 687-1325
129 W. Main Street — FAX: (513) 687-2930
New Lebanon,OH 45345

J.N. BAILEY & ASSOC.IATES — TEL: (614) 262-7274
3591 Milton Avenue — FAX: (614) 262-0384
Columbus, OH 43214

J.N. BAILEY & ASSOCIATES — TEL: (216) 273-3798
1667 Devonshire Drive — FAX: (216) 225-1461
Brunswick,OH 44212

OREGON

ATMI — TEL: (503) 643-8307
4900 SW Griffith — FAX: (503) 643-4364
Suite 155
Beaverton, OR 97005

PENNSYLVANIA

CMS SALES & MARKETING — TEL: (215) 834-6840
527 Plymouth Road — FAX: (215) 834-6848
Suite 420
Plymouth Meeting, PA 19462

PUERTO RICO

DIGIT-TECH
P.O. Box 1945 — TEL: (809) 892-4260
Calle Cruz #2 — FAX: (809) 892-3366
Bajos, San German
Puerto Rico 00753

TEXAS

O'DONNEL ASSOCIATES — TEL: (915) 778-2581
5959 Gateway West — FAX: (915) 778-6429
Suite 558
El Paso, TX 79925

VIELOCK ASSOCIATES — TEL: (214) 881-1940
555 Republic Drive — FAX: (214) 423-8556
Suite105
Plano,TX 75074

VIELOCK ASSOCIATES — TEL: (512) 345-8498
9430 Research Blvd. — FAX: (512) 346-4037
Echelon Bldg. 2, Suite 330
Austin, TX 78759

VIELOCK ASSOCIATES — TEL: (713) 974-3287
10700 Richmond Avenue — FAX: (713) 974-3289
Suite 108
Houston, TX 77042

UTAH

FRONT RANGE MARKETING, INC.
488 E. 6400 South — TEL: (801) 288-2500
Suite 280 — FAX: (801) 288-2505
Murray, UT 84107

WASHINGTON

ATMI — TEL: (206) 869-7636
8521 154th Ave., NE — FAX: (206) 869-9841
Redmond,WA 98052

WISCONSIN

DAVIX INTERNATIONAL LTD. — TEL: (414) 255-1600
N91 W17194 Appleton Avenue — FAX: (414) 255-1863
Menomonee Falls, WI 53051

• • • • •

SAMSUNG SEMICONDUCTOR SALES OFFICES-EUROPE

SAMSUNG SEMICONDUCTOR EUROPE GmbH
Am Unisyspark 1,
65843 Sulzbach (Germany)
TEL: 0049-6196-582-06
FAX: 0049-6196-750-345

MUENCHEN OFFICE
Cari-Zeiss-Ring 9
D-85737 Ismaning bei
Muenchen
TEL: 0049-89-964838
FAX: 0049-89-964873

MILANO OFFICE
Viale G. Matteotti, 26
1-20095 Cusano
Milanino
TEL: 0039-2-66400181
FAX: 0039-2-6192279

LONDON
Samsung House
225 Hook Rise South
Surbiton
Surrey
KT6 7LD
TEL: 0044-81-3914550
FAX: 0044-81-9742540

BIRMINGHAM OFFICE
Florence House St.
Mary's Road Hinckley,
Leicestershire LE10
1EQ
TEL: 0044-455-891111
FAX: 0044-455-612345

PARIS OFFICE
Centre d'Affaires La
Boursidiere RN 186, Bat.
Bourgogne, BP 202
92357 Le Plessis-Robinson
TEL: 0033-1-40940700
FAX: 0033-1-40940216

STOCKHOLM OFFICE
Bergkaellavaegen 32
P.O. Box 319
S-19130 Sollentuna
TEL: 0046-8-6269626
FAX: 0046-8-6268638

BARCELONA OFFICE
C. Provenza, 5193-1
E-08025 Barcelona
TEL: 0034-3-4-504876
FAX: 0034-3-4-331944

BELGIUM OFFICE
Rue de Geneve 10,
B3 B-1140 Brussels
TEL: 0032-2-2456510
FAX: 0032-2-2456313

SAMSUNG SEMICONDUCTOR-REPRESENTATIVES

EUROPE

BELGIUM

DANE-LEC BELGIUM
91-93 Rue J.D. Navez — TEL : 0032-2-2167058
B-1210 Bruxelles — FAX : 0032-2-2166871

DENMARK

EXATEC A/S
Mileparken 20E — TEL : 0045-44927000
DK-2740 Skovlunde — FAX : 0045-44926020

MIKO KOMPONENT AB
Segersbyvaegen 3 — TEL : 0046-853189080
S-14502 Norsborg — FAX : 0046-853175340

FINLAND

TAHINIK OY
P.O. Box 125 — TEL : 00358-1482177
SF-00241 Helsinki — FAX : 00358-1482189

OY FINTRONIC AB
Pyyntitie 3 — TEL : 00358-0887331
SF-02230 Espoo — FAX : 00358-088733342

FRANCE

MEGACHIP
7 avenue du Canada — TEL : 0033-1-69290404
ZA de Courtaboeuf — FAX : 0033-1-69290039
91966 LES UILIS Cedex
FRANCE

SCAIB
80 Rue d'Arcueil — TEL : 0033-1-46872313
Silic 137 — FAX : 0033-1-45605549
94523 RUNGIS Cedex
FRANCE

GERMANY

ASTRONIC GmbH
Gruenwalder Weg 30 — TEL : 0049-89-6130303
D-82041 Deisenhofen — FAX : 0049-89-6131668

CANNING ELECTRONIC DISTRIBUTION CED GmbH
Laatzener Str. 19 — TEL : 0049-511-87640
D-30539 Hannover Delete — FAX : 0049-551-8764160

MSC VERTRIEBS GmbH
Industrie Str. 16 — TEL : 0049-7249-9100
D-76297 Stutensee 3 — FAX : 0047-7249-7993

MICRONETICS GmbH
Dieselstrasse 12 — TEL : 0049-7159-92583-0
D-71272 Renningen — FAX : 0049-7159-9258355

SILCOM ELECTRONICS VERTRIEBS GmbH
Hindenburg Str. 284 — TEL : 0049-2161-15074
D-41061 Moenchengladbach — FAX : 0049-2161-183313

ITALY

DEUTSCHE ITT INDUSTRIES GmbH
Viale Milanofiori E/5 — TEL : 0039-2-824701
I-20090 Assago Mi — FAX : 0039-2-8242631/8242831

FANTON COMPONENTS BOLOGNA S.R.L.
Via O. Simoni, 5 — TEL : 0039-51-735015
I-40011 Anzola dell' Emilia — FAX : 0039-51-735013

RAFI ELETTRONICA SPA
Via Savona 134 — TEL : 0039-2-48300431
I-20144 Milano — FAX : 0039-2-428880

5

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

THE NETHERLANDS

MALCHUS BV HANDELMIJ
Fokkerstraat 511-513
Postbus 48
NI-3125 BD Schiedam
TEL: 0031-10-4277777
FAX: 0031-10-4154867

SPAIN

SEMICONDUCTORS S.A.
Ronda General Mitre
240 Bjs
E-08006 Barcelona
TEL: 0034-3-2172340
FAX: 0034-3-2176598

SWEDEN

MIKO KOMPONENTS
Segersbyvaegen 3
P.P. Box 2001
S-14502 Norsborg
TEL : 0046-853-189080
FAX : 0046-853-175340

SWITZERLAND

ELBATEX AG
Hard Str. 72
CH-5430 Wettingen Schweiz
TEL : 0041-56275511
FAX : 0041-56275532

UNITED KINGDOM

MAGNATEC
Coventry Road
Lutterworth
Leicestershire
LE17 4JB
TEL : 0044-455-554711
FAX : 0044-455-552612

ICE ELECTRONICS LTD.
31-32 Stephenson Road
Burrel Road Industrial Estate
St. Ives
Cambridgeshire
PE17 4WJ
TEL : 0044-480-496466
FAX : 0044-480-496621

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

ASIA

HONG KONG

AV. CONCEPT LTD.
Unit 11-15, 11/F1, Block A, Focal Industrial Centre
21 Man Lok Street, Hunghom, Kowloon, Hong Kong
TEL : 3347333
FAX : 7643108

PROTECH COMPONENTS LTD.
Unit 2,3/F, Wah Shing Centre, 11 Shing Yip Street, Kwun Tong, Kowloon, Hong Kong
TEL : 7930882
FAX : 7930811

WISEWORLD ELECTRONICS LTD.
Room 708, Tower A, 7/Fl., Hunghom Commercial Centre, 37-39 Ma Tau Wai Road, Hunghom, Kowloon, Hong Kong
TEL : 7658923
FAX : 3636203

IBDT HK LTD. (CHINA AREA)
Unit 2, 23rd floor, Westlands Center, No.20 Westlands Road, Quarry Bay, Hong Kong
TEL : 565-5898
FAX : 564-5411

SOLARBRITE ELECTRONICS LTD.
(CALCULATOR & WATCH)
Unit 1, 11/F, Tower 1, Harbour Centre, 1, Hok cheung St, Hunghom, Kowloon, Hong Kong
TEL : 3633233
FAX : 3633900
TLX : 52543 SECL HX

ATLANTIC COMPONENTS LTD.
(MEMORY & PC)
Unit 502, 5/F, Tower III, Enterprise Square, 9 Sheung Yuet Road, Kowloon Bay, Kowloon, Hong Kong
TEL: 7991996
FAX: 7559452

LISENG & CO.
(4BIT/8BIT ONE CHIP SOFTWARE HOUSE)
Flat B&C, 6/F, Four Seas Communication Bank Bldg, 49-51 Bonham Strand West, Hong Kong
TEL : 5431338
FAX : 5442602

SOLARI COMPUTER ENGINEERING LTD.
(4 BIT/8BIT ONE CHIP SOFTWARE HOUSE)
Roon 2018-2025, Tower 1, Metroplaza, Kwai Fong, N.T., Hong Kong
TEL : 418-0988
FAX : 418-0887

DATAWORLD INTERNATIONAL LTD.
(MIYUKI ELECTRONICS (HK) LTD.)
(ASIC DESIGN HOUSE)
Flat No. 3-4,5/Fl., Yuen Shing Ind. Bldg., 1033, Yee Kuk Street, West, Kowloon, Hong Kong
TEL : 7862611
FAX : 7856213
TLX : 45876 MYK HX

SYNTHESIS SYSTEMS DESIGN, LTD.
(ASIC DESIGN HOUSE)
Unit 4,12/F Chai Wan Ind. City, Phase 2, No. 70, Wing Tai Road, Chai Wan, Hong Kong
TEL : 557-1102
FAX : 889-2962

TAIWAN

YOSUN INDUSTRIAL CORP.
7F, No. 76, Sec. 1, Cheng Kung Rd. Nan Kang, Taipei, R.O.C.
TEL : (02)788-1991
FAX : (02)788-1996

SANT SONG CORP.
4F, No.12, Lane 94, Tsao Ti Wei, Shen Keng Hsiang, Taipei Hsien, Taiwan, R.O.C.
TEL : (02) 662-7829
FAX : (02) 662-0781

SUPREME ELECTRONICS CO., LTD.
18Fl., No.67, Section 2, Tun hwa S. Road, Taipei, Taiwan, R.O.C.
TEL : (02) 7023258/7023278
FAX : (02) 7063196

JAPAN

TOMEN ELECTRONICS CORP.
1-1 Uchisaiwa-Cho 2 Chome Chiyoda-Ku Tokyo, 100 Japan
TEL : (03) 3506-3654
FAX : (03) 3506-3497

RIKEI
Nichimen Bldg., 2-2 Nakanojima 2 Chome, Kita-Ku, Osaka, 530 Japan
TEL : (06) 201-2081
FAX : (06) 222-1185

ISECO
26-3, Kitamagome 2 Chome, Ota-Ku, Tokyo, 143, Japan
TEL : (03) 3777-3611
FAX : (03) 3777-3614

ADO
7F Sasage Bldg., 4-6 Sotokanda 2 Chome Chiyoda-Ku Tokyo, 101 Japan
TEL : (03) 3257-2600
FAX : (03) 3251-9705

MARUBUN
8-1 Nihombashi-Odenma-Cho Chuo-Ku Tokyo, 103 Japan
TEL : (03) 3639-9897
FAX : (03) 3661-7433

SAMSUNG JAPAN
17F, Hamacho Center BLDG. 2-31-1, Nihonbashi-Hamacho Chuo-ku, TOKYO 103 JAPAN
TEL : (03) 5641-9651
FAX : (03) 5641-9713

5

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

SINGAPORE

ASTINA ELECTRONIC(S) PTE LTD.
203, Henderson Road — TEL : 65-2769997
#12-08 Henderson Industrial Park, — FAX : 65-2769996
Singapore 0315

BOSTEX ELECTRONICS PTE LTD.
No.221 Henderson Road — TEL : 2765130
#04-06 Henderson Building — FAX : 2765132
Singapore 0315

SAMSUNG(THAILAND) CO., LTD.
15th Fl. Sathorn Thani Bldg., — TEL: 662-2367642-5
92/40-41 North Sathorn Road — FAX: 662-2368049
Bankok 10500, Thailand

SOUTH-WEST ELECTRONICS PTE LTD.
30 Kallang Pudding Road, — TEL: 7431813
#04-04 Valiant Industrial Bldg., — FAX: 7471128
Singapore 1334

VUTIPONG ELECTRONIC CO., LTD.
51-53 Pahurat Rd, (Banmoh) — TEL: 662-2266496-9
Bankok 10200, Thailand — FAX: 662-2240861

YIC SINGAPORE PTE, LTD.
623, Aljunied Road, #06-08 — TEL: 65-7490677
Aljunied Industrial Complex, — FAX: 65-7477019
Singapore, 1438

SAMSUNG SINGAPORE PTE, LTD.
4,SHENTON WAY, #18-01/10 — TEL : 65-5352808
Shingwan House, — FAX : 65-2772792
Singapore 0106

INDIA

COMPONENTS AND SYSTEMS MARKETING ASSOCIATES (INDIA) PVT. LTD.
100, Dadasaheb Phalke Road, — TEL: 4114585
Dadar, Bombay 400 — FAX: 4112546
014 — TLX: 001-4605 PDT IN

TURKEY

ELEKTRO SAN. VE TIC. KOLL STI.
Hasanpasa, Ahmet Rasim — TEL: 337-2245
Sok No. 16 Kadikoy Istanbut, — FAX: 336-8814
Turkey — TLX: 29569 elts tr

CHINA

IBDT(HK) LTD. (SHANGHAI LIAISON OFFICE)
Rm 501, — TEL : (021) 4316170
750 Zhao Jia Bang Rang Road, — FAX : (021) 4316170
Shanghai, China

KOREA

NAEWAE SEMICONDUCTOR CO., LTD.
Bangbae Center Bldg., — TEL: (02)595-1010
875-5, Bangbae-4dong, — FAX: (02)595-7888
Seocho-ku, Seoul, Korea

SAMSUNG LIGHT-ELECTRONICS CO., LTD.
4th Fl. Room 2-3, — TEL: 718-0045
Electronics Main Bldg., — 718-9531—5
16-9, Hankangro-3ka, — FAX: 718-9536
Yongsan-ku, Seoul, Korea

NEWCASTLE SEMICONDUCTOR CO., LTD.
4th Fl. Room 410-411, — TEL: 718-8531—4
Electronics Main Bldg., — FAX: 718-8535
16-9, Hankangro-3ka,
Yongsan-ku, Seoul, Korea

HANKOOK SEMICONDUCTOR & TELECOMMUNICATION CO., LTD.
#302, Monami Bldg., 125-20, — TEL: (02)542-4123
Chungdam-dong, Kangnam-ku, — FAX: (02)542-2454
Seoul, Korea

SEGYUNG INTERISE CORP.
Dansan Bldg., 301, 7-44 — TEL : (02)469-3511
Hwayang-dong, Sungdong-ku, — FAX: (02)469-7966
Seoul, Korea

SEGYUNG ELECTRONICS
182-2, Jangsa-dong, — TEL : (02)273-6781
Jongro-ku, Seoul, Korea — FAX: (02)275-9448
TLX: K24950 SUKSEMT

SAMTEK
3/4 FL. Chungju Bldg., — TEL : (02)538-4400
156-16, Samsung-dong, — FAX: (02)538-4338—9
Kangnam-ku, Seoul, Korea

SUNIN TRADING CO., LTD.
Sunin Bldg., 7Fl., 16-8, — TEL: (02)702-1257—8
Hankangro-2ka, Yongsan-ku, — FAX: (02)704-0997
Seoul, Korea

SAMSUNG SEMICONDUCTOR DISTRIBUTORS

ARIZONA

ADDED VALUE (602) 951-9788
7741 East Gray Road FAX: (602) 951-4182
Suite 9
Scottsdale, AZ 85260

CALIFORNIA

ADDED VALUE (714) 259-8258
1582 Parkway Loop FAX: (714) 259-0828
Unit G
Tustin, CA 92680

ADDED VALUE (619) 558-8890
5752 Oberlin Drive FAX: (619) 558-3018
Suite 105
San Diego, CA 92121

ALL AMERICAN (800) 831-8300
369 Van Ness Way (213) 320-0240
Unit 701 FAX: (213) 320-7207
Torrance, CA 90501

ALL AMERICAN (408) 943-1200
2360 Qume Drive, Suite C FAX: (408) 943-1393
San Jose, CA 95131

ALL AMERICAN (619) 458-5850
5060 Shoreham Place FAX: (619) 458-5866
Suite 200
San Diego, CA 92122

I.E.C. (916) 363-6030
9940 Business Park Drive FAX: (916) 362-6926
Suite 145
Sacramento, CA 95827

ITT Components (714) 727-4001
18 Technology Drive FAX: (714) 727-2109
Irvine, CA 92718

ITT Components (408) 453-1404
1580 Oakland Road FAX: (408) 453-1407
Suite C102
San Jose, CA 95131

JACO (714) 258-9003
1541 Parkway Loop FAX: (714) 258-1909
Suite A
Tustin, CA 92680

JACO (805) 495-9998
2282 Townsgate Road (800) 266-1282
Suite 100 FAX: (805) 494-3864
Westlake Village, CA 91361

JACO (408) 432-9290
2880 Zanker Road FAX: (408) 432-9298
Suite 202
San Jose, CA 95134

CANADA

ACTIVE (514) 694-7710
237 Hymus Boulevard FAX: (514) 697-8112
Point Claire, Quebec H9R 5C7

ACTIVE (604) 324-7500
100 S.E. Marine Drive FAX: (604) 324-3100
Vancouver, BC V5X 2S3

ACTIVE (416) 367-2911
100 Lombard Street FAX: (416) 367-4706
Toronto, Ontario M5C 1M3

ACTIVE (514) 731-7441
5651 Ferrier Street FAX: (514) 731-0129
Montreal, Quebec H4AP 1N1

CANADA (Continued)

ACTIVE (403) 235-5300
3220 5th Avenue, N.E. Bay 2 FAX: (403) 248-0750
Calgary, Alberta T2A 5N1

ACTIVE (204) 786-3075
106 King Edward St., E FAX: (204) 783-8133
Winnepeg, Manitoba R3H 0N8

ACTIVE (416) 238-8825
1350 Matheson Blvd, Unit 2 FAX: (416) 238-2817
Mississauga, Ontario L4W 4MI

ACTIVE (403) 438-5888
6029 103rd St. FAX: (403) 434-0812
Edmonton, Alberta T6H 2H3

ACTIVE (418) 682-5775
1990 Blvd. Charest O. FAX: (418)682-8303
Ste-Foy, Quebec G1N 4K8

ACTIVE (613) 728-7900
1023 Merivale Road FAX: (613) 728-3586
Ottawa, Ontario K1Z 6A6

ACTIVE (514) 256-7538
6080 Metropolitan East FAX: (514) 256-4890
Montreal, Quebec H1S 1A9

COLORADO

ADDED VALUE (303) 422-1701
4090 Youngfield FAX: (303) 422-2529
Wheatridge, CO 80033

I.E.C. (303) 292-5537
420 East 58th Avenue FAX: (303) 292-0114
Denver, CO 80216

I.E.C. (303) 292-6121
5750 North Logan Street FAX: (303) 297-2053
Denver, CO 80216

Q.P.S. (303) 343-9260
14291 E. 4th Avenue FAX: (303) 343-3051
Bldg. 7, Unit 208
Aurora, CO 80011

FLORIDA

ALL AMERICAN (305) 621-8282
16085 NW 52 Avenue FAX: (305) 620-7831
Miami, FL 33014-9317

ALL AMERICAN (800) 327-6237
5009 Hiatus Road FAX: (305) 749-9229
Sunrise, FL 33351

JACO (407) 241-7943
1060 Holland Drive FAX: (407) 241-7950
Suite 3K
Boca Raton, FL 33487

RM ELECTRONICS (407) 767-8005
581 East St. Rte. 434 FAX: (407) 767-8165
Longwood, FL 32750

ILLINOIS

I.E.C. (708) 843-2040
2200 N. Stronington Ave., FAX: (708) 843-2320
Suite 210
Hoffman Estates, IL 60195

QPS (708) 884-6620
101 E. Commerce Dr. FAX: (708) 884-7573
Schaumburg, IL 60173

5

INDIANA

RM ELECTRONICS (317) 580-9999
1329 W. 96th Street FAX: (317) 580-9615
Suite 10
Indianapolis, IN 46260

MARYLAND

ALL AMERICAN (301) 251-1205
14636 Rothgeb Dr. FAX: (301) 251-8574
Rockville, MD 20850

JACO (410) 995-6620
Rivers Center FAX: (410) 995-6032
10270 Old Columbia Road
Columbia, MD 21046

MASSACHUSETS

ALL AMERICAN (617) 246-2300
107 Audubon Road FAX: (617) 246-2305
Suite 104
Wakefield, MA 01880

JACO (508) 640-0010
1053 East Street. FAX: (508) 640-0755
Tewksbury, MA 01876

MICHIGAN

RM ELECTRONICS (616) 531-9300
4310 Roger B. Chaffee Drive FAX: (616) 531-2990
Grand Rapids, MI 49508

MINNESOTA

ALL AMERICAN (612) 944-2151
11409 Valley View Road FAX: (612) 944-9803
Eden Prairie, MN 55344

NEW YORK

ALL AMERICAN (516) 981-3935
711-2 Koehier Ave. FAX: (516) 981-3947
Ronkonkoma, NY 11779

CAM/RPC (716) 436-5070
200 Buell Rd. FAX: (716) 436-5093
Rochester, NY 14624

JACO (516)-273-5500
145 Oser Avenue FAX: (516) 273-5506
Hauppauge, NY 11788

NORTH CAROLINA

JACO (919) 876-7767
5206 Greens Dairy Road FAX: (919) 876-6964
Raleigh, NC 27604

OHIO

CAM/RPC (216) 461-4700
749 Miner Road FAX: (216) 461-4329
Cleveland, OH 44143

CAM/RPC (614) 888-7777
733 H. Lakeview Plaza Rd. FAX: (614) 888-9779
Worthington, OH 43085

OREGON

I.E.C. (503) 641-1690
6850 S.W. 105th Ave. FAX: (503) 646-3737
Suite B
Beaverton, Oregon 97005

PENNSYLVANIA

CAM/RPC (412) 782-3770
620 Alpha Drive FAX: (412) 963-6210
Pittsburgh, PA 15238

TEXAS

ALL AMERICAN (214) 231-5300
1819 Firman Drive FAX: (214) 437-0353
Suite 127
Richardson, TX 75081

JACO (214) 234-5565
1209 N. Glenville Drive FAX: (214) 238-7066
Richardson, TX 75081

JACO (713) 240-2255
10707 Corporate Drive FAX: (713) 240-6988
Suite 124
Stafford, TX 77477

JACO (512) 835-0220
2120-A Braker Lane FAX: (512) 339-9252
Austin, TX 78758

UTAH

ADDED VALUE (801) 975-9500
1836 Parkway Blvd. FAX: (801) 977-0245
West Valley City, UT 84119

ALL AMERICAN (801) 261-4210
4455 South - 700 East FAX: (801) 261-3885
Suite 301
Salt Lake City, UT 84107

I.E.C. (801) 977-9750
2117 South 3600 West FAX: (802) 975-1207
W. Valley City, UT 84119

WASHINGTON

I.E.C. (206) 455-2727
1750 124th Avenue, N.E. FAX: (206) 453-2963
Bellevue, WA 98005

• • • • •

SAMSUNG

ELECTRONICS

HEAD OFFICE :

8/11FL., SAMSUNG MAIN BLDG.
250, 2-KA, TAEPYUNG-RO,
CHUNG-KU, SEOUL, KOREA
C.P.O. BOX 8780
TELEX : KORSST K27970
TEL : (02) 776-0114
FAX : (02) 753-0967

SEMICONDUCTOR BUSINESS SALES & MARKETING DIVISION :

16TH FL., SEVERANCE BLDG., 84-11,
5-KA, NAMDAEMOON-RO, CHUNG-KU,
SEOUL, KOREA
TEL : (02) 259-1114
FAX : (02) 259-2468

GUMI BRANCH :

259, GONGDAN-DONG, GUMI,
KYUNGSANGBUK-DO, KOREA
TELEX : SSTGUMI K54371
TEL : (0546) 463-2570
FAX : (0546) 461-9258

SAMSUNG SEMICONDUCTOR INC. :

3655 NORTH FIRST STREET
SAN JOSE, CA 95134, USA
TEL : (408) 954-7000
FAX : (408) 954-7286

SAMSUNG SEMICONDUCTOR EUROPE GMBH :

AM UNISYS PARK 1,
65843 SULZ-BACH, GERMANY
TEL : 49-6196-58206
FAX : 49-6196-750345

SAMSUNG ELECTRONICS JAPAN CO., LTD. :

HAMACHO CENTER BLDG.,
31-1, NIHONBASHI-HAMACHO 2-CHOME,
CHUO-KU, TOKYO 103, JAPAN
TEL : (03) 5641-9850
FAX : (03) 5641-9851

SAMSUNG ELECTRONICS HONGKONG CO., LTD. :

65TH FL., CENTRAL PLAZA,
18 HARBOUR ROAD,
WANCHAI, HONG KONG
TELEX : 80303 SSTC HX
TEL : 862-6900
FAX : 866-1343

SAMSUNG ELECTRONICS CO., LTD. TAIWAN BRANCH (KOREA) :

RM 2401, 24F., INT'L TRADE BLDG.,
333, KEE LUNG RD., SEC. 1,
TAIPEI, R.O.C
TEL : (2) 757-7292
FAX : (2) 757-7311

SAMSUNG ELECTRONICS SINGAPORE PTE LTD. :

4, SHENTON WAY, #18-01/10
SHINGKWAN HOUSE, SINGAPORE 0106
TEL : 535-2808
FAX : 227-2792

SAMSUNG ELECTRONICS CO., LTD. SHANGHAI OFFICE :

SUITE 4034,
SHERATON HUATING HOTEL,
1200 CAOXIBEILU, SHANGHAI
200030, CHINA
TEL : 021-4390707
FAX : 021-4393798

Printed in the Republic of Korea