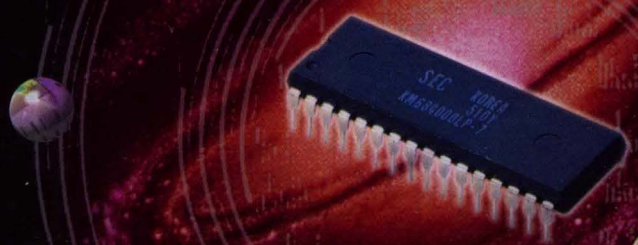
1120-7061
June 1997

1997

SRAM

DATA BOOK



SAMSUNG ELECTRONICS

CORRECTION TABLE

Page	Current	Correction
5	**TABLE OF CONTENTS** 22. KM68FV1000 ~ , 128x8, Commercial~, 195 23. KM68FS1000Z ~ , 128x8, 48-CSP~, 206	**TABLE OF CONTENTS** 22. KM68FV1000 ~ , **128Kx8**, Commercial~, 195 23. KM68FS1000Z ~ , **128Kx8**, 48-CSP~, 206
98	PIN DESCRIPTION Pin name of 44-TSOP(II) Forward and Reverse : 1.A4, 2.A3, ~ , 44.A5	PIN DESCRIPTION Changed Pin name of 44-TSOP(II)Forward and Reverse: 1.A4, 2.A3, 3.A2, 4.A1, 5.A0, 6.$\overline{CS}$, 7.I/O1, 8.I/O2, 9.I/O3, 10.I/O4, 11.Vcc, 12.Vss, 13.I/O5, 14.I/O6, 15.I/O7, 16.I/O8, 17.$\overline{WE}$, 18.A17, 19.A16, 20.A15, 21.A14, 22.A13, 23.A12, 24.A11, 25.A10, 26.A9, 27.A8, 8.N.C, 29.I/O19, 30.I/O10, 31.I/O11, 32.I/O12, 33.Vcc, 34.Vss, 35.I/O13, 36.I/O14, 37.I/O15, 38.I/O16, 39.$\overline{LB}$, 40.$\overline{UB}$, 41.$\overline{OE}$, 42.A7, 43.A6, 44.A5
130	**DC AND OPERATING CHARACTERISTICS** Standby Current, I_{SB}, Test conditions: $\overline{CS1}$=V_{IH}, CS2=V_{IH}	**DC AND OPERATING CHARACTERISTICS** Standby Current, I_{SB}, Test conditions: $\overline{CS1}$=V_{IH}, **CS2=V_{IL}**
255, 268	**TIMING WAVE FORM OF WRITE CYCLE(1)** ($\overline{OE}$=Controlled) tWP1(2)	**TIMING WAVE FORM OF WRITE CYCLE(1)** ($\overline{OE}$=Controlled) **tWP(2)**
255, 268	**TIMING WAVE FORM OF WRITE CYCLE(2)** ($\overline{OE}$=Low Fixed) tWP(2)	**TIMING WAVE FORM OF WRITE CYCLE(2)** ($\overline{OE}$=Low Fixed) **tWP1(2)**
283	**TIMING WAVE FORM OF WRITE CYCLE(1)** ($\overline{CS}$=Controlled) tWP1(2)	**TIMING WAVE FORM OF WRITE CYCLE(1)** ($\overline{CS}$=Controlled) **tWP(2)**
276, 284, 333, 384, 501, 518, 532, 548	**DATA RETENTION CHARACTERISTICS*** VCC =2.0V, $\overline{CS}$ •• VCC - 0.2V, ~	**DATA RETENTION CHARACTERISTICS*** VCC = **3.0V**, $\overline{CS}$ •• VCC - 0.2V, ~
363	**DC AND OPERATING CHARACTERISTICS** Standby Current, Test conditions: I_{SB} : Min. Cycle, $\overline{CS}$=V_{IH}	**DC AND OPERATING CHARACTERISTICS** Standby Current, **Test** conditions: I_{SB} : Min. Cycle, **$\overline{CS1}$=V_{IH} or CS2=V_{IL}**
	I_{SB1} : f=0MHz, $\overline{CS}$ •• Vcc-0.2V, VIN •• Vcc-0.2V or VIN •• 0.2V	I_{SB1} : f=0MHz, **$\overline{CS1}$ •• Vcc-0.2V or CS2 •• 0.2V**, V_{IN} •• Vcc-0.2V or V_{IN} •• 0.2V
308, 357, 402	" NOTE: Above test conditions are ~ " below TEST CONDITIONS	**Remove** "NOTE: Above test conditions are ~" below TEST CONDITIONS
411, 439, 467	Blank below **TEST CONDITIONS**	**Add** " NOTE: **Above test** conditions are also applied at industrial temperature range" below **TEST CONDITIONS**
411, 439, 467	Blank below **READ CYCLE**	**Add** " NOTE: **Above parameters** are also guaranteed at industrial temperature range" below **READ CYCLE**
412, 440, 468	Blank below **WRITE CYCLE**	**Add** " NOTE: **Above parameters** are also guaranteed at industrial temperature range" below **WRITE CYCLE**
932, 941, 950	**DC ELECTRICAL CHARACTERISTICS** Standby Current, I_{SB1}, Test conditions: f=Max, 100% Duty, Device **deselected**, ~	**DC ELECTRICAL CHARACTERISTICS** Standby Current, **I_{SB1}**, Test conditions: **f=0 MHz**, Device **deselected**, ~

If you want to get a revised specification, you **can see and download** the specification form **web site, www.sec.samsung.com/sram**, by pdf file.

SAMSUNG ELECTRONICS

Page	Current	Correction
903, 912, 921,	A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field), 256KB Module KMM764V41AG2,KMM764V41AG7, KMM764V45AG	Refer to below table

A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

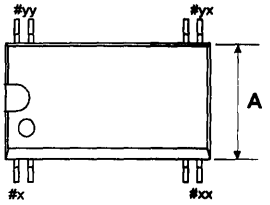
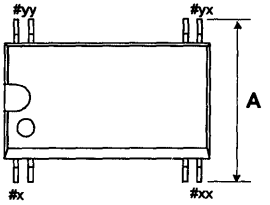
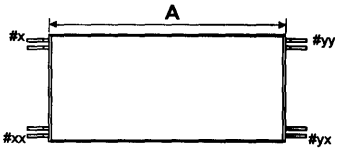
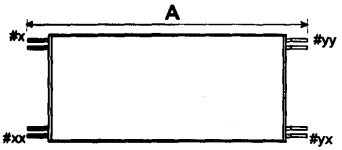
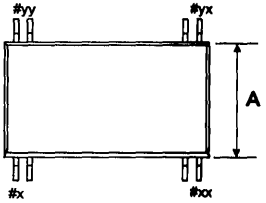
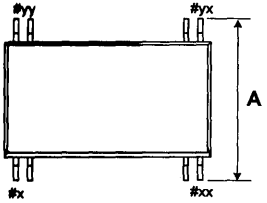
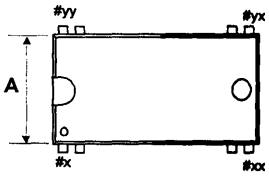
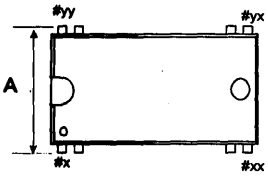
$\overline{CCS}$	$\overline{ECS}$	$\overline{ADSP}$	$\overline{CADS}$	$\overline{CADV}$	$\overline{WRITE}$	K	Address Accessed	Operation
H	X*	X	L	X	X	••	N/A	Not Selected
L	H	L	X	X	X	••	N/A	Not Selected
L	H	X	L	X	X	••	N/A	Not Selected
L	L	L	X	X	X	••	External Address	Begin Burst Read Cycle
L	L	H	L	X	L	••	External Address	Begin Burst Write Cycle
L	L	H	L	X	H	••	External Address	Begin Burst Read Cycle
X	X	H	H	L	H	••	Next Address	Continue Burst Read Cycle
H	X	X	H	L	H	••	Next Address	Continue Burst Read Cycle
X	X	H	H	L	L	••	Next Address	Continue Burst Write Cycle
H	X	X	H	L	L	••	Next Address	Continue Burst Write Cycle
X	X	H	H	H	H	••	Current Address	Suspend Burst Read Cycle
H	X	X	H	H	H	••	Current Address	Suspend Burst Read Cycle
X	X	H	H	H	L	••	Current Address	Suspend Burst Write Cycle
H	X	X	H	H	L	••	Current Address	Suspend Burst Write Cycle

Page	Current	Correction
930, 939, 948	A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field), 512KB Single Bank Module KMM764V72G2,KMM764V72G7, KMM764V75G	Refer to below table

A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

$\overline{CCS}$	$\overline{ADSP}$	$\overline{CADS}$	$\overline{CADV}$	$\overline{WRITE}$	K	Address Accessed	Operation
H	X	L	X	X	••	N/A	Not Selected
H	L	X	X	X	••	N/A	Not Selected
L	L	X	X	X	••	External Address	Begin Burst Read Cycle
L	H	L	X	L	••	External Address	Begin Burst Write Cycle
L	H	L	X	H	••	External Address	Begin Burst Read Cycle
X	H	H	L	H	••	Next Address	Continue Burst Read Cycle
H	X	H	L	H	••	Next Address	Continue Burst Read Cycle
X	H	H	L	L	••	Next Address	Continue Burst Write Cycle
H	X	H	L	L	••	Next Address	Continue Burst Write Cycle
X	H	H	H	H	••	Current Address	Suspend Burst Read Cycle
H	X	H	H	H	••	Current Address	Suspend Burst Read Cycle
X	H	H	H	L	••	Current Address	Suspend Burst Write Cycle
H	X	H	H	L	••	Current Address	Suspend Burst Write Cycle

If you want to get a revised specification, you can see and download the specification form web site,www.sec.samsung.com/sram, by pdf file.

Page	Current	Correction
	PACKAGE DIMENSIONS The arrow which indicate package width, is wrong.	**PACKAGE DIMENSIONS** See point "A" below drawing
961	XX-SOP-YYY 	XX-SOP-YYY 
962, 963, 964	XX-TSOP1-YYY.YY 	XX-TSOP1-YYY.YY 
966	XX-TSOP2-YYYY 	XX-TSOP2-YYYY 
969, 970, 971, 972, 973	XX-SOJ-YYY 	XX-SOJ-YYY 

If you want to get a revised specification, you can **see and** download the specification **form web site, www.sec.samsung.com/sram**, by pdf file.

Certified ISO 9001

Certificate No FM 24651

TABLE OF CONTENTS

I. FUNCTION GUIDE

II.SRAM DATA SHEET

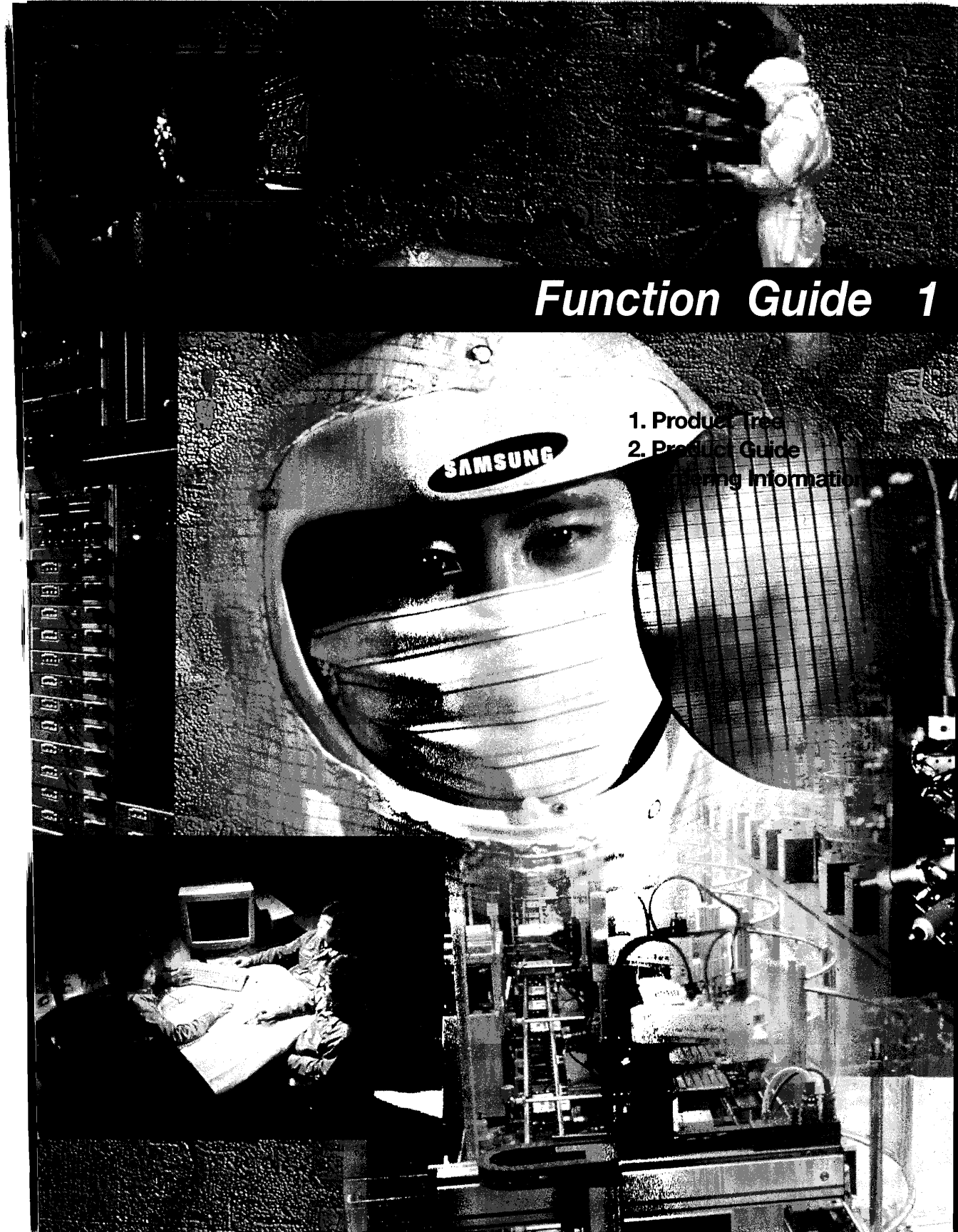
Low Power SRAM(5.0V Operation)

Low Power and Low Voltage SRAM(3.0V, 3.3V Operation)

Super Low Power and Low Voltage SRAM(Full CMOS)

Application Specification Memory for Mobile Communication

Synchronous SRAM Module

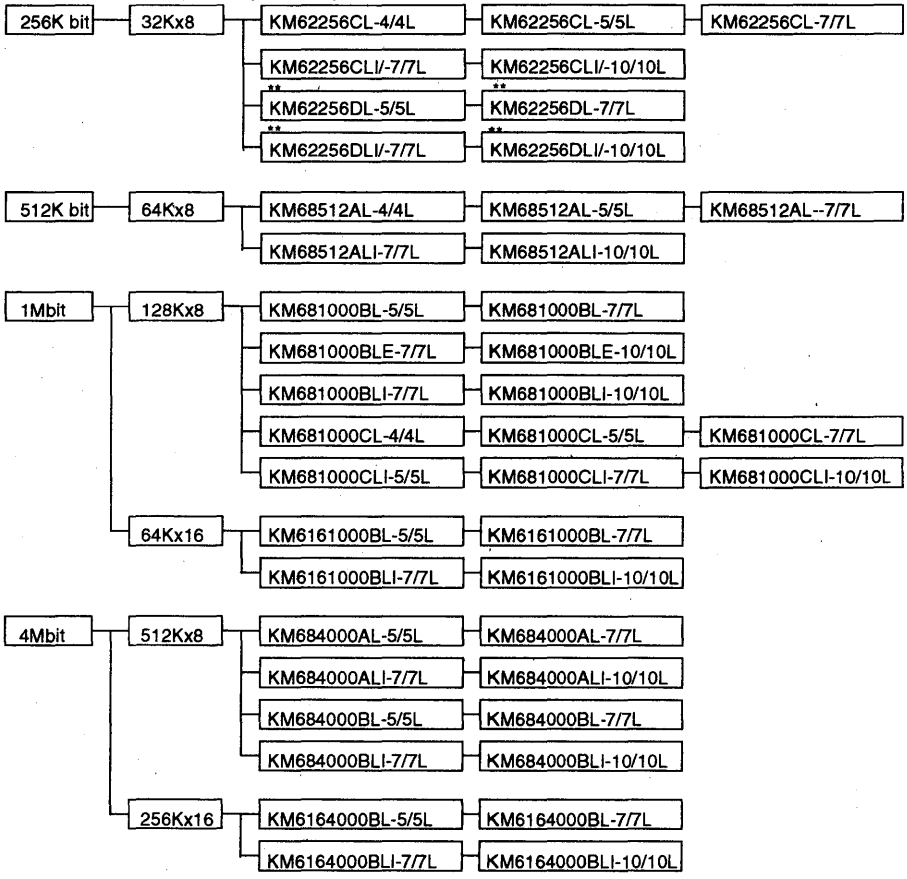


Function Guide 1

1. Product Tree
2. Product Guide
3. Ordering Information

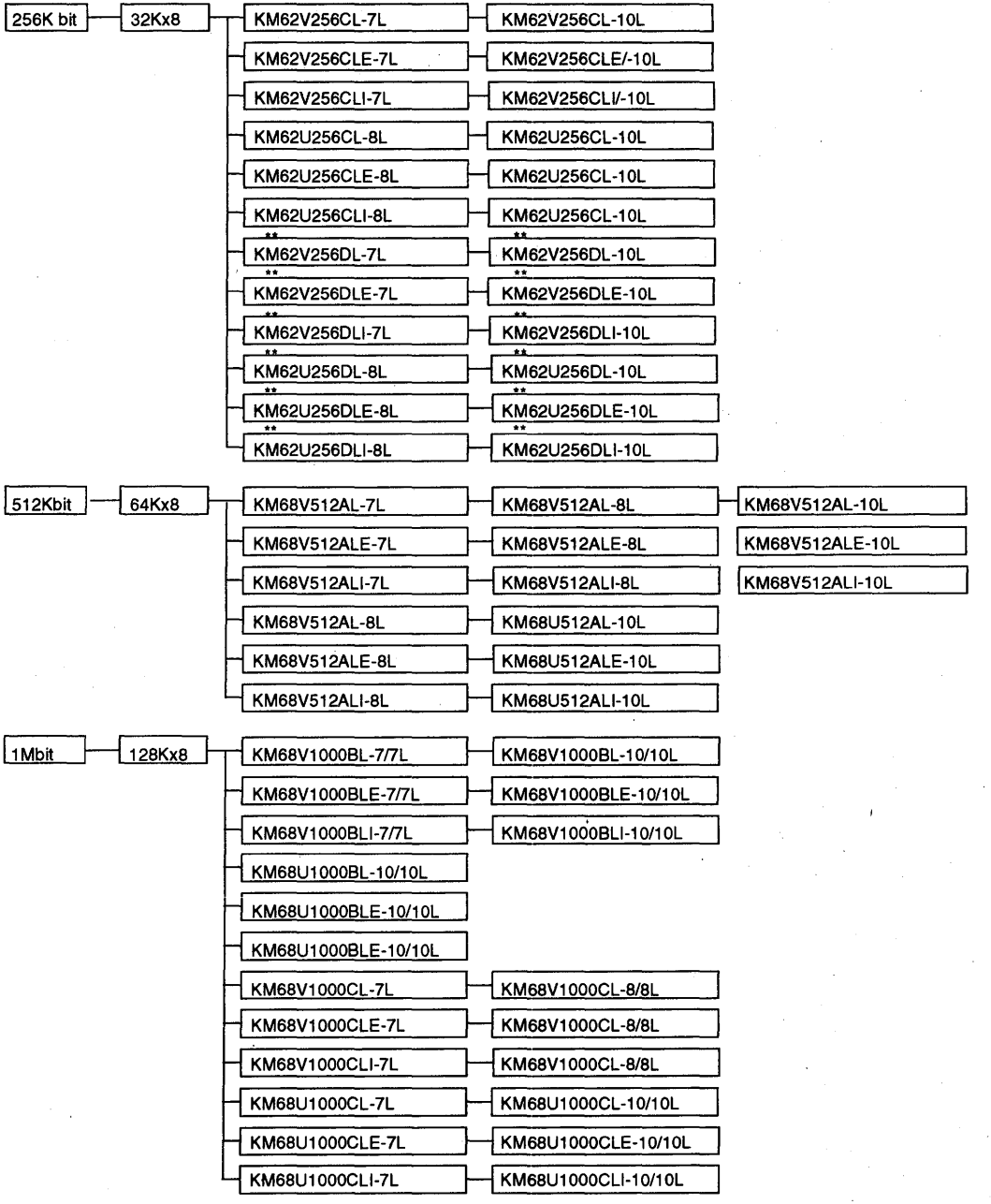
1. SRAM PRODUCT TREE

1.1.1. Low Power(5.0V Operation) SRAM



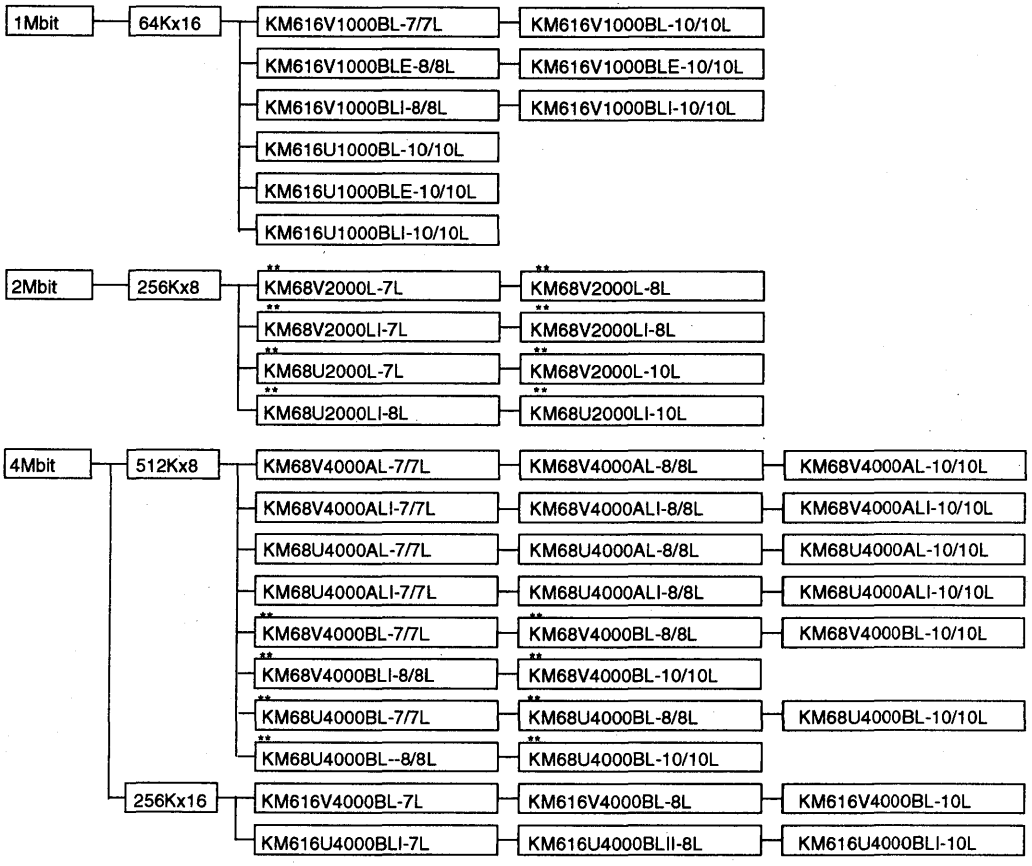
* : New Product ** : Preliminary *** : Under Development

1.1.2. Low Power and Low Voltage(3.0V, 3.3V Operation) SRAM



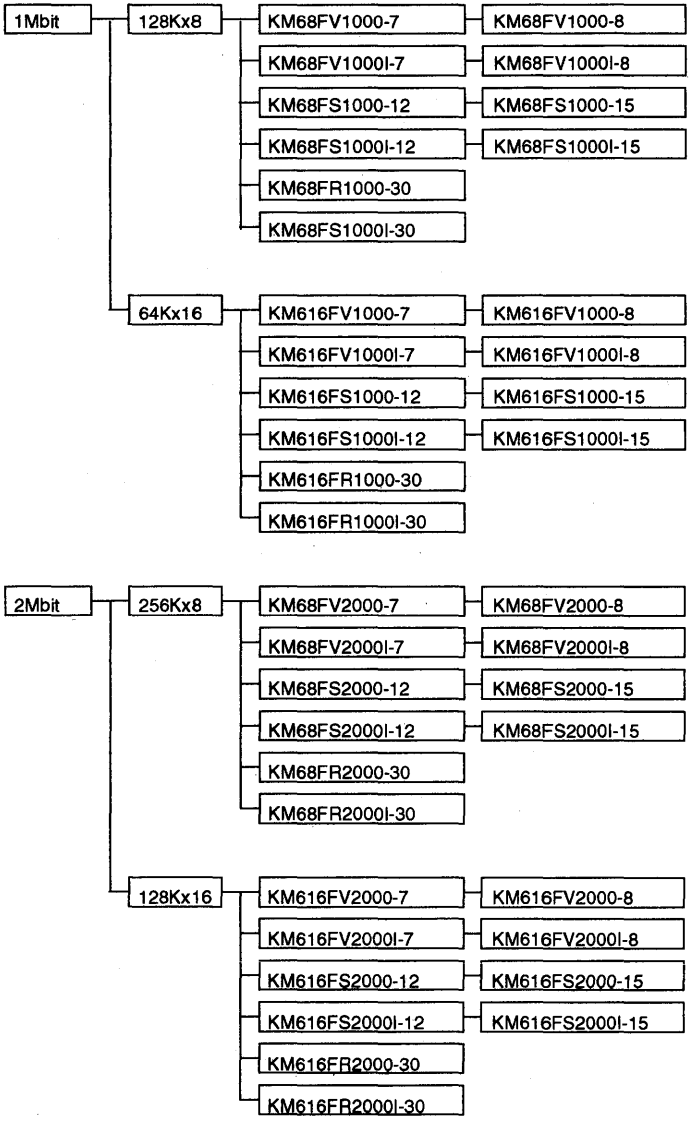
* : New Product ** : Preliminary *** : Under Development

1.1.2. Low Power and Low Voltage(3.0V, 3.3V Operation) SRAM



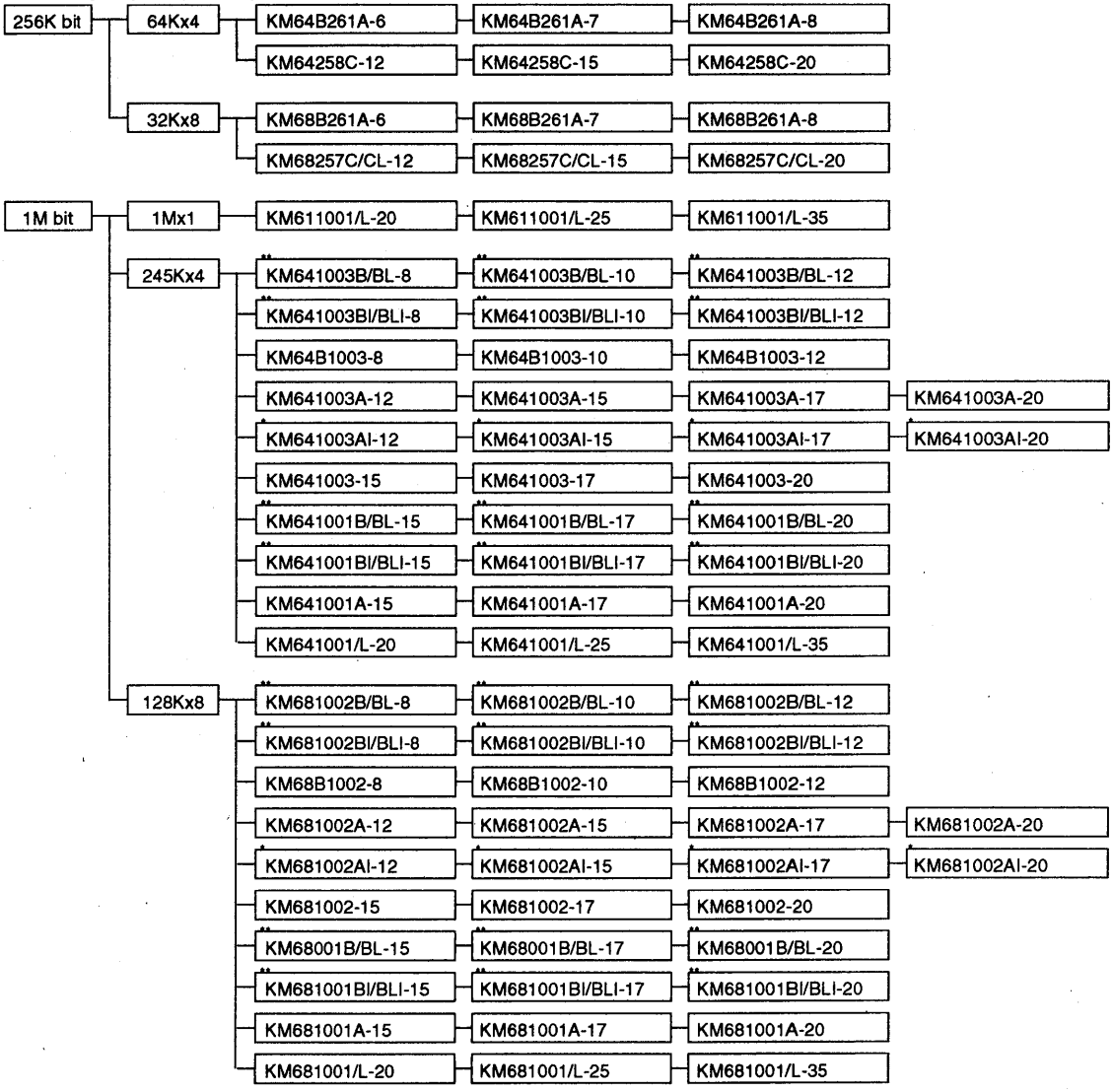
* : New Product ** : Preliminary *** : Under Development

1.1.3. Super Low Power and Low Voltage(Full CMOS) SRAM



* : New Product ** : Preliminary *** : Under Development

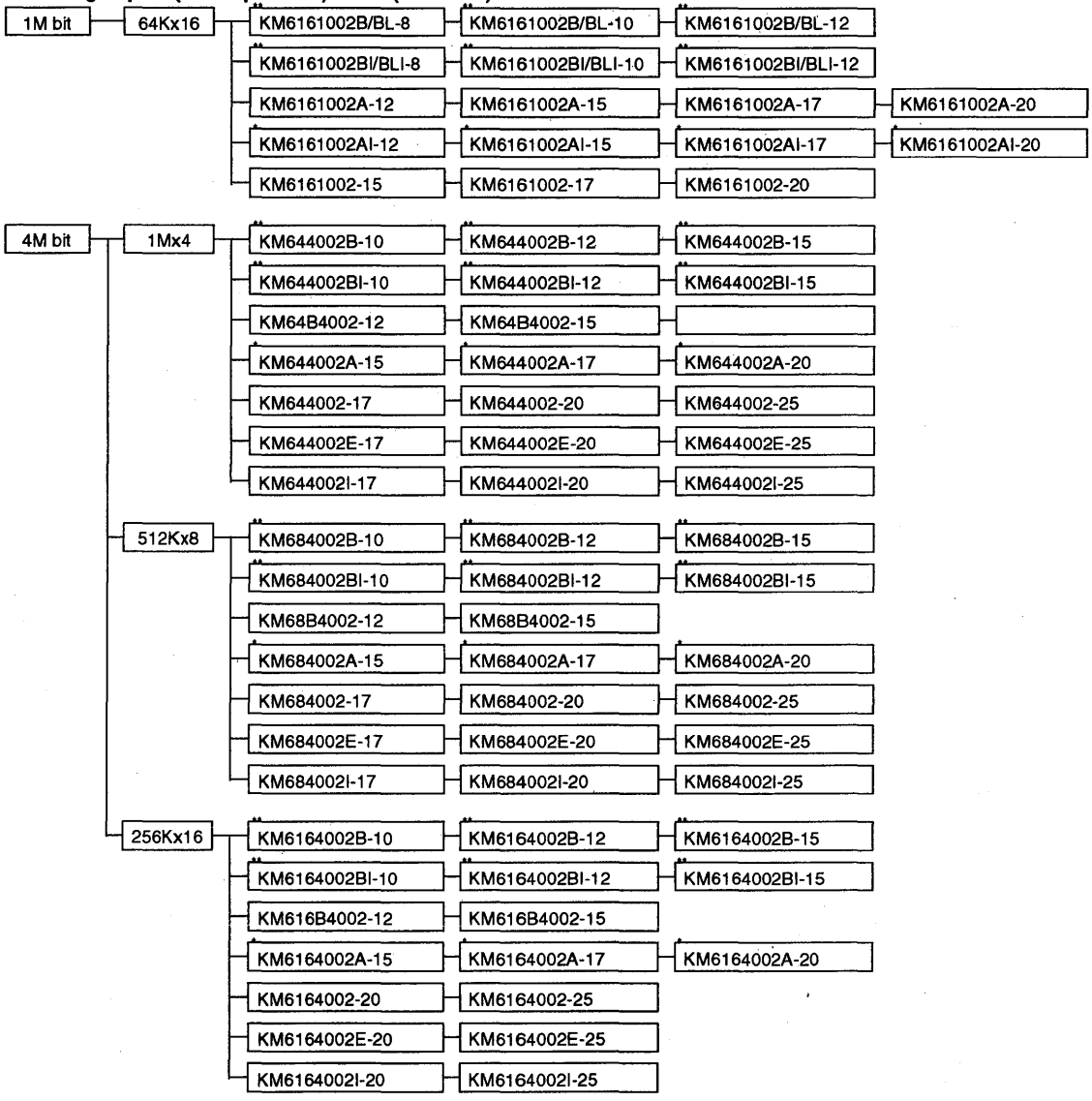
1.2.1. High Speed(5.0V Operation) SRAM



* : New Product ** : Preliminary *** : Under Development

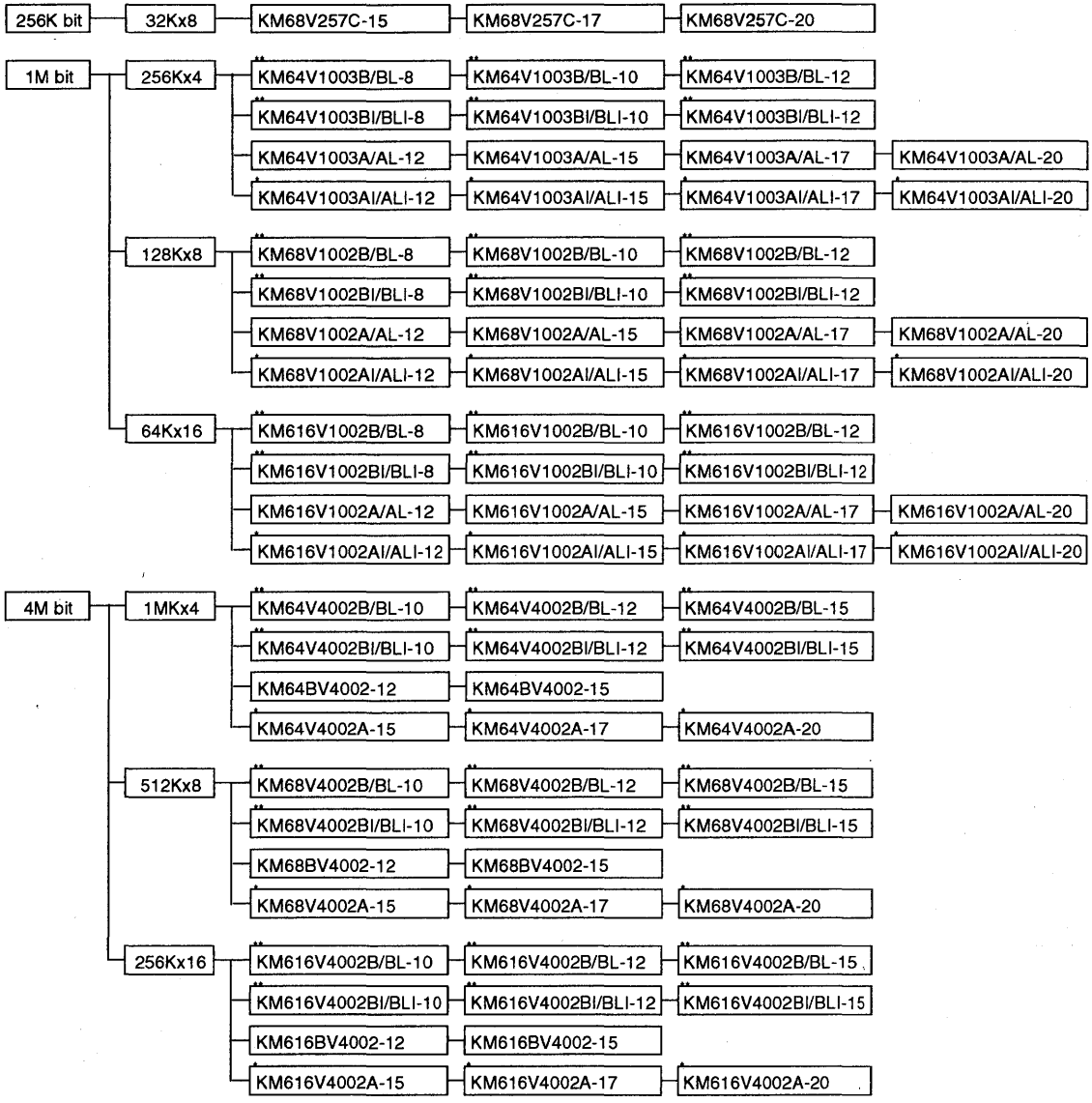
SAMSUNG ELECTRONICS

1.2.1. High Speed(5.0V Operation) SRAM(Continue)



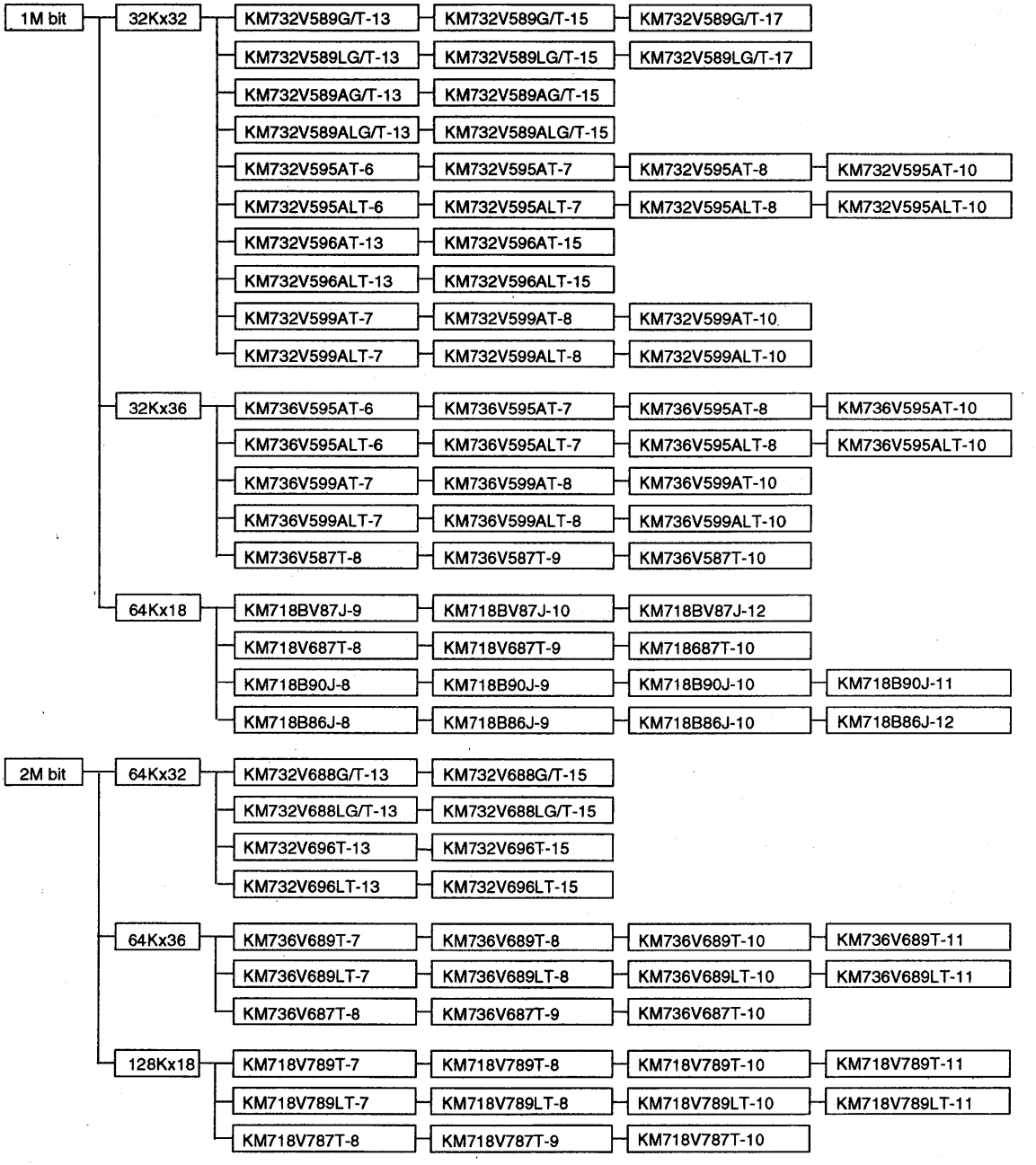
* : New Product ** : Preliminary *** : Under Development

1.2.2. High Speed(3.3V Operation) SRAM



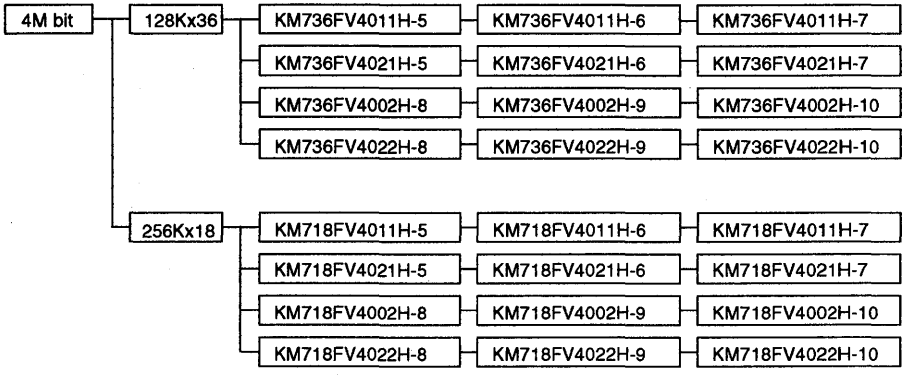
* : New Product ** : Preliminary *** : Under Development

1.3.1. Synchronous SRAM



* : New Product ** : Preliminary *** : Under Development

1.3.2. High Performance Synchronous SRAM



1

* : New Product ** : Preliminary *** : Under Development

2. SRAM FUNCTION GUIDE

2.1.1. Low Power(5.0V Operation) SRAM

Den.	Org.	Product No[Note1]	Op.Temp	Speed	Icc2/Isb1 (mA/μA)	Package
256K	32K x 8	KM62256CL KM62256CL-L	0~70℃	45/55/70	70/100 70/20	28-TSOP(I) Rew/Forward
		KM62256CLE KM62256CLE-L	-25~85℃	70/100	70/100 70/50	28-DIP
		KM62256CLI KM62256CLI-L	-40~85℃	70/100	70/100 70/50	28-SOP
		KM62256DL** KM62256DL-L**	0~70℃	55/70	70/50 70/10	28-TSOP(I) Rew/Forward
		KM62256DLI** KM62256DLI-L**	-40~85℃	70/100	70/50 70/15	28-DIP
512K	64K x 8	KM68512AL KM68512AL-L	0~70℃	45/55/70	70/100 70/20	32-TSOP(I) Forward
		KM68512ALI KM68512ALI-L	-40~85℃	70/100	70/100 70/50	32-SOP
1M	128K x 8	KM681000BL KM681000BL-L	0~70℃	55/70	70/100 70/20	
		KM681000BLE KM681000BLE-L	-25~85℃	70/100	70/100 70/50	32-TSOP(I) Rev/Forward
		KM681000BLI KM681000BLI-L	-40~85℃	70/100	70/100 70/50	32-DIP
		KM681000CL KM681000CL-L	0~70℃	45/55/70	90/50 90/10	32-SOP
		KM681000CLI KM681000CLI-L	-40~85℃	55/70/100	90/50 90/15	
	64K x 16	KM6161000BL KM6161000BL-L	0~70℃	55/70	120/100 120/20	44-TSOP(I) Rev/Forward
		KM6161000BLI KM6161000BLI-L	-40~85℃	70/100	120/100 120/50	
4M	512K x 8	KM684000AL KM684000AL-L	0~70℃	55/70	90/100 90/20	
		KM684000ALI KM684000ALI-L	-40~85℃	70/100	90/100 90/50	32-TSOP(II) Rev/Forward
		KM684000BL KM684000BL-L	0~70℃	55/70	90/100 90/20	32-SOP
		KM684000BLI KM684000BL-LI	-40~85℃	70/100	90/100 90/50	32-DIP
	256Kx16	KM6164000BL-L	0~70℃	55/70	130/20	44TSOP(II)
		KM6164000BLI-L	-40~85℃	70/100	130/50	

Note1. Refer to the ordering information for more detail description of each product.
* : New Product
** : Preliminary
*** : Under development

2.1.2. Low Power and Low Voltage(3.0V, 3.3V Operation) SRAM

Den.	Org. & Vcc	Product No note1	Op.Temp	Speed	Icc2/Isb1 (mA/μA)	Package
256K	32K x 8 (Vcc=3.0~3.6V)	KM62V256CL-L KM62V256CLE-L KM62V256CLI-L	0~70℃ -25~85℃ -40~85℃	70/100 70/100 70/100	35/10 35/20 35/20	28-TSOP(I) Reverse 28-TSOP(I) Forward 28-SOP
	32K x 8 (Vcc=2.7~3.3V)	KM62U256CL-L KM62U256CLE-L KM62U256CIL-L	0~70℃ -25~85℃ -40~85℃	85/100 85/100 85/100	35/10 35/15 35/15	
	32K x 8 (Vcc=3.0~3.6V)	KM62V256DL-L** KM62V256DLE-L** KM62V256DIL-L**	0~70℃ -25~85℃ -40~85℃	70/100 70/100 70/100	35/10 35/20 35/20	
	32K x 8 (Vcc=2.7~3.3V)	KM62U256DL-L** KM62U256DLE-L** KM62U256DIL-L**	0~70℃ -25~85℃ -40~85℃	85/100 85/100 85/100	35/10 35/15 35/15	
512K	64K x 8 (Vcc=3.0~3.6V)	KM68V512AL-L KM68V512ALE-L KM68V512ALI-L	0~70℃ -25~85℃ -40~85℃	70/85/100 70/85/100 70/85/100	40/10 40/20 40/20	32-TSOP(I) Forward 32-SOP
	64K x 8 (Vcc=2.7~3.3V)	KM68U512AL-L KM68U512ALE-L KM68U512ALI-L	0~70℃ -25~85℃ -40~85℃	85/100 85/100 85/100	45/10 45/15 45/15	
1M	128K x 8 (Vcc=3.0~3.6V)	KM68V1000BL KM68V1000BL-L KM68V1000BLE KM68V1000BLE-L KM68V1000BLI KM68V1000BLI-L	0~70℃ -25~85℃ -40~85℃	70/100 70/100 70/100 70/100 70/100 70/100	40/50 40/15 40/100 40/20 40/100 40/20	32-TSOP(I) Rev/Forward 32-SOP
		KM68V1000CL-L KM68V1000CLE-L KM68V1000CLI-L	0~70℃ -25~85℃ -40~85℃	70/85 70/85 70/85	40/10 40/20 40/20	32-TSOP(I) Rev/Forward 32-SOP
	128K x 8 (Vcc=2.7~3.3V)	KM68U1000BL KM68U1000BL-L KM68U1000BLE KM68U1000BLE-L KM68U1000BLI KM68U1000BLI-L	0~70℃ -25~85℃ -40~85℃	100 100 100 100 100 100	40/50 40/15 40/50 40/15 40/50 40/15	32-TSOP(I) Rev/Forward 32-SOP
	128K x 8 (Vcc=2.7~3.3V)	KM68U1000CL-L KM68U1000CLE-L KM68U1000CLI-L	0~70℃ -25~85℃ -40~85℃	70/100 70/100 70/100	40/10 40/20 40/20	32-TSOP(I) 32-sTSOP 32-SOP
	64K x 16 (Vcc=3.0~3.6V)	KM616V1000BL KM616V1000BL-L KM616V1000BLE KM616V1000BLE-L KM616V1000BLI KM616V1000BLI-L	0~70℃ -25~85℃ -40~85℃	70/100 70/100 85/100 85/100 85/100 85/100	65/50 65/15 65/100 65/20 65/100 65/20	44-TSOP(II) Reverse 44-TSOP(II) Forward
	64K x 16 (Vcc=2.7~3.3V)	KM616U1000BL KM616U1000BL-L KM616U1000BLE KM616U1000BLE-L KM616U1000BLI KM616U1000BLI-L	0~70℃ -25~85℃ -40~85℃	100 100 100 100 100 100	65/50 65/15 65/100 65/20 65/100 65/20	
2M	256K x 8 (Vcc=2.7~3.6V)	KM68V2000L-L** KM68V2000LI-L**	0~70℃ -40~85℃	70/85 85/100	40/15 40/30	32-TSOP(I) 32-sTSOP(I)
		KM68U2000L-L** KM68U2000LI-L**	0~70℃ -40~85℃	70/100 85/100	40/15 40/30	32-TSOP(I) 32-sTSOP(I)

2.1.2. Low Power and Low Voltage(3.0V, 3.3V Operation) SRAM(Continue)

Den.	Org. & Vcc	Product No note1	Op.Temp	Speed	Icc2/Isb1 (mA/μA)	Package
4M	512K x 8 (Vcc=3.0~3.6V)	KM68V4000AL KM68V4000AL-L KM68V4000ALI KM68V4000ALI-L	0~70℃ -40~85℃	70/85/100 70/85/100 70/85/100 70/85/100	50/50 50/15 50/50 50/20	32-TSOP(II) Rev/Forward 32-SOP
	512K x 8 (Vcc=2.7~3.3V)	KM68U4000AL KM68U4000AL-L KM68U4000ALI KM68U4000ALI-L	0~70℃ -40~85℃	70/85/100 70/85/100 70/85/100 70/85/100	50/30 50/10 50/30 50/15	32-SOP 32-TSOP(II)
	512K x 8 (Vcc=3.0~3.6V)	KM68V4000BL** KM68V4000BL-L** KM68V4000BLI** KM68V4000BLI-L**	0~70℃ -40~85℃	70/85/100 70/85/100 85/100 85/100	50/50 50/15 50/50 50/20	32-SOP 32-TSOP(II)
	512K x 8 (Vcc=2.7~3.3V)	KM68U4000BL** KM68U4000BL-L** KM68U4000BLI** KM68U4000BLI-L**	0~70℃ -40~85℃	70/85/100 70/85/100 85/100 85/100	50/30 50/15 50/30 50/20	32-SOP 32-TSOP(II)
	256K x 16 (Vcc=3.0~3.6V)	KM616V4000BL-L KM616V4000BLI-L	0~70℃ -40~85℃	70/85/100 70/85/100	70/15 70/20	44-TSOP(II)

Note1. Refer to the ordering information for more detail description of each product.
* : New Product
** : Preliminary
*** : Under development

2.1.3. Super Low Power and Low Voltage(Full CMOS) SRAM

Den.	Org.	Product No[Note1]	Op.Temp	Speed	Icc2/Isb1 (mA/μA)	Package
1M	128K x 8	KM68FV1000	0~70℃	70/85	55/5	32-TSOP(I) Forward/Reverse 32-sTSOP(I) Forward/Reverse 32-SOP
		KM68FV1000I	-40~85℃	70/85	55/5	
		KM68FS1000	0~70℃	120/150 70/85	30/5 50/5	
		KM68FS1000I	-40~85℃	120/150 70/85	30/5 50/5	
		KM68FR1000	0~70℃	300	15/5	
		KM68FR1000I	-40~85℃	300	15/5	
	64Kx16	KM616FV1000	0~70℃	70/85	80/5	44-TSOP(II) Forward/Reverse
		KM616FV1000I	-40~85℃	70/85	80/5	
		KM616FS1000	0~70℃	120/150 70/85	50/5 80/5	
		KM616FS1000I	-40~85℃	120/150 70/85	50/5 80/5	
		KM616FR1000	0~70℃	300	20/5	
		KM616FR1000I	-40~85℃	300	20/5	
2M	256K x 8	KM68FV2000	0~70℃	70/85	60/10	32-TSOP(I) Forward/Reverse 32-sTSOP(I) Forward/Reverse 32-SOP
		KM68FV2000I	-40~85℃	70/85	60/10	
		KM68FS2000	0~70℃	120/150 70/85	30/10 55/10	
		KM68FS2000I	-40~85℃	120/150 70/85	30/10 55/10	
		KM68FR2000	0~70℃	300	15/10	
		KM68FR2000I	-40~85℃	300	15/10	
	128Kx16	KM616FV2000	0~70℃	70/85	80/10	44-TSOP(II) Forward/Reverse
		KM616FV2000I	-40~85℃	70/85	80/10	
		KM616FS2000	0~70℃	120/150 70/85	50/10 80/10	
		KM616FS2000I	-40~85℃	120/150 70/85	50/10 80/10	
		KM616FR2000	0~70℃	300	20/10	
		KM616FR2000I	-40~85℃	300	20/10	

Note1. Refer to the ordering information for more detail description of each product.
* : New Product
** : Preliminary
*** : Under development

2.2.1. High Speed SRAM(5V Operation)

Den.	Org.	Product No[Note1]	Speed(ns)	Tech.	Power Dissipation		Package
					Active Max(mA)	Standby Max(mA)	
256K	64K x 4	KM64B261A	6/7/8	BiCMOS	160	20	28SOJ
		KM64258C	12/15/20	CMOS	160	2	28DIP/SOJ
	32K x 8	KM68B261A	6/7/8	BiCMOS	170	20	32SOJ
		KM68257C/CL	12/15/20	CMOS	165	2/0.1	28DIP/SOJ/TSOP1F
1M	1M x 1	KM611001/L	20/25/35	CMOS	130	2/0.5	28DIP/SOJ
	256K x 4	KM641003B/BL/BI/BLI**	8/10/12	CMOS	150	10/1	32SOJ/TSOP2F
		KM64B1003	8/10/12	BiCMOS	165	10	32SOJ
		KM641003A	12/15/17/20	CMOS	150	8	32SOJ/TSOP2F
		KM641003	15/17/20	CMOS	170	10	32SOJ
		KM641001B/BL/BI/BLI**	15/17/20	CMOS	120	5/0.5	28SOJ
		KM641001A	15/17/20	CMOS	125	8	28SOJ
		KM641001/L	20/25/35	CMOS	150	2/0.5	28DIP/SOJ
	128K x 8	KM681002B/BL/BI/BLI**	8/10/12	CMOS	160	10/1	32SOJ(300/400)/TSOP2F
		KM68B1002	8/10/12	BiCMOS	170	10	32SOJ
		KM681002A	12/15/17/20	CMOS	170	8	32SOJ(300/400)/TSOP2F
		KM681002	15/17/20	CMOS	170	10	32SOJ
		KM681001B/BL/BI/BLI**	15/17/20	CMOS	130	5/0.5	32SOJ(300/400)
		KM681001A	15/17/20	CMOS	125	8	32SOJ(300/400)
		KM681001/L	20/25/35	CMOS	170	2/0.5	32DIP/SOJ
	64K x 16	KM6161002B/BL/BI/BLI**	8/10/12	CMOS	200	10/1	44SOJ/TSOP2F
		KM6161002A	12/15/17/20	CMOS	190	8	44SOJ/TSOP2F
		KM6161002	15/17/20	CMOS	230	10	44SOJ
4M	1M x 4	KM644002B/BI**	10/12/15	CMOS	190	10	32SOJ/TSOP2F
		KM64B4002	12/15	BiCMOS	185	30	32SOJ
		KM644002A*	15/17/20	CMOS	150	10	32SOJ
		KM644002	17/20/25	CMOS	170	10	32SOJ
	512K x 8	KM684002B/BI**	10/12/15	CMOS	200	10	36SOJ/TSOP2F
		KM68B4002	12/15	BiCMOS	195	30	36SOJ
		KM684002A*	15/17/20	CMOS	170	10	36SOJ
		KM684002	17/20/25	CMOS	180	10	36SOJ
	256K x 16	KM6164002B/BI**	10/12/15	CMOS	250	10	44SOJ/TSOP2F
		KM616B4002	12/15	BiCMOS	270	30	44SOJ
		KM6164002A*	15/17/20	CMOS	210	10	44SOJ
		KM6164002	20/25/35	CMOS	240	10	44SOJ

* : New product
** : Preliminary
*** : Under development

2.2.2. High Speed SRAM(3.3V Operation)

Den.	Org.	Product No[Note1]	Speed(ns)	Tech.	Power Dissipation		Package
					Active Max(mA)	Standby Max(mA)	
256K	32K x 8	KM68V257C	15/17/20	CMOS	90	0.1	28DIP/SOJ/TSOP1F
1M	256K x 4	KM64V1003B/BL/BI/BLI** KM64V1003A/AL/AI/ALI	8/10/12 12/15/17/20	CMOS CMOS	150 130	5/0.5 5/0.5	32SOJ/TSOP2F 32SOJ/TSOP2F
	128K x 8	KM68V1002B/BL/BI/BLI** KM68V1002A/AL/AI/ALI	8/10/12 12/15/17/20	CMOS CMOS	160 140	5/0.5 5/0.5	32SOJ(300/400)/TSOP2F 32SOJ(300/400)/TSOP2F
	64K x 16	KM616V1002B/BL/BI/BLI** KM616V1002A/AL/AI/ALI	8/10/12 12/15/17/20	CMOS CMOS	200 170	5/0.5 5/0.5	44SOJ/TSOP2F 44SOJ/TSOP2F
4M	1M x 4	KM64V4002B/BL/BI/BLI** KM64BV4002 KM64V4002A*	10/12/15 12/15 15/17/20	CMOS BiCMOS CMOS	160 160 140	10/1 30 10	32SOJ/TSOP2F 32SOJ 32SOJ
	512K x 8	KM68V4002B/BL/BI/BLI** KM68BV4002 KM68V4002A*	10/12/15 12/15 15/17/20	CMOS BiCMOS CMOS	170 170 160	10/1 30 10	36SOJ/TSOP2F 36SOJ 36SOJ
	256K x 16	KM616V4002B/BL/BI/BLI** KM616BV4002 KM616V4002A*	10/12/15 12/15 15/17/20	CMOS BiCMOS CMOS	240 240 200	10/1 30 10	44SOJ/TSOP2F 44SOJ 44SOJ

* : New product
** : Preliminary
*** : Under development

2.3.1. Specialty SRAM

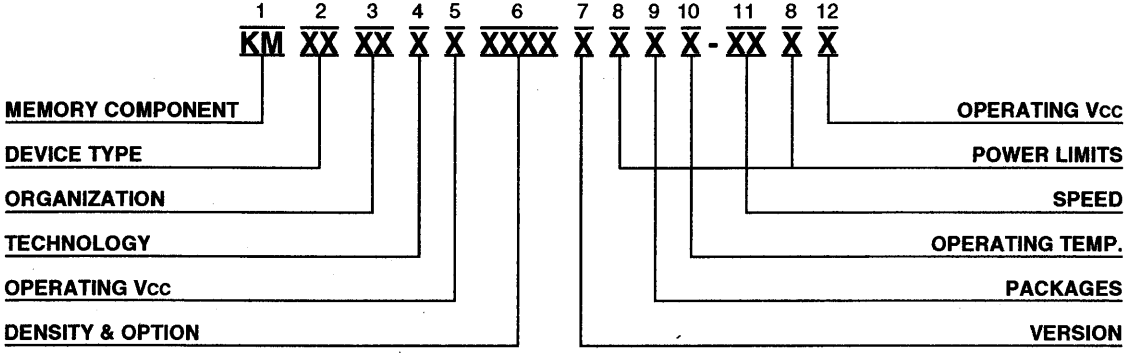
Den.	Org. & Vcc	Product No*	Mode	Op.Temp	I/O	tCYC	tCD	Package
1M	32Kx32, 3.3V	KM732V589	SPB	CMOS	3.3V	13/15	7/8	(T)QFP
		KM732V589A	SPB	CMOS	3.3V	13/15	7/8	(T)QFP
		KM732V595A	SPB	CMOS	2.5V	6.6/7.5/8.6/10	4.4/5/5/5.5	TQFP
		KM732V596A	SPB	CMOS	2.5V/3.3V	13/15	7/8	TQFP
		KM732V599A	SPB	CMOS	3.3V	7.5/8.6/10	4.5/5/5	TQFP
	32Kx36, 3.3V	KM736V595A	SPB	CMOS	2.5V	6.6/7.5/8.6/10	4.4/5/5/5.5	TQFP
		KM736V599A	SPB	CMOS	3.3V	7.5/8.6/10	4.5/5/5	TQFP
		KM736V587	SB	CMOS	3.3V	12/15/17	8.5/9/10	TQFP
	64Kx18, 3.3V	KM718BV87	SB	BiCMOS	3.3V	12/15/17	8.5/9/10	52PLCC
		KM718V687	SB	CMOS	3.3V	12/15/17	8.5/9/10	TQFP
	64Kx18, 5V	KM718B90	SB	BiCMOS	5.0V	11/15/17/20	8/9/10/12	52PLCC
		KM718B86	SB	BiCMOS	5.0V	12/15/17/20	8/9/10/12	52PLCC
2M	64Kx32, 3.3V	KM732V688	SPB	CMOS	3.3V	13/15	7/8	(T)QFP
		KM732V696	SPB	CMOS	2.5V/3.3V	13/15	7/8	TQFP
	64Kx36, 3.3V	KM736V689	SPB	CMOS	3.3V	7.5/8.6/10	4.5/5/5	TQFP
		KM736V687	SB	CMOS	3.3V	12/15/17	8.5/9/10	TQFP
	128Kx18, 3.3V	KM718V789	SPB	CMOS	3.3V	7.5/8.6/10	4.5/5/5	TQFP
		KM718V787	SB	CMOS	3.3V	12/15/17	8.5/9/10	TQFP
4M	128Kx36, 3.3V	KM736FV4011	SP	CMOS	1.5V	5/6/7	2.5/3.0/3.5	119BGA
		KM736FV4021	SP	CMOS	3.3V	5/6/7	2.5/3.0/3.5	119BGA
		KM736FV4002	RL	CMOS	2.5V	8/9/10	7/8/9	119BGA
		KM736FV4022	RL	CMOS	3.3V	8/9/10	7/8/9	119BGA
	256Kx18, 3.3V	KM718FV4011	SP	CMOS	1.5V	5/6/7	2.5/3.0/3.5	119BGA
		KM718FV4021	SP	CMOS	3.3V	5/6/7	2.5/3.0/3.5	119BGA
		KM718FV4002	RL	CMOS	2.5V	8/9/10	7/8/9	119BGA
		KM718FV4022	RL	CMOS	3.3V	8/9/10	7/8/9	119BGA

* : New product
** : Preliminary
*** : Under development

- SPB : Synchronous pipelined burst
- SB : Synchronous burst
- RL : Register to Latch

3. ORDERING INFORMATION

3.1.1. Asynchronous SRAM



1. MEMORY COMPONENT

2. DEVICE TYPE

- . 6 ---------- Asynch. SRAM
- . 7 ---------- Synch. SRAM

3. ORGANIZATION

- . 1 ---------- x1 bit
- . 4 ---------- x4 bit
- . 2 or 8 ---------- x8 bit
- . 9 ---------- x9 bit
- . 16 ---------- x16 bit
- . 32 ---------- x32 bit

4. TECHNOLOGY

- . BLANK ---------- CMOS
- . B ---------- BiCMOS
- . F ---------- Full CMOS

5. OPERATING Vcc

- . BLANK ---------- 5.0V
- . V ---------- 3.3V
- . U ---------- 3.0V
- . S ---------- 2.5V
- . T ---------- 2.0V

6. DENSITY & OPTION

- . 64 ---------- 64:64K Slow
- . 256 ---------- 256:256K Slow
- . 257 ---------- 257:257K Fast
- . 258 ---------- 258:256K Fast(with $\overline{OE}$)
- . 512 ---------- 512:512K Slow
- . 1000 ---------- 1000:1M Slow
- . 1001 ---------- 1001:1M Fast
- . 1002 ---------- 1002:1M Fast(Revolutionary)
- . 1003 ---------- 1003:1M Fast(Revolutionary, with $\overline{OE}$)
- . 2000 ---------- 2000: 2M Slow
- . 4000 ---------- 4000:4M Slow
- . 4002 ---------- 4002:4M Fast(Revolutionary)

7. VERSION

- . BLANK ---------- First Gen.
- . A ---------- Second Gen.
- . B ---------- Third Gen.
- . C ---------- Forth Gen.

8. POWER LIMITS

- . BLANK ---------- High Power(Fast) In Full CMOS Low Power SRAM(Slow)
- . L ---------- Low Power
- . L-L ---------- Low Low Power

9. PACKAGES

- . P ---------- DIP
- . G ---------- SOJ
- . J ---------- SOJ or PLCC
- . T ---------- TSOP(Standard)
- . R ---------- TSOP(Standard)

10. OPERATING TEMP.

- . BLANK ---------- Commercial
- . E ---------- Extended
- . I ---------- Industrial

11. SPEED

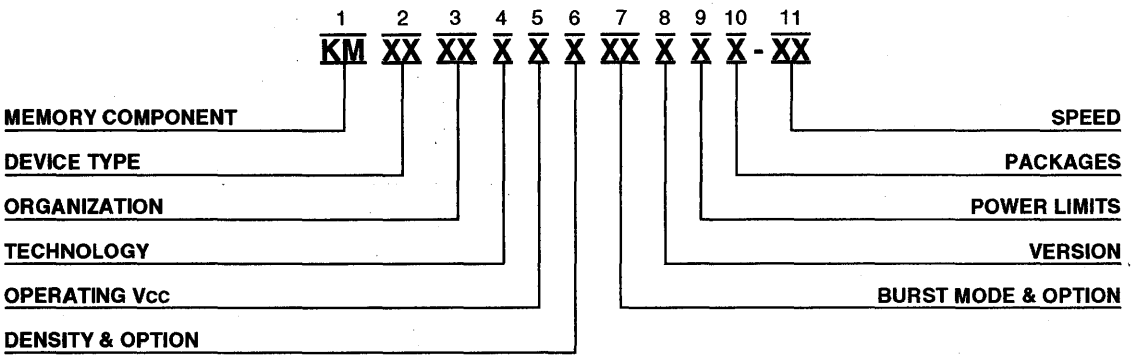
SLOW SRAM

- . 4 ---------- 45ns
- . 5 ---------- 55ns
- . 7 ---------- 70ns
- . 8 ---------- 85ns
- . 10 ---------- 100ns
- . 12 ---------- 120ns
- . 15 ---------- 150ns

FAST SRAM

- . 6 ---------- 6ns
- . 7 ---------- 7ns
- . 8 ---------- 8ns
- . 10 ---------- 10ns
- . 12 ---------- 12ns
- . 15 ---------- 15ns
- . 17 ---------- 17ns
- . 20 ---------- 20ns
- . 25 ---------- 25ns
- . 30 ---------- 30ns

3.2.1. Synchronous Burst SRAM



1. MEMORY COMPONENT

2. DEVICE TYPE

. 6	Asynch. SRAM
. 7	Synch. SRAM

3. ORGANIZATION

. 16	x16 bit
. 18	x18 bit
. 32	x32 bit
. 36	x36 bit
. 64	x64 bit

4. TECHNOLOGY

. BLANK	CMOS or AMOS
. B	BiCMOS

5. OPERATING Vcc

. BLANK	5.0V
. V	3.3V

6. DENSITY & OPTION

. BLANK	32Kx9 or 64Kx18
. 5	32K Depth
. 6	64K Depth
. 7	128K Depth

7. BURST MODE & OPTION

. 86	Binary Count
. 87	Binary Count, Guid Logic
. 88	Binary Count, Pipe Line
. 89	GW, BW, Mode, FT and ZZ
. 90	Linear Count
. 91	Linear Count, Glue Logic
. 92	Linear Count, Pipe Line
. 95	GW, BW, Mode, FT and ZZ

8. VERSION

. BLANK	First Gen.
. A	Second Gen.
. B	Third Gen.
. C	Forth Gen.

9. POWER LIMITS

. BLANK	High Power.
. L	Low Power

10. PACKAGES

. H	BGA
. T	TSOP/TQFP
. J	PLCC
. G	QFP

11. SPEED

Sync Bust(CLOCK ACCESS TIME)

. 8	8ns
. 9	9ns
. 10	10ns
. 12	12ns
. 15	15ns
. 20	20ns

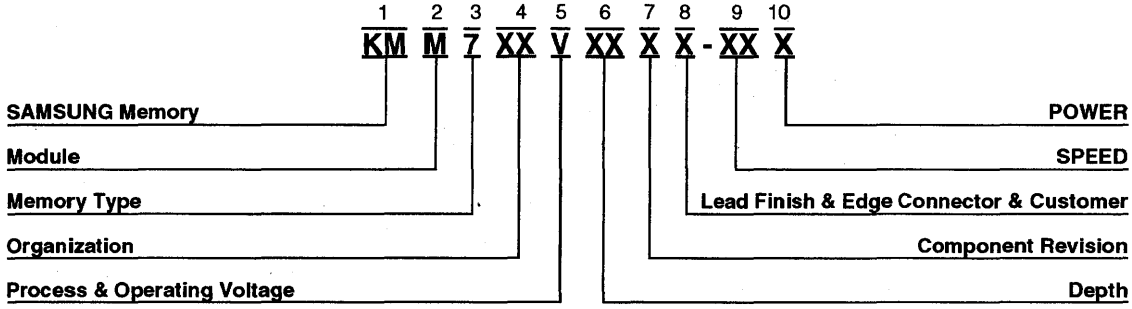
Sync Pipe & Burst(CLOCK CYCLE TIME)

. 7	133MHz
. 8	166MHz
. 10	100MHz
. 13	75MHz
. 15	66MHz
. 17	60MHz
. 20	50MHz

KM732V589(Pipelined/Non-Pipelined)

. 10	100MHz, 6ns/40MHz, 17ns
. 15	66MHz, 8ns/40MHz, 17ns
. 20	66MHz, 8ns/50MHz, 15ns
. 25	60MHz, 9ns/40MHz, 17ns

3.2.2. Synchronous Burst SRAM Module



1. SAMSUNG Memory

2. Module

3. Memory Type
- 1 : FLASH
- 2 : Mask ROM
- 3 : DRAM DIMM
- 4 : DRAM SIP
- 5 : DRAM SIMM
- 6 : Async SRAM
- 7 : Sync SRAM
- 8 : M-ROM and SRAM
- 9 : VRAM

4. Organization
- 8 : x8 bit
- 9 : x9 bit
- 16 : x16 bit
- 18 : x18 bit
- 32 : x32 bit
- 44 : x44 bit
- 64 : x64 bit
- 72 : x72 bit

5. Process & Operating Voltage
- Blank : CMOS 5V
- V : CMOS 3.3V
- B : BiCMOS 5V

6. Depth
- 32, 33, 34, 35, 36 .... : 32K
- 64, 65, 66, 67, 68 .... : 64K
- 128, 129, 130, 131 .... : 128K
- 512, 513, 514, 515 .... : 512K
- 544, 545, 546 .... : 544K

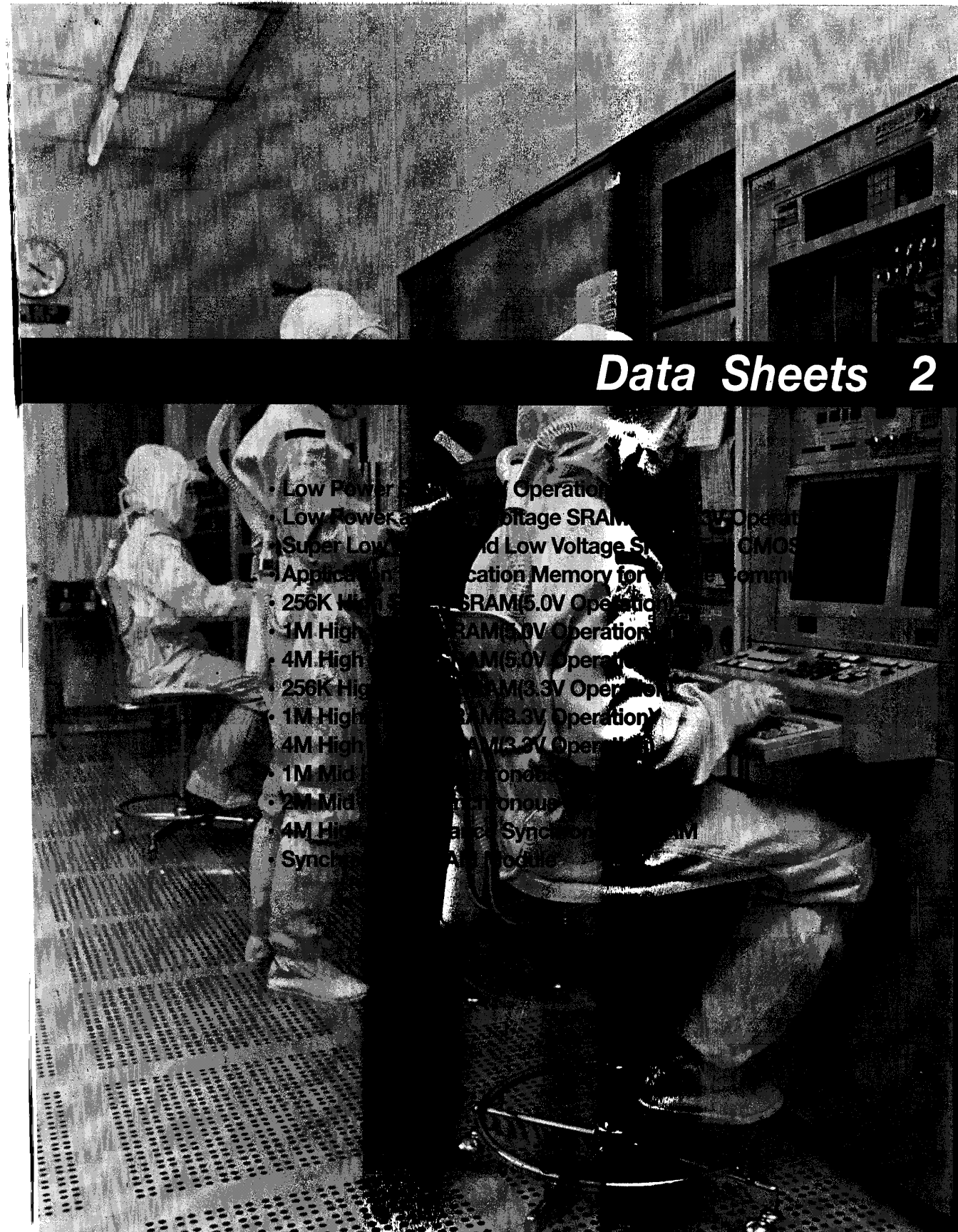
7. Component Revision
- Blank : First Gen.
- A : Second Gen
- B : Third Gen

8. Lead Finish & Edge Connector & Customer
- Blank : Solder DIMM
- G : Gold DIMM

9. Speed
- 10 : 10, 100ns
- 12 : 12, 120ns
- 13 : 13ns
- 15 : 15ns
- 17 : 17ns
- 20 : 20ns
- 25 : 25ns
- 30 : 30ns
- 35 : 135ns
- 55 : 55ns
- 70 : 70ns
- 80 : 80ns
- 90 : 90ns

10. Power Dissipation.
- Blank : Nomal Power
- L : Low Power

NOTES



Data Sheets 2

- Low Power
- Low Power
- Super Low
- Applica
- 256K
- 1M High
- 4M High
- 256K Hig
- 1M High
- 4M High
- 1M Mid
- 2M Mid
- 4M Hig
- Synch

Operation
oltage SRA
d Low Voltage S
cation Memory for
SRAM(5.0V Operation)
RAM(5.0V Operation)
M(5.0V Operat
M(3.3V Oper
M(3.3V Operation)
M(3.3V Oper
ronou
ronou
Sync
odule

Low Power SRAM(5.0V Operation)

32Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.7㎛ CMOS
- Organization : 32Kx8
- Power Supply Voltage : Single 5V ± 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  28-DIP, 28-SOP, 28-TSOP I -Forward/Reverse

GENERAL DESCRIPTION

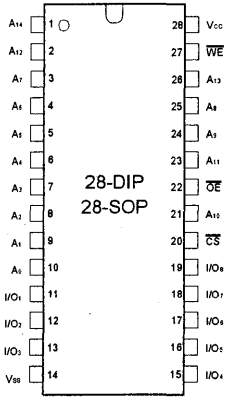
The KM62256C family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

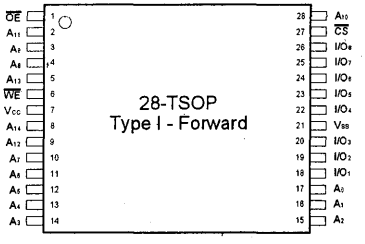
PRODUCT FAMILY

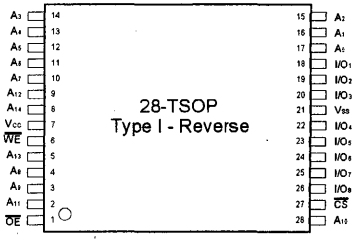
Product Family	Operating Temperature.	Speed (ns)	PKG Type	Power Dissipation	
				Standby (I_{SB1}, Max)	Operating (I_{CC2})
KM62256CL KM62256CL-L	Commercial (0~70℃)	45*/55/70ns	28-DIP, 28-SOP 28-TSOP I R/F	100㎂ 20㎂	70mA
KM62256CLE KM62256CLE-L	Extended (-25~85℃)	70/100ns	28-SOP 28-TSOP I R/F	100㎂ 50㎂	
KM62256CLI KM62256CLI-L	Industrial (-40~85℃)	70/100ns	28-SOP 28-TSOP I R/F	100㎂ 50㎂	

* The parameter is measured with 30pF test load.

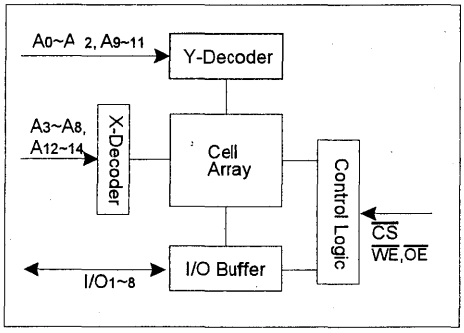
PIN DESCRIPTION







FUNCTIONAL BLOCK DIAGRAM



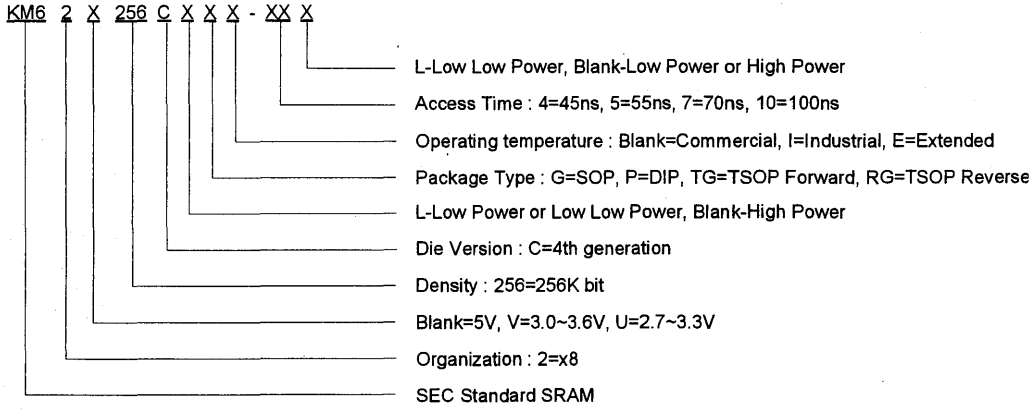
NameName	Function
A0~A14	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power(5V)
Vss	Ground

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Extended Temp Products (-25~85℃)		Industrial Temp Products (-40~85℃)	
Part Name	Function	Part Name	Function	Part Name	Function
KM62256CLP-4	28-DIP, 45ns, L-pwr	KM62256CLGE-7	28-SOP, 70ns, L-pwr	KM62256CLGI-7	28-SOP, 70ns, L-pwr
KM62256CLP-4L	28-DIP, 45ns, LL-pwr	KM62256CLGE-7L	28-SOP, 70ns, LL-pwr	KM62256CLGI-7L	28-SOP, 70ns, LL-pwr
KM62256CLP-5	28-DIP, 55ns, L-pwr	KM62256CLGE-10	28-SOP, 100ns, L-pwr	KM62256CLGI-10	28-SOP, 100ns, L-pwr
KM62256CLP-5L	28-DIP, 55ns, LL-pwr	KM62256CLGE-10L	28-SOP, 100ns, LL-pwr	KM62256CLGI-10L	28-SOP, 100ns, LL-pwr
KM62256CLP-7	28-DIP, 70ns, L-pwr	KM62256CLTGE-7	28-TSOP F, 70ns, L-pwr	KM62256CLTGI-7	28-TSOP F, 70ns, L-pwr
KM62256CLP-7L	28-DIP, 70ns, LL-pwr	KM62256CLTGE-7L	28-TSOP F, 70ns, LL-pwr	KM62256CLTGI-7L	28-TSOP F, 70ns, LL-pwr
KM62256CLG-4	28-SOP, 45ns, L-pwr	KM62256CLTGE-10	28-TSOP F, 100ns, L-pwr	KM62256CLTGI-10	28-TSOP F, 100ns, L-pwr
KM62256CLG-4L	28-SOP, 45ns, LL-pwr	KM62256CLTGE-10L	28-TSOP F, 100ns, LL-pwr	KM62256CLTGI-10L	28-TSOP F, 100ns, LL-pwr
KM62256CLG-5	28-SOP, 50ns, L-pwr	KM62256CLRGE-7	28-TSOP R, 70ns, L-pwr	KM62256CLRGI-7	28-TSOP R, 70ns, L-pwr
KM62256CLG-5L	28-SOP, 50ns, LL-pwr	KM62256CLRGE-7L	28-TSOP R, 70ns, LL-pwr	KM62256CLRGI-7L	28-TSOP R, 70ns, LL-pwr
KM62256CLG-7	28-SOP, 70ns, L-pwr	KM62256CLRGE-10	28-TSOP R, 100ns, L-pwr	KM62256CLRGI-10	28-TSOP R, 100ns, L-pwr
KM62256CLG-7L	28-SOP, 70ns, LL-pwr	KM62256CLRGE-10L	28-TSOP R, 100ns, LL-pwr	KM62256CLRGI-10L	28-TSOP R, 100ns, LL-pwr
KM62256CLTG-4	28-TSOP F, 45ns, L-pwr				
KM62256CLTG-4L	28-TSOP F, 45ns, LL-pwr				
KM62256CLTG-5	28-TSOP F, 55ns, L-pwr				
KM62256CLTG-5L	28-TSOP F, 55ns, LL-pwr				
KM62256CLTG-7	28-TSOP F, 70ns, L-pwr				
KM62256CLTG-7L	28-TSOP F, 70ns, LL-pwr				
KM62256CLRG-4	28-TSOP R, 45ns, L-pwr				
KM62256CLRG-4L	28-TSOP R, 45ns, LL-pwr				
KM62256CLRG-5	28-TSOP R, 55ns, L-pwr				
KM62256CLRG-5L	28-TSOP R, 55ns, LL-pwr				
KM62256CLRG-7	28-TSOP R, 70ns, L-pwr				
KM62256CLRG-7L	28-TSOP R, 70ns, LL-pwr				

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM62256CL/L-L
		-25 to 85	℃	KM62256CLE/LE-L
		-40 to 85	℃	KM62256CLI/LI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5V	V
Input low voltage	V_{IL}	-0.5***	-	0.8	V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Extended Product : T_A=-25 to 85℃, unless otherwise specified
3) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 50ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

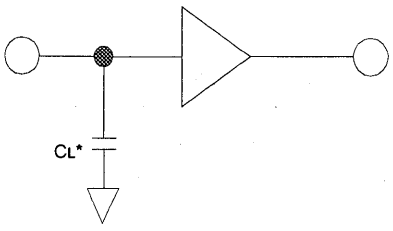
Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA		-	7	15***	mA
Average operating current		I_{CC1}	Cycle time=1μs 100% duty $\overline{CS}$≤ 0.2V, V_{IL}≤ 0.2V V_{IN} ≥Vcc -0.2V, I_{IO}=0mA		-	-	7****	mA
		I_{CC2}	Min cycle, 100% duty $\overline{CS}$=V_{IL}, I_{IO}=0mA		-	-	70	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS}$=V_{IH}		-	-	1*****	mA
Standby Current (CMOS)	KM62256CL KM62256CL-L	I_{SB1}	$\overline{CS}$ ≥Vcc-0.2V V_{IN}≥ 0.2V or V_{IN} ≤Vcc-0.2V	L(Low Power) LL(L Low Power)	- -	2 1	100 20	μA μA
	KM62256CLE KM62256CLE-L			L(Low Power) LL(L Low Power)	- -	- -	100 50	μA μA
	KM62256CLI KM62256CLI-L			L(Low Power) LL(L Low Power)	- -	- -	100 50	μA μA

* 1) Commercial Product : T_A=0 to 70℃, Vcc=5V±10% unless otherwise specified
2) Extended Product : T_A=-25 to 85℃, Vcc=5V±10% nless otherwise specified
3) Industrial Product : T_A=-40 to 85℃, Vcc=5V±10% unless otherwise specified
** T_A=25℃
*** 20mA for Extended and Industrial Products
****10mA for Extended and Industrial Products
*****2mA for Extended and Industrial Products

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL	-
	**C_L=30pF+1TTL	-



* Including scope and jig capacitance

* See DC Operating conditions
** Test load for 45ns commercial products

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM62256CL/L-L	0~70℃	5V ± 10%	45*/55/70ns	Commercial
KM62256CLE/LE-L	-25~85℃	5V ± 10%	70/100ns	Extended
KM62256CLI/LI-L	-40~85℃	5V ± 10%	70/100ns	Industrial

* The parameter is measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins								Units
			45ns*		55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	45	-	55	-	70	-	100	-	ns
	Address access time	tAA	-	45	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	45	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	20	0	30	0	35	ns
	Output disable to high-Z output	tOHZ	0	20	0	20	0	30	0	35	ns
	Output hold from address change	tOH	5	-	5	-	5	-	5	-	ns
Write	Write cycle time	tWC	45	-	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	20	0	25	0	35	ns
	Data to write time overlap	tDW	25	-	25	-	30	-	50	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	5	-	ns

* The parameter is measured with 30pF test load

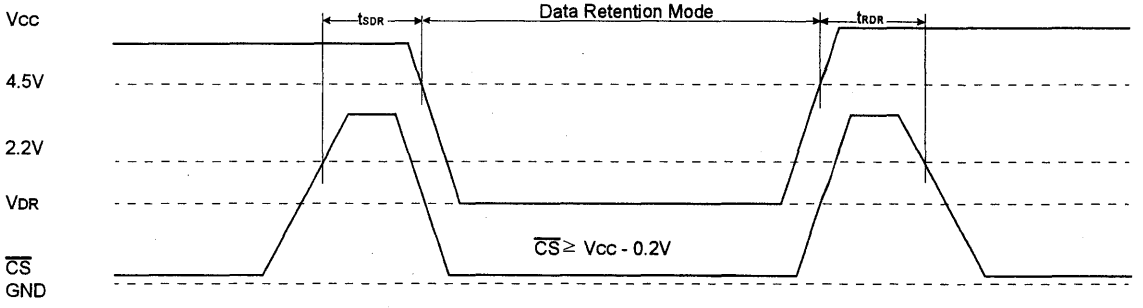
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	VDR		$\overline{CS}$ ≥ Vcc-0.2V		2.0	-	5.5	V
Data retention current	IDR	KM62256CL KM62256CL-L	Vcc=3.0V $\overline{CS}$ ≥ Vcc-0.2V	L-Ver LL-Ver	- -	1 0.5	50 10	μA
		KM62256CLE KM62256CLE-L		L-Ver LL-Ver	- -	- -	50 25	
		KM62256CLI KM62256CLI-L		L-Ver LL-Ver	- -	- -	50 25	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Extended Product : TA=-25 to 85℃, nless otherwise specified
3) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** TA=25℃

DATA RETENTION WAVE FORM

1) $\overline{CS}$ Controlled



FUNCTIONAL DESCRIPTION

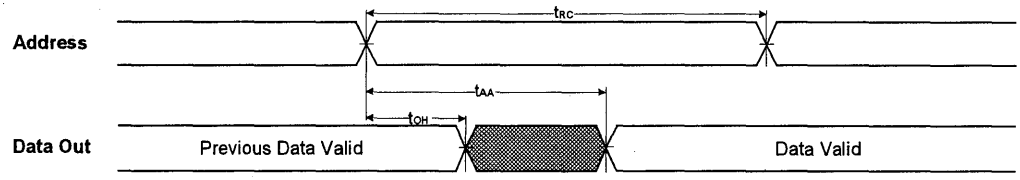
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	ISB ISB1
L	H	H	Output Disable	High-Z	Icc
L	H	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

* X means don't care

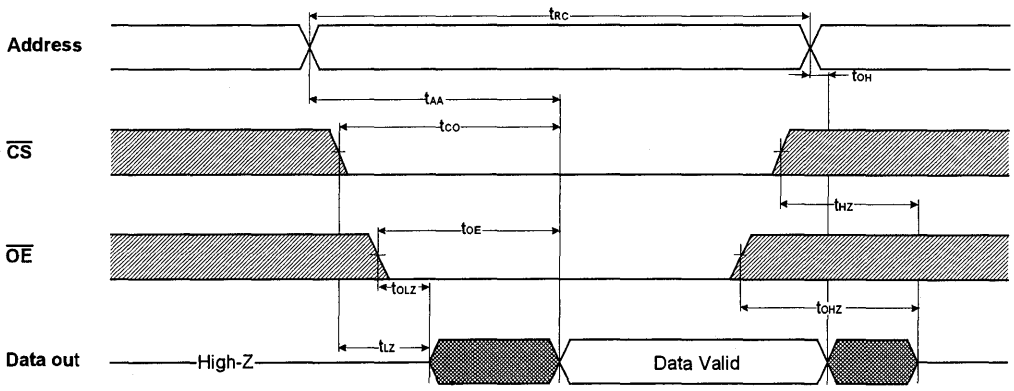
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



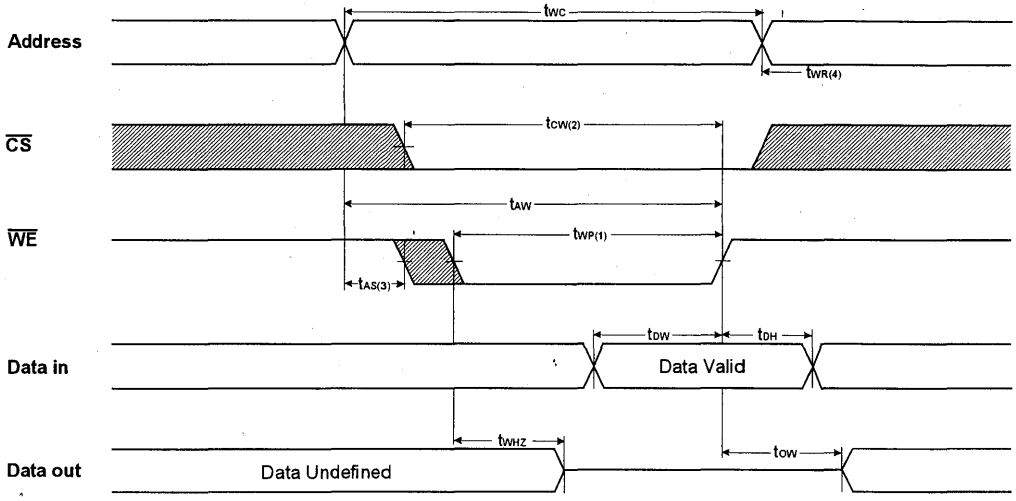
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



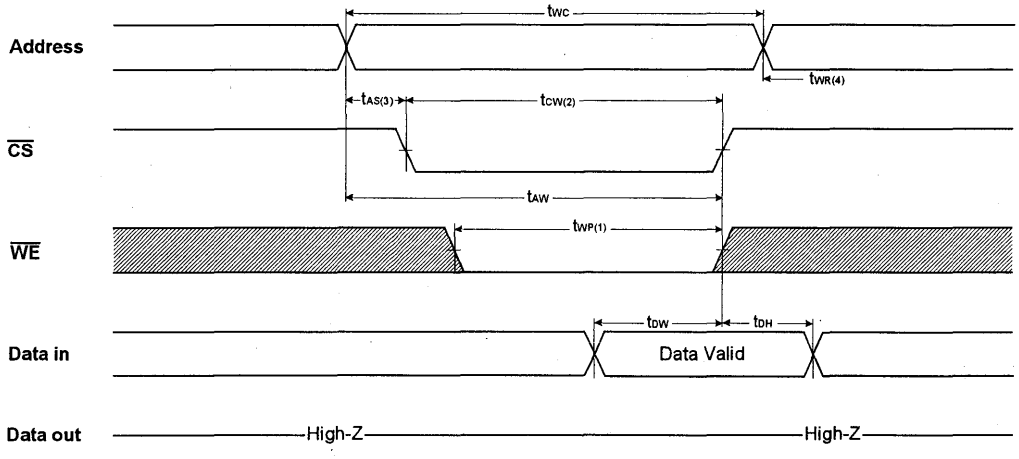
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ goes low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

32Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.4μm CMOS
- Organization : 32Kx8
- Power Supply Voltage : Single 5V ± 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  28-DIP, 28-SOP, 28-TSOP I -Forward/Reverse

GENERAL DESCRIPTION

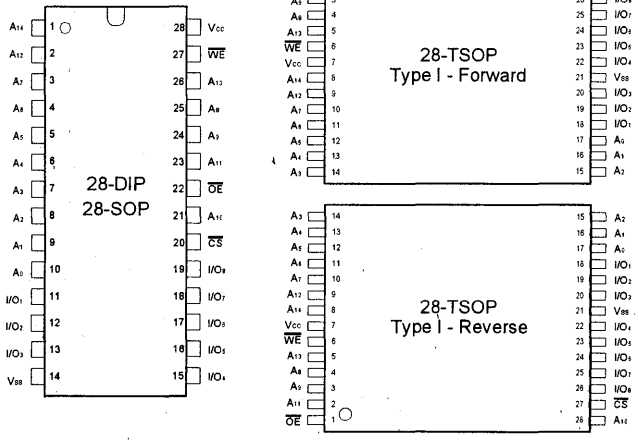
The KM62256D family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

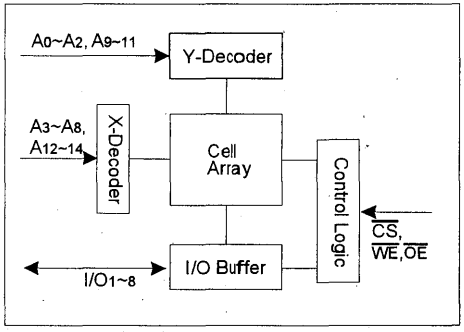
Product Family	Operating Temperature.	Speed (ns)	PKG Type	Power Dissipation	
				Standby (I_{SB1}, Max)	Operating (I_{CC2})
KM62256DL	Commercial (0~70℃)	45*/55/70ns	28-DIP,28-SOP 28-TSOP(I) R/F	50μA	70mA
KM62256DL-L				10μA	
KM62256DLI	Industrial (-40~85℃)	70/100ns	28-SOP 28-TSOP(I) R/F	50μA	
KM62256DLI-L				15μA	

* The parameter is measured with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Pin Name	Function
A_0~A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1~I/O_8	Data Inputs/Outputs
Vcc	Power(5V)
Vss	Ground

64Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.6㎛ CMOS
- Organization : 64Kx8
- Power Supply Voltage : Single 5V ± 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-SOP, 32-TSOP I -Forward

GENERAL DESCRIPTION

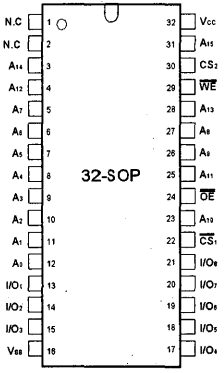
The KM68512A family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

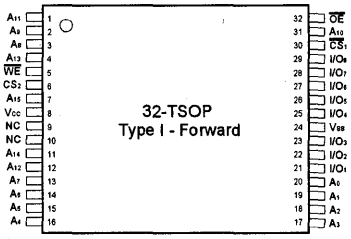
PRODUCT FAMILY

Product Family	Operating Temperature.	Vcc Range (V)	Speed (ns)	PKG Type	Power Dissipation	
					Standby (I_{SB1}, Max)	Operating (I_{CC2})
KM68512AL	Commercial (0~70℃)	5V±0.5V	45*/55/70ns	32-SOP 32-TSOP I F	100㎂	70mA
KM68512AL-L					20㎂	
KM68512ALI	Industrial (-40~85℃)	5V±0.5V	70/100ns	32-SOP 32-TSOP I F	100㎂	
KM68512ALI-L					50㎂	

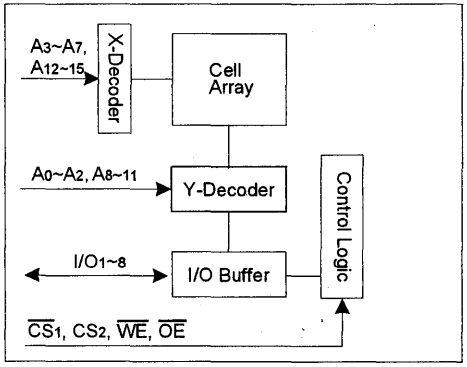
* The parameter measured with 30pF test load

PIN DESCRIPTION





FUNCTIONAL BLOCK DIAGRAM



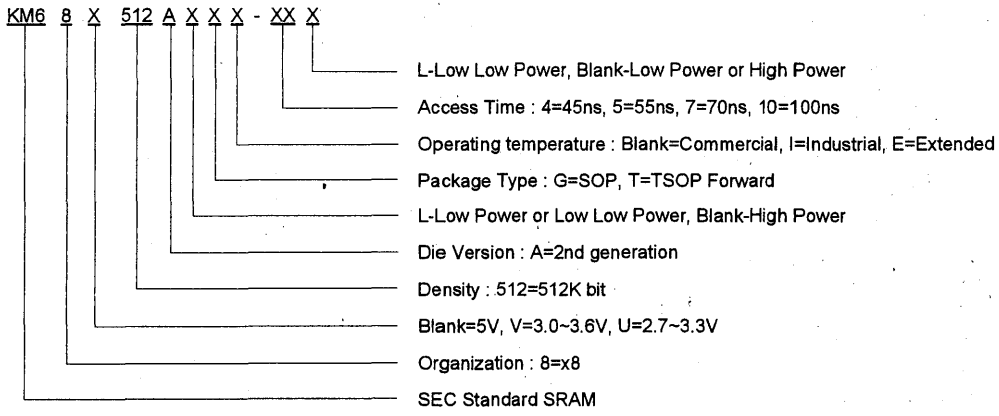
Name	Function
A_0~A_{15}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS_1}$, CS_2	Chip Select Inputs
$\overline{OE}$	Output Enable Input
I/O_1~I/O_{16}	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70°C)		Industrial Temp Products (-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**
KM68512ALG-4	32-SOP, 45ns, L-pwr	KM68512ALGI-7	32-SOP, 70ns, L-pwr
KM68512ALG-4L	32-SOP, 45ns, LL-pwr	KM68512ALGI-7L	32-SOP, 70ns, LL-pwr
KM68512ALG-5	32-SOP, 55ns, L-pwr	KM68512ALGI-10	32-SOP, 100ns, L-pwr
KM68512ALG-5L	32-SOP, 55ns, LL-pwr	KM68512ALGI-10L	32-SOP, 100ns, LL-pwr
KM68512ALG-7	32-SOP, 70ns, L-pwr	KM68512ALTI-7	32-TSOP F, 70ns, L-pwr
KM68512ALG-7L	32-SOP, 70ns, LL-pwr	KM68512ALTI-7L	32-TSOP F, 70ns, LL-pwr
KM68512ALT-4	32-TSOP F, 45ns, L-pwr	KM68512ALTI-10	32-TSOP F, 100ns, L-pwr
KM68512ALT-4L	32-TSOP F, 45ns, LL-pwr	KM68512ALTI-10L	32-TSOP F, 100ns, LL-pwr
KM68512ALT-5	32-TSOP F, 55ns, L-pwr		
KM68512ALT-5L	32-TSOP F, 55ns, LL-pwr		
KM68512ALT-7	32-TSOP F, 70ns, L-pwr		
KM68512ALT-7L	32-TSOP F, 70ns, LL-pwr		

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM68512AL/L-L
		-40 to 85	℃	KM68512ALI/LI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5V	V
Input low voltage	V_{IL}	-0.5***	-	0.8	V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for 50ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

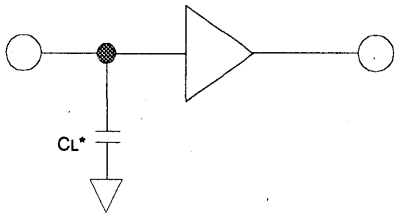
Item		Symbol	Test Conditions*		Mi	Typ**	Max	Uni
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA		-	7	15	mA
Average operating current		I_{CC1}	Cycle time=1μs 100% duty $\overline{CS_1}$≤ 0.2V, CS_2≥Vcc-0.2V V_{IL} ≤0.2V, V_{IH} ≥Vcc -0.2V, I_{IO}=0mA		-	-	10	mA
		I_{CC2}	Min cycle, 100% duty $\overline{CS_1}$=V_{IL}, CS_2=V_{IH} I_{IO}=0mA		-	-	70	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL}		-	-	3	mA
Standby Current (CMOS)	KM68512AL/L-L	I_{SB1}	$\overline{CS_1}$ ≥Vcc-0.2V CS_2 ≤0.2V V_{IN}≤0.2V or V_{IN}≥Vcc-0.2V	L(Low Power) LL(L Low Power)	- -	2 1	100 20	μA μA
	KM68512ALI/LI-L			L(Low Power) LL(L Low Power)	- -	2 1	100 50	μA μA

* 1) Commercial Product : T_A=0 to 70℃, Vcc=5V±10% unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, Vcc=5V±10% unless otherwise specified
** T_A=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL	-
	**C_L=30pF+1TTL	-



* Including scope and jig capacitance

* See DC Operating conditions
**KM68512AL/AL-4L

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68512AL/L-L	0~70℃	5V ± 10%	45*/55/70ns	Commercial
KM68512ALI/LI-L	-40~85℃	5V ± 10%	70/100ns	Industrial

* The parameter is measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins								Units
			45ns*		55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	45	-	55	-	70	-	100	-	ns
	Address access time	tAA	-	45	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	45	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	45	-	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	10	-	ns

* The parameters is measured with 30pf test load.

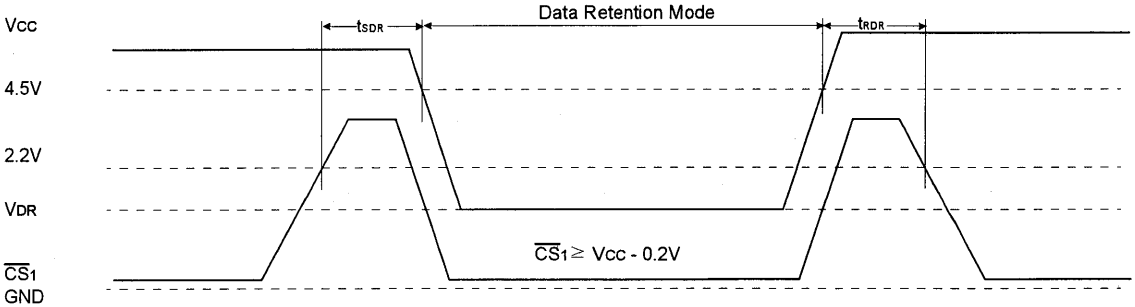
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		***$\overline{CS_1}$ ≥ Vcc-0.2V		2.0	-	5.5	V
Data retention current	I_{DR}	KM68512AL/L-L	Vcc=3.0V $\overline{CS_1}$ ≥ Vcc-0.2V	L-Ver LL-Ver	- -	1 0.5	50 10	μA
		KM68512ALI/LI-L		L-Ver LL-Ver	- -	- -	50 25	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

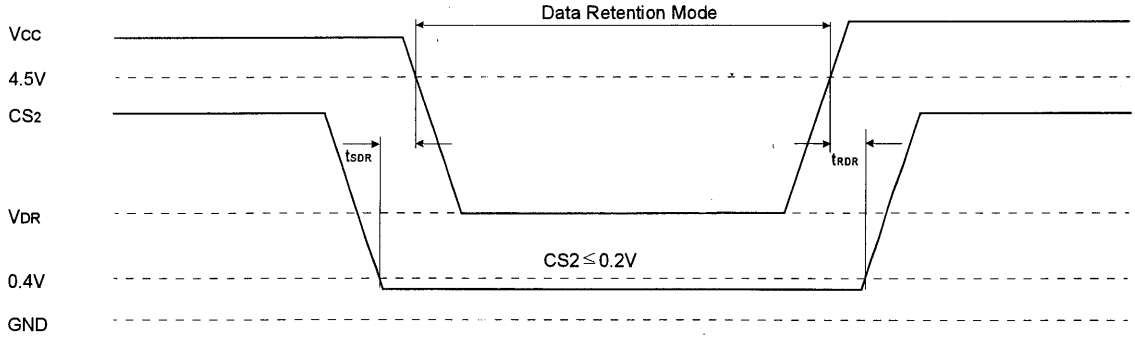
* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** $\overline{CS_1}$ ≥Vcc-2.0V, CS_2 ≥Vcc-2.0V($\overline{CS_1}$ controlled) or CS_2 ≤0.2V(CS_2 controlled)

DATA RETENTION WAVE FORM

1) $\overline{CS_1}$ Controlled



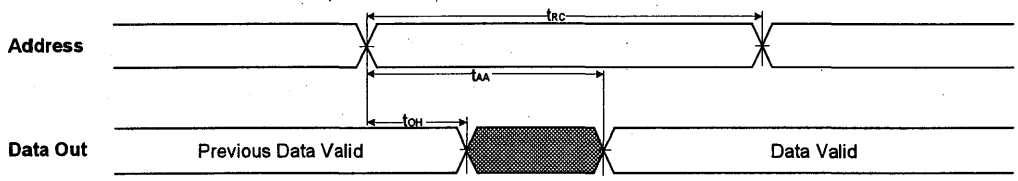
2) CS_2 Controlled



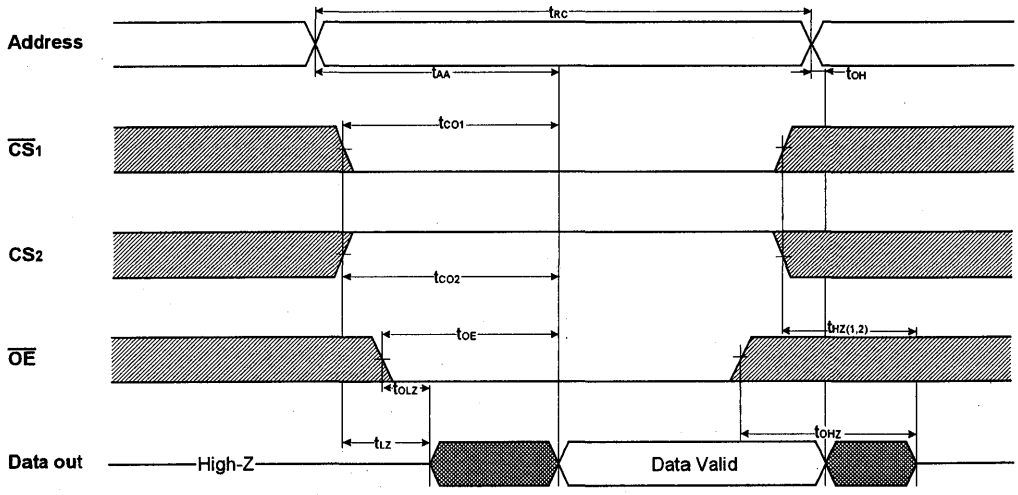
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2= $\overline{WE}$=V_{IH})



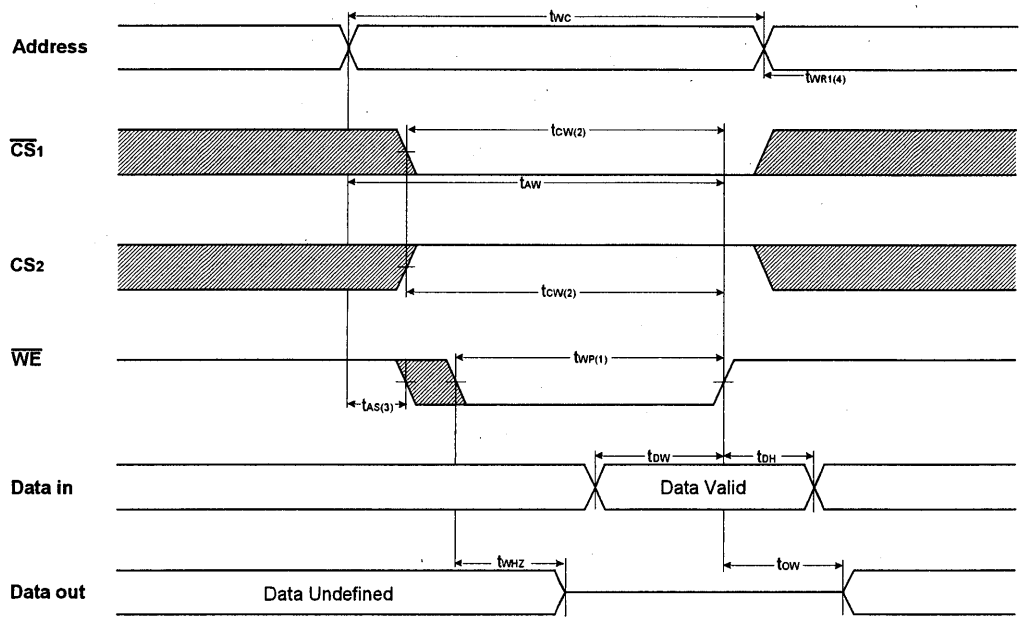
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



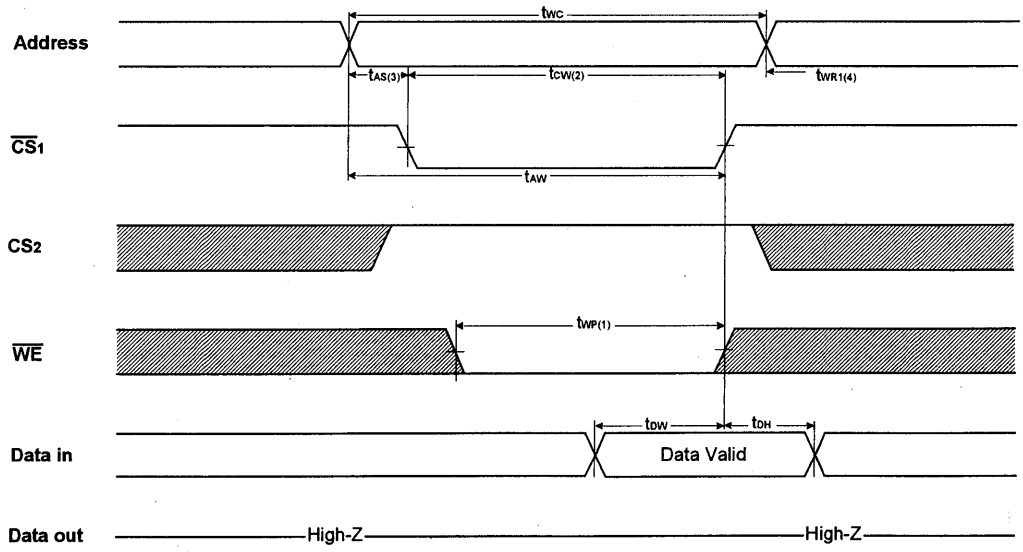
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device interconnection.

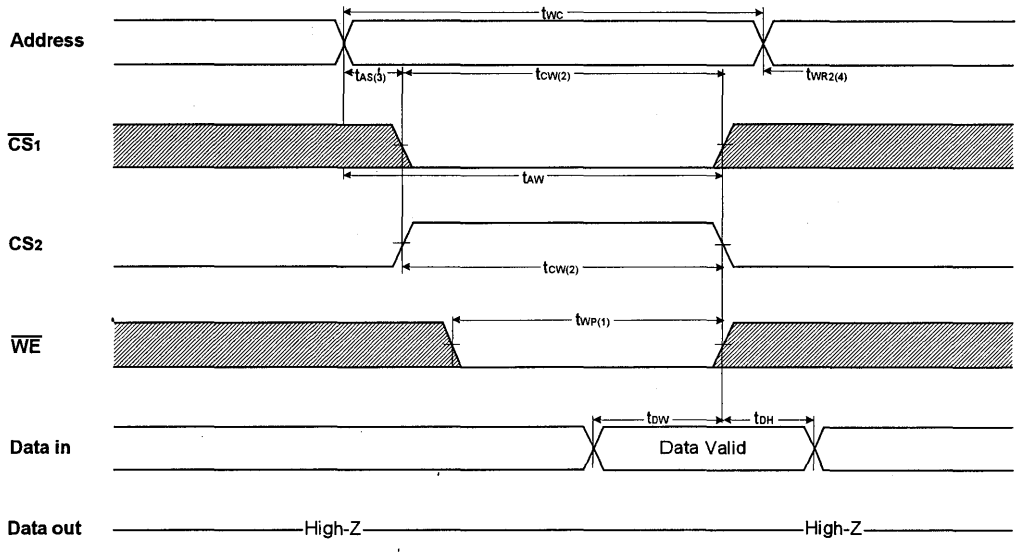
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS_2 Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap of low $\overline{CS_1}$, high CS_2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low : A write ends at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the begining of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high t_{WR2} applied in case a write ends as CS_2 going to low.

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	Dout	I_{CC}
L	H	L	X	Write	Din	I_{CC}

* X means don't care

128K x8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.6㎛ CMOS
- Organization : 128Kx8
- Power Supply Voltage : Single 5.0V ± 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-DIP, 32-SOP, 32-TSOP I R/F

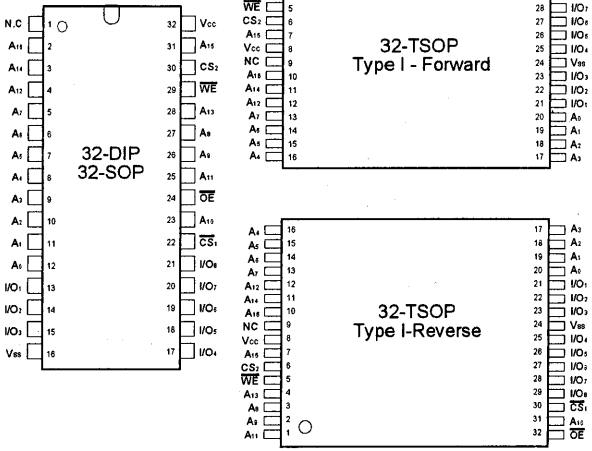
GENERAL DESCRIPTION

The KM681000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

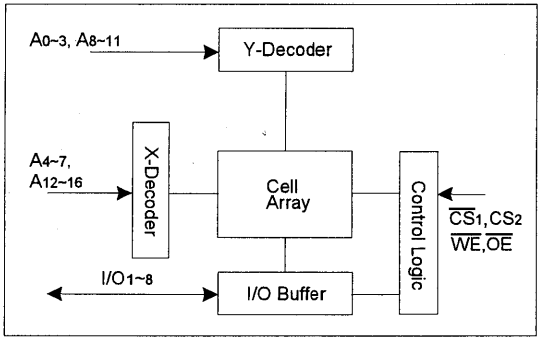
PRODUCT FAMILY

Product Family	Operating Temperature	Speed	PKG Type	Power Dissipation	
				Standby (I_{SB1}, Max)	Operating (I_{CC2})
KM681000BL	Commercial(0~70℃)	55/70ns	32-DIP,32-SOP 32-TSOP I R/F	100㎂	70mA
KM681000BL-L				20㎂	
KM681000BLE	Extended(-25~85℃)	70/100ns	32-SOP 32-TSOP I R/F	100㎂	
KM681000BLE-L				50㎂	
KM681000BLI	Industrial(-40~85℃)	70/100ns	32-SOP 32-TSOP I R/F	100㎂	
KM681000BLI-L				50㎂	

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



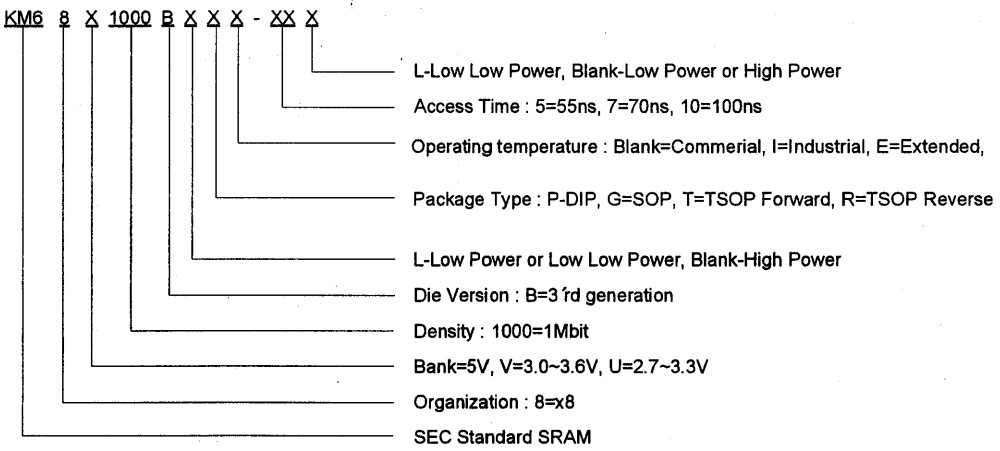
Name	Function
A0~A16	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS_1}$,CS2	Chip Select Inputs
$\overline{OE}$	Output Enable Input
I/O1~I/O18	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Extended Temp Products (-25~85℃)		Industrial Temp Products (-40~85℃)	
Part Name	Function	Part Name	Function	Part Name	Function
KM681000BLP-5	32-DIP,55ns,L-pwr	KM681000BLGE-7	32-SOP,70ns,L-pwr	KM681000BLGI-7	32-SOP,70ns,L-pwr
KM681000BLP-5L	32-DIP,55ns,LL-pwr	KM681000BLGE-7L	32-SOP,70ns,LL-pwr	KM681000BLGI-7L	32-SOP,70ns,LL-pwr
KM681000BLP-7	32-DIP,70ns,L-pwr	KM681000BLGE-10	32-SOP,100ns,L-pwr	KM681000BLGI-10	32-SOP,100ns,L-pwr
KM681000BLP-7L	32-DIP,70ns,LL-pwr	KM681000BLGE-10L	32-SOP,100ns,LL-pwr	KM681000BLGI-10L	32-SOP,100ns,LL-pwr
KM681000BLG-5	32-SOP,55ns,L-pwr	KM681000BLTE-7	32-TSOP F,70ns,L-pwr	KM681000BLTI-7	32-TSOP F,70ns,L-pwr
KM681000BLG-5L	32-SOP,55ns,LL-pwr	KM681000BLTE-7L	32-TSOP F,70ns,LL-pwr	KM681000BLTI-7L	32-TSOP F,70ns,LL-pwr
KM681000BLG-7	32-SOP,70ns,L-pwr	KM681000BLTE-10	32-TSOP F,100ns,L-pwr	KM681000BLTI-10	32-TSOP F,100ns,L-pwr
KM681000BLG-7L	32-SOP,70ns,LL-pwr	KM681000BLTE-10L	32-TSOP F,100ns,LL-pwr	KM681000BLTI-10L	32-TSOP F,100ns,LL-pwr
KM681000BLT-5	32-TSOP F,55ns,L-pwr	KM681000BLRE-7	32-TSOP R,70ns,L-pwr	KM681000BLRI-7	32-TSOP R,70ns,L-pwr
KM681000BLT-5L	32-TSOP F,55ns,LL-pwr	KM681000BLRE-7L	32-TSOP R,70ns,LL-pwr	KM681000BLRI-7L	32-TSOP R,70ns,LL-pwr
KM681000BLT-7	32-TSOP F,70ns,L-pwr	KM681000BLRE-10	32-TSOP R,100ns,L-pwr	KM681000BLRI-10	32-TSOP R,100ns,L-pwr
KM681000BLT-7L	32-TSOP F,70ns,LL-pwr	KM681000BLRE-10L	32-TSOP R,100ns,LL-pwr	KM681000BLRI-10L	32-TSOP R,100ns,LL-pwr
KM681000BLR-5	32-TSOP R,55ns,L-pwr				
KM681000BLR-5L	32-TSOP R,55ns,LL-pwr				
KM681000BLR-7	32-TSOP R,70ns,L-pwr				
KM681000BLR-7L	32-TSOP R,70ns,LL-pwr				

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM681000BL/L-L
		-25 to 85	℃	KM681000BLE/LE-L
		-40 to 85	℃	KM681000BLI/LI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5	V
Input low voltage	V_{IL}	-0.5***	-	0.8	V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Extended Product : T_A=-25 to 85℃, unless otherwise specified
3) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 50ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	Vin=0V	-	6	pF
Input/Output capacitance	C_{IO}	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Mi	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA		-	7	15**	mA
Average operating current		I_{CC1}	Cycle time=1μs 100% duty $\overline{CS_1}$≤0.2V, CS_2≥Vcc-0.2V		-	-	10***	mA
		I_{CC2}	I_{IO}=0mA $\overline{CS_1}$=V_{IL},CS_2=V_{IH} Min cycle, 100% duty		-	-	70	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL}		-	-	3	mA
Standby Current (CMOS)	KM681000BL KM681000BL-L	I_{SB1}	$\overline{CS_1}$≥Vcc-0.2V CS_2≥Vcc-0.2V or CS_2≤0.2V Other input=0~Vcc	L (Low Power) LL (Low Low Power)	- -	- -	100 20	μA μA
	KM681000BLE KM681000BLE-L			L (Low Power) LL (Low Low Power)	- -	- -	100 50	μA μA
	KM681000BLI KM681000BLI-L			L (Low Power) LL (Low Low Power)	- -	- -	100 50	μA μA

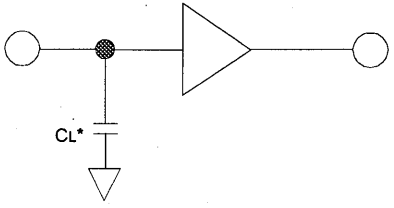
* 1) Commercial Product : T_A=0 to 70℃, Vcc=5.0V±10%, unless otherwise specified
2) Extended Product : T_A=-25 to 85℃, Vcc=5.0V±10%, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, Vcc=5.0V±10%, unless otherwise specified
** 20mA for Exteneded and Industrial Products
*** 15mA for Extended and Industrial Products

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL	-

* See DC Operating conditions



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM681000BL/L-L	0~70℃	5.0V±10%	55/70ns	Commercial
KM681000BLE/LE-L	-25~85℃	5.0V±10%	70/100ns	Extended
KM681000BLI/LI-L	-40~85℃	5.0V±10%	70/100ns	Industrial

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tCO1,tCO2	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ1,tLZ2	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ1,tHZ2	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

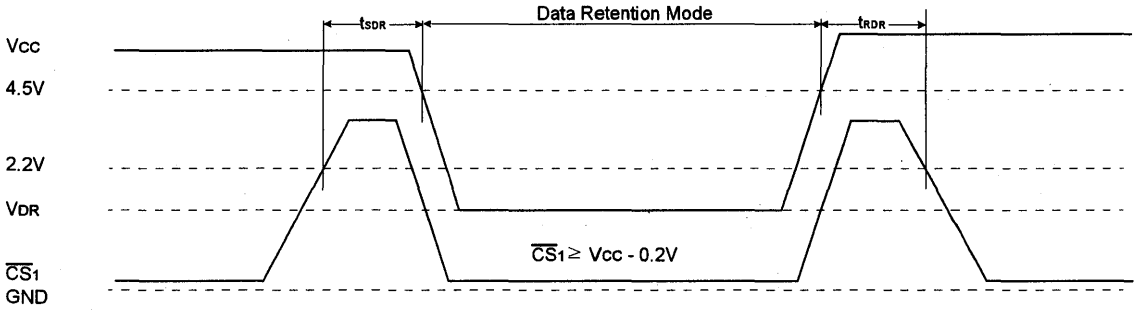
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS_1}$*** ≥ Vcc-0.2V		2.0	-	5.5	V
Data retention current	I_{DR}	KM681000BL KM681000BL-L	Vcc=3.0V $\overline{CS_1}$ ≥ Vcc-0.2V	L-Ver LL-Ver	- -	1 0.5	50 10	μA
		KM681000BLE KM681000BLE-L		L-Ver LL-Ver	- -	- -	50 25	
		KM681000BLI KM681000BLI-L		L-Ver LL-Ver	- -	- -	50 25	
Data retention set-up time	tRDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

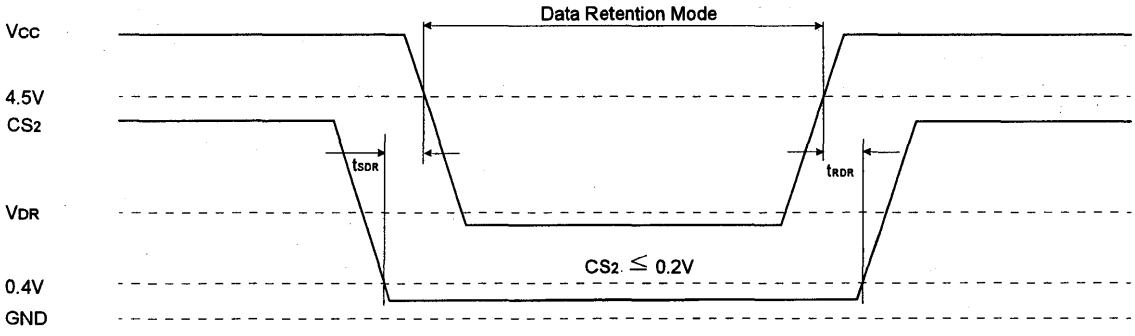
* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Extended Product : T_A=-25 to 85℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** $\overline{CS_1}$≥Vcc-0.2V,CS_2≥Vcc-0.2V($\overline{CS_1}$ controlled) or CS_2≤0.2V(CS_2 controlled)

DATA RETENTION TIMING DIAGRAM

1) $\overline{CS_1}$ Controlled



2) $\overline{CS_2}$ controlled

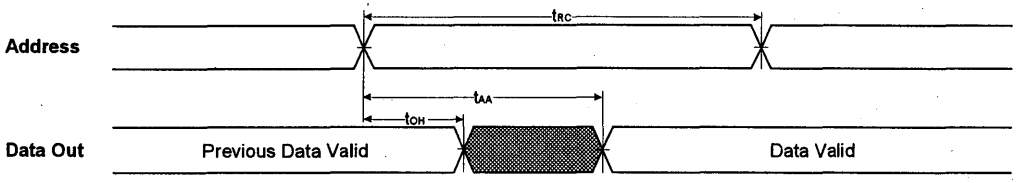


SAMSUNG ELECTRONICS

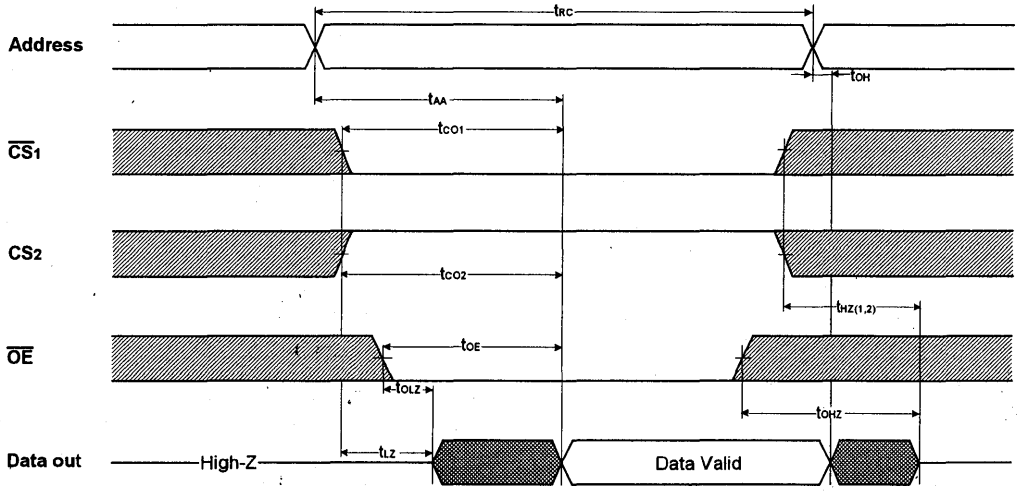
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2= $\overline{WE}$= V_{IH})



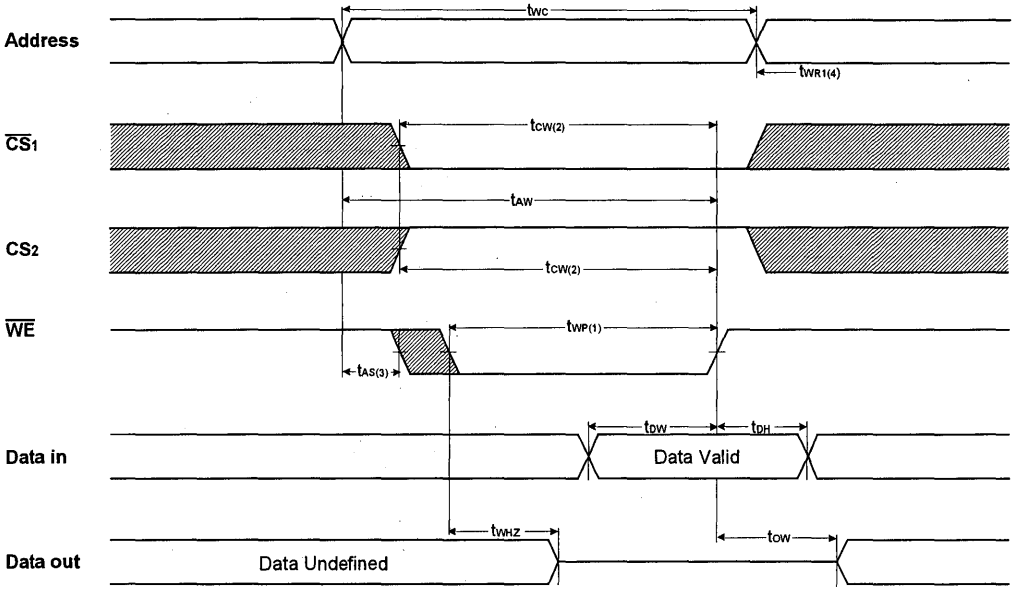
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=V_{IH})



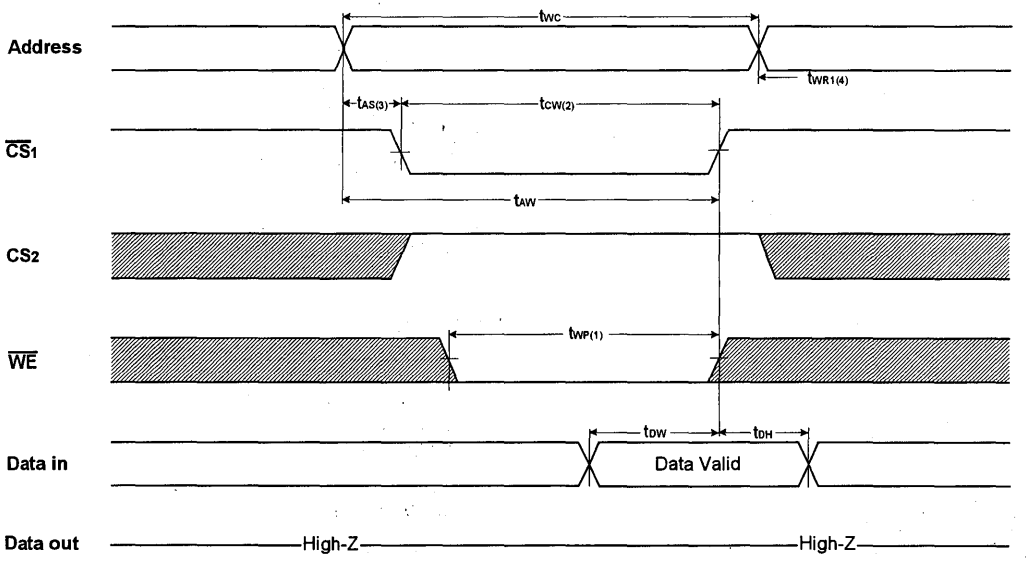
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.

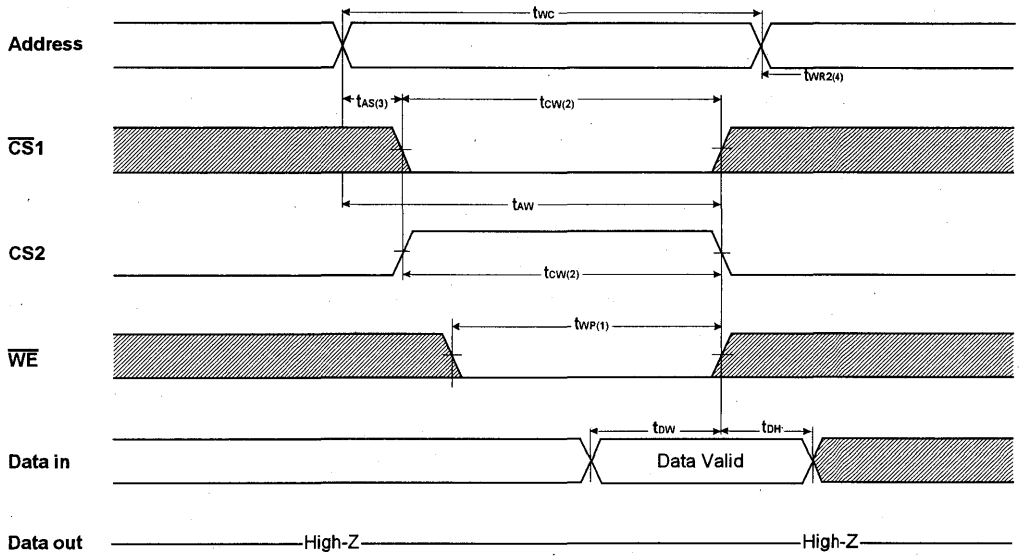
TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{CS}_2$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap of low $\overline{CS}_1$, high CS_2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}_1$ going low, CS_2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS}_1$ going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning or write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}_1$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address calid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends at $\overline{CS}_1$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS_2 going to low.

FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	I_{SB},I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB},I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	Dout	I_{CC}
L	H	L	X	Write	Din	I_{CC}

* X means don't care

128K x8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.4㎛ CMOS
- Organization : 128K x8
- Power Supply Voltage : Single 5.0V±10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-DIP, 32-SOP, 32-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

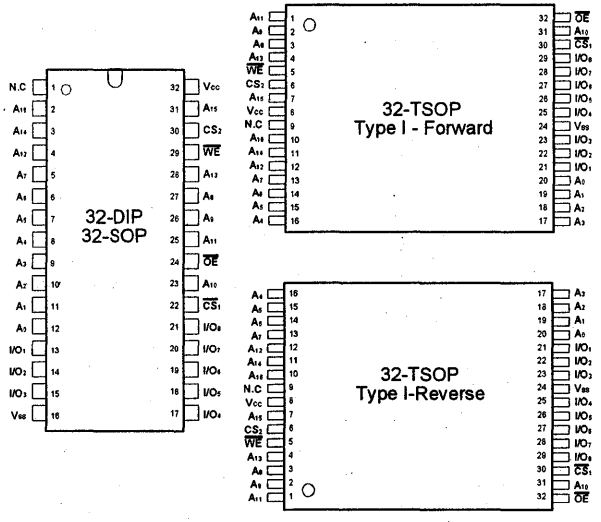
The KM681000C family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

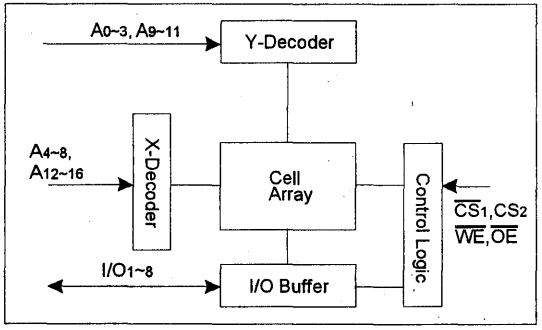
Product Family	Operating Temperature	Vcc Range(V)	Speed	PKG Type	Power Dissipation	
					Standby (I_{SB1}, Max)	Operating (I_{CC2})
KM681000CL	Commercial(0~70℃)	4.5~5.5V	45*/55/70ns	32-DIP,32-SOP 32-TSOP(I) R/F	50㎂ 10㎂	90mA
KM681000CL-L						
KM681000CLI	Industrial(-40~85℃)	4.5~5.5V	55*/70/85ns	32-DIP,32-SOP 32-TSOP(I) R/F	50㎂ 15㎂	
KM681000CLI-L						

*The parameter is measured with 30pF test load

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



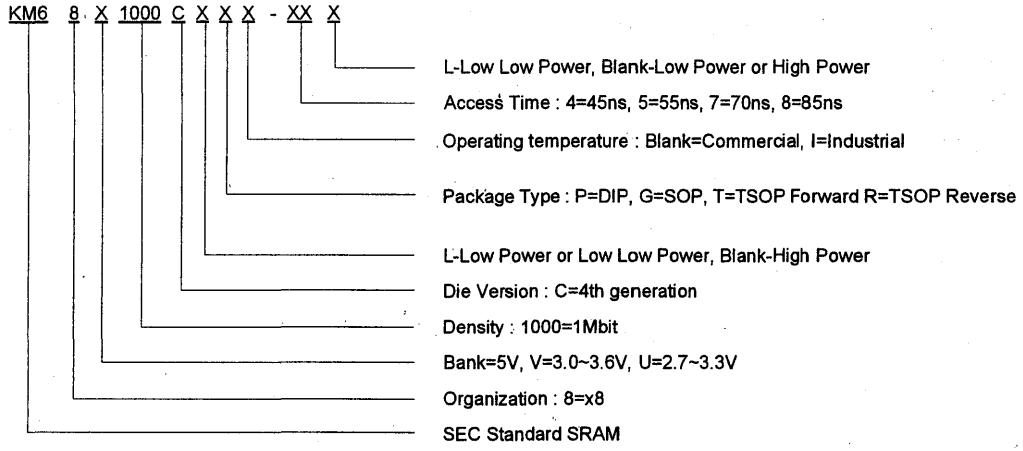
Name	Function
A0~A16	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$,CS2	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power (+5.0V)
Vss	Ground
N.C	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Industrial Temp Products (-40~85℃)	
Part Name	**Function**	**Part Name**	**Function**
KM681000CLP-4	32-DIP, 45ns, L-pwr	KM681000CLGI-5	32-SOP, 55ns, L-pwr
KM681000CLP-5	32-DIP, 55ns, L-pwr	KM681000CLGI-7	32-SOP, 70ns, L-pwr
KM681000CLP-7	32-DIP, 70ns, L-pwr	KM681000CLGI-8	32-SOP, 85ns, L-pwr
KM681000CLP-4L	32-DIP, 45ns, LL-pwr	KM681000CLGI-5L	32-SOP, 55ns, LL-pwr
KM681000CLP-5L	32-DIP, 55ns, LL-pwr	KM681000CLGI-7L	32-SOP, 70ns, LL-pwr
KM681000CLP-7L	32-DIP, 70ns, LL-pwr	KM681000CLGI-8L	32-SOP, 85ns, LL-pwr
KM681000CLG-4	32-SOP, 45ns, L-pwr	KM681000CLTI-5	32-TSOP(I) F, 55ns, L-pwr
KM681000CLG-5	32-SOP, 55ns, L-pwr	KM681000CLTI-7	32-TSOP(I) F, 70ns, L-pwr
KM681000CLG-7	32-SOP, 70ns, L-pwr	KM681000CLTI-8	32-TSOP(I) F, 85ns, L-pwr
KM681000CLG-4L	32-SOP, 45ns, LL-pwr	KM681000CLTI-5L	32-TSOP(I) F, 55ns, LL-pwr
KM681000CLG-5L	32-SOP, 55ns, LL-pwr	KM681000CLTI-7L	32-TSOP(I) F, 70ns, LL-pwr
KM681000CLG-70L	32-SOP, 70ns, LL-pwr	KM681000CLTI-8L	32-TSOP(I) F, 85ns, LL-pwr
KM681000CLT-4	32-TSOP(I) F, 45ns, L-pwr	KM681000CLRI-5	32-TSOP(I) R, 55ns, L-pwr
KM681000CLT-5	32-TSOP(I) F, 55ns, L-pwr	KM681000CLRI-7	32-TSOP(I) R, 70ns, L-pwr
KM681000CLT-7	32-TSOP(I) F, 70ns, L-pwr	KM681000CLRI-8	32-TSOP(I) R, 85ns, L-pwr
KM681000CLT-4L	32-TSOP(I) F, 45ns, LL-pwr	KM681000CLRI-5L	32-TSOP(I) R, 55ns, LL-pwr
KM681000CLT-5L	32-TSOP(I) F, 55ns, LL-pwr	KM681000CLRI-7L	32-TSOP(I) R, 70ns, LL-pwr
KM681000CLT-70L	32-TSOP(I) F, 70ns, LL-pwr	KM681000CLRI-8L	32-TSOP(I) R, 85ns, LL-pwr
KM681000CLR-4	32-TSOP(I) R, 45ns, L-pwr		
KM681000CLR-5	32-TSOP(I) R, 55ns, L-pwr		
KM681000CLR-7	32-TSOP(I) R, 70ns, L-pwr		
KM681000CLR-4L	32-TSOP(I) R, 45ns, LL-pwr		
KM681000CLR-5L	32-TSOP(I) R, 55ns, LL-pwr		
KM681000CLR-70L	32-TSOP(I) R, 70ns, LL-pwr		

ORDERING INFORMATION



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM681000CL/L-L
		-40 to 85	℃	KM681000CLI/LI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5	V
Input low voltage	V_{IL}	-0.5***	-	0.8	V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 50ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA	Read	-	-	15	mA
				Write			35	
Average operating current		I_{CC1}	Cycle time=1μs 100% duty $\overline{CS_1}$≤0.2V, CS_2≥Vcc-0.2V, I_{IO}=0mA	Read	-	-	15	mA
				Write			35	
		I_{CC2}	I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH} Min cycle, 100% duty		-	-	90	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS_1}$=V_{IH}, CS2=V_{IL}		-	-	3	mA
Standby Current (CMOS)	KM681000C KM681000CL-L	I_{SB1}	$\overline{CS_1}$≥Vcc-0.2V CS_2≥Vcc-0.2V or CS_2≤0.2V Other input=0~Vcc	L(Low Power) LL(L Low Power)	- -	- -	50 10	μA
	KM681000CLI KM681000CLI-L			L(Low Power) LL(L Low Power)	- -	- -	50 15	μA

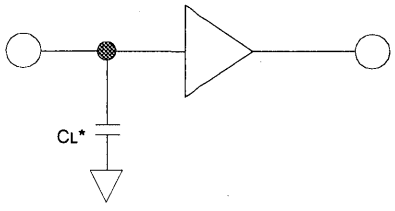
* 1) Commercial Product : T_A=0 to 70℃, Vcc=5V±10% Unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, Vcc=5V±10% Unless otherwise specified
** T_A=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL **C_L=30pF+1TTL	-

* See DC Operating conditions
** Test load for 45ns(Commercial product)/55ns(Industrial product)



* Including scope and jig capacitance

SAMSUNG ELECTRONICS

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM681000CL/L-L	0~70℃	5V±10%	45*/55/70ns	Commercial
KM681000CLI/LI-L	-40~85℃	5V±10%	55*/70/85ns	Industrial

*The parameter is measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins								Units
			45ns		55ns		70ns		85ns		
			Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	45	-	55	-	70	-	85	-	ns
	Address access time	tAA	-	45	-	55	-	70	-	85	ns
	Chip select to output	tCO1,tCO	-	45	-	55	-	70	-	85	ns
	Output enable to valid output	tOE	-	20	-	25	-	35	-	40	ns
	Chip select to low-Z output	tLZ1,tLZ2	10	-	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ1,tHZ2	0	15	0	20	0	25	0	25	ns
	Output disable to high-Z output	tOHZ	0	15	0	20	0	25	0	25	ns
	Output hold from address change	tOH	10	-	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	45	-	55	-	70	-	85	-	ns
	Chip select to end of write	tCW	40	-	45	-	60	-	70	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	40	-	45	-	60	-	70	-	ns
	Write pulse width	tWP	35	-	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	15	0	20	0	25	0	25	ns
	Data to write time overlap	tDW	25	-	25	-	30	-	35	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	5	-	ns

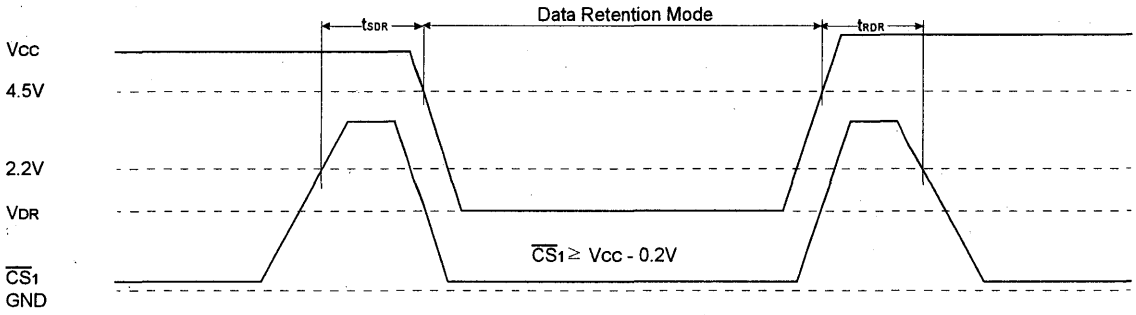
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS_1}$*** ≥ Vcc-0.2V		2.0	-	5.5	V
Data retention current	I_{DR}	KM681000CL KM681000CL-L	Vcc=3.0V $\overline{CS_1}$ ≥ Vcc-0.2V	L-Ver LL-Ver	- -	1 0.5	20 10	μA
		KM681000CLI KM681000CLI-L		L-Ver LL-Ver	- -	- -	25 10	
Data retention set-up	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

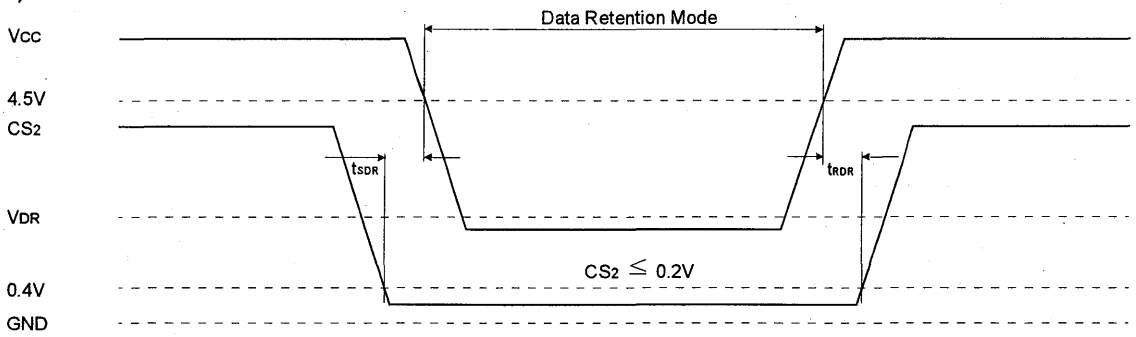
* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** $\overline{CS_1}$ ≥ Vcc-0.2V, CS_2 ≥ Vcc-0.2V($\overline{CS_1}$ controlled) or CS_2 ≤ 0.2V(CS_2 controlled)

DATA RETENTION TIMING DIAGRAM

1) $\overline{CS_1}$ Controlled



2) $\overline{CS_2}$ controlled

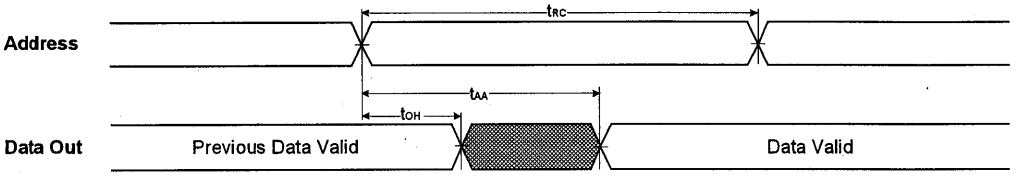


SAMSUNG ELECTRONICS

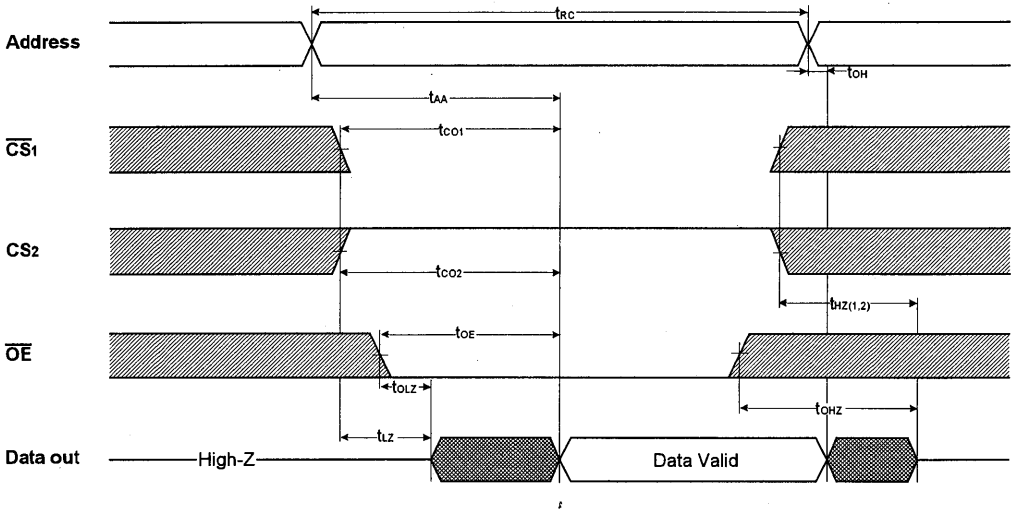
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=$\overline{WE}$=V_{IH})



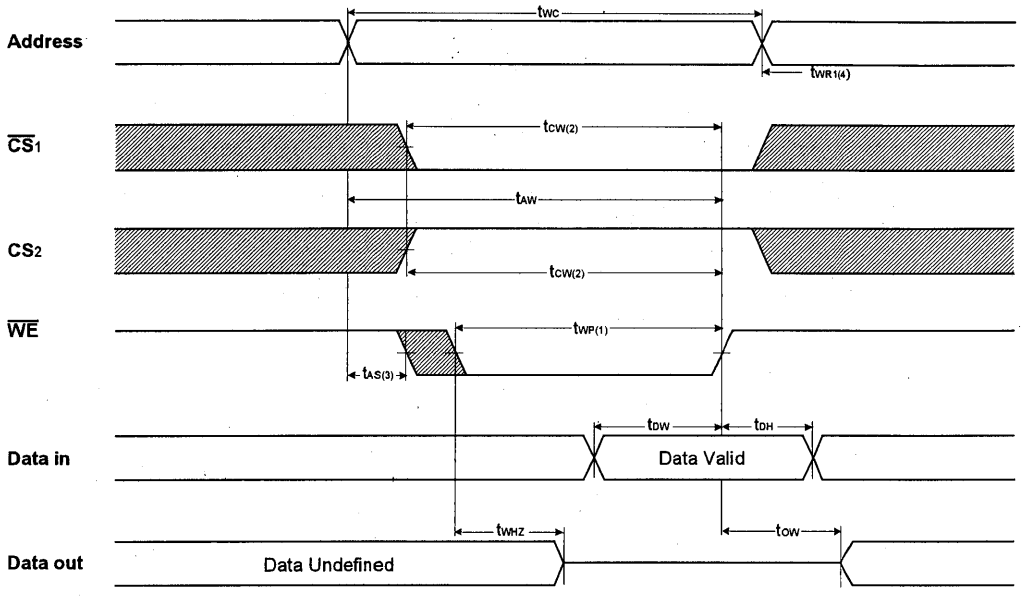
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=V_{IH})



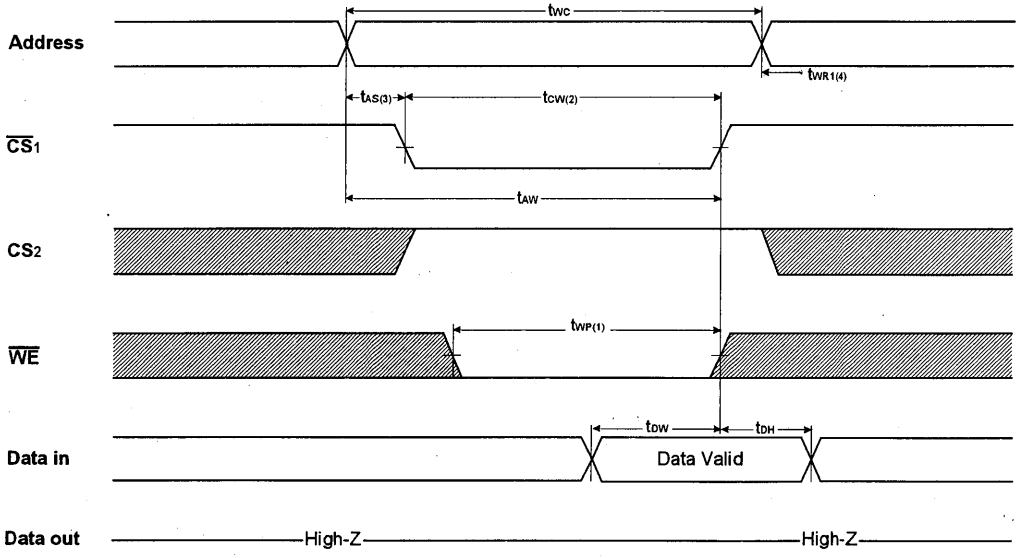
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.

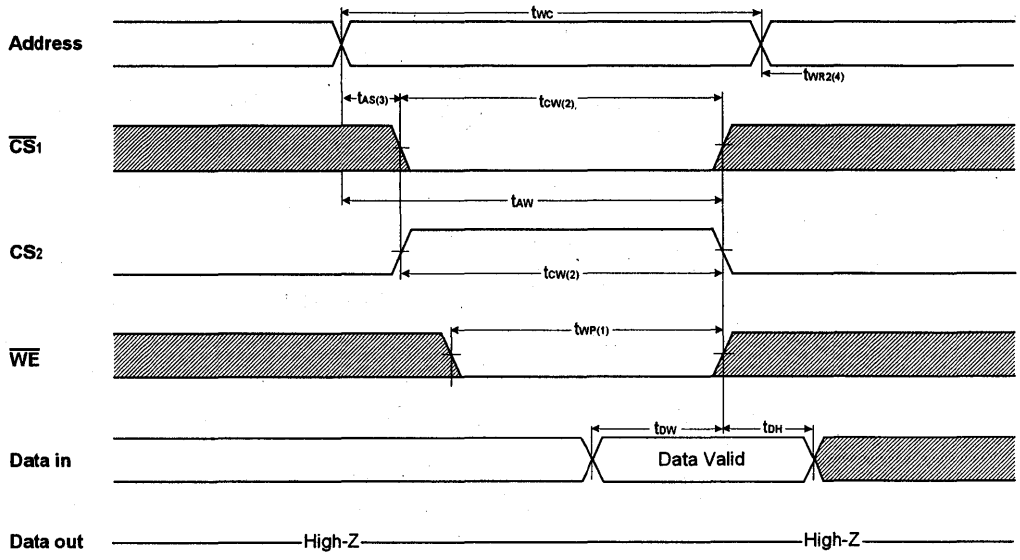
TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS_2 Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap of low $\overline{CS_1}$, high CS_2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ going low, CS_2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning or write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address calid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends at $\overline{CS_1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS_2 going to low.

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	I_{SB},I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB},I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	Dout	I_{CC}
L	H	L	X	Write	Din	I_{CC}

* X means don't care

64K x16 bit Low Power CMOS Static RAM

FEATURES SUMMARY

- Process Technology : 0.6㎛ CMOS
- Organization : 64K x16
- Data Byte Control : $\overline{LB}$=I/O1~8, $\overline{UB}$=I/O9~16
- Power Supply Voltage : 5.0V ±10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  44-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

The KM6161000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

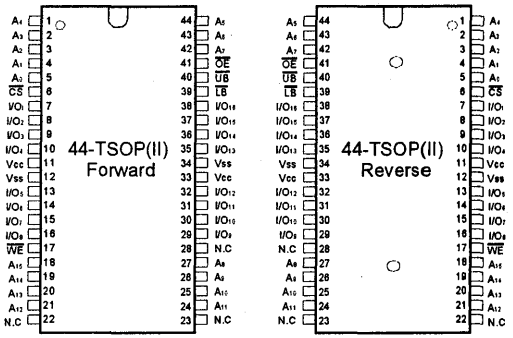
2

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range(V)	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM6161000BLT/LT-L KM6161000BLR/LR-L	Commercia (0~70℃)	4.5 to 5.5	55*/70	100/20㎂	120mA	44-TSOP(II) Forward/Reverse
KM6161000BLTI/LTI-L KM6161000BLRI/LRI-L	Industrial (-40~85℃)	4.5 to 5.5	70/100	100/50㎂		

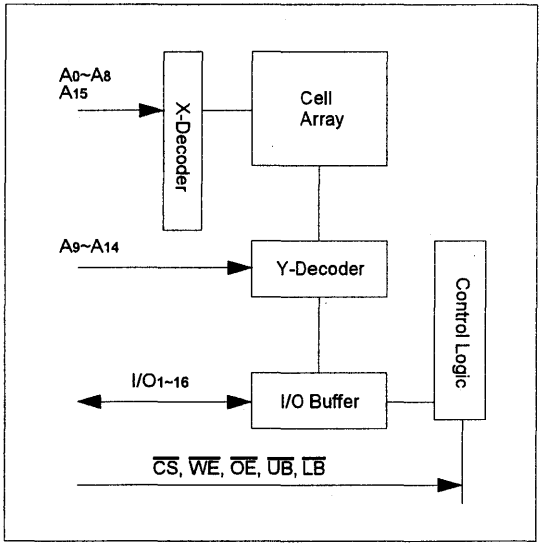
* The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
A0~A15	Address Inputs	$\overline{LB}$	Lower Byte (I/O1~8)
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O9~16)
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
I/O1~16	Data Inputs/Outputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



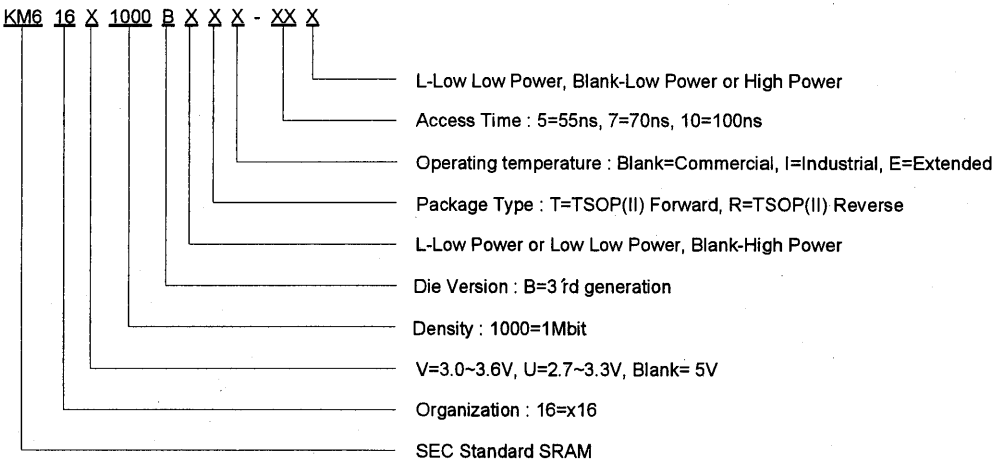
SAMSUNG ELECTRONICS

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Industrial Temp Products (-40~85℃)	
Part Name	**Function**	**Part Name**	**Function**
KM6161000BLT-5	44-TSOP(II), F, 5V, 55ns, L-pwr	KM6161000BLTI-5	44-TSOP(II), F, 5V, 70ns, L-pwr
KM6161000BLT-5L	44-TSOP(II), F, 5V, 55ns, LL-pwr	KM6161000BLTI-5L	44-TSOP(II), F, 5V, 70ns, LL-pwr
KM6161000BLT-7	44-TSOP(II), F, 5V, 70ns, L-pwr	KM6161000BLTI-7	44-TSOP(II), F, 5V, 100ns, L-pwr
KM6161000BLT-7L	44-TSOP(II), F, 5V, 70ns, LL-pwr	KM6161000BLTI-7L	44-TSOP(II), F, 5V, 100ns, LL-pwr
KM6161000BLR-5	44-TSOP(II), R, 5V, 55ns, L-pwr	KM6161000BLRI-5	44-TSOP(II), R, 5V, 70ns, L-pwr
KM6161000BLR-5L	44-TSOP(II), R, 5V, 55ns, LL-pwr	KM6161000BLRI-5L	44-TSOP(II), R, 5V, 70ns, LL-pwr
KM6161000BLR-7	44-TSOP(II), R, 5V, 70ns, L-pwr	KM6161000BLRI-7	44-TSOP(II), R, 5V, 100ns, L-pwr
KM6161000BLR-7L	44-TSOP(II), R, 5V, 70ns, LL-pwr	KM6161000BLRI-7L	44-TSOP(II), R, 5V, 100ns, LL-pwr

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM6161000BLT/LT-L KM6161000BLR/LR-L
		-40 to 85	℃	KM6161000BLTI/LTI-L KM6161000BLRI/LRI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5	V
Input low voltage	V_{IL}	-0.5***	-	0.8	V

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** Ta=25℃
*** Vil(min)=-3.0V for ≤ 50ns pulse width

CAPACITANCE* (f=1MHz, TA=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}, $\overline{UB}$=V_{IH} or $\overline{LB}$=V_{IH}, V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current Average operatingcurrent		I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA	Read	-	-	10	mA
				Write	-	-	35	
		I_{CC1}	Cycle time=1μs 100% duty $\overline{CS}$≤0.2V, I_{IO}=0mA	Read	-	-	15	mA
				Write	-	-	40	
		I_{CC2}	Min cycle, 100% duty, $\overline{CS}$=V_{IL}, I_{IO}=0mA		-	-	120	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS}$=V_{IH}		-	-	3	mA
Standby Current (CMOS)	KM6161000BL/L-L	I_{SB1}	$\overline{CS}$≥Vcc-0.2V V_{IN}≥Vcc-0.2V or V_{IN}≤0.2V	L(Low Power)	-	-	100	μA
				LL(L Low Power)	-	-	20	
	KM6161000BLI/LI-L			L(Low Power)	-	-	100	μA
				LL(L Low Power)	-	-	50	

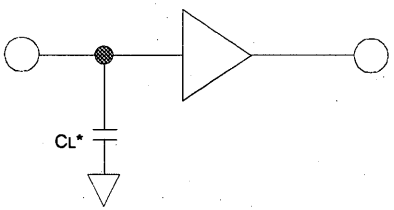
* 1) Commercial Product : T_A=0 to 70℃, Unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, Unless otherwise specified
** TA=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising and falingl time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL **C_L=30pF+1TTL	-

* See DC Operating conditions
** Test load for 55ns product



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM6161000BL/L-L	0~70℃	5.0V ± 10%	55*/70ns	Commercial
KM6161000BLI/LI-L	-40~85℃	5.0V ± 10%	70/100ns	Industrial

* The parameter is measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

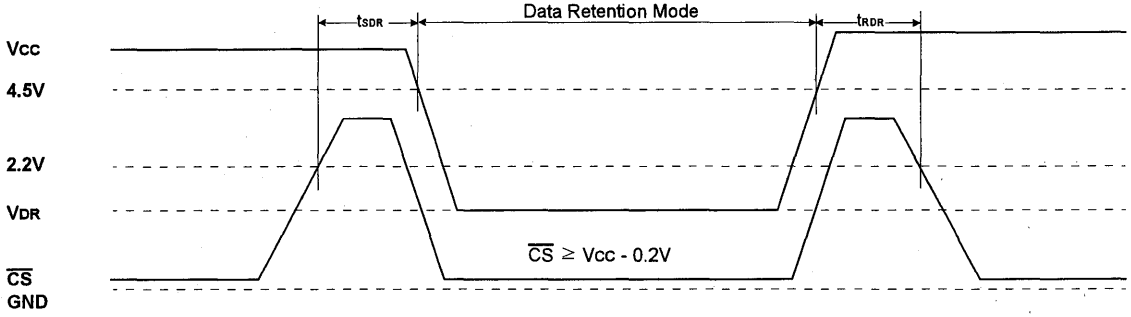
Parameter List		Symbol	Speed Bins						Units
			55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	$\overline{UB}$,$\overline{LB}$ Access Time	tBA	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	$\overline{UB}$,$\overline{LB}$ enable to low-Z output	tBLZ	5	-	5	-	5	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	0	30	ns
	$\overline{UB}$,$\overline{LB}$ disable to high-Z output	tBHZ	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	15	-	15	-	ns
Write	Write cycle time	tWC	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	70	-	ns
	$\overline{UB}$, $\overline{LB}$ valid to end of write	tBW	45	-	60	-	80	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	0	35	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS} \geq$ Vcc-0.2V		2.0	-	5.5	V
Data retention current	I_{DR}	KM6161000B Family	Vcc=3.0V $\overline{CS} \geq$ Vcc-0.2V	L-Ver LL-Ver	- -	- -	50 15	μA
		KM6161000BI Family		L-Ver LL-Ver	- -	- -	50 15	μA
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** Ta=25℃

DATA RETENTION TIMING DIAGRAM

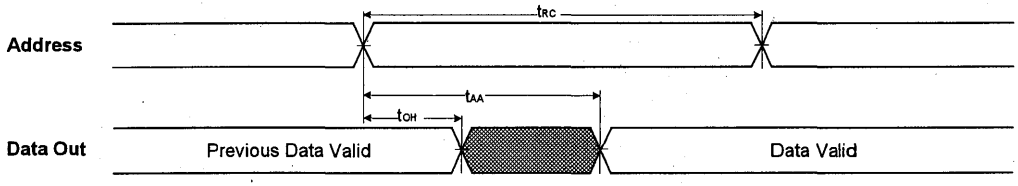


SAMSUNG ELECTRONICS

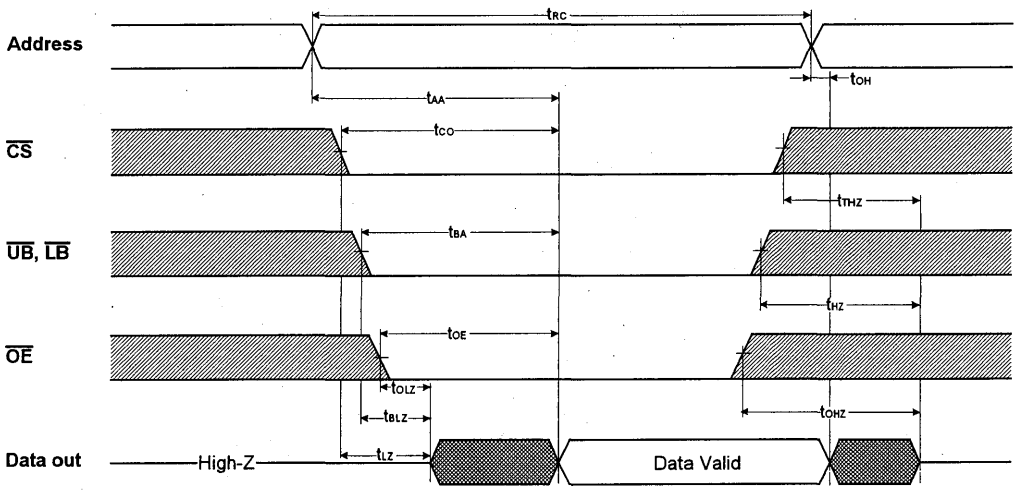
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$ or and $\overline{LB}$=V_{IL})



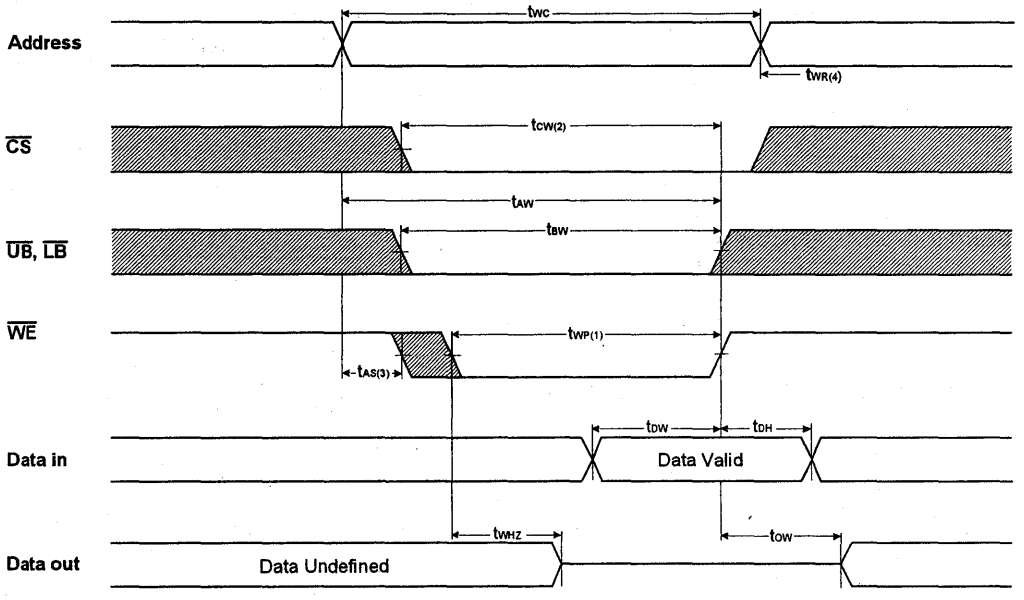
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



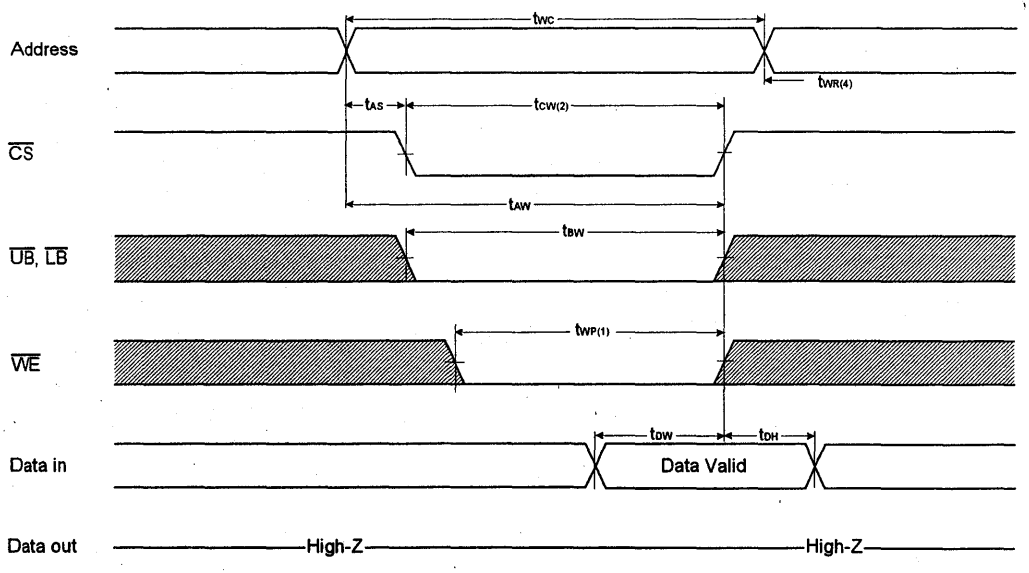
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.

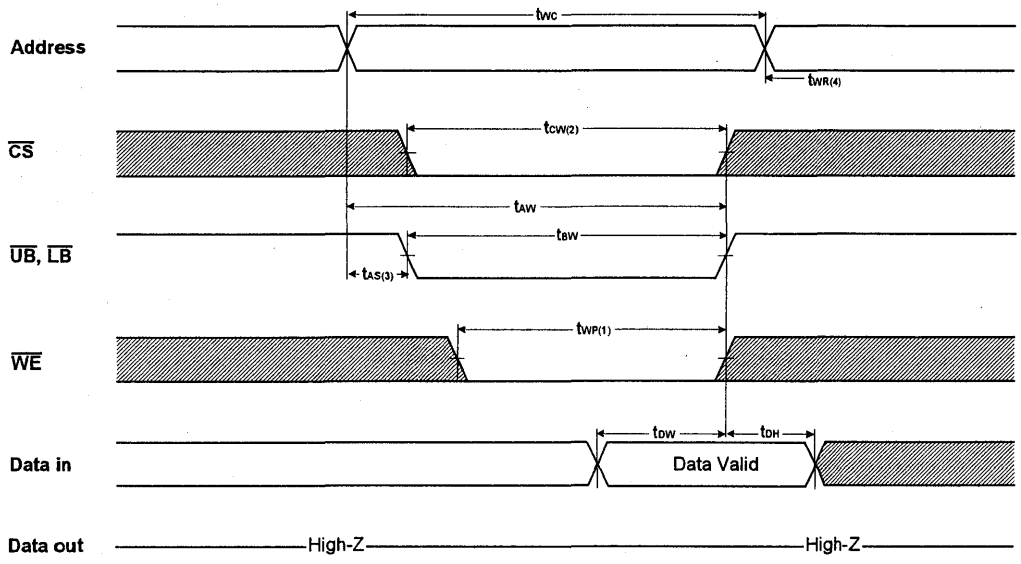
TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultenious asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{LB}$	$\overline{UB}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O1~8	I/O9~16	Current Mode
H	X	X	X	X	Not Select	High-Z	High-Z	I_{SB1}
L	X	X	H	H	Output Disable	High-Z	High-Z	Icc
L	H	H	X	X		High-Z	High-Z	
L	L H L	H L L	H	L	Read	Dout High-Z Dout	High-Z Dout Dout	Icc
L	L H L	H L L	L	X	Write	Din High-Z Din	High Din Din	Icc

* X means dont care (Must be in low or high state)

512Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.4㎛ CMOS
- Organization : 512Kx8
- Power Supply Voltage : Single 5V ± 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard 32-DIP, 32-SOP, 32-TSOP(II)-Forward/Reverse

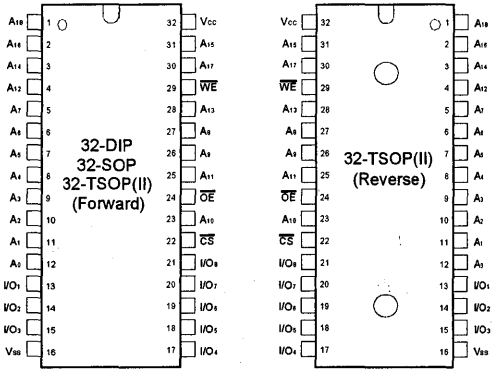
GENERAL DESCRIPTION

The KM684000A family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

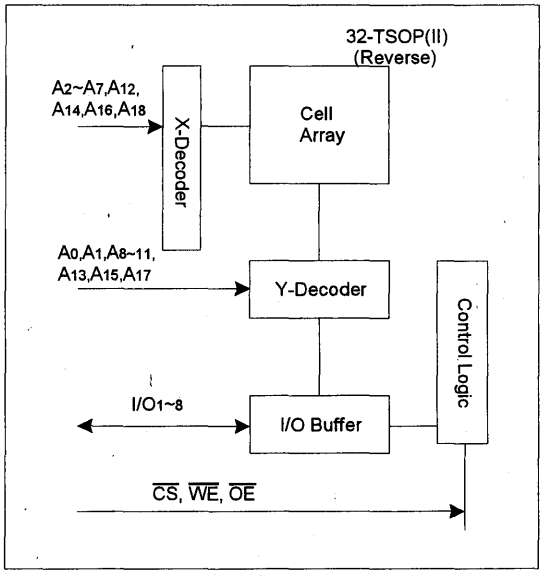
Product Family	Operating Temperature.	Vcc Range (V)	Speed (ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM684000AL KM684000AL-L	Commercial (0~70℃)	4.5~5.5V	55/70ns	100㎂ 20㎂	90mA	32-DIP,32SOP 32-TSOP(II)-R/F
KM684000ALI KM684000ALI-L	Industrial (-40~85℃)	4.5~5.5V	70/100ns	100㎂ 50㎂		32-SOP 32-TSOP(II)-R/F

PIN DESCRIPTION



Pin Name	Function
A0~A18	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power (5V)
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM



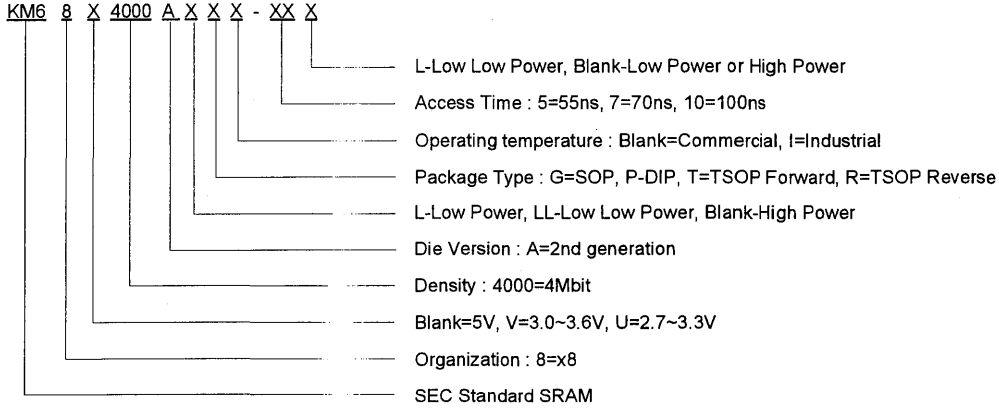
SAMSUNG ELECTRONICS

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Industrial Temp Products (-40~85℃)	
Part Name	**Function**	**Part Name**	**Function**
KM684000ALP-5	32-DIP, 55ns, L-pwr	KM684000ALGI-7	32-SOP,70ns, L-pwr
KM684000ALP-5L	32-DIP, 55ns, LL-pwr	KM684000ALGI-7L	32-SOP, 70ns, LL-pwr
KM684000ALP-7	32-DIP, 70ns, L-pwr	KM684000ALGI-10	32-SOP, 100ns, L-pwr
KM684000ALP-7L	32-DIP, 70ns, LL-pwr	KM684000ALGI-10L	32-SOP, 100ns, LL-pwr
KM684000ALG-5	32-SOP, 55ns, L-pwr	KM684000ALTI-7	32-TSOP(II)F, 70ns, L-pwr
KM684000ALG-5L	32-SOP, 55ns, LL-pwr	KM684000ALTI-7L	32T-SOP(II)F, 70ns, LL-pwr
KM684000ALG-7	32-SOP, 70ns, L-pwr	KM684000ALTI-10	32-TSOP(II)F, 100ns, L-pwr
KM684000ALG-7L	32-SOP, 70ns, LL-pwr	KM684000ALTI-10L	32-TSOP(II)F, 100ns, LL-pwr
KM684000ALT-5	32-TSOP(II)F, 55ns, L-pwr	KM684000ALRI-7	32-TSOP(II)R, 70ns, L-pwr
KM684000ALT-5L	32-TSOP(II)F, 55ns, LL-pwr	KM684000ALRI-7L	32T-SOP(II)R, 70ns, LL-pwr
KM684000ALT-7	32-TSOP(II)F, 70ns, L-pwr	KM684000ALRI-10	32-TSOP(II)R, 100ns, L-pwr
KM684000ALT-7L	32-TSOP(II)F, 70ns, LL-pwr	KM684000ALRI-10L	32-TSOP(II)R, 100ns, LL-pwr
KM684000ALR-5	32-TSOP(II)R, 55ns, L-pwr		
KM684000ALR-5L	32-TSOP(II)R, 55ns, LL-pwr		
KM684000ALR-7	32-TSOP(II)R, 70ns, L-pwr		
KM684000ALR-7L	32-TSOP(II)R, 70ns, LL-pwr		

ORDERING INFORMATION



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM684000AL/L-L
		-40 to 85	℃	KM684000ALI/LI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5V	V
Input low voltage	V_{IL}	-0.5***	-	0.8	V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 50ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

* Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, I_{IO}=0mA	Read	-	-	15	mA
				Write	-	-	35	
Average operating current		I_{CC1}	Cycle time=1μs 100% duty I_{IO}=0mA $\overline{CS}$≤0.2V, V_{IL}≤0.2V V_{IH}≥Vcc-0.2V	Read	-	-	15	mA
				Write	-	-	35	
		I_{CC2}	Min cycle, 100% duty $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, I_{IO}=0mA		-	-	90	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS}$=V_{IH}		-	-	3	mA
Standby Current (CMOS)	KM684000AL/L-L	I_{SB1}	$\overline{CS}$≥Vcc-0.2V Others=0~Vcc	Low Power	-	-	100	μA
				Low Low Power	-	-	20	μA
	KM684000ALI/L-L			Low Power	-	-	100	μA
				Low Low Power	-	-	50	μA

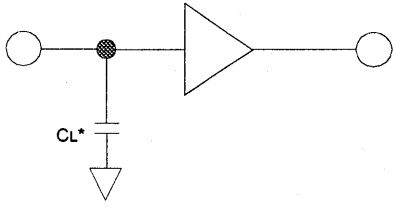
* 1) Commercial Product : T_A=0 to 70℃, Vcc=5V±10% unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, Vcc=5V±10% unless otherwise specified
** T_A=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	*C_L=100pF+1TLL	-

* See DC Operating conditions



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM684000AL/L-L	0~70℃	5V ± 10%	55/70ns	Commercial
KM684000ALI/LI-L	-40~85℃	5V ± 10%	70/100ns	Industrial

PARAMETER LIST FOR EACH SPEED BIN

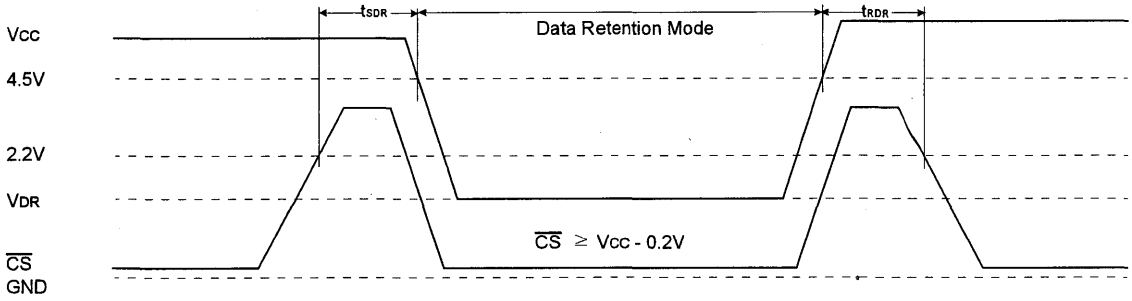
Parameter List		Symbol	Speed Bins						Units
			55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS} \geq V_{CC}-0.2V$		2.0	-	5.5	V
Data retention current	I_{DR}	KM684000AL/L-L	Vcc=3.0V $\overline{CS} \geq V_{CC}-0.2V$	L-Ver	-	-	50	μA
				LL-Ver	-	-	15	
		KM684000ALI/LI-L		L-Ver	-	-	50	
				LL-Ver	-	-	20	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** T_A=25℃

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

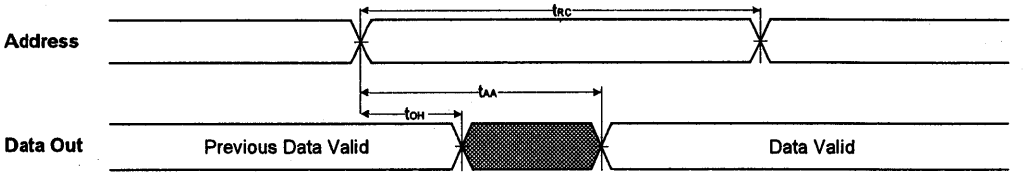
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	Icc
L	H	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

* X means don't care

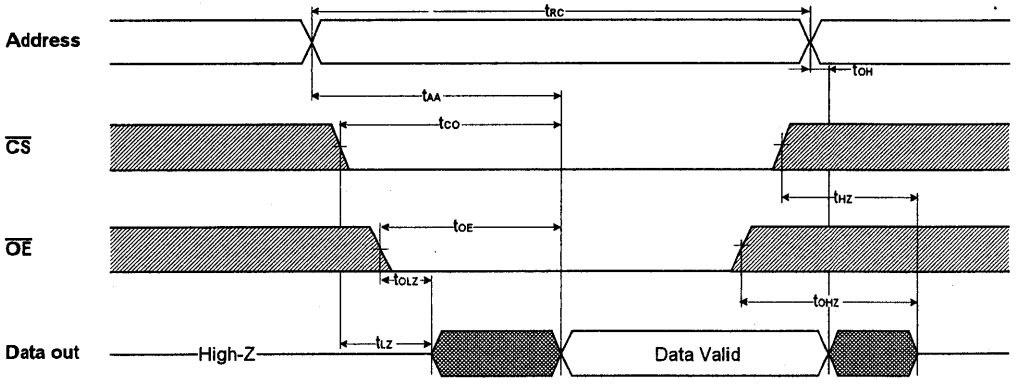
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

(CS=OE=V_{IL}, WE=V_{IH})



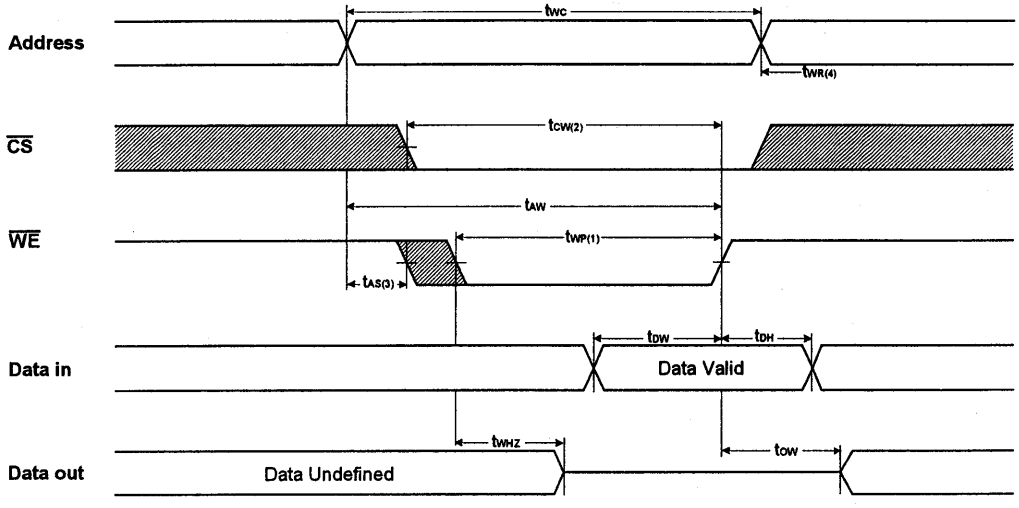
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



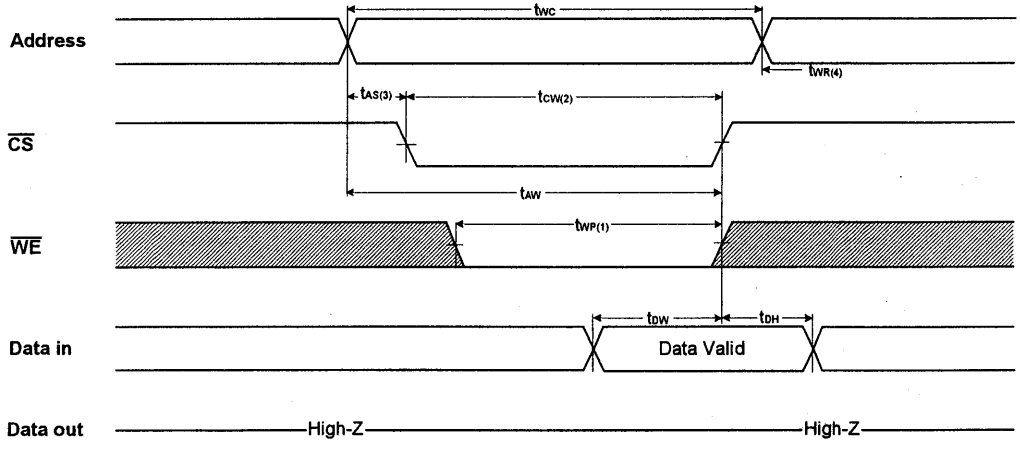
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.

512Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.4μm CMOS
- Organization : 512Kx8
- Power Supply Voltage : Single 5V $\pm$ 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard 32-DIP, 32-SOP, 32-TSOP(II)-Forward/Reverse

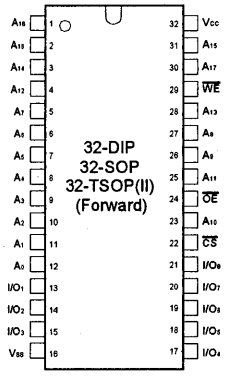
GENERAL DESCRIPTION

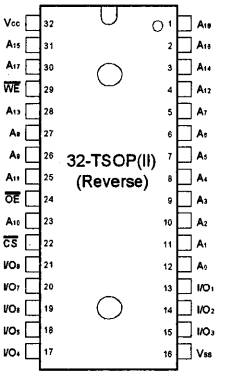
The KM684000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature.	Vcc Range (V)	Speed (ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM684000BL KM684000BL-L	Commercial (0~70℃)	4.5~5.5V	55/70ns	100μA 20μA	90mA	32-DIP,32SOP 32-TSOP(II)-R/F
KM684000BLI KM684000BLI-L	Industrial (-40~85℃)	4.5~5.5V	70/100ns	100μA 50μA		32-SOP 32-TSOP(II)-R/F

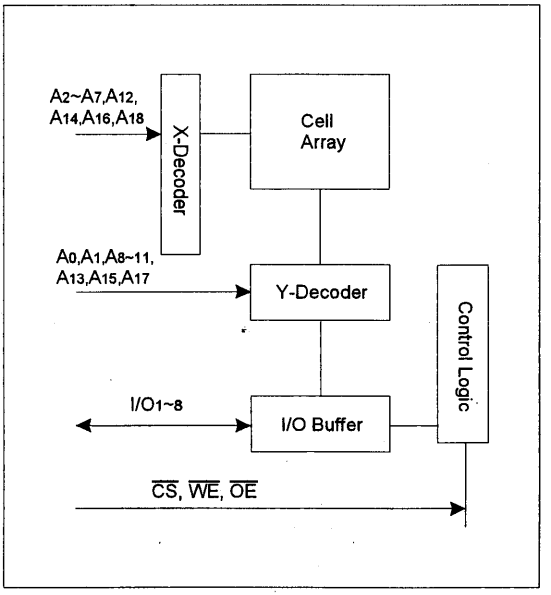
PIN DESCRIPTION





NameName	Function
A_0~A_{18}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1~I/O_8	Data Inputs/Outputs
Vcc	Power(5V)
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM



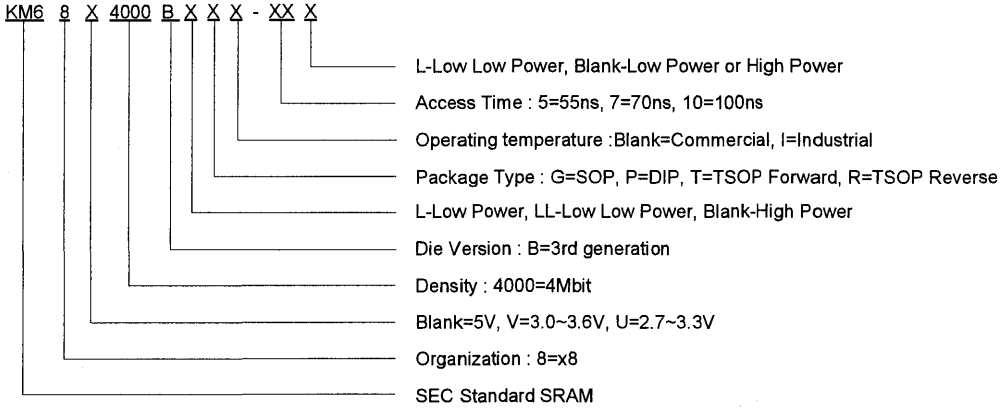
SAMSUNG ELECTRONICS

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Industrial Temp Products (-40~85℃)	
Part Name	**Function**	**Part Name**	**Function**
KM684000BLP-5	32-DIP, 55ns, L-pwr	KM684000BLGI-7	32-SOP,70ns, L-pwr
KM684000BLP-5L	32-DIP, 55ns, LL-pwr	KM684000BLGI-7L	32-SOP, 70ns, LL-pwr
KM684000BLP-7	32-DIP, 70ns, L-pwr	KM684000BLGI-10	32-SOP, 100ns, L-pwr
KM684000BLP-7L	32-DIP, 70ns, LL-pwr	KM684000BLGI-10L	32-SOP, 100ns, LL-pwr
KM684000BLG-5	32-SOP, 55ns, L-pwr	KM684000BLTI-7L	32-TSOP(II)F, 70ns, LL-pwr
KM684000BLG-5L	32-SOP, 55ns, LL-pwr	KM684000BLTI-10L	32-TSOP(II)F, 100ns, LL-pwr
KM684000BLG-7	32-SOP, 70ns, L-pwr	KM684000BLRI-7L	32-TSOP(II)R, 70ns, LL-pwr
KM684000BLG-7L	32-SOP, 70ns, LL-pwr	KM684000BLRI-10L	32-TSOP(II)R, 100ns, LL-pwr
KM684000BLT-5L	32-TSOP(II)F, 55ns, LL-pwr		
KM684000BLT-7L	32-TSOP(II)F, 70ns, LL-pwr		
KM684000BLR-5L	32-TSOP(II)R, 55ns, LL-pwr		
KM684000BLR-7L	32-TSOP(II)R, 70ns, LL-pwr		

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM684000BL/L-L
		-40 to 85	℃	KM684000BLI/LI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5V	V
Input low voltage	V_{IL}	-0.5***	-	0.8	V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 50ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, I_{IO}=0mA	Read	-	-	15	mA
				Write	-	-	45	
Average operating current		I_{CC1}	Cycle time=1μs 100% duty $\overline{CS}$≤0.2V, V_{IH}≤Vcc-0.2V,	Read	-	-	10	mA
				Write	-	-	45	
		I_{CC2}	Min cycle, 100% duty, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, I_{IO}=0mA		-	-	90	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS}$=V_{IH}		-	-	3	mA
Standby Current (CMOS)	KM684000BL/L-L	I_{SB1}	$\overline{CS}$≥Vcc-0.2V Others=0~Vcc	L(Low Power)	-	-	100	μA
				LL(L Low Power)	-	-	20	μA
	KM684000BLI/L-L			L(Low Power)	-	-	100	μA
				LL(L Low Power)	-	-	50	μA

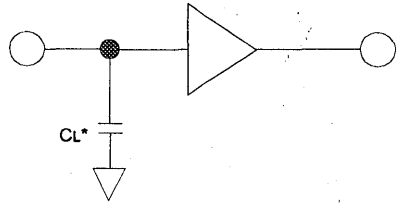
* 1) Commercial Product : T_A=0 to 70℃, Vcc=5V±10% unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, Vcc=5V±10% unless otherwise specified
** T_A=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising and falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL	-

* See DC Operating conditions



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM684000BL/L-L	0~70℃	5V ± 10%	55/70ns	Commercial
KM684000BLI/LI-L	-40~85℃	5V ± 10%	70/100ns	Industrial

PARAMETER LIST FOR EACH SPEED BIN

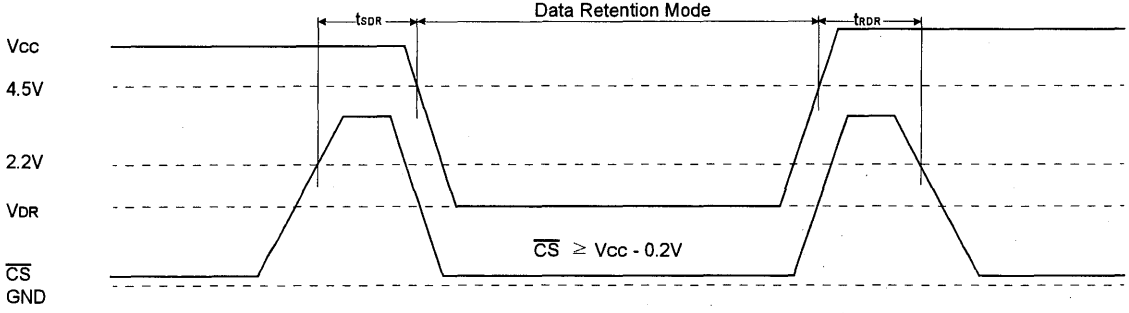
Parameter List		Symbol	Speed Bins						Units
			55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS} \geq$ Vcc-0.2V		2.0	-	5.5	V
Data retention current	I_{DR}	KM684000BL/L-L	Vcc=3.0V $\overline{CS} \geq$ Vcc-0.2V	L-Ver	-	-	50	μA
				LL-Ver	-	-	15	
		KM684000BLI/LI-L		L-Ver	-	-	50	
				LL-Ver	-	-	20	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70℃, Vcc=5V±10% unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, Vcc=5V±10% unless otherwise specified
** T_A=25℃

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

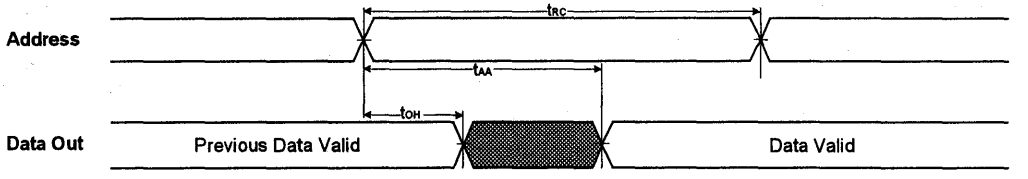
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	Icc
L	H	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

* X means don't care

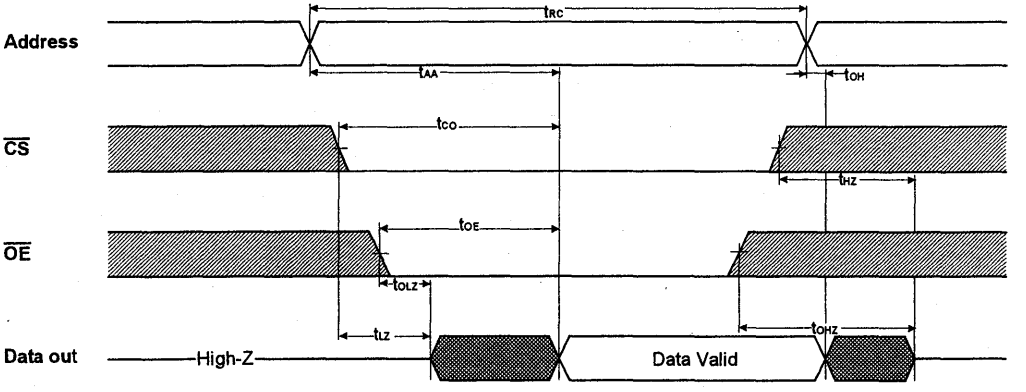
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



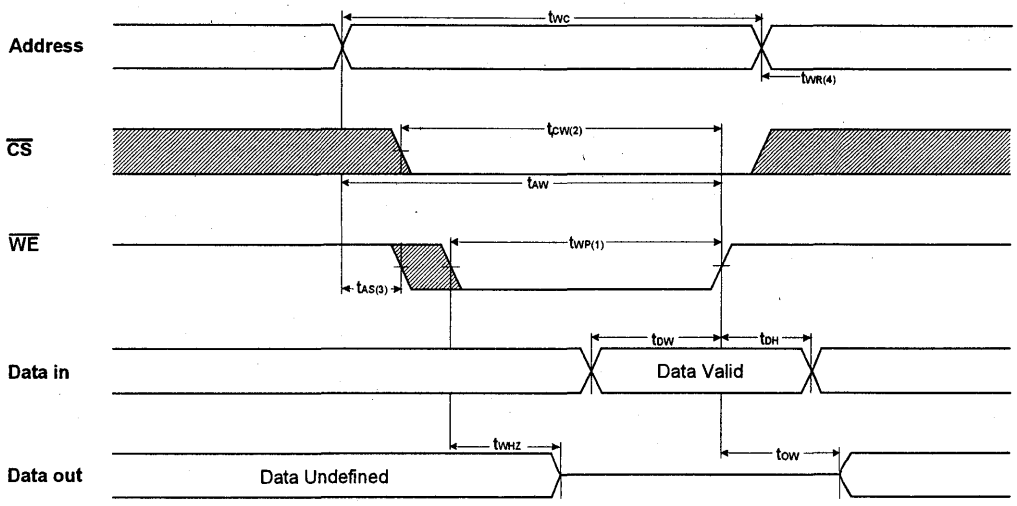
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



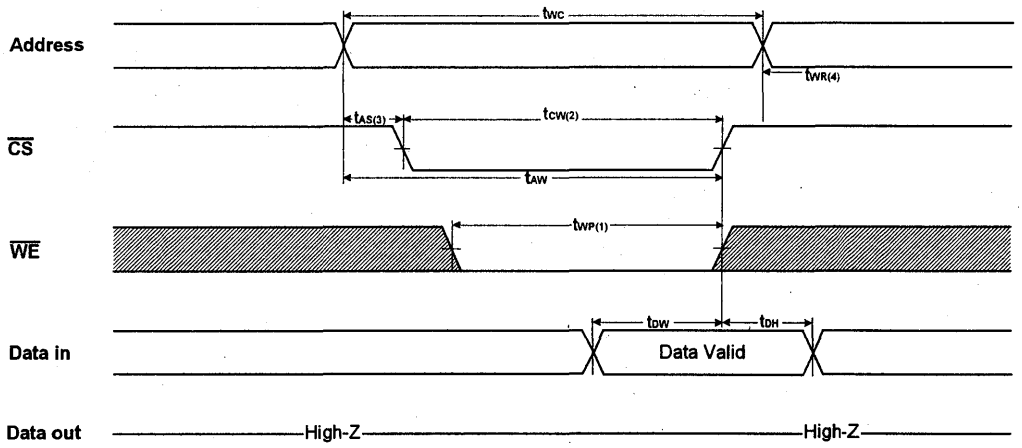
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.

256Kx16 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.4㎛ CMOS
- Organization : 256Kx16
- Power Supply Voltage : Single 5V ± 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  44-TSOP(II)-Forward/Reverse

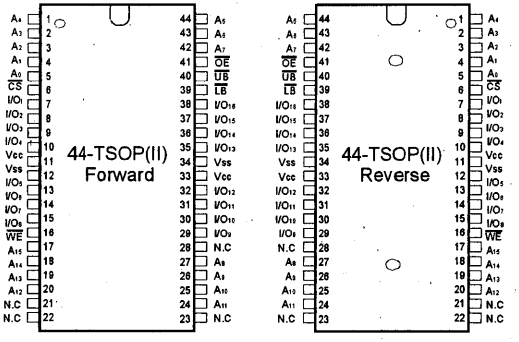
GENERAL DESCRIPTION

The KM616V4000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

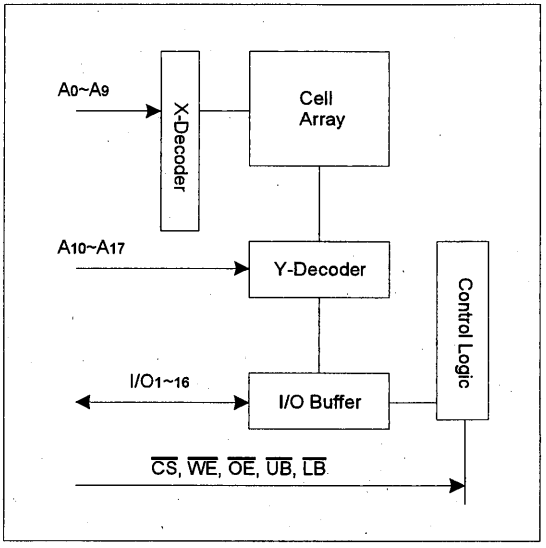
Product List	Operating Temp.	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM6164000BL-L	Commercial(0~70℃)	4.5~5.5V	55/70ns	20㎂	130mA	44-TSOP(II)-R/F
KM6164000BLI-L	Industrial(-40~85℃)	4.5~5.5V	70/100ns	50㎂		

PIN DESCRIPTION



Name	Function	Name	Function
A_0~A_{17}	Address Inputs	$\overline{LB}$	Lower Byte (I/O_1~$_8$)
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O_9~$_{16}$)
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
I/O_1~I/O_{16}	Data Inputs/Outputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

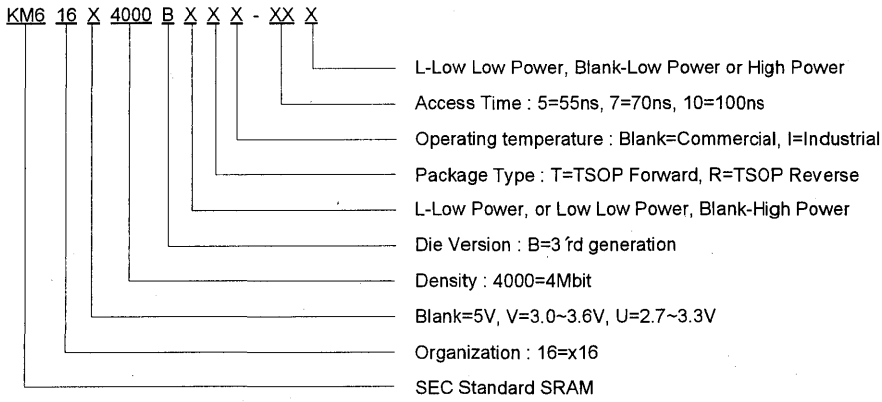
PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Industrial Temp Products (-40~85℃)	
Part Name	**Function**	**Part Name**	**Function**
KM6164000BLT-5L	44-TSOP(II)F, 55ns, LL-pwr	KM6164000BLTI-7L	44-TSOP(II)F, 70ns, LL-pwr
KM6164000BLT-7L	44-TSOP(II)F, 70ns, LL-pwr	KM6164000BLTI-10L	44-TSOP(II)F, 100ns, LL-pwr
KM6164000BLR-5L	44-TSOP(II)R, 55ns, LL-pwr	KM6164000BLRI-7L	44-TSOP(II)R, 70ns, .LL-pwr
KM6164000BLR-7L	44-TSOP(II)R, 70ns, LL-pwr	KM6164000BLRI-10L	44-TSOP(II)R, 100ns,LL-pwr

2

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM6164000BL-L
		-40 to 85	℃	KM6164000BLI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions forxtended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5	V
Input low voltage	V_{IL}	-0.5***	-	0.8	V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 50ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

* Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$ =V_{IH} or $\overline{WE}$ = V_{IL}		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, I_{IO}=0mA	Read	-	-	15	mA
				Write	-	-	75	
Average operatingcurrent		I_{CC1}	Cycle time=1μs 100% duty, I_{IO}=0mA $\overline{CS}$≤0.2V, V_{IH}≥Vcc-0.2V V_{IL}≤0.2V	Read	-	-	15	mA
				Write	-	-	75	
		I_{CC2}	Min cycle, 100%duty, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, V_{IO}=0mA		-	-	130	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current (TTL)		I_{SB}	$\overline{CS}$=V_{IH}		-	-	3	mA
Standby Current (CMOS)	KM6164000BL-L	I_{SB1}	$\overline{CS}$≥Vcc-0.2V Others inputs=0~Vcc	Low Low Power	-	-	20	μA
	KM6164000BLI-L			Low Low Power	-	-	50	μA

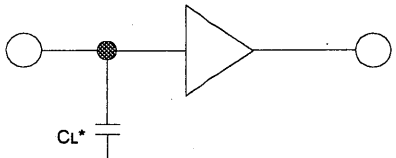
* 1) Commercial Product : T_A=0 to 70℃, Vcc=5V±10% unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, Vcc=5V±10% unless otherwise specified
** T_A=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising and falling time	5ns	-
Input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL	-

* See DC Operating conditions



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM6164000BL-L	0~70℃	5V ± 10%	55/70ns	Commercial
KM6164000BLI-L	-40~85℃	5V ± 10%	70/100ns	Industrial

* All parameters are measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	0	30	ns
	$\overline{OE}$ disable to high-Z output	tOHZ	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	10	-	ns
	$\overline{LB}$, $\overline{UB}$ valid to data output	tBA	-	25	-	35	-	50	ns
	$\overline{UB}$, $\overline{LB}$ disable to high-Z output	tBHZ	0	20	0	25	0	30	ns
Write	Write cycle time	tWC	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	600	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns
	$\overline{LB}$, $\overline{UB}$ valid to end of write	tBW	45	-	60	-	-	80	ns

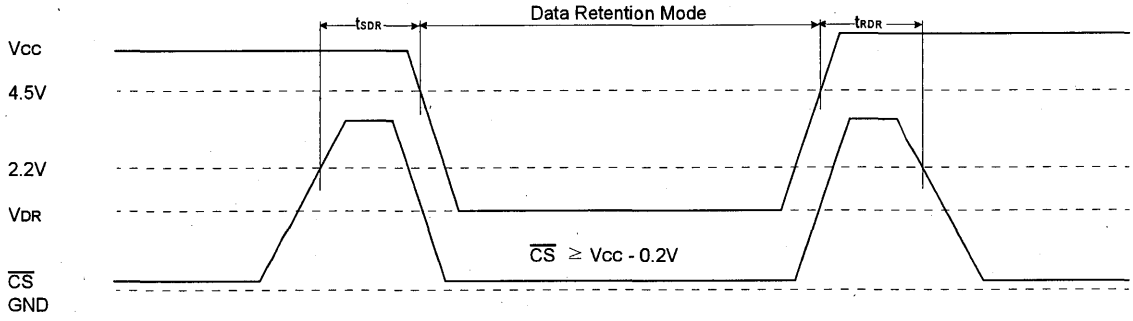
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS} \geq V_{CC}-0.2V$		2.0	-	5.5	V
Data retention current	I_{DR}	KM6164000BL-L	Vcc=3.0V $\overline{CS} \geq V_{CC}-0.2V$	LL-Ver	-	-	15	μA
		KM6164000BLI-L		LL-Ver	-	-	20	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** TA=25℃

2

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{LB}$	$\overline{UB}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O1~8	I/O9~16	Current Mode
H	X	X	X	X	Not Select	High-Z	High-Z	I_{SB1}
L	X	X	H	H	Output Disable	High-Z	High-Z	Icc
L	H	H	X	X		High-Z	High-Z	
L	L H L	H L L	H	L	Read	Dout High-Z Dout	High-Z Dout Dout	Icc
L	L H L	H L L	L	X	Write	Din High-Z Din	High-Z Din Din	Icc

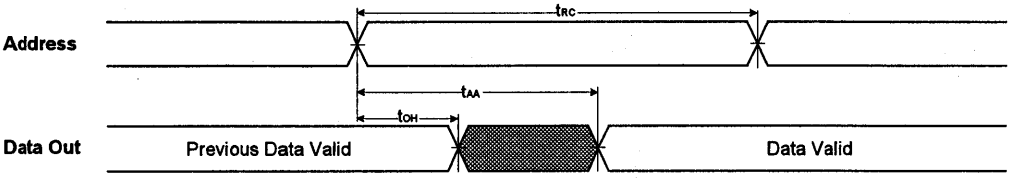
* X means don't care (Must be in low or high state)

SAMSUNG ELECTRONICS

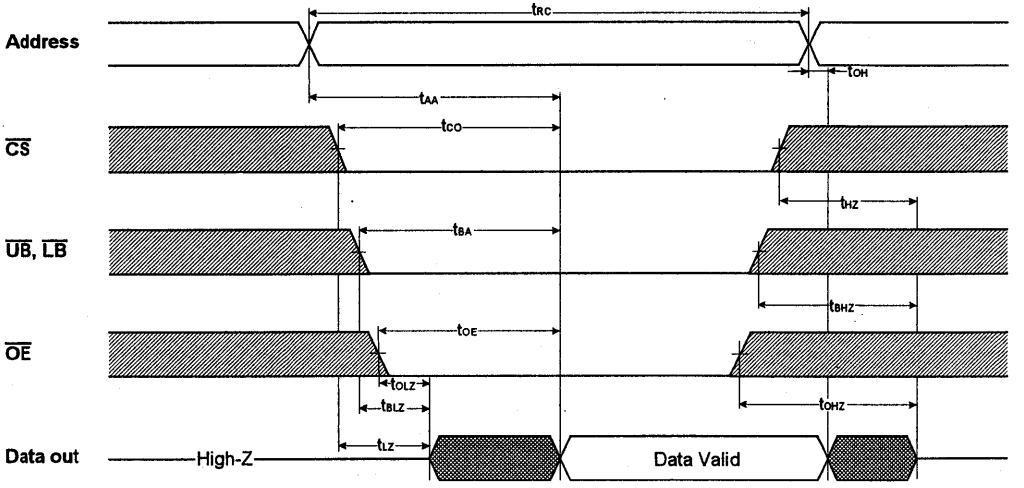
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$ or and $\overline{LB}$=V_{IL})



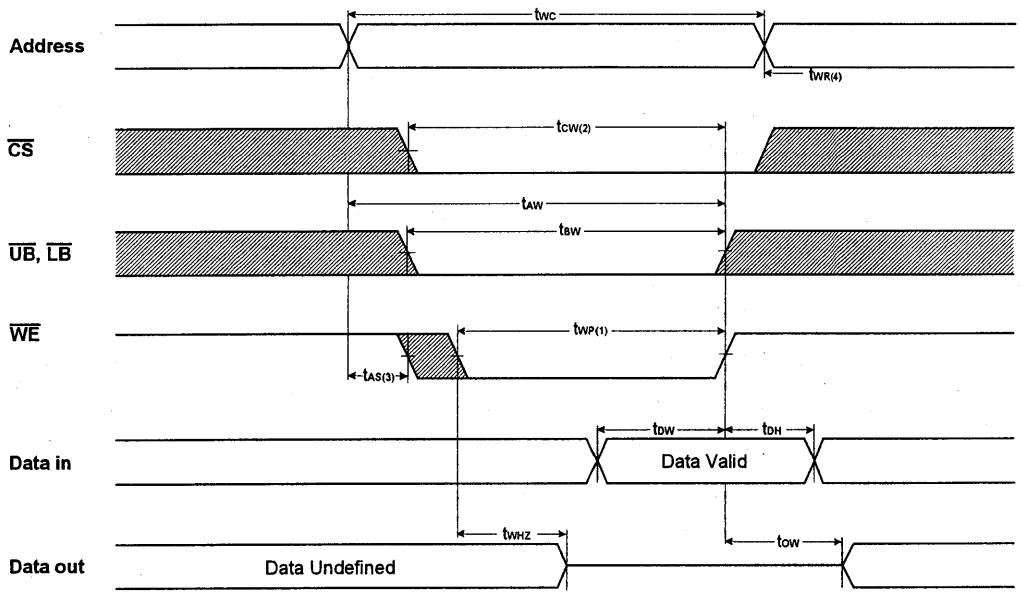
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



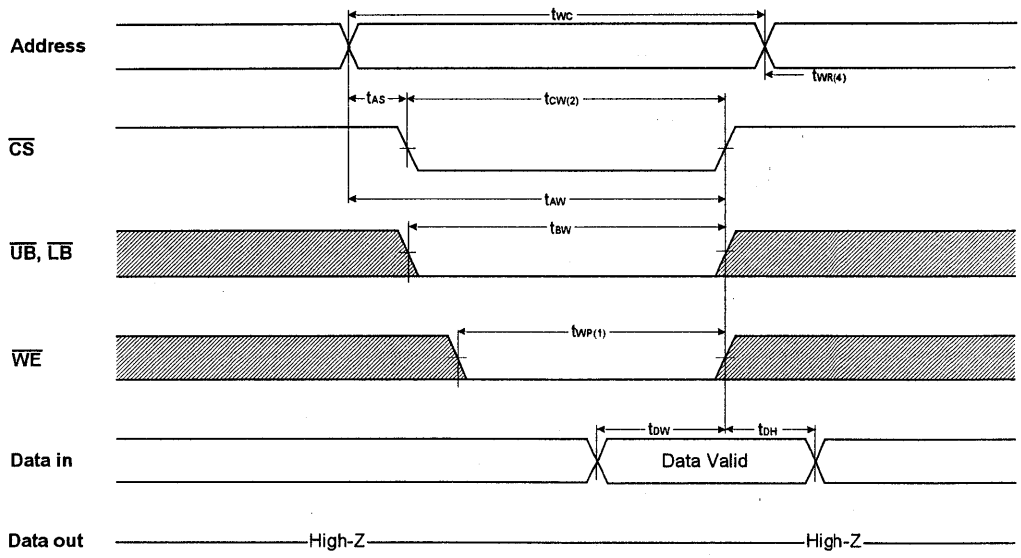
NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.

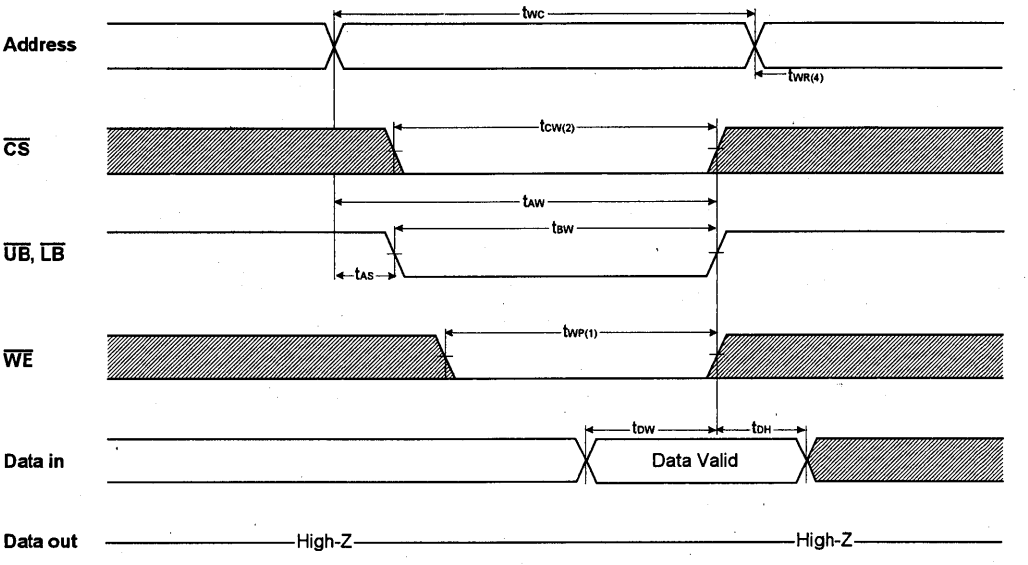
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneous asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

Low Power and Low Voltage SRAM (3.0V, 3.3V Operation)

32Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : 0.7㎛ CMOS
- Organization : 32Kx8
- Power Supply Voltage
  KM62V256C family : 3.3V ± 0.3V
  KM62U256C family : 3.0V ± 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  28-SOP, 28-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

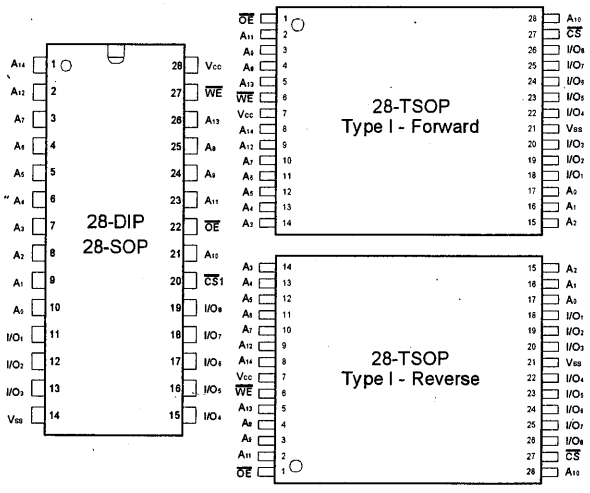
The KM62V256C and KM62U256C family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

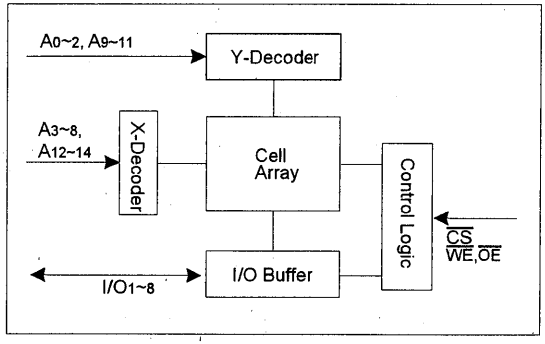
Product Family	Operating Temperature.	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM62V256CL-L	Commercial (0~70℃)	3.0 ~ 3.6V	70*/100ns	10㎂	35mA	28-SOP** 28-TSOP(I) R/F
KM62U256CL-L		2.7 ~ 3.3V	85*/100ns	10㎂		
KM62V256CLE-L	Extended (-25~85℃)	3.0 ~ 3.6V	70*/100ns	20㎂		28-SOP** 28-TSOP(I) R/F
KM62U256CLE-L		2.7 ~ 3.3V	85*/100ns	15㎂		
KM62V256CL-LI	Industrial (-40~85℃)	3.0 ~ 3.6V	70*/100ns	20㎂		28-SOP** 28-TSOP(I) R/F
KM62U256CLI-L		2.7 ~ 3.3V	85*/100ns	15㎂		

*The parameter is measured with 30pF test load.
**The deviced with 100ns SOP package in 3.0~3.6V Vcc range which is not produced.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



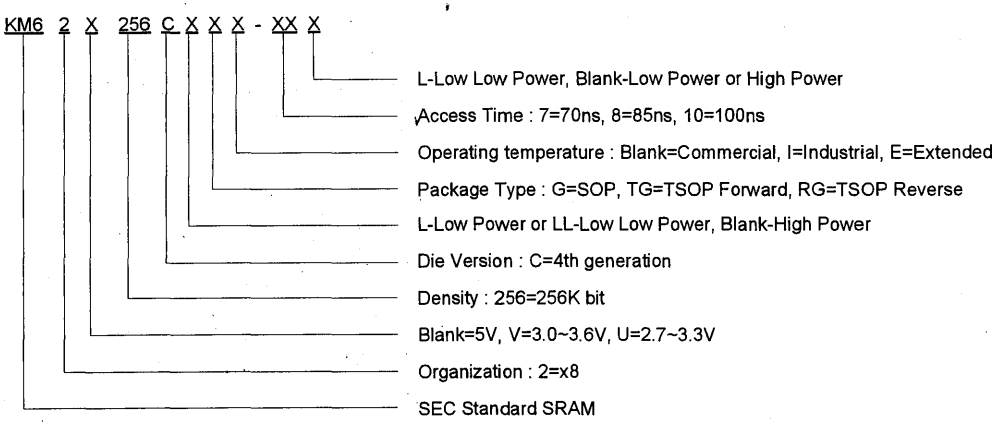
Pin Name	Function
A0~A14	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Extended Temp Products (-25~85℃)		Industrial Temp Products (-40~85℃)	
Part Name	Function	Part Name	Function	Part Name	Function
KM62V256CLG-7L	28-SOP, 70ns, 3.3V	KM62V256CLGE-7L	28-SOP, 70ns, 3.3V	KM62V256CLGI-7L	28-SOP, 70ns, 3.3V
KM62V256CLG-10L	28-SOP, 100ns, 3.3V	KM62V256CLGE-10L	28-SOP, 100ns, 3.3V	KM62V256CLGI-10L	28-SOP, 100ns, 3.3V
KM62V256CLTG-7L	28-TSOP F, 70ns, 3.3V	KM62V256CLTGE-7L	28-TSOP F, 70ns, 3.3V	KM62V256CLTGI-7L	28-TSOP F, 70ns, 3.3V
KM62V256CLTG-10L	28-TSOP F, 100ns, 3.3V	KM62V256CLTGE-10L	28-TSOP F, 100ns, 3.3V	KM62V256CLTGI-10L	28-TSOP F, 100ns, 3.3V
KM62V256CLRG-7L	28-TSOP R, 70ns, 3.3V	KM62V256CLRGE-7L	28-TSOP R, 70ns, 3.3V	KM62V256CLRGI-7L	28-TSOP R, 70ns, 3.3V
KM62V256CLRG-10L	28-TSOP R, 100ns, 3.3V	KM62V256CLRGE-10L	28-TSOP R, 100ns, 3.3V	KM62V256CLRGI-10L	28-TSOP R, 100ns, 3.3V
KM62U256CLG-8L	28-SOP, 85ns, 3.0V	KM62U256CLGE-8L	28-SOP, 85ns, 3.0V	KM62U256CLGI-8L	28-SOP, 85ns, 3.0V
KM62U256CLG-10L	28-SOP, 100ns, 3.0V	KM62U256CLGE-10L	28-SOP, 100ns, 3.0V	KM62U256CLGI-10L	28-SOP, 100ns, 3.0V
KM62U256CLTG-8L	28-TSOP F, 85ns, 3.0V	KM62U256CLTGE-8L	28-TSOP F, 85ns, 3.0V	KM62U256CLTGI-8L	28-TSOP F, 85ns, 3.0V
KM62U256CLTG-10L	28-TSOP F, 100ns, 3.0V	KM62U256CLTGE-10L	28-TSOP F, 100ns, 3.0V	KM62U256CLTGI-10L	28-TSOP F, 100ns, 3.0V
KM62U256CLRG-8L	28-TSOP R, 85ns, 3.0V	KM62U256CLRGE-8L	28-TSOP R, 85ns, 3.0V	KM62U256CLRGI-8L	28-TSOP R, 85ns, 3.0V
KM62U256CLRG-10L	28-TSOP R, 100ns, 3.0V	KM62U256CLRGE-10L	28-TSOP R, 100ns, 3.0V	KM62U256CLRGI-10L	28-TSOP R, 100ns, 3.0V

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OU}	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	0.7	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM62V256CL-L, KM62U256CL-L
		-25 to 85	℃	KM62V256CLE-L, KM62U256CLE-L
		-40 to 85	℃	KM62V256CLI-L, KM62U256CLI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM62V256C Family KM62U256C Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	Vss	All	0	0	0	V
Input high voltage	V_{IH}	KM62V256C Family KM62U256C Family	2.2 2.2	- -	Vcc+0.3V Vcc+0.3V	V
Input low voltage	V_{IL}	KM62V256C Family KM62U256C Family	-0.3 -0.3***	- -	0.4 0.4	V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Extended Product : T_A=-25 to 85℃, unless otherwise specified
3) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions[1]		Min	Typ[2]	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or V_{IL} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA		-	1.0	2.0	mA
Average operating current		I_{CC1}	Cycle time=1μs 100% duty $\overline{CS}$≤ 0.2V, V_{IL} ≤ -0.2V V_{IN} ≥ Vcc -0.2V, I_{IO}=0mA		-	2.5	5	mA
		I_{CC2}	Min cycle, 100% duty, $\overline{CS}$=V_{IL}, I_{IO}=0mA		-	20[3]	35[4]	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.2	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS}$=V_{IH}		-	-	0.3	mA
Standby Current (CMOS)	KM62V256CL-L	I_{SB1}	$\overline{CS}$ ≥ Vcc-2.0V V_{IN}≤ 2.0V or V_{IN} ≥ Vcc-2.0V	Low Low Power	-	1.5	10	μA
	KM62V256CLE-L			Low Low Power	-	1.5	20	μA
	KM62V256CLI-L			Low Low Power	-	1.5	20	μA
	KM62U256CL-L			Low Low Power	-	1.0	10	μA
	KM62U256CLE-L			Low Low Power	-	1.0	15	μA
	KM62U256CLI-L			Low Low Power	-	1.0	15	μA

1) - Commercial Product : T_A=0 to 70℃, Vcc=3.3±0.3V (62V256C Family), Vcc=3.0±0.3V (62U256C Family)
- Extended Product : T_A=-25 to 85℃, Vcc=3.3±0.3V (62V256CE Family), Vcc=3.0±0.3V (62U256CE Family)
- Industrial Product : T_A=-40 to 85℃, Vcc=3.3±0.3V (62V256CI Family), Vcc=3.0±0.3V (62U256CI Family)

2) T_A=25℃

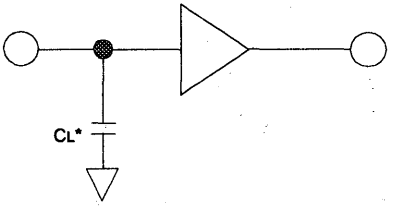
3) 25mA for KM62V256C Family

4) 30mA for KM62U256C Family but it is not 100% tested but obtained statistically

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rising & falling time	5ns	-
Input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL **C_L=30pF+1TTL	-



* Including scope and jig capacitance

* See DC Operating conditions
** KM62V256CL-7L Family, KM62U256CL-8L Family

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM62V256CL-L	0~70℃	3.3V ± 0.3	70*/100ns	Commercial
KM62V256CLE-L	-25~85℃	3.3V ± 0.3	70*/100ns	Extended
KM62V256CLI-L	-40~85℃	3.3V ± 0.3	70*/100ns	Industrial
KM62U256CL-L	0~70℃	3.0V ± 0.3	85*/100ns	Commercial
KM62U256CLE-L	-25~85℃	3.0V ± 0.3	85*/100ns	Extended
KM62U256CL-L	-40~85℃	3.0V ± 0.3	85*/100ns	Industrial

* The parameter is measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

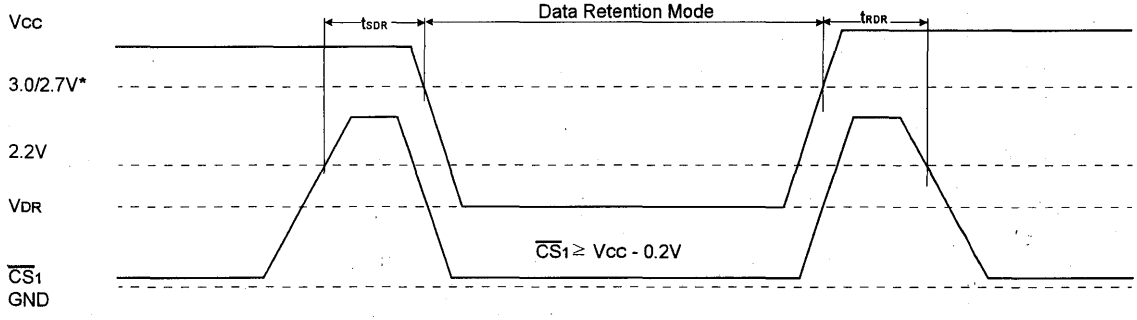
Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	30	0	30	0	35	ns
	Output disable to high-Z output	tOHZ	0	30	0	30	0	35	ns
	Output hold from address change	tOH	5	-	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	70	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	70	-	ns
	Write pulse width	tWP	50	-	60	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tDW	50	-	60	-	60	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	10	-	10	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*	Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS} \geq$ Vcc-0.2V	2.0	-	3.6	V
Data retention current	I_{DR}	KM62V256CL-L KM62U256CL-L	Vcc=3.0V $\overline{CS} \geq$ Vcc-0.2V	- -	1 0.6	8 8	µA
		KM62V256CLE-L KM62U256CLE-L		- -	1 0.6	10 10	
		KM62V256CLI-L KM62U256CLI-L		- -	1 0.6	10 10	
Data retention set-up time	t_{SDR}		See data retention waveform	0	-	-	ms
Recovery time	t_{RDR}			5	-	-	

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Extended Product : T_A=-25 to 85℃, nless otherwise specified
3) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** T_A=25℃

DATA RETENTION WAVE FORM



* 3.0V for KM62V256C Family, 2.7V for KM62U256C Family.

FUNCTIONAL DESCRIPTION

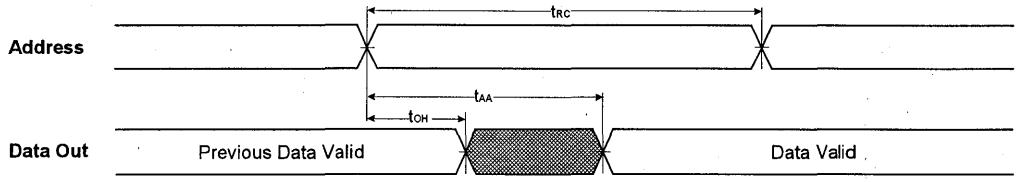
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	Dout	I_{CC}
L	L	X	Write	Din	I_{CC}

* X means don't care.

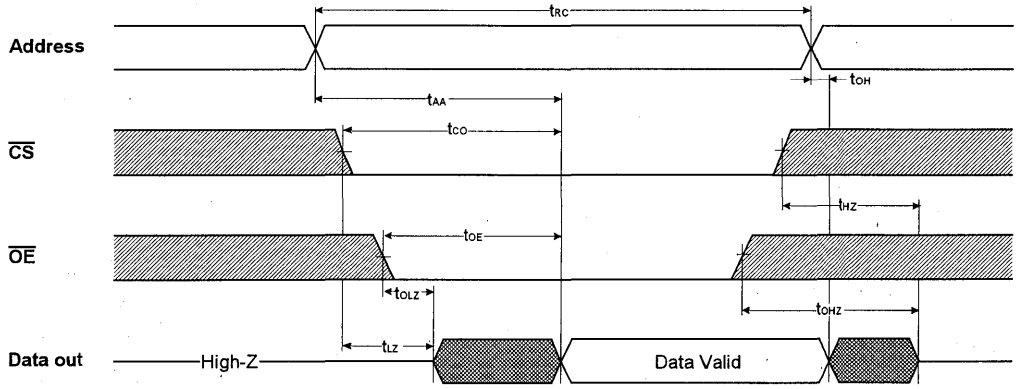
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



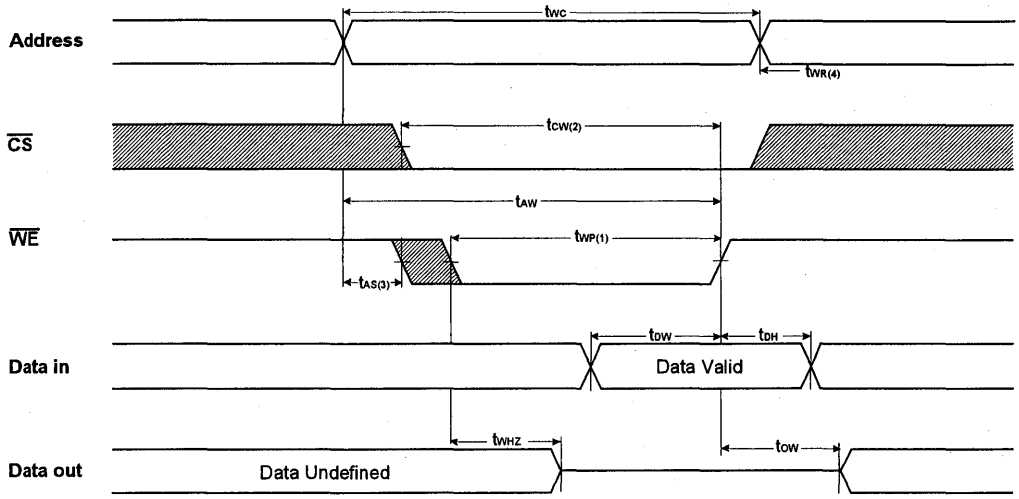
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



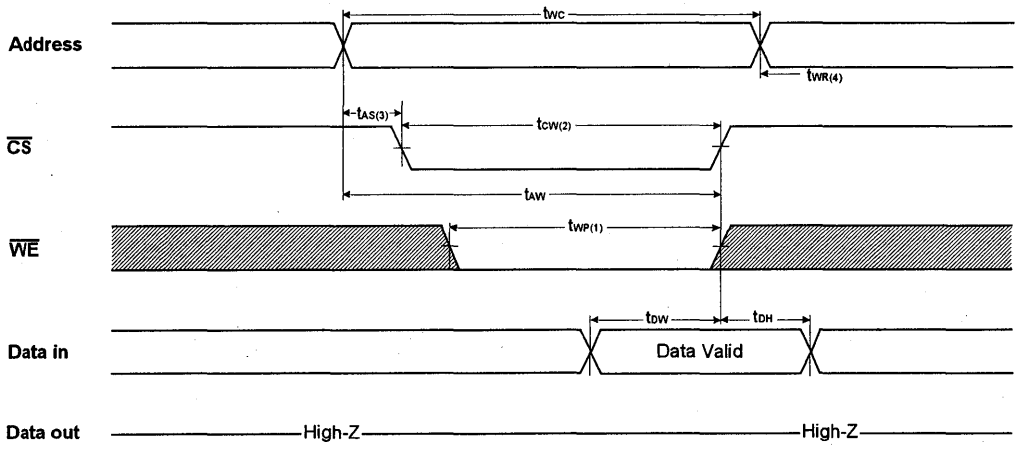
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

32Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : 0.4μm CMOS
- Organization : 32Kx8
- Power Supply Voltage
  KM62V256D family : 3.3V ± 0.3V
  KM62U256D family : 3.0V ± 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  28-SOP, 28-TSOP I -Forward/Reverse

GENERAL DESCRIPTION

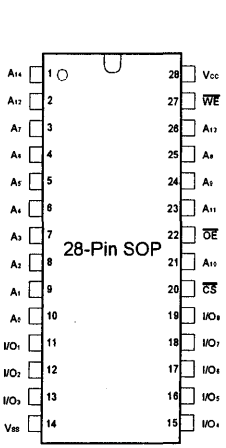
The KM62V256D and KM62U256D family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

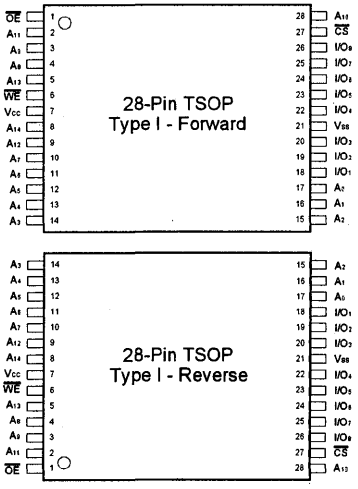
PRODUCT FAMILY

Product Family	Operating Temperature.	Vcc Range	Speed (ns)	PKG Type	Power Dissipation	
					Standby (I_{SB1}, Max)	Operating (I_{CC2})
KM62V256DL-L	Commercial (0~70℃)	3.0V ~3.6V	70*/100	28-SOP**	10μA	35mA
KM62U256DL-L		2.7V ~ 3.3V	85*/100	28-TSOP(I) R/F	10μA	
KM62V256DLE-L	Extended(-25~85℃)	3.0V ~3.6V	70*/100	28-SOP**	20μA	
KM62U256DLE-L		2.7V ~ 3.3V	85*/100	28-TSOP(I) R/F	15μA	
KM62V256DLI-L	Industrial (-40~85℃)	3.0V ~3.6V	70*/100	28-SOP**	20μA	
KM62U256DLI-L		2.7V ~ 3.3V	85*/100	28-TSOP(I) R/F	15μA	

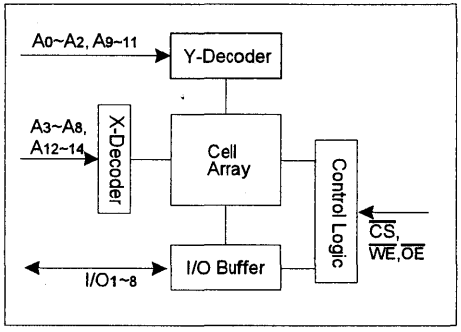
* The parameter is measured with 30pF test load.

PIN DESCRIPTION





FUNCTIONAL BLOCK DIAGRAM



Pin Name	Function
A_0~A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1~I/O_8	Data Inputs/Outputs
Vcc	Power
Vss	Ground

64Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : 0.6㎛ CMOS
- Organization : 64Kx8
- Power Supply Voltage
  KM68V512A family : 3.3V ± 0.3V
  KM68U512A family : 3.0V ± 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-SOP, 32-TSOP(I)-Forward, 32-sTSOP(I)-Forward

GENERAL DESCRIPTION

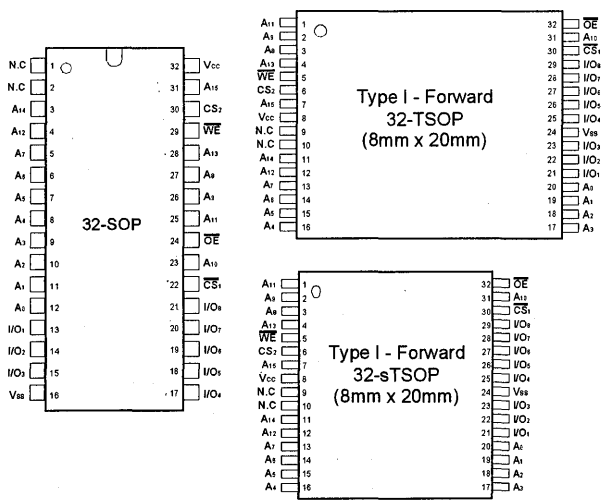
The KM68V512A and KM68U512A family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

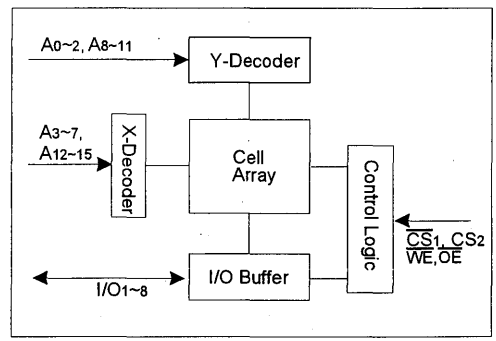
Product Family	Operating Temperature	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM68V512AL-L	Commercial (0~70℃)	3.0 ~ 3.6V	70*/85/100ns	10㎂	40mA	32-SOP 32-TSOP(I) F 32-sTSOP(I) F
KM68U512AL-L		2.7 ~ 3.3V	85*/100ns	10㎂		
KM68V512ALE-L	Extended (-25~85℃)	3.0 ~ 3.6V	70*/85/100ns	20㎂		
KM68U512ALE-L		2.7 ~ 3.3V	85*/100ns	15㎂		
KM68V512ALI-L	Industrial (-40~85℃)	3.0 ~ 3.6V	70*/85/100ns	20㎂		
KM68U512ALI-L		2.7 ~ 3.3V	85*/100ns	15㎂		

* The parameter is measured with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name Name	Function
A0~A15	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS_1}$, CS_2	Chip Select Inputs
$\overline{OE}$	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

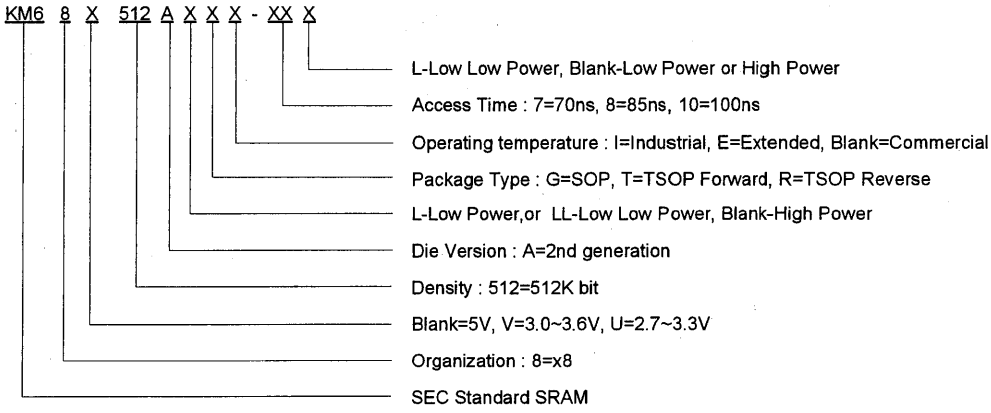
SAMSUNG ELECTRONICS

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Extended Temp Products (-25~85℃)		Industrial Temp Products (-40~85℃)	
Part Name	Function	Part Name	Function	Part Name	Function
KM68V512ALG-7L	32-SOP, 70ns, 3.3V, LL	KM68V512ALGE-7L	32-SOP, 70ns, 3.3V, LL	KM68V512ALGI-7L	32-SOP, 70ns, 3.3V, LL
KM68V512ALG-8L	32-SOP, 85ns, 3.3V, LL	KM68V512ALGE-8L	32-SOP, 85ns, 3.3V, LL	KM68V512ALGI-8L	32-SOP, 85ns, 3.3V, LL
KM68V512ALG-10L	32-SOP, 100ns, 3.3V, LL	KM68V512ALGE-10L	32-SOP, 100ns, 3.3V, LL	KM68V512ALGI-10L	32-SOP, 100ns, 3.3V, LL
KM68V512ALT-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V512ALTE-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V512ALTI-7L	32-TSOP F, 70ns, 3.3V, LL
KM68V512ALT-8L	32-TSOP F, 85ns, 3.3V, LL	KM68V512ALTE-8L	32-TSOP F, 85ns, 3.3V, LL	KM68V512ALTI-8L	32-TSOP F, 85ns, 3.3V, LL
KM68V512ALT-10L	32-TSOP F, 100ns, 3.3V,LL	KM68V512ALTE-10L	32-TSOP F, 100ns, 3.3V,LL	KM68V512ALTI-10L	32-TSOP F, 100ns, 3.3V,LL
KM68V512ALTG-7L	32-sTSOP F,70ns,3.3V,LL	KM68V512ALTGE-7L	32-sTSOP F,70ns,3.3V,LL	KM68V512ALTGI-7L	32-sTSOP F,70ns,3.3V,LL
KM68V512ALTG-8L	32-sTSOP F,85ns,3.3V,LL	KM68V512ALTGE-8L	32-sTSOP F,85ns,3.3V,LL	KM68V512ALTGI-8L	32-sTSOP F,85ns,3.3V,LL
KM68V512ALTG-10L	32-sTSOP F,100ns,3.3V,LL	KM68V512ALTGE-10L	32-sTSOP F,100ns,3.3V,LL	KM68V512ALTGI-10L	32-sTSOP F,100ns,3.3V,LL
KM68U512ALG-8L	32-SOP, 85ns, 3.0V, LL	KM68U512ALGE-8L	32-SOP, 85ns, 3.0V, LL	KM68U512ALGI-8L	32-SOP, 85ns, 3.0V, LL
KM68U512ALG-10L	32-SOP, 100ns, 3.0V, LL	KM68U512ALGE-10L	32-SOP, 100ns, 3.0V, LL	KM68U512ALGI-10L	32-SOP, 100ns, 3.0V, LL
KM68U512ALT-8L	32-TSOP F, 85ns, 3.0V, LL	KM68U512ALTE-8L	32-TSOP F, 85ns, 3.0V, LL	KM68U512ALTI-8L	32-TSOP F, 85ns, 3.0V, LL
KM68U512ALT-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U512ALTE-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U512ALTI-10L	32-TSOP F, 100ns, 3.0V, LL
KM68U512ALTG-8L	32-sTSOP F, 85ns, 3.0V, LL	KM68U512ALTGE-8L	32-sTSOP F, 85ns, 3.0V, LL	KM68U512ALTGI-8L	32-sTSOP F, 85ns, 3.0V, LL
KM68U512ALTG-10L	32-sTSOP F, 100ns,3.0V, LL	KM68U512ALTGE-10L	32-sTSOP F, 100ns,3.0V, LL	KM68U512ALTGI-10L	32-sTSOP F, 100ns,3.0V, LL

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	0.7	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM68V512AL-L, KM68U512AL-L
		-25 to 85	℃	KM68V512ALE-L, KM68U512ALE-L
		-40 to 85	℃	KM68V512ALI-L, KM68U512ALI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V512A Family KM68U512A Family	3.0 2.7	3.3 3.0	3.6 3.3	V V
Ground	Vss	All Family	0	0	0	V
Input high voltage	V_{IH}	KM68V512A Family KM68U512A Family	2.2 2.2	- -	Vcc+0.3V Vcc+0.3V	V V
Input low voltage	V_{IL}	KM68V512A Family KM68U512A Family	-0.3*** -0.3***	- -	0.4 0.4	V V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Extended Product : T_A=-25 to 85℃, unless otherwise specified
3) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

* Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

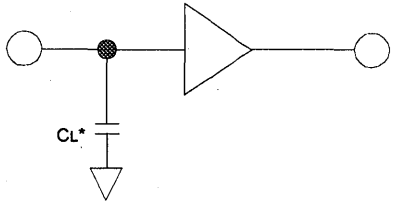
Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA		-	-	5	mA
Average operating current		I_{CC1}	Cycle time=1μs 100% duty, I_{IO}=0mA $\overline{CS_1}$≤ 0.2V, CS_2≥Vcc-0.2V		-	-	5	mA
		I_{CC2}	Min cycle, 100% duty, I_{IO}=0mA $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}		-	-	40	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL}		-	-	0.3	mA
Standby Current(CMOS)	KM68V512AL-L	I_{SB1}	$\overline{CS_1}$ ≥Vcc-0.2V CS_2 ≥Vcc-0.2V or CS_2 ≤0.2V Other input = 0~Vcc	L(Low Power)	-	-	10	μA
	KM68V512ALE-L KM68V512ALI-L			LL(L Low Power)	-	-	20	μA
	KM68V512AL-L			L(Low Power)	-	-	10	μA
	KM68V512ALE-L KM68V512ALI-L			LL(L Low Power)	-	-	15	μA

* 1) Commercial Product : T_A=0 to 70℃, Vcc=3.3V±0.3V(68V512A Family), Vcc=3.0V±0.3V(68U512A Family).
2) Extendedl Product : T_A=-25 to 85℃, Vcc=3.3V±0.3V(68V512AE Family), Vcc=3.0V±0.3V(68U512AE Family).
3) Industrial Product : T_A=-40 to 85℃, Vcc=3.3V±0.3V(68V512AI Family), Vcc=3.0V±0.3V(68U512AI Family).
** T_A=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTLL **C_L=30pF+1TTLL	-



* Including scope and jig capacitance

* See DC Operating conditions
** KM68V512AL-7L Family, KM68U512AL-8L Family

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V512AL-L	0~70℃	3.3V ± 0.3	70*/85/100ns	Commercial
KM68V512ALE-L	-25~85℃	3.3V ± 0.3	70*/85/100ns	Extended
KM68V512ALII-L	-40~85℃	3.3V ± 0.3	70*/85/100ns	Industrial
KM68U512AL-L	0~70℃	3.0V ± 0.3	85*/100ns	Commercial
KM68U512ALE-L	-25~85℃	3.0V ± 0.3	85*/100ns	Extended
KM68U512AL-L	-40~85℃	3.0V ± 0.3	85*/100ns	Industrial

* The parameter is measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			*70ns		**85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	45	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	30	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	20	0	20	ns
	Output hold from address change	tOH	10	-	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	0	35	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

* The parameter is measured with 30pF test load for KM68V512AL-7L Family.
** The parameter is measured with 30pF test load for KM68U512AL-8L Family.

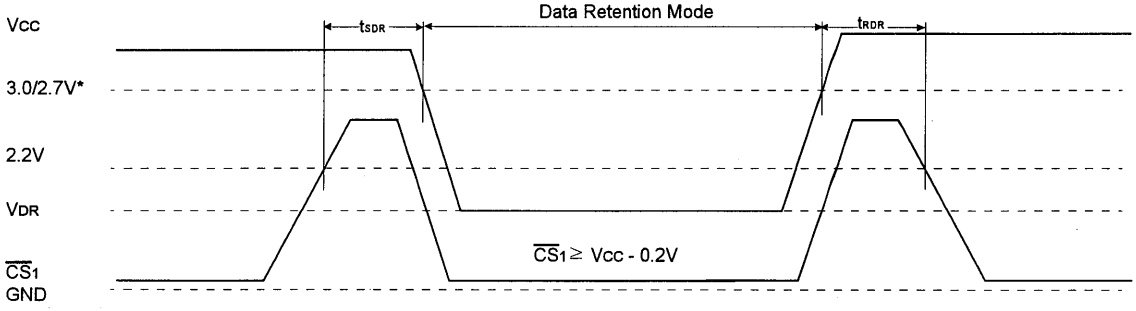
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS_1}$***≥Vcc-2.0V		2.0	-	3.6	V
Data retention current	I_{DR}	KM68V512AL-L	Vcc=3.0V $\overline{CS_1}$≥Vcc-0.2V	LL-Ver	-	-	10	µA
		KM68V512ALE-L		LL-Ver	-	-	15	
		KM68V512ALI-L		LL-Ver	-	-	15	
		KM68U512AL-L		LL-Ver	-	-	8	
		KM68U512ALE-L		LL-Ver	-	-	10	
		KM68U512ALI-L		LL-Ver	-	-	10	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

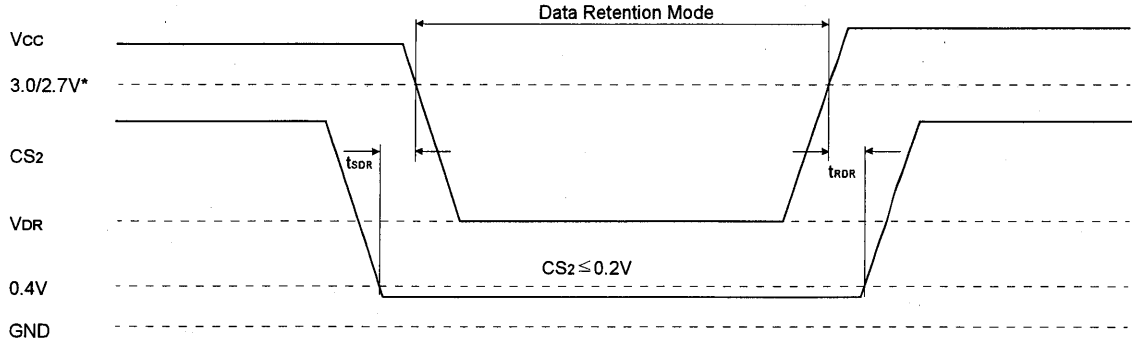
* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Extended Product : TA=-25 to 85℃, nless otherwise specified
3) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** TA=25℃
*** $\overline{CS_1}$ ≥Vcc-0.2V, CS_2 ≥Vcc-0.2V($\overline{CS_1}$ controlled) or CS_2 ≤0.2V(CS_2 controlled)

DATA RETENTION WAVE FORM

1) $\overline{CS_1}$ Controlled



2) CS_2 Controlled

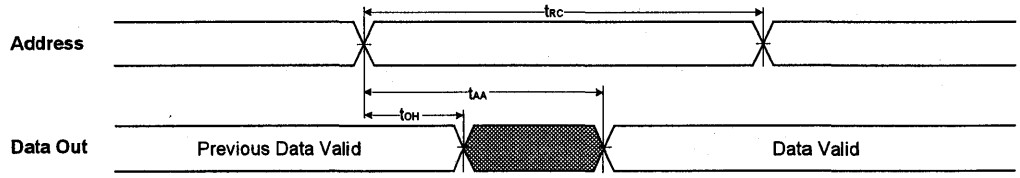


*3.0V for KM68V512A Family, 2.7V for KM68U512A Family

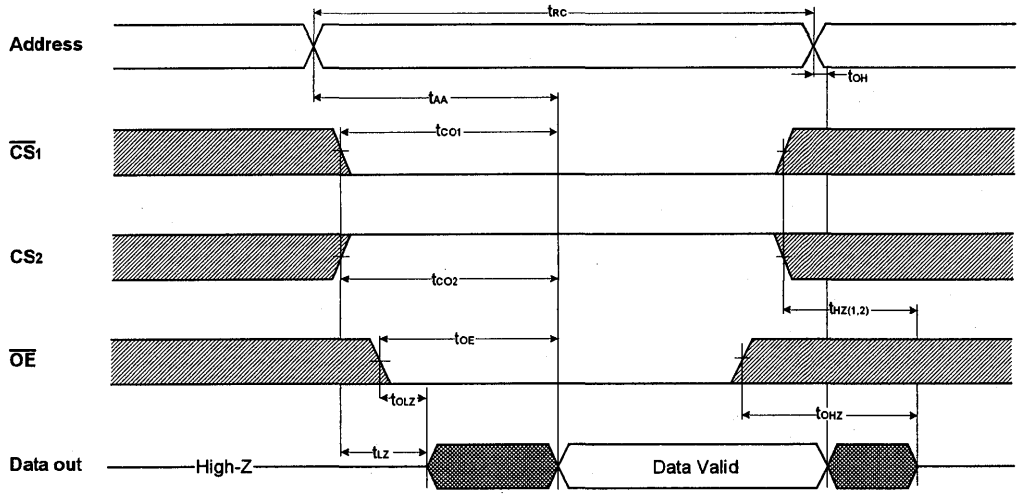
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, CS_2= $\overline{WE}$=V_{IH})



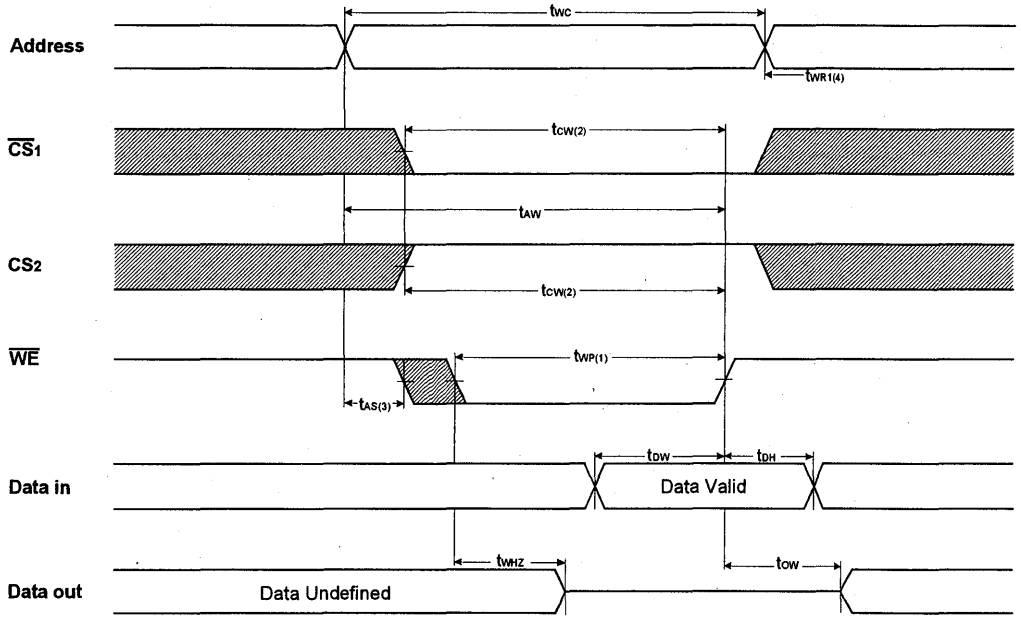
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



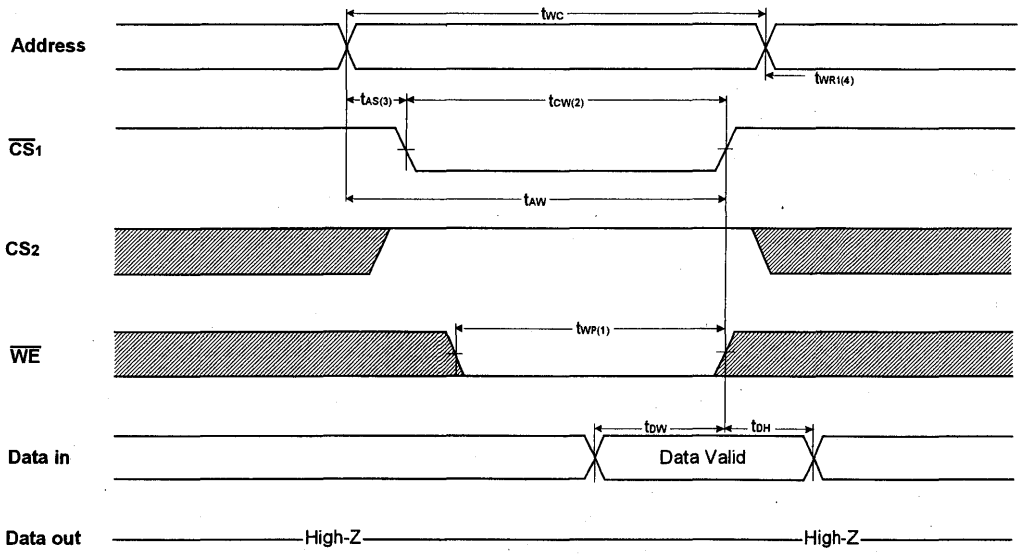
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device interconnection.

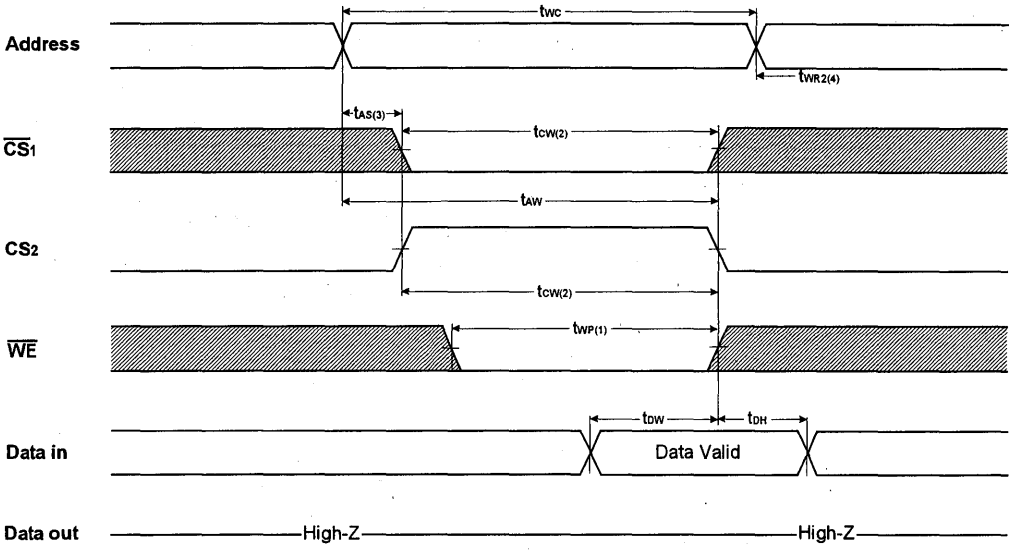
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}_2$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}_1$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}_1$ goes low, CS_2 going high and $\overline{WE}$ going low : A write ends at the earliest transition among $\overline{CS}_1$ going high, CS_2 going low and $\overline{WE}$ going high, tWP is measured from the begining of write to the end of write.
2. tCW is measured from the $\overline{CS}_1$ going low or CS_2 going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends as $\overline{CS}_1$ or $\overline{WE}$ going high tWR2 applied in case a write ends as CS_2 going to low.

FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	Isb, Isb1
X	L	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	H	Output Disable	High-Z	Icc
L	H	H	L	Read	Dout	Icc
L	H	L	X	Write	Din	Icc

* X means don't care(Must be in high or low)

128K x8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : 0.6μm CMOS
- Organization : 128K x8
- Power Supply Voltage
  KM68V1000B family : 3.3V±0.3V
  KM68U1000B family : 3.0V±0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-SOP, 32-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

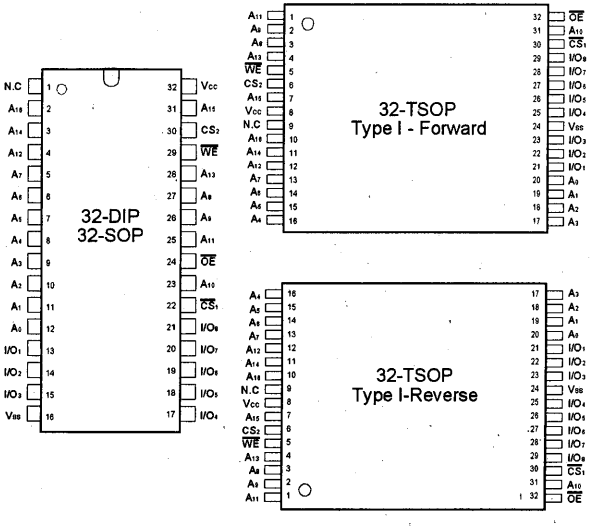
The KM68V1000B and KM68U1000B family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

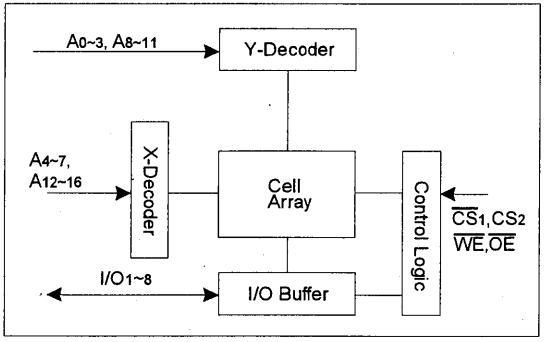
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM68V1000BL/L-L	Commercial(0~70℃)	3.0~3.6V	70*/100	50/15μA	40mA	32-SOP 32-TSOP(I) R/F
KM68U1000BL/L-L		2.7~3.3V	100	50/15μA		
KM68V1000BEL/LE-L	Extended(-25~85℃)	3.0~3.6V	70*/100	100/20μA		
KM68U1000BEL/LE-L		2.7~3.3V	100	50/15μA		
KM68V1000BLI/LI-L	Industrial(-40~85℃)	3.0~3.6V	70*/100	100/20μA		
KM68U1000BLI/LI-L		2.7~3.3V	100	50/15μA		

*The parameter is measured with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



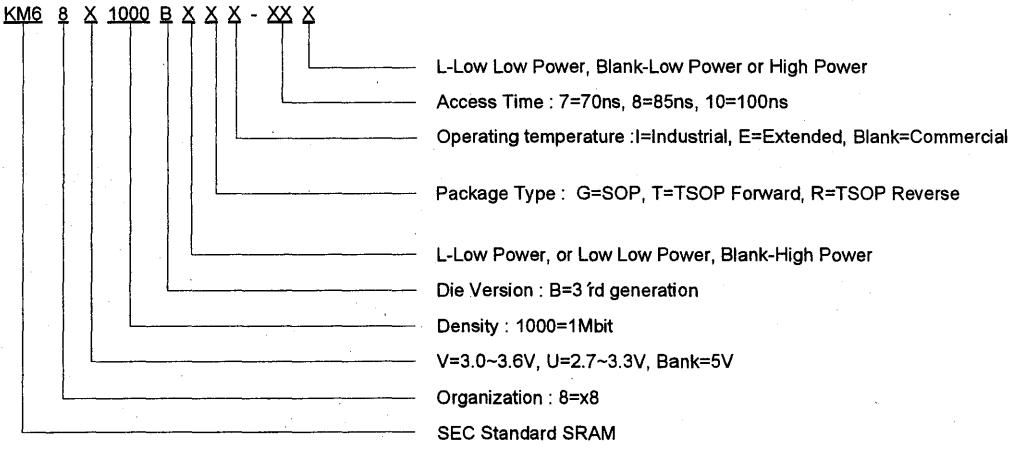
Name	Function
A0~A16	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$,CS2	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Industrial Temp Products (-25~85℃)		Industrial Temp Products (-40~85℃)	
Part Name	Function	Part Name	Function	Part Name	Function
KM68V1000BLG-7	32-SOP,70ns,3.3V,L	KM68V1000BLGE-7	32-SOP,70ns,3.3V,L	KM68V1000BLGI-7	32-SOP,70ns,3.3V,L
KM68V1000BLG-7L	32-SOP,70ns,3.3V,LL	KM68V1000BLGE-7L	32-SOP,70ns,3.3V,LL	KM68V1000BLGI-7L	32-SOP,70ns,3.3V,LL
KM68V1000BLG-10	32-SOP,100ns,3.3V,L	KM68V1000BLGE-10	32-SOP,100ns,3.3V,L	KM68V1000BLGI-10	32-SOP,100ns,3.3V,L
KM68V1000BLG-10L	32-SOP,100ns,3.3V,LL	KM68V1000BLGE-10L	32-SOP,100ns,3.3V,LL	KM68V1000BLGI-10L	32-SOP,100ns,3.3V,LL
KM68V1000BLT-7	32-TSOP F,70ns,3.3V,L	KM68V1000BLTE-7	32-TSOP F,70ns,3.3V,L	KM68V1000BLTI-7	32-TSOP F,70ns,3.3V,L
KM68V1000BLT-7L	32-TSOP F,70ns,3.3V,LL	KM68V1000BLTE-7L	32-TSOP F,70ns,3.3V,LL	KM68V1000BLTI-7L	32-TSOP F,70ns,3.3V,LL
KM68V1000BLT-10	32-TSOP F,100ns,3.3V,L	KM68V1000BLTE-10	32-TSOP F,100ns,3.3V,L	KM68V1000BLTI-10	32-TSOP F,100ns,3.3V,L
KM68V1000BLT-10L	32-TSOP F,100ns,3.3V,LL	KM68V1000BLTE-10L	32-TSOP F,100ns,3.3V,LL	KM68V1000BLTI-10L	32-TSOP F,100ns,3.3V,LL
KM68V1000BLR-7	32-TSOP R,70ns,3.3V,L	KM68V1000BLRE-7	32-TSOP R,70ns,3.3V,L	KM68V1000BLRI-7	32-TSOP R,70ns,3.3V,L
KM68V1000BLR-7L	32-TSOP R,70ns,3.3V,LL	KM68V1000BLRE-7L	32-TSOP R,70ns,3.3V,LL	KM68V1000BLRI-7L	32-TSOP R,70ns,3.3V,LL
KM68V1000BLR-10	32-TSOP R,100ns,3.3V,L	KM68V1000BLRE-10	32-TSOP R,100ns,3.3V,L	KM68V1000BLRI-10	32-TSOP R,100ns,3.3V,L
KM68V1000BLR-10L	32-TSOP R,100ns,3.3V,LL	KM68V1000BLRE-10L	32-TSOP R,100ns,3.3V,LL	KM68V1000BLRI-10L	32-TSOP R,100ns,3.3V,LL
KM68U1000BLG-8	32-SOP,85ns,3.0V,L	KM68U1000BLGE-10	32-SOP,100ns,3.0V,L	KM68U1000BLGI-10	32-SOP,100ns,3.0V,L
KM68U1000BLG-8L	32-SOP,85ns,3.0V,LL	KM68U1000BLGE-10L	32-SOP,100ns,3.0V,LL	KM68U1000BLGI-10L	32-SOP,100ns,3.0V,LL
KM68U1000BLG-10	32-SOP,100ns,3.0V,L	KM68U1000BLTE-10	32-TSOP F,100ns,3.0V,L	KM68U1000BLTI-10	32-TSOP F,100ns,3.0V,L
KM68U1000BLG-10L	32-SOP,100ns,3.0V,LL	KM68U1000BLTE-10L	32-TSOP F,100ns,3.0V,LL	KM68U1000BLTI-10L	32-TSOP F,100ns,3.0V,LL
KM68U1000BLT-8	32-TSOP F,85ns,3.0V,L	KM68U1000BLRE-10	32-TSOP R,100ns,3.0V,L	KM68U1000BLRI-10	32-TSOP R,100ns,3.0V,L
KM68U1000BLT-8L	32-TSOP F,85ns,3.0V,LL	KM68U1000BLRE-10L	32-TSOP R,100ns,3.0V,LL	KM68U1000BLRI-10L	32-TSOP R,100ns,3.0V,LL
KM68U1000BLT-10	32-TSOP F,100ns,3.0V,L				
KM68U1000BLT-10L	32-TSOP F,100ns,3.0V,LL				
KM68U1000BLR-8	32-TSOP R,85ns,3.0V,L				
KM68U1000BLR-8L	32-TSOP R,85ns,3.0V,LL				
KM68U1000BLR-10	32-TSOP R,100ns,3.0V,L				
KM68U1000BLR-10L	32-TSOP R,100ns,3.0V,LL				

ORDERING INFORMATION



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	0.7	W	-
Storage Temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	68V1000BL/L-L,68U1000BL/L-L
		-25 to 85	℃	68V1000BLE/LE-L,68U1000BLE/LE-L
		-40 to 85	℃	68V1000BLI/LI-L,68U1000BLI/LI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V1000B Family KM68U1000B Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	Vss	All Family	0	0	0	V
Input high voltage	V_{IH}	KM68V1000B Family KM68U1000B Family	2.2 2.2	- -	Vcc+0.3 Vcc+0.3	V
Input low voltage	V_{IL}	KM68V1000B Family KM68U1000B Family	-0.3*** -0.3***	- -	0.4 0.4	V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Extended Product : T_A=-25 to 85℃, unless otherwise specified
3) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}= Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL}, V_{IO} =Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA		-	2	5	mA
Average operating current		I_{CC1}	1μs cycle 100% duty, I_{IO}=0mA $\overline{CS_1}$≤ 0.2V, CS_2≥Vcc-0.2V		-	3	5	mA
		I_{CC2}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, Min cycle, 100% duty, I_{IO}=0mA		-	30	40	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.2	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IH}		-	-	0.3	mA
Standby Current (CMOS)	68V1000BL/L-L	I_{SB1}	$\overline{CS_1}$≥Vcc-2.0V CS_2≥Vcc-2.0V or CS_2≤0.2V Other input = 0~Vcc	L (Low Power) LL (Low Low Power)	- -	1 0.5	50 15	μA
	68V1000BLE/LE-L 68V1000BLI/LI-L			L (Low Power) LL (Low Low Power)	- -	1 0.5	100 20	μA
	68U1000BL/L-L			L (Low Power) LL (Low Low Power)	- -	1 0.5	50 15	μA
	68U1000BLE/LE-L 68U1000BLI/LI-L			L (Low Power) LL (Low Low Power)	- -	1 0.5	50 15	μA

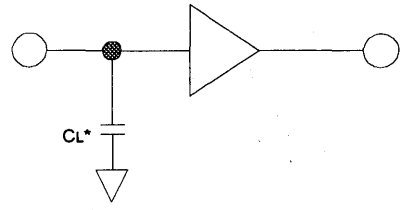
* 1) Commercial Product : T_A=0 to 70℃, Vcc=3.3V±0.3V(68V1000B Family), Vcc=3.0V±0.3V(68U1000B Family)
2) Extended Product : T_A=-25 to 85℃, Vcc=3.3V±0.3V(68V1000BE Family), Vcc=3.0V±0.3V(68U1000BE Family)
2) Industrial Product : T_A=-40 to 85℃, Vcc=3.3V±0.3V(68V1000BI Family), Vcc=3.0V±0.3V(68U1000BI Family)
** T_A=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input riseing and falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL	-

* See DC Operating conditions



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V1000BL/L-L	0~70℃	3.3V±0.3	70*/100ns	Commercial
KM68V1000BLE/LE-L	-25~85℃	3.3V±0.3	70*/100ns	Extended
KM68V1000BLI/LI-L	-40~85℃	3.3V±0.3	70*/100ns	Industrial
KM68U1000BL/L-L	0~70℃	3.0V±0.3	70ns	Commercial
KM68U1000BLE/LE-L	-25~85℃	3.0V±0.3	100ns	Extended
KM68U1000BLI/LI-L	-40~85℃	3.0V±0.3	100ns	Industrial

* The parameter is measured with 30pF test load.

2

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins				Units
			*70ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	100	-	ns
	Address access time	tAA	-	70	-	100	ns
	Chip select to output	tCO	-	70	-	100	ns
	Output enable to valid output	tOE	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	30	ns
	Output hold from address change	tOH	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	100	-	ns
	Chip select to end of write	tCW	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	80	-	ns
	Write pulse width	tWP	55	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	ns

* The parameter is measured with 30pF test load.

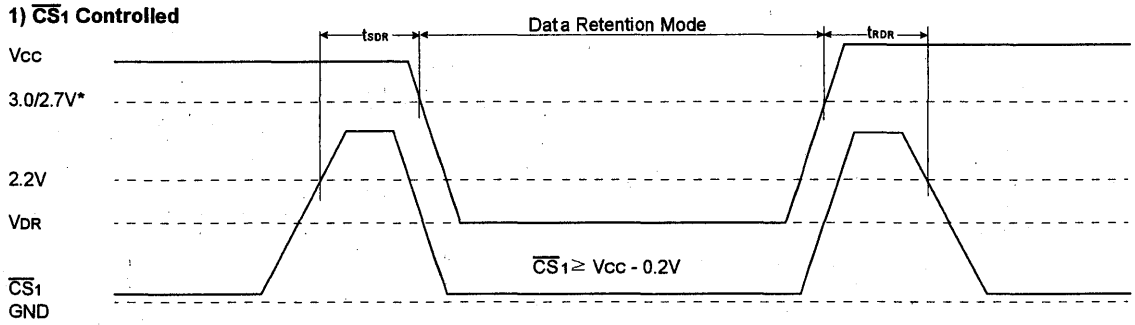
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS_1}$*** ≥ Vcc-2.0V		2.0	-	3.6	V
Data retention current	I_{DR}	KM68V1000BL KM68V1000BL-L	Vcc=3.0V $\overline{CS_1}$≥Vcc-0.2V	L-Ver LL-Ver	- -	1 0.5	30 15	µA
		KM68V1000BLE KM68V1000BLE-L		L-Ver LL-Ver	- -	- -	50 20	
		KM68V1000BLI KM68V1000BLI-L		L-Ver LL-Ver	- -	- -	50 20	
		KM68U1000BL KM68U1000BL-L		L-Ver LL-Ver	- -	- -	25 10	
		KM68U1000BLE KM68U1000BLE-L		L-Ver LL-Ver	- -	- -	25 15	
		KM68U1000BLI KM68U1000BLI-L		L-Ver LL-Ver	- -	- -	25 15	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

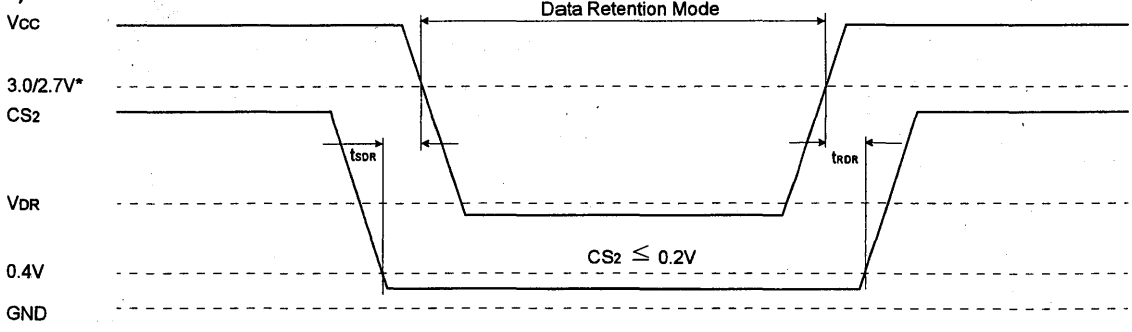
* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Extended Product : T_A=-25 to 85℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** $\overline{CS_1}$≥ Vcc-0.2V, CS2≥Vcc-0.2V($\overline{CS_1}$ controlled) or CS2≤0.2V(CS2 controlled)

DATA RETENTION TIMING DIAGRAM

1) $\overline{CS_1}$ Controlled



2) CS_2 Controlled

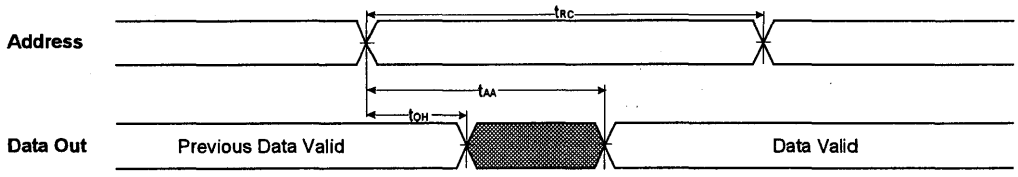


*3.0V for KM68V1000B family, 2.7V for KM68U1000B family

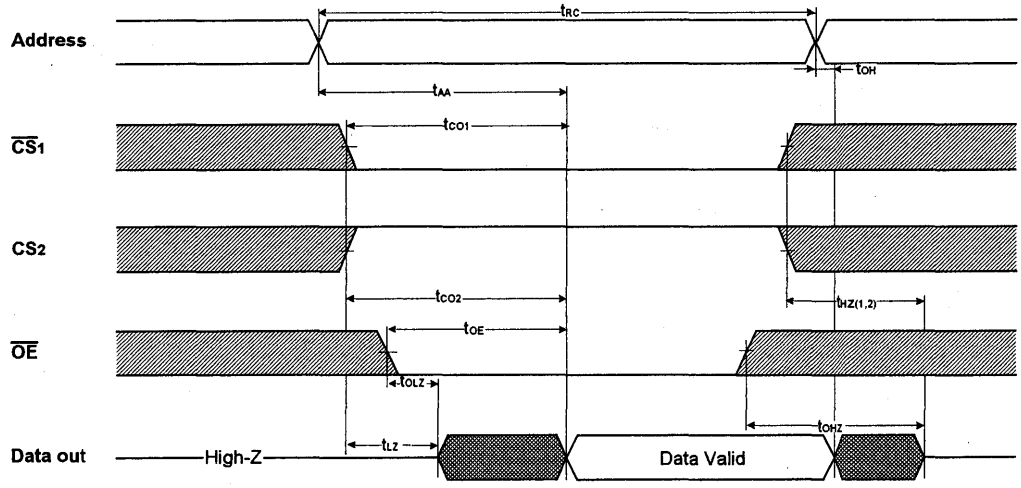
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, CS_2=$\overline{WE}$=V_{IH})



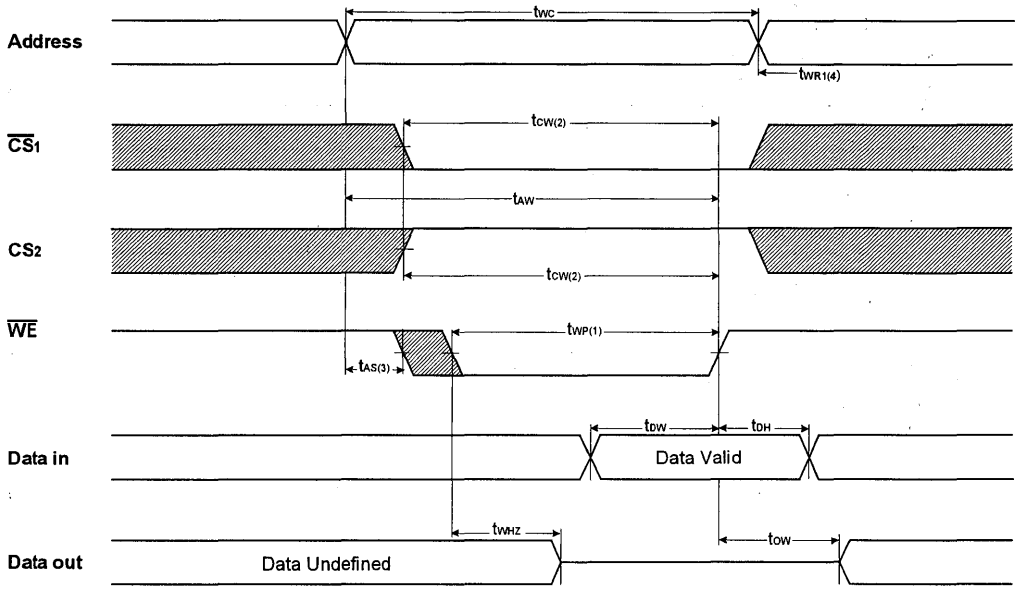
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



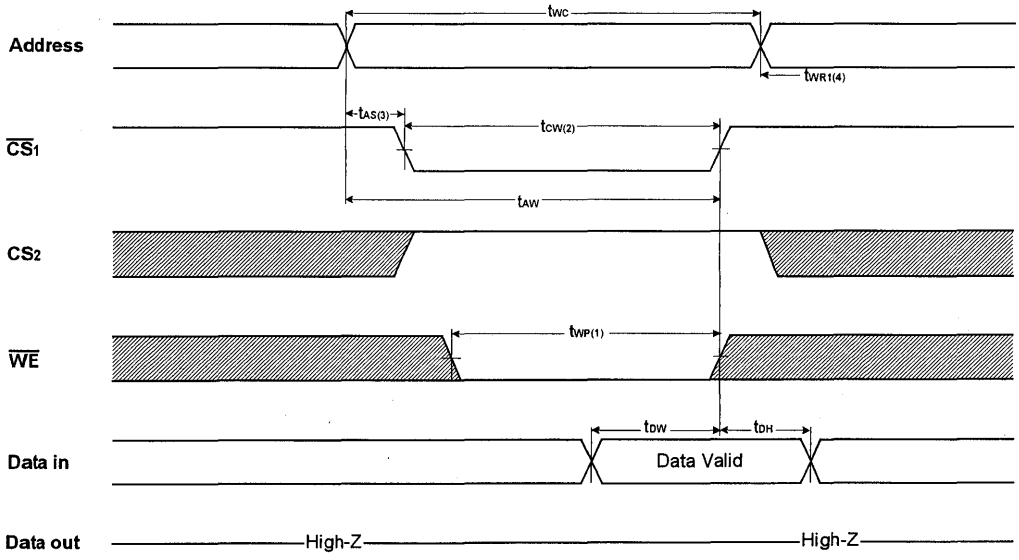
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.

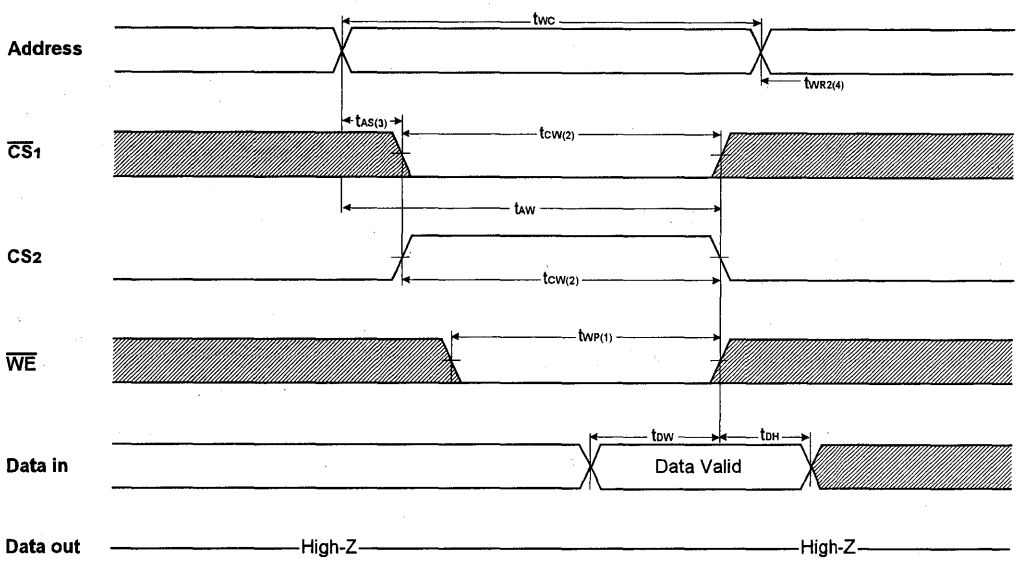
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS_2}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap of low $\overline{CS_1}$, high CS_2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ going low, CS_2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning or write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends at $\overline{CS_1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS_2 going to low.

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	I_{SB},I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB},I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	Dout	I_{CC}
L	H	L	X	Write	Din	I_{CC}

* X means don't care (Must be in high or low state)

128K x8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : 0.4㎛ CMOS
- Organization : 128K x8
- Power Supply Voltage :
  KM68V1000C family : 3.3V±0.3V
  KM68U1000C family : 3.0V±0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-SOP, 32-TSOP(I)-F/R, 32-sTSOP(I)-F/R

GENERAL DESCRIPTION

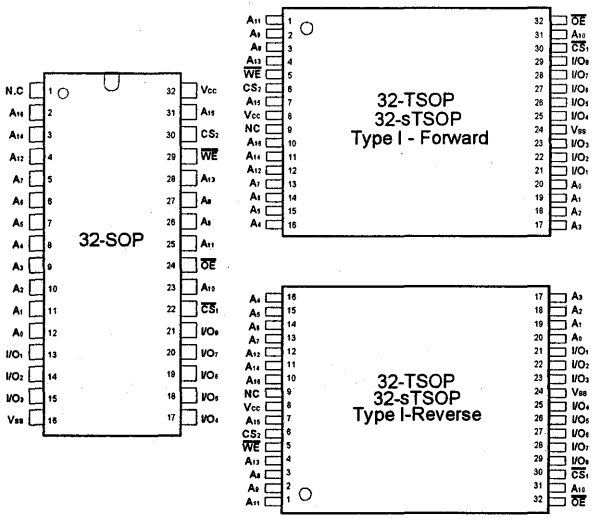
The KM68V1000C and KM68U1000C family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

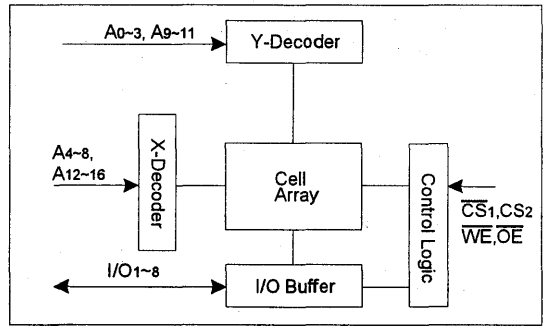
Product Family	Operating Temperature	Vcc Range(V)	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM68V1000CL-L	Commercial (0~70℃)	3.0~3.6V	70/85ns	10㎂	40mA	32-SOP 32-sTSOP(I) R/F 32-TSOP(I) R/F
KM68U1000CL-L		2.7~3.3V	70*/100ns			
KM68V1000CLE-L	Extended (-25~85℃)	3.0~3.6V	70/85ns	20㎂		
KM68U1000CLE-L		2.7~3.3V	70*/100ns			
KM68V1000CLI-L	Industrial (-25~85℃)	3.0~3.6V	70/85ns	20㎂		
KM68U1000CLI-L		2.7~3.3V	70*/100ns			

*The parameter is measured with 30pF test load.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function
A0~A16	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}_1$,CS2	Chip Select Inputs
$\overline{OE}$	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

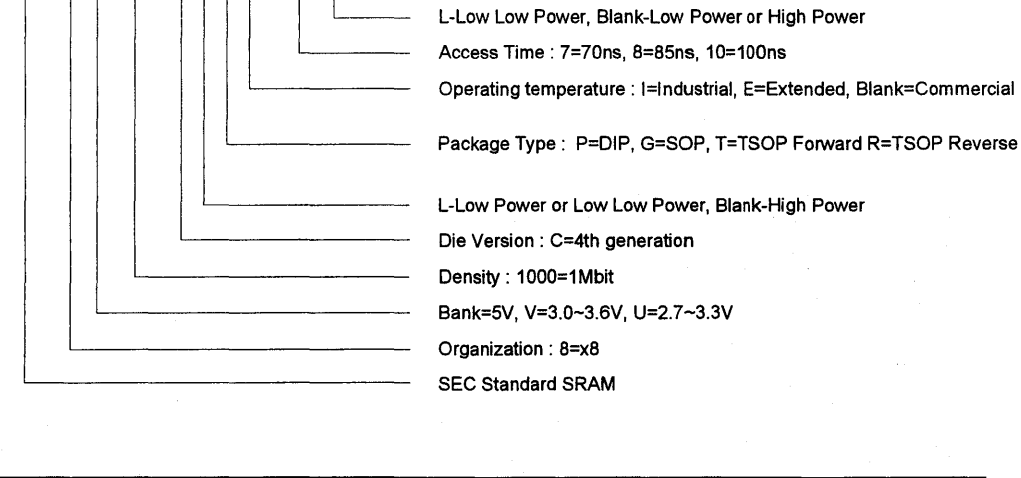
SAMSUNG ELECTRONICS

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Extended Temp Products (-25~85℃)		Industrial Temp Products (-40~85℃)	
Part Name	Function	Part Name	Function	Part Name	Function
KM68V1000CLG-7L	32-SOP,70ns,3.3V,LL	KM68V1000CLGE-7L	32-SOP,70ns,3.3V,LL	KM68V1000CLGI-7L	32-SOP,70ns,3.3V,LL
KM68V1000CLG-8L	32-SOP,85ns,3.3V,LL	KM68V1000CLGE-8L	32-SOP,85ns,3.3V,LL	KM68V1000CLGI-8L	32-SOP,85ns,3.3V,LL
KM68V1000CLT-7L	32-TSOP F,70ns,3.3V,LL	KM68V1000CLTE-7L	32-TSOP F,70ns,3.3V,LL	KM68V1000CLTI-7L	32-TSOP F,70ns,3.3V,LL
KM68V1000CLT-8L	32-TSOP F,85ns,3.3V,LL	KM68V1000CLTE-8L	32-TSOP F,85ns,3.3V,LL	KM68V1000CLTI-8L	32-TSOP F,85ns,3.3V,LL
KM68V1000CLR-7L	32-TSOP R,70ns,3.3V,LL	KM68V1000CLRE-7L	32-TSOP R,70ns,3.3V,LL	KM68V1000CLRI-7L	32-TSOP R,70ns,3.3V,LL
KM68V1000CLR-8L	32-TSOP R,85ns,3.3V,LL	KM68V1000CLRE-8L	32-TSOP R,85ns,3.3V,LL	KM68V1000CLRI-8L	32-TSOP R,85ns,3.3V,LL
KM68U1000CLG-7L	32-SOP,70ns,3.0V,LL	KM68U1000CLGE-7L	32-SOP,70ns,3.0V,LL	KM68U1000CLGI-7L	32-SOP,70ns,3.0V,LL
KM68U1000CLG-10L	32-SOP,85ns,3.0V,LL	KM68U1000CLGE-10L	32-SOP,85ns,3.0V,LL	KM68U1000CLGI-10L	32-SOP,85ns,3.0V,LL
KM68U1000CLT-7L	32-TSOP F,70ns,3.0V,LL	KM68U1000CLTE-7L	32-TSOP F,70ns,3.0V,LL	KM68U1000CLTI-7L	32-TSOP F,70ns,3.0V,LL
KM68U1000CLT-10L	32-TSOP F,100ns,3.0V,LL	KM68U1000CLTE-10L	32-TSOP F,100ns,3.0V,LL	KM68U1000CLTI-10L	32-TSOP F,100ns,3.0V,LL
KM68U1000CLR-7L	32-TSOP R,70ns,3.0V,LL	KM68U1000CLRE-7L	32-TSOP R,70ns,3.0V,LL	KM68U1000CLRI-7L	32-TSOP R,70ns,3.0V,LL
KM68U1000CLR-10L	32-TSOP R,100ns,3.0V,LL	KM68U1000CLRE-10L	32-TSOP R,100ns,3.0V,LL	KM68U1000CLRI-10L	32-TSOP R,100ns,3.0V,LL
KM68V1000CLTG-7L	32-sTSOP F,70ns,3.3V,LL	KM68V1000CLTGE-7L	32-sTSOP F,70ns,3.3V,LL	KM68V1000CLTGI-7L	32-sTSOP F,70ns,3.3V,LL
KM68V1000CLTG-8L	32-sTSOP F,85ns,3.3V,LL	KM68V1000CLTGE-8L	32-sTSOP F,85ns,3.3V,LL	KM68V1000CLTGI-8L	32-sTSOP F,85ns,3.3V,LL
KM68V1000CLRG-7L	32-sTSOP R,70ns,3.3V,LL	KM68V1000CLRGE-7L	32-sTSOP R,70ns,3.3V,LL	KM68V1000CLRGI-7L	32-sTSOP R,70ns,3.3V,LL
KM68V1000CLRG-8L	32-sTSOP R,85ns,3.3V,LL	KM68V1000CLRGE-8L	32-sTSOP R,85ns,3.3V,LL	KM68V1000CLRGI-8L	32-sTSOP R,85ns,3.3V,LL
KM68U1000CLTG-7L	32-sTSOP F,70ns,3.0V,LL	KM68U1000CLTGE-7L	32-sTSOP F,70ns,3.0V,LL	KM68U1000CLTGI-7L	32-sTSOP F,70ns,3.0V,LL
KM68U1000CLTG-10L	32-sTSOP F,100ns,3.0V,LL	KM68U1000CLTGE-10L	32-sTSOP F,100ns,3.0V,LL	KM68U1000CLTGI-10L	32-sTSOP F,100ns,3.0V,LL
KM68U1000CLRG-7L	32-sTSOP R,70ns,3.0V,LL	KM68U1000CLRGE-7L	32-sTSOP R,70ns,3.0V,LL	KM68U1000CLRGI-7L	32-sTSOP R,70ns,3.0V,LL
KM68U1000CLRG-10L	32-sTSOP R,100ns,3.0V,LL	KM68U1000CLRGE-10L	32-sTSOP R,100ns,3.0V,LL	KM68U1000CLRGI-10L	32-sTSOP R,100ns,3.0V,LL

ORDERING INFORMATION



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	0.7	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM68V1000CL-L/KM68U1000CL-L
		-25 to 85	℃	KM68V1000CLE-L/KM68U1000CLE-L
		-40 to 85	℃	KM68V1000CLI-L/KM68U1000CLI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V1000C Family KM68U1000C Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	Vss	All Family	0	0	0	V
Input high voltage	V_{IH}	KM68V1000C Family KM68U1000C Family	2.2 2.2	- -	Vcc+0.3 Vcc+0.3	V
Input low voltage	V_{IL}	KM68V1000C Family KM68U1000C Family	-0.3*** -0.3***	- -	0.4 0.4	V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Extended Product : T_A=-25 to 85℃, unless otherwise specified
3) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, TA=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

* Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL}, Vio=Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IH} or V_{IL} I_{IO}=0mA	Read	-	-	5	mA
				Write			15	
Average operating current		I_{CC1}	Cycle time=1μs 100% duty, I_{IO}=0mA $\overline{CS_1}$≤0.2V, CS_2≥Vcc-0.2V	Read	-	-	5	mA
				Write			15	
		I_{CC2}	Min cycle, 100% duty, I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}		-	30	40	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.2	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL}		-	-	0.3	mA
Standby Current (CMOS)	KM68V1000CL-L KM68V1000CLE-L KM68V1000CLI-L	I_{SB1}	$\overline{CS_1}$≥Vcc-0.2V CS_2≥Vcc-0.2V or CS_2≤0.2V Other input =0~Vcc	Low Low Power	- - -	0.5 0.5 0.5	10 20 20	μA
	KM68U1000CL-LI KM68U1000CLE-L KM68U1000CLI-L				- - -	0.5 0.5 0.5	10 20 20	μA

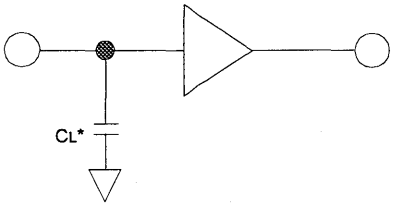
* 1) Commercial Product : T_A=0 to 70℃, Vcc=3.3V±0.3V(68V1000C Family), Vcc=3.0V±0.3V(68U1000C Family)
2) Extended Product : T_A=-25 to 85℃, Vcc=3.3V±0.3V(68V1000CE Family), Vcc=3.0V±0.3V(68U1000CE Family)
3) Industrial Product : T_A=-40 to 85℃, Vcc=3.3V±0.3V(68V1000CI Family), Vcc=3.0V±0.3V(68U1000CI Family)
** T_A=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rising and falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL **C_L=30pF+1TTL	-

* See DC Operating conditions
** KM68U1000CL-7L Family



* Including scope and jig capacitance

SAMSUNG ELECTRONICS

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V1000CL-L	0~70℃	3.3V±0.3	70/85ns	Commercial
KM68V1000CLE-L	-25~85℃	3.3V±0.3	70/85ns	Extended
KM68V1000CLI-L	-40~85℃	3.3V±0.3	70/85ns	Industrial
KM68U1000CL-L	0~70℃	3.0V±0.3	70*/100ns	Commercial
KM68U1000CLE-L	-25~85℃	3.0V±0.3	70*/100ns	Extended
KM68U1000CLI-L	-40~85℃	3.0V±0.3	70*/100ns	Industrial

* The parameter is measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	30	ns
	Output hold from address change	tOH	10	-	15	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

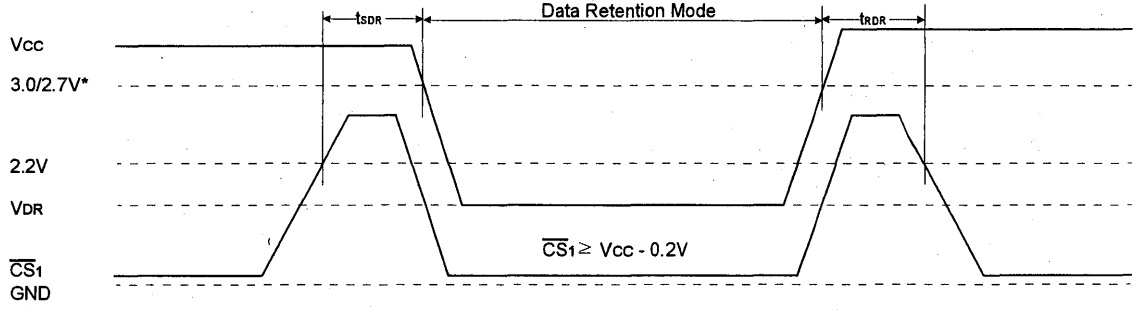
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS_1}$*** ≥Vcc-0.2V		2.0	-	3.6	V
Data retention current	I_{DR}	KM68V1000CL-L KM68V1000CLE-L KM68V1000CLI-L	Vcc=3.0V $\overline{CS_1}$≥Vcc-0.2V	Low Low Power	- - -	0.5 0.5 0.5	10 20 20	μA
		KM68U1000CL-L KM68U1000CLE-L KM68U1000CLI-L			- - -	0.5 0.5 0.5	10 20 20	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

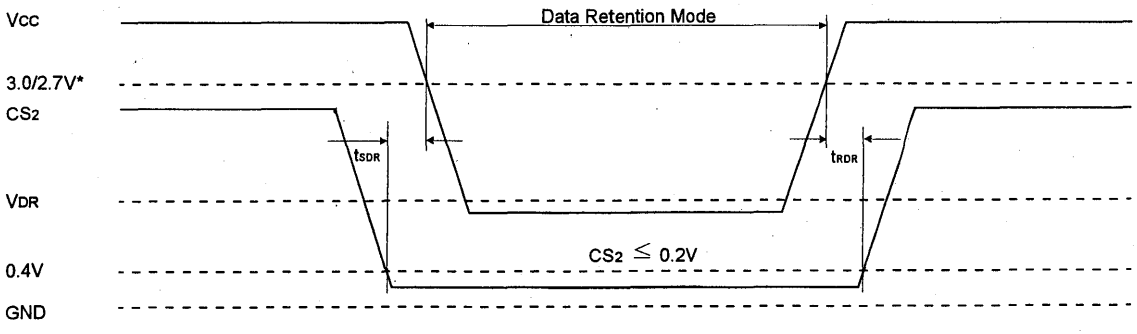
* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Extended Product : T_A=-25 to 85℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** $\overline{CS_1}$≥ Vcc-0.2V, CS_2≥Vcc-0.2V($\overline{CS_1}$ controlled) or CS_2≤0.2V(CS_2 controlled)

DATA RETENTION TIMING DIAGRAM

1) $\overline{CS_1}$ Controlled



2) CS_2 Controlled



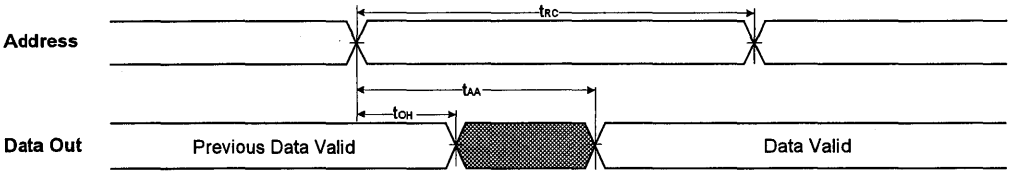
*3.0V for KM68V1000C family, 2.7V for KM68U1000C family

SAMSUNG ELECTRONICS

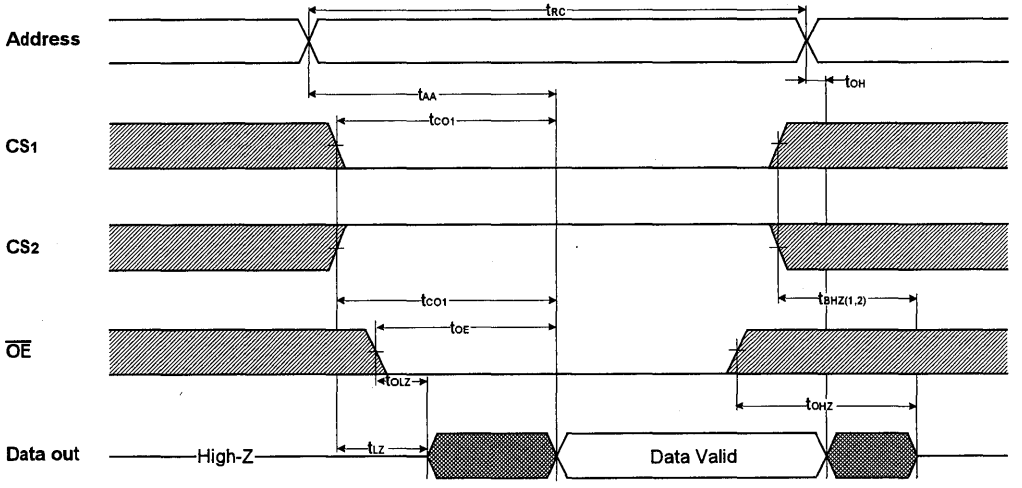
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS_1}$=$\overline{OE}$=V_{IL}, CS_2=$\overline{WE}$=V_{IH})



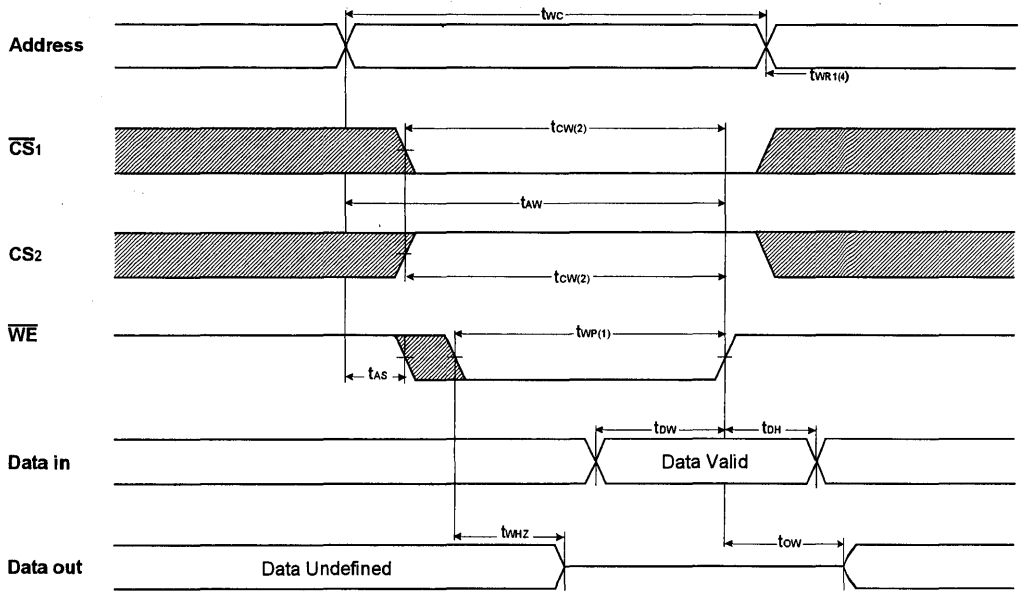
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



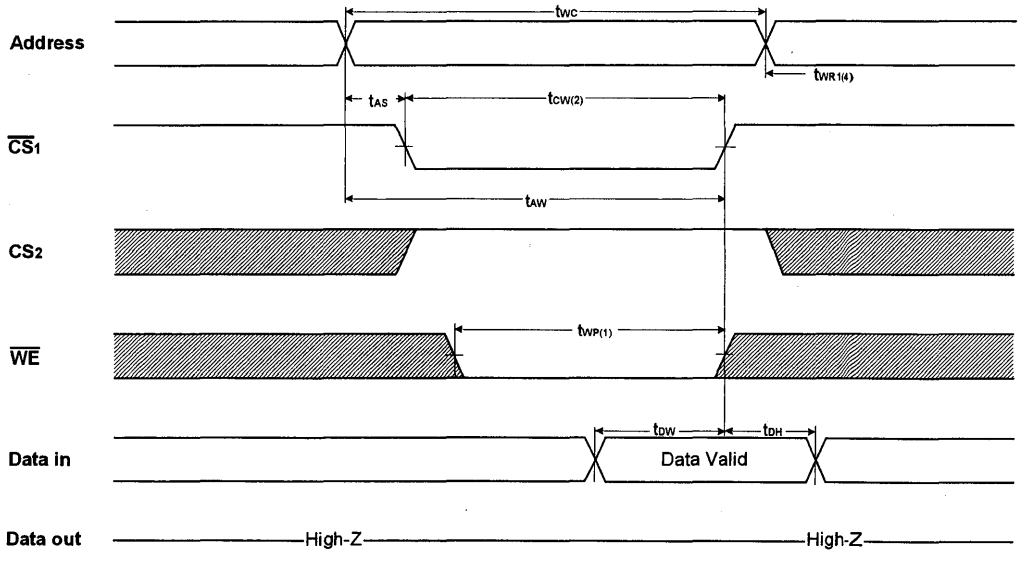
NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.

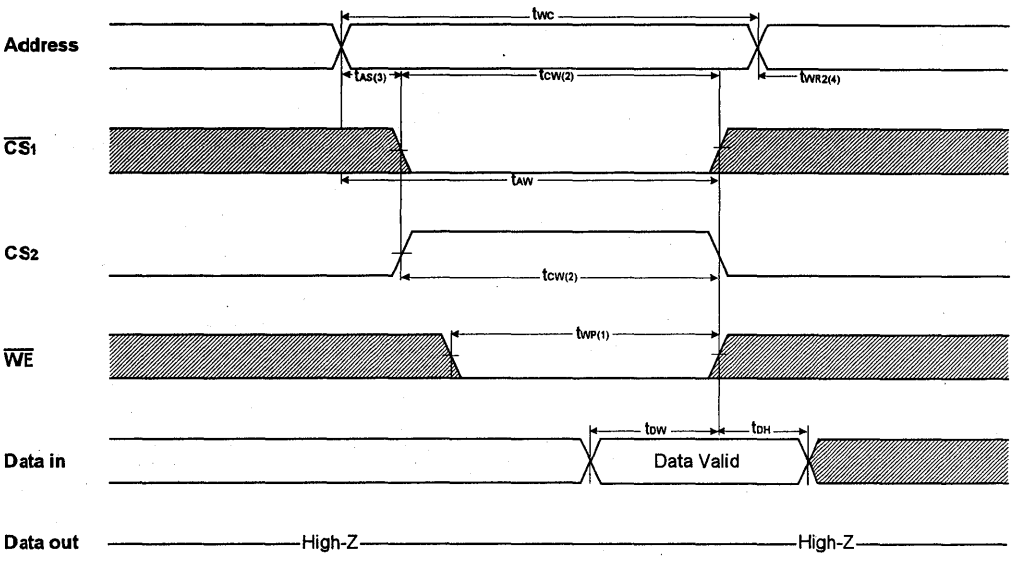
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS_2 Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap of low $\overline{CS_1}$, high CS_2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ going low, CS_2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning or write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address calid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends at $\overline{CS_1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS_2 going to low.

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	I_{SB},I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB},I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	Dout	I_{CC}
L	H	L	X	Write	Din	I_{CC}

* X means don't care(Must be in high or low status.)

64K x16 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : 0.6㎛ CMOS
- Organization : 64K x16
- Data Byte Control : $\overline{LB}$=I/O1~8, $\overline{UB}$=I/O9~16
- Power Supply Voltage :
  KM616V1000B family : 3.3V ± 0.3V
  KM616U1000B family : 3.0V ± 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  44-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

The KM616v1000B and KM616U1000B family are fabricated by SAMSUNG s advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

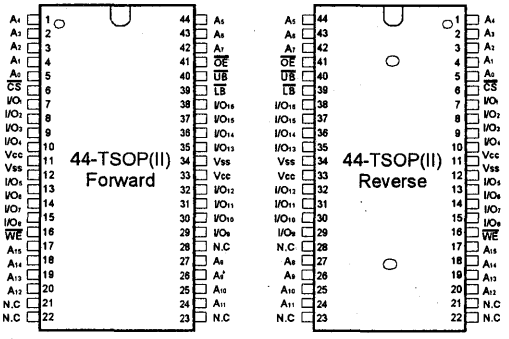
2

PRODUCT FAMILY

Product List	Operating Temp.	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2)	
KM616V1000BL/L-L KM616U1000BL/L-L	Commercia (0~70℃)	3.0~3.6V 2.7~3.3V	70*/100 100	50/15㎂ 50/15㎂	65mA	44-TSOP(II) Forward/Reverse
KM616V1000BLE/LE-L KM616U1000BLE/LE-L	Extended (-25~85℃)	3.0~3.6V 2.7~3.3V	85*/100 100	100/20㎂ 100/20㎂		
KM616V1000BLI/LI-L KM616U1000BLI/LI-L	Industrial (-40~85℃)	3.0~3.6V 2.7~3.3V	85*/100 100	100/20㎂ 100/20㎂		

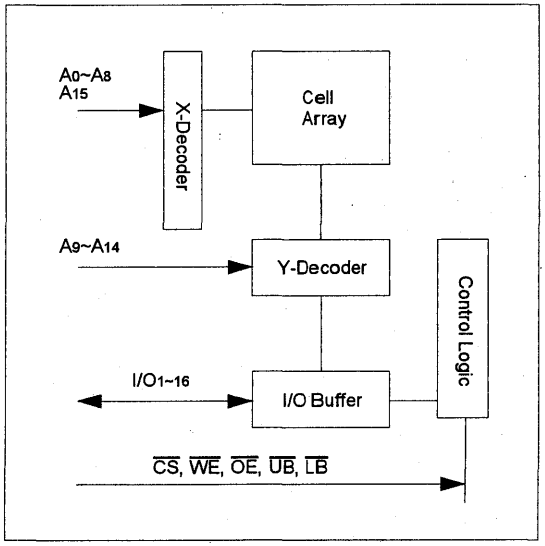
* The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
A0~A15	Address Inputs	$\overline{LB}$	Lower Byte (I/O1~8)
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O9~16)
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
I/O0~16	Data Inputs/Outputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



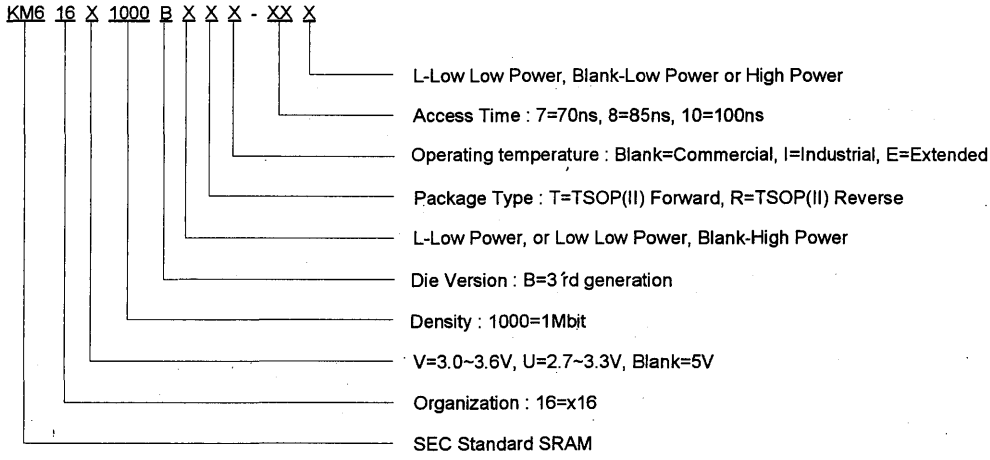
SAMSUNG ELECTRONICS

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Commercial Temp Product (-25~85℃)		Industrial Temp Products (-40~85℃)	
Part Name	Function	Part Name	Function	Part Name	Function
KM616V1000BLT-7	44-TSOP(II), F, 3.3V, 70ns, L	KM616V1000BLTE-8	44-TSOP(II), F, 3.3V, 85ns, L	KM616V1000BLTI-8	44-TSOP(II), F, 3.3V, 85ns, L
KM616V1000BLT-7L	44-TSOP(II), F, 3.3V, 70ns, LL	KM616V1000BLTE-8L	44-TSOP(II), F, 3.3V, 85ns, LL	KM616V1000BLTI-8L	44-TSOP(II), F, 3.3V, 85ns, LL
KM616V1000BLT-10	44-TSOP(II), F, 3.3V, 100ns, L	KM616V1000BLTE-10	44-TSOP(II), F, 3.3V,100ns, L	KM616V1000BLTI-10	44-TSOP(II), F, 3.3V,100ns, L
KM616V1000BLT-10L	44-TSOP(II), F, 3.3V, 100ns, LL	KM616V1000BLTE-10L	44-TSOP(II), F, 3.3V, 100ns, LL	KM616V1000BLTI-10L	44-TSOP(II), F, 3.3V, 100ns, LL
KM616U1000BLT-10	44-TSOP(II), F, 3.0V, 100ns, L	KM616U1000BLTE-10	44-TSOP(II), F, 3.0V,100ns, L	KM616U1000BLTI-10	44-TSOP(II), F, 3.0V,100ns, L
KM616U1000BLT-10L	44-TSOP(II), F, 3.0V, 100ns, LL	KM616U1000BLTE-10L	44-TSOP(II), F, 3.0V, 100ns, LL	KM616U1000BLTI-10L	44-TSOP(II), F, 3.0V, 100ns, LL
KM616V1000BLR-7	44-TSOP(II), R, 3.3V, 70ns, L	KM616V1000BLRE-8	44-TSOP(II), R, 3.3V, 85ns, L	KM616V1000BLRI-8	44-TSOP(II), R, 3.3V, 85ns, L
KM616V1000BLR-7L	44-TSOP(II), R, 3.3V, 70ns, LL	KM616V1000BLRE-8L	44-TSOP(II), R, 3.3V, 85ns, LL	KM616V1000BLRI-8L	44-TSOP(II), R, 3.3V, 85ns, LL
KM616V1000BLR-10	44-TSOP(II), R, 3.3V, 100ns, L	KM616V1000BLRE-10	44-TSOP(II), R, 3.3V,100ns, L	KM616V1000BLRI-10	44-TSOP(II), R, 3.3V,100ns, L
KM616V1000BLR-10L	44-TSOP(II), R, 3.3V, 100ns, LL	KM616V1000BLRE-10L	44-TSOP(II), R, 3.3V, 100ns, LL	KM616V1000BLRI-10L	44-TSOP(II), R, 3.3V, 100ns, LL
KM616U1000BLR-10	44-TSOP(II), R, 3.0V, 100ns, L	KM616U1000BLRE-10	44-TSOP(II), R, 3.0V,100ns, L	KM616U1000BLRI-10	44-TSOP(II), R, 3.0V,100ns, L
KM616U1000BLR-10L	44-TSOP(II), R, 3.0V, 100ns, LL	KM616U1000BLRE-10L	44-TSOP(II), R, 3.0V, 100ns, LL	KM616U1000BLRI-10L	44-TSOP(II), R, 3.0V, 100ns, LL

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 4.6	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM616V1000BL/L-L KM616U1000BL/L-L
		-25 to 85	℃	KM616V1000BLE/LE-L KM616U1000BLE/LE-L
		-40 to 85	℃	KM616V1000BLI/LI-L KM616U1000BLI/LI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM616V1000B Family KM616U1000B Family	3.0 2.7	3.3 3.0	3.6 3.3	V V
Ground	Vss	All Family	0	0	0	V
Input high voltage	V_{IH}	KM616V1000B Family KM616U1000B Family	2.2 2.2	- -	Vcc+0.3 Vcc+0.3	V V
Input low voltage	V_{IL}	KM616V1000B Family KM616U1000B Family	-0.5*** -0.5***	- -	0.4 0.4	V V

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** Ta=25℃
*** Vil(min)=-3.0V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, TA=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}, $\overline{UB}$=V_{IH} or $\overline{LB}$=V_{IH} V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current Average operatingcurrent		I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA	Read	-	-	10	mA
				Write	-	-	35	
		I_{CC1}	Cycle time=1μs 100% duty $\overline{CS}$≤0.2V, I_{IO}=0mA	Read	-	-	15	mA
				Write	-	-	40	
		I_{CC2}	Min cycle, 100% duty, $\overline{CS}$=V_{IL}, I_{IO}=0mA		-	-	65	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.2	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS}$=V_{IH}		-	-	0.5	mA
Standby current (CMOS)	616V1000BL-L-L	I_{SB1}	$\overline{CS}$≥Vcc-0.2V V_{IN}≥Vcc-0.2V or V_{IN}≤0.2V Other inputs = 0~Vcc	L(Low Power)	-	-	50	μA
				LL(L Low Power)	-	-	15	
	616V1000BLI/LI-L 616V1000BLE/LE-L			L(Low Power)	-	-	100	μA
				LL(L Low Power)	-	-	20	
	616U1000BL/L-L			L(Low Power)	-	-	50	μA
				LL(L Low Power)	-	-	15	
	616U1000BLI/LI-L 616U1000BLE/LE-L			L(Low Power)	-	-	100	μA
				LL(L Low Power)	-	-	20	

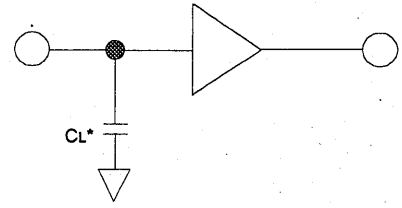
* 1) Commercial Product : T_A=0 to 70℃, Vcc=3.3V ± 0.3V(616V1000B Family), Vcc=3.0V ± 0.3V(616U1000B Family)
2) Extended Product : T_A=-25 to 85℃, Vcc=3.3V ± 0.3V(616V1000BE Family), Vcc=3.0V ± 0.3V(616U1000BE Family)
3) Industrial Product : T_A=-40 to 85℃, Vcc=3.3V ± 0.3V(616V1000BI Family), Vcc=3.0V ± 0.3V(616U1000BI Family)
** T_A=25℃
*** Industrial Product : I_{CC}(Read/Write)=10mA/40mA, I_{CC2}(Read/Write)=20mA/45mA

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.4V	-
Input rise fall time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL **C_L=30pF+1TTL	-

* See DC Operating conditions
** for 70ns, 85ns products



* Including scope and jig capacitance

SAMSUNG ELECTRONICS

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM616V1000BL-L KM616V1000BLE-L KM616V1000BLI-L	0~70℃ -25~85℃ -40~85℃	3.3V ± 0.3	70*/100ns 85*/100ns 85*/100ns	Commercial Extended Industrial
KM616U1000BL-L KM616U1000BLE-L KM616U1000BLI-L	0~70℃ -25~85℃ -40~85℃	3.0V ± 0.3	100ns	Commercial Extended Industrial

* The parameter is measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

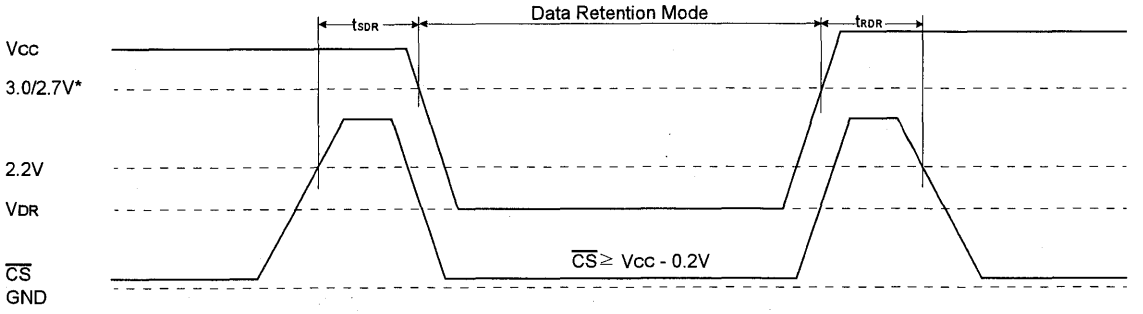
Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	$\overline{UB}$,$\overline{LB}$ Access Time	tBA	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	5	-	5	-	5	-	ns
	$\overline{UB}$,$\overline{LB}$ enable to low-Z output	tBLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	$\overline{UB}$,$\overline{LB}$ disable to high-Z output	tBHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	50	-	60	-	70	-	ns
	$\overline{UB}$, $\overline{LB}$ valid to end of write	tBW	60	-	70	-	80	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	30	0	30	0	35	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS} \geq$ Vcc-2.0V		2.0	-	3.6	V
Data retention current	I_{DR}	616V1000BL/L-L	Vcc=3.0V $\overline{CS} \geq$ Vcc-0.2V	L-Ver LL-Ver	- -	- -	30 15	µA
		616V1000BLE/LE-L 616V1000BLI/LI-L		L-Ver LL-Ver	- -	- -	50 20	
		616U1000BL/L-L		L-Ver LL-Ver	- -	- -	30 15	
		616U1000BLE/LE-L 616U1000BLI/LI-L		L-Ver LL-Ver	- -	- -	50 20	
Data retention set-up time	t_{SDR}		See data retention waveform		0	-	-	ms
Recovery time	t_{RDR}				5	-	-	

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-25 to 85℃, unless otherwise specified
3) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** Ta=25℃

DATA RETENTION TIMING DIAGRAM



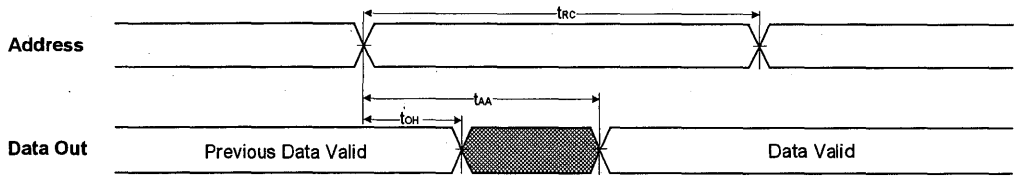
*3.0V for KM616V1000B family, 2.7V for KM616U1000B family

SAMSUNG ELECTRONICS

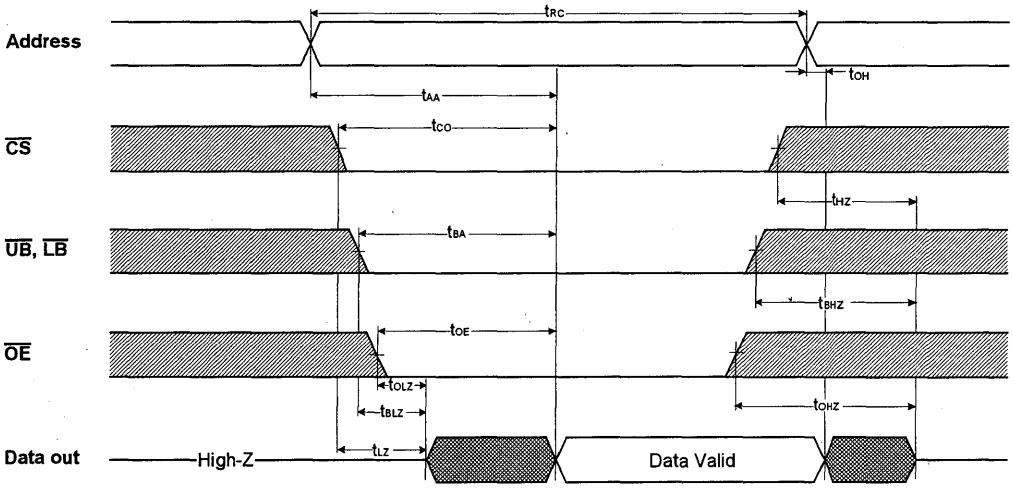
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=Vil, $\overline{WE}$=Vih, $\overline{UB}$ or and $\overline{LB}$=Vil)



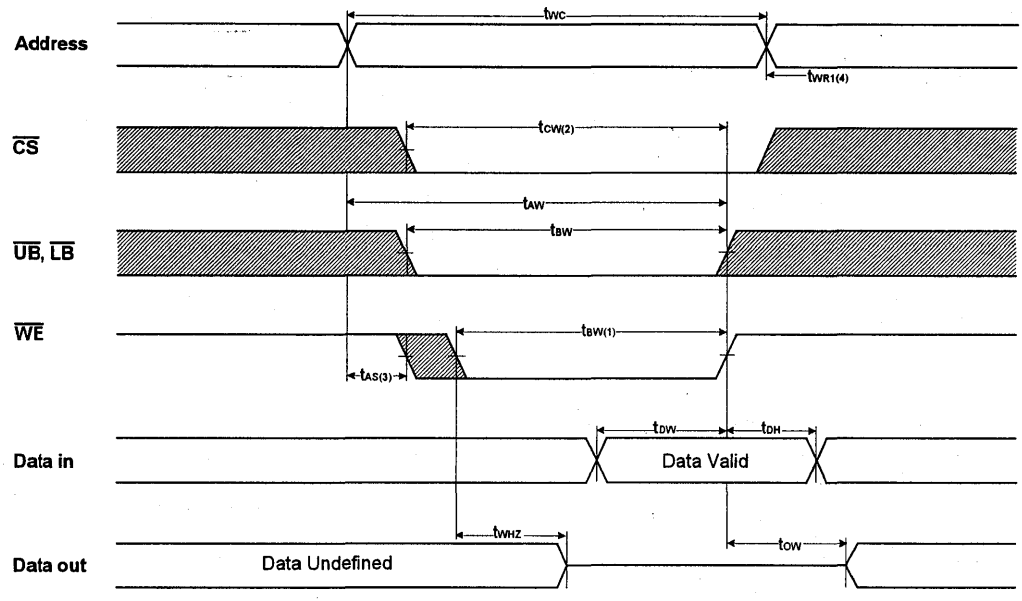
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



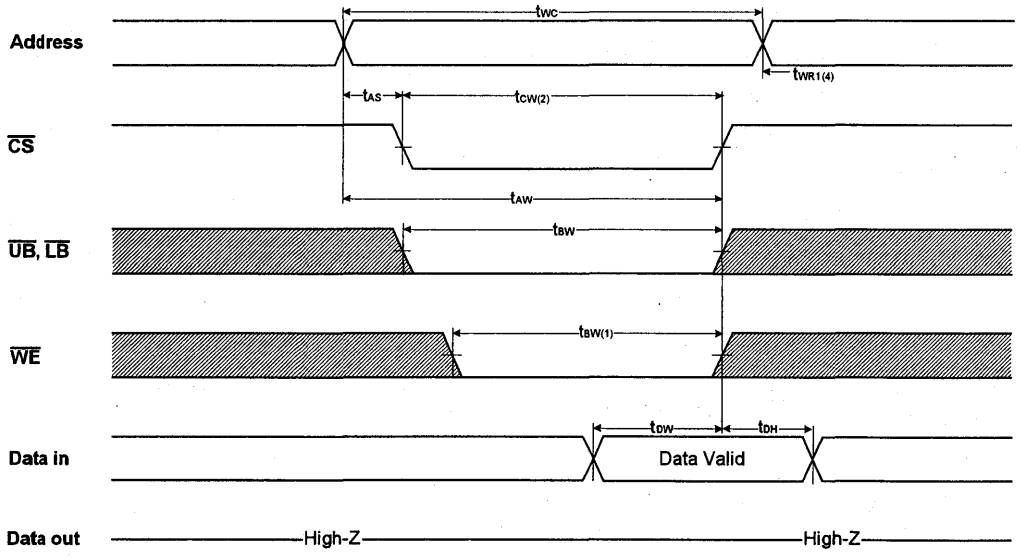
NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.

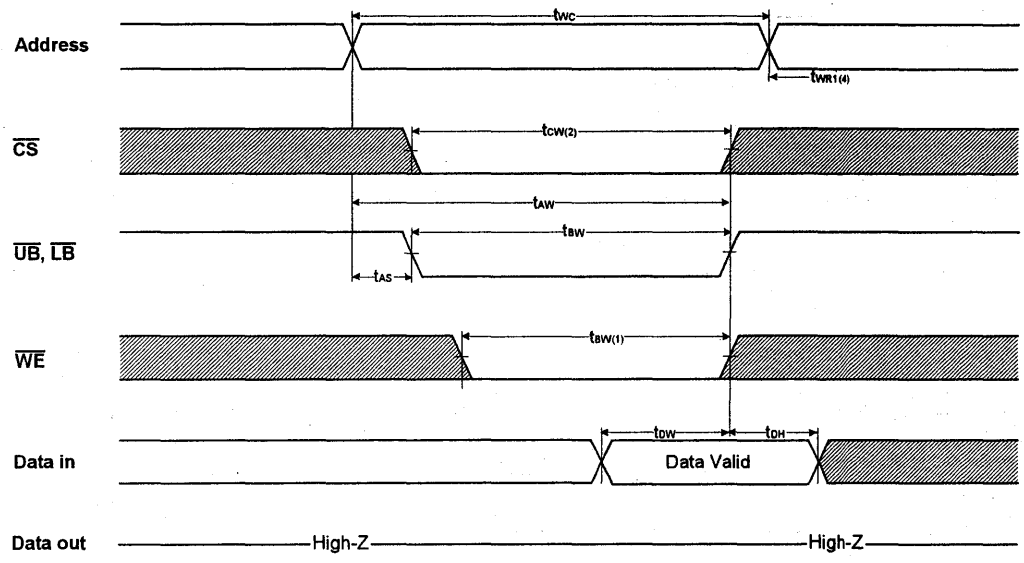
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{LB}$	$\overline{UB}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O1~8	I/O9~16	Current Mode
H	X	X	X	X	Not Select	High-Z	High-Z	Isb,Isb1
L	X	X	H	H	Output Disable	High-Z	High-Z	Icc
L	H	H	X	X		High-Z	High-Z	
L	L H L	H L L	H	L	Read	Dout High-Z Dout	High-Z Dout Dout	Icc
L	L H L	H L L	L	X	Write	Din High-Z Din	High Din Din	Icc

* X means don tcare (Must be in low or high state)

256Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : 0.4㎛ CMOS
- Organization : 256Kx8
- Power Supply Voltage
  KM68V2000A Family : 3.0V ~ 3.6V
  KM68U2000A Family : 2.7V ~ 3.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-TSOP(I)-F/R, 32-sTSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

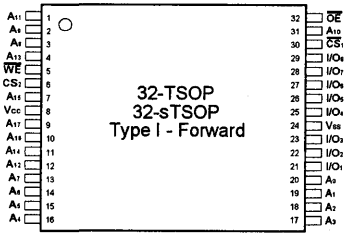
The KM68V2000 and KM68U2000 family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

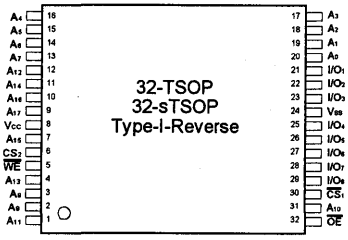
PRODUCT FAMILY

Product List	Operating Temp.	Vcc Range	Speed (ns)	PKG Type	Power Dissipation	
					Standby (I_{SB1}, Max)	Operating (I_{CC2})
KM68V2000L-L	Commercial (0~70℃)	3.0~3.6V	70/85	32-TSOP I-R/F 32-sTSOP I-R/F	15㎂	40mA
KM68U2000L-L		2.7~3.3V	70*/100		15㎂	
KM68V2000LI-L	Industria (-40~85℃)	3.0~3.6V	70/85		30㎂	
KM68U2000LI-L		2.7~3.3V	85*/100		30㎂	

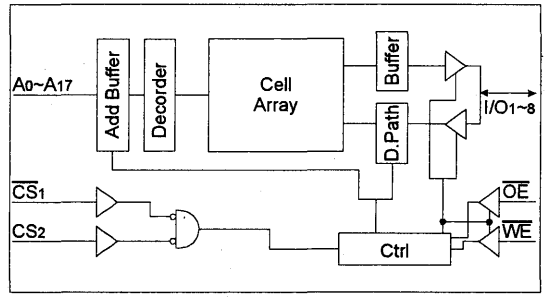
* The parameter is measured with 30pF test load.

PIN DESCRIPTION





FUNCTIONAL BLOCK DIAGRAM



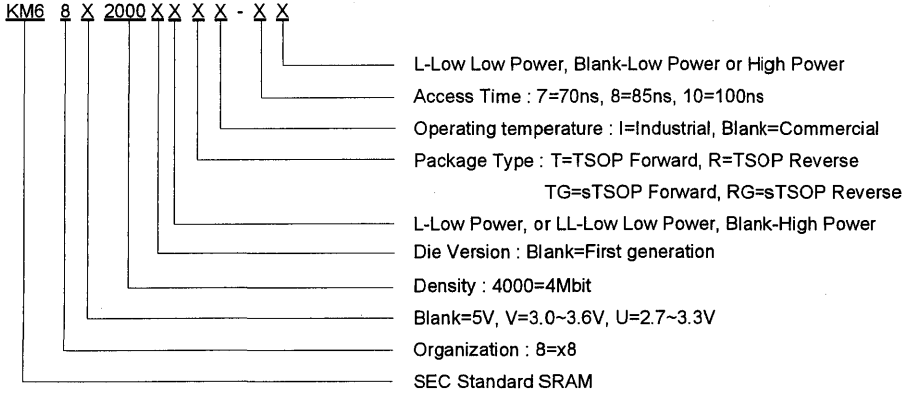
Name	Function	Name	Function
A0~A17	Address Inputs	Vcc	Power
$\overline{WE}$	Write Enable	Vss	Ground
$\overline{CS_1}$,CS2	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
$\overline{OE}$	Output Enable	N.C.	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Industrial Temp Products (-40~85℃)	
Part Name	**Function**	**Part Name**	**Function**
KM68V2000LT-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V2000LTI-7L	32-TSOP F, 70ns, 3.3V, LL
KM68V2000LT-8L	32-TSOP F, 85ns, 3.3V, LL	KM68V2000LIT-8L	32-TSOP F, 85ns, 3.3V, LL
KM68V2000LR-7L	32-TSOP R, 70ns, 3.3V, LL	KM68V2000LRI-7L	32-TSOP R, 70ns, 3.3V, LL
KM68V2000LR-8L	32-TSOP R, 85ns, 3.3V, LL	KM68V2000LRI-8L	32-TSOP R, 85ns, 3.3V, LL
KM68U2000LT-7L	32-TSOP F, 70ns, 3.0V, LL	KM68U2000LTI-8L	32-TSOP F, 85ns, 3.0V, LL
KM68U2000LT-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U2000LTI-10L	32-TSOP F, 100ns, 3.0V, LL
KM68U2000LR-7L	32-TSOP R, 70ns, 3.0V, LL	KM68U2000LRI-8L	32-TSOP R, 85ns, 3.0V, LL
KM68U2000LR-10L	32-TSOP R, 100ns, 3.0V, LL	KM68U2000LRI-10L	32-TSOP R, 100ns, 3.0V, LL
KM68V2000LTG-7L	32-sTSOP F, 70ns, 3.3V,LL	KM68V2000LTGI-7L	32-sTSOP F, 70ns, 3.3V,LL
KM68V2000LTG-8L	32-sTSOP F, 85ns, 3.3V,LL	KM68V2000LTGI-8L	32-sTSOP F, 85ns, 3.3V,LL
KM68V2000LRG-7L	32-sTSOP R, 70ns, 3.3V,LL	KM68V2000LRGI-7L	32-sTSOP R, 70ns, 3.3V,LL
KM68V2000LRG-8L	32-sTSOP R, 85ns, 3.3V,LL	KM68V2000LRGI-8L	32-sTSOP R, 85ns, 3.3V,LL
KM68U2000LTG-7L	32-sTSOP F, 70ns, 3.0V, LL	KM68U2000LTGI-8L	32-sTSOP F, 85ns, 3.0V, LL
KM68U2000LTG-10L	32-sTSOP F, 100ns, 3.0V, LL	KM68U2000LTGI-10L	32-sTSOP F, 100ns, 3.0V, LL
KM68U2000LRG-7L	32-sTSOP R, 70ns, 3.0V, LL	KM68U2000LRGI-8L	32-sTSOP R, 85ns, 3.0V, LL
KM68U2000LRG-10L	32-sTSOP R, 100ns, 3.0V, LL	KM68U2000LRGI-10L	32-sTSOP R, 100ns, 3.0V, LL

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	0.7	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM68V2000L/L KM68U2000L/L
		-40 to 85	℃	KM68V2000LI/L KM68U2000LI/L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V2000 Family KM68U2000 Family	3.0 2.7	3.3 3.0	3.6 3.3	V V
Ground	Vss	All Family	0	0	0	V
Input high voltage	V_{IH}	KM68V2000 Family KM68U2000 Family	2.2 2.2	- -	Vcc+0.3 Vcc+0.3	V V
Input low voltage	V_{IL}	KM68V2000 Family KM68U2000 Family	-0.3*** -0.3***	- -	0.4 0.4	V V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, TA=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	Vin=0V	-	8	pF
Input/Output capacitance	C_{IO}	Vio=0V	-	10	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, I_{IO}=0mA V_{IN}=V_{IH} or V_{IL}	Read	-	-	5	mA
				Write	-	-	15	
Average operatingcurrent		I_{CC1}	Cycle time=1μs 100%duty, I_{IO}=0mA $\overline{CS_1}$≤0.2V, CS_2≥Vcc-0.2V	Read	-	-	5	mA
				Write	-	-	15	
		I_{CC2}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, I_{IO}=0mA, Min cycle, 100% duty		-	30	40	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.2	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS_1}$=V_{IH}, CS2=V_{IL}		-	-	0.3	mA
Standby Current (CMOS)	KM68V2000L-I KM68V2000LI-L	I_{SB1}	$\overline{CS_1}$≥Vcc-2.0V CS_2≥Vcc-2.0V or CS_2≤0.2V Other inpts=0~Vcc	Low Low Power Low Low Power	- -	0.5 0.5	15 30	μA μA
	KM68U2000L-L KM68U2000LI-L			Low Low Power Low Low Power	-	0.5 0.5	15 30	μA μA

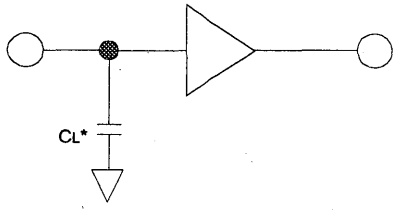
* 1) Commercial Product : T_A=0 to 70℃, Vcc=3.3±0.3V (68V2000 Family), Vcc=3.0±0.3V (68U2000 Family)
2) Industrial Product : T_A=-40 to 85℃, Vcc=3.3±0.3V (68V2000I Family), Vcc=3.0±0.3V (68U2000I Family)
** T_A=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rising and falingl time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL **C_L=30pF+1TTL	-

* See DC Operating conditions



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V2000L-L	0~70℃	3.3V ± 0.3	70/85ns	Commercial
KM68V2000LI-L	-40~85℃	3.3V ± 0.3	70/85ns	Industrial
KM68U2000L-L	0~70℃	3.0V ± 0.3	70*/100ns	Commercial
KM68U2000LI-L	-40~85℃	3.0V ± 0.3	85*/100ns	Industrial

* The parameters are measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	30	ns
	Output hold from address change	tOH	10	-	15	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

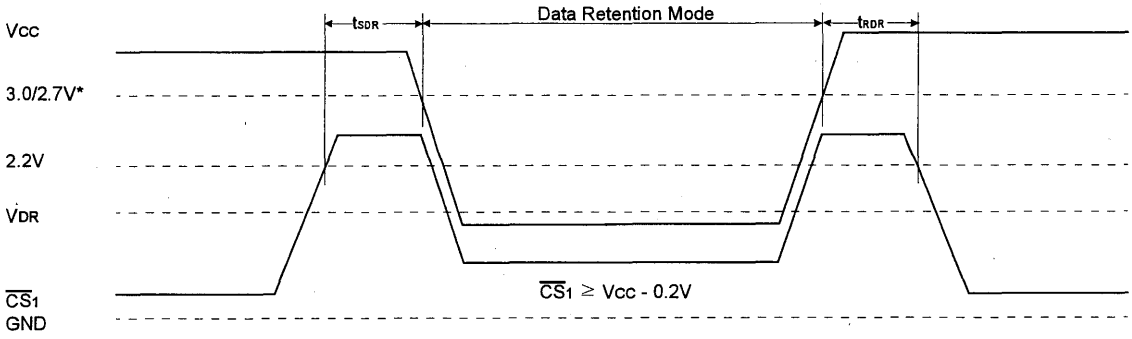
DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS_1}$***≥Vcc-2.0V		2.0	-	3.6	V
Data retention current	I_{DR}	KM68V2000L-L	Vcc=3.0V $\overline{CS_1}$≥Vcc-0.2V	LL-Ver	-	0.5	15	µA
		KM68V2000LI-L		LL-Ver	-	0.5	30	
		KM68U2000L-L		LL-Ver	-	0.5	15	
		KM68U2000LI-L		LL-Ver	-	0.5	30	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

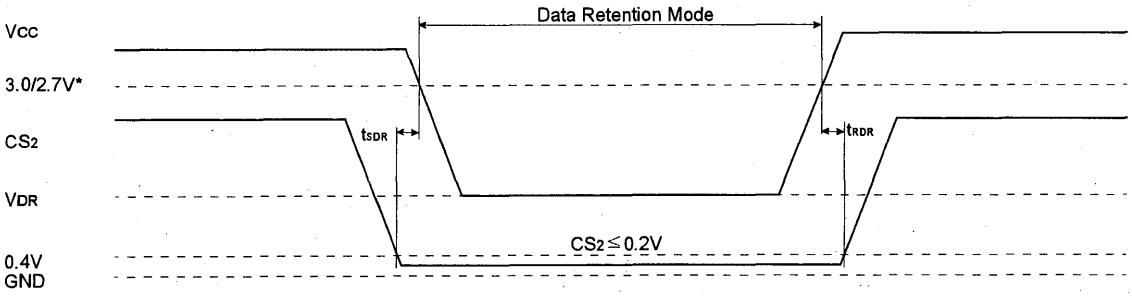
* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** Ta=25℃
*** $\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V($\overline{CS_1}$ controlled) or CS_2≤0.2V(CS_2 controlled)

DATA RETENTION WAVE FORM

1) $\overline{CS_1}$ controlled



2) CS_2 controlled

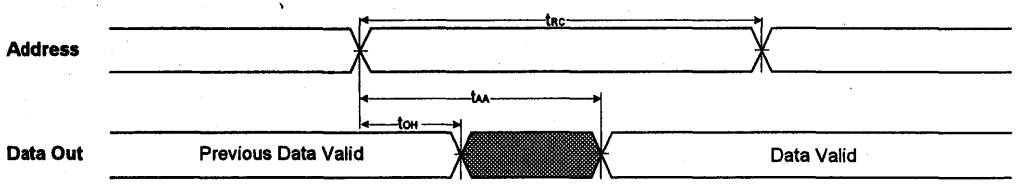


*3.0V for KM68V2000 family, 2.7V KM68U2000 family

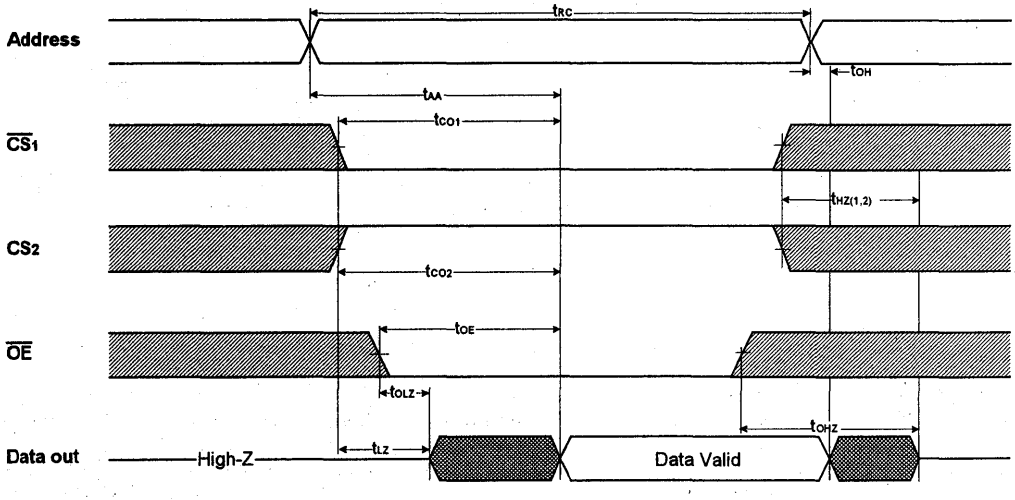
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



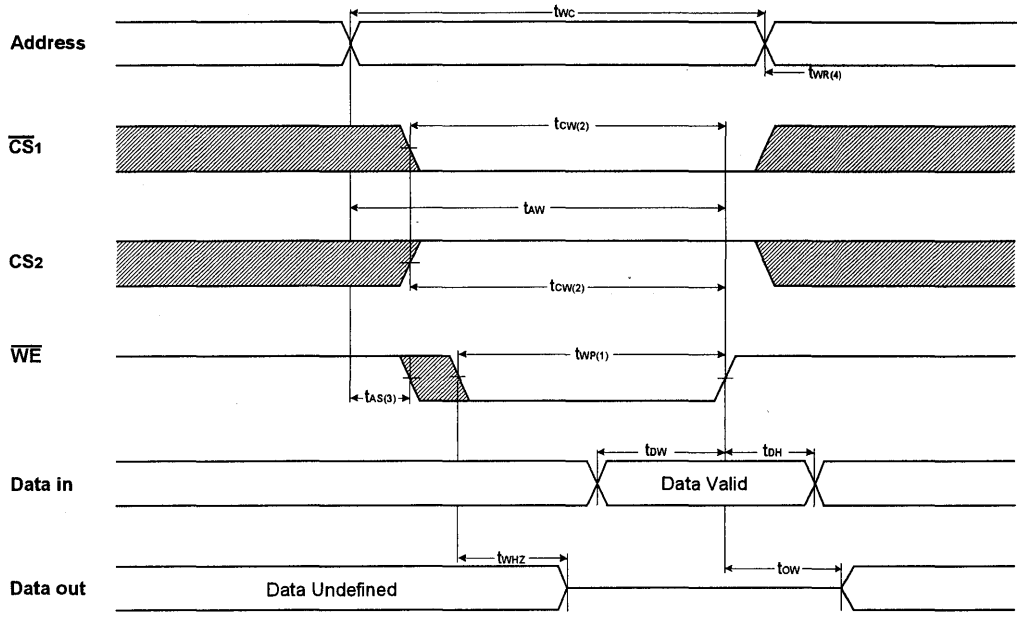
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



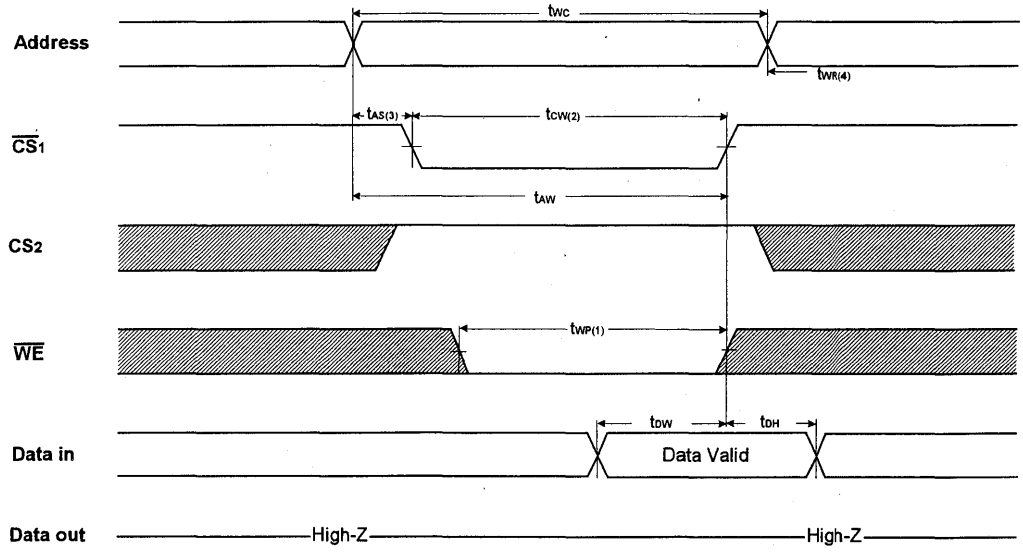
NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device interconnection.

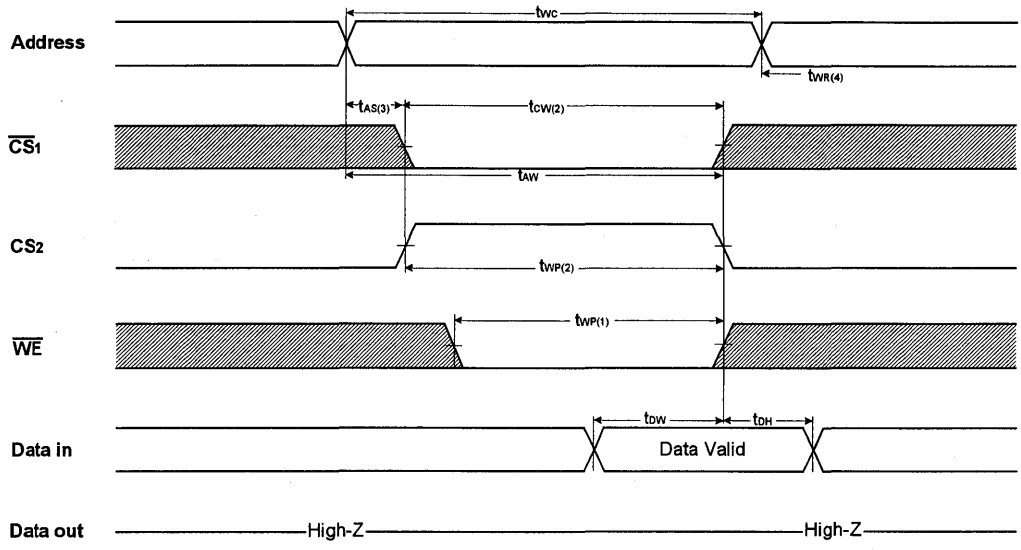
TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}_1$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS_1}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the begining of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR}(1)$ applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high $t_{WR}(2)$ applied in case a write ends as CS_2 going to low.

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Current Mode
H	X	X	X	Power Down	High-Z	I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	Dout	I_{CC}
L	H	L	X	Write	Din	I_{CC}

* X means don't care (Must be in high or low states)

512Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : 0.4μm CMOS
- Organization : 512Kx8
- Power Supply Voltage
  KM68V4000A Family : 3.3 ± 0.3V
  KM68U4000A Family : 3.0 ± 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-SOP, 32-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

The KM68V4000A and KM68U4000A family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

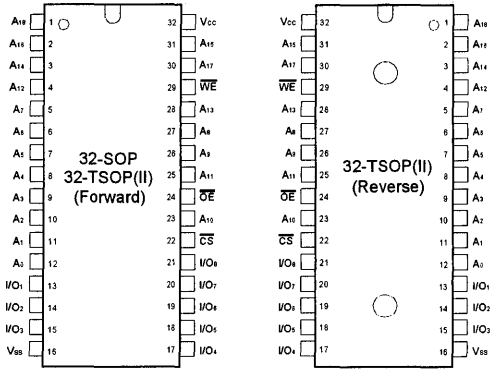
2

PRODUCT FAMILY

Product List	Operating Temp.	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM68V4000AL KM68V4000AL-L KM68V4000ALI LM68V4000ALI-L	Commercial (0~70℃)	3.0~3.6V	70*/85*/100	50/15μA	50mA	32-SOP 32-TSOP(II)-R/F
	Industrial (-40~85℃)	3.0~3.6V	70*/85*/100	50/20μA		
KM68U4000AL KM68U4000ALI-L KM68U4000ALI KM68U4000ALI-L	Commercial (0~70℃)	2.7~3.3V	70*/85*/100	30/10μA		
	Industria (-40~85℃)	2.7~3.3V	70*/85*/100	30/15μA		

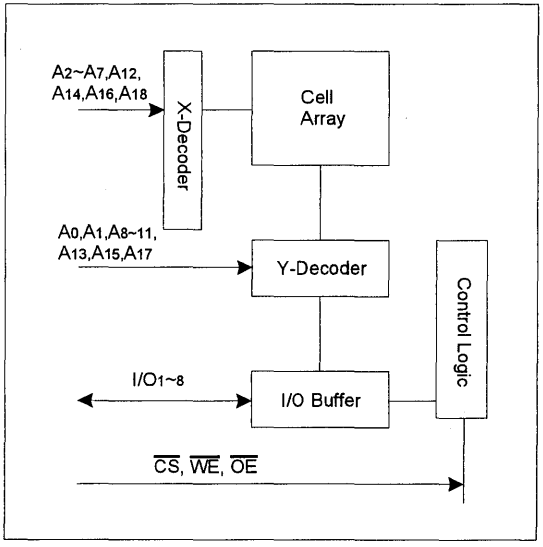
* The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
A0~A18	Address Inputs	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
$\overline{CS}$	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input		

FUNCTIONAL BLOCK DIAGRAM



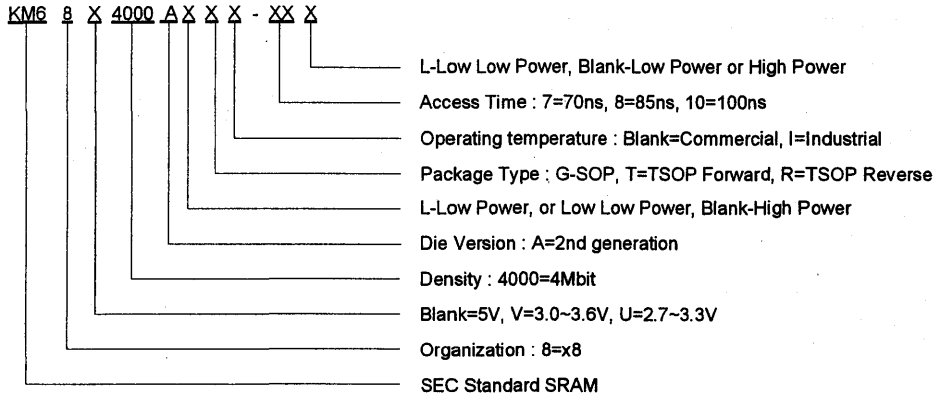
SAMSUNG ELECTRONICS

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Industrial Temp Products (-40~85℃)	
Part Name	Function	Part Name	Function
KM68V4000ALT-7	32-SOP, 70ns, 3.3V,L	KM68V4000ALG-7	32-SOP, 70ns, 3.3V,L
KM68V4000ALT-7L	32-SOP, 70ns, 3.3V,LL	KM68V4000ALG-7L	32-SOP, 70ns, 3.3V,LL
KM68V4000ALT-8	32-SOP, 85ns, 3.3V,L	KM68V4000ALG-8	32-SOP, 85ns, 3.3V,L
KM68V4000ALT-8L	32-SOP, 85ns, 3.3V,LL	KM68V4000ALG-8L	32-SOP, 85ns, 3.3V,LL
KM68V4000ALT-10	32-SOP, 100ns, 3.3V,L	KM68V4000ALG-10	32-SOP, 100ns, 3.3V,L
KM68V4000ALT-10L	32-SOP, 100ns, 3.3V,LL	KM68V4000ALG-10L	32-SOP, 100ns, 3.3V,LL
KM68V4000ALT-7L	32-TSOP(II)F, 70ns, 3.3V,LL	KM68V4000ALT-7L	32-TSOP(II)F, 70ns, 3.3V,LL
KM68V4000ALT-8L	32-TSOP(II)F, 85ns, 3.3V,LL	KM68V4000ALT-8L	32-TSOP(II)F, 85ns, 3.3V,LL
KM68V4000ALT-10L	32-TSOP(II)F, 100ns, 3.3V,LL	KM68V4000ALT-10L	32-TSOP(II)F, 100ns, 3.3V,LL
KM68V4000ALR-7L	32-TSOP(II)R, 70ns, 3.3V,LL	KM68V4000ALR-7L	32-TSOP(II)R, 70ns, 3.3V,LL
KM68V4000ALR-8L	32-TSOP(II)R, 85ns, 3.3V,LL	KM68V4000ALR-8L	32-TSOP(II)R, 85ns, 3.3V,LL
KM68V4000ALR-10L	32-TSOP(II)R, 100ns, 3.3V,LL	KM68V4000ALR-10L	32-TSOP(II)R, 100ns, 3.3V,LL
KM68U4000ALG-7	32-SOP, 70ns, 3.0V,L	KM68U4000ALGI-7	32-SOP, 70ns, 3.0V,L
KM68U4000ALG-7L	32-SOP, 70ns, 3.0V,LL	KM68U4000ALGI-7L	32-SOP, 70ns, 3.0V,LL
KM68U4000ALG-8	32-SOP, 85ns, 3.0V,L	KM68U4000ALGI-8	32-SOP, 85ns, 3.0V,L
KM68U4000ALG-8L	32-SOP, 85ns, 3.0V,LL	KM68U4000ALGI-8L	32-SOP, 85ns, 3.0V,LL
KM68U4000ALG-10	32-SOP, 100ns, 3.0V,L	KM68U4000ALGI-10	32-SOP, 100ns, 3.0V,L
KM68U4000ALG-10L	32-SOP, 100ns, 3.0V,LL	KM68U4000ALGI-10L	32-SOP, 100ns, 3.0V,LL
KM68U4000ALT-7L	32-TSOP(II)F, 70ns, 3.0V,LL	KM68U4000ALTI-7L	32-TSOP(II)F, 70ns, 3.0V,LL
KM68U4000ALT-8L	32-TSOP(II)F, 85ns, 3.0V,LL	KM68U4000ALTI-8L	32-TSOP(II)F, 85ns, 3.0V,LL
KM68U4000ALT-10L	32-TSOP(II)F, 100ns, 3.0V,LL	KM68U4000ALTI-10L	32-TSOP(II)F, 100ns, 3.0V,LL
KM68U4000ALR-7L	32-TSOP(II)R, 70ns, 3.0V,LL	KM68U4000ALRI-7L	32-TSOP(II)R, 70ns, 3.0V,LL
KM68U4000ALR-8L	32-TSOP(II)R, 85ns, 3.0V,LL	KM68U4000ALRI-8L	32-TSOP(II)R, 85ns, 3.0V,LL
KM68U4000ALR-10L	32-TSOP(II)R, 100ns, 3.0V,LL	KM68U4000ALRI-10L	32-TSOP(II)R, 100ns, 3.0V,LL

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	0.7	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM68V4000AL/L-L KM68U4000AL/L-L
		-40 to 85	℃	KM68V4000ALI/LI-L KM68U4000ALI/LI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V4000A Family KM68U4000A Family	3.0 2.7	3.3 3.0	3.6 3.3	V V
Ground	Vss	All Family	0	0	0	V
Input high voltage	V_{IH}	KM68V4000A Family KM68U4000A Family	2.2 2.2	- -	Vcc+0.3 Vcc+0.3	V V
Input low voltage	V_{IL}	KM68V4000A Family KM68U4000A Family	-0.3*** -0.3***	- -	0.4 0.4	V V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	Vin=0V	-	8	pF
Input/Output capacitance	C_{IO}	Vio=0V	-	10	pF

* Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA	Read	-	-	10	mA
				Write	-	-	20	
Average operatingcurrent		I_{CC1}	Cycle time=1μs 100% duty, I_{IO}=0mA $\overline{CS}$≤0.2V, V_{IL}≤0.2V, V_{IH}≥Vcc-0.2V	Read	-	-	10	mA
				Write	-	-	20	
		I_{CC2}	Min cycle, 100% duty $\overline{CS}$=V_{IL}, I_{IO}=0mA, V_{IN}=V_{IH} or V_{IL}		-	-	50	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.2	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS}$=V_{IH}		-	-	0.5	mA
Standby Current (CMOS)	KM68V4000AL KM68V4000AL-L	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, Others=0~Vcc	Low Power Low Low Power	-	-	50 15	μA μA
	KM68V4000ALI KM68V4000ALI-L			Low Power Low Low Power	-	-	50 20	μA μA
	KM68U4000AL KM68U4000AL-L			Low Power Low Low Power	-	-	30 10	μA μA
	KM68U4000ALI KM68U4000ALI-L			Low Power Low Low Power	-	-	30 15	μA μA

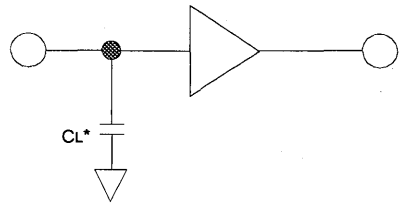
* 1) Commercial Product : T_A=0 to 70℃, Vcc=3.3±0.3V (68V4000A Family), Vcc=3.0±0.3V (68U4000A Family)
2) Industrial Product : T_A=-40 to 85℃, Vcc=3.3±0.3V (68V4000AI Family), Vcc=3.0±0.3V (68U4000AI Family)
** T_A=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rising and falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL **C_L=30pF+1TTL	-

* See DC Operating conditions
** KM68V4000A-7/KM68V4000A-8 Family, KM68U4000A-7/KM68U4000A-8 Family



* Including scope and jig capacitance

SAMSUNG ELECTRONICS

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V4000AL/L-L	0~70℃	3.3V ± 0.3	70*/85*/100ns	Commercial
KM68V4000ALI/LI-L	-40~85℃	3.3V ± 0.3	70*/85*/100ns	Industrial
KM68U4000AL/L-L	0~70℃	2.7V ± 0.3	70*/85*/100ns	Commercial
KM68U4000AL/LII-L	-40~85℃	2.7V ± 0.3	70*/85*/100ns	Industrial

* All the parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			*70ns		*85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	55	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

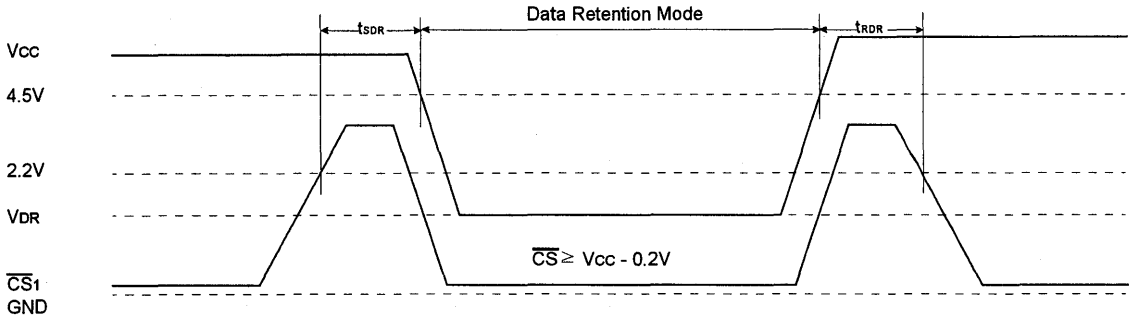
* The parameter is measured with 30pF test load.

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS} \geq$ Vcc-2.0V		2.0	-	3.6	V
Data retention current	I_{DR}	KM68V4000AL/L-L	Vcc=3.0V $\overline{CS} \geq$ Vcc-0.2V	L-Ver LL-Ver	- -	1 0.5	30 15	μA
		KM68V4000ALI/LI-L		L-Ver LL-Ver	- -	- -	30 20	
		KM68U4000AL/L-L		L-Ver LL-Ver	- -	1 0.5	30 10	
		KM68U4000ALI/LI-L		L-Ver LL-Ver	- -	- -	30 15	
Data retention set-up time	t_{SDR}		See data retention waveform		0	-	-	ms
Recovery time	t_{RDR}				5	-	-	

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** T_A=25℃

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

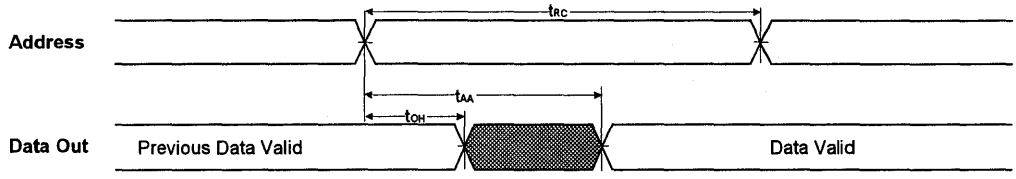
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Current Mode
H	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	Icc
L	H	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

* X means don't care (Must be in low or high state)

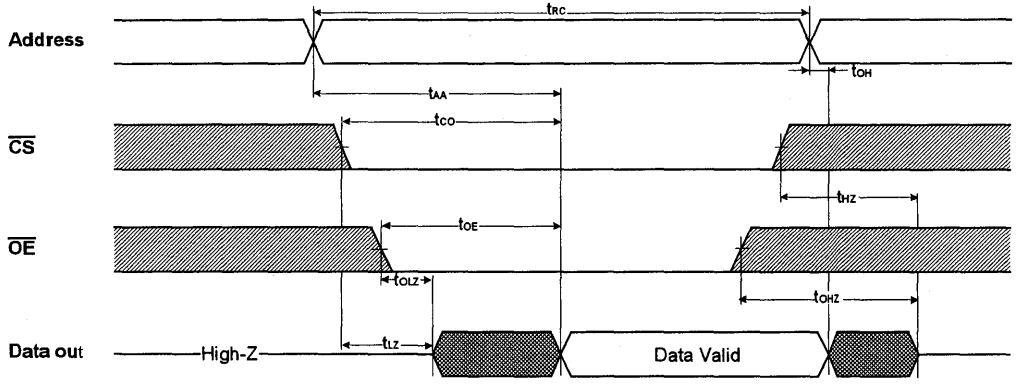
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



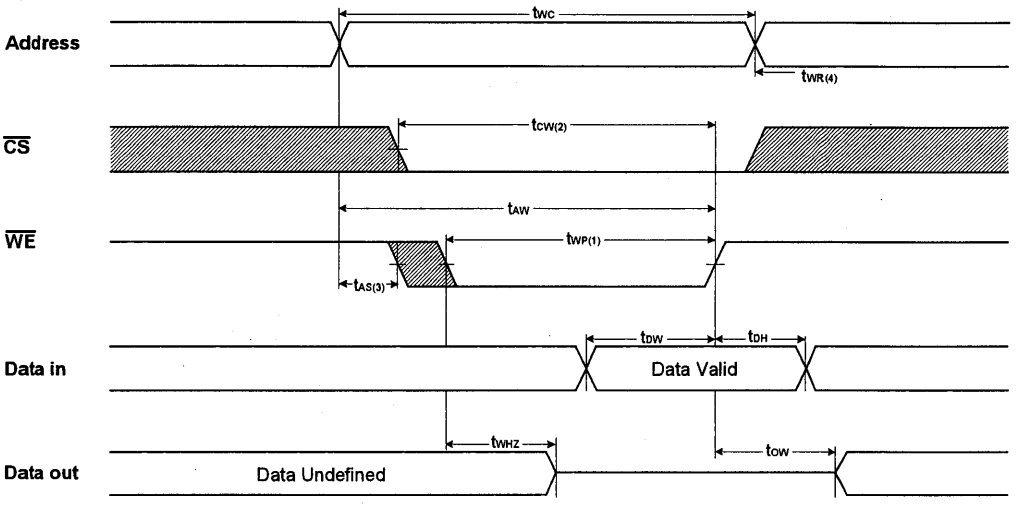
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



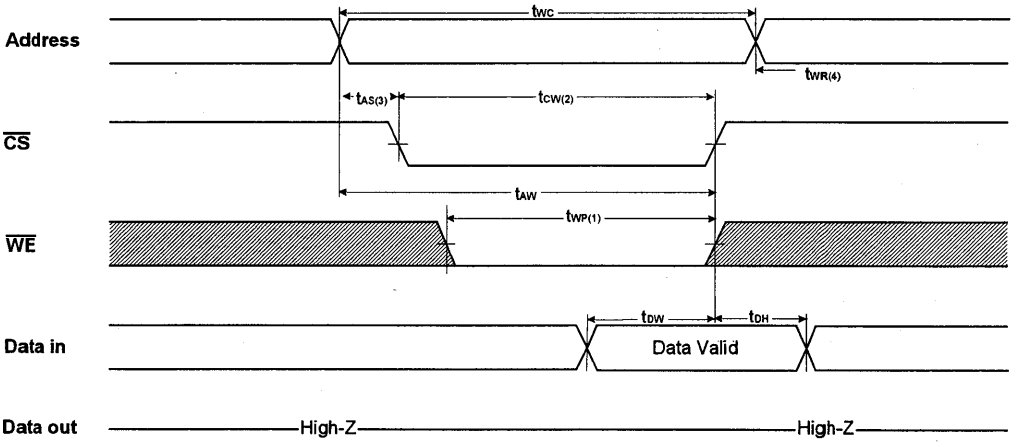
NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low CS and low WE. A write begins at the latest transition among CS goes low and WE going low : A write end at the earliest transition among CS going high and WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.

512Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : 0.4㎛ CMOS
- Organization : 512Kx8
- Power Supply Voltage
  KM68V4000B Family : 3.3 ± 0.3V
  KM68U4000B Family : 3.0 ± 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard 32-SOP,
  32-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

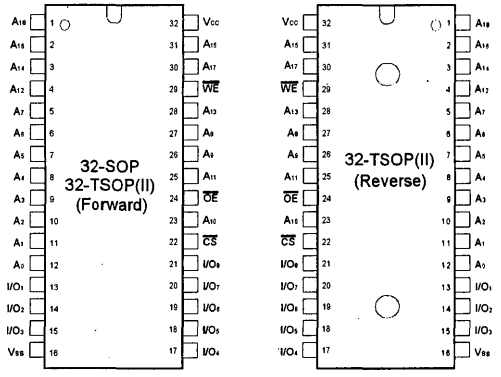
The KM68V4000B and KM68U4000B family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

2

PRODUCT FAMILY

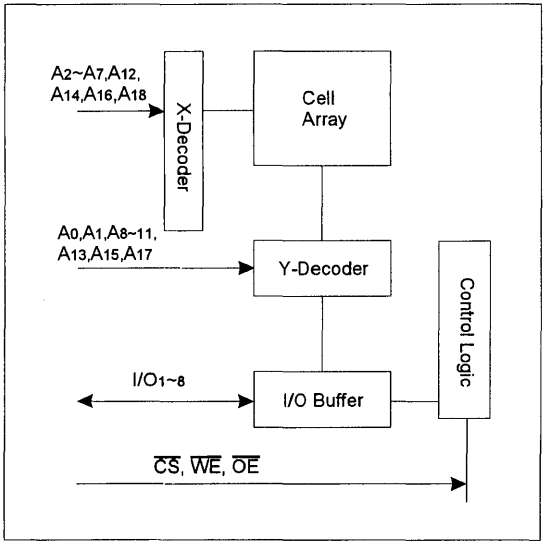
Product List	Operating Temp.	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM68V4000BL KM68V4000BL-L KM68V4000BLI LM68V4000BLI-L	Commercial (0~70℃)	3.0~3.6V	70*/85*/100	50/15㎂	50mA	32-SOP 32-TSOP(II)-R/F
	Industrial (-40~85℃)	3.0~3.6V	85*/100	50/20㎂		
KM68U4000BL KM68U4000BLI-L KM68U4000BLI KM68U4000BLI-L	Commercial (0~70℃)	2.7~3.3V	70*/85*/100	30/15㎂		
	Industria (-40~85℃)	2.7~3.3V	85*/100	30/20㎂		

PIN DESCRIPTION



Name	Function	Name	Function
A0~A18	Address Inputs	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
$\overline{CS}$	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input		

FUNCTIONAL BLOCK DIAGRAM



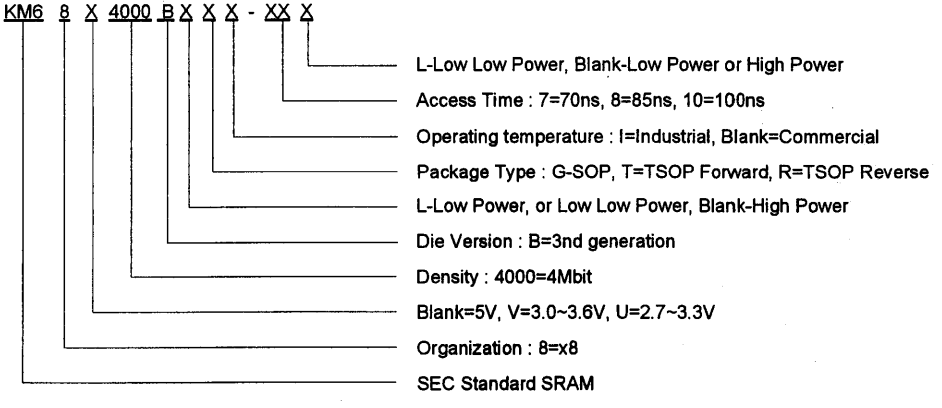
SAMSUNG ELECTRONICS

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Industrial Temp Products (-40~85℃)	
Part Name	**Function**	**Part Name**	**Function**
KM68V4000BLT-7	32-SOP, 70ns, 3.3V,L	KM68V4000BLGI-8	32-SOP, 85ns, 3.3V,L
KM68V4000BLT-7L	32-SOP, 70ns, 3.3V,LL	KM68V4000BLGI-8L	32-SOP, 85ns, 3.3V,LL
KM68V4000BLT-8	32-SOP, 85ns, 3.3V,L	KM68V4000BLGI-10	32-SOP, 100ns, 3.3V,L
KM68V4000BLT-8L	32-SOP, 85ns, 3.3V,LL	KM68V4000BLGI-10L	32-SOP, 100ns, 3.3V,LL
KM68V4000BLT-10	32-SOP, 100ns, 3.3V,L		
KM68V4000BLT-10L	32-SOP, 100ns, 3.3V,LL	KM68V4000BLTI-8	32-TSOP(II)F, 85ns, 3.3V,LL
		KM68V4000BLTI-8L	32-TSOP(II)F, 100ns, 3.3V,LL
KM68V4000BLT-7L	32-TSOP(II)F, 70ns, 3.3V,LL	KM68V4000BLRI-10	32-TSOP(II)R, 85ns, 3.3V,LL
KM68V4000BLT-8L	32-TSOP(II)F, 85ns, 3.3V,LL	KM68V4000BLRI-10L	32-TSOP(II)R, 100ns, 3.3V,LL
KM68V4000BLT-10L	32-TSOP(II)F, 100ns, 3.3V,LL		
KM68V4000BLR-7L	32-TSOP(II)R, 70ns, 3.3V,LL	KM68U4000BLGI-8	32-SOP, 85ns, 3.0V,L
KM68V4000BLR-8L	32-TSOP(II)R, 85ns, 3.3V,LL	KM68U4000BLGI-8L	32-SOP, 85ns, 3.0V,LL
KM68V4000BLR-10L	32-TSOP(II)R, 100ns, 3.3V,LL	KM68U4000BLGI-10	32-SOP, 100ns, 3.0V,L
		KM68U4000BLGI-10L	32-SOP, 100ns, 3.0V,LL
KM68U4000BLG-7	32-SOP, 70ns, 3.0V,L		
KM68U4000BLG-7L	32-SOP, 70ns, 3.0V,LL	KM68U4000BLTI-8	32-TSOP(II)F, 85ns, 3.0V,LL
KM68U4000BLG-8	32-SOP, 85ns, 3.0V,L	KM68U4000BLTI-8L	32-TSOP(II)F, 100ns, 3.0V,LL
KM68U4000BLG-8L	32-SOP, 85ns, 3.0V,LL	KM68U4000BLRI-10	32-TSOP(II)R, 85ns, 3.0V,LL
KM68U4000BLG-10	32-SOP, 100ns, 3.0V,L	KM68U4000BLRI-10L	32-TSOP(II)R, 100ns, 3.0V,LL
KM68U4000BLG-10L	32-SOP, 100ns, 3.0V,LL		
KM68U4000BLT-7L	32-TSOP(II)F, 70ns, 3.0V,LL		
KM68U4000BLT-8L	32-TSOP(II)F, 85ns, 3.0V,LL		
KM68U4000BLT-10L	32-TSOP(II)F, 100ns, 3.0V,LL		
KM68U4000BLR-7L	32-TSOP(II)R, 70ns, 3.0V,LL		
KM68U4000BLR-8L	32-TSOP(II)R, 85ns, 3.0V,LL		
KM68U4000BLR-10L	32-TSOP(II)R, 100ns, 3.0V,LL		

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	0.7	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM68V4000BL/L-L KM68U4000BL/L-L
		-40 to 85	℃	KM68V4000BLI/LI-L KM68U4000BLI/LI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68V4000B Family KM68U4000B Family	3.0 2.7	3.3 3.0	3.6 3.3	V V
Ground	Vss	All Family	0	0	0	V
Input high voltage	V_{IH}	KM68V4000B Family KM68U4000B Family	2.2 2.2	- -	Vcc+0.3 Vcc+0.3	V V
Input low voltage	V_{IL}	KM68V4000B Family KM68U4000B Family	-0.3*** -0.3***	- -	0.4 0.4	V V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	Vin=0V	-	8	pF
Input/Output capacitance	C_{IO}	Vio=0V	-	10	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or V_{IL}, Vio=Vss to Vcc		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA	Read	-	-	10	mA
				Write	-	-	20	
Average operating current		I_{CC1}	Cycle time=1μs 100%duty $\overline{CS}$≤0.2V, V_{IL}≤0.2V,	Read	-	-	10	mA
				Write	-	-	20	
		I_{CC2}	Min cycle, 100%duty, I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}		-	-	50	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.2	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS}$=V_{IH}		-	-	0.5	mA
Standby Current (CMOS)	KM68V4000BL KM68V4000BL-L	I_{SB1}	$\overline{CS}$≥ Vcc-0.2V, Others=0~Vcc	Low Power Low Low Power	-	-	50 15	μA μA
	KM68V4000BLI KM68V4000BLI-L			Low Power Low Low Power	-	-	50 20	μA μA
	KM68U4000BL KM68U4000BL-L			Low Power Low Low Power	-	-	30 15	μA μA
	KM68U4000BLI KM68U4000BLI-L			Low Power Low Low Power	-	-	30 20	μA μA

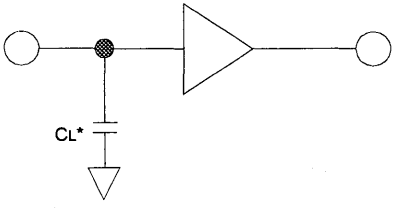
* 1) Commercial Product : T_A=0 to 70℃, Vcc=3.3±0.3V (68V4000B Family), Vcc=3.0±0.3V (68U4000B Family)
2) Industrial Product : T_A=-40 to 85℃, Vcc=3.3±0.3V (68V4000BI Family), Vcc=3.0±0.3V (68U4000BI Family)
** T_A=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rising and falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL **C_L=30pF+1TT	-

* See DC Operating conditions



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V4000BL/L-L	0~70℃	3.3V ± 0.3	70*/85*/100ns	Commercial
KM68V4000BLI/LI-L	-40~85℃	3.3V ± 0.3	85*/100ns	Industrial
KM68U4000BL/L-L	0~70℃	3.0V ± 0.3	70*/85*/100ns	Commercial
KM68U4000BLI/LI-L	-40~85℃	3.0V ± 0.3	85*/100ns	Industrial

* All the parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			*70ns		*85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	55	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

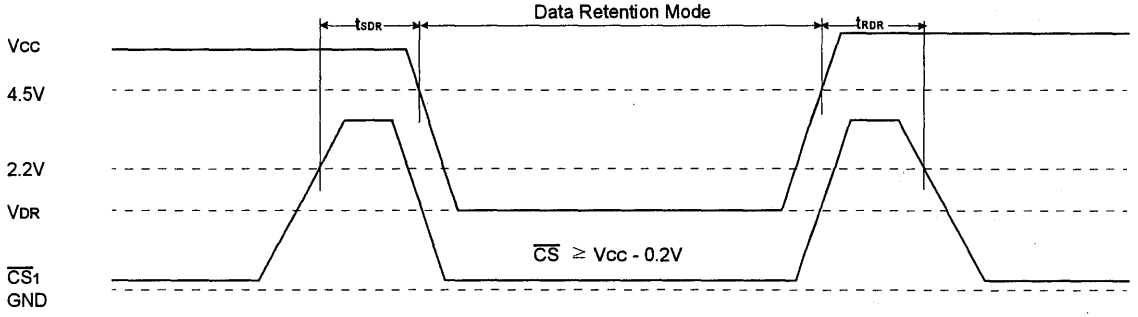
* All the parameters are measured with 30pF test load

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS} \geq$ Vcc-0.2.0V		2.0	-	3.6	V
Data retention current	I_{DR}	KM68V4000BL/L-L	Vcc=3.0V $\overline{CS} \geq$ Vcc-0.2V	L-Ver LL-Ver	- -	1 0.5	30 15	µA
		KM68V4000BLI/LI-L		L-Ver LL-Ver	- -	- -	30 20	
		KM68U4000BL/L-L		L-Ver LL-Ver	- -	1 0.5	30 15	
		KM68U4000BLI/LI-L		L-Ver LL-Ver	- -	- -	30 20	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** T_A=25℃

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

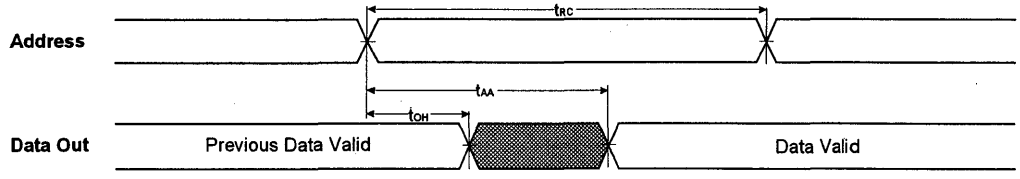
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Current Mode
H	X	X	Power Down	High-Z	I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	Dout	I_{CC}
L	L	X	Write	Din	I_{CC}

* X means don't care (Must be in low or high state)

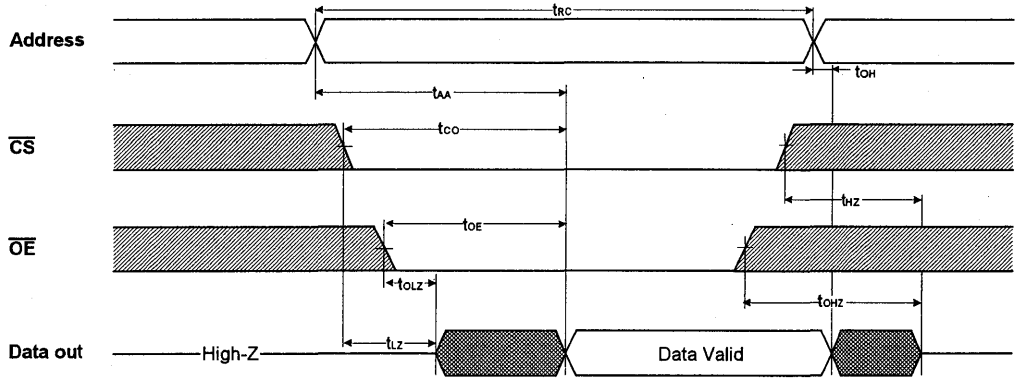
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



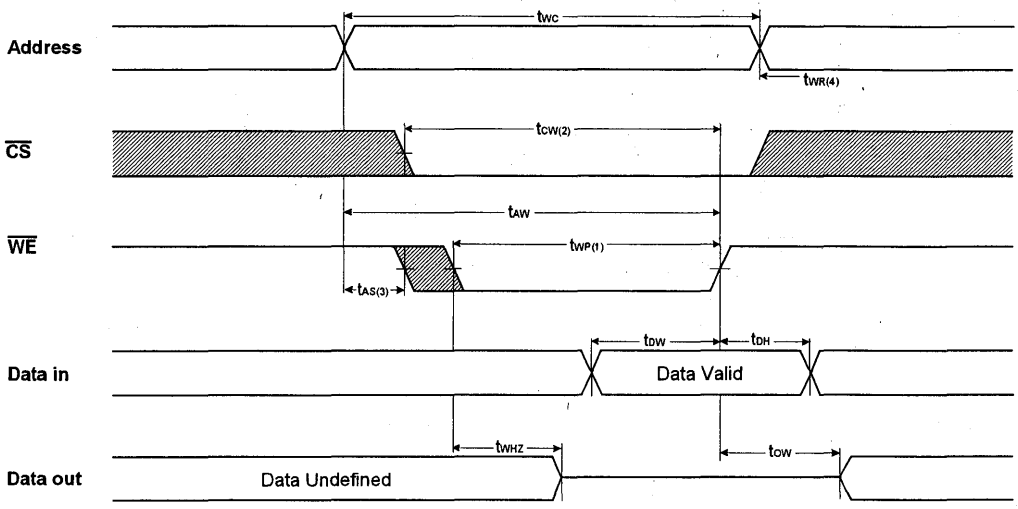
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



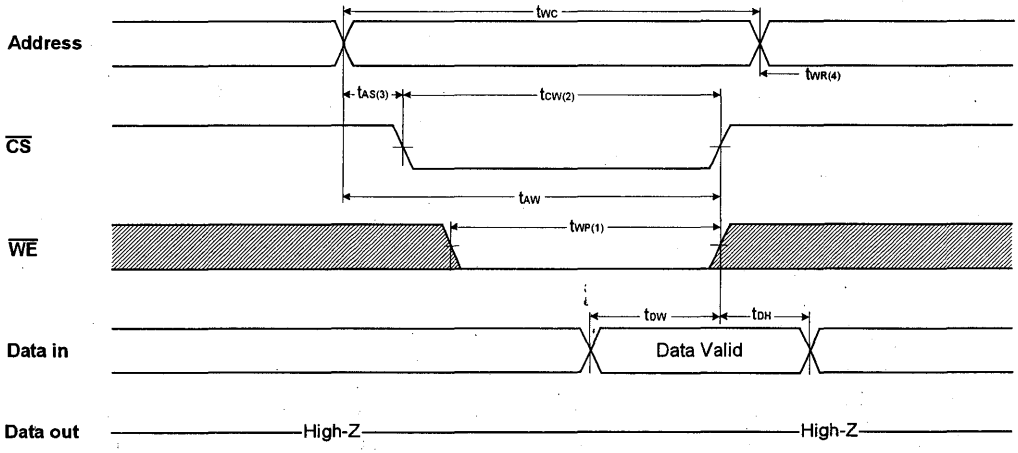
NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ goes low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

512Kx8 bit Low Power and Low Voltage CMOS SRAM with 48-CSP(Chip Size Package)

FEATURES

- Process Technology : 0.4μm CMOS
- Organization : 512Kx8
- Power Supply Voltage
  KM68V4000BZ Family : 3.3V±0.3V
  KM68U4000BZ Family : 3.0V±0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM68V4000BZ and KM68U4000BZ family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very samll from factor with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temp.Range	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Operating (I_{CC2})	Standby (I_{SB1})	
KM68V4000BLZ-L	Commercial (0~70℃)	3.0~3.6V	85	70mA(Max)	15μA (max)	48-CSP (6x8 ball area with 0.75mm ball pitch)
KM68U4000BLZ-L		2.7~3.3V	100	70mA(Max)		
KM68V4000BLI-L	Industria (-40~85℃)	3.0~3.6V	85	70mA(Max)	20μA (max)	
KM68U4000BLI-L		2.7~3.3V	100	70mA(Max)		

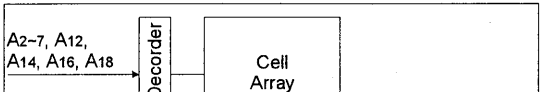
* The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
A	A_0	A_1	CS_2	A_3	A_6	A_8
B	I/O_5	A_2	$\overline{WE}$	A_4	A_7	I/O_1
C	I/O_6		NC	A_5		I/O_2
D	V_{SS}					V_{CC}
E	V_{CC}					V_{SS}
F	I/O_7		A_{18}	A_{17}		I/O_3
G	I/O_8	$\overline{OE}$	$\overline{CS_1}$	A_{16}	A_{15}	I/O_4
H	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}

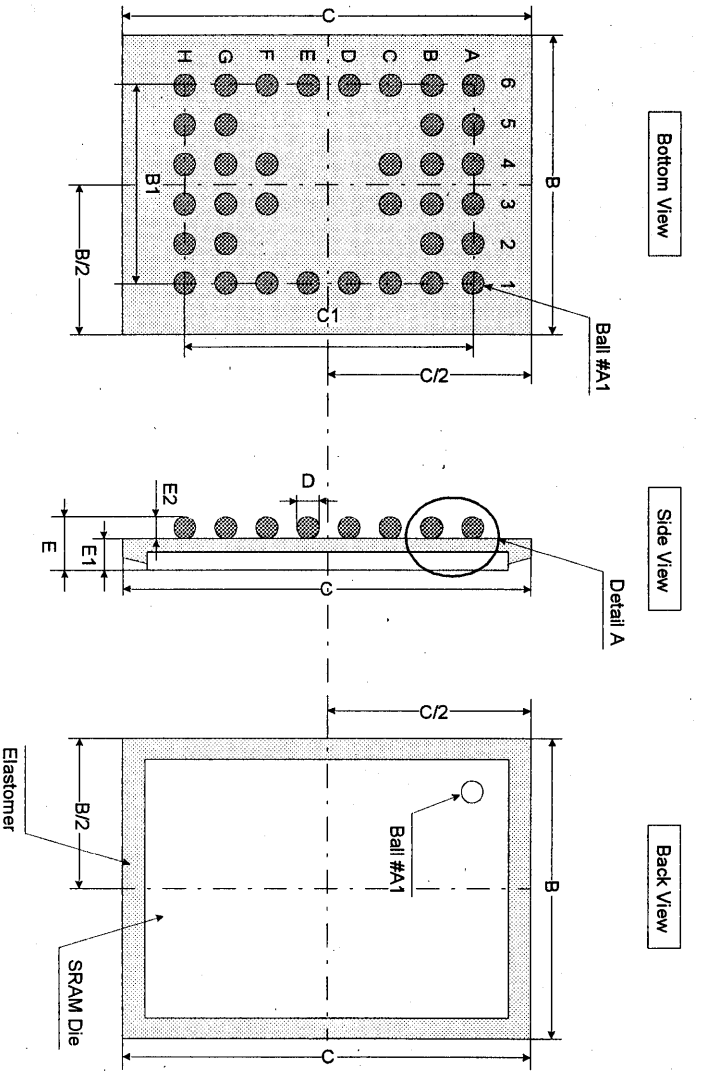
* See last page for package dimension.

FUNCTIONAL BLOCK DIAGRAM

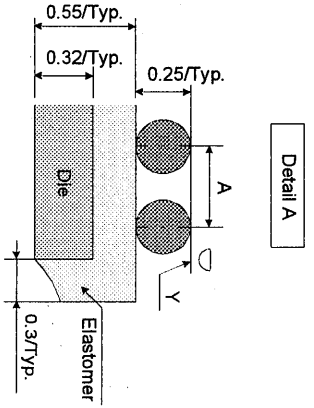


Name	Function	Name	Function
A_0~A_{18}	Address Inputs	V_{CC}	Power
$\overline{WE}$	Write Enable Input	V_{SS}	Ground
$\overline{CS}$	Chip Select Input	I/O_1~I/O_8	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input		

PACKAGE DIMENSIONS (Units : mm)



	Min	Typ	Max
A	-	0.75	-
B	7.10	7.20	7.30
B1	-	3.75	-
C	11.55	11.65	11.75
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08



Notes.

1. Bump counts : 48(8row x 6row)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is copianarity : 0.08(max)

256Kx16 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : 0.4μm CMOS
- Organization : 256K x16
- Power Supply Voltage
  KM68V4000B Family : 3.3 ± 0.3V
  KM68U4000B Family : 3.0 ± 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  44-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

The KM616V4000B and KM616U4000B family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

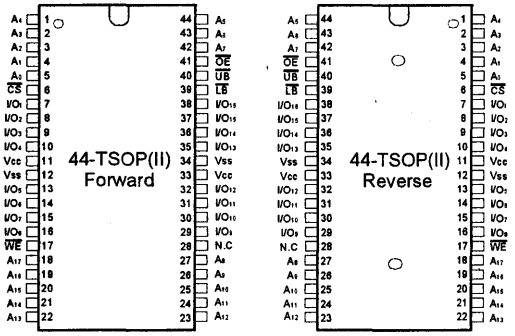
2

PRODUCT FAMILY

Product List	Operating Temp.	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM616V4000BL-L	Commercial(0~7℃)	3.0~3.6V	70*/85*/100	15μA	70mA	44-TSOP(II)-R/F
KM616V4000BLI-L	Industrial(-40~85℃)	3.0~3.6V	70*/85*/100	20μA		
KM616U4000BL-L	Commercial(0~7℃)	2.7~3.3V	70*/85*/100	15μA		
KM616U4000BLI-L	Industrial(-40~85℃)	2.7~3.3V	70*/85*/100	20μA		

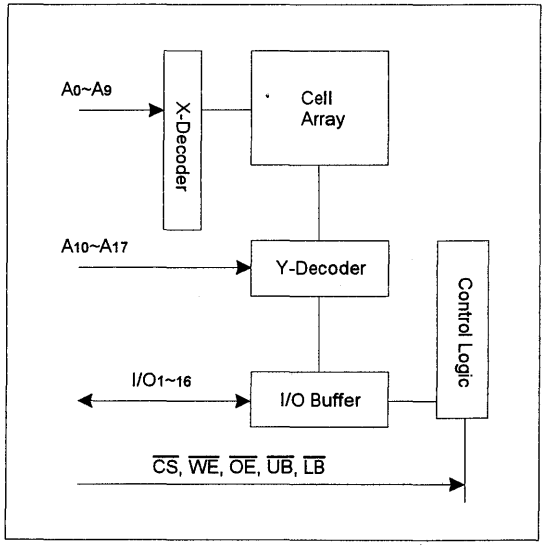
* The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
A0~A17	Address Inputs	$\overline{LB}$	Lower Byte (I/O1~8)
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O9~16)
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
I/O1~I/O16	Data Input/Output	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM

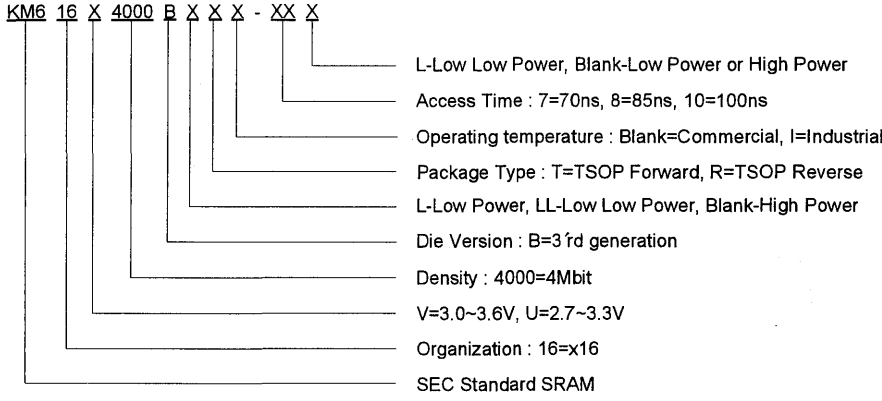


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70℃)		Industrial Temp Products (-40~85℃)	
Part Name	**Function**	**Part Name**	**Function**
KM616V4000BLT-7L	44-TSOP(II)F, 70ns, 3.3V,LL	KM616V4000BLTI-7L	44-TSOP(II)F, 70ns, 3.3V,LL
KM616V4000BLT-8L	44-TSOP(II)F, 85ns, 3.3V,LL	KM616V4000BLTI-8L	44-TSOP(II)F, 85ns, 3.3V,LL
KM616V4000BLT-10L	44-TSOP(II)F, 100ns, 3.3V,LL	KM616V4000BLTI-10L	44-TSOP(II)F, 100ns, 3.3V,LL
KM616V4000BLR-7L	44-TSOP(II)R, 70ns, 3.3V,LL	KM616V4000BLRI-7L	44-TSOP(II)R, 70ns, 3.3V,LL
KM616V4000BLR-8L	44-TSOP(II)R, 85ns, 3.3V,LL	KM616V4000BLRI-8L	44-TSOP(II)R, 85ns, 3.3V,LL
KM616V4000BLR-10L	44-TSOP(II)R, 100ns, 3.3V,LL	KM616V4000BLRI-10L	44-TSOP(II)R, 100ns, 3.3V,LL
KM616U4000BLT-7L	44-TSOP(II)F, 70ns, 3.0V,LL	KM616U4000BLTI-7L	44-TSOP(II)F, 70ns, 3.0V,LL
KM616U4000BLT-8L	44-TSOP(II)F, 85ns, 3.0V,LL	KM616U4000BLTI-8L	44-TSOP(II)F, 85ns, 3.0V,LL
KM616U4000BLT-10L	44-TSOP(II)F, 100ns, 3.0V,LL	KM616U4000BLTI-10L	44-TSOP(II)F, 100ns, 3.0V,LL
KM616U4000BLR-7L	44-TSOP(II)R, 70ns, 3.0V,LL	KM616U4000BLRI-7L	44-TSOP(II)R, 70ns, 3.0V,LL
KM616U4000BLR-8L	44-TSOP(II)R, 85ns, 3.0V,LL	KM616U4000BLRI-8L	44-TSOP(II)R, 85ns, 3.0V,LL
KM616U4000BLR-10L	44-TSOP(II)R, 100ns, 3.0V,LL	KM616U4000BLRI-10L	44-TSOP(II)R, 100ns, 3.0V,LL

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	0.7	W	-
Storage temperature	T_{STG}	-65 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM616V4000BL-L KM616U4000BL-L
		-40 to 85	℃	KM616V4000BLI-L KM616U4000BLI-L
Soldering temperature and time	T_{SOLDER}	260℃, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM616V4000B Family KM616U4000B Family	3.0 2.7	3.3 3.0	3.6 3.3	V V
Ground	Vss	All Family	0	0	0	V
Input high voltage	V_{IN}	KM616V4000B Family KM616U4000B Family	2.2 2.2	- -	Vcc+0.3 Vcc+0.3	V V
Input low voltage	V_{IL}	KM616V4000B Family KM616U4000B Family	-0.3*** -0.3***	- -	0.4 0.4	V V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified
** T_A=25℃
*** V_{IL}(min)=-3.0V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	Vin=0V	-	8	pF
Input/Output capacitance	C_{IO}	Vio=0V	-	10	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IL}=Vss to Vcc		-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or V_{IL}		-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, V_{IL}=0mA	Read	-	-	10	mA
				Write	-	-	45	
Average operatingcurren		I_{CC1}	Cycle time=1μs 100% duty $\overline{CS}$≤0.2V, V_{IL}≤0.2V,	Read	-	-	10	mA
				Write	-	-	45	
		I_{CC2}	Min cycle, 100% duty, V_{IL}=0mA $\overline{CS}$=V_{IL}, V_{IL}=V_{IH} or V_{IL}		-	-	70	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.2	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS}$=V_{IH}		-	-	0.5	mA
Standby Current (CMOS)	KM616V4000BL-L	I_{SB1}	$\overline{CS}$≥ Vcc-0.2V, Others=0~Vcc	Low Low Power	-	-	15	μA
	KM616V4000BLI-L			Low Low Power	-	-	20	μA
	KM616U4000BL-L			Low Low Power	-	-	15	μA
	KM616U4000BLI-L			Low Low Power	-	-	20	μA

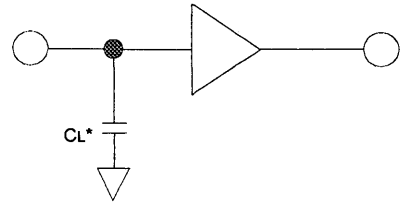
* 1) Commercial Product : T_A=0 to 70℃, Vcc=3.3±0.3V (616V4000B Family), Vcc=3.0±0.3V (616U4000B Family)
2) Industrial Product : T_A=-40 to 85℃, Vcc=3.3±0.3V (616V4000BI Family), Vcc=3.0±0.3V (616U4000BI Family)
** T_A=25℃

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rise fall time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C_L=100pF+1TTL **C_L=30pF+1TT	-

* See DC Operating conditions
** KM616V4000BL-7L/8L Family, KM616U4000BL-7L/8L Family



* Including scope and jig capacitance

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V4000BL-L	0~70℃	3.3V ± 0.3	70*/85*/100ns	Commercial
KM68V4000BLI-L	-40~85℃	3.3V ± 0.3	70*/85*/100ns	Industrial
KM68U4000BL-L	0~70℃	3.0V ± 0.3	70*/85*/100ns	Commercial
KM68U4000BLI-L	-40~85℃	3.0V ± 0.3	70*/85*/100ns	Industrial

* All the parameters are measured with 30pF test load.

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	$\overline{OE}$ disable to high-Z output	tOHZ	0	25	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	15	-	ns
	$\overline{LB}$, $\overline{UB}$ valid to data output	tBA	-	35	-	40	-	50	ns
Write	$\overline{UB}$, $\overline{LB}$ disable to high-Z output	tBHZ	0	25	0	25	0	30	ns
	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	55	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns
	$\overline{LB}$, $\overline{UB}$ valid to end of write	tBW	60	-	70	-	80	-	ns

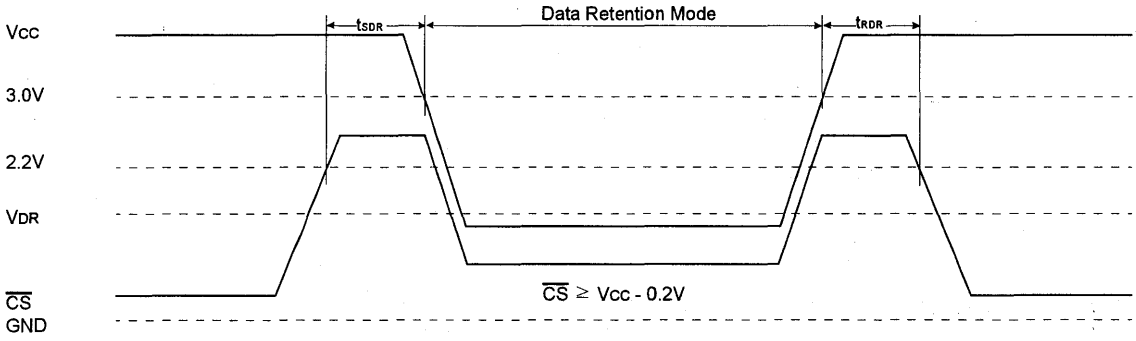
* All the parameters are measured with 30pF test load.

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS} \geq$ Vcc-0.2V		2.0	-	3.6	V
Data retention current	I_{DR}	KM68V4000BL-L	Vcc=3.0V $\overline{CS} \geq$ Vcc-0.2V	LL-Ver	-	0.5	15	µA
		KM68V4000BLI-L		LL-Ver	-	-	20	
		KM68U4000BL-L		LL-Ver	-	0.5	15	
		KM68U4000BLI-L		LL-Ver	-	-	20	
Data retention set-up time	t_{SDR}		See data retention waveform		0	-	-	ms
Recovery time	t_{RDR}				5	-	-	

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** T_A=25℃

DATA RETENTION WAVE FORM

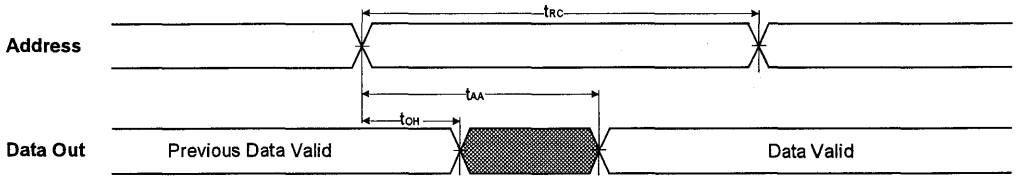


SAMSUNG ELECTRONICS

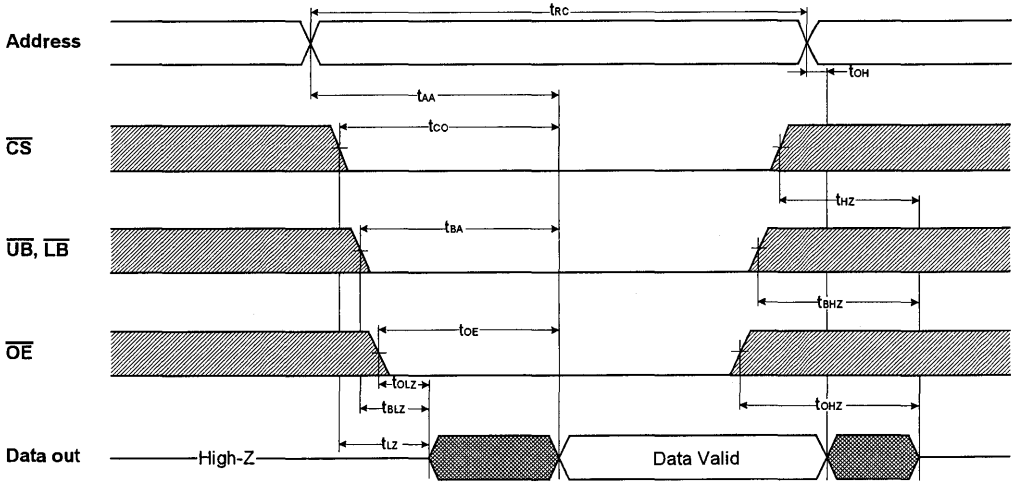
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$ or and $\overline{LB}$=V_{IL})



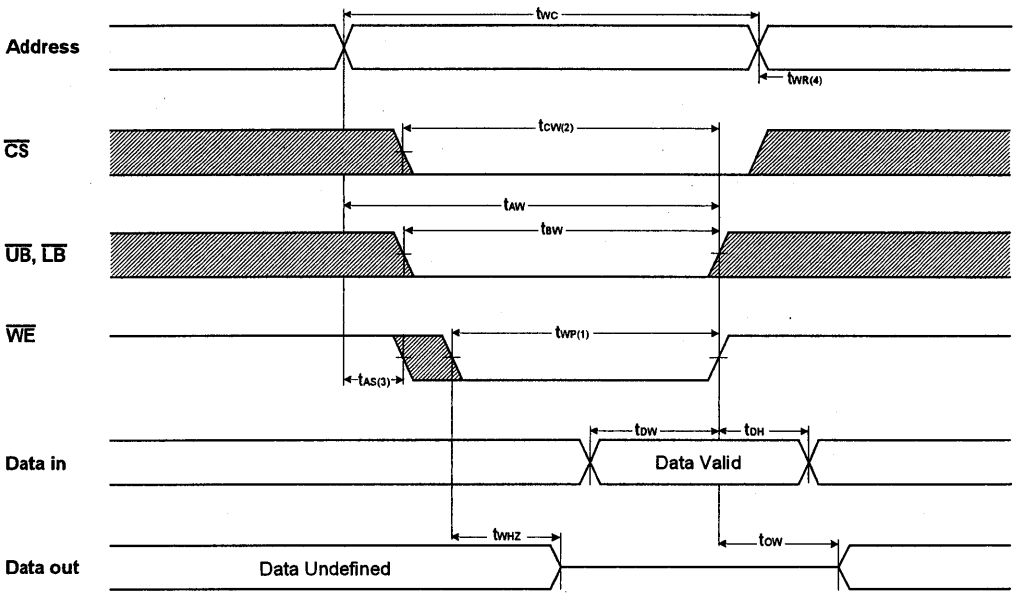
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



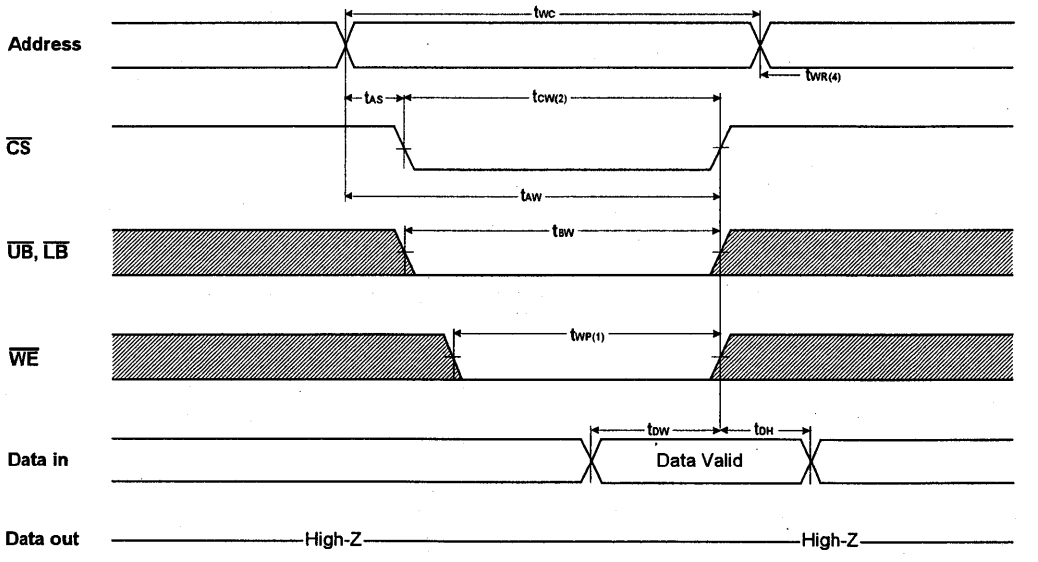
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.

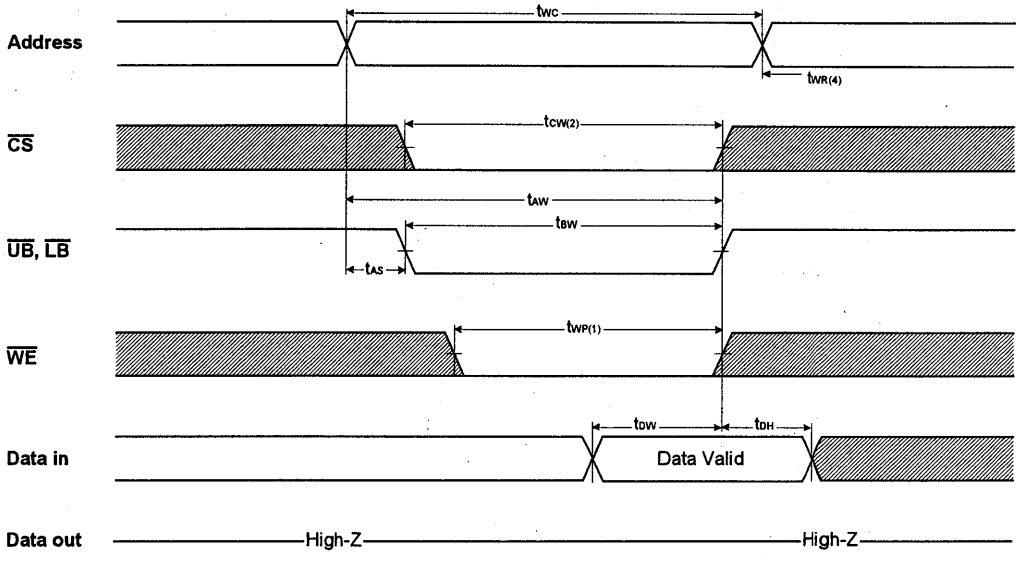
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultenious asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the $\overline{CS}$ going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end or write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{LB}$	$\overline{UB}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O1~8	I/O9~16	Current Mode
H	X	X	X	X	Not Select	High-Z	High-Z	ISB1
L	X	X	H	H	Output Disable	High-Z	High-Z	ICC
L	H	H	X	X		High-Z	High-Z	
L	L H L	H L L	H	L	Read	Dout High-Z Dout	High-Z Dout Dout	ICC
L	L H L	H L L	L	X	Write	Din High-Z Din	High Din Din	ICC

* X means don't care (Must be in low or high state)

256Kx16bit Low Power and Low Voltage CMOS SRAM with 48-CSP(Chip Size Package)

FEATURES

- Process Technology : 0.4μm CMOS
- Organization :256Kx16
- Power Supply Voltage
  KM616V4000BZ Family : 3.3V ± 0.3V
  KM616U4000BZ Family : 3.0V ± 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 48-CSP with 0.75 pitch

GENERAL DESCRIPTION

The KM616V4000BZ and KM616U4000BZ family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very samll from factor with 0.75 ball pitch and 6 x 8 ball array. he family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temp.Range	Vcc Range (min~max)	Speed(ns)	Power Dissipation		PKG Type
				Operating (Icc2)	Standby (Isb1)	
KM616V4000BLZ-L	Commercial (0~70℃)	3.0~3.6V	85	90mA(Max)	15μA (max)	48-CSP (6x8 ball area with 0.75mm ball pitch)
KM616U4000BLZ-L		1.8~2.7V	100	90mA(Max)		
KM616V4000BLZI-L	Industria (-40~85℃)	3.0~3.6V	85	90mA(Max)	20μA (max)	
KM616U4000BLZ--		2.7~3.3V	100	90mA(Max)		

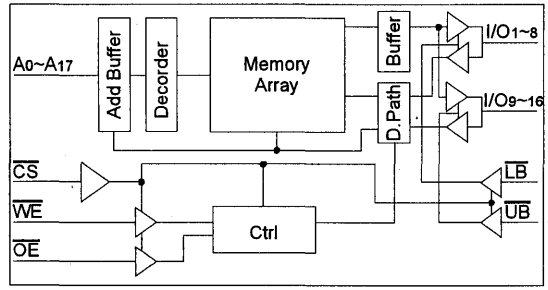
* The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_9	$\overline{UB}$	A_3	A_4	$\overline{CS}$	I/O_1
C	I/O_{10}	I/O_{11}	A_5	A_6	I/O_2	I/O_3
D	V_{SS}	I/O_{12}	A_{17}	A_7	I/O_4	V_{CC}
E	V_{CC}	I/O_{13}	NC	A_{16}	I/O_5	V_{SS}
F	I/O_{15}	I/O_{14}	A_{14}	A_{15}	I/O_6	I/O_7
G	I/O_{16}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_8
H	NC	A_8	A_9	A_{10}	A_{11}	NC

* See last page for package dimension.

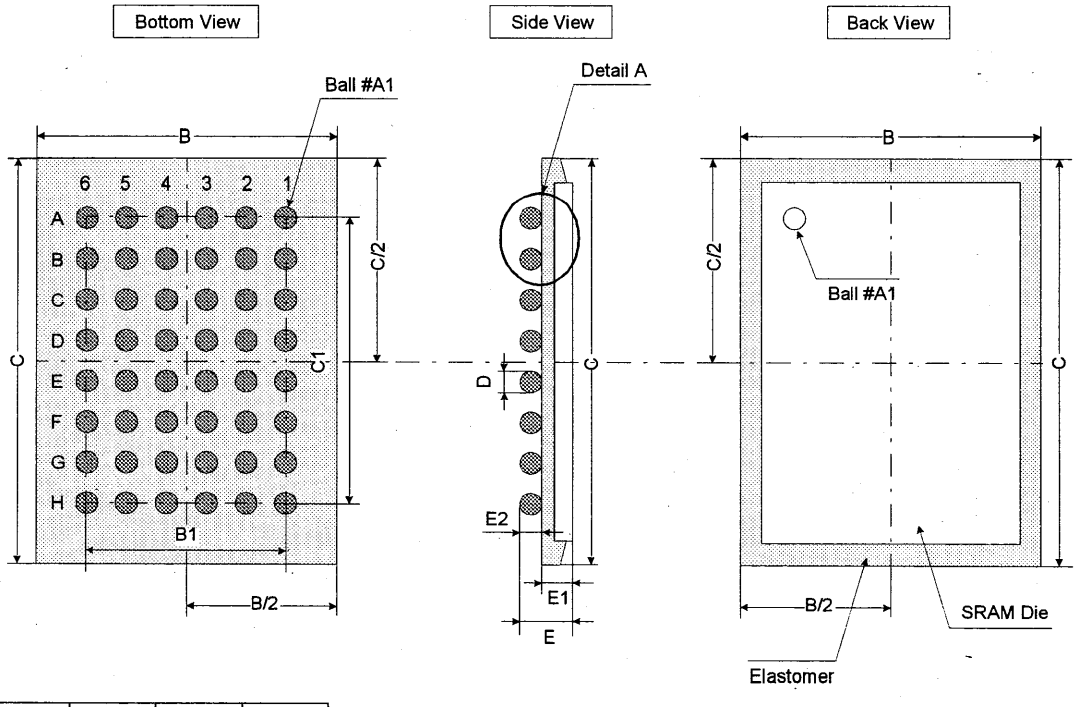
FUNCTIONAL BLOCK DIAGRAM



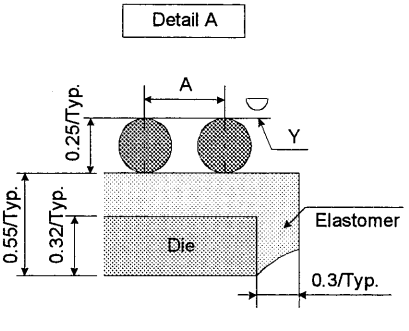
Name	Function	Name	Function
A_0~A_{17}	Address Inputs	$\overline{LB}$	Lower Byte(I/O_1 ~ 8)
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O_9 ~ 16)
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
I/O_1~I/O_{16}	Data Inputs/Outputs	N.C.	No Connection

KM616V4000BZ, KM616U4000BZ Family

PACKAGE DIMENSIONS (Units : mm)



	Min	Typ	Max
A	-	0.75	-
B	7.10	7.20	7.30
B1	-	3.75	-
C	11.55	11.65	11.75
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08



Notes.

1. Bump counts : 48(8row x 6row)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is copianarity : 0.08(max)

Super Low Power and Low Voltage SRAM (Full CMOS)

256Kx8 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology : 0.4μm Full CMOS
- Organization : 128Kx8
- Power Supply Voltage
  KM68FV1000 Family : 3.0V(Min) ~ 3.6V(Max)
  KM68FS1000 Family : 2.3V(Min) ~ 3.3V(Max)
  KM68FR1000 Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-SOP, 32-TSOP(I)-F/R, 32-sTSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

The KM68FV1000, KM68FS1000 and KM68FR1000 family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

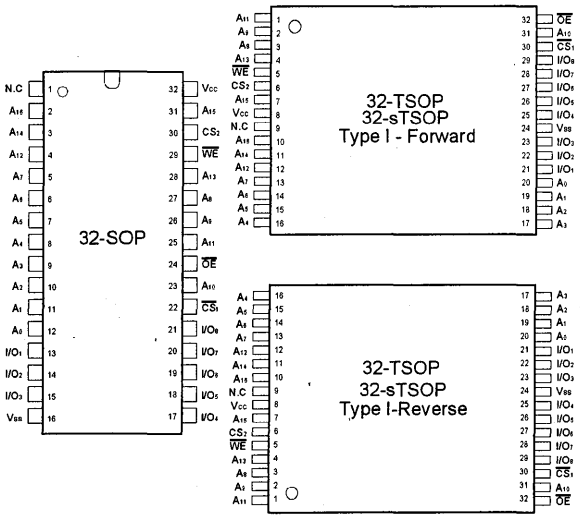
2

PRODUCT FAMILY

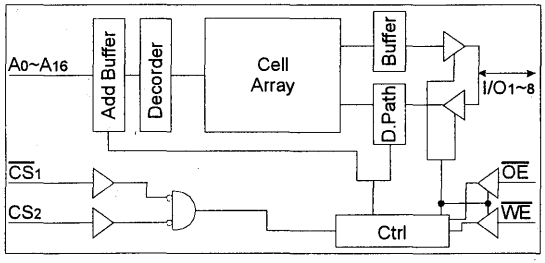
Product Family	Operating Temp.Range	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (I_{SB1})	Operating (I_{CC2})	
KM68FV1000	Commercial (0~70℃)	3.0~3.6V	70*/85@Vcc=3.3±0.3V	1μA***/5μA** (Max)	55mA(Max)	32-TSOP(I) Forward/ Reverse 32-sTSOP(I) Forward/ Reverse 32-SOP
KM68FS1000		2.3~3.3V	70*/85@Vcc=3.0±0.3V 120*/150@VCC=2.5±0.2V		50mA(Max) 30mA(Max)	
KM68FR1000		1.8~2.7V	300*@Vcc=2.0±0.2V		15mA(Max)	
KM68FV1000I	Industrial (-40~85℃)	3.0~3.6V	70*/85@Vcc=3.3±0.3V	1μA***/5μA** (Max)	55mA(Max)	
KM68FS1000I		2.3~3.3V	70*/85@Vcc=3.0±0.3V 120*/150@VCC=2.5±0.2V		50mA(Max) 30mA(Max)	
KM68FR1000I		1.8~2.7V	300*@Vcc=2.0±0.2V		15mA(Max)	

* measured with 30pF test load, ** for low power version, *** for super low power version with special handling.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A0~A16	Address Inputs	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
$\overline{CS}_1$,CS2	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
$\overline{OE}$	Output Enable	N.C.	No Connection

SAMSUNG ELECTRONICS

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST FOR LOW LOW POWER CONSUMPTION

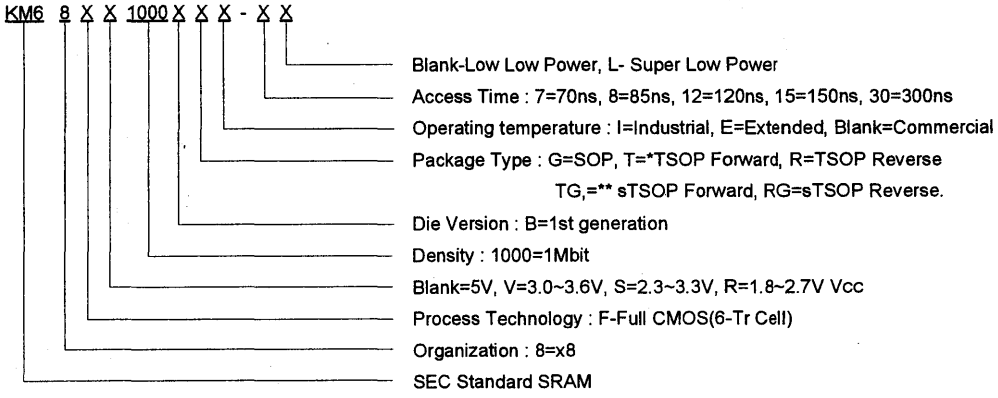
Commercial Temp Product (0~70℃)		Industrial Temp Product (-40~85℃)	
Part Name	Function	Part Name	Function
KM68FV1000G-7	32-SOP, 70ns, 3.3V, LL	KM68FV1000GI-7	32-SOP, 70ns, 3.3V, LL
KM68FV1000G-8	32-SOP, 85ns, 3.3V, LL	KM68FV1000GI-8	32-SOP, 85ns, 3.3V, LL
KM68FV1000T-7	32-TSOP F, 70ns, 3.3V, LL	KM68FV1000TII-7	32-TSOP F, 70ns, 3.3V, LL
KM68FV1000T-8	32-TSOP F, 85ns, 3.3V, LL	KM68FV1000T-8	32-TSOP F, 85ns, 3.3V, LL
KM68FV1000R-7	32-TSOP R, 70ns, 3.3V, LL	KM68FV1000RI-7	32-TSOP R, 70ns, 3.3V, LL
KM68FV1000R-8	32-TSOP R, 85ns, 3.3V, LL	KM68FV1000RI-8	32-TSOP R, 85ns, 3.3V, LL
KM68FS1000G-12	32-SOP, 120/70ns, *2.5/3.0V, LL	KM68FS1000GI-12	32-SOP, 120/70ns, 2.5/3.0V, LL
KM68FS1000G-15	32-SOP, 150/85ns, 2.5/3.0V, LL	KM68FS1000GI-15	32-SOP, 150/85ns, 2.5/3.0V, LL
KM68FS1000T-12	32-TSOP F, 120/70ns, *2.5/3.0V, LL	KM68FS1000TI-12	32-TSOP F, 120/70ns, 2.5/3.0V, LL
KM68FS1000T-15	32-TSOP F, 150/85ns, 2.5/3.0V, LL	KM68FS1000TI-15	32-TSOP F, 150/85ns, 2.5/3.0V, LL
KM68FS1000R-12	32-TSOP R, 120/70ns, 2.5/3.0V, LL	KM68FS1000RI-12	32-TSOP R, 120/70ns, 2.5/3.0V, LL
KM68FS1000R-15	32-TSOP R, 150/85ns, 2.5/3.0V, LL	KM68FS1000RI-15	32-TSOP R, 150/85ns, 2.5/3.0V, LL
KM68FS1000TG-12	32-sTSOP F, 120/70ns, 2.5/3.0V, LL	KM68FS1000TGI-12	32-sTSOP F, 120/70ns, 2.5/3.0V, LL
KM68FS1000TG-15	32-sTSOP F, 150/85ns, 2.5/3.0V, LL	KM68FS1000TGI-15	32-sTSOP F, 150/85ns, 2.5/3.0V, LL
KM68FS1000RG-12	32-sTSOP R, 120/70ns, 2.5/3.0V, LL	KM68FS1000RGI-12	32-sTSOP R, 120/70ns, 2.5/3.0V, LL
KM68FS1000RG-15	32-sTSOP R, 150/85ns, 2.5/3.0V, LL	KM68FS1000RGI-15	32-sTSOP R, 150/85ns, 2.5/3.0V, LL
KM68FR1000G-30	32-SOP, 300ns, **2.0/2.5V, LL	KM68FR1000GI-30	32-SOP, 300ns, 2.0/2.5V, LL
KM68FR1000T-30	32-TSOP F, 300ns, 2.0/2.5V, LL	KM68FR1000TI-30	32-TSOP F, 300ns, 2.0/2.5V, LL
KM68FR1000R-30	32-TSOP R, 300ns, 2.0/2.5V, LL	KM68FR1000RI-30	32-TSOP R, 300ns, 2.0/2.5V, LL
KM68FR1000TG-30	32-sTSOP F, 300ns, **2.0/2.5V, LL	KM68FR1000TGI-30	32-sTSOP F, 300ns, 2.0/2.5V, LL
KM68FR1000RG-30	32-sTSOP R, 300ns, 2.0/2.5V, LL	KM68FR1000RGI-30	32-sTSOP R, 300ns, 2.0/2.5V, LL

* The meaning of 2.5V/3.0V, 120/70ns is that the operating Vcc is ranged from 2.3V(Min) to 3.3V(Max) with speed 120ns @2.5V±0.2 and 70ns @3.0V±0.2. This type of meaning is applied to other notations like the example.
** But in case of KM68FR1000G-30, there is only one speed bin, 300ns though it supports wide range operating VCC.

PRODUCT LIST FOR SUPER LOW POWER CONSUMPTION

The product names for super low power version has letter[L] at the end of product name of low low power version. The part name for 128Kx16 Super Low Power product operating at 2.3~3.3V with 70ns @ 3.0V and 120ns @ 2.5V will be KM68FS1000TI-12L.
And if suppliment is required for those products please contact Samsung Electronics Branch near your office. Samsung will support with special treatment.

ORDERING INFORMATION



NOTES : * The size of X x Y for TSOP package is 08 x 20mm.
** The size of X x Y for sTSOP package is 08 x 13.40mm.

2

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to 3.6V[1]	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V[2]	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-55 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM68FV1000 KM68FS1000 KM68FR1000
		-40 to 85	℃	KM68FV1000I KM68FS1000I KM68FR1000I
Soldering temperature and time	T_{SOLDER}	260℃, 5sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1) VIN/VOUT=0.2 to 3.9V for KM68FV1000 Family.

2) Maximum VCC=-0.2 to 4.6V for KM68F12000 Family.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product		Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68FV1000 Family KM68FS1000 Family KM68FR1000 Family		3.0 2.3 1.8	3.3 2.5/3.0 2.0/2.5	3.6 3.3 2.7	V V V
Ground	Vss	All Family		0	0	0	V
Input high voltage	V_{IH}	KM68FV1000 Family	Vcc=3.3±0.3V	2.2	-	Vcc+0.2	V
		KM68FS1000 Family	Vcc=3.0±0.3V	2.2	-	Vcc+0.2	V
			Vcc=2.5±0.2V	2.0	-	Vcc+0.2	V
		KM68FR1000 Family	Vcc=2.5±0.2V	2.0	-	Vcc+0.2	V
			Vcc=2.5±0.2V	1.6	-	Vcc+0.2	V
Input low voltage	V_{IL}	All Family		-0.2***	-	0.4	V

* 1) Commercial Product : TA=0 to 70℃, unless otherwise specified
2) Industrial Product : TA=-40 to 85℃, unless otherwise specified

** TA=25℃

*** VIL(min)=-1.5V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	Vin=0V	-	8	pF
Input/Output capacitance	C_{IO}	Vio=0V	-	10	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Sym-bol	Test Conditions[1]			Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc			-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc			-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH} V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA		Read	-	3	5[5]	mA
					Write	-	10	15[5]	
Average operatingcurrent		I_{CC1}	Cycle time=1μs 100%duty $\overline{CS_1}$≤0.2V, CS_2≥V_{IN}≥Vcc-2.0V		Read	-	3	5[5]	mA
					Write	-	10	15[5]	
		I_{CC2}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IH} I_{IO}=0mA Min cycle, 100% duty		Vcc=3.3V@70ns	-	-	50[4]	mA
					Vcc=2.7V@120ns	-	-	30	
					Vcc=2.2V@300ns	-	-	15	
Output low voltage		V_{OL}	I_{OL}	Vcc=3.0/3.3V	2.1mA	-	-	0.4	V
				Vcc=2.5V	0.5mA	-	-	0.4	
				Vcc=2.0V	0.33mA	-	-	0.4	
Output high voltage		V_{OH}	I_{OH}	Vcc=3.0/3.3V	-1.0mA	2.4	-	-	V
				Vcc=2.5V	-0.5mA	2.0	-	-	
				Vcc=2.0V	-0.44mA	1.6	-	-	
Standby Current(TTL)		I_{SB}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL}			-	-	0.3	mA
Standby Current (CMOS)	KM68FV1000 KM68FS1000 KM68FR1000	I_{SB1}	$\overline{CS_1}$≥Vcc-2.0V CS_2≥Vcc-2.0V or CS_2≤0.2V Otherinput =0~Vcc		Super Low Power	-	0.05[3]	2[2]	μA
					Low Low Power	-	-	10[2]	
	KM68FV1000I KM68FS1000I KM68FR1000I				Super Low Power	-	0.05[3]	2[2]	μA
					Low Low Power	-	-	10[2]	

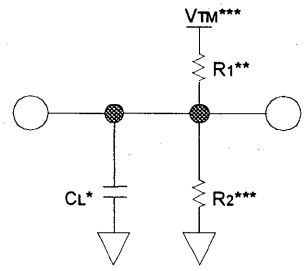
1) -Commercial Product
TA=0 to 70℃, Vcc=3.3±0.3V for 68FV1000 Family, Vcc=2.3(Min)~3.3V(Max)V for 68FS1000 Family,
Vcc=1.8(Min)~2.7V(Max)V for 68FR1000 Family.
-Industrial Product : TA=-40 to 85℃, Vcc=3.3±0.3V for 68FV1000I Family, Vcc=2.3(Min)~3.3V(Max)V for 68FS1000I Family,
Vcc=1.8(Min)~2.7V(Max)V for 68FR1000I Family.
2) The value has difference by ±1μA
Measured at Vcc=3.3(Max).
3) The value is not 100% tested but obtained statistically at Temp=25℃
4) - The value is measured at Vcc=3.0±0.3V
- ICC2=55mA with 70ns at Vcc=3.3±0.3V, but this value is not 100% tested but obtained statistically.
- ICC2=30mA with 120ns cycle at Vcc=2.5±0.2V, but this value is not 100% tested but obtained statistically.
- ICC2=15mA with 300ns cycle at Vcc=2.0±0.2V, but this value is not 100% tested but obtained statistically.
5) The value is measured ar Vcc=3.0±0.3V, The value measured at Vcc=2.5±2.0V is under the calue of Vcc=3.0±0.3V.

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	Vcc=3.3V, 3.0V, 2.5V
	0.4 to 1.8V	Vcc=2.0V
Input rise fall time	5ns	-
input and output reference voltage	1.5V	Vcc=3.3V, 3.0V
	1.1V	Vcc=2.5V
	0.9V	Vcc=2.0V,
Output load (See right)	CL=100pF	See Test Condition #2
	CL=30pF	

* See test condition of DC and Operating characteristics



* Including scope and jig capacitance
**R1=3070Ω, R2=3150Ω
***VTM=2.8V for VCC=3.0/3.3V
=2.3V for VCC=2.5V
=1.8V for VCC=2.0V

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Vcc Range	Typical Supply Vcc	Speed	Comments
KM68FR1000	0~70℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	Commercial
KM68FS1000	0~70℃	2.3(Min)~3.3(Max)	2.5V ± 0.2 Operation	120*/150ns	
			3.0V ± 0.3 Operation	85ns	
KM68FV1000	0~70℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	
KM68FR1000I	-40~85℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	Industrial
KM68FS100I0	-40~85℃	2.3(Min)~3.3(Max)	2.5V ± 0.2 Operation	120*/150ns	
			3.0V ± 0.3 Operation	85ns	
KM68FV1000I	-40~85℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	

* All the parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins												Units
			70ns		85ns		100ns		120ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Chip select to output	tCO1 tCO2	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Output enable to valid output	tOE	-	35	-	45	-	50	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ1 tLZ2	10	-	10	-	10	-	10	-	20	-	50	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	5	-	10	-	30	-	ns
	Chip disable to high-Z output	tHZ1 tHZ2	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output hold from address	tOH	10	-	15	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Chip select to end of write	tCW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	80	-	100	-	200	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	50	-	60	-	120	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	5	-	5	-	20	-	ns

* not yet available, only for reserved speed bins.

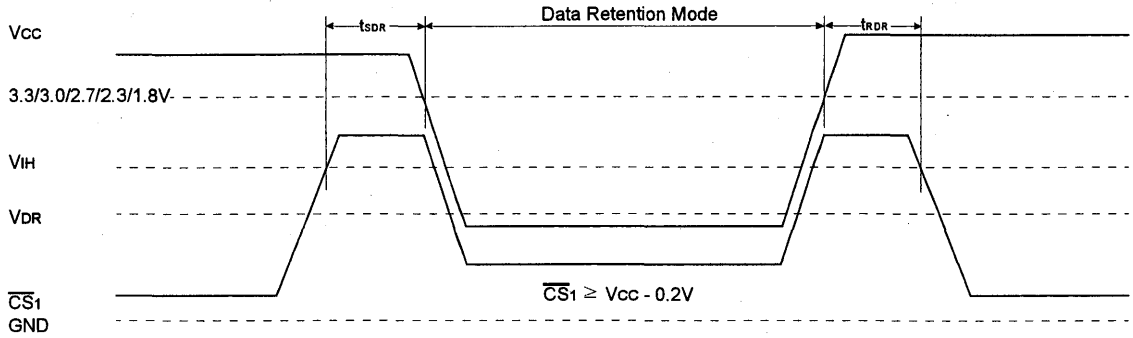
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS_1}$**** ≥ Vcc-2.0V		1.5	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V $\overline{CS_1}$ ≥ Vcc-0.2V	Super Low Power	***	0.1	1.0	μA
			Low Low Power	-	-	5.0	
Data retention set-up time	tSDR	See data retention waveform		0	-	-	ns
Recovery time	tRDR			tRC	-	-	

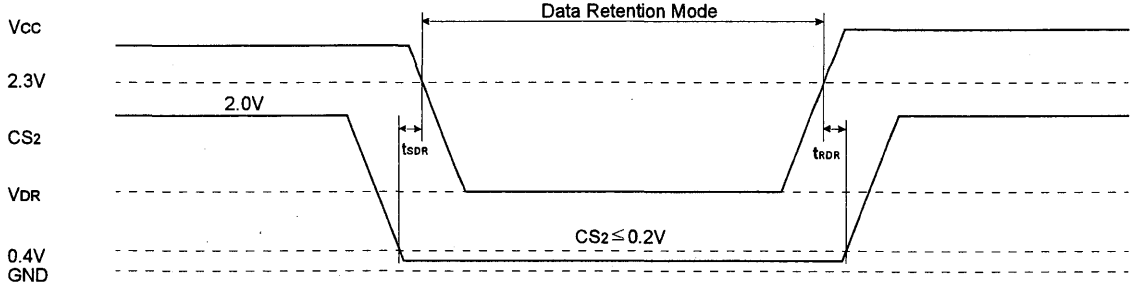
* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** TA=25℃, the value is too small to detect by test machine, 0.01μA statistically
*** The min value is almost 0nA statistically
**** $\overline{CS_1}$ ≥ Vcc-2.0V, CS_2 ≥ Vcc-2.0V($\overline{CS_1}$ controlled) or CS_2 ≤ 0.2V(CS_2 controlled)

DATA RETENTION WAVE FORM

1) $\overline{CS_1}$ controlled



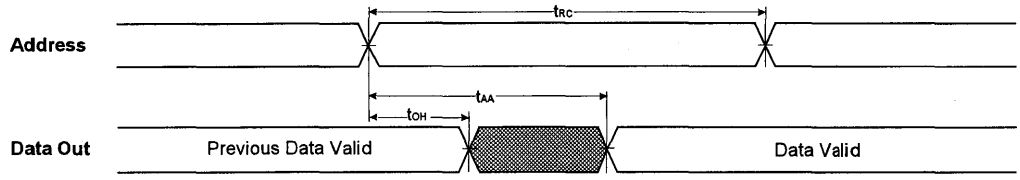
2) CS_2 controlled



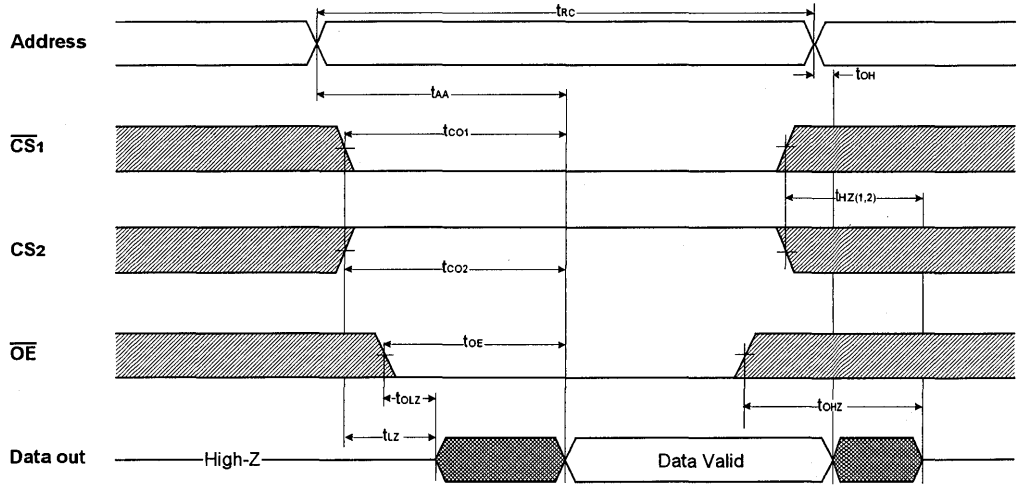
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



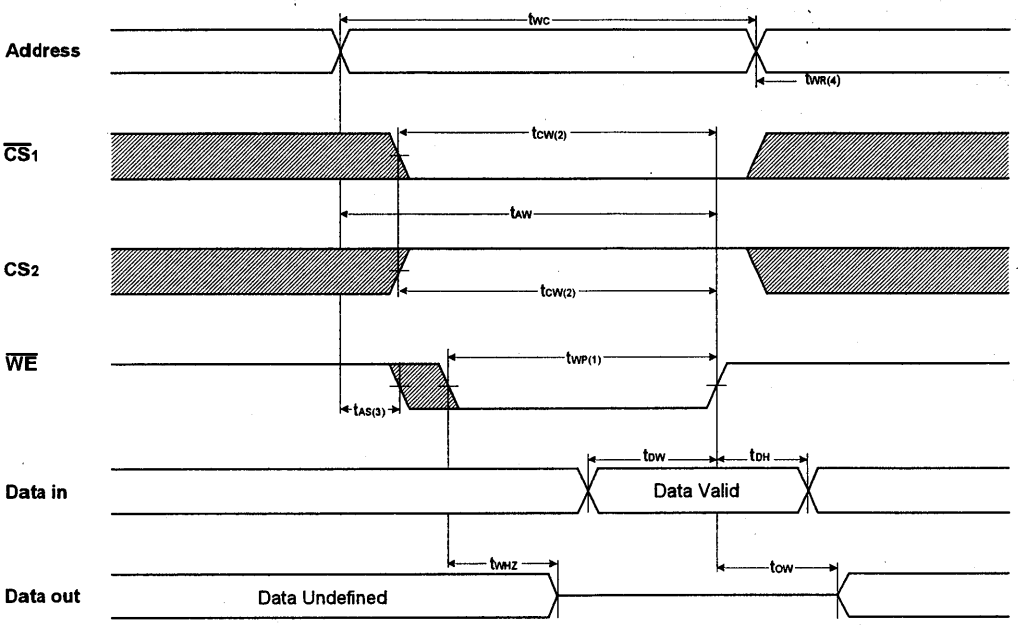
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=V_{IH})



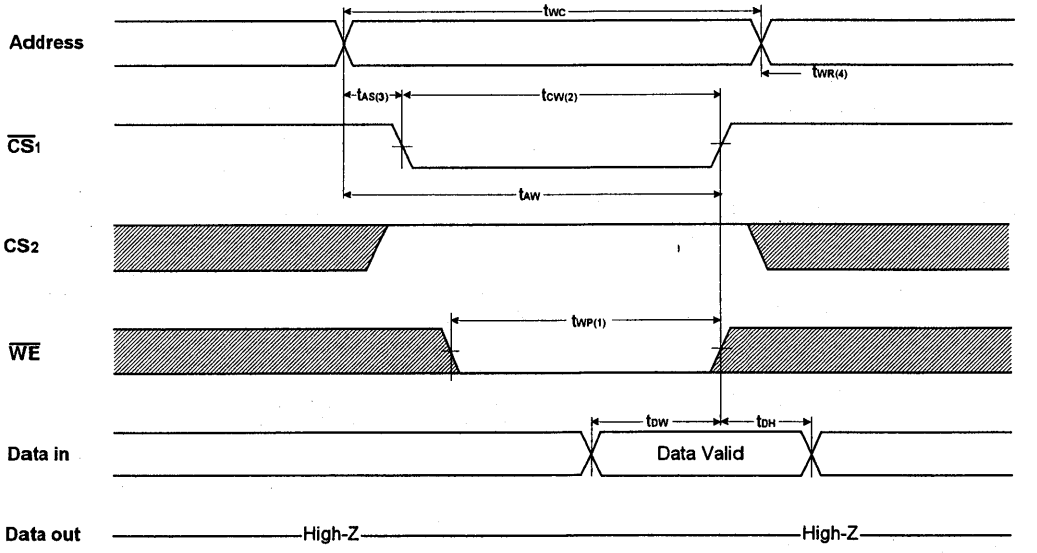
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)

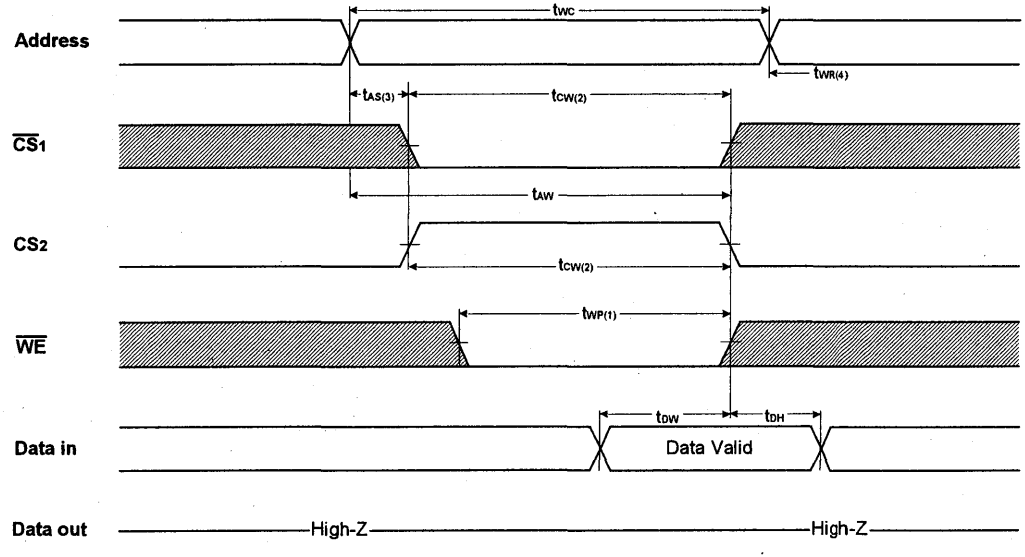


TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}_1$ Controlled)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE (CS_2 Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high, tWP is measured from the begining of write to the end of write.
2. tCW is measured from the $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR(1) applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high tWR(2) applied in case a write ends as CS_2 going to low.

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Current Mode
H	X*	X	X	Power Down	High-Z	Isb, Isb1
X	L	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	H	Output Disable	High-Z	Icc
L	H	H	L	Read	Dout	Icc
L	H	L	X	Write	Din	Icc

* X means don't care (Must be in high or low states)

128Kx8 bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Size Package)

FEATURES

- Process Technology : 0.4μm Full CMOS
- Organization : 128Kx8
- Power Supply Voltage
  KM68FS1000Z Family : 2.3V(Min) ~ 3.3V(Max)
  KM68FR1000Z Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output and TTL Compatible
- Package Type : 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM68FS1000Z and KM68FR1000Z family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very samll from factor with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temp.Range	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Operating (Icc2)	Standby (Isb1)	
KM68FS1000Z	Commercial (0~70℃)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	55mA(Max) 30mA(Max)	10μA (max)	48-CSP (6x8 ball area with 0.75mm ball pitch)
KM68FR1000Z		1.8~2.7V	300*@Vcc=2.0±0.2V	15mA(Max)		
KM68FS1000ZI	Industria (-40~85℃)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	55mA(Max) 30mA(Max)	10μA (max)	
KM68FR1000ZI		1.8~2.7V	300*@Vcc=2.0±0.2V	15mA(Max)		

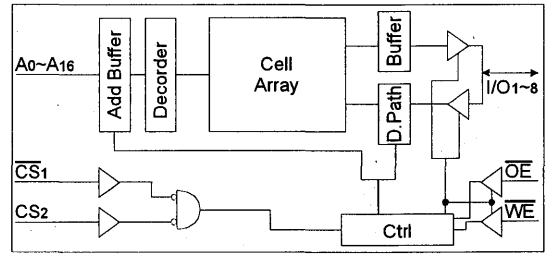
* The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
A	A_0	A_1	CS_2	A_3	A_6	A_8
B	I/O_5	A_2	$\overline{WE}$	A_4	A_7	I/O_1
C	I/O_6		NC	A_5		I/O_2
D	V_{SS}					V_{CC}
E	V_{CC}					V_{SS}
F	I/O_7		NC	NC		I/O_3
G	I/O_8	$\overline{OE}$	$\overline{CS_1}$	A_{16}	A_{15}	I/O_4
H	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}

* See last page for package dimension.

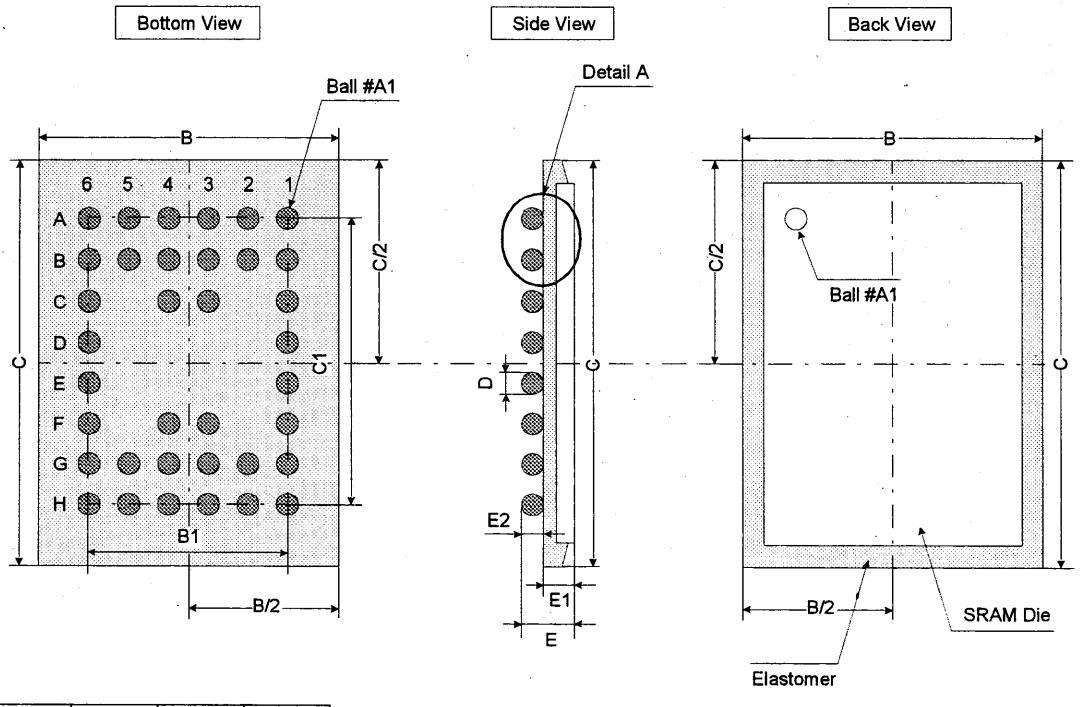
FUNCTIONAL BLOCK DIAGRAM



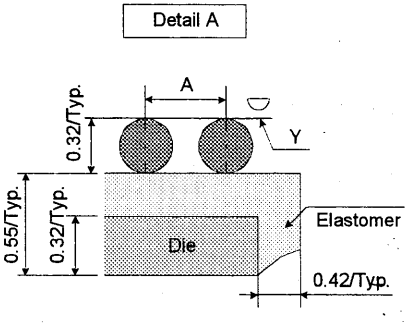
Name	Function	Name	Function
A_0~A_{16}	Address Inputs	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
$\overline{CS_1}$,CS_2	Chip Select Input	I/O_1~I/O_8	Data Inputs/Outputs
$\overline{OE}$	Output Enable	N.C.	No Connection

KM68FS1000Z, KM68FR1000Z Family

PACKAGE DIMENSIONS (Units : mm)



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08



Notes.

1. Bump counts : 48(8row x 6row)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is copianarity : 0.08(max)

64Kx16 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology : 0.4㎛ Full CMOS
- Organization : 64Kx16
- Power Supply Voltage
  KM616FV1000 Family : 3.0V(Min) ~ 3.6V(Max)
  KM616FS1000 Family : 2.3V(Min) ~ 3.3V(Max)
  KM616FR1000 Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type : JEDEC Standard
  44-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

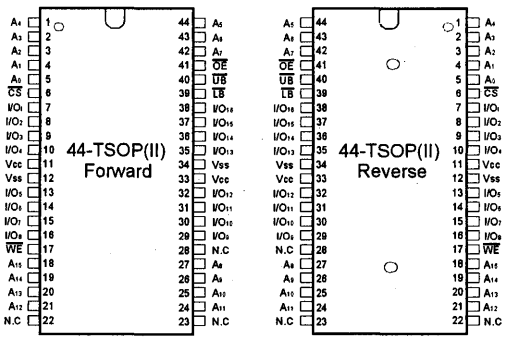
The KM616FV1000, KM616FS1000 and KM616FR1000 family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

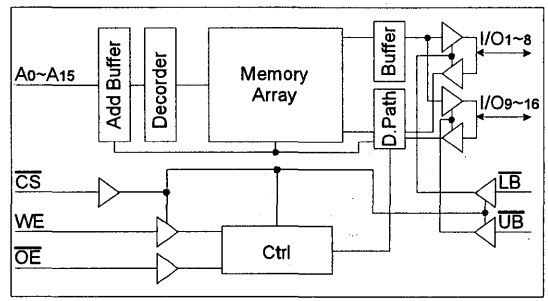
Product Family	Operating Temp.Range	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (I_{SB1})	Operating (I_{CC2})	
KM616FV1000	Commercial (0~70℃)	3.0~3.6V	70*/85@Vcc=3.3±0.3V	1㎂***/5㎂** (Max)	80mA(Max)	44-TSOP(II) Forward/ Reverse
KM616FS1000		2.3~3.3V	70*/85@Vcc=3.3±0.3V 120*/150@VCC=2.5±0.2V		80mA(Max) 50mA(Max)	
KM616FR1000		1.8~2.7V	300*@Vcc=2.0±0.2V		20mA(Max)	
KM616FV1000I	Industria (-40~85℃)	3.0~3.6V	70*/85@Vcc=3.3±0.3V	1㎂***/5㎂** (Max)	80mA(Max)	
KM616FS1000I		2.3~3.3V	70*/85@Vcc=3.3±0.3V 120*/150@VCC=2.5±0.2V		80mA(Max) 50mA(Max)	
KM616FR1000I		1.8~2.7V	300*@Vcc=2.0±0.2V		20mA(Max)	

* measured with 30pF test load, ** for low power version, *** for super low power version with special handling.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A0~A15	Address Inputs	$\overline{LB}$	Lower Byte(I/O1~8)
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O9~16)
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable	Vss	Ground
I/O1~I/O16	Data Inputs/Out-	N.C.	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST FOR LOW LOW POWER CONSUMPTION

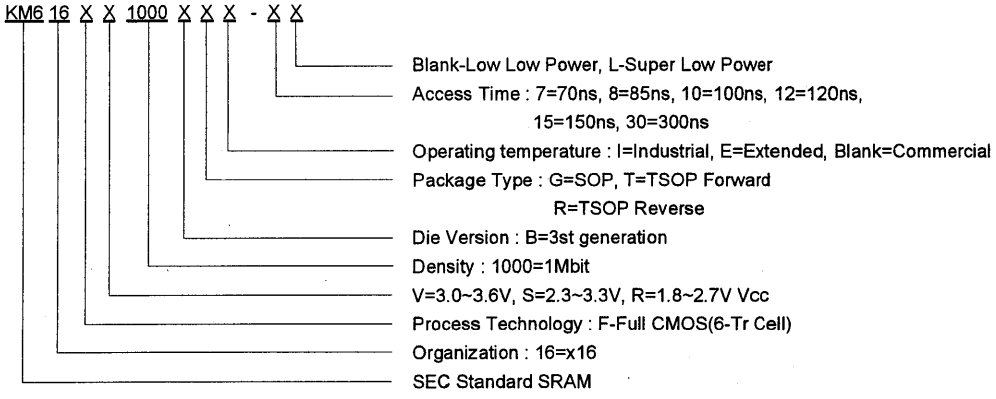
Commercial Temp Product (0~70℃)		Industrial Temp Product (-40~85℃)	
Part Name	**Function**	**Part Name**	**Function**
KM616FV1000T-7	44-TSOP F, 70ns, 3.3V, LL	KM616FV1000TI-7	44-TSOP F, 70ns, 3.3V, LL
KM616FV1000T-8	44-TSOP F, 85ns, 3.3V, LL	KM616FV1000TI-8	44-TSOP F, 85ns, 3.3V, LL
KM616FV1000R-7	44-TSOP R, 70ns, 3.3V, LL	KM616FV1000RI-7	44-TSOP R, 70ns, 3.3V, LL
KM616FV1000R-8	44-TSOP R, 85ns, 3.3V, LL	KM616FV1000RI-8	44-TSOP R, 85ns, 3.3V, LL
KM616FS1000T-12	44-TSOP F, 120/70ns, *2.5/3.0V, LL	KM616FS1000TI-12	44-TSOP F, 120/70ns, 2.5/3.0V, LL
KM616FS1000T-15	44-TSOP F, 150/85ns, 2.5/3.0V, LL	KM616FS1000TI-15	44-TSOP F, 150/85ns, 2.5/3.0V, LL
KM616FS1000R-12	44-TSOP R, 120/70ns, 2.5/3.0V, LL	KM616FS1000RI-12	44-TSOP R, 120/70ns, 2.5/3.0V, LL
KM616FS1000R-15	44-TSOP R, 150/85ns, 2.5/3.0V, LL	KM616FS1000RI-15	44-TSOP R, 150/85ns, 2.5/3.0V, LL
KM616FR1000T-30	44-TSOP F, 300ns, **2.0/2.5V, LL	KM616FR1000TI-30	44-TSOP F, 300ns, 2.0/2.5V, LL
KM616FR1000R-30	44-TSOP F, 300ns, 2.0/2.5V, LL	KM616FR1000RI-30	44-TSOP F, 300ns, 2.0/2.5V, LL

* The meaning of 2.5V/3.0V, 120/70ns is that the operating Vcc is ranged from 2.3V(Min) to 3.3V(Max) with speed 120ns @2.5V±0.2 and 70ns @3.0V±0.3. This type of meaning is applied to other notations like the example.
** But in case of KM616FR1000T-30, there is only one speed bin, 300ns though it supports wide range operating VCC.

PRODUCT LIST FOR SUPER LOW POWER CONSUMPTION

The product names for super low power version has letter[L] at the end of product name of low low power version. The part name for 64Kx16 Super Low Power product operating at 2.3~3.3V with 70ns @ 3.0V and 120ns @ 2.5V will be KM616FA1000TI-12L.
And if suppliment is required for those products please contact Samsung Electronics Branch near your office. Samsung will support with special treatment.

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.2 to 3.6V[1]	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V[2]	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-55 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM616FV1000 KM616FS1000 KM616FR1000
		-40 to 85	℃	KM616FV1000I KM616FS1000I KM616FR1000I
Soldering temperature and time	T_{SOLDER}	260℃, 5sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1) V_{IN}/V_{OUT}=0.2 to 3.9V for KM616FV1000 Family.

2) V_{CC}=-0.2 to 4.6V for KM616FV1000 Family.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product		Min	Typ**	Max	Unit
Supply voltage	Vcc	KM616FV1000 Family KM616FS1000 Family KM616FR1000 Family		3.0 2.3 1.8	3.3 2.5/3.0 2.0/2.5	3.6 3.3 2.7	V V V
Ground	Vss	All Family		0	0	0	V
Input high voltage	V_{IH}	KM616FV1000 Family	Vcc=3.3±0.3V	2.2	-	Vcc+0.2	V
		KM616FS1000 Family	Vcc=3.0±0.3V	2.2	-	Vcc+0.2	V
			Vcc=2.5±0.2V	2.0	-	Vcc+0.2	V
		KM616FR1000 Family	Vcc=2.5±0.2V	2.0	-	Vcc+0.2	V
			Vcc=2.5±0.2V	1.6	-	Vcc+0.2	V
Input low voltage	V_{IL}	All Family		-0.2***	-	0.4	V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified

** T_A=25℃

*** V_{IL}(min)=-1.5V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	Vin=0V	-	8	pF
Input/Output capacitance	C_{IO}	Vio=0V	-	10	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Sym-	Test Conditions[1]			Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc			-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc			-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS1}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA		Read	-	-	10[5]	mA
					Write	-	-	20[5]	
Average operatingcurrent		I_{CC1}	Cycle time=1μs 100%duty, $\overline{CS1}$≤0.2V		Read	-	-	10[5]	mA
					Write	-	-	20[5]	
		I_{CC2}	$\overline{CS}$=V_{IH}, I_{IO}=0mA Min cycle, 100% duty	Vcc=3.3V@70ns		-	-	80[4]	mA
				Vcc=2.7V@120ns		-	-	50	
				Vcc=2.2V@300ns		-	-	25	
Output low voltage		V_{OL}	I_{OL}	Vcc=3.0/3.3V	2.1mA	-	-	0.4	V
				Vcc=2.5V	0.5mA	-	-	0.4	
				Vcc=2.0V	0.33mA	-	-	0.4	
Output high voltage		V_{OH}	I_{OH}	Vcc=3.0/3.3V	-1.0mA	2.4	-	-	V
				Vcc=2.5V	-0.5mA	2.0	-	-	
				Vcc=2.0V	-0.44mA	1.6	-	-	
Standby Current(TTL)		I_{SB}	$\overline{CS1}$=V_{IH}			-	-	0.3	mA
Standby Current (CMOS)	KM616FV1000 KM616FS1000 KM616FR1000	I_{SB1}	$\overline{CS}$≥Vcc-2.0V Otherinput =0~Vcc		Super Low Power	-	0.05[3]	1[2]	μA
					Low Low Power	-	-	5[2]	
	KM616FV1000 KM616FS1000 KM616FR1000				Super Low Power	-	0.05[3]	1[2]	μA
					Low Low Power	-	-	5[2]	

1) -Commercial Product
T_A=0 to 70℃, Vcc=3.3±0.3V for 616FV1000 Family, Vcc=2.3(Min)~3.3V(Max)V for 616FS1000 Family,
Vcc=1.8(Min)~2.7V(Max)V for 616FR1000 Family.
-Industrial Product : T_A=-40 to 85℃, Vcc=3.3±0.3V for 616FV1000I Family, Vcc=2.3(Min)~3.3V(Max)V for 616FS1000I Family,
Vcc=1.8(Min)~2.7V(Max)V for 616FR1000I Family.

2) The value has difference by ±1μA
Measured at Vcc=3.3(Max).

3) The value is not 100% tested but obtained statistically at Temp=25℃

4) - The value is measured at Vcc=3.0±0.3V
- I_{CC2}=80mA with 70ns at Vcc=3.3±0.3V, but this value is not 100% tested but obtained statistically.
- I_{CC2}=50mA with 120ns cycle at Vcc=2.5±0.2V, but this value is not 100% tested but obtained statistically.
- I_{CC2}=25mA with 300ns cycle at Vcc=2.0±0.2V, but this value is not 100% tested but obtained statistically.

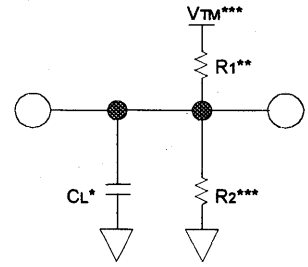
5) The value is measured ar Vcc=3.0±0.3V, The value measured at Vcc=2.5±2.0V is under the calue of Vcc=3.0±0.3V.

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	Vcc=3.3V, 3.0V, 2.5V
	0.4 to 1.8V	Vcc=2.0V
Input rise fall time	5ns	-
input and output reference voltage	1.5V	Vcc=3.3V, 3.0V
	1.1V	Vcc=2.5V
	0.9V	Vcc=2.0V,
Output load (See right)	CL=100pF+1TTL	See Test Condition #2
	CL=30pF+1TTL	

* See DC Operating conditions



* Including scope and jig capacitance
**R1=3070Ω, R2=3150Ω
***VTM=2.8V for Vcc=3.0/3.3V
=2.3V for Vcc=2.5V
=1.8V for Vcc=2.0V

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Vcc Range	TypicalSupply Vcc	Speed	Comments
KM616FR1000	0~70℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	Commercial
KM616FS1000	0~70℃	2.3(Min)~3.3(Max)	2.5V ± 0.2 Operation	120*/150ns	
			3.0V ± 0.3 Operation	70*/85ns	
KM616FV1000	0~70℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	
KM616FR1000I	-40~85℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	Industrial
KM616FS100I0	-40~85℃	2.3(Min)~3.3(Max)	2.5V ± 0.2 Operation	120*/150ns	
			3.0V ± 0.3 Operation	70*/85ns	
KM616FV1000I	-40~85℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	

* All the parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins												Units
			70ns		85ns		100ns		120ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Chip select to output	tCO1 tCO2	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Output enable to valid output	tOE	-	35	-	45	-	50	-	60	-	75	-	150	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	35	-	45	-	50	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ1 tLZ2	10	-	10	-	10	-	20	-	20	-	50	-	ns
	Output enable to low-Z output	tOLZ tBLZ	5	-	5	-	5	-	20	-	20	-	30	-	ns
	Chip disable to high-Z output	tHZ1 tHZ2	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output disable to high-Z output	tOHZ tBHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output hold from address	tOH	10	-	15	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Chip select to end of write	tCW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	80	-	100	-	200	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	50	-	60	-	120	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	5	-	5	-	20	-	ns

* not yet available, only for reserved speed bins.

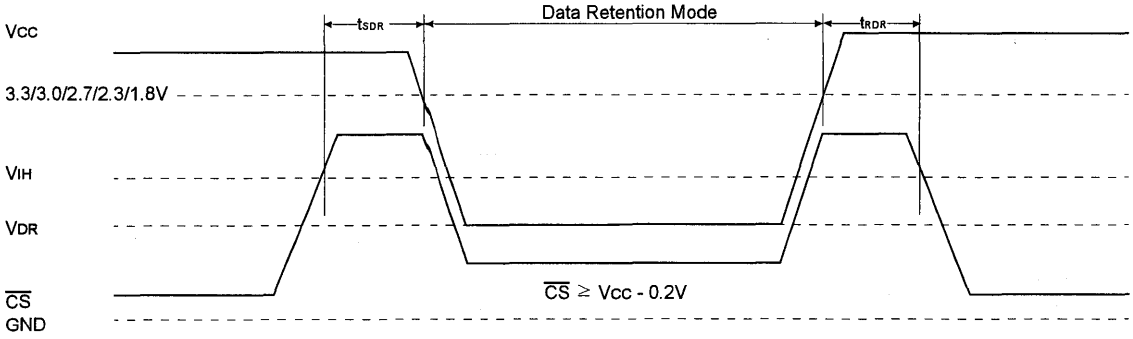
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	VDR	$\overline{CS} \geq$ Vcc-2.0V		1.5	-	3.6	V
Data retention current	IDR	Vcc=3.0V $\overline{CS} \geq$ Vcc-0.2V	Super Low Power	***	**	1.0	μA
			Low Low Power	-	-	5.0	
Data retention set-up time	tSDR	See data retention waveform		0	-	-	ns
Recovery time	tRDR			tRC	-	-	

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** TA=25℃, the value is too small to detect by test machine, 0.01μA statistically
*** The min value is almost 0nA statistically

DATA RETENTION WAVE FORM

($\overline{CS}$ controlled)

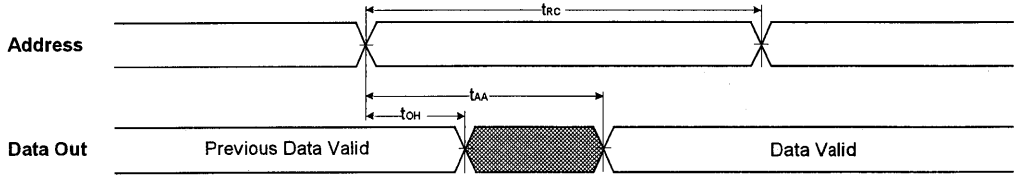


SAMSUNG ELECTRONICS

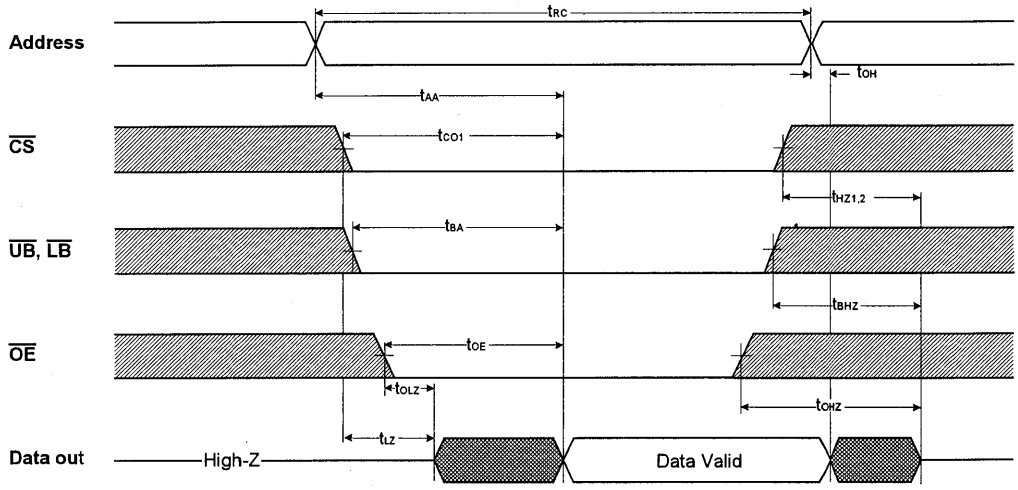
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH, $\overline{UB}$ or, and $\overline{LB}$=VIL)



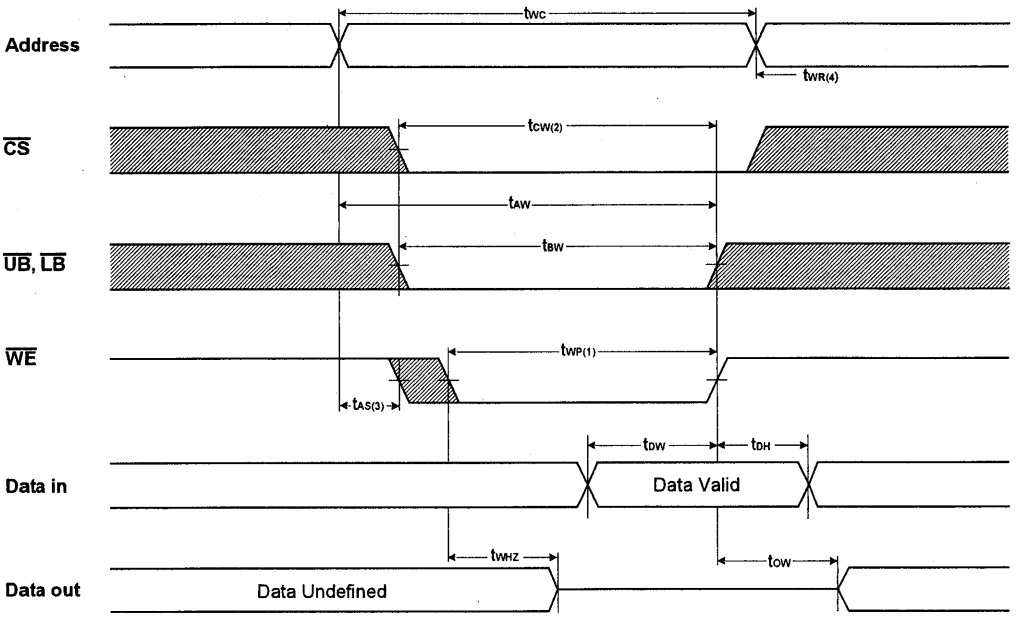
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=VIH)



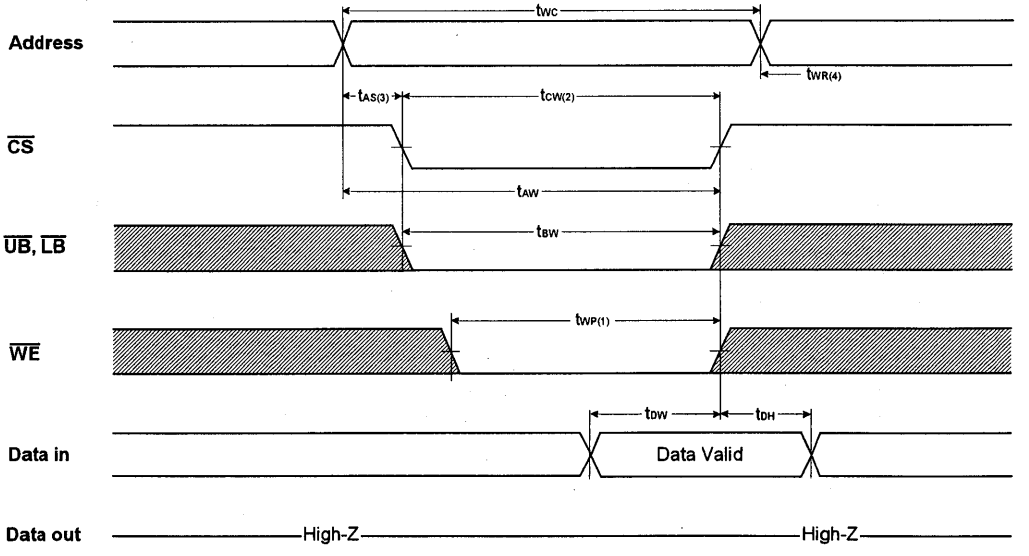
NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device interconnection.

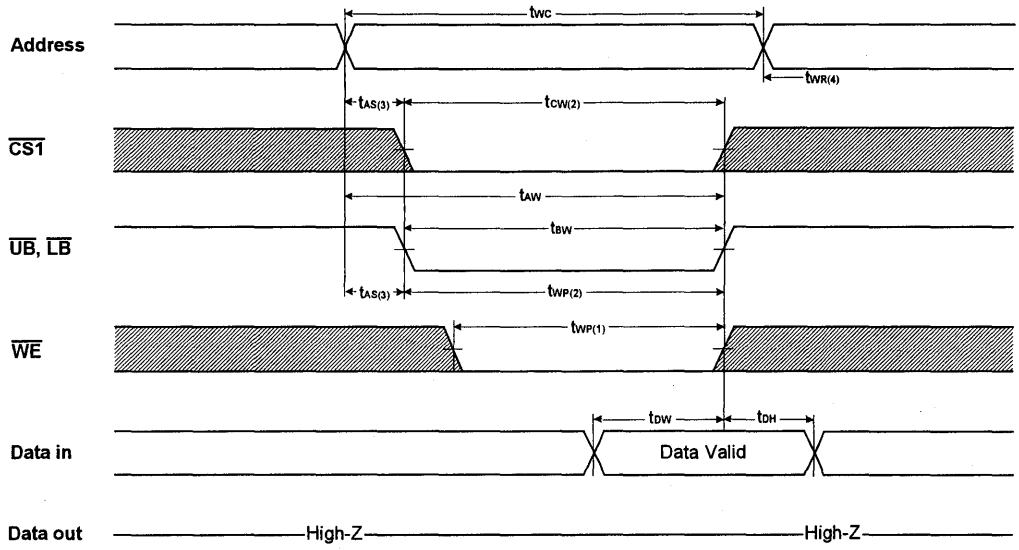
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultenious asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the $\overline{CS}$ going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end or write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{LB}$	$\overline{UB}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O1~8	I/O9~16	Current Mode
H	X	X	X	X	Not Select	High-Z	High-Z	Isb1
L	X	X	H	H	Output Disable	High-Z	High-Z	Icc
L	H	H	X	X		High-Z	High-Z	Icc
L	L	H	H	L	Read	Dout	High-Z	Icc
L	H	L	H	L	Read	High-Z	Dout	
L	L	L	H	L	Read	Dout	Dout	
L	L	H	L	X	Write	Din	High-Z	Icc
L	H	L	L	X	Write	High-Z	Din	
L	L	L	L	X	Write	Din	Din	

* X means don't care (Must be in high or low states)

64Kx16 bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Size Package)

FEATURES

- Process Technology : 0.4μm Full CMOS
- Organization :64Kx16
- Power Supply Voltage
  KM616FS2000Z Family : 2.3V(Min) ~ 3.3V(Max)
  KM616FR2000Z Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type : 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM616FS1000Z and KM616FR1000Z family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very samll from factor with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temp.Range	Vcc Range (min~max)	Speed(ns)	Power Dissipation		PKG Type
				Operating (I_{CC2})	Standby (I_{SB1})	
KM616FS1000Z	Commercial (0~70℃)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	80mA(Max) 50mA(Max)	5μA (max)	48-CSP (6x8 ball area with 0.75mm ball pitch)
KM616FR1000Z		1.8~2.7V	300*@Vcc=2.0±0.2V	25mA(Max)		
KM616FS1000ZI	Industria (-40~85℃)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	80mA(Max) 50mA(Max)	5μA (max)	
KM616FR1000ZI		1.8~2.7V	300*@Vcc=2.0±0.2V	25mA(Max)		

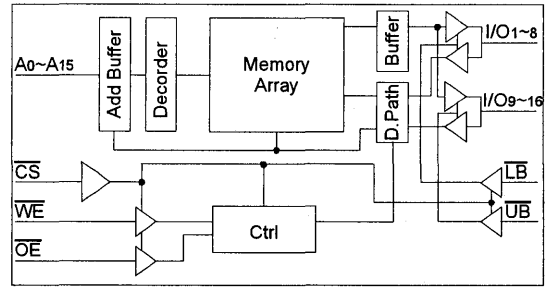
* The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_9	$\overline{UB}$	A_3	A_4	$\overline{CS}$	I/O_1
C	I/O_{10}	I/O_{11}	A_5	A_6	I/O_2	I/O_3
D	V_{SS}	I/O_{12}	NC	A_7	I/O_4	V_{CC}
E	V_{CC}	I/O_{13}	NC	NC	I/O_5	V_{SS}
F	I/O_{15}	I/O_{14}	A_{14}	A_{15}	I/O_6	I/O_7
G	I/O_{16}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_8
H	NC	A_8	A_9	A_{10}	A_{11}	NC

* See last page for package dimension.

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A_0~A_{15}	Address Inputs	$\overline{LB}$	Lower Byte(I/O_1 ~ 8)
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O_9 ~ 16)
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
I/O_1~I/O_{16}	Data Inputs/Outputs	N.C.	No Connection

PACKAGE DIMENSIONS (Units : mm)

	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08

Notes.

1. Bump counts : 48(8row x 6row)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is copianarity : 0.08(max)

256Kx8 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology : 0.4μm Full CMOS
- Organization : 256Kx8
- Power Supply Voltage
  KM68FV2000 Family : 3.0V(Min) ~ 3.6V(Max)
  KM68FS2000 Family : 2.3V(Min) ~ 3.3V(Max)
  KM68FR2000 Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

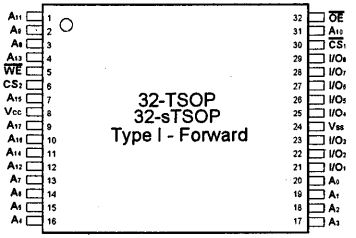
The KM68FV2000, KM68FS2000 and KM68FR2000 family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

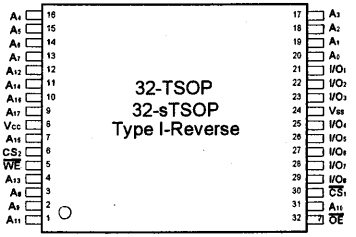
PRODUCT FAMILY

Product Family	Operating Temp.Range	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (Isb1)	Operating (Icc2)	
KM68FV2000	Commercial (0~70℃)	3.0~3.6V	70*/85@Vcc=3.3±0.3V	2μA***/10μA** (Max)	60mA(Max)	32-TSOP(I) Forward/ Reverse
KM68FS2000		2.3~3.3V	85@Vcc=3.0±0.3V 120*/150@VCC=2.5±0.2V		55mA(Max) 30mA(Max)	
KM68FR2000		1.8~2.7V	300*@Vcc=2.0±0.2V		15mA(Max)	
KM68FV2000I	Industria (-40~85℃)	3.0~3.6V	70*/85@Vcc=3.3±0.3V	2μA***/10μA** (Max)	60mA(Max)	32-TSOP(I) Forward/ Reverse
KM68FS2000I		2.3~3.3V	85@Vcc=3.0±0.3V 120*/150@VCC=2.5±0.2V		55mA(Max) 30mA(Max)	
KM68FR2000I		1.8~2.7V	300*@Vcc=2.0±0.2V		15mA(Max)	

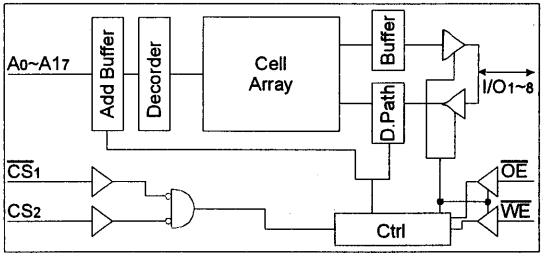
* measured with 30pF test load, ** for low power version, *** for super low power version with special handling.

PIN DESCRIPTION





FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A0~A17	Address Inputs	Vcc	Power
WE	Write Enable Input	Vss	Ground
CS1,CS2	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
OE	Output Enable	N.C.	No Connection

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST FOR LOW LOW POWER CONSUMPTION

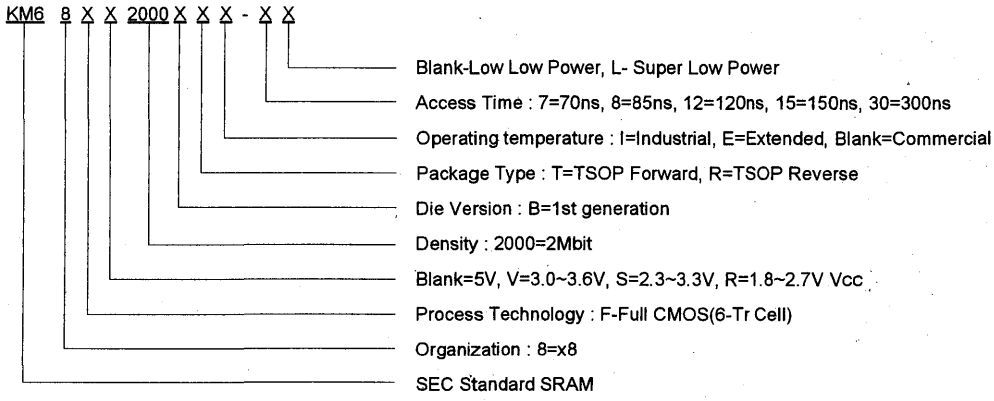
Commercial Temp Product (0~70℃)		Industrial Temp Product (-40~85℃)	
Part Name	Function	Part Name	Function
KM68FV2000T-7	32-TSOP F, 70ns, 3.3V, LL	KM68FV2000TI-7	32-TSOP F, 70ns, 3.3V, LL
KM68FV2000T-8	32-TSOP F, 85ns, 3.3V, LL	KM68FV2000TI-8	32-TSOP F, 85ns, 3.3V, LL
KM68FV2000R-7	32-TSOP R, 70ns, 3.3V, LL	KM68FV2000RI-7	32-TSOP R, 70ns, 3.3V, LL
KM68FV2000R-8	32-TSOP R, 85ns, 3.3V, LL	KM68FV2000RI-8	32-TSOP R, 85ns, 3.3V, LL
KM68FS2000T-12	32-TSOP F, 120/85ns, *2.5/3.0V, LL	KM68FS2000TI-12	32-TSOP F, 120/85ns, 2.5/3.0V, LL
KM68FS2000T-15	32-TSOP F, 150/85ns, 2.5/3.0V, LL	KM68FS2000TI-15	32-TSOP F, 150/85ns, 2.5/3.0V, LL
KM68FS2000R-12	32-TSOP R, 120/85ns, 2.5/3.0V, LL	KM68FS2000RI-12	32-TSOP R, 120/85ns, 2.5/3.0V, LL
KM68FS2000R-15	32-TSOP R, 150/85ns, 2.5/3.0V, LL	KM68FS2000RI-15	32-TSOP R, 150/85ns, 2.5/3.0V, LL
KM68FR2000T-30	32-TSOP F, 300ns, **2.0/2.5V, LL	KM68FR2000TI-30	32-TSOP F, 300ns, 2.0/2.5V, LL
KM68FR2000R-30	32-TSOP F, 300ns, 2.0/2.5V, LL	KM68FR2000RI-30	32-TSOP F, 300ns, 2.0/2.5V, LL

* The meaning of 2.5V/3.0V, 120/85ns is that the operating VCC is ranged from 2.3V(Min) to 3.3V(Max) with speed 120ns @2.5V±0.2 and 85ns @3.0V±0.3. This type of meaning is applied to other notations like the example.
** But in case of KM68FR2000T-30, there is only one speed bin, 300ns though it supports wide range operating VCC.

PRODUCT LIST FOR SUPER LOW POWER CONSUMPTION

The product names for super low power version has letter[L] at the end of product name of low low power version. The part name for 128Kx16 Super Low Power product operating at 2.3~3.3V with 85ns @ 3.0V and 120ns @ 2.5V will be KM68FS2000TI-12L.
And if suppliment is required for those products please contact Samsung Electronics Branch near your office. Samsung will support with special treatment.

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.2 to 3.6V[1]	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V[2]	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-55 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM68FV2000 KM68FS2000 KM68FR2000
		-40 to 85	℃	KM68FV2000I KM68FS2000I KM68FR2000I
Soldering temperature and time	T_{SOLDER}	260℃, 5sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
1) VIN/VOUT=0.2 to 3.9V for KM68FV2000 Family.
2) Maximum VCC=-0.2 to 4.6V for KM68FV2000 Family.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product		Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68FV2000 Family KM68FS2000 Family KM68FR2000 Family		3.0 2.3 1.8	3.3 2.5/3.0 2.0/2.5	3.6 3.3 2.7	V V V
Ground	Vss	All Family		0	0	0	V
Input high voltage	V_{IH}	KM68FV2000 Family	Vcc=3.3±0.3V	2.2	-	Vcc+0.2	V
		KM68FS2000 Family	Vcc=3.0±0.3V	2.2	-	Vcc+0.2	V
			Vcc=2.5±0.2V	2.0	-	Vcc+0.2	V
		KM68FR2000 Family	Vcc=2.5±0.2V	2.0	-	Vcc+0.2	V
			Vcc=2.5±0.2V	1.6	-	Vcc+0.2	V
Input low voltage	V_{IL}	All Family		-0.2***	-	0.4	V

* 1) Commercial Product : TA=0 to 70℃, unless otherwise specified
2) Industrial Product : TA=-40 to 85℃, unless otherwise specified
** TA=25℃
*** VIL(min)=-1.5V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	Vin=0V	-	8	pF
Input/Output capacitance	C_{IO}	Vio=0V	-	10	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Sym-bol	Test Conditions[1]			Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc			-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc			-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH} V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA		Read	-	-	$10^{5)}$	mA
					Write	-	-	$15^{5)}$	
Average operatingcurrent		I_{CC1}	Cycle time=1μs 100%duty $\overline{CS_1}$≤0.2V, CS_2≥V_{IN}≥Vcc-2.0V		Read	-	-	$10^{5)}$	mA
					Write	-	-	$15^{5)}$	
		I_{CC2}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IH} I_{IO}=0mA Min cycle, 100% duty		Vcc=3.3V@85ns	-	-	$55^{4)}$	mA
					Vcc=2.7V@120ns	-	-	30	
					Vcc=2.2V@300ns	-	-	15	
Output low voltage		V_{OL}	I_{OL}	Vcc=3.0/3.3V	2.1mA	-	-	0.4	V
				Vcc=2.5V	0.5mA	-	-	0.4	
				Vcc=2.0V	0.33mA	-	-	0.4	
Output high voltage		V_{OH}	I_{OH}	Vcc=3.0/3.3V	-1.0mA	2.4	-	-	V
				Vcc=2.5V	-0.5mA	2.0	-	-	
				Vcc=2.0V	-0.44mA	1.6	-	-	
Standby Current(TTL)		I_{SB}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL}			-	-	0.3	mA
Standby Current (CMOS)	KM68FV2000 KM68FS2000 KM68FR2000	I_{SB1}	$\overline{CS_1}$≥Vcc-2.0V CS_2≥Vcc-2.0V or CS_2≤0.2V Otherinput =0~Vcc		Super Low Power	-	$0.05^{3)}$	$2^{2)}$	μA
					Low Low Power	-	-	$10^{2)}$	
	KM68FV2000I KM68FS2000I KM68FR2000I				Super Low Power	-	$0.05^{3)}$	$2^{2)}$	μA
					Low Low Power	-	-	$10^{2)}$	

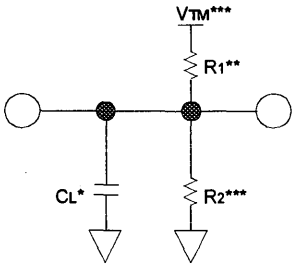
1) -Commercial Product
TA=0 to 70℃, Vcc=3.3±0.3V for 68FV2000 Family, Vcc=2.3(Min)~3.3V(Max)V for 68FS2000 Family,
Vcc=1.8(Min)~2.7V(Max)V for 68FR2000 Family.
-Industrial Product : TA=-40 to 85℃, Vcc=3.3±0.3V for 68FV2000I Family, Vcc=2.3(Min)~3.3V(Max)V for 68FS2000I Family,
Vcc=1.8(Min)~2.7V(Max)V for 68FR2000I Family.
2) The value has difference by ±1μA
Measured at Vcc=3.3(Max).
3) The value is not 100% tested but obtained statistically at Temp=25℃
4) - The value is measured at Vcc=3.0±0.3V
- ICC2=60mA with 70ns at Vcc=3.3±0.3V, but this value is not 100% tested but obtained statistically.
- ICC2=30mA with 120ns cycle at Vcc=2.5±0.2V, but this value is not 100% tested but obtained statistically.
- ICC2=15mA with 300ns cycle at Vcc=2.0±0.2V, but this value is not 100% tested but obtained statistically.
5) The value is measured ar Vcc=3.0±0.3V, The value measured at Vcc=2.5±2.0V is under the calue of Vcc=3.0±0.3V.

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	Vcc=3.3V, 3.0V, 2.5V
	0.4 to 1.8V	Vcc=2.0V
Input rise fall time	5ns	-
input and output reference voltage	1.5V	Vcc=3.3V, 3.0V
	1.1V	Vcc=2.5V
	0.9V	Vcc=2.0V,
Output load (See right)	CL=100pF	See Test Condition #2
	CL=30pF	

* See DC Operating conditions



* Including scope and jig capacitance
**R1=3070Ω, R2=3150Ω
***VTM=2.8V for VCC=3.0/3.3V
=2.3V for VCC=2.5V
=1.8V for VCC=2.0V

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Vcc Range	Typical Supply Vcc	Speed	Comments
KM68FR2000	0~70℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	Commercial
KM68FS2000	0~70℃	2.3(Min)~3.3(Max)	2.5V ± 0.2 Operation	120*/150ns	
			3.0V ± 0.3 Operation	85ns	
KM68FV2000	0~70℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	
KM68FR2000I	-40~85℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	Industrial
KM68FS2000I	-40~85℃	2.3(Min)~3.3(Max)	2.5V ± 0.2 Operation	120*/150ns	
			3.0V ± 0.3 Operation	85ns	
KM68FV2000I	-40~85℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	

* All the parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins												Units
			70ns		85ns		100ns		120ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Chip select to output	tCO1 tCO2	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Output enable to valid output	tOE	-	35	-	45	-	50	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ1 tLZ2	10	-	10	-	10	-	10	-	20	-	50	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	5	-	10	-	30	-	ns
	Chip disable to high-Z output	tHZ1 tHZ2	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output hold from address	tOH	10	-	15	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Chip select to end of write	tCW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	80	-	100	-	200	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	50	-	60	-	120	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	5	-	5	-	20	-	ns

* not yet available, only for reserved speed bins.

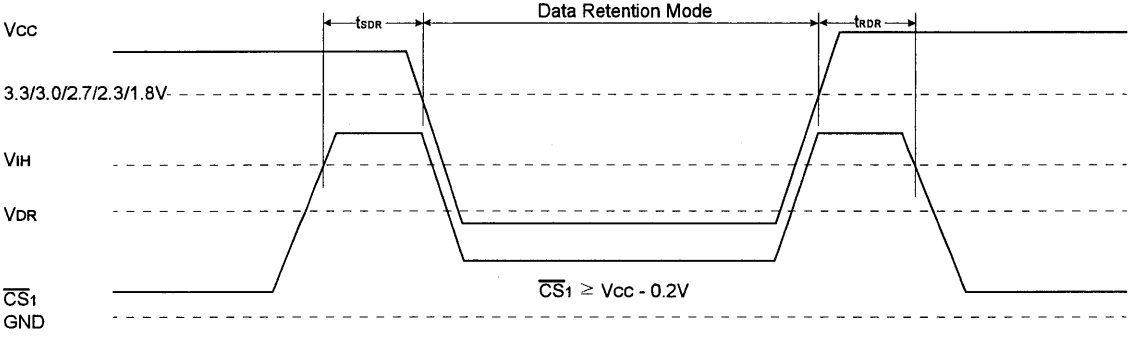
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS_1}$**** ≥ Vcc-2.0V		1.5	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V $\overline{CS_1}$ ≥ Vcc-0.2V	Super Low Power	***	0.1	2.0	μA
			Low Low Power	-	-	10	
Data retention set-up time	tSDR	See data retention waveform		0	-	-	ns
Recovery time	tRDR			tRC	-	-	

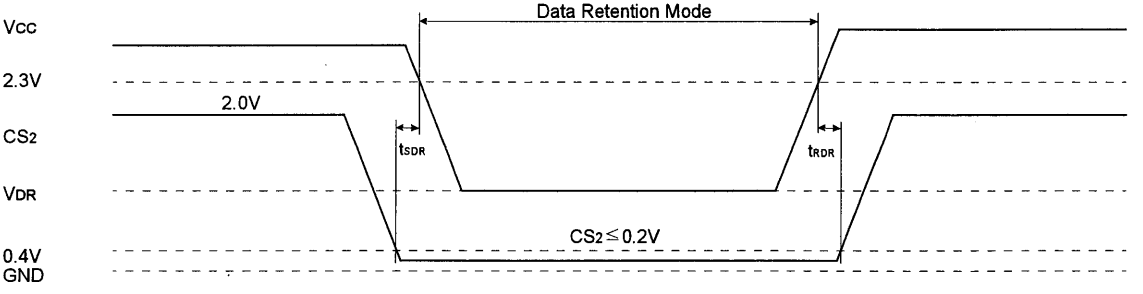
* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** TA=25℃, the value is too small to detect by test machine, 0.01μA statistically
*** The min value is almost 0nA statistically
**** $\overline{CS_1}$ ≥ Vcc-2.0V, CS_2 ≥ Vcc-2.0V($\overline{CS_1}$ controlled) or CS_2 ≤ 0.2V(CS_2 controlled)

DATA RETENTION WAVE FORM

1) $\overline{CS_1}$ controlled



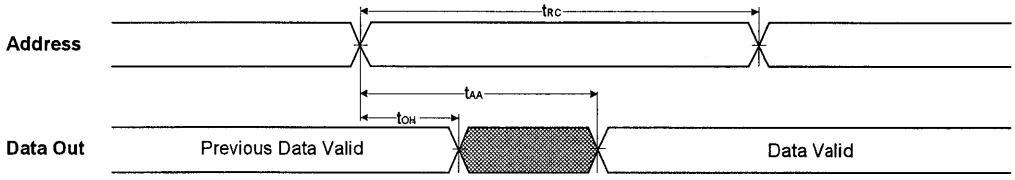
2) CS_2 controlled



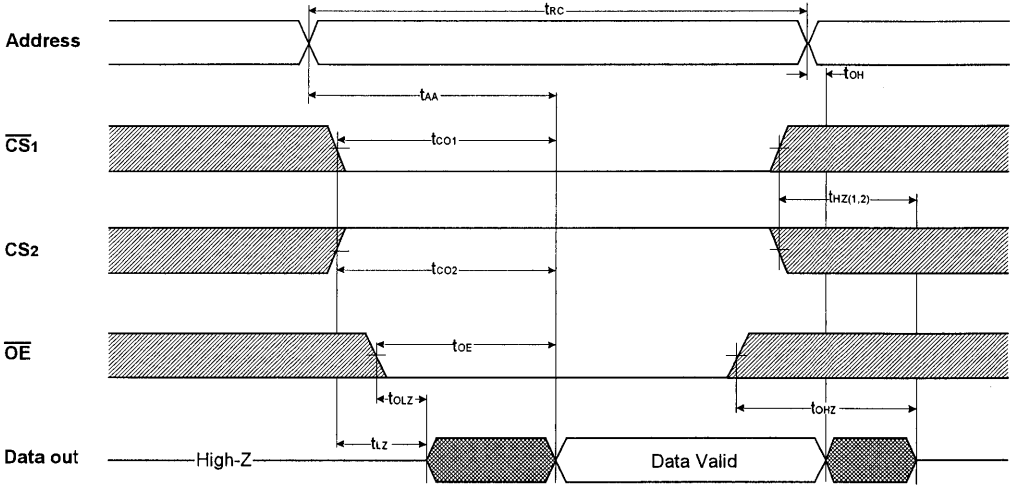
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



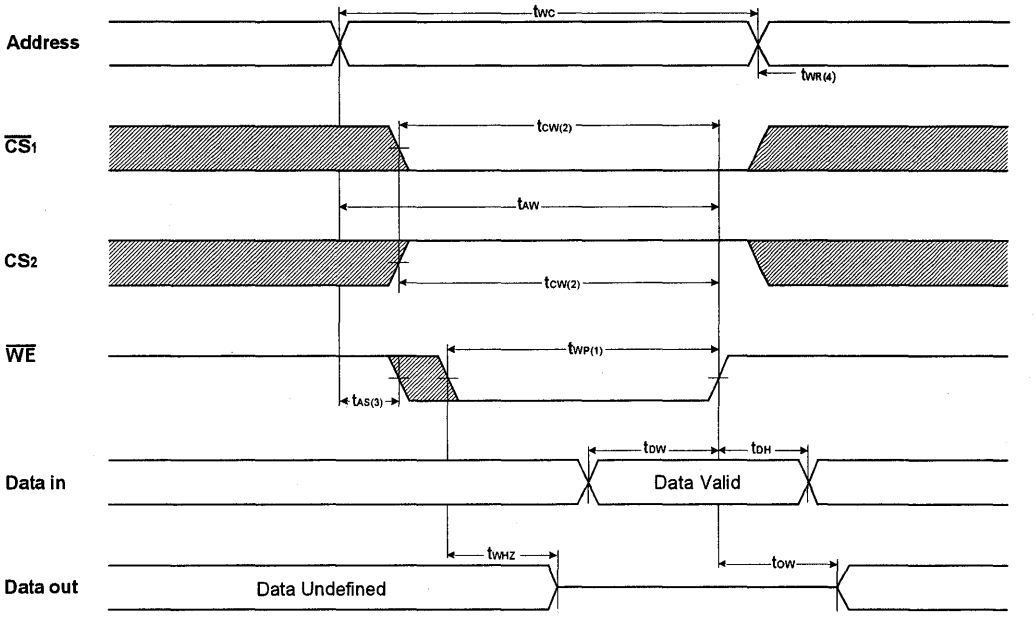
TIMING WAVEFORM OF READ CYCLE ($\overline{WE}$=V_{IH})



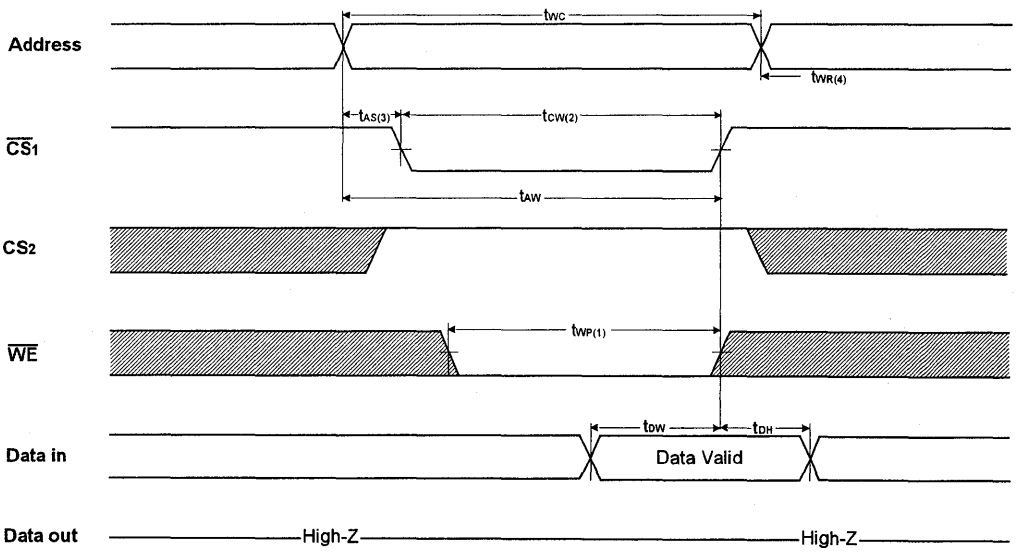
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device interconnection.

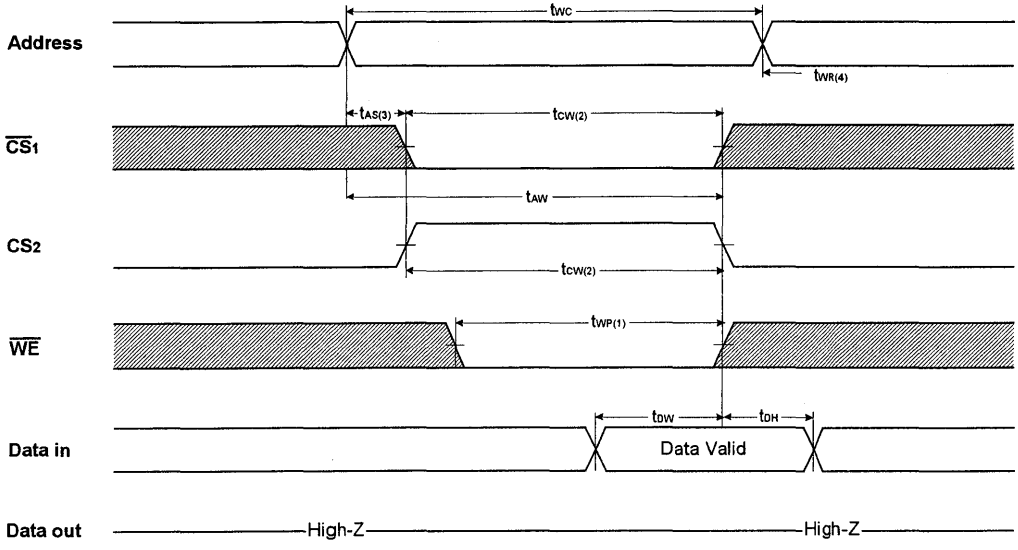
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS_2 Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high, tWP is measured from the begining of write to the end of write.
2. tCW is measured from the $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR(1) applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high tWR(2) applied in case a write ends as CS_2 going to low.

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Current Mode
H	X	X	X	Power Down	High-Z	I_{SB1}
X	L	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	Dout	I_{CC}
L	H	L	X	Write	Din	I_{CC}

* X means don't care (Must be in high or low states)

256Kx8 bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Size Package)

FEATURES

- Process Technology : 0.4μm Full CMOS
- Organization : 256Kx8
- Power Supply Voltage
  KM68FS2000Z Family : 2.3V(Min) ~ 3.3V(Max)
  KM68FR2000Z Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output and TTL Compatible
- Package Type : 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM68FS2000Z and KM68FR2000Z family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very samll from factor with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temp.Range	Vcc Range (min~max)	Speed(ns)	Power Dissipation		PKG Type
				Operating (I_{CC2})	Standby (I_{SB1})	
KM68FS2000Z	Commercial (0~70℃)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	55mA(Max) 30mA(Max)	10μA (max)	48-CSP (6x8 ball area with 0.75mm ball pitch)
KM68FR2000Z		1.8~2.7V	300*@Vcc=2.0±0.2V	15mA(Max)		
KM68FS2000ZI	Industria (-40~85℃)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	55mA(Max) 30mA(Max)	10μA (max)	
KM68FR2000ZI		1.8~2.7V	300*@Vcc=2.0±0.2V	15mA(Max)		

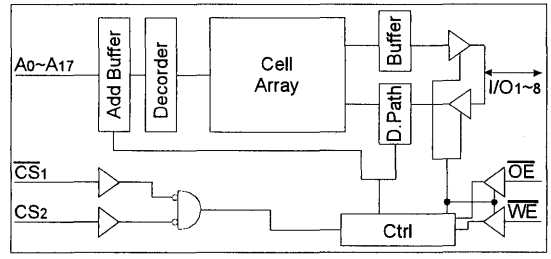
* The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
A	A_0	A_1	CS_2	A_3	A_6	A_8
B	I/O_5	A_2	$\overline{WE}$	A_4	A_7	I/O_1
C	I/O_6		NC	A_5		I/O_2
D	V_{SS}					V_{CC}
E	V_{CC}					V_{SS}
F	I/O_7		NC	A_{17}		I/O_3
G	I/O_8	$\overline{OE}$	$\overline{CS_1}$	A_{16}	A_{15}	I/O_4
H	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}

* See last page for package dimension.

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A_0~A_{17}	Address Inputs	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
$\overline{CS_1}$,CS_2	Chip Select Input	I/O_1~I/O_8	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input	N.C.	No Connection

PACKAGE DIMENSIONS (Units : mm)

	Min	Typ	Max
A	-	0.75	-
B	6.10	6.20	6.30
B1	-	3.75	-
C	13.65	13.75	13.85
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08

Notes.

1. Bump counts : 48(8row x 6row)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is copianarity : 0.08(max)

128Kx16 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology : 0.4μm Full CMOS
- Organization : 128Kx16
- Power Supply Voltage
  KM616FV2000 Family : 3.0V(Min) ~ 3.6V(Max)
  KM616FS2000 Family : 2.3V(Min) ~ 3.3V(Max)
  KM616FR2000 Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type : JEDEC Standard
  44-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

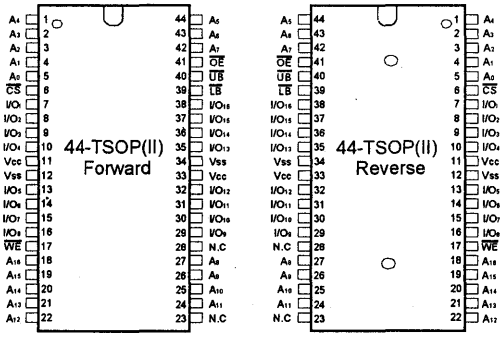
The KM616FV2000, KM616FS2000 and KM616FR2000 family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

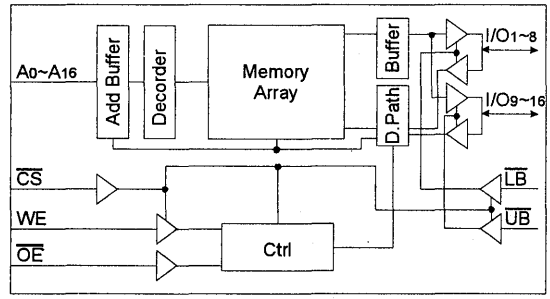
Product Family	Operating Temp.Range	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (Isb1)	Operating (Icc2)	
KM616FV2000	Commercial (0~70℃)	3.0~3.6V	70*/85@Vcc=3.3±0.3V	2μA*** /10μA** (Max)	80mA(Max)	44-TSOP(II) Forward/ Reverse
KM616FS2000		2.3~3.3V	85@Vcc=3.0±0.3V 120*/150@VCC=2.5±0.2V		80mA(Max) 50mA(Max)	
KM616FR2000		1.8~2.7V	300*@Vcc=2.0±0.2V		20mA(Max)	
KM616FV2000I	Industria (-40~85℃)	3.0~3.6V	70*/85@Vcc=3.3±0.3V	2μA*** /10μA** (Max)	80mA(Max)	44-TSOP(II) Forward/ Revers
KM616FS2000I		2.3~3.3V	85@Vcc=3.0±0.3V 120*/150@VCC=2.5±0.2V		80mA(Max) 50mA(Max)	
KM616FR2000I		1.8~2.7V	300*@Vcc=2.0±0.2V		20mA(Max)	

* measured with 30pF test load, ** for low power version, *** for super low power version with special handling.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A0~A16	Address Inputs	$\overline{LB}$	Lower Byte(I/O1~8)
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O9~16)
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable	Vss	Ground
I/O1~I/O16	Data Inputs/Out-	N.C.	No Connection

SAMSUNG ELECTRONICS

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST FOR LOW LOW POWER CONSUMPTION

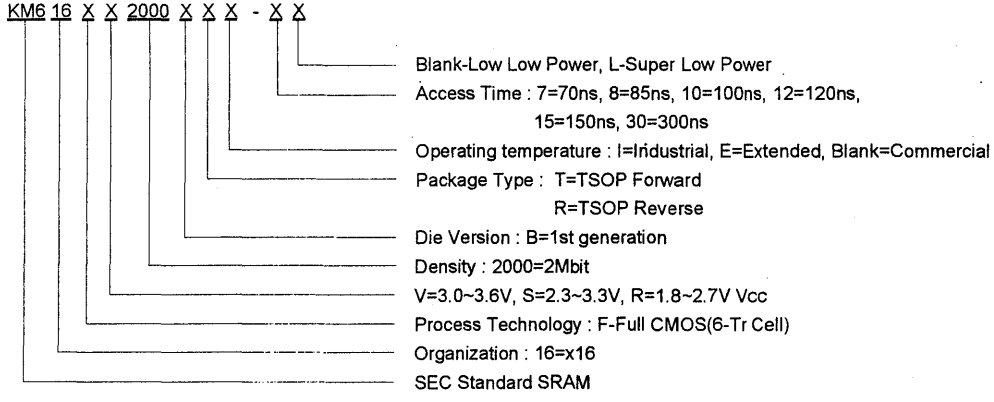
Commercial Temp Product (0~70℃)		Industrial Temp Product (-40~85℃)	
Part Name	**Function**	**Part Name**	**Function**
KM616FV2000T-7	44-TSOP F, 70ns, 3.3V, LL	KM616FV2000TI-7	44-TSOP F, 70ns, 3.3V, LL
KM616FV2000T-8	44-TSOP F, 85ns, 3.3V, LL	KM616FV2000TI-8	44-TSOP F, 85ns, 3.3V, LL
KM616FV2000R-7	44-TSOP R, 70ns, 3.3V, LL	KM616FV2000RI-7	44-TSOP R, 70ns, 3.3V, LL
KM616FV2000R-8	44-TSOP R, 85ns, 3.3V, LL	KM616FV2000RI-8	44-TSOP R, 85ns, 3.3V, LL
KM616FS2000T-12	44-TSOP F, 120/85ns, *2.5/3.0V, LL	KM616FS2000TI-12	44-TSOP F, 120/85ns, 2.5/3.0V, LL
KM616FS2000T-15	44-TSOP F, 150/85ns, 2.5/3.0V, LL	KM616FS2000TI-15	44-TSOP F, 150/85ns, 2.5/3.0V, LL
KM616FS2000R-12	44-TSOP R, 120/85ns, 2.5/3.0V, LL	KM616FS2000RI-12	44-TSOP R, 120/85ns, 2.5/3.0V, LL
KM616FS2000R-15	44-TSOP R, 150/85ns, 2.5/3.0V, LL	KM616FS2000RI-15	44-TSOP R, 150/85ns, 2.5/3.0V, LL
KM616FR2000T-30	44-TSOP F, 300ns, **2.0/2.5V, LL	KM616FR2000TI-30	44-TSOP F, 300ns, 2.0/2.5V, LL
KM616FR2000R-30	44-TSOP F, 300ns, 2.0/2.5V, LL	KM616FR2000RI-30	44-TSOP F, 300ns, 2.0/2.5V, LL

* The meaning of 2.5V/3.0V, 120/85ns is that the operating VCC is ranged from 2.3V(Min) to 3.3V(Max) with speed 120ns @2.5V±0.2 and 85ns @3.0V±0.3. This type of meaning is applied to other notations like the example.
** But in case of KM616FR2000T-30, there is only one speed bin, 300ns though it supports wide range operating VCC.

PRODUCT LIST FOR SUPER LOW POWER CONSUMPTION

The product names for super low power version has letter[L] at the end of product name of low low power version. The part name for 128Kx16 Super Low Power product operating at 2.3~3.3V with 85ns @ 3.0V and 120ns @ 2.5V will be KM616FA2000TI-12L.
And if suppliment is required for those products please contact Samsung Electronics Branch near your office. Samsung will support with special treatment.

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.2 to 3.6V[1]	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V[2]	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-55 to 150	℃	-
Operating Temperature	T_A	0 to 70	℃	KM616FV2000 KM616FS2000 KM616FR2000
		-40 to 85	℃	KM616FV2000I KM616FS2000I KM616FR2000I
Soldering temperature and time	T_{SOLDER}	260℃, 5sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1) V_{IN}/V_{OUT}=0.2 to 3.9V for KM616FV2000 Family.

2) Maximum V_{CC}=-0.2 to 4.6V for KM616FV2000 Family.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product		Min	Typ**	Max	Unit
Supply voltage	Vcc	KM616FV2000 Family KM616FS2000 Family KM616FR2000 Family		3.0 2.3 1.8	3.3 2.5/3.0 2.0/2.5	3.6 3.3 2.7	V V V
Ground	Vss	All Family		0	0	0	V
Input high voltage	V_{IH}	KM616FV2000 Family	Vcc=3.3±0.3V	2.2	-	Vcc+0.2	V
		KM616FS2000 Family	Vcc=3.0±0.3V	2.2	-	Vcc+0.2	V
			Vcc=2.5±0.2V	2.0	-	Vcc+0.2	V
		KM616FR2000 Family	Vcc=2.5±0.2V	2.0	-	Vcc+0.2	V
			Vcc=2.5±0.2V	1.6	-	Vcc+0.2	V
Input low voltage	V_{IL}	All Family		-0.2***	-	0.4	V

* 1) Commercial Product : T_A=0 to 70℃, unless otherwise specified
2) Industrial Product : T_A=-40 to 85℃, unless otherwise specified

** T_A=25℃

*** V_{IL}(min)=-1.5V for ≤ 30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	Vin=0V	-	8	pF
Input/Output capacitance	C_{IO}	Vio=0V	-	10	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Sym-	Test Conditions[1]			Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc			-1	-	1	μA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL},			-1	-	1	μA
Operating power supply current		I_{CC}	$\overline{CS}$=V_{IL} V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA		Read	-	-	10[5]	mA
					Write	-	-	20[5]	
Average operatingcurrent		I_{CC1}	Cycle time=1μs 100%duty $\overline{CS}$≤0.2V		Read	-	-	10[5]	mA
					Write	-	-	20[5]	
		I_{CC2}	$\overline{CS}$=V_{IH}, I_{IO}=0mA Min cycle, 100% duty		Vcc=3.3V@85ns	-	-	80[4]	mA
					Vcc=2.7V@120ns	-	-	60	
					Vcc=2.2V@300ns	-	-	25	
Output low voltage		V_{OL}	I_{OL}	Vcc=3.0/3.3V	2.1mA	-	-	0.4	V
				Vcc=2.5V	0.5mA	-	-	0.4	
				Vcc=2.0V	0.33mA	-	-	0.4	
Output high voltage		V_{OH}	I_{OH}	Vcc=3.0/3.3V	-1.0mA	2.4	-	-	V
				Vcc=2.5V	-0.5mA	2.0	-	-	
				Vcc=2.0V	-0.44mA	1.6	-	-	
Standby Current(TTL)		I_{SB}	$\overline{CS}$=V_{IH}			-	-	0.3	mA
Standby Current (CMOS)	KM616FV1000 KM616FS1000 KM616FR1000	I_{SB1}	$\overline{CS}$≥Vcc-2.0V Otherinput =0~Vcc		Super Low Power	-	0.05[3]	2[2]	μA
					Low Low Power	-	-	5[2]	
	KM616FV1000 KM616FS1000 KM616FR1000				Super Low Power	-	0.05[3]	2[2]	μA
					Low Low Power	-	-	5[2]	

1) -Commercial Product
T_A=0 to 70℃, Vcc=3.3±0.3V for 616FV2000 Family, Vcc=2.3(Min)~3.3V(Max)V for 616FS2000 Family,
Vcc=1.8(Min)~2.7V(Max)V for 616FR2000 Family.
-Industrial Product : T_A=-40 to 85℃, Vcc=3.3±0.3V for 616FV2000I Family, Vcc=2.3(Min)~3.3V(Max)V for 616FS2000I Family,
Vcc=1.8(Min)~2.7V(Max)V for 616FR2000I Family.

2) The value has difference by ±1μA
Measured at Vcc=3.3(Max).

3) The value is not 100% tested but obtained statistically at Temp=25℃

4) - The value is measured at Vcc=3.0±0.3V
- I_{CC2}=70mA with 70ns at Vcc=3.3±0.3V, but this value is not 100% tested but obtained statistically.
- I_{CC2}=40mA with 100ns cycle at Vcc=2.5±0.2V, but this value is not 100% tested but obtained statistically.
- I_{CC2}=20mA with 150ns cycle at Vcc=2.0±0.2V, but this value is not 100% tested but obtained statistically.

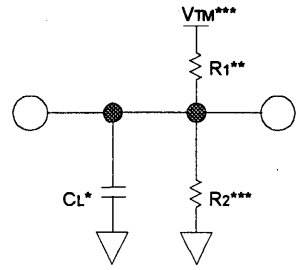
5) The value is measured ar Vcc=3.0±0.3V, The value measured at Vcc=2.5±2.0V is under the calue of Vcc=3.0±0.3V.

A.C CHARACTERISTICS

TEST CONDITIONS (1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	Vcc=3.3V, 3.0V, 2.5V
	0.4 to 1.8V	Vcc=2.0V
Input rise fall time	5ns	-
input and output reference voltage	1.5V	Vcc=3.3V, 3.0V
	1.1V	Vcc=2.5V
	0.9V	Vcc=2.0V,
Output load (See right)	C_L=100pF	See Test Condition #2
	C_L=30pF	

* See DC Operating conditions



* Including scope and jig capacitance
**R1=3070Ω, R2=3150Ω
***VTM=2.8V for VCC=3.0/3.3V
=2.3V for VCC=2.5V
=1.8V for VCC=2.0V

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Vcc Range	Typical Supply Vcc	Speed	Comments
KM616FR2000	0~70℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	Commercial
KM616FS2000	0~70℃	2.3(Min)~3.3(Max)	2.5V ± 0.2 Operation	120*/150ns	
			3.0V ± 0.3 Operation	85ns	
KM616FV2000	0~70℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	
KM616FR2000I	-40~85℃	1.8(Min)~2.7(Max)	2.0V ± 0.2 Operation	300*ns	Industrial
KM616FS200I0	-40~85℃	2.3(Min)~3.3(Max)	2.5V ± 0.2 Operation	120*/150ns	
			3.0V ± 0.3 Operation	85ns	
KM616FV2000I	-40~85℃	3.0(Min)~3.6(Max)	3.3V ± 0.3 Operation	70*/85ns	

* All the parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins												Units
			70ns		85ns		100ns		120ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Chip select to output	tCO1 tCO2	-	70	-	85	-	100	-	120	-	150	-	300	ns
	Output enable to valid output	tOE	-	35	-	45	-	50	-	60	-	75	-	150	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	35	-	45	-	50	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ1 tLZ2	10	-	10	-	10	-	20	-	20	-	50	-	ns
	Output enable to low-Z output	tOLZ tBLZ	5	-	5	-	5	-	20	-	20	-	30	-	ns
	Chip disable to high-Z output	tHZ1 tHZ2	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output disable to high-Z output	tOHZ tBHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Output hold from address	tOH	10	-	15	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	120	-	150	-	300	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	100	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	80	-	100	-	200	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	65	-	70	-	80	-	100	-	120	-	300	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	0	35	0	40	0	60	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	50	-	60	-	120	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	5	-	5	-	20	-	ns

* not yet available, only for reserved speed bins.

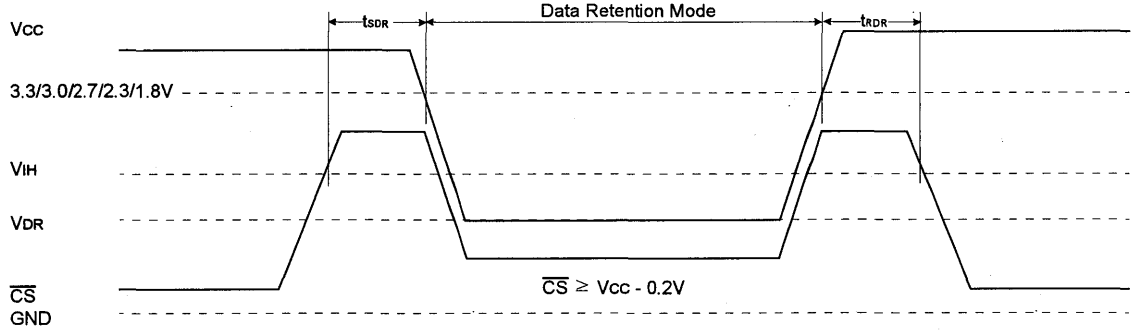
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS} \geq$ Vcc-2.0V		1.5	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V $\overline{CS} \geq$ Vcc-0.2V	Super Low Power	***	**	2.0	μA
			Low Low Power	-	-	5.0	
Data retention set-up time	tSDR	See data retention waveform		0	-	-	ns
Recovery time	tRDR			tRC	-	-	

* 1) Commercial Product : Ta=0 to 70℃, unless otherwise specified
2) Industrial Product : Ta=-40 to 85℃, unless otherwise specified
** T_A=25℃, the value is too small to detect by test machine, 0.01μA statistically
*** The min value is almost 0nA statistically

DATA RETENTION WAVE FORM

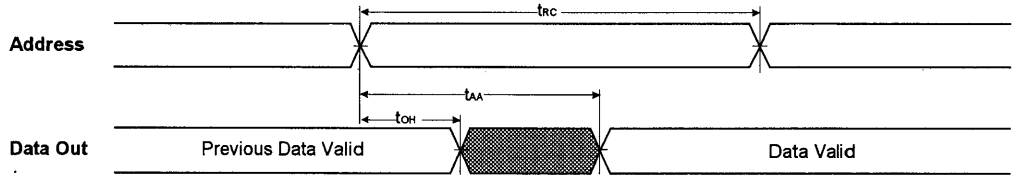
($\overline{CS}$ controlled)



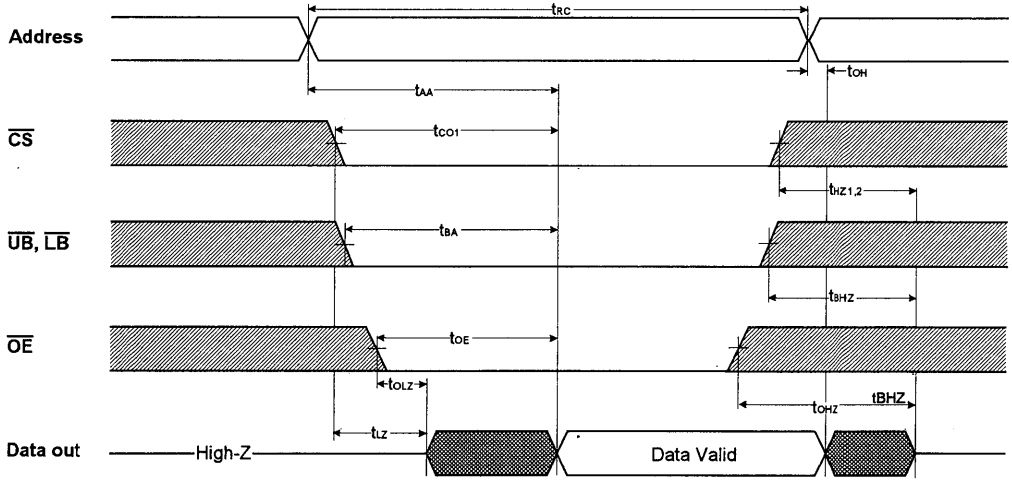
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

($\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH, $\overline{UB}$ or, and $\overline{LB}$=VIL)



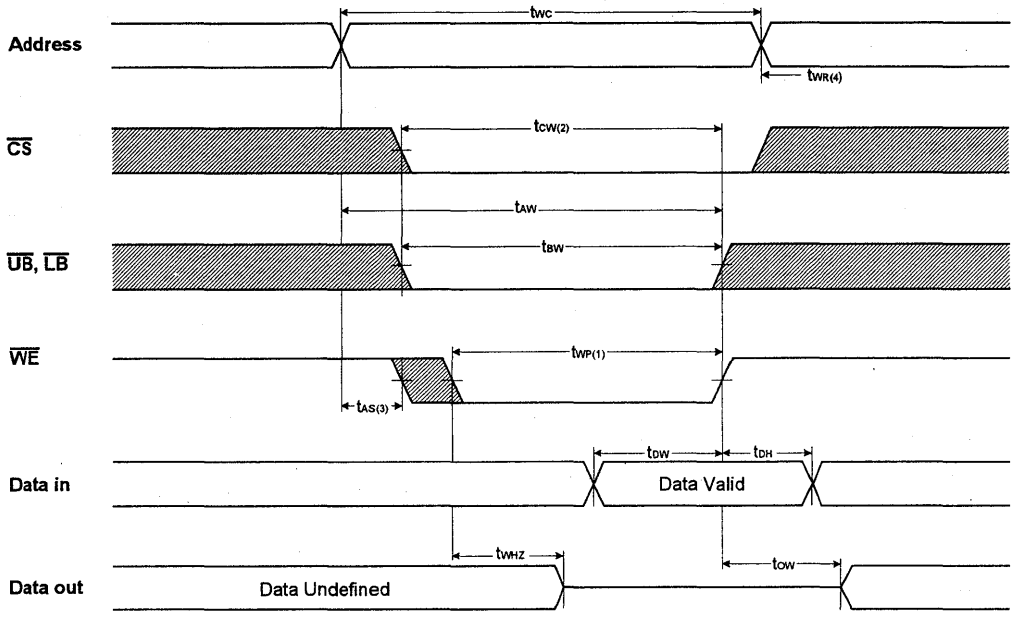
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



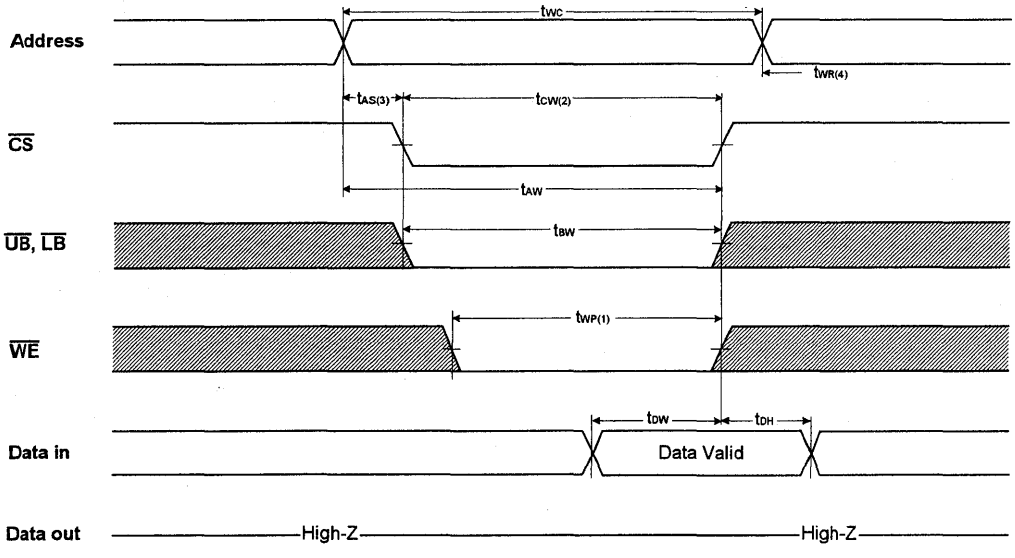
NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)

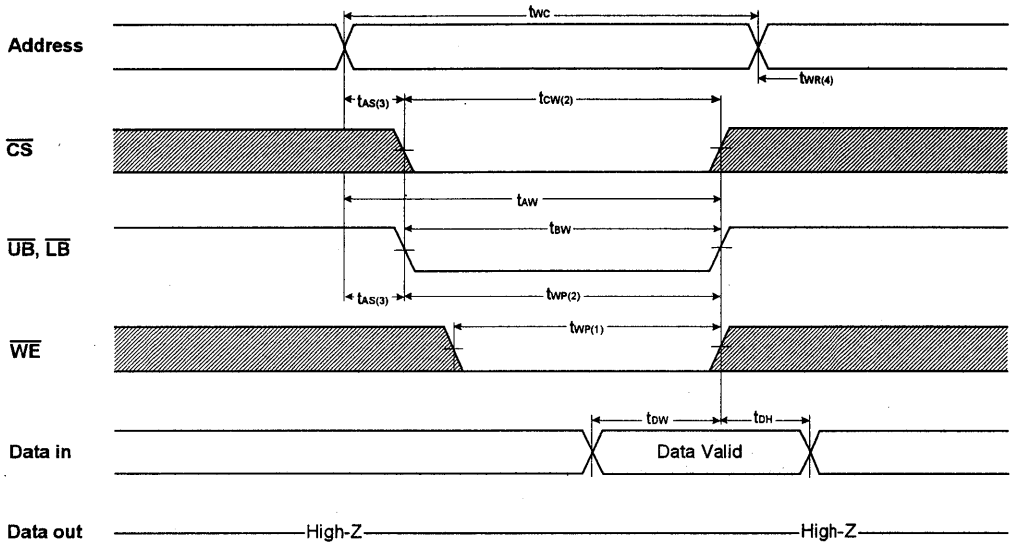


TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultenious asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{LB}$	$\overline{UB}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O1~8	I/O9~16	Current Mode
H	X	X	X	X	Not Select	High-Z	High-Z	I_{SB1}
L	X	X	H	H	Output Disable	High-Z	High-Z	Icc
L	H	H	X	X		High-Z	High-Z	
L	L	H	H	L	Read	Dout	High-Z	Icc
L	H	L	H	L		High-Z	Dout	
L	L	L	H	L		Dout	Dout	
L	L	H	L	X	Write	Din	High-Z	Icc
L	H	L	L	X		High-Z	Din	
L	L	L	L	X		Din	Din	

* X means don't care (Must be in high or low states)

128Kx16bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Size Package)

FEATURES

- Process Technology : 0.4μm Full CMOS
- Organization :128Kx16
- Power Supply Voltage
  KM616FS2000Z Family : 2.3V(Min) ~ 3.3V(Max)
  KM616FR2000Z Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type : 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM616FS2000Z and KM616FR2000Z family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very samll from factor with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temp.Range	Vcc Range (min~max)	Speed(ns)	Power Dissipation		PKG Type
				Operating (Icc2)	Standby (I_{SB1})	
KM616FS2000Z	Commercial (0~70℃)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	80mA(Max) 50mA(Max)	10μA (max)	48-CSP (6x8 ball area with 0.75mm ball pitch)
KM616FR2000Z		1.8~2.7V	300*@Vcc=2.0±0.2V	25mA(Max)		
KM616FS2000ZI	Industria (-40~85℃)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	80mA(Max) 50mA(Max)	10μA (max)	
KM616FR2000ZI		1.8~2.7V	300*@Vcc=2.0±0.2V	25mA(Max)		

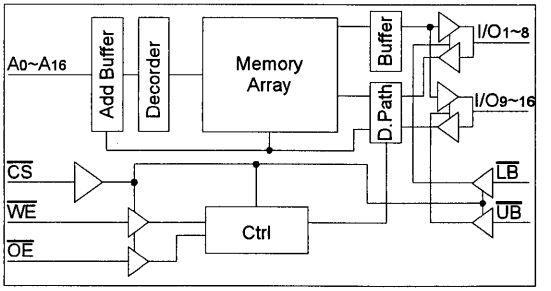
* The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_9	$\overline{UB}$	A_3	A_4	$\overline{CS}$	I/O_1
C	I/O_{10}	I/O_{11}	A_5	A_6	I/O_2	I/O_3
D	V_{SS}	I/O_{12}	NC	A_7	I/O_4	V_{CC}
E	V_{CC}	I/O_{13}	NC	A_{16}	I/O_5	V_{SS}
F	I/O_{15}	I/O_{14}	A_{14}	A_{15}	I/O_6	I/O_7
G	I/O_{16}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_8
H	NC	A_8	A_9	A_{10}	A_{11}	NC

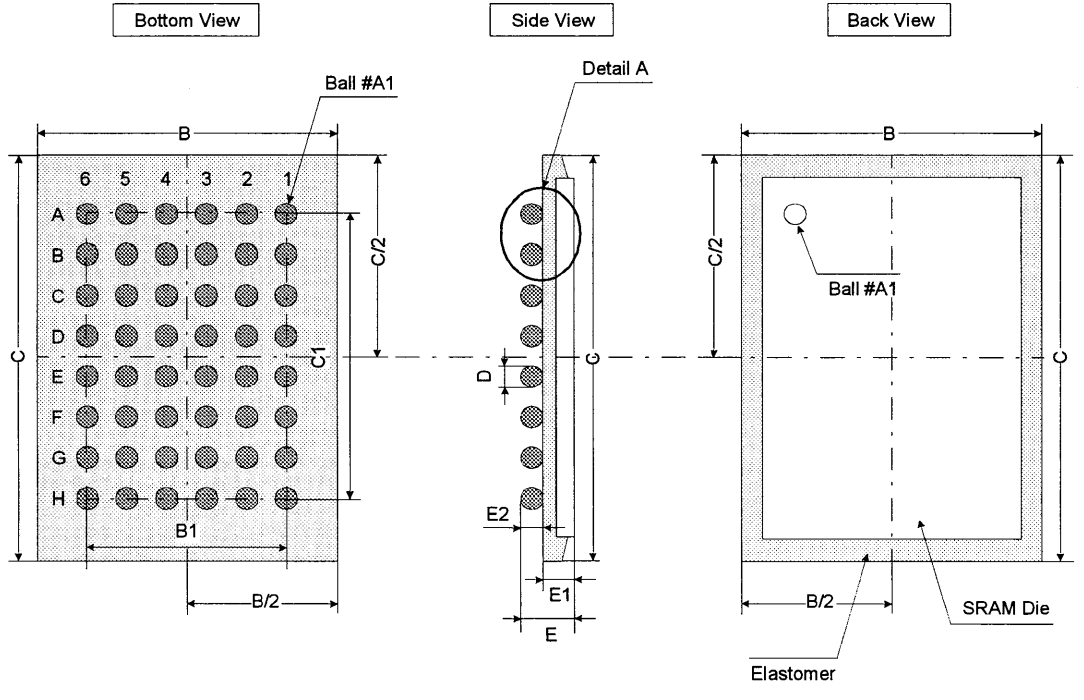
* See last page for package dimension.

FUNCTIONAL BLOCK DIAGRAM

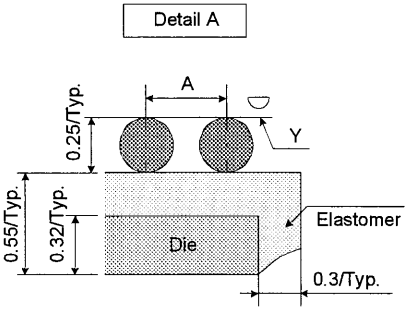


Name	Function	Name	Function
A_0~A_{16}	Address Inputs	$\overline{LB}$	Lower Byte(I/O_1 ~ 8)
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O_9 ~ 16)
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
I/O_1~I/O_{16}	Data Inputs/Outputs	N.C.	No Connection

PACKAGE DIMENSIONS (Units : mm)



	Min	Typ	Max
A	-	0.75	-
B	6.10	6.20	6.30
B1	-	3.75	-
C	13.65	13.75	13.85
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08



Notes.

1. Bump counts : 48(8row x 6row)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is copianarity : 0.08(max)

Application Specification Memory for Mobile Communication

KM88FS87, KM88FR87 Family

Integrated 256K x 8 bit MaskROM with 128K x 8 bit SRAM

FEATURES

- Process Technology : 0.4㎛ Full CMOS
- Both ROM and RAM in one chip
- Organization : 256Kx8(ROM),
  128K x 8(SRAM)
- Power Supply Voltage
  KM88FS87 Family : 2.3V(Min) ~ 2.7V(Max)
  KM88FR87 Family : 1.8V(Min) ~ 2.2V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type : 32-TSOP I - Forward
  32-sTSOP I - Forward

GENERAL DESCRIPTION

The KM88FS87 is fabricated by SAMSUNG's advanced Full CMOS process technology. The family is a combination chip consist of 2Mbit ROM organized as 256K words by 8bits and 1Mbit SRAM organized as 128K words by 8bits.

The family can support various operating temperature ranges and super low voltage operation. The family also support low data retention voltage for battery back-up operations with low data retention current.

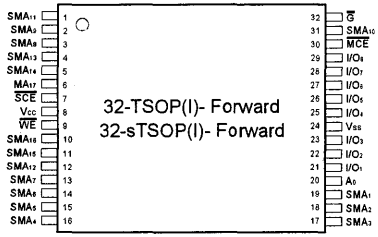
2

PRODUCT FAMILY

Product Family	Operating Temp.Range	Vcc Range	Speed (ns)*	PKG Type	Power Dissipation	
					Standby (I_{SB1}, Max)	Operating (I_{CC2})
KM88FS87	Commercial (0~70℃)	2.3~2.7V	250/500	32-TSOP I 32-sTSOP I Forward	5㎂	7/5mA
KM88FR87		1.8~2.2V	250/500			4/3mA
KM88FS87I	Industria (-40~85℃)	2.3~2.7V	250/500			7/5mA
KM88FR87I		1.8~2.2V	250/500			4/3mA

* measured with 30pF test load

PIN DESCRIPTION



Name	Function	I/O
SMA0~16	Addresses for ROM & SRAM array	I
MA17	MSB address for only ROM	I
$\overline{SCE}$	SRAM array select	I
$\overline{MCE}$	ROM array select	I
$\overline{WE}$	SRAM Write Enable	I
$\overline{G}$	Output Enable	I
I/O1~8	Inputs & Output signals	I/O

* MA17 is used only for ROM

ADDRESS SCRAMBLE

	LSB ..... MSB
SRAM	SMA0, ... SMA16
ROM	SMA0, ... SMA16, MA17*

* MA17 is not used for 128Kx8 RAM

KEY APPLICATION

Alpha-numeric pager, CT2, Cellular phone, POS, PDA, Electronic Data Bank, etc.

256K High Speed SRAM
(5.0V Operation)

64K x 4 Bit High-Speed BiCMOS Static RAM

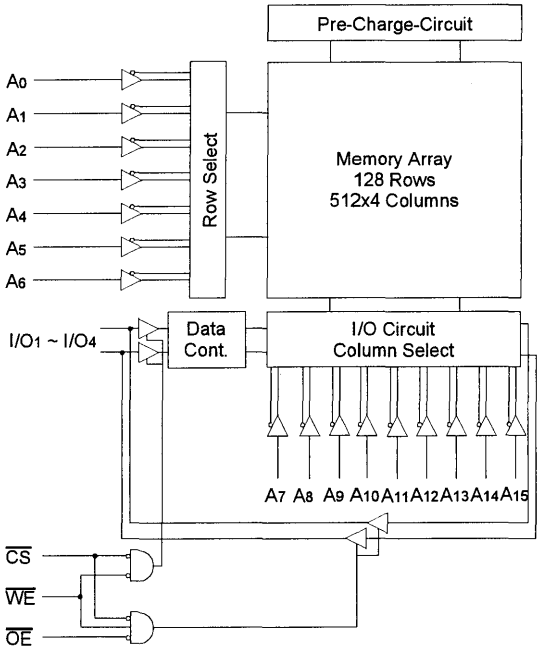
FEATURES

- Fast Access Time 6, 7, 8, ns (Max.)
- Low Power Dissipation
  Standby (TTL) : 90mA(Max.)
  (CMOS) : 20mA(Max.)
  Operating Current : 160mA(f=100MHz)
- Single 5.0V ± 5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  KM64B261AJ : 28-SOJ-300

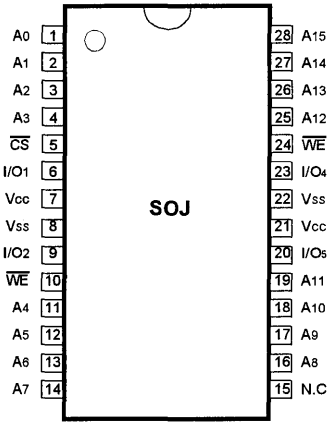
GENERAL DESCRIPTION

The KM64B261A is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits. The KM64B261A uses four common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64B261A is packaged in a 300 mil 28-pin plastic SOJ .

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0(Pulse Width≤3ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V(Pulse Width≤8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc	-10	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc	-10	10	μA
Operating Current	I_{CC}	f=100MHz, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	-	160	mA
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}	-	90	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	-	20	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA	-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA	2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

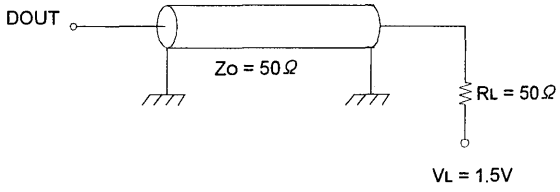
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V ± 5%, unless otherwise noted.)

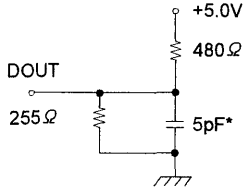
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

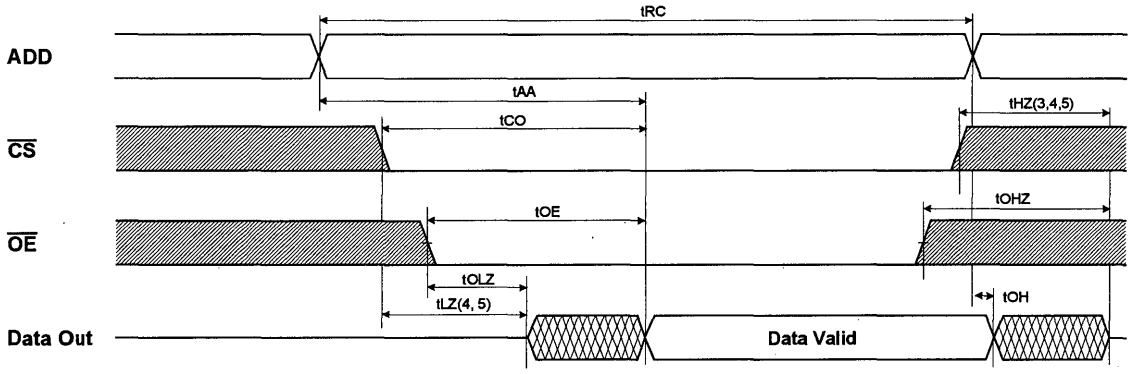
Parameter	Symbol	KM64B261A-6		KM64B261A-7		KM64B261A-8		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	6	-	7	-	8	-	ns
Address Access Time	tAA	-	6	-	7	-	8	ns
Chip Select to Output	tCO	-	6	-	7	-	8	ns
Output Enable to Valid Output	tOE	-	4	-	4	-	4	ns
Chip Enable to Low-Z Output Access Time	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	1	-	1	-	1	-	ns
Chip Disable to High-Z Output	tHZ	0	3	0	3.5	0	4	ns
Output Disable to High-Z Output	tOHZ	0	3	0	3.5	0	4	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM64B261A-6		KM64B261A-7		KM64B261A-8		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	6	-	7	-	8	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	3.5	-	4	-	4.5	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	3.5	-	4	-	4.5	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	6	-	7	-	8	-	ns
Write Recovery Time	tWR	1	-	1	-	1	-	ns
Write to Output High-Z	tWHZ	0	3	0	3.5	0	4	ns
Data to Write Time Overlap	tDW	3	-	3.5	-	4	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

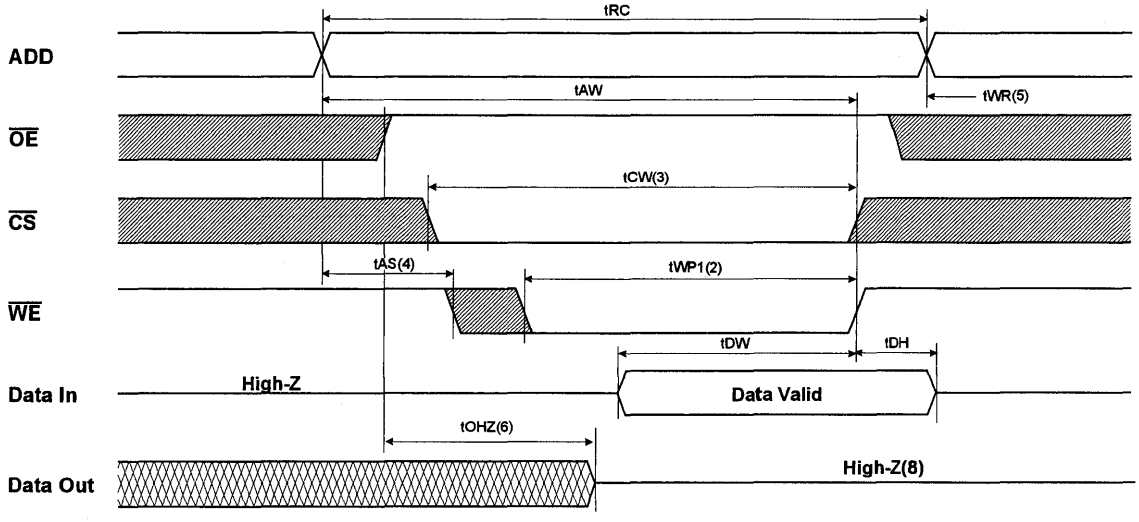
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



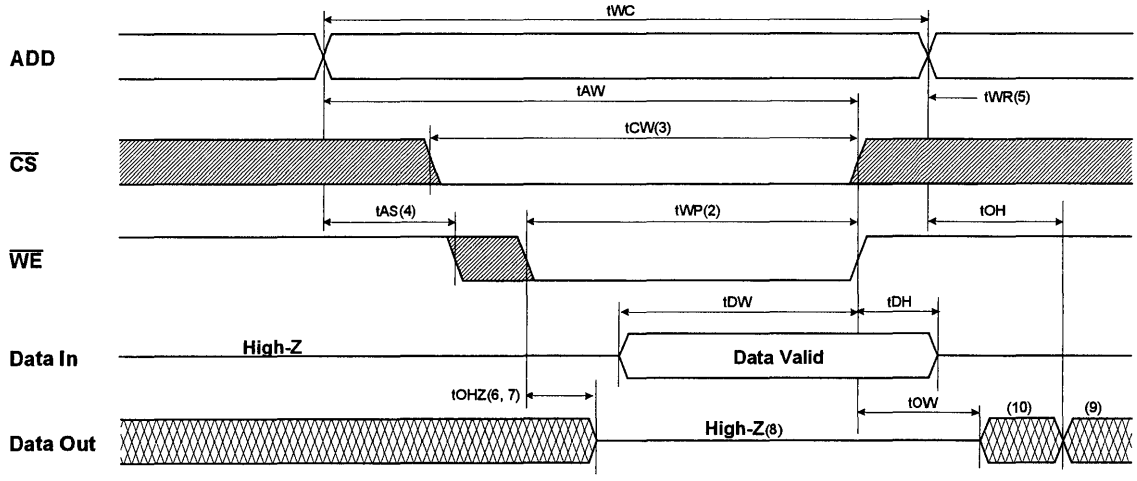
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200㎷ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

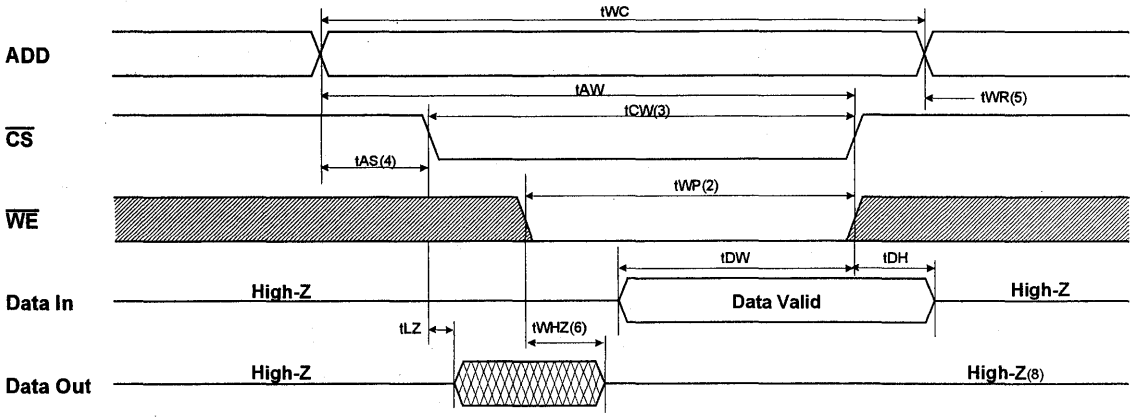
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

64K x 4 Bit High-Speed CMOS Static RAM

FEATURES

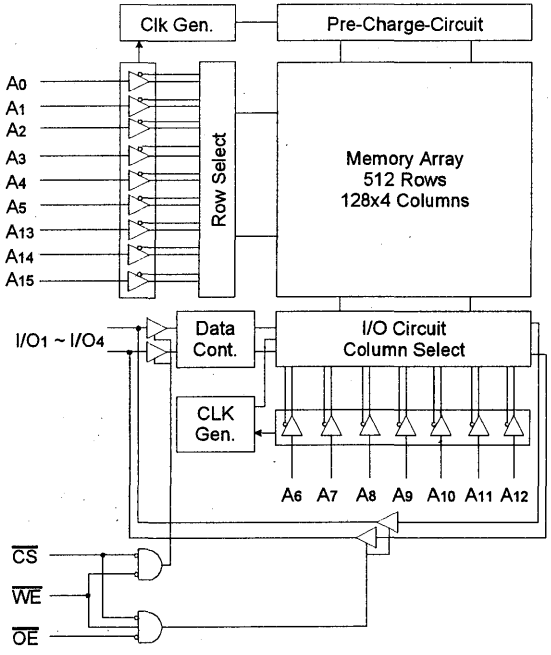
- Fast Access Time 12, 15, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 2mA(Max.)
  - Operating KM64258C - 12 : 150mA(Max.)
  - KM64258C - 15 : 140mA(Max.)
  - KM64258C - 20 : 130mA(Max.)
- Single 5.0V ±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible With 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM64258CP : 28-DIP-300
  - KM64258CJ : 28-SOJ-300

GENERAL DESCRIPTION

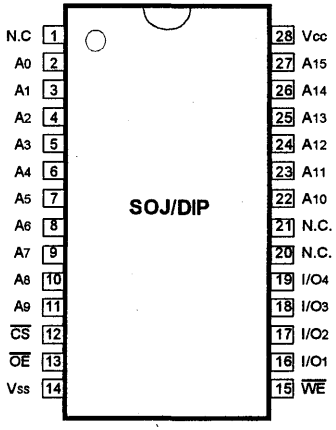
The KM64258C is a 262,144-bit high-speed Static Random Access Memory organized as 65,536 words by 4 bits. The KM64258C uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64258C is packaged in a 300 mil 28-pin plastic DIP or SOJ .

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V(Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	17ns	-	150	mA
			20ns	-	140	
			25ns	-	130	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IH} or V_{IN} ≤ 0.2V		-	2	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

* **NOTE** : Vcc= 5.0V ± 5%, Temp.=25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

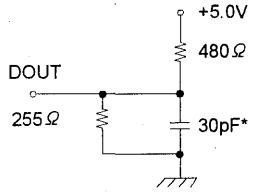
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0℃ to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

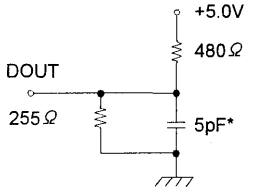
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

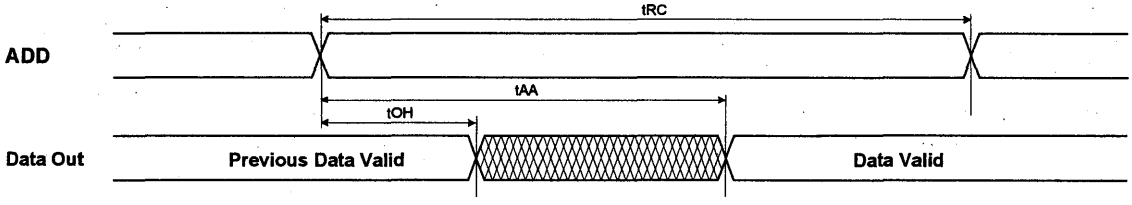
Parameter	Symbol	KM64258C-12		KM64258C-15		KM64258C-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	9	ns
Chip Enable to Low-Z Output Access	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	10	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	10	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	12	-	15	-	20	ns

WRITE CYCLE

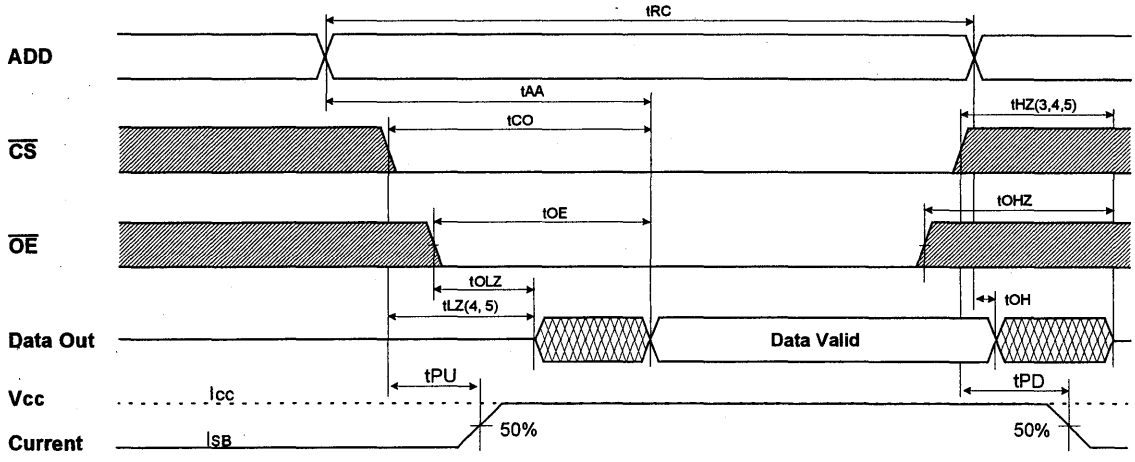
Parameter	Symbol	KM64258C-12		KM64258C-15		KM64258C-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	15	-	20	-	ns
Chip Select to End of Write	tCW	9	-	11	-	13	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	9	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	12	-	15	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	0	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



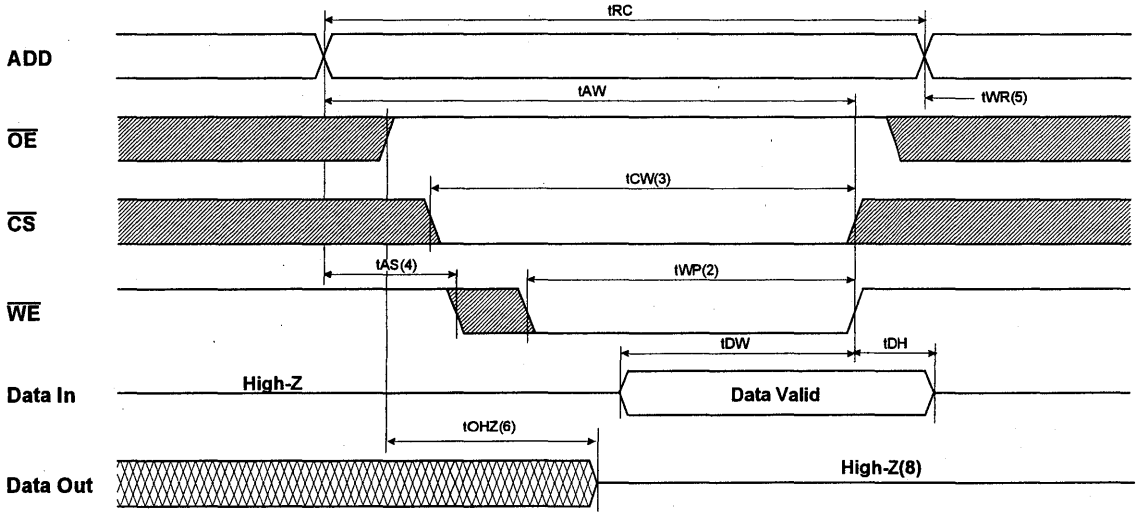
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

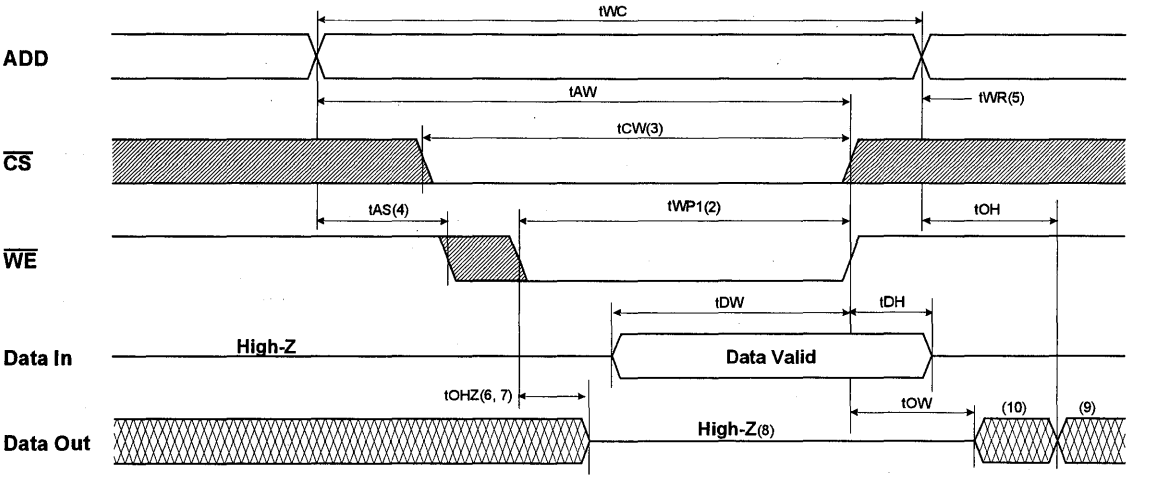
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

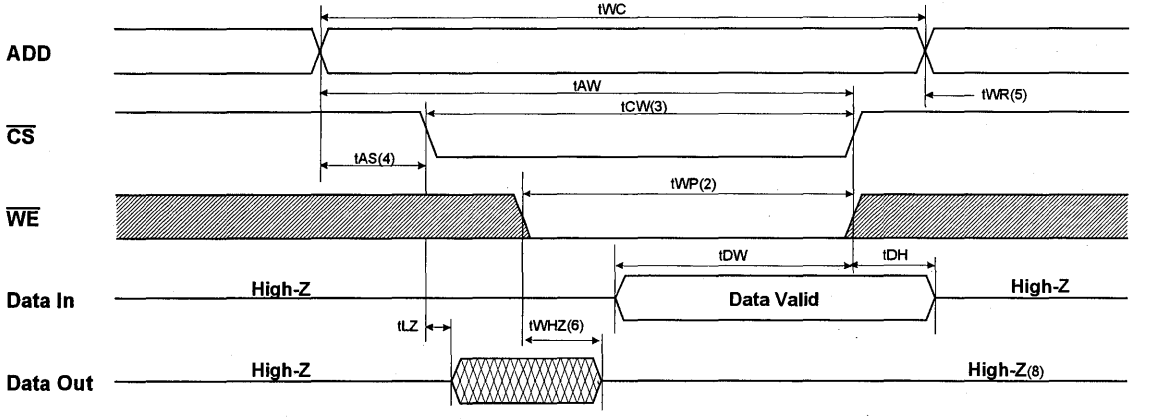


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

32K x 8 Bit High-Speed BiCMOS Static RAM

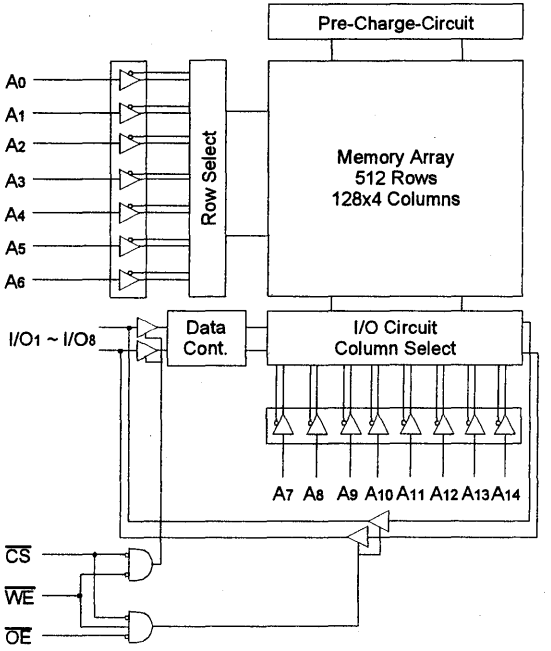
FEATURES

- Fast Access Time 6, 7, 8, ns(Max.)
- Low Power Dissipation
  Standby (TTL) : 110mA(Max.)
  (CMOS) : 20mA(Max.)
  Operating Current : 170mA(f=100MHz)
- Single 5.0V± 5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  KM68B261AJ : 32-SOJ-300

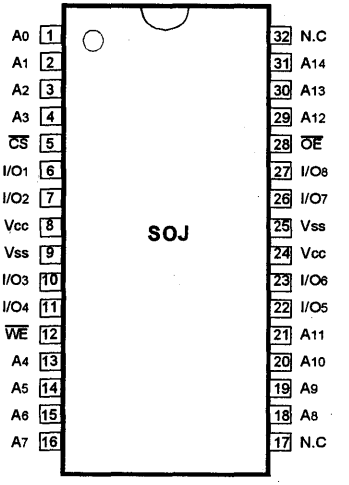
GENERAL DESCRIPTION

The KM68B261A is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits. The KM68B261A uses eight common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68B261A is packaged in a 300 mil 32-pin plastic SOJ .

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A14	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0(Pulse Width≤3ns) for I ≤ 20mA

** V_{IH}(Max) = V_{CC} + 2.0V(Pulse Width≤8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, V_{CC}= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc	-10	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc	-10	10	μA
Operating Current	I_{CC}	f=100MHz, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	-	170	mA
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}	-	110	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	-	20	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA	-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA	2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

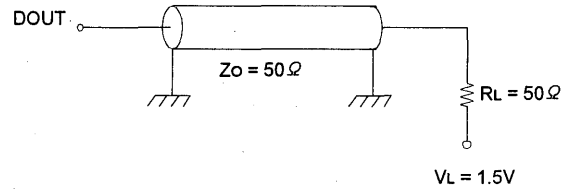
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

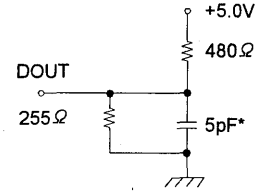
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68B261A-6		KM68B261A-7		KM68B261A-8		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	6	-	7	-	8	-	ns
Address Access Time	tAA	-	6	-	7	-	8	ns
Chip Select to Output	tCO	-	6	-	7	-	8	ns
Output Enable to Valid Output	tOE	-	4	-	4	-	4	ns
Chip Enable to Low-Z Output Access	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	1	-	1	-	1	-	ns
Chip Disable to High-Z Output	tHZ	0	3	0	3.5	0	4	ns
Output Disable to High-Z Output	tOHZ	0	3	0	3.5	0	4	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

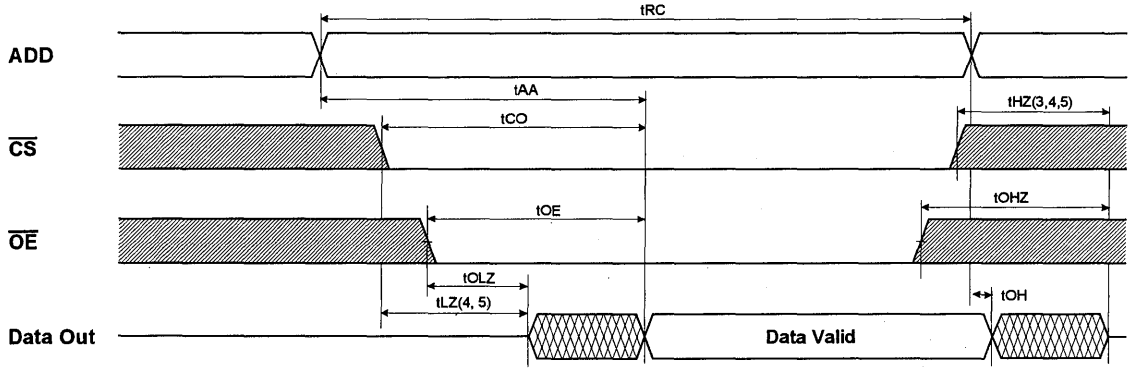
WRITE CYCLE

Parameter	Symbol	KM68B261A-6		KM68B261A-7		KM68B261A-8		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	6	-	7	-	8	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	3.5	-	4	-	4.5	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	3.5	-	4	-	4.5	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	6	-	7	-	8	-	ns
Write Recovery Time	tWR	1	-	1	-	1	-	ns
Write to Output High-Z	tWHZ	0	3	0	3.5	0	4	ns
Data to Write Time Overlap	tDW	3	-	3.5	-	4	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

2

TIMING DIAGRAMS

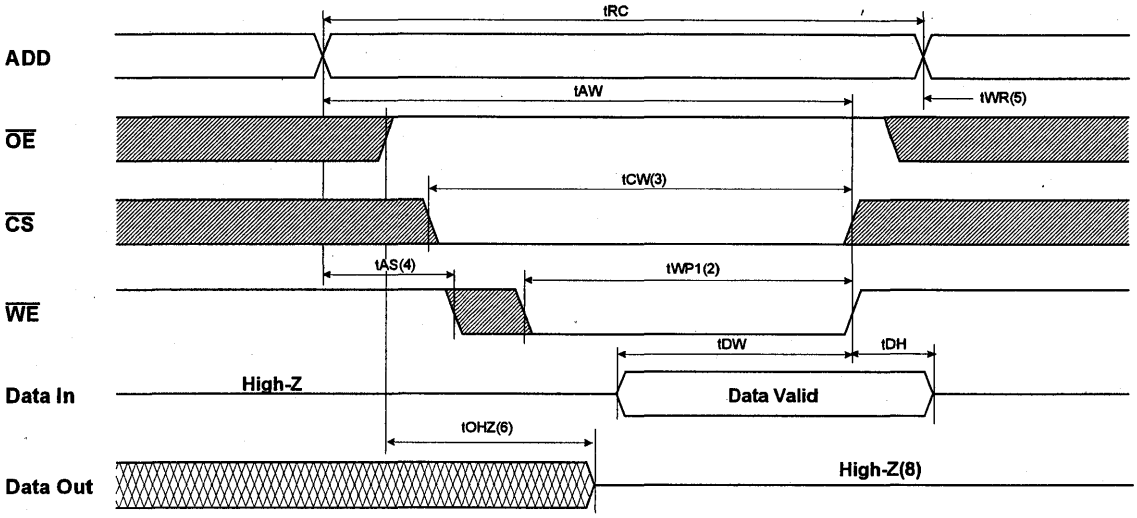
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



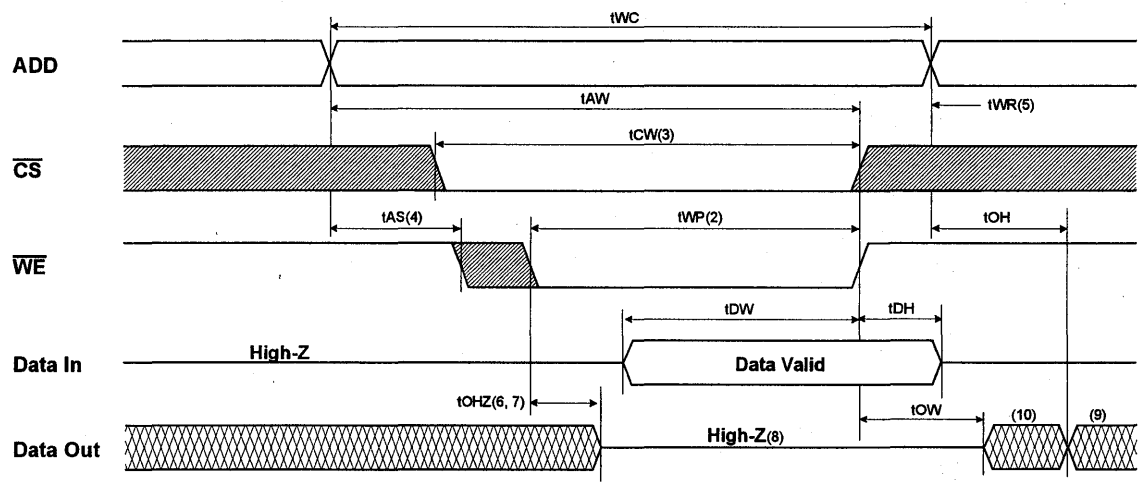
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

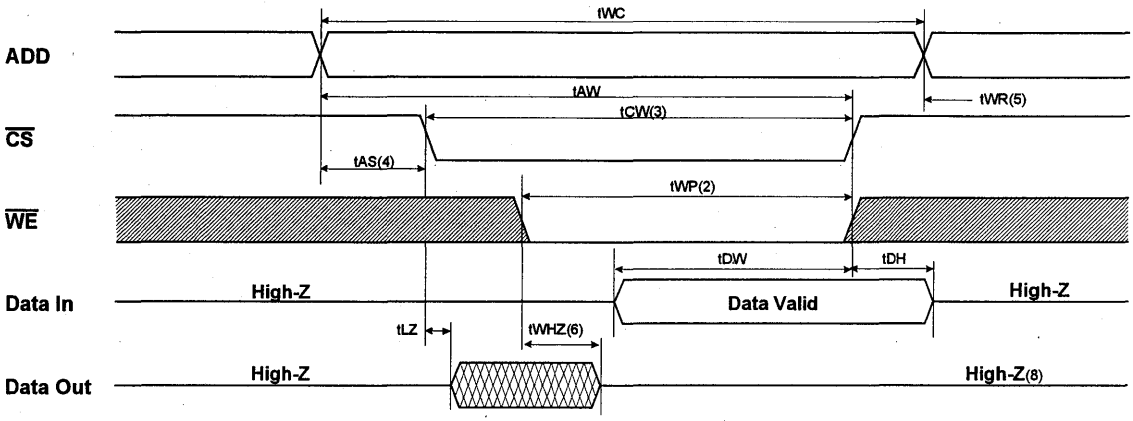
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

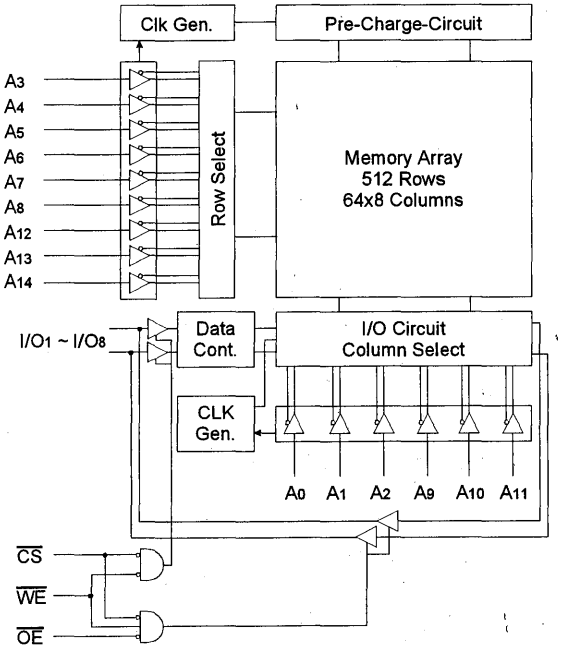
* **NOTE** : X means Don't Care.

32K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12, 15, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 2mA(Max.)
  - 0.1mA(Max.)- L-ver. only
  - Operating KM68257C/CL - 12 : 165mA(Max.)
  - KM68257C/CL - 15 : 150mA(Max.)
  - KM68257C/CL - 20 : 140mA(Max.)
- Single 5.0V ± 10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage : 2V (min.)- L-ver. only
- Standard Pin Configuration
  - KM68257C/CLP : 28-DIP-300
  - KM68257C/CLJ : 28-SOJ-300
  - KM68257C/CLTG : 28-TSOP1-0813, 4F

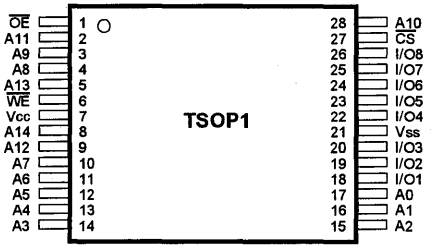
FUNCTIONAL BLOCK DIAGRAM

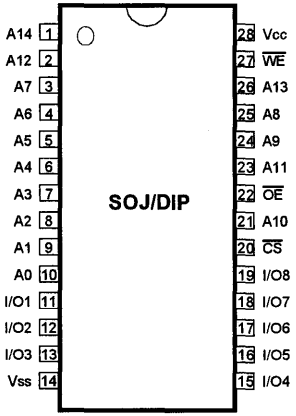


GENERAL DESCRIPTION

The KM68257C is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits. The KM68257C uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68257C is packaged in a 300 mil 28-pin plastic DIP, SOJ or TSOP1 forward.

PIN CONFIGURATION *(Top View)*





PIN FUNCTION

Pin Name	Pin Function
A_0 - A_{14}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1 ~ I/O_8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V(Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc=5.0V ± 10% unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	165	mA
			15ns	-	150	
			20ns	-	140	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	2	mA
			L-ver	-	0.1	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=0.1mA		-	3.95	V

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

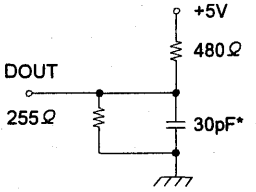
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0℃ to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

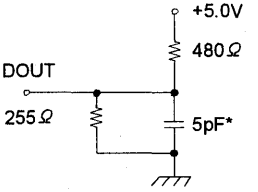
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68257C/CL-12		KM68257C/CL-15		KM68257C/CL-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	9	ns
Chip Enable to Low-Z Output Access Time	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	10	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	10	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	12	-	15	-	20	ns

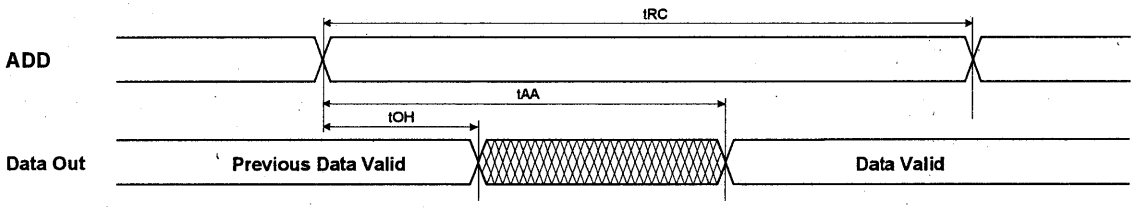
WRITE CYCLE

Parameter	Symbol	KM68257C/CL-12		KM68257C/CL-15		KM68257C/CL-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	15	-	20	-	ns
Chip Select to End of Write	tCW	9	-	11	-	13	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	9	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	12	-	15	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	0	-	ns

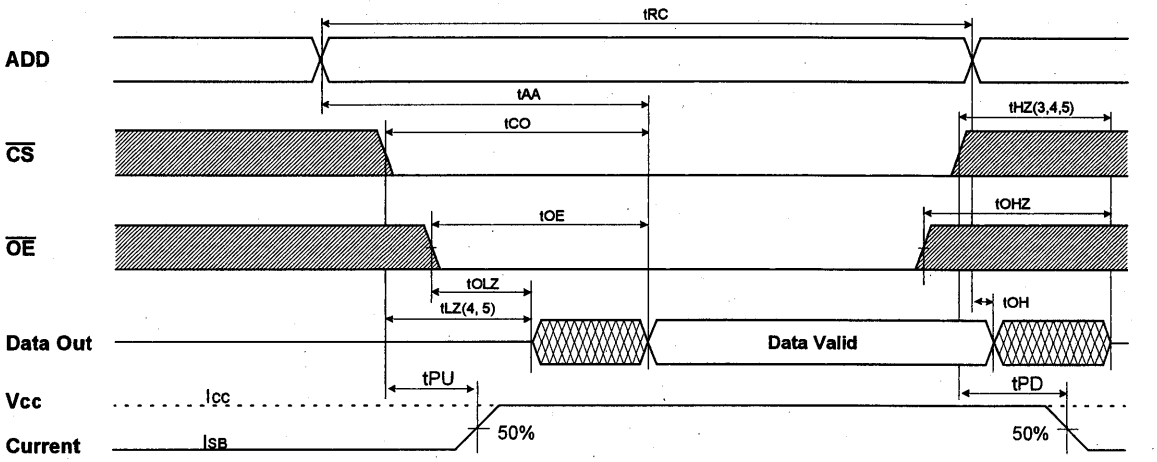
2

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



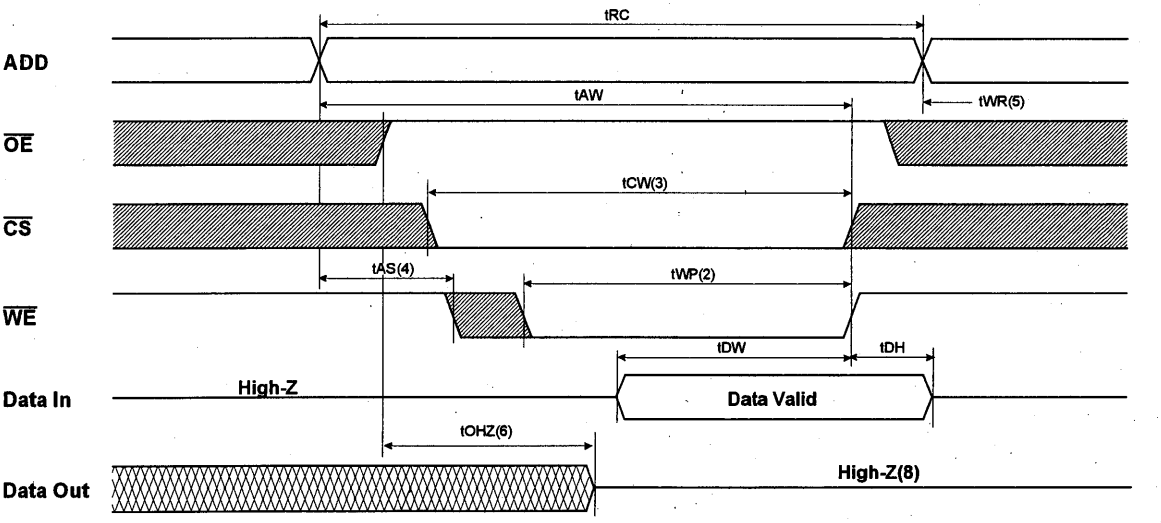
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

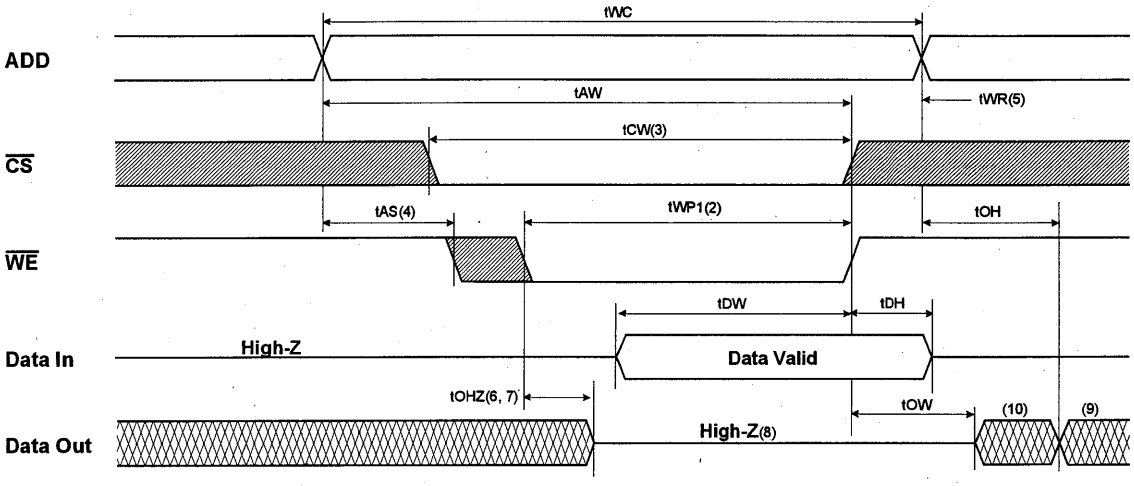
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

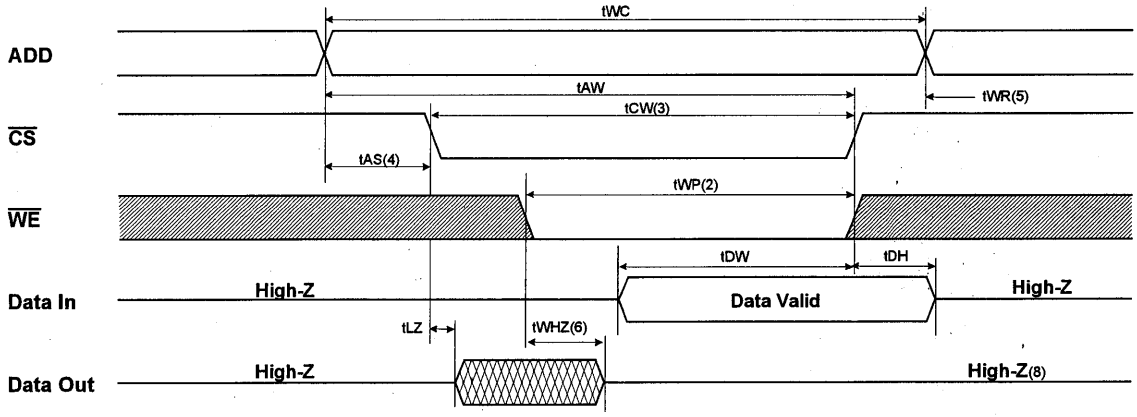


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

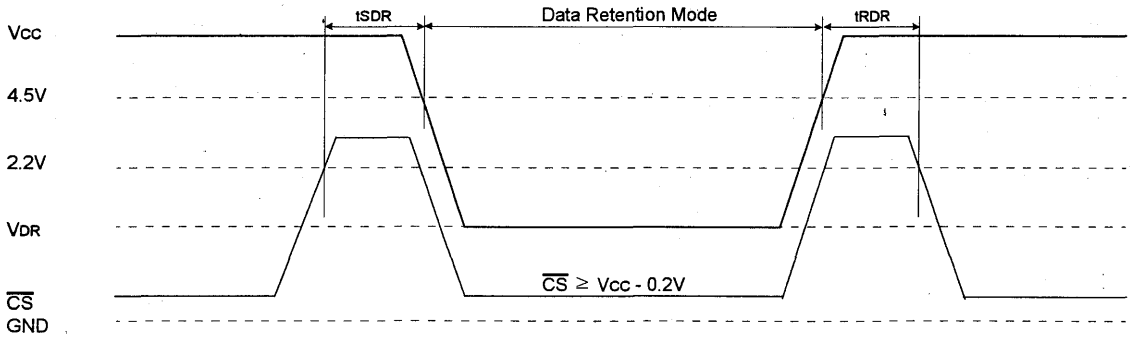
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.07	mA
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



SAMSUNG ELECTRONICS

1M High Speed SRAM
(5.0V Operation)

1M x 1 Bit High-Speed CMOS Static RAM

FEATURES

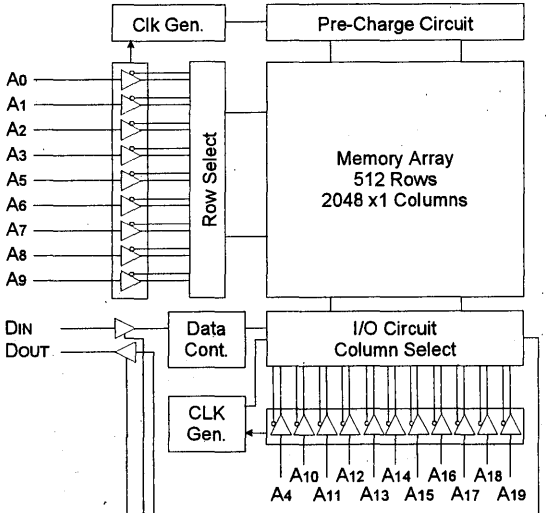
- Fast Access Time 20, 25, 35ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 2mA(Max.)
  - 0.5mA(Max.) ; L-ver. only
  - Operating KM611001/L - 20 : 130mA(Max.)
  - KM611001/L - 25 : 110mA(Max.)
  - KM611001/L - 35 : 100mA(Max.)
- Single 5.0V± 10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; 2V(Min.) - L-ver. only
- Standard Pin Configuration
  - KM611001/LP : 28-DIP-400
  - KM611001/LJ : 28-SOJ-400A

GENERAL DESCRIPTION

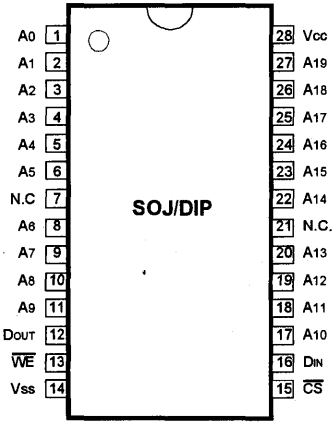
The KM611001/L is a 1,048,576-bit high-speed Static Random Access Memory organized as 1,048,576 words by 1 bit. The KM611001/L has separate input and output line for fast read and write access. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM611001/L is packaged in a 400 mil 28-pin plastic DIP or SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
WE	Write Enable
CS	Chip Select
DIN	Data Input
DOUT	Data Output
Vcc	Power(+5V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ =V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	20ns	-	130	mA
			25ns	-	110	
			35ns	-	100	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	2	mA
			L-Ver.	-	0.5	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

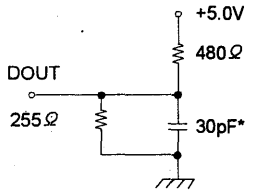
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0℃ to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

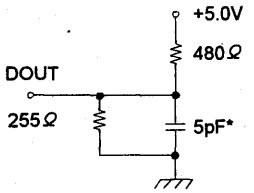
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

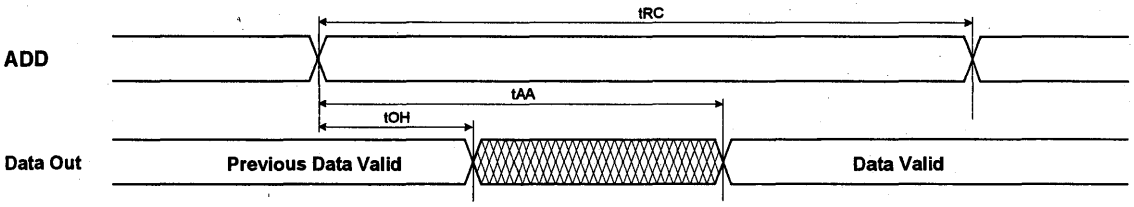
Parameter	Symbol	KM611001/L-20		KM611001/L-25		KM611001/L-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	20	-	25	-	35	-	ns
Address Access Time	tAA	-	20	-	25	-	35	ns
Chip Select to Output	tCO	-	20	-	25	-	35	ns
Chip Enable to Low-Z Output Access	tLZ	5	-	5	-	5	-	ns
Chip Disable to High-Z Output	tHZ	0	12	0	15	0	15	ns
Output Hold from Address Change	tOH	3	-	5	-	5	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	20	-	25	-	35	ns

WRITE CYCLE

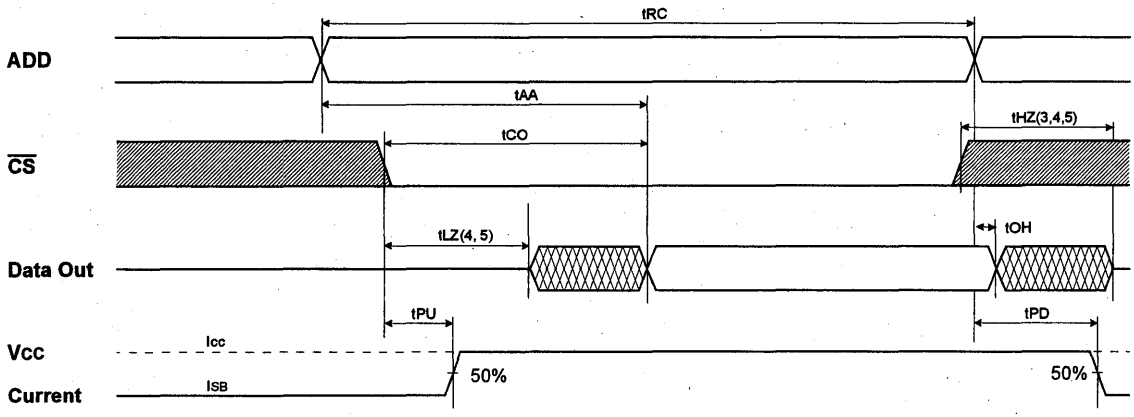
Parameter	Symbol	KM611001/L-20		KM611001/L-25		KM611001/L-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	20	-	25	-	35	-	ns
Chip Select to End of Write	tCW	17	-	20	-	30	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	17	-	20	-	30	-	ns
Write Pulse Width	tWP	15	-	20	-	25	-	ns
Write Recovery Time	tWR	2	-	3	-	3	-	ns
Write to Output High-Z	tWHZ	0	8	0	10	0	12	ns
Data to Write Time Overlap	tDW	12	-	15	-	20	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=VIL, $\overline{WE}$=VIH)



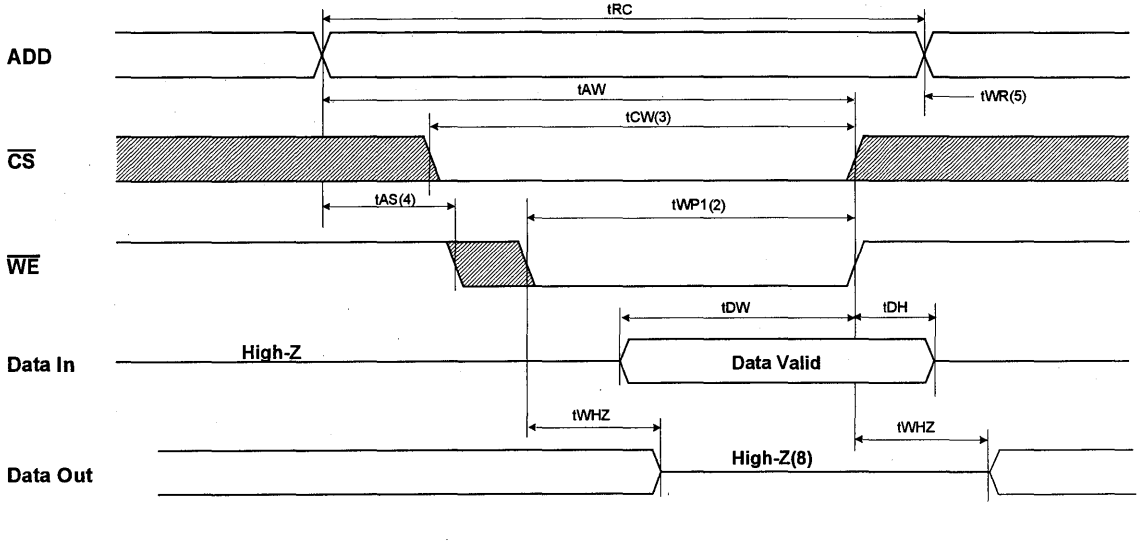
TIMING WAVE FORM OF READ CYCLE(2) (WE=VIH)



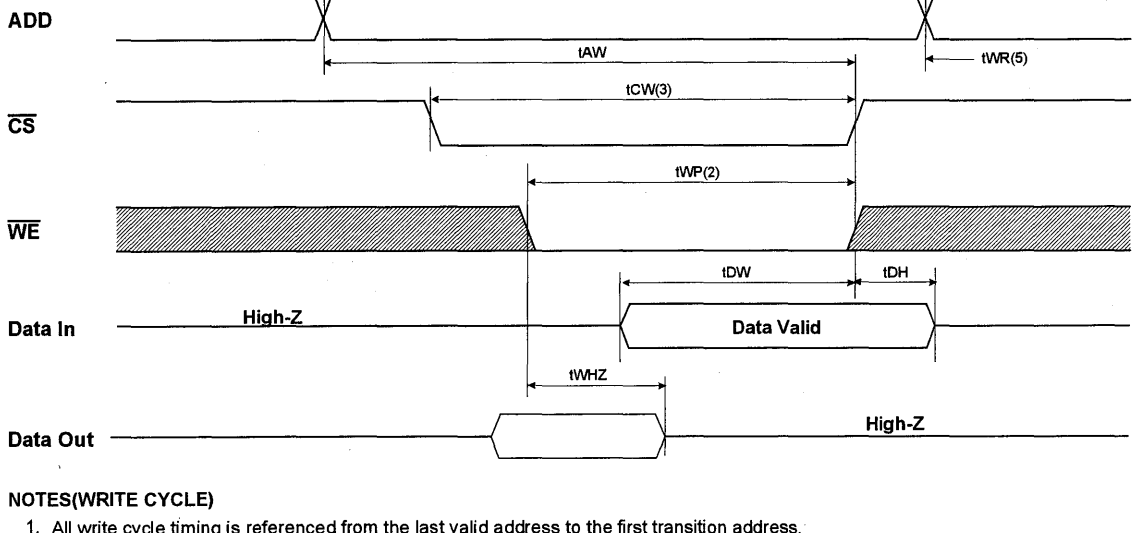
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ is defined as the time at which the output achieve the open circuit condition and is not referenced to VOH or VOL Levels. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=VIL.
6. Address valid prior to coincident with $\overline{CS}$ transition low.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{WE}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. Dout is the read data of the new address.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	Mode	I/O Pin	Supply Current
H	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	Read	D_{OUT}	I_{CC}
L	L	Write	D_{IN}	I_{CC}

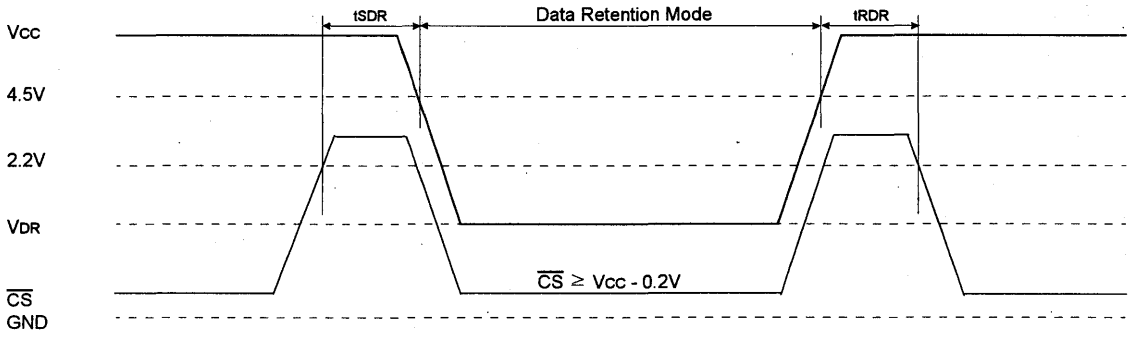
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.1	mA
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

* **NOTE** : L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



256K x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 8,10,12ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30mA(Max.)
  - (CMOS) : 10mA(Max.)
  - 1mA(Max.) - L-Ver. only
  - Operating KM641003B/BL - 8 : 150mA(Max.)
  - KM641003B/BL - 10 : 140mA(Max.)
  - KM641003B/BL - 12 : 130mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM641003B/BLJ : 32-SOJ-400
  - KM641003B/BLT: 32-TSOP2-400F

GENERAL DESCRIPTION

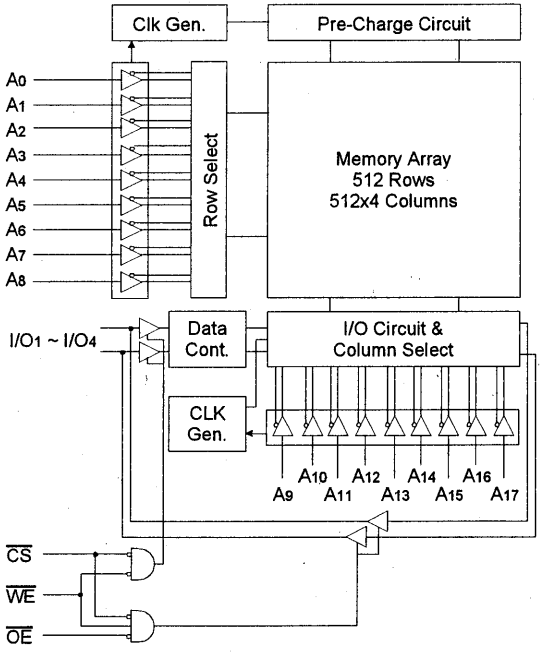
The KM641003B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641003B/BL uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641003B/BL is packaged in a 400 mil 32-pin plastic SOJ or TSOP2 forward.

2

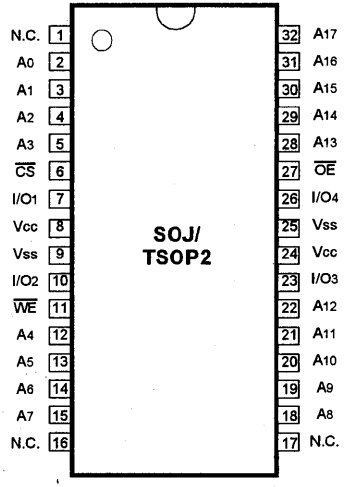
ORDERING INFORMATION

KM641003B/BL -8/10/12	Commercial Temp.
KM641003BI/BLI -8/10/12	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤6ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤6ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	8ns	-	150	mA
			10ns	-	140	
			12ns	-	130	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	30	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	10	mA
			L-Ver.	-	1	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

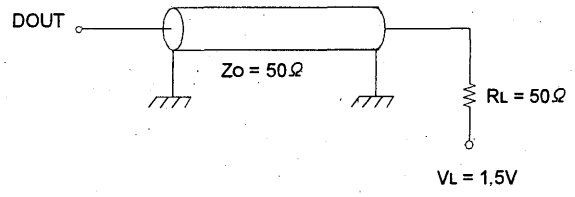
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

TEST CONDITIONS

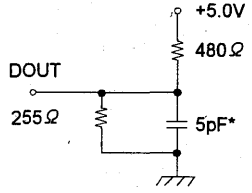
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641003B/BL-8		KM641003B/BL-10		KM641003B/BL-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	8	-	10	-	12	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

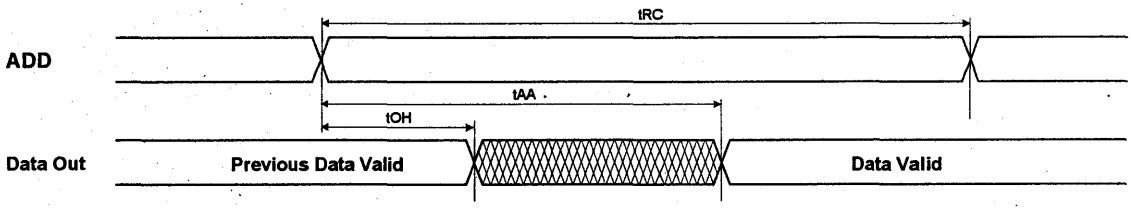
WRITE CYCLE

Parameter	Symbol	KM641003B/BL-8		KM641003B/BL-10		KM641003B/BL-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	8	-	10	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

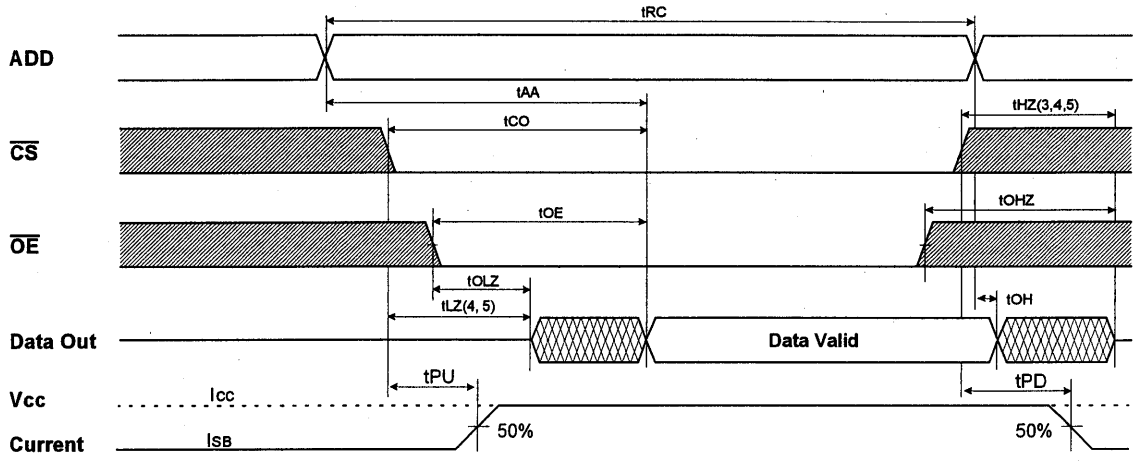
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



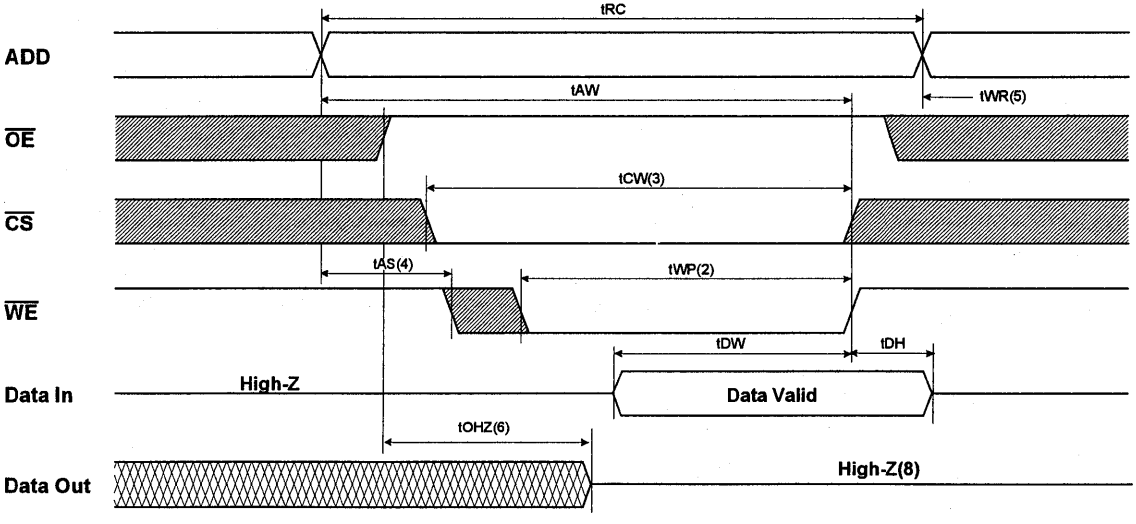
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



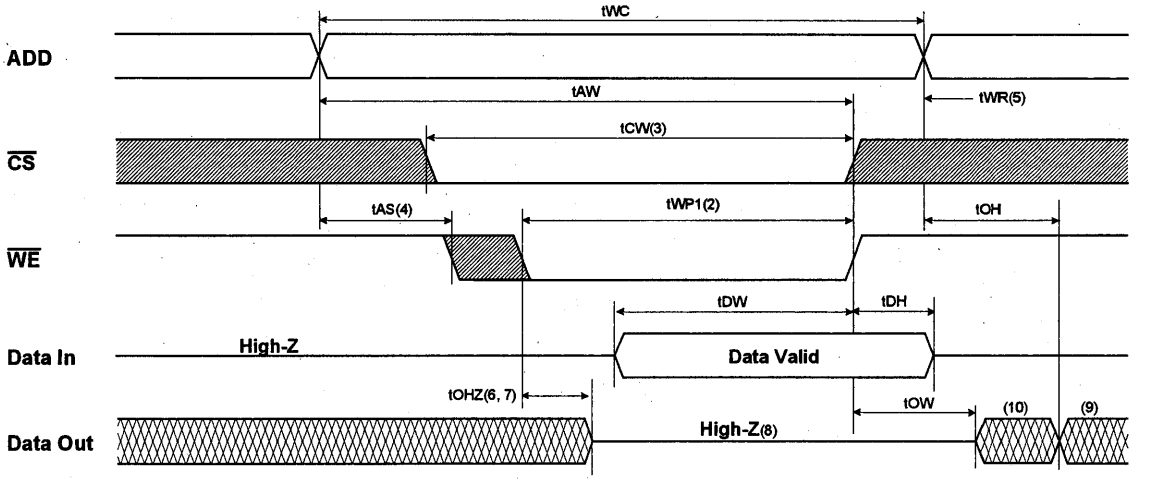
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

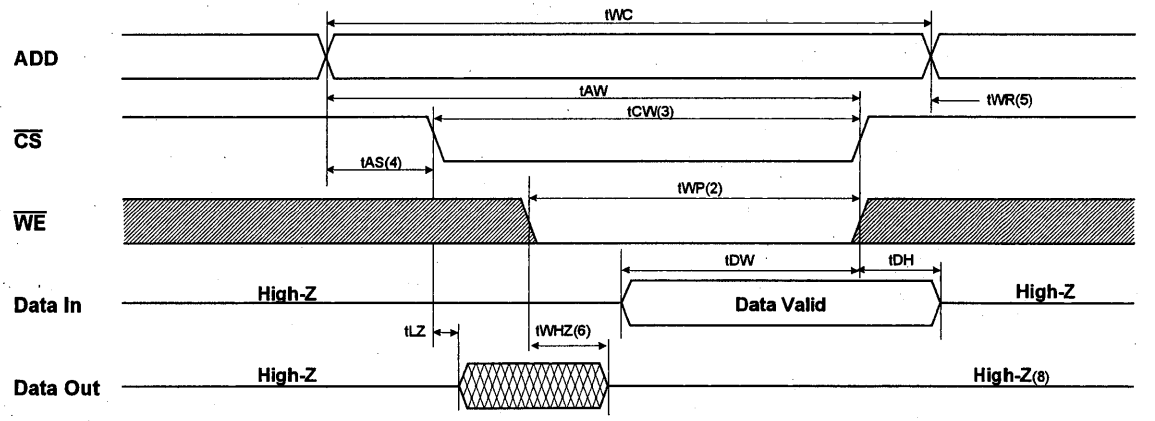
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

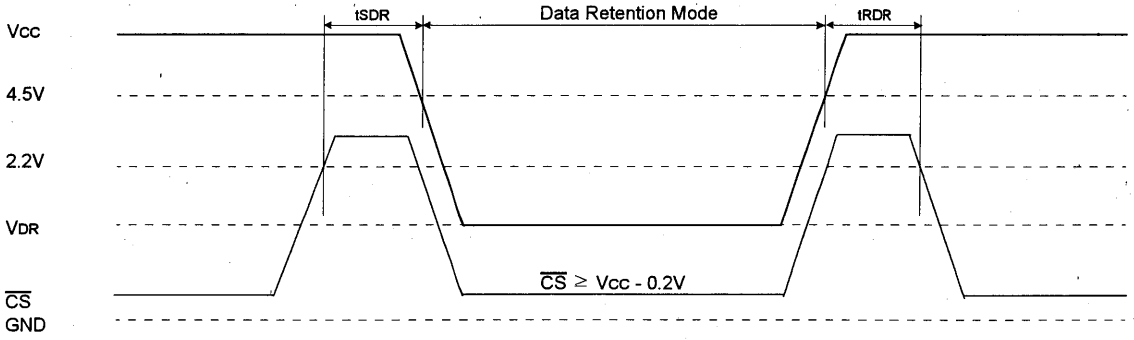
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.9	mA
		V_{CC} = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.7	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



256K x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM

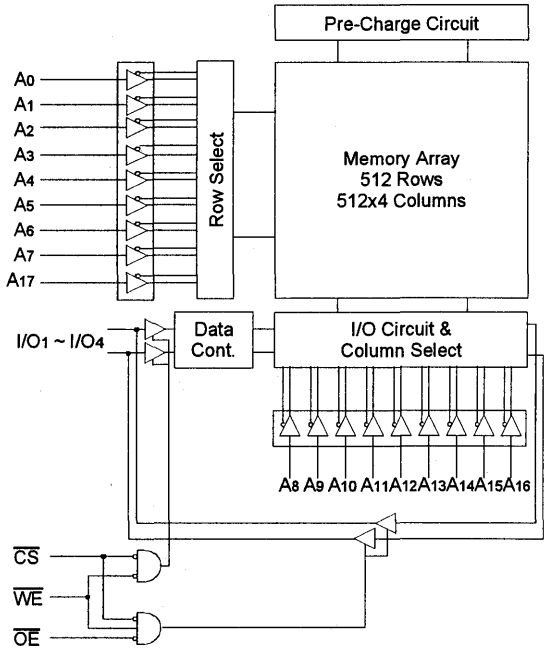
FEATURES

- Fast Access Time 8,10,12ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM64B1003 - 8 : 165mA(Max.)
  - KM64B1003 - 10 : 155mA(Max.)
  - KM64B1003 - 12 : 145mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM64B1003J : 32-SOJ-400

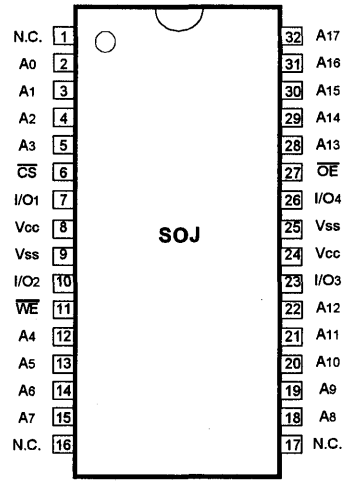
GENERAL DESCRIPTION

The KM64B1003 is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM64B1003 uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64B1003 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤6ns) for I ≤ 20㎃

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤6ns) for I ≤ 20㎃

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	㎂
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-10	10	㎂
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	8ns	-	165	㎃
			10ns	-	155	
			12ns	-	145	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	60	㎃
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	㎃
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

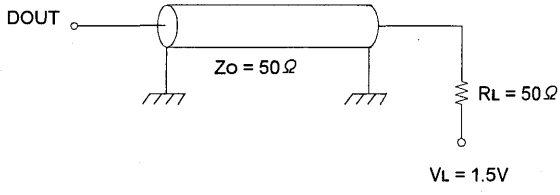
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

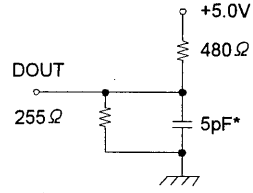
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64B1003-8		KM64B1003-10		KM64B1003-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output Access	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

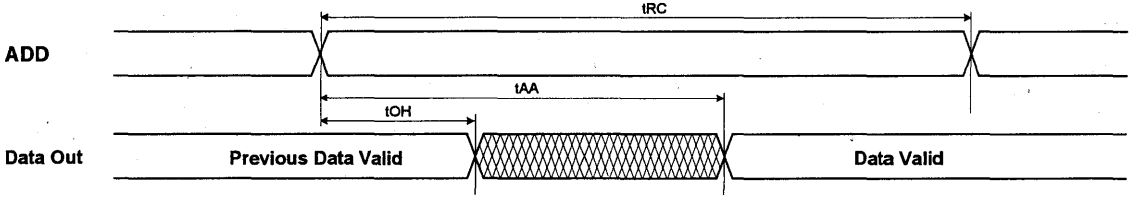
WRITE CYCLE

Parameter	Symbol	KM64B1003-8		KM64B1003-10		KM64B1003-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	8	-	9	-	10	-	ns
Write Recovery Time	tWR	1	-	1	-	1	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

2

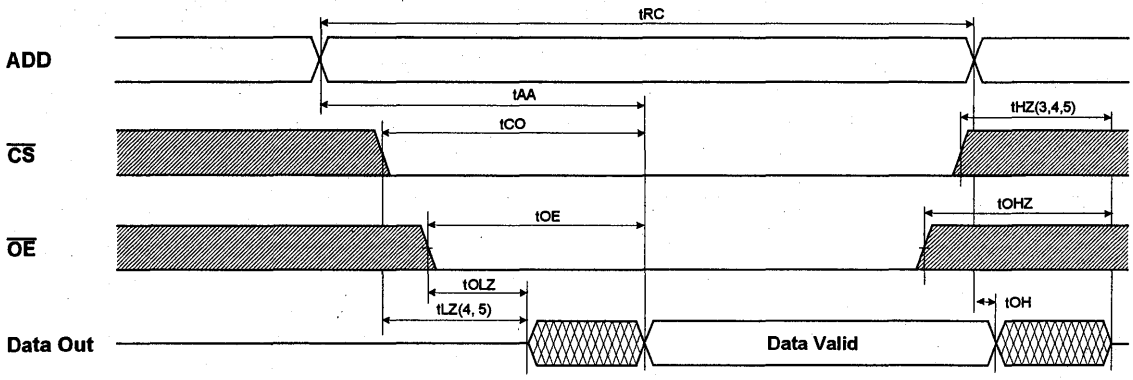
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



SAMSUNG ELECTRONICS

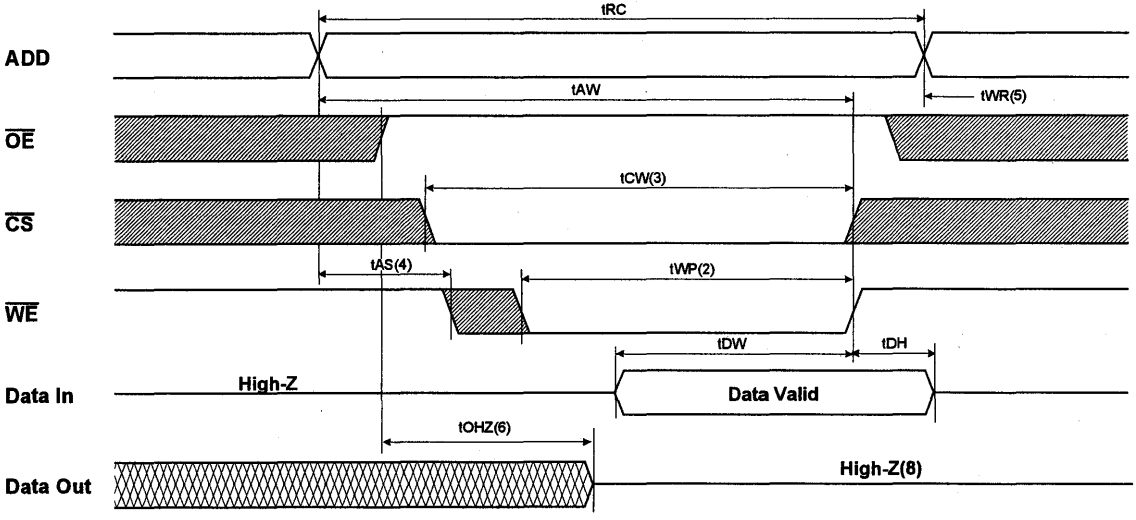
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



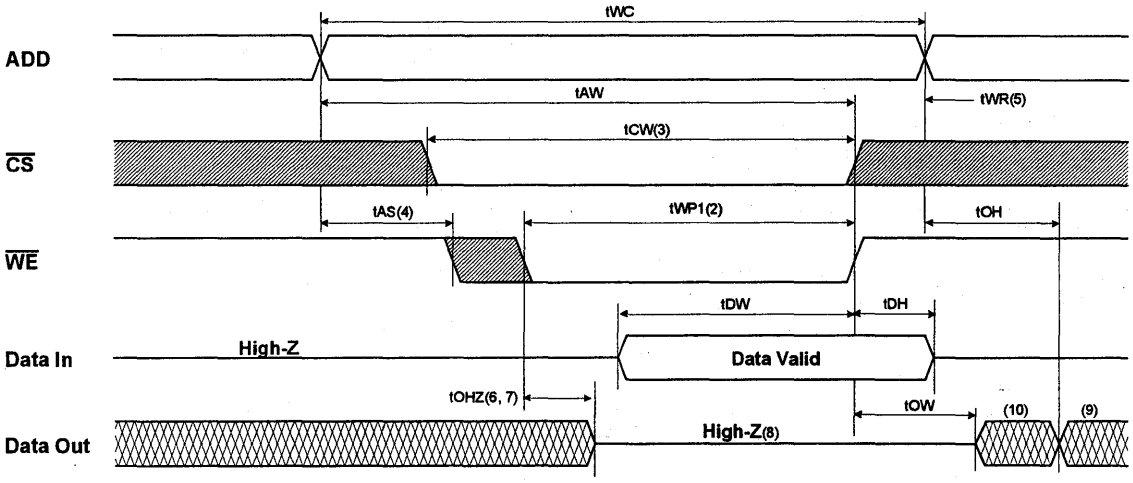
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200㎷ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

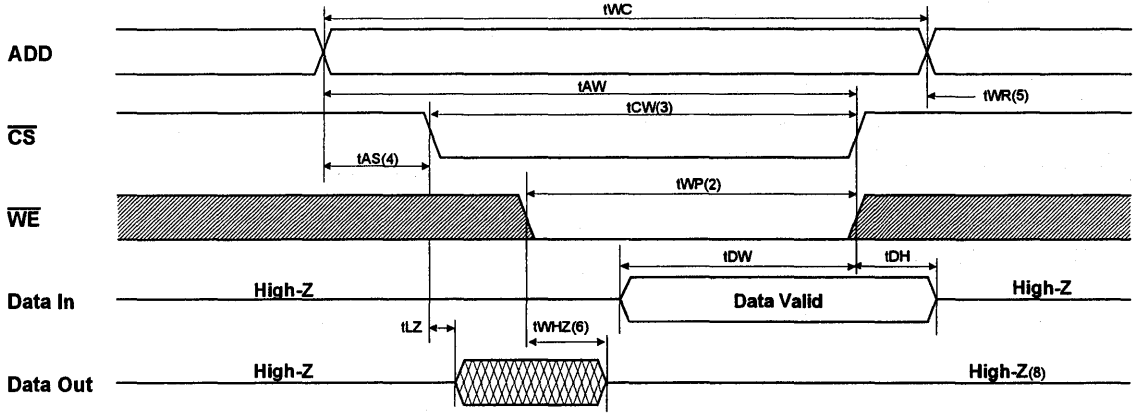
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



SAMSUNG ELECTRONICS

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

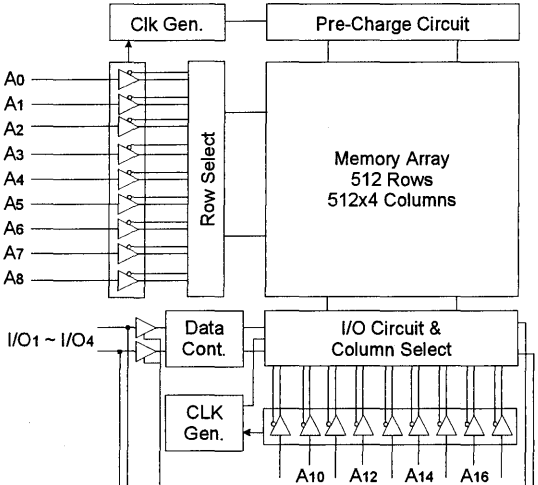
* **NOTE** : X means Don't Care.

256K x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12, 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 25mA(Max.)
  - (CMOS) : 8mA(Max.)
  - Operating KM641003A - 12 : 150mA(Max.)
  - KM641003A - 15 : 145mA(Max.)
  - KM641003A - 17 : 145mA(Max.)
  - KM641003A - 20 : 140mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM641003AJ : 32-SOJ-400
  - KM641003AT: 32-TSOP2-400F

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

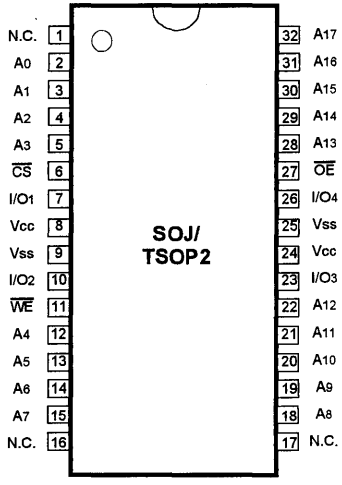
The KM641003A is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641003A uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641003A is packaged in a 400 mil 32-pin plastic SOJ or TSOP2 forward.

2

ORDERING INFORMATION

KM641003A -12/15/17/20	Commercial Temp.
KM641003AI -12/15/17/20	Industrial Temp.

PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	150	mA
			15ns	-	145	
			17ns	-	145	
			20ns	-	140	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	25	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	8	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* Vcc=5.0V ± 5% Temp = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

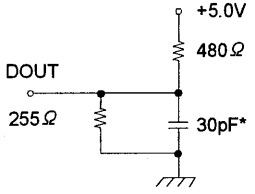
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

TEST CONDITIONS

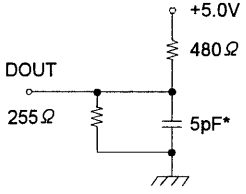
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641003A-12		KM641003A-15		KM641003A-17		KM641003A-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	17	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	12	-	15	-	17	-	20	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

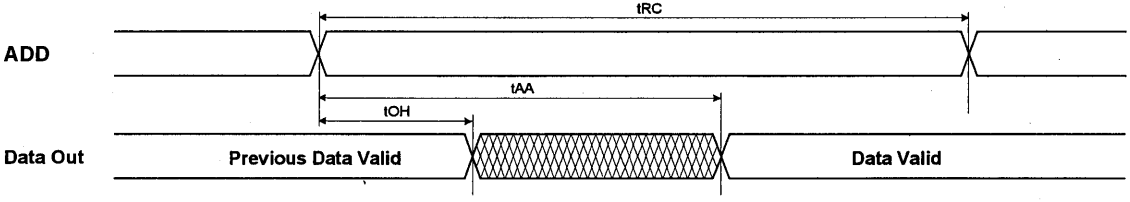
WRITE CYCLE

Parameter	Symbol	KM641003A-12		KM641003A-15		KM641003A-17		KM641003A-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	12	-	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

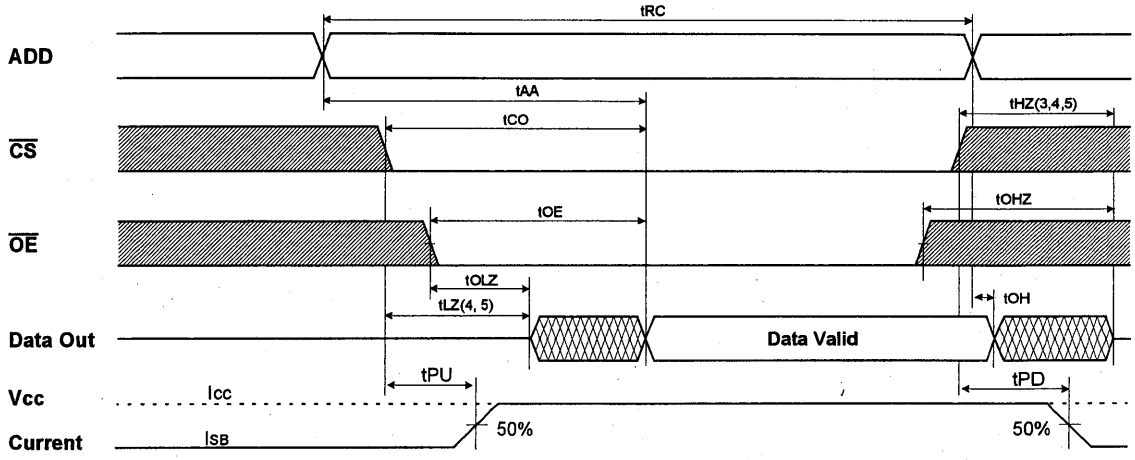
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



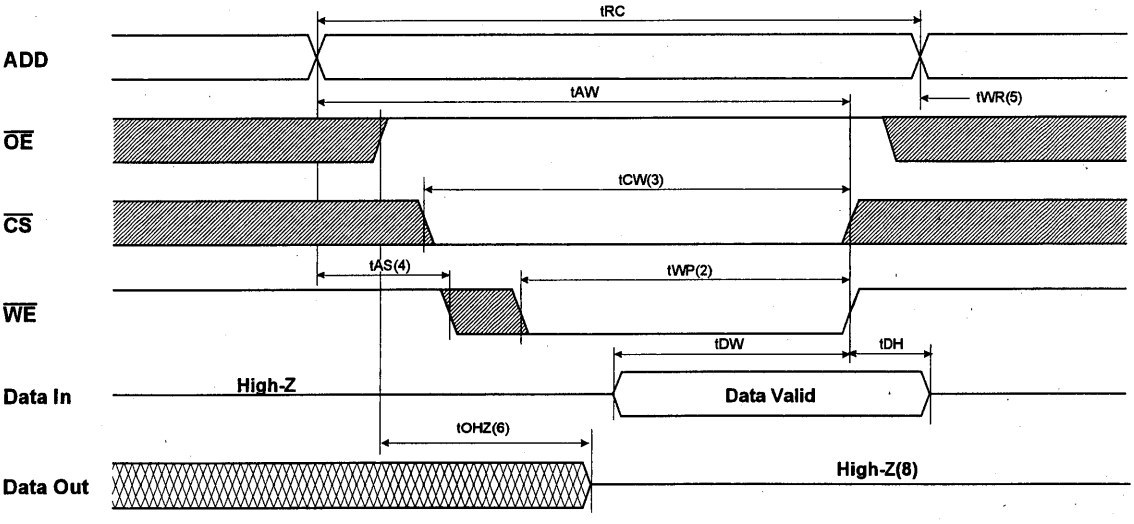
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

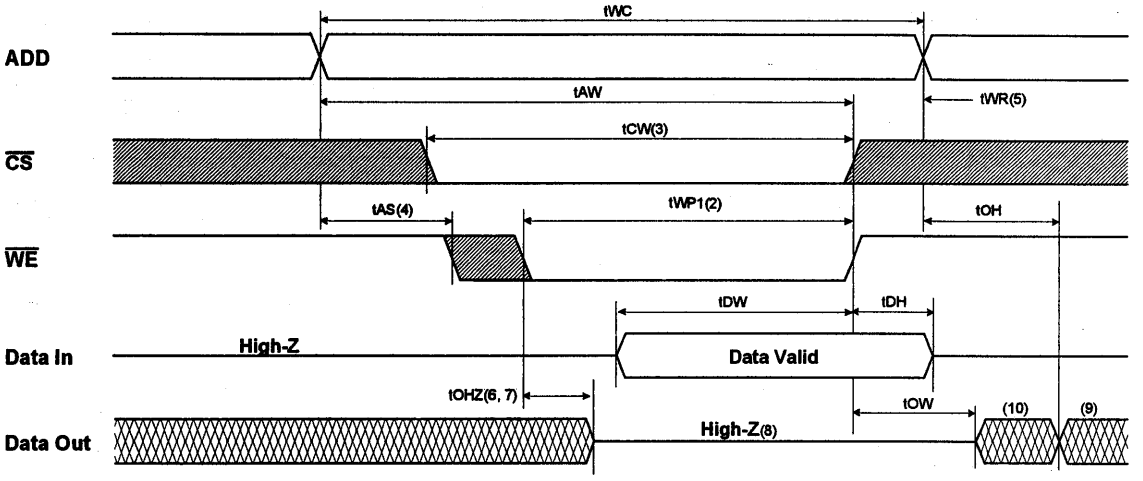
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

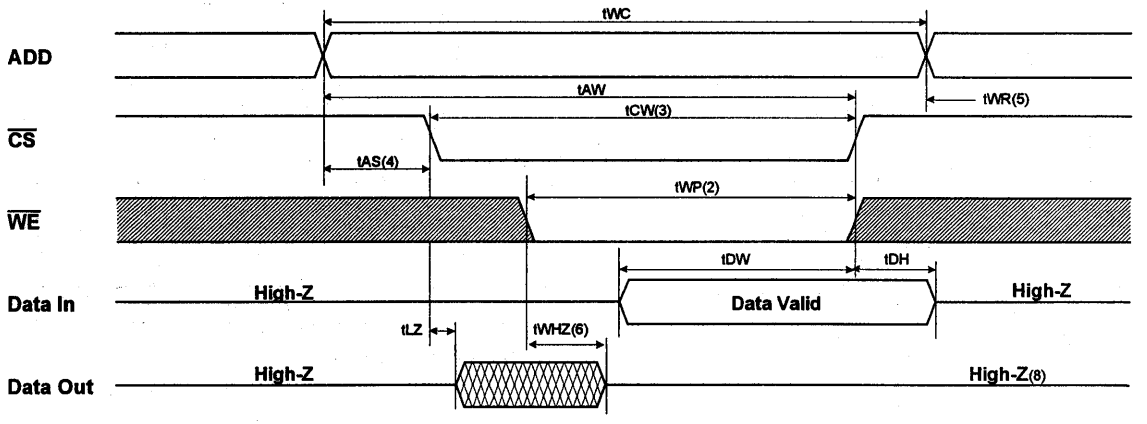


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

256K x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM

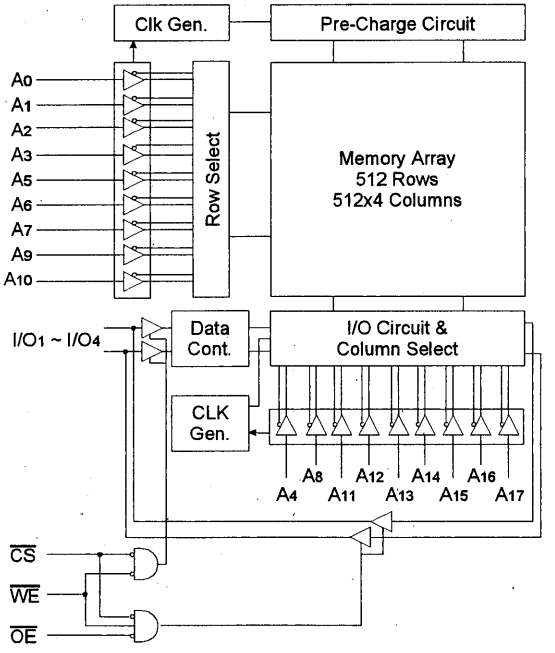
FEATURES

- Fast Access Time 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM641003 - 15 : 170mA(Max.)
  - KM641003 - 17 : 160mA(Max.)
  - KM641003 - 20 : 150mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM641003J : 32-SOJ-400

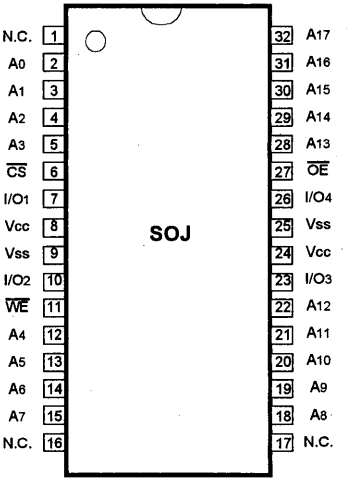
GENERAL DESCRIPTION

The KM641003 is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641003 uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641003 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	170	mA
			17ns	-	160	
			20ns	-	155	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

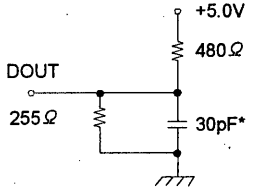
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

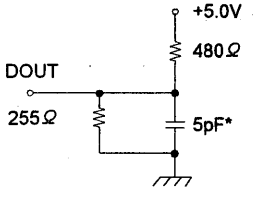
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641003-15		KM641003-17		KM641003-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9	-	10	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	5	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

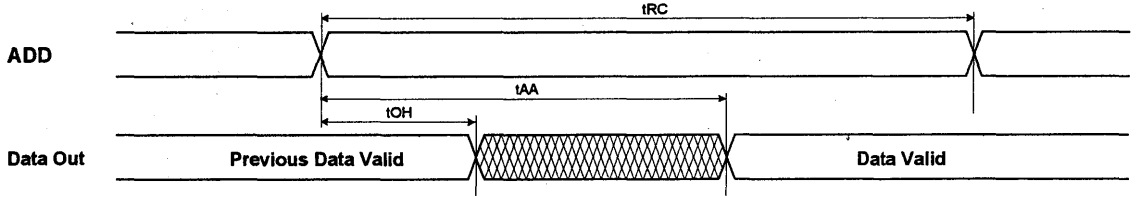
WRITE CYCLE

Parameter	Symbol	KM641003-15		KM641003-17		KM641003-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	12	-	13	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	9	-	10	-	11	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

2

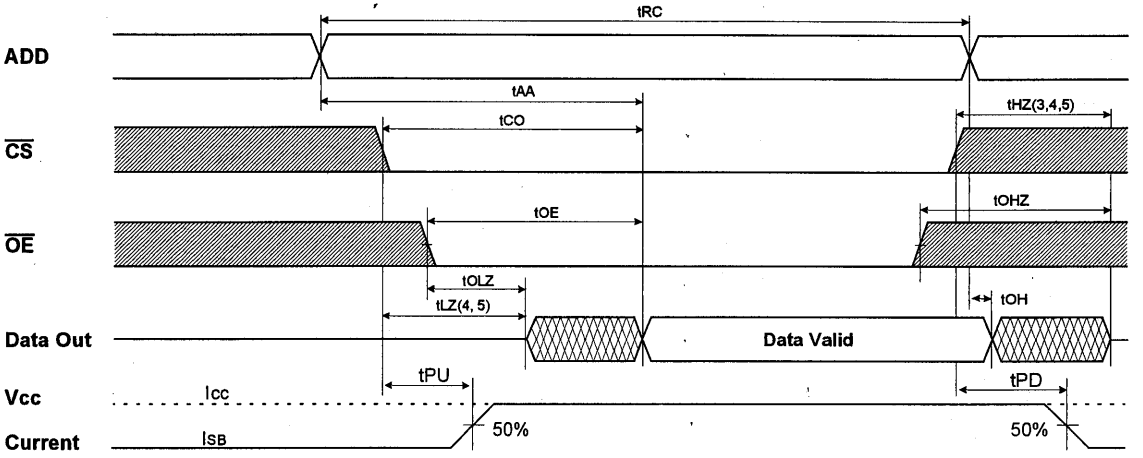
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



SAMSUNG ELECTRONICS

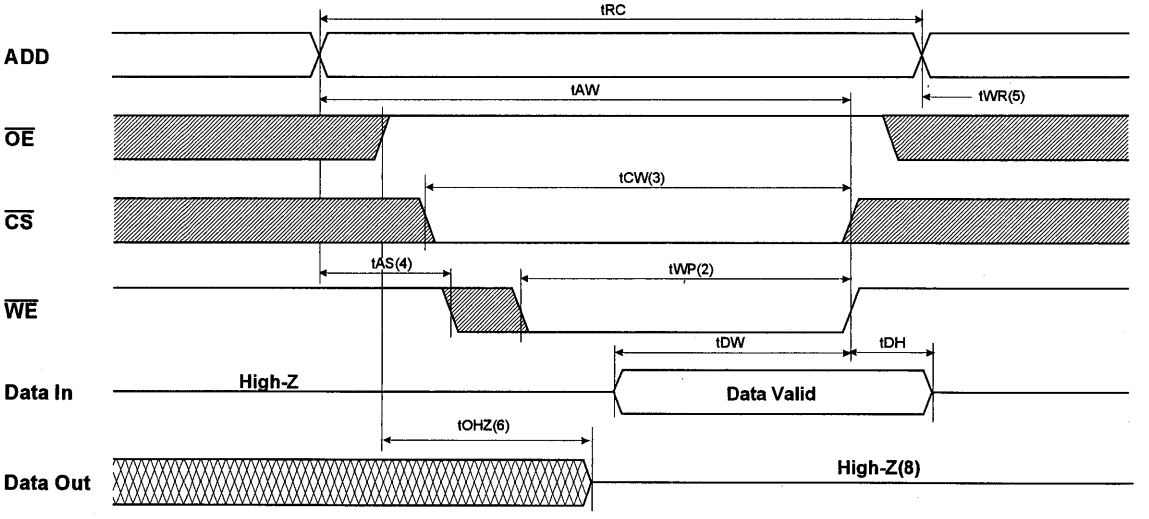
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



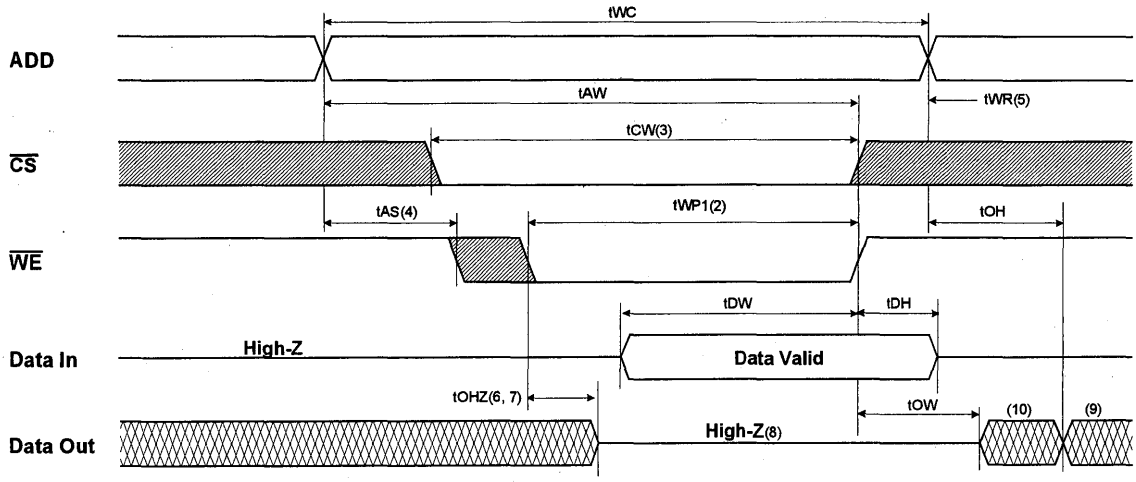
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

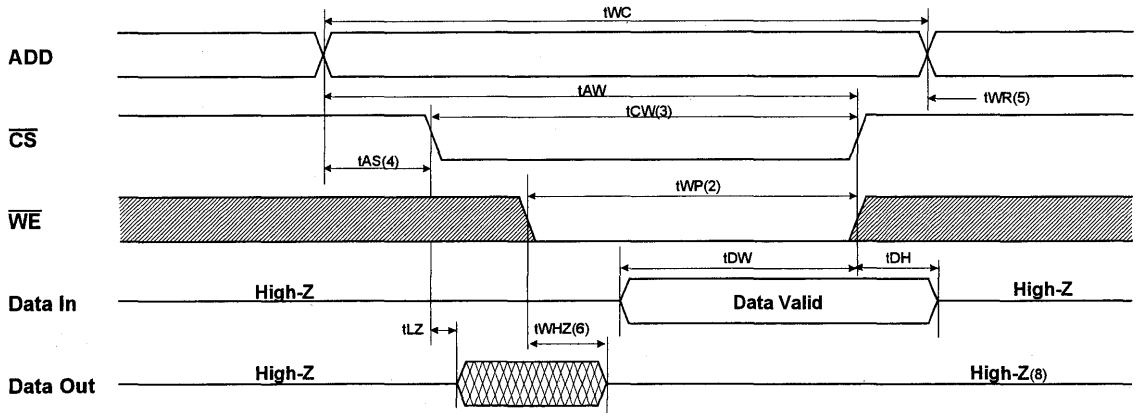
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



SAMSUNG ELECTRONICS

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

256K x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 20mA(Max.)
  - (CMOS) : 5mA(Max.)
  - 0.5mA(Max.) - L-Ver. only
  - Operating KM641001B/BL - 15 : 120mA(Max.)
  - KM641001B/BL - 17 : 110mA(Max.)
  - KM641001B/BL - 20 : 100mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Standard Pin Configuration
  - KM641001B/BLJ : 28-SOJ-400A

GENERAL DESCRIPTION

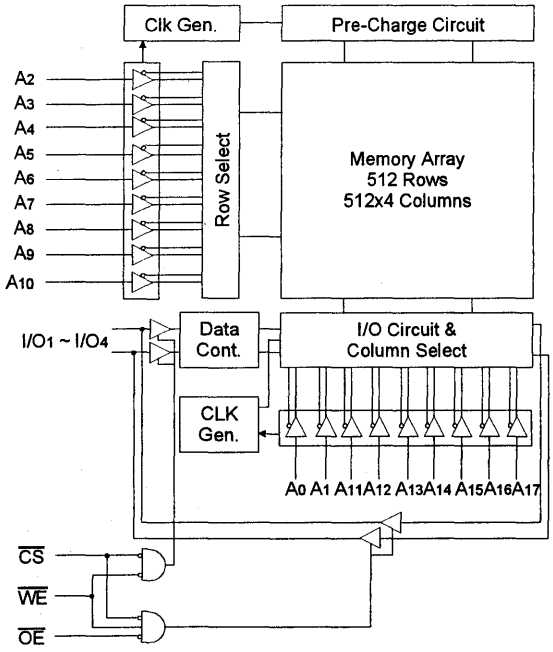
The KM641001B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641001B/BL uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641001B/BL is packaged in a 400 mil 28-pin plastic SOJ.

2

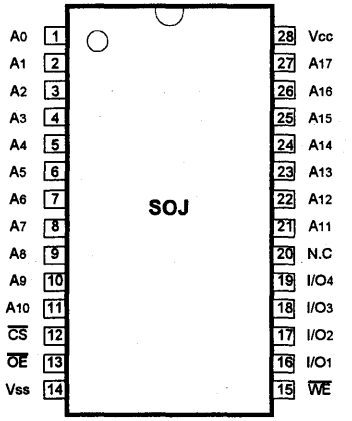
ORDERING INFORMATION

KM641001B/BL -15/17/20	Commercial Temp.
KM641001BI/BLI -15/17/20	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤ 10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	120	mA
			17ns	-	110	
			20ns	-	100	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	20	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	5	mA
			L-Ver.	-	0.5	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

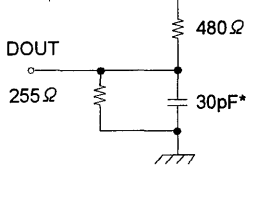
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

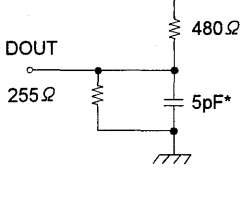
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641001B/BL-15		KM641001B/BL-17		KM641001B/BL-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9	-	10	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

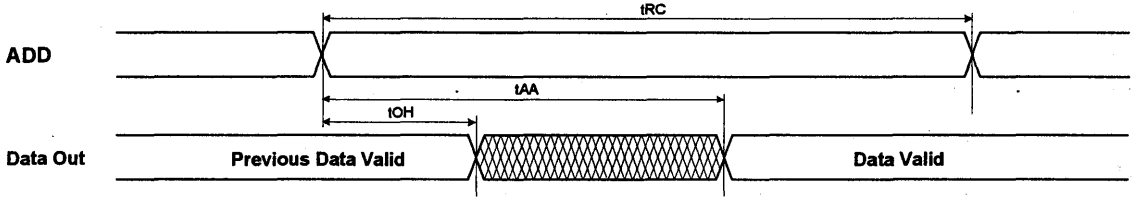
WRITE CYCLE

Parameter	Symbol	KM641001B/BL-15		KM641001B/BL-17		KM641001B/BL-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	.0	8	0	9	0	10	ns
Data to Write Time Overlap	tDW	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

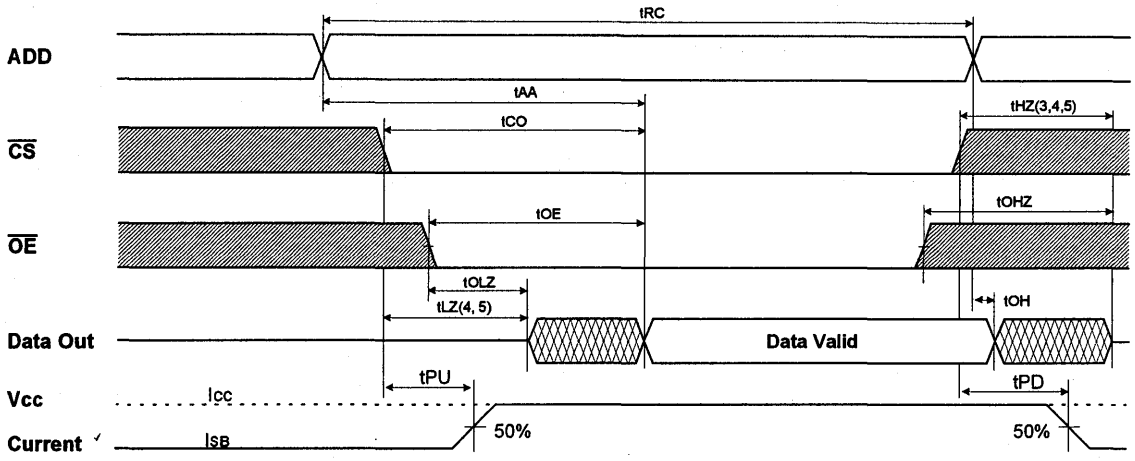
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



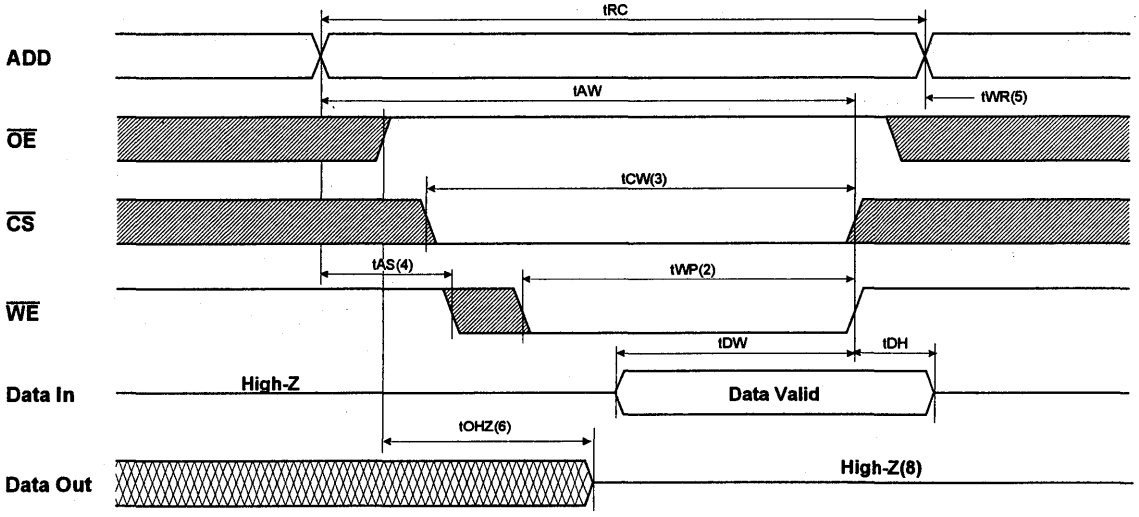
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



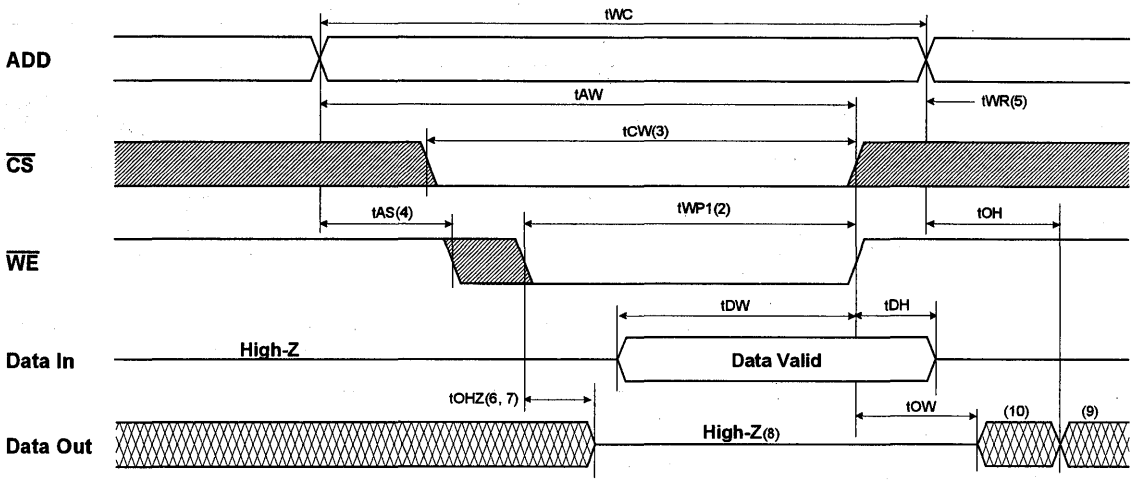
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

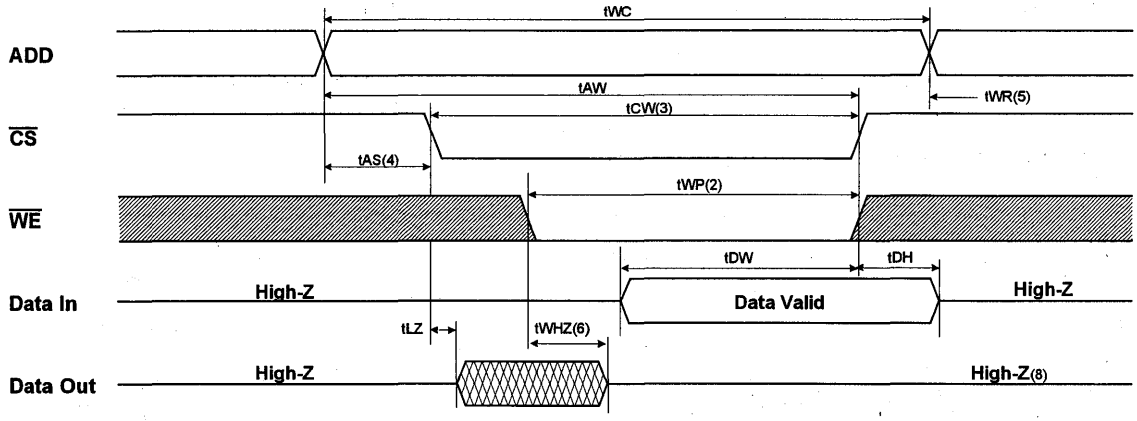
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

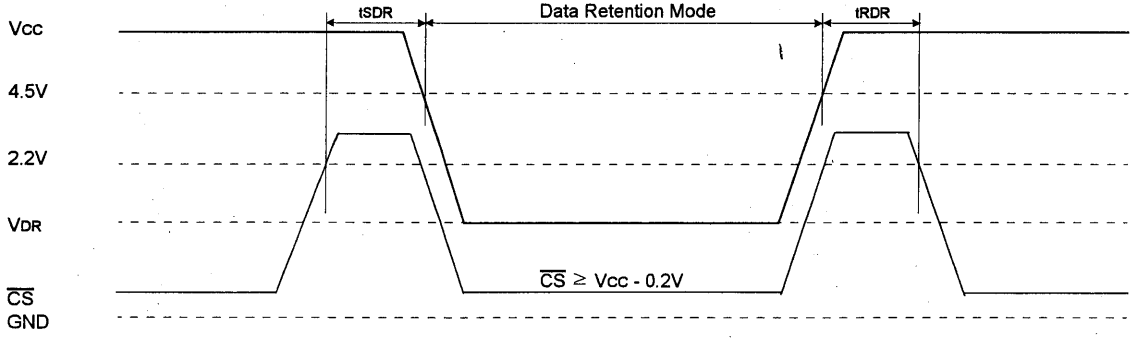
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	5.5	V
Data Retention Current	I_{DR}	Vcc = 3.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.40	mA
		Vcc = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.35	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



256K x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM

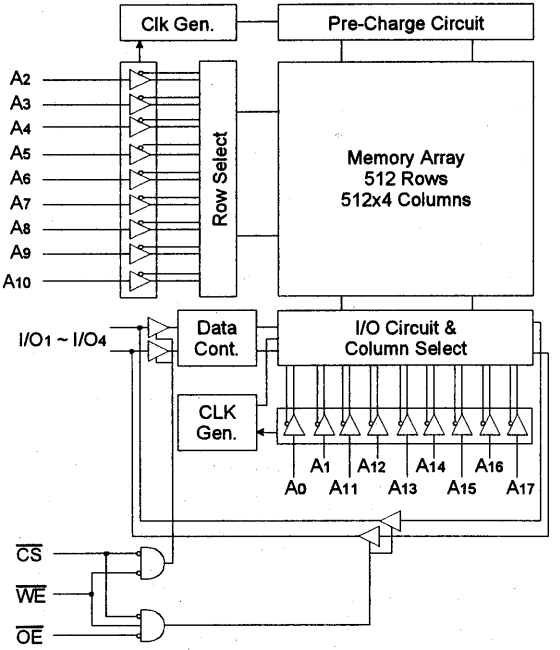
FEATURES

- Fast Access Time 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 25mA(Max.)
  - (CMOS) : 8mA(Max.)
  - Operating KM641001A - 15 : 125mA(Max.)
  - KM641001A - 17 : 125mA(Max.)
  - KM641001A - 20 : 120mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM641001AJ : 28-SOJ-400A

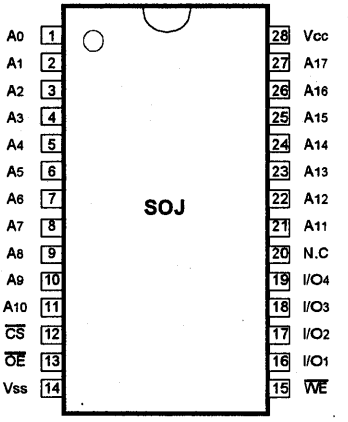
GENERAL DESCRIPTION

The KM641001A is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641001A uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641001A is packaged in a 400 mil 28-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20㎃

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20㎃

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	㎂
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	㎂
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	125	㎃
			17ns	-	125	
			20ns	-	120	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	25	㎃
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	8	㎃
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

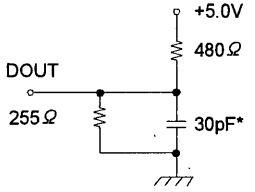
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

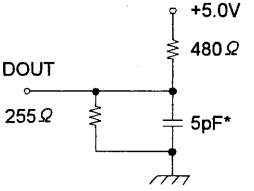
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM641001A-15		KM641001A-17		KM641001A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9	-	10	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

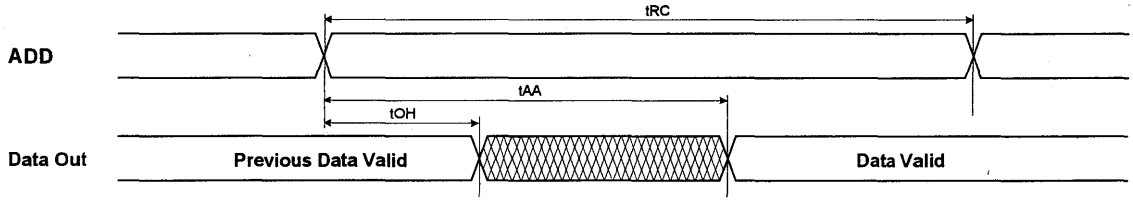
WRITE CYCLE

Parameter	Symbol	KM641001A-15		KM641001A-17		KM641001A-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	9	0	10	ns
Data to Write Time Overlap	tDW	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

2

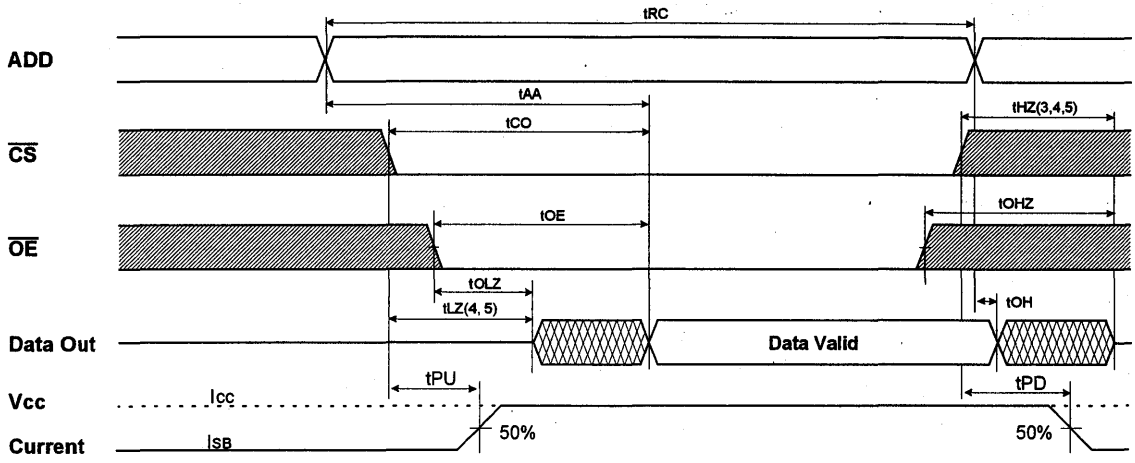
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



SAMSUNG ELECTRONICS

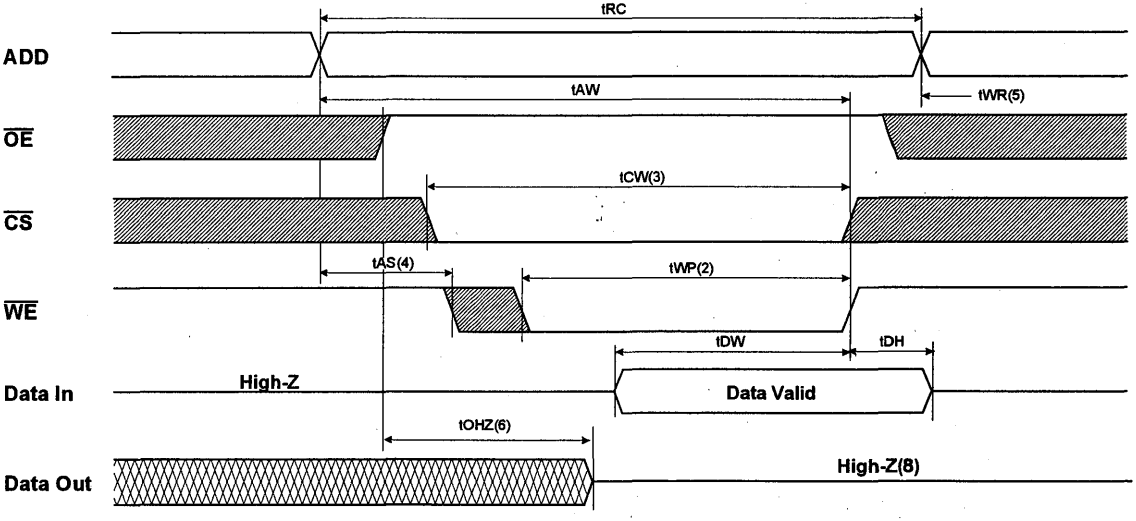
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



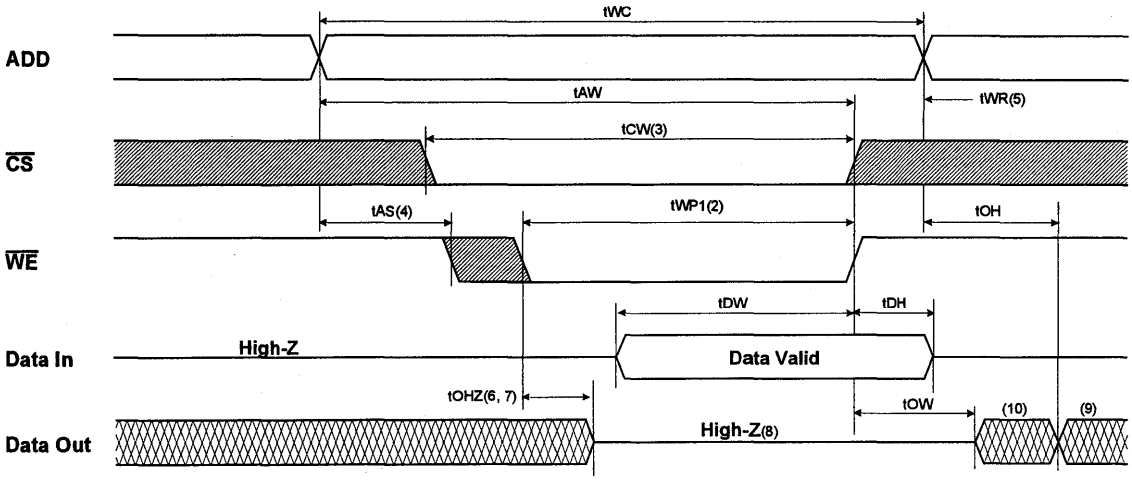
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

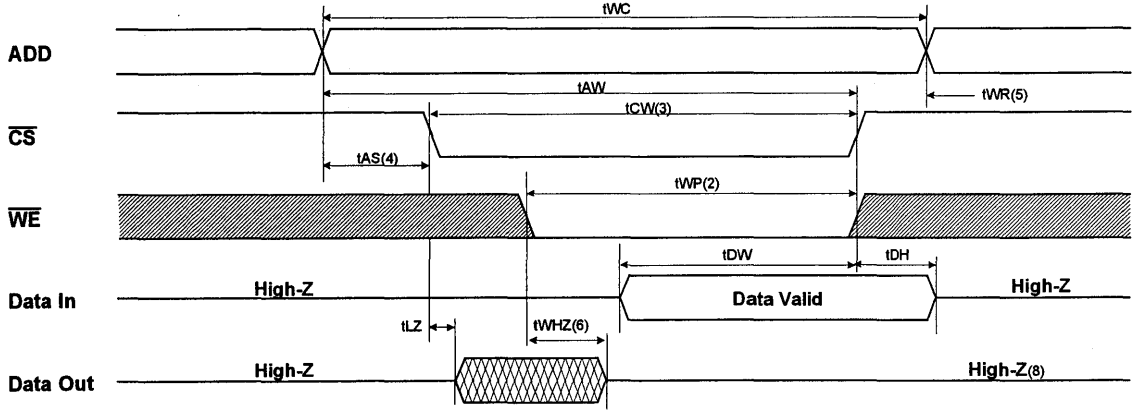
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



SAMSUNG ELECTRONICS

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

256K x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM

FEATURES

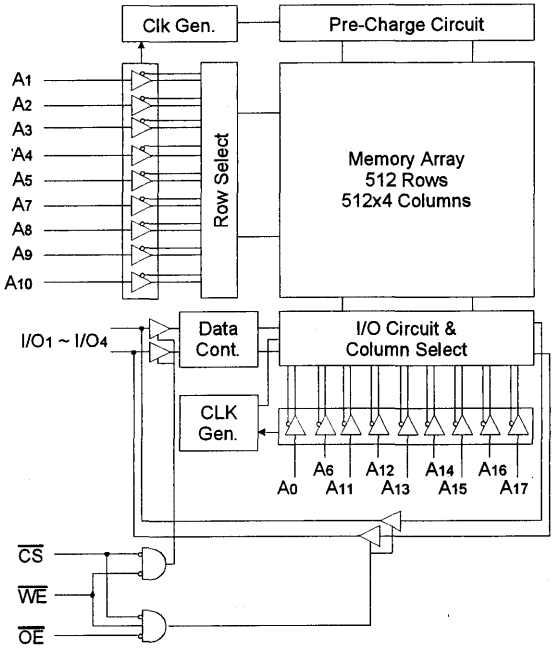
- Fast Access Time 20,25,35ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 2mA(Max.)
  - 0.5mA(Max.) - L-Ver. only
  - Operating KM641001/L - 20 : 150mA(Max.)
  - KM641001/L - 25 : 130mA(Max.)
  - KM641001/L - 35 : 110mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; 2V(Min.) - L-ver. only
- Standard Pin Configuration
  - KM641001/LP : 28-DIP-400
  - KM641001/LJ : 28-SOJ-400B

GENERAL DESCRIPTION

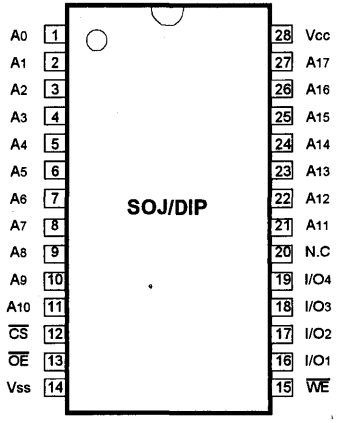
The KM641001/L is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641001/L uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641001/L is packaged in a 400 mil 28-pin plastic DIP or SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤ 10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ =V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	20ns	-	150	mA
			25ns	-	130	
			35ns	-	110	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	2	mA
			L-Ver.	-	0.5	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

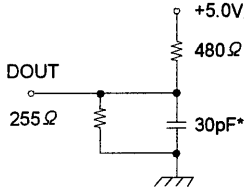
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(TA = 0 to 70℃, Vcc = 5.0V ± 10%, unless otherwise noted.)

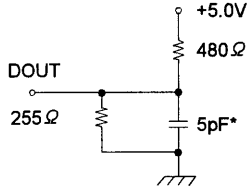
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

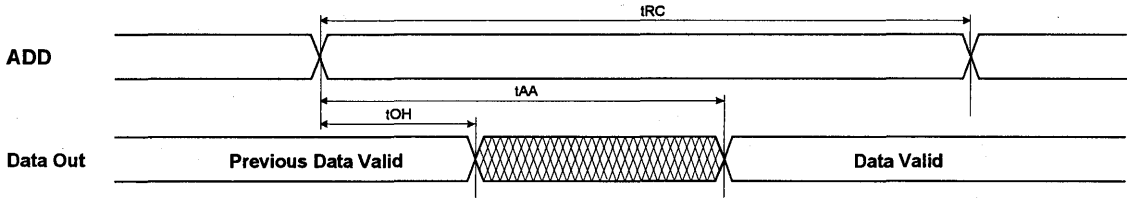
Parameter	Symbol	KM641001/L-20		KM641001/L-25		KM641001/L-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	20	-	25	-	35	-	ns
Address Access Time	tAA	-	20	-	25	-	35	ns
Chip Select to Output	tCO	-	20	-	25	-	35	ns
Output Enable to Valid Output	tOE	-	10	-	13	-	15	ns
Chip Enable to Low-Z Output	tLZ	0	-	0	-	0	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	12	0	15	0	15	ns
Output Disable to High-Z Output	tOHZ	0	8	0	10	0	15	ns
Output Hold from Address Change	tOH	3	-	5	-	5	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	20	-	25	-	35	ns

WRITE CYCLE

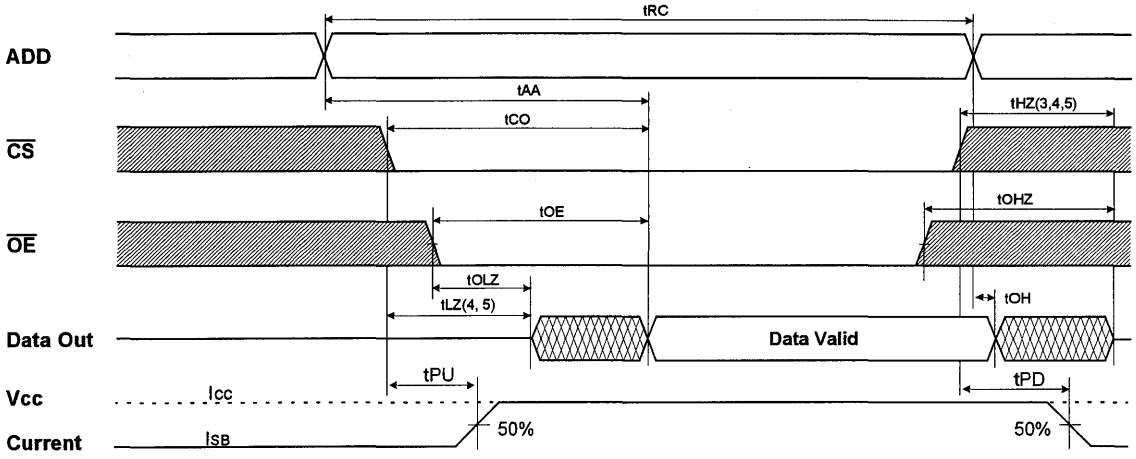
Parameter	Symbol	KM641001/L-20		KM641001/L-25		KM641001/L-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	20	-	25	-	35	-	ns
Chip Select to End of Write	tCW	17	-	20	-	30	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	17	-	20	-	30	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	15	-	20	-	25	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	20	-	25	-	35	-	ns
Write Recovery Time	tWR	2	-	3	-	3	-	ns
Write to Output High-Z	tWHZ	0	8	0	10	0	12	ns
Data to Write Time Overlap	tDW	12	-	15	-	20	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



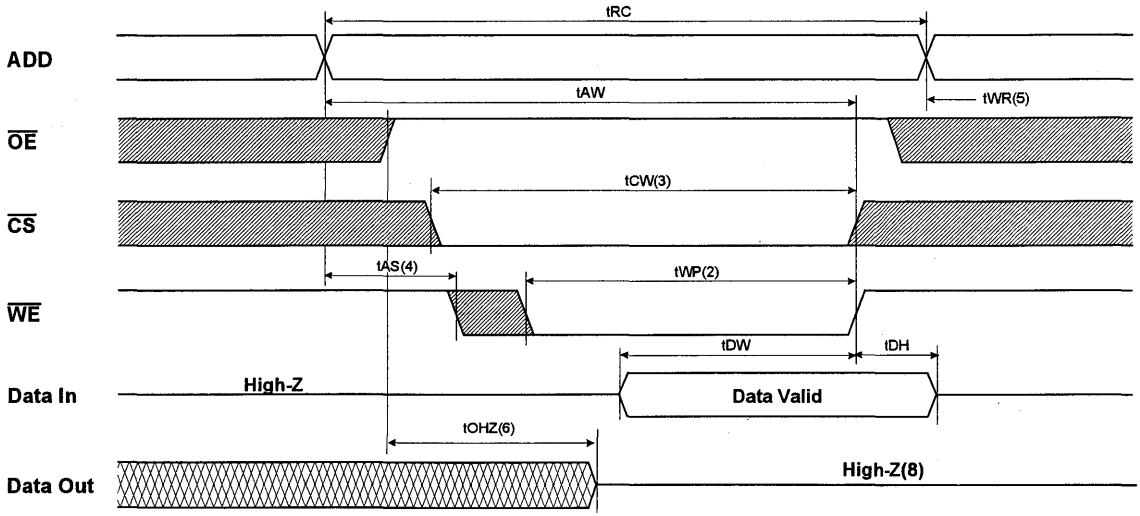
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



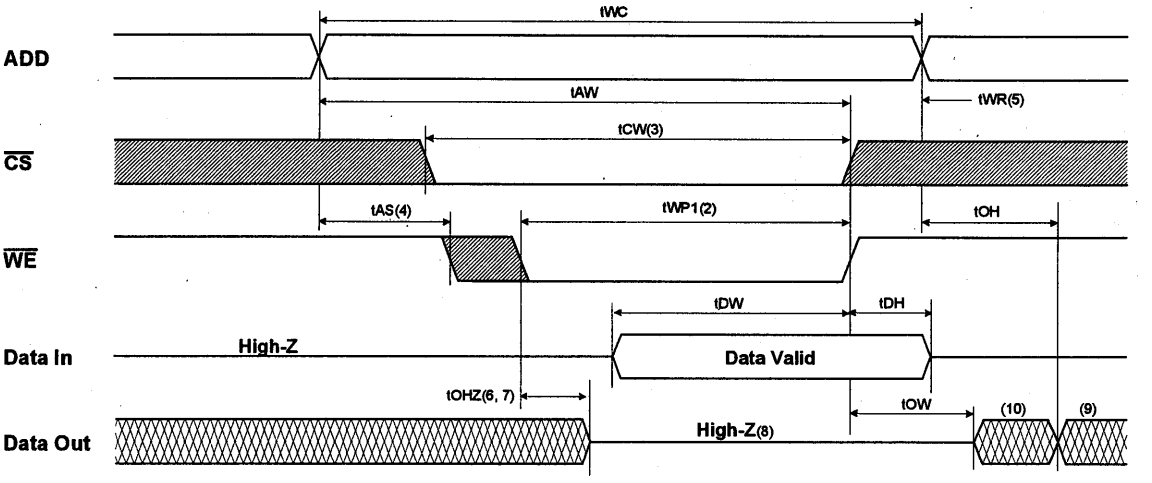
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

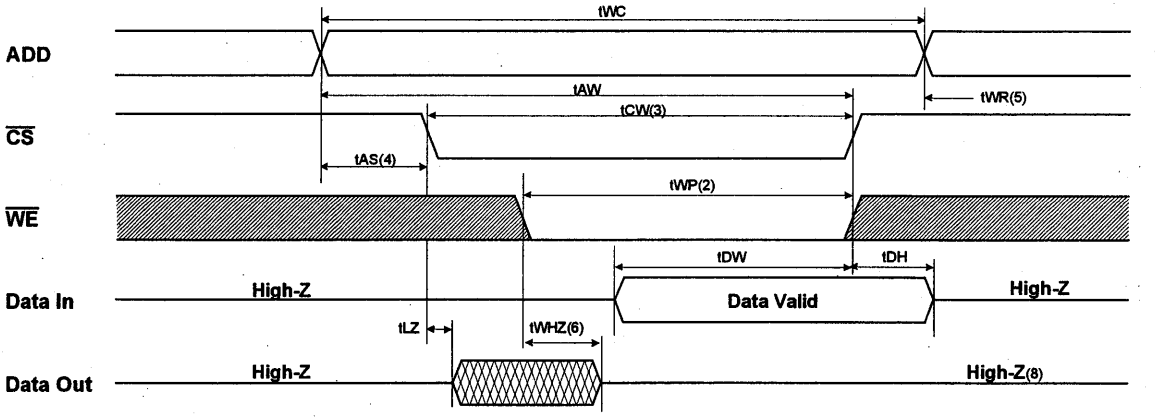
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

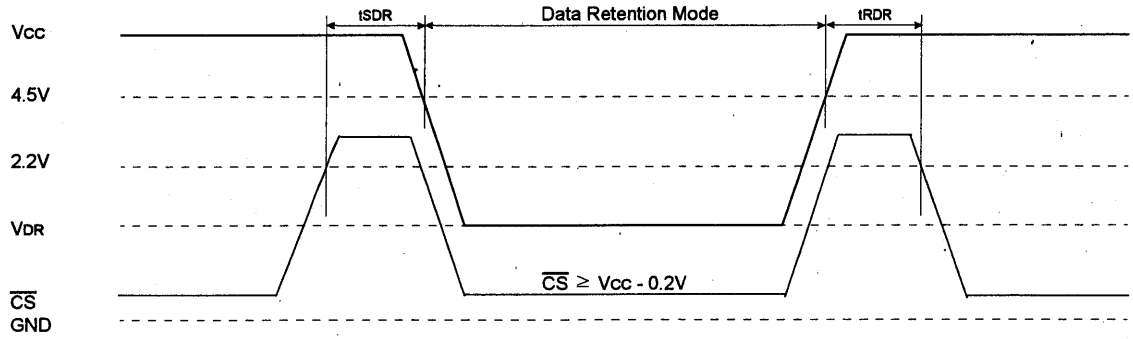
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	5.5	V
Data Retention Current	I_{DR}	Vcc = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.1	mA
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

* **NOTE** : L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



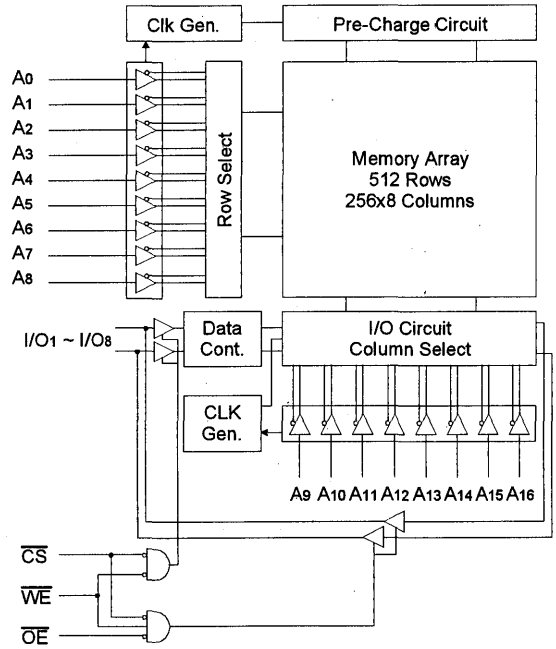
SAMSUNG ELECTRONICS

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 8,10,12ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30mA(Max.)
  - (CMOS) : 10mA(Max.)
  - 1mA(Max.) - L-Ver. only
  - Operating KM681002B/BL - 8 : 160mA(Max.)
  - KM681002B/BL - 10 : 150mA(Max.)
  - KM681002B/BL - 12 : 140mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM681002B/BLJ : 32-SOJ-400
  - KM681002B/BLSJ : 32-SOJ-300
  - KM681002B/BLT: 32-TSOP2-400F

FUNCTIONAL BLOCK DIAGRAM



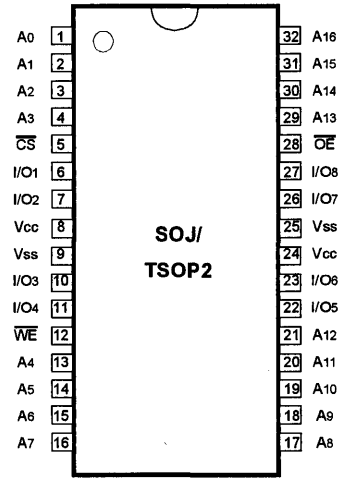
GENERAL DESCRIPTION

The KM681002B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681002B/BL uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681002B/BL is packaged in a 400/300 mil 32-pin plastic SOJ or TSOP2 forward.

ORDERING INFORMATION

KM681002B/BL -8/10/12	Commercial Temp.
KM681002BI/BLI -8/10/12	Industrial Temp.

PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		VIN, VOUT	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		Vcc	-0.5 to 7.0	V
Power Dissipation		PD	1.0	W
Storage Temperature		TSTG	-65 to 150	℃
Operating Temperature	Commercial	TA	0 to 70	℃
	Industrial	TA	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(TA = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	VIH	2.2	-	Vcc + 0.5**	V
Input Low Voltage	VIL	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* VIL(Min) = -2.0V a.c(Pulse Width≤6ns) for I ≤ 20mA

** VIH(Max) = Vcc + 2.0V a.c (Pulse Width≤6ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(TA = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	VIN = Vss to Vcc		-2	2	μA
Output Leakage Current	ILO	$\overline{CS}$=VIH or $\overline{OE}$=VIH or $\overline{WE}$=VIL VOUT = Vss to Vcc		-2	2	μA
Operating Current	ICC	Min. Cycle, 100% Duty $\overline{CS}$=VIL, VIN = VIH or VIL, IOUT=0mA	8ns	-	160	mA
			10ns	-	150	
			12ns	-	140	
Standby Current	ISB	Min. Cycle, $\overline{CS}$=VIH		-	30	mA
	ISB1	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, VIN ≥ Vcc-0.2V or VIN ≤ 0.2V	Normal	-	10	mA
			L-Ver.	-	1	
Output Low Voltage Level	VOL	IOL=8mA		-	0.4	V
Output High Voltage Level	VOH	IOH=-4mA		2.4	-	V
	VOH1*	IOH1=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(TA =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	CI/O	VI/O=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	6	pF

*** NOTE** : Capacitance is sampled and not 100% tested.

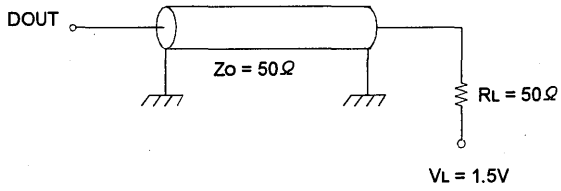
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

TEST CONDITIONS

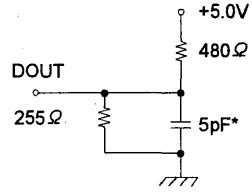
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681002B/BL-8		KM681002B/BL-10		KM681002B-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	8	-	10	-	12	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

WRITE CYCLE

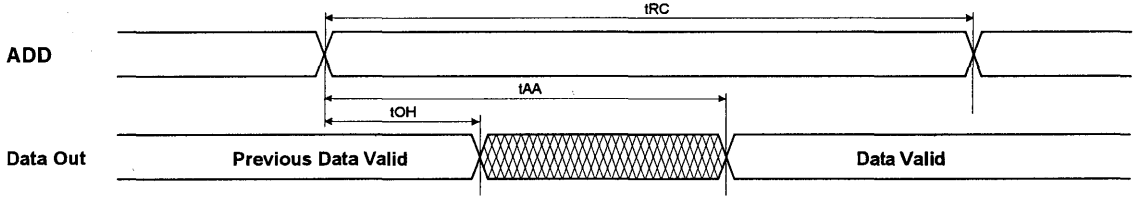
Parameter	Symbol	KM681002B/BL-8		KM681002B/BL-10		KM681002B/BL-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	8	-	10	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

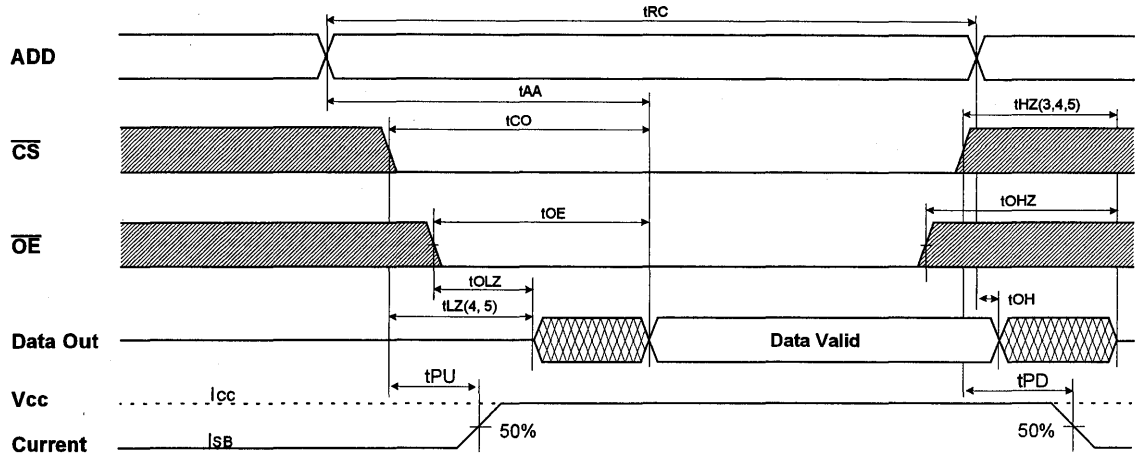
2

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



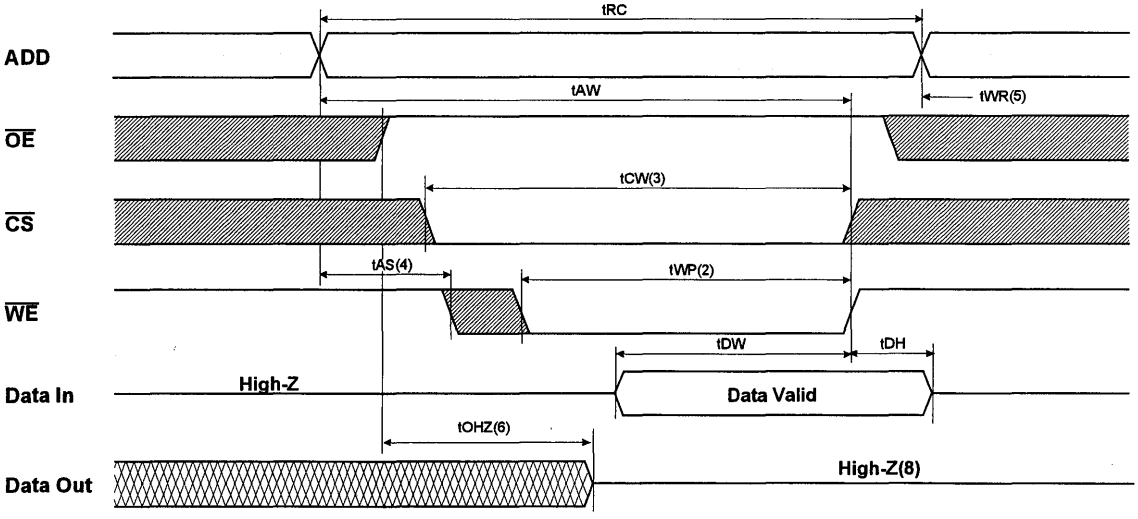
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



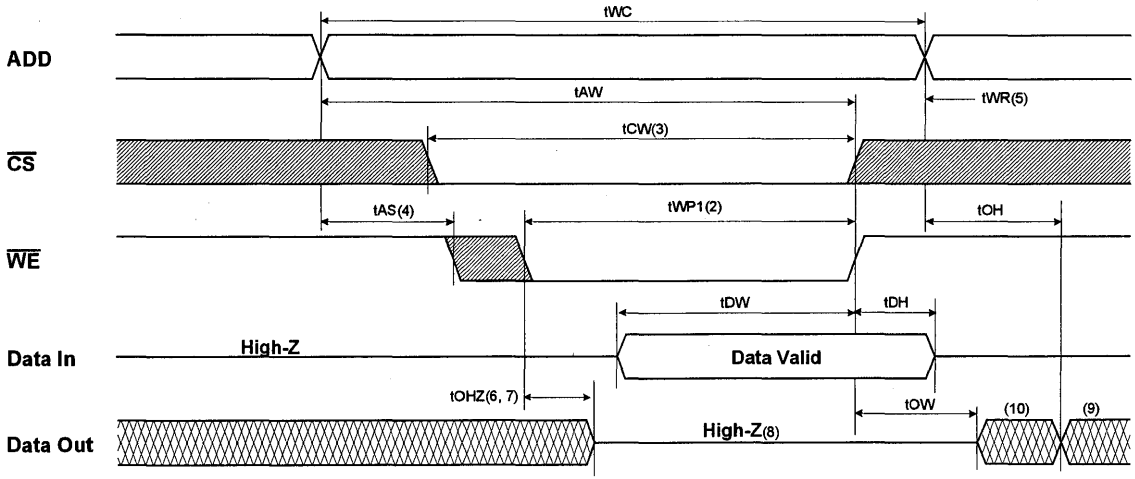
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

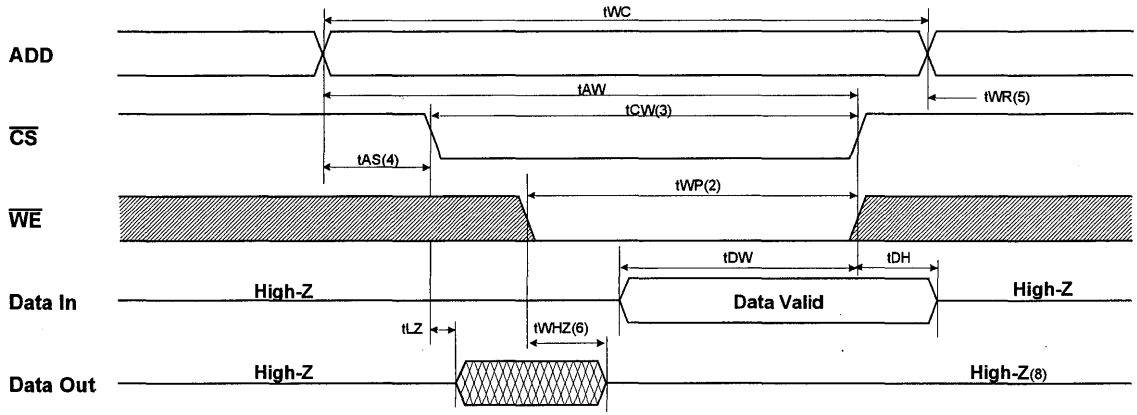
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

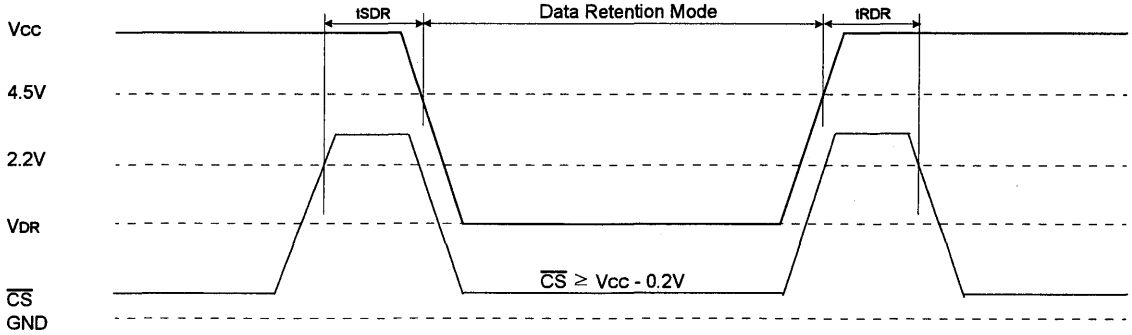
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.9	mA
		V_{CC} = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.7	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

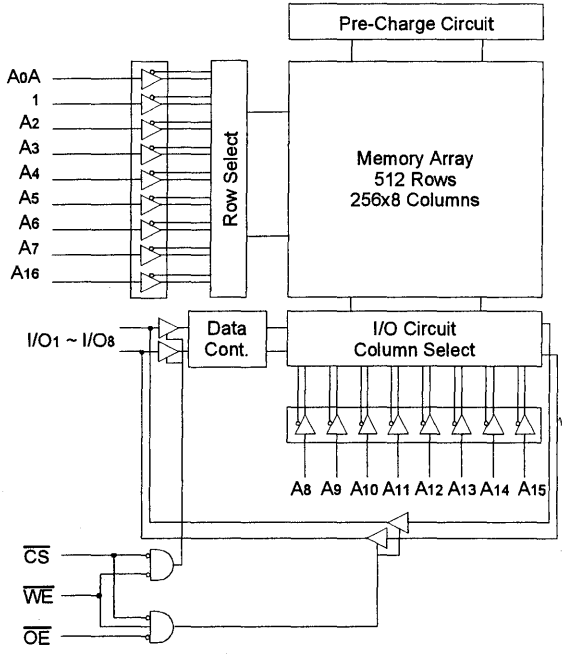
- Fast Access Time 8,10,12ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM68B1002 - 8 : 175mA(Max.)
  - KM68B1002 - 10 : 165mA(Max.)
  - KM68B1002 - 12 : 155mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM68B1002J : 32-SOJ-400

GENERAL DESCRIPTION

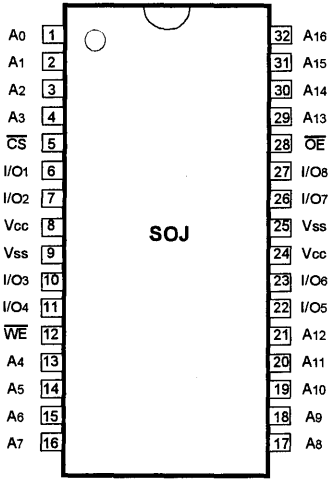
The KM68B1002 is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM68B1002 uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68B1002 is packaged in a 400 mil 32-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤6ns) for I ≤ 20mA

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width≤6ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, V_{CC}= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = V_{SS} to V_{CC}		-10	10	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	8ns	-	175	mA
			10ns	-	165	
			12ns	-	155	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	60	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ V_{CC}-0.2V, V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

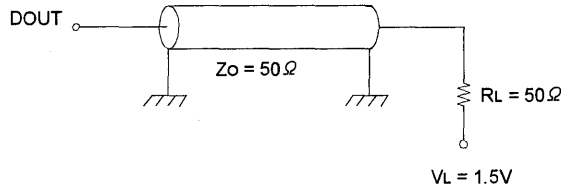
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

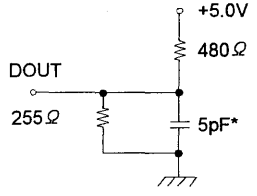
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

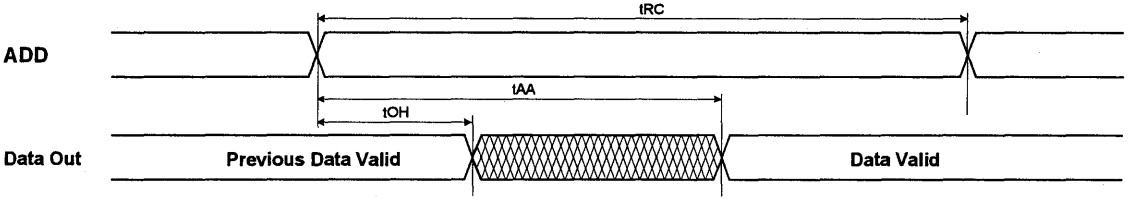
Parameter	Symbol	KM68B1002-8		KM68B1002-10		KM68B1002-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output Access	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

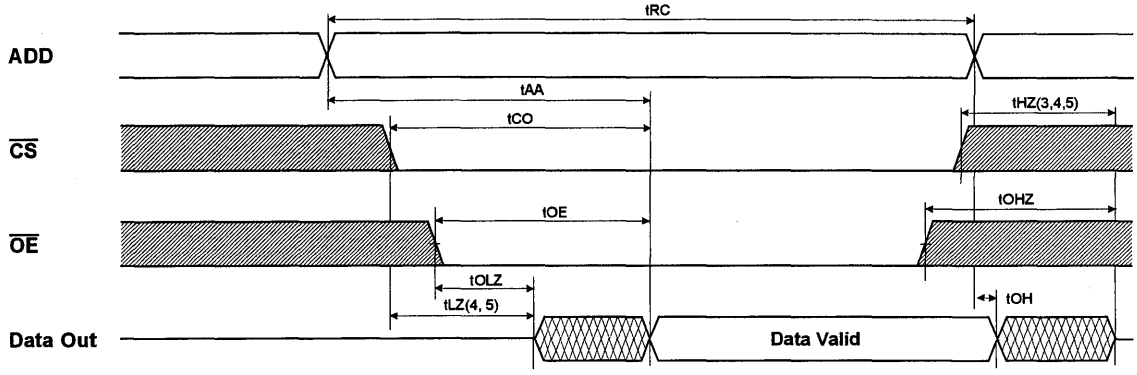
Parameter	Symbol	KM68B1002-8		KM68B1002-10		KM68B1002-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	8	-	9	-	10	-	ns
Write Recovery Time	tWR	1	-	1	-	1	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



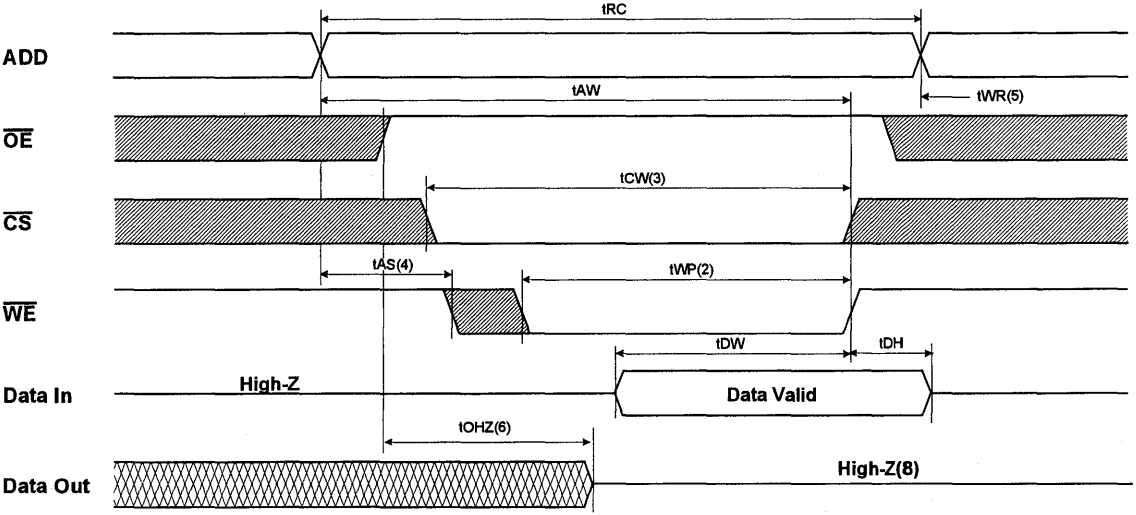
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

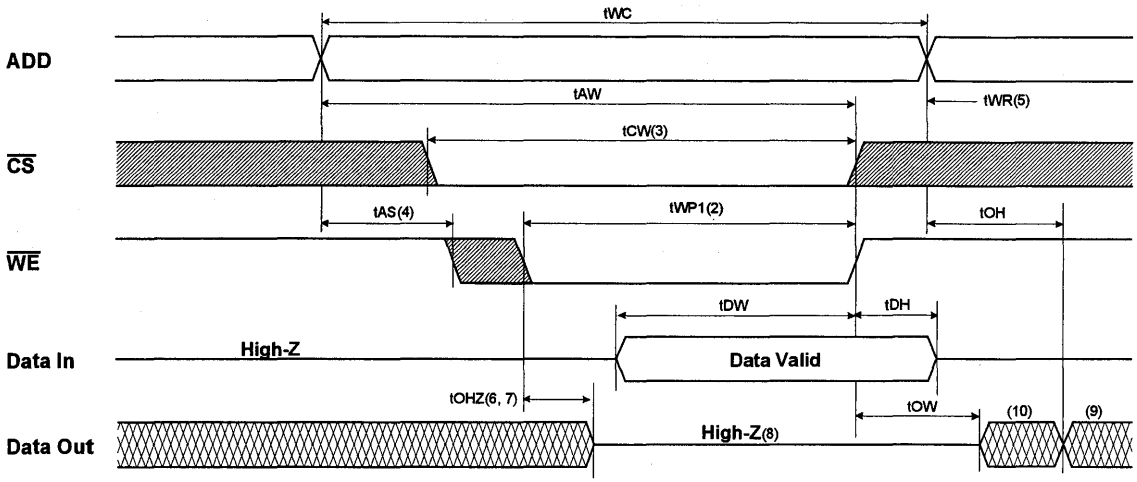
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

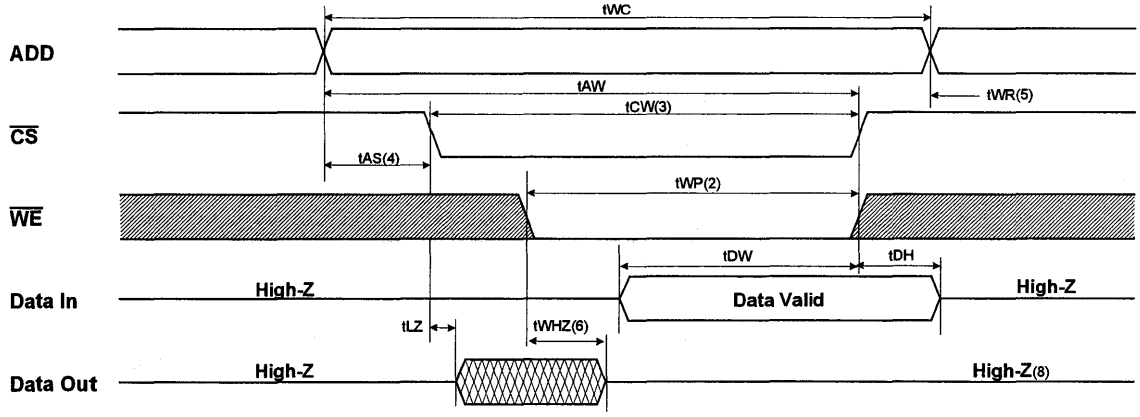


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



SAMSUNG ELECTRONICS

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 12, 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 25mA(Max.)
  - (CMOS) : 8mA(Max.)
  - Operating KM681002A - 12 : 170mA(Max.)
  - KM681002A - 15 : 165mA(Max.)
  - KM681002A - 17 : 165mA(Max.)
  - KM681002A - 20 : 160mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM681002AJ : 32-SOJ-400
  - KM681002ASJ : 32-SOJ-300
  - KM681002AT: 32-TSOP2-400F

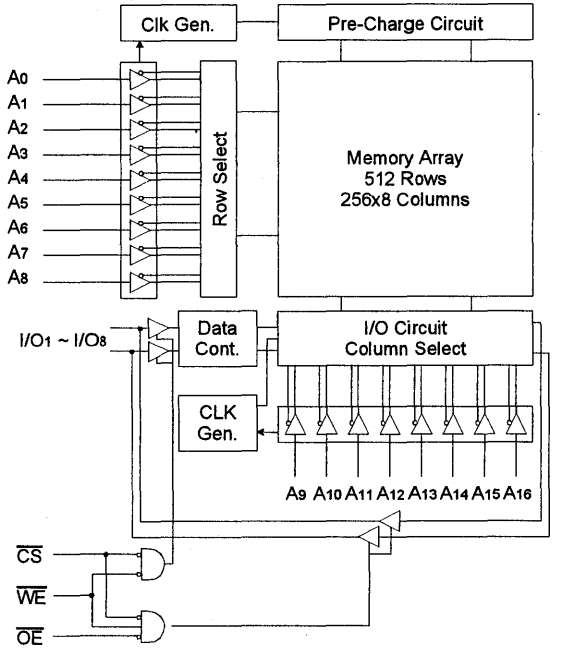
GENERAL DESCRIPTION

The KM681002A is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681002A uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681002A is packaged in a 400/300 mil 32-pin plastic SOJ or TSOP2 forward.

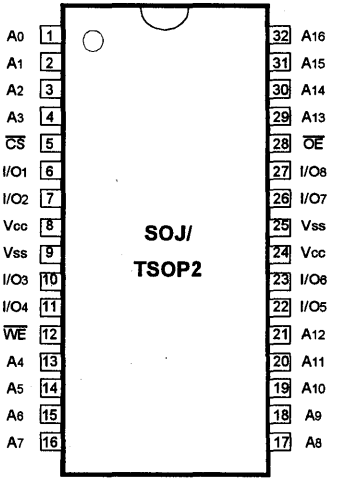
ORDERING INFORMATION

KM681002A -12/15/17/20	Commercial Temp.
KM681002AI -12/15/17/20	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	170	mA
			15ns	-	165	
			17ns	-	165	
			20ns	-	160	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	25	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	8	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

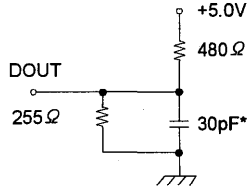
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

TEST CONDITIONS

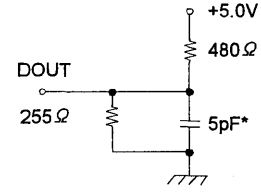
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681002A-12		KM681002A-15		KM681002A-17		KM681002A20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	17	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	12	-	15	-	17	-	20	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

WRITE CYCLE

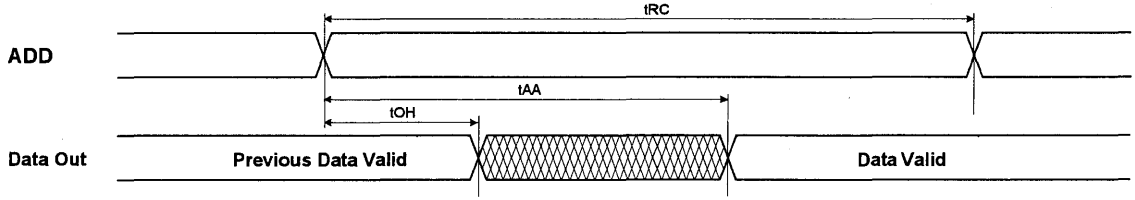
Parameter	Symbol	KM681002A-12		KM681002A-15		KM681002A-17		KM681002A-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	12	-	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

2

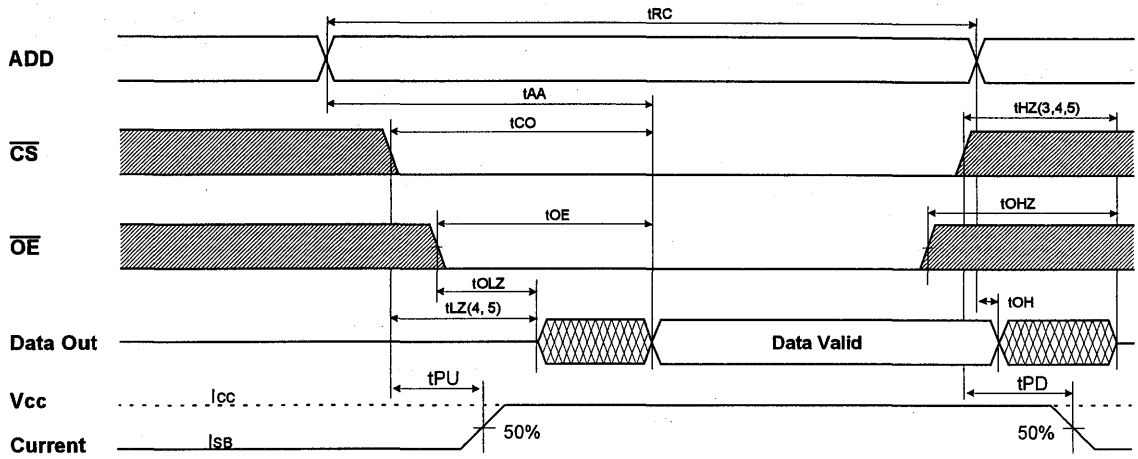
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



SAMSUNG ELECTRONICS

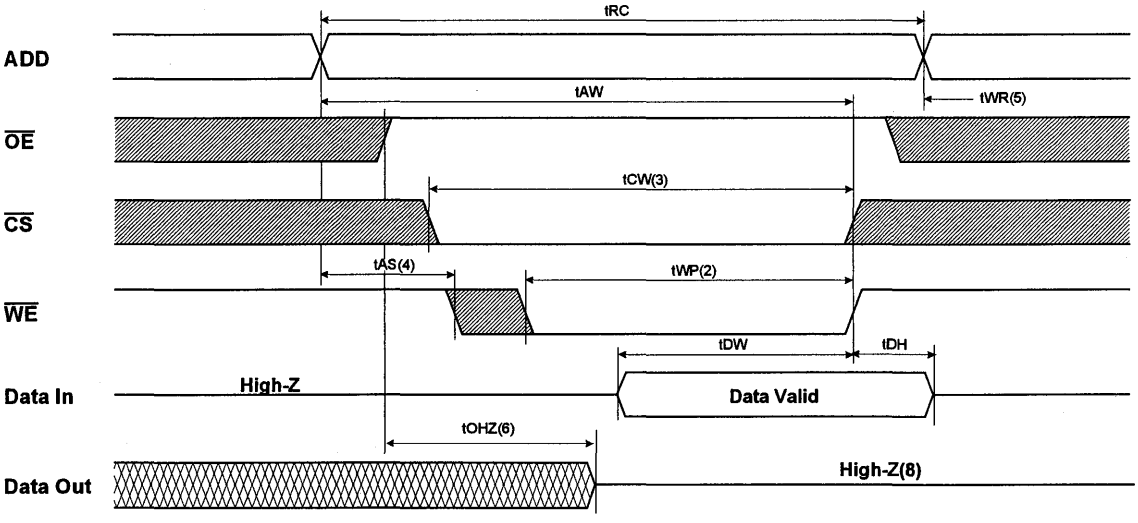
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

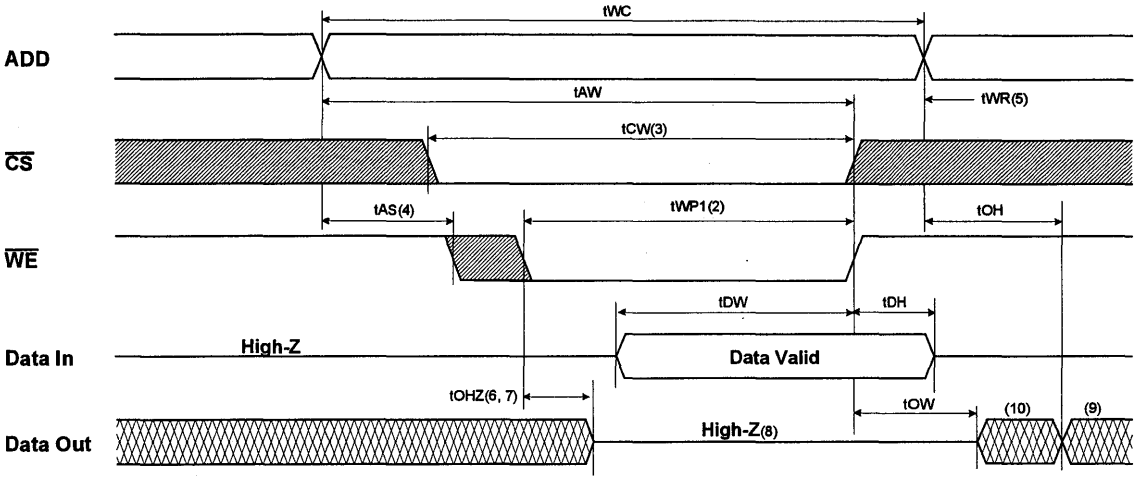
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200㎷ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

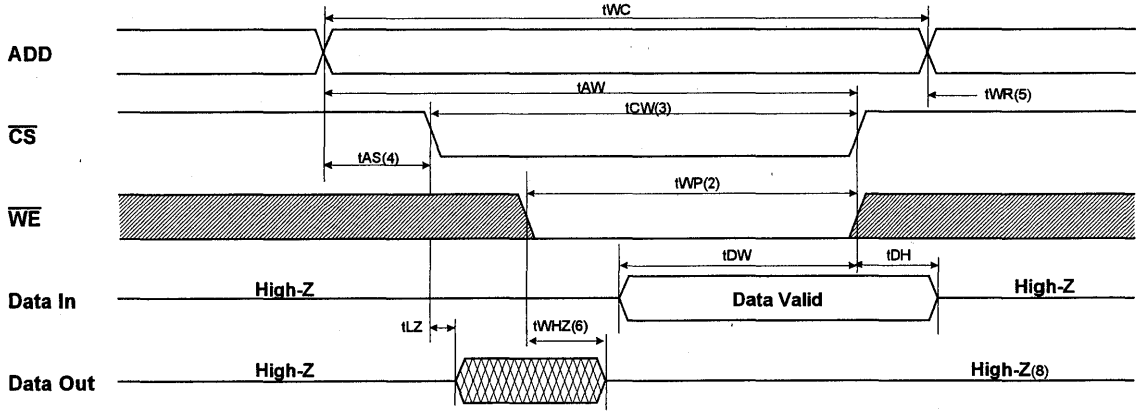


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



SAMSUNG ELECTRONICS

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

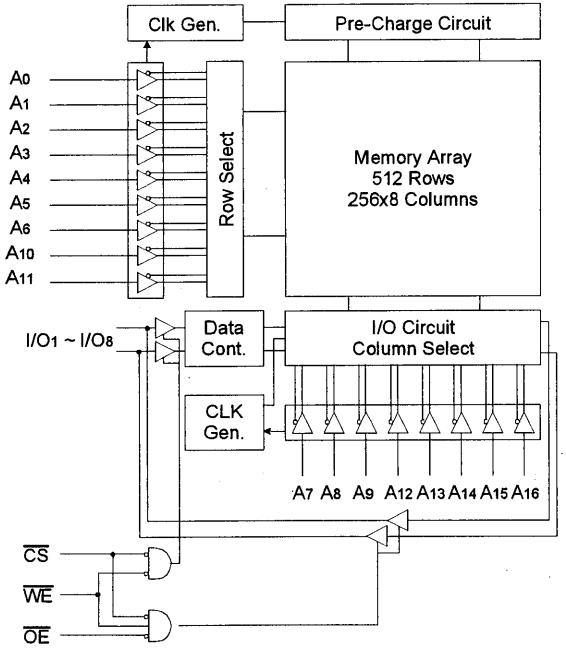
- Fast Access Time 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM681002 - 15 : 170mA(Max.)
  - KM681002 - 17 : 160mA(Max.)
  - KM681002 - 20 : 150mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM681002J : 32-SOJ-400

GENERAL DESCRIPTION

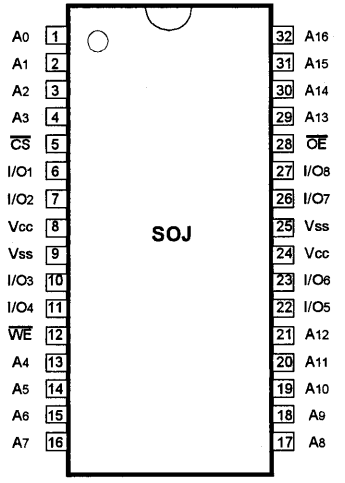
The KM681002 is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681002 uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681002 is packaged in a 400 mil 32-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20㎃

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20㎃

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	㎂
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	㎂
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	170	㎃
			17ns	-	160	
			20ns	-	150	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	㎃
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	㎃
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

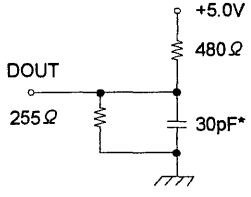
AC CHARACTERISTICS(TA = 0 to 70℃, Vcc = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

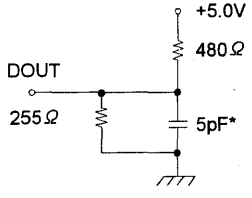
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

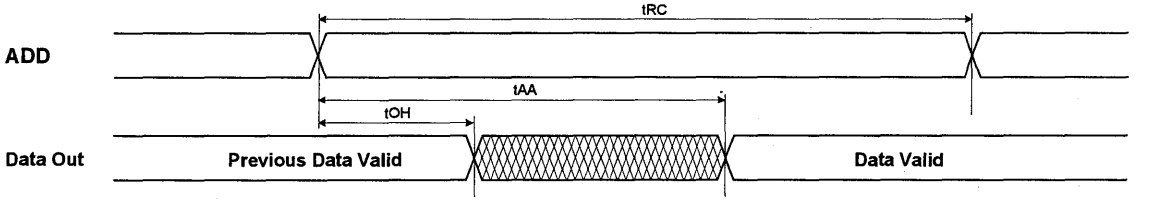
Parameter	Symbol	KM681002-15		KM681002-17		KM681002-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9	-	10	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	4	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

WRITE CYCLE

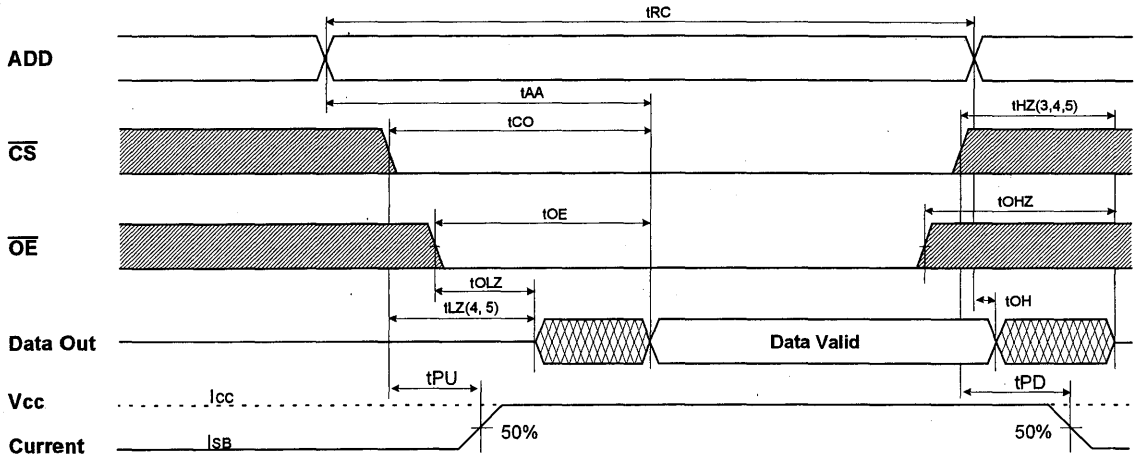
Parameter	Symbol	KM681002-15		KM681002-17		KM681002-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	12	-	13	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	9	-	10	-	11	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



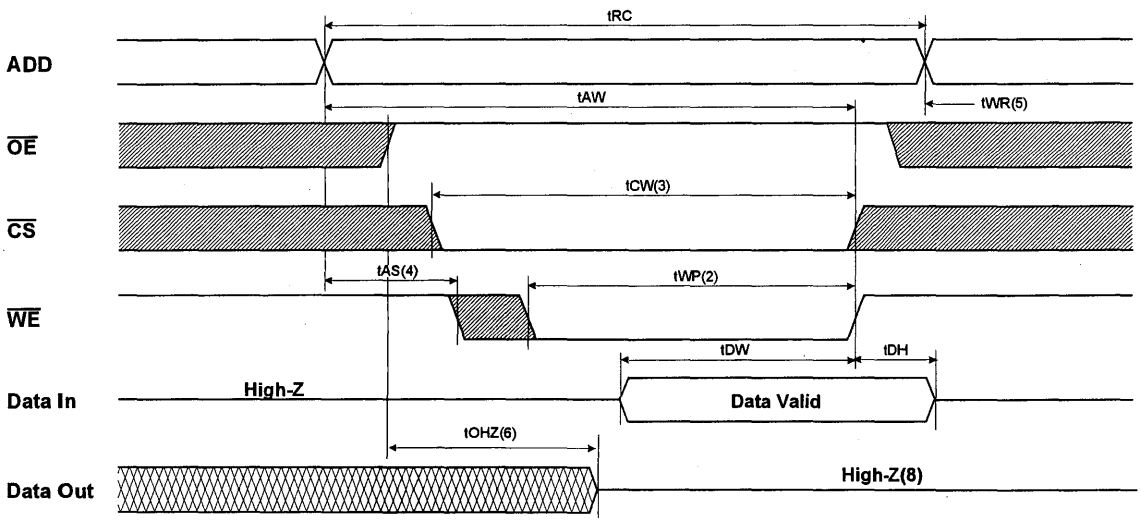
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

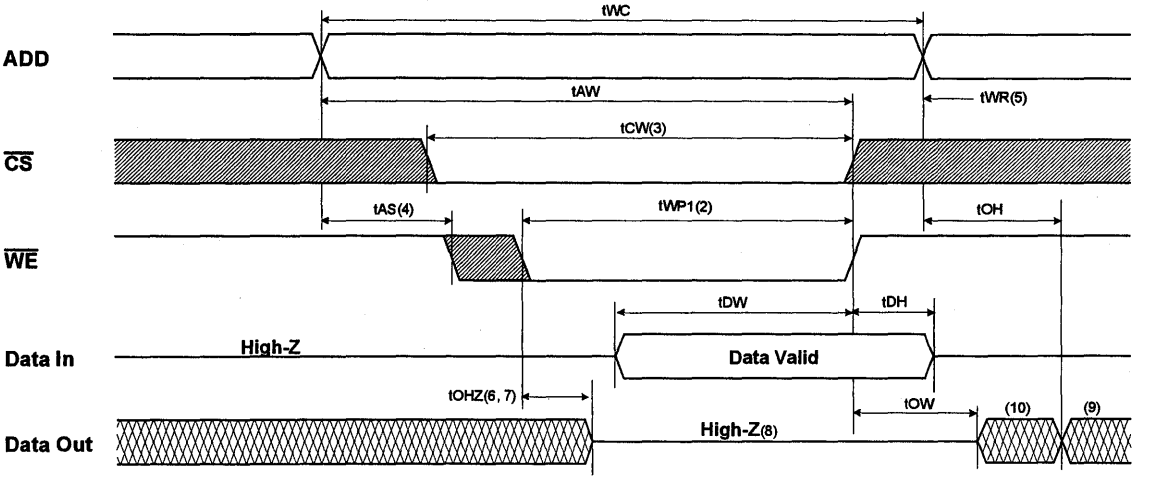
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

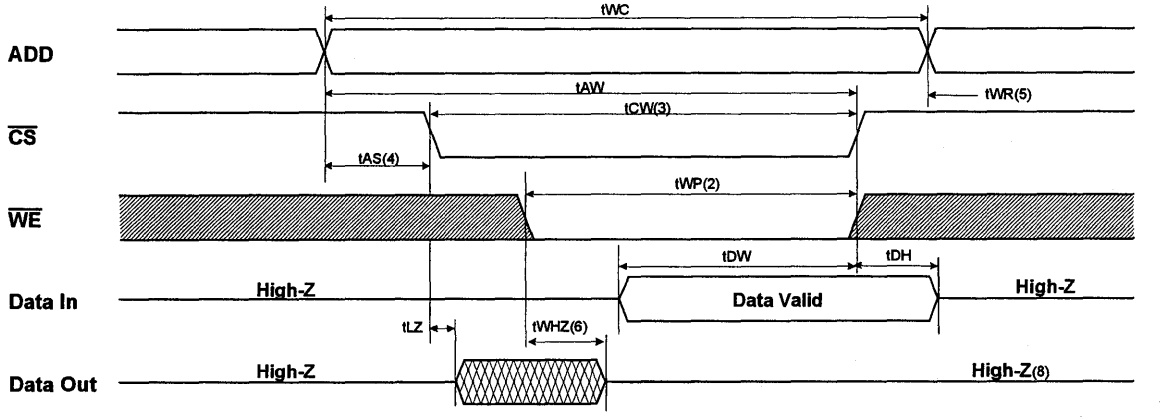


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 20mA(Max.)
  - (CMOS) : 5mA(Max.)
  - 0.5mA(Max.) - L-Ver. only
  - Operating KM681001B/BL - 15 : 130mA(Max.)
  - KM681001B/BL - 17 : 120mA(Max.)
  - KM681001B/BL - 20 : 110mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Standard Pin Configuration
  - KM681001B/BLJ : 32-SOJ-400
  - KM681001B/BLSJ : 32-SOJ-300

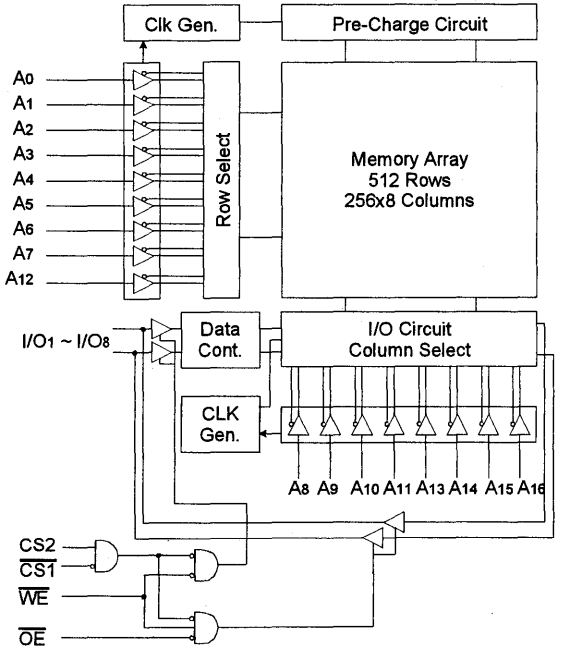
GENERAL DESCRIPTION

The KM681001B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681001B/BL uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681001B/BL is packaged in a 400/300 mil 32-pin plastic SOJ and TSOP1.

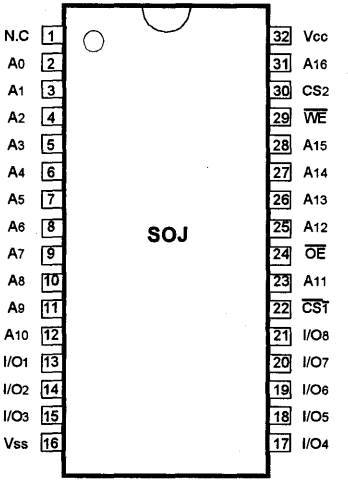
ORDERING INFORMATION

KM681001B/BL -15/17/20	Commercial Temp.
KM681001BI/BLI -15/17/20	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS1, CS2	Chip Selects
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20㎃

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20㎃

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	㎂
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	㎂
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	130	㎃
			17ns	-	120	
			20ns	-	110	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	20	㎃
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	5	㎃
			L-Ver.	-	0.5	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

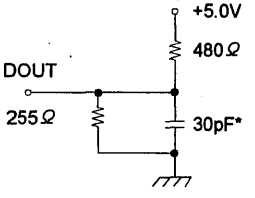
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

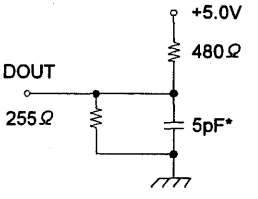
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681001B/BL-15		KM681001B/BL-17		KM681001B/BL-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO*	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9	-	10	ns
Chip Enable to Low-Z Output	tLZ*	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ*	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

NOTE 1: Above parameters are also guaranteed at industrial temperature range.
NOTE 2: tCO = tCO1, tCO2 / tLZ = tLZ1, tLZ2 / tHZ = tHZ1, tHZ2

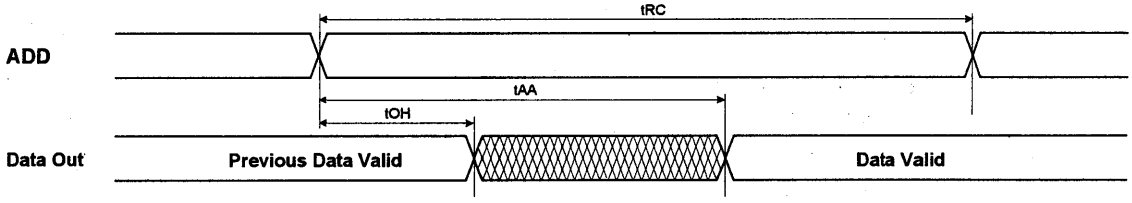
WRITE CYCLE

Parameter	Symbol	KM681001B/BL-15		KM681001B/BL-17		KM681001B/BL-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR*	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	9	0	10	ns
Data to Write Time Overlap	tDW	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

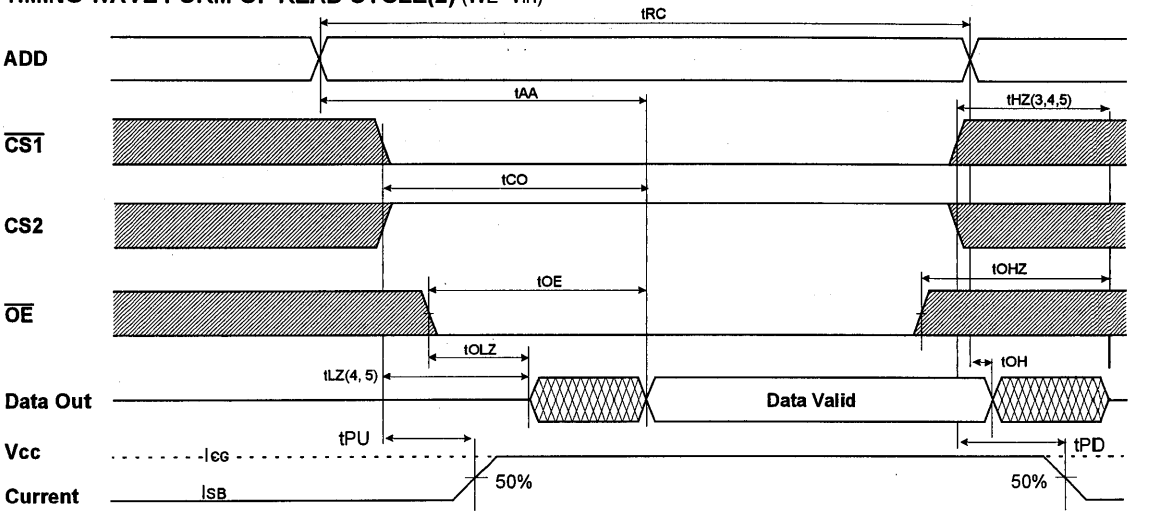
NOTE 1: Above parameters are also guaranteed at industrial temperature range.
NOTE 2: tWR = tWR1, tWR2

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}1=\overline{OE}=V_{IL}$, CS2=$\overline{WE}=V_{IH}$)



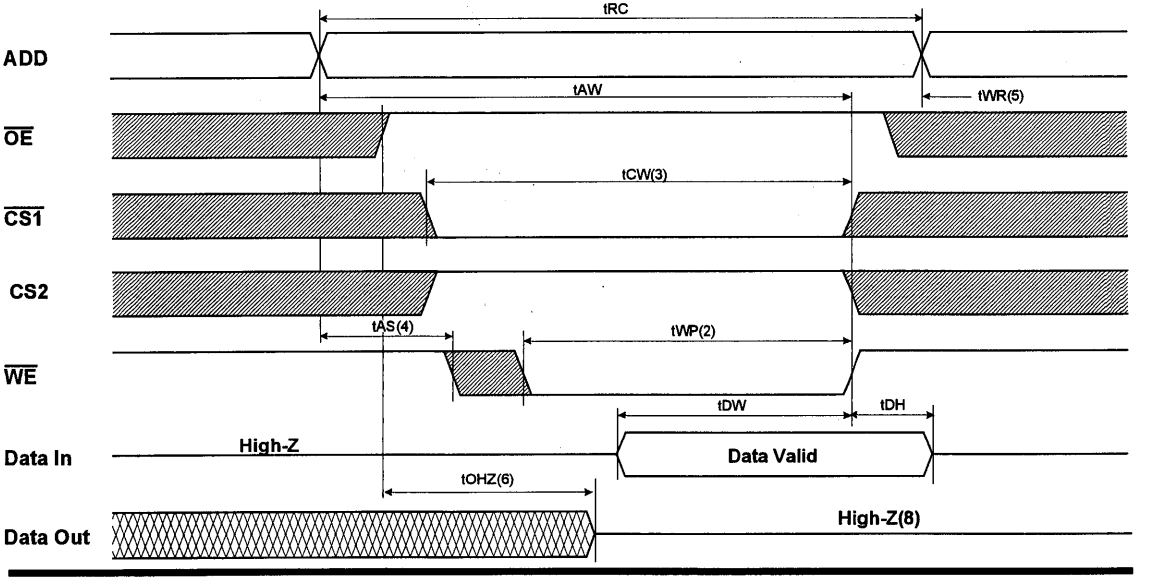
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



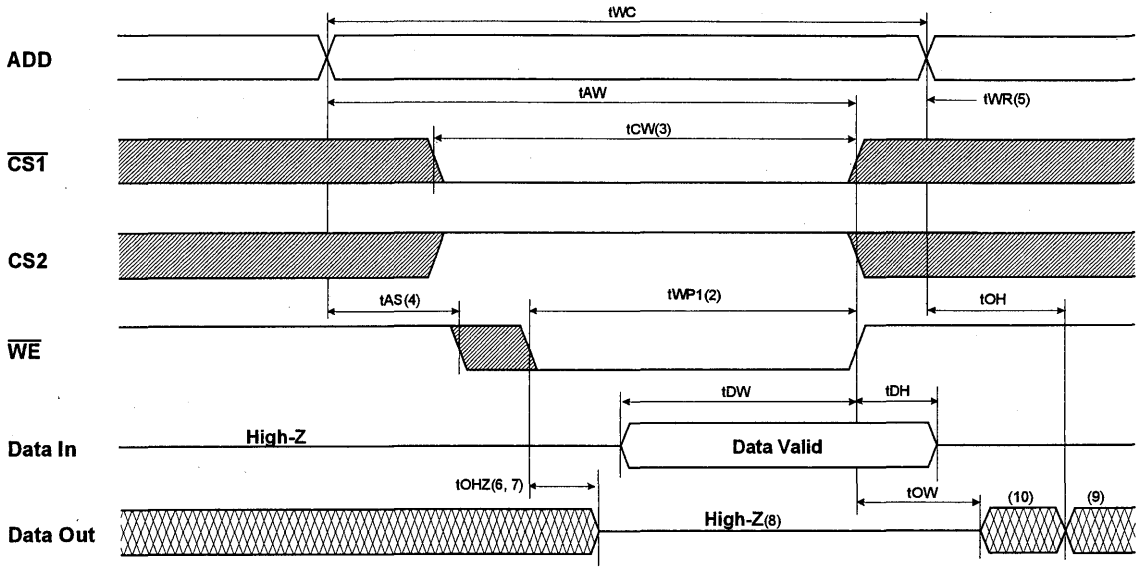
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS1}$=VIL and CS2=VIH.
7. Address valid prior to coincident with $\overline{CS1}$ transition low and CS2 transition high.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

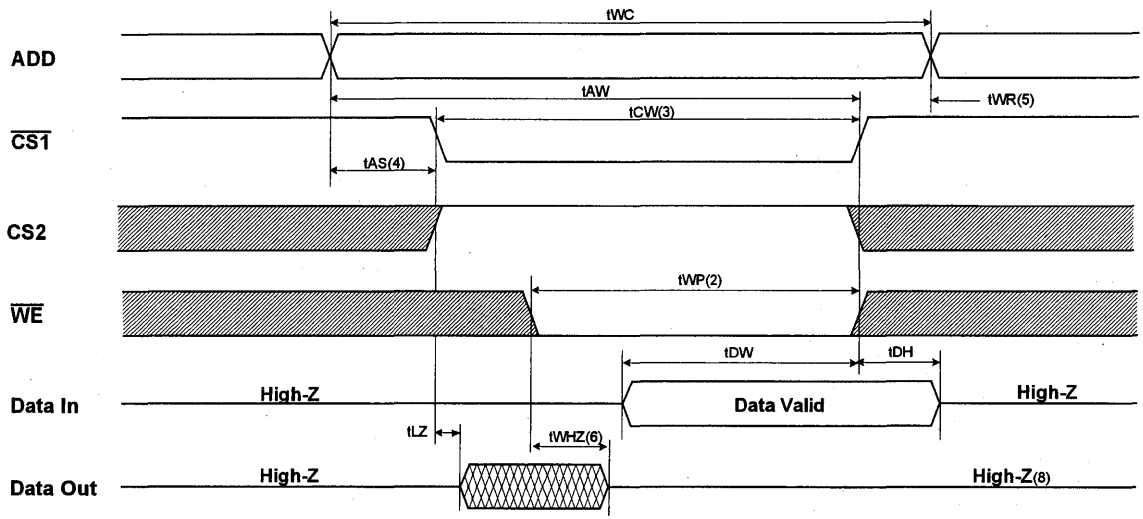
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



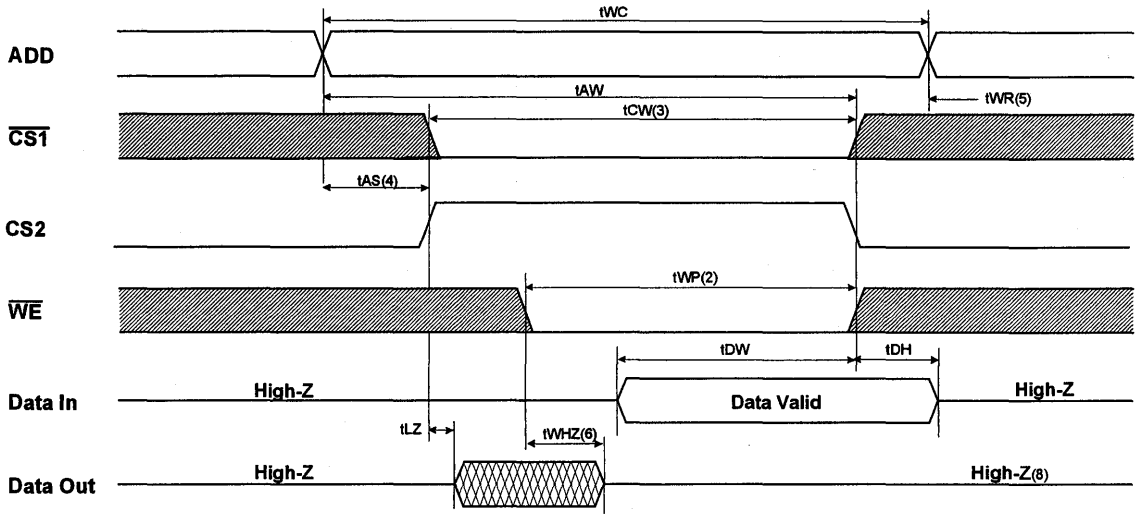
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS1}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (CS2=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS1}$ going high or CS2 going low or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high. tWR2 applied in case a write ends as CS2 going low.
6. If $\overline{OE}$, $\overline{CS1}$, CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS1}$ goes low and CS2 goes high simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS1}$ is low and CS2 is high : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

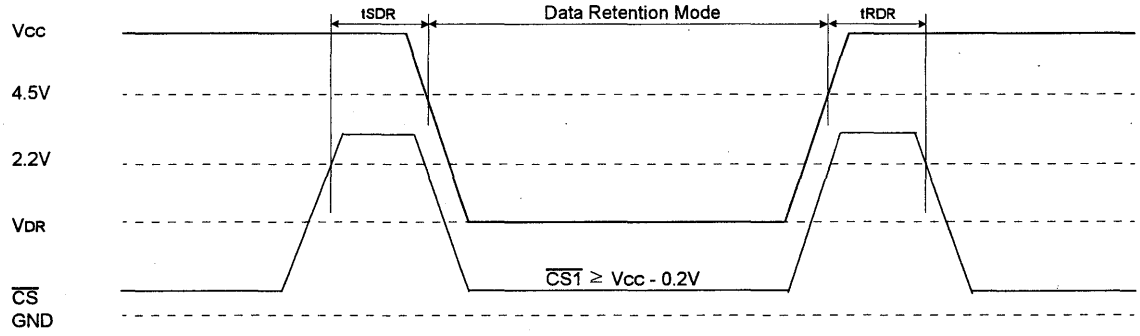
DATA RETENTION CHARACTERISTICS* (T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	V_{DR}	$\overline{CS1} \geq Vcc - 0.2VB$ or $CS2 \leq 0.2V$	2.0	-	5.5	V
Data Retention Current	I_{DR}	Vcc = 3.0V, $\overline{CS1} \geq Vcc - 0.2V$ or $CS2 \leq 0.2V$ $V_{IN} \geq Vcc - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	0.40	mA
		Vcc = 2.0V, $\overline{CS} \geq Vcc - 0.2V$ $V_{IN} \geq Vcc - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	0.35	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

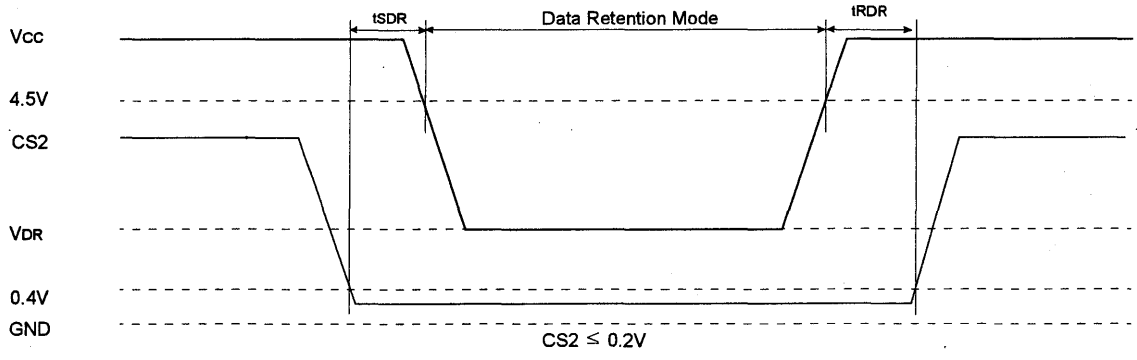
NOTE: Above parameters are also guaranteed at industrial temperature range.
* : L-Ver only.

2

DATA RETENTION WAVE FORM 1 ($\overline{CS1}$ Controlled)



DATA RETENTION WAVE FORM 2 (CS2 Controlled)



128K x 8 Bit High-Speed CMOS Static RAM

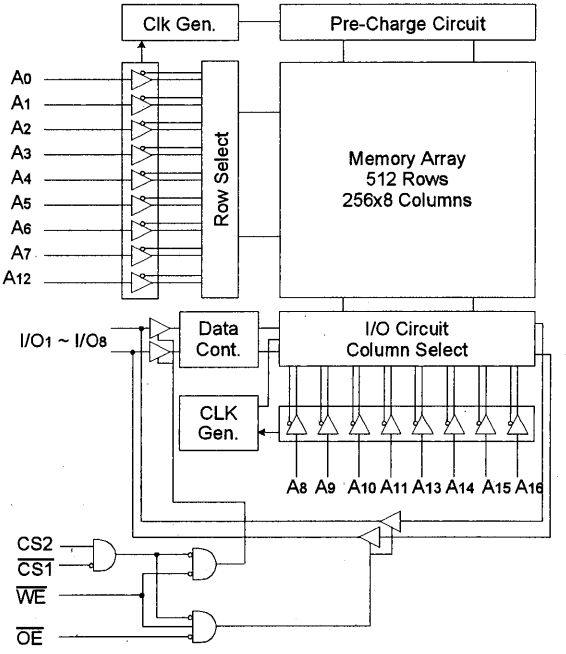
FEATURES

- Fast Access Time 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 25mA(Max.)
  - (CMOS) : 8mA(Max.)
  - Operating KM681001A - 15 : 125mA(Max.)
  - KM681001A - 17 : 125mA(Max.)
  - KM681001A - 20 : 120mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
  - KM681001AJ : 32-SOJ-400
  - KM681001ASJ : 32-SOJ-300

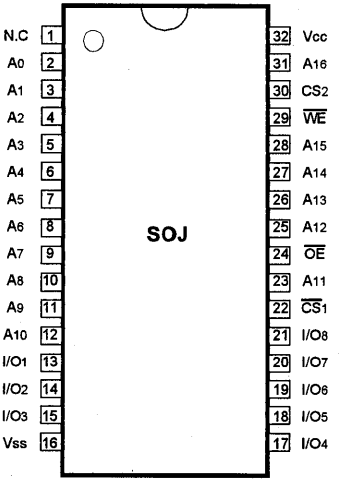
GENERAL DESCRIPTION

The KM681001A is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681001A uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681001A is packaged in a 400/300 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS1}$, CS2	Chip Selects
$\overline{OE}$	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS1}$=V_{IL}, CS2=V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	125	mA
			17ns	-	125	
			20ns	-	120	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS1}$=V_{IH} or CS2=V_{IL}		-	25	mA
	I_{SB1}	f=0MHz, $\overline{CS1}$ ≥ Vcc-0.2V or CS2 ≤ 0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	8	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

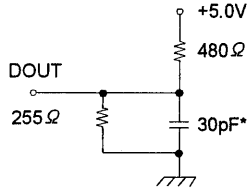
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(TA = 0 to 70℃, Vcc = 5.0V±10%, unless otherwise noted.)

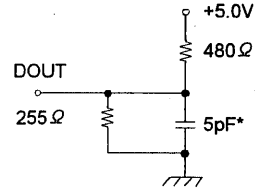
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681001A-15		KM681001A-17		KM681001A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO*	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9	-	10	ns
Chip Enable to Low-Z Output	tLZ*	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ*	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

NOTE: tCO = tCO1, tCO2 / tLZ = tLZ1, tLZ2 / tHZ = tHZ1, tHZ2

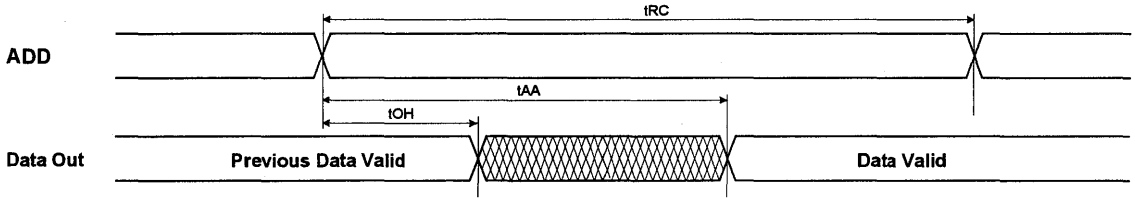
WRITE CYCLE

Parameter	Symbol	KM681001A-15		KM681001A-17		KM681001A-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR*	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	9	0	10	ns
Data to Write Time Overlap	tDW	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

NOTE: tWR = tWR1, tWR2

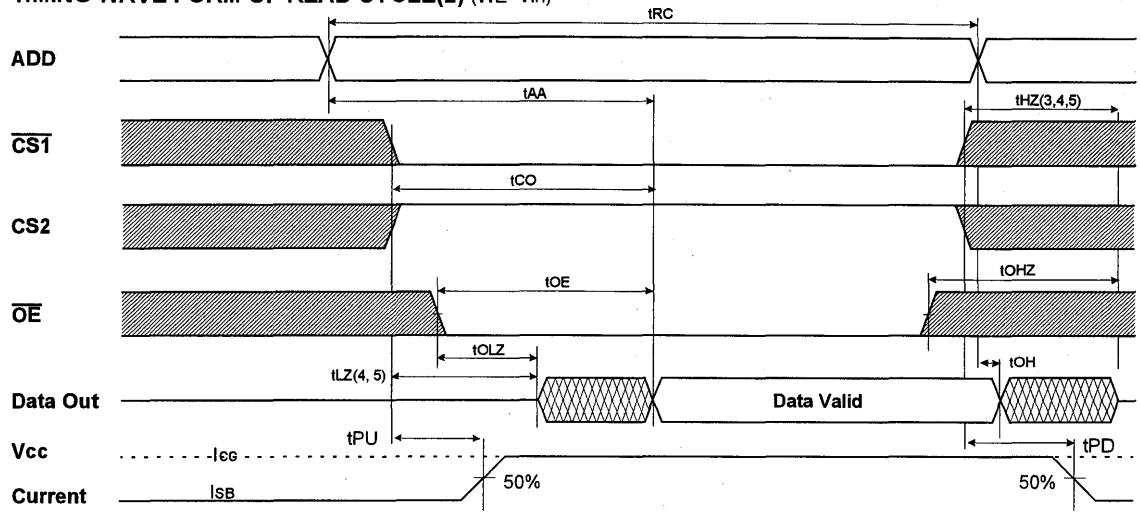
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}1=\overline{OE}=V_{IL}$, CS2=$\overline{WE}=V_{IH}$)



SAMSUNG ELECTRONICS

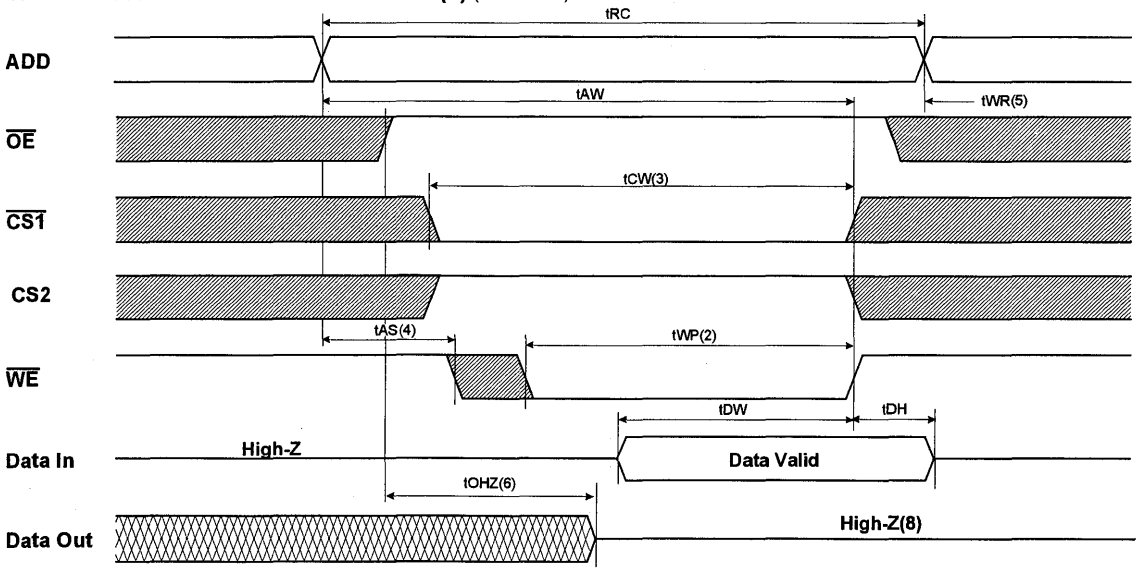
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

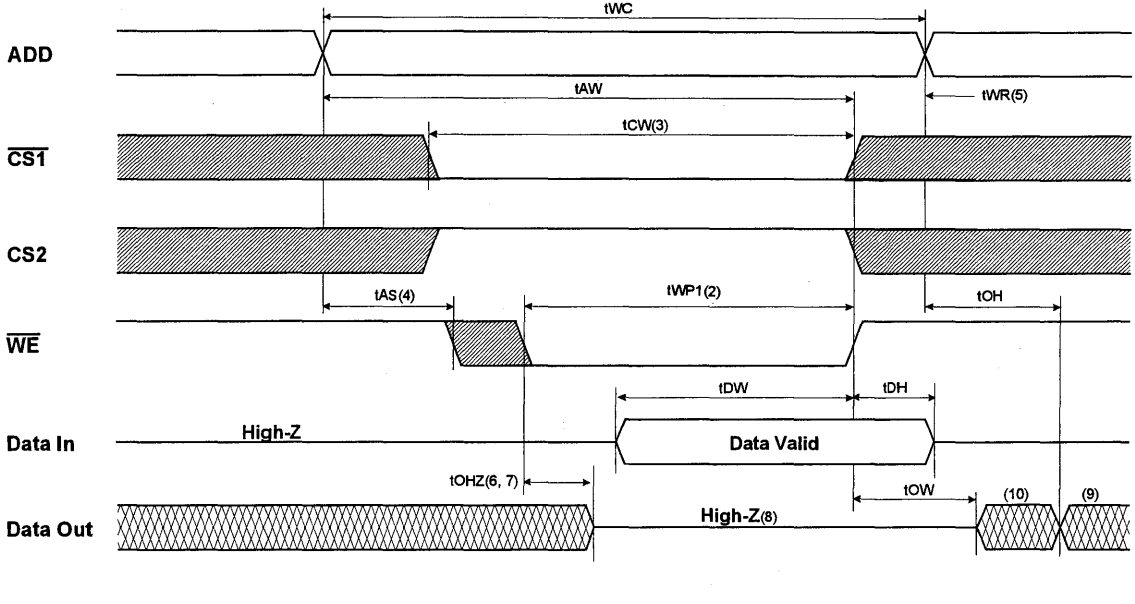
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200㎷ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS1}$=VIL and CS2=VIH.
7. Address valid prior to coincident with $\overline{CS1}$ transition low and CS2 transition high.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

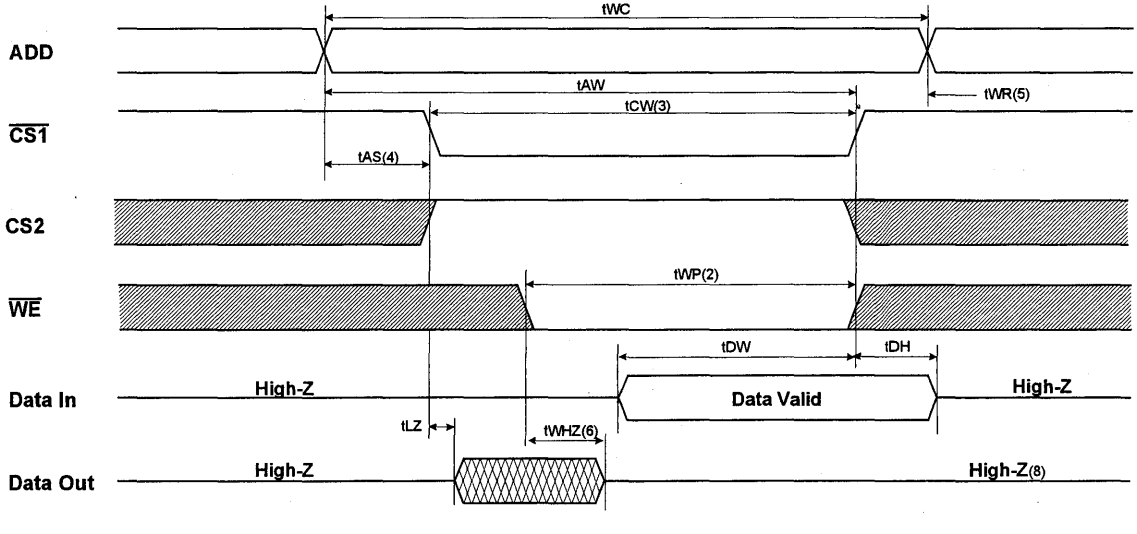


SAMSUNG ELECTRONICS

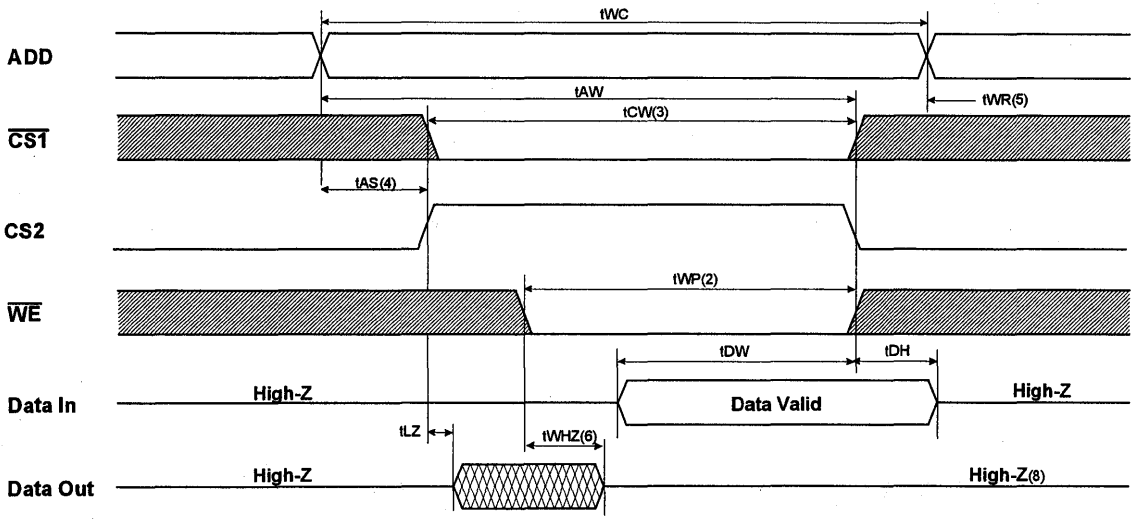
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS1}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (CS2=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS1}$ going high or CS2 going low or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high. tWR2 applied in case a write ends as CS2 going low.
6. If $\overline{OE}$, $\overline{CS1}$, CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS1}$ goes low and CS2 goes high simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS1}$ is low and CS2 is high : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

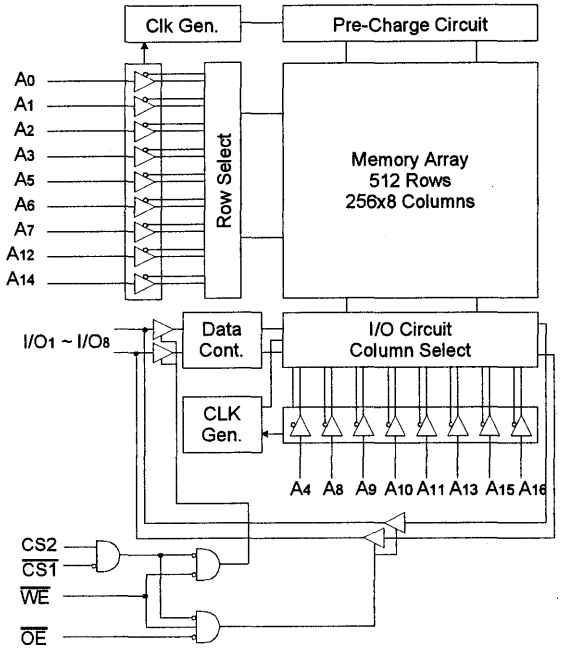
- Fast Access Time 20,25,35ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 2mA(Max.)
  - 0.5mA(Max.) - L-Ver. only
  - Operating KM681001/L - 20 : 170mA(Max.)
  - KM681001/L - 25 : 150mA(Max.)
  - KM681001/L - 35 : 130mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; 2V(Min.) - L-ver. only
- Standard Pin Configuration
  - KM681001/LP : 32-DIP-400
  - KM681001/LJ : 32-SOJ-400

GENERAL DESCRIPTION

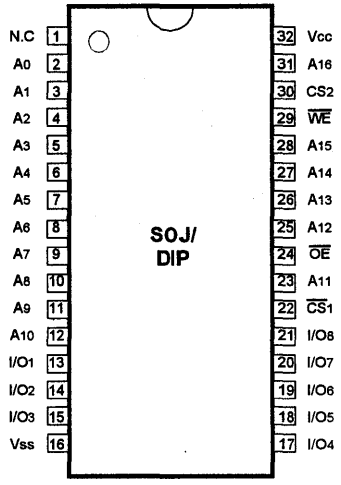
The KM681001/L is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681001/L uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681001/L is packaged in a 400 mil 32-pin plastic DIP or SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS1}$, CS2	Chip Selects
$\overline{OE}$	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS1}$=V_{IL}, CS2=V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	20ns	-	170	mA
			25ns	-	150	
			35ns	-	130	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS1}$=V_{IH} or CS2=V_{IL}		-	40	mA
	I_{SB1}	f=0MHz, $\overline{CS1}$ ≥ Vcc-0.2V or CS2 ≤ 0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	2	mA
			L-Ver.	-	0.5	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	7	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

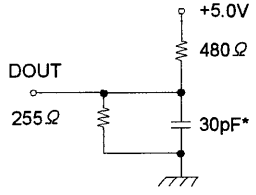
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

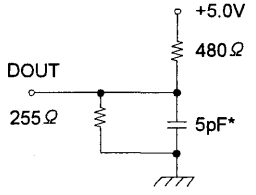
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681001/L-20		KM681001/L-25		KM681001/L-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	20	-	25	-	35	-	ns
Address Access Time	tAA	-	20	-	25	-	35	ns
Chip Select to Output	tCO*	-	20	-	25	-	35	ns
Output Enable to Valid Output	tOE	-	10	-	13	-	15	ns
Chip Enable to Low-Z Output	tLZ*	0	-	0	-	0	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ*	0	12	0	15	0	15	ns
Output Disable to High-Z Output	tOHZ	0	8	0	10	0	15	ns
Output Hold from Address Change	tOH	3	-	5	-	5	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	20	-	25	-	35	ns

NOTE: tCO = tCO1, tCO2 / tLZ = tLZ1, tLZ2 / tHZ = tHZ1, tHZ2

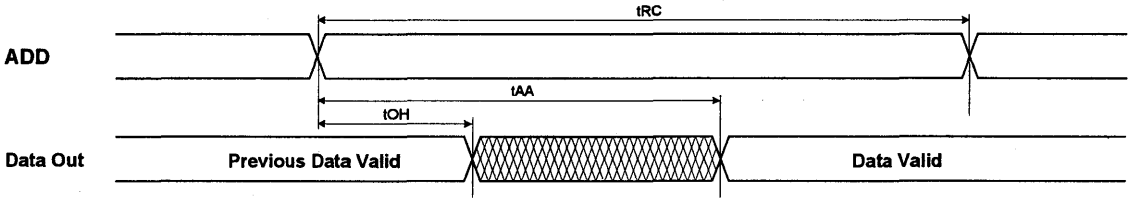
WRITE CYCLE

Parameter	Symbol	KM681001/L-20		KM681001/L-25		KM681001/L-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	20	-	25	-	35	-	ns
Chip Select to End of Write	tCW	17	-	20	-	30	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	17	-	20	-	30	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	15	-	20	-	25	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	20	-	25	-	35	-	ns
Write Recovery Time	tWR*	2	-	3	-	3	-	ns
Write to Output High-Z	tWHZ	0	8	0	10	0	12	ns
Data to Write Time Overlap	tDW	12	-	15	-	20	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

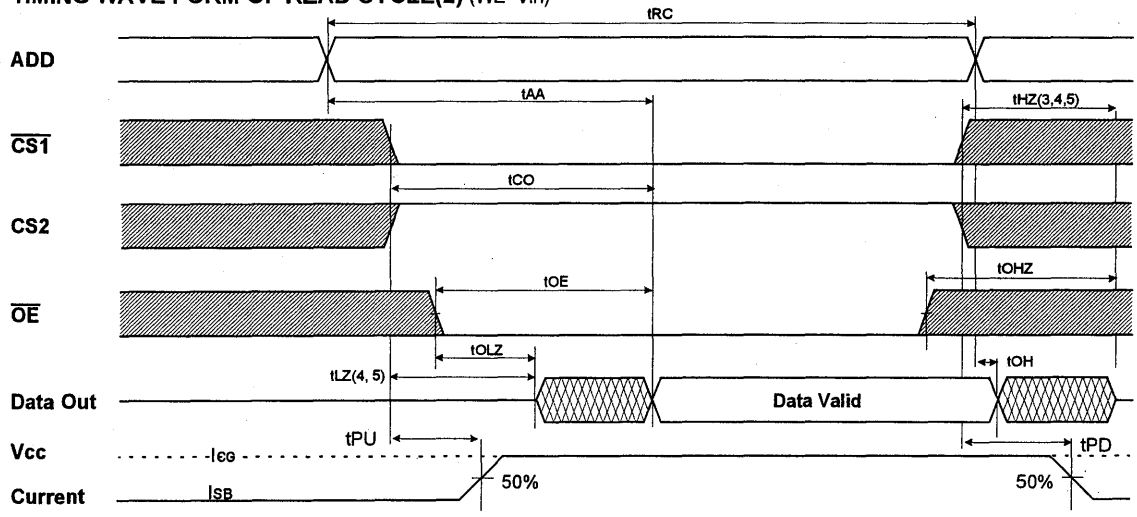
NOTE: tWR = tWR1, tWR2

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}$=$\overline{OE}$=VIL, CS2=$\overline{WE}$=VIH)



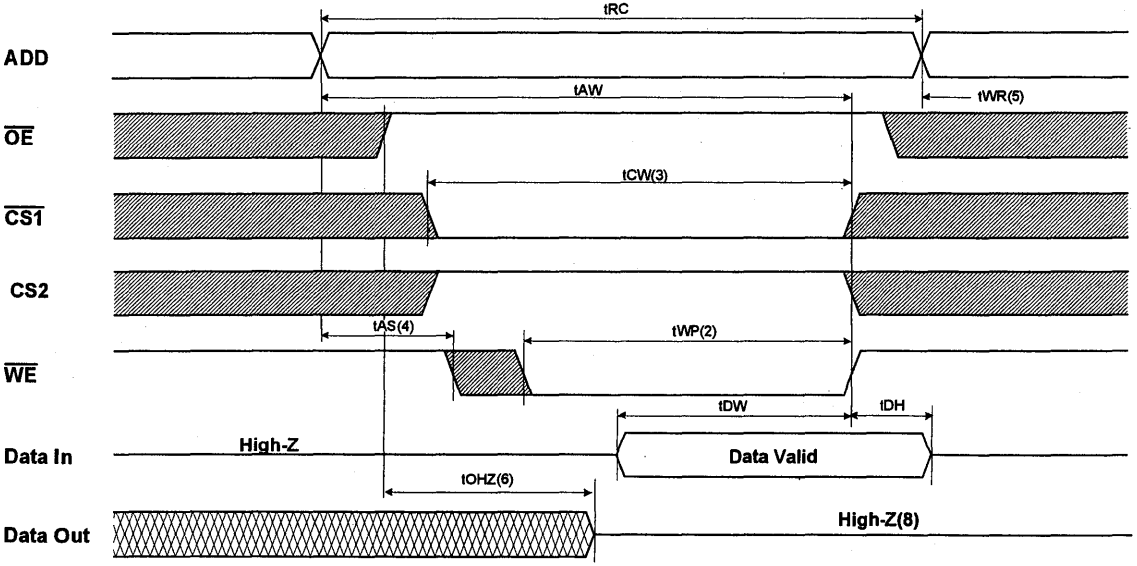
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



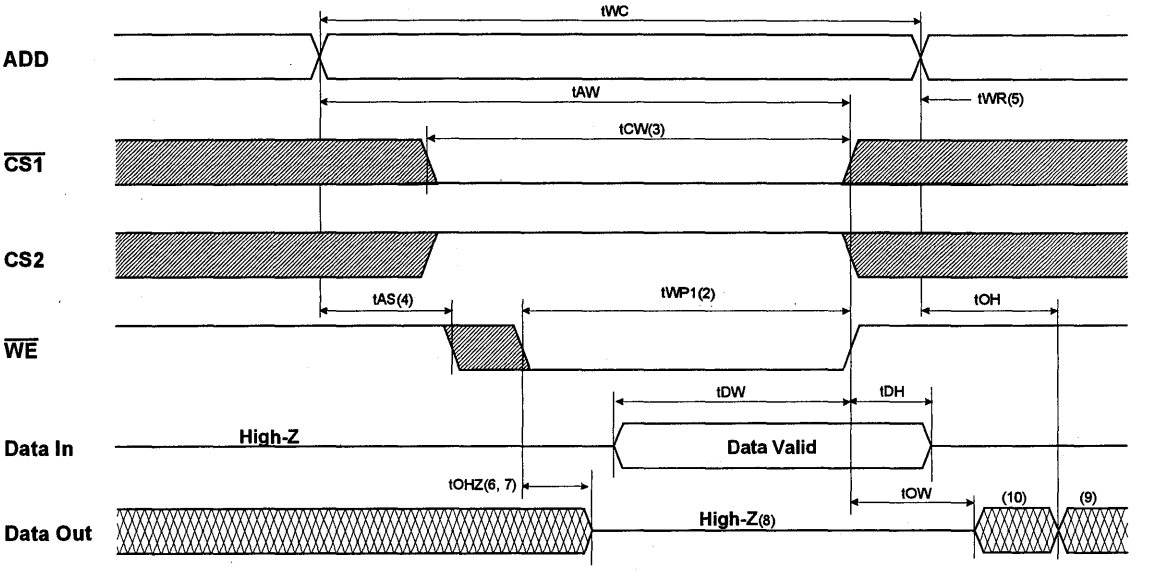
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS1}$=VIL and CS2=VIH.
7. Address valid prior to coincident with $\overline{CS1}$ transition low and CS2 transition high.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

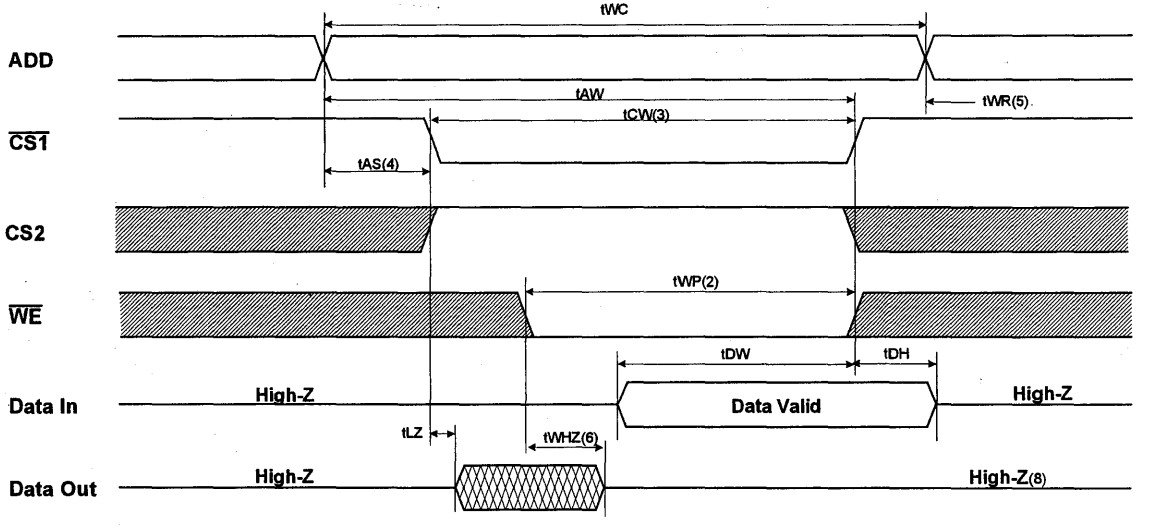
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



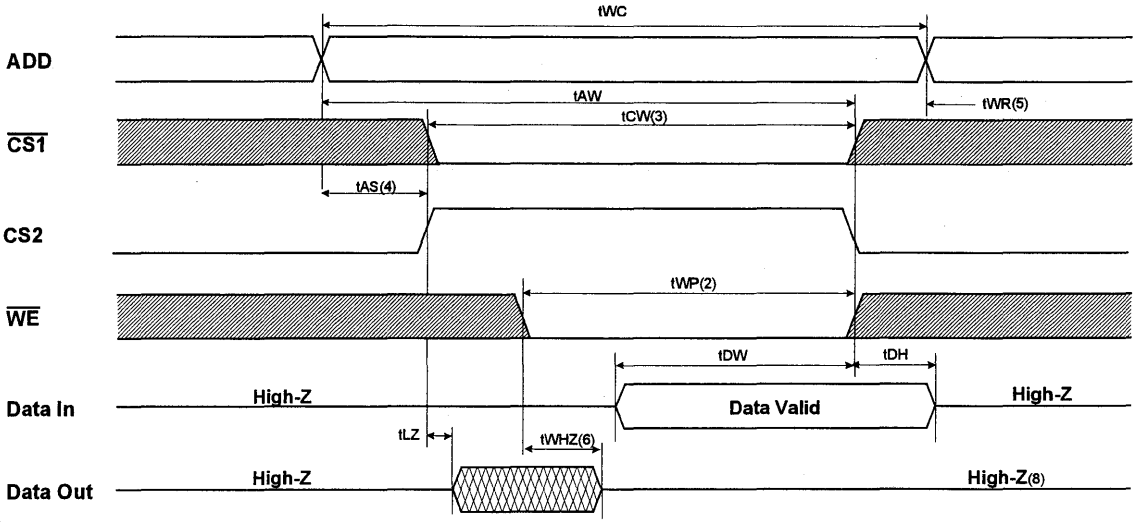
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS1}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) (CS2=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS1}$ going high or CS2 going low or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high. tWR2 applied in case a write ends as CS2 going low.
6. If $\overline{OE}$, $\overline{CS1}$, CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS1}$ goes low and CS2 goes high simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS1}$ is low and CS2 is high : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	L	H	H	Output Disable	High-Z	I_{CC}
L	L	H	L	Read	D_{OUT}	I_{CC}
L	L	L	X	Write	D_{IN}	I_{CC}

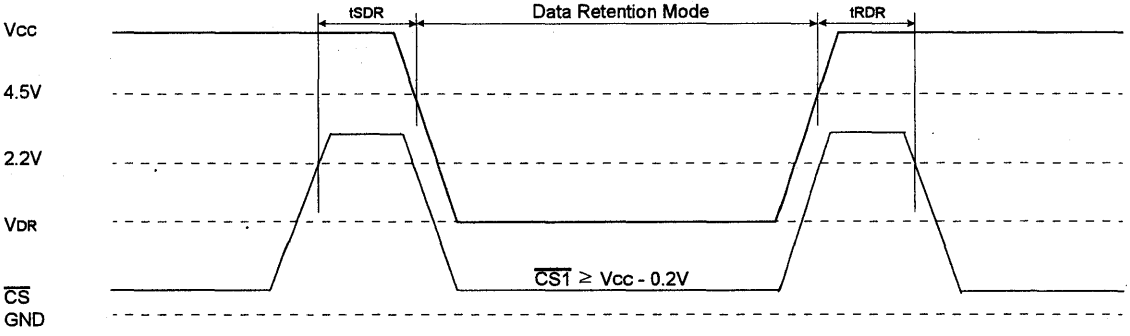
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS* (T_A = 0℃ to 70℃)

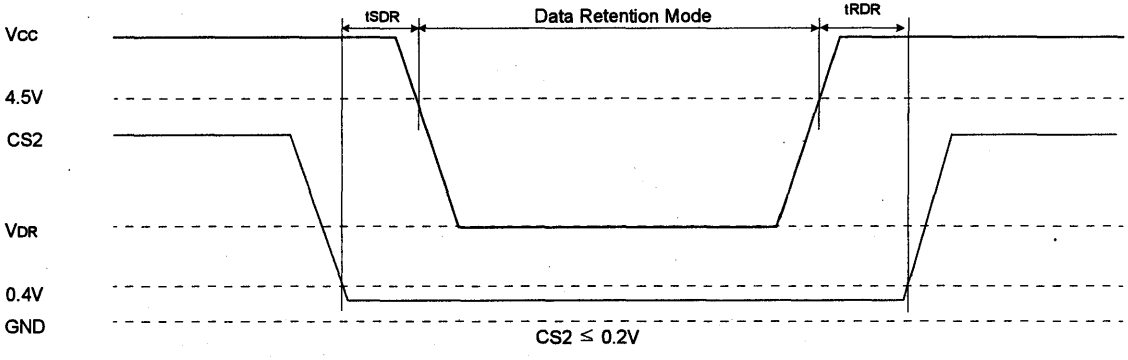
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC}$ - 0.2V or CS2 ≤ 0.2V	2.0	-	5.5	V
Data Retention Current	I_{DR}	Vcc = 2.0V, $\overline{CS1} \geq V_{CC}$ - 0.2V or CS2 ≤ 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.1	mA
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

* **NOTE** : L-Ver only.

DATA RETENTION WAVE FORM 1 ($\overline{CS1}$ Controlled)



DATA RETENTION WAVE FORM 2 (CS2 Controlled)



64K x 16 Bit High-Speed CMOS Static RAM

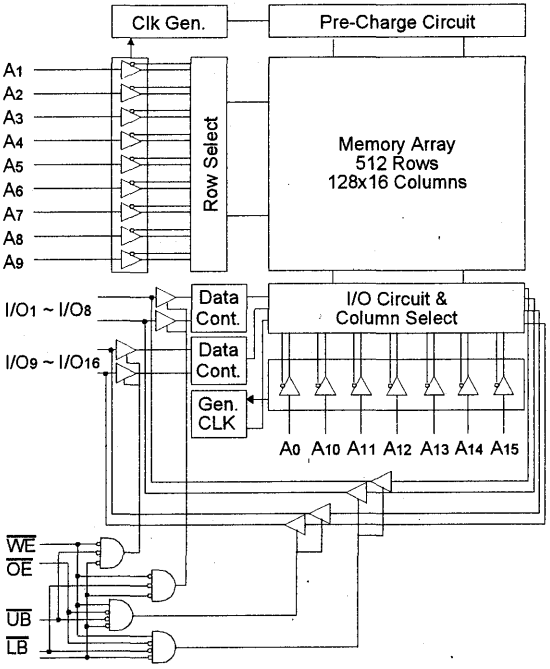
FEATURES

- Fast Access Time 8,10,12ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30mA(Max.)
  - (CMOS) : 10mA(Max.)
  - 1mA(Max.) - L-Ver. only
  - Operating KM6161002B/BL - 8 : 200mA(Max.)
  - KM6161002B/BL - 10 : 190mA(Max.)
  - KM6161002B/BL - 12 : 180mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O1~ I/O8, $\overline{UB}$: I/O9~ I/O16
- Standard Pin Configuration
  - KM6161002B/BLJ : 44-SOJ-400
  - KM6161002B/BLT: 44-TSOP2-400F

ORDERING INFORMATION

KM6161002B/BL -8/1012	Commercial Temp.
KM6161002BI/BLI -8/10/12	Industrial Temp.

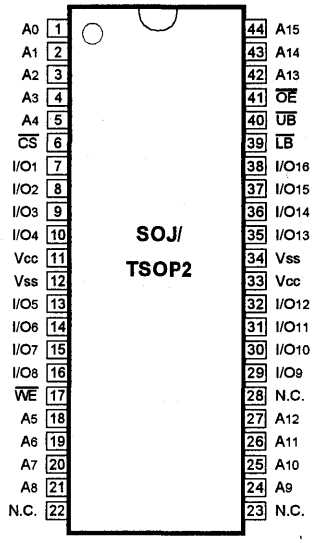
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM6161002B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The KM6161002B/BL uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6161002B/BL is packaged in a 400mil 44-pin plastic SOJ or TSOP2 forward.

PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤6ns) for I ≤ 20mA

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width≤6ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, V_{CC}= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to V_{CC}		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	8ns	-	200	mA
			10ns	-	190	
			12ns	-	180	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	30	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ V_{CC}-0.2V, V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V	Normal	-	10	mA
			L-Ver.	-	1	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{CC}=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

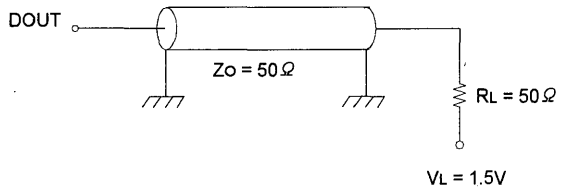
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

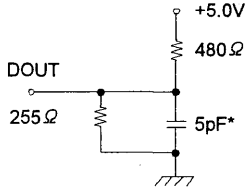
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6161002B/BL-8		KM6161002B/BL-10		KM6161002B/BL-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

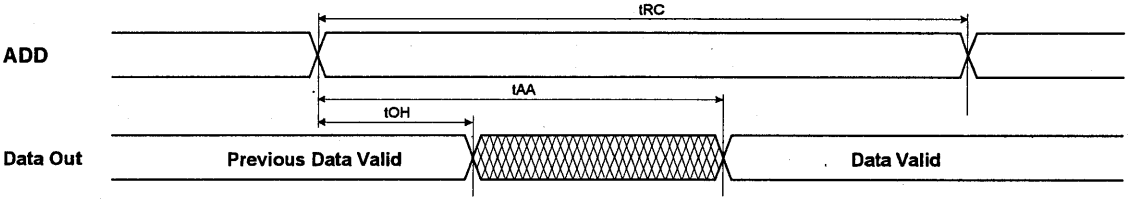
WRITE CYCLE

Parameter	Symbol	KM6161002B/BL-8		KM6161002B/BL-10		KM6161002B/BL-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	8	-	10	-	12	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	6	-	7	-	8	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

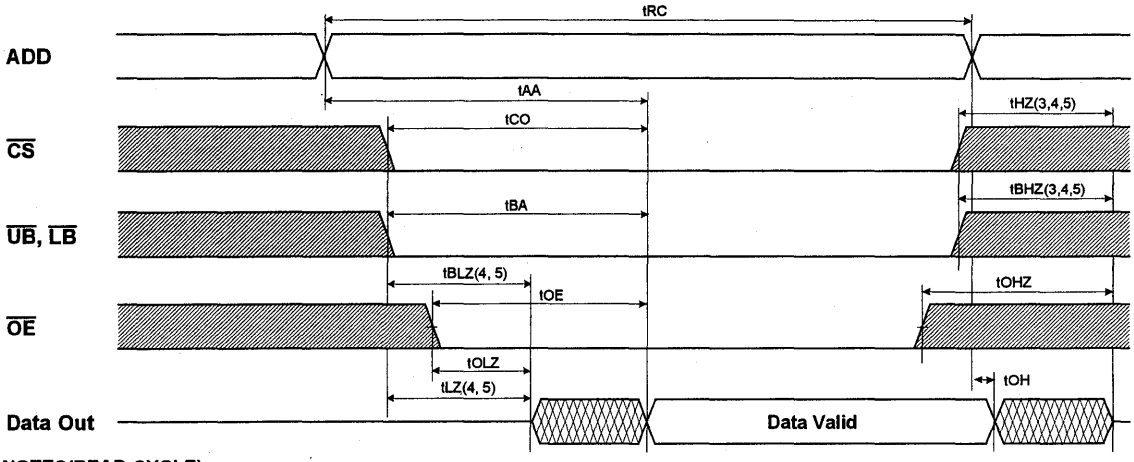
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$\overline{UB}$=$\overline{LB}$=VIL, $\overline{WE}$=VIH)



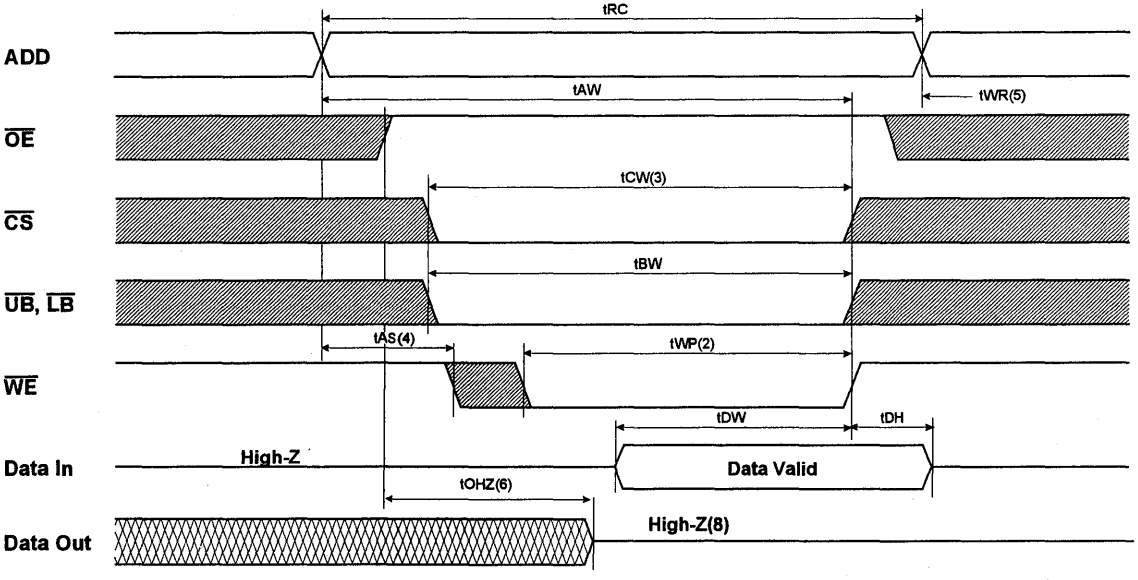
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

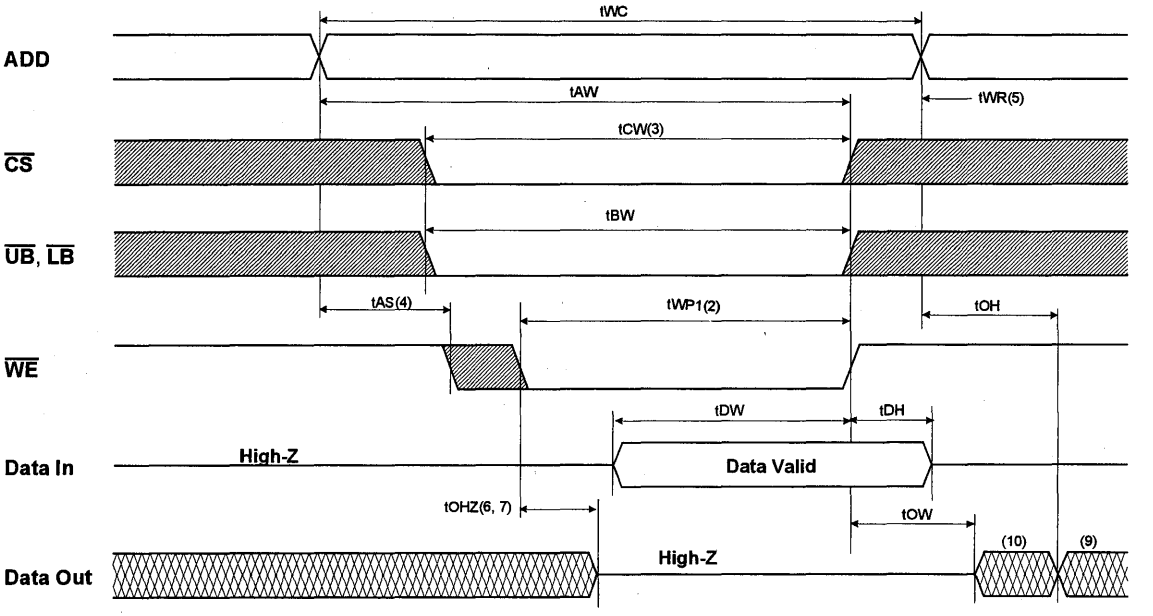
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

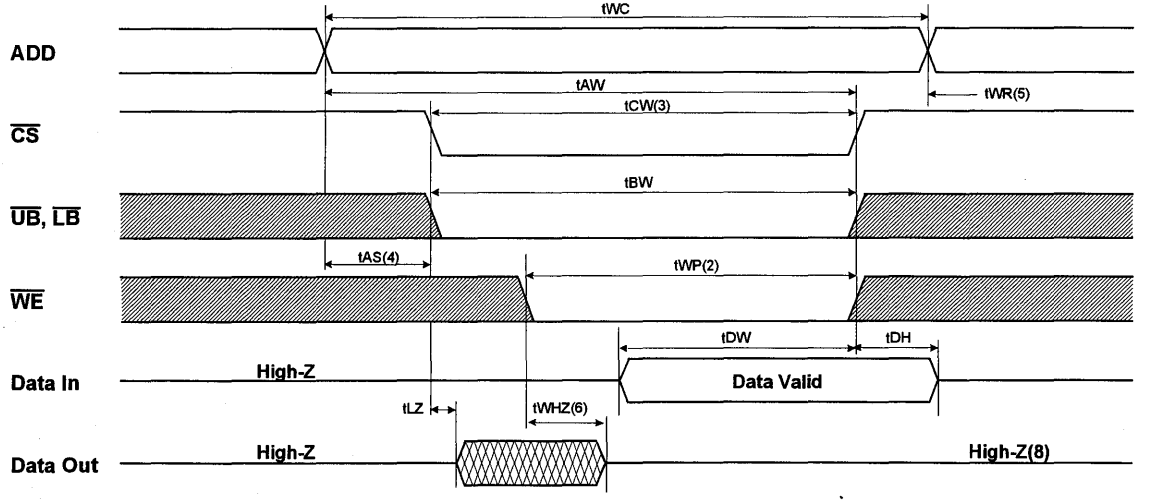


SAMSUNG ELECTRONICS

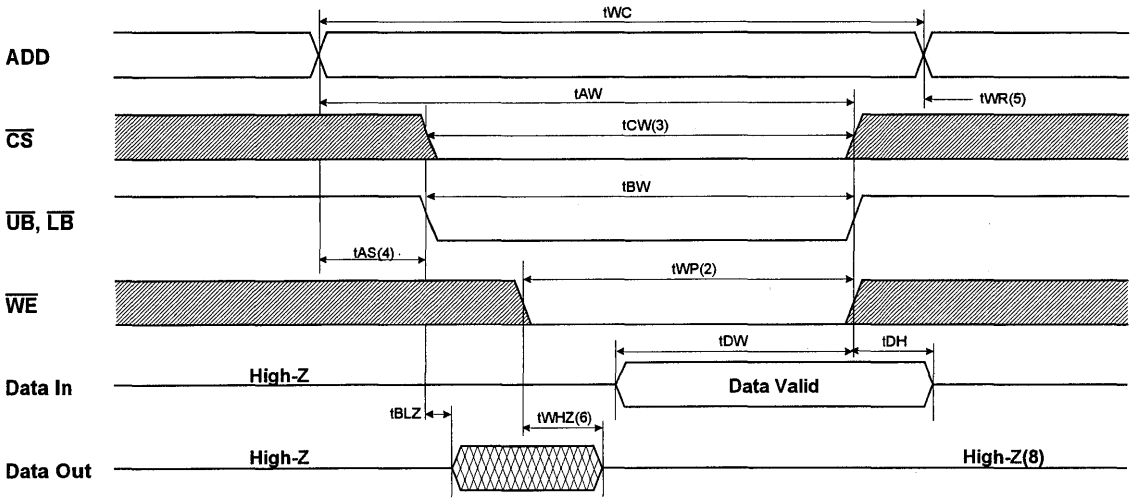
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$. $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z		ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	ICC
L	X	X	H	H				
L	H	L	L	H	Read	DOUT	High-Z	ICC
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	ICC
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

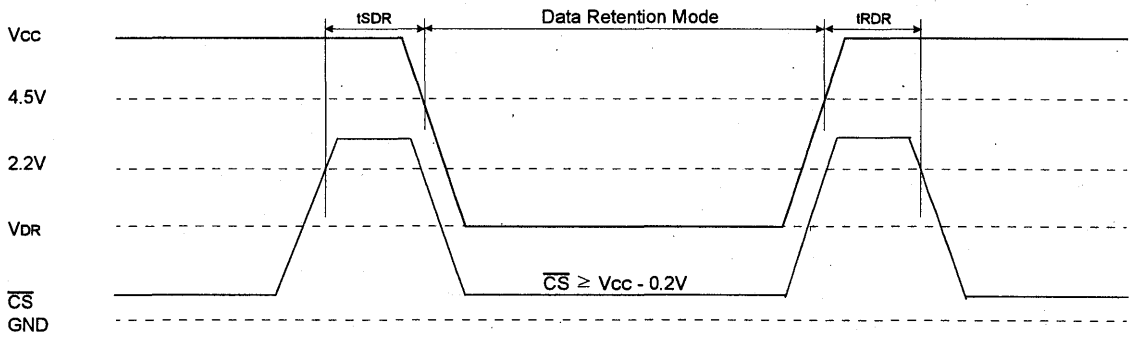
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.9	mA
		V_{CC} = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.7	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



64K x 16 Bit High-Speed CMOS Static RAM

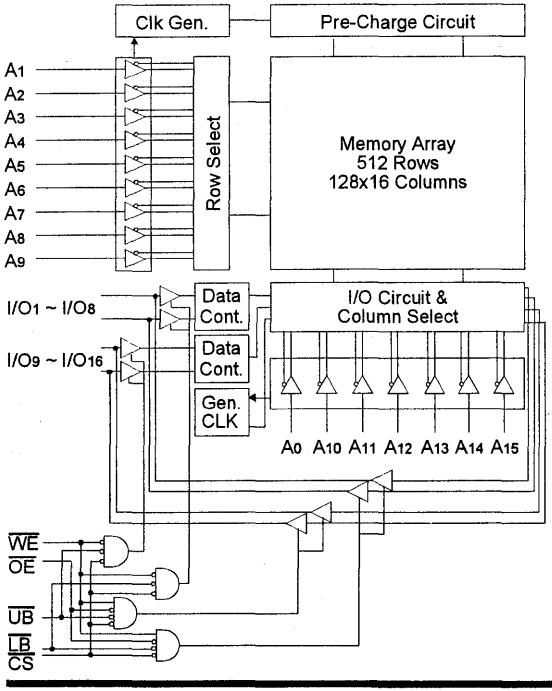
FEATURES

- Fast Access Time 12, 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 25mA(Max.)
  - (CMOS) : 8mA(Max.)
  - Operating KM6161002A - 12 : 190mA(Max.)
  - KM6161002A - 15 : 185mA(Max.)
  - KM6161002A - 17 : 185mA(Max.)
  - KM6161002A - 20 : 180mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O1~ I/O8, $\overline{UB}$: I/O9~ I/O16
- Standard Pin Configuration
  - KM6161002AJ : 44-SOJ-400
  - KM6161002AT: 44-TSOP2-400F

ORDERING INFORMATION

KM6161002A -12/15/17/20	Commercial Temp.
KM6161002AI -12/15/17/20	Industrial Temp.

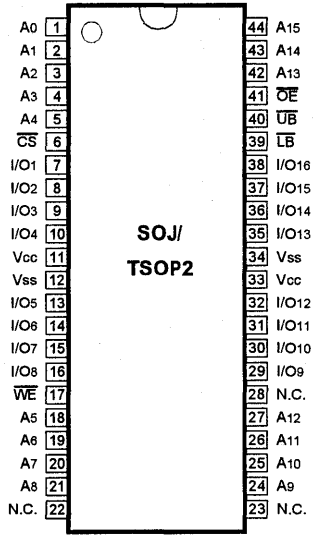
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM6161002A is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The KM6161002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6161002A is packaged in a 400mil 44-pin plastic SOJ or TSOP2 forward.

PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	190	mA
			15ns	-	185	
			17ns	-	185	
			20ns	-	180	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	25	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	8	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* Vcc=5.0V ± 5% Temp = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

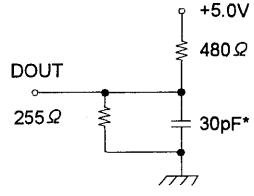
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

TEST CONDITIONS

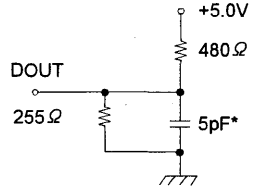
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6161002A-12		KM6161002A-15		KM6161002A-17		KM6161002A-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	17	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	8	-	9	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	6	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	0	9	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

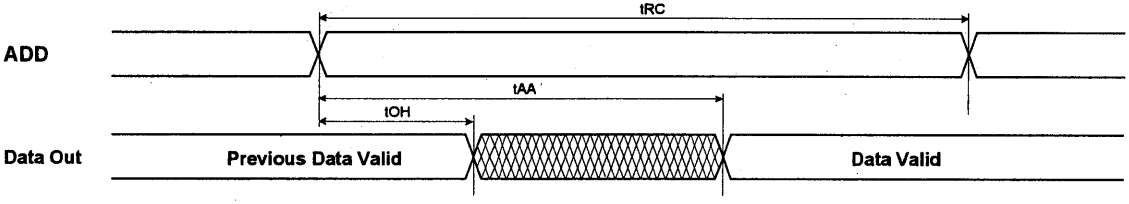
WRITE CYCLE

Parameter	Symbol	KM6161002A-12		KM6161002A-15		KM6161002A-17		KM6161002A-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	12	-	15	-	17	-	20	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	8	-	10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

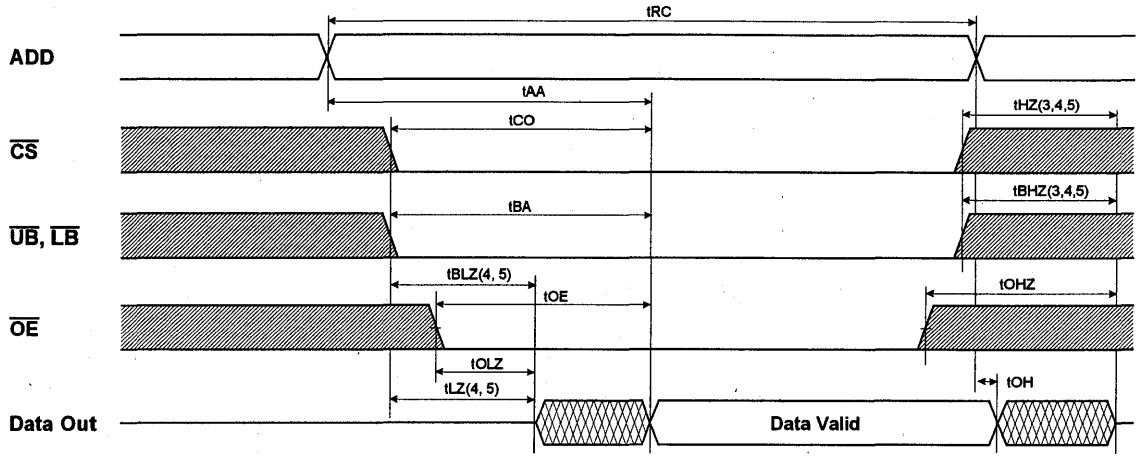
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$\overline{UB}$=$\overline{LB}$=VIL, $\overline{WE}$=VIH)



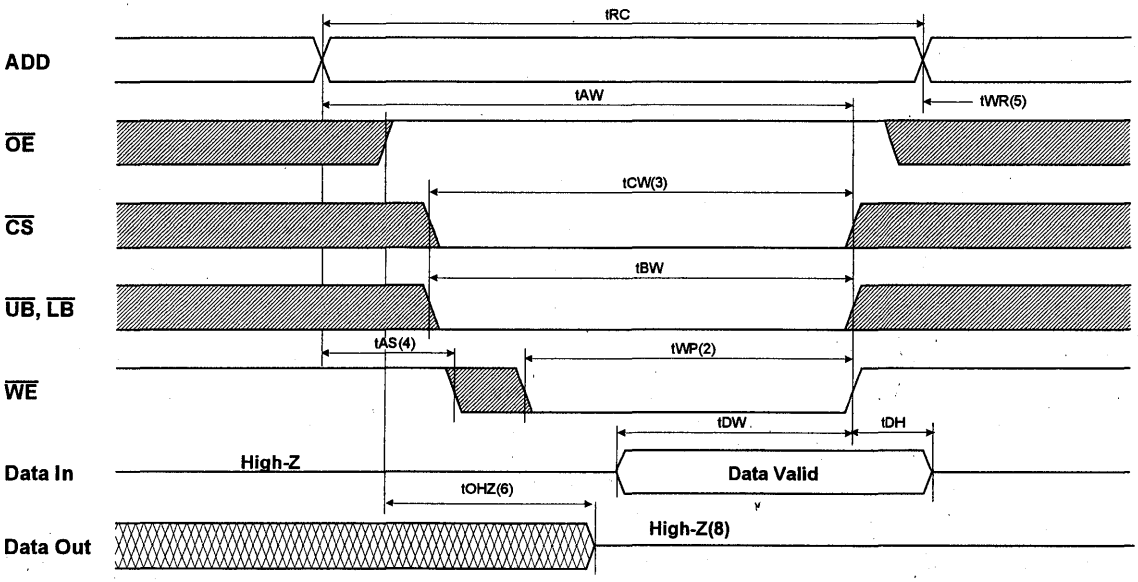
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

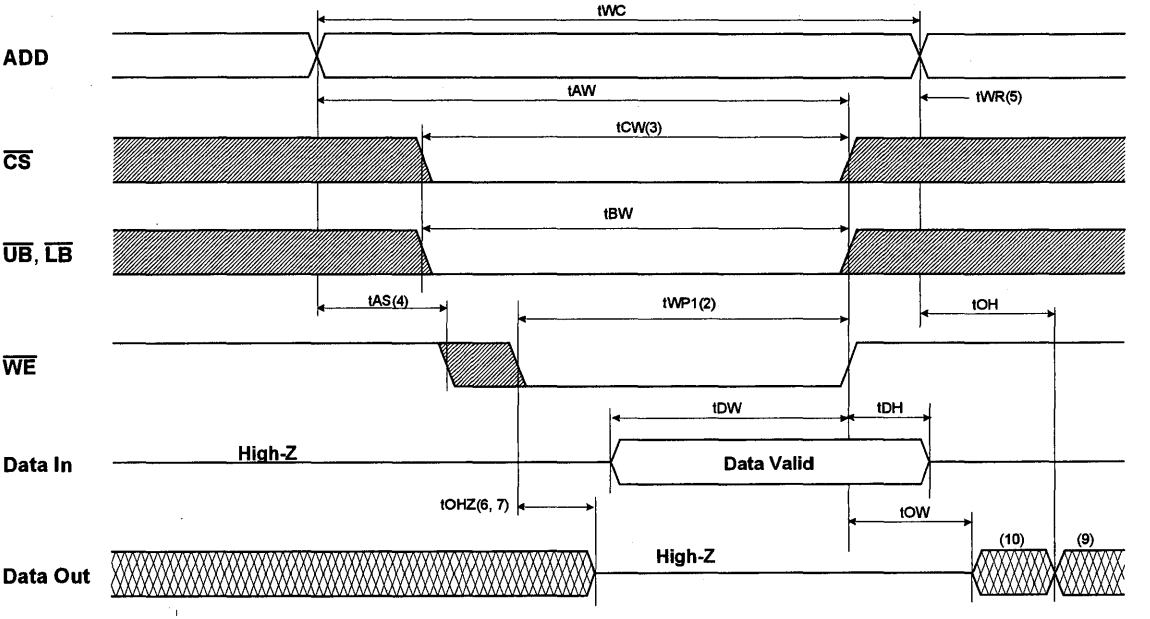
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

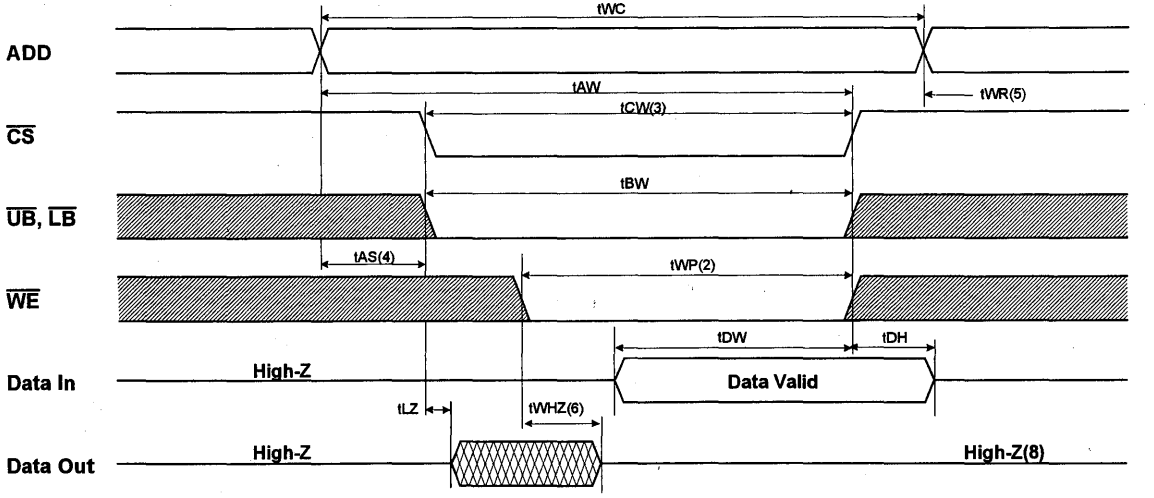


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)

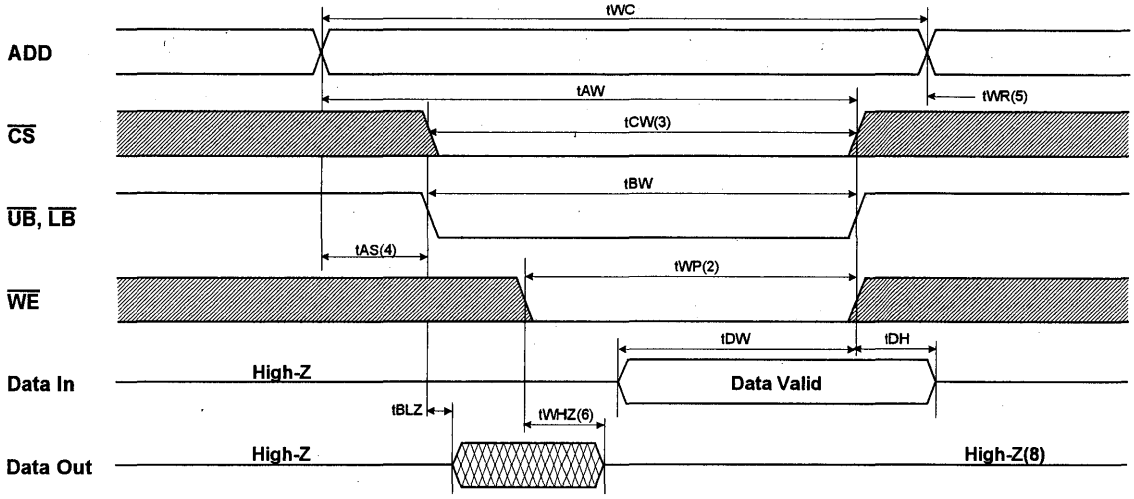


TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$. $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z		I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

* **NOTE** : X means Don't Care.

SAMSUNG ELECTRONICS

64K x 16 Bit High-Speed CMOS Static RAM

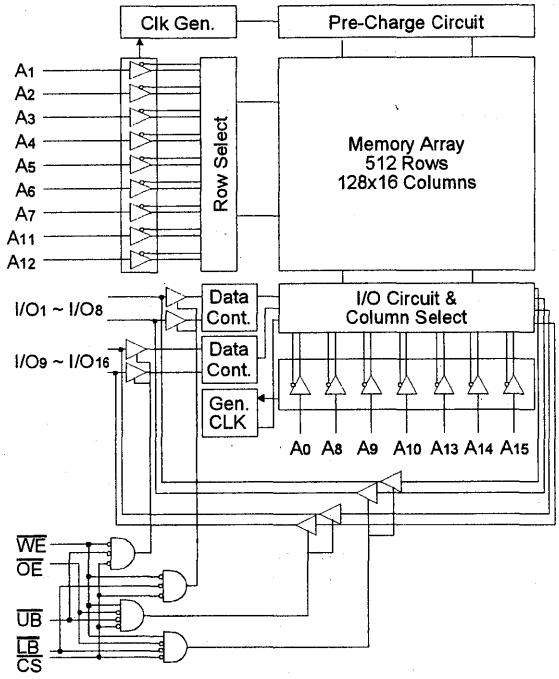
FEATURES

- Fast Access Time 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM6161002 - 15 : 230mA(Max.)
  - KM6161002 - 17 : 220mA(Max.)
  - KM6161002 - 20 : 210mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O1~ I/O8, $\overline{UB}$: I/O9~ I/O16
- Standard Pin Configuration
  - KM6161002J : 44-SOJ-400

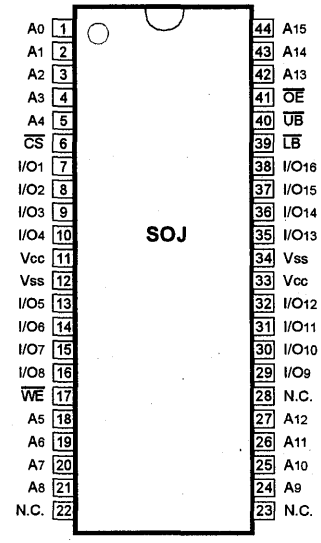
GENERAL DESCRIPTION

The KM6161002 is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The KM6161002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6161002 is packaged in a 400mil 44-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20㎃

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20㎃

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, V_{CC}= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	㎂
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	㎂
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	230	mA
			17ns	-	220	
			20ns	-	210	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

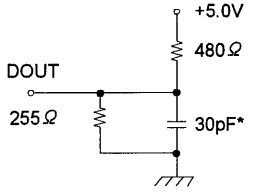
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

TEST CONDITIONS

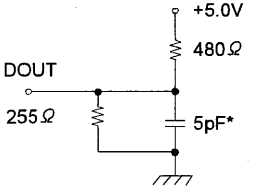
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6161002-15		KM6161002-17		KM6161002-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	9	-	10	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	8	-	9	-	20	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	6	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	4	-	ns

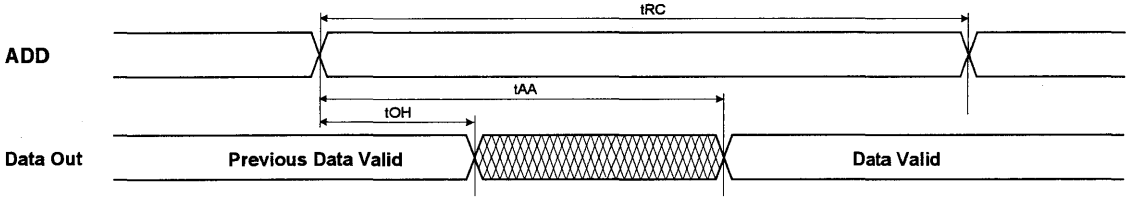
WRITE CYCLE

Parameter	Symbol	KM6161002-15		KM6161002-17		KM6161002-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	12	-	13	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

2

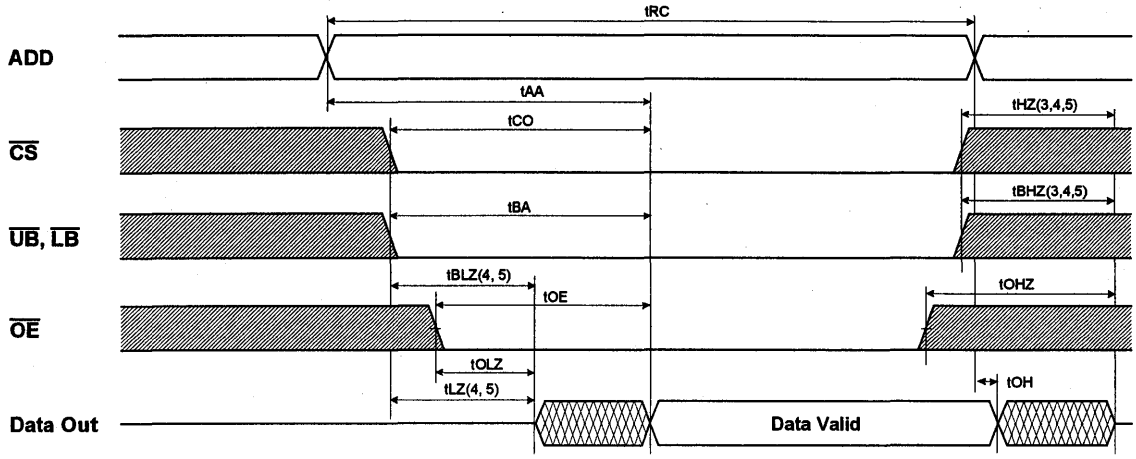
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$\overline{UB}$=$\overline{LB}$=V_{IL}, $\overline{WE}$=V_{IH})



SAMSUNG ELECTRONICS

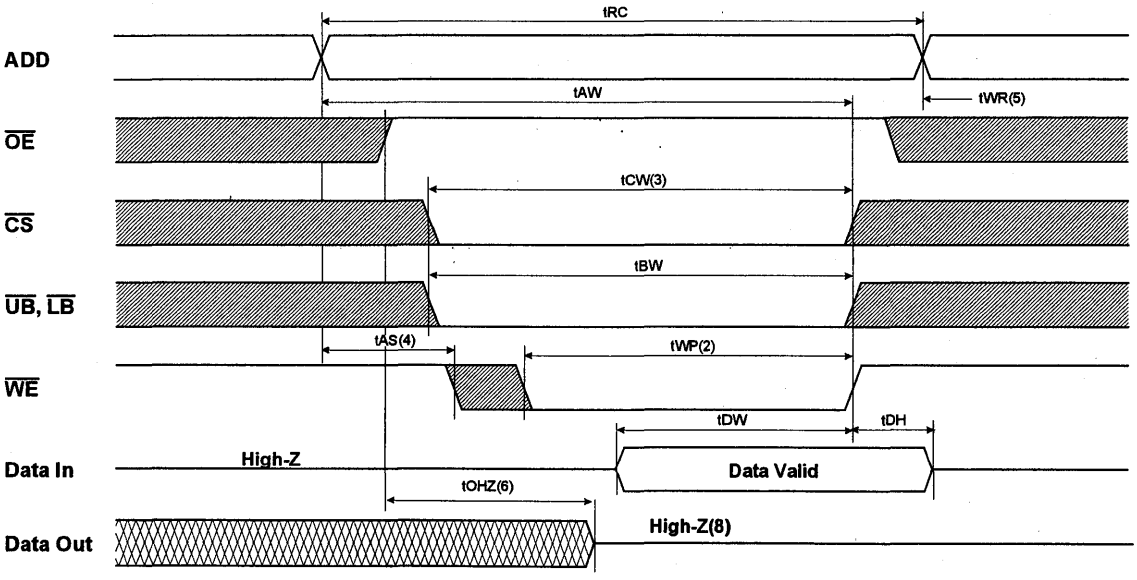
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



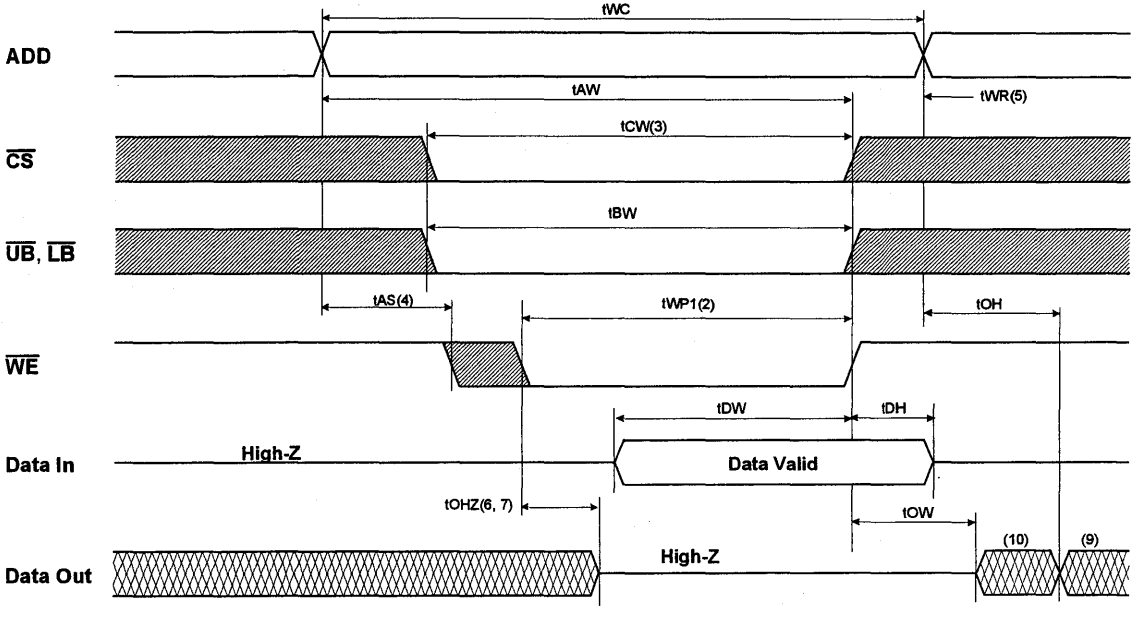
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

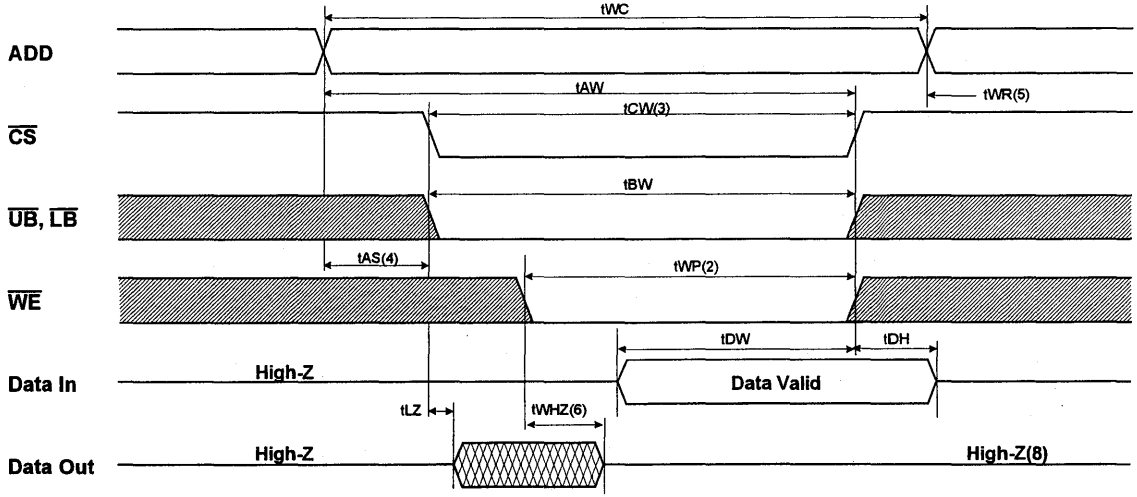
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



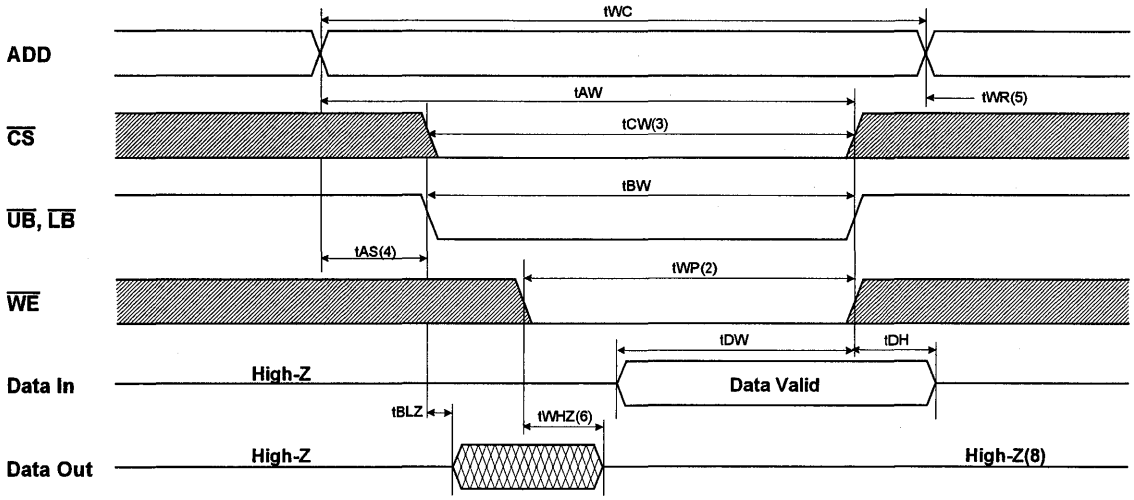
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$. $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z	-	ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	ICC
L	X	X	H	H				
L	H	L	L	H	Read	DOUT	High-Z	ICC
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	ICC
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

* **NOTE** : X means Don't Care.

4M High Speed SRAM (5.0V Operation)

1M x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM644002B - 10 : 190mA(Max.)
  - KM644002B - 12 : 180mA(Max.)
  - KM644002B - 15 : 170mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM644002BJ : 32-SOJ-400
  - KM644002BT : 32-TSOP2-400F

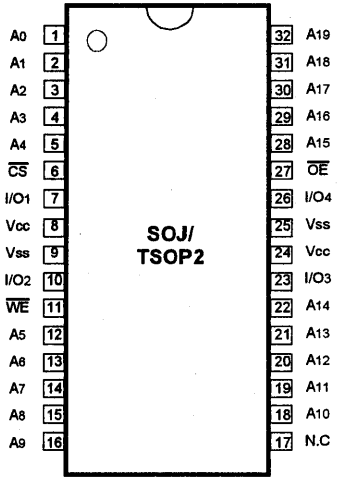
GENERAL DESCRIPTION

The KM644002B is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM644002B uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM644002B is packaged in a 400 mil 32-pin plastic SOJ or TSOP(II) forward.

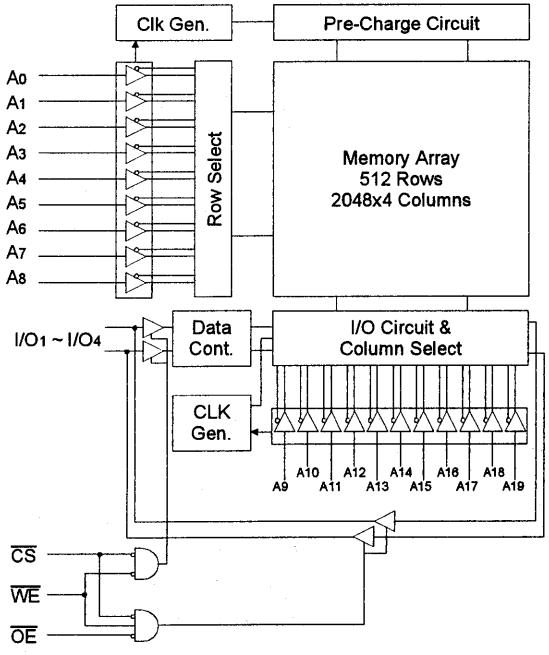
ORDERING INFORMATION

KM644002B -10/12/15	Commercial Temp.
KM644002BI -10/12/15	Industrial Temp.

PIN CONFIGURATION*(Top View)*



FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤8ns) for I ≤ 20㎃

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤8ns) for I ≤ 20㎃

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	㎂
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	㎂
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	10ns	-	190	㎃
			12ns	-	180	
			15ns	-	170	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	㎃
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	㎃
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* Vcc=5.0V ± 10% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

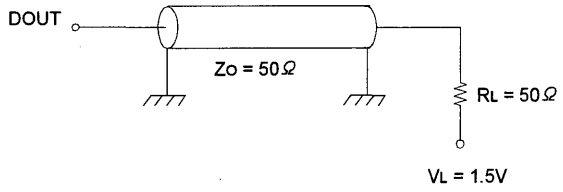
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

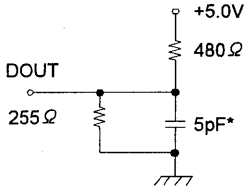
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

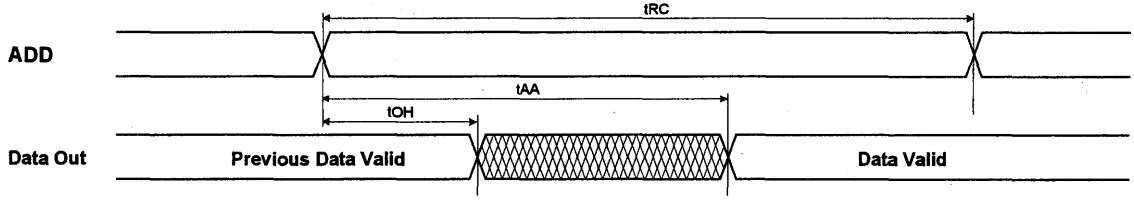
Parameter	Symbol	KM644002B-10		KM644002B-12		KM644002B-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	10	-	12	-	15	ns

WRITE CYCLE

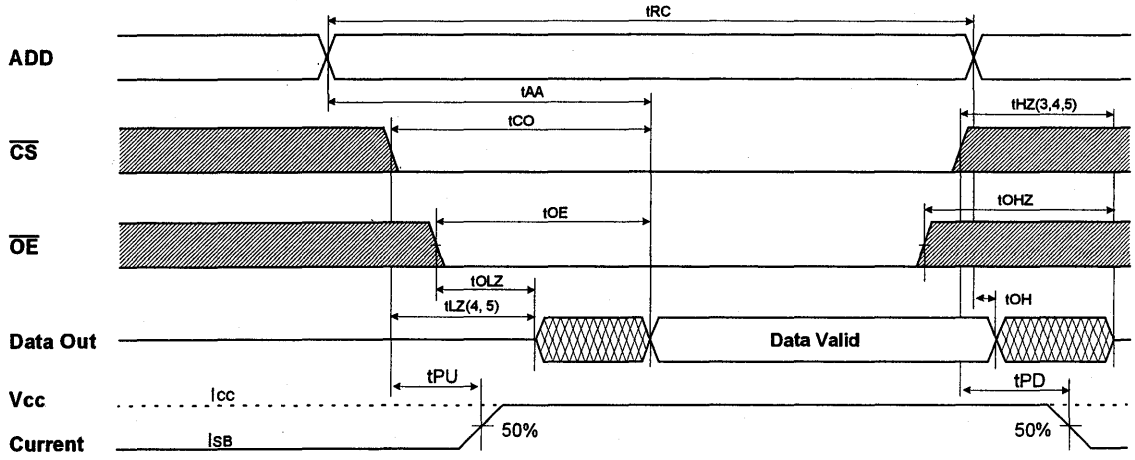
Parameter	Symbol	KM644002B-10		KM644002B-12		KM644002B-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	10	-	12	-	15	-	ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	10	-	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	5	0	6	0	7	ns
Data to Write Time Overlap	tDW	5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



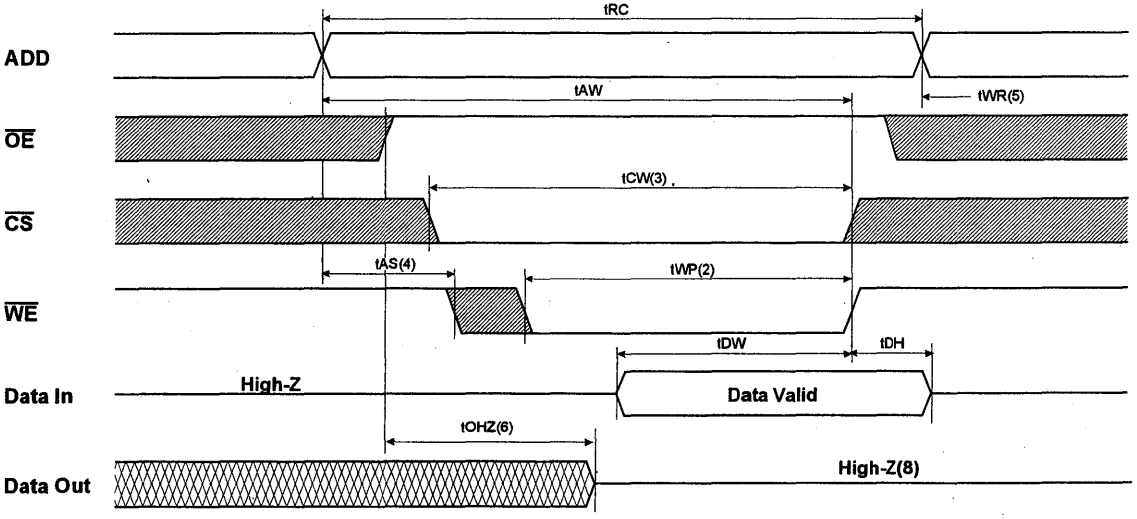
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



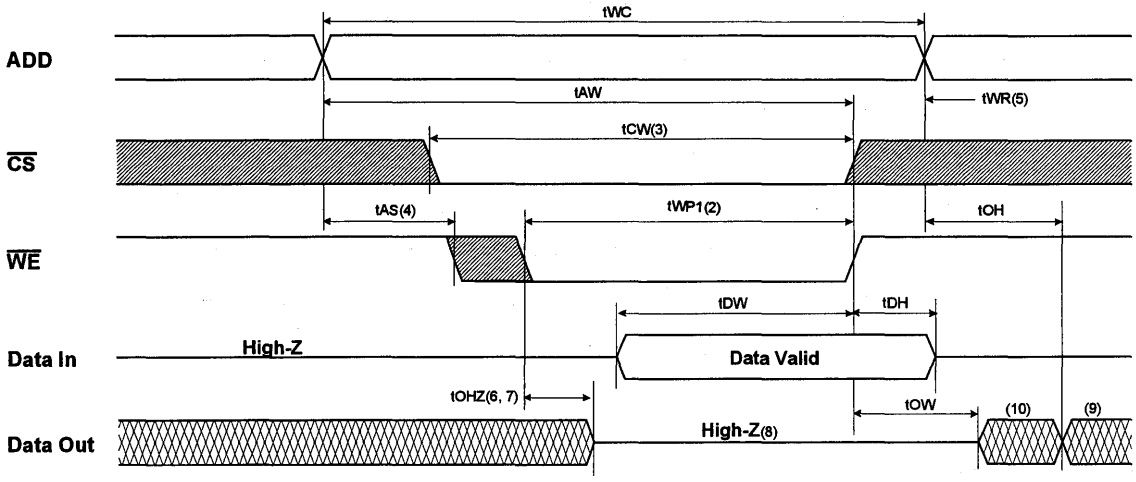
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200㎷ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

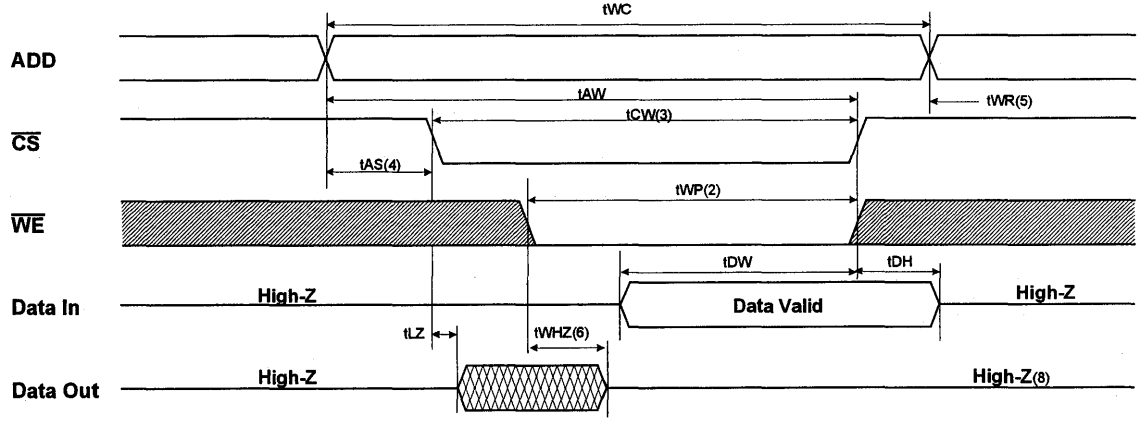
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

1M x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM

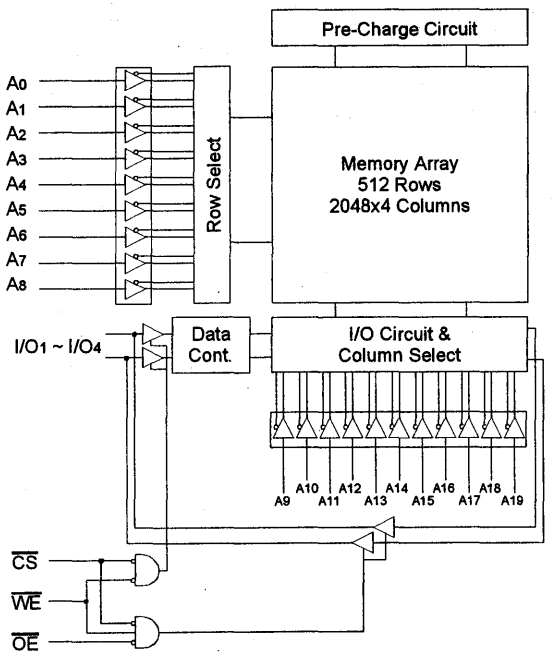
FEATURES

- Fast Access Time 12,13,15ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60mA(Max.)
  - (CMOS) : 30mA(Max.)
  - Operating KM64B4002 - 12 : 185mA(Max.)
  - KM64B4002 - 13 : 185mA(Max.)
  - KM64B4002 - 15 : 180mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM64B4002J : 32-SOJ-400

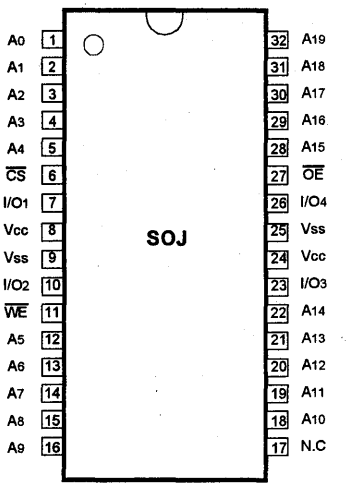
GENERAL DESCRIPTION

The KM64B4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM64B4002 uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64B4002 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20㎃

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20㎃

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	㎂
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-10	10	㎂
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	185	mA
			13ns	-	185	
			15ns	-	180	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	60	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	30	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

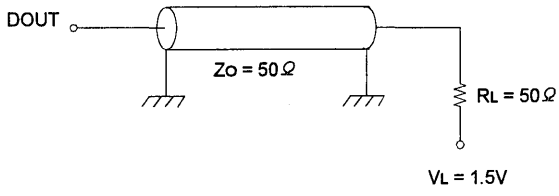
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

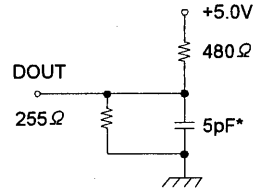
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

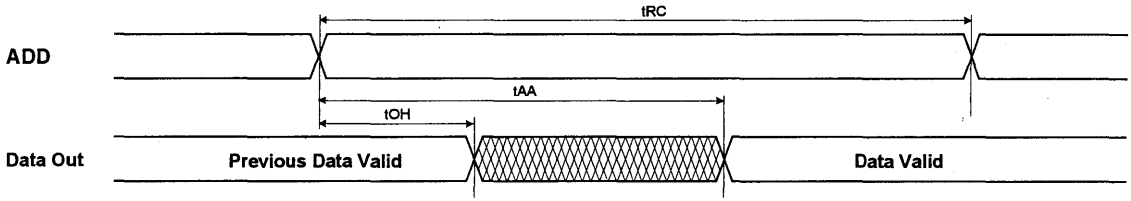
Parameter	Symbol	KM64B4002-12		KM64B4002-13		KM64B4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	6	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

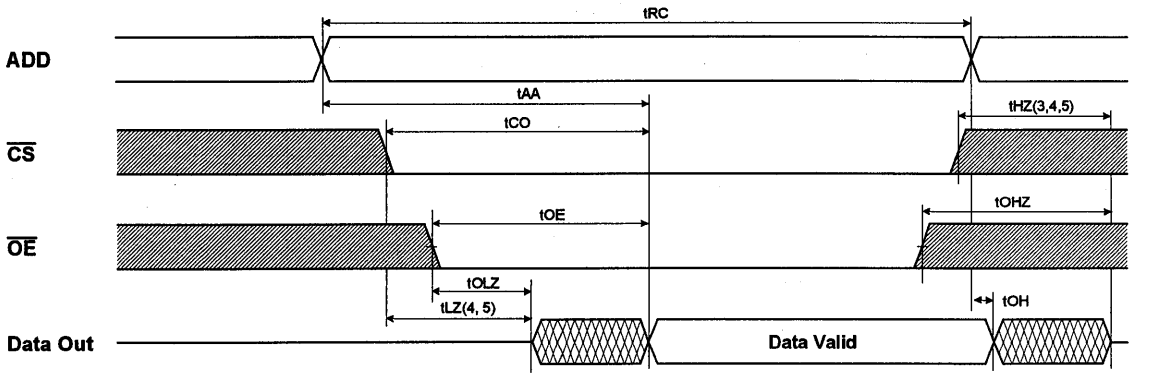
Parameter	Symbol	KM64B4002-12		KM64B4002-13		KM64B4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	13	-	15	-	ns
Chip Select to End of Write	tCW	8	-	9	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	9	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	9	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	6	0	7	ns
Data to Write Time Overlap	tDW	6	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



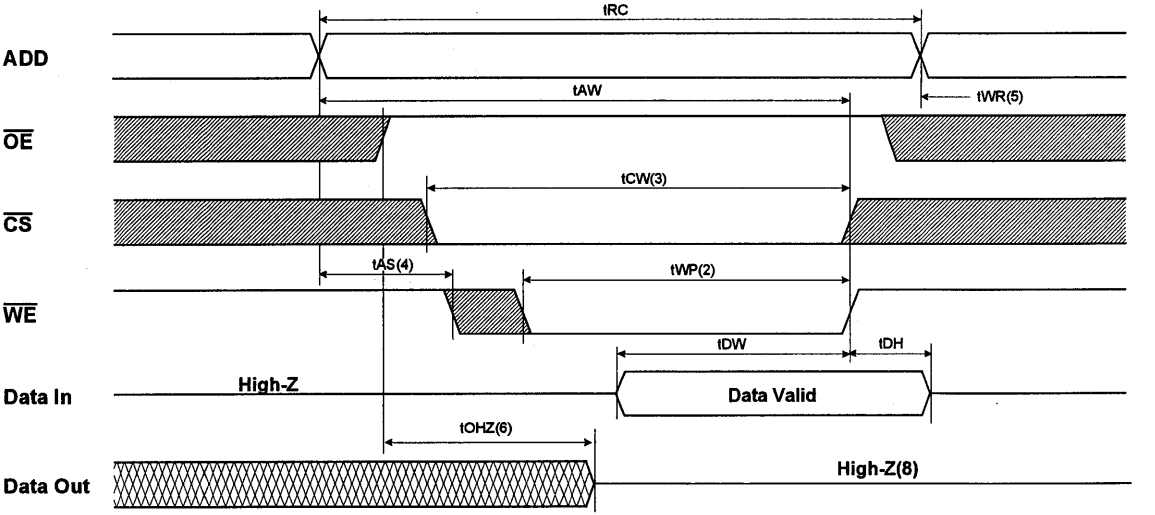
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



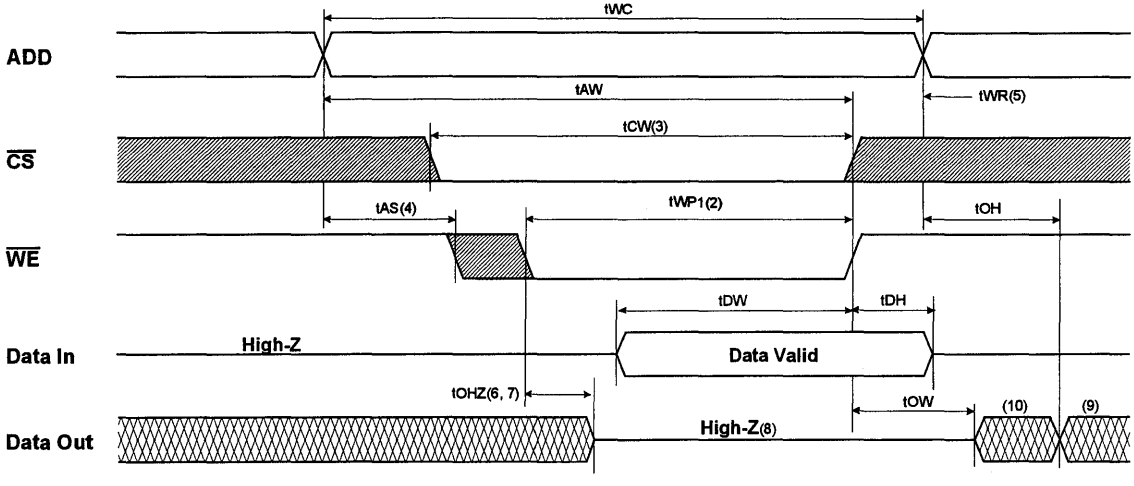
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

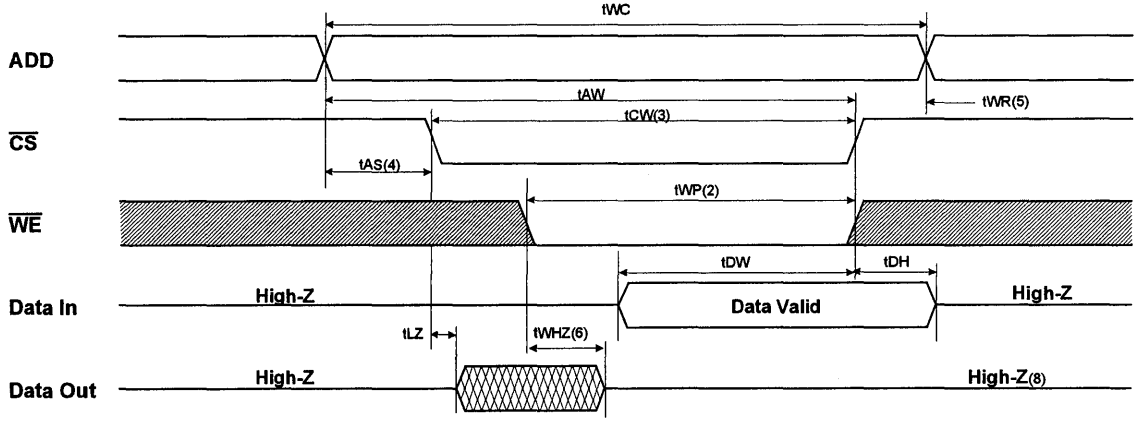
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

1M x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM

FEATURES

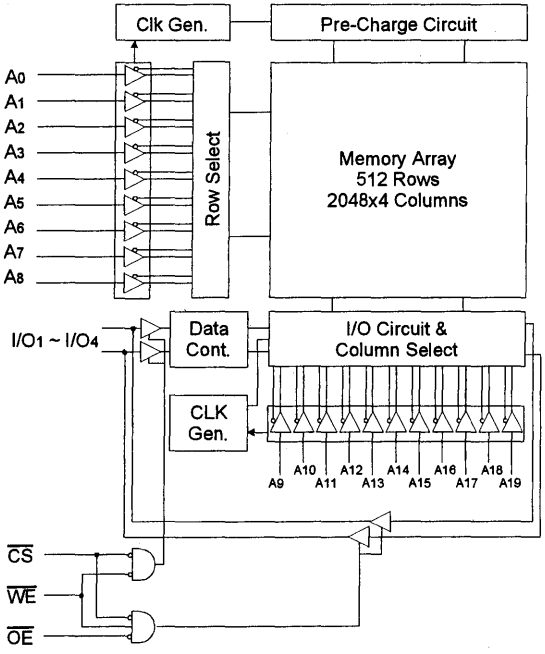
- Fast Access Time 15,17,20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM644002A - 15 : 150mA(Max.)
  - KM644002A - 17 : 145mA(Max.)
  - KM644002A - 20 : 140mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM644002AJ : 32-SOJ-400

GENERAL DESCRIPTION

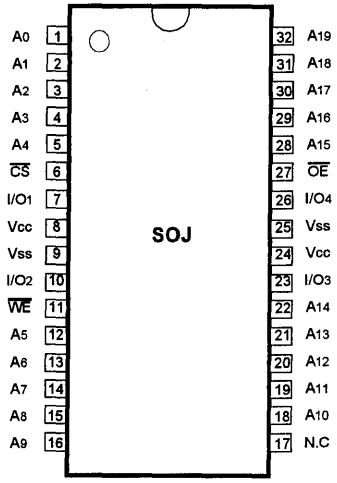
The KM644002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM644002A uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM644002A is packaged in a 400 mil 32-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	150	mA
			17ns	-	145	
			20ns	-	140	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	50	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

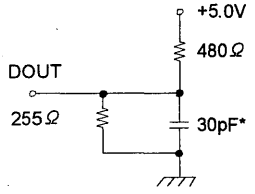
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

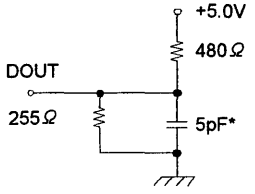
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

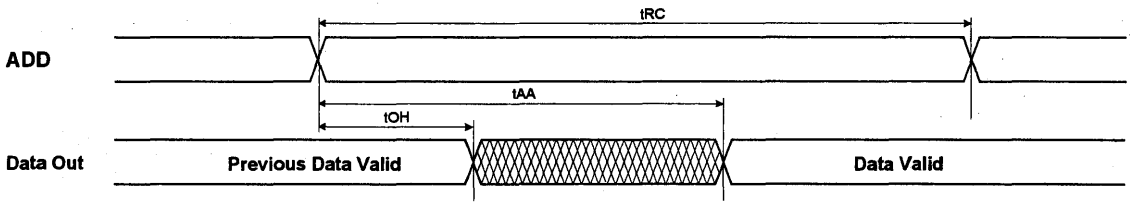
Parameter	Symbol	KM644002A-15		KM644002A-17		KM644002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

WRITE CYCLE

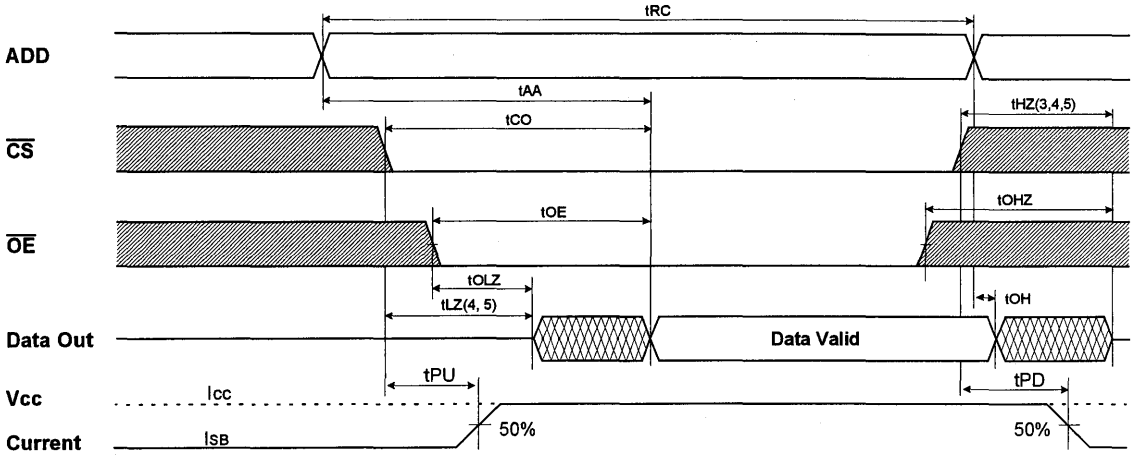
Parameter	Symbol	KM644002A-15		KM644002A-17		KM644002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



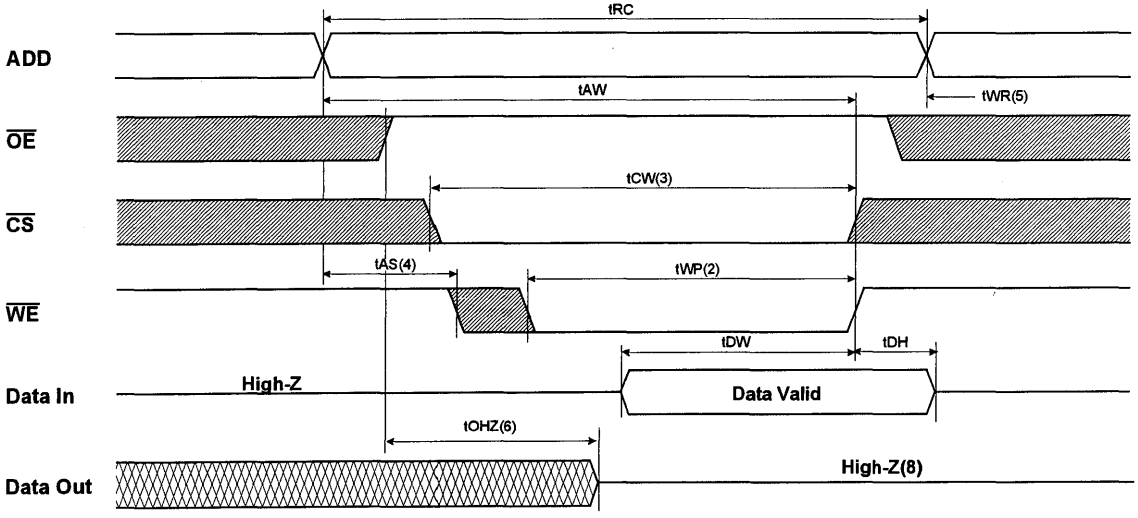
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

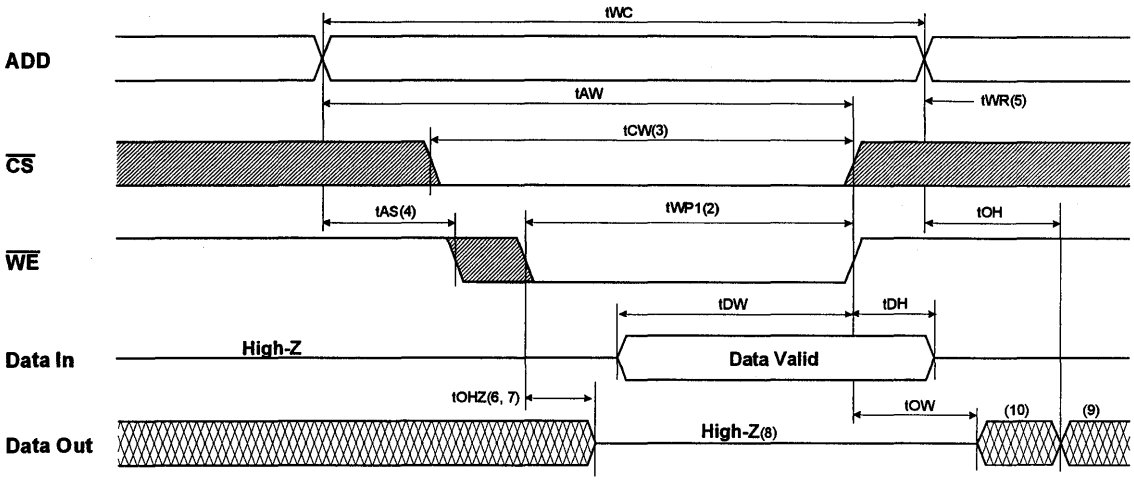
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

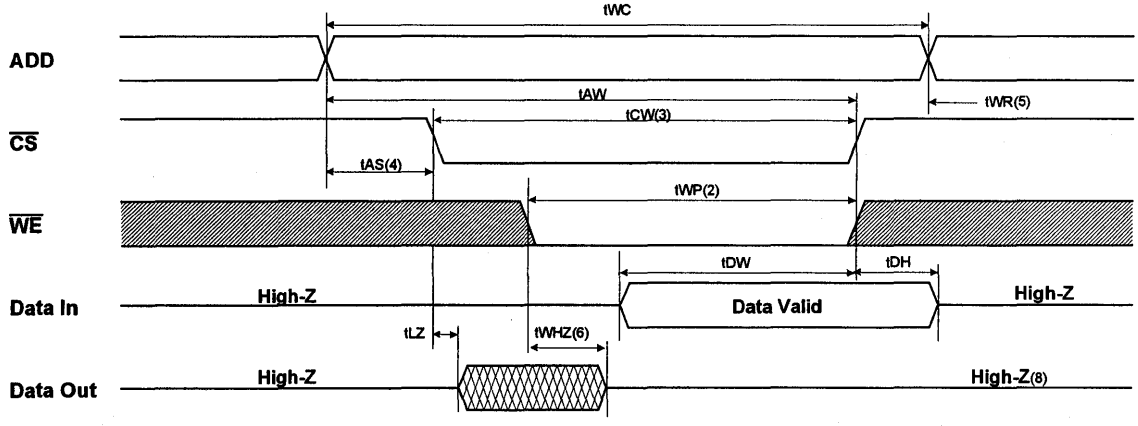


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



SAMSUNG ELECTRONICS

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

1M x 4 Bit (with $\overline{OE}$) High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 17,20,25ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM644002 - 17 : 170mA(Max.)
  - KM644002 - 20 : 150mA(Max.)
  - KM644002 - 25 : 130mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM644002J : 32-SOJ-400

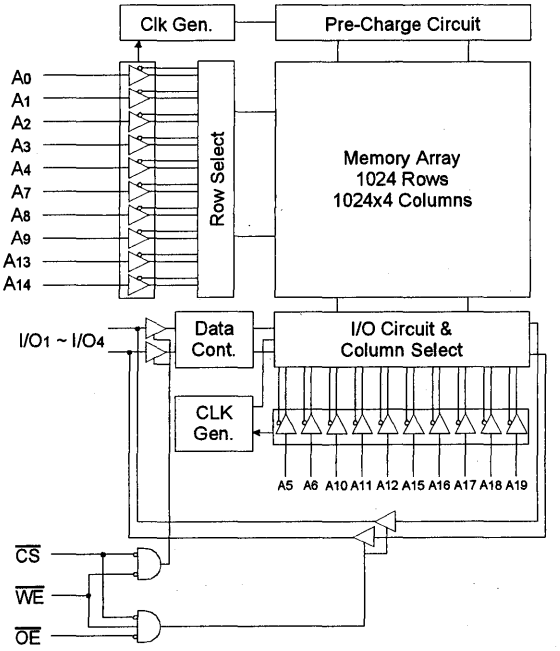
GENERAL DESCRIPTION

The KM644002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM644002 uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM644002 is packaged in a 400 mil 32-pin plastic SOJ.

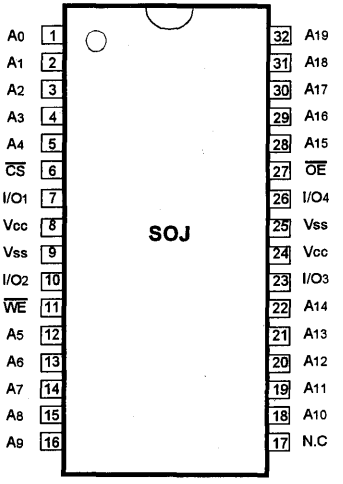
ORDERING INFORMATION

KM644002 -17/20/25	Commercial Temp.
KM644002E -17/20/25	Extended Temp.
KM644002I -17/20/25	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Extended	T_A	-25 to 85	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, V_{CC}= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	17ns	-	170	mA
			20ns	-	150	
			25ns	-	130	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	60	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

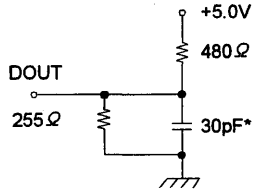
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

TEST CONDITIONS

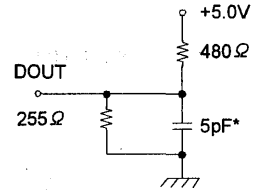
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at extended and industrial temperature ranges.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM644002-17		KM644002-20		KM644002-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	17	-	20	-	25	-	ns
Address Access Time	tAA	-	17	-	20	-	25	ns
Chip Select to Output	tCO	-	17	-	20	-	25	ns
Output Enable to Valid Output	tOE	-	8	-	10	-	12	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	10	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	10	ns
Output Hold from Address Change	tOH	3	-	4	-	5	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	17	-	20	-	25	ns

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

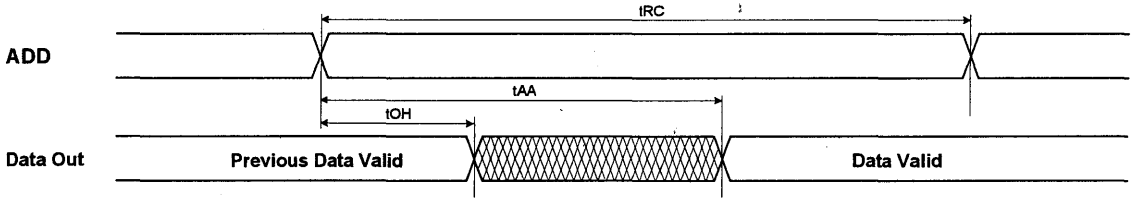
WRITE CYCLE

Parameter	Symbol	KM644002-17		KM644002-20		KM644002-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	17	-	20	-	25	-	ns
Chip Select to End of Write	tCW	12	-	13	-	15	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	15	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	12	-	13	-	15	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	17	-	20	-	25	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

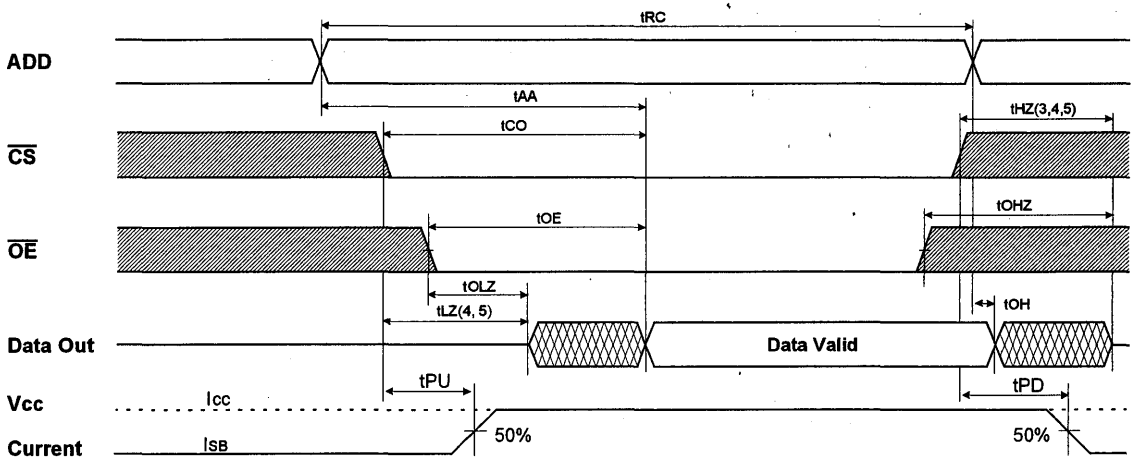
NOTE: Above parameters are also guaranteed at extended and industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



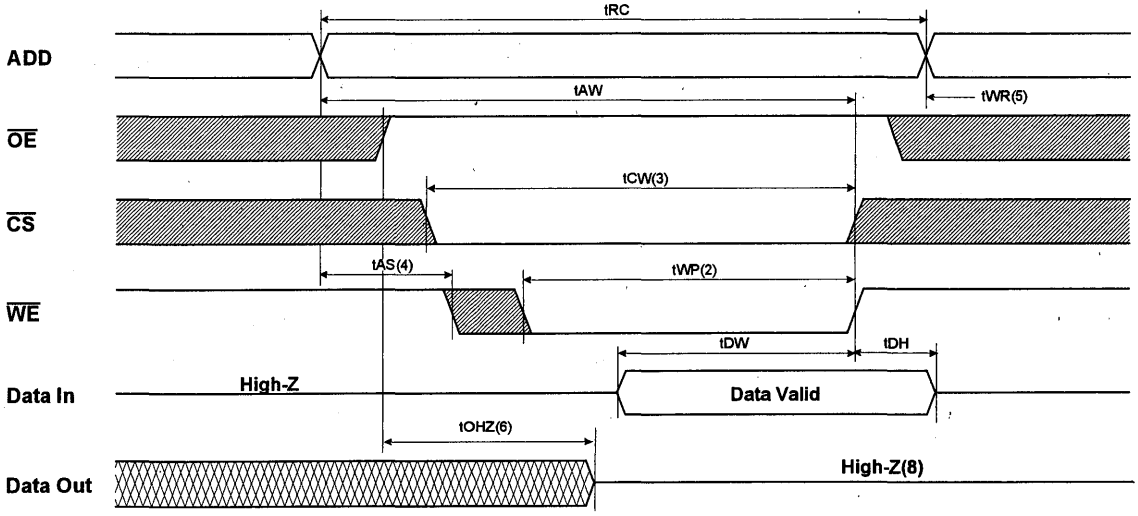
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



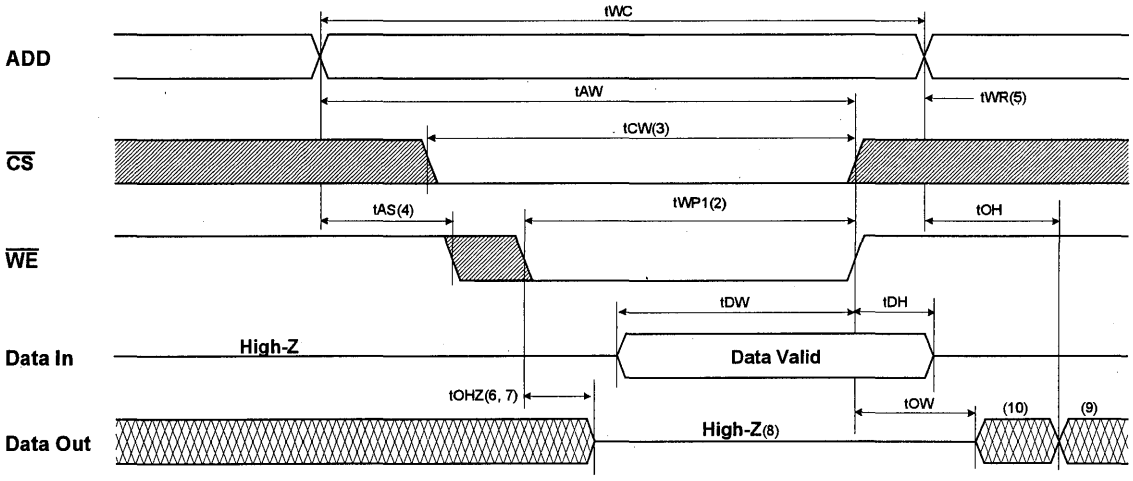
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

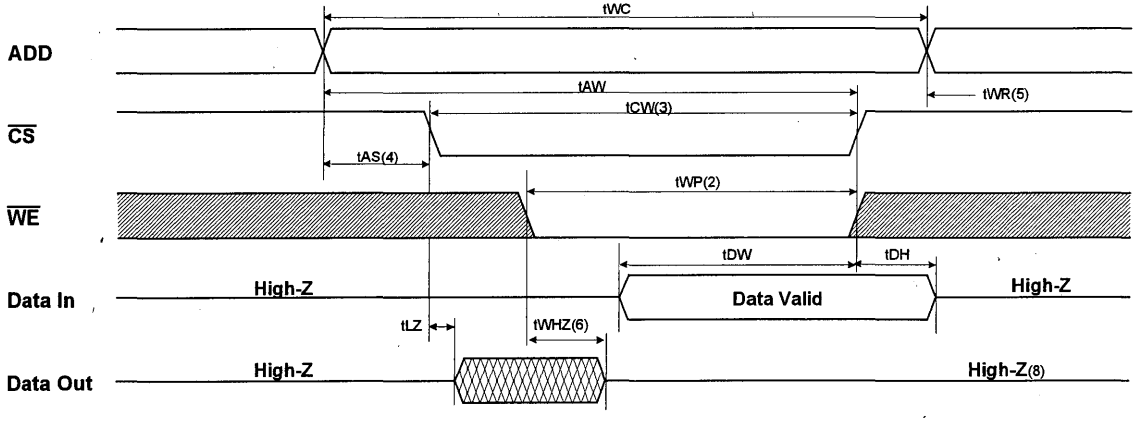
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



SAMSUNG ELECTRONICS

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

512K x 8 Bit High-Speed CMOS Static RAM

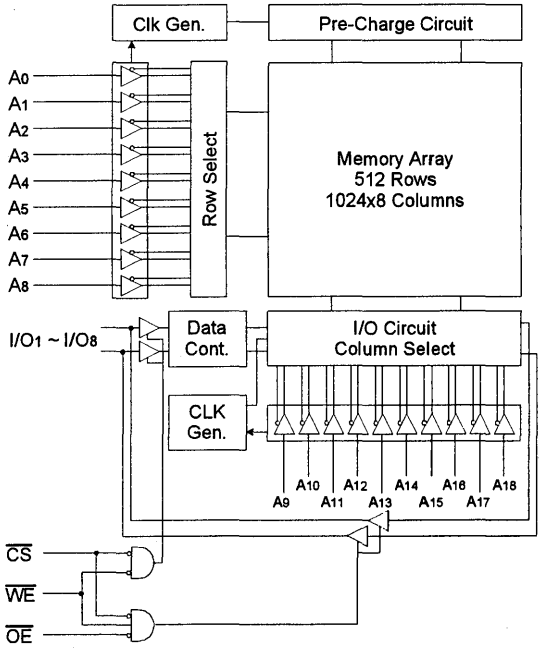
FEATURES

- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM684002B - 10 : 200mA(Max.)
  - KM684002B - 12 : 190mA(Max.)
  - KM684002B - 15 : 180mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM684002BJ : 36-SOJ-400
  - KM684002BT : 36-TSOP2-400F

ORDERING INFORMATION

KM684002B -10/12/15	Commercial Temp.
KM684002BI -10/12/15	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM

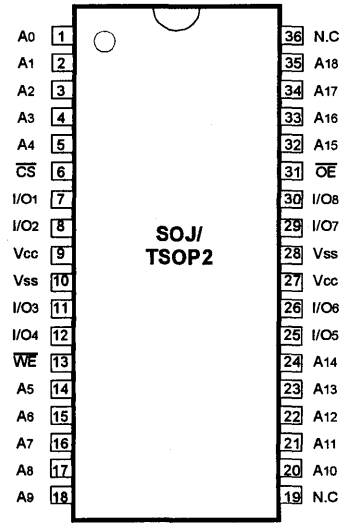


GENERAL DESCRIPTION

The KM684002B is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM684002B uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM684002B is packaged in a 400 mil 36-pin plastic SOJ or TSOP(II) forward.

2

PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤8ns) for I ≤ 20mA

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width≤8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, V_{CC}= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to V_{CC}		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	10ns	-	200	mA
			12ns	-	190	
			15ns	-	180	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ V_{CC}-0.2V, V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{CC}=5.0V ± 10% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

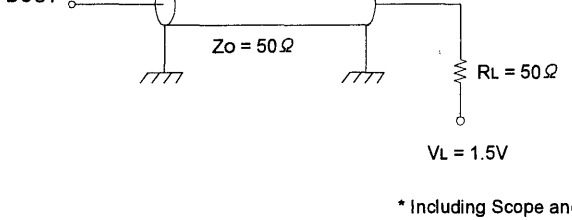
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

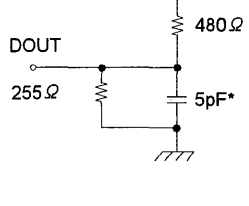
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

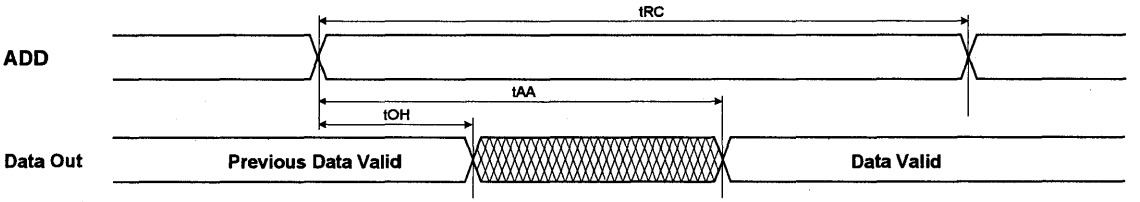
Parameter	Symbol	KM684002B-10		KM684002B-12		KM684002B-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	12	-	15	ns

WRITE CYCLE

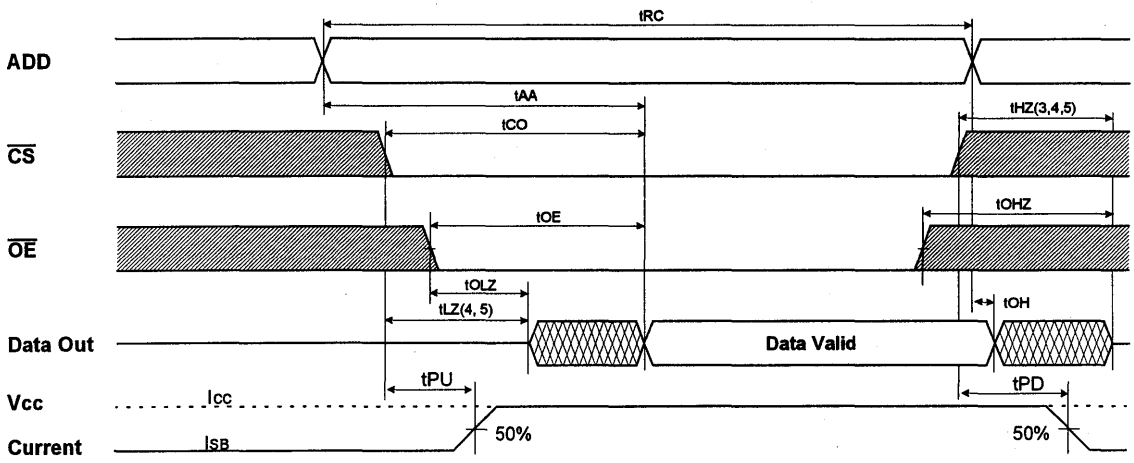
Parameter	Symbol	KM684002B-10		KM684002B-12		KM684002B-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	10	-	12	-	15	-	ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	10	-	12	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	5	0	6	0	7	ns
Data to Write Time Overlap	tDW	5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



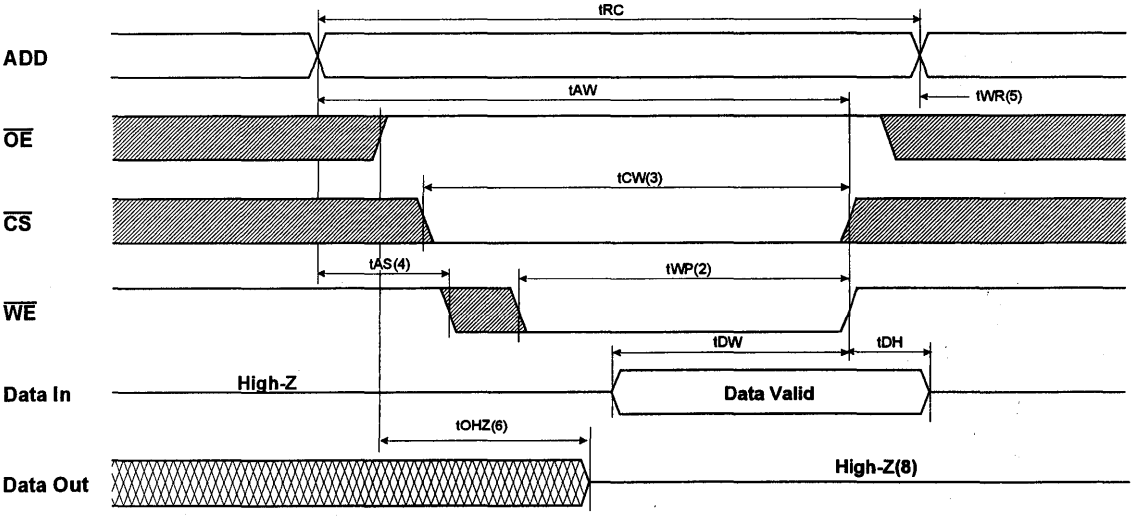
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

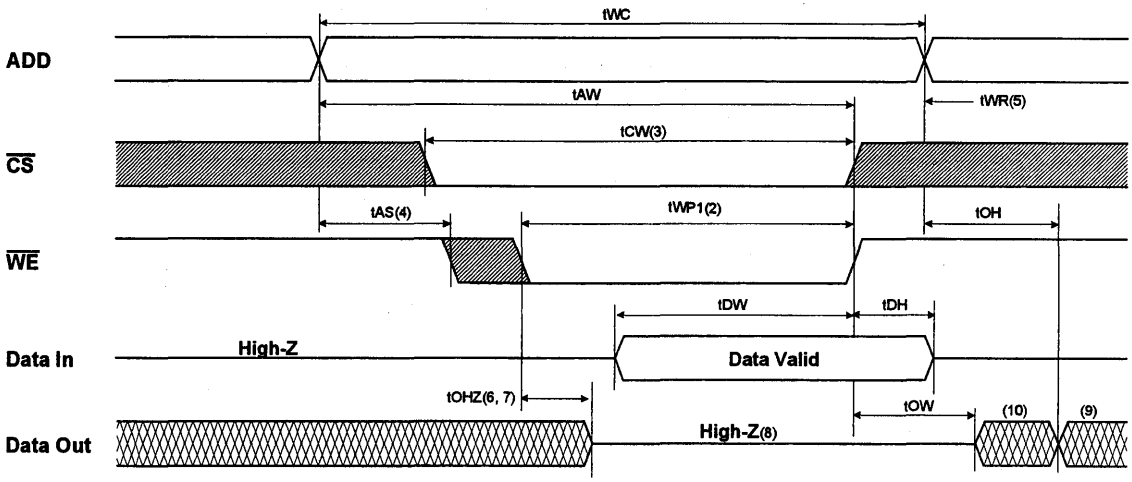
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

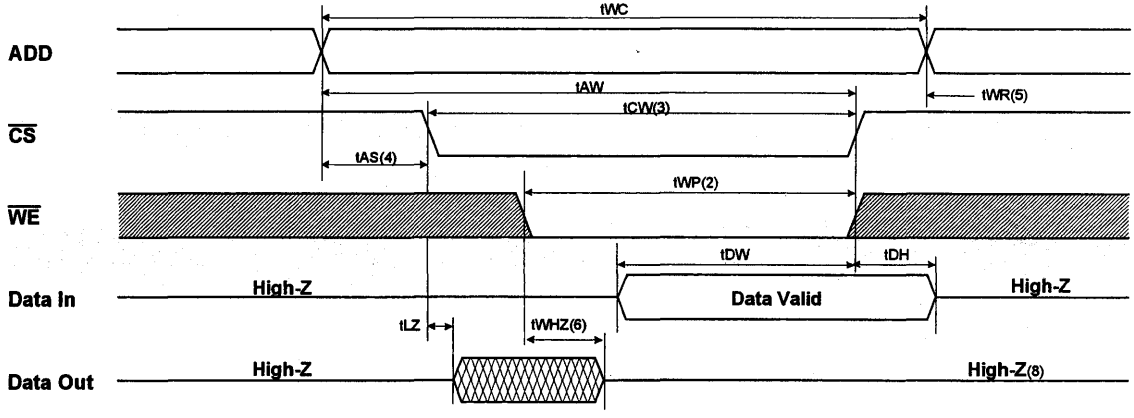


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

512K x 8 Bit High-Speed CMOS Static RAM

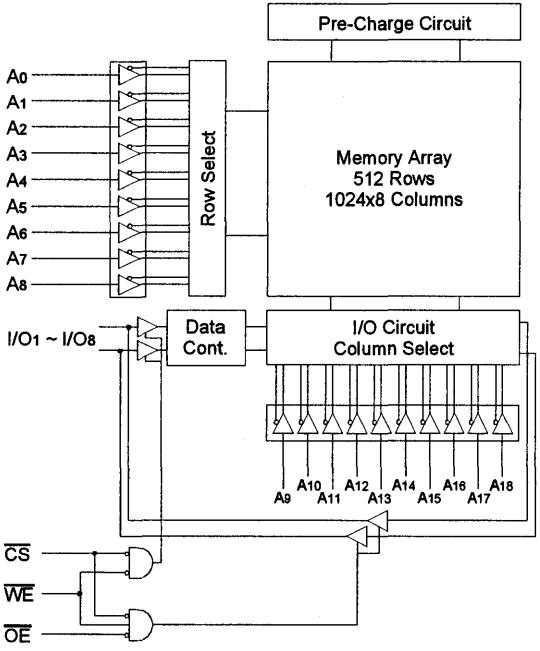
FEATURES

- Fast Access Time 12,13,15ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60mA(Max.)
  - (CMOS) : 30mA(Max.)
  - Operating KM68B4002 - 12 : 195mA(Max.)
  - KM68B4002 - 13 : 195mA(Max.)
  - KM68B4002 - 15 : 190mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM68B4002J : 36-SOJ-400

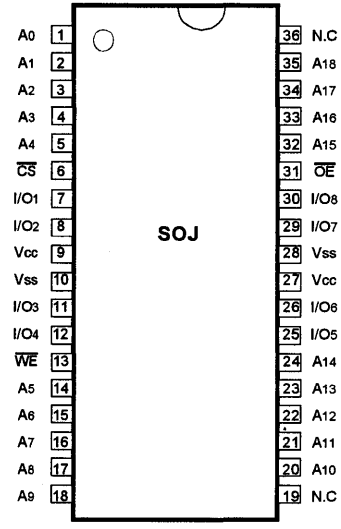
GENERAL DESCRIPTION

The KM68B4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM68B4002 uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68B4002 is packaged in a 400 mil 36-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A18	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20㎃

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20㎃

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	㎂
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-10	10	㎂
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	195	㎃
			13ns	-	195	
			15ns	-	190	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	60	㎃
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	30	㎃
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

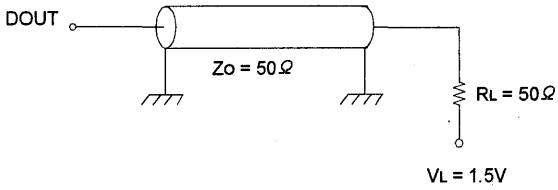
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

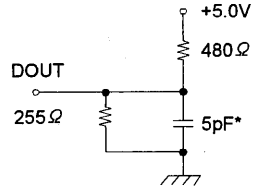
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68B4002-12		KM68B4002-13		KM68B4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	6	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

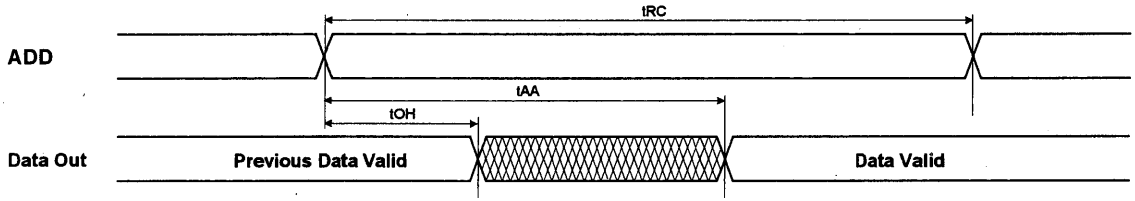
WRITE CYCLE

Parameter	Symbol	KM68B4002-12		KM68B4002-13		KM68B4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	13	-	15	-	ns
Chip Select to End of Write	tCW	8	-	9	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	9	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	9	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	6	0	7	ns
Data to Write Time Overlap	tDW	6	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

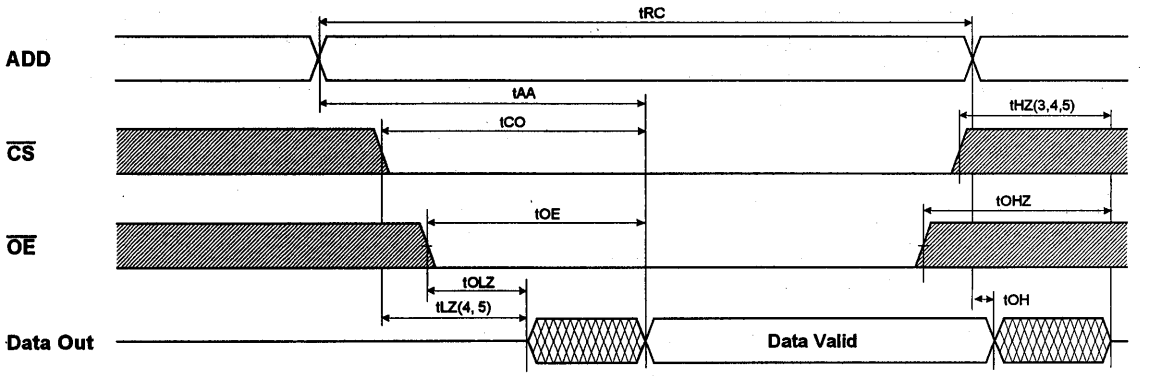
2

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



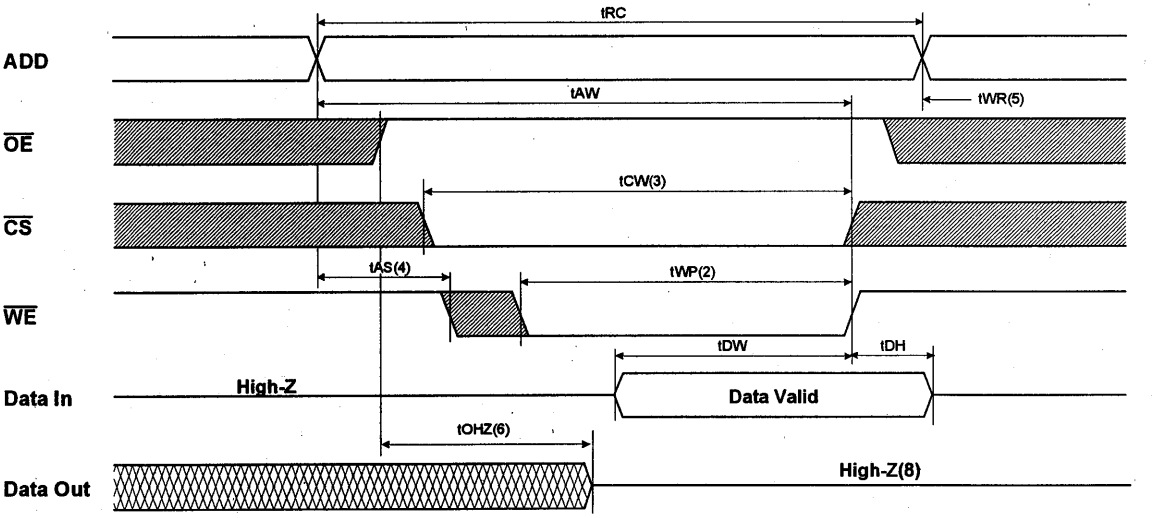
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

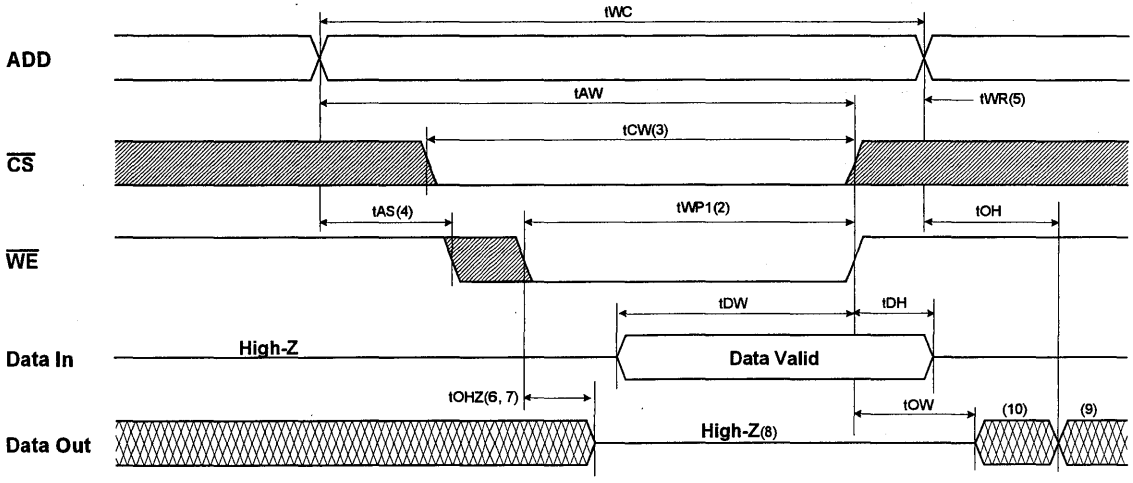
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

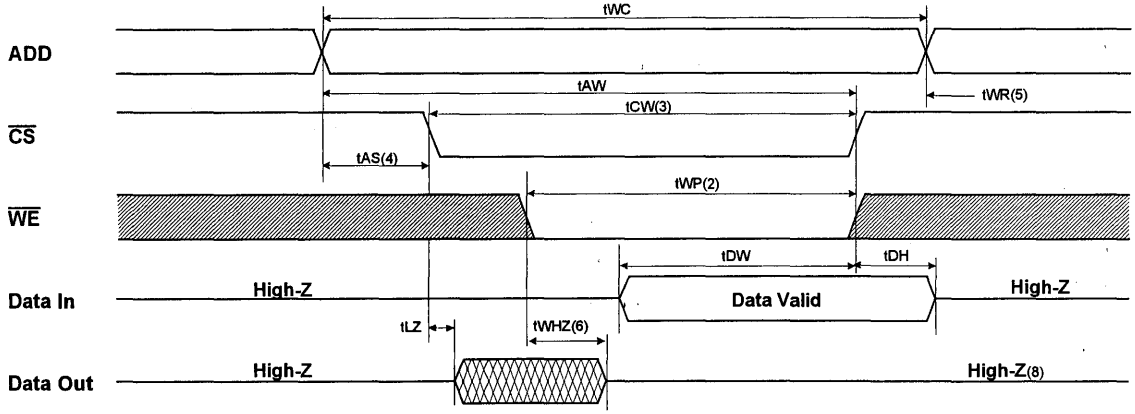


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



SAMSUNG ELECTRONICS

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

512K x 8 Bit High-Speed CMOS Static RAM

FEATURES

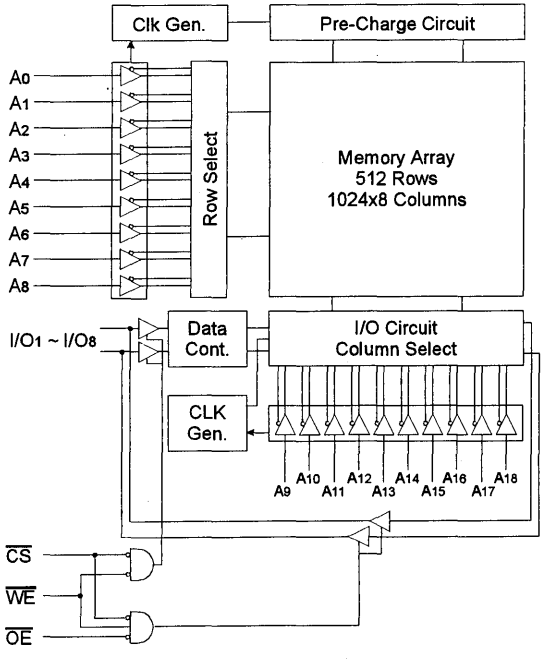
- Fast Access Time 15,17,20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM684002A - 15 : 170mA(Max.)
  - KM684002A - 17 : 165mA(Max.)
  - KM684002A - 20 : 160mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM684002AJ : 36-SOJ-400

GENERAL DESCRIPTION

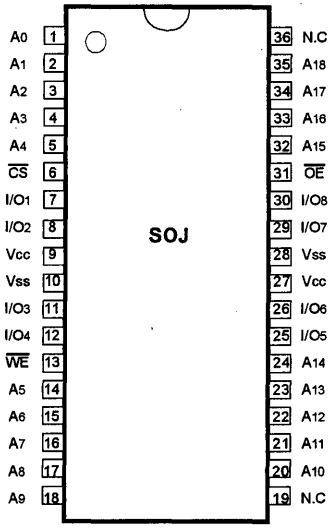
The KM684002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM684002A uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM684002A is packaged in a 400 mil 36-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	170	mA
			17ns	-	165	
			20ns	-	160	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	50	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

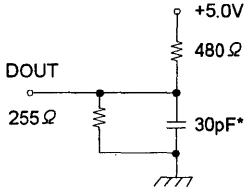
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

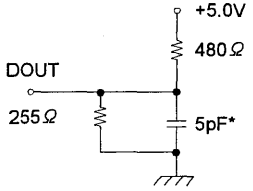
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

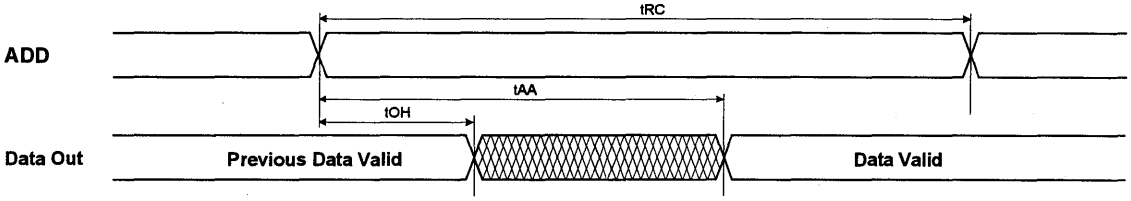
Parameter	Symbol	KM684002A-15		KM684002A-17		KM684002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

WRITE CYCLE

Parameter	Symbol	KM684002A-15		KM684002A-17		KM684002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

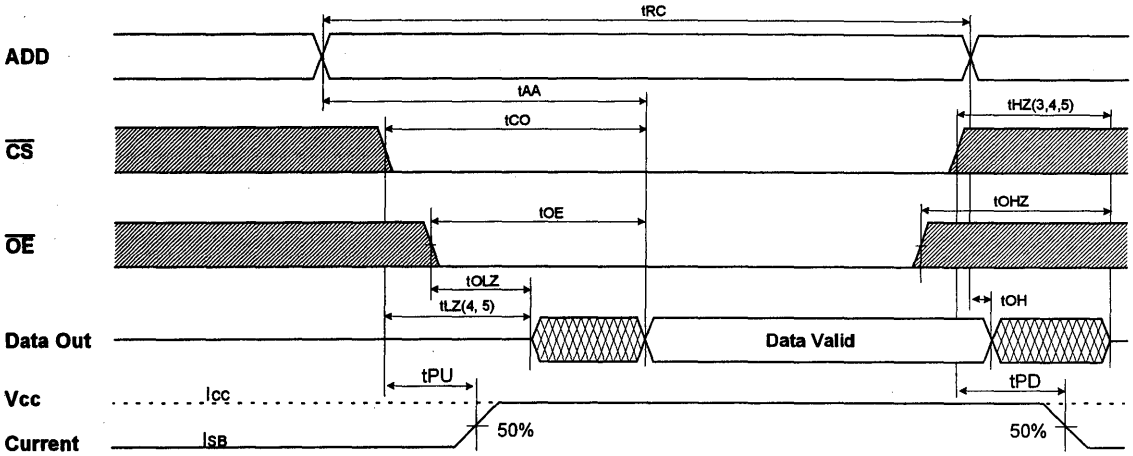
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



SAMSUNG ELECTRONICS

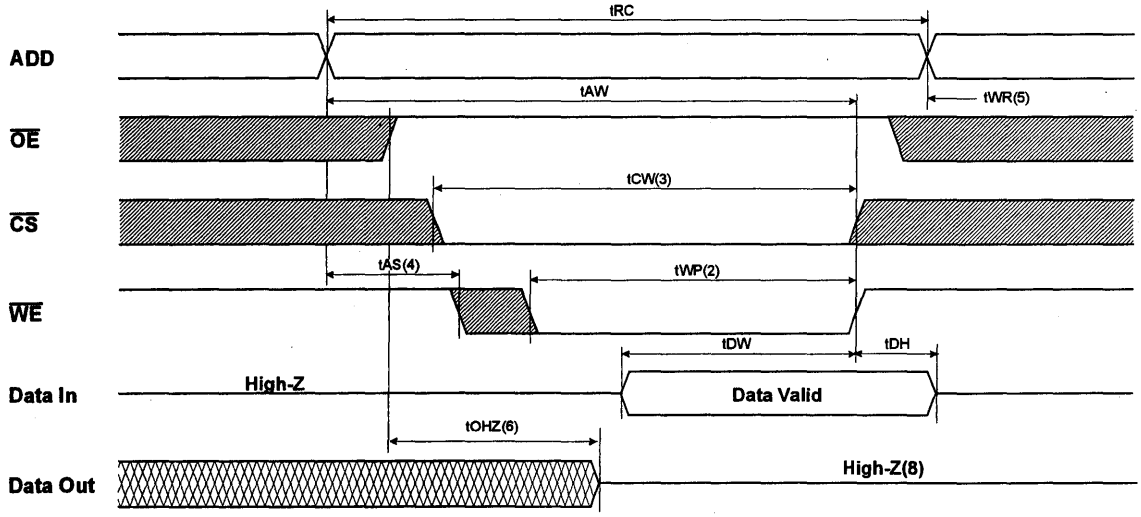
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

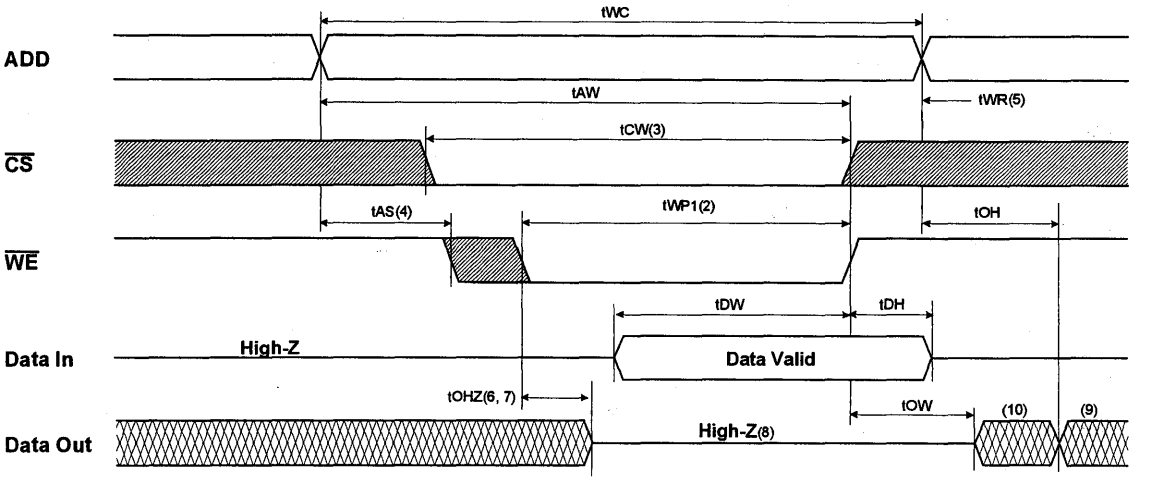
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

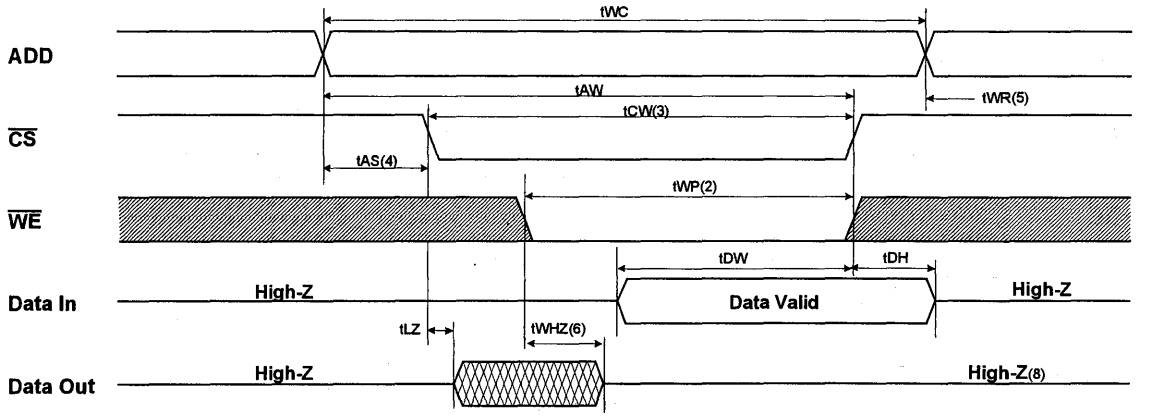


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* NOTE : X means Don't Care.

512K x 8 Bit High-Speed CMOS Static RAM

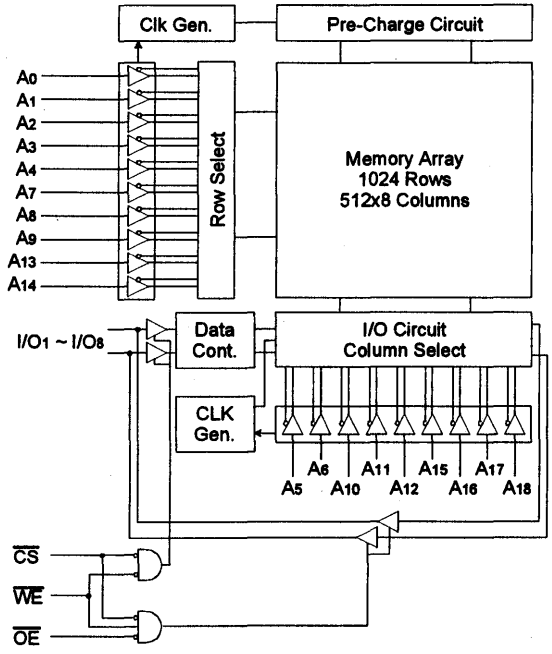
FEATURES

- Fast Access Time 17,20,25ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM684002 - 17 : 180mA(Max.)
  - KM684002 - 20 : 170mA(Max.)
  - KM684002 - 25 : 160mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM684002J : 36-SOJ-400

ORDERING INFORMATION

KM684002 -17/20/25	Commercial Temp.
KM684002E -17/20/25	Extended Temp.
KM684002I -17/20/25	Industrial Temp.

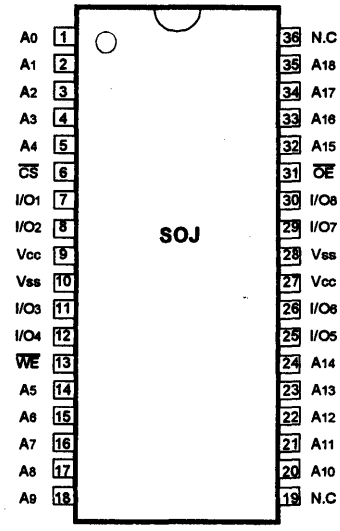
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM684002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM684002 uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM684002 is packaged in a 400 mil 36-pin plastic SOJ.

PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Extended	T_A	-25 to 85	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, V_{CC}= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to V_{CC}		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	17ns	-	180	mA
			20ns	-	170	
			25ns	-	160	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	60	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ V_{CC}-0.2V, V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

* V_{CC}=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

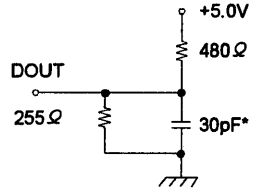
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

TEST CONDITIONS

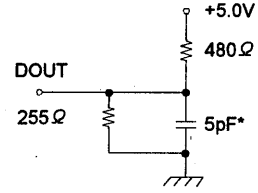
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM684002-17		KM684002-20		KM684002-25		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	17	-	20	-	25	-	ns
Address Access Time	tAA	-	17	-	20	-	25	ns
Chip Select to Output	tCO	-	17	-	20	-	25	ns
Output Enable to Valid Output	tOE	-	8	-	10	-	12	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	10	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	10	ns
Output Hold from Address Change	tOH	3	-	4	-	5	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	17	-	20	-	25	ns

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

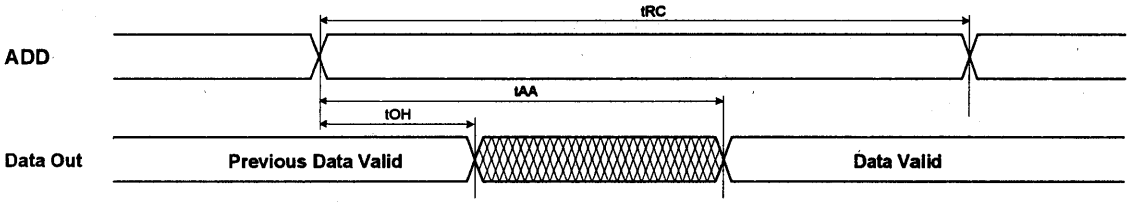
WRITE CYCLE

Parameter	Symbol	KM684002-17		KM684002-20		KM684002-25		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	17	-	20	-	25	-	ns
Chip Select to End of Write	tCW	12	-	13	-	15	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	15	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	12	-	13	-	15	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	17	-	20	-	25	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	0	10	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	5	-	ns

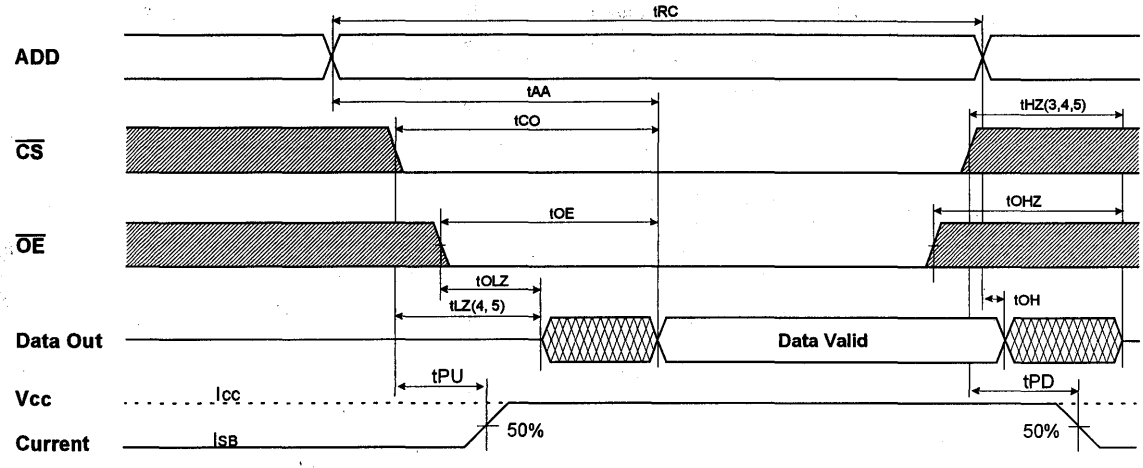
NOTE: Above parameters are also guaranteed at extended and industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



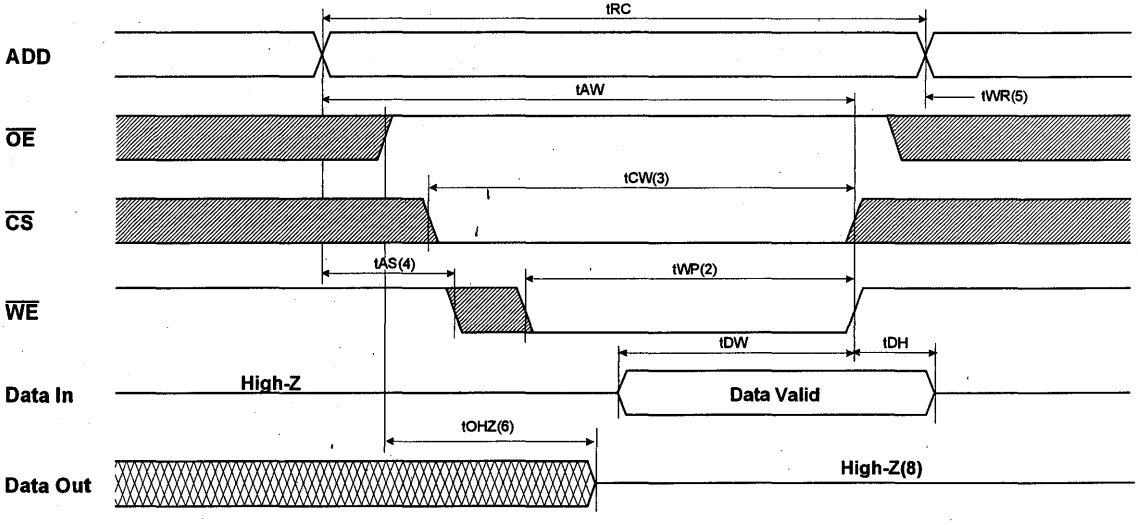
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

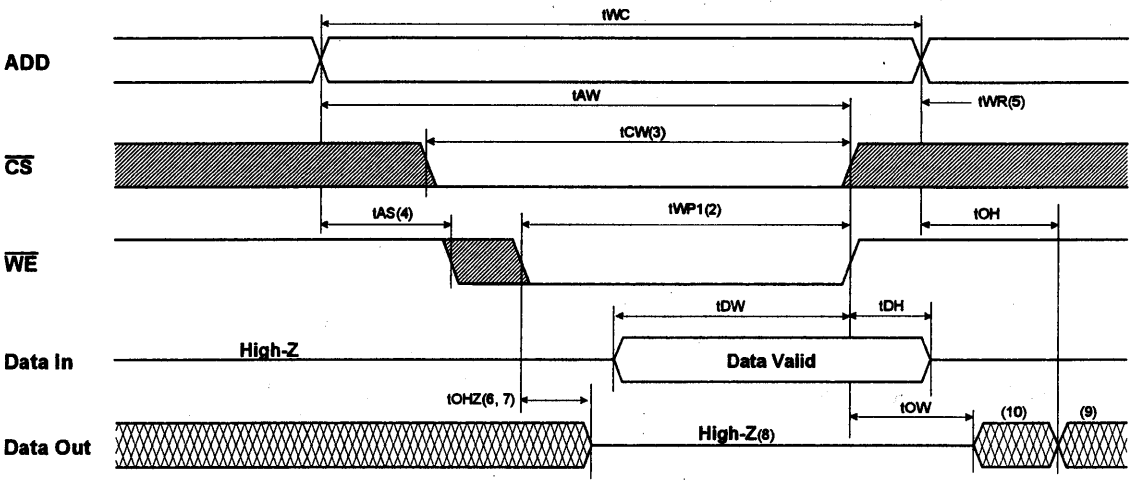
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200㎷ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

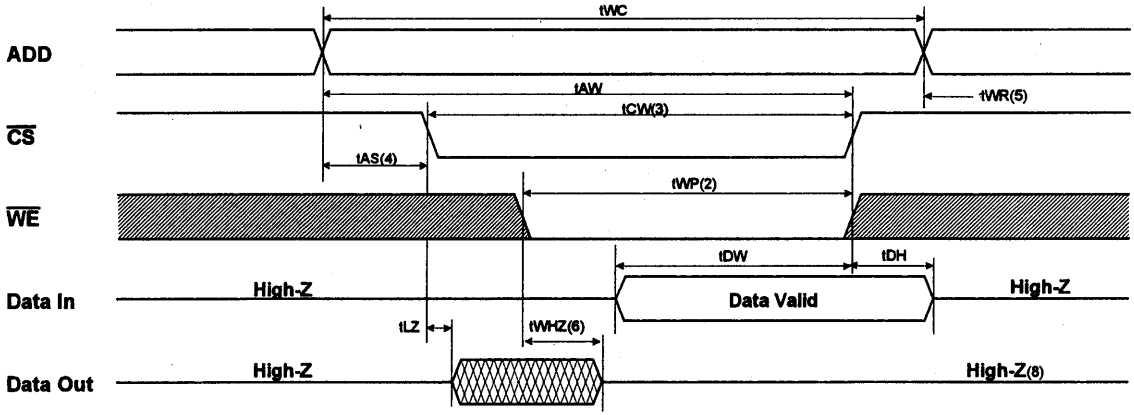


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

256K x 16 Bit High-Speed CMOS Static RAM

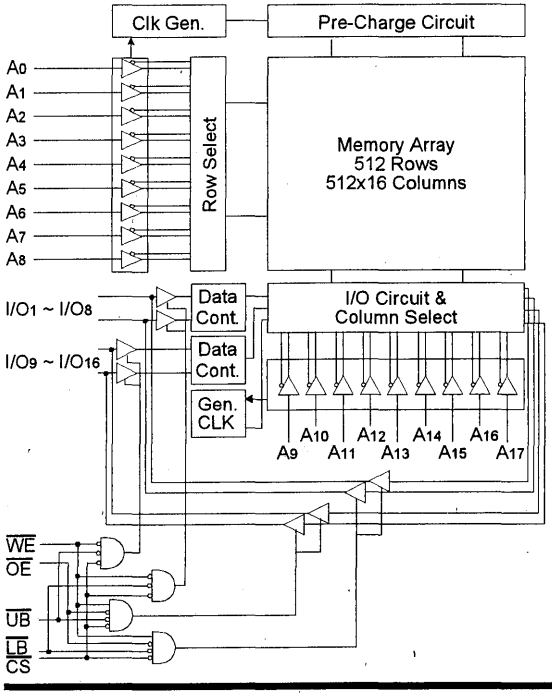
FEATURES

- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
  Standby (TTL) : 40mA(Max.)
  (CMOS) : 10mA(Max.)
  Operating KM6164002B - 10 : 250mA(Max.)
  KM6164002B - 12 : 240mA(Max.)
  KM6164002B - 15 : 230mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O1~ I/O8, $\overline{UB}$: I/O9~ I/O16
- Standard Pin Configuration
  KM6164002BJ : 44-SOJ-400
  KM6164002BT : 44-TSOP2-400F

ORDERING INFORMATION

KM6164002B -10/12/15	Commercial Temp.
KM6164002BI -10/12/15	Industrial Temp.

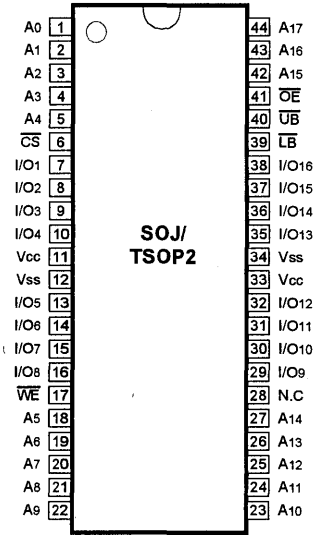
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM6164002B is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM6164002B uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6164002B is packaged in a 400mil 44-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤8ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	10ns	-	250	mA
			12ns	-	240	
			15ns	-	230	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* Vcc=5.0V ± 10% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

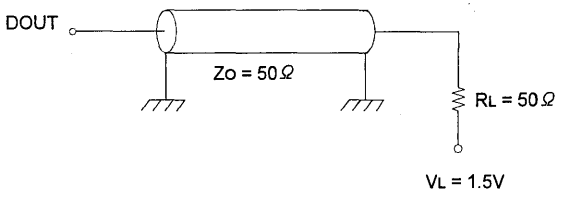
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V ± 10%, unless otherwise noted.)

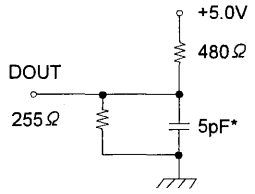
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

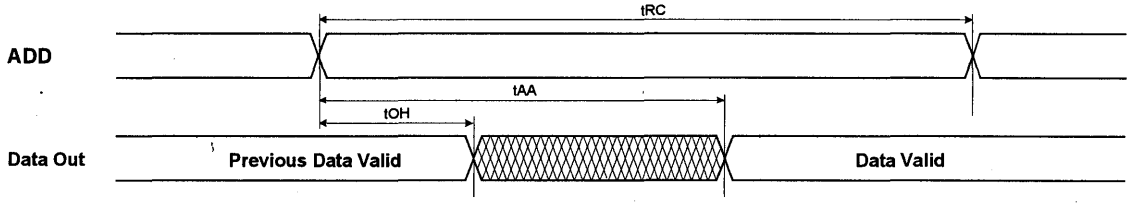
Parameter	Symbol	KM6164002B-10		KM6164002B-12		KM6164002B-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

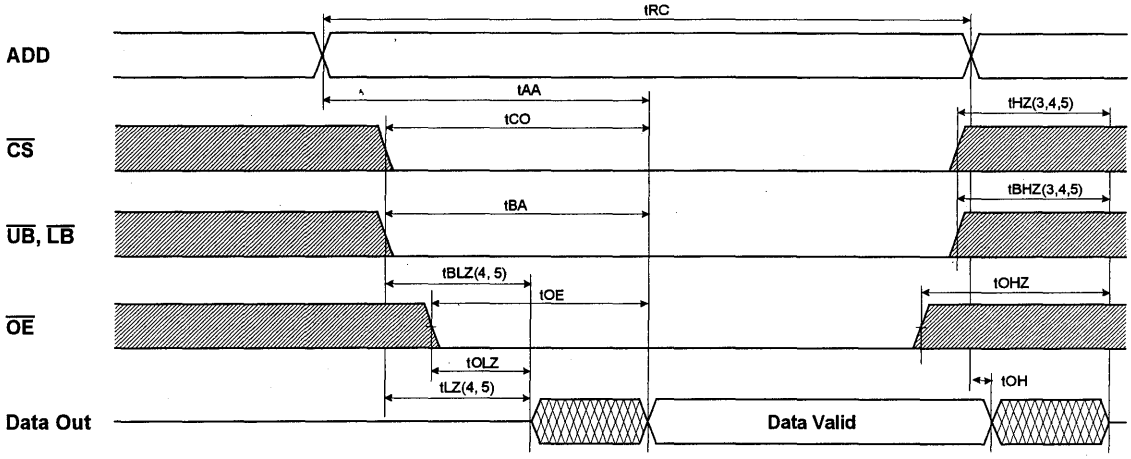
Parameter	Symbol	KM6164002B-10		KM6164002B-12		KM6164002B-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	10	-	12	-	15	-	ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	10	-	12	-	15	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	7	-	8	-	10	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	5	0	6	0	7	ns
Data to Write Time Overlap	tDW	5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$\overline{UB}$=$\overline{LB}$=VIL, $\overline{WE}$=VIH)



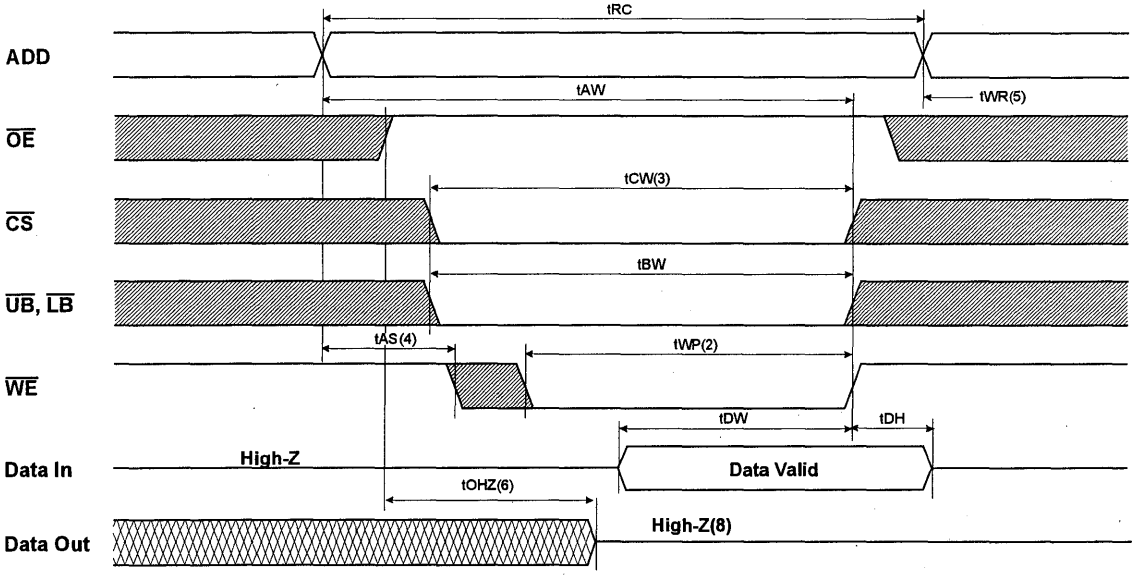
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

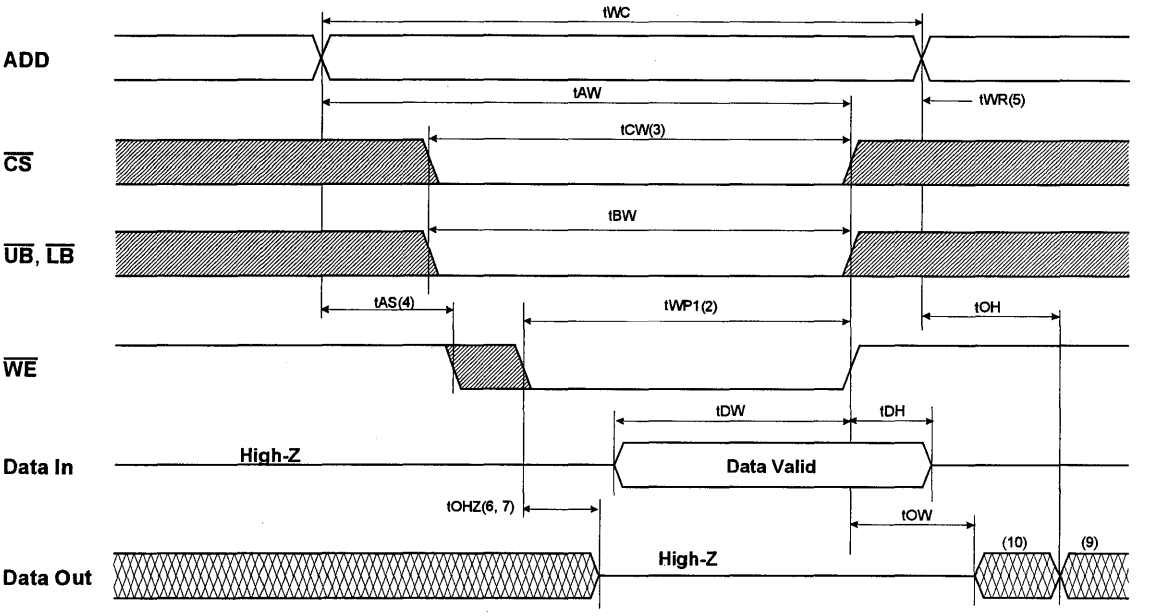
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200㎷ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

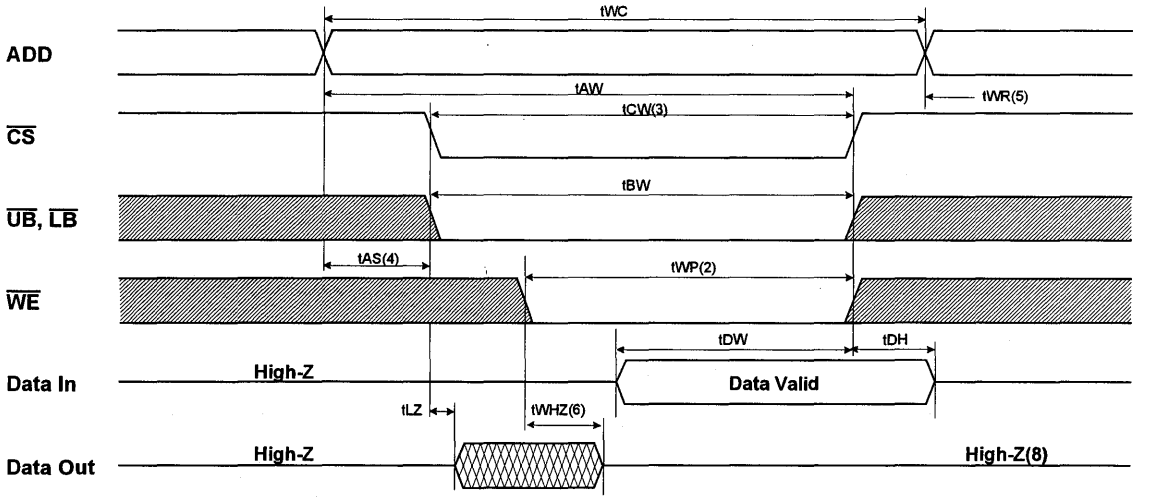


SAMSUNG ELECTRONICS

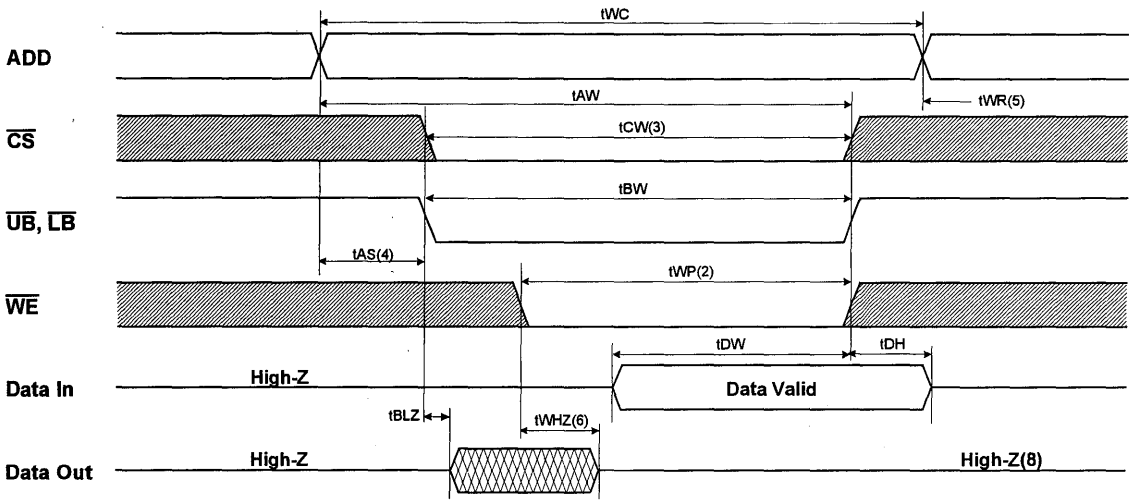
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z		ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	ICC
L	X	X	H	H				
L	H	L	L	H	Read	DOUT	High-Z	ICC
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	ICC
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

* **NOTE** : X means Don't Care.

256K x 16 Bit High-Speed BiCMOS Static RAM

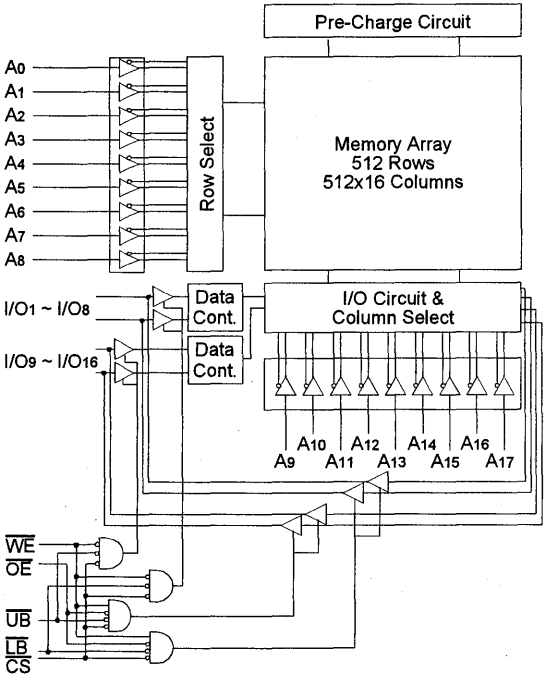
FEATURES

- Fast Access Time 12,13,15ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60mA(Max.)
  - (CMOS) : 30mA(Max.)
  - Operating KM616B4002 - 12 : 270mA(Max.)
  - KM616B4002 - 13 : 265mA(Max.)
  - KM616B4002 - 15 : 260mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O1~ I/O8, $\overline{UB}$: I/O9~ I/O16
- Standard Pin Configuration
  - KM616B4002J : 44-SOJ-400

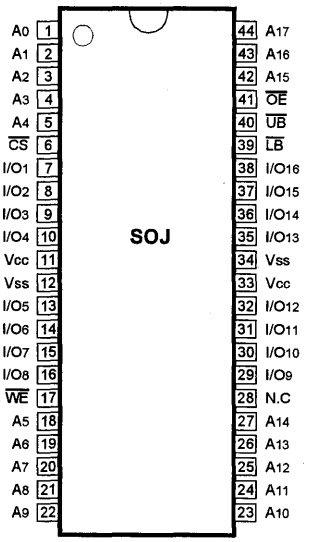
GENERAL DESCRIPTION

The KM616B4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM616B4002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616B4002 is packaged in a 400mil 44-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20㎃

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20㎃

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	㎂
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-10	10	㎂
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	270	mA
			13ns	-	265	
			15ns	-	260	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	60	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	30	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

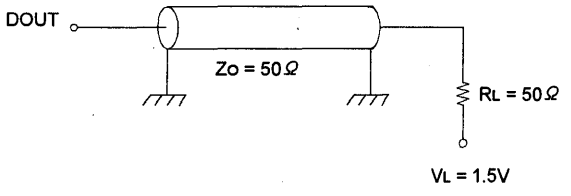
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

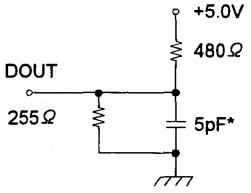
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

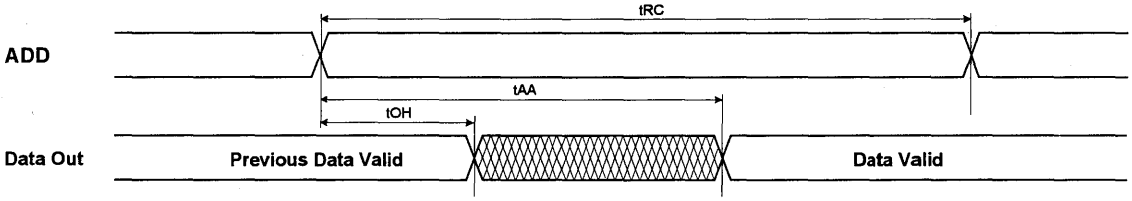
Parameter	Symbol	KM616B4002-12		KM616B4002-13		KM616B4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	7	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	6	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	6	0	6	0	7	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	6	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM616B4002-12		KM616B4002-13		KM616B4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	13	-	15	-	ns
Chip Select to End of Write	tCW	8	-	9	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	9	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	9	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	10	-	11	-	12	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	8	-	9	-	10	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	6	0	7	ns
Data to Write Time Overlap	tDW	6	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

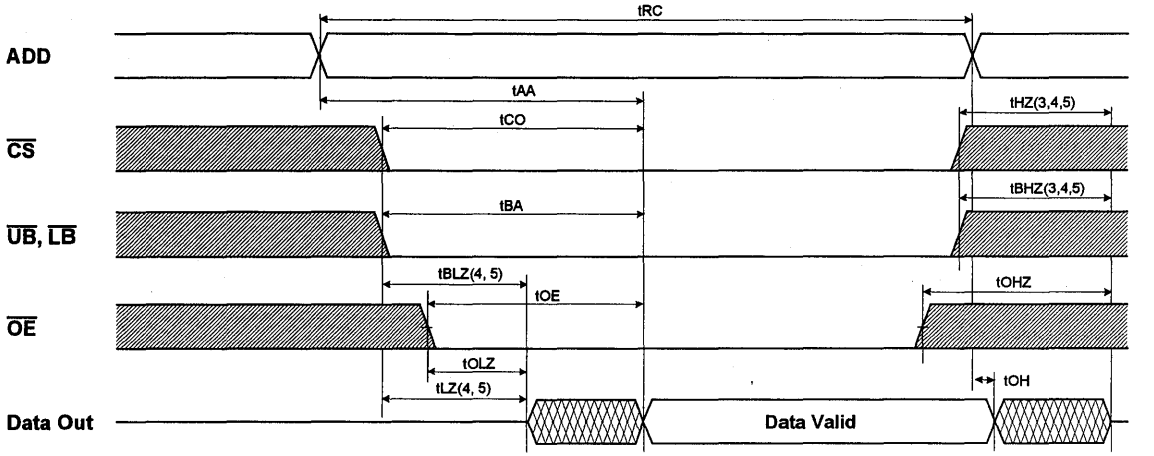
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$\overline{UB}$=$\overline{LB}$=VIL, $\overline{WE}$=VIH)



SAMSUNG ELECTRONICS

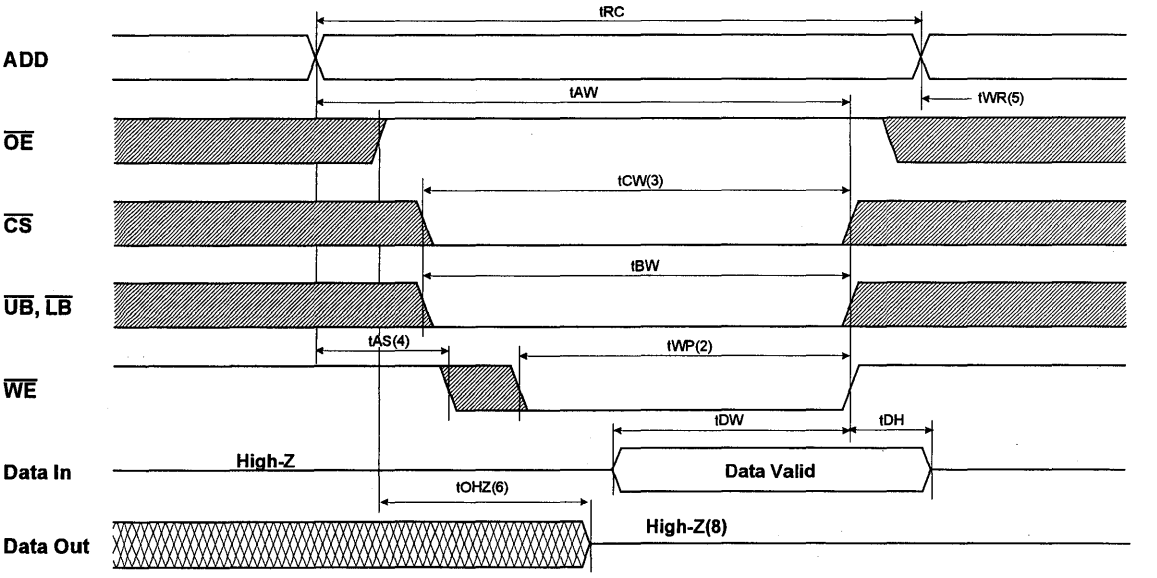
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



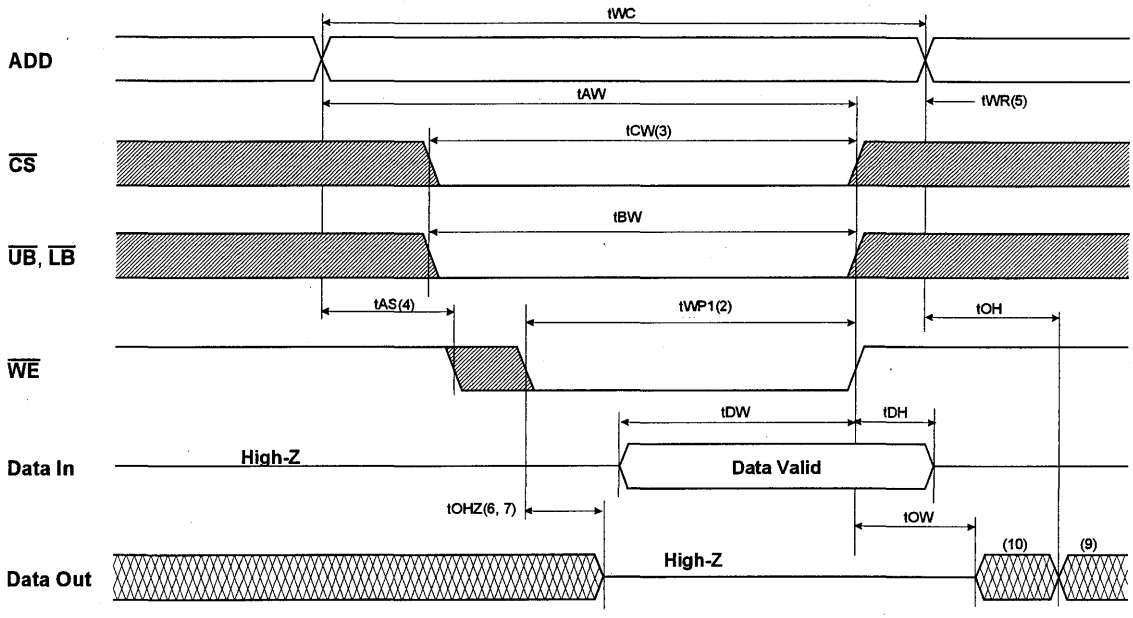
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

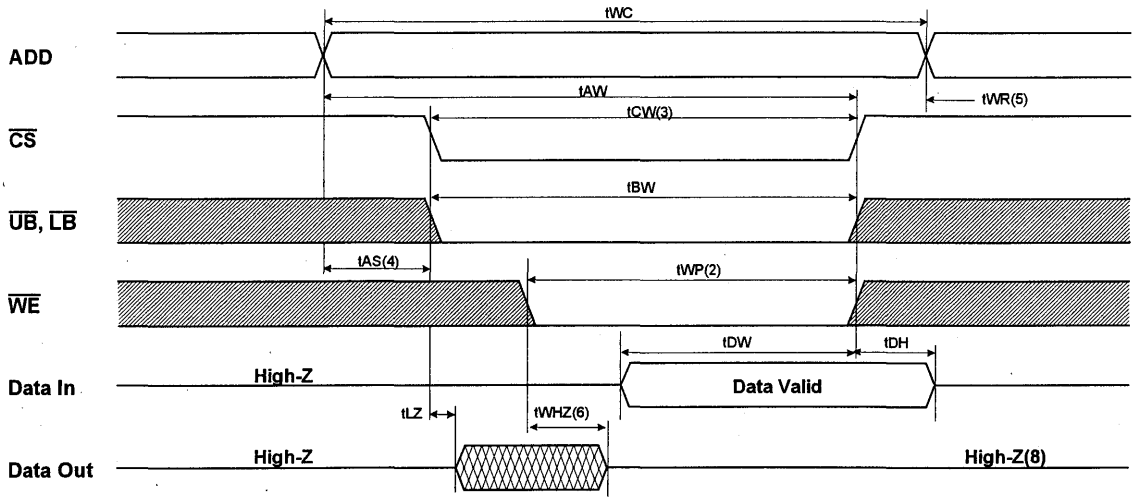
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)

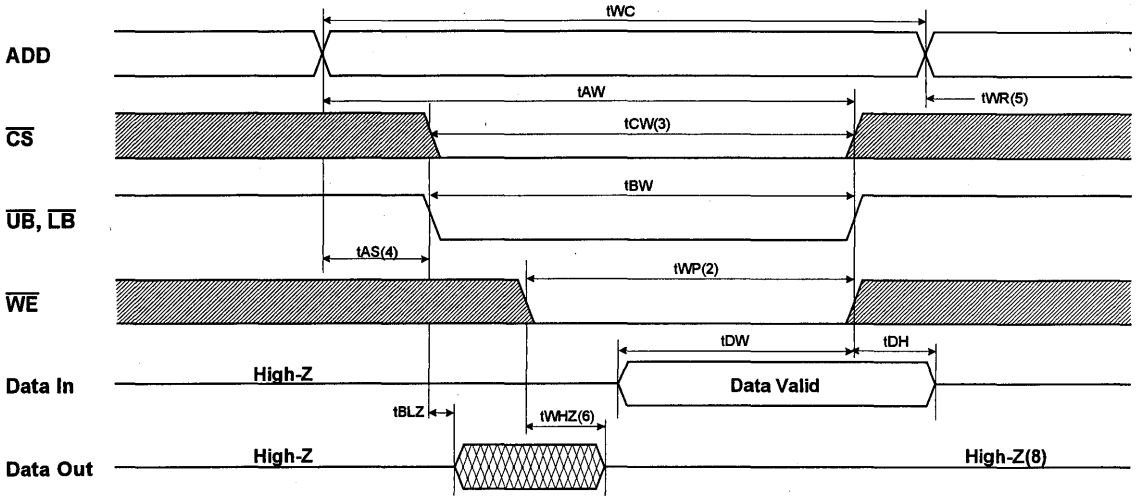


TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$. $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z		ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	ICC
L	X	X	H	H				
L	H	L	L	H	Read	DOUT	High-Z	ICC
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	ICC
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

* **NOTE** : X means Don't Care.

256K x 16 Bit High-Speed CMOS Static RAM

FEATURES

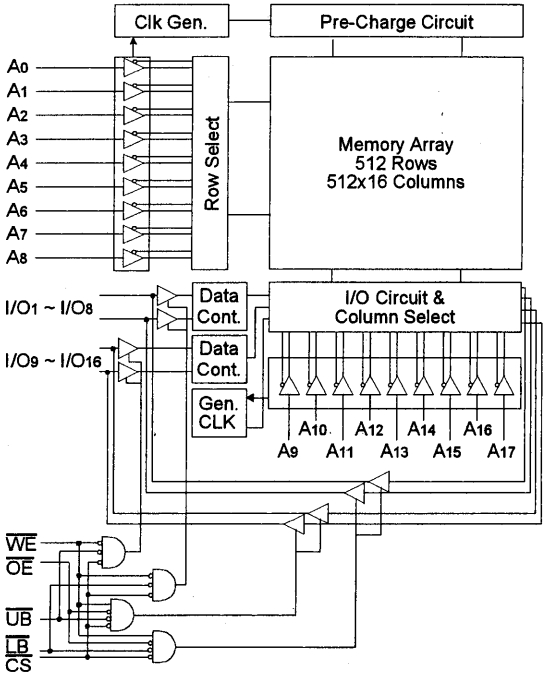
- Fast Access Time 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM6164002A - 15 : 210mA(Max.)
  - KM6164002A - 17 : 205mA(Max.)
  - KM6164002A - 20 : 200mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O1~ I/O8, $\overline{UB}$: I/O9~ I/O16
- Standard Pin Configuration
  - KM6164002AJ : 44-SOJ-400

GENERAL DESCRIPTION

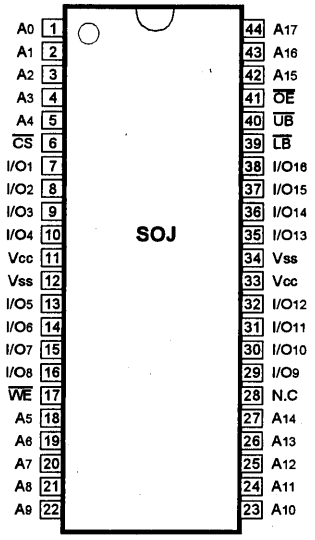
The KM6164002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM6164002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6164002A is packaged in a 400mil 44-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	210	mA
			17ns	-	205	
			20ns	-	200	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	50	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

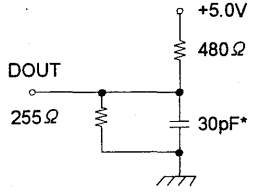
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

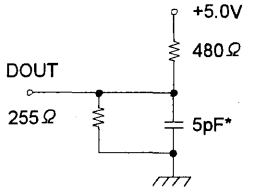
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

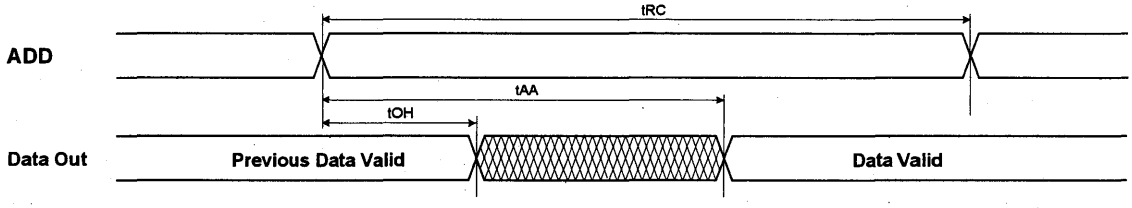
Parameter	Symbol	KM6164002A-15		KM6164002A-17		KM6164002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	7	-	8	-	9	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	9	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

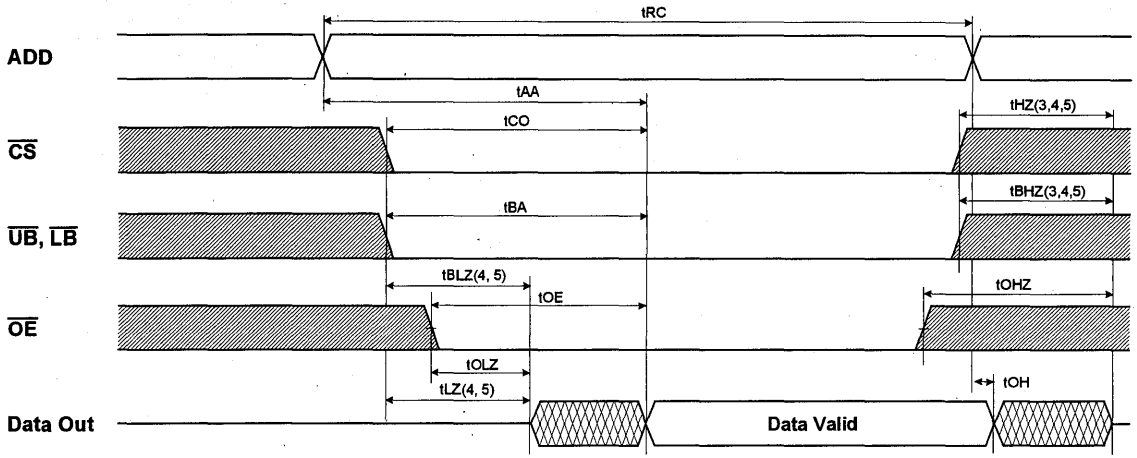
Parameter	Symbol	KM6164002A-15		KM6164002A-17		KM6164002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	12	-	13	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$\overline{UB}$=$\overline{LB}$=VIL, $\overline{WE}$=VIH)



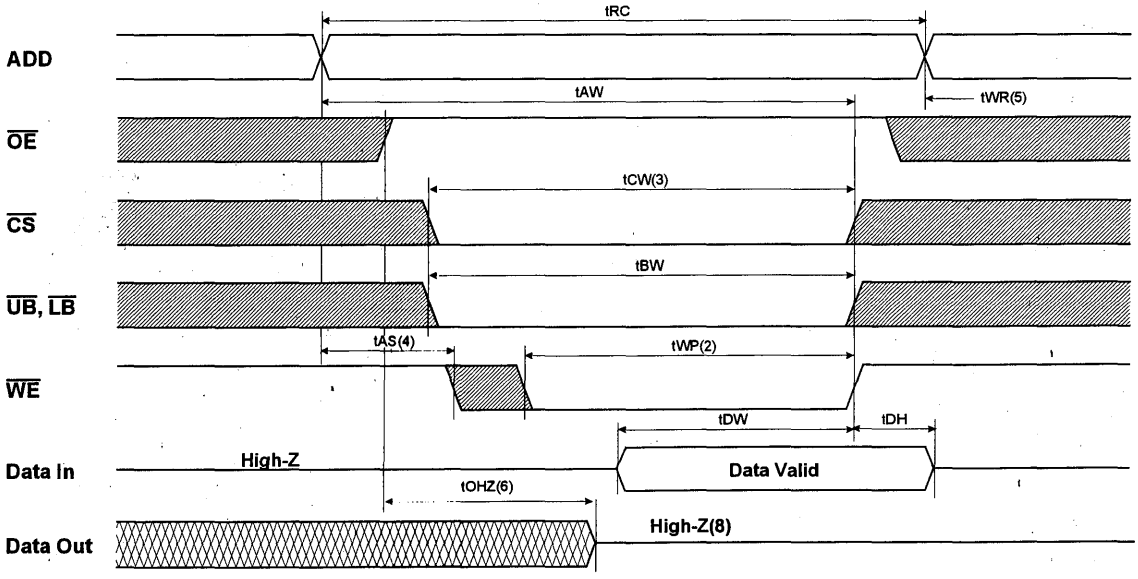
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

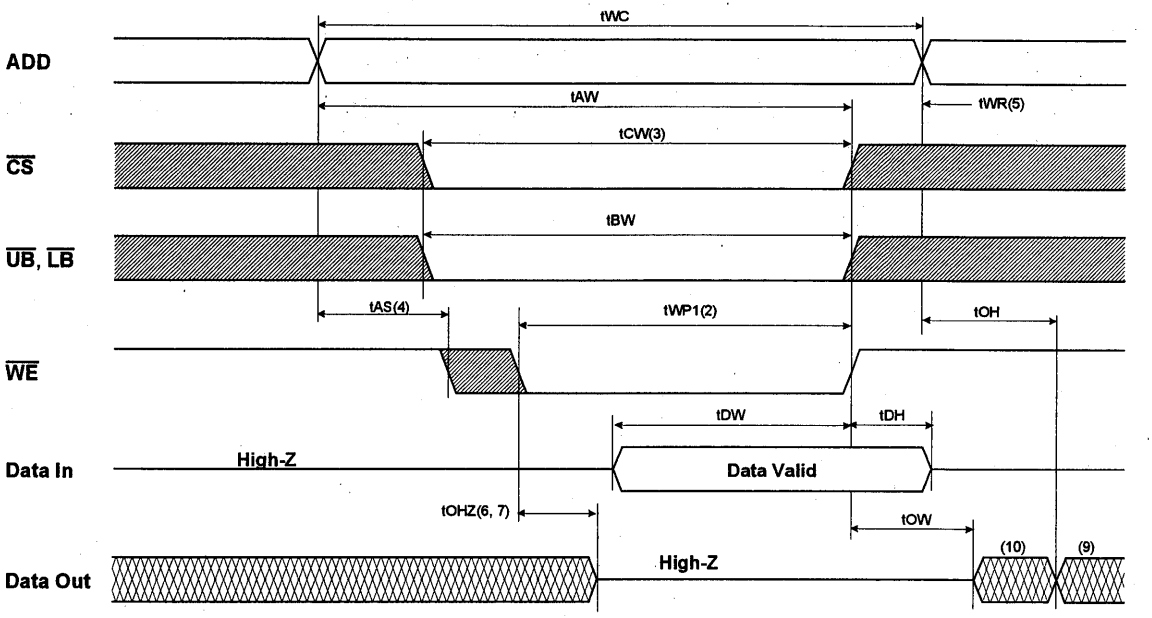
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

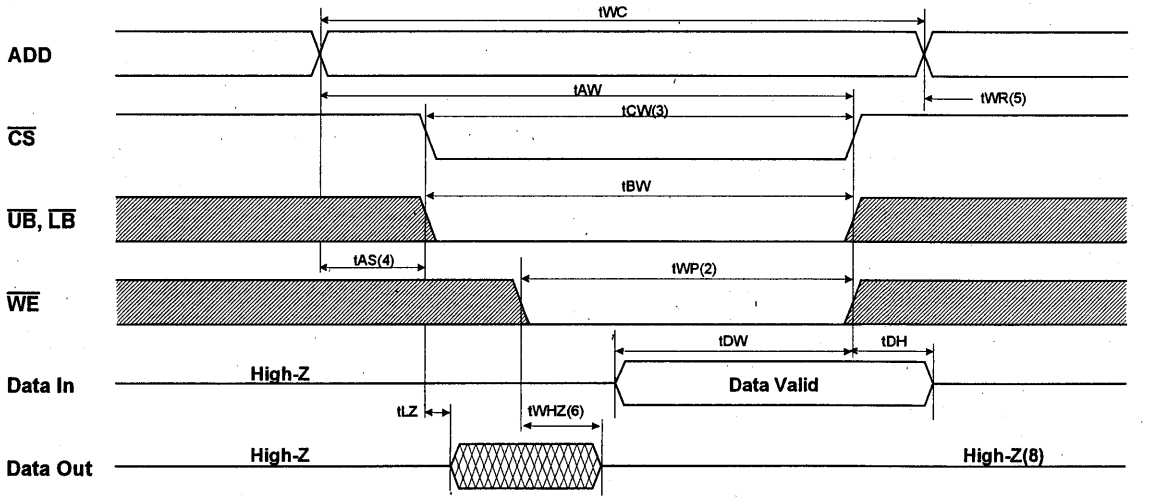


SAMSUNG ELECTRONICS

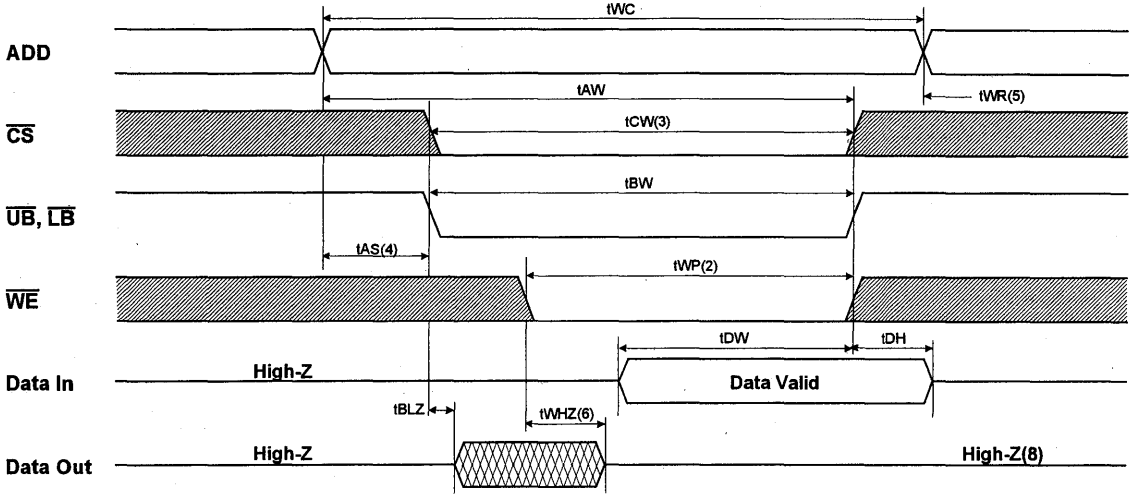
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$. $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z		I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

* **NOTE** : X means Don't Care.

256K x 16 Bit High-Speed CMOS Static RAM

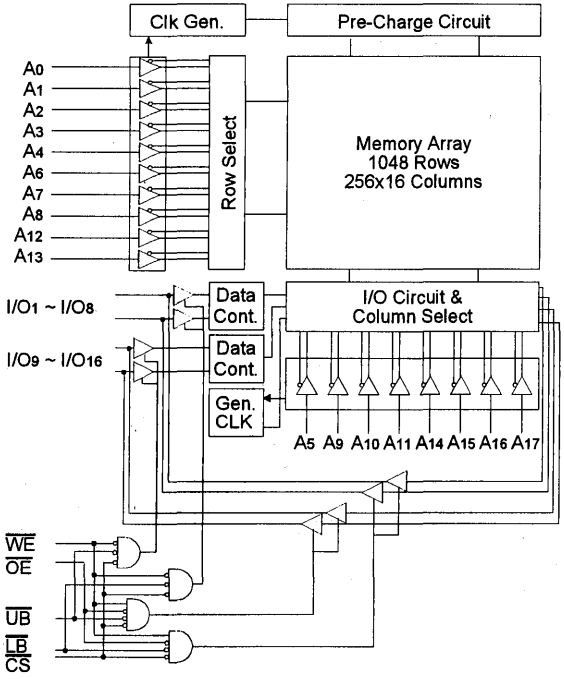
FEATURES

- Fast Access Time 20,25ns(Max.)
- Low Power Dissipation
  Standby (TTL) : 60mA(Max.)
  (CMOS) : 10mA(Max.)
  Operating KM6164002 - 20 : 240mA(Max.)
  KM6164002 - 25 : 220mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O1~ I/O8, $\overline{UB}$: I/O9~ I/O16
- Standard Pin Configuration
  KM6164002J : 44-SOJ-400

ORDERING INFORMATION

KM6164002 -20/25	Commercial Temp.
KM6164002E -20/25	Extended Temp.
KM6164002I -20/25	Industrial Temp.

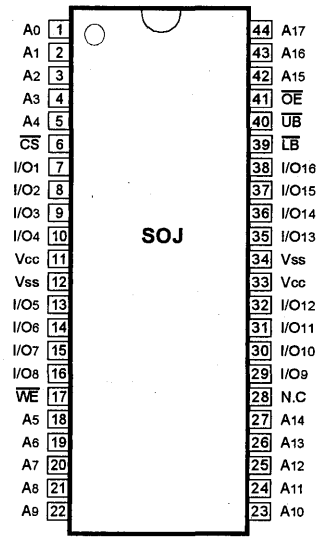
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM6164002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM6164002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM6164002 is packaged in a 400mil 44-pin plastic SOJ.

PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Extended	T_A	-25 to 85	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	20ns	-	240	mA
			25ns	-	220	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	60	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-0.1mA		-	3.95	V

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

* Vcc=5.0V ± 5% Temp. = 25℃

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

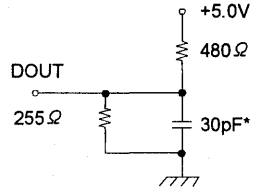
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 5.0V±10%, unless otherwise noted.)

TEST CONDITIONS

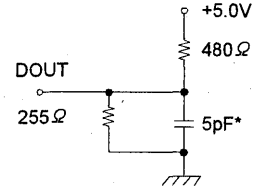
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at extended and industrial temperature ranges.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6164002-20		KM6164002-25		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	20	-	25	-	ns
Address Access Time	tAA	-	20	-	25	ns
Chip Select to Output	tCO	-	20	-	25	ns
Output Enable to Valid Output	tOE	-	10	-	12	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	10	-	12	ns
Chip Enable to Low-Z Output	tLZ	5	-	5	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	7	0	8	ns
Output Hold from Address Change	tOH	4	-	5	-	ns

NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

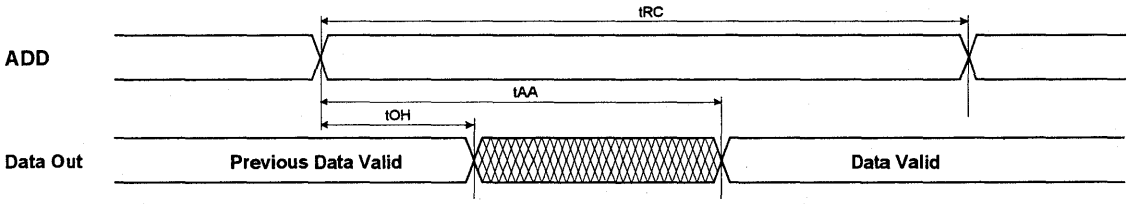
WRITE CYCLE

Parameter	Symbol	KM6164002-20		KM6164002-25		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	20	-	25	-	ns
Chip Select to End of Write	tCW	15	-	17	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	15	-	17	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	15	-	17	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	20	-	25	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	15	-	17	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	8	ns
Data to Write Time Overlap	tDW	10	-	12	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	4	-	ns

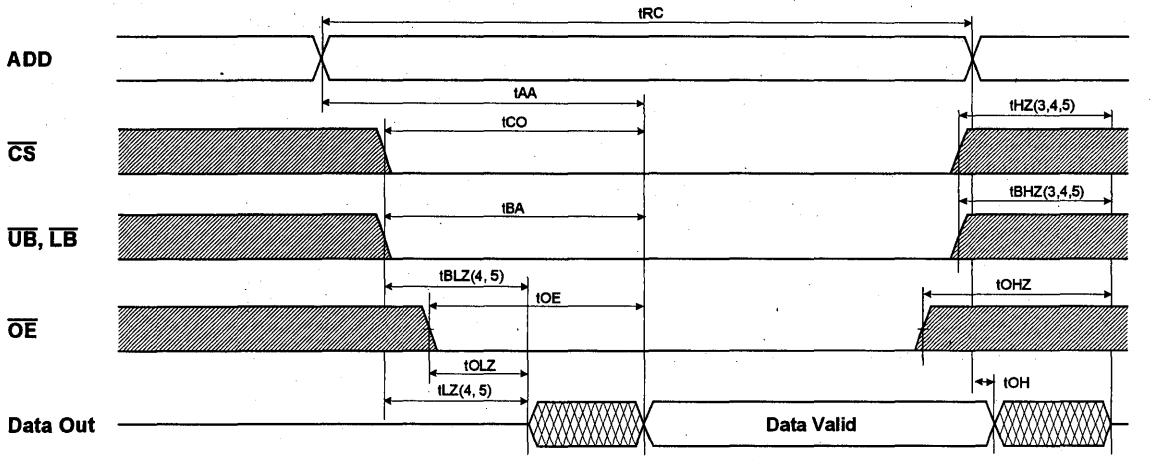
NOTE: Above parameters are also guaranteed at extended and industrial temperature ranges.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$\overline{UB}$=$\overline{LB}$=V_{IL}, $\overline{WE}$=V_{IH})



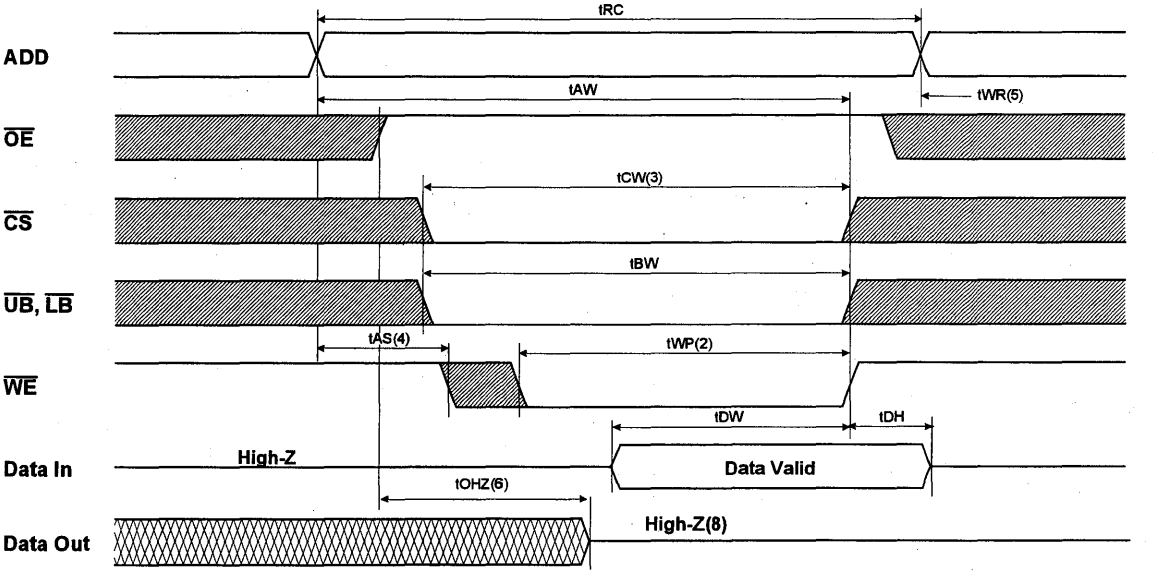
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



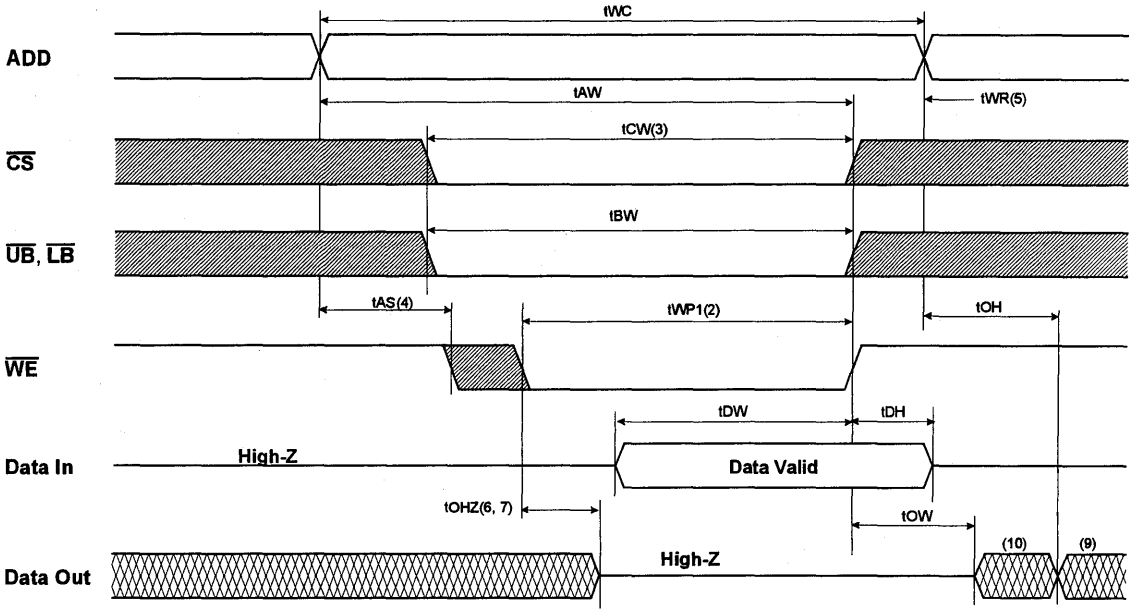
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

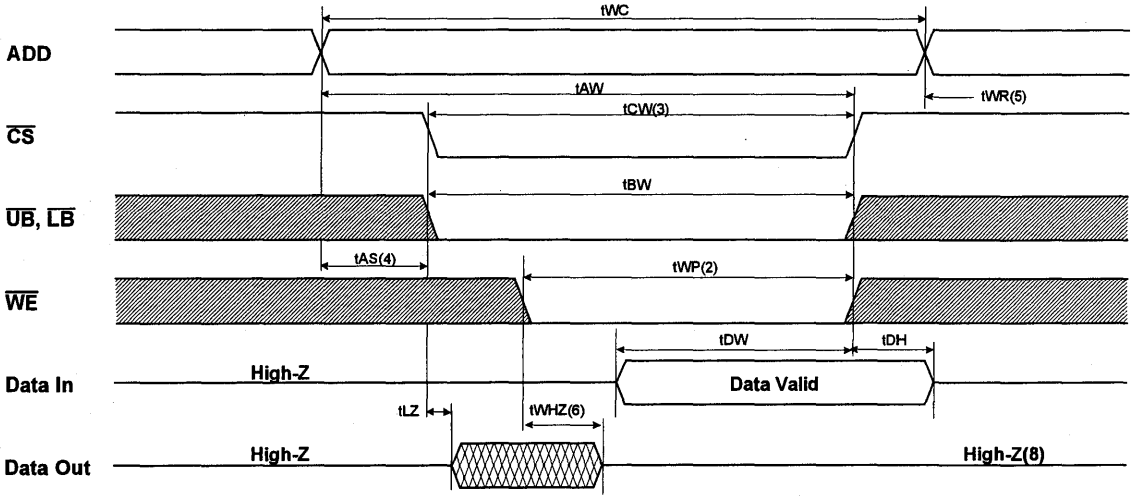
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



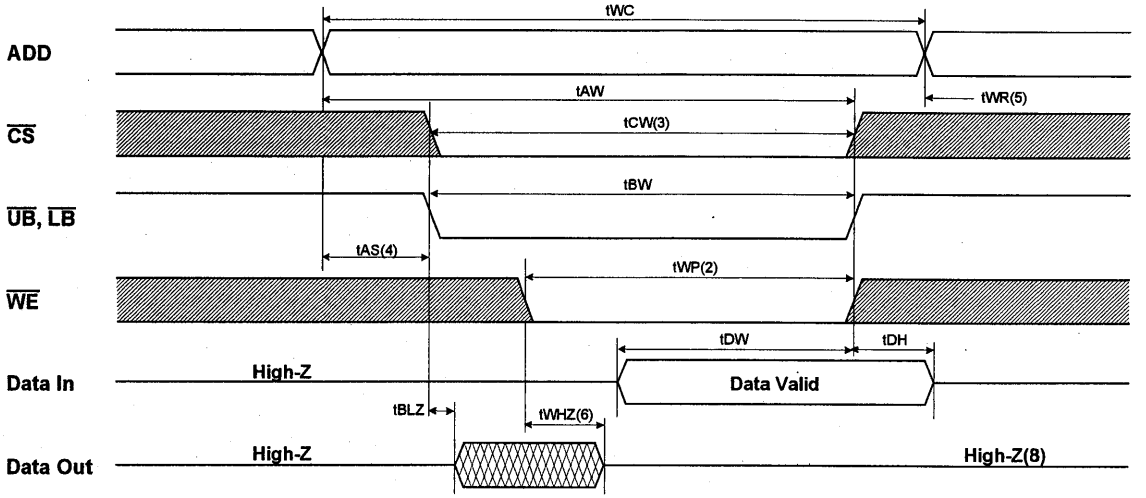
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$. $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z		ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	ICC
L	X	X	H	H				
L	H	L	L	H	Read	DOUT	High-Z	ICC
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	ICC
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

* **NOTE** : X means Don't Care.

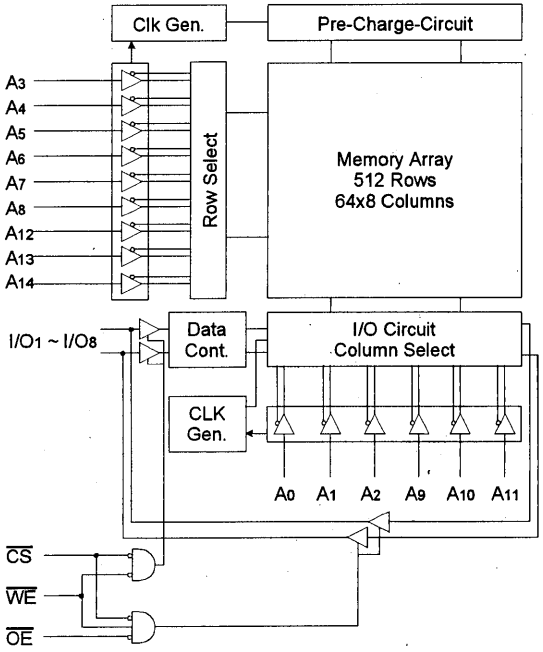
256K High Speed SRAM (3.3V Operation)

32K x 8 Bit High-Speed CMOS Static RAM (3.3V Operating)

FEATURES

- Fast Access Time 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30mA(Max.)
  - (CMOS) : 0.1mA(Max.)
  - Operating KM68V257C - 15 : 90mA(Max.)
  - KM68V257C - 17 : 80mA(Max.)
  - KM68V257C - 20 : 70mA(Max.)
- Single 3.3V ± 0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage : 2V (min)
- Standard Pin Configuration
  - KM68V257CP : 28-DIP-300
  - KM68V257CJ : 28-SOJ-300
  - KM68V257CTG : 28-TSOP1-0813, 4F

FUNCTIONAL BLOCK DIAGRAM

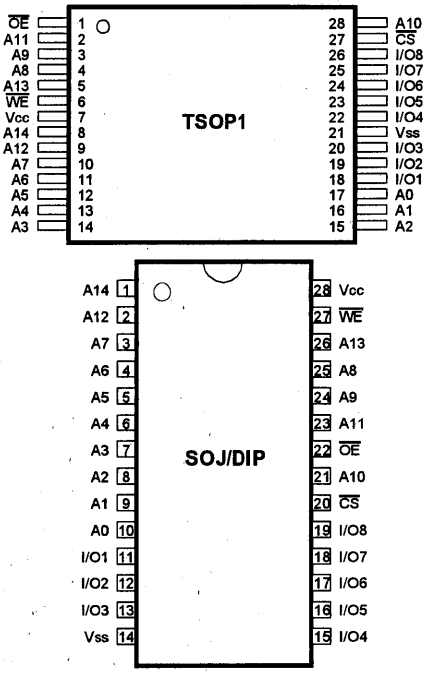


GENERAL DESCRIPTION

The KM68V257C is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits. The KM68V257C uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V257C is packaged in a 300 mil 28-pin plastic DIP, SOJ or TSOP1 forward.

2

PIN CONFIGURATION(*Top View*)



PIN FUNCTION

Pin Name	Pin Function
A0 - A14	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(Min) = -2.0(Pulse Width ≤ 12ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V(Pulse Width ≤ 12ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	90	mA
			17ns	-	80	
			20ns	-	70	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	30	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	0.1	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

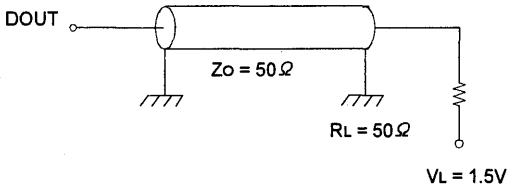
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0℃ to 70℃, V_{CC} = 3.3V±0.3V, unless otherwise noted.)

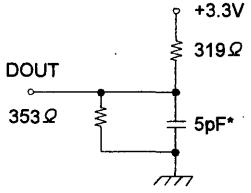
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



READ CYCLE

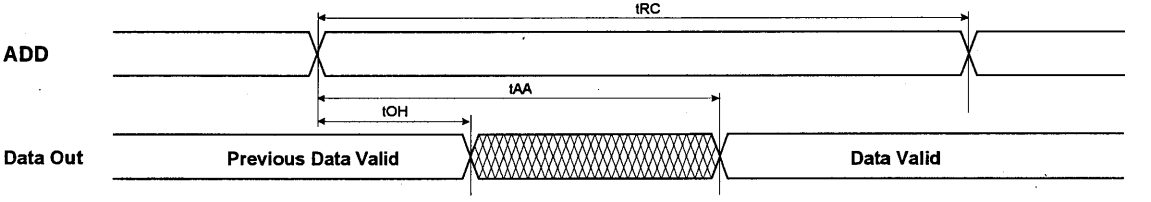
Parameter	Symbol	KM68V257C-15		KM68V257C-17		KM68V257C-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	7	-	8	-	10	ns
Chip Enable to Low-Z Output Access Time	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	10	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	10	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

WRITE CYCLE

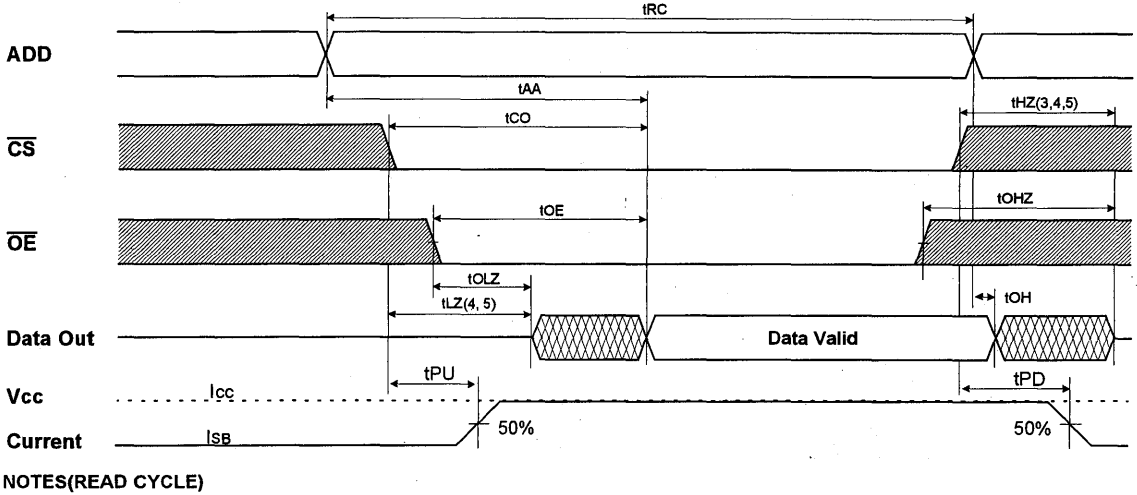
Parameter	Symbol	KM68V257C-15		KM68V257C-17		KM68V257C-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	11	-	12	-	13	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	11	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	11	-	12	-	13	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	6	0	8	ns
Data to Write Time Overlap	tDW	8	-	8	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	0	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



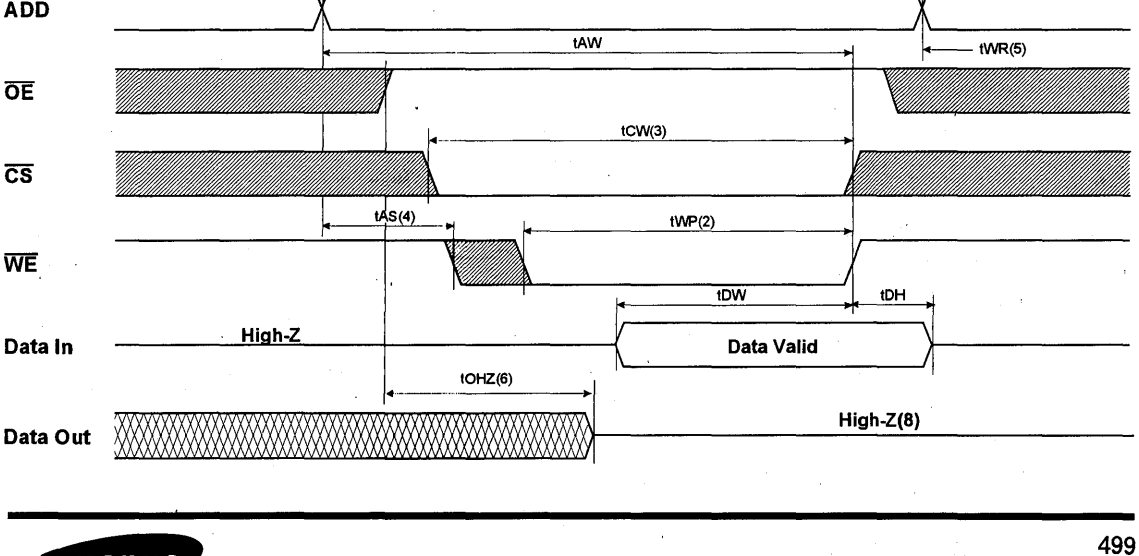
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



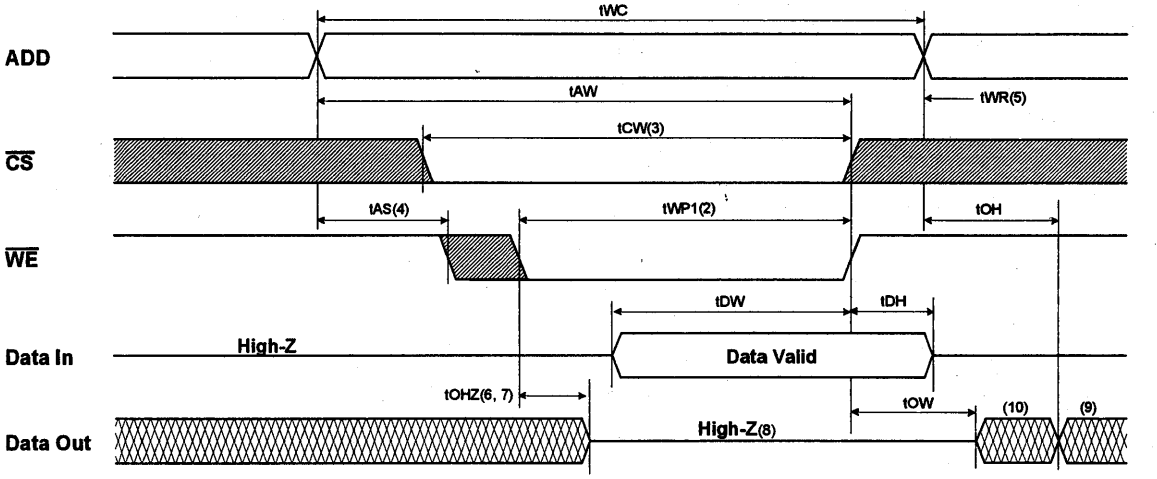
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

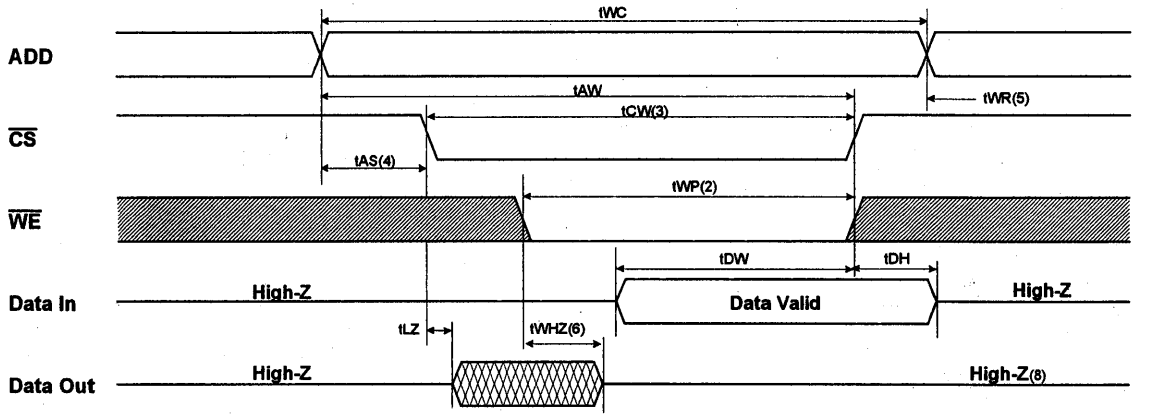
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

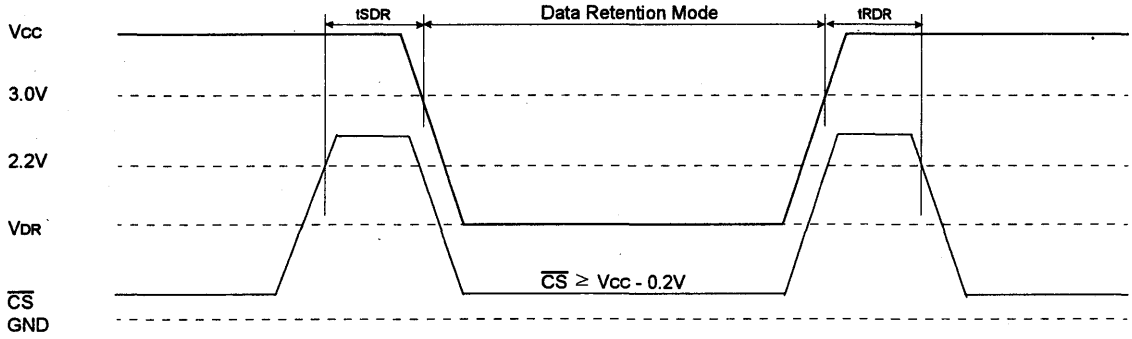
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.07	mA
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



SAMSUNG ELECTRONICS

1M High Speed SRAM (3.3V Operation)

256K x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 8,10,12ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30mA(Max.)
  - (CMOS) : 5mA(Max.)
  - 0.5mA(Max.) - L-Ver. only
  - Operating KM64V1003B/BL - 8 : 150mA(Max.)
  - KM64V1003B/BL - 10 : 140mA(Max.)
  - KM64V1003B/BL - 12 : 130mA(Max.)
- Single 3.3V ±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM64V1003B/BLJ : 32-SOJ-400
  - KM64V1003B/BLT: 32-TSOP2-400F

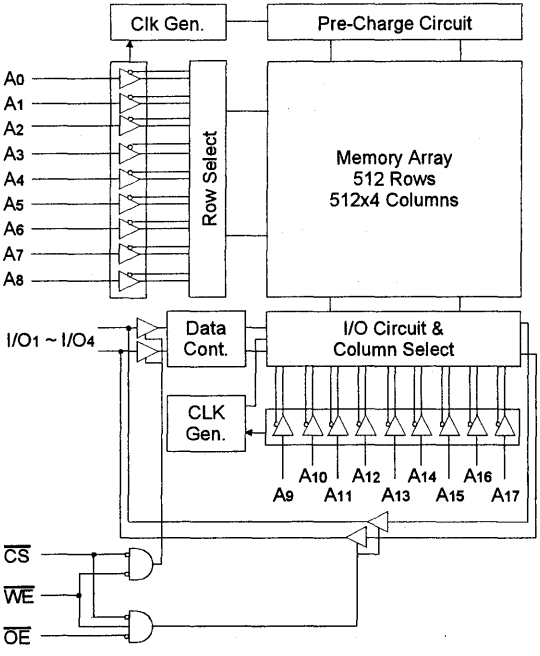
GENERAL DESCRIPTION

The KM64V1003B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM64V1003B/BL uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64V1003B/BL is packaged in a 400 mil 32-pin plastic SOJ or TSOP2 forward.

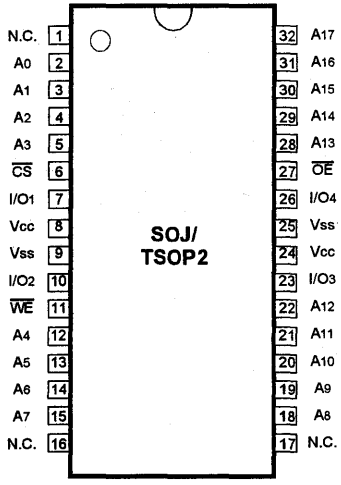
ORDERING INFORMATION

KM64V1003B/BL -8/10/12	Commercial Temp.
KM64V1003BI/BLI -8/10/12	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 5.5	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.0	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 6ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 6ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	8ns	-	150	mA
			10ns	-	140	
			12ns	-	130	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	30	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	5	mA
			L-Ver.	-	0.5	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

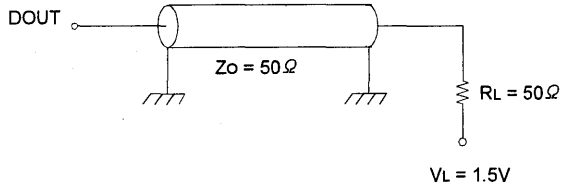
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 3.3V±0.3V, unless otherwise noted.)

TEST CONDITIONS

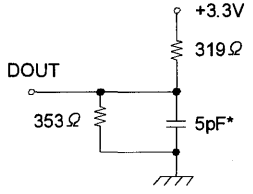
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64V1003B/BL-8		KM64V1003B/BL-10		KM64V1003B/BL-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	8	-	10	-	12	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

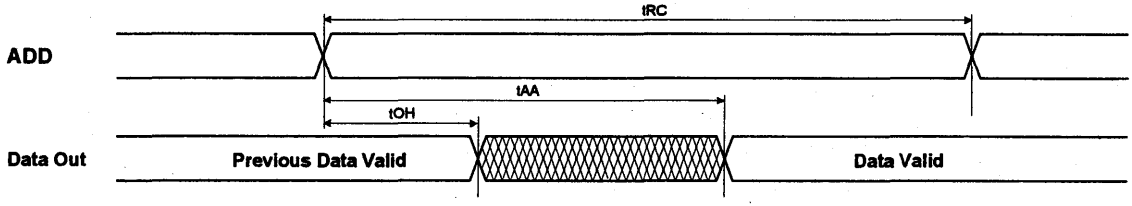
WRITE CYCLE

Parameter	Symbol	KM64V1003B/BL-8		KM64V1003B/BL-10		KM64V1003B/BL-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	8	-	10	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

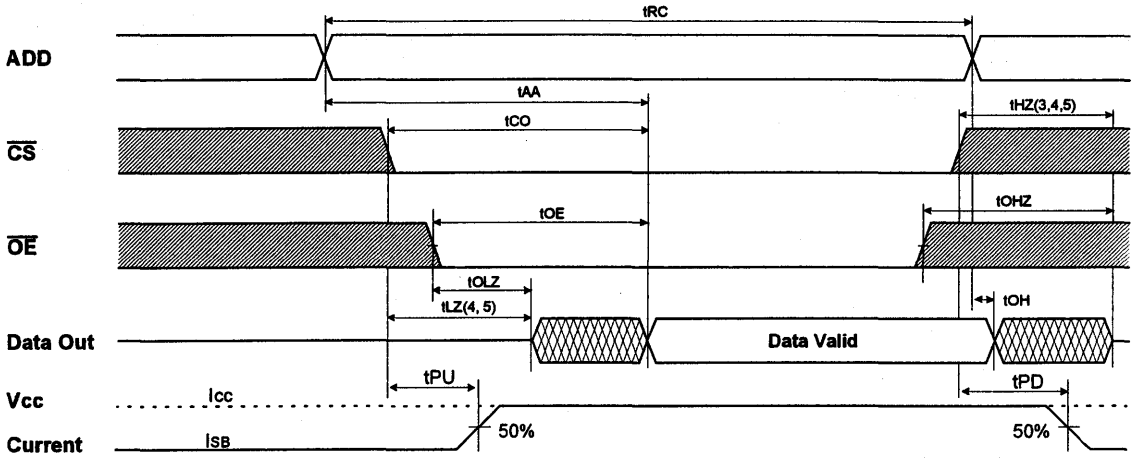
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



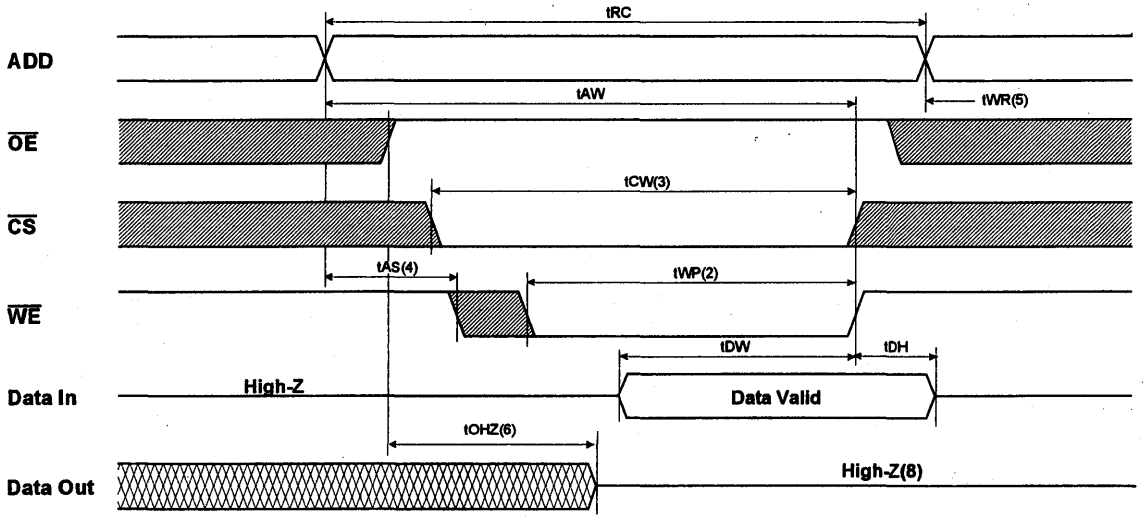
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



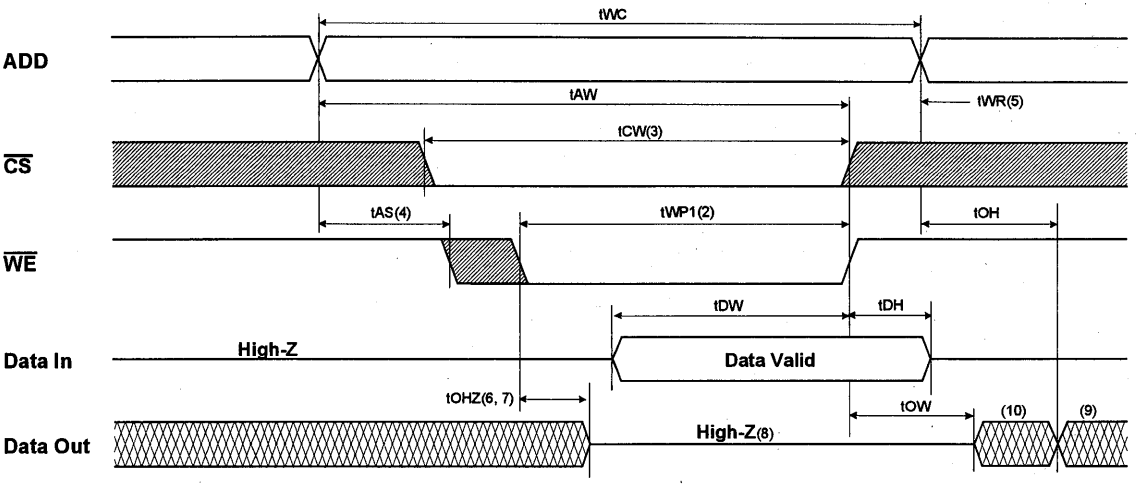
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

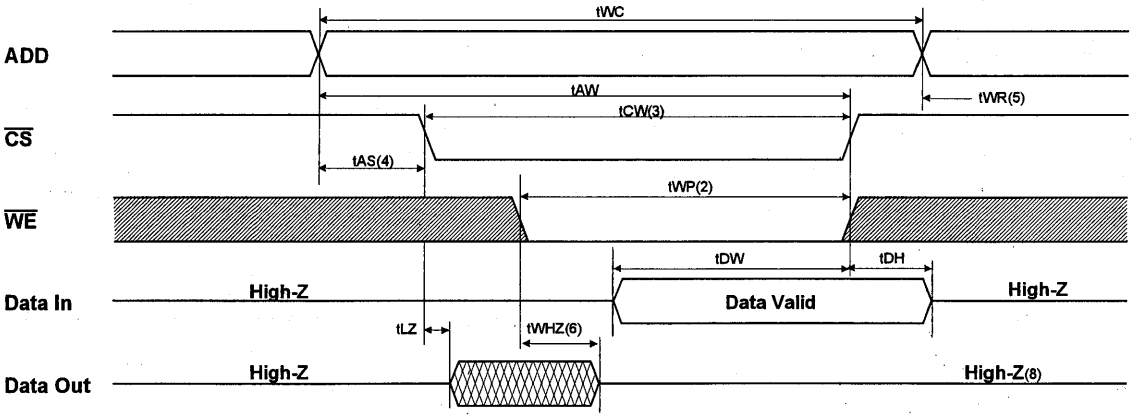
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

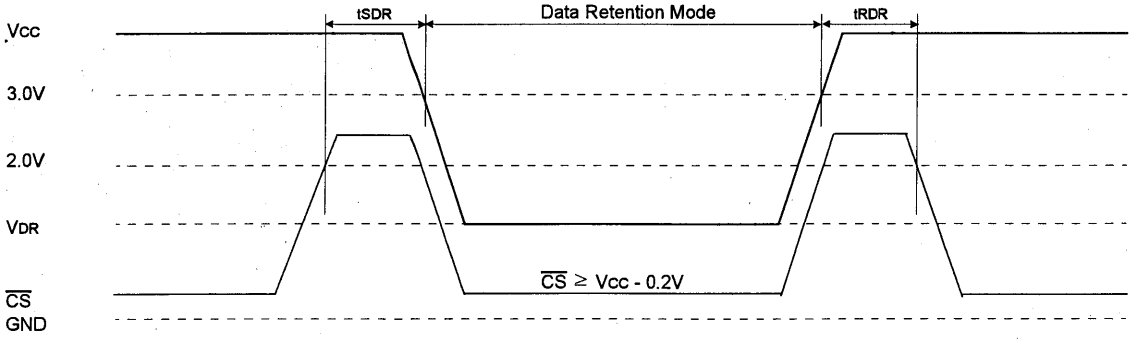
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.4	mA
		V_{CC} = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.3	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



256K x 4 Bit(with $\overline{OE}$) High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 12, 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 20mA(Max.)
  - (CMOS) : 5mA(Max.)
  - 0.5mA(Max.) ; L-ver. only
  - Operating KM64V1003A/AL - 12 : 130mA(Max.)
  - KM64V1003A/AL - 15 : 125mA(Max.)
  - KM64V1003A/AL - 17 : 125mA(Max.)
  - KM64V1003A/AL - 20 : 120mA(Max.)
- Single 3.3V±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM64V1003A/ALJ : 32-SOJ-400
  - KM64V1003A/ALT : 32-TSOP2-400F

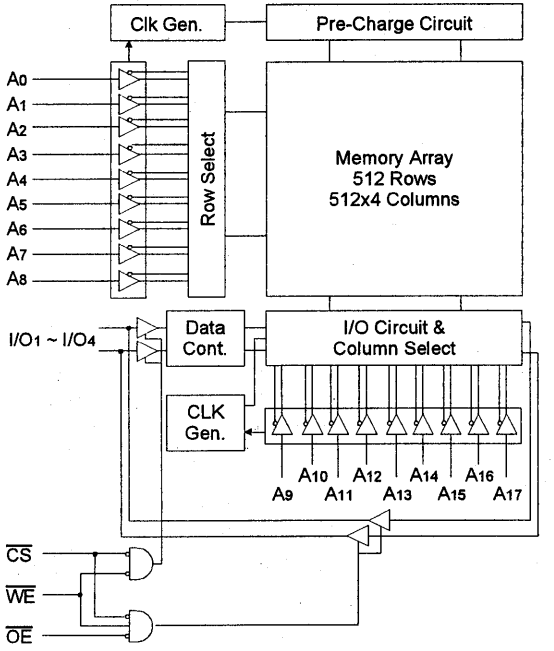
GENERAL DESCRIPTION

The KM64V1003A/AL is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM64V1003A/AL uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64V1003A/AL is packaged in a 400 mil 32-pin plastic SOJ or TSOP2 forward.

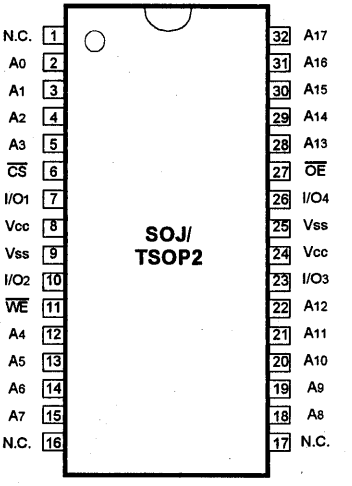
ORDERING INFORMATION

KM64V1003A/AL -12/15/17/20	Commercial Temp.
KM64V1003AI/ALI -12/15/17/20	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 5.5	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_A	0 to 70	°C
	Industrial	T_A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70°C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	130	mA
			15ns	-	125	
			17ns	-	125	
			20ns	-	120	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	20	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	5	mA
			L-Ver.	-	0.5	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

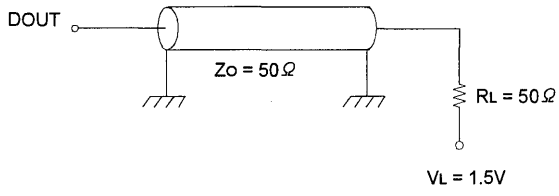
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 3.3V±0.3V, unless otherwise noted.)

TEST CONDITIONS

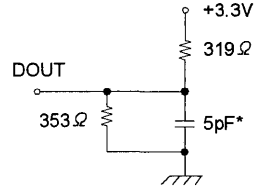
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64V1003A/AL-12		KM64V1003A/AL-15		KM64V1003A/AL-17		KM64V1003A/AL-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	17	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	12	-	15	-	17	-	20	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

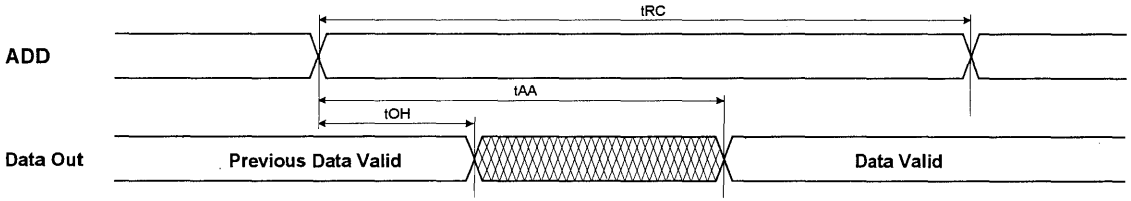
WRITE CYCLE

Parameter	Symbol	KM64V1003A/ AL-12		KM64V1003A/ AL-15		KM64V1003A/ AL-17		KM64V1003A/ AL-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	12	-	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

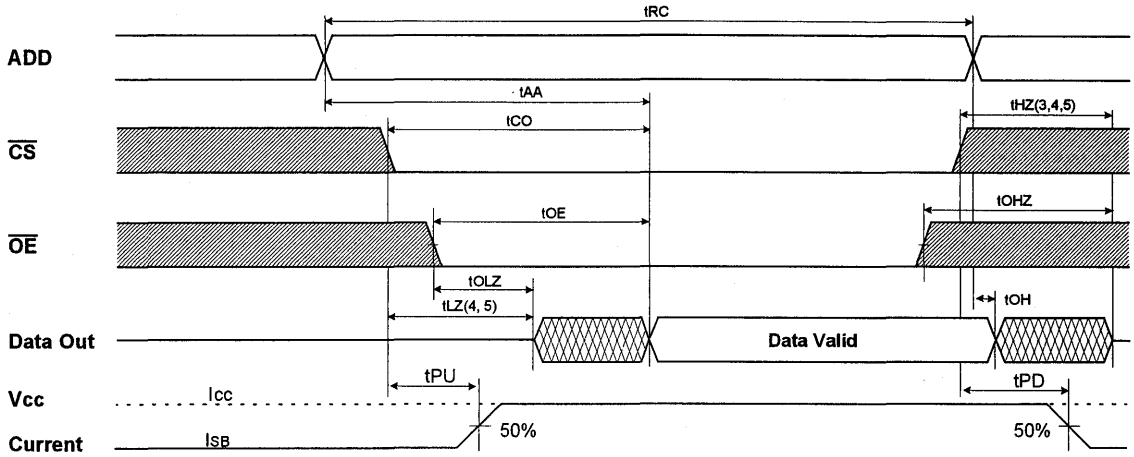
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



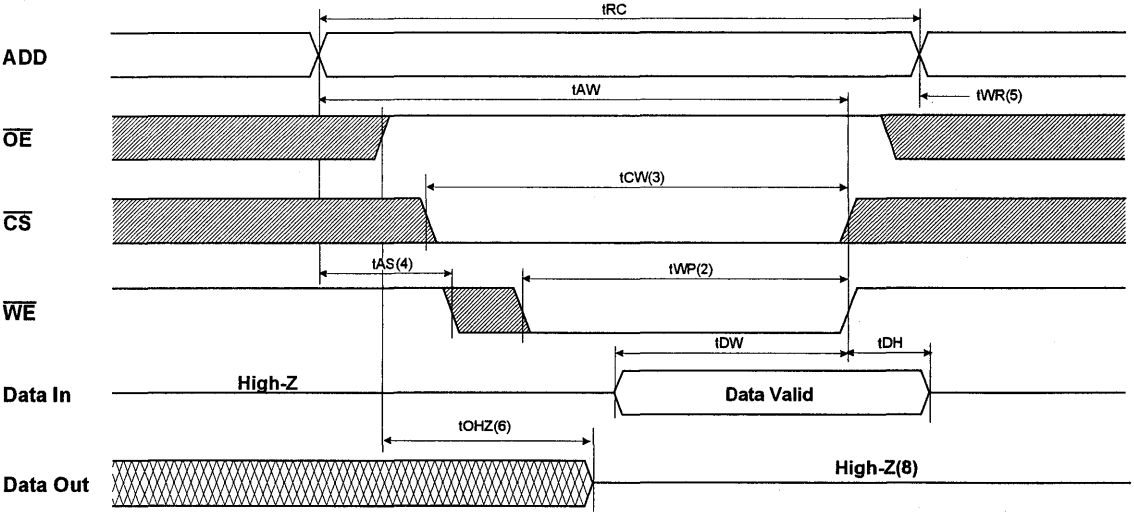
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



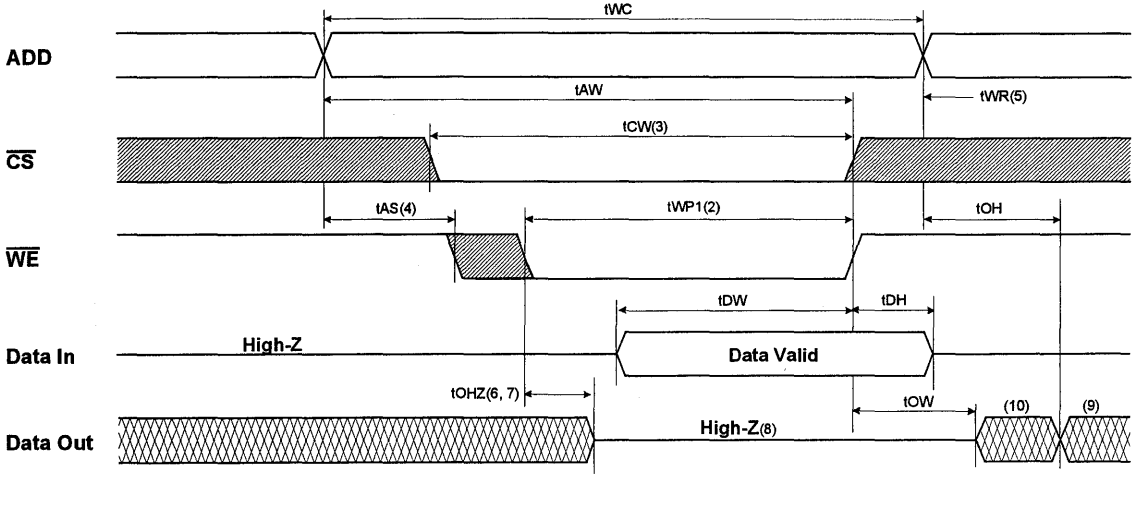
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

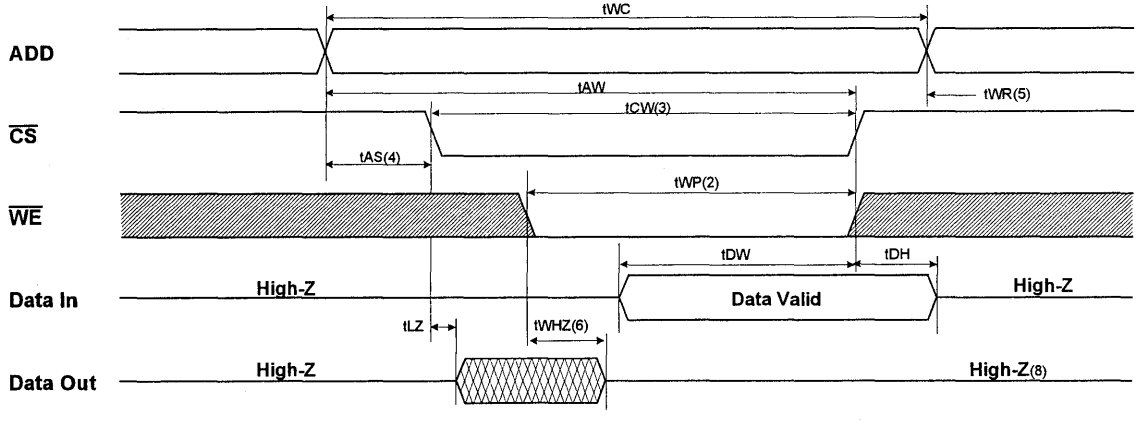
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

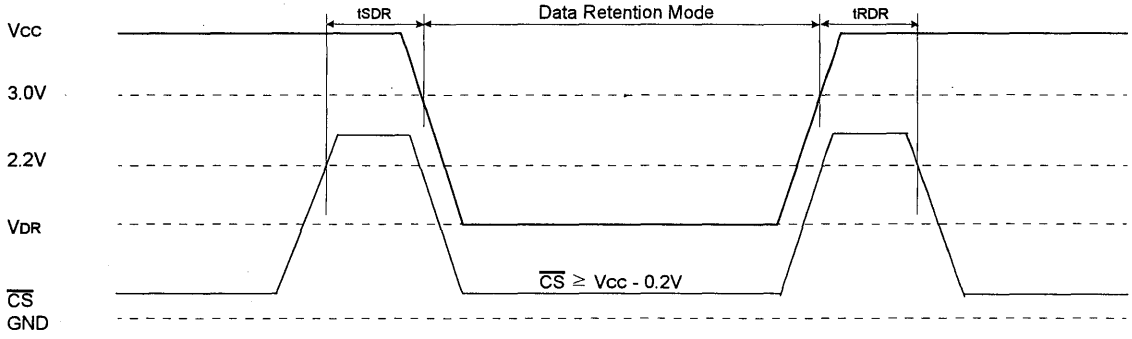
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	3.6	V
Data Retention Current	I_{DR}	Vcc = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.5	mA
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



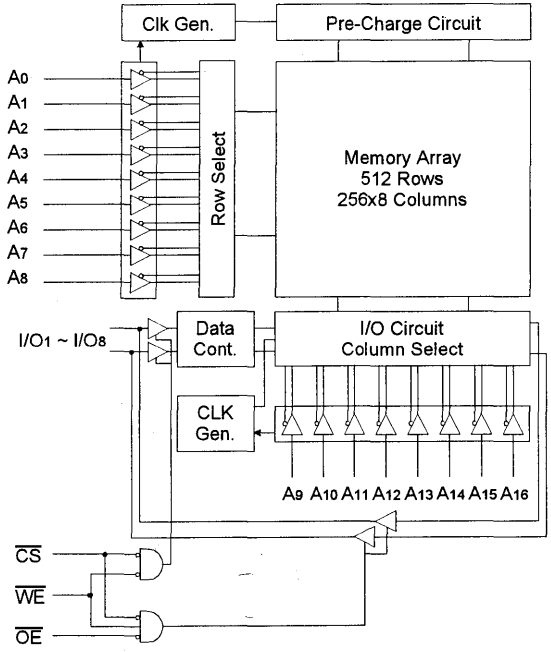
SAMSUNG ELECTRONICS

128K x 8 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 8,10,12ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30mA(Max.)
  - (CMOS) : 5mA(Max.)
  - 0.5mA(Max.) - L-Ver. only
  - Operating KM68V1002B/BL - 8 : 160mA(Max.)
  - KM68V1002B/BL - 10 : 150mA(Max.)
  - KM68V1002B/BL - 12 : 140mA(Max.)
- Single 3.3V ±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM68V1002B/BLJ : 32-SOJ-400
  - KM68V1002B/BLSJ : 32-SOJ-300
  - KM68V1002B/BLT: 32-TSOP2-400F

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

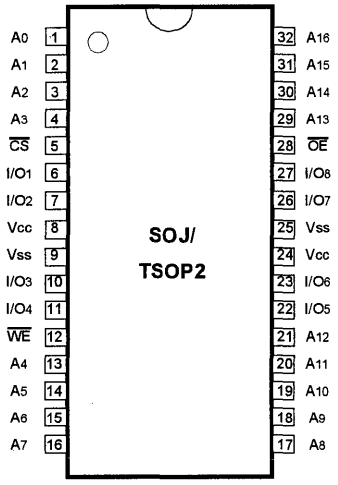
The KM68V1002B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM68V1002B/BL uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V1002B/BL is packaged in a 400/300 mil 32-pin plastic SOJ or TSOP2 forward.

2

ORDERING INFORMATION

KM68V1002B/BL -8/10/12	Commercial Temp.
KM68V1002BI/BLI -8/10/12	Industrial Temp.

PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 5.5	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.0	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤6ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤6ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	8ns	-	160	mA
			10ns	-	150	
			12ns	-	140	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	30	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	5	mA
			L-Ver.	-	0.5	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

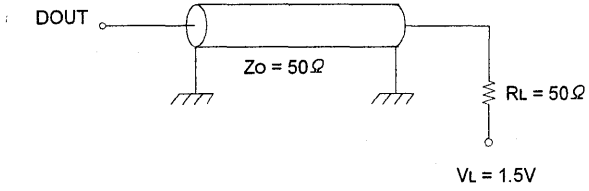
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 3.3V±0.3V, unless otherwise noted.)

TEST CONDITIONS

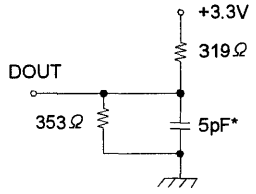
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68V1002B/BL-8		KM68V1002B/BL-10		KM68V1002B/BL-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	8	-	10	-	12	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

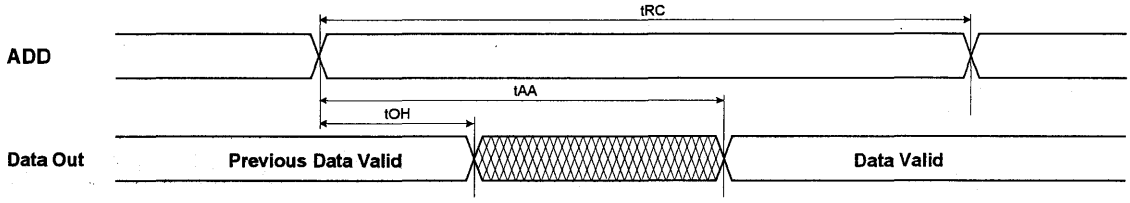
WRITE CYCLE

Parameter	Symbol	KM68V1002B/BL-8		KM68V1002B/BL-10		KM68V1002B/BL-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	8	-	10	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

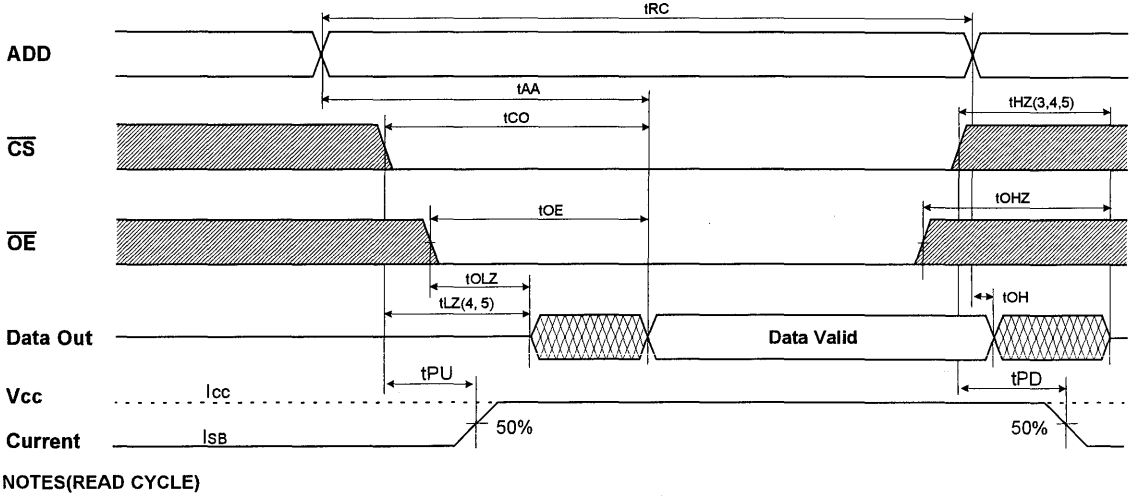
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



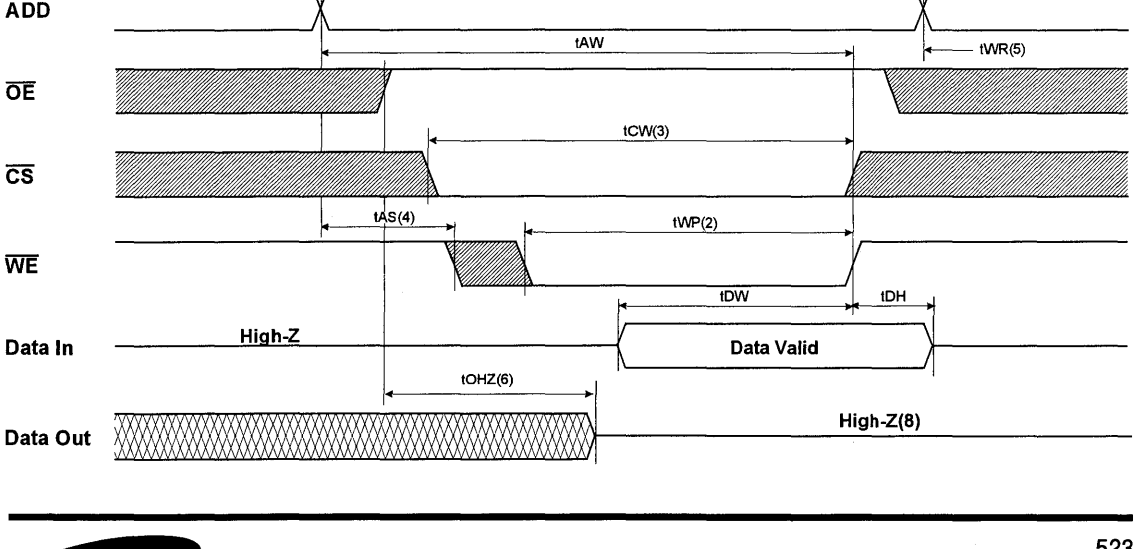
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



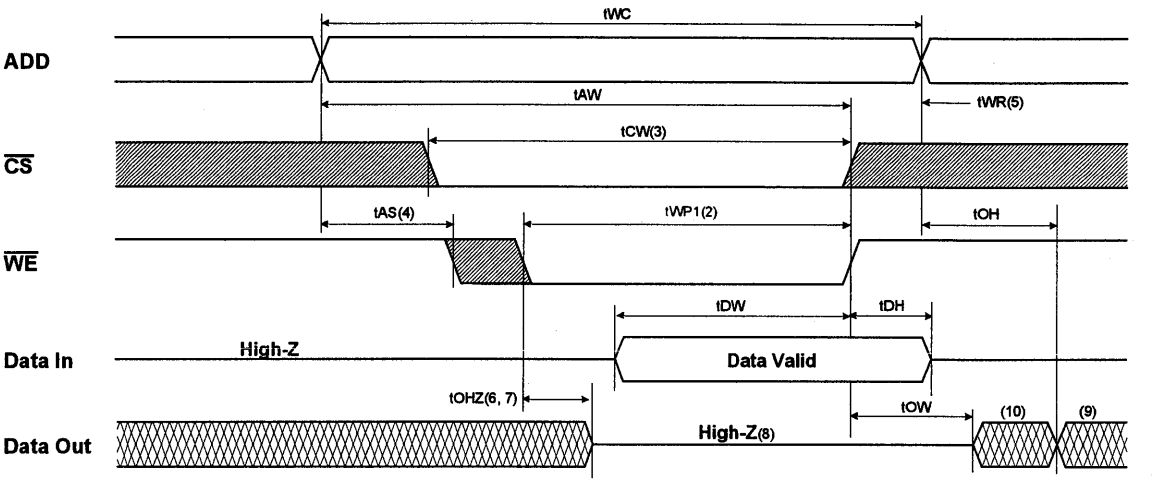
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

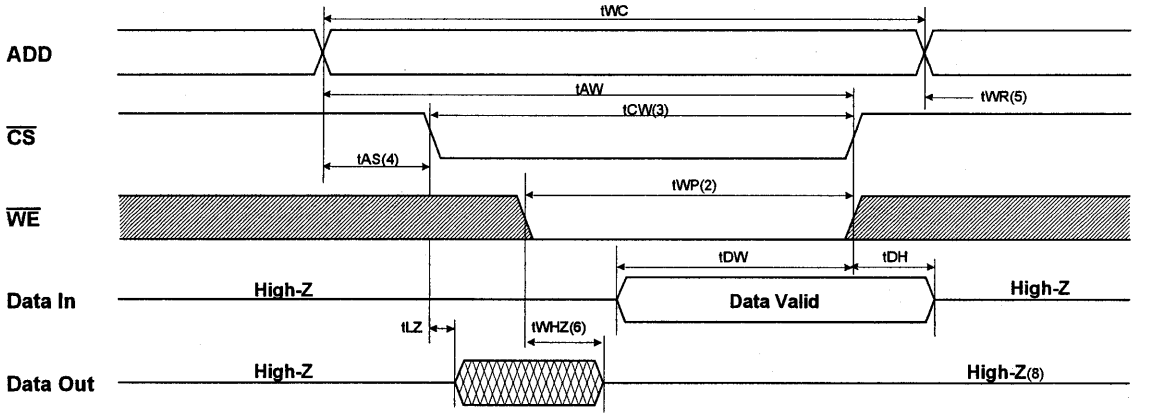
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

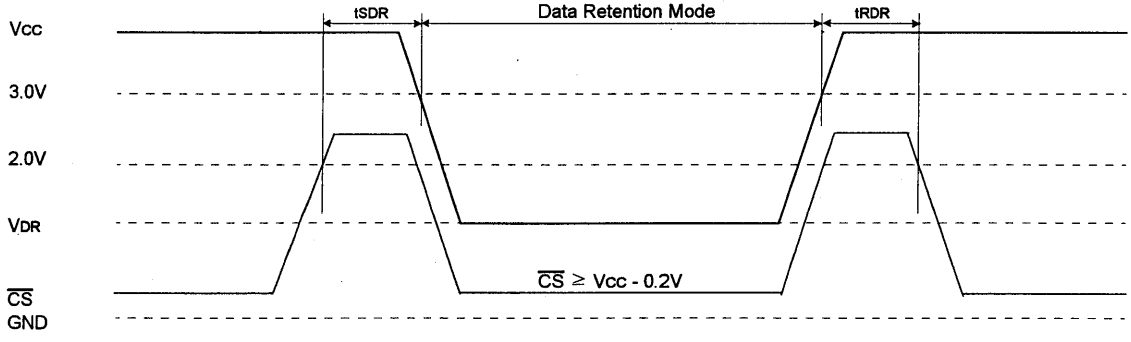
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.4	mA
		V_{CC} = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.3	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)

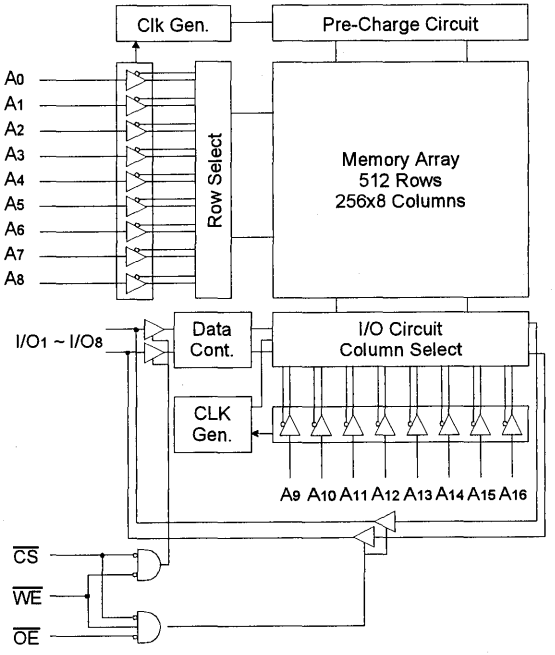


128K x 8 Bit High-Speed CMOS Static RAM(3.3V Operating)

FEATURES

- Fast Access Time 12, 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 20mA(Max.)
  - (CMOS) : 5mA(Max.)
  - 0.5mA(Max.) ; L-ver. only
  - Operating KM68V1002A/AL - 12 : 140mA(Max.)
  - KM68V1002A/AL - 15 : 135mA(Max.)
  - KM68V1002A/AL - 17 : 135mA(Max.)
  - KM68V1002A/AL - 20 : 130mA(Max.)
- Single 3.3V±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM68V1002A/ALJ : 32-SOJ-400
  - KM68V1002A/ALSJ : 32-SOJ-300
  - KM68V1002A/ALT: 32-TSOP2-400F

FUNCTIONAL BLOCK DIAGRAM



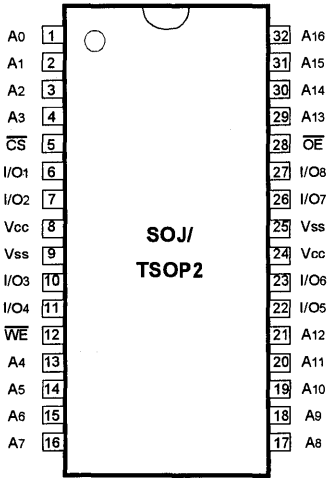
GENERAL DESCRIPTION

The KM68V1002A/AL is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM68V1002A/AL uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V1002A/AL is packaged in a 400/300 mil 32-pin plastic SOJ or TSOP2 forward.

ORDERING INFORMATION

KM68V1002A/AL -12/15/17/20	Commercial Temp.
KM68V1002AI/ALI -12/15/17/20	Industrial Temp.

PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 5.5	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, V_{CC}= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to V_{CC}		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	140	mA
			15ns	-	135	
			17ns	-	135	
			20ns	-	130	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	20	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ V_{CC}-0.2V, V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V	Normal	-	5	mA
			L-Ver.	-	0.5	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

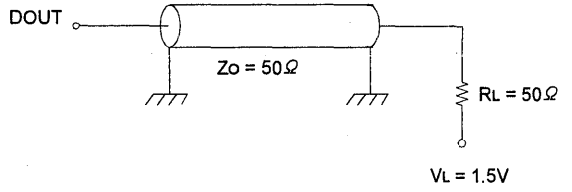
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 3.3V±0.3V, unless otherwise noted.)

TEST CONDITIONS

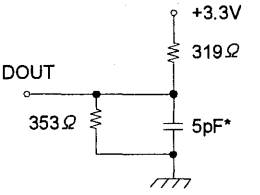
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68V1002A/AL-12		KM68V1002A/AL-15		KM68V1002A/AL-17		KM68V1002A/AL-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	17	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	12	-	15	-	17	-	20	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

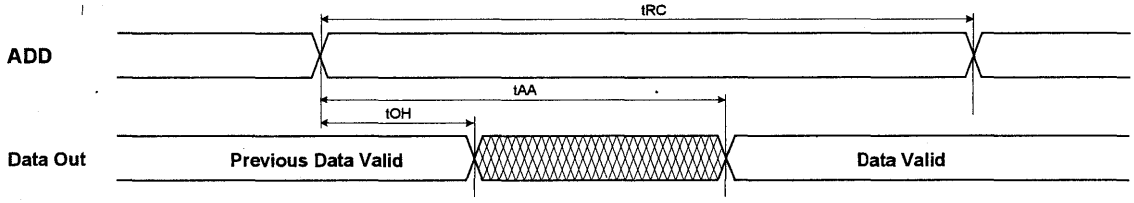
WRITE CYCLE

Parameter	Symbol	KM6161002A/AL-12		KM6161002A/AL-15		KM6161002A/AL-17		KM6161002A/AL-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	12	-	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

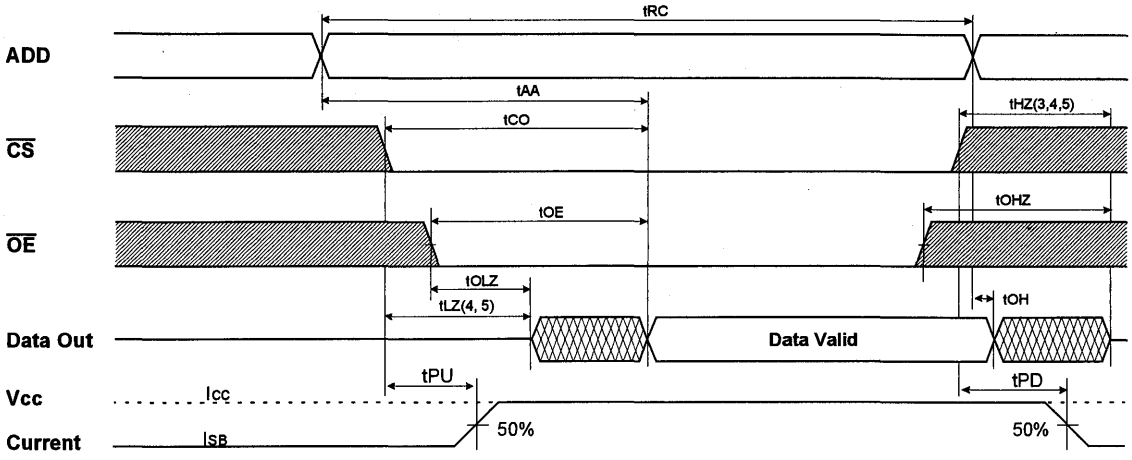
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



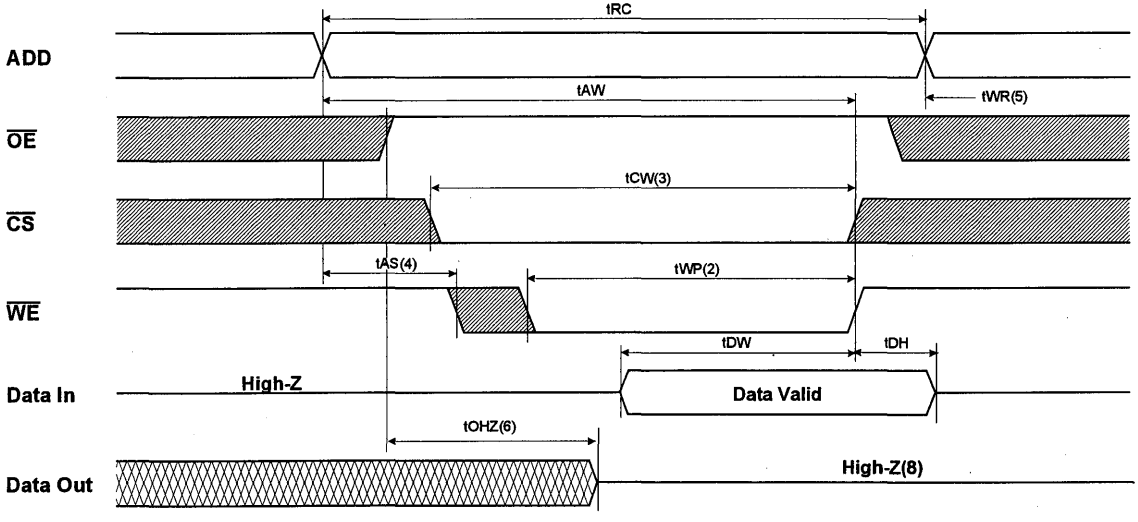
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



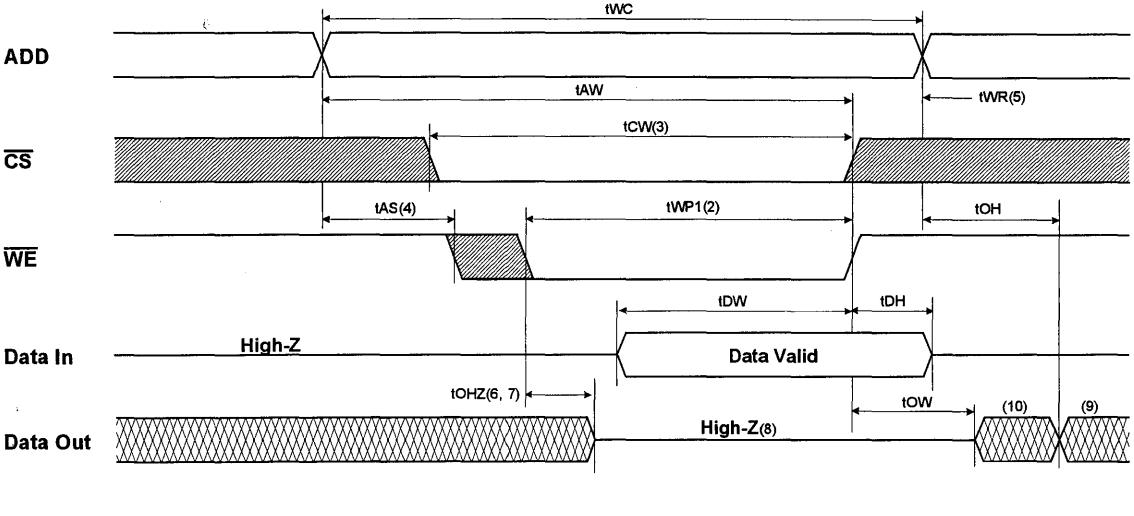
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

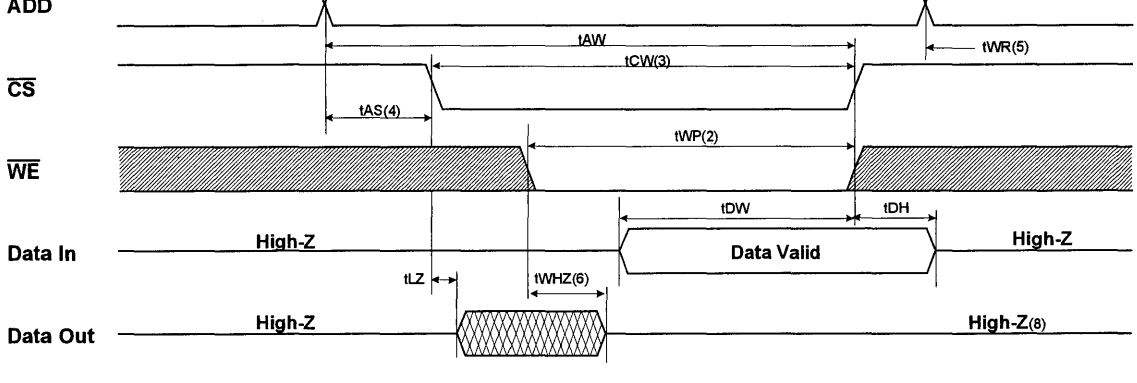
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

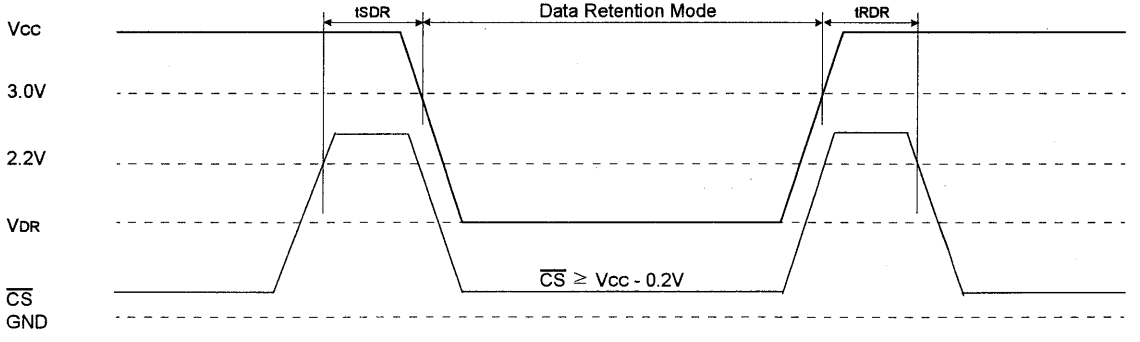
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	3.6	V
Data Retention Current	I_{DR}	Vcc = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.5	mA
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



64K x 16 Bit High-Speed CMOS Static RAM(3.3V Operating)

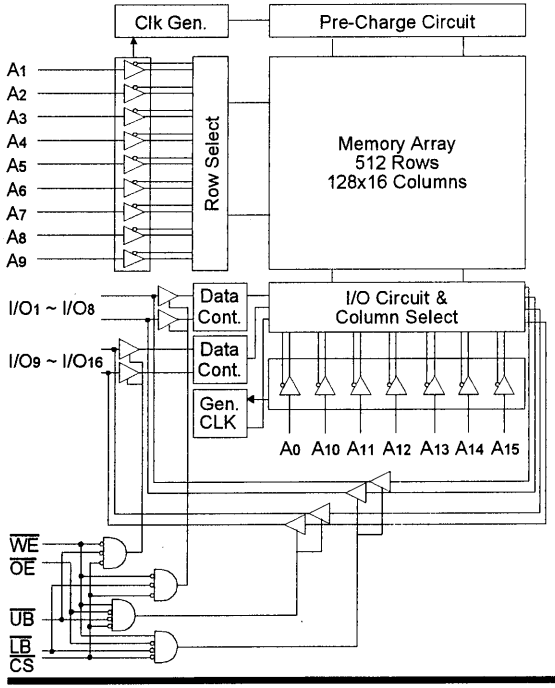
FEATURES

- Fast Access Time 8,10,12ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30mA(Max.)
  - (CMOS) : 5mA(Max.)
  - 0.5mA(Max.) - L-Ver. only
  - Operating KM616V1002B/BL - 8 : 200mA(Max.)
  - KM616V1002B/BL - 10 : 190mA(Max.)
  - KM616V1002B/BL - 12 : 180mA(Max.)
- Single 3.3V ±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O1~ I/O8, $\overline{UB}$: I/O9~ I/O16
- Standard Pin Configuration
  - KM616V1002B/BLJ : 44-SOJ-400
  - KM616V1002B/BLT: 44-TSOP2-400F

ORDERING INFORMATION

KM616V1002B/BL -8/10/12	Commercial Temp.
KM616V1002BI/BLI -8/10/12	Industrial Temp.

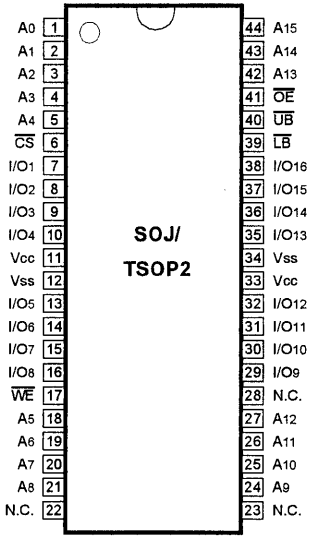
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM616V1002B/BL is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The KM616V1002B/BL uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616V1002B/BL is packaged in a 400mil 44-pin plastic SOJ or TSOP2 forward.

PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 5.5	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.0	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤6ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤6ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	8ns	-	200	mA
			10ns	-	190	
			12ns	-	180	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	30	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	5	mA
			L-Ver.	-	0.5	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

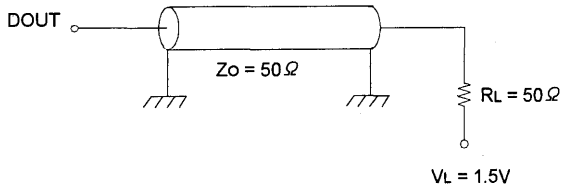
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 3.3V±0.3V, unless otherwise noted.)

TEST CONDITIONS

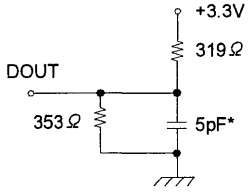
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM616V1002B/BL-8		KM616V1002B/BL-10		KM616V1002B/BL-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	8	-	10	-	12	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

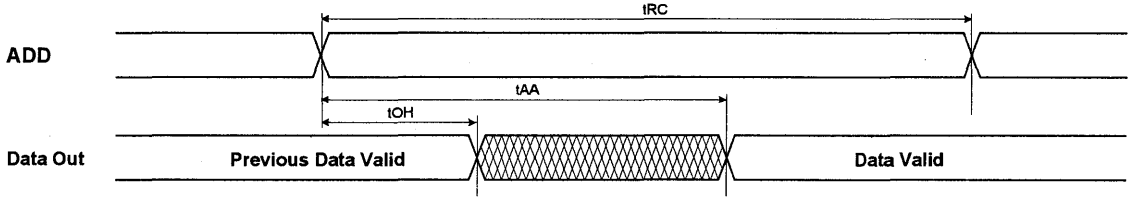
WRITE CYCLE

Parameter	Symbol	KM616V1002B/BL-8		KM616V1002B/BL-10		KM616V1002B/BL-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	8	-	10	-	12	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	8	-	10	-	12	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	6	-	7	-	8	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	ns
Data to Write Time Overlap	tDW	4	-	5	-	6	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

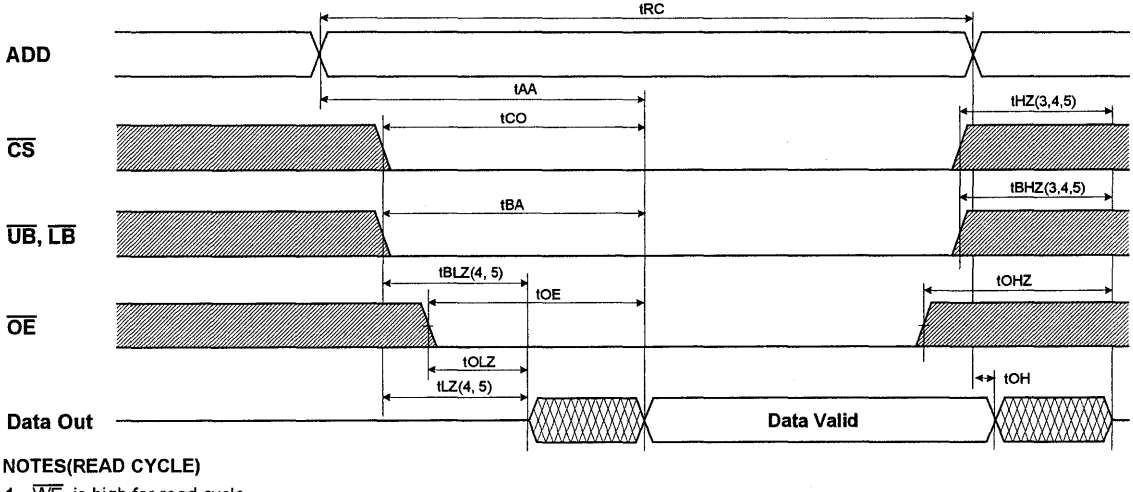
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$\overline{UB}$=$\overline{LB}$=VIL, $\overline{WE}$=VIH)



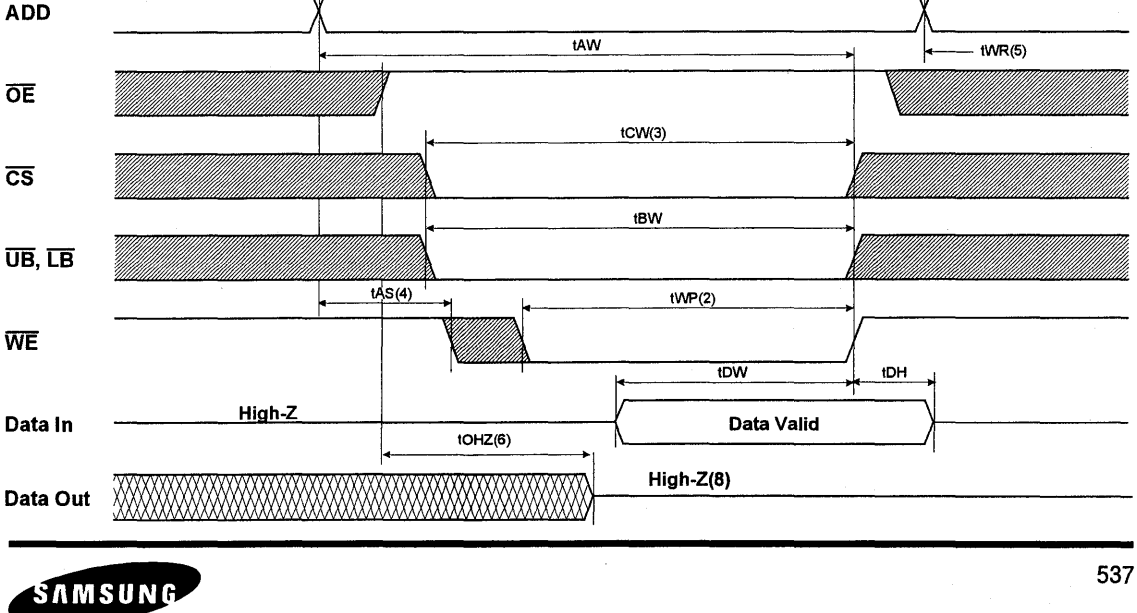
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



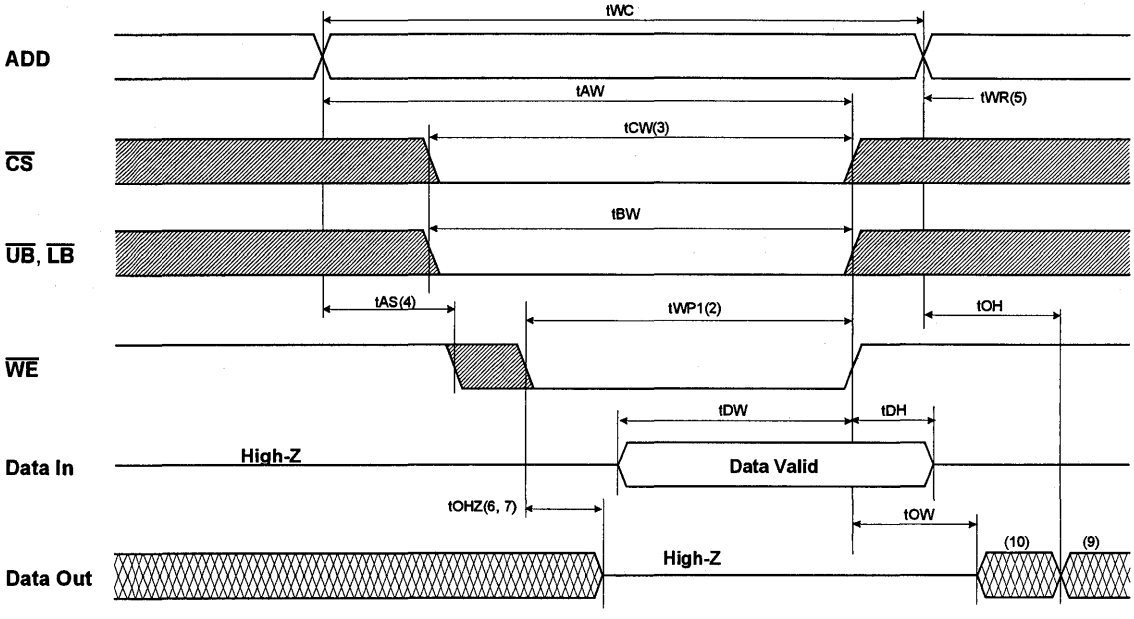
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200㎷ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

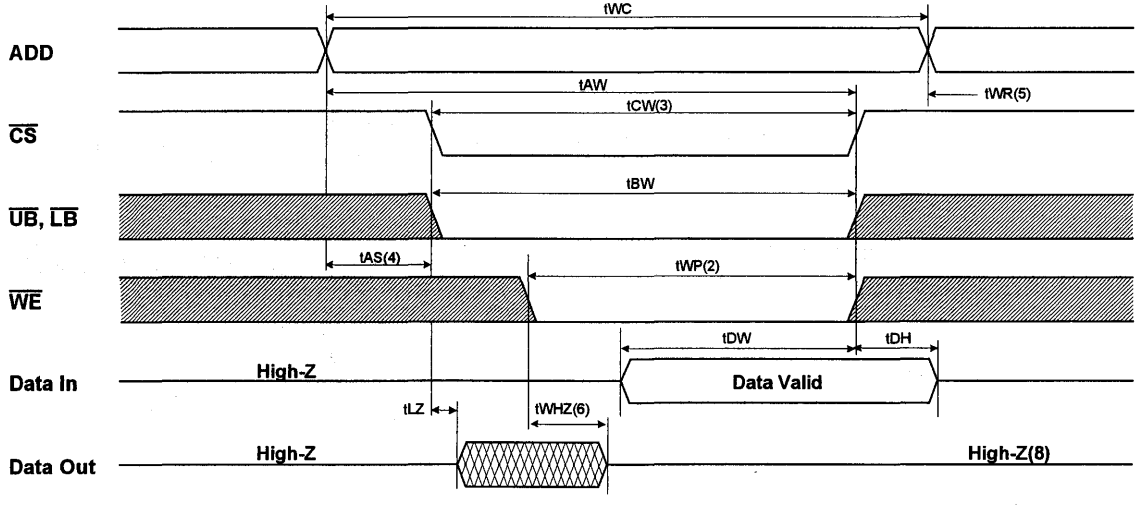
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



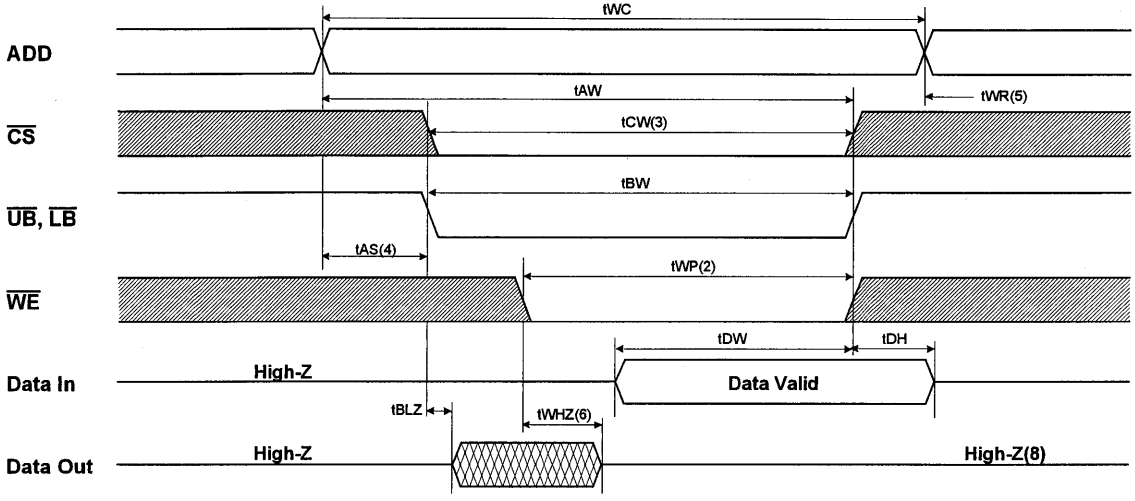
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$. $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z		ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	ICC
L	X	X	H	H				
L	H	L	L	H	Read	DOUT	High-Z	ICC
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	ICC
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

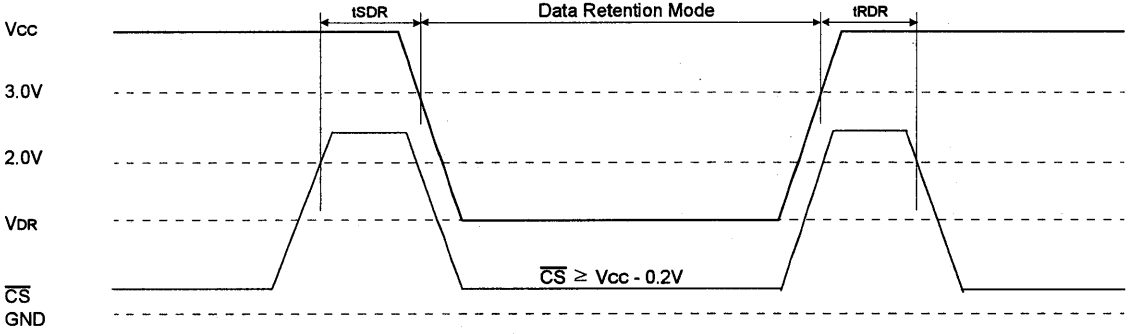
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS* (T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.4	mA
		V_{CC} = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.3	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



64K x 16 Bit High-Speed CMOS Static RAM(3.3V Operating)

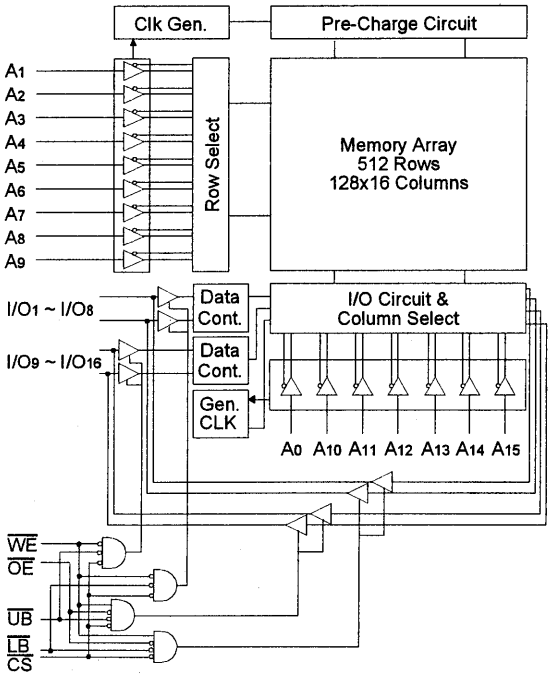
FEATURES

- Fast Access Time 12, 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 20mA(Max.)
  - (CMOS) : 5mA(Max.)
  - 0.5mA(Max.) ; L-ver. only
  - Operating KM616V1002A/AL - 12 : 170mA(Max.)
  - KM616V1002A/AL - 15 : 165mA(Max.)
  - KM616V1002A/AL - 17 : 165mA(Max.)
  - KM616V1002A/AL - 20 : 160mA(Max.)
- Single 3.3V ±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O1~ I/O8, $\overline{UB}$: I/O9~ I/O16
- Standard Pin Configuration
  - KM616V1002A/ALJ : 44-SOJ-400
  - KM616V1002A/ALT: 44-TSOP2-400F

ORDERING INFORMATION

KM616V1002A/AL -12/15/17/20	Commercial Temp.
KM616V1002AI/ALI -12/15/17/20	Industrial Temp.

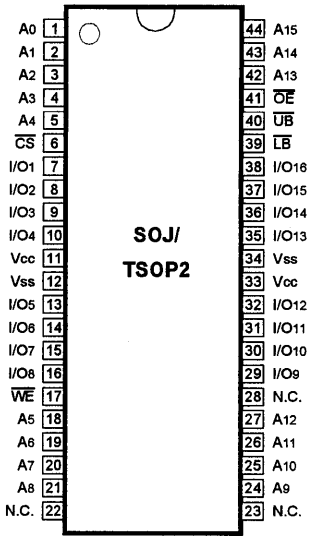
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM616V1002A/AL is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The KM616V1002A/AL uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616V1002A/AL is packaged in a 400mil 44-pin plastic SOJ or TSOP2 forward.

PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 5.5	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	170	mA
			15ns	-	165	
			17ns	-	165	
			20ns	-	160	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	20	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	5	mA
			L-Ver.	-	0.5	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

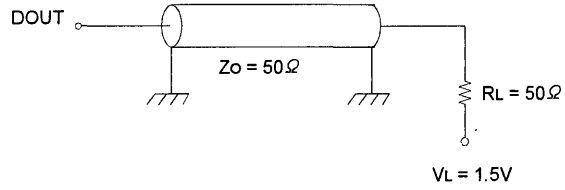
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} = 3.3V±0.3V, unless otherwise noted.)

TEST CONDITIONS

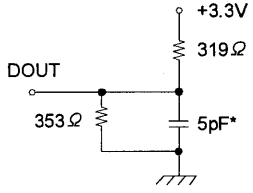
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM616V1002A/AL-12		KM616V1002A/AL-15		KM616V1002A/AL-17		KM616V1002A/AL-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	17	-	20	-	ns
Address Access Time	tAA	-	12	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	12	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	6	-	7	-	8	-	9	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	6	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	6	0	7	0	8	0	9	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	6	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

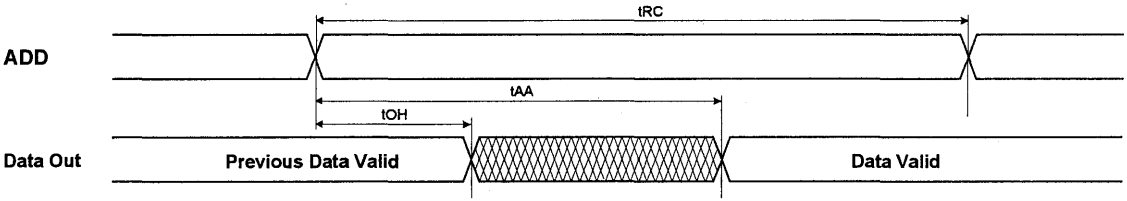
WRITE CYCLE

Parameter	Symbol	KM616V1002A/AL-12		KM616V1002A/AL-15		KM616V1002A/AL-17		KM616V1002A/AL-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	8	-	10	-	11	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8	-	10	-	11	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	12	-	15	-	17	-	20	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	8	-	10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	6	-	7	-	8	-	9	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

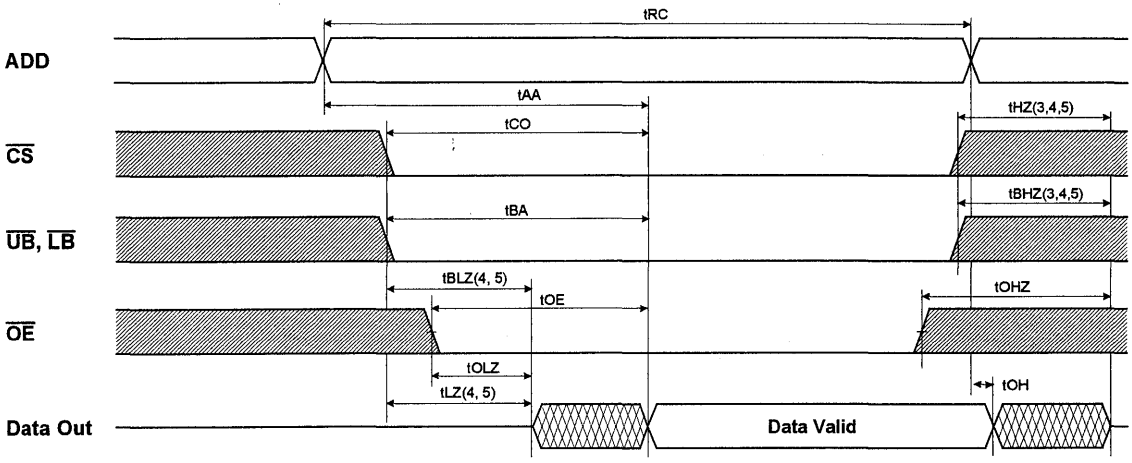
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$\overline{UB}$=$\overline{LB}$=V_{IL}, $\overline{WE}$=V_{IH})



SAMSUNG ELECTRONICS

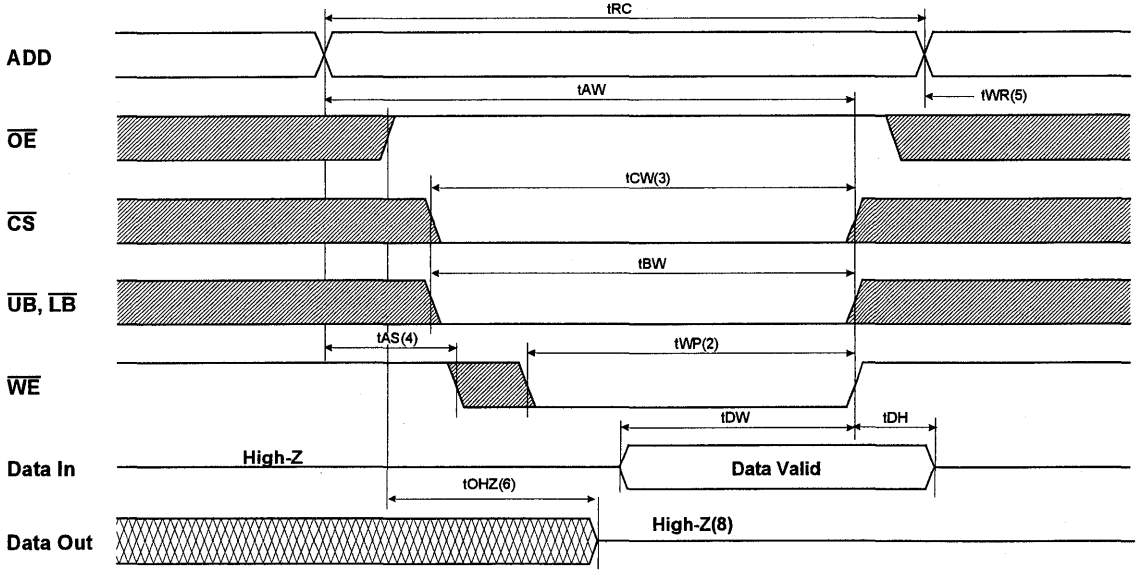
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



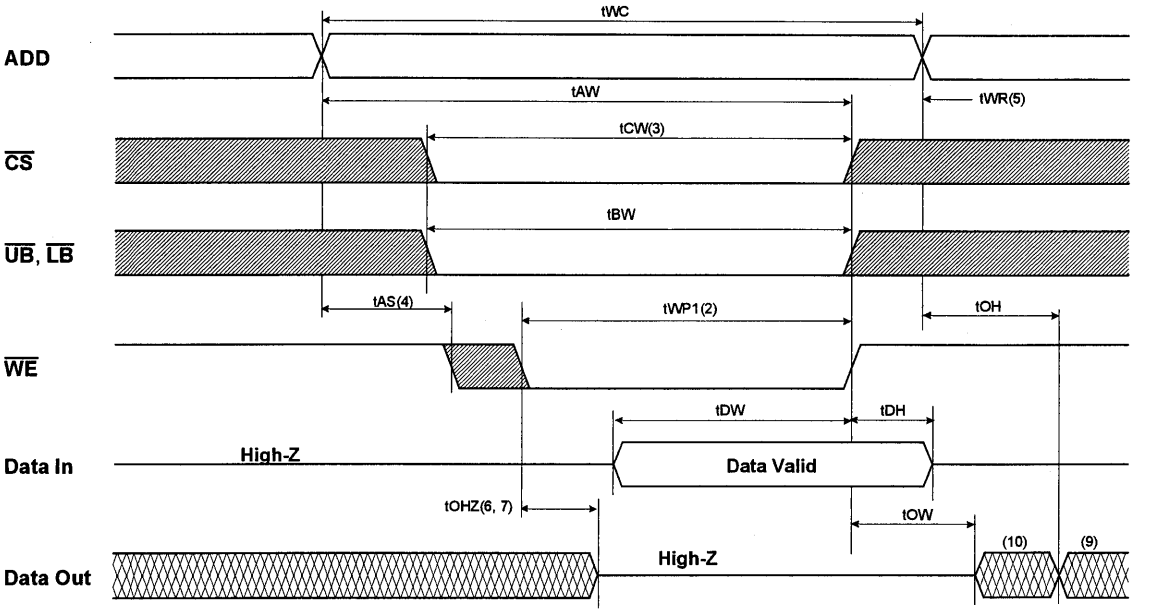
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

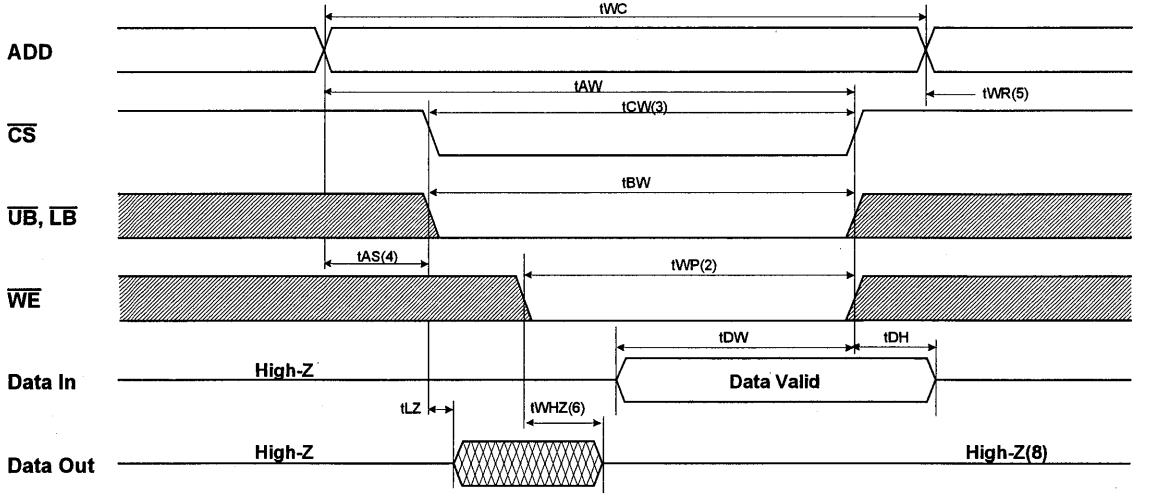
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



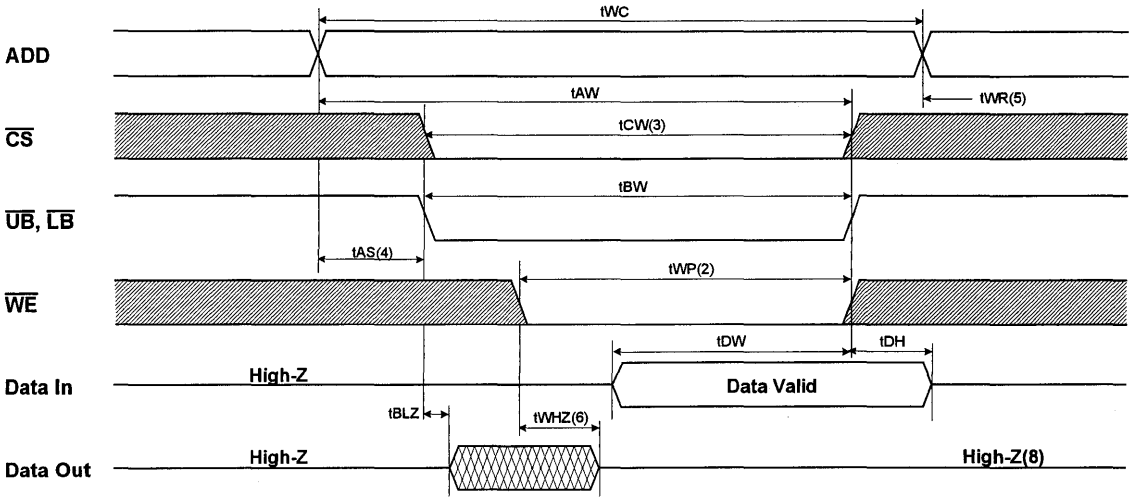
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$. $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z		ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	ICC
L	X	X	H	H				
L	H	L	L	H	Read	DOUT	High-Z	ICC
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	ICC
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

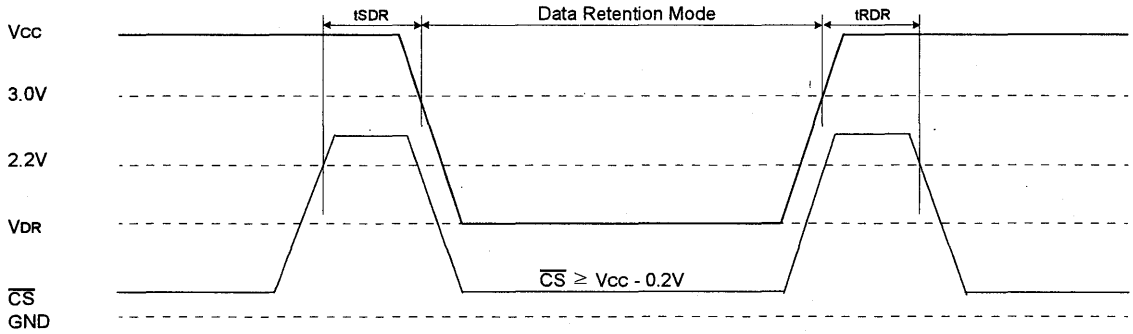
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.5	mA
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



SAMSUNG ELECTRONICS

4M High Speed SRAM (3.3V Operation)

1M x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM(3.3V Operating)

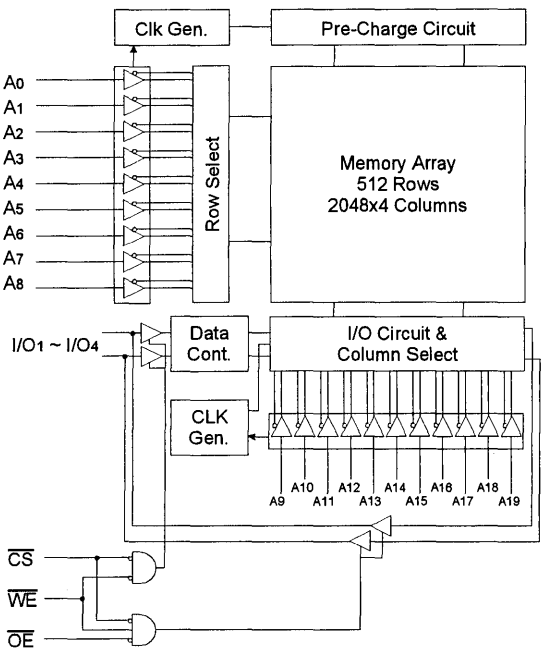
FEATURES

- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 10mA(Max.)
  - 1mA(Max.)- L-Ver.
  - Operating KM64V4002B/BL - 10 : 160mA(Max.)
  - KM64V4002B/BL - 12 : 150mA(Max.)
  - KM64V4002B/BL - 15 : 140mA(Max.)
- Single 3.3V±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage : 2V(Min.) - L-Ver. Only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM64V4002B/BLJ : 32-SOJ-400
  - KM64V4002B/BLT : 32-TSOP2-400F

ORDERING INFORMATION

KM64V4002B/BL -10/12/15	Commercial Temp.
KM64V4002B/BLI -10/12/15	Industrial Temp.

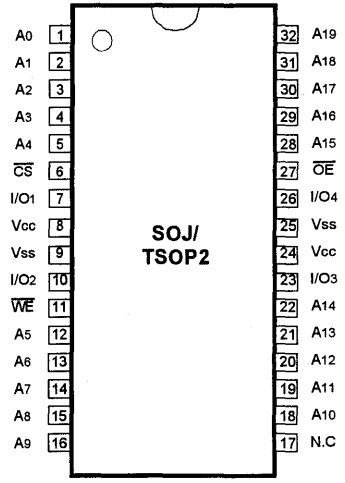
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM64V4002B/BL is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM64V4002B/BL uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64V4002B/BL is packaged in a 400 mil 32-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 5.5	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.0	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤8ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	10ns	-	160	mA
			12ns	-	150	
			15ns	-	140	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	10	mA
			L-Ver.	-	1	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

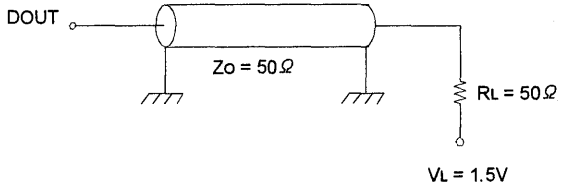
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} =3.3V±0.3V, unless otherwise noted.)

TEST CONDITIONS

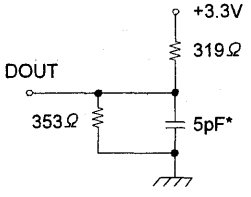
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64V4002B/BL-10		KM64V4002B/BL-12		KM64V4002B/BL-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	10	-	12	-	15	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

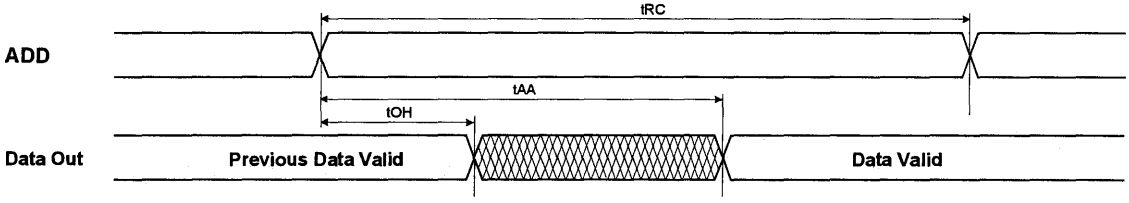
WRITE CYCLE

Parameter	Symbol	KM64V4002B/BL-10		KM64V4002B/BL-12		KM64V4002B/BL-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	10	-	12	-	15	-	ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	10	-	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	5	0	6	0	7	ns
Data to Write Time Overlap	tDW	5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

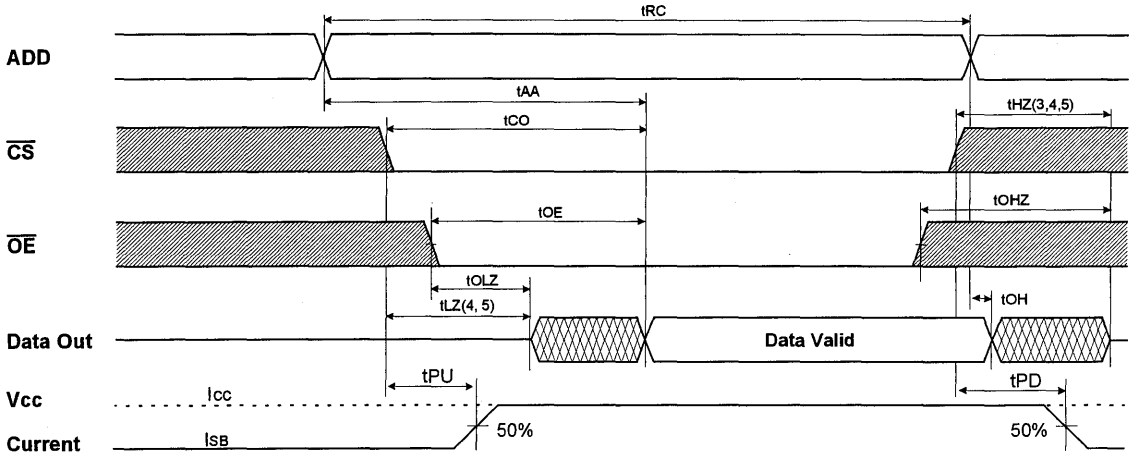
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



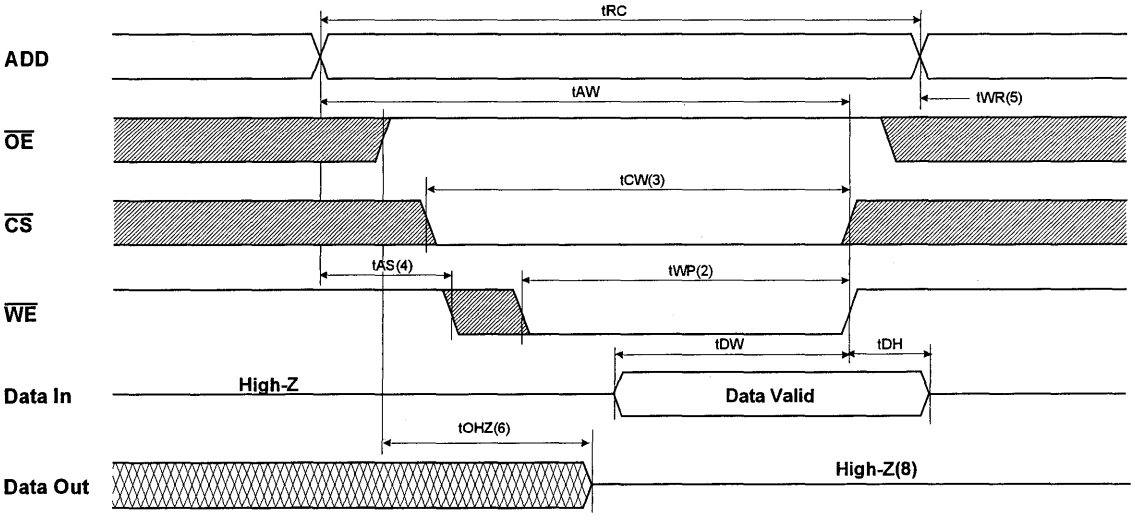
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

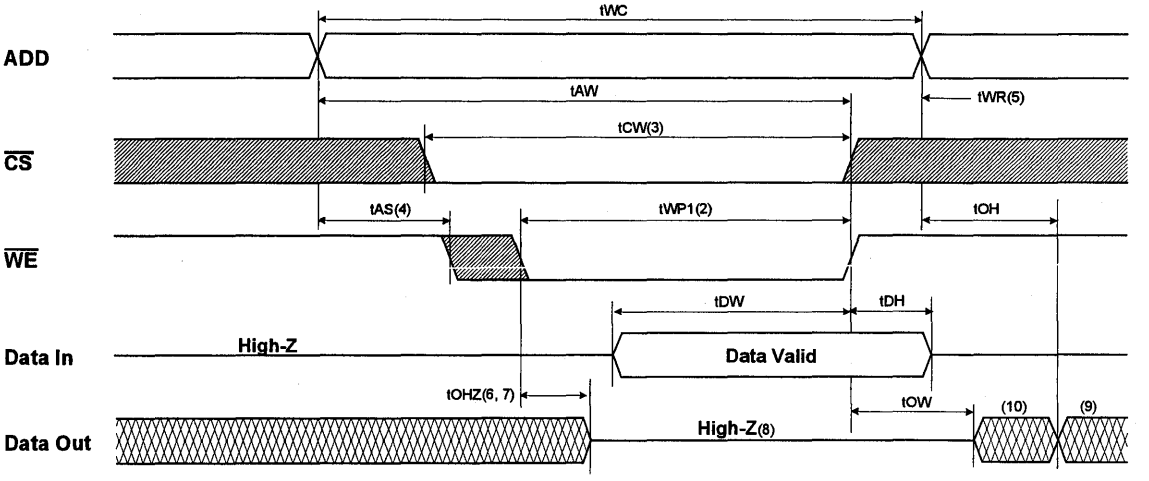
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

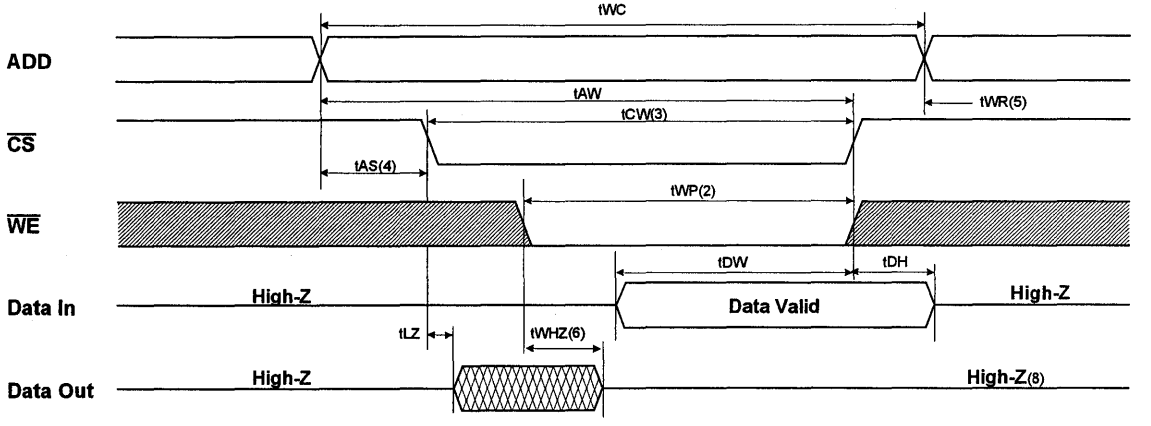


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

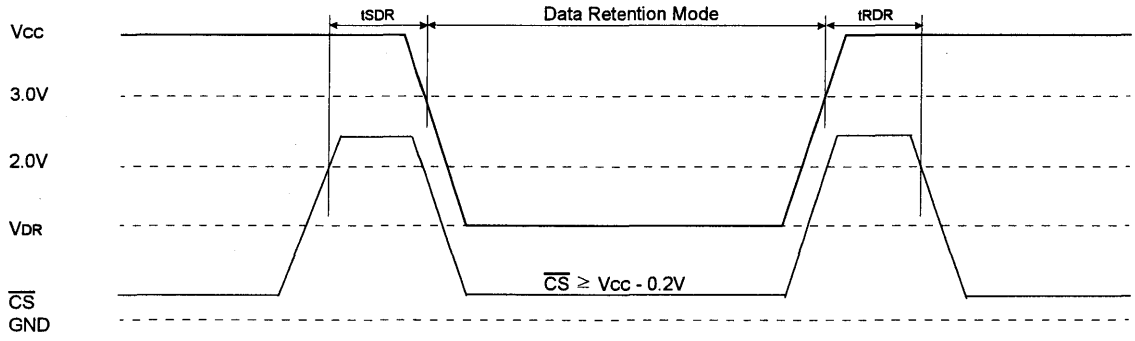
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.9	mA
		V_{CC} = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.7	mA
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



1M x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM(3.3V Operating)

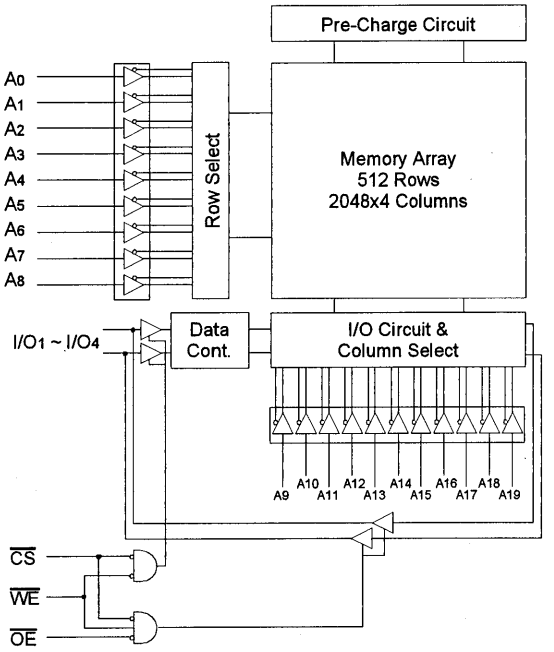
FEATURES

- Fast Access Time 12,13,15 ns (Max.)
- Low Power Dissipation
  - Standby (TTL) : 60mA(Max.)
  - (CMOS) : 30mA(Max.)
  - Operating KM64BV4002 - 12 : 160mA(Max.)
  - KM64BV4002 - 13 : 155mA(Max.)
  - KM64BV4002 - 15 : 150mA(Max.)
- Single 3.3V+10%/-5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM64BV4002 : 32-SOJ-400

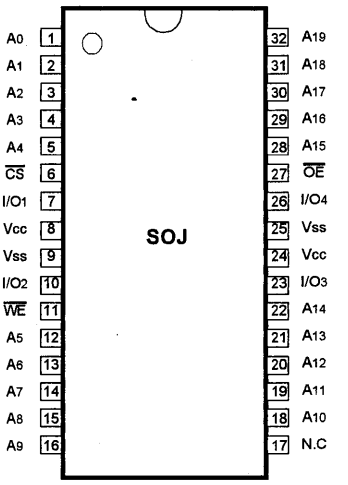
GENERAL DESCRIPTION

The KM64BV4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM64BV4002 uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64BV4002 is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, V_{CC}= 3.3V+10%/-5%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to V_{CC}		-10	10	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	160	mA
			13ns	-	155	
			15ns	-	150	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	60	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ V_{CC}-0.2V, V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V		-	30	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

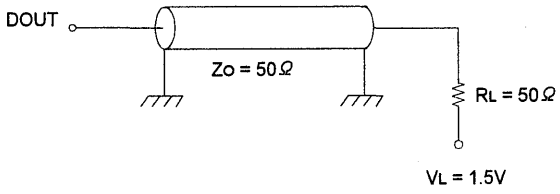
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} =3.3V +10%/-5%, unless otherwise noted.)

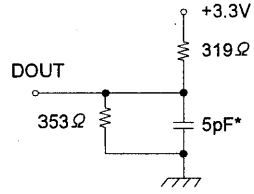
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64BV4002-12		KM64BV4002-13		KM64BV4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	6	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

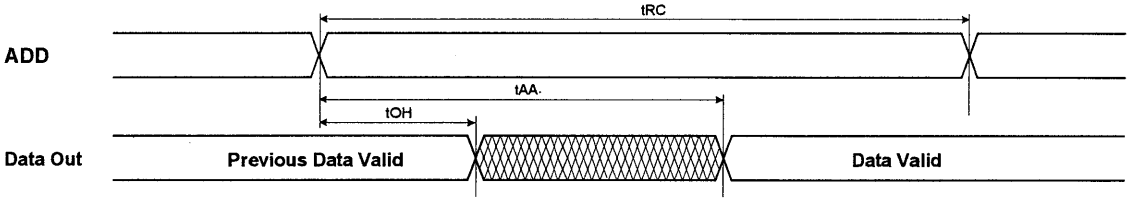
WRITE CYCLE

Parameter	Symbol	KM64BV4002-12		KM64BV4002-13		KM64BV4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	13	-	15	-	ns
Chip Select to End of Write	tCW	9	-	10	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	10	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	9	-	10	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	10	-	11	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6.5	0	7	0	7.5	ns
Data to Write Time Overlap	tDW	7	-	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

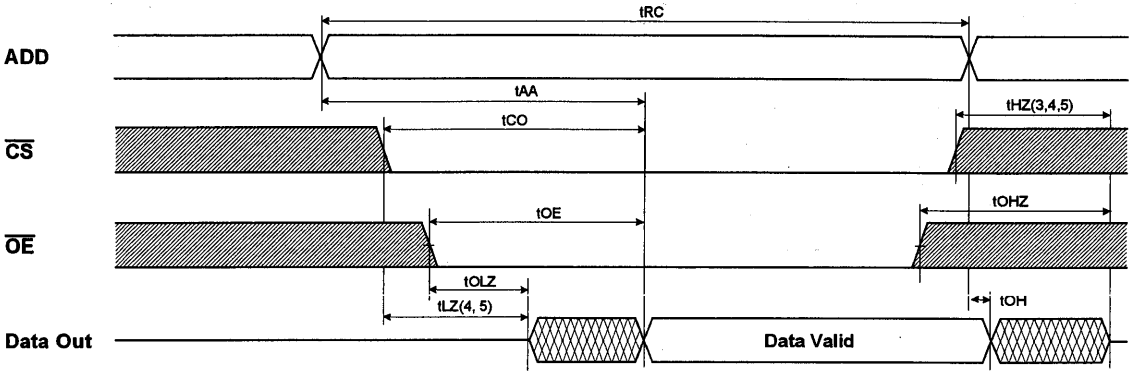
2

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



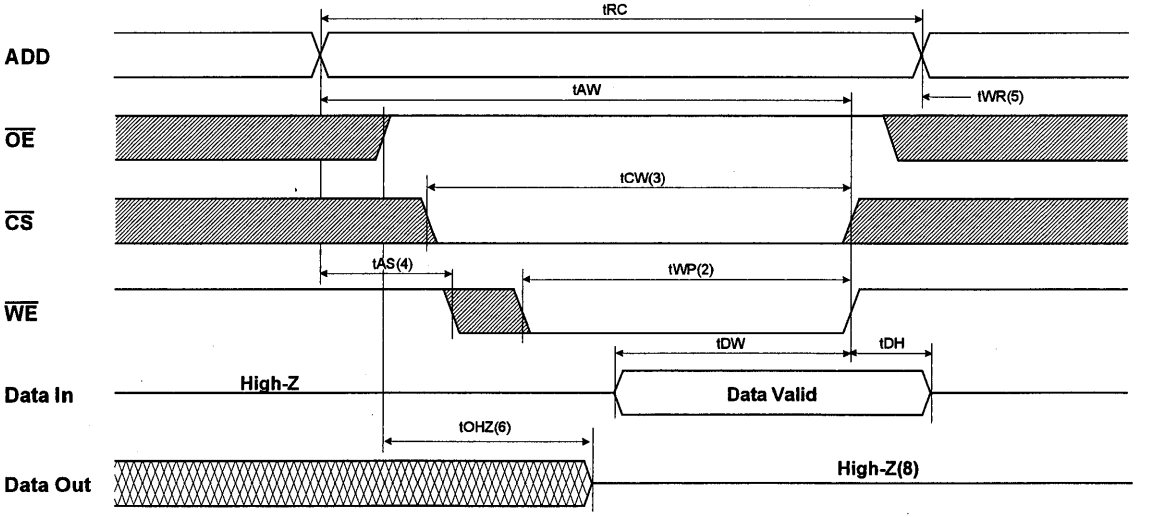
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



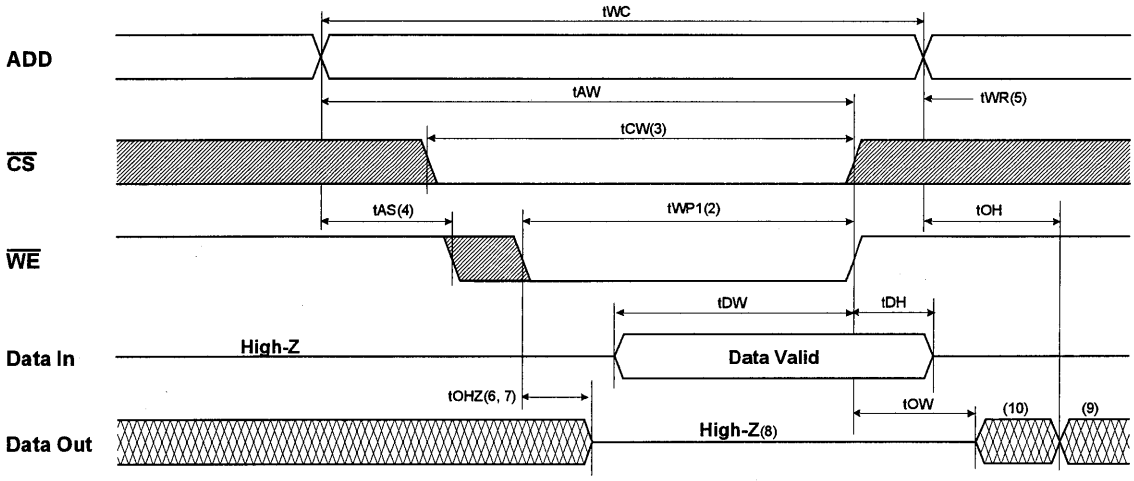
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

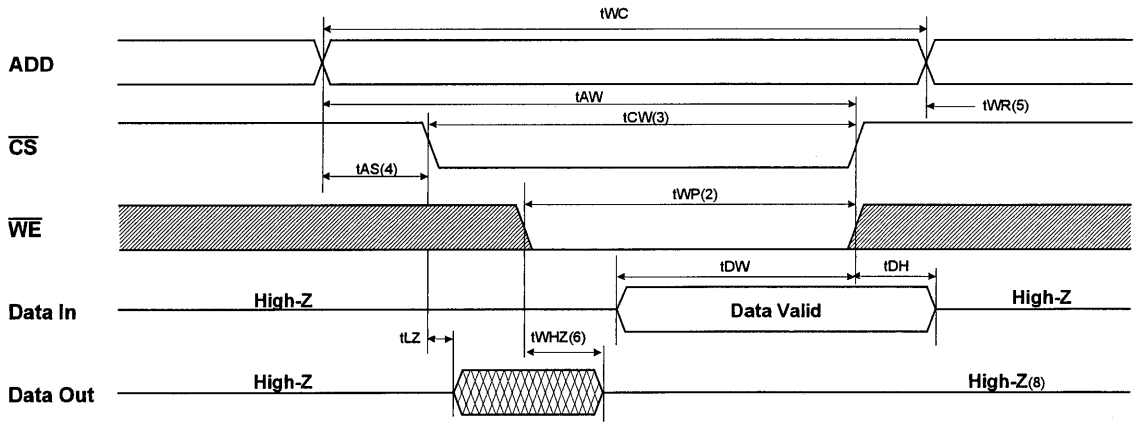
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

1M x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM

FEATURES

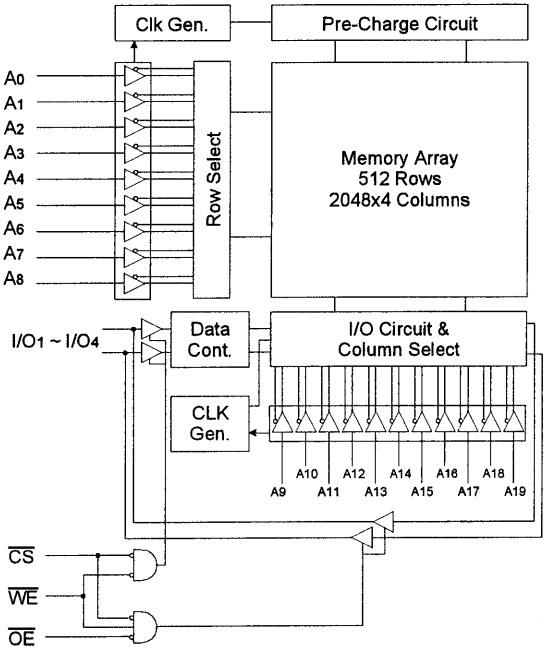
- Fast Access Time 15,17,20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM64V4002A - 15 : 140mA(Max.)
  - KM64V4002A - 17 : 135mA(Max.)
  - KM64V4002A - 20 : 130mA(Max.)
- Single 3.3V±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM64V4002AJ : 32-SOJ-400

GENERAL DESCRIPTION

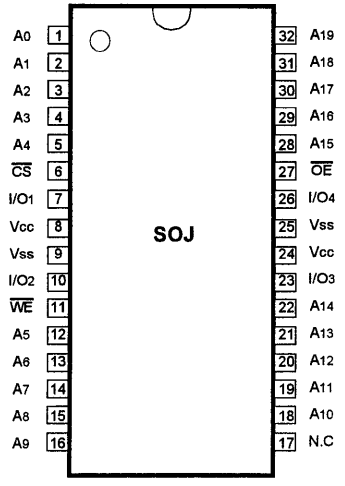
The KM64V4002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM64V4002A uses 4 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64V4002A is packaged in a 400 mil 32-pin plastic SOJ.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	140	mA
			17ns	-	135	
			20ns	-	130	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	50	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

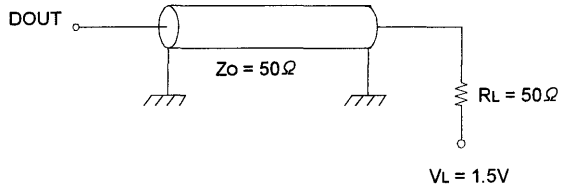
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} =3.3V±0.3V, unless otherwise noted.)

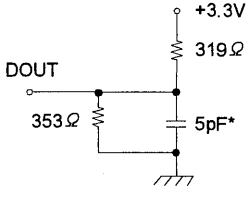
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

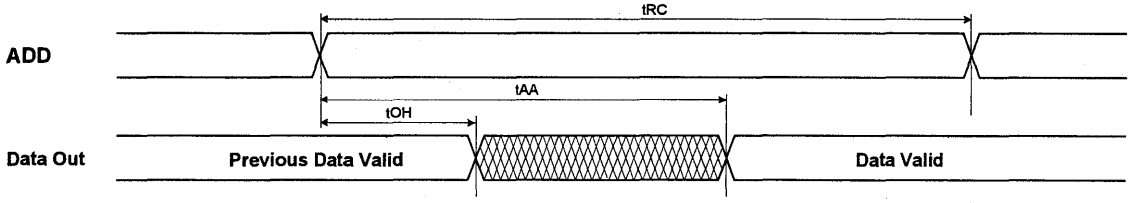
Parameter	Symbol	KM64V4002A-15		KM64V4002A-17		KM64V4002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

WRITE CYCLE

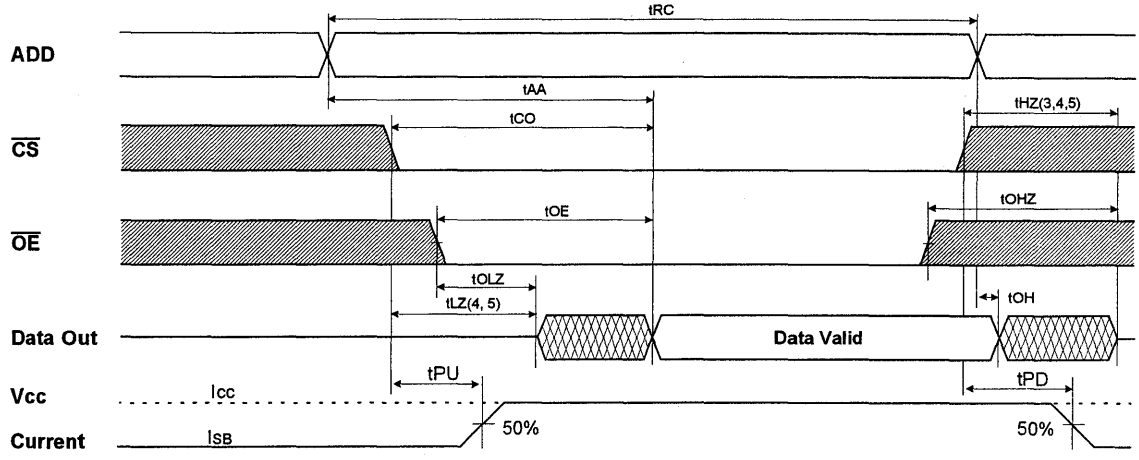
Parameter	Symbol	KM64V4002A-15		KM64V4002A-17		KM64V4002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



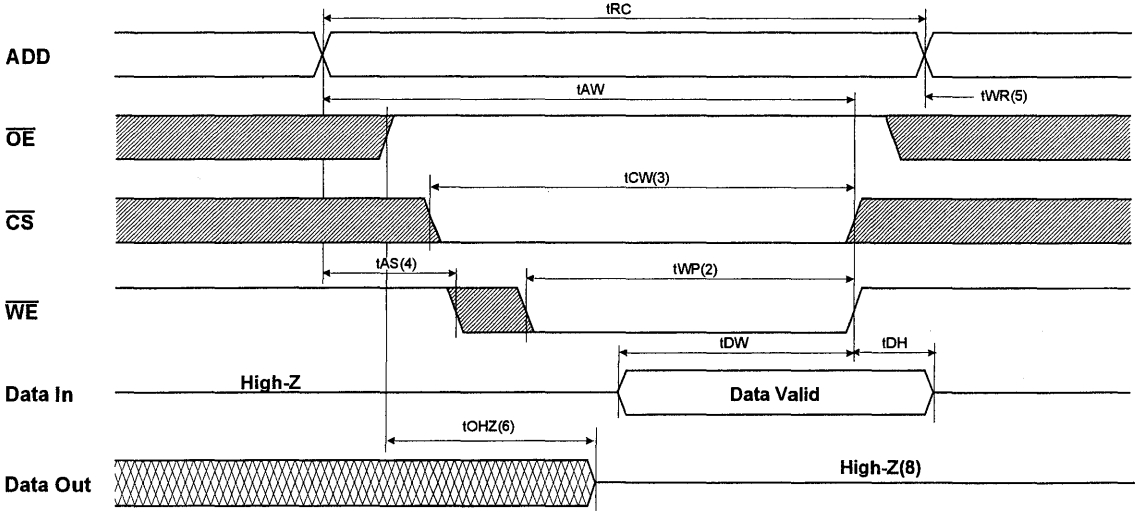
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

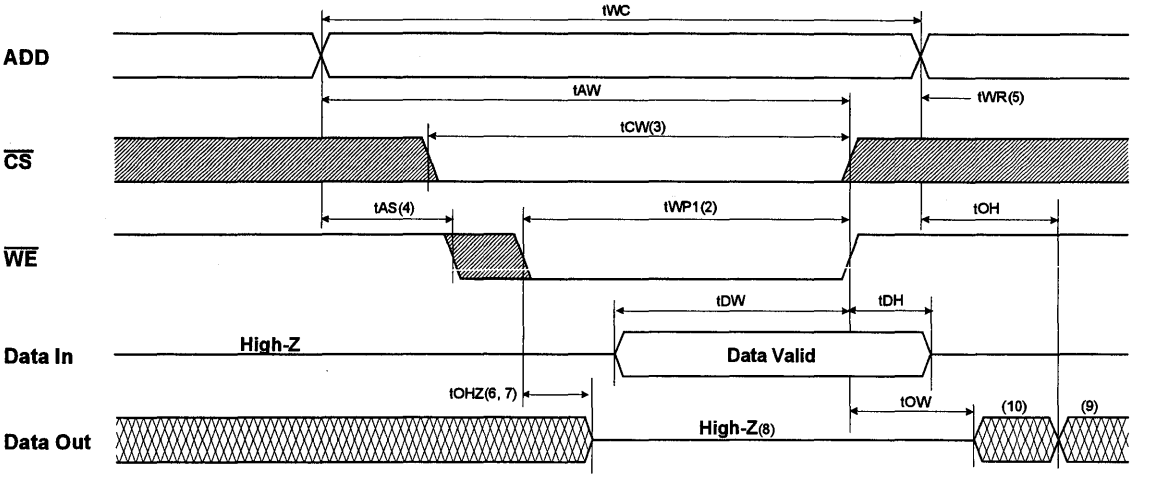
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

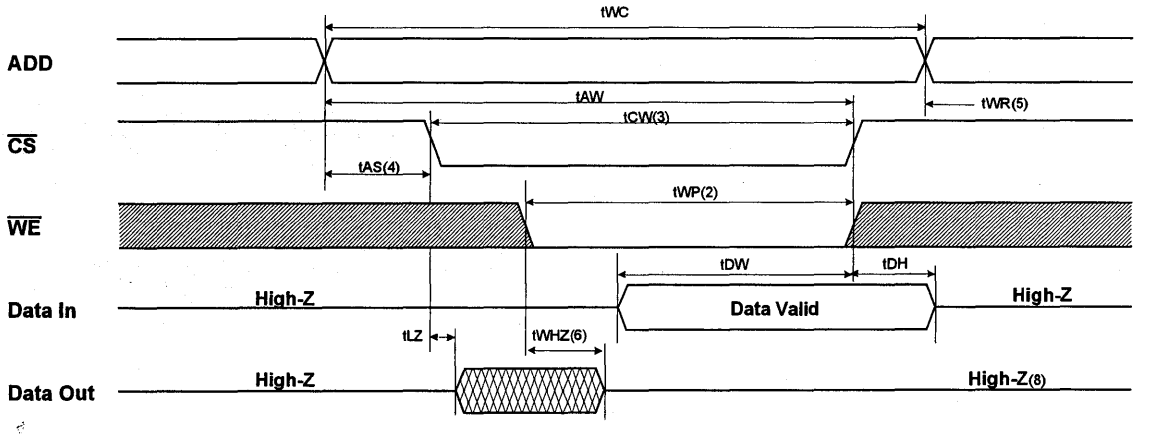


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

512K x 8 Bit High-Speed CMOS Static RAM(3.3V Operating)

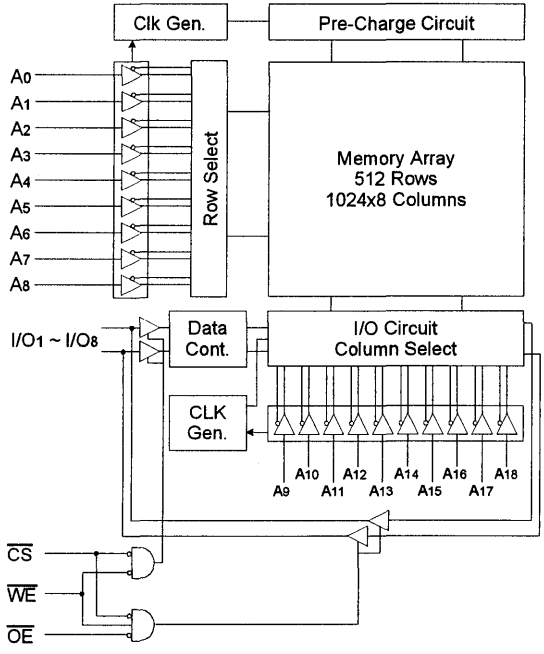
FEATURES

- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 10mA(Max.)
  - 1mA(Max.)- L-Ver.
  - Operating KM68V4002B/BL - 10 : 170mA(Max.)
  - KM68V4002B/BL - 12 : 160mA(Max.)
  - KM68V4002B/BL - 15 : 150mA(Max.)
- Single 3.3V±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage : 2V(Min.) - L-Ver. Only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM68V4002B/BLJ : 36-SOJ-400
  - KM68V4002B/BLT : 36-TSOP2-400F

ORDERING INFORMATION

KM68V4002B/BL -10/12/15	Commercial Temp.
KM68V4002B/BLI -10/12/15	Industrial Temp.

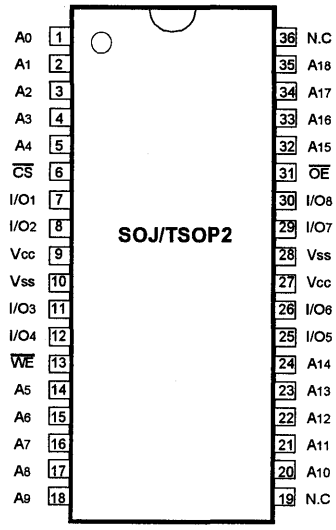
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM68V4002B/BL is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM68V4002B/BL uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V4002B/BL is packaged in a 400 mil 36-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION*(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 5.5	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	℃
Operating Temperature	Commercial	T_A	0 to 70	℃
	Industrial	T_A	-40 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.0	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤8ns) for I ≤ 20㎃

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤8ns) for I ≤ 20㎃

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	㎂
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	㎂
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	10ns	-	170	㎃
			12ns	-	160	
			15ns	-	150	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	㎃
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	10	㎃
			L-Ver.	-	1	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

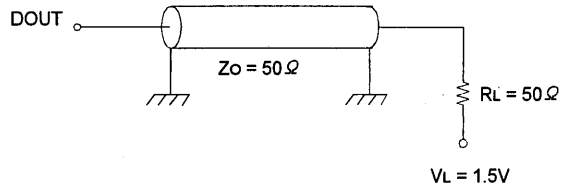
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} =3.3V±0.3V, unless otherwise noted.)

TEST CONDITIONS

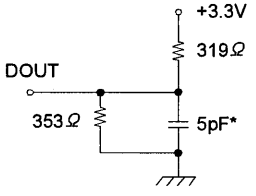
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68V4002B/BL-10		KM68V4002B/BL-12		KM68V4002B/BL-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	12	-	15	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

WRITE CYCLE

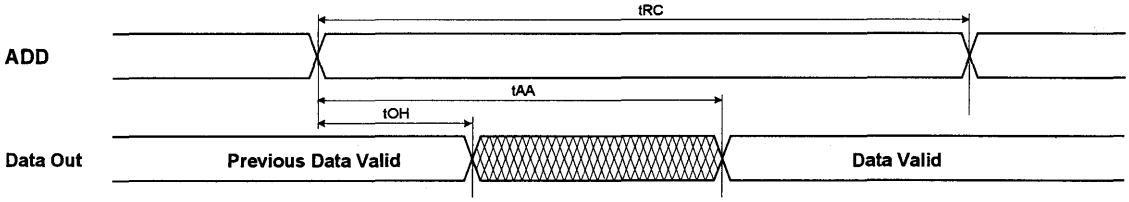
Parameter	Symbol	KM68V4002B/BL-10		KM68V4002B/BL-12		KM68V4002B/BL-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	10	-	12	-	15	-	ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	10	-	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	5	0	6	0	7	ns
Data to Write Time Overlap	tDW	5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

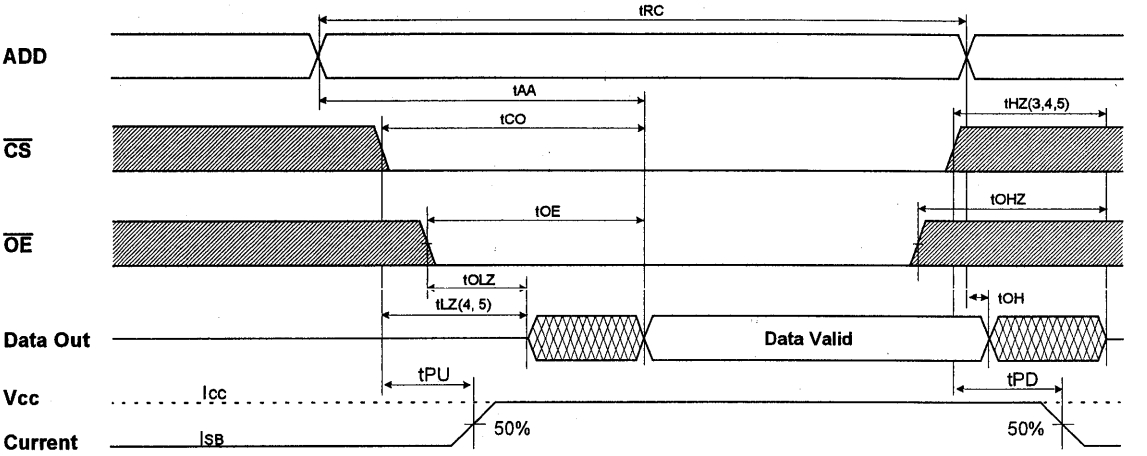
2

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



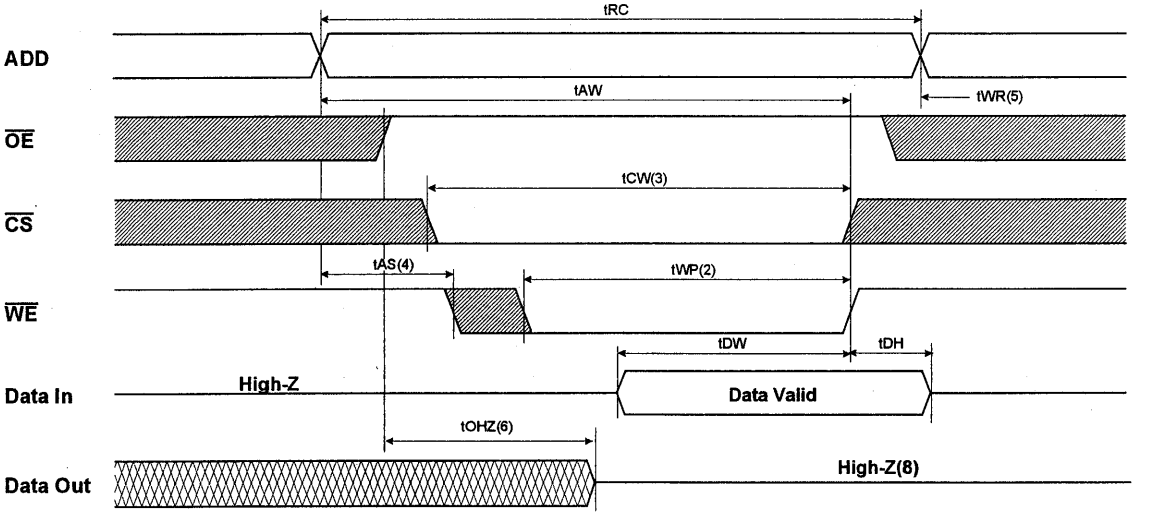
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



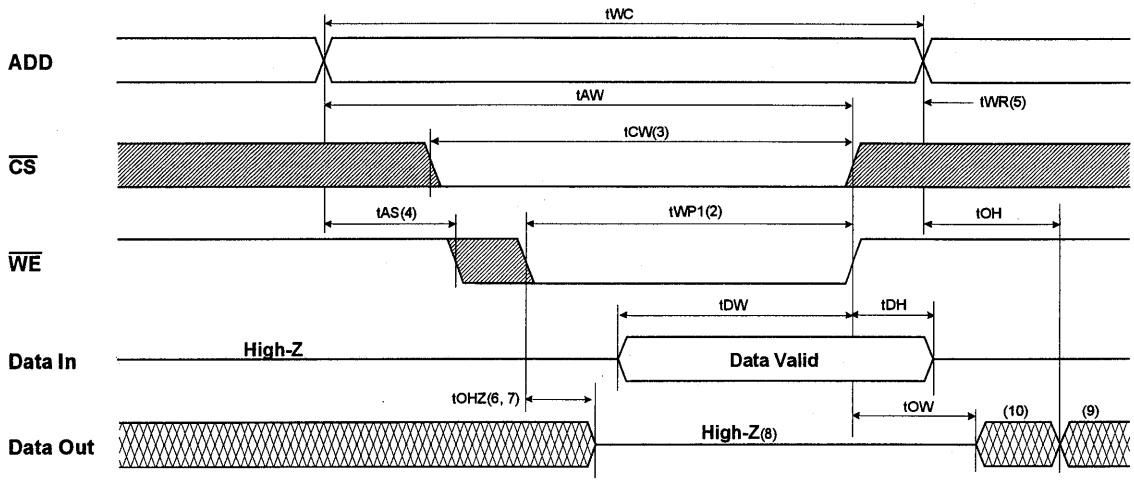
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

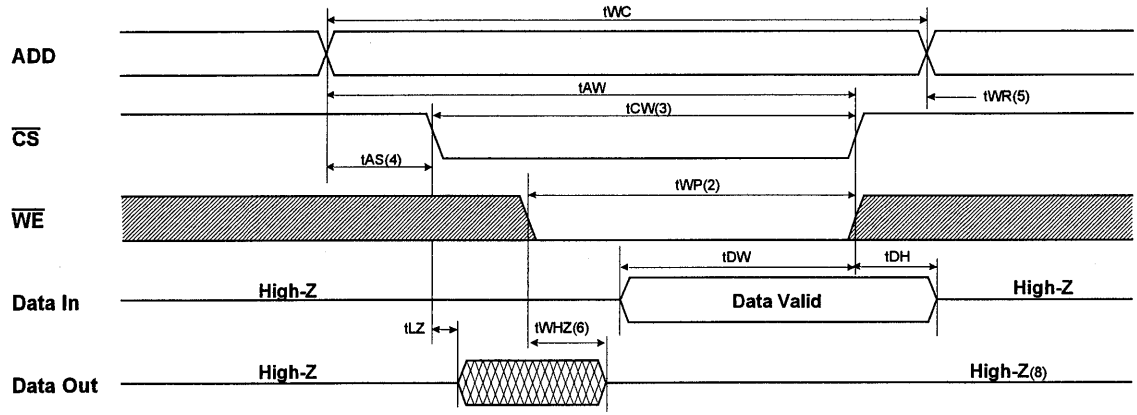
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

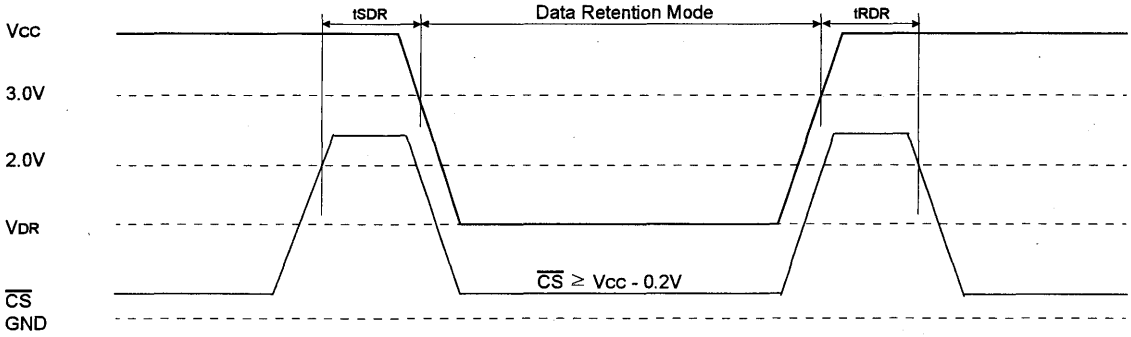
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.9	mA
		V_{CC} = 2.0V, $\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.7	mA
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



SAMSUNG ELECTRONICS

512K x 8 Bit High-Speed CMOS Static RAM(3.3V Operating)

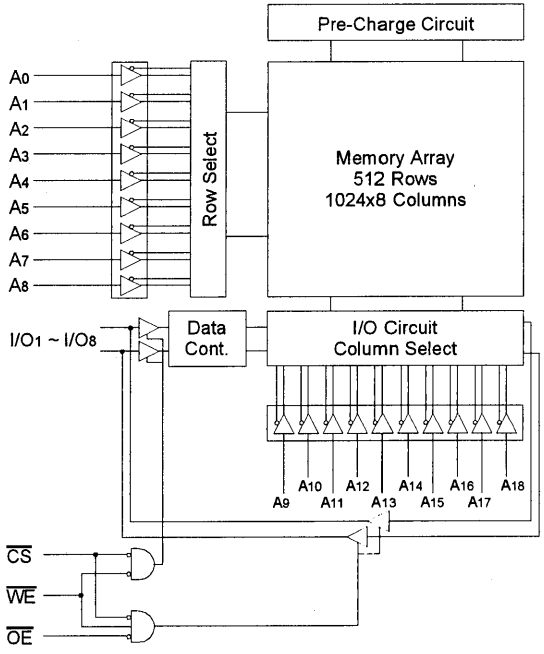
FEATURES

- Fast Access Time 12,13,15ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60mA(Max.)
  - (CMOS) : 30mA(Max.)
  - Operating KM68BV4002 - 12 : 170mA(Max.)
  - KM68BV4002 - 13 : 165mA(Max.)
  - KM68BV4002 - 15 : 160mA(Max.)
- Single 3.3V + 10%/-5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM68BV4002J : 36-SOJ-400

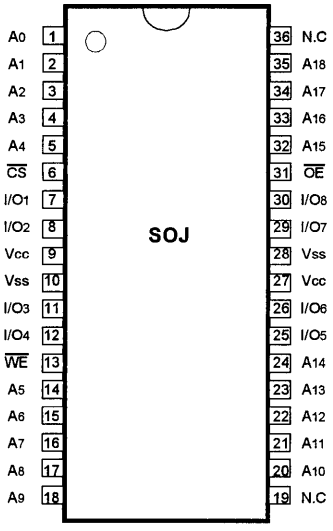
GENERAL DESCRIPTION

The KM68BV4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM68BV4002 uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68BV4002 is packaged in a 400 mil 36-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 3.3V+10%/-5%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-10	10	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	170	mA
			13ns	-	165	
			15ns	-	160	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	60	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	30	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

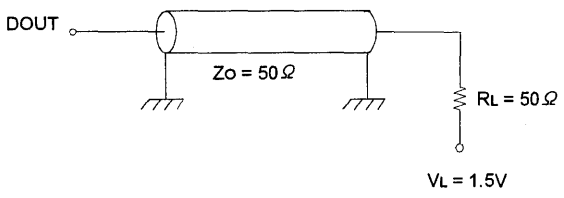
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} =3.3V +10%/-5%, unless otherwise noted.)

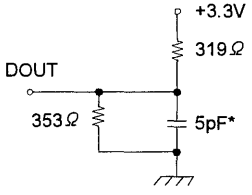
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

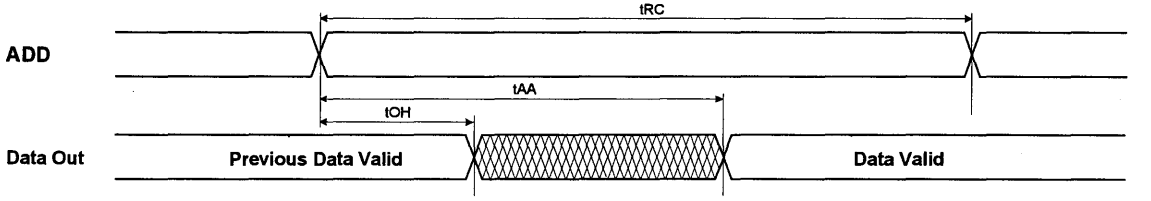
Parameter	Symbol	KM68BV4002-12		KM68BV4002-13		KM68BV4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	6	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM68BV4002-12		KM68BV4002-13		KM68BV4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	13	-	15	-	ns
Chip Select to End of Write	tCW	8.5	-	8.5	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	8.5	-	8.5	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	8.5	-	8.5	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	10	-	10	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	6	0	7	ns
Data to Write Time Overlap	tDW	7	-	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

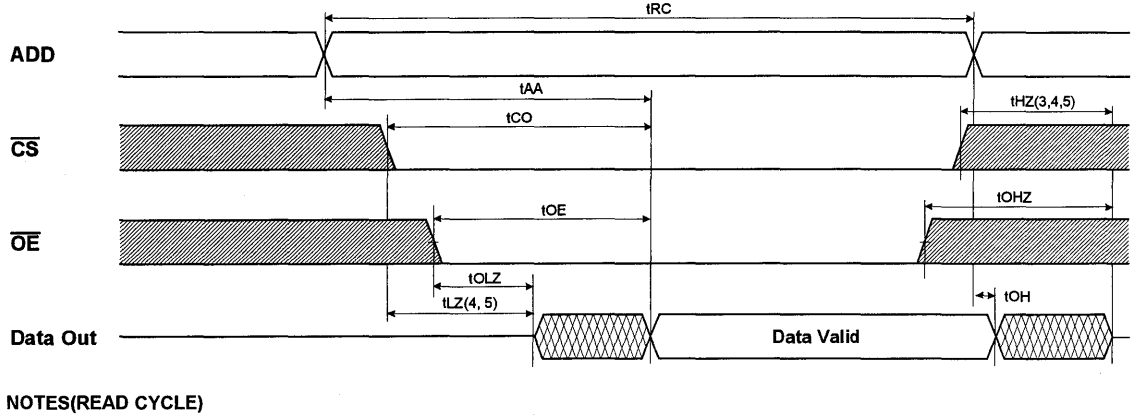
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



SAMSUNG ELECTRONICS

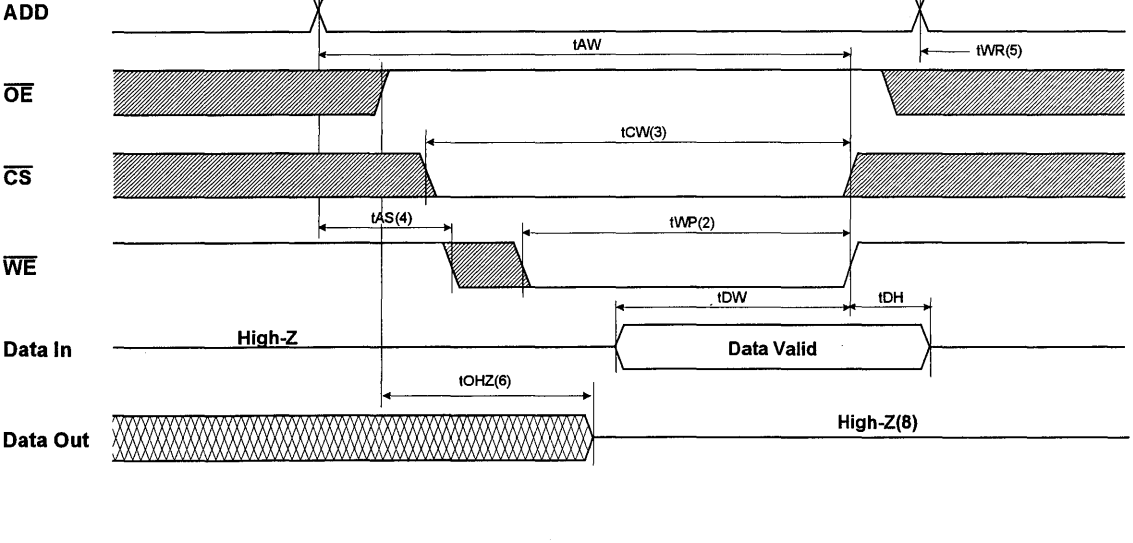
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



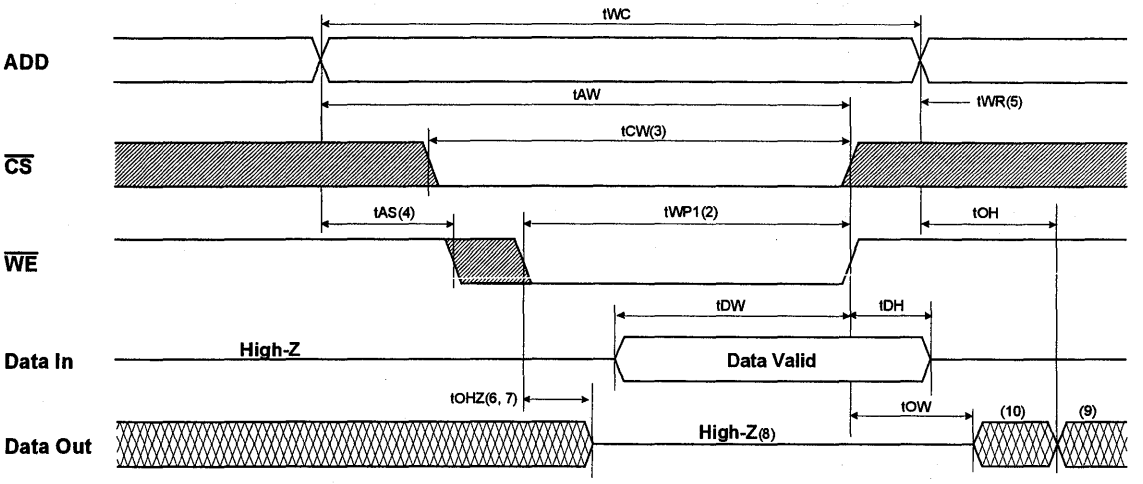
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200㎷ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

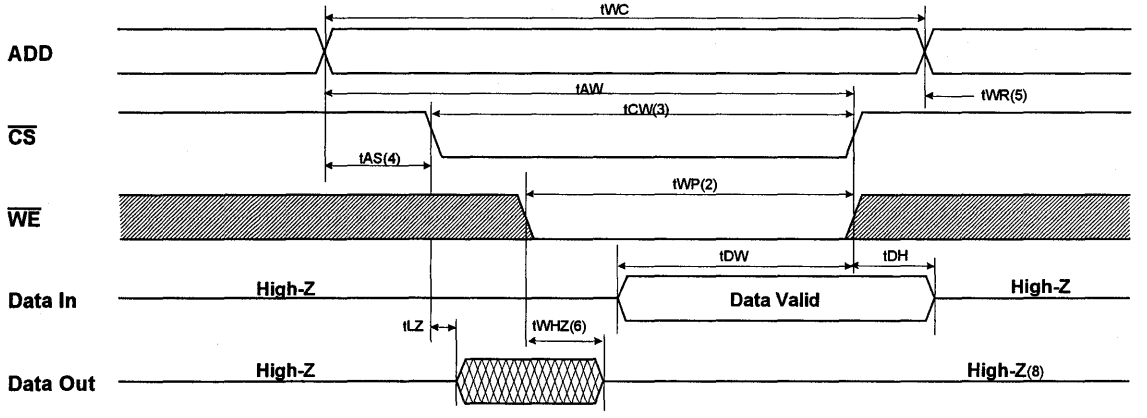
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

2

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

512K x 8 Bit High-Speed CMOS Static RAM

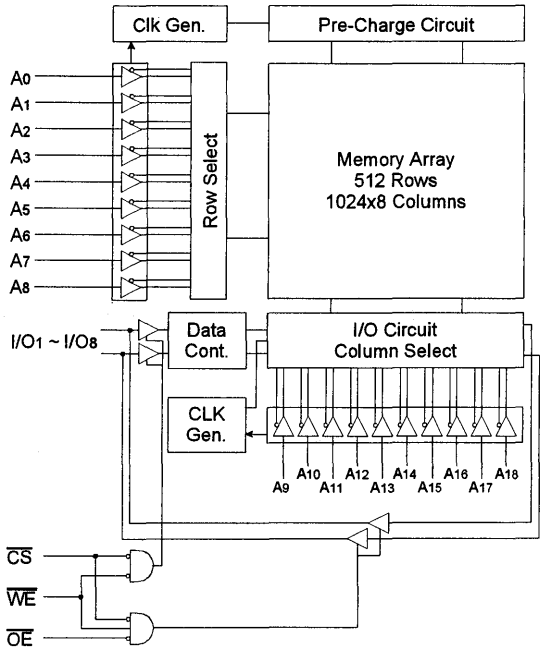
FEATURES

- Fast Access Time 15,17,20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM68V4002A - 15 : 160mA(Max.)
  - KM68V4002A - 17 : 155mA(Max.)
  - KM68V4002A - 20 : 150mA(Max.)
- Single 3.3V±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM68V4002AJ : 36-SOJ-400

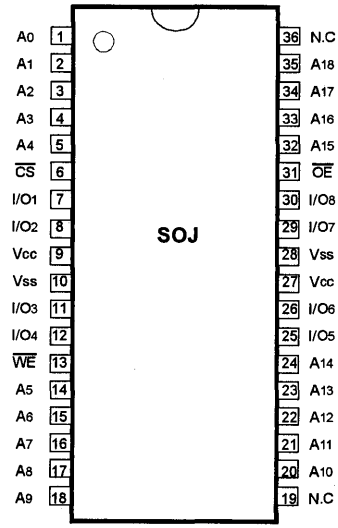
GENERAL DESCRIPTION

The KM68V4002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM68V4002A uses 8 common input and output lines and has an output enable pin which operates faster than address access time ar read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V4002A is packaged in a 400 mil 36-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20㎃

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20㎃

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	㎂
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	㎂
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	160	㎃
			17ns	-	155	
			20ns	-	150	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	50	㎃
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	㎃
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

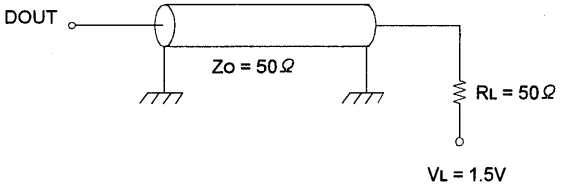
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} =3.3V±0.3V, unless otherwise noted.)

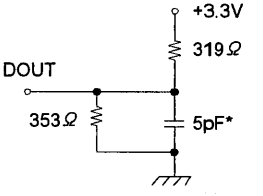
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM68V4002A-15		KM68V4002A-17		KM68V4002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	-	20	ns

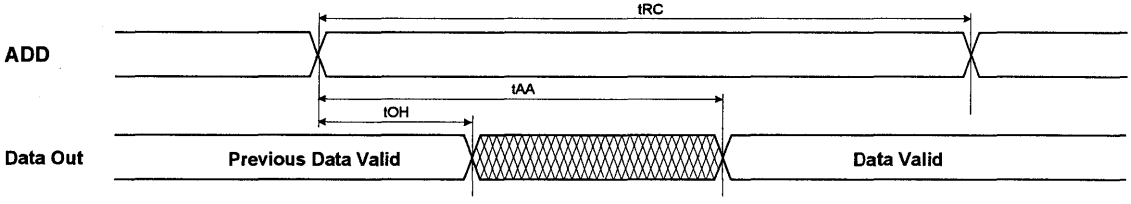
WRITE CYCLE

Parameter	Symbol	KM68V4002A-15		KM68V4002A-17		KM68V4002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

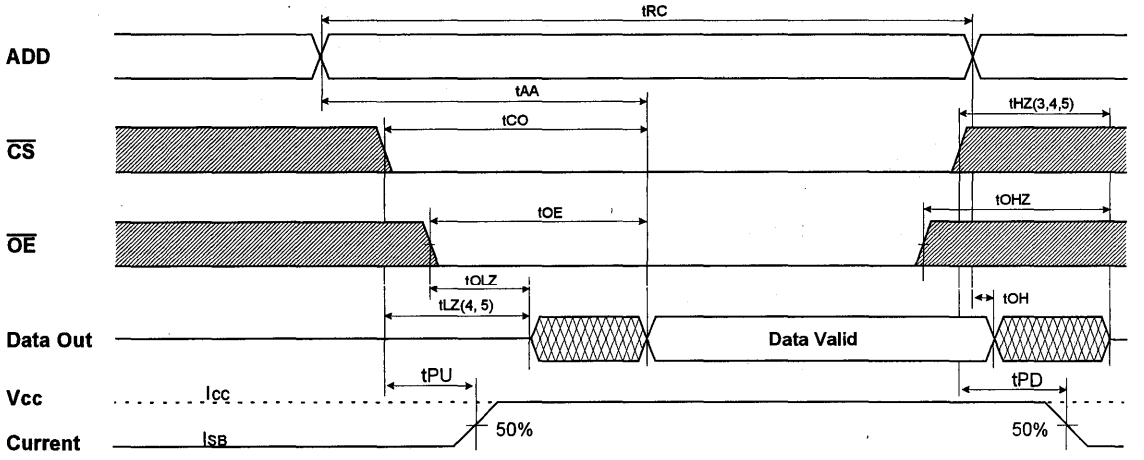
2

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH)



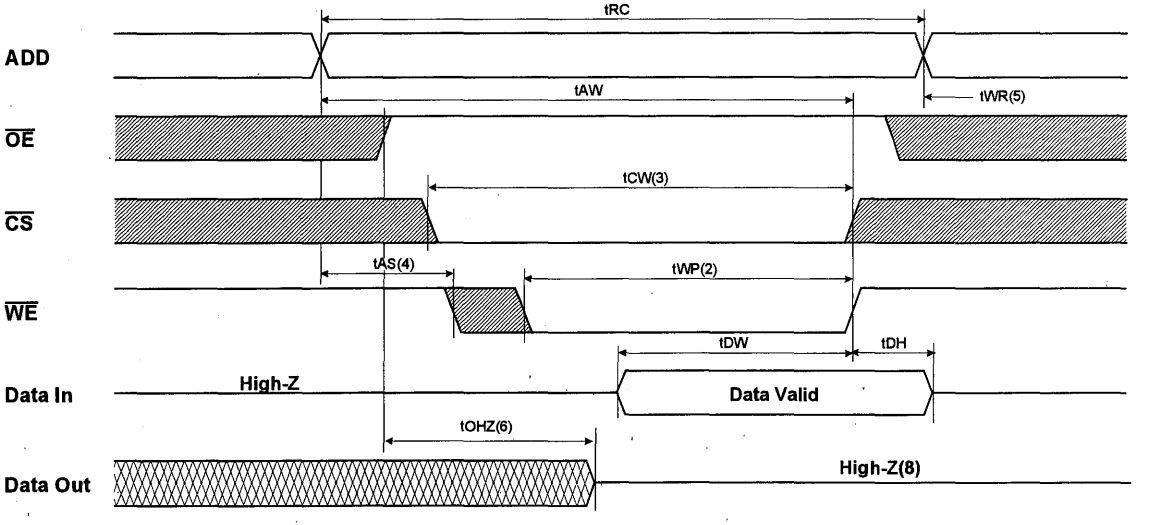
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



NOTES(READ CYCLE)

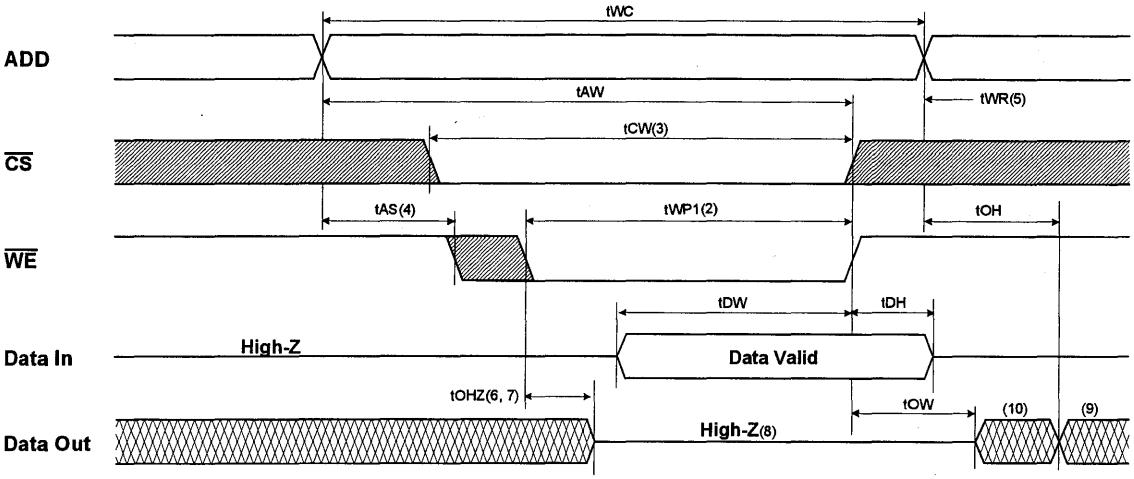
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)

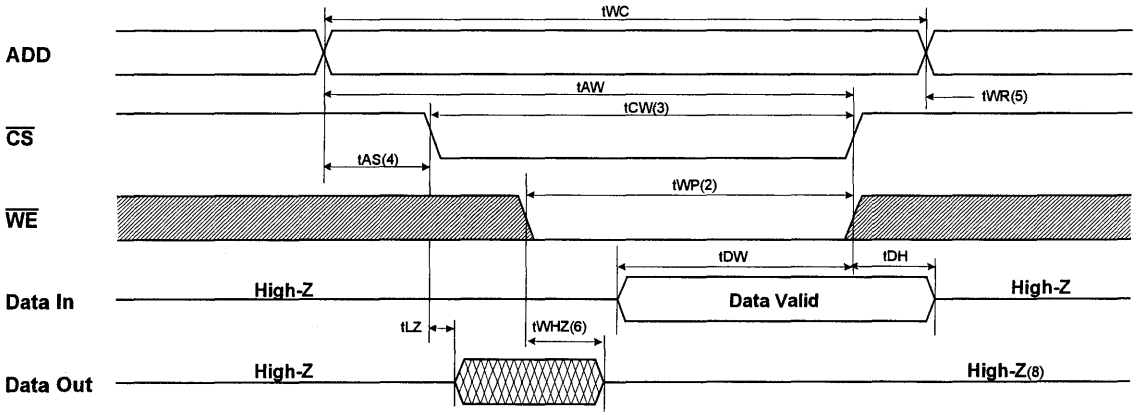


SAMSUNG ELECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



SAMSUNG ELECTRONICS

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* **NOTE** : X means Don't Care.

256K x 16 Bit High-Speed CMOS Static RAM(3.3V Operating)

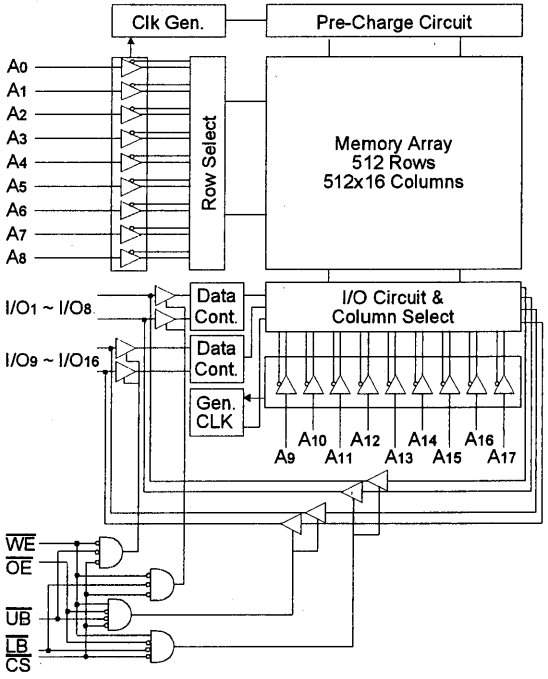
FEATURES

- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 10mA(Max.)
  - 1mA(Max.)- L-Ver.
  - Operating KM616V4002B/BL - 10 : 240mA(Max.)
  - KM616V4002B/BL - 12 : 230mA(Max.)
  - KM616V4002B/BL - 15 : 220mA(Max.)
- Single 3.3V±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage : 2V(Min.) - L-Ver. Only
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O1~ I/O8, $\overline{UB}$: I/O9~ I/O16
- Standard Pin Configuration
  - KM616V4002B/BLJ : 44-SOJ-400
  - KM616V4002B/BLT : 44-TSOP2-400F

ORDERING INFORMATION

KM616V4002B/BL -10/12/15	Commercial Temp.
KM616V4002B/BLI -10/12/15	Industrial Temp.

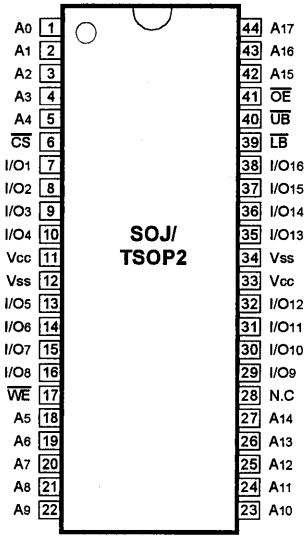
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The KM616V4002B/BL is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM616V4002B/BL uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616V4002B/BL is packaged in a 400mil 44-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V_{CC}	-0.5 to 5.5	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_A	0 to 70	°C
	Industrial	T_A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.0	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤8ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70°C, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	10ns	-	240	mA
			12ns	-	230	
			15ns	-	220	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	40	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V	Normal	-	10	mA
			L-Ver.	-	1	
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

NOTE: Above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

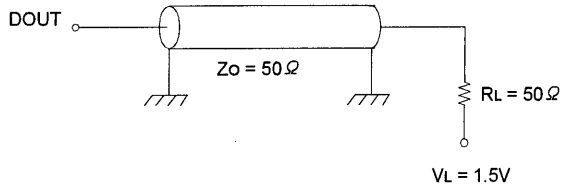
AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} =3.3V±0.3V, unless otherwise noted.)

TEST CONDITIONS

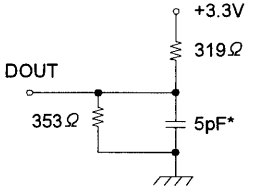
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

NOTE: Above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM616V4002B/BL-10		KM616V4002B/BL-12		KM616V4002B/BL-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

NOTE: Above parameters are also guaranteed at industrial temperature range.

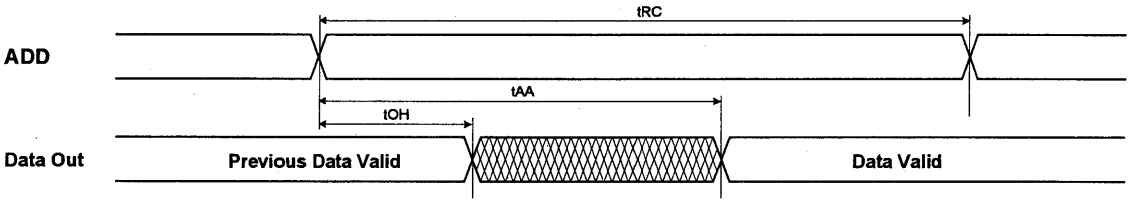
WRITE CYCLE

Parameter	Symbol	KM616V4002B/BL-10		KM616V4002B/BL-12		KM616V4002B/BL-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	10	-	12	-	15	-	ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	10	-	12	-	15	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	7	-	8	-	10	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	5	0	6	0	7	ns
Data to Write Time Overlap	tDW	5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

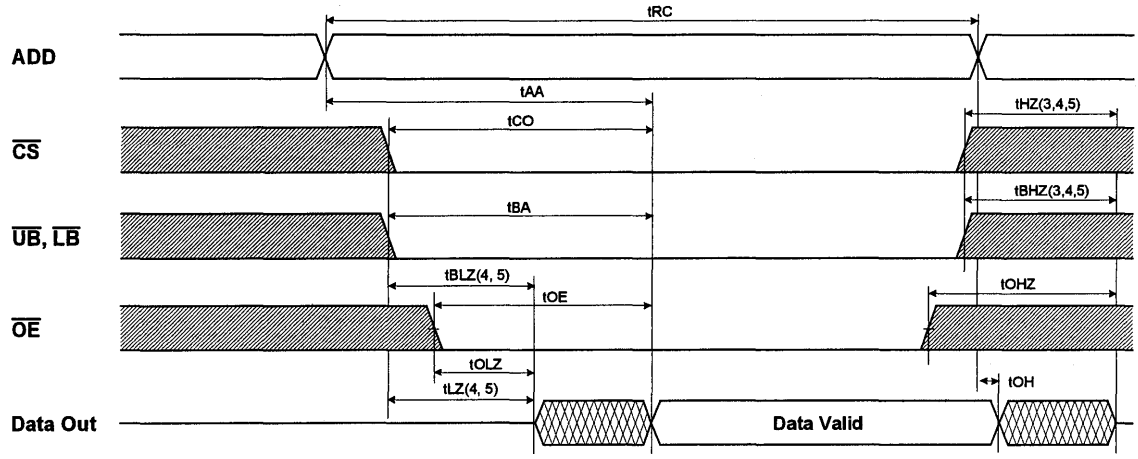
NOTE: Above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$\overline{UB}$=$\overline{LB}$=V_{IL}, $\overline{WE}$=V_{IH})



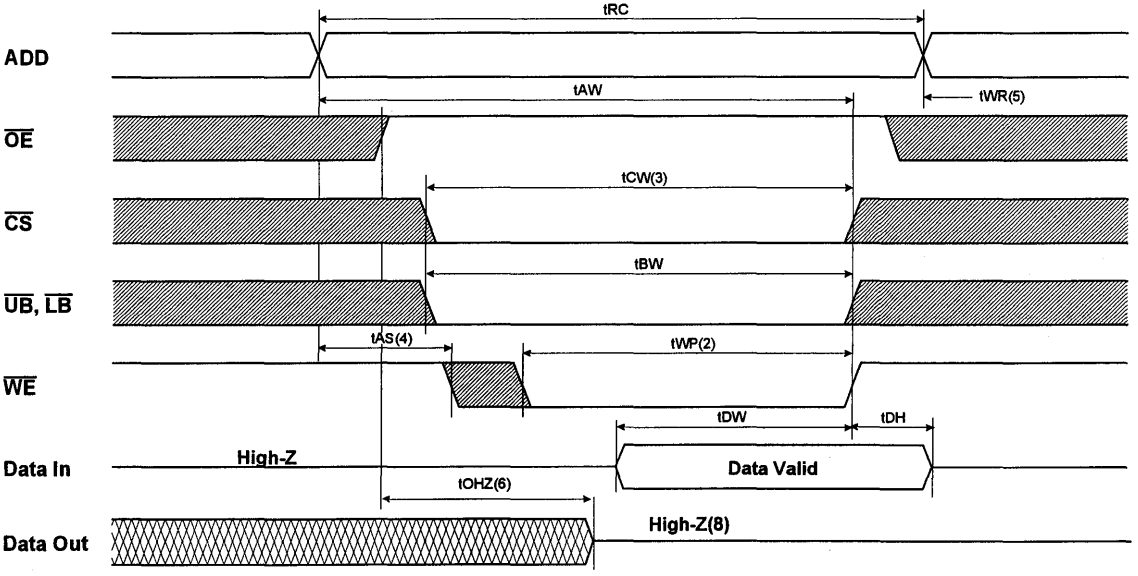
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



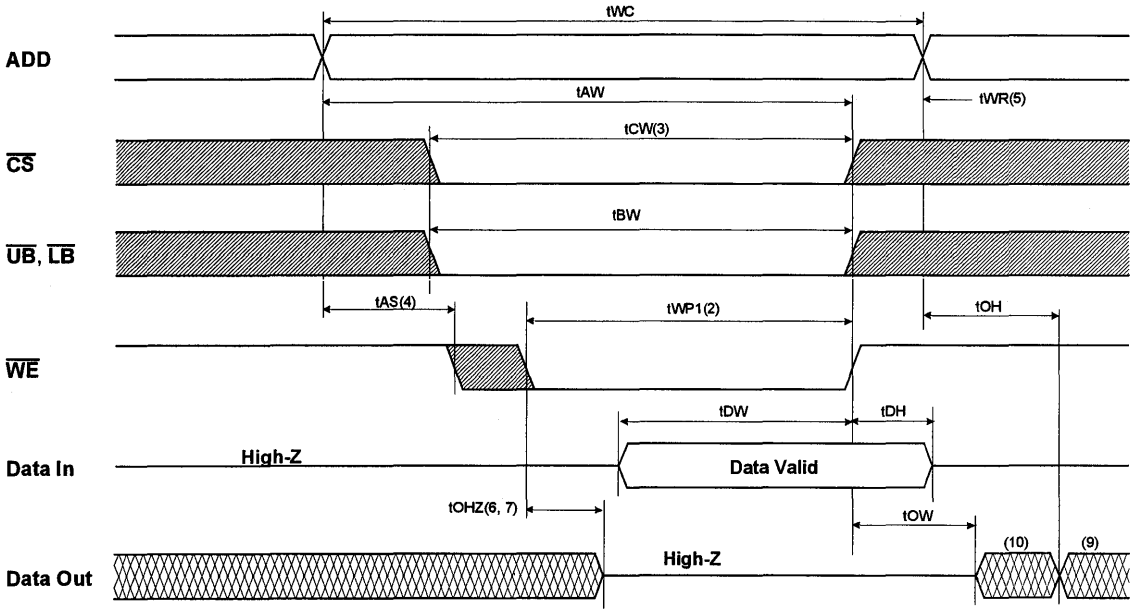
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200㎷ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

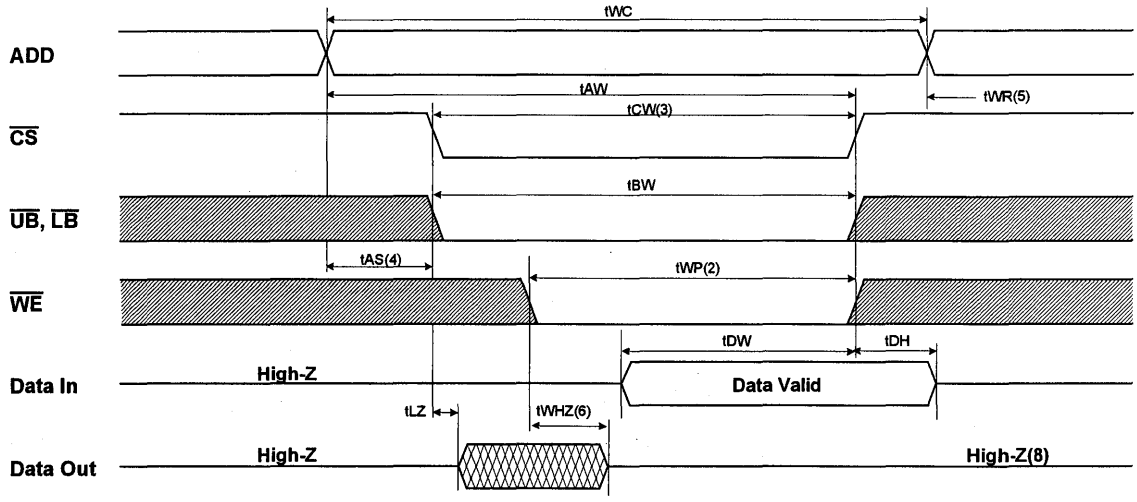
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



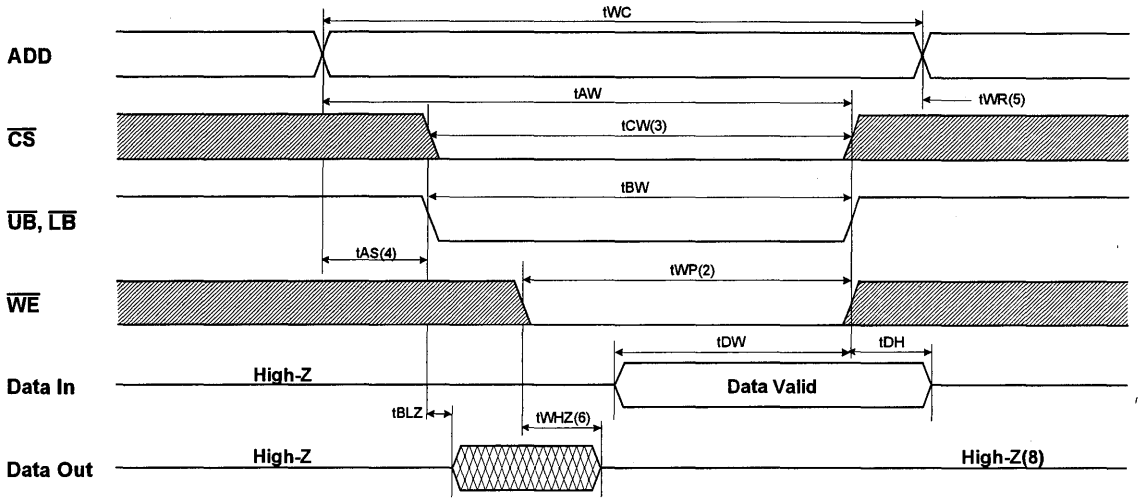
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$. $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z		I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

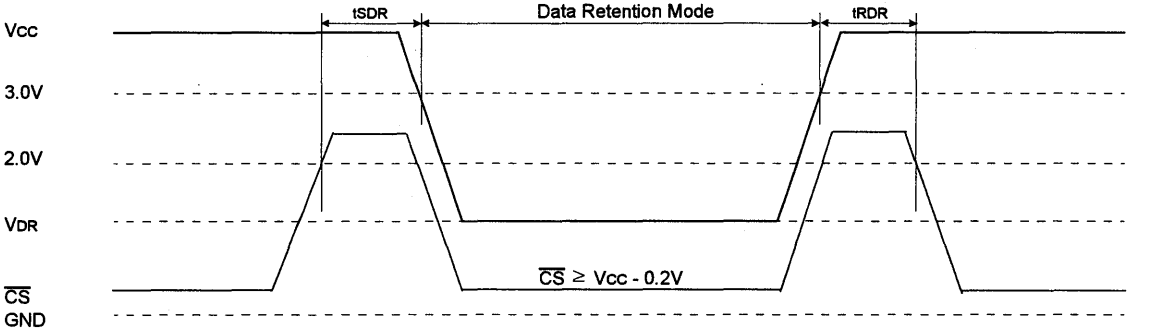
* **NOTE** : X means Don't Care.

DATA RETENTION CHARACTERISTICS*(T_A = 0℃ to 70℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$ - 0.2V	2.0	-	3.6	V
Data Retention Current	I_{DR}	Vcc = 3.0V, $\overline{CS} \geq$ Vcc - 0.2V $V_{IN} \geq$ Vcc - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.9	mA
		Vcc = 2.0V, $\overline{CS} \geq$ Vcc - 0.2V $V_{IN} \geq$ Vcc - 0.2V or $V_{IN} \leq$ 0.2V	-	-	0.7	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

NOTE: Above parameters are also guaranteed at industrial temperature range.
* L-Ver only.

DATA RETENTION WAVE FORM($\overline{CS}$ Controlled)



256K x 16 Bit High-Speed BiCMOS Static RAM(3.3V Operating)

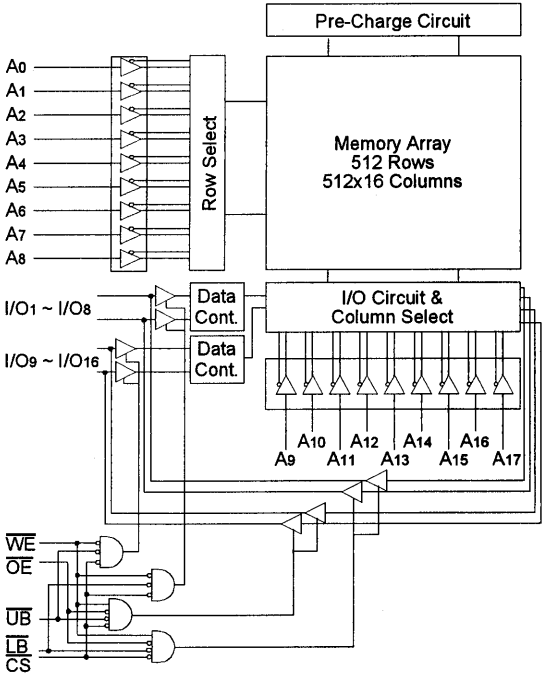
FEATURES

- Fast Access Time 12,13,15ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60mA(Max.)
  - (CMOS) : 30mA(Max.)
  - Operating KM616BV4002 - 12 : 240mA(Max.)
  - KM616BV4002 - 13 : 235mA(Max.)
  - KM616BV4002 - 15 : 230mA(Max.)
- Single 3.3V+ 10%/-5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O1~ I/O8, $\overline{UB}$: I/O9~ I/O16
- Standard Pin Configuration
  - KM616BV4002J : 44-SOJ-400

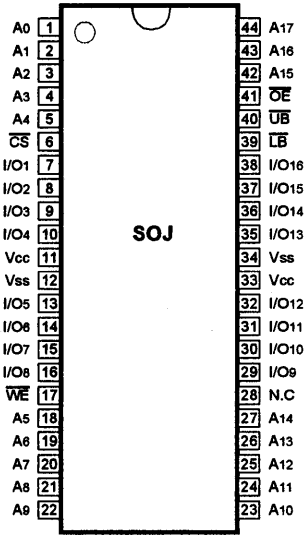
GENERAL DESCRIPTION

The KM616BV4002 is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM616BV4002 uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616BV4002 is packaged in a 400mil 44-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 5.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 3.3V+10%/-5%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-10	10	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	12ns	-	240	mA
			13ns	-	235	
			15ns	-	230	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	60	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	30	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

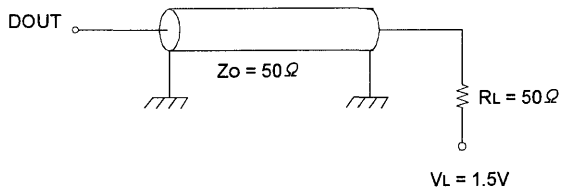
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(TA = 0 to 70℃, Vcc =3.3V +10%/-5%, unless otherwise noted.)

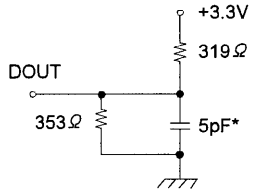
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

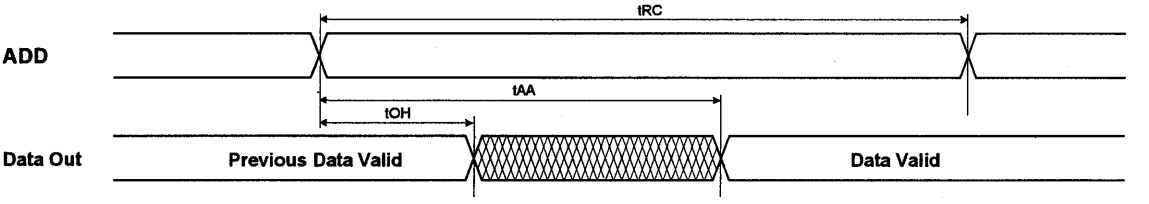
Parameter	Symbol	KM616BV4002-12		KM616BV4002-13		KM616BV4002 -15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	13	-	15	-	ns
Address Access Time	tAA	-	12	-	13	-	15	ns
Chip Select to Output	tCO	-	12	-	13	-	15	ns
Output Enable to Valid Output	tOE	-	6	-	6	-	7	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	6	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	6	0	6	0	7	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	6	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

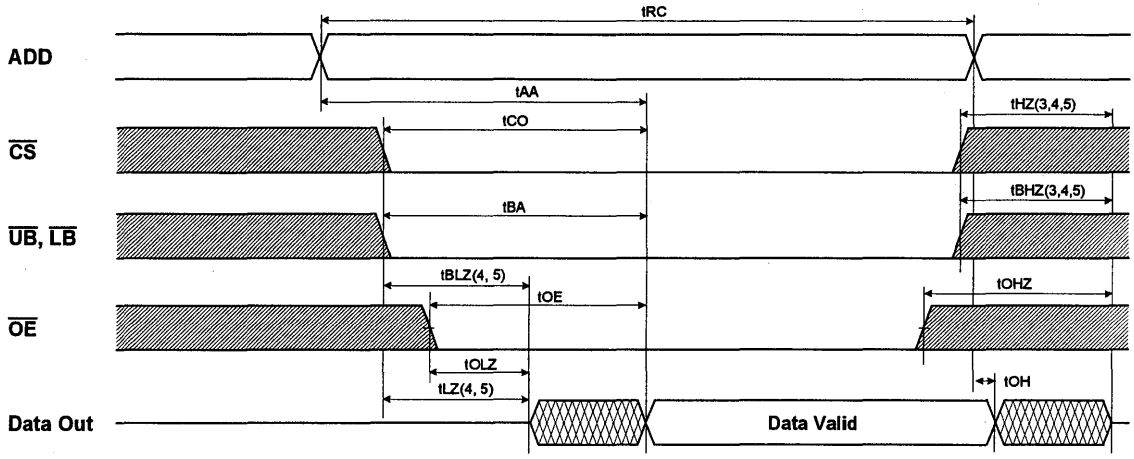
Parameter	Symbol	KM616BV4002-12		KM616BV4002-13		KM616BV4002-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	12	-	13	-	15	-	ns
Chip Select to End of Write	tCW	9	-	10	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	10	-	10	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	9	-	10	-	10	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	10	-	11	-	12	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	9	-	10	-	10	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6.5	0	7	0	7.5	ns
Data to Write Time Overlap	tDW	7	-	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$\overline{UB}$=$\overline{LB}$=V_{IL}, $\overline{WE}$=V_{IH})



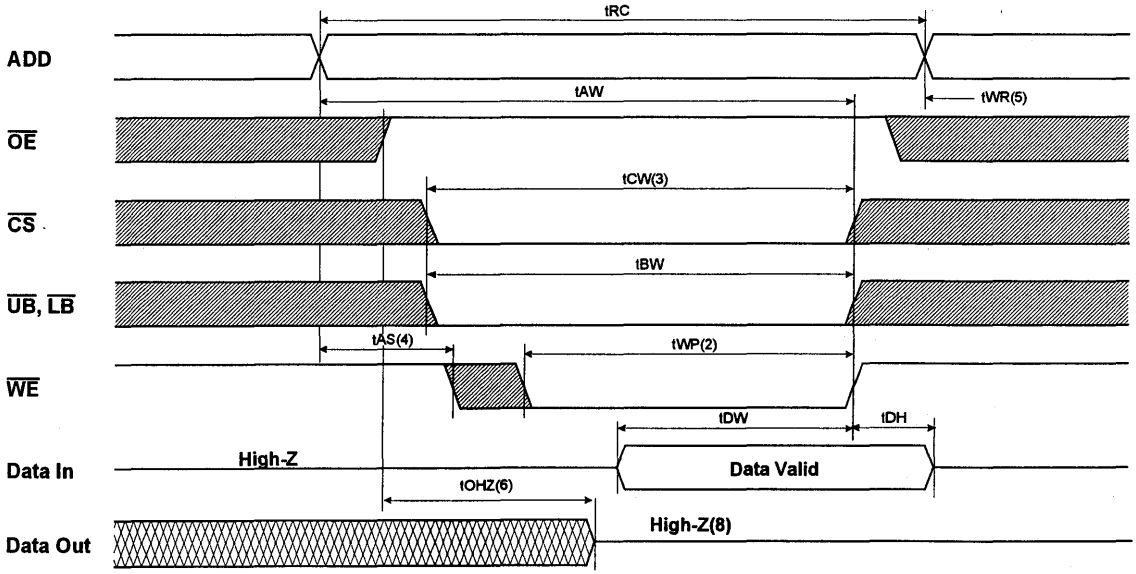
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=VIH)



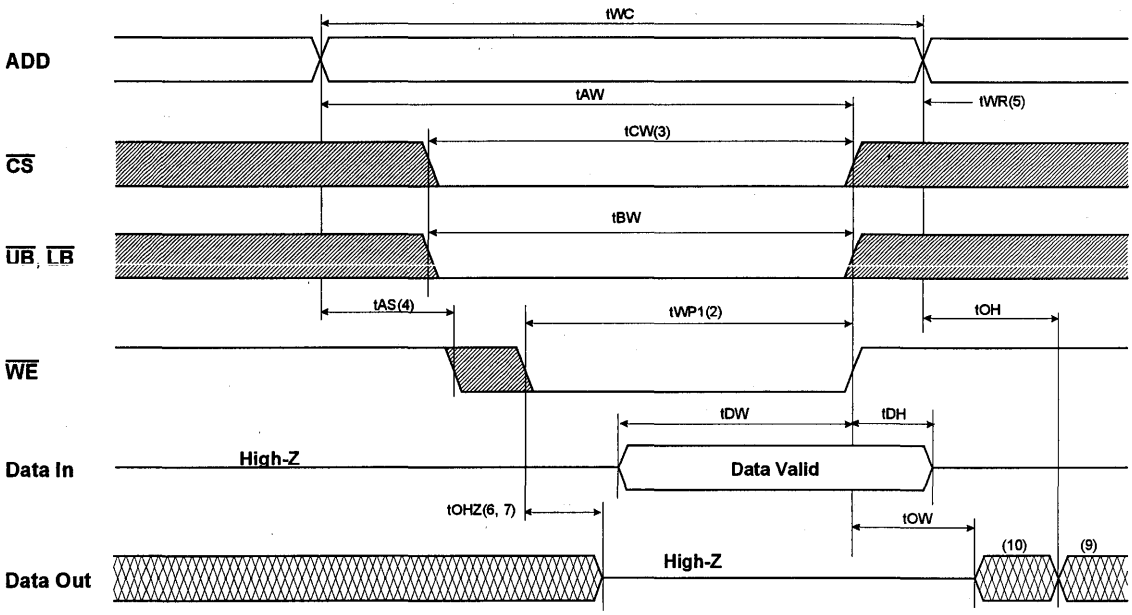
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=VIL.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

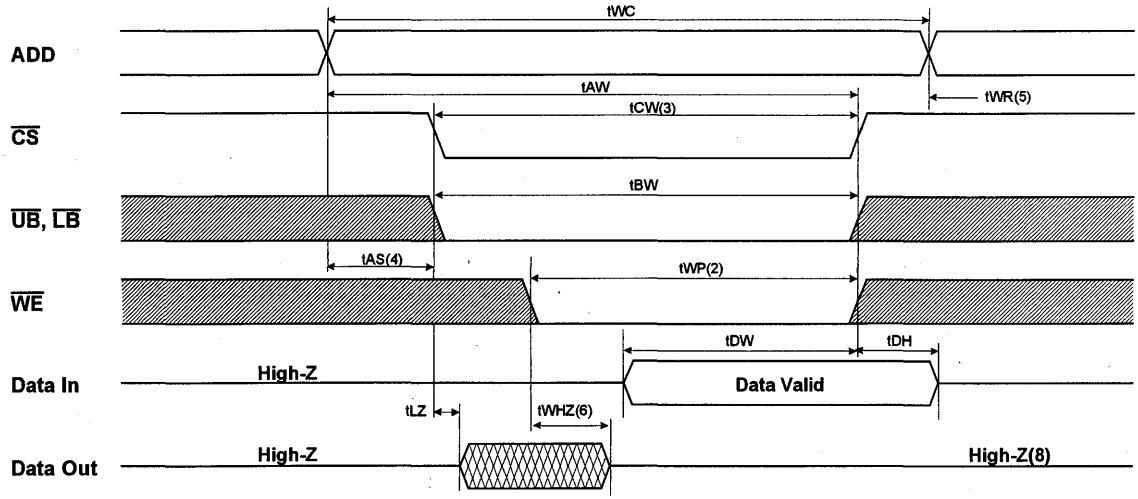
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



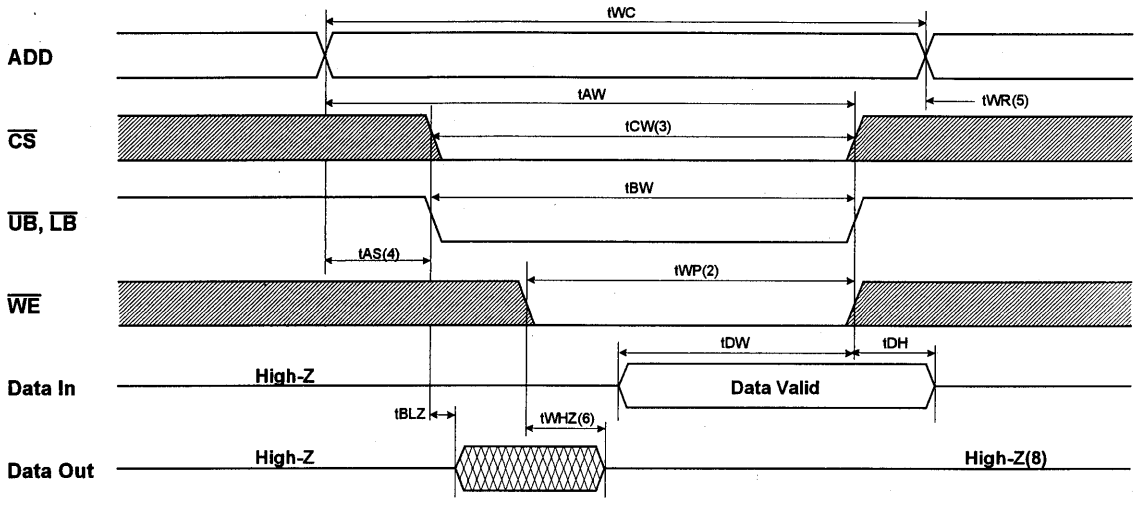
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$. $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z		I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

* **NOTE** : X means Don't Care.

256K x 16 Bit High-Speed CMOS Static RAM

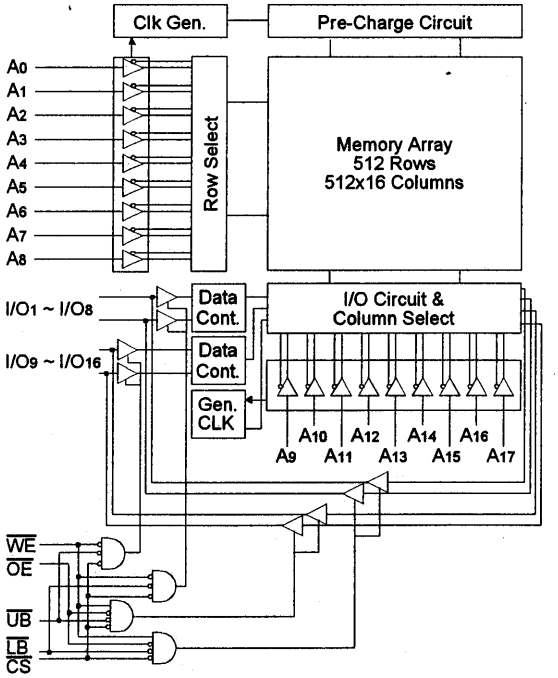
FEATURES

- Fast Access Time 15, 17,20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM616V4002A - 15 : 200mA(Max.)
  - KM616V4002A - 17 : 195mA(Max.)
  - KM616V4002A - 20 : 190mA(Max.)
- Single 3.3V±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control : $\overline{LB}$: I/O1~ I/O8, $\overline{UB}$: I/O9~ I/O16
- Standard Pin Configuration
  - KM616V4002AJ : 44-SOJ-400

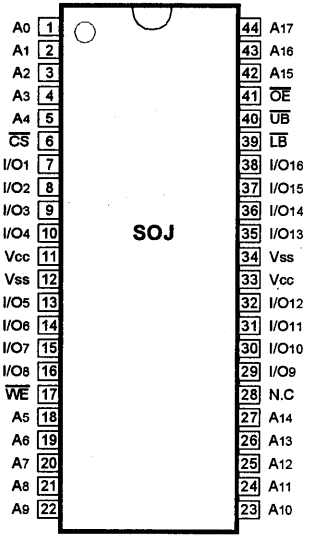
GENERAL DESCRIPTION

The KM616V4002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM616V4002A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control ($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616V4002A is packaged in a 400mil 44-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O1~I/O8)
$\overline{UB}$	Upper-byte Control(I/O9~I/O16)
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc + 0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A = 0 to 70℃, Vcc= 3.3V ± 0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to Vcc		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	200	mA
			17ns	-	195	
			20ns	-	190	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	50	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥ Vcc-0.2V, V_{IN} ≥ Vcc-0.2V or V_{IN} ≤ 0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25℃, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

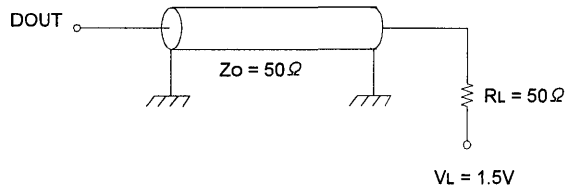
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A = 0 to 70℃, V_{CC} =3.3V±0.3V, unless otherwise noted.)

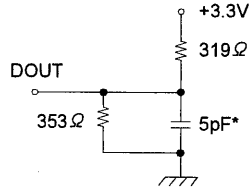
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

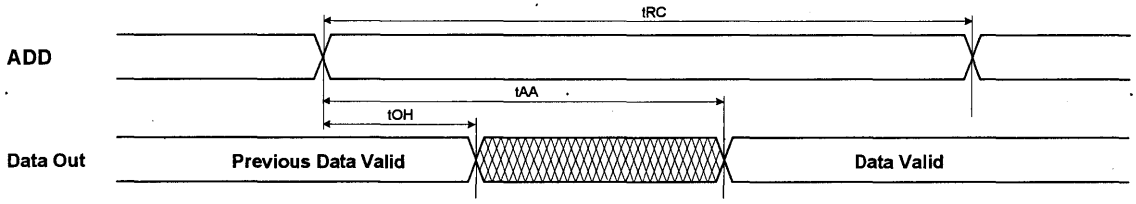
Parameter	Symbol	KM616V4002A-15		KM616V4002A-17		KM616V4002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	20	-	ns
Address Access Time	tAA	-	15	-	17	-	20	ns
Chip Select to Output	tCO	-	15	-	17	-	20	ns
Output Enable to Valid Output	tOE	-	7	-	8	-	9	ns
$\overline{UB}$, $\overline{LB}$ Access Time	tBA	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	tBLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	9	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	9	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	tBHZ	0	7	0	8	0	9	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

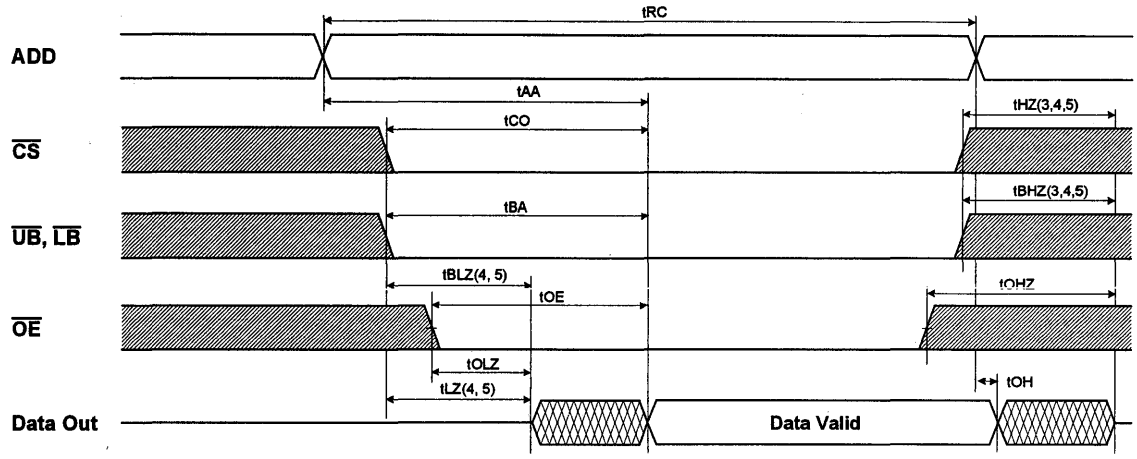
Parameter	Symbol	KM616V4002A-15		KM616V4002A-17		KM616V4002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	20	-	ns
Chip Select to End of Write	tCW	12	-	13	-	14	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ High)	tWP	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	-	17	-	20	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	tBW	12	-	13	-	14	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	7	0	8	0	9	ns
Data to Write Time Overlap	tDW	8	-	9	-	10	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$\overline{UB}$=$\overline{LB}$=VIL, $\overline{WE}$=VIH)



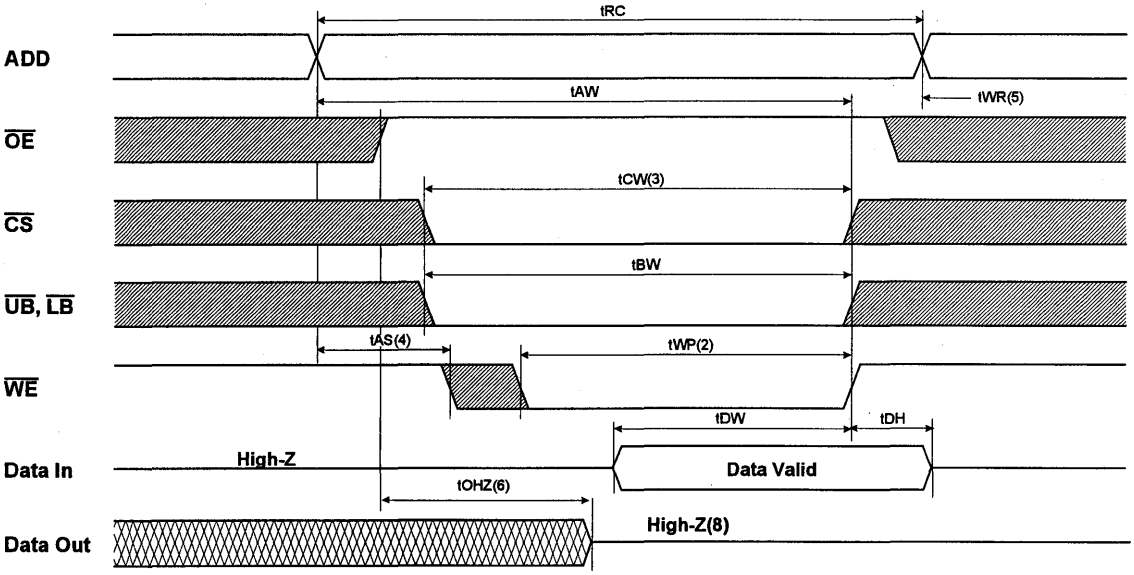
TIMING WAVE FORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



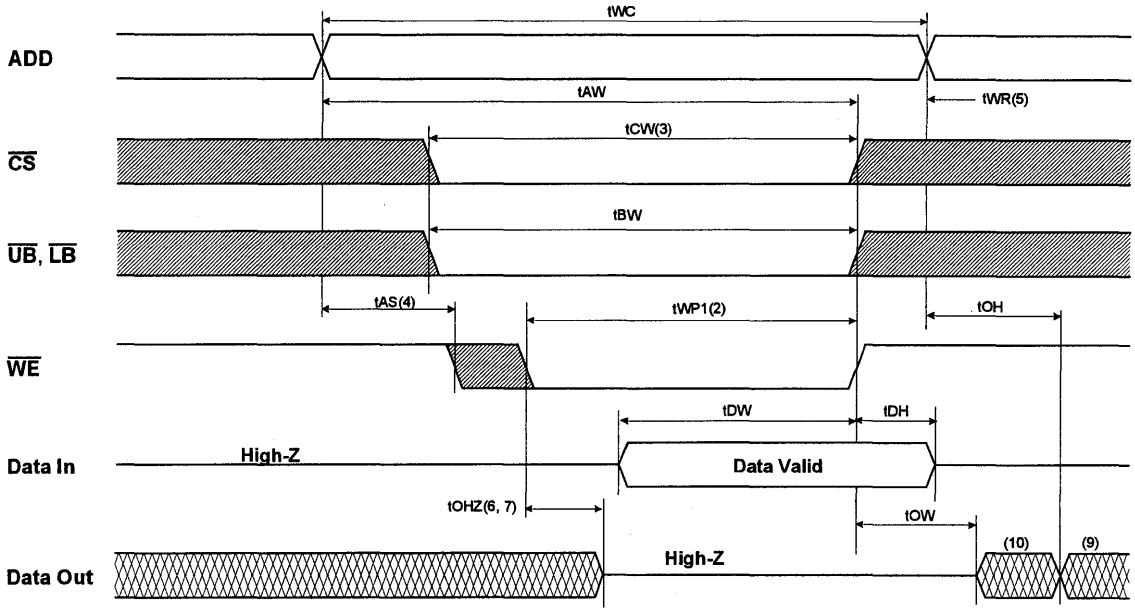
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} Levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ (min.) both for a given device and from device to device.
5. Transition is measured ±200㎷ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

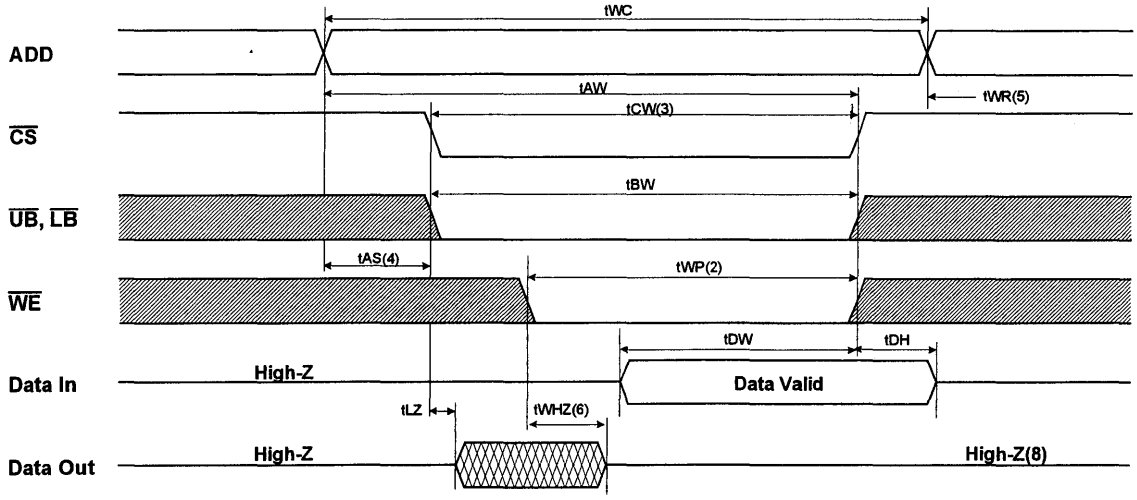
TIMING WAVE FORM OF WRITE CYCLE(1) ($\overline{OE}$=Clock)



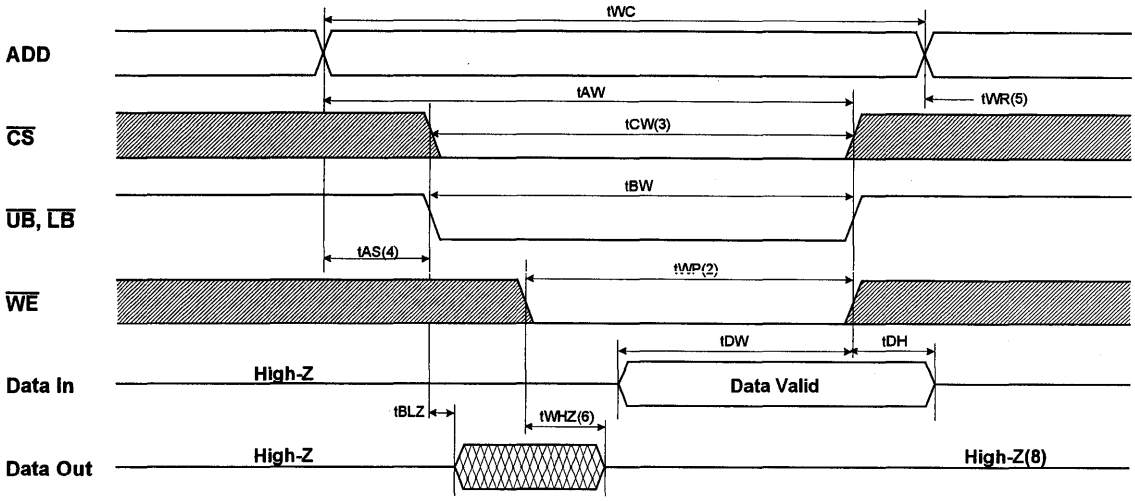
TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



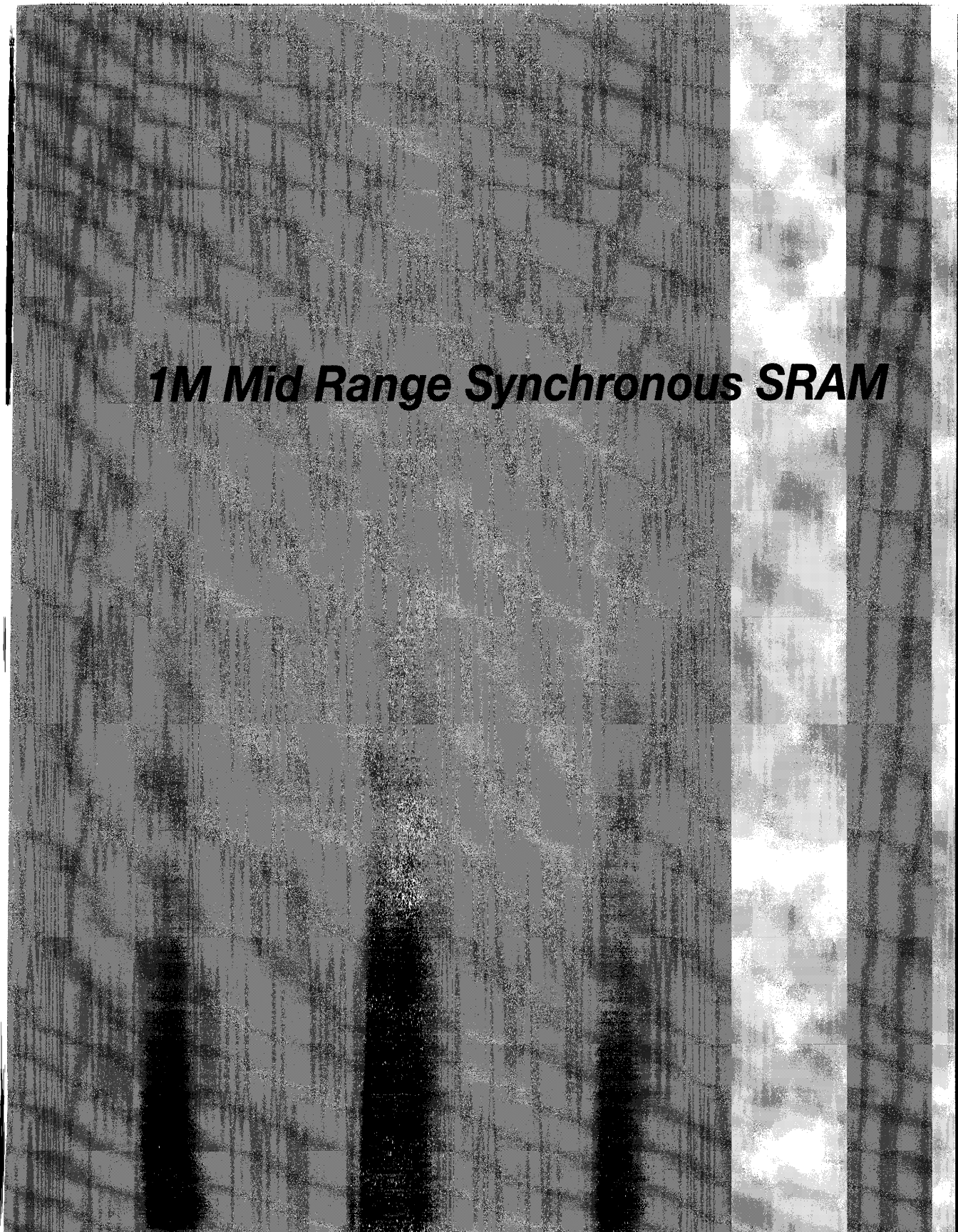
NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{CS}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
6. If $\overline{OE}$. $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z		ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	ICC
L	X	X	H	H				
L	H	L	L	H	Read	DOUT	High-Z	ICC
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	ICC
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

* **NOTE** : X means Don't Care.


1M Mid Range Synchronous SRAM

64Kx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- Single 5V± 5% Power Supply.
- Byte Writable Function.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 3.3V I/O Compatible.
- 52-Pin PLCC Package.

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	-12	Unit
Cycle Time	tCYC	15	15	17	20	ns
Clock Access Time	tCD	8	9	10	12	ns
Output Enable Access Time	tOE	5	5	5	6	ns

GENERAL DESCRIPTION

The KM718B86 is a 1,179,648 bits Synchronous Static Random Access Memory designed to support 66MHz of Intel secondary caches.

It is organized as 65,536 words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components count implementations of high performance cache RAM applications.

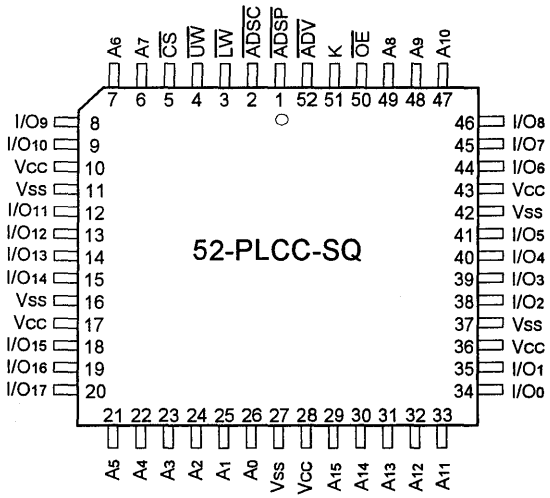
Write cycles are internally self-timed and synchronous.

The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

The KM718B86 is implemented with SAMSUNG's high performance BiCMOS technology and is available in a 52pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce.

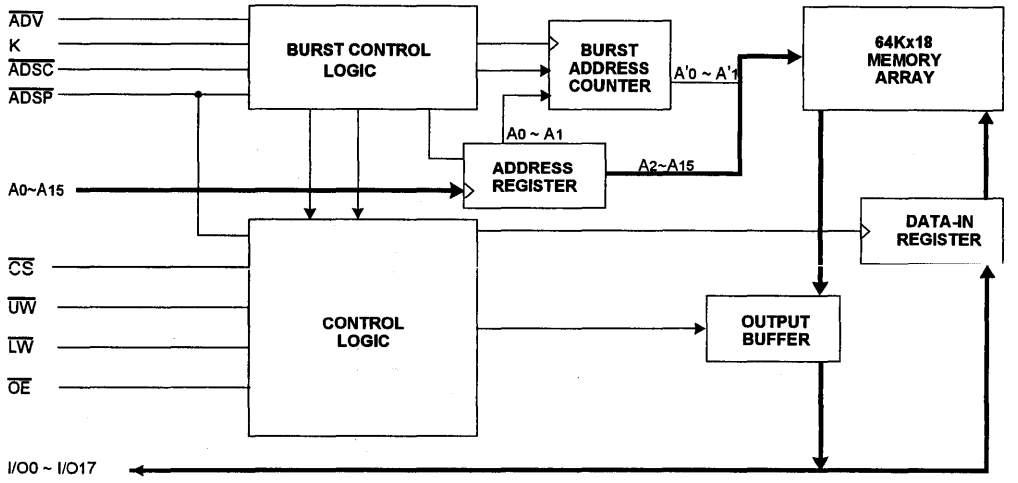
PIN CONFIGURATION(TOP VIEW)



PIN NAME

Pin Name	Pin Function
A0 - A15	Address Inputs
K	Clock
$\overline{LW}$, $\overline{UW}$	Write Enable
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
I/O0~I/O17	Data Inputs/Outputs
Vcc	+5V Power Supple
Vss	Ground

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718B86 is a synchronous SRAM designed to support the burst address accessing sequence of the Power microprocessor. All inputs(with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSP}$ and $\overline{ADSC}$. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with $\overline{ADV}$.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{LW}$, $\overline{UW}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sample low, The chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$, $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the next and subsequent clock edges. The address is increased internally for the next access of the burst when $\overline{LW}$, $\overline{UW}$ is sampled HIGH and $\overline{ADV}$ is sampled low.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{LW}$, $\overline{UW}$. $\overline{LW}$, $\overline{UW}$ is ignored on the clock edge that sampled ADSP low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when $\overline{LW}$, $\overline{UW}$ is sampled low (regardless of $\overline{OE}$). Data is clocked into the input register when $\overline{LW}$, $\overline{UW}$ is sampled low. The address increases internally to the next address of burst, if both $\overline{LW}$, $\overline{UW}$ and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed sampling low only one byte write enable signals($\overline{LW}$ or $\overline{LU}$)and $\overline{LW}$ controls I/O0~I/O7 and $\overline{UW}$ controls I/O8~I/O17.
Read or write cycles (depending on $\overline{LW}$, $\overline{LU}$)may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
$\overline{LW}$, $\overline{UW}$ is sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

(Interleaved Burst)

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE(See Notes 1 and 2)

$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{LW}$/$\overline{UW}$	K	Address Accessed	Operation
H	L	X	X	X	↑	N/A	Not Selected
H	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE1 : X means "Don't Care".

NOTE2 : The rising edge of clock is symbolized by ↑.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{OE}$	Operation
L	Read I/O0~I/O17
H	Output High-Z
X	Not Selected, Outputs High-Z

NOTE1 : X means "Don't Care".

NOTE2 : For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.5 to 7.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***NOTE** : Sampled not 100% tested.

TEST CONDITIONS(T_A = 0℃ to 70℃, V_{DD} = 5V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Max ; V_{IN} = Vss to Vcc		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled		-2	+2	μA
Operating Current	I_{CC}	Vcc = Max I_{OUT} = 0mA Cycle Time ≥ tCYC min	15ns	-	270	mA
			17ns	-	260	
			20ns	-	250	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, Min Cycle All Inputs= V_{IH} and V_{IL}, V_{IH} ≥3V and V_{IL}=0v		-	90	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	3.3	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.2	Vcc+0.5	V

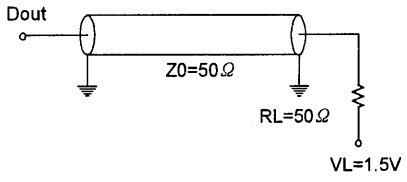
* V_{IL}(min) = -3.0(Pulse Width≤20ns)

AC TIMING CHARACTERISTICS(T_A = 0℃ to 70℃, V_{CC} = 5V±5%)

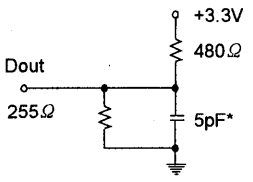
Parameter	Symbol	KM718B86-8		KM718B86-9		KM718B86-10		KM718B86-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	15	-	15	-	17	-	20	-	ns
Clock Access Time	tCD	-	8	-	9	-	10	-	12	ns
Output Enable to Data Valid	tOE	-	5	-	5	-	5	-	6	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	6	-	6	-	6	-	6	ns
Clock High Pulse Width	tCH	5	-	5	-	5	-	6	-	ns
Clock Low Pulse Width	tCL	5	-	5	-	5	-	6	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address/Advance Setup to Clock	tADVS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for this device to remain enabled.

Output Load(A)



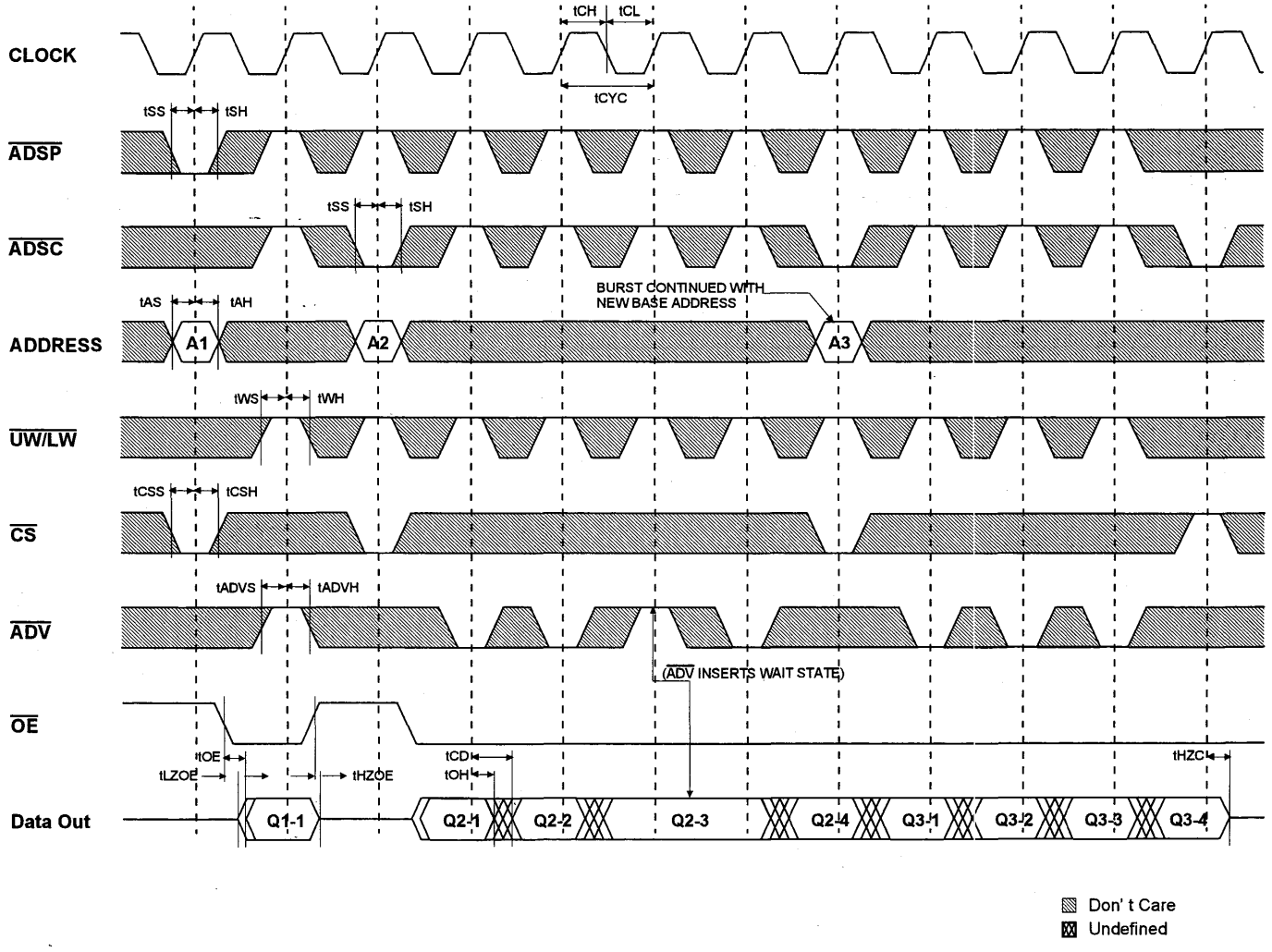
Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)



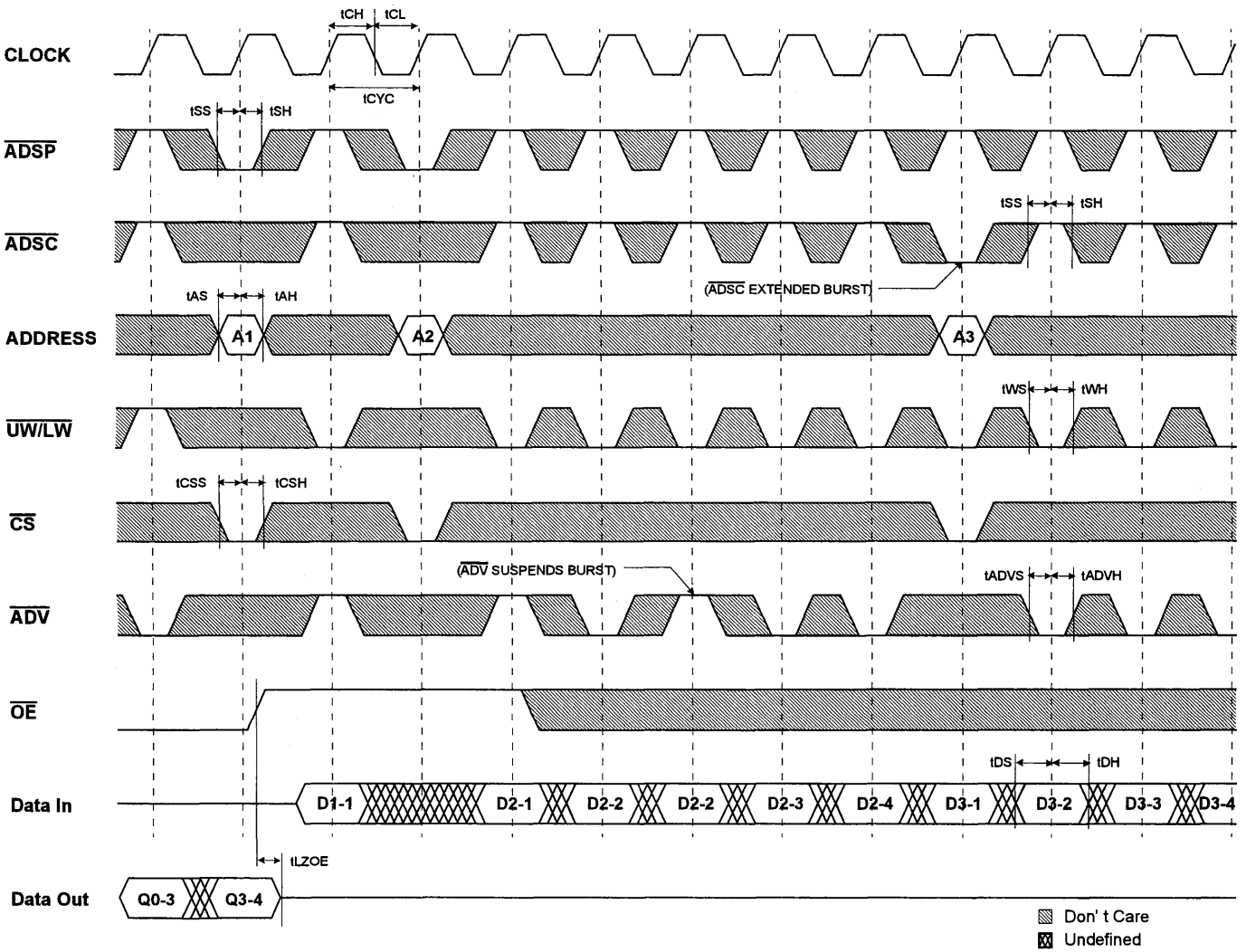
* Including Scope and Jig Capacitance

Fig. 1

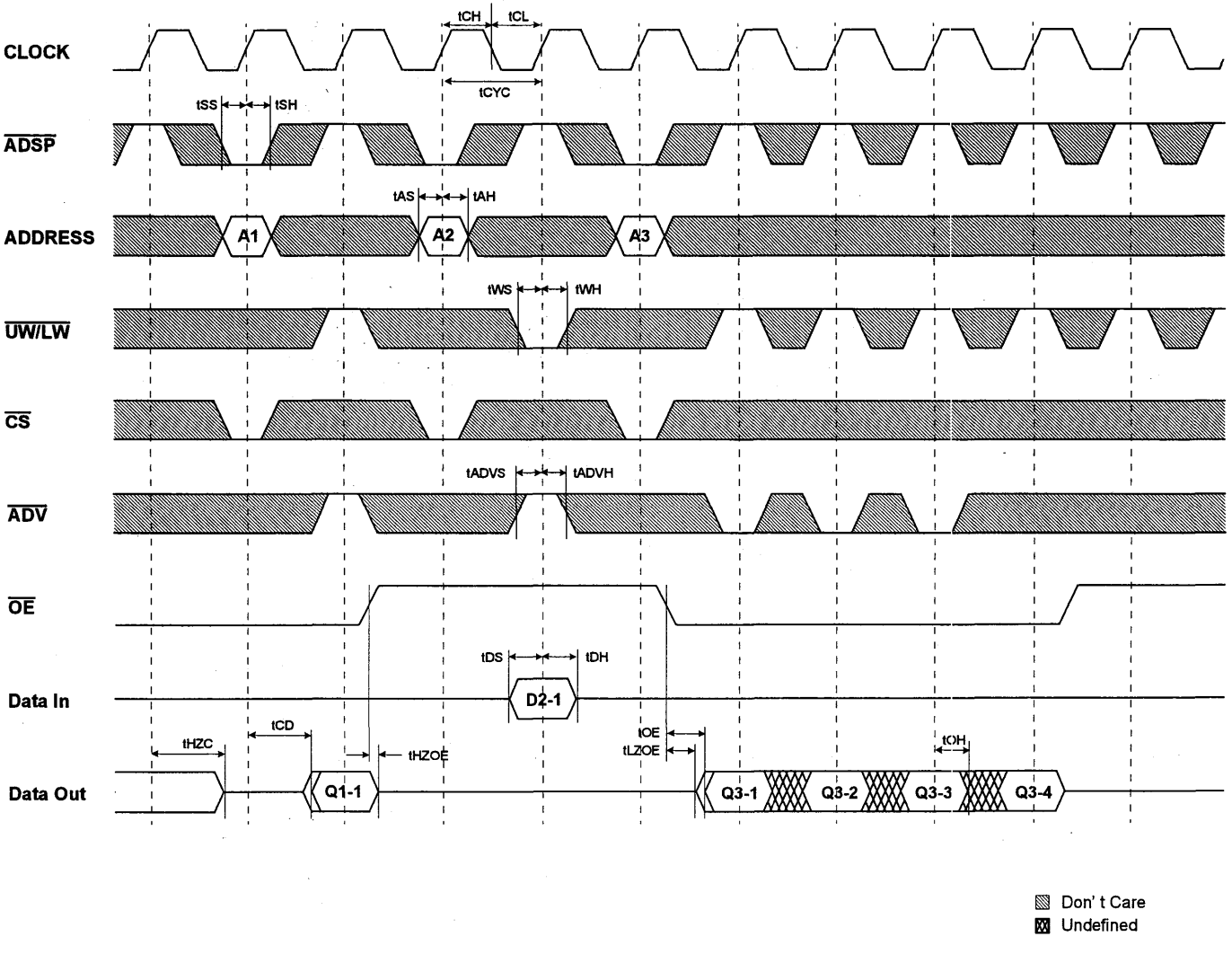
TIMING WAVEFORM OF READ CYCLE



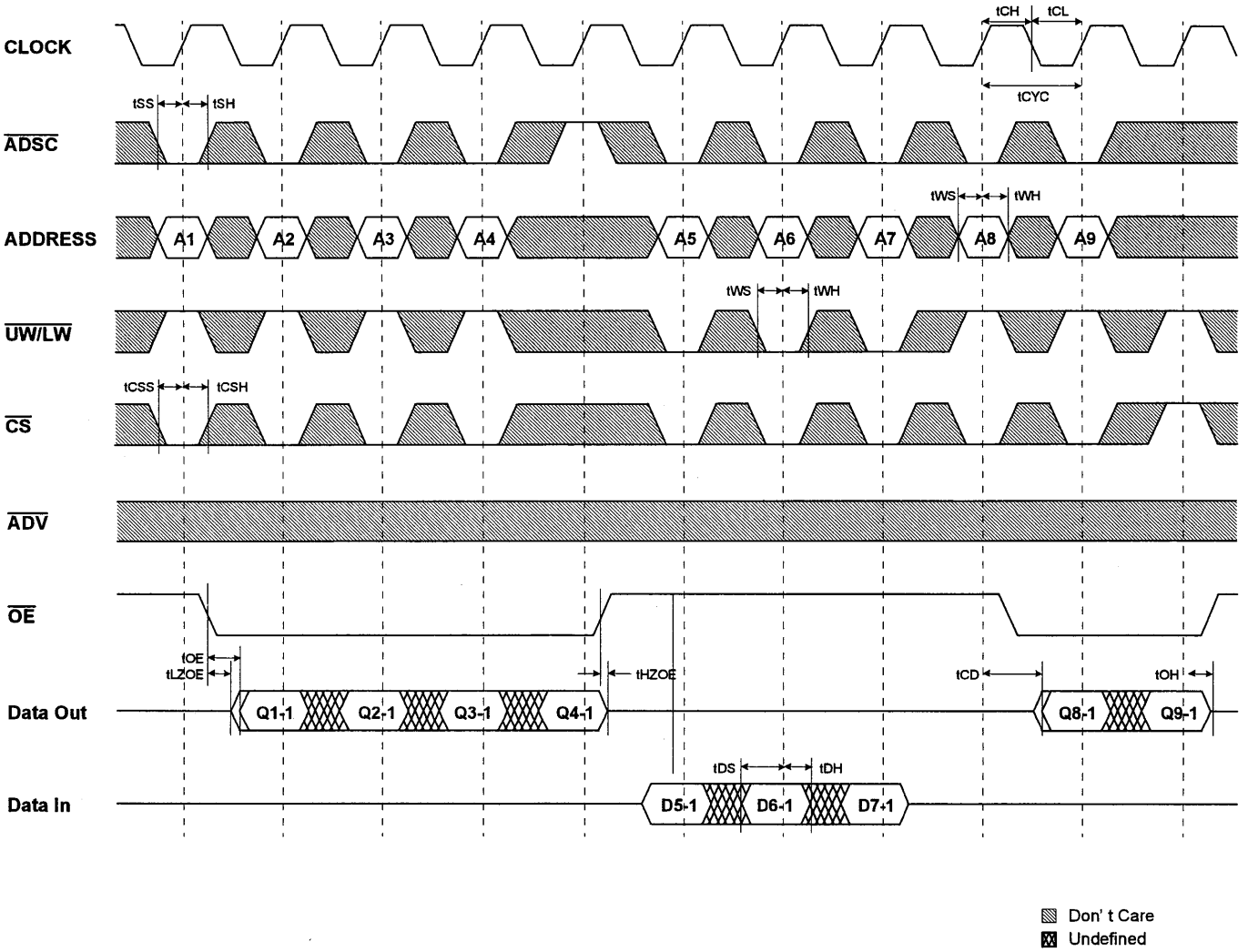
TIMING WAVEFORM OF WRTE CYCLE



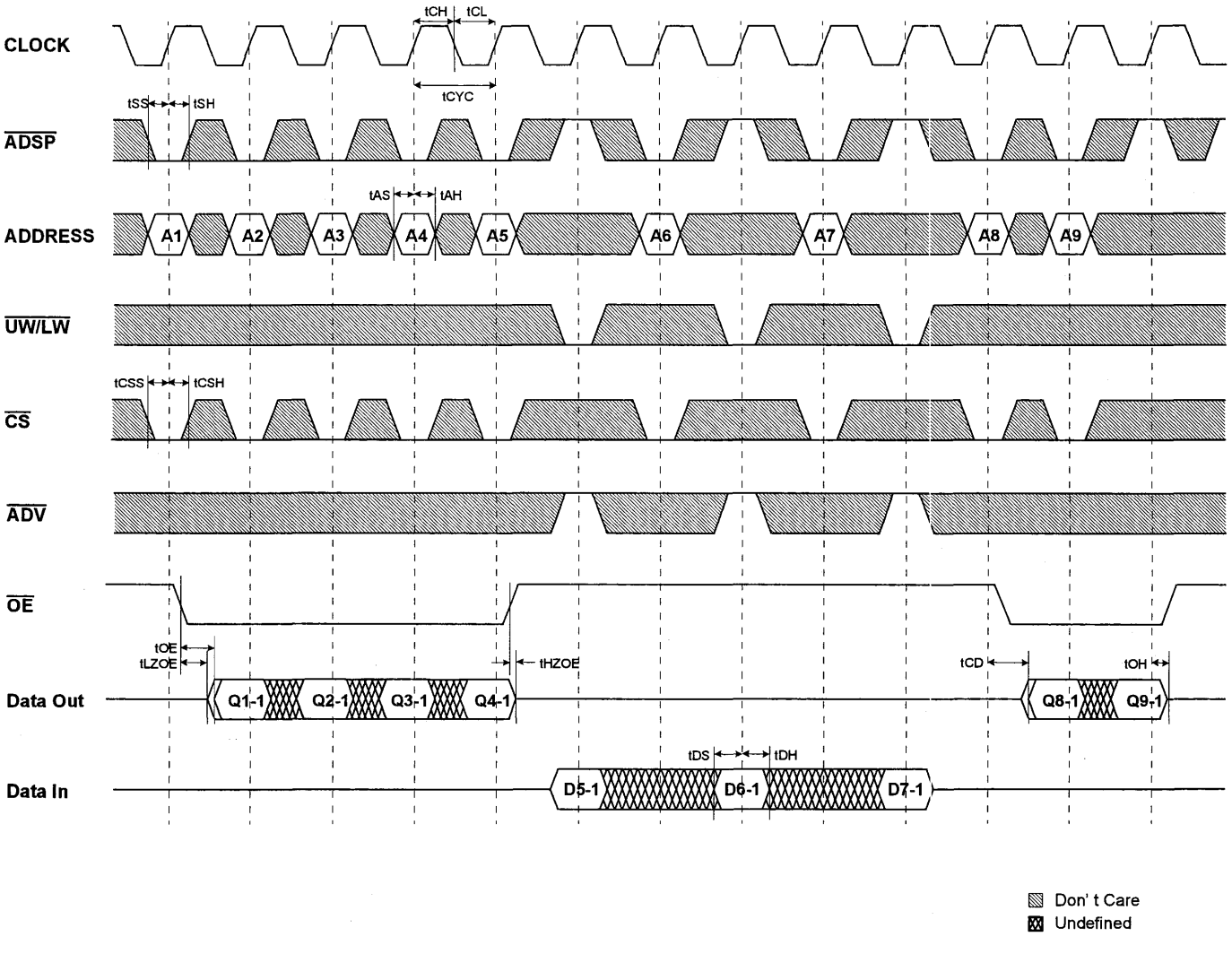
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



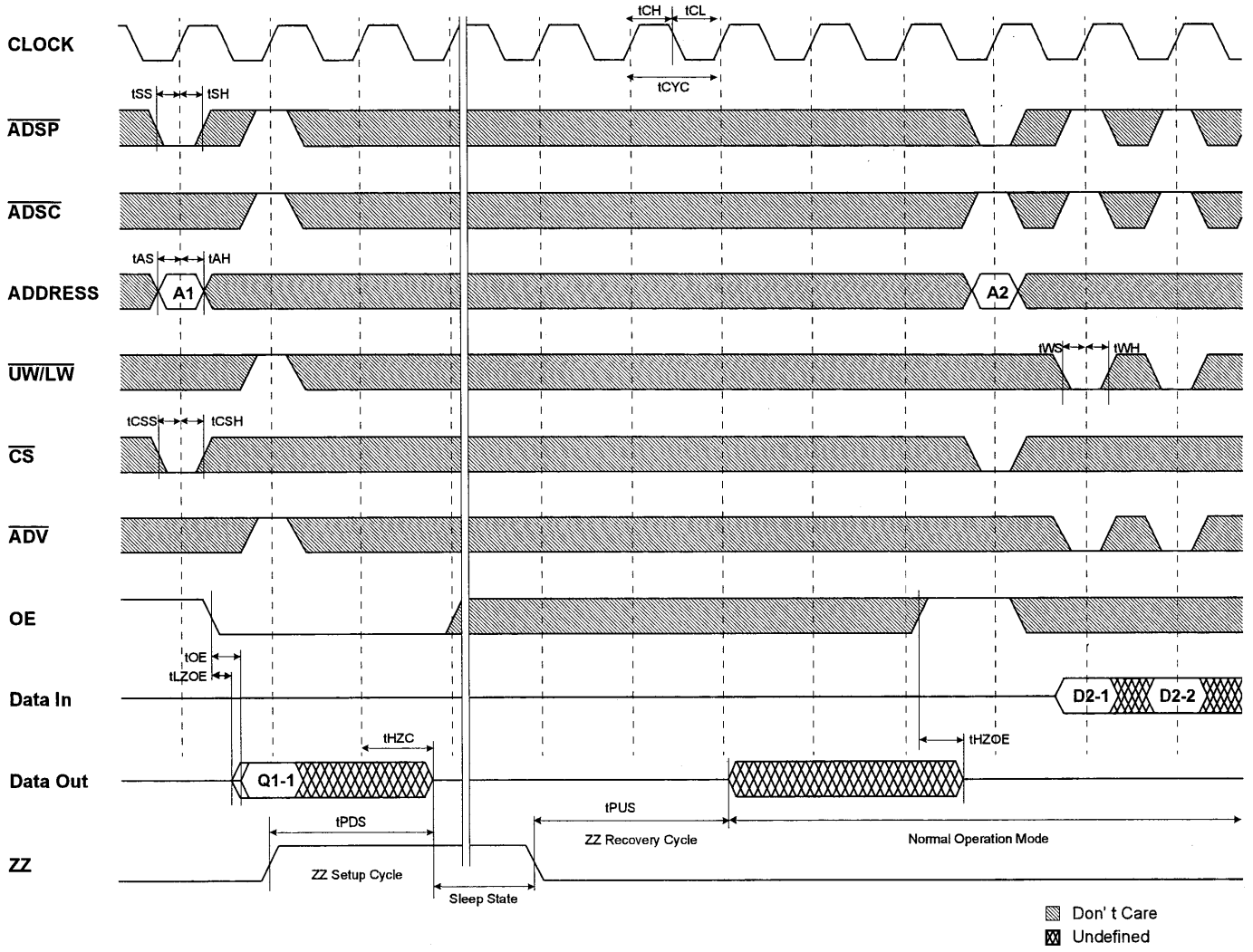
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ CONTROLLED, $\overline{ADSP}$=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



TIMING WAVEFORM OF POWER DOWN CYCLE



64Kx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- Single 5V ± 5% Power Supply.
- Byte Writable Function.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 3.3V I/O Compatible.
- 52-Pin PLCC Package.

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	-11	Unit
Cycle Time	tCYC	15	15	17	20	ns
Clock Access Time	tCD	8	9	10	11	ns
Output Enable Access Time	tOE	5	5	5	6	ns

GENERAL DESCRIPTION

The KM718B90 is a 1,179,648 bits Synchronous Static Random Access Memory designed to support 66MHz of Intel secondary caches.

It is organized as 65,536 words of 18 bits. And it integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components counts implementation of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous.

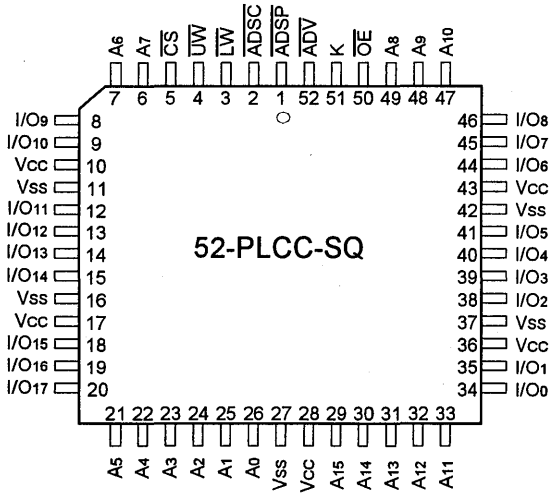
The self-timed write feature eliminates complex off chip write puise shaping iogic, simpiifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The KM718B90 is implemented with SAMSUNG's high performance BiCMOS technology and is available in a 52pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce.

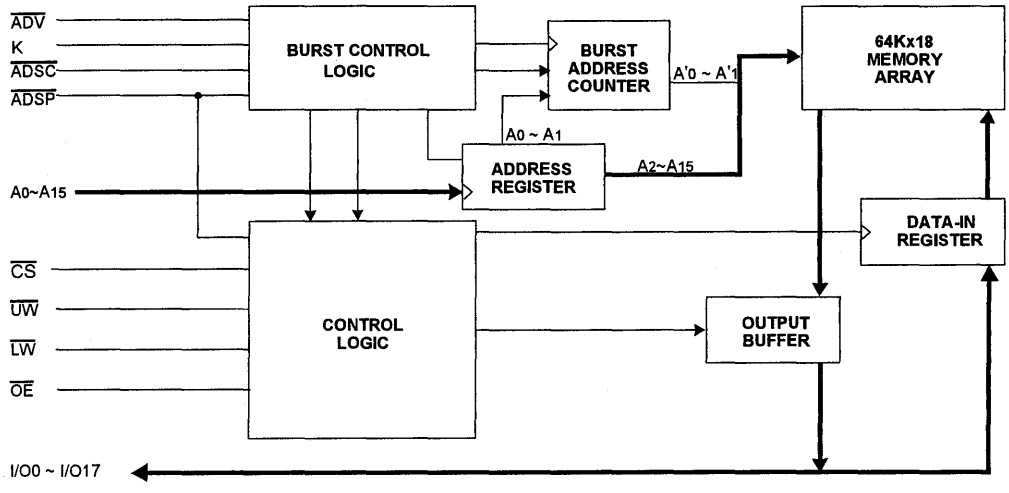
PIN CONFIGURATION(TOP VIEW)



PIN NAME

Pin Name	Pin Function
A0 - A15	Address Inputs
K	Clock
$\overline{LW}$, $\overline{UW}$	Write Enable
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
I/O0~I/O17	Data Inputs/Outputs
Vcc	+5V Power Supple
Vss	Ground

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718B90 is a synchronous SRAM designed to support the burst address accessing sequence of the Power microprocessor. All inputs(with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSP}$ and $\overline{ADSC}$. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with $\overline{ADV}$.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{LW}$, $\overline{UW}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sample low, The chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$, $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the next and subsequent clock edges. The address is increased internally for the next access of the burst when $\overline{LW}$, $\overline{UW}$ is sampled HIGH and $\overline{ADV}$ is sampled low.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{LW}$, $\overline{UW}$. $\overline{LW}$, $\overline{UW}$ is ignored on the clock edge that sampled ADSP low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when $\overline{LW}$, $\overline{UW}$ is sampled low (regardless of $\overline{OE}$). Data is clocked into the input register when $\overline{LW}$, $\overline{UW}$ is sampled low. The address increases internally to the next address of burst, if both $\overline{LW}$, $\overline{UW}$ and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed sampling low only one byte write enable signals($\overline{LW}$ or $\overline{LU}$)and $\overline{LW}$ controls I/O0~I/O7 and $\overline{UW}$ controls I/O8~I/O17.
Read or write cycles (depending on $\overline{LW}$, $\overline{LU}$)may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ are as follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
$\overline{LW}$, $\overline{UW}$ is sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst accesses as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

(Linear Burst)

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

SAMSUNG ELECTRONICS

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE(See Notes 1 and 2)

$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{LW}$/$\overline{UW}$	K	Address Accessed	Operation
H	L	X	X	X	↑	N/A	Not Selected
H	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Write Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE1 : X means "Don't Care".

NOTE2 : The rising edge of clock is symbolized by ↑.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{OE}$	Operation
L	Read I/O0~I/O17
H	Output High-Z
X	Not Selected, Outputs High-Z

NOTE1 : X means "Don't Care".

NOTE2 : For write cycles that follow read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.5 to 7.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***NOTE** : Sampled not 100% tested.

TEST CONDITIONS(T_A = 0℃ to 70℃, V_{DD} = 5V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 5V±5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{IL}	V_{DD} = Max ; V_{IN} = Vss to Vcc		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled		-2	+2	μA
Operating Current	I_{CC}	Vcc = Max I_{OUT} = 0mA Cycle Time ≥ tCYC min	15ns	-	270	mA
			17ns	-	260	
			20ns	-	250	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, Min Cycle All Inputs= V_{IH} and V_{IL}, V_{IH} ≥3V and V_{IL}=0v		-	90	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	3.3	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.2	Vcc+5.5	V

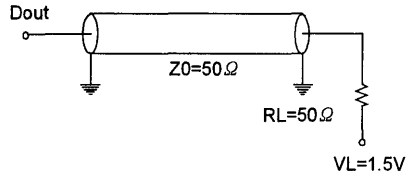
* V_{IL}(min) = -3.0(Pulse Width≤20ns)

AC TIMING CHARACTERISTICS(T_A = 0℃ to 70℃, V_{CC} = 5V±5%)

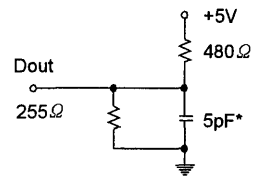
Parameter	Symbol	KM718B90-8		KM718B90-9		KM718B90-10		KM718B90-11		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	15	-	15	-	17	-	20	-	ns
Clock Access Time	tCD	-	8	-	9	-	10	-	11	ns
Output Enable to Data Valid	tOE	-	5	-	5	-	5	-	6	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	6	-	6	-	6	-	6	ns
Clock High Pulse Width	tCH	5	-	5	-	5	-	6	-	ns
Clock Low Pulse Width	tCL	5	-	5	-	5	-	6	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address/Advance Setup to Clock	tADVS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for this device to remain enabled.

Output Load(A)



Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)

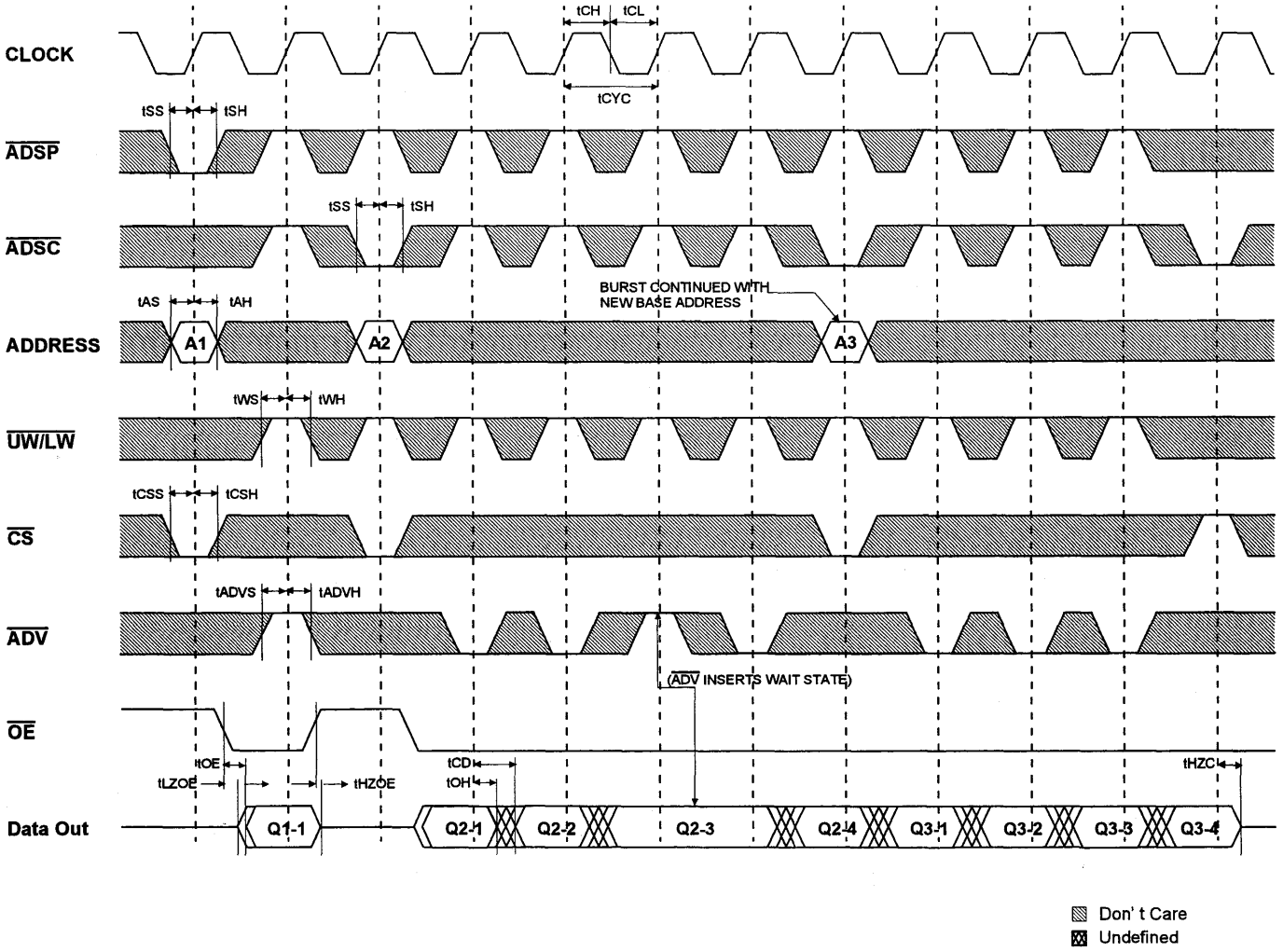


* Including Scope and Jig Capacitance

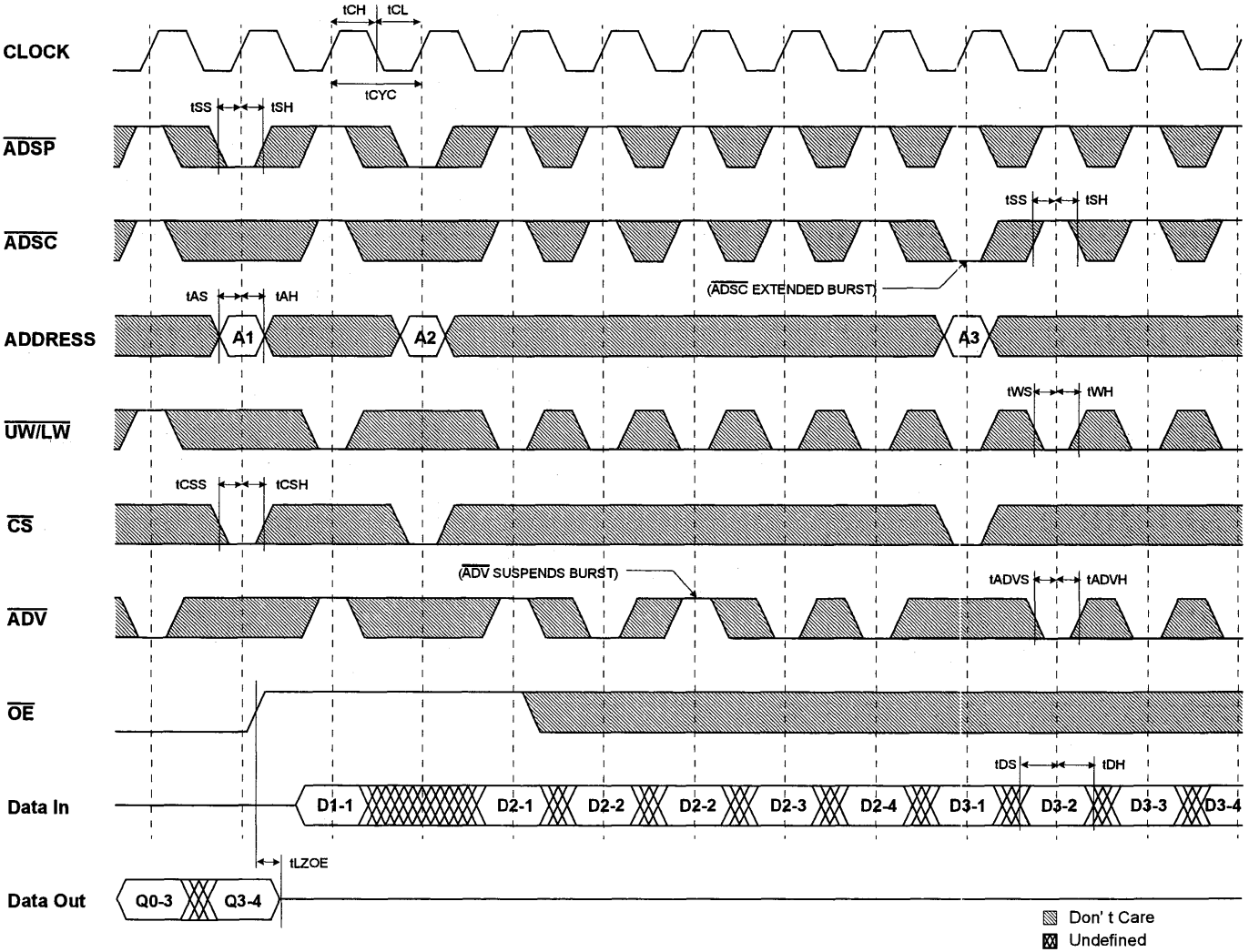
Fig. 1

SAMSUNG ELECTRONICS

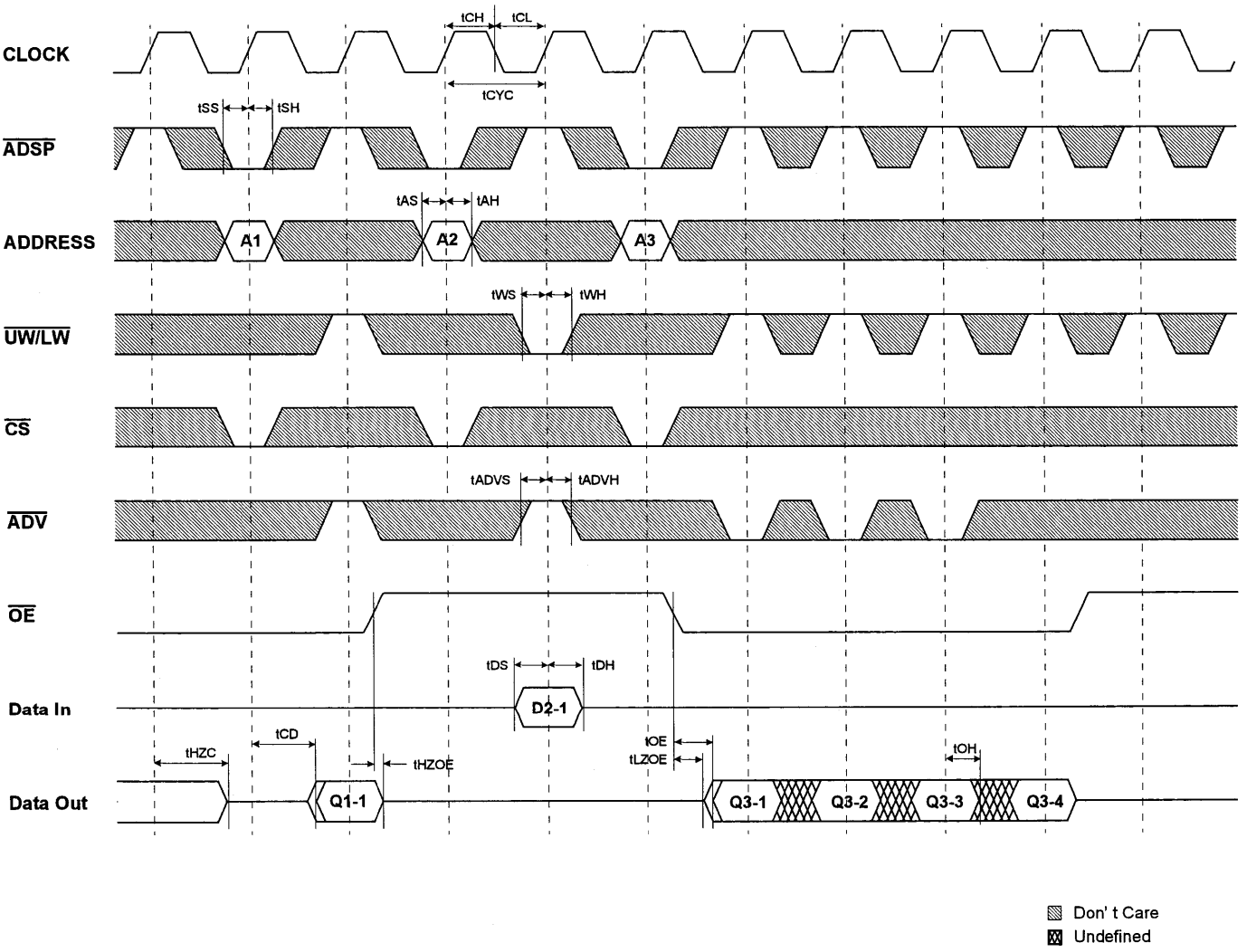
TIMING WAVEFORM OF READ CYCLE



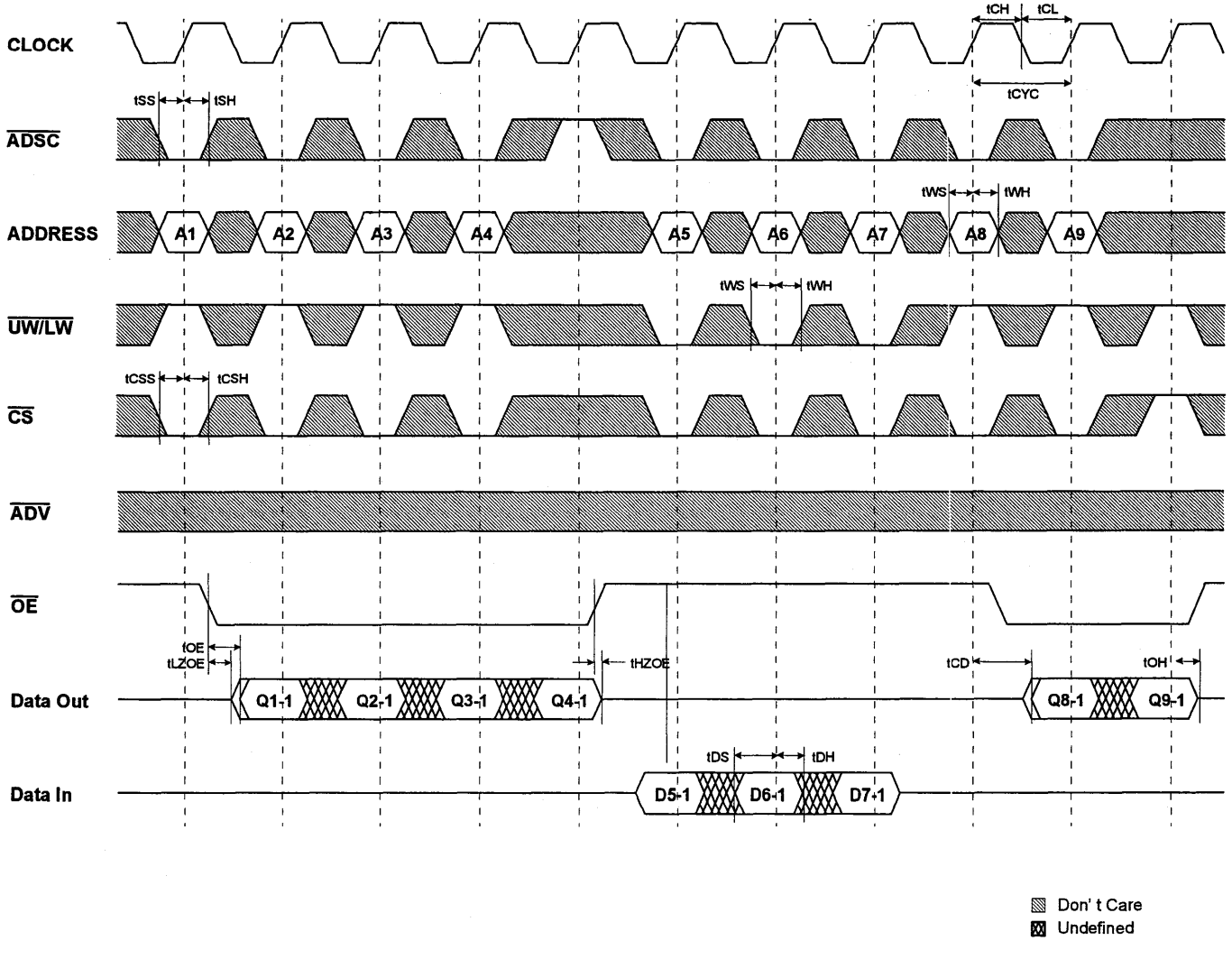
TIMING WAVEFORM OF WRTE CYCLE



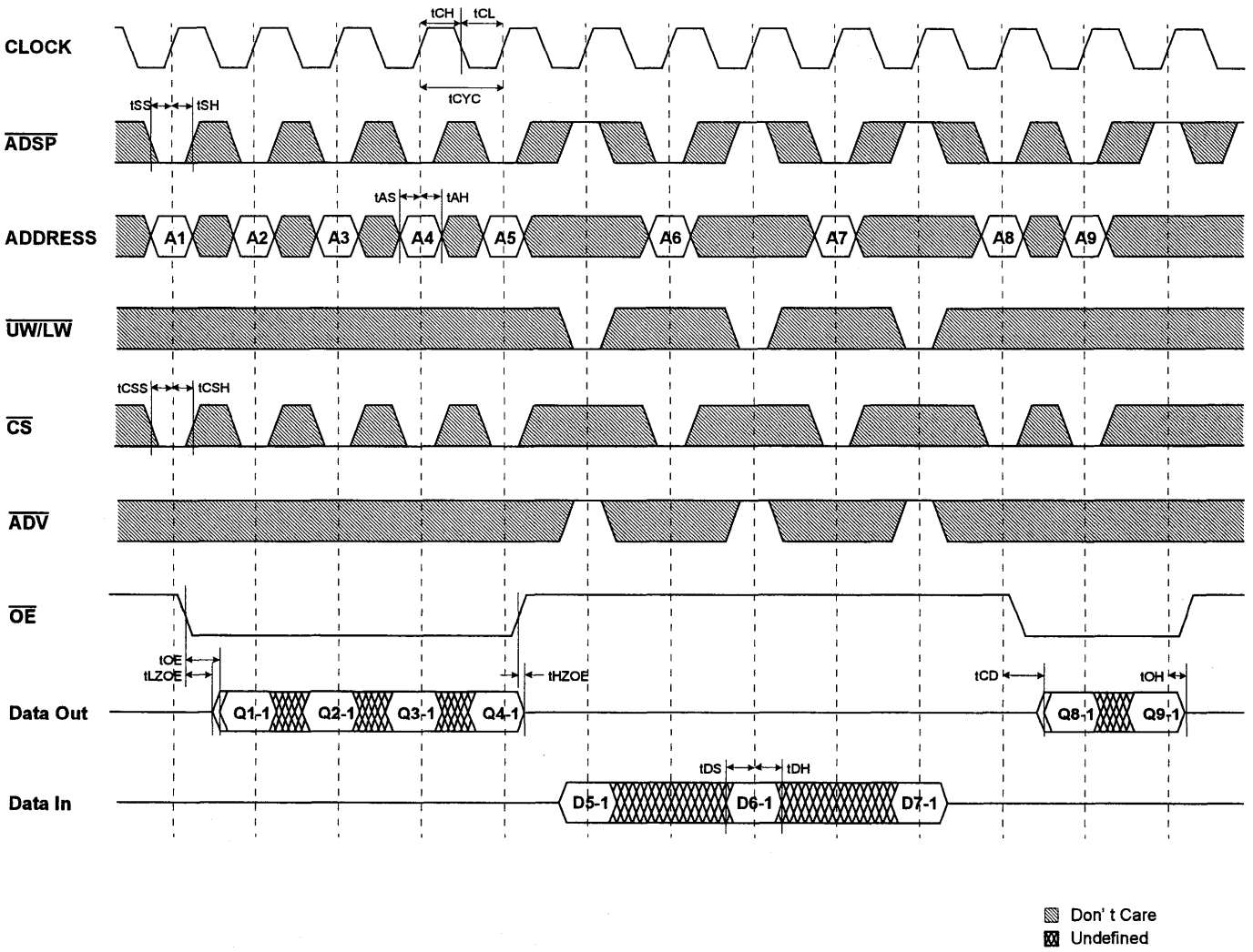
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



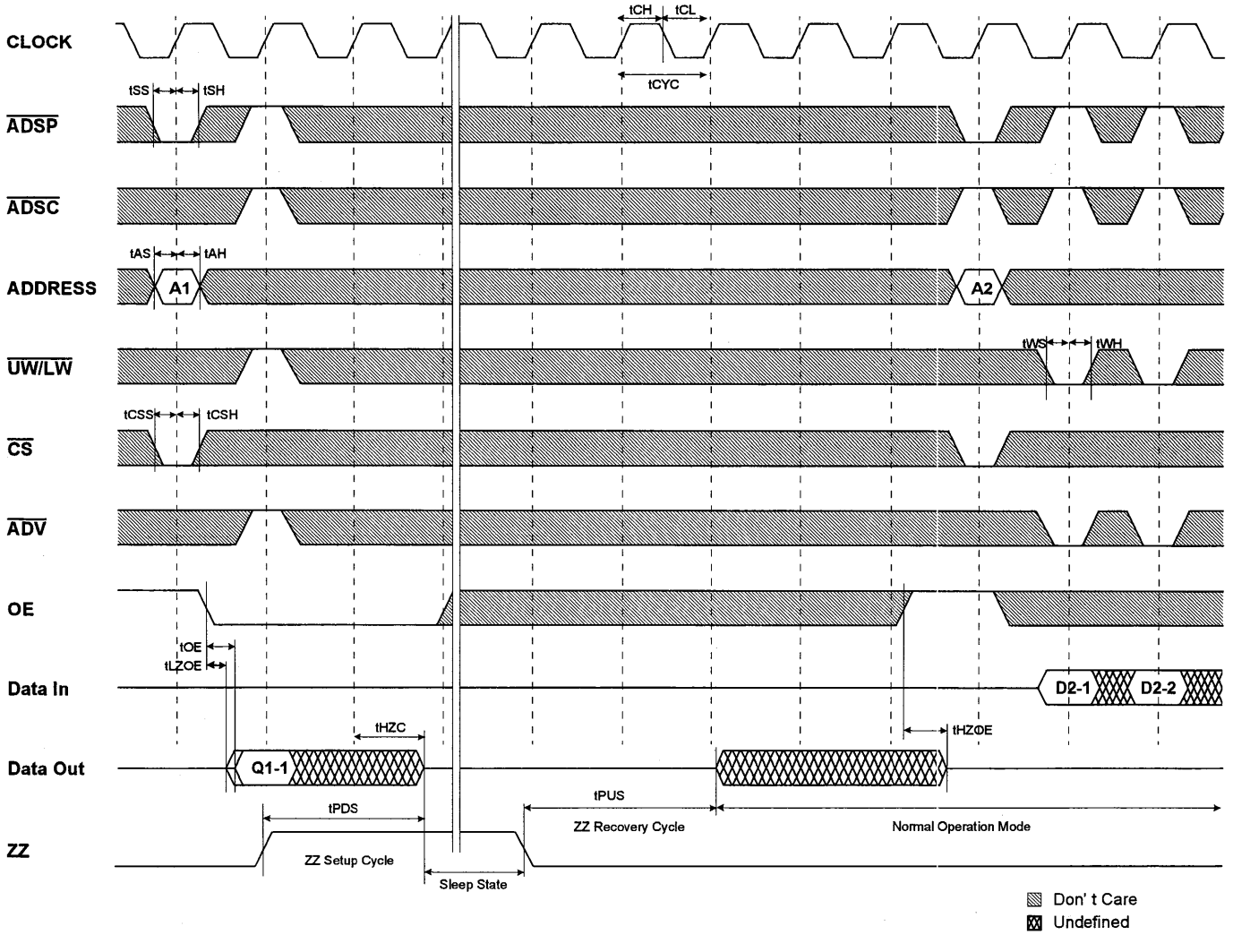
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ CONTROLLED, $\overline{ADSP}$=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



TIMING WAVEFORM OF POWER DOWN CYCLE



64Kx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- Single 3.3V ± 5% Power Supply.
- Byte Writable Function.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 5V I/O Compatible.
- 52-Pin PLCC Package.

FAST ACCESS TIMES

Parameter	Symbol	-9	-10	-12	Unit
Cycle Time	tCYC	15	17	20	ns
Clock Access Time	tCD	9	10	12	ns
Output Enable Access Time	tOE	5	5	6	ns

GENERAL DESCRIPTION

The KM718BV87 is a 1,179,648 bits Synchronous Static Random Access Memory designed to support zero wait state performance with advanced i486/Pentium address pipelining.

When $\overline{CS}$ is high, $\overline{ADSP}$ is blocked to control singles.

It is organized as 65,536 words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components count implementations of high performance cache RAM applications.

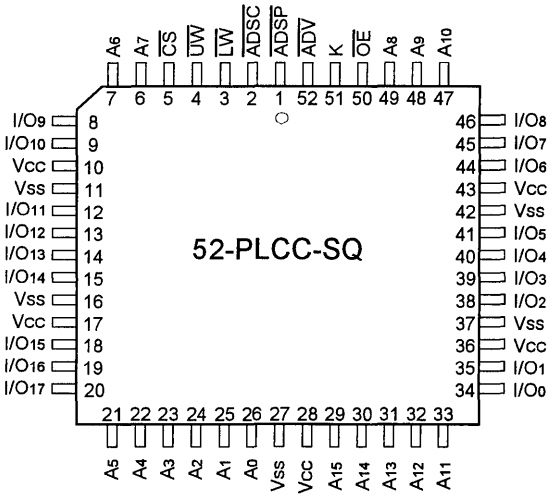
Write cycles are internally self-timed and synchronous.

The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

The KM718BV87 is implemented with SAMSUNG's high performance BiCMOS technology and is available in a 52pin PLCC package. Multiple power and ground pins are utilized to minimize ground bounce.

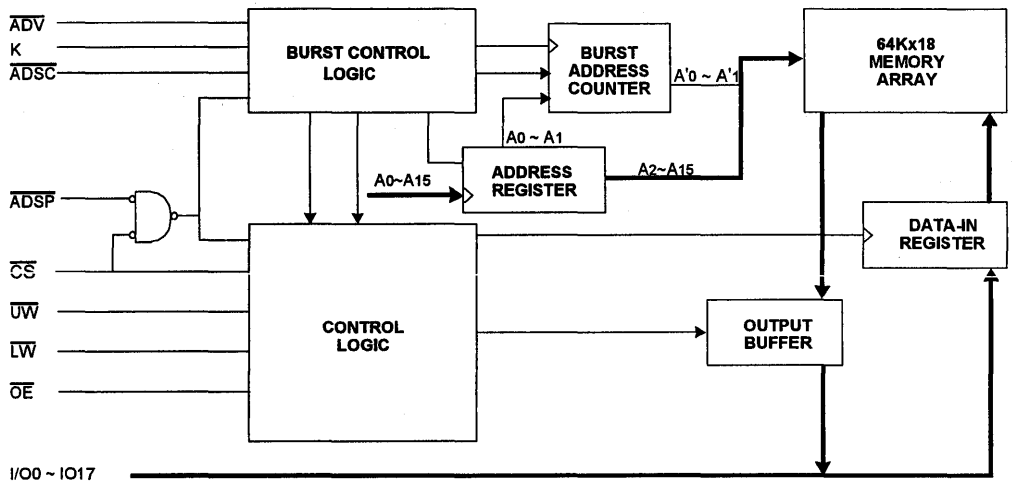
PIN CONFIGURATION(TOP VIEW)



PIN NAME

Pin Name	Pin Function
A0 - A15	Address Inputs
K	Clock
$\overline{LW}$, $\overline{UW}$	Write Enable
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
I/O0~I/O17	Data Inputs/Outputs
Vcc	+3.3V Power Supple
Vss	Ground

LOGIC BLOCK DIAGRAM



FUNCTION DESCRIPTION

The KM718BV87 is a synchronous SRAM designed to support the burst address accessing sequence of the i486/586 microprocessor. All inputs(with the exception of $\overline{OE}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$ and $\overline{ADSP}$. The accesses are enabled with the chip select signals and output enable. Wait states are inserted into the access with $\overline{ADV}$.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{LW}$, $\overline{UW}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sample low, The chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$, $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the next and subsequent clock edges. The address is increased internally for the next access of the burst when $\overline{LW}$, $\overline{UW}$ is sampled HIGH and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS}$.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{LW}$, $\overline{UW}$. $\overline{LW}$, $\overline{UW}$ is ignored on the clock edge that samples $\overline{ADSP}$ low, but is sampled on the next and subsequent clock edges. The output buffers are disabled when $\overline{LW}$, $\overline{UW}$ is sampled low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{LW}$, $\overline{UW}$ is sampled low. The address increases internally to the next address of burst, if both $\overline{LW}$, $\overline{UW}$ and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by sampling low only one byte write enable signals($\overline{LW}$ or $\overline{LU}$)and $\overline{LW}$ controls I/O0~I/O7 and $\overline{UW}$ controls I/O8~I/O17.
Read or write cycles (depending on $\overline{LW}$, $\overline{LU}$)may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSP}$ and $\overline{ADSC}$ are as follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
$\overline{LW}$, $\overline{UW}$ is sampled on the same clock edge that sampled $\overline{ADSC}$ loe(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

BURST SEQUENCE TABLE

(Interleaved Burst)

	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE(See Notes 1 and 2)

$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{LW}$/$\overline{UW}$	K	Address Accessed	Operation
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
H	X	L	X	X	↑	N/A	Not Selected
H	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle

NOTE1 : X means "Don't Care".

NOTE2 : The rising edge of clock is symbolized by ↑.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

$\overline{OE}$	Operation
L	Read I/O0~I/O17
H	Output High-Z
X	Not Selected, Outputs High-Z

NOTE1 : X means "Don't Care".

NOTE2 : For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{CC}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	3.13	3.3	3.47	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***NOTE** : Sampled not 100% tested.

TEST CONDITIONS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Max ; V_{IN} = Vss to V_{CC}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled		-2	+2	μA
Operating Current	I_{CC}	V_{CC} = Max I_{OUT} = 0mA Cycle Time ≥ tCYC min	15ns	-	270	mA
			17ns	-	260	
			20ns	-	250	
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, I_{OUT} = 0mA, Min Cycle		-	80	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.2	+5.5	V

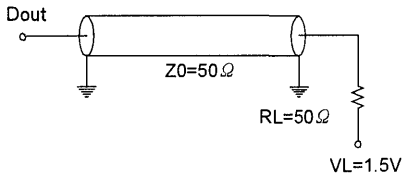
* V_{IL}(min) = -3.0(Pulse Width≤20ns)

AC TIMING CHARACTERISTICS(T_A = 0℃ to 70℃, V_{CC} = 5V±5%)

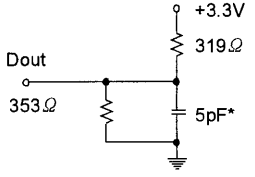
Parameter	Symbol	KM718BV87-9		KM718BV87-10		KM718BV87-12		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	15	-	17	-	20	-	ns
Clock Access Time	tCD	-	9	-	10	-	12	ns
Output Enable to Data Valid	tOE	-	5	-	5	-	6	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	6	-	6	-	6	ns
Clock High Pulse Width	tCH	5	-	5	-	6	-	ns
Clock Low Pulse Width	tCL	5	-	5	-	6	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	ns
Address/Advance Setup to Clock High	tADVS	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for this device to remain enabled.

Output Load(A)



Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)

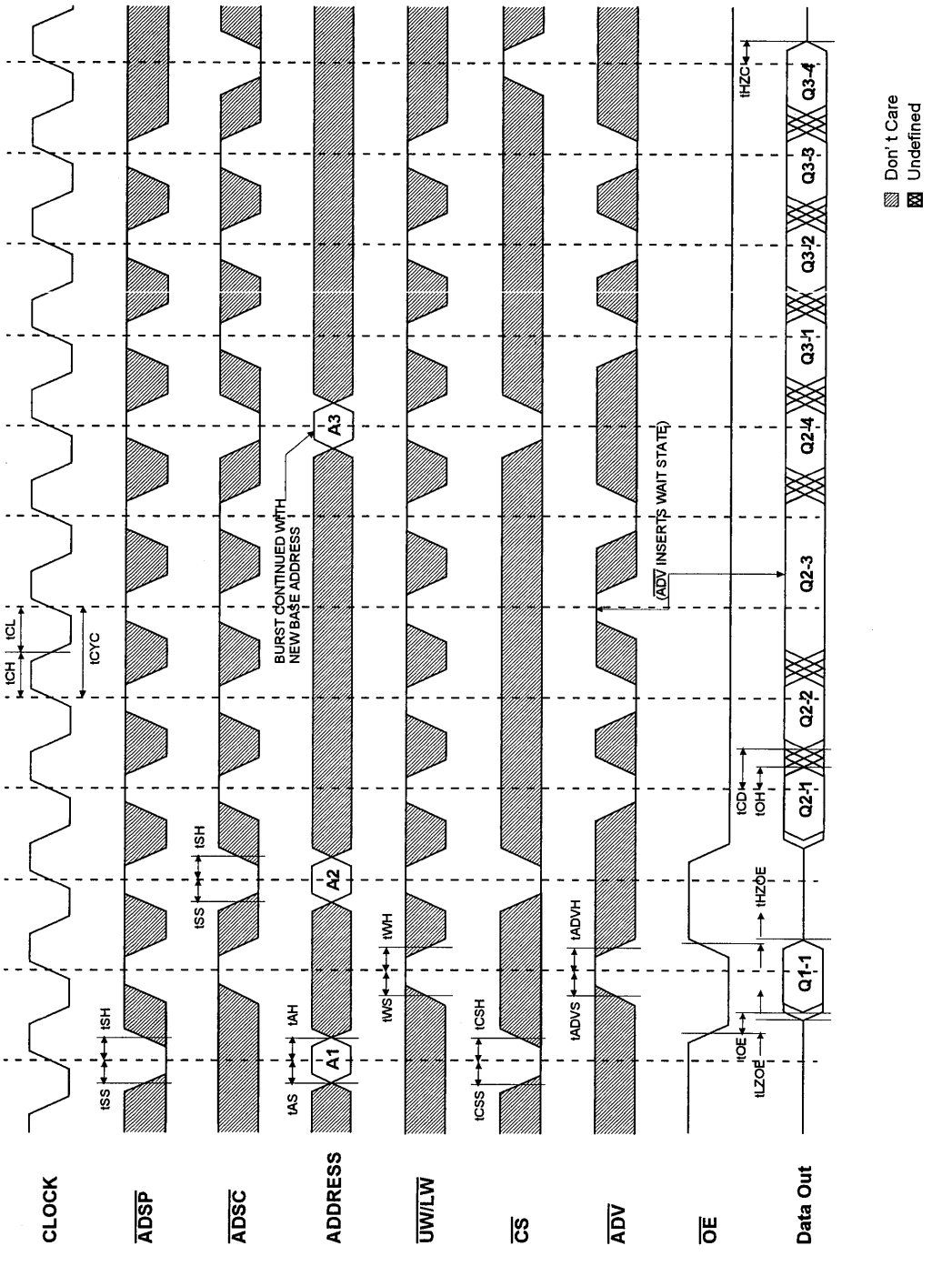


* Including Scope and Jig Capacitance

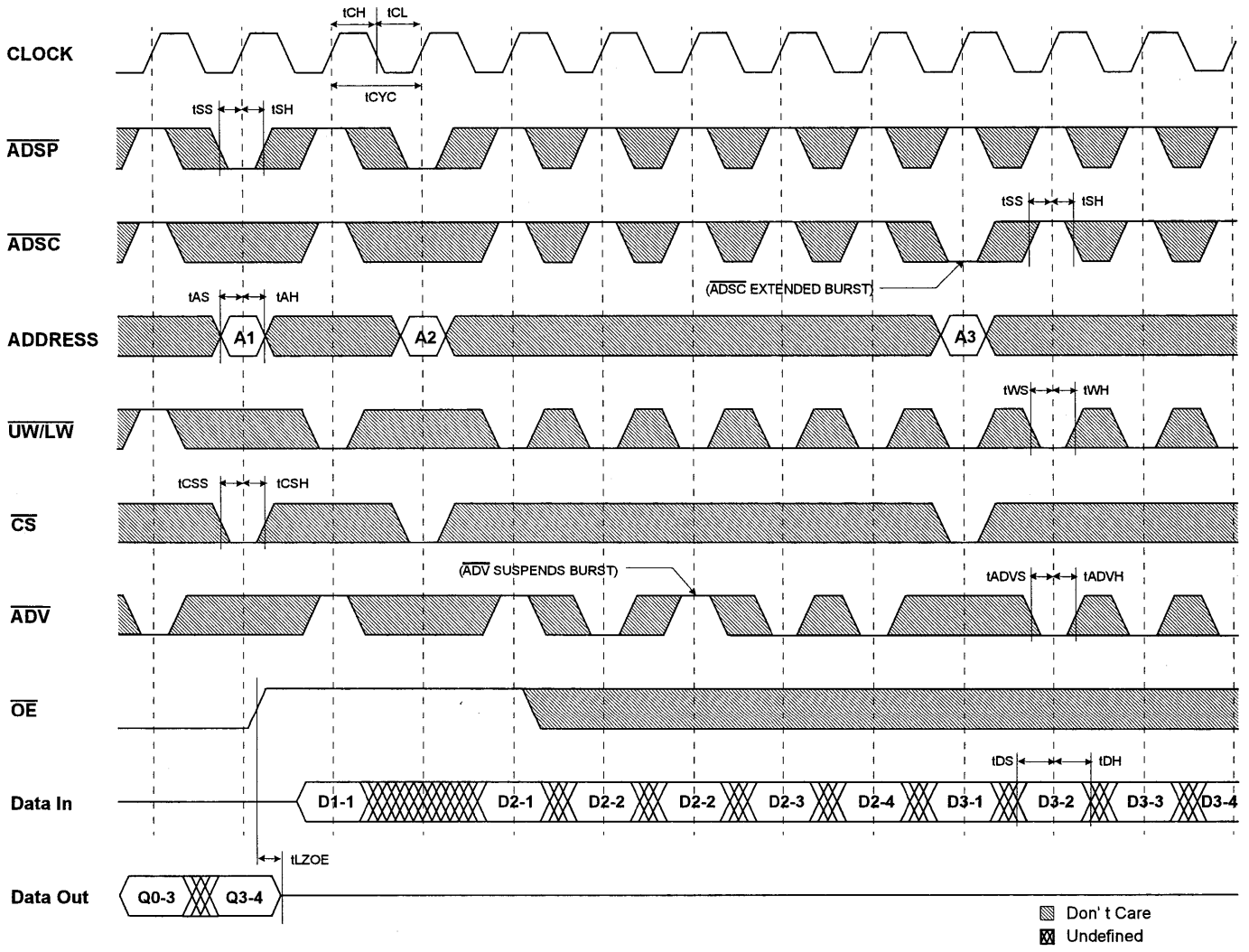
Fig. 1

SAMSUNG ELECTRONICS

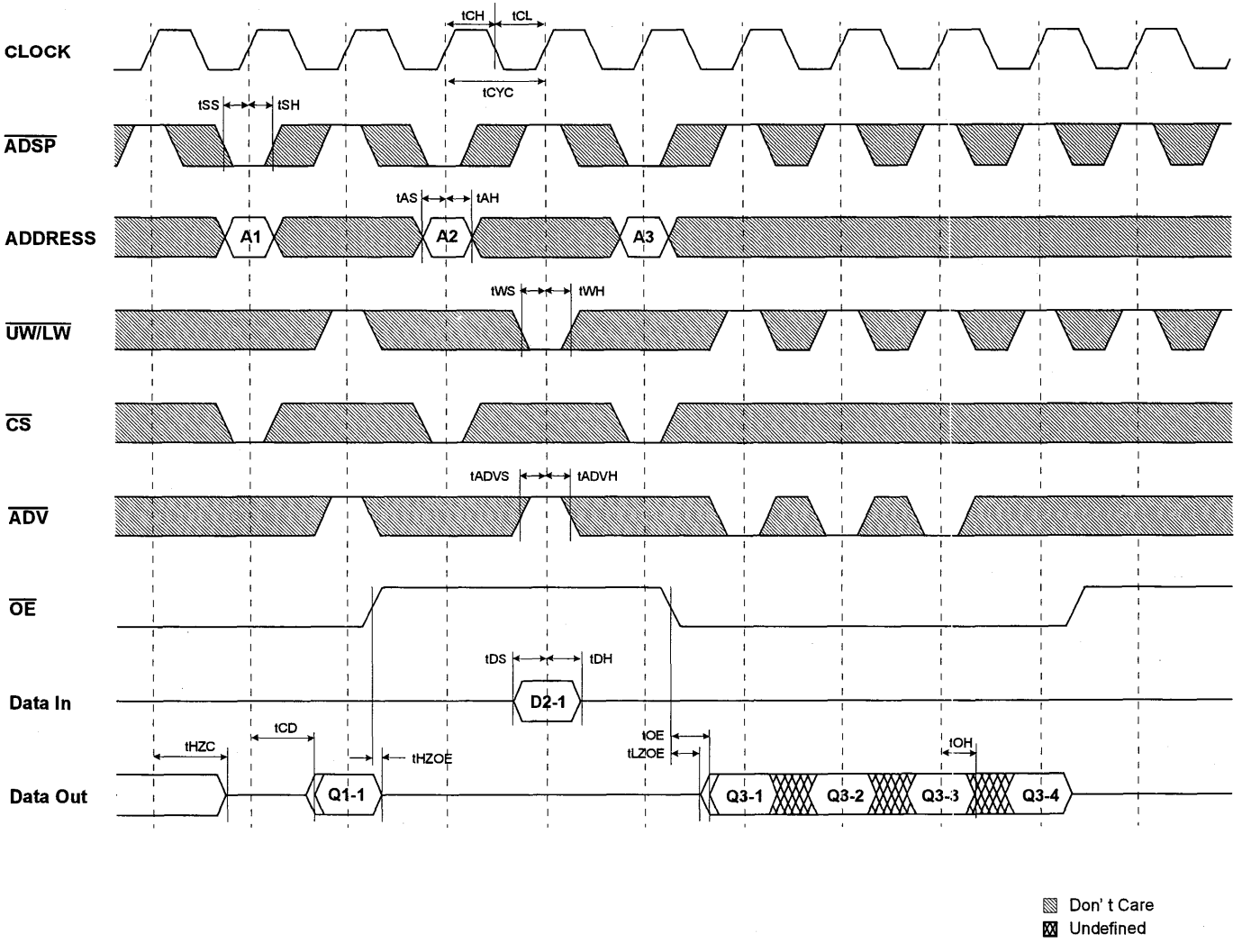
TIMING WAVEFORM OF READ CYCLE



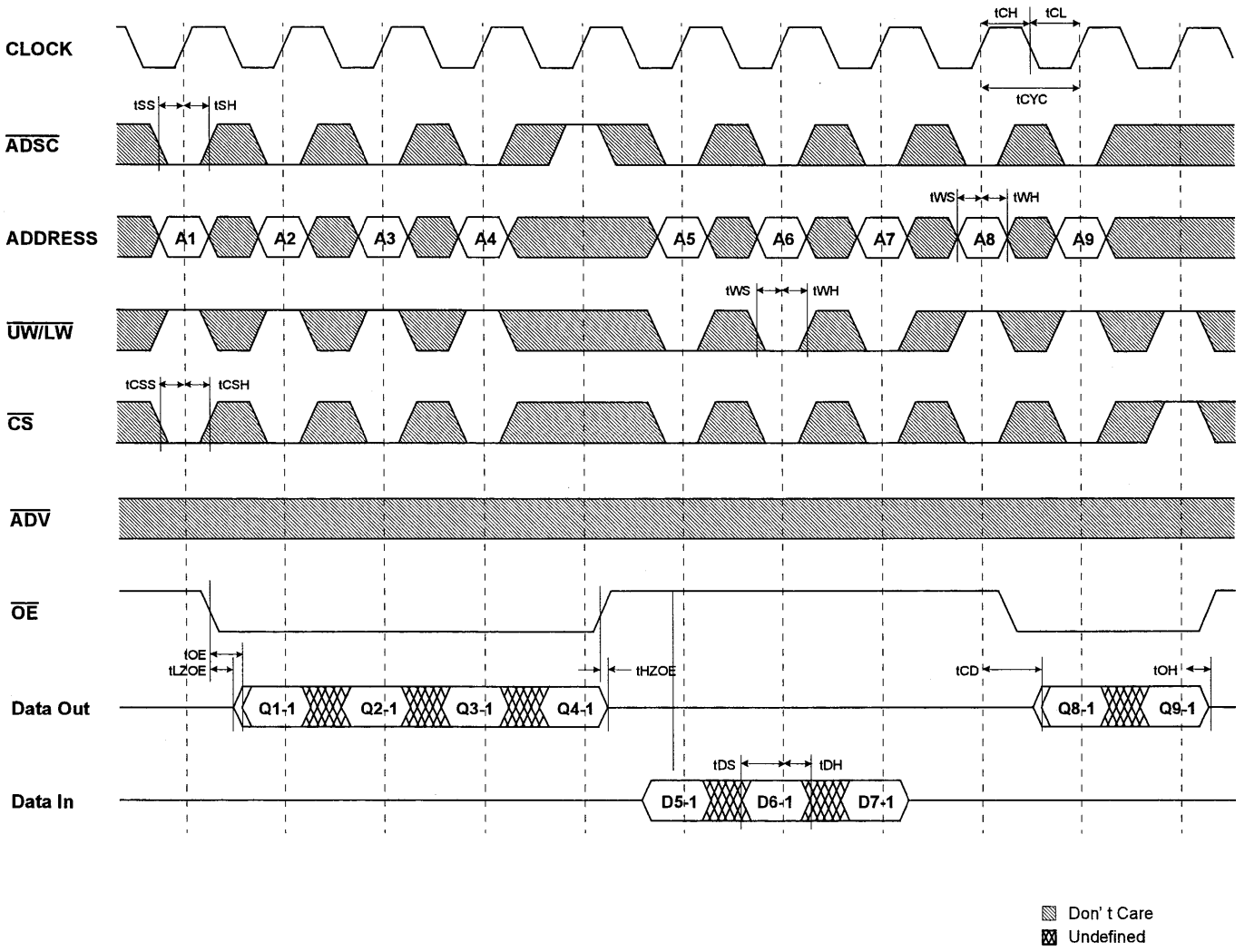
TIMING WAVEFORM OF WRTE CYCLE



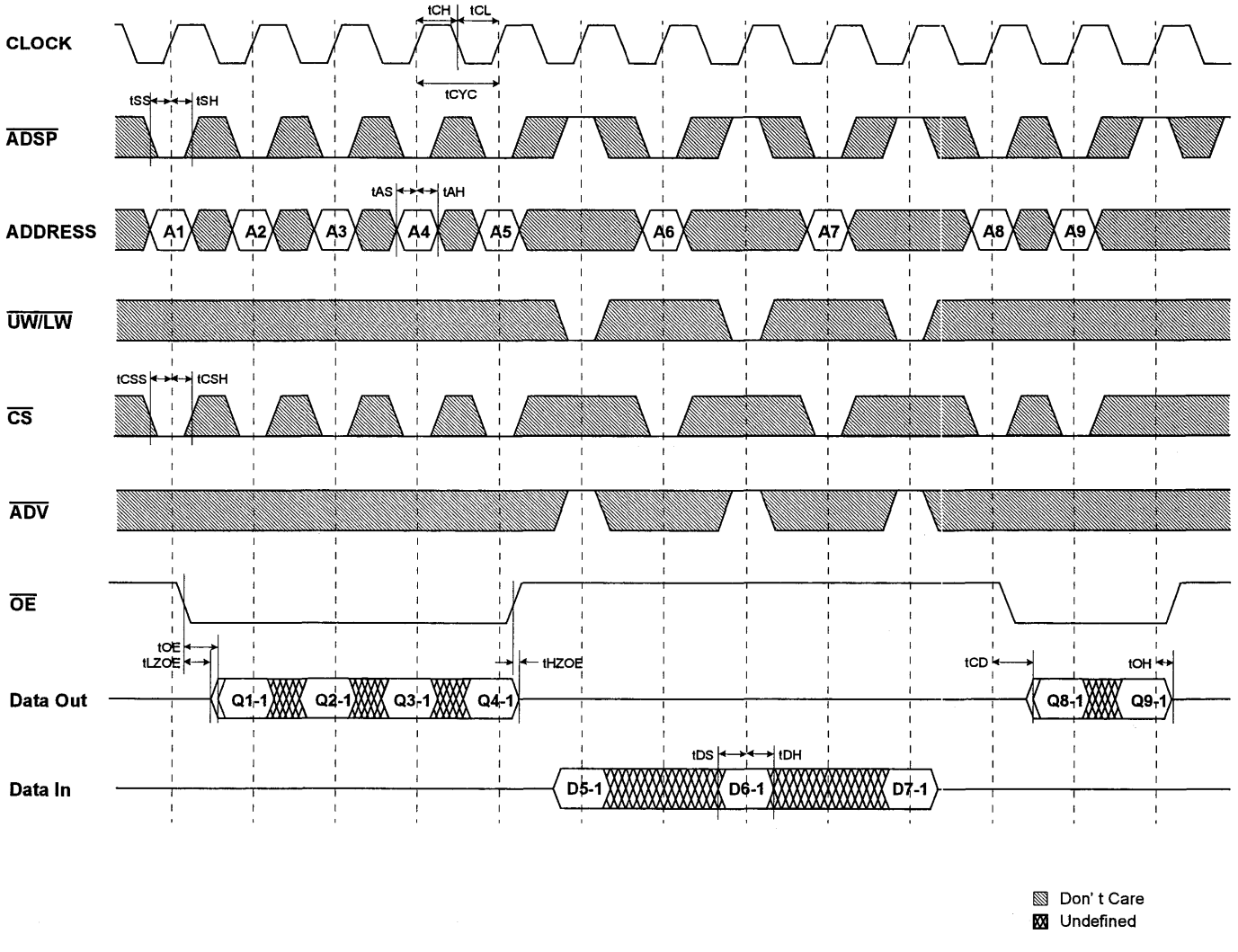
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



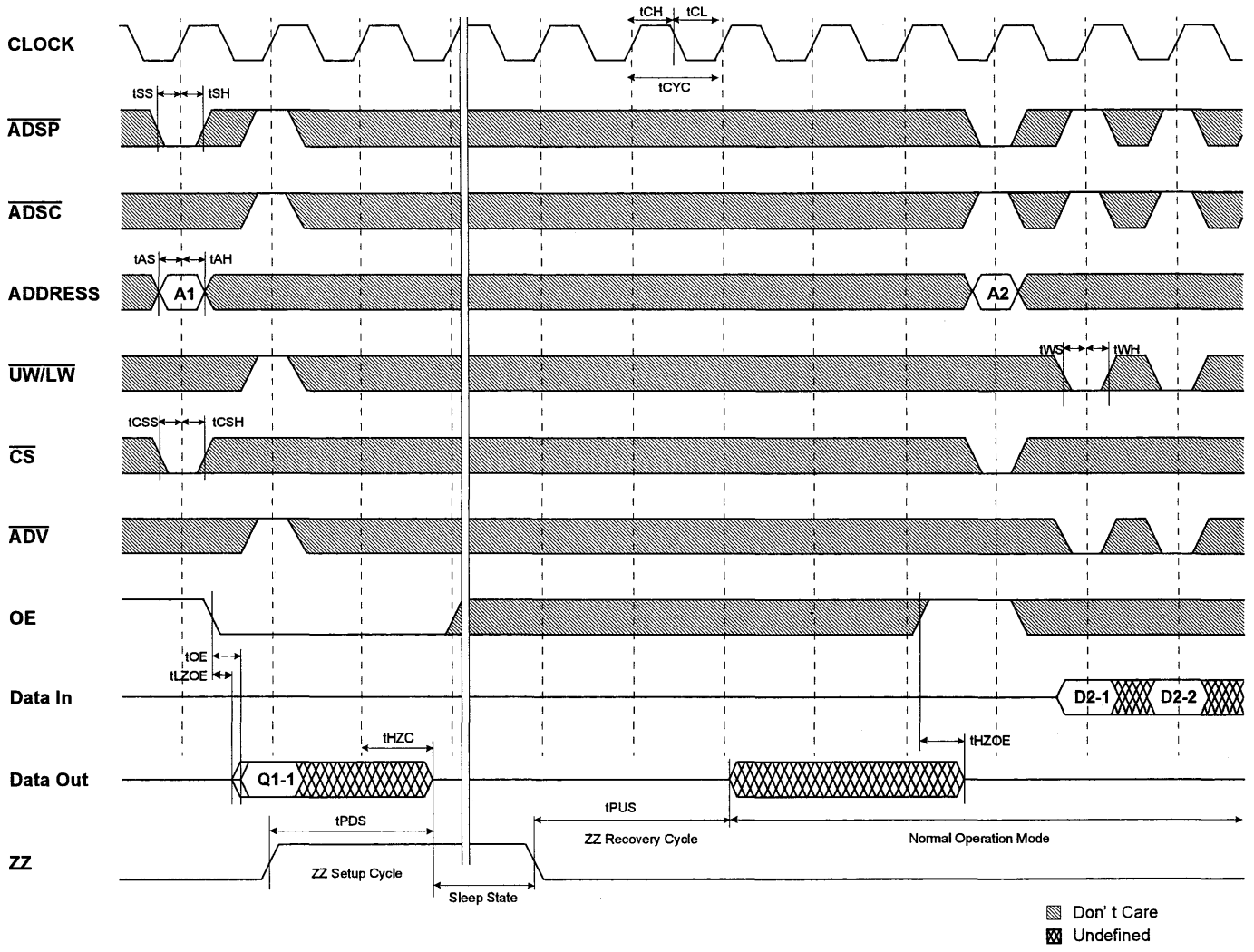
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ CONTROLLED, $\overline{ADSP}$=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



TIMING WAVEFORM OF POWER DOWN CYCLE



32Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- Single 3.3V-5%/+10% Power Supply
- 5V Tolerant Inputs except I/O Pins
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-Pin QFP/TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	-17	Unit
Cycle Time	tCYC	13	15	17	ns
Clock Access Time	tCD	7	8	9	ns
Output Enable Access Time	tOE	6	7	8	ns

GENERAL DESCRIPTION

The KM732V589/L is a 1,048,576-bit Synchronous Static Random Access Memory designed for high performance second level cache of i486/Pentium and Power PC based System.

It is organized as 32K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WEx}$ and $\overline{BW}$ when $\overline{GW}$ is high.

And with $\overline{CS1}$ high, $\overline{ADSP}$ disable to support address pipelining.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs.

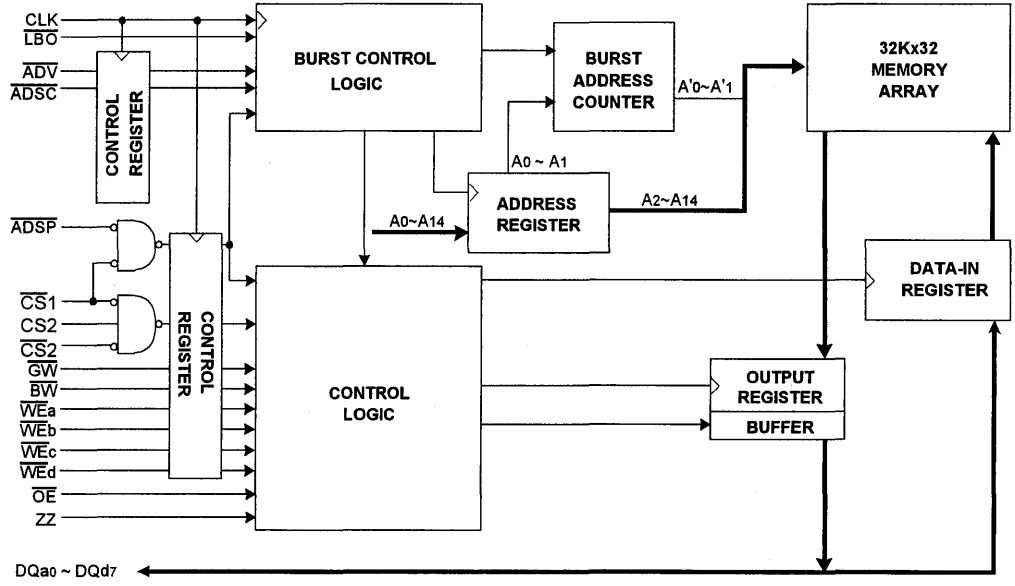
Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

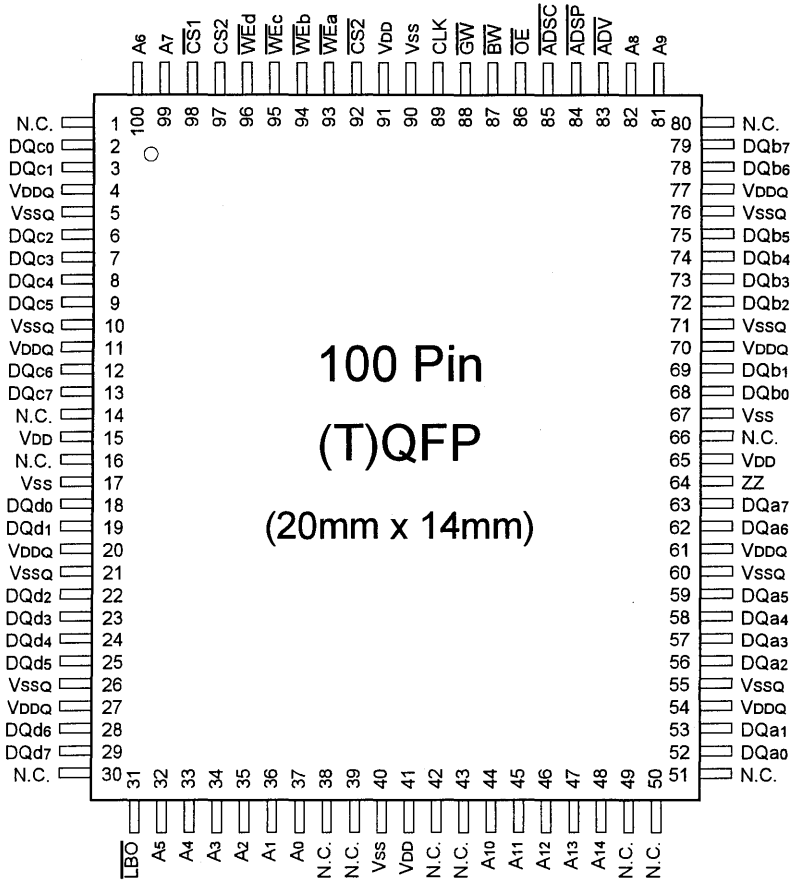
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The KM732V589/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin QFP/TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,81, 82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			Vss	Ground	17,40,67,90
			N.C.	No Connect	1,14,16,30,38,39,42,43, 49,50,51,66,80
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97			
$\overline{CS2}$	Chip Select	92	VDDQ	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
$\overline{WEx}$	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM732V589/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$. The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WEx}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WEx}$ are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$(regardless of $\overline{BW}$ and $\overline{WEx}$.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WEx}$ when $\overline{GW}$ is high.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WEx}$. $\overline{WEx}$ are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WEx}$ are sampled Low(regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WEx}$ sampled Low. The address increases internally to the next address of burst, if both $\overline{WEx}$ and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WEa}$, $\overline{WEb}$, $\overline{WEc}$ or $\overline{WEd}$) sampled low. The $\overline{WEa}$ controls $DQa_0 \sim DQa_7$, $\overline{WEb}$ controls $DQb_0 \sim DQb_7$, $\overline{WEc}$ controls $DQc_0 \sim DQc_7$, and $\overline{WEd}$ controls $DQd_0 \sim DQd_7$. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
$\overline{WEx}$ are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WRITE}$	Operation	$\overline{CS1}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.
2. $\overline{WE}$x means $\overline{WE}$a ~ $\overline{WE}$d.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
	V_{DDQ}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

CAPACITANCE*(T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(V_{DD}=3.3V-5%+10%, T_A = 0℃ to 70℃)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{IL}	V_{DD} = Vss to V_{DD} ; V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	-13	-	200	mA
			-15	-	180	
			-17	-	160	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V		-	30	mA
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	5	mA
			L-Ver.	-	1	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	5	mA
			L-Ver.	-	200	μA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.2	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)

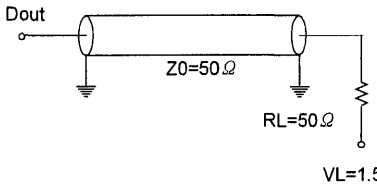
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

TEST CONDITIONS

(T_A = 0℃ to 70℃, V_{DD}=3.3V-5%/+10% unless otherwise specified)

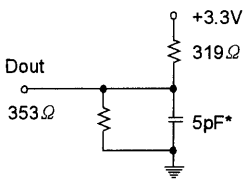
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)



* Capacitive Load consists of all components of the test environment.

Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

(V_{DD}=3.3V-5%/+10%, T_A = 0℃ to 70℃)

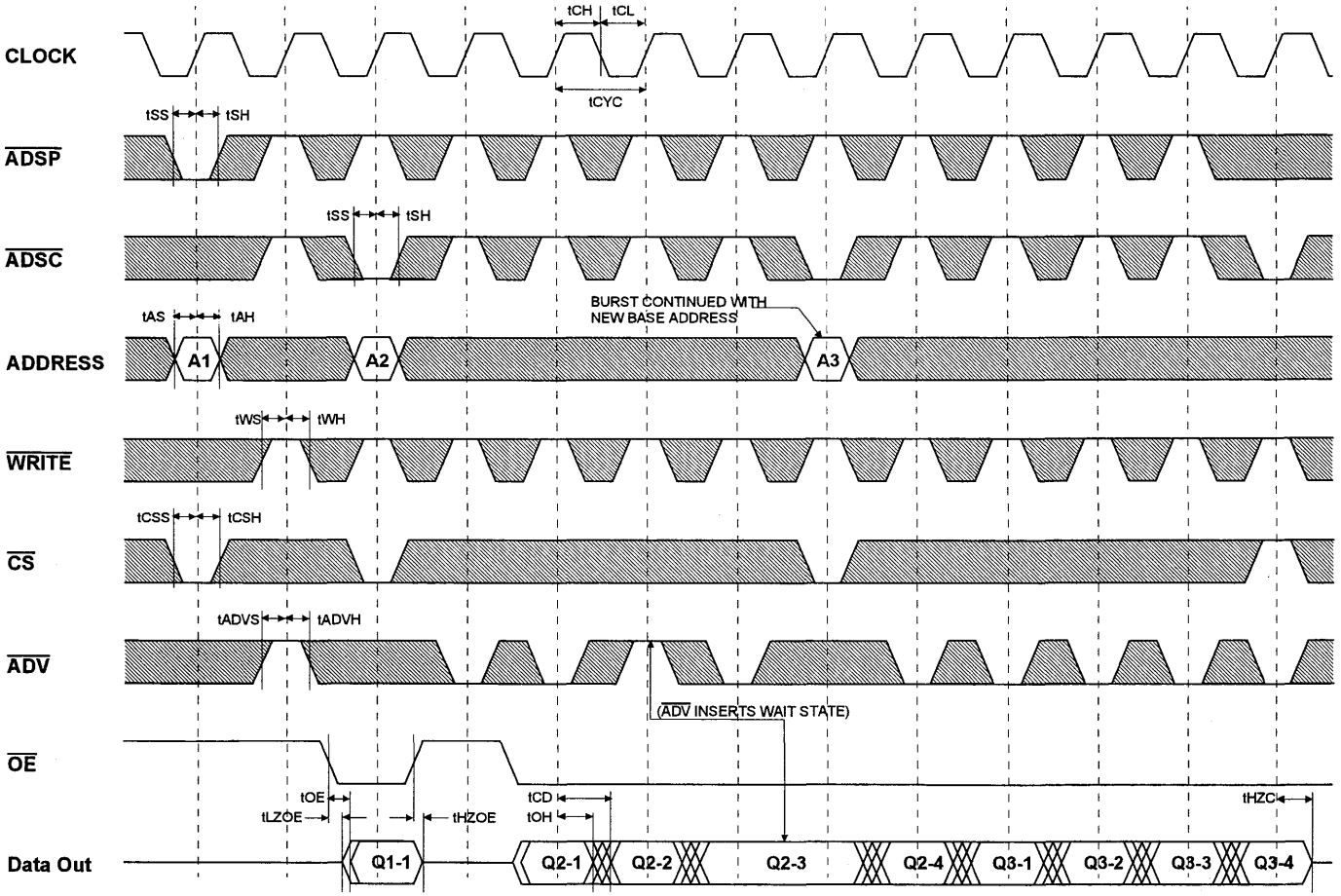
Parameter	Symbol	KM732V589-13		KM732V589-15		KM732V589-17		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	13	-	15	-	17	-	ns
Clock Access Time	tCD	-	7	-	8	-	9	ns
Output Enable to Data Valid	tOE	-	6	-	7	-	8	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	6	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	2	-	2	-	2	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	2	-	ns
Clock High to Output High-Z	tHZC		7		7		7	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	6	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	6	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWS	2.5	-	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

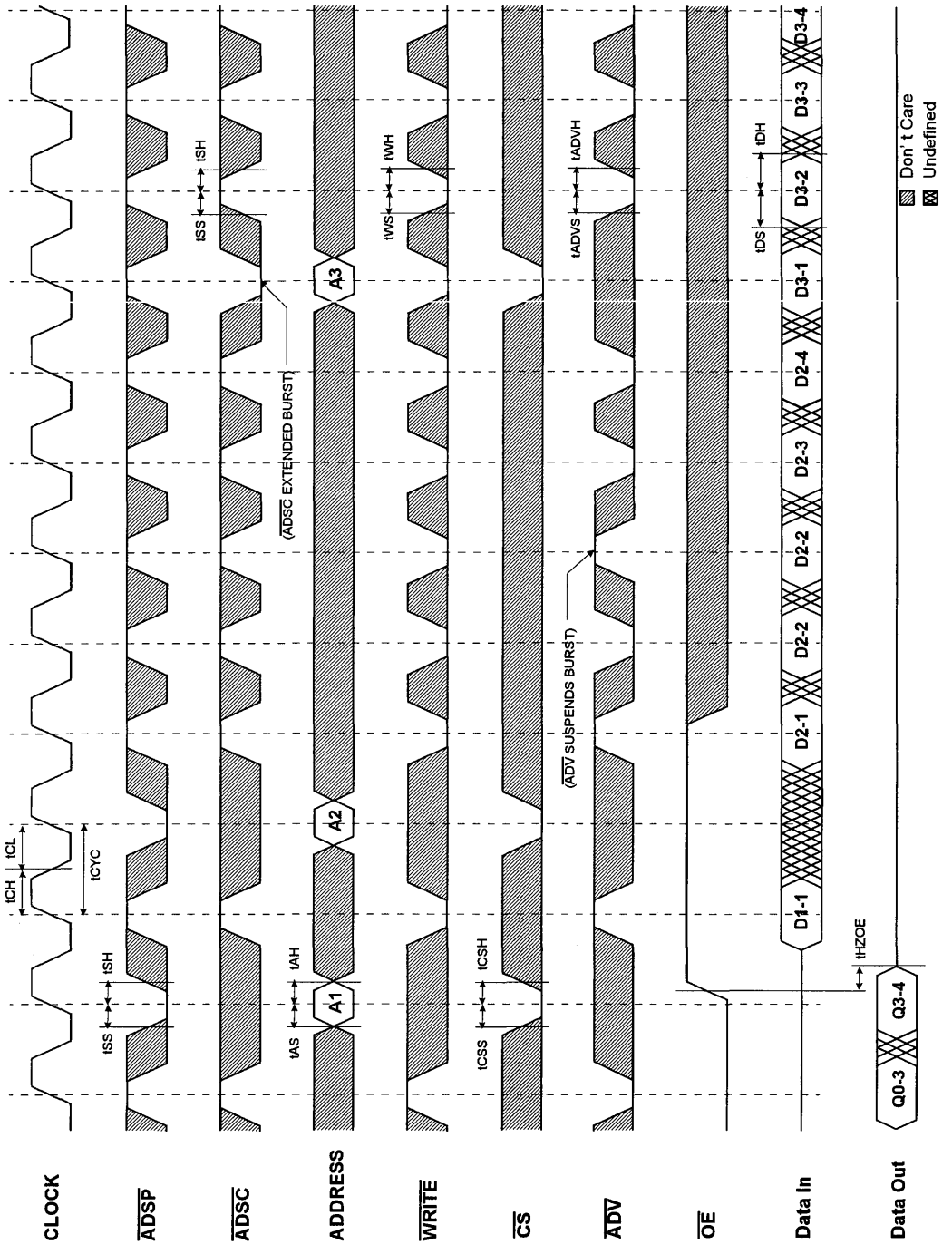
TIMING WAVEFORM OF READ CYCLE



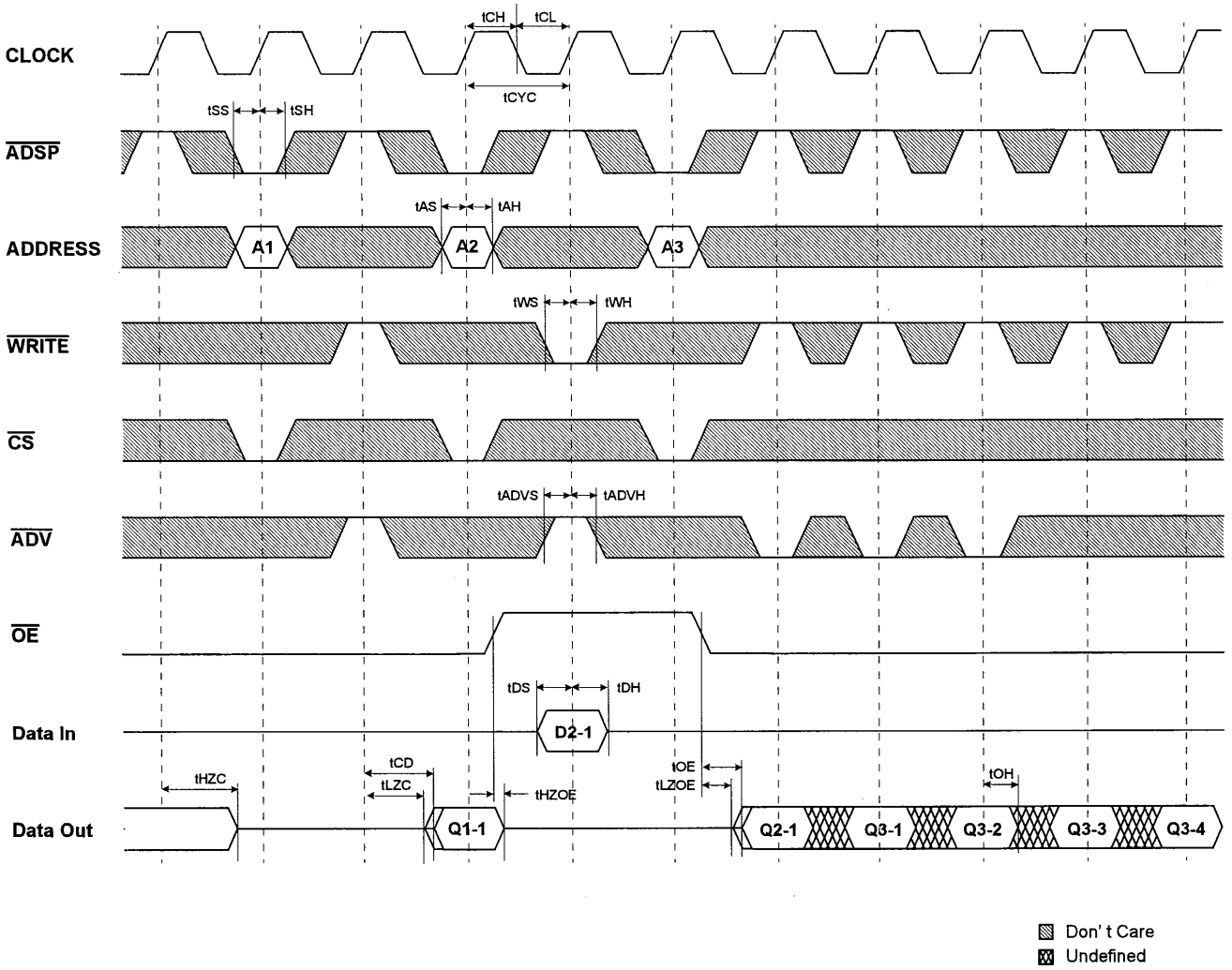
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}x$ = L
$\overline{CS}$ = L means $\overline{CS}1$ = L, CS2 = H and $\overline{CS}2$ = L
$\overline{CS}$ = H means $\overline{CS}1$ = H, or $\overline{CS}1$ = L and $\overline{CS}2$ = H, or $\overline{CS}1$ = L, and CS2 = L

Don' t Care
Undefined

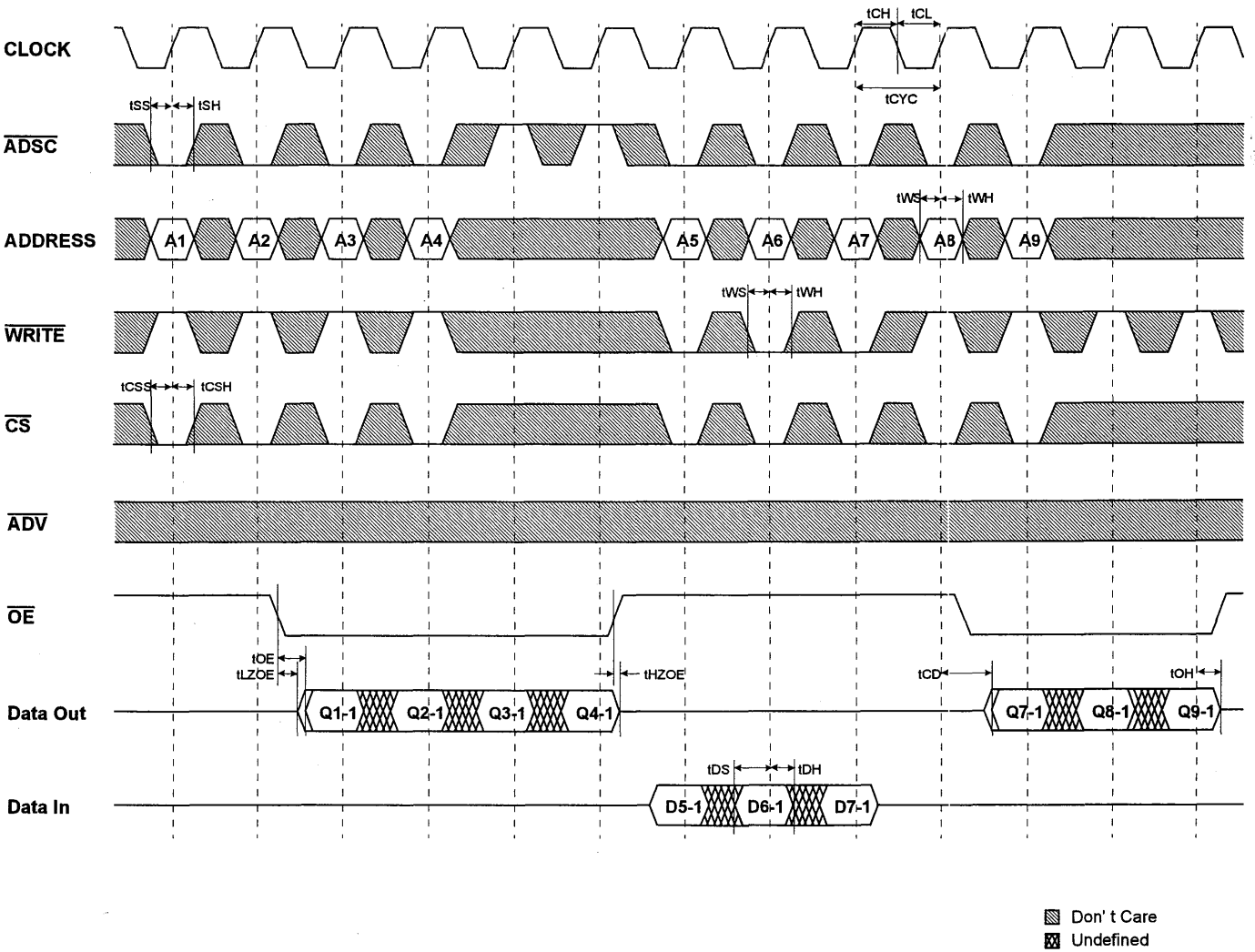
TIMING WAVEFORM OF WRTE CYCLE



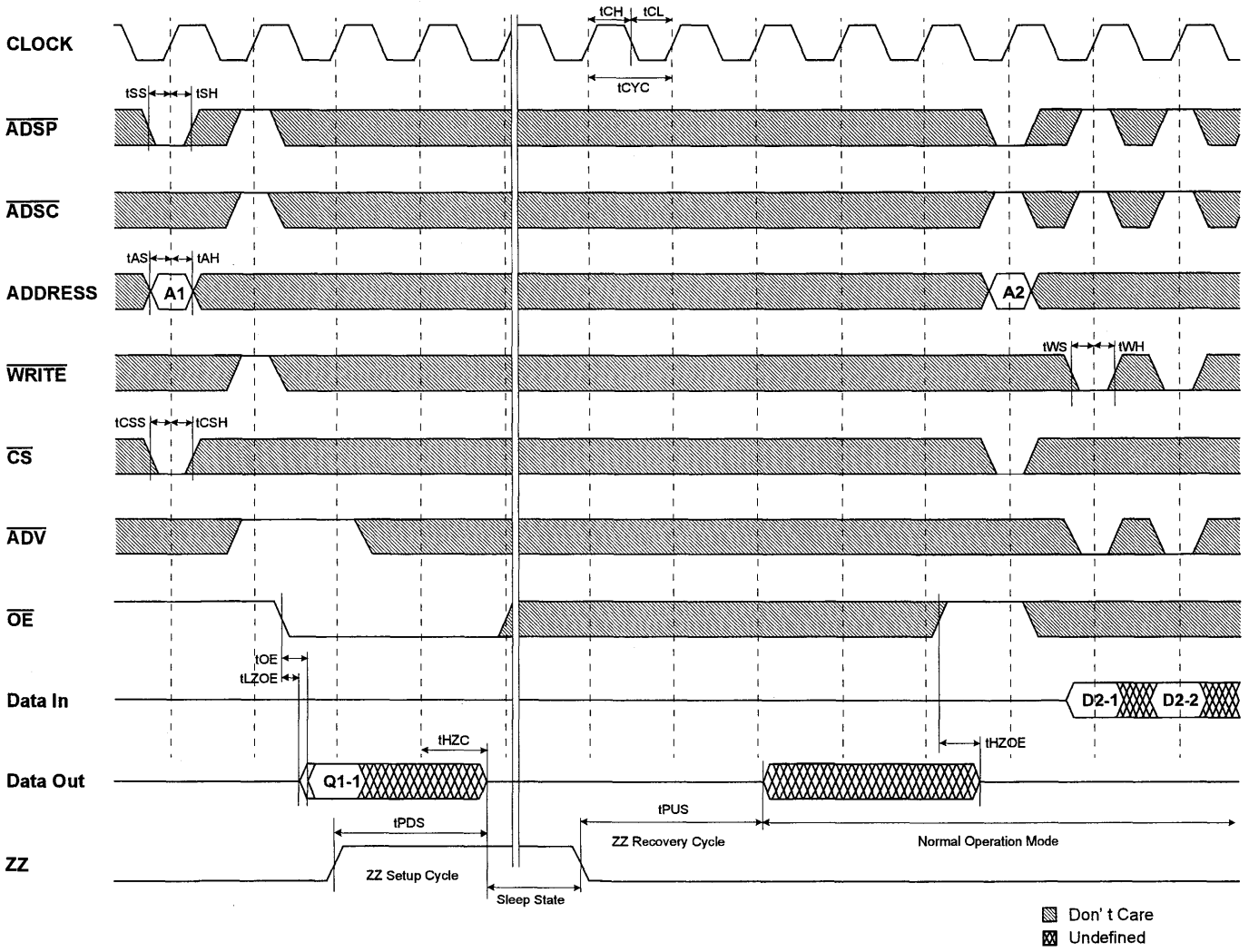
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



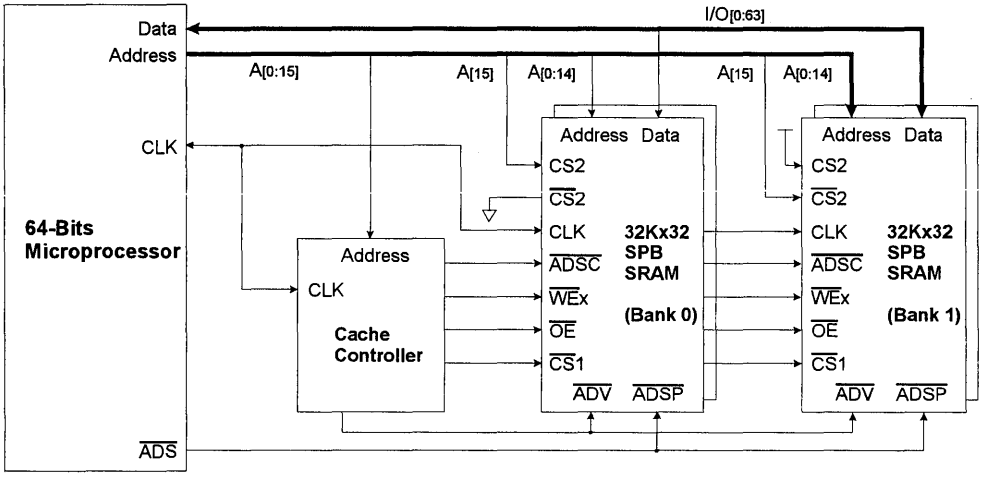
TIMING WAVEFORM OF POWER DOWN CYCLE



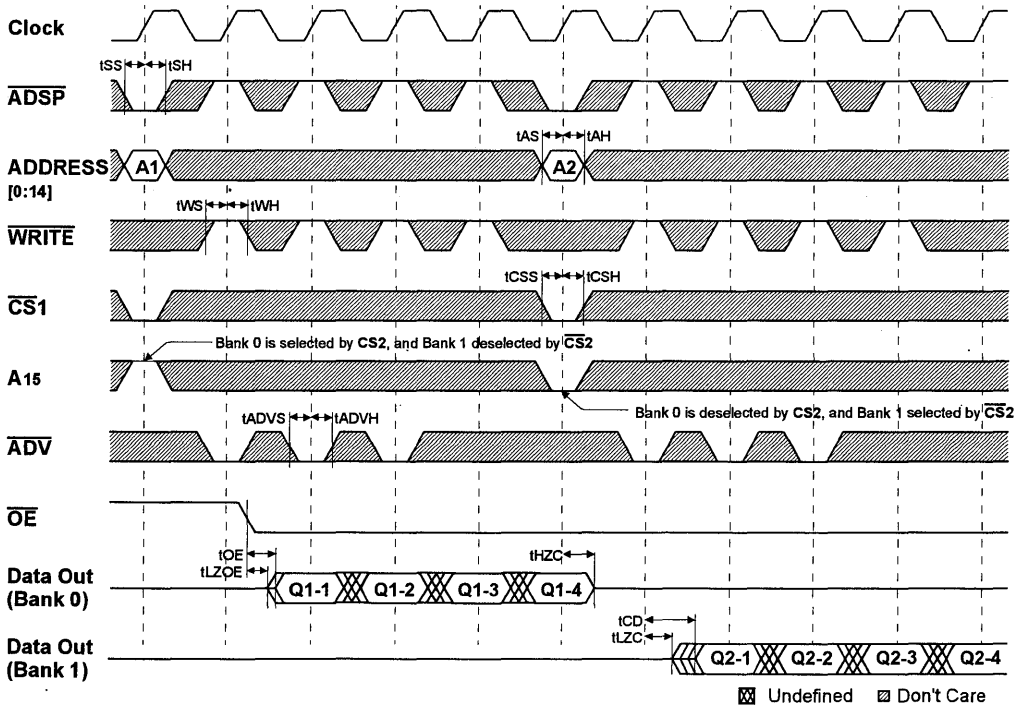
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)



32Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- VDD = 3.3V-5%/+10% Power Supply
- 5V Tolerant Inputs except I/O Pins
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-Pin QFP/TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	Unit
Cycle Time	tCYC	13	15	ns
Clock Access Time	tCD	7.0	8.0	ns
Output Enable Access Time	tOE	6.0	7.0	ns

GENERAL DESCRIPTION

The KM732V589A/L is a 1,048,576-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 32K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS1}$ high, $\overline{ADSP}$ disable to support address pipelining.

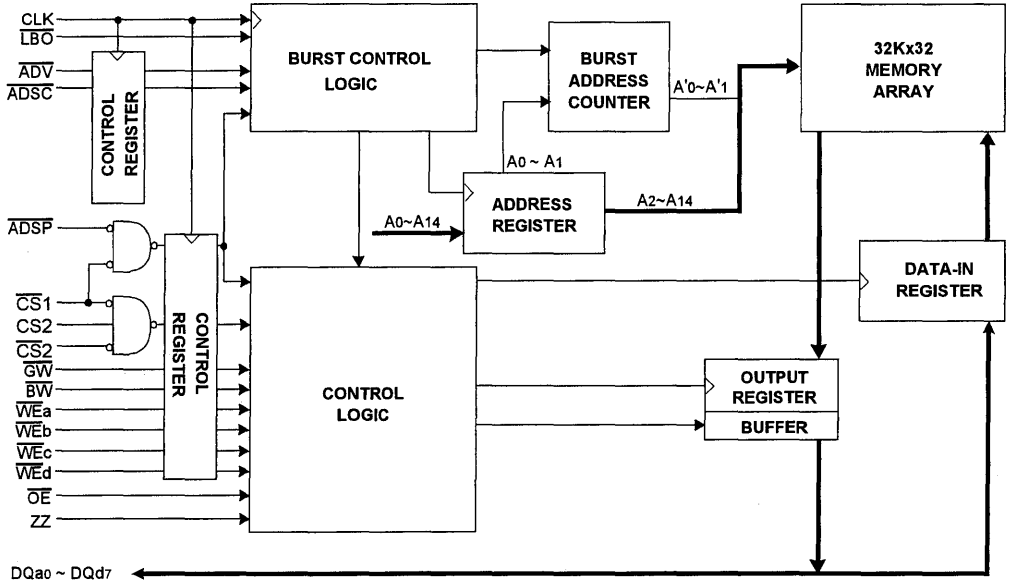
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

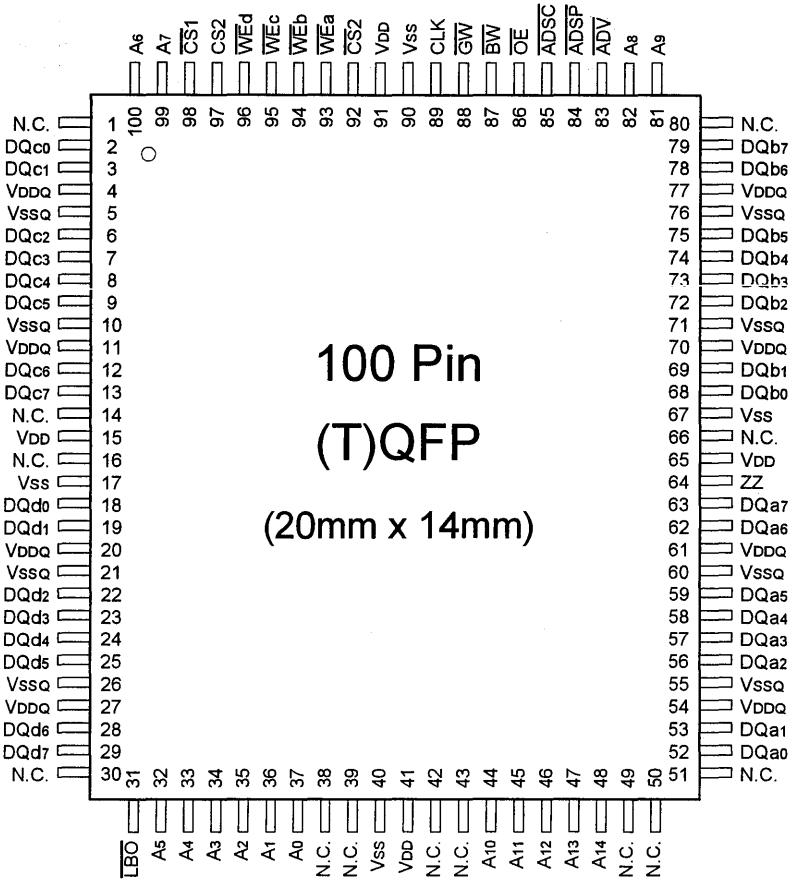
The KM732V589A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin QFP/TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,81, 82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			Vss	Ground	17,40,67,90
			N.C.	No Connect	1,14,16,30,38,39,42,43, 49,50,51,66,80
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97			
$\overline{CS2}$	Chip Select	92	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
$\overline{WEx}$	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86	Vssq	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM732V589A/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$. The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$(regardless of $\overline{BW}$ and $\overline{WE}$x.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x when $\overline{GW}$ is high.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled Low(regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled Low. The address increases internally to the next address of burst, if both $\overline{WE}$x and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. The $\overline{WE}$a controls DQ_{a0} ~ DQ_{a7}, $\overline{WE}$b controls DQ_{b0} ~ DQ_{b7}, $\overline{WE}$c controls DQ_{c0} ~ DQ_{c7}, and $\overline{WE}$d controls DQ_{d0} ~ DQ_{d7}. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
$\overline{WE}$x are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WRITE}$	Operation	$\overline{CS1}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.
2. $\overline{WE}$x means $\overline{WE}$a ~ $\overline{WE}$d.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
	V_{DDQ}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

CAPACITANCE*(T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(V_{DD}=3.3V-5%+10%, T_A = 0℃ to 70℃)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Vss to V_{DD} ; V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	-13	-	200	mA
			-15	-	180	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V		-	40	mA
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	5	mA
			L-Ver.	-	1	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	5	mA
			L-Ver.	-	500	μA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.2	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)

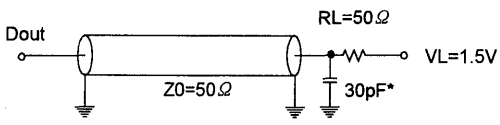
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

TEST CONDITIONS

(T_A = 0℃ to 70℃, V_{DD}=3.3V-5%/+10% unless otherwise specified)

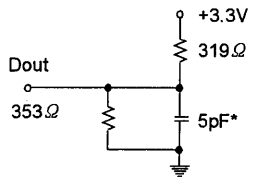
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)



* Capacitive Load consists of all components of the test environment.

Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

SAMSUNG ELECTRONICS

AC TIMING CHARACTERISTICS

(V_{DD}=3.3V-5%/+10%, T_A = 0℃ to 70℃)

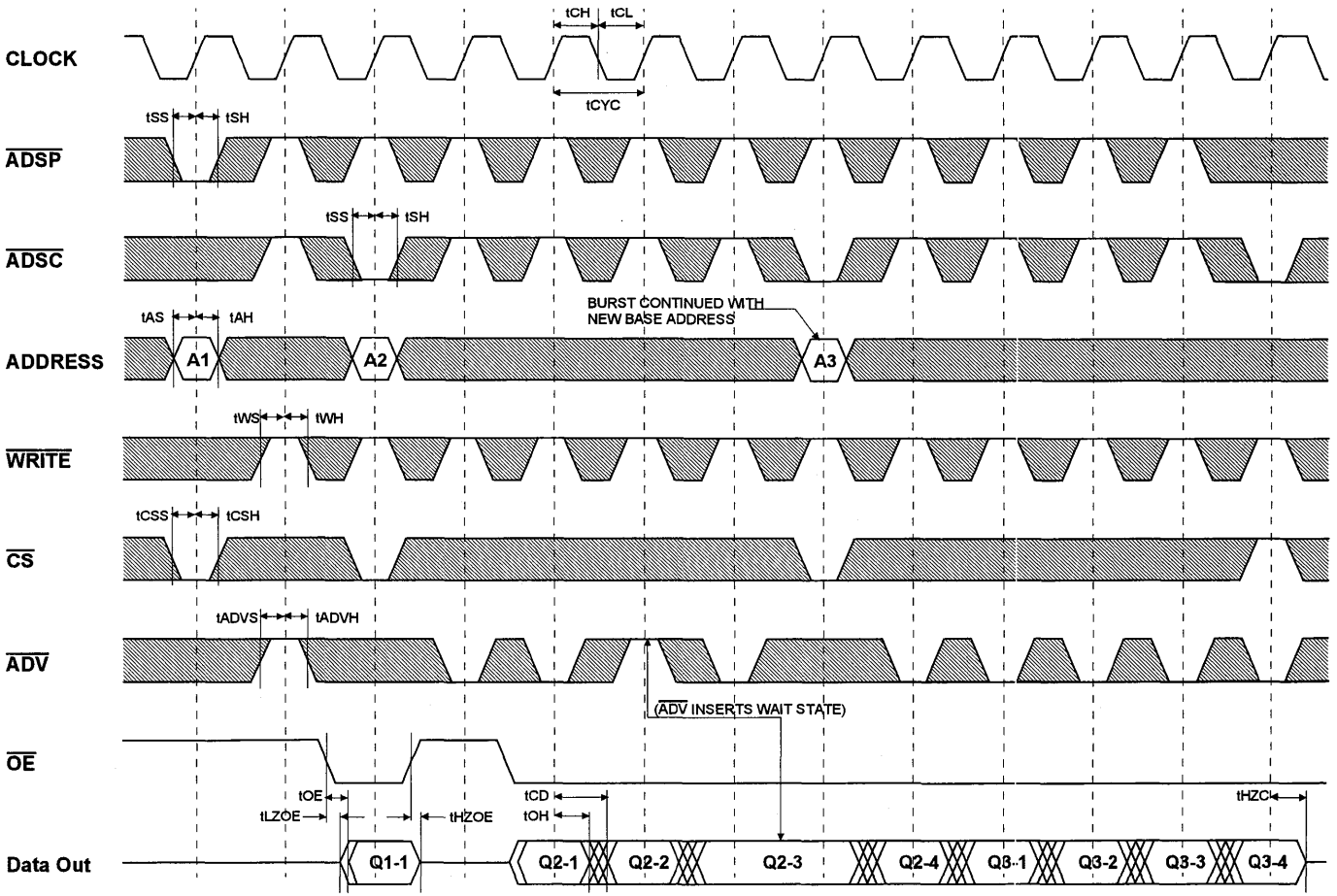
Parameter	Symbol	KM732V589A-13		KM732V589A-15		Unit
		Min	Max	Min	Max	
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7.0	-	8.0	ns
Output Enable to Data Valid	tOE	-	6.0	-	7.0	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	2.0	6.0	ns
Clock High Pulse Width	tCH	4.5	-	6.0	-	ns
Clock Low Pulse Width	tCL	4.5	-	6.0	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

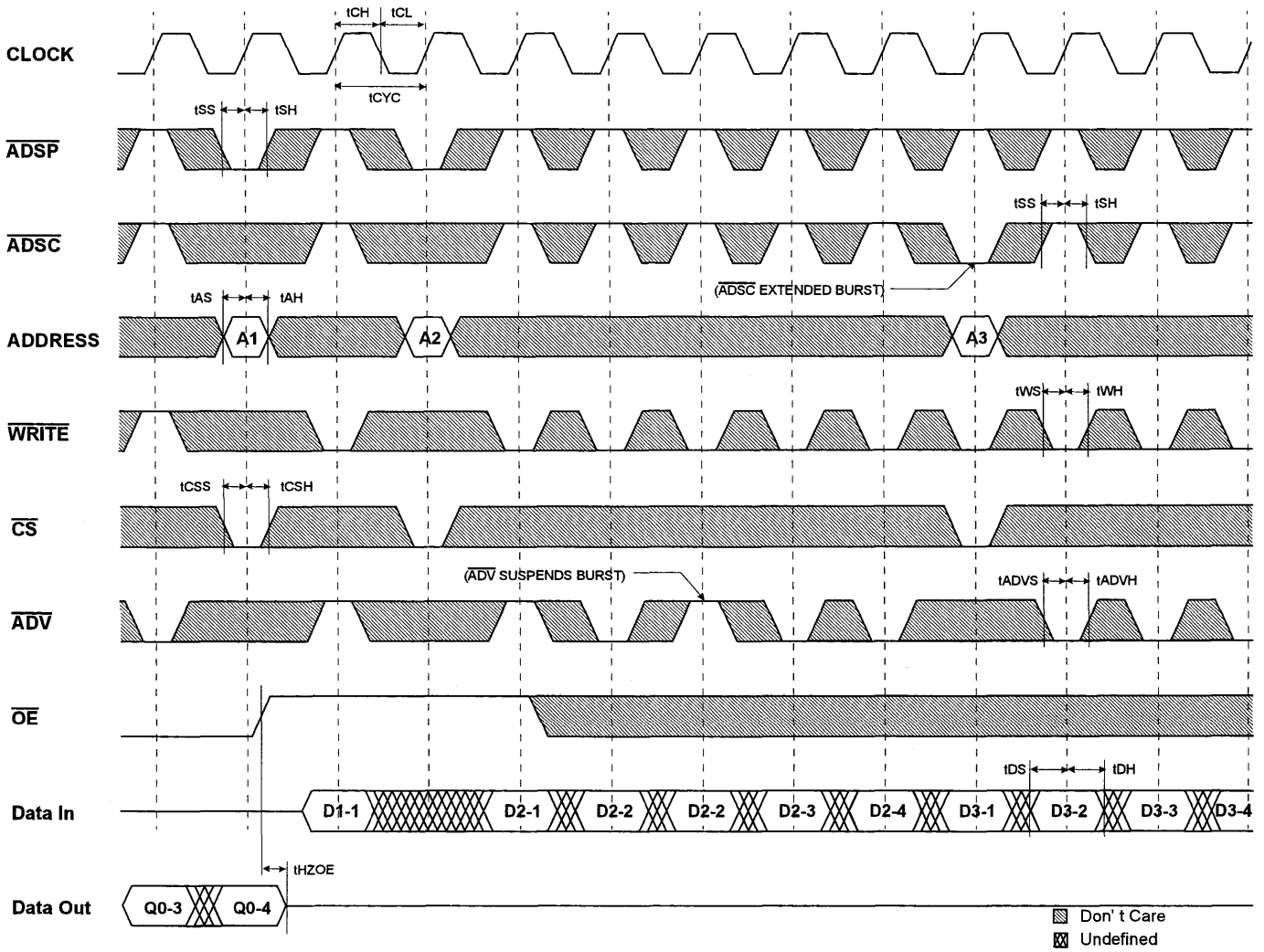
TIMING WAVEFORM OF READ CYCLE



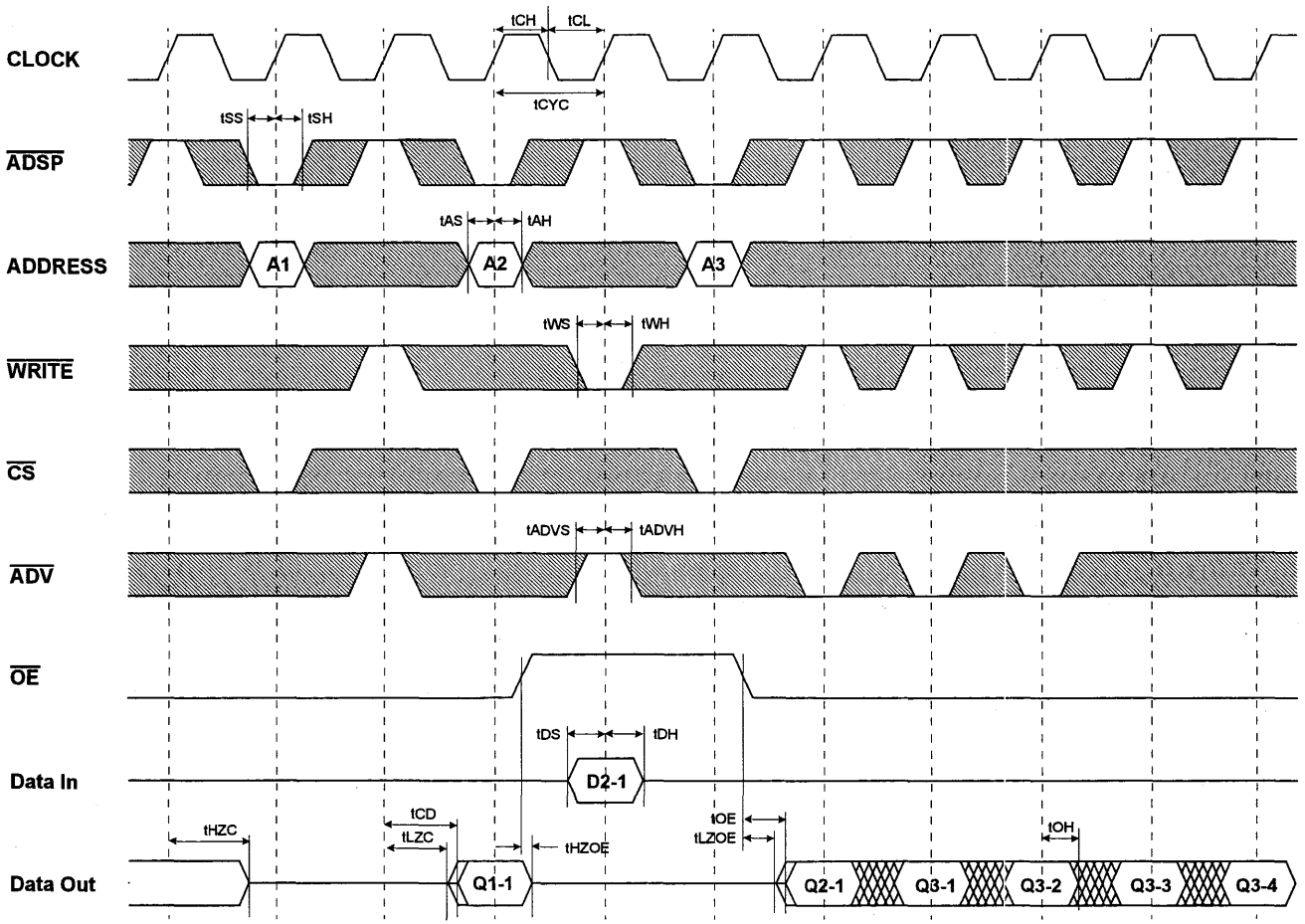
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}x$ = L
$\overline{CS}$ = L means $\overline{CS}1$ = L, CS2 = H and $\overline{CS}2$ = L
$\overline{CS}$ = H means $\overline{CS}1$ = H, or $\overline{CS}1$ = L and $\overline{CS}2$ = H, or $\overline{CS}1$ = L, and CS2 = L

▨ Don' t Care
▩ Undefined

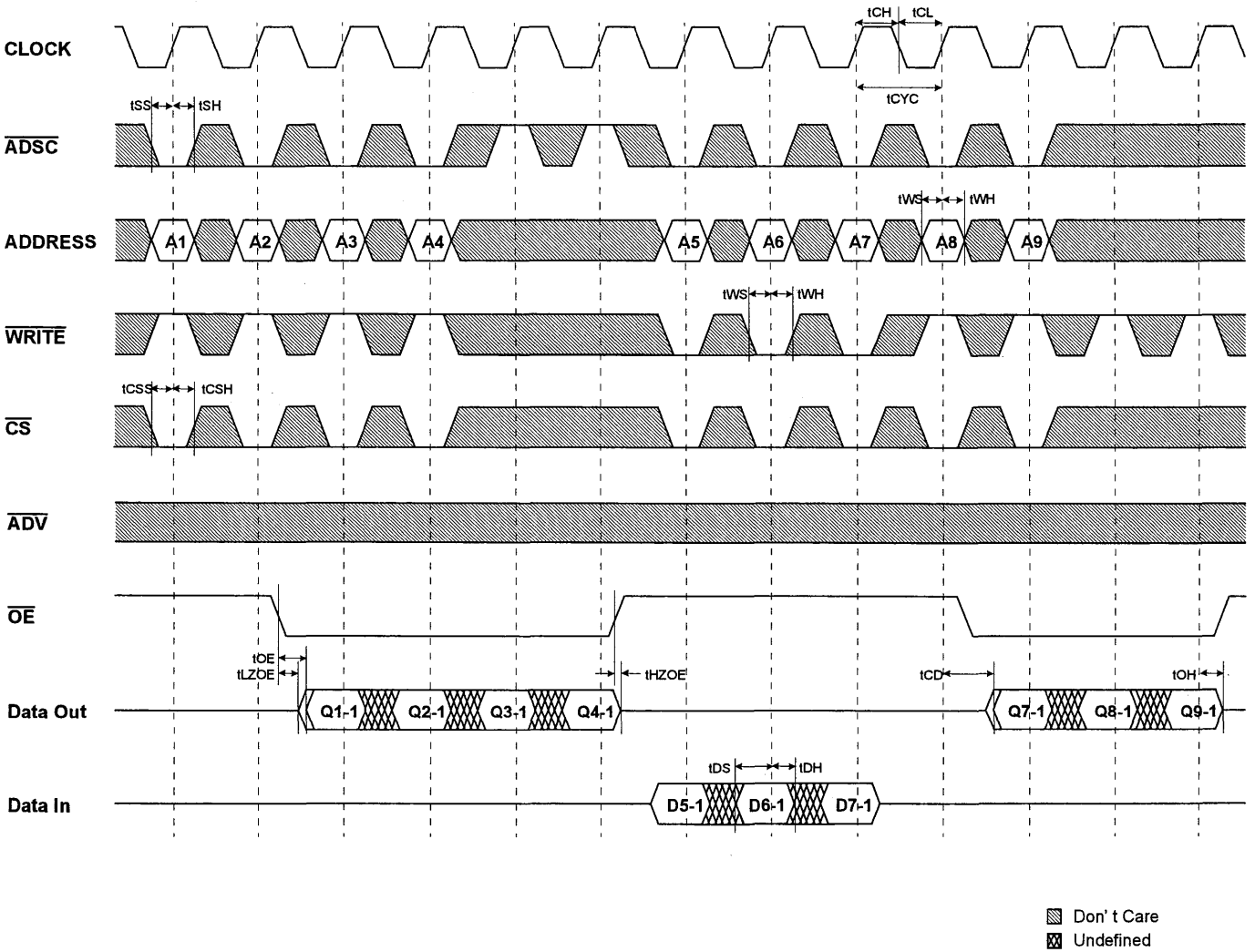
TIMING WAVEFORM OF WRTE CYCLE



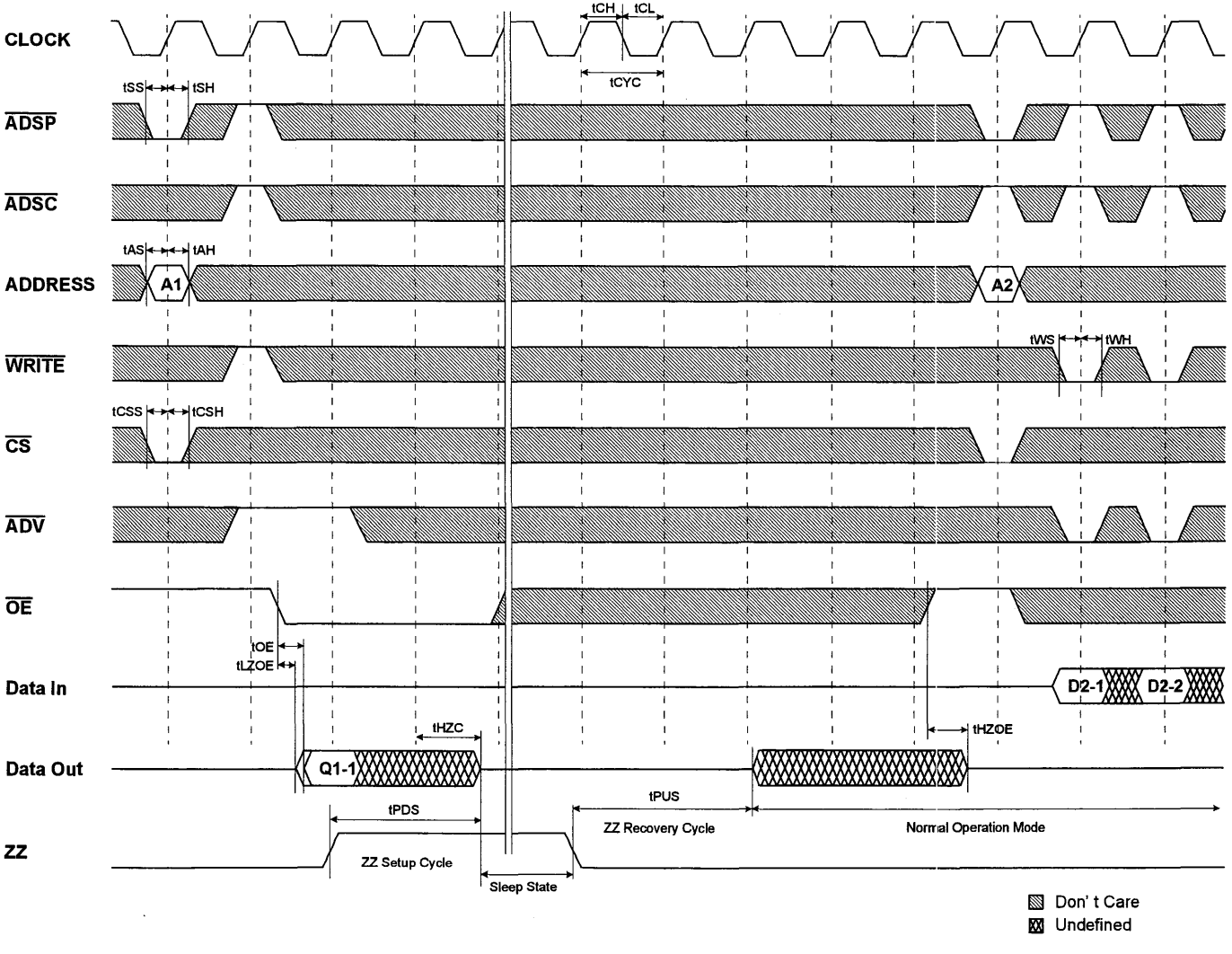
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



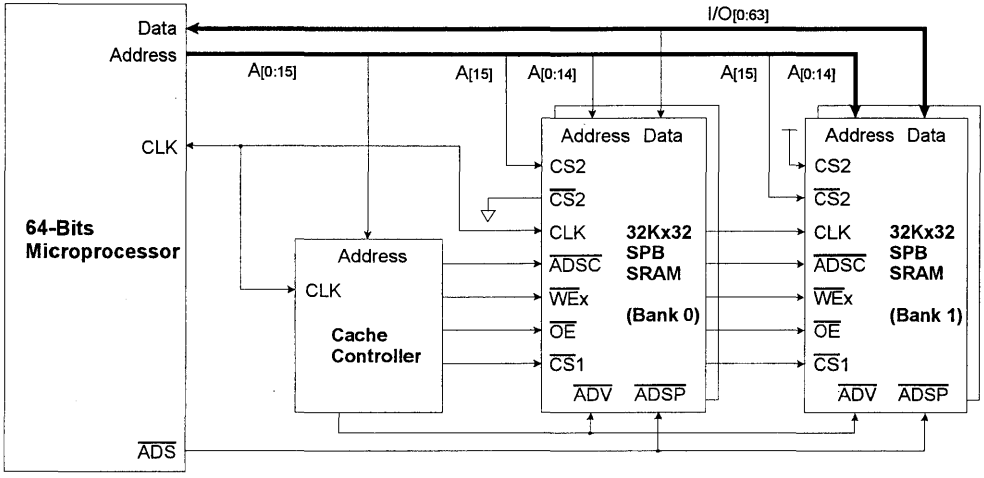
TIMING WAVEFORM OF POWER DOWN CYCLE



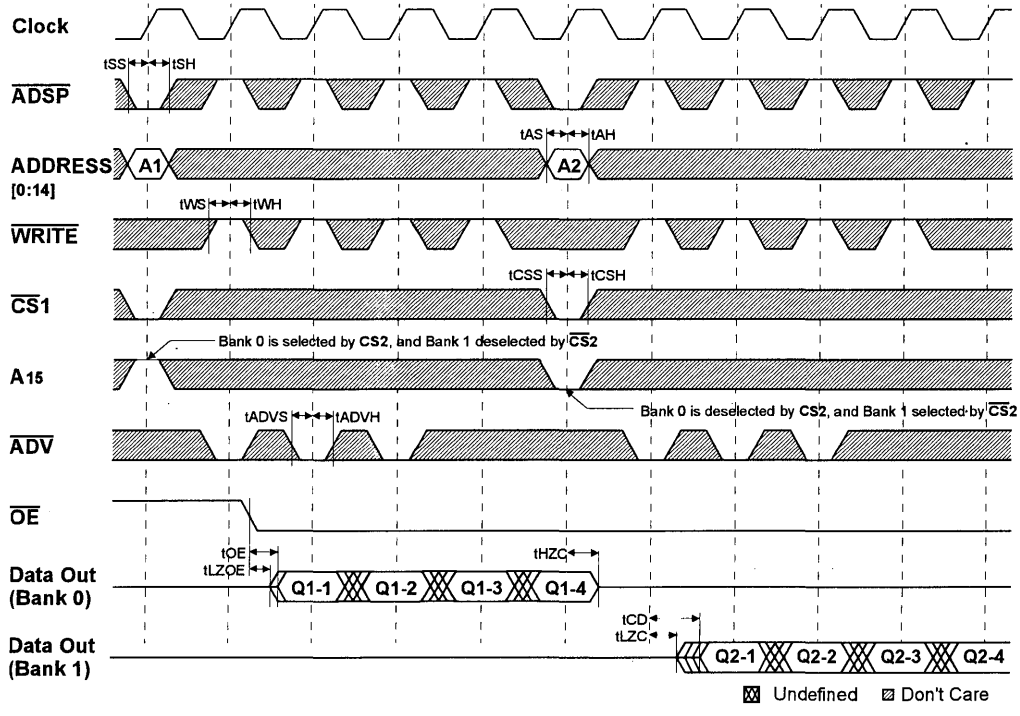
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)



32Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- On-Chip Address and Control Registers.
- V_{DD}=3.3V-5%/+10% Power Supply for 3.3V I/O.
- V_{DD}=3.3V±5% Power Supply for 2.5V I/O.
- I/O Supply Voltage : 3.3V-5%/+10% for 3.3V I/O
  or 2.5V+0.4V/-0.13V for 2.5V I/O
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	Unit
Cycle Time	tCYC	13	15	ns
Clock Access Time	tCD	7	8	ns
Output Enable Access Time	tOE	6	7	ns

GENERAL DESCRIPTION

The KM732V596A/L is a 1,048,576 bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based Mobile System.

It is organized as 32K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WEx}$ and $\overline{BW}$ when $\overline{GW}$ is high.

And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signals.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs.

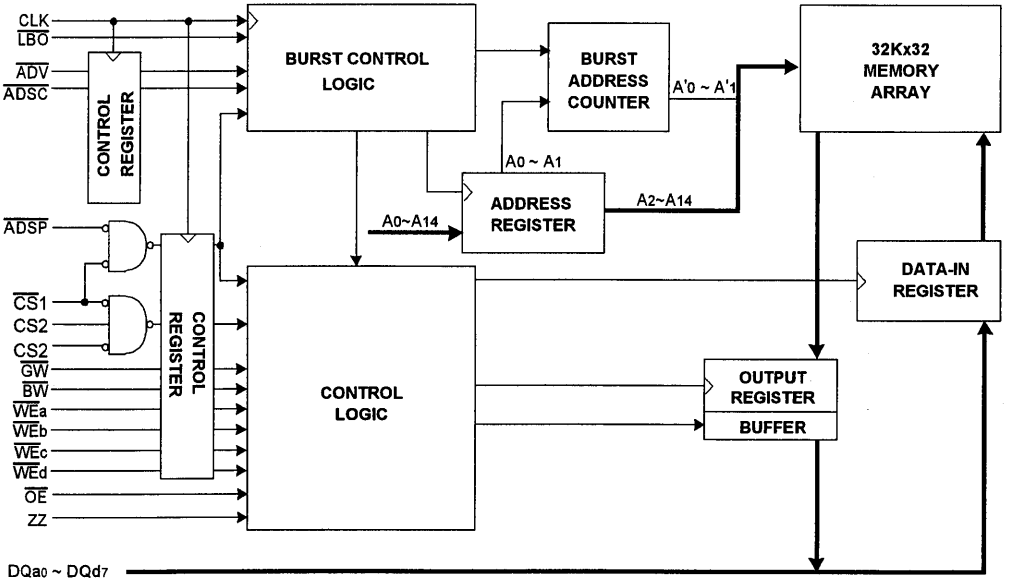
Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

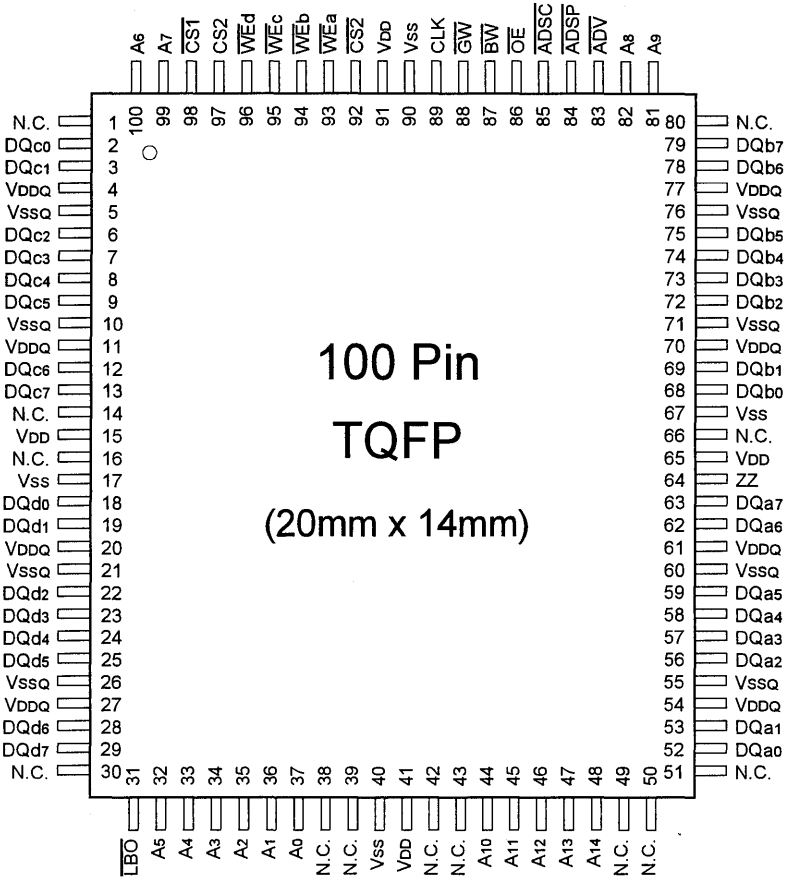
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The KM732V596A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,81, 82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			Vss	Ground	17,40,67,90
			N.C.	No Connect	1,14,16,30,38,39,42,43, 49,50,51,66,80
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97			
$\overline{CS2}$	Chip Select	92	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
$\overline{WEx}$	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
$\overline{ZZ}$	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

SAMSUNG ELECTRONICS

FUNCTION DESCRIPTION

The KM732V596A/L is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs(with the exception of $\overline{OE}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, $\overline{ADSP}$, $\overline{ADSC}$ and $\overline{ADV}$. The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to Low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WEx}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output [ins. ADV is ignored on the clock edge that samples ADSP asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WEx}$ are sampled high and $\overline{ADV}$ is sampled Low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$(regardless of $\overline{BW}$ and $\overline{WEx}$.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WEx}$ when $\overline{GW}$ is High. Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WEx}$. $\overline{WEx}$ are ignored on the clock edge that samples $\overline{ADSP}$ Low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WEx}$ are sampled Low(regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WEx}$ sampled Low. The address increases internally to the next address of burst, if both $\overline{WEx}$ and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. THE $\overline{WE}$a control $DQa_0 \sim DQa_7$, $\overline{WE}$b controls $DQb_0 \sim DQb_7$, $\overline{WE}$c control $DQc_0 \sim DQc_7$, and $\overline{WE}$d control $DQd_0 \sim DQd_7$. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
$\overline{WEx}$ are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑ .
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally.
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WRITE}$	Operation	$\overline{CS}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O(0℃ ≤ T_A ≤ 70℃)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
	V_{DDQ}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O(0℃ ≤ T_A ≤ 70℃)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.47	V
	V_{DDQ}	2.37	2.5	2.9	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(V_{DD}=3.3V-5%/+10%, V_{DDQ}=3.3V-5%/+10%, or V_{DD}=3.3V±5%, V_{DDQ}=2.5V+0.4V/-0.13V, T_A = 0℃ to 70℃)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Vss to V_{DD}, V_{IN} = Vss to V_{DD}		-2	2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA,	-13	-	200	mA
		ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH}	-15	-	180	
		Cycle Time ≥ tCYC min				
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V		-	40	mA
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs = fixed(V_{DD}-0.2V or 0.2V)		-	5	mA
			L-Ver.	-	1.0	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	5	mA
			L-Ver.	-	500	μA
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL} = 1.0mA		-	0.2	V
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH} = -1.0mA		2.0	-	V
Input Low Voltage(3.3V I/O)	V_{IL}			-0.5*	0.8	V
Input High Voltage(3.3V I/O)	V_{IH}			2.0	5.5**	V
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V
Input High Voltage(2.5V I/O)	V_{IH}			1.7	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)

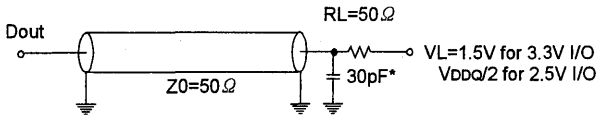
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

TEST CONDITIONS

(T_A = 0℃ to 70℃, V_{DD}=3.3V-5%/+10%, V_{DDQ}=3.3V-5%/+10%, or V_{DD}=3.3V±5%, V_{DDQ}=2.5V +0.4V/-0.13V)

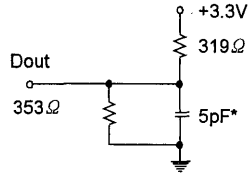
Parameter	Value
Input Pulse Level (for 3.3V I/O)	0 to 3V
Input Pulse Level (for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	2ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	2ns
Input and Output Timing Reference Levels(for 3.3V I/O)	1.5V
Input and Output Timing Reference Levels(for 2.5V I/O)	V_{DDQ}/2
Output Load	See Fig. 1

Output Load(A)



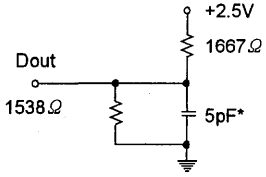
* Capacitive Load consists of all components of the test environment.

Output Load(B),(3.3V I/O)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Output Load(C),(2.5V I/O)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

(V_{DD}=3.3V-5%/+10%, V_{DDQ}=3.3V-5%/+10%, or V_{DD}=3.3V±5%, V_{DDQ}=2.5V+0.4V/-0.13V, T_A = 0℃ to 70℃)

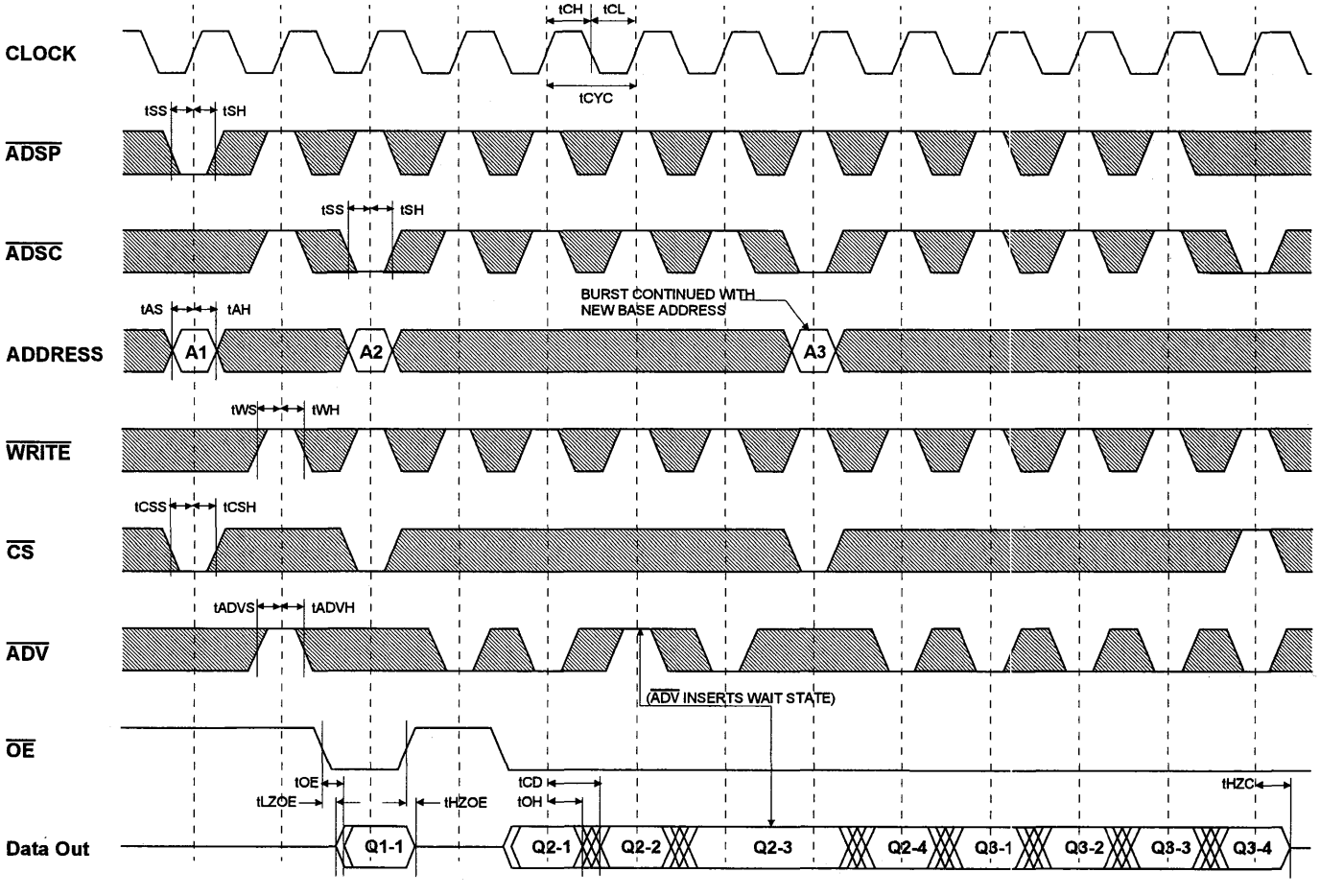
Parameter	Symbol	KM732V596A-13		KM732V596A-15		Unit
		Min	Max	Min	Max	
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7.0	-	8.0	ns
Output Enable to Data Valid	tOE	-	6.0	-	7.0	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	2.0	6.0	ns
Clock High Pulse Width	tCH	4.5	-	6.0	-	ns
Clock Low Pulse Width	tCL	4.5	-	6.0	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

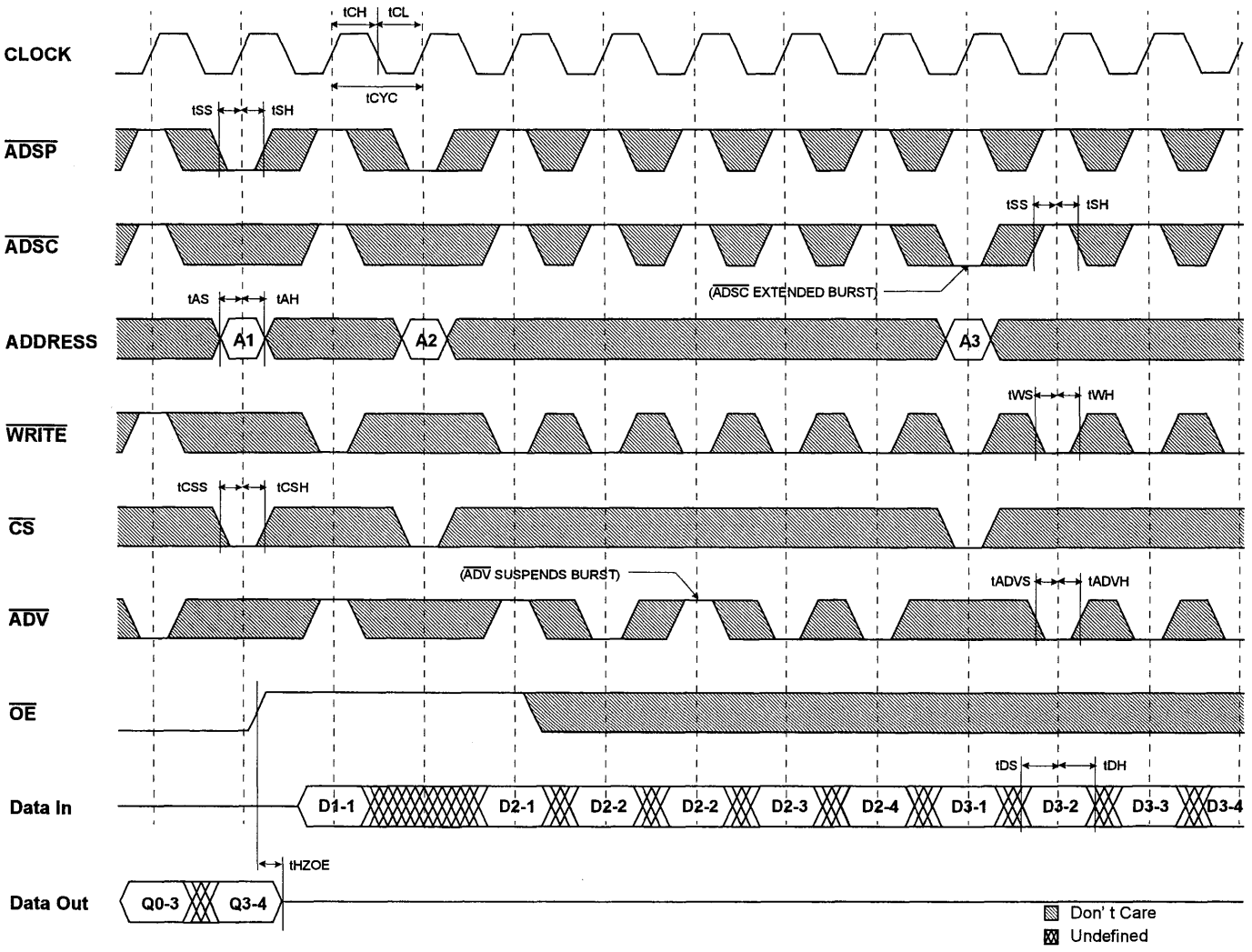
TIMING WAVEFORM OF READ CYCLE



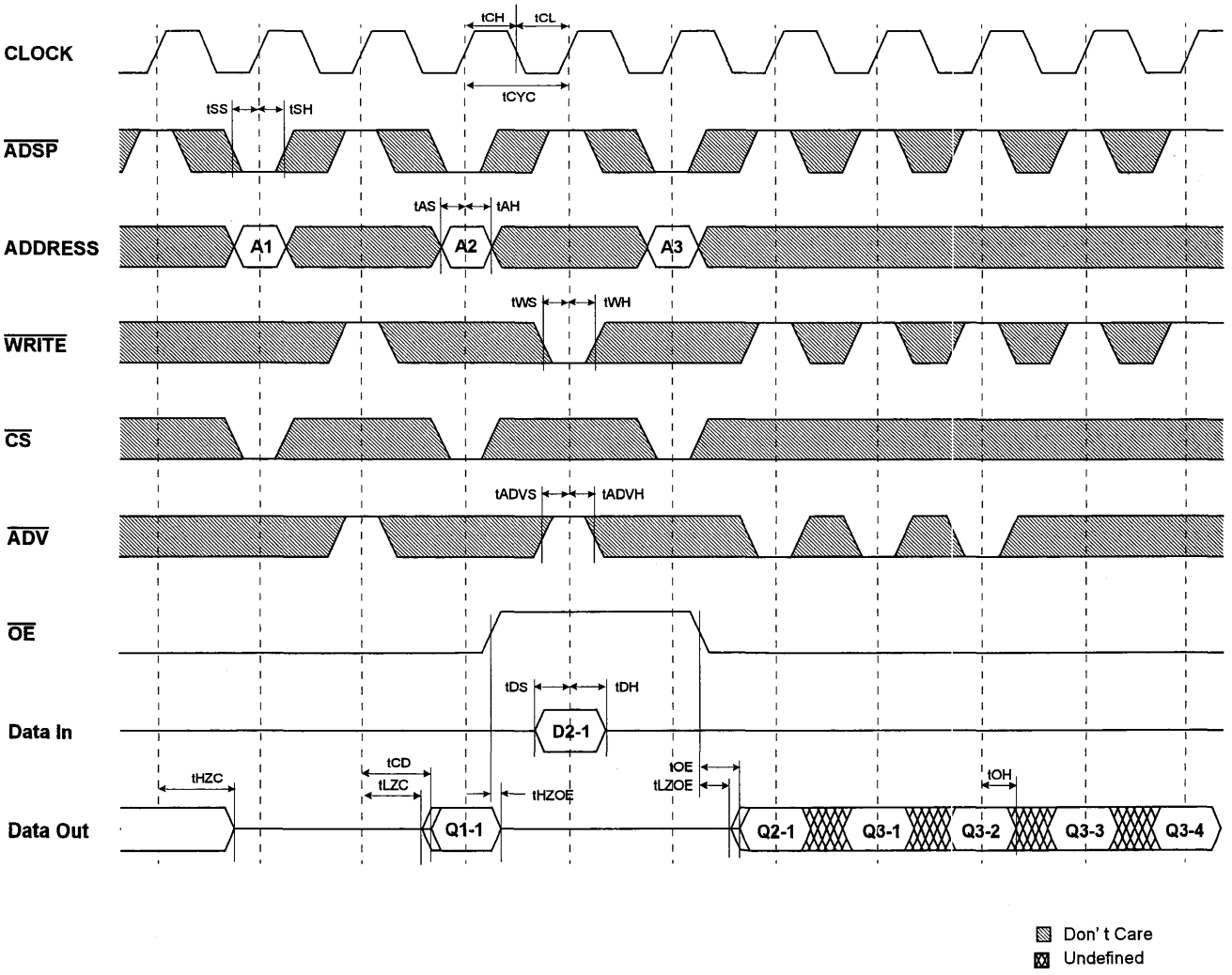
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}x$ = L
$\overline{CS}$ = L means $\overline{CS1}$ = L, CS2 = H and $\overline{CS2}$ = L
$\overline{CS}$ = H means $\overline{CS1}$ = H, or $\overline{CS1}$ = L and $\overline{CS2}$ = H, or $\overline{CS1}$ = L, and CS2 = L

Don' t Care
Undefined

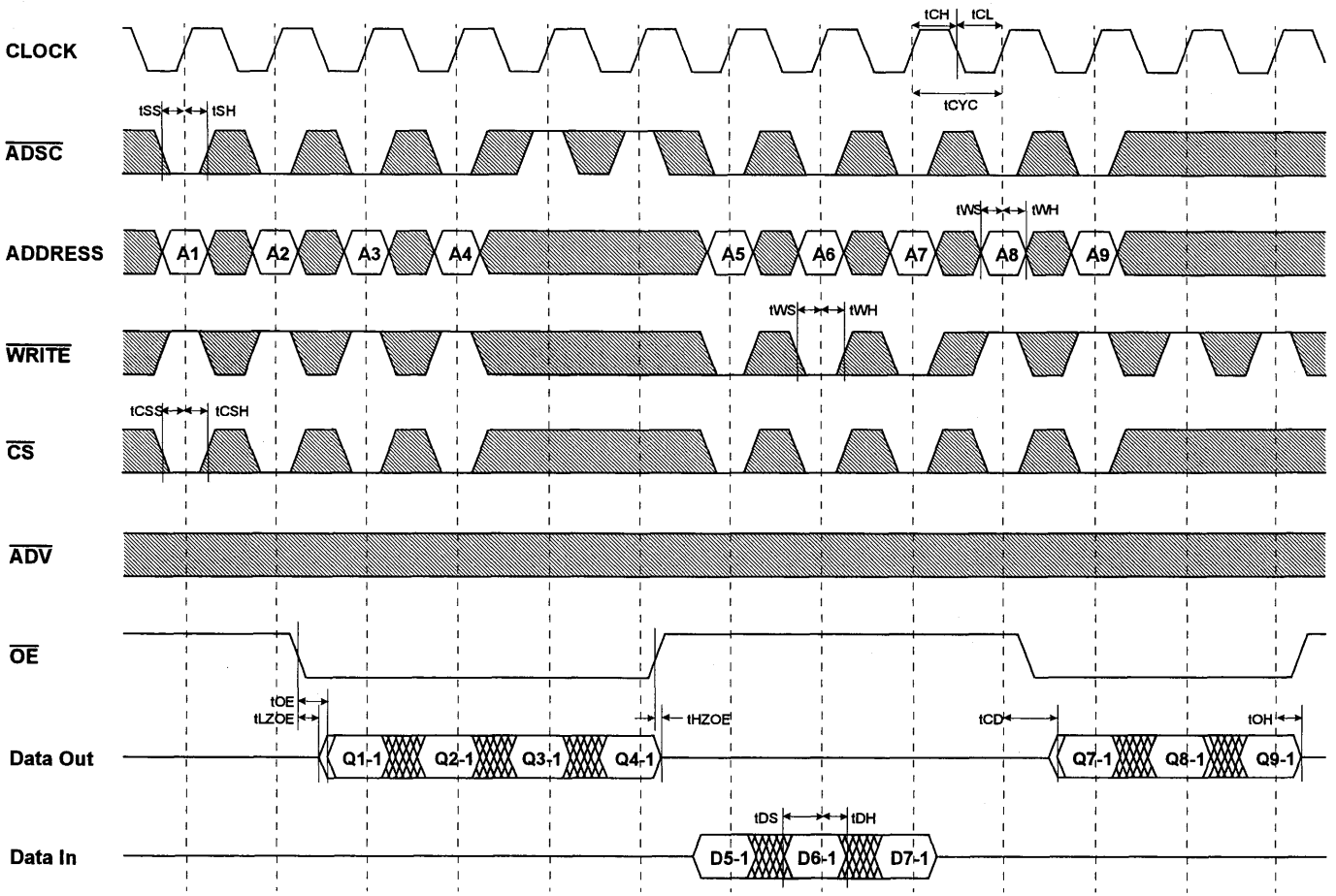
TIMING WAVEFORM OF WRTE CYCLE



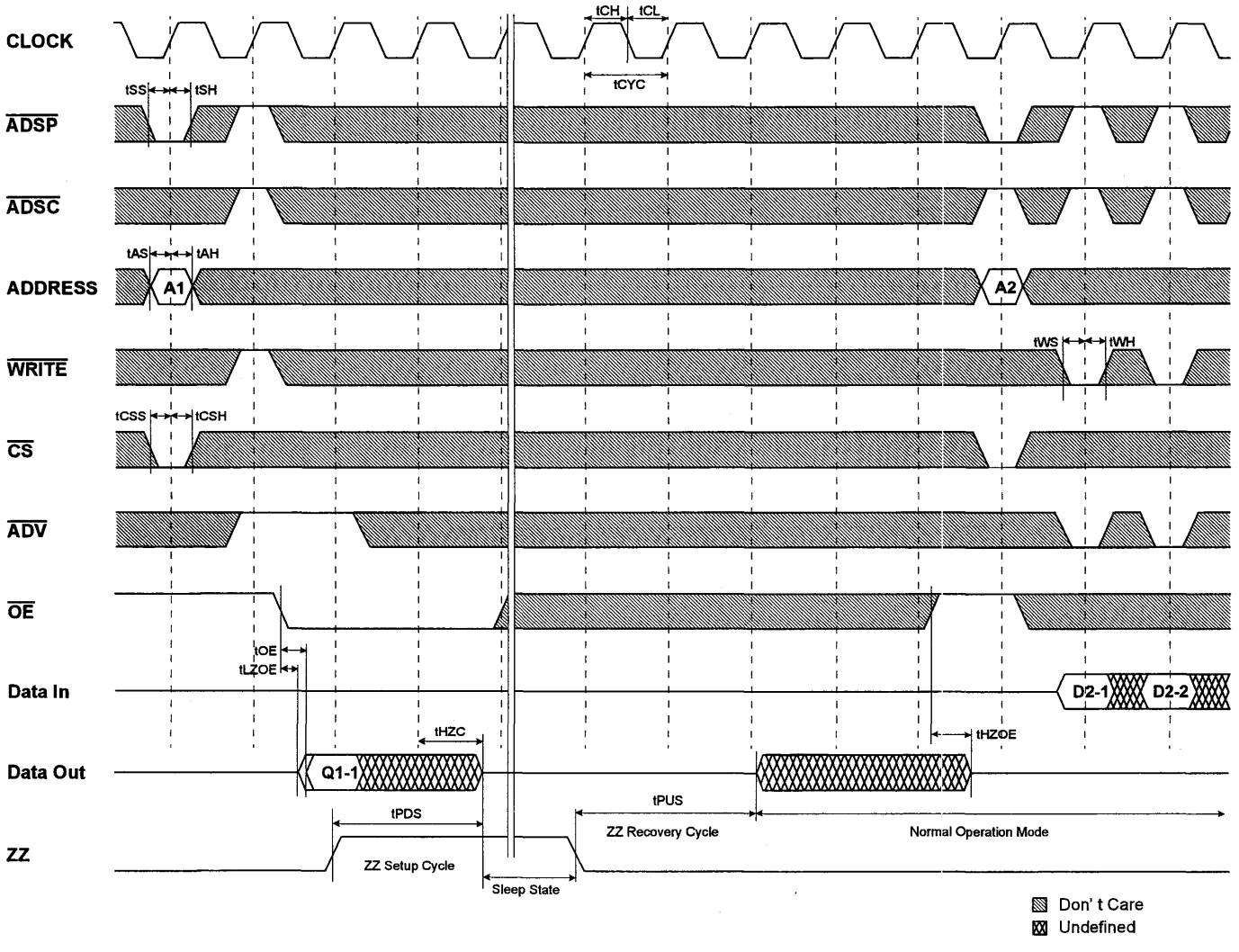
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



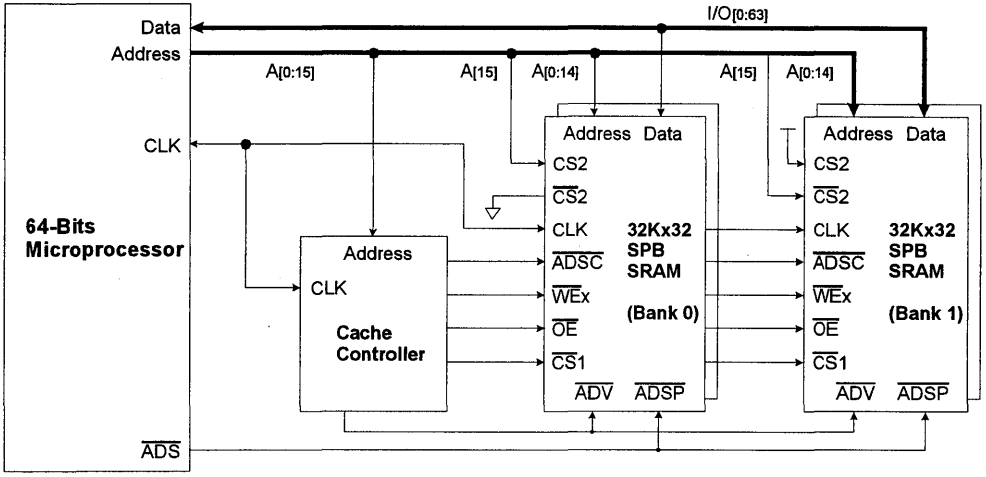
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

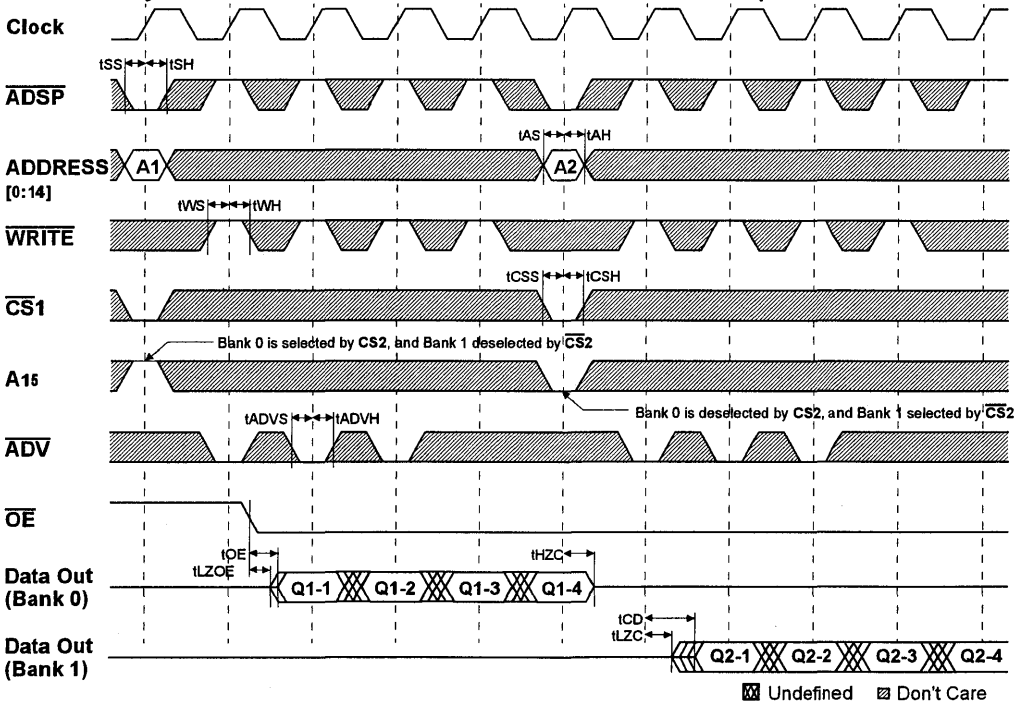
DEPTH EXPANSION

The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.



32Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- Core Supply Voltage : 3.3V±5%
- 5V Tolerant Inputs except I/O Pins
- I/O Supply Voltage : 2.5V+0.4/-0.13V.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-6	-7	-8	-10	Unit
Cycle Time	tCYC	6.6	7.5	8.6	10	ns
Clock Access Time	tCD	4.4	5.0	5.0	5.5	ns
Output Enable Access Time	tOE	4.8	4.8	5.0	5.5	ns

GENERAL DESCRIPTION

The KM732V595A/L is a 1,048,576 bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 32K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signals.

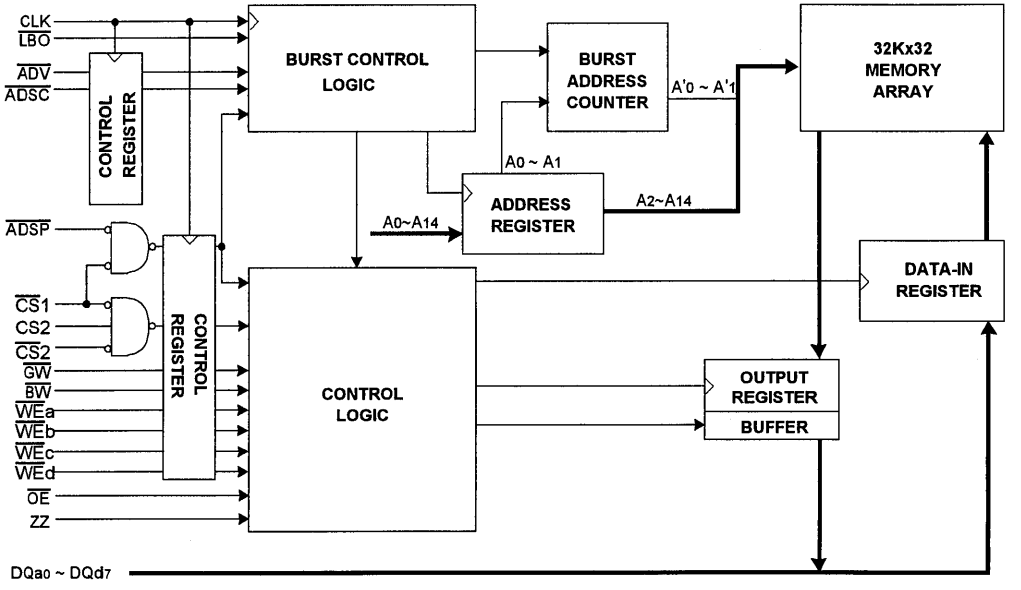
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence (linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

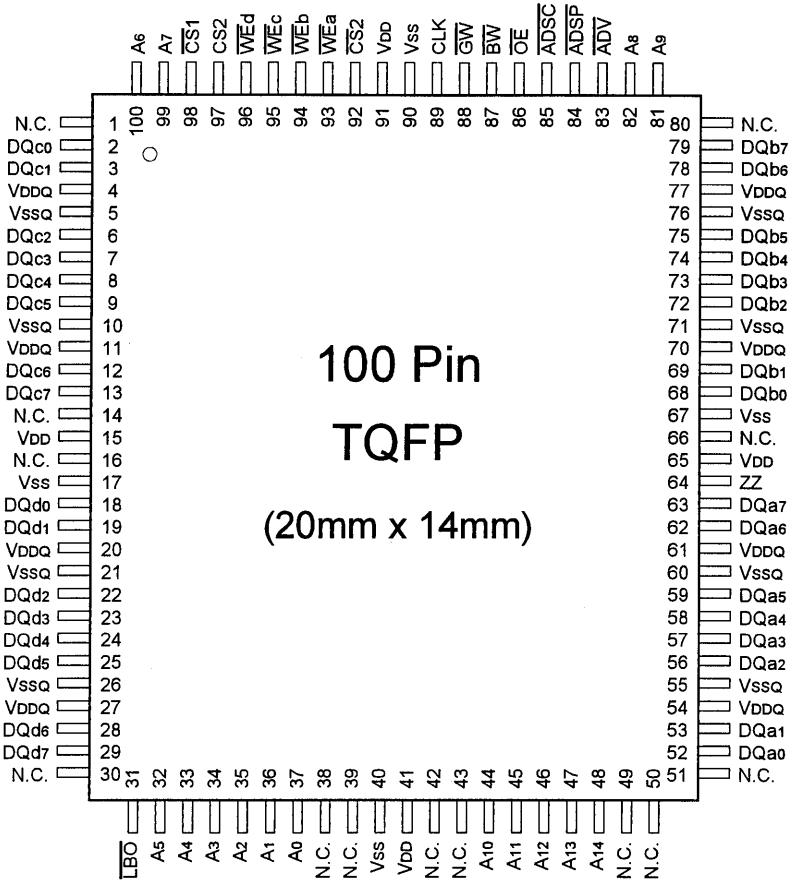
The KM732V595A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,81, 82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,14,16,30,38,39,42,43, 49,50,51,66,80
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	VDDQ	Output Power Supply (+2.5V)	4,11,20,27,54,61,70,77
$\overline{CS2}$	Chip Select	92			
$\overline{WEx}$	Byte Write Inputs	93,94,95,96	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

SAMSUNG ELECTRONICS

FUNCTION DESCRIPTION

The KM732V595A/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$(regardless of $\overline{BW}$ and $\overline{WE}$x.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x when $\overline{GW}$ is high.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled Low(regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled Low. The address increases internally to the next address of burst, if both $\overline{WE}$x and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. The $\overline{WE}$a controls $DQa_0 \sim DQa_7$, $\overline{WE}$b controls $DQb_0 \sim DQb_7$, $\overline{WE}$c controls $DQc_0 \sim DQc_7$, and $\overline{WE}$d controls $DQd_0 \sim DQd_7$. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$x are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WRITE}$	Operation	$\overline{CS1}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.47	V
	V_{DDQ}	2.37	2.5	2.9	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(V_{DD}=3.3V±5%, V_{DDQ}=2.5V+0.4V/-0.13V or T_A = 0℃ to 70℃)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Vss to V_{DD}, V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	-6	-	290	mA
			-7	-	270	
			-8	-	260	
			-10	-	240	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-6	-	70	mA
			-7/8/10	-	60	
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	10	mA
			L-Ver.	-	1.0	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	10	mA
			L-Ver.	-	500	μA
Output Low Voltage	V_{OL}	I_{OL} = 1.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA		2.0	-	V
Input Low Voltage	V_{IL}			-0.3*	0.7	V
Input High Voltage	V_{IH}			1.7	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)

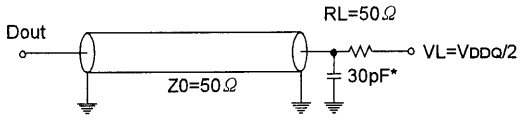
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

TEST CONDITIONS

(T_A = 0℃ to 70℃, V_{DD}=3.3V±5%, V_{DDQ}=2.5V+0.4V/-0.13V, unless otherwise specified)

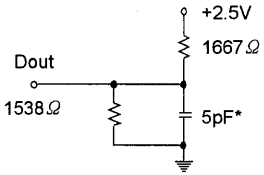
Parameter	Value
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.1V)	2ns
Input and Output Timing Reference Levels	V_{DDQ}/2
Output Load	See Fig. 1

Output Load(A)



* Capacitive Load consists of all components of the test environment.

Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

SAMSUNG ELECTRONICS

AC TIMING CHARACTERISTICS

(V_{DD}=3.3V±5%, V_{DDQ}=2.5V+0.4V/-0.13V, T_A = 0℃ to 70℃)

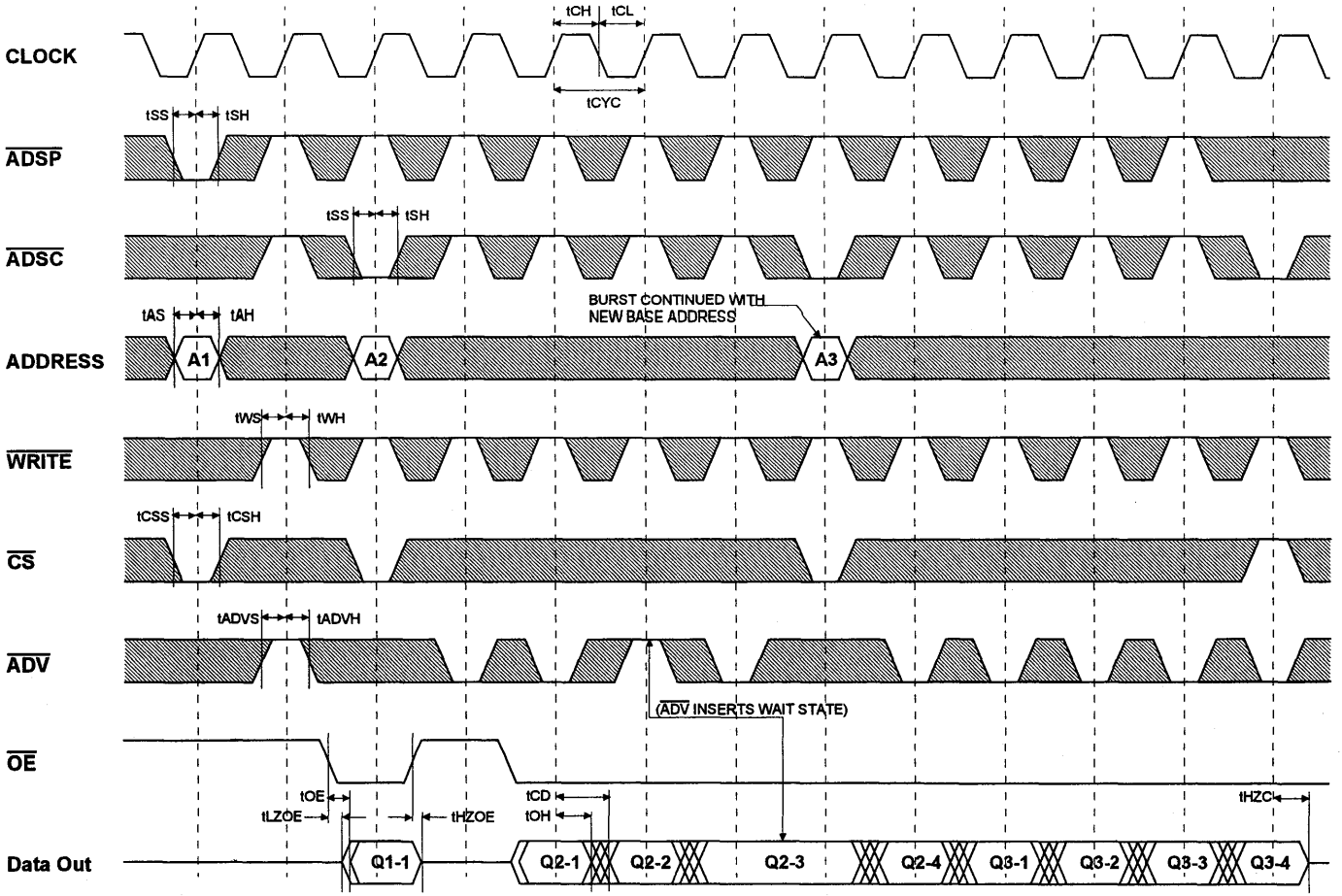
Parameter	Symbol	KM732V595A-6		KM732V595A-7		KM732V595A-8		KM732V595A-10		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	6.6	-	7.5	-	8.6	-	10	-	ns
Clock Access Time	tCD	-	4.4	-	5.0	-	5.0	-	5.5	ns
Output Enable to Data Valid	tOE	-	4.8	-	4.8	-	5.0	-	5.5	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	2.0	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	2.5	-	2.5	-	2.5	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.5	-	2.5	-	2.5	-	3.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

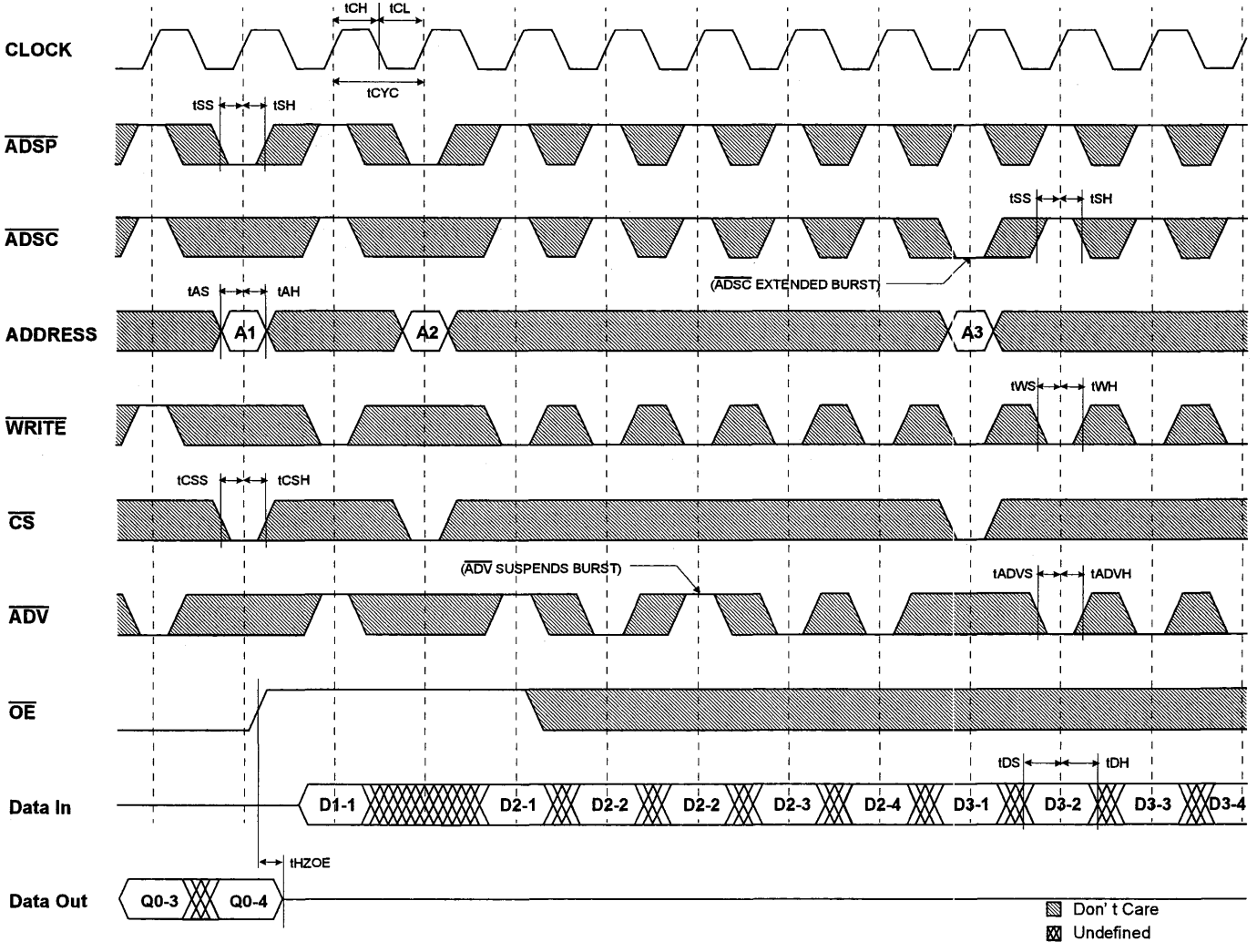
TIMING WAVEFORM OF READ CYCLE



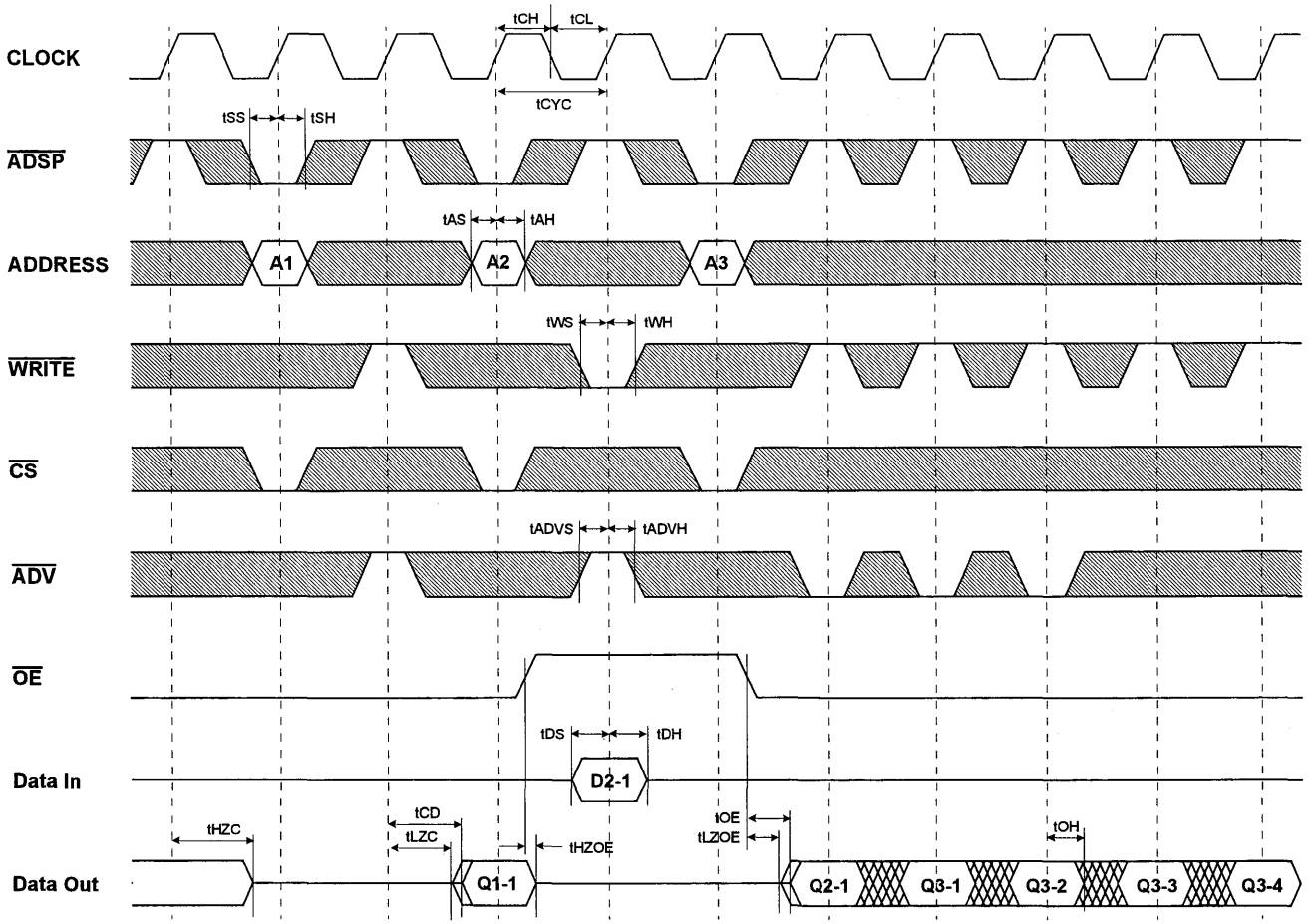
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}x$ = L
$\overline{CS}$ = L means $\overline{CS}1$ = L, CS2 = H and $\overline{CS}2$ = L
$\overline{CS}$ = H means $\overline{CS}1$ = H, or $\overline{CS}1$ = L and $\overline{CS}2$ = H, or $\overline{CS}1$ = L, and CS2 = L

▨ Don' t Care
▩ Undefined

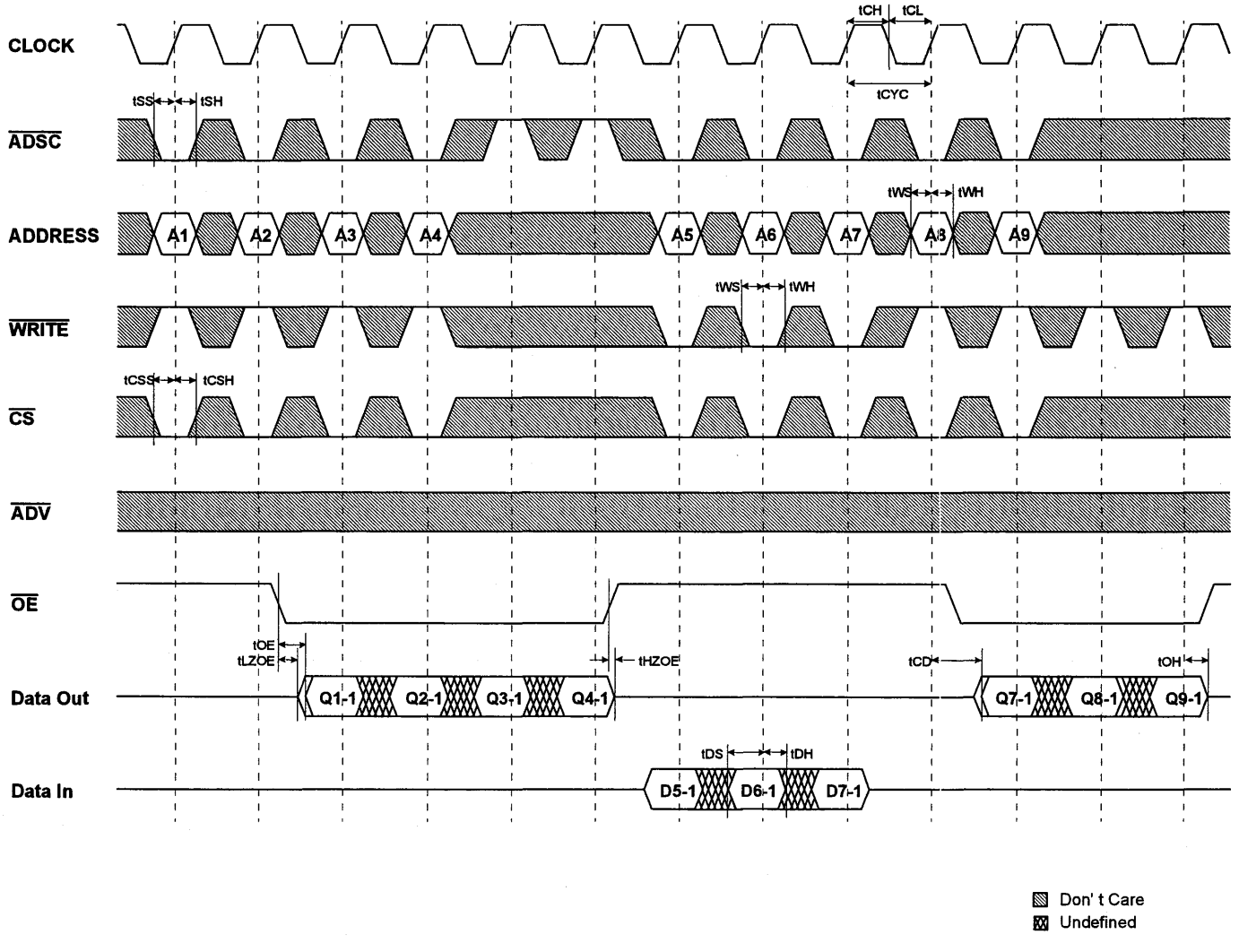
TIMING WAVEFORM OF WRTE CYCLE



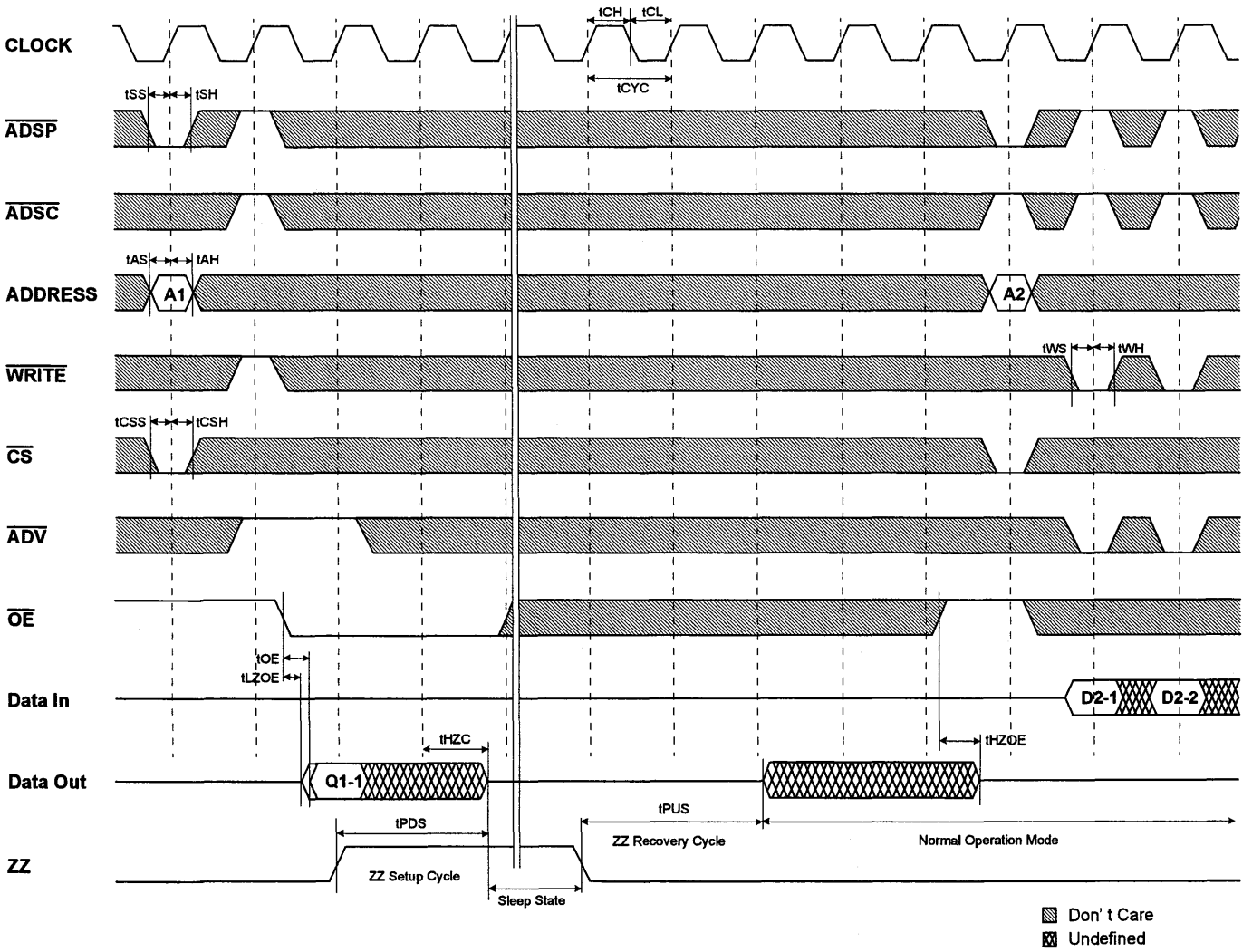
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



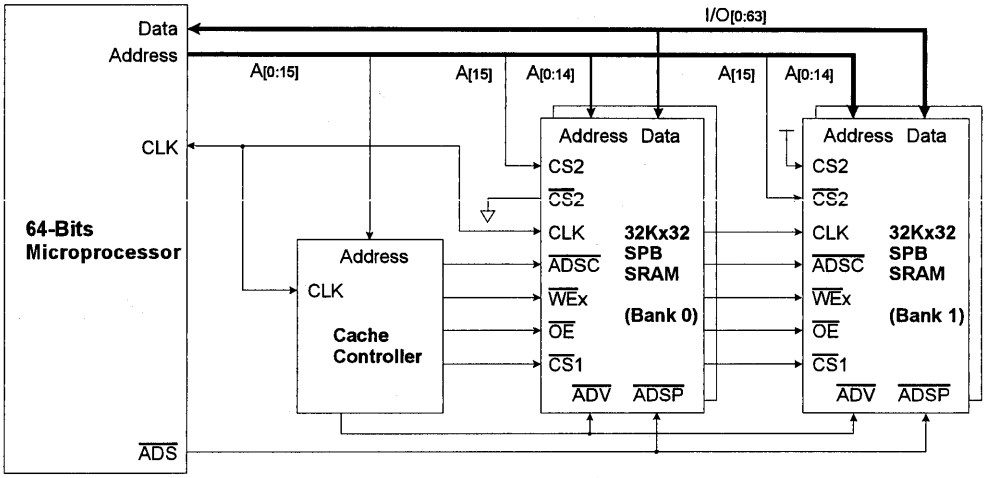
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

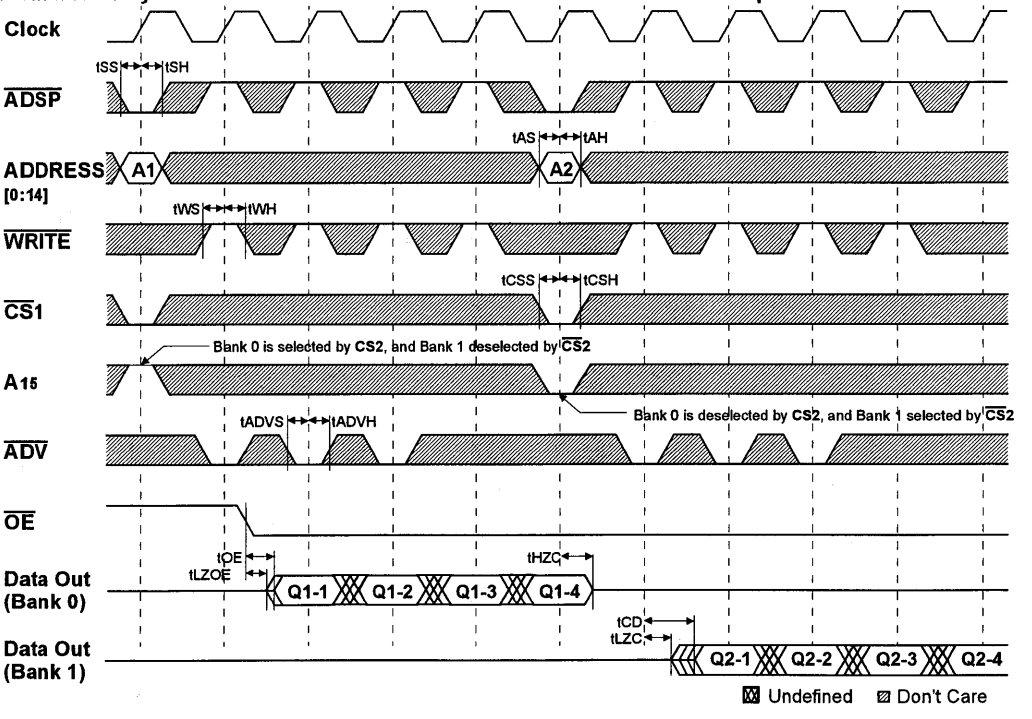
DEPTH EXPANSION

The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer non-interleave write timing for interleave write timing)

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.



32Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- VDD = 3.3V-5%/+10% Power Supply
- 5V Tolerant Inputs except I/O Pins
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-7	-8	-10	Unit
Cycle Time	tCYC	7.5	8.6	10	ns
Clock Access Time	tCD	4.5	5.0	5.0	ns
Output Enable Access Time	tOE	4.5	5.0	5.0	ns

GENERAL DESCRIPTION

The KM732V599A/L is a 1,048,576-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 32K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signals.

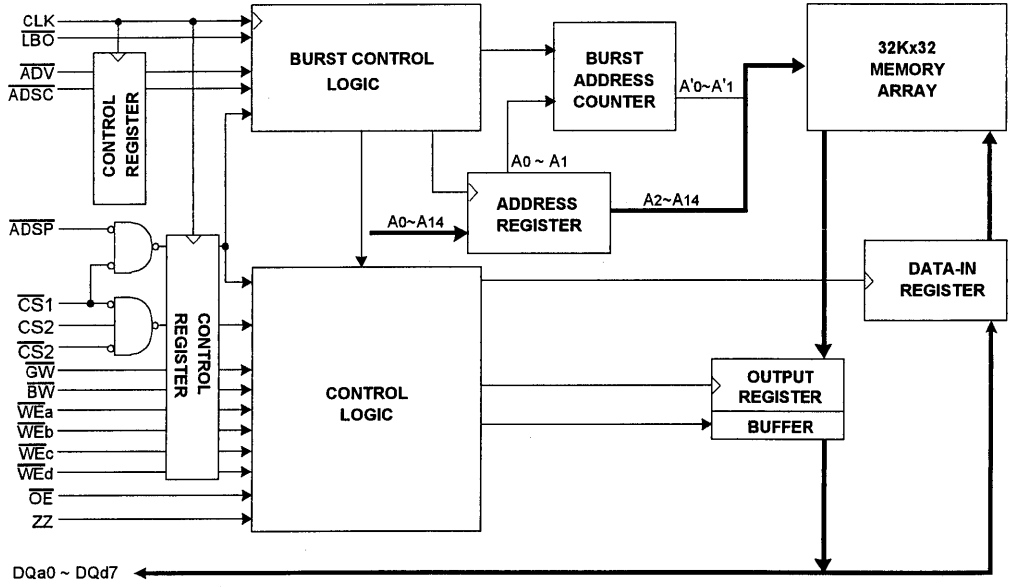
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

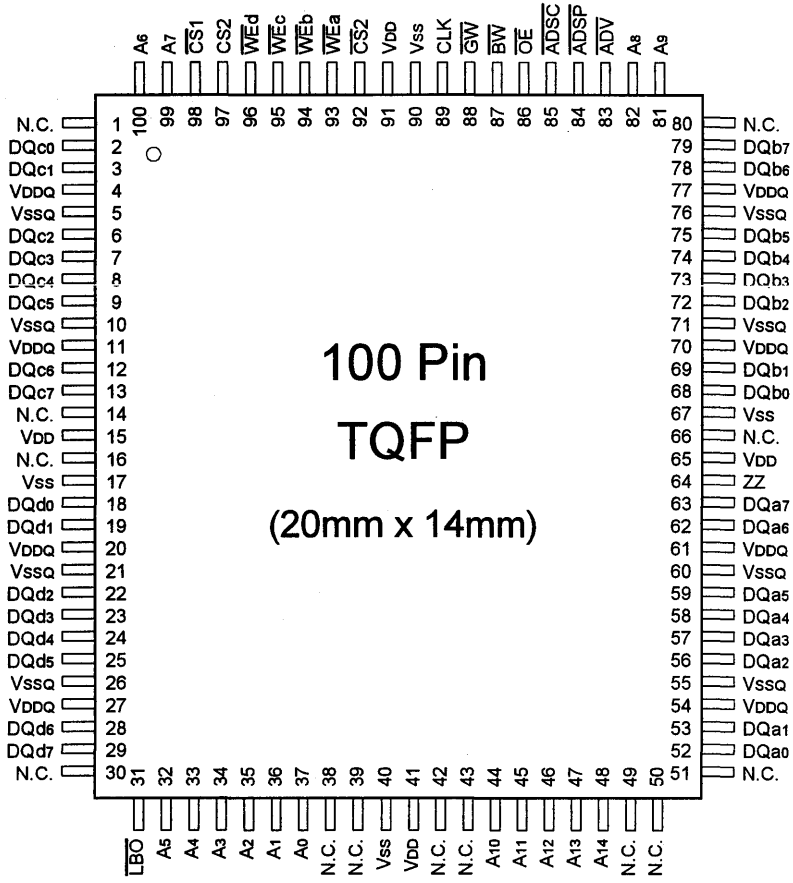
The KM732V599A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,81, 82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,14,16,30,38,39,42,43, 49,50,51,66,80
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97			
$\overline{CS2}$	Chip Select	92	VDDQ	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
$\overline{WE}$x	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

SAMSUNG ELECTRONICS

FUNCTION DESCRIPTION

The KM732V599A/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$. The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WEx}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WEx}$ are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$(regardless of $\overline{BW}$ and $\overline{WEx}$.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WEx}$ when $\overline{GW}$ is high.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WEx}$. $\overline{WEx}$ are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WEx}$ are sampled Low(regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WEx}$ sampled Low. The address increases internally to the next address of burst, if both $\overline{WEx}$ and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WEa}$, $\overline{WEb}$, $\overline{WEc}$ or $\overline{WEd}$) sampled low. The $\overline{WEa}$ controls DQa_0 ~ DQa_7, $\overline{WEb}$ controls DQb_0 ~ DQb_7, $\overline{WEc}$ controls DQc_0 ~ DQc_7, and $\overline{WEd}$ controls DQd_0 ~ DQd_7. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
$\overline{WEx}$ are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WRITE}$	Operation	$\overline{CS1}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.
2. $\overline{WE}$x means $\overline{WE}$a ~ $\overline{WE}$d.

2

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
	V_{DDQ}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

CAPACITANCE*(T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(V_{DD}=3.3V-5%+10%, T_A = 0℃ to 70℃)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Vss to V_{DD}, V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	-7	-	270	mA
			-8	-	260	
			-10	-	240	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-7	-	60	mA
			-8	-	60	
			-10	-	60	
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs = fixed(V_{DD}-0.2V or 0.2V)		-	10	mA
			L-Ver.	-	1.0	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	10	mA
			L-Ver.	-	500	μA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.0	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)

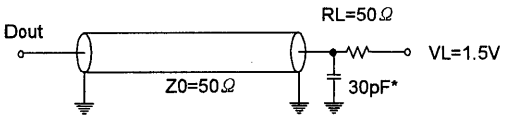
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

TEST CONDITIONS

(T_A = 0℃ to 70℃, V_{DD}=3.3V-5%/+10% unless otherwise specified)

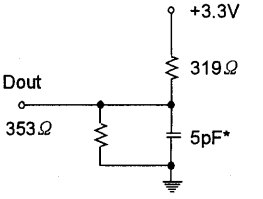
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)



* Capacitive Load consists of all components of the test environment.

Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

(V_{DD}=3.3V-5%/+10%, T_A = 0℃ to 70℃)

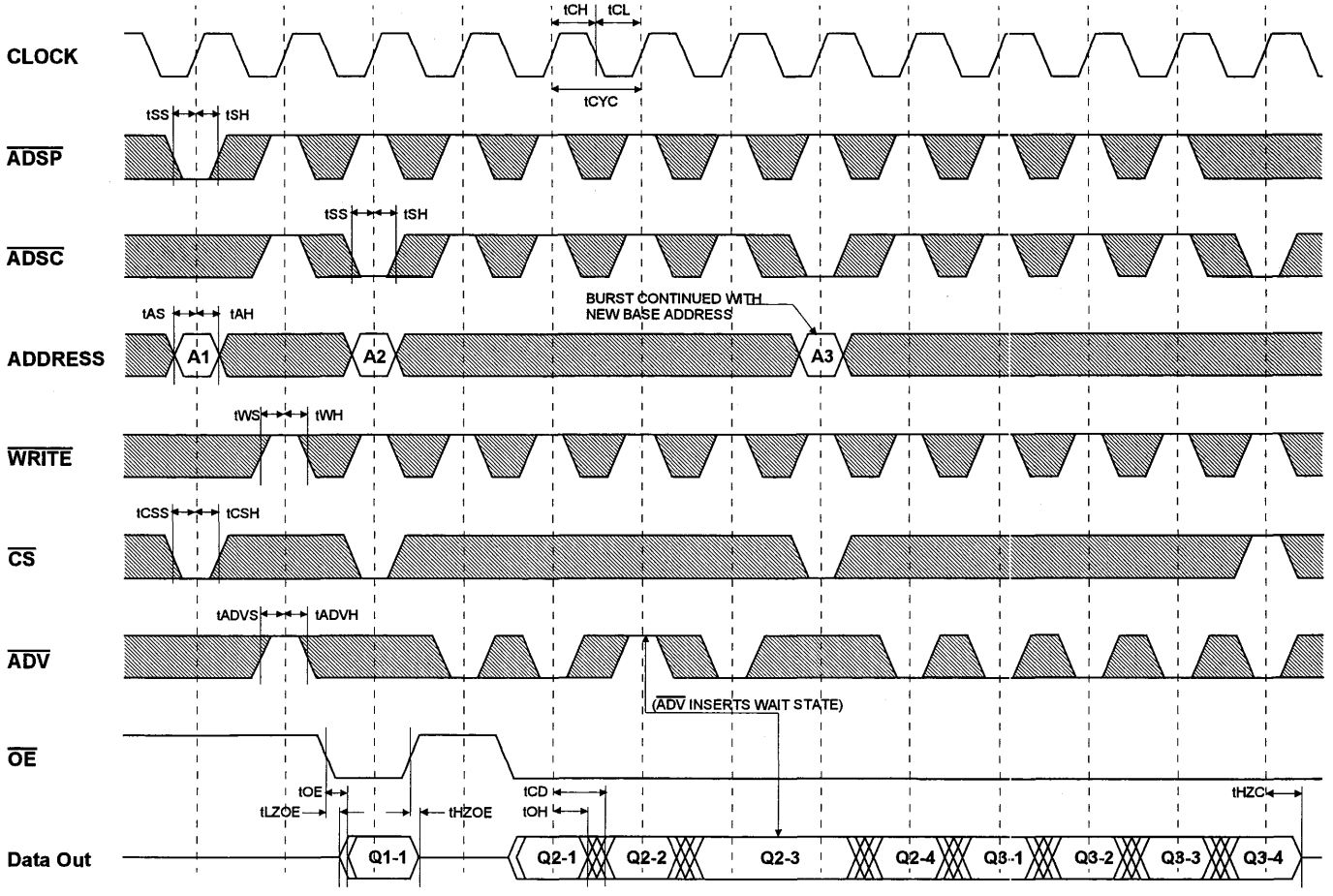
Parameter	Symbol	KM732V599A-7		KM732V599A-8		KM732V599A-10		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	7.5	-	8.6	-	10	-	ns
Clock Access Time	tCD	-	4.5	-	5.0	-	5.0	ns
Output Enable to Data Valid	tOE	-	4.5	-	5.0	-	5.0	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	2.5	-	2.5	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.5	-	2.5	-	3.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWS	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

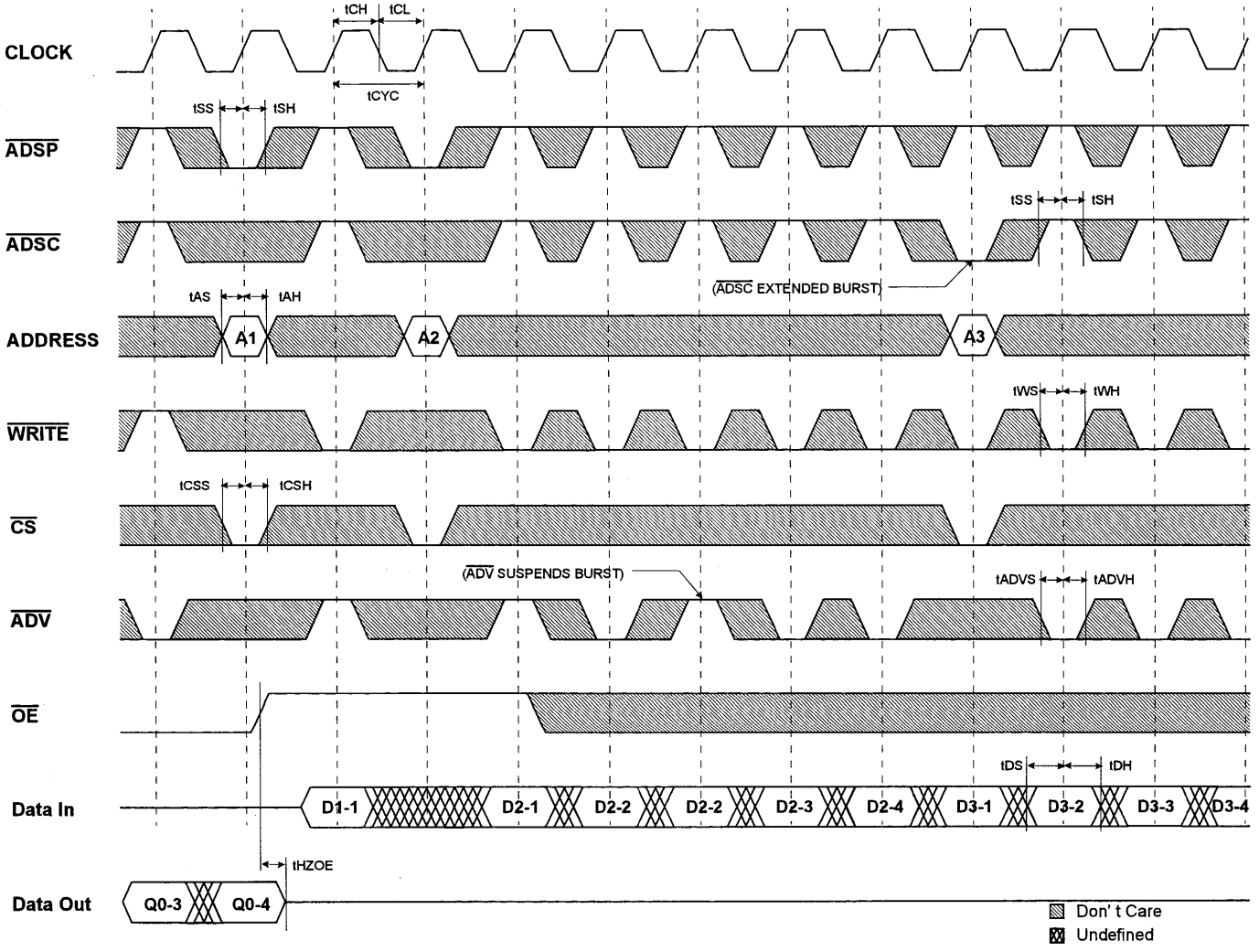
TIMING WAVEFORM OF READ CYCLE



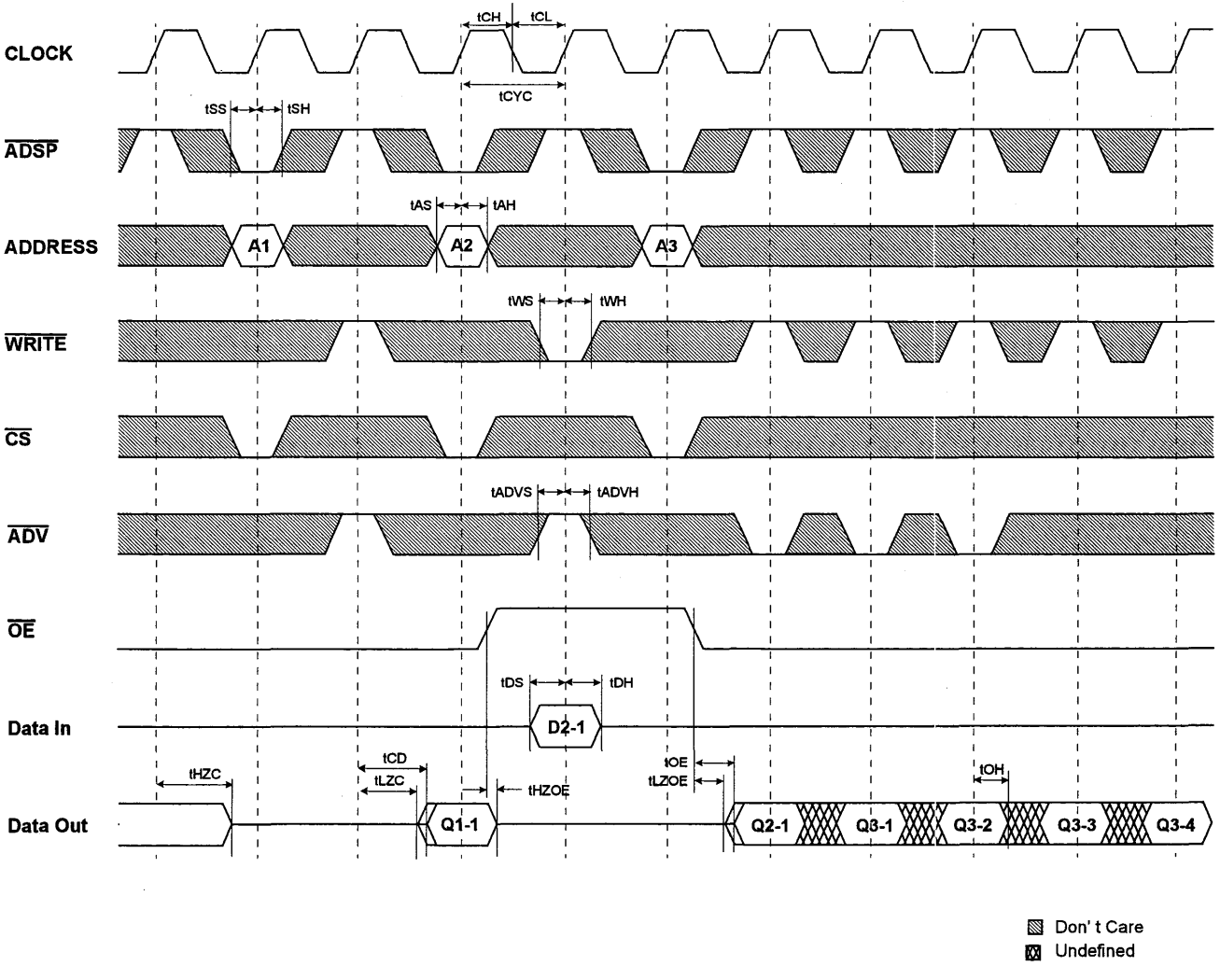
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WEx}$ = L
$\overline{CS}$ = L means $\overline{CS1}$ = L, CS2 = H and $\overline{CS2}$ = L
$\overline{CS}$ = H means $\overline{CS1}$ = H, or $\overline{CS1}$ = L and $\overline{CS2}$ = H, or $\overline{CS1}$ = L, and CS2 = L

Don' t Care
Undefined

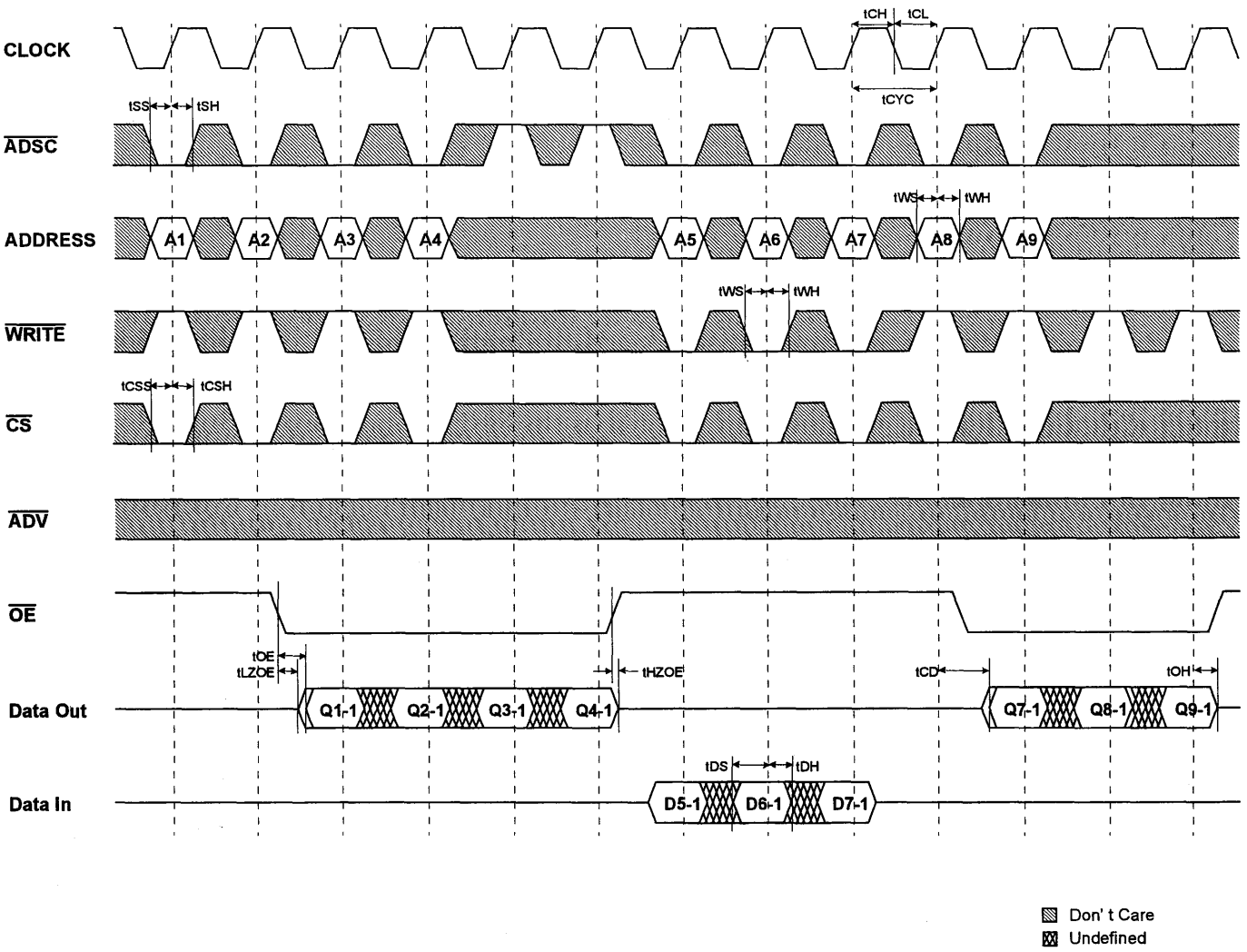
TIMING WAVEFORM OF WRTE CYCLE



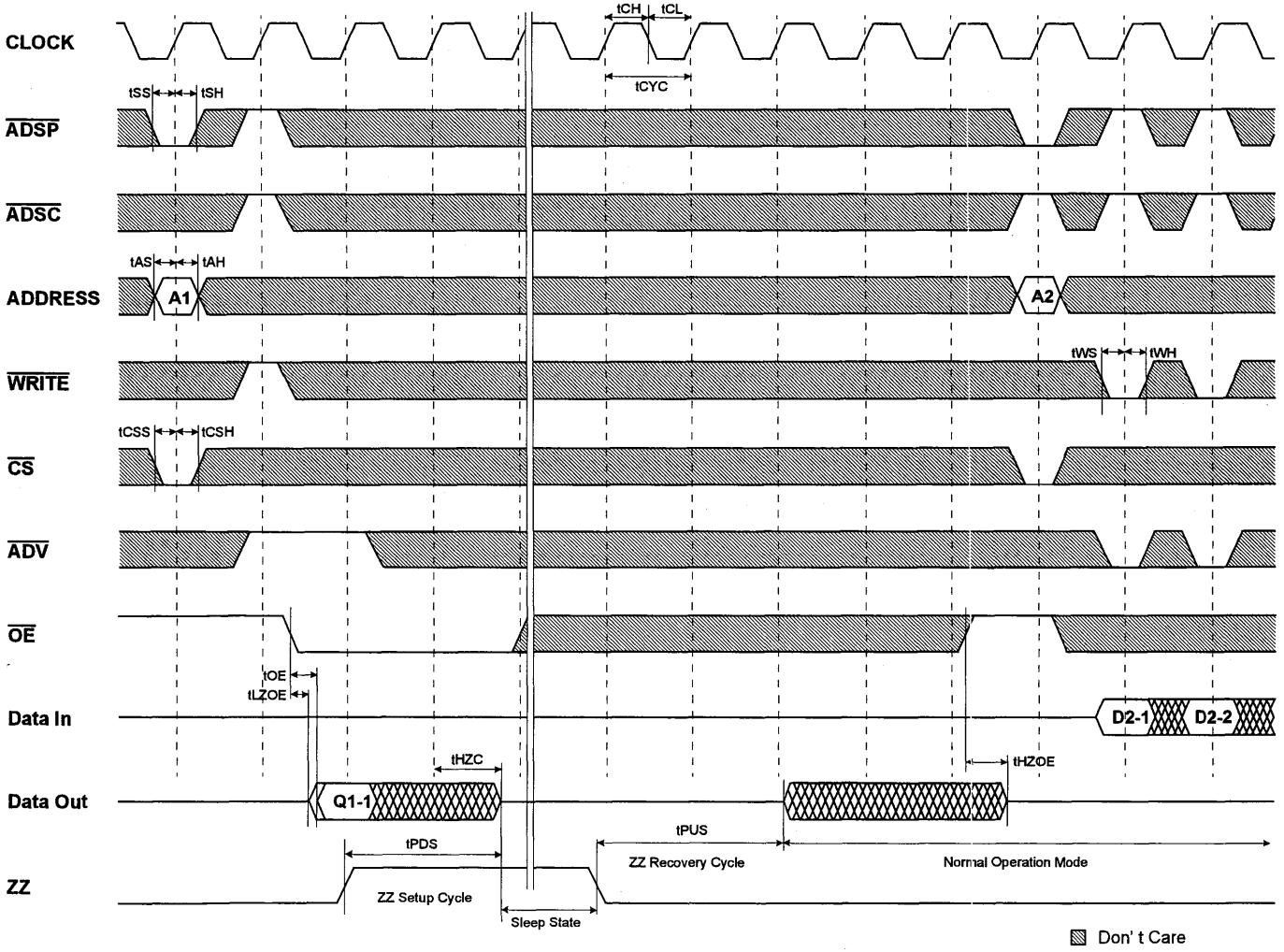
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



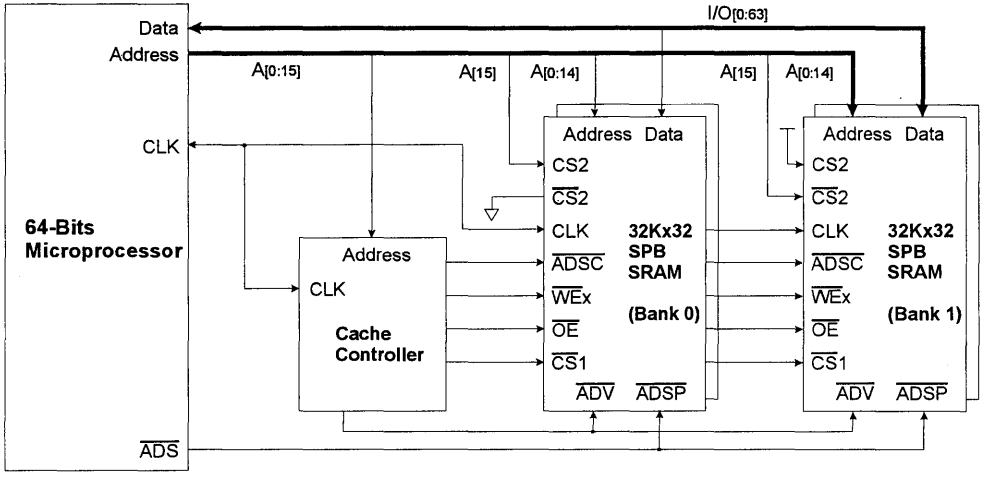
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

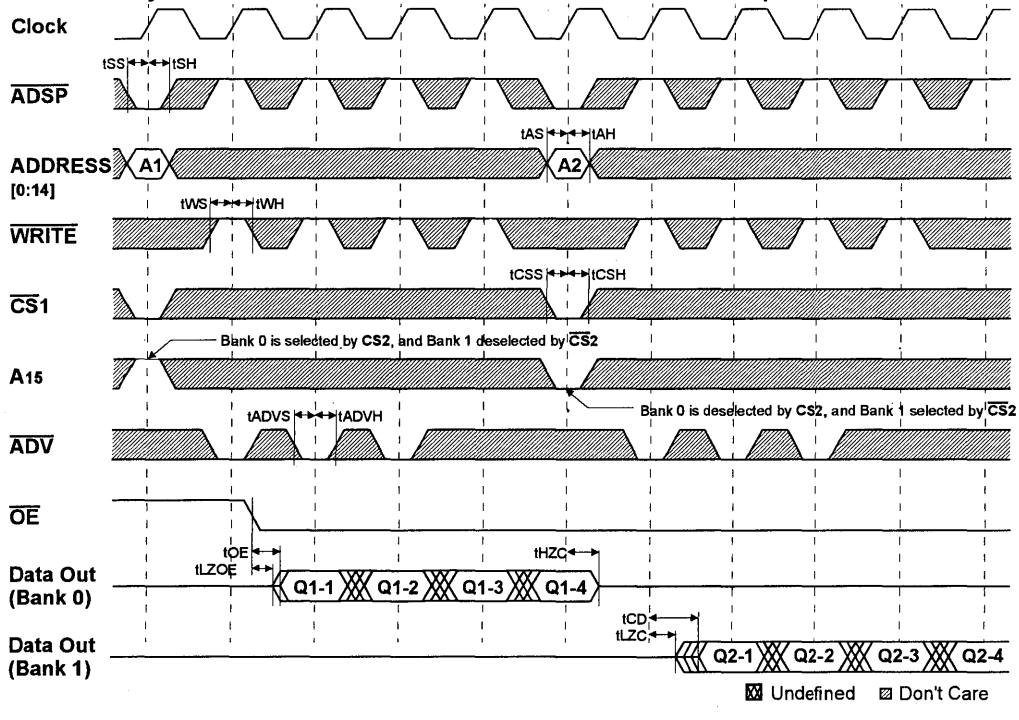
DEPTH EXPANSION

The Samsung 32Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.



32Kx36-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- Core Supply Voltage : 3.3V±5%
- I/O Supply Voltage : 2.5V+0.4/-0.13V.
- 5V Tolerant Inputs except I/O Pins
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-6	-7	-8	-10	Unit
Cycle Time	tCYC	6.6	7.5	8.6	10	ns
Clock Access Time	tCD	4.4	5.0	5.0	5.5	ns
Output Enable Access Time	tOE	4.8	4.8	5.0	5.5	ns

GENERAL DESCRIPTION

The KM736V595A/L is a 1,179,648 bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 32K words of 36bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high.

And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signals.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs.

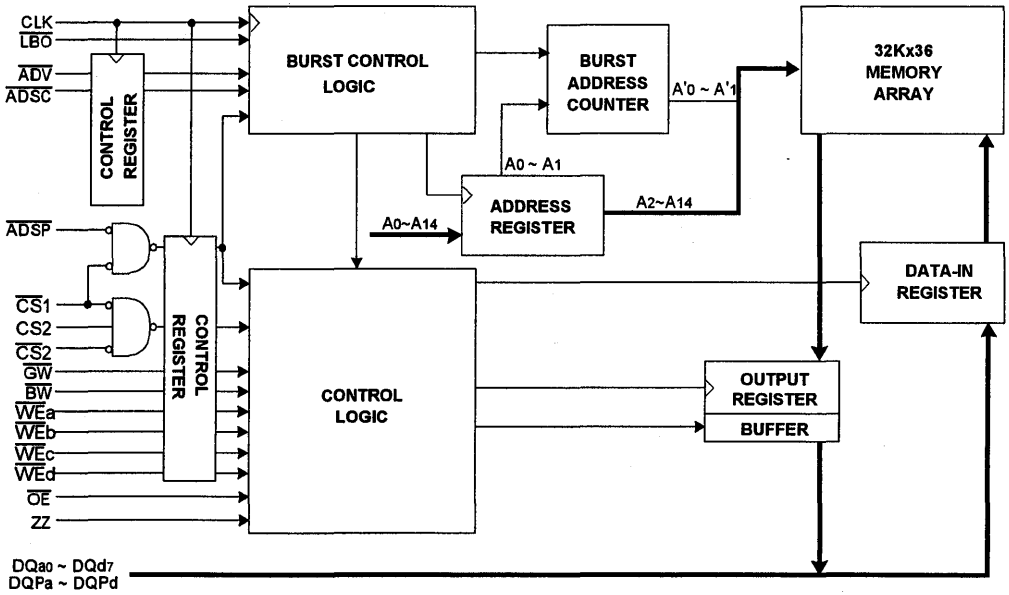
Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

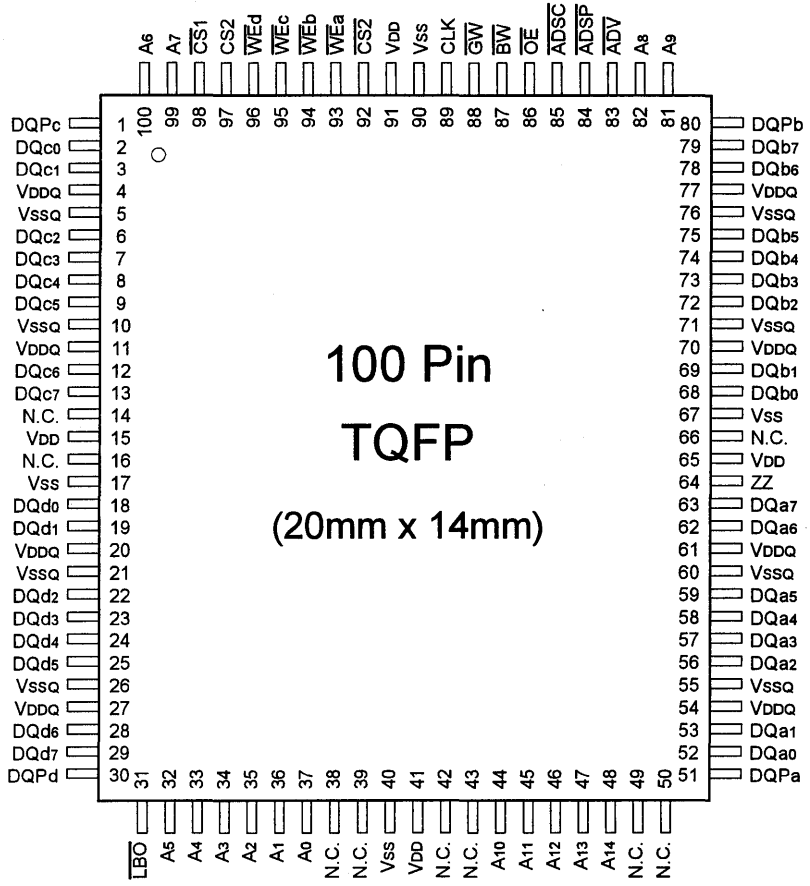
The KM736V595A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,81, 82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,43,49,50 66
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa~Pd		51,80,1,30
$\overline{CS2}$	Chip Select	92			
$\overline{WEx}$	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply (+2.5V)	4,11,20,27,54,61,70,77
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM736V595A/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$. The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$(regardless of $\overline{BW}$ and $\overline{WE}$x.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x when $\overline{GW}$ is high.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled Low(regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled Low. The address increases internally to the next address of burst, if both $\overline{WE}$x and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. The $\overline{WE}$a controls DQa_0 ~ DQa_7 and DQPa, $\overline{WE}$b controls DQb_0 ~ DQb_7 and DQPb, $\overline{WE}$c controls DQc_0 ~ DQc_7 and DQPc, and $\overline{WE}$d control DQd_0 ~ DQd_7 and DQPd. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$x are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WRITE}$	Operation	$\overline{CS1}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.47	V
	V_{DDQ}	2.37	2.5	2.9	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(V_{DD}=3.3V±5%, V_{DDQ}=2.5V+0.4V/-0.13V or T_A = 0℃ to 70℃)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Vss to V_{DD}, V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	-6	-	290	mA
			-7	-	270	
			-8	-	260	
			-10	-	240	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-6	-	70	mA
			-7/8/10	-	60	mA
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	10	mA
			L-Ver.	-	1.0	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	10	mA
			L-Ver.	-	500	μA
Output Low Voltage	V_{OL}	I_{OL} = 1.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA		2.0	-	V
Input Low Voltage	V_{IL}			-0.3*	0.7	V
Input High Voltage	V_{IH}			1.7	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)

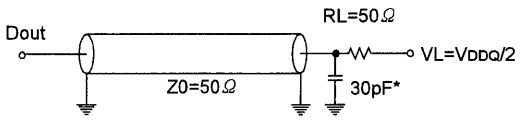
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

TEST CONDITIONS

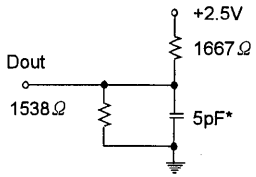
(T_A = 0℃ to 70℃, V_{DD}=3.3V±5%, V_{DDQ}=2.5V+0.4V/-0.13V unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.1V)	2ns
Input and Output Timing Reference Levels	V_{DDQ}/2
Output Load	See Fig. 1

Output Load(A)



Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

(V_{DD}=3.3V±5%, V_{DDQ}=2.5V+0.4V/-0.13V, T_A = 0℃ to 70℃)

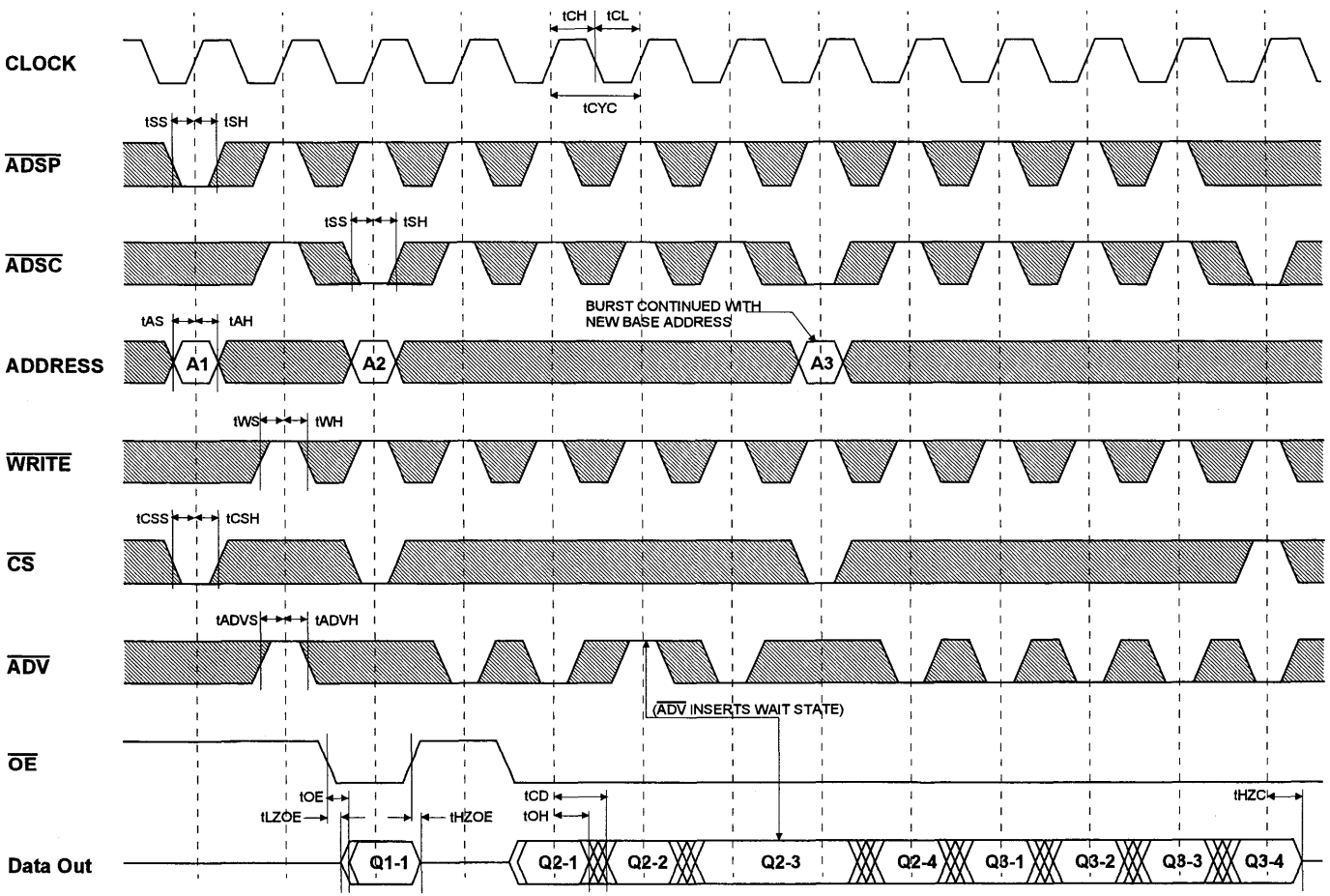
Parameter	Symbol	KM736V595A-6		KM736V595A-7		KM736V595A-8		KM736V595A-10		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	6.6	-	7.5	-	8.6	-	10	-	ns
Clock Access Time	tCD	-	4.4	-	5.0	-	5.0	-	5.5	ns
Output Enable to Data Valid	tOE	-	4.8	-	4.8	-	5.0	-	5.5	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	2.0	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	2.5	-	2.5	-	2.5	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.5	-	2.5	-	2.5	-	3.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

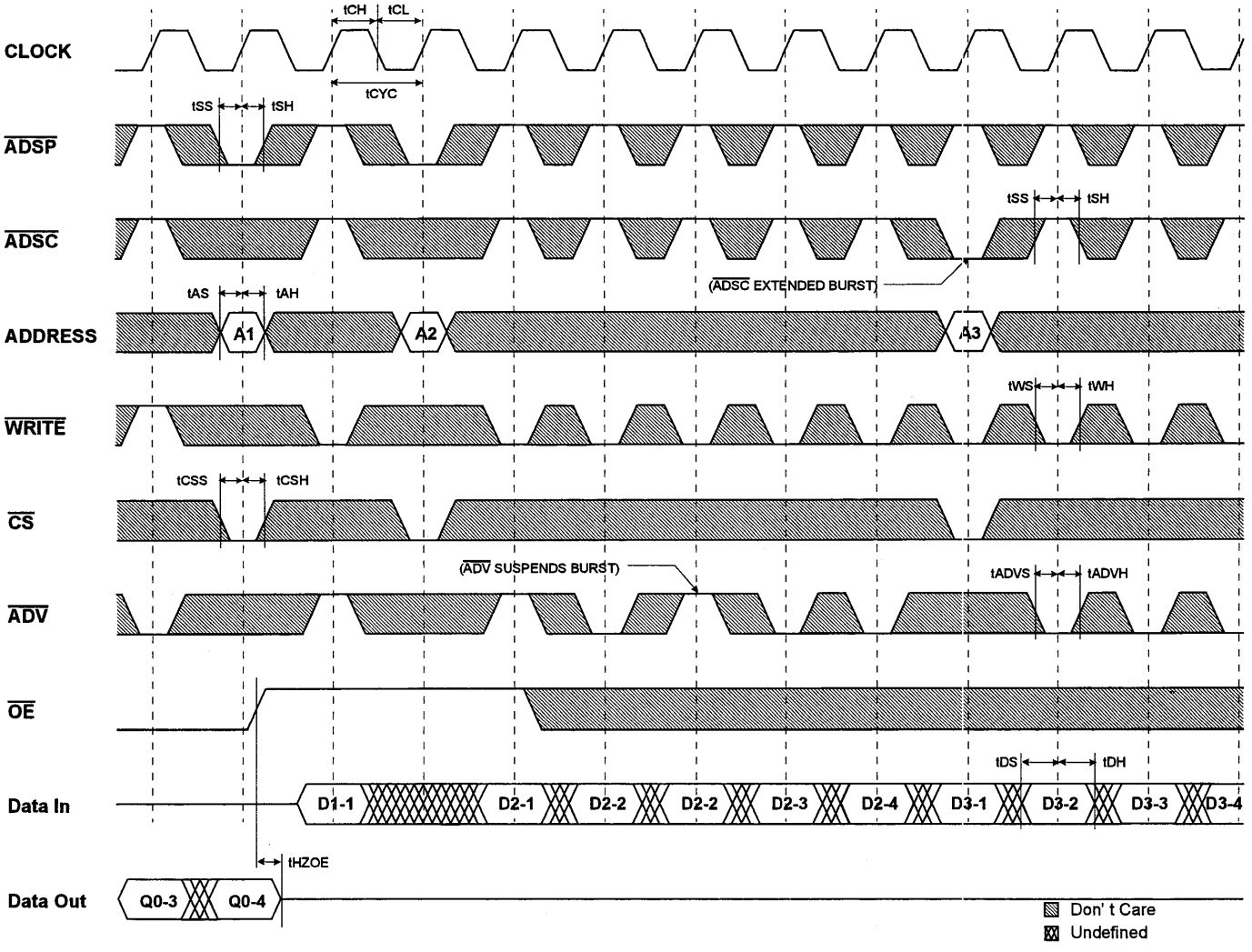
TIMING WAVEFORM OF READ CYCLE



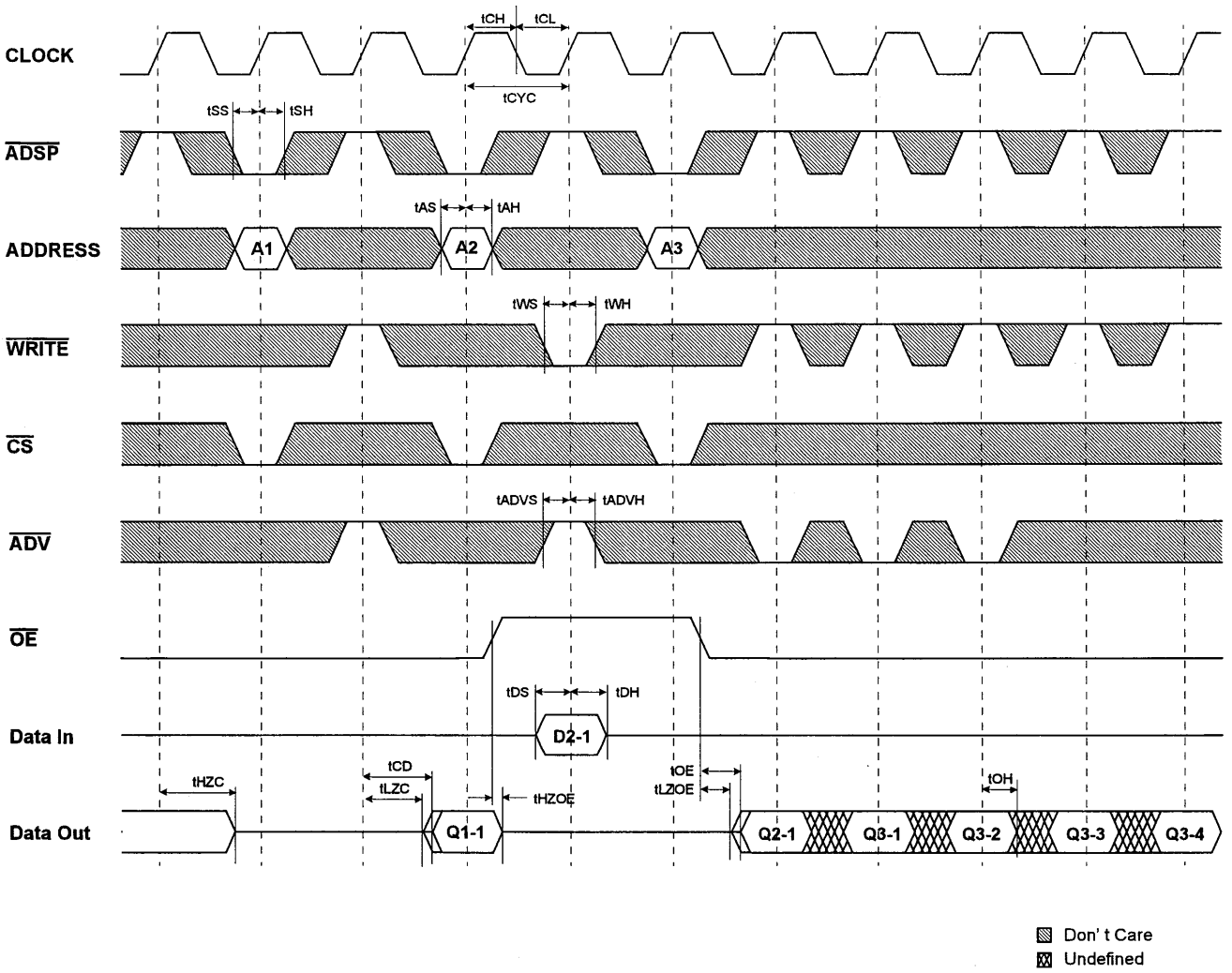
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}x$ = L
$\overline{CS}$ = L means $\overline{CS1}$ = L, CS2 = H and $\overline{CS2}$ = L
$\overline{CS}$ = H means $\overline{CS1}$ = H, or $\overline{CS1}$ = L and $\overline{CS2}$ = H, or $\overline{CS1}$ = L, and CS2 = L

▨ Don' t Care
▩ Undefined

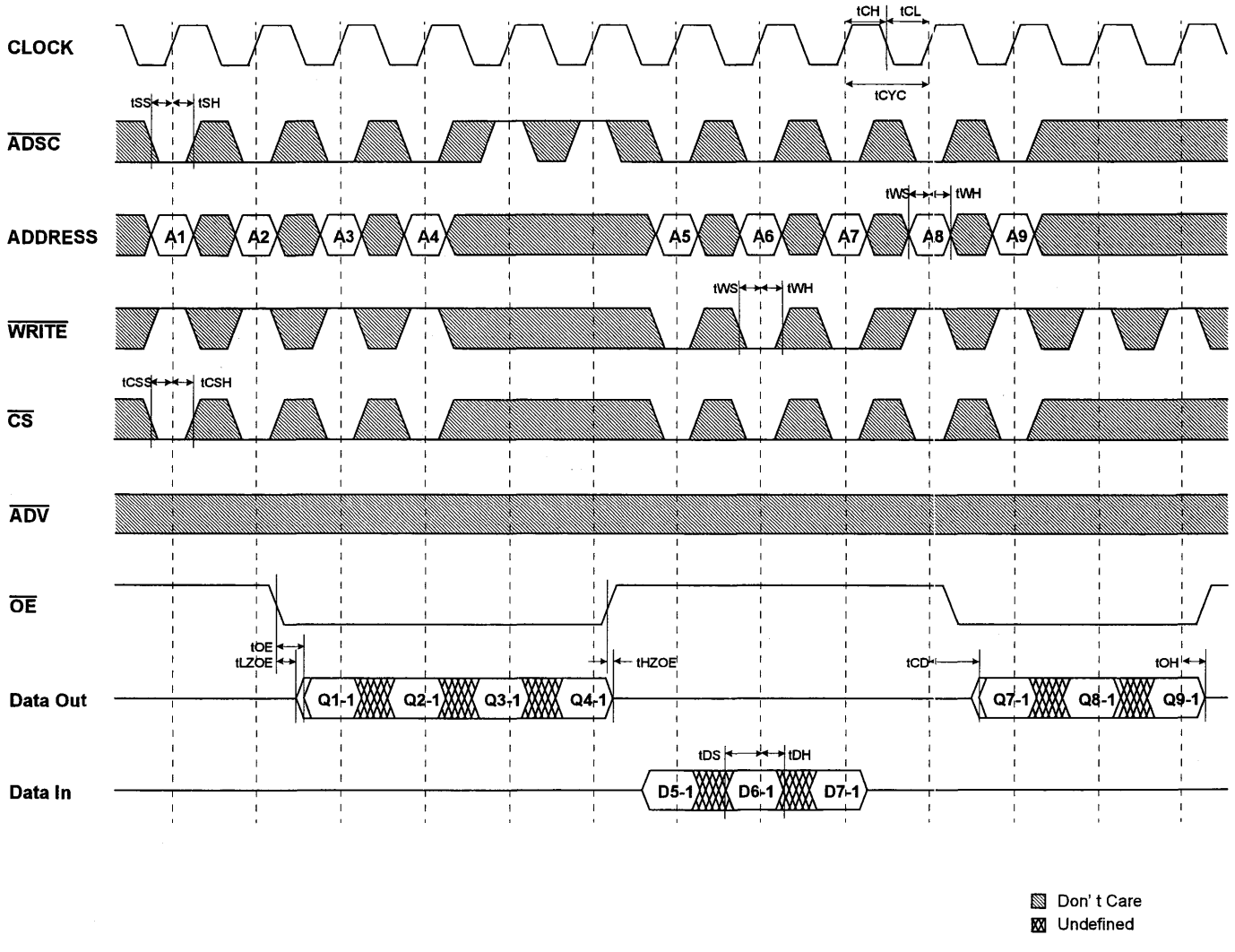
TIMING WAVEFORM OF WRTE CYCLE



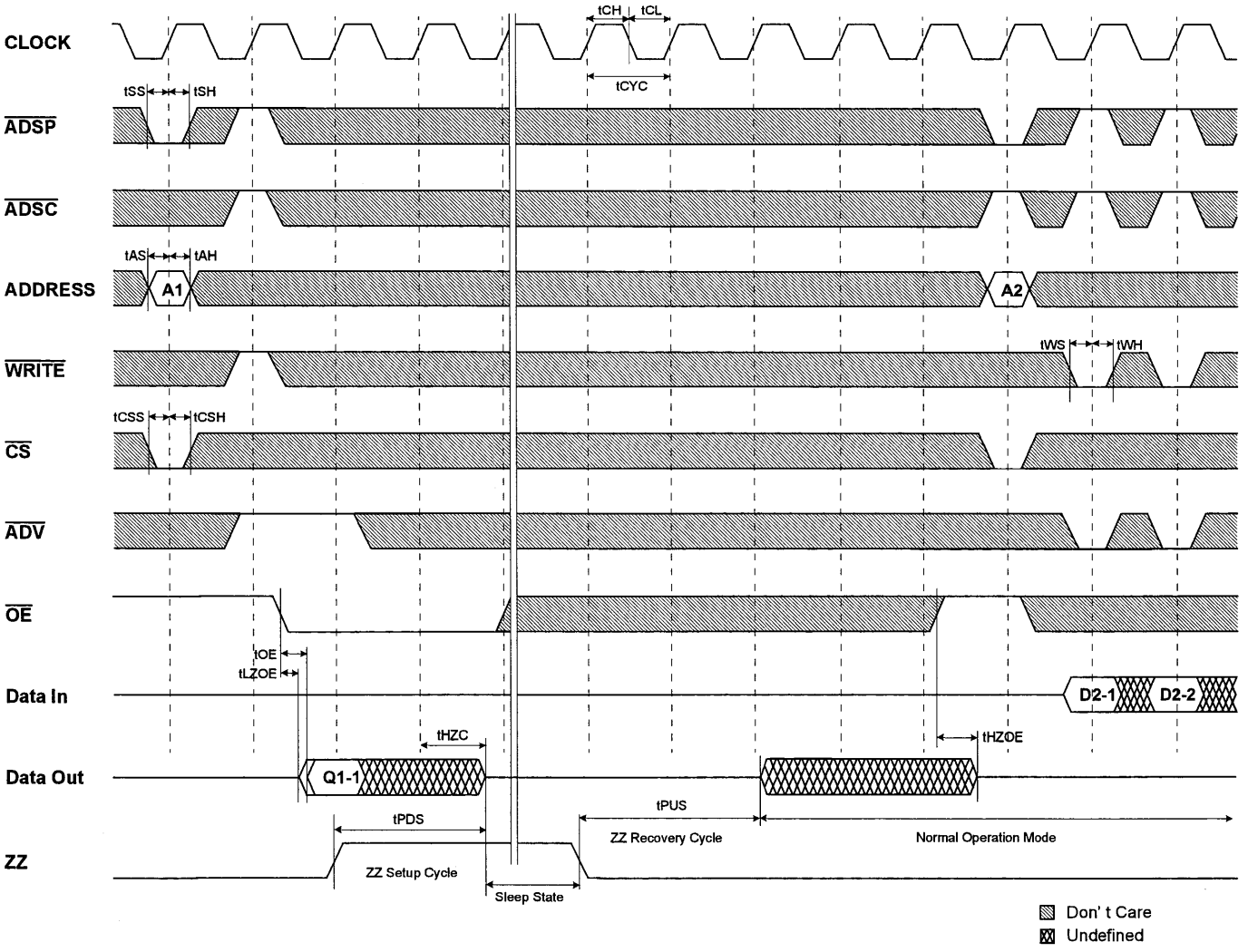
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



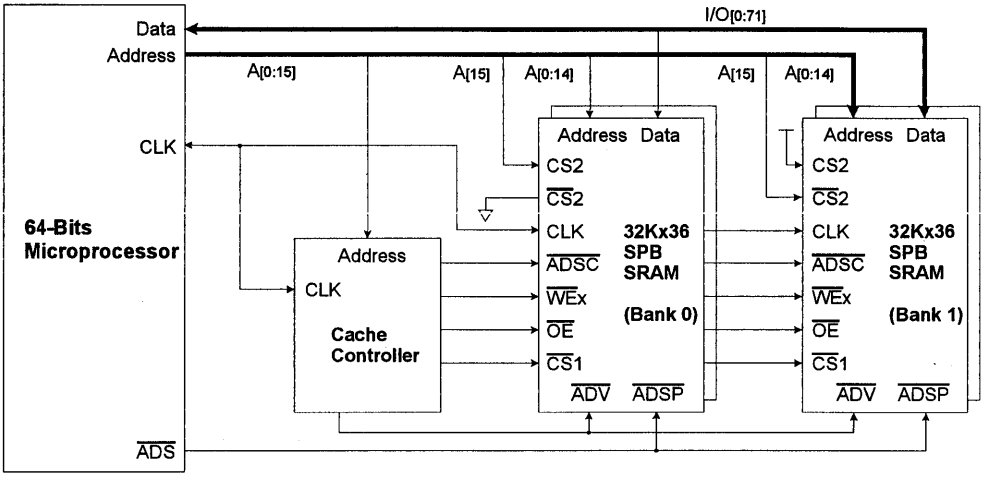
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

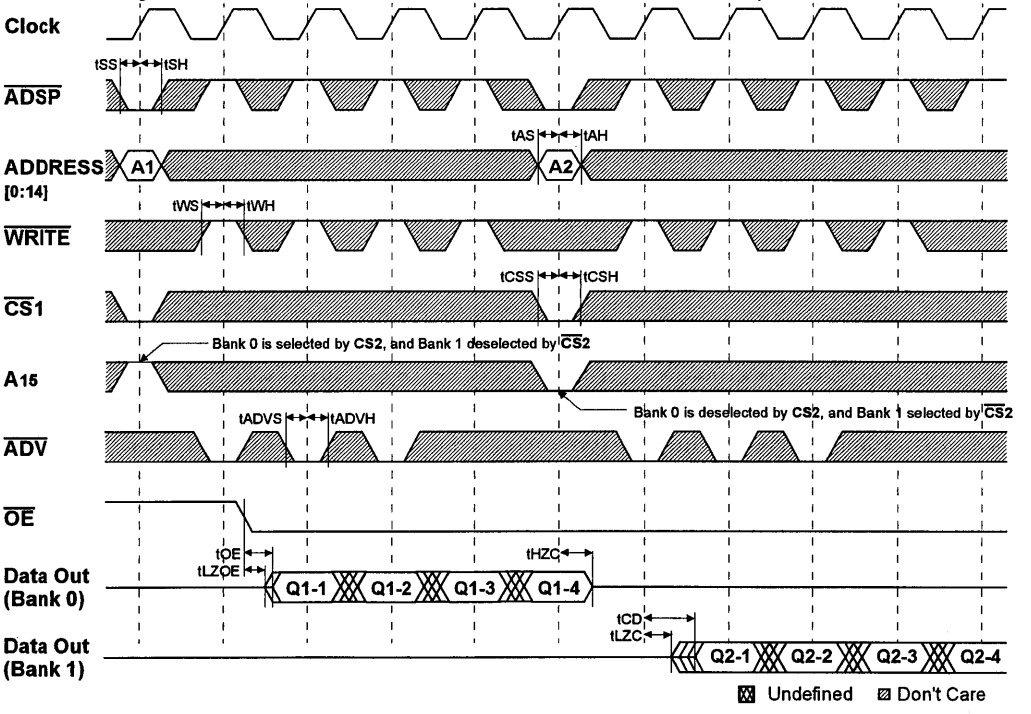
DEPTH EXPANSION

The Samsung 32Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.



32Kx36-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- Add= 3.3V-5%/+10% Power Supply
- 5V Tolerant Inputs except I/O Pins
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-Pin TQFP Package.

FAST ACCESS TIMES

Parameter	Symbol	-7	-8	-10	Unit
Cycle Time	tCYC	7.5	8.6	10	ns
Clock Access Time	tCD	4.5	5.0	5.0	ns
Output Enable Access Time	tOE	4.5	5.0	5.0	ns

GENERAL DESCRIPTION

The KM736V599A/L is a 1,179,648-bit Synchronous Static Random Access Memory designed for high performance second level cache of P6 and Power PC based System.

It is organized as 32K words of 36bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signals.

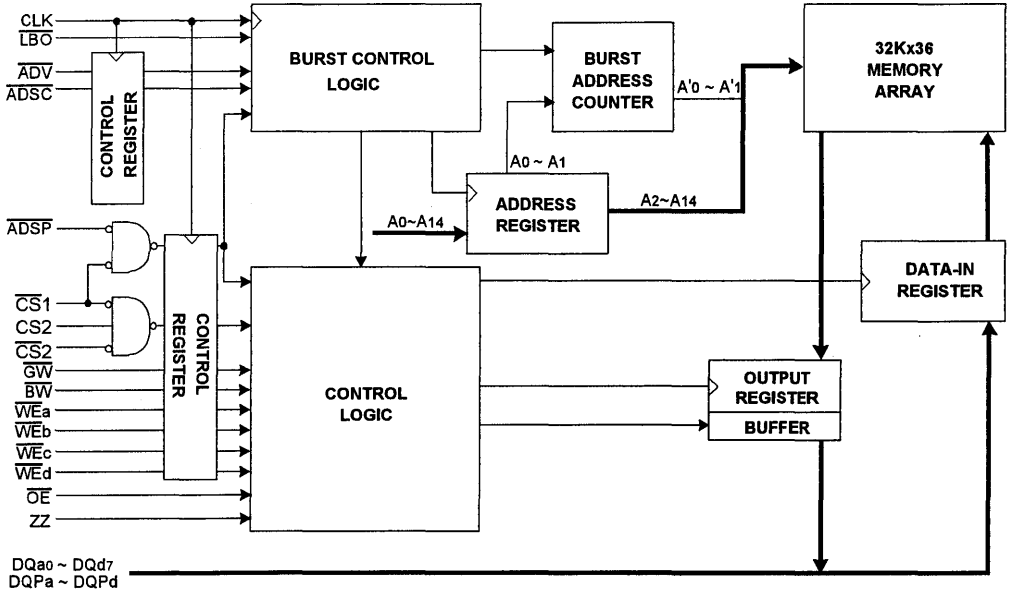
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

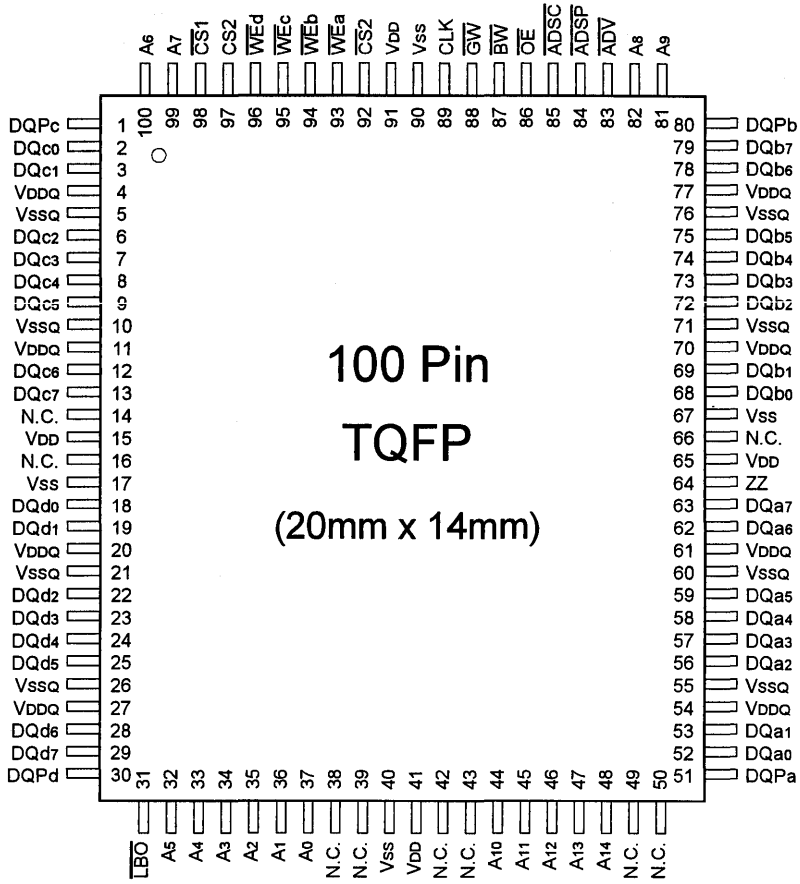
The KM736V599A/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48, 81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,43,49,50, 66
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa~Pd		51,80,1,30
$\overline{CS2}$	Chip Select	92			
$\overline{WEx}$	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

SAMSUNG ELECTRONICS

FUNCTION DESCRIPTION

The KM736V599A/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{CS1}$, $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$. The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$(regaedless of $\overline{BW}$ and $\overline{WE}$x.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x when $\overline{GW}$ is high.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled Low(regaedless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled Low. The address increases internally to the next address of burst, if both $\overline{WE}$x and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. The $\overline{WE}$a controls DQa_0 ~ DQa_7 and DQPa, $\overline{WE}$b controls DQb_0 ~ DQb_7 and DQPb, $\overline{WE}$c controls DQc_0 ~ DQc_7 and DQPc, and $\overline{WE}$d controls DQd_0 ~ DQd_7 and DQPd. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
$\overline{WE}$x are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WRITE}$	Operation	$\overline{CS1}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.
2. $\overline{WE}$x means $\overline{WE}$a ~ $\overline{WE}$d.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
	V_{DDQ}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(V_{DD}=3.3V-5%/+10%, T_A = 0℃ to 70℃)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Vss to V_{DD}, V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	-7	-	270	mA
			-8	-	260	
			-10	-	240	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-7	-	60	mA
			-8	-	60	
			-10	-	60	
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs = fixed(V_{DD}-0.2V or 0.2V)		-	10	mA
			L-Ver.	-	1	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	10	mA
			L-Ver.	-	500	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.0	5.5**	V

* V_{IL}(min)= -3.0 (Pulse Width ≤ 20ns)

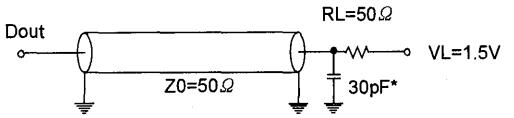
** In Case of I/O Pins, The Max. V_{IH}=V_{DDQ} + 0.5V

TEST CONDITIONS

(T_A = 0℃ to 70℃, V_{DD}=3.3V-5%/+10% unless otherwise specified)

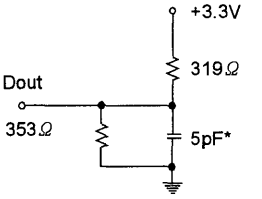
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)



* Capacitive Load consists of all components of the test environment.

Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

(V_{DD}=3.3V-5%/10%, T_A = 0℃ to 70℃)

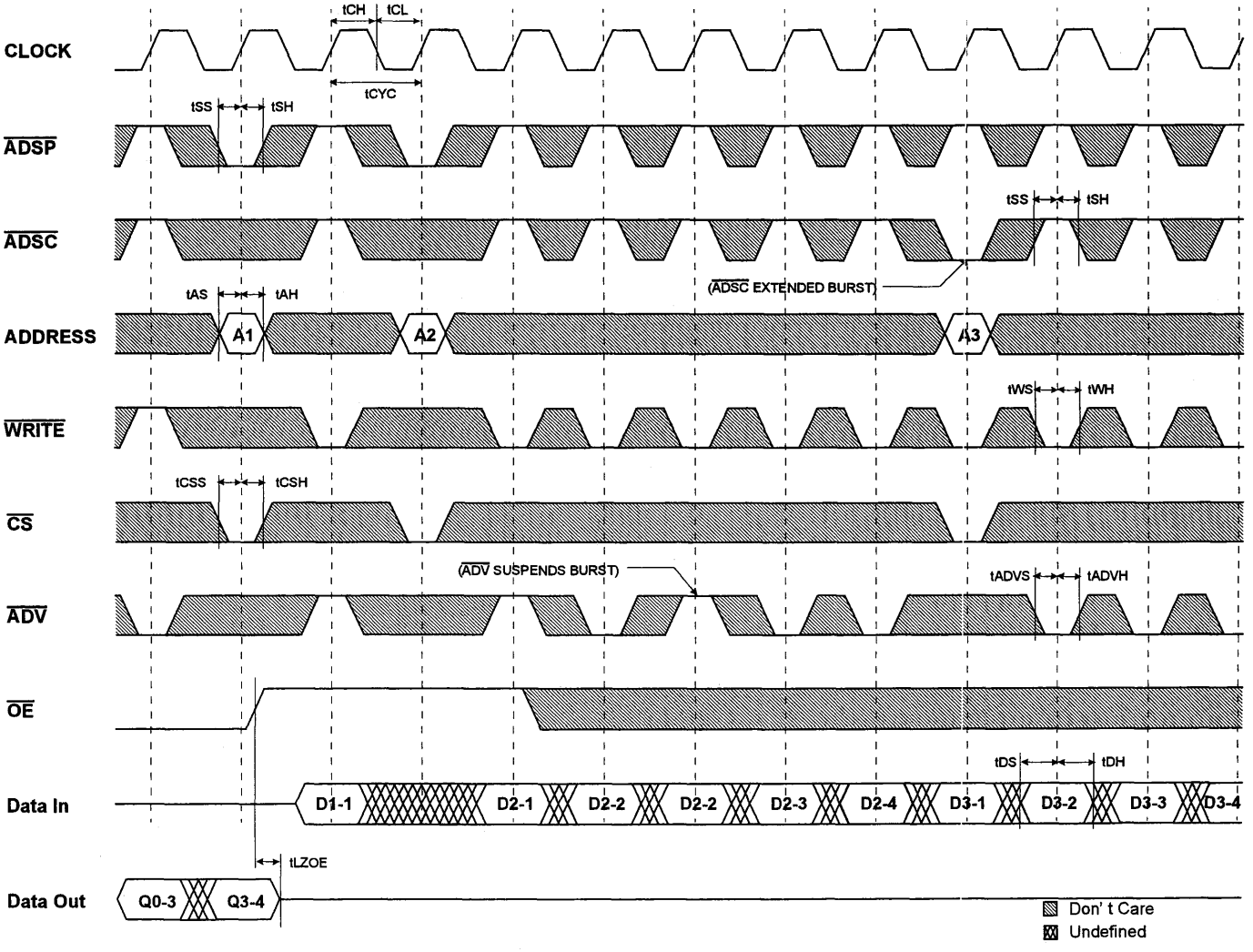
Parameter	Symbol	KM736V599A-7		KM736V599A-8		KM736V599A-10		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	7.5	-	8.6	-	10	-	ns
Clock Access Time	tCD	-	4.5	-	5.0	-	5.0	ns
Output Enable to Data Valid	tOE	-	4.5	-	5.0	-	5.0	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	2.5	-	2.5	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.5	-	2.5	-	3.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWS	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

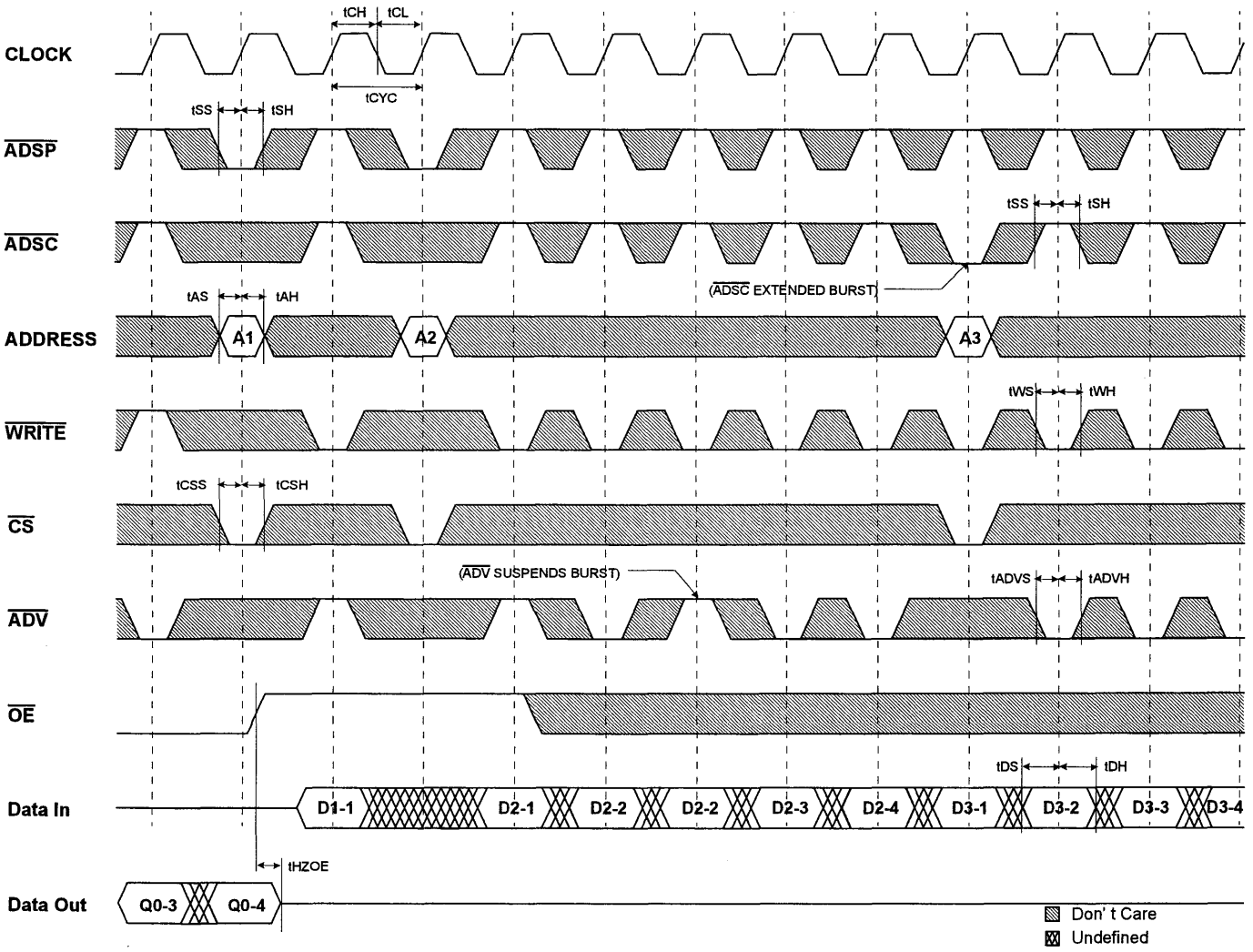
2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

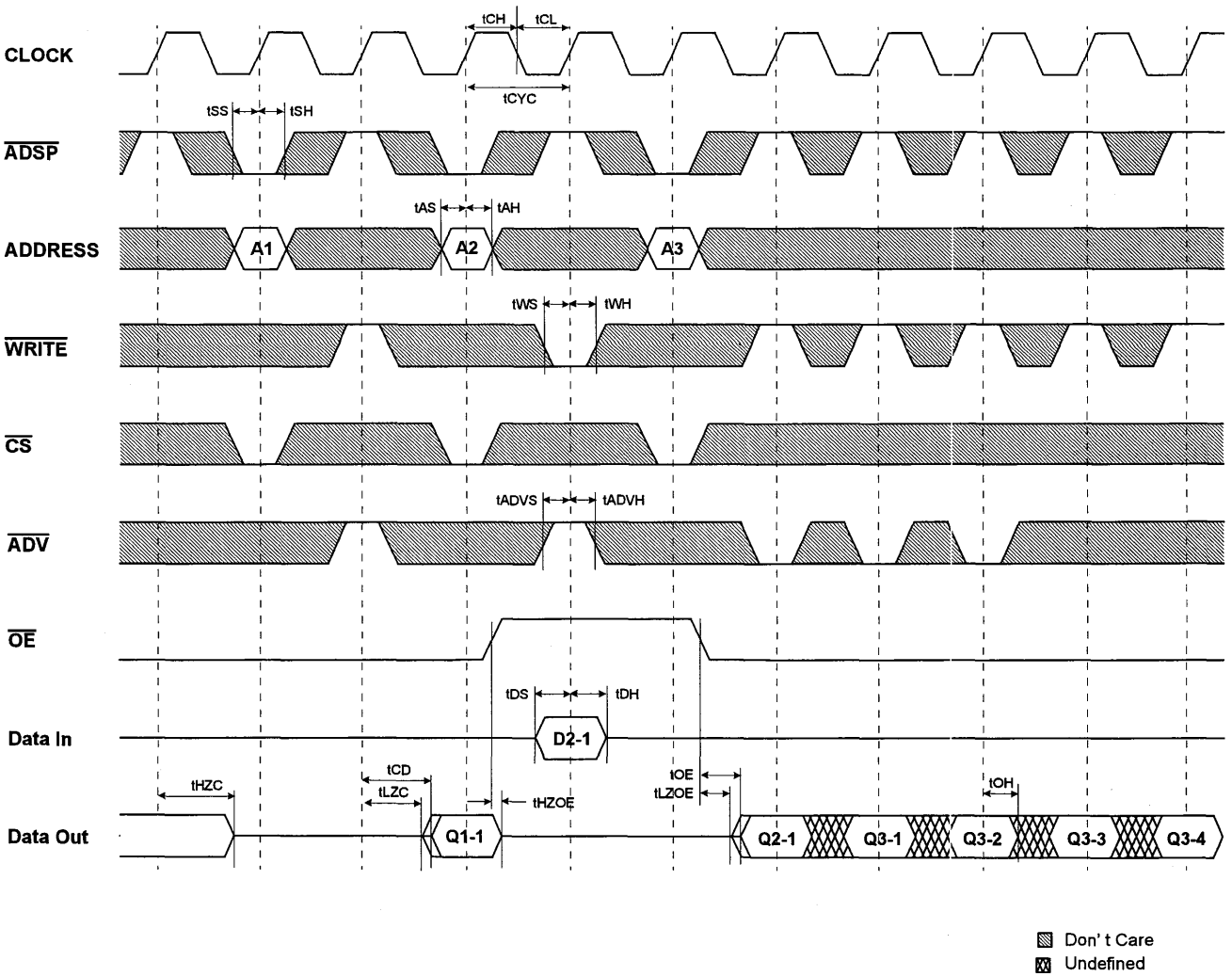
TIMING WAVEFORM OF WRTE CYCLE



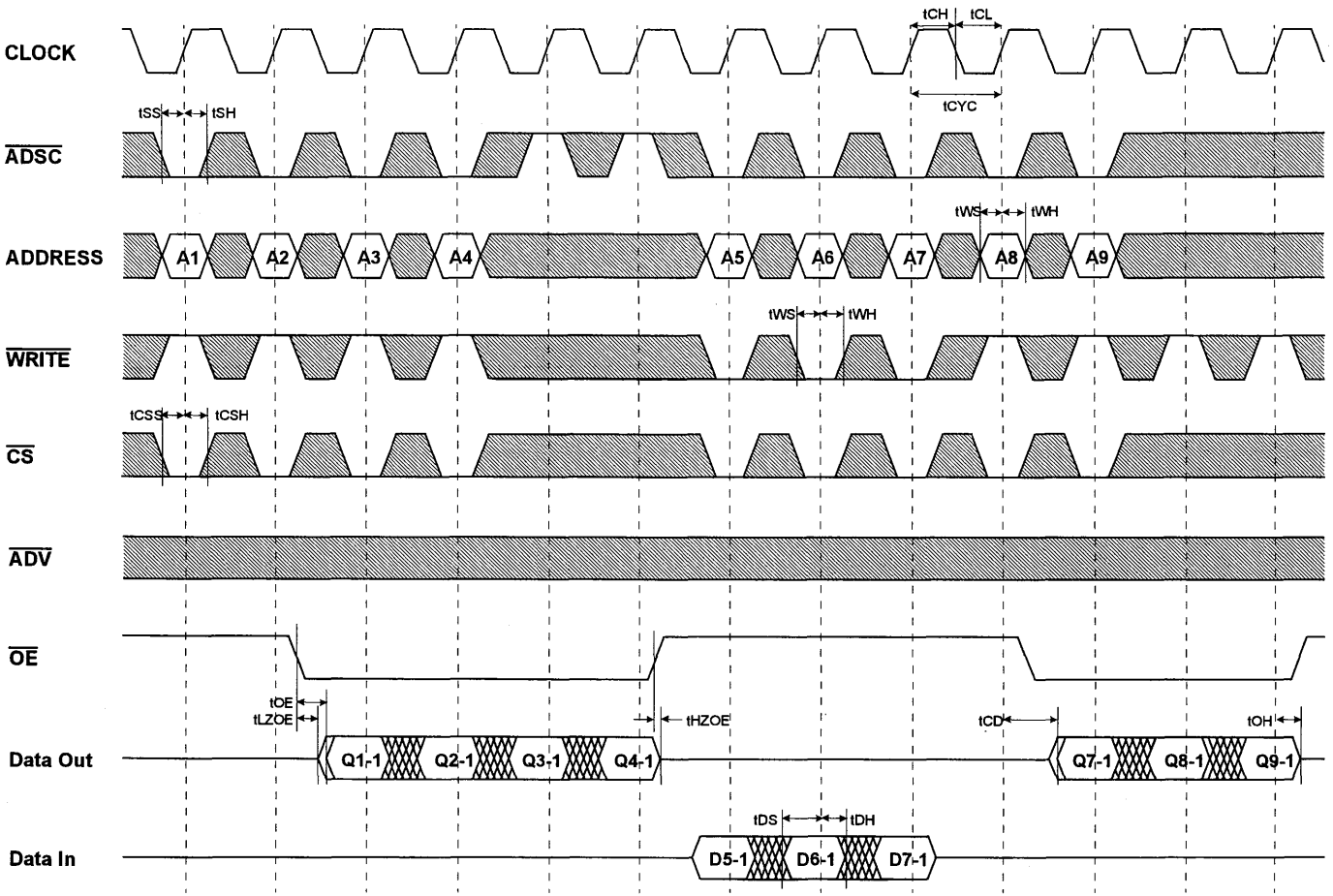
TIMING WAVEFORM OF WRTE CYCLE



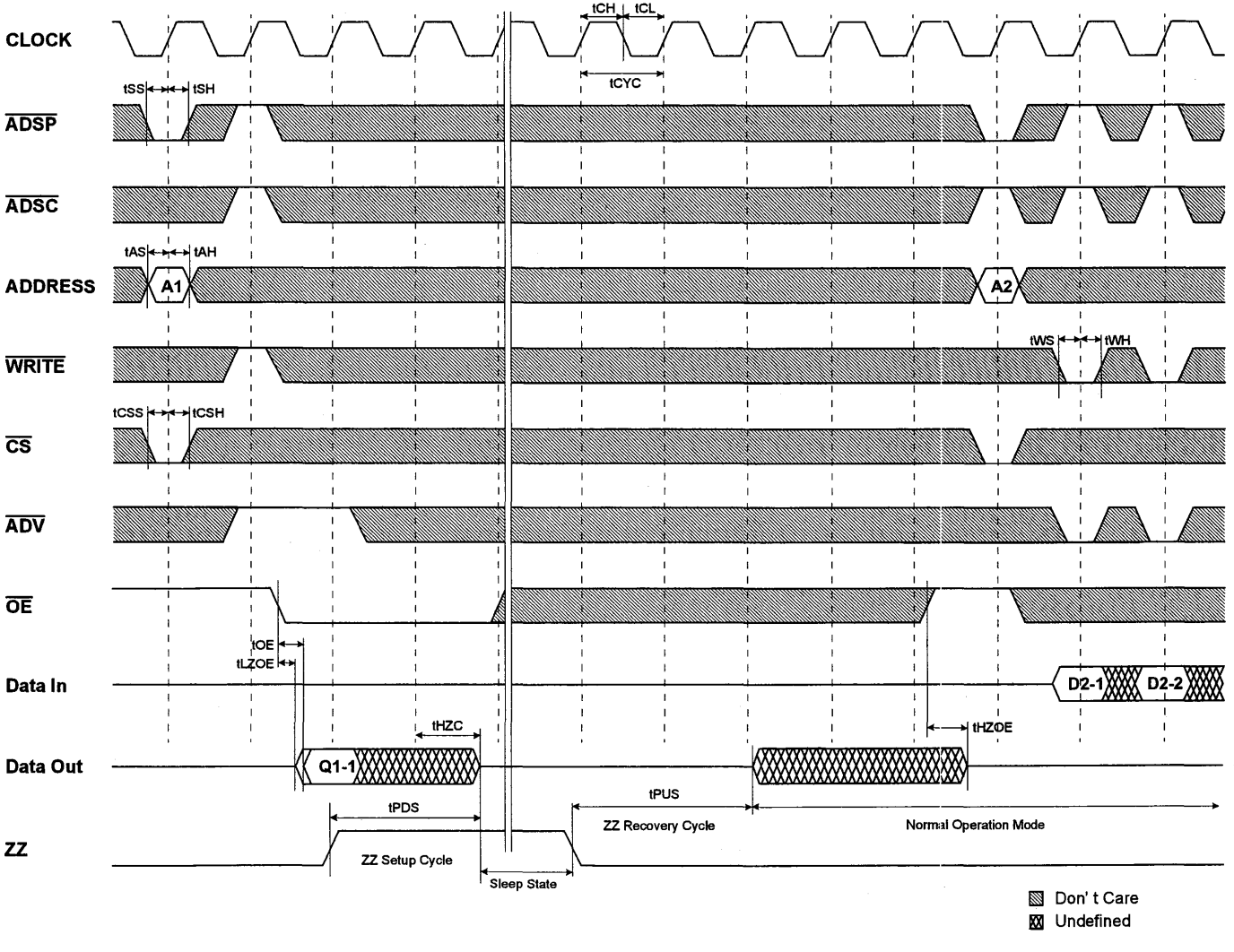
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



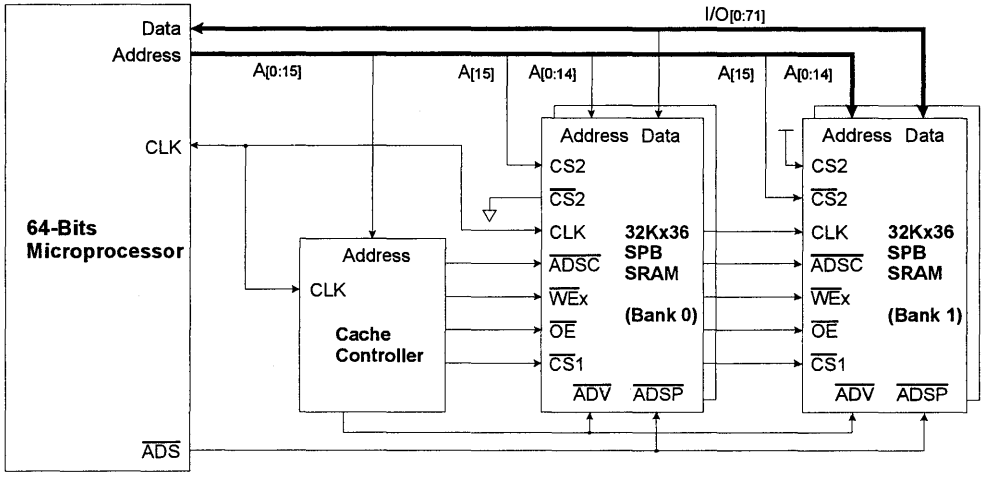
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

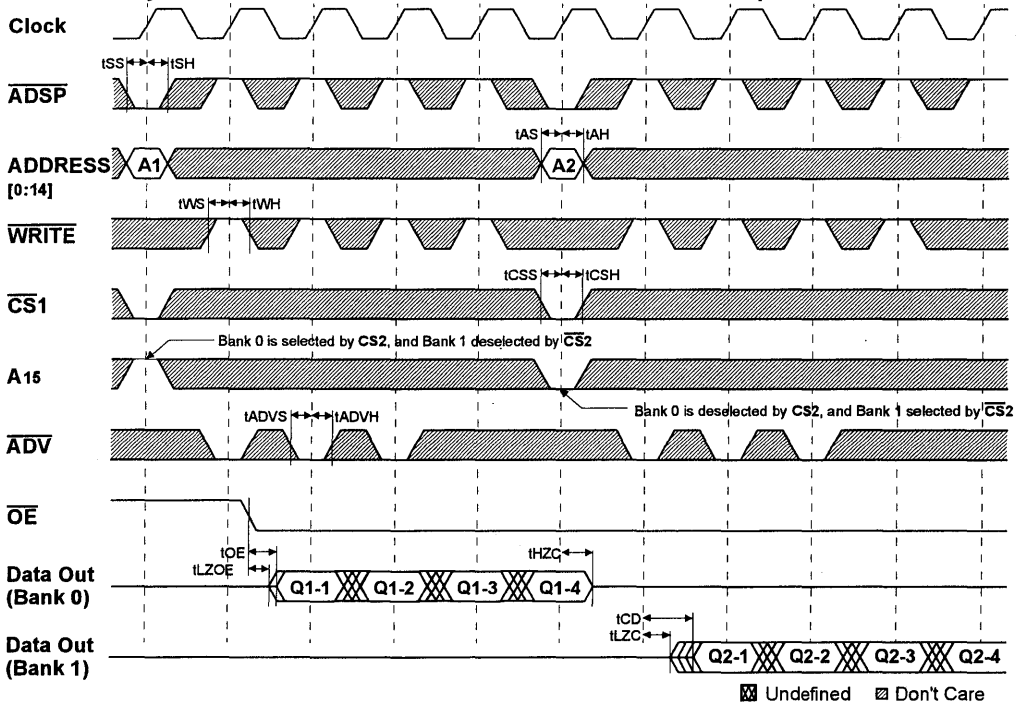
DEPTH EXPANSION

The Samsung 32Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.



SAMSUNG ELECTRONICS

64Kx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- On-Chip Address and Control Registers.
- Single 3.3± 5% Power Supply.
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention.
- TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	Unit
Cycle Time	tCYC	12	12	15	ns
Clock Access Time	tCD	8.5	9	10	ns
Output Enable Access Time	tOE	4	4	5	ns

GENERAL DESCRIPTION

The KM718V687 is a 1,179,648 bits Synchronous Static Random Access Memory designed to support zero wait state performance for advanced Pentium and Power PC based system. And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signal.

It is organized as 64K words of 18 bits. And it integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components counts implementation of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous.

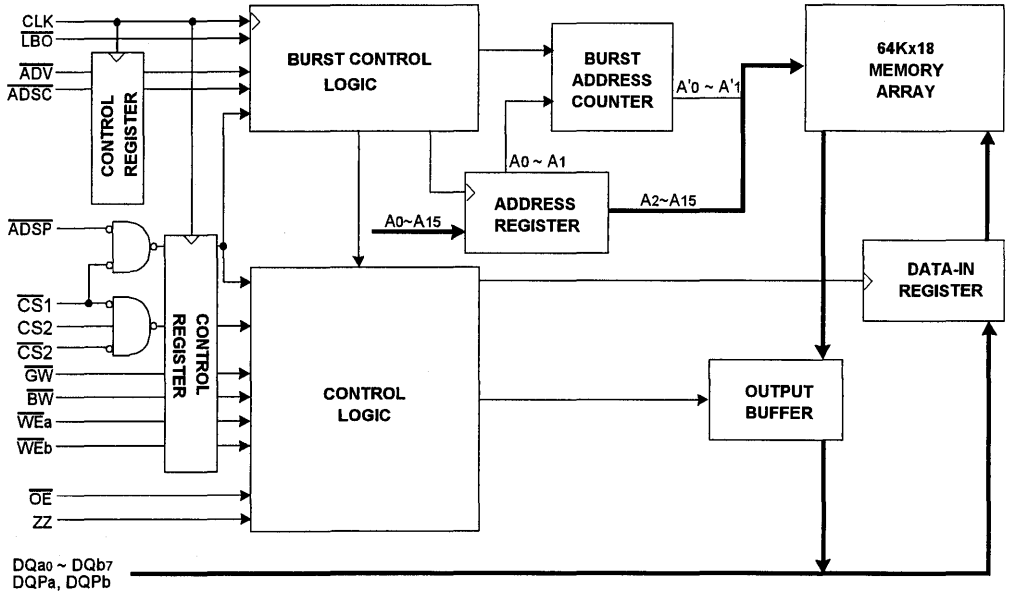
The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

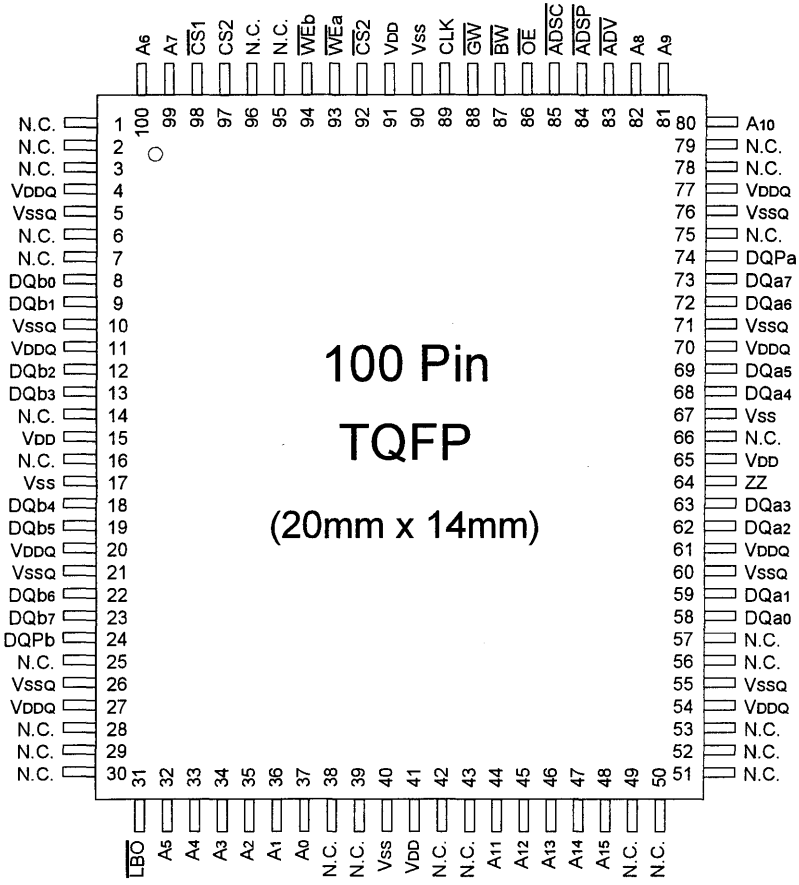
The KM718V687 is implemented with SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A15	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,80, 81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			Vss	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,14,16,25,28,29 ,30,38,39,42,43,49,50, 51,52,53,56,57,66,75, 78,79,95,96
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85			
CLK	Clock	89	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
$\overline{CS1}$	Chip Select	98	DQb0 ~ b7		8,9,12,13,18,19,22,23
CS2	Chip Select	97	DQPa, Pb		74,24
$\overline{CS2}$	Chip Select	92	VDDQ	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
$\overline{WEx}$	Byte Write Inputs	93,94			
$\overline{OE}$	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

SAMSUNG ELECTRONICS

FUNCTION DESCRIPTION

The KM718V687 is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs(with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges.
The start and duration of the burst access is controlled by $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ and Chip Select pins.

When ZZ is pulled HIGH, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to LOW, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and both $\overline{WE}$a and $\overline{WE}$b are high, When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$, the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$(or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.
All byte write occurs by enabling $\overline{GW}$(in dependent of $\overline{BW}$ and $\overline{WE}$x.), and individual byte write is performed only when $\overline{GW}$ is High and $\overline{BW}$ is Low. In KM718V687, A 64Kx18 organization, $\overline{WE}$a controls DQa0 ~ DQa7 and DQPa, $\overline{WE}$b controls DQb0 ~ DQb7 and DQPb.

$\overline{CS}$1 is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And when this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN: HIGH	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN: LOW	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	Operation
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.47	V
	V_{DDQ}	3.13	3.3	3.47	V
Ground	Vss	0	0	0	V

CAPACITANCE*(T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***NOTE** : Sampled not 100% tested.

TEST CONDITIONS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%, unless otherwise specified)

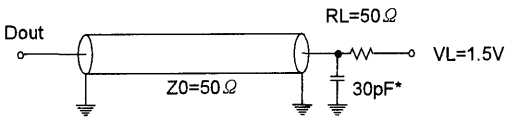
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%)

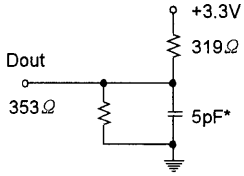
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Max , V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	8ns	-	330	mA
			9ns	-	330	
			10ns	-	300	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL},f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	8ns	-	80	mA
			9ns	-	80	
			10ns	-	60	
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs = fixed (V_{DD}-0.2V or 0.2V)		-	10	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.2	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

Output Load(A)



Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance **Fig. 1**

2

AC TIMING CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%)

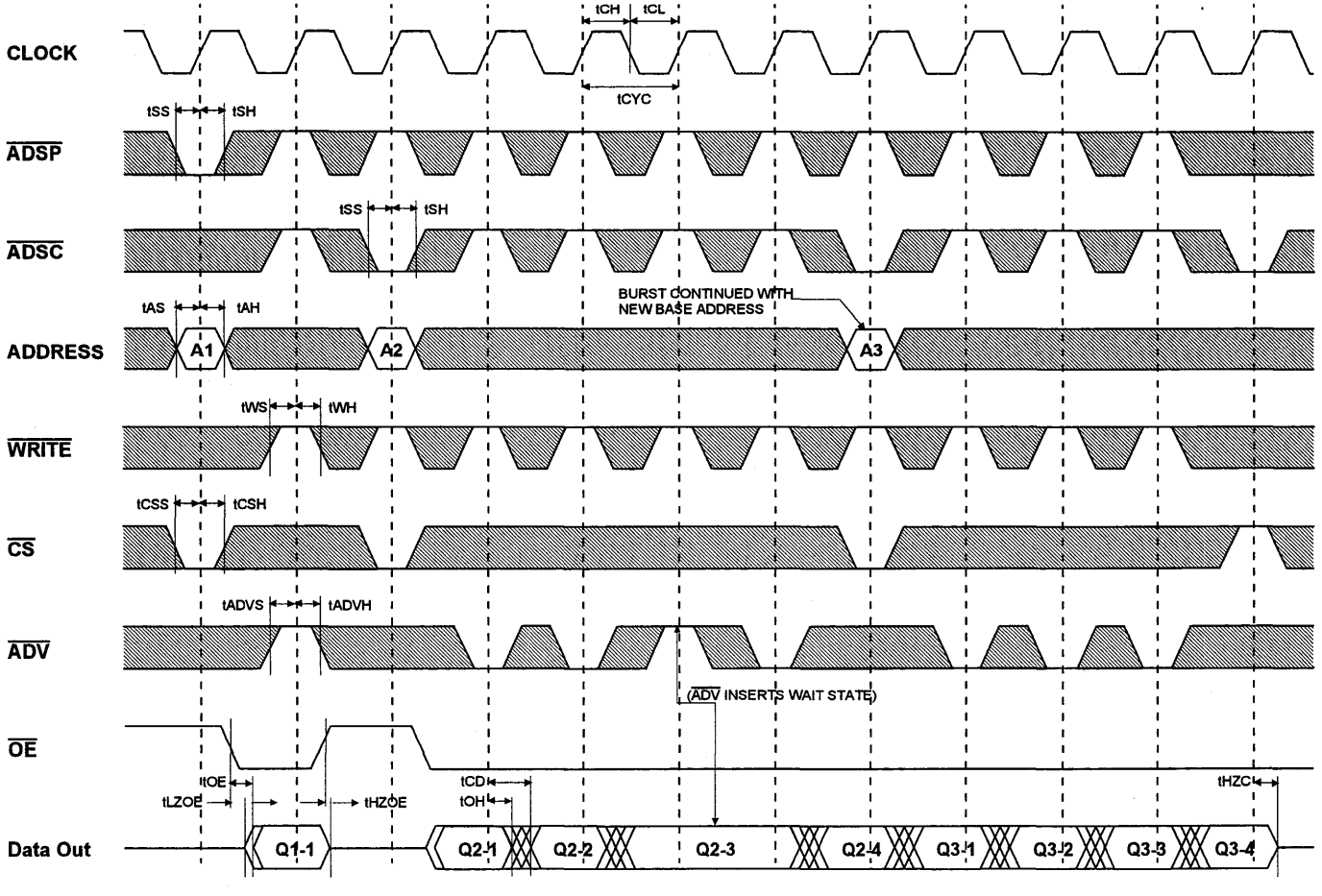
Parameter	Symbol	KM718V687-8		KM718V687-9		KM718V687-10		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	12	-	12	-	15	-	ns
Clock Access Time	tCD	-	8.5	-	9	-	10	ns
Output Enable to Data Valid	tOE	-	4	-	4	-	5	ns
Clock High to Output Low-Z	tLZC	4	-	4	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	5	-	5	-	6	ns
Clock High Pulse Width	tCH	4	-	4	-	5	-	ns
Clock Low Pulse Width	tCL	4	-	4	-	5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	ns
Address/Advance Setup to Clock High	tADVS	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

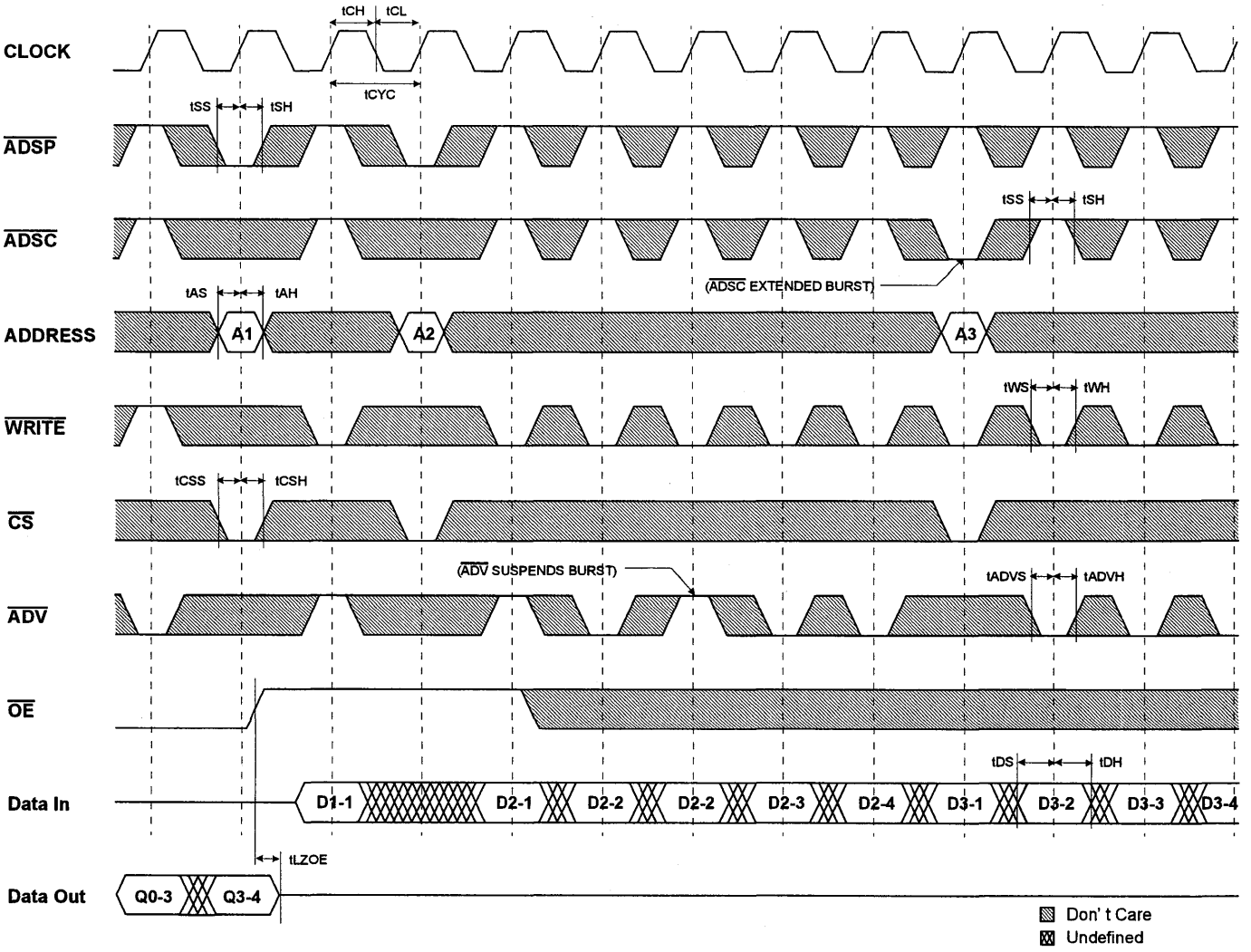
TIMING WAVEFORM OF READ CYCLE



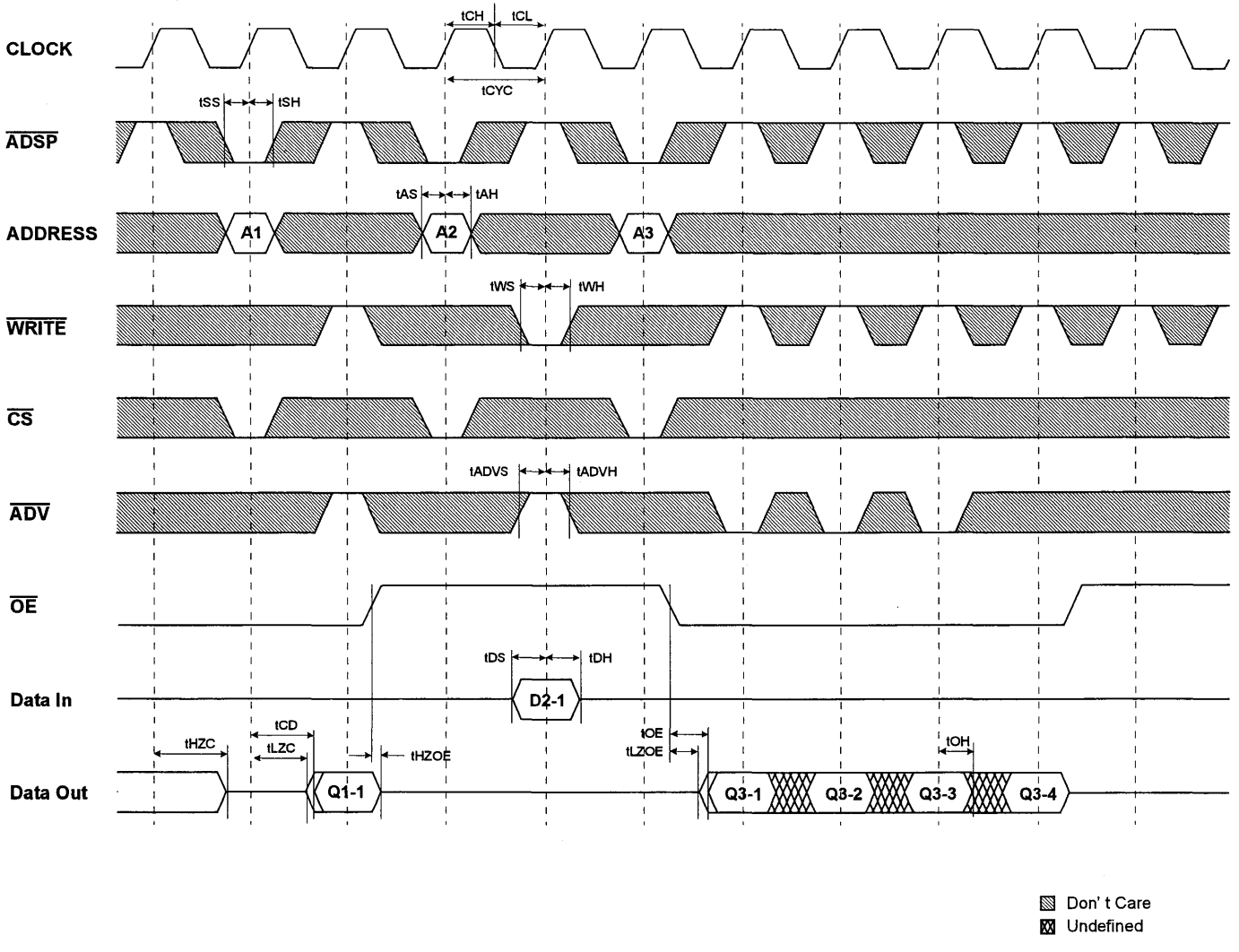
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}$x.= L
$\overline{CS}$ = L means $\overline{CS1}$ = L, CS2 = H and $\overline{CS2}$ = L
$\overline{CS}$ = H means $\overline{CS1}$ = H, or $\overline{CS1}$ = L and $\overline{CS2}$ = H, or $\overline{CS1}$ = L, and CS2 = L

▨ Don' t Care
▩ Undefined

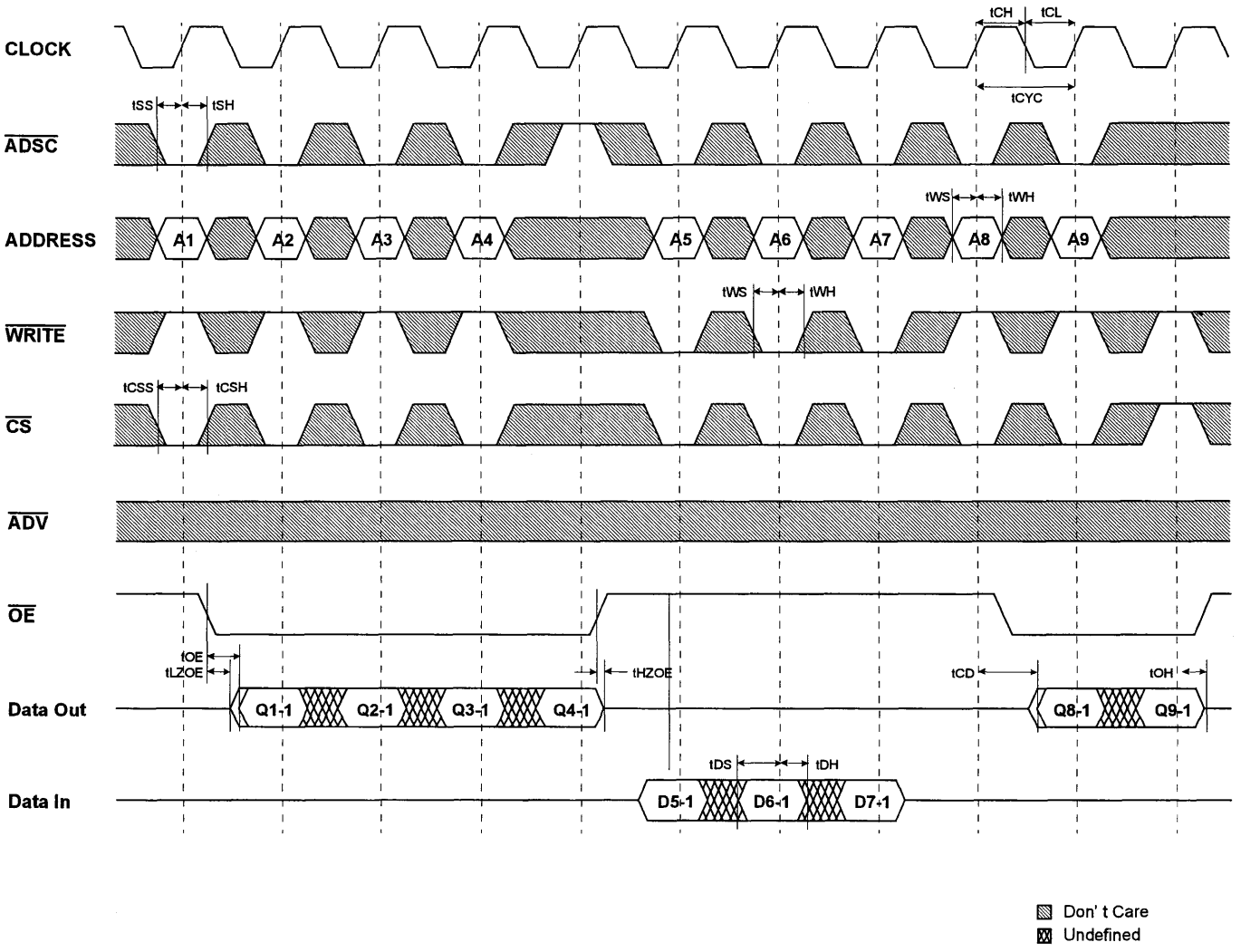
TIMING WAVEFORM OF WRTE CYCLE



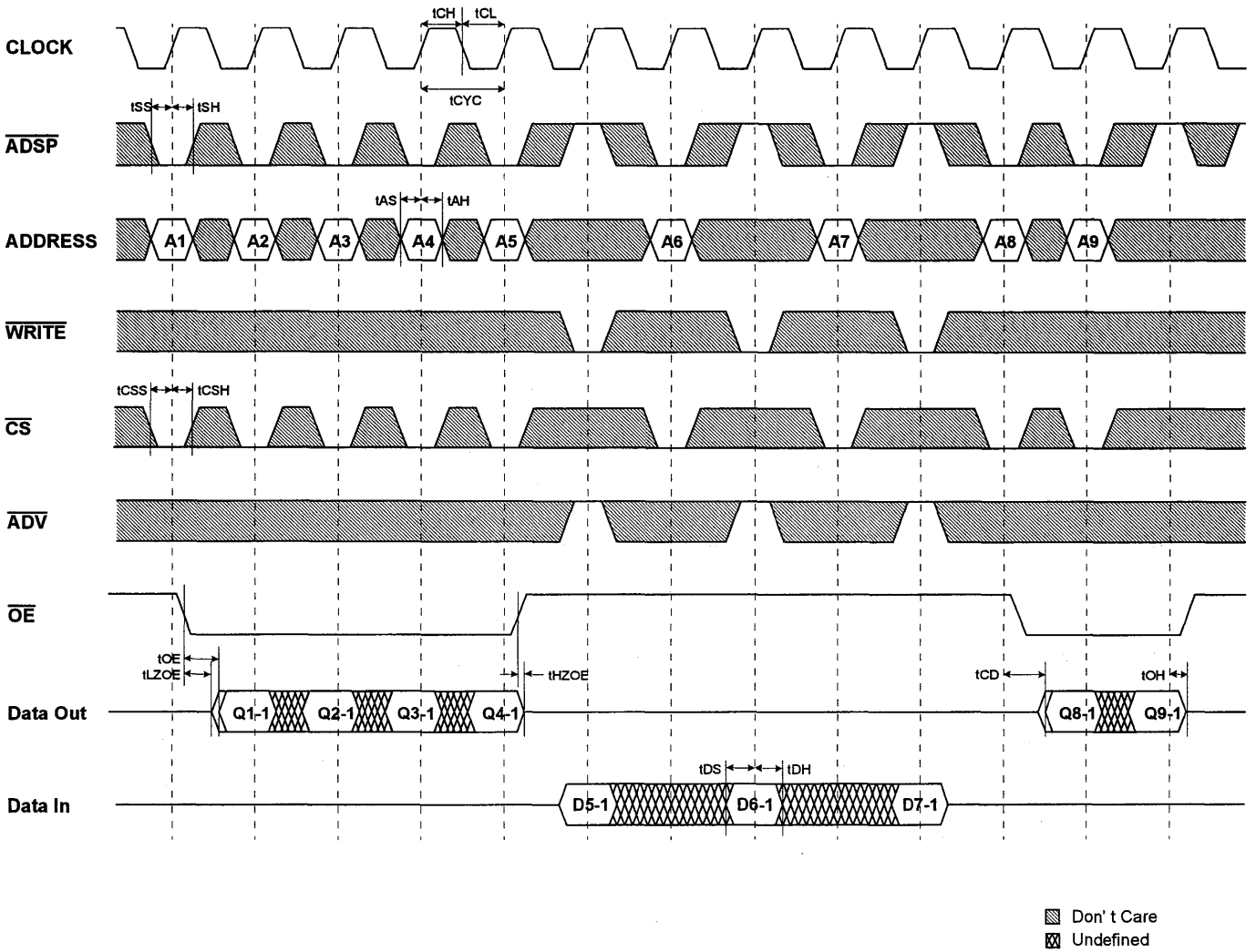
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



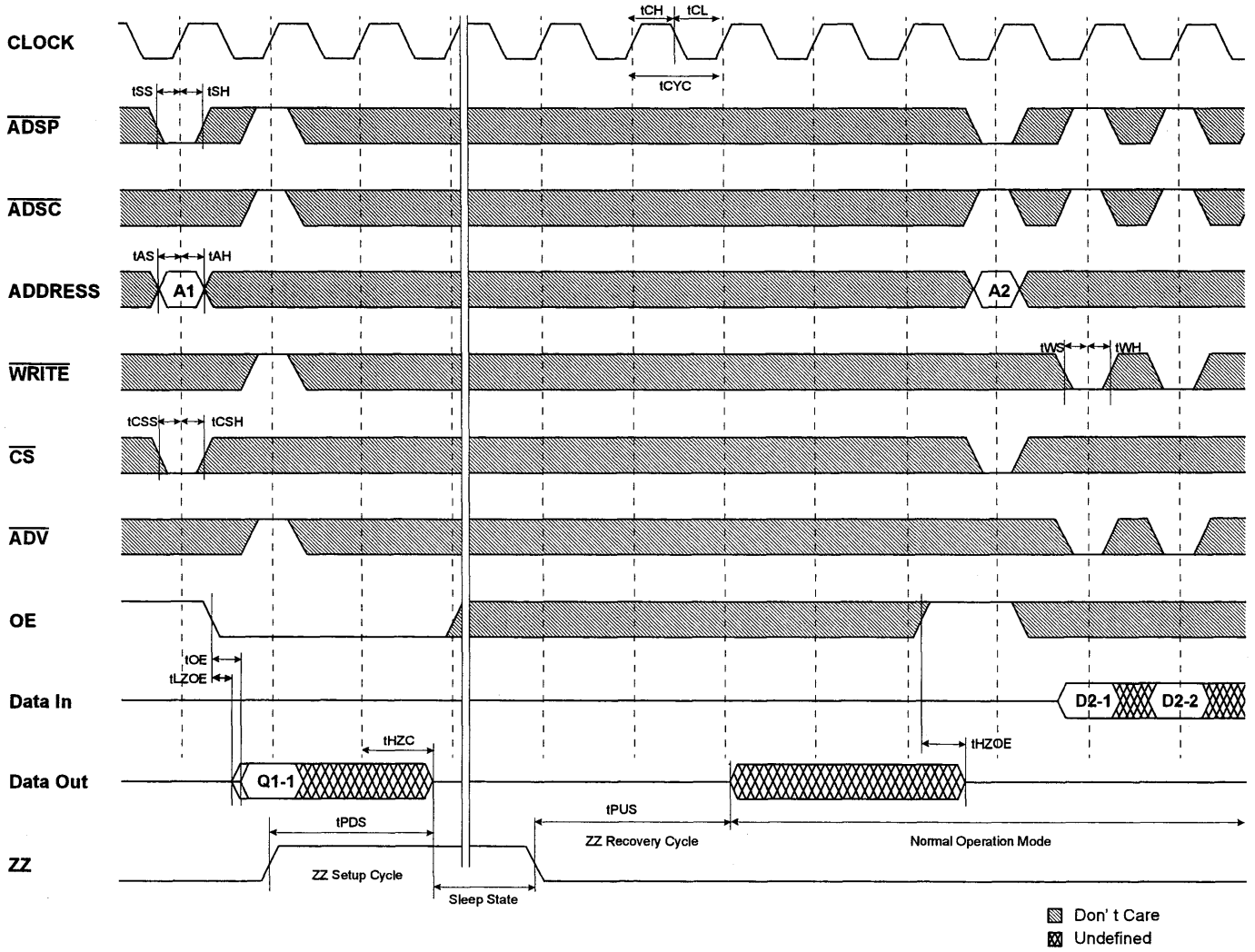
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ CONTROLLED, $\overline{ADSP}$=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



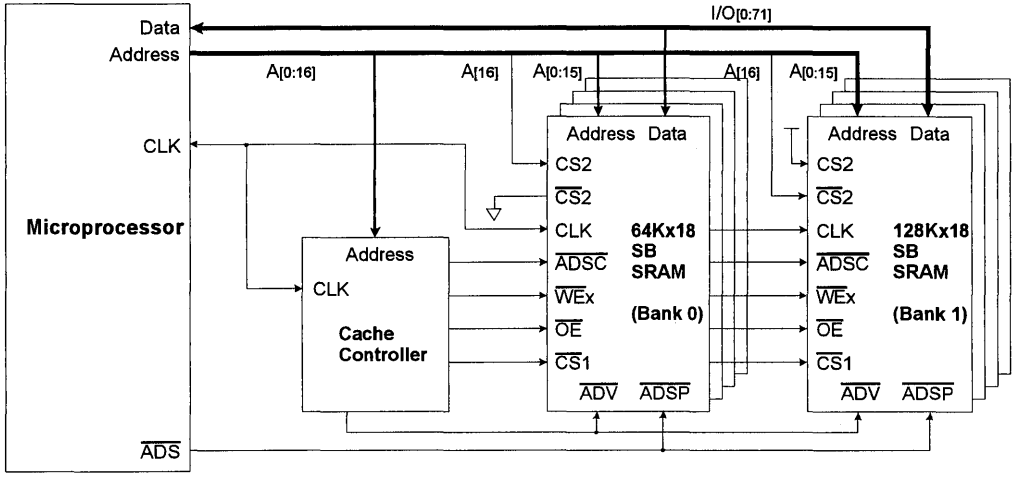
TIMING WAVEFORM OF POWER DOWN CYCLE



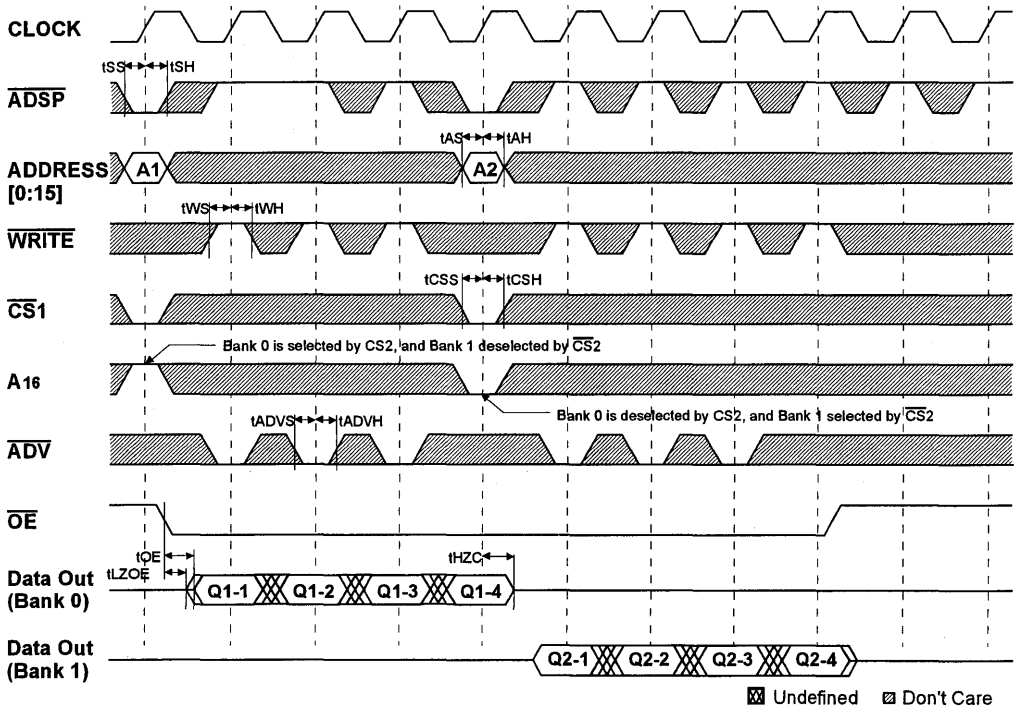
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 64Kx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)



SAMSUNG ELECTRONICS

32Kx36-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- On-Chip Address and Control Registers.
- Single 3.3V ± 5% Power Supply.
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention.
- TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	Unit
Cycle Time	tCYC	12	12	15	ns
Clock Access Time	tCD	8.5	9	10	ns
Output Enable Access Time	tOE	4	4	5	ns

GENERAL DESCRIPTION

The KM736V587 is 1,179,648 bits Synchronous Static Random Access Memory designed to support zero wait state performance for advanced Pentium/Power PC based system. And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signals.

It can be organized as 32K words of 36 bits. And it integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components counts implementation of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous.

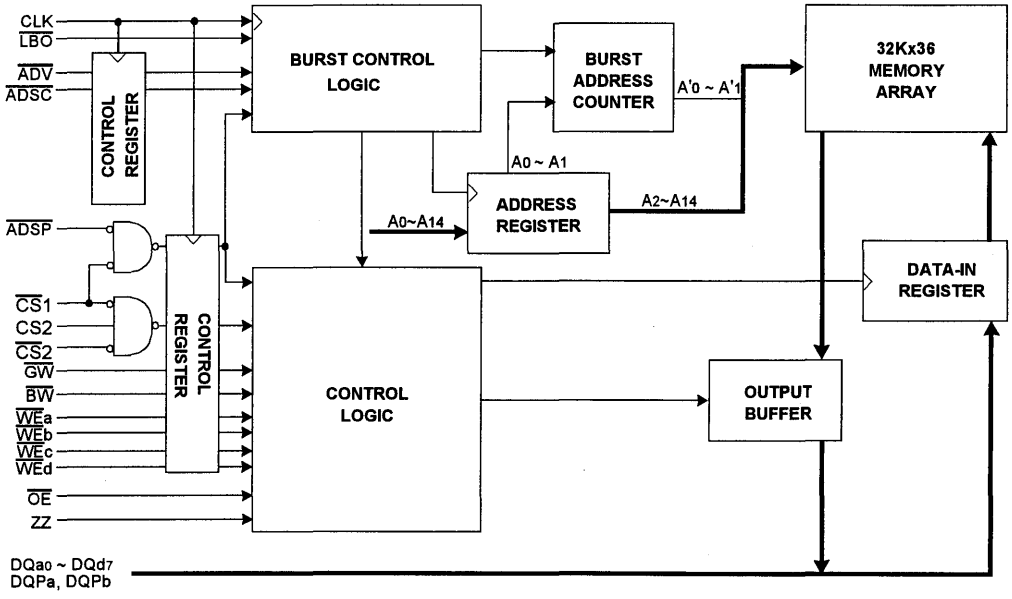
The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

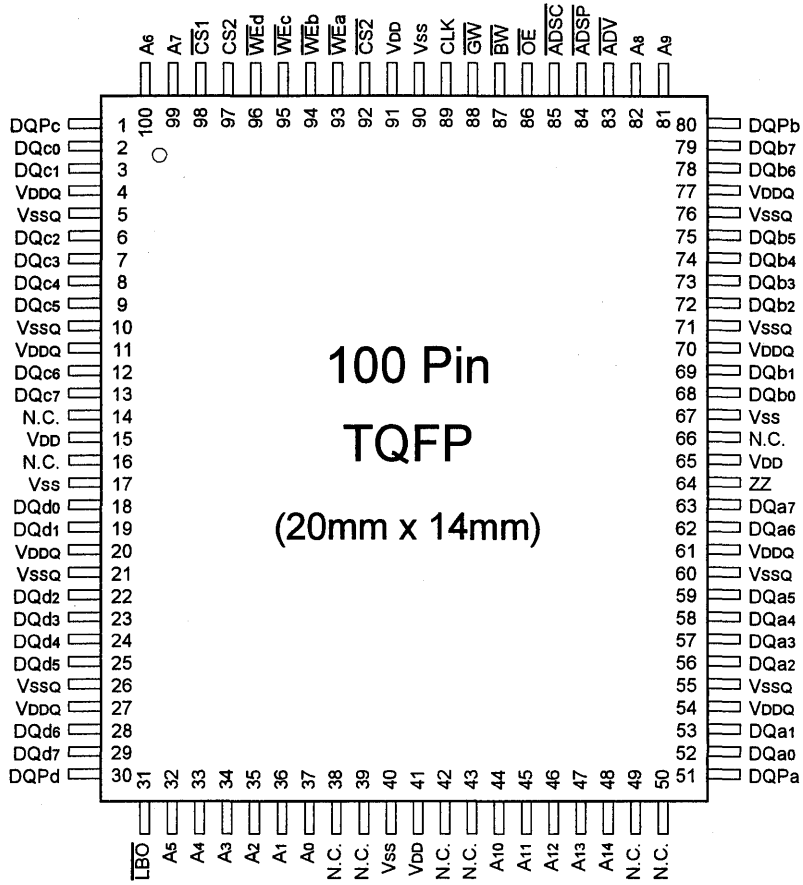
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The KM736V587 is implemented with SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A14	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,81, 82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			Vss	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,43,49,50, 66
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa ~ Pd		51,80,1,30
$\overline{CS2}$	Chip Select	92			
$\overline{WEx}$	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88	VssQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

SAMSUNG ELECTRONICS

FUNCTION DESCRIPTION

The KM736V587 is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c, and $\overline{WE}$d are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$(or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.
All byte write occurs by enabling $\overline{GW}$(independent of $\overline{BW}$ and $\overline{WE}$x.), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In KM736V587, a 32Kx36 organization, $\overline{WE}$a controls DQa0 ~ DQa7 and DQPa, $\overline{WE}$b controls DQb0 ~ DQb7 and DQPb, $\overline{WE}$c controls DQc0 ~ DQc7 and DQPc and $\overline{WE}$d controls DQd0 ~ DQd7 and DQPd.

$\overline{CS1}$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN: HIGH	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN: LOW	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	1	0	1	1	0	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.47	V
	V_{DDQ}	3.13	3.3	3.47	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***NOTE** : Sampled not 100% tested.

TEST CONDITIONS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%, unless otherwise specified)

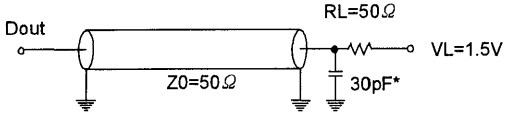
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Max , V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	-8	-	330	mA
			-9	-	330	
			-10	-	300	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-8	-	80	mA
			-9	-	80	
			-10	-	60	
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs = fixed (V_{DD}-0.2V or 0.2V)		-	10	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.2	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

Output Load(A)



* Including Scope and Jig Capacitance

Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)

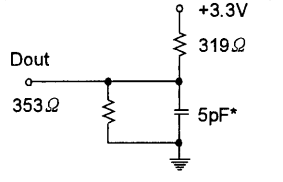


Fig. 1

SAMSUNG ELECTRONICS

AC TIMING CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%)

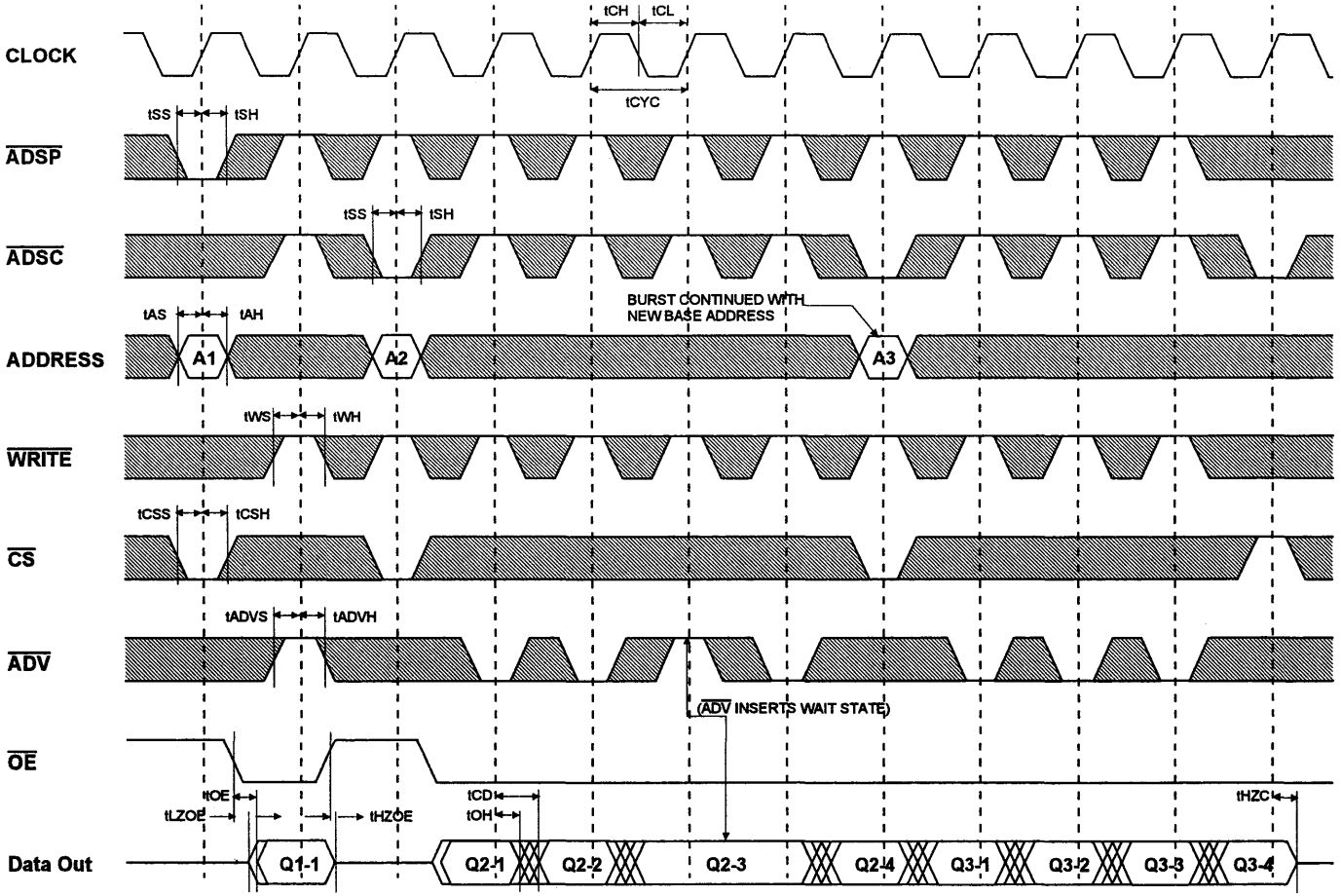
Parameter	Symbol	KM736V587-8		KM736V587-9		KM736V587-10		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	12	-	12	-	15	-	ns
Clock Access Time	tCD	-	8.5	-	9	-	10	ns
Output Enable to Data Valid	tOE	-	4	-	4	-	5	ns
Clock High to Output Low-Z	tLZC	4	-	4	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	5	-	5	-	6	ns
Clock High Pulse Width	tCH	4	-	4	-	5	-	ns
Clock Low Pulse Width	tCL	4	-	4	-	5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	ns
Address/Advance Setup to Clock High	tADVS	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

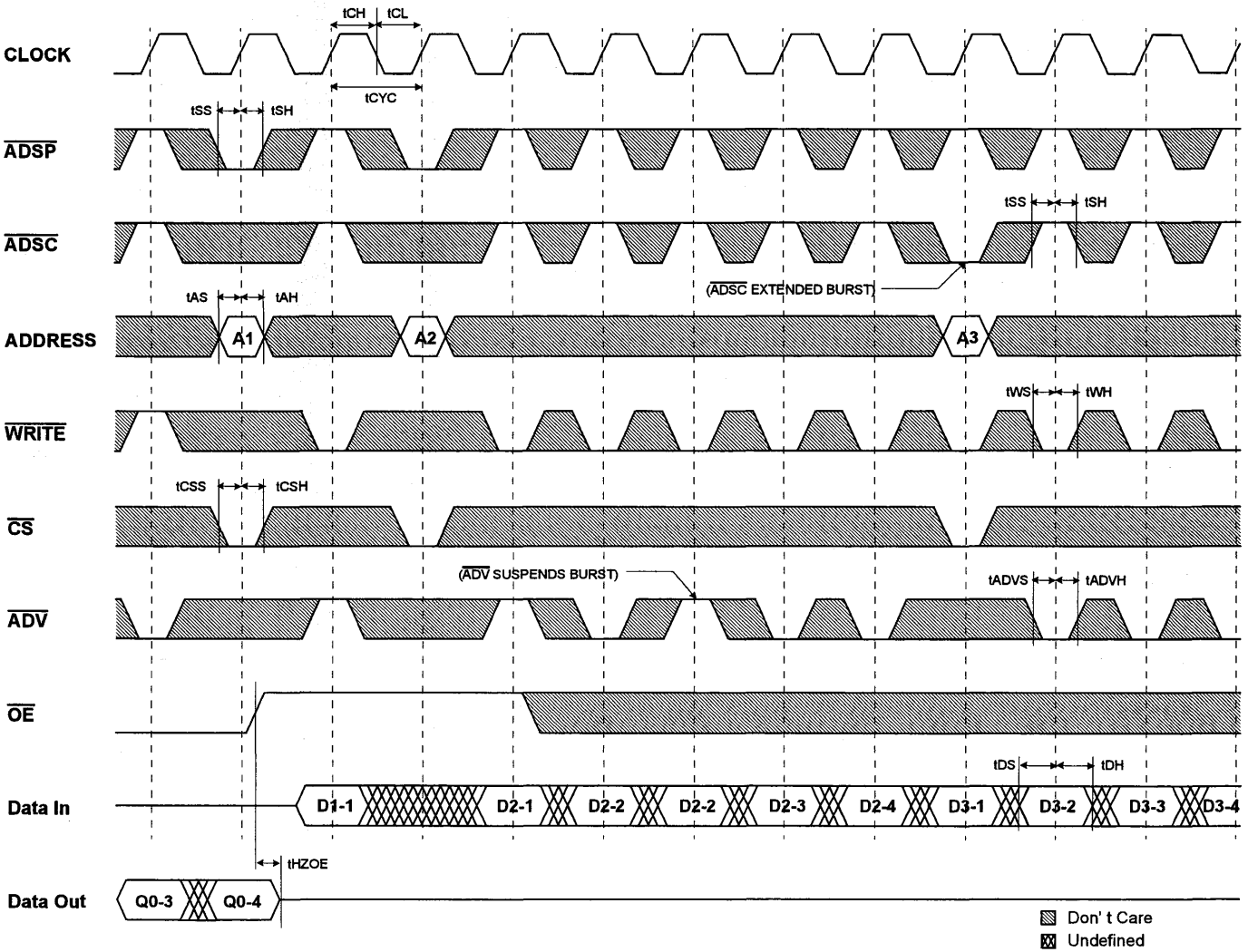
TIMING WAVEFORM OF READ CYCLE



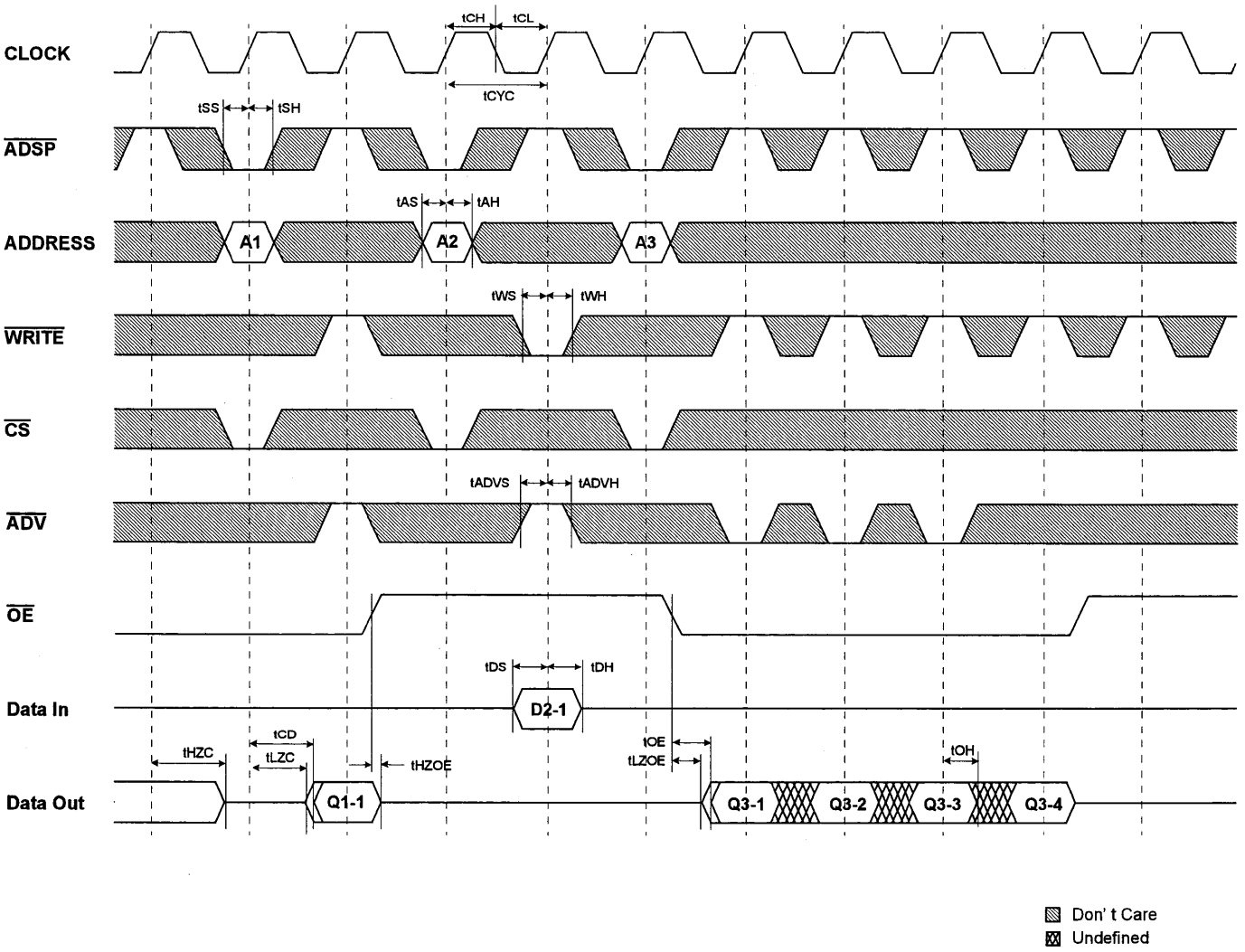
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}$x.= L
$\overline{CS}$ = L means $\overline{CS}1$ = L, CS2 = H and $\overline{CS}2$ = L
$\overline{CS}$ = H means $\overline{CS}1$ = H, or $\overline{CS}1$ = L and $\overline{CS}2$ = H, or $\overline{CS}1$ = L, and CS2 = L

▨ Don' t Care
▩ Undefined

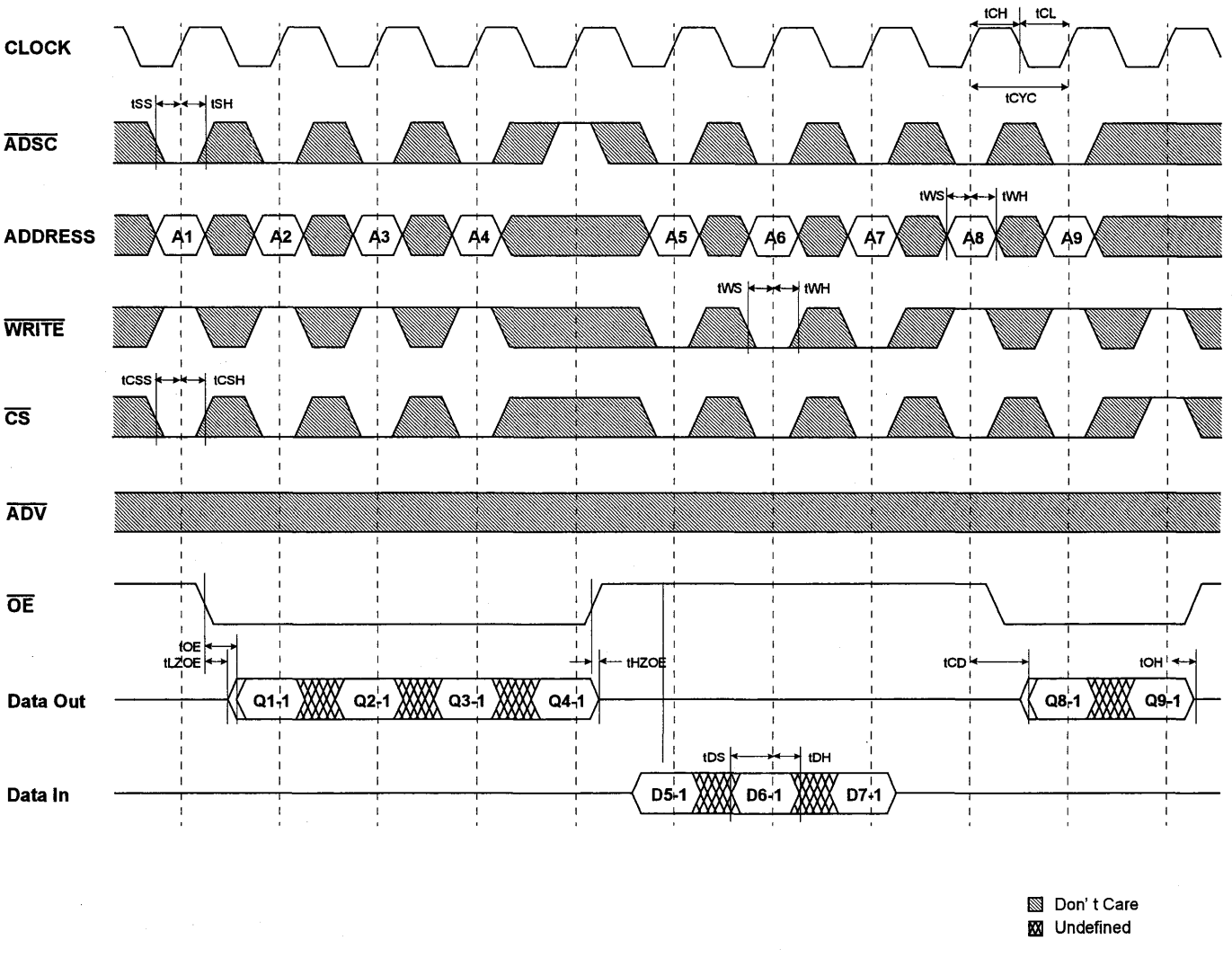
TIMING WAVEFORM OF WRTE CYCLE



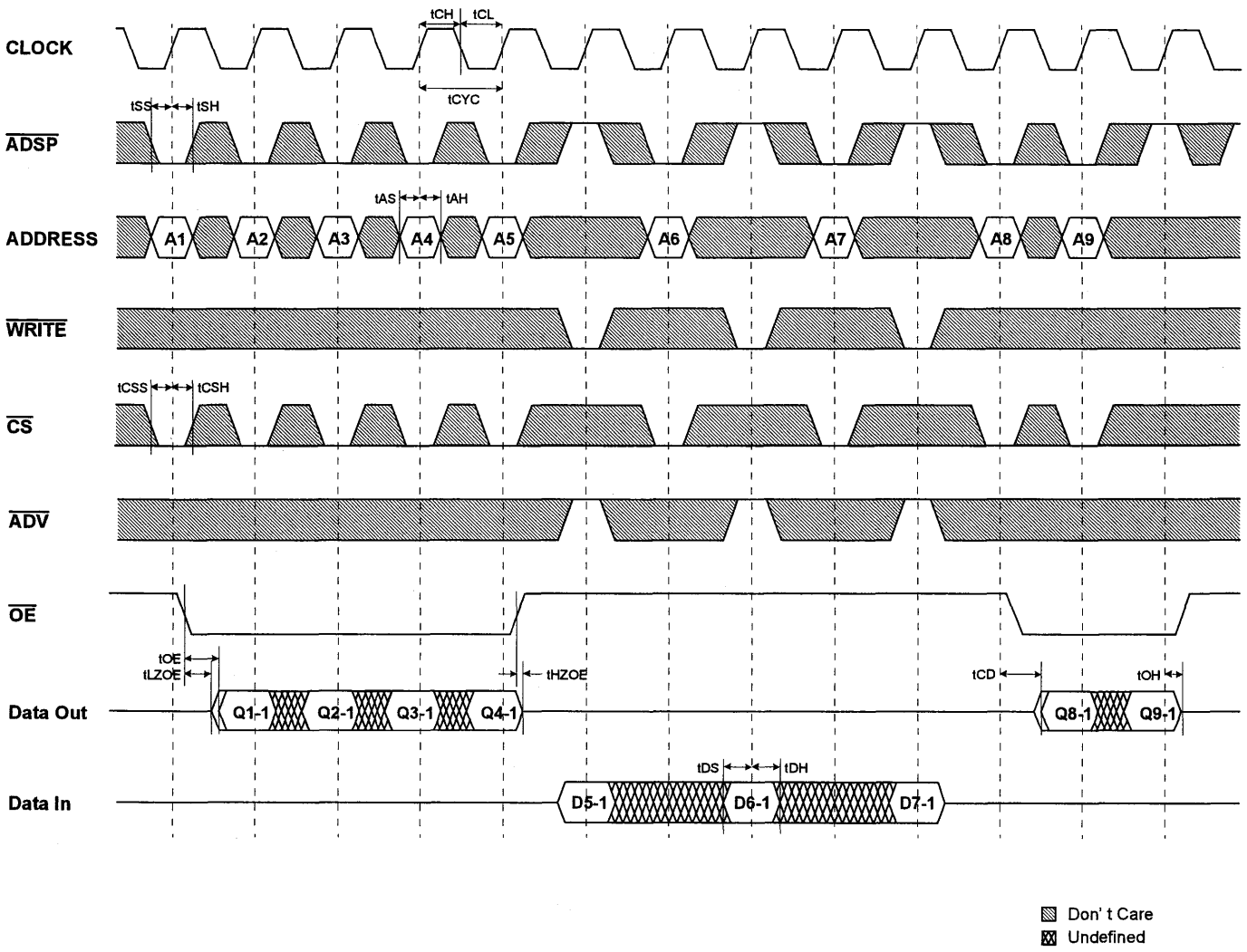
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



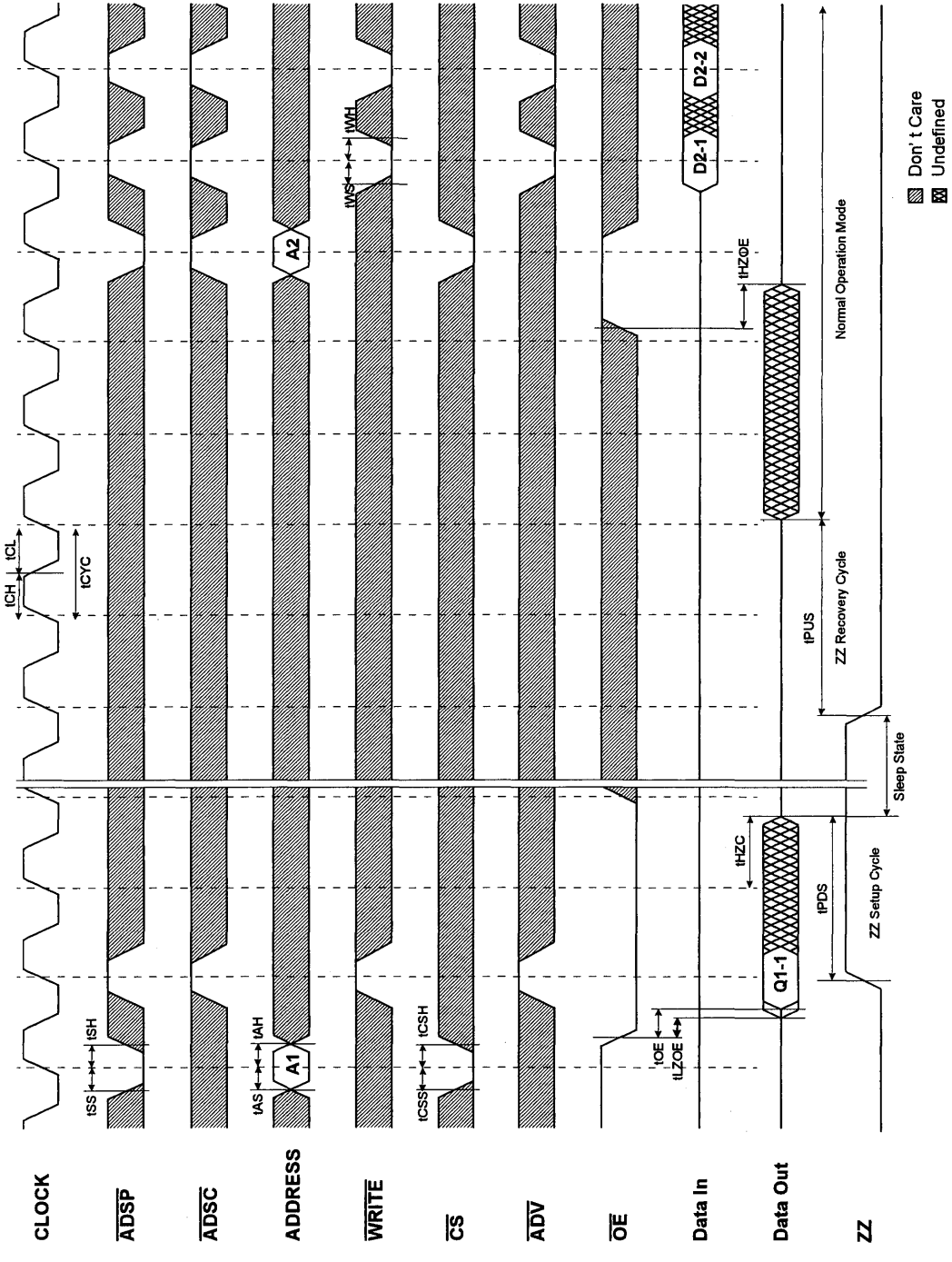
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ CONTROLLED, $\overline{ADSP}$=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



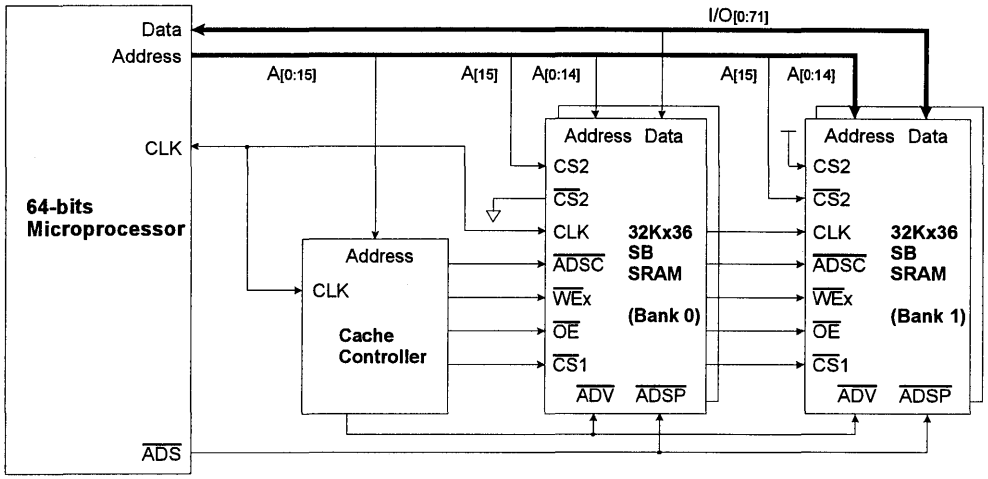
TIMING WAVEFORM OF POWER DOWN CYCLE



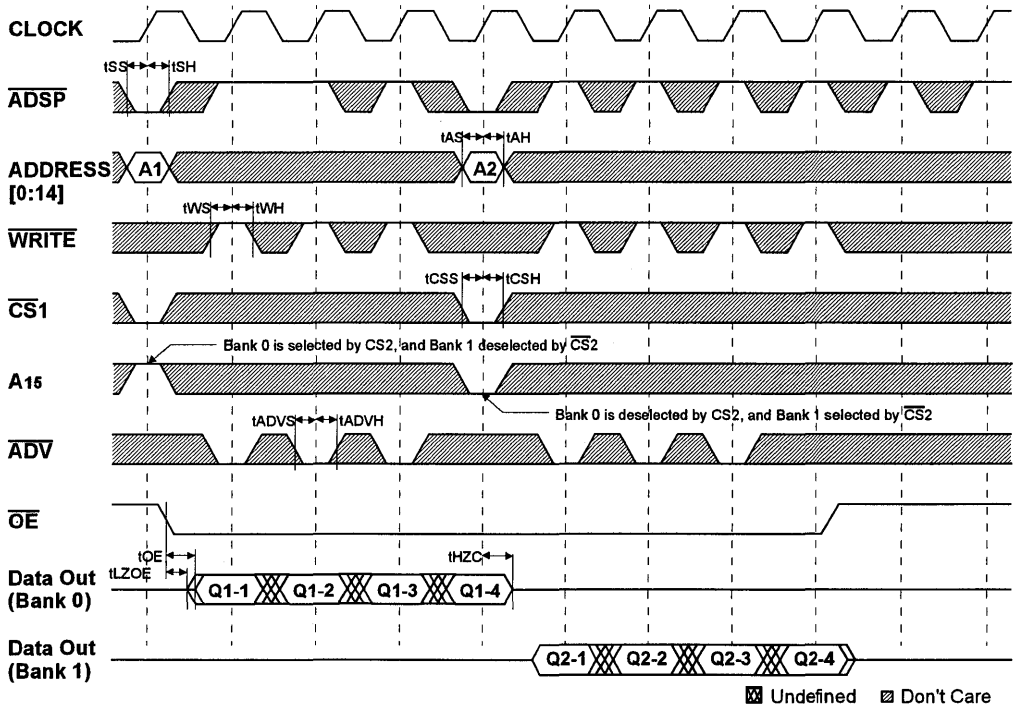
APPLICATION INFORMATION

DEPTH EXPANSION

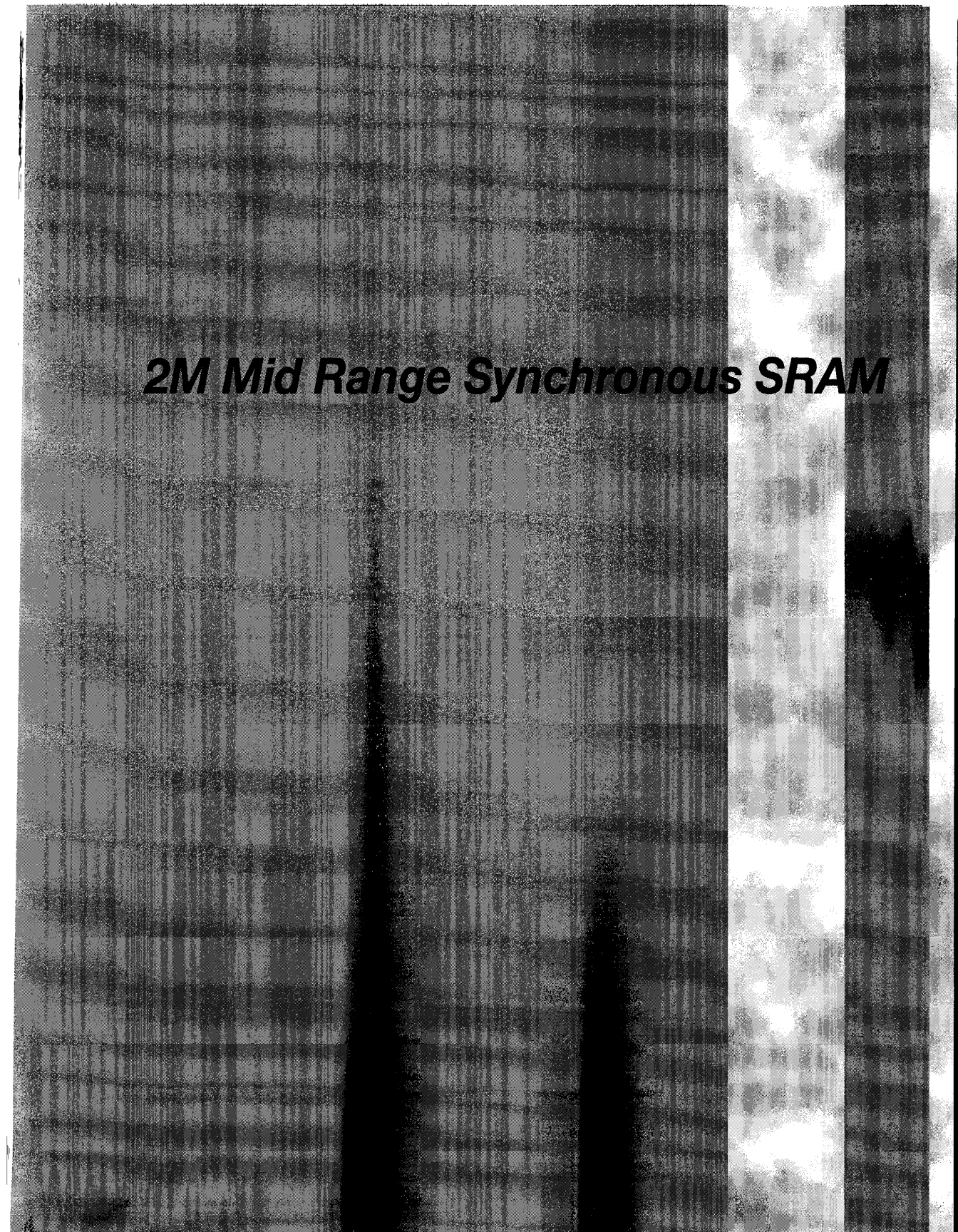
The Samsung 32Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 32K depth to 64K depth without extra logic.



INTERLEAVE READ TIMING (Refer non-interleave write timing for interleave write timing)



SAMSUNG ELECTRONICS


2M Mid Range Synchronous SRAM

64Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- V_{DD}=3.3V-5%/+10% Power Supply
- I/O Supply Voltage : 3.3V-5%/+10%
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- TTL-Level Three-State Output.
- 100-Pin QFP/TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	Unit
Cycle Time	tCYC	13	15	ns
Clock Access Time	tCD	7	8	ns
Output Enable Access Time	tOE	6	7	ns

GENERAL DESCRIPTION

The KM732V688/L is a 2,097,152 bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 64K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signals.

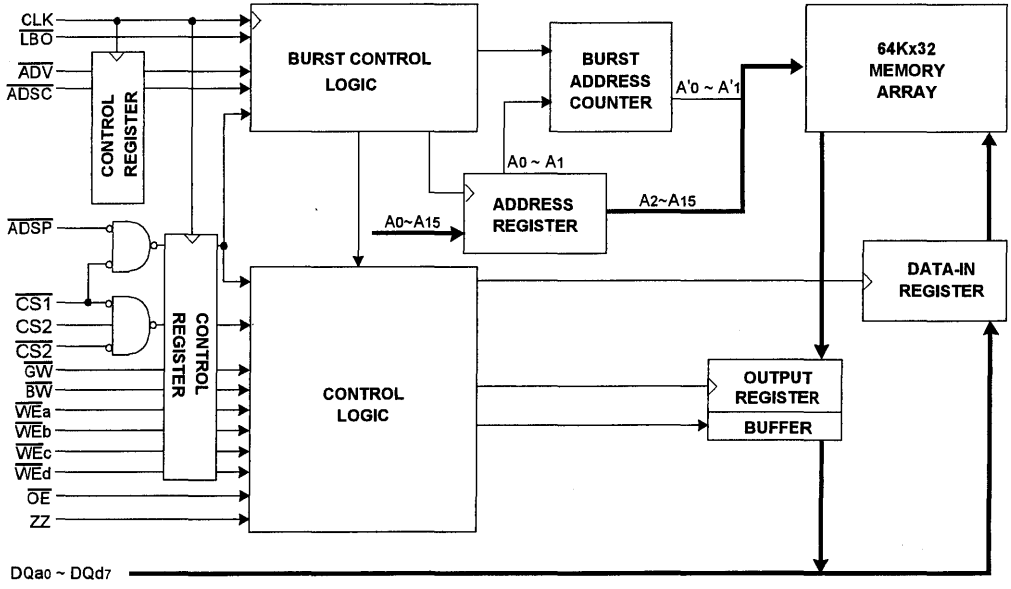
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

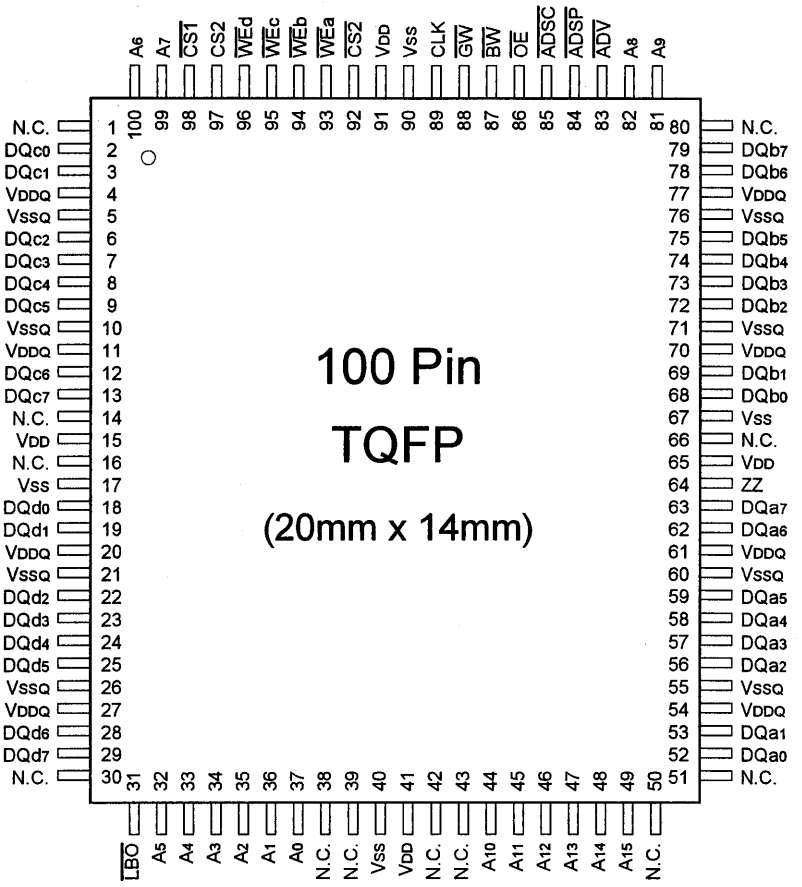
The KM732V688/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin QFP/TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A15	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,49, 81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,14,16,30,38,39,42,43, 50,51,66,80
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	VDDQ	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
$\overline{CS2}$	Chip Select	92			
$\overline{WEx}$	Byte Write Inputs	93,94,95,96	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM732V688/L is a synchronous SRAM designed to support the burst address accessing sequence of the CISC and RISC microprocessor. All inputs(with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled High and $\overline{ADV}$ is sampled Low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS}$1.

All byte write is done by $\overline{GW}$(regardless of $\overline{BW}$ and $\overline{WE}$x.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x when $\overline{GW}$ is High.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ Low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled Low(regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled Low. The address increases internally to the next address of burst, if both $\overline{WE}$x and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$b) sampled low. The $\overline{WE}$a controls $DQa_0 \sim DQa_7$, $\overline{WE}$b controls $DQb_0 \sim DQb_7$, $\overline{WE}$c control $DQc_0 \sim DQc_7$, and $\overline{WE}$d controls $DQd_0 \sim DQd_7$. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
$\overline{WE}$x are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WRITE}$	Operation	$\overline{CS1}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
	V_{DDQ}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(V_{DD}=3.3V-5%/+10%, V_{DDQ}=3.3V-5%/+10%, T_A = 0℃ to 70℃)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Vss to V_{DD}, V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA,	-13	-	250	mA
		ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH}	-15	-	220	
		Cycle Time ≥ tCYC min				
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V		-	60	mA
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs = fixed(V_{DD}-0.2V or 0.2V)		-	10	mA
			L-Ver.	-	2.0	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	10	mA
			L-Ver.	-	1	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.0	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)

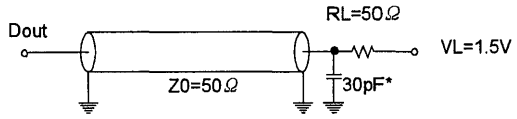
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

TEST CONDITIONS

(T_A = 0℃ to 70℃, V_{DD}=3.3V-5%/+10%, V_{DDQ}=3.3V-5%/+10%, unless otherwise specified)

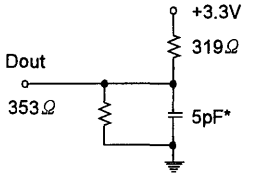
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)



* Capacitive Load consists of all components of the test environment.

Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

(V_{DD}=3.3V-5%/+10%, T_A = 0℃ to 70℃)

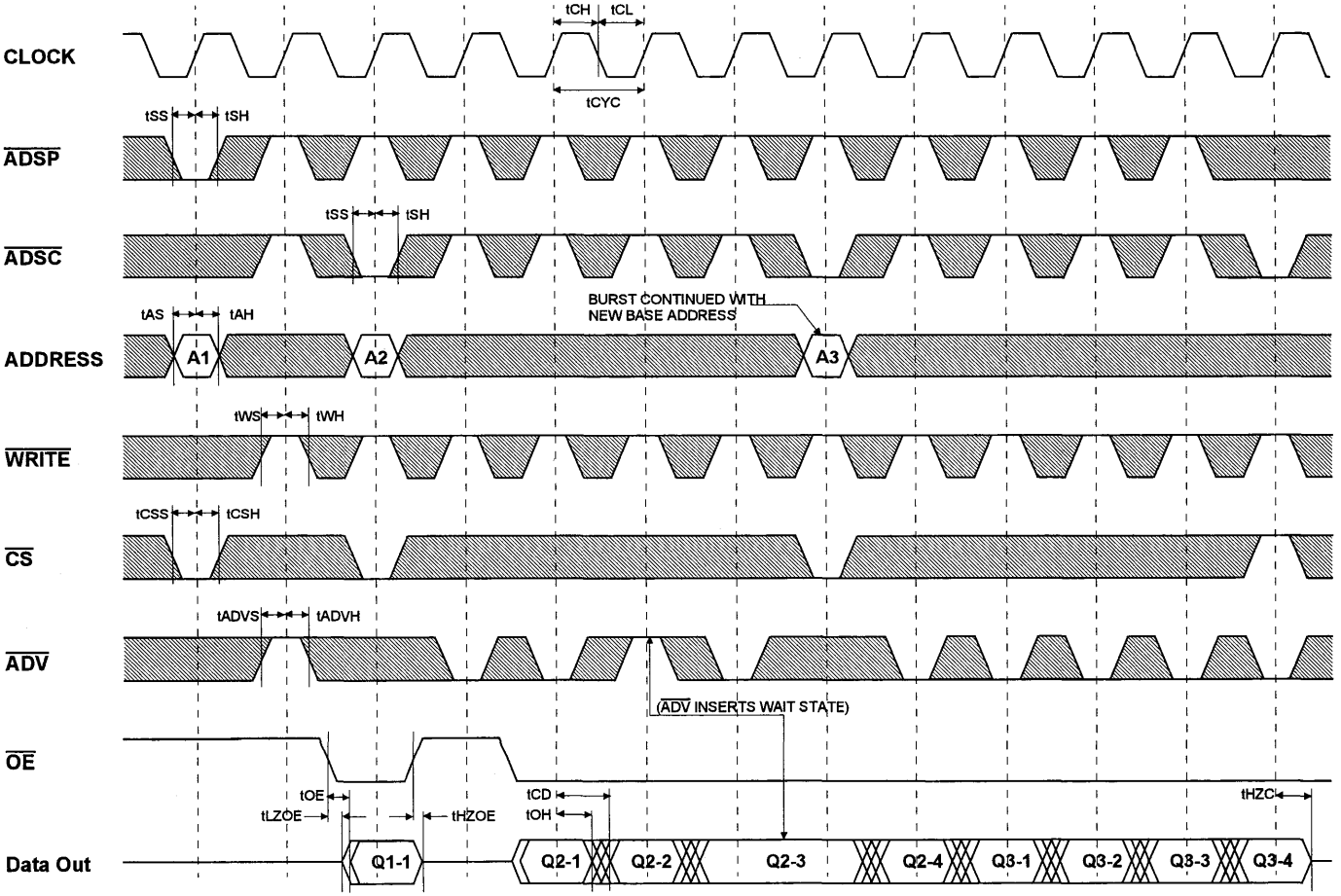
Parameter	Symbol	KM732V688-13		KM732V688-15		Unit
		Min	Max	Min	Max	
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	8	ns
Output Enable to Data Valid	tOE	-	6	-	7	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	2.0	-	2.0	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

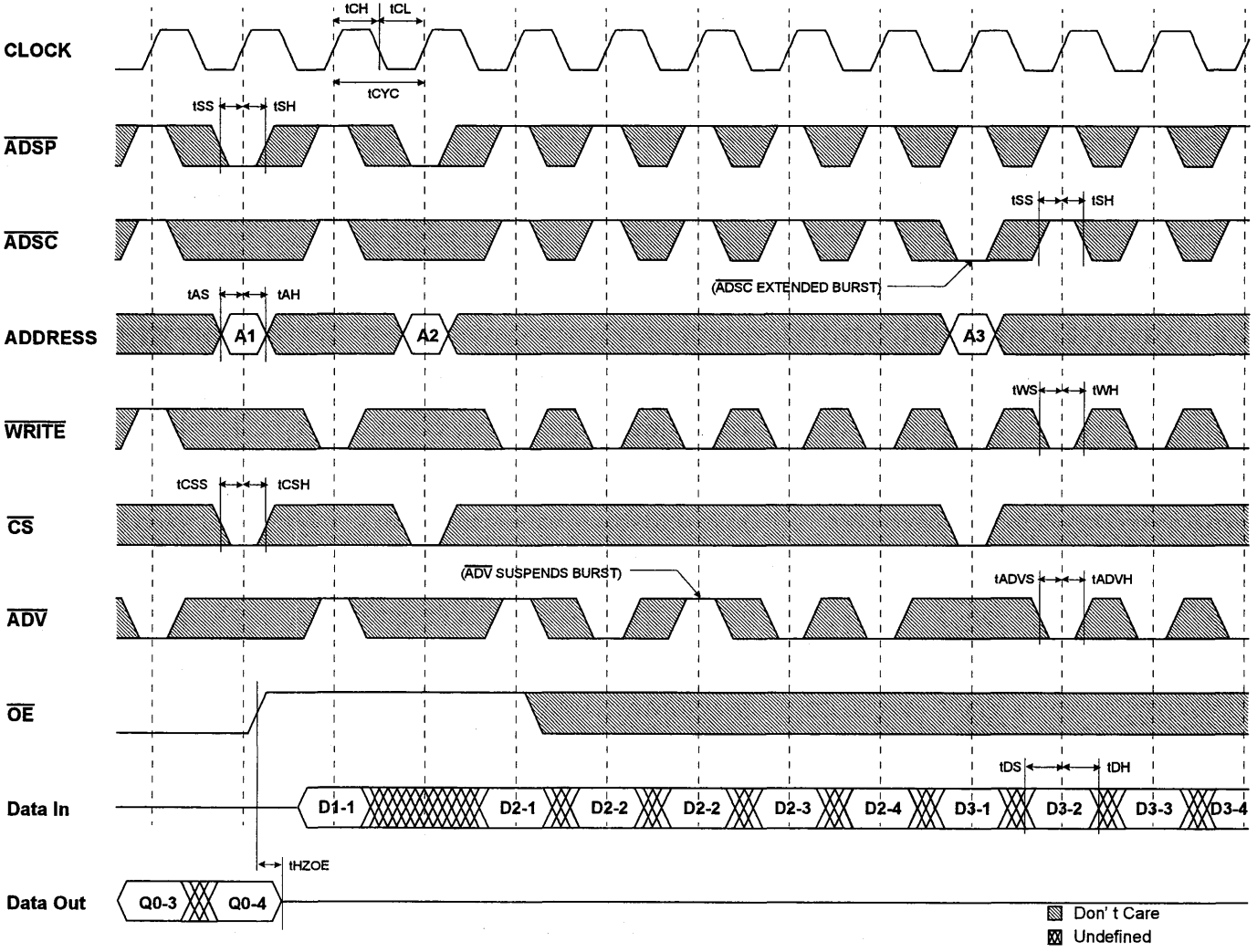
TIMING WAVEFORM OF READ CYCLE



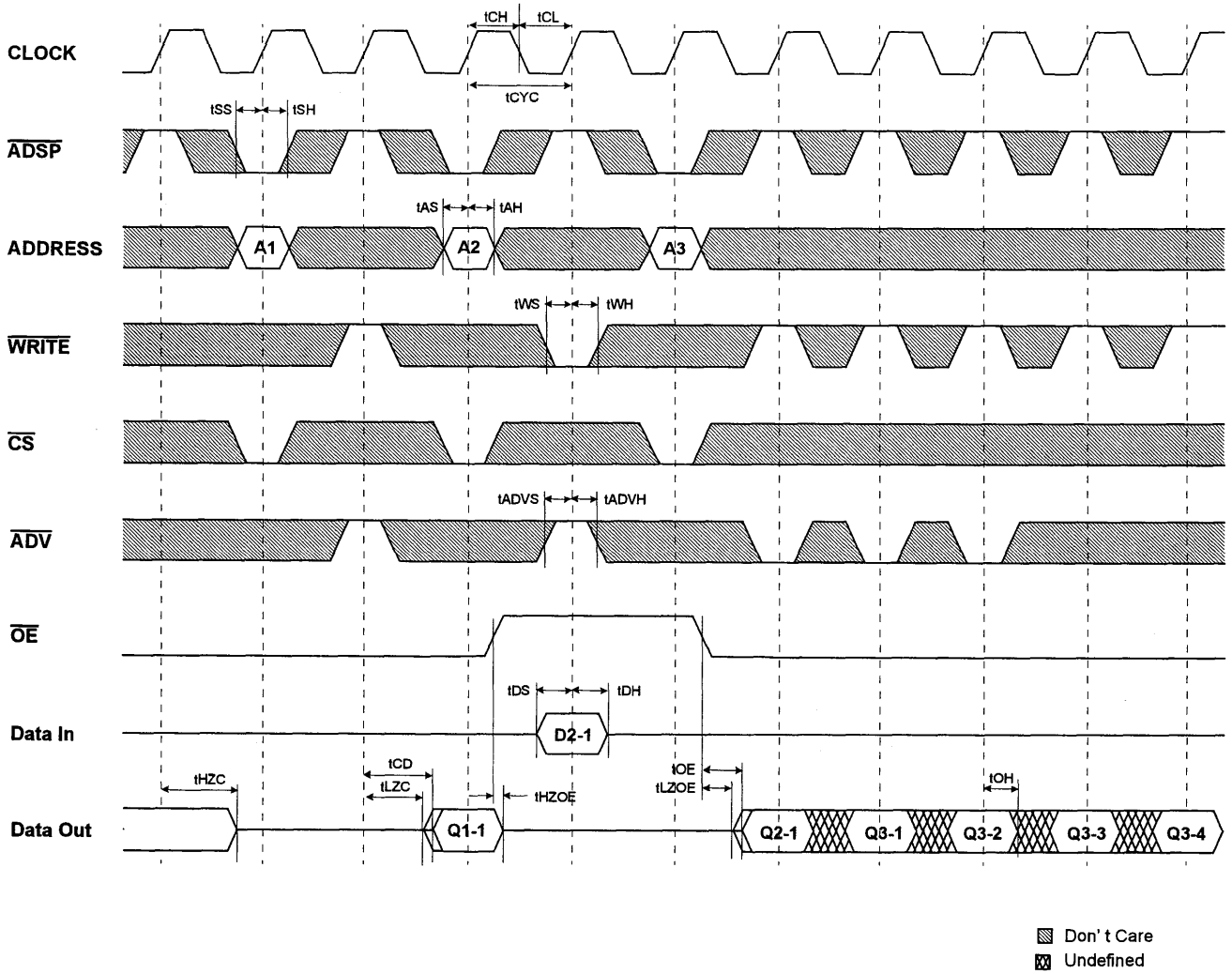
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}x$ = L
$\overline{CS}$ = L means $\overline{CS}1$ = L, CS2 = H and $\overline{CS}2$ = L
$\overline{CS}$ = H means $\overline{CS}1$ = H, or $\overline{CS}1$ = L and $\overline{CS}2$ = H, or $\overline{CS}1$ = L, and CS2 = L

▨ Don' t Care
▩ Undefined

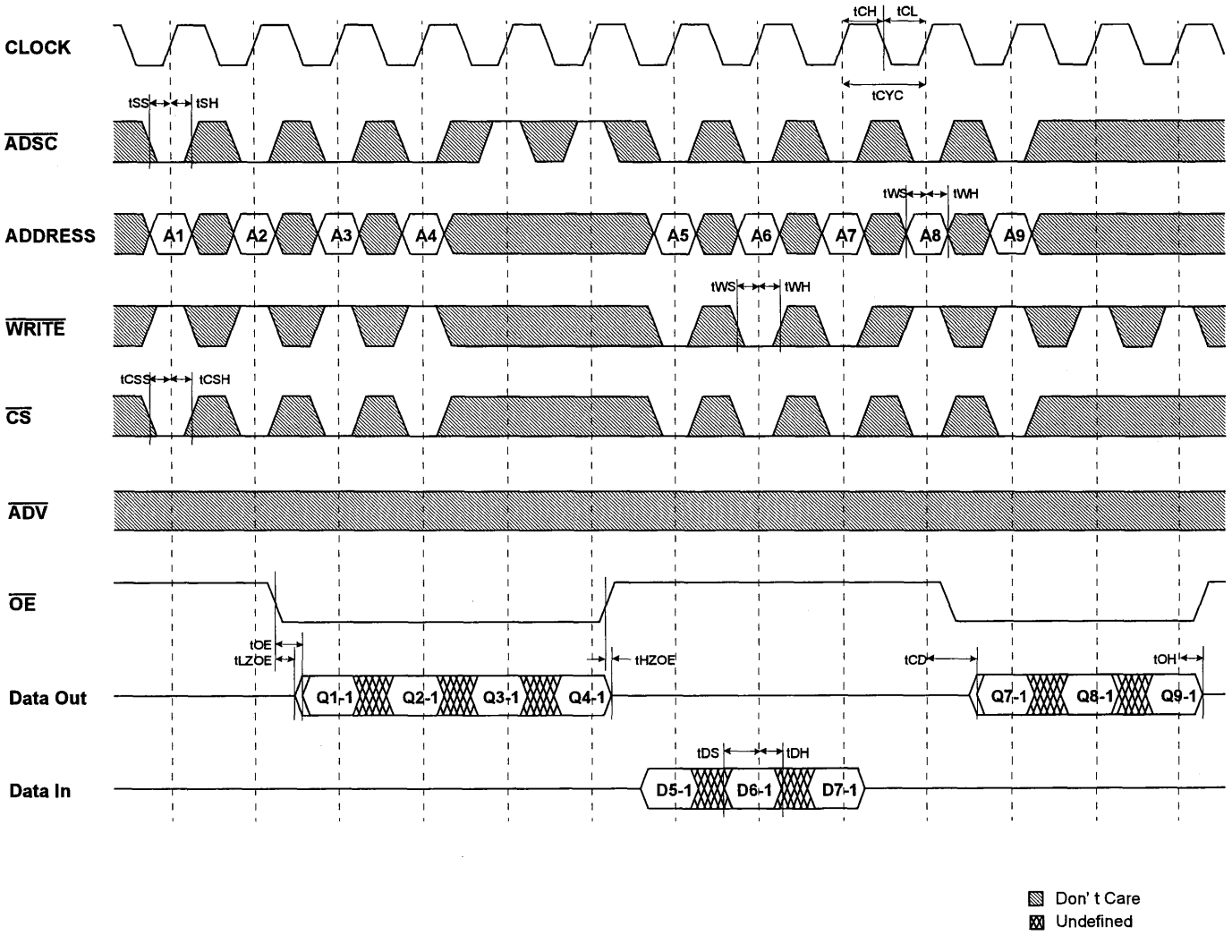
TIMING WAVEFORM OF WRTE CYCLE



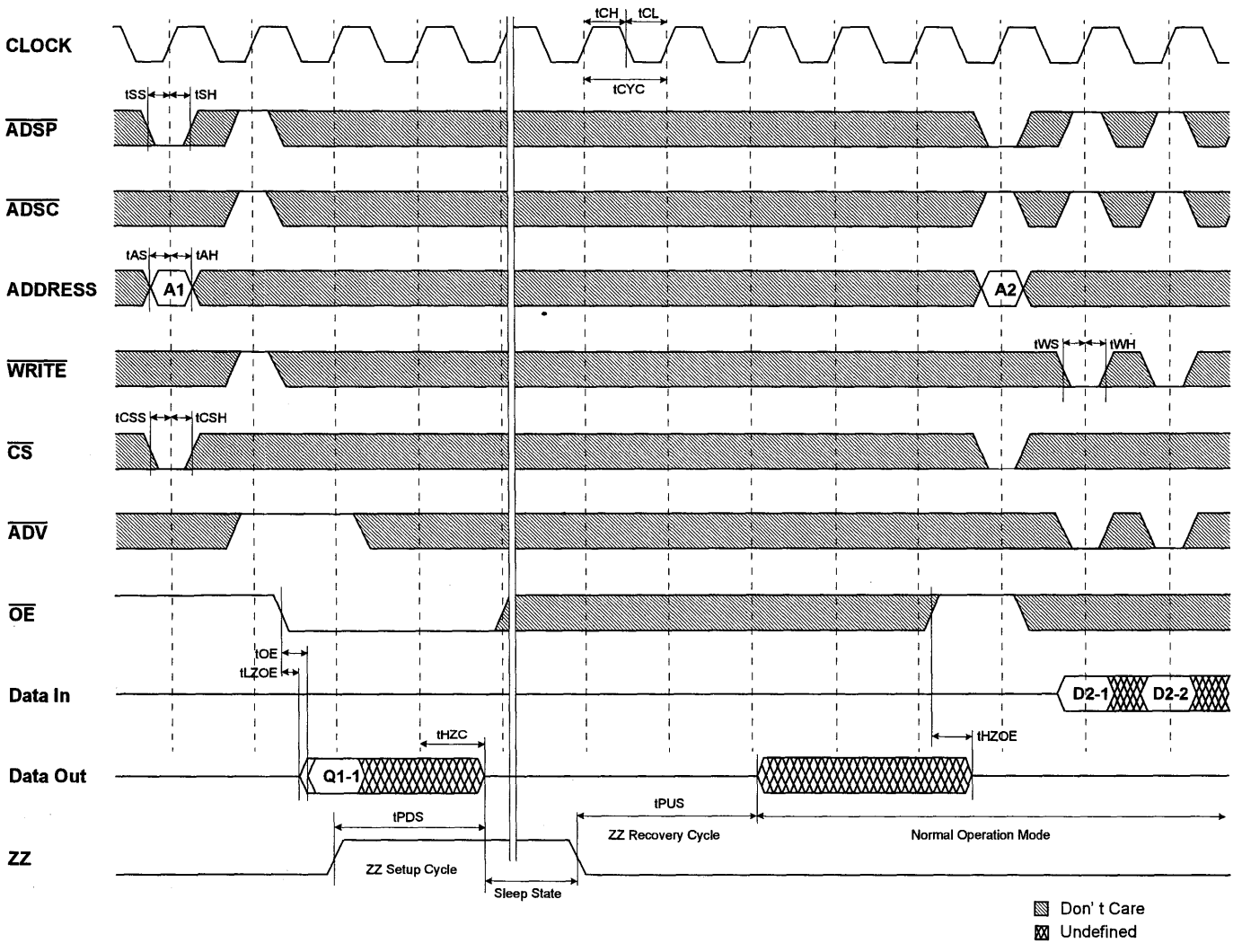
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



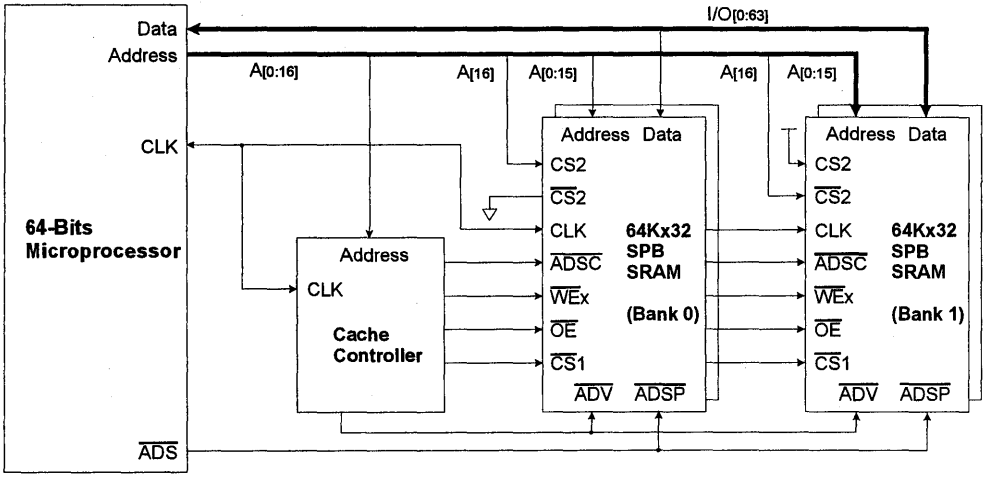
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

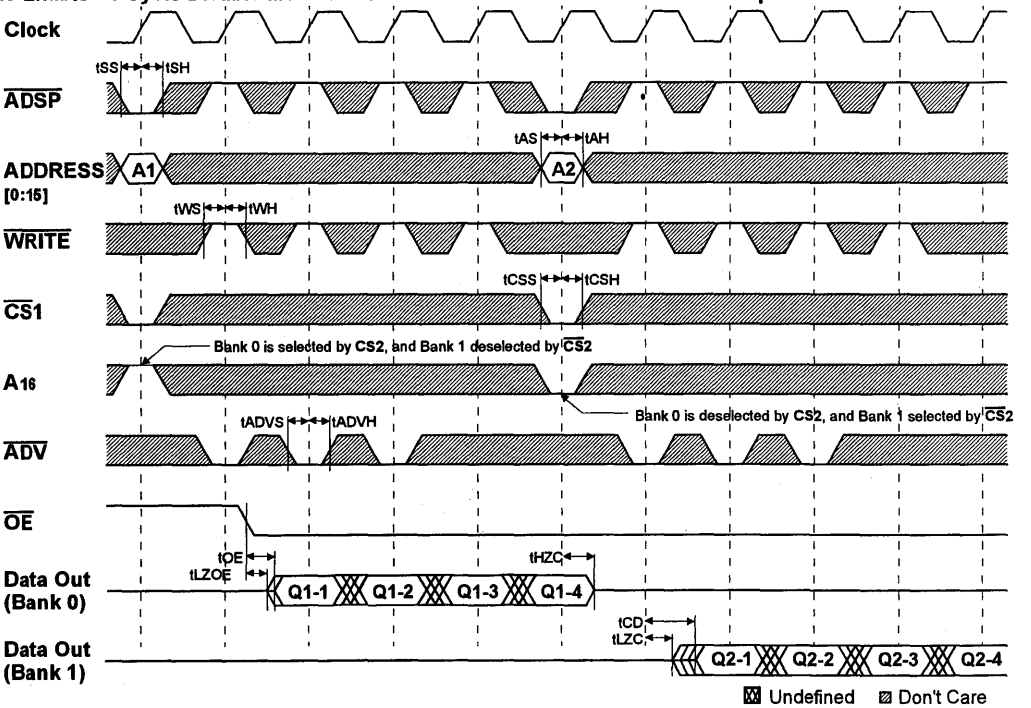
DEPTH EXPANSION

The Samsung 64Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING (Refer non-interleave write timing for interleave write timing)

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.



SAMSUNG ELECTRONICS

64Kx32-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- V_{DD}=3.3V-5%/+10% Power Supply for 3.3V I/O
- V_{DD}=3.3V±5% Power Supply for 2.5V I/O
- I/O Supply Voltage : 3.3V-5%/+10% for 3.3V I/O
  or 2.5V+0.4V/-0.13V for 2.5V I/O
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-13	-15	Unit
Cycle Time	tCYC	13	15	ns
Clock Access Time	tCD	7	8	ns
Output Enable Access Time	tOE	6	7	ns

GENERAL DESCRIPTION

The KM732V696/L is a 2,097,152 bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 64K words of 32 bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signals.

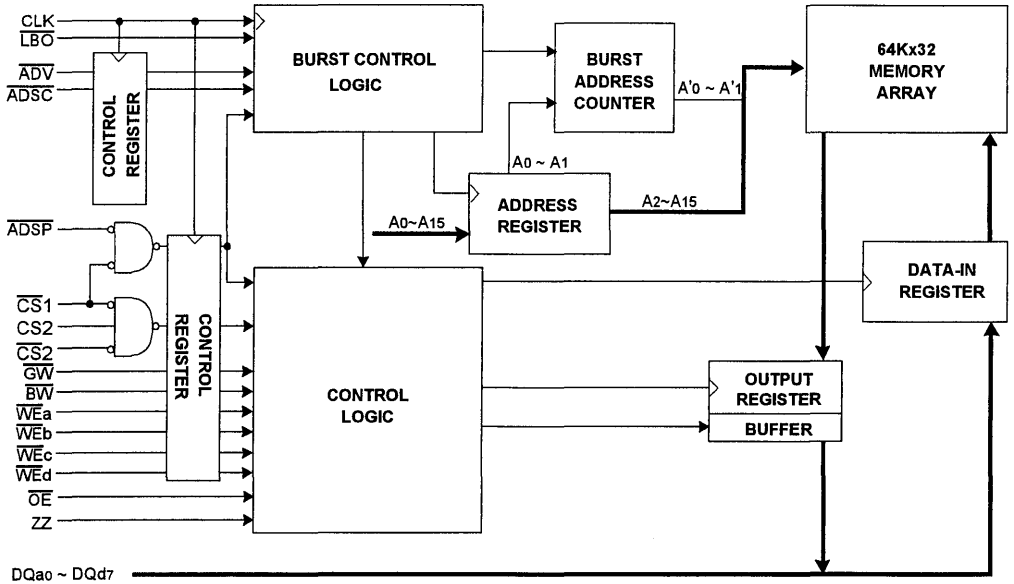
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

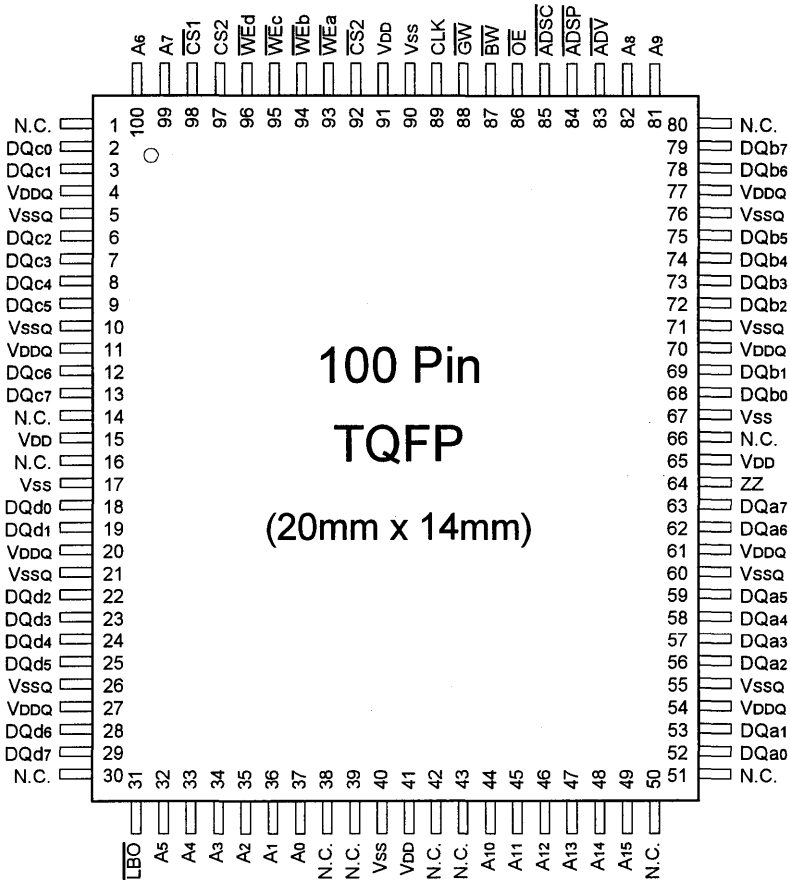
The KM732V696/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A15	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,49, 81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,14,16,30,38,39,42,43, 50,51,66,80
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97			
$\overline{CS2}$	Chip Select	92	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
$\overline{WEx}$	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM732V696/L is a synchronous SRAM designed to support the burst address accessing sequence of the CISC and RISC microprocessor. All inputs(with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled High and $\overline{ADV}$ is sampled Low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$(regardless of $\overline{BW}$ and $\overline{WE}$x.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x when $\overline{GW}$ is High.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ Low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled Low(regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled Low. The address increases internally to the next address of burst, if both $\overline{WE}$x and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. The $\overline{WE}$a controls $DQa_0 \sim DQa_7$, $\overline{WE}$b controls $DQb_0 \sim DQb_7$, $\overline{WE}$c controls $DQc_0 \sim DQc_7$, and $\overline{WE}$d control $DQd_0 \sim DQd_7$. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
$\overline{WE}$x are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	WRITE	Operation	CS1	WRITE	OE	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

2

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O(0℃ ≤ T_A ≤ 70℃)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
	V_{DDQ}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O(0℃ ≤ T_A ≤ 70℃)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.47	V
	V_{DDQ}	2.37	2.5	2.9	V
Ground	Vss	0	0	0	V

CAPACITANCE* (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

*NOTE : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(V_{DD}=3.3V-5%/+10%, V_{DDQ}=3.3V-5%/+10%, or V_{DD}=3.3V±5%, V_{DDQ}=2.5V+0.4V/-0.13V, T_A = 0℃ to 70℃)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Vss to V_{DD}, V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	-13	-	250	mA
			-15	-	220	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V		-	60	mA
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs = fixed (V_{DD}-0.2V or 0.2V)		-	10	mA
			L-Ver.	-	2.0	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	10	mA
			L-Ver.	-	1.0	mA
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL} = 1mA		-	0.2	V
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH} = -1mA		2.0	-	V
Input Low Voltage(3.3V I/O)	V_{IL}			-0.5*	0.8	V
Input High Voltage(3.3V I/O)	V_{IH}			2.0	5.5**	V
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V
Input High Voltage(2.5V I/O)	V_{IH}			1.7	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

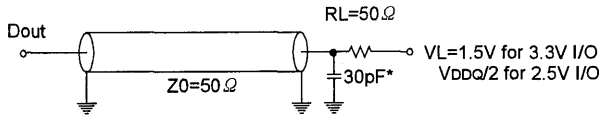
TEST CONDITIONS

(T_A = 0℃ to 70℃, V_{DD}=3.3V-5%/+10%, V_{DDQ}=3.3V-5%/+10%, or V_{DD}=3.3V±5%, V_{DDQ}=2.5V +0.4V/-0.13V)

Parameter	Value
Input Pulse Level (for 3.3V I/O)	0 to 3V
Input Pulse Level (for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	2ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	2ns
Input and Output Timing Reference Levels(for 3.3V I/O)	1.5V
Input and Output Timing Reference Levels(for 2.5V I/O)	V_{DDQ}/2
Output Load	See Fig. 1

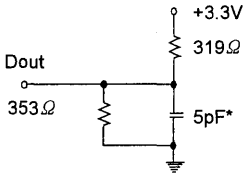
2

Output Load(A)



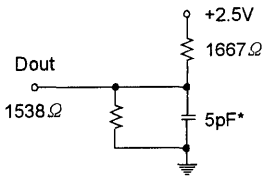
* Capacitive Load consists of all components of the test environment.

Output Load(B), (3.3V I/O)
(for tLZC, tLZOE, tHZOE & tHZC)



* Including Scope and Jig Capacitance

Output Load(C), (2.5V I/O)
(for tLZC, tLZOE, tHZOE & tHZC)



* Including Scope and Jig Capacitance

Fig. 1

SAMSUNG ELECTRONICS

AC TIMING CHARACTERISTICS

(T_A = 0℃ to 70℃, V_{DD}=3.3V-5%/+10%, V_{DDQ}=3.3V-5%/+10%, or V_{DD}=3.3V±5%, V_{DDQ}=2.5V +0.4V/-0.13V, unless otherwise specified)

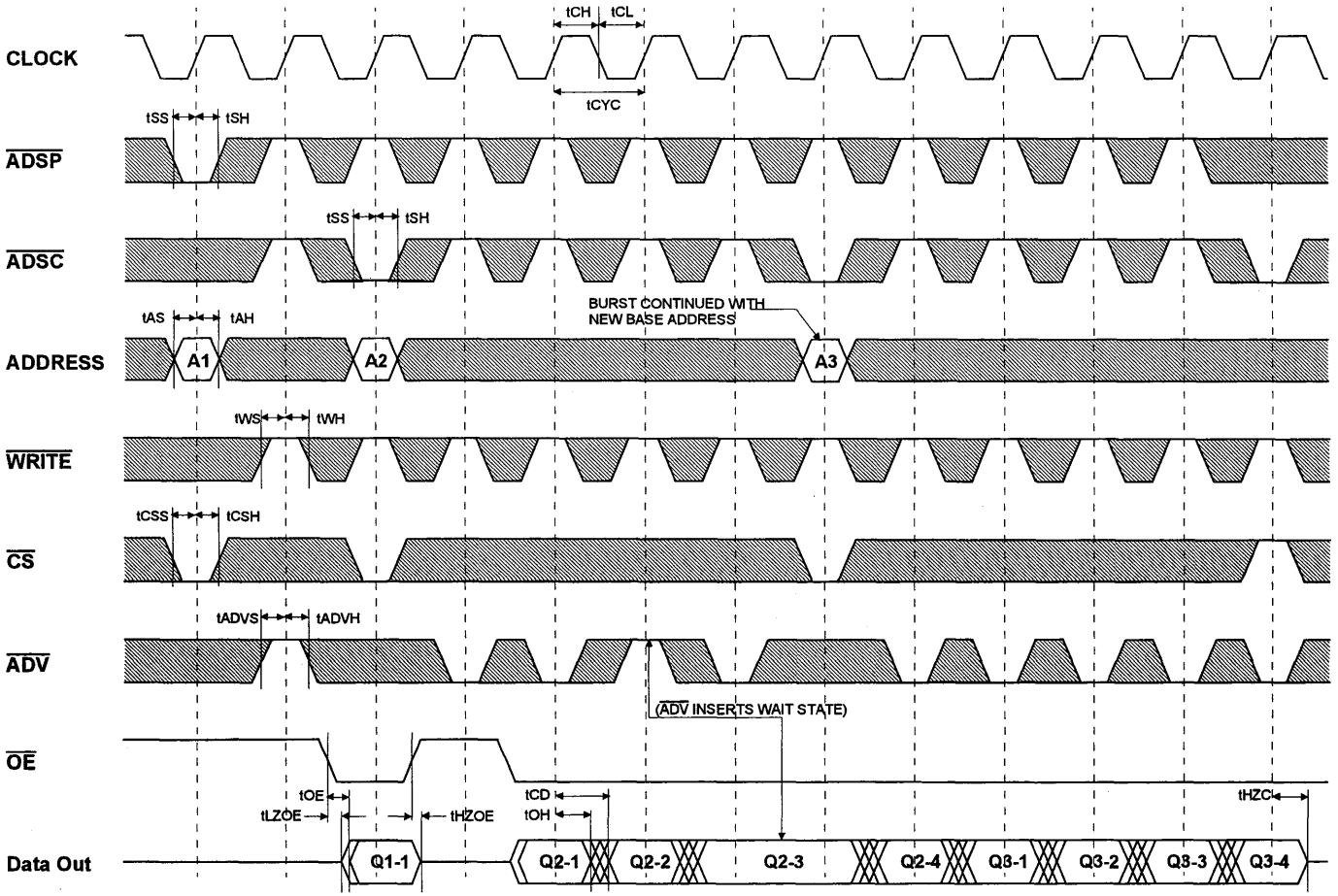
Parameter	Symbol	KM732V696-13		KM732V696-15		Unit
		Min	Max	Min	Max	
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	8	ns
Output Enable to Data Valid	tOE	-	6	-	7	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	2.0	-	2.0	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

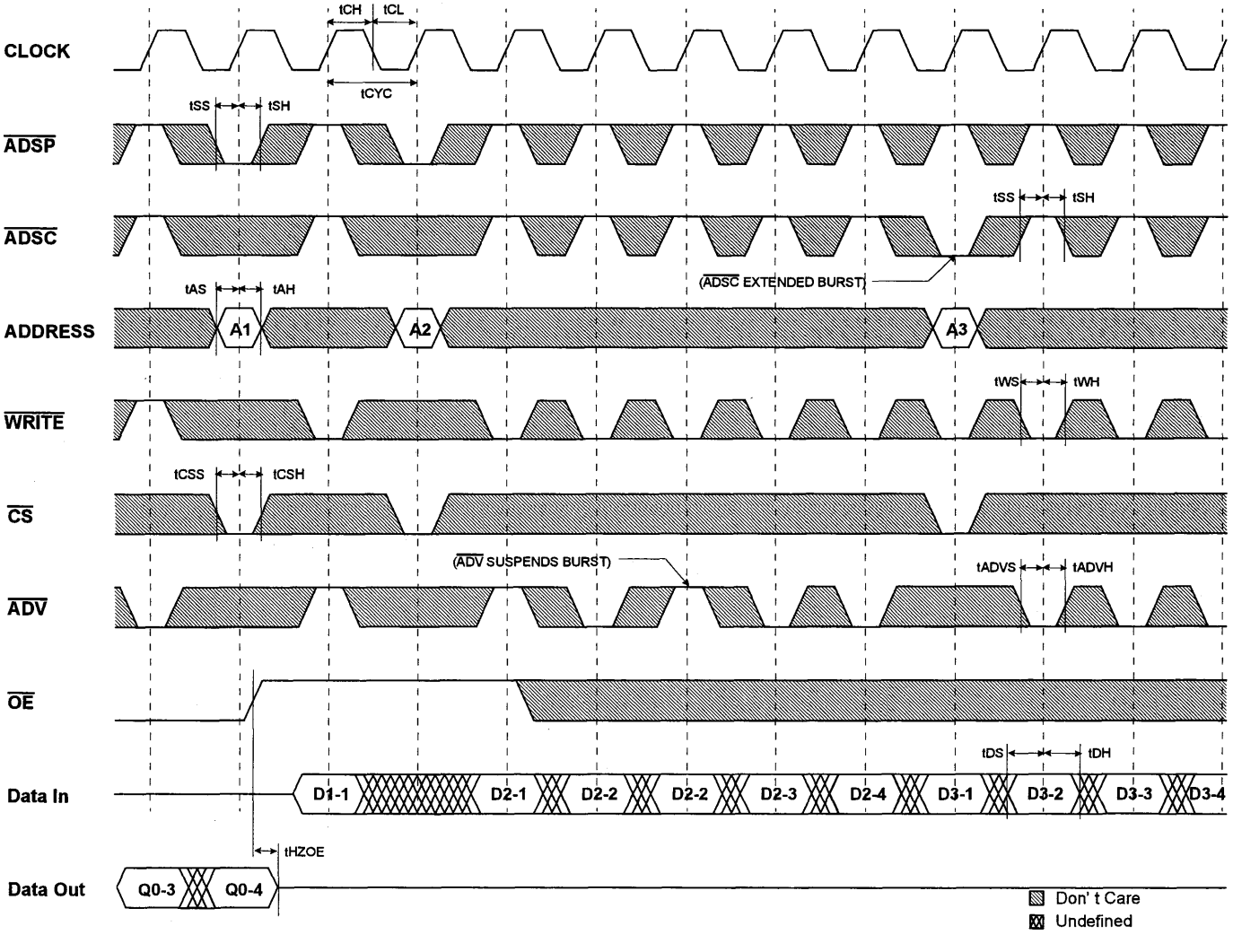
TIMING WAVEFORM OF READ CYCLE



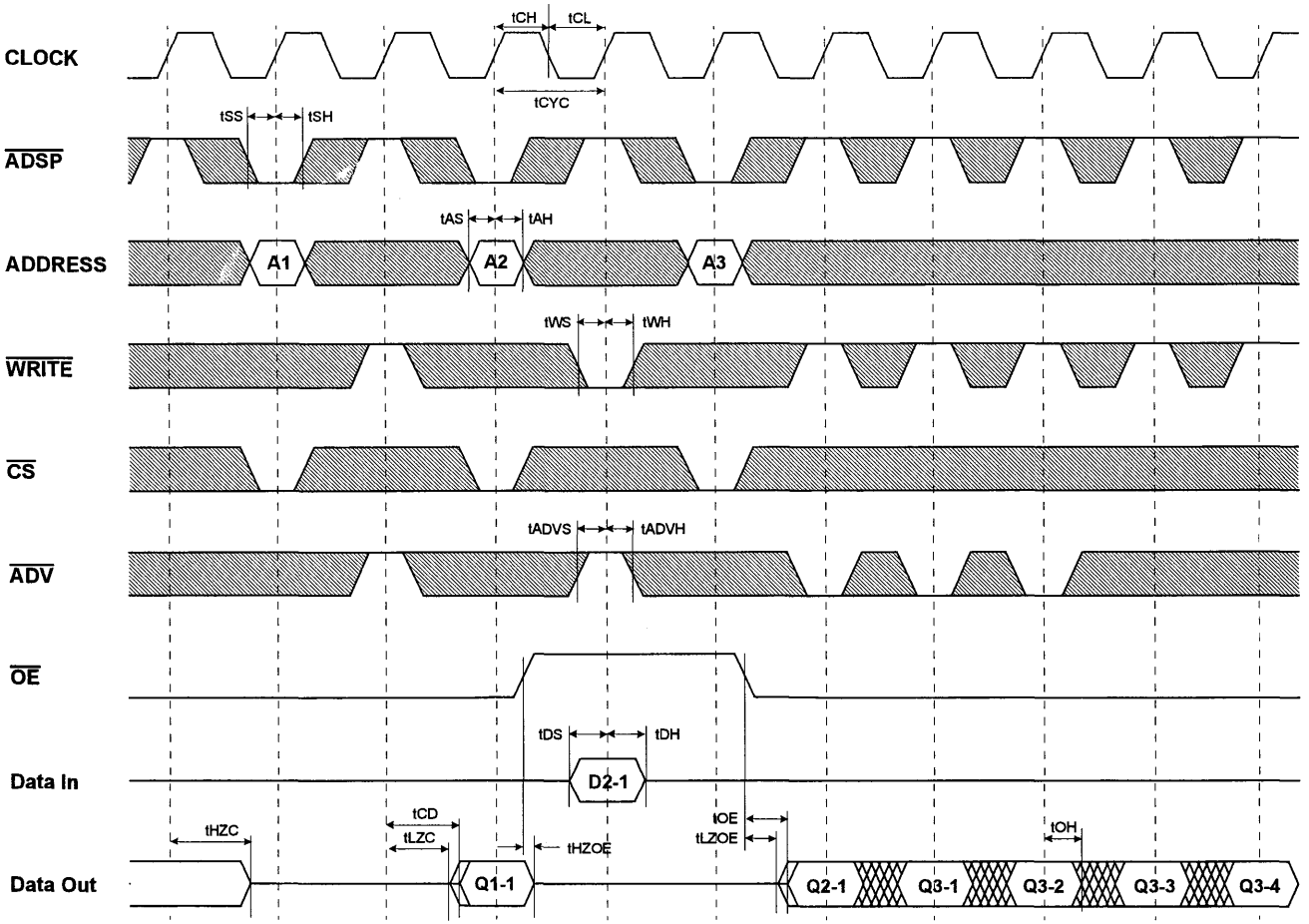
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}x$ = L
$\overline{CS}$ = L means $\overline{CS1}$ = L, CS2 = H and $\overline{CS2}$ = L
$\overline{CS}$ = H means $\overline{CS1}$ = H, or $\overline{CS1}$ = L and $\overline{CS2}$ = H, or $\overline{CS1}$ = L, and CS2 = L

▨ Don' t Care
▩ Undefined

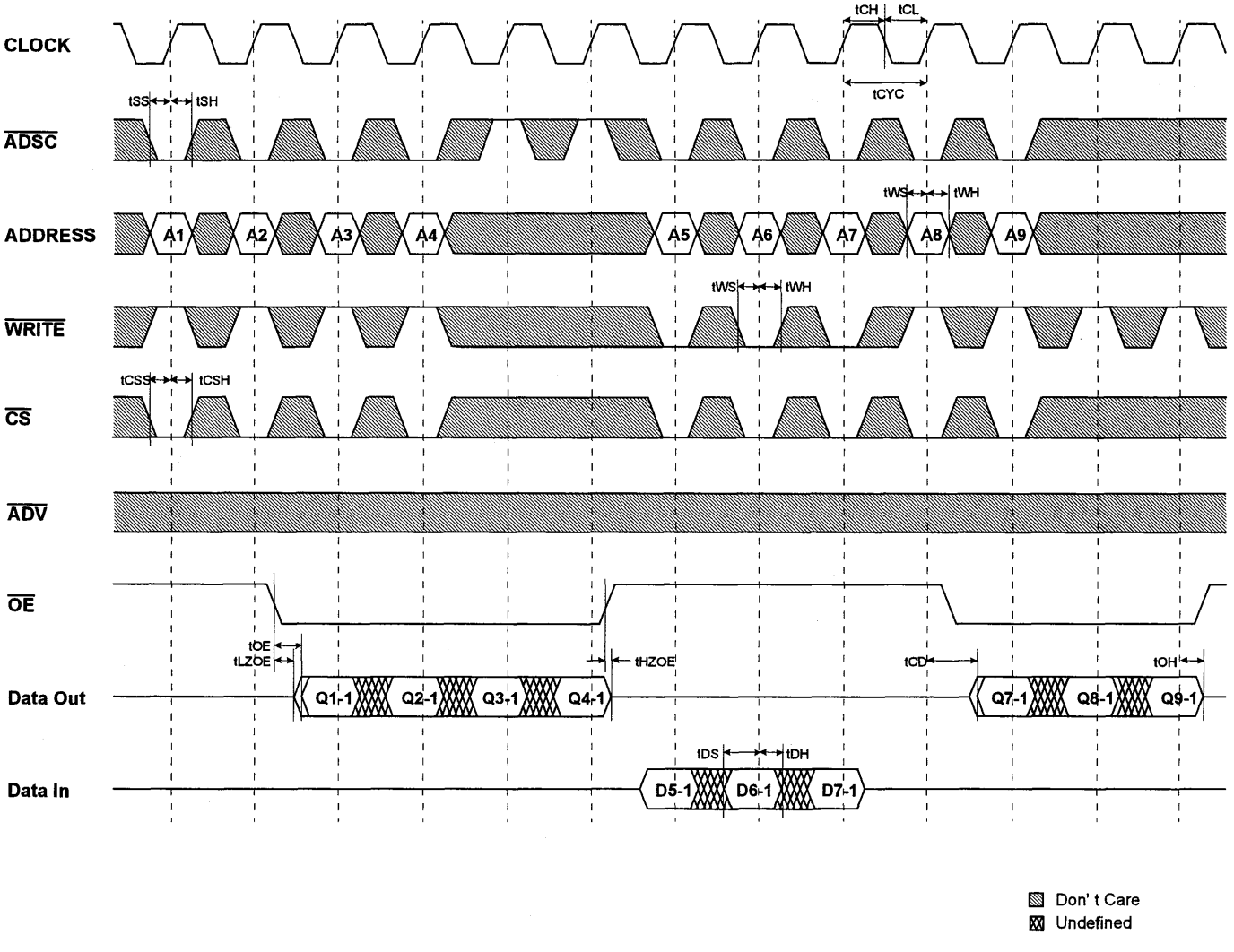
TIMING WAVEFORM OF WRTE CYCLE



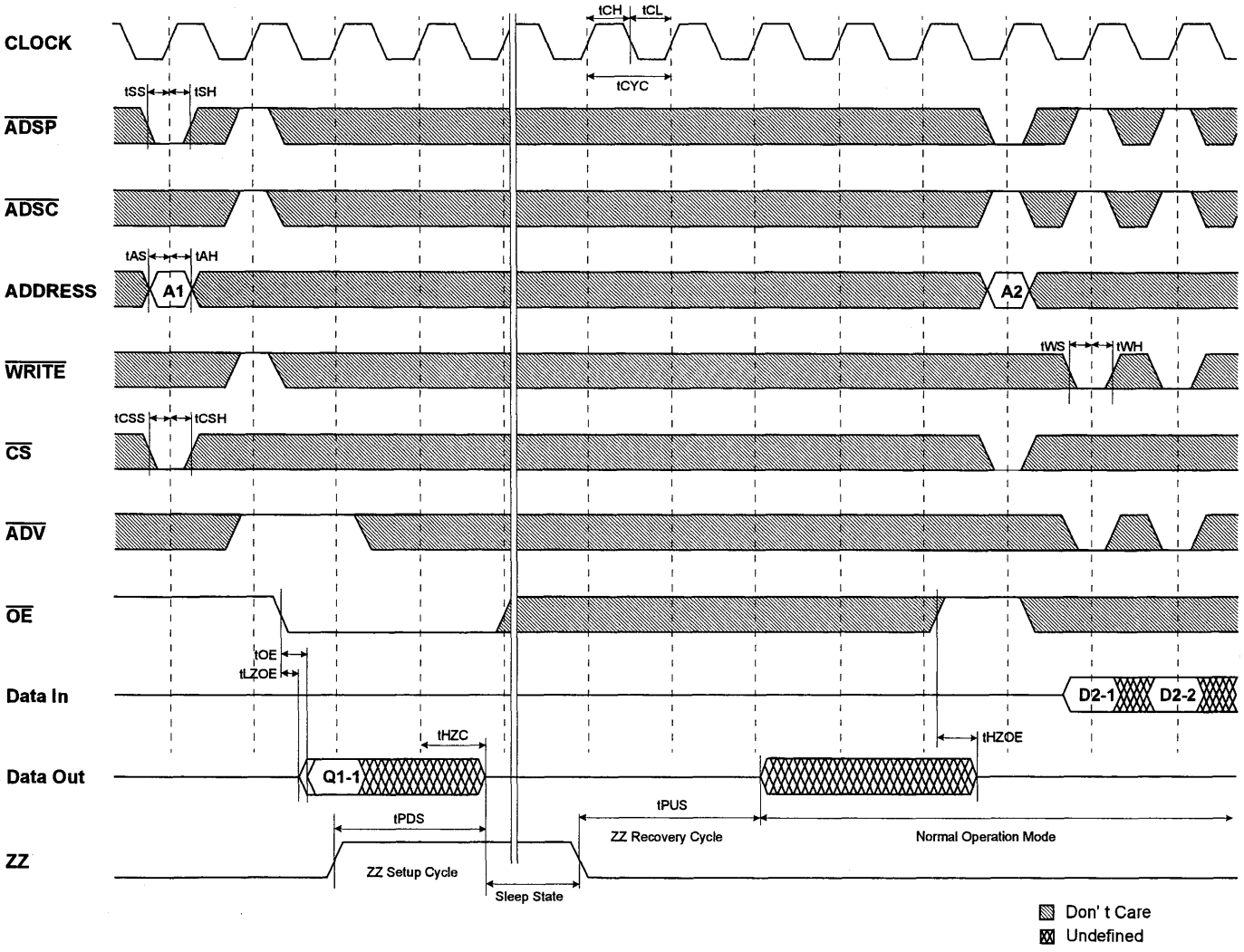
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



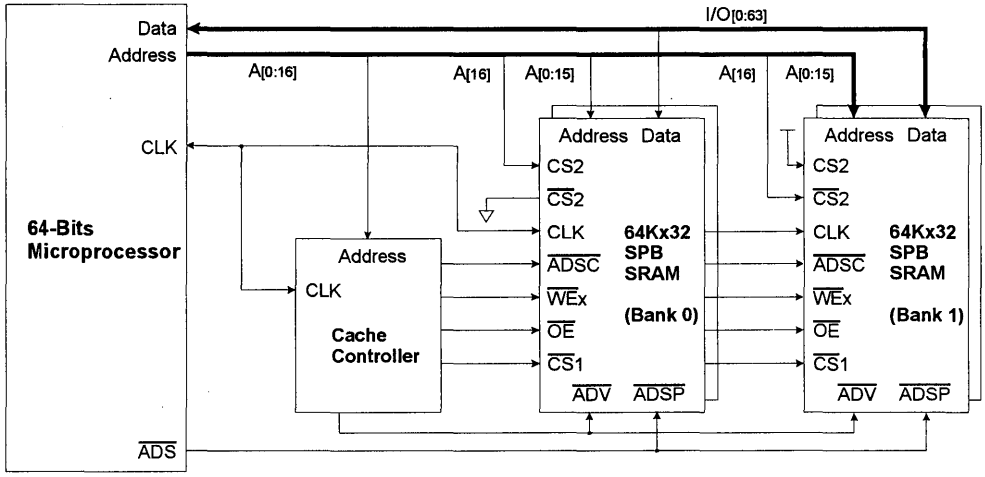
TIMING WAVEFORM OF POWER DOWN CYCLE



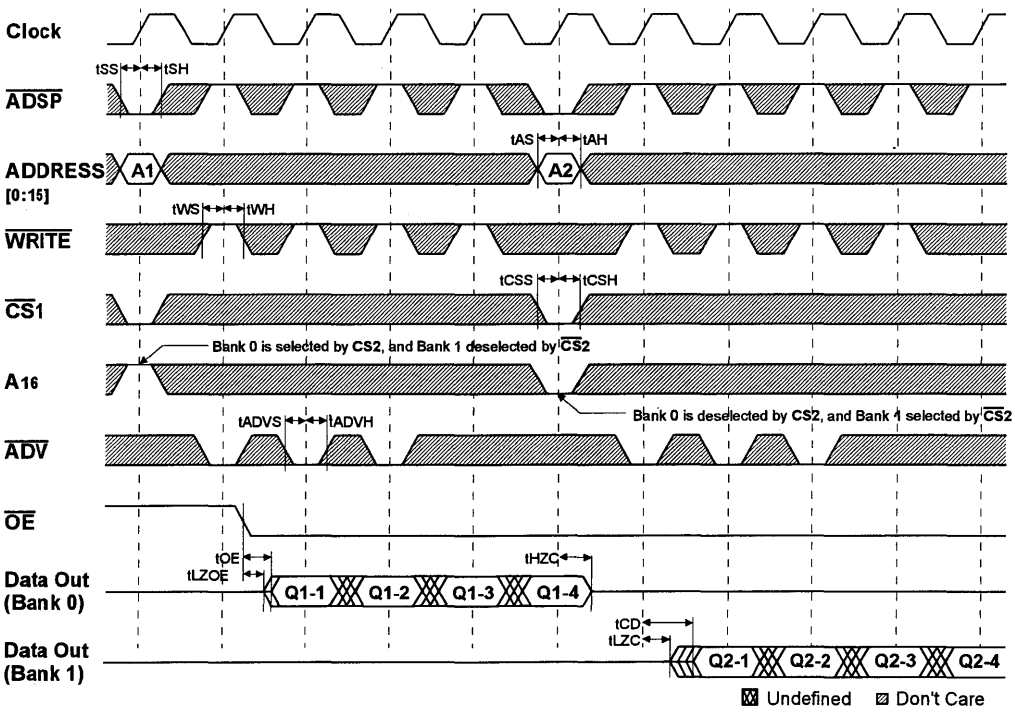
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 64Kx32 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING (Refer non-interleave write timing for interleave write timing)



128Kx18-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined Operation With 4 Burst
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- V_{DD} = 3.3V-5%/+10% Power Supply.
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-7	-8	-10	-11	Unit
Cycle Time	tCYC	7.5	8.6	10	11	ns
Clock Access Time	tCD	4.5	5.0	5.0	6.0	ns
Output Enable Access Time	tOE	4.5	5.0	5.0	6.0	ns

GENERAL DESCRIPTION

The KM718V789/L is a 2,359,296 bits Synchronous Static Random Access Memory designed for high performance second level cache of pentium and Power PC based system.

It is organized as 128K words of 18 bits. And it integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, $\overline{ZZ}$.

Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS1}$ high, $\overline{ADSP}$ disable to support address pipelining.

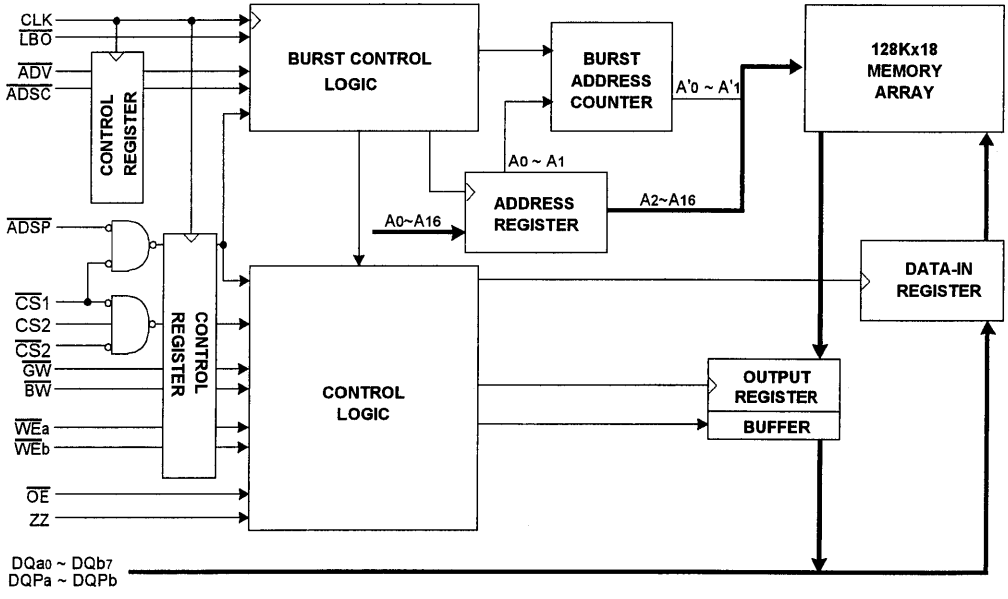
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence (linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

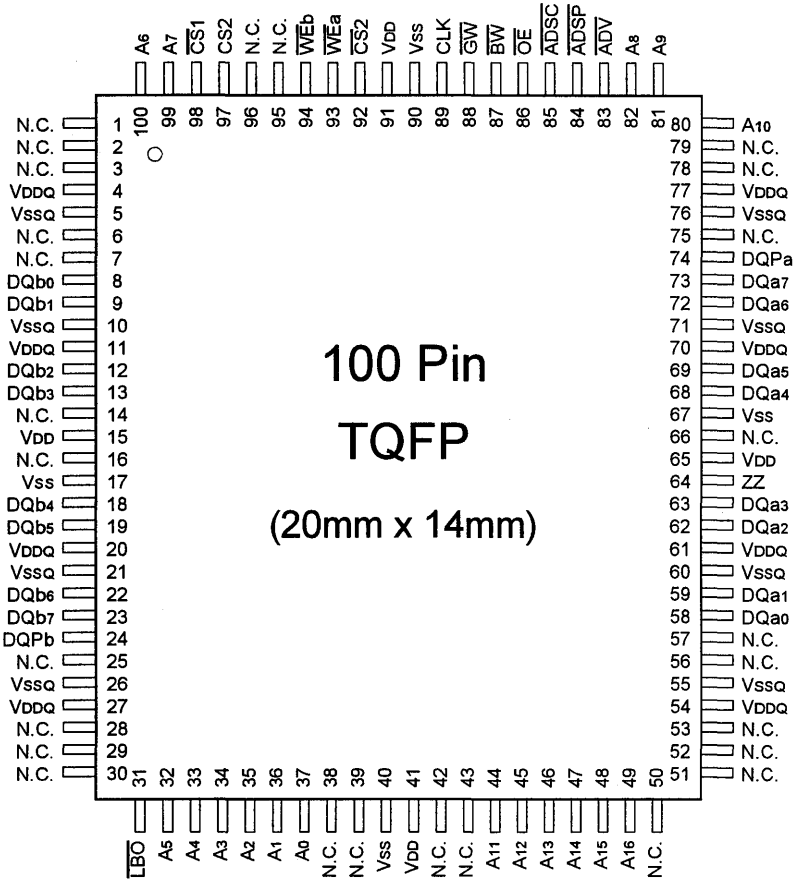
The KM718V789/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A16	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,49, 80,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			Vss	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,14,16,25,28,29 ,30,38,39,42,43,50, 51,52,53,56,57,66,75, 78,79,95,96
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85			
CLK	Clock	89	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
$\overline{CS1}$	Chip Select	98	DQb0 ~ b7		8,9,12,13,18,19,22,23
CS2	Chip Select	97	DQPa, Pb		74,24
$\overline{CS2}$	Chip Select	92	VDDQ	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
$\overline{WEx}$	Byte Write Inputs	93,94			
$\overline{OE}$	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

SAMSUNG ELECTRONICS

FUNCTION DESCRIPTION

The KM718V789 is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs(with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ and Chip Select pins.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled High and $\overline{ADV}$ is sampled Low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS}$1.

All byte write is done by $\overline{GW}$ (regardless of $\overline{BW}$ and $\overline{WE}$x.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x when $\overline{GW}$ is High.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ Low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled Low(regaedless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled Low. The address increases internally to the next address of burst, if both $\overline{WE}$x and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a or $\overline{WE}$b) sampled low. The $\overline{WE}$a controls DQa0 ~ DQa7 and DQPa, $\overline{WE}$b controls DQb0 ~ DQb7 and DQPb. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

$\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
$\overline{WE}$x are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And when this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN: HIGH	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN: LOW	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	1	0	1	1	0	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	Operation
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	$\overline{WRITE}$	Operation	$\overline{CS1}$	$\overline{WRITE}$	$\overline{OE}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.
2. $\overline{WE}$x means $\overline{WE}$a ~ $\overline{WE}$d.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ}+ 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
	V_{DDQ}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

CAPACITANCE*(T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%)

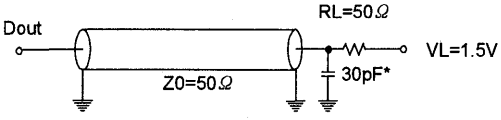
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Vss to V_{DD} ; V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT}=Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	-7	-	395	mA
			-8	-	360	
			-10	-	320	
			-11	-	320	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-7	-	100	mA
			-8	-	90	
			-10	-	80	
			-11	-	80	
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	10	mA
			L-Ver	-	5.0	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	10	mA
			L-Ver	-	1.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.0	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

TEST CONDITIONS(T_A = 0℃ to 70℃, V_{DD} = 3.3V-5%/+10%, unless otherwise specified)

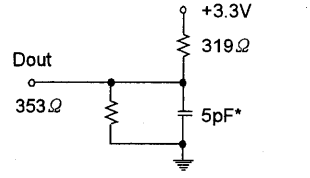
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)



* Capacitive Load consists of all components of the test environment.

Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

SAMSUNG ELECTRONICS

AC TIMING CHARACTERISTICS

(V_{DD}=3.3V-5%/+10%, T_A = 0℃ to 70℃)

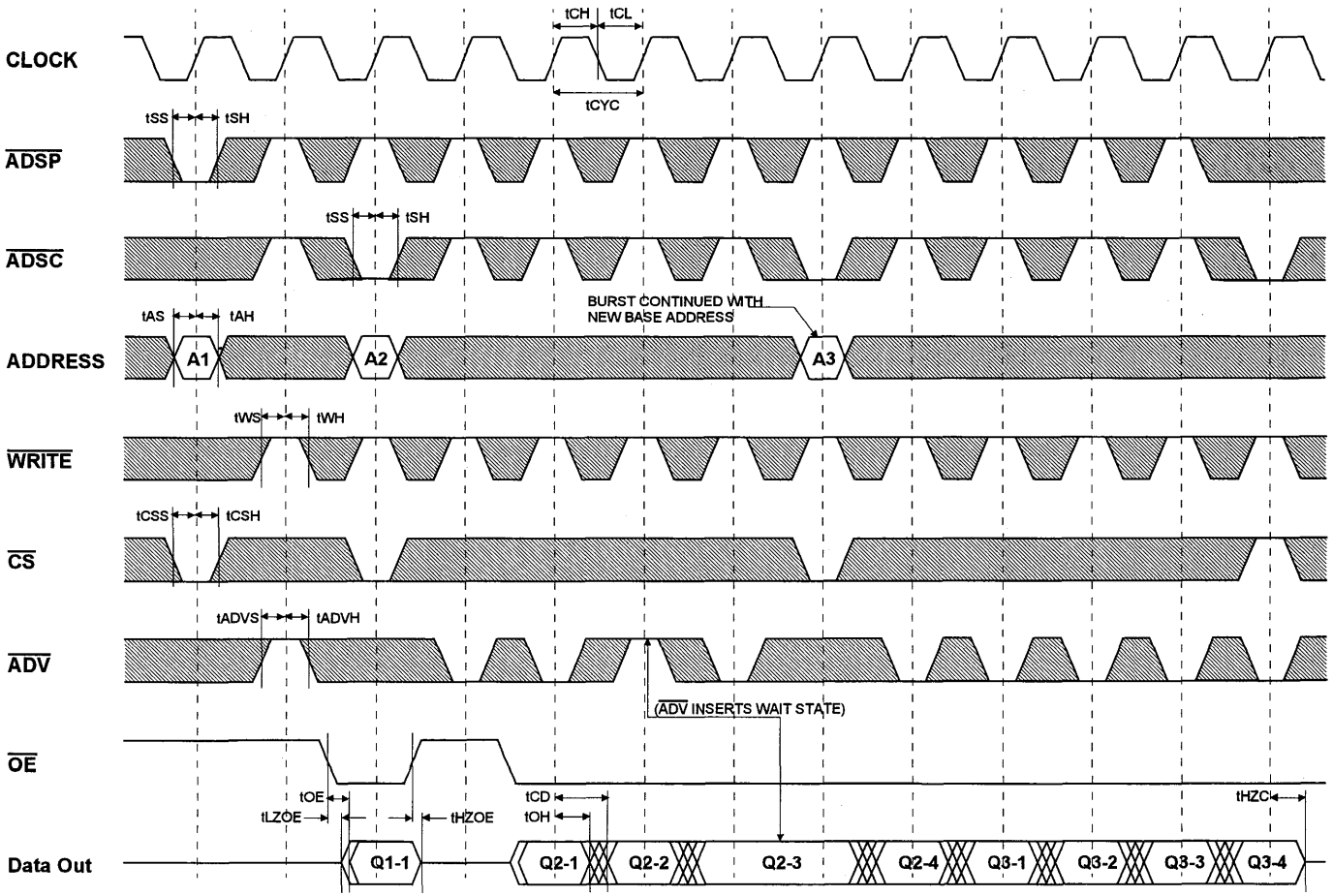
Parameter	Symbol	-7		-8		-10		-11		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	7.5	-	8.6	-	10	-	11	-	ns
Clock Access Time	tCD	-	4.5	-	5.0	-	5.0	-	6.0	ns
Output Enable to Data Valid	tOE	-	4.5	-	5.0	-	5.0	-	6.0	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	3.0	-	3.5	-	4.0	-	4.0	-	ns
Clock Low Pulse Width	tCL	3.0	-	3.5	-	4.0	-	4.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.5	-	2.5	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	2	-	cycl
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	2	-	cycl

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

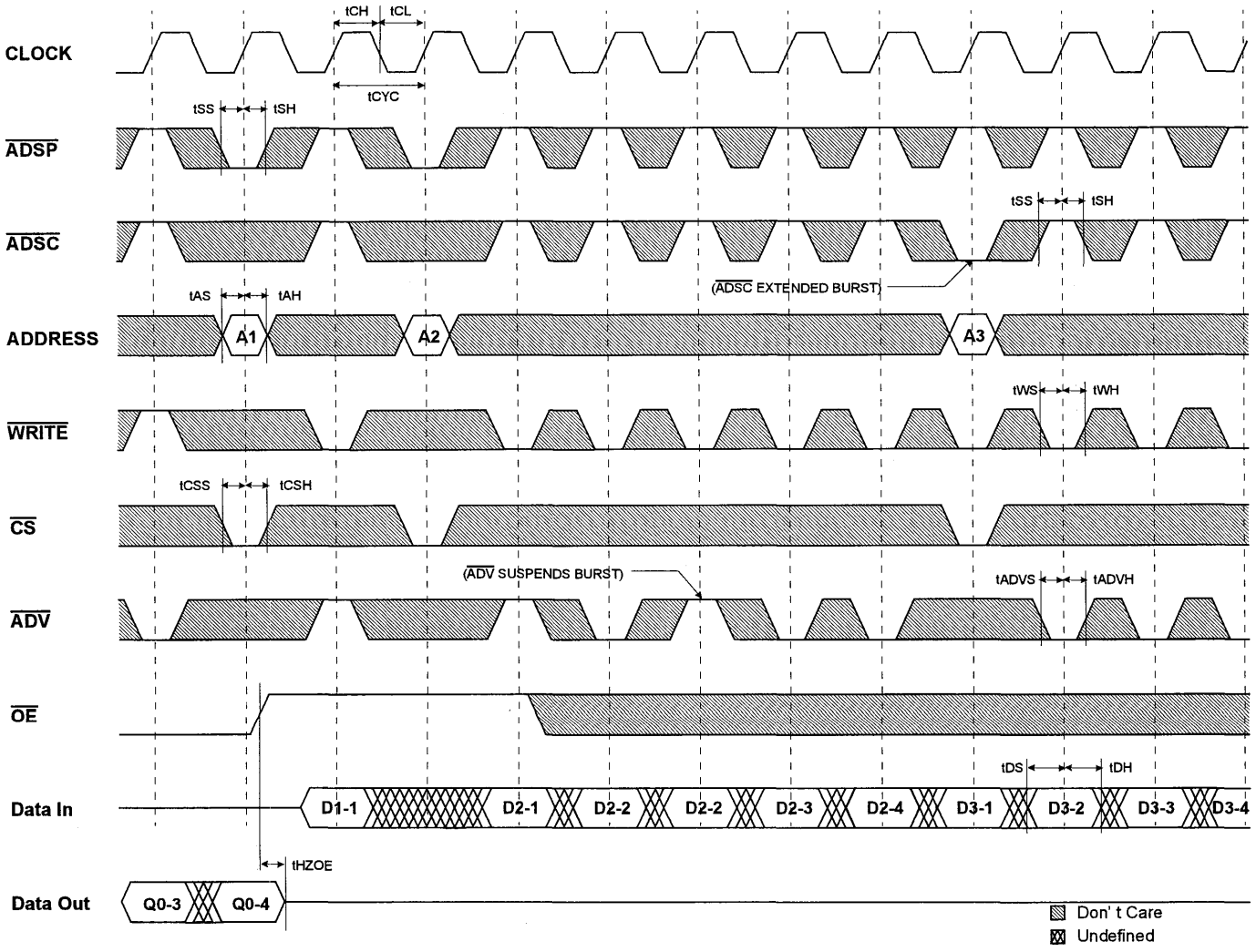
TIMING WAVEFORM OF READ CYCLE



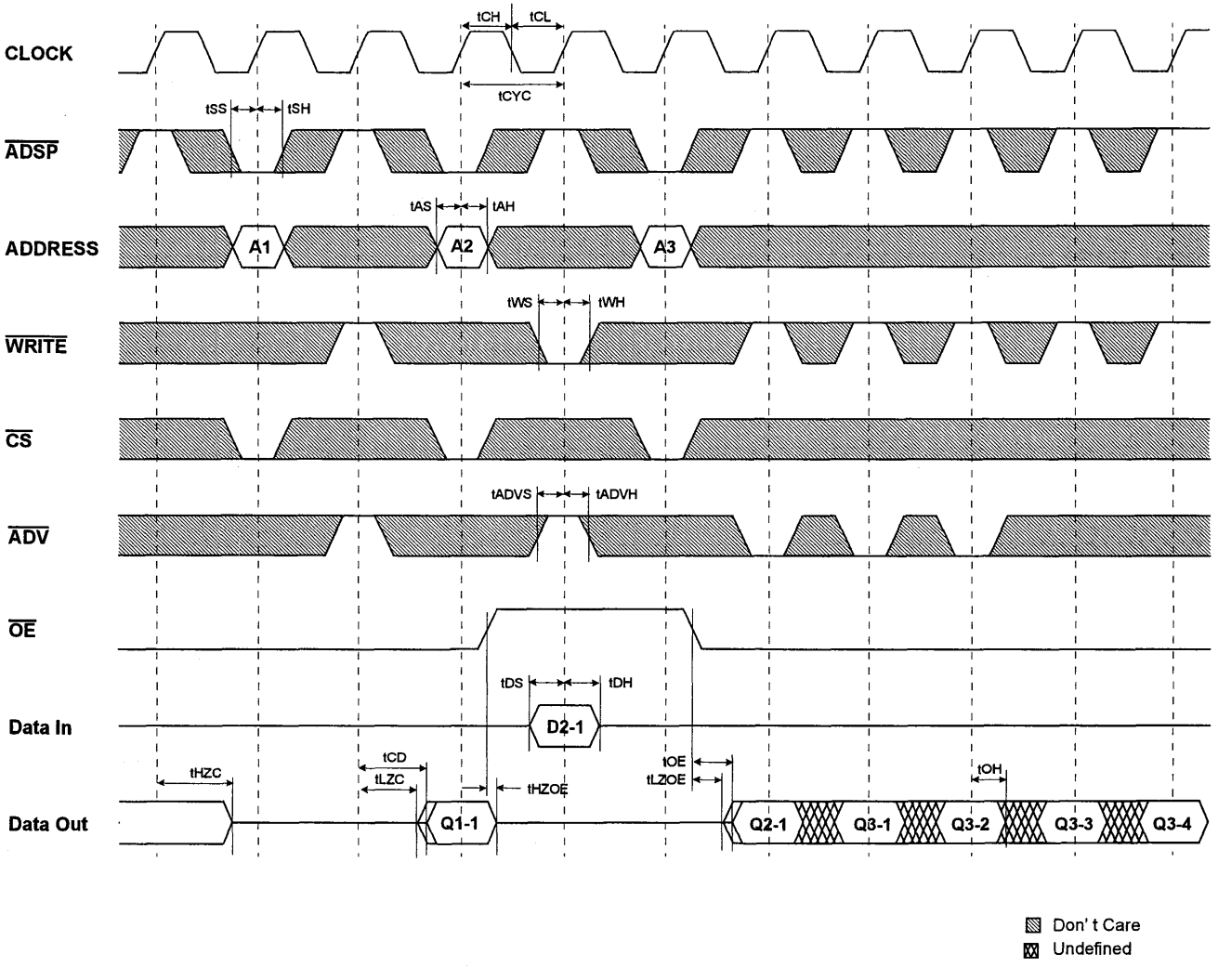
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}x$ = L
$\overline{CS}$ = L means $\overline{CS}1$ = L, CS2 = H and $\overline{CS}2$ = L
$\overline{CS}$ = H means $\overline{CS}1$ = H, or $\overline{CS}1$ = L and $\overline{CS}2$ = H, or $\overline{CS}1$ = L, and CS2 = L

▨ Don' t Care
▩ Undefined

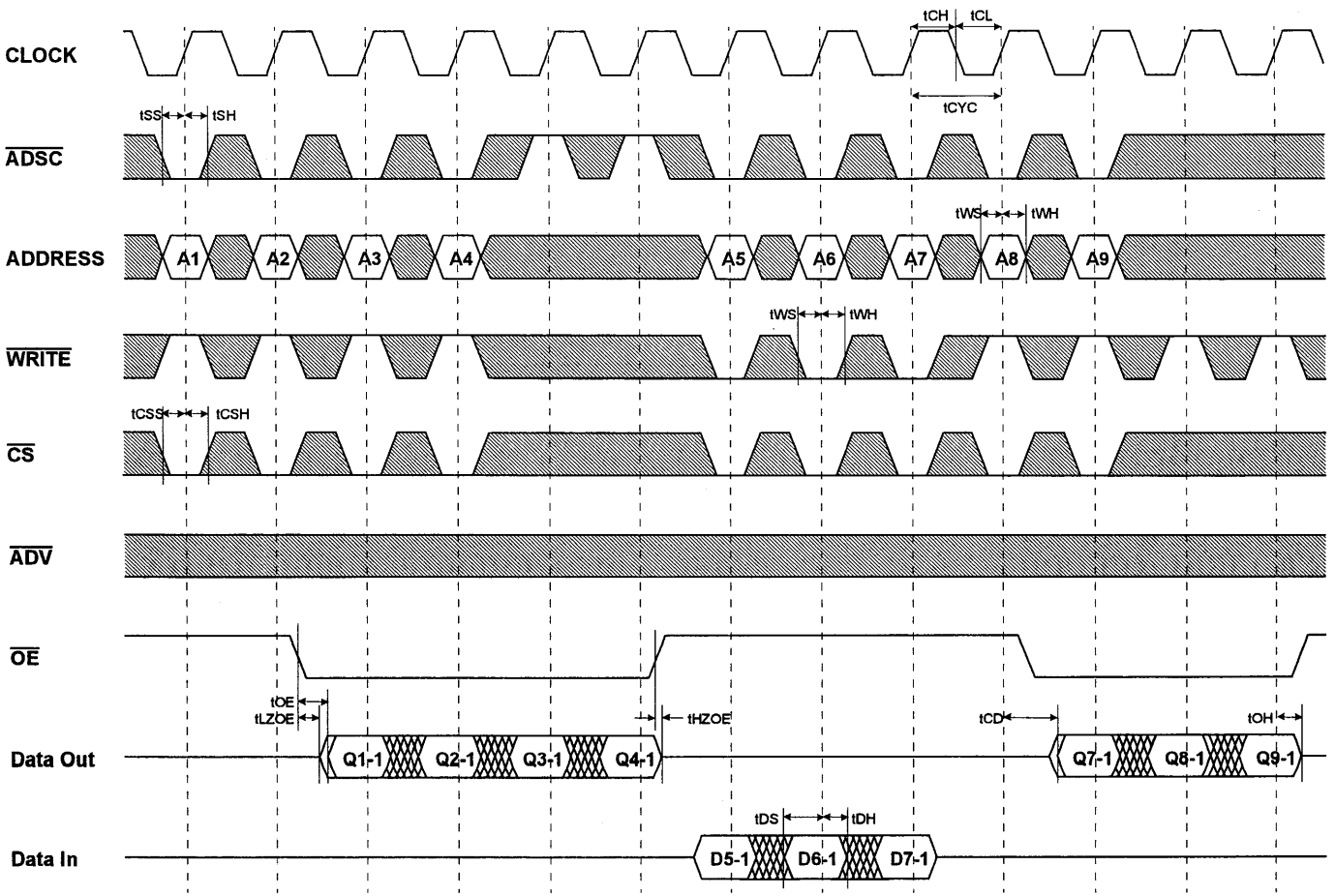
TIMING WAVEFORM OF WRTE CYCLE



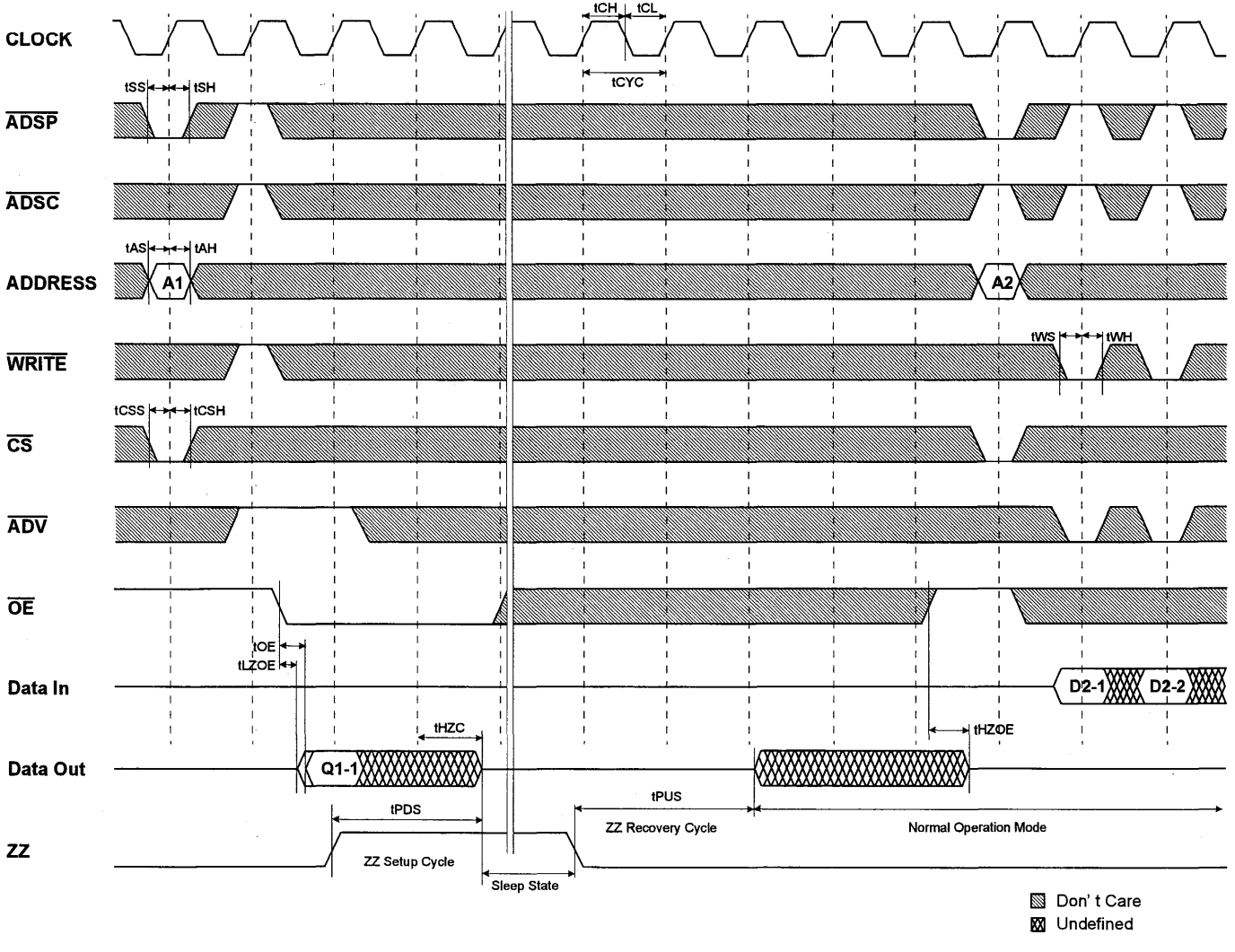
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



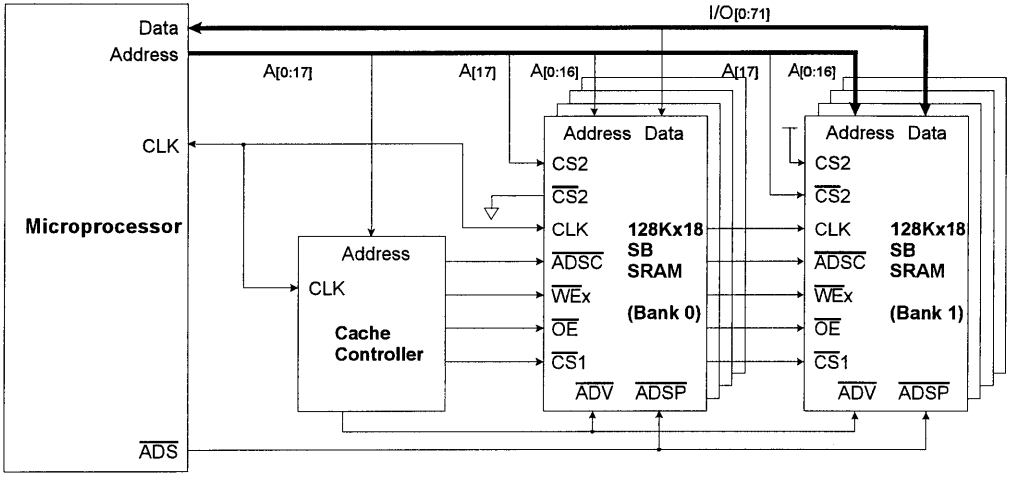
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

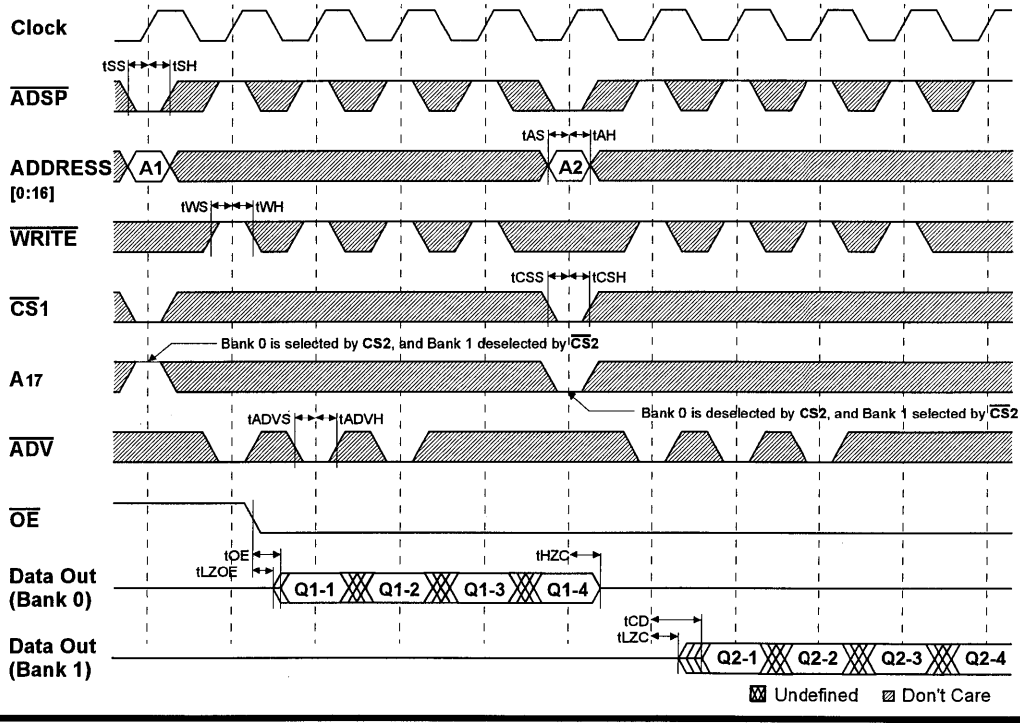
DEPTH EXPANSION

The Samsung 128Kx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.



64Kx36-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- V_{DD}= 3.3V-5%/+10% Power Supple
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2 cycle Enable, 1 cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-7	-8	-10	-11	Unit
Cycle Time	tCYC	7.5	8.6	10	11	ns
Clock Access Time	tCD	4.5	5.0	5.0	6.0	ns
Output Enable Access Time	tOE	4.5	5.0	5.0	6.0	ns

GENERAL DESCRIPTION

The KM736V689/L is a 2,359,296-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 64K words of 36bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, $\overline{LBO}$, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WE}$x and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signals.

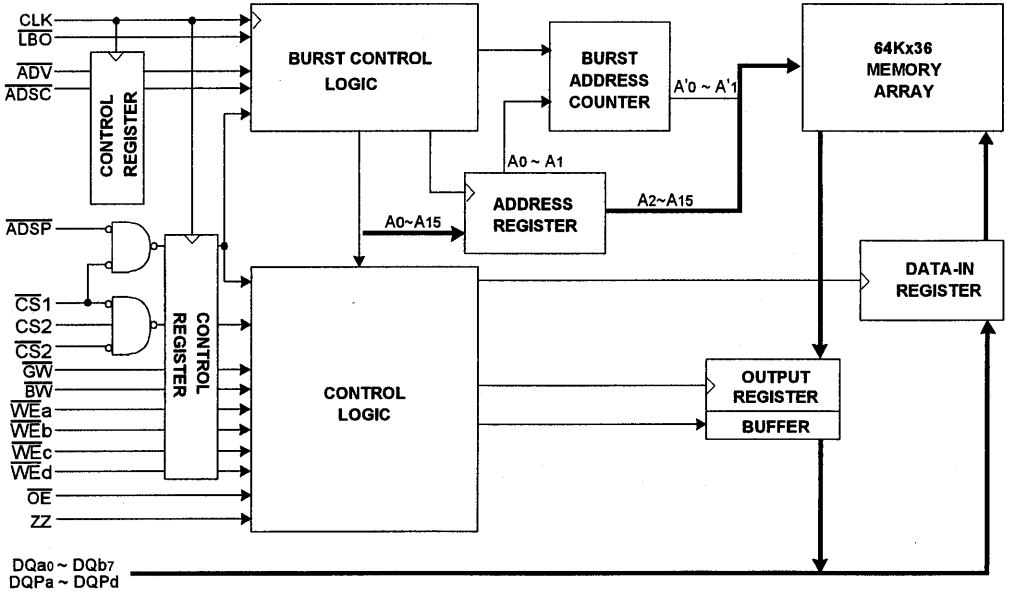
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

$\overline{LBO}$ pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

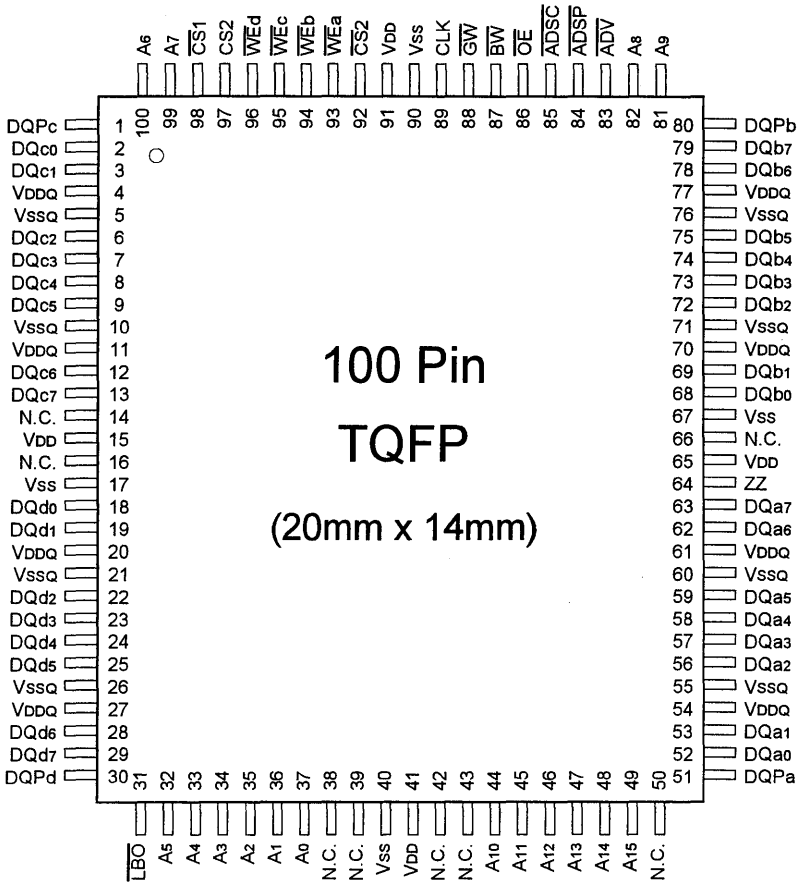
The KM736V689/L is fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A15	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,49, 81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,43,50,66
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa~Pd		51,70,1,20
$\overline{CS2}$	Chip Select	92	VDDQ	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
$\overline{WEx}$	Byte Write Inputs	93,94,95,96			
$\overline{OE}$	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM736V689/L is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(regardless of $\overline{WE}$x and $\overline{ADSC}$) using the new external address clocked into the on-chip address register whenever $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{WE}$x are sampled High and $\overline{ADV}$ is sampled low. And $\overline{ADSP}$ is blocked to control signals by disabling $\overline{CS1}$.

All byte write is done by $\overline{GW}$(regaedless of $\overline{BW}$ and $\overline{WE}$x.), and each byte write is performed by the combination of $\overline{BW}$ and $\overline{WE}$x when $\overline{GW}$ is high.
Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$x. $\overline{WE}$x are ignored on the clock edge that samples $\overline{ADSP}$ low, but are sampled on the subsequent clock edges. The output buffers are disabled when $\overline{WE}$x are sampled Low(regaedless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$x sampled Low. The address increases internally to the next address of burst, if both $\overline{WE}$x and $\overline{ADV}$ are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals($\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c or $\overline{WE}$d) sampled low. The $\overline{WE}$a control DQa_0 ~ DQa_7 and DQPa, $\overline{WE}$b controls DQb_0 ~ DQb_7 and DQPb, $\overline{WE}$c controls DQc_0 ~ DQc_7 and DQPc, and $\overline{WE}$d control DQd_0 ~ DQd_7 and DQPd. Read or write cycle may also be initiated with $\overline{ADSC}$, instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ as are follows;

- $\overline{ADSP}$ must be sampled high when $\overline{ADSC}$ is sampled low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$x are sampled on the same clock edge that sampled $\overline{ADSC}$ low(and $\overline{ADSP}$ high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRIT}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	WRITE	Operation	CS1	WRITE	OE	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.
2. $\overline{WE}$x means $\overline{WE}$a ~ $\overline{WE}$d.

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS ($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.6	V
	V_{DDQ}	3.13	3.3	3.6	V
Ground	Vss	0	0	0	V

CAPACITANCE*(T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***NOTE** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Vss to V_{DD} ; V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT}=Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	-7	-	395	mA
			-8	-	360	
			-10	-	320	
			-11	-	320	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-7	-	100	mA
			-8	-	90	
			-10	-	80	
			-11	-	80	
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	10	mA
			L-Ver	-	5.0	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	10	mA
			L-Ver	-	1.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.0	5.5**	V

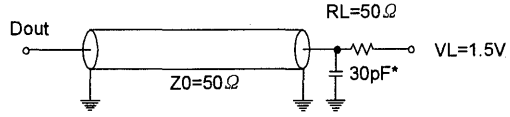
* V_{IL}(min) = -3.0(Pulse Width≤20ns)
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

TEST CONDITIONS

(T_A = 0℃ to 70℃, V_{DD}=3.3V-5%/+10%,unless otherwise specified)

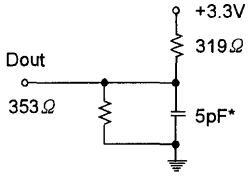
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

Output Load(A)



* Capacitive Load consists of all components of the test environment.

Output Load(B),(3.3V I/O)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS

(V_{DD}=3.3V-5%/+10%, T_A = 0℃ to 70℃)

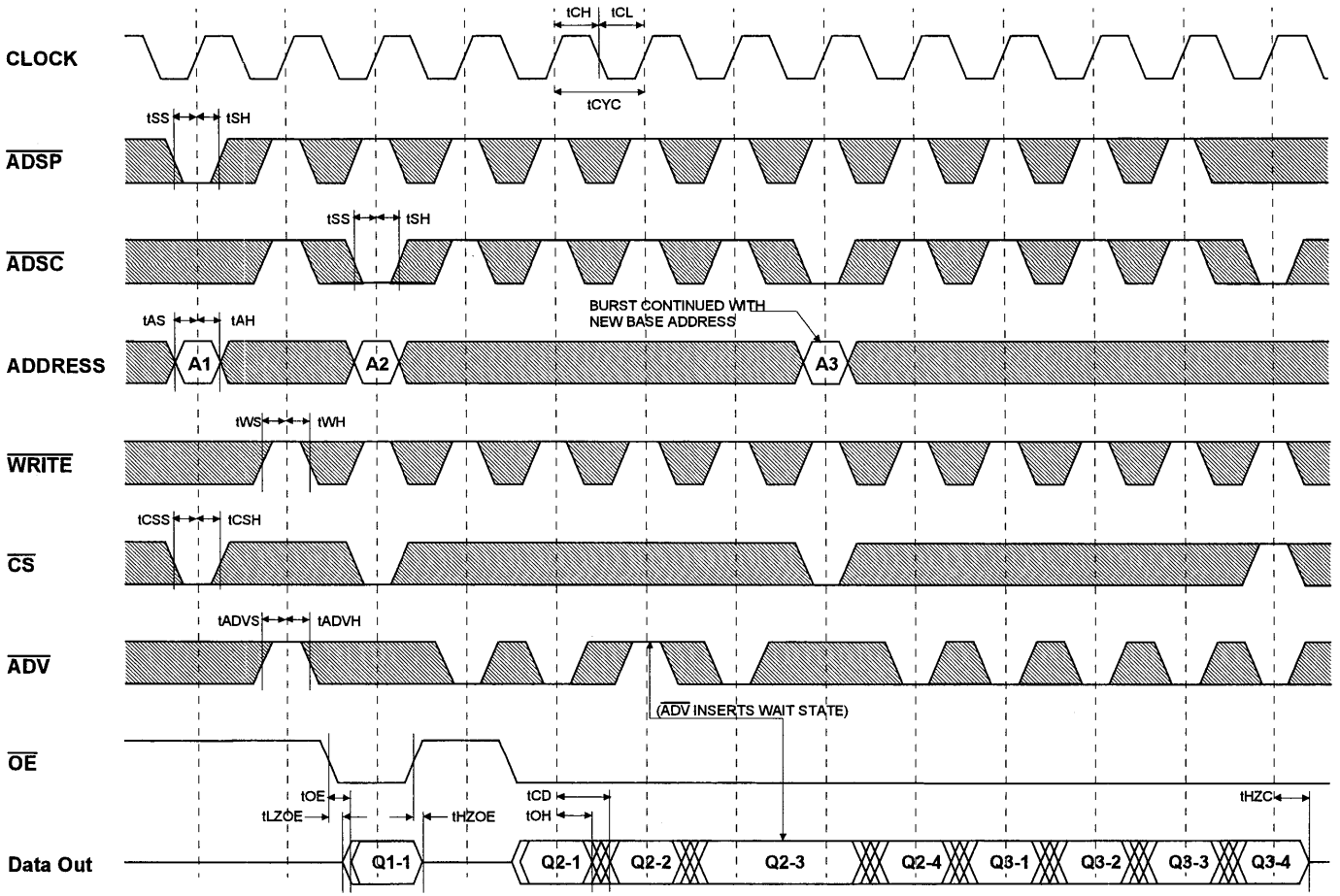
Parameter	Symbol	-7		-8		-10		-11		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	7.5	-	8.6	-	10	-	11	-	ns
Clock Access Time	tCD	-	4.5	-	5.0	-	5.0	-	6.0	ns
Output Enable to Data Valid	tOE	-	4.5	-	5.0	-	5.0	-	6.0	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4.0	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	tHZC	1.5	5.0	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	tCH	3.0	-	3.5	-	4.0	-	4.0	-	ns
Clock Low Pulse Width	tCL	3.0	-	3.5	-	4.0	-	4.0	-	ns
Address Setup to Clock High	tAS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	2.0	-	2.0	-	2.5	-	2.5	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	2	-	cycl
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	2	-	cycl

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

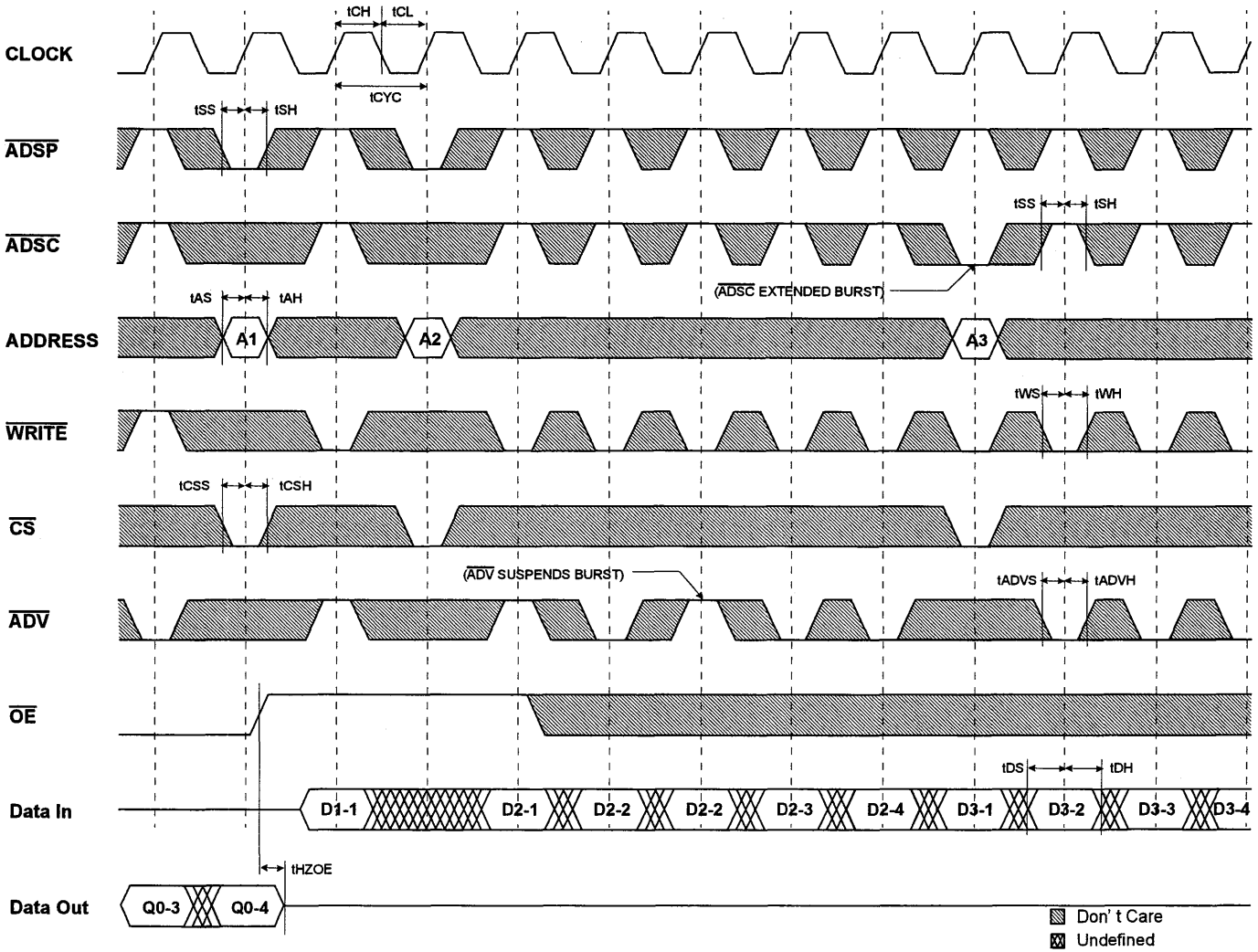
TIMING WAVEFORM OF READ CYCLE



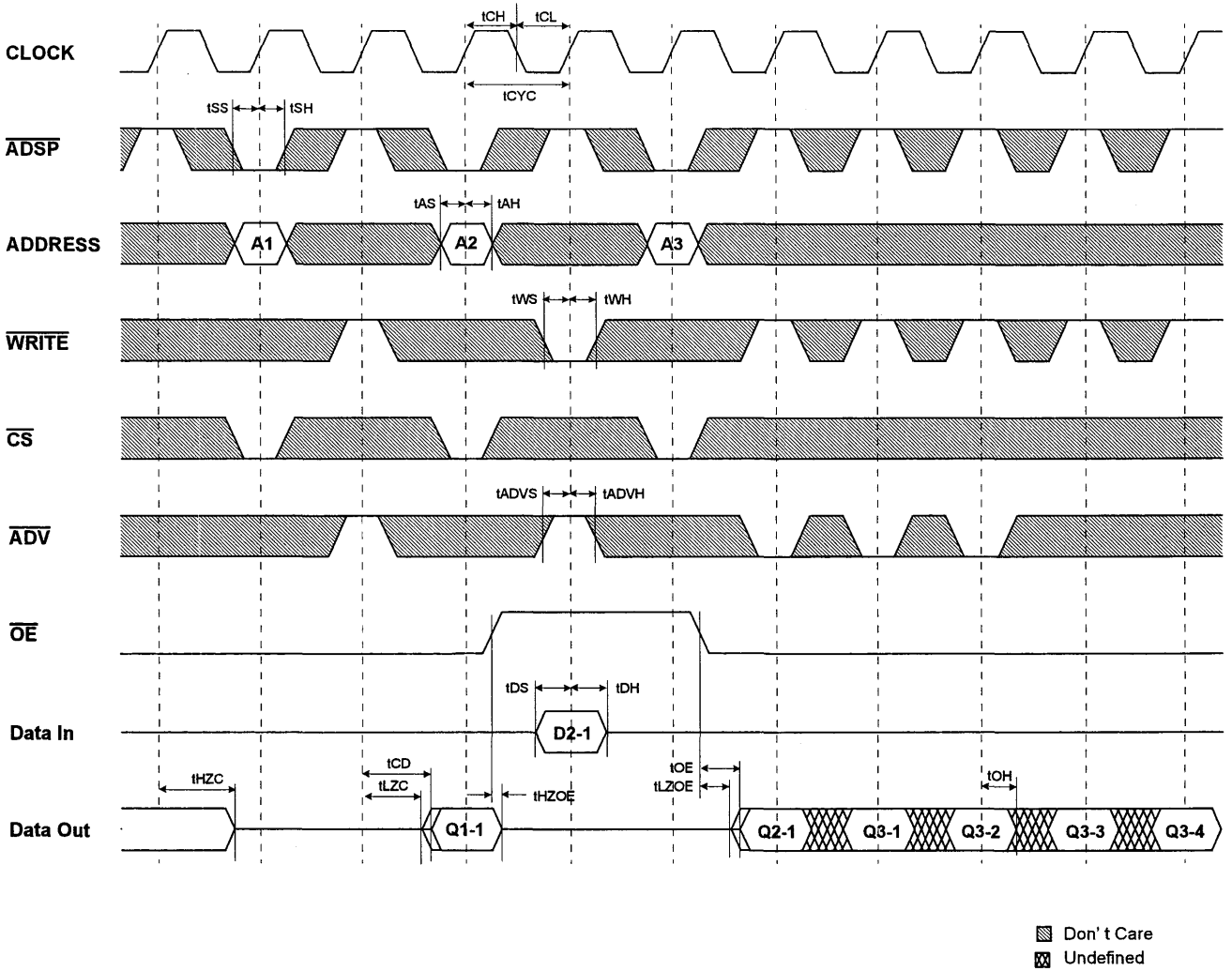
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WEx}$ = L
$\overline{CS}$ = L means $\overline{CS1}$ = L, CS2 = H and $\overline{CS2}$ = L
$\overline{CS}$ = H means $\overline{CS1}$ = H, or $\overline{CS1}$ = L and $\overline{CS2}$ = H, or $\overline{CS1}$ = L, and CS2 = L

Don' t Care
Undefined

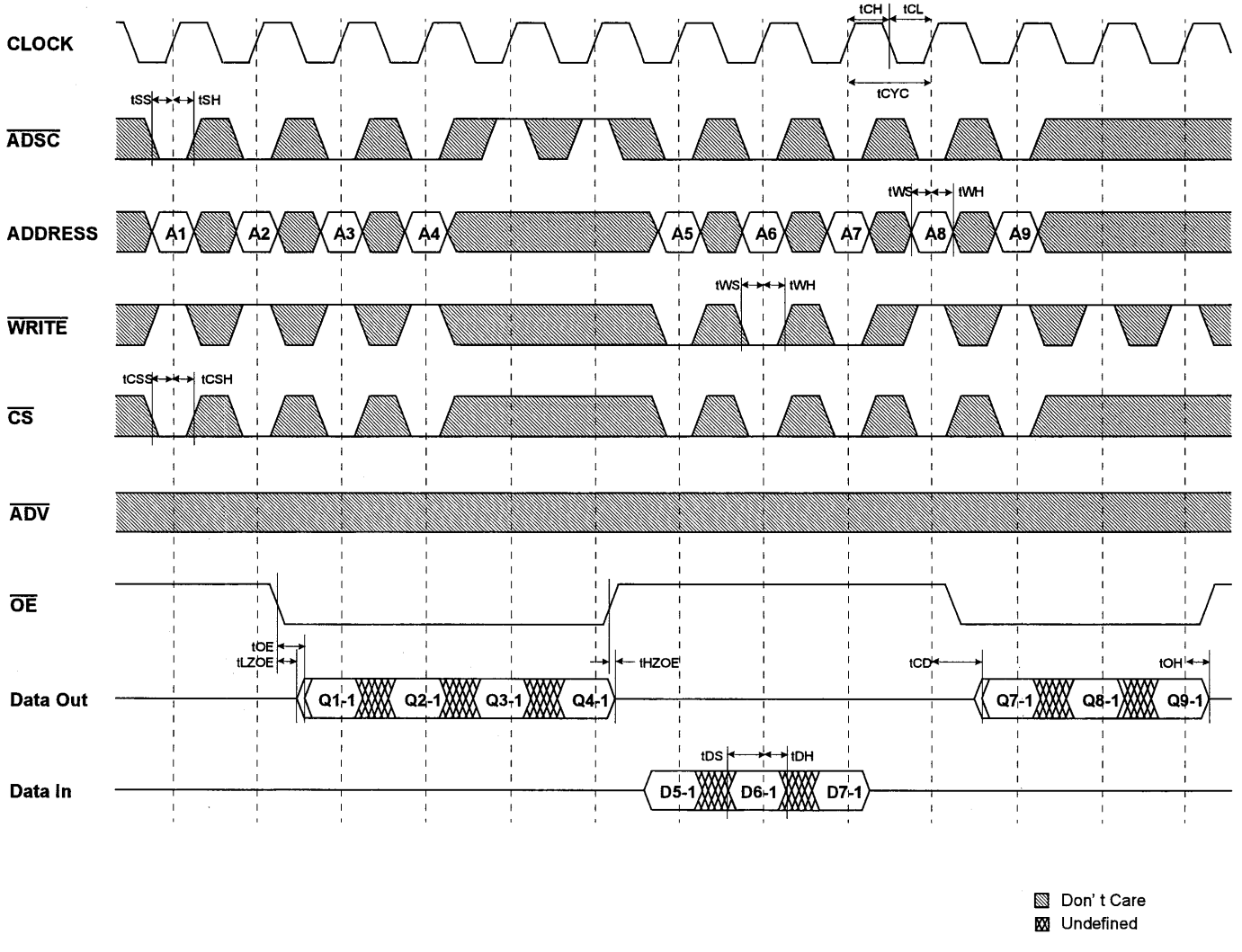
TIMING WAVEFORM OF WRTE CYCLE



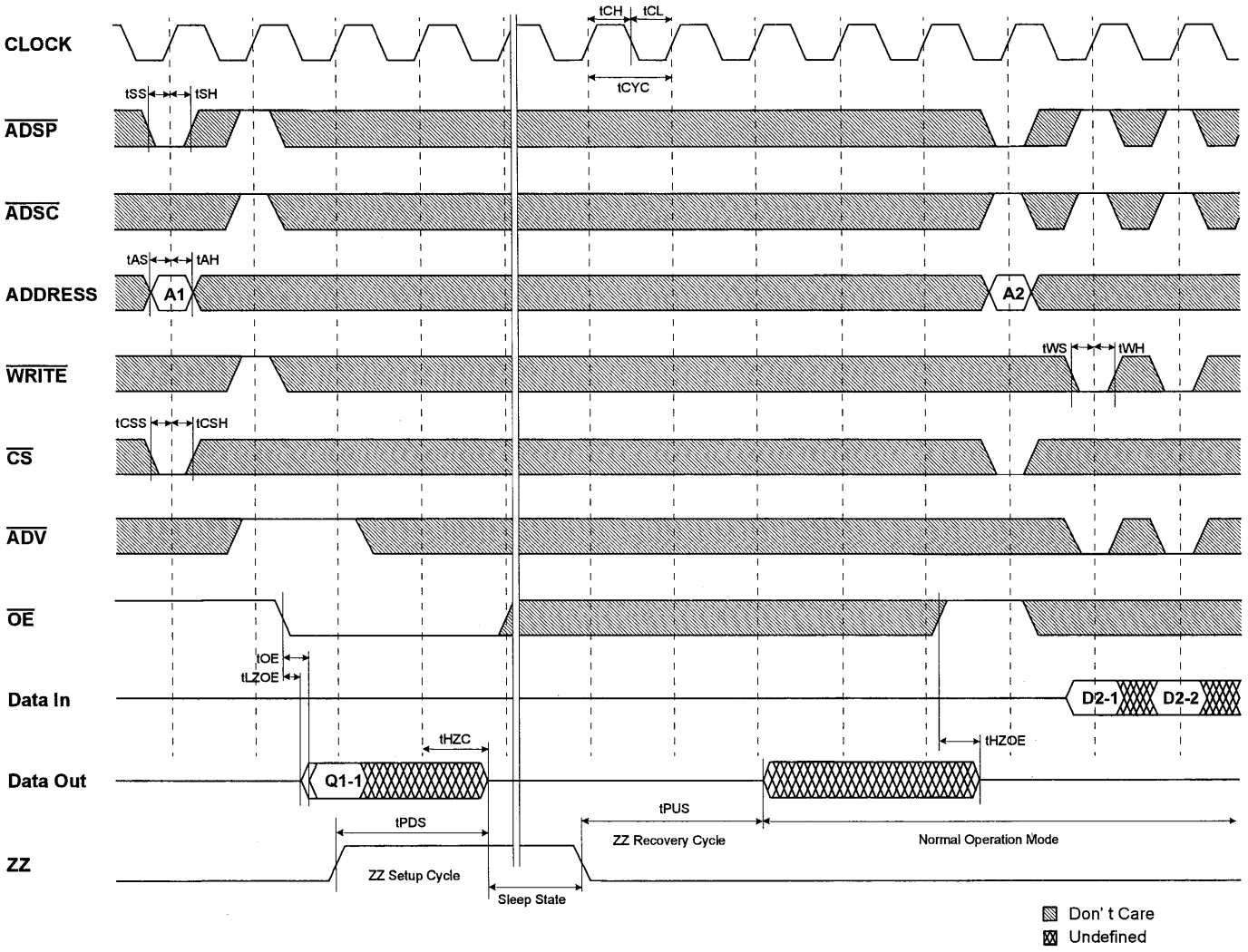
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE



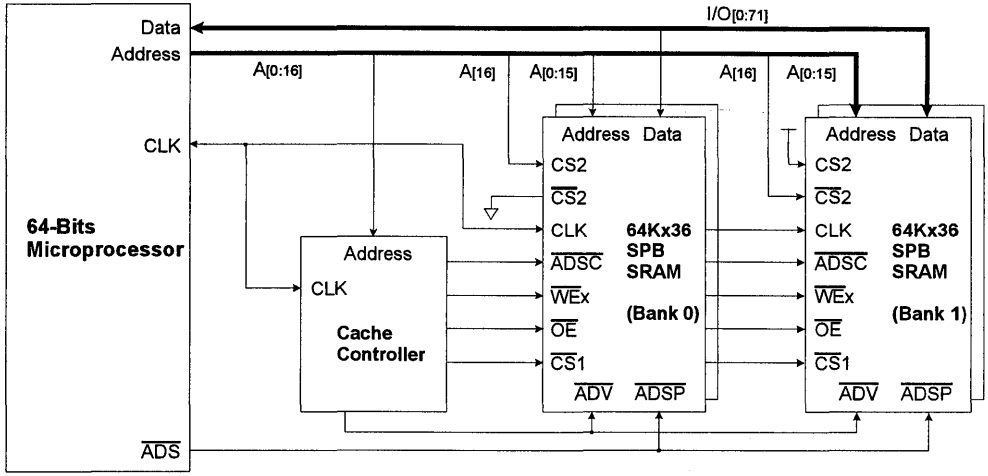
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

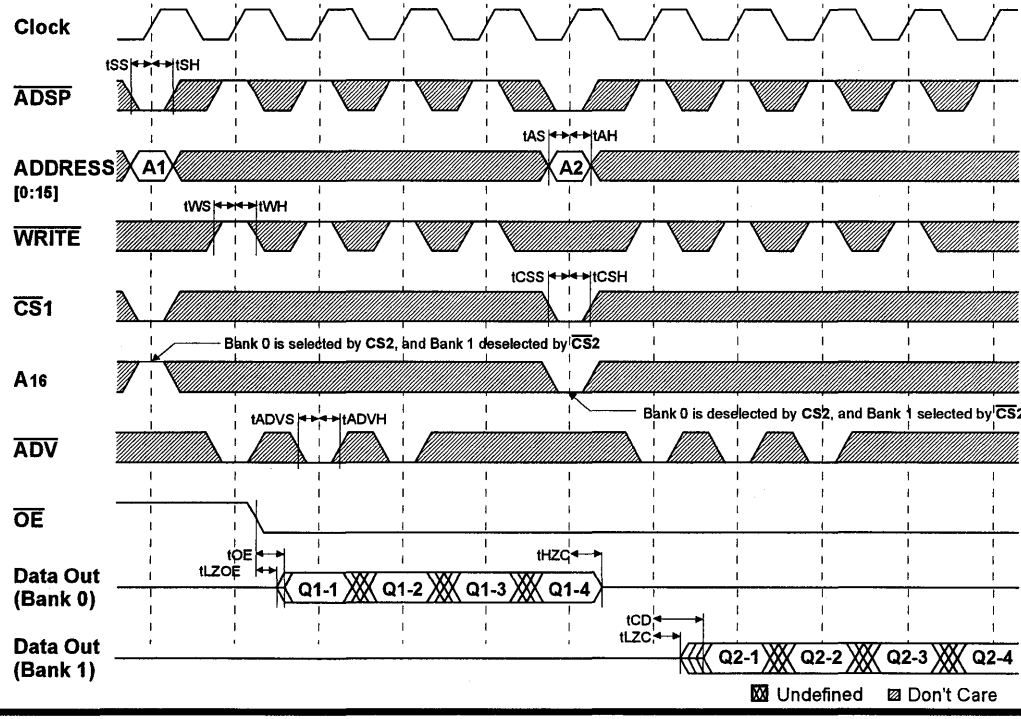
DEPTH EXPANSION

The Samsung 64Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

2 Cycle Enable - 1 Cycle Disable Mode can reduce Data Contention in Dual Bank Operation.



128Kx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- On-Chip Address and Control Registers.
- Single 3.3± 5% Power Supply.
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention.
- TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	Unit
Cycle Time	tCYC	12	12	15	ns
Clock Access Time	tCD	8.5	9	10	ns
Output Enable Access Time	tOE	4	4	5	ns

GENERAL DESCRIPTION

The KM718V787 is a 2,359,296 bit Synchronous Static Random Access Memory designed for support zero wait state performance for advanced Pentium/Power PC address pipelining. And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signal.

It is organized as 128K words of 18 bits and integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components count implementation of high performance cache RAM applications.

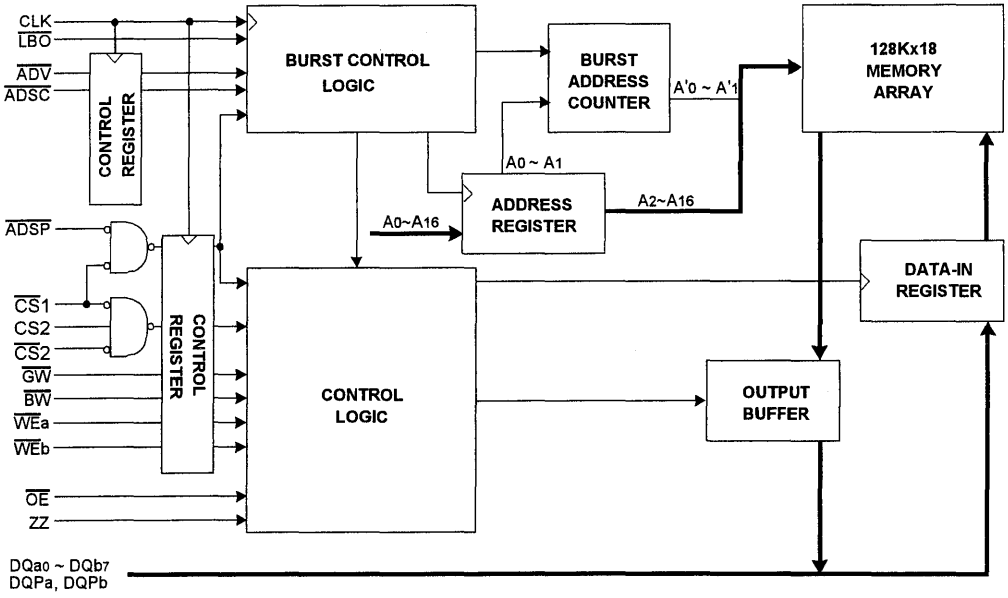
Write cycles are internally self-timed and synchronous.

The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

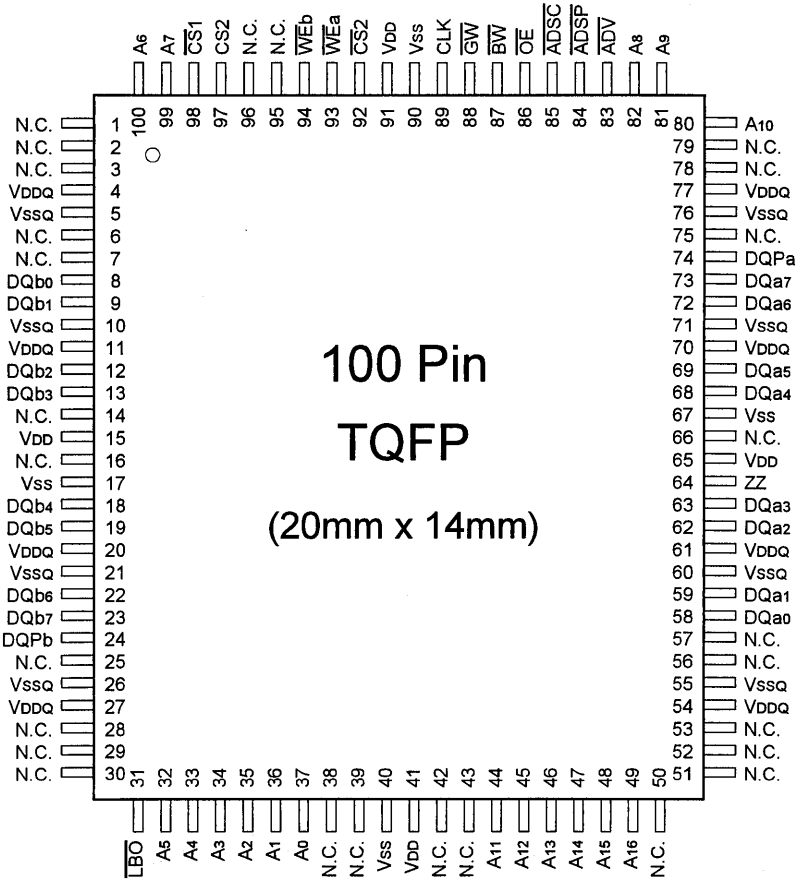
Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input. ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The KM718V787 is implemented in SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A16	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,49, 80,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			Vss	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,14,16,25,28, 29,30,38,39,42,43,50, 51,52,53,56,57,66,75, 78,79,95,96
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85			
CLK	Clock	89	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
$\overline{CS1}$	Chip Select	98	DQb0 ~ b7		8,9,12,13,18,19,22,23
CS2	Chip Select	97	DQPa, Pb		74,24
$\overline{CS2}$	Chip Select	92	VDDQ	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
$\overline{WEx}$	Byte Write Inputs	93,94			
$\overline{OE}$	Output Enable	86	Vssq	Output Ground	5,10,21,26,55,60,71,76
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

SAMSUNG ELECTRONICS

FUNCTION DESCRIPTION

The KM718V787 is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs(with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges.
The start and duration of the burst access is controlled by $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ and Chip Select pins.

When ZZ is pulled HIGH, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and both $\overline{WE}$a and $\overline{WE}$b are high, When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$, the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$(or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation. All byte write occurs by enabling $\overline{GW}$(in dependent of $\overline{BW}$ and $\overline{WE}$x.), and individual byte write is performed only when $\overline{GW}$ is High and $\overline{BW}$ is Low. $\overline{WE}$a controls DQa0 ~ DQa7 and DQPa, $\overline{WE}$b controls DQb0 ~ DQb7 and DQPb.

$\overline{CS1}$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is low, linear burst sequence is selected. And when this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN: HIGH	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN: LOW	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	None	Not Selected
L	L	X	L	X	X	X	↑	None	Not Selected
L	X	H	L	X	X	X	↑	None	Not Selected
L	L	X	X	L	X	X	↑	None	Not Selected
L	X	H	X	L	X	X	↑	None	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑ .

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	Operation
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.47	V
	V_{DDQ}	3.13	3.3	3.47	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

*NOTE : Sampled not 100% tested.

TEST CONDITIONS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%, unless otherwise specified)

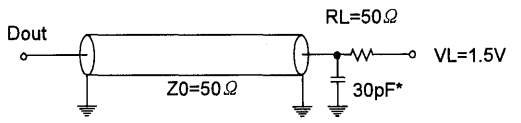
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%)

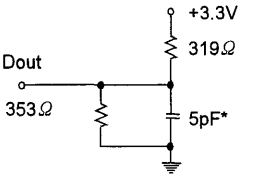
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Max ; V_{IN} = Vss to V_{DD}		-2	2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	-8	-	330	mA
			-9	-	330	
			-10	-	300	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-8	-	80	mA
			-9	-	80	
			-10	-	60	
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs = fixed (V_{DD}-0.2V or 0.2V)		-	10	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.2	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

Output Load(A)



Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%)

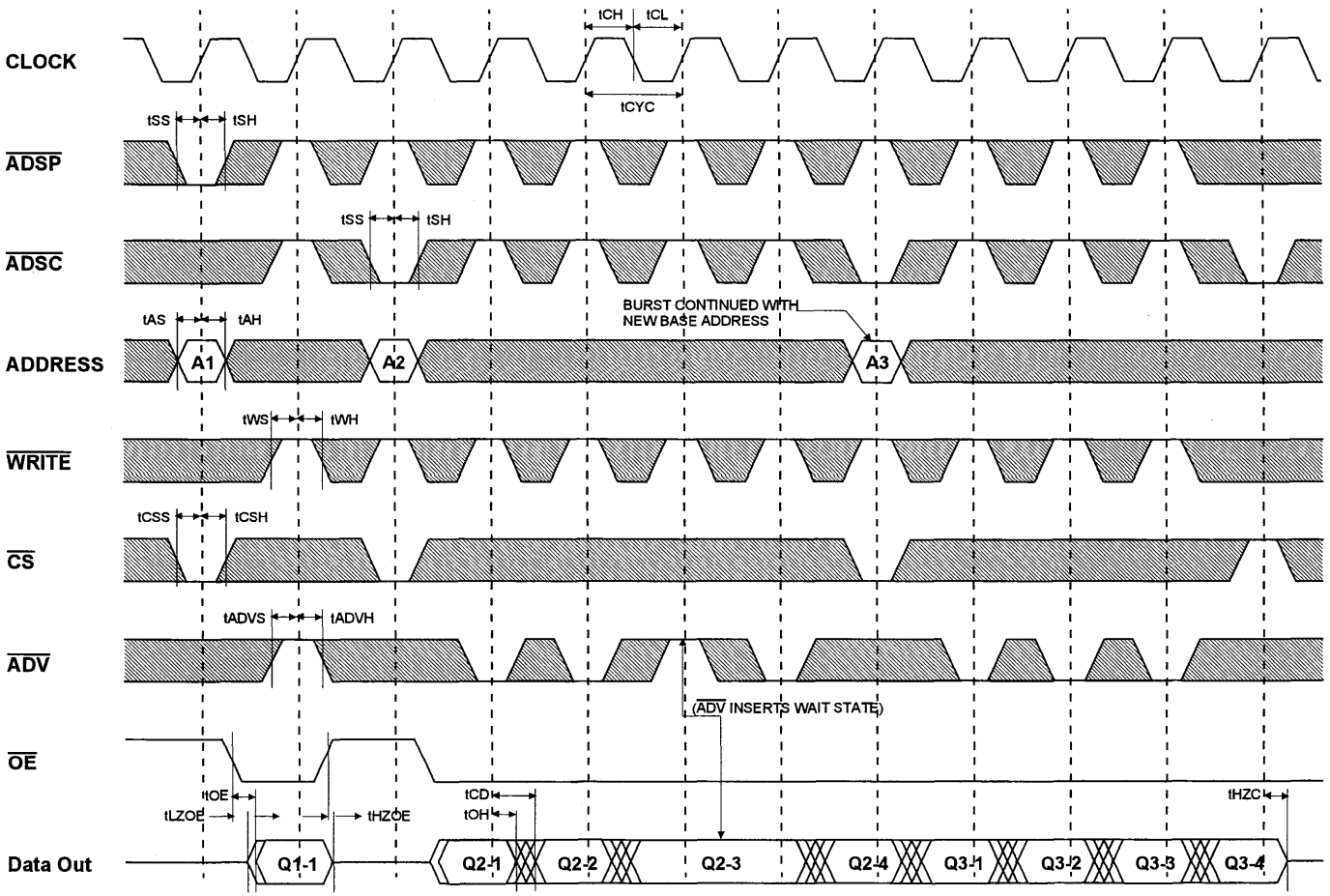
Parameter	Symbol	KM718V787-8		KM718V787-9		KM718V787-10		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	12	-	12	-	15	-	ns
Clock Access Time	tCD	-	8.5	-	9	-	10	ns
Output Enable to Data Valid	tOE	-	4	-	4	-	5	ns
Clock High to Output Low-Z	tLZC	4	-	4	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	5	-	5	-	6	ns
Clock High Pulse Width	tCH	4	-	4	-	5	-	ns
Clock Low Pulse Width	tCL	4	-	4	-	5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

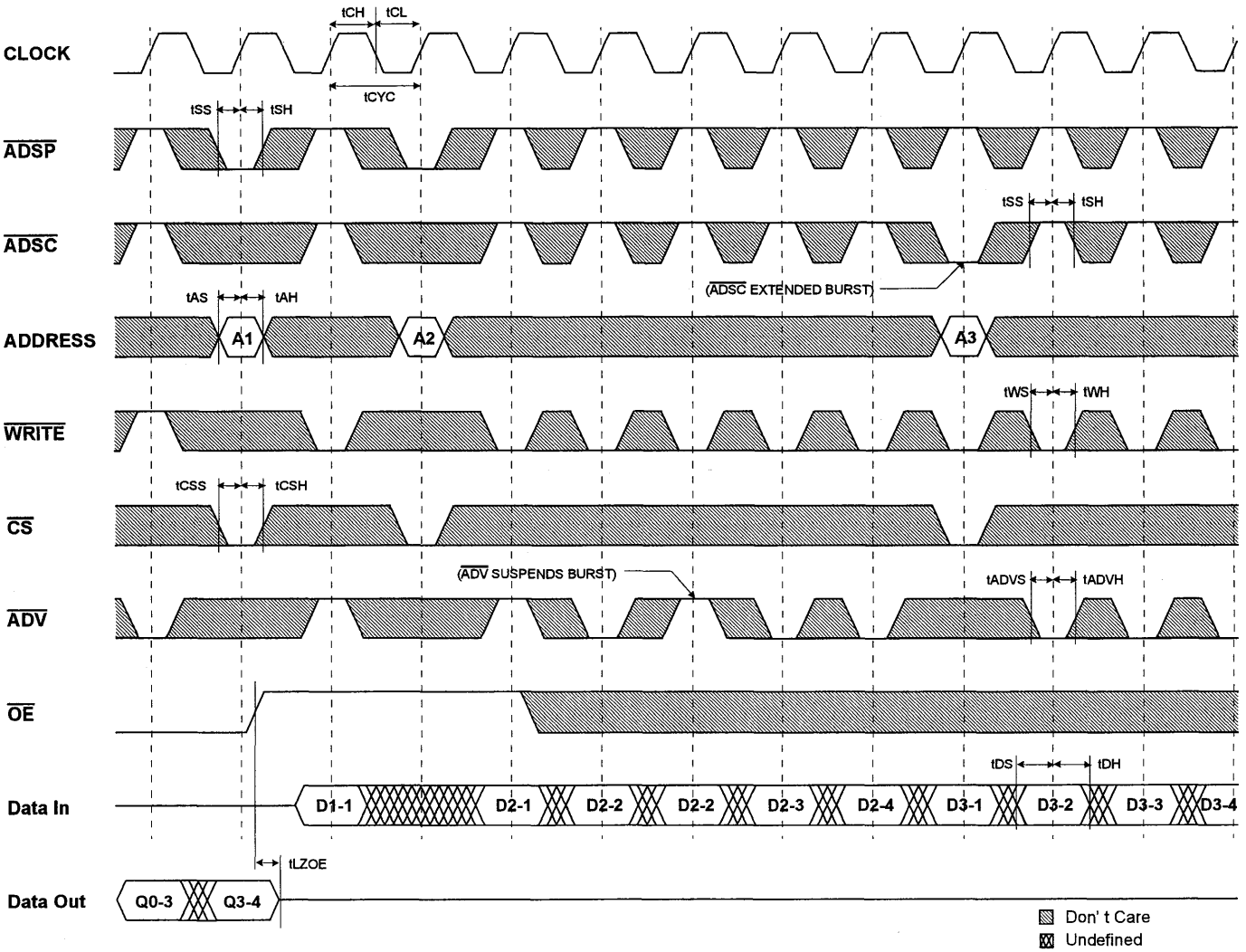
TIMING WAVEFORM OF READ CYCLE



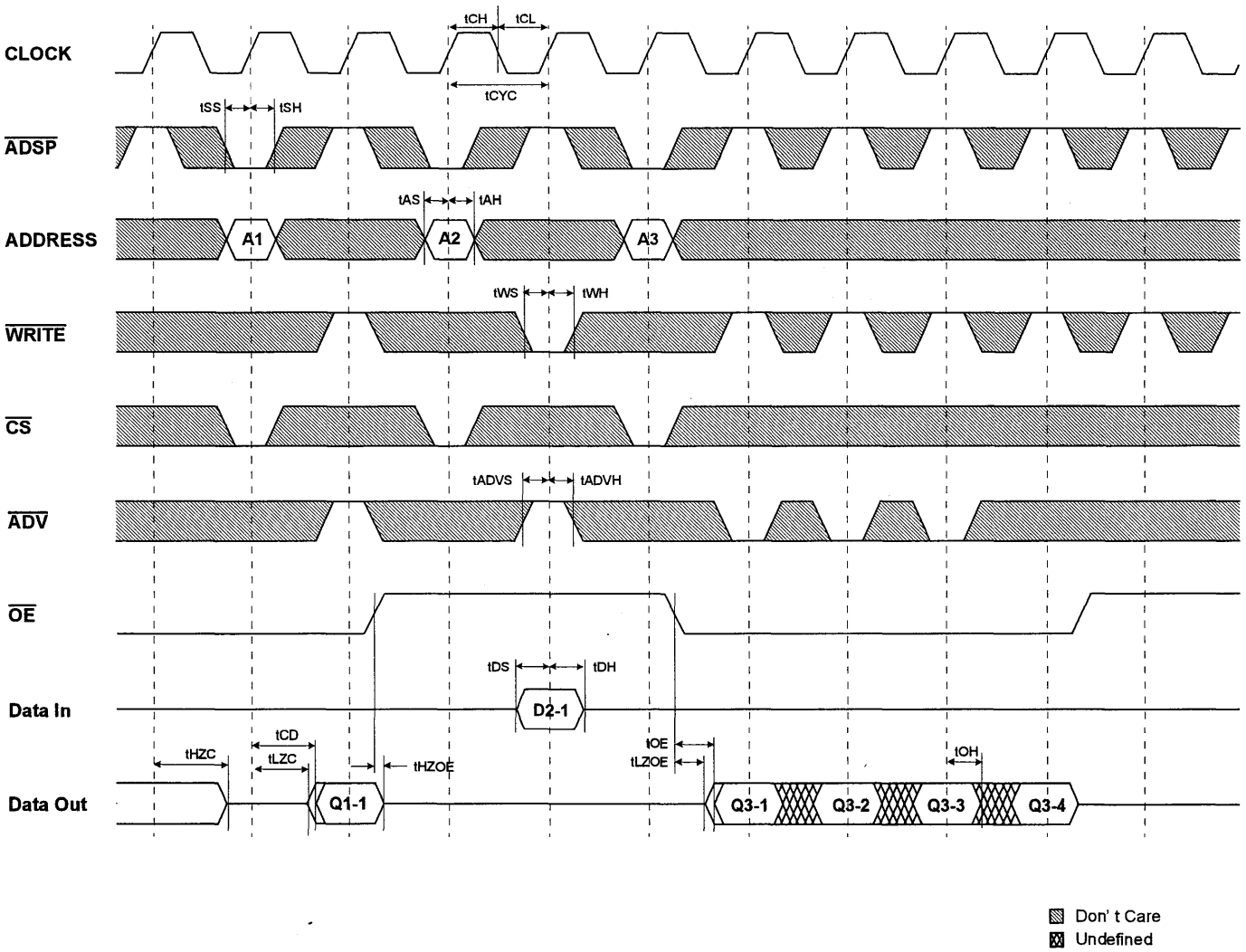
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}$x.= L
$\overline{CS}$ = L means $\overline{CS}$1 = L, CS2 = H and $\overline{CS}$2 = L
$\overline{CS}$ = H means $\overline{CS}$1 = H, or $\overline{CS}$1 = L and $\overline{CS}$2 = H, or $\overline{CS}$1 = L, and CS2 = L

▨ Don' t Care
▩ Undefined

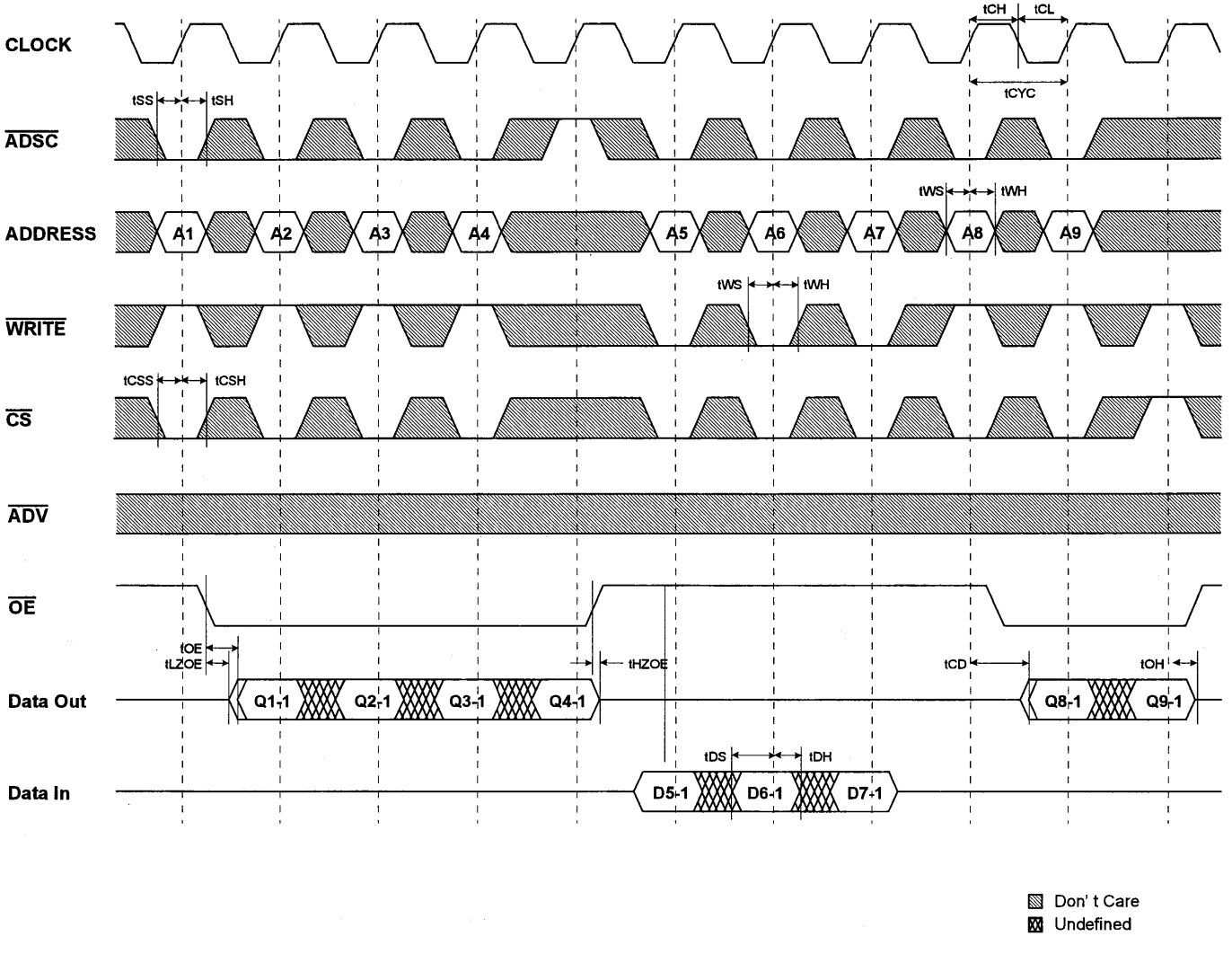
TIMING WAVEFORM OF WRTE CYCLE



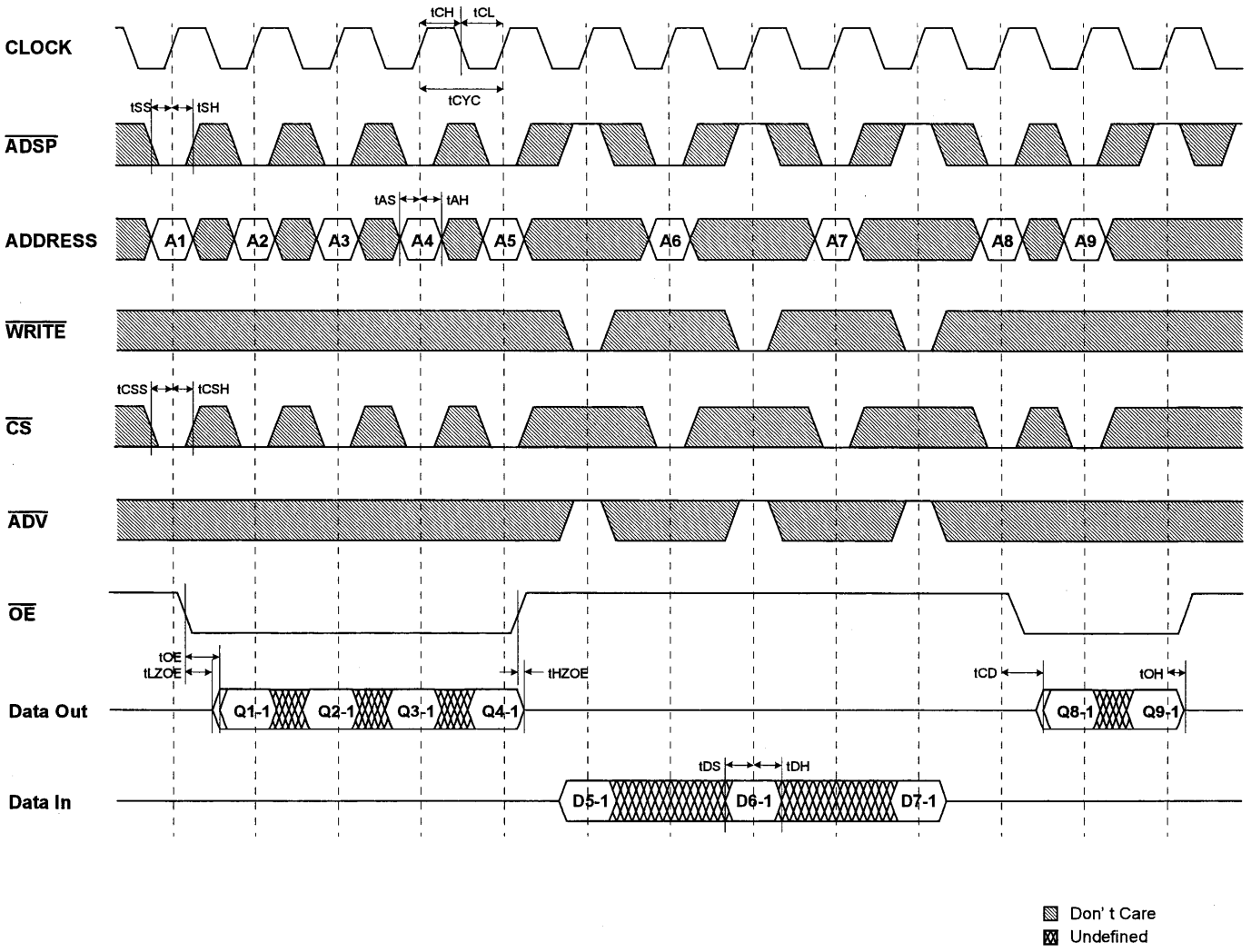
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



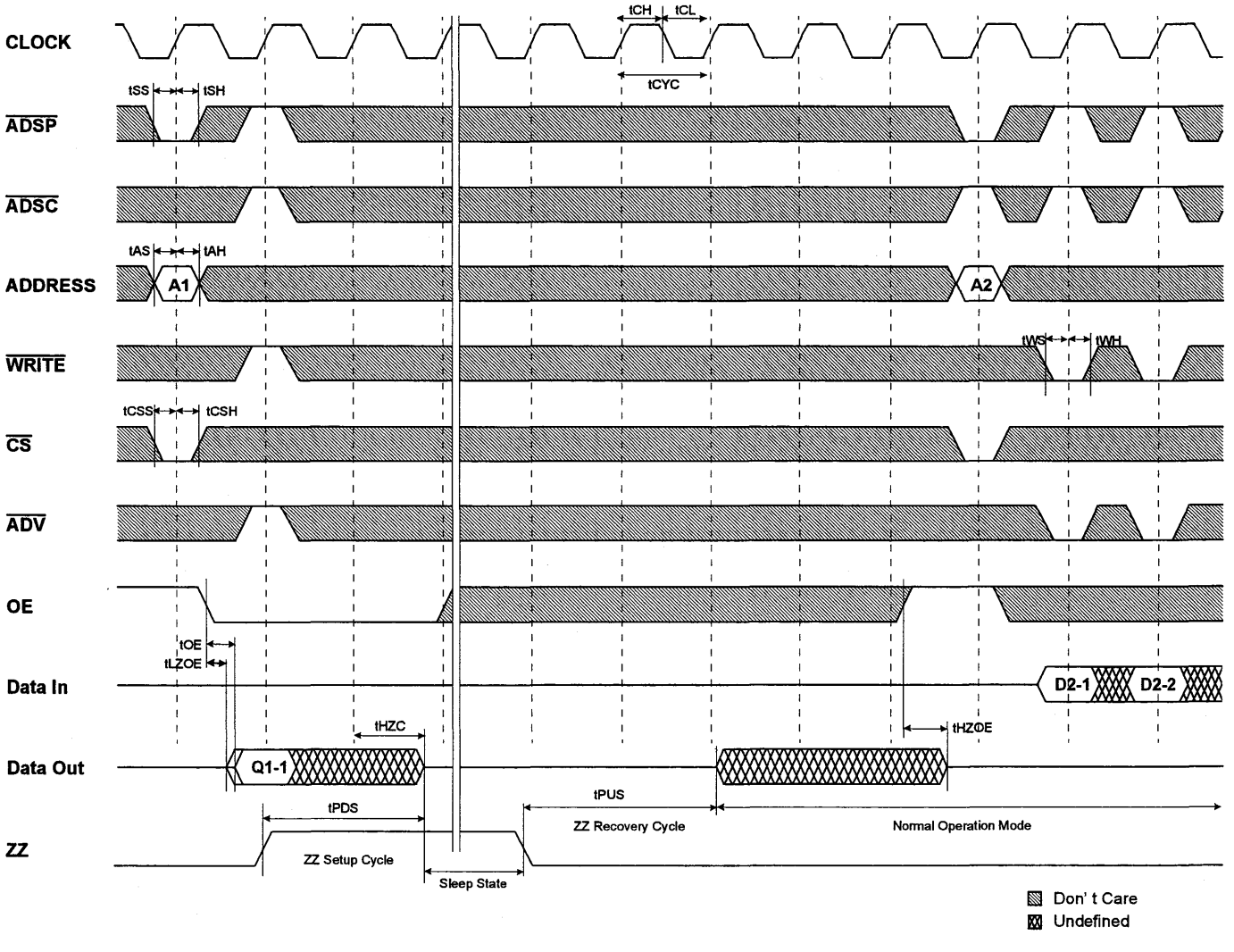
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ CONTROLLED, $\overline{ADSP}$=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



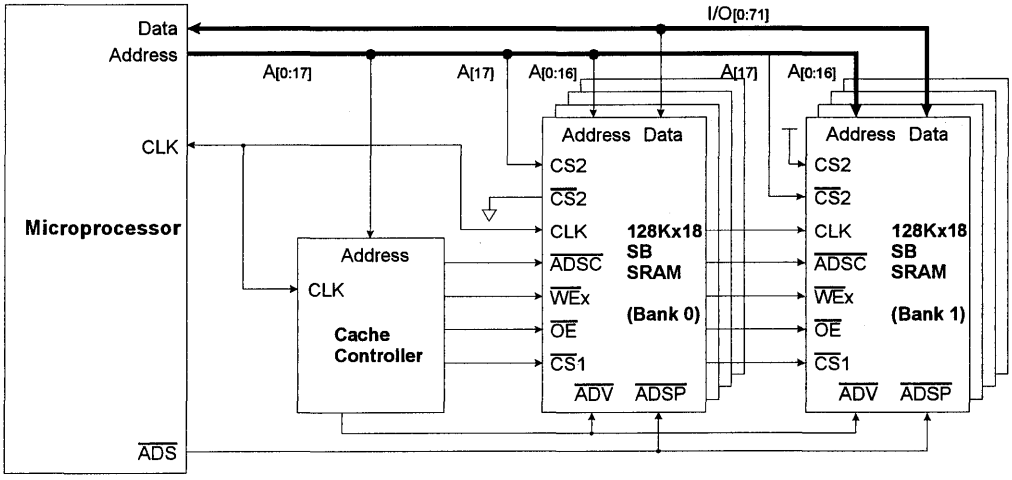
TIMING WAVEFORM OF POWER DOWN CYCLE



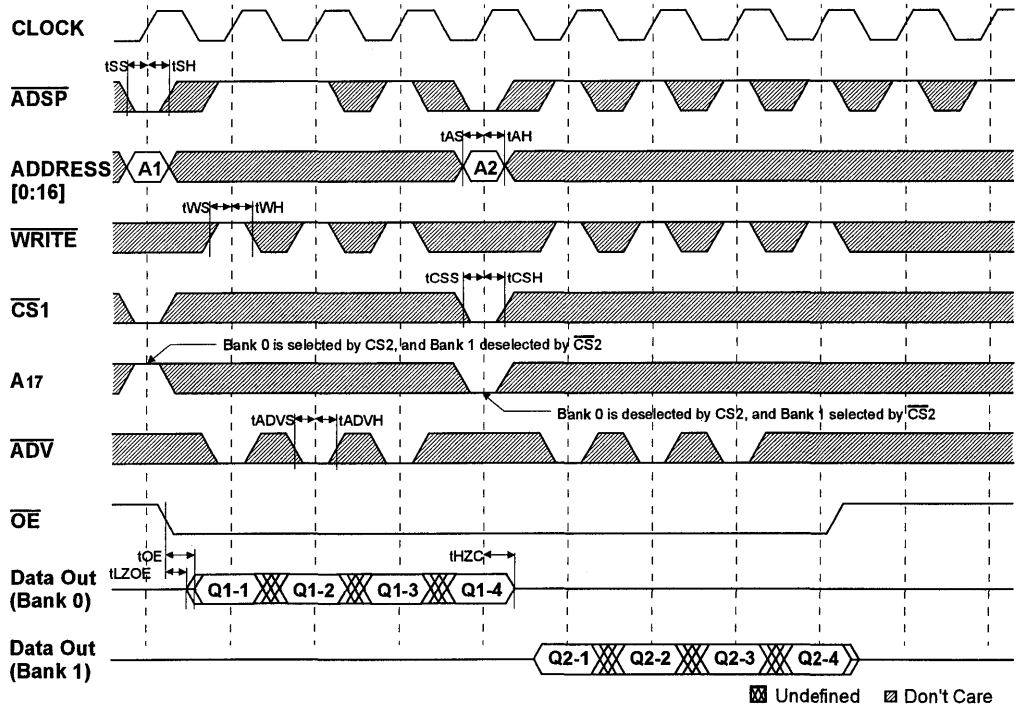
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 128Kx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.



INTERLEAVE READ TIMING (Refer non-interleave write timing for interleave write timing)



64Kx36-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- On-Chip Address and Control Registers.
- Single 3.3V ± 5% Power Supply.
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Burst Control Pins.
- $\overline{LBO}$ Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention.
- TTL-Level Three-State Output.
- 100-Pin TQFP Package

FAST ACCESS TIMES

Parameter	Symbol	-8	-9	-10	Unit
Cycle Time	tCYC	12	12	15	ns
Clock Access Time	tCD	8.5	9	10	ns
Output Enable Access Time	tOE	4	4	5	ns

GENERAL DESCRIPTION

The KM736V687 is 2,359,296 bits Synchronous Static Random Access Memory designed to support zero wait state performance for advanced Pentium/Power PC based system. And with $\overline{CS1}$ high, $\overline{ADSP}$ is blocked to control signals.

It can be organized as 64K words of 36 bits. And it integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components counts implementation of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous.

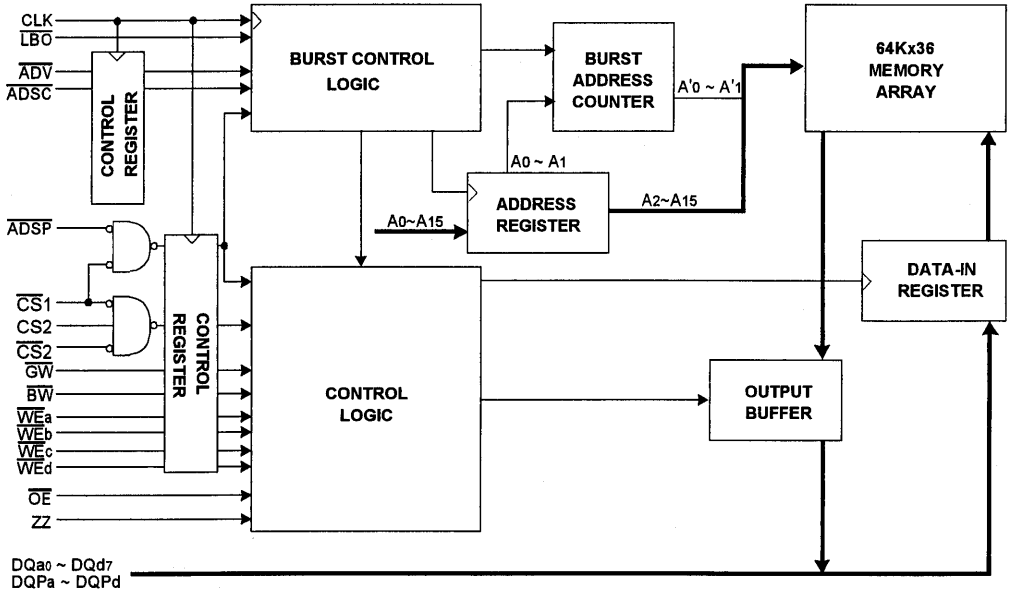
The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

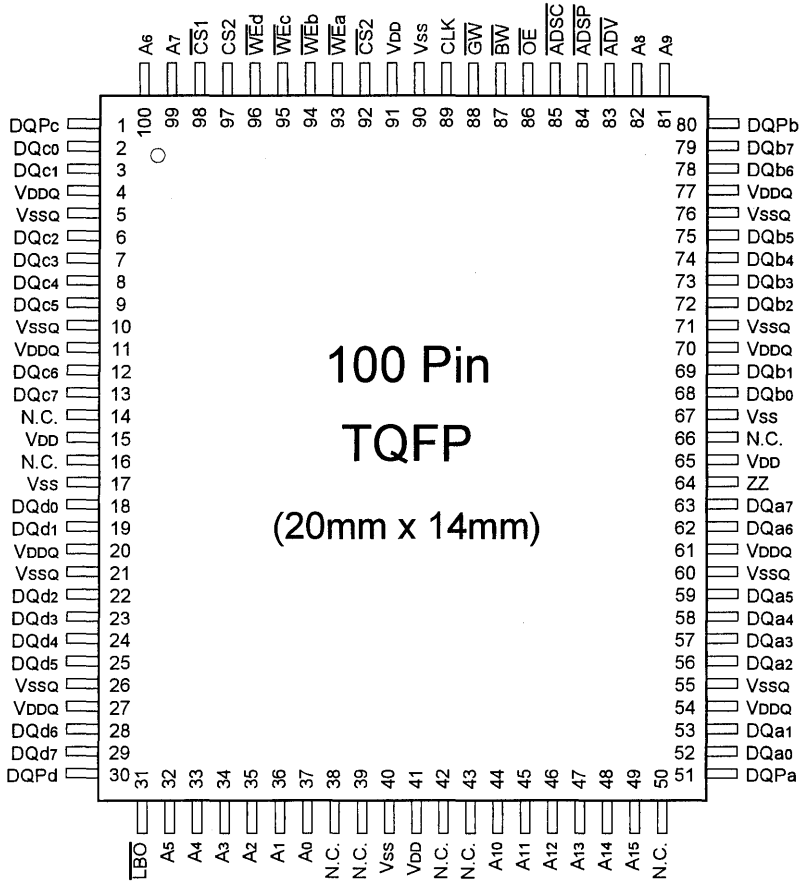
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The KM736V687 is implemented with SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A15	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,49, 81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,43,50,66
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84	DQa0 ~ a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
$\overline{ADSC}$	Address Status Controller	85	DQb0 ~ b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0 ~ c7		2,3,6,7,8,9,12,13
$\overline{CS1}$	Chip Select	98	DQd0 ~ d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa~Pd		51,80,1,30
$\overline{CS2}$	Chip Select	92			
$\overline{WEx}$	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
$\overline{BW}$	Byte Write Enable	87			
ZZ	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

FUNCTION DESCRIPTION

The KM736V687 is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c, and $\overline{WE}$d are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$(or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.
All byte write occurs by enabling $\overline{GW}$(independent of $\overline{BW}$ and $\overline{WE}$x.), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In KM736V687, a 64Kx36 organization, $\overline{WE}$a controls DQa0 ~ DQa7 and DQPa, $\overline{WE}$b controls DQb0 ~ DQb7 and DQPb, $\overline{WE}$c controls DQc0 ~ DQc7 and DQPc and $\overline{WE}$d controls DQd0 ~ DQd7 and DQPd.

$\overline{CS}$1 is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : 1. $\overline{LBO}$ pin must be tied to high or low, and floating state must not be allowed.

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

SYNCHRONOUS TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{CS2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

NOTE : 1. X means "Don't Care".

2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

NOTE : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ABSOLUTE MAXIMUM RATING*

Parameter	Symbol	Rating	Unit
Voltage on V_{DD} Supply Relative to Vss	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to Vss	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to Vss	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

***NOTE** : Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0℃ \leq T_A \leq 70℃$)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.13	3.3	3.47	V
	V_{DDQ}	3.13	3.3	3.47	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A = 25℃, f = 1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

*NOTE : Sampled not 100% tested.

TEST CONDITIONS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%, unless otherwise specified)

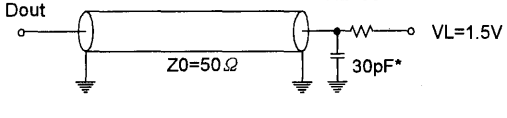
Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

DC ELECTRICAL CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%)

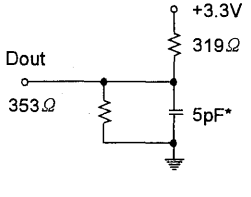
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Max , V_{IN} = Vss to V_{DD}		-2	+2	μA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT} = Vss to V_{DDQ}		-2	+2	μA
Operating Current	I_{CC}	Device Selected, I_{OUT} = 0mA, ZZ≤V_{IL}, All Inputs = V_{IL} or V_{IH} Cycle Time ≥ tCYC min	-8	-	330	mA
			-9	-	330	
			-10	-	300	
Standby Current	I_{SB}	Device deselected, I_{OUT} = 0mA, ZZ≤V_{IL}, f = Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-8	-	80	mA
			-9	-	80	
			-10	-	60	
	I_{SB1}	Device deselected, I_{OUT} = 0mA, ZZ≤0.2V, f = 0, All Inputs = fixed (V_{DD}-0.2V or 0.2V)		-	10	mA
	I_{SB2}	Device deselected, I_{OUT} = 0mA, ZZ≥V_{DD}-0.2V, f = Max, All Inputs≤V_{IL} or ≥V_{IH}		-	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Input Low Voltage	V_{IL}			-0.5*	0.8	V
Input High Voltage	V_{IH}			2.2	5.5**	V

* V_{IL}(min) = -3.0(Pulse Width≤20ns)
** In Case of I/O Pins, the Max. V_{IH} = V_{DDQ} + 0.5V

Output Load(A)



Output Load(B)
(for tLZC, tLZOE, tHZOE& tHZC)



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS(T_A = 0℃ to 70℃, V_{DD} = 3.3V±5%)

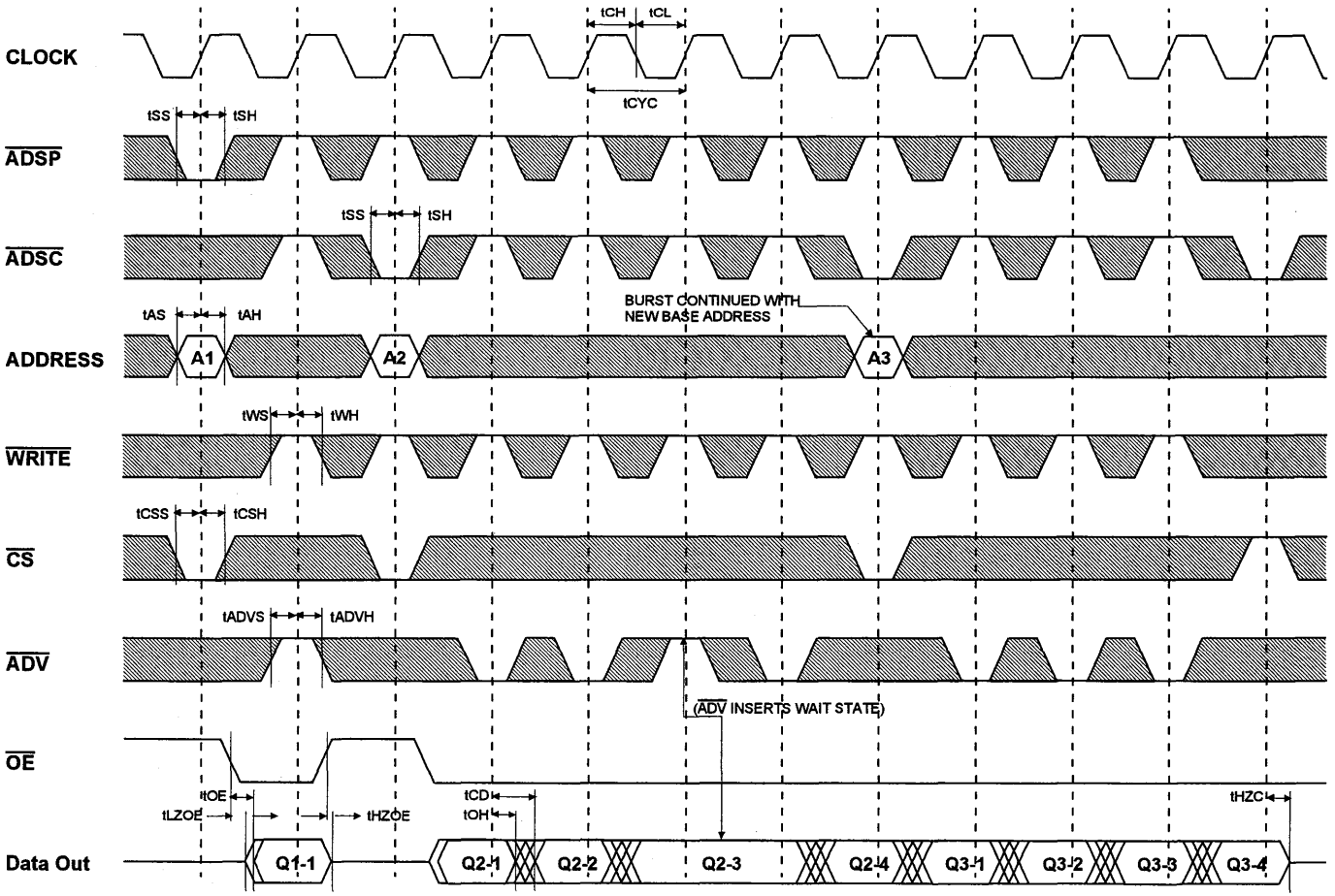
Parameter	Symbol	KM736V687-8		KM736V687-9		KM736V687-10		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	12	-	12	-	15	-	ns
Clock Access Time	tCD	-	8.5	-	9	-	10	ns
Output Enable to Data Valid	tOE	-	4	-	4	-	5	ns
Clock High to Output Low-Z	tLZC	4	-	4	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	5	2	5	ns
Clock High to Output High-Z	tHZC	-	5	-	5	-	6	ns
Clock High Pulse Width	tCH	4	-	4	-	5	-	ns
Clock Low Pulse Width	tCL	4	-	4	-	5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	2.5	-	ns
Address Status Setup to Clock High	tSS	2.5	-	2.5	-	2.5	-	ns
Data Setup to Clock High	tDS	2.5	-	2.5	-	2.5	-	ns
Write Setup to Clock High	tWS	2.5	-	2.5	-	2.5	-	ns
Address/Advance Setup to Clock High	tADVS	2.5	-	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

NOTE : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

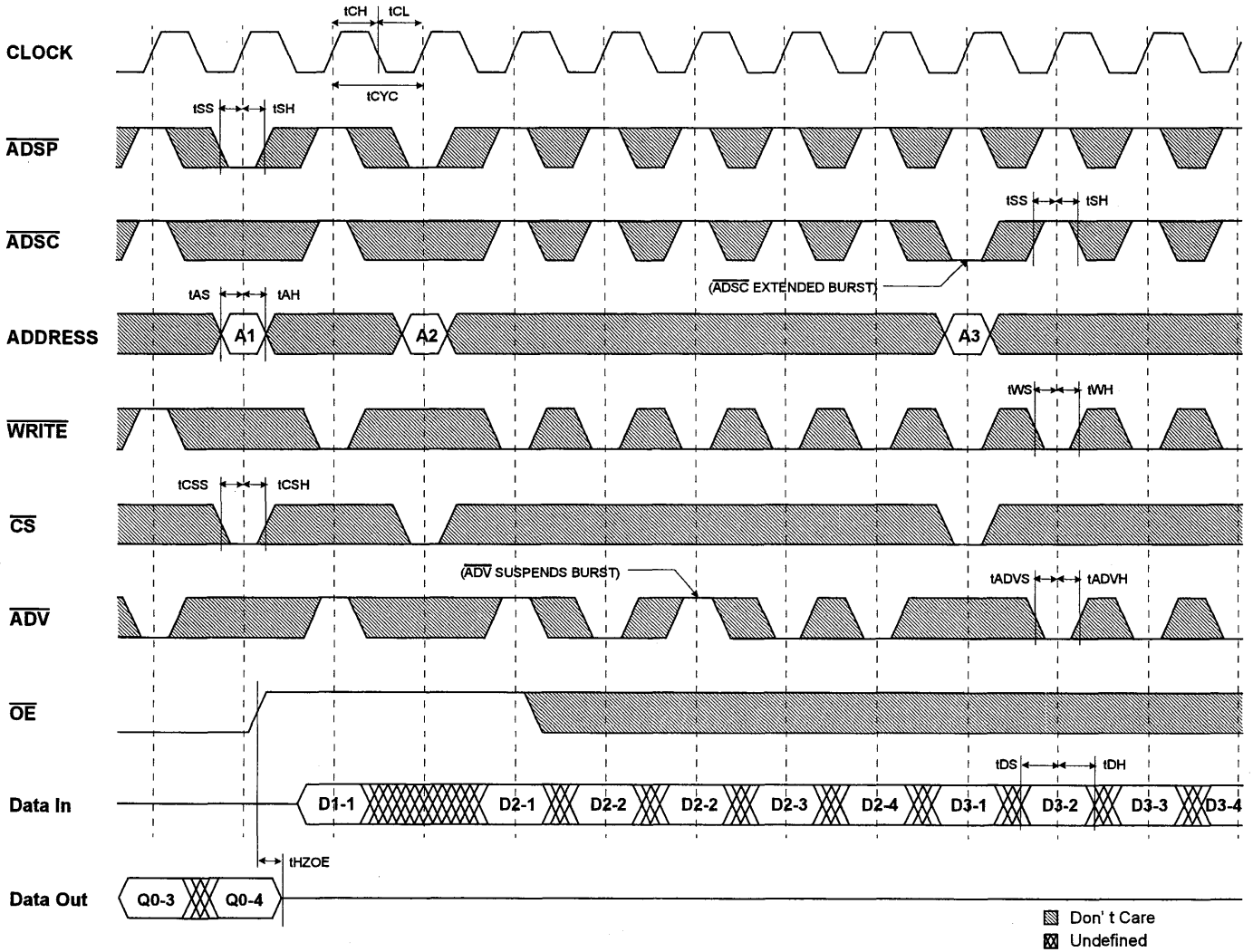
TIMING WAVEFORM OF READ CYCLE



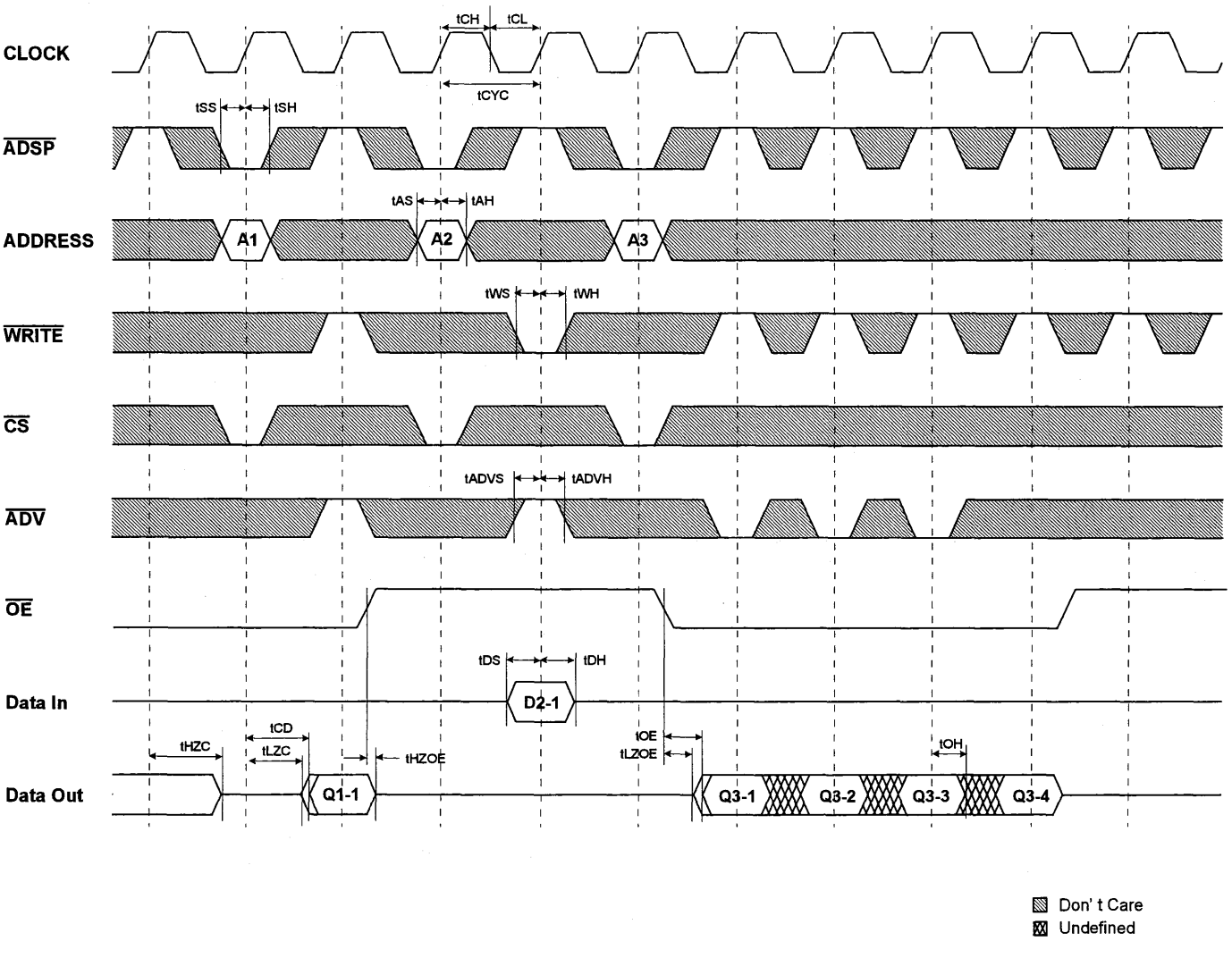
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE}$x.= L
$\overline{CS}$ = L means $\overline{CS}$1 = L, CS2 = H and $\overline{CS}$2 = L
$\overline{CS}$ = H means $\overline{CS}$1 = H, or $\overline{CS}$1 = L and $\overline{CS}$2 = H, or $\overline{CS}$1 = L, and CS2 = L

▨ Don' t Care
▩ Undefined

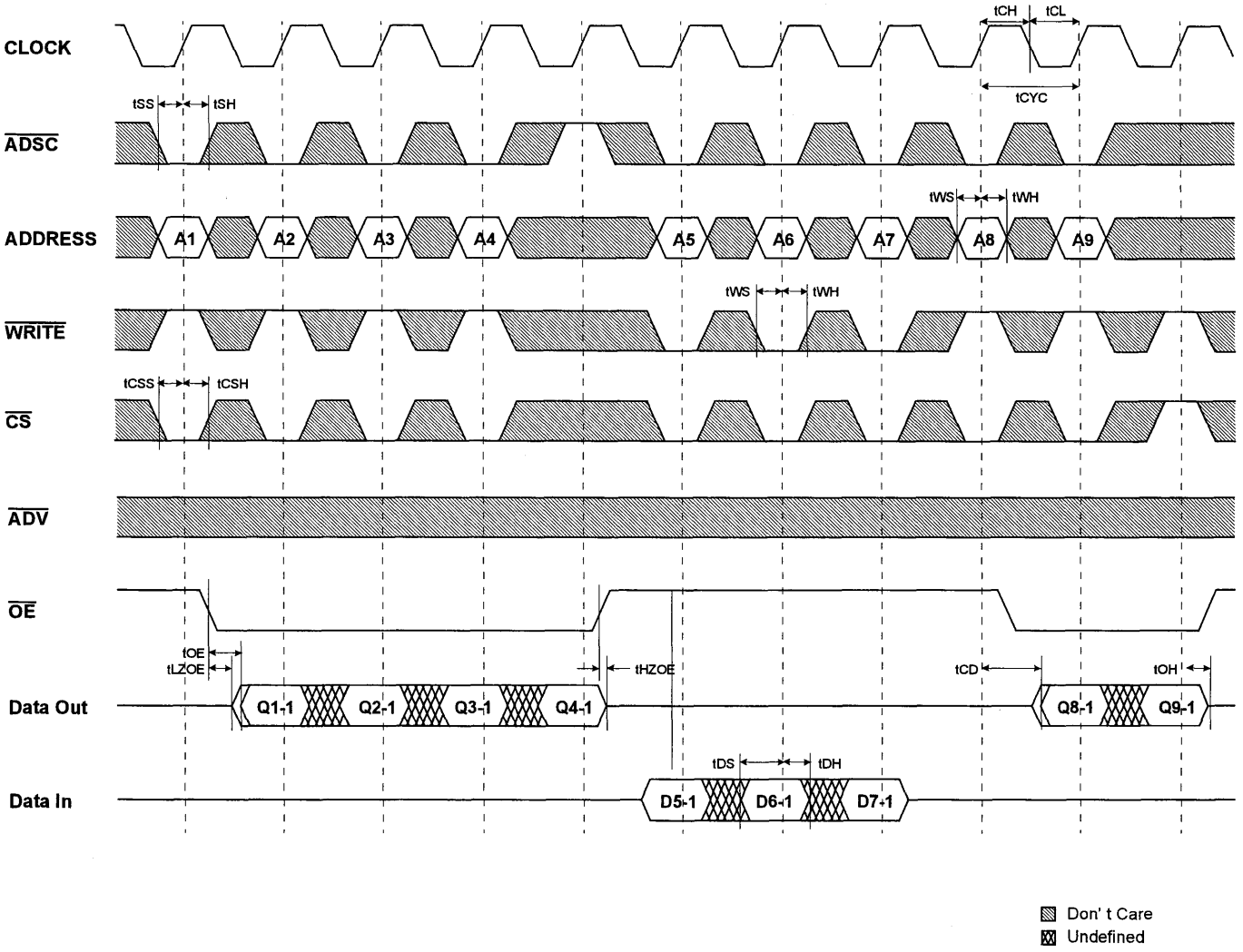
TIMING WAVEFORM OF WRTE CYCLE



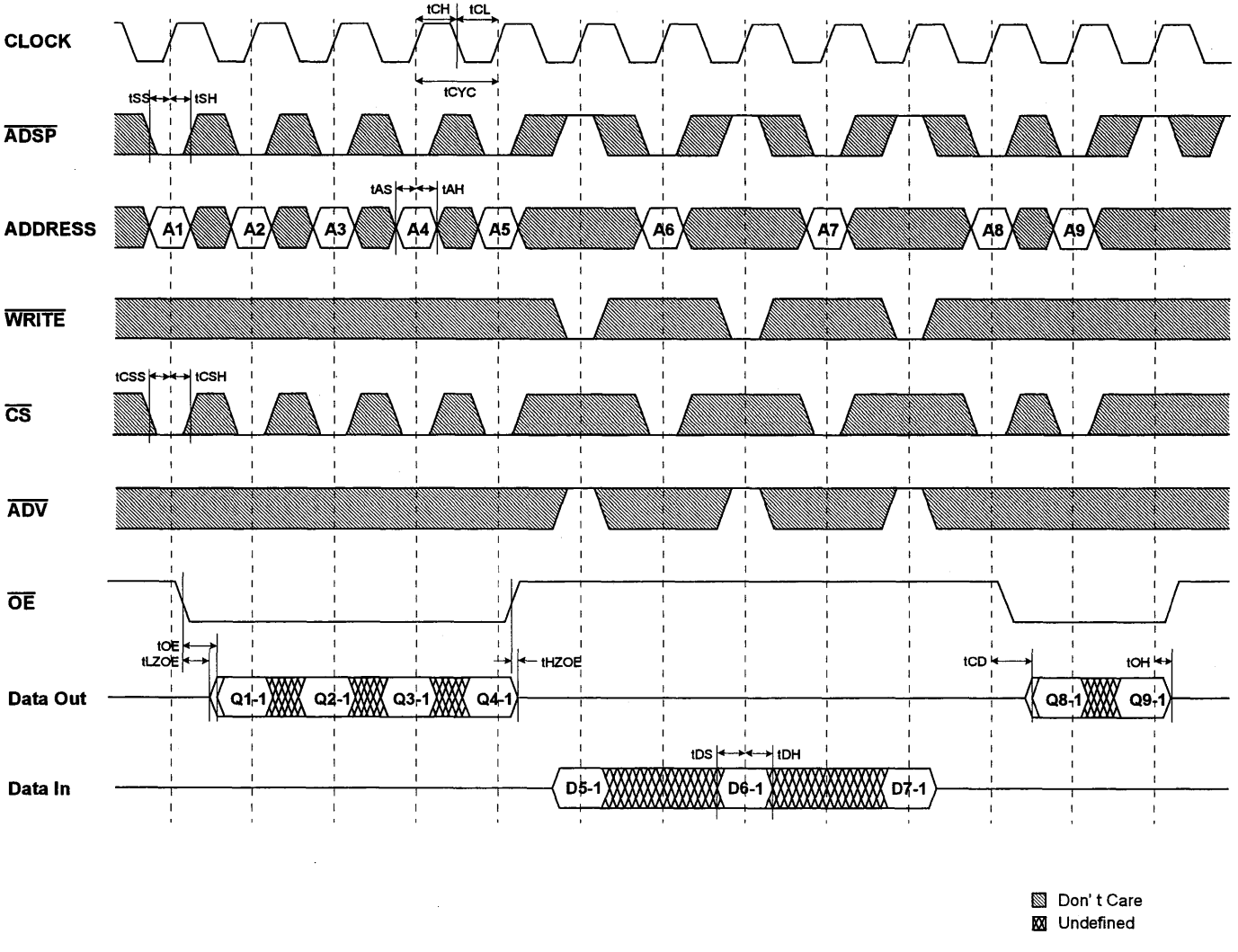
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



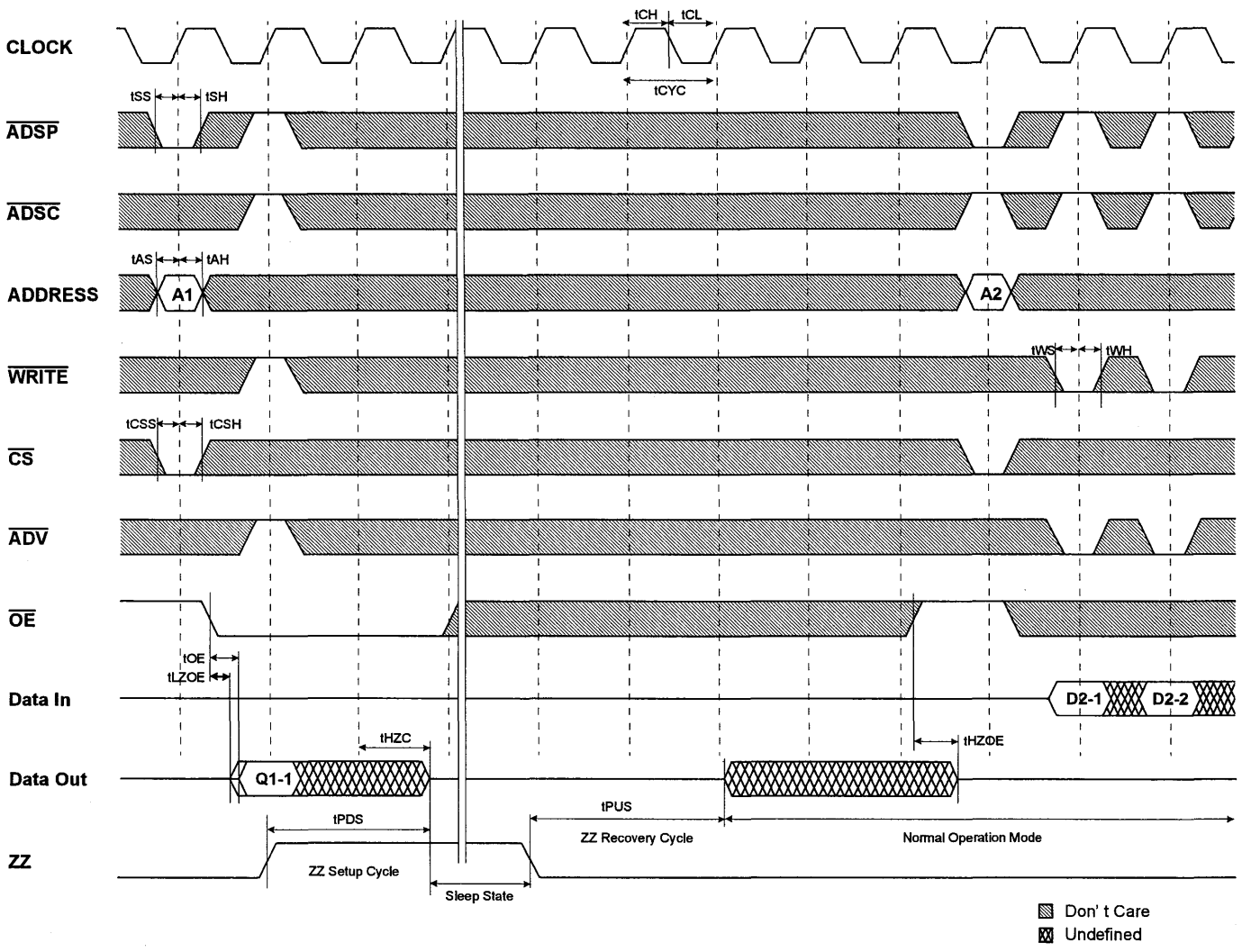
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ CONTROLLED, $\overline{ADSP}$=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



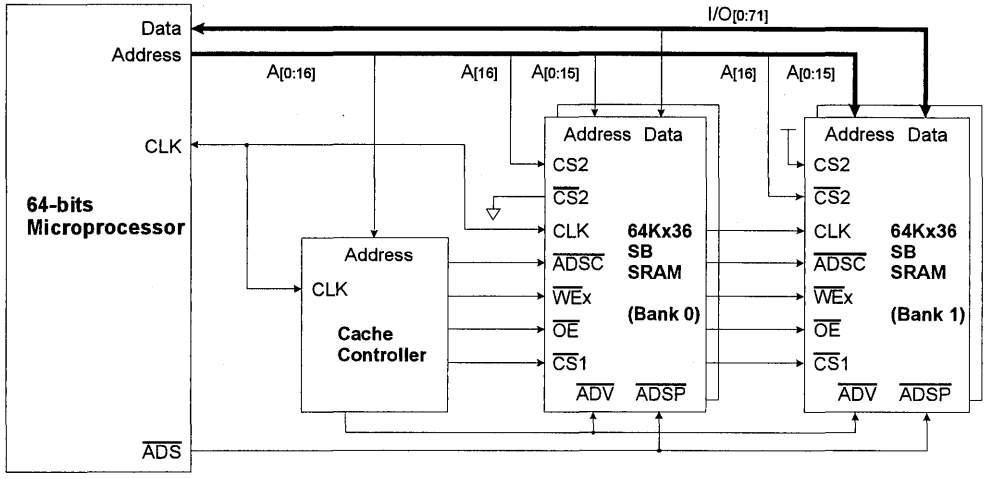
TIMING WAVEFORM OF POWER DOWN CYCLE



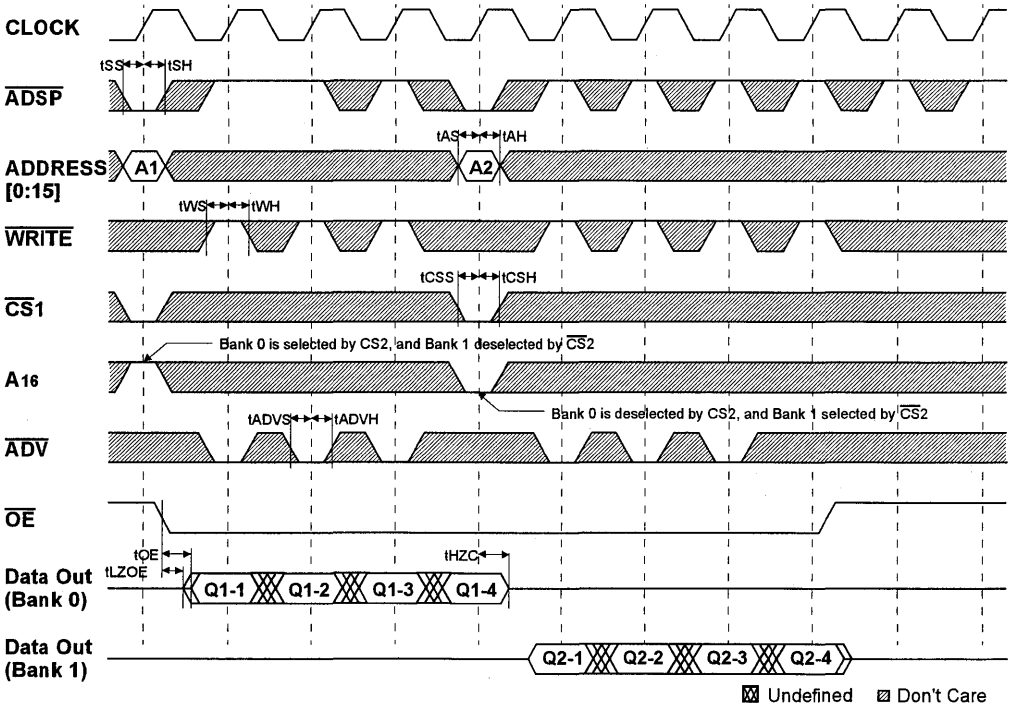
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 64Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING (Refer non-interleave write timing for interleave write timing)



4M High Performance Synchronous SRAM

128Kx36 & 256Kx18 Synchronous Pipelined SRAM

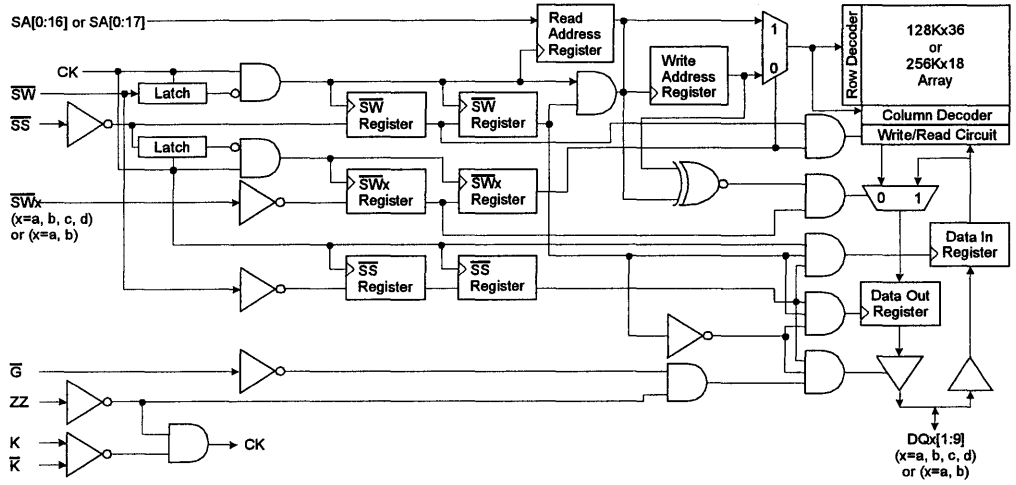
FEATURES

- 128Kx36 or 256Kx18 Organizations.
- 3.3V Core/1.5V Output Power Supply.
- HSTL Input and Output Levels.
- Differential, HSTL Clock Inputs K, $\overline{K}$.
- Synchronous Read and Write Operation
- Registered Input and Registered Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9 bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- Programmable Impedance Output Drivers.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17) Pin Ball Grid Array Package(14mm x 22mm).

Organization	Part Number	Cycle Time	Access Time
128Kx36	KM736FV4011H-5	5	2.5
	KM736FV4011H-6	6	3.0
	KM736FV4011H-7	7	3.5
256Kx18	KM718FV4011H-5	5	2.5
	KM718FV4011H-6	6	3.0
	KM718FV4011H-7	7	3.5

2

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, $\overline{K}$	Differential Clocks	C, $\overline{C}$	Differential Output Clocks
SAn	Synchronous Address Input	M_1, M_2	Read Protocol Mode Pins
DQn	Bi-directional Data Bus	$\overline{G}$	Asynchronous Output Enable
$\overline{SW}$	Synchronous Grobal Write Enable	$\overline{SS}$	Synchronous Select
$\overline{SW}a$	Synchronous Byte a Write Enable	TCK	JTAG Test Clock
$\overline{SW}b$	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
$\overline{SW}c$	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
$\overline{SW}d$	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
$\overline{ZZ}$	Asynchronous Power Down	ZQ	Output Driver Impedance Control Input HSTL Level
V_{DD}	Core Power Supply	Vss	GND
V_{DDQ}	Output Power Supply	NC	No Connection
V_{REF}	HSTL Input Reference Voltage		

NOTE : 1. This SRAM only supports single clock, register-register read protocol and have fixed impedance output driver. Therefore the following inputs must be set with power up and must not change during SRAM operation ; C=V_{DD}, $\overline{C}$=Vss, M_1=Vss, M_2=V_{DD}. But they are also designed to operate being left floating.

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

KM736FV4011(128Kx36)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA_{13}	SA_{10}	NC	SA_7	SA_4	V_{DDQ}
B	NC	NC	SA_9	NC	SA_8	NC	NC
C	NC	SA_{12}	SA_{11}	V_{DD}	SA_6	SA_5	NC
D	DQc8	DQc9	Vss	ZQ	Vss	DQb9	DQb8
E	DQc6	DQc7	Vss	$\overline{SS}$	Vss	DQb7	DQb6
F	V_{DDQ}	DQc5	Vss	$\overline{G}$	Vss	DQb5	V_{DDQ}
G	DQc3	DQc4	$\overline{SW}c$	$\overline{C}$	$\overline{SW}b$	DQb4	DQb3
H	DQc1	DQc2	Vss	C	Vss	DQb2	DQb1
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQd1	DQd2	Vss	K	Vss	DQa2	DQa1
L	DQd3	DQd4	$\overline{SW}d$	$\overline{K}$	$\overline{SW}a$	DQa4	DQa3
M	V_{DDQ}	DQd5	Vss	$\overline{SW}$	Vss	DQa5	V_{DDQ}
N	DQd6	DQd7	Vss	SA_{16}	Vss	DQa7	DQa6
P	DQd8	DQd9	Vss	SA_0	Vss	DQa9	DQa8
R	NC	SA_{15}	M_1	V_{DD}	M_2	SA_2	NC
T	NC	NC	SA_{14}	SA_1	SA_3	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

KM718FV4011(256Kx18)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA_{13}	SA_{10}	NC	SA_7	SA_4	V_{DDQ}
B	NC	NC	SA_9	NC	SA_8	NC	NC
C	NC	SA_{12}	SA_{11}	V_{DD}	SA_6	SA_5	NC
D	DQb1	NC	Vss	ZQ	Vss	DQa9	NC
E	NC	DQb2	Vss	$\overline{SS}$	Vss	NC	DQa8
F	V_{DDQ}	NC	Vss	$\overline{G}$	Vss	DQa7	V_{DDQ}
G	NC	DQb3	$\overline{SW}b$	$\overline{C}$	Vss	NC	DQa6
H	DQb4	NC	Vss	C	Vss	DQa5	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQb5	Vss	K	Vss	NC	DQa4
L	DQb6	NC	Vss	$\overline{K}$	$\overline{SW}a$	DQa3	NC
M	V_{DDQ}	DQb7	Vss	$\overline{SW}$	Vss	NC	V_{DDQ}
N	DQb8	NC	Vss	SA_{16}	Vss	DQa2	NC
P	NC	DQb9	Vss	SA_1	Vss	NC	DQa1
R	NC	SA_{15}	M_1	V_{DD}	M_2	SA_2	NC
T	NC	SA_{17}	SA_{14}	NC	SA_3	SA_0	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

FUNCTION DESCRIPTION

The KM736FV4011 and KM718FV4011 are 4,718,592 bit Synchronous Pipeline Mode SRAM. It is organized as 131,072 words of 36 bits(or 262, 144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology.
Single differential HSTL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, All addresses , Write Enables, Synchronous Select and Data Ins are registered internally. Data outs are updated from output registers edge of the next rising edge of the K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During reads, the address is registered during the frist clock edge, the internal array is read between this first edge and the second edge, and data is captured in the output register and driven to the CPU during the second clock edge. $\overline{SS}$ is driven low during this cycle, signaling that the SRAM should drive out the data.
During consecutive read cycles where the address is the same, the data output must be held constant without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and $\overline{SW}$ are sampled on the clock rising edge. $\overline{SW}$ is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and $\overline{SW}$ have been sampled by the SRAM. $\overline{SS}$ will be driven low during the same cycle that the Address, $\overline{SW}$ and $\overline{SW}$[a:d] are valid to signal that a valid operation is on the Address and Control Input.
Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals $\overline{SW}$[a:d] signal which 9-bit bytes will be writen. Timing of $\overline{SW}$[a:d] is the same as the $\overline{SW}$ signal.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

Low Power Dissipation Mode

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time(tZZR) is required before the SRAM resumes to normal operation.

TRUTH TABLE

K	ZZ	$\overline{G}$	$\overline{SS}$	$\overline{SW}$	$\overline{SW}$a	$\overline{SW}$b	$\overline{SW}$c	$\overline{SW}$d	DQa	DQb	DQc	DQd	Operation
X	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
X	L	H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled.
↑	L	L	H	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	L	H	X	X	X	X	DOUT	DOUT	DOUT	DOUT	Read Cycle
↑	L	L	L	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
↑	L	L	L	L	L	H	H	H	DIN	Hi-Z	Hi-Z	Hi-Z	Write first byte
↑	L	L	L	L	H	L	H	H	Hi-Z	DIN	Hi-Z	Hi-Z	Write second byte
↑	L	L	L	L	H	H	L	H	Hi-Z	Hi-Z	DIN	Hi-Z	Write third byte
↑	L	L	L	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte
↑	L	L	L	L	L	L	L	L	DIN	DIN	DIN	DIN	Write all byte

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	V_{DD}	-0.5 to 4.6	V
Output Supply Voltage Relative to Vss	V_{DDQ}	-0.5 to 4.6	V
Voltage on any I/O pin Relative to Vss	V_{TERM}	-0.5 to V_{DDQ}+0.5	V
Maximum Power Dissipation	P_D	2.5	W
Output Short-Circuit Current	I_{OUT}	25	mA
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature	T_{STG}	-65 to 125	℃

NOTE : Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	V_{DD}	3.15	3.3	3.45	V	
Output Power Supply Voltage	V_{DDQ}	1.4	1.5	1.6	V	
Input High Level	V_{IH}	V_{REF}+0.1	-	V_{DDQ} + 0.3	V	1, 2
Input Low Level	V_{IL}	-0.3	-	V_{REF} - 0.1	V	1, 3
Input Reference Voltage	V_{REF}	V_{DDQ}/2	-	2V_{DDQ}/3	V	1
Clock Input Signal Voltage	V_{IN}-CLK	-0.3	-	V_{DDQ} + 0.3	V	1
Clock Input Differential Voltage	V_{DIF}-CLK	0.1	-	V_{DDQ} + 0.6	V	1
Clock Input Common Mode Voltage	V_{CM}-CLK	V_{DDQ}/2	-	2V_{DDQ}/3	V	1
Operating Junction Temperature	T_J	10	-	110	℃	4

NOTE :1. These are DC V_{IH}/V_{IH} spec. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
2. V_{IH} (Max)DC = V_{DD}+0.3V, V_{IH} (Max)AC = V_{DD}+1.5V(pulse width≤5ns).
3. V_{IL} (Min)DC = -0.3V, V_{IL} (Min)AC =-1.5V(pulse width≤5ns).
4. Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. T_J = T_A + P_D x THETA_JA

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (V_{IN}=V_{IH} or V_{IL}, ZZ & $\overline{SS}$=V_{IL})	I_{DD}	-	700	mA	1
Average Power Supply Operating Current-x18 (V_{IN}=V_{IH} or V_{IL}, ZZ & $\overline{SS}$=V_{IL})	I_{DD}	-	650	mA	1
Power Supply Standby Current (V_{IN}=V_{IH} or V_{IL}, ZZ =V_{IH})	I_{SB}	-	100	mA	1
Input Leakage Current (V_{IN}=Vss or V_{DD})	I_{LI}	-1	1	μA	
Output Leakage Current (V_{OUT}=Vss or V_{DD}, ZZ =V_{IH})	I_{LO}	-5	5	μA	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	V_{DDQ}/2+0.3	V_{DDQ}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	Vss	V_{DDQ}/2+0.3	V	

NOTE :1. Minimum cycle. I_{OUT}=0mA.

PIN CAPACITANCE

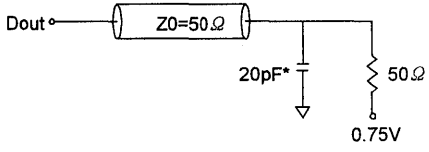
Parameter	Symbol	Pin Name	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	K, $\overline{K}$, $\overline{SS}$, $\overline{SW}$, $\overline{G}$, ZZ $\overline{SW}$x, ZQ, M_1, M_2, SAn, TCK, TMS, TDI	3	4	5	pF
Output Capacitance	C_{OUT}	DQn, TDO	5	6	7	pF

NOTE : Periodically sampled and 100% tested.(dV=0V, f=1MHz)

AC TEST CONDITIONS

Parameter	Symbol	Value	Unit
Input High/Low Level	V_{IH}/V_{IL}	1.5/0.0	V
Input Reference Level	V_{REF}	0.75	V
Input Rise/Fall Time	T_R/T_F	1.0/1.0	ns
Output Rise/Fall Time	T_R/T_F	0.5~1.0	ns
Input and Out Timing Reference Level		0.75	V
Clock Input Timing Reference Level		Cross Point	V

AC TEST OUTPUT LOAD

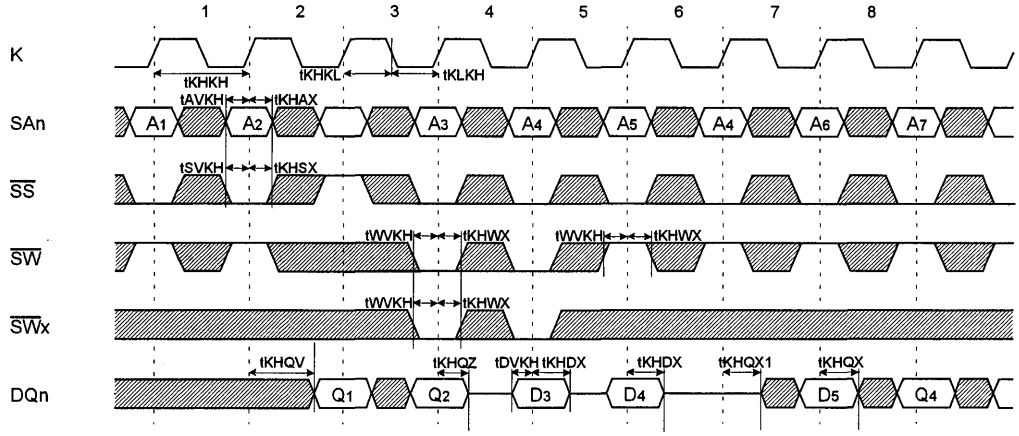


*Capacitive load consists of all components of the tester environment

AC CHARACTERISTICS

Parameter	Symbol	-5		-6		-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	tKHKH	5.0	-	6.0	-	7.0	-	ns	
Clock High Pulse Width	tKHKL	2.0	-	2.4	-	2.8	-	ns	
Clock Low Pulse Width	tKLKH	2.0	-	2.4	-	2.8	-	ns	
Clock High to Output Valid	tKHQV	-	2.5	-	3.0	-	3.5	ns	
Clock High to Output Hold	tKHQX	1.0	-	1.0	-	1.0	-	ns	
Address Setup Time	tAVKH	0.5	-	0.5	-	0.5	-	ns	
Address Hold Time	tKHAX	1.0	-	1.0	-	1.0	-	ns	
Write Data Setup Time	tDVKH	0.5	-	0.5	-	0.5	-	ns	
Write Data Hold Time	tKHDX	1.0	-	1.0	-	1.0	-	ns	
$\overline{SW}$, $\overline{SW}$[a:d] Setup Time	tWVKH	0.5	-	0.5	-	0.5	-	ns	
$\overline{SW}$, $\overline{SW}$[a:d] Hold Time	tKHWX	1.0	-	1.0	-	1.0	-	ns	
$\overline{SS}$ Setup Time	tSVKH	0.5	-	0.5	-	0.5	-	ns	
$\overline{SS}$ Hold Time	tKHSX	1.0	-	1.0	-	1.0	-	ns	
Clock High to Output Hi-Z	tKHQZ	-	2.5	-	3.0	-	3.5	ns	
Clock High to Output Low-Z	tKHQX1	1.0	-	1.0	-	1.0	-	ns	
$\overline{G}$ High to Output High-Z	tGHQZ	-	2.5	-	3.0	-	3.5	ns	
$\overline{G}$ Low to Output Low-Z	tGLQX	0.5	-	0.5	-	0.5	-	ns	
$\overline{G}$ Low to Output Valid	tGLQV	-	2.5	-	3.0	-	3.5	ns	
ZZ High to Power Down(Sleep Time)	tZZE	-	5.0	-	6.0	-	7.0	ns	
ZZ Low to Recovery(Wake-up Time)	tZZR	-	5.0	-	6.0	-	7.0	ns	

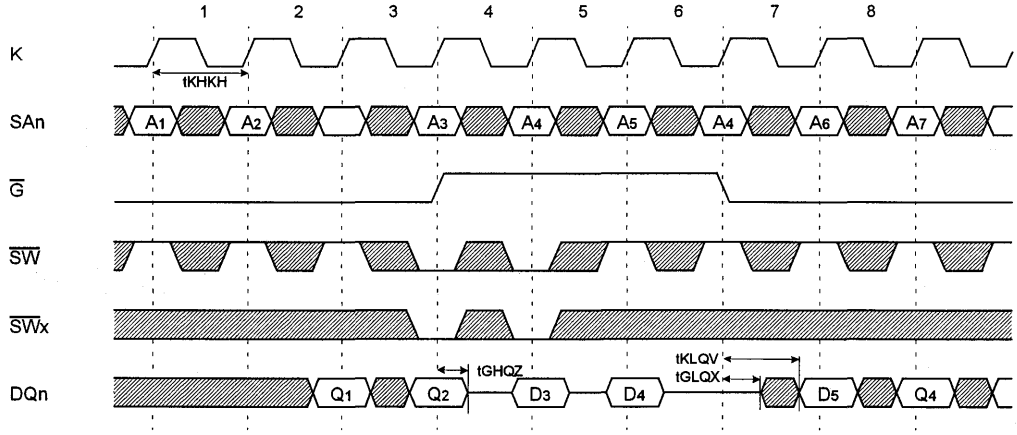
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES($\overline{SS}$ Controlled, $\overline{G}$=Low)



NOTE :

1. D_3 is the input data written in memory location A_3.
2. Q_4 is the output data read from the write data buffer(not from the cell array), as a result of address A_4 being a match from the last write cycle address.

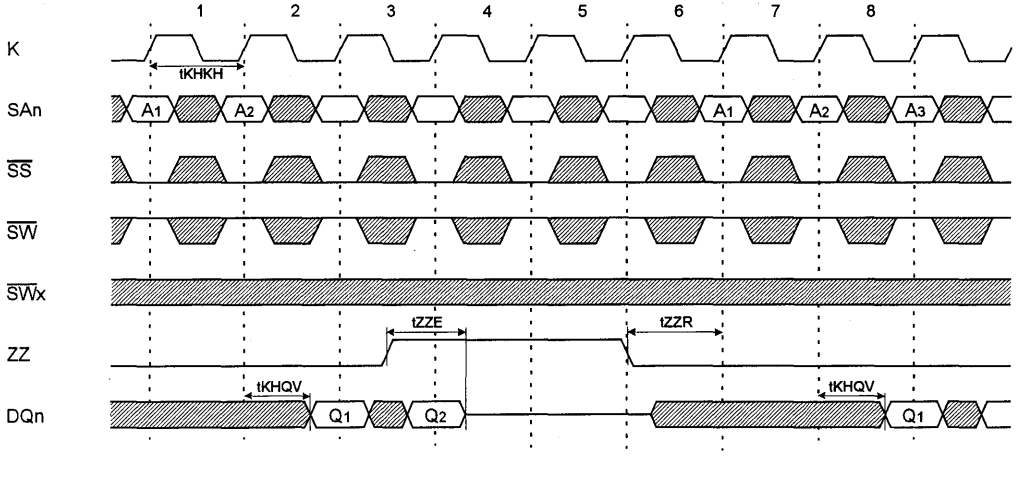
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES($\overline{G}$ Controlled, $\overline{SS}$=Low)



NOTE :

1. D_3 is the input data written in memory location A_3.
2. Q_4 is the output data read from the write data buffer(not from the cell array), as a result of address A_4 being a match from the last write cycle address.

TIMING WAVEFORMS OF STANDBY CYCLES



PROGRAMMABLE IMPEDANCE OUTPUT BUFFER OPERATION

The designer can program the SRAM's output buffer impedance by terminating the ZQ pin to Vss through a precision resistor(RQ). The value of RQ is five times the output impedance desired. For example, 250Ω resistor will give an output impedance of 50Ω. The allowable range of RQ to guarantee impedance matching with a tolerance of 7.5% is between 175Ω and 350Ω. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. They may also occur in cycles initiated with $\overline{G}$ high. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM. Periodic readjustment is necessary as the impedance is greatly affected by drifts in supply voltage and temperature.
Impedance updates occur no more often than every 32 clock cycles. Clock cycles are counted whether the SRAM is selected or not and proceed regardless of the type of cycle being executed. Therefore, the user can be assured that after 33 continuous read cycles have occurred, an impedance update will occur the next time $\overline{SS}$ or $\overline{G}$ are high at a rising edge of the K clock. There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

DC Electrical Characteristics

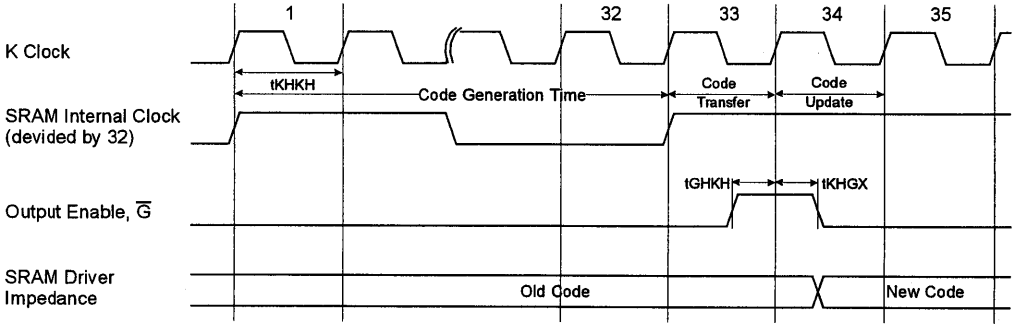
Parameter	Symbol	Min	Typ	Max	Unit	Note
Impedance Control Resistor Range	RQ	175	250	350	Ω	-
Driver Impedance	ZD	RQ/5-7.5%	-	RQ/5+7.5%	Ω	1

NOTE : 1. Measured at $V_{OUT}=V_{DDQ}/2$. $I_{OUT}=(V_{DDQ}/2)/(RQ/5)\pm 7.5\%$ @$V_{OUT}=V_{DDQ}/2$.

AC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output Impedance Update $\overline{G}$ Setup Time	tGHKH	0.5	-	-	ns	-
Output Impedance Update $\overline{G}$ Hold Time	tKHGX	1.0	-	-	ns	-

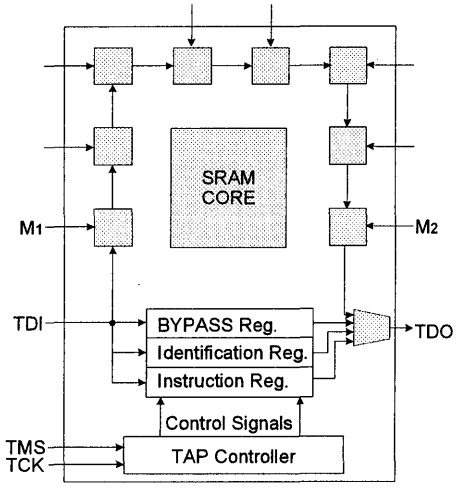
TIMING WAVEFORMS OF Driver Impedance Update Control



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



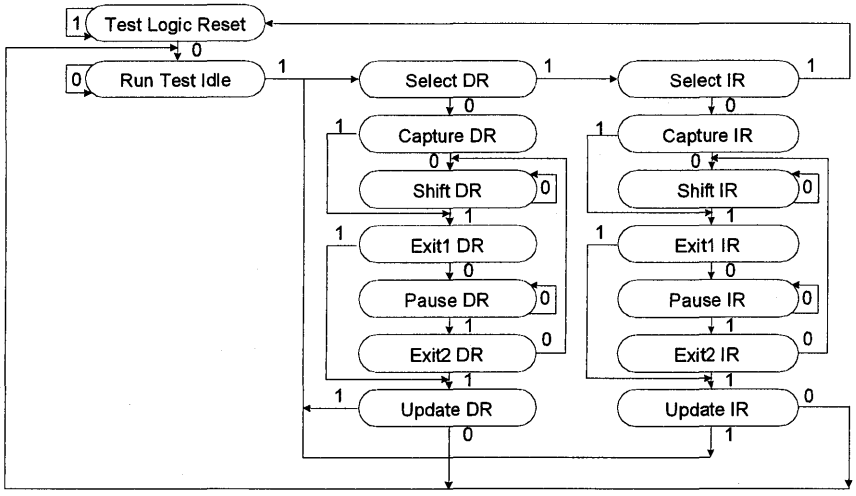
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	000000	00001001110	1
256Kx18	0000	00110 00011	000000	00001001110	1

BOUNDARY SCAN EXIT ORDER(x36)

36	3B	SA_9		SA_8	5B	35
37	2B	NC		NC	6B	34
38	3A	SA_{10}		SA_7	5A	33
39	3C	SA_{11}		SA_6	5C	32
40	2C	SA_{12}		SA_5	6C	31
41	2A	SA_{13}		SA_4	6A	30
42	2D	DQc9		DQb9	6D	29
43	1D	DQc8		DQb8	7D	28
44	2E	DQc7		DQb7	6E	27
45	1E	DQc6		DQb6	7E	26
46	2F	DQc5		DQb5	6F	25
47	2G	DQc4		DQb4	6G	24
48	1G	DQc3		DQb3	7G	23
49	2H	DQc2		DQb2	6H	22
50	1H	DQc1		DQb1	7H	21
51	3G	$\overline{SW}c$		$\overline{SW}b$	5G	20
52	4D	ZQ		$\overline{G}$	4F	19
53	4E	$\overline{SS}$		K	4K	18
54	4G	$\overline{C}$		$\overline{K}$	4L	17
55	4H	C		$\overline{SW}a$	5L	16
56	4M	$\overline{SW}$		DQa1	7K	15
57	3L	$\overline{SW}d$		DQa2	6K	14
58	1K	DQd1		DQa3	7L	13
59	2K	DQd2		DQa4	6L	12
60	1L	DQd3		DQa5	6M	11
61	2L	DQd4		DQa6	7N	10
62	2M	DQd5		DQa7	6N	9
63	1N	DQd6		DQa8	7P	8
64	2N	DQd7		DQa9	6P	7
65	1P	DQd8		ZZ	7T	6
66	2P	DQd9		SA_3	5T	5
67	3T	SA_{14}		SA_2	6R	4
68	2R	SA_{15}		SA_1	4T	3
69	4N	SA_{16}		SA_0	4P	2
70	3R	M_1		M_2	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

26	3B	SA_9		SA_8	5B	25
27	2B	NC		NC	6B	24
28	3A	SA_{10}		SA_7	5A	23
29	3C	SA_{11}		SA_6	5C	22
30	2C	SA_{12}		SA_5	6C	21
31	2A	SA_{13}		SA_4	6A	20
				DQa9	6D	19
32	1D	DQb1				
33	2E	DQb2				
				DQa8	7E	18
				DQa7	6F	17
34	2G	DQb3				
				DQa6	7G	16
				DQa5	6H	15
35	1H	DQb4				
36	3G	$\overline{SW}b$				
37	4D	ZQ		$\overline{G}$	4F	14
38	4E	$\overline{SS}$		K	4K	13
39	4G	$\overline{C}$		$\overline{K}$	4L	12
40	4H	C		$\overline{SW}a$	5L	11
41	4M	$\overline{SW}$		DQa4	7K	10
42	2K	DQb5		DQa3	6L	9
43	1L	DQb6				
44	2M	DQb7		DQa2	6N	8
45	1N	DQb8		DQa1	7P	7
				ZZ	7T	6
46	2P	DQb9		SA_3	5T	5
47	3T	SA_{14}		SA_2	6R	4
48	2R	SA_{15}				
49	4N	SA_{16}		SA_1	4P	3
50	2T	SA_{17}		SA_0	6T	2
51	3R	M_1		M_2	5R	1

NOTE : 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	3.15	3.3	3.45	V	
Input High Level	V_{IH}	2.0	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.8	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	2.4	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	Vss	-	0.4	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

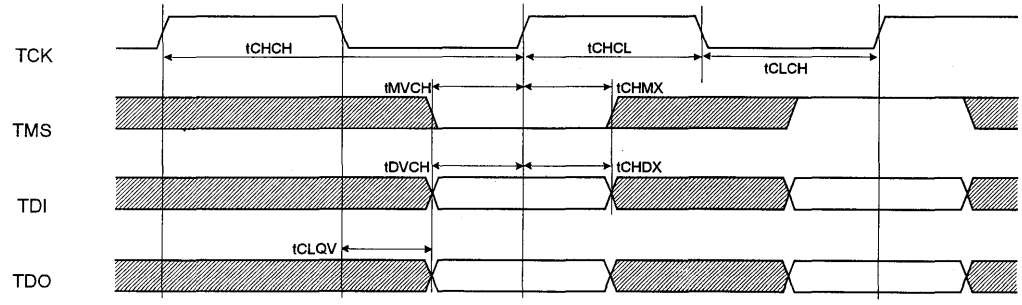
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	3.0/0.0	V	
Input Rise/Fall Time	TR/TF	2.0/2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

NOTE : 1. See SRAM AC test output load on page 5.

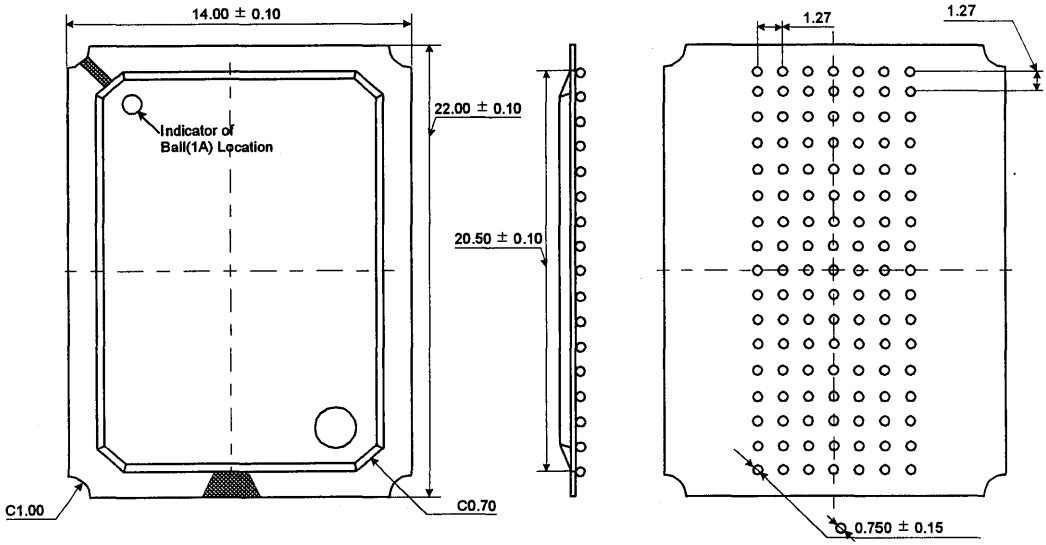
JTAG AC Characteristics

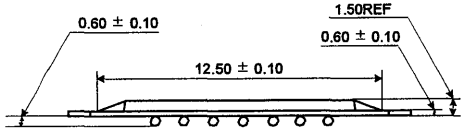
Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	tCHCH	50	-	ns	
TCK High Pulse Width	tCHCL	20	-	ns	
TCK Low Pulse Width	tCLCH	20	-	ns	
TMS Input Setup Time	tMVCH	5	-	ns	
TMS Input Hold Time	tCHMX	5	-	ns	
TDI Input Setup Time	tDVCH	5	-	ns	
TDI Input Hold Time	tCHDX	5	-	ns	
Clock Low to Output Valid	tCLQV	0	10	ns	

JTAG TIMING DIAGRAM



119 BGA PACKAGE DIMENSIONS





NOTE :

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.

119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Junction to Ambient(at still air)	Theta_JA	-	-	50	°C/W	
Junction to Ambient(at air flow of 100 LFPM)	Theta_JA	-	-	40	°C/W	
Junction to Case	Theta_JC	-	-	8	°C/W	
Junction to Solder Ball	Theta_JB	-	-	10	°C/W	

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D \times Theta\_JA$.

128Kx36 & 256Kx18 Synchronous Pipelined SRAM

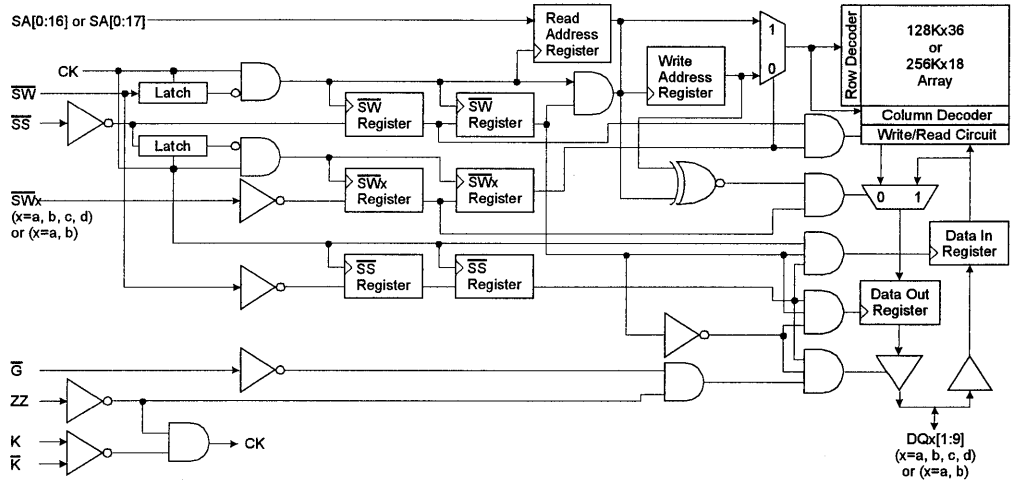
FEATURES

- 128Kx36 or 256Kx18 Organizations.
- 3.3V Core/ Output Power Supply.
- LVTTL 3.3V Input and Output Levels.
- Differential, PECL Clock Inputs K, $\overline{K}$.
- Synchronous Read and Write Operation
- Registered Input and Registered Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9 bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17) Pin Ball Grid Array Package(14mm x 22mm).

Organization	Part Number	Cycle Time	Access Time
128Kx36	KM736FV4021H-5	5	2.5
	KM736FV4021H-6	6	3.0
	KM736FV4021H-7	7	3.5
256Kx18	KM718FV4021H-5	5	2.5
	KM718FV4021H-6	6	3.0
	KM718FV4021H-7	7	3.5

2

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, $\overline{K}$	Differential Clocks	C, $\overline{C}$	Differential Output Clocks
SAn	Synchronous Address Input	M_1, M_2	Read Protocol Mode Pins
DQn	Bi-directional Data Bus	$\overline{G}$	Asynchronous Output Enable
$\overline{SW}$	Synchronous Grobal Write Enable	$\overline{SS}$	Synchronous Select
$\overline{SW}$a	Synchronous Byte a Write Enable	TCK	JTAG Test Clock
$\overline{SW}$b	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
$\overline{SW}$c	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
$\overline{SW}$d	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	ZQ	Output Driver Impedance Control Input HSTL Level
V_{DD}	Core Power Supply	Vss	GND
V_{DDQ}	Output Power Supply	NC	No Connection
V_{REF}	HSTL Input Reference Voltage		

NOTE : 1. This SRAM only supports single clock, register-register read protocol and have fixed impedance output driver. Therefore the following inputs must be set with power up and must not change during SRAM operation ; C=V_{DD}, $\overline{C}$=Vss, M_1=Vss, M_2=V_{DD}, ZQ=V_{DD} and V_{REF}=V_{DD}. But they are also designed to operate being left floating.

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

KM736FV4021(128Kx36)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA_{13}	SA_{10}	NC	SA_7	SA_4	V_{DDQ}
B	NC	NC	SA_9	NC	SA_8	NC	NC
C	NC	SA_{12}	SA_{11}	V_{DD}	SA_6	SA_5	NC
D	DQc8	DQc9	Vss	ZQ	Vss	DQb9	DQb8
E	DQc6	DQc7	Vss	$\overline{SS}$	Vss	DQb7	DQb6
F	V_{DDQ}	DQc5	Vss	$\overline{G}$	Vss	DQb5	V_{DDQ}
G	DQc3	DQc4	$\overline{SW}c$	$\overline{C}$	$\overline{SW}b$	DQb4	DQb3
H	DQc1	DQc2	Vss	C	Vss	DQb2	DQb1
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQd1	DQd2	Vss	K	Vss	DQa2	DQa1
L	DQd3	DQd4	$\overline{SW}d$	$\overline{K}$	$\overline{SW}a$	DQa4	DQa3
M	V_{DDQ}	DQd5	Vss	$\overline{SW}$	Vss	DQa5	V_{DDQ}
N	DQd6	DQd7	Vss	SA_{16}	Vss	DQa7	DQa6
P	DQd8	DQd9	Vss	SA_0	Vss	DQa9	DQa8
R	NC	SA_{15}	M_1	V_{DD}	M_2	SA_2	NC
T	NC	NC	SA_{14}	SA_1	SA_3	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

KM718FV4021(256Kx18)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA_{13}	SA_{10}	NC	SA_7	SA_4	V_{DDQ}
B	NC	NC	SA_9	NC	SA_8	NC	NC
C	NC	SA_{12}	SA_{11}	V_{DD}	SA_6	SA_5	NC
D	DQb1	NC	Vss	ZQ	Vss	DQa9	NC
E	NC	DQb2	Vss	$\overline{SS}$	Vss	NC	DQa8
F	V_{DDQ}	NC	Vss	$\overline{G}$	Vss	DQa7	V_{DDQ}
G	NC	DQb3	$\overline{SW}b$	$\overline{C}$	Vss	NC	DQa6
H	DQb4	NC	Vss	C	Vss	DQa5	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQb5	Vss	K	Vss	NC	DQa4
L	DQb6	NC	Vss	$\overline{K}$	$\overline{SW}a$	DQa3	NC
M	V_{DDQ}	DQb7	Vss	$\overline{SW}$	Vss	NC	V_{DDQ}
N	DQb8	NC	Vss	SA_{16}	Vss	DQa2	NC
P	NC	DQb9	Vss	SA_1	Vss	NC	DQa1
R	NC	SA_{15}	M_1	V_{DD}	M_2	SA_2	NC
T	NC	SA_{17}	SA_{14}	NC	SA_3	SA_0	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

FUNCTION DESCRIPTION

The KM736FV4021 and KM718FV4011 are 4,718,592 bit Synchronous Pipeline Mode SRAM. It is organized as 131,072 words of 36 bits(or 262, 144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology.
Single differential PECL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, All addresses , Write Enables, Synchronous Select and Data Ins are registered internally. Data outs are updated from output registers edge of the next rising edge of the K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During reads, the address is registered during the frist clock edge, the internal array is read between this first edge and the second edge, and data is captured in the output register and driven to the CPU during the second clock edge. $\overline{SS}$ is driven low during this cycle, signaling that the SRAM should drive out the data.
During consecutive read cycles where the address is the same, the data output must be held constant without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and $\overline{SW}$ are sampled on the clock rising edge. $\overline{SW}$ is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and $\overline{SW}$ have been sampled by the SRAM. $\overline{SS}$ will be driven low during the same cycle that the Address, $\overline{SW}$ and $\overline{SW}$[a:d] are valid to signal that a valid operation is on the Address and Control Input.
Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals $\overline{SW}$[a:d] signal which 9-bit bytes will be writen. Timing of $\overline{SW}$[a:d] is the same as the $\overline{SW}$ signal.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

Low Power Dissipation Mode

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time(tZZR) is required before the SRAM resumes to normal operation.

TRUTH TABLE

K	ZZ	$\overline{G}$	$\overline{SS}$	$\overline{SW}$	$\overline{SW}$a	$\overline{SW}$b	$\overline{SW}$c	$\overline{SW}$d	DQa	DQb	DQc	DQd	Operation
X	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
X	L	H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled.
↑	L	L	H	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	L	H	X	X	X	X	DOUT	DOUT	DOUT	DOUT	Read Cycle
↑	L	L	L	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
↑	L	L	L	L	L	H	H	H	DIN	Hi-Z	Hi-Z	Hi-Z	Write first byte
↑	L	L	L	L	H	L	H	H	Hi-Z	DIN	Hi-Z	Hi-Z	Write second byte
↑	L	L	L	L	H	H	L	H	Hi-Z	Hi-Z	DIN	Hi-Z	Write third byte
↑	L	L	L	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte
↑	L	L	L	L	L	L	L	L	DIN	DIN	DIN	DIN	Write all byte

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	V_{DD}	-0.5 to 4.6	V
Output Supply Voltage Relative to Vss	V_{DDQ}	-0.5 to 4.6	V
Voltage on any I/O pin Relative to Vss	V_{TERM}	-0.5 to V_{DDQ}+0.5	V
Maximum Power Dissipation	P_D	2.5	W
Output Short-Circuit Current	I_{OUT}	25	mA
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature	T_{STG}	-65 to 125	℃

NOTE : Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	V_{DD}	3.15	3.3	3.45	V	
Output Power Supply Voltage	V_{DDQ}	3.15	3.3	3.45	V	
Input High Level	V_{IH}	2.0	-	V_{DD} + 0.3	V	1, 2
Input Low Level	V_{IL}	-0.3	-	0.8	V	1, 3
PECL Clock Input High Level	V_{IH}-PECL	2.135	-	2.420	V	1
PECL Clock Input Low Level	V_{IL}-PECL	1.490	-	1.825	V	1
Operating Junction Temperature	T_J	10	-	110	℃	4

NOTE :1. These are DC V_{IH}/V_{IH} spec. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
2. V_{IH} (Max)DC = V_{DD}+0.3V, V_{IH} (Max)AC = V_{DD}+1.5V(pulse width$\leq$5ns).
3. V_{IL} (Min)DC = -0.3V, V_{IL} (Min)AC =-1.5V(pulse width$\leq$5ns).
4. Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. $T_J = T_A + P_D \times THETA\_JA$

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (V_{IN}=V_{IH} or V_{IL}, ZZ & $\overline{SS}$=V_{IL})	I_{DD}	-	700	mA	1
Average Power Supply Operating Current-x18 (V_{IN}=V_{IH} or V_{IL}, ZZ & $\overline{SS}$=V_{IL})	I_{DD}	-	650	mA	1
Power Supply Standby Current (V_{IN}=V_{IH} or V_{IL}, ZZ =V_{IH})	I_{SB}	-	100	mA	1
Input Leakage Current (V_{IN}=Vss or V_{DD})	I_{LI}	-1	1	μA	
Output Leakage Current (V_{OUT}=Vss or V_{DD}, ZZ =V_{IH})	I_{LO}	-5	5	μA	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	2.4	V_{DDQ}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	Vss	0.4	V	

NOTE :1. Minimum cycle. I_{OUT}=0mA.

PIN CAPACITANCE

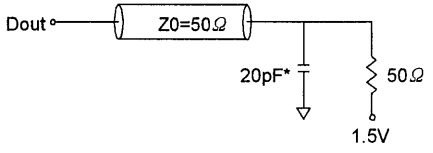
Parameter	Symbol	Pin Name	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	K, $\overline{K}$, $\overline{SS}$, $\overline{SW}$, $\overline{G}$, ZZ $\overline{SW}$x, ZQ, M_1, M_2, SAn, TCK, TMS, TDI	3	4	5	pF
Output Capacitance	C_{OUT}	DQn, TDO	5	6	7	pF

NOTE : Periodically sampled and 100% tested.(dV=0V, f=1MHz)

AC TEST CONDITIONS

Parameter	Symbol	Value	Unit
Input High/Low Level	V_{IH}/V_{IL}	3.0/0.0	V
Clock Input High/Low Level(PECL)	V_{IH}/V_{IL}	2.4/1.5	V
Input Rise/Fall Time	T_R/T_F	1.0/1.0	ns
Clock Input Rise/Fall Time(PECL)	T_R/T_F	0.5/0.5	ns
Output Rise/Fall Time	T_R/T_F	0.5~1.0	ns
Input and Out Timing Reference Level		1.5	V
Clock Input Timing Reference Level		Cross Point	V

AC TEST OUTPUT LOAD

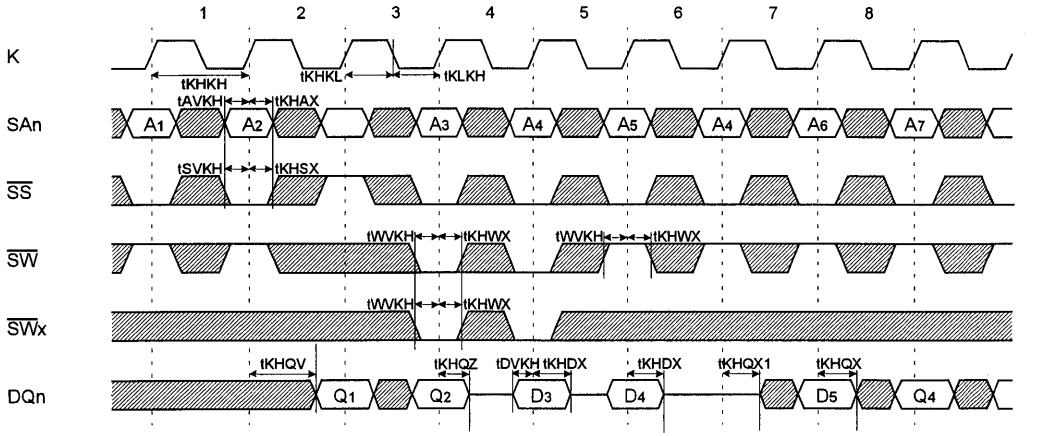


*Capacitive load consists of all components of the tester environment

AC CHARACTERISTICS

Parameter	Symbol	-5		-6		-7		Unit	Note
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	tKHKH	5.0	-	6.0	-	7.0	-	ns	
Clock High Pulse Width	tKHKL	2.0	-	2.4	-	2.8	-	ns	
Clock Low Pulse Width	tKLKH	2.0	-	2.4	-	2.8	-	ns	
Clock High to Output Valid	tKHQV	-	2.5	-	3.0	-	3.5	ns	
Clock High to Output Hold	tKHQX	1.0	-	1.0	-	1.0	-	ns	
Address Setup Time	tAVKH	0.5	-	0.5	-	0.5	-	ns	
Address Hold Time	tKHAX	1.0	-	1.0	-	1.0	-	ns	
Write Data Setup Time	tDVKH	0.5	-	0.5	-	0.5	-	ns	
Write Data Hold Time	tKHDX	1.0	-	1.0	-	1.0	-	ns	
$\overline{SW}$, $\overline{SW}$[a:d] Setup Time	tWVKH	0.5	-	0.5	-	0.5	-	ns	
$\overline{SW}$, $\overline{SW}$[a:d] Hold Time	tKHWX	1.0	-	1.0	-	1.0	-	ns	
$\overline{SS}$ Setup Time	tSVKH	0.5	-	0.5	-	0.5	-	ns	
$\overline{SS}$ Hold Time	tKHSX	1.0	-	1.0	-	1.0	-	ns	
Clock High to Output Hi-Z	tKHQZ	-	2.5	-	3.0	-	3.5	ns	
Clock High to Output Low-Z	tKHQX1	1.0	-	1.0	-	1.0	-	ns	
$\overline{G}$ High to Output High-Z	tGHQZ	-	2.5	-	3.0	-	3.5	ns	
$\overline{G}$ Low to Output Low-Z	tGLQX	0.5	-	0.5	-	0.5	-	ns	
$\overline{G}$ Low to Output Valid	tGLQV	-	2.5	-	3.0	-	3.5	ns	
ZZ High to Power Down(Sleep Time)	tZZE	-	5.0	-	6.0	-	7.0	ns	
ZZ Low to Recovery(Wake-up Time)	tZZR	-	5.0	-	6.0	-	7.0	ns	

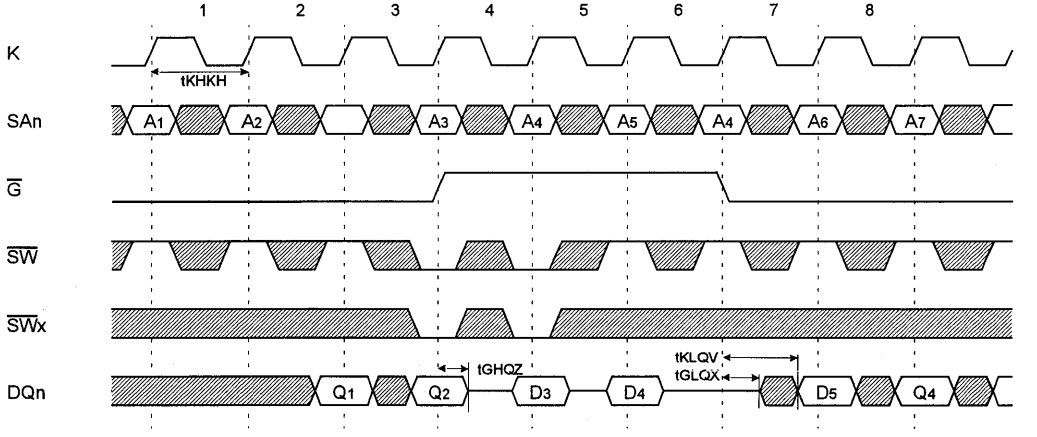
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES($\overline{SS}$ Controlled, $\overline{G}$=Low)



NOTE :

1. D_3 is the input data written in memory location A_3.
2. Q_4 is the output data read from the write data buffer(not from the cell array), as a result of address A_4 being a match from the last write cycle address.

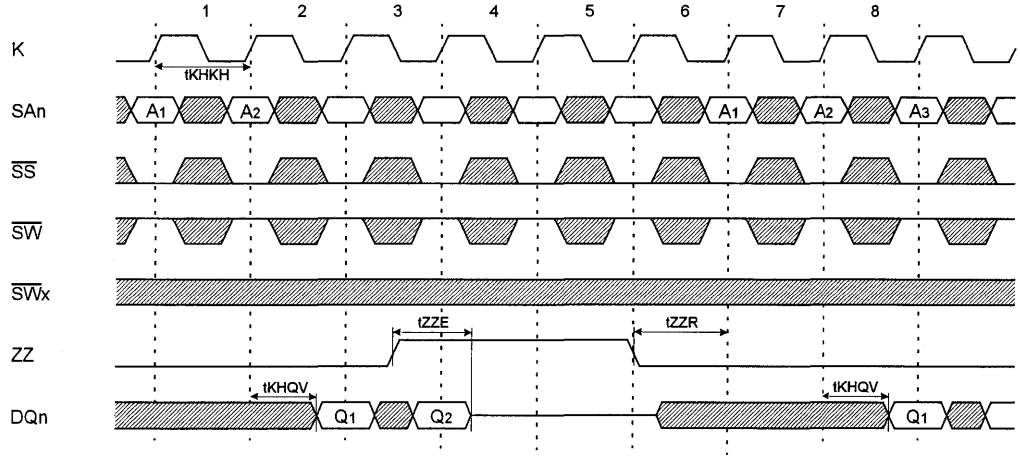
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES($\overline{G}$ Controlled, $\overline{SS}$=Low)



NOTE :

1. D_3 is the input data written in memory location A_3.
2. Q_4 is the output data read from the write data buffer(not from the cell array), as a result of address A_4 being a match from the last write cycle address.

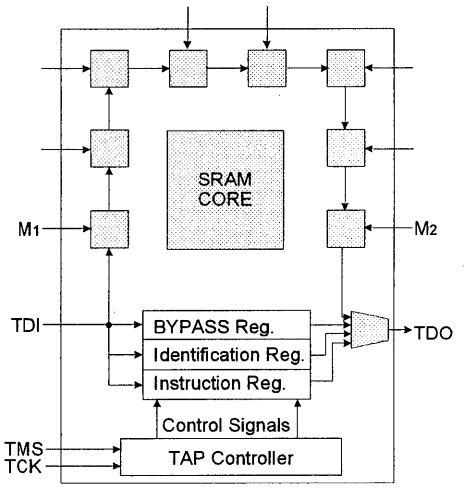
TIMING WAVEFORMS OF STANDBY CYCLES



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



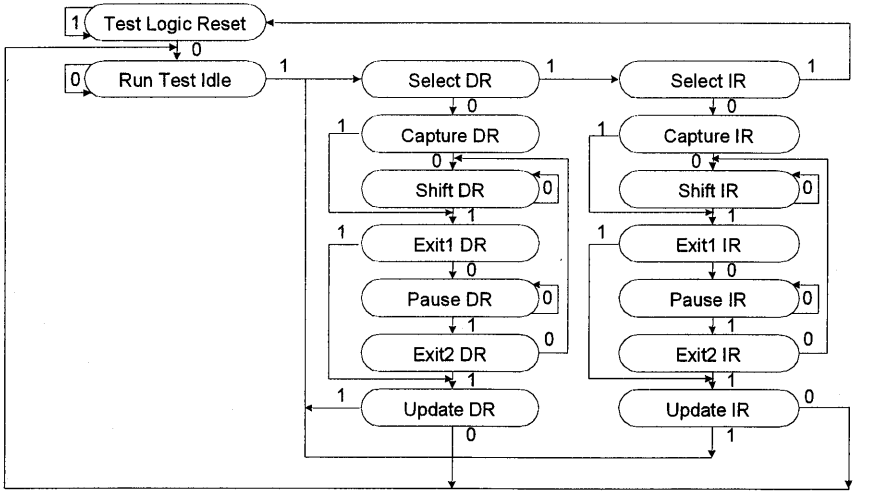
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	000000	00001001110	1
256Kx18	0000	00110 00011	000000	00001001110	1

BOUNDARY SCAN EXIT ORDER(x36)

36	3B	SA_9		SA_8	5B	35
37	2B	NC		NC	6B	34
38	3A	SA_{10}		SA_7	5A	33
39	3C	SA_{11}		SA_6	5C	32
40	2C	SA_{12}		SA_5	6C	31
41	2A	SA_{13}		SA_4	6A	30
42	2D	DQc9		DQb9	6D	29
43	1D	DQc8		DQb8	7D	28
44	2E	DQc7		DQb7	6E	27
45	1E	DQc6		DQb6	7E	26
46	2F	DQc5		DQb5	6F	25
47	2G	DQc4		DQb4	6G	24
48	1G	DQc3		DQb3	7G	23
49	2H	DQc2		DQb2	6H	22
50	1H	DQc1		DQb1	7H	21
51	3G	$\overline{SW}c$		$\overline{SW}b$	5G	20
52	4D	ZQ		$\overline{G}$	4F	19
53	4E	$\overline{SS}$		K	4K	18
54	4G	$\overline{C}$		$\overline{K}$	4L	17
55	4H	C		$\overline{SW}a$	5L	16
56	4M	$\overline{SW}$		DQa1	7K	15
57	3L	$\overline{SW}d$		DQa2	6K	14
58	1K	DQd1		DQa3	7L	13
59	2K	DQd2		DQa4	6L	12
60	1L	DQd3		DQa5	6M	11
61	2L	DQd4		DQa6	7N	10
62	2M	DQd5		DQa7	6N	9
63	1N	DQd6		DQa8	7P	8
64	2N	DQd7		DQa9	6P	7
65	1P	DQd8		ZZ	7T	6
66	2P	DQd9		SA_3	5T	5
67	3T	SA_{14}		SA_2	6R	4
68	2R	SA_{15}		SA_1	4T	3
69	4N	SA_{16}		SA_0	4P	2
70	3R	M_1		M_2	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

26	3B	SA_9		SA_8	5B	25
27	2B	NC		NC	6B	24
28	3A	SA_{10}		SA_7	5A	23
29	3C	SA_{11}		SA_6	5C	22
30	2C	SA_{12}		SA_5	6C	21
31	2A	SA_{13}		SA_4	6A	20
				DQa9	6D	19
32	1D	DQb1				
33	2E	DQb2				
				DQa8	7E	18
				DQa7	6F	17
34	2G	DQb3				
				DQa6	7G	16
				DQa5	6H	15
35	1H	DQb4				
36	3G	$\overline{SW}b$				
37	4D	ZQ		$\overline{G}$	4F	14
38	4E	$\overline{SS}$		K	4K	13
39	4G	$\overline{C}$		$\overline{K}$	4L	12
40	4H	C		$\overline{SW}a$	5L	11
41	4M	$\overline{SW}$		DQa4	7K	10
42	2K	DQb5		DQa3	6L	9
43	1L	DQb6				
44	2M	DQb7		DQa2	6N	8
45	1N	DQb8		DQa1	7P	7
				ZZ	7T	6
46	2P	DQb9		SA_3	5T	5
47	3T	SA_{14}		SA_2	6R	4
48	2R	SA_{15}				
49	4N	SA_{16}		SA_1	4P	3
50	2T	SA_{17}		SA_0	6T	2
51	3R	M_1		M_2	5R	1

NOTE : 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	3.15	3.3	3.45	V	
Input High Level	V_{IH}	2.0	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.8	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	2.4	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	Vss	-	0.4	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

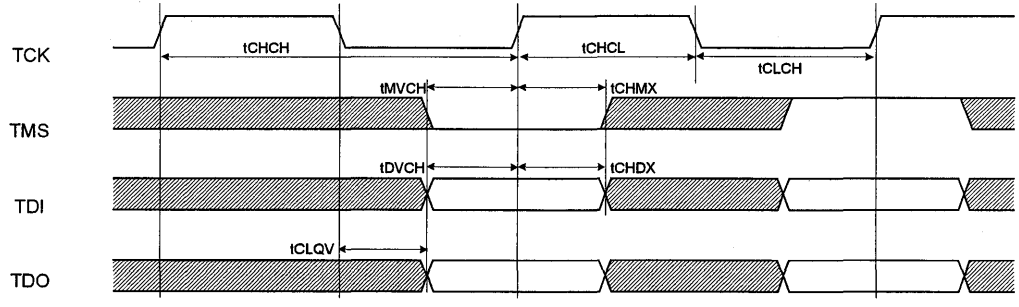
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	3.0/0.0	V	
Input Rise/Fall Time	TR/TF	2.0/2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

NOTE : 1. See SRAM AC test output load on page 5.

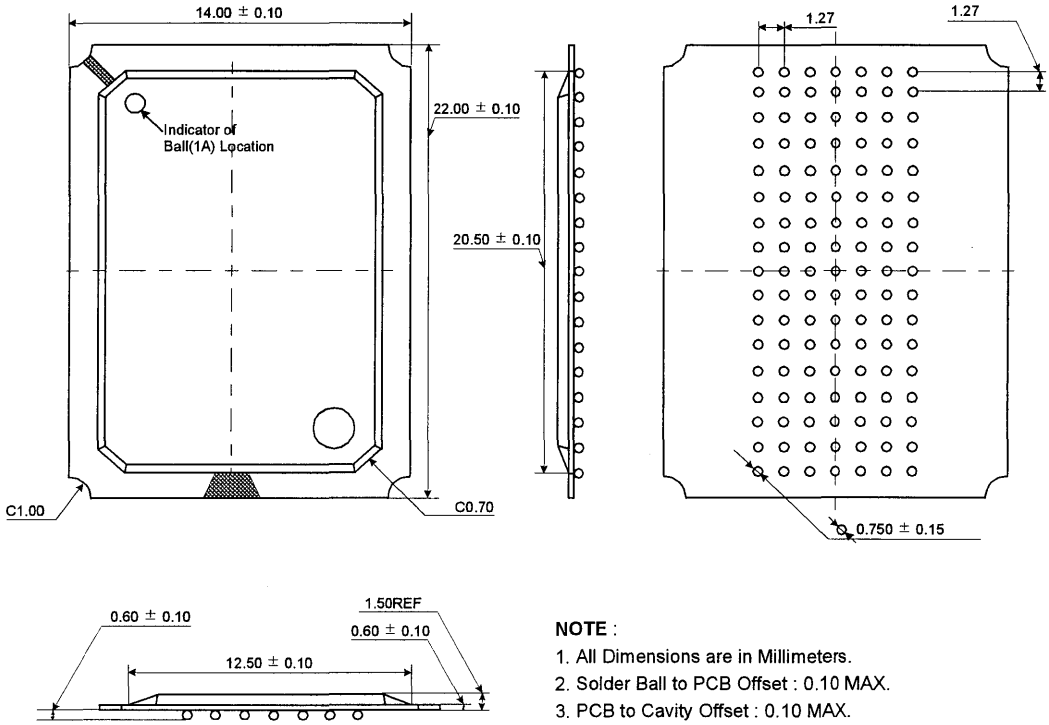
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	tCHCH	50	-	ns	
TCK High Pulse Width	tCHCL	20	-	ns	
TCK Low Pulse Width	tCLCH	20	-	ns	
TMS Input Setup Time	tMVCH	5	-	ns	
TMS Input Hold Time	tCHMX	5	-	ns	
TDI Input Setup Time	tDVCH	5	-	ns	
TDI Input Hold Time	tCHDX	5	-	ns	
Clock Low to Output Valid	tCLQV	0	10	ns	

JTAG TIMING DIAGRAM



119 BGA PACKAGE DIMENSIONS



NOTE :

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.

119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Junction to Ambient(at still air)	Theta_JA	-	-	50	℃/W	
Junction to Ambient(at air flow of 100 LFPM)	Theta_JA	-	-	40	℃/W	
Junction to Case	Theta_JC	-	-	8	℃/W	
Junction to Solder Ball	Theta_JB	-	-	10	℃/W	

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D \times Theta\_JA$.

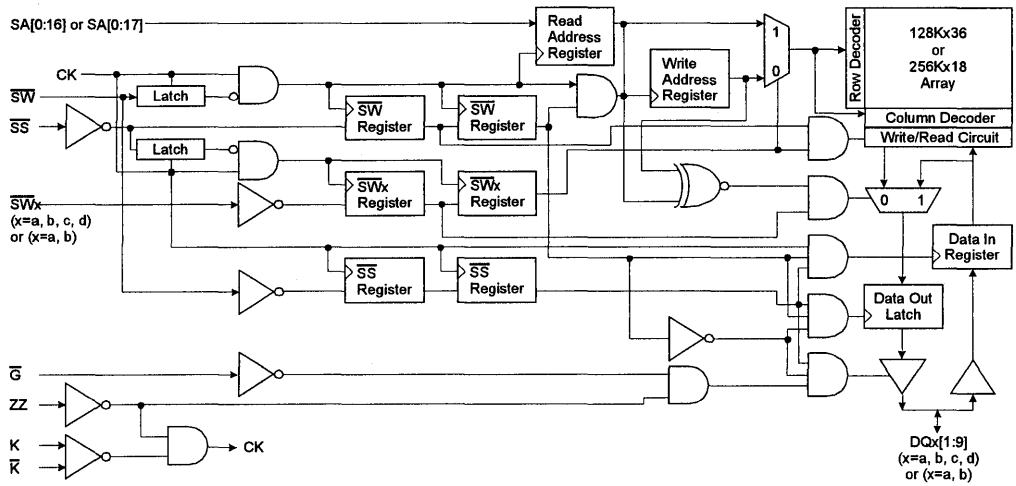
128Kx36 & 256Kx18 Synchronous Pipelined SRAM

FEATURES

- 128Kx36 or 256Kx18 Organizations.
- 3.3V Core/2.5V Output Power Supply.
- LVCMOS Input and Output Levels.
- Differential, PECL Clock Inputs K, $\overline{K}$.
- Synchronous Read and Write Operation
- Registered Input and Latched Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9 bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17) Pin Ball Grid Array Package(14mm x 22mm).

Organization	Part Number	Cycle Time	Access Time
128Kx36	KM736FV4002H-8	8	7.0
	KM736FV4002H-9	9	8.0
	KM736FV4002H-10	10	9.0
256Kx18	KM718FV4002H-8	8	7.0
	KM718FV4002H-9	9	8.0
	KM718FV4002H-10	10	9.0

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, $\overline{K}$	Differential Clocks(PECL Level)	C, $\overline{C}$	Differential Output Clocks
SAn	Synchronous Address Input	M_1, M_2	Read Protocol Mode Pins
DQn	Bi-directional Data Bus	$\overline{G}$	Asynchronous Output Enable
$\overline{SW}$	Synchronous Grobal Write Enable	$\overline{SS}$	Synchronous Select
$\overline{SW}a$	Synchronous Byte a Write Enable	TCK	JTAG Test Clock
$\overline{SW}b$	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
$\overline{SW}c$	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
$\overline{SW}d$	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	ZQ	Output Driver Impedance Control Input HSTL Level
V_{DD}	Core Power Supply	Vss	GND
V_{DDQ}	Output Power Supply	NC	No Connection
V_{REF}	HSTL Input Reference Voltage		

NOTE : 1. This SRAM only supports single clock, register-latch read protocol and have fixed impedance output driver. Therefore the following inputs must be set with power up and must not change during SRAM operation ; C=V_{DD}, $\overline{C}$=Vss, M_1=V_{DD}, M_2=Vss, ZQ=V_{DD} and V_{REF}=V_{DD}. But they are also designed to operate being left floating.

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

KM736FV4002(128Kx36)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA_{13}	SA_{10}	NC	SA_7	SA_4	V_{DDQ}
B	NC	NC	SA_9	NC	SA_8	NC	NC
C	NC	SA_{12}	SA_{11}	V_{DD}	SA_6	SA_5	NC
D	DQc8	DQc9	Vss	ZQ	Vss	DQb9	DQb8
E	DQc6	DQc7	Vss	$\overline{SS}$	Vss	DQb7	DQb6
F	V_{DDQ}	DQc5	Vss	$\overline{G}$	Vss	DQb5	V_{DDQ}
G	DQc3	DQc4	$\overline{SW}c$	$\overline{C}$	$\overline{SW}b$	DQb4	DQb3
H	DQc1	DQc2	Vss	C	Vss	DQb2	DQb1
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQd1	DQd2	Vss	K	Vss	DQa2	DQa1
L	DQd3	DQd4	$\overline{SW}d$	$\overline{K}$	$\overline{SW}a$	DQa4	DQa3
M	V_{DDQ}	DQd5	Vss	$\overline{SW}$	Vss	DQa5	V_{DDQ}
N	DQd6	DQd7	Vss	SA_{16}	Vss	DQa7	DQa6
P	DQd8	DQd9	Vss	SA_0	Vss	DQa9	DQa8
R	NC	SA_{15}	M_1	V_{DD}	M_2	SA_2	NC
T	NC	NC	SA_{14}	SA_1	SA_3	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

KM718FV4002(256Kx18)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA_{13}	SA_{10}	NC	SA_7	SA_4	V_{DDQ}
B	NC	NC	SA_9	NC	SA_8	NC	NC
C	NC	SA_{12}	SA_{11}	V_{DD}	SA_6	SA_5	NC
D	DQb1	NC	Vss	ZQ	Vss	DQa9	NC
E	NC	DQb2	Vss	$\overline{SS}$	Vss	NC	DQa8
F	V_{DDQ}	NC	Vss	$\overline{G}$	Vss	DQa7	V_{DDQ}
G	NC	DQb3	$\overline{SW}b$	$\overline{C}$	Vss	NC	DQa6
H	DQb4	NC	Vss	C	Vss	DQa5	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQb5	Vss	K	Vss	NC	DQa4
L	DQb6	NC	Vss	$\overline{K}$	$\overline{SW}a$	DQa3	NC
M	V_{DDQ}	DQb7	Vss	$\overline{SW}$	Vss	NC	V_{DDQ}
N	DQb8	NC	Vss	SA_{16}	Vss	DQa2	NC
P	NC	DQb9	Vss	SA_1	Vss	NC	DQa1
R	NC	SA_{15}	M_1	V_{DD}	M_2	SA_2	NC
T	NC	SA_{17}	SA_{14}	NC	SA_3	SA_0	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

FUNCTION DESCRIPTION

The KM736FV4002 and KM718FV4002 are 4,718,592 bit Synchronous SRAM. It is organized as 131,072 words of 36 bits(or 262, 144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology.
Single differential PECL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses , Write Enables, Synchronous Select and Data Ins are registered internally. Data outputs are updated from output latches of the falling edge of the K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During reads, the address is registered during the clock rising edge and the internal array is read. The data is driven to the CPU in the following cycle. $\overline{SS}$ is driven low during this cycle, signaling that the SRAM should drive out the data.
During consecutive read cycles where the address is the same, the data output must be held constantly without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and $\overline{SW}$ are both sampled on the clock rising edge. $\overline{SW}$ is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and $\overline{SW}$ have been sampled by the SRAM. $\overline{SS}$ will be driven low during the same cycle that the Address, $\overline{SW}$ and $\overline{SW}$[a:d] are valid to signal that a valid operations is on the Address and Control Input.
Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals $\overline{SW}$[a:d] signal which 9-bit bytes will be writen. Timing of $\overline{SW}$[a:d] is the same as the $\overline{SW}$ signal.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

Low Power Dissipation Mode

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time(tZZR) is required before the SRAM resumes to normal operation.

TRUTH TABLE

K	ZZ	$\overline{G}$	$\overline{SS}$	$\overline{SW}$	$\overline{SW}$a	$\overline{SW}$b	$\overline{SW}$c	$\overline{SW}$d	DQa	DQb	DQc	DQd	Operation
X	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
X	L	H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	H	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	L	H	X	X	X	X	DOUT	DOUT	DOUT	DOUT	Read Cycle
↑	L	L	L	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
↑	L	L	L	L	L	H	H	H	DIN	Hi-Z	Hi-Z	Hi-Z	Write first byte
↑	L	L	L	L	H	L	H	H	Hi-Z	DIN	Hi-Z	Hi-Z	Write second byte
↑	L	L	L	L	H	H	L	H	Hi-Z	Hi-Z	DIN	Hi-Z	Write third byte
↑	L	L	L	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte
↑	L	L	L	L	L	L	L	L	DIN	DIN	DIN	DIN	Write all byte

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	V_{DD}	-0.5 to 4.6	V
Output Supply Voltage Relative to Vss	V_{DDQ}	-0.5 to 4.6	V
Voltage on any I/O pin Relative to Vss	V_{TERM}	-0.5 to V_{DDQ}+0.5	V
Maximum Power Dissipation	P_D	2.5	W
Output Short-Circuit Current	I_{OUT}	25	mA
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature	T_{STG}	-55 to 125	℃

NOTE : Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	V_{DD}	3.15	3.3	3.45	V	
Output Power Supply Voltage	V_{DDQ}	2.4	2.5	2.6	V	
Input High Level	V_{IH}	1.7	-	V_{DD} + 0.3	V	1, 2
Input Low Level	V_{IL}	-0.3	-	0.7	V	1, 3
PECL Clock Input High Level	V_{IH}-PECL	2.135	-	2.420	V	1
PECL Clock Input Low Level	V_{IL}-PECL	1.490	-	1.825	V	1
Operating Junction Temperature	T_J	10	-	110	℃	4

NOTE :1. These are DC V_{IH}/V_{IH} spec. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
2. V_{IH} (Max)DC = V_{DD}+0.3V, V_{IH} (Max)AC = V_{DD}+1.5V(pulse width≤5ns).
3. V_{IL} (Min)DC = -0.3V, V_{IL} (Min)AC =-1.5V(pulse width≤5ns).
4. Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. T_J = T_A + P_D x THETA_JA

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (V_{IN}=V_{IH} or V_{IL}, ZZ & $\overline{SS}$=V_{IL})	I_{DD}	-	450	mA	1
Average Power Supply Operating Current-x18 (V_{IN}=V_{IH} or V_{IL}, ZZ & $\overline{SS}$=V_{IL})	I_{DD}	-	400	mA	1
Power Supply Standby Current (V_{IN}=V_{IH} or V_{IL}, ZZ =V_{IH})	I_{SB}	-	100	mA	1
Input Leakage Current (V_{IN}=Vss or V_{DD})	I_{LI}	-1	1	μA	
Output Leakage Current (V_{OUT}=Vss or V_{DD}, ZZ =V_{IH})	I_{LO}	-5	5	μA	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	2.0	V_{DDQ}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	Vss	0.4	V	

NOTE :1. Minimum cycle. I_{OUT}=0mA.

PIN CAPACITANCE

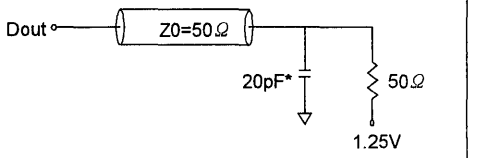
Parameter	Symbol	Pin Name	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	K, $\overline{K}$, $\overline{SS}$, $\overline{SW}$, $\overline{G}$, ZZ $\overline{SW}$x, ZQ, M1, M2, SAn, TCK, TMS, TDI	3	4	5	pF
Output Capacitance	C_{OUT}	DQn, TDO	5	6	7	pF

NOTE : Periodically sampled and 100% tested.(dV=0V, f=1MHz)

AC TEST CONDITIONS

Parameter	Symbol	Value	Unit
Input High/Low Level	V_{IH}/V_{IL}	2.5/0.0	V
Clock Input High/Low Level(PECL)	V_{IH}/V_{IL}	2.4/1.5	V
Input Rise/Fall Time	T_R/T_F	1.0/1.0	ns
Clock Input Rise/Fall Time(PECL)	T_R/T_F	0.5/0.5	ns
Output Rise/Fall Time	T_R/T_F	0.5~1.0	ns
Input and Out Timing Reference Level		1.25	V
Clock Input Timing Reference Level		Cross Point	V

AC TEST OUTPUT LOAD

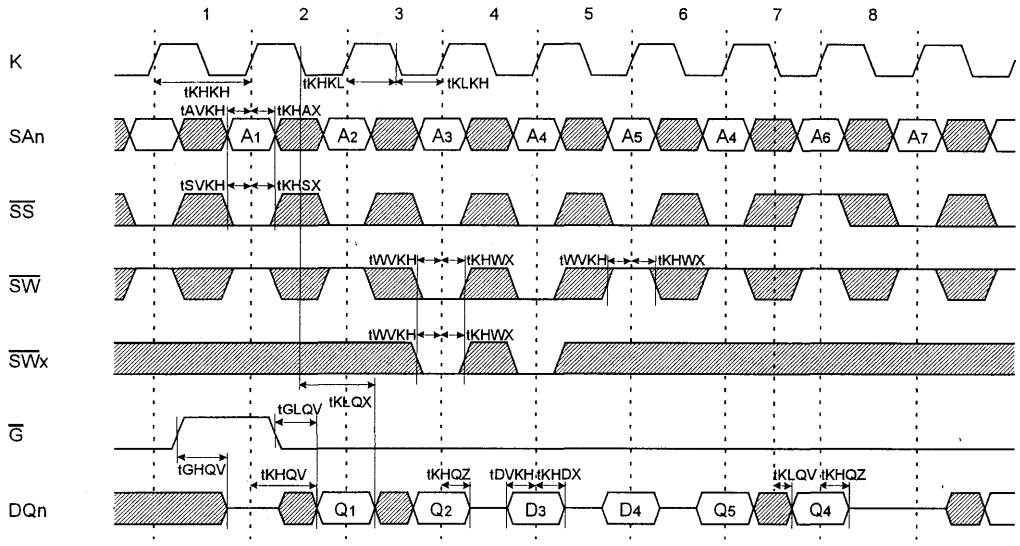


*Capacitive load consists of all components of the tester environment

AC CHARACTERISTICS

Parameter	Symbol	-8		-9		-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	tKHKH	8.0	-	9.0	-	10.0	-	ns	
Clock High Pulse Width	tKHKL	3.2	-	3.6	-	4.0	-	ns	
Clock Low Pulse Width	tKLKH	3.2	-	3.6	-	4.0	-	ns	
Clock High to Output Valid	tKHQV	-	7.0	-	8.0	-	9.0	ns	
Clock Low to Output Valid	tKLQV	-	2.5	-	3.0	-	3.5	ns	
Clock Low to Output Hold	tKLQX	1.0	-	1.0	-	1.0	-	ns	
Address Setup Time	tAVKH	0.5	-	0.5	-	0.1	-	ns	
Address Hold Time	tKHAX	1.0	-	1.0	-	1.0	-	ns	
Write Data Setup Time	tDVKH	0.5	-	0.5	-	0.5	-	ns	
Write Data Hold Time	tKHDX	1.0	-	1.0	-	1.0	-	ns	
$\overline{SW}$, $\overline{SW}$[a:d] Setup Time	tWVKH	0.5	-	0.5	-	0.5	-	ns	
$\overline{SW}$, $\overline{SW}$[a:d] Hold Time	tKHWX	1.0	-	1.0	-	1.0	-	ns	
$\overline{SS}$ Setup Time	tSVKH	0.5	-	0.5	-	0.5	-	ns	
$\overline{SS}$ Hold Time	tKHSX	1.0	-	1.0	-	1.0	-	ns	
Clock High to Output Hi-Z	tKHQZ	-	2.5	-	3.0	-	3.5	ns	
Clock Low to Output Low-Z	tKHQX1	1.0	-	1.0	-	1.0	-	ns	
$\overline{G}$ High to Output High-Z	tGHQZ	-	2.5	-	3.0	-	3.5	ns	
$\overline{G}$ Low to Output Low-Z	tGLQX	0.5	-	0.5	-	0.5	-	ns	
$\overline{G}$ Low to Output Valid	tGLQV	-	2.5	-	3.0	-	3.5	ns	
ZZ High to Power Down(Sleep Time)	tZZE	-	8.0	-	9.0	-	10.0	ns	
ZZ Low to Recovery(Wake-up Time)	tZZR	-	8.0	-	9.0	-	10.0	ns	

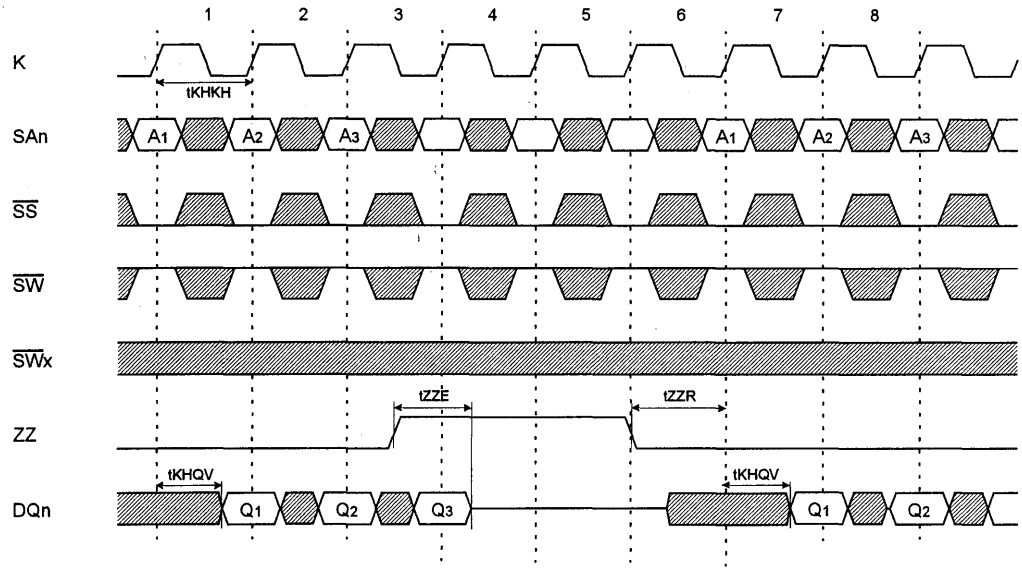
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES



NOTE :

1. D_3 is the input data written in memory location A_3.
2. Q_4 is the output data read from the write data buffer(not from the cell array), as a result of address A_4 being a match from the last write cycle address.
3. Data is valid at the output at the later of tKHQV following the rising clock edge, or tKLQV following the fallowing clock edge.
4. When $\overline{SS}$ is sampled high or $\overline{SW}$ is sampled low on the rising edge of clock, the outputs go into Hi-Z state no later than tKHQZ following the rising clock edge.
5. When $\overline{SS}$ is low and $\overline{SW}$ is high on the rising edge of clock, the outputs go into Low-Z state(being driven) no earlier than tKHQX following the next falling edge of clock.
6. When the SRAM is deselected, the output goes Hi-Z at tKHQZ following the rising clock edge. On the next read cycle, note that the SRAM output do not leave the Hi-Z state until tKLQX after the falling clock edge.

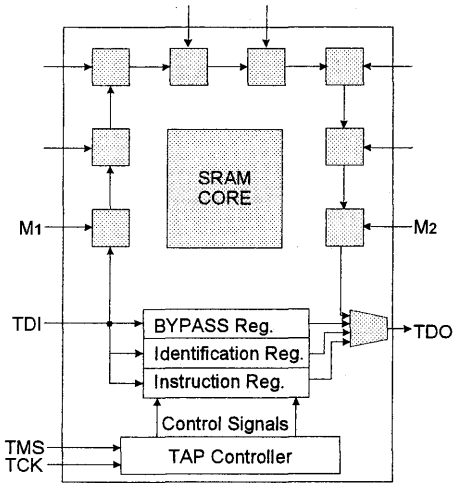
TIMING WAVEFORMS OF STANDBY CYCLES



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



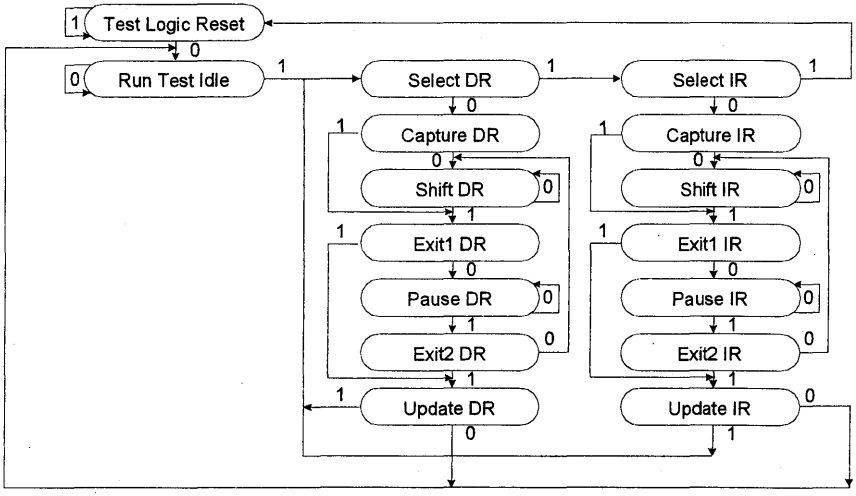
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	000000	00001001110	1
256Kx18	0000	00110 00011	000000	00001001110	1

BOUNDARY SCAN EXIT ORDER(x36)

36	3B	SA_9		SA_8	5B	35
37	2B	NC		NC	6B	34
38	3A	SA_{10}		SA_7	5A	33
39	3C	SA_{11}		SA_6	5C	32
40	2C	SA_{12}		SA_5	6C	31
41	2A	SA_{13}		SA_4	6A	30
42	2D	DQc9		DQb9	6D	29
43	1D	DQc8		DQb8	7D	28
44	2E	DQc7		DQb7	6E	27
45	1E	DQc6		DQb6	7E	26
46	2F	DQc5		DQb5	6F	25
47	2G	DQc4		DQb4	6G	24
48	1G	DQc3		DQb3	7G	23
49	2H	DQc2		DQb2	6H	22
50	1H	DQc1		DQb1	7H	21
51	3G	$\overline{SW}c$		$\overline{SW}b$	5G	20
52	4D	ZQ		$\overline{G}$	4F	19
53	4E	$\overline{SS}$		K	4K	18
54	4G	$\overline{C}$		$\overline{K}$	4L	17
55	4H	C		$\overline{SW}a$	5L	16
56	4M	$\overline{SW}$		DQa1	7K	15
57	3L	$\overline{SW}d$		DQa2	6K	14
58	1K	DQd1		DQa3	7L	13
59	2K	DQd2		DQa4	6L	12
60	1L	DQd3		DQa5	6M	11
61	2L	DQd4		DQa6	7N	10
62	2M	DQd5		DQa7	6N	9
63	1N	DQd6		DQa8	7P	8
64	2N	DQd7		DQa9	6P	7
65	1P	DQd8		ZZ	7T	6
66	2P	DQd9		SA_3	5T	5
67	3T	SA_{14}		SA_2	6R	4
68	2R	SA_{15}		SA_1	4T	3
69	4N	SA_{16}		SA_0	4P	2
70	3R	M_1		M_2	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

26	3B	SA_9		SA_8	5B	25
27	2B	NC		NC	6B	24
28	3A	SA_{10}		SA_7	5A	23
29	3C	SA_{11}		SA_6	5C	22
30	2C	SA_{12}		SA_5	6C	21
31	2A	SA_{13}		SA_4	6A	20
				DQa9	6D	19
32	1D	DQb1				
33	2E	DQb2				
				DQa8	7E	18
				DQa7	6F	17
34	2G	DQb3				
				DQa6	7G	16
				DQa5	6H	15
35	1H	DQb4				
36	3G	$\overline{SW}b$				
37	4D	ZQ		$\overline{G}$	4F	14
38	4E	$\overline{SS}$		K	4K	13
39	4G	$\overline{C}$		$\overline{K}$	4L	12
40	4H	C		$\overline{SW}a$	5L	11
41	4M	$\overline{SW}$		DQa4	7K	10
42	2K	DQb5		DQa3	6L	9
43	1L	DQb6				
44	2M	DQb7		DQa2	6N	8
45	1N	DQb8		DQa1	7P	7
				ZZ	7T	6
46	2P	DQb9		SA_3	5T	5
47	3T	SA_{14}		SA_2	6R	4
48	2R	SA_{15}				
49	4N	SA_{16}		SA_1	4P	3
50	2T	SA_{17}		SA_0	6T	2
51	3R	M_1		M_2	5R	1

NOTE: 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	3.15	3.3	3.45	V	
Input High Level	V_{IH}	2.0	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.8	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	2.4	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	Vss	-	0.4	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

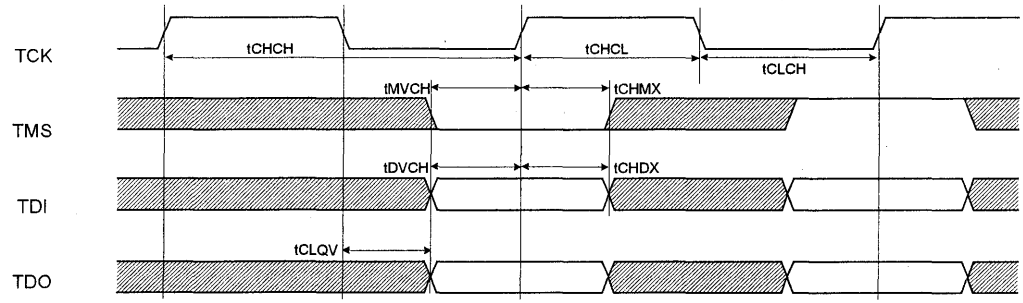
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	3.0/0.0	V	
Input Rise/Fall Time	TR/TF	2.0/2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

NOTE : 1. See SRAM AC test output load on page 5.

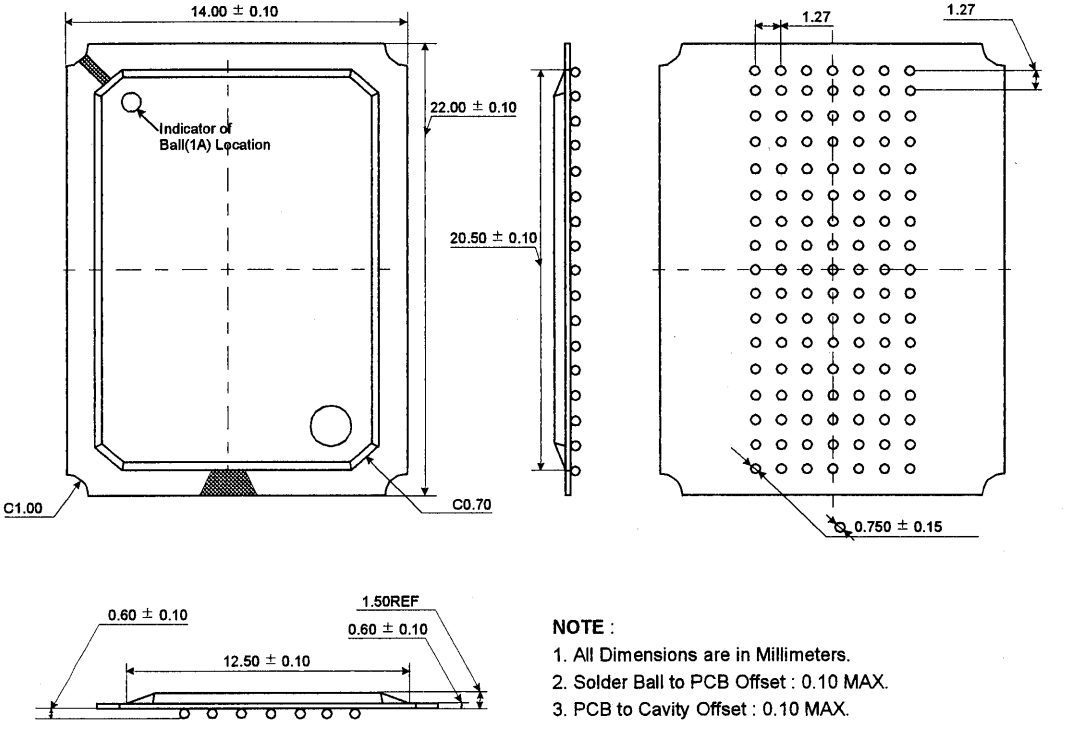
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	tCHCH	50	-	ns	
TCK High Pulse Width	tCHCL	20	-	ns	
TCK Low Pulse Width	tCLCH	20	-	ns	
TMS Input Setup Time	tMVCH	5	-	ns	
TMS Input Hold Time	tCHMX	5	-	ns	
TDI Input Setup Time	tDVCH	5	-	ns	
TDI Input Hold Time	tCHDX	5	-	ns	
Clock Low to Output Valid	tCLQV	0	10	ns	

JTAG TIMING DIAGRAM



119 BGA PACKAGE DIMENSIONS



NOTE :

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.

119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Junction to Ambient(at still air)	Theta_JA	-	-	50	°C/W	
Junction to Ambient(at air flow of 100 LFPM)	Theta_JA	-	-	40	°C/W	
Junction to Case	Theta_JC	-	-	8	°C/W	
Junction to Solder Ball	Theta_JB	-	-	10	°C/W	

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D \times Theta\_JA$.

128Kx36 & 256Kx18 Synchronous Pipelined SRAM

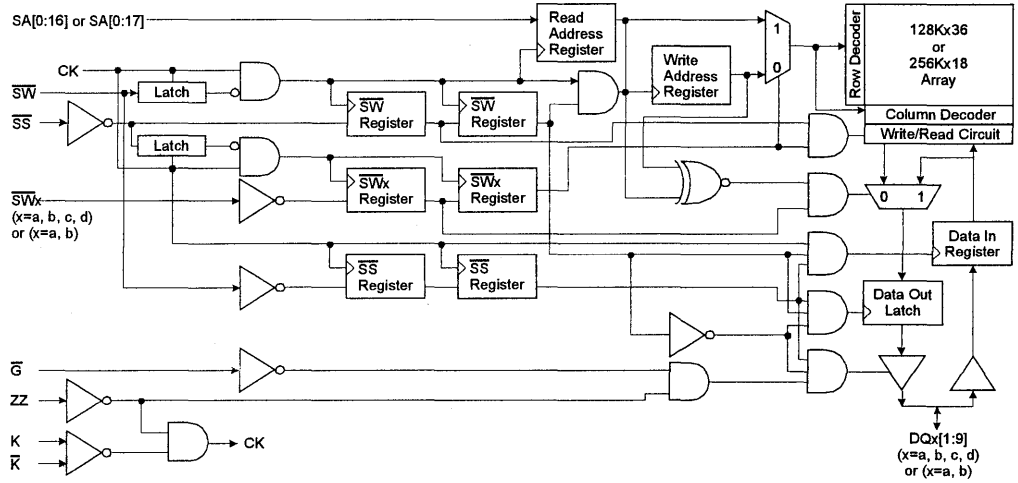
FEATURES

- 128Kx36 or 256Kx18 Organizations.
- 3.3V Core/ Output Power Supply.
- LVTTL 3.3V Input and Output Levels.
- Differential, PECL Clock Inputs K, $\overline{K}$.
- Synchronous Read and Write Operation
- Registered Input and Latched Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9 bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17) Pin Ball Grid Array Package(14mm x 22mm).

Organization	Part Number	Cycle Time	Access Time
128Kx36	KM736FV4022H-8	8	7.0
	KM736FV4022H-9	9	8.0
	KM736FV4022H-10	10	9.0
256Kx18	KM718FV4022H-8	8	7.0
	KM718FV4022H-9	9	8.0
	KM718FV4022H-10	10	9.0

2

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, $\overline{K}$	Differential Clocks(PECL Level)	C, $\overline{C}$	Differential Output Clocks
SAn	Synchronous Address Input	M1, M2	Read Protocol Mode Pins
DQn	Bi-directional Data Bus	$\overline{G}$	Asynchronous Output Enable
$\overline{SW}$	Synchronous Grobal Write Enable	$\overline{SS}$	Synchronous Select
$\overline{SW}$a	Synchronous Byte a Write Enable	TCK	JTAG Test Clock
$\overline{SW}$b	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
$\overline{SW}$c	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
$\overline{SW}$d	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	ZQ	Output Driver Impedance Control Input HSTL Level
V_{DD}	Core Power Supply	Vss	GND
V_{DDQ}	Output Power Supply	NC	No Connection
V_{REF}	HSTL Input Reference Voltage		

NOTE : 1. This SRAM only supports single clock, register-latch read protocol and have fixed impedance output driver. Therefore the following inputs must be set with power up and must not change during SRAM operation ; C=V_{DD}, $\overline{C}$=Vss, M1=V_{DD}, M2=Vss, ZQ=V_{DD} and V_{REF}=V_{DD}. But they are also designed to operate being left floating.

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

KM736FV4022(128Kx36)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA_{13}	SA_{10}	NC	SA_7	SA_4	V_{DDQ}
B	NC	NC	SA_9	NC	SA_8	NC	NC
C	NC	SA_{12}	SA_{11}	V_{DD}	SA_6	SA_5	NC
D	DQc8	DQc9	Vss	ZQ	Vss	DQb9	DQb8
E	DQc6	DQc7	Vss	$\overline{SS}$	Vss	DQb7	DQb6
F	V_{DDQ}	DQc5	Vss	$\overline{G}$	Vss	DQb5	V_{DDQ}
G	DQc3	DQc4	$\overline{SW}c$	$\overline{C}$	$\overline{SW}b$	DQb4	DQb3
H	DQc1	DQc2	Vss	C	Vss	DQb2	DQb1
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQd1	DQd2	Vss	K	Vss	DQa2	DQa1
L	DQd3	DQd4	$\overline{SW}d$	$\overline{K}$	$\overline{SW}a$	DQa4	DQa3
M	V_{DDQ}	DQd5	Vss	$\overline{SW}$	Vss	DQa5	V_{DDQ}
N	DQd6	DQd7	Vss	SA_{16}	Vss	DQa7	DQa6
P	DQd8	DQd9	Vss	SA_0	Vss	DQa9	DQa8
R	NC	SA_{15}	M_1	V_{DD}	M_2	SA_2	NC
T	NC	NC	SA_{14}	SA_1	SA_3	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

KM718FV4022(256Kx18)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA_{13}	SA_{10}	NC	SA_7	SA_4	V_{DDQ}
B	NC	NC	SA_9	NC	SA_8	NC	NC
C	NC	SA_{12}	SA_{11}	V_{DD}	SA_6	SA_5	NC
D	DQb1	NC	Vss	ZQ	Vss	DQa9	NC
E	NC	DQb2	Vss	$\overline{SS}$	Vss	NC	DQa8
F	V_{DDQ}	NC	Vss	$\overline{G}$	Vss	DQa7	V_{DDQ}
G	NC	DQb3	$\overline{SW}b$	$\overline{C}$	Vss	NC	DQa6
H	DQb4	NC	Vss	C	Vss	DQa5	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQb5	Vss	K	Vss	NC	DQa4
L	DQb6	NC	Vss	$\overline{K}$	$\overline{SW}a$	DQa3	NC
M	V_{DDQ}	DQb7	Vss	$\overline{SW}$	Vss	NC	V_{DDQ}
N	DQb8	NC	Vss	SA_{16}	Vss	DQa2	NC
P	NC	DQb9	Vss	SA_1	Vss	NC	DQa1
R	NC	SA_{15}	M_1	V_{DD}	M_2	SA_2	NC
T	NC	SA_{17}	SA_{14}	NC	SA_3	SA_0	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

FUNCTION DESCRIPTION

The KM736FV4022 and KM718FV4022 are 4,718,592 bit Synchronous SRAM. It is organized as 131,072 words of 36 bits(or 262, 144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology.
Single differential PECL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses , Write Enables, Synchronous Select and Data Ins are registered internally. Data outputs are updated from output latches of the falling edge of the K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During reads, the address is registered during the clock rising edge and the internal array is read. The data is driven to the CPU in the following cycle. $\overline{SS}$ is driven low during this cycle, signaling that the SRAM should drive out the data.
During consecutive read cycles where the address is the same, the data output must be held constantly without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and $\overline{SW}$ are both sampled on the clock rising edge. $\overline{SW}$ is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and $\overline{SW}$ have been sampled by the SRAM. $\overline{SS}$ will be driven low during the same cycle that the Address, $\overline{SW}$ and $\overline{SW}$[a:d] are valid to signal that a valid operations is on the Address and Control Input.
Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles.
Byte writes are supported. The byte write signals $\overline{SW}$[a:d] signal which 9-bit bytes will be writen. Timing of $\overline{SW}$[a:d] is the same as the $\overline{SW}$ signal.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

Low Power Dissipation Mode

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time(tZZR) is required before the SRAM resumes to normal operation.

TRUTH TABLE

K	ZZ	$\overline{G}$	$\overline{SS}$	$\overline{SW}$	$\overline{SW}$a	$\overline{SW}$b	$\overline{SW}$c	$\overline{SW}$d	DQa	DQb	DQc	DQd	Operation
X	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
X	L	H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	H	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	L	H	X	X	X	X	DOUT	DOUT	DOUT	DOUT	Read Cycle
↑	L	L	L	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
↑	L	L	L	L	L	H	H	H	DIN	Hi-Z	Hi-Z	Hi-Z	Write first byte
↑	L	L	L	L	H	L	H	H	Hi-Z	DIN	Hi-Z	Hi-Z	Write second byte
↑	L	L	L	L	H	H	L	H	Hi-Z	Hi-Z	DIN	Hi-Z	Write third byte
↑	L	L	L	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte
↑	L	L	L	L	L	L	L	L	DIN	DIN	DIN	DIN	Write all byte

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	V_{DD}	-0.5 to 4.6	V
Output Supply Voltage Relative to Vss	V_{DDQ}	-0.5 to 4.6	V
Voltage on any I/O pin Relative to Vss	V_{TERM}	-0.5 to V_{DDQ}+0.5	V
Maximum Power Dissipation	P_D	2.5	W
Output Short-Circuit Current	I_{OUT}	25	mA
Operating Temperature	T_{OPR}	0 to 70	℃
Storage Temperature	T_{STG}	-55 to 125	℃

NOTE : Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	V_{DD}	3.15	3.3	3.45	V	
Output Power Supply Voltage	V_{DDQ}	3.15	3.3	3.45	V	
Input High Level	V_{IH}	2.0	-	V_{DD} + 0.3	V	1, 2
Input Low Level	V_{IL}	-0.3	-	0.8	V	1, 3
PECL Clock Input High Level	V_{IH}-PECL	2.135	-	2.420	V	1
PECL Clock Input Low Level	V_{IL}-PECL	1.490	-	1.825	V	1
Operating Junction Temperature	T_J	10	-	110	℃	4

NOTE :1. These are DC V_{IH}/V_{IH} spec. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
2. V_{IH} (Max)DC = V_{DD}+0.3V, V_{IH} (Max)AC = V_{DD}+1.5V(pulse width$\leq$5ns).
3. V_{IL} (Min)DC = -0.3V, V_{IL} (Min)AC =-1.5V(pulse width$\leq$5ns).
4. Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. T_J = T_A + P_D x $THETA_JA$

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (V_{IN}=V_{IH} or V_{IL}, ZZ & $\overline{SS}$=V_{IL})	I_{DD}	-	450	mA	1
Average Power Supply Operating Current-x18 (V_{IN}=V_{IH} or V_{IL}, ZZ & $\overline{SS}$=V_{IL})	I_{DD}	-	400	mA	1
Power Supply Standby Current (V_{IN}=V_{IH} or V_{IL}, ZZ =V_{IH})	I_{SB}	-	100	mA	1
Input Leakage Current (V_{IN}=Vss or V_{DD})	I_{LI}	-1	1	μA	
Output Leakage Current (V_{OUT}=Vss or V_{DD}, ZZ =V_{IH})	I_{LO}	-5	5	μA	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	2.4	V_{DDQ}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	Vss	0.4	V	

NOTE :1. Minimum cycle. I_{OUT}=0mA.

PIN CAPACITANCE

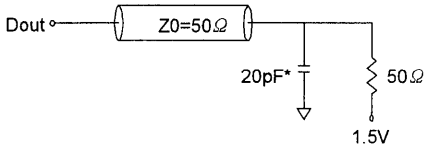
Parameter	Symbol	Pin Name	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	K, $\overline{K}$, $\overline{SS}$, $\overline{SW}$, $\overline{G}$, ZZ $\overline{SW}$x, ZQ, M_1, M_2, SAn, TCK, TMS, TDI	3	4	5	pF
Output Capacitance	C_{OUT}	DQn, TDO	5	6	7	pF

NOTE : Periodically sampled and 100% tested.(dV=0V, f=1MHz)

AC TEST CONDITIONS

Parameter	Symbol	Value	Unit
Input High/Low Level	V_{IH}/V_{IL}	3.0/0.0	V
Clock Input High/Low Level(PECL)	V_{IH}/V_{IL}	2.4/1.5	V
Input Rise/Fall Time	T_R/T_F	1.0/1.0	ns
Clock Input Rise/Fall Time(PECL)	T_R/T_F	0.5/0.5	ns
Output Rise/Fall Time	T_R/T_F	0.5~1.0	ns
Input and Out Timing Reference Level		1.5	V
Clock Input Timing Reference Level		Cross Point	V

AC TEST OUTPUT LOAD

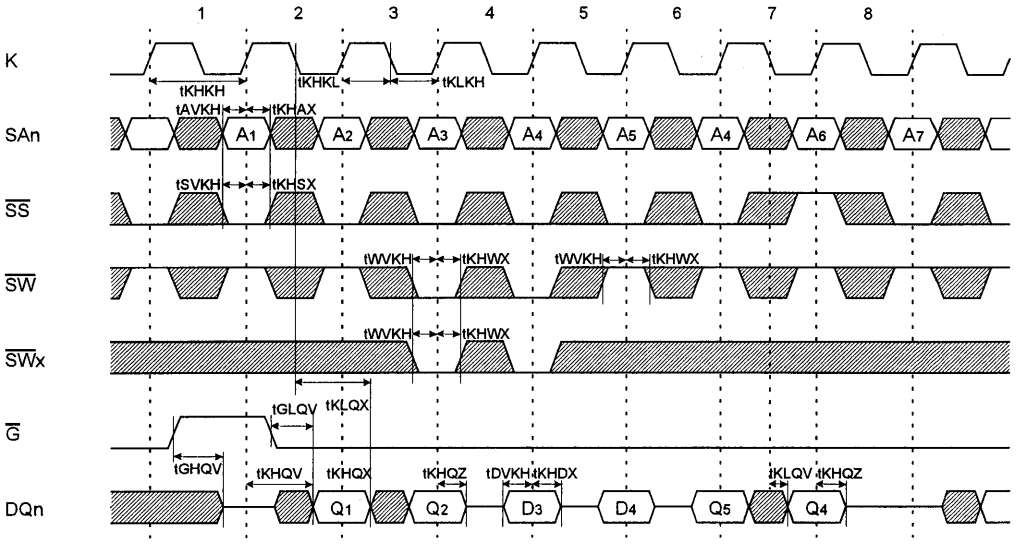


*Capacitive load consists of all components of the tester environment

AC CHARACTERISTICS

Parameter	Symbol	-8		-9		-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	tKHKH	8.0	-	9.0	-	10.0	-	ns	
Clock High Pulse Width	tKHKL	3.2	-	3.6	-	4.0	-	ns	
Clock Low Pulse Width	tKLKH	3.2	-	3.6	-	4.0	-	ns	
Clock High to Output Valid	tKHQV	-	7.0	-	8.0	-	9.0	ns	
Clock Low to Output Valid	tKLQV	-	2.5	-	3.0	-	3.5	ns	
Clock Low to Output Hold	tKLQX	1.0	-	1.0	-	1.0	-	ns	
Address Setup Time	tAVKH	0.5	-	0.5	-	0.1	-	ns	
Address Hold Time	tKHAX	1.0	-	1.0	-	1.0	-	ns	
Write Data Setup Time	tDVKH	0.5	-	0.5	-	0.5	-	ns	
Write Data Hold Time	tKHDX	1.0	-	1.0	-	1.0	-	ns	
$\overline{SW}$, $\overline{SW}$[a:d] Setup Time	tWVKH	0.5	-	0.5	-	0.5	-	ns	
$\overline{SW}$, $\overline{SW}$[a:d] Hold Time	tKHWX	1.0	-	1.0	-	1.0	-	ns	
$\overline{SS}$ Setup Time	tSVKH	0.5	-	0.5	-	0.5	-	ns	
$\overline{SS}$ Hold Time	tKHSX	1.0	-	1.0	-	1.0	-	ns	
Clock High to Output Hi-Z	tKHQZ	-	2.5	-	3.0	-	3.5	ns	
Clock Low to Output Low-Z	tKHQX1	1.0	-	1.0	-	1.0	-	ns	
$\overline{G}$ High to Output High-Z	tGHQZ	-	2.5	-	3.0	-	3.5	ns	
$\overline{G}$ Low to Output Low-Z	tGLQX	0.5	-	0.5	-	0.5	-	ns	
$\overline{G}$ Low to Output Valid	tGLQV	-	2.5	-	3.0	-	3.5	ns	
ZZ High to Power Down(Sleep Time)	tZZE	-	8.0	-	9.0	-	10.0	ns	
ZZ Low to Recovery(Wake-up Time)	tZZR	-	8.0	-	9.0	-	10.0	ns	

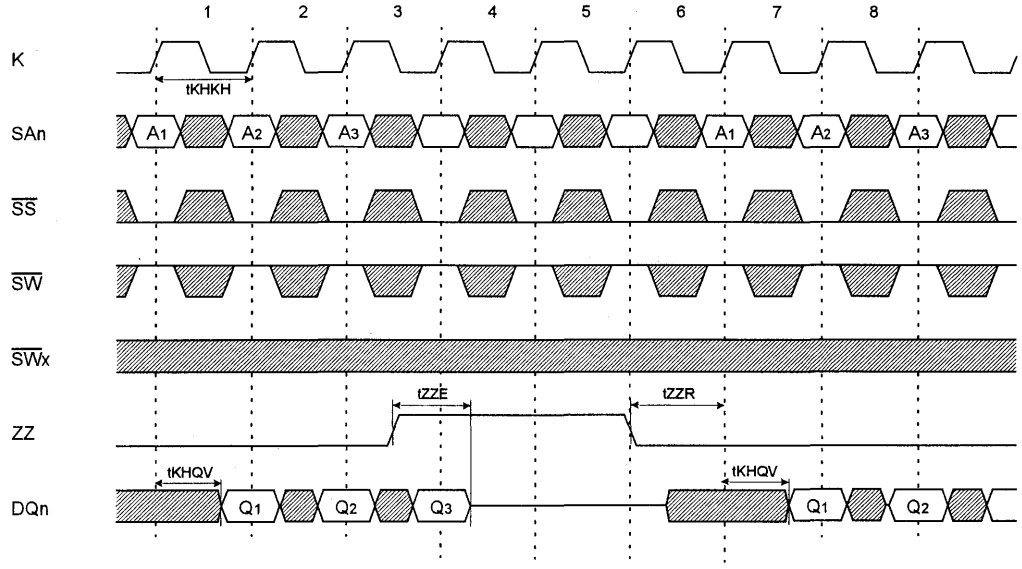
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES



NOTE :

1. D_3 is the input data written in memory location A_3.
2. Q_4 is the output data read from the write data buffer(not from the cell array), as a result of address A_4 being a match from the last write cycle address.
3. Data is valid at the output at the later of tKHQV following the rising clock edge, or tKLQV following the fallowing clock edge.
4. When $\overline{SS}$ is sampled high or $\overline{SW}$ is sampled low on the rising edge of clock, the outputs go into Hi-Z state no later than tKHQZ following the rising clock edge.
5. When $\overline{SS}$ is low and $\overline{SW}$ is high on the rising edge of clock, the outputs go into Low-Z state(being driven) no earlier than tKHQX following the next falling edge of clock.
6. When the SRAM is deselected, the output goes Hi-Z at tKHQZ following the rising clock edge. On the next read cycle, note that the SRAM output do not leave the Hi-Z state until tKLQX after the falling clock edge.

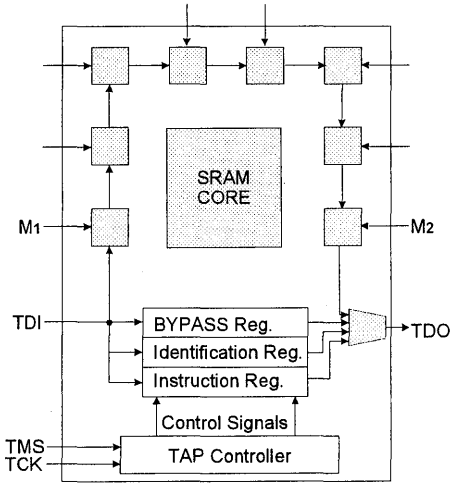
TIMING WAVEFORMS OF STANDBY CYCLES



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



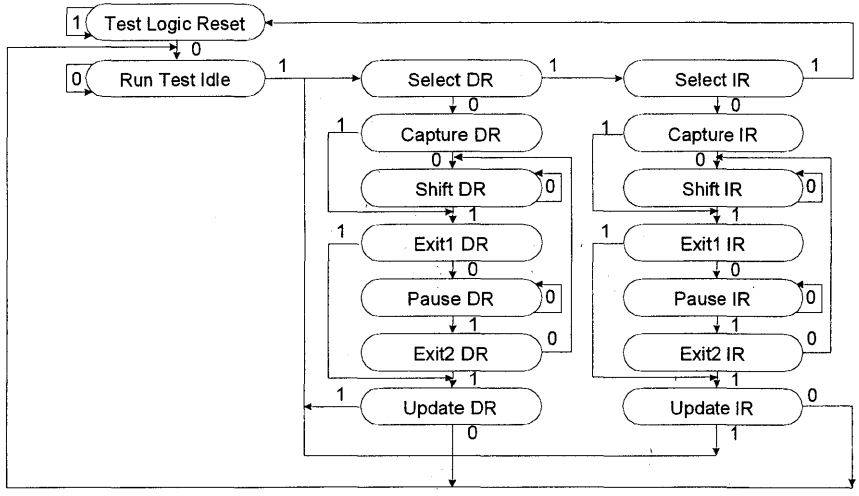
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	000000	00001001110	1
256Kx18	0000	00110 00011	000000	00001001110	1

BOUNDARY SCAN EXIT ORDER(x36)

36	3B	SA_9		SA_8	5B	35
37	2B	NC		NC	6B	34
38	3A	SA_{10}		SA_7	5A	33
39	3C	SA_{11}		SA_6	5C	32
40	2C	SA_{12}		SA_5	6C	31
41	2A	SA_{13}		SA_4	6A	30
42	2D	DQc9		DQb9	6D	29
43	1D	DQc8		DQb8	7D	28
44	2E	DQc7		DQb7	6E	27
45	1E	DQc6		DQb6	7E	26
46	2F	DQc5		DQb5	6F	25
47	2G	DQc4		DQb4	6G	24
48	1G	DQc3		DQb3	7G	23
49	2H	DQc2		DQb2	6H	22
50	1H	DQc1		DQb1	7H	21
51	3G	$\overline{SWc}$		$\overline{SWb}$	5G	20
52	4D	ZQ		$\overline{G}$	4F	19
53	4E	$\overline{SS}$		K	4K	18
54	4G	$\overline{C}$		$\overline{K}$	4L	17
55	4H	C		$\overline{SWa}$	5L	16
56	4M	$\overline{SW}$		DQa1	7K	15
57	3L	$\overline{SWd}$		DQa2	6K	14
58	1K	DQd1		DQa3	7L	13
59	2K	DQd2		DQa4	6L	12
60	1L	DQd3		DQa5	6M	11
61	2L	DQd4		DQa6	7N	10
62	2M	DQd5		DQa7	6N	9
63	1N	DQd6		DQa8	7P	8
64	2N	DQd7		DQa9	6P	7
65	1P	DQd8		ZZ	7T	6
66	2P	DQd9		SA_3	5T	5
67	3T	SA_{14}		SA_2	6R	4
68	2R	SA_{15}		SA_1	4T	3
69	4N	SA_{16}		SA_0	4P	2
70	3R	M_1		M_2	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

26	3B	SA_9		SA_8	5B	25
27	2B	NC		NC	6B	24
28	3A	SA_{10}		SA_7	5A	23
29	3C	SA_{11}		SA_6	5C	22
30	2C	SA_{12}		SA_5	6C	21
31	2A	SA_{13}		SA_4	6A	20
				DQa9	6D	19
32	1D	DQb1				
33	2E	DQb2				
				DQa8	7E	18
				DQa7	6F	17
34	2G	DQb3				
				DQa6	7G	16
				DQa5	6H	15
35	1H	DQb4				
36	3G	$\overline{SWb}$				
37	4D	ZQ		$\overline{G}$	4F	14
38	4E	$\overline{SS}$		K	4K	13
39	4G	$\overline{C}$		$\overline{K}$	4L	12
40	4H	C		$\overline{SWa}$	5L	11
41	4M	$\overline{SW}$		DQa4	7K	10
42	2K	DQb5		DQa3	6L	9
43	1L	DQb6				
44	2M	DQb7		DQa2	6N	8
45	1N	DQb8		DQa1	7P	7
				ZZ	7T	6
46	2P	DQb9		SA_3	5T	5
47	3T	SA_{14}		SA_2	6R	4
48	2R	SA_{15}				
49	4N	SA_{16}		SA_1	4P	3
50	2T	SA_{17}		SA_0	6T	2
51	3R	M_1		M_2	5R	1

NOTE : 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	3.15	3.3	3.45	V	
Input High Level	V_{IH}	2.0	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.8	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	2.4	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	Vss	-	0.4	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

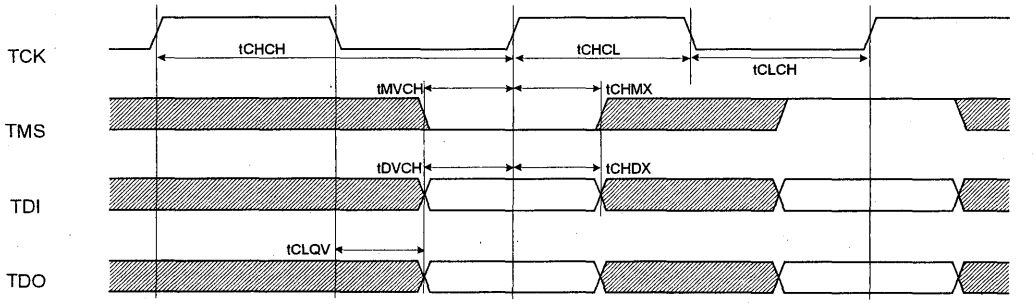
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	3.0/0.0	V	
Input Rise/Fall Time	TR/TF	2.0/2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

NOTE : 1. See SRAM AC test output load on page 5.

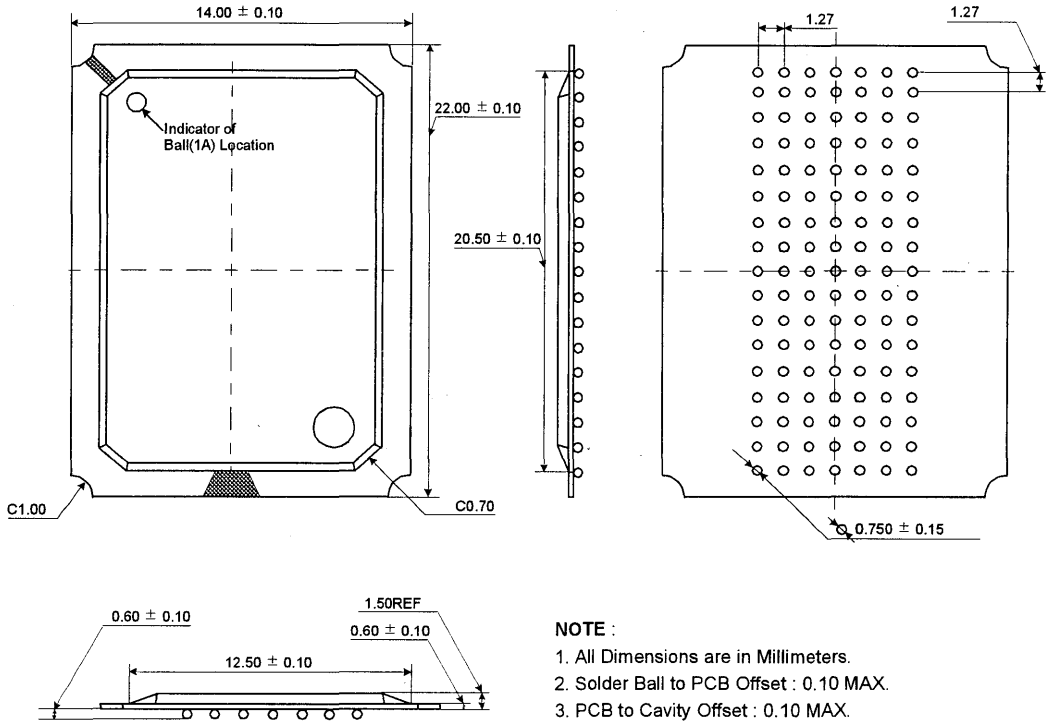
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	tCHCH	50	-	ns	
TCK High Pulse Width	tCHCL	20	-	ns	
TCK Low Pulse Width	tCLCH	20	-	ns	
TMS Input Setup Time	tMVCH	5	-	ns	
TMS Input Hold Time	tCHMX	5	-	ns	
TDI Input Setup Time	tDVCH	5	-	ns	
TDI Input Hold Time	tCHDX	5	-	ns	
Clock Low to Output Valid	tCLQV	0	10	ns	

JTAG TIMING DIAGRAM



119 BGA PACKAGE DIMENSIONS



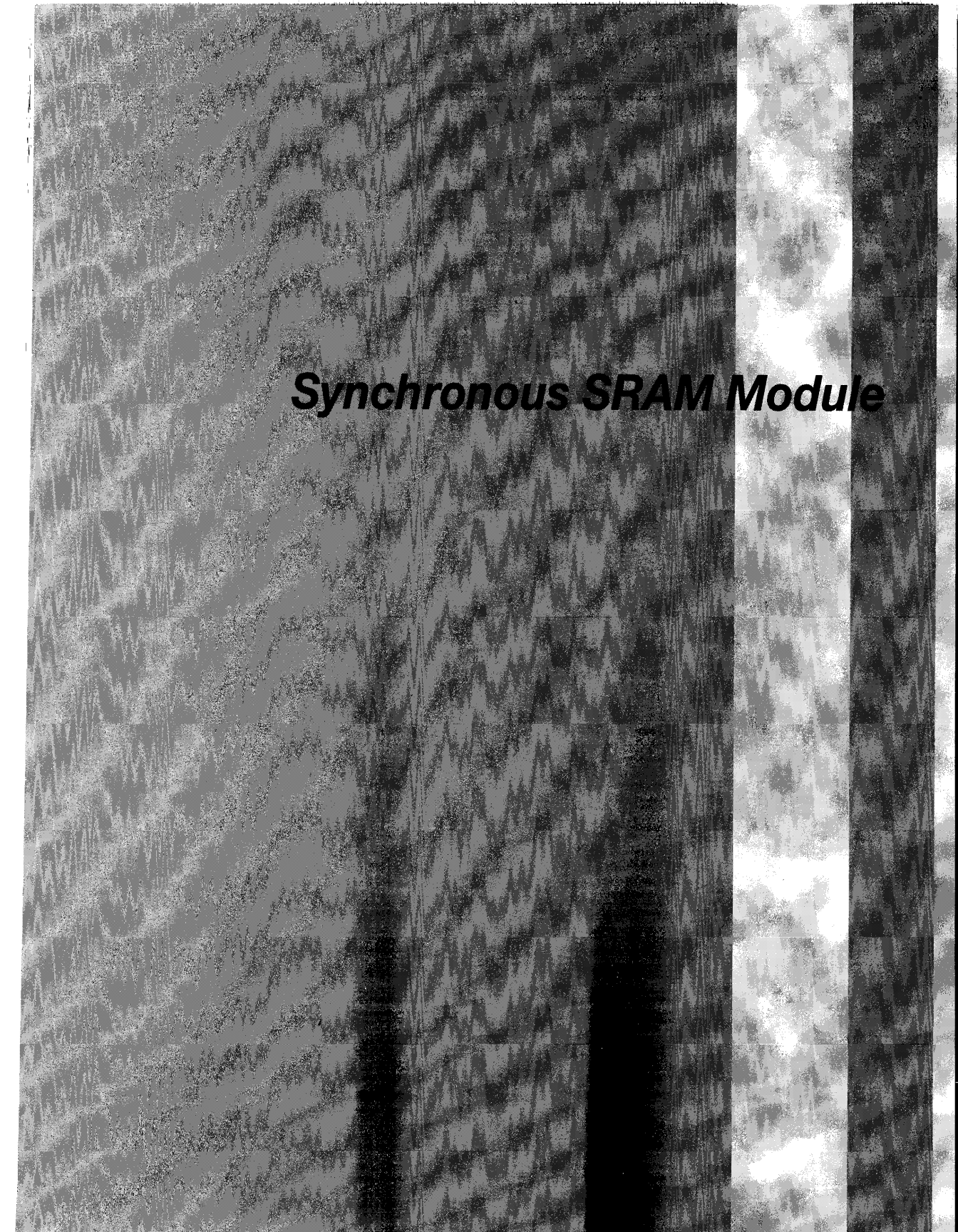
NOTE :

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.

119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Junction to Ambient(at still air)	Theta_JA	-	-	50	℃/W	
Junction to Ambient(at air flow of 100 LFPM)	Theta_JA	-	-	40	℃/W	
Junction to Case	Theta_JC	-	-	8	℃/W	
Junction to Solder Ball	Theta_JB	-	-	10	℃/W	

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D \times Theta\_JA$.


Synchronous SRAM Module

256KB Synchronous Pipelined Burst SRAM Module

FEATURES

- Implemented based on **COAST 3.1**
- Supports Interleave Burst and Linear Burst Mode
- Zero-wait-state operation at 75/66MHz
- TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- 160-pin DIMM with gold plated Tap
- PCB : Height (1130mil)
- Product Family : KMM764V41AG2-13/15

GENERAL DESCRIPTION

The KMM764V41AG2 is 256K byte high-frequency Synchronous Pipelined Burst Static Random Access Memory module organized as 32K words by 64 bits. The module is designed specially to function as the secondary cache in Pentium, K5, M1, and Power PC-based systems and using SAMSUNG's PCB design tool. The device for this module is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology.

PIN NAMES

Pin Name	Pin Function
CLK[1:0]	Clock Inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[7:0]	Tag RAM Data Inputs/Outputs
$\overline{TWE}$	Tag RAM Write Enable Input
$\overline{ECS}$[2:1]	Chip Select Inputs for Depth Expansion
$\overline{CCS}$	Chip Select Input
$\overline{CWE}$[7:0]	Write Enable Inputs
$\overline{COE}$	Output Enable Input
$\overline{ADSP}$	Address Status Processor
$\overline{CADS}$	Address Status Controller
$\overline{CADV}$	Burst Address Advance
$\overline{BWE}$	Byte Write Enable Input
$\overline{GWE}$	Grobal Write Enable Input
$\overline{LBO}$	Burst Mode Control
Vcc5	Power Supply(5V)
Vcc3	Power Supply(3.3V)
Vss	Ground
N.C	No Connection

PD PIN INFORMATION

PD Pin Allocation				Module Part No
PD3	PD2	PD1	PD0	
N.C	Vss	N.C	N.C	KMM764V41AG2

PIN CONFIGURATION *(Top View)*

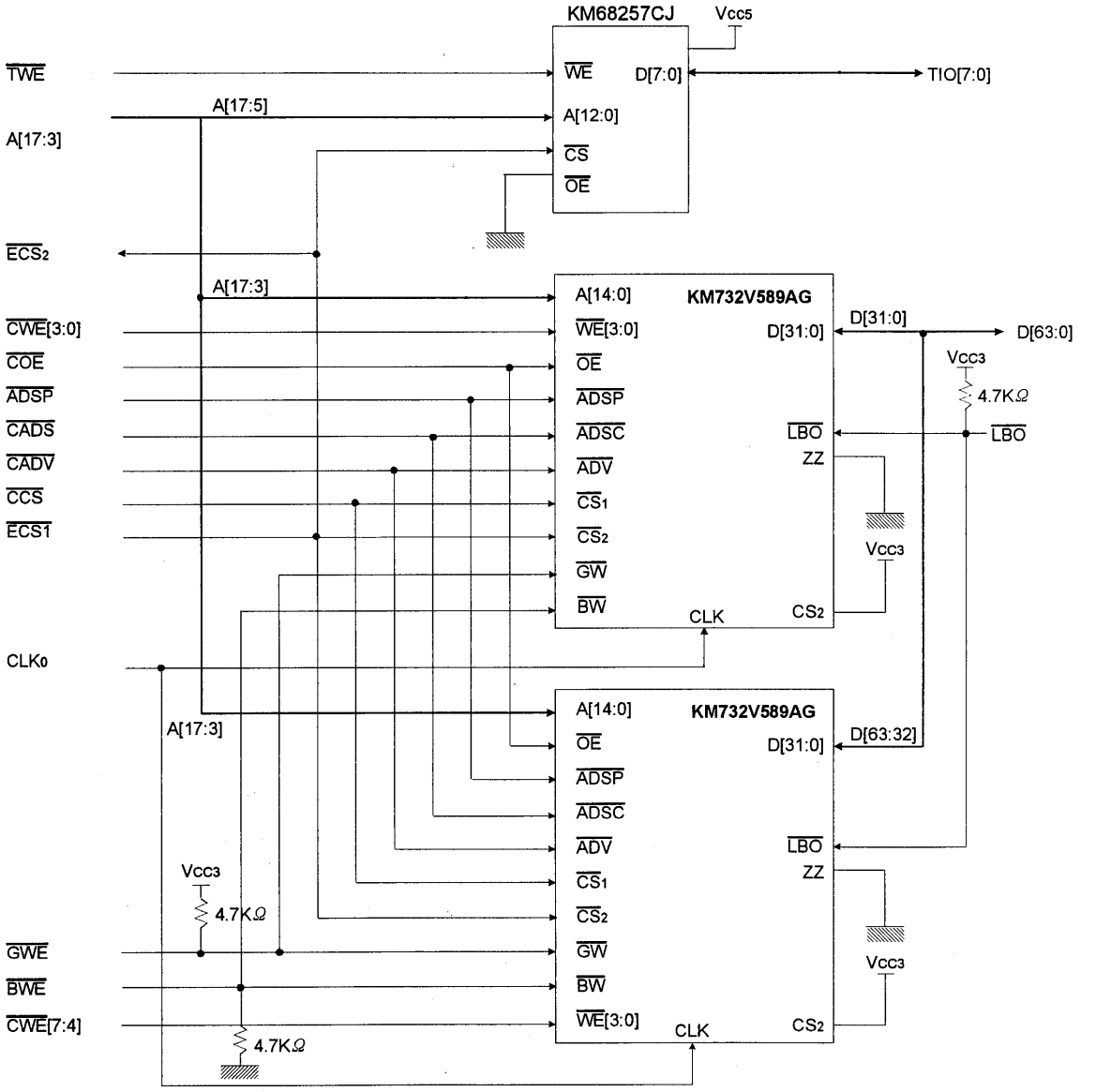
Vss	81	1	Vss	D57	122	42	D56
TIO1	82	2	TIO0				
TIO7	83	3	TIO2				
TIO5	84	4	TIO6	Vss	123	43	Vss
TIO3	85	5	TIO4	D55	124	44	D54
N.C	86	6	N.C	D53	125	45	D52
Vcc5	87	7	Vcc3	D51	126	46	D50
N.C	88	8	$\overline{TWE}$	D49	127	47	D48
$\overline{CADV}$	89	9	$\overline{CADS}$	Vss	128	48	Vss
Vss	90	10	Vss	D47	129	49	D46
$\overline{COE}$	91	11	$\overline{CWE}$4	D45	130	50	D44
$\overline{CWE}$5	92	12	$\overline{CWE}$6	D43	131	51	D42
$\overline{CWE}$7	93	13	$\overline{CWE}$0	Vcc5	132	52	Vcc3
$\overline{CWE}$1	94	14	$\overline{CWE}$2	D41	133	53	D40
Vcc5	95	15	Vcc3	D39	134	54	D38
$\overline{CWE}$3	96	16	$\overline{CCS}$	D37	135	55	D36
N.C	97	17	$\overline{GWE}$(3)	Vss	136	56	Vss
N.C	98	18	$\overline{BWE}$(3)	D35	137	57	D34
Vss	99	19	Vss	D33	138	58	D32
N.C	100	20	A3	D31	139	59	D30
A4	101	21	A7	Vcc5	140	60	Vcc3
A6	102	22	A5	D29	141	61	D28
A8	103	23	A11	D27	142	62	D26
A10	104	24	A16	D25	143	63	D24
Vcc5	105	25	Vcc3	Vss	144	64	Vss
A17	106	26	A18(1)	D23	145	65	D22
Vss	107	27	Vss	D21	146	66	D20
A9	108	28	A12	D19	147	67	D18
A14	109	29	A13	Vcc5	148	68	Vcc3
A15	110	30	$\overline{ADSP}$	D17	149	69	D16
N.C	111	31	$\overline{ECS}$1	D15	150	70	D14
PD0	112	32	$\overline{ECS}$2	D13	151	71	D12
PD2	113	33	PD1	Vss	152	72	Vss
$\overline{LBO}$(2)	114	34	PD3	D11	153	73	D10
Vss	115	35	Vss	D9	154	74	D8
CLK0	116	36	CLK1(1)	D7	155	75	D6
Vss	117	37	Vss	Vcc5	156	76	Vcc3
D63	118	38	D62	D5	157	77	D4
Vcc5	119	39	Vcc3	D3	158	78	D2
D61	120	30	D60	D1	159	79	D0
D59	121	41	D58	Vss	160	80	Vss

NOTE :

1. These pins are used for 512KB module only and they should be no connect for this module.
2. Default is no connect for Intel processor based designs becouse this pin pulled up with 4.7Kohm resistor on the module.
3. When these pins are no connect, all byte write should be controlled by all $\overline{CWEx}$ pins.

FUNCTIONAL BLOCK DIAGRAM

KMM764V41AG2



NOTE :

1. ZZ pin is internally connected to Vss and not pinout on the module.
2. $\overline{LBO}$ is pulled up with 4.7Kohm resistor.
3. $\overline{GWE}$ is pulled up with 4.7Kohm resistor and $\overline{BWE}$ is pulled down with 4.7Kohm resistor.

A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

$\overline{CCS}$	$\overline{ECS}$	$\overline{ADSP}$	$\overline{CADS}$	$\overline{CADV}$	$\overline{WRITE}$	K	Address Accessed	Operation
H	X*	X	L	X	X	↑	N/A	Not Selected
L	X	L	X	X	X	↑	N/A	Not Selected
L	H	L	X	X	X	↑	N/A	Not Selected
L	X	X	L	X	X	↑	N/A	Not Selected
L	H	X	L	X	X	↑	N/A	Not Selected
L	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	L	H	L	X	L	↑	External Address	Begin Burst Read Cycle
L	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	H	H	L	L	↑	Next Address	Continue Burst Read Cycle
H	X	X	H	L	L	↑	Next Address	Continue Burst Read Cycle
X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	H	H	H	L	↑	Current Address	Suspend Burst Read Cycle
H	X	X	H	H	L	↑	Current Address	Suspend Burst Read Cycle

NOTE :

1. X means "Don't Care"
2. $\overline{ECS}$ = $\overline{ECS1}$ and $\overline{ECS2}$
3. The rising edge of clock is symbolized by ↑
4. $\overline{WRITE}$=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table
   $\overline{WRITE}$=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table
5. Operation finally depends on status of asynchronous input pin ($\overline{COE}$)

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE(Data field)

$\overline{GWE}$	$\overline{BWE}$	$\overline{CWE[1:0]}$	$\overline{CWE[3:2]}$	$\overline{CWE[5:4]}$	$\overline{CWE[7:6]}$	Operation
H	H	X	X	X	X	Read
H	L	H	H	H	H	Read
H	L	L	H	H	H	Write Byte D[15:0]
H	L	H	L	H	H	Write Byte D[31:16]
H	L	H	H	L	L	Write Byte D[63:32]
H	L	L	L	L	L	Write All Bytes
L	X	X	X	X	X	Write All Bytes

NOTE :

1. X means "Don't Care"
2. All input in this table must meet setup and hold time around the rising edge of CLK(↑).

B-1. ASYNCHRONOUS TRUTH TABLE(Tag field)

$\overline{ECS}$	$\overline{TWE}$	Mode	I/O Pin	Supply Current
H	X*	Not Selest	HIGH-Z	I_{SB},I_{SB1}
L	H	Read	D_{OUT}	I_{CC}
L	L	Write	D_{IN}	I_{CC}

NOTE : X means "Don't Care"

C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	High	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	0	0	1	1	1	0
Third Address		1	0	1	1	0	0	0	1
Fouth Address		1	1	1	0	0	1	0	0

NOTE :

1. When this pin is no connects, $\overline{LBO}$ should be high.
2. Dafault is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	1	0	1	1	0	0
Third Address		1	0	1	1	0	0	0	1
Fouth Address		1	1	0	0	0	1	1	0

NOTE : $\overline{LBO}$ must be tied to low because this pin is pulled up with 4.7KΩ on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{CC3} Supply Relative to Vss	V_{CC3}	-0.3 to 4.6	V
Voltage on V_{CC5} Supply Relative to Vss	V_{CC5}	-0.3 to 6.0	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any outher conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (T_A =0 to 70℃)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC3}	3.13	3.3	3.6	V
	V_{CC5}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IL}*	-0.3	-	0.8	V
Input High Voltage	V_{IH}**	2.2	-	Vcc***+0.3	V

* V_{IL3}(min) = -1.4 (Pulse width ≤ 10ns), V_{IL5}(min) = -2.0 (Pulse Width ≤ 10ns)

** V_{IH3}(max) = 5.0V (Pulse Width ≤ 10ns) ; In case of I/O pins, the maximum V_{IH3}(max) = 4.1V (Pulse Width ≤ 10ns)
V_{IH5}(max) = 7.0V (Pulse Width ≤ 10ns)

*** V_{CC} =V_{CC3} or V_{CC5}

2

DC ELECTRICAL CHARACTERISTICS* (T_A =0 to 70℃,V_{CC3}=3.3V+10%/-5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage current	I_{LI}**	V_{CC3}=Max, V_{IN}=Vss to V_{CC3}		-5	5	μA
Output Leakage Current	I_{LO}	Output Disable, V_{OUT}=Vss to V_{CC3}		-5	5	μA
Operating Current	I_{CC}	f=Max, 100% Duty V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	75MHz	-	400	mA
			66MHz	-	360	
Standby Current	I_{SB}	f=Max, 100% Duty, Device deselected, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		-	80	mA
	I_{SB1}	f=0MHz, Device deselected, V_{IN} ≥ V_{CC3} -0.2V or V_{IL}, V_{IN} ≤ 0.2V, I_{OUT}=0mA		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

* Excludes Tag field.

** ILI for $\overline{LBO}$, $\overline{GWE}$, TIO(8,9,10) and $\overline{BWE}$ is ± 1mA(Max.)

CAPACITANCE*(f=1MHz,T_A=25℃)

Item	Symbol	Test Condition	Min.	Max.	Unit
Address, $\overline{ECS}$ Input Capacitance	C_{IN1}	V_{IN}=0V	-	35	pF
$\overline{TWE}$, $\overline{CWE}$, CLK Input Capacitance	C_{IN2}	V_{IN}=0V	-	20	pF
$\overline{COE}$, $\overline{ADSP}$, $\overline{CADS}$, $\overline{CADV}$, $\overline{CCS}$ $\overline{GWE}$, $\overline{BWE}$ Input Capacitance	C_{IN3}	V_{IN}=0V	-	20	pF
Data and Tag Input/Output Capacitance	$C_{I/O1}$	$V_{I/O}$=0V	-	15	pF

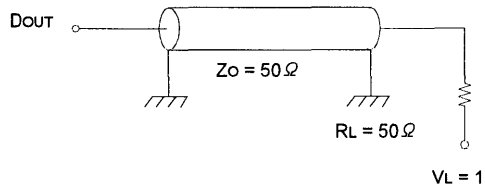
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

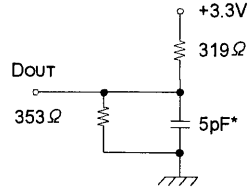
TEST CONDITIONS ON DATA RAM (T_A =0 to 70℃, V_{CC3}=3.3V+10%/-5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tLZC, tLZOE, tHZOE & tHZC)



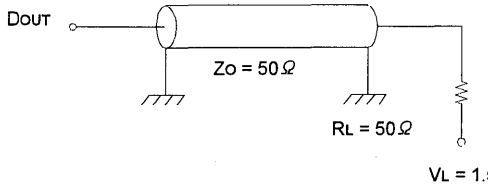
* Including Scope and Jig Capacitance

Fig. 1

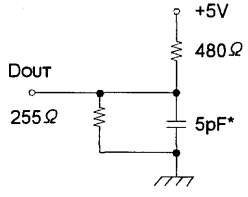
TEST CONDITIONS ON TAG RAM (T_A =0 to 70℃, V_{CC5}=5.0V±5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ & tOW)



* Including Scope and Jig Capacitance

Fig. 2

SAMSUNG ELECTRONICS

AC TIMING CHARACTERISTICS ON DATA RAM (T_A =0 to 70℃, V_{CC3}=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V41AG2-13		KMM764V41AG2-15		Unit
		Min	Max	Min	Max	
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	7	ns
Output Enable to Data Valid	tOE	-	6	-	6	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4	-	4	ns
Clock High to Output High-Z	tHZC	1.5	5	2.0	6	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE :

1. All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever $\overline{CADS}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{CADS}$ or $\overline{ADSP}$ is sampled low in order to the this device remained at enable.
3. $\overline{CADS}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clocks after leaving ZZ state.

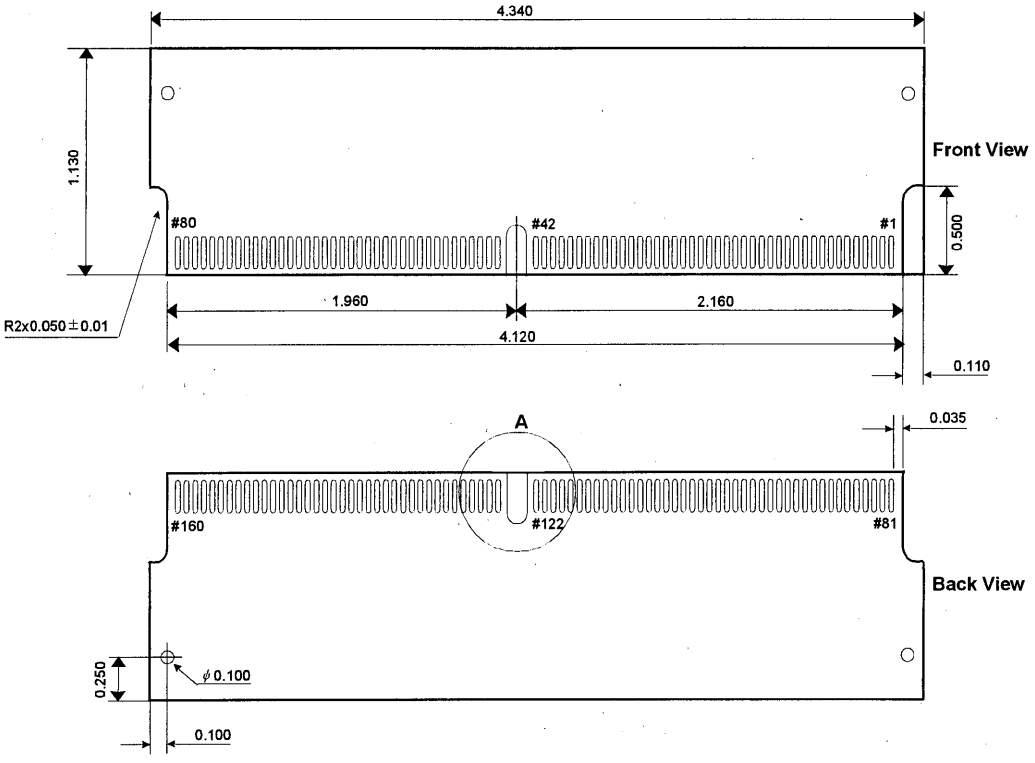
AC TIMING CHARACTERISTICS ON TAG RAM (T_A =0 to 70℃, V_{CC5}=5.0V±5%)

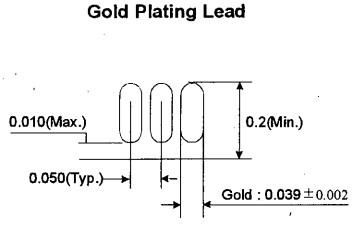
Refers to the individual components, not the whole module

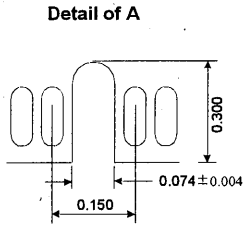
Parameter	Symbol	KMM764V41AG2-13		KMM764V41AG2-15		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	ns
Address Access Time	tAA	-	12	-	15	ns
Chip Select to Output	tCO	-	12	-	15	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Write cycle Time	tWC	12	-	15	-	ns
Chip Select to End of Write	tCW	9	-	11	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	ns
Write Pulse Width	tWP	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

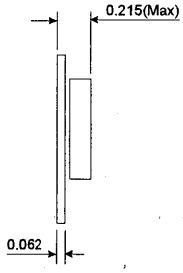
PACKAGE DIMENSIONS

Units : Inches









Tolerances : ±0.005 unless otherwise specified

SAMSUNG ELECTRONICS

256KB Synchronous Pipelined Burst SRAM Module

FEATURES

- Implemented based on **COAST 3.1**
- Supports Interleave Burst and Linear Burst Mode
- Zero-wait-state operation at 75/66MHz
- TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- 160-pin DIMM with gold plated Tap
- Series 22 ohm resistors for niose immunity
- Product Family : KMM764V41AG7-13/15

GENERAL DESCRIPTION

The KMM764V41AG7 is 256K byte high-frequency Synchronous Pipelined Burst Static Random Access Memory module organized as 32K words by 64 bits. The module is designed specially to function as the secondary cache in Pentium and Power PC-based systems. The device for this module is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. The module uses two of SAMSUNG's KM732V589AG and one KM68257C for 8bits tag ROM

PIN NAMES

Pin Name	Pin Function
CLK[1:0]	Clock Inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[7:0]	Tag RAM Data Inputs/Outputs
$\overline{TWE}$	Tag RAM Write Enable Input
$\overline{ECS}$[2:1]	Chip Select Inputs for Depth Expansion
$\overline{CCS}$	Chip Select Input
$\overline{CWE}$[7:0]	Write Enable Inputs
$\overline{COE}$	Output Enable Input
$\overline{ADSP}$	Address Status Processor
$\overline{CADS}$	Address Status Controller
$\overline{CADV}$	Burst Address Advance
$\overline{BWE}$	Byte Write Enable Input
$\overline{GWE}$	Grobal Write Enable Input
$\overline{LBO}$	Burst Mode Control
V_{CC5}	Power Supply(5V)
V_{CC3}	Power Supply(3.3V)
Vss	Ground
N.C	No Connection

PD PIN INFORMATION

PD Pin Allocation				Module Part No
PD_3	PD_2	PD_1	PD_0	
N.C	Vss	N.C	N.C	KMM764V41AG7

PIN CONFIGURATION *(Top View)*

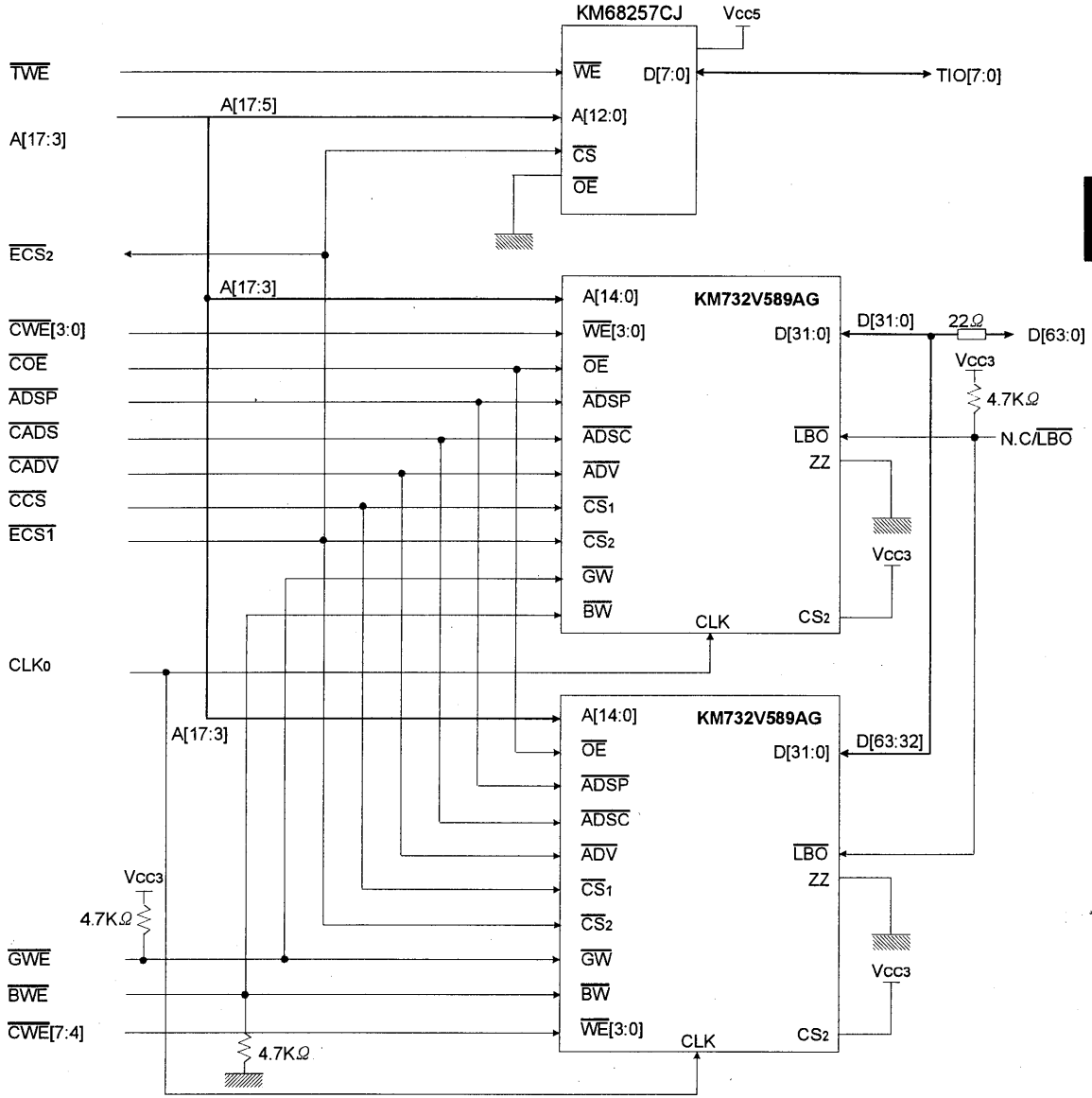
V_{SS}	81	1	V_{SS}	D_{57}	122	42	D_{58}
TIO_1	82	2	TIO_0				
TIO_7	83	3	TIO_2				
TIO_6	84	4	TIO_8	V_{SS}	123	43	V_{SS}
TIO_3	85	5	TIO_4	D_{55}	124	44	D_{54}
N.C	86	6	N.C	D_{53}	125	45	D_{52}
V_{CC5}	87	7	V_{CC3}	D_{51}	126	46	D_{50}
N.C	88	8	$\overline{TWE}$	D_{49}	127	47	D_{48}
$\overline{CADV}$	89	9	$\overline{CADS}$	V_{SS}	128	48	V_{SS}
V_{SS}	90	10	V_{SS}	D_{47}	129	49	D_{46}
$\overline{COE}$	91	11	$\overline{CWE_4}$	D_{45}	130	50	D_{44}
$\overline{CWE_5}$	92	12	$\overline{CWE_6}$	D_{43}	131	51	D_{42}
$\overline{CWE_7}$	93	13	$\overline{CWE_0}$	V_{CC5}	132	52	V_{CC3}
$\overline{CWE_1}$	94	14	$\overline{CWE_2}$	D_{41}	133	53	D_{40}
V_{CC5}	95	15	V_{CC3}	D_{39}	134	54	D_{38}
$\overline{CWE_3}$	96	16	$\overline{CCS}$	D_{37}	135	55	D_{36}
N.C	97	17	$\overline{GWE}$(3)	V_{SS}	136	56	V_{SS}
N.C	98	18	$\overline{BWE}$(3)	D_{35}	137	57	D_{34}
V_{SS}	99	19	V_{SS}	D_{33}	138	58	D_{32}
N.C	100	20	A_3	D_{31}	139	59	D_{30}
A_4	101	21	A_7	V_{CC5}	140	60	V_{CC3}
A_6	102	22	A_5	D_{29}	141	61	D_{28}
A_8	103	23	A_{11}	D_{27}	142	62	D_{26}
A_{10}	104	24	A_{16}	D_{25}	143	63	D_{24}
V_{CC5}	105	25	V_{CC3}	V_{SS}	144	64	V_{SS}
A_{17}	106	26	A_{18}(1)	D_{23}	145	65	D_{22}
V_{SS}	107	27	V_{SS}	D_{21}	146	66	D_{20}
A_9	108	28	A_{12}	D_{19}	147	67	D_{18}
A_{14}	109	29	A_{13}	V_{CC5}	148	68	V_{CC3}
A_{15}	110	30	$\overline{ADSP}$	D_{17}	149	69	D_{16}
N.C	111	31	$\overline{ECS_1}$	D_{15}	150	70	D_{14}
PD_0	112	32	$\overline{ECS_2}$	D_{13}	151	71	D_{12}
PD_2	113	33	PD_1	V_{SS}	152	72	V_{SS}
$\overline{LBO}$(2)	114	34	PD_3	D_{11}	153	73	D_{10}
V_{SS}	115	35	V_{SS}	D_9	154	74	D_8
CLK_0	116	36	CLK_1(1)	D_7	155	75	D_6
V_{SS}	117	37	V_{SS}	V_{CC5}	156	76	V_{CC3}
D_{63}	118	38	D_{62}	D_5	157	77	D_4
V_{CC5}	119	39	V_{CC3}	D_3	158	78	D_2
D_{61}	120	30	D_{60}	D_1	159	79	D_0
D_{59}	121	41	D_{58}	V_{SS}	160	80	V_{SS}

NOTE :

1. These pins are used for 512KB module only and they should be no connect for this module.
2. Default is no connect for Intel processor based designs becouse this pin pulled up with 4.7Kohm resistor on the module.
3. When these pins are no connect, all byte write should be controlled by all $\overline{CWEx}$ pins.

FUNCTIONAL BLOCK DIAGRAM

KMM764V41AG7



NOTE :

1. ZZ pin is internally connected to Vss and not pinout on the module.
2. $\overline{LBO}$ is pulled up with 4.7Kohm resistor.
3. $\overline{GWE}$ is pulled up with 4.7Kohm resistor and $\overline{BWE}$ is pulled down with 4.7Kohm resistor.

A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

$\overline{CCS}$	$\overline{ECS}$	$\overline{ADSP}$	$\overline{CADS}$	$\overline{CADV}$	$\overline{WRITE}$	K	Address Accessed	Operation
H	X*	X	L	X	X	↑	N/A	Not Selected
L	X	L	X	X	X	↑	N/A	Not Selected
L	H	L	X	X	X	↑	N/A	Not Selected
L	X	X	L	X	X	↑	N/A	Not Selected
L	H	X	L	X	X	↑	N/A	Not Selected
L	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	L	H	L	X	L	↑	External Address	Begin Burst Read Cycle
L	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	H	H	L	L	↑	Next Address	Continue Burst Read Cycle
H	X	X	H	L	L	↑	Next Address	Continue Burst Read Cycle
X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	H	H	H	L	↑	Current Address	Suspend Burst Read Cycle
H	X	X	H	H	L	↑	Current Address	Suspend Burst Read Cycle

NOTE :

1. X means "Don't Care"
2. $\overline{ECS}$ = $\overline{ECS}$1 and $\overline{ECS}$2
3. The rising edge of clock is symbolized by ↑
4. $\overline{WRITE}$=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table
   $\overline{WRITE}$=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table
5. Operation finally depends on status of asynchronous input pin ($\overline{COE}$)

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE(Data field)

$\overline{GWE}$	$\overline{BWE}$	$\overline{CWE}$[1:0]	$\overline{CWE}$[3:2]	$\overline{CWE}$[5:4]	$\overline{CWE}$[7:6]	Operation
H	H	X	X	X	X	Read
H	L	H	H	H	H	Read
H	L	L	H	H	H	Write Byte D[15:0]
H	L	H	L	H	H	Write Byte D[31:16]
H	L	H	H	L	L	Write Byte D[63:32]
H	L	L	L	L	L	Write All Bytes
L	X	X	X	X	X	Write All Bytes

NOTE :

1. X means "Don't Care"
2. All input in this table must meet setup and hold time around the rising edge of CLK(↑).

B-1. ASYNCHRONOUS TRUTH TABLE(Tag field)

$\overline{ECS}$	$\overline{TWE}$	Mode	I/O Pin	Supply Current
H	X*	Not Selest	HIGH-Z	I_{SB},I_{SB1}
L	H	Read	D_{OUT}	I_{CC}
L	L	Write	D_{IN}	I_{CC}

NOTE : X means "Don't Care"

C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	High	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	0	0	1	1	1	0
Third Address		1	0	1	1	0	0	0	1
Fouth Address		1	1	1	0	0	1	0	0

NOTE :

1. When this pin is no connects, $\overline{LBO}$ should be high.
2. Dafault is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	1	0	1	1	0	0
Third Address		1	0	1	1	0	0	0	1
Fouth Address		1	1	0	0	0	1	1	0

NOTE : $\overline{LBO}$ must be tied to low because this pin is pulled up with 4.7KΩ on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{CC3} Supply Relative to Vss	V_{CC3}	-0.3 to 4.6	V
Voltage on V_{CC5} Supply Relative to Vss	V_{CC5}	-0.3 to 6.0	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any outher conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (T_A =0 to 70℃)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC3}	3.13	3.3	3.6	V
	V_{CC5}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IL}*	-0.3	-	0.8	V
Input High Voltage	V_{IH}**	2.2	-	V_{CC}***+0.3	V

* V_{IL3}(min) = -1.4 (Pulse width ≤ 10ns), V_{IL5}(min) = -2.0 (Pulse Width ≤ 10ns)

** V_{IH3}(max) = 5.0V (Pulse Width ≤ 10ns) ; In case of I/O pins, the maximum V_{IH3}(max) = 4.1V (Pulse Width ≤ 10ns)
V_{IH5}(max) = 7.0V (Pulse Width ≤ 10ns)

*** V_{CC} =V_{CC3} or V_{CC5}

DC ELECTRICAL CHARACTERISTICS* (T_A =0 to 70℃,V_{CC3}=3.3V+10%/-5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage current	I_{LI}**	V_{CC3}=Max, V_{IN}=Vss to V_{CC3}		-5	5	μA
Output Leakage Current	I_{LO}	Output Disable, V_{OUT}=Vss to V_{CC3}		-5	5	μA
Operating Current	I_{CC}	f=Max, 100% Duty V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	75MHz	-	400	mA
			66MHz	-	360	
Standby Current	I_{SB}	f=Max, 100% Duty, Device deselected, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		-	80	mA
	I_{SB1}	f=0MHz, Device deselected, V_{IN}≥V_{CC3} -0.2V or V_{IL}, V_{IN} ≤ 0.2V, I_{OUT}=0mA		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

* Excludes Tag field.

** ILI for $\overline{LBO}$, $\overline{GWE}$ and $\overline{BWE}$ is ±1mA(Max.)

CAPACITANCE*(f=1MHz,T_A=25℃)

Item	Symbol	Test Condition	Min.	Max.	Unit
Address, $\overline{ECS}$ Input Capacitance	C_{IN1}	V_{IN}=0V	-	35	pF
$\overline{TWE}$, $\overline{CWE}$, CLK Input Capacitance	C_{IN2}	V_{IN}=0V	-	20	pF
$\overline{COE}$, $\overline{ADSP}$, $\overline{CADS}$, $\overline{CADV}$, $\overline{CCS}$ $\overline{GWE}$, $\overline{BWE}$ Input Capacitance	C_{IN3}	V_{IN}=0V	-	20	pF
Data and Tag Input/Output Capacitance	$C_{I/O1}$	$V_{I/O}$=0V	-	15	pF

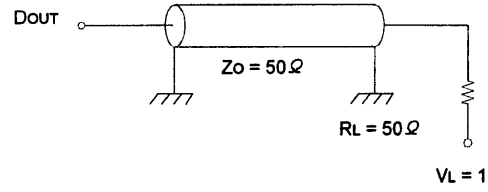
* NOTE : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

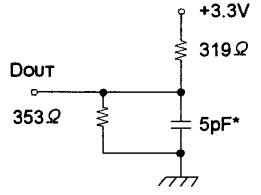
TEST CONDITIONS ON DATA RAM (T_A =0 to 70℃, V_{CC3}=3.3V+10%/-5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tLZC, tLZOE, tHZOE & tHZC)



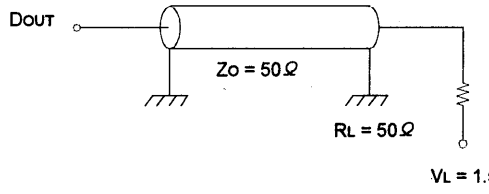
* Including Scope and Jig Capacitance

Fig. 1

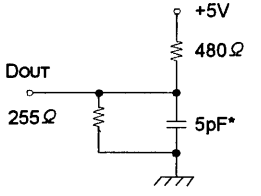
TEST CONDITIONS ON TAG RAM (T_A =0 to 70℃, V_{CC5}=5.0V±5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ & tOW)



* Including Scope and Jig Capacitance

Fig. 2

AC TIMING CHARACTERISTICS ON DATA RAM (T_A =0 to 70℃, V_{CC3}=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V41AG7-13		KMM764V41AG7-15		Unit
		Min	Max	Min	Max	
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	7	ns
Output Enable to Data Valid	tOE	-	6	-	6	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4	-	4	ns
Clock High to Output High-Z	tHZC	1.5	5	2.0	6	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE :

1. All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever $\overline{CADS}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{CADS}$ or $\overline{ADSP}$ is sampled low in order to the this device remained at enable.
3. $\overline{CADS}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clocks after leaving ZZ state.

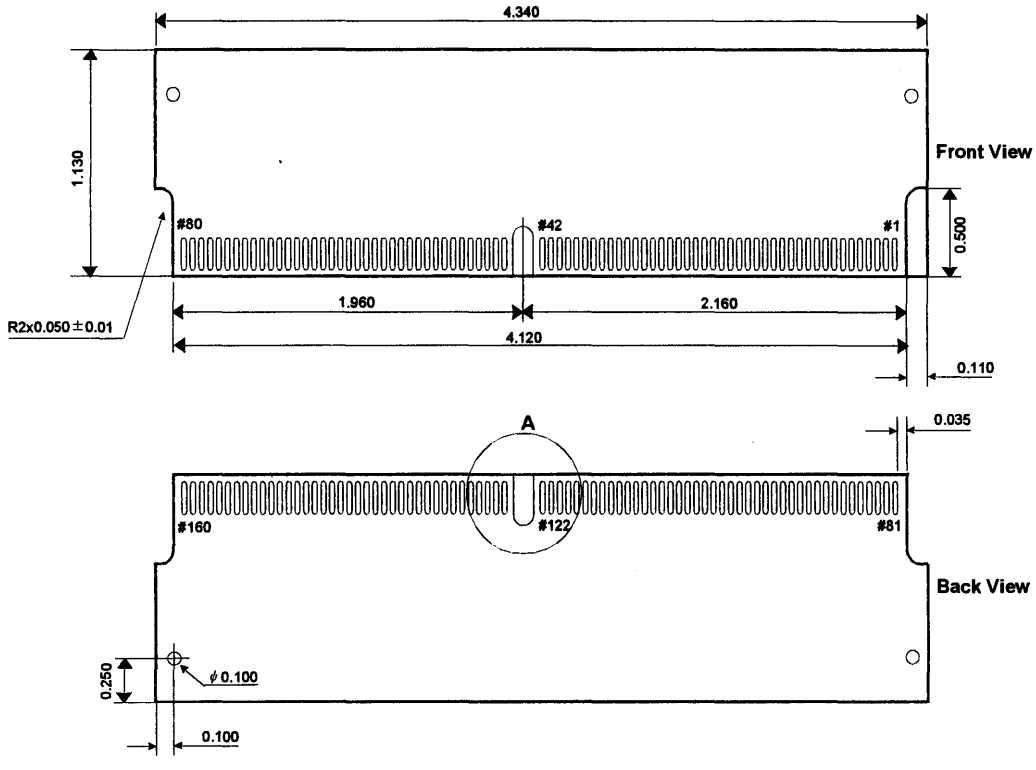
AC TIMING CHARACTERISTICS ON TAG RAM (T_A =0 to 70℃, V_{CC5}=5.0V±5%)

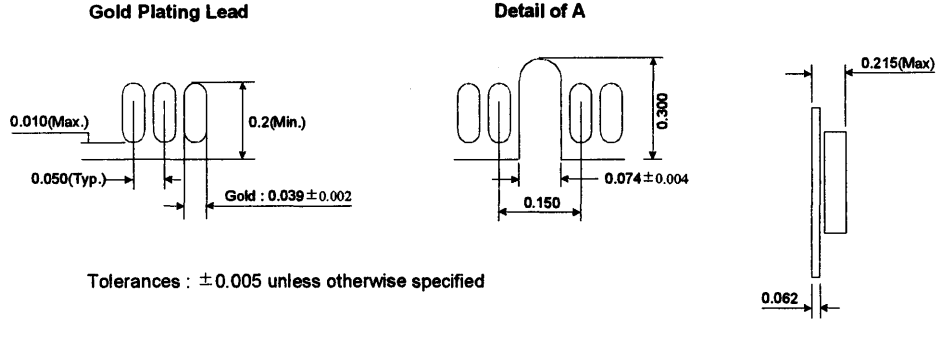
Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V41AG7-13		KMM764V41AG7-15		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	ns
Address Access Time	tAA	-	12	-	15	ns
Chip Select to Output	tCO	-	12	-	15	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Write cycle Time	tWC	12	-	15	-	ns
Chip Select to End of Write	tCW	9	-	11	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	ns
Write Pulse Width	tWP	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

PACKAGE DIMENSIONS

Units : Inches





Tolerances : ±0.005 unless otherwise specified

256KB Synchronous Pipelined Burst SRAM Module

FEATURES

- Implemented based on **COAST 3.1**
- Supports Interleave Burst and Linear Burst Mode
- Zero-wait-state operation at 75/66MHz
- TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- 160-pin DIMM with gold plated Tap
- Series 22 ohm resistors for niose immunity
- Product Family : KMM764V45AG-13/15

GENERAL DESCRIPTION

The KMM764V45AG7 is 256K byte high-frequency Synchronous Pipelined Burst Static Random Access Memory module organized as 32K words by 64 bits. The module is designed specially to function as the secondary cache in Pentium and Power PC-based systems. The component on this module is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. The module uses two of SAMSUNG's KM732V589AG and one KM68257C for 11bits tag RAM.

PIN NAMES

Pin Name	Pin Function
CLK[1:0]	Clock Inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[7:0]	Tag RAM Data Inputs/Outputs
$\overline{TWE}$	Tag RAM Write Enable Input
$\overline{ECS}$[2:1]	Chip Select Inputs for Depth Expansion
$\overline{CCS}$	Chip Select Input
$\overline{CWE}$[7:0]	Write Enable Inputs
$\overline{COE}$	Output Enable Input
$\overline{ADSP}$	Address Status Processor
$\overline{CADS}$	Address Status Controller
$\overline{CADV}$	Burst Address Advance
$\overline{BWE}$	Byte Write Enable Input
$\overline{GWE}$	Grobal Write Enable Input
$\overline{LBO}$	Burst Mode Control
V_{CC5}	Power Supply(5V)
V_{CC3}	Power Supply(3.3V)
Vss	Ground
N.C	No Connection

PD PIN INFORMATION

PD Pin Allocation				Module Part No
PD_3	PD_2	PD_1	PD_0	
N.C	Vss	N.C	N.C	KMM764V45AG

PIN CONFIGURATION *(Top View)*

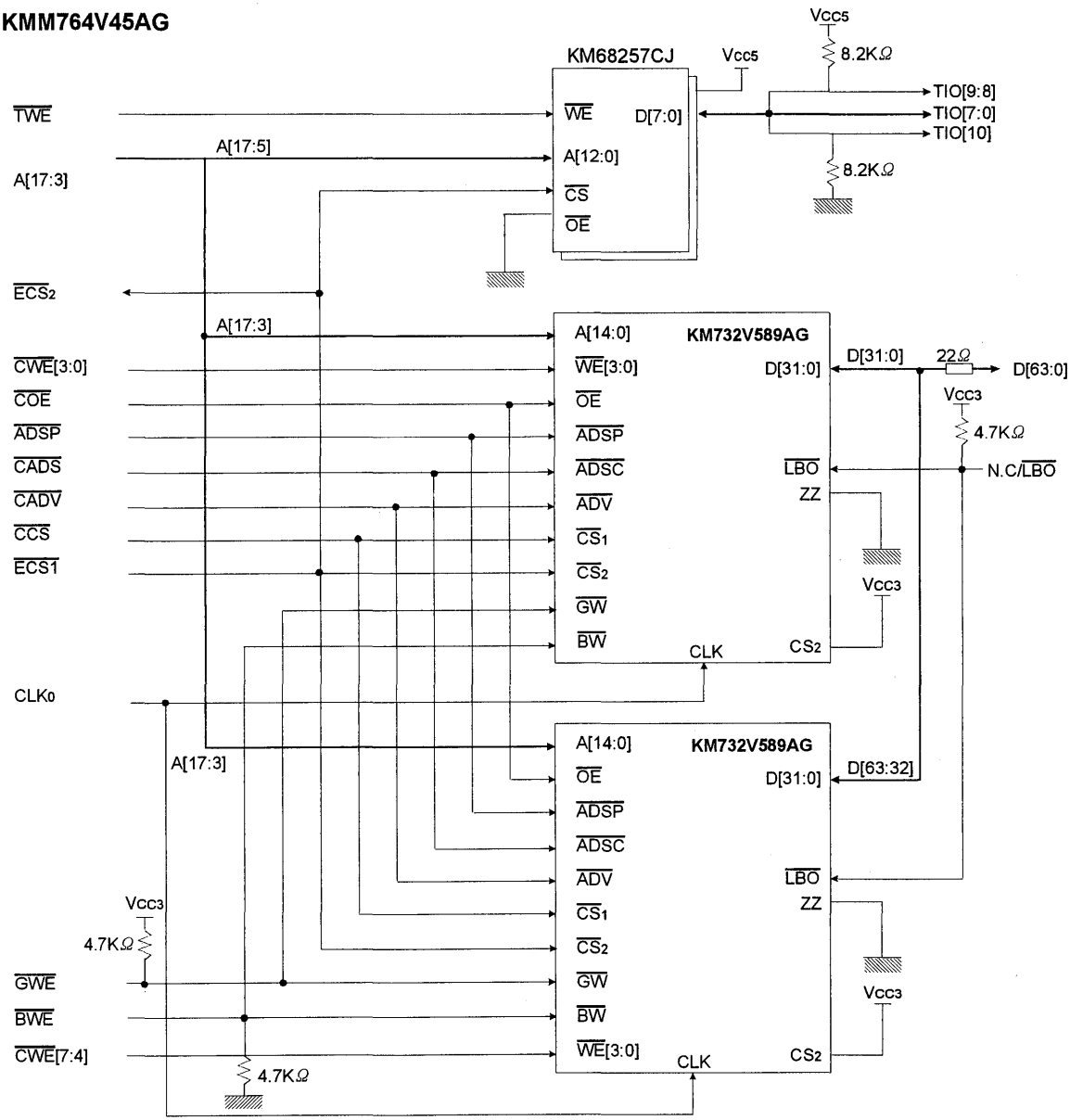
Vss	81	1	Vss	D_{57}	122	42	D_{56}
TIO_1	82	2	TIO_0				
TIO_7	83	3	TIO_2				
TIO_5	84	4	TIO_6	Vss	123	43	Vss
TIO_3	85	5	TIO_4	D_{55}	124	44	D_{54}
TIO_8	86	6	TIO_8	D_{53}	125	45	D_{52}
V_{CC5}	87	7	V_{CC3}	D_{51}	126	46	D_{50}
TIO_{10}	88	8	$\overline{TWE}$	D_{49}	127	47	D_{48}
$\overline{CADV}$	89	9	$\overline{CADS}$	Vss	128	48	Vss
Vss	90	10	Vss	D_{47}	129	49	D_{46}
$\overline{COE}$	91	11	$\overline{CWE_4}$	D_{45}	130	50	D_{44}
$\overline{CWE_5}$	92	12	$\overline{CWE_6}$	D_{43}	131	51	D_{42}
$\overline{CWE_7}$	93	13	$\overline{CWE_0}$	V_{CC5}	132	52	V_{CC3}
$\overline{CWE_1}$	94	14	$\overline{CWE_2}$	D_{41}	133	53	D_{40}
V_{CC5}	95	15	V_{CC3}	D_{39}	134	54	D_{38}
$\overline{CWE_3}$	96	16	$\overline{CCS}$	D_{37}	135	55	D_{36}
N.C	97	17	$\overline{GWE}$(3)	Vss	136	56	Vss
N.C	98	18	$\overline{BWE}$(3)	D_{35}	137	57	D_{34}
Vss	99	19	Vss	D_{33}	138	58	D_{32}
N.C	100	20	A_3	D_{31}	139	59	D_{30}
A_4	101	21	A_7	V_{CC5}	140	60	V_{CC3}
A_6	102	22	A_5	D_{29}	141	61	D_{28}
A_8	103	23	A_{11}	D_{27}	142	62	D_{26}
A_{10}	104	24	A_{16}	D_{25}	143	63	D_{24}
V_{CC5}	105	25	V_{CC3}	Vss	144	64	Vss
A_{17}	106	26	A_{18}(1)	D_{23}	145	65	D_{22}
Vss	107	27	Vss	D_{21}	146	66	D_{20}
A_9	108	28	A_{12}	D_{19}	147	67	D_{18}
A_{14}	109	29	A_{13}	V_{CC5}	148	68	V_{CC3}
A_{15}	110	30	$\overline{ADSP}$	D_{17}	149	69	D_{16}
N.C	111	31	$\overline{ECS_1}$	D_{15}	150	70	D_{14}
PD_0	112	32	$\overline{ECS_2}$	D_{13}	151	71	D_{12}
PD_2	113	33	PD_1	Vss	152	72	Vss
$\overline{LBO}$(2)	114	34	PD_3	D_{11}	153	73	D_{10}
Vss	115	35	Vss	D_9	154	74	D_8
CLK_0	116	36	CLK_1(1)	D_7	155	75	D_6
Vss	117	37	Vss	V_{CC5}	156	76	V_{CC3}
D_{63}	118	38	D_{62}	D_5	157	77	D_4
V_{CC5}	119	39	V_{CC3}	D_3	158	78	D_2
D_{61}	120	30	D_{60}	D_1	159	79	D_0
D_{59}	121	41	D_{58}	Vss	160	80	Vss

NOTE :

1. These pins are used for 256KB module only and they should be no connect for this module.
2. Default is no connect for Intel processor based designs becouse this pin pulled up with 4.7Kohm resistor on the module.
3. When these pins are no connect, all byte write should be controlled by all $\overline{CWEx}$ pins.

FUNCTIONAL BLOCK DIAGRAM

KMM764V45AG



NOTE :

1. ZZ pin is internally connected to Vss and not pinout on the module.
2. $\overline{LBO}$ is pulled up with 4.7Kohm resistor.
3. $\overline{GWE}$ is pulled up with 4.7Kohm resistor and $\overline{BWE}$ is pulled down with 4.7Kohm resistor.

A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

$\overline{CCS}$	$\overline{ECS}$	$\overline{ADSP}$	$\overline{CADS}$	$\overline{CADV}$	$\overline{WRITE}$	K	Address Accessed	Operation
H	X*	X	L	X	X	↑	N/A	Not Selected
L	X	L	X	X	X	↑	N/A	Not Selected
L	H	L	X	X	X	↑	N/A	Not Selected
L	X	X	L	X	X	↑	N/A	Not Selected
L	H	X	L	X	X	↑	N/A	Not Selected
L	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	L	H	L	X	L	↑	External Address	Begin Burst Read Cycle
L	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	H	H	L	L	↑	Next Address	Continue Burst Read Cycle
H	X	X	H	L	L	↑	Next Address	Continue Burst Read Cycle
X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	H	H	H	L	↑	Current Address	Suspend Burst Read Cycle
H	X	X	H	H	L	↑	Current Address	Suspend Burst Read Cycle

NOTE :

1. X means "Don't Care"
2. $\overline{ECS}$ = $\overline{ECS}$1 and $\overline{ECS}$2
3. The rising edge of clock is symbolized by ↑
4. $\overline{WRITE}$=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table
   $\overline{WRITE}$=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table
5. Operation finally depends on status of asynchronous input pin ($\overline{COE}$)

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE(Data field)

$\overline{GWE}$	$\overline{BWE}$	$\overline{CWE}$[1:0]	$\overline{CWE}$[3:2]	$\overline{CWE}$[5:4]	$\overline{CWE}$[7:6]	Operation
H	H	X	X	X	X	Read
H	L	H	H	H	H	Read
H	L	L	H	H	H	Write Byte D[15:0]
H	L	H	L	H	H	Write Byte D[31:16]
H	L	H	H	L	L	Write Byte D[63:32]
H	L	L	L	L	L	Write All Bytes
L	X	X	X	X	X	Write All Bytes

NOTE :

1. X means "Don't Care"
2. All input in this table must meet setup and hold time around the rising edge of CLK(↑).

B-1. ASYNCHRONOUS TRUTH TABLE(Tag field)

$\overline{ECS}$	$\overline{TWE}$	Mode	I/O Pin	Supply Current
H	X*	Not Selest	HIGH-Z	I_{SB}, I_{SB1}
L	H	Read	D_{OUT}	I_{CC}
L	L	Write	D_{IN}	I_{CC}

NOTE : X means "Don't Care"

C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	High	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	0	0	1	1	1	0
Third Address		1	0	1	1	0	0	0	1
Fouth Address		1	1	1	0	0	1	0	0

NOTE :
1. When this pin is no connects, $\overline{LBO}$ should be high.
2. Dafault is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	1	0	1	1	0	0
Third Address		1	0	1	1	0	0	0	1
Fouth Address		1	1	0	0	0	1	1	0

NOTE : $\overline{LBO}$ must be tied to low because this pin is pulled up with 4.7KΩ on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{CC3} Supply Relative to Vss	V_{CC3}	-0.3 to 4.6	V
Voltage on V_{CC5} Supply Relative to Vss	V_{CC5}	-0.3 to 6.0	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any outher conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (T_A =0 to 70℃)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC3}	3.13	3.3	3.6	V
	V_{CC5}	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V
Input Low Voltage	V_{IL}*	-0.3	-	0.8	V
Input High Voltage	V_{IH}**	2.2	-	Vcc***+0.3	V

* V_{IL3}(min) = -1.4 (Pulse width ≤ 10ns), V_{IL5}(min) = -2.0 (Pulse Width ≤ 10ns)

** V_{IH3}(max) = 5.0V (Pulse Width ≤ 10ns) ; In case of I/O pins, the maximum V_{IH3}(max) = 4.1V (Pulse Width ≤ 10ns)
V_{IH5}(max) = 7.0V (Pulse Width ≤ 10ns)

*** V_{CC} =V_{CC3} or V_{CC5}

2

DC ELECTRICAL CHARACTERISTICS*(T_A =0 to 70℃,V_{CC3}=3.3V+10%/-5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage current	I_{LI}**	V_{CC3}=Max, V_{IN}=Vss to V_{CC3}		-5	5	μA
Output Leakage Current	I_{LO}	Output Disable, V_{OUT}=Vss to V_{CC3}		-5	5	μA
Operating Current	I_{CC}	f=Max, 100% Duty V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	75MHz	-	400	mA
			66MHz	-	360	
Standby Current	I_{SB}	f=Max, 100% Duty, Device deselected, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		-	80	mA
	I_{SB1}	f=0MHz, Device deselected, V_{IN}≥V_{CC3} -0.2V or V_{IL}, V_{IN} ≤ 0.2V, I_{OUT}=0mA		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

* Excludes Tag field.

** ILI for $\overline{LBO}$, $\overline{GWE}$ and $\overline{BWE}$ is ±1mA(Max.)

CAPACITANCE*(f=1MHz,T_A=25℃)

Item	Symbol	Test Condition	Min.	Max.	Unit
Address, $\overline{ECS}$ Input Capacitance	C_{IN1}	V_{IN}=0V	-	35	pF
$\overline{TWE}$, $\overline{CWE}$, CLK Input Capacitance	C_{IN2}	V_{IN}=0V	-	20	pF
$\overline{COE}$, $\overline{ADSP}$, $\overline{CADS}$, $\overline{CADV}$, $\overline{CCS}$ $\overline{GWE}$, $\overline{BWE}$ Input Capacitance	C_{IN3}	V_{IN}=0V	-	20	pF
Data and Tag Input/Output Capacitance	$C_{I/O1}$	$V_{I/O}$=0V	-	15	pF

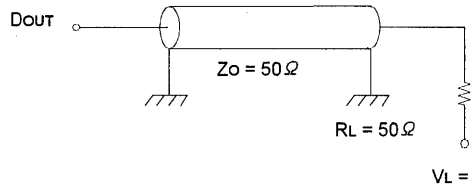
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

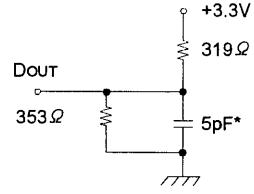
TEST CONDITIONS ON DATA RAM (T_A =0 to 70℃, V_{CC3}=3.3V+10%/-5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tLZC, tLZOE, tHZOE & tHZC)



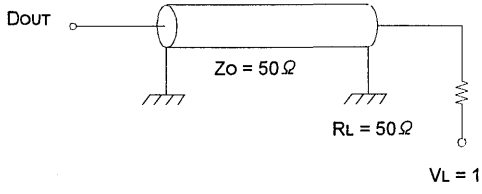
* Including Scope and Jig Capacitance

Fig. 1

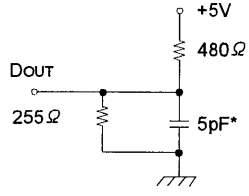
TEST CONDITIONS ON TAG RAM (T_A =0 to 70℃, V_{CC5}=5.0V±5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ & tOW)



* Including Scope and Jig Capacitance

Fig. 2

AC TIMING CHARACTERISTICS ON DATA RAM (T_A =0 to 70℃, V_{CC3}=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V41AG7-13		KMM764V41AG7-15		Unit
		Min	Max	Min	Max	
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	7	ns
Output Enable to Data Valid	tOE	-	6	-	6	ns
Clock High to Output Low-Z	tLZC	0	-	0	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	4	-	4	ns
Clock High to Output High-Z	tHZC	1.5	5	2.0	6	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE :

1. All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever $\overline{CADS}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{CADS}$ or $\overline{ADSP}$ is sampled low in order to the device remained at enable.
3. $\overline{CADS}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clocks after leaving ZZ state.

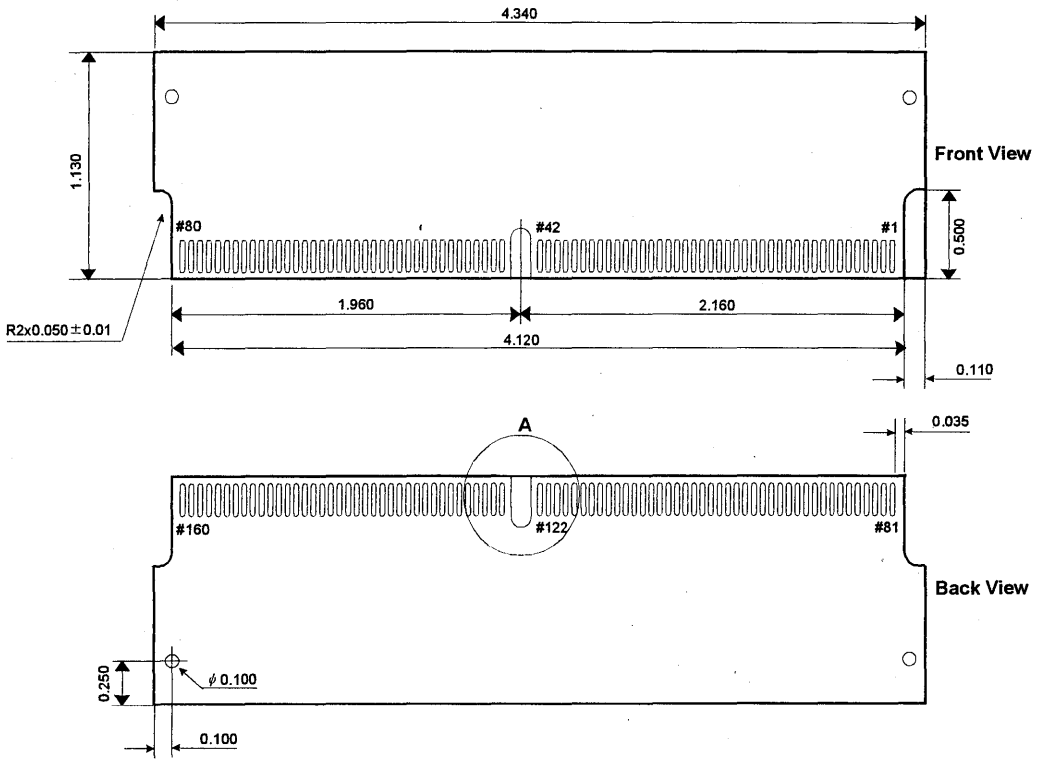
AC TIMING CHARACTERISTICS ON TAG RAM (T_A =0 to 70℃, V_{CC5}=5.0V±5%)

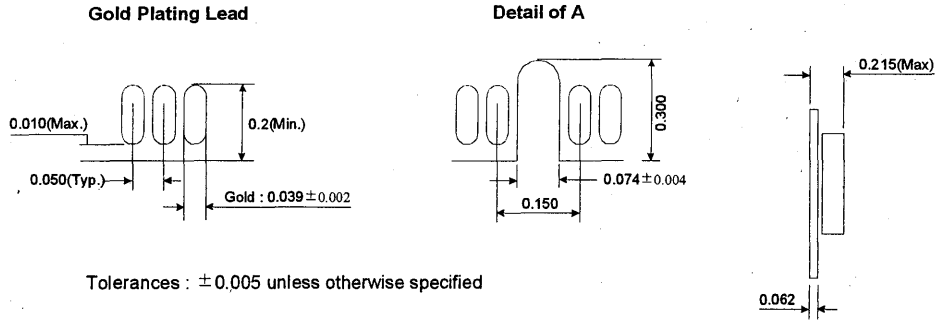
Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V41AG7-13		KMM764V41AG7-15		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	ns
Address Access Time	tAA	-	12	-	15	ns
Chip Select to Output	tCO	-	12	-	15	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	ns
Chip Disable to High-Z Output	tHZ	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Write cycle Time	tWC	12	-	15	-	ns
Chip Select to End of Write	tCW	9	-	11	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	ns
Write Pulse Width	tWP	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

PACKAGE DIMENSIONS

Units : Inches





Tolerances : ±0.005 unless otherwise specified

512KB SPB SRAM Module (Single Bank Operation)

FEATURES

- Implemented based on **COAST 1.4**
- Supports Interleave Burst and Linear Burst Mode
- Single Bank Operation
- Zero-wait-state operation at 75/66MHz
- TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- 160-pin DIMM with gold plated Tap
- PCB : Height (1130mil)
- Product Family : KMM764V72G2-13/15

GENERAL DESCRIPTION

The KMM764V72G2 is 512K byte high-frequency Synchronous Pipelined Burst Static Randomd Access Memory module organized as 64K words by 64 bits. The module is designed specially to function as the secondary cache in Pentium, K5,M1, and Power PC-based systems and using SAMSUNG's PCB design tool. The device for this module is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology.

PIN NAMES

Pin Name	Pin Function
CLK[1:0]	Clock Inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[7:0]	Tag RAM Data Inputs/Outputs
$\overline{TWE}$	Tag RAM Write Enable Input
$\overline{ECS}$[2:1]	Chip Select Inputs for Depth Expansion
$\overline{CCS}$	Chip Select Input
$\overline{CWE}$[7:0]	Write Enable Inputs
$\overline{COE}$	Output Enable Input
$\overline{ADSP}$	Address Status Processor
$\overline{CADS}$	Address Status Controller
$\overline{CADV}$	Burst Address Advance
$\overline{BWE}$	Byte Write Enable Input
$\overline{GWE}$	Grobal Write Enable Input
$\overline{LBO}$	Burst Mode Control
V_{CC5}	Power Supply(5V)
V_{CC3}	Power Supply(3.3V)
Vss	Ground
N.C	No Connections

PD PIN INFORMATION

PD Pin Allocation				Module Part No
PD_3	PD_2	PD_1	PD_0	
Vss	N.C	N.C	N.C	KMM764V72G2

PIN CONFIGURATION *(Top View)*

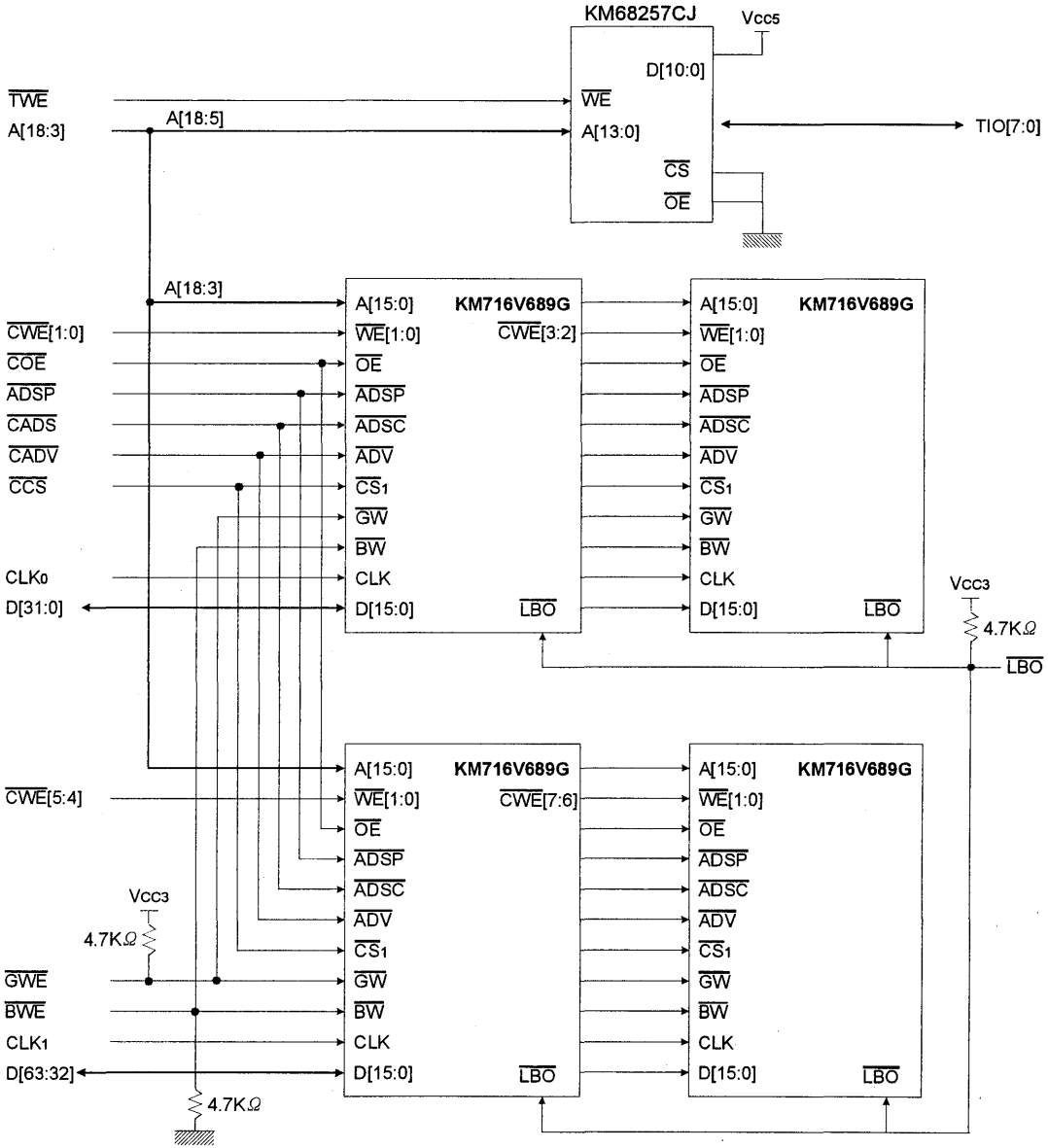
V_{SS}	81	1	V_{SS}	D_{57}	122	42	D_{56}
TIO_1	82	2	TIO_0				
TIO_7	83	3	TIO_2				
TIO_5	84	4	TIO_6	Vss	123	43	Vss
TIO_3	85	5	TIO_4	D_{55}	124	44	D_{54}
N.C	86	6	N.C	D_{53}	125	45	D_{52}
V_{CC5}	87	7	V_{CC3}	D_{51}	126	46	D_{50}
N.C	88	8	$\overline{TWE}$	D_{49}	127	47	D_{48}
$\overline{CADV}$	89	9	$\overline{CADS}$	Vss	128	48	Vss
Vss	90	10	Vss	D_{47}	129	49	D_{46}
$\overline{COE}$	91	11	$\overline{CWE_4}$	D_{45}	130	50	D_{44}
$\overline{CWE_5}$	92	12	$\overline{CWE_6}$	D_{43}	131	51	D_{42}
$\overline{CWE_7}$	93	13	$\overline{CWE_0}$	V_{CC5}	132	52	V_{CC3}
$\overline{CWE_1}$	94	14	$\overline{CWE_2}$	D_{41}	133	53	D_{40}
V_{CC5}	95	15	V_{CC3}	D_{39}	134	54	D_{38}
$\overline{CWE_3}$	96	16	$\overline{CCS}$	D_{37}	135	55	D_{36}
N.C	97	17	$\overline{GWE}$(3)	Vss	136	56	Vss
N.C	98	18	$\overline{BWE}$(3)	D_{35}	137	57	D_{34}
Vss	99	19	Vss	D_{33}	138	58	D_{32}
N.C	100	20	A_3	D_{31}	139	59	D_{30}
A_4	101	21	A_7	V_{CC5}	140	60	V_{CC3}
A_6	102	22	A_5	D_{29}	141	61	D_{28}
A_8	103	23	A_{11}	D_{27}	142	62	D_{26}
A_{10}	104	24	A_{16}	D_{25}	143	63	D_{24}
V_{CC5}	105	25	V_{CC3}	Vss	144	64	Vss
A_{17}	106	26	A_{18}	D_{23}	145	65	D_{22}
Vss	107	27	Vss	D_{21}	146	66	D_{20}
A_9	108	28	A_{12}	D_{19}	147	67	D_{18}
A_{14}	109	29	A_{13}	V_{CC5}	148	68	V_{CC3}
A_{15}	110	30	$\overline{ADSP}$	D_{17}	149	69	D_{16}
N.C	111	31	$\overline{ECS_1}$(1)	D_{15}	150	70	D_{14}
PD_0	112	32	$\overline{ECS_2}$(1)	D_{13}	151	71	D_{12}
PD_2	113	33	PD_1	Vss	152	72	Vss
$\overline{LBO}$(2)	114	34	PD_3	D_{11}	153	73	D_{10}
Vss	115	35	Vss	D_9	154	74	D_8
CLK_0	116	36	CLK_1	D_7	155	75	D_6
Vss	117	37	Vss	V_{CC5}	156	76	V_{CC3}
D_{63}	118	38	D_{62}	D_5	157	77	D_4
V_{CC5}	119	39	V_{CC3}	D3	158	78	D_2
D_{61}	120	30	D_{60}	D_1	159	79	D_0
D_{59}	121	41	D_{58}	Vss	160	80	Vss

NOTE :

1. These pins are used for 256KB module only and they should be no connect for this module.
2. Default is no connect for Intel processor based designs becouse this pin pulled up with 4.7Kohm resistor on the module.
3. When these pins are no connect, all byte write should be controlled by all $\overline{CWEx}$ pins.

FUNCTIONAL BLOCK DIAGRAM

KMM764V72G2



NOTE :

1. ZZ pin is internally connected to Vss and not pinout on the module.
2. $\overline{LBO}$ is pulled up with 4.7Kohm resistor.
3. $\overline{GWE}$ is pulled up with 4.7Kohm resistor and $\overline{BWE}$ is pulled down with 4.7Kohm resistor.

A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

$\overline{CCS}$	$\overline{ADSP}$	$\overline{CADS}$	$\overline{CADV}$	$\overline{WRITE}$	K	Address Accessed	Operation
H	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	N/A	Not Selected
L	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Read Cycle
H	X	H	L	L	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Read Cycle
H	X	H	H	L	↑	Current Address	Suspend Burst Read Cycle

NOTE :

1. X means "Don't Care"
2. The rising edge of clock is symbolized by ↑
3. $\overline{WRITE}$=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table
   $\overline{WRITE}$=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table
4. Operation finally depends on status of asynchronous input pin ($\overline{COE}$)

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE(Data field)

$\overline{GWE}$	$\overline{BWE}$	$\overline{CWE}$[1:0]	$\overline{CWE}$[3:2]	$\overline{CWE}$[5:4]	$\overline{CWE}$[7:6]	Operation
H	H	X	X	X	X	Read
H	L	H	H	H	H	Read
H	L	L	H	H	H	Write Byte D[15:0]
H	L	H	L	H	H	Write Byte D[31:16]
H	L	H	H	L	L	Write Byte D[63:32]
H	L	L	L	L	L	Write All Bytes
L	X	X	X	X	X	Write All Bytes

NOTE :

1. X means "Don't Care"
2. All input in this table must meet setup and hold time around the rising edge of CLK(↑).

B-1. ASYNCHRONOUS TRUTH TABLE(Tag field)

$\overline{TWE}$	Mode	I/O Pin	Supply Current
H	Read	DOUT	ICC
L	Write	DIN	ICC

NOTE : X means "Don't Care"

C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO# pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	High	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	0	0	1	1	1	0
Third Address		1	0	1	1	0	0	0	1
Fouth Address		1	1	1	0	0	1	0	0

NOTE :

1. When this pin is no connects, $\overline{LBO}$ should be high.
2. Dafault is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	1	0	1	1	0	0
Third Address		1	0	1	1	0	0	0	1
Fouth Address		1	1	0	0	0	1	1	0

NOTE : $\overline{LBO}$ must be tied to low because this pin is pulled up with 4.7KΩ on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{CC3} Supply Relative to Vss	V_{CC3}	-0.3 to 4.6	V
Voltage on V_{CC5} Supply Relative to Vss	V_{CC5}	-0.3 to 6.0	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any outher conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (T_A =0 to 70℃)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC3}	3.13	3.3	3.6	V
	V_{CC5}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IL}*	-0.3	-	0.8	V
Input High Voltage	V_{IH}*	2.2	-	Vcc***+0.3	V

* V_{IL3}(min) = -1.4 (Pulse Width ≤ 10ns), V_{IL5}(min) = -2.0 (Pulse Width ≤ 10ns)

** V_{IH3}(max) = 5.0V (Pulse Width ≤ 10ns) ; In case of I/O pins, the maximum V_{IH3}(max) = 4.1V (Pulse Width ≤ 10ns)
V_{IH5}(max) = 7.0V (Pulse width ≤ 10ns)

*** V_{CC} =V_{CC3} or V_{CC5}

DC ELECTRICAL CHARACTERISTICS* (T_A =0 to 70℃,V_{CC3}=3.3V+10%/-5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage current	I_{LI}**	V_{CC3}=Max, V_{IN}=Vss to V_{CC3}		-5	5	μA
Output Leakage Current	I_{LO}	Output Disable, V_{OUT}=Vss to V_{CC3}		-5	5	μA
Operating Current	I_{CC}	f=MAX, 100% Duty V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	75MHz	-	800	mA
			66MHz	-	720	
Standby Current	I_{SB}	f=MAX, 100% Duty, Device deselected, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		-	120	mA
	I_{SB1}	f=MAX, 100% Duty, Device deselected, V_{IN}≥V_{CC3} -0.2V or V_{IL}, V_{IN} ≤ 0.2V, I_{OUT}=0mA		-	20	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

* Excludes Tag field.

** ILI for $\overline{LBO}$(pin 114), $\overline{GWE}$(pin 17) and $\overline{BWE}$(pin 18) is ±1mA(Max.)

CAPACITANCE*(f=1MHz,T_A=25℃)

Item	Symbol	Test Condition	Min.	Max.	Unit
Address, $\overline{ECS}$ Input Capacitance	C_{IN1}	V_{IN}=0V	-	40	pF
$\overline{TWE}$, $\overline{CWE}$, CLK Input Capacitance	C_{IN2}	V_{IN}=0V	-	20	pF
$\overline{COE}$, $\overline{ADSP}$, $\overline{CADS}$, $\overline{CADV}$, $\overline{CCS}$ $\overline{GWE}$, $\overline{BWE}$ Input Capacitance	C_{IN3}	V_{IN}=0V	-	30	pF
Data and Tag Input/Output Capacitance	$C_{I/O1}$	$V_{I/O}$=0V	-	15	pF

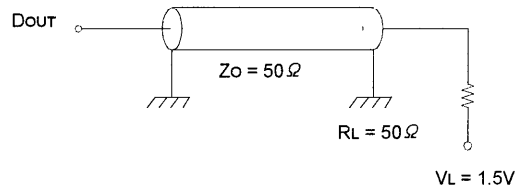
*** NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

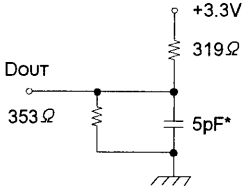
TEST CONDITIONS ON DATA RAM (T_A =0 to 70℃, $V_{CC}3$=3.3V+10%/-5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tLZC, tLZOE, tHZOE & tHZC)



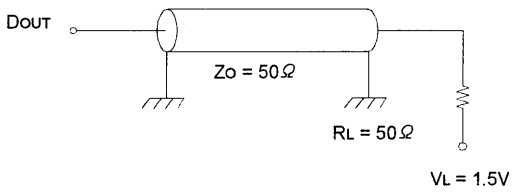
* Including Scope and Jig Capacitance

Fig. 1

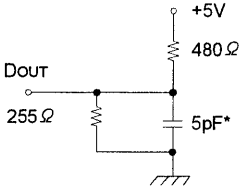
TEST CONDITIONS ON TAG RAM (T_A =0 to 70℃, $V_{CC}5$=5.0V±5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ & tOW)



* Including Scope and Jig Capacitance

Fig. 2

AC TIMING CHARACTERISTICS ON DATA RAM (T_A =0 to 70℃, V_{CC3}=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V72G2-13		KMM764V72G2-15		Unit
		Min	Max	Min	Max	
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	8	ns
Output Enable to Data Valid	tOE	-	6	-	7	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	2	-	2	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	ns
Clock High to Output High-Z	tHZC	-	7	-	7	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE :

1. All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever $\overline{CADS}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{CADS}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
3. $\overline{CADS}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clocks after leaving ZZ state.

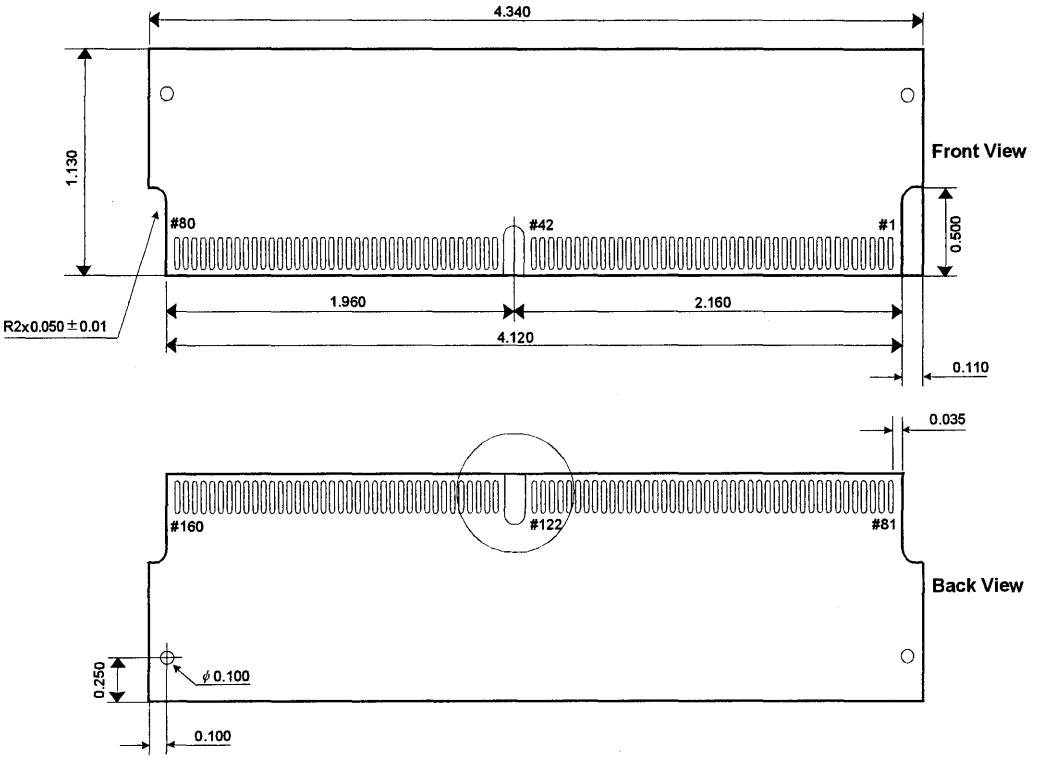
AC TIMING CHARACTERISTICS ON TAG RAM (T_A =0 to 70℃, V_{CC5}=5.0V±5%)

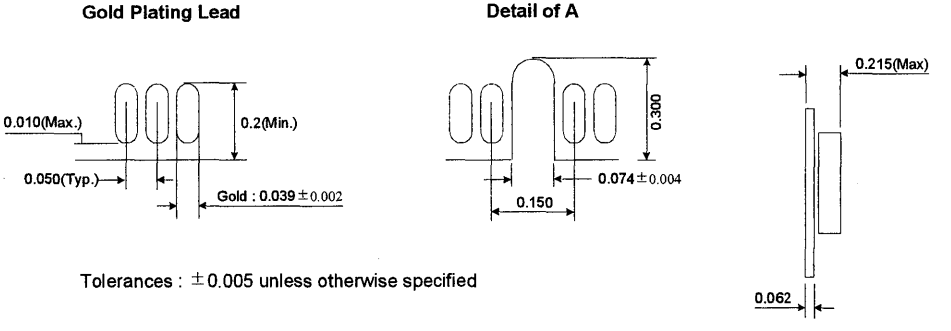
Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V72G2-13		KMM764V72G2-15		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	ns
Address Access Time	tAA	-	12	-	15	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Write cycle Time	tWC	12	-	15	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	ns
Write Pulse Width	tWP	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

PACKAGE DIMENSIONS

Units : Inches





Tolerances : ±0.005 unless otherwise specified

512KB SPB SRAM Module (Single Bank Operation)

FEATURES

- Implemented based on **COAST 1.4**
- Supports Interleave Burst and Linear Burst Mode
- Single Bank Operation
- Zero-wait-state operation at 75/66MHz
- TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- 160-pin DIMM with gold plated Tap
- Series 22 ohm resistors for nuose immunity
- Product Family : KMM764V72G7-13/15

GENERAL DESCRIPTION

The KMM764V72G7 is 512K byte high-frequency Synchronous Pipelined Burst Static Randomd Access Memory module organized as 64K words by 64 bits. The module is designed specially to function as the secondary cache in Pentium and Power PC-based systems. The device for this module is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. The module uses four SAMSUNG's KM716V689G and KM68257C for 8-bits tag RAM.

PIN NAMES

Pin Name	Pin Function
CLK[1:0]	Clock Inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[10:0]	Tag RAM Data Inputs/Outputs
$\overline{TWE}$	Tag RAM Write Enable Input
$\overline{ECS}$[2:1]	Chip Select Inputs for Depth Expansion
$\overline{CCS}$	Chip Select Input
$\overline{CWE}$[7:0]	Write Enable Inputs
$\overline{COE}$	Output Enable Input
$\overline{ADSP}$	Address Status Processor
$\overline{CADS}$	Address Status Controller
$\overline{CADV}$	Burst Address Advance
$\overline{BWE}$	Byte Write Enable Input
$\overline{GWE}$	Grobal Write Enable Input
$\overline{LBO}$	Burst Mode Control
Vcc5	Power Supply(5V)
Vcc3	Power Supply(3.3V)
Vss	Ground
N.C	No Connections

PD PIN INFORMATION

PD Pin Allocation				Module Part No
PD3	PD2	PD1	PD0	
Vss	N.C	N.C	N.C	KMM764V72G7

PIN CONFIGURATION *(Top View)*

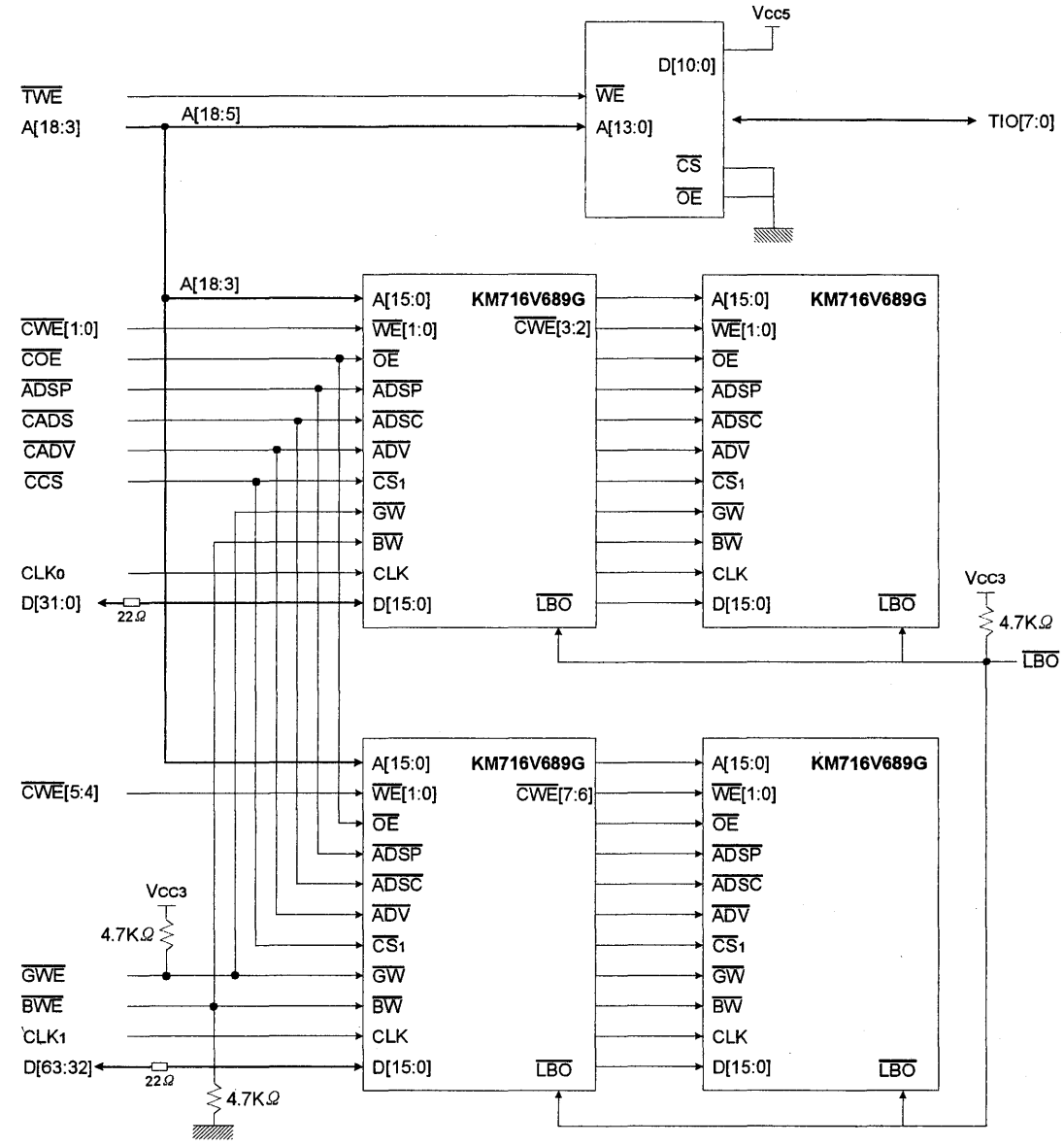
Vss	81	1	Vss	D57	122	42	D58
TIO1	82	2	TIO0				
TIO7	83	3	TIO2				
TIO5	84	4	TIO6	Vss	123	43	Vss
TIO3	85	5	TIO4	D55	124	44	D54
N.C	86	6	N.C	D53	125	45	D52
Vcc5	87	7	Vcc3	D51	126	46	D50
N.C	88	8	$\overline{TWE}$	D49	127	47	D48
$\overline{CADV}$	89	9	$\overline{CADS}$	Vss	128	48	Vss
Vss	90	10	Vss	D47	129	49	D46
$\overline{COE}$	91	11	$\overline{CWE}$4	D45	130	50	D44
$\overline{CWE}$5	92	12	$\overline{CWE}$6	D43	131	51	D42
$\overline{CWE}$7	93	13	$\overline{CWE}$0	Vcc5	132	52	Vcc3
$\overline{CWE}$1	94	14	$\overline{CWE}$2	D41	133	53	D40
Vcc5	95	15	Vcc3	D39	134	54	D38
$\overline{CWE}$3	96	16	$\overline{CCS}$	D37	135	55	D36
N.C	97	17	$\overline{GWE}$(3)	Vss	136	56	Vss
N.C	98	18	$\overline{BWE}$(3)	D35	137	57	D34
Vss	99	19	Vss	D33	138	58	D32
N.C	100	20	A3	D31	139	59	D30
A4	101	21	A7	Vcc5	140	60	Vcc3
A6	102	22	A5	D29	141	61	D28
A8	103	23	A11	D27	142	62	D26
A10	104	24	A16	D25	143	63	D24
Vcc5	105	25	Vcc3	Vss	144	64	Vss
A17	106	26	A18	D23	145	65	D22
Vss	107	27	Vss	D21	146	66	D20
A9	108	28	A12	D19	147	67	D18
A14	109	29	A13	Vcc5	148	68	Vcc3
A15	110	30	$\overline{ADSP}$	D17	149	69	D16
N.C	111	31	$\overline{ECS}$1(1)	D15	150	70	D14
PD0	112	32	$\overline{ECS}$2(1)	D13	151	71	D12
PD2	113	33	PD1	Vss	152	72	Vss
$\overline{LBO}$(2)	114	34	PD3	D11	153	73	D10
Vss	115	35	Vss	D9	154	74	D8
CLK0	116	36	CLK1	D7	155	75	D6
Vss	117	37	Vss	Vcc5	156	76	Vcc3
D63	118	38	D62	D5	157	77	D4
Vcc5	119	39	Vcc3	D3	158	78	D2
D61	120	30	D60	D1	159	79	D0
D59	121	41	D58	Vss	160	80	Vss

NOTE :

1. These pins are used for 256KB module only and they should be no connect for this module.
2. Default is no connect for Intel processor based designs becouse this pin pulled up with 4.7Kohm resistor on the module.
3. When these pins are no connect, all byte write should be controlled by all $\overline{CWEx}$ pins.

FUNCTIONAL BLOCK DIAGRAM

KMM764V72G7



NOTE :

1. ZZ pin is internally connected to Vss and not pinout on the module.
2. $\overline{LBO}$ is pulled up with 4.7Kohm resistor.
3. $\overline{GWE}$ is pulled up with 4.7Kohm resistor and $\overline{BWE}$ is pulled down with 4.7Kohm resistor.

A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

$\overline{CCS}$	$\overline{ADSP}$	$\overline{CADS}$	$\overline{CADV}$	$\overline{WRITE}$	K	Address Accessed	Operation
H	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	N/A	Not Selected
L	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Read Cycle
H	X	H	L	L	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Read Cycle
H	X	H	H	L	↑	Current Address	Suspend Burst Read Cycle

NOTE :

1. X means "Don't Care"
2. The rising edge of clock is symbolized by ↑
3. $\overline{WRITE}$=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table
   $\overline{WRITE}$=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table
4. Operation finally depends on status of asynchronous input pin ($\overline{COE}$)

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE(Data field)

$\overline{GWE}$	$\overline{BWE}$	$\overline{CWE}$[1:0]	$\overline{CWE}$[3:2]	$\overline{CWE}$[5:4]	$\overline{CWE}$[7:6]	Operation
H	H	X	X	X	X	Read
H	L	H	H	H	H	Read
H	L	L	H	H	H	Write Byte D[15:0]
H	L	H	L	H	H	Write Byte D[31:16]
H	L	H	H	L	L	Write Byte D[63:32]
H	L	L	L	L	L	Write All Bytes
L	X	X	X	X	X	Write All Bytes

NOTE :

1. X means "Don't Care"
2. All input in this table must meet setup and hold time around the rising edge of CLK(↑).

B-1. ASYNCHRONOUS TRUTH TABLE(Tag field)

$\overline{TWE}$	Mode	I/O Pin	Supply Current
H	Read	DOUT	ICC
L	Write	DIN	ICC

NOTE : X means "Don't Care"

C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO# pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	High	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	0	0	1	1	1	0
Third Address		1	0	1	1	0	0	0	1
Fouth Address		1	1	1	0	0	1	0	0

NOTE :

1. When this pin is no connects, $\overline{LBO}$ should be high.
2. Dafault is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	1	0	1	1	0	0
Third Address		1	0	1	1	0	0	0	1
Fouth Address		1	1	0	0	0	1	1	0

NOTE : $\overline{LBO}$ must be tied to low because this pin is pulled up with 4.7KΩ on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{CC3} Supply Relative to V_{SS}	V_{CC3}	-0.3 to 4.6	V
Voltage on V_{CC5} Supply Relative to V_{SS}	V_{CC5}	-0.3 to 6.0	V
Voltage on Any Other Pin Relative to V_{SS}	V_{IN}	-0.3 to 6.0	V
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any outher conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (T_A =0 to 70℃)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC3}	3.13	3.3	3.6	V
	V_{CC5}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IL}*	-0.3	-	0.8	V
Input High Voltage	V_{IH}*	2.2	-	Vcc***+0.3	V

* V_{IL3}(min) = -1.4 (Pulse Width ≤ 10ns), V_{IL5}(min) = -2.0 (Pulse Width ≤ 10ns)

** V_{IH3}(max) = 5.0V (Pulse Width ≤ 10ns) ; In case of I/O pins, the maximum V_{IH3}(max) = 4.1V (Pulse Width ≤ 10ns)
V_{IH5}(max) = 7.0V (Pulse width ≤ 10ns)

*** Vcc =V_{CC3} or V_{CC5}

2

DC ELECTRICAL CHARACTERISTICS* (T_A =0 to 70℃, V_{CC3}=3.3V+10%/-5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage current	I_{LI}**	V_{CC3}=Max, V_{IN}=Vss to V_{CC3}		-5	5	μA
Output Leakage Current	I_{LO}	Output Disable, V_{OUT}=Vss to V_{CC3}		-5	5	μA
Operating Current	I_{CC}	f=MAX, 100% Duty V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	75MHz	-	800	mA
			66MHz	-	720	
Standby Current	I_{SB}	f=MAX, 100% Duty, Device deselected, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		-	120	mA
	I_{SB1}	f=MAX, 100% Duty, Device deselected, V_{IN}≥V_{CC3} -0.2V or V_{IL}, V_{IN} ≤ 0.2V, I_{OUT}=0mA		-	20	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

* Excludes Tag field.

** ILI for $\overline{LBO}$, $\overline{GWE}$ and $\overline{BWE}$ is ±1mA (Max.)

CAPACITANCE*(f=1MHz, T_A=25℃)

Item	Symbol	Test Condition	Min.	Max.	Unit
Address, $\overline{ECS}$ Input Capacitance	C_{IN1}	V_{IN}=0V	-	45	pF
$\overline{TWE}$, $\overline{CWE}$, CLK Input Capacitance	C_{IN2}	V_{IN}=0V	-	20	pF
$\overline{COE}$, $\overline{ADSP}$, $\overline{CADS}$, $\overline{CADV}$, $\overline{CCS}$ $\overline{GWE}$, $\overline{BWE}$ Input Capacitance	C_{IN3}	V_{IN}=0V	-	30	pF
Data and Tag Input/Output Capacitance	$C_{I/O1}$	$V_{I/O}$=0V	-	15	pF

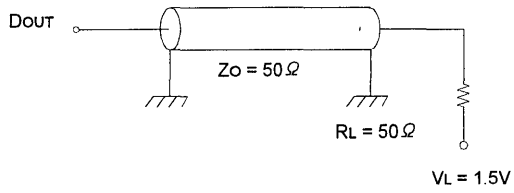
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

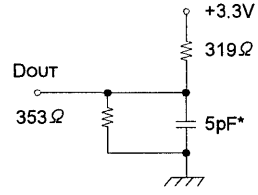
TEST CONDITIONS ON DATA RAM (T_A =0 to 70℃,Vcc3=3.3V+10%/-5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tLZC, tLZOE, tHZOE & tHZC)



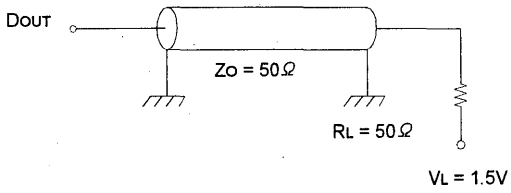
* Including Scope and Jig Capacitance

Fig. 1

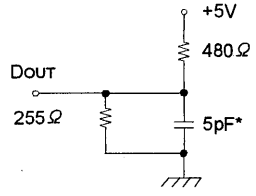
TEST CONDITIONS ON TAG RAM (T_A =0 to 70℃,Vcc5=5.0V±5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ & tOW)



* Including Scope and Jig Capacitance

Fig. 2

AC TIMING CHARACTERISTICS ON DATA RAM (T_A =0 to 70℃, V_{CC3}=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V72G7-13		KMM764V72G7-15		Unit
		Min	Max	Min	Max	
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	8	ns
Output Enable to Data Valid	tOE	-	6	-	7	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	2	-	2	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	ns
Clock High to Output High-Z	tHZC	-	7	-	7	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE :

1. All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever $\overline{CADS}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{CADS}$ or $\overline{ADSP}$ is sampled low in order to the device remained at enable.
3. $\overline{CADS}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clocks after leaving ZZ state.

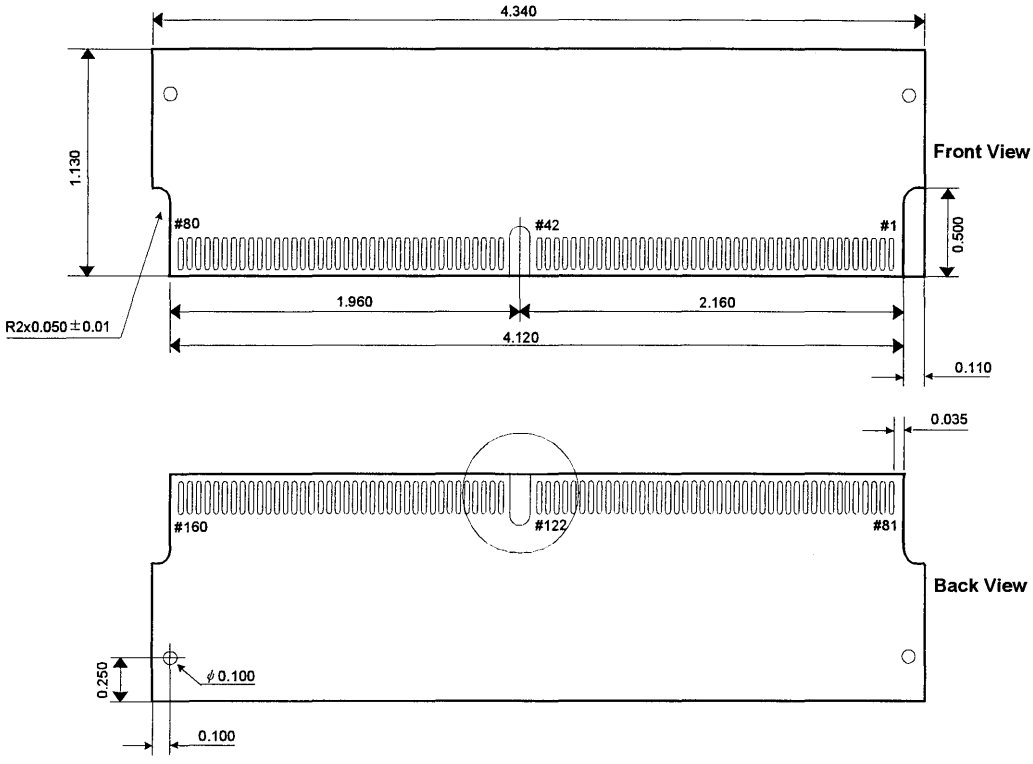
AC TIMING CHARACTERISTICS ON TAG RAM (T_A =0 to 70℃, V_{CC5}=5.0V±5%)

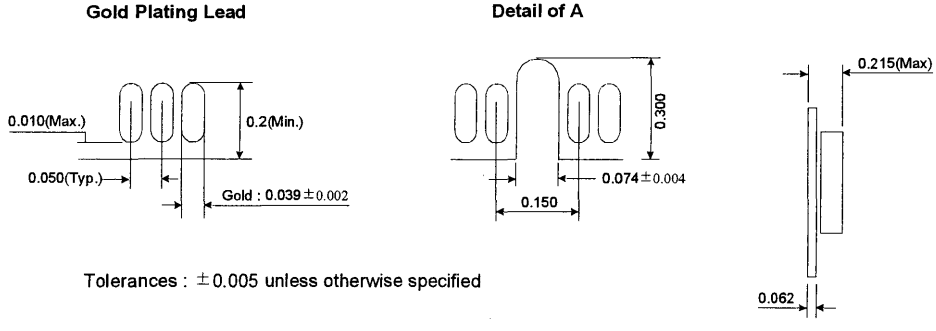
Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V72G7-13		KMM764V72G7-15		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	ns
Address Access Time	tAA	-	12	-	15	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Write cycle Time	tWC	12	-	15	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	ns
Write Pulse Width	tWP	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

PACKAGE DIMENSIONS

Units : Inches





Tolerances : ±0.005 unless otherwise specified

512KB SPB SRAM Module (Single Bank Operation)

FEATURES

- Implemented based on **COAST 3.1**
- Supports Interleave Burst and Linear Burst Mode
- Single Bank Operation
- Zero-wait-state operation at 75/66MHz
- TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- 160-pin DIMM with gold plated Tap
- Series 22 ohm resistors for nuose immunity
- Product Family : KMM764V75G-13/15

GENERAL DESCRIPTION

The KMM764V75G is 512K byte high-frequency Synchronous Pipelined Burst Static Randomd Access Memory module organized as 64K words by 64 bits. The module is designed specially to function as the secondary cache in Pentium and Power PC-based systems. The device for this module is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. The module uses four SAMSUNG's KM716V689G and KM68257C for 11-bits tag RAM.

PIN NAMES

Pin Name	Pin Function
CLK[1:0]	Clock Inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[10:0]	Tag RAM Data Inputs/Outputs
$\overline{TWE}$	Tag RAM Write Enable Input
$\overline{ECS}$[2:1]	Chip Select Inputs for Depth Expansion
$\overline{CCS}$	Chip Select Input
$\overline{CWE}$[7:0]	Write Enable Inputs
$\overline{COE}$	Output Enable Input
$\overline{ADSP}$	Address Status Processor
$\overline{CADS}$	Address Status Controller
$\overline{CADV}$	Burst Address Advance
$\overline{BWE}$	Byte Write Enable Input
$\overline{GWE}$	Grobal Write Enable Input
$\overline{LBO}$	Burst Mode Control
V_{CC5}	Power Supply(5V)
V_{CC3}	Power Supply(3.3V)
Vss	Ground
N.C	No Connections

PD PIN INFORMATION

PD Pin Allocation				Module Part No
PD_3	PD_2	PD_1	PD_0	
Vss	N.C	N.C	N.C	KMM764V75G

PIN CONFIGURATION *(Top View)*

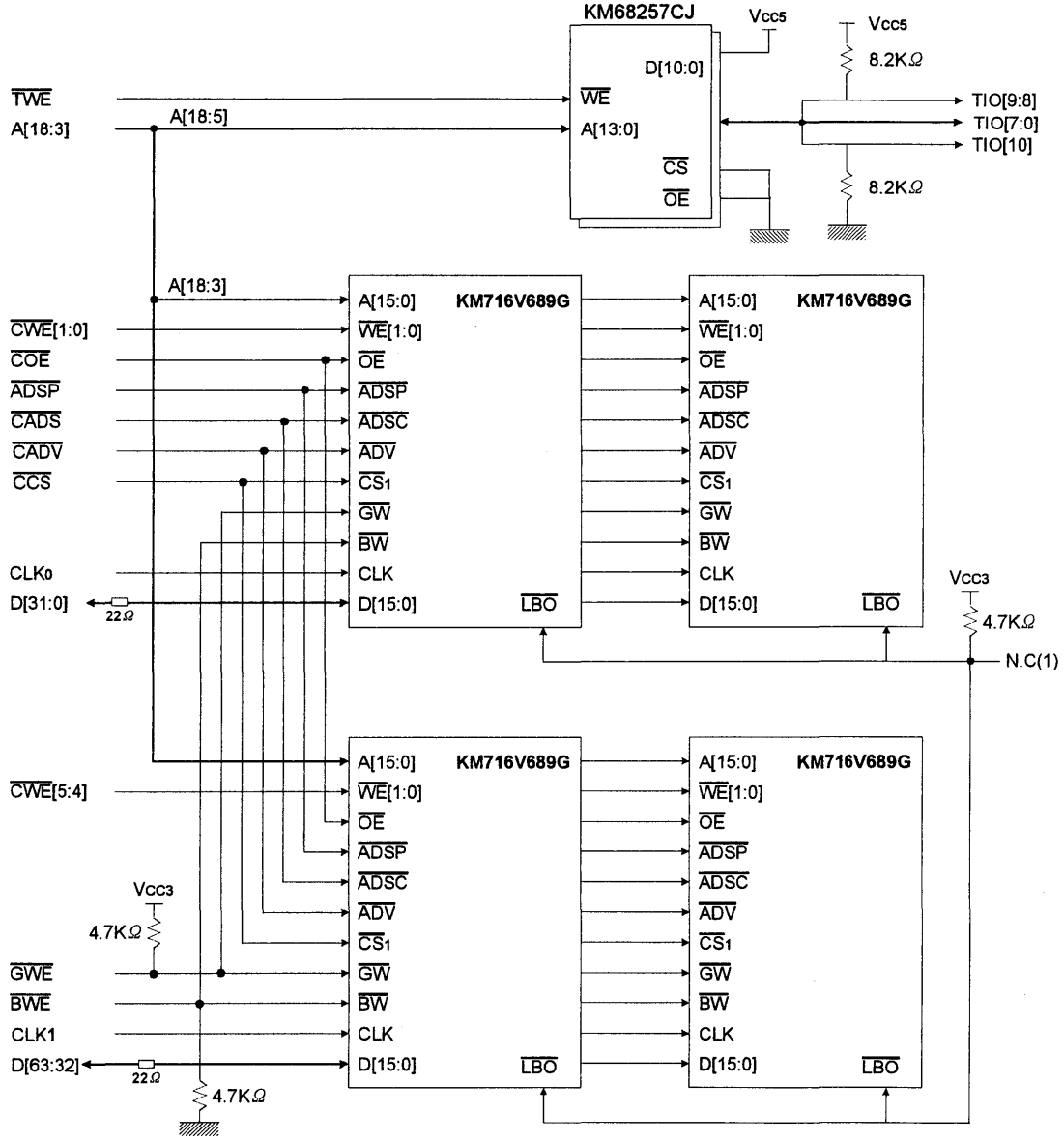
Vss	81	1	Vss	D_{57}	122	42	D_{56}
TIO_1	82	2	TIO_0				
TIO_7	83	3	TIO_2				
TIO_5	84	4	TIO_6	Vss	123	43	Vss
TIO_3	85	5	TIO_4	D_{55}	124	44	D_{54}
TIO_9	86	6	TIO_8	D_{53}	125	45	D_{52}
V_{CC5}	87	7	V_{CC3}	D_{51}	126	46	D_{50}
TIO_{10}	88	8	$\overline{TWE}$	D_{49}	127	47	D_{48}
$\overline{CADV}$	89	9	$\overline{CADS}$	Vss	128	48	Vss
Vss	90	10	Vss	D_{47}	129	49	D_{46}
$\overline{COE}$	91	11	$\overline{CWE_4}$	D_{45}	130	50	D_{44}
$\overline{CWE_5}$	92	12	$\overline{CWE_6}$	D_{43}	131	51	D_{42}
$\overline{CWE_7}$	93	13	$\overline{CWE_0}$	V_{CC5}	132	52	V_{CC3}
$\overline{CWE_1}$	94	14	$\overline{CWE_2}$	D_{41}	133	53	D_{40}
V_{CC5}	95	15	V_{CC3}	D_{39}	134	54	D_{38}
$\overline{CWE_3}$	96	16	$\overline{CCS}$	D_{37}	135	55	D_{36}
N.C	97	17	$\overline{GWE}$(3)	Vss	136	56	Vss
N.C	98	18	$\overline{BWE}$(3)	D_{35}	137	57	D_{34}
Vss	99	19	Vss	D_{33}	138	58	D_{32}
N.C	100	20	A_3	D_{31}	139	59	D_{30}
A_4	101	21	A_7	V_{CC5}	140	60	V_{CC3}
A_6	102	22	A_5	D_{29}	141	61	D_{28}
A_8	103	23	A_{11}	D_{27}	142	62	D_{26}
A_{10}	104	24	A_{16}	D_{25}	143	63	D_{24}
V_{CC5}	105	25	V_{CC3}	Vss	144	64	Vss
A_{17}	106	26	A_{18}	D_{23}	145	65	D_{22}
Vss	107	27	Vss	D_{21}	146	66	D_{20}
A_9	108	28	A_{12}	D_{19}	147	67	D_{18}
A_{14}	109	29	A_{13}	V_{CC5}	148	68	V_{CC3}
A_{15}	110	30	$\overline{ADSP}$	D_{17}	149	69	D_{16}
N.C	111	31	$\overline{ECS_1}$(1)	D_{15}	150	70	D_{14}
PD_0	112	32	$\overline{ECS_2}$(1)	D_{13}	151	71	D_{12}
PD_2	113	33	PD_1	Vss	152	72	Vss
$\overline{LBO}$(2)	114	34	PD_3	D_{11}	153	73	D_{10}
Vss	115	35	Vss	D_9	154	74	D_8
CLK_0	116	36	CLK_1	D_7	155	75	D_6
Vss	117	37	Vss	V_{CC5}	156	76	V_{CC3}
D_{63}	118	38	D_{62}	D_5	157	77	D_4
V_{CC5}	119	39	V_{CC3}	D3	158	78	D_2
D_{61}	120	30	D_{60}	D_1	159	79	D_0
D_{59}	121	41	D_{58}	Vss	160	80	Vss

NOTE :

1. These pins are used for 256KB module only and they should be no connect for this module.
2. Default is no connect for Intel processor based designs becouse this pin pulled up with 4.7Kohm resistor on the module.
3. When these pins are no connect, all byte write should be controlled by all $\overline{CWEx}$ pins.

FUNCTIONAL BLOCK DIAGRAM

KMM764V75G



NOTE :

1. ZZ pin is internally connected to Vss and not pinout on the module.
2. $\overline{LBO}$ is pulled up with 4.7Kohm resistor.
3. $\overline{GWE}$ is pulled up with 4.7Kohm resistor and $\overline{BWE}$ is pulled down with 4.7Kohm resistor.

A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE(Data field)

$\overline{CCS}$	$\overline{ADSP}$	$\overline{CADS}$	$\overline{CADV}$	$\overline{WRITE}$	K	Address Accessed	Operation
H	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	N/A	Not Selected
L	X	L	X	X	↑	N/A	Not Selected
L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	X	L	↑	External Address	Begin Burst Read Cycle
L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	H	H	L	L	↑	Next Address	Continue Burst Read Cycle
H	X	H	L	L	↑	Next Address	Continue Burst Read Cycle
X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	H	H	H	L	↑	Current Address	Suspend Burst Read Cycle
H	X	H	H	L	↑	Current Address	Suspend Burst Read Cycle

NOTE :

1. X means "Don't Care"
2. The rising edge of clock is symbolized by ↑
3. $\overline{WRITE}$=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table
   $\overline{WRITE}$=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table
4. Operation finally depends on status of asynchronous input pin ($\overline{COE}$)

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE(Data field)

$\overline{GWE}$	$\overline{BWE}$	$\overline{CWE}$[1:0]	$\overline{CWE}$[3:2]	$\overline{CWE}$[5:4]	$\overline{CWE}$[7:6]	Operation
H	H	X	X	X	X	Read
H	L	H	H	H	H	Read
H	L	L	H	H	H	Write Byte D[15:0]
H	L	H	L	H	H	Write Byte D[31:16]
H	L	H	H	L	L	Write Byte D[63:32]
H	L	L	L	L	L	Write All Bytes
L	X	X	X	X	X	Write All Bytes

NOTE :

1. X means "Don't Care"
2. All input in this table must meet setup and hold time around the rising edge of CLK(↑).

B-1. ASYNCHRONOUS TRUTH TABLE(Tag field)

$\overline{TWE}$	Mode	I/O Pin	Supply Current
H	Read	DOUT	ICC
L	Write	DIN	ICC

NOTE : X means "Don't Care"

C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO# pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	High	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	0	0	1	1	1	0
Third Address		1	0	1	1	0	0	0	1
Fouth Address		1	1	1	0	0	1	0	0

NOTE :

1. When this pin is no connects, $\overline{LBO}$ should be high.
2. Dafault is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	1	0	1	1	0	0
Third Address		1	0	1	1	0	0	0	1
Fouth Address		1	1	0	0	0	1	1	0

NOTE : $\overline{LBO}$ must be tied to low because this pin is pulled up with 4.7KΩ on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{CC3} Supply Relative to Vss	V_{CC3}	-0.3 to 4.6	V
Voltage on V_{CC5} Supply Relative to Vss	V_{CC5}	-0.3 to 6.0	V
Voltage on Any Other Pin Relative to Vss	V_{IN}	-0.3 to 6.0	V
Storage Temperature	T_{STG}	-65 to 150	℃
Operating Temperature	T_A	0 to 70	℃
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	℃

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any outher conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (T_A =0 to 70℃)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC3}	3.13	3.3	3.6	V
	V_{CC5}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IL}*	-0.3	-	0.8	V
Input High Voltage	V_{IH}*	2.2	-	Vcc***+0.3	V

* V_{IL3}(min) = -1.4 (Pulse Width ≤ 10ns), V_{IL5}(min) = -2.0 (Pulse Width ≤ 10ns)

** V_{IH3}(max) = 5.0V (Pulse Width ≤ 10ns) ; In case of I/O pins, the maximum V_{IH3}(max) = 4.1V (Pulse Width ≤ 10ns)
V_{IH5}(max) = 7.0V (Pulse width ≤ 10ns)

*** V_{CC} =V_{CC3} or V_{CC5}

DC ELECTRICAL CHARACTERISTICS*(T_A =0 to 70℃,Vcc3=3.3V+10%/-5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage current	I_{LI}**	V_{CC3}=Max, V_{IN}=Vss to V_{CC3}		-5	5	μA
Output Leakage Current	I_{LO}	Output Disable, V_{OUT}=Vss to V_{CC3}		-5	5	μA
Operating Current	I_{CC}	f=MAX, 100% Duty V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	75MHz	-	800	mA
			66MHz	-	720	
Standby Current	I_{SB}	f=MAX, 100% Duty, Device deselected, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		-	120	mA
	I_{SB1}	f=MAX, 100% Duty, Device deselected, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		-	20	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

* Excludes Tag field.

** ILI for $\overline{LBO}$, $\overline{GWE}$, TIO(8,9,10) and $\overline{BWE}$ is ±1mA(Max.)

CAPACITANCE*(f=1MHz,T_A=25℃)

Item	Symbol	Test Condition	Min.	Max.	Unit
Address, $\overline{ECS}$ Input Capacitance	C_{IN1}	V_{IN}=0V	-	45	pF
$\overline{TWE}$, $\overline{CWE}$, CLK Input Capacitance	C_{IN2}	V_{IN}=0V	-	20	pF
$\overline{COE}$, $\overline{ADSP}$, $\overline{CADS}$, $\overline{CADV}$, $\overline{CCS}$ $\overline{GWE}$, $\overline{BWE}$ Input Capacitance	C_{IN3}	V_{IN}=0V	-	30	pF
Data and Tag Input/Output Capacitance	$C_{I/O1}$	$V_{I/O}$=0V	-	15	pF

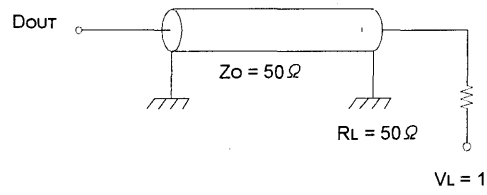
* **NOTE** : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

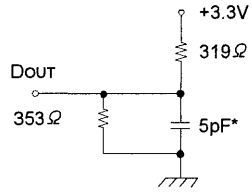
TEST CONDITIONS ON DATA RAM (TA =0 to 70℃,Vcc3=3.3V+10%/-5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tLZC, tLZOE, tHZOE & tHZC)



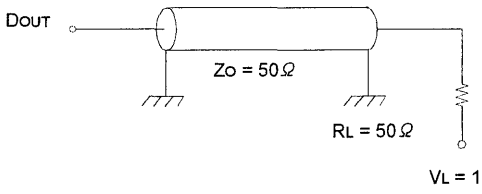
* Including Scope and Jig Capacitance

Fig. 1

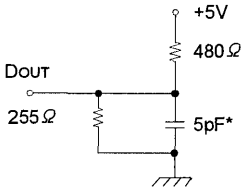
TEST CONDITIONS ON TAG RAM (TA =0 to 70℃,Vcc5=5.0V±5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ & tOW)



* Including Scope and Jig Capacitance

Fig. 2

AC TIMING CHARACTERISTICS ON DATA RAM (T_A =0 to 70℃, V_{CC3}=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V75G-13		KMM764V75G-15		Unit
		Min	Max	Min	Max	
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	8	ns
Output Enable to Data Valid	tOE	-	6	-	7	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	2	-	2	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	ns
Clock High to Output High-Z	tHZC	-	7	-	7	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	cycle

NOTE :

1. All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever $\overline{CADS}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{CADS}$ or $\overline{ADSP}$ is sampled low in order to the device remained at enable.
3. $\overline{CADS}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clocks after leaving ZZ state.

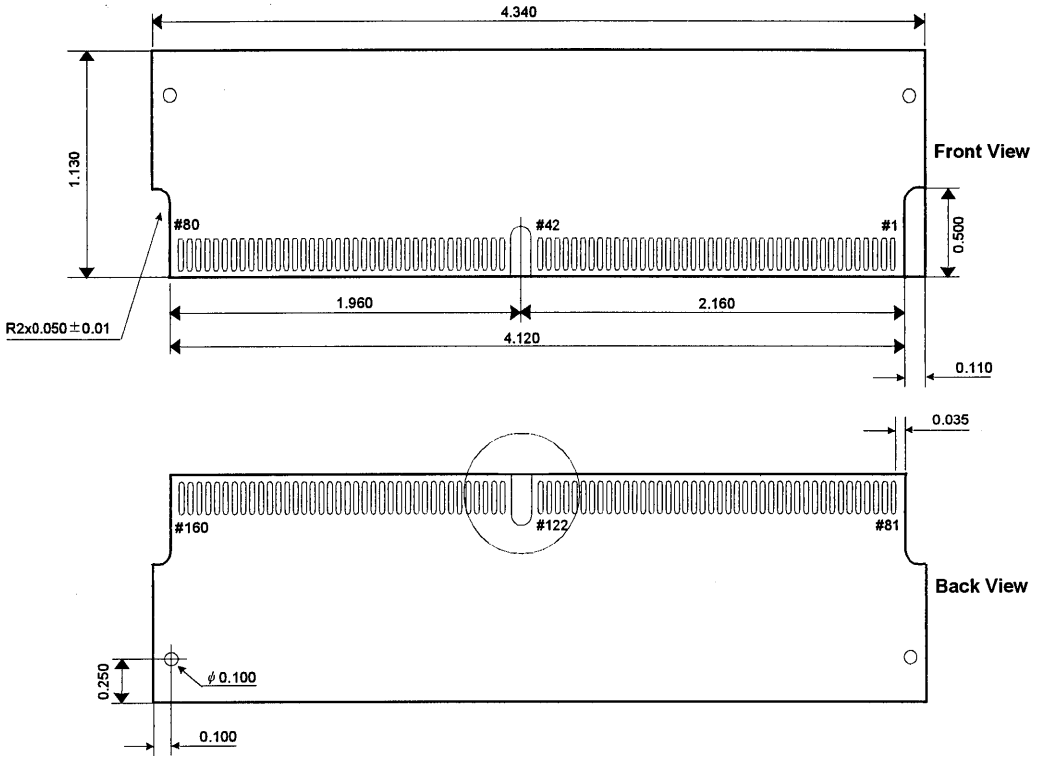
AC TIMING CHARACTERISTICS ON TAG RAM (T_A =0 to 70℃, V_{CC5}=5.0V±5%)

Refers to the individual components, not the whole module

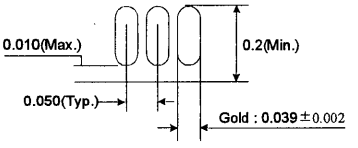
Parameter	Symbol	KMM764V75G-13		KMM764V75G-15		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	ns
Address Access Time	tAA	-	12	-	15	ns
Chip Select to Low-Z Output	tLZ	3	-	3	-	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Write cycle Time	tWC	12	-	15	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	ns
Write Pulse Width	tWP	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

PACKAGE DIMENSIONS

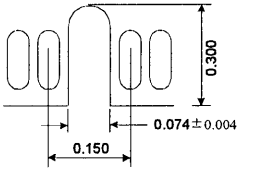
Units : Inches

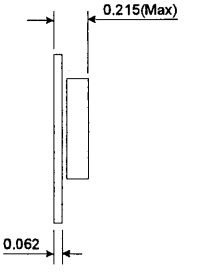


Gold Plating Lead



Detail of A





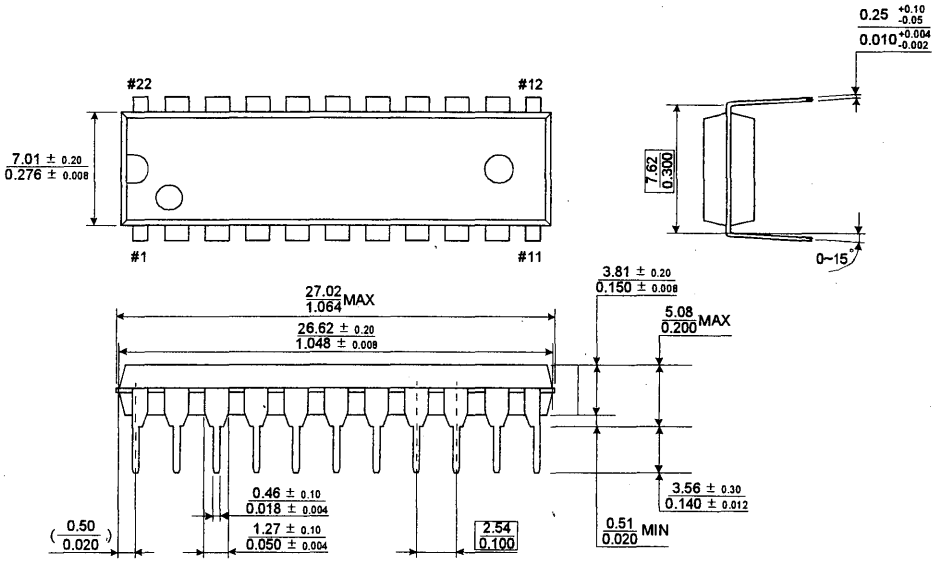
Tolerances : ±0.005 unless otherwise specified

Package Dimensions 3

PACKAGE DIMENSIONS

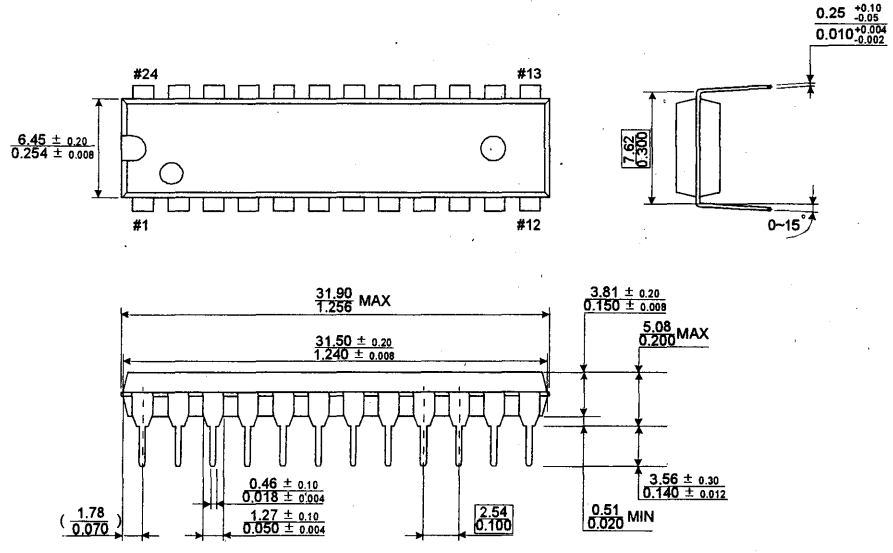
22-DIP-300B

Units : millimeters (Inches)



24-DIP-300

Units : millimeters (Inches)

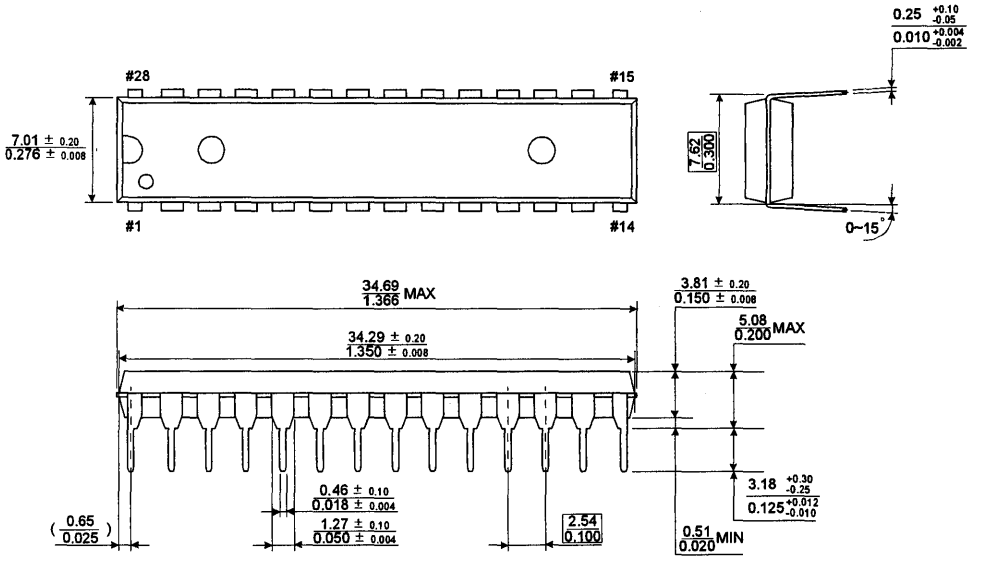


SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS

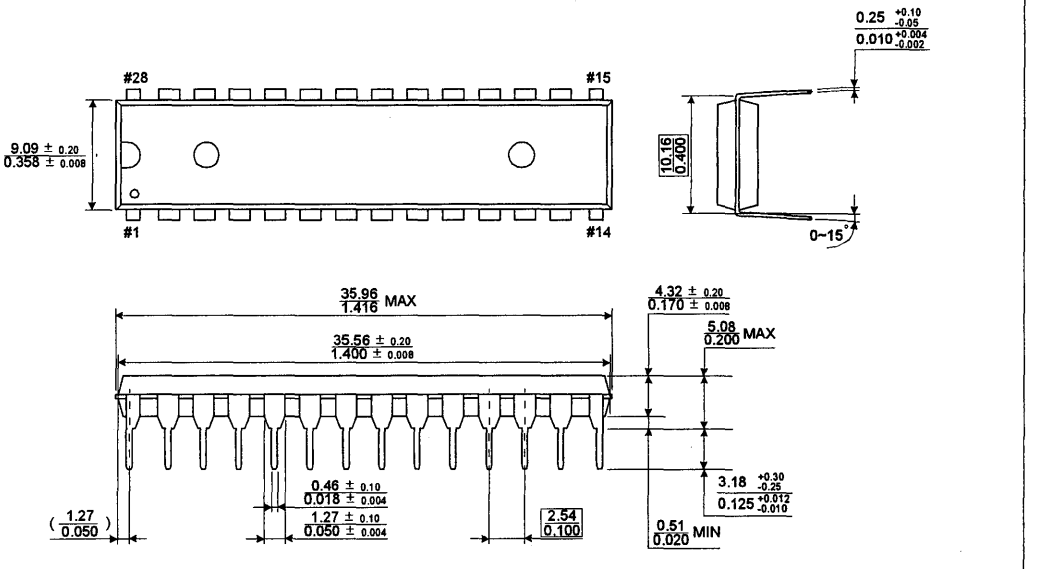
28-DIP-300

Units : millimeters (Inches)



28-DIP-400

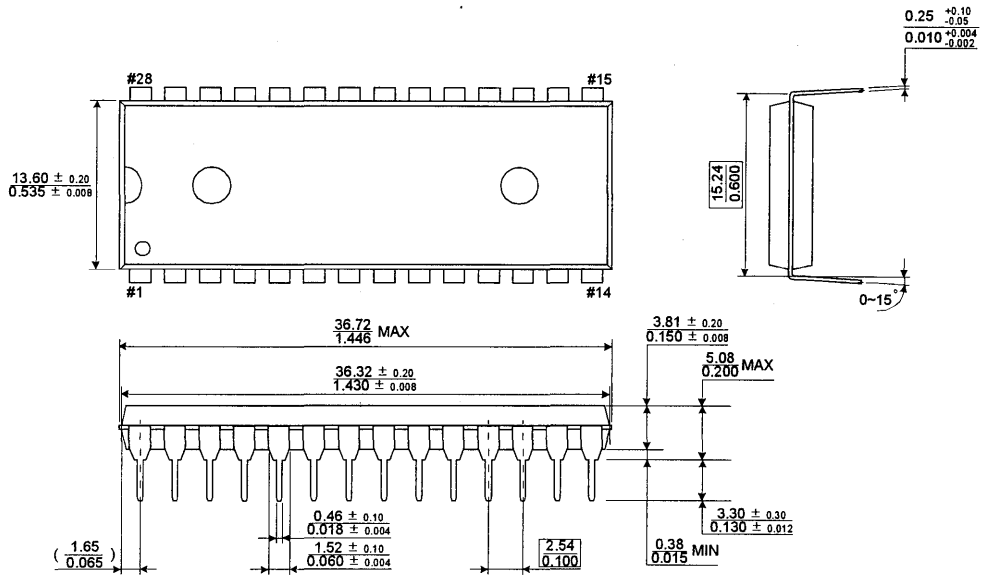
Units : millimeters (Inches)



PACKAGE DIMENSIONS

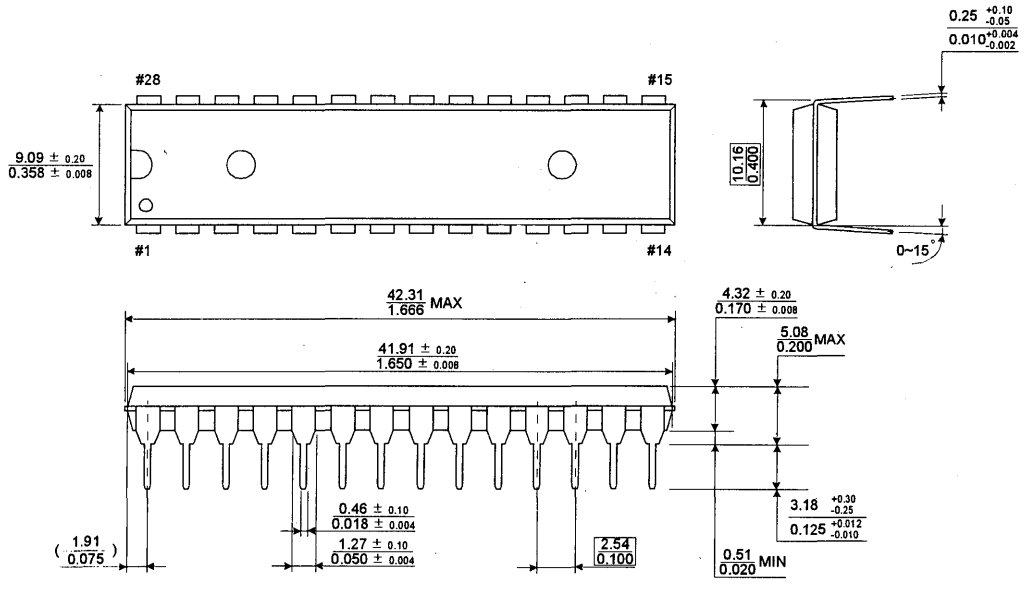
28-DIP-600B

Units : millimeters (Inches)



32-DIP-400

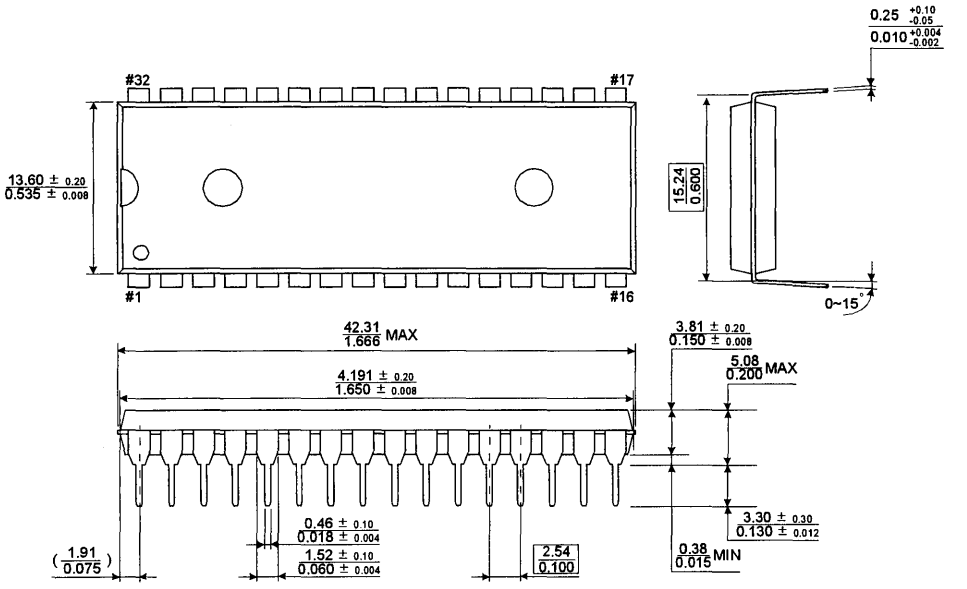
Units : millimeters (Inches)



PACKAGE DIMENSIONS

32-DIP-600

Units : millimeters (Inches)



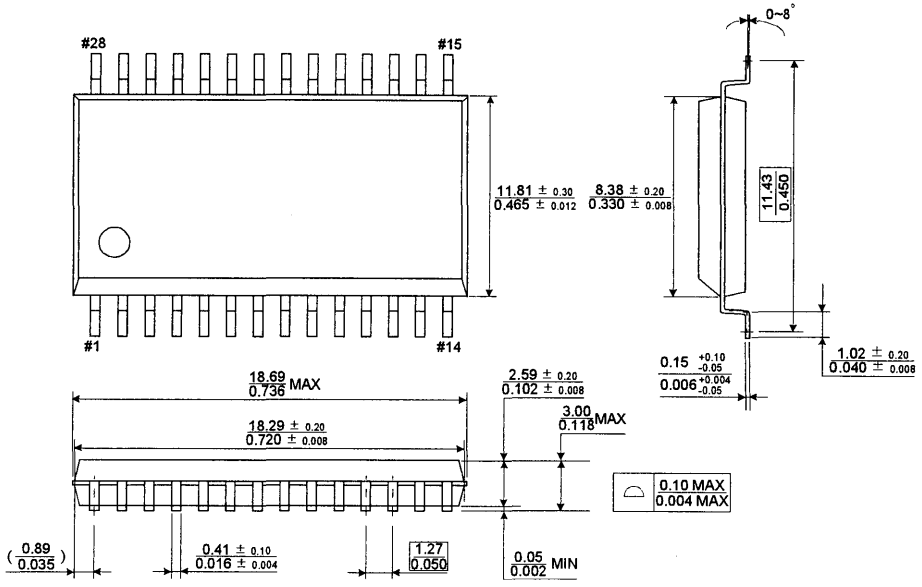
Units : millimeters (Inches)

SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS

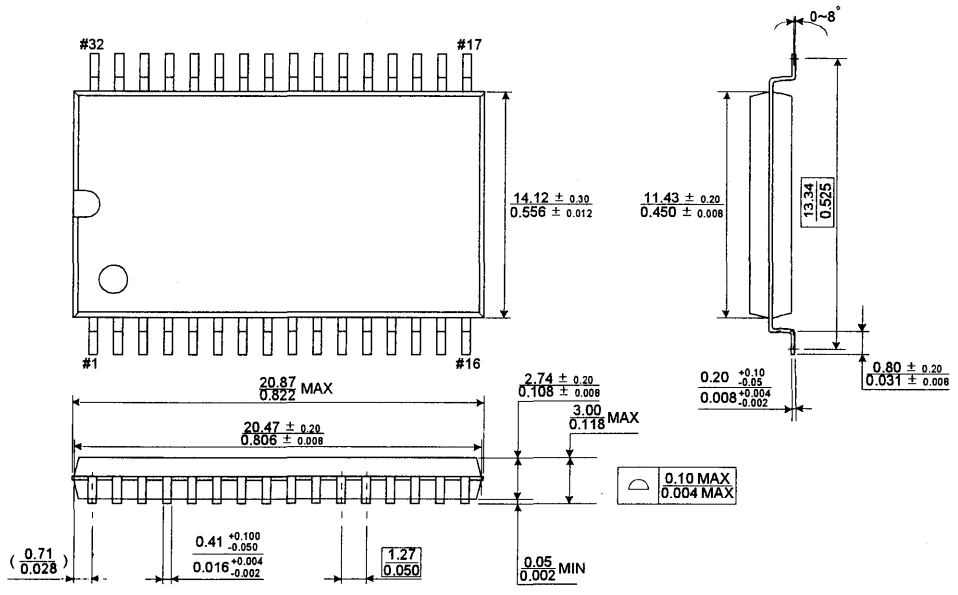
28-SOP-450

Units : millimeters (Inches)



32-SOP-525

Units : millimeters (Inches)



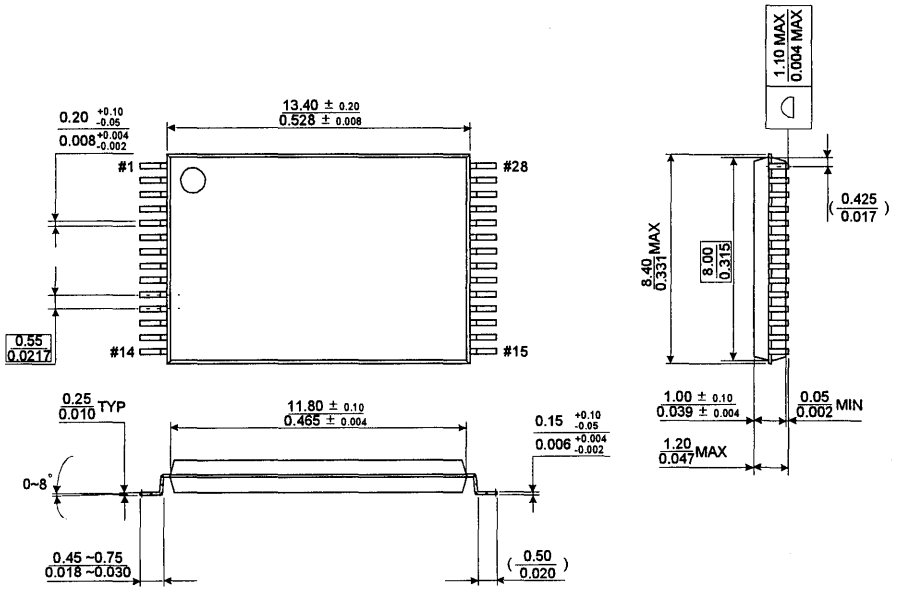
3

SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS

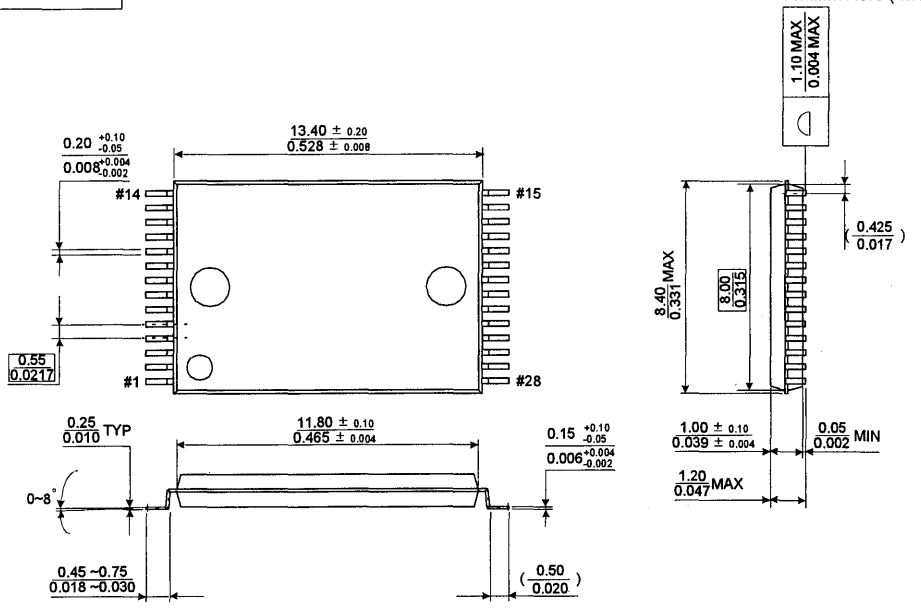
28-TSOP1-0813.4F

Units : millimeters (Inches)



28-TSOP1-0813.4R

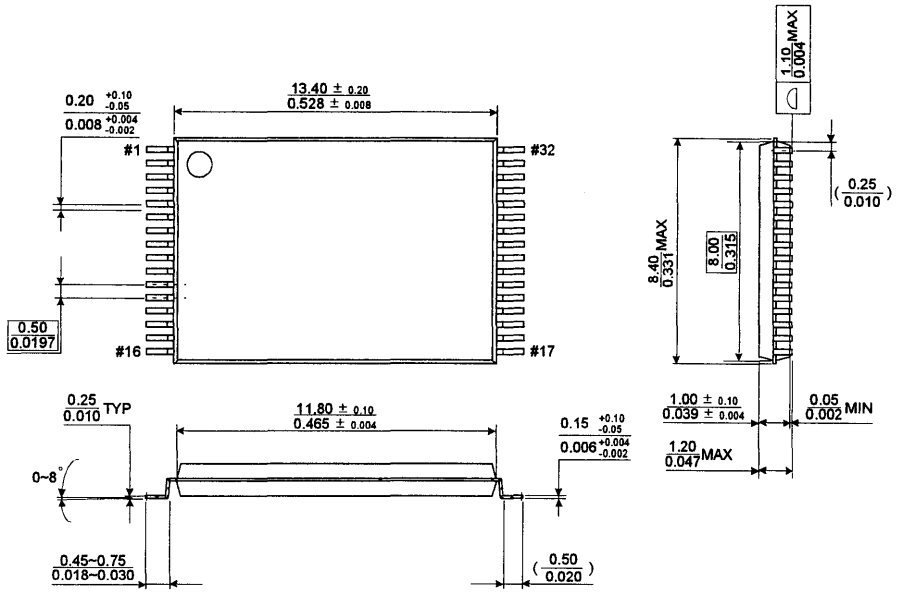
Units : millimeters (Inches)



PACKAGE DIMENSIONS

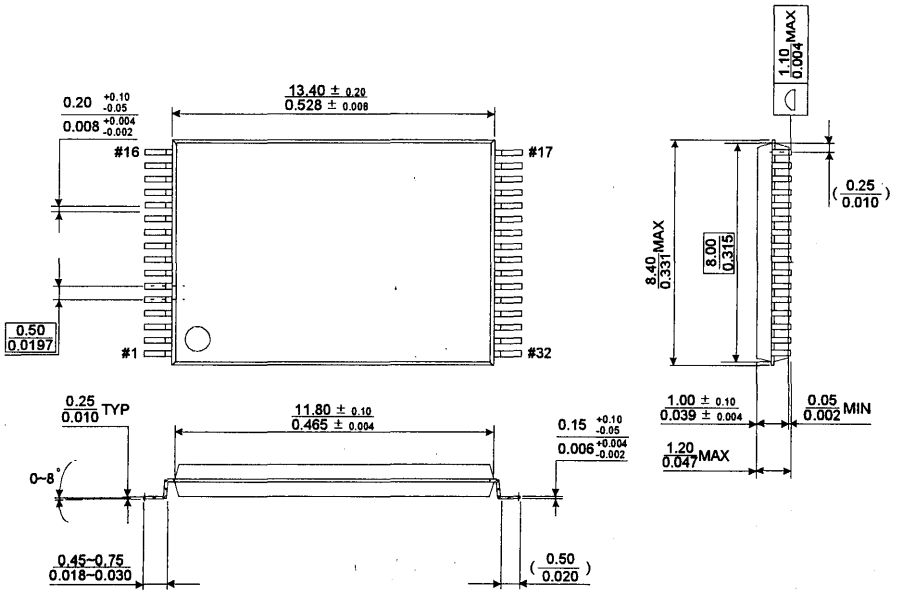
32-TSOP1-0813.4F

Units : millimeters (Inches)



32-TSOP1-0813.4R

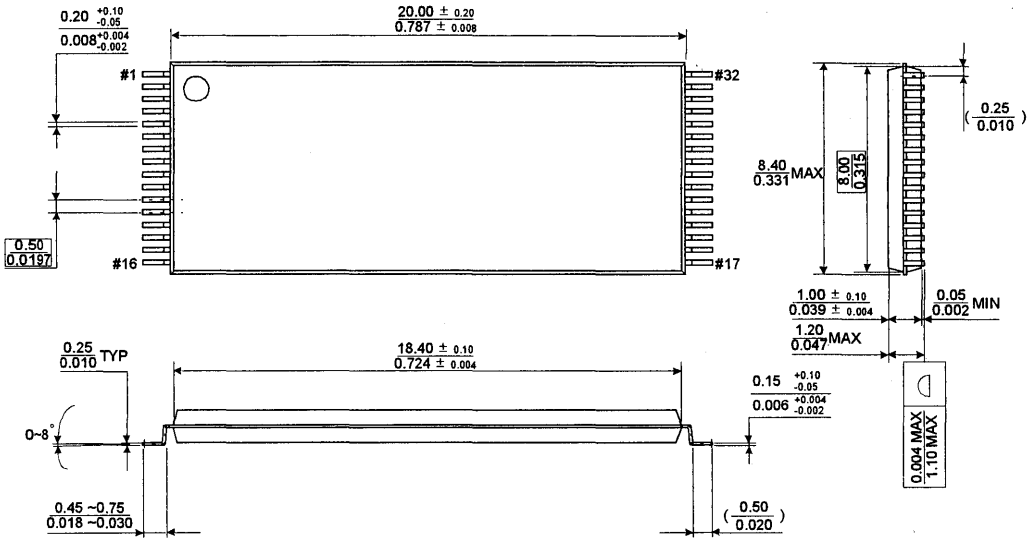
Units : millimeters (Inches)



PACKAGE DIMENSIONS

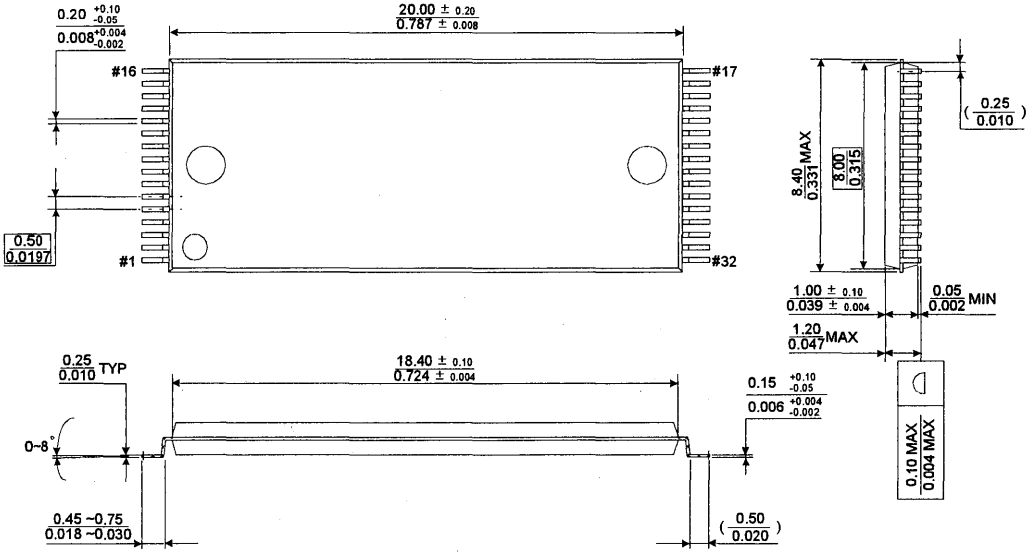
32-TSOP1-0820F

Units : millimeters (Inches)



32-TSOP1-0820R

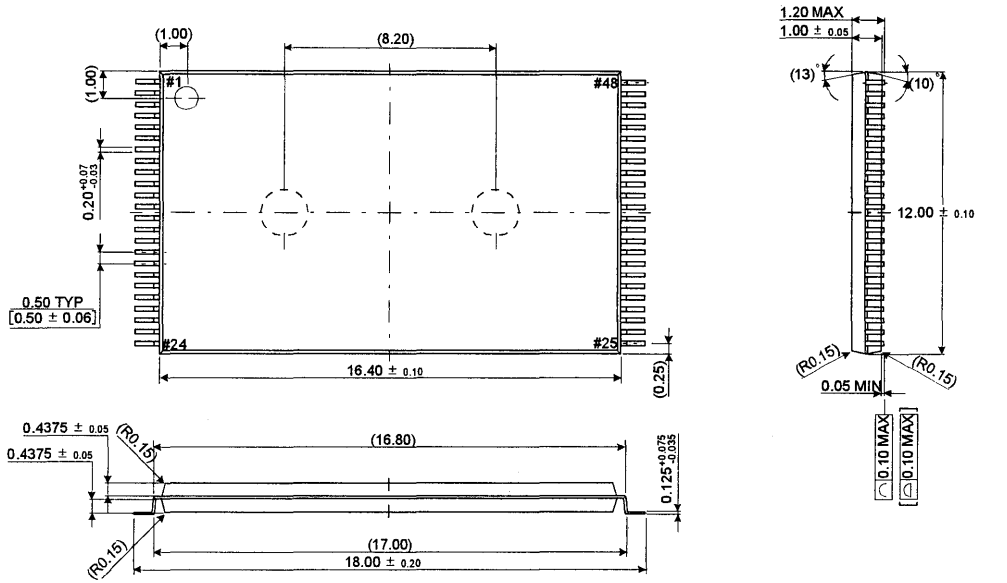
Units : millimeters (Inches)



PACKAGE DIMENSIONS

48-TSOP1-1218F

Units : millimeters (Inches)

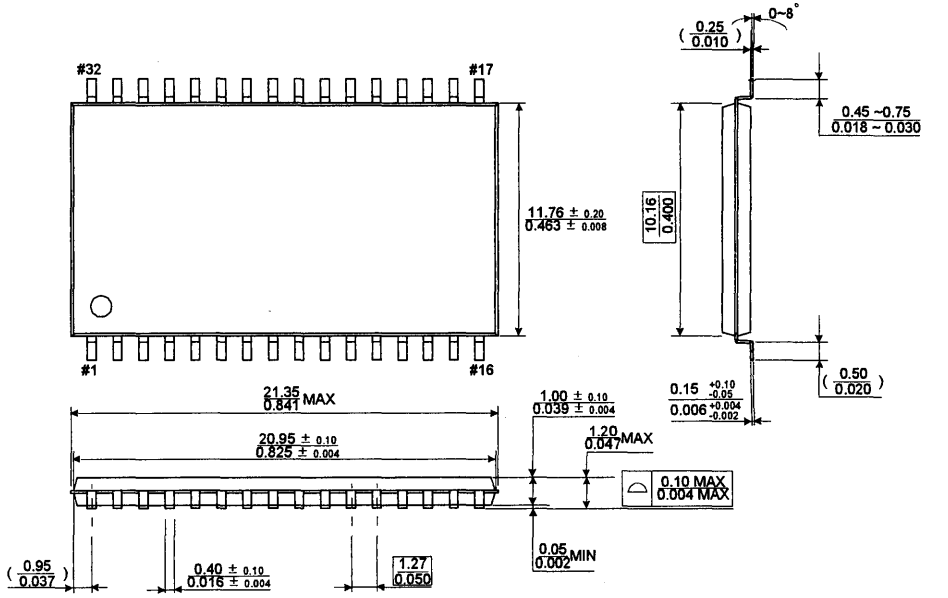


Units : millimeters (Inches)

PACKAGE DIMENSIONS

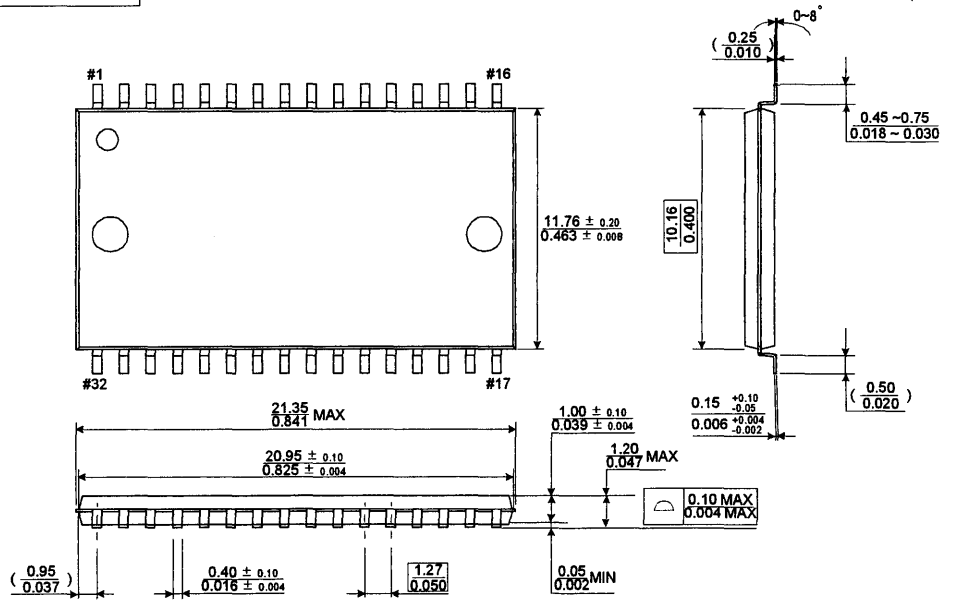
32-TSOP2-400F

Units : millimeters (Inches)



32-TSOP2-400R

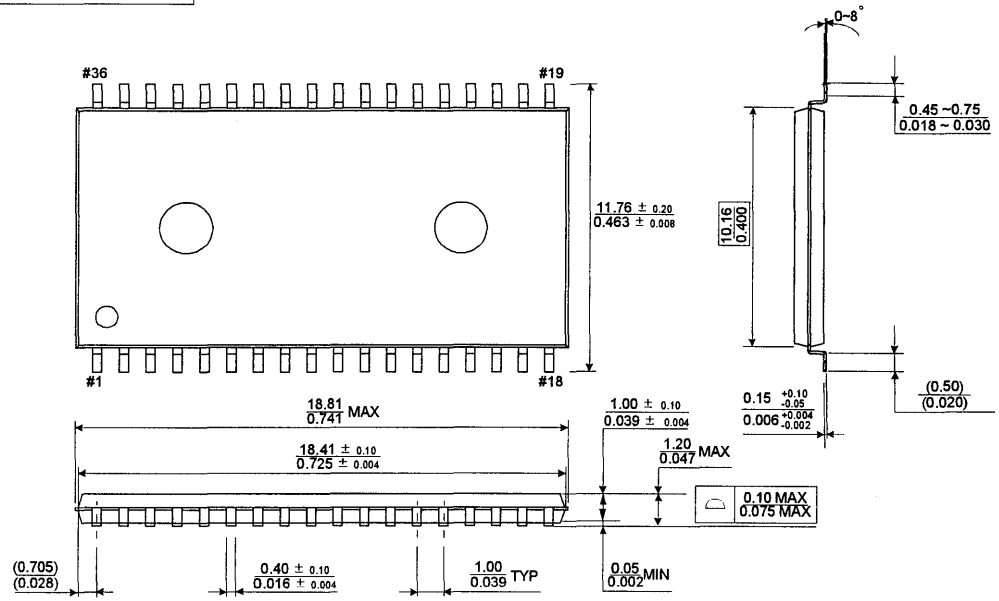
Units : millimeters (Inches)



PACKAGE DIMENSIONS

36-TSOP2-400F

Units : millimeters (Inches)

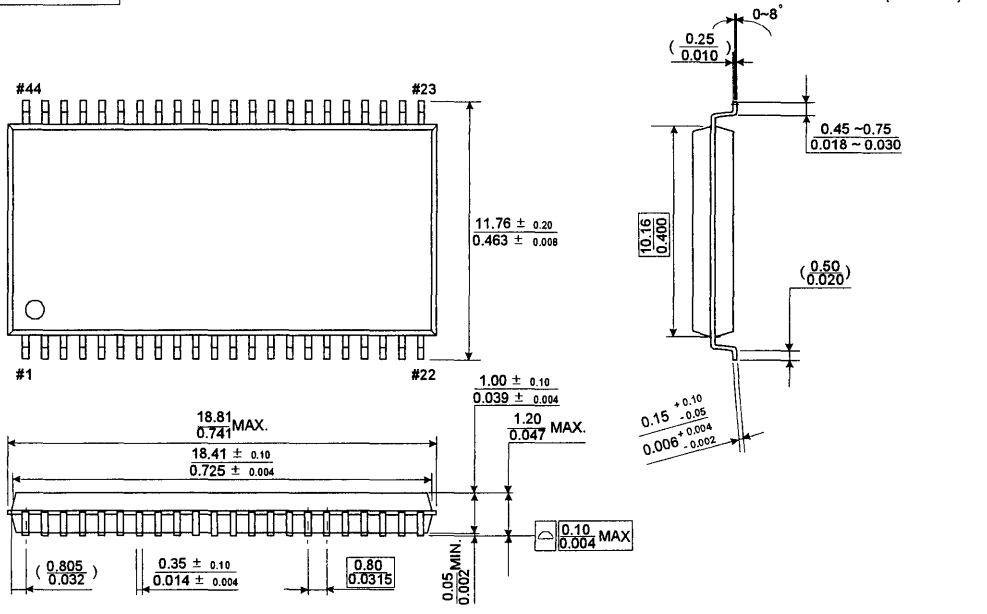


Units : millimeters (Inches)

PACKAGE DIMENSIONS

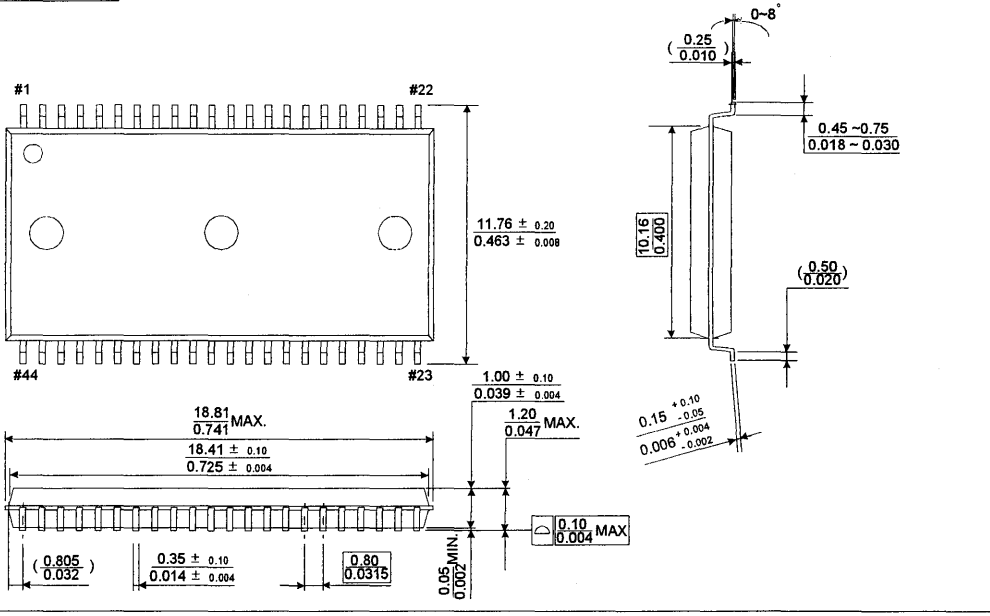
44-TSOP2-400F

Units : millimeters (Inches)



44-TSOP2-400R

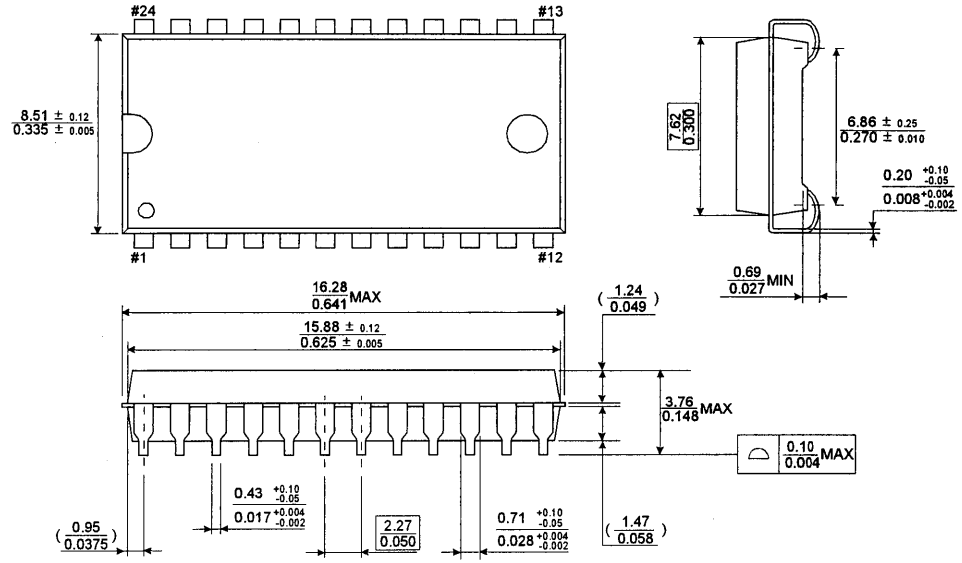
Units : millimeters (Inches)



PACKAGE DIMENSIONS

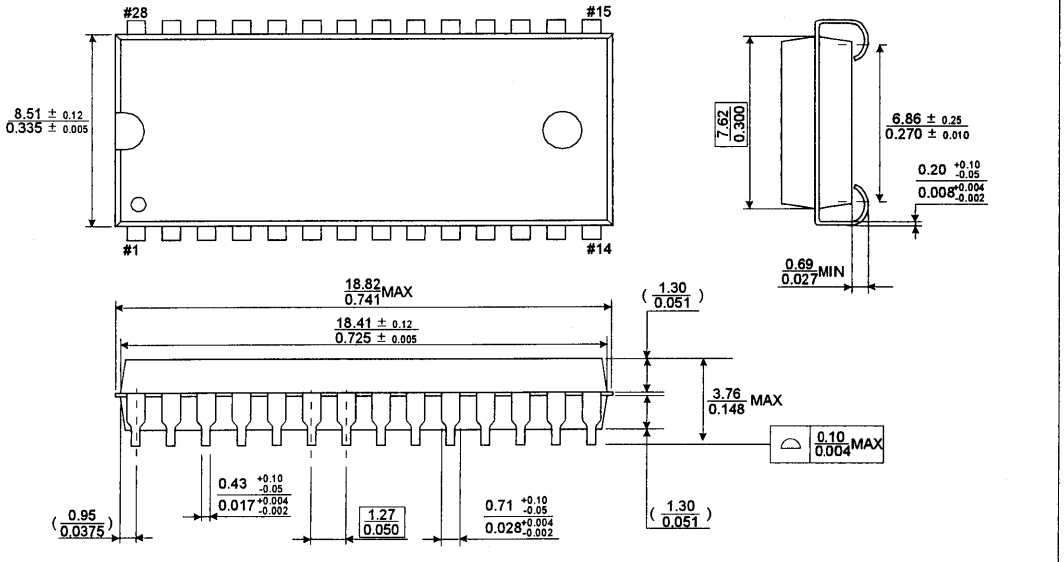
24-SOJ-300

Units : millimeters (Inches)



28-SOJ-300

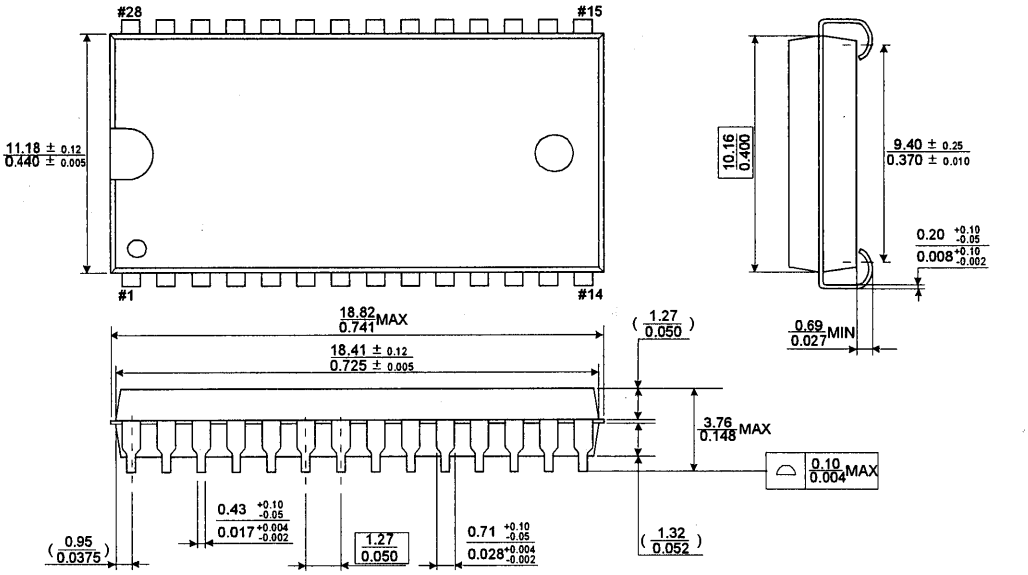
Units : millimeters (Inches)



PACKAGE DIMENSIONS

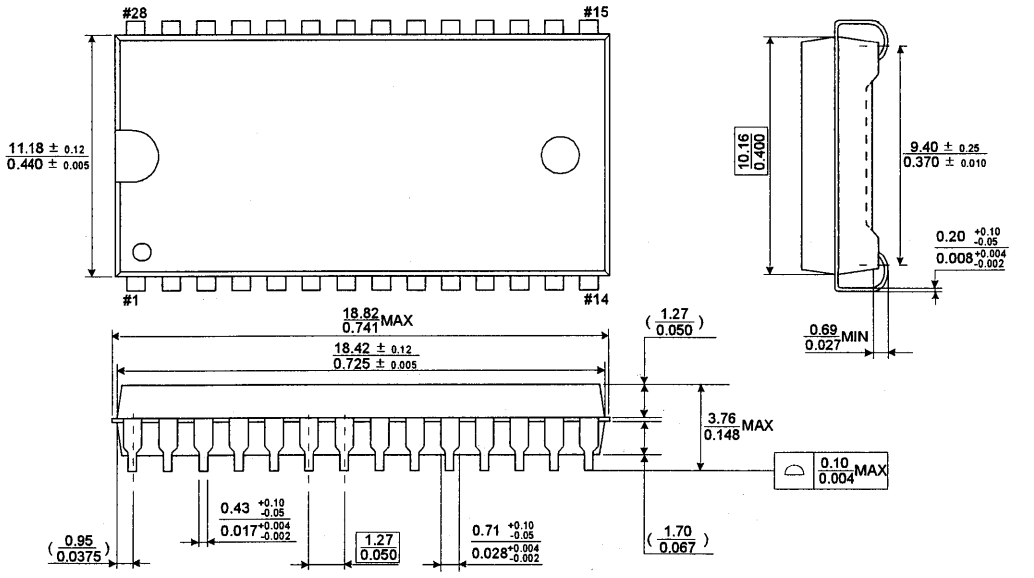
28-SOJ-400A

Units : millimeters (Inches)



28-SOJ-400B

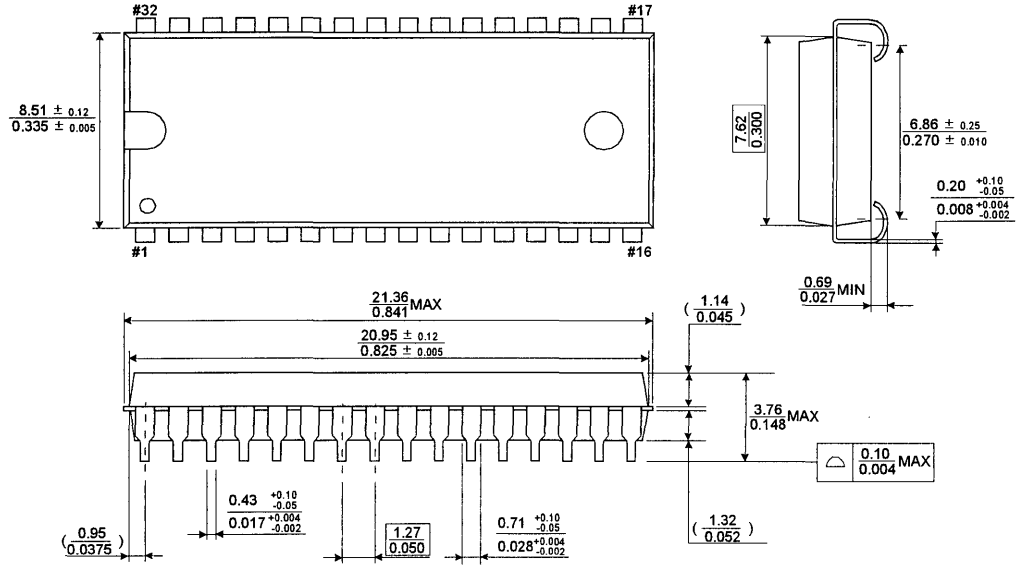
Units : millimeters (Inches)



PACKAGE DIMENSIONS

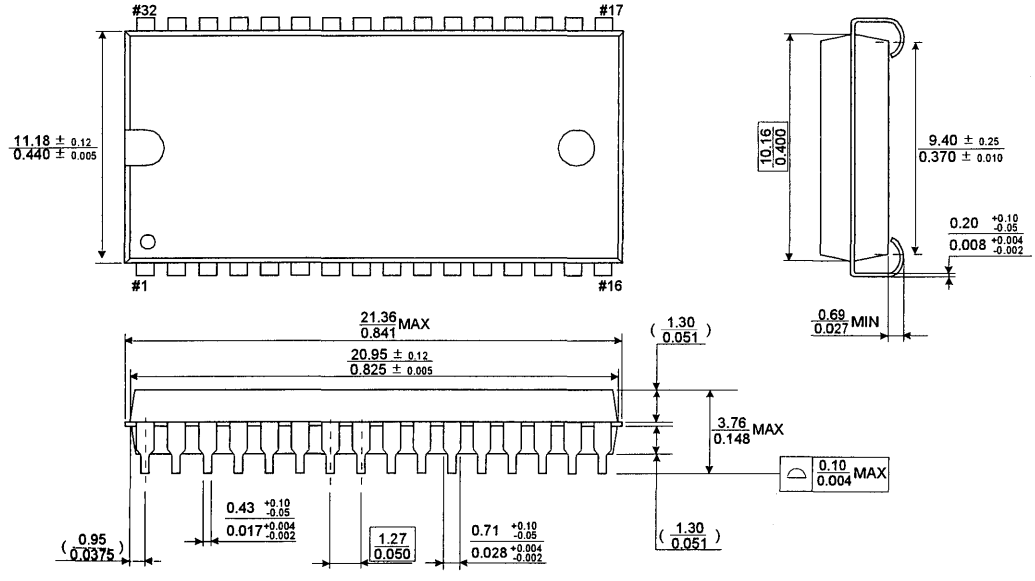
32-SOJ-300

Units : millimeters (Inches)



32-SOJ-400

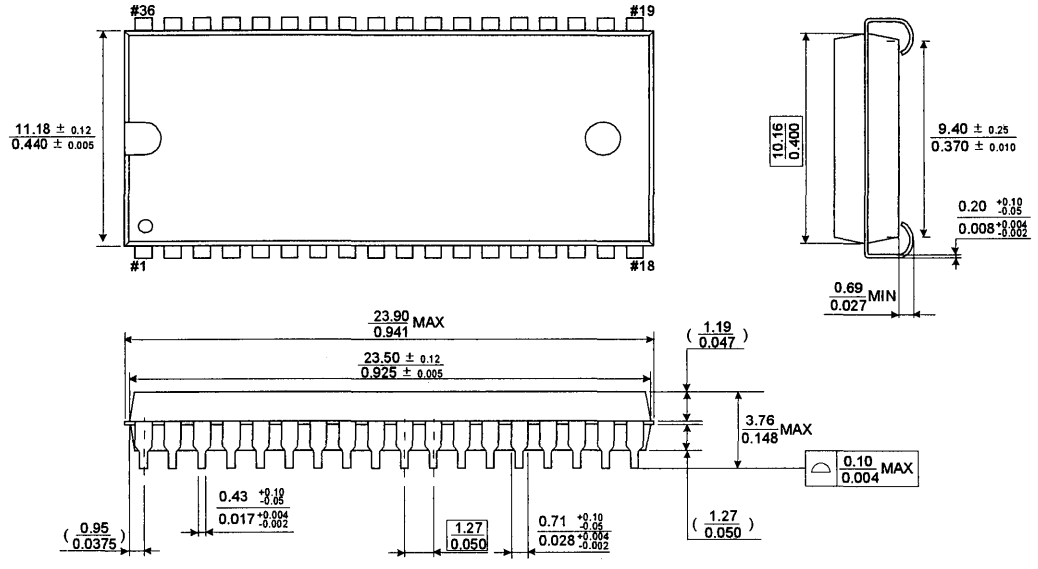
Units : millimeters (Inches)



PACKAGE DIMENSIONS

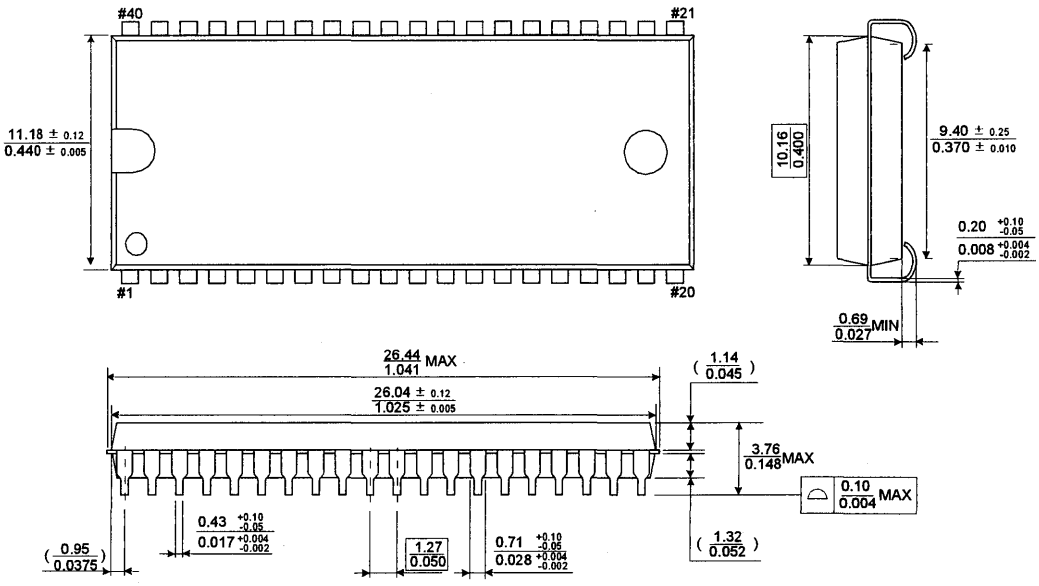
36-SOJ-400

Units : millimeters (Inches)



40-SOJ-400

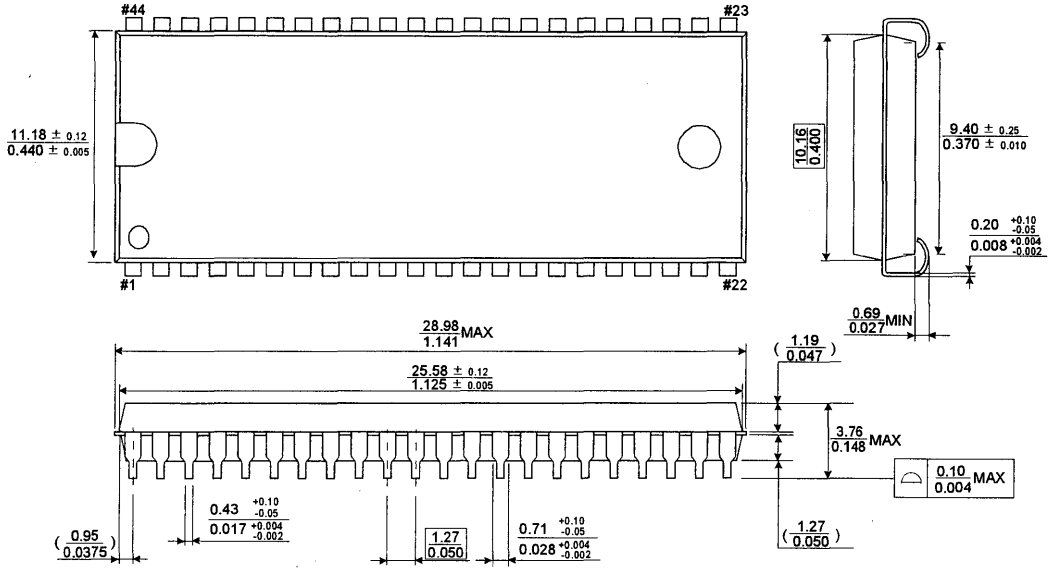
Units : millimeters (Inches)



PACKAGE DIMENSIONS

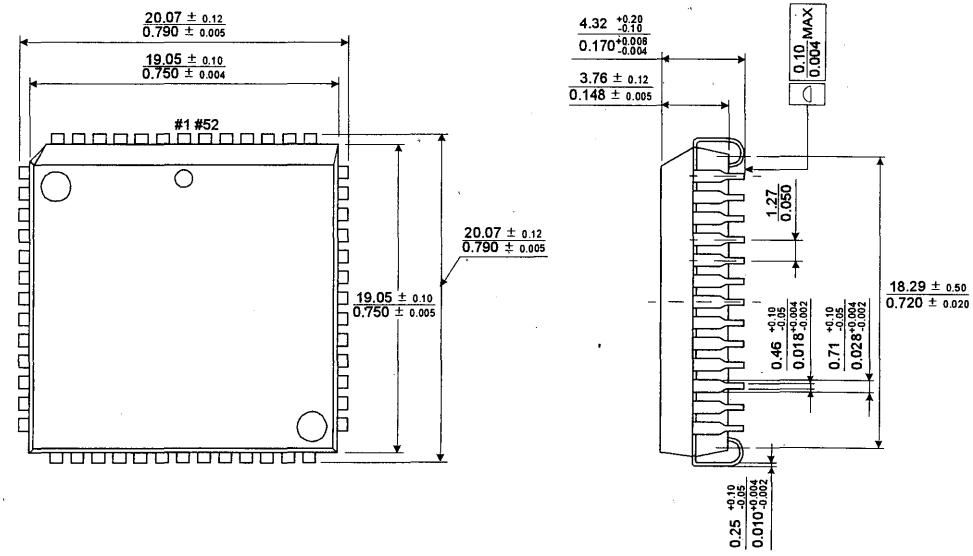
44-SOJ-400

Units : millimeters (Inches)



52-PLCC-SQ.

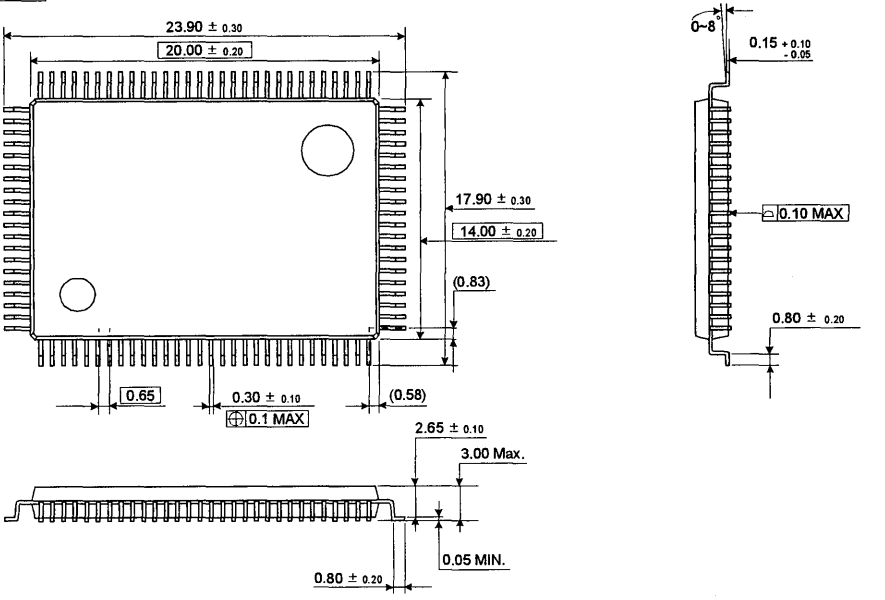
Units : millimeters (Inches)



PACKAGE DIMENSIONS

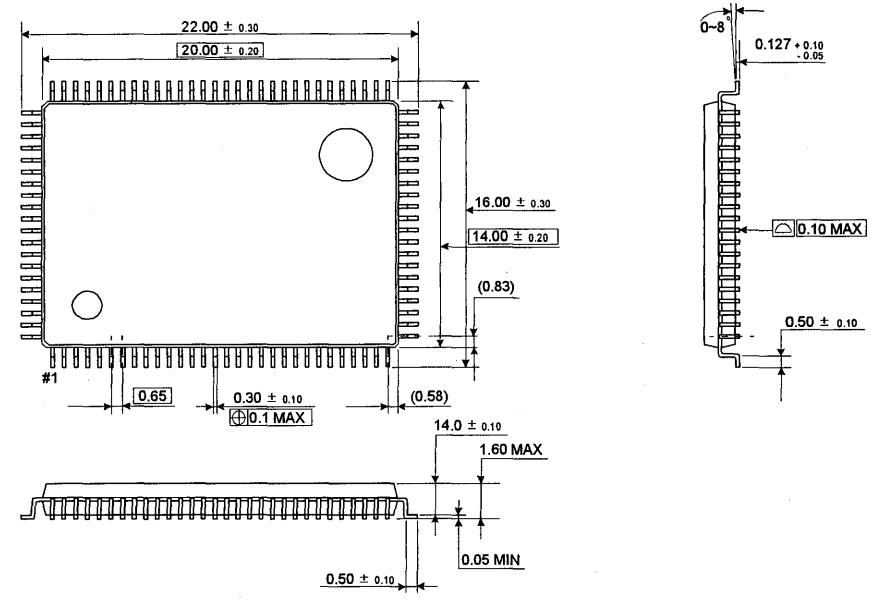
100-QFP-1420C

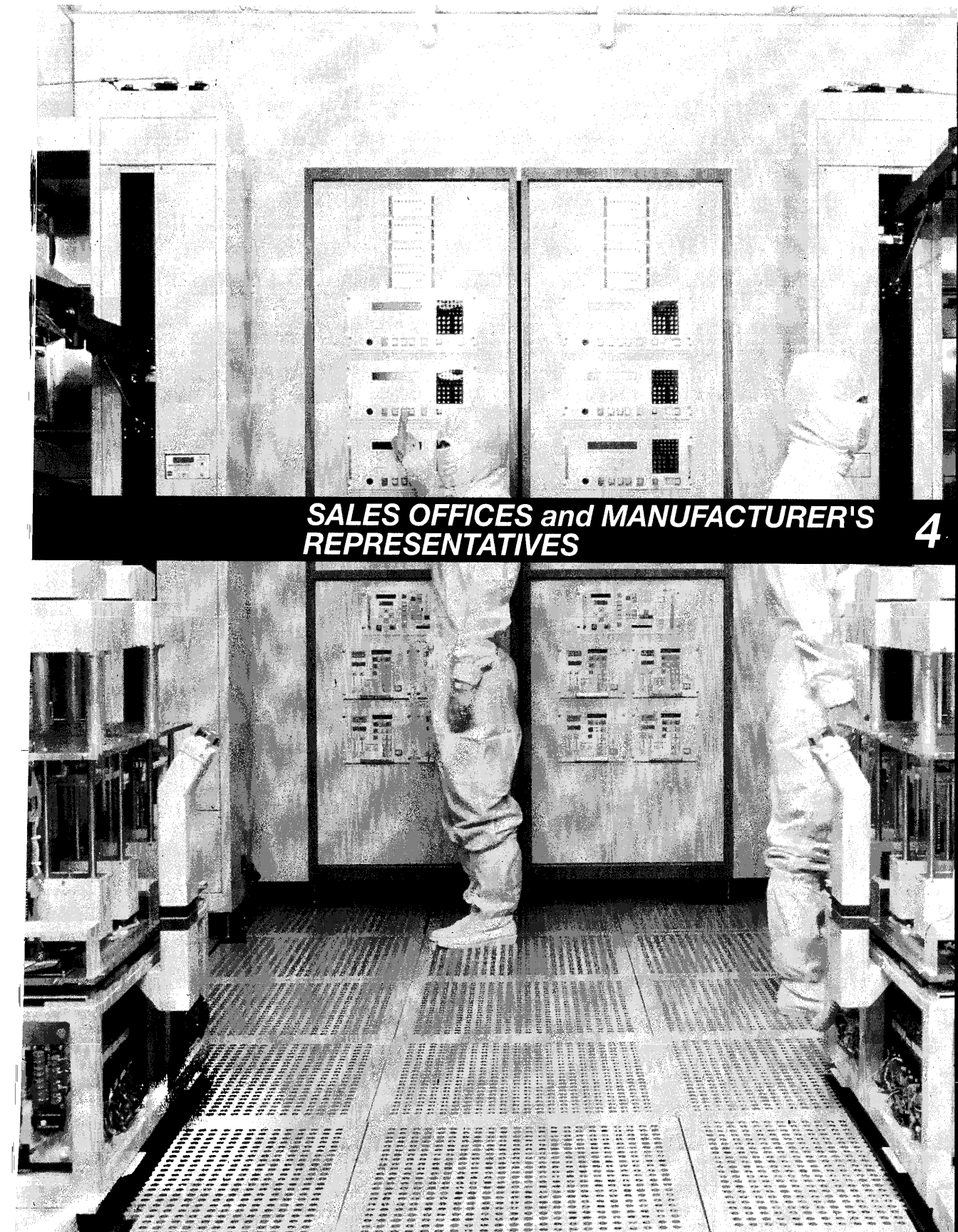
Units : millimeters (Inches)



100-TQFP-1420A

Units : millimeters (Inches)





SALES OFFICES and MANUFACTURER'S REPRESENTATIVES

4

SAMSUNG SEMICONDUCTOR SALES OFFICE-U.S.A.

Northwest
3655 North First Street
San Jose, CA 95134
TEL : 408-954-7000
FAX : 408-954-7883

Southwest
7700 Irvine Center Drive
Suite #150, Irvine, CA 92718
TEL : 714-753-7530
FAX : 714-753-7544

7037 Financial Drive
Mississauga, Ontario
Canada L5N 6R3
TEL : 905-819-5109
FAX : 905-819-5122

North Central
300 Park Boulevard, Suite #210
Itasca, IL 60143-2636
TEL : 630-775-1050
FAX : 630-775-1058

South Central
15770 Dallas Pkwy, Suite #777
Dallas, TX 75248
TEL : 972-385-1114
FAX : 972-385-1173

8303 Mopac Blvd. Suite #A100
Austin, TX 78759
TEL : 512-342-1904
FAX : 512-342-1915

20405 SH 249, Suite 370,
Houston, TX 77070
TEL : 713-376-2191
FAX : 713-376-2192

Northeast
238 Littleton Rd. Suite 201
Westford, MA 01886
TEL : 508-392-2220
FAX : 508-392-2240

300 Westage Bus. Ctr, Suite 295
Fishkill, NY 12524
TEL : 914-897-7777
FAX : 914-897-7780

Southeast
2000 Regency Pkwy, Suite #285
Cary, NC 27511
TEL : 919-380-8483
FAX : 919-380-8492

190 Lime Quarry Road, Suite 205,
Madison, AL 35758
TEL : 205-772-7050
FAX : 205-772-8844

4

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

ALABAMA
REP ONE
2707 Artie Street, Bldg 200 — TEL : 205-539-7371
Suite 12, Huntsville, AL 35805 — FAX : 205-533-4509

ARIZONA
SUMMIT SALES
7802 E. Gray Rd. Suite #600 — TEL : 602-998-4850
Scottsdale, AZ 85260 — FAX : 602-998-5274

CALIFORNIA
BESTRONICS
9683 Tierra Grande Street — TEL : 619-693-1111
Suite #102, San Diego, CA 92126 — FAX : 619-693-1963
I-SQUARED
3255-1 Scott Blvd, Suite 102 — TEL : 408-988-3400
Santa Clara, Ca 95054 — FAX : 408-988-2079
I-SQUARED
9198 Greenback Lane, Suite 214 — TEL : 916-989-0843
Orangevale, Ca 95662 — FAX : 916-989-2841
WESTAR
15265 Alton Parkway, — TEL : 714-453-7900
Suite #400, Irvine, CA 92718 — FAX : 714-453-7930
WESTAR
26500 Agoura Rd., Suite #204 — TEL : 818-880-0594
Calabasas, CA 91302 — FAX : 818-880-5013

CANADA
InTELaTECH. INC
5225 Orbitor Drive, Suite 2 — TEL : 905-629-0082
Mississauga, Ontario — FAX : 905-629-1795
Canada L4W 4Y8

InTELaTECH. INC
300 3665 Kings Way — TEL : 604-434-5699
Vancouver, B.C. V5R 5W2 — FAX : 604-434-5655
InTELaTECH. INC
6765 Cote De Liesse, Suite #366, — TEL : 514-343-4877
St. Laurent, Quebec — FAX : 514-343-4355
Canada H4T 1E5

COLORADO
FRONT RANGE MARKETING, INC.
3100 Arapahoe Road, #404 — TEL : 303-443-4780
Boulder, CO 80303 — FAX : 303-447-0371

FLORIDA
DYNE-A-MARK CORPORATION
500 Winderley Place — TEL : 407-660-1661
Suite #100, Maitland, FL 32751 — FAX : 407-660-9407
DYNE-A-MARK CORPORATION
742 Penguin Avenue NE — TEL : 407-725-7470
Palm Bay, FL 32905 — FAX : 407-984-2718
DYNE-A-MARK CORPORATION
Two Prospect Park Business Ctr, — TEL : 954-485-3500
3351 N.W. 55th Street — FAX : 954-485-6555
Fort Lauderdale, FL 33309
DYNE-A-MARK CORPORATION
508 Palm Drive — TEL : 813-586-3778
Largo, FL 34640 — FAX : 813-586-3863

GEORGIA
SOUTH ATLANTIC COMPONENT SALES
728 Holcomb Bridge Rd, — TEL : 770-447-6154
Norcross, GA 30071 — FAX : 770-447-6714

ILLINOIS

DAVIX INTERNATIONAL LTD.
1655 N. Arlington Heights RD. TEL : 847-259-5300
Suite #204 East, Arlington Heights, FAX : 847-259-5428
IL 60004

IDAHO

INTERMOUNTAIN TECH
1310 East First Street TEL : 208-888-6071
Meridian, Idaho 83642 FAX : 208-888-6074

INDIANA

GEN II MARKETING
1415 Magnavox Way, #130 TEL : 219-436-4485
Ft, Wayne, IN 46804 FAX : 219-436-1977

GEN II MARKETING
31 E. Main Street TEL : 317-848-3083
Carmel, IN 46032 FAX : 317-848-1264

KANSAS

CUSTOMER 1ST
10540 Marty #200N TEL : 913-385-0390
Overland Park, KS 66212` FAX : 612-851-7907

KENTUCKY

GEN II MARKETING
861 Corporate Drive, Suite 210 TEL : 606-223-9181
Lexington, KY 40503 FAX : 606-223-2864

MARYLAND

BEACON NORTH
8965 Guilford Road TEL : 410-381-4309
Columbia, MD 21046 FAX : 410-381-4752

BESCON NORTH
2821 Sommersby Road TEL : 301-831-5492
Mt. Airy, MD 21771 FAX : 301-829-2167

MASSACHUSETTS

NEW TECH SOLUTIONS
1 Van de Graaff Drive 4th Drive TEL : 617-229-8888
Burlington, MA 01803 FAX : 617-229-1614

MICHIGAN

GEN II MARKETING
4849 Gallagher Road TEL : 810-231-0004
Whitmore Lake, MI 48189 FAX : 810-231-0009

MINESOTA

CUSTOMER 1ST
2950 Metro Drive, Suite #101 TEL : 612-851-7909
Bloomington, MN 55425 FAX : 612-851-7907

NORTH CAROLINA

SOUTH ATLANTIC COMPONENT SALES
211 Commonwealth Court TEL : 919-380-1133
Cary, NC 27511 FAX : 919-380-0801

SOUTH ATLANTIC COMPONENT SALES
5200 Park Road, STE. 103 TEL : 704-525-0510
Charlotte, NC 28209 FAX : 704-525-9714

NEW YORK

NECCO
255 Executive Dr, Suite #211 TEL : 516-349-1600
Plainview, NY 11803 FAX : 516-349-1343

T-SQUARED
7353 Victor-Pittsford Road TEL : 716-924-9101
Victor, NY 14564 FAX : 716-924-4946

T-SQUARED
4226 Bayview Rd, TEL : 716-824-6508
Blasdell, NY 14219 FAX : 716-824-3484

T-SQUARED
1790 Pennsylvania Avenue TEL : 607-625-3983
Apalachin, NY 13732 FAX : 607-625-5294

OREGON

ADVANCED TECH MKTG, INC
4900 SW Griffith Drive, Suite #155 TEL : 503-643-8307
Beaverton, OR 97005 FAX : 503-643-4364

INTERMOUNTAIN TECH
1730 SW Skyline Blvd. TEL : 503-291-0360
Suite #226, Portland, OR 97221 FAX : 503-291-0362

OHIO

BAILEY, J.N. & ASSOC.
503 Windsor Park DR. TEL : 513-291-1354
Centerville, OH 45459 FAX : 513-291-9023

BAILEY, J.N. & ASSOC.
288 Crackel RD, TEL : 216-543-6988
Aurora, OH 44202 FAX : 216-543-6985

BAILEY, J.N. & ASSOC.
3591 Milton Avenue TEL : 614-262-7274
Columbus, OH 43214 FAX : 614-262-0384

BAILEY, J.N. & ASSOC.
1638 Longwood AVE, TEL : 216-605-0410
Cleveland, Oh 44124 FAX : 216-605-0411

PENNSYLVANIA

CMS SALES & MARKETING INC.
521 Plymouth Road, Suite #111 TEL : 610-834-6840
Plymouth Meeting, PA 19462 FAX : 610-834-6848

PUERTO RICO

DIGIT-TECH
P.O.BOX 1945 TEL : 787-892-4260
Calle DR, Veve #59 Altos FAX : 787-892-3366
San German, Puerto Rico 00683

UTAH

FRONT RANGE MARKETING INC.
448 East 6400 South, Suite 280 TEL : 801-288-2500
Murray, UT 84107 FAX : 801-288-2505

VIRGINIA

BEACON NORTH
21607 Goodwin Court TEL : 703-855-8235
Ashburn, VA 22011 FAX : 703-724-4033

BEACON NORTH
1324 Gristmill Drive TEL : 804-296-6245
Charlottesville, VA 22902 FAX : 804-296-6273

WASHINGTON

ADVANCED TECH MKTG, INC

8521 154th AVE, NE	TEL : 206-869-7636
Redmond, WA 98052	FAX : 206-869-9841

WISCONSIN

DAVIX INTERNATIONAL LTD.

N84 W15787 Menomonee AVE.	TEL : 414-255-1600
Menomonee Falls, WI 53051	FAX : 414-255-1863

TEXAS

VIELOCK ASSOC.

555 Repulic Drive, suite 105	TEL : 972-881-1940
Plano, TX 75074	FAX : 972-423-8556

VIELOCK ASSOC.

9811 Anderson Mill Road, #201	TEL : 512-918-1189
Austin, TX 78750	FAX : 512-918-1199

VIELOCK ASSOC.

10700 Richmond Ave, STE. #108	TEL : 713-974-3287
Houston, TX 77042	FAX : 713-974-3289

ADELSA McALLEN OFFICE

2303 E. 21st Street	TEL : 210-585-8659
Mission, TX 78572	FAX : 210-519-4976

MEXICO

ADELSA HEADQUARTERS

Club Cuicacalli #66	TEL : 525-374-0981
Cto. Cronistas, Zona Azunl,	FAX : 525-374-0997
Cd Satelite, CP 53100 Naucalpan,	
Edo, de Mexico	

ADELSA Guadalajara OFFICE

Otranto No. 3080-2, Providencia	TEL : 5236-420-865
Guadalajara, Jalisco MEX 44630	FAX : 5236-419-465

ADELSA Cd.Juarez OFFICE

Jardin Misioneros 1720	TEL : 5216-188-244
Fracc. Jardines del Seminario	FAX : 5216-188-244
C.P.32500 Cd. Juarez, Chihuahua	

ADELSA MONTEREY OFFICE

Av. Revolucio'n 3532-A	TEL : 528-387-4822
Col. Primavera	FAX : 528-387-4822
Monterey, Nuevo Leon MEX 64830	

• • • • •

SAMSUNG SEMICONDUCTOR INC. DISTRIBUTORS-U.S.A.

ALABAMA

ADVENT
4717 University DR., #107 TEL : 205-830-6669
Huntsville, AL 35816 FAX : 205-830-5585

ALL AMERICAN
4590 Corporate DR., #115D TEL : 205-837-1555
Huntsville, AL 35805 FAX : 205-837-7733

BELL INDUSTRIES
555 Sparkmen Drive, STE. 600D TEL : 205-430-3150
Huntsville, AL 35816 FAX : 205-430-3160

MILGRAY
8215 Highway 20 West TEL : 205-464-8646
Madison, AL 35805 FAX : 205-464-8655

ARIZONA

ALL AMERACAN
4636 E. University DR., #155 TEL : 602-966-0006
Phoenix, AZ 85034 FAX : 602-966-0007

BELL INDUSTRIES
10611 N. Hayden Rd. STE. D-103 TEL : 602-905-2355
Scottsdale, AZ 85260 FAX : 602-905-2356

JACO
2432 W. Peoria AVE, #1344 TEL : 602-906-4004
Phoenix, AZ 85029 FAX : 602-906-4054

MILGRAY
410 North 44th Street, STE #150 TEL : 602-914-4240
Phoenix, AZ 85008 FAX : 602-914-4241

CALIFORNIA

ALL AMERICAN
26010 Mureau RD., #120 TEL : 818-878-0555
Calabasas, CA 91302 FAX : 818-878-0533

ALL AMERICAN
10805 Holder ST., #100 TEL : 714-229-8600
Cypress, CA 90630 FAX : 714-229-8603

ALL AMERICAN
6390 Greenwich DR., #170 TEL : 619-658-0200
San Diego, CA 92122 FAX : 619-658-0201

ALL AMERICAN
230 Devcon DR., TEL : 408-441-1300
San Jose, CA 95112 FAX : 408-437-8970

ALL AMERICAN
14192 Chambers RD. TEL : 714-573-5000
Tustin, CA 92780 FAX : 714-573-5050

ALL AMERICAN
111. S. Court ST., #104 TEL : 209-734-8861
Visalia, CA 93291 FAX : 209-734-8865

BELL INDUSTRIES
11812 San Vicente BLVD., STE. 300 TEL : 310-447-6312
Los Angeles, CA 90049 FAX : 310-826-1534

BELL INDUSTRIES
220 Technology DR., STE. 100 TEL : 714-727-4500
Irvine, CA 92718 FAX : 714-453-4610

BELL INDUSTRIES
5520 Ruffin RD., STE. 103 TEL : 619-576-3290
San Diego, CA 92123 FAX : 619-492-9826

BELL INDUSTRIES
125 Auburn Court, STE. 110 TEL : 805-373-5600
Westlake Village, CA 91362 FAX : 805-496-7340

BELL INDUSTRIES
1161 North Fairoaks AVE, TEL : 408-734-8570
Sunnyvale, CA 94089 FAX : 408-734-8875

BELL INDUSTRIES
3001 Douglas BLVD, STE. 205 TEL : 916-781-8070
Roseville, CA 95661 FAX : 916-781-2954

IEC
9940 Business Park DR., 145 TEL : 916-363-6030
Sacramento, CA 95827 FAX : 916-362-6926

JACO
1610-A Berryessa Road, TEL : 408-928-1600
San Jose, CA 95134 FAX : 408-928-1616

JACO
1541 Parkway Loop, #A TEL : 714-258-9003
Tustin, CA 92680 FAX : 714-258-1909

JACO
2282 Townsgate Rd., TEL : 805-495-9998
Westlake Village, CA 91361 FAX : 805-494-3864

MILGRAY
2880 Zanker RD., STE #102 TEL : 408-456-0900
San Jose, CA 95134 FAX : 408-456-0300

MILGRAY
275 E. Hillcrest Drive, STE #145 TEL : 805-371-9399
Thousand Oaks, CA 91360 FAX : 805-371-9317

MILGRAY
25 Mauchly, STE #329 TEL : 714-753-1282
Irvine, CA 92718 FAX : 714-753-1682

MILGRAY
6835 Flanders DR., STE #300 TEL : 619-457-7545
San Diego, CA 92121 FAX : 619-457-9750

CANADA

ALL AMERICAN
6375 Dixie RD., Units 4,5 & 6 TEL : 905-670-5946
Mississauga, ON L5T2E7 FAX : 905-670-5947

MILGRAY
4185 Still Creek DR., STE #B201 TEL : 604-291-0044
Burnaby, B.C. V5C6G9, CN FAX : 604-291-9939

MILGRAY
6600 Trans Canada HWY. Suite #209 TEL : 514-426-5900
Pointe Claire, Quebec, CN H9R4S2 FAX : 514-426-5836

MILGRAY
2783 Thamesgate DR., TEL : 905-678-0958
Mississauga, Ontario, CN L4T1G5 FAX : 905-678-1213

COLORADO

ALL AMERICAN
4090 Youngfield ST., TEL : 303-422-1701
Wheatridge, CO 80033 FAX : 303-422-2529

BELL INDUSTRIES
9351 Grant Street, STE. 460 TEL : 303-280-1115
Thornton, CO 80229 FAX : 303-280-0005

IEC
420 East 58th AVE — TEL : 303-292-5537
Denver, CO 80216 — FAX : 303-292-0114
IEC
5750 North Logan ST., — TEL : 303-292-6121
Denver, CO 80216 — FAX : 303-297-2053

JACO
695 Pierce Street — TEL : 303-828-3074
Erie, CO 80516 — FAX : 303-828-3080
MILGRAY
8787 Turnpike DR., STE #160 — TEL : 303-657-2750
Westminster, CO 80030 — FAX : 303-657-2952

CONNECTICUT

ALL AMERICAN
100 Mill Plain RD., #360 — TEL : 203-791-3816
Danbury, CT 6811 — FAX : 203-791-3801
BELL INDUSTRIES
1064 East Main ST., — TEL : 203-639-6000
Meridian, CT 1801 — FAX : 203-639-6005
MILGRAY
326 W. MAIN ST., — TEL : 203-878-5538
Milford, CT 6460 — FAX : 203-878-6970

FLORIDA

ADVENT
111 North Palm AVE., — TEL : 407-952-8669
Indialantic, FL 32903 — FAX : 407-984-2487
ADVENT
10500 NW 50th ST., #101 — TEL : 954-748-9781
Sunrise, FL 33351 — FAX : 954-748-9784
ALL AMERICAN
16115 N.W. 52nd AVE., — TEL : 305-620-7831
Miami, FL 33014 — FAX : 305-620-7831
ALL AMERICAN
14450 46th ST., #116 — TEL : 813-532-9800
Clearwater, FL 34622 — FAX : 813-538-5567
ALL AMERICAN
1400 E. Newport CTR. DR. #205 — TEL : 954-429-2800
Deerfield Beach, FL 33442 — FAX : 954-429-0391
ALL AMERICAN
16115 NW 52nd AVE., — TEL : 305-621-8282
Miami(Headquarters), FL 33014
BELL INDUSTRIES
650 S. Northlake BLVD., #400 — TEL : 407-339-0078
Altamonte Springs, FL 32701 — FAX : 407-339-0139
CHIP SUPPLY
7725 N. Orange Blossom Trail — TEL : 407-298-7100
Corlando, FL 32810 — FAX : 407-290-0164
JACO
9900 West Sample RD., #404 — TEL : 305-341-8280
Coral Springs, FL 33065 — FAX : 305-341-7848
MILGRAY
755 Rinehart RD., STE #100 — TEL : 407-321-2555
Lakemary, FL 32746 — FAX : 407-322-4225

GEORGIA

BELL INDUSTRIES
3850 Holcomb Bridge RD. Suite #110 — TEL : 770-446-2333
Norcross, GA 30092 — FAX : 770-446-7264
MILGRAY
3000 Northwoods PKWY., Suite #115 — TEL : 404-446-9777
Norcross, GA 30071 — FAX : 404-446-1186

ILLINOIS

ADVENT
1865 Miner ST., — TEL : 847-297-6200
Desplaines, IL 60016 — FAX : 847-297-6650
ALL AMERICAN
1930 N. Thoreau, Suite #200 — TEL : 847-303-1995
Schaumburg, IL 60173 — FAX : 847-303-1996
BELL INDUSTRIES
175 W. Central RD., — TEL : 847-202-6400
Schaumburg, IL 60195 — FAX : 847-202-5850
IEC
2401 W.Hassell RD., Suite #1505 — TEL : 847-843-2040
Hoffman Estates, IL 60915 — FAX : 847-843-2320
JACO
101 E. Commerce DR., — TEL : 847-884-6620
Schaumburg, IL 60173 — FAX : 847-884-7573
MILGRAY
1530 E. Dundee RD., — TEL : 847-202-1900
Palatine, IL 60067 — FAX : 847-202-1985

INDIANA

ADVENT
8446 Moller RD., — TEL : 317-872-4910
Indianapolis, IN 46268 — FAX : 317-872-9987
BELL INDUSTRIES
6982 Hillsdale Court — TEL : 317-842-4244
Indianapolis, IN 46250 — FAX : 317-570-1344
BELL INDUSTRIES
525 Airport No. Office Park — TEL : 219-490-2100
Fort Wayne, IN 46825 — FAX : 219-490-2104
MILGRAY
5226 Elmwood AVE., — FAX : 317-781-9997
Indianapolis, IN 46203 — FAX : 317-718-6970

IOWA

ADVENT
682 58TH AVE. CT. SW — TEL : 319-363-0221
Cedar Rapids, IA 52404 — FAX : 319-363-4514

KANSAS

ADVENT
9521 Mission RD., — TEL : 913-381-9003
Overland, KS 66206 — FAX : 913-381-0866
MILGRAY
6400 Glenwood, STE #313 — TEL : 913-236-8800
Overland Park, KS 66202 — FAX : 913-384-6825

MASSACHUSETTS

ALL AMERICAN
19C Crosby DR., — TEL : 617-275-8888
Bedford, MA 1730 — FAX : 617-275-1982
BELL INDUSTRIES
100 Burtt RD., #G01 — TEL : 508-623-3200
Andover, MA 1810 — FAX : 508-474-8902

JACO
1053 East ST., TEL : 508-640-0010
Tewksbury, MA 1876 FAX : 508-640-0755
MILGRAY
187 Ballardvale ST. TEL : 508-657-5900
Wilmington, MA 1887 FAX : 508-658-7989

MARYLAND

ALL AMERICAN
14636 Rothgeb DR., TEL : 301-251-1205
Rockville, MD 20850 FAX : 301-251-8574

BELL INDUSTRIES
8945 Guilford, RD., STE. 130 TEL : 410-290-5100
Columbia, MD 21046 FAX : 410-290-8006
JACO
10260 Old Columbia RD., TEL : 410-995-6620
Columbia, MD 21046 FAX : 410-995-6032
MILGRAY
6460 Dobbin RD., STE #D TEL : 410-730-6119
Columbia, MD 21045 FAX : 410-730-8940

MICHIGAN

ADVENT
24713 Crestview CT., TEL : 810-477-1650
Farmington Hills, MI 48335 FAX : 313-477-2630
ALL AMERICAN
39201 Schoolcraft RD., #B20 TEL : 313-464-2202
Livonia, Mi 48150 FAX : 313-464-2433

MINESOTA

ALL AMERICAN
7716 Golden Triangle DR., TEL : 612-944-2151
Eden Prarie, MN 55344 FAX : 612-944-9803
BELL INDUSTRIES
9401 James Avenue south, #142 TEL : 612-888-7747
Bloomington, MN 55431 FAX : 612-888-7757
JACO
10340 Viking DR., Suite #115 TEL : 612-941-2757
Eden Prarie, MN 55344 FAX : 612-941-1989

MISSOURI

ADVENT
1029 East Terra Lane TEL : 314-272-4281
O'Fallon, MO 63366 FAX : 314-272-2950

NEW JERSEY

ADVENT
600 Penn ST., TEL : 609-964-8560
Camden, NJ 8102 FAX : 609-964-0423
ALL AMERICAN
8. E. Stow RD., #100 TEL : 609-596-6666
Marlton, NJ 8053 FAX : 609-797-1700
BELL INDUSTRIES
271 Route 46 West, Suites #F202-203 TEL : 201-227-6060
Fairfield, NJ 7004 FAX : 201-227-2626
BELL INDUSTRIES
158 Gaither DR., STE. #110 TEL : 609-439-8860
MT. Laurel, NJ 8054 FAX : 609-439-9009
MILGRAY
523 Fellowship Rd., STE #275 TEL : 609-778-1300
MT. Laurel., NJ 8054 FAX : 609-778-7669
MILGRAY
3799 Route 46 East Suite #303 TEL : 201-335-1766
Parsippany, NJ 7054 FAX : 201-335-2110

NEW YORK

ALL AMERICAN
275B Marcus BLVD. TEL : 516-434-9000
Hauppauge, NY 11788 FAX : 516-434-9394
ALL AMERICAN
333 Metro Park TEL : 716-292-6700
Rochester, NY 14623 FAX : 716-292-6755
BELL INDUSTRIES
300 Vanderbilt Motor PKWY, TEL : 516-435-8910
Suite #217, Hauppauge, NY 11788 FAX : 516-435-8913
JACO
145 Oser AVE. TEL : 516-273-5500
Hauppauge, NY 11788 FAX : 516-273-5799
MILGRAY
77 Schmitt BLVD., TEL : 516-391-3000
Farmingdale, NY 11735 FAX : 516-420-0685
MILGRAY
1170 Pittsford-Victor RD., Suite #200 TEL : 716-381-9700
Pittsford, NY 14534 FAX : 716-381-9495

NORTH CAROLINA

BELL INDUSTRIES
3100 Smoketree Court, STE. 800 TEL : 919-874-0011
Raleigh, NC 27604 FAX : 919-874-0013
JACO
5206 Greens Dairy RD., TEL : 919-876-7767
Raleigh, NC 27604 FAX : 919-876-6964

OHIO

ALL AMERICAN
26650 Renaissance PKWY. TEL : 216-514-0625
Warrenville Heights, OH 44128 FAX : 216-514-0822
BELL INDUSTRIES
31200 Solon RD., Suite 12 TEL : 216-498-2002
Solon, OH 44139 FAX : 216-498-2006
BELL INDUSTRIES
444 Windsor Park DR., TEL : 513-435-5922
Dayton, OH 45459 FAX : 513-435-3122
BELL INDUSTRIES
446 Windsor Park DR., TEL : 513-434-8231
Dayton, OH 45459 FAX : 513-434-8103
MILGRAY
6155 Rockside RD., STE #206 TEL : 216-447-1520
Cleveland, OH 44131 FAX : 216-447-1761

OREGON

ALL AMERICAN
1815 NW 169th PL., Suite #6025 TEL : 503-531-3333
Beaverton, OR 97006 FAX : 503-531-3695
BELL INDUSTRIES
8705 SW Nimbus AVE., STE. #100 TEL : 503-644-3444
Portland, OR 97008 FAX : 503-520-1948
IEC
3720 S.W. 141st ST., 102 TEL : 503-641-1690
Beaverton, OR 97005 FAX : 503-646-3737

JACO
4900 SW Griffith DR., #129 TEL : 503-626-1439
Beaverton, OR 97005 FAX : 503-626-0979
MILGRAY
8705 S.W.Nimbus AVE., TEL : 503-626-4040
Beaverton, OR 97008 FAX : 503-641-0650

TEXAS

ALL AMERICAN
13706 Research BLVD., STE. #103 TEL : 512-335-2280
Austin, TX 78750 FAX : 512-335-2282
ALL AMERICAN
11210 Steeplecrest, #206 TEL : 713-955-1993
Houston, TX 77065 FAX : 713-955-2215
ALL AMERICAN
1771 International Pkwy, #101 TEL : 214-231-5300
Richardson, TX 75081 FAX : 214-437-0353
BELL INDUSTREIS
14110 Dallas Parkway, Suite #170 TEL : 214-248-0047
Dallas, TX 75240 FAX : 214-404-0267
BELL INDUSTRIES
10700 Richmond, Suite #263 TEL : 713-974-2111
Houston, TX 77042 FAX : 713-974-2125
JACO
2120 A-Braker Lane TEL : 512-835-0220
Austin, TX 78758 FAX : 512-339-9252
JACO
1209 N Glenville DR., TEL : 214-234-5565
Richardson, TX 75081 FAX : 214-238-7068
MILGRAY
11824 Jollyville RD., TEL : 512-331-9961
Austin, TX 78759 FAX : 512-331-1070
MILGRAY
16610 N. Dallas PKWY., TEL : 972-248-1603
Dallas, TX 75248 FAX : 972-248-0218
MILGRAY
12000 Richmond AVE., STE #310 TEL : 713-870-8101
Houston, TX 77082 FAX : 713-870-8122

UTAH

ALL AMERICAN
6955 Union Park Center, #101 TEL : 801-565-8300
Midvale, UT 84047 FAX : 801-565-9983
BELL INDUSTRIES
6912 S.185 West, Suite B TEL : 801-561-9691
Midvale, UT 84047 FAX : 801-255-2477
IEC
2117 South 3600 West TEL : 801-977-9750
West Valley City, UT 84119 FAX : 801-975-1207
MILGRAY
310 E. 4500 S, STE. #110 TEL : 801-261-2999
Murray, UT 84107 FAX : 801-261-0880

WASHINGTON

ALL AMERICAN
11807 Northcreek PKWY. S.#112 TEL : 206-806-4800
Bothel, WA 98011 FAX : 206-806-9900
BELL INDUSTRIES
19119 N. Creek PKWY., STE.#102 TEL : 206-646-8750
Bothell, WA 98004 FAX : 206-646-8559

IEC
1750 124th AVE, N.E. TEL : 206-455-2727
Bellevue, WA 98005 FAX : 206-453-2963
JACO
17220 127th Place NE, #300 TEL : 206-481-3372
Woodinville, WA 98072 FAX : 206-481-1664

WISCONSIN

ADVENT
237 South Curtis RD., TEL : 414-475-6860
West Allis, WI 53214 FAX : 414-475-0440
ALL AMERICAN
18000 Sarah Lane, Suite #145 TEL : 414-792-0436
Brookfield, WI 53045 FAX : 414-792-9733
BELL INDUSTRIES
W. 226 N.900 Eastmond DR., TEL : 414-547-8879
Waukesha, WI 53186 FAX : 414-547-6547

• • • • •

SAMSUNG SEMICONDUCTOR SALES OFFICE-EUROPE

Central Europe

Samsung Semiconductor Europe Gmbh
Am Kronberger Hang 6 — TEL : 06196-663-300
65824 Schwalbach — FAX : 06196-663-311

MUNICH

Samsung Semiconductor Eurpoe Gmbh
Representative Office
Carl-Zeiss-Ring 9 — TEL : 089-964838
85737 Ismaning — FAX : 089-964873

UK-Hinckley Birmingham

Samsung Semiconductor Europe LTD
Representative Office
Florence House St.Marys Road — TEL : 00441-455-891111
Hinckley LEICS LE10 1EQ — FAX : 00441-455-612345

UK-London

Samsung Semiconductor Europe LTD
Semiconductor Division
2nd Fl., Great West House, — TEL : 00441-81-380-7200
Great West Road, — FAX : 00441-81-380-7220
Brentford, Middlesex TW8 9DQ

Scotland Glasgow

Samsung Semiconductor Europe Gmbh
Representative Office
Trojan House, Phoenix — TEL : 00441-41-840-2424
Business Park, — FAX : 00441-41-840-4747
Paisley PA1 2BH, Scotland

Ireland Dublin

Samsung Semiconductor Europe Gmbh
Representative Office
Block 8, St. John's Court, — TEL : 00353-1-8621688
Swords Road, Santry, Dublin 9, — FAX : 00353-1-8621684
Ireland

France Paris

Samsung Semiconductor France S.A.R.L
Centre d'affaires la, — TEL : 0033-1-46017181
Boursidiere RN 186, BAT. — FAX : 0033-1-40940216
Bourgogne, BP202, F-92357 Le,
Plessis-Robinson

Italy Milan

Samsung Semiconductor Italia S.A.R.L
Procaccini Center, Via Messina, 38 — TEL : 0039-234578231
20154 Milano — FAX : 0039-233604027

Nordic Stockhoim

Samsung Semiconductor Europe Gmbh
Representative Office
Johanneslundsvagen4 — TEL : 0046-8-59410841
S-194 81 Upplands Vasby — FAX : 0046-8-59410849
Belgium Brussels
Buro & Design Center — TEL : 0032-24740852
Heyzel Esplanade, Loc 524 Box 47 — FAX : 0032-24740851
1120 Brussel

Spain

Samsung Semiconductor Europe Gmbh
Representative Office
Edificio samsung Electronica 1st Fl., — TEL : 0034-3-2616700
Ciencies, 55- 65, Pol. Pedrosa, — FAX : 0034-3-2616790
08908 Hospitalet de Llobregat

Turkey

Samsung Semiconductor Europe Gmbh
Representative Office
Bahariye Caddesi, Dr.Dilemre — TEL : 0090-216-3488557
Is Merkezi — FAX : 0090-216-3483964
No 80/7 81300 Kadikoy,Istanbul, Turkey

SAMSUNG SEMICONDUCTOR DISTRIBUTORS-EUROPE

Austria

SEI-Elbatex Ges
Eitnergasse 6, TEL : 1866420
A-1230, Wien FAX : 186642201

Belgium

AVER S.A.
Zoning Gosset, Avenue Gossetlaan 15, TEL : 2-4633414
B-1702, Groot-Bijgaarden FAX : 2-4632219
Malchus Belgium
Generaal de Wittelaan 9/14 TEL : 15-287898
B-2800, Mechelen FAX : 15-287890

Denmark

Arrow-Exatec
Mileparken 20E TEL : 449-27000
DK-2740 Skovlunde FAX : 449-26020
Future Electronics TEL : 961-00961
Holstebro FAX : 961-00962

East Europe

Eltron Electronic
Ul. Szewska 3, PL-50-053 TEL : 71-442532
Wroclaw FAX : 71-441141
Future Electronics TEL : 226189202
Warszawa FAX : 226188050
GM
Karlinske Nam.6 TEL : 2-2322606
CZ-18600 Prag 8 FAX : 2-2321194

Finland

Computer 2000 Finland
P.O.Box 44 (Pyyntitie 3) TEL : 3589-8873330
FIN-02231, Espoo FAX : 3589-88733289
Future Electronics TEL : 3589-5259950
Espoo FAX : 3589-4551050

FRANCE

Arrow-Computer Products
7, Avenue du Canada, TEL : 1-60926060
Z.A.de Courtaboeuf FAX : 1-60926020
F-91966, Les Ulis Cedex
Arrow-CCI Electronique
12, Allée de la Vierge; Silic 577 TEL : 1-41807000
F-94653, Rungis Cedex FAX : 1-46753207
Future Electronics
3 Avenue du Canada-Bat. TEL : 1-69821111
Theta 2; L.P. 854 Les Ulis FAX : 1-69821100
F-91974, Courtabeuf Cedex
SEI-Scaib
6, Rue Ambroise Croizat TEL : 1-69198900
Z.A.E. Les Glaises FAX : 1-69198920
F-91127 Palaiseau Cedex

Germany

Arrow-Spoerle Electronic
Max-Planck-Str. 1-3 TEL : 6103-3040
D-63303, Dreieich FAX : 6103-304201
Autronic-Melchers
An der Roßweid 18 TEL : 721-962640
D-76229, Karlsruhe FAX : 721-9626480
Distec
Industriestr. 1, TEL : 89-8943630
D-82110, Gemering FAX : 89-89436339
Future Electronics
Münchner Str. 18 TEL : 89-957270
D-85774, Unterföhring FAX : 89-95727173
Micronetics
Dieselstr. 12 TEL : 7259-925830
D-71272, Renningen FAX : 7159-9258355
MSC HQ
Industriestr. 16 TEL : 7249-9100
D-76297, Stutensee FAX : 7249-4232
SEI-Jermyn
Kapellenstr. 15 TEL : 6431-508-220
D-65555, Limburg FAX : 6431-54662

ISRAEL

Data JCE
3, Hashikma Str. TEL : 3-5583318
IR-58001, Azor FAX : 3-5583325

ITALY

Arrow-Claitron
Viale Fulvio Testi, 280/B TEL : 2-661251
I-20126, Milano FAX : 2-66105666
Eurodis Fanton
Via Melegnano 22 TEL : 2-48920341
I-20019, Settimo Milanese(MI) FAX : 2-4597913
Future Electronics
Via Fosse Ardeatine, 4 TEL : 2-660941
I-20092, Cinisello Balsamo Milano FAX : 2-66012843
Kerr Technology Bridge
Piazza Toscana 1 TEL : 2-90782053
I-20090, Peive Emanuele Milano FAX : 2-90781663
Rafi Electronica
Via Savona 134 TEL : 2-4779181
I-20144, Milano FAX : 2-428880
SEI-Sonelco
Via Monfalcone, 15 TEL : 2-66011349
I-20092 Cinisello Balsamo Milano FAX : 2-66011295

Netherlands

Future Electronics TEL : 765444888
Breda FAX : 765444880
Malchus
Fokkerstraat 511-513 TEL : 10-2452452
NL-3125 BD Schiedam FAX : 10-5154466

Planhold Computers
Hoogdreef 68 TEL : 20-4303030
NL-1101, BE Amsterdam FAX : 20-6964699
Ronin Nederland
Poldermolen 4 TEL : 1-786414022
NL-3352, TH Papendrecht FAX : 1-786413164
SEI-Sonetech Netherland
Takkebijsters 2 TEL : 765722333
NL-4817, BL Breda FAX : 765722395
SPaSE
Kerkenbos 1021 TEL : 24-378-2882
NL-6546 BB Nijmegen FAX : 24-378-8388

Norway
Future Electronics TEL : 22-905800
Oslo FAX : 22-905790
SEI-Jakob Hatteland
Postbox 25 TEL : 53-763000
N-5578 Nedre Vats FAX : 53-765339

Spain
Arrow-Amitron
Albasanz, 75 TEL : 1-3043040
E-28037, Madrid FAX : 1-3272472
ATD Electronica
Albasanz, 75 TEL : 1-3041534
E-28037, Madrid FAX : 1-3272778
Iberica de Componentes
Avda, Somosierra, 11; 1 Of A. TEL : 1-7373671
E-28709, San Sebastian de Los Reyes FAX : 1-7375464
SEI-Selco
Ctra de la Coruna N-VI TEL : 1-6371011
KM 18200 Via de Servicio FAX : 1-6371506
E-28230, Las Rozas de Madrid
SIDSA
Isaac. Newton, 1 TEL : 1-8035052
E-28760 Tres Cantos, Madrid FAX : 1-8039557

Sweden
Arrow-Microtronica
Ellipsvägen 5 TEL : 8-6807800
S-14175, Huddinge FAX : 8-74044515
Future Electronics TEL : 8-279479
Solna FAX : 8-822833
Ingram Micro
Kronborgsgränd 1 TEL : 8-7525400
S-16487, Kista FAX : 8-7039348
Miko Komponent
Segersbyvaegen 3 TEL : 853-1-93900
S-14502 Norsborg FAX : 853-1-93939

Swiss
Primelco
Blegistrasse 23, TEL : 41-7670170
CH-6342, Baar FAX : 41-7670179
SEI-Elbatex
Hardstr. 72 TEL : 564375111
CH-5430, Wettingen FAX : 564375454

UK
Arrow-Jermyn
Cambride Road, TEL : 1-234270027
UK-MK42 0LE, Bedford FAX : 1-234791786
Assured Technologies
581 London Road TEL : 181-7580758
UK-TW7 4EJ, Middlesex; Isleworth FAX : 181-7580708
Future Electronics HQ
Future House, Poyle Road, Colnbrook TEL : 1-753-763000
UK-SL3 0EZ, Berkshire FAX : 1-753-689100
Just Rams
Unit 6, Iron Bridge Business Park, TEL : 1-814517766
GT Cent Way, UK-NW10 0UW, FAX : 1-814596301
London
Magnatec/Semelab
Coventry Road, Lutterworth TEL : 1-455-554711
UK-LE17 4JB, Leicestershire FAX : 1-455-558843
MSC
Pavillion House, 6/7 Old Steine Sussex TEL : 1273-622446
UK-BN1 1EJ, Brighton FAX : 1273-622533
Oxford Semiconductors
68, Milton Park TEL : 1-235861461
UK-OX14 4RX, Abingdon Oxfordshire FAX : 1-235821141
SEI-2001
Stevenage Business Park, TEL : 1-438742001
Pin Green-Stevenage, FAX : 1-438742002
UK-SG1 4SU, Herts
Dondene/Transonics
Woodside Place, Mount Pleasant TEL : 1-819001334
UK-HA0 1UW, Wembley/Middlesex FAX : 1-819002040

• • • • •

SAMSUNG SEMICONDUCTOR REPRESENTATIVES-ASIA

HONG KONG

AV. CONCEPT LTD
Unit 11-15, 11fl., Block A, TEL : 2334-7333
Focal Industrial Centre FAX : 2764-3108
21 Man Lok Street, Hunghom,Kowloon, Hong Kong

PROTECH COMPONENTS LTD
Unit 2, 3fl., Wah Shing Centre, TEL : 2950-2888
11 Shing Yip Street, FAX : 2950-2828
Kwun Tong, Kowloon,Hong Kong

WISEWORLD ELECTRONICS LTD
Room 708, Tower A, 7fl., TEL : 2765-8923
Hunghom Commercial Centre, FAX : 2363-6203
31-39 Ma Tau Wai Road, Honghom, Hong Kong

CENTENNIAL ELECTRONICS LTD
Unit 2, 23fl., Westlands Center, TEL : 2565-5898
No.20 Westlands Road., FAX : 2564-5411
Quarry Bay, Hong Kong

SOLARBRITE ELECTRONICS LTD (CALCULATOR & WATCH)
Unit 1, 11fl., Tower 1, TEL : 2363-3233
Horbour Centre 1, Hok Cheung St., FAX : 2363-3900
Hunghom, Kowloon,Hong Kong

ATLANTIC COMPONENTS LTD (MEMORY & PC)
Unit 502, 5fl., Tower 3, TEL : 2799-1996
Enterprise Square,9 Sheung Yuet Rd, FAX : 2755-9452
Kowloon Bay,Kowloon, Hong Kong

SAMTEK SEMICON DEVICES H.K LTD
Room 2104, Windsor House 311 TEL : 2890-7933
Gloucester Road., Causeway Bay, FAX : 2890-7890
Hong Kong

Li SENG TECHNOLOGY LTD
Flat B&C. 6fl., TEL : 2540-8348
Four Seas Comm. Bank Bldg FAX : 2547-5706
49-51 Bonham Strand West, Hong Kong

LEGEND-VALENCE SEMICONDUCTOR DESIGN LTD
Units 1-7, 19F, Apec Plaza TEL : 2656-1151
49 Hoi Yuen Road, Kwun Tong, FAX : 2652-2301
Kowloon, Hong Kong

MACRO LONG DELEVELOPMENT LTD
Room 1008, 1 Hung To Road., TEL : 23575780
Kwan Long, Kowloon, Hong Kong FAX : 27935697

TAIWAN

YOSUN INDUSTRIAL CORP
7FL., No76 SEC 1, Cheng Kung Rd., TEL : 02-788-1991
Nan Kang, Taipei, R.O.C FAX : 02-788-1996

SANT SONG CORP.
4FL., No.12, Lane 94, Tsao TEL : 02-662-7829
Ti Wei, Shen Keng Hsiang FAX : 02-662-0781
Taipei, Hsien, Taiwan, R.O.C.

SUPREME ELECTRONICS CO., LTD.
18FL.,NO.67 Section 2, TEL : 02-7023258/7023278
Tun Hwa S. Road, FAX : 02-7063196
Taipei, Taiwan, R.O.C.

JAPAN

TOMEN DEVICES CORP.
10-15, Horidome-Cho, 1 Chome, TEL : 03-5640-1386
Nihonbashi Chuo-Ku, Tokyo103 Japan FAX : 03-5640-8583

RIKEI SEMICONDUCTOR CORP.
Meiji Seimei Bldg., TEL : 03-3490-2173
2-27-4, Nishi-Gotanda, FAX : 03-3490-2179
Shinagawa-Ku Tokyo 141 Japan,

ISECO
2-26-3, Kitamagome 2-Chome, TEL : 03-3777-3611
Ota-Ku, Tokyo, 143 Japan FAX : 03-3777-3614

SINGAPORE

SAMSUNG ASIA PTE LTD. MALAYSIA LIAISON OFFICE
9-2 Menara Penang Garden, TEL : 604-2291671
42-A, Jalan Sultan Ahmad Shah FAX : 604-2291678
10500 Penang, Malaysia

SAMSUNG ASIA PTE LTD. BANGALORE LIAISON OFFICE
10FL., Prestige Meridian Building TEL : 9180-555-0555
No.29 M,G,Road, FAX : 9180-555-0558
Bangalore-560 001, India

SAMSUNG ASIA PTE LTD. NEW DELHI LIAISON OFFICE
11FL., DR Gopal Das Bhawan TEL : 9111-3720340~2
28 Barakhamba Road, FAX : 9111-3755390
New Delhi-110001, India

Astina Electronics(S) PTE LTD.
203B Henderson Road, TEL : 276-9997
#12-08, Henderson Industrial Park, FAX : 276-9996
Singapore 159548

Bostex Electronics PTE LTD.
219 Henderson Road, TEL : 339-0713
#10-01, Henderson Industrial Park FAX : 338-9536
Singapore 159556

YIC Singapore PTE LTD.
159 Sin Ming Road, TEL : 552-4811
#04-04, Amtech Building FAX : 552-5811
Singapore 575625

Samtek Semicon Devices(S) PTE LTD.
80, Robinson Road, TEL : 225-9177
#16-01, Singapore 068898 FAX : 225-9477

Samtek Semicon Devices New Delhi Liaison Office
Hotel Samrat, #582,Chanakyapuri, TEL : 687-1723
New Delhi-110021, India FAX : 687-1725

South West Electronics PTE LTD.
159 Sin Ming Road, TEL : 553-3118
#04-03, Amtech Building FAX : 553-3008
Singapore 575625

Tomen Devices Corporation Singapore Branch
10 Shenton Way, TEL : 221-1422
#16-02, MAS building FAX : 221-0400
Singapore 079117

Rikei Corporation(S) PTE LTD.
15 Scotts Road, TEL : 235-2427
#03-11, Thong Tech Building FAX : 235-2463
Singapore 228218

Vutipong Technology Co., LTD.
47-49 Pahurat Road, TEL : 662-2266496
Bangkok, Thailand 10200 FAX : 662-2240861

CHINA

Centennial Electronics LTD. (Shanghai Office)
Room 808, Area B, TEL : 021-64810697
Yin Hai Comm. Bldg, FAX : 021-64824668
250 Cao Xi Road, Xu Hui District,
Shanghai, P.R.C

Centennial Electronics LTD. (Shenzhen Office)
Unit 10, 22Fl., Oriental Bldg., TEL : 0755-2284262
39 Jianshe Road., Shenzhen, FAX : 0755-2282536
Guangdong, China

Qinghua-Samsung MICOM Software House (Dept of Electronics)
Qinghua Yuan, TEL : 01-2594785
Beijing, China FAX : 01-2594176

Suman Electronics Products Co.,
Room `117, Technology Trading Center TEL : 01-6846-7032~4
No.37 Bai Qiao Road,Beijing, China FAX : 01-6846-7035

Suman Electronics (Tianjin Office)
No.203-205, HongQi Road, TEL : 022-451-6680/1
Nankai District, Tianjin, China FAX : 022-451-6680

Suman Electronics (Hangzhou Office)
No.27, Wen-San Road, TEL : 0571-803607/5
Hangzhou City, China FAX : 0571-806-6087

Suman Electronics (Nanjing Office)
No.8 Shitiao Xiang, Gulou, TEL : 025-3364473/4578
Nanjing, China FAX : 025-336-4658

Suman Electronics (Xian Office)
No.106 Frengging Road, TEL : 029-4262014
Xian, China FAX : 029-4262306

AUSTRALIA

SAMSUNG CO., Ltd.
Level 20, Northpoint Bldg., TEL : 61-2-9955-3888
100 Miller Street, North Sydney, FAX : 61-2-9955-4233
NSW 2060 Australia

KOREA

Sechang Semiconductor Co., LTD.
4FL., Chung-Lim Bldg., TEL : 02-597-8121
924-13, Bangbae 1-Dong, TEL : 0551-84-3743
Seocho-Ku, Seoul, Korea FAX : 02-525-9762

Samsung Light-Electronics Co., LTD.
4FL., Room 2-3, Electronicland TEL : 02-718-0045
Main Bldg., TEL : 02-718-0931~5
16-9, Hankangro 3-Ka, FAX : 02-718-9536
Yongsan-Ku, Seoul, Korea

Sinsung Semiconductor Co., LTD.
5FL., Electronicland Bldg., TEL : 02-3272-9300
1-1, Hankangro 3-Ka, FAX : 02-718-8534~5
Yongsan-Ku, Seoul, Korea

Hankook Semiconductor & Telecommunications Co., LTD.
3FL., Sungwon Bldg., TEL : 02-539-4123
119-3, Samsun-Dong, Kangnam-Ku, FAX : 02-508-8558
Seoul, Korea

Samtek Corp.
4Fl., ChungLim Bldg., TEL : 02-3458-9000
154-16, Samsung-Dong, FAX : 02-3458-9300
Kangnam-Ku, Seoul, Korea

Sunin Trading Co., LTD.
7FL., Sunin Bldg., TEL : 02-702-1257~8
16-8, Hankangro 2-Ka, FAX : 02-704-0997
Yongsan-Ku, Seoul, Korea

Mujin Electronics Co., LTD.
Sambo Bldg.,13-2, Yeuido-Dong TEL : 02-783-4890
Youngdeungpo-Ku, Seoul, Korea FAX : 02-785-7661

Ghilwon Electronics Co., LTD.
6FL., NamPung Bldg., TEL : 02-784-9966~7
13-19, Yeuido-Dong, FAX : 02-784-9968
Youngdeungpo-Ku, Seoul, Korea

• • • • •

NOTES

NOTES

HEAD OFFICE
8/11FL., SAMSUNG MAIN BLDG.
250, 2-KA, TAEPYUNG-RO,
CHUNG-KU, SEOUL, KOREA
TEL : 2-727-7114
FAX : 2-753-0967

SEMICONDUCTOR BUSINESS SALES & MARKETING DIVISION:
15/16FL., SEVERANCE BLDG.,
84-11, 5-KA, NAMDAEMOON-RO,
CHUNG-KU, SEOUL, KOREA
TEL : 2-259-1114
FAX : 2-259-2468

SAMSUNG SEMICONDUCTOR INC.
3655 NORTH FIRST STREET,
SAN JOSE, CA 95134, U.S.A.
TEL : 408-954-7000
FAX : 408-954-7873

SAMSUNG SEMICONDUCTOR EUROPE GMBH
SAMSUNG HOUSE,
AM KRONBERGER HANG 6,
65824, SCHWALBACH/TS
TEL : 49-6196-663300
FAX : 49-6196-663311

SAMSUNG SEMICONDUCTOR EUROPE LTD.
GREAT WEST HOUSE
GREAT WEST ROAD, BRENTFORD
MIDDLESEX TW8 9DQ
TEL : 181-380-7132
FAX : 181-380-7220

SAMSUNG ELECTRONICS JAPAN CO., LTD.
HAMACHO CENTER BLDG.,
31-1, NIHONBASHI-HAMACHO, 2-CHOME,
CHUO-KU, TOKYO 103, JAPAN
TEL : 3-5641-9850
FAX : 3-5641-9851

SAMSUNG ELECTRONICS HONG KONG CO., LTD.
65TH FL., CENTRAL PLAZA,
18 HARBOUR ROAD,
WANCHAI, HONG KONG
TEL : 852-2862-6900
FAX : 852-2866-1343

SAMSUNG ELECTRONICS TAIWAN CO., LTD.
30FL., NO.333 KEELUNG RD.,
SEC 1, TAIPEI, TAIWAN, R.O.C.
TEL : 886-2-757-7292
FAX : 886-2-757-7311

SAMSUNG ASIA PRIVATE LIMITED
80 ROBINSON ROAD, #20-01,
SINGAPORE 068898
TEL : 65-535-2808
FAX : 65-227-2792

SAMSUNG ELECTRONICS CO., LTD. SHANGHAI OFFICE
9F, SHANHAI INTERNATIONAL TRADE CENTRE
NO.2200 YANAN(W) RD.
SHANGHAI, P.R.C 200335
TEL : 8621-6270-4168
FAX : 8621-6275-2975

SAMSUNG ELECTRONICS CO., LTD. SEMICONDUCTOR BUSINESS BEIJING OFFICE
15FL., BRIGHT CHINA CHANG AN BLDG.,
NO.7, JIANGUOMEN, NEI AVENUE,
BEIJING, CHINA 100005
TEL : 8610-6510-1234(0)
FAX : 8610-6510-1545